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SiGe Millimeter-Wave (W-Band) Down-Converter for Phased Focal Plane Array

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A Thesis Presented

by

MARUTHI NAGAVALLI YOGEESH

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ABSTRACT

SiGe MILLIMETER-WAVE (W-BAND) DOWN-CONVERTER FOR PHASED FOCAL PLANE ARRAY

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A millimeter-wave (W-Band) down-converter for phased focal plane arrays (PFPAs) has been designed and fabricated using the IBM Silicon-Germanium (SiGe) BiCMOS 8HP process technology. The radio frequency (RF) input range of the down-converter chip is from 70GHz to 95GHz. The intermediate frequency (IF) range is from 5 to 30GHz. The local oscillator (LO) frequency is fixed at 65GHz. The down-converter chip has been designed to achieve a conversion gain greater than 20dB, a noise figure (NF) below 10dB and input return loss greater than 10dB. The chip also has novel LO circuitry facilitating LO feed-through among down-converters chips in cascade. This

wide bandwidth down-converter will be part of millimeter-wave PFPA receiver designed and fabricated in collaboration with the University of Massachusetts-Amherst Department of Astronomy. This PFPA receiver will be installed on Green Bank Telescope (GMT) / Large millimeter wave telescope (LMT) in Q2 of 2014. This project is collaboration between the University of Massachusetts-Amherst (UMass), Brigham Young University (BYU) and National Radio Astronomy Observatory (NRAO).

To the best of the author's knowledge, this will be the first wide bandwidth down-converter at W-band to achieve this high gain and low noise figure among Si/SiGe based systems.

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CHAPTER 1

INTRODUCTION AND BACKGROUND MATERIAL

This thesis is about the design of a SiGe BICMOS mm-wave (W-band) down-converter for phased focal plane array (PFPA) receivers. The PFPA which is currently under design is expected to be installed on Green Bank Telescope (GBT) / Large millimeter wave Telescope (LMT) in Q2 of 2014. This design represents the first very wideband (25GHz), low-noise and high gain W-band down-converter chip designed and fabricated using SiGe BiCMOS process technology. The chip also has on-chip LO driver circuitry for LO feed through between down-converter chips operating in cascade. This feature makes LO routing much simpler, which helps in the design of very complex and compact array receivers. The PFPA receiver design is a collaborative project between The University of Massachusetts-Amherst[1] (UMass), Brigham Young University[2] , and the National Radio Astronomy Observatory (NRAO). UMass is involved with the design and fabrication of PFPA hardware (Frontend, Down-converters, IF modules, etc..), BYU is responsible for the baseband signal processing, and NRAO is providing research assistance with regard to GBT installation and testing.

[1] The UMass team is lead by Professors N.Erickson, G.Narayanan, and J.Bardin

[2] The BYU team is lead by Professors B. Jeffs and K. Warnick

This chapter is divided into five sections:

1) **Millimeter-wave radio frequency systems (Section 1.1)** - This section gives an introduction to mm-wave systems, ongoing research in this area and some of the novel applications using these systems in areas such as astronomy, imaging, radars and communication.
2) **Process technology for millimeter wave integrated systems (Section 1.2) –** This section discusses the SiGe process technology used for fabrication of mm-wave down-converters. It also discuss about how this process technology is different from standard Si-CMOS and III-V processes.
3) **Introduction to PFPA's (Section 1.3)** - This section covers the phased focal plane array receiver, how it is different from a conventional focal plane arrays (FPA) and the ongoing research in this area.
4) **PFPA Architecture (Section 1.4)** - This section discusses the PFPA architecture currently being designed and fabricated here at University of Massachusetts-Amherst. This section also gives an overview of the important role played by the SiGe millimeter-wave (W-band) down-converter from a overall systems point of view.
5) **Introduction to SiGe mm-wave (W-band) down-converters (Section 1.5)** - This section discusses the main thesis topic - the SiGe mm-wave (W-band) down-converter. It also discusses the goals to be met by this down-converter, the system level implementation and presents a comparison with already existing research works.

1.1 Millimeter-Wave Radio Frequency Systems

The millimeter-wave radio frequency band spans from 30 to 300GHz [1]. This band has recently been explored for many applications such as astronomical observations, medical imaging, weather and collision avoidance radar systems, and gigabit communications. Atmospheric absorption in this frequency band is shown in Fig. 1.1 [2]. Due to higher absorption by the earth's atmosphere, the range of mm-wave signals in some bands, such as from 50GHz to 60GHz, is limited to a few meters [1]. This characteristics of mm-waves is very attractive for near-field imaging and gigabit communication over short distances, where ensuring security of information is of critical importance. The mm-wave frequency range is relatively unused and is therefore largely free from interference when compared to today's standard low freqeuncy communication bands. It also provides users with a large available bandwidth [2]. The Federal Communication Commision (FCC) has assigned a license free band between 57 – 64GHz for industrial, scientific and medical (ISM) research applications [2]. This makes it very attractive for designing next generation electronic systems operating in this frequency band.

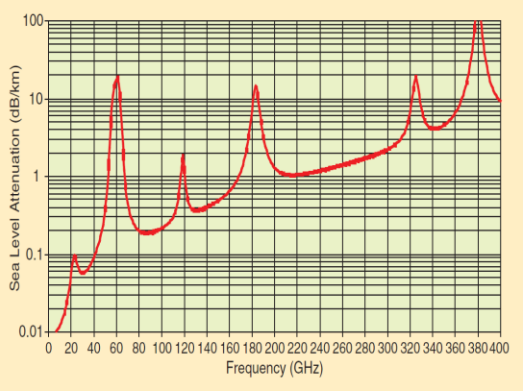


Figure 1.1: Atmospheric attenuation of electromagnetic waves. Reproduced from [2]

1.1.1 Applications of mm-wave RF systems

- **Astronomy**

The millimeter-wave frequency range is of great interest to astronomers. The International Astronomical Union (IAU) has listed important spectral lines of interest for mm-wave astronomy. Some of the prominent spectral lines are Carbon monoxide, Formic acid (CH3OH), Deuterated water (HDO), and Cyanamid (NH2CN) [3][4]. The frequency bands of these spectral lines are protected. So no satellite transmitters are allowed to emit at these frequency bands [3]. By observing these molecular spectral lines, astronomers can characterize the galaxies and, the formation of stars and dark clouds [4].

A simplified mm-wave radio telescope is shown in Fig 1.2. A large primary reflector is employed to collect the electromagnetic signal from outer space. The focus of the primary reflector is the antenna array and receiver system. The signals received by the antenna array are amplified and down converted to a lower frequency by the receiver electronics, which consists of low noise amplifiers, mixers and filters. The receiver electronics should have very high gain and very low noise since the amplitude of the astronomical signal is very low (-70dBm). This low frequency signal is then digitized and processed. The digitization is done using a high speed Analog to digital converter (ADCs). The digital signal is then processed and stored using super computers [5].

Many millimeter-wave radio telescopes have been built around the world. Some prominent examples are the Green Bank Telescope (GBT), the Atacama Large Millimeter Array (ALMA), the South Pole telescope (SPT), the DeLingha in China, the GaLenki RT-70 in Russia and the Effelsberg in Germany [6].

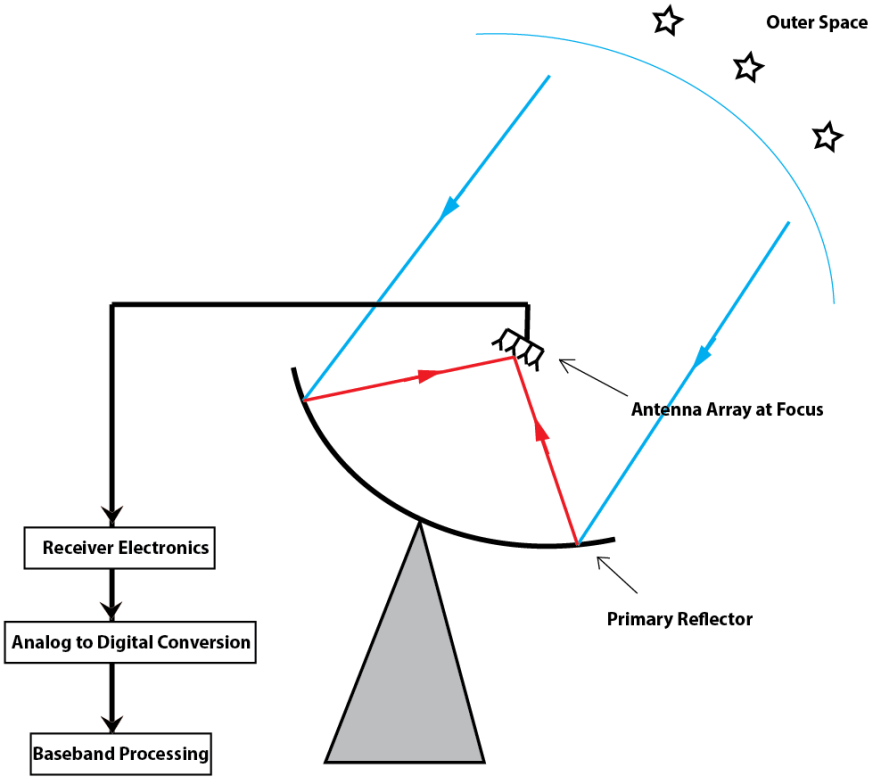


Figure 1.2: Radio telescope and associated receiver electronics

- **Millimeter wave Imaging**

Millimeter-wave radiation is reflected and transmitted quite differently by materials of different dielectric constants. This property of millimeter-waves has recently been explored for imaging application[8]. Research groups at MIT, UMass-Amherst, and Tufts have shown the advantage of using mm-waves for Breast Cancer imaging [7]. The advantage of millimeter-wave imaging systems is that they are non ionizing and non radioactive [7].

Millimeter-wave imaging is also being employed by airport security personal (TSA) for detection of illegal materials. L3-ProVision has designed a mm-wave

automatic target detection (ATD) system which can image a person for illegal objects. In this system they have multiple millimeter-wave transreceivers placed at different azimuth and elevation angles to enable 3-D imaging.

- **Gigabit communication**

Millimeter waves in certain frequency bands travel very short distance (10 - 15m) before getting attenuated due to atmospheric absorption. This property permits secure communications. Moreover the large available bandwidth at millimeter-wave frequencies makes it the best candidate for near distance giga bit comunication. Recently researchers have demonstrated new millimeter wave transreceivers which when integrated with cell phones, modems, laptops could completely overcome the need to connect by Cables (HDMI, USB) for large data transfer[10]. Researchers at Industries and Universities are working towards developing low power mobile systems which operate in the mm-wave band for data transfer[10][11]. Electronic devices could share videos and data wirelessly at giga bits per second [11].

- **Radar systems**

Millimeter-wave radars have higher sensitivity and resolution compared to microwave based radars. This is due to shorter wavelength. This feature is very useful for remote sensing. Fig 1.3a shows a millimeter-wave (W Band) weather radar designed at University of Massachusetts Amherst - Microwave Remote Sensing Laboratory (MIRSL) for understanding and predicting tornados in advance of its actual development[12]. Fig 1.3b shows real time image of tornado formation obtained using

this radar. Millimeter wave radars are also used for mapping of forests, land scapes and earth's natural resources[13] [14].

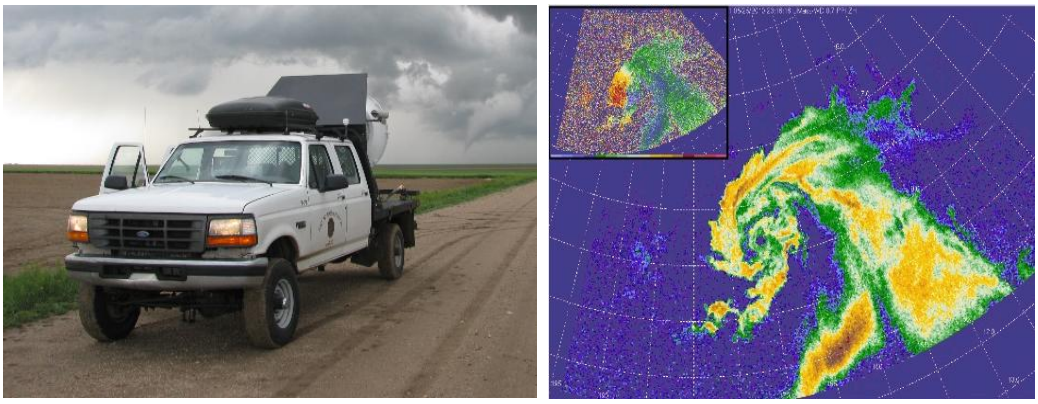


Figure 1.3: (a) mm-wave (Wband) mobile Doppler radar at MIRSL (b) Real time image of tornado formation obtained with the help of millimeter (Wband) radar. Reproduced from [12]

1.1.2 Process Technology for mm-wave integrated systems

In this work the 0.12um IBM8HP SiGe BiCMOS process technology is being used for chip design due to its superior performance compared to the Si CMOS process. SiGe HBTs are obtained by band gap engineering of the base of Si HBTs. The base of SiGe HBTs have graded Germanium-Ge content which modifies the energy band and improves the current gain, cutoff frequency f_t and maximum oscillation frequency f_{max} [15][16]. Fig 1.5 (left) shows the comparison between the energy band diagram of SiGe npn transistor (dashed) and Si npn transistor (bold) process technology [15]. With graded Germanium doping in the base of SiGe transistor the collector current gain is increased.

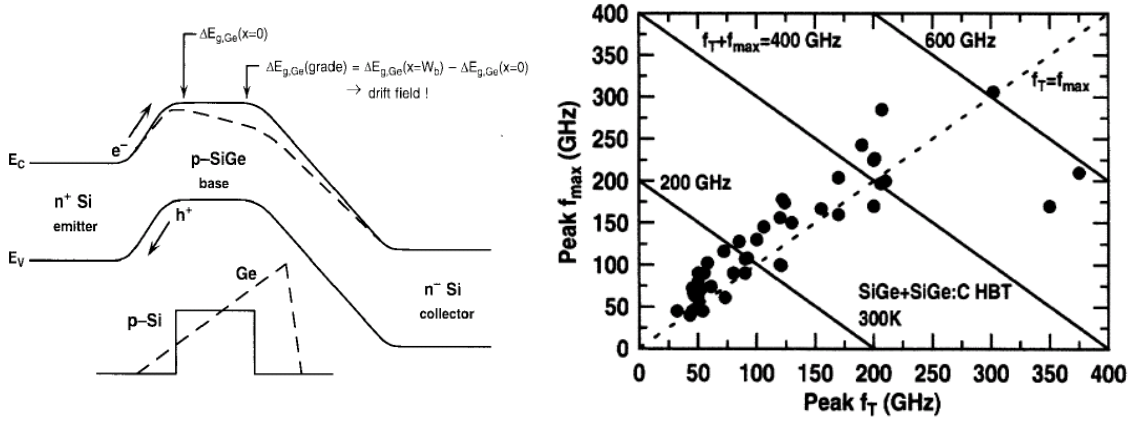


Figure 1.4: Energy band diagram comparison between SiGe BJT (dashed lines) with Si BJT(left). f_t and f_{max} of SiGe process (right). Reproduced from [38][39]

The Fig 1.4 (right) shows the f_t and f_{max} of different SiGe process technology. A 0.12um SiGe process is used for our down-converter design that has f_t greater than 200GHz and f_{max} greater than 265GHz. With further improvements in band engineering one could see this process technology being used for design of sub millimeter and terahertz transceivers [16].

The SiGe process also has advantages over commonly used high frequency III-V process technologies. They typically have at least 5 metal layers for signal routing, whereas III-V technologies typically only provide two layers. This helps in the implementation of very compact and complex design. Finally, SiGe BiCMOS processes provide the designer with the additional advantage of having digital circuits along with RF circuits which is not currently possible with III-V technologies [17][18].

1.2 Introduction to Phased Focal Plane Arrays (PFPA)

In conventional Focal Plane Arrays (FPA) the beam is obtained from a single feed. N different beams are obtained if there are N feed elements. These N beams are each discretised and processed separately. They do not provide full coverage of the area of interest of the outer space (reduced field of view). The feed elements should be steered mechanically to two or more positions to completely cover the area of interest. This results in reduced survey speed [20][21]. Fig 1.5 shows a FPA on a radio telescope and the corresponding field of view. Recently researchers around the world have devoted effort to improve the field of view and survey speed of FPA based radio telescopes [20]. The only way is to build a denser array and combine the signals from multiple elements by means of beamforming [21][22][23]. These focal plane arrays are called phased focal plane arrays (PFPAs). Fig 1.6 shows an PFPA on a radio telecscope and the corresponding field of view. A denser antenna array helps in obtaining a sharper beam, and beamforming helps in multiplying the signals obtained from different elements with suitable weights (different amplitudes and phase) to form a single beam. Section 1.3 discusses the architecture of PFPA being designed here at University of Massachusetts-Amherst.

The National Radio Astronomy Observatory - USA , The National Research Council – Canada, The Netherlands Foundation for Research in Astronomy (ASTRON) and The Commonwealth Scientific and Industrial Research Organization (CSIRO) – Australia are some of the research institutes which are putting in effort to build PFPAs [20]. The Green Bank Telescope (GBT) – West Virginia-USA, Karro Array Telescope –

South Africa and the Square kilometer Array – Australia are some of the radio telescopes that will be fitted with PFPAs in the near future [20].

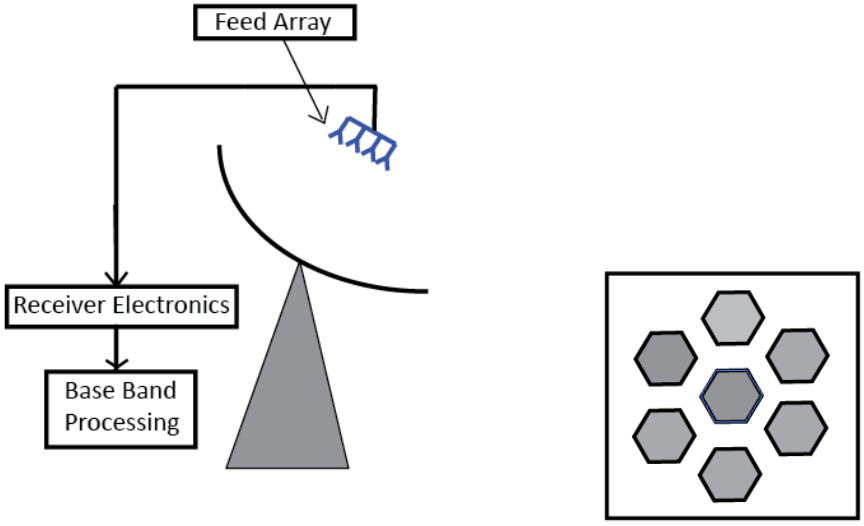


Figure 1.5: FPA on radio telescope and the corresponding field of view[21]

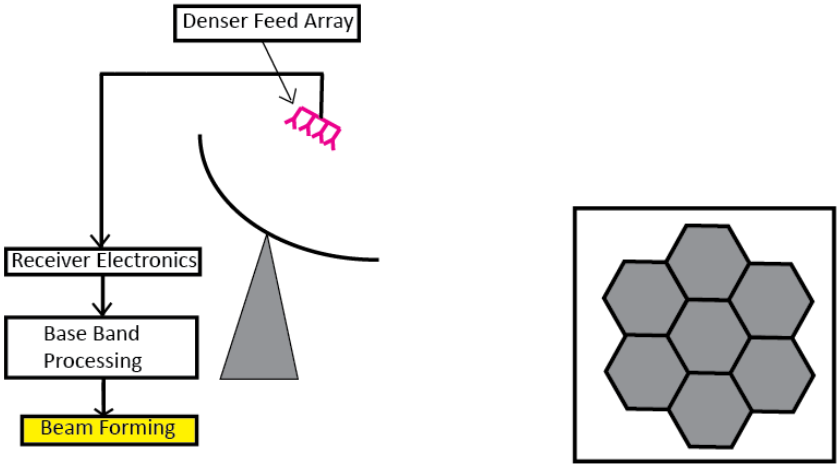


Figure 1.6: PFPA on radio telescope and the corresponding field of view[21]

1.3 Phased Focal Plane Array (PFPA) Architecture

The architecture of the PFPA being currently being designed and fabricated at The University of Massachusetts-Amherst is shown in Fig 1.7. The front end block consists of feed elements and preamplifiers. A waveguide Horn antenna is being used as feed element and 64 feed elements are placed in an 8*8 array [24][25]. The signals received by the feed elements are amplified using InP MMIC preamplifiers which provide a gain and noise temperature of approximately 30dB and 30K respectively [26]. This frontend block is placed inside a cryostat, which is maintained at 20K.

After leaving the Cryostat, the signal enters the room temperature block which consists of 1st and 2nd stage of down-converters. The 1st stage down-converter is the SiGe millimeter-wave (W-band) down-converter chip that is the focus of this thesis. This chip will down-convert the radio frequency-(RF) input signal (70 – 95GHz) to an intermediate frequency-(IF) signal (5-30GHz) using a fixed local oscillator-(LO) signal (~65GHz). This down-converter chip has a differential low noise amplifier, a double balanced Gilbert cell mixer, a differential IF amplifier and LO driver circuitry. This IC has a simulated conversion gain greater than 20dB, noise figure less than 9dB, and return loss greater than 10dB over the entire frequency band. This wideband down-converter requires a differential signal for its proper operation. This requirement is met using an external balun at the input. The on-chip LO driver circuitry allows the LO signal to be passed between the down-converters chips connected in parallel (see Fig 1.7).

The signal leaving the 1st stage down-converter is single ended as required by the second stage down-converter, which consists of a wideband IQ mixer (Avago Technologies 5-30GHz IQ Mixer [26]). This IQ mixer down-converts the output IF (5-

30GHz) to a baseband frequency signal (~1.5GHz+100MHz). The bandwidth of baseband signal is 100MHz. The LO signal for the IQ mixer is obtained from a frequency synthesizer (5-30GHz). The baseband signal leaving the 2nd stage down-converter enters the digital block. This block consists of ADCs and ROACH FPGA board [27]. The baseband signal is digitized, filtered and processed (beam-forming, spectroscopy, storage) by this block. The baseband processing is being done at the Radio Astronomy Systems Group – at Brigham Young University [21].

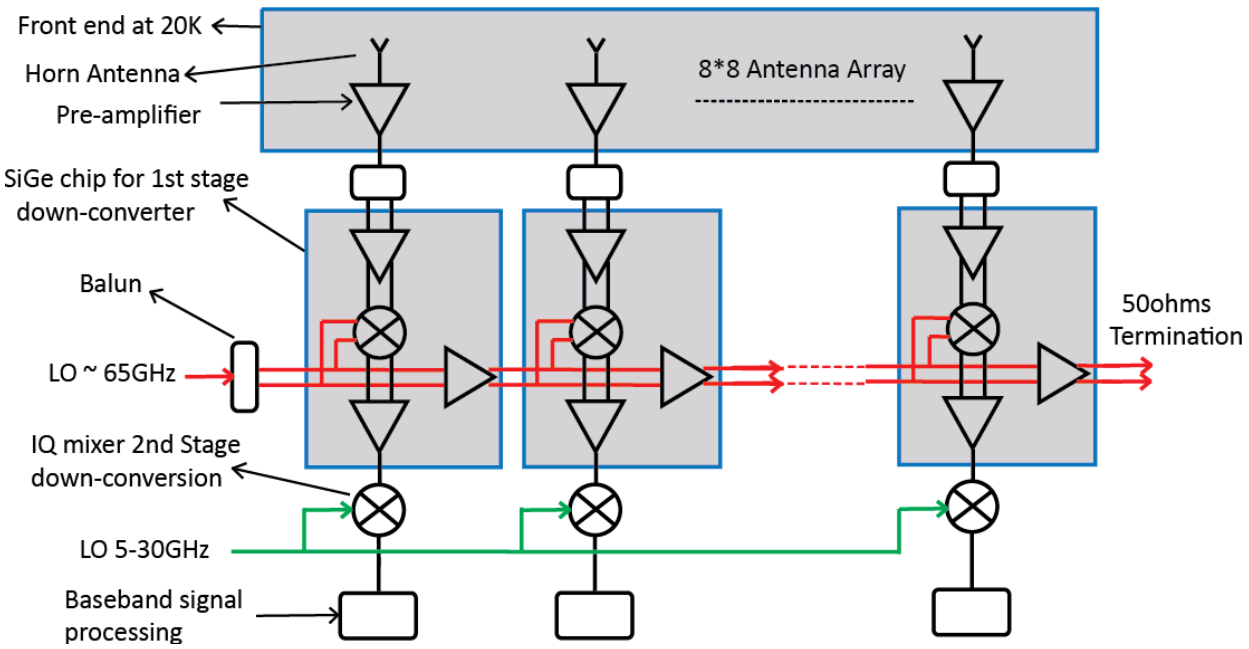


Figure 1.7: Architecture of Phased Focal Plane Array

1.4 SiGe mm-wave (W-band) Down-Converter

A millimeter-wave (W-band) down-converter for the phased focal plane array has been designed and fabricated using IBM Silicon Germanium (SiGe) 8HP process technology. The RF input frequency range of the down converter is 70 - 95GHz, the IF output frequency range is from 5 - 30GHz, and the LO frequency is fixed at 65GHz. Fig 1.8 shows the block diagram of the millimeter-wave down-converter chip. It consists of a differential low noise amplifier (LNA), a double balanced Gilbert cell mixer, a differential IF amplifier/Output driver, and LO driver circuitry. The specifications of this down-converter chip are given in Table-1. As this process has no through vias, there is no well defined ground connection between the chip and the chassis. Therefore a differential topology is being used for implementing the circuit in order to provide good on-chip grounding. The differential signal needed for proper working of the chip is obtained using a fin-line based balun.

A two stage cascode topology is being used for the design of the differential low noise amplifier. This amplifier has a broadband input match network to provide good noise and impedance match. The inter-stage match is designed to provide impedance match between the output of stage-1 and input impedance of stage-2. The output match network again provides a wideband impedance match between output of LNA and the input of the Gilbert cell mixer [27]. Since the entire design is on a single chip there is no need to match 50Ω at each internal node. Chapter-2 will discuss the design of LNA in detail.

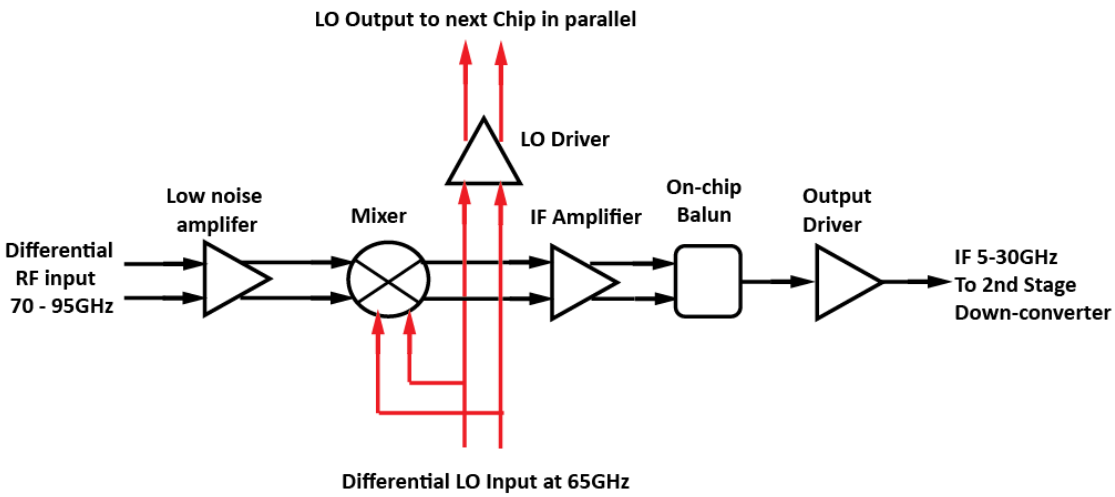


Figure 1.8: Block diagram of SiGe mm-wave down-converter

Conversion Gain in dB	**>20dB**
Input Match in dB	**<-10dB**
Output Match in dB	**<-10dB**
Noise figure in dB	**<10db**
Linearity - output 0.1dB compression point	**-10dBm**
Power dissipation	**< 200mW**
LO path gain	**4dB to overcome LO path transmission loss**
LO path input match	**< -10dB**

Table 1: Specifications of the SiGe mm-wave down-converter

Since the mixer has to operate at high frequencies, a Gilbert cell topology has been used for down-conversion. This is an active mixer which has lower noise and small gain compared to a lossy passive mixer. To obtain LO to IF and RF to IF isolation, a double balanced topology is used in place of a single balanced Gilbert cell mixer. This gives better performance at the cost of higher power consumption. The mixer RF input frequency is 70 – 95GHz, the IF output frequency is at 5 - 30GHz and the fixed LO frequency is 65GHz. The output of the mixer feeds the differential IF stage which consists of a wideband differential IF amplifier, on-chip balun and a single ended output driver. An on-chip balun is used for converting differential output of IF amplifier to single ended. It also ensures loading on IF amplifier is symmetric. The output driver is matched to 50Ω impedance (input impedance of 2^{nd} stage down-converter). A single ended output is necessary since the 2^{nd} stage down-converter has a single ended IQ mixer.

The on-chip LO driver circuitry is responsible for both supplying the LO signal needed by the Gilbert cell mixer of the chip and also to buffer and drive the LO port of the next channel down converter chip. The LO signal needs to be provided to both the mixer and the LO-driver. This is done by routing the LO on transmission lines (Grounded CPW lines) realized using top metal layers M7-M5. The IF, which is the output of the mixer is routed via transmission lines (Grounded CPW lines) realized using metal layers M4-M1. This novel feature of LO circuitry will assist in easy routing of LO from one chip to another in cascade thereby overcoming the complex issue of LO distribution/wiring for densely packed arrays.

The layout of the SiGe mm-wave Down-converter is as shown in Fig 1.9. The inductances are realized using grounded coplanar waveguide (GCPW) based transmission lines which have better shielding in comparison to microstrip lines. The size of the layout with bond-pads are 1.6 * 0.9mm^2. Two versions of the chip have been designed and fabricated. The second version is an optimized version of the first.

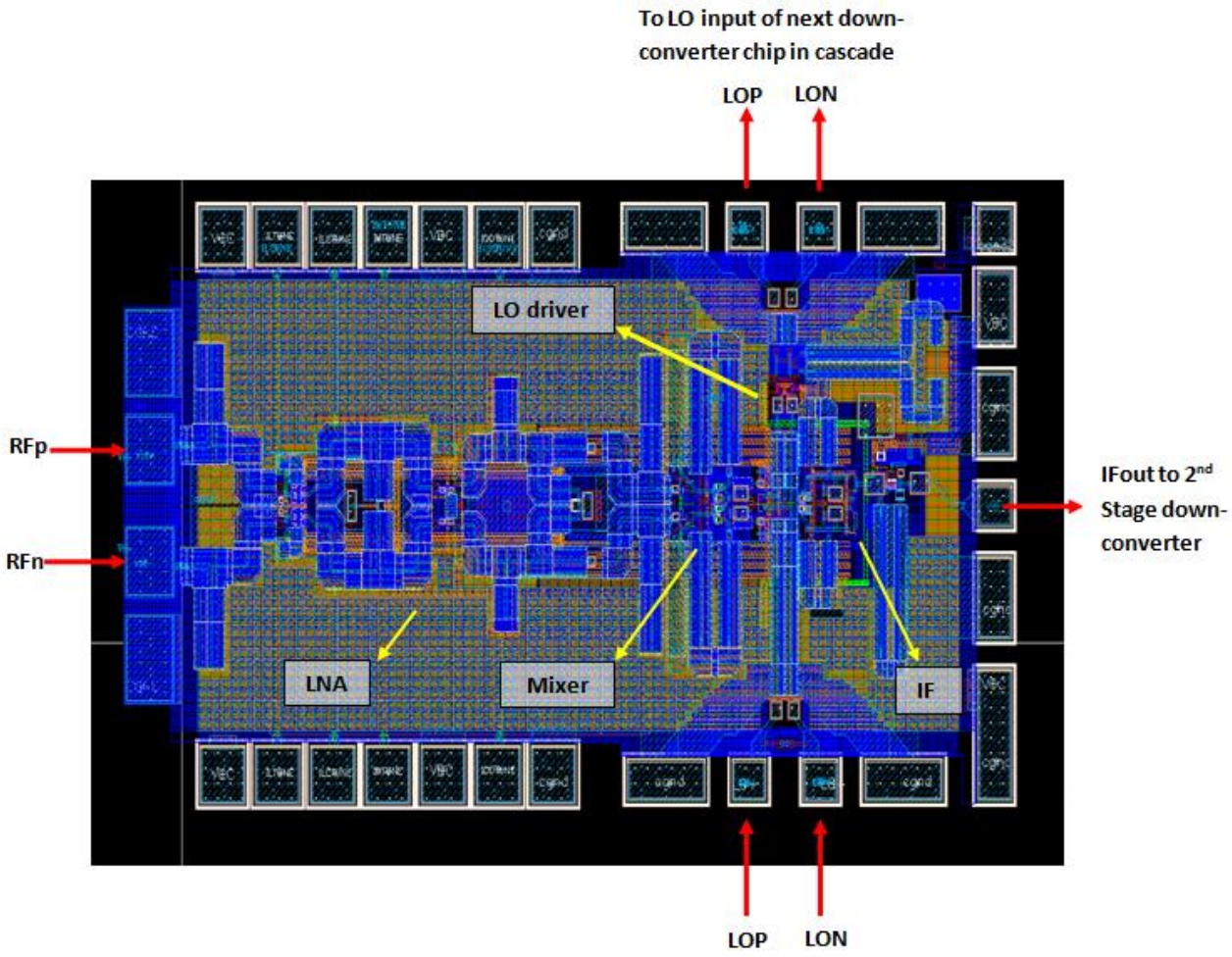


Figure 1.9: Layout of SiGe W-band down-converter IC

The overall simulation results (Conversion gain, Return loss and Noise figure) of the SiGe down-converter chip are discussed in chapter 2 – section 2.5. Table -2 gives a comparison of our work with other Si/SiGe based down-converter designs. If the measured results match simulation then this will be first high frequency wideband down-converter with this high gain, low noise figure, and linearity among Si/SiGe systems.

Frequency range in GHz	Technology	Conversion gain in dB	Noise figure in dB	IP1 in dBm	DC Power	Reference
77-83	SiGe	37	8-10	-27.5	121mW	[29]
80-84	CMOS 65nm	12	9-10	-13	94mW	[30]
75-86	0.13um SiGe	26	11	-16	1072mA	[31]
81-90	0.13um SiGe	36	Not shown	-33	274mW	[32]
73-81	0.13um SiGe	46	7-10.5	-38	195mW	[33]
75-95	0.18um SiGe	33dB	7dB	-35(i)	250mW	[34]
70 – 95	0.13um SiGe	25	8 – 10dB	-10 (0.1dB)	120mW	Our Work

Table 2: Comparison between our Down-Converter and currently published works

CHAPTER 2

DESIGN OF THE SIGE W-BAND DOWN-CONVERTER

A SiGe millimeter-wave (W-band) down-converter for a phased focal plane array has been designed and fabricated using IBM BiCMOS 8HP process technology. Fig 1.9 shows the block diagram of the down-converter chip.

An outline of this chapter is as follows: Section 2.1 will discuss the system specifications, Section 2.2 will cover the design of the differential low noise amplifier, Section 2.3 will discuss the design of the double balanced Gilbert cell mixer, Section 2.4 will cover the design of the IF stage and the output driver, Section 2.5 will discuss the design and implementation of the novel LO distribution network, Section 2.6 provides the overall simulation results of the SiGe down-converter, and section 2.7 will discuss the design of printed circuit boards for characterization of the integrated circuits.

2.1 SiGe Down-Converter Specifications

The SiGe down-converter plays the role of the first stage down-converter in the PFPA receiver shown in Fig 1.8. It is preceded by approximately 30dB of amplification. The total integrated signal power reaching the SiGe down-converter is in the range of -50 to -40dBm. The down-converter design depends on six important specifications namely – conversion gain, input match, output match, noise figure, linearity and power dissipation. Table-1 gives the specifications to be met by this down-converter.

The overall system noise should be less than 35K. The front end has a gain of 30dB and contributes noise of 30-32K to the overall system. This sets the limit for noise that the down-converter and the following stages can contribute to the overall system. The maximum noise that the down-converter can generate, referenced to the output of the cryogenic preamplifier is 3000K (a 10dB noise figure). To meet this specification, the low noise amplifier of the down-converter should be designed to achieve very low noise in the band of interest and also high gain to minimize the total noise contribution from the mixer and the IF stage. From Friis' equation [35], the low noise amplifier should have greater than 20dB of gain and a noise figure between 8-10 dB to meet the specifications of the down-converter.[3]

Another important factor to consider is the linearity of the down-converter. In our design the linearity is measured in terms of the 0.1dB output compression point. The set specification for output 0.1dB compression is -10dBm.

Power dissipation also plays an important role in the design of the receiver array. Higher power dissipation demands better cooling. This chip will be part of a PFPA receiver which is going to be operated continuously for long durations. The goal set for the down-converter chip is to have power dissipation $P_{disp} < 200mW$. This means an array of 8 such chips will dissipate less than 1.6W and an entire 2D array of 64 chips dissipates less than 13 W.

[3]The mixer noise figure and gain are assumed to be 12dB and 3dB. Substituting these values into Friss equation with LNA gain being unknown parameter, we obtain the minimum gain LNA should have (20dB) to meet the down-converter specifications.

Another important design issue with respect to the entire PFPA receiver is the LO distribution. Since the PFPA receiver has 8 x 8 down-converters arranged in a 2D array, the question of LO distribution becomes very important. Various designs were analyzed and it was decided to route the LO from chip to chip in cascade (see Fig 1.8). The LO input signal will propagate through 8 down-converter chips in cascade. The output of the eighth chip will be terminated in 100 Ω differential impedance. Section 2.5 will discuss the LO distribution architecture in more detail.

A differential design topology is used for the design of circuits. The reason for this is that the SiGe process technology has no well-defined connection to the chassis ground. The virtual ground obtained from a differential design helps to achieving a reliable on-chip ground. This comes at the cost of increased power dissipation with respect to a single-ended design.

2.2 Design of the Differential Low Noise Amplifier

It is very important to design the LNA with very low noise and high gain. In our case the LNA has to provide a gain greater than 20dB and noise figure less than 9dB, respectively, to add 3K noise temperature to the PFPA receiver. A 2-stage common emitter cascode topology is used for design of the LNA. Stage-1 is biased for minimum noise and impedance match, and stage-2 is biased for getting good gain. Fig 2.1 shows the schematic of the LNA. A cascode topology is used since it improves the gain–band-width product and also provides very good isolation S_{12} between input and output [35][17]. Since the LNA input RF and IF bandwidths are very wide, it requires a broad band input, inter-stage, and output match networks. The input match network is

designed for noise and impedance match whereas inter-stage and output match networks are designed to achieve maximum power gain.

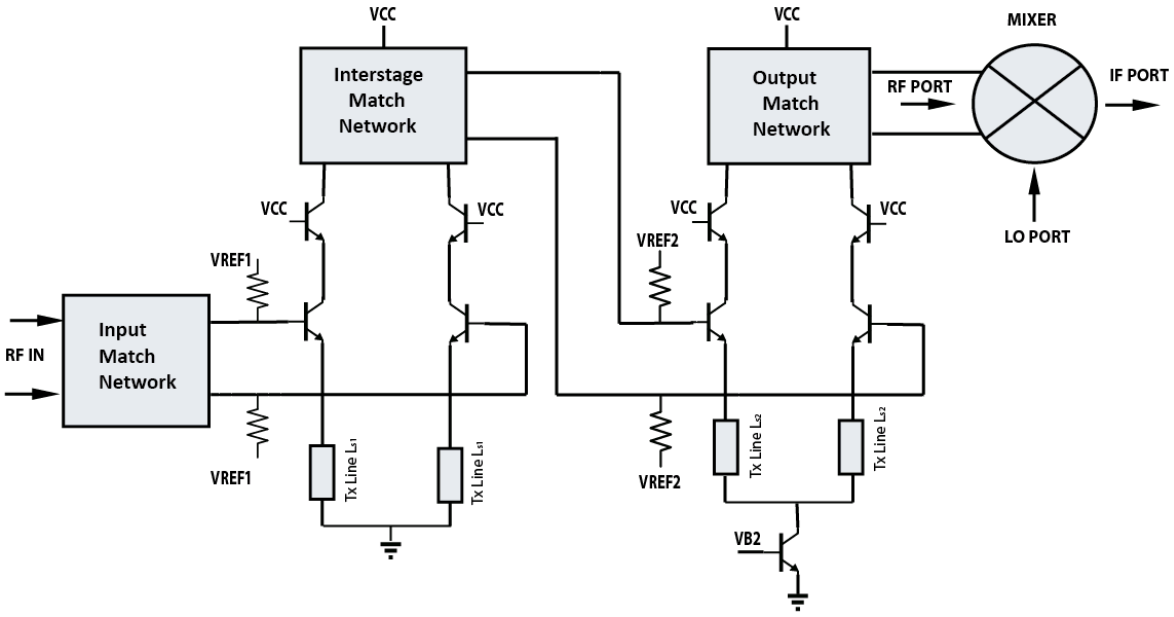


Figure 2.1: Schematic of 2-stage differential low noise amplifier

2.2.1 Broad Band Matching

Broad-band matching networks are required to achieve the bandwidth specifications of the LNA. The most commonly used matching networks methods are N-stage reactive elements based matching networks, resistive matching networks and feedback matching networks. We chose the N-stage reactive matching network since it is less lossy, which will result in superior noise performance. The first step in broad band matching involves modeling the input impedance of the network which needs to be matched[4].

[4] For noise match the input should be modeled as conj(Zopt) rather than Zin

This can be modeled as a series or parallel combination of resistor and capacitor. Fig 2.2 shows the model of the input impedance of the LNA.

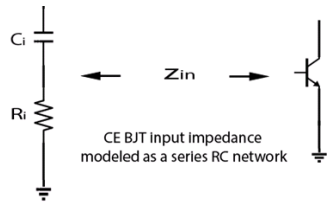


Figure 2.2: RC model of the input impedance of the LNA

The second step involves obtaining the insertion loss from the power loss ratio (PLR) [35] (equation 2.3 and 2.4). PLR is defined as the ratio of power available from the source to the power delivered to the load. PLR is determined by system specifications – input match and noise figure.

$$\text{Power Loss Ratio (PLR)} = \frac{\text{Pavs}}{\text{Pdel}} \qquad \text{equation 2.3}$$

Where Pavs is the power available from the source and Pdel is the power delivered to the load.

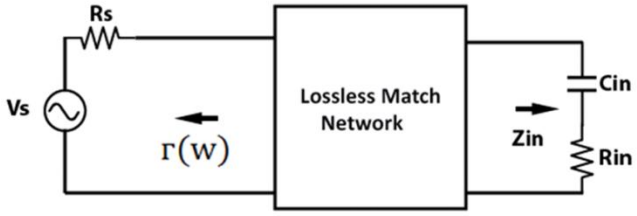
$$\text{Insertion loss IL} = 10 * \text{Log (PLR)} \qquad \text{equation 2.4}$$

The Third step involves correlating the insertion loss obtained from PLR with standard insertion loss functions like Butter worth, Elliptic or Chebyshev filter functions [35]. We chose Chebyshev insertion loss function since it gives broader match for the given number of reactive elements [36][5].

[5]Elliptic filters could also be used but the issue with them is requirement of complex zeros for realization. Complex zeros are more complicated to realize on-chip.

The only issue with this function is ripples in the pass band. From this correlation and doing numerical analysis we obtain the values of the reactive elements of the match network.

There are many limitations involved in the design of a broad band matching network. The main reason for this limitation is the modeled input capacitance associated with any transistor [35][28]. The Bode–Fano criteria will describe the limitations regarding the best possible match [35]. Considering the case of a series RC network (modeled input impedance of the transistor) the limit for best match that could be designed is given by Fig 2.3. The larger the input capacitance is the poorer the input match ($\Gamma(w)$) will be.



$$\int_0^{\infty} \frac{1}{w^2} \ln \frac{1}{\Gamma(w)}\, dw < \frac{\pi}{Rin * Cin}$$

Figure 2.3: Bode Fano criteria for match network for series RC model [35]

2.2.1.1 Design of the Input match network (IMN)

The main goal of the IMN is to provide minimum insertion loss. In doing so we also try to get minimum noise [40]. The IMN has to provide an impedance match between the source impedance *Rs* to the conjugate of input impedance *Zin*. The input transistor sizing is done such that *Ropt* (real part of *Zopt*) is close in value to *Rs* (Real part of *Zs*). The DC biasing is done such that we are operating this transistor at the current density required to achieve minimum noise figure [33]. The network is synthesized as described by the following steps.

The first step in input match network synthesis involves biasing HBT Q1 (see Fig 2.4) for minimum noise. The sizing of Q1 is done such that *Ropt* is closer in value to source impedance *Rs* (finline balun output port impedance ~ 55Ohms). This helps in obtaining minimum noise figure. Cascode transistor Q2 is selected to have same size as Q1. It adds very little noise to the LNA. It helps in getting high gain and good isolation (S_{12}).

The second step involves modeling of the input impedance of LNA stage-1 into *Rin* and *Cin*. This is as shown in Fig 2.4. Degeneration inductance - Le is used for additional control over input impedance *Zin* . It is used to bring *Zin* closer to *Zs*. It is around 20pH and has very small effect on Ropt and noise performance. A Smith chart plot of S_{11} at the input of stage 1 and its corresponding RC model are shown in Fig 2.4. The *Rin* and *Cin* are selected based on the good overlap of S_{11} plots of input of stage1 and RC model.

The third step involves the design of a match network which transforms the source impedance *Rs* to conjugate of input impedance *Zin*. A second order Chebyshev filter function is used for realization of match network [35][28]. The procedure involves first deriving the insertion loss function *IL(w)* based on LNA input specification (Return loss > 10dB). The input impedance function *Z(s)* is obtained from insertion loss function *IL(w)*. The network elements are obtained from *Z(s)* using numerical analysis or fraction expansion [28]. Matlab Code is used for synthesis (see Appendix A.1) of the network. (The code used here is modified version of the one used in Ref [28]). Fig 2.5 shows the input match network synthesized using the method described above. This network is made up of ideal circuit elements.

The fourth step involves tuning of the match network obtained above so that it could be realized using real elements. This network is shown in Fig 2.6. The inductance L_3 is added so that the network could be realized using transmission lines.

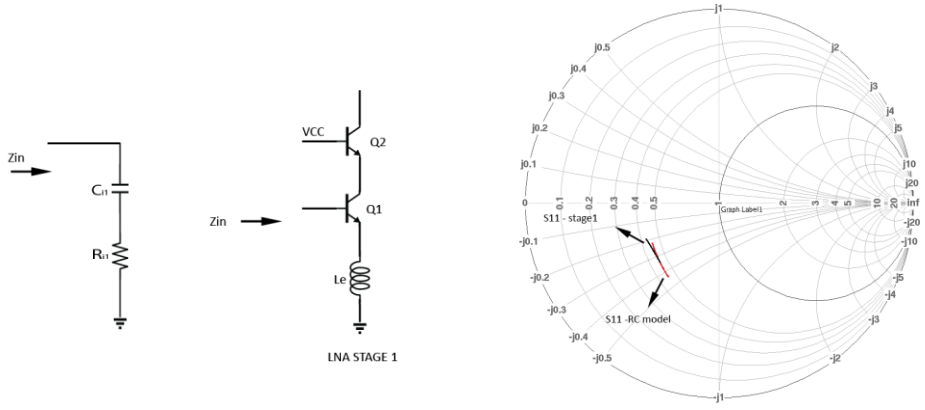


Figure 2.4: Modeling of input impedance *Zin* of transistor [28]

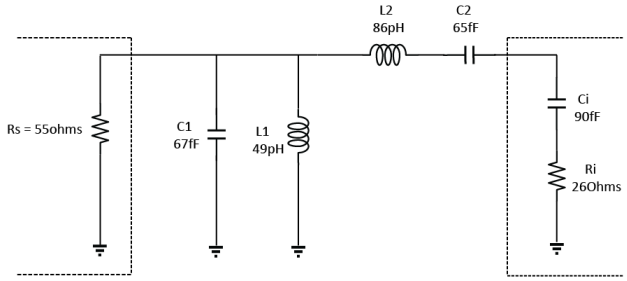


Figure 2.5: Input match network synthesized using ideal elements

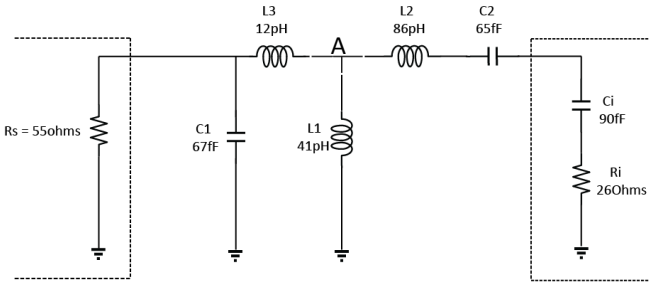


Figure 2.6: Tuned input match network realized using ideal elements

In the network shown in Fig 2.6, the inductances - L_1, L_2 and L_3 are realized using grounded cpw (GCPW) lines. These transmission lines have better shielding than microstrip lines. They need to connected at the node joining the 3 lines (node-A). This is realized using TEE junction. The capacitance C_2 is realized using MIM capacitance. The partial network realized using real elements are shown in Fig 2.7. The Return loss (S_{11}) and gain (S_{21}) for the two networks (ideal and T-line) are shown in Fig 2.8 and Fig 2.9. Additional tuning of transmission lines (length and width) is carried out to get closer match between the ideal and real element results. The noise figure of the LNA input – stage is shown in Fig 2.10. There is a small increase in noise figure due to additional losses associated with transmission lines.

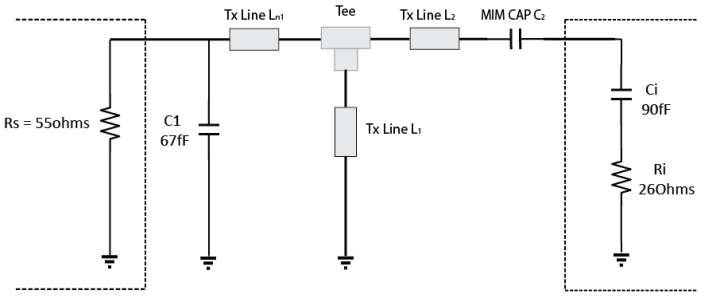


Figure 2.7: Input match network partially realized using ideal elements

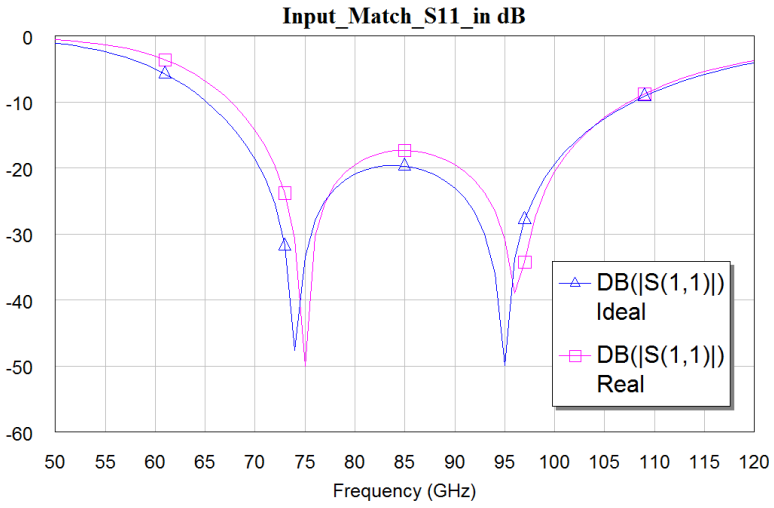


Figure 2.8: Input match S11 in dB. (ideal (blue), T-line (pink))

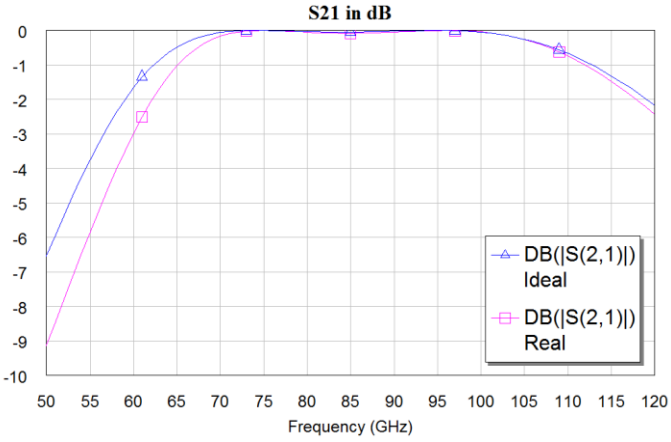


Figure 2.9: Input match S21 in dB. (ideal(blue) , T-line (pink)).

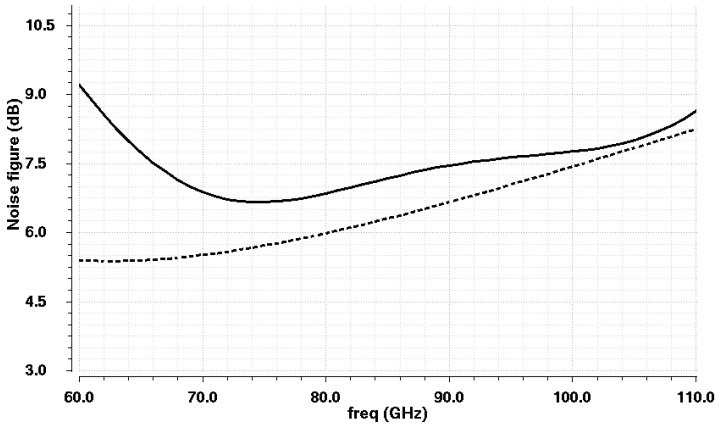


Figure 2.10: Noise figure of LNA - Stage1. NF (bold), NFmin (dash)

In the design described above the bondwire inductance L_{bw} was not taken into account. When L_{bw} was included in the design shown in Fig 2.7, the input match gets negatively affected. To overcome the effect of L_{bw} an additional tuning capacitor Cn was included as shown in Fig 2.11. Capacitors C1 and Cn are realized through the capacitance of the input bondpad. Fig 2.12 shows the complete input network realized using the elements provided by IBM BiCMOS 8HP process technology. The layout is symmetrical on both sides of the differential signal paths (rf+ and rf-). 3 mils long wire bonds are assumed between the signal bond-pads and the transmission lines on the PCB.

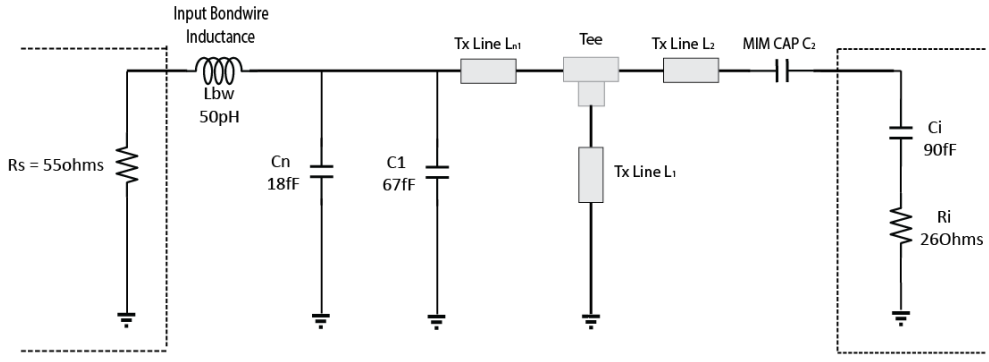


Figure 2.11:Input match network with bondwire inductance *Lbw* and tuning capacitor *Cn*

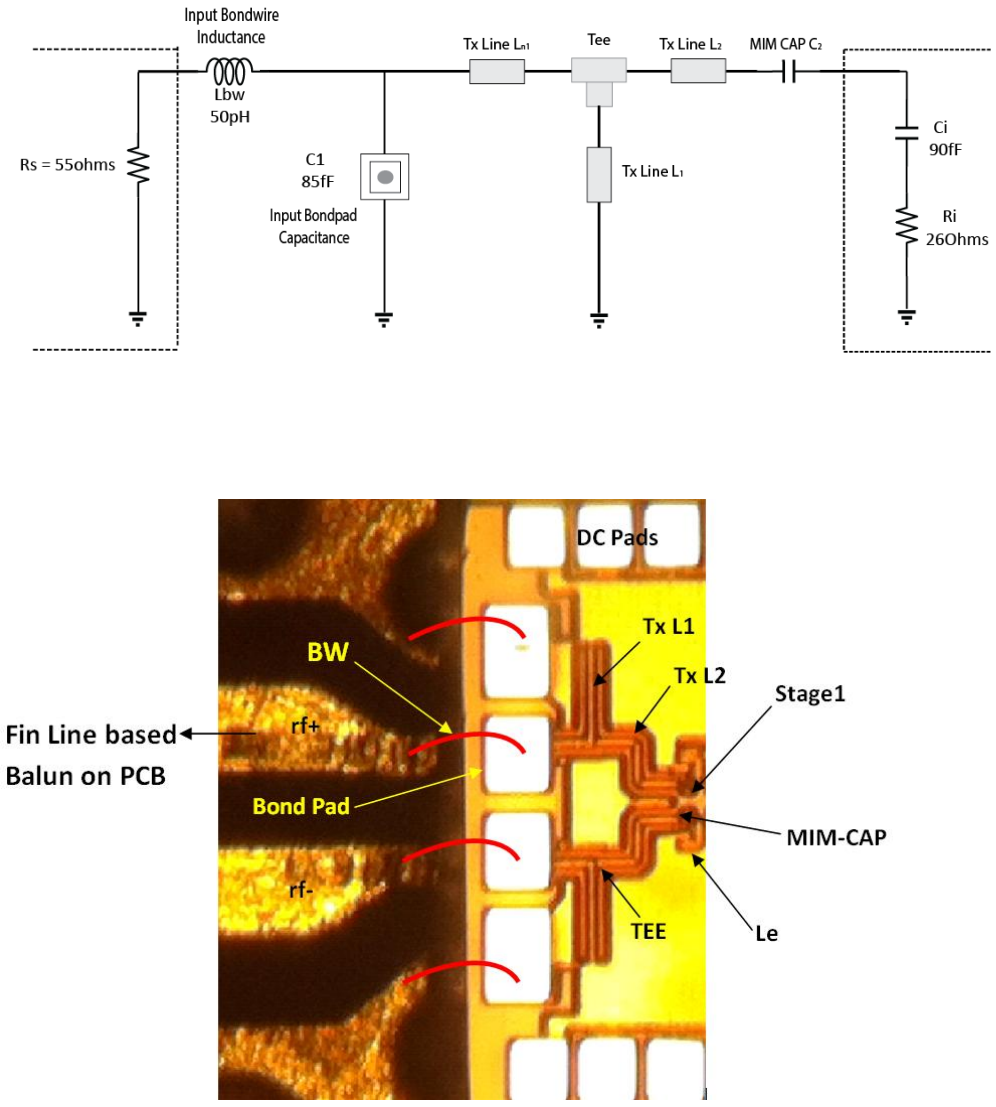


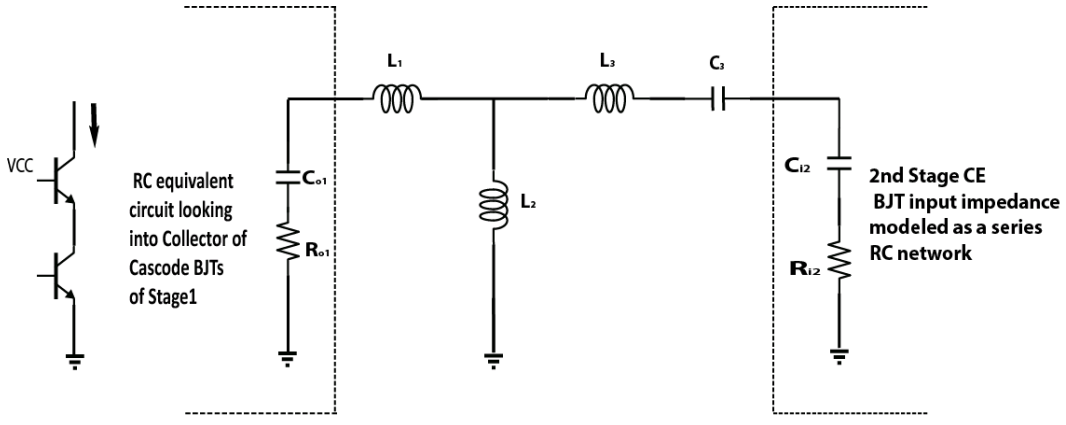
Figure 2.12: (a) Schematic-IMN realized using real elements. (b) Top view of fabricated layout of IMN

2.2.1.2 Design of inter-stage match network (ISMN)

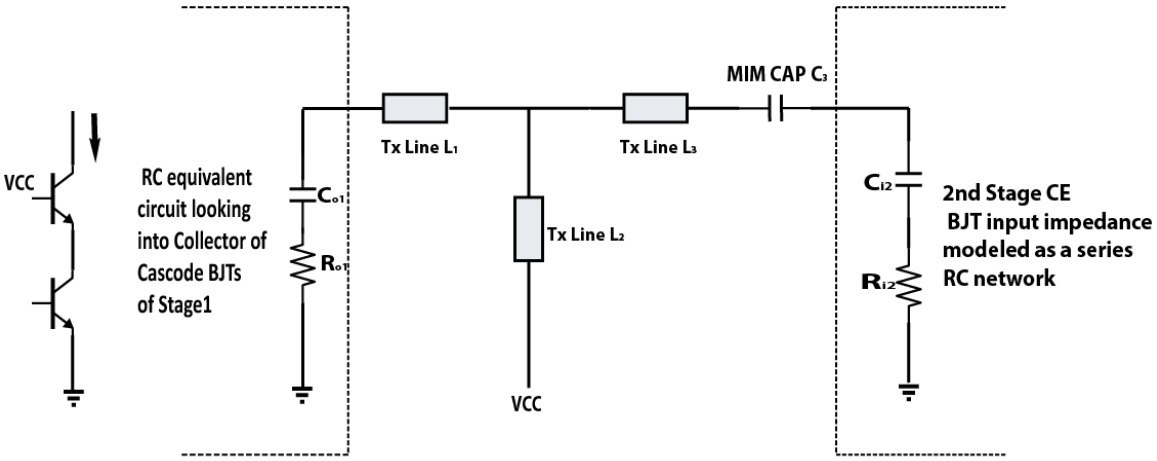
The gain of Stage-1 rolls off as 6dB per octave. The role of the inter-stage match network is to provide an impedance match between the output impedance of stage-1 and the input impedance of stage-2. It should flatten the gain roll off introduced by stage-1. The procedure for synthesis of ISMN is very similar to that described for the IMN Section 2.2.1.1. The main difference is that the IMN design is done for noise and impedance match of LNA stage-1,whereas here, it is to the input impedance of stage-2 (Power match).

A 4^{th} order match network is realized (See Figure 2.13a). The procedure for transformation from ideal to real match network is similar to the one described in IMN. The ideal inductors are realized using transmission lines (GCPW) and ideal capacitors by MIM capacitors. Figure 2.13b shows the ISMN realized using real elements provided by process technology. Figure 2.13c shows the S_{21} plot of the ISMN.

(a)



(b)



(c)

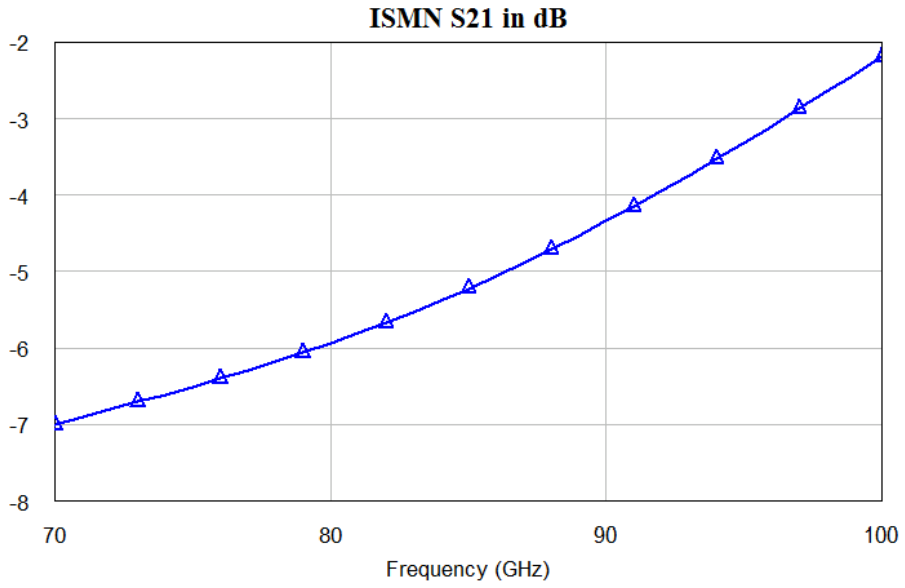


Figure 2.13: (a) Schematic of ISMN. (b) ISMN realized using transmission lines.

(c)ISMN S21 in dB

2.2.1.3 Design of output match network (OMN)

The gain of Stage-2 rolls off as 6dB per decade. The role of the output match network is 1) to flatten this gain roll off and 2) to provide an impedance match between output impedance of stage-2 and input impedance of the Mixer. Figure 2.14 shows the output match network concept. The Stage-2 input insertion loss is flat over entire bandwidth (see Fig 2.14a). This is then multiplied by the insertion loss of stage-2 (-6dB roll-off per octave – see fig 2.14b). This results in stage-2 output insertion loss having a 6db roll-off per octave – see fig 2.14c. The role of OMN is to correct this roll-off. To do so it should have positive 6dB rolloff per octave – see fig 2.14d.

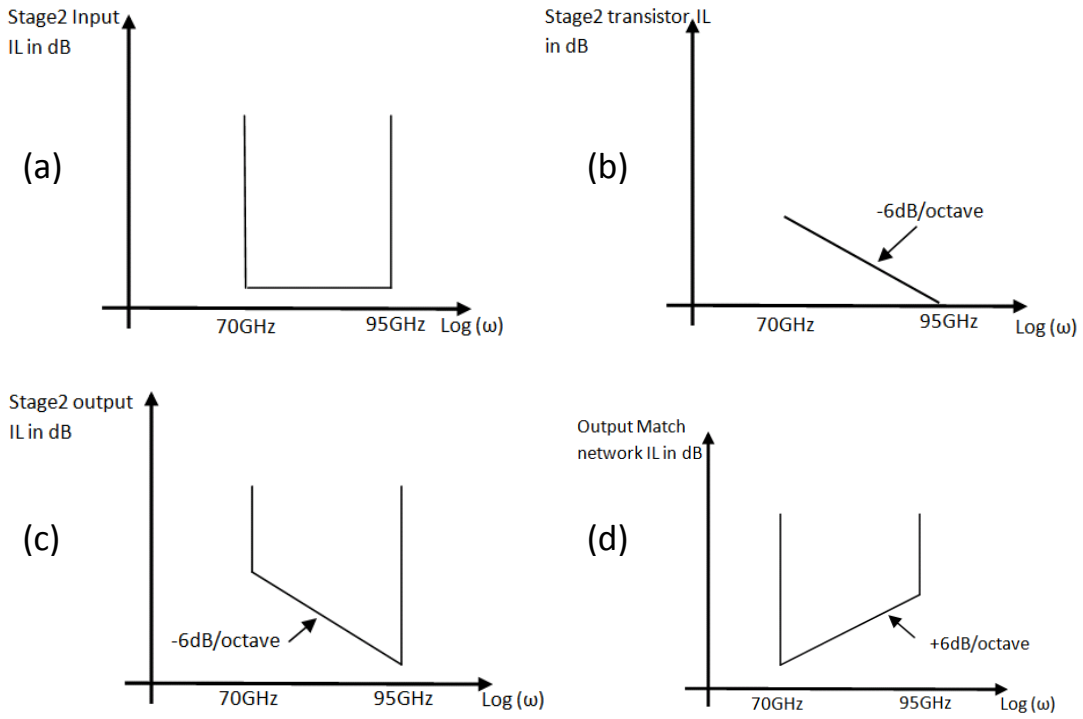
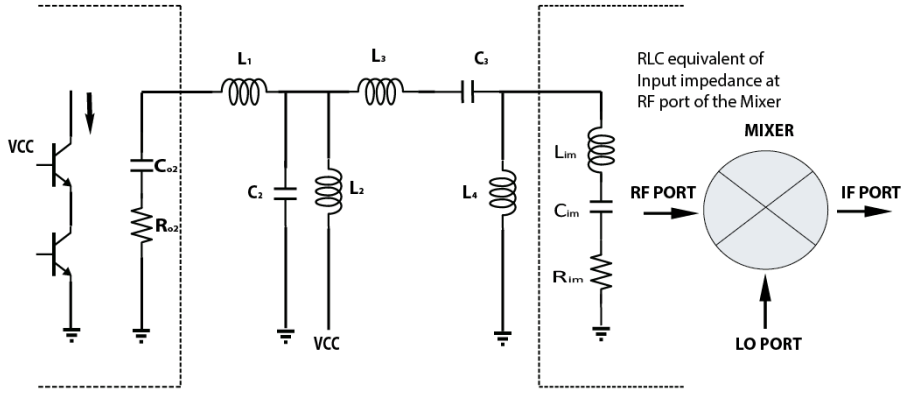


Figure 2.14: Output match network concept

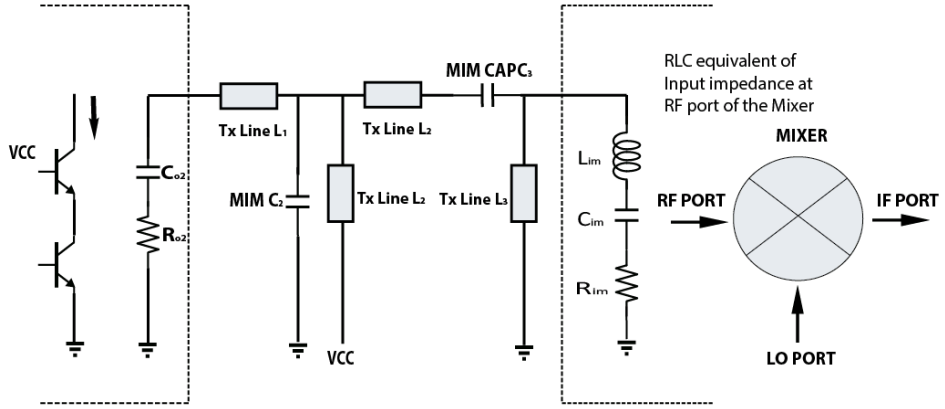
The procedure is similar to ISMN. The first step is modeling of the input impedance of mixer (see fig 2.15a - The inductance *Lim* in the modeled input impedance of the mixer is due to the inductance used between transconductance RF transistors and LO switching transistors in design of double balanced Gilbert cell mixer). This is followed by match network synthesis. A 6^{th} order network is designed rather than 4^{th} order to realize the match specifications (See Fig 2.15b, S_{21} of this network is shown in Fig 2.15c). The reason 6^{th} order match network is designed because the lower order networks could not meet the insertion loss specification.

Here again MATLAB code for realizing network parameters. (Appendix A.1.2). Figure 2.16 shows the physical layout of all the three match networks used for design of broad band LNA.

(a)



(b)



(c)

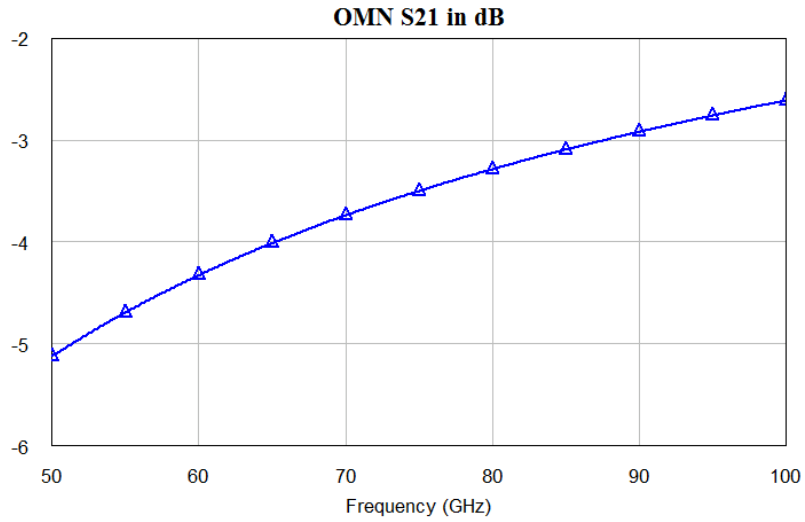


Fig 2.15: (a) Schematic of OMN ideal. (b) OMN realized using transmission lines. (c) OMN S_{21} in dB.

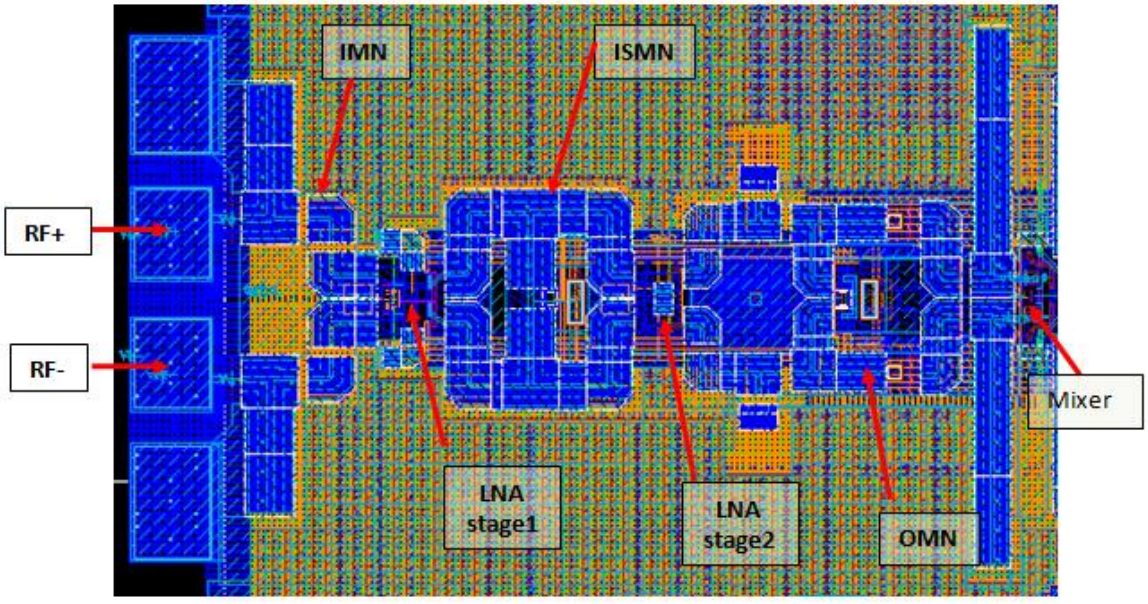
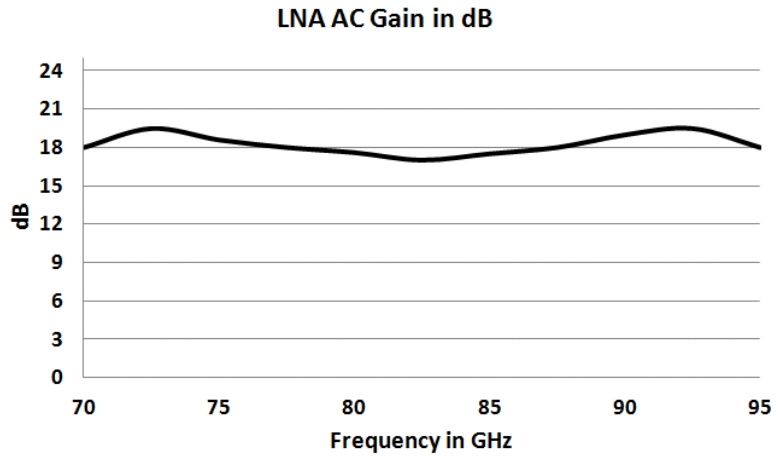
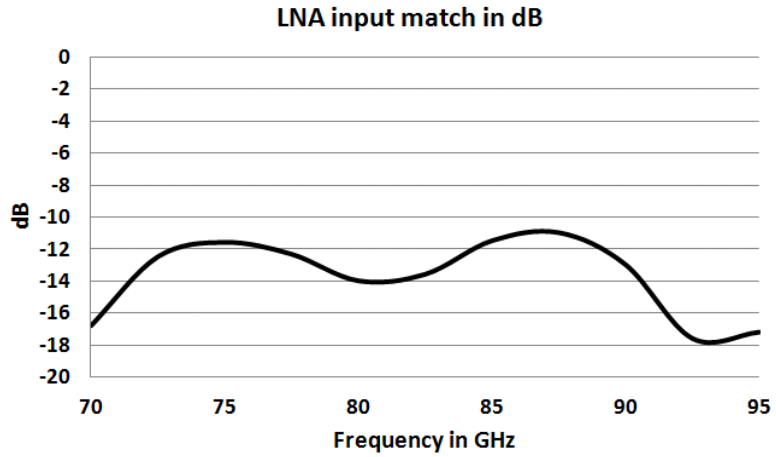


Figure 2.16: Layout of LNA showing all 3 match networks.

2.2.2 Simulation results

The LNA AC and S-parameter simulation was carried out using Analog design environment (ADE) in Cadence – Virtuoso. The AC gain of the LNA is as shown in figure 2.17a. As per specification the gain is around 18dB covering the entire band. The input match and noise figure are shown in figure 2.17b and 2.17c. The input match is less than -10dB over the entire band. Electromagnetic models (EM) of transmission lines (obtained using EM tool and HFSS) are used for simulation.





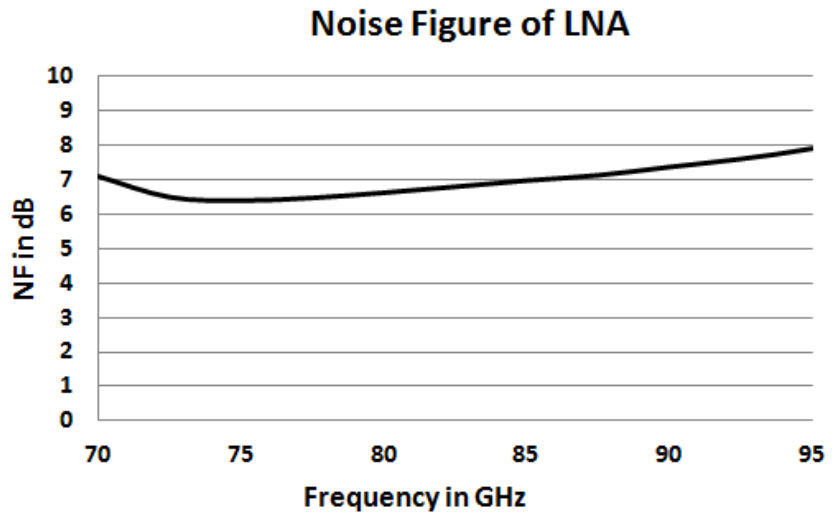


Figure 2.17: LNA (a) AC gain. (b) Input match-S_{11}. (c) Noise Figure

2.3 Design of Double Balanced Gilbert cell mixer

The function of the mixer is to down-convert the LNA output to an IF signal using a local oscillator signal. In our case the RF frequency band is from 70 – 95GHz, the IF band is from 5 – 30GHz and the LO is fixed at 65GHz. Fig 2.18 shows the block diagram of the mixer including the IF low pass filter. There is no issue of image frequency in our mixer design due to two reasons namely – (1) The image frequency is filtered by the optics in front of the PFPA receiver. (2) The noise in the image band generated by LNA is very low due to the sharp gain roll-off below 70GHz. The IF low pass filter cut off frequency is 30GHz. The frequency spectrum is as shown in the Fig 2.19.

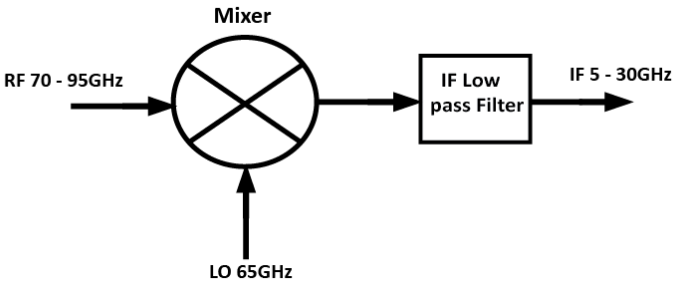


Figure 2.18: Mixer with IF low pass filter

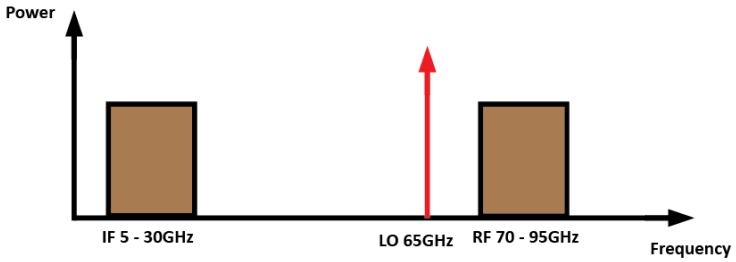


Figure 2.19: Frequency spectrum of the Mixer in the down-converter

There are active and passive mixer topologies. An active mixer acts both as a mixer and an amplifier whereas a passive mixer acts as a mixer and an attenuator. Since we are interested in having gain in the mixer stage and lower LO swing requirements (dictated by the LO frequency synthesizer used at telescope station), we are using active mixer topology. Since the RF frequency band of the mixer in the SiGe down-converter is very high, we decided to go with Gilbert cell active mixer topology [17]. Double balanced topology is used to get good LO – IF and LO – RF isolation (See Fig 2.20).

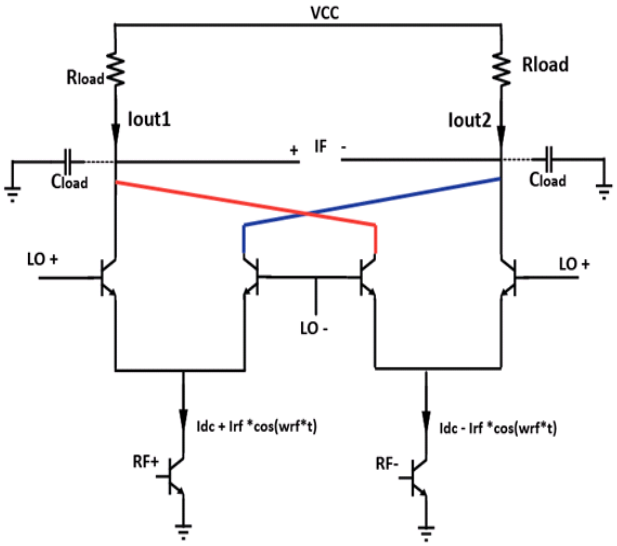


Figure 2.20: Double balanced Gilbert cell mixer (right)

Figure 2.21 shows the schematic of a double balanced Gilbert cell mixer designed using the SiGe 8HP process. The load includes resistor-R_{load} and an inductance-L_{load} for gain peaking at high frequencies. The inductive load is implemented using GCPW transmission lines. There is also an inductance *TxLc* used between transconductance-RF transistors and LO switching transistors for reducing the effect of the bandwidth limiting capacitance at the output of the transconductance transistors. The IF low pass filtering is carried out using an RC filter with capacitance *Cout* being the output capacitance looking into the switching transistors and resistance *Rout* includes a parallel combination of load resistor R_{load} and output resistance R_o looking into the switching transistors. The cutoff frequency of this filter is at around 35GHz. DC biasing details are also shown in Figure 2.21 (left). The additional trimmer pin "*IMtweak*" in the bias schematic permits control the conversion gain by +/- 2.5dB. This DC pin will alter the bias of the input transconductance-rf transistors and there by controls the gain of the mixer. Figure 2.22 shows the expected conversion gain of the Mixer.

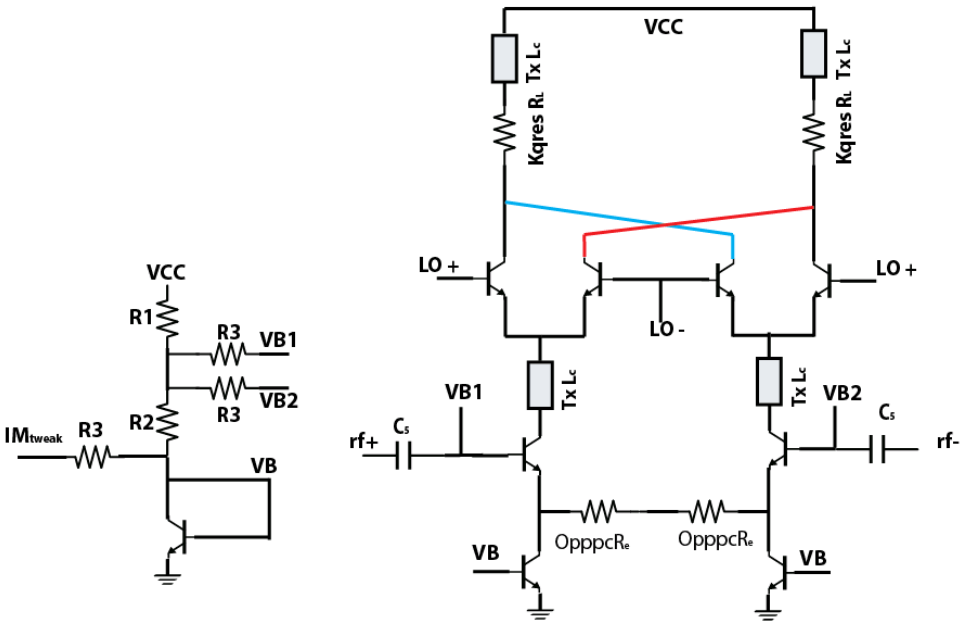


Figure 2.21: Double Balanced Gilbert cell Mixer

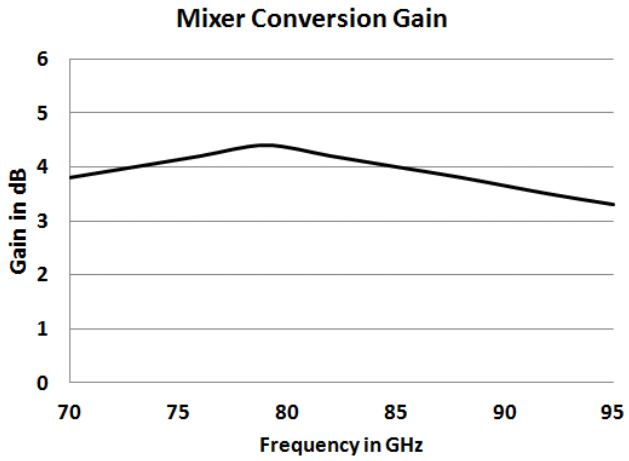


Figure 2.22: Conversion gain of Mixer with respect to RF input frequency

2.4 Design of the IF stage

The IF stage consists of differential IF amplifier, an on-chip wide band active balun, and a single ended output driver (see Figure 2.23). The differential IF amplifier provides a gain of 3dB. The IF stage is followed by an off-chip 2nd stage down-converter which is a single ended image reject mixer. This 2nd stage down-converter will down-convert the IF input at 5 -30GHz to baseband. To get the single ended IF output, an on-chip active balun follows the differential IF amplifier, as shown in Figure 2.23. This balun is followed by a single ended output driver to provide additional gain and output match. This driver is output matched to a 50Ω termination. The schematic of the differential IF amplifier, on-chip Balun and output driver are as shown in Figure 2.24. GCPW transmission lines are used for the realization of high frequency gain peaking inductor realization. The bond-pad capacitance and bond-wire inductance are taken into account during the output match design.

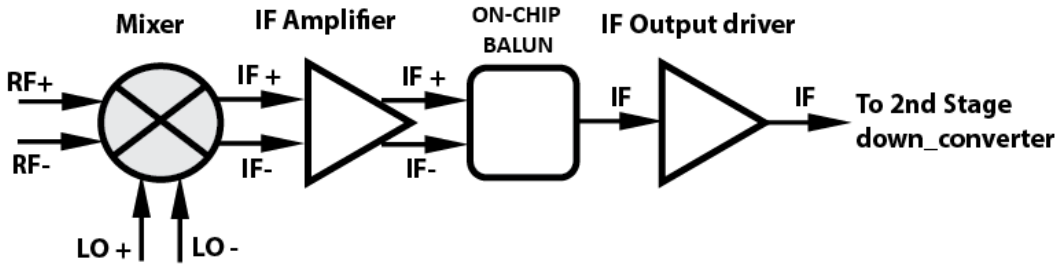


Figure 2.23: Block diagram of IF stage

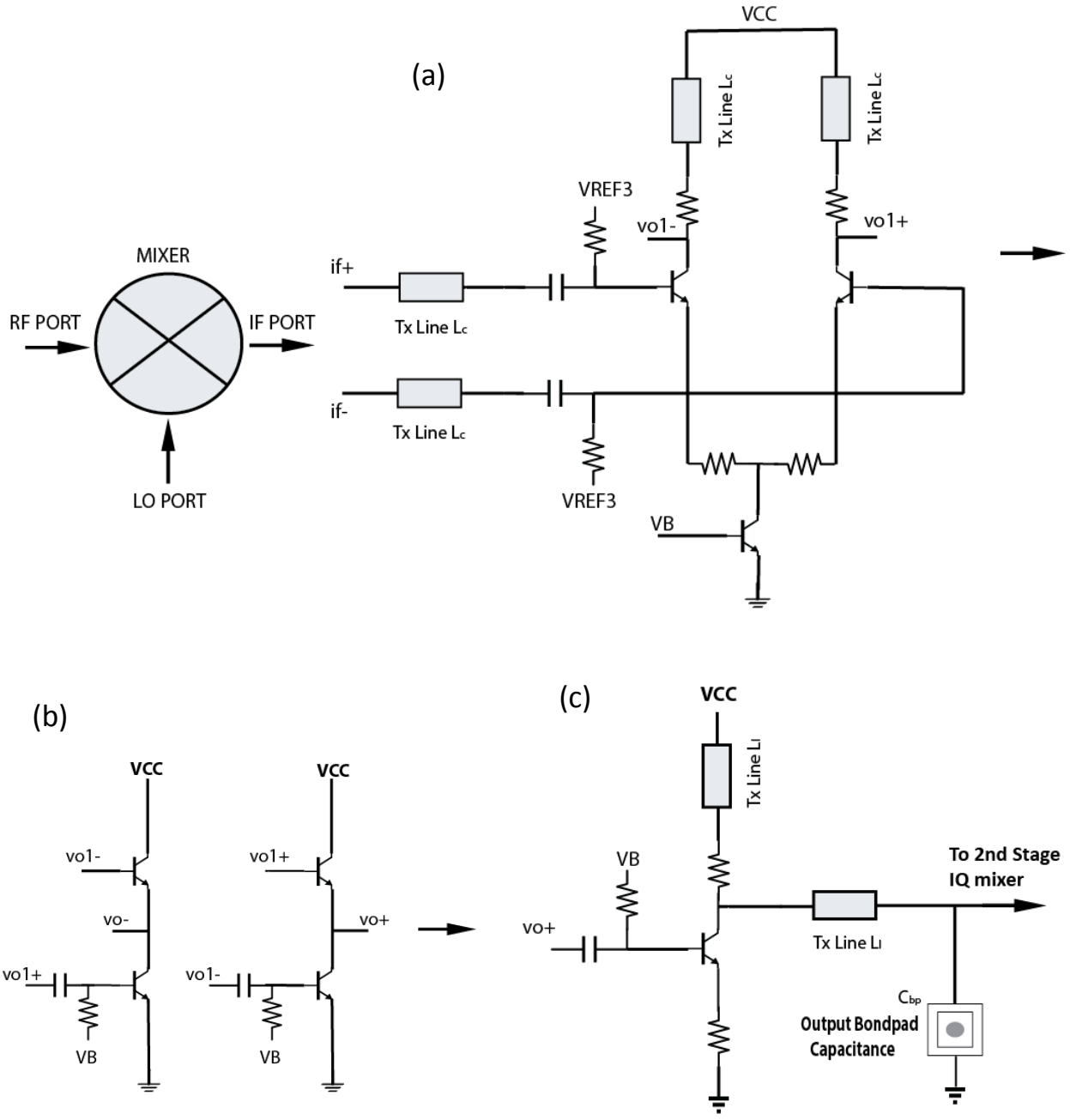


Figure2.24: Schematic a) Differential IF amplifier b) On-chip Balun and c) Output driver.

Figure 2.25 shows the gain of the IF stage gain versus frequency. In this simulation EM models have been included for the transmission lines used for matching and routing the IF signal beneath the LO distribution network (see Figure 2.28). The simulation also includes the output bond-pad capacitance and bond-wire inductances. The tweak point associated with the output driver could be used for additional control of the gain. The IF stage provides a gain of 4dB across the band.

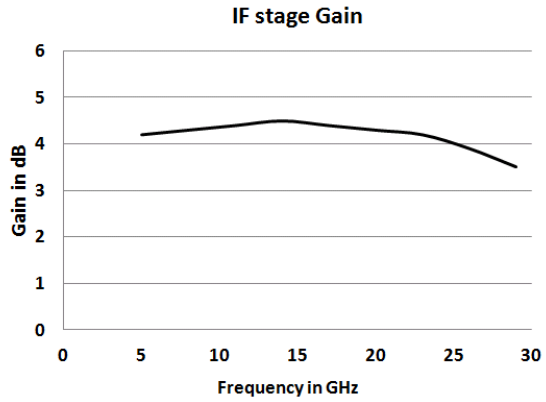


Figure 2.25: IF stage Gain vs Frequency.

2.5 Design of Local Oscillator Distribution Network

The on-chip local oscillator distribution network is responsible for supplying the LO signal needed by the Gilbert cell mixer of the current chip and also to buffer and drive the LO port of the next down converter chip. Figure 2.26 shows the block diagram of the on-chip LO driver circuitry. The LO driver is a differential amplifier which provides a gain of 4dB at 65GHz to overcome losses associated with the inter-chip connections. The input of this amplifier is matched to a 100Ω differential impedance. The

output is matched to 100Ω differential impedance of LO input of next chip in cascade. Figure 2.27 shows the schematic of this LO driver.

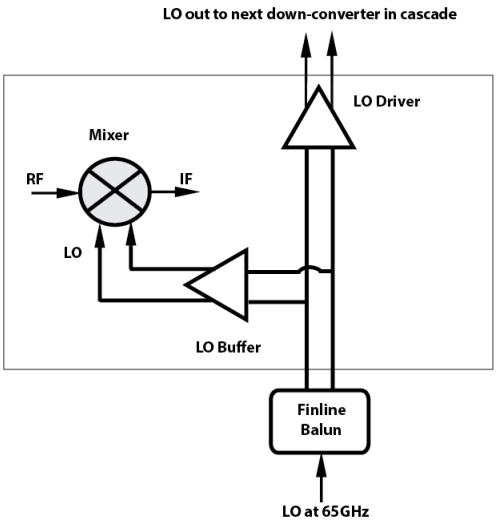


Figure 2.26: Block diagram of on-chip LO driver circuitry.

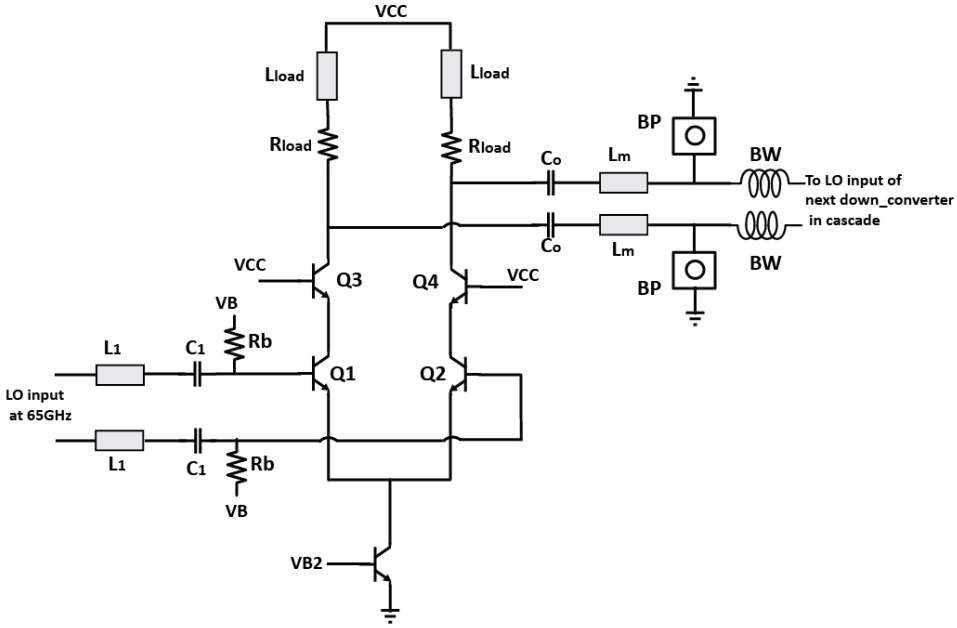


Figure 2.27: Schematic of LO driver

Figure 2.28 shows how the novel LO distribution is realized on-chip by using different metal layers. The LO signal needs to be provided to both the mixer and the LO-driver. This is done by routing the LO on transmission lines (Grounded CPW lines) realized using top metal layers M7-M5 (shown by grey lines). The IF, which is the output of the mixer, is routed via transmission line (Grounded CPW lines) realized using lower metal layers M4-M1 (shown by red lines). This feature of the LO circuitry will assist in easy routing of LO from one chip to another in cascade and thereby will overcome the complex issue of LO distribution/wiring for densely packed arrays. (The Fig 2.28 is just an illustration of LO distribution network. In main design there is no gap between the two transmission lines shown in Fig 2.28. The LO and IF lines are on top of each other. There is no spacing as illustrated in Fig 2.28.)

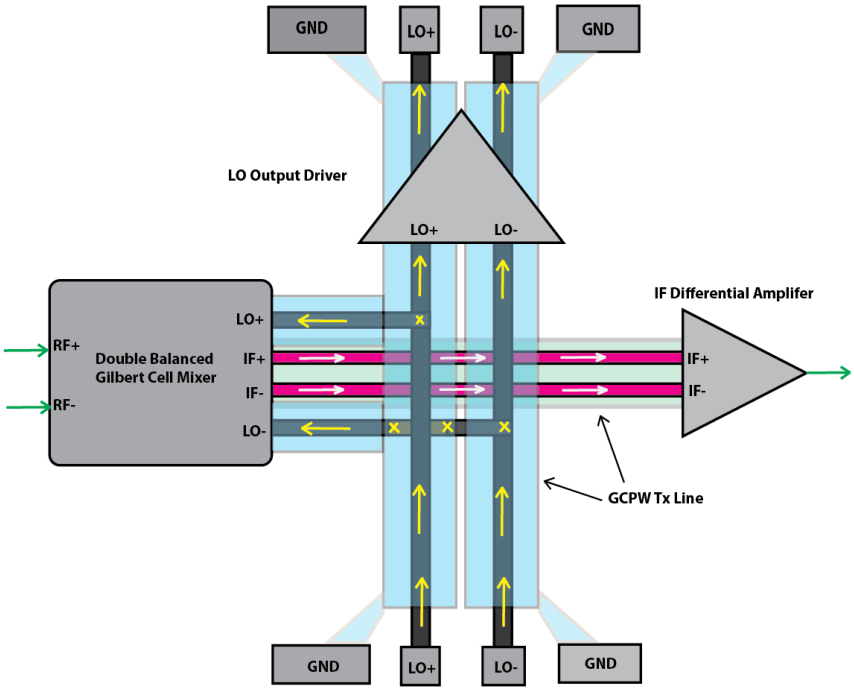


Figure 2.28: On-chip realization of LO distribution using different metal layers

2.6 Simulation results of the SiGe down-converter

2.6.1 Simulation result of the W-band SiGe Down-converter

Figure 2.29 shows the simulation results of the W-band down-converter. The conversion gain meets the specification requirement (Gain > 20dB). This simulation includes the input and output RF/LO waveguide baluns (S-parameters obtained from HFSS simulation), input and output bondpad capacitances and bond wire inductances (S-parameters), and EM extracted models of transmission lines used for matching networks and signal routing. The input return loss is better than -10dB which also meets the specification. The noise figure is less than 9dB over band.

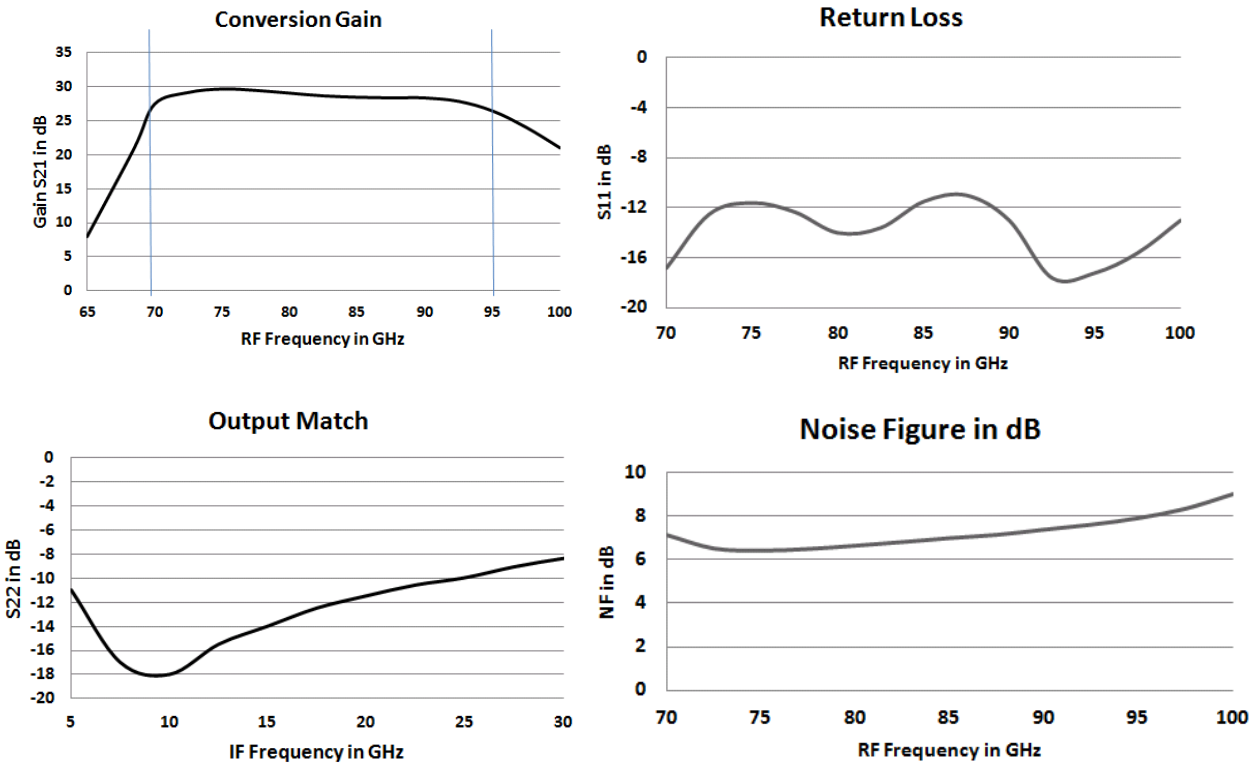


Figure 2.29: Simulation results of SiGe Wband down-converter

2.6.2 Simulation results of LO-distribution network

The LO driver gain is greater than 4dB at 65GHz, which is believed to be sufficient to overcome any loss associated with signal transmission between chips (see LO gain Figure 2.30). The input and output match are better than -10dB. The output of the LO driver was terminated with 100Ω differential impedance. Here again for simulations we had taken into account the EM model of the LO distribution network shown in Figure 2.28.

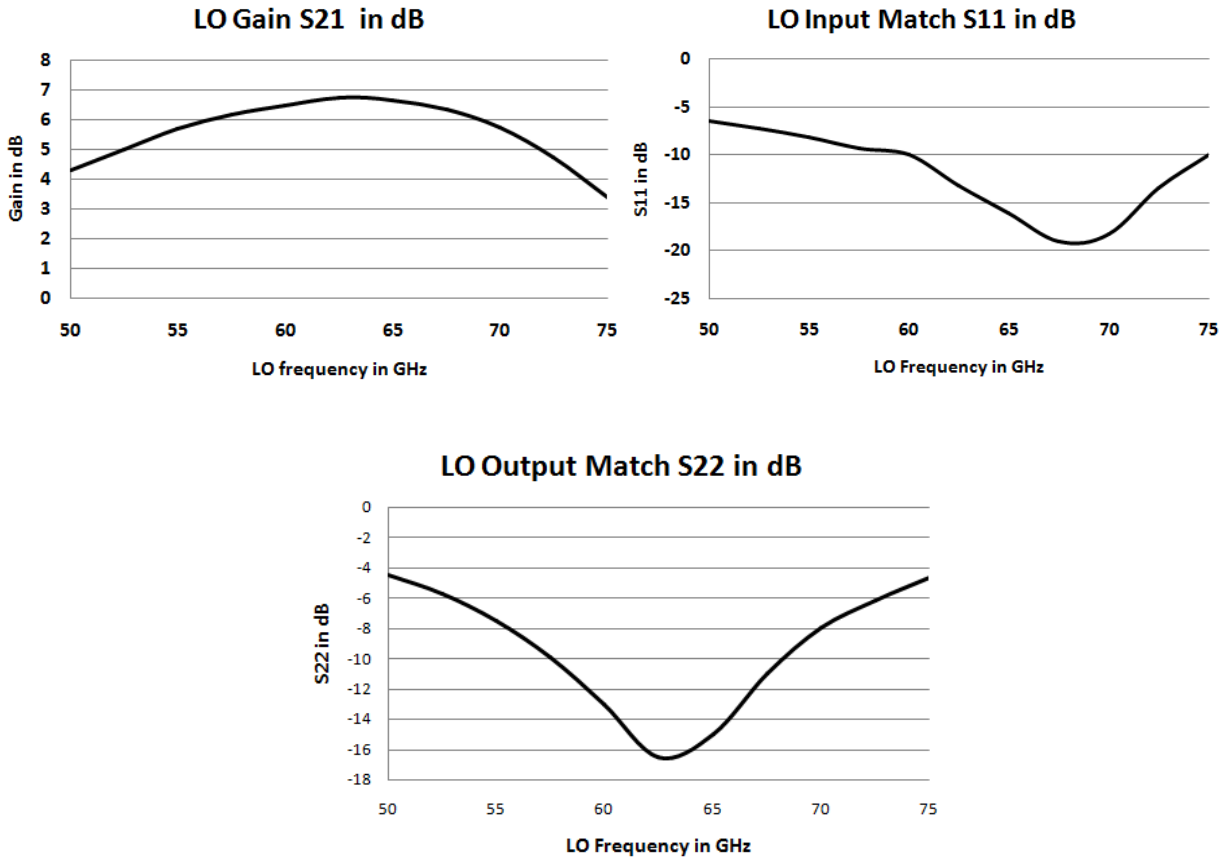


Figure 2.30: Simulation results of LO distribution network

2.7 Design of Printed circuit boards

Two PCBs have been designed for measurement of the down-converter chips. PCB-1 is for measurement of single down-converter chip performance (See Figure 2.31). It has differential RF input and a single ended IF output. Rogers Corporation RT/Duroid 5870 high frequency laminate is used for PCB fabrication. It has the lowest electrical loss and uniform electrical properties over entire frequency band of interest [37]. It also has a very low dielectric constant (Er - 2.333), meaning that machining specifications are relaxed in comparison to higher materials with higher dielectric constants. Tweak points are incorporated on the left top and bottom of the chip of the PCB for additional tuning if necessary. The DC bias is provided from right side of the chip. Vias provide proper shielding. The PCB was designed using AUTOCAD and simulated in HFSS.

PCB-2 was designed to permit testing of the LO feed through between two down-converters chips in cascade (See Figure 2.32). The LO output of chip1 is 100Ω differential and it continues to the LO input of chip-2. A 6mm long differential transmission line connects the LO output of chip-1 to LO input of chip-2. The width of the signal line is 5mils and a gap of 3mils is maintained between the differential lines. The loss of 4dB associated with this transmission is taken into account in the design of LO driver. Vias surrounding the differential lines provide proper shielding and reduce any interference. I am highly thankful to Prof. Neal Erickson and Prof. Gopal Narayanan (UMass Astronomy) for their contribution in PCB design.

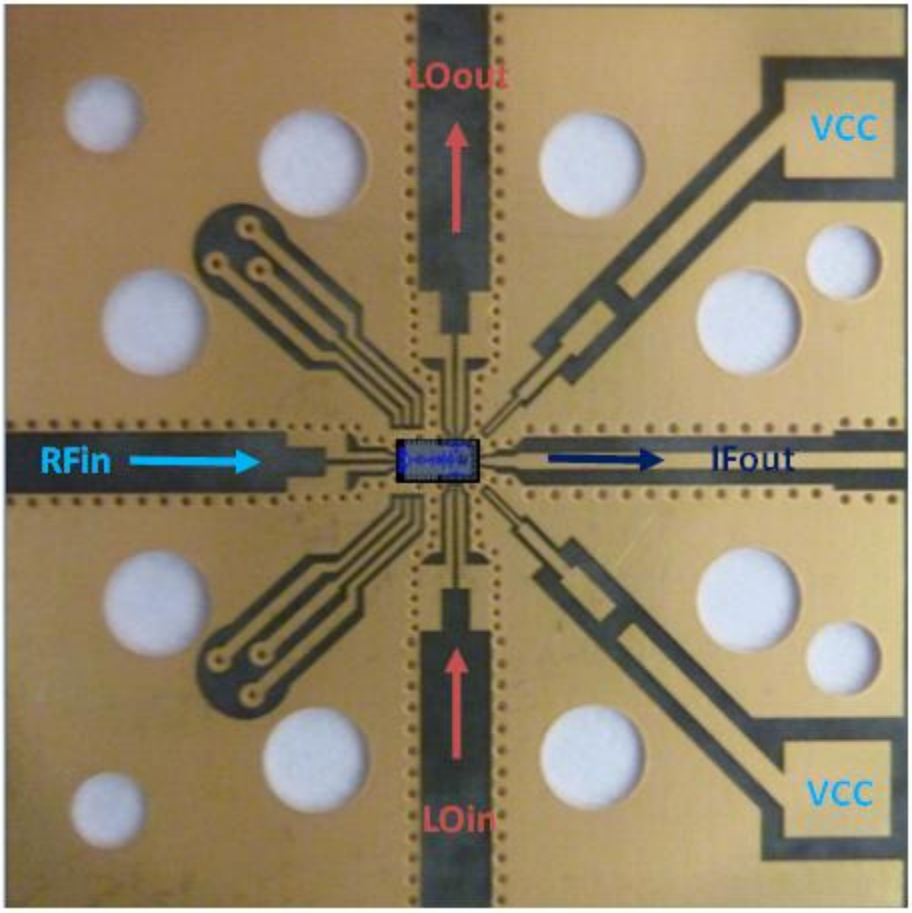


Figure 2.31: Fabricated Printed circuit board -1 for measuring down-converter

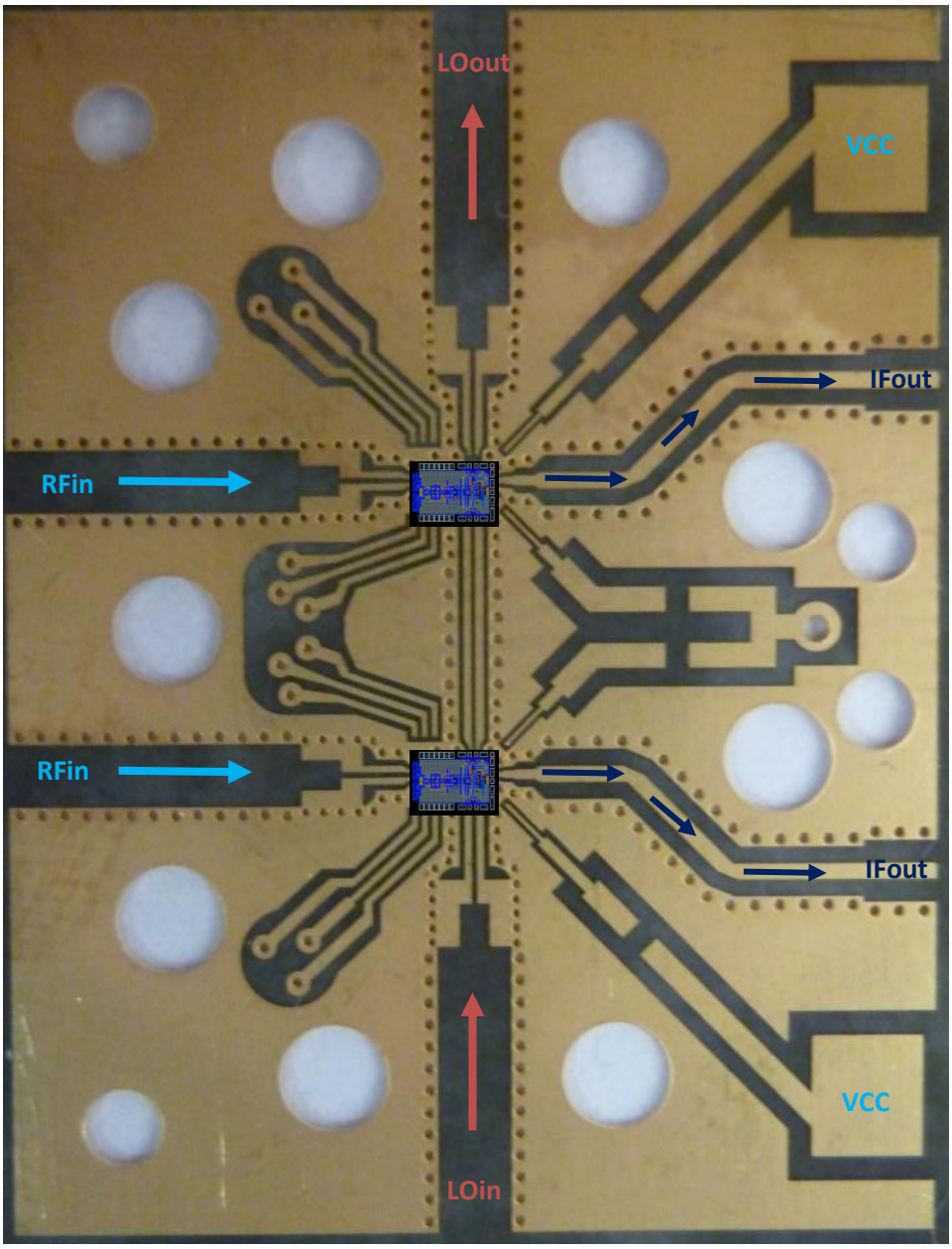


Figure 2.32: Fabricated printed circuit board-2 for measuring the LO feed through between down-converter chips in cascade.

CHAPTER 3

MEASUREMENTS AND ANALYSIS

Measurements of the SiGe down-converter chip measurements were carried out at the Millimeter Wave Instrumentation Lab, UMass Astronomy. The measurements were lead by Prof. Neal Erickson (UMass Astronomy). The following measurements are of interest:

1. Conversion Gain, input match and output match – Section 3.1.

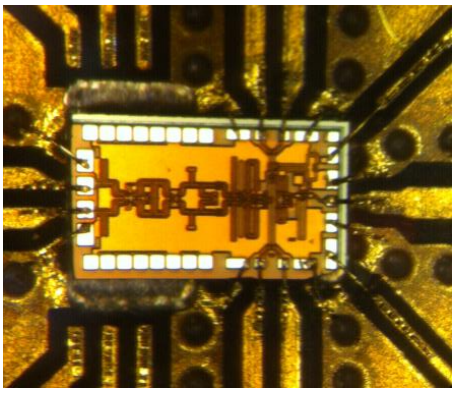
2. Noise figure – Section 3.2

3. LO driver circuitry input match, output match and Gain – Section 3.3

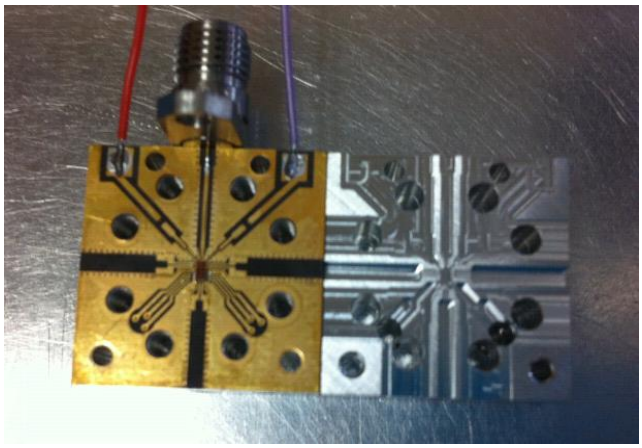
Before measurements, the chips had to be bonded to the PCB (see section 2.7) and packaged in a waveguide module. Fig 3.1a to 3.1c shows the bonded SiGe down-converter chip and packaged waveguide module used for measurement of the chips. Gold wire bonds were made to bond pads on chip to the signal lines on the PCB. The wire bonding was carried out by Vern Fath using a K&S wire bonder. The waveguide module was designed and fabricated by Prof.Gopal Narayanan and Ron Groslein at UMass Astronomy – mm-wave lab. 8mil vias were fabricated around the signal transmission lines for conducting waveguide walls. They provide good shielding. The DC supply to the chip comes in from the right side of the PCB (2^{nd} stage down-converter attached to this module). The differential RF and LO signals are routed

through GCPW lines. They transform to differential slot lines at the chip for ease of bonding.

(a)



(b)



(c)

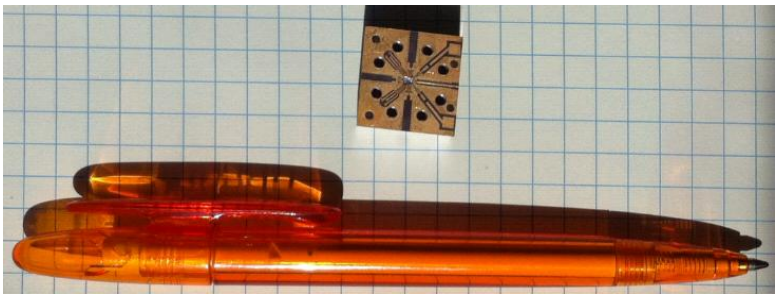


Figure 3.1: a) Bonded SiGe down-converter chip. b) Packaged aluminum waveguide module for measurement of the down-converter chip. c) Size comparison between the module and a standard pen.

3.1 Setup for measuring SiGe Down-converter

The setup for measuring the conversion gain, return loss and output match is shown in Figure 3.2. A HP scalar network analyzer is used for S parameter measurement. Port-1 was connected to the HP sweep oscillator for generating the RF signal. The input RF signal was provided by frequency multiplying the HP sweep oscillator output signal by factor of six. This RF input signal could be swept from 70GHz to 90GHz. The LO input was provided by frequency multiplying the HP synthesized sweeper signal by factor of four. The LO output was terminated in 100Ω differential impedance. The IF output of the down-converter was connected to a power detector, which drives Port-2 of HP scalar network analyzer. Additional attenuators were connected to enable control over the RF input and IF output signal levels.

Figures 3.3 – 3.5 shows the measured and simulated conversion gain of the SiGe down-converter. Due to parasitics in the wiring to the transistors – a factor that went unaccounted for in the design process - the measured results are off in frequency with respect to simulated results. Chapter-4 will discuss this problem in detail and how it was resolved in the following tape-out. Figure 3.3 shows the conversion gain of the chip. There is a close match between the measured and simulation results (with parasitics included). Figure 3.4 shows the AC gain simulation results of LNA (with parasitics included) for observation of the performance below RF band. Figure 3.5 shows the input and output match comparison between measured and simulation. As the input network was less sensitive to parasitic wiring effects, the measured results are quite close to expectation.

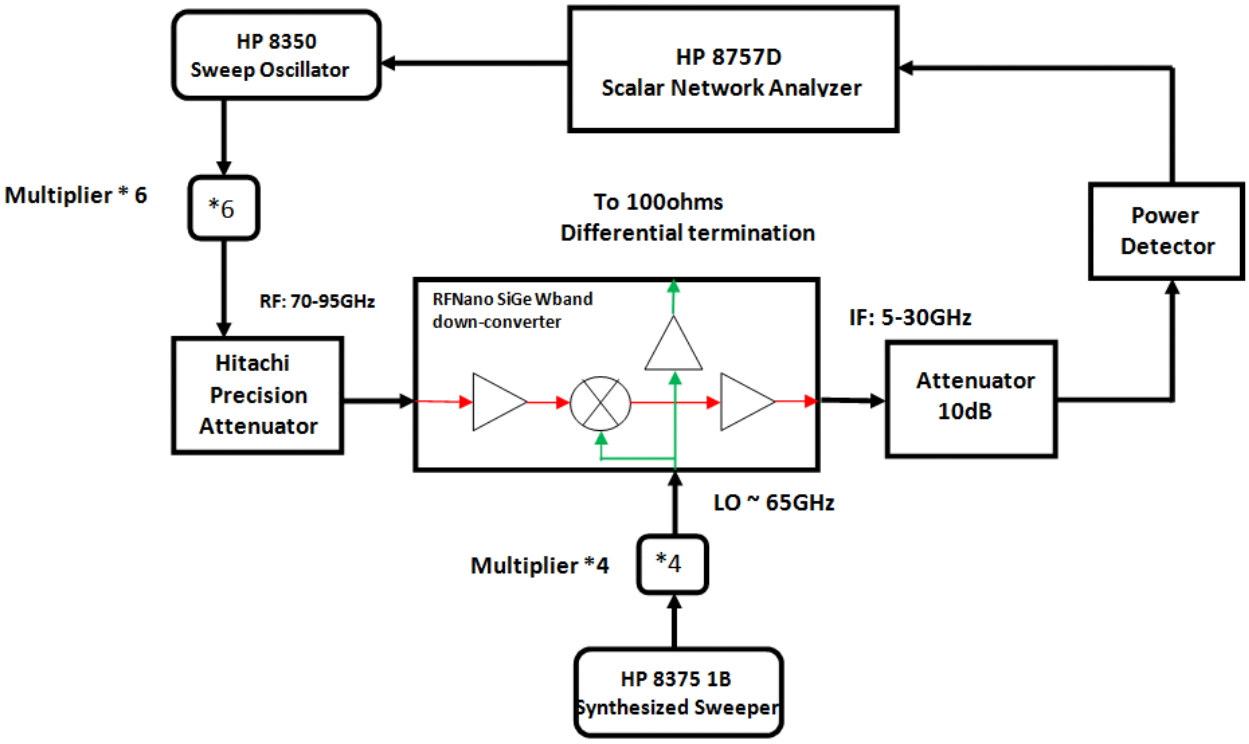


Figure 3.2: Setup for measuring SiGe Down-convertor.

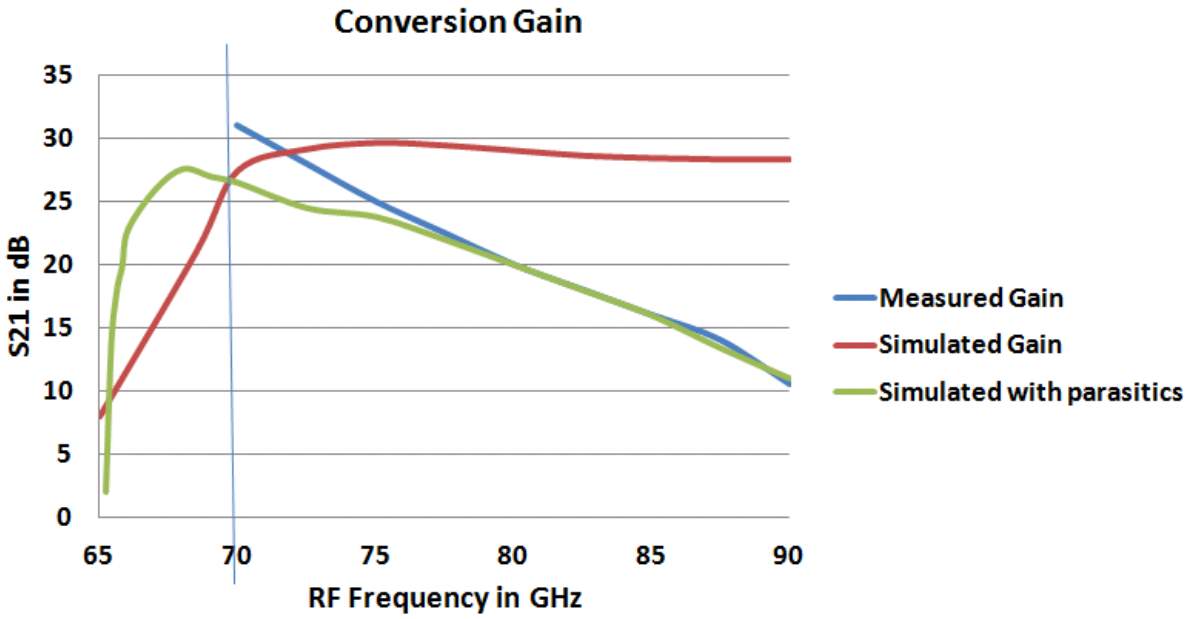


Figure3.3: Conversion gain of SiGe down-converter.

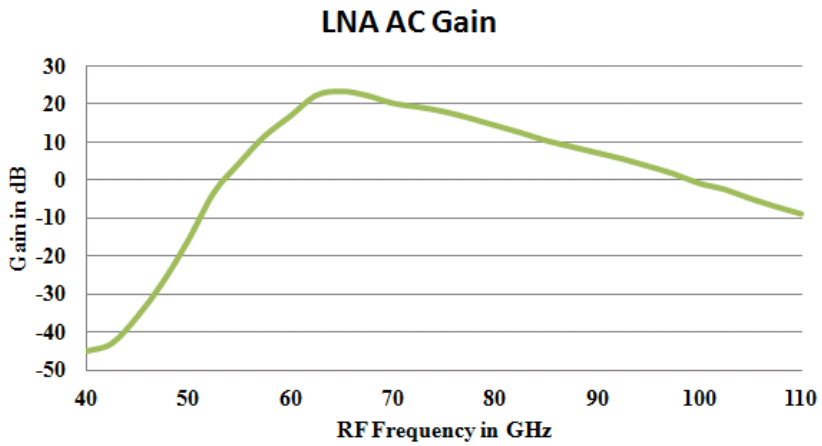


Fig 3.4 AC gain of LNA simulated with parasitics.

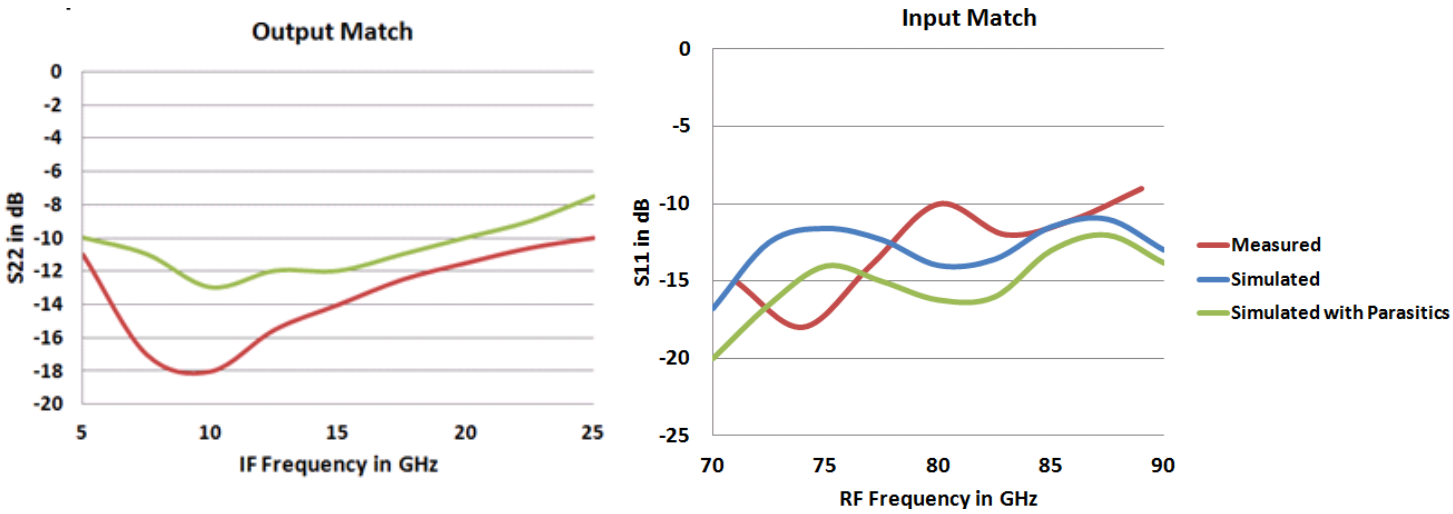


Figure 3.5: Input and output match of SiGe down-converter

Note – Conversion gain (see Fig 3.3) and LNA AC gain (see Fig 3.4) simulation with parasitics results are shown below 70GHz to observe the effect of image sideband on noise performance (See section 3.2).

3.2 Setup for measuring Noise Figure

The setup used for measuring noise figure is shown in Figure 3.6. The Y-factor noise measurement method was used for measuring noise figure of the down-converter [35]. Two noise sources T_{hot} (at 290K) and T_{cold} (at 77K) were used for measuring Y-factor (see equation 3.1).

$$\text{Yfactor} \quad Y = \frac{Nhot}{Ncold} = \frac{(Thot+Te)}{(Tcold+Te)} \qquad \text{equation 3.1}$$

$$\text{Noise figure} \quad NF = 10*\log\left(1+\frac{Te}{To}\right) \quad \text{in dB} \qquad \text{equation 3.2}$$

In equation 3.1 Nhot is measured output noise due to Thot source, Ncold is measured output noise due to Tcold source, Te is noise temperature of down-converter to be determined. From Y-factor the noise temperature is determined. Noise figure is obtained from noise temperature using equation 3.2. An narrow band IF filter (200MHz) was used to set the noise bandwidth. HP Power meter was used for measuring the output noise power.

Figure 3.7 shows the noise figure comparison between the simulation and measurements. Due to non availability of the IF filters at different IF frequencies the noise figure measurement was carried out at single IF frequency (see Fig 3.7b). The result was very close in match with simulation (with parasitics) at LO of 65GHz. From the measurement results we can see that for LO frequencies below 65GHz the noise figure was decreasing. This interesting result is being investigated to see the feasibility of using

this down-converter chip for a lower LO frequency (58GHz). This is still in research and not yet finalized. The noise figure increases with frequency is due to gain roll-off associated with the low noise amplifier. LNA when simulated with parasitics (see Fig 3.3) has some gain below 70GHz. This may be the reason for the noise increase due to image frequency at 63GHz.

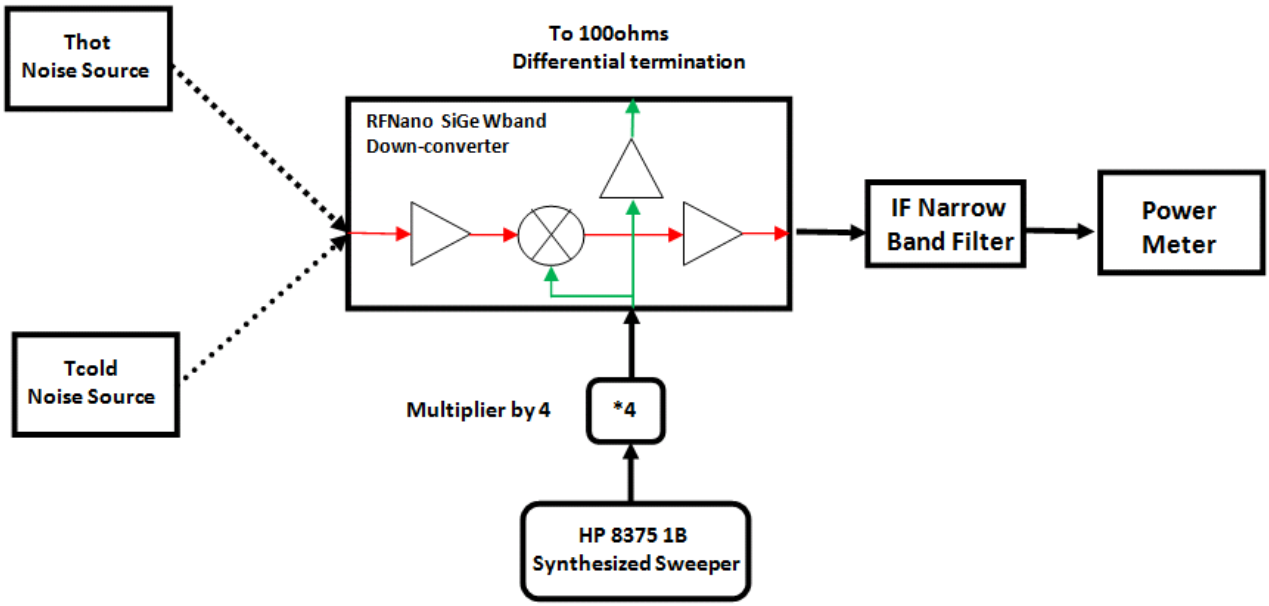


Fig 3.6: Setup for measuring Noise Figure

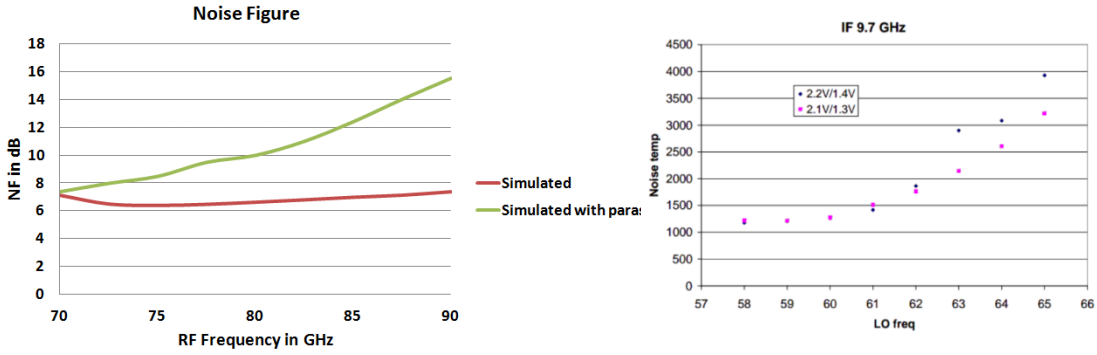


Figure 3.7: Noise Figure of SiGe down-converter (a) Simulation with parasitics (green) and without parasitics (red) (b) Measured noise figure at IF of 9.7GHz for different LO frequencies (57GHz to 66GHz).

3.3: Setup for measurement of LO distribution network

The setup for measurement of the LO distribution network is shown in Figure 3.8. As mentioned in section 2.5 the LO distribution network is responsible for providing the LO signal for the mixer and also to provide an LO signal to the next down-converter in cascade. The important measurements are the gain along the LO path and the LO input match. The differential LO signal is provided by a fin line based balun that is incorporated in the PCB module of the down-converter (see section 2.6). The S-parameter measurements are carried out using HP 8757D scalar network analyzer. The LO input is obtained by frequency multiplying the output of an HP sweep oscillator by factor of four (Port 1 of network analyzer is synchronized with sweep oscillator). The amplified LO output power is detected by power meter (Port 2 of the network analyzer is synchronized with Power detector output).

Figures 3.9 shows the comparison between measured and simulated results of the LO driver circuitry. The gain along the LO path is shifted lower in frequency due to the same issue with parasitic wiring effects that is described above (Chapter 4 will discuss this in more detail). The input match is also poor due to higher bond wire inductance and due to the wrong instantiation of input capacitor (100fF instead of 50fF).

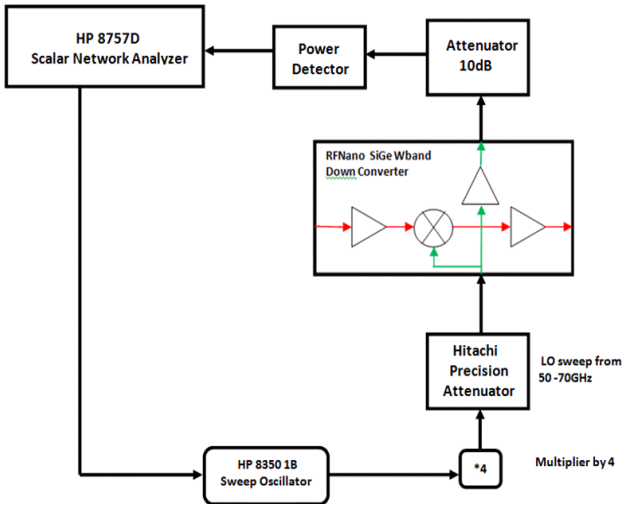


Figure 3.8: Measurement of LO distribution network

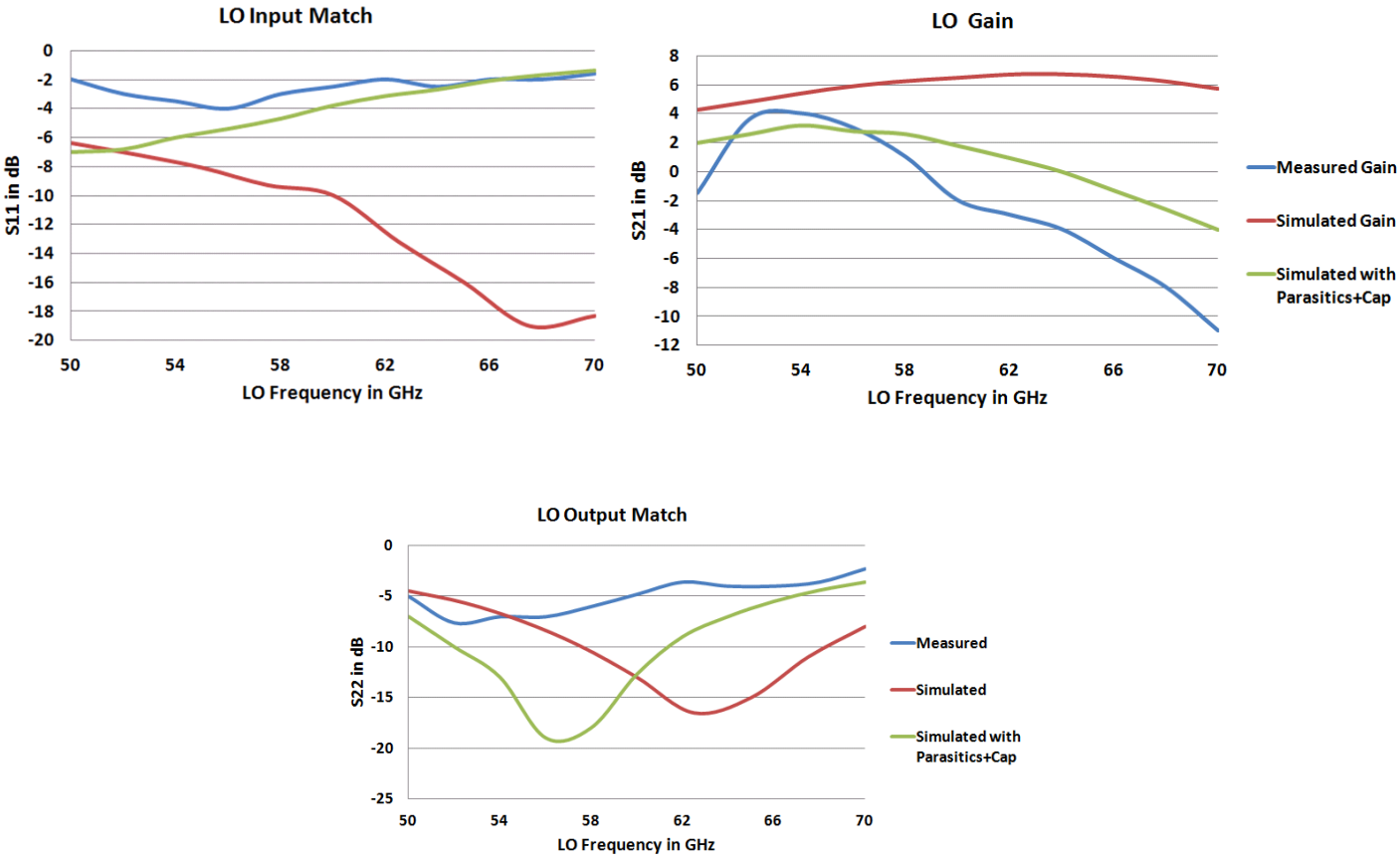


Figure 3.9: LO driver input match, gain and output match

CHAPTER 4

REDESIGN OF SIGE DOWN-CONVERTER (IMPROVED VERSION)

The performance of the first down-converter chip mentioned in the previous chapter had several significant shortcomings due to parasitic wiring effects which were not accounted for in the design process. The issues affected like the gain flatness, RF output match, noise figure and all-around LO driver performance. When measurements were done we came across the results which we had not expected. After debugging for couple of days understanding what went wrong between the simulation and measurements, we came across the following factors which resulted in performance getting worse.

1. Reliability layout – an option in IBM PDK – was employed for all npn transistors assuming that they would to perform better than regular npn in terms of reliability. These npn transistors have a larger collector area compared to regular ones. (Shown in figure 4.1). Each of these reliable transistors are having 15-20fF parasitic capacitance between collector to substrate (See figure 4.2). This parasitic capacitance is not included with the base VBIC model, but only shows up in post extraction simulation. Unfortunately, parasitic extraction was not carried out in the original design cycle and the effect was only simulated post-measurement. These parasitics caused the major gain roll off in the low noise amplifier at higher frequencies and also noise degradation at higher frequencies. This issue was resolved in the 2nd down-converter chip design by doing parasitic extractions of each transistor and replacing the major reliable npn transistors in amplifiers and

mixers with regular npn transistors (lower parasitic capacitance). While this helped reduce the effect of these extra capacitances, to obtain the desired response retuning of the matching networks was also required.

2. The second major issue was the wrong instantiation of one of the input match network capacitors (100Ff instead of 50fF). This resulted in poor LO result. This was corrected in the 2nd IC design.
3. The third major issue with respect to poor input and output match along LO driver circuitry was due to assumption of lower bond-wire inductance (ribbon bond-wire - 30pH). But this assumption went wrong during measurement phase. Due to technical issues we could not use ribbon bonds and had to use wire bonds. These wire bonds have higher inductance (100pH) compared to ribbon bonds (30pH). This effect was taken into account in the design of 2nd down-converter chip.
4. The fourth major reason for measured results to be slightly off the simulated results is due to change in the design of balun. During the design of the first chip we had plans on using waveguide balun and simulations were done using S-parameters of this balun. But just a few days before measurement the plan to use waveguide balun got changed due to complexity and higher cost involved in the fabrication. The measurements were done using these new baluns which resulted in results to be slightly affected. The 2nd down-converter chips are designed and simulated with these new baluns.
5. The fifth and final reason for poor LO input match is due to poor dicing on the chip along the LO input side. Due to this extra substrate we had to bond the LO

input using 4mil long bond wire instead of 1mil which further increased the input inductance and poor input mismatch.

Section 4.1 and 4.2 gives the simulation results of this improved down-converter IC (IC-2). In this simulation the issues mentioned above have been accounted for. Therefore, this second down-converter chip is expected to perform to meet the specifications.

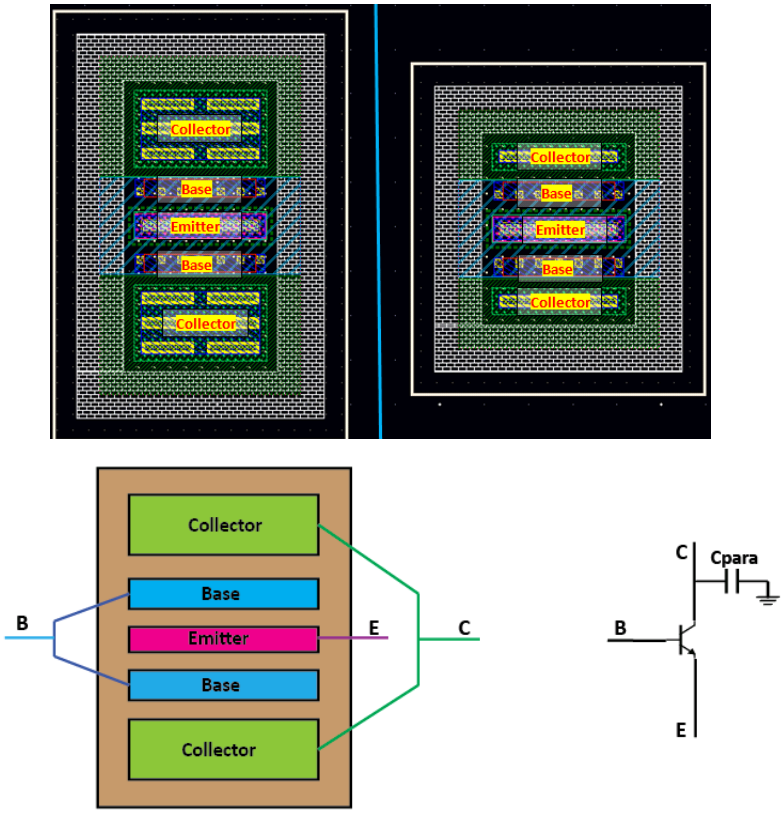


Figure 4.1: Top: comparison between npn reliable transistor layout (left) and normal npn transistor of same size (width,length) (right). Bottom: reliable transistor layout with additional parasitic capacitance (Cpara) between collectors to ground.

4.1 Simulation results of SiGe down-converter IC-2

Figures 4.2 shows the simulation results of down-converter IC-2. This simulation is done by taking into account all factors – parasitic models wiring effects, bondwire inductances, EM models of transmission lines and S-parameters of balun. The conversion gain shown in Figure 4.2 meets the specification requirement (> 20dB). This gain can be controlled by additional tweak bias points of LNA, mixer and IF driver. The gain rolls off below 5GHz. The input match and output match are < -10dB. Noise figure is < 9dB over entire RF band

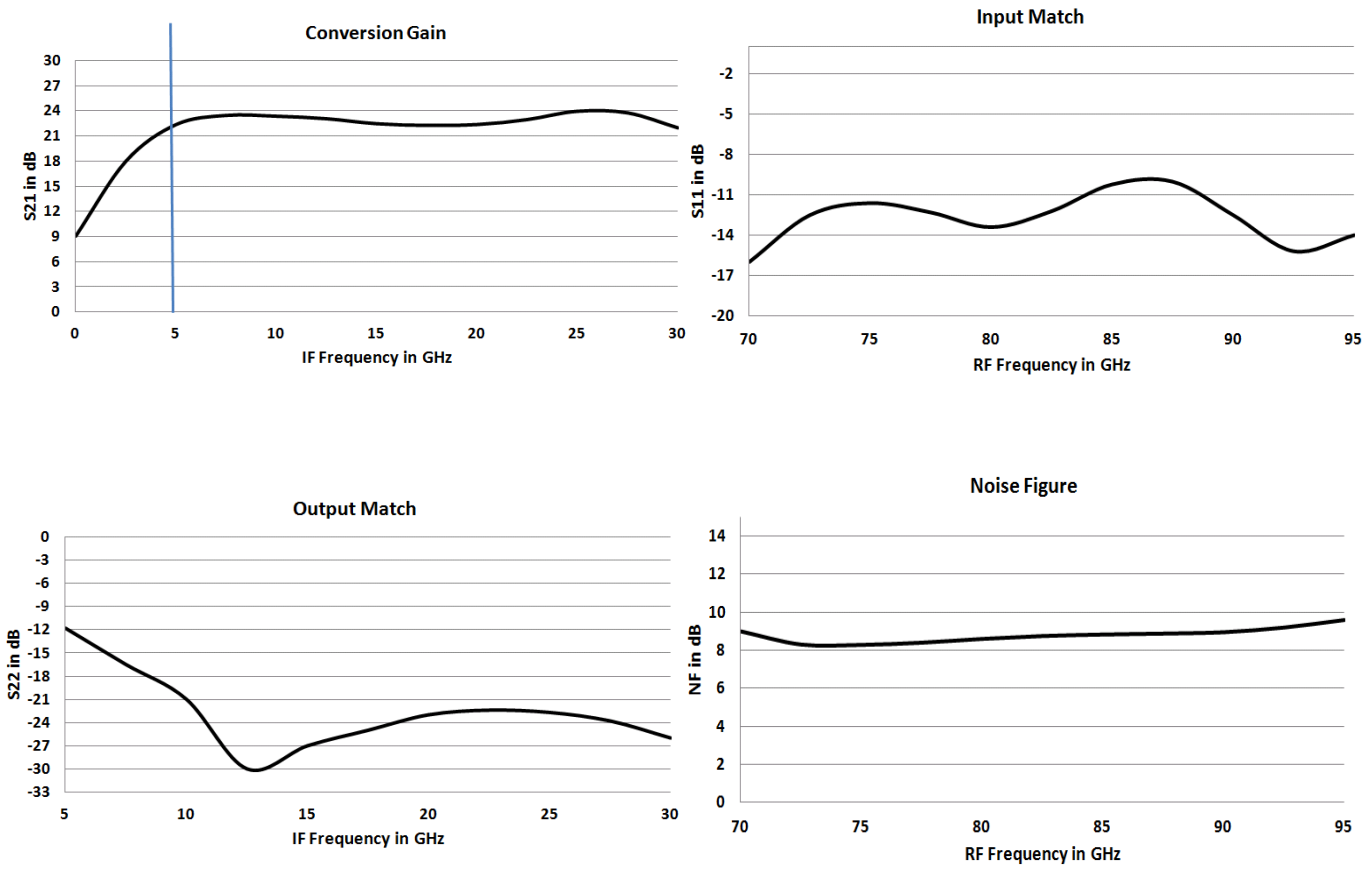


Figure 4.2: Simulation results of SiGe down-converter IC-2

4.2 Simulation results of LO distribution network-IC2

Figure 4.3 shows the simulation results of LO distribution network of IC-2. The LO driver gain is greater than 4dB at 65GHz to overcome any loss associated with signal transmission between chips (see LO gain Figure 2.31). The gain BW is kept broad enough to have flexibility of changing the LO frequency. The input and output match are better than -10dB. The output of LO driver was terminated with a 100Ω differential impedance. Here again for simulations we had taken into account all the parasitics associated with LO driver and buffer, and the EM model of the LO distribution network shown in Figure 2.28.

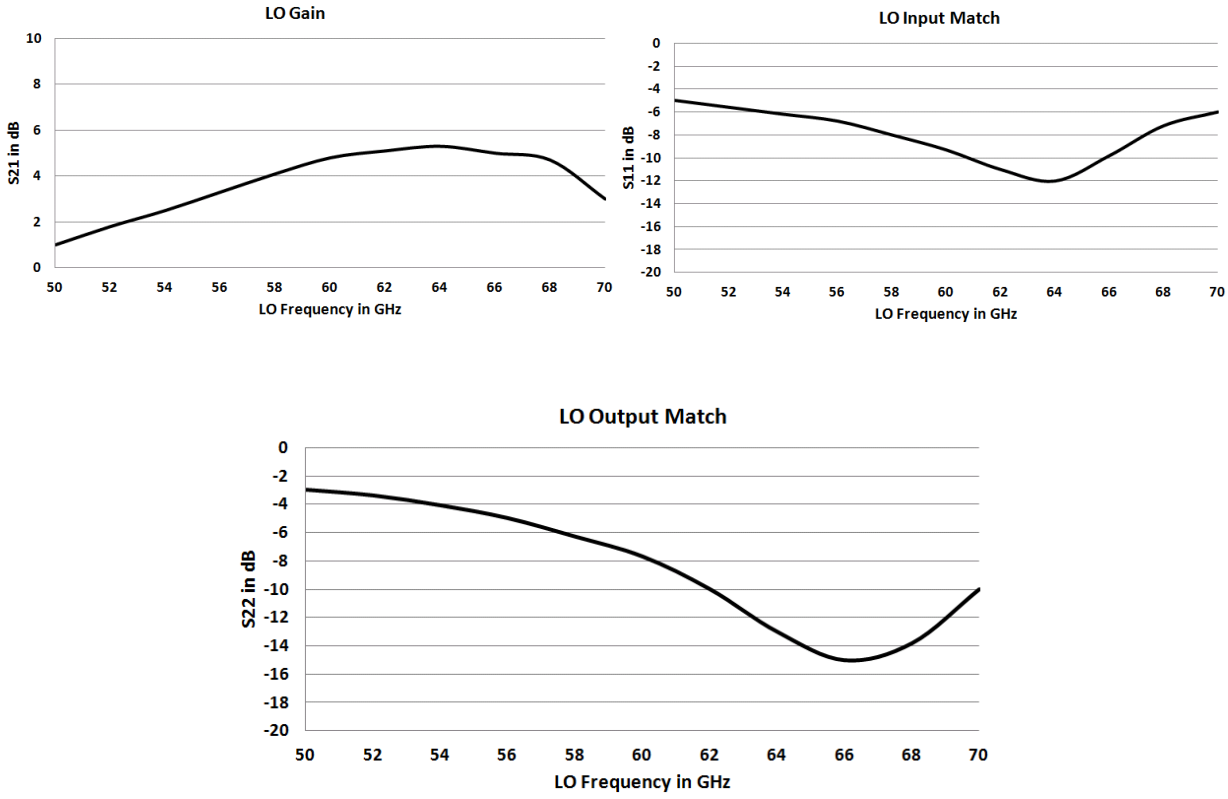


Figure 4.3: Simulation results of LO distribution network of IC-2

CHAPTER 5

SUMMARY AND PROPOSED NEXT STEPS

A Wband SiGe down-converter for a phased focal plane array receiver was designed, simulated and measured. Once integrated with the front end, the down-converter will be an important part of a state of the art W-band receiver for astronomy applications. The first down-converter chip performance was off from expectations due to a failure to include parasitic wiring effects into the simulation, a mistake in a capacitance value in the fabricated chip, and changes in the balun and bond-wire inductances. These were taken into account during the second chip design. This down-converter was simulated with all parasitics (R,L,C), EM models of transmission lines and S-parameters of balun and bond-wire inductances (HFSS simulation results). The measurements of the first set of chips have provided a good understanding of the working of these chips, which could be used for RF band of 70 – 85GHz. Beyond this the performance starts getting worse. The second set of chips should work over the entire band and also could extend the band to 100GHz.

The next steps involves: 1) the measurement of the second set of chips. 2) bonding all 8 chips - in cascade as shown in single row of an array (Figure 1.10) and measuring the LO distribution among chips. 3) Following successful measurement of chips, the IC will be integrated with front end and PFPA receiver system will be characterized. Having done the entire receiver measurement, the goal is to place the

receiver on Green Bank Telescope/Large millimeter telescope for measuring astronomy spectral lines of interest (Quarter-2 of 2014).

APPENDIX

MATLAB CODE OF MATCH NETWORKS

A.1 Matlab code for synthesis of 4th order match network

```
%REFERENCE:
%Prof Bardin  Active microwave circuits notes on Broad band LNA design
%Microwave engineering - Pozar; chapter - impedance matching , filters
%Microwave filters, impedance match nw - Mathei, Young and Jones

loss = 0;
ripple = 1;
wu = 1.26;
k0=10^(loss/10);
kc0=10^(ripple/10)-1;
alpha=wu-1/wu;
a0=4*kc0/alpha^4;
a2=-4*kc0*(4+alpha^2)/alpha^4;
a4=((8+(4+alpha^2)^2)*kc0+alpha^4*k0)/alpha^4;
a6=-4*kc0*(4+alpha^2)/alpha^4;
a8=4*kc0/alpha^4;
%wu=1;
a0p=wu^2*a0;
a2p=wu^2*a2;
a4p=wu^2*a4;
a6p=wu^2*a6;
a8p=wu^2*a8;
num=[a8p 0 -(a6p-1) 0 a4p 0 -a2p 0 a0p];
den=[a8p 0 -a6p 0 a4p 0 -a2p 0 a0p];
kc0/alpha^4;
y=roots(num);
ry=[1,2,5,6];
z=roots(den);
rz=[3,4,7,8];
sgne=1;
numg=sgne*conv([1 y(ry(1))],conv([1 y(ry(2))],conv([1 y(ry(3))],[1 y(ry(4))])));
deng=conv([1 z(rz(1))],conv([1 z(rz(2))],conv([1 z(rz(3))],[1 z(rz(4))])));
numz=(deng+numg)/2;
denz=(deng-numg)/2;
```

C1 = real(denz(4));
L2 = real(numz(2)/denz(3));
C3 = real((numz(3)-L2*C1-numz(1)/(L2*C1))/L2);
L4 = real(numz(1)/(C3*L2*C1));
R4 = real(denz(3)/(C3*C1));

C1F = C1/(SF*K);
C3F = C3/(SF*K);
L2F = L2*SF/K;
L4F = L4*SF/K;
R4F = R4*SF;

A.1.2 Design equations associated with 4th order match network

Determination of Insertion loss function of match network

1. Consider 2nd order Chebyshev filter function

$$Tm(\omega) = 2(\omega)^2 - 1$$

2. Determine low pass IL function

$$\text{IL} = Ko + Kco * [Tm(\omega)]^2$$

Ko = 1
Kco = 0.26

$$\text{IL} = 1 + 0.26 * [2(\omega)^2 - 1]^2$$

3. Low pass to Band pass transformation of IL function [28]

Lower frequency: ωl = 70GHz * 2pi
Higher frequency: ωh = 95GHz * 2pi

Band pass IL function

$$\text{IL} = \frac{(16.64*\omega^8 - 70.72*\omega^6 + 109.42*\omega^4 - 70.72*\omega^2 + 16.64)}{\omega^4}$$

4. Determine the Reflection coefficient Γ(s) where s = j*ω

$$|\Gamma(s)|^2 = 1 - \frac{1}{IL}$$

$$|\Gamma(s)|^2 = \frac{(16.64 * s^8 + 70.72 * s^6 + 108.42 * s^4 + 70.72 * s^2 + 16.64)}{(16.64 * s^8 + 70.72 * s^6 + 109.42 * s^4 + 70.72 * s^2 + 16.64)}$$

Use Matlab code (see appendix A.1) to determine Γ(s)
Note – Select right LHP poles and suitable zeros. – They determine the network elements

5. Determine input impedance function Z(s)

$$Z(s) = \frac{1+\Gamma(s)}{1-\Gamma(s)}$$

$$Z(s) = \frac{0.55*s^3 + 0.18*s^2 + 0.55s}{2*s^4 + 0.55*s^3 + 4.42*s^2 + 0.55*s + 2}$$

Doing Numerical analysis or fractional expansion the ideal elements of the match network are synthesized.

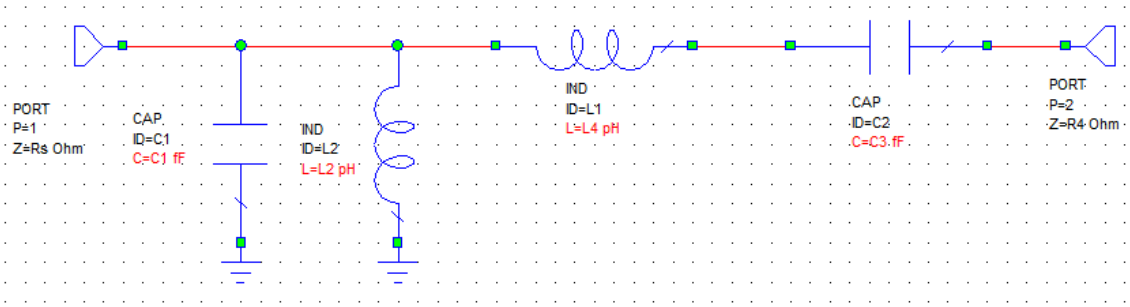


Fig A.1: 4TH Order match network

A.2 Matlab code for synthesis of 6th order match network

```
%REFERENCE:
%Prof Bardin  Active microwave circuits notes on Broad band LNA design
%Microwave engineering - Pozar; chapter - impedance matching , filters
%Microwave filters, impedance match nw - Mathei, Young and Jones

Ko  = 1; % 0dB attenuation in pass band
Kco = 0.122; % 0.5dB ripple in pass band
a = 2.066; % wo/(wh-wl) where wo = norm(sqrt(wh*wl))=1; wh = 2pi*105G; wl =
2pi*65G
SF = 50;   % impedance scaling factor
K = 52e10; % frequency scaling factor
wh = 1.26;
% INSERTION LOSS IL %

a12 = 16*a^6*Kco;
a10 = -(24*a^4+96*a^6)*Kco;
 a8 = (9*a^2+96*a^4+240*a^6)*Kco;
 a6 = Ko - (144*a^4+320*a^6+18*a^2)*Kco;
 a4 = (9*a^2+96*a^4+240*a^6)*Kco;
 a2 = -(24*a^4 + 96*a^6)*Kco;
 a0 = 16*a^6*Kco;

syms w;
IL = vpa(a12*w^12+a10*w^10+a8*w^8+a6*w^6+a4*w^4+a2*w^2+a0)/w^6;
ILdB = 10*log10(IL);
d = 0:0.01:2;
y = subs(ILdB,d);
plot(d, y);

%Insertion loss function with -6dB slope %

 ILs = vpa(wh^2*(a12*w^12+a10*w^10+a8*w^8+a6*w^6+a4*w^4+a2*w^2+a0))/w^8;
ILsdB = 10*log10(ILs);
d = 0:0.01:2;
y = subs(ILsdB,d);
plot(d, y);

a12s = 16*a^6*Kco*wh^2;
```

```
a10s = -(24*a^4+96*a^6)*Kco*wh^2;
 a8s = (9*a^2+96*a^4+240*a^6)*Kco*wh^2;
 a6s = -(-Ko + (144*a^4+320*a^6+18*a^2)*Kco)*wh^2;
 a4s = (9*a^2+96*a^4+240*a^6)*Kco*wh^2;
 a2s = -(24*a^4 + 96*a^6)*Kco*wh^2;
 a0s = 16*a^6*Kco*wh^2;

% REFLECTION COEFFICIENT Gamma %

Gamma2w = vpa((a12s*w^12+a10s*w^10+(a8s-
1)*w^8+a6s*w^6+a4s*w^4+a2s*w^2+a0s)/(a12s*w^12+a10s*w^10+a8s*w^8+a6s*w^6
+a4s*w^4+a2s*w^2+a0s));
syms s
w = -s*1i;
Gamma2s = vpa((a12s*w^12+a10s*w^10+(a8s-
1)*w^8+a6s*w^6+a4s*w^4+a2s*w^2+a0s)/(a12s*w^12+a10s*w^10+a8s*w^8+a6s*w^6
+a4s*w^4+a2s*w^2+a0s));
Gz = roots([a12s 0 -a10s 0 (a8s-1) 0 -a6s 0 a4s 0 -a2s 0 a0s]);
Gp = roots([a12s 0 -a10s 0 a8s 0 -a6s 0 a4s 0 -a2s 0 a0s]);
x = [3,4,7,8,11,12];
y = [1,2,5,6,9,10];
GammaN = conv([1 Gz(x(1))],conv([1 Gz(x(2))],conv([1 Gz(x(3))],conv([1
Gz(x(4))],conv([1 Gz(x(5))],[1 Gz(x(6))])))); % Numerator of reflection coeffcient
GammaD = conv([1 -Gp(y(1))],conv([1 -Gp(y(2))],conv([1 -Gp(y(3))],conv([1 -
Gp(y(4))],conv([1 -Gp(y(5))],[1 -Gp(y(6))])))); % Denominator of reflection coeffcient

% Input impedance Zin %

ZinN = GammaD + GammaN; % Numerator of Input impedance Zin
ZinD = GammaD - GammaN;% Denominator of Input impedance Zin
Z1N = ZinN;
Z1D = ZinD;

% %synthesis of network elements%

C1 = real(Z1D(6)/Z1N(7));
Z2N = [Z1N(1) Z1N(2) Z1N(3)-Z1D(2)/C1 Z1N(4)-Z1D(3)/C1 Z1N(5)-Z1D(4)/C1
Z1N(6)-Z1D(5)/C1 Z1N(7)-Z1D(6)/C1];
Z2D = Z1D;
L2 = real(Z2N(1)/Z2D(2));
Z3N = [Z2N(1)-L2*Z2D(2) Z2N(2)-L2*Z2D(3) Z2N(3)-L2*Z2D(4) Z2N(4)-L2*Z2D(5)
Z2N(5)-L2*Z2D(6) Z2N(6)-L2*Z2D(7) Z2N(7)];
Z3D = Z2D;
Y3N = Z3D;
Y3D = Z3N;
L3 = real(Y3D(5)/Y3N(6));
```

```
Y4N = [Y3N(1) Y3N(2)-Y3D(1)/L3 Y3N(3)-Y3D(2)/L3 Y3N(4)-Y3D(3)/L3 Y3N(5)-
Y3D(4)/L3 Y3N(6)-Y3D(5)/L3 Y3N(7)-Y3D(6)/L3];
Y4D = Y3D;
Z4N = Y4D;
Z4D = Y4N;
C4 = real(Z4D(4)/Z4N(5));
Z5N = [Z4N(1) Z4N(2) Z4N(3)-Z4D(2)/C4 Z4N(4)-Z4D(3)/C4 Z4N(5)-Z4D(4)/C4
Z4N(6)-Z4D(5)/C4 Z4N(7)-Z4D(6)/C4];
Z5D = Z4D;
L5 = real(Z5D(2)/Z5N(3));
C6 = real(Z5N(3)/Z5D(4));
R6 = real(Z5N(3)/Z5D(3));

% IMPEDANCE SCALING %

L2F = L2*SF/K;
C1F = C1/(SF*K);
L3F = L3*SF/K;
C4F = C4/(SF*K);
L5F = L5*SF/K;
C6F = C6/(SF*K);
R6F = R6*SF;
```

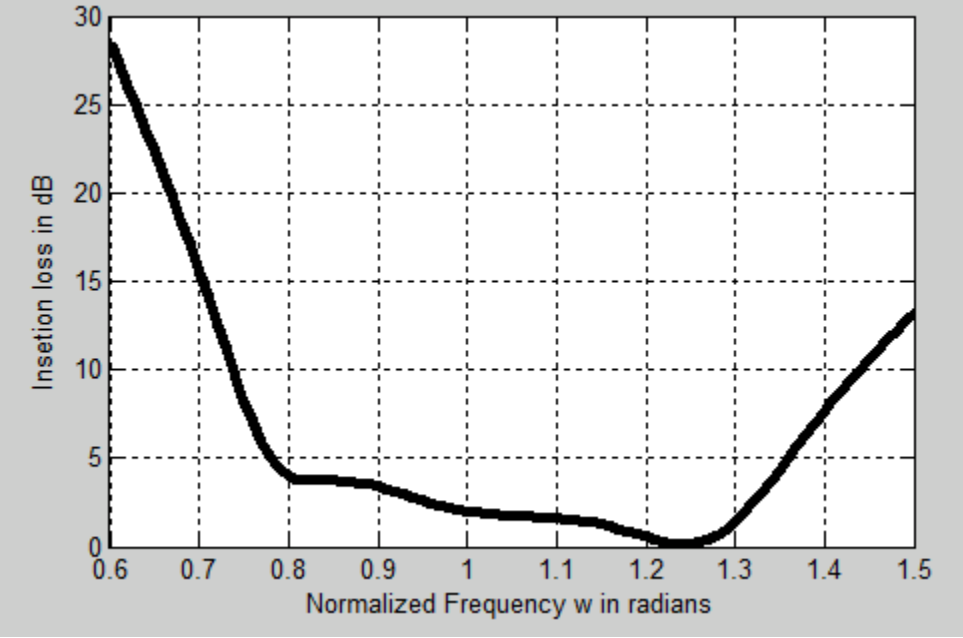


Figure A.2: Insertion loss in dB of 6th order match network

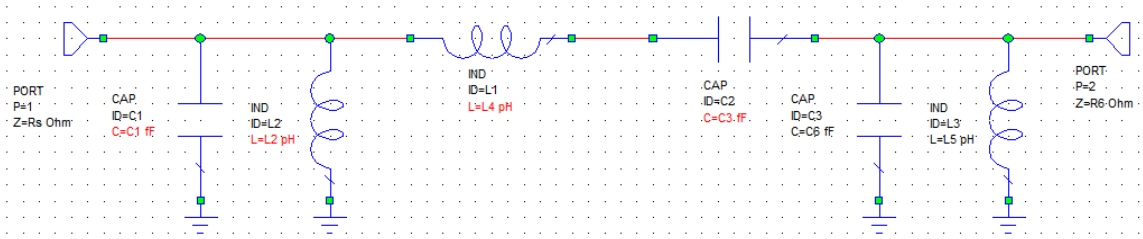


Figure A.3: 6TH Order match network

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