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Impact of Manufacturing Flow on Yield Losses in Nanoscale Fabrics

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IMPACT OF MANUFACTURING FLOW ON YIELD LOSSES IN NANOSCALE FABRICS

A Thesis Presented

by

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ABSTRACT

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Reliable and scalable manufacturing of nanofabrics entails significant challenges. Scalable nano-manufacturing approaches that employ the use of lithographic masks in conjunction with nanofabrication based on self-assembly have been proposed. A bottom-up fabrication of nanoelectronic circuits is expected to be subject to various defects and identifying the types of defects that may occur during each step of a manufacturing pathway is essential in any attempt to achieve reliable manufacturing. This thesis aims at analyzing the sources of defects in a nano-manufacturing flow and estimating the resulting yield loss. It integrates physical fabric considerations, manufacturing sequences and the resulting defect scenarios. This is in contrast to most current approaches that use conventional defect models and assume constant defect rates without analyzing the manufacturing pathway to determine the sources of defects and their probabilities. The manufacturing pathway will be analyzed for identifying the defects introduced during each manufacturing step in the sequence, followed by yield loss estimation.

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CHAPTER 1

INTRODUCTION

Semiconductor nanowires[1][2], spin waves[3] , carbon nanotubes[4][5], and graphene[6]are some of the emerging nano-materials and devices proposed for novel computational fabrics. Reliable manufacturing of nanoscale computational architectures is quite challenging. With the very high defect rates associated with nanoscale manufacturing, different approaches such as built-in defect tolerance[7][8] and reconfiguration[9][10]have been explored for emerging nano-computational fabrics to achieve fault tolerance[11][12]. Most of the prior publications have, focused on the impact of the assumed defects at device/circuit/architectural levels and have not analyzed the potential sources of the defects. For example, a modular approach is used by Patwardhan[13] to reprogram faulty 'nodes' (a functional block) but the source of the defect so assumed has not been discussed. Built-in defect tolerance for stuck-on or stuck-off devices (with up to 10% defect rates) has been considered for the NASIC fabric[7][8][14][15][16]. However, a procedure for analyzing the sources of defects in a nano-manufacturing flow and hence estimating the resulting yield loss has never been employed. The mask overlay related yield loss, particulate limited yield loss, nanowire transfer limited yield loss needs to evaluated to understand the implication of manufacturing steps.

Our goal in this thesis is to analyze the sources of defects from a manufacturing perspective. Identifying the potential defects that may occur during each step of the bottom-up fabrication of nanoelectronic circuits is important since it would provide a better estimate of the defect rates allowing a more accurate yield analysis.

Scalable nanofabric manufacturing techniques have been proposed which utilize lithography masks for functionalization and interfacing in conjunction with nanofabrication based on self-assembly approaches [16][18]. Each step in the manufacturing process can be viewed as a combination of "alignment of a mask for pattern transfer" followed by a "processing step." Defects can be introduced during (a) the alignment of the mask, or (b) the processing step after the mask alignment, and can also be the result of (c) impurities during the manufacturing steps.

Defects introduced during the mask alignment are commonly classified as systematic defects. Systematic yield, Y_S is design and process specific and no definite formula exists. Systematic problems are topology specific and may result in defects with particular characteristics.

Defects introduced during the processing step can be either random or systematic. Process limited Yield loss accounts for the defects introduced during the processing steps in the nano-manufacturing flow. Processing steps like 'nanowire transfer' can be classified as systematic. A careful and thorough analysis of such manufacturing steps is required to understand how a particular fault resulting from defects during these steps would manifest itself in terms of logical and system behavior. This will further pave way for efficient fault mitigation techniques.

Impurity related defects are random in nature. Particulate defect limited yield has been thoroughly researched and well understood in CMOS technology [19][20]. However, as the technology scaled, the influence of random defects from particulates has been in the decline compared to systematic defects [21].Still, random impurity limited yield may influence the final production yield and hence needs to be accounted.

The overall die yield can hence be defined as the product of systematic mechanism limited yield (Y_S) and random-defect limited yield (Y_R) [21].Yield Estimation is a crucial step in the chip

design flow. Early yield estimation helps the designers to adopt a Design-for-Yield (DFY) perspective and thereby achieve better yield margins. Analyzing the defect source and modeling of the fault and yield has always remained a key challenge.

This thesis work focuses on a) identification of defects introduced during each step of a manufacturing pathway, b) estimation of particulate limited yield loss, and c) estimation of systematic yield loss through careful analysis of the manufacturing sequence

1.1 Organization

The thesis is organized as follows. Sections 1.3 and 1.4 discuss the Nanoscale Application Specific Integrated Circuits (NASICs) fabric and the Wire Streaming Processor WISP-0 design mapped to NASIC fabric. Chap.2 discusses the related work in the field of nanofabrics. Chap.3 presents the yield modeling in conjunction with analysis of the nano-fabric manufacturing sequence. Random defect based yield modeling is discussed in Chap. 4. Chap. 5 discusses nanowire alignment, mask overlay and registration evaluation for systematic yield modeling, Chap.6 presents the overall yield estimation and Chap.7 concludes and summarizes the thesis.

1.2 Overview of NASIC's

Nanoscale Application Specific Integrated Circuit (NASICs) is a nanoscale computational fabric [8][14][15][22][23] that implements logic on semiconductor NWs with field effect transistors (FETs), and uses microwires that provide VDD, GND and control signals for data streaming.

In NASICs, design choices at multiple levels are tailored towards the minimization of fabric area and manufacturing requirements. For example, a) by using dynamic circuits and pipelining on the wires, NASICs eliminate the need for explicit flip-flops and therefore can improve the density considerably, b) the dynamic style logic implementation in conjunction with

external sequencing schemes does not require complementary doping for the logic transistors, c) based on 2-level AND-OR logic style, NASIC designs can be optimized to achieve high density. By slight modification of the NASIC dynamic control scheme and circuit style, we can implement arbitrary logic functions with one type of FETs in NASICs. A design using only n-type FETs will implement a NAND-NAND cascaded scheme whereas a design using only p-type FETs will implement a NOR-NOR scheme. Fig. 1 demonstrates the design of a 1-bit full adder implemented in NAND-NAND logic dynamic style [8].

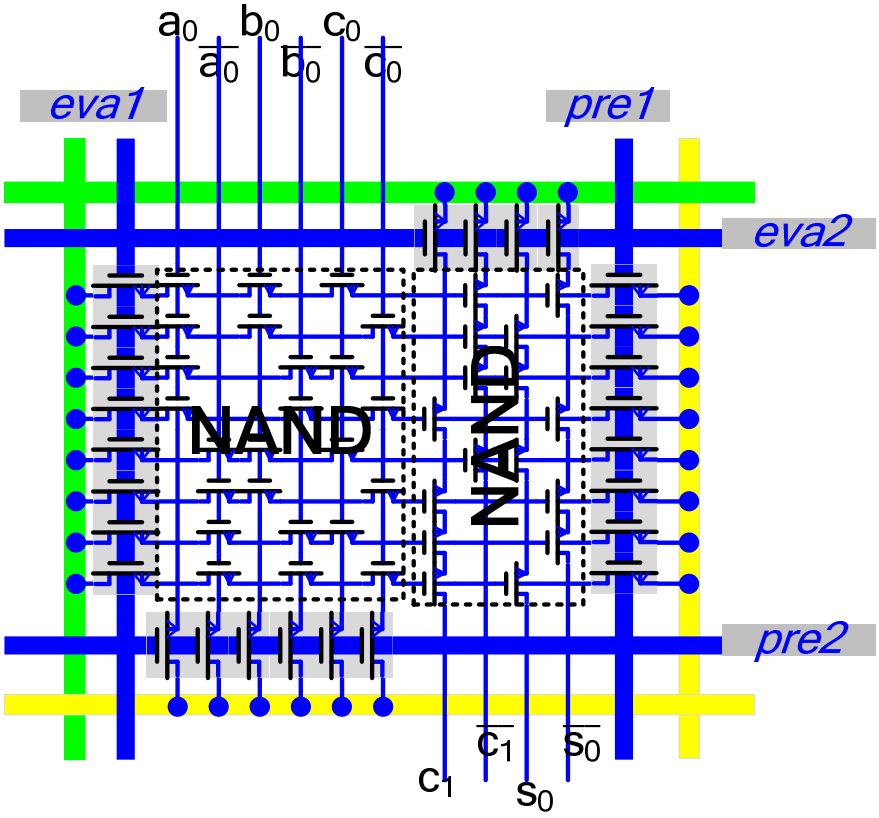

Figure 1. 1-bit Full adder using NASICs [8]

The elemental units in NASICs are known as *nanotiles*. A tile contains for example, an adder or multiplexers. Individual tiles can be connected with nanowires to form a larger multi-tile structure performing an application-specific computation. The nanotile is surrounded by microwires (MWs) which carry ground (Gnd), power supply voltage (Vdd), and control signals for the dynamic evaluation of outputs. Complementary signals are required to implement arbitrary

logic functions in 2-level logic style, and hence we generate complementary outputs ~c1 and ~s0 for cascading (as shown in Fig. 1)[8] in multi-tile designs.

1.3 Overview of WISP-0

WISP-0 is a stream processor with a five-stage pipelined streaming architecture using five nanotiles: Program Counter - PC, Read Only Memory - ROM, Decoder - DEC, Register File - RF and Arithmetic Logic Unit - ALU [14][23]. Adjacent nanotiles communicate using nanowires, with each nanotile being driven by surrounding microwires as shown in Fig. 2 WISP-0 supports five instructions: nop, mov, mvi, add and mult. Each instruction contains a 3-bit opcode and two 2-bit operands. The ALU was further partitioned into two stages to achieve a more balanced pipeline. In this thesis we use WISP-0 processor design mapped to NASIC fabric to perform evaluations.

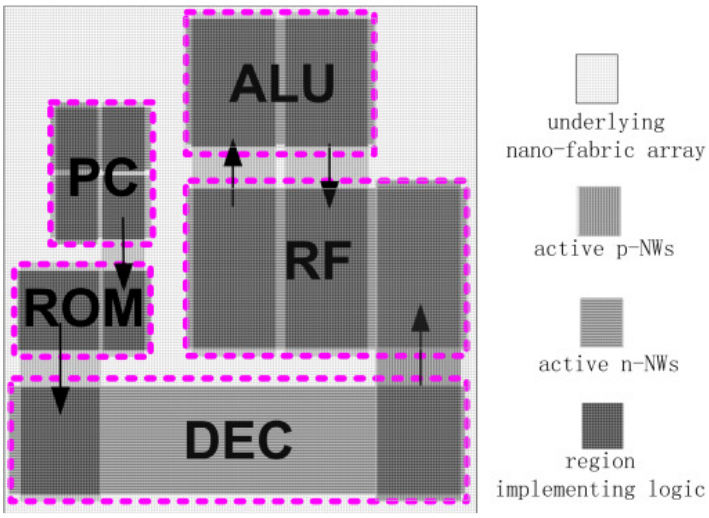

Figure 2.WISP-0 Floorplan [14]

CHAPTER 2

RELATED WORK

2.1 Introduction

Reliability and manufacturability are two major concerns in nanoscale regime. Although the manufacturing process is progressing, the defect levels in nanofabrics are still at least in a few percent ranges [24]. Such a high defect rate makes fault tolerance a critical aspect in nanoscale architecture. The fault tolerance techniques employed are highly related to fault types and distributions.

2.2 Fault tolerance in nanofabrics

NASICs [8][14][15][22][25], NanoPLA [26], CMOL [17][27], FPNI[9] are being demonstrated as promising alternatives to CMOS. The logic implementation style is different among these nanofabrics. NASICs use field-effect transistors (FETs) at nano-crossbar junctions to implement logic while diodes or molecular switches are being used by NanoPLA, CMOL and FPNI.

The fault tolerance methodologies adopted by these fabrics differ as well. The techniques proposed for providing fault-tolerance in the nano-PLAs can be broadly classified into two types: on-line repair [28] and fault masking [29]. It has been observed that the device missing effect (crosspoints may be with or without devices) is dominant in nano-PLAs [24][30][31]. [32] discusses a von Neumann's NAND multiplexing implementation in basic circuits and reconfigurable architectures mapped to the overall system. In [33] and [34], the authors have developed a tautology technique for providing fault tolerance for PLA architecture. The yield analysis of PLA devices has been performed by mathematical means [33][35] or using a PLA analyzer[36]. The PLA analyser is a tool that is able to operate both on PLAs which have been

mapped with redundant terms, or can add redundancy in the form of replicated wires. However, the performed yield calculation doesnot look at the manufacturing process to analyze the type of defects. Four types of faults are assumed in nanoPLA yield estimation: a) Bad ohmic contacts among nanowires and microwires, b) Faults in the decoder patterns, c) Disconnected crosspoints, and d) Broken nanowires. These yield estimation is carried out for a range of defect percentages assigned. However, no analysis of the manufacturing process is done in order to estimate the types and percentage of the defects.

CMOL employs a reconfiguration technique for providing fault tolerance. The switches in CMOL fabric play two roles: they provide diode-like behavior for logic circuit operation, and allow circuit mapping on CMOL fabric and its reconfiguration around defective nanodevices. [37] have demonstrated that the reconfiguration in CMOL fabric allows increasing the circuit yield above 99% at the fraction of bad nanodevices above 20%. The yield calculations are obtained by employing Monte Carlo simulations (so far only for the "stuck-on-open"-type defects which are expected to dominate in CMOL circuits).

FPNI models "stuck-open" as the most common defect expected in such crossbar fabric. This is modeled as a switch where a high-impedance junction that cannot be configured to a low-impedance state [9].The FPNI compiler developed maps logic circuits onto FPNI chips. The compiler performs placement, routing, timing analysis and power analysis. The compiler takes two files as inputs -a circuit file and -an FPNI chip description file and produces a mapping of that circuit onto the chip followed by the expected yield of the fabric for the given design.

While most of the above fabrics rely on reconfigurable devices, defect map extraction, and reconfiguration around defects, NASICs employs built-in fault tolerance techniques. Details of the built-in fault tolerance techniques in NASIC fabric are discussed in the next few sections.

2.3 Fault model assumed

In NASICs, built-in fault tolerance techniques have been provided for uniform and clustered defect models. Broken NWs, stuck-on and stuck-off are the defects which have been studied and analyzed in NASIC fabric. A stuck-off transistor is treated as broken NW. Stuck-off FETs are also less likely especially in depletion mode fabrics. Research suggests that we will be able to control the reliability of NWs fairly well so broken NWs or stuck-off FETs will be likely less frequent than stuck-on FETs [14]. In addition to permanent defects other error sources such as due to process variation and transient faults are also discussed [8][38]. In NASIC's defect rates of up to 15% have been considered for evaluation.

2.4 Built-in Fault-Tolerance in NASICs: Circuit-Level and Structural Redundancy

Redundant copies of NWs are added and redundant signals are created and logically merged in the logic planes with the regular signals. Horizontal NWs are predischarged to "0" and then evaluated. Vertical NWs are precharged to "1" and then evaluated.

A NASIC design is implemented in AND-OR (or equivalent) logic planes (Fig. 3). If a break on a horizontal NW in the AND plane (position A) causes the signal on the NW to be "0", as it is disconnected from Vdd. The faulty "0" signal can, however, be masked in the following logic OR

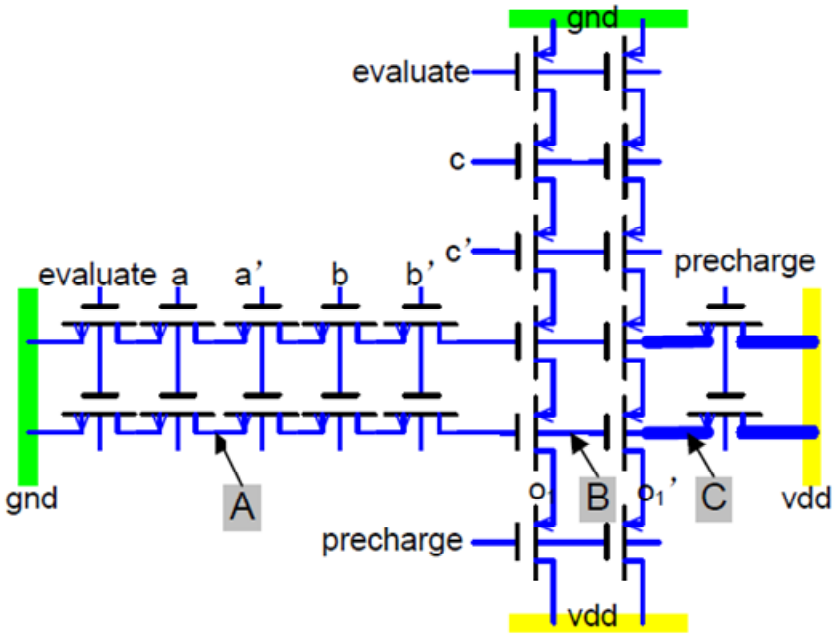

Figure 3. Simple 2-way structural redundancy [14]

plane if the corresponding redundant NW is not defective (position B). Similarly, a NW break at position C can be masked in the next stage. Similar masking strategies for interleaving of nanowires [8][14] have been successfully implemented for NASICs.

2.5 Voting at Nanoscale

Modular redundancy implementation uses majority voters. Conventional majority voters are not used in NASIC fault tolerance techniques; instead biased voters are used. Faulty 0's tend to be less common in high fan-in stages; since this requires many devices on a single nanowire to be simultaneously stuck-on (a single correctly switched-off device will prevent evaluation to '0'). Since performance of the design is dominated by the evaluation-to-'0' of high fan-in stages, implementation of voters biased to zero have performance benefits[14][15][38]. The FastTrack scheme is based on the following observation: i) some block inputs arrive sooner than others, ii) it is a property of the NASIC circuit that logic '0' faults are considerably less likely than logic '1' related faults[15][38]. Thus, the voters used in this scheme are biased toward zero. Here, a voter denoted by $V_0^{2/5}$ indicates that it is biased to '0' and requires only 2 of the 5 inputs to be '0' to

produce a result of ‘0’while 3 ‘1` inputs are still necessary to produce a result of’1`. This is in contrast to a majority voter where at least 3 out of the 5 inputs are required to be zero in order for the voter output to be zero. Other nano-computing fabrics may require different biasing schemes based on the underlying fault models. Leveraging these asymmetric delay paths (resulting from some inputs being faster than the other) combined with biased voting schemes results in a redundancy scheme with better performance but at the cost of a lower effective yield.

CHAPTER 3

YIELD MODELING

3.1 Introduction

Our goal in this thesis is to analyze the sources of defects from a manufacturing perspective and estimate the yield loss associated. Identifying the potential defects that may occur during each step of the bottom-up fabrication of nanoelectronic circuits is important since it would provide a better estimate of the defect rates allowing a more accurate yield analysis. A major objective of the yield estimation is to relate the occurrence of defects generated at each manufacturing step to the loss in yield that they cause, so that specific action can be taken to lower the number of defects and increase yield.

Design technology has traditionally aimed at the three parameters – area, timing and power as its main objectives. Even with these objectives being of paramount importance, increasing focus is being laid on manufacturability and yield. For sub-90nm technologies, yield is increasingly becoming an issue in all steps of design phase; from processing to sign-off. Yield must therefore become the fourth design parameter, to be optimized along with power, area and performance at different stages of the design flow. Reducing the yield loss mechanisms requires improvement of the manufacturing process. Hence yield analysis with a manufacturing perspective is the required approach.

3.2 Manufacturing Pathway

Integration of devices into a large scale functional system has been demonstrated in the nanoscale research. Chen et al. have successfully designed a ring oscillator using carbon nanotubes [39]. Lu et al. have realized a decoder circuit from NWs [2]. A complementary symmetry NW logic circuitry implementation has been demonstrated in [40] by manufacturing

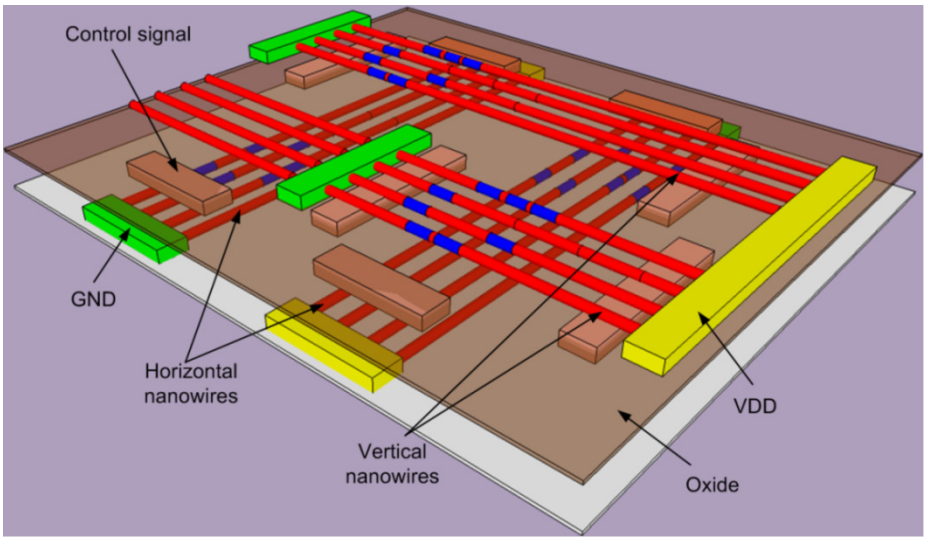

Figure 4. NASIC Fabric [16]

of XOR gates.While the above work concentrates on device characterization and prototyping; studies' focusing on scalable manufacturing of nanofabric are also being done. For example, Cerofolini *et al.* have described terascale integration and arrangement of Si-nanowires [18]. Narayanan *et al.* have proposed a manufacturing pathway using a combination of unconventional and photolithographic manufacturing steps and have described the associated challenges for nanoscale systems [16]. This implies that yield implications for emerging nanofabrics need to be carefully examined from a manufacturing perspective. The questions that need to be answered include: What kinds of defects are introduced in the given nanomanufacturing sequence? What is the yield loss associated with successive mask overlays? How do yield losses change for different overlay requirements? How sensitive is the overall yield to the choice of physical fabric design parameters (e.g., pitch/width of nanowires)? What is the impact of particulate defects on overall yield?

The manufacturing pathway proposed by Narayanan et.al focuses on realizing the NASIC fabric (see Fig. 4) incorporating all the contacts, interconnects and devices. Fig. 5 shows the manufacturing sequence. Horizontal NWs are grown and aligned on a substrate (Fig. 5.A);

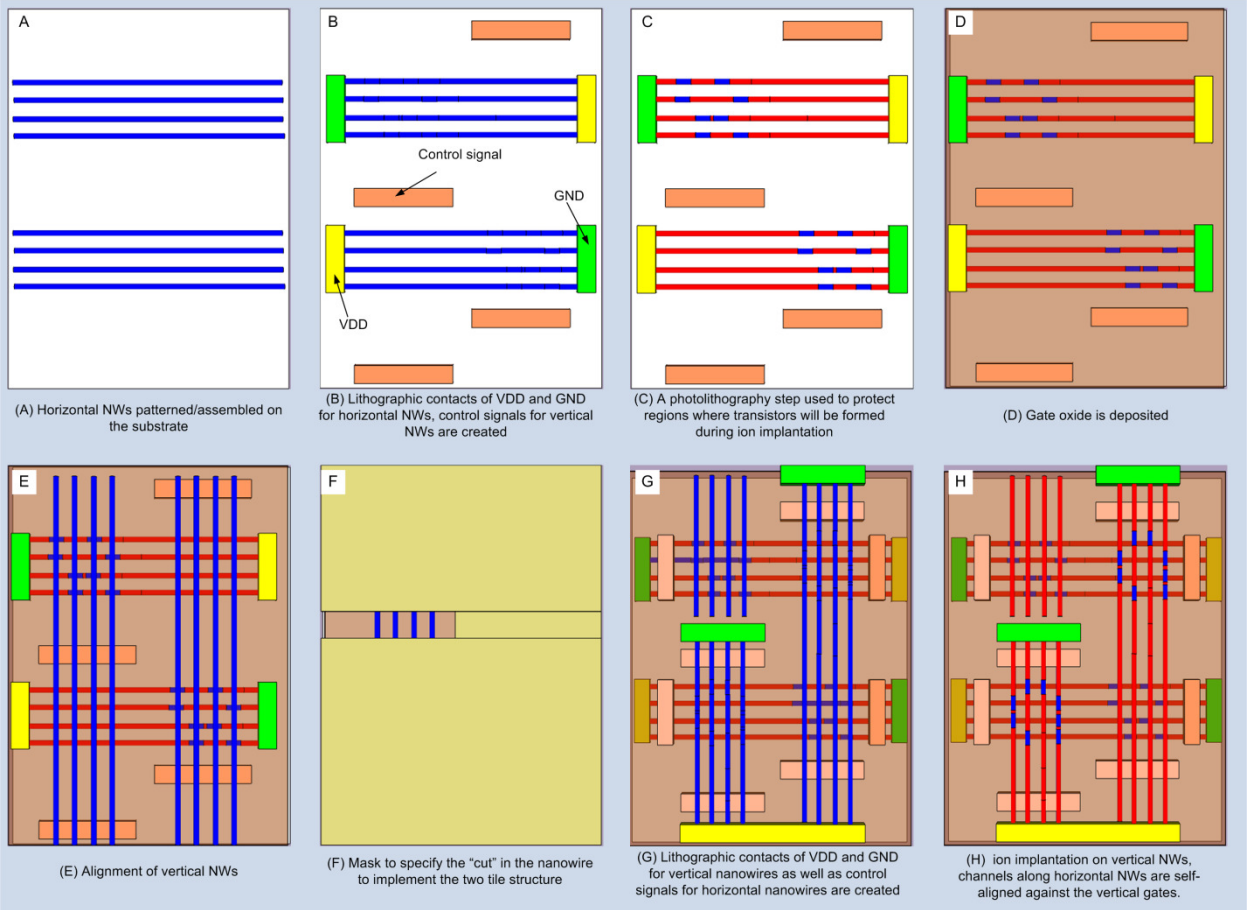

Figure 5. NASIC's manufacturing sequence using "two nanowire transfer"[16]

Lithographic contacts of VDD and GND for horizontal nanowires as well as control signals for vertical nanowires are then created (Fig. 5.B). A photolithography step is used to protect regions where transistors will be formed while creating high conductivity regions (using ion implantation) elsewhere (Fig. 5.C). Gate dielectric layer is then deposited (or oxide is grown) (Fig. 5.D) followed by alignment of vertical NWs (Fig. 5.E).The next mask is used to cut the nanowires using an etch-back process to implement the two-tile structure (Fig. 5.F)[7]. Lithographic contacts of VDD and GND for vertical nanowires as well as control signals for horizontal nanowires are created (Fig. 5.G). During ion implantation on vertical NWs (Fig. 5.H), channels along horizontal NWs are self-aligned against the vertical gates.

It should be noted that the total number of masks required to realize the fabric is much less than that for conventional CMOS design. The reasons for this are: a) NASIC circuits require very limited customization: only one type of FET [22] is used in the logic portions of the design and there is no requirement for arbitrary placement or sizing of devices; b) Devices and interconnects are achieved on the nanowire grid itself in a single functionalization step; interconnection of devices does not require a metal stack.

3.3 Analysis

A bottom-up fabrication of nanoelectronic circuits is expected to be subjected to various defects. Identifying the types of defects that may occur during each step of a manufacturing pathway is essential in any attempt to achieve reliable manufacturing.

It should be noted that defects can be introduced during a) alignment of masks, b) processing steps like nanowire transfer, and c) as impurities during manufacturing step. The above nano-manufacturing issues are hence going to be considered in the proposed yield analysis procedure. Each of the issues can be associated with certain specific step/steps of the NASIC manufacturing pathway described in Section 3.2.

1) Particles introduced during the manufacturing process

Although lithographic distortion is emerging as the dominant mode of failure, particulate defects still remain an important source of defects. Defect-related yield losses may be the result of the cleanroom environment and the lithography process. Dust particles in the cleanroom, mask defects left over from the mask fabrication process, imperfections in mask substrate are few known sources of random defects [21]. The random-defect limited yield loss will be analyzed and investigated for the NASIC fabric

2) Successive mask overlays

Lithographic masks are required at the following manufacturing steps: (a) Creation of VDD and GND contacts for horizontal nanowires along with control signals for vertical nanowires (Fig. 5.B), (b) Functionalization of horizontal nanowires (Fig. 5.C), (c) Mask used to specify the cut in the nanowires during etch-back process (Fig. 5.F), (d) Creation of VDD and GND contacts for vertical nanowires along with control signals for horizontal nanowires (Fig. 5.G), and (e) Functionalization of vertical nanowires (Fig. 5.H). All masks except the one used to cut nanowires using an etch-back process will be considered in our systematic yield analysis. The mask used for etch-back has high tolerance for overlay imprecision (i.e., it does not introduce any defects when misaligned in the range specified by ITRS [41]; lithographically defined regions to cut the nanowires are of dimensions larger than the minimum feature size and hence greater tolerance is achieved).

3) Nanowire transfer

The manufacturing steps of transferring horizontal nanowires and transferring vertical nanowires should be analyzed for yield loss due to nanowire alignment. The ideal technique to form aligned nanowire arrays is expected to guarantee a concurrent control over three key parameters: (i) the number of nanowires, (ii) the inter-nanowire pitch, and (iii) the nanowire diameter within the array, and (iv) the spacing between two arrays/sets of nanowires [16]. The state-of-the-art semiconductor nanowire array formation with alignment techniques needs to be analyzed to estimate the systematic yield loss resulting due to nanowire transfer.

The subsequent chapters in the thesis deal with each of the above mentioned yield loss mechanisms in detail.

CHAPTER 4

RANDOM DEFECT BASED YIELD

4.1 Introduction

Random defect limited yield modeling of chip requires the calculation of Probability of Failure (POF) or analysis of Critical Area (CA). Critical Area $A_i(x)$, for defects of type i and diameter x is defined as the area in which the center of a defect of type i and diameter x must fall in order to cause a circuit failure [21]. Historically, yield loss due to random defects has been a significant concern [19]. Consequently, random defect modeling and particle induced yield loss techniques were developed for CMOS technology [19][20][42]. Several studies have been done in analyzing the particulate defect limited yield in CMOS technology. In [43], Walker has proposed a VLASIC Monte Carlo yield simulator for efficient and detailed critical area computation. Carl Zhou et al. have successfully illustrated the methodology of using Critical Area Analysis (CAA) in conjunction with in-line defect data to predict the random defect yield [44]. It should be noted that the failure probability depends on a) the defect size distribution, b) the layout/design feature density, and c) failure mode such as short or open.

Methodologies have been developed to evaluate the critical area [21]:

1. Monte Carlo Simulation: Large numbers of defects with their radii distributed according to the defect size distribution are sampled; it is then checked whether such a defect causes short or open. Conducting particles are expected to cause a short and non-conducting particles are expected to cause an open (Fig. 6).
2. Geometric Methods: The methodology involves computing the area of critical region for several different values of defect sizes independently. A weighted approach is later applied to approximate the total critical area.

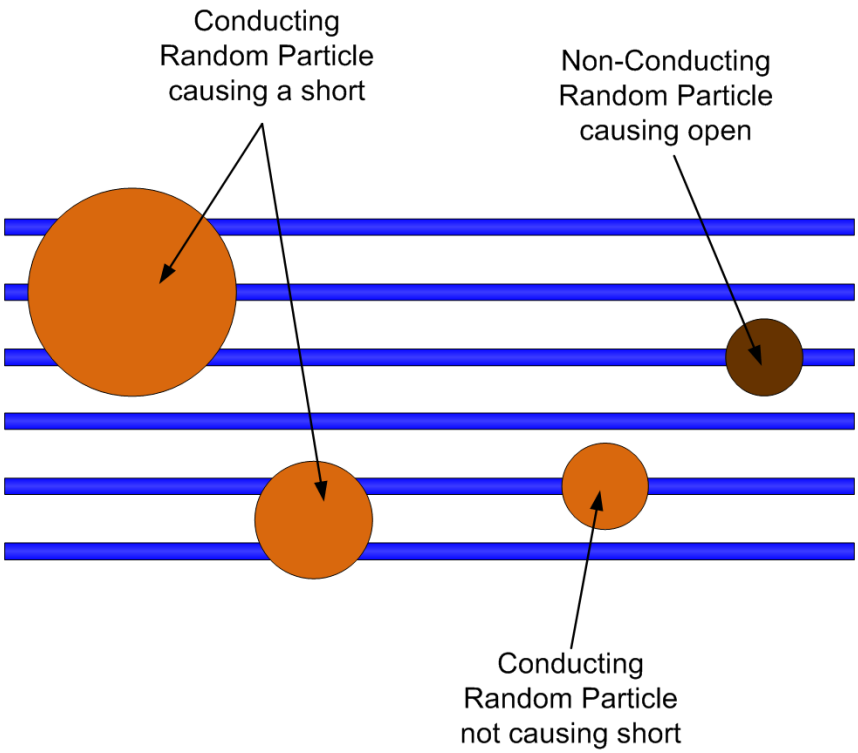

Figure 6. Particulate defects

With the NASIC being a uniform grid-based 2D nanofabric, it is intuitive to envision a high POF for shorts and opens. With the shrinking sizes of the nanowires used in the NASIC fabric design, smaller defects are expected to become killer defects. But because die size also shrinks for the same design, the yield is expected to almost remain constant (with decreasing nanowire dimension). A particulate defect based yield analysis is however required to estimate the overall die yield.

4.2 Methodology Followed

In the procedure employed, we perform critical area analysis by calculating the *Probability of Failure* (POF). The various tiles in the WISP-0 processor were analyzed for potential defects using the Monte Carlo approach. Simulations were performed for random defect sizes starting with

a minimum size of 10nm [41] up to 210nm. The minimum particle size was chosen as 10nm as projected by ITRS [41].

The tiles were analyzed for a possible failure either in the form of bridging faults or open faults at a number (5000 points per tile) of uniformly distributed random location. The POF is estimated using the equation given below [45]:

$$POF = \int_{x_{min}}^{\infty} POF(x) \times p(x) \qquad (1)$$

where

x is the defect size starting from a minimum value of x_{min}

POF(x) is the Probability of failure for a defect size x. The pseudo code to generate POF(x) appears below

The probability of defect size *p(x)* for a given defect size x is given by [45]:

$$p(x) = \begin{cases} {}^{x}/_{x_0^2} \ for \ 0 \leq x \leq x_0 \\ {}^{x_0^2}/_{x^3} \ for \ x_0 \leq x \leq \infty \end{cases} \qquad (2)$$

where

x_0 , the point of discontinuity is a function of the mean of the defect size.

The Critical Area of each tile is obtained by the product of POF and the tile area.

$$A_c = POF \times A_{tile} \qquad (3)$$

From the critical area, the die yield can be estimated using the either the Poisson model [46]or the cluster model [21][47].

Pseudo code for estimation of POF for short for the nano-tiles

1. **initialize fabric parameters pitch, width for the NASIC fabric**

2. **input the nano-tile design**

3. **generate particle size Pj/ Pj ϵ Range projected by ITRS**

4. **initialize** *Number_Of_locations* = N

5. **initialize** $F_j = 0$, $POF_j = 0$

6. **foreach** particle size Pj

7. **do until** (*location_count* = N)

8. **generate** location L_k (x_k, y_k)

9. Create Simulation Window SW_k around L_k

10. **forall** nanowires in SW_k

11. Check for short in presence of particle

12. **if** short

13. Add one to F_j

14. **enddo**

15. **calculate** $POF_j = F_j / N$

A similar analysis was carried out to evaluate the POF for open faults in NASICs

4.3 Simulation Results

The Monte Carlo simulations were run for 5000 points per tile to obtain the POF for shorts. The analysis was also performed for various NASIC fabric pitch and width.

Sensitivity to Width: Fig. 7 represents the POF (for shorts) for nanowire of width 5nm at two different pitches. It can be observed that at a given width with increase in pitch there is a slight decrease of POF. This is intuitive due to the increasing space between two nanowires with increasing pitch. However, it should be noted that the POF value is extremely high due to high

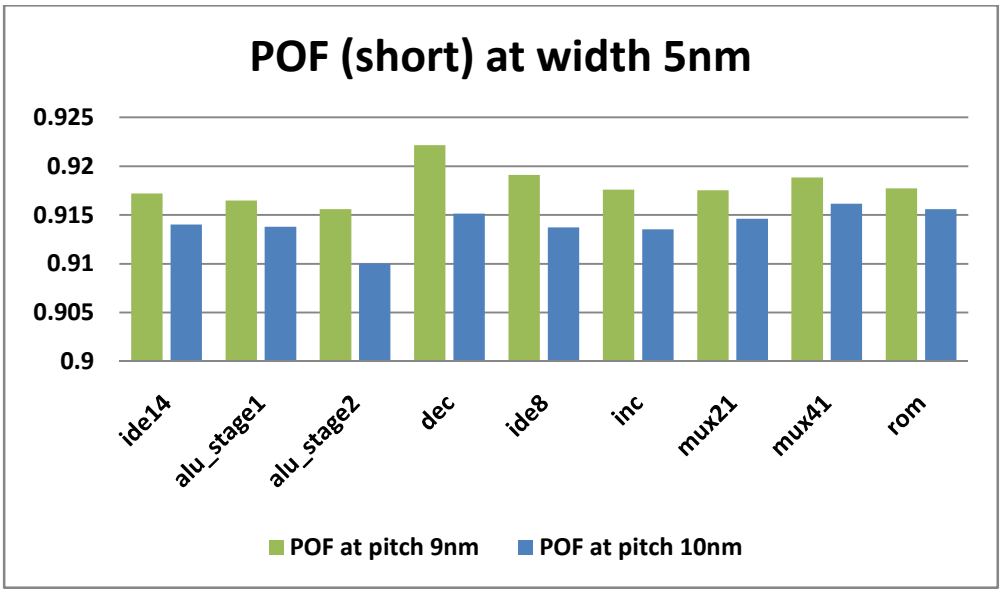

Figure 7. POF for shorts at 5nm width

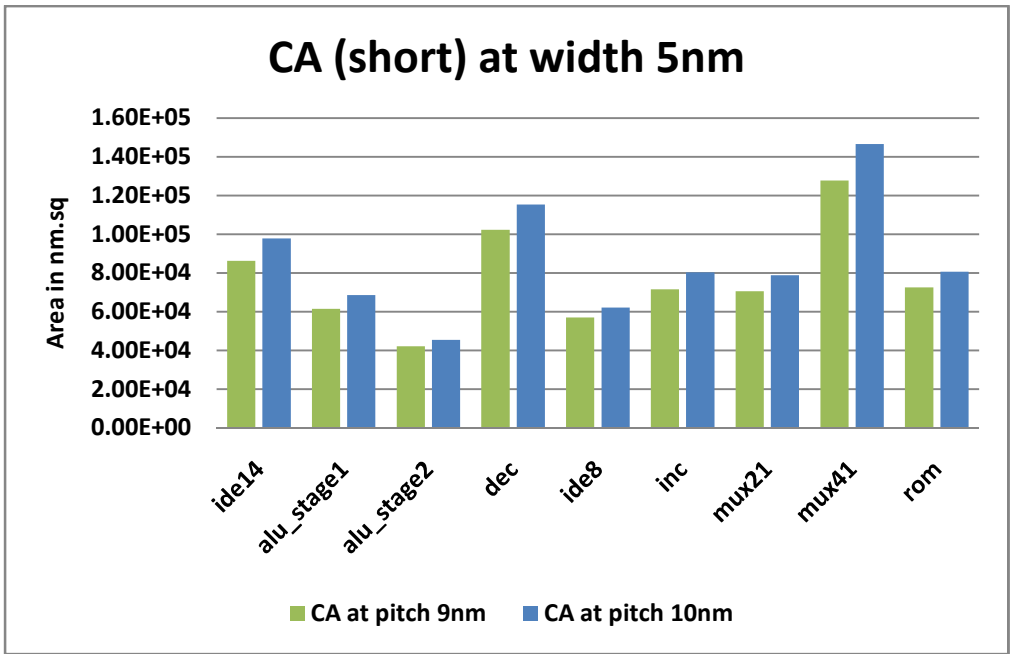

Figure 8. CA for short at 5nm width

density of the NASIC fabric (approximately 30X denser than conventional CMOS at 16nm technology node [25]). The critical areas for various designs were obtained by using the equation (3) and area of the various WISP-0 tiles for varying pitch. The critical area plot at constant width

of 5nm is shown in Fig. 8. It can be seen that the increasing tile area due to increase in pitch completely removes the advantage of decrease in POF.

Sensitivity to Pitch: Fig. 9 shows the POF (shorts) at a constant pitch of 10nm with varying width. It can be seen that the POF increases with increase in width, for a given pitch. This is due to the decreased spacing between the two nanowires at constant pitch. Fig. 10 depicts the CA (shorts) for the same scenario. It can be observed that the increase in POF is negligible so that the CA almost remains the same at constant nanowire pitch (the difference in critical area at constant pitch and changing width is of 10^{-3}nm.sq).

Poisson yield model: The yield plot for bridging faults (shorts) can be obtained from the critical area by using the Poisson yield model [21][46] . The defect density is 0.01defects/cm.sq as projected by ITRS [41]. It can be observed that a yield approximately equal to unity is obtained for the projected defect density for critical area up to 1000um.sq. Plot of yield as a function of

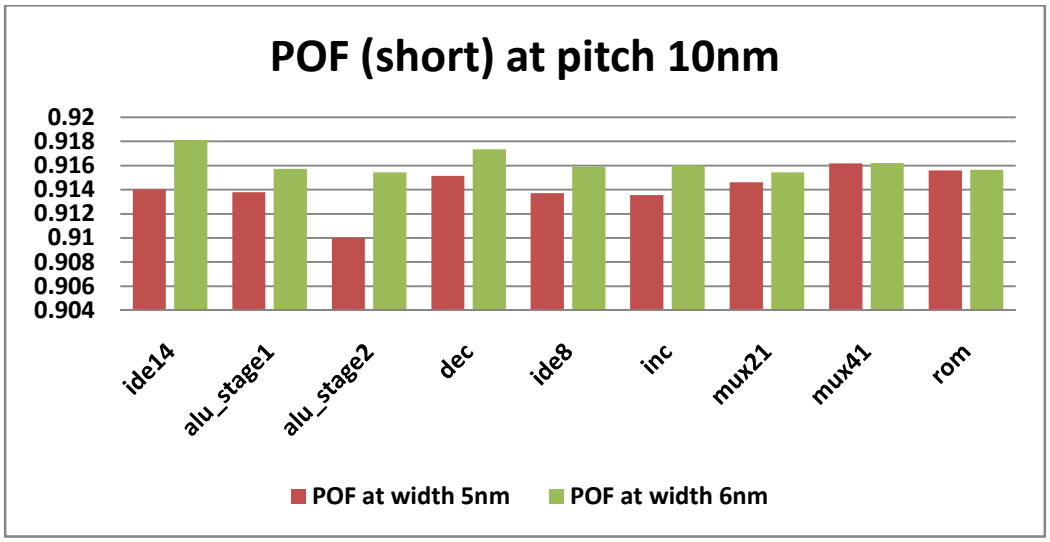

Figure 9. POF for shorts at 10nm pitch

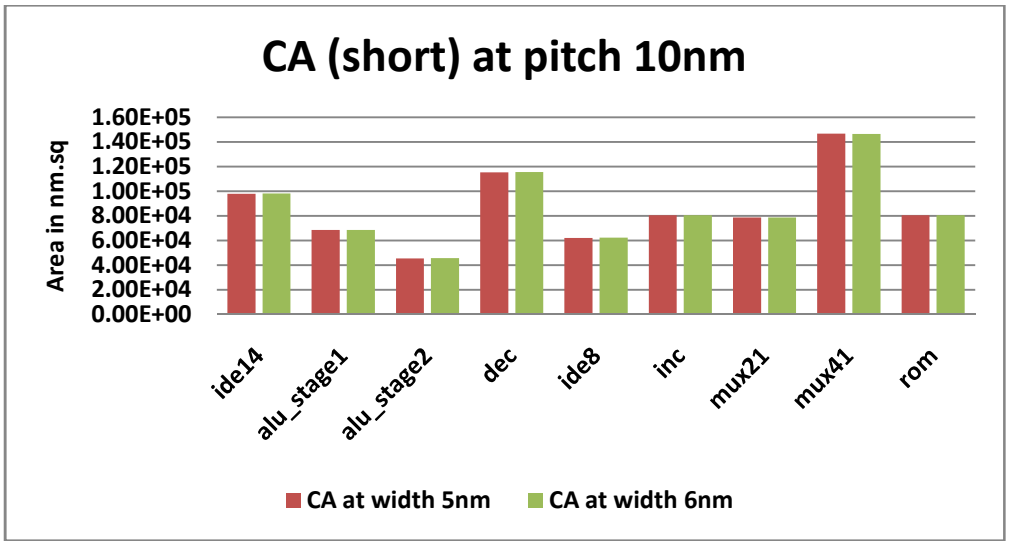

Figure 10. CA for shorts at 10nm pitch

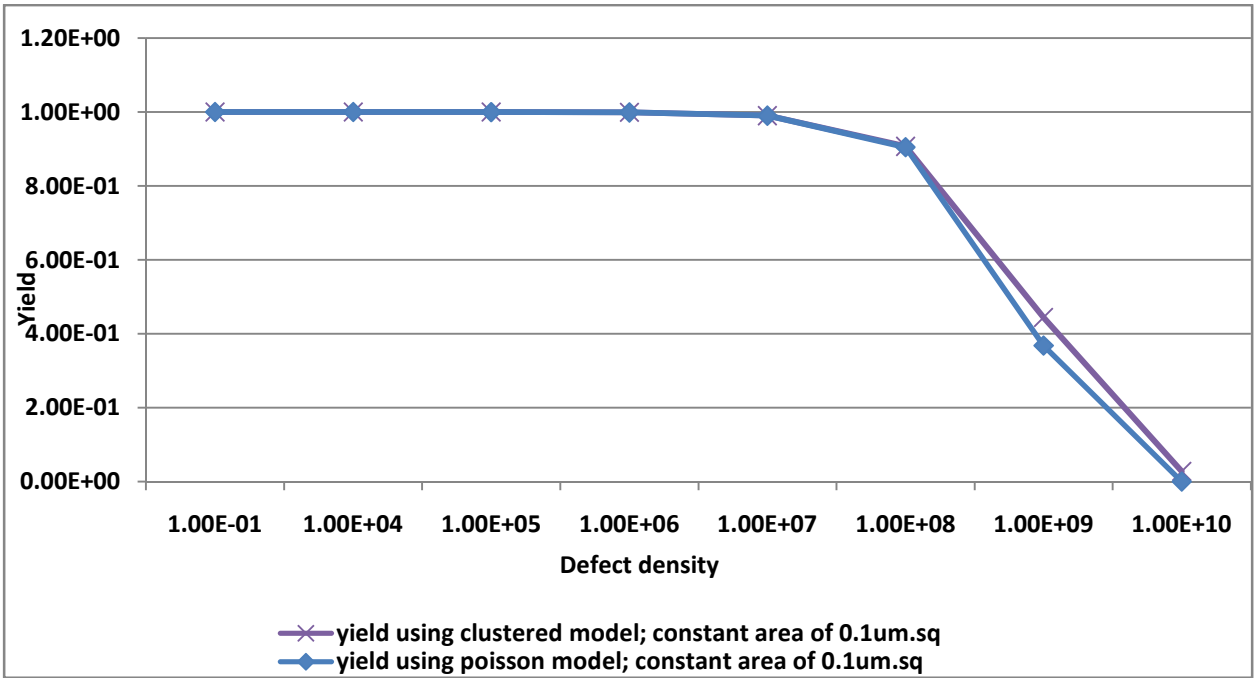

Figure 11. Variation of random defect limited yield with defect density

critical area and defect density is shown in Fig. 11. A defect density of 10^7 defects/cm^2 would result in considerable yield loss for NASIC designs with area comparable to WISP-0 processor (as per the projected defect rate by ITRS, an area greater than 10cm.sq would result in considerable yield loss). It can also be projected that a defect density of 10000 defects/cm^{2}for a design mapped

to 10000um.sq area of NASIC fabric would result in 64% random-defect limited yield loss. For the projected density of 0.01/cm.sq 10^{10}sq.um area would result in a similar yield of 64%. This would imply that a design as large as 10,000 million wisp-0 designs would result in 64% yield at current defect density projections.

A similar analysis was carried out for open faults and similar trend was observed.

Clustered yield model: The yield plot for bridging faults (shorts) can be obtained from the critical area by using the clustered yield model [21][47]. The random defect limited yield using the clustered model is given by the equation below:

$$\text{Yield} = \left({}^{1}\Big/_{1 + \left(\frac{\text{AcDo}}{\alpha}\right)} \right)^{\alpha} \quad (4)$$

The cluster parameter α is projected to have a value of 2 by ITRS [41]. Fig.11 shows the variation of random defect limited yield for the clustered model. Variation of yield can be seen (when compared to Poisson model) only for defect densities greater than 10^8 defects/cm.sq ; for a critical area of 0.01 sq.um. Hence a difference in random defect limited yield between the Poisson model and clustered model can only be observed for large defect densities/ high critical area. For designs with bigger area (10^{10} times the area of WISP-0), yield improvement of up to 10% is seen with clustered model.

4.4 Conclusion

An analysis of random defect limited yield was carried out for a WISP-0 design mapped to NASIC fabric. The Monte Carlo approach was adopted to obtain POF, followed by Critical Area calculation. The particulate limited yield loss being considerably small, the fraction of yield loss

which is inevitable is noted. The observations and results also stress the emerging need for affordable, accurate real time sensors for non-particulate contamination which are leading to yield loss. Pre-contact clean, reticle exposures are cited as processes that first need this capability [41].With systematic components of yield frequently constraining yield in early stages of manufacturing, the next chapter analyzes the systematic yield loss.

CHAPTER 5

SYSTEMATIC YIELD LOSS IN NANOSCALE FABRICS

5.1 Introduction

This section deals with the systematic yield loss associated with the nanoscale manufacturing flow of NASIC fabric. Yield evaluation has been carried out using a scalable manufacturing pathway that focuses on realizing the NASIC fabric with incorporated contacts, interconnects and devices [16], and using the overlay misalignment tolerance projected by ITRS [41]. Yield predictions obtained using the prescribed procedure would be more realistic and help us gain a perspective on the adopted manufacturing flow through: (a) yield loss associated with successive mask overlays, (b) yield implications for different overlay requirements, (c) yield implications for different feature sizes, and (d) yield implications due to nanowire transfer steps.

5.1.1 Mask Offset and Overlay

Mask registration/mask offset may be defined as the difference $(\Delta x, \Delta y)$ between the actual position of a feature on a substrate and its intended position. Mask overlay error is defined as the displacement error of an exposed photo image (feature) relative to a previously exposed image (feature). It can hence be expressed as $(\Delta x_1 - \Delta x_2, \Delta y_1 - \Delta y_2)$ for any two successive masks in the manufacturing sequence. In order to achieve the required functionality, the lithographic masks in the fabrication must overlay each other to within acceptable tolerance. Mask overlay has been a key design issue even in CMOS. Critical layer mask pairs such as active-to-gate, gate-to-contact, and contact-to-metal have been traditionally analyzed for overlay related errors [48]. Active-to-gate mis-registration can result in gate leakage or reduced static noise margin. Gate-to-contact mis-registration can result in shorts and functional failures. Contact-to-metal mis-registration quite

often results in resistive or open interconnect [48]. As the number of metal layers increases in CMOS, the probability of a metal-to-via overlay failure also increases.

To build a nanofabric in a scalable fashion, lithography needs to be used for functionalization. This implies that mask overlay and registration requirements as well as the systematic yield implications for emerging nanofabrics need to be carefully examined. The questions that should be answered include: What kinds of defects are introduced due to mask overlays in the considered nanomanufacturing sequence? What is the yield loss associated with successive mask overlays? How do yield losses change for different overlay requirements? How sensitive is the overall yield to the choice of physical fabric design parameters (e.g., pitch/width of nanowires)? We have carried out a detailed analysis of systematic sources of defects for the manufacturing pathway proposed in [16]. Lithographic masks used in the NASIC manufacturing pathway are considered for overlay analysis (See section. 3.3 for more details).

5.1.1.1 Implications of varying feature size on systematic yield

Another key design/process parameter that could be optimized for improving yield is the feature size. In a NASIC manufacturing pathway, the manufacturing resolution required is determined by the functionalization step, where certain regions on the grid (where FET channels need to be defined) are masked out and surrounding regions are ion implanted to form high conductivity source/drain regions and local interconnect. Smaller feature size might imply shorted channels, whereas larger features might cause undesirable stuck-opens at neighboring crosspoints. Therefore, in addition to the pitch/width parameters, the minimum feature size of the mask defined on the grid needs to be analyzed in depth.

5.1.2 Nanowire Alignment

Several techniques have been proposed for nanowire alignment. *In-situ*, *ex-situ* and unconventional patterning approaches are being studied for formation of aligned nanowire arrays. Superlattice Nanowire Pattern Transfer (SNAP) has been demonstrated for silicon nanowire arrays at 13nm pitch and 8nm width [40],[49]. *Ex-situ* processes employ techniques such as the Langmuir-Blodgett technique [50]-[51], fluidic-guided method [52], electric field guided assembly [53], or organic self-assembly [54]-[55], to align the semiconductor nanowires that are synthesized elsewhere (through techniques such as Vapor-Liquid-Solid (VLS) growth) [50]-[55] to produce almost parallel nanowires array.

The state-of-the-art semiconductor nanowire array formation with alignment techniques need to be analyzed to estimate the yield loss resulting due to nanowire transfer. With respect to nanowire alignment issues, horizontal and vertical nanowire transfer steps needs to be analyzed. Nanowire array will be patterned for horizontal arrays. Vertical nanowire transfer is assumed to be *ex-situ* as prescribed in the manufacturing flow [16]. In the vertical nanowire case, the precision of nanowire about its nominal position needs to be studied and analyzed (patterned nanowires with 6nm half pitch have been demonstrated in [49] which implies tight pitch horizontal nanowire patterns). Literature survey was carried out to obtain the distribution (and hence variation) of the nanowire about its nominal position for the alignment scheme employed. Following the literature survey the vertical nanowire transfer has been modeled.

5.2 Analysis

It should be noted that nanowire assembly is carried out prior to any lithographic step without any overlay requirement. In the case of techniques like NIL [56], alignment markers for registering against photolithographic steps are created in conjunction with the logic nanowire array using a single mold as shown in Fig. 12. For techniques like SNAP, patterned nanowires (of a different dimension than that of the logic nanowires) can be used as alignment markers (Fig. 13), since arbitrary alignment patterns may be difficult. The alignment nanowires would form Moiré patterns/fringes [57]-[58] for alignment. The creation of markers for registration is accomplished in the same step using the same mold/superlattice as the logic nanowires and is therefore self-aligned.

The underlying arrangement of the uniform and regular nanowires allows the first lithographic mask to be "offset" horizontally with tolerance on the grid and still achieve correct functionality. The effect of mask offset (registration or alignment of the first lithographic mask) can be envisioned as shown in Fig. 14. A uniform parallel array of nanowires is first patterned (or assembled). The accompanying alignment marks (i.e., AM#1 in Fig. 14.a) are also simultaneously created for registration purposes. During the alignment of the first mask (e.g., to create metal contacts, Fig. 5.B), AM#1 will be used as the alignment target (Fig. 14.b). An excessive offset in the y-direction can potentially result in defective chips (Fig. 14.c), with some nanowires not being contacted to power rails. New alignment markers should also be created for subsequent steps. As shown in Fig. 14.b,c new alignment patterns (AM#2), are defined on the photoresist in addition to contact patterns for the current step. After the development of the photoresist, the intended process is carried out. For example, metal deposition to create contacts

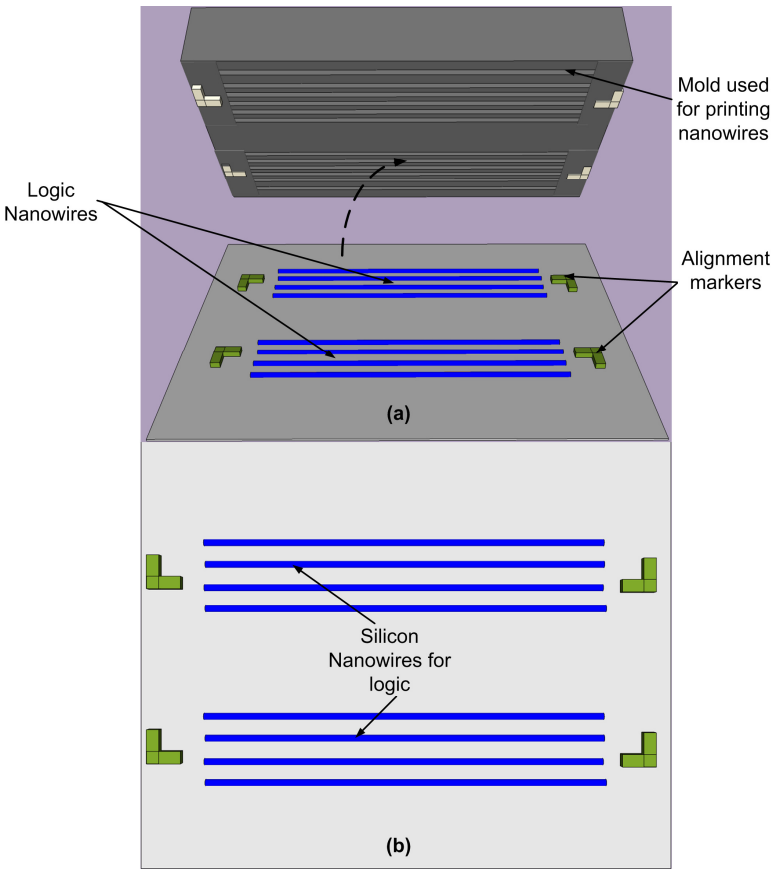

Figure 12. NIL technique showing both the nanowires and the alignment markers in the same mold and control may be carried out. Metal markers (AM#2) would then be created on the substrate itself and used as alignment targets for the subsequent step. After creating the contacts, functionalization is done to define the positions of devices and interconnects on the horizontal nanowire array (Fig. 5.C). Lithographically defined regions with a minimum size of (pitch × pitch) squares are blocked out, and ion-implantation/metallization is done elsewhere.

Fig. 15 shows transistor defects that arise from misalignment of this mask. Fig. 15.a shows the correct alignment scenario. Pitch and width parameters are labeled as ‘p’ and ‘w’. A vertical misalignment of up to (p – w)/2 may be tolerated without any defects in this step (Fig. 15.b). A misalignment greater than this value would result in shorted channels across the horizontal nanowire array, leading to yield loss (Fig. 15.c).

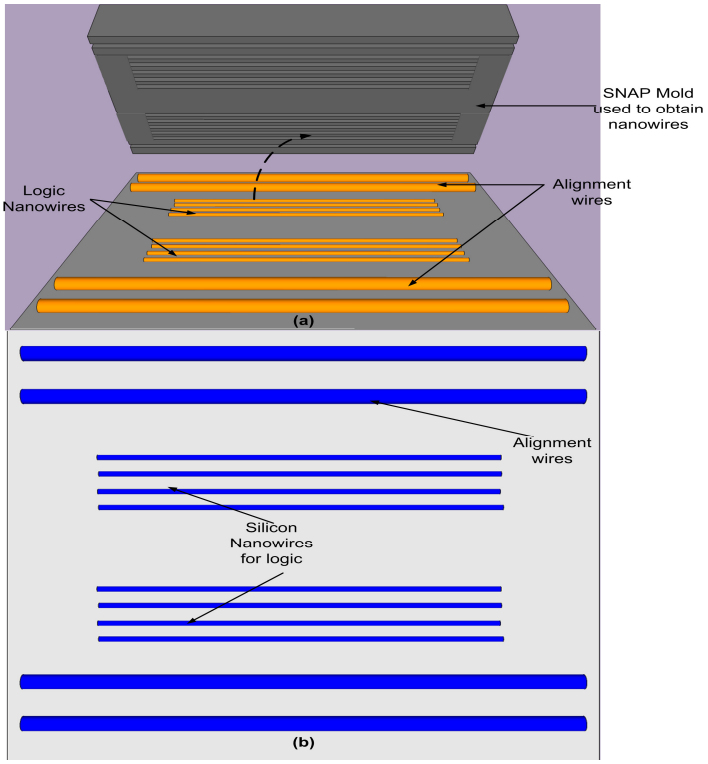

Figure 13. SNAP technique, showing patterned nanowires (different dimension than logic nanowires) which can be used as alignment markers for moiré patterning

While at this point the chip is already defective, for completeness, a case where both incorrectly shorted and incorrectly functionalized devices are created, is shown (see Fig. 15.d) when the misalignment exceeds (p+w)/2. This cannot be envisioned as shifting the design 'up' by a nanowire pitch, since the contacts are already defined in a previous step. It must be noted that additional markers will also be created in this step similar to Fig. 14; however, these have not been shown for clarity.

Horizontal nanowire functionalization step is followed by the vertical nanowire transfer step. Controllable number of nanowires should however be assembled in predefined locations, and orientations to achieve scalable systems with expected behavior. In this thesis, we evaluate the

systematic yield loss due to the vertical nanowire transfer step using the Stamped transfer process. K.S. Shin et.al [60] have demonstrated the Stamped transfer process for both VLS and SOI etched nanowires. The implementation of all stamping transfer steps of pre-patterned nanowire arrays is done with a mask aligner. Poly DiMethylSiloxane (PDMS) polymer is used for pickup and stamping process.

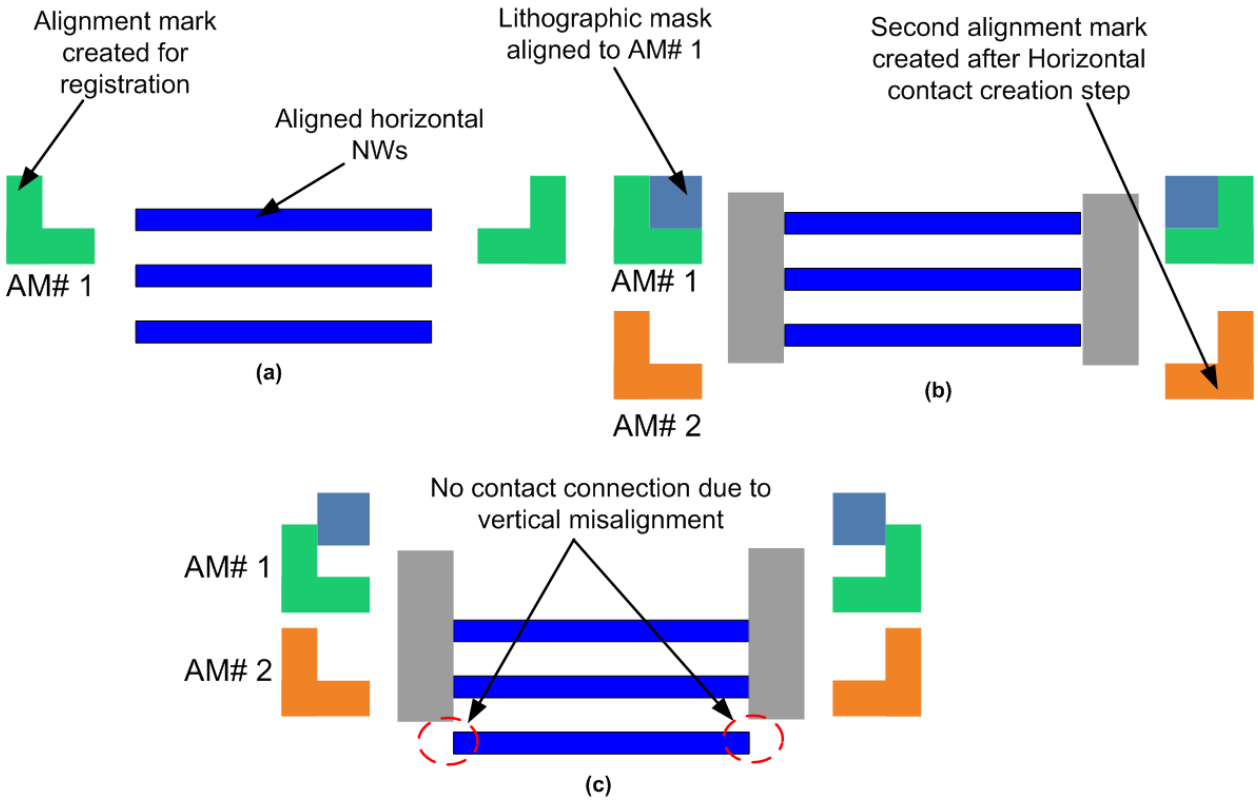

Figure 14. Depiction of mask registration during "horizontal contact creation" step

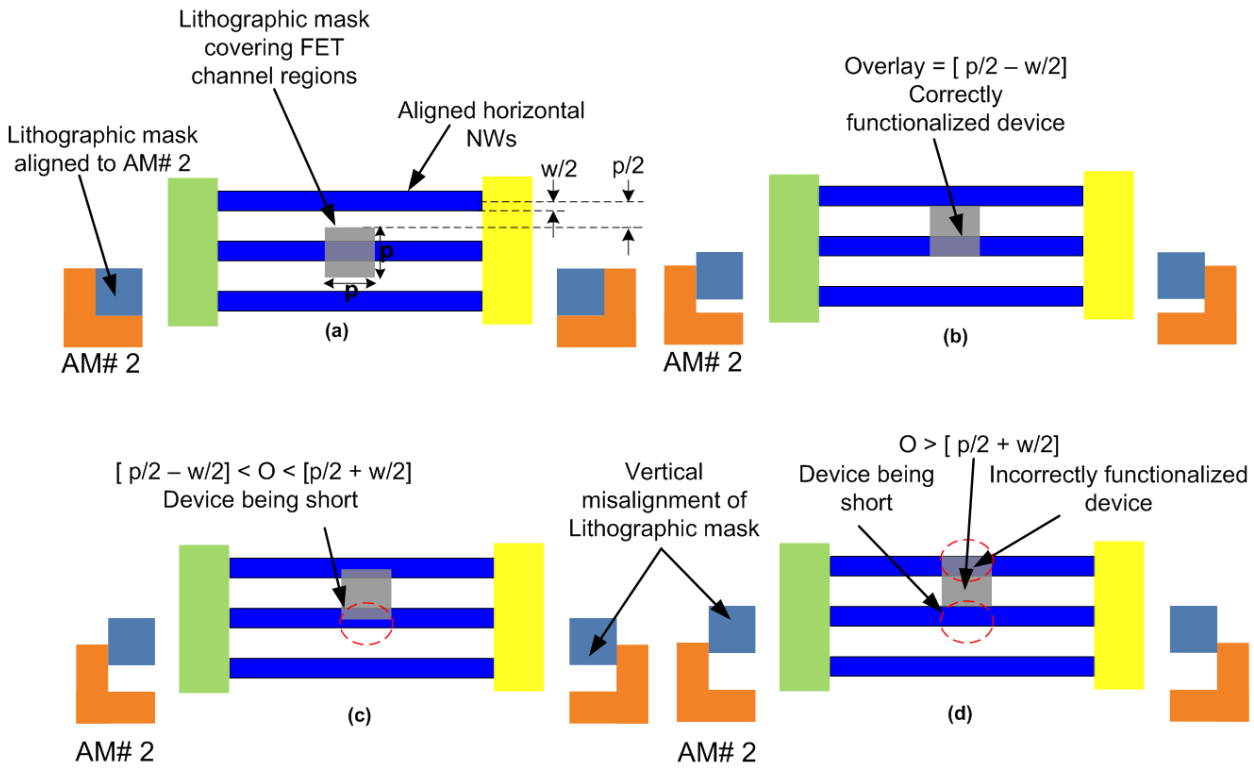

Figure 15. Depiction of the mask overlay effect during the "Horizontal Functionalization" step

5.3 Modeling Approach

The following section discusses the modeling strategy adopted.

5.3.1 Lithographic Mask – Overlay Modeling

The lithographic mask set utilized in the nanomanufacturing flow was modeled for mask overlay related yield losses. The procedure adopted for the same is discussed further.

5.3.1.1 Modeling of Mask Overlay

The effect of mask overlay misalignment for successive masks in the NASIC manufacturing sequence was studied through simulation. The overlay misalignment between successive masks

was modeled as a Gaussian random variable. As discussed in the previous section, all possible defect scenarios for a given manufacturing step and a sampled value of overlay misalignment were modeled using a custom simulator.

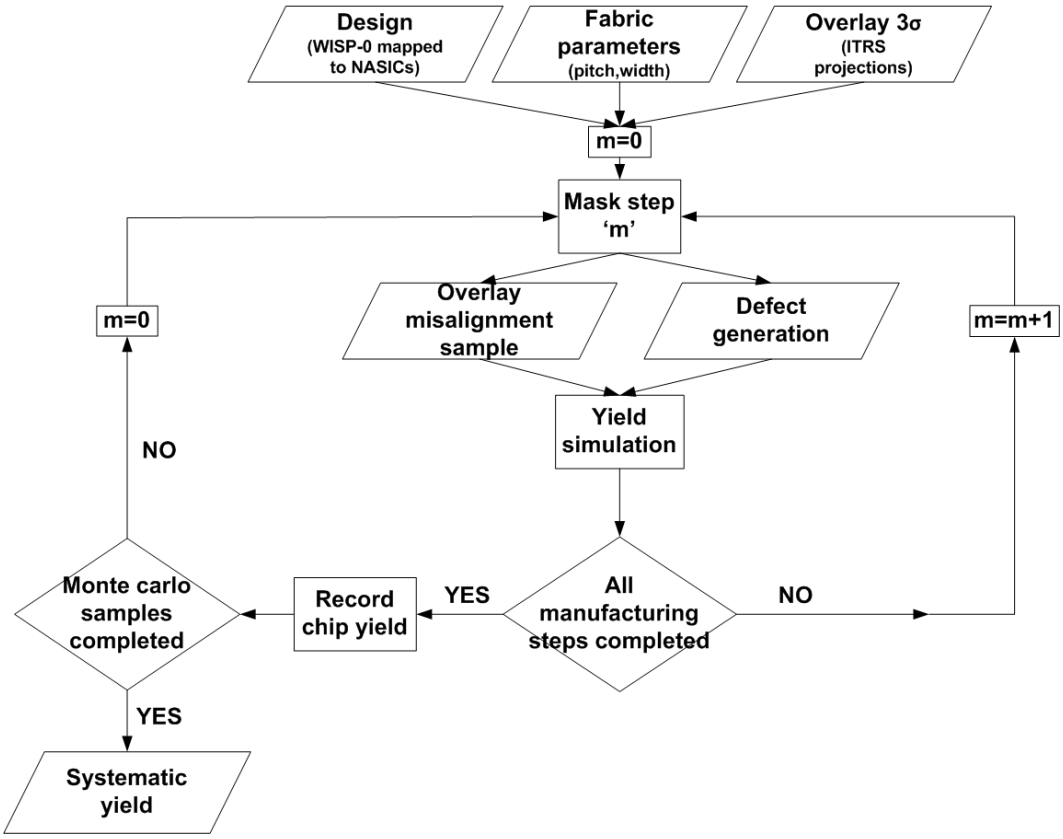

Figure 16. Procedure for yield estimation to predict the systematic yield loss due to mask overlay

The procedure used for yield estimation is shown in Fig. 16. Inputs to the simulation include fabric parameters such as width/pitch, the given design and the overlay standard deviation. For every manufacturing step, an overlay misalignment value with respect to the previous marker is sampled. This is an input to the simulator with all possible defect scenarios; the simulator determines whether the chip is either defective or defect-free (for a chip without redundancy, these are the two outcomes of systematic effects). After all mask steps are completed, the chip is recorded to either pass or fail. After a specified number of Monte Carlo simulations are complete

(in this case 5000- as a sample set larger than 5000 does not add any significant improvement to the accuracy of the result), the overall yield is calculated. Mask overlay misalignment for each lithographic step with respect to its previous step was hence modeled as a Gaussian random variable. If, for a given step, the sampled value of the misalignment exceeds tolerance limits, the chip would be systematically defective. Monte Carlo simulations will be carried out, with N different Gaussian random variables ($M_1, M_2, \ldots, M_N$) sampled independently in each run, where N is the total number of lithographic masks in the manufacturing process, and each M_i ($1 \leq i \leq N$) is the overlay misalignment for the given mask with respect to the previous one. From the Monte Carlo simulations, the percentage of yielding chips can be estimated.

This procedure allows analysis of systematic yield implications for nanofabrics. It integrates physical fabric considerations (including geometric parameters such as pitch and width), manufacturing sequences and associated defect scenarios to estimate the yield. This is in contrast to prior approaches that used generic defect models that typically assume constant defect rates (or a range of constant defect rates) without considering the manufacturing pathway and the potential sources of defects. While the focus of this thesis is the estimation of the mask overlay-limited yield for different fabric assumptions, this procedure can be easily extended to include 'processing-related' defects, like lateral diffusion during ion implantation leading to a shorted device, despite a correctly aligned mask.

This enables addressing key overlay and registration requirements. For example, it is possible to estimate the overlay limited yield for a range of overlay projections. It is also possible to address sensitivity of the overlay-limited yield to key fabric parameters such as the width and pitch of nanowires.

5.3.1.2 Modeling of mask feature size

Different values of the mask feature sizes will be examined. As shown in Fig. 17.a and b, the mask to print the smallest feature size could be between dimensions of ***a***=(pitch X pitch) and ***b***=[(2p-w)X (2p-w)], where *w* is the width and *p* is the pitch of nanowire. From Fig. 17, we can intuitively say that any size less than ***a*** has less tolerance to misalignment in the y-direction (leading to short). Similarly, any size above ***b*** has zero tolerance to misalignment in the x-direction (leading to opens) unclear. Since multiple lithographic masks would be used for creation of contacts and for functionalization of nanowires in horizontal and vertical directions, detailed simulations are necessary to estimate an optimal mask size for a fixed value of pitch and width. The simulation procedure previously proposed was modified to incorporate the mask feature size parameter and its implications for the various defect scenarios in each process step. Overlay misalignment was modeled as a Gaussian random variable as described previously and yield estimation across a large number of Monte Carlo simulations was carried out.

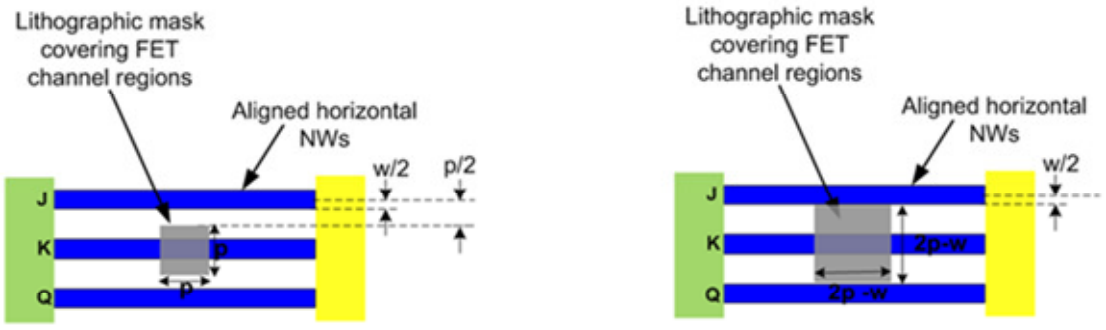

Figure 17. Mask feature size of dimension (a) (pitch) X (pitch) (b) (2p - w) X (2p - w)

5.3.2 Modeling of Nanowire Transfer

The PDMS stamping process has been shown to have a positional misalignment of 3σ = 100nm. This misalignment is measured as a distance between the two sets of nanowires upon transfer. Since, a single transfer step would consist of multiple sets of nanowires; the effect of nanowire misalignment is alleviated.

5.4 Experiments and Results

Year of Prod	mask overlay(nm)	MPU gate in resist (nm)
2009	10.3	47
2010	9	41
2011	8	35
2012	7.1	31
2013	6.4	28
2014	5.7	25
2015	5.1	22
2016	4.5	20
2017	4	18
2018	3.6	16
2019	3.2	14
2020	2.8	12
2021	2.5	11
2022	2.3	10
2023	2	9
2024	1.8	8

Figure 18. Overlay values as projected by ITRS

5.4.1 Mask Overlay and Registration

Simulations were performed to check the impact of mask overlay and offset on the nano-manufacturing flow prescribed for NASIC fabric. The WISP-0 nanoscale processor design

(mapped to the NASIC fabric), NASIC fabric assumptions, and overlay values were input to the simulator. The yield implications were studied for the various overlay values as shown in Fig. 18. Manufacturing solutions are known and are being optimized for the green (top) region; manufacturing solutions are known for the yellow (middle) region; and manufacturing solutions are as yet unknown for the red (bottom) region [41]. As mentioned in Section III, defect scenarios and consequently systematic yield loss are strongly dependent on the pitch and width parameters of the NASIC fabric.

5.4.1.1 Sensitivity to pitch

The impact of the nanowire pitch on the systematic yield loss due to mask overlay imprecision was evaluated. An xnwFET with a larger NW pitch is significantly easier to manufacture due to the increased minimum feature size on resist and also the increased spacing between adjacent nanowires. It is also expected to have better overlay imprecision tolerance. However, as expected, a larger NW pitch will result in a lower overall density, so it is important to understand its impact at the system level. WISP-0 consumes 0.839sq.um, 0.977sq.um, 1.125sq.um, 2.2394sq.um when mapped to 8nm, 9nm, 10nm and 16nm pitch NW, respectively. Fig. 19 shows the value of the systematic yield at various overlay values for a nanowire width of 5nm and varying pitch. At an overlay of 5.7nm, 80.6% yield was observed at 9nm pitch and 63.6% yield was observed for 8nm pitch. At a cost of 16.5% area increase, the yield can be increased by 42%. This implies different design choices; for example, for a design with a larger pitch it may be feasible to give up some yield for better devices.

We use the metric “Effective Yield” which takes into account the tradeoff between yield and area overhead and represents the number of functional chips obtained from a given area. Effective

yield is defined as (Overall Yield)*(Area of design with smaller pitch/Area of design with increased pitch). Fig. 20 shows the effective yield for 5nm width nanowires and varying pitch. It can be seen that up to overlay imprecision of 4.5nm, a design with an 8nm pitch gives a higher effective yield. For overlay imprecision greater than 4.5nm, a 9nm pitch design has a better yield. This result suggests starting manufacturing at a relatively lower density and gradually scaling down the pitch with improvements in manufacturing alignment. While at high overlay imprecision, a low density fabric offers a better effective yield, with improvement in alignment precision a denser fabric can be obtained.

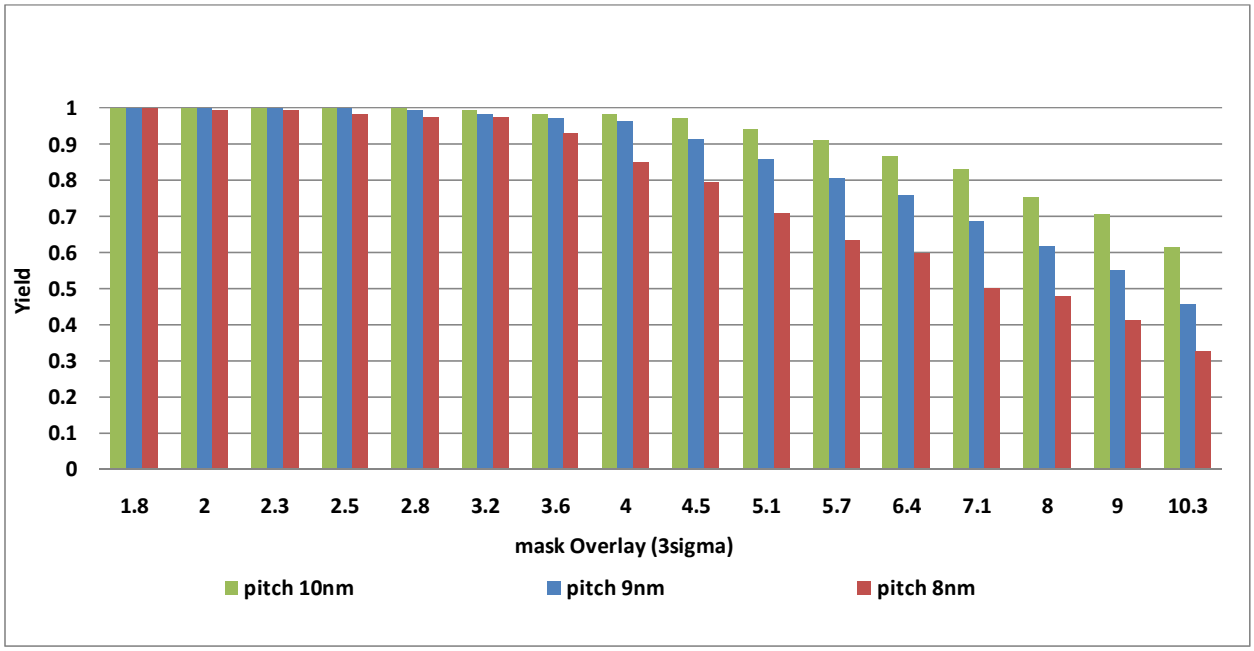

Figure 19. Variation in yield for width of 5nm

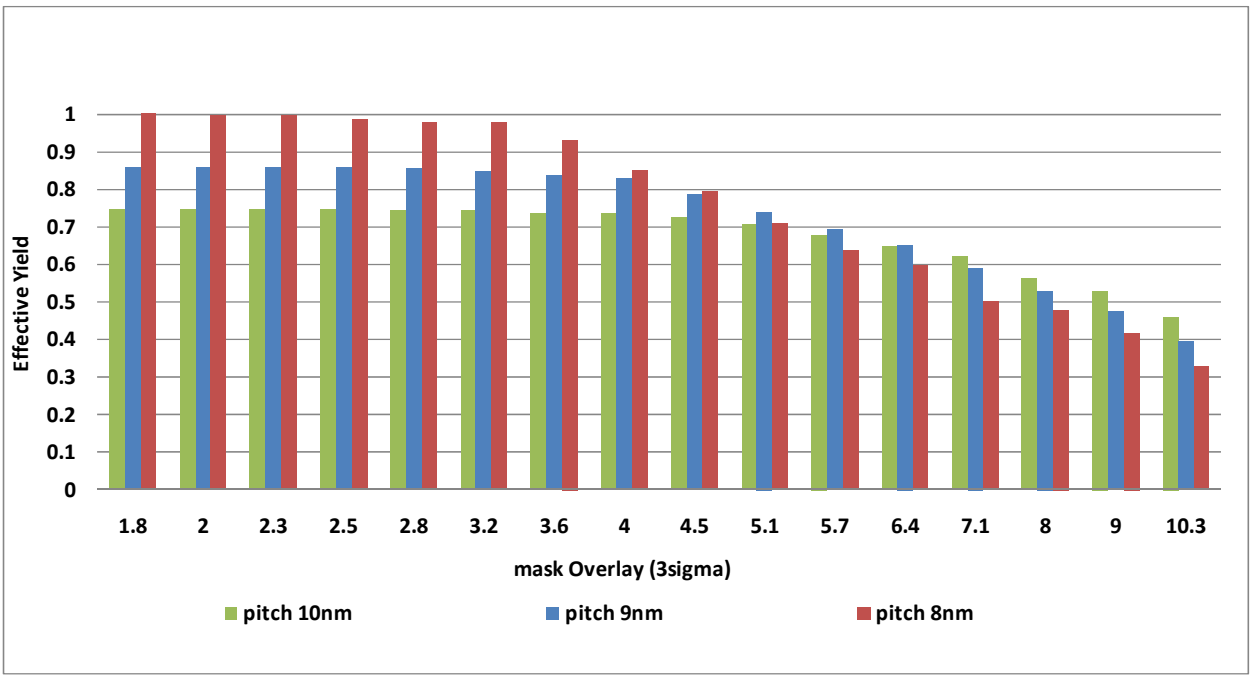

Figure 20. Variation in effective yield for width of 5nm

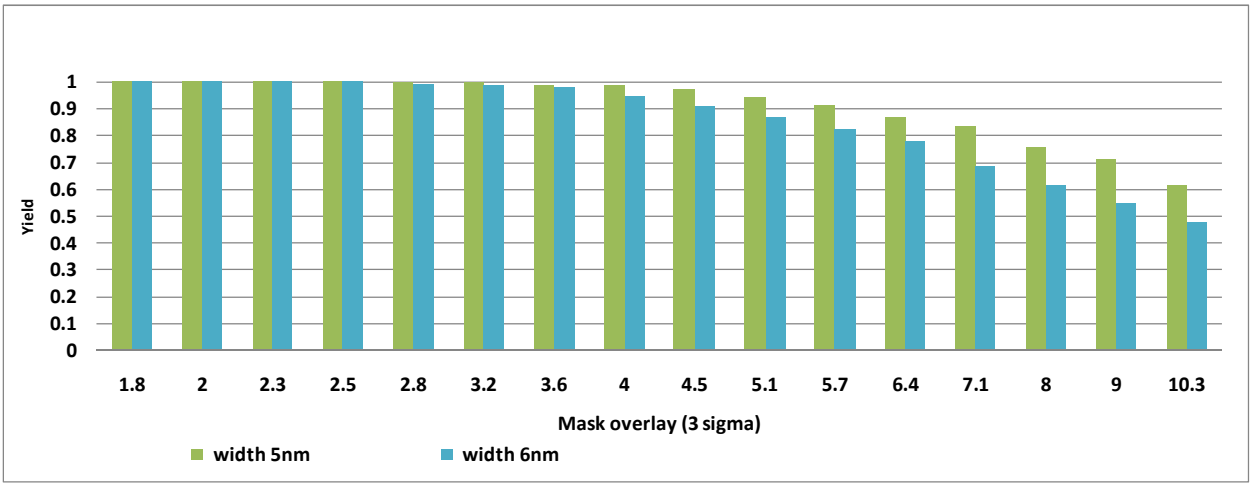

Figure 21. Variation in yield for nanowire pitch of 10nm

5.4.1.2. Sensitivity to width

The sensitivity of overlay-limited yield to nanowire width was also evaluated. For a given pitch, the area of a NASIC design is constant irrespective of the width. Evaluation was carried out for

varying mask overlay for a WISP design mapped to 10nm pitch and different nanowire widths as shown in Fig. 21. At a constant pitch, an increase in the width of the nanowires would imply an increased channel cross-section for devices and hence a greater Ion current for devices, leading to performance improvements. On the other hand, yield loss due to overlay imprecision increases due to decreasing spacing between the adjacent wires. For example, in Fig. 15, the margin for functionalization mask misalignment was shown to be (p-w)/2, which implies that the misalignment margin is reduced with increasing widths, leading to yield loss. Similar trends were observed for other process steps.

The trends for a pitch of 10nm are shown in Fig. 21. As expected, for the same 3-sigma overlay imprecision, the yield is lower since less misalignment tolerance is available.

The following observations were made during the evaluation: a) the impact of the nanowire width on the yield increases with increasing overlay imprecision, b) the *rate of decrease in yield* with increasing width, is faster at lower pitches as expected, c) the 'sensitivity of yield to width' analysis aids in achieving an efficient yield-performance tradeoff during the manufacturing

An analysis of the contribution of each manufacturing step towards the yield loss was also carried out. This can be used to bring about improvements in manufacturing flow. The results in Fig. 22 show that the vertical functionalization step (Fig. 5.H) is the most sensitive to mask overlay effects. Additional alignment markers may be used to alleviate overlay imprecision for this step. It can also be observed that the horizontal contact creation step (Fig. 5.B) is the least contributor towards yield loss, implying that nanofabrication techniques (based on contact patterning or self-assembly based approaches) tend to favor the formation of regular periodic structures such as grids as the bottom most layer. Registration requirements in such regular structures are alleviated since

an initial lithography mask may be 'offset' with no loss of functionality. In CMOL [17] and HP's FPNI [9], nanofabric unconventional techniques such as Nanoimprint are necessary after the fabrication of CMOS layers. This results in overlay alignment for imprint lithography with 3σ=±105nm [59], which implies significant challenges in alignment against previously formed features. Such a large overlay misalignment can contribute to significant yield losses (or conversely trade-off much of the density benefit for acceptable yield) and is not ideal. Furthermore, if an unconventional manufacturing step is performed before any lithographic masking, it is not affected by any overlay requirement. Thus, the result motivates us to utilize the uniform nanowire grid as the bottom most layer in the manufacturing pathway.

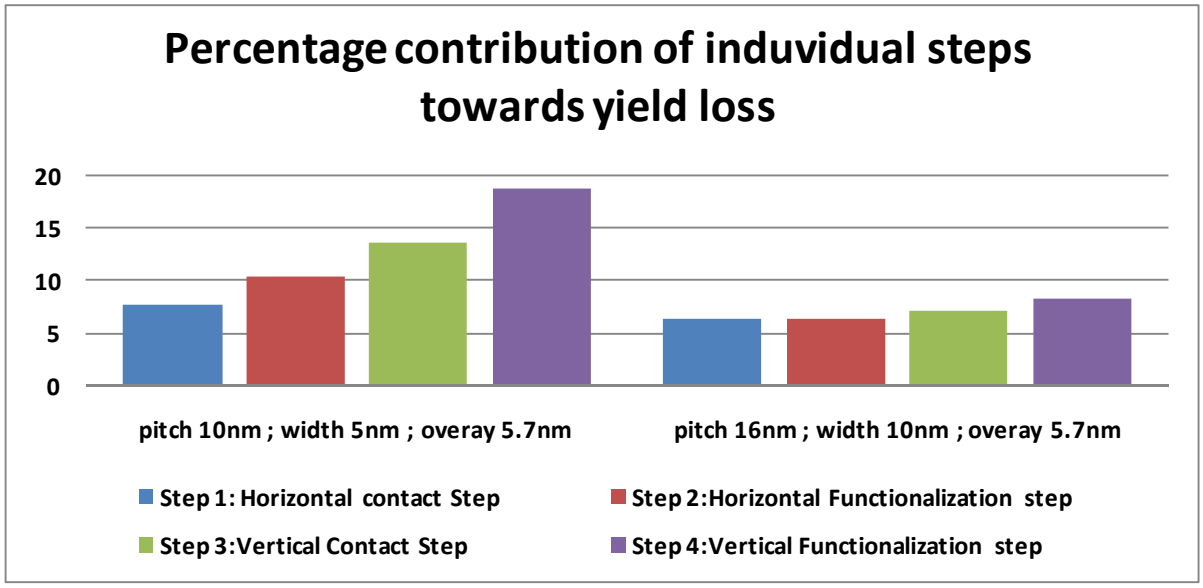

Figure 22. Percentage contributions of individual steps towards yield loss

5.4.1.3. Sensitivity to mask feature size

The impact of the varying mask feature size on the systematic yield loss due to mask overlay imprecision was evaluated. The mask feature size was varied from dimensions of (pitch X pitch) up until [(2p-w) X (2p-w)], where *w* is the width and *p* is the pitch of nanowire. Fig. 23 shows transistor defects that arise from misalignment of the mask (with mask feature size being

(2p-w) X (2p-w)). Fig. 23.a shows the correct alignment scenario. A vertical misalignment less than [p-w/2] but greater than w, has resulted in shorted channels across the horizontal nanowire array, leading to yield loss (Fig. 23.c). While at this point the chip is already defective, for completeness, a case where both incorrectly shorted and incorrectly functionalized devices are created is shown (Fig. 23.b) when the misalignment exceeds (p-w/2). Fig. 23.d shows the formation of FET at the intended position as well at an undesired location due to mask overlay. To summarize,

[m/2 + O] >= (p + w/2), resulted in the formation of transistors at undesired locations;

[O > m/2 – w/2], resulted in shorting of devices;

where,

m = minimum feature size

O = mask overlay

w = nanowire width

p = nanowire pitch

Fig. 24 depicts the results for pitch of 16nm, width of 8nm. The mask feature size was varied from 16nm (pitch X pitch) up until 24nm [(2p-w) X (2p-w)]. Percentage increase in yield of up to 9% was seen when mask overlay of 5.7nm was considered. However, the increase in yield due to the increased mask feature size was ~1% at high mask overlay of 10.3nm. The results also indicate that the occurrence of open interconnect is less probable (as ion implant creates high conductive region and aids in alleviating overlay imprecision) and hence results in yield

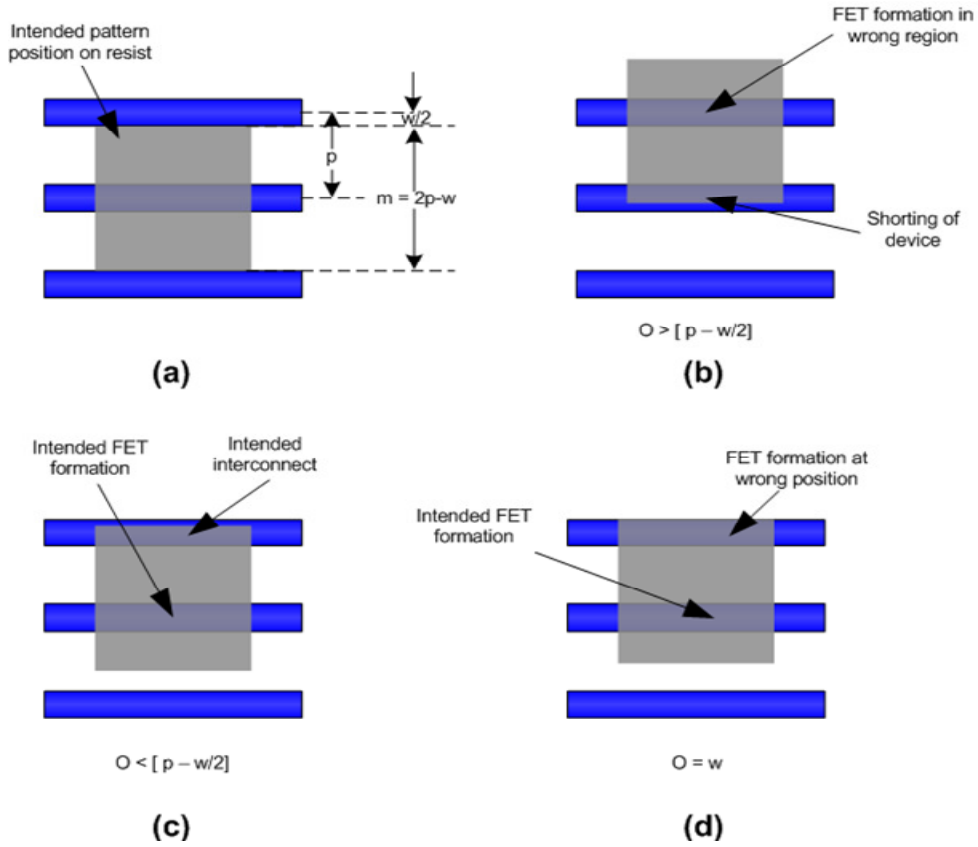

Figure 23. Implication of mask overlay with mask feature size of dimension (2p - w) X (2p - w)

improvement. The results also emphasize that manufacturing requirements can be significantly alleviated for a larger feature size. The yield drops to a very low value upon increasing the minimum feature size to 25nm (which is greater than [(2p-w) X (2p-w)]). This is due to the fact that a very minimum overlay would also result in the formation of a transistor at the wrong position. Fig. 25 depicts the yield for pitch 10nm, width 5nm nanowires for mask feature size varying from 10nm to 15nm.

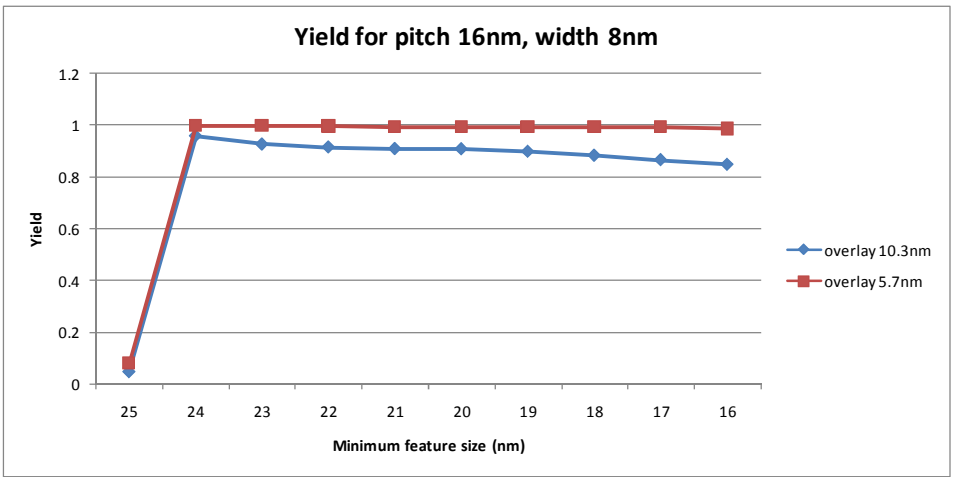

Figure 24. Yield for varying mask feature size, pitch 16nm, width 8nm

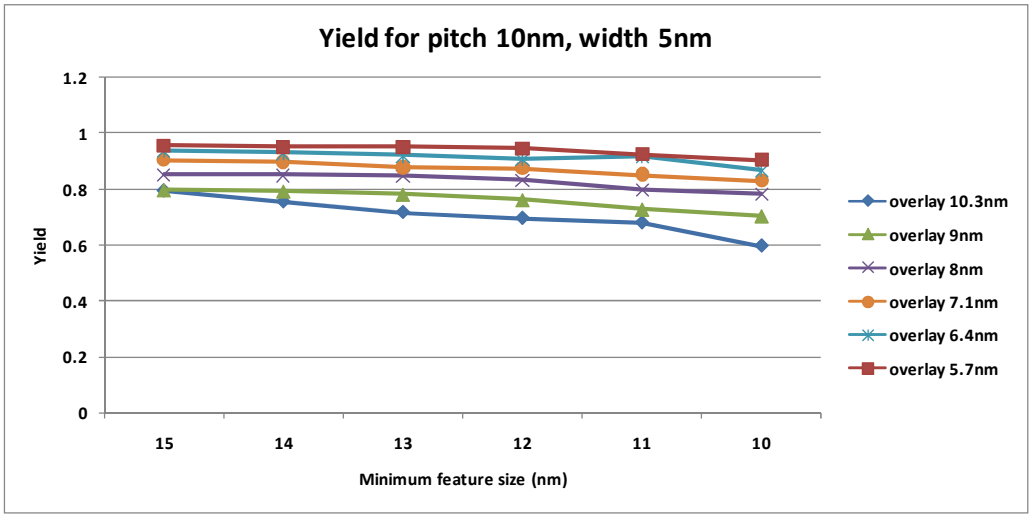

Figure 25. Yield for varying mask feature size, pitch 10nm, width 5nm

5.4.2 'Nanowire transfer' implications on Systematic Yield

The implication of nanowire transfer step on the systematic yield was evaluated. The physical parameters (pitch, width) of the fabric play an important role in yield estimation. The simulations were performed for varying pitch and width. The yield loss due to nanowire transfer varied from ~40% (at 3σ mask overlay of 1.8nm) to ~37% (at 3σ mask overlay of 10.3nm) for 16nm pitch nanowires. This result shows that the yield due to Nanowire transfer is more critical

than the mask overlay limited yield. The results also indicate slight improvement in yield due to decreasing width of nanowire for a constant pitch. Fig. 26 shows the Nanowire transfer limited yield loss for pitch 18nm, 20nm and 22nm respectively (for various widths, and selected mask overlay). A yield loss of ~40-50% was observed in the above scenario.

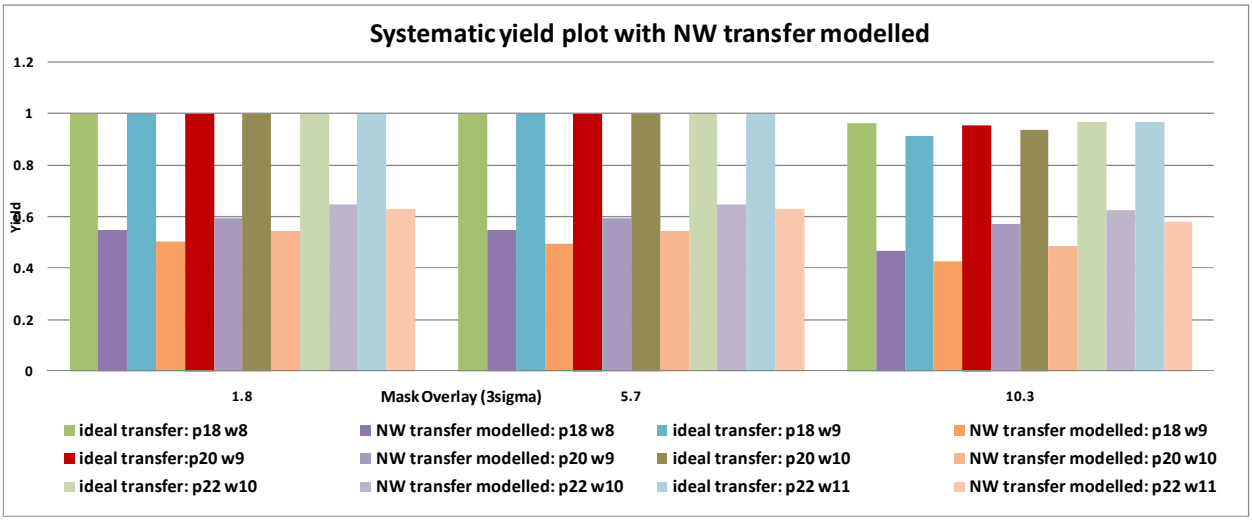

Figure 26. Yield with Nanowire (NW) transfer modeled; for varying NW width and pitch

In order to account for the area penalty of the large pitch, effective yield was also evaluated. It can be seen from Fig. 27 that when ideal NW transfer is assumed, pitch 16nm; width 8nm designs had the highest effective yield. However, upon modeling the NW transfer, (Fig. 28) it was seen that pitch 18nm, width 8nm designs had the highest effective yield. [With the base design being WISP-0 mapped to 10nm pitch fabric; effective yield is given by, (Effective Yield)= (Yield at NW pitch considered)*(Area of WISP-0 at 10nm pitch)/(Area of WISP-0 at NW pitch considered)]. Hence, the choice of the physical parameters of the fabric can be made depending on the precision of the manufacturing step available.

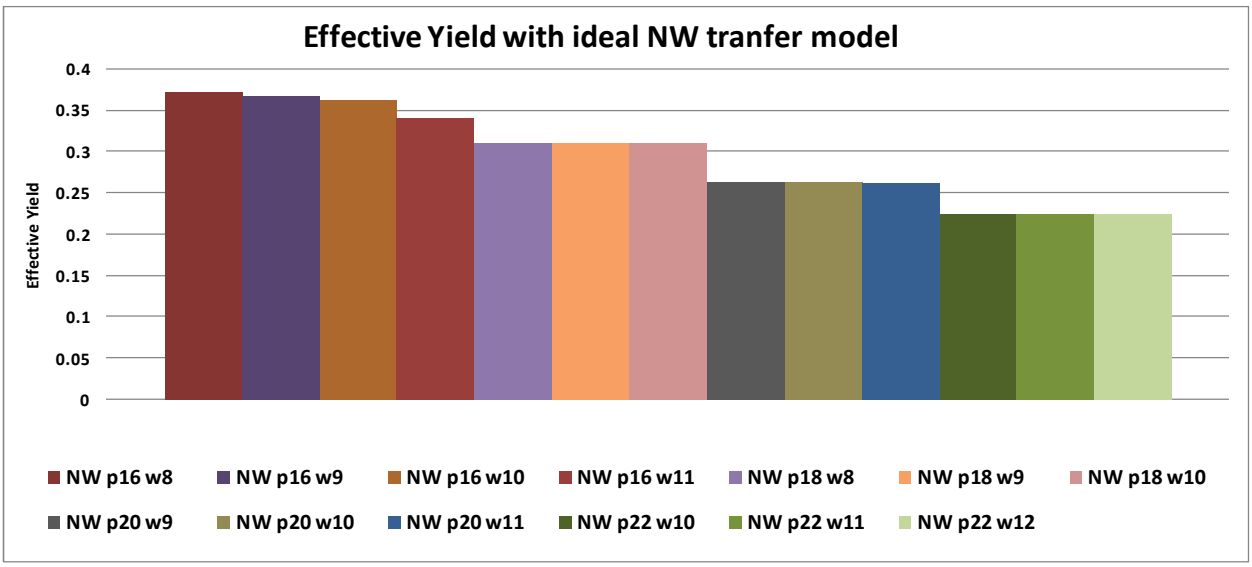

Figure 27. Effective yield plots for varying pitch and width

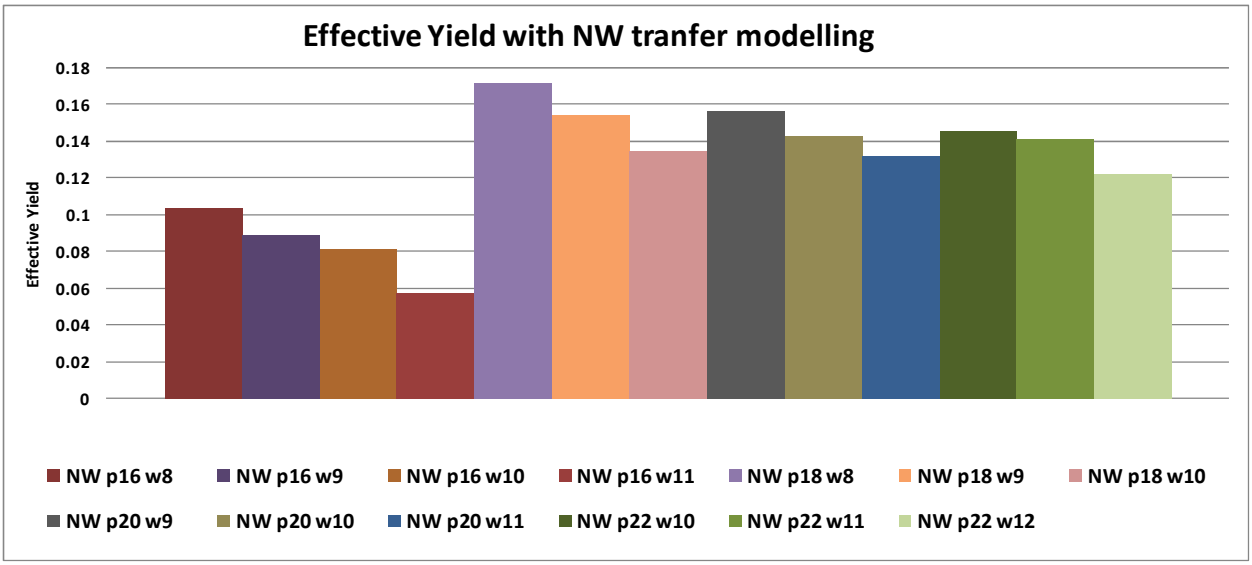

Figure 28. Effective yield plots for varying pitch and width (NW transfer modeled)

5.5. Conclusion

The current chapter discussed the systematic yield calculation of the WISP-0 design mapped to NASIC fabric. However, the overall yield of the design is of significance. Is the particulate limited yield loss independent of the systematic yield loss? Does nanowire transfer

result in interdependency among the two yield estimates? The above questions are answered in the next chapter where the overall yield estimation procedure is discussed.

CHAPTER 6

OVERALL YIELD ESTIMATION

Chap. 4 discussed the particulate limited yield loss and Chap.5 discussed the systematic yield loss. However, the interdependency between the above two yield losses needs to be evaluated. Variation in the critical area is estimated based on evaluation of functional wisp layout witnessing nanowire misalignment due to transfer step. The functional wisp layout (upon nanowire transfer) was subjected to POF evaluation using the approach mentioned in section 4.2.

Fig. 29 shows the variation in POF (shorts) for 16nm pitch at widths 8, 9, 10 and 11nm. An increase of up to ~6% was seen in POF for shorts. Similar analysis was carried out for opens which saw a decrease of up to ~4%. Critical Area was subsequently evaluated which was used for particulate limited yield loss estimation. Fig. 30 shows the particulate limited yield loss at the projected defective density 0.01 defects/cm.sq. Fig. 31 depicts the particulate limited yield loss using the clustered parameter. (See Chap. 4 for more details).In both the scenarios, no variation was seen in the particulate limited yield loss, with and without systematic variation. It must be noted that the increase or decrease observed in Critical Area would have an influence on the random defect limited yield only when the area of the design is large. For smaller designs, the number of defects observed is very small and hence even a considerable change in critical area may not manifest as random yield loss. Therefore, variations in POF did not show any variation in yield due to the small area of the WISP design used for evaluation. However, a variation of 0.05% in yield would be seen at designs of area 10^{10} as that of WISP area. This leads us to the conclusion that the interdependence of systematic yield loss and the particulate limited yield loss is negligible and hence the two can be considered independent.

The overall yield of the design can hence be considered as the product of the particulate limited yield and systematic yield as shown in Fig. 32 and Fig. 33. The overall yield of design mapped to NASIC fabric of pitch 16nm, width 8nm at defect density of 0.01 defects/sq.cm is given by Fig.32 and at 0.1 defects/sq.um is given by Fig. 33 respectively. The systematic yield analysis

however assumes zero rotational misalignment of nanowires and also the nanowires to be perfectly parallel. The above assumptions are valid and hold true for designs of WISP-0 dimension. However, the above assumptions need to be revisited when analyzing larger designs.

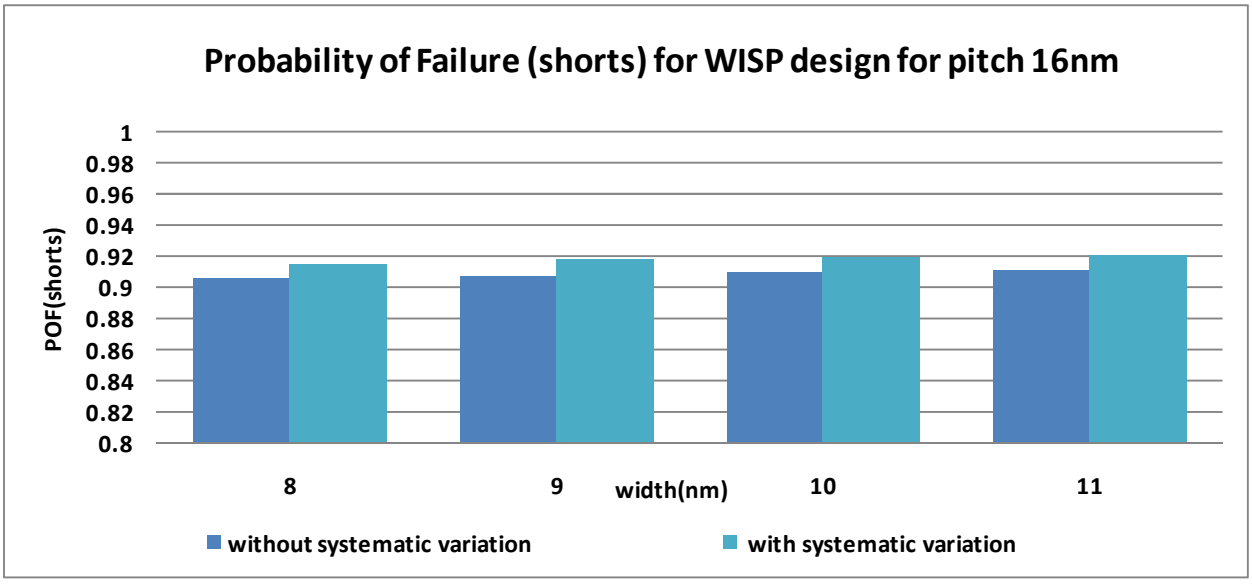

Figure 29. POF plot for pitch 16nm; width 8, 9nm (with and without systematic variation)

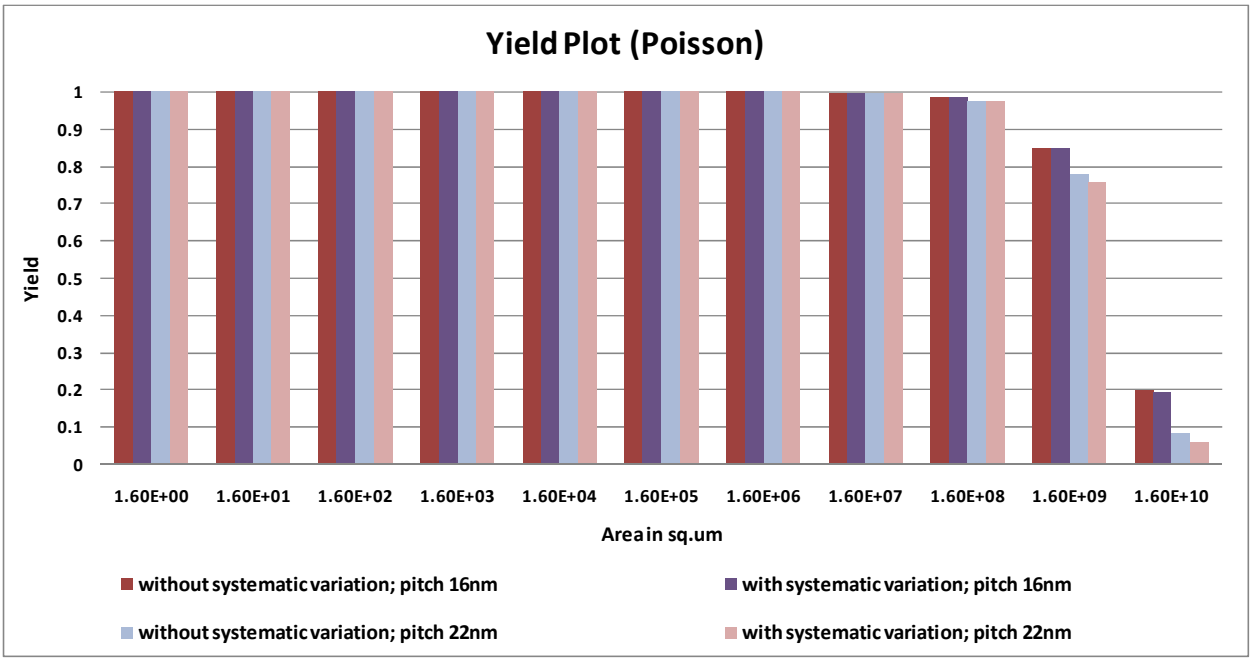

Figure 30. Particulate Limited Yield loss using Poisson model

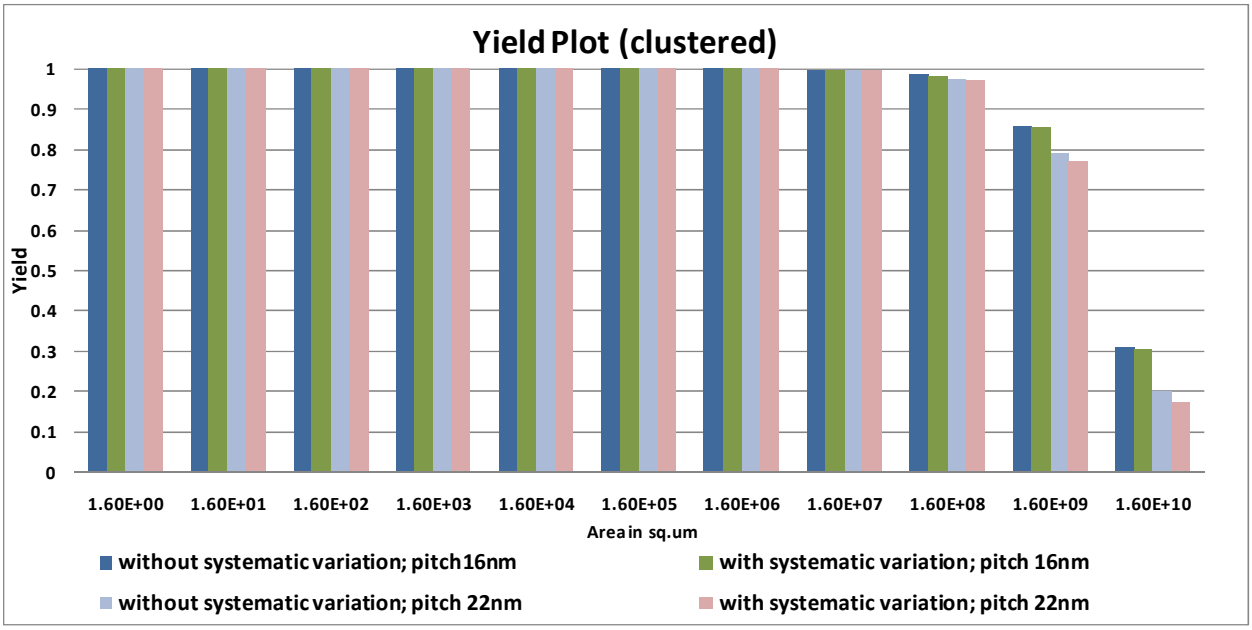

Figure 31. Particulate Limited Yield loss using Clustered model

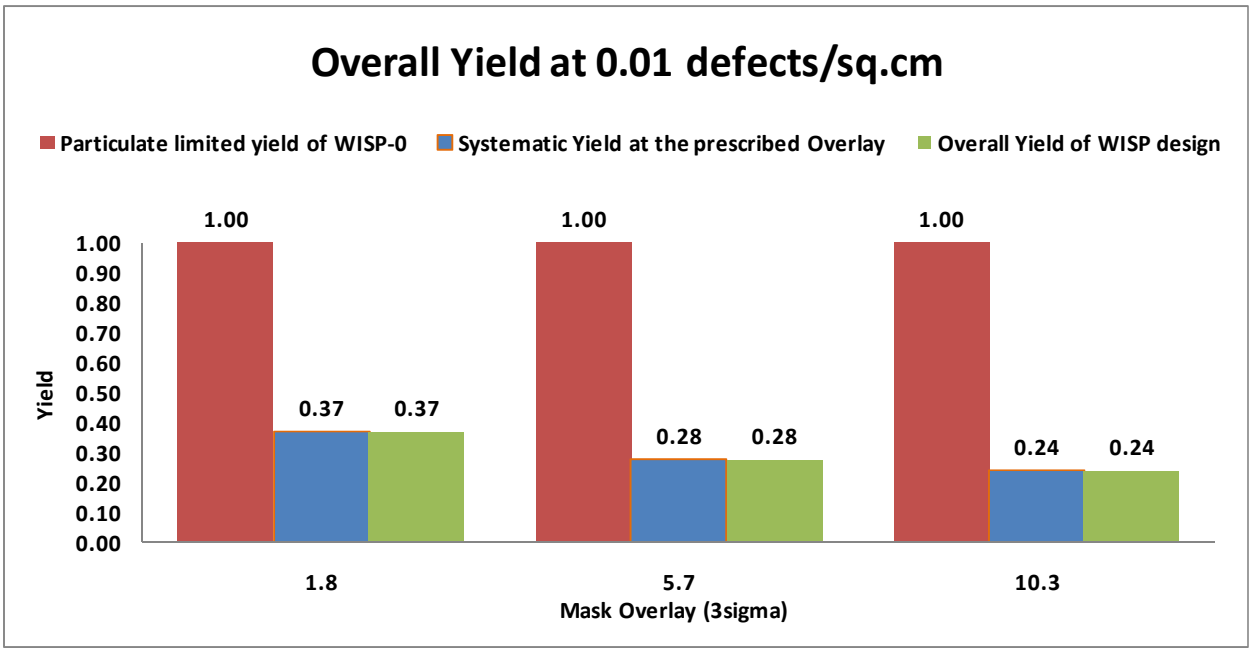

Figure 32. Overall Yield estimation of wisp design at pitch16nm; width 8nm

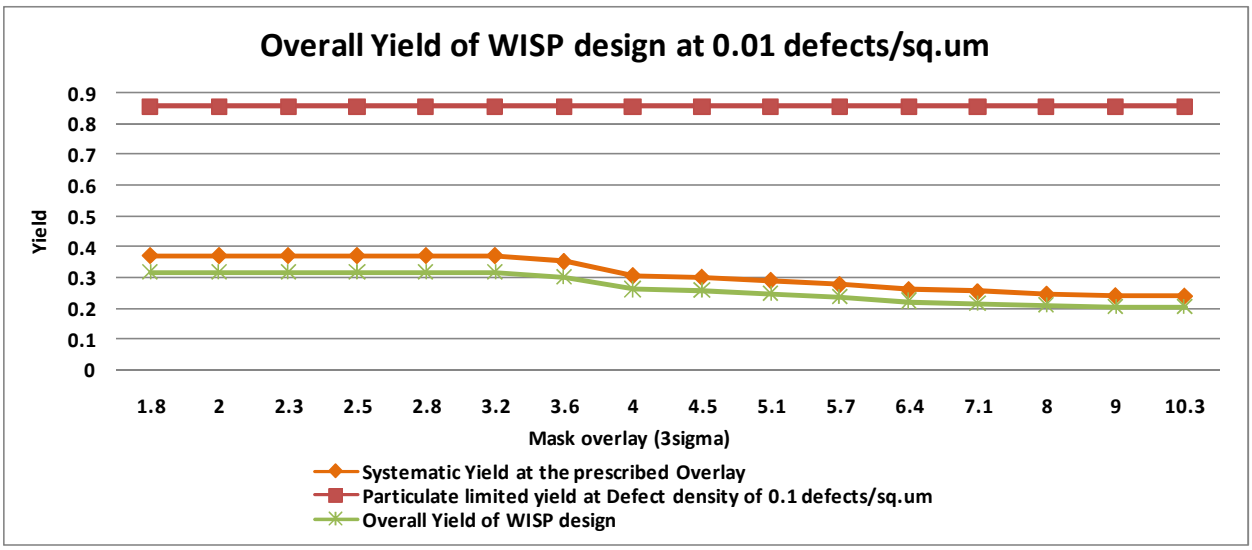

Figure 33. Overall Yield estimation of wisp design at pitch16nm; width 8nm (at varying overlay)

CHAPTER 7

CONCLUSION

To understand and deal with the challenges associated with a bottom-up fabrication of nanoelectronic circuits, identification of defects introduced during each step of the manufacturing pathway is essential. A study of the yield implications of the manufacturing sequence proposed for NASIC has been presented. The sensitivity of the projected yield to physical fabric parameters was evaluated. It was evident that the nanowire transfer was the most critical step in the manufacturing process which resulted in ~40% systematic yield loss. An analysis of the contribution of each manufacturing step towards the yield loss was also carried out. This can be used to bring about improvements in manufacturing flow. The results also show that the vertical functionalization step is the most sensitive to mask overlay effects. Additional alignment markers may be used to alleviate overlay imprecision for this step. It can also be observed that the horizontal contact creation step is the least contributor towards yield loss, implying that nanofabrication techniques (based on contact patterning or self-assembly based approaches) tend to favor the formation of regular periodic structures such as grids as the bottom most layer. Registration requirements in such regular structures are alleviated since an initial lithography mask may be 'offset' with no loss of functionality. The pitch and width of the nanowire can be chosen in accordance with the lithographic alignment precision available to achieve an intended chip yield. Finally, the overall yield of the WISP-0 design was calculated considering both systematic and particulate limited yield loss.

The thesis estimated the yield loss by analyzing the sources of defects in a nano-manufacturing flow. It integrates physical fabric considerations, manufacturing sequences and the resulting defect scenarios. This is in contrast to most current approaches that use conventional defect models and assume constant defect rates without analyzing the manufacturing pathway to determine the sources of defects and their probabilities. The manufacturing pathway was analyzed for identifying the defects introduced during each manufacturing step in the sequence, followed by

yield loss estimation. The yield analysis can hence be used to identify effective design choices in fabric manufacturing. The pitch and width of the nanowire can be chosen in accordance with the lithographic alignment precision, nanowire transfer precision, available to achieve an intended chip yield.

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