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A Theoretical Approach to Fault Analysis and Mitigation in Nanoscale Fabrics

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A THEORETICAL APPROACH TO FAULT ANALYSIS AND MITIGATION IN NANOSCALE FABRICS

A Thesis Presented

By

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ABSTRACT

A THEORETICAL APPROACH TO FAULT ANALYSIS AND MITIGATION IN NANOSCALE FABRICS

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High defect rates are associated with novel nanodevice-based systems owing to unconventional and self-assembly based manufacturing processes. Furthermore, in emerging nanosystems, fault mechanisms and distributions may be very different from CMOS due to unique physical layer aspects, and emerging circuit and logic styles. Thus, theoretical fault models for nanosystems are necessary to extract detailed characteristics of fault generation and propagation. Using the intuition garnered from the theoretical analysis, modular and structural redundancy schemes can be specifically tailored to the intricacies of the fabric in order to achieve higher reliability of output signals.

In this thesis, we develop a detailed analytical fault model for the Nanoscale Application Specific Integrated Circuits (NASIC) fabric that can determine probabilities of output faults taking into account the defect scenarios, the logic and circuit style of the fabric as well as structural redundancy schemes that may be incorporated in the circuits. Evaluation of fault rates using the analytical model for single NASIC tiles show an inequality of the probability of output faulty ‘1’s and ‘0’s. To mitigate the effects of the

unequal fault rates, biased voting schemes are introduced and are shown to achieve up to 27% improvement in the reliability of output signals compared to conventional majority voting schemes.

NASIC circuits have to be cascaded in order to build larger systems. Furthermore, modular redundancy alone will be insufficient to tolerate high defect rates since multiple input modules may be faulty. Hence incorporation of structural redundancy is crucial. Thus in this thesis, we study the propagation of faults through a cascade of NASIC circuits employing the conventional structural redundancy scheme which is referred to here as the *Regular Structural Redundancy*. In our analysis we find that although circuits with *Regular Structural Redundancy* achieve greater signal reliability compared to non-redundant circuits, the signal reliability rapidly drops along the cascade due to an escalation of faulty '0's. This effect is attributed to the poor tolerance of input faulty '0's exhibited by circuits with the Regular Structural Redundancy. Having identified this, we design a new scheme called the *Staggered Structural Redundancy* prioritizing the tolerance of input faulty '0's. A cascade of circuits employing the *Staggered Structural Redundancy* is shown to maintain signal reliability greater than 0.98 for over 100 levels of cascade at 5% defect rate whereas the signal reliability for a cascade of circuits with the Regular Structural Redundancy dropped to 0.5 after 7 levels of cascade.

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CHAPTER 1

INTRODUCTION

A variety of nano-materials and nano-devices including semiconductor nanowires [1],[2], carbon nanotubes [3], quantum cellular automata (QCA) [4], graphene-based devices [5], spin-wave fabrics [6] and molecular devices [7] have been proposed as alternatives to conventional CMOS. However, self-assembly and unconventional manufacturing approaches for scalable assembly of nanostructures may imply orders of magnitude higher defect rates compared to CMOS [8]. Furthermore, nanoscale computational fabrics may have very different fault models due to novel circuit and logic styles and different defect scenarios. It is thus necessary to first study the fault characteristics in nanoscale fabrics using detailed theoretical models. The intuition garnered from this analysis will facilitate the design of fault-tolerance schemes that are better tailored to these unique fault characteristics thus achieving improved yield.

In this thesis, we derive detailed analytical expressions for the probability of '0' to '1' faults (referred to as faulty '1's) and '1' to '0' faults (faulty '0's) at the output of circuits implemented in the Nanoscale Application Specific ICs (NASICs) fabric [9] [10]. The expressions are in terms of the probability of defects, input faults and the specific logic and circuit styles of the fabric. The detailed analytical fault models are also capable of accounting for structural redundancies that may be implemented within the circuits. Results obtained from analyzing single NASIC tiles using the model indicate that the probabilities of the two types of faults are unequal. Since one fault is more likely to occur, biased voting schemes instead of conventional majority voting schemes provide higher signal reliabilities by offering greater protection against the most likely faults. Our

theoretical analysis shows that the biased voting schemes provide up to 27% improvement in signal reliability compared to the conventional majority voting schemes.

To build larger systems NASIC circuits will have to be cascaded. Hence, evaluation of the fault characteristics and improvement of the signal reliability through cascaded NASIC tiles is necessary. Furthermore, modular redundancy alone will not be sufficient to tolerate the high defect rates characteristic of nanoscale fabrics since multiple input modules may be faulty. Thus, structural redundancy needs to be incorporated within individual circuits. Thus in this thesis, we study the propagation of faulty '1's and faulty '0's through cascades of structurally redundant NASIC circuits and their effect on the overall Signal Reliability. In our analysis, we demonstrate that the Signal Reliability through cascades of circuits employing the conventional structural redundancy scheme (referred to as Regular Structural Redundancy (RSR)) rapidly drops along the cascade due to an escalation of the probability of faulty '0's. Having identified that Regular Structural Redundancy schemes are intolerant of input faulty '0's, we propose and introduce a novel structural redundancy scheme called the Staggered Structural Redundancy (SSR) that offers improved resilience against input faulty '0's. The novel Staggered Structural Redundancy schemes are shown to have 56% improved tolerance of input faulty '0's compared to the Regular Structural Redundancy. Our results show that although the signal reliability through cascades of RSR circuits drops to 0.5 after 7 levels of cascades at 10% defect rate, the signal reliability through cascades of SSR circuits remain above 0.98 for over 100 levels of cascade due to its adequate capability of tolerating both input faulty '1's and '0's.

The rest of the thesis is organized as follow. Chapter 2 discusses related prior work in the fault tolerance in nanofabrics and provides overview of NASICs and its structural redundancy schemes. Chapter 3 provides the derivation of the detailed analytical fault models for the NASIC fabric, both for circuits with and without structural redundancy. Chapter 4 utilizes the analytical models to demonstrate the benefits of biased voting schemes in improving signal reliability. Chapter 5 provides a study of the fault propagation through cascades of circuits with conventional structural redundancy and introduces a novel structural redundancy which is shown to achieve improved signal reliability. Finally, chapter 6 summarizes this thesis.

CHAPTER 2

RELATED BACKGROUND

2.1 Overview of NASICs

Nanoscale Application Specific Integrated Circuits (NASICs) [11]-[16] is a computational fabric based on a 2-dimensional grid of semiconductor nanowires with external dynamic control for data streaming and cascading.

Cross-nanowire transistors (xnwFETs) are formed at selected cross-points to implement the logic function. Microwires are used to provide VDD, GND and control signals for data streaming. In NASICs, the 2-stage dynamic NAND-NAND logic style is one of the logic families used [14]. The output signals from the first stage NAND gates become the input signals for the nanowire transistors in the second stage NAND gate. Dynamic circuits and pipelining in NASICs obviate the need for explicit latching and improves the density. Furthermore, the NAND-NAND logic style requires only n-type xnwFETs leading to a simplified manufacturing pathway.

The elemental unit in NASICs is called a *Tile*. It is a single NASIC circuit implementing a 2-stage logic function. Figure 1 shows a single NASIC tile (consisting of 2 dynamic NAND stages) implementing a 1-bit full adder. In Figure 1, hpre and heva are the precharge and evaluate control transistors that enable dynamic circuit evaluation. Many such tiles can be cascaded together to build a large-scale system such as a processor [17] or an image processing architecture [18].

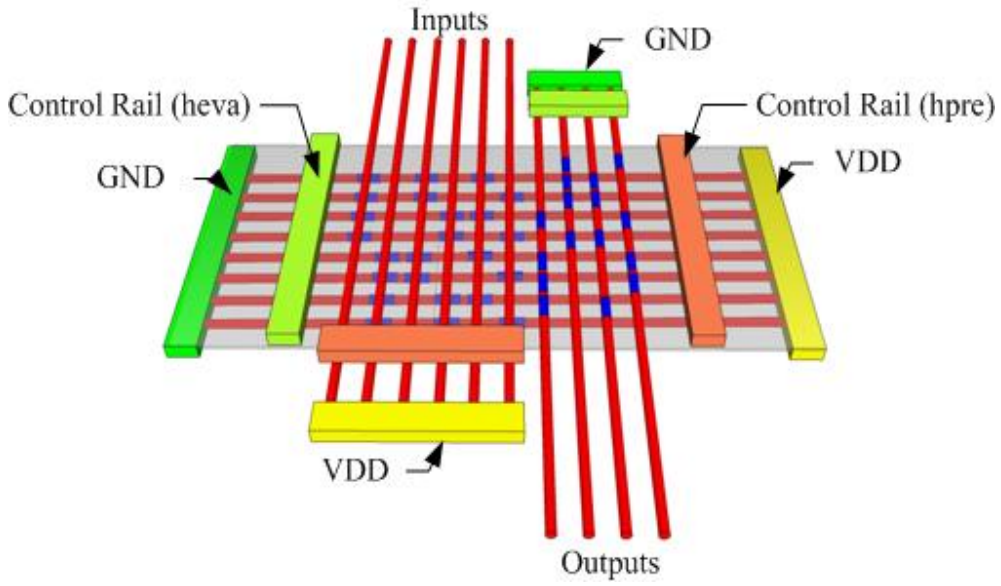


Figure 1. A full adder implemented in NASICs

In NASICs, high fan-in circuits are possible since delay scales linearly with respect to fan-in as opposed to conventional CMOS where the trend is typically quadratic [19]. This is due to the unique dynamic control schemes used, where successive cascaded stages are evaluated using different control signals. The series stack resistance of a given stage is overcome during and after the pre-charge of the previous stage. This implies that during the evaluation of the current stage, only the linear impact of capacitance affects the performance with increasing fan-in. This behavior has been verified through detailed simulations of device behavior and circuit characteristics. Additional details can be found in [19].

2.2 Fault Tolerance in Nanofabrics

Self-assembly and unconventional manufacturing approaches for scalable assembly of nanostructures may imply orders of magnitude higher defect rates compared to CMOS [8]. Therefore, built-in fault tolerance techniques need to be incorporated in

nanoscale systems at various levels to achieve high-yield systems. Prior work on fault tolerance of hard defects includes techniques such as reconfiguration and built-in redundancy. Techniques for reconfigurable fabrics include mapping of logic functions onto defective circuits or reconfiguring around defective blocks [20] -[23] and built-in self test techniques for testing and diagnosis [24][25]. In hardware redundancy techniques for non-reconfigurable crossbar architectures, a lot of the previous work concentrated on the efficient mapping of logic functions onto defective crossbars [26]-[28]. Both these approaches lead to technical challenges such as the need for special reconfigurable devices or the complex interfacing between micro and nano circuits to extract defect maps.

Modular redundancy techniques have been widely researched in the past few decades and include Triple modular redundancy (TMR) [29]-[32] and N-tuple modular redundancy [33]. Designs of new voter circuits [34] [35] and even NMR systems without a centralized voter [36] have been proposed. A more fine-grained built-in fault tolerance technique is the structural redundancy [37]. As the focus shifts to nanoscale devices, hardware redundancy techniques still hold promise [38]-[40].

2.3 Structural Redundancy in NASICs

In NASICs, possible defects include broken nanowires, stuck-on and stuck-off type defects. Reliable manufacturing of nanowires up to a few microns in length has been demonstrated in [2], so the frequency of broken nanowires is expected to be very low. Stuck-on transistors are the most prevalent in the proposed manufacturing pathway [41] due to the ion implantation and metallization processes involved.

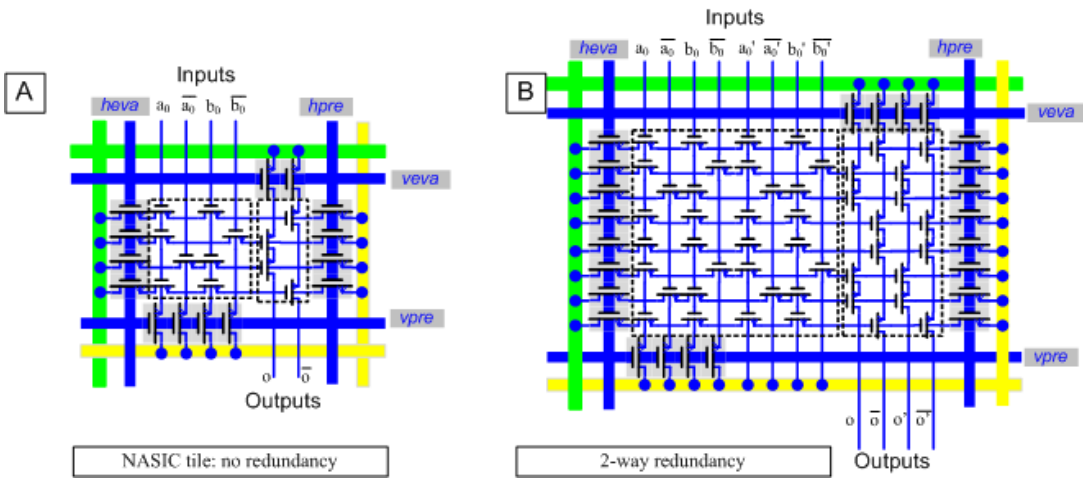


Figure 2. NASIC fault tolerance schemes: (a) NASIC tile with no redundancy incorporated. (b) 2-way redundant implementation of the NASIC tile in (a).

Structural redundancy is employed in NASICs by creating redundant copies of nanowires. Redundant signals are created and logically merged in the logic planes with regular signals. Every xnwFET has a redundant copy so that even if one of the copies is stuck-on, then the redundant copy or copies will be able to switch off, thus ensuring proper logic implementation.

Figure 2 (a) shows a single non-redundant NASIC tile and Figure 2 (b) shows its 2-way redundant implementation. In the 2-way redundant tile, every nanowire is duplicated, each containing twice as many xnwFETs. The redundant signals are merged within the logic plane itself. In Figure 2 (a) and (b), $\overline{a_0}$ and a_0' is the complement and the redundant signal of a_0, respectively.

CHAPTER 3

ANALYTICAL FAULT MODEL FOR NASICs

3.1 Introduction

Analytical fault models for NASICs are necessary to extract detailed characteristics of error generation and propagation. This will facilitate the exploration of improved fault tolerance schemes that are specifically tailored to the intricacies of the fabric. In this chapter, we first derive an analytical fault model for a NASIC tile without any structural redundancy and then extend it to include tiles with Regular Structural Redundancy. The analytical model is capable of calculating output fault rates and signal reliabilities in the presence of stuck-on defects and input faults.

3.2 Defect Model

Defects in the NASICs fabric depend on the manufacturing pathway used. One possible manufacturing pathway has been described in [41]. Reliable manufacturing of nanowires up to a few microns in length has been demonstrated in [2], so the frequency of broken nanowires is assumed to be negligible. Stuck-on transistors are the most prevalent in this pathway due to the ion implantation and metallization processes involved. Thus in the derivation of the model only stuck-on type defects are considered. The probability of a transistor being stuck-on, denoted by P_{S-ON}, thus represents the defect rate of the NASIC fabric in this chapter. These defects are considered to occur independently of each other, since they are caused by local effects (e.g. lateral diffusion after ion implant).

A defect rate of up to 15% is considered because, according to our initial work [13], at defect rates higher than this, any density advantage over projected CMOS would likely be eliminated in the context of microprocessor designs. It must be noted that this is a device-level defect rate and is 10 orders of magnitude higher than in scaled CMOS. For instance, CMOS defect rates are 0.4 defects/cm^2 [42] whereas 1%-15% defect rate in NASICs translates to billions of defects/cm^2.

3.3 Assumptions

In the derivation of the model, stuck-on defects in the NASIC tile are assumed to occur independently since they are caused by local effects such as lateral diffusion after ion implantation. The following assumptions are also made for tractability of the model:

- Logic functions on the NASIC tiles are assumed to be implemented in the canonical sum of products form without minimization.
- All the inputs of a tile are assumed to have the same probability of being faulty and they are assumed to occur independently.
- Occurrences of faults on horizontal nanowires are assumed to be independent of one another.

3.4 Notations

Figure 3 shows two NAND stages in a single n-input NASIC tile. Here, input signals are denoted by i. M_0 to M_{m-1} are the minterms generated by the first NAND stage and $T2_0$ to $T2_{m-1}$ denote the transistors in the 2nd stage NAND gate.

The rest of the notations that have been used in the derivation of the model are given in Table 1.

Table 1. Notations

Symbol	Description
n	Number of inputs for the logic function implemented
m	Number of minterms generated by the first NAND stage
S^C	Correct output of logic function
S^A	Actual fault-prone output from a defective NASIC tile
M_i^C	Correct ith minterm expected from a defect-free circuit, $0 \leq i \leq m-1$
M_i^A	Actual fault-prone ith minterm in a defective circuit
$T1^C$($T1^A$)	Correct (actual) state of Transistor in the first NAND stage
$T2_i^C$ ($T2_i^A$)	Correct (actual) state of Transistor gated by minterm Mi in the second stage NAND gate
$P_{0/1}^{out}$ = Prob$\{S^A=0\|S^C=1\}$	Probability of a faulty '0' at the output of a defective tile
$P_{1/0}^{out}$ = Prob$\{S^A=1\|S^C=0\}$	Probability of a faulty '1' at the output of a defective tile
$P_{0/1}^{min}$ = Prob$\{M_i^A=0\|M_i^C=1\}$	Probability of the minterm, Mi, being a faulty '0'
$P_{1/0}^{min}$ = Prob$\{M_i^A=1\|M_i^C=0\}$	Probability of the minterm, Mi, being a faulty '1'
$P_{0/1}^{inp}$	Probability that an input is faulty '0'

$P_{1/0}^{inp}$	Probability that an input is faulty '1'
$P_{ON/OFF}^{T1}$	$Prob(T1_i^A = ON \mid T1_i^C = OFF)$; Probability that transistor in first NAND stage, T1, is switched-on due to fault whereas ideally it should have been switched-off
$P_{ON/OFF}^{T2}$	$Prob(T2_i^A = ON \mid T2_i^C = OFF)$; Probability that transistor in second NAND stage, T2, is switched-on due to fault whereas ideally it should have been switched-off
P_{S-ON}	Probability that a transistor is Stuck-ON

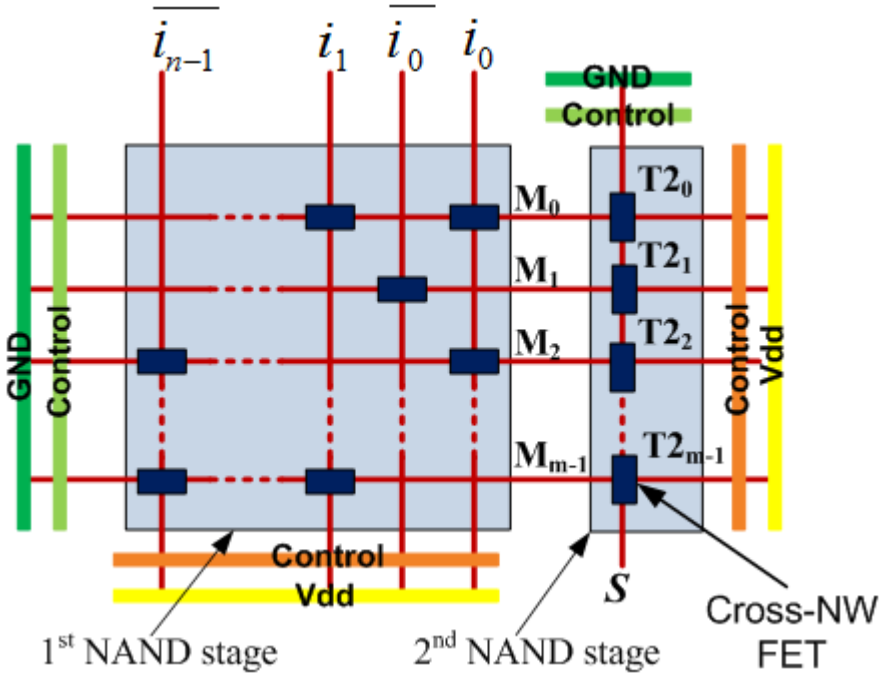


Figure 3. An n-input NASIC tile built with 2 NAND stages.

3.5 Tiles without Structural Redundancy

3.5.1 Occurrence of Faulty '1'

In this section we derive the equation for the probability of occurrence of a faulty '1' (0-to-1 fault) at the output of a structurally non-redundant NASIC tile, given the probability of stuck-on defects, stuck-off defects and input faults.

In a 2-stage dynamic NAND-NAND logic implementation, a '0' is produced at the output if all of the input signals (minterms) to the second stage NAND gate are '1's. Thus, in a NASIC tile, all of the xnwFETs (transistors) in the second stage dynamic NAND gate must be correctly switched on to allow the output to evaluate to '0'. Hence, for a faulty '1' to be produced at the output, any one of the transistors has to be switched-off to prevent evaluation to '0'. This will happen if any of the transistors in the 2nd stage NAND gate is incorrectly switched-off. Mathematically,

$$P_{1/0}^{out} = Prob\{S^A = 1 \,|\, S^C = 0\} = 1 - Prob\{S^A = 0 \,|\, S^C = 0\} \tag{3.1}$$

$$P_{1/0}^{out} = 1 - Prob\{\cap_{i=0}^{m-1}(T2_i^A = ON | T2_i^C = ON)\} \tag{3.2}$$

A transistor, $T2_i$ will be correctly switched-on in the event that the transistor is functional and the minterm gating it carries a correct '0', or in the event that the transistor is simply stuck-on. Thus,

$$P_{ON/ON}^{T2} = Prob\{T2_i^A = ON \,|\, T2_i^C = ON\}$$

$$P_{ON/ON}^{T2} = Prob\{T2_i = stuck-on \cup (T2_i = \text{not stuck on} \cap \mathrm{M_i^A} = 1 | \mathrm{M_i^C} = 1)\} \tag{3.3}$$

$$P_{ON/ON}^{T2} = P_{S-ON} + (1 - P_{S-ON})(1 - P_{0/1}^{min}) \tag{3.4}$$

Substituting Equation 3.4 into Equation 3.2 and simplifying, we get an expression for the probability of occurrence of a faulty '1' at the output of a NASIC tile,

$$P_{1/0}^{out} = 1 - (1 - P_{0/1}^{min} + P_{S-ON} \times P_{0/1}^{min})^m \tag{3.5}$$

The above probability of a faulty '1' has been expressed in terms of the probability of a transistor being stuck-on, P_{S-ON}, the number of minterm signals, m, and the probability of a minterm producing an incorrect '0', $P_{0/1}^{min}$.

In this model, the probability of a minterm being a faulty '0', $P_{0/1}^{min}$, is entirely dependent on the transistors of the first stage NAND gates being defective. The transistors in the first NAND stage are gated by tile inputs. For an n-input NASIC tile, there are 2^n possible input combinations. Since each of the horizontal nanowires in the first stage is a dynamic NAND gate, only for one particular input pattern should the output of the horizontal nanowire be '0'. The output should be a '1' for all of the rest of the input patterns. For each of these input patterns that should produce an output '1', one or more transistors will be correctly switched off to keep the output of the minterm at '1'. Thus, for a minterm to be a faulty '0', one or more transistors need to be incorrectly switched-on (depending on the input pattern), and the rest of the transistors need to remain correctly switched-on. For instance, in a 2 input logic function implemented in the NASIC fabric, at any one of the first stage NAND gates, there are 3 input patterns ($2^2 - 1 = 3$) that should produce an output of '1' at that NAND gate. 1 out of those 3 input patterns will require both transistors in the gate to be incorrectly switched-on to produce a faulty '0'. 2 of the input patterns will require 1 transistor to be incorrectly

switched-on and the other transistor to be remain correctly switched-on. Assuming all input patterns are equally probable, $P_{0/1}^{min}$ for this specific case of 2-input logic function would be,

$$P_{0/1}^{min} = \frac{1}{3}({P_{ON/OFF}^{T1}}^2 + 2P_{ON/OFF}^{T1}P_{ON/ON}^{T1}) \tag{3.6}$$

Extending this for an n-input NASIC tile and using the binomial theorem for simplification, the probability of minterm faulty '0' in an n-input tile is,

$$P_{0/1}^{min} = \frac{1}{2^n - 1}[\left(P_{ON/OFF}^{T1} + P_{ON/ON}^{T1}\right)^n - {P_{ON/ON}^{T1}}^n] \tag{3.7}$$

The above probability is written in terms of the probability of transistors in the first NAND stage being correctly and incorrectly switched-on. A transistor in the first stage may be incorrectly switched-on if it is either stuck-on or if the tile input gating the transistor is carrying a faulty '1'. Thus, the probability of T1 being incorrectly switched-on can be written as,

$$P_{ON/OFF}^{T1} = P_{S-ON} + (1 - P_{S-ON})(P_{1/0}^{inp}) \tag{3.8}$$

Similarly, the probability of a transistor in the 1st NAND stage being correctly switched-on is the probability of the event that the transistor is stuck-on or the transistor is functional with the input gating the transistor carrying a correct logic '1'. Thus,

$$P_{ON/ON}^{T1} = P_{S-ON} + (1 - P_{S-ON})(1 - P_{0/1}^{inp}) \tag{3.9}$$

Finally, by substituting Equation 3.8 and 3.9 into Equation 3.7 and subsequently substituting Equation 3.7 into Equation 3.5, the expression for the probability of an

output faulty ‘1’ is expressed in terms of the probability of stuck-on defects, the probability of input faults, the fan-in and the number of minterms of the specific NASIC tile.

3.5.2 Occurrence of Faulty ‘0’

In this section we derive the equation for the probability of occurrence of a faulty ‘0’ (1-to-0 fault) at the output of a NASIC tile. A faulty ‘0’ is said to occur when the inputs to a tile are such that in an ideal case, the output of the tile should be a ‘1’ but due to defects within the tile and input faults from the preceding tile, the output is a ‘0’.

When an input pattern that should produce a ‘1’ at the output of a defect-free circuit arrives at such a 2-stage NAND-NAND circuit, all of the minterms (inputs to the second NAND stage) carry logic ‘1’ except for one minterm, Mx, that carries a logic ‘0’. Thus, only one transistor, say Tx, at the second stage NAND gate is correctly switched-off in a defect-free circuit to keep the output at logic ‘1’. Hence, for a faulty ‘0’ to occur in a defective circuit, transistor Tx should be incorrectly switched-on while the other transistors remain switched-on, enabling evaluation to faulty ‘0’.

$$P_{0/1}^{out} = Prob(S^A = 0 | S^C = 1) \tag{3.10}$$

$$P_{0/1}^{out} = Prob\{(\bigcap_{i=0;i\neq x}^{m-1} T2_i^A = ON | T2_i^C = ON) \bigcap (T2_x^A = ON | T2_x^C = OFF)\} \tag{3.11}$$

$$P_{0/1}^{out} = {P_{ON/ON}^{T2}}^{m-1} \times P_{ON/OFF}^{T2} \tag{3.12}$$

Transistor $T2_x$ will incorrectly switch-on in the event that the transistor is functional but the minterm gating the transistor is incorrectly '1'or in the event that the transistor is stuck-on.

$$P_{ON/OFF}^{T2} = P_{S-ON} + (1 - P_{S-ON})(P_{1/0}^{min}) \tag{3.13}$$

The minterm will be a faulty '1' if at least one of the 1st stage transistors is incorrectly switched-off. Thus,

$$P_{1/0}^{min} = 1 - (P_{ON/ON}^{T1})^n \tag{3.14}$$

The above probability of minterm faulty '0' can be calculated by using Equation 3.9. By substituting Equation 3.4 and 3.13 into Equation 3.12, the probability of occurrence of a faulty '0' can be written as,

$$\begin{aligned} P_{0/1}^{out} = {} & (P_{S-ON} + P_{1/0}^{min} - P_{S-ON} \times P_{1/0}^{min}) \\ & \times (1 - P_{0/1}^{min} + P_{S-ON} \times P_{0/1}^{min})^{m-1} \end{aligned} \tag{3.15}$$

By substituting Equation 3.7 and 3.14 into Equation 3.15, probability of faulty '0' at the output of a NASIC tile with no structural redundancy can be obtained

3.6 Tiles with Regular Structural Redundancy

In this section we will extend the analytical model to incorporate α-way Regular Structural Redundancy. An overview of structural redundancy has been provided in Chapter 1. For tractability of the model, we assume that horizontal nanowires have no logical dependencies between them.

The notation used for the probability of faulty output and minterm for a tile with α-way Regular Structural Redundancy is $P_{i/j}^{out-\propto w}$ and $P_{i/j}^{min-\propto w}$.

3.6.1 Occurrence of Faulty '1'

In tiles with structural redundancy, copies of are made of transistors on each nanowire and of the nanowires themselves. In a 2-way redundant tile for instance, every transistor will have a redundant copy in the same nanowire and every nanowire will be duplicated and logically merged with the next stage. Thus, in a 2-way redundant tile, twice as many transistors have to be correctly switched-on in order to produce a correct '0' at the output. Hence Equation 3.5 can be extended for the case of 2-way and α-way Regular Structural Redundancy as follows,

$$P_{1/0}^{out-2w} = 1 - (1 - P_{0/1}^{min-2w} + P_{S-ON} \times P_{0/1}^{min-2w})^{2m} \quad (3.16)$$

$$P_{1/0}^{out-\alpha w} = 1 - (1 - P_{0/1}^{min-\alpha w} + P_{S-ON} \times P_{0/1}^{min-\alpha w})^{\alpha m} \quad (3.17)$$

Note that the probability of a minterm being faulty '0' in a structurally redundant tile, $P_{0/1}^{min-\propto w}$, is not the same as the probability of a faulty '0' minterm in a non-redundant tile. This is because redundant copies of transistors are present on each horizontal nanowire gated by redundant copies of inputs. Thus, In order for a minterm faulty '0' to occur in 2-way structurally redundant tile for a specific input pattern, twice as many 1st stage transistors have to be incorrectly switched-on and twice as many transistors have to remain correctly switched-on compared to a non-redundant tile. Thus Equation 3.7 can be extended for a structurally redundant tile as follows,

$$P_{0/1}^{min-\alpha w} = \frac{1}{2^n - 1}\left[\left(P_{ON/OFF}^{T1}{}^{\alpha} + P_{ON/ON}^{T1}{}^{\alpha}\right)^n - P_{ON/ON}^{T1}{}^{\alpha n}\right] \quad (3.18)$$

Equations 3.8 and 3.9 remain valid for tiles with structural redundancy.

3.6.2 Occurrence of Faulty '0'

The probability of a faulty '0' for a structurally redundant tile can be extended from the non-redundant case in a similar manner as faulty '1'. Since there are α times the number of transistors in a α-way FSR compared to a non-redundant tile, the probability of a faulty '0' is,

$$P_{0/1}^{out-\alpha w} = P_{ON/ON}^{T2}{}^{\alpha(m-1)} \times P_{ON/OFF}^{T2}{}^{\alpha} \quad (3.19)$$

The expression for $P_{ON/OFF}^{T2}$ is the same as in Equation 3.13 except that the probability of a minterm being faulty '1' is different in the case of a structurally redundant tile since there are redundant transistors present in the horizontal nanowires.

$$P_{ON/OFF}^{T2} = P_{S-ON} + (1 - P_{S-ON})(P_{1/0}^{min-\alpha w}) \quad (3.20)$$

Since there are α times the number of transistors in the first stage horizontal nanowire of a α-way FSR compared to a non-redundant tile, the probability of minterm faulty '1' can be expressed as,

$$P_{1/0}^{min-\alpha w} = 1 - (P_{ON/ON}^{T1})^{\alpha n} \quad (3.21)$$

Similarly $P_{ON/ON}^{T2}$ for α-way FSR is similar to Equation 3.4 with the probability of faulty minterm being different,

$$P_{ON/ON}^{T2} = P_{S-ON} + (1 - P_{S-ON})(1 - P_{0/1}^{min-\alpha w}) \tag{3.22}$$

By substituting Equation 3.20 and 3.22 into Equation 3.19, the final expression for the probability of an output faulty '0' can be written as,

$$P_{0/1}^{out-\alpha w} = (P_{S-ON} + P_{1/0}^{min-\alpha w} - P_{S-ON} \times P_{1/0}^{min-\alpha w})^{\alpha} \times (1 - P_{0/1}^{min-\alpha w} + P_{S-ON} \times P_{0/1}^{min-\alpha w})^{\alpha(m-1)} \tag{3.23}$$

3.7 Summary

In this chapter, we have derived detailed analytical fault models for NASIC tiles with and without Regular Structural Redundancy, taking into consideration the defect scenarios, input faults, circuit and logic style of the fabric. These models will be used in the next Chapters to analyze the relative proportions of the probability of faulty '1's and '0's and discuss and introduce both modular redundancy and structural redundancy techniques for their mitigation.

CHAPTER 4

BIASED VOTING FOR IMPROVED SIGNAL RELIABILITY

4.1 Introduction

Modular redundancy techniques have been widely researched in the past few decades and include Triple modular redundancy (TMR) [29]-[32] and N-tuple modular redundancy [33]. Designs of new voter circuits [34][35] and even NMR systems without a centralized voter [36] have been proposed.

In modular redundancy techniques, identical replicas of modules are created whose outputs are then voted upon. For instance, in TMR, the outputs of three identical copies of a (non-redundant) module are fed into a majority voter. If, for example, at least two of the three modules produce logic ‘0’s, then the voter outputs a ‘0’. Otherwise, the voter outputs logic ‘1’. The inherent assumption that is made, when majority voters are employed, is that a ‘0’ to ‘1’ fault (faulty ‘1’) is as likely as a ‘1’ to ‘0’ fault (faulty ‘0’). In other words, it is assumed that defects within the computational fabric may cause faulty ‘0’s and faulty ‘1’s with equal probability. However, with nanoscale computation fabrics based on novel circuit and logic styles, and different defect scenarios due to unconventional manufacturing, this assumption may no longer be valid. One type of fault may be more frequent than another. This provides an opportunity to potentially achieve higher yields by using biased voters, i.e., by offering greater protection against the most likely faults and less against the others.

In this chapter, we use the analytical models derived in the previous chapter to analyze the proportions of the probability of output faulty ‘1’ and output faulty ‘0’ for a structurally non-redundant NASIC tile with non-faulty inputs. We show that for such a

tile the probability of output faulty ‘1’s is greater than the probability of output faulty ‘0’s. In other words, faulty ‘1’s are more likely to occur at the output of such a tile compared to faulty ‘0’s. Thus, we compare biased voters to traditional majority voting in such cases where the probabilities of faulty ‘0’s and faulty ‘1’s are unequal. We show that as the imbalance between the two fault probabilities is increased, the biased voting schemes become more effective. In section 4.3, we compare biased voting schemes to conventional majority voting schemes for general case without regard to any specific fabric. In section 4.4, we apply biased voting schemes to NASICs and analyze improvements in the reliability of outputs. Section 4.5 studies the effects on the results when the voters themselves are allowed to be defective. Section 4.6 summarizes the chapter.

4.2 Fault Probability Ratio

In order to study the relative proportions of the two types of faults for which probabilities were derived in the previous sections, we define a parameter called the Fault Probability Ratio (FPR). The Fault Probability Ratio is the ratio of the probability of a faulty ‘1’ to the probability of a faulty ‘0’. Thus,

$$FPR = P_{1/0}^{out} / P_{0/1}^{out} \qquad (4.1)$$

By substituting Equation 3.5 and Equation 3.15 into the above equation, the FPR can be calculated. From the equations derived in the previous sections it is evident that the FPR is a function of the defect probability, P_{S-ON}, the probability of input fault, $P_{i/j}^{inp}$,

the number of inputs of the logic function, n and the number of minterms, m. However, in this chapter the inputs to the tile are assumed to be non-faulty. Thus, $P_{0/1}^{inp} = P_{1/0}^{inp} = 0$.

Figure 4 shows the FPR of a structurally non-redundant NASIC tile with a fan-in of $n = 8$ for an increasing number of minterms (m) at three different defect rates. It is observed that the FPR rises with increasing number of minterms. This is expected since an increase in the number of transistors in the 2nd stage NAND gate makes faulty '0's less likely and faulty '1's more likely. A qualitative explanation for this is that a single transistor being incorrectly switched-off is sufficient to prevent the output node from discharging to '0'.

Furthermore, for a certain NASIC tile, the FPR is greater for a higher value of the defect rate, P_{S-ON}. For instance, the FPR is 8.1 for a tile with $n = 8$ and $m = 160$ at a defect rate of 5% and 18.22 for a defect rate of 15%. This can be better observed from Figure 5 that shows the FPR for a range of defect rates up to 15%. This trend occurs because as more transistors in the first NAND stage are stuck-on, the probability of the minterms carrying faulty '0's rises and thus there is an increased chance of a transistor in the second NAND stage gate being incorrectly switched-off and causing a faulty '1' at the output of the tile.

Defect rates of up to 15% are considered because any density advantage over CMOS is lost beyond this rate. In the plots of Figure 5, the average case (i.e., a symmetric function) was considered where the logic function implemented should produce (in the defect-free case) a '1' output for half of the 2^n input patterns and '0' for the remaining half. Hence, the number of minterms for such a logic function is, $m = 2^n - 1$.

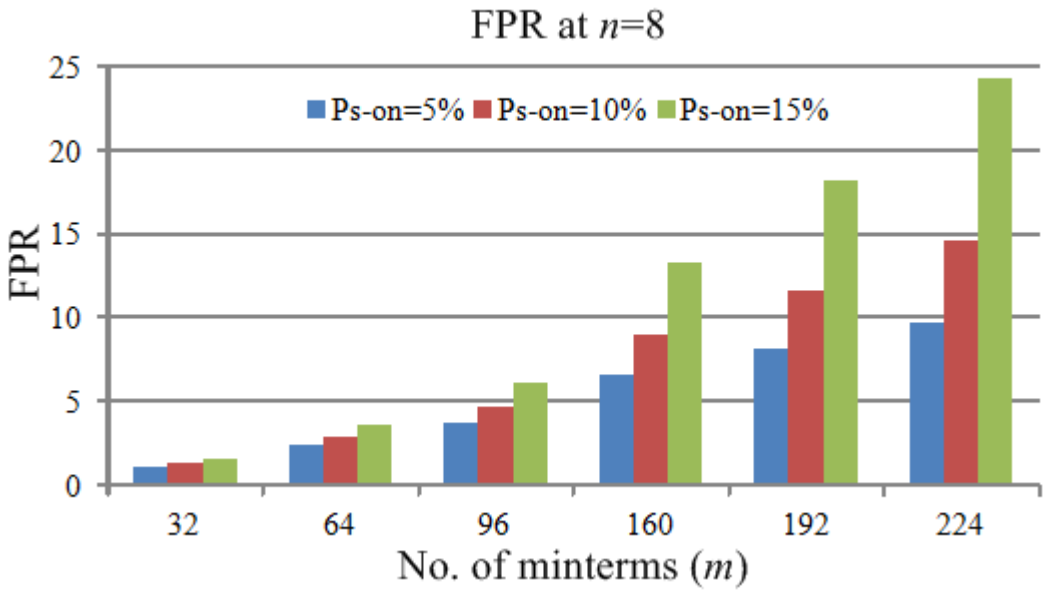


Figure 4. Fault Probability Ratio as a function of number of minterms for n=8 at defect rates of 5%, 10% and 15%

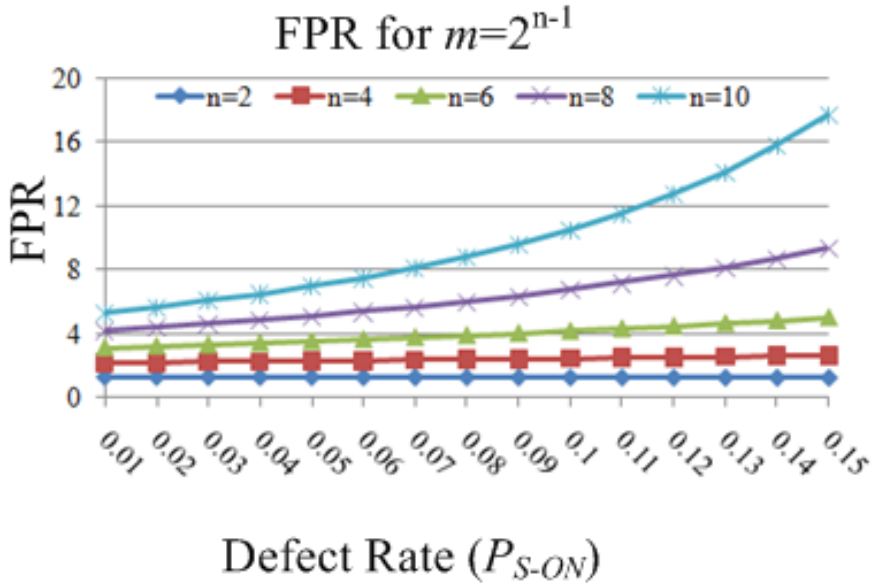


Figure 5. Fault Probability Ratio as a function of defect rate for a range of fan-in (n) when $m=2^{n-1}$

Figure 5 shows that although the FPR rises with the defect rate, the rate of increase is more marked for circuits with higher fan-in (n). Moreover, for a particular defect rate, the FPR is greater for circuits with higher fan-in. For instance, at a defect rate of 12%, a tile with a fan-in of 6 had an FPR of 4.5 whereas a tile with a fan-in of 10 had

an FPR of 12.7. This can be attributed largely to the increase in the number of minterms and thus increased chances of any one of them carrying a faulty ‘0’ and switching a 2nd stage NAND gate transistor incorrectly off.

4.3 Biased Voting in General Case

In this section, we compare biased voting schemes to conventional majority voting schemes for general case without regard to any specific fabric. Figure 6 shows a TMR and a biased voting configuration. The key difference between the two is the voting decision: in the first case (TMR) a majority voter is used to vote on three structurally non-redundant input modules whereas in the second, a voter biased towards a single logic ‘0’ is used. The notation used for this biased voter is V01/3 (voter biased towards logic ‘0’ that will produce logic ‘0’ even if only 1 out of the 3 inputs is ‘0’). A biased voter has a lower (higher) tolerance for the less (more) prevalent fault type. For instance, the V01/3 biased voter will not be able to tolerate any faulty ‘0’s but can tolerate up to two faulty ‘1’s.

Our objective is to find out whether the use of a biased voter instead of a conventional majority voter can enhance the expected yield of the voting configuration.

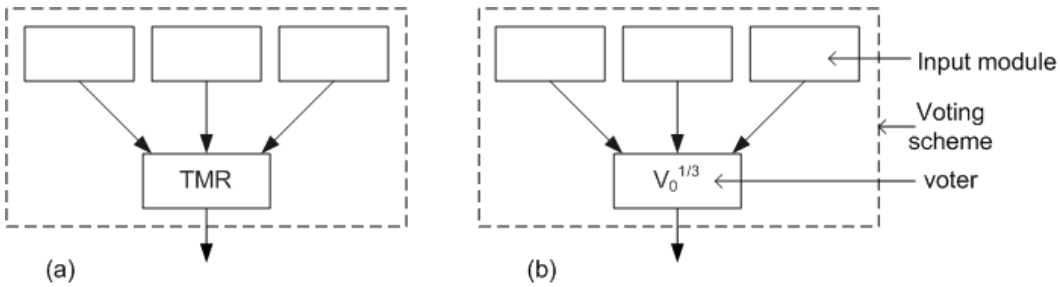


Figure 6. Voting configurations: (a) TMR majority voting, (b) $V_0^{1/3}$ biased voting

Yield is the probability that the circuit will produce a correct output in the presence of manufacturing defects. The two voting configurations (shown in Figure 6) use the same three non-redundant nano-modules. Thus, the difference in the probability of producing a correct output by the two circuits will be due to the different voting schemes. Such an accurate comparison between the two voting schemes and their corresponding voter designs can be achieved by using the Signal Reliability metric [43],[44].

To derive the probabilities of producing correct '0' and '1' outputs by the two voting configurations we use the notations shown in Table 2.

Table 2. Notations

Symbol	Description
V^C	Correct output from the **voting scheme** if it were to take inputs from defect-free input modules
V^A	Actual output from the voting scheme taking inputs from defective input modules
$P_{i/j}^{out} = P_{i/j}$	Conditional probability of getting a **input module** output of *i* given that the correct module output should have been *j* (*i*,*j*=0,1). Clearly,$P_{0/j}^{out}+P_{1/j}^{out}$=1, for j=0,1.
$P_{i/j}^{v}$	Conditional probability of getting a **voter** output of *i* given that the correct voter output should have been *j* (*i*,*j*=0,1) based on inputs to the voter. *i* may differ from j **only due to defects within the voter circuit**
$P_{i/j}^{TMR}$	Conditional probability of getting a TMR majority **voting scheme** output of *i* given that the correct output should have been *j* (*i*,*j*=0,1) based on inputs to the input modules. *i* may differ from *j* **due to defects within the voter circuit and/or defects in the input modules**
$P_{i/j}^{V01/3}$	Conditional probability of getting a $V_0^{1/3}$ biased **voting scheme** output of *i* given that the correct output should have been *j* (*i*,*j*=0,1) based on inputs to the input modules. *i* may differ from *j* **due to defects within the voter circuit and/or defects in the input modules**

SR	Signal Reliability: Probability of a correct output from a voter taking inputs from defective modules

As a preliminary study, faults in voters are not considered in this section to simplify the resulting expressions. However, section 4.5 discusses the changes in results when voters are prone to defects. Thus in this section, $P^{V}_{0/1} = P^{V}_{1/0} = 0$.

Assuming ideal voter circuits, a correct '0' ('1') will be produced by a TMR if all three inputs to the voter (from the modules) are correct '0's ('1's) or if any two of the inputs are correct '0's ('1's). The probabilities that a TMR generates correct '0's are,

$$P_{0/0}^{TMR} = Prob\{V_{TMR}^{A} = 0 \,|\, V_{TMR}^{C} = 0\} \tag{4.2}$$

$$P_{0/0}^{TMR} = (1 - P_{1/0})^3 + 3P_{1/0}(1 - P_{1/0})^2 \tag{4.3}$$

$$P_{0/0}^{TMR} = (P_{0/0})^3 + 3P_{1/0}(P_{0/0})^2 \tag{4.4}$$

The probabilities that a TMR generates correct '1's are,

$$P_{1/1}^{TMR} = Prob\{V_{TMR}^{A} = 1 \,|\, V_{TMR}^{C} = 1\} \tag{4.5}$$

$$P_{1/1}^{TMR} = (1 - P_{0/1})^3 + 3P_{0/1}(1 - P_{0/1})^2 \tag{4.6}$$

$$P_{1/1}^{TMR} = (P_{1/1})^3 + 3P_{0/1}(P_{1/1})^2 \tag{4.7}$$

Similarly, probability expressions for the V01/3 biased voter can be derived,

$$P_{0/0}^{V01/3} = Prob\{V_{V01/3}^{A} = 0 \,|\, V_{V01/3}^{C} = 0\} \tag{4.8}$$

$$P_{0/0}^{V01/3} = (1 - P_{1/0})^3 + 3P_{1/0}(1 - P_{1/0})^2 + 3{P_{1/0}}^2(1 - P_{1/0}) \tag{4.9}$$

$$P_{0/0}^{V01/3} = (P_{0/0})^3 + 3P_{1/0}(P_{0/0})^2 + 3{P_{1/0}}^2 P_{0/0} \tag{4.10}$$

$$P_{1/1}^{V01/3} = (1 - P_{0/1})^3 = {P_{1/1}}^3 \tag{4.11}$$

The values of $P_{i/j}^{TMR}$ and $P_{i/j}^{V01/3}$ are dependent on the defect rate, defect model and the circuit and logic styles of the nano-fabric considered.

The signal reliability of the voting scheme's output can be expressed as:

$$SR^{TMR} = [P_{0/0}^{TMR} \times P(V^C = 0)] + [P_{1/1}^{TMR} \times P(V^C = 1)] \tag{4.12}$$

$$SR^{V01/3} = [P_{0/0}^{V01/3} \times P(V^C = 0)] + [P_{1/1}^{V01/3} \times P(V^C = 1)] \tag{4.13}$$

The signal reliability expressions for the TMR and V01/3 can be obtained by substituting Equations 4.4 & 4.7 and 4.10 & 4.11 into Equation 4.12 and 4.13 respectively. Using a similar approach, the signal reliability for other majority and biased voting configurations can be found. It is evident from Equations 4.12 and 4.13 that the signal reliability not only depends on the probability of faulty '1's and '0's produced by the input modules but also on the number of input patterns that should correctly generate '0's $P(V^C = 0)$ and those that should correctly generate '1's $P(V^C = 1)$. Figure 7 shows the signal reliabilities for four different voting schemes over a range of Fault Probability Ratios (FPR), where the FPR is the ratio between the probability of a faulty '1' to the probability of a faulty '0' as defined in Equation 4.1. The $V_0^{2/5}$ biased voting scheme is biased towards 2 '0's out of the 5 inputs and the 5MR is a majority voting scheme voting on 5 redundant inputs. Figure 7 (a) and (b) show the signal reliability for $P_{0/1}$ values of 0.05 and 0.1, for a symmetric function where $P(V^C = 0) = P(V^C = 1) = 0.5$. However,

it is also possible for a logic function to be skewed towards '1' or '0' in terms of correct outputs. Figure 7 (c) and (d) show the signal reliabilities for the cases where $P(V^C = 1) = 0.75$ and $P(V^C = 0) = 0.25$, respectively.

As can be seen from Figure 7 (a) and (b), the biased voting schemes ($V_0^{1/3}$ and $V_0^{2/5}$) have a higher signal reliability compared to their corresponding majority voting schemes (TMR and 5MR, respectively) with increasing FPR. As the probability of a faulty '1' rises compared to that of a faulty '0', the voters biased to logic '0' will be more likely to produce a correct output. For example, in Figure 7 (b) where $P_{0/1}$ = 0.1 with $P(V^C = 0) = P(V^C = 1) = 0.5$, the $V_0^{2/5}$ scheme has 20% higher signal reliability than the 5MR majority scheme while the $V_0^{1/3}$ biased scheme has a 16% higher signal reliability than the TMR at FPR $= 7$.

The $V_0^{2/5}$ scheme exhibits higher signal reliability than 5MR for FPR ≥ 3, whereas for the $V_0^{1/3}$ scheme the benefits over TMR are achieved only for FPR > 4. This is due to the comparatively poor resilience of the latter scheme to faulty '0's, since a single faulty '0' causes diminished reliability in that scheme. In this case, the probability of generating correct '1's at the output of the voter is the dominating factor. On the other hand, for FPR > 7, the faulty '1' probability is much higher and the requirement for 2-out-of-5 '0's for the $V_0^{2/5}$ voter is harder to achieve. However in the case of the $V_0^{1/3}$ voter, a single correct '0' is sufficient to ensure a correct final output implying that the overall reliability is higher. The probability of generating correct '0's is the dominating factor in this scenario.

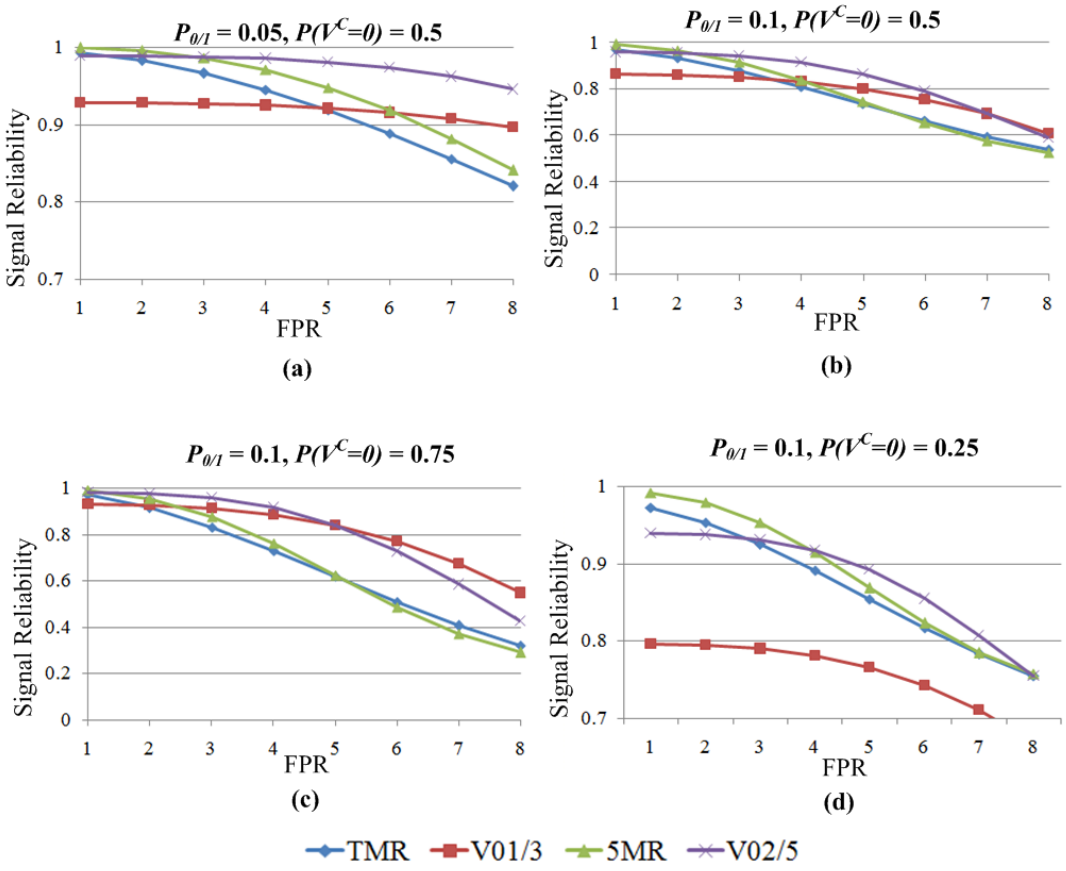


Figure 7. Signal reliability as a function of Fault Probability Ratio (FPR) for (a) $P_{0/1}$ *= 0.05,* $P(V^C=0)$ *= 0.5 and (b)* $P_{0/1}$ *=0.1,* $P(V^C=0)$ *= 0.5 (c)* $P_{0/1}$ *= 0.1,* $P(V^C=0)$ *= 0.75 and (d)* $P_{0/1}$ *= 0.1,* $P(V^C=0)$ *= 0.25*

In situations where $P(V^C = 0) > P(V^C = 1)$ such as the case shown in Figure 7, the frequency of occurrence of faulty '1's (0's) is further increased (reduced). At an FPR of 7, a 57% increase in reliability is attained by the $V_0^{2/5}$ scheme over the 5MR while a 66% increase in reliability is demonstrated by the $V_0^{1/3}$ scheme over the TMR. Figure 7 (d) shows the opposite case where $P(V^C = 0) < P(V^C = 1)$. Here the frequency of occurrence of faulty '1's is reduced while that of faulty '0's is increased. The $V_0^{2/5}$ scheme is still able to show a higher reliability from an FPR value of 4 up to 8. On the

other hand, the $V_0^{1/3}$ scheme shows low reliability because of its inability to tolerate even a single faulty '0'. This suggests that a higher reliability maybe attained by switching the bias of the voters from logic '0' to '1'. However, in nanoscale fabrics that implement two level logic styles, for functions where $P(V^C = 0) < P(V^C = 1)$, the complementary rather than the true output is likely to be implemented for reduced area. This again takes us back to the reverse case depicted in Figure 7 where the biased voters demonstrate significantly higher signal reliabilities.

To summarize, our analysis of biased and majority voting schemes has shown that as the ratio of faulty '1's to faulty '0's increases, biased voting configurations exhibit up to 66% higher signal reliability.

4.4 Biased Voting in NASICs

Section 4.2 showed that the rate of occurrence of faulty '1's is expected to be higher than that of faulty '0's in NASICs and section 4.3 demonstrated the improvement in signal reliability that can be gained by applying biased voters to fabrics that have unequal fault rates. It follows that applying biased voting schemes to NASICs will provide improved fault tolerance compared to conventional majority voters. In this section, we apply biased voting schemes to NASICs and compare them to conventional majority voting schemes.

In this section, the probability expressions for faulty '1's and faulty '0's derived in Chapter 3, are used to compare the signal reliabilities for circuits implemented with biased and majority voting schemes. Figure 8 shows the reliabilities for n-input NASIC circuits for the voting schemes introduced in the previous section.

As we have previously observed for a given defect rate, there is a minimum fan-in (n) before biased voting schemes show a higher reliability over majority voting schemes. Moreover, this required minimum value of fan-in decreases with increasing defect rates. For example, at a defect rate of 5%, the $V_0^{1/3}$ biased voting scheme has a greater reliability than the TMR scheme only for NASIC circuits with $n = 9$ or greater. However, at a defect rate of 15%, the $V_0^{1/3}$ scheme has a higher reliability even for circuits that have a fan-in of 6. This suggests that at the high defect rates that nanoscale fabrics are subject to, using biased voting schemes will provide a greater reliability even for circuits with low fan-in.

For a particular defect rate, the biased voting schemes give a higher reliability as the circuit fan-in increases due to the increasing FPR discussed in the previous section. For instance at 15% defect rate for tiles with fan-in of 10, the $V_0^{1/3}$ biased scheme has a 27% greater reliability compared to the TMR scheme while the $V_0^{2/5}$ biased scheme has 24% higher reliability than the 5MR scheme. At a defect rate of 10%, the $V_0^{2/5}$ exhibits 20% greater signal reliability and the $V_0^{1/3}$ exhibits 17% greater signal reliability for circuits with fan-in of 10. The reliability advantage will be even greater when $P(V^C = 0) \neq P(V^C = 1)$ as shown in section 4.3. This implies that biased voters could be employed at key architectural points in the design, specifically at the outputs of high fan-in stages, for greater yield, while carefully managing yield-area tradeoffs.

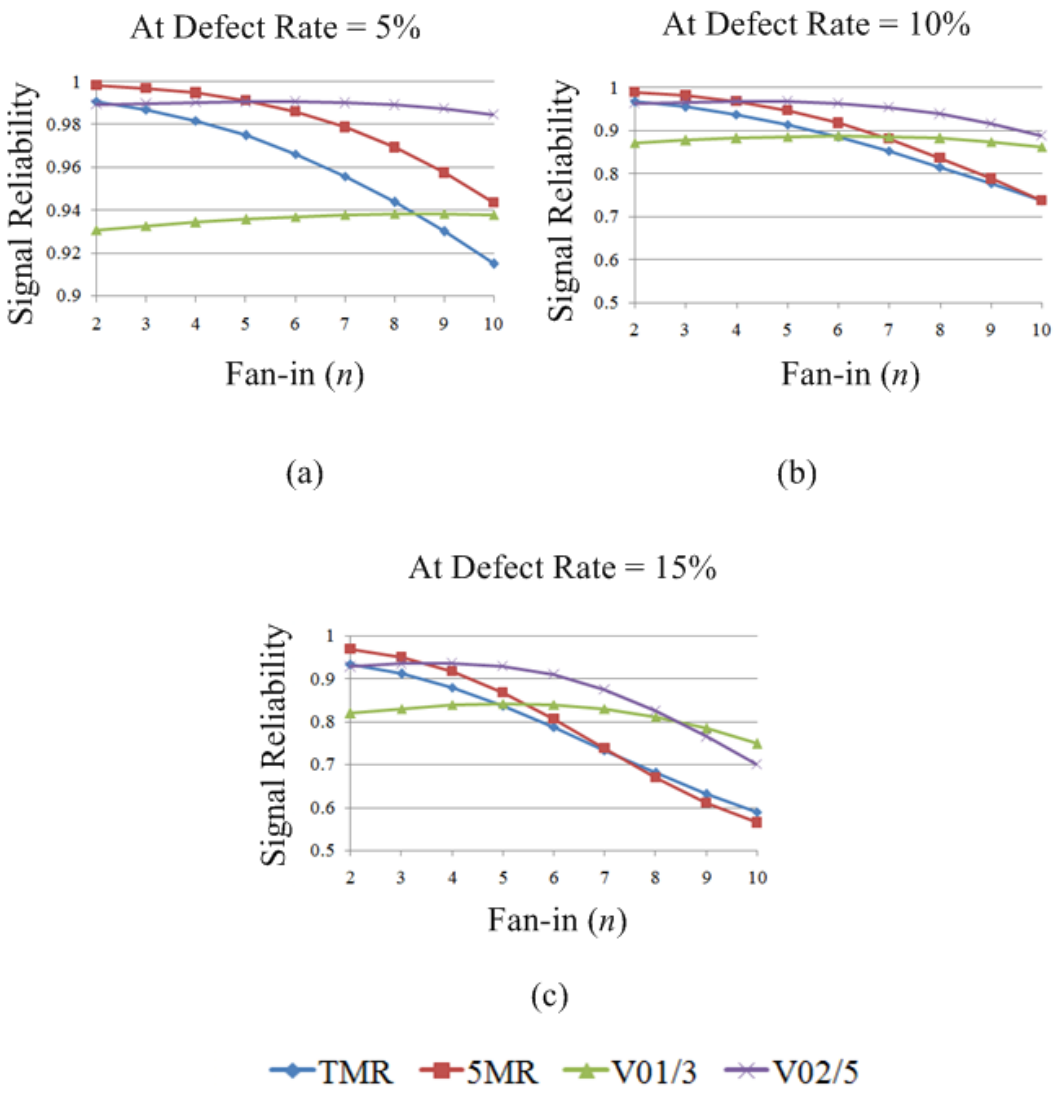


Figure 8. Signal Reliability comparison for biased and majority voting schemes at defect rates of: (a) 5%, (b) 10%, and (c) 15%

The biased voting schemes may also be more area efficient than majority voters or, at the worst case, consume the same area when implemented with 2-level logic such as used in the NASIC fabric. This is because the number of minterms for a biased voter will be less than or equal to the number of minterms for a majority voter with the same number of inputs. This implies that the effective yield (i.e., yield divided by the area increase factor) for biased voting schemes may be higher.

4.5 Voter Reliability

In the analysis done in the previous sections of this chapter, voters were assumed to be perfect. However, since the voters have to be implemented in the same nanoscale fabric, such as the $V_0^{2/4}$ biased voter shown in Figure 9 implemented in the NASICs fabric, they are also susceptible to manufacturing defects. Thus in a realistic scenario voter faults have to be taken into account. In this section, we analyze and compare signal reliabilities in voting schemes with voter defects. Notations that have been used in this section are described in Table 2.

A correct '0' ('1') will be produced by a TMR majority voting scheme if a majority of the input modules produce correct '0's ('1's) and the voter circuit itself produces a correct '0' ('1') or if a majority of the input modules produce incorrect '1's

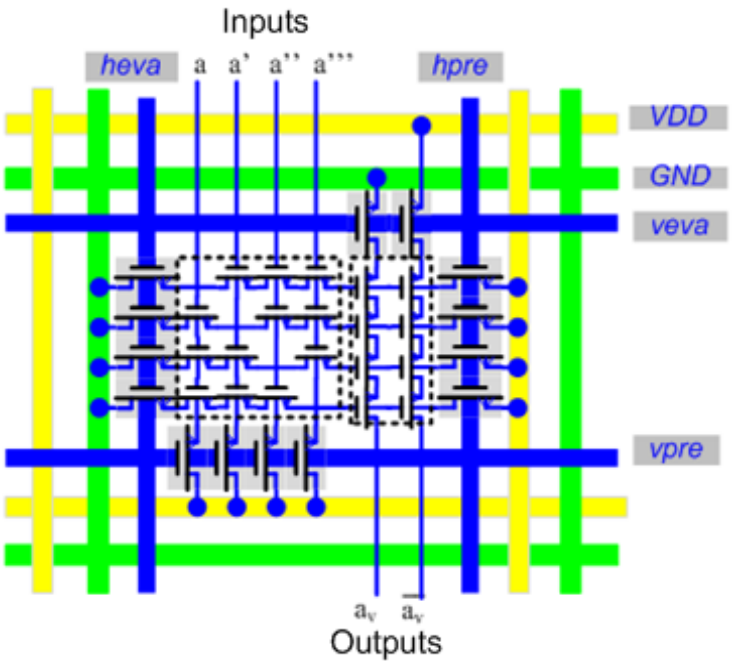


Figure 9. $V_0^{2/4}$ *biased voter in NASICs.*

('0's) and the voter circuit produces an incorrect '0' ('1'). The probabilities that this majority voting scheme generates correct '0's and '1's are,

$$P_{0/0}^{TMR} = P_{0/0}^{V}[(P_{0/0})^3 + 3P_{1/0}(P_{0/0})^2] + P_{0/1}^{V}[(P_{1/0})^3 + 3P_{0/0}(P_{1/0})^2]$$

$$P_{1/1}^{TMR} = P_{1/1}^{V}[(P_{1/1})^3 + 3P_{0/1}(P_{1/1})^2] + P_{1/0}^{V}[(P_{0/1})^3 + 3P_{1/1}(P_{0/1})^2]$$

Similarly, probability expressions for the $V_0^{1/3}$ biased voter can be derived,

$$P_{0/0}^{V01/3} = P_{0/0}^{V}[1 - (P_{1/0})^3] + P_{0/1}^{V}[(P_{1/0})^3]$$

$$P_{1/1}^{V01/3} = P_{1/1}^{V}[(P_{1/1})^3] + P_{1/0}^{V}[1 - (P_{1/1})^3]$$

The signal reliability of the TMR majority voting scheme and the $V_0^{1/3}$ biased voting scheme can be expressed as follows where $i = 0$ or 1:

$$SR^{TMR} = [P_{0/0}^{TMR} \times P_{i/0}^{TMR}] + [P_{1/1}^{TMR} \times P_{i/1}^{TMR}]$$

$$SR^{V01/3} = [P_{0/0}^{V01/3} \times P_{i/0}^{V01/3}] + [P_{1/1}^{V01/3} \times P_{i/1}^{V01/3}]$$

The signal reliability expressions for the TMR and $V_0^{1/3}$ can be obtained by substituting Equations 4.14 & 4.15 and 4.16 & 4.17 into Equations 4.18 and 4.19 respectively. The values for $P_{i/j} = P_{i/j}^{out}$ can be calculated based on the equations derived in Chapter 3.5 for NASICs.

The values for $P_{0/0}^{V}$ for the TMR and the $V_0^{1/3}$ biased voted can also be calculated in a similar manner and is determined by the fan-in and number of minterms in the voter circuit. For instance, a structurally non-redundant TMR voter would have a fan-in of 3

and 3 minterms and a $V_0^{1/3}$ would have the same fan-in but only one minterm since it will produce a '1' only when all three inputs to it are '1's.

Figure 10 shows the signal reliabilities for the same voting schemes that were considered in Figure 8 but with consideration of voter defects. As expected, the signal reliabilities overall decrease since the voters are now defective. It is interesting to note,

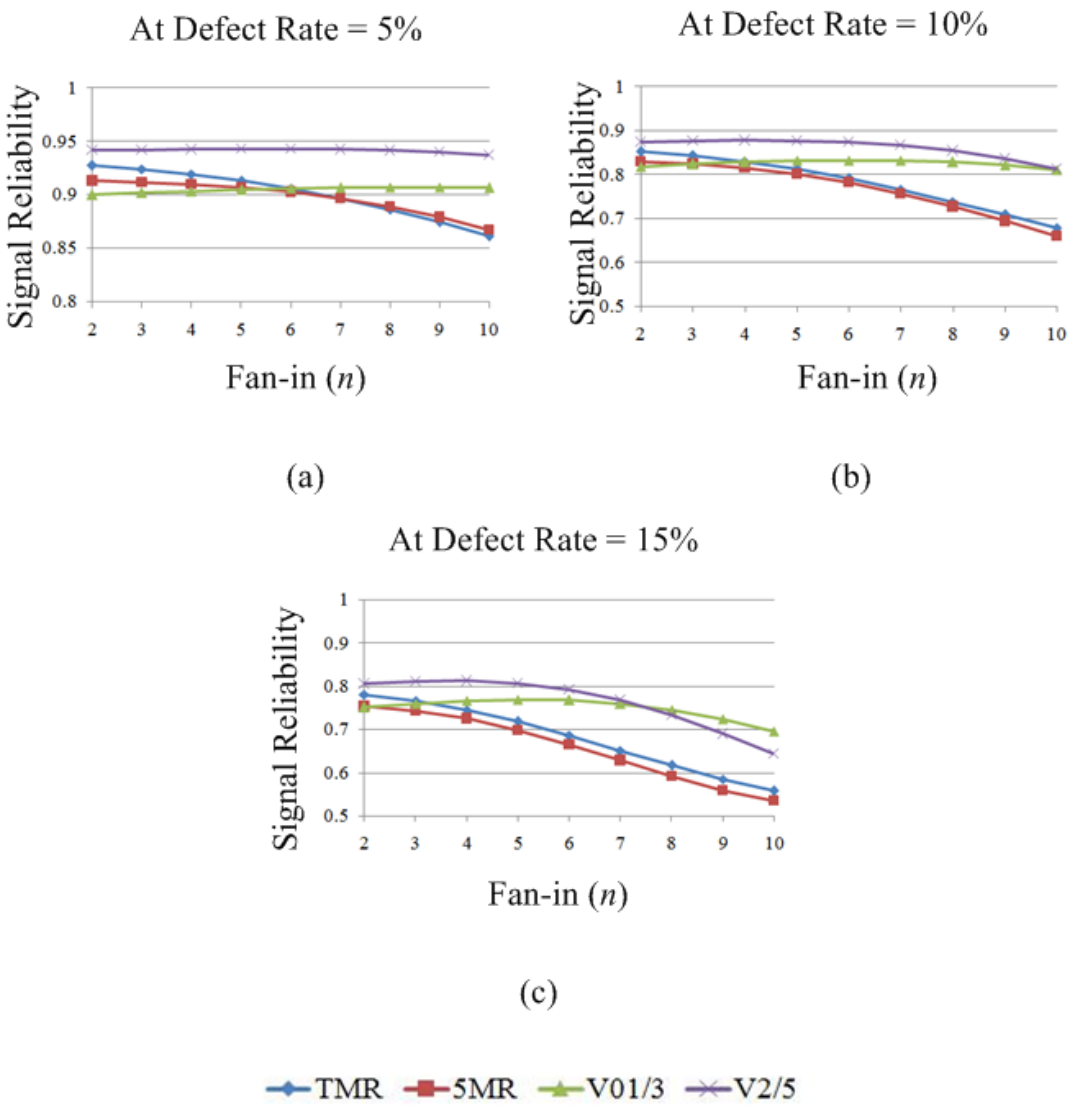


Figure 10. Signal Reliability comparison for biased and majority voting schemes after considering voter defects at defect rates of: (a) 5%, (b) 10%, and (c) 15%

however, that the biased schemes show an advantage over majority schemes much earlier on now. For instance at defect rate of 10% in Figure 10 (a) $V_0^{2/5}$ biased scheme now has greater signal reliability for circuits of any fan-in and the $V_0^{1/3}$ voter overtakes the TMR for circuits with fan-in greater than 4 as opposed to 6. This is because the biased voter circuits require fewer minterms than majority voter circuits and hence the number of transistors in the biased voter circuits is fewer. Thus they have a lower probability of being defective compared to majority voters which have larger circuits. On the same note, biased voters are expected to take lesser area than majority voters and thus provide greater signal reliability per unit area.

4.6 Summary

In this chapter we have shown that for structurally non-redundant NASIC tiles with non-faulty inputs, the probability of output faulty '1's can be as much as 12 times greater than the probability of output faulty '0's for a tile with a fan-in of 10. It was shown that this ratio can be even greater for circuits with a higher fan-in and at greater defect rates. We have shown that the application of biased voting schemes as compared to conventional majority voting schemes provided improved signal reliability in NASICs due to the inequality in fault rates. The biased voting schemes were shown to have as much as 27% greater signal reliability compared to conventional majority voting schemes. This advantage over majority voting schemes was shown to be retained when voter defects were considered.

CHAPTER 5

STRUCTURAL REDUNDANCY IN CASCADED NASICS

5.1 Introduction

In the previous chapters we utilized analytical models to analyze fault characteristics in non-cascaded and structurally non-redundant NASIC tiles with ideal inputs. To build larger systems, however, NASIC tiles will have to be cascaded. Hence, evaluation of the fault characteristics and improvement of the signal reliability through cascaded NASIC tiles is necessary. Furthermore, modular redundancy alone will not be sufficient to tolerate the high defect rates characteristic of nanoscale fabrics since multiple input modules may be faulty. Thus, structural redundancy needs to be incorporated in the tiles. In this chapter, we will study the propagation of faulty '1's and faulty '0's through cascades of structurally redundant NASIC tiles and their effect on the overall Signal Reliability. In our analysis, we demonstrate that the Signal Reliability through cascades of tiles with Regular Structural Redundancy rapidly drops after a few cascades due to an escalation of the probability of output faulty '0's. Having identified that tiles with Regular Structural Redundancy are intolerant of input faulty '0's, we propose and introduce a novel structural redundancy scheme called the Staggered Structural Redundancy (SSR) that offers improved resilience against input faulty '0's. We show that cascades of tiles with Staggered Structural Redundancy maintain high signal reliability for larger levels of cascades than were possible using Regular Structural Redundancy.

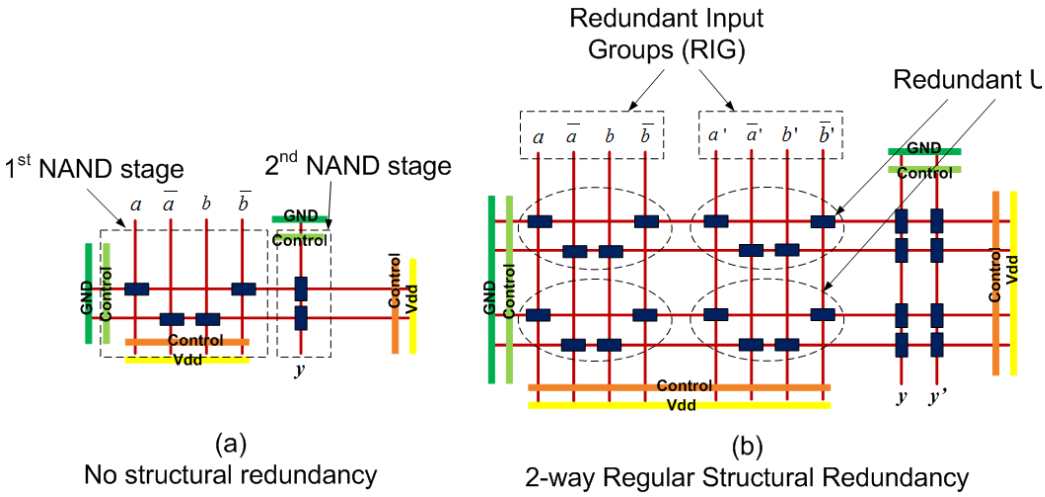


Figure 11: Regular Structural Redundancy schemes for a NASIC tile implementing a 2-input XOR logic function: (a) NASIC tile with no structural redundancy incorporated (b) NASIC tile with 2-way RSR

5.2 Regular Structural Redundancy

Figure 11 shows a 2-input XOR NASIC tile without structural redundancy and its implementation with 2-way and 3-way Regular Structural Redundancy. In the 2-way RSR shown in Figure 11 (b), each nanowire has two Redundant Units and there are four such Redundant Units in total in the first stage of the tile.

5.2.1 Fault Propagation along cascade

In this section we analyze the propagation of faulty '1' and faulty '0' through a cascade of NASIC tiles with Regular Structural Redundancy. Depending on the specific NASIC system, tiles may be cascaded differently. For instance, output signals from a tile may be input to multiple tiles at different levels of the cascade. We analyze the propagation of faults through one example of the cascade structure shown in Figure 12 (another example of Ripple Carry Adder is shown in Section 5.4). In this cascade

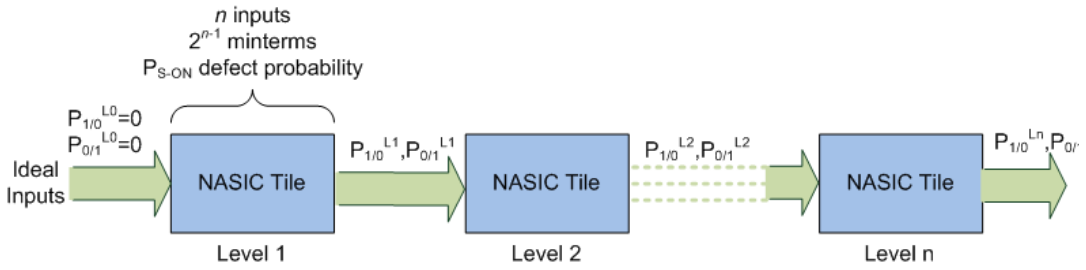


Figure 12: Cascade structure used to analyze propagation of faults

structure, there are n levels of cascade. Each tile in the cascade is assumed to have the same number of inputs and minterms. All the inputs of a tile in the cascade are assumed to have the same probability of being faulty and this is equal to the probability of output faults from the preceding tile in the cascade.

In order to analyze the propagation of faults through the cascade shown in Figure 12, we have used the analytical model derived in Chapter 3. The model determined the probability of output faulty '1' and '0' in terms of the probability of defects within the tile and the probability of input faults from the preceding tile. This model is used to calculate the probability of output faults after each level of the cascade using the values from the preceding tile as its probability of input faults. Inputs to the tile in Level 1 of the cascade are assumed to be fault-free.

Figure 13(a) shows the probability of output faults and the Signal Reliability (SR) at the output of each cascade level along a cascade of NASIC tiles with no structural redundancy (1w-RSR) and with tile specifications of n=4 and m=8 at a defect rate of 10%. The Signal Reliability (SR) is the probability of a correct output as was defined in Chapter 4. In our analysis we assume that output '0' and '1' are equally likely at the output of an ideal NASIC tile. Hence, the Signal Reliability is $SR = 0.5 \times (P_{1/0} + P_{0/1})$

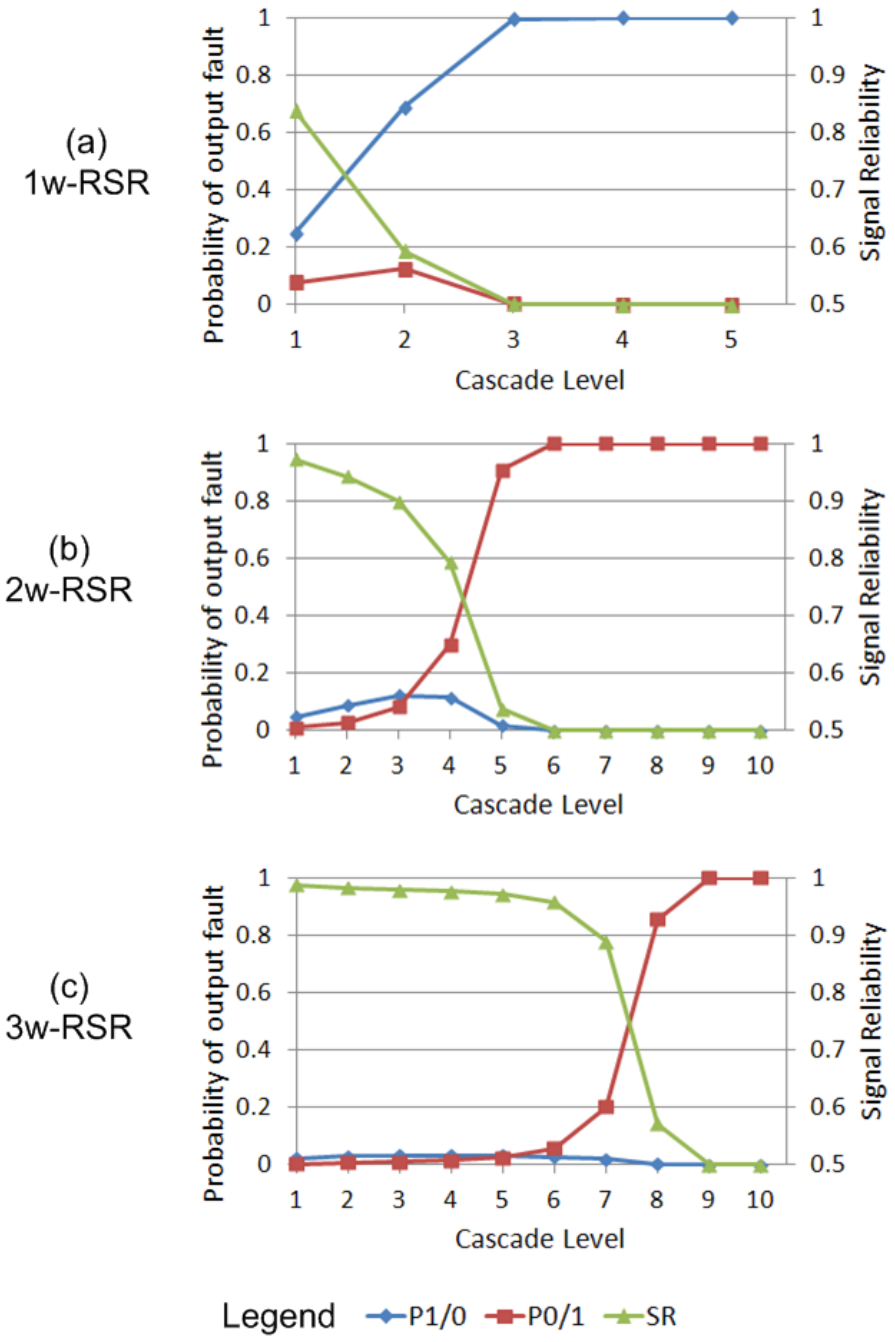


Figure 13: Probability of output faulty '0' and faulty '1' and Signal Reliability of cascaded tiles with n=4 and m=8 at 10% stuck-on probability for (a) tiles with no structural redundancy (b) with 1w-RSR and (c) with 2w-RSR

where $P_{1/0}$ and $P_{0/1}$ is the probability of output faulty '1' and faulty '0' respectively. Figure 13(a) shows that the probability of output faulty '1' is 0.24 after the first cascade level and the probability of output faulty '0' is 0.08. The Fault Probability Ratio is thus

greater than 1 and this is consistent with our analysis in Chapter 4.1. It can be seen from Figure 13(a) that the probability of faulty '1' increases along the cascade suppressing the probability of faulty '0'. This is because as the rate of input faulty '1's increases, transistors in the first NAND stage of a NASIC tile (such as the shown in Figure 11(a)) are incorrectly switched-on. This increases the rate of minterm faulty '0's causing transistors in the 2nd NAND stage to be incorrectly switched-off thus causing output faulty '1's. For the same reason, the rate of output faulty '0's are reduced. This can also be explained using the analytical models derived in Chapter 3. As $P_{1/0}^{inp}$ increases in Equation 3.8, $P_{ON/OFF}^{T1}$ increases and this causes $P_{0/1}^{min}$ to also increase in Equation 3.7. With that $P_{ON/ON}^{T2}$ reduces in Equation 3.4 finally causing $P_{1/0}^{out}$ in Equation 3.5 to increase and $P_{0/1}^{out}$ to decrease in Equation 3.12.

It can be seen from Figure 13(a) that after 3 levels of cascade, the probability of faulty '1' reaches 1 and the probability of faulty '0' reaches 0. This means that the output of the third cascade level will be stuck at logic '1'. The Signal Reliability is 0.5 because about half the time logic '1' is the correct value. Thus, clearly NASIC tiles cannot be cascaded without structural or modular redundancy since the faults will accumulate along the cascade.

Figure 13(b) shows the results for a cascade of the same tile specifications but implemented with 2-way Regular Structural Redundancy (2w-RSR). It can be seen that the Signal Reliability in this case drops to 0.5 much later in the cascade, i.e. after 6 levels, compared to the previous case. This is because every transistor has a redundant copy thus providing tolerance against stuck-on defects. However, it is interesting to observe that the reason for the drop in Signal Reliability in this cascade, is the escalation of probability of

output faulty ‘0’s instead of faulty ‘1’s, unlike the previous case. Although the probability of output faulty ‘0’ starts off with a lower value compared to the probability of output faulty ‘1’ after level 1 of the cascade, it quickly dominates and saturates to 1 after 6 levels of cascade. This leads us to conclude that tiles with Regular Structural Redundancy have reduced resilience against input faulty ‘0’s and improved resilience against input faulty ‘1’s compared to structurally non-redundant tiles. Hence, if the resilience against input faulty ‘0’s from preceding tiles could be improved alongside tolerating stuck-on defects within the structurally redundant tile, then Signal Reliability can be further improved, enabling larger cascades.

We have identified two factors that cause diminished resilience against input faulty ‘0’ in tiles with Regular Structural Redundancy. Firstly, for tiles with RSR the probability of the minterm being faulty ‘1’ is greater. This is due to the fact that a single incorrectly switched-off transistor in a horizontal nanowire (induced by an input faulty

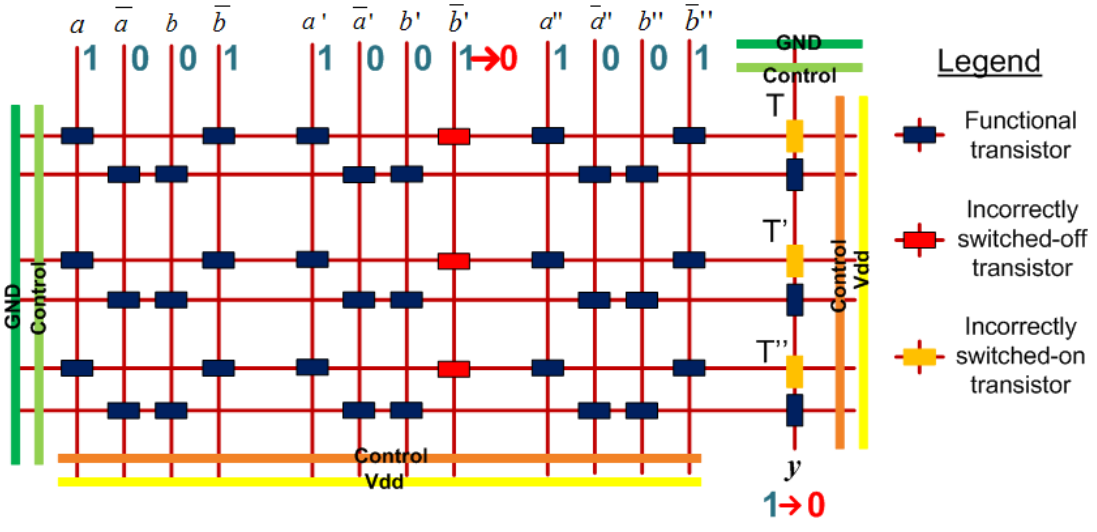


Figure 14: 3w-RSR tile demonstrating diminished resilience to input faulty '0'

‘0’) is sufficient to cause the minterm to be faulty ‘1’ and furthermore, the number of transistors in the horizontal nanowire is multiplied due to redundancy. For instance, a 3w-RSR tile has three times the number of transistors in each horizontal nanowire compared to a non-redundant tile. Secondly, logical dependencies exist between redundant copies of horizontal nanowires because they are gated by the same input signals. Thus, a faulty ‘0’ input may cause all redundant copies of a horizontal nanowire to produce faulty minterm ‘1’s leading to faulty output ‘0’ at the vertical nanowire. Figure 14 shows the 3w-RSR tile from Figure 11(c) this time with inputs. The correct inputs to the tile (shown in green) are $a = 1$ and $b = 0$ which in an ideal scenario would produce an output $y = 1$. However if any of the input ‘1’s become a faulty ‘0’, such as $\overline{b'}$ shown in the figure, then the relevant transistors in all three horizontal nanowires are incorrectly switched-off. In the example shown in Figure 14, this causes all the three transistors shown in yellow in the vertical nanowire to be incorrectly switched-on resulting in a faulty ‘0’ at the output. In section 5.3 we propose a novel structural redundancy scheme that circumvents this problem to improve resilience against input faulty ‘0’s while tolerating stuck-on defects.

5.2.2 Resilience to Input Faults

In this section, we study the resilience of the 3w-RSR scheme against input faulty '0's. Figure 15(a) shows a 4-input NASIC tile with ideal input '1's and faulty '0's with a probability of $P_{0/1}^{inp}$. Figure 15(b) shows the probability of output faulty '1's and '0's as the probability of input faulty '0' varies from 0 to 0.5. The results were obtained using the analytical fault models from Chapter 3. When $P_{0/1}^{inp} = 0$, the probability of output faults for 1w-RSR is the greatest because it does not have any redundancy against the stuck-on defects. The probability of output faulty '1's is greater than faulty '0's due to the reasons stated in Chapter 4. As the probability of input faulty '0's increases, probability of output faulty '0's for the 3w-RSR becomes greater than the 2w-RSR and the 1w-RSR.

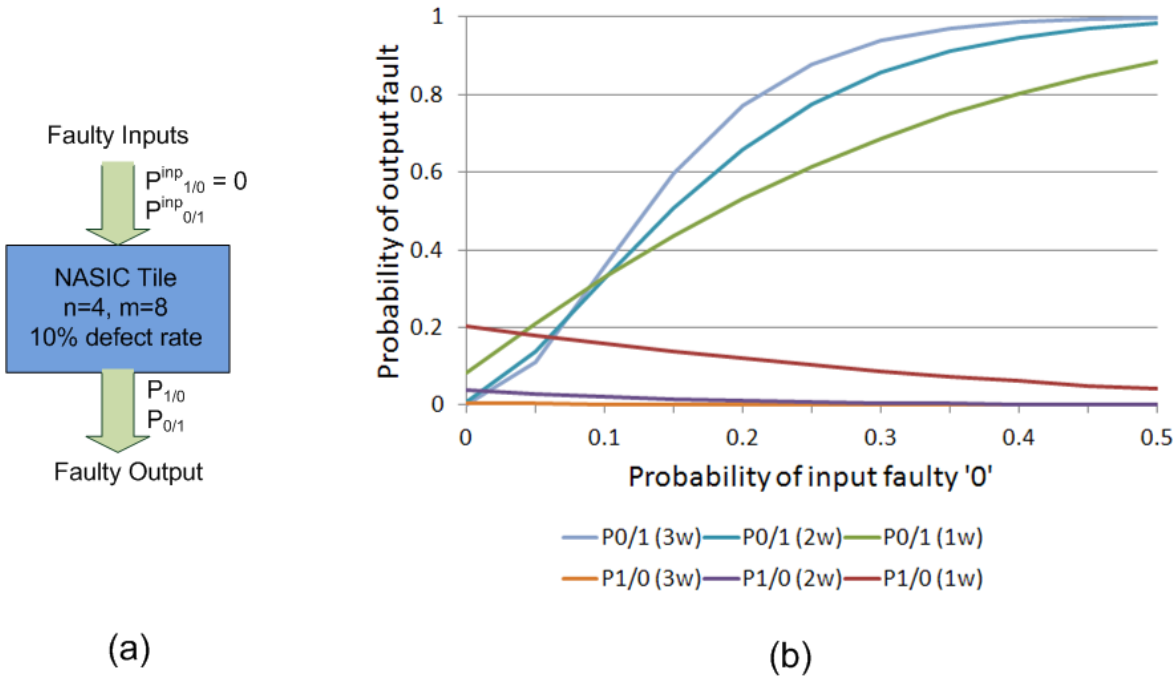


Figure 15: Resilience to input faulty '0' by non-redundant tile, 2w-RSR and 3w-RSR for n=4, m=8. (a) 4-input tile with 10% defect rate and with faulty input '0's. (b) Probability of output faults as a function of probability of input faulty '0's

This is because the 3w-RSR has three times the number of input signals due to redundancy compared to the non-redundant signal coupled with the fact that a single input faulty ‘0’ may cause an output faulty ‘0’ as explained in the preceding section.

5.3 Staggered Structural Redundancy

5.3.1 Introduction

Having identified the rapid escalation of faulty ‘0’s along the cascade of tiles with Regular Structural Redundancy, the goal in designing the new Staggered Structural Redundancy is to increase tolerance against input faulty ‘0’s. This will delay or even avoid the ‘avalanche’ of faulty ‘0’s making larger cascades feasible. In Staggered Structural Redundancy (SSR), we propose to selectively remove certain redundant units from the corresponding Regular Structural Redundancy such that each Redundant Input Group (RIG) does not gate transistors on all 3 redundant copies of each horizontal nanowire. Figure 16 shows one example of the Staggered Structural Redundancy, the (3,2)-SSR. It is so named because it has 3 RIGs and each horizontal nanowire is 2-way redundant. The (3,2)-SSR is more resilient against input faulty ‘0’ compared to the 3w-RSR in Figure 14. For instance, if the same input, $\overline{b'}$, is faulty ‘0’, transistor T′ in the vertically nanowire is not affected and is correctly switched-off to produce the correct output of ‘1’. Thus, assuming no defects, the (3,2)-SSR tile is guaranteed to tolerate at least a single input faulty ‘0’ whereas the 3w-RSR in Figure 14 was unable to tolerate even a single input faulty ‘0’. On the other hand, the (3,2)-SSR has reduced tolerance to stuck-on defects compared to compared to the 3w-RSR since each horizontal nanowire is

now 2way redundant instead of 3way. Thus, at very high defect rates the (3,2)-SSR will show reduced advantage over the 3w-RSR and this is discussed in Section 5.3.5.

5.3.2 Criteria and Notation

In order to define criteria for the Staggered Structural Redundancy schemes, we first define matrix notations for the schemes that relates to the presence or absence of Redundant Units in the first NAND stage of the tile. In the m × m square matrix, 1 indicates the presence of Redundant Units of transistors and 0 indicates absence. Thus, the matrix notation for the 3w-RSR shown in Figure 14 will be 3×3 square matrix with all elements as 1.

The criteria that needs to be fulfilled by the Staggered Structural Redundancy scheme to achieve improved resilience to input faulty ‘0’s without considerable loss of tolerance of stuck-on defects are as follows:

- At least a single 0 and at least a single 1 in each column of the matrix notation for

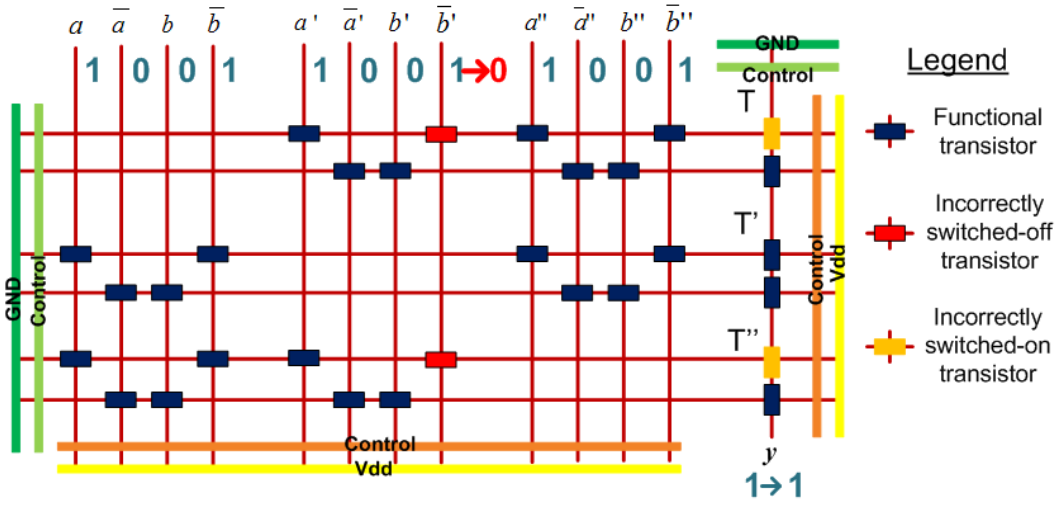


Figure 16. (3,2) staggered structural redundancy of 2-input XOR gate in NASICs

the staggered structural redundancy.

- An equal number of 1s and an equal number of 0s in each column of the matrix notation.

The above two criteria ensure that at least a single input faulty '0' is tolerated by a tile assuming the tile itself is defect-free. Furthermore, it ensures that all horizontal nanowires are equally redundant. The presence of a lesser redundant nanowire in the tile could make the whole tile susceptible to stuck-on defects or input faulty '1's. Note that for each SSR scheme there may be more than one possible matrix notation. However, in terms of logic implementation and input fault tolerance, the different matrix notations will have the same effect. Table 3 shows the matrix notations of 3w-RSR and two possible SSR schemes with the same number of Redundant Input Groups, the (3,2)-SSR and the (3,1)-SSR.

Table 3: Matrix notation of structural redundancy schemes

Structural Redundancy Type	Possible Matrix Notation
3w-RSR:	$\begin{bmatrix}1 & 1 & 1\\1 & 1 & 1\\1 & 1 & 1\end{bmatrix}$
(3,2)-SSR:	$\begin{bmatrix}0 & 1 & 1\\1 & 0 & 1\\1 & 1 & 0\end{bmatrix}$
(3,1)-SSR	$\begin{bmatrix}0 & 0 & 1\\1 & 0 & 0\\0 & 1 & 0\end{bmatrix}$

The (3,1)-SSR scheme has three Redundant Input Groups and each horizontal nanowire in the tile is 1way redundant. In other words, there are no redundant transistors

presents. Thus, although the tile would be more tolerant of input faulty ‘0’s, it is more susceptible to stuck-on defects and input faulty ‘1’s compared to the (3,2)-SSR.

5.3.3 Simulation Framework

The analytical models derived in Chapter 3 did not take into account logical dependencies between horizontal nanowires in order to keep the models tractable. Thus to achieve more accurate comparisons of the fault tolerance of the Staggered Structural Redundancy and the Regular Structural Redundancy schemes, Monte Carlo simulations have been used. The simulator first creates a faulty tile by mapping stuck-on defects on the ideal tile based on the probability of stuck-on defects. It then generates an input pattern from a set of all possible input patterns with uniform distribution. Faulty input patterns are created by flipping the bits based on the probability of input faulty ‘1’ and faulty ‘0’. The ideal inputs are fed into the defect-free tile and faulty inputs are fed into the faulty tile and the outputs are compared. Based on the comparison results of 100,000 such iterations the probability of output faults and the Signal Reliability are computed.

5.3.4 Resilience to Input Faults

Figure 17 compares the resilience to input faulty ‘0’ offered by the 3way Regular Structural Redundancy and the (3,2) Staggered Structural Redundancy schemes. Figure 17(a) shows the NASIC tile simulated for this purpose which is a 4-input tile implementing the XOR function. Simulations were carried out for the 3w-RSR and the (3,2)-RSR schemes with a 10% defect rate, probability of input faulty ‘1’ as 0 and varying the probability of input faulty ‘0’ from 0 to 0.4. Figure 17(b) shows the probability of output faulty ‘1’ and the probability of output faulty ‘0’ for the two

schemes. The probability of output faulty ‘0’ increases and the probability of output faulty ‘1’ decreases or stays at 0 for both schemes with increasing probability of input faulty ‘0’. This is because input faulty ‘0’s cause minterms to be faulty ‘1’s which in turn causes output faulty ‘0’s. Also, the presence of input faulty ‘0’s may mask the effect of stuck-on transistors in the horizontal nanowires and avoid minterm faulty ‘0’s, thus reducing the probability of output faulty ‘1’s. This can be explained using the analytical

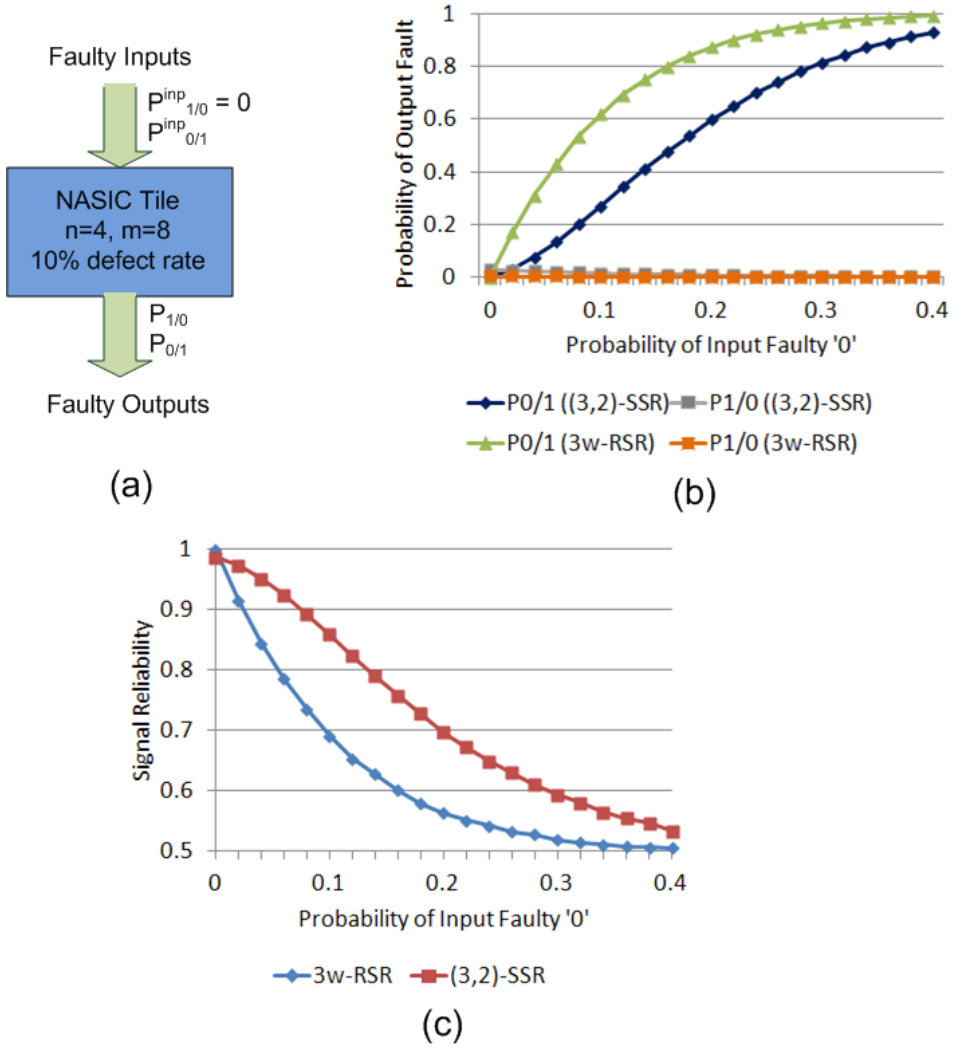


Figure 17: Resilience to input faulty '0' by 3w-RSR and (3,2)-SSR for n=4, m=8. (a) 4-input XOR tile with 10% defect rate and with faulty input ‘0’s. (b) Probability of output faults for the two schemes (c) Signal Reliability for the two schemes

models just as was done for input faulty ‘1’s in Section 5.3.1.

From Figure 17(b) it can be seen that the probability of output faulty ‘0’ in the (3,2)-SSR is lower than that of the 3w-RSR. For instance, at a probability of input faulty ‘0’ of 0.1, the probability of output faulty ‘0’ for the 3w-RSR is 0.62 and that for the (3,2)-SSR is 0.27 representing a 56% improvement over the 3w-RSR. This is because in the (3,2)-SSR scheme, a single faulty ‘0’ does not affect all the redundant horizontal nanowires due to the absence of Redundant Units as shown in Figure 16. As a result, at least one transistor in the corresponding vertical nanowire will be correctly switched-off (if it is not defective) and prevent an output faulty ‘0’. On the other hand, in the 3w-RSR, a single faulty ‘0’ may affect cause all transistors in the corresponding vertical nanowire to switch-on, leading to an output faulty ‘0’. It can also be seen that the probability of output faulty ‘1’ of the (3,2)-SSR is slightly higher compared to the 3w-RSR at low probability of input faulty ‘0’s. This is because in the (3,2)-SSR each horizontal nanowire is 2way redundant whereas in the 3w-RSR they are 3way redundant. Hence (3,2)-SSR has reduced tolerance to stuck-on defects and to input faulty ‘1’s which may cause the minterm to be faulty ‘0’ leading to output faulty ‘1’s. However, having identified the rapid escalation of faulty ‘0’s along a cascade of 3w-RSR, the benefits of increased tolerance to input faulty ‘0’ by the (3,2)-SSR is expected to outweigh the reduced tolerance to stuck-on defects and input faulty ‘1’s at low enough defect rates along the cascade.

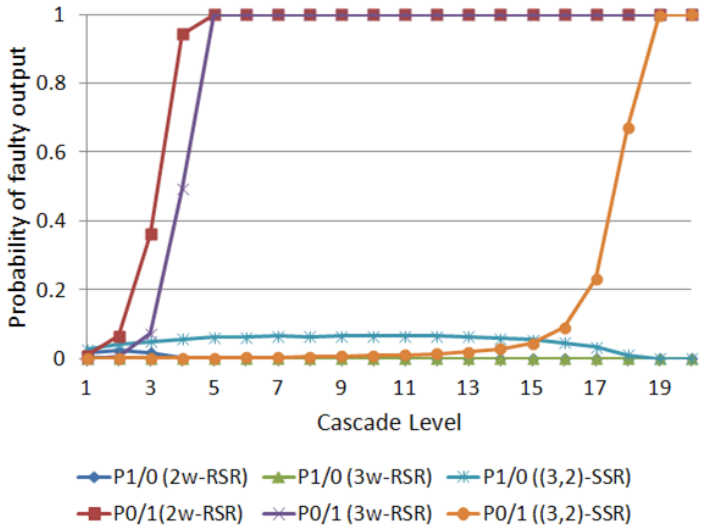
Figure 17(c) shows the overall Signal Reliability of the output of the two redundancy schemes. It can be seen that the Signal Reliability of the (3,2)-SSR is greater than that of the 3w-RSR at a particular probability of input faulty ‘0’. For instance, at a

probability of input faulty ‘0’ of 0.1, the Signal Reliability of the (3,2)-SSR is 0.86 whereas that of the 3w-RSR is 0.69 representing a 24% increase in Signal Reliability compared to the 3w-RSR. This increase in Signal Reliability is dominated by the reduced probability of output faulty ‘0’ of the (3,2)-SSR.

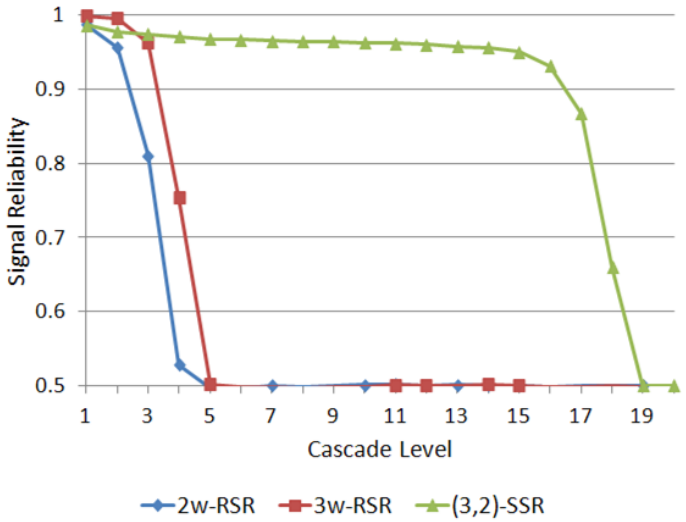
5.3.5 Fault Propagation along cascade

Figure 18 shows the fault probabilities and Signal Reliability at each level of the cascade shown in Figure 12 for 2w-RSR, 3w-RSR and (3,2)-SSR. Each NASIC tile is simulated using the simulation framework described in Section 5.3.3 with the output fault probabilities of one tile being the input fault probabilities for the tile in the next cascade level.

Figure 18(a) shows the probability of output faulty ‘1’ and ‘0’ for the three schemes at 10% defect rate. It can be seen that the probability of output faulty ‘0’ for the 2w-RSR and 3w-RSR rises rapidly after the 2^{nd} and 3^{rd} cascade level, respectively, whereas the escalation of output faulty ‘0’s in the (3,2)-SSR is delayed until the 17th level thus marking a significant improvement. On the other hand, the probability of output faulty ‘1’ is slightly higher for the (3,2)-SSR due to its reduced tolerance to input faulty ‘1’s and susceptibility to stuck-on defects compared to corresponding RSR schemes. Figure 18(b) shows the overall Signal Reliability for the three schemes. The trends are seen to be strongly dominated by the probability of output faulty ‘0’s as expected. The Signal Reliability for the 3w-RSR is better compared to the (3,2)-SSR before the 3rd cascade level, because during those initial cascades, the Signal Reliability is dominated by the output faulty ‘1’s since the probability of output ‘0’s is still low.



(a)



(b)

Figure 18:(a)Probability of output faults and (b) Signal Reliability along cascade of tiles with n=4 and m=8 at 10% defect rate

Figure 19(a) and (b) shows the Signal Reliabilities for the three schemes at 5% and 10% defect rates, respectively.

It can be seen from Figure 19(a) that the Signal Reliability of the (3,2)-SSR is nearly 1 for at least 15 cascades whereas the Signal Reliability of the 2w-RSR and the

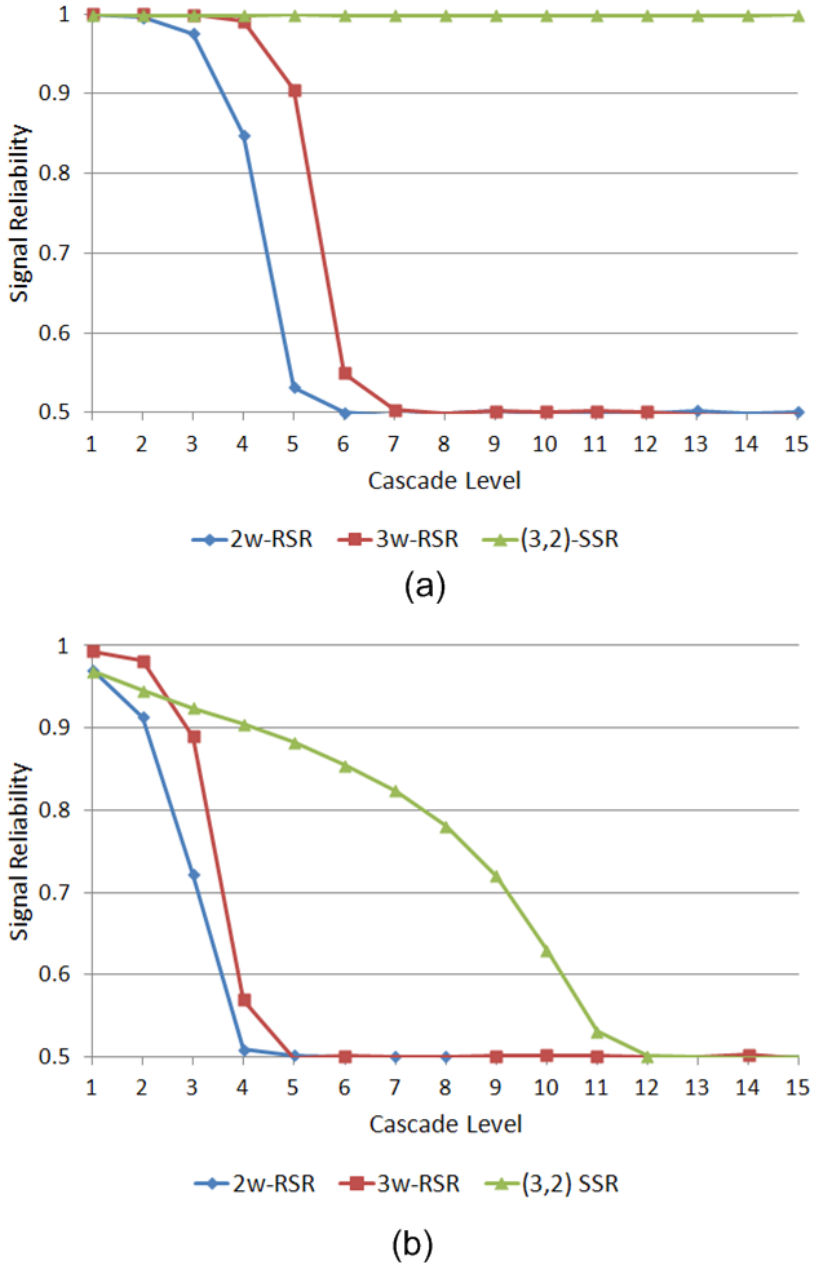


Figure 19: Signal Reliability along cascade of 2w-RSR, 3w-RSR and (3,2)-SSR for tiles with n=4, m=8 and at (a) 5% defect rate and (b) 15% defect rate

3w-RSR drop to 0.5 after 6 and 7 cascade levels, respectively. In fact, the Signal Reliability of the (3,2)-SSR have been found to be over 0.98 for more than 100 cascade levels. This is because the output faulty '1's and '0's that are produced by a (3,2)-SSR tile at 5% defect rate, is effectively tolerated by the next tile in the cascade avoiding

magnification of fault probabilities. As a result an 'avalanche' of faults is avoided keeping the Signal Reliability above 0.98 for a significantly large number of cascade levels.

Table 4 lists the cascade levels at which the Signal Reliability drops to 0.5 for the 2w-RSR, 3w-RSR and (3,2)-SSR schemes at different defect rates up to 15%. For defect rates below 8%, the Signal Reliability of the (3,2)-SSR scheme does not drop below 0.98 for at least 100 levels of cascade. The maximum cascade level with Signal Reliability above 0.5 for the (3,2)-SSR starts decreasing rapidly for increasing defect rates above 8%. This is because more transistors in the 2nd NAND stage of the tile are stuck-on leading to output faulty '0's thus causing an 'avalanche' much earlier on in the cascade. It is interesting to note that at 15% defect rate, the gradual fall of the Signal Reliability of the (3,2)-SSR shown in Figure 19(b) is due to a gradual rise in output faulty '1's. This occurs because each horizontal nanowire in the (3,2)-SSR is 2way redundant thus producing more output faulty '1's. The increased number of output faulty '1's mask output faulty '0's and eventually dominate.

Table 4: Cascade level after which Signal Reliability is 0.5

	Defect Rates				
	3%	5%	8%	10%	15%
2w-RSR	6	6	5	4	4
3w-RSR	7	7	6	5	5
(3,2)-SSR	>100	>100	75	20	12

5.4 Example: Ripple Carry Adder

In this section, we compare the degradation of the Signal Reliability of the carry signal through a 16-bit ripple carry adder implemented with 3w-RSR and (3,2)-SSR.

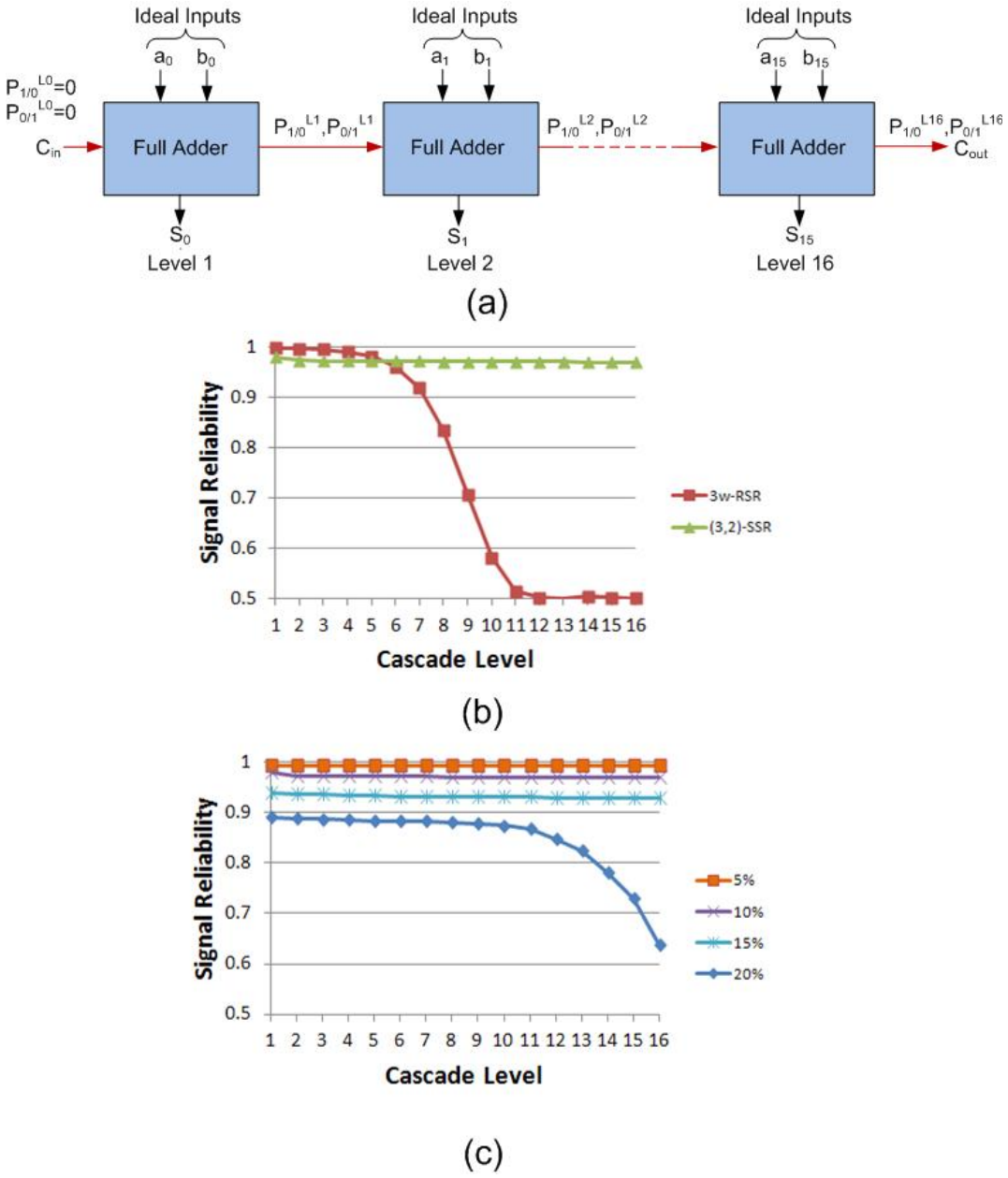


Figure 20: (a) 16-bit Ripple carry adder with ideal inputs and faulty carry signal. (b) Signal Reliability of carry signal at each cascade level for 3w-RSR and (3,2)-SSR at 10% defect rate (b) Signal Reliability of the (3,2)-SSR at 5%, 10% , 15% and 20% defect rates

Figure 20(a) shows the 16-bit ripple carry adder with ideal inputs and C_{in} to the first tile in the cascade. The reliability of the carry signal degrades through the cascade. Figure 20(b) shows the signal reliability of the carry signal at the output of each cascade level

for the implementations, 3w-RSR and (3,2)-SSR, at 10% defect rate. The signal reliability of the carry signal in the 3w-RSR implementation drops to 0.5 after 11 cascades levels. However, the signal reliability of the carry out signal at the end of the 16 cascade levels in the (3,2)-SSR implementation is 0.97, marking a significant improvement over the 3w-RSR scheme. Figure 20(c) shows the signal reliability of the carry signal in the (3,2)-SSR implementation at 5%, 10%, 15% and 20% defect rates. The signal reliability of the carry signal after 16 levels of cascade are 0.99, 0.97, 0.94 and 0.64 respectively. The signal reliability is lower with higher defect rates because the probability of faulty '1's increases with increasing probability of stuck-on transistors as was shown in Chapter 3.

5.5 Example: Cascade of 2-bit Comparators

In this section, we compare the Signal Reliabilities of signals in RSR and SSR implementations through a cascade of 2-bit comparators whose output is the maximum of two 2-bit numbers. Such a cascade of 16 levels is shown in Figure 21(a). Figure 21(b) shows the Signal Reliability of each of the two bits propagating along the cascade for 3w-RSR and (3,2)-SSR implementations at 5% defect rate. It can be seen that the Signal Reliabilities in the 3w-RSR implementation drops to their minimum value after 7 levels of cascade. After 7 levels of cascade, the output signals are all '0's. The minimum values are different for the two bits because the number of minterms is different and thus the probability that '0' is the correct output signal is different for the two bits. The Signal Reliabilities of the (3,2)-SSR scheme remain above 0.98 after 16 levels of cascade.

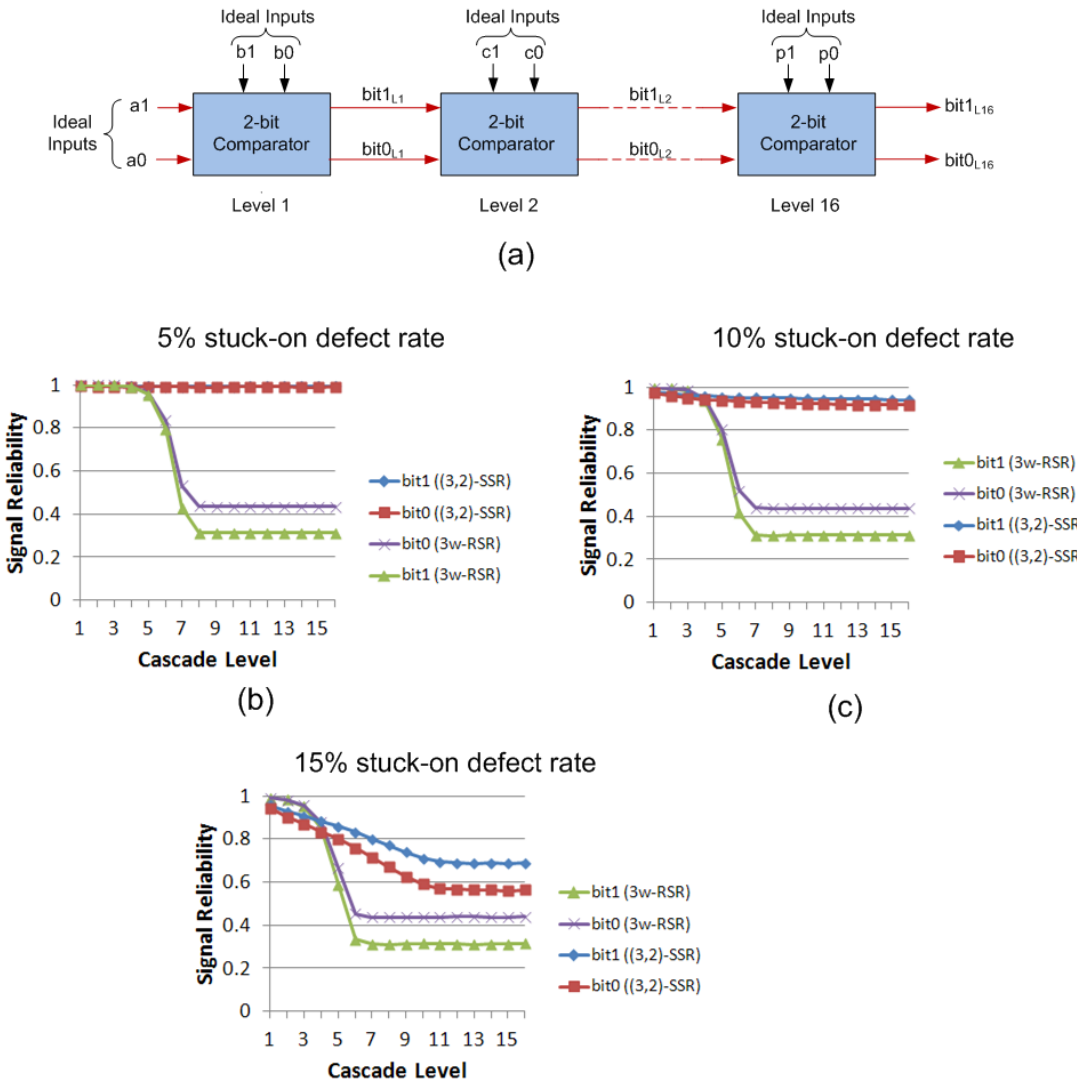


Figure 21: (a) Cascade of 2-bit comparators. (b) Signal Reliability along cascade of 3w-RSR and (3,2)-SSR implementations at 5%, (b) 10% and (c) 15% defect rate

Figure 21(b) shows the Signal Reliabilities at 10% defect rate. It can be seen that the degradation in Signal Reliability for the (3,2)-SSR scheme is greater in this case. Figure 21(c) shows the comparisons at 15% defect rate. It can be seen that the Signal Reliabilities of the (3,2)-SSR schemes reaches their minimum values after 10 levels of cascade. This occurs due to an escalation and eventual saturation of faulty '1's. The

minimum value is different from the 3w-RSR case because in the 3w-RSR a saturation of faulty ‘0’s occur.

5.6 Sensitivity to Stuck-Off Defects

In our analysis so far, we considered only stuck-on defects. In this section we provide a sensitivity analysis of the Signal Reliability through cascade implementations with stuck-off defects. Figure 22 shows the Signal Reliability along the cascade shown in Figure 12 with 10% total defect rate among which PS-OFF is the stuck-off rate and PS-ON is the stuck-on rate. $P_{S-ON} = 0.1 - P_{S-OFF}$. Figure 22(a) shows the Signal Reliability in 3w-RSR implementation of the cascade. It can be seen that significant drop in Signal Reliability occurs with even 1% rate of stuck-off defects. This is because a single stuck-off defect is sufficient to cause output of nanowire to be stuck at ‘1’.

Figure 22(b) shows the Signal Reliability in a (3,2)-SSR implementation. It can be seen that the SSR scheme is also equally affected by stuck-off defects. This is because, regardless of faults in the input signals, local stuck-off defects will have the same impact on both schemes since a single stuck-off transistors is sufficient to cause permanent fault at output a nanowire.

5.7 Summary

An analysis of fault propagation along a cascade of tiles with Regular Structural Redundancy was conducted using detailed analytical fault models. It was found that a rapid escalation of the probability of output faulty ‘0’s occurred along such a cascade and this was the dominant factor in the sharp drop in Signal Reliability after a few cascade levels. A new redundancy scheme called the Staggered Structural Redundancy was proposed whose design was motivated by the need to improve tolerance against input

faulty ‘0’s in order make larger cascades feasible. Simulation results showed that a single tile with (3,2) Staggered Structural Redundancy offered up to 56% more resilience against input faulty ‘0’s compared to the 3way Regular Structural Redundancy at 10% defect rate. The (3,2)-SSR scheme showed significant improvements in the Signal Reliability along a cascade of tiles compared to the 2w-RSR and the 3w-RSR. For instance, at a defect rate of 5%, the (3,2)-SSR Signal Reliability was greater than 0.98 after at least 100 levels of cascade whereas the that of the 3w-RSR dropped to 0.5 after 7 levels of cascade.

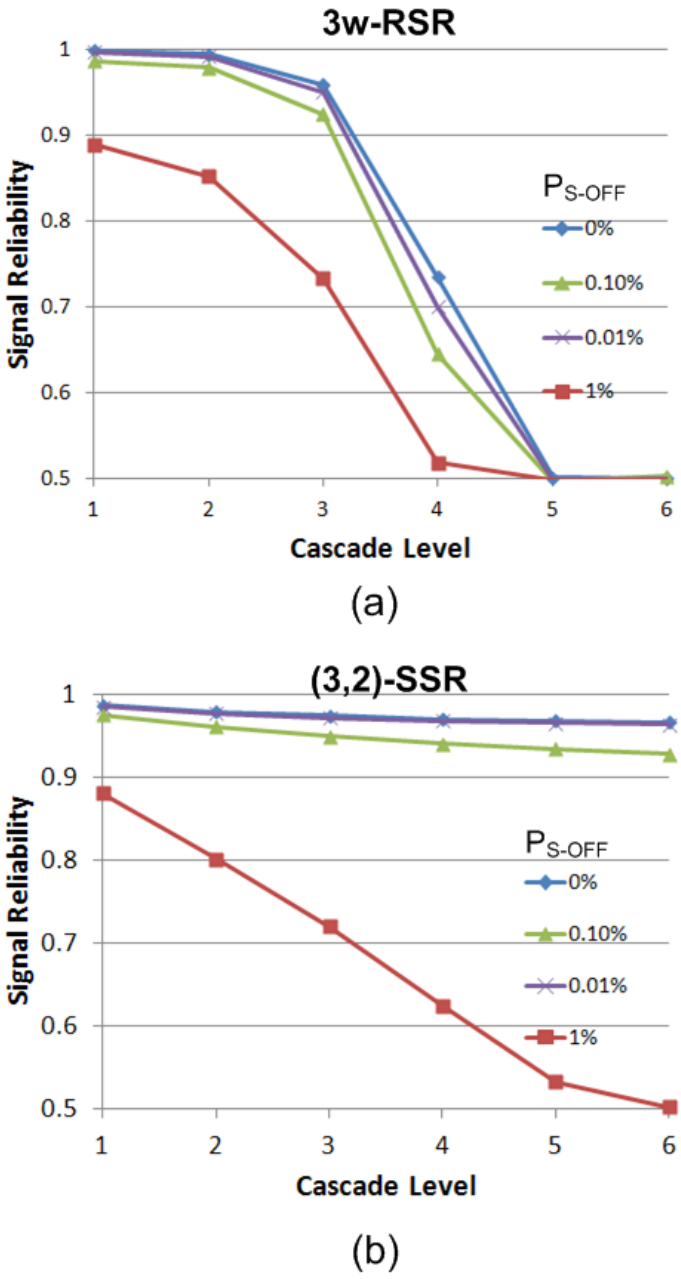


Figure 22: Signal Reliability along cascade with 10% total defect rate and PS-OFF stuck-off rate for (a) 3w-RSR and (b) (3,2)-SSR

CHAPTER 6

CONCLUSION

In this thesis, we developed detailed analytical fault models of the NASIC fabric taking into account its defect scenarios and its logic and circuit styles. Using the model, we have shown that the probability of output faulty ‘1’s and ‘0’s are unequal for single NASIC tiles. Consequently, application of biased voting schemes was shown to have up to 27% improvement on the signal reliability compared to conventional majority voting schemes. In this thesis, we also provided a study of the propagation of faults through a cascade of structurally redundant NASIC tiles. We have shown that a rapid escalation of faulty ‘0’s occur along the cascade of tiles with Regular Structural Redundancy eventually leading to decreased signal reliability. Motivated by this, we designed and introduced novel Staggered Structural Redundancy schemes that provide up to 56% improved tolerance to input faulty ‘0’s. We demonstrate that in a cascade of NASIC tiles employing the Staggered Structural Redundancy, the signal reliability of outputs at each cascade level remained above 0.98 for over 100 levels of cascade at 5% defect rate.

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