2011

Integrated Cmos Iq Upconverter/Downconverter for an X-Band Phased-Array Radar Application

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INTEGRATED CMOS IQ UPCONVERTER/DOWNCONVERTER FOR AN X-BAND PHASED-ARRAY RADAR APPLICATION

A Thesis Presented

by

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Submitted to the Graduate School of the
University of Massachusetts Amherst in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

September 2011

Department of Electrical and Computer Engineering

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FOR SALMA MIRZA

ACKNOWLEDGEMENTS

I would like to thank my advisor, Professor Robert Jackson, for his guidance and patience, and for providing me a challenging and practical project to serve as the basis of my graduate work. I thank him for teaching me many of the principles of microwave circuit design. I would also like to thank Professors Sigfrid Yngvesson and Christopher Salthouse, who both served as members of my thesis committee. Special thanks are due to Raytheon, for having supported the larger effort to which this thesis is a part and for providing the funding that made my assistantship and this project possible. Critical contributions were also made by IBM, which generously provided the wafer space on which this project was fabricated. I thank Lincoln Laboratory for the use of their multi-axis wafer probe station and the test equipment needed to perform certain measurements. I would like to thank the graduate academic program coordinator, Barbara Barnett, for her kind assistance in resolving any issues that arose with the graduate school, particularly in coping with the array of deadlines and forms. I especially thank my fiancée, Salma Mirza, for her continued encouragement, patience, assistance, and overall support throughout the entire process. Lastly, I would like to thank my parents for the many years of advice and encouragement that led up to this point.

ABSTRACT

INTEGRATED CMOS IQ UPCONVERTER/DOWNCONVERTER FOR AN X-BAND PHASED-ARRAY RADAR APPLICATION

SEPTEMBER 2011

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This thesis describes the design and measurement of an X-band IQ up/down converter that has been fabricated on a 180nm RF CMOS process. This converter includes components for mixing, frequency doubling, quadrature generation, amplification, and limiting. The specific circuit topologies used include passive double-balanced mixers, RC polyphase filters, and injection locked LC oscillators.

The converter is part of a transceiver chain that will make up the dedicated circuitry for each active antenna element of a phased-array radar. An active antenna element combines a radiator with its own transceiver subsystem. A phased-array radar, NetRad, is under development at the University of Massachusetts Amherst and will require thousands of active antenna elements. This motivates the need for low-cost integrated solutions. A silicon-based RF CMOS process provides a low-cost candidate technology to fulfill this requirement.

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CHAPTER 1

INTRODUCTION

In this thesis, the implementation of one part of a transceiver subsystem is presented. The subsystem is an active antenna module for an electronically steered phased-array radar and the specific requirements originate from the needs of CASA and its NetRad radar project. This project and the active antenna module are summarized in section 1.1 below.

This thesis specifically implements a CMOS IQ upconverter and downconverter, with associated quadrature LO conditioning circuitry. It is implemented in four variants, with various test configurations for each variant, all fabricated on a 5x5 mm IC. The four variants include either sub-harmonic(LO/2) or fundamental LO references and the presence or absence of quadrature coupling in internal injection-locked oscillators. The remainder of this thesis will discuss these implementations in detail. A high-level overview of the IQ conversion system is provided in CHAPTER 2. Circuit implementation details are covered in CHAPTER 3. Simulations of the complete systems will be presented in CHAPTER 4. Measurements of the fabricated die will be presented in CHAPTER 5. This work is concluded in CHAPTER 6. All designs in this thesis have been realized and tested on the IBM 7RF 180 nm RF CMOS process.

1.1 NetRad Weather Radar

The Center for Adaptive Sensing of the Atmosphere (CASA) is developing a weather radar system that can replace or augment the existing system, NEXRAD, used in the United States and elsewhere. NEXRAD uses many long range radars to cover an observation area. It is mechanically steered and its low-altitude visibility is limited by line-of-sight obstructions, such as the curvature of the Earth's surface. CASA proposes a new system, NetRad, which will employ electronically steer-able antennas and be densely distributed for improved low-altitude visibility. Electronically steered arrays will enable the use of algorithms for real-time tracking and observation and eliminate the maintenance problem of inertia, suffered by mechanically steered systems[1]. The NetRad system will require approximately 10,000 radars to cover the entire United States[1]. This is significantly more radars than are required by NEXRAD and this requirement motivates the need for a low cost radar design that falls under $10,000 per unit[1]. The resolution and observation distance of each unit, as well as size limitations for deployment[1], dictate an operating frequency in the X-band range.

The NetRad phased array will be implemented on a two-dimensional panel with many square microstrip patch antennas used as the radiating elements[2]. In order to provide the necessary directed beamwidth of 1°[1][2], the panel must have approximately 4,000 elements. Each of these elements will require its own transceiver subsystem, or active antenna module. In order to cover a 360° azimuth scan range, a minimum of 3 array panels will be necessary per radar[1]. As a result, approximately 12,000 active antenna modules will be required for each unit. For a total target radar cost of $10,000,

the active antenna modules will need to be very inexpensive. Low-cost active antenna modules, particularly multi-chip system in package(SiP) implementations, have been studied in [3][4]. In large volumes, even lower costs can be achieved by using a custom monolithic circuit implemented on a cheap semiconductor process[2]. CMOS processes are particularly low cost because they use a silicon substrate and are manufactured in very high volumes with high yield. CMOS is well suited to high levels of integration and can support mixed-mode circuits, leading to versatile single-die implementations. The node targeted for the monolithic active module and the implementation of this thesis, 180nm IBM 7RF CMOS, is expected to be sufficient to operate at the planned NetRad operating frequency, i.e. X-band.

CHAPTER 2

SYSTEM OVERVIEW

The following sections overview the IQ Upcoverter/Downconverter module and its place in the overall transmit and receive system. The module components will be discussed briefly in section 2.2. Some previous work is summarized in section 2.3.

2.1 Electronically Steered Phased Array Radar and Active Antenna Module

This thesis implements a part of the transceiver subsystem found within the active antenna modules dedicated to each antenna element of the CASA phased-array radar. This system must form and steer a narrow electromagnetic beam. The signal exciting each element in the phased array must, therefore, have a specific phase relationship with respect to that of all other elements. This scenario can be achieved if the active antenna module appropriately phase-shifts a transmit or receive RF signal that is distributed uniformly to every antenna element via a corporate feed network or some other mechanism. To realize such an architecture only a phase shifter, and possibly low noise(LNA) and power(PA) amplifiers, must be implemented in the active antenna module. The LNA and PA would be used to boost the transmit and receive signal levels and to reduce system noise. The challenging requirement of this architecture is the distribution of an RF signal throughout the array. The impact of signal loss and manufacturing tolerances on such an approach can be significant [3]. A slightly more complex alternative is preferred to overcome these challenges. One such alternative is to distribute a low-frequency IF signal and an LO signal instead of the RF. The resulting increase in complexity would require, in addition to the phase shifter, several typical

transceiver building blocks. This is the approach adopted for the active module to which this work applies. A functional diagram of the antenna module architecture is depicted in Figure 1 below. This system constitutes an entire active module that could be integrated onto a single 180 nm CMOS MMIC.

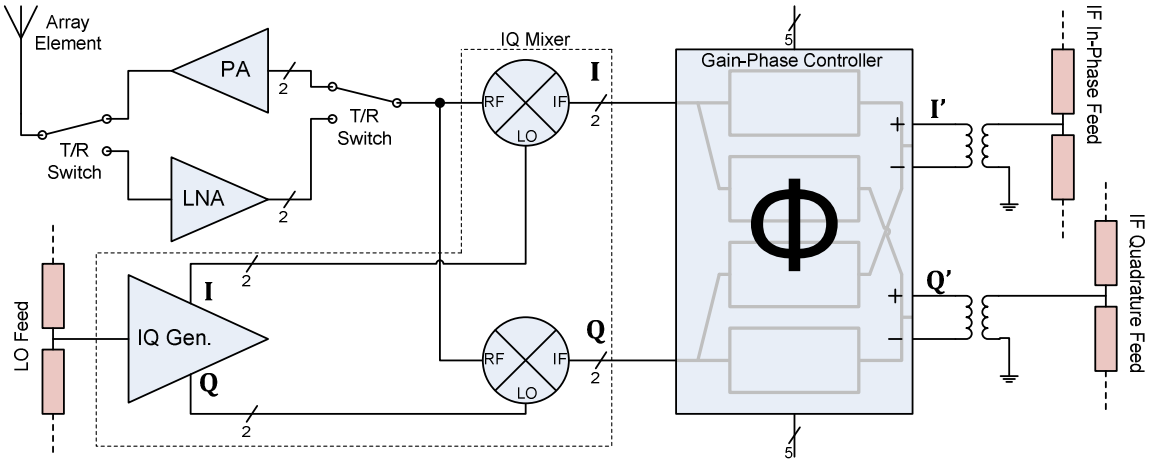


Figure 1. An active antenna module implementation for the CASA phased array. This implementation requires an LO and quadrature IF feeds. This work implements the circuits enclosed in the dotted lines. The Gain-Phase Controller was also designed and implemented as part of the same MOSIS fabrication run used for this project, but it is not the subject of this thesis.

CASA's use of shorter range radars, when compared to NEXRAD, will allow the use of shorter wavelength signals. Due to the lesser distances involved, the precipitation loss of the transmit and return pulse is no longer so great as to rule out the use of those frequencies. The NetRad radar will use an X-band transmit and receive frequency around 9.6 GHz. This is in contrast to the much lower frequency of 1.4 GHz(S-band) currently used by NEXRAD. The higher frequencies that are used by NetRad will allow better target resolution and are the enabling factor for meeting the antenna size requirement. At 9.6 GHz, a panel with the desired beamwidth and scan ranges can be fit into a 1-meter square area [2]. The drawback to using a 9.6 GHz RF signal is that it is more costly, in

terms of power and noise, to distribute on the panel. This is largely due to high frequency conductor and dielectric losses. With respect to manufacturing tolerances, another drawback is that the losses at high frequency become more difficult to control and may lead to signal levels that do not match up properly at the antenna elements [2].

In the topology of Figure 1, the RF signal is not distributed directly. Instead, three different microwave signals are distributed on the array panel. These are the in-phase IF, quadrature IF, and LO signals that are used for upconversion and downconversion. The IF signals are much lower in frequency than the RF signal and do not suffer significant conductor loss. For these signals, a corporate feed network is not necessary to match the power losses to and from each element and a much simpler series feed network can be used instead.

The LO signal is used to upconvert the IF signal on transmit and downconvert it on receive and, therefore, must be distributed on the panel at a frequency near that of the RF. Alternatively, the LO should be recoverable from a distributed signal that is a factor of a near-RF frequency. Given that the LO signal carries no critical information beyond its fundamental tone and phase relationship, more freedom can be exercised in its distribution to, and handling within, each active module when compared with a distributed RF. The same challenges that burden the distribution of an RF signal do not necessarily apply to the LO.

A high frequency distributed LO will suffer from conductor loss in the panel distribution network in the same way that the RF signal would. A possible way to reduce conductor power loss is to distribute the LO at a sub-harmonic and restore the fundamental at the active antenna module. Even if the LO is distributed at its fundamental frequency, it can be distributed with significantly relaxed regard for uneven conductor loss because the original amplitude relationship is unimportant and can be equalized at each element by a gain-limiting stage. A series feed network on the panel, despite looser tolerances, would also be sufficient for the distribution of such a signal.

An IQ phase shifter is included as the final stage before the IF feeds in Figure 1. Any relative phase mismatch at the IF or LO feeds to each element can be compensated with this phase-shifter. The phase shifters could be used to compensate for deterministic phase shifts as well as process related phase shifts with the addition of a calibration step.

In Figure 1, the antenna element represents a single square microstrip patch element through which the active antenna module will transmit(Tx) or receive(Rx). Tx/Rx switches dictate whether the Power Amplifier(PA) or Low-Noise Amplifier(LNA) are within the signal path. The PA is used for transmit and the LNA for receive. These devices are connected to the two mixers, which operate bi-directionally. The shared differential RF port of the mixers is an input, from the LNA, when operating in receive mode and an output, to the PA, when operating in transmit mode. The mixers are used to generate or receive differential I and Q signals at the IF port for the purpose of image rejection during upconversion or downconversion. The IF quadrature relationship is

guaranteed by ensuring a quadrature relationship between the LO signals driving each mixer's LO port. The two LO signals are generated by the circuits represented with the IQ generator block in Figure 1.

The IQ generator receives a single-ended synchronization signal that has been distributed on the array panel and outputs a pair of amplitude-limited differential LO signals that have a quadrature(IQ) relationship. The phases of the LO signals are locked to the synchronization signal, which may or may not be at the same frequency. Gain-limiting is necessary to equalize the LO outputs at each mixer and at each active module.

The gain-phase controller block, shown in Figure 1, provides configurable phase shifting functionality to the active antenna module. It is not a part of this thesis but has been designed and fabricated on the same MOSIS wafer run. The differential in-phase and quadrature IF ports of the mixers are connected to the gain-phase controller. The circuit then reproduces those signals with additional programmed phase shift and optimized impedance. The gain-phase controller block is bidirectional, allowing the IQ IF signals to be phase shifted on transmit or receive. This block provides the fundamental phase-shifting required at each element for array beam-forming. In Figure 1, the panel LO and IF feeds that are depicted are series feeds that would be used in a row-column architecture[2].

2.2 Image Reject Mixer and LO Feed Circuit

This thesis focuses on the dashed-outlined functional blocks of the system presented in Figure 1. These are the IQ (quadrature) generator and mixers. As mentioned

previously, two mixers must be implemented to realize an image reject capability in the system. A Hartley image reject scheme, as shown in Figure 2, is used, where the two mixers are driven by quadrature LO signals. Final image rejection is then achieved by phase shifting the IF output of one mixer by 90 degrees and adding it to the other. This operation is done by circuits on the array panel that are not part of the active modules. The quadrature LO signals that are used to drive the two mixers are generated on chip from the globally distributed LO synchronization signal, herein referred to as the LO reference signal in the implementations that will be presented. Figure 3 and Figure 4 depict two on-chip implementations of the relevant circuits for this functionality. The two implementations are each specific to a certain method of distributing the reference LO on the array panel. In Figure 3 the reference LO is distributed at a sub-harmonic, whereas, in Figure 4, it is distributed at its fundamental. These figures represent the two quadrature generation, or LO conditioning, methods that have been designed, fabricated, and tested for this work.

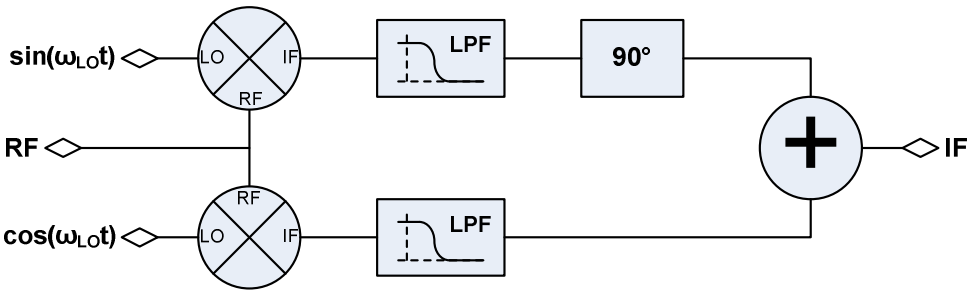


Figure 2. Hartley Image-reject Architecture.

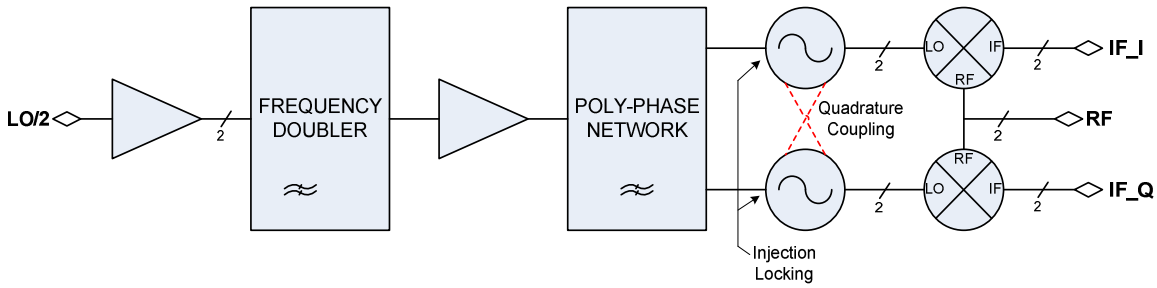


Figure 3. System level diagram for LO quadrature generation and mixing. For this circuit, the reference LO will be distributed at a sub-harmonic, 4.7 GHz. The circuit employs a frequency doubler and single stage RC polyphase filter. A common-drain amplifier follows the frequency doubler, serving as a low-impedance driver for the polyphase network.

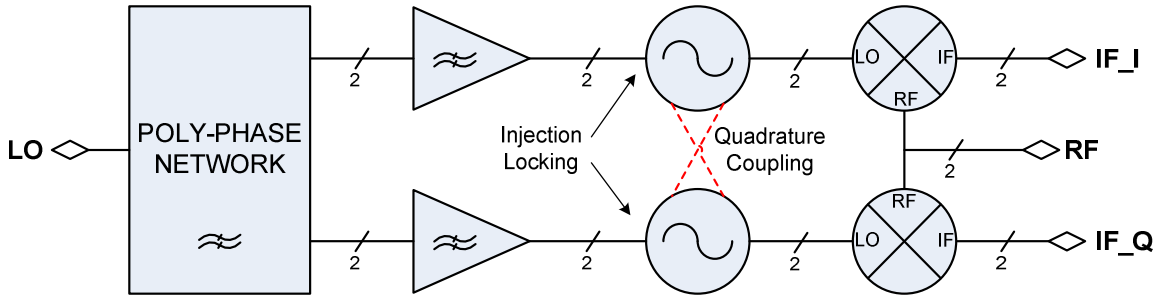


Figure 4. System level diagram for LO quadrature generation and mixing. For this circuit, the reference LO will be distributed at its fundamental, 9.4 GHz. This circuit employs a double stage RC polyphase filter.

In the implementation of Figure 3, herein referred to as the *sub-harmonic method*, the half LO frequency reference is fed into a balun that produces a differential output to drive a frequency doubler. The single-ended output of the frequency doubler passes through a buffer amplifier and a single stage polyphase filter to produce single-ended quadrature outputs.

In Figure 4, herein referred to as the *fundamental method*, a double stage polyphase filter is used to generate differential quadrature outputs directly from the

fundamental LO reference input. These outputs are each followed by a tuned buffer amplifier stage.

In both the fundamental and sub-harmonic methods, ignoring buffer stages, the polyphase networks are followed by two injection locked LC oscillators. These oscillators effectively amplify and amplitude-limit the in-phase and quadrature LO signals. One oscillator is dedicated to the I channel and one to the Q channel, with each one being injection-locked to the corresponding I or Q output of the preceding polyphase network. The two oscillators can be optionally coupled to each other, in which case they would become injection-locked and quadrature coupled LC oscillators. This optional coupling is represented by the dotted lines between oscillators in Figure 3 and Figure 4. Quadrature coupling is a specific method of cross coupling each oscillator's inputs to the opposite oscillator's outputs that forces them to oscillate in quadrature. The injection-locked oscillators have been fabricated in both uncoupled and quadrature-coupled variants.

2.3 Previous Work

The work in this thesis concerns the implementation of a quadrature up/downconverter on 180nm CMOS at X-band. The majority of similar CMOS transceiver systems reported in the literature operate at frequencies commonly targeted for unlicensed commercial wireless communications. Systems similar to this work, or sharing certain circuits, typically operate between 2.5 to 5 GHz.

A low-IF system of a very similar topology to the one implemented, fabricated on 180nm CMOS and operating at 2.45 GHz, is presented in [7] for downconversion only. This work uses a double-balanced passive mixer for down-conversion, but adds a dynamically compensating circuit for the DC bias voltage of the mixer FET gates. This reduces performance changes due to process variation. LO quadrature is generated with an RC-CR polyphase filter. A three-stage polyphase filter is used, where the additional stages are intended to improve quadrature-accuracy robustness against process variation. The LO buffer is a 3 stage chain of resistively-loaded differential amplifiers. IF buffers are also included at the mixer outputs. In this thesis project , an injection locked oscillator is used as the LO buffer which relaxes the polyphase filter requirements. Such a buffer provides both good drive strength and gain limiting.

A double-quadrature architecture [13] using 180nm CMOS is presented in [10] for 5 GHz operation. The double-quadrature architecture is shown in Figure 5. This circuit requires the generation of RF quadrature as well, but the double quadrature architecture helps suppress the effects of mismatches in the LO signals on image rejection. [10] employs a ring-oscillator based VCO for quadrature LO generation. An active polyphase filter is used for the low IF I and Q outputs to realize image rejection between 40 and 65 dB.

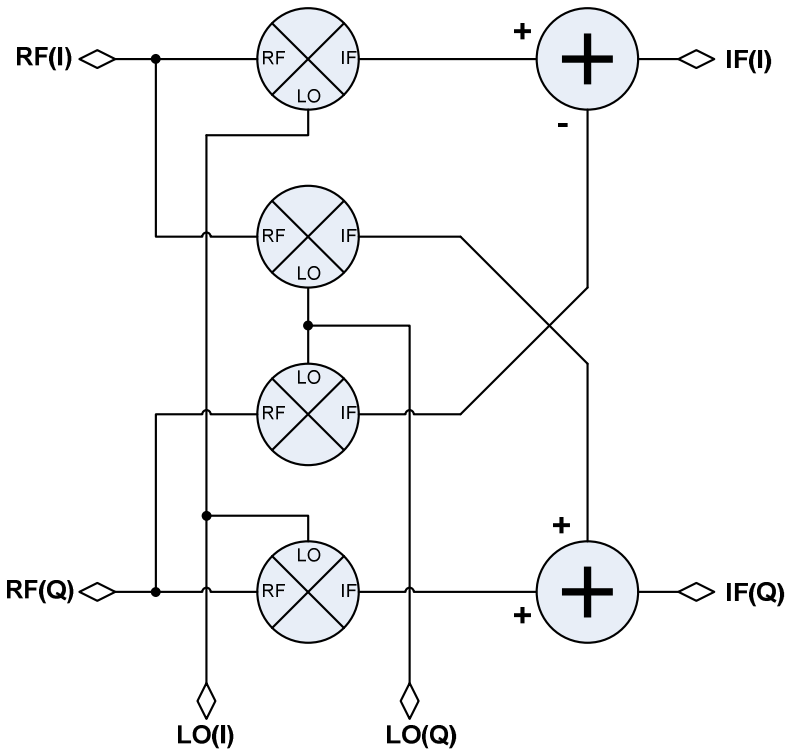


Figure 5. Double-quadrature architecture, adapted from [13].

A 5GHz SiGe direct-conversion quadrature modulator is presented in [6], which utilizes LO quadrature generation through the use of an RC-CR polyphase filter. The polyphase filter follows a doubly stacked architecture where additional RC elements are used to hide the impedance mismatches associated with certain unavoidable long transmission lines in the polyphase filter layout.

A notable feature of our approach, in one of its configurations, is the use of a sub-harmonic LO reference which must be doubled before generating quadrature. A sub-harmonic LO is used directly in [5] through the implementation of a sub-harmonic mixer. In [5], quadrature is generated at the sub-harmonic frequency. Unfortunately, this quadrature is a requirement of sub-harmonic mixing and not used for image rejection. The demonstrated mixer is for direct conversion architectures, where image rejection is

not important. [5] achieves a very high frequency of operation, 24 GHz, on 130 nm CMOS. A Low-IF mixer topology that uses a sub-harmonic LO is presented in [8]. This work uses a single-FET unbalanced passive mixer and a different method of frequency doubling. No quadrature is generated. The circuit operates at 28 GHz and is implemented on a 180 nm CMOS process.

The circuit implemented in this thesis uses injection locked LC oscillators for gain-limiting, improved driving capability and good amplitude match between quadrature signals. The performance of quadrature coupling between the LC oscillators has been examined. An injection-locked and quadrature coupled VCO is presented in [9], with prototypes implemented on 180nm CMOS. In that work the target operating frequency is 1.8 GHz and the injection locking is performed through the use of a second harmonic (3.6 GHz). The quadrature coupling provides the quadrature accuracy and the injection-locking is used to enhance phase noise performance. Due to the high frequency used in this work, second harmonic injection locking is not used.

CHAPTER 3

FUNCTIONAL BLOCKS

This chapter will cover the specific circuit implementations used for the various blocks represented in Figure 3 and Figure 4 of CHAPTER 2. Section 3.1 describes the IQ Mixer that is common to all of the methods of LO conditioning. The LO conditioning circuits, sub-harmonic and fundamental, will be described in sections 3.2 and 3.3, respectively. These two methods use similar injection-locked LC oscillator designs for the final stages. Discussion of these oscillators will be left for section 3.4. Layout drawings of specific circuits will be presented along with the discussion of those circuits throughout this chapter. Figure 6 and Figure 7 are layout drawings of the complete fundamental and sub-harmonic architectures. All other layout drawings presented will be a subset of these two drawings.

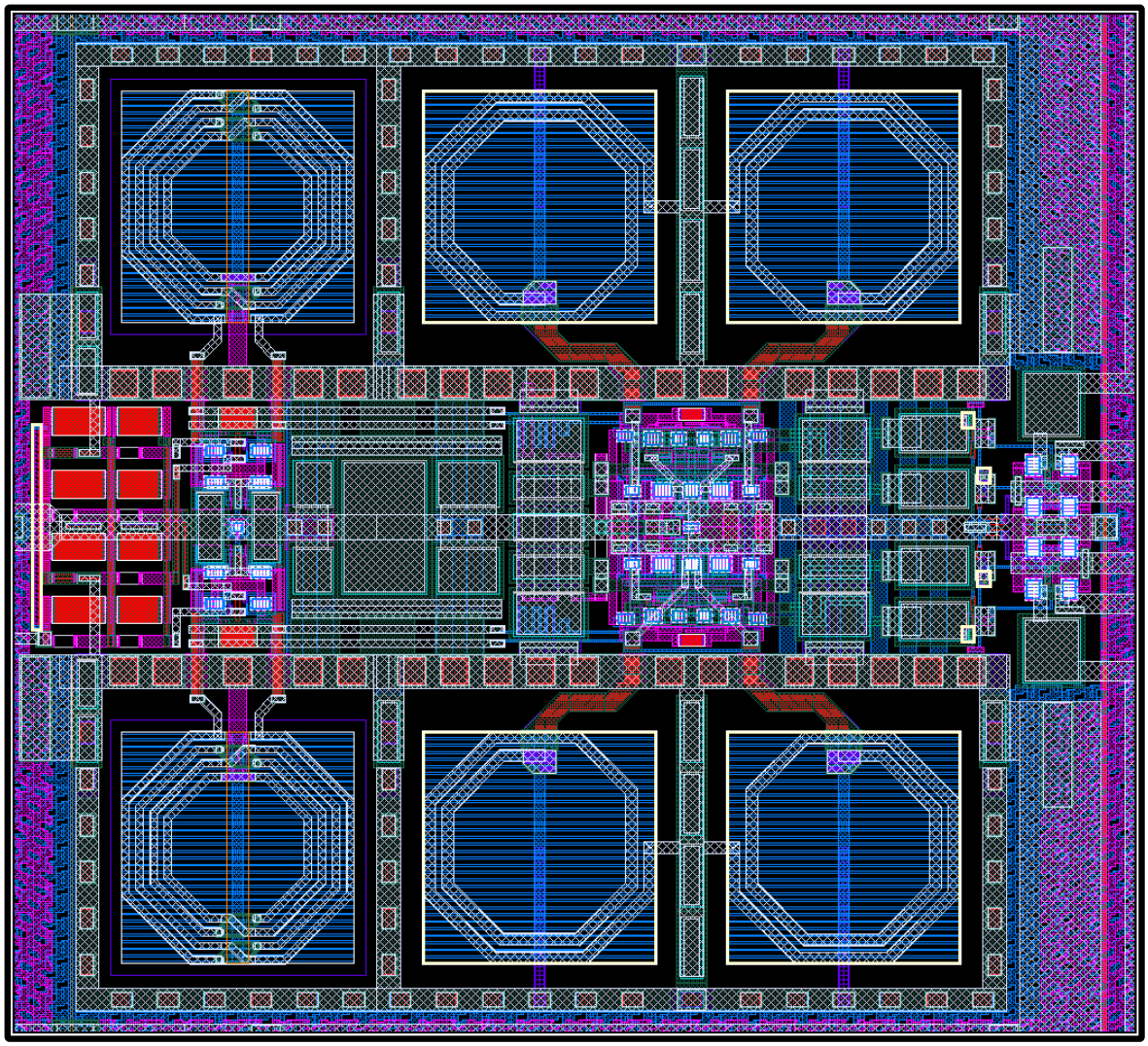


Figure 6. Layout of the differential quadrature LO generation and IQ mixing system. The system is referenced by an input signal at the fundamental LO frequency.

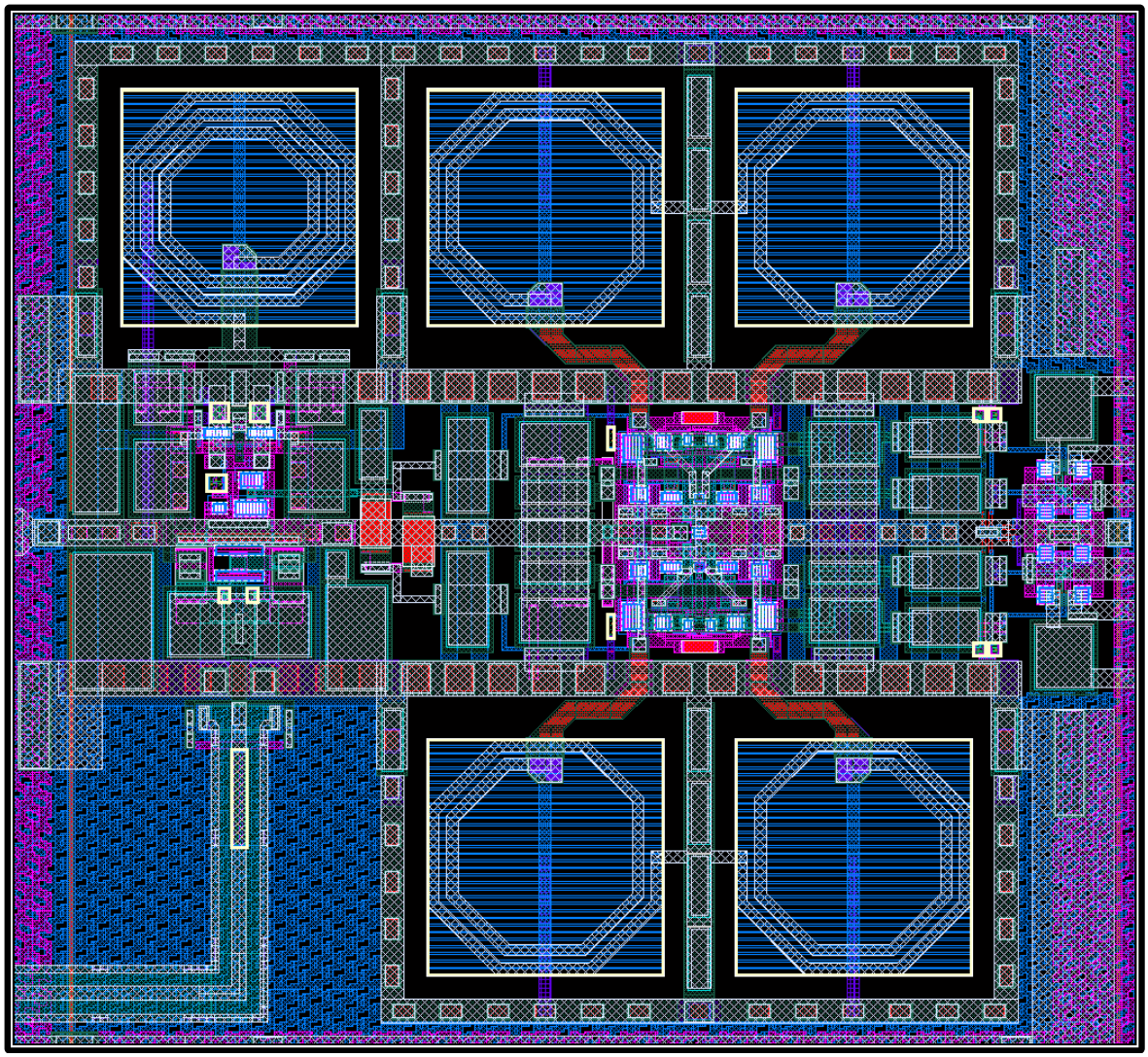


Figure 7. Layout of the differential quadrature LO generation and IQ mixing system. The system is referenced by an input signal at an LO sub-harmonic frequency, which is doubled by the circuit to recover the fundamental LO.

3.1 IQ Mixer

Figure 3 depicts two mixers, with differential ports, that are used for upconversion and downconversion. For this implementation, the mixing functionality was realized with a double-balanced passive FET mixer circuit. Passive mixers suffer less 1/f noise, or flicker noise, than other FET-based circuits by avoiding the use of DC currents for biasing. 1/f noise is observed at low frequencies and grows inversely proportional to the

frequency at which it is observed. The point at which the 1/f trend begins to appear above the otherwise constant noise floor is the 1/f noise corner and is a figure of merit for mixers and circuits in general. A low 1/f noise corner can permit the use of a low frequency IF, simplifying baseband processing. In addition to the noise benefits, passive mixers suffer less from the linearity impact of a limited supply voltage headroom. This increases the output compression point and leads to potentially large IIP3 [7]. Passive mixers can, therefore, exhibit a large dynamic range. This is particularly useful to radar applications that may see varying strengths of return signals.

Like any passive device, a passive mixer will suffer a power loss. The possible impact of such a loss is the need for additional RF gain from the LNA. Tradeoffs associated with attaining that additional gain may lessen or negate apparent improvements to noise or linearity that would be provided by the passive mixer architecture. The loss metric of interest for a mixer is the conversion loss. Conversion loss relates the RF and IF signal power levels.

For the fabricated FET-based IQ mixer, two passive mixers, each in a differential double-balanced arrangement and with a shared RF port, were chosen as shown in Figure 8. With appropriate quadrature LO signals driving the two LO ports, one of the two mixers will provide the in-phase(I) IF and the other will provide the quadrature(Q) IF. The IF I and Q signals, in conjunction with an off-chip 90° phase shift, will provide an image reject capability, as per the Hartley image reject architecture. It is important to note that all ports are differential in this circuit.

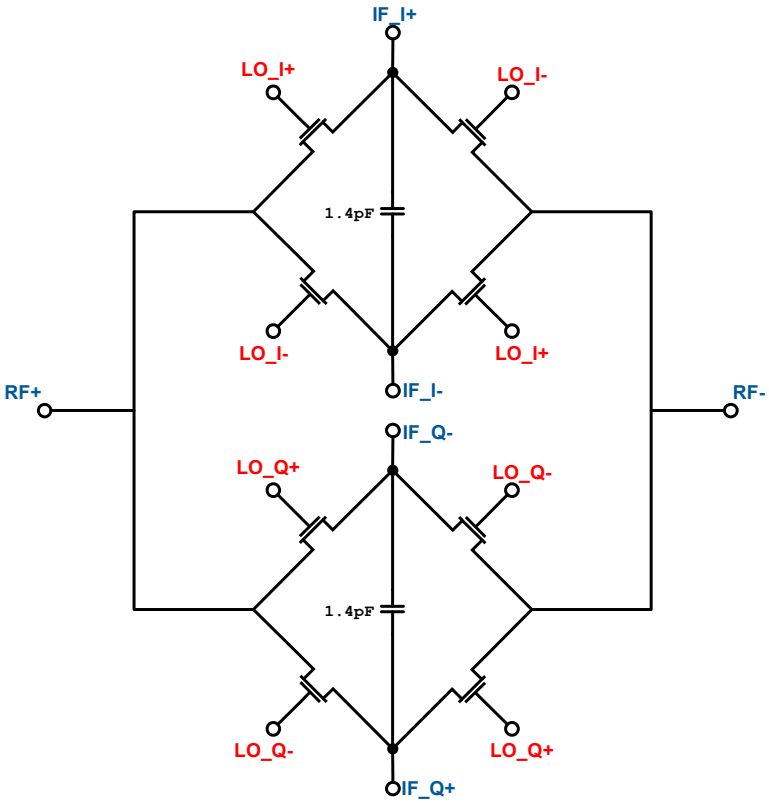


Figure 8. Two double-balanced passive FET mixers with common RF port. This arrangement can provide image rejection when the mixers are driven by quadrature LO signals. The in-phase differential LO port is indicated by LO_I+/LO_I- and the quadrature by LO_Q+/LO_Q-. The RF port is RF+/RF-. The IF in-phase and quadrature ports are IF_I+/IF_I- and IF_Q+/IF_Q-, respectively.

The passive double balanced mixer is a switching type mixer because the FET devices are alternated between the cutoff and triode regions. By switching on(triode) and off(cutoff) certain devices in the signal path, the RF current can be commutated back and forth between the antiphase IF ports. The differential quadrature LO signals, connected at the FET gates, control the switching action.

3.1.1 Conversion Loss

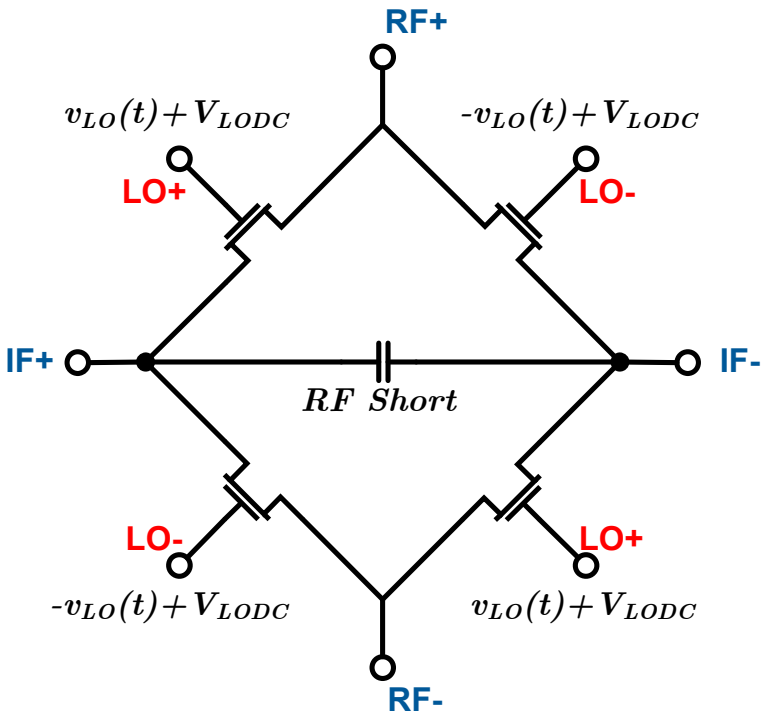


Figure 9. Double balanced passive FET mixer.

Mixer conversion loss computations require circuit analysis that accounts for at least three frequencies of interest. These are the IF, RF, and image frequencies. The analysis requires that the large-signal V-I characteristics for each non-linear device are considered. The LO is typically the only large signal excitation in a mixer and it is therefore possible to linearize the device V-I characteristics as a function of the LO. With a small RF voltage, the FETs in the passive mixer of Figure 9 are biased near zero-V_{DS} and exhibit the well known FET conductance, $g_T(t)$, in the triode region, as given below.

$$g_T(t) = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T) \quad , \quad V_{GS} > V_T \qquad \text{(Eq. 3.1)}$$

The gates of the FETs are driven by the LO signal, v_{LO}, which may be added to a constant DC bias, V_{LODC}. Given that the LO signal is described by the voltage waveform, $V_{LO}cos(\omega_{LO}t)$, the gate voltage will become $v_{GS}= V_{LO}cos(\omega_{LO}t)+V_{LODC}$ and (Eq. 3.1) can be rewritten as follows:

$$g_T(t) = \mu_n C_{ox} \frac{W}{L} (V_{LO}\cos(\omega_{LO}t) - V_K)u[V_{LO}\cos(\omega_{LO}t) - V_K] \quad \text{(Eq. 3.2)}$$
$$V_K = V_T - V_{LODC}$$

The inclusion of the unit step function, $u[]$, accounts for the transition of the FET into cutoff during part of the LO cycle where $V_{GS} < V_T$ and assumes an ideal cutoff. The expression provided by (Eq. 3.2) will therefore be valid over an entire cycle of the LO.

The above treatment assumes that the conductance does not vary for small variations of the RF(V_{DS}) present at each FET. This assumption effectively linearizes the conductance with respect to the LO and will allow the mixer conversion loss calculations to be simplified.

Further treatment of the conversion loss requires finding the first three coefficients of the Fourier series of $g_T(t)$, as given in (Eq. 3.2). The step function can be removed from $g_T(t)$ within the Fourier series integral if the limits of integration are modified accordingly. Considering also that $g_T(t)$ is an even function, the Fourier series coefficients are fully described by the following integral:

$$a_n = \frac{\omega_{LO}}{2\pi} \int_{-\frac{\cos^{-1}\left(\frac{V_K}{V_{LO}}\right)}{\omega_{LO}}}^{\frac{\cos^{-1}\left(\frac{V_K}{V_{LO}}\right)}{\omega_{LO}}} \mu_n C_{ox} \frac{W}{L} (V_{LO}\cos(\omega_{LO}t) - V_K)\cos(n\omega_{LO}t)dt \qquad \text{(Eq. 3.3)}$$

The solutions for the first three coefficients are:

$$\begin{aligned} a_0 = 2g_0 &= \frac{\mu_n C_{ox} W}{\pi L}\left(V_{LO}\sqrt{1-\left(\frac{V_K}{V_{LO}}\right)^2} - V_K\cos^{-1}\left(\frac{V_K}{V_{LO}}\right)\right) \\ a_1 = 2g_1 &= \frac{\mu_n C_{ox} W}{2\pi L}\left(V_{LO}\cos^{-1}\left(\frac{V_K}{V_{LO}}\right) - V_K\sqrt{1-\left(\frac{V_K}{V_{LO}}\right)^2}\right) \\ a_2 = 2g_2 &= \frac{\mu_n C_{ox} W}{3\pi V_{LO} L}(V_{LO}^2 - V_K^2)\sqrt{1-\left(\frac{V_K}{V_{LO}}\right)^2} \end{aligned} \qquad \text{(Eq. 3.4)}$$

The partial Fourier series expansion of $g_T(t)$, including these coefficients, is:

$$g_T(t) = g_0 + 2g_1 cos(\omega_{LO}t) + 2g_2 cos(2\omega_{LO}t) \qquad \text{(Eq. 3.5)}$$

In the above, g_0, g_1, and g_2 are elements that can be used to build a conversion matrix. The conversion matrix describes the linear relationship between the voltages and currents of a device at the RF, IF, and image frequencies. The conversion matrix is given below in (Eq. 3.6). The subscripts -1, 0, and +1 represent the voltages or currents through a device at the image, IF and RF frequencies, respectively.

$$\begin{bmatrix} I_{-1} \\ I_0 \\ I_{+1} \end{bmatrix} = \begin{bmatrix} g_0 & g_1 & g_2 \\ g_1 & g_0 & g_1 \\ g_2 & g_1 & g_0 \end{bmatrix} \begin{bmatrix} V_{-1} \\ V_0 \\ V_{+1} \end{bmatrix} \qquad \text{(Eq. 3.6)}$$

In the passive mixer, all of the FET devices have the same geometry and, consequently, the same conversion matrix with one notable difference—some of the

FETs are driven by an LO differential that is 180° out of phase. If the two LO phases are to be considered in the same analysis, the conversion matrix of those FETs driven by the out-of-phase LO must be adjusted accordingly. A 180^0 phase shift can be applied to $g_T(t)$ by substituting t with t' = t+π/ωLO, which will make the fundamental term of (Eq. 3.5) negative. Thus the conversion matrix for the affected devices will become:

$$\begin{bmatrix} I_{-1} \\ I_0 \\ I_{+1} \end{bmatrix} = \begin{bmatrix} g_0 & -g_1 & g_2 \\ -g_1 & g_0 & -g_1 \\ g_2 & -g_1 & g_0 \end{bmatrix} \begin{bmatrix} V_{-1} \\ V_0 \\ V_{+1} \end{bmatrix} \qquad \text{(Eq. 3.7)}$$

The conversion matrices and calculated Fourier series coefficients provide 3 equations and 6 unknowns for each device. The circuit needs to be taken into account to develop the remaining three equations, for each device, that will allow the system to be solved. The three equations are developed from circuit analysis at the three different frequencies of interest, the RF, IF and Image. Analysis of the entire circuit should therefore yield four independent equations at each frequency. The figure below shows the mixer circuit once more with the appropriate RF and IF port terminating impedances, g_s and g_{if}. Also shown are equivalent models of the mixer at the RF, IF and image frequencies. A capacitor across the terminals of the IF port is assumed to be a perfect short at RF and an open at IF.

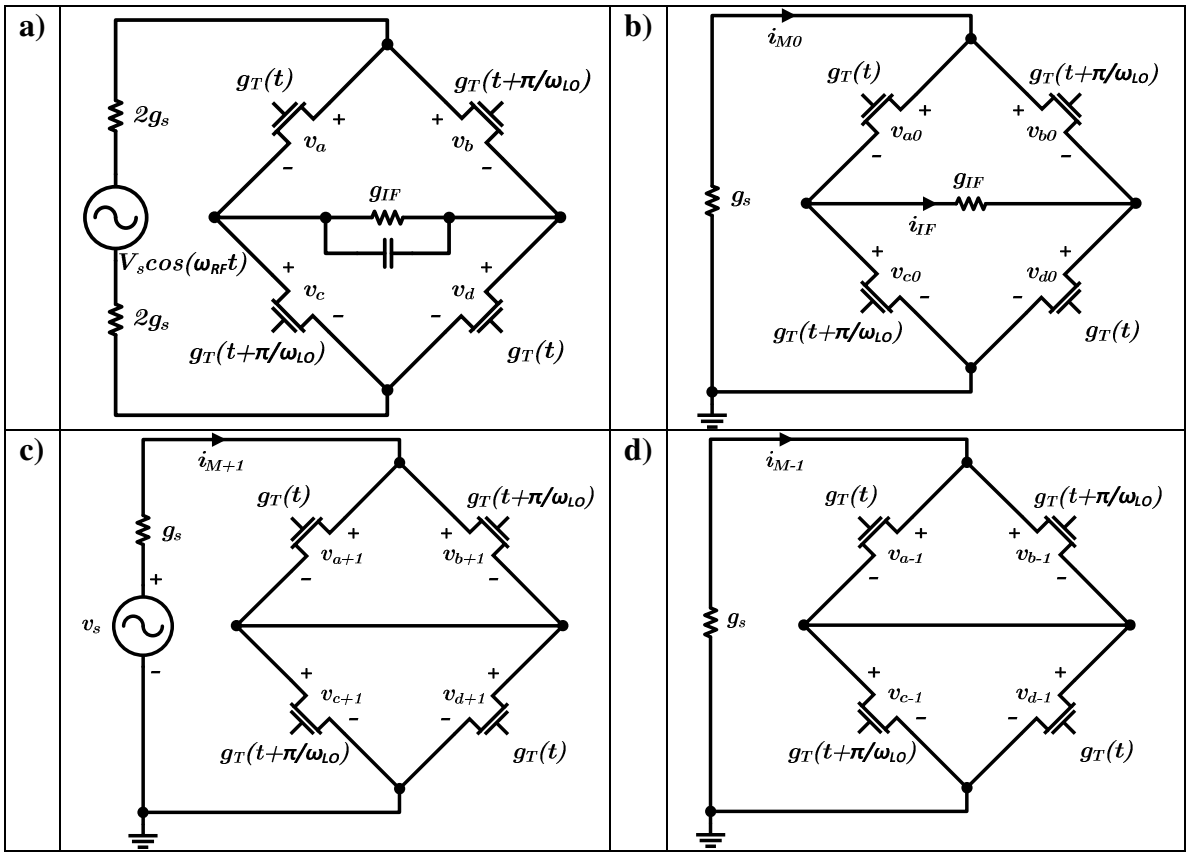


Figure 10. A model of the passive mixer(a) with RF and IF port terminations included. Also shown are simplified models at the IF(b), RF(c), and image(d) frequencies. The FETs pictured are treated as conductances that vary in the time domain according to g_T.

Twelve independent circuit equations that can be determined from circuit analysis of the above models and the four conversion matrices for each device are summarized in the table below.

Circuit Analysis-Based Relationships		
RF (Figure 10c)	Image (Figure 10d)	IF (Figure 10b)
$i_{a+1} + i_{b+1} = i_{c+1} + i_{d+1}$ $v_{a+1} = v_s - \frac{i_{M+1}}{g_s} - v_{c+1}$ $v_{a+1} = v_{b+1}$ $v_{c+1} = v_{d+1}$	$i_{a-1} + i_{b-1} = i_{c-1} + i_{d-1}$ $v_{a-1} = -\frac{i_{M-1}}{g_s} - v_{c-1}$ $v_{a-1} = v_{b-1}$ $v_{c-1} = v_{d-1}$	$i_{a0} + i_{b0} = i_{c0} + i_{d0}$ $v_{a0} = -\frac{i_{M0}}{g_s} - v_{c0}$ $v_{b0} = -\frac{i_{M0}}{g_s} - v_{d0}$ $v_{b0} = v_{a0} + \frac{i_{IF}}{g_{IF}}$
where, $i_{M+1} = i_{a+1} + i_{b+1}$	*where,* $i_{M-1} = i_{a-1} + i_{b-1}$	*where,* $i_{M0} = i_{a0} + i_{b0}$ $i_{IF} = i_{a0} - i_{c0}$
Conversion Matrix Relationships for Each Device		
$\begin{bmatrix} i_{a-1} \\ i_{a0} \\ i_{a+1} \end{bmatrix} = \begin{bmatrix} g_0 & g_1 & g_2 \\ g_1 & g_0 & g_1 \\ g_2 & g_1 & g_0 \end{bmatrix} \begin{bmatrix} v_{a-1} \\ v_{a0} \\ v_{a+1} \end{bmatrix}$	$\begin{bmatrix} i_{b-1} \\ i_{b0} \\ i_{b+1} \end{bmatrix} = \begin{bmatrix} g_0 & -g_1 & g_2 \\ -g_1 & g_0 & -g_1 \\ g_2 & -g_1 & g_0 \end{bmatrix} \begin{bmatrix} v_{b-1} \\ v_{b0} \\ v_{b+1} \end{bmatrix}$	
$\begin{bmatrix} i_{c-1} \\ i_{c0} \\ i_{c+1} \end{bmatrix} = \begin{bmatrix} g_0 & -g_1 & g_2 \\ -g_1 & g_0 & -g_1 \\ g_2 & -g_1 & g_0 \end{bmatrix} \begin{bmatrix} v_{c-1} \\ v_{c0} \\ v_{c+1} \end{bmatrix}$	$\begin{bmatrix} i_{d-1} \\ i_{d0} \\ i_{d+1} \end{bmatrix} = \begin{bmatrix} g_0 & g_1 & g_2 \\ g_1 & g_0 & g_1 \\ g_2 & g_1 & g_0 \end{bmatrix} \begin{bmatrix} v_{d-1} \\ v_{d0} \\ v_{d+1} \end{bmatrix}$	

Table 1. Equations defining the relationship between voltages and currents in the passive mixer circuit at three different frequencies. Summarized are those equations defined by the circuit topology and the conversion matrices determined for each device in the circuit.

The equations in Table 1 can be solved for all 24 unknowns, however the IF current, i_{IF}, passing through g_{IF} is of particular interest for the conversion loss calculation. The IF current has the following solution:

$$i_{IF} = i_{a0} - i_{b0} = \frac{v_s g_1 g_{IF} g_s}{(g_0 + g_{IF})(g_0 + g_2 + g_s) - 2{g_1}^2} \qquad \text{(Eq. 3.8)}$$

The conversion loss, L_C, for the mixer is the ratio of the power available from the RF source at the RF frequency to that delivered to the IF load, g_{IF}, at the IF frequency:

$$L_C = \frac{P_{av,RF}}{P_{del,IF}} \qquad \text{where,} \quad P_{del,IF} = \frac{|i_{IF}|^2}{2g_{IF}} \quad , \quad P_{av,RF} = \frac{g_s|v_s|^2}{8} \tag{Eq. 3.9}$$

Using (Eq. 3.8) and (Eq. 3.9) together will yield the conversion loss below. This is the solution via the conversion matrix method for the passive mixer of Figure 9:

$$L_C = \frac{\left((g_0 + g_{IF})(g_0 + g_2 + g_s) - 2{g_1}^2\right)^2}{4{g_1}^2 g_{IF} g_s} \tag{Eq. 3.10}$$

The following process parameters for the IBM 7RF process are freely available from MOSIS:

$$\mu_n C_{ox} = 310.6\ \frac{\mu A}{V^2}$$

$$\mu_n = 405\ \frac{cm^2}{V \cdot s} \tag{Eq. 3.11}$$

$$V_{T0} = 0.5\ V$$

The fabricated mixer employs FETs that each have a 50μm channel width and the minimum channel length, 0.18 μm. A DC bias voltage of 0.4 V is presented to the FET gates. In the best case, the mixer will be driven by a peak differential LO drive voltage of 1 Volt. This means that each gate sees a single-ended LO voltage waveform with a peak AC amplitude of 0.5 Volts. The IF source impedance is 100Ω differential and the RF impedance is 200Ω differential. A 200Ω RF source impedance reflects that the power is split between the two mixers in the IQ arrangement. Therefore, the conversion loss calculated for the single mixer with the above parameters will be the same as the total conversion loss of the IQ mixer of Figure 8. Evaluating (Eq. 3.10) with the process

parameters of (Eq. 3.11) and the design parameters described above yields a conversion gain of -6.63dB. Additional trends are shown in the figures below. The color plot, Figure 12, shows how the conversion gain is affected by both the RF and IF source impedance. The conversion gain is greatest for very high impedances because the ON resistances of the FETs become negligible in comparison. These high impedances are impractical, however, and will be largely attenuated by the unconsidered parasitic effects. The best conversion gains for a given IF or RF impedance are seen when the impedances are about the same, the skew of which is determined by the FET performance.

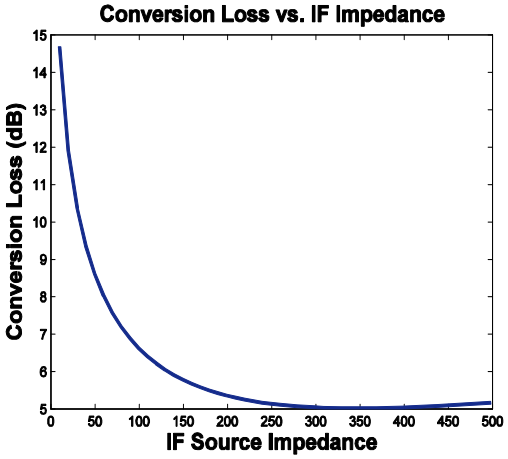


Figure 11. Conversion loss versus the IF port impedance with an RF source resistance of 200Ω.

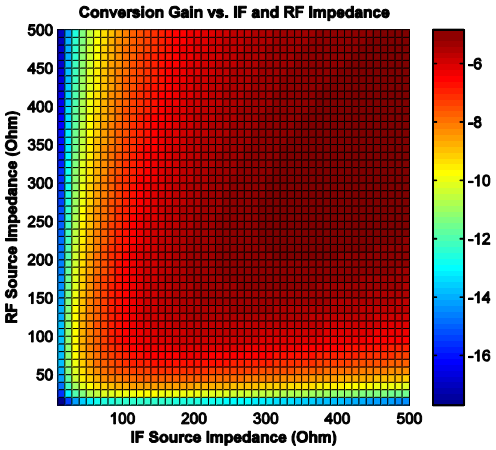


Figure 12. Color plot indicating how RF and IF impedance both affect conversion gain.

Conversion gain is a good measure of performance where power transfer is concerned, such as during the measurement or when the system is used as an isolated device. In a fully integrated implementation, where integrated amplifiers are located near the mixers, maximization of the conversion gain may not be the optimal solution. For example, on receive, the RF port would be driven by an LNA and the IF port would be connected to an integrating amplifier. The LNA, as a transadmittance amplifier, would

drive a fixed current into the connected mixer port. The IF amplifier would produce an output proportional to the current driving its input, thus behaving as a transimpedance amplifier. For this situation, the optimal solution is one that drives the greatest possible current out of the IF port for a given input current at the RF port. It is the current conversion gain, therefore, that is the figure of merit for a fully integrated implementation.

The current conversion gain is the ratio of the IF current, i_{IF}, to the Norton equivalent source current, i_s. The IF current can be found by substituting v_s in (Eq. 3.8) with the expression relating it to the current i_s of the Norton equivalent.

$$v_s = \frac{i_s}{g_s} \quad ; \quad i_{IF} = \frac{i_s g_1 g_{IF}}{(g_0 + g_{IF})(g_0 + g_2 + g_s) - 2{g_1}^2} \qquad \text{(Eq. 3.12)}$$

The current conversion gain, G_I, can be found simply as:

$$G_I = \frac{i_{IF}}{i_s} = \frac{g_1 g_{IF}}{(g_0 + g_{IF})(g_0 + g_2 + g_s) - 2{g_1}^2} \qquad \text{(Eq. 3.13)}$$

Figure 13 below is a color plot, based on (Eq. 3.13), of the current conversion gain versus the IF and RF port impedances. It is evident that this parameter is optimal when the RF impedance is high and the IF impedance is low.

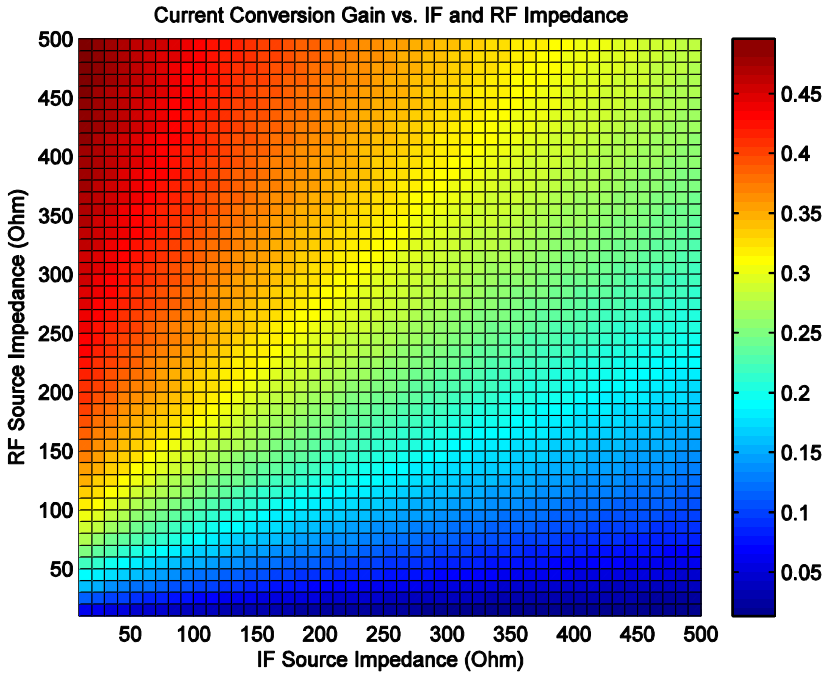


Figure 13. Color plot indicating how RF and IF impedance both affect current conversion gain. The color axis is A/A.

It is important to note that, in either optimization case, the transistor sizing is not chosen based on source matching but rather to be as large as possible while still allowing the LO voltage drive to reach an amplitude that will saturate the transistor. A mixer designed in this way will provide the best performance in both use cases. If the channel width can not be increased due to parasitics at the design frequencies, increased LO drive will still offer some benefit to current or power conversion gain. Such a limitation can arise, for example, when capacitances to the substrate become large enough to shunt the RF input, given the impedance and frequency of the RF source.

3.1.2 Noise and Linearity

The IQ mixer is a fundamental stage in the transceiver architecture and should be designed to add as little noise as possible so that the overall noise figure of the system will not be increased significantly. The passive mixer noise figure is at least equal to its conversion loss, but significantly better than active alternatives. This effectively shifts the noise tradeoff to other circuits in the transceiver architecture where compensating for the loss may be an issue. The passive mixer also exhibits superior 1/f noise performance, making it suitable for low-IF and direct-conversion architectures. The noise performance of passive FET mixers is examined in [22]. A double-balanced passive mixer, fabricated on a 130nm CMOS process, is reported in [23] and achieves a SSB noise figure of 8 dB between 5 and 6 GHz for a passive mixer with a conversion loss of 7 dB. The mixer described in section 3.1.1 and implemented for this thesis is expected to provide the same level of noise performance as indicated by [22] and [23]. Indeed, the fabricated device does exhibit a noise figure almost equal to the conversion loss in both simulation and measurement. Similarly, any 1/f noise trend was negligible and not observed over the IF frequency range of interest to this thesis.

Linearity performance will affect the dynamic range and spurious-free dynamic range of a mixer. A more linear response will allow the transceiver system to respond properly and predictably to a wider range of input signal levels. This thesis examines both the input-referred 1dB compression point, P1dB, and the input-referred third order intercept point, IIP3, for the fabricated mixer. The 1dB compression point indicates the maximum input level below which the conversion gain will remain relatively constant; it

is simulated in 3.1.4. The IIP3 is a measure of the third order intermodulation products and indicates the potential for out-of-band signals to mix and appear in-band. IIP3 is simulated in the frequency domain in a manner similar to the P1dB and with recent models that correctly predict a 3:1 slope[24]. IIP3 can vary with LO drive. It is measured to be around 10dBm for the fabricated circuits of the fundamental method and 6-8 dBm for the sub-harmonic circuits. In comparison, [20] reports a P1dB of 7 dBm and IIP3 of 14 dBm for a passive mixer implementation on a 180nm BiCMOS process. In [21], a 1dB compression point of 5dBm and an IIP3 of 11 dBm are observed near 10 GHz on a 180 nm CMOS process.

3.1.3 Layout

The eight FET devices that comprise the IQ passive mixer arrangement are each 50μm in width. The minimum 0.18μm channel length is used for all devices, in keeping the channel conductance as high as possible. The FETs are multi-fingered devices, having 10 fingers of 5μm width each, and can be seen in the center of the layout shown in Figure 14. The corresponding schematic is shown in Figure 15. The optimum point for the DC bias(V_{GS}), in this case 0.4 V, was chosen based on the equations of section 3.1.1 and fined tuned in simulation for maximum conversion gain. Those DC bias levels are set by four resistive voltage dividers, implemented with “precision” poly-silicon resistors, that each connect a pair of FET gates within the mixer. The precision poly-silicon resistors provide the highest sheet resistance (1600 Ω/sq.) for this process and require an additional mask. The resistors add an additional differential impedance of 4.11k ohms at either LO port and negligibly attenuate the LO signals driving those ports. Each end of the differential I or Q LO signal must be AC coupled to the mixer LO ports. The RF

filtering capacitors connected to the IF ports of either mixer are 1.4 pF MIM capacitors visible at the extreme right or left of the layout shown in Figure 14.

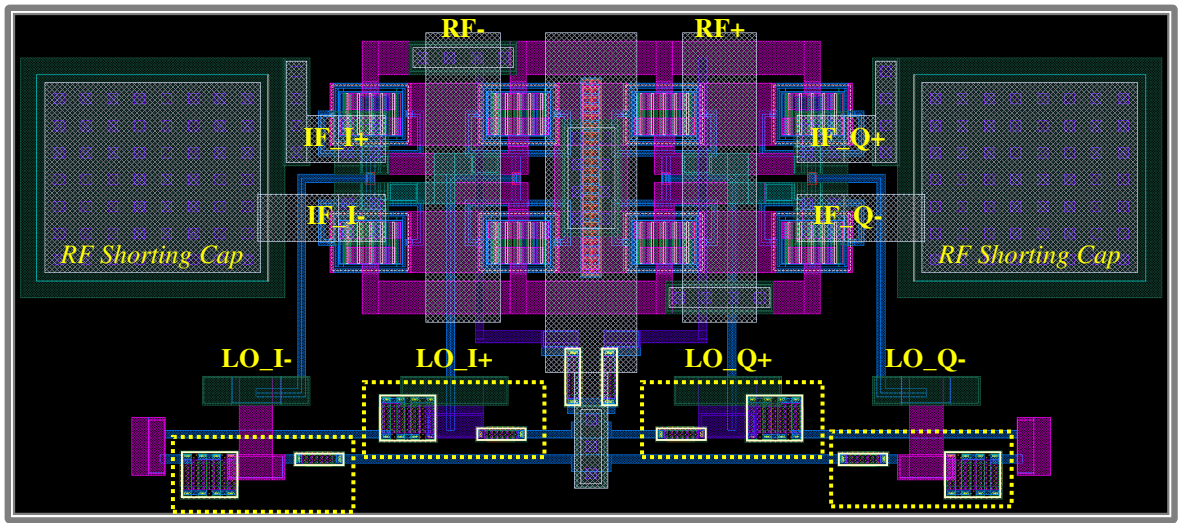


Figure 14. Layout of the double-balanced passive IQ mixer. MIM capacitors at the extreme right and left short any RF signal content at the IF ports. Each LO differential has a DC bias set by resistive voltage dividers, which are located within the regions indicated by dotted lines. This image corresponds to a 138μm by 66μm area.

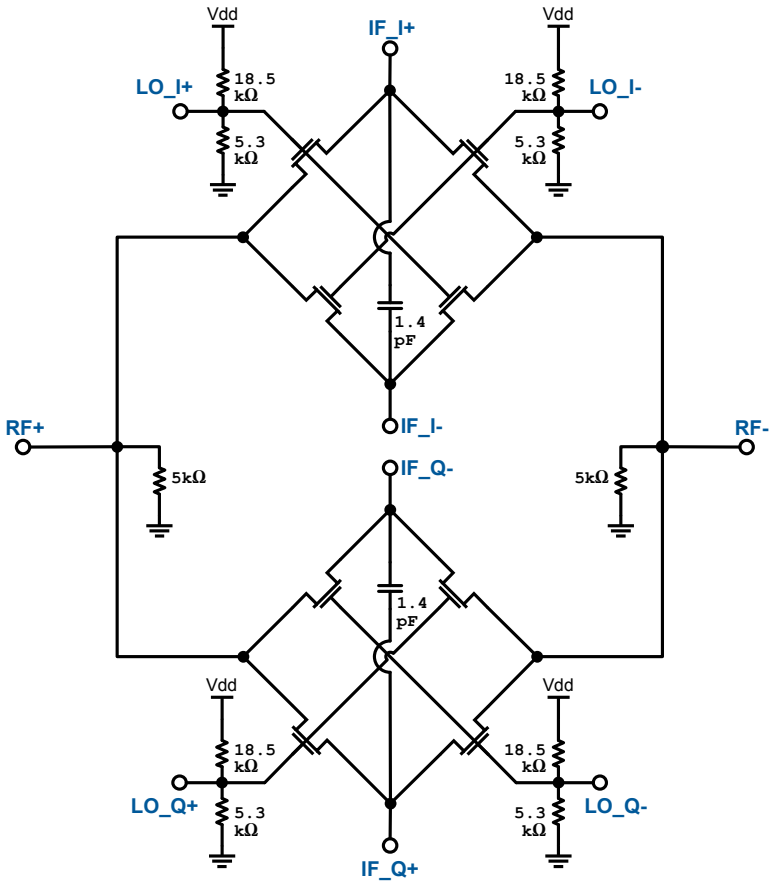


Figure 15. Complete schematic of the double-balanced passive IQ mixer. All FETs use W/L dimensions of 50µm/0.18µm.

3.1.4 Simulation

The following simulations correspond to the extracted netlist for the layout of Section 3.1.3, which is the IQ mixer, by itself, without connection to the rest of the system. Included in the extraction are interconnect resistances, parasitic capacitances, and detailed models for the devices used. Frequency domain harmonic balance simulation in ADS is used for the analysis. All simulations correspond to a 9.4 GHz LO, 9.6 GHz RF, and 200 MHz IF.

Nominally, the IQ mixer is driven by quadrature differential LO signals having a 1V peak amplitude at the LO frequency. This corresponds to a 0.5 V peak single-ended signal at each FET gate in the circuit. The simulated image rejection ratio for the mixer by itself, driven with perfect quadrature LO signals, is -55.5 dB and the P1dB is 3dBm. The image rejection ratio figure is optimistic, and is instead limited by the quality of the quadrature generation in the complete implementations of Figure 3 and Figure 4.

The strength of the LO drive affects both conversion gain and linearity. IIP3 linearity improves with increasing LO drive, as does the P1dB[23]. There are diminishing benefits to the conversion gain in increasing the LO drive beyond a certain point. At that point, it is better to increase the size of the transistors in the mixer, thereby reducing the ON resistance. Figure 16 and Figure 17 below show the simulated trends in the extracted IQ mixer's conversion gain and IIP3 performance versus the single-ended LO drive voltage. In these simulations, the RF source differential impedance is 100Ω(or 200Ω at each mixer) and the IF differential impedances are each 100Ω. In other words, the available power to the two mixers combined is supplied by a 100-ohm source and the output power delivered at either the IF_Q or IF_I ports is delivered to a 100-ohm load. The conversion gain shown here for the LO overdrive voltage used in the example of 3.1.1 is about 0.7dB worse than predicted. Further simulation results are provided in CHAPTER 4.

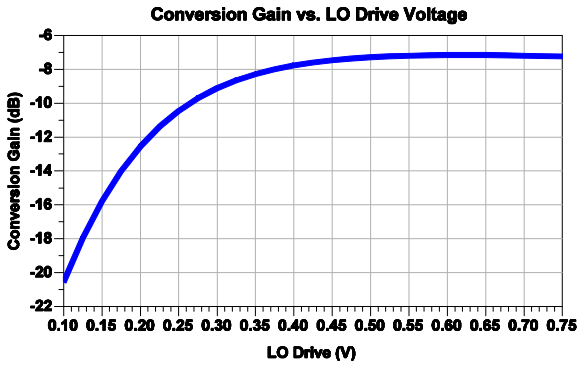


Figure 16. Simulated conversion gain versus peak LO voltage drive at each FET gate.

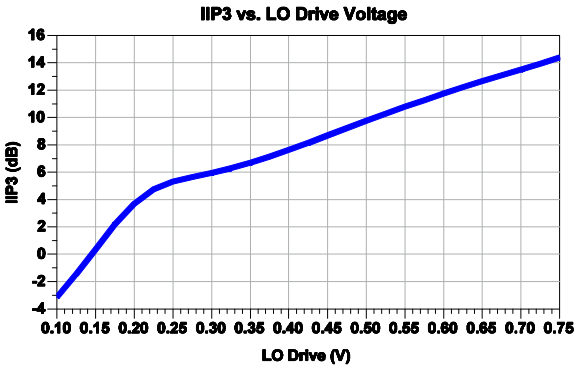


Figure 17. Simulated IIP3 versus peak LO voltage drive at each FET gate.

3.2 Quadrature LO Generator with Sub-Harmonic LO Reference

The topology for the sub-harmonically referenced LO quadrature generator, as shown in Figure 3 and Figure 7, contains a balun, frequency doubler, buffer amplifier, and polyphase filter. These circuits will be addressed with more detail in the following sections. Discussion of the LC oscillators, used for boosting the LO level, is left for section 3.4.

3.2.1 Input Balun

The reference LO input is a 4.7 GHz, single-ended, first sub-harmonic of the fundamental LO frequency. This sub-harmonic needs to be doubled to recover the desired frequency of the LO signal. The frequency doubling circuit requires a balanced input, motivating the need for the single-ended to differential buffer presented in this section.

The reference LO buffer, or input balun, is represented by the first stage of Figure 3. A somewhat high input impedance should be presented by this stage because the LO reference is tapped from a low impedance feed line that will be tapped by other identical

active antenna modules. The choice of device sizes will control this impedance. The topology for the input balun is shown in Figure 18 below. This configuration is reported in [5].

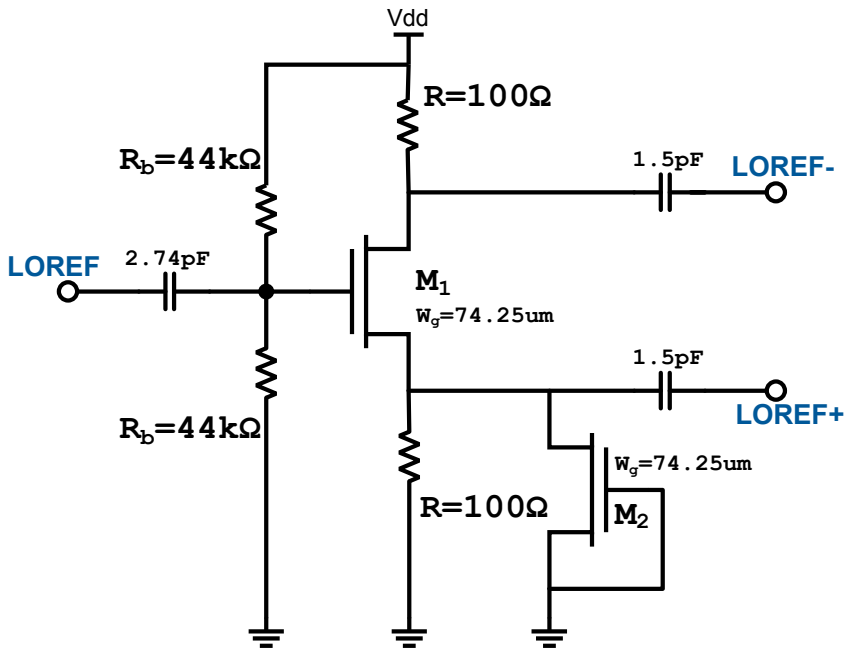


Figure 18. Single-ended to differential buffer as reported in [5]. This is a resistively loaded and degenerated common source stage. The second transistor, M_2, is added for the matching of drain-gate capacitances at both differentials. The single-ended input and balanced outputs are at the sub-harmonic LO frequency.

The schematic of Figure 18 is a resistively-loaded single stage amplifier. The devices are each multi-fingered FETs, with 27 fingers, and have a total width of 74.25µm and a 180nm length. Each FET has 27 fingers of 2.75µm width. The input impedance is predominantly capacitive and approximately equal to 0.3 pF. The advantage of this configuration is the lack of resonant structures, especially inductors, which allows this topology to be area efficient. This amplifier is also broad band, so it will not contribute to losses as a result of consecutive mismatches in tuning. The relatively large input signal will cause this amplifier to saturate, providing some amount of gain limiting. The

majority of gain limiting performance is provided by the later injection-locked oscillator stages. This circuit requires that low resistances be used for R to increase drive capability and improve linearity when wide FETs are used. This adds to the DC current consumption, which is a drawback to this topology.

The input signal, v_{LOREF} in Figure 18, varies the incremental drain current of the M_1 FET device. The transconductance is chosen by varying the device size while maintaining a gate bias voltage at half of the supply voltage. Increasing the transconductance in this way will increase the gain of the stage and also increase the DC bias current the stage draws. Therefore, the DC current is the limiting factor in choosing the device size. The gate bias voltage is chosen to allow the maximum swing of the differential output(v_{LOREF} + and v_{LOREF} -). The gate bias voltage is maintained by the resistors, R_b, which form a voltage divider.

The differential outputs are taken at the source and drain of M_1. If the input signal is driving the incremental current high, the voltage difference between the two outputs is small. As the incremental current is reduced, this difference increases. This produces two antiphase signals at the output. For a small input signal, and taking into account only the parasitic gate capacitance of the input transistor, the output phasors may be expressed as follows.

$$v_{LOREF}{}^{-} = -\frac{g_m R\, v_{LOREF}}{1 + g_m R + j\omega RC_{gs}}$$
$$v_{LOREF}{}^{+} = \frac{v_{LOREF}\left(g_m R + j\omega RC_{gs}\right)}{1 + g_m R + j\omega RC_{gs}} \qquad \text{(Eq. 3.14)}$$

These expressions ignore output resistance, parasitic drain-source capacitance, and gate-drain capacitance as well as the substrate body effect. C_{gs} and g_m are the gate capacitance and transconductance of M_1 in Figure 18. It is immediately evident from the expressions that the two outputs will be 180° out of phase if C_{gs} is negligible. At high frequencies, non-negligible C_{gs} will result in a divergence from a perfect 180° phase relationship and amplitude match. Further down in the LO conditioning chain, this will result in feedthrough of the sub-harmonic LO and will not directly contribute to amplitude or phase mismatch of the LO signals driving the mixers. Other parasitic capacitances have a similar effect to C_{gs} in this circuit and other effects are partially compensated by the presence of M_2, described below. Additional amplitude and phase mismatches arise from linearity issues as the amplifier saturates.

The input balun of Figure 18 is susceptible to imbalances as a result of parasitic capacitance mismatches at the source and drain terminals of the common-source device, M_1. A second transistor, M_2, with equal width is used to balance the gate-drain capacitance seen at each of these terminals[5]. This balancing works in the small signal regime; however, in this implementation, the amplifier will be driven near saturation, introducing additional sources of mismatch. Any mismatch will manifest itself as fundamental feedthrough at the single-ended output of the frequency doubler. Fortunately, this feedthrough will be attenuated by the output tank in the frequency doubler and by the polyphase filter. The later injection-locked LC oscillator stages very effectively suppress any remaining feedthrough of the sub-harmonic LO. The insensitivity of the overall quadrature generator to mismatch at this stage is what allows

this circuit to be a viable choice for a simple and area-efficient balun in this topology. Due to the additional sources of mismatch , particularly those resulting from non-linearity when the amplifier nears saturation, the benefits of M_2 in this circuit become negligible. M_2 is kept in the final layout and fabricated die, however.

The fabricated circuit uses K1 BEOL resistors, as described in the appendix to this thesis, to achieve a resistance of 100 ohms that is as well matched as possible and wide enough to carry the bias current. The DC bias current required by this circuit is about 4mA. The bias resistors, R_b, are poly-silicon resistors chosen for their higher resistance density so that the bias circuitry will have a negligible effect on the input impedance. The layout of this circuit is shown in Figure 21, along with the frequency doubler and polyphase filter.

3.2.2 Frequency Doubler

The frequency doubler is a key component of the architecture of Figure 3. It is responsible for the recovery of the fundamental LO from the sub-harmonic LO reference. The frequency doubler implementation is shown in Figure 19. This circuit includes a buffer amplifier stage before the final output for better matching to the following stage.

The frequency doubler is made up of the transistors M_1 and M_2, as shown in Figure 19. The differential sub-harmonic input is AC coupled to the gates of these devices, where either gate is 180° out of phase with the other. The drains share a common node to which M_1 and M_2 together drive a full-wave rectified version of the sub-harmonic LO reference. This becomes a recovered fundamental LO reference when filtered by a

resonant tank circuit. The tank, provided by L_{tank} and C_{tank}, is used for output peaking at the LO frequency. The tank capacitance, C_{tank}, is implemented as a MIM capacitor and will also include the load capacitance at the output and capacitive parasitics. C_{byp} and R_1 drop the supply voltage to avoid gate oxide breakdown of M_1 or M_2. R_{b1} and R_{b2} set the voltage of the DC gate bias.

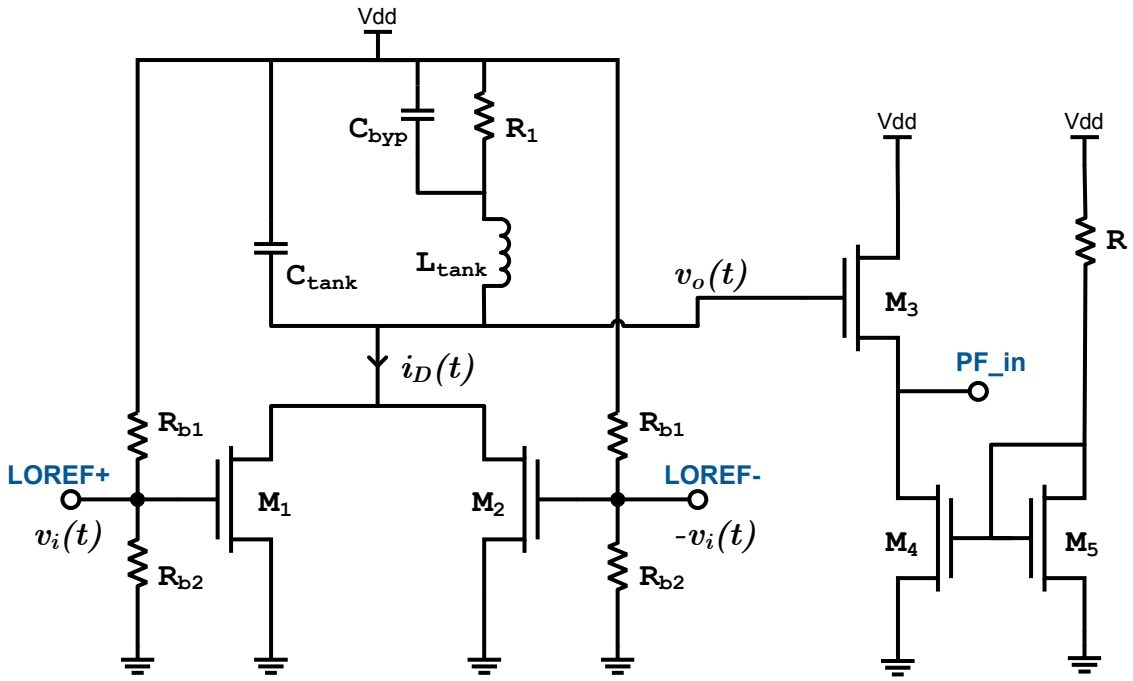


Figure 19. Frequency doubler with output buffer.

In Figure 19, the differential sub-harmonic LO inputs, LOREF + and LOREF -, are driven by the waveforms $v_i(t)$ and $-v_i(t)$, which represent the differential output from the input balun of Section 3.2.1. The output waveform is defined as $v_o(t)$. $i_D(t)$ represents the combined drain current of the two FETs, M_1 and M_2. Given that $v_i(t)=V_i\cos(\omega_s t)$, the Fourier series of the current, $i_D(t)$ can be determined for the two transistors as they alternate between cutoff and saturation. The expression for $i_D(t)$ is provided by (Eq. 3.15) below. This is the sum of the square law expressions for the saturation drain currents of

each transistor. The unit step functions have been added to the saturation expressions so that $i_D(t)$ is valid for the cutoff region of the FETs as well. (Eq. 3.15) assumes an ideal cutoff.

$$i_D(t) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_i cos(\omega_s t) - V_k)^2 u\left[cos(\omega_s t) - \frac{V_k}{V_i}\right] + \frac{\mu_n C_{ox}}{2}\frac{W}{L}(-V_i cos(\omega_s t) - V_k)^2 u\left[-cos(\omega_s t) - \frac{V_k}{V_i}\right] \quad \text{(Eq. 3.15)}$$

The Fourier series coefficients of (Eq. 3.15) are given by the Fourier series integral:

$$a_n = \frac{\omega_s}{2\pi}\int_{-\frac{\pi}{\omega_s}}^{\frac{\pi}{\omega_s}} i_D(t) cos\,(n\omega_s t)dt =$$

$$\frac{\omega_s}{2\pi}\int_{\frac{-cos^{-1}\left(\frac{V_k}{V_i}\right)}{\omega_s}}^{\frac{cos^{-1}\left(\frac{V_k}{V_i}\right)}{\omega_s}} \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_i cos(\omega_s t) - V_k)^2 cos(n\omega_s t)dt + \frac{\omega_s}{2\pi}\int_{\frac{\pi - cos^{-1}\left(\frac{V_k}{V_i}\right)}{\omega_s}}^{\frac{\pi + cos^{-1}\left(\frac{V_k}{V_i}\right)}{\omega_s}} \frac{\mu_n C_{ox}}{2}\frac{W}{L}(-V_i cos(\omega_s t) - V_k)^2 cos(n\omega_s t)dt \quad \text{(Eq. 3.16)}$$

The unit step functions of $i_D(t)$ are removed from the Fourier integral in (Eq. 3.16) by modifying the bounds of the integral. In the above equations, the angular frequency, ω_s, is that of the sub-harmonic LO. The bias-corrected threshold voltage, V_K, is equal to V_T - V_B, where V_B is the DC gate bias voltage of M_1 and M_2. W and L are the width and length of the FETs.

The DC component of the Fourier series of $i_D(t)$, I_{DC}, is equal to the DC current requirement of the circuit. The first Fourier series coefficient is the solution to (Eq. 3.16) when $n=0$. That coefficient, a_0, and the DC current, can be shown to be:

$$I_{DC} = \frac{1}{2}a_0 = \frac{\mu_n C_{ox}}{4\pi}\frac{W}{L}\left((V_i^2 + 2V_K^2)cos^{-1}\left(\frac{V_K}{V_i}\right) - 3V_i V_k \sqrt{1 - \frac{V_K^2}{V_i^2}} \right) \quad \text{(Eq. 3.17)}$$

$$I_{DC}|_{V_k=0} = \frac{\mu_n C_{ox} V_i^2}{8}\frac{W}{L}$$

The FETs, M_1 and M_2, will drive the current $i_D(t)$ through the tank circuit of Figure 19. At resonance, $\omega_{tank}=1/\sqrt{[L_{tank}C_{tank}]}$, the ideal tank impedance is infinity. Assuming that the load equivalent resistance is large and that the load capacitance is included in C_{tank}, the loss of the tank will determine the voltage conversion gain of the circuit at resonance. The output voltage magnitude at that frequency, V_o, will be proportional to the equivalent parallel resistance, R_p, of the tank at resonance. R_p models the tank loss and is given by the quality factor, Q, of the tank. Therefore, V_o is computed as follows:

$$\begin{aligned} V_o = v_o(\omega_{tank}) &= -R_p i_D(\omega_{tank}) \\ &= -i_D(\omega_{tank})\frac{\omega_{tank}L_{tank}}{Q}(Q^2+1) \ , \end{aligned} \quad \text{(Eq. 3.18)}$$

$$\omega_{tank} = \frac{1}{\sqrt{L_{tank}C_{tank}}}$$

The voltage conversion gain, G_{conv}, of the frequency doubler is the ratio of V_o and $2V_i$. The tank resonance is designed to match the fundamental LO frequency, $\omega_{tank} = \omega_{LO}$

$= 2\omega_s$. The magnitude of $i_D(\omega)$ at this frequency is simply the second harmonic coefficient, a_2, of the Fourier series of $i_D(t)$, which can be solved from the expression of (Eq. 3.16). The conversion gain will therefore be as shown in (Eq. 3.19).

$$G_{conv} = \frac{V_o}{2V_i} = -a_2 \frac{\omega_{LO} L_{tank}(1+Q^2)}{2QV_i}$$

$$\text{where, } a_2 = \frac{\mu_n C_{ox}}{12\pi V_i}\frac{W}{L}\left(V_K(2V_K^2 - 5V_i^2)\sqrt{1-\frac{V_K^2}{V_i^2}} + 3V_i^3 cos^{-1}\left(\frac{V_K}{V_i}\right)\right) \quad \text{(Eq. 3.19)}$$

$$G_{conv}|_{V_K=0} = -\frac{u_n C_{ox}\omega_{LO} L_{tank} V_i (1+Q^2)}{16Q}\frac{W}{L}$$

The factor of 2 in the denominator of G_{conv} accounts for the differential to single ended voltage conversion. Q is the quality factor of the inductor, L_{tank}. Using (Eq. 3.19) and setting V_i*=0.5 V*, *Ltank=921 pH*, *Q=10*, W_d/L_d*=45/0.18*, and $\mu_n C_{ox}$*=310.6* $\mu A/V^2$, a voltage conversion gain of -1.45 V/V will be computed. This assumes that the FETs are biased near threshold, or V_K =0. For the sub-harmonic quadrature generator, ω_{LO} is 9.4 GHz.

It is important to note that the conversion gain given by (Eq. 3.19) depends on V_i because the FET saturation current has a square law dependence on the gate voltage. As a result, the conversion gain will increase with the input level. This linear increase in gain will continue until velocity saturation occurs in the FET channels. In the short channel limit of the saturation current, I_D will become:

$$I_D(t) = \frac{\mu_n C_{ox}}{2} E_{sat} W (V_i cos(\omega_s t) - V_k) u\left[cos(\omega_s t) - \frac{V_k}{V_i}\right] + \frac{\mu_n C_{ox}}{2} E_{sat} W (-V_i cos(\omega_s t) - V_k) u\left[-cos(\omega_s t) - \frac{V_k}{V_i}\right] \quad \text{(Eq. 3.20)}$$

As in (Eq. 3.15), (Eq. 3.20) is the sum of the square law expressions for the saturation drain currents of M_1 and M_2, but in the limit of velocity saturation[25]. In this limit, the voltage conversion gain can be shown to be:

$$G_{conv}|_{V_K=0} = -\frac{u_n C_{ox} \omega_{LO} L_{tank} E_{sat} W (1 + Q^2)}{6\pi Q} \quad \text{(Eq. 3.21)}$$

(Eq. 3.21) is derived following the same procedure as (Eq. 3.19). Given that $E_{sat}=4x10^6$ *V/m*, (Eq. 3.21) yields a voltage conversion gain of -1.77 V/V. This gain is not dependent on V_i. (Eq. 3.21) places an upper limit on the attainable gain with respect to increases of V_i. Achieving that limit requires large gate overdrive voltages, approximately 0.7 V, which can be reached in the current implementation with sufficient sub-harmonic LO reference input power.

The frequency doubler exhibits the high impedance output encountered with common source stages. The polyphase filter presents a low impedance input. In order to use both of these stages together, a buffer amplifier is necessary that presents the appropriate impedance to both circuits. Transistors M_3, M_4, and M_5, as shown in Figure 19, make up this circuit. It is a basic source follower that presents a high impedance at the input, by virtue of the gate of M_3, and a low impedance output, by virtue of the drain-source conductance of M_3. The resistance R determines the bias current for the current mirror consisting of M_4 and M_5. The device size for the source follower has been

optimized, given a 1.5 mA bias current, for a best match between the frequency doubler and polyphase filter. In simulation, the maximum output voltage from the quadrature outputs of the polyphase filter occurred with a device size of 60µm, corresponding to an output impedance of approximately 60 Ω.

3.2.3 Polyphase Filter

As represented by the third stage of the block diagram of Figure 3, a polyphase filter is used to generate quadrature from the recovered fundamental LO. This implementation uses a single stage RC-CR polyphase filter as shown in Figure 20. The passive topology is preferred to active and switched-capacitor polyphase circuits when the frequency of operation is high, near RF[11]. In the figure, the single-ended input, PF_in, is provided by the low impedance output of the preceding source follower stage. Two single-ended quadrature outputs, Inj_I and Inj_Q, are available from the network to injection-lock the LC oscillator stages that follow.

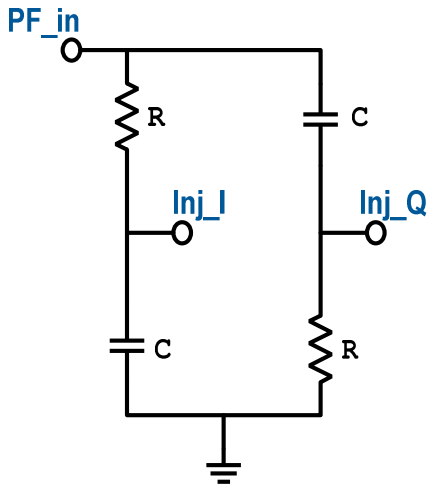


Figure 20. Single stage polyphase filter network.

The center frequency, ω_0, of the poly phase filter can be determined by the simple relation:

$$\omega_0 = \frac{1}{RC} \qquad \text{(Eq. 3.22)}$$

At this center frequency, the best quadrature matching will be observed. Outside of the center frequency, perfect quadrature phase(assuming perfect component tolerance) will still be maintained, however amplitude mismatch between the quadrature outputs will begin to develop. This amplitude mismatch will define the usable bandwidth of the poly-phase filter and is one reason that multi-stage polyphase filters are usually used in favor of single-stage filters. The use of injection-locked LC oscillators in the later stages of this work conveniently corrects for amplitude mismatch, as described in Section 3.4, effectively extending the bandwidth so that a single stage polyphase network is a reasonable option.

Process variation can also affect the quality of the amplitude and phase mismatch of the polyphase filter outputs, even at the center frequency. Adding additional filter stages will have the benefit of improving the process-related amplitude mismatch, but this technique generally offers no reduction in quadrature phase mismatch [11]. Given that the LC oscillators correct for amplitude mismatch, there is no reason to increase the number of stages beyond one. Each stage would also increase the insertion loss by at least 3dB, and such a power loss cannot be easily tolerated by the sub-harmonic architecture. For these reasons, a single stage polyphase filter has been chosen for the design.

In the fabrication of the polyphase filter, small values must be used for the resistors. This prevents the need for unreasonably small capacitor values. Capacitors that are too small will not provide reasonable tolerances and may not be possible to realize with the process. The design has been implemented with an R of 120Ω and C of 144 fF, for a center frequency of 9.4 GHz. The values chosen provide allow the polyphase filter to be implemented with resistors and capacitors of similar physical size. The low resistance dictates a low input impedance and justifies the need for the source follower that follows the frequency doubler output.

The layout for the polyphase filter is shown in Figure 21 at the extreme right of the figure. The resistors are K1 BEOL resistors, which are available as part of the IBM 7RF process and are described in the appendix to this thesis. These resistors feature low parasitic capacitance to substrate. Such capacitance increases the loss through the polyphase filter and causes quadrature error at high frequencies[12]. This loss is very noticeable if common diffusion resistors are used. The K1 BEOL resistors also have a low sheet resistance, allowing the small resistances in the polyphase filter to be implemented with large area, improving the overall tolerance. These resistors provide the best tolerance and match of all the resistors in the 7RF process. The capacitors are implemented as IBM vertical-natural capacitors, which are made up of interdigitated fingers on the various metal layers. These capacitors have lower capacitance density than other options, allowing the 144fF capacitors to be implemented with reasonable tolerance. In fact, the tolerance is better than any other capacitance options modeled by IBM. The K1 BEOL resistors have a nominal 0.06% matching tolerance and 8%

resistance tolerance. The vertical-natural capacitors, as implemented in the polyphase filter layout, have a matching tolerance of approximately 0.2% and an overall value tolerance of 11%.

3.2.4 Layout

The figure below depicts the layout of circuits discussed in section 3.2. Refer to Figure 7 for a complete layout.

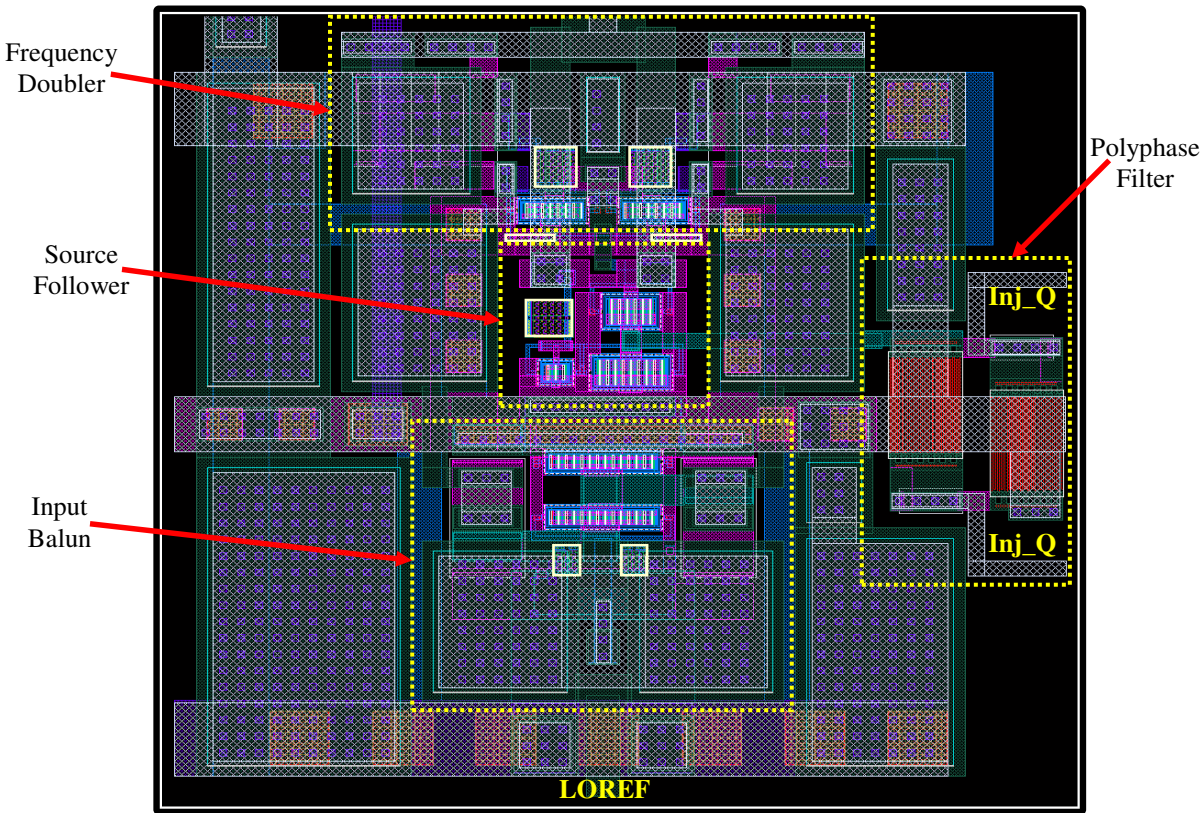


Figure 21: Layout of the input balun with coupling capacitors(bottom center), source follower(center), frequency doubler(top center) and polyphase filter(far right). The spiral inductor for the tank of the frequency doubler tank is not shown. Large capacitors for supply decoupling are seen throughout. This image corresponds to a 160µm by 150µm area.

3.3 Quadrature LO Generator with Fundamental LO Reference

The topology for the fundamentally-referenced quadrature generator, as shown in Figure 4 and Figure 6, contains a polyphase filter and differential buffer amplifiers. These circuits will be addressed with more detail in the following sections. Discussion of the LC oscillators, used for boosting the LO level and amplitude-limiting, is left for section 3.4.

3.3.1 Polyphase Filter

The input stage to the non-doubling architecture of Figure 4 is a double stage polyphase filter network as depicted in Figure 22 below. Unlike the sub-harmonic system, frequency doubling is not required to recover the LO fundamental prior to generating quadrature and this allows the polyphase network to be the input stage. The input impedance, output impedance, and the impedances of intermediate stages of the polyphase filter network must be low, in general, to keep the loss due to parasitics minimal at the relatively high frequencies of interest[12]. This is convenient for the 50Ω source impedances available with measurement instrumentation. Depending on the method of LO signal distribution throughout the phased array, a buffer amplifier may be desired before the polyphase filter in a final implementation.

Given that loss in the polyphase network is unavoidable, its use as the first stage is also advantageous because the loss can be overcome by increasing the power from the source. That increase is not limited by the saturation of a preceding active stage, as in the circuit of 3.2.3. The difference can be seen in the plots of locking range, in sections 4.2 and 4.3, where the locking range of the sub-harmonic circuit eventually flattens out with

increasing LO reference power. Having more loss headroom also allows a polyphase network with differential in-phase and quadrature outputs to be used. In this way, the injection locking pair of the LC oscillators can be differentially driven, increasing the achievable input signal strength to that pair. The LC oscillators are discussed in section 3.4.

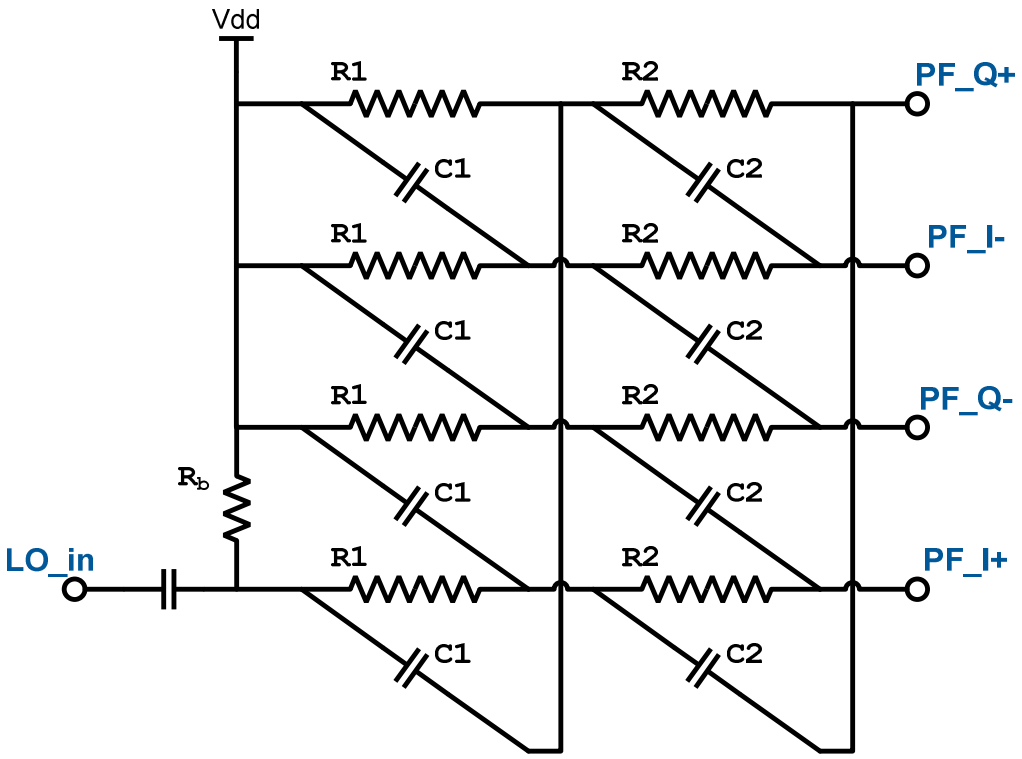


Figure 22. Double stage polyphase filter. R_b sets a DC bias on the decoupled input. This network provides differential I and Q outputs.

The polyphase network pictured in Figure 22 has two stages. Each additional stage that is added will result in a weaker output signal but can improve the overall bandwidth of the network. The use of two stages for broader bandwidth simplifies the polyphase filter design in that it will be less of a factor in the alignment of multiple tuned

stages. The resulting design, which requires four times the area of the single stage network, makes use of space previously dedicated to the frequency doubling circuits and buffer amplifiers of the sub-harmonic architecture.

The two stages of the polyphase network are stagger-tuned to realize a more broadband response. The best amplitude match will occur at the corner frequencies and the greatest amplitude divergence will occur at the geometric mean of the corner frequencies. These frequencies should be chosen far enough in either direction from the desired center frequency that the bandwidth will be large. They must however, be close enough to keep the amplitude mismatch tolerable. In this design, because of the LC oscillators, this mismatch can be larger than usual so a fairly broadband network can be realized. The individual center frequencies of the two filters, which set the pole frequencies of the entire network, are given by:

$$\omega_1 = \frac{1}{R_1 C_1} \qquad \omega_2 = \frac{1}{R_2 C_2} \qquad \text{(Eq. 3.23)}$$

In this design, R1=113Ω, C1=168fF, R2=113Ω, and C2=135fF. This sets the two corner frequencies at 8.4 GHz and 10.4 GHz. R_b is a 3kΩ resistance that ensures the PF_I+ output is biased at V_{DD}, as are the other outputs.

Although the multi-stage filter uses more components and provides better bandwidth performance, the considerations in terms of circuit layout and matching tolerances are the same as they are for the single stage polyphase filter. Phase mismatch from component variation does not improve with additional filter stages[12] and parasitic

capacitance still affects the high-frequency cutoff of this circuit. Therefore, K1 BEOL resistors and vertical natural capacitors were used in this layout and the greatest amount of chip area that could be afforded was used to improve overall component tolerances.

3.3.2 Differential Amplifiers

In the fundamental LO architecture, two amplifiers have been inserted between the polyphase filter and the injection locked oscillators. There is a dedicated amplifier for each of the in-phase and quadrature channels, as shown in Figure 4. The amplifiers are not strictly required for the architecture but they increase the signal levels available for injection locking and consequently reduce the reference LO input power requirements. The amplifiers make use of available space in the layout after having removed the frequency doubling circuit from the sub-harmonic implementation. A more optimal design may exclude these amplifiers altogether and thereby reduce the space requirement. By preserving the same layout dimensions in this implementation, it was possible to test the sub-harmonic and fundamental architectures with the same test structures.

The amplifiers are basic CMOS differential pairs loaded by LC tanks to peak the gain at the LO frequency and are shown below in Figure 23. These amplifiers provide a voltage gain of about 1.9 V/V in simulation. They also effectively buffer the polyphase network by loading its outputs with less capacitance than the LC oscillators would present. The actual improvement to the injection locking voltage is about four times what the polyphase filter would achieve alone.

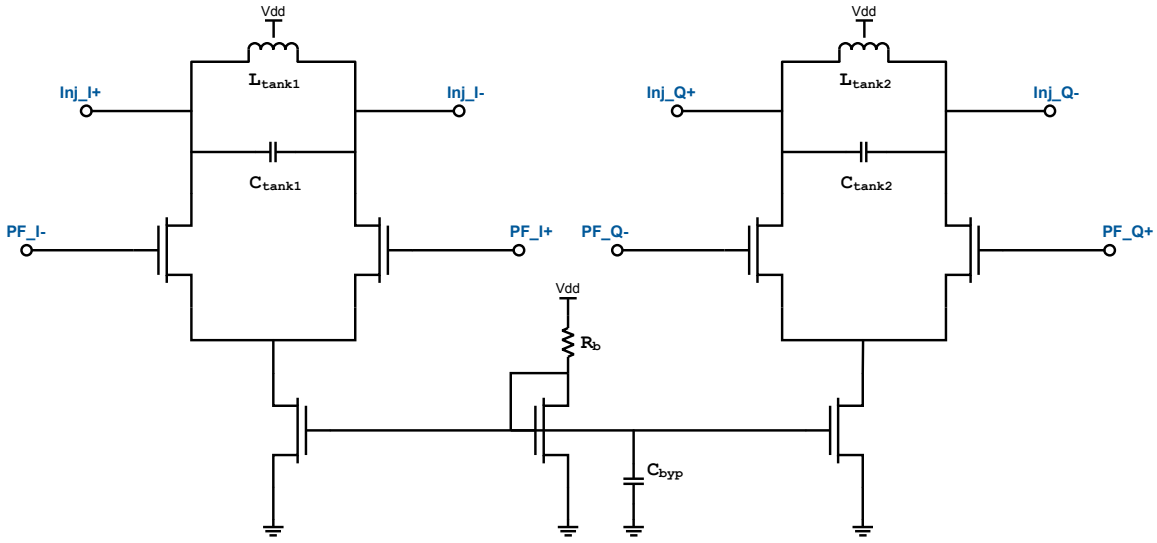


Figure 23. Two differential amplifier stages.

A current mirror biases each amplifier such that each pair draws 2 mA of DC current. Each FET in the pair is a 35um device with 10 fingers. The gates are biased at V_{DD} by the polyphase filter outputs. Given the process parameters from MOSIS, (Eq. 3.11), and the 1mA per FET current bias condition, the transconductance of each device is *gm=11mS*. The resonant frequency of the tank, set by C_{tank} and L_{tank}, is 9.4 GHz. C_{tank} includes the parasitic capacitance of the loading stages(the injection-locked oscillators). The tank inductance is determined by a center-tapped symmetric planar inductor with a total inductance of 1.58 nH. Each branch of a single differential pair is effectively loaded by an LC tank with the values $L=L_{tank}/2=790\ pH$ and $C=2C_{tank}$. The voltage gain of the differential pair, assuming a perfect current bias but including C_{gs} and C_{gd} of the transistors in the pair is:

$$A_V = \frac{\omega_0 L(1+Q^2)(g_m - j\omega_0 C_{gd})}{Q + j\omega_0^2 L(C_{ds} + C_{gd})(1+Q^2)} \qquad \text{(Eq. 3.24)}$$

(Eq. 3.24) assumes a tank parallel resistance at resonance related to inductor Q in the same manner as for the tank of the frequency doubler of section 3.2.2. With a simulated inductor Q of 13.5, a calculated C_{gd} of 60fF, and neglecting C_{ds}, the calculated gain of the amplifier is 2.97 V/V. C_{gd} is calculated from the oxide capacitance and overlap capacitance parameters of the process.

3.3.3 Layout

The figure below depicts the layout of circuits discussed in section 3.3. Refer to Figure 6 for a complete layout.

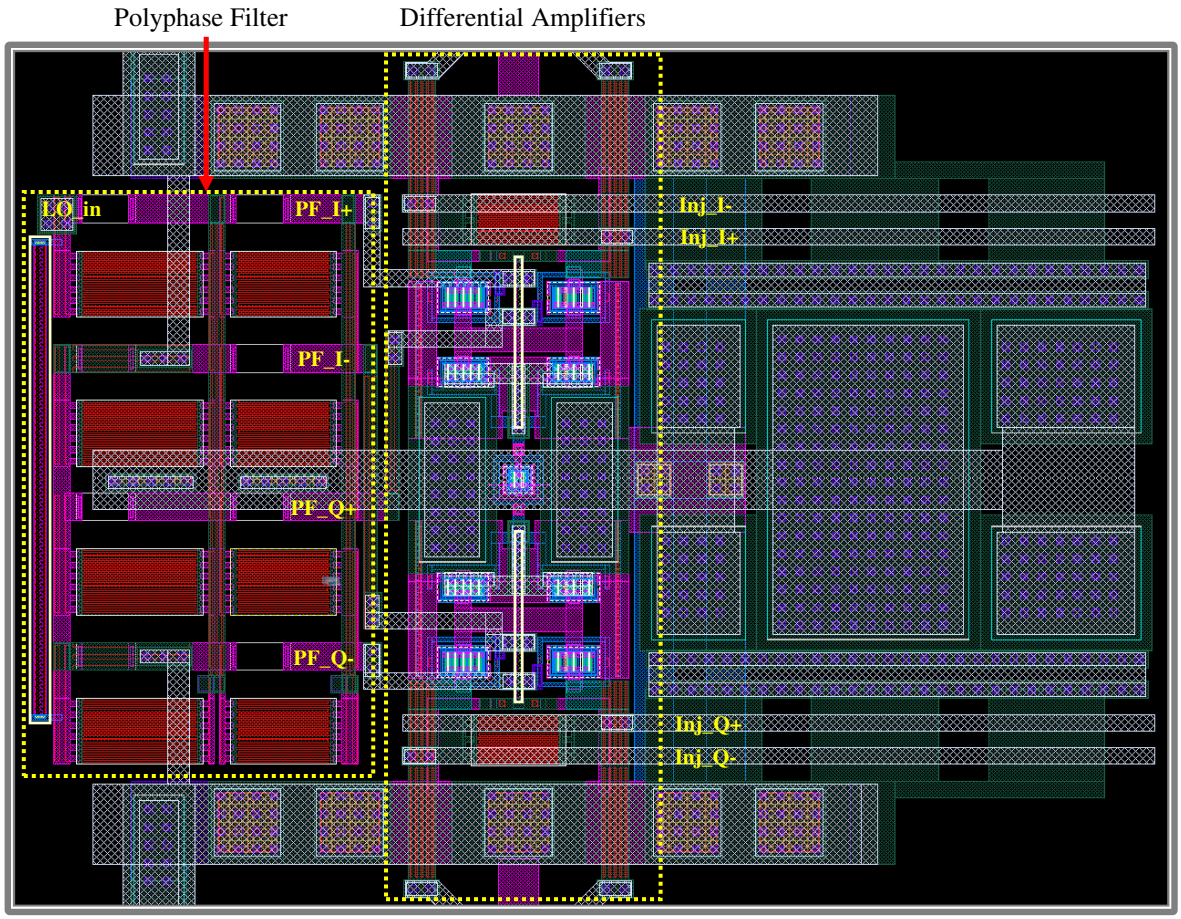


Figure 24. Layout of the double stage polyphase filter(left), differential amplifiers(center), and decoupling capacitors (right). The symmetric spiral inductors for the tanks of the differential amplifiers are not shown.

In the layout of Figure 24, the eight large blocks visible to the far left are the interdigitated capacitors of the double stage polyphase filter. To the right of the polyphase filter, and near the center of the layout, nine FETs can be counted. Of these nine, the centermost FET is a current mirror that sets the gate bias for two adjacent transistors above and two below that draw the tail currents through the four remaining transistors that comprise the differential pairs. A number of large MIM capacitors fill the remaining area to the right and are used for supply decoupling. The symmetric spiral inductors for the differential pairs can be seen in Figure 6.

3.4 Injection-Locked LC Oscillators

Injection-locked LC oscillators are used in both the fundamental and sub-harmonic methods of quadrature generation, as shown in Figure 3 and Figure 4. These circuits are the final stages in the quadrature generation chain and are used to drive the LO ports of the mixers with large amplitude. In the circuits having a fundamental LO reference, the oscillators are injection-locked by the buffered quadrature outputs of an RC-CR polyphase network. In those having the sub-harmonic reference, the oscillators are injection-locked by the polyphase network outputs directly.

The motivation and background for the use of LC oscillators and injection-locking is discussed in Section 3.4.1. Section 3.4.2 describes a method of coupling the two LC oscillators that enforces quadrature by design. Every implementation of the quadrature generation circuitry requires adjustment of the oscillator tail current and the ratios of the injection or coupling current to that tail current, as set with appropriate transistor sizing. These differences are discussed in Section 3.4.3.

3.4.1 Background

At its resonant frequency and with adequate Q and DC bias, an integrated LC oscillator can provide the large output drive capability needed to drive the LO ports of a passive mixer. If such an oscillator is also injection-locked, the oscillation frequency and phase of the LC oscillator will follow that of the injected signal. The LC oscillator will essentially behave as a narrow-band limiting amplifier to the injection signal source. When viewed as an amplifier, the injection-locked oscillator provides a high gain in a single stage. It is an effective limiter due to the weak dependence of the oscillation

amplitude on the injection-locking signal. In the application for this thesis, the limiting behavior is needed to equalize the conversion gain of the IQ mixer over varying input levels of the LO reference. Amplitude mismatch originating from the RC-CR polyphase filters is also corrected by the limiting.

LC oscillators are preferred in many applications due to their low power or low phase noise performance versus other topologies [17]. Phase noise performance will suffer if the quality factor of the LC tank is low, which is often the case with integrated solutions, and can be compensated for with increased power consumption [19]. When present, injection-locking can improve phase noise performance if the injection-locking signal is itself a low noise signal. This is treated in detail in [18].

A pair of injection-locked LC oscillators, as implemented for this thesis, is shown in Figure 27. Each oscillator provides differential outputs. Aside from the tank Q, the oscillator drive capability will depend on the signal current switched though the cross-coupled FET pairs, M_{osc1}/M_{osc2} in one oscillator, and M_{osc3}/M_{osc4} in the other. The amplitude of that current will be proportional to the transconductance of the cross-coupled devices, which suggests that the FETs must be as wide as possible and that the tail bias current to each FET pair must be sufficiently large. The tail bias currents will dictate the power requirement of the circuit. Also shown in Figure 27 are the injection-locking pairs of FETs. Injection-locking is introduced to the LC oscillator by the addition of a second differential pair with gates that are driven by the injection-locking signal source. These transistor pairs are marked as M_{inj1}/M_{inj2} and M_{inj3}/M_{inj4}. A similar set of

cross-coupled and injection locking FET pairs can be seen in Figure 28. This figure provides the schematic for the quadrature-coupled and injection-locked LC oscillators that were implemented for this thesis and that are described in section 3.4.2. The topology is the same as Figure 27, with the exception of differential pairs added for quadrature coupling. The FET device sizing for the four separate implementations in which these two oscillator topologies were used is given by Table 2 and Table 3.

Circuit		**Individual FET Width (µm)**		
LO Reference	Oscillator Type	Cross-Coupled FET Pairs, M_{osc1-4}	Injection-Locking FET Pairs, M_{inj1-4}	Quadrature-Coupled FET Pairs, M_{C1-4}
Fundamental, 9.4 GHz	Injection-Locked	60	21	-
Fundamental, 9.4 GHz	Injection-Locked, Quadrature-Coupled	36	21	21
Sub-Harmonic, 4.7 GHz	Injection-Locked	40	30	-
Sub-Harmonic, 4.7 GHz	Injection-Locked, Quadrature-Coupled	35	100	9

Table 2. Size of the devices used in differential pairs that make up injection-locked and, in some cases, quadrature-coupled oscillators implemented for this thesis. Refer to Figure 27 or Figure 28 for the device designations. Channel length is 180 nm for all devices.

Circuit		Individual FET Width (μm)				Total Current (mA) (Includes M_{ref})
LO Reference	Oscillator Type	M_{b_osc1-2}	M_{b_inj1-2}	M_{b_C1-2}	M_{ref}	
Fundamental, 9.4 GHz	Injection-Locked	120	42	-	20	9.5 mA
Fundamental, 9.4 GHz	Injection-Locked, Quadrature-Coupled	100	42	40	20	10.7 mA
Sub-Harmonic, 4.7 GHz	Injection-Locked	80	116	-	20	11.1 mA
Sub-Harmonic, 4.7 GHz	Injection-Locked, Quadrature-Coupled	60	93.6	10	16.4	11 mA

Table 3. Size of the devices used for the tail current bias of various differential pairs that make up injection-locked and, in some cases, quadrature-coupled oscillators implemented for this thesis. Refer to Figure 27 or Figure 28 for the device designations. Channel length is 180 nm for all devices. The total current drawn to supply all the tail bias currents for each oscillator is also shown.

The AC signal current driven by an injection-locking pair of FETs in an injection-locked LC oscillator must be a sizeable fraction of the current driven by the cross-coupled(oscillating) pair in order to allow injection-locking over a reasonable range in frequency around the oscillator resonant frequency. Process variation, particularly the variation in the resonant frequencies of the oscillators, dictates the necessary injection-locking range. The locking range must be greater than the expected spread of resonant frequencies. This was roughly determined through Monte-Carlo simulation with IBM foundry supplied models. Given approximately 150 to 200 MHz of range, a test case for a single injection-locked LC oscillator repeatedly locks, within 2 standard deviations of the sample size, to the target center frequency. The range can be affected by varying the power from the LO reference and by varying the relative sizing of the injection locking FET pairs and the amplitude of their tail current bias. The nominal reference LO input

power for systems that injection-lock with a doubled version of that reference is 1 mW. For those that use the reference at its fundamental, it is 0.1 mW.

The locking range for an injection locked oscillator can be calculated with the following equation, which is derived in [18]:

$$\text{Lock Range} = \frac{\omega_0}{Q}\frac{1}{\sqrt{\left(\frac{4i_{osc}}{\pi i_{inj}}\right)^2 - 1}} \quad \omega_0 = \frac{1}{\sqrt{L_{tank}C_{tank}}} \qquad \text{(Eq. 3.25)}$$

In the above equation, Q is the quality factor of the LC tank. The current, i_{osc}, is the AC current magnitude(near the resonant frequency) through either branch of the cross-coupled FET pair. i_{inj} is the AC current magnitude through a branch of the injection-locking pair. As an example, a branch of the cross-coupled pair of either LC oscillator in the fabricated fundamentally-referenced circuit with uncoupled oscillators has a typical AC current magnitude, near the LO reference frequency, of 3.3 mA. The plot in Figure 25 shows, based on (Eq. 3.25), how the locking range varies with the injected AC current magnitude, if it is increased from zero to 1.5 mA. The horizontal axis of this plot is linear with i_{inj}^2 to provide a more direct comparison to the locking range plots based on simulation and measurement in CHAPTER 4 and CHAPTER 5, which are related to the input power of the LO reference. The trend for the locking range provided by (Eq. 3.25) in [18] is in very good agreement with these results. The same trend will be observed even in cases where quadrature coupling is present.

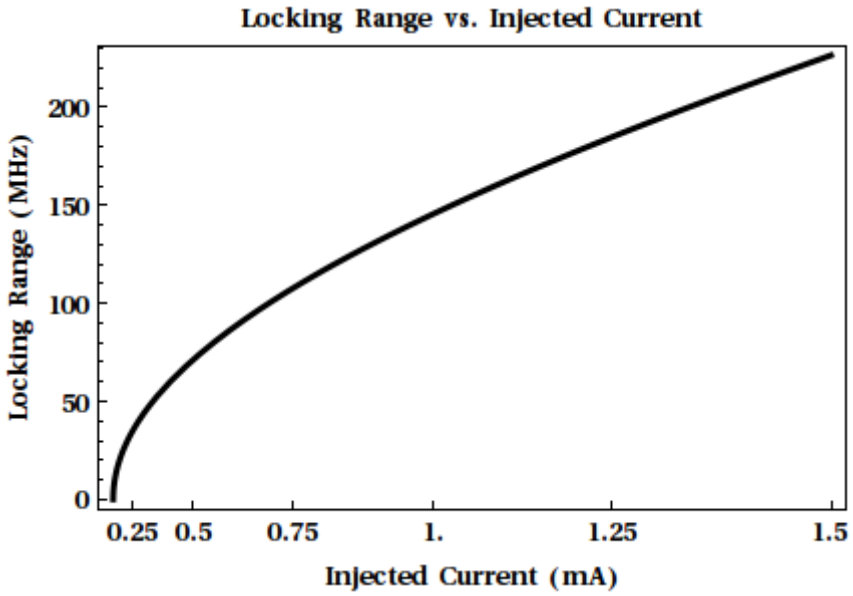


Figure 25. The range in frequency over which injection locking is possible, for an injection locked LC oscillator, as the injected current is varied. The horizontal axis lists the injected current, $i_{inj,}$ in mA, but is linear with i_{inj}^2. Therefore, the displayed trend is representative of the locking range with respect to the power of the injected signal. The oscillator current, $i_{osc,}$ is 3.3 mA.

3.4.2 Quadrature Coupling

This thesis examines quadrature coupling of the two LC oscillators, as shown in Figure 28. Such coupling will generate quadrature by design. In the figure, the labels I+, I-, Q+ and Q- indicate the coupling lines. This configuration requires an additional differential pair, like the ones used for injection locking, to be added to each LC oscillator. In fact, quadrature coupling can be treated as a particular method of injection locking[18], where each oscillator is injection-locked with the outputs from the other oscillator. It is important to point out that the quadrature-coupled oscillators of this thesis are still injection-locked by externally generated signals, as was the case with the

uncoupled oscillators, and that quadrature coupling is simply an addition to the uncoupled architecture.

Noting that the quadrature-coupled oscillators are also injection-locked by signals already in quadrature, the outputs of a polyphase network, coupled-oscillator quadrature generation seems redundant. The additional injection-locking primarily ensures phase coherence with the reference LO. The polyphase network provides even injection locking signals for both oscillators, in terms of amplitude and appropriate quadrature phase shift. When the oscillators are locked, the injection-locking currents from the polyphase network will simply add to the locally generated quadrature. This thesis examines how the presence or absence of quadrature coupling in the final oscillator stages affects the quality of the final output quadrature.

As operating frequency increases, the various quadrature generation schemes become more difficult to implement or can not be realized. Polyphase filters will lose quadrature accuracy or require increased power consumption[16]. LC oscillators allow load capacitances and parasitic capacitances to be lumped into the total tank capacitance and provide a narrowband solution that can achieve a high frequency of operation[16]. When coupling is introduced that provides quadrature by design rather than by careful tuning, the implication is that quadrature-coupled LC oscillators can be extended more reliably into higher frequencies. If that is the case, the quadrature oscillator may compensate for mismatch in the polyphase filter outputs that the uncoupled oscillators would not compensate. Figure 26 presents Monte-Carlo simulation comparing the

quadrature accuracy for quadrature-coupled and uncoupled injection-locked LC oscillators. For the uncoupled oscillators, the variation is approximately 6° within two standard deviations from the nominal. This variation is 3.5° in the quadrature-coupled case, indicating that there is a benefit in quadrature phase performance. Measurement, CHAPTER 5, appears to show the same benefit. A drawback with the coupled oscillators is a nominal amplitude mismatch that is much greater than in the uncoupled case. This is likely a result of the non-ideal and asymmetric coupling lines between the two oscillators. Although the amplitude mismatch in the uncoupled case is quite good, measurement of the fabricated devices shows an amplitude mismatch that is greater than anticipated.

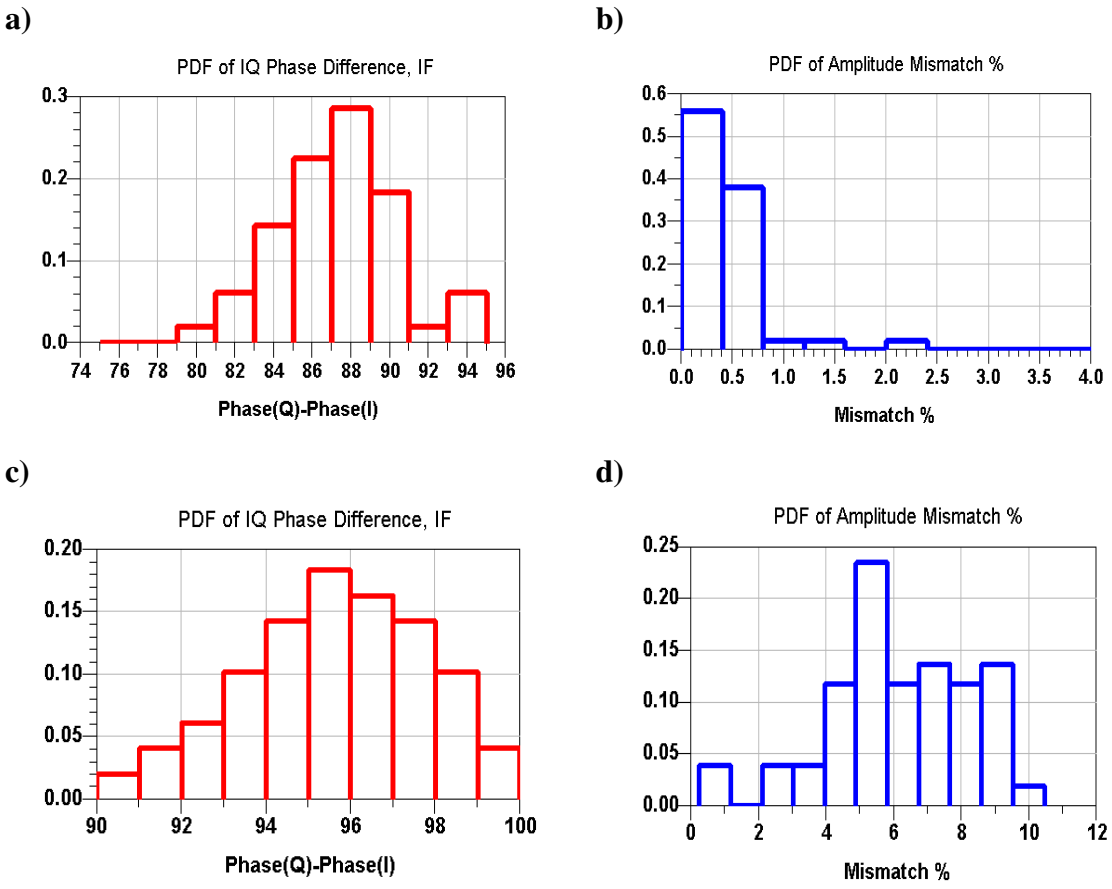


Figure 26. Simulated PDFs for quadrature phase and amplitude mismatch for injection-locked(a,b) and injection-locked, quadrature coupled(c,d) LC oscillators. These results are based on fully-extracted layouts of the two oscillator variants.

Quadrature coupled LC oscillators can have two stable operating frequencies. Assuming the coupling lines are ideal wires, these are derived in [18] as:

(Eq. 3.26)

In the above equation, i_{osc}, Q, and ω_0 represent the same quantities that are found in (Eq. 3.25) and are common to both LC oscillators in the configuration. i_c represents the

AC magnitude, at the steady-state oscillation frequency, of the current through an FET of the coupling pair in either of the LC oscillators. The angular frequency, ω_1, is considered that of the first operating mode and ω_2 is the second mode. The two operating points exhibit reversed lag-lead relationships for the quadrature outputs. In either case, the absolute phase difference remains 90 degrees.

The quadrature-coupled oscillator can start up in either mode of operation given by (Eq. 3.26), although, as a result of complex circuit non-idealities, such an oscillator will usually reliably settle into the second mode[18]. Still, this phenomenon has remained a source of unpredictable start up in many cases[18]. The polyphase network, via injection locking, enforces a certain lag-lead relationship for the output quadrature of the coupled oscillator implementation of this thesis. Each of the two lag-lead possibilities is particular to a specific operating point, ω_1 or ω_2, and, therefore; either stable operating frequency can be chosen depending on the connection of the polyphase filter. This behavior was observed in simulation as well and effectively guarantees reliable start up into a particular mode, setting the center frequency for the overall locking range. Given the choice of operating point, the second mode is more desirable and is the one chosen for this thesis. ω_2 corresponds to a higher frequency of operation for a particular tank capacitance and inductance. If the tank capacitance is kept relatively constant the second mode will allow the target oscillation frequency to be achieved with the largest possible inductance, improving the overall tank Q and increasing the output amplitude of the oscillator.

A difficulty with the architecture of the quadrature coupled oscillator is that the quadrature coupling can not be done perfectly symmetrically, leading to nominal phase or amplitude error. Process variation in the LC tank also contributes to these errors and is estimated in [18]. These issues are also discussed in section 5.2 of this thesis.

LC oscillators provide excellent phase noise when compared to other free-running oscillator topologies, especially those that generate quadrature[17]. LC oscillators that are quadrature-coupled will trade off phase noise performance for quadrature accuracy but will, in general, still exhibit the superior phase noise of the LC oscillator[26]. The oscillators of this thesis are also injection-locked to an external reference. Such injection-locking can equalize the local phase noise to that of the LO reference, resulting in an improvement if the reference is itself a low phase noise source[15].

3.4.3 Variations

There are four possible variations of the injection-locked LC oscillator in the circuits implemented for this thesis. For each LO reference type, fundamental or sub-harmonic, the circuit is built with both uncoupled and quadrature-coupled LC oscillators, as shown in Figure 27 and Figure 28. In the case of the sub-harmonic referenced circuits, the polyphase filter supplies only single ended outputs. As a result, the negative differentials of the injection-locking pairs in the oscillators are tied to V_{DD}(1.8 V). Those signals are Inj_I- and Inj_Q- in Figure 27 and Figure 28. Device sizes are also specifically tuned for each circuit and are summarized in Table 2 and Table 3. The result is a total of four slightly different injection-locked LC oscillator pairs.

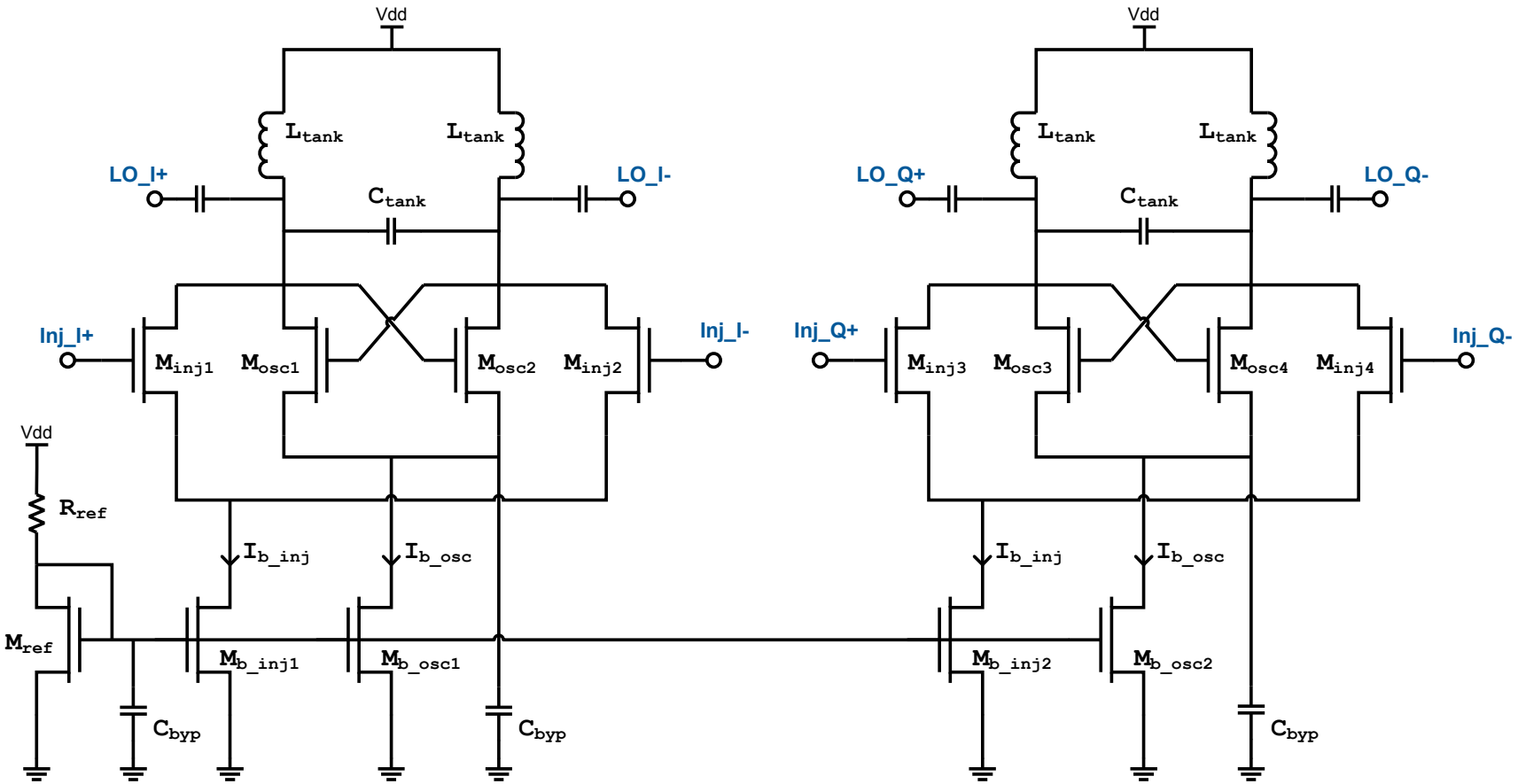


Figure 27. A pair of injection-locked LC oscillators. One oscillator is locked to an in-phase signal and the other to a quadrature-phase signal. The bypass capacitor connected to the sources of the cross-coupled pair, C_{byp}, increases the output voltage swing.

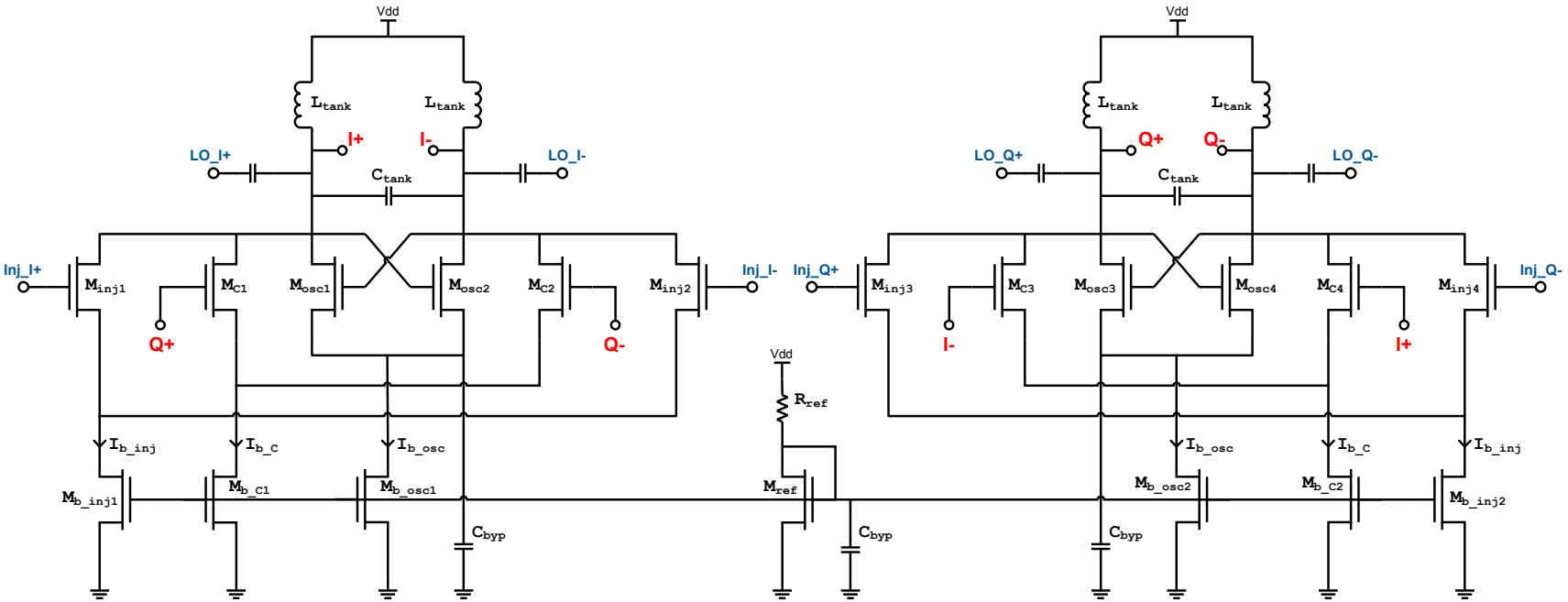


Figure 28. Injection-locked and quadrature-coupled LC oscillators. These oscillators produce quadrature and are injection-locked by signals already in quadrature.

3.4.4 Layout

Layout images of the injection-locked oscillators are shown below. The top halves of the pictured layouts depict one oscillator and the bottom halves the other. With the exception of the coupling lines in the quadrature-coupled oscillators, the two oscillators are mirror images of one another.

Figure 29 is the quadrature-coupled implementation of the oscillators. The coupling lines are clearly visible on this layout and are routed on two layers. The top most layers are used for this routing to reduce the parasitics that will be unequally introduced for each of the vertically asymmetric coupling lines. An additional six transistors, when compared the uncoupled, Figure 30, oscillators can also be seen. These transistors are the quadrature-coupling pairs along with their tail current biases. The transistor in the center of Figure 29 or Figure 30 is the current mirror reference for all of the tail current biases in the oscillator circuit.

The tank capacitance for an oscillator is made up of the parasitic capacitance of the planar inductors, FET drains and routing. It also includes an interdigitated capacitor between the two differentials. This type of capacitor is discussed in the appendix to this thesis and exhibits better mismatch tolerance than the MIM capacitors in the 7RF process. MIM capacitors are also not suitable for implementing the small capacitances needed for the tank at 9.4 GHz.

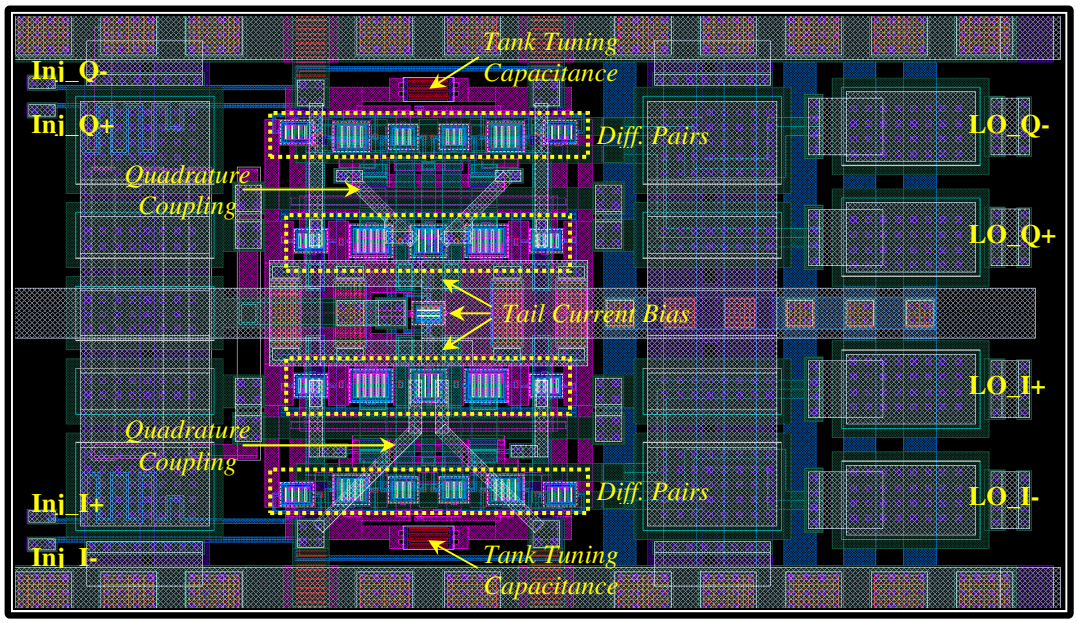


Figure 29. Layout of the injection-locked and quadrature-coupled LC oscillators. Four planar inductors are not shown. The top half of the drawing is one oscillator and the bottom half is the second.

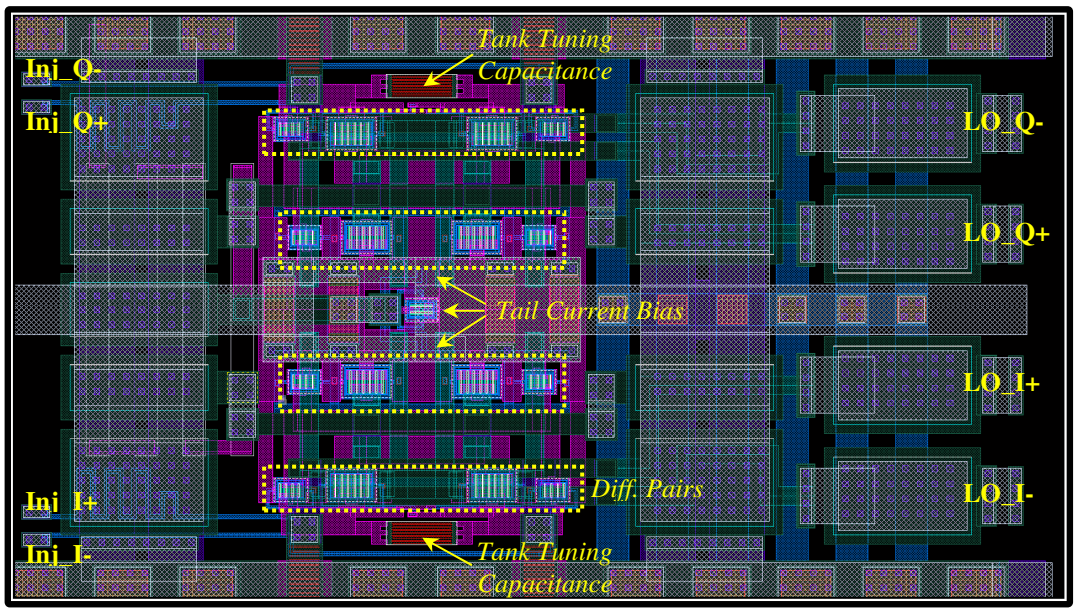


Figure 30. Layout of the injection-locked LC oscillators. There is no coupling between the two oscillators in this layout. The four planar inductors of the tanks are not shown.

CHAPTER 4

SIMULATION

This chapter presents simulation results for the various topologies of the quadrature conversion system that has been discussed. Section 4.1 provides details of the simulation procedure. Sections 4.2 and 4.3 summarize results for the systems with a fundamental reference LO and sub-harmonic reference LO, respectively.

4.1 Overview

IBM supplied device models and Agilent ADS are used to verify functionality, following netlist extraction, of the four quadrature conversion circuit variants. Simulation results for these systems are provided in the following sections. Analyses of both the uncoupled, Figure 27, and coupled, Figure 28, LC oscillator variants with both sub-harmonic and fundamental LO reference architectures are included.

The passive mixers of these circuits are intended to be driven by an integrated LNA or phase-gain control IF circuitry. The fabricated versions of the circuits for this thesis have these ports connected to bondpads. The bondpads will increas loss to some degree and the difference between the two is simulated and a comparison provided in the following sections. Detailed simulation plots will be shown for the circuits without bondpads, however, all other operating conditions remain the same and the trends when bondpads are included can be drawn directly from the summarized comparisons.

Nominally, many of the simulated performance parameters, such as conversion gain, certain non-linearities, and RF and LO feedthrough are predominantly features of the passive mixers. Other parameters, such as the amplitude and phase accuracy of the quadrature, are dependent on the polyphase filters and LC oscillator circuits.

Parasitic extraction of circuit layouts was performed with the Cadence QRC tool and associated IBM design kit. The design kit supports resistance and capacitance extraction of the entire layout. Some filtering and reduction was turned on to keep the netlist sizes manageable because an unfiltered extraction can result in tens of thousands of simulation components. Specific inductances were characterized by Sonnet and were included in the simulations as S-parameter blocks. These include the planar inductors in the tanks of the injection-locked LC oscillators and of the frequency doubler.

The majority of the analyses for the complete extracted systems were done with swept transient simulation trials in Agilent ADS. This affords the best accuracy and improves the likelihood of convergence, particularly when simulating oscillator circuits that involve injection locking. With a long enough transient simulation, frequency domain performance can be determined from fast Fourier transforms of the resulting data. Specific characteristics, such as linearity performance(P1dB, IIP3), noise, and port impedance were determined through harmonic-balance(frequency domain-analysis) simulation in ADS. These analyses were performed under conditions where convergence at a particular frequency was guaranteed. The necessary conditions included that the LC

oscillators must successfully lock at the analysis frequency for a given input power of the reference LO. These conditions can be known from prior transient simulations. In addition, a transient-assisted harmonic balance option must be turned on. This option allows ADS to determine the steady-state conditions of the circuit with a short initial transient analysis. Without this option, the computed steady state will be incorrect. Specifically, the oscillators will not be able to start up and the LO drive seen by the mixers will be very small.

Sections 4.2 and 4.3 provide plots of simulated data. The plotted ranges, in power and frequency, were chosen to be sufficient in showing the discussed trends. The number of simulation data points that can be presented is limited by the available computer memory that can be used to process the final simulation data set. The data set for each simulated circuit contains the results of a long transient simulation for each plotted point. The overall simulation time creates an additional limitation, where each circuit takes about a day to simulate.

4.2 Complete Fundamental Quadrature Conversion System

Plots presented from Figure 31 to Figure 42 show the performance of the fundamental LO-referenced circuits without bondpad parasitics included at the RF and IF ports. Figure 31 to Figure 36 represent a circuit with uncoupled LC oscillators and Figure 37 to Figure 42 represent a circuit with quadrature-coupled LC oscillators. Bondpad parasitics have a slight impact on performance—reducing the strength of the reference LO signal and shunting some of the RF power, thereby reducing conversion gain. Table 4

provides a comparison of simulated performance parameters, with and without bondpads, for each type of oscillator coupling.

Oscillator Circuit	Conversion Gain (dB)	IIP3 (dBm)	P1dB (dBm)	Noise Figure (dB)	RF Feed-through (dBc)	LO Feed-through (dBm)
Uncoupled	-7.35	8.2	3.0	9.75	-58	-84
Coupled	-7.37	8.17	3.0	10.07	-54	-86
Uncoupled, bondpads	-7.77	8.12	3.0	10.21	-58	-86
Coupled, bondpads	-7.79	8.10	3.0	10.52	-54	-86

Table 4. Some simulated parameters for the quadrature mixer implementations that use a fundamental LO reference. The RF and LO feedthrough represent the power of those respective signal frequencies at the IF port. Values given in dBc are relative to the desired signal power at IF. Values shown in the table are nominal and may vary slightly according to the input conditions present. Further detail is provided in sections 4.2.1 and 4.2.2.

For the fundamental referenced circuits, the optimal real source impedance for the reference LO port is approximately 50 ohms. No matching network is provided for the reactive component of that impedance and, using a 50-ohm source, about two-thirds of the available power will be absorbed by the circuit. The impedance was optimized primarily for measurement by 50-ohm test equipment rather than a specific distribution scheme. This impedance depends largely on the polyphase filter that follows the input.

A differential RF source impedance of 100 ohms is used for all of the simulation results presented. The differential IF impedance is also 100 ohms. This is practical, given the measurement scenario and application, but not necessarily optimal. A better option is to decrease the RF source impedance and increase the IF impedance. This will allow the FETs of the passive mixer to commutate more current into a larger IF load. At an RF

source resistance of 60Ω and an IF load resistance of 150Ω, a maximum conversion gain of -6.88 dB(-7.17 dB, with bondpads) is achieved in simulation. With 100-ohm impedances, the negative effect on conversion gain is less than 0.5 dB, as seen in Table 4.

The fundamental system consumes a constant DC bias current of 14 mA when independent LC oscillators are used. Additional differential pairs used for quadrature coupling increase this current to 15.1mA in the case of coupled LC oscillators. In both cases, the necessary current is steady and does not vary with input and output conditions, as shown by Figure 31 and Figure 37, respectively. All DC currents are the tail current bias for various differential pairs in these circuits.

An increase in the power of the reference LO input will allow the internal oscillators to be injection-locked at greater offsets. The locking range for various power levels is provided by Figure 32 and Figure 38 for the two oscillator variants. The injection locking range in Figure 38 is slightly less at each power due to the additional load of the quadrature coupling pair of transistors on the injection locking pair in each oscillator. Monte Carlo simulations show that the oscillators will injection lock with 95% confidence if the LO power is sufficient for a range of 150 MHz. For this design, this is achieved with as little as 0.1mW available power from the reference.

The simulated differential drive that the oscillators, either coupled or uncoupled, provide to each passive mixer is nominally 1Vpp and will change only slightly as the

oscillators are pulled from their center frequency or the LO input power changes. This provides effective amplitude saturation and limiting of the LO seen by the mixers, resulting in consistent frequency conversion performance with regards to variation of the input conditions. For the mixer driven by uncoupled oscillators, as shown in Figure 33, the conversion gain is flat within 0.2dB for an LO frequency variation of 70% of the locking range. For the plotted range of the reference LO power, which corresponds to a 0.35 mW variation, the conversion gain is also flat within 0.2 dB. For the coupled oscillators over the same ranges, as indicated by Figure 39, the conversion gain variation is about the same with frequency and is 0.4dB with power. Conversion gain changes more steeply versus frequency near the edges of the locking range. The LO drive from the oscillators in either case contributes to a total LO feedthrough at the IF ports of the mixers that is less than -84 dBm(Table 4).

Simulations of the linearity parameters show that, for downconversion, the 1dB compression will occur at an RF input power of approximately 3 dBm. The third order intermodulation power(IIP3, relative to the mixer RF ports), found with the IF ports summed in perfect quadrature, is 8dBm. These simulations are shown in Table 4 and are nominal values found with an LO near the center of the locking range.

The noise figure, shown in Table 4, is the DSB noise figure when the two mixer IF ports are summed in perfect quadrature. This measurement configuration allows for image rejection and, as a result, the DSB noise figure is also the SSB noise figure.

The image rejection ratio(IRR) of the system depends heavily on the quality of the quadrature produced between the LO signals driving each mixer. The error in these signals will, at least, be seen in the quality of the quadrature at the IF ports after downconversion. In the case of upconversion, the effects are less obvious but will be related to the amount of power in the unwanted sideband. In the simulation data of the following sections, IRR is inferred from simulations showing the amplitude mismatch and phase mismatch of the IF quadrature after downconversion, for swept input conditions. The IF quadrature error, when the mixers are driven by uncoupled oscillators, shows a nominal amplitude mismatch of 0.4% and a phase mismatch of 3°(Figure 34 and Figure 35). For coupled oscillators, these values increase to 6% and 6°(Figure 40 and Figure 41), respectively. The corresponding nominal image rejection ratios are -32 dB and -24 dB. It is evident that there is little added benefit to quadrature coupling of the oscillators, particularly with regards to the way amplitude mismatch is affected.

4.2.1 Fundamental System with Uncoupled LC Oscillators

The following figures provide more detailed simulation data for the fundamental system with uncoupled LC oscillators. The effects of bondpad parasitics at the RF and IF ports are not included in this data. The LO source impedance is 50Ω. The RF and IF source impedances are each 100Ω. For plots versus LO frequency, the values shown correspond to a reference LO input power of 0.25mW. This corresponds to approximately 350 MHz of locking range and matches the locking range shown for plots versus frequency in the figures of section 4.2.2.

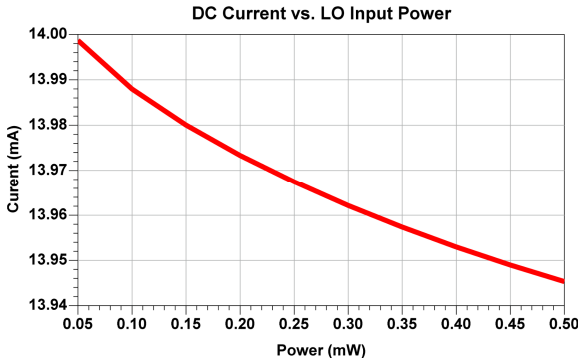


Figure 31. DC current requirement versus the available power from the fundamental LO reference. The LO power does not affect the current.

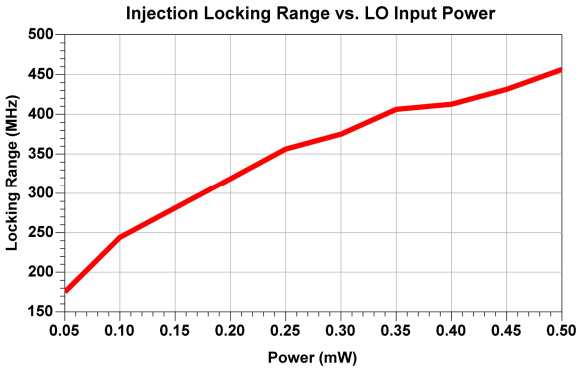
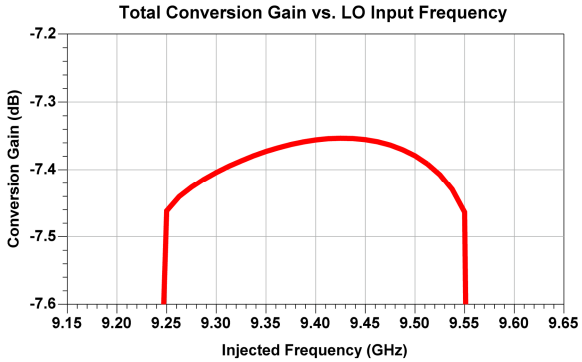


Figure 32. An increase in the injection locking range is observed with increasing LO reference power.

a.



b.

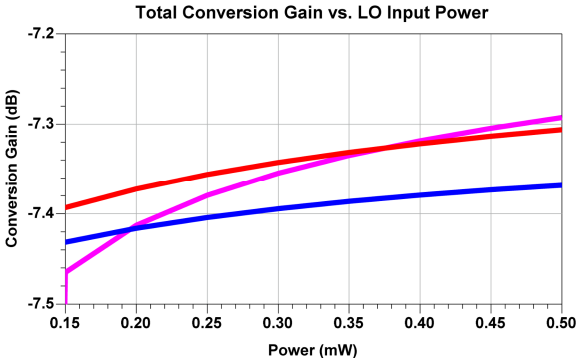
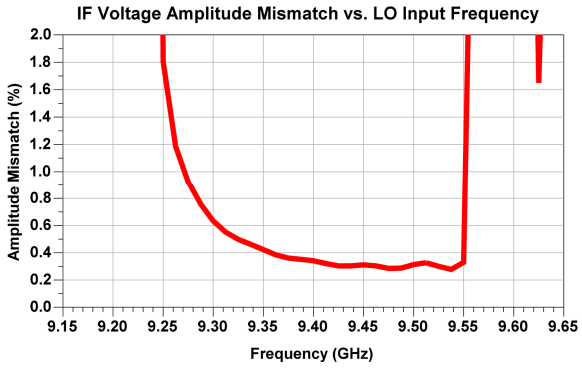


Figure 33. a) Conversion gain versus the frequency of a 0.25mW LO reference. Conversion gain is steady within 0.1 dB until the lock is lost at 9.25 and 9.55 GHz. **b)** The conversion gain versus LO power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet). The center of the injection locking range is 9.4 GHz.

a.



b.

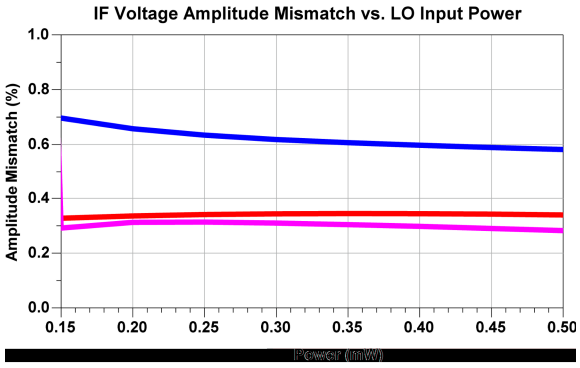


Figure 34. a) The amplitude mismatch, in percent, of the two quadrature IF signals versus the frequency of a 0.25mW LO reference. **b)** The amplitude mismatch versus LO power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet). In general, the match is better than 1%.

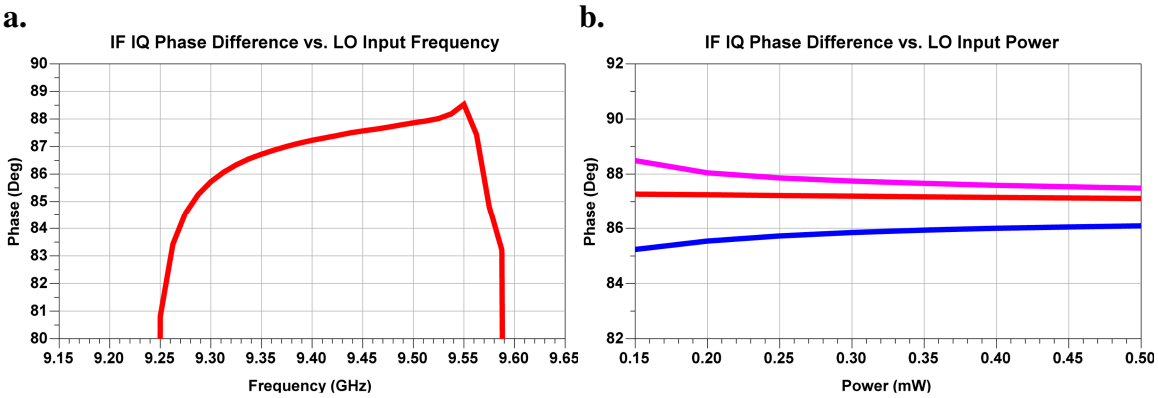


Figure 35. a) The simulated phase difference between the quadrature IF signals versus the frequency of a 0.25mW LO reference. **b)** The phase difference versus power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet). Phase error up to 5 degrees is observed and will be the limiting factor in image rejection performance.

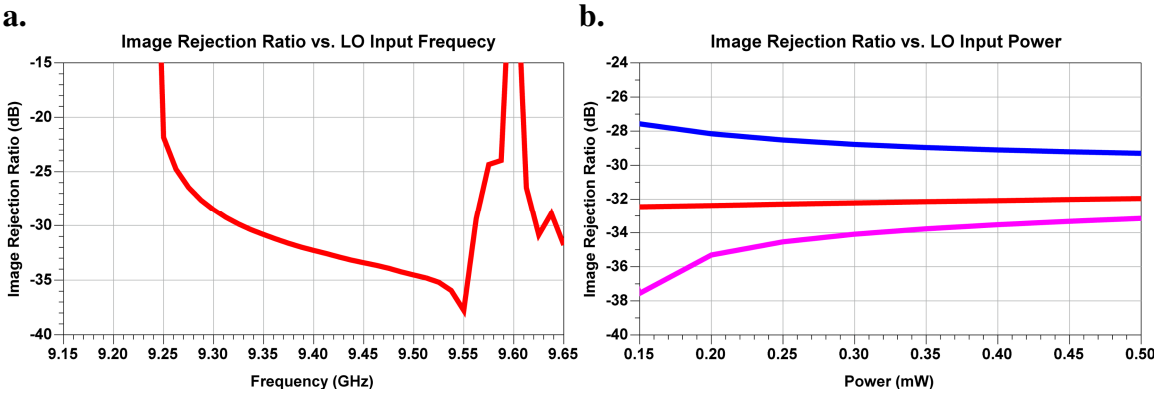


Figure 36. Image rejection ratio given that the IF signals are summed through a perfect quadrature combiner. In **a)** the IRR is shown versus the frequency of a 0.25mW LO reference. In **b)** the IRR is shown versus LO power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet).

4.2.2 Fundamental System with Coupled LC Oscillators

The following figures provided detailed simulation data for the fundamental system with quadrature-coupled LC oscillators. The effects of bondpad parasitics at the RF and IF ports are not included in this data. The LO source impedance is 50Ω. The RF and IF source impedances are each 100Ω. For plots versus LO frequency, the values shown correspond to a reference LO input power of 0.35mW. This corresponds to approximately 350 MHz of locking range.

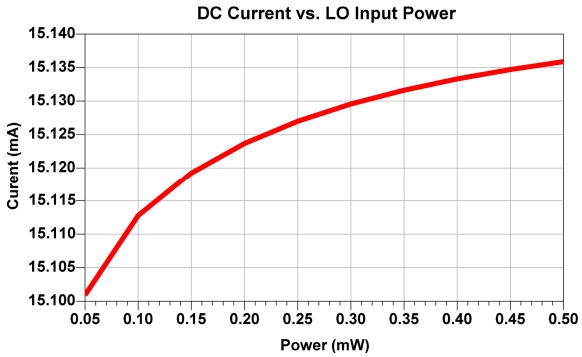


Figure 37. DC current requirement versus the available power from the fundamental LO reference. The LO power does not affect the current.

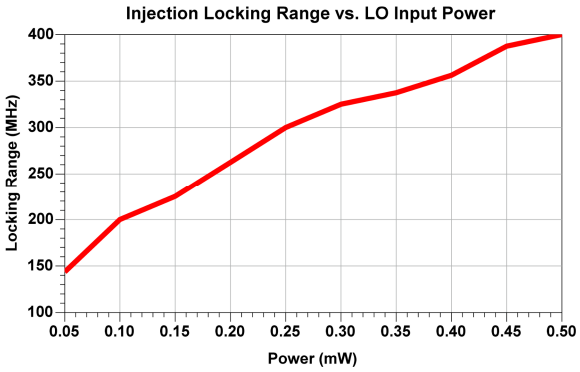


Figure 38. An increase in the injection locking range is observed with increasing LO reference power.

a. **b.**

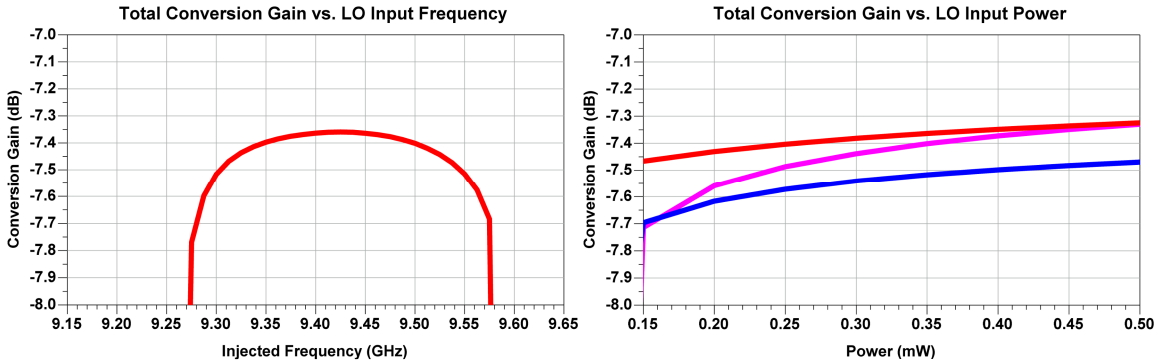


Figure 39. a) Conversion gain versus the frequency of a 0.35mW LO reference. Conversion gain is steady within 0.4 dB until the lock is lost at 9.28 and 9.58 GHz. **b)** The conversion gain versus LO power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet). The center of the injection locking range is 9.4 GHz.

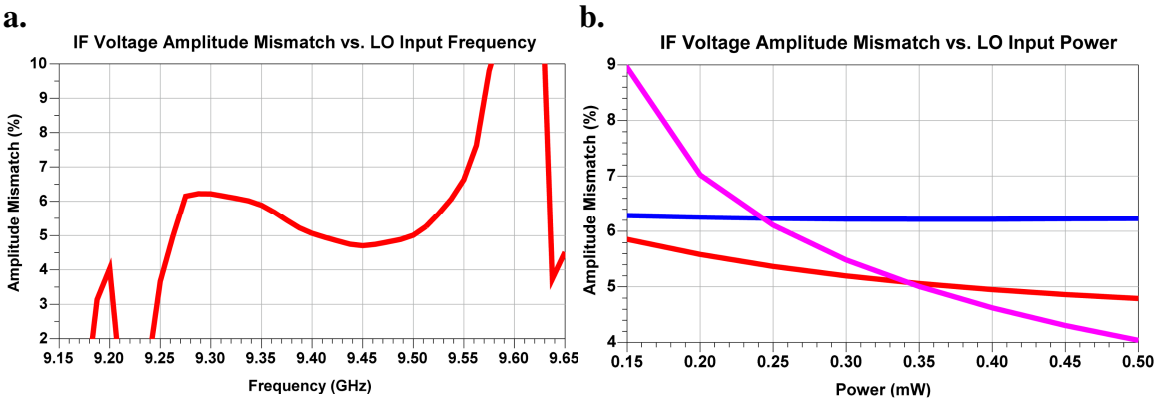


Figure 40. a) The amplitude mismatch, in percent, of the two quadrature IF signals versus the frequency of a 0.35mW LO reference. **b)** The amplitude mismatch versus LO power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet). In general, the match is better than 1%.

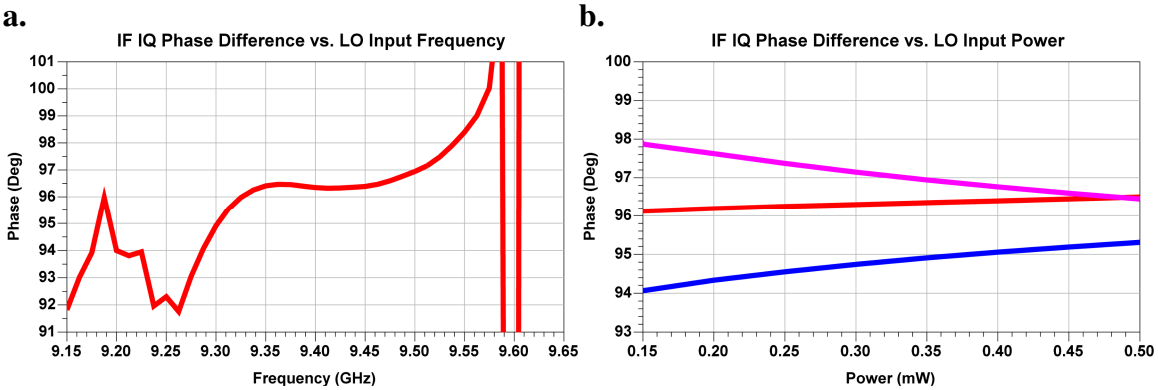


Figure 41. a) The simulated phase difference between the quadrature IF signals versus the frequency of a 0.35mW LO reference. **b)** The phase difference versus power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet). Phase error up to 8 degrees is observed, which limits image rejection performance.

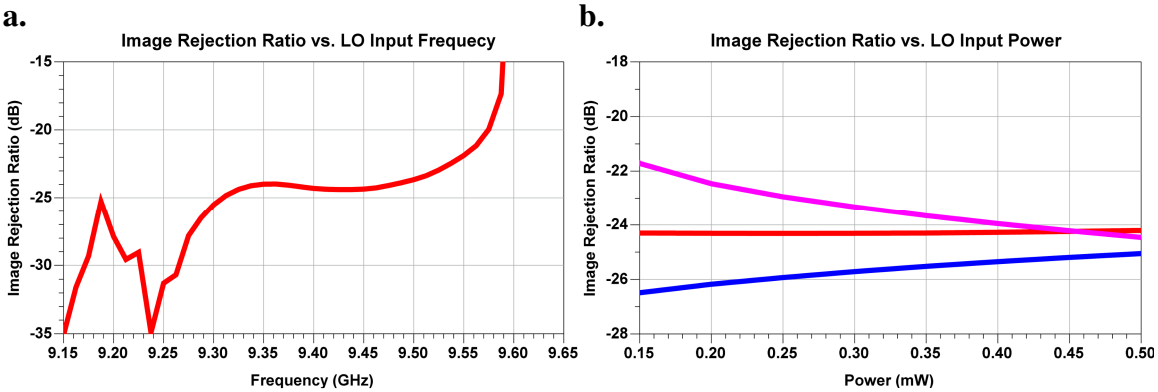


Figure 42. Image rejection ratio given that the IF signals are summed through a perfect quadrature combiner. In **a)** the IRR is shown versus the frequency of a 0.35mW LO reference. In **b)** the IRR is shown versus LO power at 9.3 GHz(blue), 9.4 GHz(red), and 9.5 GHz(violet). The nominal image rejection ration is -24 dB.

4.3 Complete Sub-harmonic Quadrature Conversion System

Simulation data for the circuits referenced to a sub-harmonic LO was computed following the methods that are described in section 4.1. The plots provided in section 4.3.1 correspond to a circuit with independent LC oscillators and those of section 4.3.2 correspond to the circuit with quadrature-coupled oscillators. Table 5, below, provides the summary comparison of simulated performance parameters for these two circuit variants, with and without bondpads at the RF and IF ports.

Oscillator Circuit	Conversion Gain (dB)	IIP3 (dBm)	P1dB (dBm)	Noise Figure (dB)	RF Feed-through (dBc)	LO/2 Feed-through (dBm)	LO Feed-through (dBm)
Uncoupled	-8.6	6.31	1.00	11.51	-58	-110	-90
Coupled	-9.9	5.63	-0.75	13.70	-53	-110	-96
Uncoupled, bondpads	-9.0	6.39	1.00	11.93	-58	-110	-90
Coupled, bondpads	-10.11	5.60	-0.75	14.13	-53	-110	-93

Table 5. Some simulated parameters for the quadrature mixer implementations that use a sub-harmonic LO reference. The RF and LO feedthrough represent the power of the respective signal frequencies at the IF port. Values given in dBc are relative to the desired signal power at IF. Values shown in the table are nominal and may vary slightly according to the input conditions present. Further detail is provided in sections 4.3.1 and 4.3.2.

For the sub-harmonically referenced circuits, a differential RF and IF source impedance of 100 ohms is used for all of the simulation results presented. These circuits draw a variable amount of current at DC due to the squaring of the sub-harmonic LO waveform by the frequency doubler. These currents are approximately equal when either the uncoupled or quadrature coupled LC oscillators are present, as shown in Figure 43 and Figure 49, respectively.

Simulations of the extracted layout show that the quadrature coupled LC oscillator designed for use in the sub-harmonic system is close to being critically-damped. As a result, the conversion gain plot assumes more of a bandpass characteristic and a very large locking range is achieved. Despite these issues, the oscillators do start up and exhibit a locking range in simulation. This does not occur with the fabricated circuits, which typically do not start up on their own and behave more like amplifiers. Therefore, the simulated conversion loss turns out to be under predicted slightly when compared to measurement. The circuit with uncoupled LC oscillators agrees much better with measurement. The locking ranges of both circuits flatten out at large LO reference powers due to the saturation of the input stages. This is shown in Figure 44 and Figure 50. The locking range is defined based on the range of the locked oscillator frequency, rather than the sub-harmonic LO frequency.

The image rejection ratio for the sub-harmonic circuits can be inferred from the simulations of amplitude mismatch and phase mismatch of the IF quadrature after downconversion through the mixers. The IF quadrature error, when the mixers are driven by uncoupled oscillators, shows a nominal amplitude mismatch of 1% and a phase mismatch of 6°(Figure 46 and Figure 47). For coupled oscillators, these values increase to 6% and 6°(Figure 52 and Figure 53). The image rejection ratio of the circuit with uncoupled oscillators is steadily -26dB. The coupled circuit exhibits a nominal image rejection ratio of -22dB and can vary by about ±2 dB when considering a bandwidth similar to the locking range of the uncoupled circuit.

4.3.1 Sub-Harmonic System with Uncoupled LC Oscillators

The following figures provide detailed simulation data for the system referenced to a sub-harmonic LO input and having independent(uncoupled) LC oscillators for the in-phase and quadrature LO drive. The effects of bondpad parasitics at the RF and IF ports are not included in this data. The LO source impedance is 50Ω. The RF and IF source impedances are each 100Ω. For plots versus LO frequency, the values shown correspond to a reference LO input power of 2mW and locking range of 200 MHz.

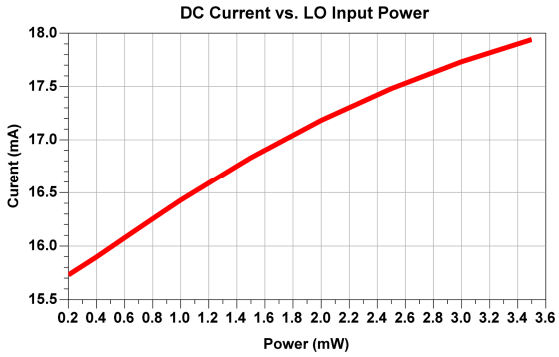


Figure 43. DC current drawn by the circuit versus the power of the sub-harmonic LO reference.

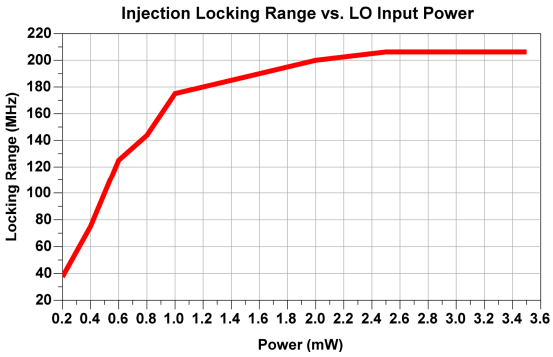


Figure 44. Injection locking range versus the power of the sub-harmonic LO reference. The input stage of the circuit saturates at 2.5 mW.

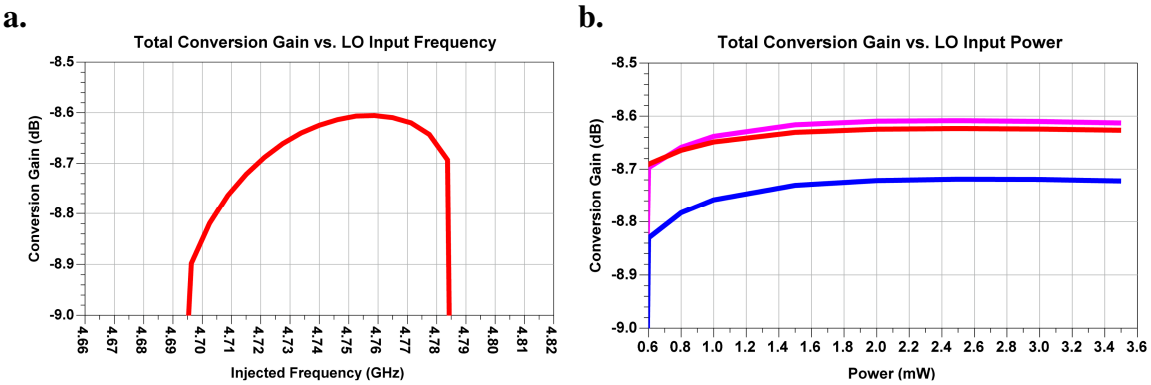


Figure 45. a) Conversion gain versus the frequency of a 2mW sub-harmonic LO reference. Conversion gain is steady within 0.3 dB until the lock is lost at 4.7 and 4.78 GHz. **b)** The conversion gain versus LO power at 4.715 GHz(blue), 4.740 GHz(red), and 4.765 GHz(violet). The center of the injection locking range is 4.740 GHz.

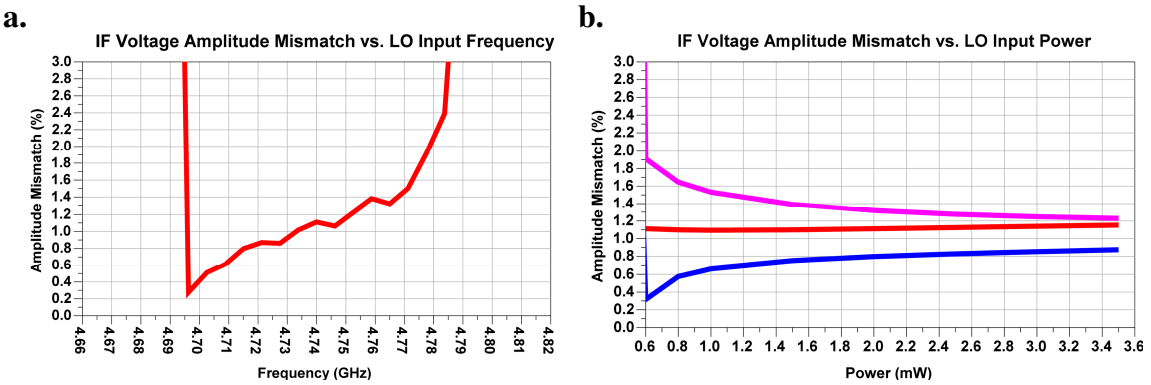


Figure 46. a) The amplitude mismatch, in percent, of the two quadrature IF signals versus the frequency of a 2mW sub-harmonic LO reference. **b)** The amplitude mismatch versus LO power at 4.715 GHz(blue), 4.740 GHz(red), and 4.765 GHz(violet). In general, the match is better than 2%.

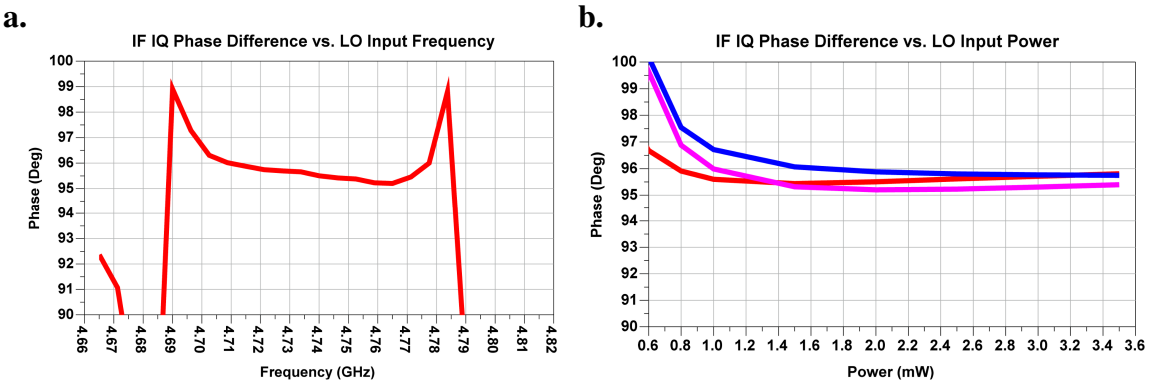


Figure 47. a) The simulated phase difference between the quadrature IF signals versus the frequency of a 2mW sub-harmonic LO reference. **b)** The phase difference versus power at 4.715 GHz(blue), 4.740 GHz(red), and 4.765 GHz(violet). Phase error up to 6 degrees is observed.

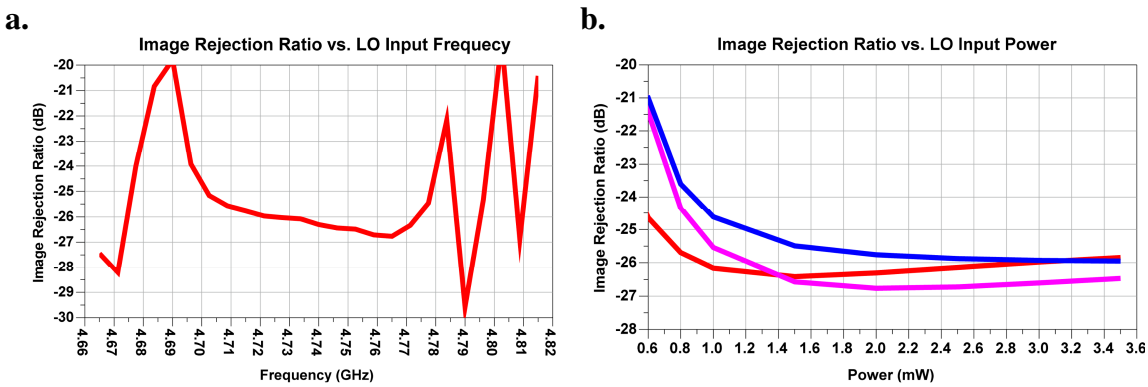


Figure 48. Image rejection ratio given that the IF signals are summed through a perfect quadrature combiner. In **a)** the IRR is shown versus the frequency of a 2mW sub-harmonic LO reference. In **b)** the IRR is shown versus LO power at 4.715 GHz(blue), 4.740 GHz(red), and 4.765 GHz(violet).

4.3.2 Sub-Harmonic System with Coupled LC Oscillators

The following figures provided detailed simulation data for the system referenced to a sub-harmonic LO input and having quadrature-coupled LC oscillators for the IQ LO drive. The effects of bondpad parasitics at the RF and IF ports are not included in this data. The LO source impedance is 50Ω. The RF and IF source impedances are each 100Ω. For plots versus LO frequency, the values shown correspond to a reference LO input power of 2mW.

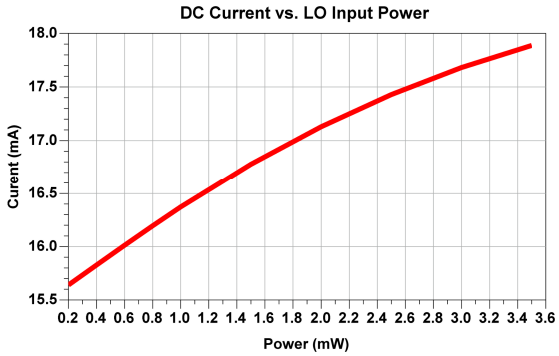


Figure 49. DC current drawn by the circuit versus the power of the sub-harmonic LO reference.

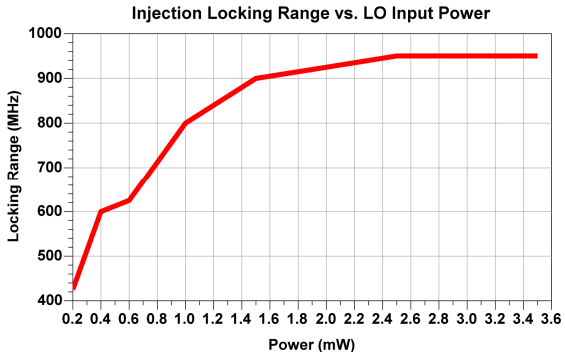
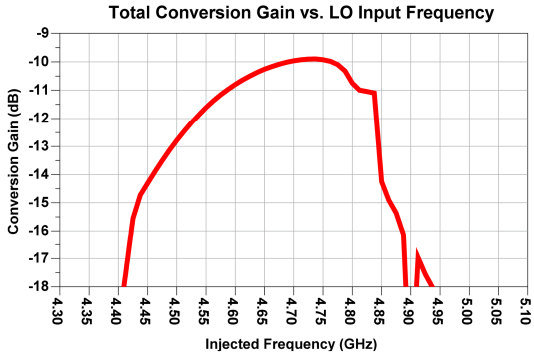


Figure 50. Injection locking range versus the power of the sub-harmonic LO reference. The input stage of the circuit saturates at 2.5 mW.

a.



b.

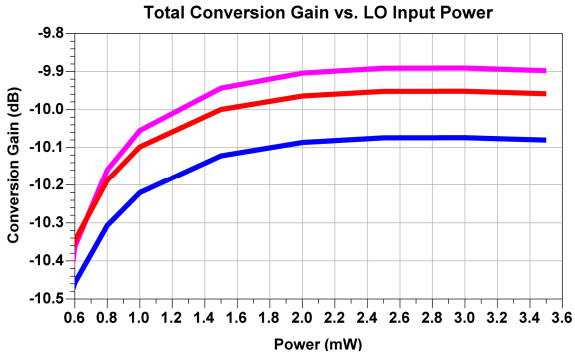
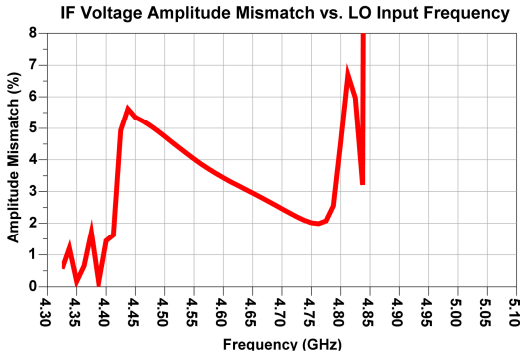


Figure 51. a) Conversion gain versus the frequency of a 2mW sub-harmonic LO reference. **b)** The conversion gain versus LO power at 4.675 GHz(blue), 4.7 GHz(red), and 4.725 GHz(violet). Conversion gain varies by approximately 0.2 dB over a 100 MHz window.

a.



b.

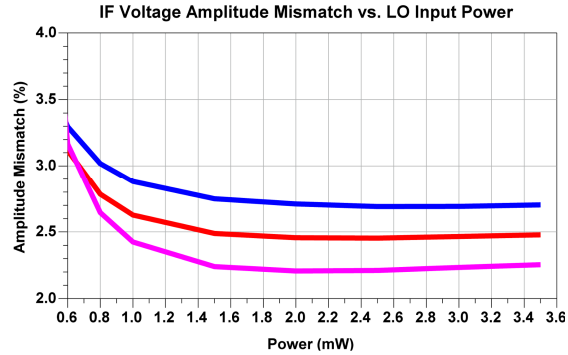


Figure 52. a) The amplitude mismatch, in percent, of the two quadrature IF signals versus the frequency of a 2mW sub-harmonic LO reference. **b)** The amplitude mismatch versus LO power at 4.675 GHz(blue), 4.7 GHz(red), and 4.725 GHz(violet). In general, the match is better than 5%.

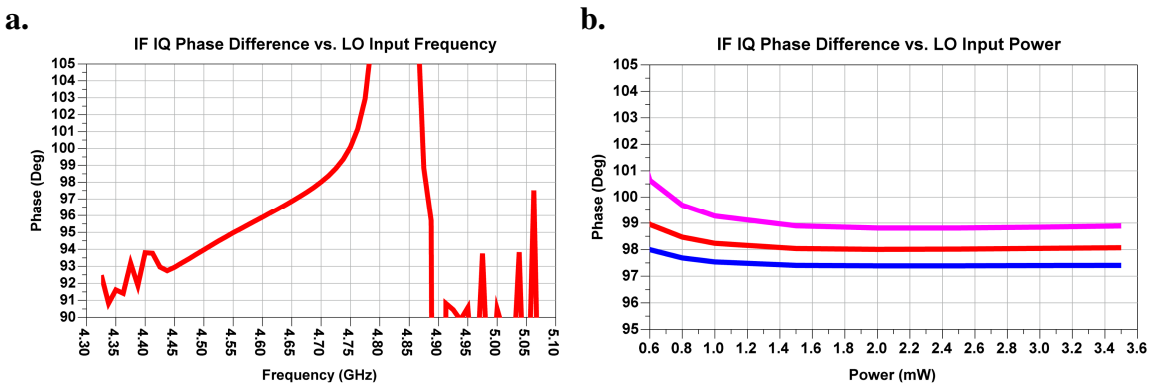


Figure 53. a) The simulated phase difference between the quadrature IF signals versus the frequency of a 2mW sub-harmonic LO reference. **b)** The phase difference versus power at 4.675 GHz(blue), 4.7 GHz(red), and 4.725 GHz(violet). Phase error up to 10 degrees is observed and can severely limit the IRR.

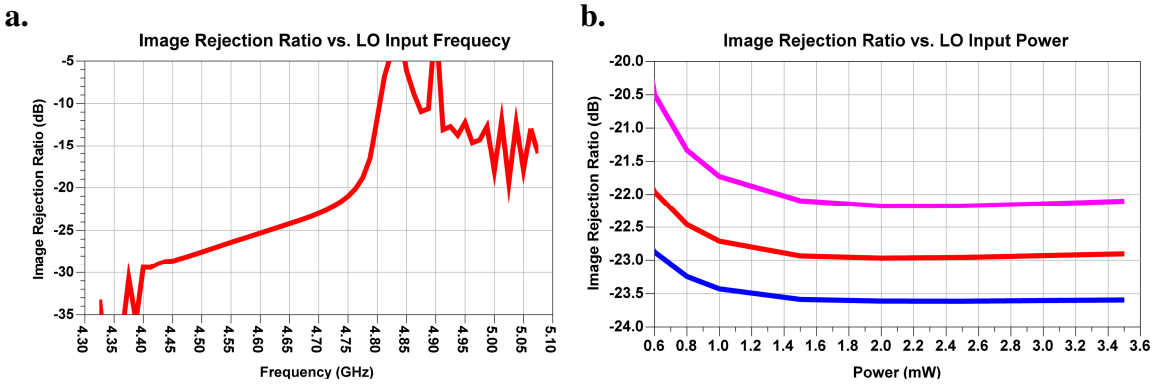


Figure 54. Image rejection ratio given that the IF signals are summed through a perfect quadrature combiner. In **a)** the IRR is shown versus the frequency of a 2mW sub-harmonic LO reference. In **b)** the IRR is shown versus LO power at 4.675 GHz(blue), 4.7 GHz(red), and 4.725 GHz(violet).

CHAPTER 5

MEASUREMENT

This chapter discusses measurements of the four variations of the quadrature generation and frequency conversion system fabricated for this thesis. Section 5.1 will cover the procedures used to perform the measurements. Sections 5.2 and 5.3 present the results for the fundamental and sub-harmonic systems, respectively.

5.1 Methodology

Fabricated parts were received as bare die. During testing, pads on the die were either contact probed or wirebonded. DC signals, such as the 1.8V supply line, were wire-bonded to a carrier PCB. RF signals were probed via specialized 40GHz GSG(ground-signal-ground) or GSSG(ground-signal-signal-ground) wafer probes. Images of the test setup are shown in Figure 55. The cut die and the PCB used for testing are shown in Figure 56 and Figure 57. The bondpads along the edges of the die are 150um square with 250 micron pitch and can be wire-bonded to the custom carrier PCB for testing. The internal bondpads, used exclusively for contact probing, are 115 um square with 150 micron pitch. All bondpads on the fabricated die are aluminum.

Different test configurations were used to measure the various performance parameters of the fabricated system. These are detailed in sections 5.1.1 through 5.1.3. A brief discussion of the fabrication process, IBM 7RF, can be found in the appendix to this thesis.

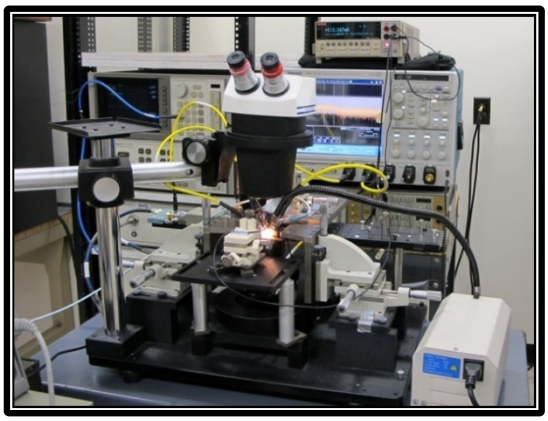
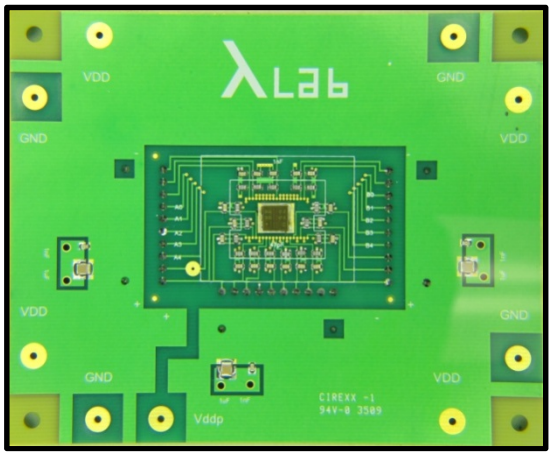
a.  b. 

Figure 55. a) The test set up, including probe station and instrumentation, in LAMMDA Lab. **b)** Close up view of microwave probes over the fabricated die.



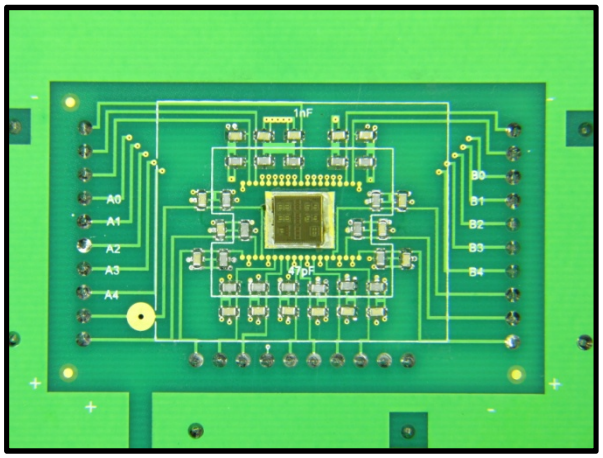


Figure 56. The PCB used to test designs on the fabricated IC. This image was taken before wire-bonding. The die is attached with silver-epoxy to a 1mm gold spacer that is soldered to the PCB. The spacer provides a good substrate ground and enough clearance from nearby surface-mount devices for contact probing.

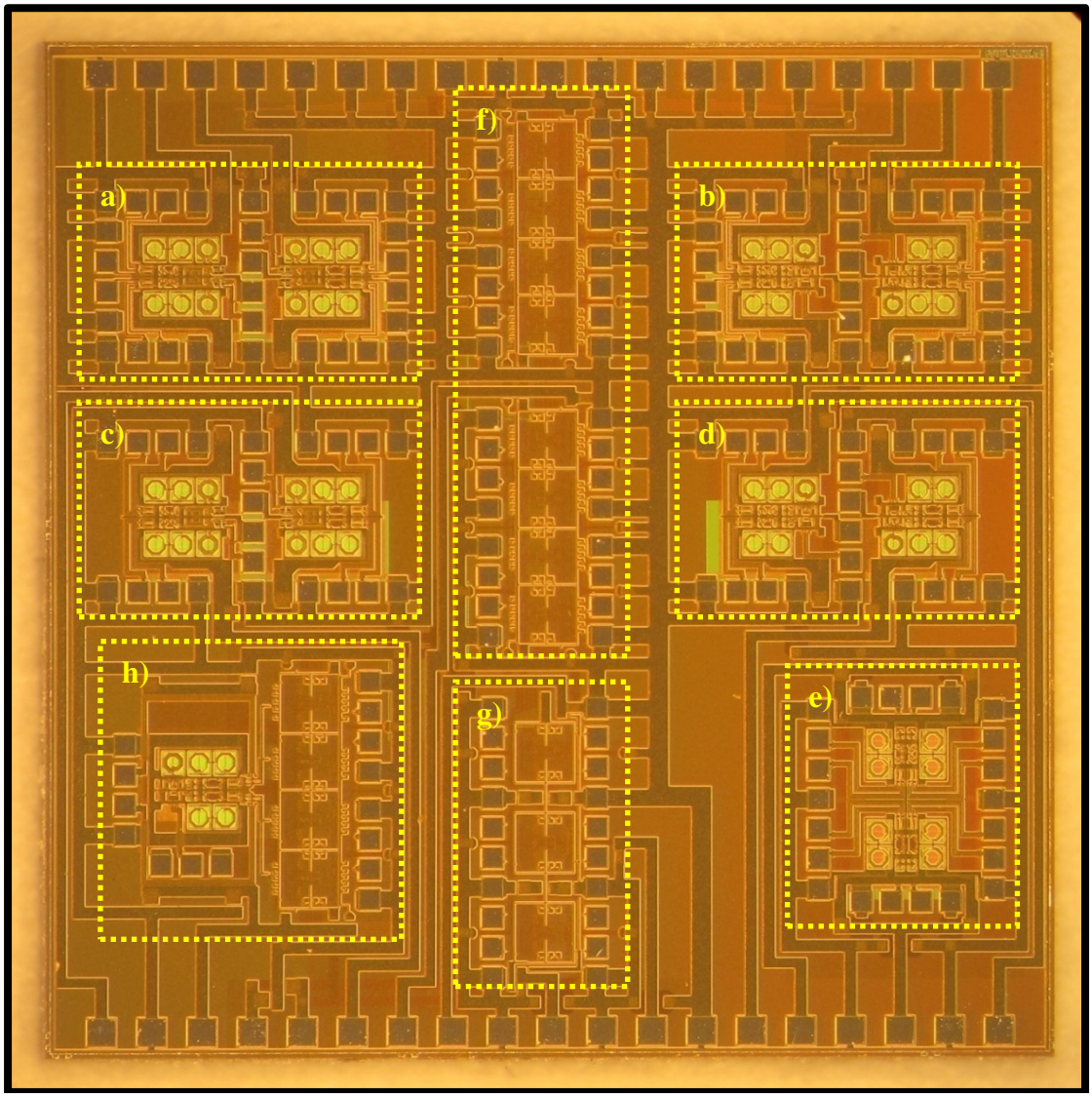


Figure 57. Micrograph of the 5mm X 5mm test die. Included are—**a)** Two variations of the complete IQ upconversion/downconversion sub-system with a fundamental LO reference. **b)** Two variations of the system with a sub-harmonic reference. **c)** The fundamental LO conditioning circuits alone. **d)** The sub-harmonic LO conditioning circuits alone. **e)** Injection-locked LC oscillator test circuits. **f)** Two gain-phase controller circuits. **g)** Gain-phase controller transmit and receive amplifier test circuits. **h)** The combined IQ up/down conversion and gain-phase controller blocks.

5.1.1 Conversion Gain, Locking Range, IIP3, and Power Dissipation

For the measurement of conversion gain, locking range, intermodulation distortion, and the overall power dissipation, the test configuration shown in Figure 58 was used. The bold italic text indicates system outputs that are monitored with various test equipment throughout the measurement process. These ports are each terminated to 50Ω during measurements. The block labeled "DUT" is one LO conditioning and mixing device from the die pictured in Figure 57. Due to the restrictions of the probe station and available translation axes, only three multipoint probes could be used simultaneously to measure or excite RF ports in the device. As a result, one set differential IF ports, I or Q, must be left open while the other is measured. At the IF frequency, the open IF output port of one mixer will not noticeably affect the measurement being performed at the IF port of the other mixer. At the RF frequency, RF energy will continue to be shorted across the IF capacitor as shown in Figure 9.

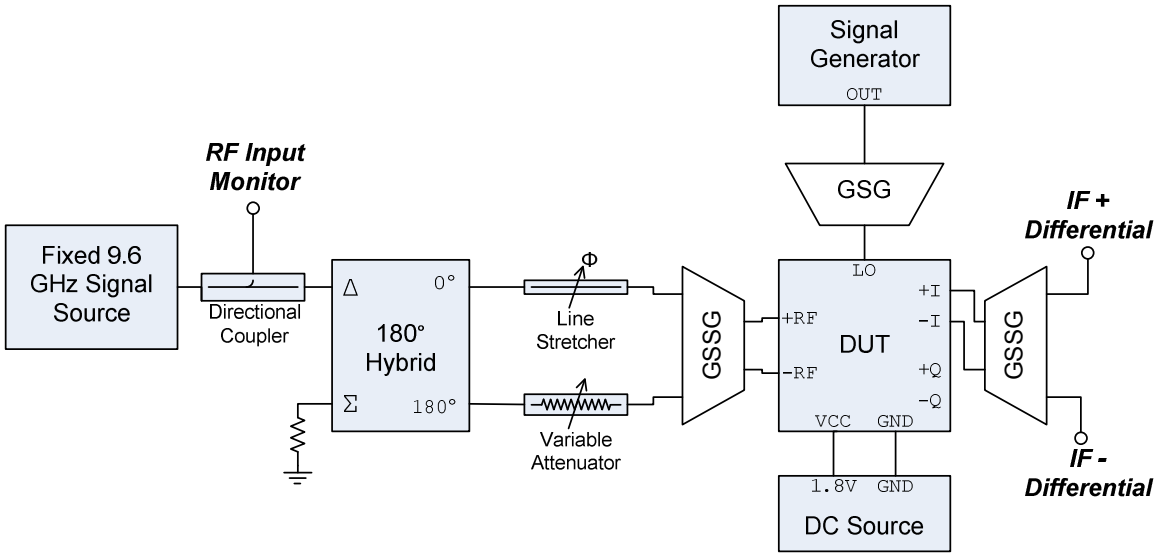


Figure 58. Measurment set-up for conversion gain, locking range, and IIP3 measurements.

Much of the test setup shown in Figure 58 is used for the generation of a differential RF at 9.6 GHz, to be fed into the fabricated mixers. A network analyzer provides the signal source, which is first fed into a directional coupler for monitoring. A 180° hybrid is used to split the RF signal into two components. It is not important that the hybrid provide antiphase outputs—any power splitter at the appropriate frequency would work. A variable phase shifting component is connected at one output to make any phase corrections. A variable attenuator at the opposite output allows the power at that output to be adjusted to match the phase shifted output. The RF signal is calibrated by connecting the two outputs, via two matched 2.92mm coaxial cables, to two channels of a DPO71254B 50Gsps Tektronix sampling oscilloscope. The signal source is configured to output a 9.6 GHz tone with enough power to be well into the dynamic range of the oscilloscope. The oscilloscope is itself ranged to have a maximum input level that is similar to the expected power levels on the two outputs, thus minimizing quantization

noise. The oscilloscope must also be configured to take a large number of samples and perform an FFT that will provide the required measurement with sufficient averaging. At this point, the slide on the line-stretcher is adjusted until the oscilloscope shows a 180° phase difference between the two outputs. The variable attenuator is then adjusted until both outputs exhibit equal power/amplitude. The phase and attenuation can be adjusted iteratively until the outputs are simultaneously observed, from the calculated FFT phasor at the frequency of interest, to be both anti-phase and equal in amplitude. The cables feeding the two channels on the oscilloscope will eventually be connected to the GSSG probe feeding the RF input on the DUT.

RF power was calibrated by monitoring the power levels at the directional coupler and each differential output of the RF conditioning network described above. These powers were measured with the power meter, oscilloscope, and spectrum analyzer. This was done for a number of signal source powers from the network analyzer. With this information a relative correlation between the power levels measured on each instrument and the coupled output of the directional coupler could be established. Ideally the power should be seen to scale linearly, perhaps with some offset, on each instrument. The lack of dynamic range provided by the oscilloscope yielded the least consistent results in this regard. For accuracy in conversion gain measurements, the spectrum analyzer was used. The oscilloscope is accurate when comparing signals of relatively similar power. The specific measurements that were made are detailed in the following sections. The

compression point, P1dB, could not be measured due to a limited maximum output power of the RF signal source at 9.6 GHz.

5.1.1.1 Power Dissipation

The power dissipation measurement is the most straightforward. The DC power supply used during all measurements has built in supply current measurement capabilities. Therefore, the current being drawn by the circuits was easily recorded for every measurement taken. The supply voltage was 1.8V. Power dissipation can vary with the signal power of the reference LO input.

5.1.1.2 Conversion Gain

To determine the conversion gain to either the I or Q mixer port, the 12.5GHz oscilloscope was first used to verify that the signals at the positive and negative IF differentials of the port under test were essentially equal in power (less than 0.1 dB mismatch, as measured). This was true for all the cases observed. The spectrum analyzer was then used to measure the IF signal power at one differential end while the other was terminated with 50Ω. This power, for a particular 9.6 GHz signal source power, was then compared to the power at the output of the directional coupler and the earlier power level correlations were used to de-embed the conversion gain. Cable loss through the IF feed lines connecting to the instruments is not an issue at the IF frequency. Nonetheless, all coaxial feed lines were individually characterized with the network analyzer for power loss and group delay at various frequencies, including IF.

5.1.1.3 Locking Range

Locking range was determined by varying the LO signal frequency and observing the IF output spectrum on the oscilloscope after downconversion. The fixed RF of 9.6 GHz is applied at constant power throughout this measurement. When locked, the I and Q IF outputs should show a single peak at a low IF frequency. When the locking range is exceeded, multiple peaks and sidebands begin to appear. These include both the downconverted LO and free running oscillator frequency, and the continuous higher order mixing products of the two. The frequency difference between upper and lower reference LO frequencies, that each correspond to the onset of multiple peaks within the IF output spectrum, is proportional to the locking range. In the fundamental-referenced circuit, this difference is the actual locking range, whereas, in the sub-harmonic circuit, it is one half of the locking range. The locking range is defined in terms of the recovered LO that drives the mixers rather than the reference LO. The variation in the IF output power over frequencies within the locking range is also recorded.

5.1.1.4 Intermodulation Distortion

For IIP3 measurements, the network analyzer was not used as a signal source. Instead, two signal generators were used. Their outputs were connected into 3dB attenuators and combined with a hybrid power combiner. The combined output was fed into a selectable attenuator. Two equal power tones spaced by 10 MHz were produced by the two signal generators and centered around the previously tuned 9.6 GHz RF frequency for which antiphase outputs would be generated from the RF differential conditioning network. Again, the directional coupler was monitored to determine total

input power(combined power from both tones) with the power meter. The spectrum analyzer was used to observe the IF output power at the fundamental and third order mixing product frequencies for each selectable attenuation. The logarithmic powers of the fundamental and third order components will each increase linearly with input power and can be extrapolated to determine the IIP3, which is the input power where the extrapolated trends intersect. Figure 59 below illustrates the process for the extraction of IIP3. In the example, two(overlapped) lines of slope 1:1 are shown and represent the power of the I and Q fundamental tones. The other two lines are the I and Q third order mixing products, with a slope of 3:1. Linear trend lines are superimposed over the data. If these trend lines are continued into increasing input power levels they will intersect. That intersection point determines the IIP3 and can be calculated from the line equations of the fitted trend lines. This extrapolation assumes a weakly non-linear system. In some cases, the fitted trend lines will have slope slightly less than anticipated. For these instances trend lines with the correct slope are used and they intersect the measured data at the lowest input power(greatest attenuator setting).

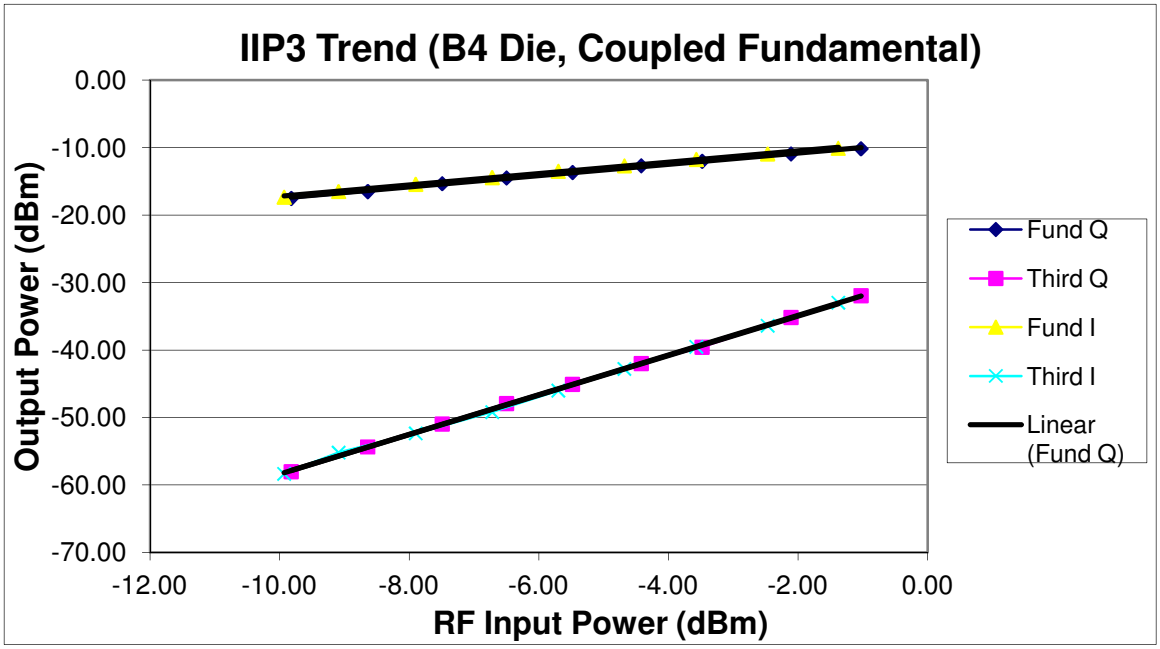


Figure 59. Plotting trends for the extrapolation of IIP3.

5.1.2 I and Q Relative Phase/Quadrature Accuracy

Measurement of the quadrature phase between the two I and Q IF outputs of the system was not initially possible because a four-axis probe station was required and only three axes were available. To accommodate the limitation, each of the four variants of the quadrature conversion system was fabricated on the test die without the mixers. The quadrature LO outputs of the injection-locked oscillators were probed directly, eliminating the need for a fourth probe that supplies a differential RF signal. This approach added additional overhead to the measurement and subsequent analysis, due to the high signal frequencies that needed to be compared as a result of the modification. It was necessary to characterize the group delays of the cables connecting to the measurement instrumentation in order to compensate for the phase shift that they would

add to the measured signals. Unfortunately, the resulting measurements were difficult to analyze and possibly unreliable. The coaxial cables that were used exhibited some phase sensitivity if bent or moved.

A four axis probe station was provided by Lincoln Laboratory in Lexington, Massachusetts, for use in their facility. This allowed for the direct measurement of phase performance at IF frequencies. A diagram of the measurement configuration is shown in Figure 60 below. Two signal generators provided the LO and RF signals. The LO frequency was varied within the measured locking range of the circuit and the RF frequency was adjusted for a fixed IF at 100 MHz. The four IF output signals, I+, I-, Q+, and Q-, were connected to a four channel high-speed (LeCroy SDA 13000) oscilloscope. This oscilloscope was used for making phase comparisons of the four signals. The phases were resolved by computing FFTs over long sampling intervals. The oscilloscope could do this automatically and immediately provide phase data at the IF frequency for each measurement channel. Matched cable lengths were used for the connection to each channel and were not critical at 100 MHz as they were at 9.4 GHz.

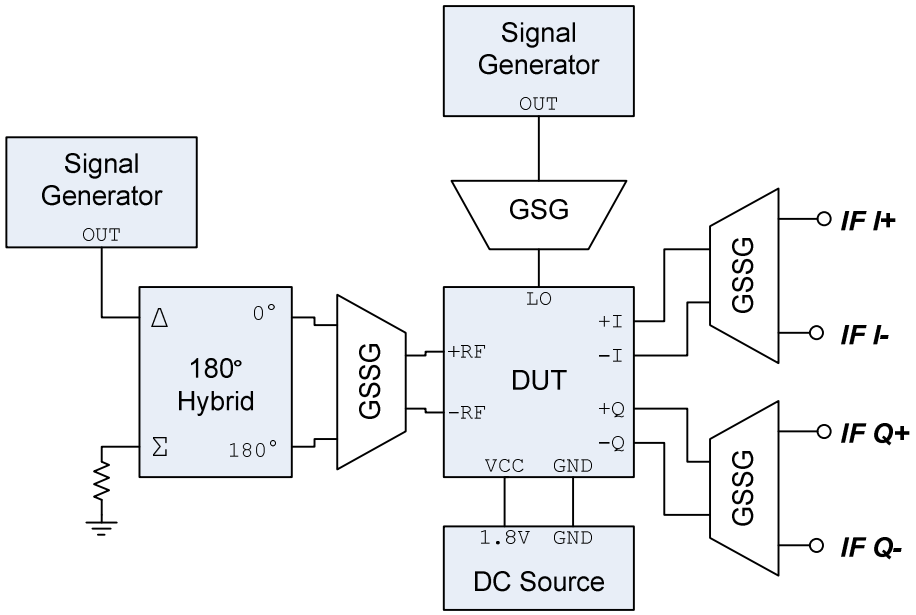


Figure 60. Measurement setup for quadrature LO phase performance. The four outputs are connected via coaxial cables to a SDA 13000 series oscilloscope.

5.1.3 Noise

Measurement of noise figure was performed with an Agilent N8974A noise figure analyzer(NFA). The NFA controls an external excess noise source and provides a single ended input with 3 GHz of bandwidth. The noise source that was used in conjunction with the NFA provided calibrated noise levels up to 26 GHz.

The configuration used to make noise measurements of the fabricated systems is shown in Figure 61 below. The noise source feeds a 180° hybrid that provides the differential RF input source to the mixer under test. The line stretcher and variable attenuator maintain their calibrations as described in section 5.1.1. Only one differential IF port of the IQ mixer arrangement is connected. It is converted to a single ended signal through a wide-band balun(Mini-Circuits, ADT2-1T-1P) transformer. A 20 dB IF

amplifier increases the level of the output noise for better measurement with the NFA. The IF amplifier is included in the initial calibration sequence for the NFA such that the noise figure returned is the noise figure of the system from the input of the 180° hybrid to the output of the balun. The NFA is configured for a downconversion measurement and properly shifts its ENR(excess noise ratio) tables to account for noise being downconverted from the higher RF frequency. The returned noise figure is a DSB measurement.

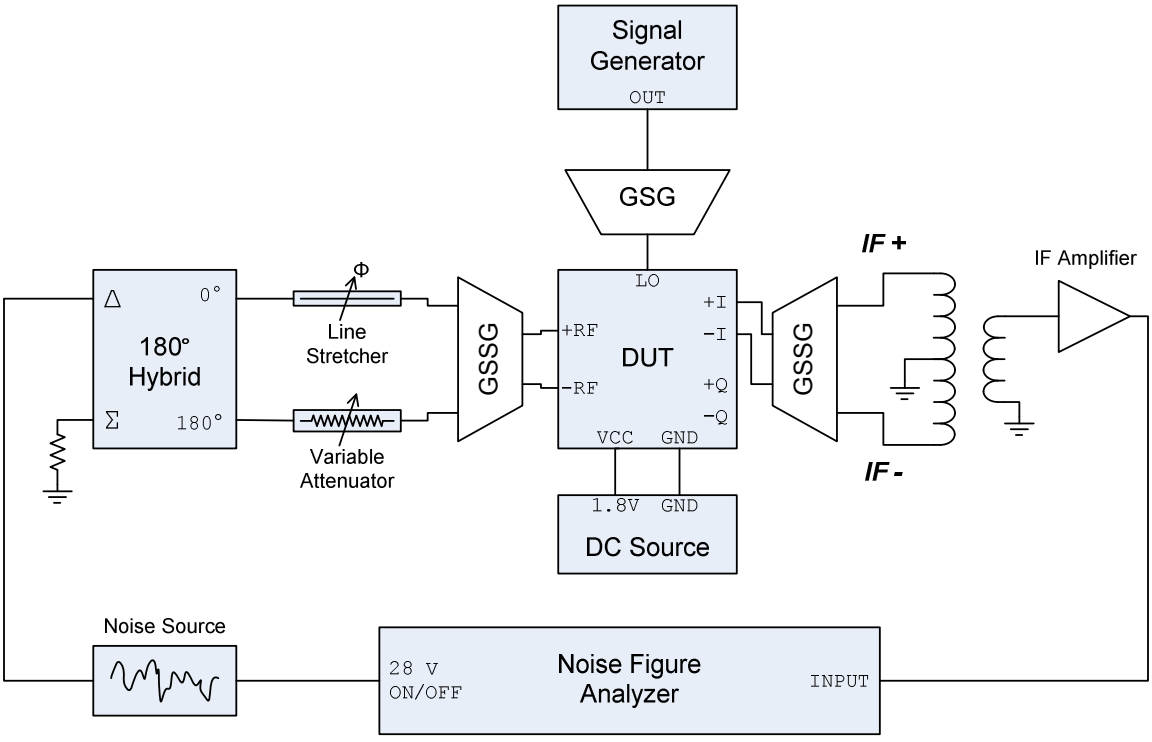


Figure 61. Test set-up for DSB noise figure measurement.

In order to extract a useful value from the measurement procedure described, the DUT noise figure must be de-embedded from the noise contributions of the various passive devices in the test set-up. The de-embedding is performed by solving the Friis

formula for the noise figure of cascaded stages, once all of the individual noise contributions are known. In this set-up, there are three contributors that must be known and that make up the complete cascaded system. These are the 9.6 GHz RF differential conditioning network, the IF balun transformer, and the differential microwave probes. The losses of the microwave probes at the frequencies of interest are supplied by manufacturer data sheets that are shipped with each probe. The noise figure of the RF conditioning network was determined with the measurement approach shown in Figure 62, below. For this measurement, an external mixer is connected before the IF amplifier in order to downconvert the noise at RF to a band within the NFA's measurement range. The NFA is designed for high-frequency measurements of this type and includes both the mixer and IF amplifier in its calibration routine. The noise figure that is measured includes only one end of the differential output of the conditioning network and the other end is terminated. The choice of which end is terminated does not matter. It can be shown that for a 180° hybrid with equal attenuation following each of the anti-phase ports the differential noise figure versus the noise figure with one port terminated is:

$$F_{(differential)} = \frac{2R(R+2Z_0)^2}{Z_0(R+Z_0)^2} + 1$$
$$F_{(single)} = \frac{4R(R+2Z_0)^2}{Z_0(R+Z_0)^2} + 2 \qquad \text{(Eq. 5.1)}$$

In the above, the resistance R accounts for the attenuation connected at each port by adding the resistance in series with the outputs of an ideal 180° hybrid. (Eq. 5.1) shows that the measured noise figure will be 3dB more than the noise figure of the network as it is used in the system of Figure 61. The measured noise figure is 5.24 dB and, therefore,

the actual noise figure of the RF conditioning network, as used in Figure 61, is 2.232 dB. The differential to single-ended balun is measured in a similar fashion to the RF differential conditioning network. The mixer and IF amplifier of Figure 62 are not used because the measurement falls within the NFA bandwidth. The IF balun exhibits a noise figure of about 0.6 dB as used in the system of Figure 61.

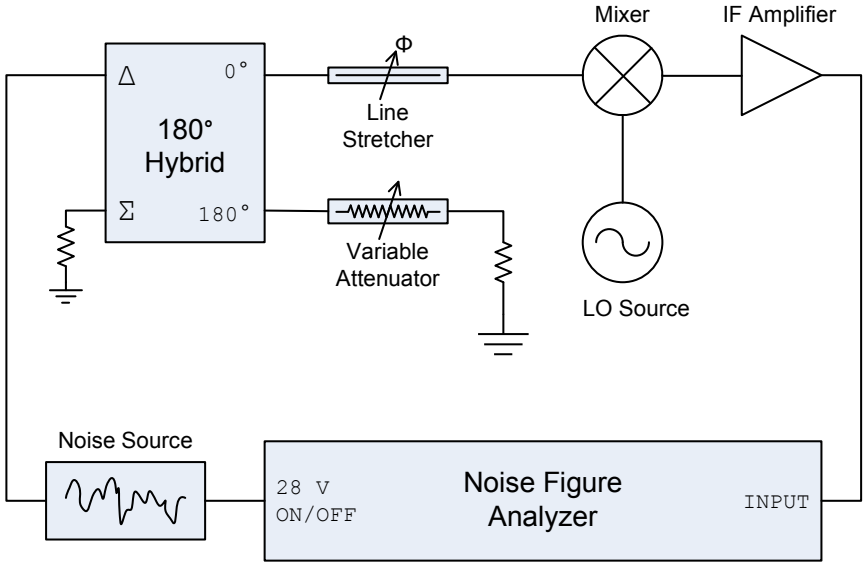


Figure 62. Test set-up for measuring the noise figure of the passive RF conditioning network.

It is important to note that, when using the measurement approach of Figure 61, the de-embedded noise figure is the DSB noise figure for a single mixer in the IQ arrangement, with the IF port of the other mixer left open. Leaving the IF port of one of the mixers open affects the noise figure of the remaining mixer by less than 0.1 dB in simulation.

5.2 Fundamental System Performance Measurements

Table 7 and Table 8 outline the measured performance parameters for the quadrature conversion systems with fundamental LO references. Table 7 summarizes circuits with uncoupled LC oscillators and Table 8 summarizes circuits with coupled LC oscillators. The measured parameters are listed in columns that indicate the die on which the particular circuit was tested. The die are labeled B2, B4, B5, W1, W2, W3 and W4. Each die contains one of each circuit variation of the quadrature conversion system.

Measurements for die B2, B4, and B5 were made following the procedures detailed in section 5.1.1. W1 and W2 were measured according to the procedure of section 5.1.3. W3 and W4 followed the procedure of section 5.1.2. Each of these procedures was designed to yield results for different performance parameters. The die B2, B4, and B5 were used for the measurement of conversion gain and non-linearities. W1 and W2 were used for the measurement of noise. W3 and W4 were used to measure quadrature phase and amplitude accuracy. Some performance data, such as conversion gain or locking range, could be measured in multiple test configurations. Table 6 summarizes how each die was measured.

All signals, RF and DC, on the die B2, B4, and B5 were contact probed. W1, W2, W3, W4 and W5 differ in that all DC signals were wire-bonded from the die to a PCB. These wirebonds were necessary to allow probe positioning in the arrangement required

for certain measurements. For those measurements, having an additional single-point probe for the DC supply would be an obstruction to necessary microwave probes.

A fact that can be noted from the tables below is that certain types of measurements, for a particular circuit, were taken from different die than had been used for other measurements. This is, in part, because certain measurements did not require wirebonds on the die and it was possible to make those measurements while other die were in the process of being wirebonded. In addition, pads were occasionally gouged during probing; this also required switching samples. Lastly, a second series of measurements were made at MIT Lincoln Laboratories in Lexington, MA and, at that time, only certain die were available for measurement.

Die Designator	**B2**	**B4**	**B5**	**W1**	**W2**	**W3**	**W4**	**W5**
Measurement Procedure	5.1.1	5.1.1	5.1.1	5.1.3	5.1.3	5.1.2	5.1.2	5.1.2

Table 6. Table of the measurement procedures primarily followed for each of eight die that were measured. The procedures are indicated beneath the designation of each die with the numbering of the related thesis section.

Die Designator	B5	B4	W1	W2	W3	W4
Free Running Oscillator Frequency (GHz)	9.821	9.822	9.807	9.802	9.829	9.846
DC current (mA, No LO)	13.458	13.370	13.653	13.177	13.93	13.19
Conversion Gain to I port (dB)	-10.66	-10.65	-10.129	-10.089	-	-
Conversion Gain to Q port (dB)	-9.23	-9.29	-9.508	-10.045	-	-
Conversion Gain Total (dB)	-6.87	-6.91	-6.80	-7.06	-	-
IIP3 (dBm)	10.78	10.29	-	-	-	-
Noise Figure to I port (dB)	-	-	10.46	10.03	-	-
Noise Figure to Q port (dB)	-	-	9.47	10.05	-	-
Quadrature Phase (deg)	-	-	-	-	103	109
Amplitude Mismatch (%)	16.43	15.63	7.15	0.51	1.50	3.57

Table 7. General performance data for the uncoupled, fundamental LO circuit. The IIP3 tones were separated by 10 MHz during measurement. B5 and B4 conversion gains are de-embedded from measurement with a spectrum analyzer. W1 and W2 conversion gains and noise are de-embedded from measurements with a noise figure meter.

Die Designator	B2	B4	W1	W2	W3	W4
Free Running Oscillator Frequency (GHz)	9.624	9.694	9.698	9.665	9.731	9.754
DC current (mA, No LO)	14.912	14.634	14.083	14.310	14.12	13.98
Conversion Gain to I port (dB)	-10.66	-10.26	-10.14	-9.05	-	-
Conversion Gain to Q port (dB)	-10.72	-10.75	-10.30	-9.5	-	-
Conversion Gain Total (dB)	-7.68	-7.48	-7.21	-6.28	-	-
IIP3 (dBm)	-	10.50	-	-	-	-
Noise Figure to I port (dB)	-	-	10.50	9.39	-	-
Noise Figure to Q port (dB)	-	-	10.07	9.58	-	-
Quadrature Phase (deg)	-	-	-	-	92.38	93.02
Amplitude Mismatch (%)	0.70	5.64	1.84	5.18	9.43	4.95

Table 8. General performance data for the quadrature coupled, fundamental LO circuit. The IIP3 tones were separated by 10 MHz during measurement. B2 and B4 conversion gains are de-embedded from measurement with a spectrum analyzer. W1 and W2 conversion gains and noise are de-embedded from measurements with a noise figure meter.

Figure 65 through Figure 70 provide specific performance measurements versus the available power from the reference LO source. Each figure plots data for multiple measured die. The color of each trend indicates data from a particular die.

The measured injection locking ranges for the fundamentally referenced quadrature conversion circuits are shown in Figure 65 and Figure 66, below. These circuits filter, amplify, and buffer the reference LO signal and use the resulting outputs to injection lock the differential LC oscillators. There is no amplifier saturation, at reasonable input levels, before injection locking, so an increase in the LO signal power should always correspondingly increase the power of the injection locking signal. This results in a continuous increase in the locking range, but with diminishing gain as the reference LO power increases. The measured trends are as expected for both the quadrature-coupled and uncoupled circuits; however, the ranges are 150 MHz to 200 MHz less than predicted in section 4.2 for the uncoupled circuits. The coupled circuits exhibit locking ranges in closer agreement with simulation. The discrepancy could be a result of better tuning of the resonant frequency of the coupled oscillators versus the uncoupled oscillators. The tuning should match, in terms of center frequency, the tuning of the preceding conditioning stages for the injection locking signals. In measurement, the uncoupled circuits oscillate approximately 400 MHz above the intended design frequency of 9.4GHz, whereas the quadrature-coupled circuits oscillate 300 MHz above that frequency. In simulation, both circuits oscillate at 9.4 GHz.

The strength of the LO reference signal, although it improves the locking range, should ideally have no effect on the conversion gain of the IQ mixer. Figure 69 and Figure 70 plot the measured variation in conversion gain with an increase in the reference signal power. This change is the result of a slight addition of current from the injection

locking pair, within each oscillator, to the differential outputs of the oscillator as the input power increases. The measured values are in good agreement with simulation, except for an increase in the conversion gain of the uncoupled circuit at low reference powers. In Table 7, these same circuits show an unusually high amplitude mismatch that is not seen with the other samples measured. A possible explanation is that there was a measurement issue that arose from the placement of the probes for this circuit. B4 and B5 were not wirebonded and the proximity of the DC probe to the circuit or to the other probes may have been an issue for the uncoupled circuit in particular. Conversion gain can also vary depending on how close the oscillator is locked to its resonant frequency, which is plotted based on simulation in section 4.2.

For the fundamentally referenced circuits, power dissipation is relatively constant regardless of the LO input conditions. This is illustrated in the Figure 67 and Figure 68 and agrees with the simulated current requirements.

Figure 71 and Figure 72 plot data related to image rejection ratio for the uncoupled and quadrature coupled circuits, respectively. Parts (a) and (d) of these figures plot expected values of the IRR assuming that the I and Q IF signals are summed after a perfect quadrature hybrid. The IRR plots are calculated trends that take into account the measured phase and amplitude mismatches, which are also plotted in the two figures.

For the uncoupled circuits, referring to Figure 71f, the measured variation in phase with frequency is similar to what was found in simulation. The average phase, however, deviates from the simulated, Figure 35, nominal phase and is different between the two samples measured. Also, as indicated by Figure 71b and Figure 35, there is a stronger dependence of the phase on the power of the reference LO than in simulation.

A nominal error in phase at the quadrature outputs of the poly-phase filter can be caused by the parasitic capacitances of its resistors[12]. These parasitic capacitances, however, are well modeled in simulation. The measurements show inconsistency between the two samples, suggesting that the errors are the result of process variation. Component mismatch in the polyphase filter affects amplitude more than phase, to which the network has a broadband response, so the phase error in the measurements of Figure 71 can be most likely attributed to errors in the tanks of the LC oscillators and the narrowband differential amplifiers. The voltage across an LC tank, excited by a current i_{tank}, at a frequency, ω, can be shown to be:

$$v_{tank(\omega)} = i_{tank} \frac{j\omega\omega_0 L(1+Q^2)}{j\omega Q - \omega_0(1+Q^2)\left(\frac{\omega^2}{\omega_0^2} - 1\right)} \qquad \text{(Eq. 5.2)}$$

The above represents a parallel LC tank with a resistance in series with the inductor that is related to the Q as in section 3.2.2. ω_0 is the resonant frequency of the tank. The tank capacitance is rewritten in terms of ω_0 and inductance, L. The argument of (Eq. 5.2) represents the phase shift and is shown below:

$$\emptyset = Tan^{-1}\left(\frac{Im[v_{tank}(\omega)]}{Re[v_{tank}(\omega)]}\right) = Tan^{-1}\left(-\frac{(1+Q^2)(\omega-\omega_0)(\omega+\omega_0)}{Q\omega\omega_0}\right) \quad \text{(Eq. 5.3)}$$

Figure 63 shows the phase shift, according to (Eq. 5.3), for various off-resonant frequencies of the LC tank, over ±10% of the resonant frequency. Two trends are plotted, one for the differential amplifier stages, Q=13.5, and another for the oscillators, Q=15.7. Considering only the two differential amplifiers, if the tanks were to differ in their resonant frequencies by just 0.5%, the resulting phase error, based on (Eq. 5.3), would fall between 7° and 8°. Thus, it is reasonable to suspect that tank mismatches are contributing to the process-related phase error observed in the final quadrature. These results make a case for quadrature coupling, given that such coupling can be expected to enforce sufficient quadrature accuracy in the final oscillator stages.

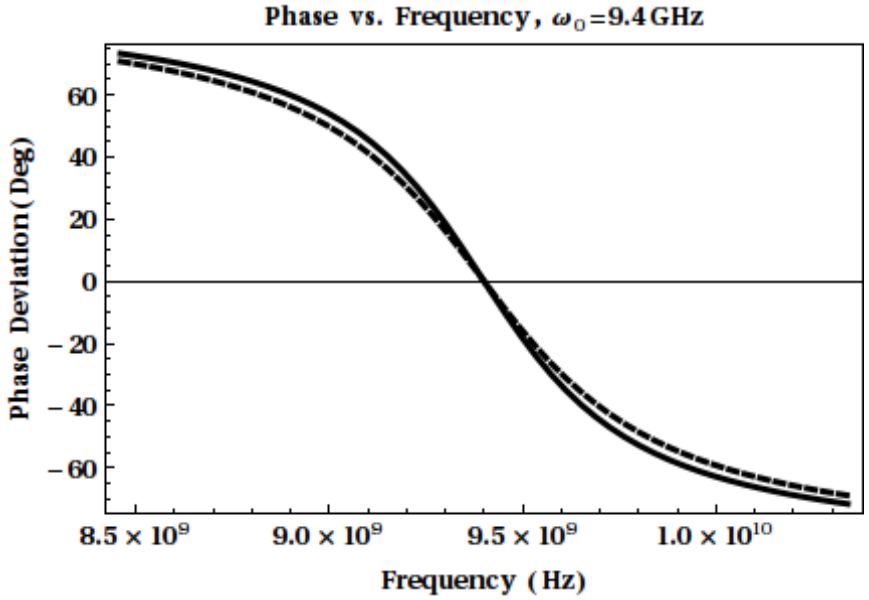


Figure 63. Voltage and current phase difference for an LC tank over a ω_0 ±10% range in frequency, where ω_0=9.4 GHz. The tanks plotted have a Q of 13.5(dashed) and 15.7(solid).

The amplitude mismatch observed in Figure 71 can also be explained by the effect of process variation on the tank resonant frequencies. A difference in the resonant frequencies of the two tanks will result in a difference of the tank voltage magnitudes at a particular frequency. (Eq. 5.2) can be manipulated to show how the relative magnitude varies away from the resonant frequency:

$$\frac{|v_{tank}(\omega)|}{|v_{tank}(\omega_0)|} = \frac{Q\omega\omega_0}{\sqrt{Q^2\omega^2\omega_0^2 + (1+Q^2)^2(\omega^2-\omega_0^2)^2}} \qquad \text{(Eq. 5.4)}$$

According to (Eq. 5.4), if the frequency of the tank input current is 1% off resonance, the tank voltage will change by 5%. This does not directly relate to Figure 71, which plots the amplitude mismatch of the two quadrature IF signals at the outputs of the mixer. The actual relationship is complicated by the downconversion process. The mixer tends to lessen amplitude mismatch due to the LO because of the nonlinear relationship of the gate voltage and drain current of the current-commutating transistors in the mixer[18]. Nonetheless, process variation of the LC tanks presents a reasonable explanation for the amplitude mismatches observed. Such mismatches would not be corrected with quadrature coupling and this represents a drawback, in general, to the use of the injection-locked oscillators as final-stage matched amplitude limiters. The tanks must be designed for the best possible match and, if the match is not sufficient, the Q must be lowered for a more gradual slope to the trend plotted in Figure 63. Lowering the Q will, however, reduce the amplitude of the LO, requiring the mixers to be re-optimized and detracting from the achievable conversion gain.

The plots provided in Figure 72 show the measured performance of the fundamental-referenced circuits with quadrature-coupled oscillators. The quadrature-coupled oscillators show a clear advantage in phase performance. In Figure 72f, the phase deviates very little between the two samples because the quadrature relationship is enforced by the coupling rather than preceding stages and the matching of those stages. The phase also does not change significantly with input power, as shown in Figure 72b. Indeed, quadrature coupling does appear to compensate for phase error from the polyphase filter and preceding amplifiers that supply the injection-locking signals.

The difference in phase between the two quadrature-coupled samples that is due to process variation is little, approximately 1°. The nominal mismatch of the two samples varies with the frequency of the injection-locking signal and can reach up to 6° at the upper extreme of the locking range. At the resonant frequency of the quadrature oscillator, the nominal mismatch is about 3°. This is likely the result of a systematic mismatch in phase shift between the differential coupling lines that connect the two oscillators. Such mismatch is possible in the circuit layout of this thesis because the coupling lines follow different paths and can not be laid out perfectly symmetrically. Similar mismatch is also observed in fully-extracted layout simulations, such as Figure 41 and Figure 53. (Eq. 5.5) is a solution for the phase difference of the two outputs of a quadrature oscillator. This solution is adapted from [18] to account for only the mismatches between the natural resonant frequencies of the two tanks and the phase

shifts of the two coupling lines. i_{osc} and i_c are the AC current magnitudes driven by the cross-coupled and coupling transistor pairs in the coupled oscillators. ω_0 is the average resonant frequency of the LC tanks and $\Delta\omega_0$ is the frequency mismatch between the two. Φ is the average phase shift through the two coupling lines and $\Delta\Phi$ is the mismatch in their phase shifts. Q is the tank Q-factor and ψ is the phase difference of the quadrature oscillator outputs.

$$\psi = \frac{\Delta\Phi}{2} - \frac{\pi}{2} - \frac{\Delta\omega_0 iQ\left(1 + \frac{i_c^2}{i^2} + \frac{2i_c Sin(\Phi)}{i}\right)}{\omega_0 I_C\left(\frac{i_c}{i} + Sin(\Phi)\right)} \qquad \text{(Eq. 5.5)}$$

It is important to note that (Eq. 5.5) does not include the effects of injection locking, which would account for the variation with frequency and amplitude of quantities plotted in Figure 72. The analysis is useful when comparing results near the resonant frequency of the quadrature oscillator. If the nominal mismatch of the LC tank frequencies, $\Delta\omega_0$, is zero then (Eq. 5.5) indicates that the phase error of the quadrature outputs is equal to half of the mismatch in the phase shifts, $\Delta\Phi$,of the oscillator coupling lines. According to simulation, the quadrature phase error is 5°, suggesting that $\Delta\Phi$ is 10° (2×5°). This agrees with the phase error measured near the resonant frequency of the quadrature oscillator. Note that the resonant frequency of the quadrature oscillator is greater than ω_0 of either LC tank, which is one of the possible stable modes of such an oscillator.

Amplitude mismatch of the quadrature outputs is still observed with the quadrature-coupled circuits and is worse than what is observed with the uncoupled circuits. Quadrature-coupling does not provide any correction for amplitude mismatch between the two oscillators and, in fact, exacerbates the problem. (Eq. 5.6) provides a solution for the two output amplitudes, derived from the analysis in [18]. The amplitudes are based in part on the phase, ψ, provided by (Eq. 5.5). $\Delta\Phi$ will cancel out of (Eq. 5.6) when ψ is substituted. The quantity, R, is related to the Q and models the loss of the oscillator tank.

$$A_1 = \frac{4R}{\pi}\left(i - i_c Cos\left(\Phi + \frac{\Delta\Phi}{2} - \psi\right)\right)$$
$$A_2 = \frac{4R}{\pi}\left(i + i_c Cos\left(-\Phi + \frac{\Delta\Phi}{2} - \psi\right)\right) \qquad \text{(Eq. 5.6)}$$

Given that $\Delta\Phi$ cancels out of (Eq. 5.6), mismatch between the coupling line phase shifts has no effect on the amplitude mismatch. The average coupling line phase shift, Φ, does affect the output amplitudes but, if $\Delta\omega_0$ is zero when ψ is substituted, both amplitudes will be equally affected and will not differ. Therefore, the coupling lines do not contribute to nominal amplitude error unless there is a source of nominal mismatch, $\Delta\omega_0$, between the tank resonances.

There are no remaining quantities treated in (Eq. 5.6) that can account for nominal amplitude mismatch. Such mismatch is predicted by simulation, however, and is observed at about the same level in the measurements. Therefore, the mismatch must be

caused by phenomena untreated in (Eq. 5.6); possibly by interactions between the quadrature oscillator and the external circuits it is connected to. Some internal possibilities include systematic mismatch of the tail currents of the various differential pairs, or of the Qs of the two resonant tanks. The tail current mismatches are excluded in the simplifications above but treated in [18], as are the effects of dissimilar tank quality factors. These are not probable sources of the mismatch, however; simulation, which shows the nominal phase mismatch, does not show either of these phenomena. This suggests an external cause and the most likely explanation seems to be the polyphase filter. It has been observed that the polyphase filter can affect the startup mode of the quadrature oscillator, even when it is not driven (ie. no LO reference is provided to the system). A more thorough analysis of the quadrature oscillator with the polyphase filter included is needed to confirm this possibility.

Although a considerable portion of the amplitude mismatch is nominal, process variation can also account for significant mismatch, as observed in the two measurements of Figure 72. Figure 64 shows how the amplitude mismatch varies, according to (Eq. 5.5) and (Eq. 5.6), with the mismatch in the tank resonant frequencies. This trend is steeper than what can be predicted with (Eq. 5.4) for the uncoupled oscillators. Also shown is the rate at which quadrature phase error develops, assuming $\Delta\Phi = \Phi = 0$. The values for i and i_c are taken from simulation and are 2.4 mA and 1.4mA, respectively.

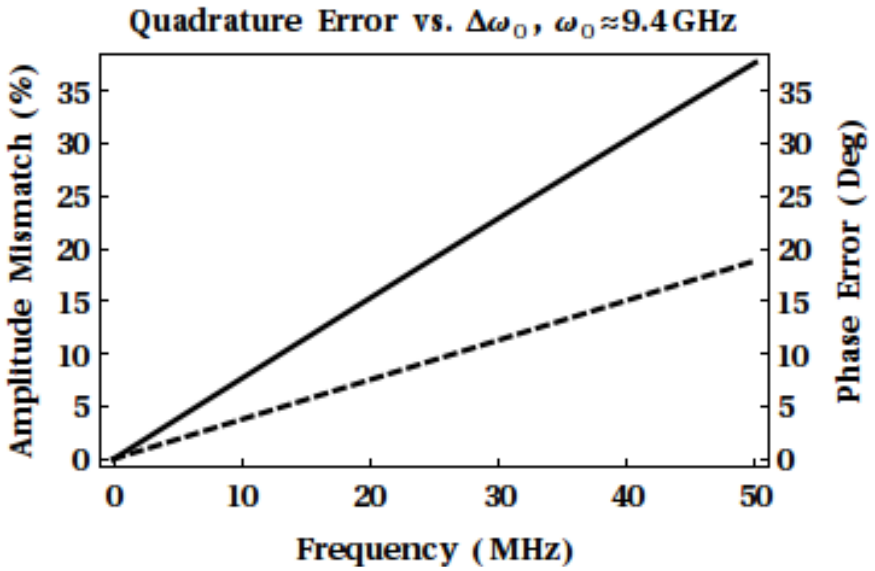


Figure 64. Quadrature amplitude mismatch(solid) and phase error(dashed) versus the difference in resonant frequency of the two tanks comprising the quadrature oscillator. The resonant frequencies of the two tanks are centered around 9.4 GHz.

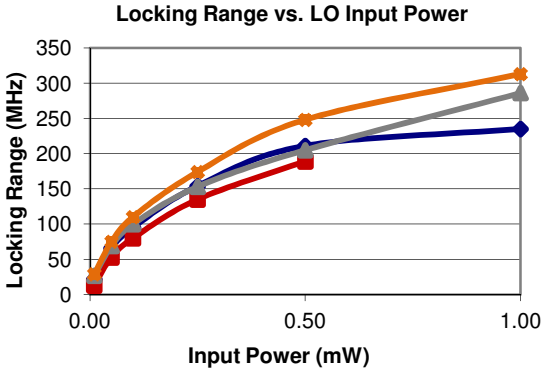


Figure 65. Measured injection locking range versus the fundamental reference LO power for four fabricated circuits with independent LC oscillators.

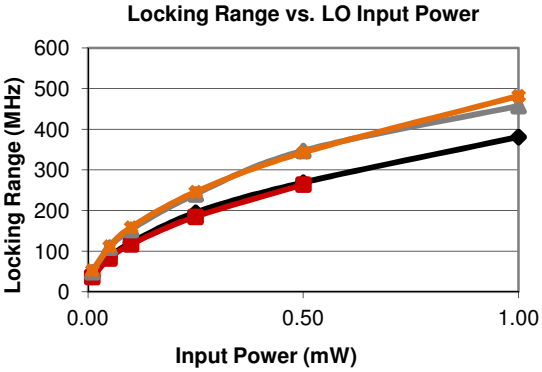


Figure 66. Measured injection locking range versus the fundamental reference LO power for four fabricated circuits with quadrature-coupled LC oscillators.

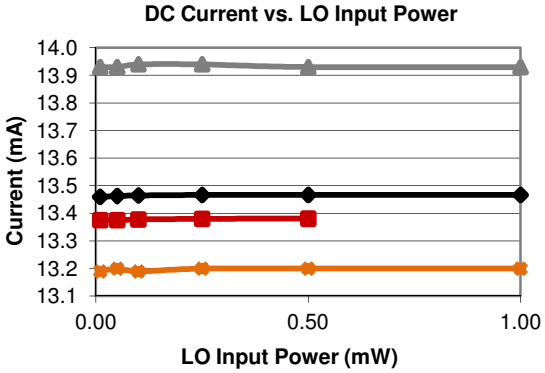


Figure 67. Total DC current drawn by a circuit versus the fundamental reference LO power for four fabricated circuits with independent LC oscillators.

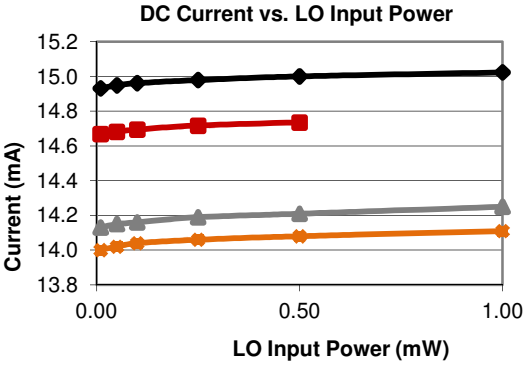


Figure 68. Total DC current drawn by a circuit versus the fundamental reference LO power for four fabricated circuits with quadrature-coupled LC oscillators.

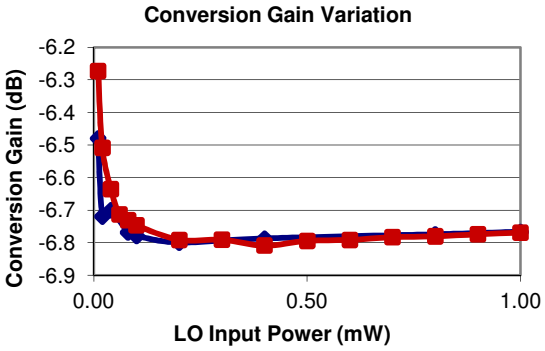


Figure 69. Measured conversion gain versus the fundamental reference LO power for two fabricated circuits with independent LC oscillators.

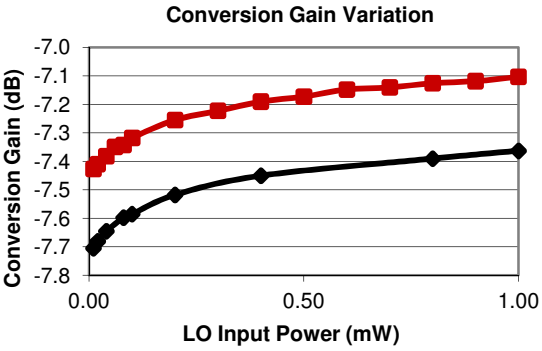


Figure 70. Measured conversion gain versus the fundamental reference LO power for two fabricated circuits with quadrature-coupled LC oscillators.

Above: Collection of figures plotting measured performance parameters of fundamental LO referenced circuits on various die. Data from B2,B4, B5, W3, and W4 are plotted in black, red, blue, grey and orange, respectively.

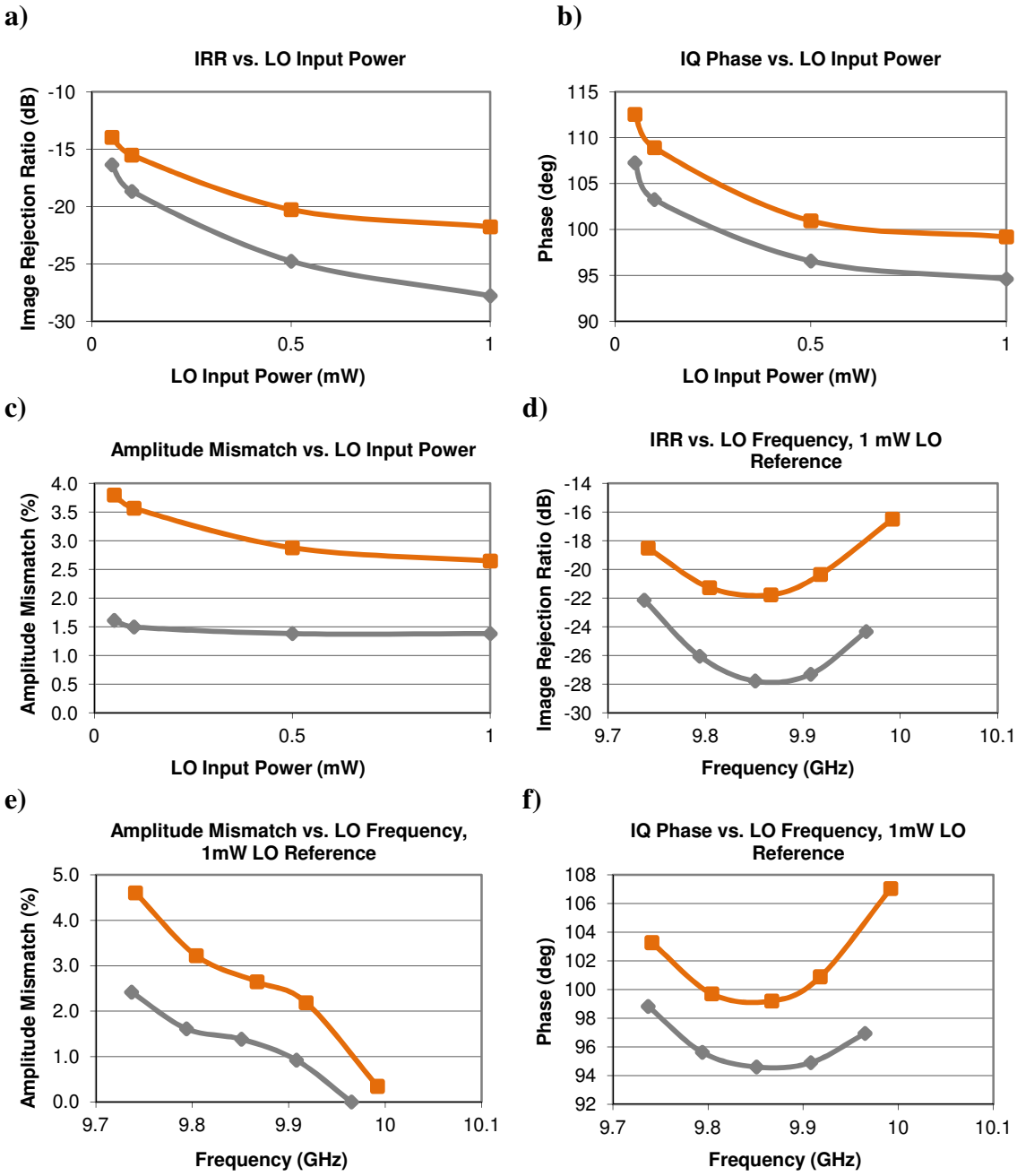


Figure 71. Measured parameters related to the image rejection ratio(IRR) for circuits with independent LC oscillators and a fundamental LO reference. Data is plotted versus the power or frequency of the reference. Die W3 and W4 are plotted in grey and orange, respectively.

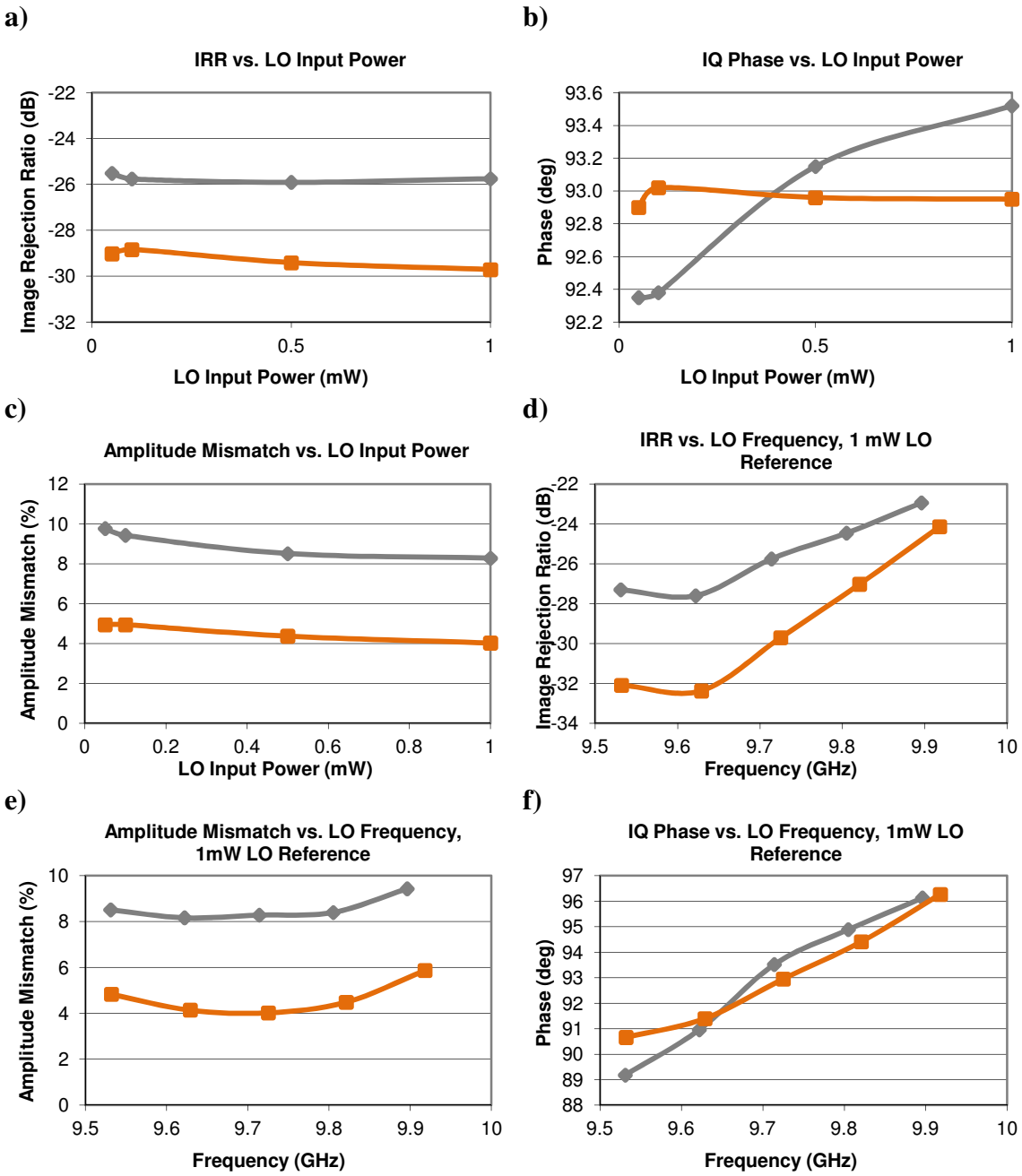


Figure 72. Measured parameters related to the image rejection ratio(IRR) for circuits with quadrature-coupled LC oscillators and a fundamental LO reference. Data is plotted versus the power or frequency of the reference. Die W3 and W4 are plotted in grey and orange, respectively.

5.3 Sub-Harmonic System Performance Measurements

Table 9 and Table 10 outline the measured performance parameters for the quadrature conversion systems with sub-harmonic LO references. Table 9 summarizes systems with uncoupled LC oscillators and Table 10 summarizes the systems with quadrature-coupled LC oscillators. The measured parameters are listed in columns that indicate the die on which a circuit was tested. Each die contains each of the four variants of the quadrature conversion system covered in this section and section 5.2. The die considered in this section are labeled B4, B5, W1, W2, W3, W4, and W5. The measurement procedures followed with each of these die are summarized by Table 6. As before, the die B4 and B5 were contact probed. W1 through W5 were wire-bonded for easy connection of DC signals and to permit probe positioning for specific measurements.

Die Designator	B4	B5	W1	W2	W5
Free Running Oscillator Frequency (GHz)	9.648	9.639	9.624	9.641	9.654
DC current (mA, No LO)	16.14	15.29	15.93	15.60	15.06
Conversion Gain to I port (dB)	-11.74	-11.79	-11.14	-11.23	-
Conversion Gain to Q port (dB)	-11.61	-11.59	-11.02	-11.18	-
Conversion Gain Total (dB)	-8.66	-8.68	-8.07	-8.19	-
IIP3 (dBm)	7.84	7.98	-	-	-
Noise Figure to I port (dB)	-	-	12.32	12.09	-
Noise Figure to Q port (dB)	-	-	12.43	11.66	-
Quadrature Phase (deg)	-	-	-	-	86.65
Amplitude Mismatch (%)	1.50	2.30	1.38	0.58	6.91

Table 9. General performance data for the uncoupled, sub-harmonic LO circuit. The IIP3 tones were separated by 10 MHz during measurement. B4 and B5 conversion gains are de-embedded from measurement with a spectrum analyzer. W1 and W2 conversion gains and noise are de-embedded from measurements with a noise figure meter.

Die Designator	B4	W1	W2	W3	W4
Free Running Oscillator Frequency (GHz)	No Start	No Start	No Start	10.031	No Start
DC current (mA, No LO)	15.525	15.135	15.284	15.02	14.25
Conversion Gain to I port (dB)	-13.72	-14.40	-14.09	-	-
Conversion Gain to Q port (dB)	-13.46	-14.67	-14.12	-	-
Conversion Gain Total (dB)	-10.58	-11.52	-11.09	-	-
IIP3 (dBm)	6.18	-	-	-	-
Noise Figure to I port (dB)	-	15.47	14.98	-	-
Noise Figure to Q port (dB)	-	15.67	15.12	-	-
Quadrature Phase (deg)	-	-	-	97.42	98.87
Amplitude Mismatch (%)	2.99	3.11	3.45	2.99	4.58

Table 10. General performance data for the quadrature coupled, sub-harmonic LO Circuit. The oscillator did not independently start in this version of the circuit. The IIP3 tones were separated by 10 MHz during measurement. The B4 conversion gains are de-embedded from measurement with a spectrum analyzer. W1 and W2 conversion gains and noise are de-embedded from measurements with a noise figure meter.

Figure 73 through Figure 78 provide specific performance measurements versus the available power from the sub-harmonic reference LO source. Each figure plots data for each die from which complete data related to the measurement was collected.

Measured injection locking ranges for sub-harmonic circuits having uncoupled LC oscillators are provided by Figure 73. In the case of circuits referenced to a sub-harmonic LO, increasing the power of the reference LO signal will eventually saturate the input stage. When that happens, the injection locking signals that are generated for the LC oscillators will cease to increase and the injection locking range will remain relatively constant. The saturating power is seen to occur with reference LO power levels greater than about 2 mW. This behavior, and the measured ranges themselves, agree closely with simulation. Increasing the input signal beyond the saturating power also has very little effect on the conversion gain, as seen in Figure 77 and Figure 78 for both quadrature-coupled and uncoupled circuits. Above the saturating power, the sub-harmonic circuits do a better job of keeping the conversion gain constant when compared to the fundamentally referenced circuits. This is due to the input balun, which was also designed to act as a first-stage amplitude limiter when saturated. The fundamental reference circuits have no balun.

The quadrature coupled oscillators in the sub-harmonically referenced circuits did not start on their own when powered up. When an LO reference was present and varied in frequency there was no distinguishable injection-locking range and the circuit, instead,

behaved as a narrow-band amplifier. One circuit, on die W3, did start up at a free-running frequency and exhibited a distinct locking range. This is the locking range reported in Figure 74. The range is twice that predicted in simulation, most likely due to an oscillation that is much weaker than predicted. This is supported by the measured conversion gain, which is about 3dB less than predicted by simulation.

The difficult start up observed with the quadrature-coupled circuits can be explained by optimizations that were made to the oscillator topology to support a sub-harmonic LO reference and quadrature coupling. The injection-locking signals presented to the oscillators in the sub-harmonic referenced circuits are single-ended and weaker than that of the fundamental referenced circuits. The strength of the oscillations had to be lessened by reducing the size(channel width) of the cross-coupled transistors so that the circuit could still be injection-locked over a reasonable bandwidth. The injection-locking transistors were also increased in size to amplify their effect. Finally, the quadrature-coupling pair of transistors that are required for coupled oscillators were added. These place an additional load on the oscillator, further reducing the strength of the oscillations. The contribution of all transistors to capacitive parasitics at the tank must be low enough that the tank can still resonate at 9.4 GHz, which limits the aggregate size of all transistors involved in the topology. These issues combine to make the sub-harmonic and quadrature-coupled circuit a worst-case scenario for startup. Simulations performed prior to fabrication showed that the oscillators would start up and exhibit a defined locking range, albeit barely reaching the amplitude required to drive the mixer. In reality, it

appears that not enough margin was provided for the fabrication, especially considering the shifts in resonant frequency that were observed (about 250 MHz for the sub-harmonic referenced circuits).

The oscillators in the quadrature-coupled circuits that did not start could often be started by applying a reference LO near the resonant frequency of those oscillators. Upon removal of that signal, the oscillators would continue to oscillate at the resonant frequency. This suggests that the oscillator has two stable modes, with one mode being critically damped. The two modes could be related to the two stable modes of the basic quadrature-coupled oscillator. Interestingly, the phase measurement of Figure 80f, for which the corresponding circuit did start up, shows a near phase reversal within the locking range. A phase reversal would be seen between the two modes of a quadrature oscillator, although, for this implementation, one mode would be competing with the phase injected by the polyphase filter.

For both the uncoupled and quadrature-coupled sub-harmonic referenced circuits, the power dissipation increases with increasing power from the LO reference source. This is illustrated in Figure 75 and Figure 76. The reason for this is that the signal produced by the frequency doubler has a proportional DC component in its doubled output signal. The change in current for these circuits is as expected when compared to simulation.

Figure 79 and Figure 80 plot IRR related measurements for the uncoupled and quadrature-coupled circuits, respectively. For the quadrature-coupled circuits, data from only one die, the die containing the self-starting oscillator, is plotted. For the uncoupled circuits, only one die is plotted because of a probe-to-wirebond short that invalidated the second set of measurements that were taken. As in section 5.2, the quadrature-coupled circuit exhibits better phase performance over frequency. Amplitude mismatch is worst for the uncoupled oscillator for the particular case plotted in Figure 79c, but is generally better than the quadrature coupled case, as indicated by Table 9. These results are in agreement with the observed performance differences between the quadrature coupled and uncoupled oscillators in section 5.2.

The primary drawback to the sub-harmonic topologies is a weaker injection-locking signal. This is due to the use of a single-ended polyphase network and the active circuits used for frequency doubling that can produce a limited maximum signal swing. These limitations require adjustments to the oscillator stages that reduce the final achievable conversion gain. In the case of the quadrature-coupled oscillator, this resulted in a circuit that does not function reliably. The benefit of the sub-harmonic topology is that is can be referenced by a signal distributed at a lower frequency. In the intended application, this would reduce power loss in the distribution network. This gain, however, may be offset by the fact that the fundamental referenced circuits require ten times less input power.

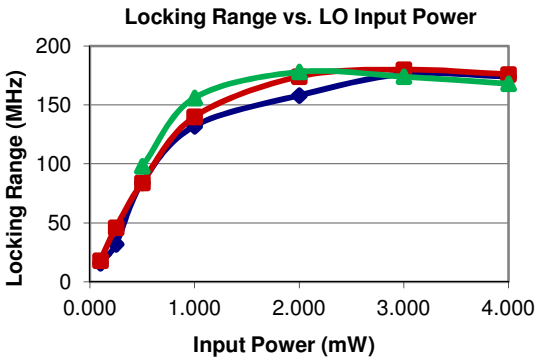


Figure 73. Measured injection locking range versus the sub-harmonic reference LO power for three fabricated circuits with independent LC oscillators.

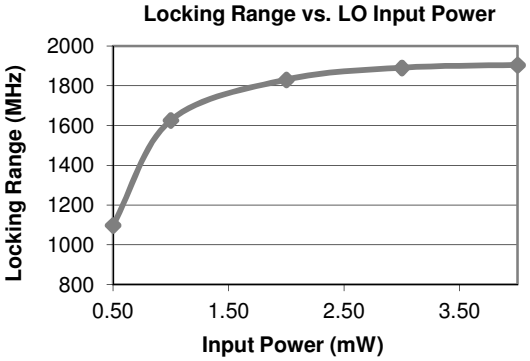


Figure 74. Measured injection locking range versus the sub-harmonic reference LO power for two fabricated circuits with quadrature-coupled LC oscillators.

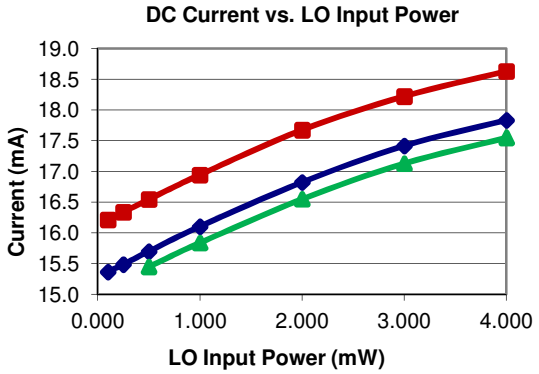


Figure 75. Total DC current drawn by a circuit versus the sub-harmonic reference LO power for three fabricated circuits with independent LC oscillators.

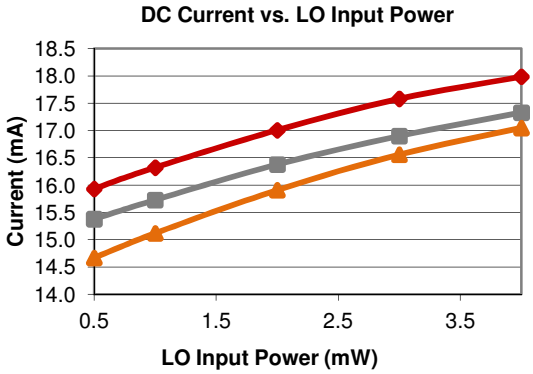


Figure 76. Total DC current drawn by a circuit versus the sub-harmonic reference LO power for the fabricated circuit with quadrature-coupled LC oscillators.

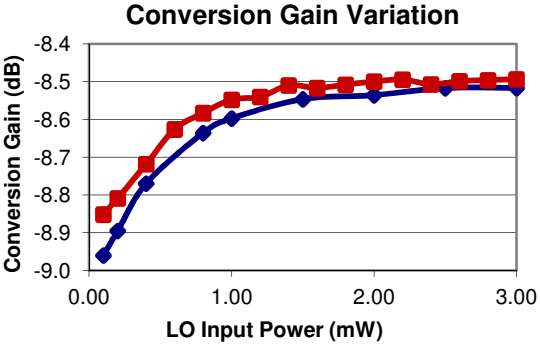


Figure 77. Measured conversion gain versus the sub-harmonic reference LO power for two fabricated circuits with independent LC oscillators.

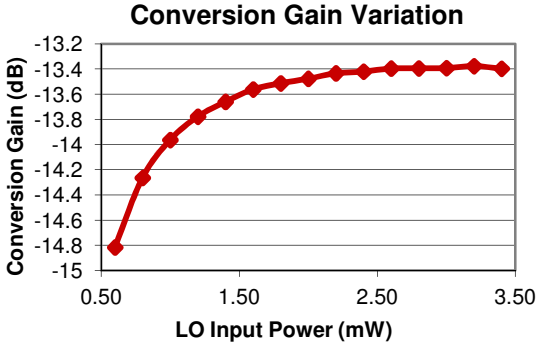


Figure 78. Measured conversion gain versus the sub-harmonic reference LO power for the fabricated circuit with quadrature-coupled LC oscillators.

Above: Collection of figures plotting measured performance parameters of sub-harmonic LO referenced circuits on various die. Data from B4, B5, W3, W4, and W5 are plotted in red, blue, grey, orange, and green, respectively.

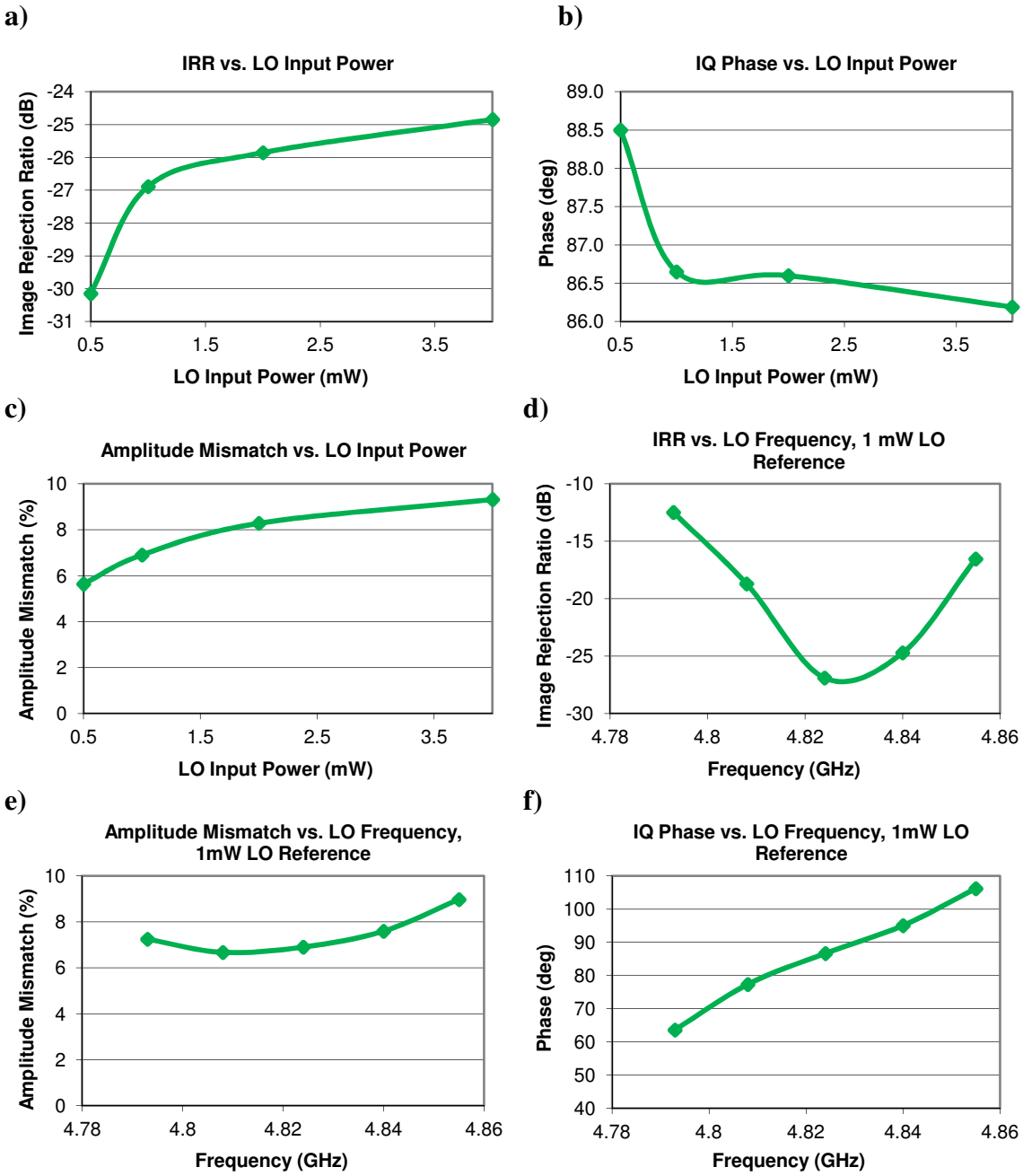


Figure 79. Measured parameters related to the image rejection ratio(IRR) for the circuit from die W5 with independent LC oscillators and a sub-harmonic LO reference. Data is plotted versus the power or frequency of the reference.

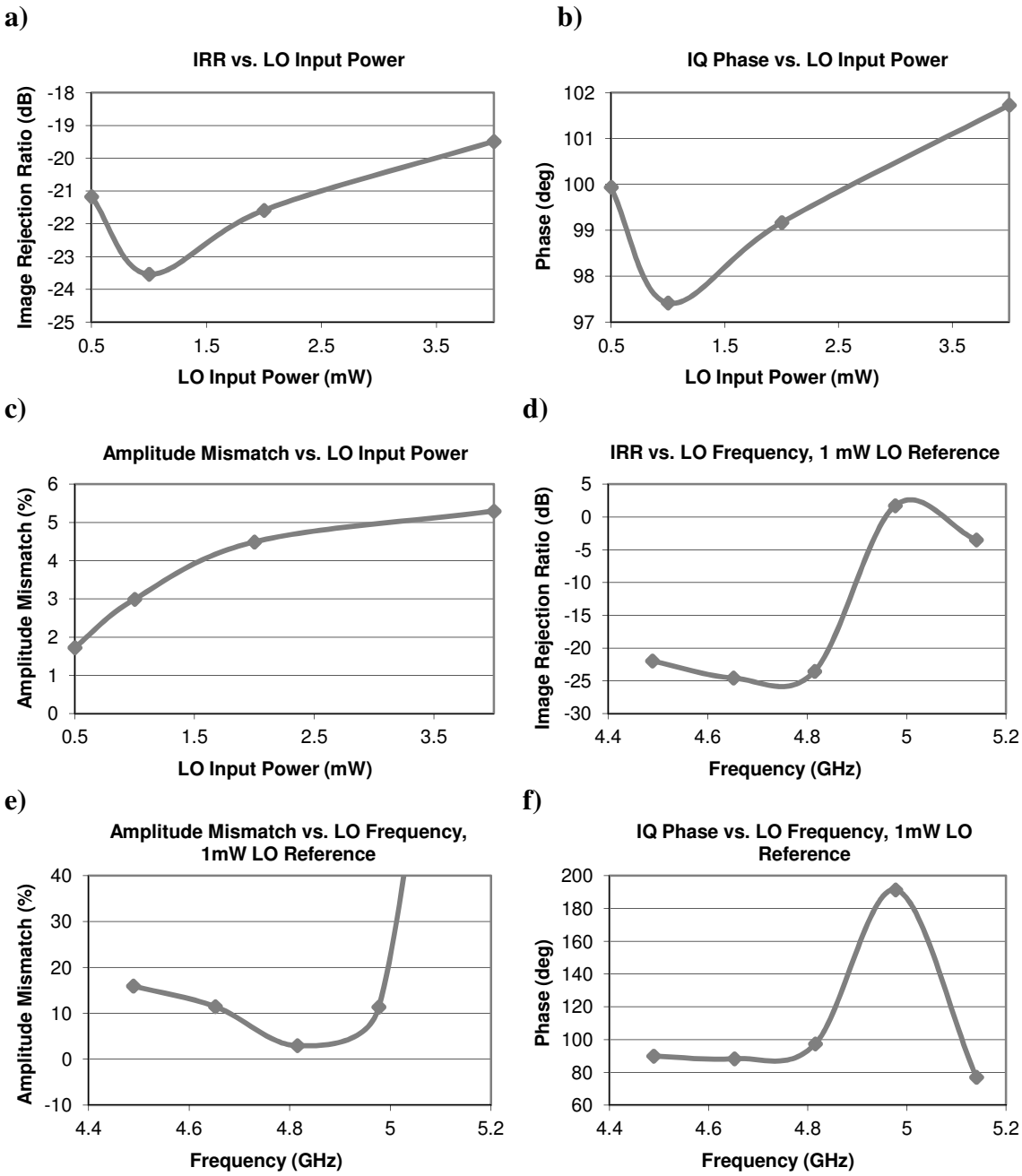


Figure 80. Measured parameters related to the image rejection ratio(IRR) for the circuit from die W4 with quadrature-coupled LC oscillators and a sub-harmonic LO reference. Data is plotted versus the power or frequency of the reference.

CHAPTER 6

CONCLUSIONS

This thesis examined the architecture and implementation of an integrated quadrature conversion system locked to an external LO reference. Slight variations of a basic architecture allowed for the realization of four different discrete implementations of that system. Two implementations were designed to be referenced to the first sub-harmonic of a desired LO frequency and the second two were referenced at the same frequency as the LO. In general the latter, fundamental referenced, implementations performed more favorably. This was predominantly due the stronger signals available for oscillator injection-locking that were produced by these variants.

The sub-harmonic referenced circuits suffered from a weak injection-locking signal that required compromises in the design of the injection-locked oscillators. In the quadrature-coupled version, this resulted in a circuit that was essentially unusable. For these circuits, a single-ended signal was produced by a frequency doubling stage and subsequently suffered loss through a polyphase network before being used to injection-lock the oscillators. In contrast, the LO reference of the fundamental architecture first passed through a polyphase network and was then amplified through a fully-differential signal conditioning chain to produce the injection-locking signal. Thus, in the fundamental circuits, the polyphase network did not introduce loss after a swing-limited

amplifier stage and the maximum signal swings were essentially doubled because the signal was fully differential.

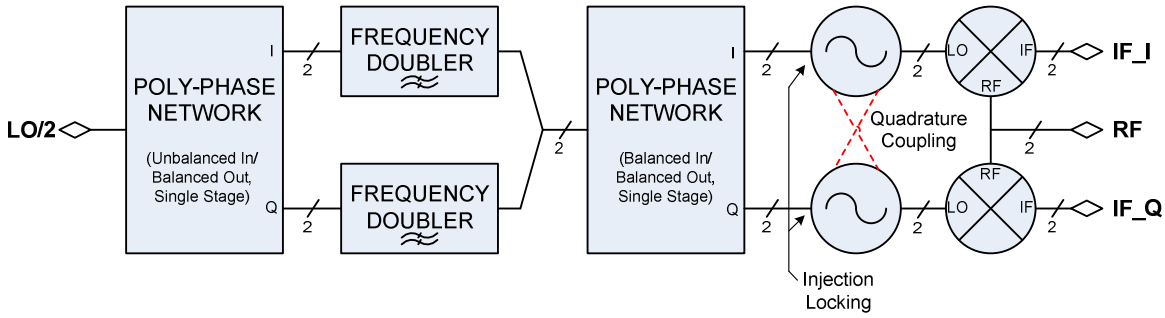


Figure 81. Proposed sub-harmonic architecture for improved injection-locking performance.

Figure 81 presents a modified sub-harmonic architecture intended to increase the maximum amplitude of the injection-locking signal so that better performance can be achieved from the oscillators. In this topology, the sub-harmonic LO reference enters a polyphase network that produces differential quadrature I and Q outputs. This could be similar to, or a single stage version of, the network shown in Figure 22. Each differential output, I or Q, drives the differential input of a frequency doubler. The single ended outputs of each of the doublers would then be twice the frequency of the LO reference and they would be 180° out of phase with each other. The outputs are treated together as a single differential signal and drive a second polyphase network. The quadrature differential outputs of that network then injection-lock each of the oscillators. Buffer amplifiers can be inserted between the frequency doublers and second polyphase filter, if

needed. Injection-locking is improved in this architecture because it is fully differential, increasing the maximum effective signal swing that can be presented to the oscillators. The sub-harmonic circuits, shown in Figure 7, have sufficient unused area in the layout for the second frequency doubler and its inductor.

Amplitude mismatch and phase error were potentially degraded in the fundamental referenced circuits due to the contribution of two sets of tank mismatches to the quadrature outputs; one set in the differential amplifiers and one set in the oscillator tanks. This is most evident in the circuit with uncoupled oscillators because the oscillators do not provide any correction of phase error introduced by the preceding differential amplifier stages. With increased input power, these amplifiers would not be a necessary part of the implementation; however, the power requirement would put a greater load on the external LO distribution network. If the input polyphase network was also reduced to a single stage, the need for additional power could be avoided and there would likely be no resultant drawback to phase performance[12]. A second iteration of fundamental referenced designs would benefit from the removal of the differential amplifiers and one stage of the polyphase network. These changes would also reduce the die real estate requirement.

Amplitude mismatch between quadrature LO signals that results from mismatches between the LC tanks of the final oscillator stages is a drawback suffered by any of the examined implementations. The measured amplitude mismatches are typically as much

as 5% and can be limiting to the overall image rejection ratio. This could suggest that additional dedicated amplitude limiting stages would be beneficial, but such stages would most likely have a negative impact on the quadrature phase error. Tailoring the design and layout for the best possible matching of the LC tanks may be the best option.

The benefit of quadrature-coupling to phase error is evident when process mismatch is considered; however, the coupling can itself introduce errors. These include a nominal phase error and increased amplitude mismatch sensitivity. The nominal phase error is at least in part due to non-symmetry in the layout of the quadrature coupling lines. Analysis of the quadrature oscillator shows that long phase delays in the coupling lines are acceptable, and even desired[17][18], as long as the coupling lines between the two oscillators both introduce the same phase delay. The effect of coupling line phase delay mismatch is illustrated by (Eq. 5.5), where the mismatch, $\Delta\Phi$, adds directly to the output quadrature phase, ψ. Considering the implementation of this thesis, a modification to the layout of the coupling lines could be made that increases the length and phase shift of each line in the interest of keeping the two phase shifts well matched to each other, thereby reducing nominal phase error. This is illustrated by Figure 82. In this figure, the "I" oscillator(blue) has two outputs driven by antiphase current branches, I+ and I-, and two corresponding inputs, C_{I+} and C_{I-}, that couple current into those branches when driven by the other oscillator. The second "Q" oscillator(red) similarly has outputs, Q+ and Q-, and inputs, C_{Q+} and C_{Q-}. In Figure 82a, paths representative of the quadrature coupling lines used in the layout of this thesis are shown. Each end of a differential pair,

I+/I- or Q+/Q-, drives an equal length and symmetric connection to inputs that belong to the other oscillator, accurately maintaining the antiphase nature of the differential signal at either set of inputs. With the antiphase ends treated together as a pair, however, the resultant differential coupling line driven by the "I" oscillator is not length-matched or symmetric to that driven by the "Q" oscillator. This translates to phase delay mismatch of the coupling lines and nominal quadrature phase error. It is also worth noting that the crossover within the differential line driven by the "Q" oscillator introduces an asymmetry that can affect the ideal antiphase relationship of that signal.

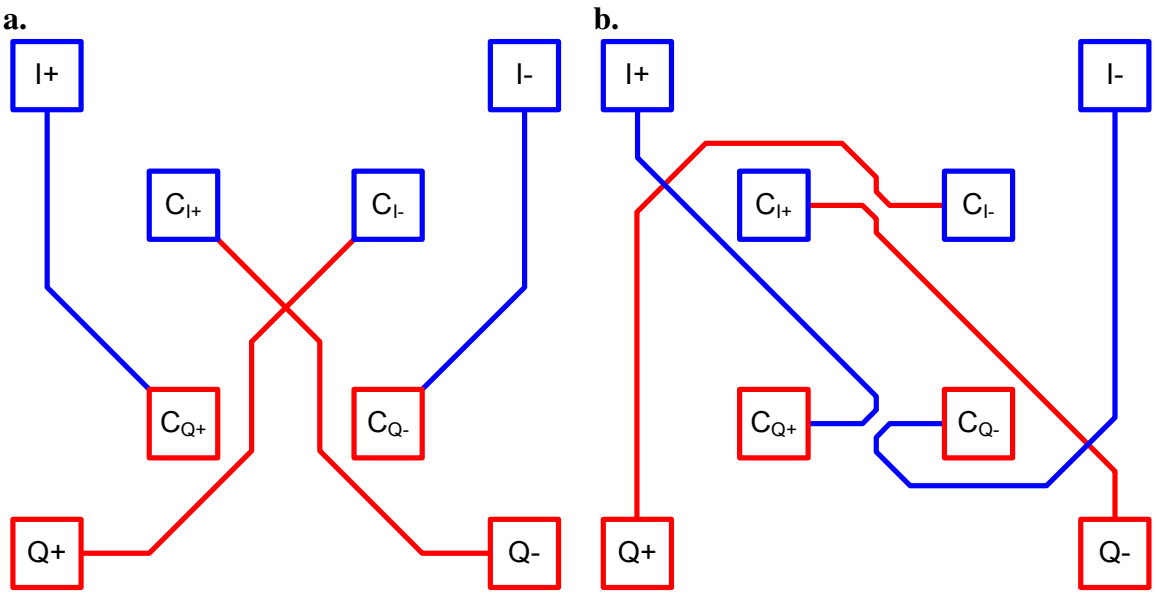


Figure 82. Possible paths for the layout of the quadrature coupling lines of a quadrature oscillator. In **a)** the layout of coupling lines for this thesis is shown. In **b)** a layout is presented to improve the overall matching of one set of coupling connections(blue) to the next(red).

In Figure 82b, the length of the connection driven by I+ matches that driven by Q- and the same is true for I- with respect to Q+. The connections are also, for the most part, rotationally symmetric(the implemented quadrature oscillator without coupling is symmetric horizontally, vertically, and rotationally). Considering the pairs as a whole, this means that the coupling line driven by the "I" oscillator matches, in length and symmetry, that from the "Q" oscillator. Two crossovers are also introduced, which are crossovers of connections from different differential signal pairs and can be used to maintain the symmetry. This arrangement, Figure 82b, should therefore be closer to matching the coupling line phase shifts by design. A drawback to Figure 82b is that the differential ends I-/I+ and Q-/Q+ no longer drive connections that are matched by design. This could be somewhat compensated by symmetrically adding length to the shorter of two connections from each oscillator. Any mismatch will manifest itself as imperfect antiphase at the differential inputs or equivalently a small common-mode signal at those inputs at the LO frequency. Nevertheless, a modification such as the one suggested by Figure 82b could help to resolve nominal quadrature phase mismatch issues in a revised design. Note that, although length matching is stressed in the foregoing explanation, the primary goal is to match the distributed parasitics of the coupling lines.

A better analytical understanding of the effects of injection-locking on the quadrature oscillators could help to reduce both phase error and amplitude mismatch. Including the polyphase filter in such an analysis would also be beneficial, as its interaction with the quadrature oscillators is likely to be responsible for part of the observed quadrature error,

nominal and process related. Additionally, it is important to note that the high operating frequency of circuits from this thesis, relative to the 180nm CMOS process, requires the effects of all parasitic delays, phase shifts, and mismatches to be considered where they are often ignored in many applications. [17] and [18] present methods of deliberately introducing a 90-deg phase shift to the quadrature coupling lines that are shown to reduce the effects of nominal and process related mismatch. Such modifications would require significant changes to the layout of this thesis, but could provide benefits to amplitude and phase performance if applied.

APPENDIX

FABRICATION PROCESS

The quadrature upconverter/downconverter and LO conditioning circuit was designed for the IBM 7RF process. This is a 180 nm RF CMOS process. The process details are protected by a non-disclosure agreement, however, general information, parametric test results and the corresponding extracted spice models, are freely available from MOSIS. The 7RF process provides a number of options, a subset of which is offered through MOSIS. For this project six metal layers were available. The first metal layer is copper, followed by 4 intermediate aluminum metal layers with identical thickness. The top layer is a thick aluminum layer suitable for wide low-resistance routing and for implementing the on-chip planar inductors.

The NFET and PFET devices for this process are specified for operation with a 1.8V supply. 3V and 5V options are also available from IBM with additional mask steps but these were not used or included in this fabrication run. The process also provides MIM capacitors, and models are provided for capacitors comprised of interdigitated fingers on the metal layers. The design was originally created with high-k MIM capacitors having double the capacitance density, however these were replaced with standard MIMs at the request of MOSIS (one less mask is required). Special resistors, the K1 BEOL, resistors are also available and offer, at the expense of lower sheet

resistance, improved tolerance and matching as well as low parasitic capacitance. In particular, these resistors are useful for the polyphase filters.

IBM provides design kits for layout, DRC, parasitic extraction, and simulation with the Cadence Virtuoso interface and associated cadence tools. DRC was also possible via Mentor Graphics Calibre and simulation models were provided for the Agilent ADS simulation interface.

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