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On Process Variation Tolerant Low Cost Thermal Sensor Design

Spandana Remarsu
University of Massachusetts Amherst

ON PROCESS VARIATION TOLERANT LOW COST THERMAL SENSOR DESIGN

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SPANDANA REMARSU

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SPANDANA REMARSU

Approved as to style and content by:

_____
Sandip Kundu, Chair

_____
Wayne Burleson, Member

_____
Massimo V. Fischetti, Member

_____
C. V. Hollot, Department Chair
Electrical and Computer Engineering

DEDICATION

To my Teacher, Family and Friends

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I am deeply thankful to my advisor, Professor Sandip Kundu for his encouragement, support and constant guidance throughout my graduate studies. I would like to thank Professor Max Fischetti and Professor Wayne Burleson for their feedback and constructive suggestions on my work. I have been fortunate to have worked with knowledgeable and friendly people at VLSI Circuits and Systems laboratory at UMass. I would also like to thank my vast list of friends in Amherst for making my stay here truly memorable. Finally, I would like to thank my mother and my fiancé Ravi for their endless love and support.

ABSTRACT

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SPANDANA REMARSU

B.E., E.C.E., ANDHRA UNIVERSITY, ANDHRA PRADESH, INDIA

M.S.E.C.E., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Professor Sandip Kundu

Thermal management has emerged as an important design issue in a range of designs from portable devices to server systems. Internal thermal sensors are an integral part of such a management system. Process variations in CMOS circuits cause accuracy problems for thermal sensors which can be fixed by calibration tables. Stand-alone thermal sensors are calibrated to fix such problems. However, calibration requires going through temperature steps in a tester, increasing test application time and cost. Consequently, calibrating thermal sensors in typical digital designs including mainstream desktop and notebook processors increases the cost of the processor. This creates a need for design of thermal sensors whose accuracy does not vary significantly with process variations. Other qualities desired from thermal sensors include low area requirement so that many of them maybe integrated in a design as well as low power dissipation, such that the sensor itself does not become a significant source of heat. In this work, we developed a process variation tolerant thermal sensor design with (i) active compensation circuitry and (ii) signal dithering based self calibration technique to meet the above

requirements in 32nm technology. Results show that we achieve ±3ºC temperature accuracy, with a relatively small design which compares well with designs that are currently used.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

As CMOS technology continues to scale down to attain higher performance and integration, power densities also continue to increase. Figure 1 shows the increasing power densities and corresponding temperature as the CMOS technology scales down.

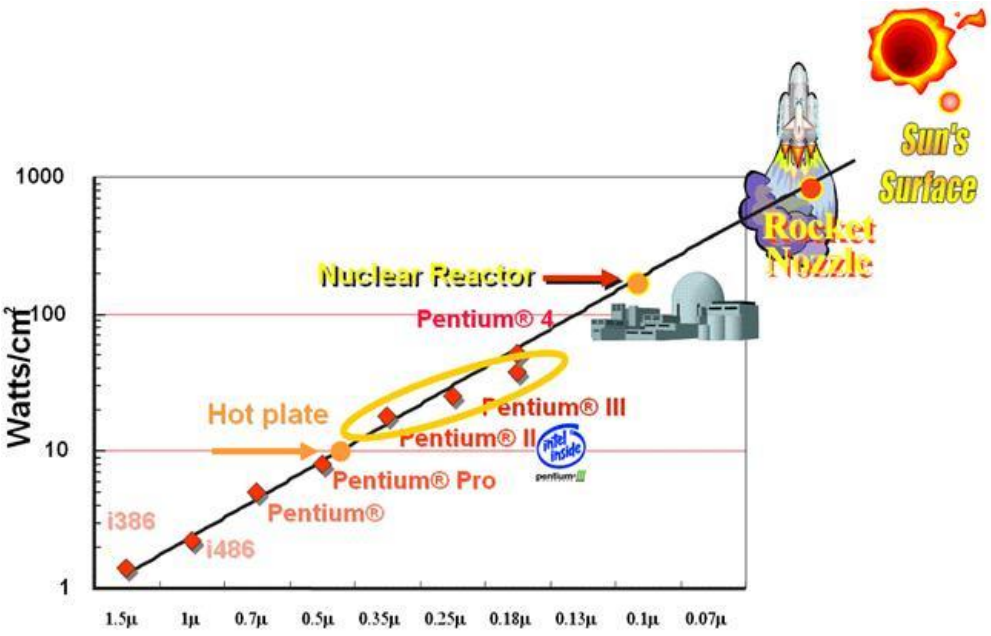


Figure 1: Increasing power densities in various generations of processors [1]

Higher power densities lead to higher temperatures of operation of a chip. Higher temperatures cause the chip to malfunction[2]. Large temperature variation across the chip will decrease the reliability of the circuits as well as degrade its performance. It can not only cause timing errors, but also inflict physical damage to the circuit because of the

phenomenon of electron migration. The recommended junction temperatures of Intel 1.5Ghz Pentium 4 processor and AMD 1.2Ghz Athlon processor are 72 ºC and 95 ºC respectively [3]. It is also reported that 1 ºC decrement in temperature can reduce IC failure by 2-3% [3]. As a result the lifetime of the circuits will be greatly reduced.

Without a proper thermal solution such as an efficient heat sinker or a self-protection mechanism, a chip is easily overheated to function incorrectly or to receive a fatal damage. This emphasizes the need temperature control of a chip.

1.2 Motivation

From a digital design perspective, if a processor is designed for the worst case power dissipation and the worst case ambient temperature, the design needs to maintain a large performance guardband, leading to poor performance. A more preferred approach is to reduce performance guardband that allows a chip to operate at higher performance levels while avoiding chip failures at high temperatures by implementing a thermal sense and respond technique. The response typically involves relaxation of cycle time by throttling clock and lowering frequency. Thermal sensors along with dynamic power management schemes implement temperature regulation [4].

Until recently, thermal sensing was done by off-chip thermometers. However, due to the thermal resistance and capacitance of chip packaging, they suffer from time lag in sensing. This, points to a need for integrated on-die thermal sensors [5]. Integrating thermal sensor provides instant information to enable real time thermal management[5]. There are many off-chip thermal sensors which provide high accuracy in sensing which is not the case with the integrated thermal sensors. Also, on-chip thermal sensors are required to be compact in area and easy to integrate leading to some compromises.

Another problem in today's processors is that the temperature is not evenly distributed across the chip. Units like ALU, register banks have higher temperatures than units like caches that tend to have low temperature[6]. Also the temperatures of the units vary with time and are specific to workload.

Figure 2 shows the distribution of temperature for processor block for SPEC2000 benchmark [6]. Efficient thermal management techniques can be employed if we can sense the temperature of the thermal hotspots on the chip.

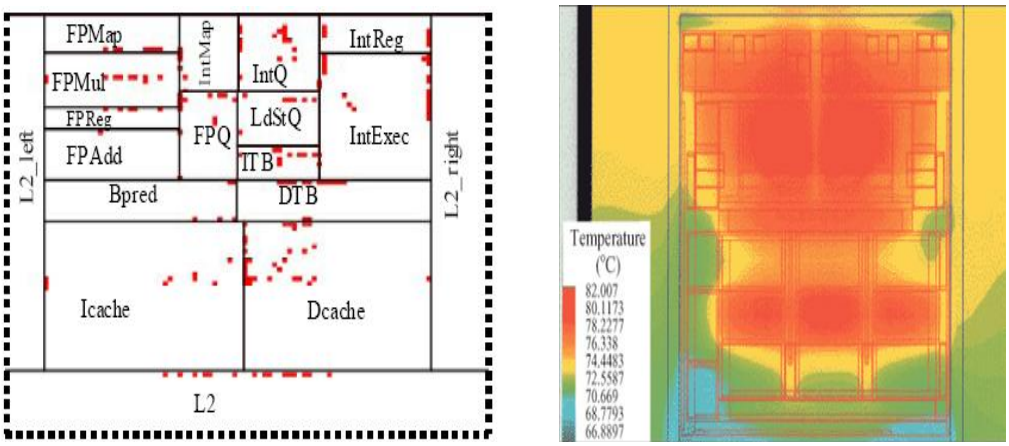


Figure 2: a) Distribution of hotspots for each processor block for SPEC 2000 benchmarks [6]. b) Map of FET junction temperatures for 115W packaged Power4 chip [6].

In most thermal sensors used today, the accuracy of sensing is improved by temperature calibration. Temperature calibration compensates for inaccuracies in temperature measurement and helps improve system accuracy. However, temperature sensor calibration is expensive. First, it imposes an overhead in design cost and silicon area. Secondly, there is a calibration cost as it requires pre heating and testing the sensor to know the offset, drift, slope and uncertainty errors. Once these errors are known the sensing unit is calibrated using A/D converters and look-up tables. Compensating for

dynamic errors require even more complex signal processing. Thus, testing imposes test time overhead that translates to cost, while A/D converters and look-up tables impose area overhead. It is well known that the accuracy of the thermal sensors decrease dramatically without calibration.

Table 1 shows the un-calibrated readings of the thermal assist unit used in IBM25PPC750L processors [7]. The difference between highest and lowest reading shows the sensitivity range of the TAU which is reproduced below for readers' convenience.

Table 1: Un-calibrated Worst case readings of Thermal Assist Unit(TAU) readings for IBM25PPC750L Processors (°C).

Actual temperature	Highest reading	Lowest reading
35	46	13
95	109	61

The cost of calibration can be expensive. Particularly in products featuring more than one thermal sensor [8] can be prohibitive. Consequently, many commodity microprocessors use uncalibrated thermal sensors [9]. Our goal is to devise an architecture which eliminates the need of calibration while providing high accuracy sensing.

In un-calibrated sensors, an effect of process variation on sensing accuracy is of paramount importance. Unfortunately, process variation has become a larger concern with rapidly scaling technology [10]. The basic element of the proposed sensing circuit uses a pair of matched transistors which are highly sensitive to process variation. We have proposed an approach to reduce the effect of process variation between the matched

transistors and increase the accuracy of sensing.

In most of the reported literature, impact of process variation and calibration/test cost has not received adequate attention. In this work, we mainly focus on how to devise an on chip sensor architecture that senses most of the hotspots, occupy little area, provide high accuracy in sensing and reduce the test and calibration cost.

1.3 Approach

To achieve our goal we take the approach shown in the Figure 3. The main aim of this thesis is to device a thermal sensor architecture which can sense all the hot spots of the chip. We have developed an architecture with multiple diodes placed at different parts of the chip, a multiplexor, a comparator and a control logic unit. The problem with this approach was the process variation on the comparator, which reduced the sensing accuracy of the sensor. To reduce the process variation on the comparator we propose self-compensation technique. This technique increases the accuracy of the sensor, but is still not comparable to the accuracy sensor calibration provides. However sensor calibration is costly and consumes lot of area in terms of look up tables. To make the sensor more cost effect and to increase the sensing accuracy of the sensor as that of the sensor calibration we introduce dithering. Dithering in the one of the inputs of the comparator reduces the offset thus increasing the sensing accuracy.

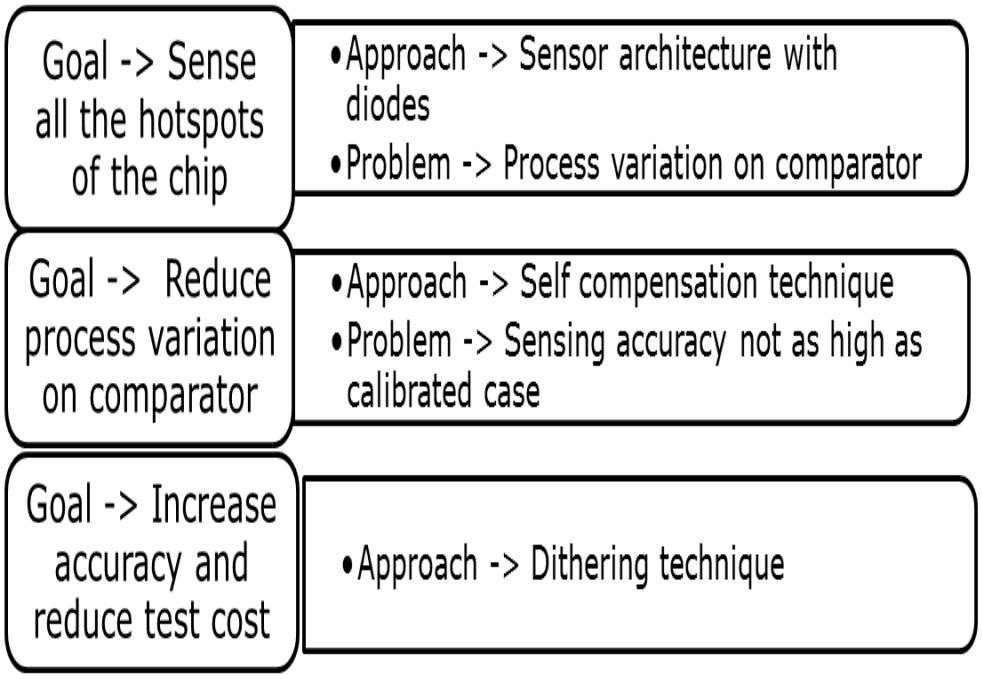


Figure 3: Overview of design approach

The rest of the thesis as organized. In chapter 2 architecture and design of the thermal sensor is discussed. Chapter 3 shows the effect of process variation on the sensing accuracy of the thermal sensor. Compensation circuitry to overcome the limitations posed by process variation is discussed in chapter 4. Chapter 5 introduces dithering and demonstrates how the compensation circuitry and dithering together reduces the effect of process variation and help increase accuracy of the thermal sensor. We conclude this work in chapter 6.

CHAPTER 2

THERMAL SENSORS AND MANAGEMENT

2.1 Introduction

With the aggressive downscaling of technology nodes and constantly-increasing on-chip power consumption, thermal management is becoming a significant design challenge for high-performance microprocessors, integrated network processors, and SoCs. On-chip temperature directly impacts the performance and time to failure of switching devices. Moreover, sub-threshold leakage of CMOS devices depends greatly on the temperature. The failure rate due to electromigration and oxide breakdown is exponentially dependent on temperature. In addition to the rise of the peak on-chip temperature, various system-level power-management techniques and non-uniform power-distribution policies over the substrate surface result in a non-uniform, on-chip thermal profile and creation of hot spots. The temperature inside a chip can vary by 5 ºC ~ 30 ºC from one location to another [11].

Thus the processor or SOC requires a thermal solution to maintain temperatures within operating limits. Operating at temperatures beyond these limits may cause permanent damage to the processor or Soc. Maintaining proper thermal environment is the key to reliable, long-term system operation.

Several thermal management techniques have been proposed [12] [13] [14] [15] [16] which rely greatly on the accuracy of thermal sensors. To capture the

temperature variations across the processor chip we need a large number of inexpensive sensors to optimize and localize thermal management schemes.

2.2 On chip thermal sensors

Many groups have explored a variety of designs for temperature sensors. The temperature sensors can be divided into two groups

1. On-chip thermal sensors
2. Off-chip thermal sensors.

On-chip thermal sensors are preferred over off-chip ones because of their time efficient response, low cost and the fact that they can be designed for low area/power overhead. Many on-chip thermal sensor designs have been proposed in the recent years based either on MOS or bipolar circuits [5]. Sensor size is a critical design concern in embedded thermal sensors. Unfortunately, there appears to be a direct trade-off between sensor accuracy and sensor area.

CMOS sensor for low cost applications with limited measurement range based on time-to-digital converter was proposed by Chen at al [17]. Differential cascade amplifier based sensor working on dynamically biasing the sensor based on output current was proposed by Syal et al [18][19]. Kohari et al [20] developed cascade current mirror based frequency output thermal sensor, which produced currents and voltage independent of supply voltage. Ring oscillator based temperature sensor with very limited accuracy was proposed [21]. For wide range of temperature sensitivity substrate PNP transistor based thermal sensor was proposed [22]. Comparison of these sensors on accuracy, power dissipation and area is given

in [23].

Most of these sensors have large area overhead. Low area overhead differential temperature sensor was proposed by Roy et al in [24]. However, this design suffers from relatively low accuracy. Built-in/on-chip thermal sensors can be classified on the basis of their output type**,** circuit type and process technology**.** Table 2 shows the different on-chip thermal sensors. A detailed comparison of all the on-chip sensors is given in [23].

Table 2: Different on-chip thermal sensors.

Output Type	Circuit Type	Process Technology
1. Current 2. Voltage 3. Frequency 4. Delay 5. Leakage/ decay period	1. Differential cascode amplifier 2. 2-stage Operational Transconductance amplifier 3. 4T SRAM cell based 4. Ring Oscillator based 5. CMOS lateral bipolar transistor sensor 6. CMOS substrate bipolar transistor sensor (integrated with σ-δ converter) 7. Delay cell with time-to-digital converter 8. Diode based – Intel Pentium 4	1. CMOS process - bulk - Silicon-on-Insulator 2. Carbon Nanotube thermal sensors 3. Germanium on Insulator (GOI) process

2.3 Proposed sensor architecture

An emerging critical issue due to technology scaling is the effect of on-die temperature variation. What was previously a second-order effect that could be

adequately addressed with a few corner cases and guardbands has now become a first-order effect. It interacts with a number of these other issues in ways that make analysis difficult. If the temperature distribution across a die is not known, overly pessimistic guard bands must be applied, leading to costly and unnecessary design margins. Also, an analysis based on constant temperature cannot detect the design violations that arise from the non-uniform temperature distribution.

The objective of our sensor architecture is to sense the temperature of different parts of the chip by having small thermal sensors embedded near every unit of the chip. For example the temperature of a microprocessor is not evenly distributed. Units like ALU, multipliers etc tend to be hotter than units like memory. This temperature variation leads to formation of hot spots on the chip. Having a thermal sensor at each of these units would give us the temperature information of each unit individually, which could be used to employ more efficient thermal management techniques. To embed a thermal sensor at each unit of the chip the sensor has to be very small and occupy very little area of the chip. At the same time the sensor has to provide accurate reading of the temperature. In this thesis we have proposed a sensor architecture, which senses the temperature of all the hot spots of the chip, occupy little area and provide high accuracy in sensing.

The overall architecture of the proposed sensor is described. Figure 4 shows the block diagram of the sensor architecture. It comprises of many thermal sensors, a multiplexor, a comparator and a control logic unit.

If sensor size is large, it cannot be placed where the thermal hotspots are as the thermal hotspots on a chip also happen to be some of the densest circuit regions.

Instead of placing the entire sensor near a thermal hotspot, we propose to use a probe. The probe is simply a p-n junction diode connected to resistors. P-n junction diodes occupy little area and have strong temperature dependence.

The temperature dependence of a forward biased p-n junction can be given by the diode equation According to the diode equation

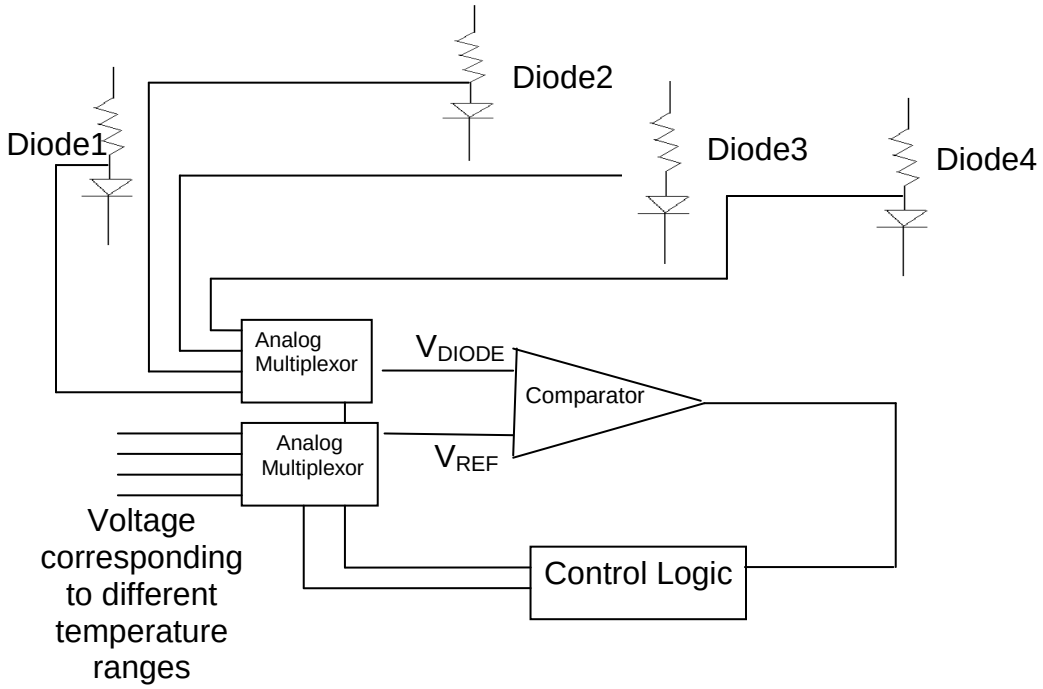


Figure 4: Block diagram of our sensor architecture

$$I_D = I_S\left(e^{\frac{qV}{NkT}} - 1\right)$$

Where I_D is diode current, I_S is saturation current, e is Euler's constant (2.71828...), q is charge of electron (1.6 * 10-19 As), V is voltage across the diode, N is "non-ideality" coefficient (typ. between 1 and 2), K is Boltzmann's constant

(1.38 * 10-23) and T is temperature in Kelvin. If the current through the forward-biased silicon PN junction is held constant, the forward drop decreases about 1.6mV per °C [25]. Thus they are ideal to be placed in a highly dense area of a chip.

The analog multiplexor is used to probe the voltage from multiple points on a chip input through multiple p-n junction diodes. The comparator unit is used to compare the voltages from the p-n junction diodes and the reference voltage that corresponds to some temperature. The comparator unit works as a single-bit A/D converter that tells whether the sense voltage is above or below a threshold.

The voltage Selection of the reference voltage corresponding to specific temperature and selection of sensing module is done by analog multiplexers, which are controlled by control logic. The reference voltage is assumed to be input from an external input. If the reference voltage is generated within the chip there are chances it may not be accurate which may lead to incorrect sensing of the temperature. To have a constant and accurate reference voltage the voltage must be input from an external pin. As the comparator is based on MOS technology, effect of temperature on it is minimal [26].

Thus wide ranges of temperature at different parts of the chip can be sensed by multiplexing.

2.4 Comparator design

In this thermal sensor architecture accuracy and speed of sensing mainly depends on accuracy and speed of the comparator. It is a general practice to use op-amps as

comparators, but using op-amps as comparators often degrade the performance of the comparator [27]. Comparators are designed to work as open-loop systems, to drive logic circuits, and to work at high speed, even when overdriven. Op amps are designed for none of these. They are intended to work as closed-loop systems, to drive simple resistive or reactive loads, and should never be overdriven to saturation [27].

The design of comparator here is based on Differential Cascade Voltage Switch Logic (DCVSL). DCVSL is constructed of differential NMOS/PMOS pair which senses the input difference and cross coupled PMOS/NMOS transistors which act as load. DCVSL has lower power dissipation, occupies lesser area and has lesser delay compared to the traditional CMOS designs [28].

Figure 5 shows the comparator design. The NMOS transistors M1 and M2 are the differential pair which senses the reference voltage V_{REF} and the output voltage V_{DIODE} of the sensing module respectively. The NMOS transistor M3 acts as a constant current source for transistors M1 and M2. The PMOS transistors M6 and M7 drive the output HIGH if SEN signal is low, i.e. when it is not sensing.

When SEN is high transistor M3 is ON and transistors M6 and M7 are OFF. If Vdiode is higher than Vref, slightly more current flows through transistor M2. This causes unequal voltage drop across transistors M4 and M5 and thus the voltage at the drain of transistors M1 and M2 are different. As drains of transistors M2 and M1 drive the gates of transistors M4 and M5, regenerative action takes place pulling transistor M5 to saturation and transistors M4 to triode region and drives the output HIGH. If V_{DIODE} is less than V_{REF}, more current flows through transistor M1 and the

output is driven LOW. When SEN is low transistor M3 is OFF, the sources of transistors M1 and M2 are floating and the output is driven HIGH by transistors M6 and M7.

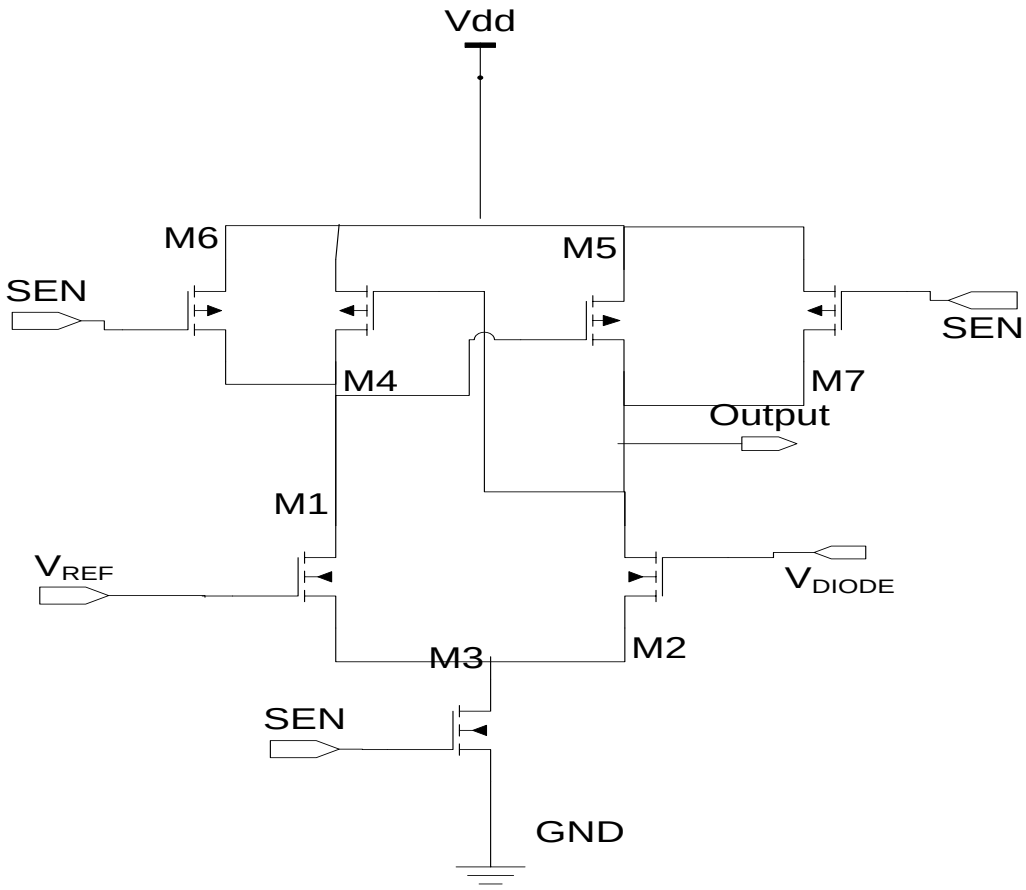


Figure 5: Comparator Circuit (NMOS Differential Pair)

Figure 6 shows the design of a comparator based on PMOS differential pair. The PMOS based design has same number of transistors as the NMOS based design. However the sensing happens at the negative pulse of the sensing signal as we are using the PMOS transistors.

When SEN is high the transistors M1, M2 and M3 are off and the output is pulled high by the transistors M7 and M8. When SEN goes low M2 and M3 are in saturation. The difference in V_{REF} and V_{DIODE} causes unequal voltage drop across transistors M4 and M5. This causes regenerative action which pulls transistor M5 to saturation and transistors M4 to triode region and drives the output HIGH.

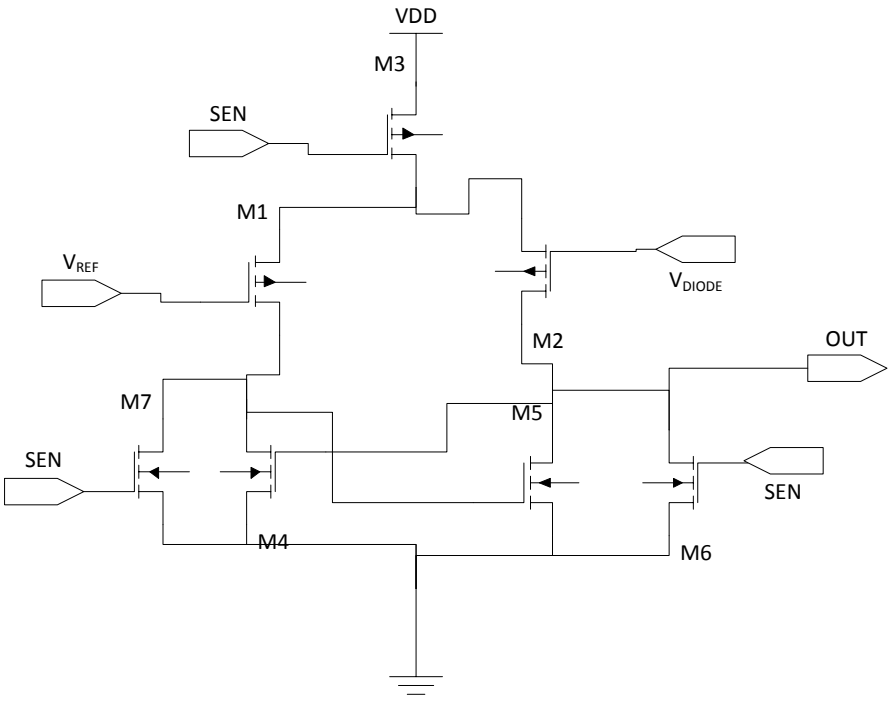


Figure 6: Comparator Circuit (PMOS Differential Pair)

However, conventional bulk CMOS scaling beyond 32nm is severely constrained by short channel effects and vertical gate insulator tunneling [29]. Double-gate FinFET technology [30] has been proposed as a very promising candidate to circumvent the conventional bulk CMOS scaling constraint by changing the device structure in such a way that MOSFET gate length can be scaled further even with thicker oxide, which makes it possible to continue scaling beyond

the limit of the conventional bulk CMOS. Unlike planar single- and double-gate devices, the FinFET effective channel width is perpendicular to the semiconductor plane. Therefore, it is possible to increase the effective channel width and drive current per unit planar area by increasing the fin-height. Interconnect dominated circuits such as memory arrays are likely to get benefited from the increased driving current. Therefore, it is essential to develop a comparator design technique for the new device such as FinFET.

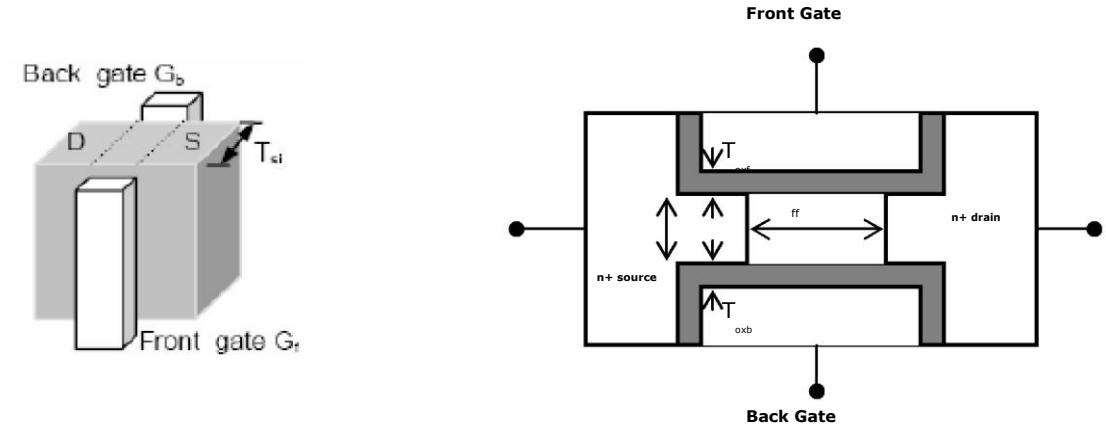


Figure 7: FinFET Structure and Symbol

Figure 7 shows the structure of multi-fin double-gate FinFET device. Current flow is parallel with the wafer plane. The thickness t_{si} of the single fin equals to the silicon channel thickness. Each fin provides the width of the device, and H is the height of the each fin. FinFET circuit behavior is studied using PTM (Predictive Technology Model) of the 32 nm CMOS FinFET technologies [31].

Figure 8 shows the comparator design based on FINFET Technology. The operation of the comparator is same as the comparator with NMOS differential pair. FINFETs F1 and F2 are the differential pair which senses the reference voltage

VREF and the output voltage VDIODE of the sensing module respectively. The FINFET F3 acts as a constant current source for the FINFETs F1 and F2. The p-FINFETs F6 and F7 drive the output HIGH if SEN signal is low, i.e. when it is not sensing.

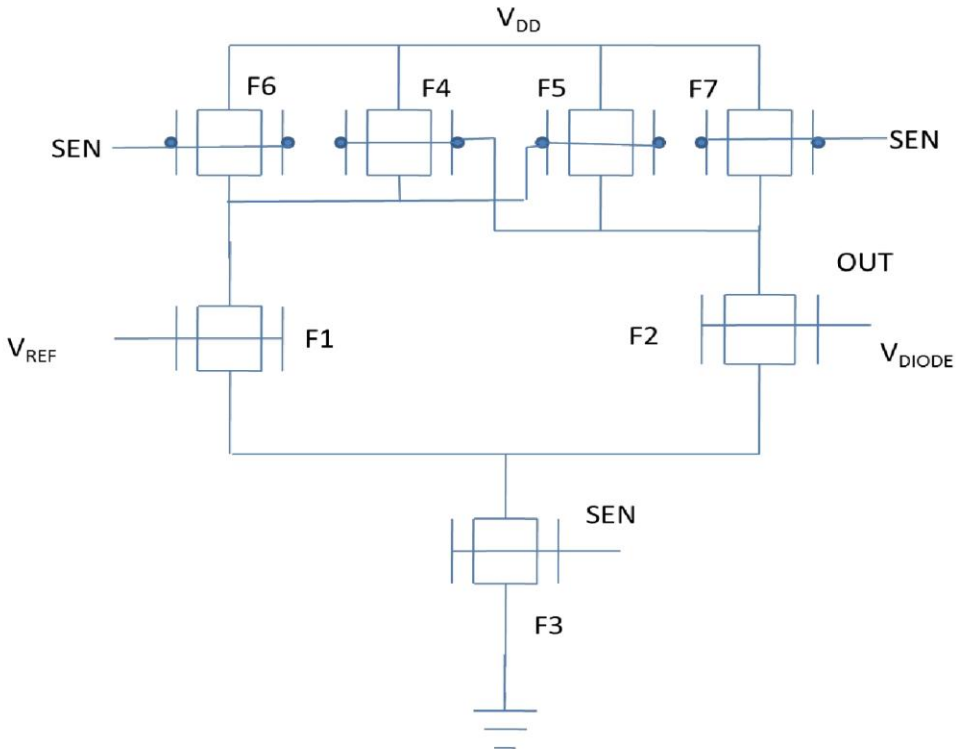


Figure 8: Comparator Circuit with FINFET Technology

When SEN is high FinFET F3 is, if V_{DIODE} is higher than VREF, slightly more current flows through F2. This causes unequal voltage drop across F4 and F5 and regenerative action takes place pulling F5 to saturation and F4 to triode region and drives the output HIGH. If V_{DIODE} is less than V_{REF}, more current flows through

FinFET F1 and the output is driven LOW. When SEN is low transistor M3 is OFF, the sources of the output is driven HIGH by FinFETs F6 and F7.

Figure 9 shows the waveforms and operation of the comparator. Output swing of the comparator is increased by connecting an inverter at the output of the comparator. The circuit simulation result based on HSPICE [32] using 32nm PTM [33] models.

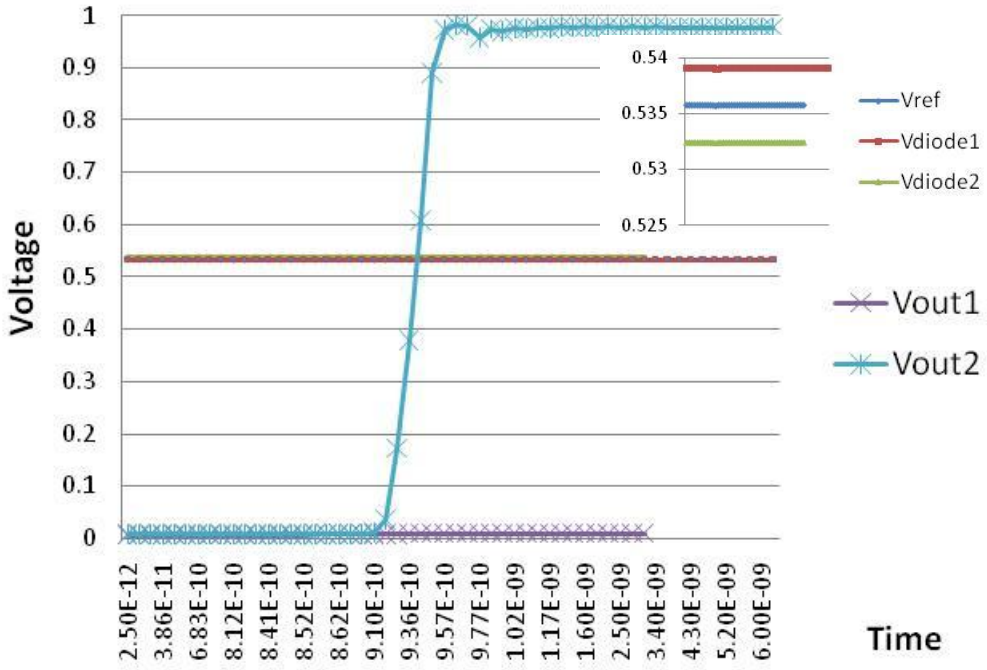


Figure 9: Waveforms showing operation of Comparator

CHAPTER 3

PROCESS VARIATION

3.1 Introduction

Moore's-Law-driven technology scaling has improved the performance of VLSI tremendously in the last four decades. As advanced technologies continue the pursuit of Moore's Law, a variety of challenges will need to be overcome. One of these challenges is management of process variation [34][35].

Although there has been a trend in the CMOS literature in recent years to convey process variation as a new challenge associated with advanced CMOS technologies, that viewpoint does not effectively capture the history of process variation. Process variation has always been a critical aspect of semiconductor fabrication.

The first discussion of random variation in semiconductor devices was Shockley's 1961 analysis of random fluctuations in junction breakdown [36]. Keyes [37] in 1975 extended Shockley's concepts of random variation were extended to MOS devices, when he modeled the effect of random fluctuations in the number of impurity atoms in the depletion layer of a field-effect transistor (FET). Schemmert and Zimmer [38] computed the sensitivity of ion-implanted MOS threshold voltages as a function of the implantation energy and the oxide thickness and were first to address systematic variation.. A more extensive analysis of threshold voltage

sensitivity using a closed-forum numerical simulation was presented by Yokoyama et al. in 1980 [39] with a Monte Carlo approach developed by Alvarez in the same year [40]. Interconnect variation has also received significant attention over the years, with Lin et al. presenting a detailed treatment in 1998 [41]. While the continued decrease in the ratio of feature sizes to fundamental dimensions (such as atomic dimensions and light wavelengths) means that management of variation will play a significant role in future technology scaling, the evidence shows that process variation has been a continuing theme throughout semiconductor history.

Process variations occur due to various reasons. Examples include highly random effects (random dopant fluctuation (RDF), line-edge and line-width roughness, line-edge and line-width roughness (LER) and (LWR), respectively, variations in the gate dielectric (oxide thickness variations, fixed charge, and defects and traps), patterning proximity effects (classical, and those associated with OPC), variation associated with polish (shallow trench isolation (STI), gate, and interconnect), and variation associated with implants and anneals (tool-based, pocket implants, rapid-thermal anneal RTA and variation associated with poly grains). All these variations lead to performance degradation and random error in the operation. The process variation can also cause the delays of wires and gates within a chip to vary. As a result, some chip may also operate correctly at slower speeds.

Process variations can either systematic or random variations.

1. *Systematic variation*: Systematic variations are deterministic in nature and are caused by the structure of a particular gate and its topological environment.

The systematic variations are the component of variation that can be attributed to a layout or manufacturing equipment related effects. They generally show spatial correlation behavior.

2. *Random variation*: Random or non-systematic variations are unpredictable in nature and include random variations in the device length, discrete doping fluctuations and oxide thickness variations. Random variations cannot be attributed to a specific repeatable governing principle. The radius of this variation is comparable to the sizes of individual devices, so each device can vary independently.

Process variations can also be classified into two types

1. *Inter-die*: Inter-chip variations are variations that occur from one die to next, meaning that the same device on a chip has different features among different die of one wafer, from wafer to wafer and from wafer lot to wafer lot. Die-to-die variations have a variation radius larger than the die size including within wafer, wafer to wafer, lot to lot and fab to fab variations. Inter die variations are typically accounted for in circuit design as a shift in the mean of some parameter values (e.g. VT or wire width) equally across all devices or structures on any one chip. For purposes of circuit design it is usually assumed that each contribution or component in the inter die variation is due to different physical and independent sources.

2. *Intra-die*: Intra-die variations are the variations in device features that are

present within a single chip, meaning that a device feature varies between different locations on the same die. Intra-chip variations exhibit spatial correlations and structural correlations. Intra die variation is random and occurs due to the semiconductor manufacturing process.

3.2 Impact of process variation on sensor architecture

Our proposed sensor architecture is affected by both inter and intra die process variation. The inter die or local variations can be mapped to the variations in length, width and oxide thickness of the transistors on the same die. These variations have the most impact on the comparator which acts as a 1 bit A/D converter. The process variation in diodes can be reduced by increasing the doping concentrations of the p-n junction diodes. The increase in doping concentration will be a compromise with the area of the chip.

The impact of process variation on comparator is of paramount importance because in this thermal sensor architecture accuracy and speed of sensing mainly depends on accuracy and speed of the comparator. Process variation on comparator may lead to incorrect and erroneous sensing of temperature.

Operation of the comparator is based mainly on the difference in current flowing through the transistors M1 and M2, to which the voltages V_{REF} and V_{DIODE} are fed. The current through drains of transistors M1 and M2 is determined by the overdrive voltage of the transistors, which is given by

$$I_D = K' * (V_{GS} - V_T)^2$$

$$K' = \mu_n * C_{ox} * \left(W/L\right)$$

When both the transistors M1 and M2 have identical dimensions (i.e length and Width) and threshold voltages, their drain currents only depends on the gate-source voltage V_{GS}.

$$I_{DM1} = K' * (V_{GSM1} - V_{TM1})^2$$

$$I_{DM2} = K' * (V_{GSM2} - V_{TM2})^2$$

Since both the transistors have identical source voltage, the drain current depends on the gate input voltage only.

$$I_{DM1} = K' * (V_S - V_{REF} - V_{TM1})^2$$

$$I_{DM2} = K' * (V_S - V_{DIODE} - V_{TM2})^2$$

Due to process variation, threshold voltage V_T of the transistors M1 and M2 may differ which result in variation of the current through transistors M1 and M2. Even when the inputs are at same voltage (i.e the voltages V_{REF} and V_{DIODE}) are same the currents through the transistors are not same. This leads to incorrect sensing of the temperature. Thus there is certain voltage difference between the inputs called the input offset voltage for which the currents through the transistors are same and the comparator operates properly.

The input offset voltage of the comparator plays a major role in determining the accuracy of the comparator. The offset voltage may result from transistor

dimension mismatch as well. However, it can be mapped as a function of threshold voltage of the transistors.

$$V_{os} = f(V_T)$$

Where V_{OS} is the comparator offset voltage and V_T is the threshold voltage.

As described earlier, process variation causes the input offset voltage to be higher leading to incorrect sensing of temperature. Moreover diode voltage changes only -1.6mV/ ºC [25], so input offset increase of 5mV can lead to 3 ºC of incorrect sensing which is shown experimentally.

3.3 Experimental setup

The comparator is said to be perfectly balanced transistor parameters on the left-hand side are equal to parameters on the right-hand side. For process variation analysis we consider only the variation threshold voltage of the transistors as the channel length and width variation manifest as threshold variations in circuit design perspective. Our analysis assumes that a particular V_T of the device is varied randomly.

Simulations are carried out for 32nm using CMOS technology, using Predictive Technology Model [33] and considering nominal values of NMOS and PMOS transistor threshold voltages at 0.3288V (V_{Tn}) and -0.250V (V_{Tp}) respectively. The incorrect sensing of the temperature is shown in Figure 10.

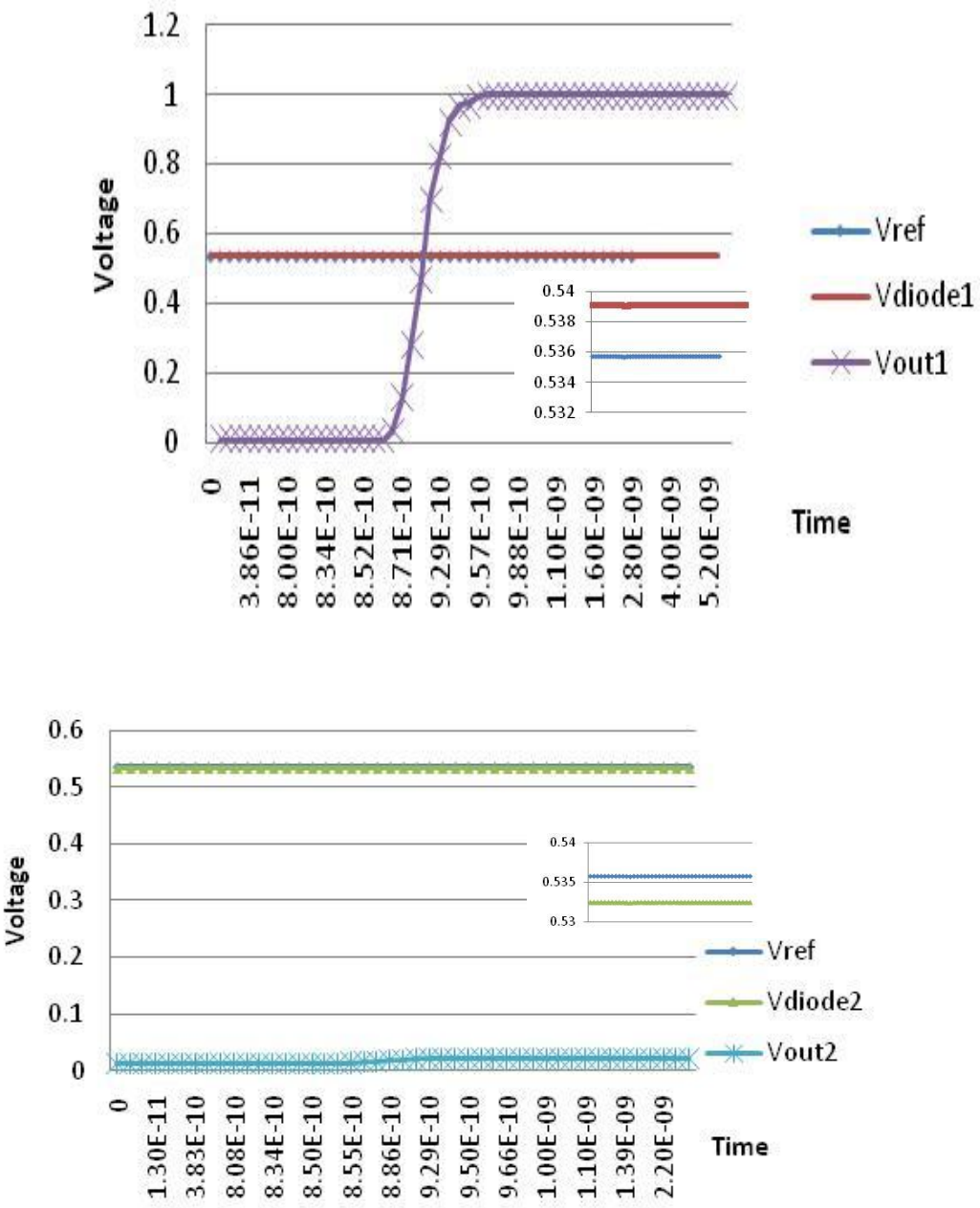


Figure 10: Waveforms showing incorrect sensing due to process variation (a) when VREF < VDIODE (The output switched even when VREF < VDIODE) (b) when VREF >VDIODE (The output switched even when VREF > VDIODE)

3.4 Results

We performed Monte Carlo simulations for analyzing sensing accuracy of comparator circuits while varying threshold voltage V_T of all the transistors. Ten thousand comparators were taken as input sample and their operation is observed for 15 ºC above and below the target temperature of 85 ºC. Figure 11 shows the histogram for the number of comparators switching at various temperature points. All the measurements are made on the basis that output voltage of comparator should be switch at 85 ºC.

From the histogram it is seen that the number of comparators Vs temperature follows a Gaussian distribution with mean at 85 ºC. However the 3σ point is different for each comparator. The FINFET technology based comparator has the lowest 3σ point at 9 degrees. The NMOS and PMOS differential pair based comparators have their 3σ point at 10 degrees. This shows that the sensor has less than 9 degrees accuracy in presence of process variation with respect to 3σ variation. All the circuit simulation results are based on HSPICE [32] using 32nm PTM [33] models.

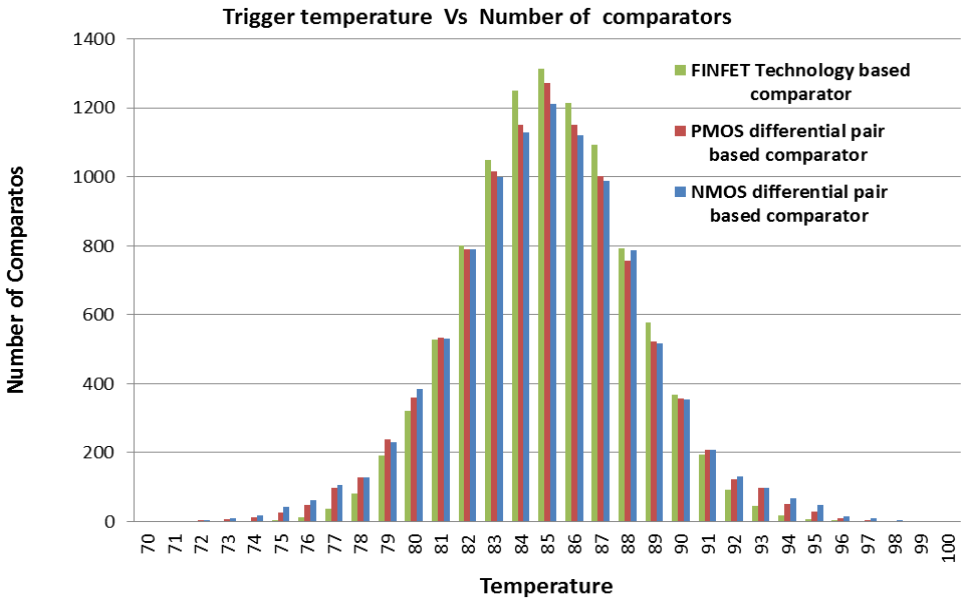


Figure 11: Histogram of trigger temperature for comparator without compensation

CHAPTER 4

SELF COMPENSATING COMPARATOR

As described earlier, the differential part of the comparator is most sensitive to process variation. In order to make the comparator resilient to process variation, the differential part of comparator has to made process variation tolerant. To achieve this we added a compensation circuitry for the crucial transistors M1 and M2. We have also seen in the previous section that current changes in transistors M1 and M2 lead to incorrect sensing of the comparator. The idea of compensation circuitry is to map the current flowing through the transistors to voltage across capacitors, and use this voltage to reduce the current through the other transistor by body biasing or back gate biasing.

4.1 Self compensation through Body Biasing

Figure 12 shows a cross-section of a long channel NMOS with source, drain and bulk terminals grounded. As the gate voltage is increased from 0V, depletion region is created below the gate. As the gate voltage is increased further, a condition of strong inversion is reached wherein the silicon surface inverts from p-type material to n-type. This phenomenon of strong inversion occurs at a critical value of gate-source voltage, which is termed as the threshold voltage, V_T [44].

The threshold voltage is a function of three voltage components: - the difference in work function between gate and substrate (ϕ_{MS}), the fixed oxide charge present at the Si − SiO2 interface ($-Q_{OX}/C_{OX}$) and the gate voltage required

to bring the surface potential to the strong inversion condition ($2\phi_F$) and to offset the induced depletion region charge ($-Q_B/C_{OX}$). ϕ_F is called Fermi potential.

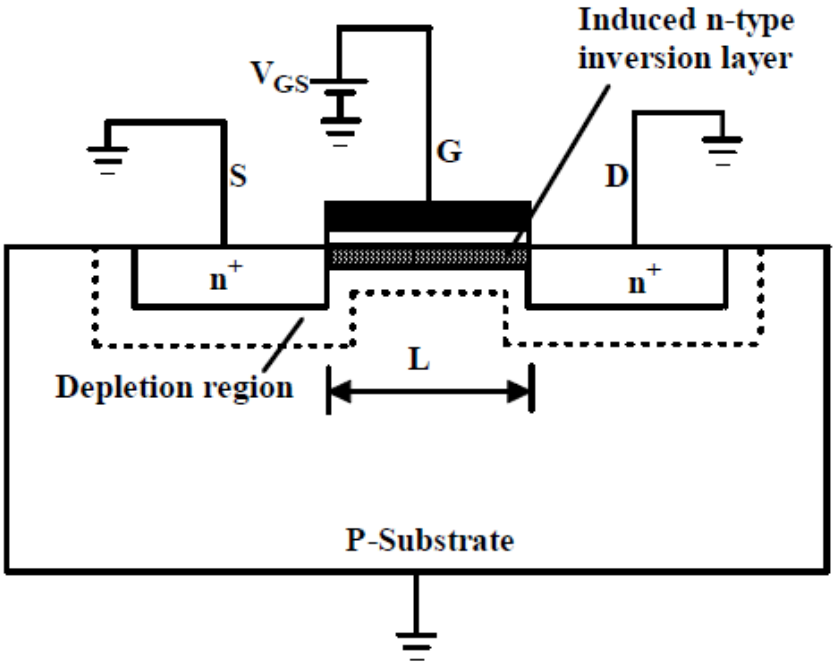


Figure 12: Cross- section of a long channel NMOS with source, drain and bulk terminals grounded

Putting the above three components together, the threshold voltage under no body bias condition can be given by [44].

$$V_T = V_{T0} = \phi_{MS} - \frac{Q_{OX}}{C_{OX}} + 2\phi_F - \frac{Q_B}{C_{OX}}$$

With no body bias (V_{SB} = 0V), the charge stored in depletion region under the strong inversion condition can be expressed as

$$Q_B = Q_{B0} = -\sqrt{2qN_A\varepsilon_{si}|2\phi_F|}$$

Where q is the electron charge, N_A is doping concentration and ε_{si} is the permittivity of silicon. A body effect coefficient γ is defined as

$$\gamma = \sqrt{2qN_A\varepsilon_{si}} \Big/ C_{OX}$$

Thus equation 3.1 can be simplified using equation 3.2 as

$$V_{T0} = \phi_{MS} - \frac{Q_{OX}}{C_{OX}} + 2\phi_F + \gamma\sqrt{2\phi_F}$$

Under body biasing condition (V_{SB}=0V), the surface potential required for strong inversion increases from $|2\phi_F|$ to $|2\phi_F + V_{SB}|$ and the charge stored in the depletion region is given by [44]

$$Q_B = -\sqrt{2qN_A\varepsilon_{si}|2\phi_F + V_{SB}|}$$

The threshold voltage under different body biasing conditions can then be written as follows

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{2\phi_F}\right)$$

For V_{SB}<0 threshold voltage V_T increases which increases the current through transistor and V_{SB}>0 vice versa happens.

4.1.1 Operation of Self Compensating Comparator

The self compensating comparator based on body biasing is shown in the Figure 13. The body of transistors M1 and M2 is connected to the compensation circuitry, which includes capacitance C1 and C2 for storing the source-bulk voltage for M2 and M1 respectively. Transistors M3 and M4 act as training transistors, that map the current in M1 and M2 to voltage on C1 and C2. Transistors M5 and M6 pull body of M1 and M2 to ground while transistors M7 and M8 pull the body to voltage on C2 and C1 during different phases of operation. The transistors M14 and M15 act as switches for SEN signal.

The operation of self compensating comparator is divided into two phases, namely training phase and sensing phase.

Training phase: During training phase FET_TRAIN is high and transistors M3, M4, M5, M6, M19 and M16 are ON. Capacitors C1 and C2 are charged through transistors M3 and M4 and body of transistors M1 and M2 is pulled to ground by transistors M14, M15 and M19. Same voltage V_{DD} is given to the gates of both transistors M1 and M2 through transistors M16 and M19. Let us assume that due to process variation transistor M1 conducts more current than transistor M2. Since capacitor C1 is charged through transistor M1 and capacitor C2 is charged through transistor M2, capacitor C1 will develop more voltage than capacitor C2.

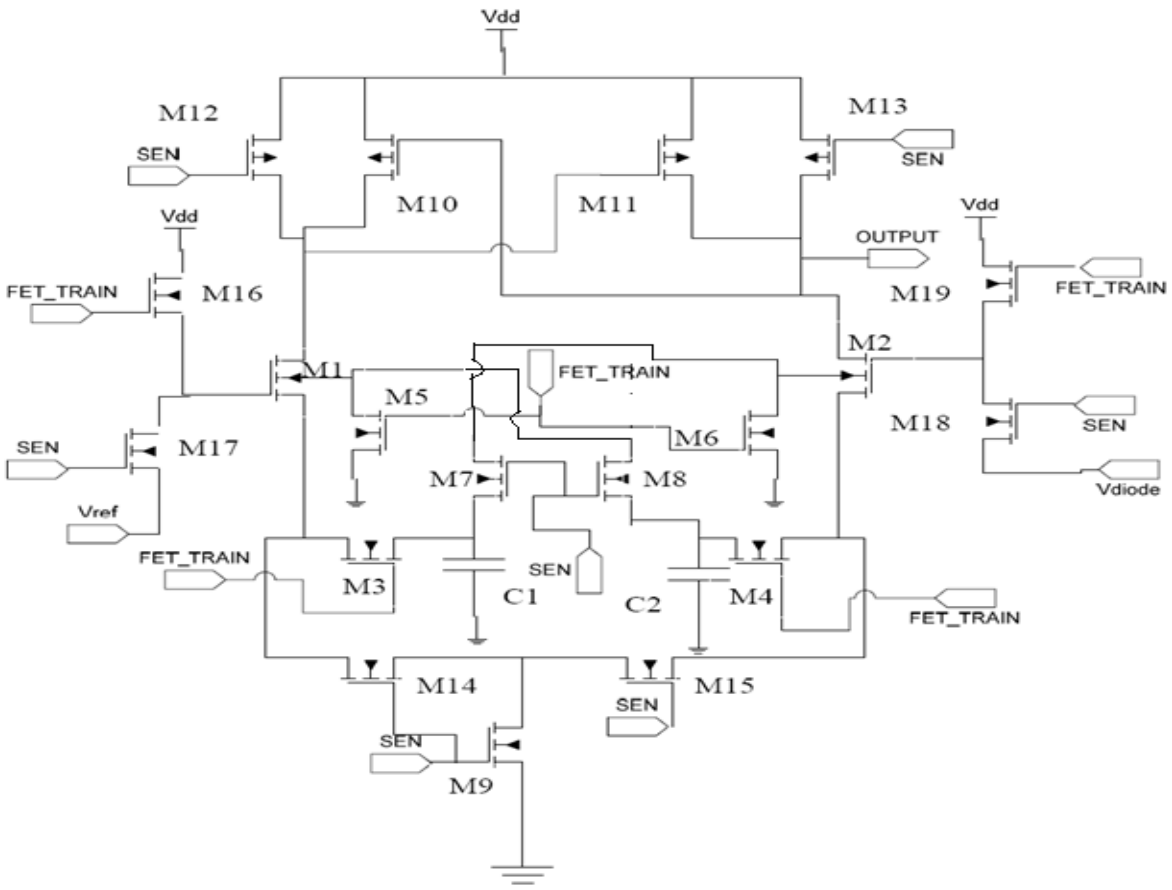


Figure 13: Self Compensating Comparator based on Body Bias (NMOS differential pair)

Sensing Phase: During the sensing phase SEN is high and body of transistors M1 and M2 is connected to capacitors C2 and C1 respectively as transistors M7 and M8 are ON. As voltage on capacitor C1 is higher than capacitor C2, due to body biasing the threshold voltage VT of transistor M2 will decrease and threshold voltage VT of transistor M1 will increase. Thus VT mismatch between the two critical transistors is reduced. The value of capacitors C1 and C2 and the pulse width of FET_TRAIN pulse is chosen such that charge on them do not leak away before the SEN signal is

applied. It is to be noted that before every FET_TRAIN pulse voltages C1 and C2 have to be completely discharged.

The self-compensation circuitry can also be applied to the comparator built on the PMOS differential pair.

Figure 14 shows the circuit diagram of the comparator build on PMOS differential pair.

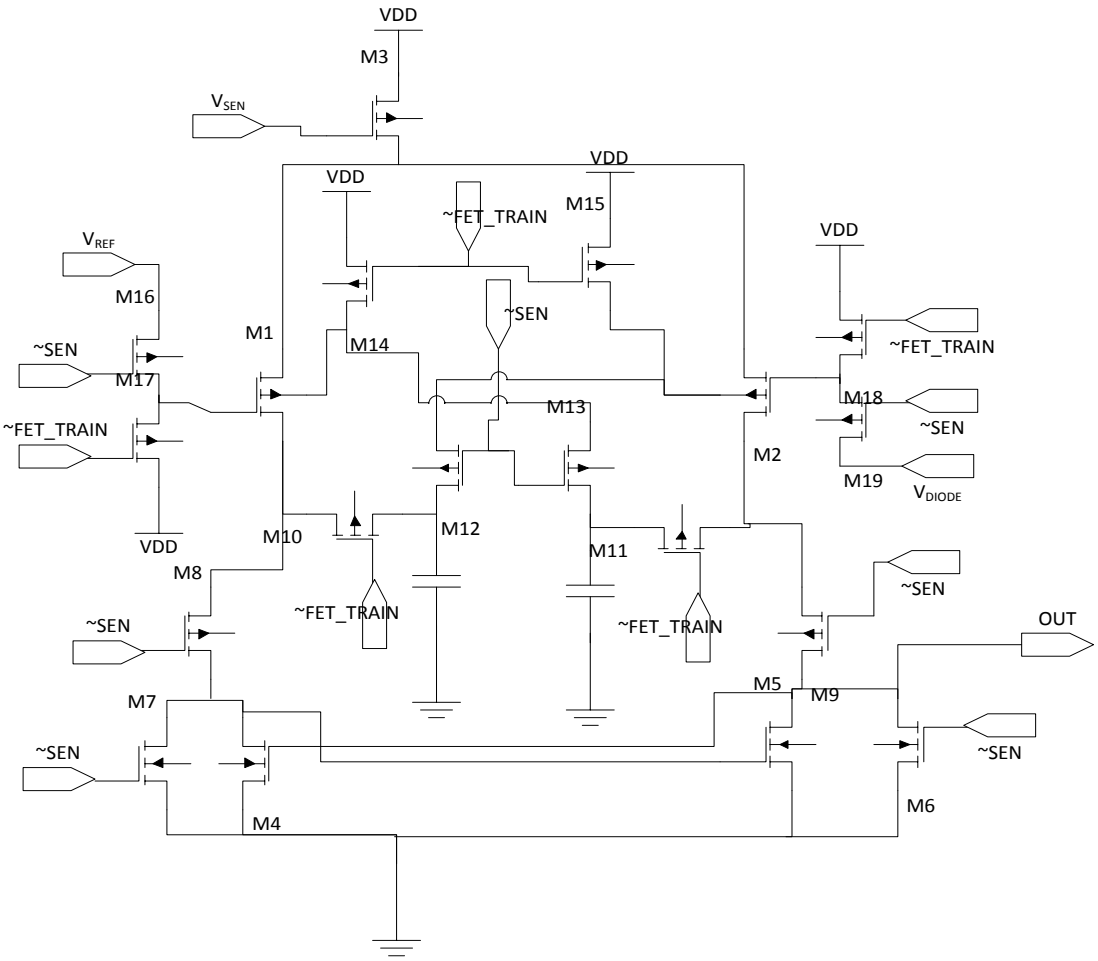


Figure 14: Self Compensating Comparator based on Body Bias (PMOS differential pair)

The operation of the comparator is similar to the compared based on NMOS differential pair. However the sensing and training of capacitors happens at the negative edge of SEN and FET_TRAIN signals.

The timing scheme of self-compensating comparator is shown in Figure 15. Figure 16 shows that during training phase the capacitors are charged to different values due to the process variation on the transistors.

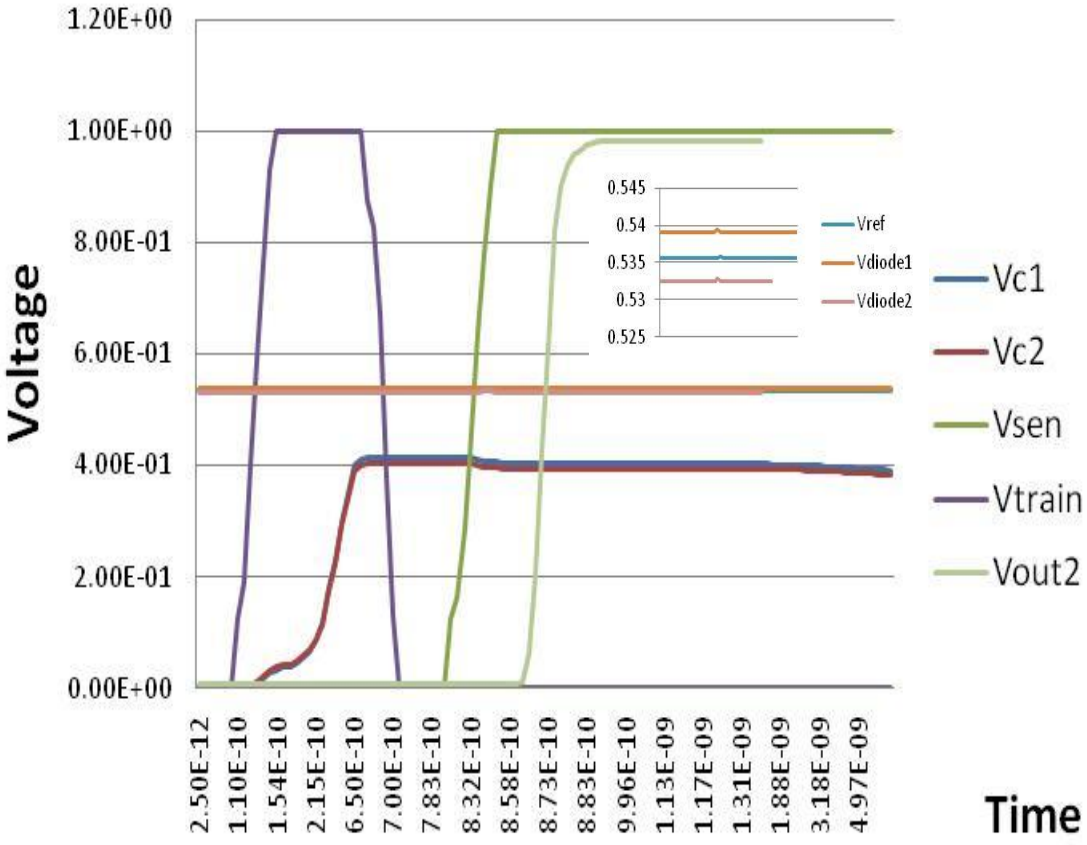


Figure 15: Waveforms showing working of self-compensating comparator

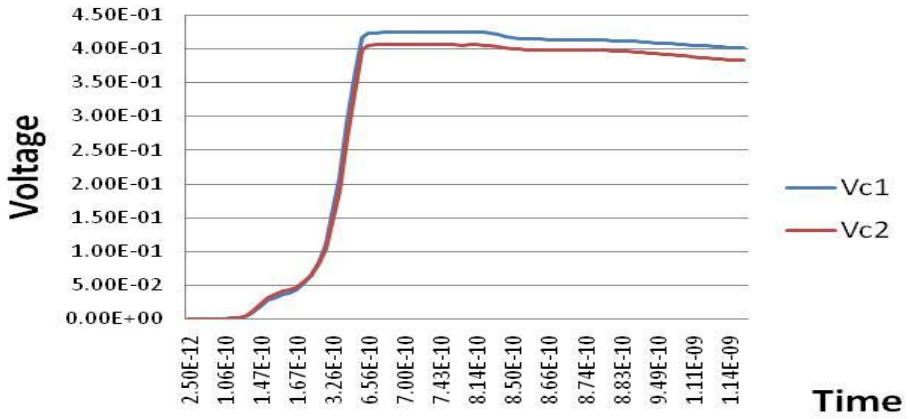


Figure 16: Waveforms showing voltage on capacitors C1 and C2

4.2 Self Compensation through Back gate Biasing

The self-compensation circuitry can also be built by connecting two transistors called back-gates in parallel to the two critical NMOS transistors.

We know that current in a transistor when in saturation is given by

$$I_D = K' * (V_{GS} - V_T)^2$$

$$K' = \mu_n * C_{ox} * \left(W/L\right)$$

When we have two transistors parallel to each other the current is the sum of I1 and I2.

Thus the total current becomes $I_{DM1} = I_{D1} + I_{D1'}$ and $I_{DM2} = I_{D2} + I_{D2'}$

$$I_{D_1} = K' * (V_{GS_1} - V_{T_1})^2$$
$$I_{D_{1'}} = K' * (V_{GS_{1'}} - V_{T_{1'}})^2$$
$$I_{D_2} = K' * (V_{GS_2} - V_{T_2})^2$$
$$I_{D_{2'}} = K' * (V_{GS_{2'}} - V_{T_{2'}})^2$$

Mismatch of V_{T1} and V_{T2} due to process variation leads to mismatch of I_{D1} and I_{D2}. Suppose $I_{D1} > I_{D2}$, to have $I_{DM1} = I_{DM2}$ we have decrease $I_{D1'}$ and increase $I_{D2'}$. This is done by decreasing $V_{GS1'}$ and increasing $V_{GS2'}$

4.2.1 Operation of Self Compensating Comparator

The self-compensating comparator based on back gate biasing is shown in the Figure 17. Additional transistors M1' and M2' are added in parallel to transistors M1 and M2 respectively. Transistors M3 and M4 act as training transistors, that map the current in transistor pair of M1 and M2 to voltage on C1 and C2. Transistors M5 and M6 gate voltage of M1' and M2' to ground while transistors M7 and M8 pull the gate voltage to voltage on C2 and C1 during different phases of operation. The transistors M14 and M15 act as switches for SEN signal.

The operation of self compensating comparator is divided into two phases, namely training phase and sensing phase.

Training phase: During training phase FET_TRAIN is high and transistors M3, M4, M5, M6, M19 and M16 are ON. Capacitors C1 and C2 are charged through transistors M3 and M4 and the gate voltage of transistors M1' and M2' is pulled to ground by transistors M14, M15 and M19. Same voltage V_{DD} is given to the gates

of both transistors M1 and M2 through transistors M16 and M19. Let us assume that due to process variation transistor M1 conducts more current than transistor M2. Since capacitor C1 is charged through transistor M1 and capacitor C2 is charged through transistor M2, capacitor C2 will develop more voltage than capacitor C1.

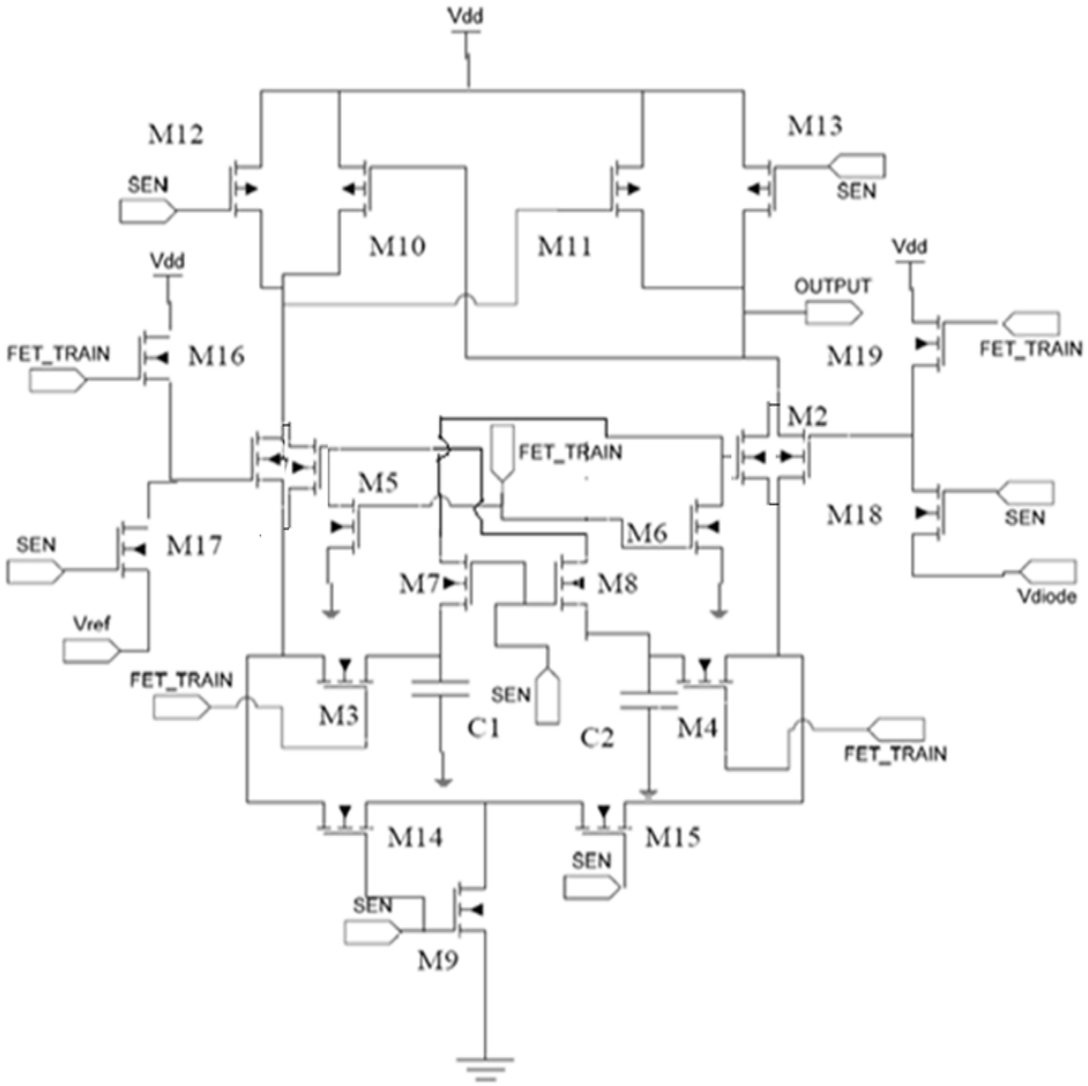


Figure 17: Self Compensating Comparator based on Back gate Bias (NMOS Differential pair)

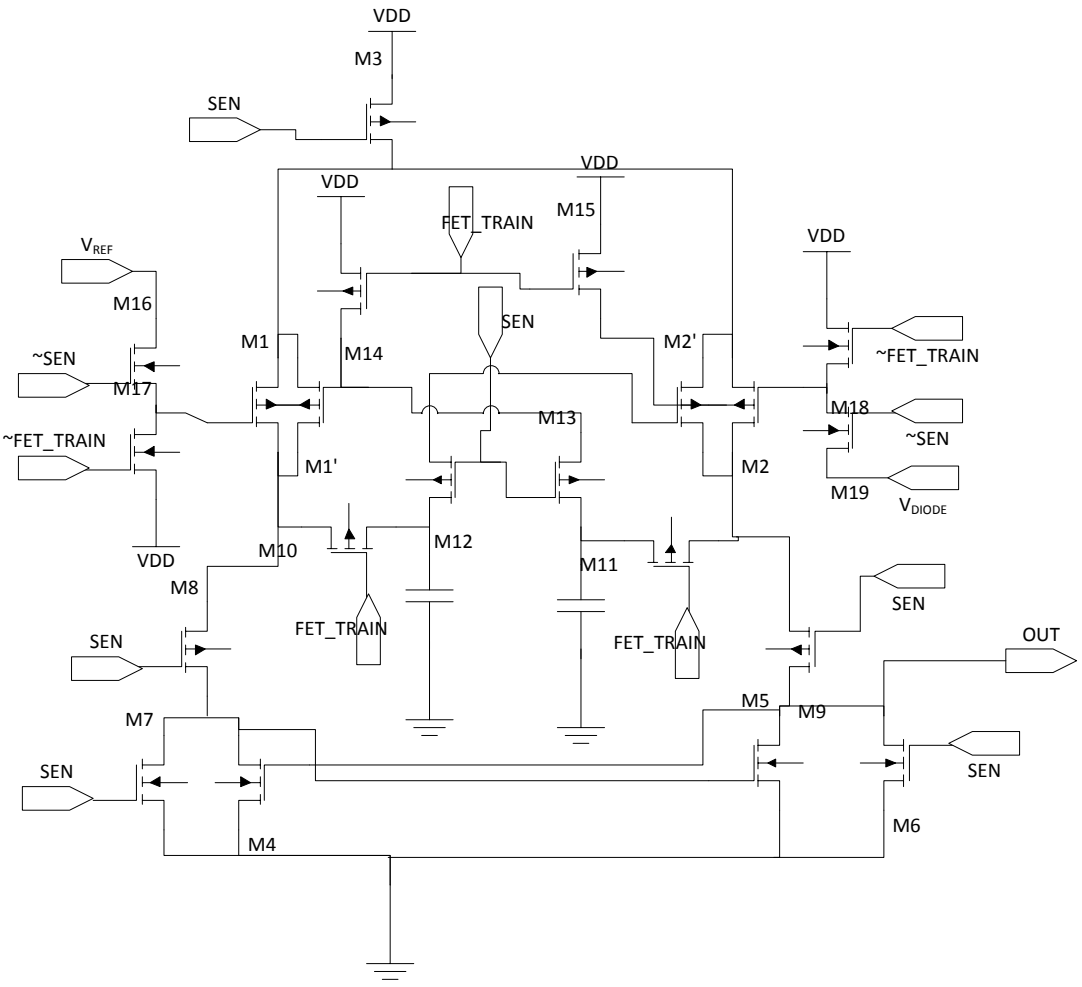


Figure 18: Self Compensating Comparator based on Back gate Bias (PMOS Differential pair)

Sensing Phase: During the sensing phase SEN is high and the gate of transistors M1' and M2' is connected to capacitors C2 and C1 respectively as transistors M7 and M8 are ON. As voltage on capacitor C1 is higher than capacitor C2, the gate voltage of transistor M2' will greater than that of the transistor M1'. Thus V_T mismatch between the two critical transistors M1 and M2 can be offset by pumping more current through M2' and less current through M1'. The value of capacitors C1 and C2 and the pulse width of FET_TRAIN pulse is chosen such that charge on

them do not leak away before the SEN signal is applied. It is to be noted that before every FET_TRAIN pulse voltages C1 and C2 have to be completely discharged.

The PMOS based design in shown in Figure 18. The timing scheme of self-compensating comparator based on back gate biasing is same as the timing scheme self-compensating comparator based on body biasing as shown in the Figure 15 and Figure 16.

4.3 Self compensation through FINFET technology

Though process invariant, the compensation circuit in bulk CMOS at 32nm will have other effects like, short Channel Effects, DIBL, GIDL, Punch Through and V_T Roll off which will affect the sensing accuracy of the sensor. To overcome these effects and improve the performances we can readily apply the back gate biasing technique to double gate FINFETS. The FINFET is by far the option being investigated most widely [45]. It resolves many of the concerns mentioned previously. In fact, it improves some of the scaling problems so well, that practically industry has started looking at implementing it even while there is still considerable lifetime in the conventional MOSFET.

One unique property of the FinFET is the electrical coupling between the front and back gates. The implication of this coupling is that the threshold voltage of the front gate (V_{thf}) is not only governed by the process, but also it can be controlled by the back gate voltage (V_{Gb}). This is similar to the body effect in the bulk transistor.

An independent-gate FinFET operates in the dual-gate mode (DGM) when both gates are biased to induce channel inversion. Alternatively, an independent-gate n-FinFET (p-FinFET) operates in the single-gate mode when one of the gates is deactivated by connecting the gate to ground (V_{DD}). Disabling one of the gates in the single-gate mode (SGM) increases the absolute value of the threshold voltage compared to the DGM. Therefore, it is possible to modulate the threshold voltage of FinFET by biasing the two gates independently [46].

4.3.1 Operation of Self Compensating Comparator

The self-compensating comparator based on FINFET technology is shown in the Figure 19. The back gate of FinFETs F1 and F2 is connected to the compensation circuitry, which includes capacitance C1 and C2. The capacitors are used for storing the voltage for back gate of F2 and F1 respectively. FinFETs F3 and F4 act as training FinFETs, that map the current in F1 and F2 to voltage on C1 and C2.

The operation of self-compensating comparator is divided into two phases, namely training phase and sensing phase.

Training phase: During training phase FET_TRAIN is high and capacitors C1 and C2 are charged through FinFETs F3 and F4. The front and back gates of FinFETs F1 and F2 are tied together and connected to VDD. Let us assume that due to process variation, FinFET F1 conducts more current than F2. Since capacitor C1 is charged through FinFET F1 and capacitor C2 is charged through FinFET F2, capacitor C2 will develop more voltage than capacitor C1.

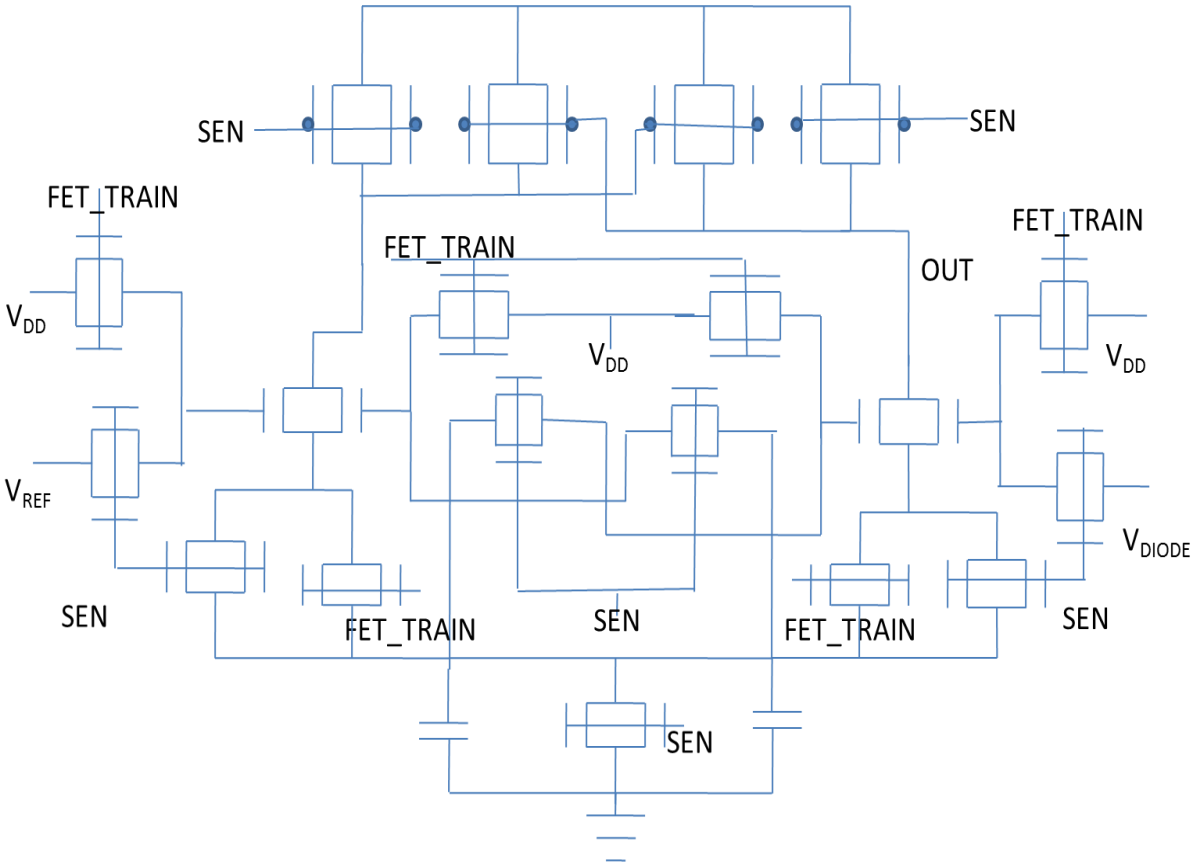


Figure 19: Self Compensating Comparator based on based on FINFET Technology

Sensing Phase: During the sensing phase SEN is high and the back gate of FinFETS F1 and F2 is connected to capacitors C2 and C1 respectively. As the voltage on capacitor C1 is higher than the voltage on capacitor C2, back gate voltage of FinFET F2 will be greater than that of the FinFET F1. Thus V_T mismatch between the two critical FinFETS F1 and F2 is offset. The value of capacitors C1 and C2 and the pulse width of FET_TRAIN pulse is chosen such that charge on them do not leak away before the SEN signal is applied. It is to be noted that before every FET_TRAIN pulse voltages C1 and C2 have to be completely discharged.

The timing scheme of self-compensating comparator based on FinFET technology is same as the timing scheme self-compensating comparator based on body biasing as shown in the Figure 15 and Figure 16.

4.4 Impact of process variation on self-compensating comparator

The accuracy of thermal sensor is determined by its ability is sense in presence of process variation.

4.4.1 Experimental Setup

The effect of process variation on self-compensated comparator is studied from Monte Carlo Simulations through HSPICE [32] where all the transistors are subjected to process variation. As the transistors M1 and M2 are the differential part of the circuit, they are most sensitive to process variation, and hence the compensation for M1 and M2 yields most benefit.

As in the study of process variation on comparator without compensation circuitry, ten thousand comparators were taken as input sample and their operation was observed for 15 ºC above and below the original temperature.

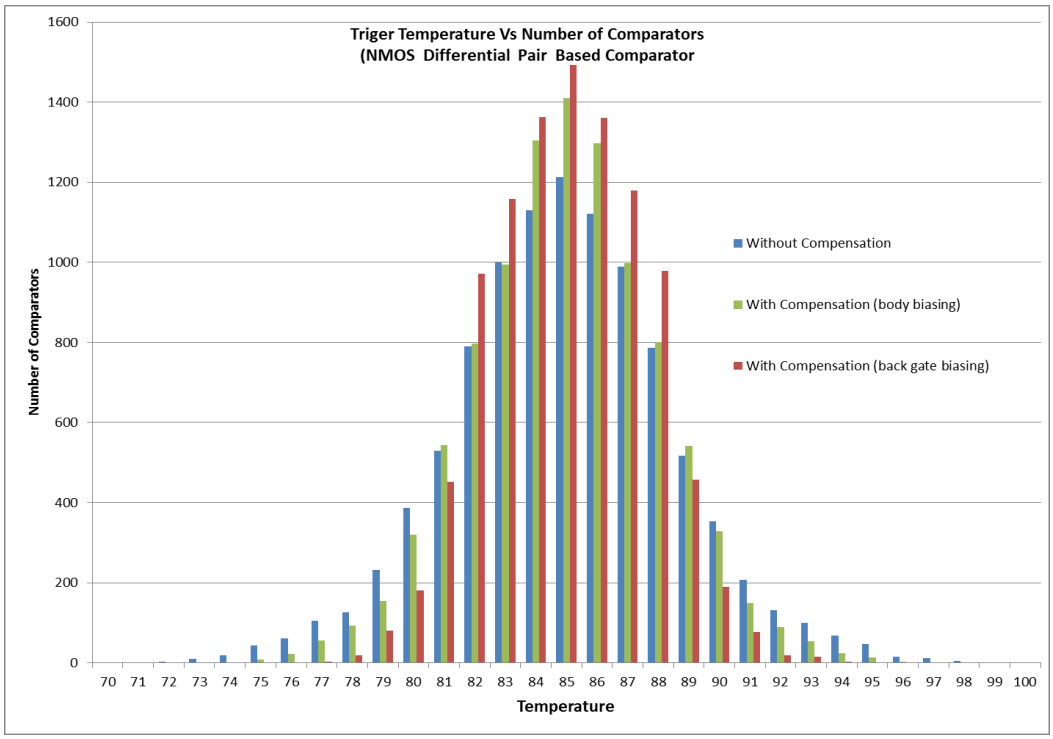
4.4.2 Results

Figure 20 shows the comparison between the circuit without compensation and circuit with compensation based on body biasing and back gate biasing for NMOS and PMOS differential pair based comparators. Self-compensation based on back

gate biasing gives the best results in both the cases. Self-compensation based on body-biasing has 3σ variation of 9 degrees and 8 degrees in case of comparator based on NMOS differential pair and comparator based on PMOS differential pair respectively. Whereas for self-compensation based on back gate biasing the 3σ variation of 7 degrees is same for both NMOS and PMOS differential pair based comparators. Thus with self-compensation with back gate biasing we have 3 degrees improvement in sensing accuracy for both NMOS and PMOS differential pair based comparators.

Figure 21 shows the comparison between the circuit without compensation and circuit with compensation based FINFET technology. The 3σ variation extends 7 degrees above and the mean value. This is an improvement of 2 degrees over the uncompensated comparator.

Figure 22 shows the comparison between different compensation techniques. Compensation circuit based on FINFET technology gives the best results followed by self-compensation based on back-gate biasing followed by self-compensation based on body biasing.



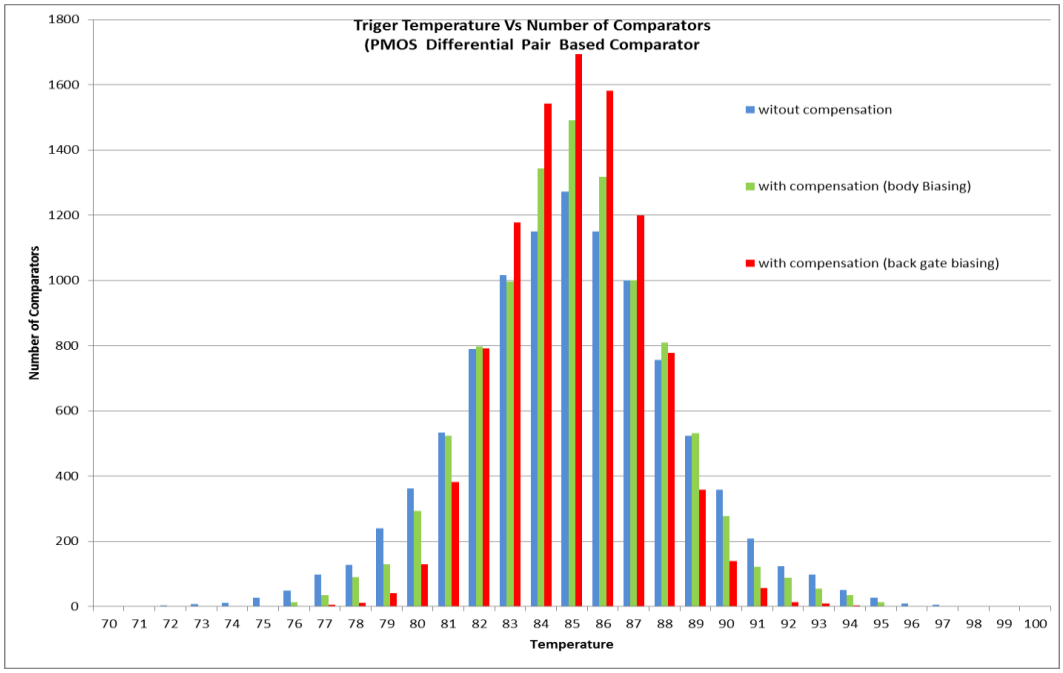


Figure 20: Histogram of trigger temperature for comparator with and without compensation (a) NMOS differential pair based comparator (b)PMOS differential pair based comparator

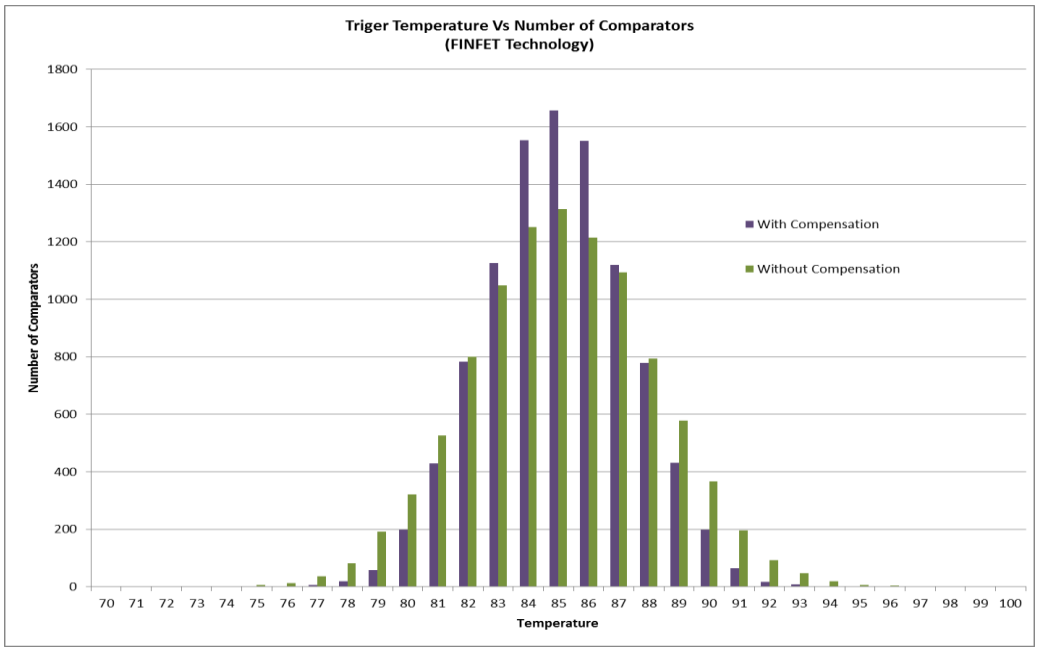


Figure 21: Histogram of trigger temperature for comparator with and without compensation for FINFET Technology

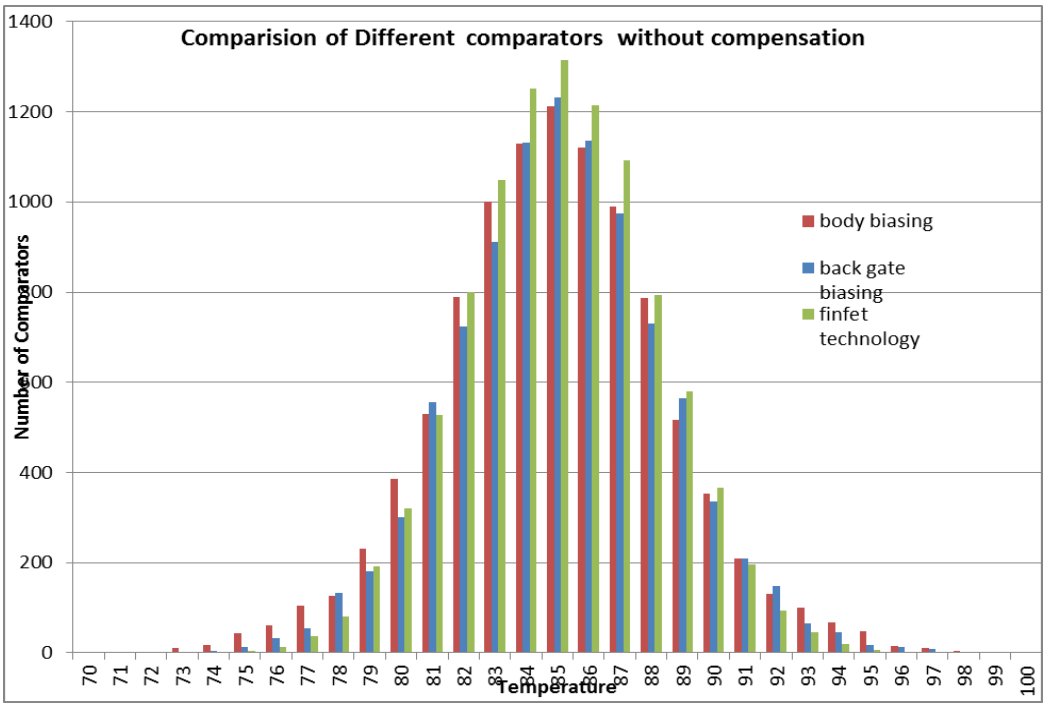


Figure 22: Histogram of trigger temperature for different self-compensation techniques

4.5 Area overhead

Comparator circuit with compensation circuitry has twelve transistors more than the comparator circuit without compensation circuitry, which imposes an area overhead of approximately 114%. However, in this architecture as diodes are the sensing units that are replicated throughout the chip, the extra transistors added do not cause much area overhead to the entire chip. Also in this architecture there is no area overhead due to the calibration unit.

CHAPTER 5

SELF-CALIBRATION USING DITHERED REFERENCE

5.1 Introduction

In most thermal sensors used today, the accuracy of sensing is improved by temperature calibration. Temperature calibration compensates for inaccuracies in temperature measurement and helps improve system accuracy. However, temperature sensor calibration is expensive. The costs for calibration depend mainly on the time the chip is in the tester. Time is needed to assure temperature stability, to obtain temperature information and to do the programming. Temperature calibration also imposes an overhead in design cost and silicon area. It requires pre heating and testing the sensor to know the offset, drift, slope and uncertainty errors. Once these errors are known the sensing unit is calibrated using A/D converters and look-up tables. Compensating for dynamic errors require even more complex signal processing. Thus, testing imposes test time overhead that translates to cost, while A/D converters and look-up tables impose area overhead.

We have shown in the previous section that accuracy of sensing can be increased by self-compensating but is still not comparable to the calibrated sensor. To increase the accuracy further, without an increase in test cost we propose a novel idea of signal dithering.

5.2 Dither

"Dither" is a British colloquialism for "undecidedness". Dithering is the process of injecting noise into the reference signal in order to reduce noise in measurement. Dither most often surfaces in the fields of digital audio and video, where it is applied to sample-rate conversions and to bit-depth transitions (but optionally if sufficient noise already is present). It is utilized in many different fields where digital processing and analysis are used, especially waveform analysis.

To explain dithering let us consider an example. We know that in digital system a bit becomes a “1” or a “0” depending on whether the input signal crosses a threshold or not. Let us consider that the value of each bit is worth one volt and the threshold is exactly 0.5. When the input signal gets above 0.5 volts, the bit turns on and becomes a “1”. When the input signal gets below 0.5 volts, the bit turns off and becomes a “0.”

If we add some dither to the signal it helps us determine the level of the input signal. Dither is a signal that is added to the input signal. The dither signal can be random noise, a triangular waveform, or some complex mathematically derived waveform. We will add a sinusoidal waveform to our signal that is exactly 0.5 (peak-to-peak voltage). This is half of the value of our “bit.” This sinusoidal waveform that we are adding to the signal makes our bit keep flipping from “0” to “1” as the combined signal crosses the 0.5 threshold. If the level of our input signal was exactly 0.5, and if we counted the ones and zeros for exactly one second we would have 22,050 zeros and 22,050 ones (at a 44.1kHz sample rate). The average

signal level during that second would be 0.5 which is exactly what our input signal is.

Now we change the input signal level to 0.75. When we count the zeros and ones for a second we get 33,075 ones and 11,025 zeros. This means that 3/4 of the time the signal registered as a "1" and 1/4 of the time the signal registered as a "0." The addition of the dither signal has increased the accuracy of our digital system without adding additional bits. Dither signals can be added in the analog domain to increase the signal capture resolution of the A/D converter, or it can be added digitally to increase the resolution after a 32bit DSP plug-in or after a level change or addition of reverb. When we transfer analog tape to digital, the noise floor of the analog tape makes the signal self-dithering.

5.3 Dither applied to comparator

We have seen earlier that the process variation of the sensor can be mapped to offset voltage of the comparator. However, after the chip has been manufactured the threshold voltages of the transistors are fixed and thus the offset voltage of the comparator does not change. If we can find out the offset voltage of the comparator we can increase the accuracy of the comparator tremendously. To find the offset voltage of the comparator, we dither the reference voltage V_{REF} of the comparator keeping the diode voltage V_{DIODE} constant. This can be done by adding a random noise into the reference voltage. For practical purposes the signal can be a simple sinusoidal signal. Once the offset voltage of the comparator is known the control logic multiplexes the V_{REF} such that the offset voltage is zero or very less. Figure 23 shows the overview of dithering.

In order to calculate the offset voltage, multiple measurements are made at a constant temperature with dithered reference signal. Depending on the number of 1s and 0s obtained at the output of the comparator we calculate the offset voltage. If the number of 1s and 0s are equal then there is no offset or in other words offset is zero. If the number of 1s is greater than number of 0s then the offset is negative i.e. the reference voltage has to be shifted left in order to make the offset zero and vice versa if number of 1s is less than number of 0s.

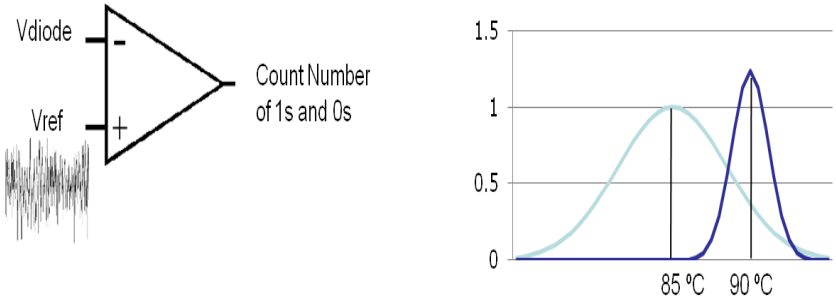


Figure 23: Overview of how dithering is done

The offset voltage is computed based on number of 0(1) at the output of the comparator. The conversion table is based on erf() function.

Let number of 1's at the output of comparator = 90%

Then we know that the Cumulative distribution function CDF of the output of the comparator = 0.9

We have the relation between CDF and ERF as $CDF = \frac{1}{2}\left(1 + erf\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right)$

We now have the relation $erf\left(\frac{x-\mu}{\sigma\sqrt{2}}\right) = 2CDF - 1$

Where erf is the error function and μ and σ are the mean and variance of distribution of the process variation

The above equation can be deduced to $\left(\frac{x-\mu}{\sigma\sqrt{2}}\right) = erf^{-1}(CDF - 1)$

We also have the relation $erf^{-1}(y) = \sqrt{\Pi}\left(\frac{1}{2}y + \frac{1}{20}\Pi y^3 + ...\right)$

From the above relations we can find x which is the reference voltage and (x-μ) which is the shift in the reference voltage or in other terms offset voltage of the comparator. Once we know the offset voltage of the comparator the sensing can be done accurately by changing the input reference V_{REF} with the offset obtained.

5.4 Experimental Setup

To find out the offset voltage of the comparator with the signal dithering by means of procedure explained in the previous section we need to know the mean and variance of the error function. To find the mean and variance of the error function first we took a sensor and introduce random process variation of 10 percent in the threshold voltage in the comparator. The 10 percent process variation was introduced by 500 montecarlo simulations in Hspice [32]. The distribution of the sensing temperature gave us the mean and variance of the error function.

To find out the offset voltage we applied the dither signal (random noise) to the reference signal and calculated the number of zeros and ones at the output. We mapped these numbers to the offset voltage of the comparator based on the

equations given in pervious section. A sample of 500 comparators (both differential and self compensating) was taken for the experiment.

The flow of the process is as shown in Figure 24.

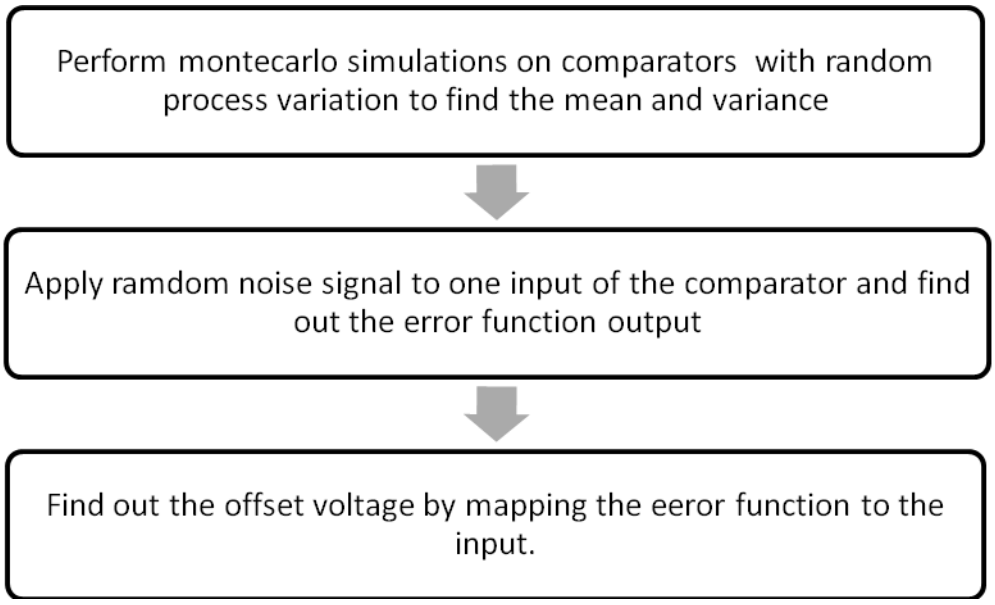


Figure 24: Overview of how dither is applied

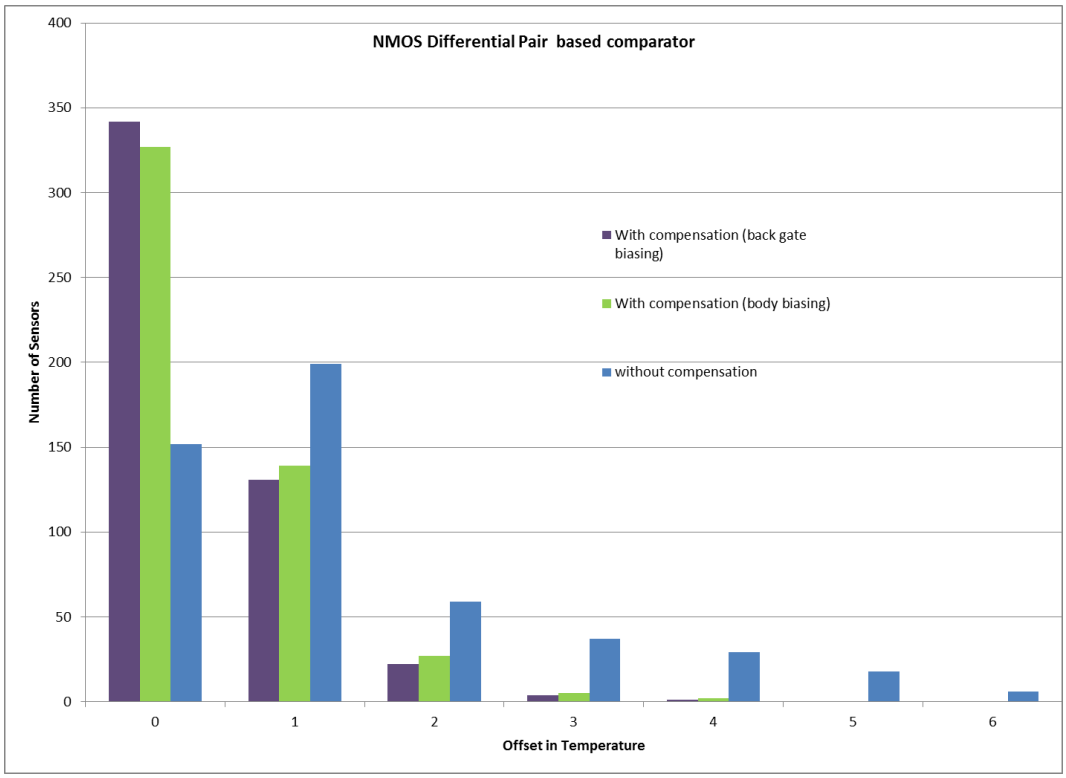
5.5 Results

The dithering results for the three cases of without compensation and compensation with body biasing and back gate biasing for the comparator based on NMOS and PMOS differential pair are shown in the Figure 25. Figure 26 shows the dithering results comparison between the circuit without compensation and circuit with compensation based FinFET technology.

Figure 27 shows the comparison between different compensation techniques. Compensation circuit based on FINFET technology gives the best results followed by self-compensation based on back-gate biasing followed by self-

compensation based on body biasing.

It is clear from the histogram that the accuracy improves with combination of active compensation and dithering. We have achieved an accuracy of 2 degrees for the self-compensated comparators. It is also seen that the accuracy of sensing improves 5 degrees for the comparator with any self-compensation.



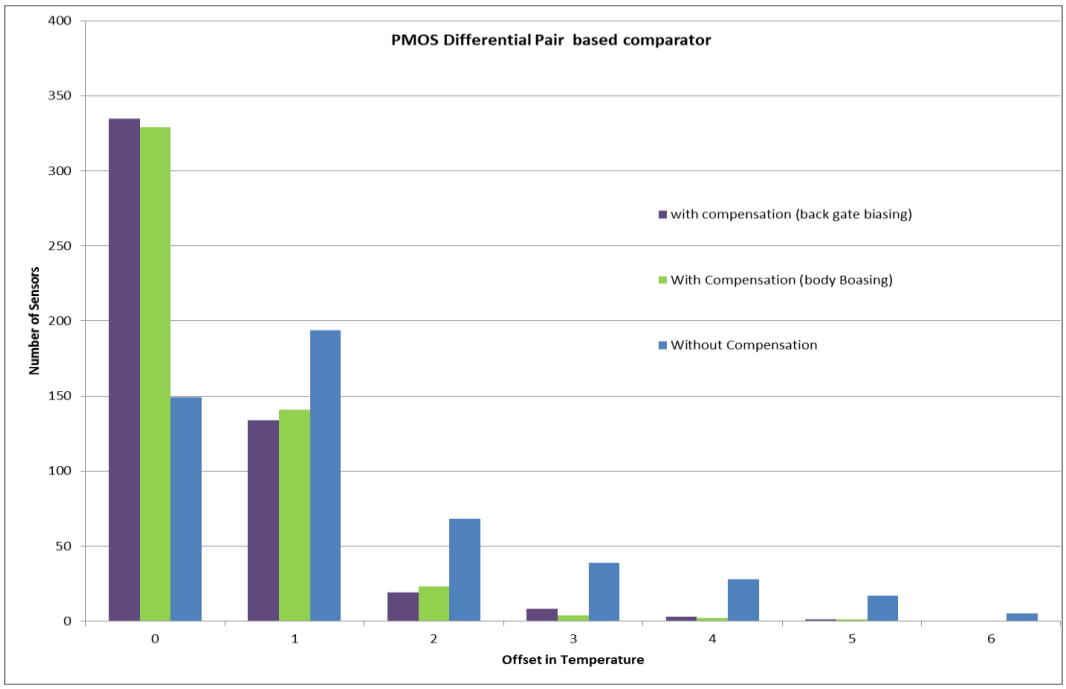


Figure 25: Number of sensors Vs Offset in temperature with and without compensation circuitry (a) NMOS differential pair based comparator (b)PMOS differential pair based comparator

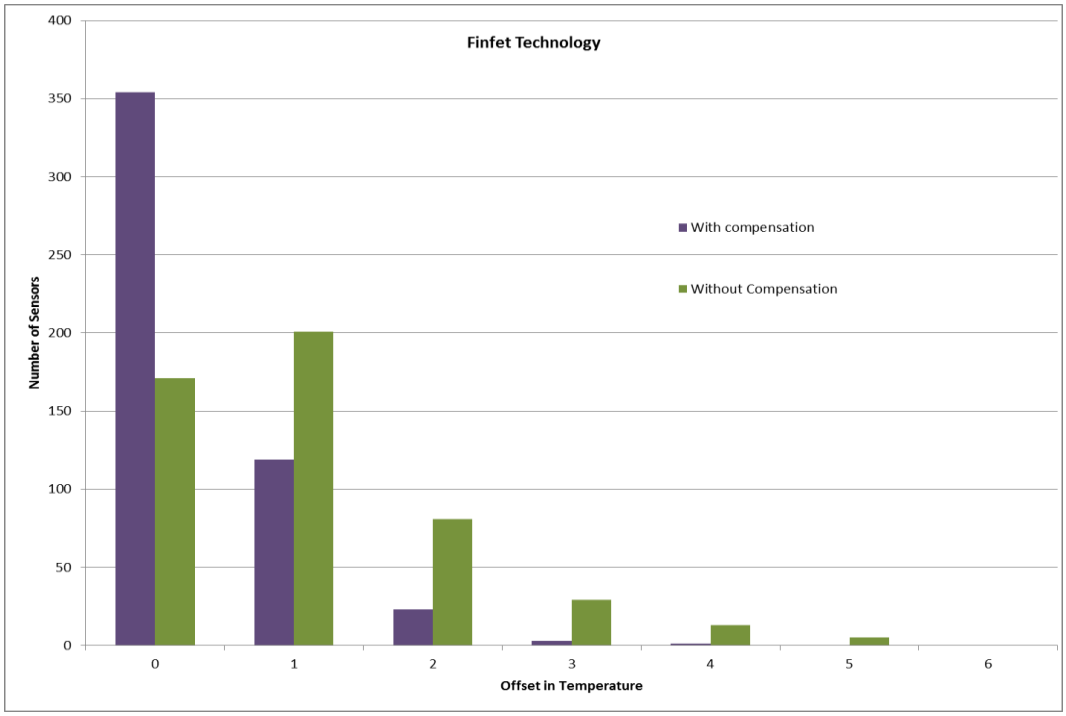


Figure 26: Number of sensors Vs Offset in temperature with and without compensation circuitry for FINFET Technology

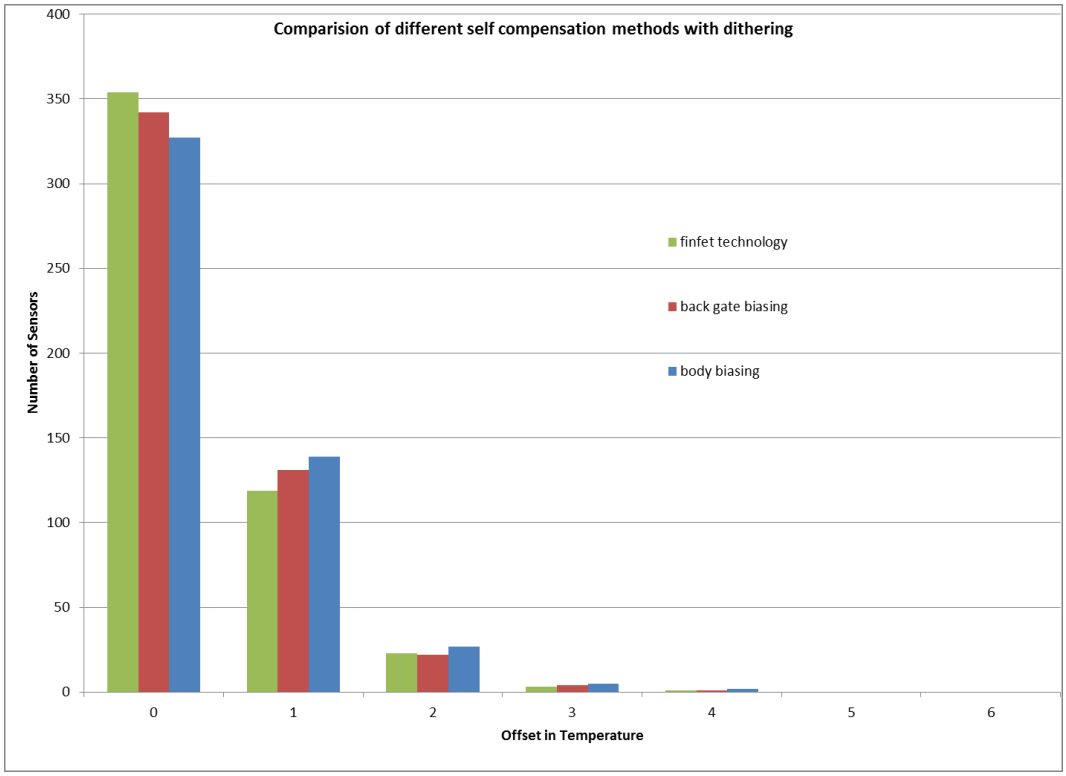


Figure 27: Number of sensors Vs Offset in temperature for different self-compensation techniques

CHAPTER 6

CONCLUSION

As thermal management systems gain greater use from mobile devices to mainstream processors, embedded thermal sensors are used more widely. Inaccuracy of thermal sensors reduces effectiveness of thermal management systems. Manufacturing process variations cause inaccuracy problems in thermal sensors. However, in many applications, cost considerations prevent calibration of thermal sensors.

We have presented a very small thermal sensor design with active process variation compensation circuitry that improves thermal sensor accuracy to 7 degrees. With the calibration technique and compensation scheme presented earlier, we achieve the targeted goal of less than 3 degree inaccuracy for 3σ variation in thermal sensing without using a tester based calibration system. This was the major goal of this work.

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