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ROBUST SIGNALING TECHNIQUES
FOR THROUGH SILICON VIA BUNDLES

A Thesis Presented

by

KRISHNA C CHILLARA

Submitted to the Graduate School of the
University of Massachusetts Amherst in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

September 2011

Department of Electrical and Computer Engineering

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ROBUST SIGNALING TECHNIQUES

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A Thesis Presented

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KRISHNA C CHILLARA

Approved as to style and content by:

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Wayne Burleson, Chair

____

Christopher Salthouse, Member

____

Russell Tessier, Member

____

C.V. Hollot, Department Head

Department of Electrical and Computer Engineering

DEDICATION

To my parents and brother

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I would like to thank my advisor Professor Wayne Burleson for all his support and guidance throughout this work. His constant guidance and valuable feedback helped me focus on the topics of this research. I thank Prof. Salthouse and Prof. Tessier for serving on my committee and providing valuable suggestions during the course of this work. Special thanks to Jinwook Jang for several valuable discussions we had regarding this work and other topics of common interest. I would like to thank Vinay, Basab and Ibis for their suggestions on several related topics on VLSI. I thank all my lab mates and friends specially Ashwin, Sud, Girish, Tej, Sudhi and Vikram for their support and encouragement. Finally I would like to thank my parents and my brother for their love and support.

ABSTRACT

ROBUST SIGNALING TECHNIQUES

FOR THROUGH SILICON VIA BUNDLES

SEPTEMBER 2011

KRISHNA C CHILLARA

B.TECH, VELLORE INSTITUTE OF TECHNOLOGY, INDIA

M.S.E.C.E., UNIVERSITY OF MASSACHUSETTS AMHERST

Directed by: Prof. Wayne P. Burleson

3D circuit integration is becoming increasingly important as one of the remaining techniques for staying on Moore's law trajectory. 3D Integrated Circuits (ICs) can be realized using the Through Silicon Via (TSV) approach. In order to extract the full benefits of 3D and for better yield, it has been suggested that the TSVs should be arranged as bundles rather than parallel TSVs. TSVs are required to route the signals through different dies in a multi-tier 3D IC. TSVs are excellent but scarce electrical conductors. Hence, it is important to utilize these resources very efficiently.

In high performance 3D ICs, signaling techniques play a crucial role in determining the overall performance of the system. In this work, 3x3 and 4x4 TSV bundles are considered. Electrical parasitics of TSV bundles are extracted using Ansoft Q3D Extractor. Various techniques for signaling over TSV bundles are analyzed in this work. Performance, energy and robustness are the crucial aspects to be considered for analyzing a signaling technique. For performance analysis, maximum data rate for each of the signaling techniques is obtained and the dominant factors that determine these values are identified. 3D integration is fairly a new field and does not have common

standards. Different research groups (both academic and industry) across the globe have different manufacturing technologies to suit their needs. In this work, we obtain the electrical parasitics of TSV bundles for different TSV radii ranging from 1μm to 15μm. The TSV radius for most of the 3D integration technologies falls within this range. Maximum data rates are determined for different TSV radii ranging from 1μm to 15μm. This study across different TSV radii helps in choosing a better signaling technique for a particular TSV radius depending on the design goals. Energy/bit for each of the signaling techniques is obtained for a common data rate of 10Gbps Pseudo Random Bit Sequence (PRBS) input. For robustness analysis, the impact of process, voltage and temperature variations between driver and receiver circuits is analyzed. Ansoft Q3D extractor, NCSU 45nm PDK and HSPICE simulation tool are used.

From the simulation results, it is observed that a differential technique is beneficial for smaller radii in terms of maximum data rate that can be obtained. For a radius above 7μm, single ended current mode signaling gives a better data rate. Low swing single ended signaling techniques consume less energy but suffer slightly more due to process variations compared to full swing voltage mode signaling. In terms of robustness to supply noise, differential signaling is more robust compared to single ended techniques. An increase in the temperature reduces the data rates of both single ended and differential signaling techniques. Hence, depending on the TSV radius of target technology and process and environment variations, an optimum signaling technique can be chosen.

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CHAPTER 1

INTRODUCTION

1.1 Moore's Law and Interconnect Bottleneck

Any digital system is composed of three main components: memory, data path and control logic. The performance in such systems primarily depends on how well these components can perform the required tasks while communicating with each other. At a lower level the two key factors that determine the overall performance of a digital system are device (transistor) delay and the interconnect delay. One approach to achieve higher performance is by technology scaling. By scaling, the channel length of the device is reduced. In other words, the charge carriers have to travel smaller distances in order to reach the drain terminal from the source terminal. This reduces the amount of time taken to move charge carriers from source to drain, thus resulting in faster circuits. The voltage required to drive the charge carriers after creating the channel is also reduced. This is significant as it reduces the amount of power consumed by the system.

Reduced device and interconnect helps to add more components on a single integrated circuit in compliance with Moore's law [1]. According to Moore's law, the number of transistors that can be added to an integrated circuit doubles every two years. Thus technology scaling has been the driving force behind the semiconductor industry to stay in course with Moore's law. However in Deep Sub Micron (DSM) technologies, scaling of interconnect is not in proportion to that of devices. According to Amdahl's law, overall performance of the system is determined by the slowest unit in the system.

At DSM technology nodes, interconnect delay is higher compared to device delay. Thus, interconnect which is relatively slow compared to device in terms of delay determines the overall performance of an Integrated Circuit. Furthermore, the increased functionality due to scaling has led to the scenario where the overall power is dominated by the interconnects. Hence, there is a need for new methodology to tackle this problem of Interconnect Bottleneck.

1.2 Motivation for 3D Integration

The primary reason for Interconnect bottleneck problem is that the interconnect delay increases in a quadratic manner with an increase in interconnect length [2] [3]. This is due to the linear dependency of both resistance and capacitance of interconnect on its length. Thus RC delay has a quadratic dependency on the wirelength. Techniques like tapered buffers and repeater insertion [4] are proposed to handle this interconnect bottleneck. In these techniques, buffers/repeaters are inserted in such a way that the repeater delay is equal to interconnect delay, thus making the delay a linear function of wirelength. But these repeaters in general are huge inverters consuming both area and power. There is a compromise in terms of power consumed [5] and area occupied with these approaches. One way to handle the interconnect bottleneck is to decrease the length of the interconnects. This was the motivation for the emergence of Three Dimensional Integrated Circuits.

1.3 Benefits of 3D Integration

In 3D Integration, different dies can be connected using inter-tier interconnects that directly pass through the substrate. This is called Through Silicon Via (TSV) based 3D integration technology. In 3D integration, the average interconnect length is reduced significantly. Figure 1.1 shows 2D and 3D implementation of a particular design containing both Memory and Logic. In 2D, the logic and memory are placed next to each other and interconnect of length L is required to make a connection. The same design when implemented in 3D, reduces the interconnect length significantly. At system level, it allows the integration of memory with logic, thus allowing larger memory at lower access times, addressing the Memory Bottleneck problem more efficiently.

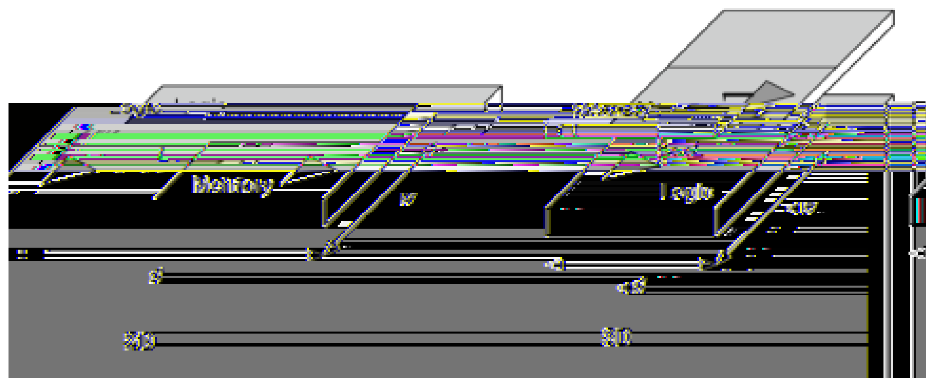

Figure 1.1 Long interconnects in 2D replaced with shorter 3D interconnects [6]

The inherent advantages of 3D ICs and their ability to go beyond Moore's Law make it more interesting to explore new designs based on 3D integration. Some of the potential benefits of 3D ICs are

1) Higher levels of integration

2) Shorter interconnects

3) Heterogeneous integration

4) High speed operation

5) Reduced risk of reverse engineering [7]

3D integration supports higher levels of integration for a given area. It also allows different designs to be implemented in different technologies. This is particularly useful for System on Chip (SoC) designs. In current 2D SoC designs, we are restricted to fabricate the entire chip in a single technology. Thus, 2D SoC designs require analog, digital and RF blocks to be implemented in a single technology. In 3D integration, different wafers can be stacked using TSVs. Hence it can be used for heterogeneous integration as shown in Figure 1.2.

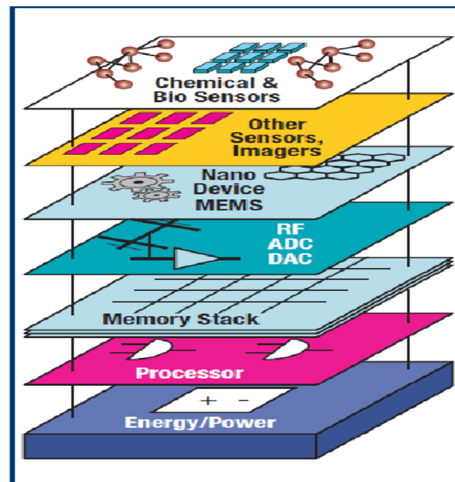

Figure 1.2 Heterogeneous 3D Integration[8]

1.4 Challenges in 3D Integration

In this section, some of the challenges associated with 3D ICs are discussed. Due to the increasing demand for higher functionality, processors with billions of transistors are in demand. The biggest challenge in such processors is the increasing power density and associated thermal issues. In order to fully utilize the benefits of 3D, it is beneficial to have as many tiers as possible. This increased stacking leads to an increased power density. In 3D ICs, the tier that is farthest from the heat sink will have the highest thermal resistivity and requires greater time to dissipate the heat. The results in [8] show that the temperature increases by 17K for 2 die stack and 33K for a 4 die stack.

Apart from thermal issues, several challenges related to 3D CAD tools remain unaddressed. Due to the addition of another dimension, the complexity in the design and verification increases. It becomes a more complicated problem in case of 3D ICs with heterogeneous integration. Due to this increased complexity, the design flow should include many more hierarchical levels. Apart from this, 3D thermal, signal and power TSVs have to be supported by the CAD tools. This demands the need for 3D tools from physical design to logic verification. Most of the logic and functionality verification tools available for 2D can be utilized for 3D circuits. CAD tools, like 3D CACTI [10] and NCSU3D PDK [11] which can support 3D layout up to 2 layers, are available. But the current version of NCSU 3DPDK cannot extract the RLC parasitics for 3D ICs. Another academic tool from MITLL can only support the 180nm 3D SOI technology. Considering the current 2D processor technology nodes, 180nm is far behind from ITRS roadmap of 28nm technology for 3D ICs.

Post silicon validation and testing for 3D ICs is a big challenge. Techniques that are used for 2D ICs can no longer be effective for 3D ICs. A new approach to handle these 3D ICs is yet to be developed. TSVs in contact with interconnects made of another material (aluminum or copper) are sensitive to temperature. Variations in temperature would lead to the production of a voltage relative to the temperature difference between the two materials. This voltage would affect the signal on the TSV, introducing a significant noise component. Reliability is one of the biggest concerns for 3D ICs. Although TSVs are excellent electrical conductors, a failed TSV can cause a number of known good dies that are stacked together to be discarded. Hence, it is a good idea to consider some fault tolerance scheme. However, this increases additional resources as well as TSV count. These challenges have to be addressed to extract the full benefits of 3D ICs.

1.5 Problem Statement

This thesis is aimed at identifying *Robust signaling techniques for Through Silicon Via bundles*. Most of the earlier work on TSVs has been focused on electrical characterization and modeling. The first work on signaling over TSVs has been carried out by Weerasekera in [12]. But it was restricted to single ended signaling on 3 parallel TSV structures for a particular TSV technology. In order to extract the benefits of 3D, it is important to consider an array of TSVs (also called a TSV bundle), which helps in more efficient usage of die area and yield [13]. Hence, analyzing the signaling schemes over TSV bundles is important.

The following are the contributions of this work.

- We explored various signaling techniques like single ended voltage mode, current mode and differential technique. We obtained the maximum data rates for each of these signaling techniques and identified the factors that determine these numbers.

- Electrical parasitics of a TSV bundle vary with TSV radius. Due to lack of standards for signal TSVs, different research groups across the globe have different manufacturing technologies with different TSV radii. In this work, we considered various TSV radii to understand when a particular signaling technique (single ended or differential) might be beneficial to use.

- Robustness analysis of these signaling schemes is an important aspect. In this work, we analyze the impact of process, voltage and temperature variations on signaling over TSV bundles with focus on variations between the driver and receiver circuits which are residing on different dies.

Thus, in this work we explore signaling over through silicon via bundles, identify the key factors that determine the performance of a particular signaling technique and finally perform robustness analysis to identify the most optimum signaling technique for TSV bundles for a given TSV radius.

1.6 Document Organization

The rest of this document is organized as follows:

- Chapter 2 deals with the necessary background information and related prior work.

- Chapter 3 is dedicated to TSV parasitic extraction and analysis of its electrical parasitics and crosstalk.

- Chapter 4 explores various signaling techniques over TSV bundles and their performance for various TSV radii.

- Chapter 5 contains the robustness analysis.

- Chapter 6 provides the conclusion and suggestions for future work.

CHAPTER 2

BACKGROUND AND PRIOR WORK

This chapter provides the necessary background information on the 3D integration with focus on Through Silicon Via (TSV) based 3D ICs and related prior work on TSV characterization and signaling techniques in such 3D ICs.

2.1 3D Integration Technologies

Apart from its several other benefits, 3D integration allows stacking of dies with different technologies. Several techniques are used for stacking of the chips for 3D integration. Some of them place the individual chips one over the other and connect them across the periphery. These techniques suffer due to the reduced number of I/O connections like in 2D. Such packaging techniques like System in Package (SiP) and Chip Stack Multi-Chip-Module (MCM) do not integrate the chips into a single circuit. True benefits of 3D can be realized using TSV based 3D integration. In TSV based 3D integration, multiple chips can communicate with each other with the help of direct connections in the vertical direction. Such techniques in general are referred to as 3D integrated circuits or simply 3D ICs.

Integration techniques like wire-bonding, micro-bumps, through-vias, and contact less interconnects differ from each other in terms of their density and limitations in their usage. Wire-bonding is the most common approach for general purpose applications. These applications do not include the high performance processors or real time high performance embedded systems. However, it is not a true 3D integration as shown in

Figure 2.1. In this technique, all the connections should go through the chip carrier. The primary advantage of wire-bonding is its reduced complexity and low cost as it simply connects the dies across the periphery. The drawback of this approach is its limited integration density as the communication between the dies is restricted to the periphery, as shown in Figure 2.1. The number of metal layers needed for pads is also more due to the increased mechanical stress, which has the potential to destroy the devices under the pad due to extreme pressure.

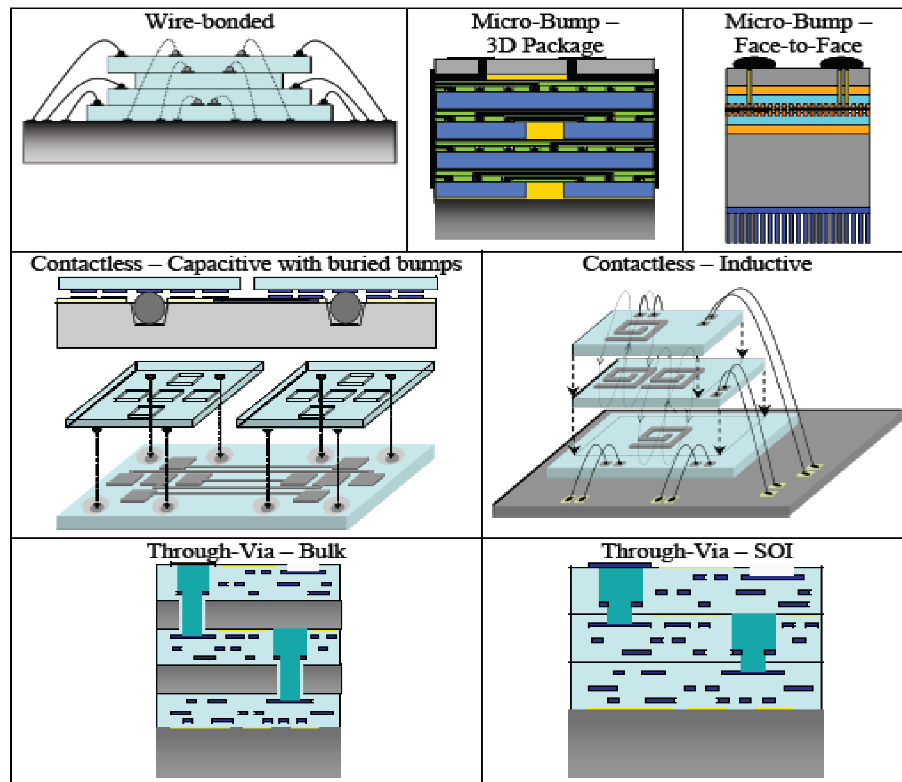

Figure 2.1 Various 3D Integration Technologies [19]

Micro-bumps technology uses the solder to make connections on the surface of the die [12]. The mechanical stress in this technique is comparatively lower than that of the wire-bonding approach, thus requiring only one metal layer for pads. The number of

layers it can handle is primarily limited by the heat assembled inside the package rather than the assembly process. Face-Face approach provides better performance due to the reduction in the parasitics. The primary disadvantage with face to face approach is its inability to support more than two tiers.

As discussed earlier, 3D circuits can be realized using TSVs. TSVs provide the most promising solution for high performance 3D Integrated Circuits. These TSVs can be assembled in a wafer-wafer approach or die-wafer approach, depending on the application and yield requirements. Generally, the wafer-wafer approach provides higher yield but supports fewer heterogeneous technology integration compared to die-wafer approach. These can be bonded in face-face or face-back manner depending on the application. TSVs with very small dimensions are obtained in Silicon on Insulator (SOI) technology [15] compared to the bulk approach [16]. This is primarily due to low substrate thickness in SOI and hence, for a given aspect ratio, smaller TSV diameters and therefore smaller pitches can be used in 3D SOI technology. The contactless interconnects are achieved using the capacitive and inductive coupling [17] [18] for communication between the layers. This approach is more suitable where there are 3-4 chips that are stacked and communication is required between the chips throughout the stack.

Structured definitions of 3D Interconnect technologies as presented in ITRS [20] are shown in Table 2.1. TSV based 3D integration for high performance applications falls into the category of 3D SICs and 3D ICs as mentioned in Table 2.1, and referred to as 3D ICs throughout the document. Since this work is primarily focused on developing robust

signaling techniques for high performance applications, we will discuss more about TSV based 3D ICs or simply 3D ICs in the next section.

Table 2.1 3D Interconnect Technologies based on Interconnect hierarchy [20]

Level	*Suggested Name*	*Supply Chain*	*Key Characteristics*
Package	3D-Packaging (3D-P)	OSAT Assembly PCB	▪ Traditional packaging of interconnect technologies, e.g., wire-bonded die stacks, package-on-package stacks. ▪ Also includes die in PCB integration ▪ No through-Si-vias (TSVs)
Bond-pad	3D-Wafer-level Package (3D-WLP)	Wafer-level Packaging	▪ WLP infrastructure, such as redistribution layer (RDL) and bumping. ▪ 3D interconnects are processed after the IC fabrication, "post IC-passivation" (via last process). Connections on bond-pad level. ▪ TSV density requirements follow bond-pad density roadmaps.

Global	3D-Stacked Integrated Circuit/ 3D-System-on-Chip (3D-SIC /3D-SOC)	Wafer Fab	▪ Stacking of large circuit blocks (tiles, IP-blocks, memory –banks), similar to an SOC approach but having circuits physically on different layers. ▪ Unbuffered I/O drivers (Low C, little or no ESD protection on TSVs). ▪ TSV density requirement significantly higher than 3D-WLP.
Intermediate	3D-SIC	Wafer Fab	▪ Stacking of smaller circuit blocks, parts of IP-blocks stacked in vertical dimensions. ▪ Mainly wafer-to-wafer stacking. ▪ TSV density requirements very high.
Local	3D-Integrated Circuit (3D-IC)	Wafer Fab	▪ Stacking of transistor layers. ▪ Common BEOL interconnect stack on multiple layers of FEOL. ▪ Requires 3D connections at the density level of local interconnects.

2.2 Through Silicon Via based 3D ICs

In Through Silicon Via based 3D ICs, as the name indicates, the vertical interconnect (TSV) will cut through the silicon substrate forming a connection between the two tiers. Generally the TSVs are filled with Cu or W metal and a dielectric coating is applied to prevent any diffusion of the metal into the silicon substrate. Several

approaches can be used to realize this and all the approaches have three common modules [20], as mentioned below.

1. Order of Through Silicon Via process
2. Wafer thinning, thin wafer handling and backside processing
3. The actual 3D-Stacking process.

Depending on the order in which the TSV process occurs with respect to the device fabrication process, the TSV process can be characterized into Via first, Via middle and Via last approach. In Via first approach, TSVs are fabricated before the Front End of Line (FEOL) process. In Via middle approach, TSVs are fabricated after the FEOL but before the Back End of Line (BEOL) process. In Via last approach, the TSV fabrication takes place after the BEOL. 3D ICs can also be differentiated depending on the method of 3D Bonding. Three common approaches are

1. Wafer to wafer (W2W) bonding
2. Die to Wafer (D2W) bonding
3. Die to die (D2D) bonding

Apart from this, secondary classification is made depending on whether it is a Face to face (F2F) bonding approach or Face to back (F2B) approach. Figure 2.2 represents various key process modules in TSV based 3D ICs.

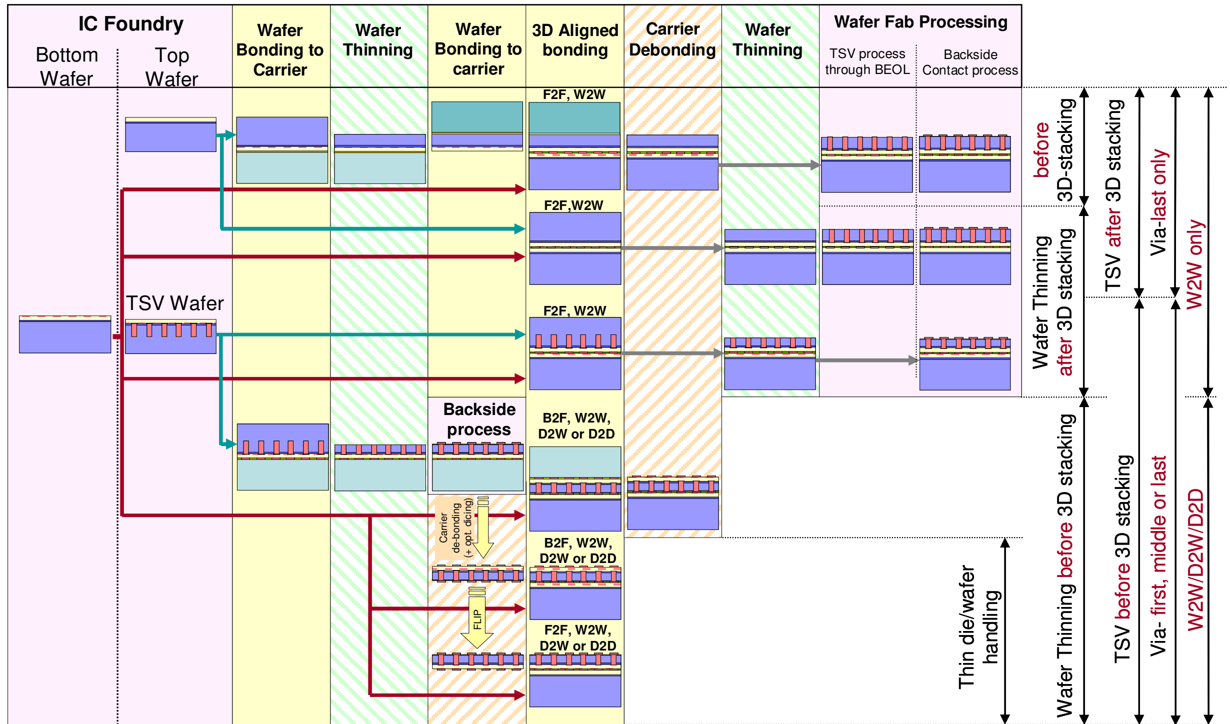

Figure 2.2 Schematic representing the key process modules in 3D ICs. [20]

The performance of 3D ICs depends on the vertical interconnect (TSV) parasitics. Since the electrical characteristics of TSVs are primarily dependent on their physical material, geometry and dimensions, ITRS proposed the roadmap for the minimum TSV dimensions for interconnects as shown in Table 2.2. From Table 2.2, it can be observed that the pitches in general are twice the diameter. The minimum TSV depth can be as low as 20 µm.

Table 2.2 ITRS roadmap for TSV dimensions for interconnects [20]

Global Level, W2W, D2W or D2D 3D-stacking	*2009-2012*	*2012-2015*
Minimum TSV diameter	4-8 µm	2-4µm
Minimum TSV pitch	8-16 µm	4-8 µm
Minimum TSV depth	20-50 µm	20-50 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Number of tiers	2-3	2-4

Having discussed the key features of 3D integration technologies in general and TSV based 3D ICs in particular, it is important to understand the electrical characteristics of TSVs. Resistance, Inductance and Capacitance of the TSV play a crucial role in determining the overall performance of 3D ICs. As this work is focused on signaling techniques over TSV based 3D ICs, a background on TSV modeling and electrical characterization is presented in the following section.

2.3 Through Silicon Via parasitic extraction

The purpose of TSV modeling is to obtain the equivalent circuits that can completely describe the electrical characteristics of the TSV. A simple RLC lumped model of a single interconnect is shown in Figure 2.3. It consists of a series resistance, series inductance and parallel capacitance. Depending on the geometrical dimensions of the interconnect, the values of R, L and C vary significantly.

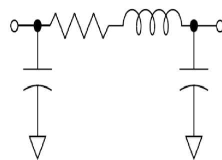

Figure 2.3 RLC modeling of interconnect.

Through Silicon Via modeling should expand the single interconnect modeling of Figure 2.3 by including the impact of silicon substrate, dielectric insulator and coupling effects from surrounding TSVs. A simple electrical equivalent model of 3 parallel TSVs with one of them used as signal TSV and the remaining two connected to ground is

shown in Figure 2.4. Through Silicon Via, as the name suggests, is a via across the silicon substrate. Generally Cu or W is used as the metal filling for the TSV. SiO_2 dielectric can be used as coating over the metal to avoid any DC leakage of metal into the substrate.

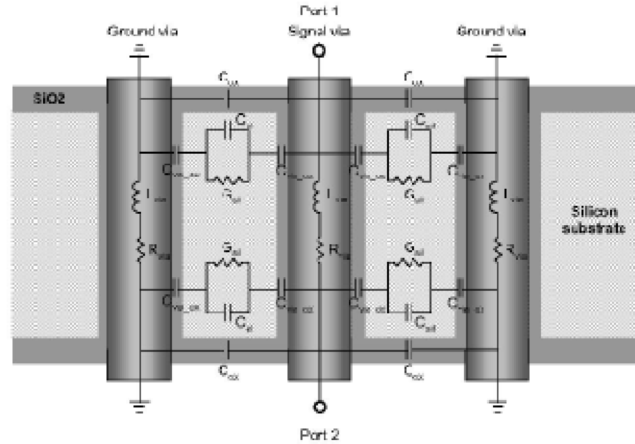

Figure 2.4 Equivalent Circuit Model of Through Silicon Via GSG [21]

Several attempts have been made to understand and model the electrical characteristics of Through Silicon Vias. In [22], Friedman et al. have developed the closed form expressions for a 3D via. Closed form expressions for R, L and C developed in [22] are for a single 3D via. Though these expressions cannot be used directly for a group of TSVs, it provides a good model to understand the electrical behavior of Through Silicon Vias.

RLC coupling between two 3D Vias is investigated in [24]. Ansoft Quick 3D extractor [25] is used for RLC parasitic extraction. RLC parasitic extraction is carried out for various configurations by increasing the distance between the two 3D Vias. The results explained that the values of DC coupling capacitance and inductance decrease

with via separation and the AC R, L and C values tend to approach the extracted RLC values of a single 3D via. In [22] and [24], multiple configurations of parallel 3D vias with and without ground plane are considered for the extraction of RLC parasitics. The inclusion of ground plane did not affect the total resistance or inductance but drastically increased the capacitance. The closed form expressions developed are only for individual TSVs and hence cannot be used for obtaining all the parasitics, including coupling for all the surrounding TSVs in case of an array or bundle of TSVs.

Most recent work on developing equivalent lumped element models for n-port TSV models is presented in [23]. In [23], the authors proposed an equivalent lumped model for multi-TSV arrangements. The closed form expressions are developed in terms of physical dimensions and material properties. For checking the accuracy of the model, Q3D extractor is used for extracting the electrical parasitics of various TSV configurations. Each TSV is surrounded by a SiO_2 dielectric coating. The silicon substrate surrounding the TSVs is connected to ground plane.

In [26], electrical characterization of TSVs depending on number of TSV stacks is analyzed. S-parameters for a frequency range of 100MHz to 30GHz are obtained. The s-parameters from 3D full wave simulation are used to evaluate the signal integrity. (2^7-1) PRBS data streams at 1 Gbps, 2 Gbps, 5 Gbps and 10 Gbps with a 10% rise and fall time are considered. The eye diagrams are obtained by passing the bit stream through a single TSV once and through the stack of 2, 5 and 10 TSVs next, to understand the impact of TSV stacks. It is observed that for a single TSV, capacitance is the dominating factor whereas for a stack of 10 TSVs resistance and capacitance both dominate.

2.4 Delay and power in 2D and 3D interconnects

In this section, we will see after what length of 2D interconnect it is beneficial to switch to 3D interconnect both in terms of delay and power. For this study we consider 2D and 3D interconnects with similar driver and load. 2D interconnect model is shown in Figure 2.5. In this we considered a PI-model. PI-model gives Elmore delay equal to distributed RC model delay [27]. In 3D interconnects, capacitance is the dominating factor [28] and it is represented by C_{TSV} in Figure 2.6. R_{TSV} is not considered in Figure 2.6 as its resistance is much less compared to driver resistance (R_D). The delay equation considering R_{TSV} and modeling it similar to 2D interconnect PI-model is given by

$$T_{3D} = 0.5 R_D C_{TSV} + 0.5(R_D + R_{TSV})C_{TSV} + (R_D + R_{TSV})C_{Load}$$

R_D is few hundreds of ohms and R_{TSV} is few tens of milli-ohms. Hence we can ignore R_{TSV} and model the TSV as a capacitive load. The authors in [28] also modeled the TSV as a capacitive load for the delay analysis through TSVs stating that R_{TSV} has negligible impact on delay.

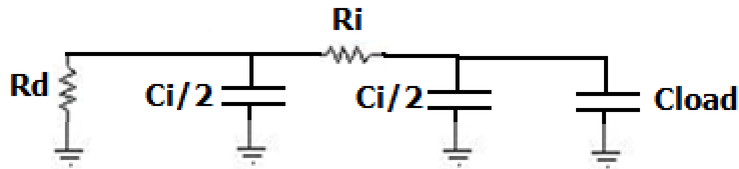

Figure 2.5 2D interconnect with driver and load

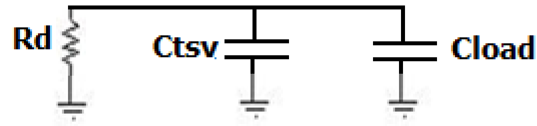

Figure 2.6 Simple model of 3D interconnect with driver and load

Now, we will see the equivalent length of 2D interconnect that gives delay equal to that of a 3D interconnect.

Delay of 2D interconnect is given by

$$T_{2D} = 0.5R_D C_I + 0.5(R_D + R_I)C_I + (R_D + R_I)C_{Load}$$

R_D is th driver resistance, C_I is interconnect capacitance, C_{Load} is load capacitance, Considering the unit length capacitance and resistance of interconnect in 45nm technology, we have capacitance per 1mm of length = 250fF and resistance per 1mm of length = 69.84 ohm [29].

Let us say capacitance per 1mm length = a

Resistance per 1mm length = b

Let the length of 2D interconnect be l_{2D}.

$$T = R_D(al_{2D}) + (al_{2D})(bl_{2D}) + (bl_{2D})C_{Load} + R_D C_{Load}$$

Now we will estimate the delay in case of 3D.

$$T_{3D} = R_D(C_{Load} + C_{TSV})$$

For a TSV radius of 5µm and length of 25µm, the equivalent length of 2D interconnect for equal delay is calculated to be 154µm. If we do not consider the driver resistance for both 2D and 3D interconnects just to compare the 2D interconnect with TSVs, we see that the length of 2D interconnect that gives the delay equal to a TSV (of length 25 µm and radius 5µm) is 0.7µm. This is due to much lower resistance of TSV compared to 2D interconnect for a given length.

However when driver resistance is considered we observed that for 2D interconnects with length higher than 154µm it is beneficial to move to 3D interconnect (radius 5µm and length 25 µm).

Now we will do similar estimation in terms of power. The interconnect power dissipation is given by

$$P = 0.5kfC_I V^2$$

P is the power dissipation

C_I is interconnect capacitance

V is voltage on the interconnect

k is the activity factor

f is the frequency of operation

Considering similar activity factor, frequency and voltage on the interconnect we can estimate the length of 2D interconnect that dissipates equal power compared to 3D interconnect. The calculated length of 2D interconnect that has equal power dissipation

through the TSV of radius 5µm and length 25 µm is 160µm. From this study we observed that it is beneficial to use 3D interconnects when length of 2D interconnect exceeds 154µm (for delay) and 160µm (for power).

2.5 Signaling, supply noise and reliability in 3D ICs

2.5.1 Signaling over TSVs

Most of the earlier work has been focused on electrical modeling and characterization of TSVs and very little has been explored on signaling techniques for 3D ICs. TSVs are excellent electrical interconnects but occupy significant area. In [12], the authors considered 3 parallel TSVs to explore signaling over TSVs and crosstalk for a particular TSV technology. Figure 2.7 shows the simulation setup for investigating the effect of crosstalk in 3 parallel TSVs used in [12].

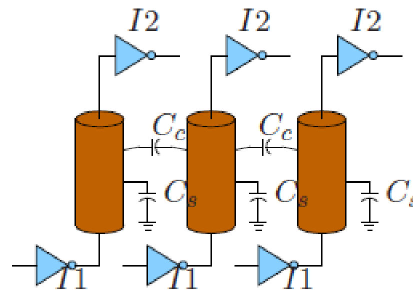

Figure 2.7 Signaling over 3 parallel TSVs [12]

Simple voltage and current mode signaling using inverters as drivers is considered in [12]. For current mode, self-biased inverters are considered at the receiver to provide low impedance. A Pseudo Random Bit Sequence with 10ps rise and fall times and a period of 200ps is applied to 3 parallel TSVs. For the dimensions considered in [12],

coupling is not negligible and shielding technique is employed to reduce the impact of coupling. In shielding technique, crosstalk between the conductors is reduced by introducing shield conductors between the signal conductors. Figure 2.8 shows how the introduction of a ground conductor turns coupling capacitance into capacitance to ground.

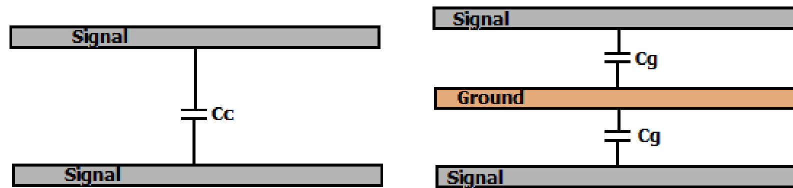

Figure 2.8 Shielding technique

2.5.2 Supply Noise in 3D ICs

Power distribution network plays a crucial role in determining the overall performance of the system. In general, supply noise can be categorized into two types:

1. Static Noise
2. Dynamic Noise

Static Noise is primarily due to the IR drop, as the supply voltage has to pass through the RLC networks associated with the power distribution scheme. The impact of IR drop can be handled by designing a more efficient and balanced power distribution network such as power grids. However, dynamic noise is due to the fluctuations in the supply voltage depending on the activity of the functional blocks. The inductance component of the supply network contributes to the dynamic noise. Maximum supply voltage drop occurs during the first droop. With increased scaling, the voltage levels have

come down significantly. Adding to this, the number of functional blocks on a single chip has increased tremendously, consequently demanding higher currents. Designing an efficient power distribution network in Deep Sub Micron (DSM) technologies has been the biggest challenge.

In 3D ICs, by stacking several tiers we are increasing the functionality of the single chip. Also the power distribution network should tackle the additional noise due to the activity in different tiers. 3D stack with k tiers would require k-times higher current compared to a single 2D chip with the same footprint. The supply noise amplitude in stacked 3D ICs is found to be as high as 10% of the supply voltage for a stack of 2 dies. The dynamic noise can increase to up to 240mV (24% of VDD) for a stack of 5 dies [27] [31].

2.5.3 TSV Fault tolerance using redundancy

Improving the yield is another important aspect in 3D ICs. It is suggested in [13] that arranging the TSVs in the form of blocks, as shown in Figure 2.9, can provide higher yield compared to sprinkling the TSVs all around. Redundancy based fault tolerance is a simple solution to handle the problem with TSV faults. Each TSV block can contain a TSV chain which includes the fault tolerance architecture. A simple architecture shown in Figure 2.10 can be used as a fault recovery mechanism.

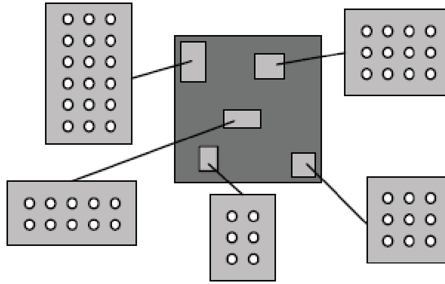

Figure 2.9 Arranging the TSVs in the form of blocks improves yield [13]

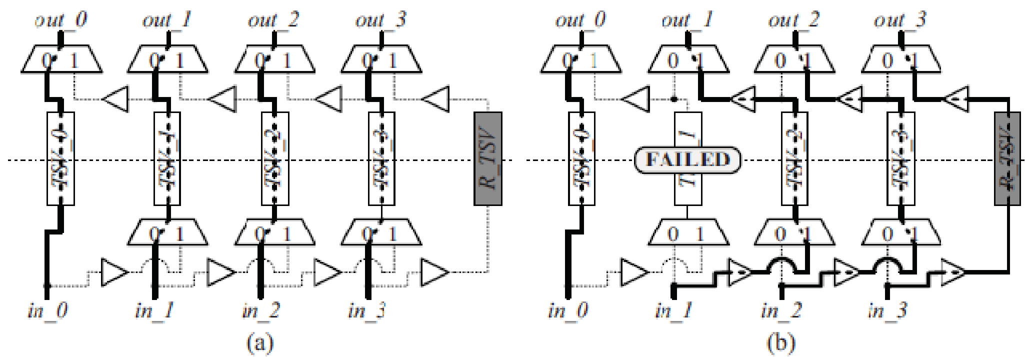

Figure 2.10 Fault Recovery Mechanism a) No failure b) TSV_1 is failed [13]

From Figure 2.10 (b), it can be observed that all TSVs towards the right starting from TSV_1 are shifted. This provides good performance improvement when compared to shifting only the failed TSV signal all the way to the end. Since it is the slowest signal that determines the overall performance, it is advantageous to shift all the signals by 1 unit as shown in Figure 2.10 (b).

In this chapter necessary background information is provided. TSV modeling and parasitic extraction, signaling techniques for TSVs and various factors that can impact the signaling over Through Silicon Vias like power supply noise are discussed. Through Silicon Via parasitic extraction and their electrical characteristics are covered in Chapter 3.

CHAPTER 3

THROUGH SILICON VIA PARASITIC EXTRACTION

As we go into the Deep Sub-Micron (DSM) era, parasitic effects have to be considered. 3D field solvers provide more accurate information on the parasitic values compared to first order analytical expressions. In general, these field solvers require significant computation time and resources. Most of the parasitic effects of the 2D interconnects are well studied and simple analytical models are developed. Since 3D ICs are still in the phase of development, simple electrical models of 3D interconnects are not yet available. This is primarily due to the lack of standardization, which resulted in a wide range of TSV dimensions that can be chosen depending on the application. As mentioned in Chapter 1, there is no proper CAD support for 3D interconnects. Currently NCSU3DPDK is the only available academic PDK for 3D ICs using bulk CMOS technology. It is still in the development phase and currently does not support RLC parasitic extraction and post layout simulation. Hence, 3D field solvers are generally used to obtain the electrical parasitics of TSV.

In this chapter, we first explain the methodology used for the extraction of RLGC parasitics of Through Silicon Via bundle and their frequency dependency. Q3D extractor, a 3D field solver from Ansoft, is used for the parasitic extraction.

3.1 TSV parasitic extraction methodology

The step-by-step procedure to be followed for the extraction of TSV parasitics using Q3D extractor is shown in Figure 3.1.

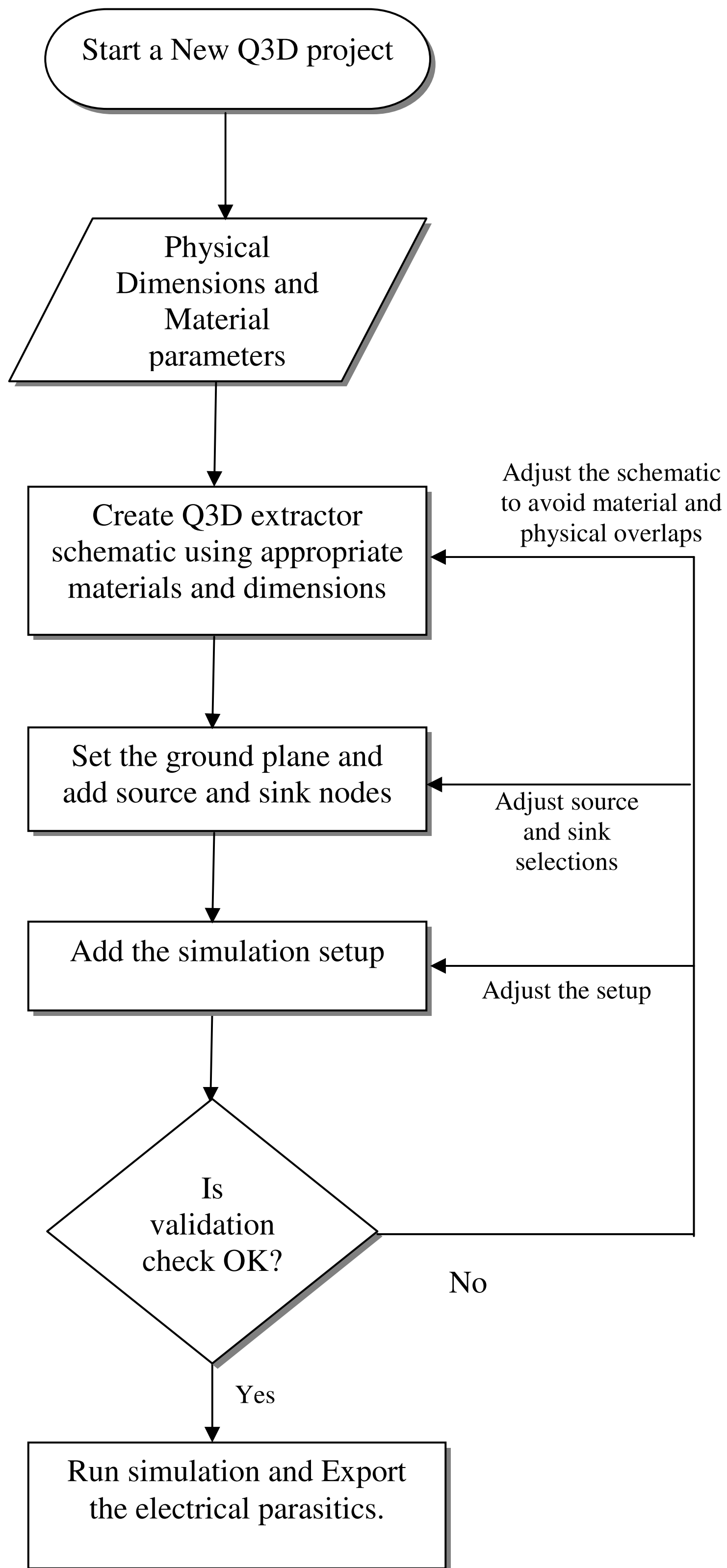
Start a New Q3D project
Physical Dimensions and Material parameters
Create Q3D extractor schematic using appropriate materials and dimensions
Adjust the schematic to avoid material and physical overlaps
Set the ground plane and add source and sink nodes
Adjust source and sink selections
Add the simulation setup
Adjust the setup
Is validation check OK?
No
Yes
Run simulation and Export the electrical parasitics.

Figure 3.1 RLGC parasitic extraction methodology using Q3D

Schematic of 3x3 TSV bundle developed in Q3D extractor is shown in Figure 3.2.

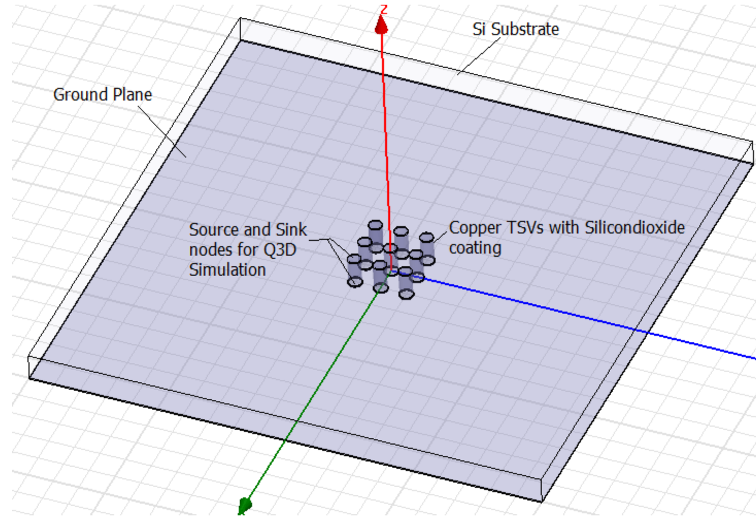

Figure 3.2 Q3D Schematic of 3x3 TSV Bundle

Q3D schematics of Through Silicon Vias with dielectric coating over them are made and embedded in a silicon substrate. Copper is chosen to be the TSV metal fill. Silicon is chosen as the substrate material. Silicon dioxide is used as a dielectric material. The geometrical dimensions of TSV bundles shown in Figure 3.2 are

1. TSV diameter = 10 µm
2. TSV pitch = 20 µm
3. TSV height = 25 µm
4. Thickness of dielectric coating over TSV = 0.2 µm
5. Silicon substrate = 400 µm x 400 µm

Once the schematic is ready, the source and sink nodes along with the ground plane are defined. In the simulation setup, a new frequency setup is created and the

frequencies are selected ranging from 100 MHz to 35 GHz. A validation check is performed before running the parasitic extractor. It checks for 3D Model boundaries, excitations, material overlaps and analysis setup. If the validation check fails, check for the errors and modify the appropriate material parameter or geometry. Some of the most common errors are with material overlaps and parametric setup. Once the validation check is complete, the parasitic extractor is executed and the results are obtained in a Touchstone file, which consists of RLGC values for DC and all the frequencies defined in the frequency setup. The Touchstone file can be given as an input for frequency dependent simulations in HSPICE.

3.2 Frequency dependency of TSV parasitics

TSV parasitics, particularly Resistance (R), Conductance (G) and Inductance (L) vary with frequency. The variation of resistance and conductance with frequency for a substrate conductivity of 100kS/m and the previously mentioned TSV dimensions are shown in Figure 3.4. It can be observed that the resistance of the TSV and the conductance through the dielectric increase with frequency. The increase of TSV resistance with frequency is due to the skin effect. As the frequency increases, the skin depth decreases thus reducing the overall cross section area for the currents to flow through the conductor (TSV). Since the current flowing through the conductor decreases, the resistance of the conductor increases. In other words, for a given current, the cross section area A decreases, thus increasing the resistance according to

$$R = \frac{\rho l}{A}$$

R – Resistance of the conductor

ρ - Resistivity of the conducting material

l - Length of the conductor

A – Area of cross section

The conductance per unit length mentioned is the leakage conductance and not the conductance of the TSV. This is measured in perpendicular direction to the TSV length. Consider a simple RLGC transmission line model as shown in Figure 3.3. As we double the length of the transmission line, the series resistance R of the conductor doubles. However the shunt resistance of the conductor is halved. As we double the length of the line there is more area through which the leakage current can flow, reducing the shunt resistance. In other words, shunt conductance doubles. Hence we can say that shunt resistance or the leakage resistance is nothing but the inverse of shunt conductance 'G'.

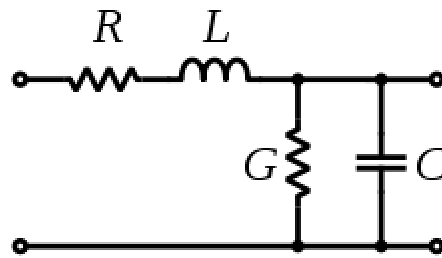

Figure 3.3 RLGC transmission line model

$$G = \frac{1}{R_{Leakage}}$$

The dielectric constant of a material is a complex quantity and is represented as

$\varepsilon_r = \varepsilon_r' - i\, \varepsilon_r''$ [34]

ε_r is the complex dielectric constant

$\varepsilon_r^{'}$ representing the real component

$\varepsilon_r^{''}$ representing the imaginary component

The angle of the vector with the real axis is called the loss angle δ.

$tan\ (\delta) = \varepsilon_r^{''} / \varepsilon_r^{'}$

$\varepsilon_r^{''} = \varepsilon_r^{'}\ tan\ (\delta)$

For the voltage $V = V_0\ exp(i\omega t)$, the current through the dielectric is given by

$I = C\ dV/dt = iC\omega V = i\varepsilon_r C_0 \omega V = i\ \varepsilon_r^{'} C_0 \omega V + \varepsilon_r^{''} C_0 \omega V$

In the above equation, the real part represents the loss and the imaginary part represents the capacitive current.

Now, $R_{Leakage} = V/Real(I) = V/\ (\varepsilon_r^{''} C_0 \omega V) = 1/\ (\omega\ C\ tan\ (\delta))$

Conductance $G = 1/R_{Leakage} = \omega\ C\ tan\ (\delta)$

Thus leakage conductance G increases with the frequency.

The inductance in a bundle is comprised of self and mutual inductance components. For a 3x3 bundle, mutual inductance between two TSVs varies with spacing.

Considering the arrangement of TSV bundle as shown in Figure 3.5, it can be observed that the TSV-0 is surrounded by a maximum of 8 TSVs. We denote the total mutual inductance by TSV-0 as Lm1. Similarly the total mutual inductance by the TSVs at 1, 3, 6 and 8 is denoted by Lm2 and by the TSVs 2, 4, 5 and 7 is denoted by Lm3. In

Figure 3.6, Ls represents the self inductance and Lm1, Lm2 and Lm3 represent the mutual inductances as discussed above.

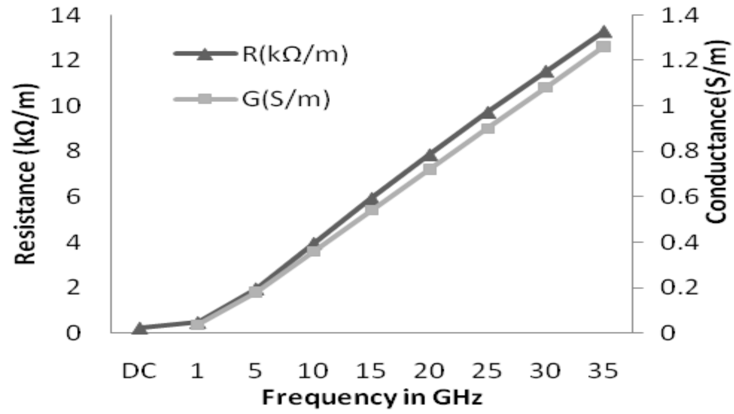

Figure 3.4 Linear dependency of R and G with frequency for σ=100kS/m.

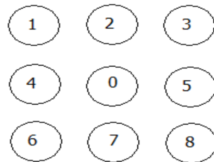

Figure 3.5 TSV configuration of a 3x3 bundle

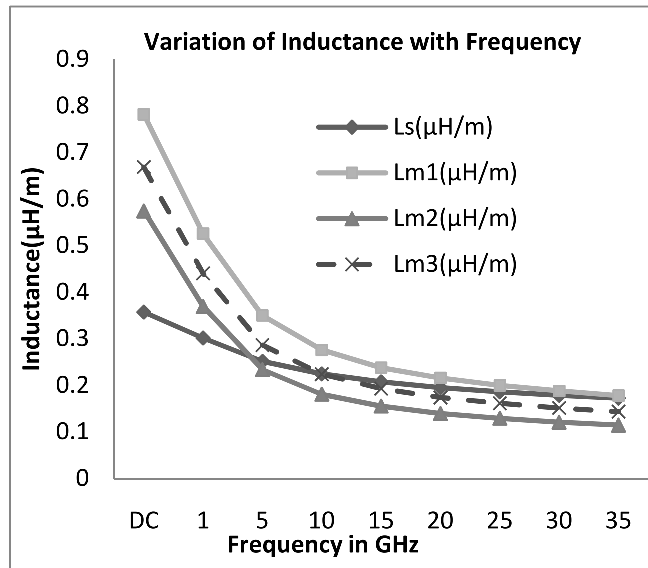

Figure 3.6 Inverse variation of L with frequency

At higher frequencies, the current inside the conductor decreases due to skin effect. Consider a conductor cross-section as shown in Figure 3.7. Total inductance is the sum of internal and external self inductance. As the frequency increases, the current re-distributes inside the conductor away from the center thus decreasing the number of internal field rings surrounding the current. This results in the reduction in internal inductance of the conducting rod, thus reducing the total inductance. This is observed in Figure 3.6 where the inductance values decrease with frequency.

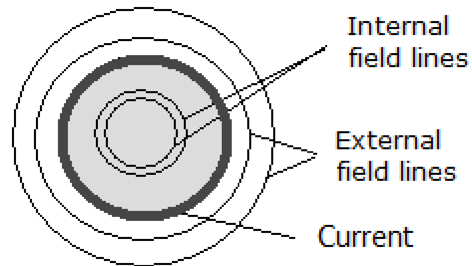

Figure 3.7 Magnetic field line rings surrounding solid conductor [34]

3.3 Skin effect and TSV resistance

The resistance of a conductor is evaluated using the formula

$$R = \frac{\rho l}{A}$$

R is the resistance of the conductor, ρ is the resistivity of the conducting material, l is the length of the conductor and A is the area of cross-section. Now let us consider a cylindrical TSV of radius r as shown in Figure 3.8.

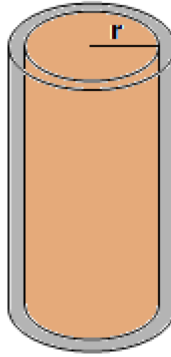

Figure 3.8 Cylindrical TSV with radius r surrounded by dielectric coating

The resistance of cylindrical TSV of length l and radius r as considered in Figure 3.8 is given by

$$R = \rho l / \pi r^2$$

Here the area is taken as the total cross-section area of the cylinder given by $A = \pi r^2$. This is true for evaluating DC resistance. However, the current distribution in a conductor is not uniform throughout its cross-section. At higher frequencies the current tends to travel along the outside of the conductor and this phenomenon is known as “Skin effect” i.e. the tendency of the current to flow on the skin (outer surface) of the conductor. As a result of this, the effective area through which the current can flow decreases resulting in increase in the resistance for higher frequencies.

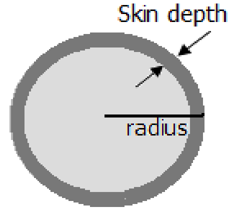

Figure 3.9 Skin effect in cylindrical conductor

The resistance of the interconnect also depends on the skin effect of the substrate depending on the substrate conductivity of silicon [36][37][38]. For substrates with very high conductivity, the skin depth will be low and results in skin effect due to substrate. This results in large variations in current density and current distribution in substrate and leads to variations in interconnect resistance for high frequencies [38]. In substrates with high conductivity, the effective resistance of the interconnect at high frequencies will increase due to both substrate skin effect and the interconnect skin effect. However for substrates with low substrate conductivity, the impact of substrate skin effect is little as the substrate skin depth increases with reduction in substrate conductivity. The skin depth is given by

$$\delta_s = \sqrt{2\rho / 2\pi f \mu_0 \mu_R}$$

δ_s is the skin depth, f is the frequency, ρ is the resistivity of the material and μ_0 is the permeability of free space and μ_R is the relative permeability of the material.

For substrates with low conductivity, the dominant factor is the conductor skin effect. As discussed earlier, the resistance of a conductor varies with frequency due to skin effect. For hand calculations, simple expression for skin depth is considered for understanding

its impact on resistance. Once the skin depth is calculated, we can obtain the resistance using the formula

$$R = \frac{\rho l}{A} \text{ and } A = \pi r^2 - \pi (r - \delta_s)^2$$

The resistance obtained using hand calculation and those obtained from Q3D are shown in Figure 3.10.

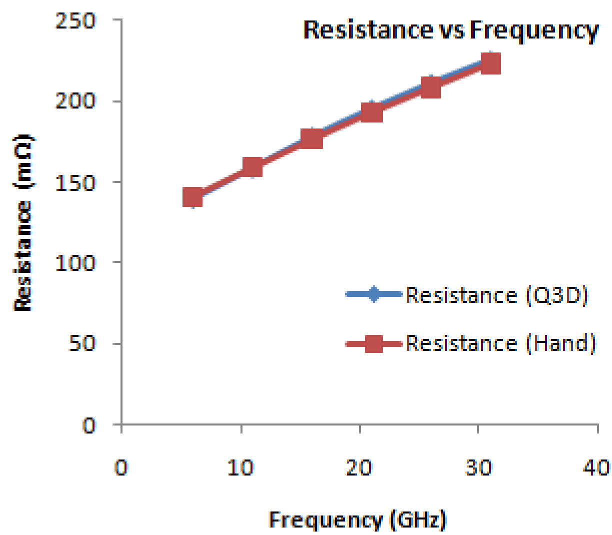

Figure 3.10 Variation of resistance with frequency

3.4 Mutual Inductance and Coupling Capacitance in 3x3 TSV Bundle

In a 3x3 TSV bundle, each TSV will have coupling from all other TSVs. Considering the TSV bundle arrangement shown in Figure 3.5, the total mutual inductance of the center TSV (numbered 0) is

$Lm1 = L_{01} + L_{02} + L_{03} + L_{04} + L_{05} + L_{06} + L_{07} + L_{08}$

Due to symmetry,

$L_{01} = L_{03} = L_{06} = L_{08}$

$L_{02} = L_{04} = L_{05} = L_{07}$

Similarly the total mutual inductance by TSV 1, TSV 3, TSV 6 and TSV 8 is the same and it is equal to

$Lm2 = L_{12} + L_{13} + L_{14} + L_{15} + L_{16} + L_{17} + L_{18} + L_{10}$ for TSV 1

Due to symmetry,

$L_{13} = L_{16}$; $L_{12} = L_{14}$; $L_{15} = L_{17}$

The total mutual inductance by TSV 2, TSV 4, TSV 5 and TSV 7 is the same and is given by

$Lm3 = L_{20} + L_{21} + L_{23} + L_{24} + L_{25} + L_{26} + L_{27} + L_{28}$

Due to symmetry,

$L_{20} = L_{21} = L_{23}$

$L_{24} = L_{25}$ and $L_{26} = L_{28}$

Similar to inductance, the coupling capacitance depends on the location of the TSVs.

The total coupling capacitance of the center TSV is given by

$Cc1 = C_{01} + C_{02} + C_{03} + C_{04} + C_{05} + C_{06} + C_{07} + C_{08}$

Due to symmetry, we have

$C_{01} = C_{03} = C_{06} = C_{08}$ and $C_{02} = C_{04} = C_{05} = C_{07}$

Similarly, the total coupling capacitance of each of TSV 1, TSV 3, TSV 6 and TSV 8 is the same and it is equal to

$Cc2 = C_{12} + C_{13} + C_{14} + C_{15} + C_{16} + C_{17} + C_{18} + C_{10}$ for TSV 1

Due to symmetry,

$C_{13} = C_{16}$; $C_{12} = C_{14}$; $C_{15} = C_{17}$

The total coupling capacitance of each of TSV 2, TSV 4, TSV 5 and TSV 7 is the same and is given by

$Cc3 = C_{20} + C_{21} + C_{23} + C_{24} + C_{25} + C_{26} + C_{27} + C_{28}$

Due to symmetry,

$C_{20} = C_{21} = C_{23}$

$C_{24} = C_{25}$ and $C_{26} = C_{28}$

The extracted values from the field solver at DC and 2GHz frequency are shown in Table 3.1. Self Capacitance and Self Inductance values are denoted under Cs and Ls. As discussed earlier, Lm1, Lm2 and Lm3 represent the mutual inductance and Cc1, Cc2 and Cc3 represent coupling capacitance experienced by different TSVs depending on their location.

Table 3.1 Electrical parasitics at DC and 2 GHz frequency

Freq.	**R (mΩ)**	**Ls (pH)**	**Lm1(pH)**	**Lm2(pH)**	**Lm3 (pH)**	**Cs (fF)**	**Cc1 (fF)**	**Cc2 (fF)**	**Cc3 (fF)**
DC	4.88	7.14	15.648	11.515	13.364	116.34	0.104	0.076	0.049
2GHz	16.38	5.66	7.768	5.486	6.536	116.34	0.104	0.076	0.049

From Table 3.1, it can be observed that the coupling capacitance is less compared to self capacitance. This is due to higher spacing between the TSVs and the substrate acting as a shield. Total mutual inductance values are comparable to self inductance values.

3.5 Circuit model

In this section a simplified circuit model is presented. The simulations are carried out to check the accuracy of the simplified circuit model with that of the full circuit model obtained from the Q3D extractor. Consider a simple 2x1 structure (2 pair of TSVs) as shown in Figure 3.11. The TSV radius is 5µm and length 25µm. Its equivalent circuit is shown in Figure 3.12.

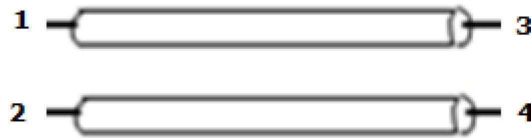

Figure 3.11 2x1 TSV structure

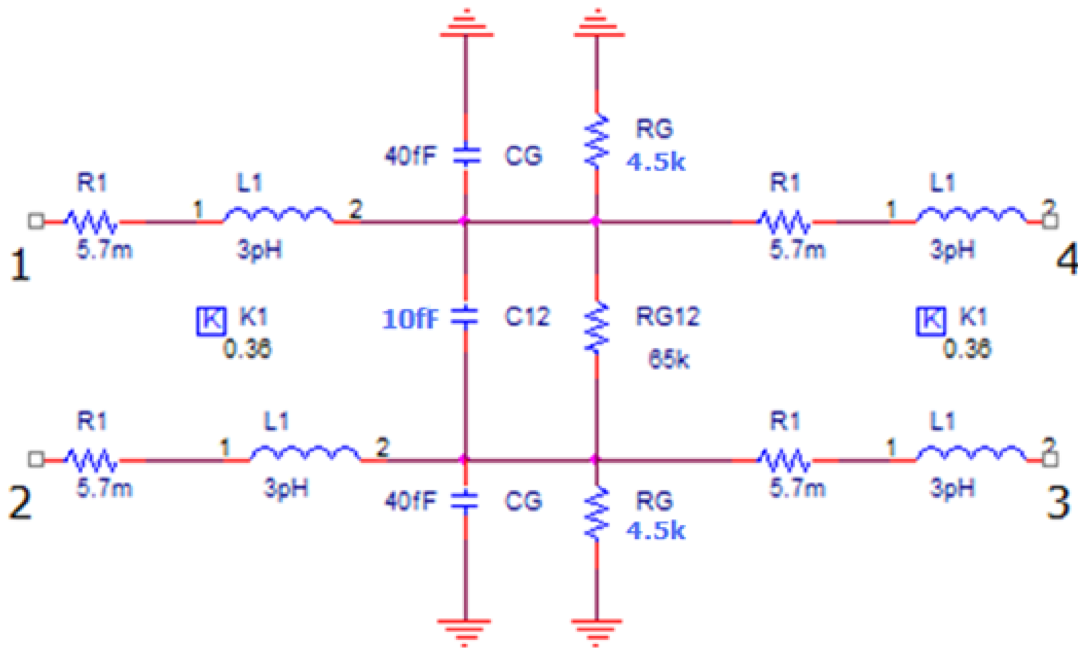

Figure 3.12 Equivalent circuit of 2x1 TSV structure

Simulations are carried out to check the accuracy of the simplified RLC equivalent circuit compared to the full circuit model. The detection of the signal at the receiver circuit depends on the eye opening of the signal at the receiver. Peak to peak voltage of the noise indicates the distortion in the eye opening and hence chosen as a metric. For a 2x1 structure as shown in Figure 3.11, port 1 is given a rising input and the peak to peak voltage at the outputs 3 and 4 are obtained. A similar analysis is carried for 3x1 structure.

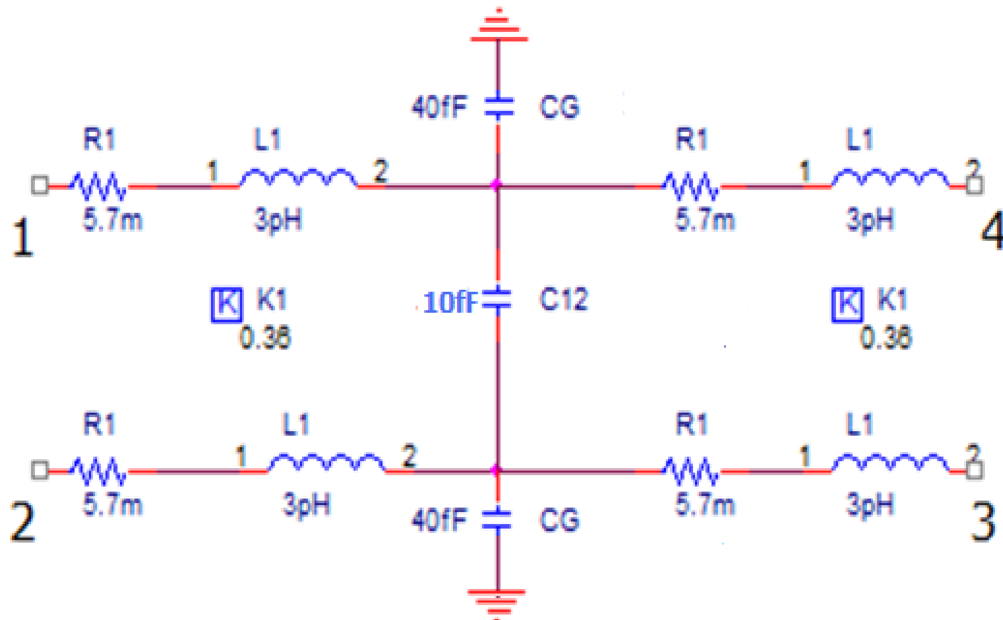

Figure 3.13 Simplified RLC equivalent circuit of 2x1 TSV structure

The peak-peak noise voltages using RLC equivalent circuit model and full circuit model are shown in Table 3.2. It can be observed that the results from RLC circuit model are close to full circuit model.

Table 3.2 Peak-peak voltage using full model and RLC model

Output Node	$V_{(p-p)}$ full model (V)	$V_{(p-p)}$ RLC model (V)
2x1 aggressor	0.068	0.067
2x1 victim	0.061	0.062
3x1 aggressor	0.054	0.057
3x1 victim-1	0.059	0.060
3x1 victim-2	0.043	0.047

3.6 Crosstalk

In this section, crosstalk in 3x1 and 3x3 structures is examined. Simulation setup for crosstalk analysis for 2D interconnects is suggested in [35]. The simulation setup for crosstalk analysis suggested in [35] is shown in Figure 3.14. Figure 3.15 shows the equivalent circuit model. The inverter on the driver side is modeled as the resistance Rtr and the inverter on the receiver is modeled as a capacitive load C_L as shown in Figure 3.15.

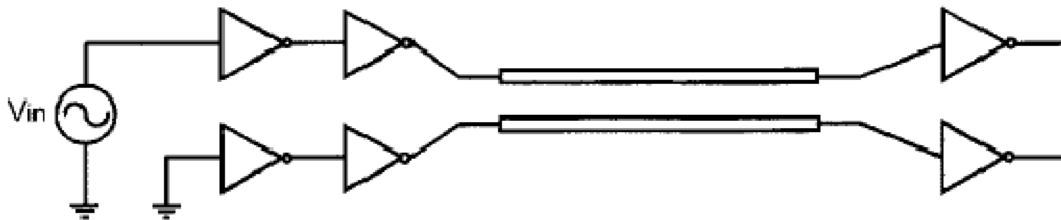

Figure 3.14 Simulation setup for analyzing crosstalk [35]

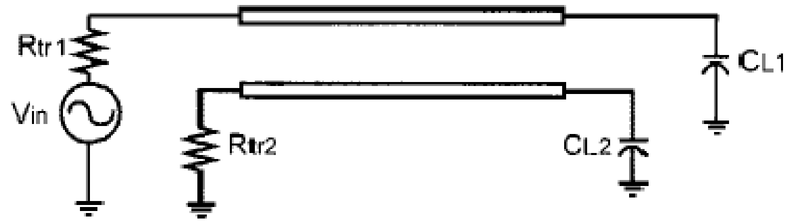

Figure 3.15 Circuit model for crosstalk analysis [35]

In this work, we consider 3x1 and 3x3 structures for crosstalk analysis. For each of these two structures we consider two cases – static case and switching case. By static case we mean that only one of the TSVs will have a switching signal and rest of the TSVs are given a static input. In switching case, we have center TSV switching in opposite direction relative to rest of the TSVs. To understand the crosstalk in interconnects, similar simulation setup as in Figure 3.14 is considered. Simulation setup for 3x1 structure for static case is shown in Figure 3.16. In Figure 3.16, on the input side we have one node with a rising input and the other two nodes are given a "ground" input. The simulation results are shown in Figure 4.

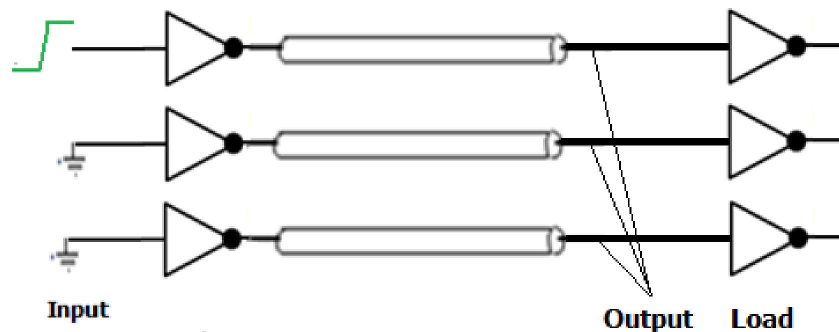

Figure 3.16 Simulation setup for crosstalk estimation in 3x1 (static case)

Simulation results are shown in Figure 3.17. From Figure 3.17, it can be observed that the peak to peak voltage of noise induced due to the aggressor on the other TSVs

decreases as we move away from it. This is due to the reduction in coupling between the TSVs. Assuming 3 TSVs arranged as 3x1 (3 parallel TSVs), the coupling between 1 and 2 will be high compared to the coupling between 1 and 3. This is both due to the increase in spacing as well as the shielding provided by the middle TSV.

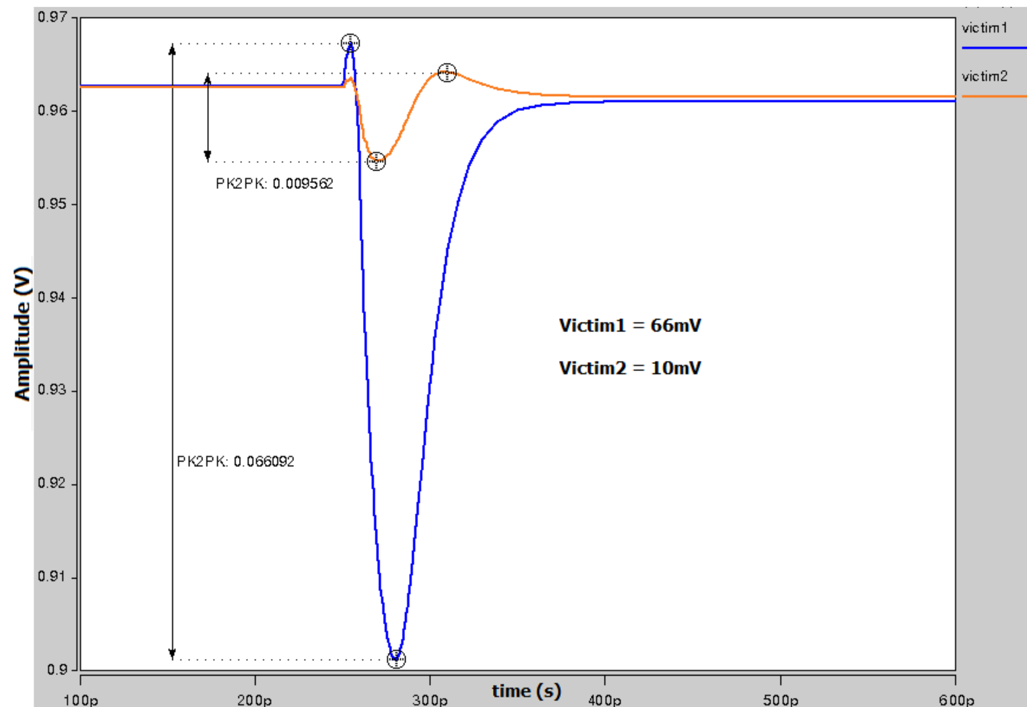

Figure 3.17 Waveforms showing the crosstalk in 3x1 (static case)

However, when all the TSVs are used for signaling, the worst case switching scenario occurs when the center TSV switches in the opposite direction relative to rest of the TSVs. Now let us consider this scenario shown in Figure 3.18 to analyze the crosstalk in worst case switching.

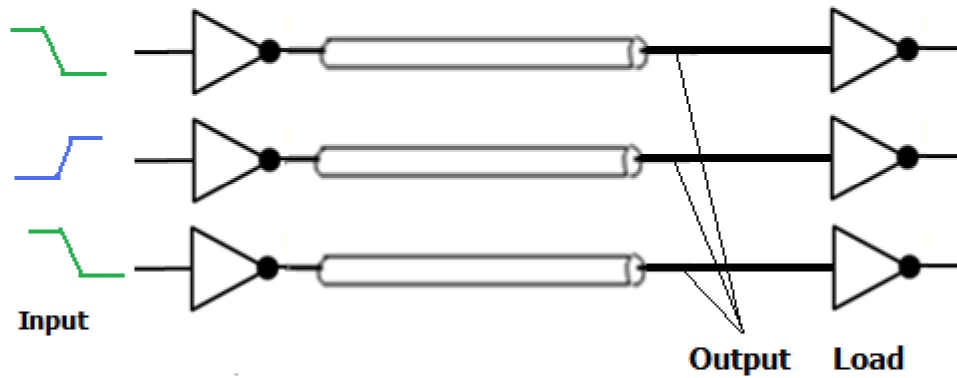

Figure 3.18 Simulation setup for 3x1 with switching inputs

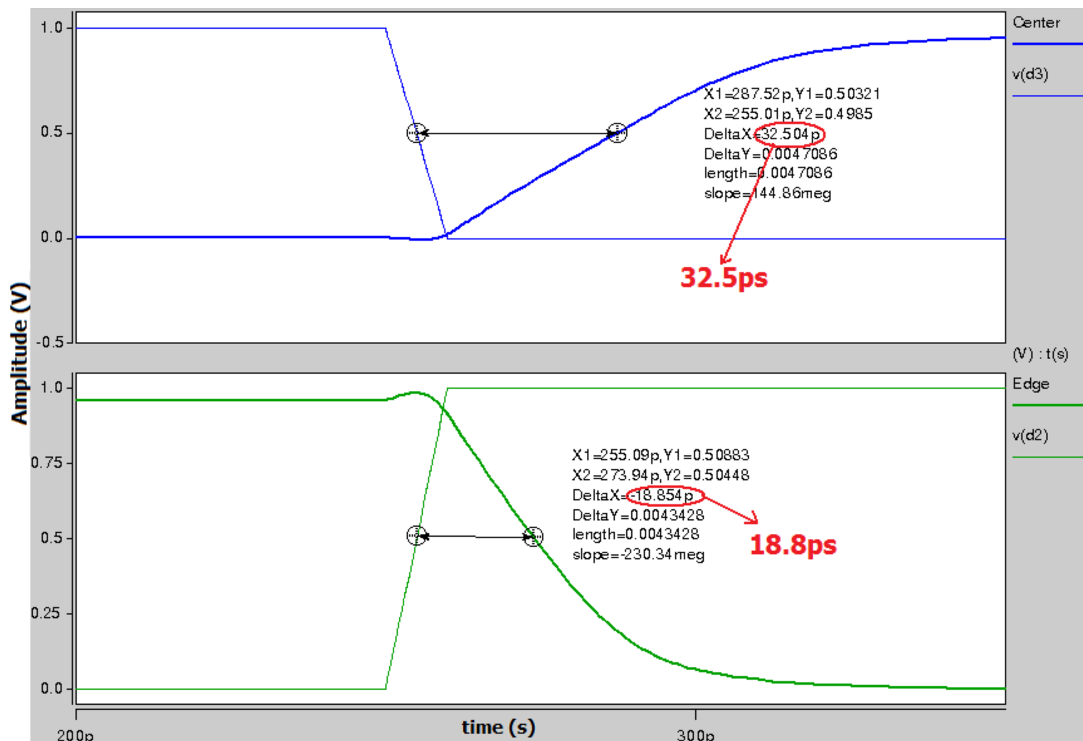

Figure 3.19 Waveforms showing impact of crosstalk in 3x1 (switching case)

The simulation results for worst case switching in 3x1 structure is shown in Figure 3.19. In switching case all the TSVs have a changing input. However the propagation delay depends on the relative switching between the conductor and its neighboring nodes. For 3x1 switching case, the center TSV will suffer more due to

crosstalk. This is because it has two neighbors switching in the opposite direction resulting in change in voltage of 4VDD. For the edge TSVs, there is only one switching neighbor resulting in 2VDD change in the voltage. From the simulation results it can be observed that the center TSV has higher delay compared to edge TSV.

Now we will discuss the crosstalk in 3x3 TSV structure. For static case, we will give a rising input to one of the TSV drivers and the rest of the drivers are "grounded" at the input. Depending on the location of the TSV with respect to aggressor node, the noise due to crosstalk varies. 3x3 TSV structure indicating the aggressor and victim TSV nodes is shown in Figure 3.20. TSVs located orthogonal to the switching TSV are named as orthogonal1 and orthogonal2, orthogonal1 being the TSV immediately orthogonal to the switching TSV and orthogonal2 being the TSV next to orthogonal1. TSVs that are diagonal to switching TSV are named as diagonal1, diagonal2 and diagonal3 as mentioned in Figure 3.20.

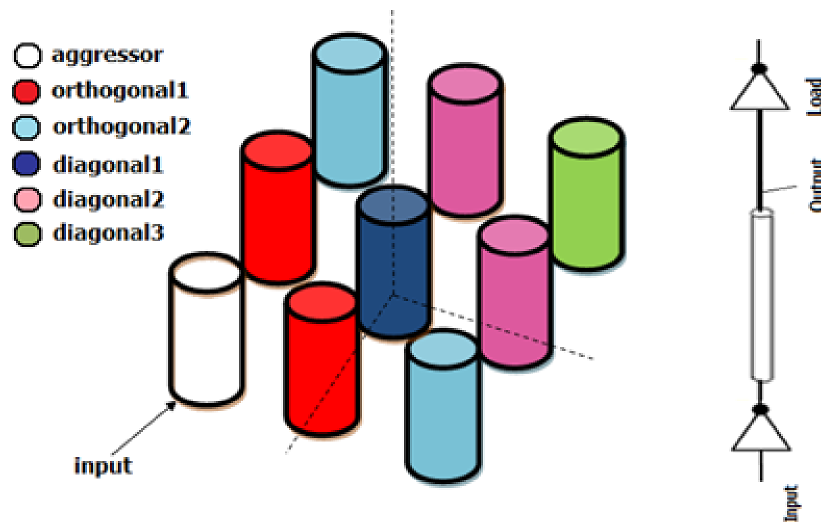

Figure 3.20 Simulation structure for cross talk in 3x3 (static)

Simulation results are shown in Figure 3.21. In a 3x3 TSV structure, crosstalk noise depends on the location of victim TSV relative to aggressor. The TSVs that are immediately close to aggressor suffer more compared to rest of the TSVs. It can be noticed that the immediate orthogonal TSVs (in red) and immediate diagonal TSV (in dark blue) will have higher crosstalk noise compared to rest of the TSVs. The crosstalk on non immediate neighbors is less due to increased spacing as well as shielding by the immediate neighbors.

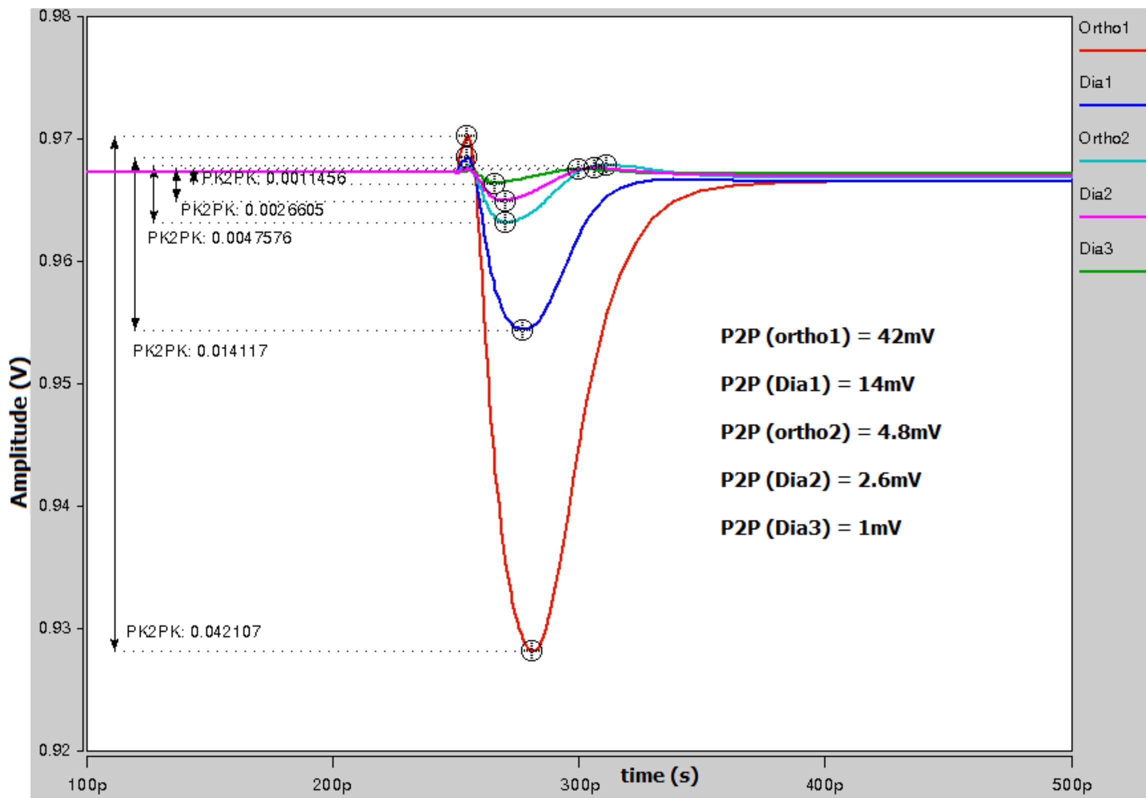

Figure 3.21 Crosstalk in 3x3 structure (static)

Now we will consider the switching case in 3x3 structure. As discussed earlier, when all the TSVs in a 3x3 bundle are used for signaling, we will have worst case noise when the center TSV switches in the opposite direction relative to rest of the TSVs. Let

us call this the worst case switching scenario and simulation setup is shown in Figure 3.22. The center TSV and rest of the TSVs switch in opposite directions. All the TSVs surrounding the center TSV can be categorized into orthogonal and diagonal TSVs depending on their relative location with respect to the center TSV in the bundle. Simulation results are shown in Figure 3.23.

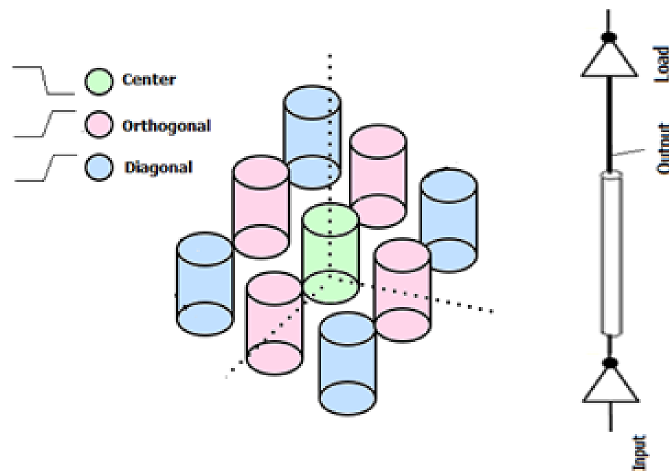

Figure 3.22 Simulation setup for worst case switching in 3x3

From Figure 3.23 it can be observed that the center TSV has the maximum delay due to crosstalk. The delay through the orthogonal TSV is 14.1ps and the delay through the diagonal TSV is 15.6ps. In this chapter, we dealt with TSV parasitic extraction, circuit model and crosstalk in 3x1 and 3x3 structures. Signaling techniques and their performance for different TSV radii will be discussed in Chapter 4.

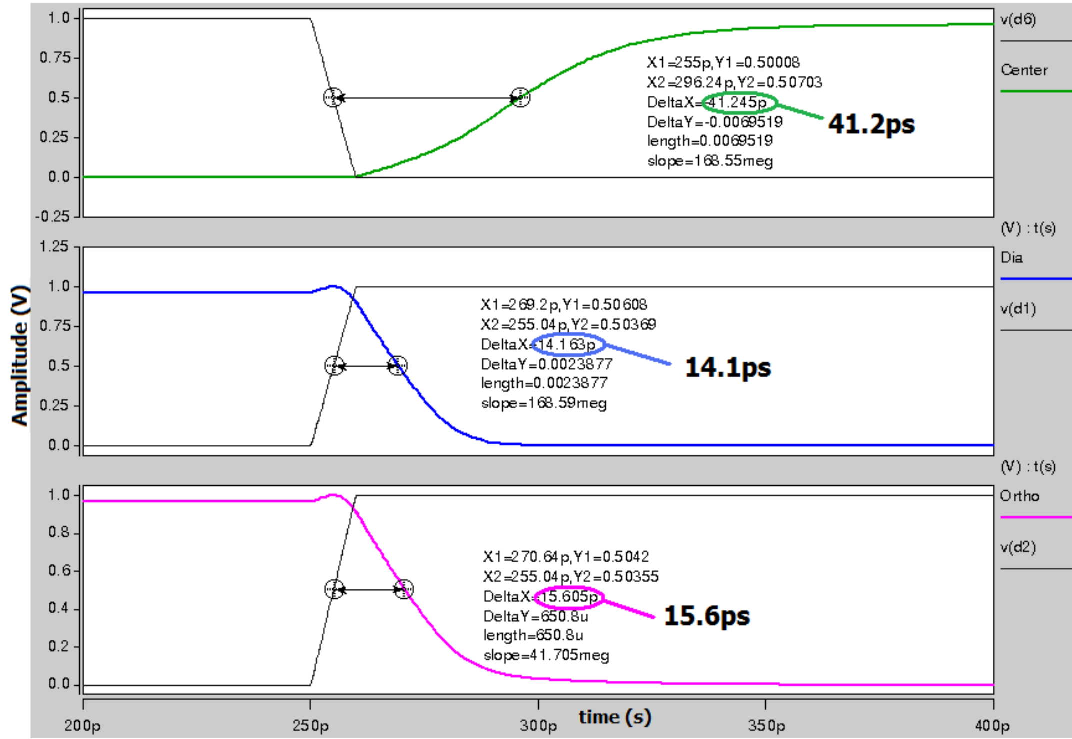

Figure 3.23 Crosstalk in 3x3 (switching)

CHAPTER 4

SIGNALING ON THROUGH SILICON VIA BUNDLES

Signaling techniques play a crucial role in determining overall performance of a digital system. A typical signalling system consists of a transmitter/driver, channel and a receiver. Depending on the electrical representation of the data, signaling techniques are classified into voltage mode/high impedance mode and current mode/ low impedance mode.

In voltage mode, the signal is represented by the voltage levels, whereas the signal is represented by the currents in current mode. In general, both voltage and current mode primarily depend on the termination at the receiver. If the receiver used is a low impedance termination, then it is more suitable for current mode transmission, since all the current can flow into the receiver as opposed to flowing into ground through a low impedance path. If the receiver is a high impedance node, then voltage mode is suitable since all the voltage can be applied at that node. Based on the number of interconnects used for signal transmission, signaling techniques can be classified into two types.

a) Single ended signaling technique

b) Differential signaling technique

In single ended techniques, there is a common reference for all the signals at both transmitter and the receiver. At the receiver side, the signal is compared with this common reference to determine whether the transmitted bit is 0 or 1. In differential signaling technique, each signal requires two interconnects. At the driver side, both signal

and its complement are transmitted. At the receiver side, these two signals are compared to identify the transmitted bit.

In this chapter we present various signaling techniques for TSV based 3D ICs. Single ended and differential signaling techniques are explored. Maximum data rates and energy/bit for each of the signaling techniques are obtained. All the driver and receiver circuits are designed using 45nm CMOS technology using NCSU PDK. As TSV parasitics vary with its radius, we extracted the parasitics for TSV radii ranging from 1μm to 15μm and maximum data rates are determined for each of the signaling techniques determined above.

4.1 Single Ended Techniques

4.4.1 Voltage Mode Signaling

Voltage Mode signaling is also called high impedance mode signaling due to the high input impedance of the receiver circuit. The driver and receiver circuit in voltage mode signaling can be realized using a simple inverter. Some of the crucial parameters to be considered while designing driver and receiver circuits are

- Rise and Fall times
- Maximum Data rate
- Power consumption

Rise and fall times at the output are important for power and performance issues. For a simple inverter circuit, during the transition from 0 to 1 or 1 to 0, for certain duration both NMOS and PMOS are ON. During this period, there is a direct current path

from VDD to ground which contributes to dynamic leakage power. In general, longer rise and fall times reduce the overall performance. One way to obtain sharp rise and fall times is to increase the drive strength. Hence, it is important to determine the drive strength to increase the data rate. The rise and fall times are determined by the sizing of pull up and pull down networks. For voltage mode signaling with inverters as drivers and receivers, the rise and fall times are determined by the P/N ratio of the inverter and the absolute widths of the transistors. Based on the simulation results, the P/N ratio for equal rise and fall times is found to be 3.5. As the size of the inverter increases, its drive strength increases. However, it also increases the load capacitance due to the driver. After certain point, the reduction in delay due to the increase in drive strength is overcome by the increase in the capacitance. Based on this, simulations are carried out to obtain the absolute widths with performance as primary objective.

The maximum data rate for a particular signaling scheme depends on load capacitance of the driver, interconnect capacitance and the input capacitance of the load. For voltage mode signaling, a unit inverter driving a Fan Out of 4 (FO4) load is considered as the receiver. The parasitics for 3x3 TSV bundle are obtained from Q3D extractor and provided as input touchstone file for HSPICE simulation. Simulations are performed to obtain the maximum datarate that can be achieved using Single Ended Voltage Mode signaling (SEVM). Based on the simulations for minimum delay each TSV of the 3x3 bundle is driven by the 64 x inverter. All the TSVs in a bundle are driven in the same way. The simulation setup for one of the TSVs in 3x3 bundles for SEVM is shown in Figure 4.1.

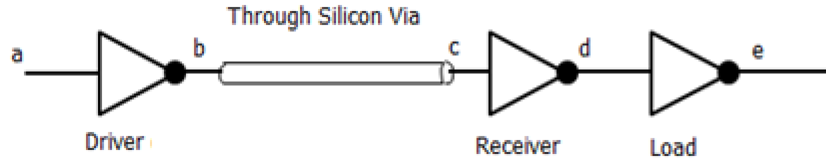

Figure 4.1 SEVM signaling simulation setup for one of the TSVs [39]

The center TSV will experience the maximum coupling in the bundle. Hence, all the simulation results are taken at the nodes of the center TSV. Simulations are performed in HSPICE with $2^7 - 1$ Pseudo Random Bit Sequence (PRBS) as inputs. The eye diagrams are plotted at the output of the 1x receiver, *node'd'* in Figure 4.1. A rise and fall time of 10ps is given at the input. Targeting an eye height of 60% of VDD as considered in [26], the maximum data rate that can be supported by voltage mode signaling for particular TSV radius is determined. For a TSV radius of 10µm, the maximum data rate is found to be 21.7 GBPS. The eye diagram for voltage mode signaling at 21.7 GBPS is shown in Figure 4.2.

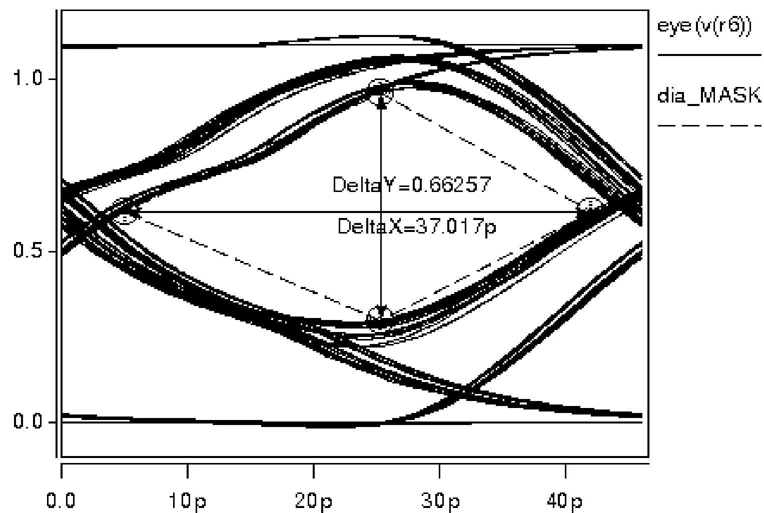

Figure 4.2 Eye Diagram at 21.7 GBPS for SEVM signaling[39]

4.4.2 Current Mode Signaling

In this section, the current mode signaling scheme is designed and analyzed. Current mode signaling is also called low impedance mode signaling due to the low input impedance of the receiver circuit. A simple inverter circuit cannot be used as a receiver for current mode signaling due to high input impedance offered by the PMOS and NMOS gate terminals. A simple self biased inverter as shown in Figure 4.3 can be used as a receiver.

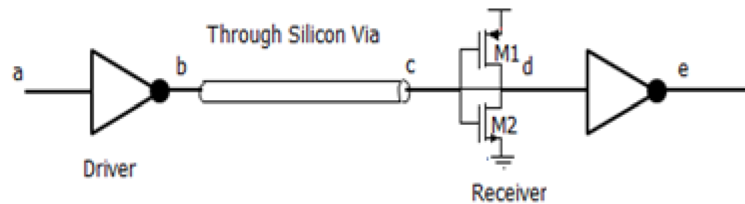

Figure 4.3 Simulation setup for SECM1 [39]

The simulation setup is similar to that of voltage mode except the receiver circuit, which is mainly a low impedance node. Let us call this circuit as Current Mode Receiver 1 (CMR1) and the signaling technique, Single Ended Current Mode1 (SECM1). The self biased inverter receiver shown in Figure 4.3 has a low input impedance. The drains of the transistors have high impedance (rd). However the total impedance is reduced due to feedback. The input impedance is given by $1/\ \{(gm_1+gm_2+\ (1/rd_1)\ +\ (1/rd_2)\}$.Voltage swing at the receiver in current mode signaling can be less than VDD (full swing). This provides the performance improvement. Considering the CMR1, the sizing of M1 and M2 plays a crucial role in determining the signal swing at *node 'c' or node 'd'* (as both are connected directly). Transistors M1 and M2 act like active load resistors. As the size

of M1 and M2 transistors increases, the signal swings decreases thus increasing the speed. But this improvement in speed gradually decreases and the link fails once the signal levels are too low to switch the inverter following *node'd'*. From simulation results for maximum speed, the size of M1 and M2 are chosen to be 64x unit size at 45nm CMOS technology. Similar to voltage mode simulations, the inputs to the 3x3 TSV bundle are provided by the $2^7 - 1$ PRBS with rise and fall times of 10ps. Considering 60% eye height as a criteria, the maximum data rate for TSV radius of 10μm is found to be 32.2 GBPS for CMR1. The eye diagram at 32.2 GBPS is shown in Figure 4.4.

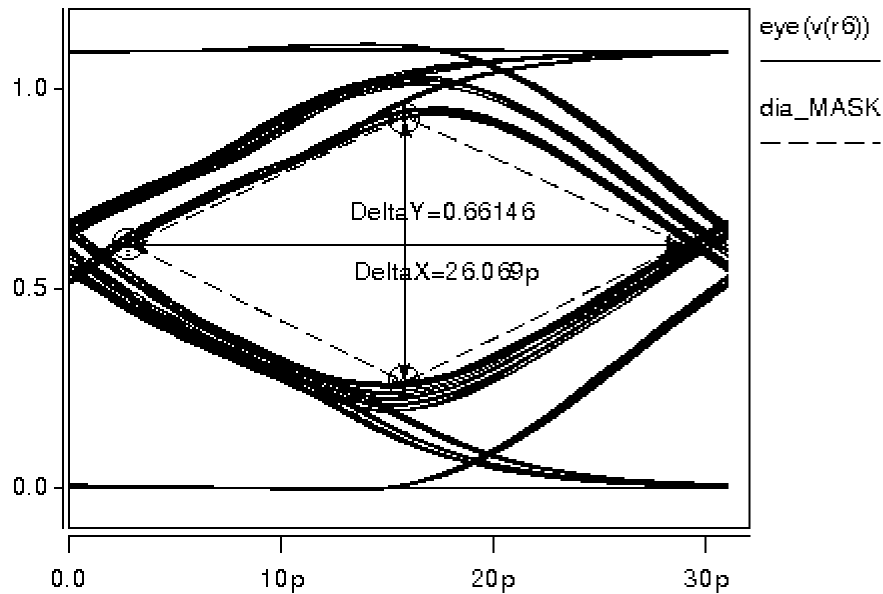

Figure 4.4 Eye Diagram at 32.2 GBPS for SECM1 signaling

An improvement to the receiver circuit of CMR1 can be made by adding an NMOS transistor between the nodes 'c' and 'd', as shown in Figure 4.5. This circuit is introduced in [40] where the signaling mode switches from current mode to voltage mode depending on whether this transistor is switched on or off, which in turn depends on whether there is a transition in the incoming data signal. In [40], the gate voltage of M3

varies depending on the input data and its transition, and is primarily used as a part of the repeater circuit. In this work, we bias it to a fixed voltage to operate at a maximum gain. This increased gain also helps in reduction in the overall impedance between input and output, as the total impedance is now divided by the factor of (gain+1) due to Miller Effect. The input impedance is given by $(rd_3+A)/(1+A(gm_1+gm_2))$ where $A = (rd_1+rd_2)\{1+rd_3(gm_3+gmb_3)\}$. The sizing of the feedback transistor plays a significant role in determining the performance of the circuit. As the transistor size increases, the gain increases and at the same time, the drain and source capacitance of M3 at the input and output nodes increases. Hence, the improvement in performance with increase in the transistor size gradually decreases due to the increasing capacitance.

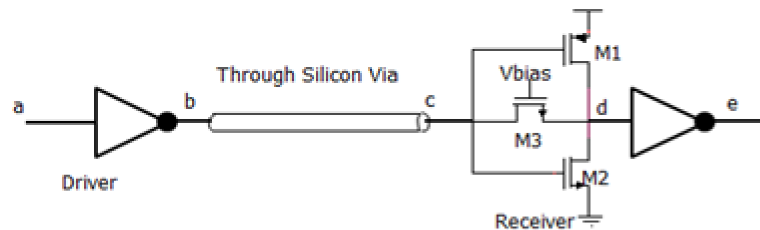

Figure 4.5 Simulation setup for SECM2 signaling [39]

Similar to earlier simulations, the input is a $2^7 - 1$ PRBS with rise and fall times of 10ps. The maximum data rate for a TSV radius of 10μm is found to be 36.6 GBPS. The eye diagram at 36.6 GBPS is shown in Figure 4.6. However it can be observed that this circuit is highly affected by Inter Symbol Interference (ISI). From the eye diagram it can be observed that there are “sub-eyes” which are misaligned. This can be handled by adding an equalization circuit at the driver or receiver.

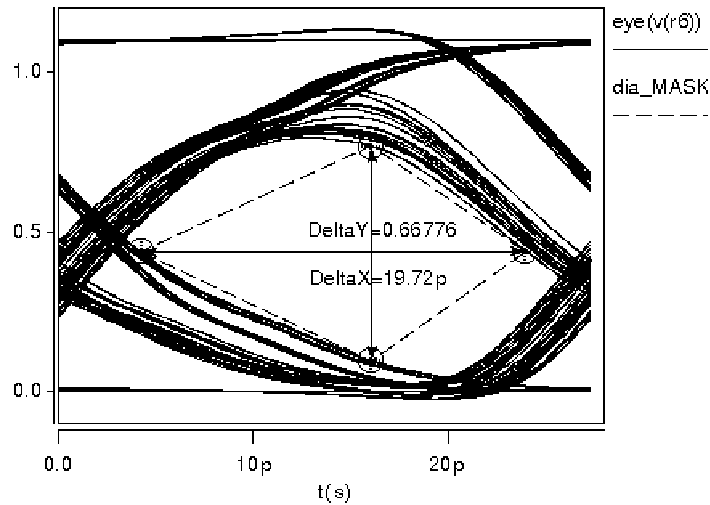

Figure 4.6 Eye Diagram at 36.6 GBPS for SECM2 signaling

4.2 Differential technique

The choice of a signaling technique depends on performance, power and robustness. A single ended signaling scheme which considers VDD and VSS as high and low voltages, respectively, suffers significantly due to common-mode noise. In differential signaling, each signal is represented as a pair of complementary signals (V+ and V-). At the receiver end, both the signals are compared to obtain the transmitted bit. The primary drawback of single ended signaling is its vulnerability to common mode noise.

In differential signaling, the receiver takes the difference of the two complementary signals, thus mitigating the common mode noise. Also the maximum voltage swing in differential technique is twice that of single ended signaling. This helps in providing higher noise margins compared to single ended signaling. In other words, it allows lower voltage swings for similar noise margins. Dynamic power has the quadratic

dependency on the voltage level. As differential technique requires lower voltage swings, significant savings in dynamic power can be obtained with this technique. Lower voltage swings can provide higher data rates as the load capacitance need not charge or discharge for complete supply swing.

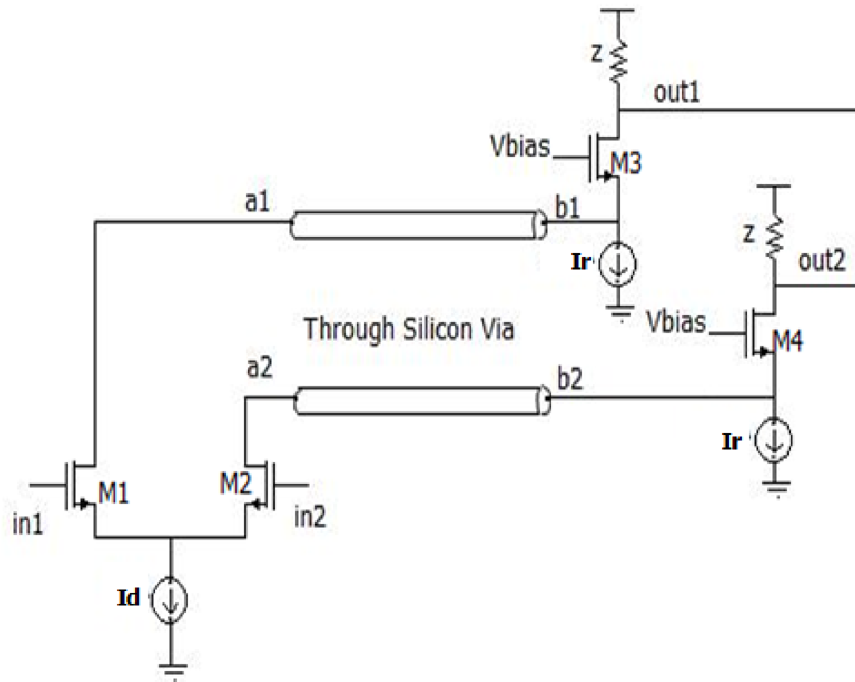

Figure 4.7 Schematic for Differential Signaling technique [39]

In this work, a differential signaling scheme as shown in Figure 4.7 is considered. The differential inputs are applied to the gates of the transistors M1 and M2, which are pinned to carry a total current of 1mA with the help of a tail current source. At the receiver side, a simple common gate transistor with a load resistor is used for each leg. Depending on the differential inputs, the current in one of the legs dominates over the other, resulting in differential outputs. The bias voltage is applied to operate the transistors in saturation region. Such a receiver configuration with a simple common

source driver is explained in [41]. Simulations are performed using $2^7 - 1$ PRBS inputs and the eye diagram at 31 GBPS is shown in Figure 4.8. The differential voltage at the nodes out1 and out2 is shown in Figure 4.8.

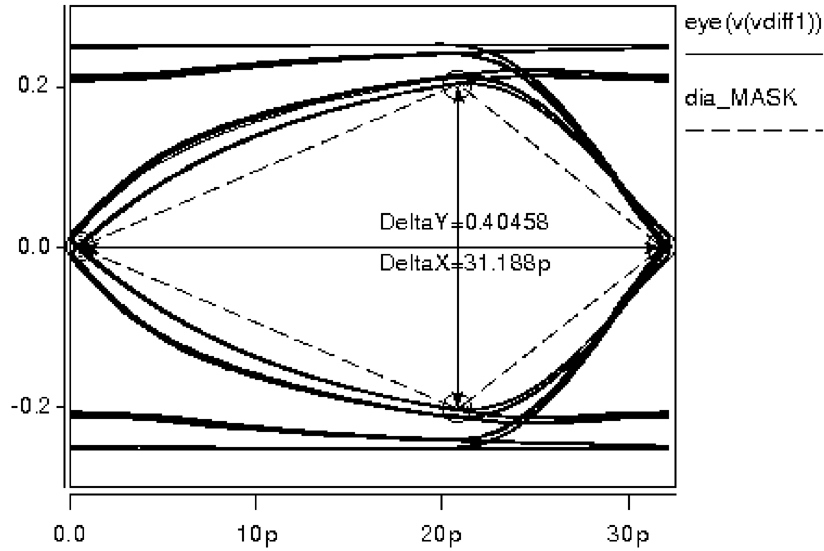

Figure 4.8 Differential output eye diagram at 31 GBPS

It was observed that the Inter Symbol Interference (ISI) is dominating and simple driver equalization with one bit emphasis circuit can significantly improve the signal quality. A one bit emphasis circuit configuration as explained in [42] is used to improve the signal quality to obtain an eye opening as shown in Figure 4.8. The configuration mentioned in [42] is shown in Figure 4.9. It can be observed that for the first signal transition both the current sources will be ‘on’ and for consecutive ‘1’s the current is steered from one source into the other.

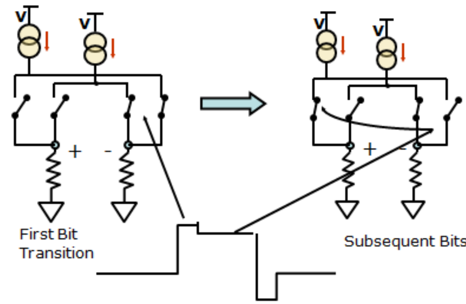

Figure 4.9 One-bit emphasis circuit [42]

4.3 Energy/bit comparison of signaling techniques

The energy/bit is an important metric to estimate the energy consumption of the signaling scheme. For energy/bit comparison, all the signaling techniques are given an input of 10 Gbps to have a common (iso) data rate comparison. Energy/bit is evaluated using average power obtained from the HSPICE simulation. HSPICE gives the total power consumed by all the 9 TSVs averaged to bit time. The energy consumed by all the 9 TSVs is obtained by multiplying the power for 9 TSVs with bit time. For Single Ended Voltage Mode signaling, transmitting each bit requires only one TSV. So energy/bit is estimated by dividing the total energy by 9. For differential signaling with 4x4 structure, all the 16 TSVs are used for sending 8 signals. Hence, the total energy/bit is divided by 8.

The primary drawback of differential signaling is that it requires 2N interconnects for transferring N signals. But single ended schemes require only N interconnects. From Table 4.1, it can be observed that SECM2 requires the least energy for transmitting the same number of bits at 10 Gbps. It can be observed that differential signaling requires the energy close to SECM1 signaling for 10 Gbps input.

Table 4.1 Energy/bit for various signaling techniques at 10 GBPS

Signaling technique	Energy/bit (fJ)
SEVM	1.715
SECM1	1.348
SECM2	0.981
DCM	1.282

4.4 Performance of signaling techniques for different TSV radius

The electrical parasitics of a TSV are dependent on its radius. Depending on the application, different research groups (both academia and industry) use a different TSV radius. To understand the performance of different signaling techniques across different TSV radii we extracted electrical parasitics of TSVs for radius ranging from 1μm to 15μm. The following section will discuss the variation of TSV electrical parasitics with radius. The arrangement of a TSV pair for parasitic extraction is shown in Figure 4.10.

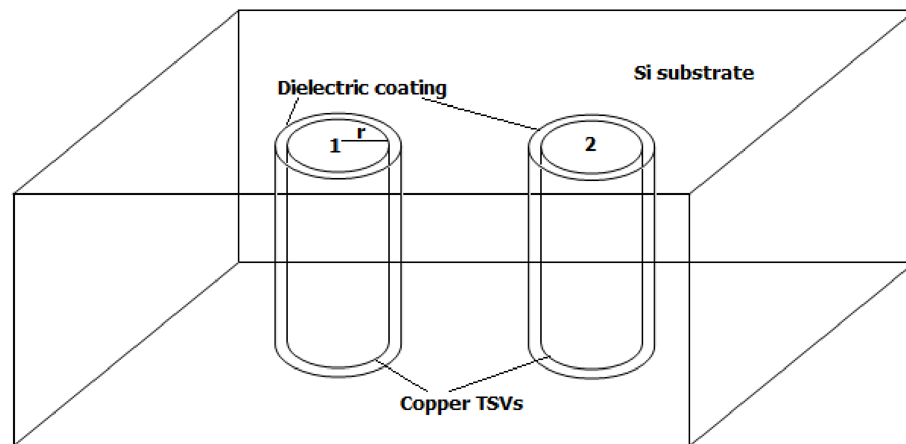

Figure 4.10 A pair of TSVs in a silicon substrate

4.4.1 Variation of resistance, inductance and capacitance with TSV radius

The resistance of a material is inversely proportional to its cross-sectional area. As the radius of the TSV increases, its cross-sectional area increases in a quadratic manner, thus reducing the resistance. The resistance of a TSV is given by

$$R = \rho * \frac{l}{A}$$

R is the resistance of the conductor, ρ is the resistivity of the material, l is the length of the conductor and A is its area of cross-section of a cylindrical conductor. The area of cross-section is proportional to the square of the radius. In Figure 4.11, the variation of resistance of TSV with radius is shown.

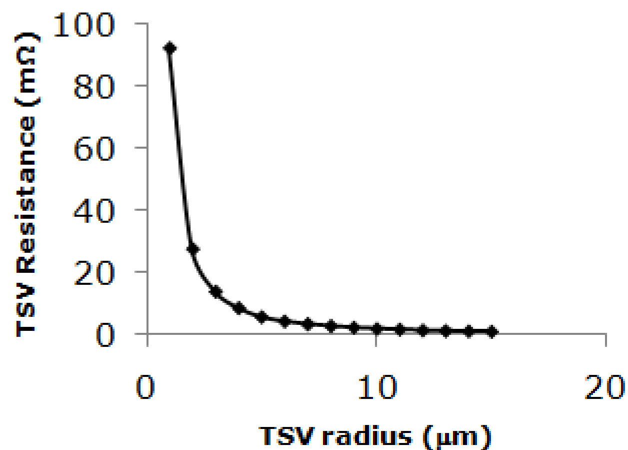

Figure 4.11 Variation of resistance with TSV radius

Inductance of a TSV also varies inversely with TSV radius. As the radius of TSV increases, the cross section area increases. This results in spreading of the current, thus decreasing the inductance of the conductor. The mutual inductance also decreases with an increase in TSV radius, as the spacing increases with increase in radius. This reduces the

number of magnetic field lines that can couple with a neighboring TSV. Variation of inductance with TSV radius is shown in Figure 4.12. In Figure 4.12, the mutual inductance shown is the mutual inductance between two immediate TSVs evaluated by multiplying the coupling coefficient ‘k’ between the two TSVs with the self inductance.

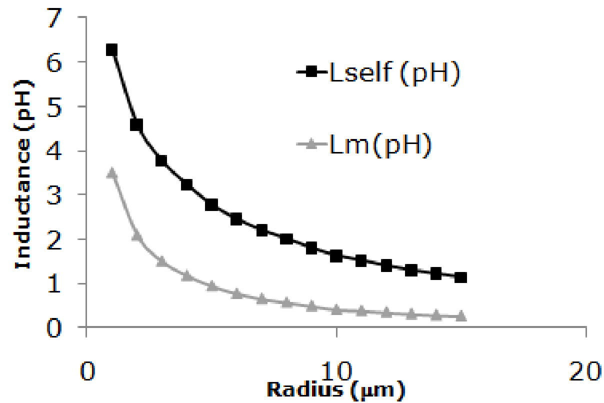

Figure 4.12 Variation of TSV inductance with radius

Now variation of capacitance with TSV radius is discussed. The self capacitance of TSV increases with TSV radius. As the TSV radius increases, the contact area of TSV with the dielectric coating increases. This results in an increase in the self capacitance of the TSV. As shown in Figure 4.13, as the TSV radius increases, the surface area of the cylinder (TSV) increases, thus increasing the contact area with the dielectric coating surrounding the TSV.

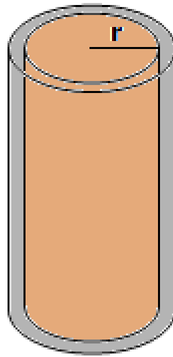

Figure 4.13 Single TSV with dielectric coating

The coupling capacitance depends on the portion of the surface area of the cylinders that face each other and the spacing between them. Figure 4.14 shows a pair of TSVs. The spacing between them is indicated as ‘S’. The coupling capacitance between TSVs 1 and 2 depend on the spacing ‘S’ and the surface area where the TSVs face each other. Initially for smaller radii the coupling capacitance increases slightly due to the increase in the surface area but for larger radii, the spacing dominates and the coupling capacitance decreases, as shown in Figure 4.15.

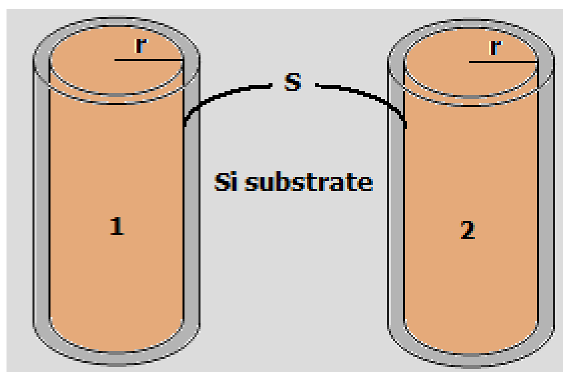

Figure 4.14 Coupling capacitance between a pair of TSVs

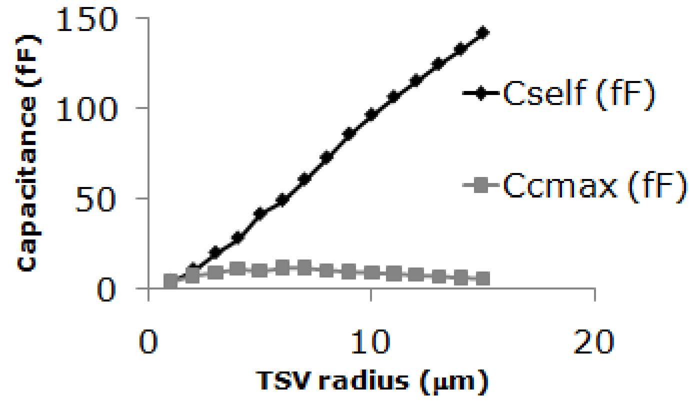

Figure 4.15 Variation of capacitance with TSV radius

4.4.2 Variation of mutual inductance and coupling capacitance with spacing

In this section, impact of TSV spacing on mutual inductance and coupling capacitance is studied. We considered a fixed TSV radius of 1µm and extracted the parasitics of TSVs for different spacing. Simulation results showing mutual inductance for different TSV spacing is shown in Figure 4.16.

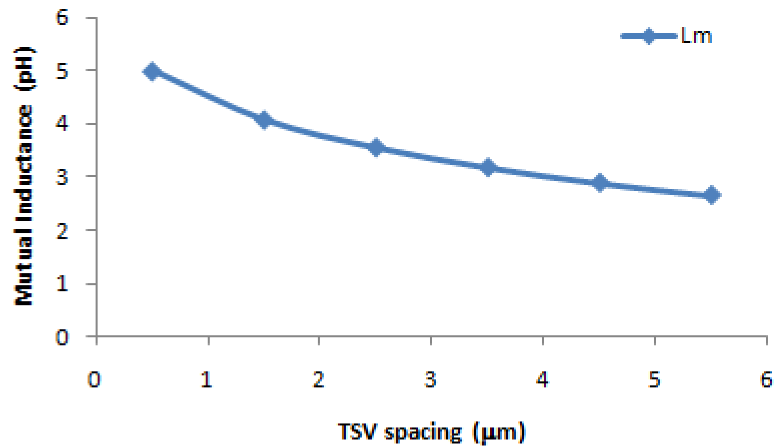

Figure 4.16 Variation of mutual inductance with TSV spacing

From 5.1.1Figure 4.16, it can be observed that as the spacing between the TSVs increases the mutual inductance between them decreases. This is because, as the spacing increases the number of magnetic field lines that can surround both the TSVs decreases, resulting in decrease in the mutual inductance.

Simulation results showing the variation of coupling capacitance with TSV spacing are shown in Figure 4.17. From Figure 4.17, it can be observed that the coupling capacitance decreases with an increase in spacing between the TSVs. As the capacitance between the two conductors is given by C = (εA)/d; indicating the inverse variation of capacitance with the spacing between the conductors given by 'd'.

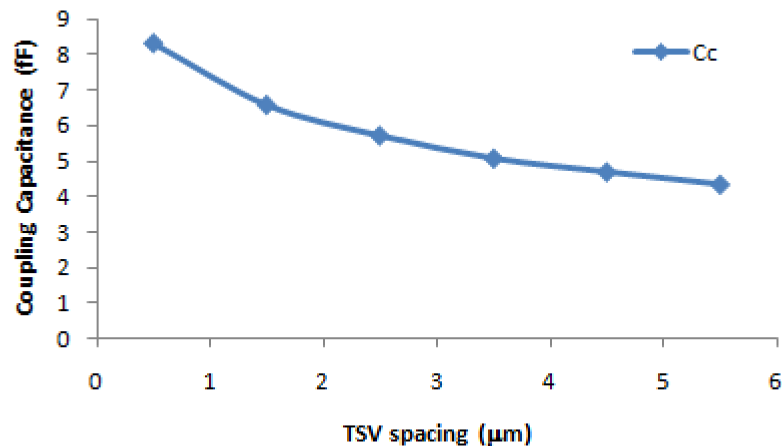

Figure 4.17 Variation of coupling capacitance with TSV spacing

4.4.3 Performance of signaling techniques for different TSV radii

In this section, we will see the impact of TSV radius on the performance (speed). To understand this we will write the delay equation through TSV. Let us consider the equivalent circuit model for delay estimation through TSV as shown in Figure 4.18.

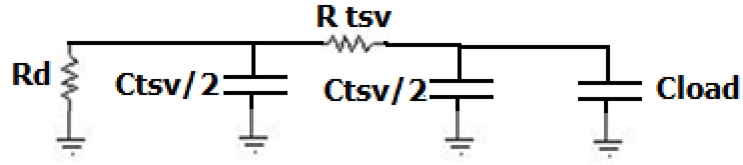

Figure 4.18 Equivalent circuit for TSV delay estimation

In Figure 4.18, the driver resistance is represented as R_D and load capacitance is represented as C_{Load}. TSV resistance is represented as R_{TSV} and TSV capacitance is represented as C_{TSV}. For the circuit in Figure 4.18, delay equation can be written as

$$T_D = 0.5 R_D C_{TSV} + 0.5(R_D + R_{TSV})C_{TSV} + (R_D + R_{TSV})C_{Load}$$

From the above equation it is understood that TSV delay is a function of R_D, R_{TSV}, C_{TSV} and C_{Load}. For understanding the impact of TSV radius on performance, we use TSVs with different TSV radius. As the TSV radius increases, its resistance decreases due to the increase in cross-section area. Maximum resistance is obtained for minimum TSV radius. Maximum TSV capacitance is obtained for higher TSV radius. Delay increases as the resistance and capacitance of TSV increase. However in case of TSVs, due to their length in microns, resistance is in milli ohms and the capacitance is found to be the dominating factor. Thus, TSV can be modeled as a capacitance ignoring the resistance. This is also mentioned in [28] where the authors first consider RC delay model for TSV interconnect and owing to very small resistance of TSV compared to driver resistance, they show that TSV is a capacitance dominated element and can be modeled as a simple capacitance. Resistance of TSV can be ignored because of its low value compared to the

driver resistance. So we can replace (R_D+R_{TSV}) in the delay equation with just R_D. To see why TSV resistance can be ignored we consider the maximum resistance of TSVs used in this work. The resistance of TSV of radius 1µm and at a frequency of 31GHz (62 Gbps) is found to be 225mΩ. This is much smaller compared to the minimum driver resistance of 165 Ω (for 64x inverter in 45nm). Hence we can ignore the TSV resistance and model it as a simple capacitance. Now the delay equation can be written as

$$T_D = R_D(C_{TSV} + C_{Load})$$

From the above equation it can be observed that for a given driver resistance and load capacitance, the delay depends on the capacitance of TSV. The delay increases with increase in TSV capacitance. From our study on dependency of capacitance on TSV radius, we observed that as the radius increases, TSV capacitance increases. As shown in Figure 4.19, the area of TSV in contact with the dielectric is the surface area of the cylinder. The surface area increases with an increase in TSV radius thus increasing the capacitance of TSV. The TSV capacitance for varying radius is shown in Figure 4.19.

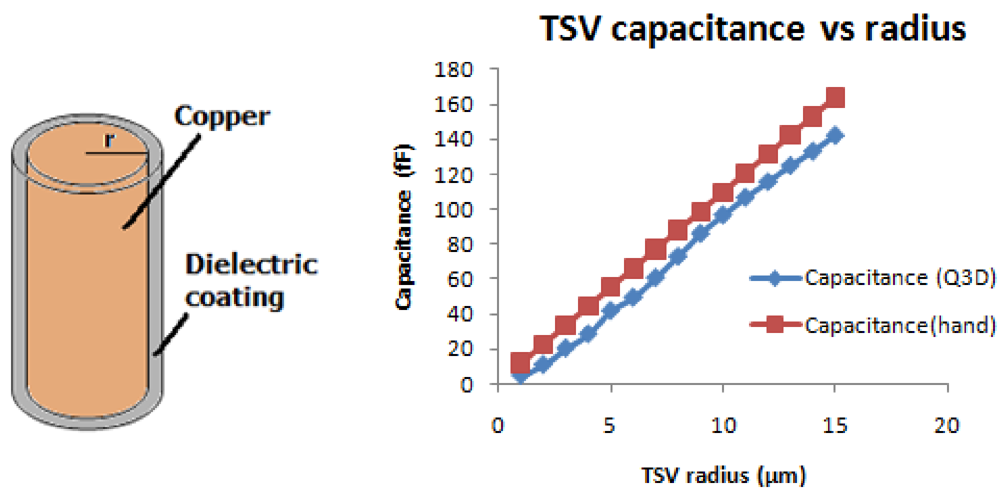

Figure 4.19 Copper TSV and its capacitance for different TSV radius

For hand calculation, we use the capacitance formula mentioned in [22] and given by

$$C = \frac{\varepsilon * 2\pi RL}{t}$$

C is the capacitance of TSV, ε is the permittivity of dielectric (silicon dioxide), R is TSV radius, L is length of TSV and t is thickness of dielectric coating. The authors in [22] mentioned that the capacitance formula mentioned above gives a simple expression for hand calculation. However they mention that the capacitance is over-estimated using the above mentioned formula as it assumes that the electric field lines from 3D via terminate on the cylinder surrounding the via dielectric liner[22].

Now we can see how TSV radius impacts the delay. From the delay equation $T_D = R_D(C_{TSV} + C_{Load})$, it can be observed that TSV delay increases with an increase in TSV capacitance. From Figure 4.19, we see that TSV capacitance increases with TSV radius. Hence we can say that TSV delay increases with an increase in TSV radius. TSV parasitics are extracted for 3x3 and 4x4 structures for TSV radius ranging from 1µm to 15µm. Using the single ended and differential signaling techniques discussed earlier and the extracted TSV parasitics for different TSV radii, simulations are carried out. In this work, we considered the TSV pitch to be twice the diameter as suggested by ITRS 2009 [20]. The simulation results for maximum data rates that can be obtained from each of the signaling techniques are shown in Figure 4.20.

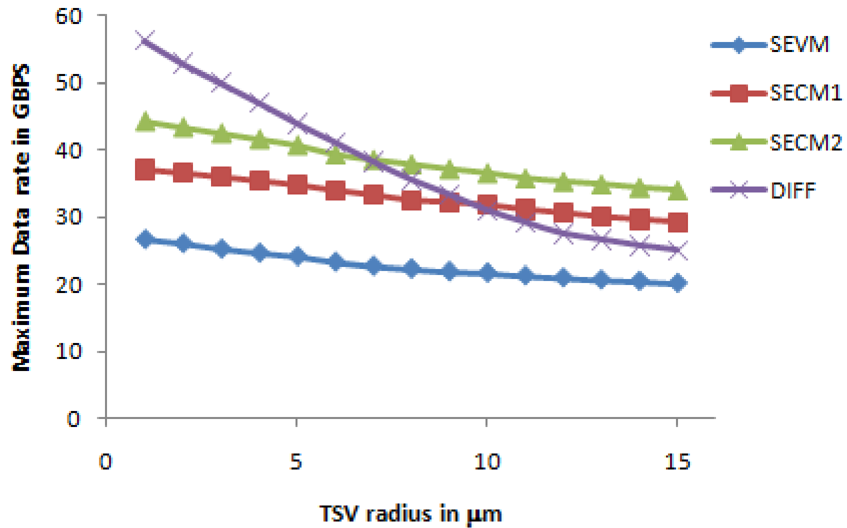

Figure 4.20 Maximum data rates of signaling techniques for different TSV radii

From Figure 4.20 it can be observed that as the TSV radius increases, the data rate of signaling techniques decreases. This is because, as the TSV radius increases, the total capacitance of the TSV increases, thus resulting in a reduction of the maximum data rate that can be attained. It can also be observed that differential signaling performs better for smaller radii compared to single ended techniques. Single ended voltage mode signaling has low data rates compared to other techniques. This is due to the full rail-to-rail swing required for SEVM compared to low swing in other signaling techniques. From this it is understood that the capacitance of a TSV is the dominating factor that determines the maximum data rate through TSV bundles. For applications that look for technologies with smaller radii, differential signaling provides the maximum data rate. For higher TSV radius (above 7µm), single ended techniques provide better performance.

To understand how data rates of single ended and differential signaling vary with TSV, a simple step response analysis can be carried out. For step response analysis, we

consider the equivalent circuit model of TSV shown in Figure 4.18. We provide a step input with rise and fall times of 10ps. The maximum data rate is obtained by reducing the bit time of the step input until it reaches the minimum eye opening criteria of 660mV for single ended and 400mV for differential signaling. From the step response eye diagrams it is observed that, for differential signaling we have maximum data rates of 60.6Gbps and 27Bbps for radius of 1µm and 15 µm respectively. For voltage mode signaling similar analysis is carried out and from simulaitons we observed the maximum data rates of 28.57Gbps and 21.7 Gbps for radius of 1µm and 15 µm respectively. The results from this step response analysis follow the results obtained from full circuit model simulations using PRBS input sequence shown in Figure 4.20.

In this chapter, various signaling techniques are explored. TSV parasitics are extracted for different TSV radii and performance of signaling techniques across TSV radius is analyzed. Impact of process, voltage and temperature variations between driver and receiver circuits will be discussed in next chapter.

CHAPTER 5

ROBUSTNESS ANALYSIS

In chapter 4, various techniques for signaling over TSV bundles are introduced. In case of signaling over TSV bundles, the driver and receiver circuits will be on different dies and these are subjected to process, voltage and temperature variations. In this chapter, we analyze the impact of these variations between driver and receiver circuits on single ended and differential signaling techniques.

5.1 Process Variations

In this section, the impact of process variations between driver and receiver circuits is considered. Process variations can be represented as threshold voltage (Vt) and effective channel length (Leff) variations. For this study, 4 corner cases as mentioned below are considered. Figure 5.1 shows the corner case process variations for driver and receiver circuits.

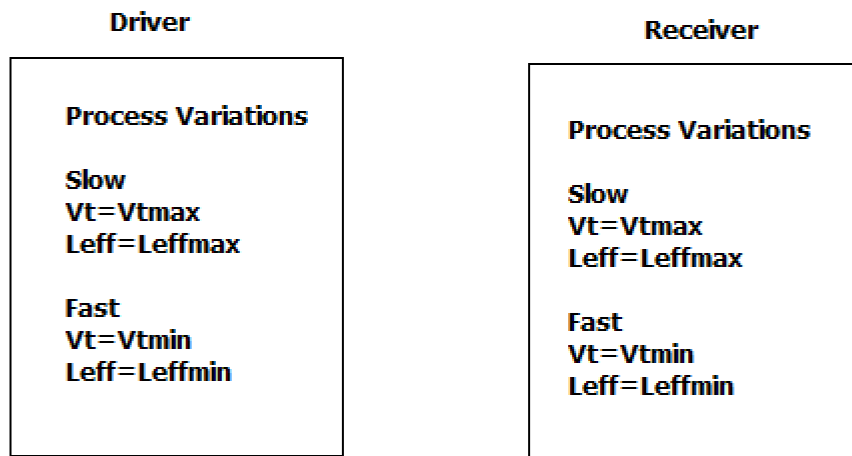

Figure 5.1 Corner case process variations between driver and receiver circuits

Case 1 – Slow Driver and Slow Receiver (SDSR)

Case 2 – Slow Driver and Fast Receiver (SDFR)

Case 3 – Fast Driver and Slow Receiver (FDSR)

Case 4 – Fast Driver and Fast Receiver (FDFR)

5.1.1 Threshold Voltage variations

Threshold voltage is one of the key factors that determine the performance of CMOS devices. Threshold voltage determines the electric potential that has to be applied on the gate terminal to create a channel and allow the majority carrier current flow through the device. An NMOS transistor is said to be "on" if the applied gate voltage relative to the source voltage is at least greater than threshold voltage. Threshold voltage can have a significant impact on the performance of the device. For a given input gate voltage, as threshold voltage increases, the device slows down. This is due to the decrease in the current that is used to charge and discharge the load capacitance. In this work, we consider the corner cases for analyzing the impact of threshold voltage variations between driver and receiver circuits. The driver or receiver circuit with a high threshold voltage will be slow and those with a low threshold voltage will be fast. ITRS [47] suggested a threshold voltage variation of 40% (3σ value), which is considered for this study. Using the ITRS suggested variation of ΔVt and Vt_{nom}, we can obtain Vt_{max} and Vt_{min} as shown below.

$Vt_{max} = Vt_{nom} + \Delta Vt$

$Vt_{min} = Vt_{nom} - \Delta Vt$.

Vt_{max} is the threshold voltage of a slow circuit

Vt_{min} is the threshold voltage of a fast circuit

Vt_{nom} is the nominal threshold voltage under no variations

ΔVt is the variation in threshold voltage.

4 corner cases can be identified depending on the threshold voltages of driver and receiver circuits. The maximum data rates for each of the signaling techniques for a TSV radius of 10µm are obtained. As shown in Table 5.1, it can be observed that compared to full swing single ended voltage mode signaling, the impact of process variations on low swing SECM2 signaling is high. The 3σ variation of 40% mentioned in ITRS is for a minimum size device. Process variations decrease with the increase in device size. It is inversely proportional to square root of area (W x L). Hence we consider an appropriate value of ΔVt depending on the size of the MOS transistor. Thus, the impact of process variation also depends on the size of transistors used.

From Table 5.1, it can be observed that low swing single ended signaling techniques suffer more due to Vt variations compared to full swing voltage mode signaling. In full swing signaling, the noise margin levels will be high compared to low swing signaling, thus making the low swing single ended signaling techniques more sensitive to process variations. The impact of process variations also depends on the size

of the transistors used in the circuit. For a circuit with bigger transistor sizes, the variations will be less resulting in low process variations.

Table 5.1 Impact of threshold voltage variation

Scenario	SEVM (Gbps)	SECM1 (Gbps)	SECM2 (Gbps)	DIFF (Gbps)
SDSR	19.8	28.8	32.5	28.5
SDFR	22.6	33.7	37.3	29.9
FDSR	21.5	30.0	34.8	31.9
FDFR	23.5	35.1	39.3	33.8
Nominal	21.7	32.2	36.6	31.0
Worst deviation	-8.7 %	-10.5%	-11.2%	-8.06%

5.1.2 Effective channel length variation

The effective channel length of a MOS transistor is the distance between the drain and source regions. Nominal channel length is the length of the gate region. However the drain and source regions spread beneath the gate region to a little extent, thus reducing the effective distance between drain and source regions. This distance between the drain and source regions is called the effective channel length of the MOS transistor. Variation in the channel length varies the current through the MOS transistor. As the channel length increases, the current through the device decreases. This results in a decrease in the performance of the device. Hence, shorter channel lengths yield faster circuits and longer

channel lengths result in slower circuits. Thus, we can have L_{max} and L_{min} as channel lengths for slow circuit and fast circuit, respectively. L_{max} and L_{min} are calculated using the nominal L_{eff} and variation in the channel length. Let ΔL be the variation of channel length. Then L_{max} and L_{min} are calculated as mentioned below.

$L_{max} = L_{eff} + \Delta L$

$L_{min} = L_{eff} - \Delta L$.

L_{max} is the effective channel length of a slow circuit.

L_{min} is the effective channel length of a fast circuit.

L_{eff} is the nominal effective channel length under no variations.

In this work, corner case analysis is carried out to analyze the impact of effective channel length variation. The channel length variation of 12% as suggested in ITRS 2009[47] is considered. Simulations are carried out considering the corner cases of channel length variation. As shown in Table 5.2, maximum data rates are obtained for each of the signaling techniques under effective channel length variations. It can be observed that similar to Vt variations, the impact of channel length variation is high on low swing single ended signal techniques compared to full swing voltage mode signaling. Differential signaling also has less impact compared to other signaling techniques. This might be due to usage of fixed current sources in differential signaling tolerating the impact of current variations due to effective channel length variations.

Table 5.2 Impact of effective channel length variation

Scenario	SEVM (Gbps)	SECM1 (Gbps)	SECM2 (Gbps)	DIFF (Gbps)
SDSR	19.6	28.5	31.7	28.8
SDFR	22.4	33.4	36.2	29.4
FDSR	20.8	30.7	35.4	31.9
FDFR	23.4	36.0	40.6	33.3
Nominal	21.7	32.2	36.6	31.0
Worst deviation	-9.7%	-11.5%	-13.4%	-7.1%

For differential signaling it is important to consider the impact of mismatch between the transistors on different legs. The resistors used in two legs can have a variation. The threshold voltage and effective channel length variations between the transistors on different legs can have different values due to mismatch. As shown in Figure 5.2, the resistor and the transistors on one leg are considered to have different threshold voltage, effective channel length and resistance values compared to those on the other leg. Variations in effective channel length and threshold voltage are considered similar to earlier analysis of driver receiver variations. A resistance variation of 10% is assumed. The impact of mismatch variation is tabulated. From Table 5.3, it can be observed that mismatch between the legs of a differential circuit results in a shift in the average output voltage. To understand this consider the transistors and resistor of leg1 (colored green) to form a low Vt, low Leff and low resistance leg, resulting in an increase in the output voltage out1 by say k1 from its nominal case.

$Out1_{new} = Out1_{nom} + k1$

Similarly consider the transistors in the other leg (colored blue) are at high Vt, Leff and a high resistance. The output voltage out2 decreases in this leg. This results in the output of this leg to reduce by an amount k2 (say) from its nominal value.

$Out2_{new} = Out2_{nom} – k2$

Now the difference voltage is given by

$Out1_{new} – Out2_{new} = (Out1_{nom}- Out2_{nom}) + k1+k2.$

The term (k1+k2) is the shift in the output voltage of the difference signal. The output shift for Vt mismatch, Leff mismatch and resistance mismatch results are shown in Table 5.3.

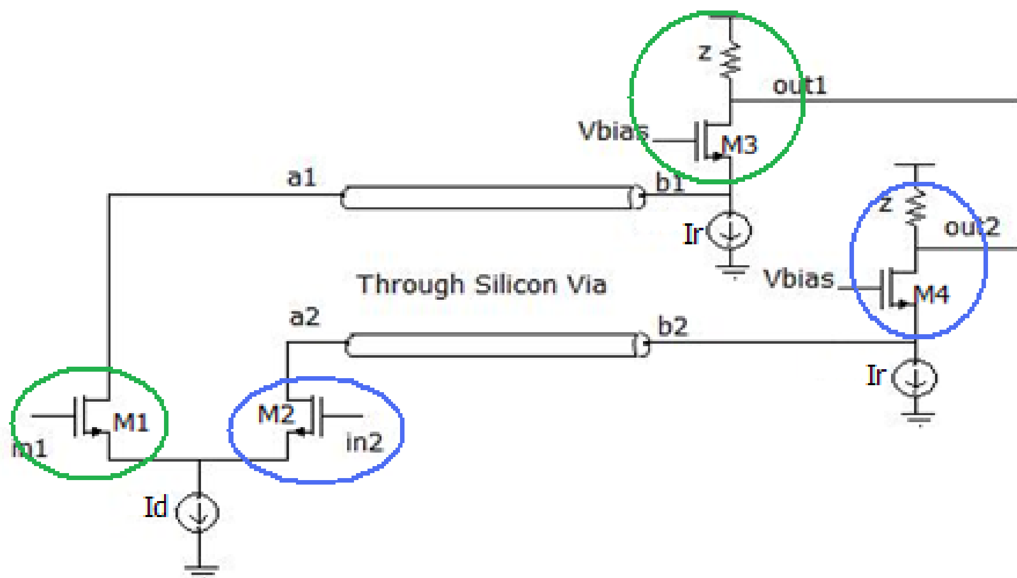

Figure 5.2 Mismatch analysis for differential signaling

Table 5.3 Impact of mismatch in differential signaling

Scenario	Output shift (mV)
Nominal	0
Vt mismatch	51.6
Leff mismatch	36.5
Resistance mismatch	23
Vt + Leff + Res mismatch	121.6

From this process variations study, it is observed that single ended low swing signaling techniques suffer more compared to full swing signaling techniques. For differential signaling, mismatch between the transistors shifts the output voltage level by as much as 121mV in the worst case. However, there is not much impact on the data rate due to mismatch in differential signaling.

5.2 Voltage variations

Supply voltage is one of the key factors that determine the performance of the signaling system. Higher supply voltage (VDD) results in faster circuits. This is due to the increase in the current flowing through the circuit. This increased current can charge the load quickly resulting in a faster circuit. However, supply voltage is not constant throughout the chip. This is due to the presence of IR drop and L (di/dt) noise due to parasitics of power distribution network.

In this work, we considered VDD variations of 10% due to IR drop as suggested in ITRS 2009[47], and simulations are carried out for the corner cases considering the VDD variations due to IR drop between driver and receiver circuits. VDD_{max} and VDD_{min} are evaluated considering the maximum variation of 10 % VDD.

$VDD_{max} = 1.1*VDD$ and $VDD_{min} = 0.9*VDD$

Table 5.4 Impact of VDD (IR drop) variation on signaling techniques

Scenario	SEVM (Gbps)	SECM1 (Gbps)	SECM2 (Gbps)	DIFF (Gbps)
SDSR	17.9	26.5	28.5	30.5
SDFR	19.0	30.8	34.1	31.5
FDSR	19.0	30.5	33.9	30.7
FDFR	24.1	35.9	3.6	31.8
Nominal	21.7	32.2	36.6	31.0
% worst deviation	-17.5	-17.7	-22.1	-1.6

.

The circuit with VDD_{max} gives the fast circuit while the circuit with VDD_{min} gives the slow circuit. Since we are interested in variations between driver and receiver circuit, 4 corner cases, Slow Driver Slow Receiver (SDSR), Slow Driver Fast Receiver (SDFR), Fast Driver Slow Receiver (FDSR) and Fast Driver Fast Receiver (FDFR) are considered. The simulation results are shown in Table 5.4. It can be observed that single ended signaling techniques suffer significantly due to VDD variations. Differential signaling

sees little impact due to the variation in supply voltage due to its high rejection to common mode noise.

Supply voltage suffers from L∗(di/dt) noise due to the activity of neighboring circuits. In current technology nodes, the supply voltages have reduced significantly, resulting in lower noise margins. Lower voltage supplies with increased functionality and data rates have resulted in significant increase in the impact of power supply noise. As discussed earlier in Chapter 2, this problem is much more severe in 3D ICs. 3D stack with k tiers would require k-times higher current compared to a 2D chip with a similar foot print. In 3D ICs, the variation in currents drawn in one tier can impact the supply nodes in adjacent tiers resulting in an increased dynamic noise. A significant increase in power supply noise with increase in the number of tiers is shown in [31].

In this work, a global power supply noise of 100MHz frequency as mentioned in [27] is considered. In [27], the authors considered a stack of 5 dies and estimated the supply noise in a 5 stack 3D IC. The voltage drop value for a 5 stack 3D IC estimated in [27] is shown in Figure 5.3. It can be observed that the noise frequency does not change from tier to tier. However, its amplitude varies from 100mV for tier1 and increases up to 140mV for the 5th tier. In this work, we considered the supply noise amplitudes of 100mV and 120mV, as suggested in [27]. Two cases are considered assuming the worst case supply drop of 120mV and 100mV on the driver receiver pair. Case 1 with 100mV drop on the driver side and 120mV drop on the receiver side and case 2 with 120mV drop on the driver side and 100mV drop on the receiver side.

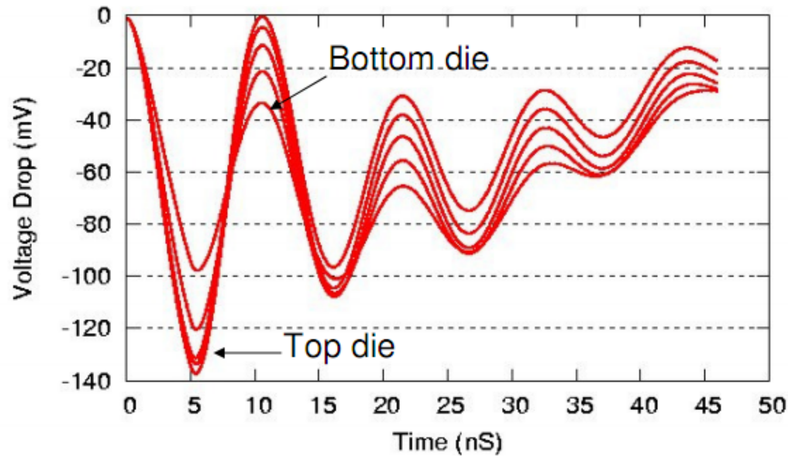

Figure 5.3 Voltage drop across different tiers in 3D IC [27]

Simulation results to understand the impact of supply noise on signaling techniques are shown in Table 5.5. It can be observed that single ended signaling techniques suffer significantly due to the supply noise. However, differential signaling technique has better robustness to supply noise due to its ability to reject the common mode noise.

Table 5.5 Impact of supply noise on signaling techniques

Scenario	SEVM (Gbps)	SECM1 (Gbps)	SECM2 (Gbps)	DIFF (Gbps)
Case 1	18.3	26.9	28.8	30.4
Case 2	17.9	26.5	28.4	30.5
Nominal	21.7	32.2	36.6	31.0
% deviation worst case	-17.5	-17.7	-22.4	-1.9

Among single ended techniques, low swing signaling technique SECM2 suffers more compared to full swing SEVM technique. In the full swing technique, we have higher noise margins compared to the low swing techniques. In conclusion, it can be said that differential signaling is highly robust to supply voltage variations.

5.3 Impact of temperature

On chip temperatures vary due to the activity of the circuit blocks. The power dissipated by the active blocks can result in a local temperature rise. Heat removal mechanisms are needed to control the rise in temperature. As technology scales down, the number of functional blocks on a chip increases, resulting in higher number of active blocks for a given area. This results in an increase in temperature of a chip with the technology scaling. This becomes a more severe problem for 3D ICs. Consider a 2D chip redesigned into a 3D structure with same functionality (similar power dissipation but with a smaller foot print). The power density in this redesigned 3D structure will be higher compared to 2D. To achieve higher performance and cost benefits, the number of stacks in a 3D IC is increased. However, as the number of stacks in a 3D IC increases, the temperature increases. Furthermore, the heat generated by the dies that are located away from the heat sink is difficult to transfer. This results in a temperature gradient in the vertical direction.

In this work, we perform simulations to understand how the signaling techniques perform for different temperature assumptions on the driver and receiver sides. The temperature between two dies in a 3D stack varies depending on the activity of individual dies. Temperature gradients as high as 50ºC are reported for high performance

microprocessors [44]. As the temperature is highly dependent on the activity of the neighboring blocks, we consider the following cases to understand how different signaling techniques behave under these thermal conditions.

Case1 – 50ºC on both driver and receiver

Case 2 – 50ºC on driver and 100ºC on receiver

Case 3 – 100ºC on driver and 50ºC on receiver

Case 4 – 100ºC on both driver and receiver.

The simulation results are compared with nominal maximum data rates at 25ºC, as shown in Table 5.6.

From Table 5.6, it can be observed that an increase in the temperature significantly reduces the maximum data rate of all the signaling techniques. However, it should be noted that we have considered the worst scenario assuming the hotspots located close to driver and receiver circuits. Temperature impact depends on the relative location of the hotspots and the driver and receiver circuits. Thermal aware placement mechanisms can significantly reduce the impact of temperature.

Table 5.6 Impact of temperature on signaling techniques

Scenario	SEVM (Gbps)	SECM1 (Gbps)	SECM2 (Gbps)	DIFF (Gbps)
Case-1	18.3	27.6	30.5	26.9
Case-2	15.1	23.6	25.7	23.4
Case-3	15.3	23.7	24.1	22.5
Case-4	13.3	20.2	22.2	19.0
Nominal (25ºC)	21.7	32.2	36.6	31.0
% worst deviation	-38.7	-37.3	-39.3	-38.8

5.4 Mechanical impact of temperature on TSV

In this section, we will see the impact of temperature on the dielectric surrounding the TSVs. As the temperature increases the material dimensions expand depending on the coefficient of thermal expansion (*CTE*) of the material. The *CTE* describes by how much the material will expand for a 1°C rise in temperature. This is given by

$$CTE = dT\left(\frac{dl}{l}\right)$$

In the above equation, *dl* is the change in length *l* of the material due to expansion and *dT* is the change in temperature.

Now, we will calculate the change in thickness of dielectric due to temperature increase from 25°C (nominal value) to 100°C. The *CTE* of silicon dioxide material is 0.5µm/m/°C [48]. Thickness of dielectric is 0.2µm.

Change in thickness of dielectric = *CTE∗(initial thickness)∗(dT).*

Initial thickness at 25°C = 0.2µm.

dT = New temperature – nominal temperature = 100°C – 25°C = 75°C.

Change in thickness of dielectric = 0.5µm/m/°C∗0.2µm∗75°C = 7.5pm.

From the above solution it can be observed that the thickness of dielectric increases by 7.5pm when temperature increases from the nominal value of 25°C to 100°C. This shows that the mechanical impact of temperature on thickness of dielectric is very little as the increase of 7.5pm is low compared to its thickness of 0.2 µm.

Now we will see the impact of temperature on copper metal of the TSV.

CTE for copper is 16.75µm/m/°C

For radius of 5 µm, change in radius of copper can be calculated using

Change in radius of copper = *CTE∗(initial radius)∗(dT)* = 16.75µm/m/°C∗5 µm∗75°C = 6.26nm

From this it can be observed that the radius of the copper metal will expand by 6.26nm. This is much less compared to its radius of 5 μm.

5.5 TSV fault tolerance architectures

In this section we discuss TSV fault tolerance architectures. Although TSVs are excellent electrical conductors, a failed TSV can cause a number of known good dies that are stacked together to be discarded. Hence, it is important to consider fault tolerance in TSV based 3D ICs. Redundancy based fault tolerant schemes provide a simple solution [13]. In this section, a simple analysis on redundancy based fault tolerant architectures with particular focus on their impact on high speed serial signaling techniques is explained. Figure 5.4 shows three possible approaches of redundancy based fault tolerant architectures obtained by changing the relative positions of Serializer (Ser), fault recovery multiplexer (MUX) and the driver circuits. The redundant TSV (R_TSV) and faulty TSV are shown in Figure 5.4 assuming that the second TSV is a faulty one and the fourth is a redundant TSV.

Fault tolerant model A, as shown in Figure 5.4 (a) is a simple solution consisting of a serializer, followed by a driver and a one bit 2x1 MUX or the delay cell. There are two major issues with this approach. The first one is the dependency of the MUX and delay logic implementation on the signaling scheme. For example, differential signaling with Current Mode Logic (CML) driver requires the MUX and delay cells to be implemented in CML compatible logic. In order to utilize these excellent but scarce TSVs efficiently, it is important to operate at the maximum data rate through the TSV that can be supported by a particular signaling technique. Hence, it necessitates the

design of fault recovery MUX and delay cells to support such high speeds ,resulting in an increased design complexity and power consumption.

In approach B, as shown in Figure 5.4 (b), it can be observed that the MUX and the delay cell logic can be implemented independently of the signaling technique and the implementation logic of the driver. This comes with an overhead of additional driver circuit for redundant TSV. This approach still necessitates the design of fault recovery MUX and delay cells to be able to operate at the data rates through TSVs.

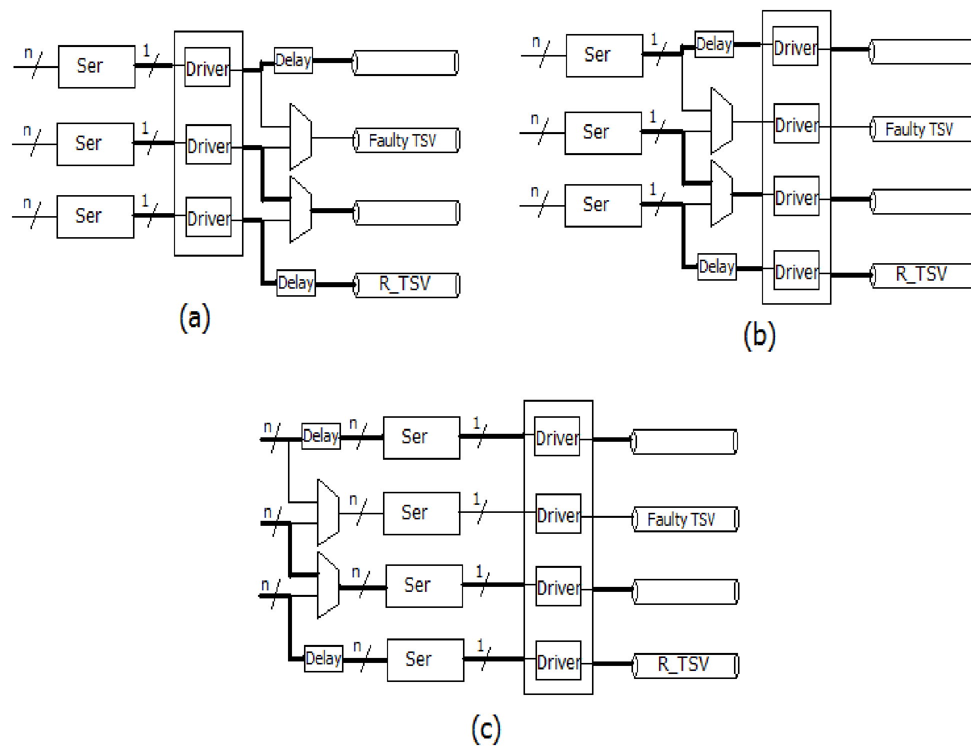

Figure 5.4 Redundancy based fault tolerant architectures (a) Final stage MUX based approach (b) Driver decoupling MUX and TSV approach (c) MUX before Serializer approach

In approach C, as shown in Figure 5.4 (c), the multiplexing is moved before the serialization block. This facilitates the design of MUX and delay cells that can operate at the data rates that are ‘n’ times smaller than the signal data rates for an n:1 Serializer. This approach reduces the power and design complexity of the MUX and delay cells. The overhead involves an additional Serializer and the driver circuit for the redundant TSV. Also, one bit 2x1 MUX and delay cells are now replaced with ‘n’ bit 2x1 MUX and ‘n’ bit delay cells. Thus, depending on the signaling technique, an optimum fault tolerance scheme should be determined considering the above tradeoffs. In order to efficiently utilize the excellent electrical properties of TSVs, it is important to operate at the maximum data rates supported by the signaling scheme.

5.6 Impact of stuck at faults

Assuming the fault tolerance scheme described in Figure 5.4 (c), simulations are performed to understand the impact of a faulty TSV in a 3x3 bundle. The faulty TSV can be stuck at 1, stuck at 0, short circuited to another net or open circuited. The eye height and eye width on the center TSV under the ideal case, and those when one of the TSVs is stuck at VDD, VSS or open circuited for SEVM, is shown in Table 5.7. From Table 5.7, it can be observed that there is little impact of the faulty TSV on the normal TSV. This is primarily due to the low coupling capacitance. If we had significant coupling, the faulty TSV can act as a VDD or VSS TSV depending on the stuck at fault, thus providing improvement to the eye diagram acting as a shield TSV. Since the coupling capacitance values are very low, the signaling on the TSVs is dominated by power supply noise and Inter Symbol Interference rather than coupling.

Table 5.7 Impact of fault TSV

Fault Type	Eye Height (V)	Eye Width (ps)
No Faulty TSV	0.6719	33.242
Undriven TSV	0.6721	33.251
Stuck at VDD	0.6723	33.233
Stuck at VSS	0.6719	33.247

In this chapter, we have considered process, voltage and temperature variations between driver and receiver circuits to study their impact on single ended and differential signaling techniques. Low swing single ended signaling techniques suffer more compared to full swing single ended signaling. Differential signaling is highly robust to supply noise variations compared to other signaling techniques. An increase in the temperature decreases the maximum data rate of both single ended and differential signaling techniques.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusions

This thesis focuses on signaling over Through Silicon Via (TSV) bundles. TSV based 3D ICs are one of the possible solutions to tackle the problem of interconnect bottleneck of 2D ICs. In this work, we extracted the electrical parasitics of TSV bundles and obtained maximum data rates for single ended and differential signaling techniques. As TSV parameters are not yet standardized by the 3D community, TSV technologies with different TSV dimensions are considered by the research community. TSV radius is one of the key parameters that determine the electrical parasitics of TSV. To understand the behavior of signaling over TSV bundles across different technologies, we extracted the electrical parasitics of TSV bundles for different TSV radii (from 1μm to 15μm). The maximum data rate for each of the signaling techniques is determined for a TSV radius from 1μm to 15μm. Based on the simulation results, it is observed that differential signaling gives better performance for a TSV radius less than 7μm.

Robustness analysis on signaling techniques is carried out on single ended and differential signaling techniques. For robustness analysis, the impact of process, voltage and temperature variations between driver and receiver circuits is considered. Single ended low swing signaling techniques suffer more due to process variations compared to full swing voltage mode signaling. Supply voltage variations have significant impact on the single ended signaling techniques. In differential signaling, the differential output

nullifies the impact of supply voltage variations, as both the legs see the same noise on the output. With an increase in temperature, all the signaling techniques suffer significantly. Based on these results, one can opt for differential signaling for lower TSV radii and for the environment with higher supply voltage variations. For higher TSV radius, and with less supply voltage variations, single ended signaling techniques will be a better choice over differential technique. Among single ended techniques, low swing techniques provide higher performance but suffer more due to process variations.

6.2 Future work

3D integration is one of key research areas in semiconductor industry to tackle the problem of the interconnect bottleneck. As mentioned in this work, it stills lacks the standardization and CAD tool support for a timely and more extensive research. In this work, we tried to show how signaling techniques perform for different TSV radii and their behavior under process, voltage and temperature variations. Future work can focus on exploring various TSV parameters (both material and physical dimensions) and help in developing some standards for signal TSV dimensions and material. Fault tolerance is one of the key areas that can be considered. However, it requires TSV fault models for different TSV dimensions and material. Developing fault models that can be incorporated in SPICE simulations can save significant time invested on extracting electrical parasitics under different fault assumptions. Thermal aspects of 3D ICs are also being extensively researched by the 3D community. It might be an interesting problem to see the impact of using thermal TSVs along with signal TSVs and suggest an optimum signaling technique that meets performance, energy and temperature requirements. Signal encoding

techniques might help in reducing the power dissipation and can be incorporated in the study of co-optimizing power, thermal, performance and fault tolerance aspects for signaling over TSVs.

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