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# Millimeter Wave Indium Phosphide Heterojunction Bipolar Transistors: Noise Performance and Circuit Applications

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*University of Massachusetts Amherst*

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**MILLIMETER WAVE INDIUM PHOSPHIDE  
HETEROJUNCTION BIPOLAR TRANSISTORS: NOISE  
PERFORMANCE AND CIRCUIT APPLICATIONS**

A Thesis Presented

by

Metin AYATA

Submitted to the Graduate School of the  
University of Massachusetts Amherst in partial fulfillment  
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

September 2014

Electrical and Computer Engineering

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C.V.Hollot, Department Chair  
Electrical and Computer Engineering

*In the name of Allah, the Most Gracious, the Most Merciful.  
To My Family*

**ABSTRACT**

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HETEROJUNCTION BIPOLAR TRANSISTORS: NOISE  
PERFORMANCE AND CIRCUIT APPLICATIONS**

SEPTEMBER 2014

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# CHAPTER 1

## INTRODUCTION

The performance of III-V heterojunction bipolar transistors (HBTs) has improved significantly over the past two decades. Today's state of the art Indium Phosphide (InP) HBTs have a maximum frequency of oscillation greater than 800 GHz [2] and have been used to realize an amplifier operating above 600 GHz [3]. In comparison to silicon (Si) based devices, III-V HBTs have superior transport properties that enables a higher gain, higher speed, and noise performance, and much higher Johnson figure-of-merit<sup>1</sup> [4–6]. From this perspective, the InP HBT is one of the most promising candidates for high performance mixed signal electronic systems.

Since small-signal modelling and noise characterization form a bridge between engineering and system design, there is a tremendous need for accurate and verified small-signal and noise models. *This thesis is focused on the development and use of small-signal HBT noise models valid from 0.01–67 GHz.*

In the first part of the thesis, there is an introduction to bipolar junction transistor (BJT) and InP HBTs technology is provided. The concepts of band gap energy and electron and hole mobility will also be discussed in the first chapter. At the end of the chapter, commonly used compact HBT models are reviewed and the approach of the work is described.

In the second chapter, the fundamentals of small-signal modelling will be covered. The extraction methods for the each model parameter are discussed and statistics

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<sup>1</sup>The Johnson figure-of-merit is equal to the product of transistor cutoff frequency and breakdown voltage.

for each parameter are provided. Furthermore, the frequency and bias dependence of the parameters is explored. Finally, agreement between the models and measurement data will be investigated

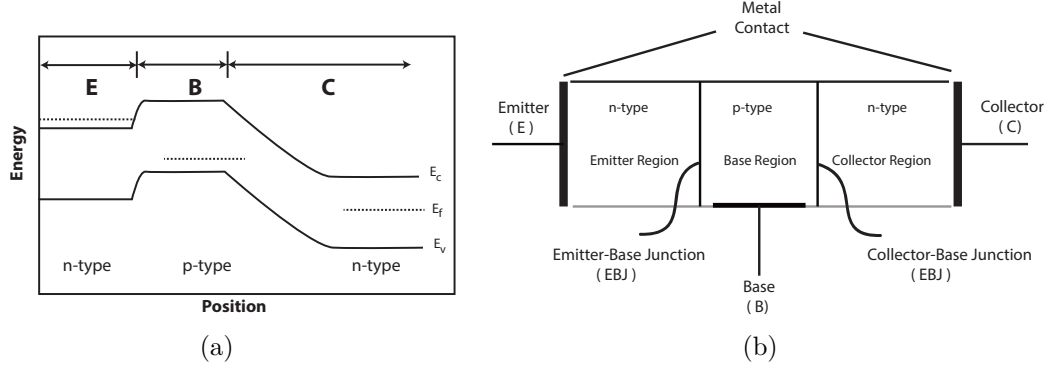
In the third chapter, the noise in HBTs is studied. The most common noise figure measurement techniques are discussed and the measurement setup used in this work is presented. Measurement results showing the collector current, frequency, and size dependency of the noise figure will be presented. In the last part of the chapter, the noise modelling of transistors is examined. Finally, the noise parameters of the different sized transistors is presented and discussed.

The last part of the thesis includes an application based on the extracted small-signal noise model. A Ku band low noise amplifier (LNA) is designed to exercise the extracted device models. Also, the comparison between an available VBIC model and the extracted model will be presented.

## 1.1 Bipolar Junction Transistor

The first solid-state BJT was invented by William Shockley, John Bardeen, and Walter Brattain in 1948 [7]. A bipolar junction transistor consists of two back-to-back p-n junctions that share a single p-doped region. Metal contacts are made to all three regions. The two outer regions are the heavily n-type doped emitter and the lightly n-type doped collector. The middle p-type doped region is called the base. The structure of an npn bipolar transistor is shown in Figure 1.1. Transport in a BJT in the forward active region is explained through the energy diagram of Figure 1.1 (a).

Since the emitter is heavily doped, the electrons diffuse from the emitter into the base and holes diffuse from the base into the emitter creating a diffusion current. Once the electrons arrive at the base-collector depletion region, they are swept through the depletion layer due to the electric field across the reverse biased base-collector junction. These electrons contribute to the collector current. As detailed in [9], the



**Figure 1.1.** (a)Energy-band-diagram of a BJT. Reproduced from [8], and (b)Basic Bipolar Junction Transistor

terminal currents are written as the summation of the electron and hole diffusion currents and the base layer recombination currents. The DC current gain ( $\beta_{DC}$ ) of the transistor is defined as ( $\beta_{DC}$ ) [10]

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{J_C}{J_B} \approx \frac{\mu_n L_{PE} N_{DE}^+}{\mu_p W_B N_{AB}^-}. \quad (1.1)$$

where  $\mu_n$  and  $\mu_p$  are the electron and hole mobilities, respectively,  $L_{PE}$  is the diffusion length,  $W_B$  is the base width,  $N_{AB}^-$  is the ionized acceptor concentration in the base and  $N_{DE}^+$  is the ionized donor concentration in the emitter, respectively.

The DC current gain depends both material and geometric parameters, as well as the ratio of ionized dopant concentration in the emitter to that in the base. It should be noted that the diffusion length is inversely proportional to doping [11].

Thus, the main degree of freedom for controlling  $\beta_{DC}$  is the ratio of  $N_{DE}^+$  to  $N_{AB}^-$ . However, the ionized donor concentration in the emitter cannot be increased infinitely, as both the mobility and diffusion length are inversely proportional to doping [12]. Also, increasing the doping concentration of emitter results in a decrease in the band gap. In other words, in order to increase the DC current gain, the only option is to decrease the ionized acceptor concentration in the base ( $N_{AB}^-$ ). However, there is a



trade-off between increasing the current gain and base resistance. To understand this trade-off, note that the base resistance is inversely proportional to the conductance of the base film, which can be written as:

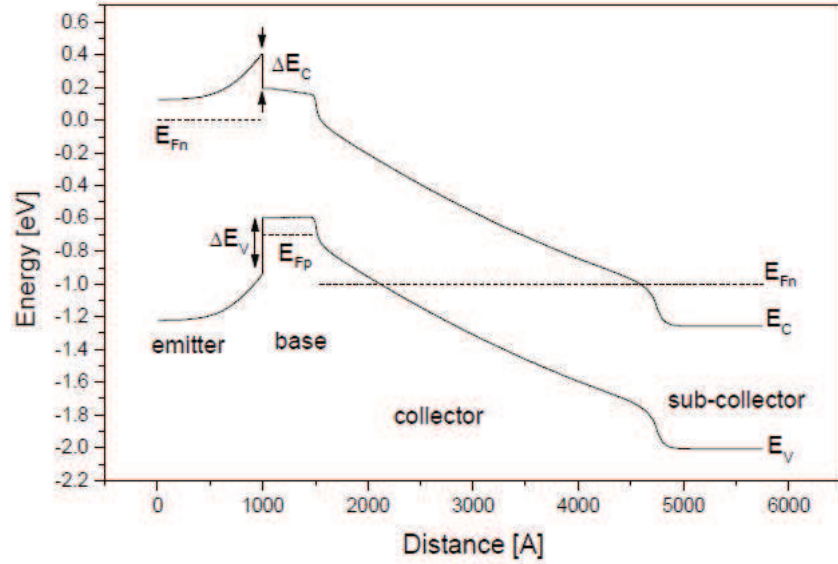
$$\sigma = q(p\mu_p + n\mu_n). \quad (1.2)$$

where  $q$  is the charge of an electron, and  $\mu_p$  and  $\mu_n$  are the mobilities of the electrons and holes and  $n$  and  $p$  refer to the density of electrons and holes, respectively. Since decreasing the ionized acceptor concentration results in high base resistance, it will also result in a decrease in the maximum oscillation frequency of the device, which is a very important figure-of-merit describing high frequency operation. Thus, transistors with both high DC current gain and high frequency of operation are not practical using homojunction BJT technologies. This shortcoming limits the use of homojunction BJT technology in micro/millimeter wave low noise applications [13].

## 1.2 Indium-Phosphide HBT Technology

The idea of the Heterojunction Bipolar Transistor was first presented by Herbert Kroemer in 1957 [14]; for this and other work on heterojunctions, he received the 2000 Nobel Prize in Physics [15]. An HBT is composed of three layers regions; emitter, base, and collector like a homojunction BJT. However, different from a homojunction BJT, an HBT has a heterojunction, where two different materials with two different band gaps are used. Using a wide band gap heterojunction emitter allows the base to be highly doped which increases the conductivity of the base and DC current gain [11]. As a result of the highly doped base region, the resistivity of the base region reduces. These fundamental advantages of HBTs provide high speed and high current gain devices.

The energy band gap diagram of an InP based HBT is shown in Fig. 1.2. The drift component of carrier transport through the base, due to electric field and concentration gradient, is similar to homojunction bipolar transistors. However, in contrast to BJTs, HBTs have narrower base and wider emitter band gap energy levels region. In these systems, the potential barrier seen by base holes in the valence band is higher than what is seen by emitter electrons in the conduction band. For a given highly doped base, this results in higher emitter injection efficiency, leading to higher gain [12].



**Figure 1.2.** Energy band gap diagram of an HBT under forward active bias. Reproduced from [16]

InP based HBTs have superior mobility compared to Silicon/Silicon Germanium (Si/SiGe) based HBTs because of having high band-gap energy at the emitter terminal which is,  $E_g = 1.35$  eV for the emitter and  $E_g = 0.76$  eV for the base [14,17]. Since, the emitter has a higher band gap energy than the base region, a high DC current gain

can be obtained. Moreover, the base transit time is reduced due to narrower base band gap that means the transistor cut-off frequency also known as the unity gain,  $f_t$ , increases since it is inversely proportional to the base transit time [16]. The table shown below (see Table 1.1) is the summary of the important parameters of different type of semiconductor materials. From this table it can also be seen that the electron mobility of InP is greater than Si by a ratio of 4:1. This is another advantage for high performance systems.

**Table 1.1.** Important parameters of different type of semiconductor materials [1]

Material Property at T=300 K	Units	InP	$In_{0.53}Ga_{0.47}As$	Si
Bandgap	eV	1.35	0.75	1.2
Thermal Conductivity	W/cm.K	0.68	0.05	1.5
Electron Effective Mass	$M_0$	0.078	0.041	0.98/0.19
Electron Peak Velocity	$\times 10^7$ cm/s	2.5	3	1
Electron Mobility ( $N_D=1 \times 10^{17} cm^3$ )	$cm^2/V.s$	3200	7000	800

### 1.3 Overview of the Models

Accurate simulation models are required to efficiently implement integrated circuits. To ensure scalability of these models, it is desirable that they are physics based. Hence, engineers have developed a variety of different physics-based simulation models. The most widely used compact HBT models are, Gummel-Poon Model, VBIC (Vertical Bipolar Inter-Company model), HICUM (High Current Model) and MEXTRAM (Most EXquisite TRAnsistor Model).

Before skipping to the models, the shot noise concept needs to be explained. Shot noise occurs due to DC currents through the pn junctions. Physically, when the carriers diffuse across a the potential barrier, they create the shot noise. When a BJT is under forward active bias, majority holes from the base and majority electrons from the emitter cross the base-emitter potential barrier contribute to shot noise. Current crossing the base-collector junction has a noise component as well, although this

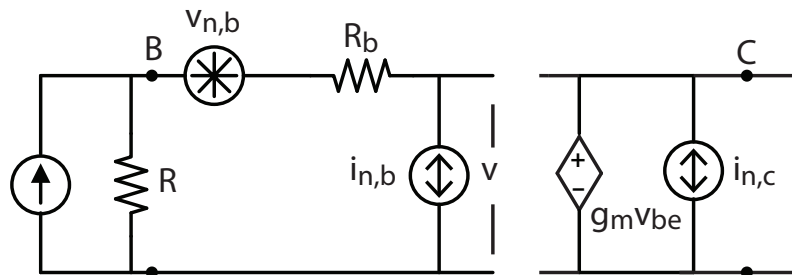
noise was actually generated at the base-emitter junction. Therefore, the correlation of these sources is given by a time delay which is critical at high frequencies described in the equation 1.5 [18]. All the expressions for base and collector shot noises and the correlation between these noises are given below.

$$\overline{|i_{n,b}|^2} = 2q(I_B + |1 - \exp(-j\omega\tau_n)|^2 I_C) \quad (1.3)$$

$$\overline{|i_{n,c}|^2} = 2qI_C \quad (1.4)$$

$$\overline{i_{n,b} \cdot i_{n,c}^*} = 2qI_C (\exp\{j\omega\tau_n\} - 1). \quad (1.5)$$

where  $i_{n,b}$  and  $i_{n,c}^*$  are base and collector shot noises respectively,  $I_C$  is collector DC current,  $\tau$  is the noise transit time and  $f$  is the frequency. A low-frequency noise equivalent circuit is given in Figure 1.3. It can be seen that the two dominant noise sources at low frequencies are thermal and shot noise. Moreover, at low frequencies the determination of the noise parameters is straightforward since the correlation between the base and the collector shot noise sources is zero.



**Figure 1.3.** Simple noise equivalent circuit of transistor

The VBIC model is the model available for the technology considered in this work and it has four terminals; the base, emitter, collector and substrate. In later chapters, we will be comparing our model results to the foundry supplied VBIC

model. Therefore, it is important to briefly summarize the VBIC formulation. From the noise point of view, the resistances ( $R_{BX}$ ,  $R_{CX}$ ,  $R_E$ ,  $R_S$ ,  $R_{BP}$ ,  $R_{CI}$ ,  $R_{BI}$ ) are the source of the thermal noise, shot noise of currents are;  $I_{be}$ ,  $I_{bep}$ ,  $I_{txf}$ - $I_{tzt}$ ,  $I_{tfp}$ - $I_{trp}$ ,  $I_{bex}$  and the flicker noise due to the currents are,  $I_{bep}$ ,  $I_{be}$ . Although the shot noises due to substrate current and avalanche are taken into account, the shot noise correlation between the base and collector currents is not considered, which is the main limitation of the VBIC model. The details of the formulas and derivations can be found in [19].

The MEXTRAM also has four terminals. As detailed in [20], series emitter resistance, constant base resistance, constant collector resistance and variable base resistance ( $R_E$ ,  $R_{Bc}$ ,  $R_{Cc}$ ,  $R_{Bv}$ ) are the sources of thermal noise, shot noise of currents are; main current, collector-emitter saturation current, ideal and non-ideal forward base current, reverse base current, extrinsic current, substrate current, ( $I_N$ ,  $I_S$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{ex}$ ,  $XI_{ex}$ ,  $I_{sub}$ , and  $XI_{sub}$ ) and flicker noise sources are; emitter saturation current, ideal and non-ideal forward base current, reverse base current, extrinsic current ( $I_S$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{ex}$ ,  $XI_{ex}$ ). Similar to the VBIC model, shot noise due to base and collector are not correlated. One also, additional collector current and forward base current shot noise, due to Avalanche [21].

Another widely used and well developed compact model is HICUM. Similar to the VBIC and MEXTRAM models, the noise sources are thermal noise due to series resistances, shot noise due to transfer currents and flicker noise due to base current components injected across base-emitter junction. As reported in [22], there is a correlation between transfer and dynamic base current. Also, the base and collector currents are correlated especially at high frequencies.

## 1.4 Approach

The most important aspect of this thesis is to develop a small-signal and noise models from on-wafer test structures. The frequency range for noise and s-parameters

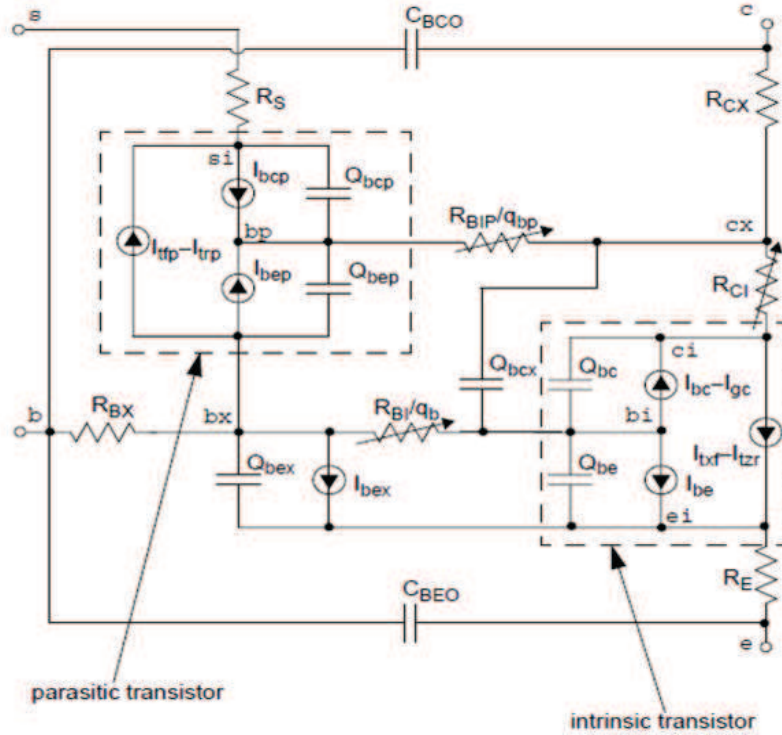


Figure 1.4. VBIC Equivalent Network. Reproduced from [20]

measurements are from DC to 50 GHz and DC to 67 GHz, respectively. The reason of not being able to execute the noise model up to 67 GHz is the lack of the equipment that is capable of performing noise measurement beyond 50 GHz. In order to model the transistors precisely, the effects of the parasitic elements are removed using high frequency open and short de-embedding structures [23]. From the measured and de-embedded s-parameters, the small-signal and the related noise parameters are extracted by using variety of techniques based on DC and RF measurements. As described in the previous section there is a correlation between the base and the collector shot noise currents especially at high frequencies. Therefore, in order to complete the full and accurate model, these effects must be accounted for.

After developing small-signal noise model, a low noise amplifier is going to be designed for the verification of model at microwave frequencies. After verifying the validity of the model, the comparison of the high frequency performance of the ex-

tracted small-signal based LNA and VBIC model based LNA will be examined. The objective of this investigation is to point out the shortcomings of the existing VBIC model especially in the noise figure estimation of the transistors as well as circuits.

## **1.5 Summary**

In this chapter, we have introduced the motivation of this work and its importance in today's technology. Then, since bipolar junction transistors are the basis of HBTs, we briefly discussed the basic principle of BJTs and related energy band gap diagram. Moreover, the fundamental concepts, which provide crucial advantages, of the InP HBT technology were presented. In the last part of the chapter, the importance of the compact models has been emphasized and the models that are most widely used have been discussed. Finally, the compact models have been discussed in terms of noise models. In the next chapter DC properties and RF figure-of-merits of InP HBTs will be discussed. Also, the small-signal equivalent circuit parameters as well as the agreement between measurements and models will be examined.

## CHAPTER 2

# INDIUM-PHOSPHIDE HETEROJUNCTION BIPOLAR TRANSISTORS MODELLING

### 2.1 Introduction

Heterojunction bipolar transistors based on III-V semiconductor materials, require an accurate model in order to optimize the device performance to give the most reliable results for different applications in microwave and millimeter wave frequencies. Recently, considerable analytical [24–27] and numerical [28,29] approaches have been suggested to come up with the best small-signal equivalent circuit representation. As mentioned in the first chapter of the thesis, the main objective of this work is to model the small-signal and noise performance of InP HBTs .

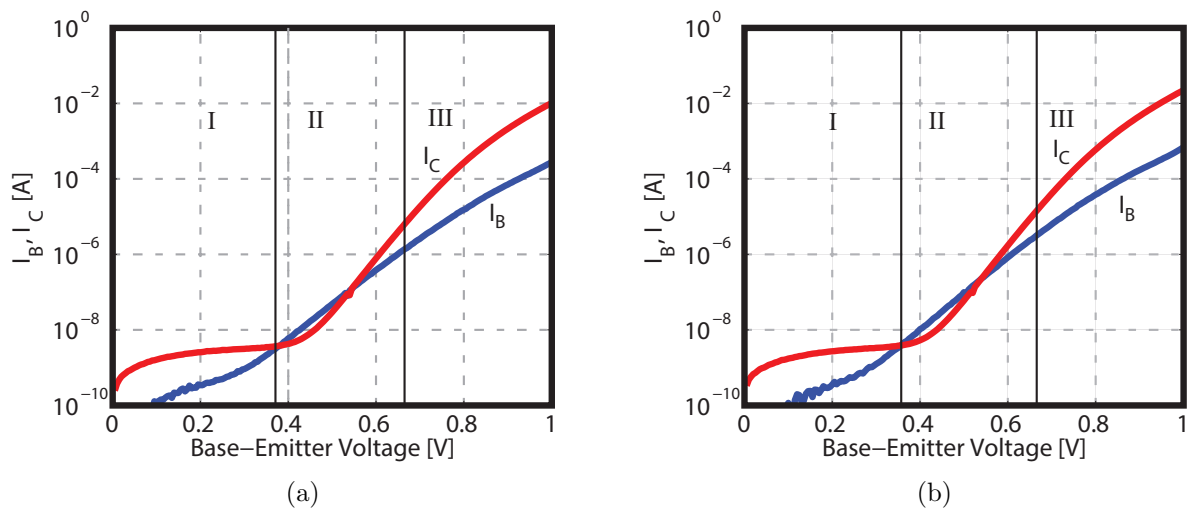
This chapter is devoted the small-signal parameter extraction. The chapter begins with a discussion of the DC performance of InP HBTs and their RF figure-of-merits. Then, the techniques that are commonly used for extraction intrinsic and extrinsic components are presented. The extracted parameter plots and their values with respect to bias and device dimension will be given as well. After extracting all parameters, the agreement between measured and modelled s-parameters for various sized transistors is investigated.

### 2.2 DC Performance of InP HBTs

Before skipping to the modelling procedure of HBTs, the DC performance of the technology will be briefly described. Typical gummel plots for two different sized devices are shown in Figure 2.1. Each plot is divided into three regions. Region-I is



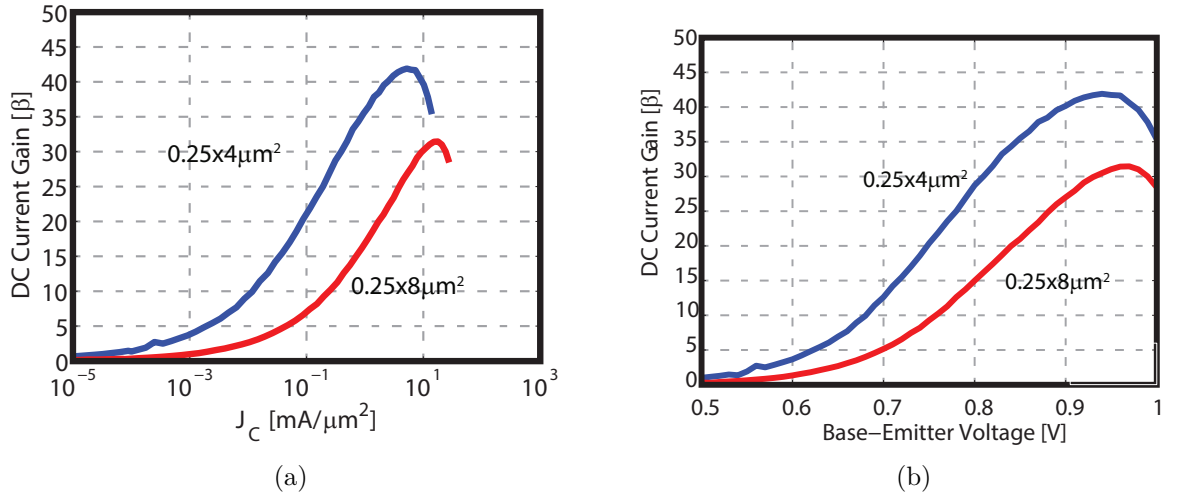
the nonlinear region, which means that leakage currents and low voltage effects are dominant [30]. The second region shows the exponential behaviour of the transistor, where the DC current gain is almost constant in the ideal case. However, practically this is not the case because of the different emission coefficients [30]. In Region-III, high-current and series-resistance effects dominate. For the active-bias measurements, the transistors have been biased to operate in Region-III. Comparison of Fig. 2.1 (a) with 2.1 (b) shows that the base and collector currents scale with emitter area as expected.



**Figure 2.1.** Sample gummel plots (a)  $0.25 \times 4 \mu\text{m}^2$  transistor (b)  $0.25 \times 8 \mu\text{m}^2$  device.

DC current gain is an important figure-of-merit and affects the low frequency noise performance of transistors. Sample plots corresponding to two different device are depicted in Fig 2.2. The peak values observed are 42 and 32, for  $0.25 \times 4 \mu\text{m}^2$  and  $0.25 \times 8 \mu\text{m}^2$  devices, respectively. It should be noted that regardless of the device size, the  $\beta_{DC}$  value of InP HBTs is smaller in comparison to SiGe HBTs. The probable reason for low  $\beta_{DC}$  value is the recombination of the electrons emitted by the emitter with the holes in base terminal meaning that not all electrons are able to reach to the base-collector junction [13]. In fact, due to the high levels of base

doping required to realize a low base resistance despite the low hole mobility in the base, the base current is dominated by this recombination component. Another likely reason can be an increase in hole injection from the base to collector meaning that base gets wider. Thus, the base transit time increases and it is therefore, the current gain degrades [31].



**Figure 2.2.** Beta versus collector current density and  $V_{BE}$ . (a)  $\beta_{DC}$  vs  $J_C$  (b)  $\beta_{DC}$  vs  $V_{BE}$  for  $0.25 \times 4 \mu\text{m}^2$  and  $0.25 \times 8 \mu\text{m}^2$  devices.

### 2.3 RF Figures-of-Merit

The high frequency performance of transistors is often described by the current gain cut-off frequency ( $f_t$ ) and the unilateral power gain cut-off frequency or maximum oscillation ( $f_{max}$ ) frequency. Typically, these figure-of-merits are determined from the extrapolation of unilateral and AC current gain that are based on measured s-parameters. However, dependency of these parameters to the circuit elements should also be kept in mind. These metrics can be approximated in terms of circuit parameters as,

$$f_t \approx \frac{1}{2\pi\tau_d} \quad (2.1)$$

and,

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi R_b C_{bc}}}. \quad (2.2)$$

where,  $\tau_d$  is transit time,  $R_b$  is the associated total base resistance and  $C_{bc}$  is the total base-collector capacitance.

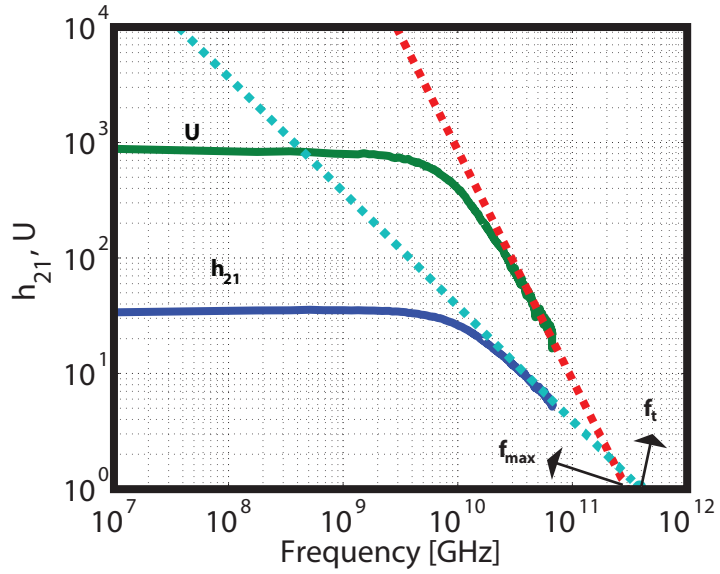
From Equations 2.1 and 2.2, the dependence of  $f_{max}$  on  $f_t$  can be seen as it is proportional to the square root of  $f_t$ .  $f_t$  can also be approximated by extrapolating the AC current gain from the measured s-parameters by assuming 20 dB/decade roll-off with respect to frequency. Likewise,  $f_{max}$  can be extrapolated from unilateral power gain when plotted with respect to  $\sqrt{f}$ . The formulas used in determination of these parameters are shown below [32]

$$h_{21} = \frac{Y_{21}}{Y_{11}} \quad (2.3)$$

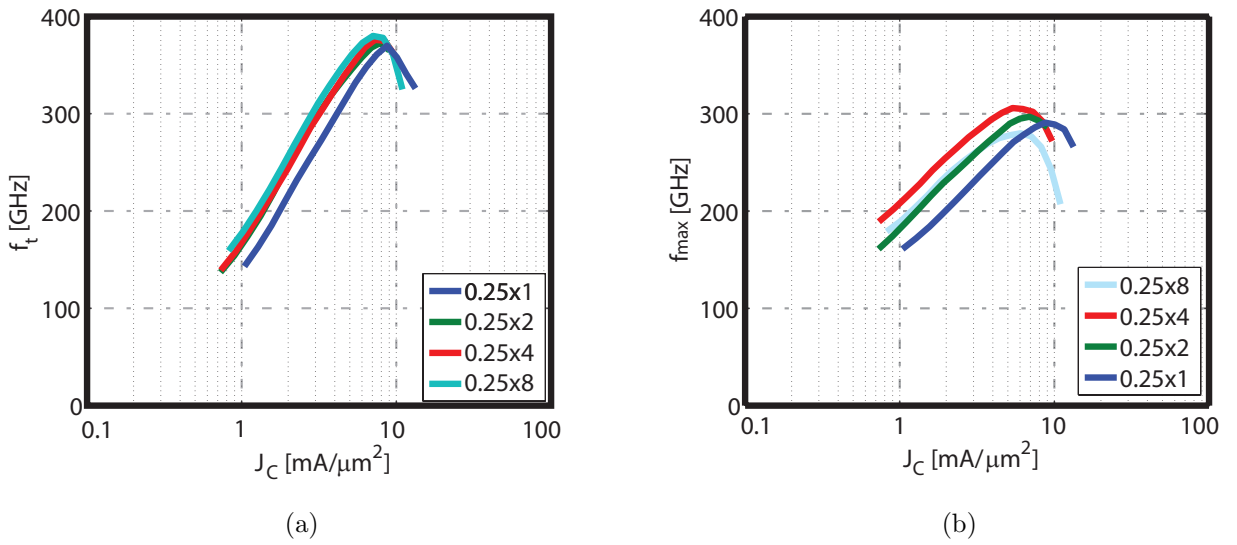
and,

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(\Re\{Y_{11}\} \Re\{Y_{22}\} - \Re\{Y_{12}\} \Re\{Y_{21}\})}. \quad (2.4)$$

A sample plot showing the extrapolation of  $f_t$  and  $f_{max}$  from AC current and unilateral gain is reported in Fig 2.3. From the graph,  $f_t$  and  $f_{max}$  can be easily extracted by extrapolating  $h_{21}$  and  $U$ . By following the same procedure, the extracted  $f_t$  and  $f_{max}$  values are plotted versus collector current density (See Fig 2.4). As seen from these plots, the devices have a peak  $f_t$  value in the range of 370-380 GHz. Regarding  $f_{max}$ , the peak value is more than 300 GHz for the  $0.25 \times 4 \mu\text{m}^2$  device whereas the other devices with  $0.25 \times 8 \mu\text{m}^2$  and  $0.25 \times 2 \mu\text{m}^2$  and  $0.25 \times 1 \mu\text{m}^2$  emitter areas have a bit lower than 300 GHz peak values. An important note is that, in extraction of  $f_t$  and  $f_{max}$ , parasitic effects have been removed using an open/short de-embedding method which will be discussed later on.



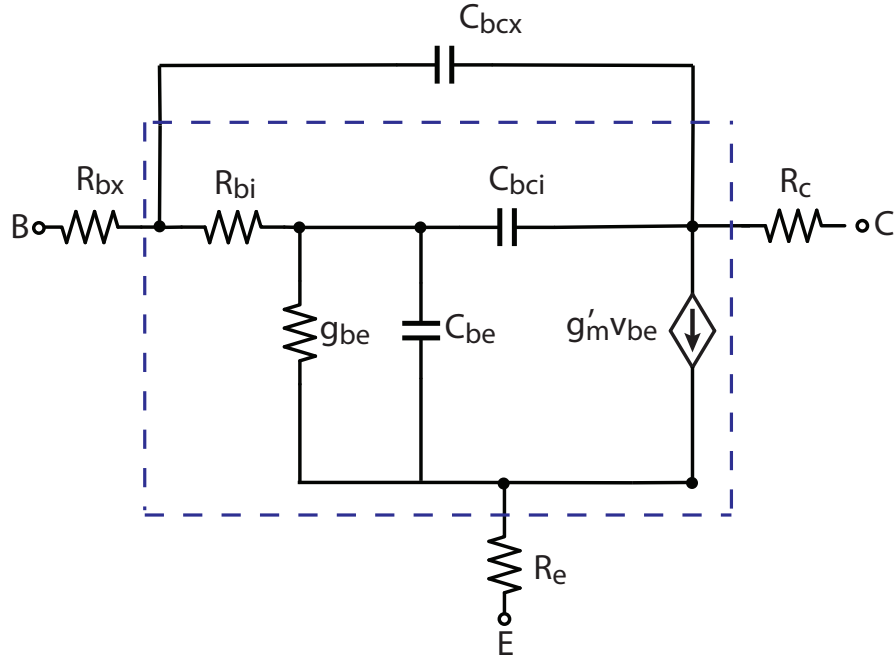
**Figure 2.3.** Unilateral and AC current gain. The blue line correspond to  $h_{21}$  whereas the green line belongs to  $U$



**Figure 2.4.** Sample  $f_t$  and  $f_{max}$  plots. (a)  $f_t$  (b)  $f_{max}$  when sketched versus collector current density ( $J_C$ ) for four different size of transistors.

## 2.4 Small-Signal Modeling

In the analysis of the high frequency circuits using HBTs, there is a necessity of having a valid and accurate equivalent model. For a decent equivalent circuit, the



**Figure 2.5.** The hybrid  $\pi$ -model small signal equivalent circuit consists of two parts, intrinsic and extrinsic.

extraction technique must be based on the physical structure of the devices. In this work, all small-signal parameters are extracted from different sets of measurements such as cold-bias, active-bias, overdriven base current condition, (where the base-emitter and base-collector junctions are forward-biased, and DC measurements. The HBT equivalent circuit is shown in Figure 2.5.

There are nine parameters to be extracted in order to create a precise model. The equivalent circuit is divided into two parts, one of which is bias independent and includes the extrinsic base resistance ( $R_{bx}$ ), the emitter resistance ( $R_e$ ), the collector resistance ( $R_c$ ), and the extrinsic base-collector capacitance ( $C_{bcx}$ ). The bias dependent portion of the circuit includes the intrinsic base resistance ( $R_{bi}$ ), the base-emitter capacitance ( $C_{be}$ ), the intrinsic base-collector capacitance ( $C_{bci}$ ) the base-emitter conductance ( $g_{be}$ ) and the transconductance ( $g_m$ ).

Prior to skipping to the description of parameter extraction in detail, there is an important concept called de-embedding that should be explained. In order to

make a transistor measurable, it has to be surrounded with bondpads for contacting and feedlines for biasing purposes. These bondpads and feedlines can be modeled as shunt capacitors and series inductors. For accurate and reliable extraction, the effect of these bondpads and feedlines must be removed in order to get the actual parameters of the Device-Under-Test (DUT). The process of removing these parasitics is called de-embedding. In this work, an open/short de-embedding procedure is used [23]. The associated matlab code is provided in Appendix A of the thesis.

The parameter extraction procedure is as follow:

1. Removal the effect of bondpads and feedlines.
2. Extraction of the emitter resistance using the open-collector method.
3. Extraction of the extrinsic base and collector resistances using the over-driven base current conditions.
4. Removal the extracted resistance to obtain the bias dependent intrinsic part.
5. Extraction of intrinsic elements using the forward active-bias measurements.

The extraction procedure has been used to determine the parameters of four different size of transistors from various reticules within the wafer. InP HBTs were measured on-wafer and scattering parameters were obtained with an Agilent N5247A-029 VNA over the frequency range of 10 MHz-67 GHz. The system is calibrated with known standards using on-wafer Short-Open-Load-Thru (SOLT) and Thru-Reflect-Line calibration routines.

#### **2.4.1 Extraction of the Emitter Resistance**

The extraction of parameters starts with the emitter resistance since it has a significant influence on the remaining part of the circuit. A variety of methods can be used to find  $R_e$ , including forward active-bias measurements, gummel measurements,

and open-collector measurements. From the observation of a large quantity of data, it was seen that the open-collector method gives the most reliable result among the other techniques described in [3].

As detailed in [33], in the open-collector method, a current source is applied to the base node of transistor while the collector current is forced to zero. Under such conditions, both the base-emitter and the base-collector junctions are forward biased, meaning that the device is in the saturation regime. As detailed in [10], the collector saturation voltage expression can be approximated as,

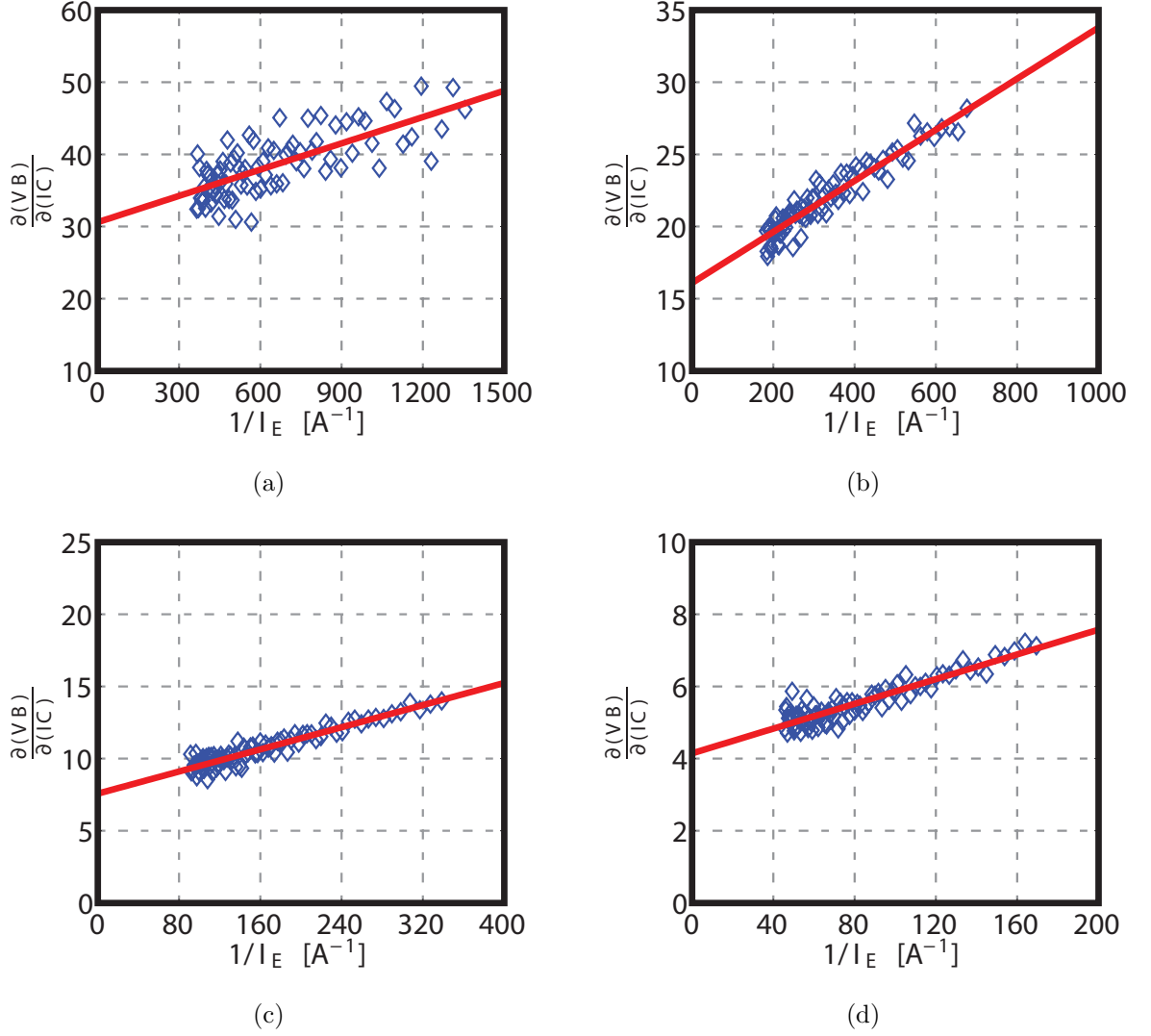
$$V_C \approx I_B R_e + V_T \ln \left\{ \left( \frac{I_B}{I_{C0}} \right)^{n_c} \left( \frac{I_{BR0}}{I_B} \right)^{n_{br}} \right\}. \quad (2.5)$$

where,  $V_T = \frac{kT}{q}$ ,  $n_c$  is the collector current ideality factor and  $I_{BR0}$  and  $n_{br}$  are the saturation coefficient and ideality factor respectively, associated with the base-emitter component of the base current [10].

By taking the derivative of the both sides with respect to  $I_B$ , we find,

$$\left. \frac{\partial V_C}{\partial I_B} \right|_{I_C=0} = R_e + \frac{V_T}{I_B} (n_c - n_{br}) \quad (2.6)$$

From the equation shown above,  $R_e$  can be extrapolated from the y-intercept point of the plots (see Figure 2.6) by curve fitting  $\partial V_C / \partial I_B$  as a function of  $1/I_B$ . From Figure 2.6 shown above, the  $R_e$  values are 30.6  $\Omega$ , 16.1  $\Omega$ , 7.7  $\Omega$  and 4.1  $\Omega$  for the devices with  $0.25 \times 1 \mu\text{m}^2$ ,  $0.25 \times 2 \mu\text{m}^2$ ,  $0.25 \times 4 \mu\text{m}^2$  and  $0.25 \times 8 \mu\text{m}^2$  emitter area, respectively. From a scaling point of view, the extracted values seem reasonable, as the resistance value is inversely proportional to device size, meaning that the doubled size device has half resistance value compared to the smaller device. Statistical information can be found in Table 2.1.



**Figure 2.6.** Extraction of emitter resistances for four devices. (a) The smallest size transistor that has  $0.25 \times 1 \mu\text{m}^2$  emitter area, (b) The transistor has  $0.25 \times 2 \mu\text{m}^2$  emitter area, (c) The transistor has  $0.25 \times 4 \mu\text{m}^2$  emitter area and (d) The largest transistor with the dimension of  $0.25 \times 8 \mu\text{m}^2$  emitter area. Solid lines correspond to fitting and diamond markers belong to the obtained data points.

#### 2.4.2 Extraction of the Extrinsic Base Resistance

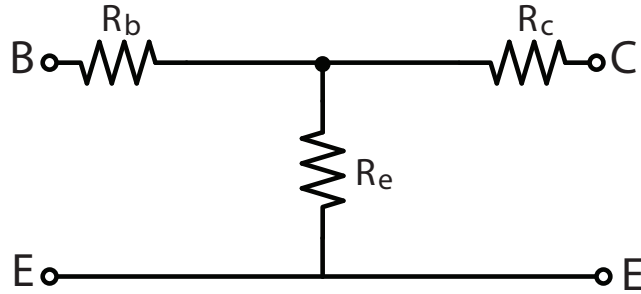
Base resistance is one of the most important parameters in device characterization, since it has a great impact on the high frequency and noise performance of the device. For this reason, special attention must be paid in order to avoid any potential inaccuracy. From the small-signal equivalent circuit shown in Figure 2.5, it can



**Table 2.1.**  $R_e$  values with respect to device dimension

	Emitter Area( $\mu\text{m}^2$ )			
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$
	$R_e$ ( $\Omega$ )			
Reticule-1	30.1	16.1	7.7	4.1
Reticule-2	25.7	14.3	7.2	4.5
Reticule-3	30.2	15.3	7.6	4.6
Reticule-4	28.7	14.5	5.5	4
Mean	28.8	15.1	7.03	4.3
Standard Deviation	2.2	0.83	1.05	0.29

be seen that the base resistance is divided into two parts. The extrinsic portion is extracted from the over-driven base bias condition, where  $V_B$  is swept from 0.9 V to 1.05 V while  $V_C$  is held at zero voltage. Under such circumstances, the effect of bias on the intrinsic base resistances is almost negligible because of the high base-current density. The corresponding circuit becomes as Figure 2.7.



**Figure 2.7.** Corresponding equivalent for the over-driven base current condition. This circuit is valid for the transistors operated in the base current range of 5mA-25mA depending on the device size.

$R_{bx}$  can be determined by plotting the real part of  $(Z_{11} - Z_{12})$  with respect the inverse of  $I_B$ . The y-intercept point gives the  $R_{bx}$  by curve fitting as  $I_B \rightarrow \infty$  [34]. Sample plots are shown in Fig 2.8 for different sized devices. The determined values

**Table 2.2.**  $R_{bx}$  values with respect to device dimension

	Emitter Area( $\mu\text{m}^2$ )			
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$
	$R_{bx}$ ( $\Omega$ )			
Reticule-1	8.9	7.9	6.6	5.8
Reticule-2	8.8	7.4	6.2	5.6
Reticule-3	9.1	7.9	6.3	5.4
Reticule-4	8.8	7.4	6	4.9
Mean	8.9	7.65	6.28	5.43
Standard Deviation	0.14	0.29	0.25	0.39

of  $R_{bx}$  are  $9.1 \Omega$ ,  $7.9 \Omega$ ,  $6.3 \Omega$  and  $5.4 \Omega$  for  $0.25 \times 1 \mu\text{m}^2$ ,  $0.25 \times 2 \mu\text{m}^2$ ,  $0.25 \times 4 \mu\text{m}^2$  and  $0.25 \times 8 \mu\text{m}^2$  devices, respectively.

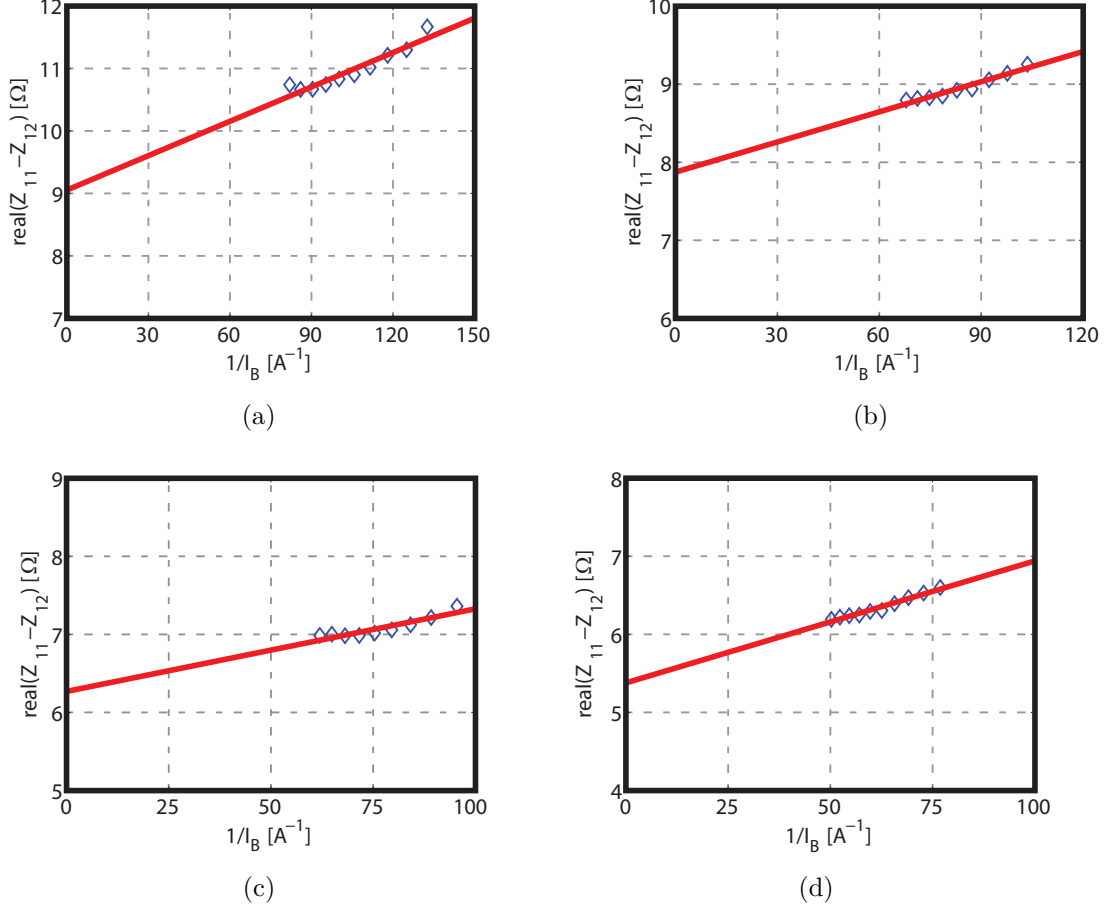
Determined values of  $R_{bx}$  from different reticules with the mean and the standard deviation info are expressed in Table 2.2. As seen due to the distributed nature of base resistance, the scalability is poor.

### 2.4.3 Extraction of the Collector Resistance

The collector resistance is also extracted from s-parameters while the device is under the over-driven base current operation. Referring back to Fig. 2.7,  $R_c$  is determined from the y-intercept point when  $I_B \rightarrow \infty$  while the real part of  $(Z_{22}-Z_{12})$  is plotted as a function of  $1/I_B$ . It was observed that  $R_c$  does not have a great impact on the overall extracted small-signal equivalent circuit. Sample plots are shown in Fig.2.9.

$$R_c = \Re \{Z_{22} - Z_{12}\} \quad (2.7)$$

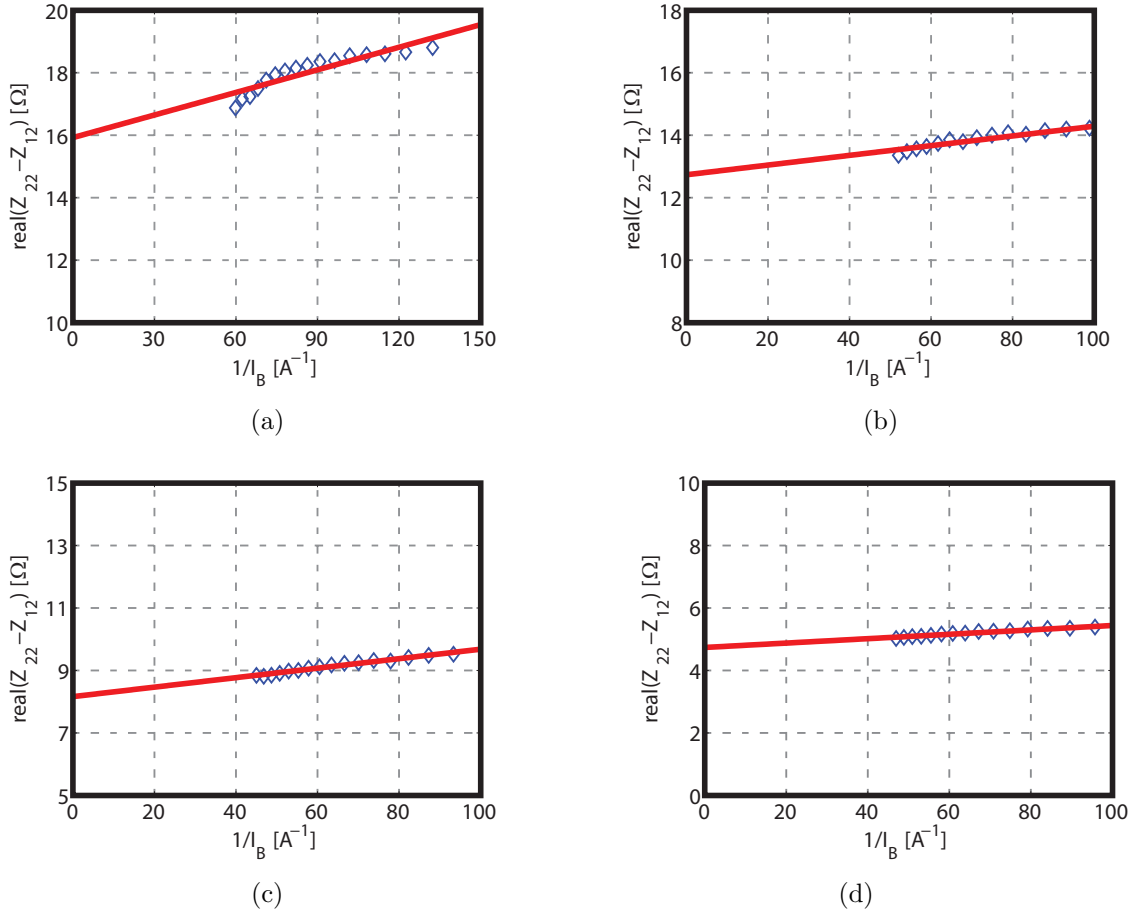
Extracted  $R_c$  and the mean and the standard deviation values correspond to different reticules are presented in Table 2.3.



**Figure 2.8.** Extraction of  $R_{bx}$  of four devices. (a)  $0.25 \times 1 \mu\text{m}^2$  device, (b) The transistor has  $0.25 \times 2 \mu\text{m}^2$  emitter area, (c)  $0.25 \times 4 \mu\text{m}^2$  transistor and (d)  $0.25 \times 8 \mu\text{m}^2$  device. Solid lines correspond to fitting and diamond markers belong to the obtained data points

#### 2.4.4 Determination of the Base-Collector Total Capacitance

The base-collector capacitance is usually determined by using cold-bias measurements meaning the transistor is under cut-off mode [35,36]. We have observed that there is no significant difference between the extracted  $C_{bc}$  value obtained using active-bias measurements, where the transistor is forward biased, and cold-bias measurements. In this work, the total  $C_{bc}$  is determined from measured s-parameters when the transistor is under active-bias operation, as detailed in [37]. The expression is shown below.



**Figure 2.9.** Extraction of  $R_c$  for four devices. (a)  $0.25 \times 1 \mu\text{m}^2$  device, (b) The transistor has  $0.25 \times 2 \mu\text{m}^2$  emitter area, (c)  $0.25 \times 4 \mu\text{m}^2$  transistor and (d)  $0.25 \times 8 \mu\text{m}^2$  device. Solid lines correspond to fitting and diamond markers belong to the obtained data points. It should be noted that the data points are obtained from the bias conditions where  $V_{BE}$  is swept from 0.9 to 1.05 V. For the sake of consistency this interval is used for all devices.

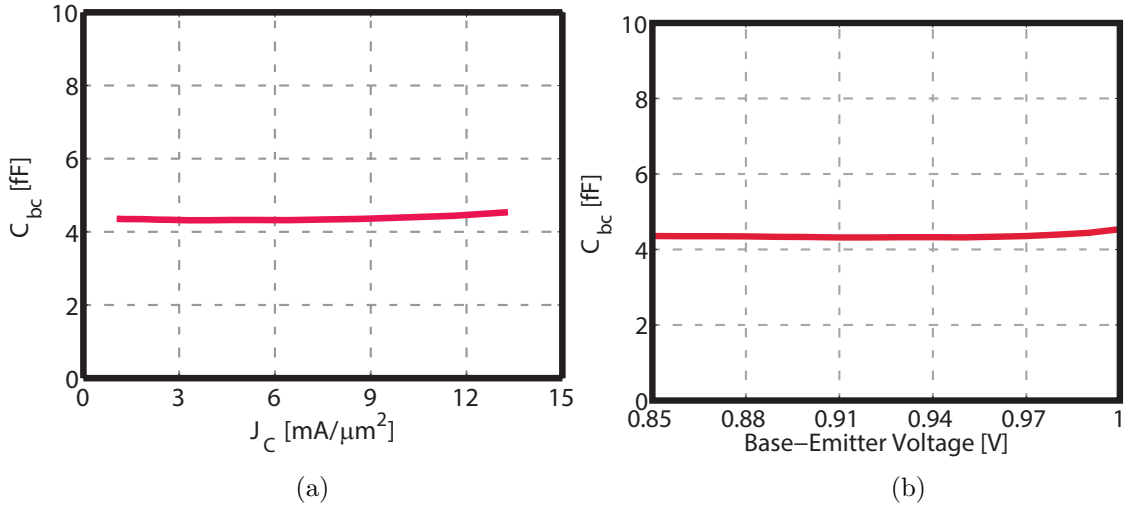
**Table 2.3.**  $R_e$  values with respect to device dimension

	Emitter Area( $\mu\text{m}^2$ )			
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$
	$R_e$ ( $\Omega$ )			
Reticule-1	16.8	12.2	8.7	4.7
Reticule-2	15.9	12.7	8.2	4.8
Reticule-3	15.7	11.9	8.2	4.8
Reticule-4	16.4	12.7	8.4	5.3
Mean	16.2	12.4	8.4	4.9
Standard Deviation	0.5	0.4	0.24	0.29

$$C_{bc} = C_{bcx} + C_{bci} \approx -\frac{\Im\{Y_{12}\}}{\omega} \quad (2.8)$$

$C_{bc}$  is weakly depend on the bias point as demonstrated in Fig 2.10, it is almost insensitive to the change in bias which is the proof of the fact that only a diffusion capacitance depends upon the voltage across the terminals whereas a depletion capacitance or a junction capacitance is weakly bias dependent. Thus, unlike the access resistances,  $C_{bc}$  should be extracted at a fixed base-collector voltage. For this work, we set the base-collector voltage to 0 V for all measurements. Sample plots showing the determination of  $C_{bc}$  at a fixed bias point, where  $J_C=4\text{mA}/\mu\text{m}^2$ , appears in Fig. 2.11.

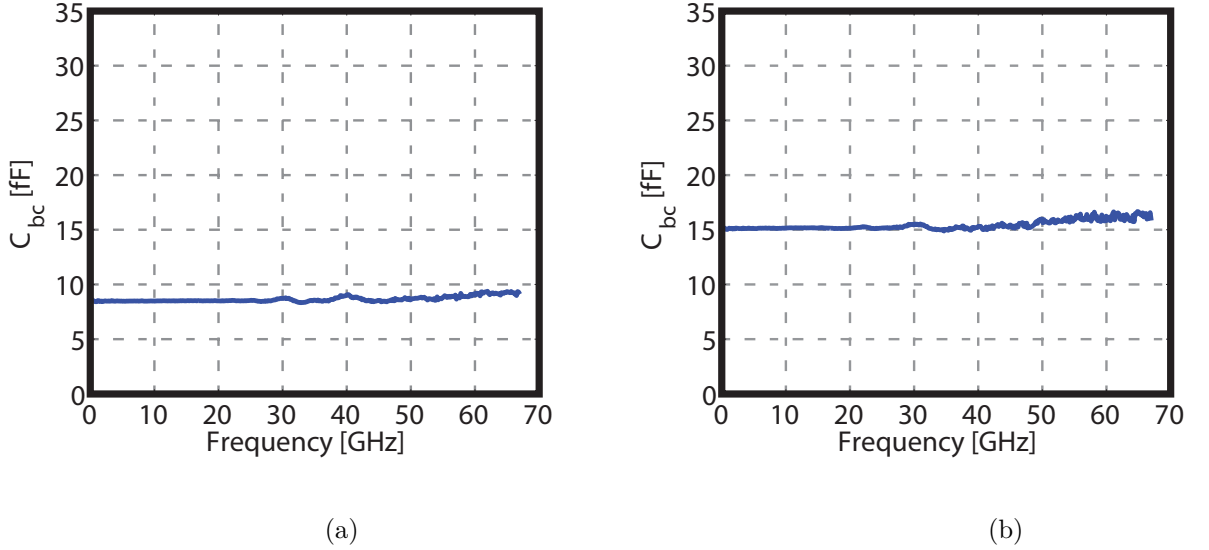
$C_{bc}$  can be determined at low frequency from the y-intercept point when  $\omega \rightarrow 0$  from the range in which the  $C_{bc}$  versus frequency curve has a flat characteristic. From the plots (see Fig. 2.11) it can be clearly observed that the base-collector capacitance value does not fluctuate especially at frequencies below 30 GHz. This parameter has been extracted by taking the mean of the curve in the frequency band between 1-30 GHz for all transistors. Regarding the extracted values, a larger device has a bigger capacitance value. This is expected since  $C_{bc}$  proportional to the effective emitter



**Figure 2.10.** Example of data showing the  $C_{bc}$  as a function of voltage and current of  $0.25 \times 1 \mu\text{m}^2$ . (a)  $C_{bc}$  versus  $J_C$  (b)  $C_{bc}$  versus  $V_{BE}$ .

area. The extracted values are 8.6 fF for  $0.25 \times 4 \mu\text{m}^2$  device whereas it is 15 fF for doubled size device. To explore the statistics provided in Table 2.4 in terms of scaling, scaling is better while the device dimension gets larger. One probable reason of this lack of scalability between smaller transistors can be the fringing capacitance from the side wall of adjacent layers.

Once again it is helpful to point out that the  $C_{bc}$  is independent of  $V_{BE}$ , whereas it strongly dependent upon  $V_{BC}$ . Also, it should be emphasized that four sets (each set has four transistors with different emitter area) of transistors are modelled at a fixed but different  $J_C$  value for each reticules. Moreover,  $V_{BC}$  is kept at zero voltage for forward active-bias measurements while each device is biased to assure a desired collector current density. Therefore, instead of providing the specific  $V_{BE}$  values which may vary from device to device to obtain this fixed collector current density,  $J_C$  is given in the table.



**Figure 2.11.** Example of data used for extraction of  $C_{bc}$  (a)  $0.25 \times 4 \mu\text{m}^2$  device, (b) the transistor has  $0.25 \times 8 \mu\text{m}^2$  emitter area. The curves represent  $C_{bc}$  with respect to frequency while  $V_{BC}=0$ .

**Table 2.4.**  $C_{bc}$  values at a single collector current

	Emitter Area( $\mu\text{m}^2$ )				
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$	$J_C$
	$C_{bc}$ (fF)				$\text{mA}/\mu\text{m}^2$
Reticule-1	4.2	5.6	8.4	14	4.8
Reticule-2	4.3	5.5	8.3	14.4	4.4
Reticule-3	4.3	5.7	8.3	14.8	2
Reticule-4	3.6	4.8	8.6	15	4

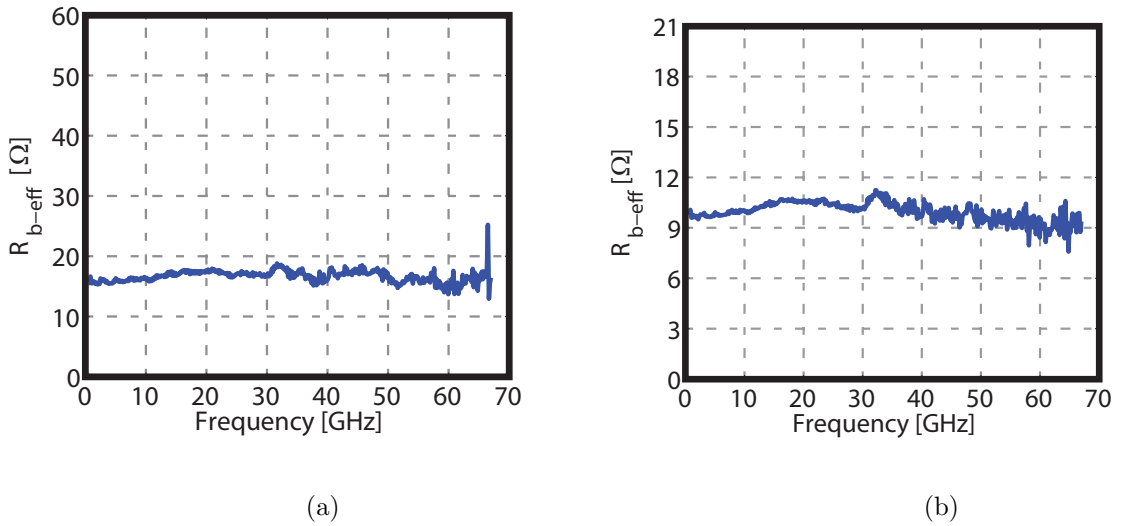
#### 2.4.5 Extraction of The Effective Base Resistance

The extraction of the effective base resistance has received an immense deal of attention. It should be noted that the effective base resistance is not equal to the summation of  $R_{bx}$  and  $R_{bi}$  (see Eq. 2.10) as they are separated by  $C_{bcx}$ . A Variety of methods to determine  $R_{b-eff}$  have been described in the literature [38–40]. Unlike  $R_{bx}$ , the effective base resistance must be evaluated at a single bias point because of the distributed nature of the intrinsic resistance across the base emitter diode [10,37,

41]. After extracting  $R_e$ ,  $R_c$  and  $R_{bx}$ , they are removed from the overall circuit in order to obtain the bias-dependent intrinsic circuit. Then,  $R_{b-eff}$  is extracted from measured s-parameters, using the formula shown below, when the device is under forward-active operation.

$$R_{b-eff} = \Re \{Z_{11} - Z_{12}\} \quad (2.9)$$

As described above,  $R_{b-eff}$  is extracted at single fixed bias point. Figure 2.12 shows the change in the extracted  $R_{b-eff}$  with respect to frequency. If we compare these two plots we can clearly see that larger device has approximately half resistance value of the larger device. This is expected, since, the base resistance of a device is inversely proportional to the its effective emitter area.

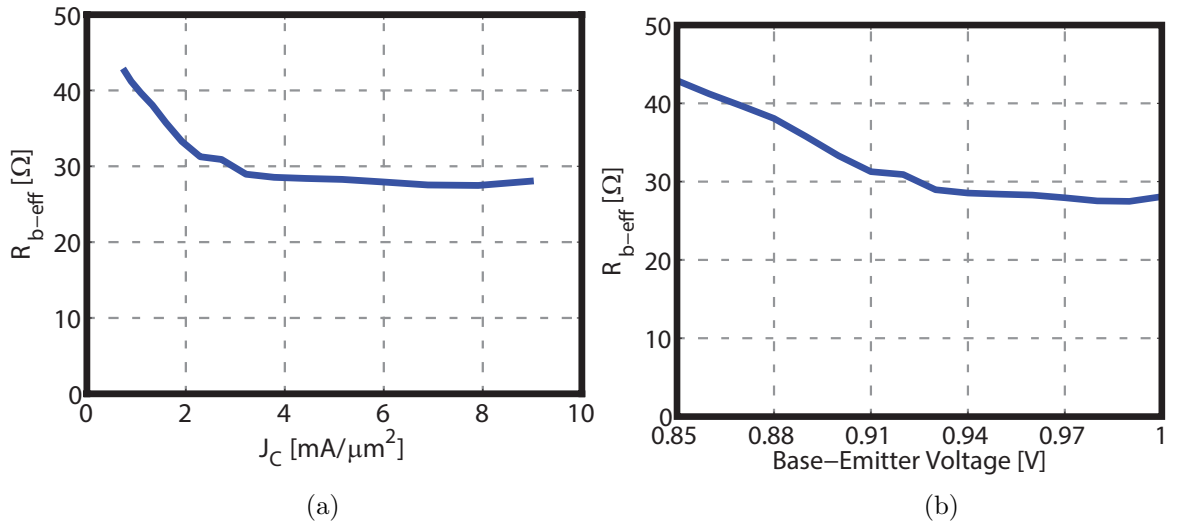


**Figure 2.12.** Sample plots used to determine  $R_{b-eff}$  for the transistors having the effective emitter area of (a)  $0.25 \times 4 \mu\text{m}^2$ , and (b)  $0.25 \times 8 \mu\text{m}^2$ .

The change in  $R_{b-eff}$  when plotted as a function of base-emitter voltage and collector current density for a single  $0.25 \times 2 \mu\text{m}^2$  transistor is indicated in Fig. 2.13. As seen from the figures,  $R_{b-eff}$  decreases as  $J_C$  or  $V_{BE}$  goes up. The critical bias



point occurs at  $J_C = 4\text{mA}/\mu\text{m}^2$ . This bias point is also the optimum current density where the transistors have the best noise figure performance (see Section 3.3.4).



**Figure 2.13.** The variation of  $R_{b-eff}$  with respect to (a) collector current density, and (b) base-emitter voltage. Data belongs to single transistor.

#### 2.4.6 Determination of Intrinsic Base-Collector Capacitance and Intrinsic Base Resistance

After extracting the effective base resistance and the total base-collector capacitance, the intrinsic base resistance and base-collector capacitance can be evaluated by using the expression reported by Johansen.*et.al* [42].

$$R_{b-eff} = \Re \{Z_{11} - Z_{12}\} \approx R_{bx} + X(I_c) R_{bi}, \quad (2.10)$$

where  $X(I_c)$  the current dependent distribution factor for the base-collector capacitance and it is defined as,

$$X(I_c) = \frac{C_{bi}}{C_{bc}}. \quad (2.11)$$

Thus after algebraic process the expression can be rewritten as,

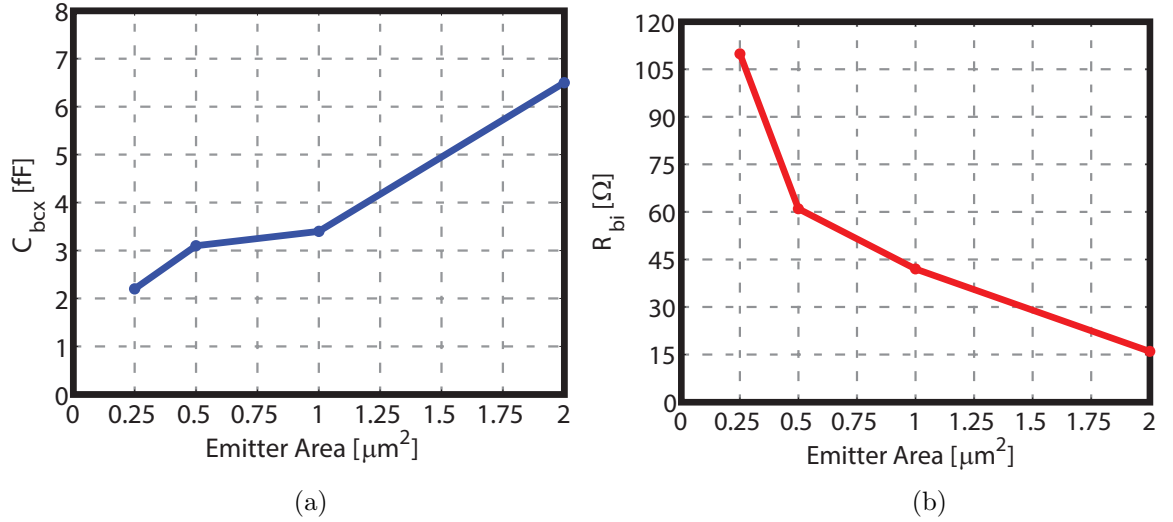
$$C_{bcx} = \left( \frac{R_{bi} + R_{bx} - R_{b-eff}}{R_{bi}} \right) C_{bc}. \quad (2.12)$$

Finally, it needs be pointed out that  $C_{bcx}$  is the most sensitive parameter since it has remarkable influence on the overall noise performance of the equivalent circuit. Hence, this parameter has been optimized by using the equation shown above in such a way that the agreement between measured noise figure and small-signal noise circuit has been maximized. Moreover, this optimization process is done with measuring a single transistor in terms of both s-parameters and noise figure at four different  $J_C$  points. Then, since  $C_{bcx}$  is bias independent, its value is optimized and fixed for all these four points. The corresponding  $R_{bi}$  value for each bias point is calculated using Equation 2.12. The remaining part of data are summarized in Table 2.5. Example plots are shown in Fig. 2.14 and the associated values are shown in Table 2.6.

From the graphs, it can be seen that the resistance value decreases with the increasing value of emitter dimension whereas the capacitance value decreases with

**Table 2.5.**  $R_{bi}$  values at a single bias point

	Emitter Area( $\mu\text{m}^2$ )				
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$	$J_C$
	$R_{bi}$ ( $\Omega$ )				$\text{mA}/\mu\text{m}^2$
Reticule-1	61	29	18	7.8	4.8
Reticule-2	58	28.9	19.4	12	4.4
Reticule-3	50	29	20	12.8	2
Reticule-4	54	27	18.2	10.9	4



**Figure 2.14.** Sample plots showing (a)  $C_{bcx}$ , and (b)  $R_{bi}$  as a function of emitter area for the same collector current density.

respect to the emitter area as expected. The ratio does not scale due to various parameters such as the device noise figure, DC current gain ( $\beta_{DC}$ ), gain etc.

**Table 2.6.**  $C_{bcx}$  values belong to variety of transistors from different reticules

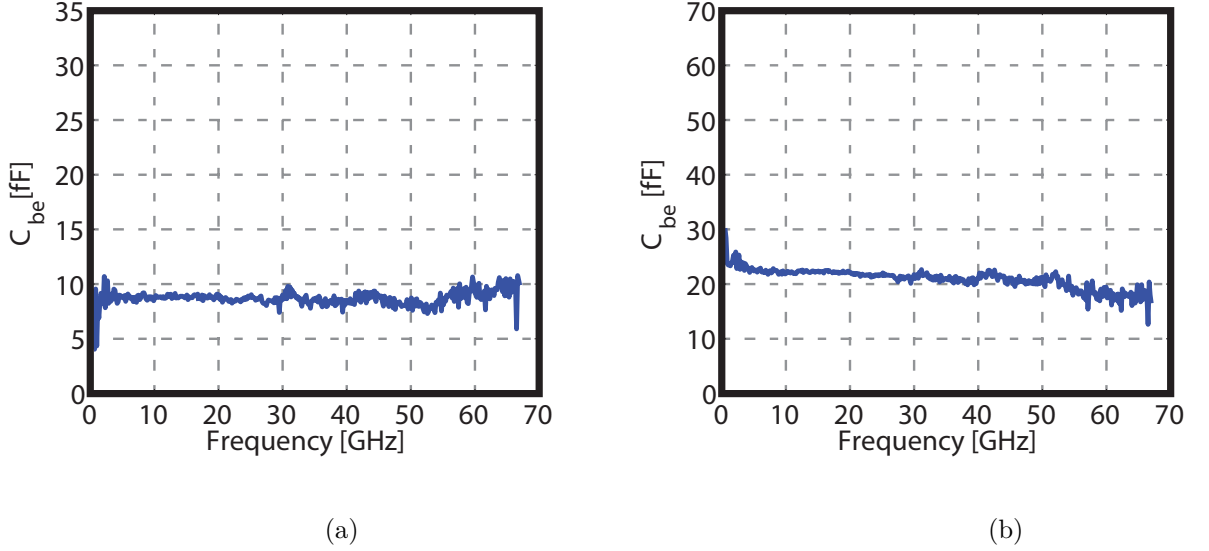
	Emitter Area( $\mu\text{m}^2$ )				
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$	$J_C$
	$C_{bcx}$ (fF)				$\text{mA}/\mu\text{m}^2$
Reticule-1	2.2	3.7	5.5	6.3	4.8
Reticule-2	2.7	3.6	5.3	6.2	4.4
Reticule-3	3.1	3.8	5.8	8.2	2
Reticule-4	2.5	3.1	3.4	6.5	4

#### 2.4.7 Determination of Base-Emitter Capacitance

Similar to the base-collector capacitance, the base-emitter capacitance is also extracted from forward-active region measurements after removal of the extrinsic components. The expression used for the extraction is,

$$C_{be} = \frac{\Im \{Y_{11} + Y_{12}\}}{\omega}. \quad (2.13)$$

Sample plots showing the frequency dependency of  $C_{be}$  appear in Fig. 2.15. As demonstrated in Fig. 2.15,  $C_{be}$  is flat over the majority of the frequency band.

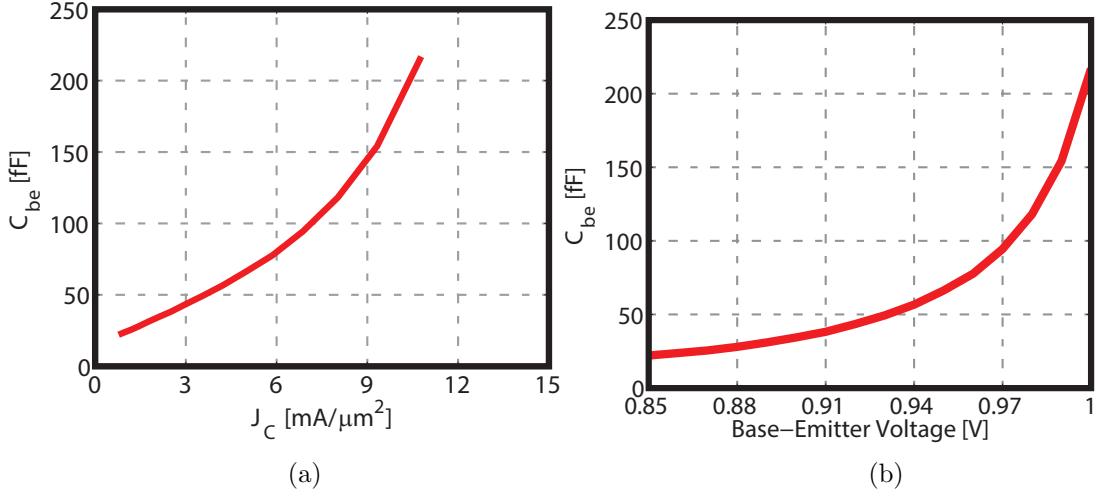


**Figure 2.15.** Determination of the  $C_{be}$  (a)  $0.25 \times 2 \mu\text{m}^2$  device, (b)  $0.25 \times 4 \mu\text{m}^2$  emitter area. The curves represent  $C_{be}$  with respect to frequency.

In contrast to  $C_{bc}$ ,  $C_{be}$  is strongly depend on bias (see Fig. 2.16). This is expected as this a combination of depletion and diffusion capacitances and due to diffusion capacitance part, its value strongly depends on the potential difference across the terminals. The detailed statistical data at a single bias point for each reticule is provided in Table 2.7

#### 2.4.8 Extraction of $g_{be}$ , $g_m$ and $\tau$

The final elements that must be determined to complete the model are the transconductance ( $g_m$ ), the base-emitter conductance ( $g_{be}$ ) and the time delay ( $\tau_d$ ). These elements are extracted from  $Y$  parameters obtained from active-bias s-parameter



**Figure 2.16.** Example of data showing  $C_{be}$  of  $0.25 \times 8 \mu\text{m}^2$  device as a function of voltage and current. (a)  $C_{be}$  versus  $J_C$  (b)  $C_{be}$  versus  $V_{BE}$ .

**Table 2.7.**  $C_{be}$  values belong to variety of transistors from different reticules

	Emitter Area( $\mu\text{m}^2$ )				
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$	$J_C$
	$C_{be}$ (fF)				$\text{mA}/\mu\text{m}^2$
Reticule-1	9.7	13	23	40	4.8
Reticule-2	9	12.5	21	38	4.4
Reticule-3	4	8.5	19	36	2
Reticule-4	11	16	28	66	8

measurements. The expressions as detailed in [43], are used in the determination of these parameters. It should be noted that after removing, the extrinsic components and  $R_{bi}$ , these parameters can be determined using the following expressions,

$$g_m \approx |Y_{21} - Y_{12}|, \quad (2.14)$$

$$\tau_d \approx -\frac{\text{phase} \{Y_{21} - Y_{12}\}}{\omega}, \quad (2.15)$$

and finally,

$$g_{be} \approx \Re \{Y_{11} + Y_{12}\}. \quad (2.16)$$

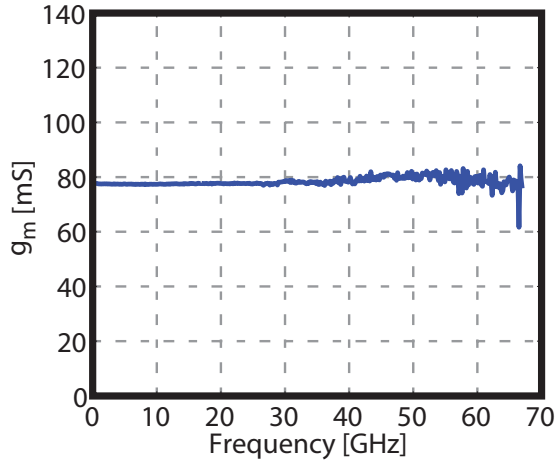
Example plots showing the change in  $g_m$  and  $g_{be}$  with respect to frequency can be seen in Fig. 2.17. Typically, both parameters are extracted from the flat zone at low frequencies. In contrast to resistance, conductance values increases proportionally with the area of the device, as clearly seen from the plots shown in Fig. 2.17. For instance,  $g_m$  is approximately 75 mS for the  $0.25 \times 4 \mu\text{m}^2$  device from reticule-4, whereas the  $0.25 \times 8 \mu\text{m}^2$  device from the same reticule has a transconductance of 174 mS. Similar behaviour can be observed for  $g_{be}$  as well. Extracted values for these two parameters are summarized in the Table 2.8. When we take a look to the trend of both parameters, it is seen that they increase proportionally with the collector current.

**Table 2.8.**  $g_m$ ,  $g_{be}$  values for different bias points

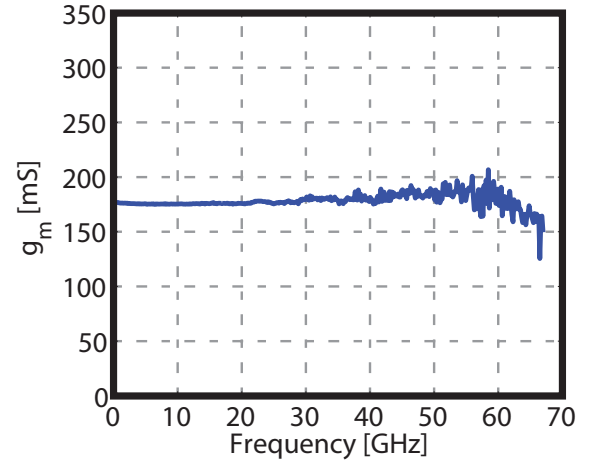
	Emitter Area( $\mu\text{m}^2$ )								
Reticule Number	$0.25 \times 1$	$0.25 \times 2$	$0.25 \times 4$	$0.25 \times 8$					$J_C$
	$g_m$	$g_{be}$	$g_m$	$g_{be}$	$g_m$	$g_{be}$	$g_m$	$g_{be}$	$\text{mA}/\mu\text{m}^2$
	mS								
Reticule-1	29	0.82	47	1.3	95	2.7	115	3.4	4.8
Reticule-2	29	0.59	46	1	92	1.4	129	3.8	4.4
Reticule-3	12	0.29	22	0.54	83	1.6	89	2.57	2
Reticule-4	22	0.55	37	0.93	75	1.9	174	3.65	4

## 2.5 Results and Discussions

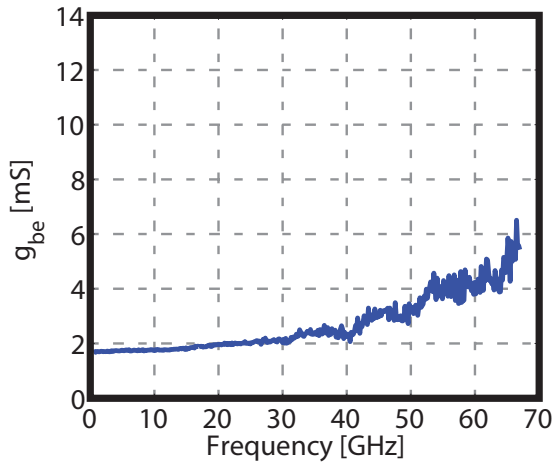
After determining all necessary parameters to create the small-signal equivalent circuit, the agreement between the model and measurements has been investigated. A sample plot showing the comparison of s-parameters is provided in Figure 2.18. There



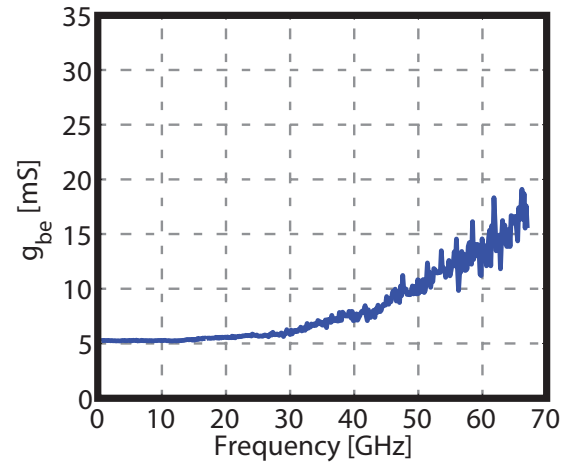
(a)



(b)



(c)



(d)

**Figure 2.17.** Sample plots showing transconductance and base-emitter conductance for four different emitter size devices (a)  $g_m$  of  $0.25 \times 4 \mu\text{m}^2$  device, (b)  $g_m$  of  $0.25 \times 8 \mu\text{m}^2$  device (c)  $g_{be}$  of  $0.25 \times 4 \mu\text{m}^2$  device and (d)  $g_{be}$  of  $0.25 \times 8 \mu\text{m}^2$  device. Both parameters shown in this plots are extracted at the same  $J_C$

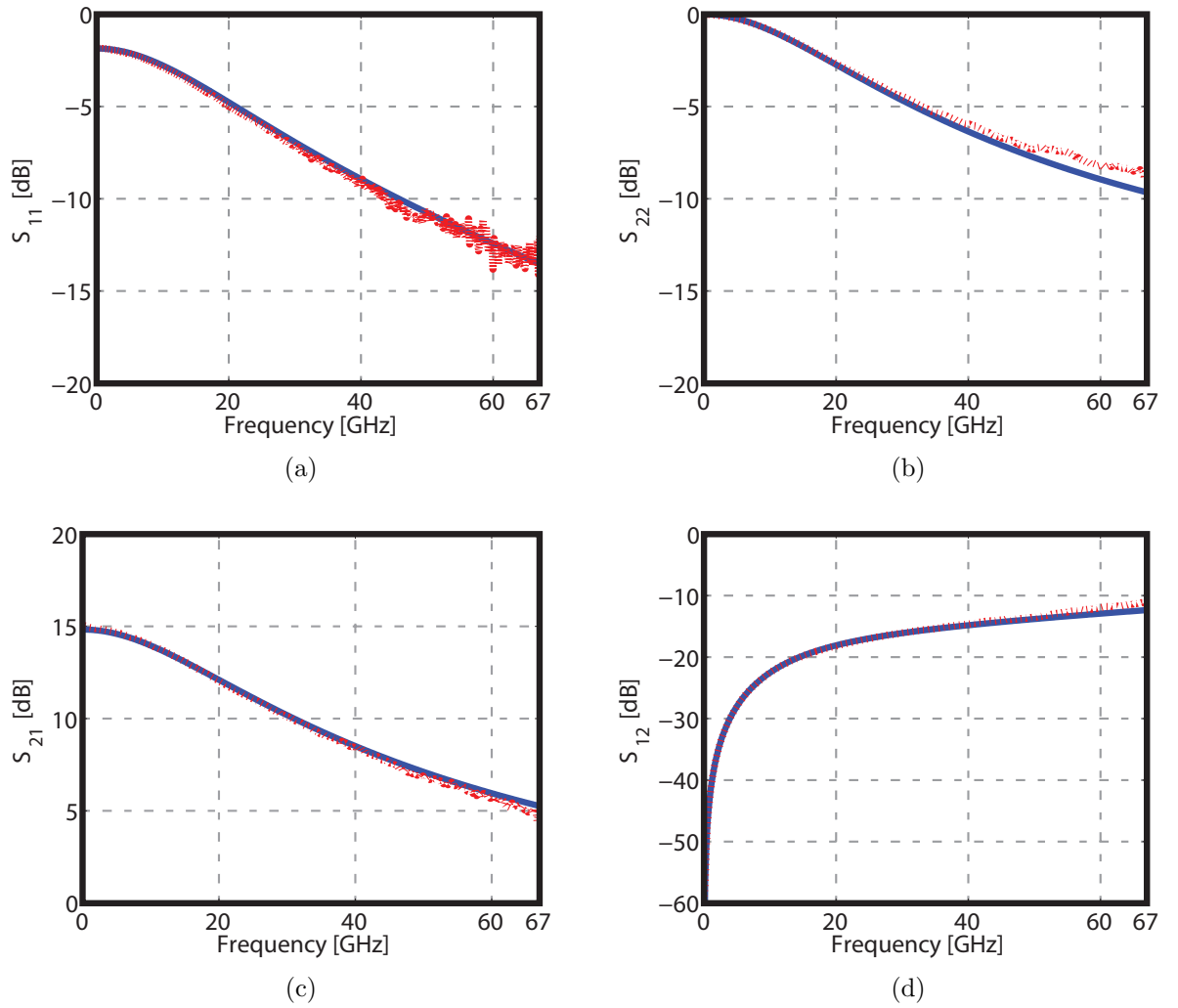
is an excellent agreement between measured and modelled s-parameters over the frequency range of interest. Another way of looking the correlation of measurement and model is to plot all these parameters on the smith chart and polar chart, in which the complex form of  $S_{11}/S_{22}$  and  $S_{21}/S_{12}$  can be sketched. Another set of data belong

to two different devices are also shown in Fig 2.19. Again the agreement between measurement and model is quite good for both devices.

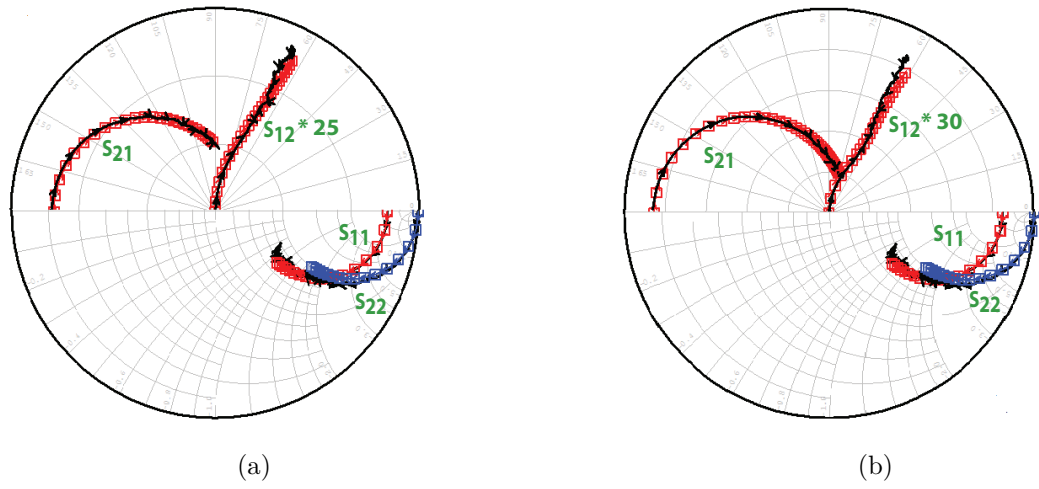
## 2.6 Summary

In this chapter, we started from the DC properties of InP HBTs and presented the fundamental plots such as the  $\beta_{DC}$  and gummel curves. Then,  $f_t$  and  $f_{max}$  have been discussed. The rest of the chapter was devoted to the small-signal parameter extraction procedure. The behaviour of each element was discussed in terms of either the frequency dependency or bias dependency. After determining all parameters for the small-signal equivalent circuit, the correlation between model and measurements was investigated. In the next chapter of this work, the noise performance and the noise modelling concepts will be examined.





**Figure 2.18.** S-parameter comparison of a single  $0.25 \times 8 \mu\text{m}^2$  device in cartesian coordinates. (a)  $S_{11}$ , (b)  $S_{22}$ , (c)  $S_{21}$ , and (d)  $S_{12}$ . Solid and blue lines correspond to model and dashed red lines belong to measured s-parameters.



**Figure 2.19.** S-parameter Comparison on Smith and Polar Charts. Top semi chart displays  $S_{21}$  and  $S_{12}$  curves whereas bottom semi chart shows  $S_{11}$  and  $S_{22}$  in both plots. (a)  $0.25 \times 4 \mu\text{m}^2$ , (b)  $0.25 \times 8 \mu\text{m}^2$  device.

## CHAPTER 3

### NOISE PERFORMANCE

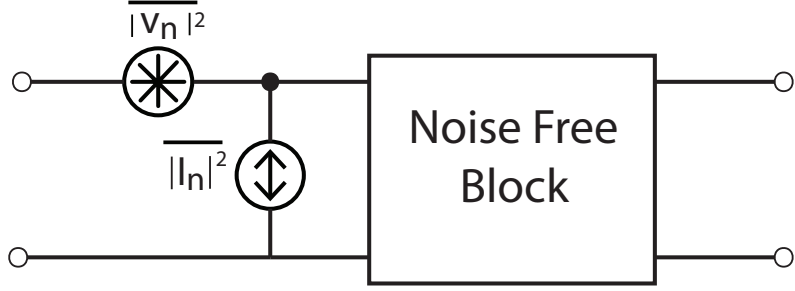
#### 3.1 Introduction

In electronics, unwanted fluctuations due to the random motion of electrons and holes are observed when transmitting or receiving information in a system. These fluctuations are called *Noise*. Noise is observed over both active and passive electronic devices and can be detected on voltages or currents. In communication systems it is crucial to transfer and receive the desired data in the most accurate and effective way. For this reason, noise has received an enormous deal of attention by researchers. The main objective is to increase signal-to-noise ratio (*SNR*), which is the ratio of actual signal to the detected noise in the system. Hence, for the design and optimization of low noise circuits, the noise behaviour of the devices must be accurately described by a precise noise measurement.

In this chapter the basics of noise in HBTs is covered first. The basic type of noise and the sources of noise in HBTs is also discussed. Then, the noise measurement methods and the setup used in this work are presented. The noise performance of different size of transistors is also demonstrated. Finally, the noise modelling of InP HBTs that have different emitter sizes is shown. The agreement between measured and modelled noise figure is investigated, and the noise parameter plots are displayed.

#### 3.2 Noise in HBTs

Transistors are the key components in receiver systems since they are used in all active components. Thus, a small amount of additive noise introduced by the HBTs



**Figure 3.1.** The representation of a noisy two-port network

used in sensitive front-end blocks may result in a tremendous impact on the overall system performance. To facilitate the presentation of the HBT noise model, we begin by reviewing the type of noises. The two dominant noise sources of noise in HBTs are thermal noise (also known as Johnson-Nyquist noise) and shot noise.

#### A) Thermal Noise:

Thermal noise arises due to the thermal agitation of particles in a conductor. It is also called as Johnson-Nyquist [44, 45] noise. The spectrum of thermal noise is approximately white up to 1 THz [46]. The voltage, power, and current spectral densities of noisy of a resistor (see Figure 3.1) can be expressed as,

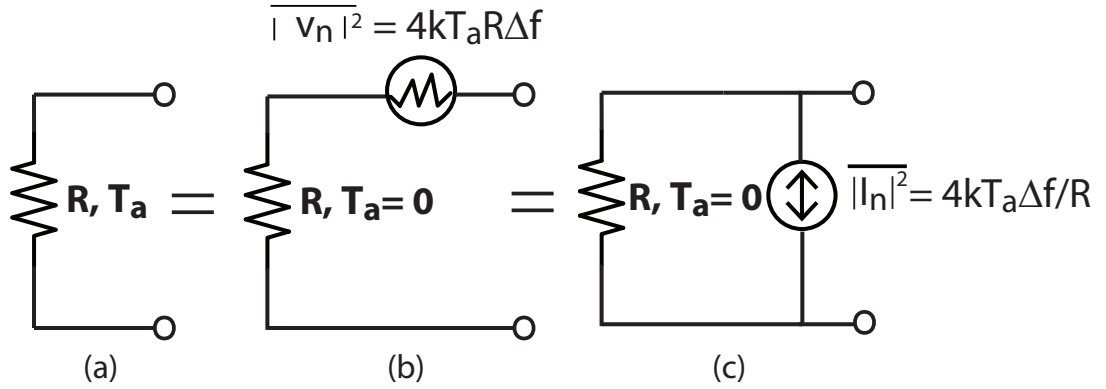
$$\overline{V_n^2} = 4k_B T R \Delta f, \quad (3.1)$$

$$P_n = k_B T \Delta f, \quad (3.2)$$

and,

$$\overline{I_n^2} = \frac{4k_B T \Delta f}{R}. \quad (3.3)$$

where  $k_B$  is Boltzmann's constant,  $T$  is the resistor's absolute temperature,  $R$  is the resistance value and  $\Delta f$  is the bandwidth. It should be emphasized that  $P_n$  is independent of the resistance value as it is shown in the equation above. The circuit

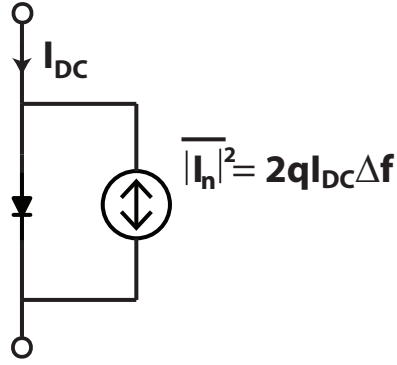


**Figure 3.2.** The equivalent circuit representation of (a) A resistor at a non-zero temperature  $T_a$  (b) Noiseless resistor with a series noise voltage source (Thevenin representation) and (c) Noiseless resistor with a parallel noise current source (Norton representation). All these three shown circuits are equivalent.

representation of thermal noise appears in Fig. 3.2. The thermal noise sources in HBTs are the access resistances associated to the base, collector, and emitter resistances.

### B) Shot Noise:

The shot noise concept was first introduced by Walter Schottky in 1918 while he studied the fluctuation of current in vacuum tubes [47]. In a typical HBT, shot noise is formed due to the quantized nature of charge. The physical source of the shot noise is when electrons and holes diffuse and cross the base-emitter junction, they randomly traverse which creates shot noise. Correlation of the base and collector shot noise sources was first reported by *Van Der Ziel* [48]. As described in Section 1.3, the electrons injected from the emitter into the base contribute to both the base and collector current resulting in correlation between the base and collector shot noise sources. The correlation of this component of the currents is a frequency dependent quantity related to a transit delay from the base to collector. This delay is only a portion of the total transit delay from the emitter to the collector and is not critical at low frequency since the product of  $\omega\tau_n$  is not sizable. However, this product becomes



**Figure 3.3.** The equivalent circuit representation of the shot noise while the diode is forward biased.

severe at high frequencies and must be taken into account for a precise design or application. The formula used in the calculation of shot noise is shown below.

$$\overline{|I_n^2|} = 2qI_{DC}\Delta f, \quad (3.4)$$

where  $q$  is the elementary charge,  $I_{DC}$  is dc current flowing through the terminal and  $\Delta f$  is the bandwidth. The circuit representation of the shot noise is demonstrated in Fig. 3.3. The equation shows the frequency dependence of the correlation between the base and the collector shot noises.

$$\overline{i_{n,b} \cdot i_{n,c}^*} = 2qI_C\Delta f(e^{j\omega\tau_n} - 1). \quad (3.5)$$

where  $i_{n,b}$  and  $i_{n,c}^*$  are base and collector shot noises, respectively,  $I_C$  is collector DC current,  $\tau$  is the noise transit time, and  $f$  is the frequency. To explain the correlation, when an HBT is forward active bias regime, majority holes from the base and majority electrons from the emitter traverse the base-emitter potential barrier. Furthermore, the electrons injected from the emitter into the base that cross the potential barrier, and then reach the collector meaning that the base and the collector currents shot

noise are not created separately. As a result of noisy injection, current crossing the base-collector junction has a noise component as well. The time needed for electrons to reach the collector terminal is called transit time.

### 3.3 Noise Figure Measurements

Noise figure is the one of the most critical parameters in a typical transceiver as well as almost all RF systems. Traditionally, the main figure-of-merit that describes the noise behaviour of a transistor is the noise factor ( $F$ ), can be defined as

$$F = \frac{S_i/N_i}{S_o/N_o} \quad \text{or} \quad F = 1 + \frac{T_e}{T_0}, \quad (3.6)$$

where  $S_i$  and  $S_o$  are the available signal powers at the input and output of the DUT respectively, and  $N_i$  and  $N_o$  are the available noise powers at the input and output of the DUT, respectively,  $T_e$  is the equivalent noise temperature which is used to specify the noise of the device, and  $T_0=290$  K is the standard reference temperature. The relation of  $T_e$  on noise factor is given in the equation shown above. Noise figure is the most common way of expressing the noise performance of a transistor as well as a two-port network and is formulated as,

$$NF = 10 \log_{10} F \text{ dB} \quad (3.7)$$

Accurate noise measurement methods are required to characterize system performance. Two common ways to measure noise figure are the  $Y$ -factor method and cold-source method.

### 3.3.1 Y-Factor Method

The  $Y$ -factor method is the most common technique for the measurement of noise figure. It requires a noise source which is connected to the input of the DUT and a noise receiver. This noise source is used in either the *on* state (also called the *hot* state) or the *off* state (also known as the *cold* state). A diode which is biased near the avalanche breakdown voltage is typically used to generate the hot state. The diode is in the cold state while it is reverse biased. In  $Y$ -factor measurement, it is assumed that the output impedance of the noise source is a constant  $Z_0$  in both states; if the output impedance of the noise source differs between the hot and cold states, this will translate to an error in the measurement. The excess noise ratio of a noise source is defined as [49],

$$ENR = \frac{T_h - T_c}{T_0}, \quad (3.8)$$

where,  $T_h$  and  $T_c$  are the equivalent noise temperatures in the hot and cold states, respectively. Selecting an appropriate  $ENR$  for a given measurement is critical since, any uncertainties of the  $ENR$  will directly impact the noise measurement accuracy. For instance, for a  $DUT$  with high  $NF$ , higher  $ENR$  should be used, whereas a lower  $ENR$  should be employed for a  $DUT$  with a low  $NF$ .

The  $Y$ -factor can be defined as,

$$Y = \frac{P_h}{P_c} = \frac{T_h + T_e}{T_c + T_e}. \quad (3.9)$$

Hence the effective noise temperature can be written as,

$$T_e = \frac{T_h - YT_c}{Y - 1}. \quad (3.10)$$

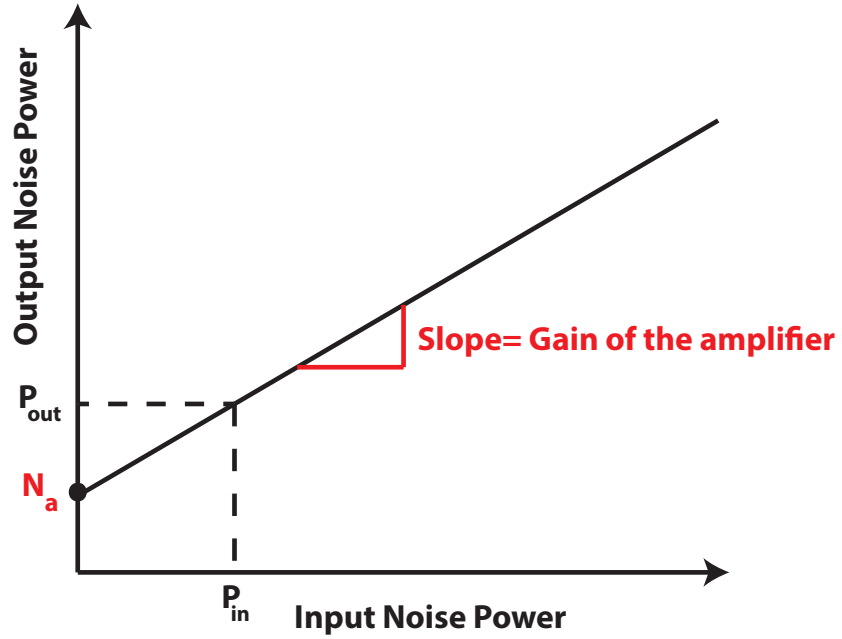


The main limitation of the  $Y$ -factor method is that it assumes the same match for both hot and cold states. Therefore, any imperfection may result in additional error to the measurement [50]. Moreover, the  $ENR$  should also be chosen carefully since any uncertainties of the  $ENR$  directly affects the accuracy of the measurement. Finally, if the  $DUT$  has low gain, the calibration may not work properly [51].

### 3.3.2 Cold Source Measurement

In this method, there is a tuner to generate different source impedances to the DUT. Measuring the noise figure at different impedances enable the determination of the standard noise parameters. Moreover, as reported by Agilent [52], the total noise is measured at first and then from the amplified measured noise, the gain of the amplifier, (which is denoted as  $N_a$  in the Figure 3.4) is calculated and subtracted to achieve the noise contribution of the DUT as graphically shown in Fig.3.4. It should be emphasized that knowing the gain of the amplifier plays a major role in performing an accurate noise measurement. For this reason, VNA has a significant impact on the precision of the cold source noise measurement technique. Another advantage of using the cold source measurement method is the fact that the calibration plane can be set, which is useful for non-50 ohm devices.

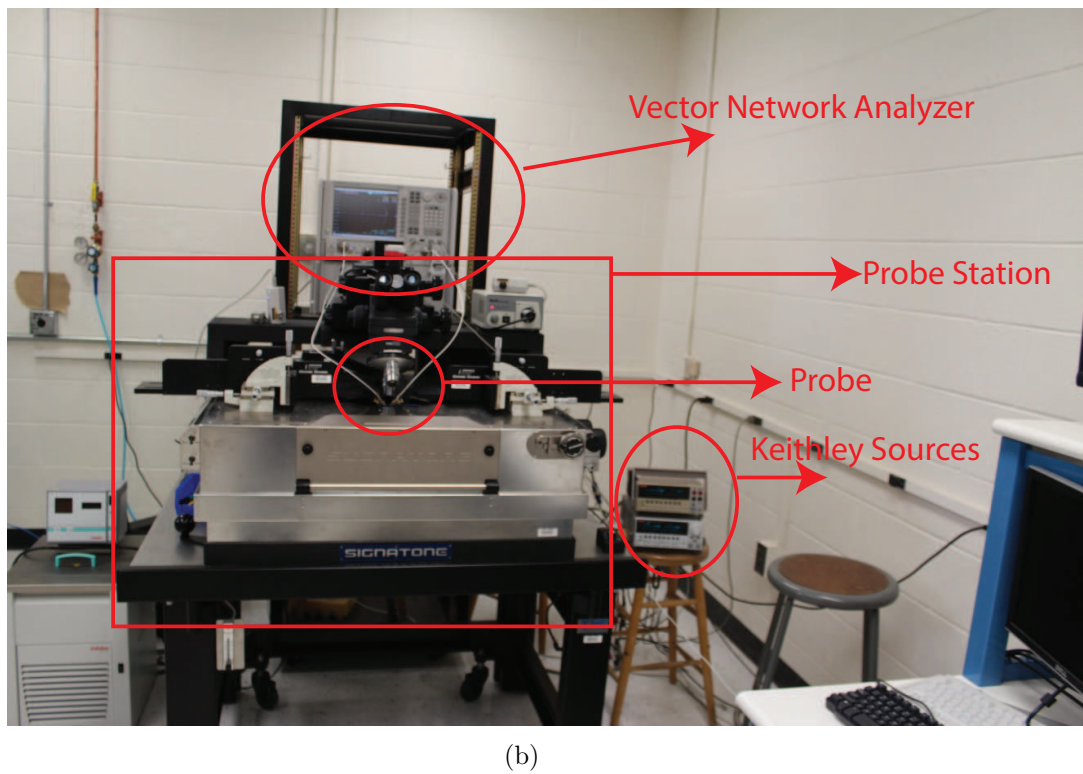
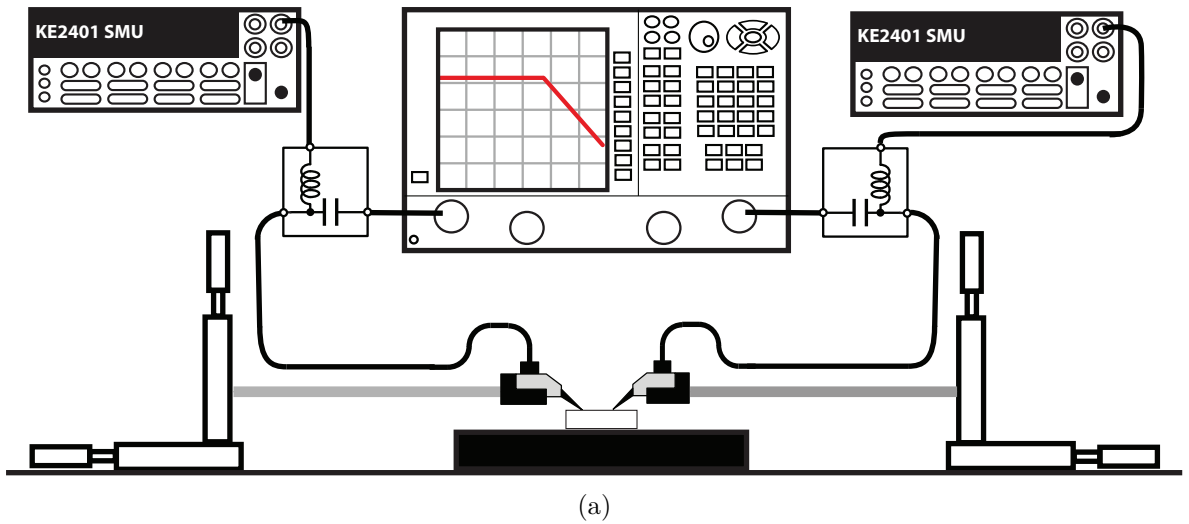
The cold source measurement method is based on using the vector corrected  $s$ -parameters to compensate reflections at interfaces in the measurement setup. In addition, the VNA measures  $s$ -parameters to vector-correct the mismatches. Hence, more accurate measurement can be performed by using the cold source method. As a result, the effect mismatch error is quite small in comparison to the  $Y$ -factor method. In contrast to the  $Y$ -factor method, there is a single cold (typically at room temperature) termination at the input of the DUT and it remains in the cold state. In this work we have used cold source measurement method to perform the noise measurements.



**Figure 3.4.** The cold source measurement method in graphical representation.

### 3.3.3 Measurement Setup

Noise figure measurements of InP HBTs were made from 1–50 GHz using the vector corrected cold source method measured by an Agilent N5247A VNA, which is capable of making high precision noise measurement to 50 GHz. Scattering parameter measurements were also made from 1–67 GHz using the same VNA. The block diagram and the photograph of the measurement setup are shown in Figure 3.5. Bias was provided through the internal bias tees of the VNA using Keithley sources meters. The transistors were contacted using Cascade Microtech *i67* wafer probes. All measurements were computer automated using the Matlab Instrument Control Toolbox. Prior to device measurements, a noise calibration was performed by connecting a noise source that provides a calibrated input noise power and the E-Cal to generate different source admittances in order to determine the four noise parameters of the receiver system. As a final step, an SOLT calibration was performed to move the reference plane from the port of the VNA to the probe tips.



**Figure 3.5.** Measurement setup. (a) Block diagram representation and (b) Picture of the setup.

### 3.3.4 Measurements

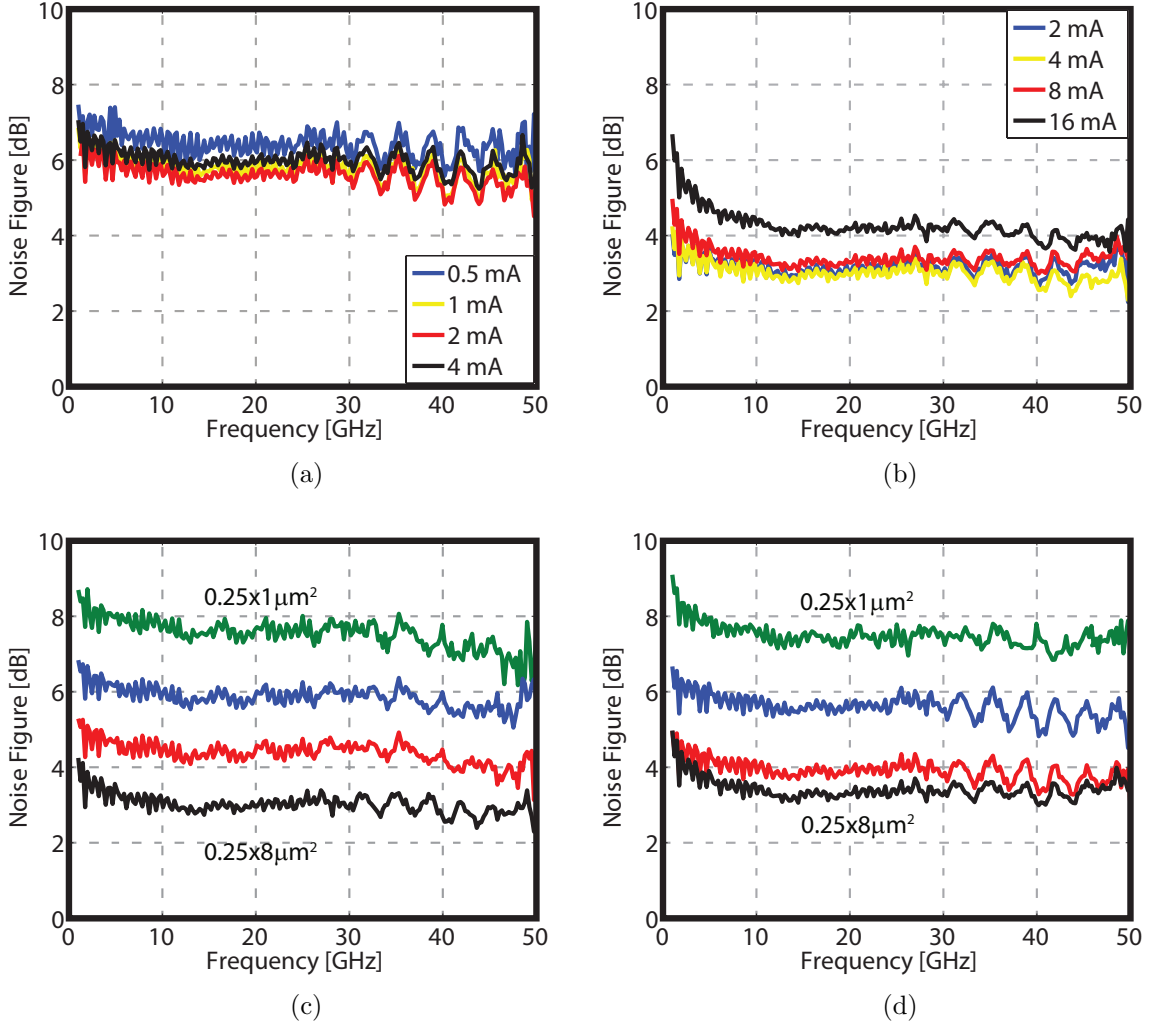
InP HBTs of different emitter areas were measured on-wafer from several different reticules and at different collector current densities. From the physical behaviour of the transistors, the noise figure is expected to be smooth with respect to frequency.

However, practically speaking this is not true as there is always measurement uncertainty (for instance due to measurement noise or  $ENR$  error in the cal step). Besides mismatch effect, we have observed that there are also multiple parameters influencing the noise performance of the devices such as the  $\beta_{DC}$  of the device, gain of the transistor, the transistor size etc.

Sample plots, showing the effect of collector current as well as  $J_C$  and the sizing of the transistor on the overall noise performance, are displayed in Figure 3.6. It is seen that the NF of the transistors is quite high at low frequencies. One probable explanation is, measurement uncertainty due to the fact that  $\Gamma_{opt}$  is far from 50 ohm. Figure 3.6 (a) and 3.6 (b) show the  $J_C$  dependency of the transistors on noise figure. We have observed that even though intrinsic base-resistance decreases moderately with respect to increasing collector current, the shot noise contribution of the collector and base currents increases which means noise figure increase as well. However, while  $J_C$  is lower than the optimum current density, the gain of the transistor becomes another parameter that has a vital impact on the noise performance. We have observed that regardless of the device size, the optimum noise figure performance was achieved at  $J_C = 4\text{mA}/\mu\text{m}^2$ . (see Figure 3.6 (a) and 3.6 b)).

Figure 3.6 (c) and 3.6 (d) display the frequency dependence of the noise performance at a fixed collector current density. Typically, the noise figure of a transistor increases with frequency. However, the correlation of the shot noise becomes non-zero at high frequency which makes the noise performance of the transistors slightly better at high frequencies. From the graph it can be seen that for the same collector current density, the smaller device has a greater noise figure ((see Figure 3.6 (a) and 3.6 b))). With the assumption of having the same  $\beta_{DC}$ , despite the fact that,  $T_{min}$  is equal for all devices,  $\Gamma_{opt}$  is not same for all devices. Also, large device has higher gain compared with smaller devices, which is critical as well for achieving better noise

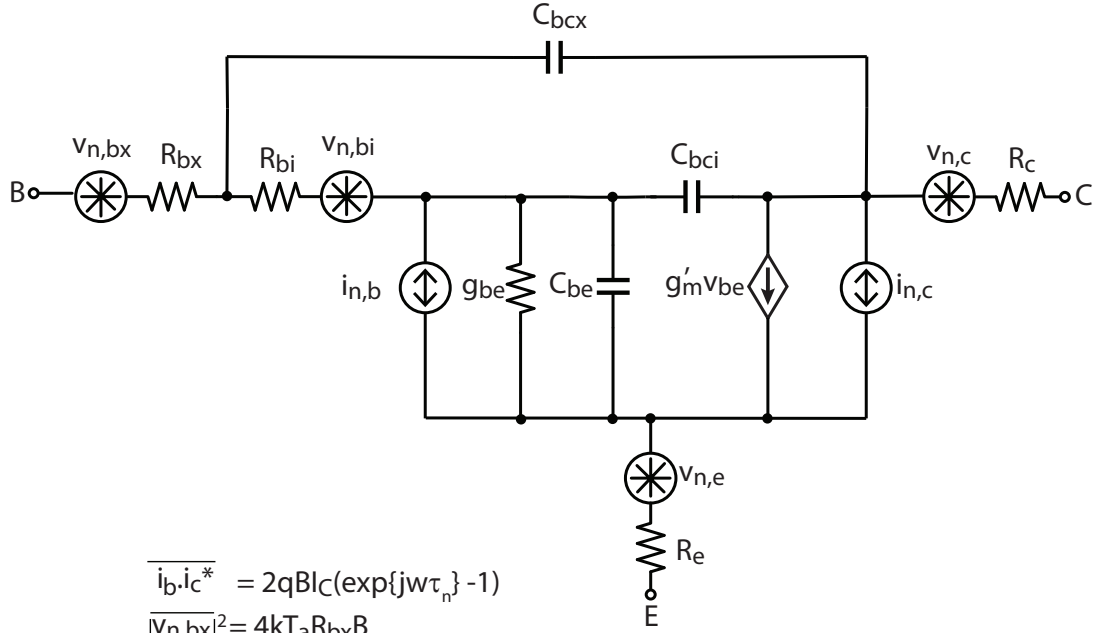
performance.



**Figure 3.6.** Noise Figure plots. (a) NF at different  $J_C$  for  $0.25 \times 2 \mu\text{m}^2$ , (b) NF at different  $J_C$  for  $0.25 \times 8 \mu\text{m}^2$ , (c) NF of four different transistors at fixed  $J_C = 2 \text{mA}/\mu\text{m}^2$  and (d) NF of four different transistors at fixed  $J_C = 4 \text{mA}/\mu\text{m}^2$

### 3.4 Noise Modeling

A physics-based analytical HBT noise model is desirable for understanding the noise performance. In Chapter 2, the small-signal equivalent circuit parameters were extracted. To complete the small-signal noise model, thermal noise and shot noise



$$\begin{aligned} \overline{i_b i_c^*} &= 2qB I_C (\exp\{j\omega\tau_n\} - 1) \\ \overline{|v_{n,bx}|^2} &= 4kT_a R_{bx} B \\ \overline{|v_{n,bi}|^2} &= 4kT_a R_{bi} B & \overline{|v_{n,ci}|^2} &= 4kT_a R_c B & \overline{|i_{n,b}|^2} &= 2qB (I_B + |1 - \exp\{-j\omega\tau_n\}| I_C) \\ \overline{|v_{n,e}|^2} &= 4kT_a R_e B & g'_m &= g_m \exp\{-j\omega\tau\} & \overline{|i_{n,c}|^2} &= 2qI_C B \end{aligned}$$

**Figure 3.7.** The small-signal noise model

sources are added. The circuit schematic is presented in Figure 3.7. Since the  $g_{be}$  is not a physical resistance, it does not have any thermal noise contribution. With the model already extracted, the investigation of the agreement between measurements and models is straightforward. It has been observed that the transit time has a significant impact on the noise figure, especially at high frequencies. The shot noise delay term is taken as 65% of the full delay,  $\tau$ , following results described by Rudolph [53, 54]. For comparison to measurement, the effect of parasitics due to the feed-lines and padframe have been re-embedded onto the model. Sample plots for four different sized of transistors appear in Figure 3.8. There is an excellent agreement between model and measurement for all four transistors in the frequency range of 1-50 GHz.

Apart from the comparison of the model and measurements, noise parameters were explored as well. The standard noise parameters  $R_n$ ,  $T_{min}$ ,  $R_{opt}$  and  $X_{opt}$  were computed in the frequency range from DC-100 GHz. Prior discussing the results, the

equations showing the  $\beta_{DC}$  and frequency dependencies of  $R_{opt}$  and  $T_{min}$  should be recalled as

$$R_{opt} \approx \frac{\beta_{DC}}{g_m(1 + \beta_{DC}(f/f_t)^2)} \sqrt{\frac{1}{\beta_{DC}} \left( 1 + \frac{2g_m(R_b + R_e)}{n_c} \right) + \frac{2g_m(R_b + R_e)}{n_c} \left( \frac{f}{f_t} \right)^2}, \quad (3.11)$$

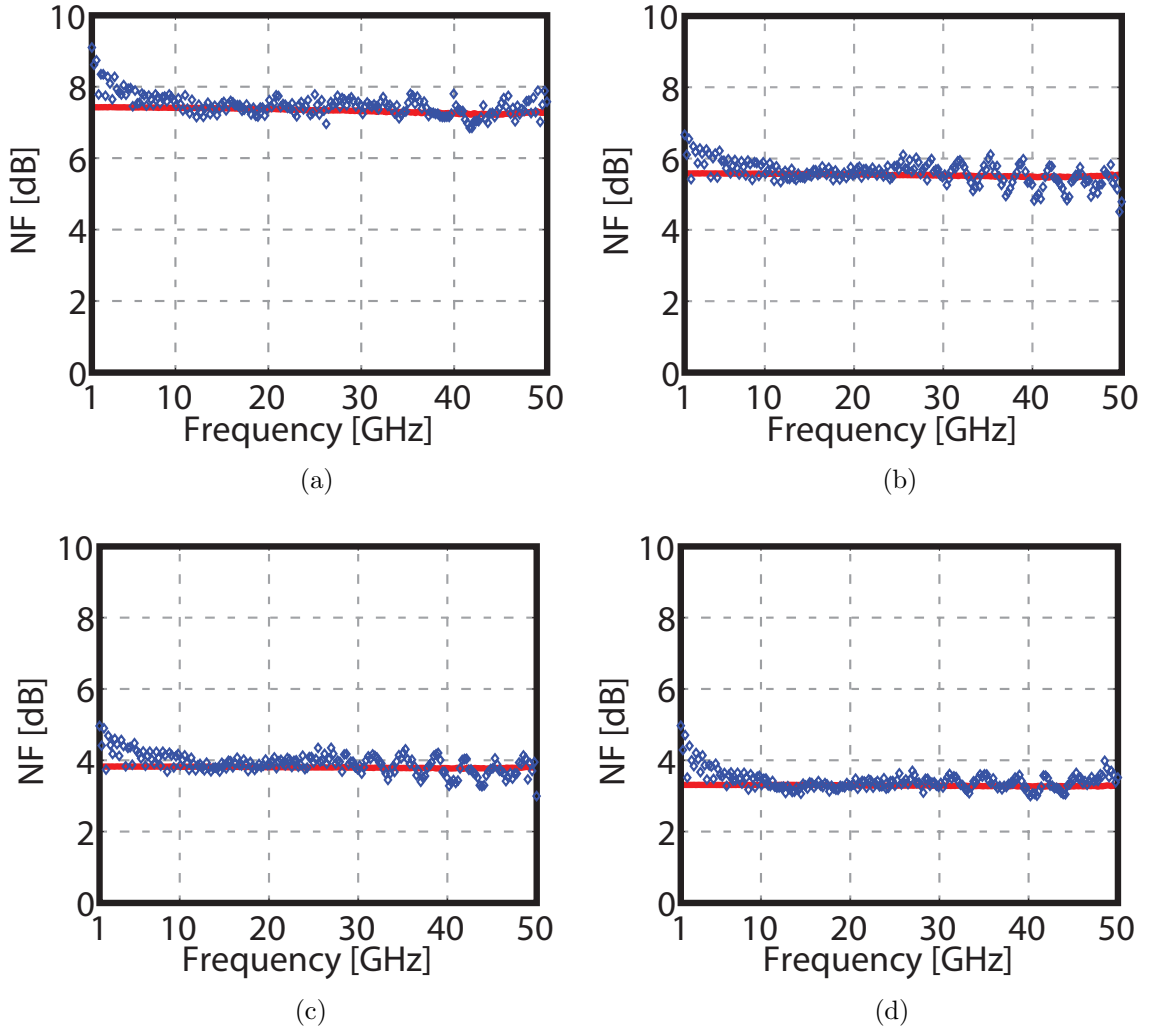
$$T_{min} \approx T_a n_c \sqrt{\frac{1}{\beta_{DC}} \left( 1 + \frac{2g_m(R_b + R_e)}{n_c} \right) + \frac{2g_m(R_b + R_e)}{n_c} \left( \frac{f}{f_t} \right)^2}. \quad (3.12)$$

Figures 3.9 and 3.10 summarize the parameter values of four different size devices. As expected,  $R_n$  is inversely dependent on device area (see Figure 3.9 (a)). Moreover,  $R_n$  decreases at high frequencies. This effect is more rapid for the smaller device due to the time delay and extrinsic base-collector capacitance [55]. Moreover,  $R_n$  rises below a current density of  $4 \mu\text{m}^2$ , but is constant above this level (see Fig. 3.9(e) and 3.9 (f)).

As expected,  $R_{opt}$  and  $X_{opt}$  also are inversely proportional to the device size (see Figure 3.10 (c) and 3.10 (d)). Furthermore, the  $R_{opt}$  and  $X_{opt}$  of the larger device are approximately equal to the half values of the smaller device.  $R_{opt}$  decreases as the collector current density goes higher because of the increasing value of  $g_m$  and the decreasing value of  $R_b$  (see Equation 3.11) as well as a result of decreasing of the equivalent noise resistance ( $R_n$ ) [56]. Similarly,  $X_{opt}$  decreases with increasing collector current density, as shown in Figures 3.10 (e) and 3.10 (f).

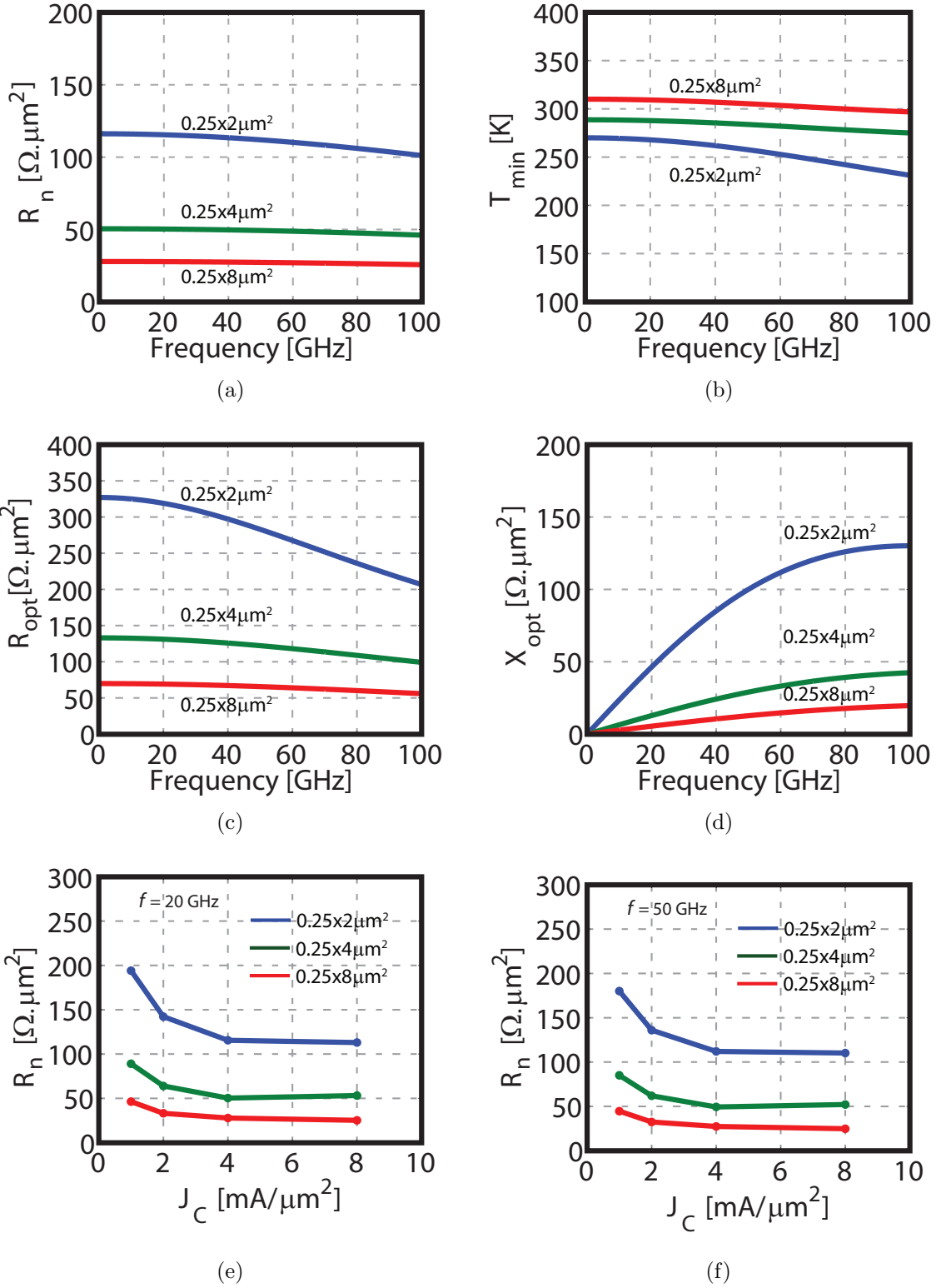
$T_{min}$  is expected to increase monotonically with respect to frequency [56,57]. However, since the shot noise correlation becomes non-zero at high frequencies, a decline is observed at high end as seen in Fig 3.9(b). In addition,  $T_{min}$  is size independent,

but depends upon collector current density. The observed differences in the minimum noise temperature are explained by differences in  $\beta_{DC}$ . Figure 3.10 (a) and 3.10 (b) illustrate the dependence of  $T_{min}$  on collector current density.  $T_{min}$  increases with current density due to the high shot noise contribution. The dependency of  $T_{min}$  on  $\beta_{DC}$  and frequency is shown in the Equation 4.5 [10].

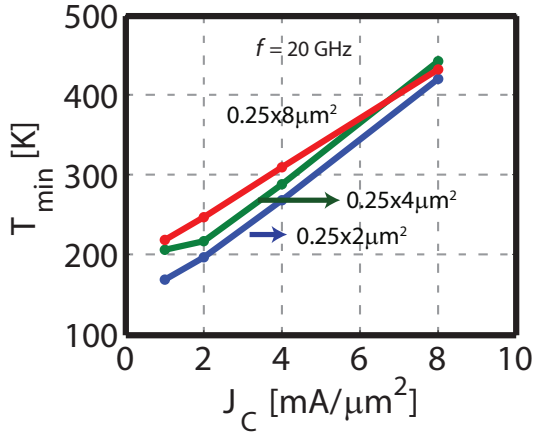


**Figure 3.8.** Noise figure comparison of small-signal noise models and measurements at  $J_C=4 \text{ mA}/\mu\text{m}^2$ . (a)  $0.25 \times 1 \mu\text{m}^2$ , (b)  $0.25 \times 2 \mu\text{m}^2$ , (c)  $0.25 \times 4 \mu\text{m}^2$  (d)  $0.25 \times 8 \mu\text{m}^2$ . Solid lines correspond to models whereas marked curves represent the measurements.

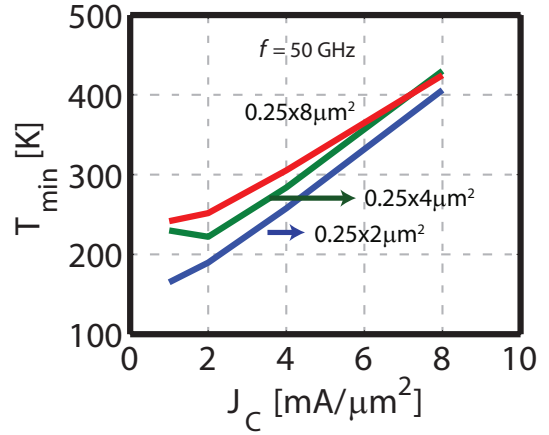




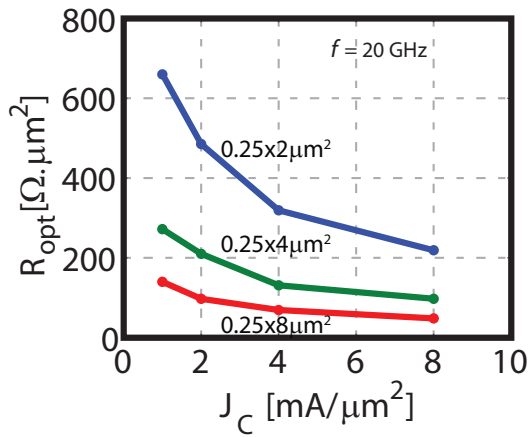
**Figure 3.9.** Noise parameters. (a)  $R_n$  versus frequency at  $J_C=4 \text{ mA}/\mu\text{m}^2$ , (b)  $T_{\min}$  vs frequency at  $J_C=4 \text{ mA}/\mu\text{m}^2$ , (c)  $R_{\text{opt}}$  vs frequency at  $J_C=4 \text{ mA}/\mu\text{m}^2$ , (d)  $X_{\text{opt}}$  vs frequency at  $J_C=4 \text{ mA}/\mu\text{m}^2$ , (e)  $R_n$  vs  $J_C$  at  $f=20 \text{ GHz}$ , (f)  $R_n$  vs  $J_C$  at  $f=50 \text{ GHz}$ . Blue lines correspond to  $0.25 \times 2 \mu\text{m}^2$ , green lines represent  $0.25 \times 4 \mu\text{m}^2$  and red lines indicate  $0.25 \times 8 \mu\text{m}^2$  device parameters for all plots.



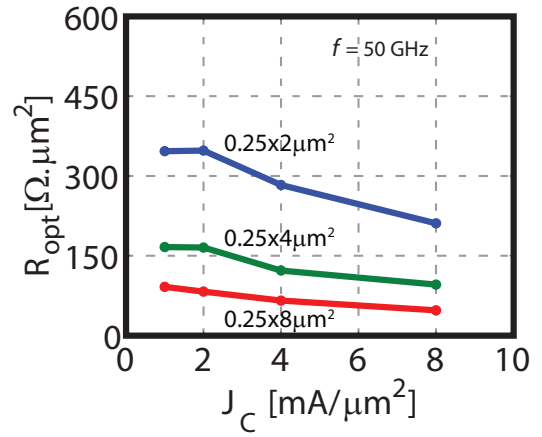
(a)



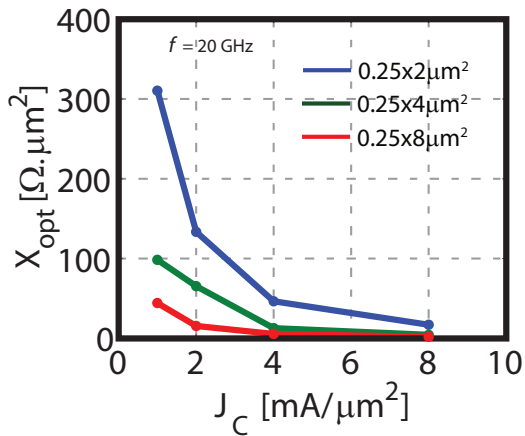
(b)



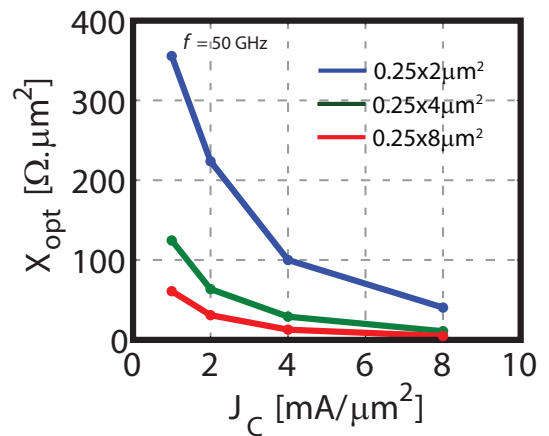
(c)



(d)



(e)



(f)

**Figure 3.10.** The standard noise parameters at a fixed frequency. (a)  $T_{min}$  vs  $J_C$  at  $f=20$  GHz, (b)  $T_{min}$  vs  $J_C$  at  $f=50$  GHz, (c)  $R_{opt}$  vs  $J_C$  at  $f=20$  GHz (d)  $R_{opt}$  vs  $J_C$  at  $f=50$  GHz, (e)  $X_{opt}$  vs  $J_C$  at  $f=20$  GHz, (f)  $X_{opt}$  vs  $J_C$  at  $f=50$  GHz.

### 3.5 Summary

The noise concept of the transistors has been covered in this chapter. We began with the fundamental background of noise and the importance of it in system's performance respect. The noise types were physically explained and the basic formulas in the calculation of noise factor as well as noise figure were given. The noise characterization methods were described and the measurement setup used to obtain data was demonstrated. Sample noise figure plots with respect to collector current density and frequency were shown. Finally, the noise modelling of the transistor was explored with giving the extraction of the noise parameters. The comparison of the models and measurements were also investigated. The circuit application that is designing a low noise amplifier will be expressed in the next chapter

## CHAPTER 4

### APPLICATIONS

#### 4.1 Introduction

Low noise amplifiers (LNAs) are one of the fundamental building blocks required for any communication system. LNAs are used to amplify signals while adding little noise. (see Equation 4.1). To understand the importance of the LNA and its impact on SNR, the Friis equation should be analysed [58].

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \quad (4.1)$$

where,  $F_i$  is the noise factor of the  $i^{th}$  component in the receiver chain, and  $G_i$  is the gain of the  $i^{th}$  stage or device.

From the formula, it is clear that the first amplification stage will dominate the overall system noise figure, provided that its gain is sufficiently high. The design of LNAs is challenging and the aim is to maximize the agreement between simulated and measured parameters. Available compact models do not always give accurate results at very high frequencies due to model inaccuracies. If available for a desired bias point, small-signal noise models can be used instead. The transistor model that is used in the design of LNA, is based on extracted small-signal noise model presented in Chapters 2 and 3.

In this part of the thesis, the design of a broadband low noise Ku band (12–18 GHz) amplifier will be discussed. The chapter starts with the basic concepts of LNAs. Then, the circuit topology used in this design will be presented. After that,

the comparison of the VBIC compact models and the extracted small-signal models in terms of the scattering parameters and noise figure will be explored.

## 4.2 Low Noise Amplifier Design

### 4.2.1 Basic Concepts in LNA Design

Design of an LNA begins with the evaluation of the nominal noise and gain impedance matching networks required to optimize the performance. For this purpose, the design procedure should begin with plotting the optimum generation impedance for noise match ( $\Gamma_{opt}$ , see Equation 4.2) on the Smith chart. The generator impedance ( $\Gamma_g$ ) must be near  $\Gamma_{opt}$  in order to achieve minimum noise. The expression indicating the dependency of noise factor on the mismatch between  $\Gamma_{opt}$  and  $\Gamma_s$  appears in the equation shown below.

$$\Gamma_{opt} = \frac{Z_{opt} - 1}{Z_{opt} + 1} \quad (4.2)$$

where,  $Z_{opt} = R_{opt} + jX_{opt}$

$$F = F_{min} + \frac{4R_n}{Z_0} \left\{ \frac{|\Gamma_{opt} - \Gamma_s|^2}{|1 + \Gamma_{opt}|^2 (1 - |\Gamma_s|^2)} \right\}. \quad (4.3)$$

For a given conjugately matched impedance, lower noise figure can be achieved. Furthermore, the expression for available gain is

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2 |1 - \Gamma_{out}|^2}, \quad (4.4)$$

where,  $P_{avn}$  and  $P_{avs}$  are the power available from the source and the power available from the network respectively. These two equations are the basic relationships between gain and noise figure as a function of source impedance. While linearity

is another important parameter in LNA design, it is not discussed as the linearity properties of InP HBTs is beyond the scope of this thesis.

#### 4.2.2 Microwave LNA Design

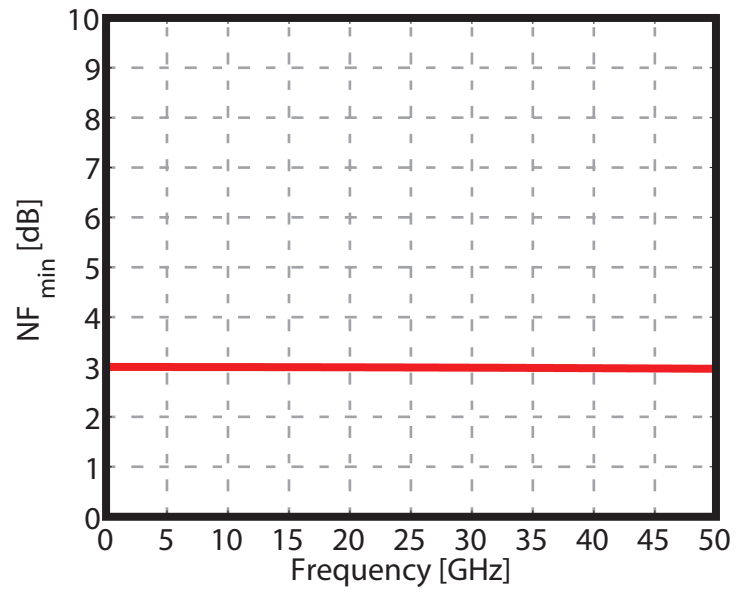
The first step of the design procedure is to select a collector current density at which the device simultaneously has sufficient gain and noise performance over the frequency range of interest. Therefore, operating point and device size is fixed as an initial step.

A device with  $0.25 \times 4 \mu\text{m}^2$  emitter area used in LNA design. Next, an equivalent circuit model to match to  $50 \Omega$  is needed. When designing for noise match, an input network is designed to transform the generator impedance to  $\gamma_{\text{opt}}$  over a desired frequency range. After designing the input matching circuit, the output matching network is designed to achieve the available gain. Thus, synthesis of the output matching network involves transforming the load impedance to  $S_{22}^*$  of the noise matched device.

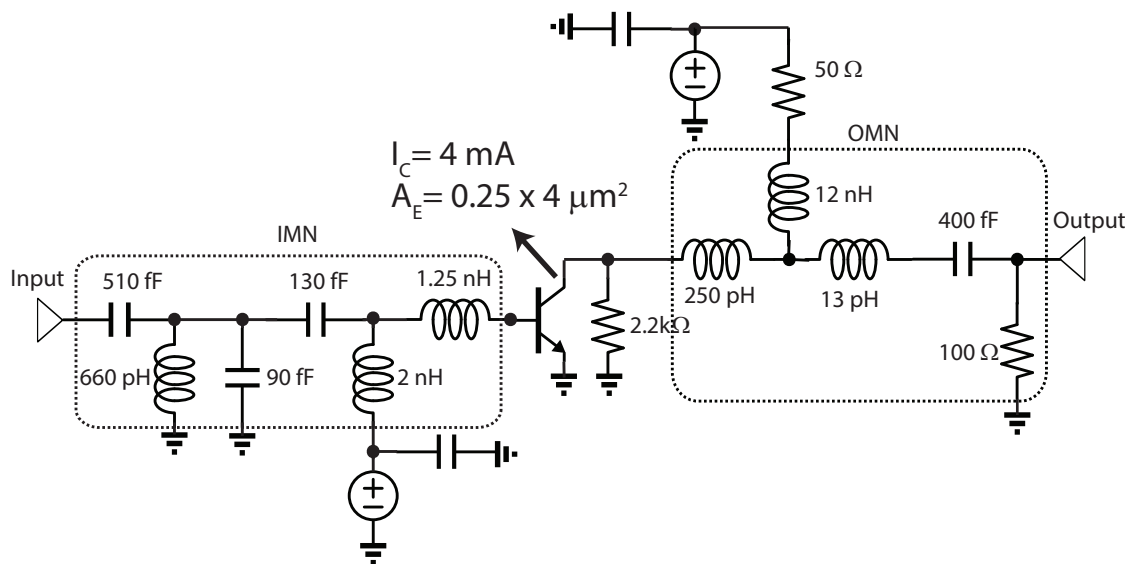
In the design of LNA, a transistor with  $0.25 \times 4 \mu\text{m}^2$  emitter area has been used. Since the emitter area is fixed, the single degree of freedom that can be optimized is  $J_C$ ; in this case and it is set to  $4\text{mA}/\mu\text{m}^2$ . The model parameters of the transistor used in this model are displayed in Table 4.1 and the corresponding minimum noise figure with respect to frequency can be seen in Figure 4.1.

**Table 4.1.** Model Parameters of  $0.25 \times 4 \mu\text{m}^2$  at  $J_C = 4\text{mA}/\mu\text{m}^2$

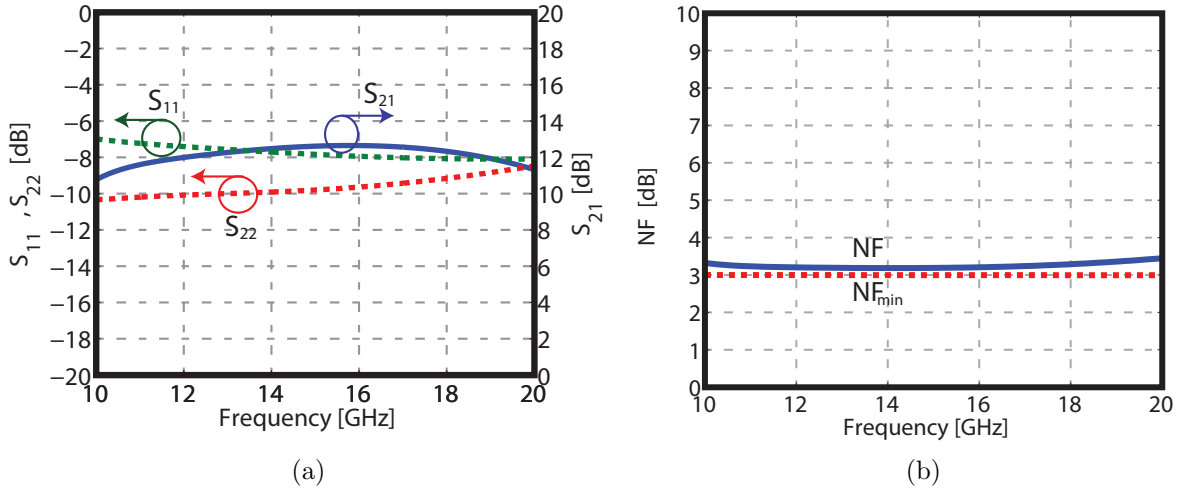
$R_{bx}$	$R_{bi}$	$R_e$	$R_c$	$C_{bcx}$	$C_{bci}$	$C_{be}$	$g_{be}$	$g_m$	$\tau$	$I_B$	$I_C$	$\beta_{DC}$
$\Omega$				fF			mS	ps	mA			
6	20.2	5.5	8.4	3.4	5.2	23	1.94	75	0.4	0.14	4	29



**Figure 4.1.** Noise Figure of the device has  $0.25 \times 4 \mu\text{m}^2$  emitter area at  $J_C=4 \mu\text{m}^2$ .



**Figure 4.2.** Schematic of the low noise amplifier.



**Figure 4.3.** High frequency performance of the LNA. (a) Simulated S-parameters, and (b) Noise figure and minimum noise figure

### 4.3 Results and Comparisons

The LNA topology is shown in Figure 4.2. Simulated s-parameters and noise figure are shown in Fig 4.3. The LNA has more than 12 dB gain and approximately 8 dB and 10 dB input and output losses, respectively, across the entire frequency band. The simulated noise figure is approximately 3.3 dB whereas the minimum achievable noise figure with the modelled transistor is around 3 dB (see Fig 4.3 (b)).

The simulated performance as predicted using the models developed in this thesis can also be compared with that predicted using existing the VBIC model (note, the VBIC model does not account for shot noise correlation). The same size transistor with the same collector current density is used for all comparisons. Figure 4.4 shows the comparison of s-parameters and noise figure of small-signal model based LNA with the VBIC model based LNA.

The gain and output reflection coefficient simulations demonstrate excellent agreement over the frequency range of interest (see Fig. 4.4 (a) and (b)). On the other hand, there is a significant deviation between the input return loss and NF curves

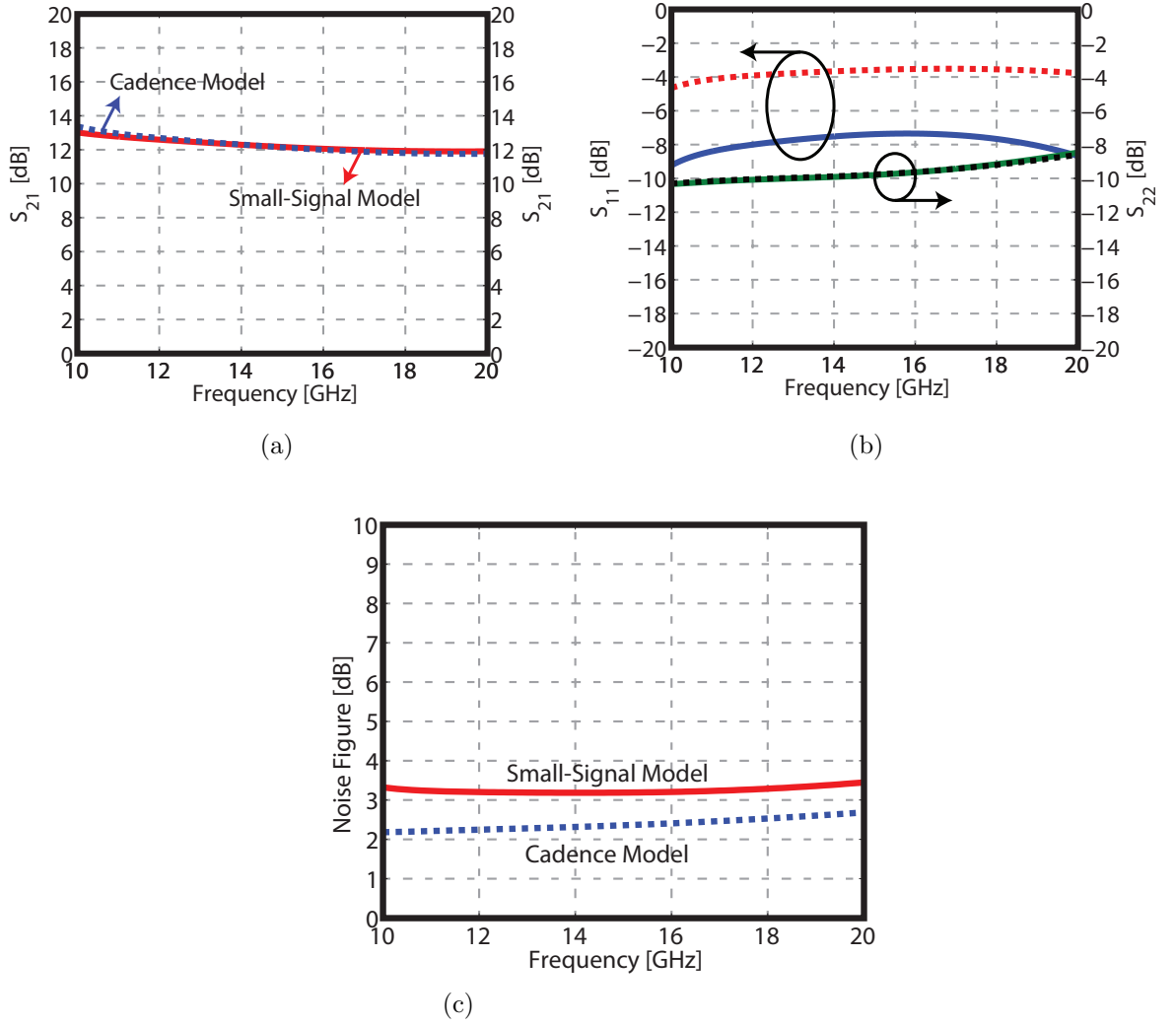


predicted using the small-signal and VBIC models. Although the small signal model based LNA has lower  $S_{11}$ , NF of the cadence model based LNA is better by 1 dB (see Fig. 4.4 (c)). Fortunately, this disagreement is easily explained by differences in the value of the DC current gain predicted by each of the models. We found that, at  $4 \mu\text{m}^2$ , the  $\beta_{DC}$  of the transistor we have measured is 29, whereas it is 80 for the VBIC model. Hence, in order to make a fair comparison between the models, the  $\beta_{DC}$  value of the small-signal model should be adjusted accordingly. To adjust this value, the base current of modelled transistor is reduced.

To incorporate the impact of increased  $\beta_{DC}$  in the small-signal model, the base shot noise source was reduced and the the base-emitter resistance was increased. The resulting s-parameter and noise figure results are shown in Fig. 4.5. The reduction in the base shot noise results in an improvement to NF (see Fig. 4.5 (a)). To explain this improvement, relationship of  $NF_{min}$  to  $\beta_{DC}$  should needed to be reviewed. The equation shown below expresses the  $\beta_{DC}$  dependency of noise figure [59]

$$T_{min} \approx T_a n_c \sqrt{\frac{1}{\beta_{DC}} \left( 1 + \frac{2g_m(R_b + R_e)}{n_c} \right) + \frac{2g_m(R_b + R_e)}{n_c} \left( \frac{f}{f_t} \right)^2}. \quad (4.5)$$

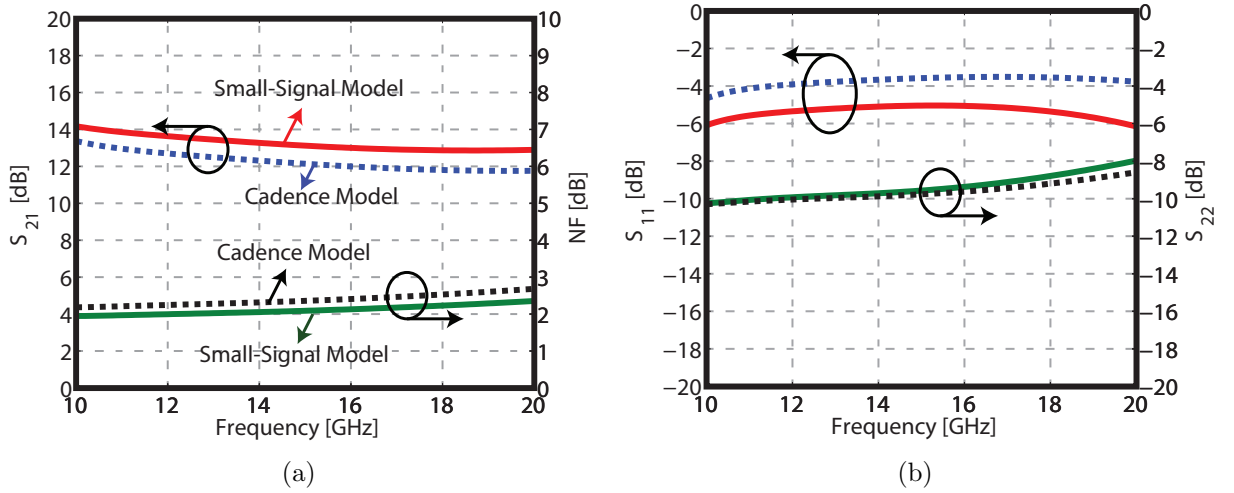
From the formula, inverse proportionality of  $T_{min}$  as well as noise figure on  $\beta_{DC}$  is seen. Therefore, an increase in  $\beta_{DC}$  results in a decrease in the overall NF. After making this tuning, not only have we improved the NF (see Fig. 4.5 (a)), but also we systematically shown that the simulated noise performance of the small-signal noise model is better than VBIC model. Furthermore,  $S_{11}$  has also been improved while  $S_{21}$  and  $S_{22}$  agreements are still quite good as seen in the Fig. 4.5 (a) and (b).



**Figure 4.4.** Comparison of the small-signal model based LNA and the Cadence model based LNA in terms of, (a)  $S_{21}$ , and (b)  $S_{11}$  and  $S_{22}$ , and (c) NF comparisons.

#### 4.4 Summary

In the last part of the thesis, a low noise Ku band amplifier has been designed and simulated as an example application of the presented small-signal noise models. Then, the RF figures-of-merit of the designed LNA are shown. The agreement of the small-signal model based LNA and the VBIC model based LNA was explored. As discussed in Results and Comparison section, as a result of overestimated DC current gain by the VBIC model, the measured noise figure might not agree with



**Figure 4.5.** S-parameters and NF comparison after tuning  $\beta_{DC}$  in terms of, (a)  $S_{21}$  and NF, and (b)  $S_{11}$  and  $S_{22}$ . Solid lines reflect the small-signal model parameters whereas dashed curves correspond to the Cadence model.

the simulated noise figure. Thus, it should be revised to prevent the disagreement between simulation and measurement. In addition, the shot noise correlation must be considered for high frequency applications.

## CHAPTER 5

### CONCLUSION

Throughout this thesis, we have explored the modelling of InP based HBTs in terms of small-signal and noise, which has successfully accomplished in a very broadband frequency. Furthermore, a low noise Ku band amplifier was designed to validate the extracted model. In Chapter 1, the fundamentals of BJT as well as the idea of HBT were discussed. In addition, the most commonly used compact models, Gummel-Poon Model, VBIC (Vertical Bipolar Inter-Company model), HICUM (High Current Model) and MEXTRAM (Most EXquisite TRAnsistor Model) were briefly explained. The second chapter of the thesis addressed the DC and RF performance as well as a systematic procedure of small-signal modelling of variety of transistors that have different emitter areas. In addition, the correlation between measurements and models was studied.

The third chapter of the thesis includes the noise concept and common measurement techniques as well as the noise modelling of the transistors. Noise parameter characteristics in terms of bias, frequency and device size were also inspected. In the last part of the thesis, a circuit application which was based on the model we have derived was presented. A low noise Ku band amplifier was designed for validity purpose. The comparison results were highlighted and any probable cause of disagreement was investigated. From the results we have obtained, it has been demonstrated that, the extracted simple equivalent circuit reflects accurate performance metrics in comparison to the VBIC compact model.

## APPENDIX A

### MATLAB CODES

#### A.1 Network Parameter Conversion

From s-parameters to Y-parameters;

```
function[y]=stoy(data)
[s11r,s11i]=pol2cart(data(:,3)*pi/180,10.^(data(:,2)/20));
[s21r,s21i]=pol2cart(data(:,5)*pi/180,10.^(data(:,4)/20));
[s12r,s12i]=pol2cart(data(:,7)*pi/180,10.^(data(:,6)/20));
[s22r,s22i]=pol2cart(data(:,9)*pi/180,10.^(data(:,8)/20));
s11=s11r+i*s11i;
s21=s21r+i*s21i;
s12=s12r+i*s12i;
s22=s22r+i*s22i;
delta=(1+s11).*(1+s22)-(s12.*s21);
y11=((1-s11).*(1+s22)+s12.*s21)./delta/50;
y12=-2*s12./delta/50;
y21=-2*s21./delta/50;
y22=((1+s11).*(1-s22)+s12.*s21)./delta/50;
y(:,1)=y11;
y(:,2)=y12;
y(:,3)=y21;
y(:,4)=y22;
end
```

From s-parameters to Z-parameters;

```
function [z]=stoz(data)
[s11r,s11i]=pol2cart(data(:,3)*pi/180,10.^(data(:,2)/20));
[s21r,s21i]=pol2cart(data(:,5)*pi/180,10.^(data(:,4)/20));
[s12r,s12i]=pol2cart(data(:,7)*pi/180,10.^(data(:,6)/20));
[s22r,s22i]=pol2cart(data(:,9)*pi/180,10.^(data(:,8)/20));
s11=s11r+i*s11i;
s21=s21r+i*s21i;
s12=s12r+i*s12i;
s22=s22r+i*s22i;
delta=(1-s11).*(1-s22)-(s12.*s21);
z11=((1+s11).*(1-s22)+s12.*s21)./delta*50;
z12=2*s12./delta*50;
z21=2*s21./delta*50;
z22=((1-s11).*(1+s22)+s12.*s21)./delta*50;

z(:,1)=z11;
z(:,2)=z12;
z(:,3)=z21;
z(:,4)=z22;
end
```

From Y-parameters to Z-parameters;

```
function [z] = YtoZ(data)
delta=data(:,1).*data(:,4)-data(:,2).*data(:,3);
z11=data(:,4)./delta;
z12=-data(:,2)./delta;
```

```
z21=-data(:,3)./delta;  
z22=data(:,1)./delta;
```

```
z(:,1)=z11;  
z(:,2)=z12;  
z(:,3)=z21;  
z(:,4)=z22;  
end
```

From Z-parameters to Y-parameters;

```
function [y] = ZtoY(data)  
delta=data(:,1).*data(:,4)-data(:,2).*data(:,3);  
y11=data(:,4)./delta;  
y12=-data(:,2)./delta;  
y21=-data(:,3)./delta;  
y22=data(:,1)./delta;
```

```
y(:,1)=y11;  
y(:,2)=y12;  
y(:,3)=y21;  
y(:,4)=y22;  
end
```

From Z-parameters to S-parameters;

```
for i=1:length(freq)  
    Yd=[Ydut(i,1) Ydut(i,2);Ydut(i,3) Ydut(i,4)];  
    temp=y2s(Yd);
```

```

ser1(i,2)=20*log10(abs(temp(1,1)));
ser1(i,3)=radtodeg(phase(temp(1,1)));
ser1(i,4)=20*log10(abs(temp(2,1)));
ser1(i,5)=radtodeg(phase(temp(2,1)));
ser1(i,6)=20*log10(abs(temp(1,2)));
ser1(i,7)=radtodeg(phase(temp(1,2)));
ser1(i,8)=20*log10(abs(temp(2,2)));
ser1(i,9)=radtodeg(phase(temp(2,2)));

end

fid = fopen('Sdut.s2p','w');
fprintf(fid,'%s\n','!S2P File: Measurements: S11. S21. S12. S22:');
fprintf(fid,'%s\n','# Hz S dB R 50');
fclose(fid);
dlmwrite('Sdut.s2p',ser1,'-append','delimiter',' ');

```

## A.2 De-embedding Code

In order to remove the parasitics, open/short de-embedding method was used. The following Matlab code was written for this process;

```

%read device and convert to Y
d=input('Enter Device Number','s');
r=input('Enter Reticle Number','s');
b=input('Enter Bias Number','s');
device=dlmread(sprintf('D%s_R%s_%s.s2p',d,r,b),'',[9 0 (401+8) 8]);
Ydev=stoy(device);

%read open and convert to Y
open=dlmread('open.s2p','',[9,0,409,8]);
Yop= stoy(open);

```



```

%read short and convert to Y
short=dlmread('short.s2p','',[9,0,409,8]);
Ysh=stoy(short);
% Define shunt parasitic
YA=Yop(:,1)+Yop(:,2);
YC=Yop(:,4)+Yop(:,2);
% Write YA and YC in the matrix as 'Par' Parasitic Matrix
for i=1:length(open(:,1))
    matr=[YA(i,1) 0;0 YC(i,1)];
    Ypar(i,1)=matr(1,1);
    Ypar(i,2)=matr(1,2);
    Ypar(i,3)=matr(2,1);
    Ypar(i,4)=matr(2,2);
end
% Subtract parasitics YA and YC from Yss
Y=Ysh-Ypar;
%take the inverse of Y
Z=YtoZ(Y);
%define series parasitic
ZA=Z(:,1)-Z(:,2);
ZB=Z(:,2);
ZC=Z(:,4)-Z(:,2);
%last shunt parasitics
YB=(-(1./Yop(:,2))-ZA-ZC).^-1;
% Step-1: From Two-port Y parameters to removed first
parasitics YA and YC Parameters
Ya= Ydev-Ypar;

```

```

% Step-2: convert Ya to Za
Za=YtoZ(Ya);
% Step-3: Remove Z parasitics
Zb=(Za)-[ZA+ZB ZB ZB ZB+ZC];
% Step-4: Convert Zb to Yb
Yb=ZtoY(Zb);
% Step-5: Remove last parasitic to get Ydut
Ydut=Yb-[YB -YB -YB YB];
%convert Ydut to Zdut
Zdut=YtoZ(Ydut);

```

### A.3 Matlab Code Used For Parameter Extractions

The Matlab code used for the parameter extractions are as follow.

#### A.3.1 Emitter Resistance

```

vc=device(:,2);
vb=device(:,1);
ib=device(:,3);
ic=device(:,4);
%calculate partial derivative
partialvcib=(vc(2:length(vc))-vc(1:(length(vc)-1)))./
(ib(2:length(ib))-ib(1:(length(ib)-1)));
%find average emitter current
iem=0.5*(ib(1:(length(ib)-1))+ib(2:length(ib))+
ic(1:(length(ic)-1))+ic(2:length(ic)));
%find linear range
plot(1./iem(20:100),partialvcib(20:100))

```

```
cftool(1./iem(20:100),partialvcib(20:100))
```

### A.3.2 The Rest Of The Small-Signal Parameters

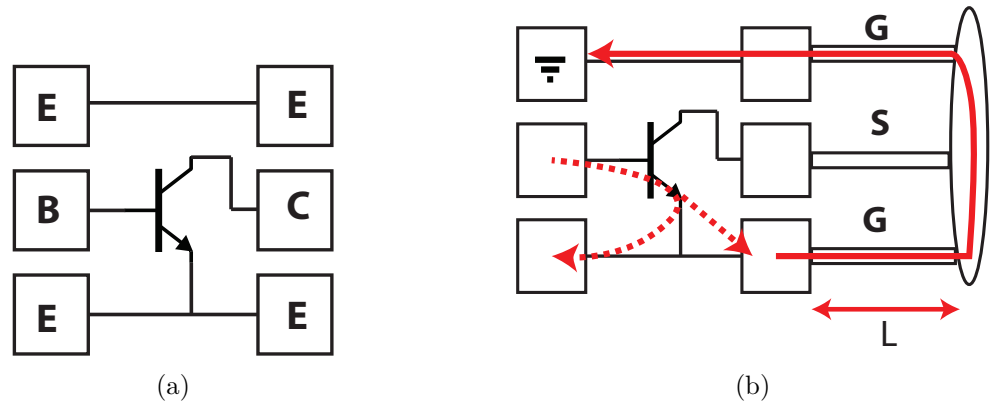
From De-embedded Y and Z-parameters,

```
Rb=real(Zdut(:,1)-Zdut(:,2));  
Rc=real(Zdut(:,4)-Zdut(:,3));  
Zint=Zdut-[Rb+Re Re Re Re+Rc];  
Yint=ZtoY(Zint);  
Cbc= -imag(Yint(:,2))/(2*pi*freq);  
Cbe=imag(Yint(:,1)+ Yint(:,2))/(2*pi*freq);  
gm=abs(Yint(:,3)- Yint(:,2));  
gbe=abs(Yint(:,1)+ Yint(:,2));  
t=-(phase((Yint(:,3)-Yint(:,2)))/(2*pi*freq));
```

## APPENDIX B

### ASYMMETRIC STRUCTURE ISSUE

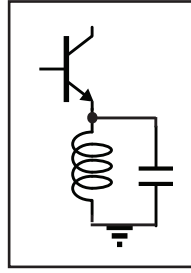
The transistors were measured in this work are in the common-emitter configuration as seen in Figure B.1 (a). In a common-emitter transistor, the input is given to the base node and the output is received over the collector. Ideally, upper and lower pad frame pairs are tied to ground. However, the transistor structures used in this work has asymmetric structures in which the bottom pad frames are not tied to the ground (see Figure B.1 (b)). In such case the returning path of the current gets longer and this path has an inductive behaviour at the frequencies lower than the resonant frequencies whereas it is capacitive at high frequencies higher than the resonant frequencies.



**Figure B.1.** The common-emitter configuration. (a) Symmetric structure, and (b) Asymmetric structure)

It should be noted that in order to make a reliable comparison of the model and measurement, the effect of this ground path has been taken into account and modelled as an inductor in parallel with a capacitor associated with the emitter of

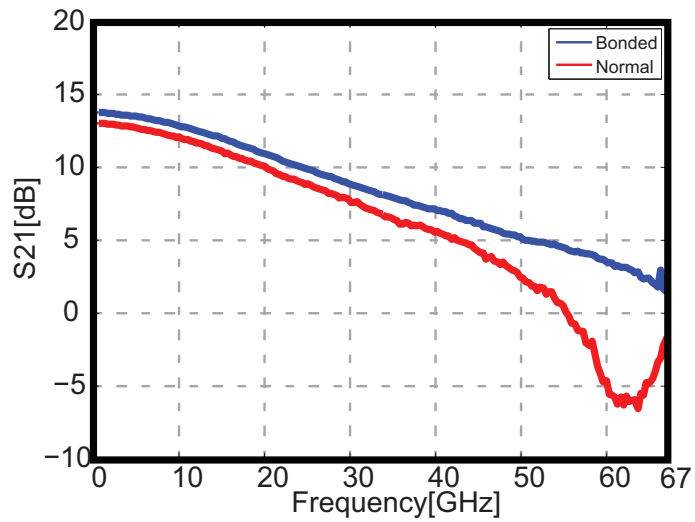
the transistors(see Figure B.2). After determination of this inductor, it is removed from the equivalent circuit to extract the remaining parameters precisely.



**Figure B.2.** Equivalent circuit model of the transistor with the inductor and capacitor.

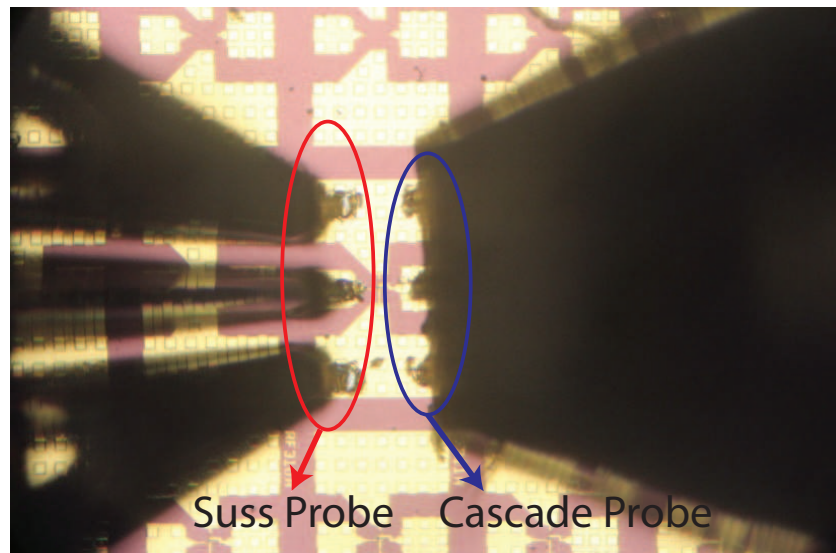
As described above, this equivalent circuit has an inductive behaviour for the frequencies lower than the  $\omega_r$ . Thus, the value of this inductor is determined from the active-bias measurement by using the expression is shown below.

$$L_e = \frac{\Im\{Z_{12}\}}{\omega} \quad (\text{B.1})$$



**Figure B.3.** The effect of the inductor on the measured s-parameter.

The effect of this inductor can be seen in the Figure B.3. In order to prove the effect of this inductor, we have bonded the bottom and top pad frames to shorten the ground path. With shorting pad frames we have observed that the resonance has gone. After proving this shortcoming of the integration process, fortunately, by changing the probes we were able to shift this resonance to higher frequencies which helped us to perform accurate measurements. Moreover, the length of the probe tips that were used for the initial measurements are longer than the one was used for final measurements. From the Figure B.4, it is seen that Cascade probe has a shorter probe tip length which means the length of the ground loop shorter in comparison to the SUSS probe. Therefore, the inductance of this loop decreases which shifts the resonant frequency to higher frequencies.

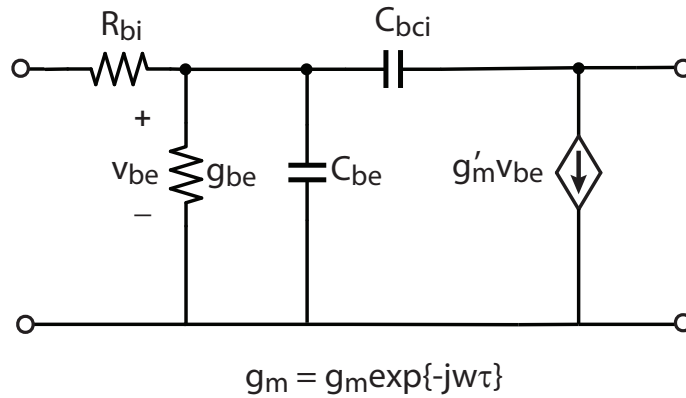


**Figure B.4.** The photo of the probe tips.

## APPENDIX C

### THE INTRINSIC NETWORK DERIVATIONS

As discussed in Chapter 2, the small-signal equivalent circuit consists of the bias independent extrinsic network and bias dependent intrinsic network. Once the extrinsic component are determined, they are removed from the entire circuit to obtain intrinsic network. The intrinsic network includes six parameters that are;  $R_{bi}$ ,  $C_{bci}$ ,  $C_{be}$ ,  $g_m$ ,  $g_{be}$  and  $\tau$  as seen in Figure C.1.



**Figure C.1.** Bias dependent intrinsic network.

$R_{bi}$  is extracted and removed as discussed in Chapter 2. From the remaining circuit the rest of the parameters are extracted using the following equations.

$$Y_{11} = \frac{I_1}{V_1} \Big|_{V_2=0} = j\omega(C_{bci} + C_{be}) + g_{be}, \quad (\text{C.1})$$

$$Y_{12} = \frac{I_1}{V_2} \Big|_{V_1=0} = -j\omega C_{bci}, \quad (\text{C.2})$$

$$Y_{21} = \frac{I_2}{V_1} \Big|_{V_2=0} = g_m \exp(-j\omega\tau) - j\omega C_{bci}, \quad (\text{C.3})$$

$$Y_{22} = \frac{I_2}{V_2} \Big|_{V_1=0} = j\omega C_{bci}, \quad (\text{C.4})$$

Once  $Y$ -matrix is determined, intrinsic parameters are extracted using following expressions.

$$C_{bci} \approx -\frac{\Im \{Y_{12}\}}{\omega} \quad (\text{C.5})$$

$$g_m \approx |Y_{21} - Y_{12}|, \quad (\text{C.6})$$

$$\tau_d \approx -\frac{\text{phase} \{Y_{21} - Y_{12}\}}{\omega}, \quad (\text{C.7})$$

and finally,

$$g_{be} \approx \Re \{Y_{11} + Y_{12}\}. \quad (\text{C.8})$$



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