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Development of a Solid-State Doppler Marine Radar

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DEVELOPMENT OF
A SOLID-STATE DOPPLER MARINE RADAR

A Thesis Presented

by

GITA PATHAK

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To my family and friends.

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CHAPTER 1

INTRODUCTION

The dynamic nearshore region extends seaward from the shoreline to just beyond the breaker zone. Information regarding this region's hydrodynamic processes and morphological changes can be gathered to produce quantitative estimates of present and future nearshore physical conditions. Video cameras are often used to monitor this zone from a remote location but can only operate during daylight and fair weather conditions. Radars, on the other hand, are not bound by these limitations and, therefore, provide a solution to the limitations associated with video cameras.

Radar measurements have been conducted to produce estimates of ocean processes that increase our understanding of ocean dynamics. In World War II, Plan Position Indicator (PPI) display radars were first introduced aboard ships for the objective of target detection and ranging [2]. The data collected by these radars included Bragg scattering from the ocean surface and was classified as environmental clutter. In 1985, Young et al. performed a 3-dimensional Fourier transform analysis on a sequence of radar images [3] collected by equipment that was mounted on an oil platform in the open sea. With prior knowledge of the water depth, the frequency wave spectra were derived from the wavenumber spectra using linear wave theory. From this, a method for estimating near surface currents was established. Later in 1994, McIntosh et al and Frasier et al conducted experiments based primarily upon the study of the nearshore zone [4, 5]. From a location on a pier, at near-grazing angles, the wave vector-frequency spectra were derived from the recorded Doppler shifts and backscatter signature of the ocean due to the high resolution of the radar. Further tower-based experiments were conducted by Bell in 1995 [6], with cliff-side installations

overlooking the beach. Results from Bell's study revealed that the shoaling and refracting of the waves prevented the wavenumber spectra from producing a full variation in the wave parameters. This showed that the scattering which occurs in the nearshore zone is more complex than that in the open sea. More recently, in 1998, Dittmer and Ziemer created the Wave Monitoring System (WaMoS)[7], which uses commercially available X-band nautical radars to calculate the surface wave spectra and near surface current. Most watercraft have these navigational radars onboard enabling them to use their existing equipment to gather data on currents and waves with minimal cost and effort [8].

The Microwave Remote Sensing Laboratory (MIRSL) at the University of Massachusetts (UMass) modified a Raytheon MK2 navigational radar for the purpose of estimating nearshore currents. This radar was altered to employ a coherent-on-receive technique, which enables the high powered (25kW), incoherent, magnetron based radar to record Doppler information [9]. In 2003, MIRSL deployed this radar at the Nearshore Canyon Experiment (NCEX) to provide images of the incident wave fields and surface currents through the measurement of backscattered power and Doppler velocities [10]. Collected data contributed to nearshore processing models (i.e.: Beach Wizard, Comprehensive Community Model for Physical Processes in the Nearshore) and was compared to other remote sensing techniques (video) [11] and in situ measurements to identify scattering mechanisms observed during the experiment [10]. Although the radar was adequate for the purposes of the experiment, providing a visible incident wave field in radar backscatter images, it provided less than desirable range resolution [12]. Thus, it was desirable to build a next generation marine radar system for monitoring the ocean surface waves and velocities.

MIRSL proposed a low cost Solid State Doppler Marine Radar (SSDMR) in 2004 for monitoring of the ocean surface waves and velocities. The radar uses frequency modulation and pulse compression to produce improved spatial resolution and Doppler frequency stability compared to the radar deployed in 2003 at NCEX. The transmitter employs a low-power (10W) semiconductor-based power amplifier. Using solid-state technology enables

the transmitted signal to have a linear phase compared to magnetrons that produce the random phase found in traditional radars. The receiver is a conventional down converter integrated with a calibration loop, which allows monitoring of the transmitted signal. This coherent radar was tested in the autumn of 2006 at locations in Northampton MA, Milford CT, and Cape Cod MA.

The following chapters present the details of the Solid State Marine Doppler Radar design and operation. Chapter 2 discusses the design requirements that were considered in the Marine Doppler Radar System: operating frequency, power budget, SNR, etc. Chapter 3 describes the RF and IF subsystems design and implementation. The description includes detailed information regarding the antenna, RF/IF sections, internal calibration loop, FPGA, digital chirp generator, and software code. Different parts of the Data Acquisition System (DAQ) as well as the Radar Control Unit (RCU) are also discussed in this chapter. Chapter 4 gives some observations on tests conducted to demonstrate the performance of the radar. Chapter 5 summarizes what was learned from this radar and concludes the thesis.

CHAPTER 2

MARINE RADAR THEORY

2.1 Scattering Theory

On the ocean surface, the microwave backscatter is dominated by the reflection of electromagnetic waves from the short capillary waves. Capillary waves are generated by the wind and have very small amplitudes that are generally less than 3cm in height. Bragg scattering is the dominant source of backscatter from the ocean surface for vertically polarized radar signals (VV, vertically polarized transmission and vertically polarized reception) at large incidence angles. The surface must have characteristics that include roughness and a periodic distribution in the direction of the wave propagation, whose spacing is equal to half of the wavelength projected onto the surface. The relationship between capillary waves, wind, and instances of Bragg scattering is depicted in Figure 2.1.

Radars are primarily sensitive to the waves traveling along their line of sight. For Bragg scattering to occur, the periodic perturbation on top of the ocean surface waves must have a wavelength of half the radar's wavelength:

$$\bigwedge_w = \frac{\bigwedge}{2\sin(\theta_i)}, \tag{2.1}$$

where $\bigwedge$ is the electromagnetic wavelength of the transmitted signal, $\bigwedge_w$ is the physical wavelength of the ocean waves and θ_i is the local incidence angle.

The Solid State Doppler Marine Radar employs an X-band Radio Frequency (RF) of 9.875GHz, or $\lambda_{em} \approx 3cm$. This allows the transmitted signal to interact with small capillary waves with a $\bigwedge_w \approx 1.5cm$.

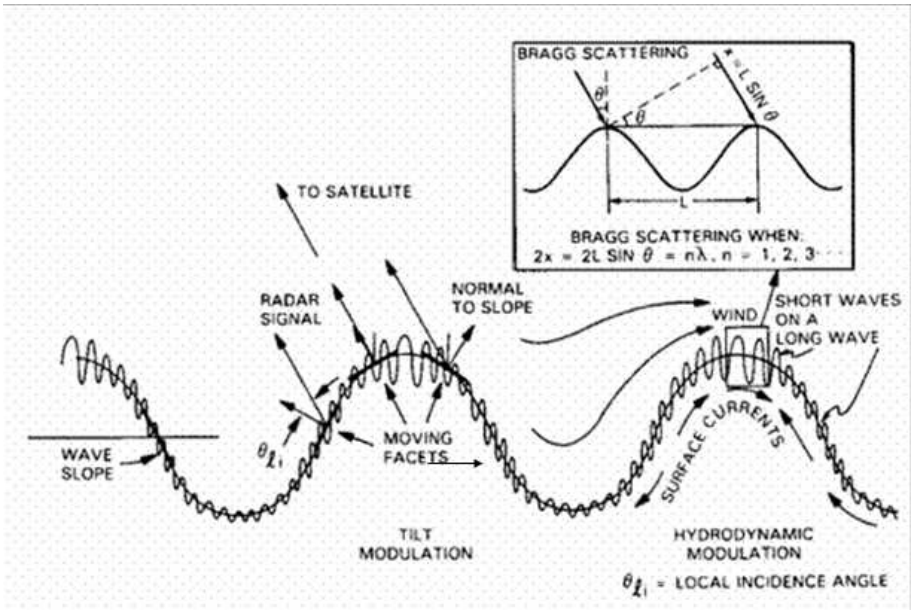

Figure 2.1. The relation of gravity waves, capillary waves and wind is illustrated in this diagram. Bragg scattering is also depicted. [13]

2.2 Signal to Noise Ratio (SNR)

The ability to detect ocean waves and their velocities depends on the radar's location, sensitivity, environmental conditions, and ability to record Doppler information. Figure 2.2 shows the Marine Doppler Radar's placement with respect to the nearshore zone. Using this figure, the sensitivity of the radar can be found.

The radar's sensitivity can be determined using the Radar Range Equation given by:

$$SNR = \frac{P_T \lambda^2 \sigma G^2}{(4\pi)^3 R^4 P_n}, \tag{2.2}$$

where P_T is transmitted power, λ is the electromagnetic wavelength, G is antenna gain, σ is the radar cross section, R is range to the target, and P_n is the noise power. The radar's transmit signal has a center frequency, f_c, of 9.375GHz (λ=3cm) and a peak power of 10W (P_T). The antenna used with this radar has a gain of 30dB. Equation (2.3) shows the radar cross-section calculation with respect to the backscattering coefficient, σ°, or the

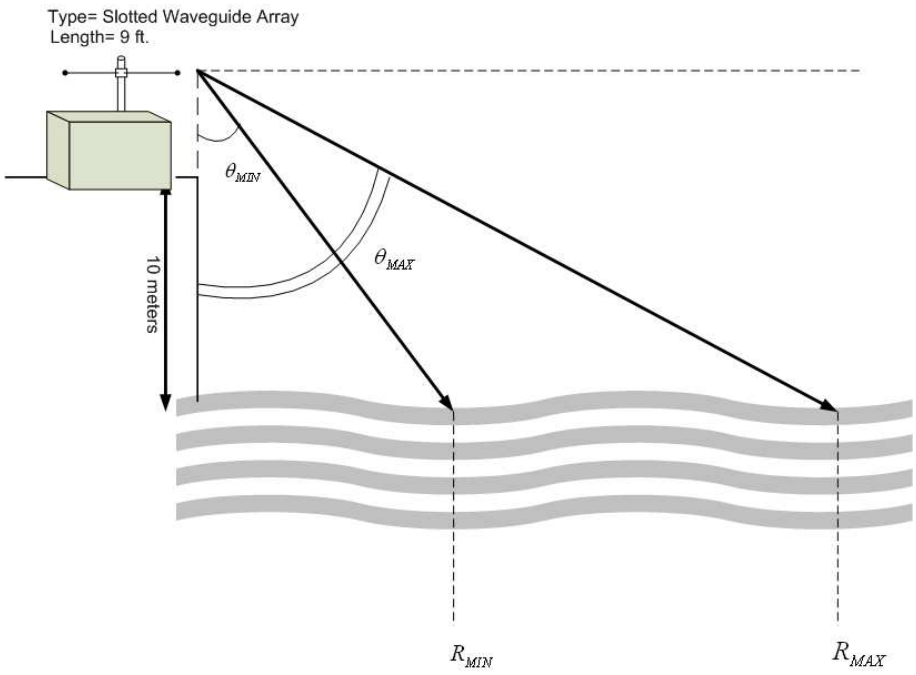

Figure 2.2. Proposed Deployment Scenario

Normalized Radar Cross Section (NRCS). For ocean wave backscatter, with near grazing antenna look angles, a typical value for σ° is -40dB. The NRCS is given by:

$$\sigma = \sigma^\circ dA = \sigma^\circ R dR d\theta, \tag{2.3}$$

where σ is the radar cross section (m^2), σ° is the NRCS, and dA is the illuminated area. The resolution area, dA, defines the maximum precision with which the radar can detect a wave and its associated period. The ground range resolution, dR, can be computed by (2.4), where c is the speed of light, τ_{eff} is the effective pulse width (before compression), and θ_d is the angle of incidence. The resolution area of this radar is $3m^2$, therefore, the minimum detectable wavelength of an ocean wave, λ_w, is 6m.

$$dR = \frac{c\tau_{eff}}{2\cos(\theta_d)} = R_2 - R_1 \tag{2.4}$$

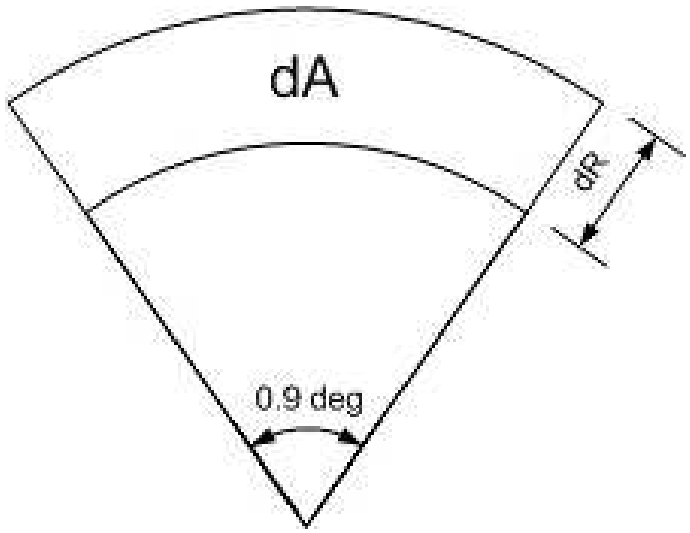

Figure 2.3. Antenna horizontal beamwidth depicting range resolution area, dA, where dR is the ground range resolution.

The sensitivity of the radar also relies upon the receiver noise power, P_n. The parameter P_n can be found by using (2.5), where k, Boltzmann's constant, is $1.38x10^{(-23)}$ (J/°K), T, the ambient temperature, is 290°K, and B is the system bandwidth, 50MHz. The noise figure, F_n, can be calculated using (2.6). Each active microwave device has a specified noise floor, F_n and an associated gain G_n. These values are then placed into the equation in order of device appearance in the chain in order to evaluate a comprehensive noise figure. Substituting these values in 2.5, the theoretical noise power of the receiver is -90.52dBm.

$$P_n = kTBF_n \tag{2.5}$$

$$F_n = \frac{SNR_{in}}{SNR_{out}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{2.6}$$

Analyzing the radar range equation, (2.2), the relation of the radar's Signal to Noise Ratio of one pulse (SNR_1) to its detectable range can be found. A plot of the SNR_1 versus range distance is shown in Figure 2.4. The radar's SNR with respect to range can be improved by pulse compression (discussed further in Section 2.3), this is achieved by coding

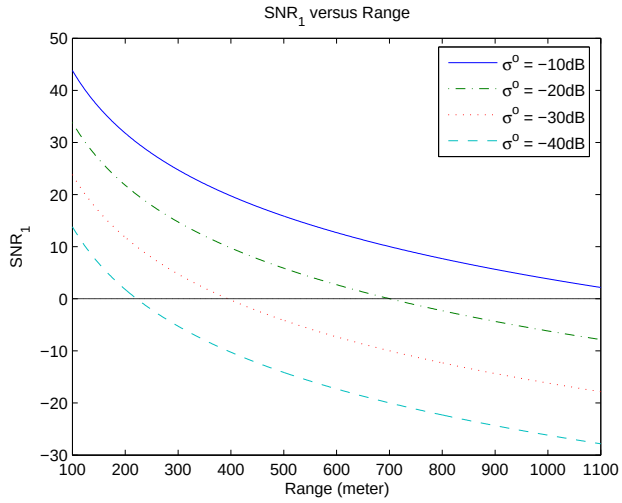

Figure 2.4. A plot of the radar's SNR_1 versus the detectable range is shown. The SNR_1 is calculated using the theoretical values of the radar components.

a narrow pulse into a long pulse for transmission and decoding the received echo into a narrow pulse during processing [14]. This enables the radar to maintain a fine resolution, which is associated with narrow pulses, while also lowering its peak power requirement. Increasing the pulse duration causes the radar's average power to increase. This process adds excess gain, called Pulse Compression Gain (PCG), that is equal to the pulse's bandwidth-time product given by:

$$PCG = G_c = B\tau = \frac{\tau}{\tau_{eff}}, \tag{2.7}$$

where τ is the compressed pulse width and τ_{eff} is the effective pulse width before compression. The new SNR_1 versus detectable range with PCG taken into account is shown in Figure 2.5.

$$SNR_1 = \frac{P_T \lambda^2 \sigma G^2 G_c}{(4\pi)^3 R^4 P_n}. \tag{2.8}$$

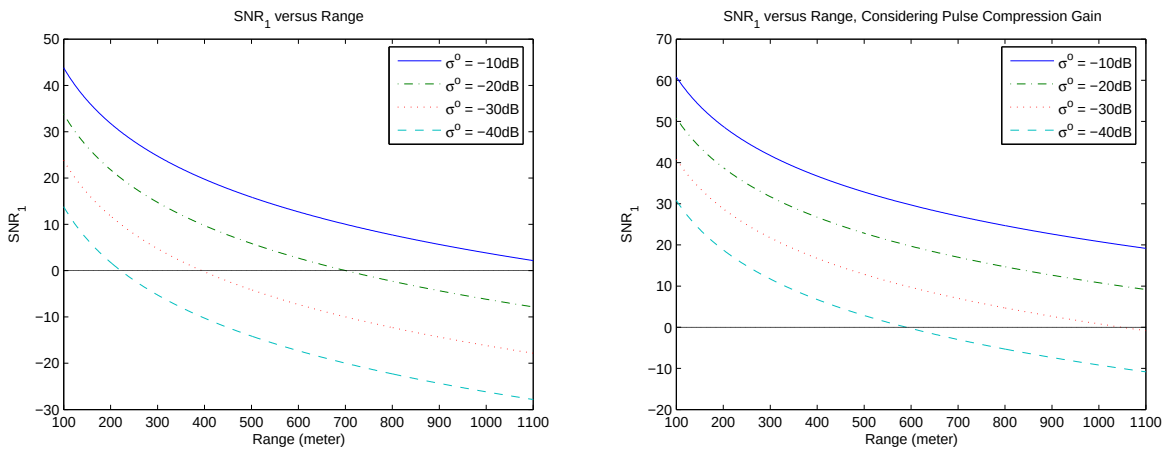

Figure 2.5. The radar's SNR versus the detectable range are shown above. The plot on the right takes PCG into consideration, using a pulse width of 1μs while the left on excludes it.

2.3 Pulse Compression

The radar's range resolution is dependent on the transmitted pulse bandwidth, as shown in (2.9). It is desirable to have a transmitted pulse that enables both high resolution and detectability by the receiver. The time duration of the pulse is inversely proportional to the bandwidth and, thus, a shorter pulse time duration yields higher resolution. The received signal becomes easier to detect if the pulse has either a long time duration or a higher power, which translates to the transmitted signal initially having a higher power. To increase the power level of the transmitted signal, high voltage power supplies can be utilized (i.e.: magnetron). These power sources are often unreliable, extremely heavy, and are very costly. If this method is chosen, the devices located after the high power signal source must also be capable of handling the same power and pulse duration. These devices can also become costly. One method that will enable the transmitted pulse to provide high resolution as well as easy detectability by the receiver is by using pulse compression.

$$dA = \frac{c\tau}{2} = \frac{c}{2B} \tag{2.9}$$

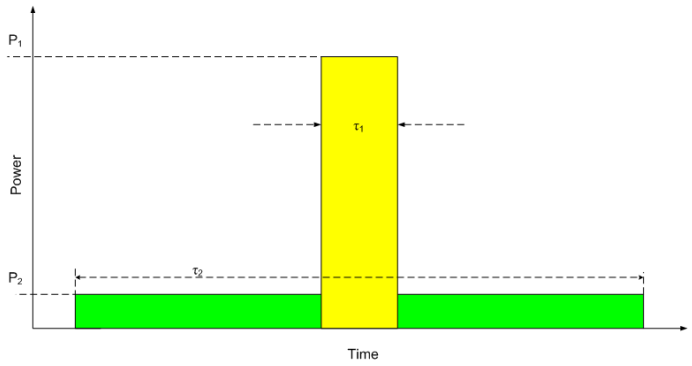

Figure 2.6. The comparison of a pulse with a long duration and low power is energy comparable to a pulse with short duration and high power.

Pulse compression enables the radar to transmit a long time duration pulse that has the bandwidth corresponding to a shorter pulse. The energy associated with the longer pulse that has low power is equivalent to that of a shorter pulse with higher power. To enact pulse compression, the radar uses Linear Frequency Modulation, shown in Figure 2.7. This allows the signal to have the frequency be linearly stepped within the pulse width. The linear frequency modulation can be characterized by:

$$s(t) = Acos(2\pi f_c t + 0.5kt^2 + \phi_c) \;\; for \;\; 0 \leq \tau \leq t, \tag{2.10}$$

where f_c is the center frequency of the chirp in Hz and k is the chirp rate in Hz per second. By implementing this, the transmitted signal has a higher pulse width, higher bandwidth than that of the resulting pulse width allowance, and lower power.

Using Linear Frequency Modulation (LFM) pulse compression affects the signal in two ways. First, there is the added effect of PCG which was discussed in Section 2.2. Second, reception becomes problematic due to the appearance of time-sidelobes in the received signal. On receive, the signal passes through a matched filter and the envelope of the output signal is proportional to $sin(\pi Bt)/(\pi Bt)$, as shown in Figure 2.8. This contains peak time-sidelobes of 13.2dB below the main signal. High sidelobes can increase the

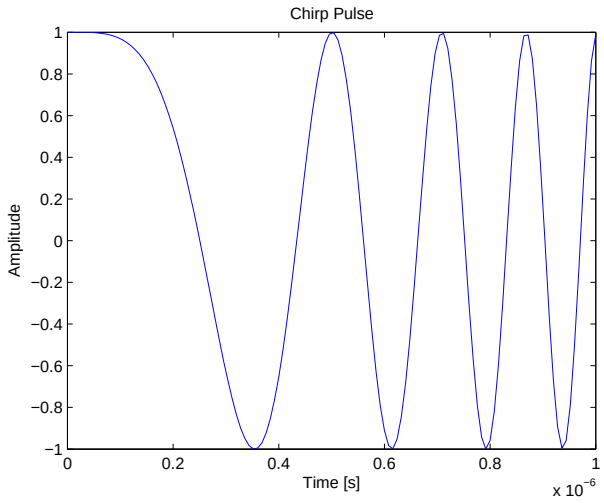

Figure 2.7. A transmitted waveform for a chirped radar using frequency modulation and a pulse width of 1μs.

amount of false alarms and/or mask weaker target echoes. Conducting digital windowing of the signal by the use of a weighting function before frequency analysis will reduce time-sidelobes. Applying this method only on receive causes the matched filter to become mismatched therefore causing a loss in SNR [9]. If windowing is applied, the benefits of pulse compression usually outweigh the problems encountered. Some common weighting functions with their correlating properties are displayed in Table 2.1.

Table 2.1. Properties of Weighting Functions

Function	Peak Sidelobe [dB]	Loss [dB]	Mainbeam Width (Relative)
Taylor ($\bar{n} = 6$)	-40	1.2	1.4
Hamming	-42.8	1.34	1.5
Uniform	-13.2	0	1.0
Dolph Chebyshev	-40	–	1.35
$0.33 + 0.66\cos^2(\pi f/B)$	-25.7	0.55	1.23
$0.16 + 0.84\cos^2(\pi f/B)$	-34	1.0	1.4
$\cos^2(\pi f/B)$	-31.7	1.76	1.65

[9]

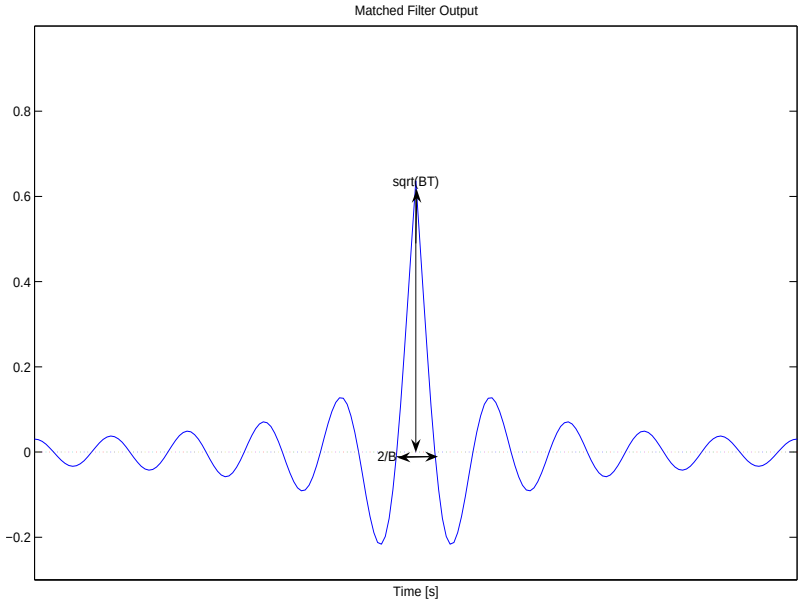

Figure 2.8. The output signal of a pulse compression filter, also known as a matched filter. The output waveform is the autocorrelation of the input signal to the digital filter.

2.4 Radar's Dynamic Range

The dynamic range of a radar system is limited by the noise figure of the receiver, P_{min}, and the maximum detectable signal, P_{max}, of the Analog to Digital Converter (ADC). Dynamic range, DR, is then expressed by:

$$DR = P_{max} - P_{min}, \tag{2.11}$$

$$P_{max} \mid_{ADC} = 10log(\frac{V_{RNG}^2}{2R_L}) + 30[dBm], \tag{2.12}$$

$$P_{min} \mid_{ADC} = 10log(\frac{(V_{RNG}/2^n)^2}{2R_L}) + 30[dBm]. \tag{2.13}$$

The signal limitations can be calculated by using 2.12 and 2.13, where V_{RNG} is the maximum voltage detectable by the ADC, R_L is the input impedance of the ADC, assumed to be 50Ω, and n is the number of bits of the ADC. The upper limit of the signal power is

dictated by the ADC full scale signal limitation, whereas the radar receiver system noise floor is the small signal limitation. Sampled signals must be within the dynamic range of the system to be detected.

The dynamic range of the A/D converter is directly related to the overall gain of the radar receiver. This gain is equal to the level detected at the A/D converter input plus the noise floor of the receiver:

$$G_{min} = P_{min} + P_n[dB] \tag{2.14}$$

$$G_{max} = P_{max} + P_n[dB]. \tag{2.15}$$

Here P_n is the receiver noise power as discussed in Section 2.2. Thus,

$$G_{min} = -68 + 90.5 = 22[dB]. \tag{2.16}$$

This calculation shows that the receiver must have a minimum gain of 22dB for the ADC to detect the received signals. Similarly, the maximum gain of the receiver must not exceed 106dB.

2.5 The Doppler Effect

If a relative motion exists between the radar and target, then a corresponding shift in frequency is observable in the signal echo. This shift in frequency is known as a Doppler shift. Consider a situation where a target is located a distance, R, away from the radar and is within the radar's antenna beam. Then the two way path between the radar and the target has $2R/\lambda$ total wavelengths, where each wavelength corresponds to an angular phase change, ϕ, of 2π radians. If the target is stationary with respect to the radar, then the phase is constant over multiple returns. On the other hand, if the target is moving with respect to the radar, then the phase will vary from pulse to pulse. The rate of phase change is known as the Doppler angular frequency, ω_d, and is defined in (2.17), with ν_R being the radial velocity of the target with respect to the radar. The corresponding shift in frequency

is defined in (2.18). The angle between the radar antenna and the target with respect to the surface normal is θ, and is depicted in Figure 2.2. [15, 9]

$$\omega_d = \frac{d\phi}{dt} = \frac{4\pi}{\lambda}\frac{dR}{dt} = \frac{4\pi\nu_R}{\lambda} \tag{2.17}$$

$$f_d = \frac{2\nu_r}{\lambda}\sin(\theta) \tag{2.18}$$

To reconstruct a Doppler shift, the Nyquist theorem states that the maximum f_d must adhere to the constraint: PRF$> 2f_d$. Using a PRF of 1.25kHz and (2.18) the radar can sense an unambiguous range of radial velocities from approximately $\pm$9.6m/s.

CHAPTER 3

SYSTEM DESCRIPTION

The SSDMR was designed, built, and tested with the objective of accurately detecting ocean surface waves and their velocities. The radar system transceiver diagram is shown in Figure 3.1. The transmit chain consists of the Radar Control Unit (RCU), a chirp pulse generator, an up-converter, and a power amplifier. A single antenna is used for both transmitting and receiving. A typical down-converter scheme is used for the receive chain. The received signals are downconverted and demodulated into respective In-phase (I) and Quadrature (Q) components before digitization. Raw data is sampled and stored onto the DAQ computer with minimal processing. A calibration loop was included to enable sampling of the transmitted signal. The oscillators are all phased locked to a 10 MHz reference clock (Miteq, XT-01-10-B-15P). For deployment, all radar components, shown in Figure 3.2, are mounted onto a truck bed. Computer peripherals and the DAQ computer are also packed into the truck for usage at the deployment site. Remote monitoring from another location can be established if an internet connection is provided at the deployment site. The following sections detail implementations of the devices used in the design.

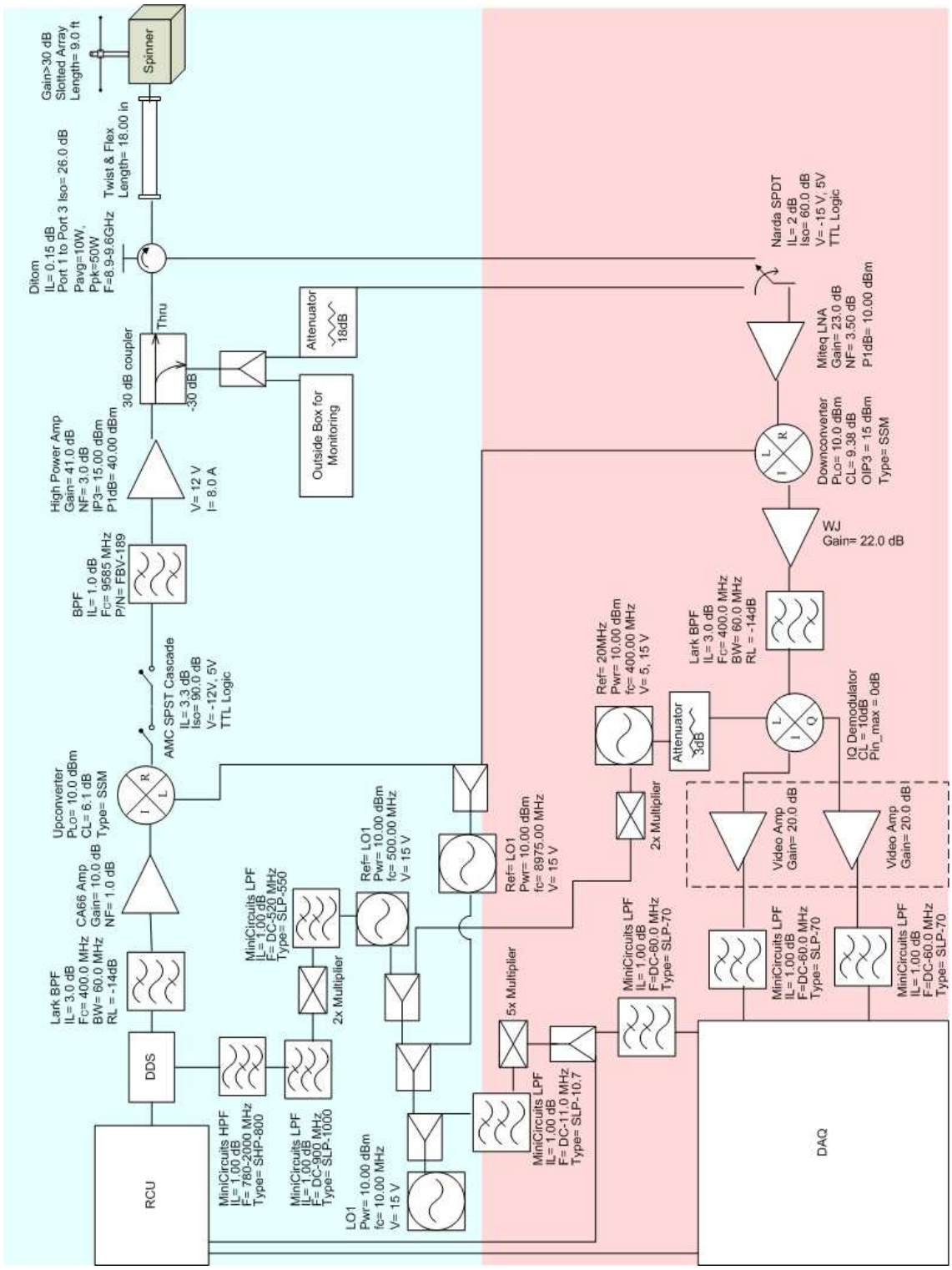

Figure 3.1. The block diagram of the Solid-State Doppler Marine Radar transceiver. The transmit section is shown in blue while the receiver section is depicted in red.

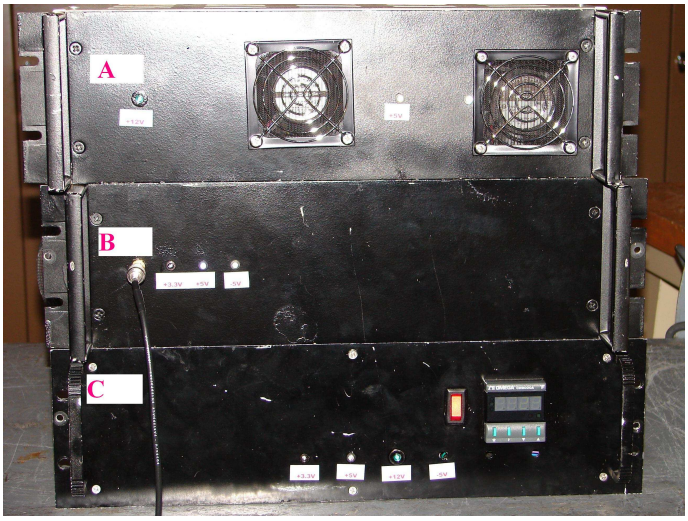

Figure 3.2. The rack mountable radar boxes comprising the radar RF/ IF systems are shown above. In the picture above, A: Transceiver Box (RF/IF Subsystems and Oscillator Chain), B: Radar Control Unit Box (RCU computer, FPGA, Buffer Board, and Direct Digital Synthesizer), and C: Power Box.

3.1 RF Subsystem

The RF transmit subsection, shown in Figure 3.3, receives an IF chirp pulse centered at 400MHz as an input. The signal is up-converted using a Single Side-band Mixer (SSM) (WJ, M38UC-400) to 9.375 GHz via an 8.975GHz Phased Locked Oscillator (PLO) (Herley-CTI, XPDRO-8346), which is phase locked to the 10MHz reference oscillator. After the SSM, the signal enters a preamplifier switching stage, then it passes through a generic Band Pass Filter (BPF, P/N:FBV-189) that is used to ensure attenuation was applied to any extra spurious signals that are located outside the bandwidth of the radar ($9.3-9.4$GHz). The preamplifier switching stage is comprised of two American Microwave switches (SP2T, SW2183-1AT) that provide a nominal combined isolation of 90dB on receive, such that the combined insertion loss of the two switches is -3.8dB when the radar is transmitting. The cascade of these two switches lowers the input noise into the Solid State Power Amplifier (SSPA), while the radar is in the receive mode. In the ideal case, a high

power switch could be placed after the SSPA, but many problems with the switch manufacturer prevented the implementation of this scheme. The amplifier also has the capability to have its amplification toggled on and off by a Transistor-Transistor Logic (TTL) control signal. This could toggle the 10W amplification without the need of extra time for the amplifier to warm up. However, after discussions with the manufacturer it was determined that the switching time specified for the SSPA TTL signal is 1 ms. The radar's PRF is 1.25kHz, or 0.8 ms, therefore the TTL signal on the SSPA can not be used. During transmission, the signal, with an input power level of 2.28dBm, enters the SSPA (MA-LTD, AM53-9.1-9.6-40-40) with a gain of 41dB. The signal is then passed through the low loss port of the high power coupler (Triangle Microwave Incorporated, YL-78) and into the circulator (Ditom, D3C8596) for low loss routing through a waveguide (Airtron Incorporated, CG-182/AMP-40(18")) to the antenna for transmission. All components in the transmit chain located after the SSPA are capable of handling 10W peak power with little insertion loss. The transmit leakage into the receiver path during reception is discussed below and in Section 3.4.

The RF receiver subsection obtains an input from the antenna through the circulator. During receive, the signal enters the receiver switch (Narda SP2T, S123D) with 60dB of isolation (2dB insertion loss); this lowers the transmission noise leakage that can combine with the received signal. The switch is connected to the calibration loop during transmit for two reasons. It enables the receiver to sample the attenuated transmit signal, and it omits the reflections from the waveguide antenna for better comparison with the receive signal during data processing. The signal is then routed through a Low Noise Amplifier (LNA) (Miteq, AFS4-02001800-35-ULN) with 23.6 dB gain and 3.08 dB noise figure (NF). The maximum input power level to the LNA is -12 dB, to avoid saturation. A Double Sided Mixer (DSM) (WJ M38DC-400) then downconverts the signal to IF. The same PLO is used to mix the signals up and down to/from the RF frequency. Table 3.1 summarizes the specifications of the RF transmitter and receiver sections, respectively. The control signals for the switches in this subsystem are created and managed in the Radar Control Unit (RCU), discussed

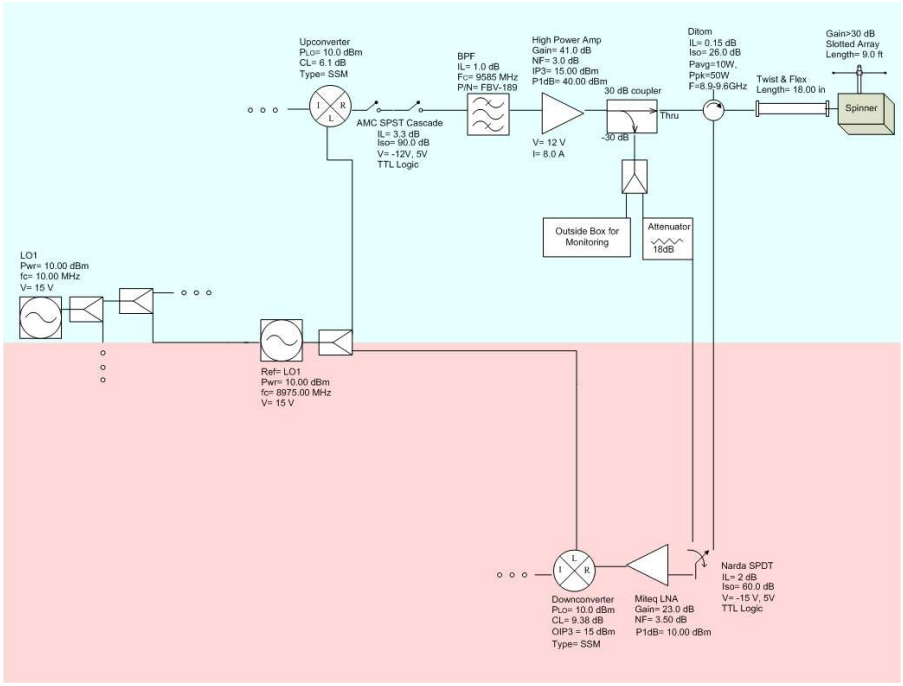

Figure 3.3. Block diagram of the RF subsection. The transmit section is shown in blue while the receive section is in red.

further in Section 3.6. Table 3.2 shows the switching states according to the control signal level. All switching control signals are created to achieve cold switching, or switching the state while no or extremely low power is applied at the input of the switch.

The RF subsystem, contains two paths that allow the transmit signal to leak into the receiver section. First, the transmit signal can leak into the receiver through the circulator, which has a 20dB isolation between Port 1 (where the transmit signal enters) and Port 3 (where the receive signal is routed to the receiver). During transmission, the signal leaks from Port 1 to Port 3 and is able to enter the receiver. This power level was not able to be measured, but the equation shown in 3.1 shows expected leakage power level. The leakage level was found to be within an acceptable range; the receiver switch supplies an extra 60 dB of isolation during transmission. This causes the leakage lie below the noise floor of the Gage card, as discussed in Chapter 4. The transmit noise floor leakage into the receiver via the circulator during transmit and receive mode is shown in Figures 3.4 and

Table 3.1. RF Section Specifications

Parameter	Value
Transmit Section	
Frequency of Operation [GHz]	9.375
Transmit Power [W]	$<$10
Tx Noise Figure at output of coupler [dB]	5.5
Supply Voltages (DC) [V]	$\pm$12, 5
Input Chirp:	
Center Frequency [MHz]	400
Bandwidth [MHz]	50
Power [dBm]	2.28
Receive Section	
Supply Voltages (DC) [V]	$\pm$15, 5
Miteq LNA Gain [dB]	23
Miteq LNA Noise Figure [dB]	3.5

Table 3.2. RF Switches

Switch ID	Control Signal	Action
PreAmp Switch 1	preamp_sw	H=OFF, L=ON
PreAmp Switch 2	preamp_sw	H=OFF, L=ON
Narda Switch	rx_sw	CNTRL J3 High, CNTRL J2 Low = Circulator Port 3 CNTRL J3 Low, CNTRL J2 High = Calibration Loop

3.5. These measurements took place in September 2007, after the RCU components were dismantled, and therefore do not show the actual noise floor leakage power levels. However, these figures can provide the approximate amount of noise floor leakage the receiver is being presented with. The transmit section noise floor leakage into the receiver section is compensated for by measuring the noise floor of the receiver (with the receiver switch connected to the calibration loop), such that post processing would have the capability to remove it from the data. This is discussed in Chapter 5. The second leakage path is through the -30 dB coupler, and is discussed in Chapter 3.4.

$$P_{received} + P_{tx} - P_{circulatorisolation} = -90dBm + 41dB - 20dB = -69dBm \quad (3.1)$$

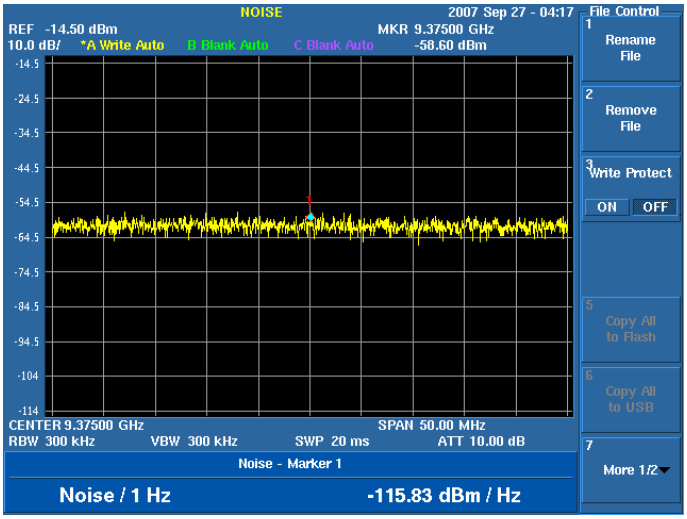

Figure 3.4. The measured transmit section noise floor leakage of -115.8 dBm/Hz (-38.8 dBm for a 50MHz bandwidth) which entered the receiver by the circulator while the radar was in transmission mode. This measurement was conducted without the RCU components (including the Direct Digital Synthesizer) and thus may not be considered as the actual leakage that was present during radar operation.

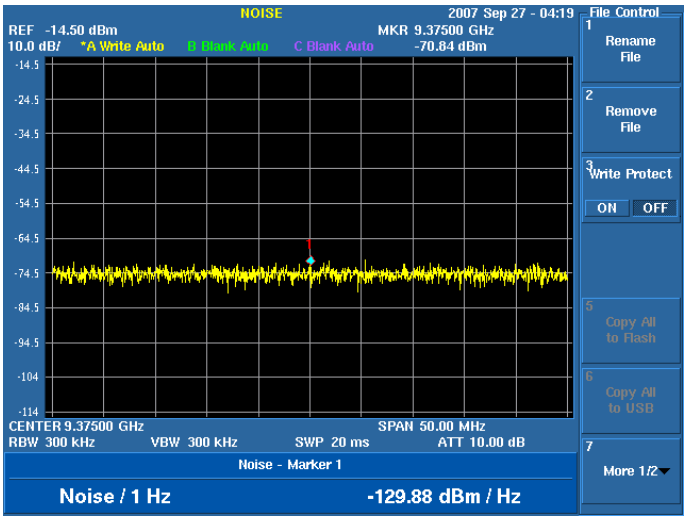

Figure 3.5. The measured transmit section noise floor leakage of -128.8 dBm/Hz (-52.8 dBm for a 50MHz bandwidth) which entered the receiver by the circulator while the radar was in receive mode. This measurement was conducted without the RCU components (including the Direct Digital Synthesizer) and thus may not be considered as the actual leakage that was present during radar operation.

3.2 IF Subsystem

The IF section has two main purposes: to create the frequency chirp centered at 400MHz and to down convert the demodulated received signal, using an IQ demodulator, before digitization. Figure 3.6 shows the block diagram of the IF subsystem.

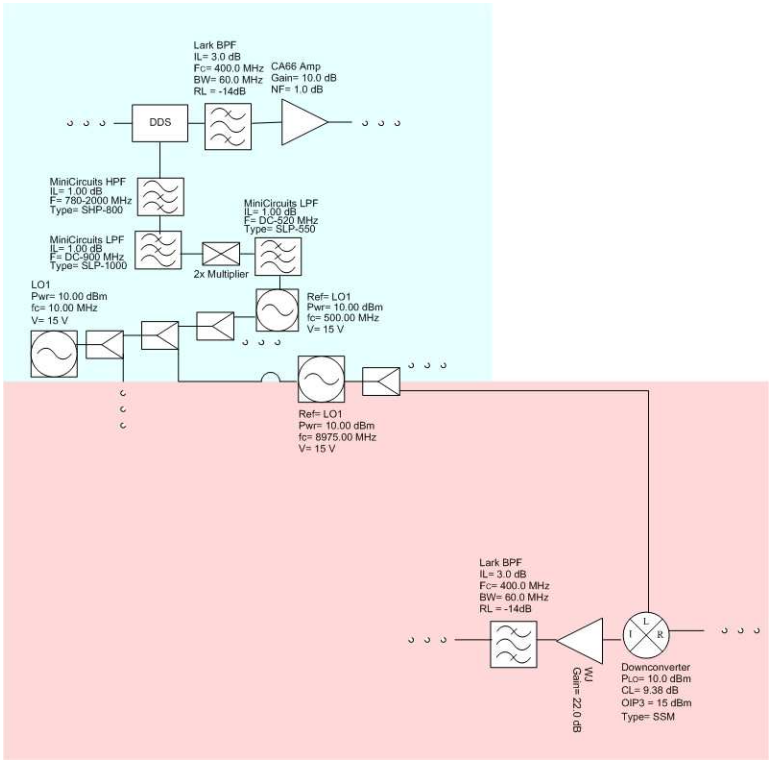

Figure 3.6. Block diagram of the IF subsection. The transmit section is shown in blue while the receive section is in red.

The Direct Digital Synthesizer (DDS), discussed further in Section 3.3, has a reference clock of 1 GHz derived from a 500MHz PLO (Miteq, PLD-1C-10-500-15P) by use of a doubler. It generates an FM waveform chirp with the specifications shown in Table 3.3. The signal is then routed to the bandpass filter (Lark, MC400-65-5AA) which removes harmonics from the DDS board. The amplifier (WJ, CA-66-1) is introduced to the IF chain to increase the power level of the IF chirp to an acceptable level for the SSM (WJ, M38UC-400) to up-convert the signal to RF.

In the receive chain of the IF section the signal is amplified by the gain stage (WJ, CA-66-1) and then bandpass filtered (Lark, MC400-65-5AA) before entering an IQ baseband demodulator (Merrimac, 10M-20A-400B). The maximum RF input level to the IQ demodulator is 0dBm. The IQ demodulator downconverts and demodulates the signal into its In-phase (I) and Quadrature (Q) components using a 400MHz reference oscillator. The bandwidth of the baseband I and Q signals is DC - 25MHz. These two signals are then amplified by a video amplifier (Texas Instruments, THS4022), with a gain of 20dB [16], and anti-aliased by a low pass filter (LPF) (Miteq, SLP-70).

Table 3.3. IF Section Specifications

Parameter	Value
Rx Noise Floor (BW=50MHz) at DAQ Input [dBm]	-43
Rx Noise Floor Including DAQ [dBm]	-65
Gage Card Noise Floor [dBm]	-78
DDS Output Chirp:	
Center Frequency [MHz]	400
Bandwidth [MHz]	50
Pulse Width [μs]	1, 0.5
Power [dBm]	2.28

3.3 Digital Chirp Generator

The SSDMR uses an evaluation Direct Digital Synthesizer board (DDS) (Analog Devices AD9858) to generate a frequency modulated (FM) chirp pulse centered at 400MHz with a 50MHz bandwidth. The board needs a 1 GHz clock reference to produce an output frequency of up to 500MHz, due to the Nyquist equation. Figure 3.7 shows the residual phase noise specification for an output frequency of 403 MHz while using a 1GHz reference clock, also denoted as the System Clock (SYSCLK). This figure shows that the phase noise produced by the board is theoretically -129dBc/Hz (-52.02dBc for a 50MHz bandwidth), excluding the additional phase noise produced by SYSCLK. The radar bases its capability

to locate targets by the phase change of the signal, so if there is noise/jitter riding on the transmitted signal, target location becomes more difficult.

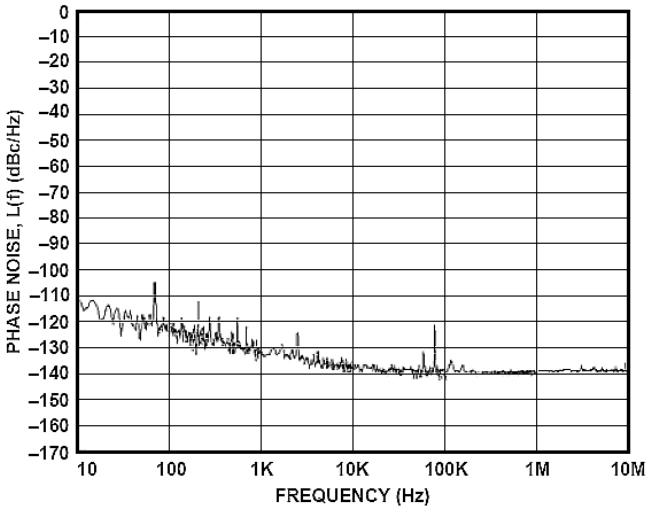

Figure 3.7. The DDS residual phase noise specification for $f_{out} = 403MHz$. This can be used for SSDMR which has $f_{out} = 400MHz$.

To produce the linear frequency chirp, the DDS operates in Frequency-Sweeping mode. This mode requires 3 tuning words: the Delta Frequency Tuning Word (DFTW), the Delta Frequency Ramp Rate Word (DFRRW), and the Frequency Tuning Word (FTW). The DFTW is the freqeuncy step increment on every clock multiplied by the DFRRW cycle. The DFRRW is the clock cycle multiplication for the Frequency Modulated (FM) ramp. The FTW is the center frequency of the chirp. Each tuning word is interrelated with another to ensure the calculated register values are correct for the chirp to be produced as desired.

$$FTW = \frac{f_s \times 2^{32}}{SYSCLK} - 4294967.296 \tag{3.2}$$

$$DFRRW = \frac{\Delta t \times SYSCLK}{8} \tag{3.3}$$

$$DFTW = \frac{|f_F - f_S| \times 2^{35}}{SYSCLK^2} \times \frac{DFRRW}{T} \tag{3.4}$$

$$f_F = f_S + T \times \frac{\Delta f}{\Delta t} \tag{3.5}$$

In (3.2 - 3.5) Δf is the frequency increment in MHz, Δt is the time between each frequency step in seconds, T is the duration of the sweep in seconds, f_s is the starting chirp frequency, and f_F is the stop frequency. With the chirp information loaded into the DDS, the Control Function Register (CFR) is able to implement pulsing of the chirp by toggling the clear frequency accumulator and clear phase accumulator bites. If these bites hold, respectively, a binary logic of "1", the chirp would stop. Likewise a binary logic of "0" restarts the chirp output waveform. The read and write capability of the DDS works on $\frac{1}{8}$SYNCLK, i.e. 125MHz. This board is managed by the FPGA, which controls all timing events for the radar; it is discussed in Section 3.6.

The radar is designed to have a variable pulse width, bandwidth, and period which are user definable in the RCU computer file, 'marine_params.dh'. The RCU computer program is designed to read in the file, appropriately calculate the DDS register values, and communicate the values to the FPGA. Table 3.4 displays the tested input specifications given by the user and the DDS output signal characteristics that are used for experiments. The DDS works according to desired specifications, with little modification to obtain the appropriate bandwidth, for τ equal to 1 and 0.5 μs, although 1μs was used during all deployments. The bandwidth desired for radar operation is 50 MHz. When inserted into the DDS equations, (3.2 - 3.5), the resulting τ is 0.87μs. To obtain both the desired 50 MHz bandwidth and 1μs pulse width, a programmed bandwidth of 57 MHz is required.

Table 3.4. DDS Input Specifications and Output Characteristics

Parameter	Value
Supply Voltage (DC) [V]	5
External Input Reference Clock [GHz]	1
Output Power Level [dBm]	2
Phase Noise Specification [dBc]	129
Programmed Chirp:	
Center Frequency [MHz]	400
Bandwidth [MHz]	57
Pulse Width [μs]	1
Output Chirp:	
Center Frequency [MHz]	400
Bandwidth [MHz]	50
Pulse Width [μs]	1
Power [dBm]	2.28

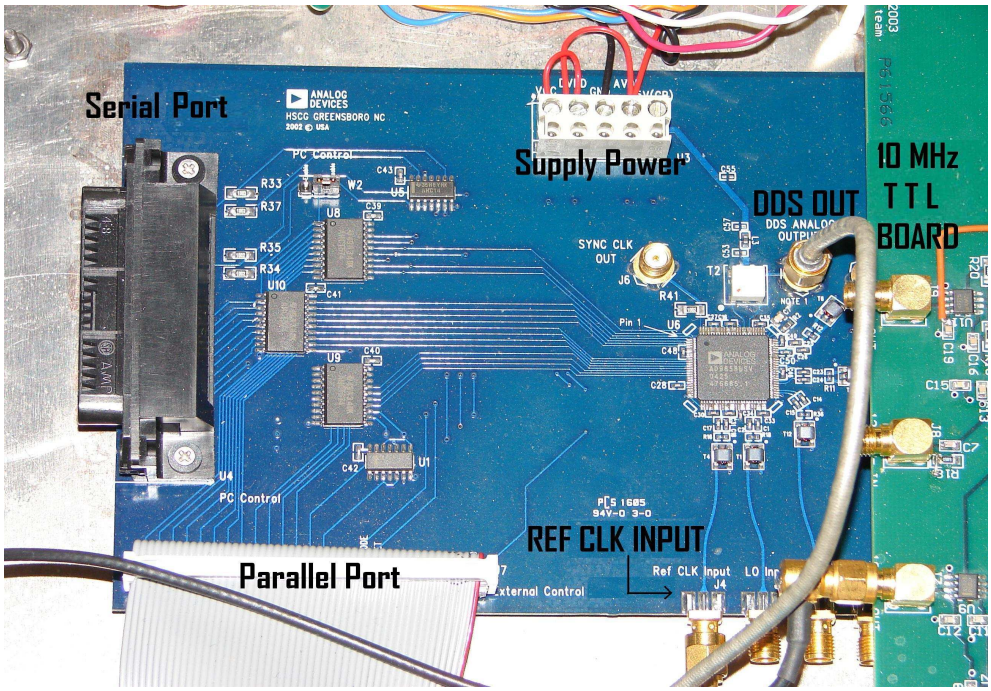

Figure 3.8. DDS board located within the RCU box of the SSDMR.

3.4 Calibration Loop

Calibration enables a radar system to provide more precise measurements. There exist two methods of calibration that can be performed on a radar system: internal (or relative) and external (or absolute). Internal calibration monitors for changes in device operation (i.e.: their phase variations). Absolute calibration is used to compare results from two different systems. The SSDMR uses phase measurements to retrieve movement information from the target, thus, internal calibration is essential in the radar. The calibration loop is incorporated for periodic sampling of the transmit signal once it has passed through both the transmitter and receiver. This provides the capability to implement a good matched filter for data compression. External calibration was conducted and will be discussed in Section 5.1.

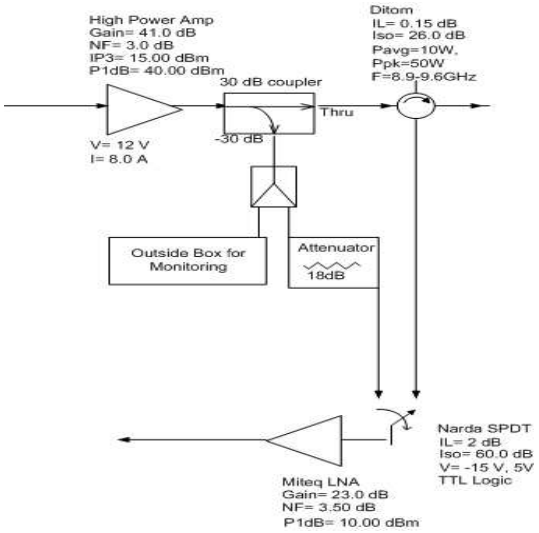

Figure 3.9. Block diagram of the calibration loop.

The SSDMR calibration loop is shown in Figure 3.9. A 30 dB directional coupler is placed directly after the SSPA to sample the attenuated transmit signal. While in transmit mode, the transmitted signal is amplified to a power level of 41dBm at the output of the SSPA. The signal is then sampled through the -30 dB coupler path, which enters the power divider, and goes through an attenuation block of 18 dB. At this location, the signal was

measured to be -13 dBm by the Peak Power Meter (HP 8911A Peak Power Analyzer). The final power level presented to the LNA was -15dBm. This is below the specified -12dBm needed to keep the LNA from saturating. This loop is also considered a leakage path, but due to the capability to control when the Gage card samples incoming data, this leakage is not viewed to be problematic.

3.5 Antenna

The Solid-State Marine Doppler Radar uses a slotted waveguide fan-beam antenna whose specifications are shown in Table 3.5. Vertical polarization allows the detection of ocean wave height. The horizontal and vertical antenna patterns are shown in Figures 3.10 and 3.11. Figure 3.11 depicts an antenna pattern evaluated from a seven foot Linear Slotted Array antenna, analyzed by the manufacturing company and given as a reference. The vertical antenna pattern has a main beamwidth of 22^o, which forces the radar to be at an elevated location in order to avoid ground clutter contamination. The antenna is mounted on a spinner that rotates at 24 rpm, which, when combined with a Pulse Repetition Frequency (PRF) of 1.25 kHz, enables the radar to transmit 8 pulses per beam in 6.9 ms.

The spinner scanning rate limits the maximum wave frequency that can be detected by the radar. The maximum frequency, f_{wave} is:

$$f_{wave} = \frac{rev}{2 \times 60s} = \frac{24}{2 \times 60s} = 0.2Hz. \tag{3.6}$$

Using (3.6), the radar has the capability to measure ocean waves with a maximum period, T, of 5s.

Table 3.5. 9 Foot Linear Slotted Array Antenna Characteristics

Polarization	Vertical
Frequency of Operation (60MHz Band) [GHz]	9.3-9.5
Gain [dB]	>30dB
Beamwidth Horizontal (-3dB) [Deg]	≤ 0.9
Beamwidth Vertical [Deg]	$22\cdot \pm 2.3$
Duty Cycle	0.001
Weight [Lbs.]	<22
VSWR	$< 1.2{:}1.0$
Peak Power [KW]	90

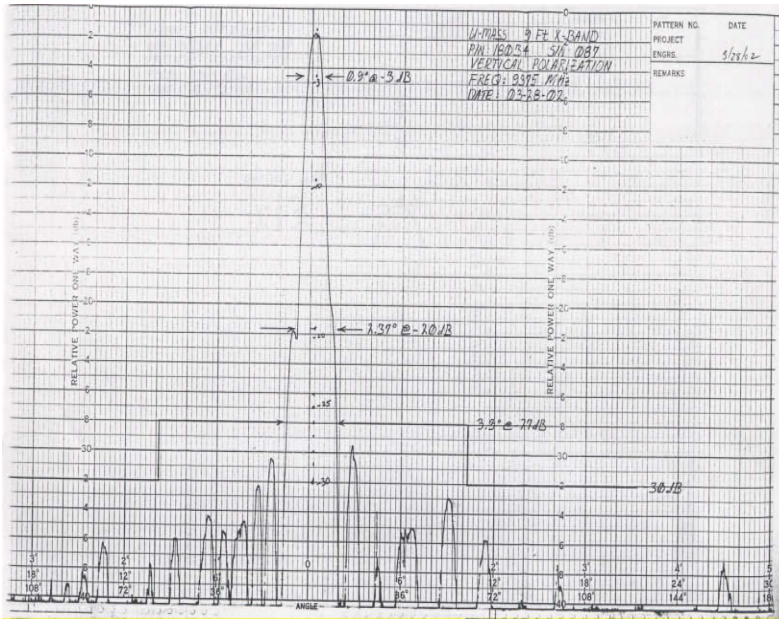

Figure 3.10. A plot of the 9 foot Linear Slotted Array antenna's horizontal pattern.

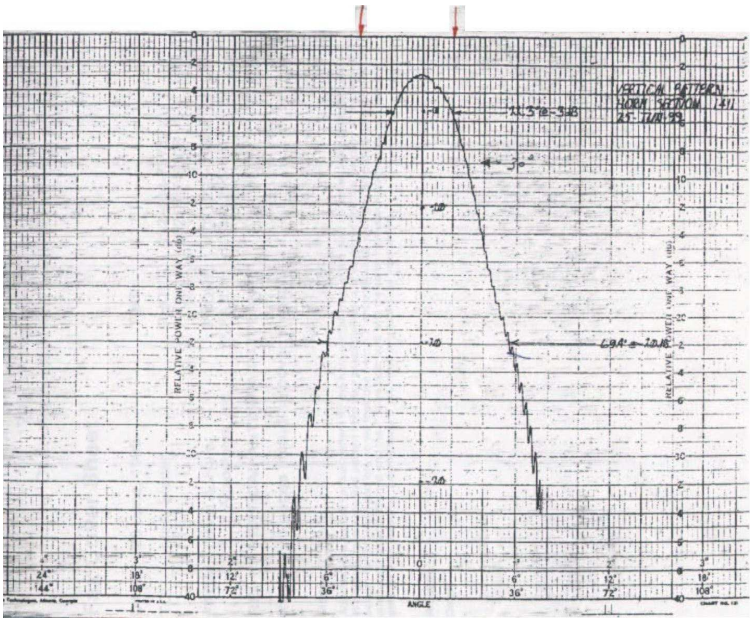

Figure 3.11. A plot of a 7 foot Linear Slotted Array antenna's vertical pattern which is applicable to the 9 foot linear slotted array purchased for the SSDMR.

3.6 FPGA

Synchronization is required to achieve coherence on receive. A Field Programmable Gate Array (FPGA) is used to create all timing and switching signals within the radar (i.e. PRF, sampling trigger, etc.). The signals that are sent out of the FPGA are routed through the custom buffer board to the intended destination. The purpose of the buffer board is to protect the FPGA from high voltage signals and convert the Low Voltage Transistor-Transistor Logic (LVTTL) to Transistor-Transistor Logic (TTL) signals. The FPGA logic design was created using Quartus, which has an output (.ttf file) that is loaded into the FPGA's Read Only Memory (ROM) chip on power up. Table 3.6 shows the main inputs and outputs of the FPGA.

The main input for the FPGA is a 50 MHz phase locked clock that is internally divided to create a FPGA system clock of 25MHz. To create the PRF, the 25MHz system clock is

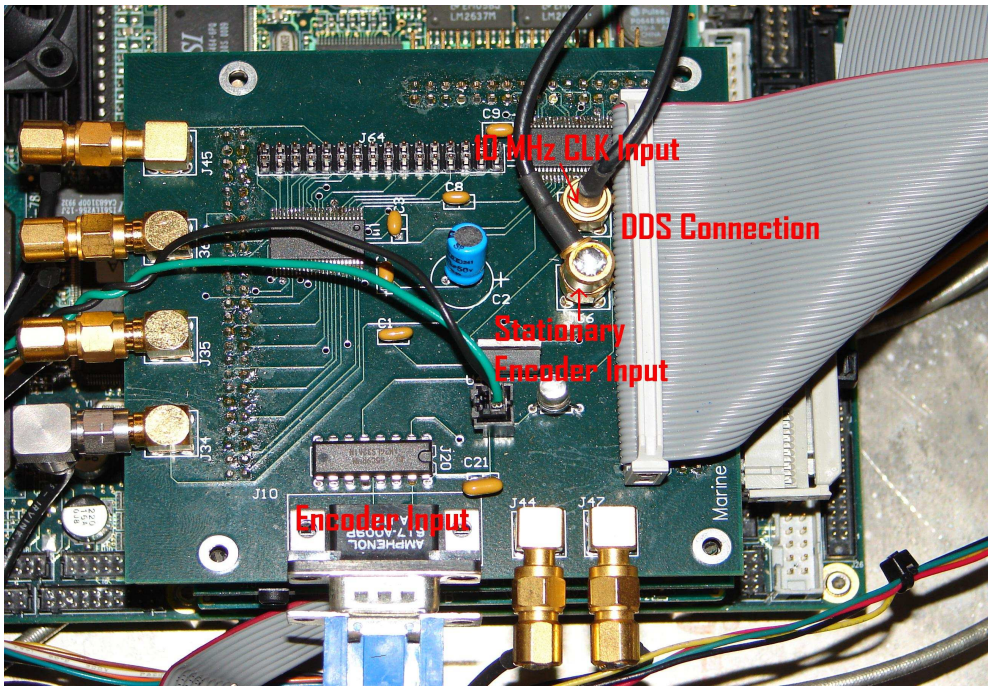

Figure 3.12. The Buffer Board was created to sit directly on top of the FPGA board to achieve a direct connection.

Table 3.6. FPGA Input and Output Signals

Parameter	Value	Origin/Destination
Input Signals:		
100mhz_in	50 MHz clock	TTL Board in RCU
DDS Tuning Words	FTW,DFRRW,DFTW	RCU
Transmit Pulse Width [μs]	1, 0.5	RCU
Start and Stop Scan Angles [Deg.]	≤ 120	RCU
Range Gate Width [μs]	6	RCU
Ch.A, Ch.B, Index	Encoder	Spinner Unit
Output Signals:		
start_scan_position	≤ 16384	RCU
CAL_out	TTL	Rx switch
rx_switch	TTL	Rx switch
amp_sw, t/r_sw	TTL	Preamplifier Switches
DDSADD, DDSDATA	FTW,DFRRW,DFTW	DDS
WR, Fud, reset_dds	DDS Control	DDS
Gage_sampling	TTL	Gage Trigger

further divided by 8 [17] and input into the PRF creation block, 'prfckt' which computes the PRF by:

$$PRF = \frac{CLK}{N \times (N_P + 1)} = 1.25KHz \tag{3.7}$$

where CLK = 3.1MHz, N is a division factor to obtain higher or lower PRFs, and N_P is the number of pulses in T_P.

Once the PRF signal is formed, it is sent into a three input AND block to enable proper chirp pulsing of the DDS output signal, as shown in Figure 3.13. The three AND block inputs are: (1) PRF signal from module 'prfckt', (2) enable PRF signal, and (3) enable encoder signal. The PRF enable signal is a command sent by the RCU computer that is routed through a status register module inside the FPGA to inform other blocks when the radar is in operation. When in operation, the PRF enable signal switches from the ground state to the high state (vcc). Another vital input to the FPGA is the antenna position signal, which controls the antenna encoder.

The encoder is located in the spinner box. It is a quadrature encoder; thus, it has three sinusoidal outputs (A, B, and X) that are routed to the FPGA. Signals A and B track the location of the antenna. There exists a phase difference between both A and B which distinguishes the antenna rotation direction. The antenna, however, spins in only one direction and therefore the phase difference is not tracked by the FPGA. The index signal, X, resets the signals A and B after every full rotation. Once the encoder signals enter the FPGA program, they are directed into a decoder block, shown in Figure 3.14. The decoder module creates a counter that associates each rising edge of either signal A or B to a count, which is attributed to an angular position. This count is then transferred to a comparator that checks to see if the current antenna position is within the desired span. If true, then the encoder enabler signal is set to high (vcc) and the current angle is sent out of the FPGA and into a file on the RCU computer for better pairing with the gathered data set that is being recorded on the DAQ computer. If false, the enable signal stays in the low (ground) state and waits until the logic becomes true.

The radar system is required to operate with both stationary and rotational modes. The above paragraph describes the rotational mode case. If the system is to operate in the stationary mode, with the antenna spinner box turned off, the encoder's position signals cannot be sent to the FPGA. To supplement the FPGA requirement of knowing the location of the antenna in order to properly program the DDS board, the user has to first select the stationary scan mode on the configuration file located in the RCU computer. This informs the FPGA to obtain a position signal from a Function /Arbitrary Waveform Generator (HP 33120A, 15MHz). The input clock was set to a rate of 3.5KHz, which corresponds to the clock frequency of the encoder inputs A or B (an antenna rotation rate of 26rpm or 155.9 degrees/sec). This input is directed into a module that creates a counter, where each count corresponds to a theoretical angular position. The count is sent to the the same comparator logic blocks that were previously discussed to toggle the encoder enable signal.

Once all three signals are sent into the AND gate, the logic output is sent to the 'pulsegen', 'calmod', and 'rangegate' modules for the purpose of creating the radar switches' control signals. The 'pulsegen' module produces an output signal that is duplicated to cre-

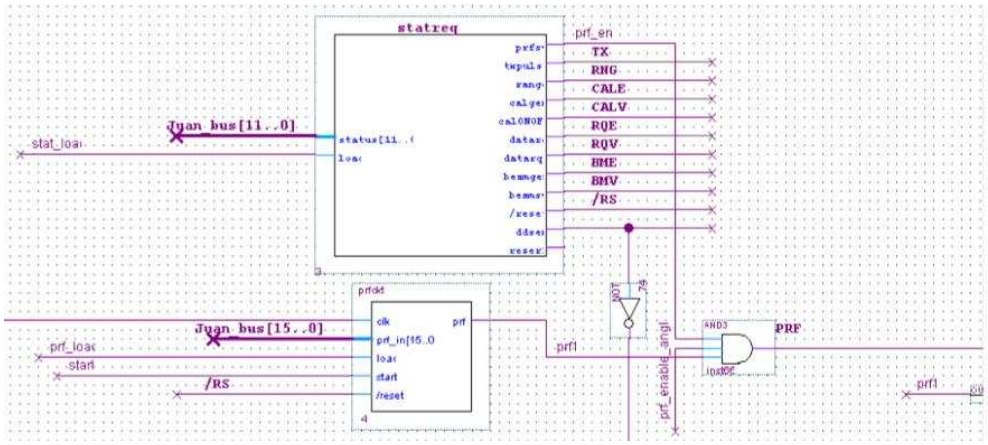

Figure 3.13. The PRF circuit which fed into a 3 input AND logic gate for enabling pulsing of the DDS chirp

ate the two control signals for both preamplifier switches. Since both switches are the same make and model, the switching times are equivalent and the timing signals must be exactly

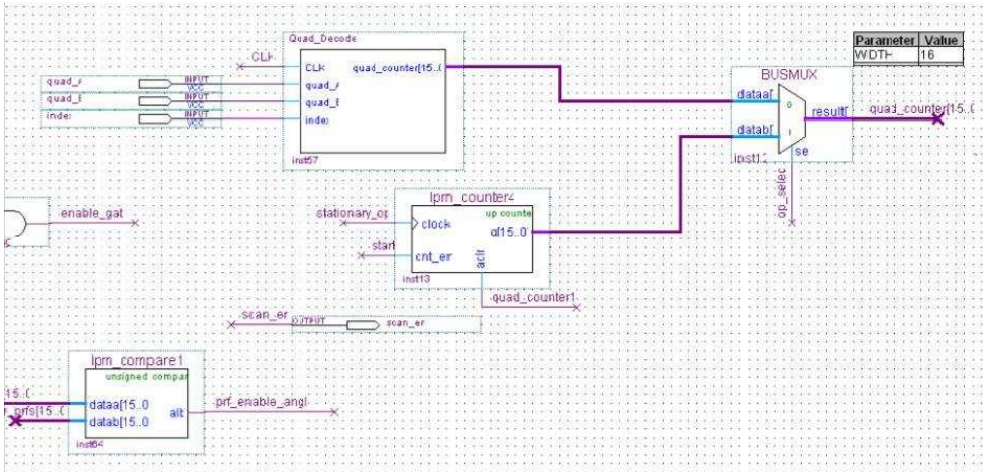

Figure 3.14. Quadrature decoder with encoder A, B, and X (index) inputs. Attached to the decoder is the stationary versus rotating mode option select.

the same. The control signal switches from ground to vcc, and vice versa, 0.1μs before and after the PRF pulse. This ensures that the transmit signal passing through the switches is not cut off. The 'calmod' module creates one of the receiver switch controls which samples the calibration path. This control signal samples the transmitted pulse every 0.8μs for assurance that the radar is working properly. The 'rangegate' module creates the second control signal for the receiver switch, which dictates how long the receiver will sample the backscattered power. It takes into account the PRT and the range gate delay that is required for proper separation of the FPGA circuit. The range gate delay is theoretically equal to the transmitted signal pulse width of 1μs, or 150m. In this radar, the value of 1.2μs, or 180m, is used due to the lack of a steep cliff and some clutter.

The FPGA also controls the DDS board, through parallel programming, by using the parameters passed to it from the RCU. This is achieved by using the 'ddsparam' and 'ddsrun' modules. Both modules receive the FPGA system clock as an input and base all programming and pulse enabling on it. When the radar is run (*trial.c* program is executed) the derived parameters for the DDS board are sent to the 'ddsparam' latch module. This module holds the DDS parameter values and waits for both the load signal to toggle high and a

rising clock edge to load the parameters into a temporary register. The parameters are then latched to an output register on the negative edge of the clock and sent into the 'ddsrun' module.

The 'ddsrun' module is a state machine that passes the desired parameter values to the DDS board and enables chirp pulsing capability. The trigger input is the PRF signal, enable input begins the process of the DDS board initialization, and the input clock is active on rising edges. Within this module, there are two case loops which use the 'wr' and 'fud' variables to properly program the parameters to their associated address location in the DDS. The first case loop stores the current address and parameter into two corresponding dummy variables, regadd[] and regdata[]. The address and associated parameter value are then stored into a temporary buffer when the variable 'wr' toggles high. The next step associates the next DDS address and parameter value to regadd[]/regdata[] and toggling the 'fud' variable high to write what is stored in the temporary register into the DDS memory. This loop continues until all chirp configuration parameters are written to their corresponding address location in the DDS board. The second case loop toggles the chirp on and off by modifying the CFR register within the DDS, as discussed in Section 3.3. The modification of the CFR register is accomplished by using the same method as in the first case loop (i.e.: assigning the address and parameter values to regadd[] and regdata[], respectively, and then toggling 'wr' and 'fud' to ultimately write the values into the DDS memory).

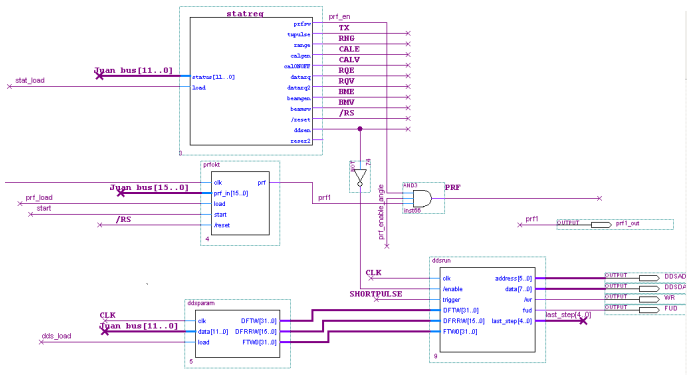

Figure 3.15. Two main modules, ddsparam (a latch) and ddsrun (a state machine), that control the DDS initializations and enable pulsing of the chirp signal.

CHAPTER 4

CONTROL AND DATA ACQUISITION SYSTEM

4.1 Data Acquisition Overview

The SSDMR uses a 14-bit A/D converter with a maximum simultaneous channel sampling frequency of 50MHz. This DAQ card captures the raw data and stores it to a file on the hard drive. A block diagram of the DAQ system is shown in Figure 4.1. A complete description of the A/D converter capabilities is described in [18, 19, 20]. The DAQ system provides the ability to save the raw data gathered by the radar to the hard drive of the computer for storage. Further signal postprocessing of the data is conducted to create the maps of ocean surface waves from the raw data. The I/Q channels are sampled by the DAQ. The data gathered by the A/D converter is transferred for direct storage, via a PCI slot, from the Gage buffer memory to a file on the hard drive.

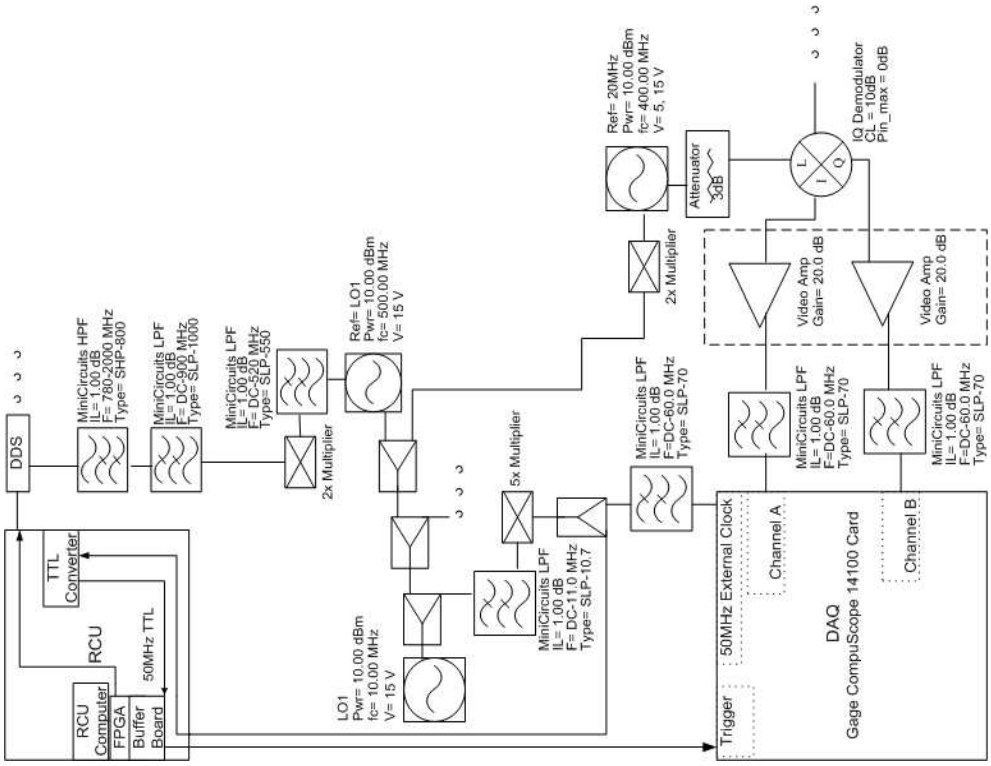

Figure 4.1. The block diagram of the RCU and DAQ systems.

An external trigger signal for the DAQ board is created by the FPGA. It informs the Gage board when to acquire samples. The DAQ card is clocked at 50MHz by an external clock input. A software program written in C was developed to initialize and control the Gage card while properly directing incoming data.

4.2 A/D Converter

The minimum and maximum input signals accepted by the A/D converter card are determined by the converter's dynamic range. As discussed in Section 2.4, the dynamic range is bounded by the maximum power that the A/D converter can allow and the minimum power sensitivity of the radar receiver. The Gage card has a noise level that is 15dB less than the receiver's in order to determine the receiver's minimum power sensitivity. The converter card's voltage range, dynamic range, are related to the noise level of the receiver

by:

$$N_{receiver} = -15dB + 6 \times N = 10log(\frac{V_{pp}^2}{8R}) = 69dBm. \quad (4.1)$$

Here $N_{receiver}$ is the radar receiver's noise level, N is the number of bites of the A/D converter, and V_{pp} is the maximum range of the A/D converter voltage.

A test was conducted to determine the noise level of the Gage A/D converter card. This was accomplished by attaching a 50Ω load to both channels A and B while still sending the external clock and trigger to the card. The measured noise level was -78dBm (2mV to -3mV, 5mV amplitude range), as seen in Figure 4.2. The processing code for this measurement did not use coherent averaging of 2 pulses, so it depicted the Gaussian noise associated with the Gage converter card. Similarly, another test was conducted to measure the full impact of the transmitter noise floor on the receiver. This test was conducted on September 26, 2006, when the I and Q channel outputs were measured with a Spectrum Analyzer (Agilent E4407B, ESA-E Series, 9kHz - 26.5GHz). The radar was fully powered, though no pulses were transmitted through the system. The preamplifier switches were both in the "off" position while the receiver switch was connected to the calibration loop path in order to sample the maximum effect of the transmitter noise on the receiver. The noise floor recorded was -115dBm/Hz (-43dBm for a bandwidth of 50MHz).

A second test was conducted to determine the noise level of the receiver as seen by the Gage A/D converter card. The radar receiver power was turned on and the I and Q channels were connected to the Gage A/D converter card to allow sampling of the noise level. During this process, no pulses were sent through the transmit and receive chain. The preamplifier switches were set to the "off" position while the receiver switch was connected to the calibration loop port. As seen in Figure 4.3, the noise level was found to be between -68 and -65dBm (37mV amplitude range). These results adhere to (4.1). This measurement was conducted using coherent averaging of two pulses, therefore it reduced Gaussian noise that was generated by both radar devices and the Gage converter card. For the purposes of

this radar, ± 1 V was the most suitable dynamic range for the converter card. This allows for an individual channel input power range of -68 dBm to $+6$ dBm.

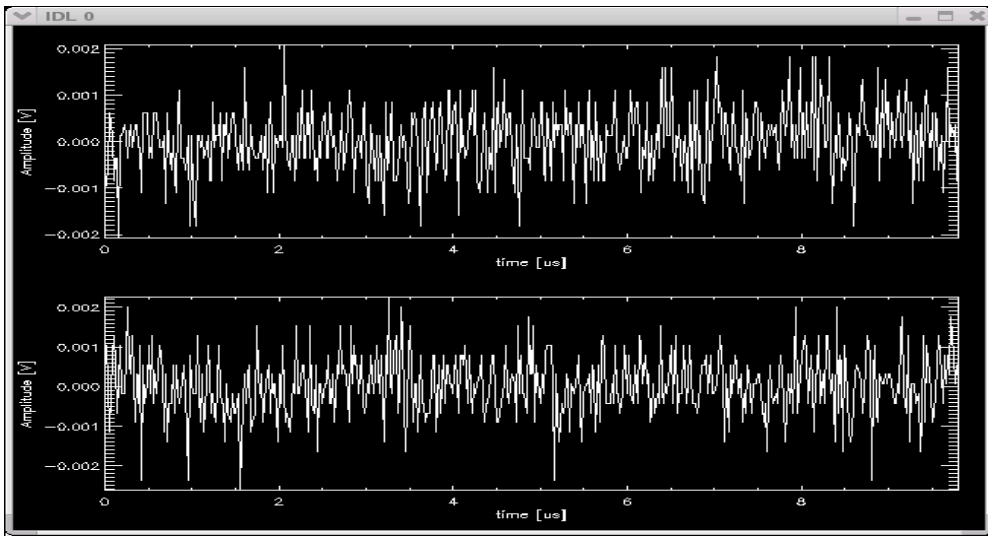

Figure 4.2. The measured noise of the Gage converter card. This was taken with the Gage converter card receiving the trigger and external clock inputs while having channels A and B terminated with 50Ω.

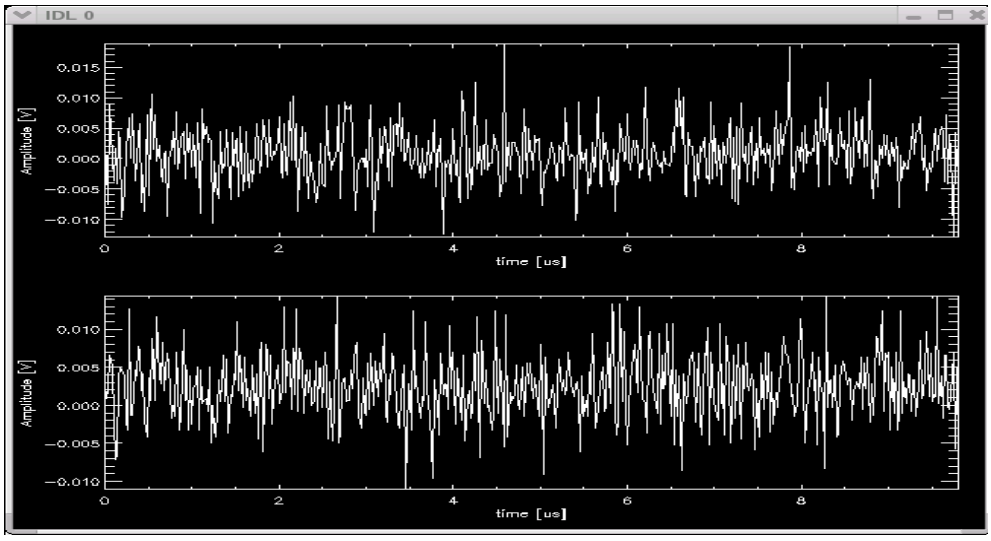

Figure 4.3. The measured noise of the radar system. The radar system was turned on, though no pulse was sent through the transmit/ receive paths, and the Gage converter card sampled the system noise through the I and Q channels.

4.3 A/D Converter Control and Pre-Processing

The DAQ system Gage card is initialized and controlled by a C software program. This program was derived from a skeleton code that was provided by Gage Applied, Inc. along with the Gage card. The code, titled *gage2hd.c*, was modified and split into two portions. The first portion initializes the Gage card with the modes shown in Table 4.1, then captures data from two profiles, each consisting of 256 bytes, from both input channels once the positive trigger slope is detected. The data is then stored in the gage card buffer. Once the buffer is filled, the second portion of the code is executed. This section first accesses a user-defined parameter file, located in the same folder as *gage2hd.c*. These parameters, shown in Table 4.2, are translated into data header structures and stored into a .dh file for direct access during postprocessing. The code then takes the data, located in the Gage card buffer queue, and conducts coherent averaging of 2 pulses on both channels. The averaged data is subsequently stored in a binary file located in "/mnt/data". The file naming convention used is YYYYMMDDTTTT.dat, which encompassed a 4 digit year, two digit month and day, as well as a 4 digit time using GMT in 24 hour format. The data inside the file is written as: profile number, time stamp, averaged data, channel A, profile number, time stamp, averaged data, and channel B. The program continues capturing the data, storing it in the Gage card buffer, averaging it, and routing it to the file until all scans are completed. For every 1^o that is scanned by the radar, 8 profiles are taken; this creates 4 sets of data to undergo averaging.

Table 4.1. DAQ A/D Converter Initializations

Parameter	Setting
External Clock / Sampling Rate [MHz]	50
Number of Bits [#]	14
Voltage Range [V_{pp}]	1
Input Impedance [Ω]	50
Record Mode	Multiple
Operational Mode	Dual Channel, DC Voltage
Trigger:	
Source	External
Slope	Positive
Sample Depth After Trigger [Bytes]	512
Voltage Range [V_{pp}]	5, AC Voltage

Table 4.2. Main Parameters and Values in the DAQ Configuration File

Parameter	Value
PRF [KHz]	1.25
Antenna Spinner [rpm]	26
Chirp Bandwidth [MHz]	50
Pulse Width [μs]	1, 0.5
Range Samples	512
Azimuth Coverage [Deg]	0$\leq$X$\leq$120
Azimuth Coverage Offset [Deg]	$0 < X < 240$
Horizontal Beamwidth [Deg]	0.9
Coherent Integration [# of pulses to average]	2

4.4 Client - Server Connection

The radar uses software in order to synchronize hardware components and enable communication between the user, embedded RCU computer, and the DAQ computer for proper data acquisition. Figure 4.4 displays a flow chart diagram of the overview of the server-client processes. First, to synchronize the radar hardware components, the user specifies parameters located in the 'marine_params.dh' configuration file. Table 4.3 displays the main parameters along with the typical values used during radar operation. Once the parameter values are set, the user has to change the associated parameters in the user-definable parameter file located on the DAQ computer, as discussed in Section 4.3. Sample parameter files are shown in Appendix A.

Table 4.3. Main Parameters and Values in the RCU Configuration File

Parameter	Value
PRF [KHz]	1.25
DDS Center Frequency [MHz]	400
Chirp Bandwidth [MHz]	50
Pulse Width [μs]	1, 0.5*
Range Gate Width [μs]	6
Start Scan Angle [Deg]	0$\leq$X$\leq$360
Stop Scan Angle [Deg]	$> X$
Calpulse PRF [Sample 1 Calibration Pulse After # of PRFs]	1000
Range Gate Delay [μs]	1.2

* Although having the capability to produce and process this pulse width, no experiments were carried out with it.

Once the parameters are defined, the radar connections are bridged. The inputs and outputs of all 3 radar rack mountable boxes, discussed in Chapter 3, must be connected according to the labels on each port. When all connections are made, the radar power box is switched ON such that all components have power and are ready for operation. The RCU computer also contains a software program titled *trial.c*, located in the same folder as *marine_params.dh*, which reads the parameter file. When all parameters are read, the required variables are calculated and passed to the FPGA registers, as discussed in Chapter 3.

Embedded in both the *gage2hd.c* and the *trial.c* programs is a server-client program that serves as the communication portal for both computers. The *trial.c* program acts as a server while the *gage2hd.c* acts as a client. Once the *trial.c* program is executed, it suspends running until the *gage2hd.c* program is executed and a request is received by the server. Once the request is sent, the *trial.c* program will synchronize the time and date of the DAQ computer with that of the RCU computer. Next, the starting angle of the scan and subsequent angular positions are stored in a file located in the RCU computer along with their correlated time stamps (in seconds and microseconds). When all scans are finished, and the angular positions and time stamps are acquired, the file is closed and sent to the DAQ computer for later processing. Then the *gage2hd.c* program will end, closing the client program. The *trial.c* program will continue to run and wait for more requests sent by the DAQ computer via another execution of the *gage2hd.c* program. The *trial.c* program will run in a continuous loop until the program is manually ended by the user pressing the <enter> key. The program is only ended if the radar's scan parameters need to be altered or the experiment is complete. This enables the radar to continue running the hardware without resetting between scans, assuming that consecutive scans utilize the same radar parameters.

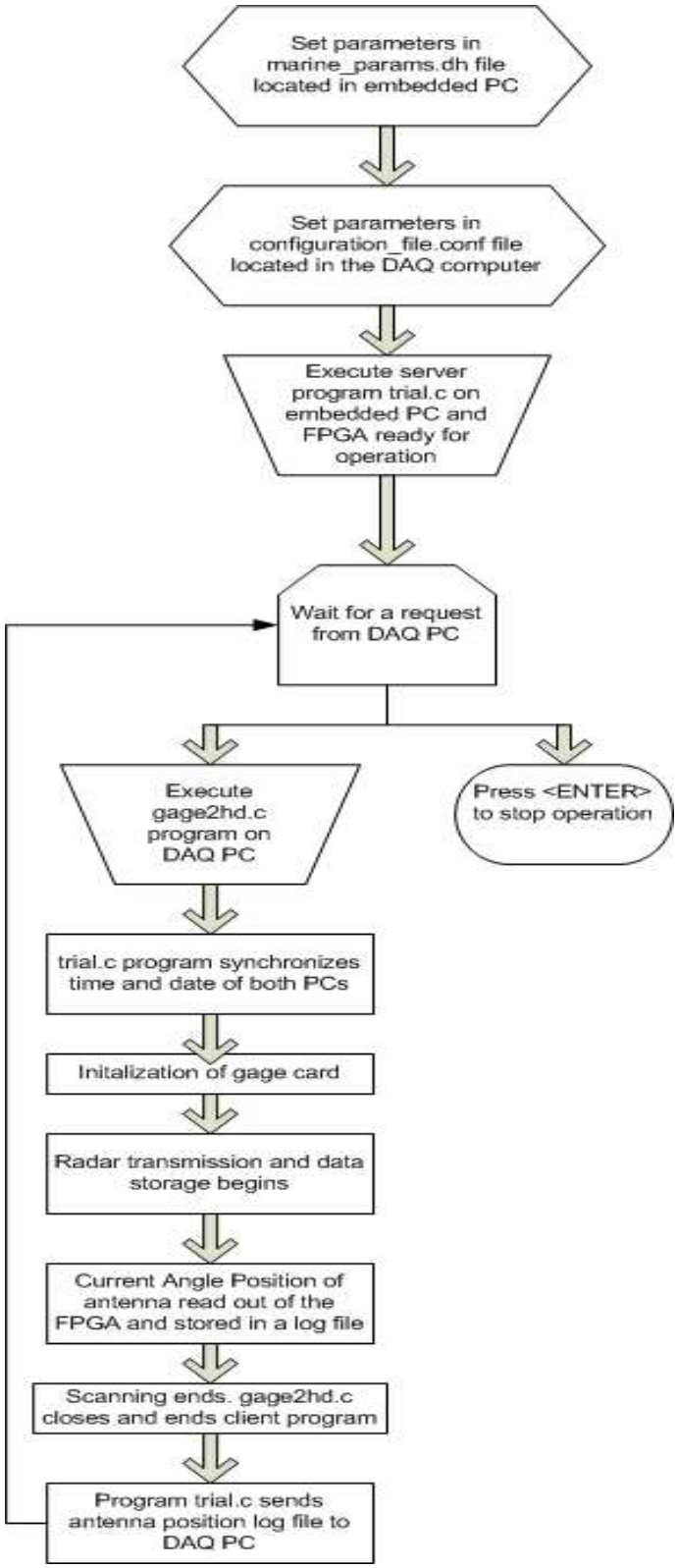

Figure 4.4. A flow chart that describes the order of program execution with respect to the server-client connection.

CHAPTER 5

FIELD TESTING AND CONCLUSIONS

To validate the capability of SSDMR, two experiments were conducted. First, the radar was taken to the airport for initial testing in Northampton, Massachusetts. The second experiment took place in Milford, Connecticut. This location was chosen because it provided a clear look at the nearshore zone and an interesting underwater topography.

5.1 Northampton, MA Airport Testing

The airport at Northampton, MA was chosen for calibration because it provided a long, open space where calibration could be conducted while using stationary and normal operation modes. An X-band corner reflector was used for calibration purposes. It was placed approximately 300 meters away from the radar location, as illustrated in Figure 5.1. Stationary mode was used to ensure that the radar calibration was conducted correctly. The I and Q outputs were disconnected from the DAQ Gage card and attached directly to an oscilloscope (HP 54602A, 150MHz, 4 Channel), as shown in Figure 5.2. This configuration allowed manual rotation of the antenna during operation while instantaneously viewing the I and Q output signals.

When a direct line of sight between the antenna and corner reflector was established, both I and Q data channels showed maximum signal levels. Once the correct antenna position was found, the I and Q channels were reconnected to the Gage converter card and a data set was taken. The recorded data set shows a pulse reflected from the corner reflector, as shown in Figure 5.3. The distance between the corner reflector and the radar was calculated from the received signal. The determined distance was 330 meters. Special

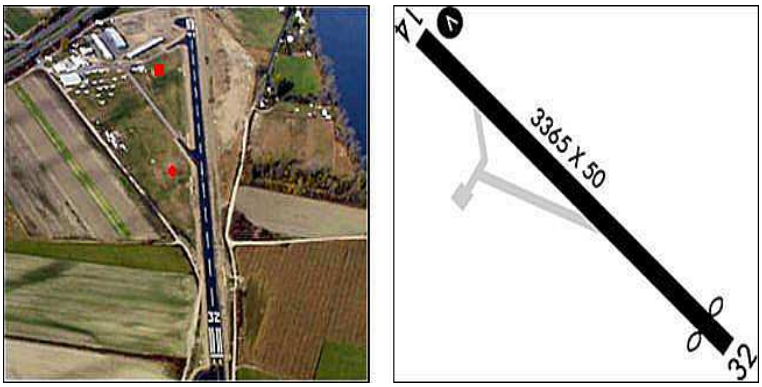

Figure 5.1. The distance of the X-band corner reflector calculated to be approximately 330m. The red square depicts the location of SSDMR while the red circle depicts the location of the X-band corner reflector. [1]

Figure 5.2. The equipment used to aid in the detection of the X-band corner reflector during operation.

care has been taken to position the corner reflector away from bushes and trees in order to avoid high returns from ground clutter. The noise floor data from the lab experiments was used to normalize the acquired data in order to more accurately display and interpret the signals.

The normalized SNR plot for this data set is shown in Figure 5.4. The average noise floor is -52.89dB. The noise floor level was determined from the portions of the data with-

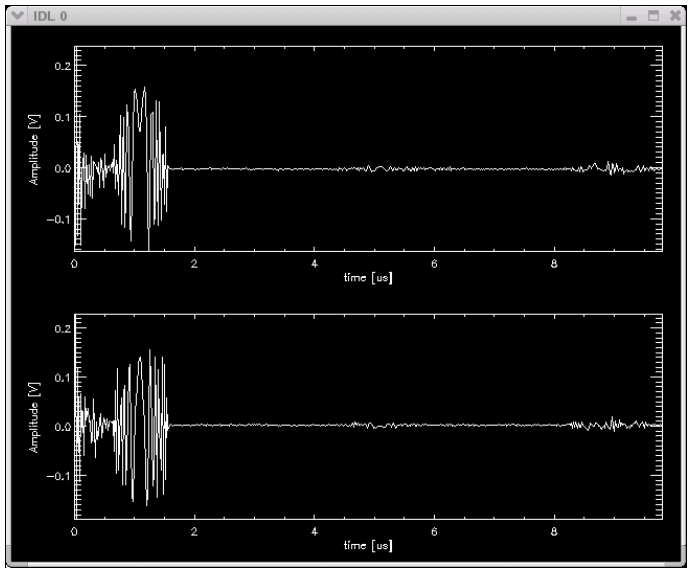

Figure 5.3. I and Q data received during calibration at the Northampton, MA experiment.

out any targets echoes, which for this data set occurred occurred between the 200 to 215μs time markers. The noise floor level is approximately 12dB higher than its original expected value. The physical configuration of the deployment location (flat piece of land) did not allow a minimum of 10m height difference between the radar and the X-band corner reflector; therefore, the additional noise can be attributed to an increase in the amount of sidelobe clutter. The surrounding environment could also have contributed to the higher noise floor. The return from the X-band corner reflector is visible as the signal located within the first 100 samples.

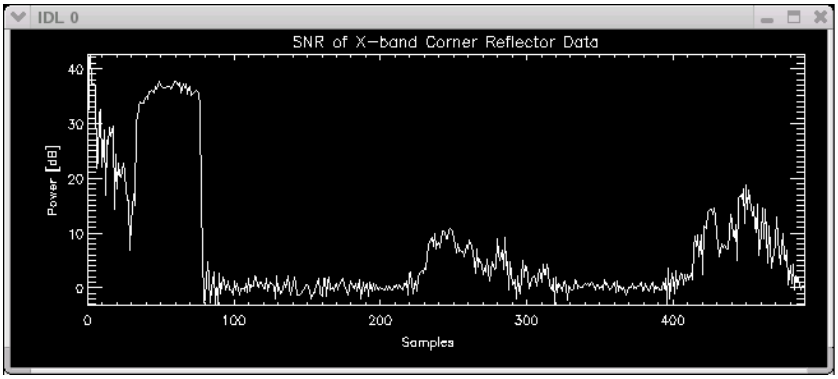

Figure 5.4. The SNR for the Calibration Experiment. The averaged noise floor was found to be -52.98dB.

5.2 Observations

Once confidence in the radar's capability to detect ocean surface waves and their velocities was achieved, the radar was taken to Milford, CT. This test site provided a clear look at the nearshore zone, as shown in Figure 5.5. This location could not provide a cliff from which to operate the radar. Therefore, the height of the radar, 2m, was due solely to the radar mount on the truck bed. A cliff would have been more suitable for the experiment, in order to avoid the influence of the clutter.

The data gathered and processed at this location on September 20, 2006 is shown in Figure 5.7. During postprocessing, a pulse compression was applied to the data set. Pulse compression filter coefficients were generated from the 1μs chirp that was recorded during the calibration experiment at the airport in Northampton, MA. A plot of the compressed data is shown in Figure 5.6. The compressed chirp can be seen between samples 0 and 25. For this data set, the wind was directed WNW with a maximum specified speed of 7m/s, which was greater than the minimum wind speed necessary for acquiring the acceptable data set [21]. In the data, a boat can be seen at the coordinates (-.28,0.550). Waves can be seen from 150m to 250m away from the radar. Two more boats can also be seen located approximately 344m and 604m, respectively, from the radar.

Figure 5.5. Radar deployment set-up at Silver Sands Beach located in Milford, CT on September 20, 2006.

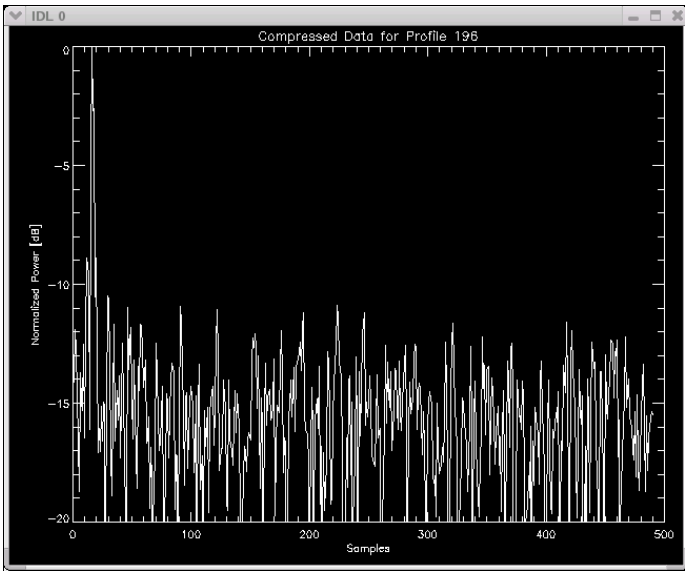

Figure 5.6. The data profile 196 after pulse compression has been applied. The chirp can be seen between samples 0 to 25.

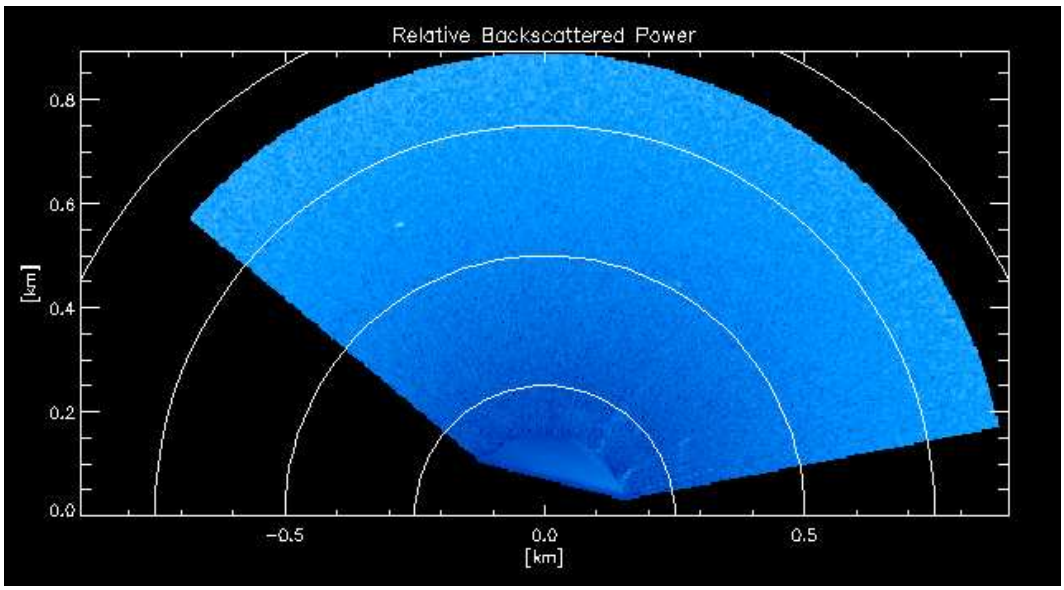

Figure 5.7. The processed data taken by the SSMDR. This data set was taken on September 20, 2006 at Silver Sands Beach.

5.3 Summary and Conclusions

The X-band Solid State Doppler Marine Radar was built in the Microwave Remote Sensing Lab during 2005 to 2006. The radar is designed to monitor ocean waves and their velocities, preferably from an elevated location (i.e.: a cliff). The design process began by considering the theoretical constraints that would drive the system requirements. In this thesis the various subsystems of the radar were described: RF, IF, Radar Control Unit, and Data Acquisition. The performance of the radar has been demonstrated by two main experiments carried out in Autumn 2006 at the Northampton Airport (Massachusetts) and the Silver Sands beach, Milford, CT. The results from both experiments have verified that the radar is capable of detecting ocean waves and their corresponding velocities.

APPENDIX A

SAMPLE PARAMETER FILES

There are two parameter files, one located on the embedded RCU computer and the other on the DAQ computer. Prior to the execution of both *trial.c* and *gage2hd.c*, these parameter files must be checked to ensure that the values are as desired, modifying the parameters to desired value if needed, and then saved. Sample parameter files are shown in Tables A.1 and A.2. The values displayed for each parameter were utilized in experiments conducted at the Northampton Airport in Northampton, Massachusetts and the beaches in Milford, Connecticut.

Table A.1. Sample RCU Parameter File: marine_params.dh

Parameter	Value
Date and time of the file =	Mon Aug 15 12 : 13 : 53 2005
PRF (kHz) =	1.25
FPGA clock frequency (MHz) =	25
Sampling frequency(MHz) =	50
DDS center frequency (MHz) =	400
Chirp bandwidth (MHz) =	50
Pulsewidth (us) =	1.0
Extra pulse width (us) =	0.1
Number of range samples=	512
First range gate (m) =	0
Range gate delay (us) =	1.2
Range gate width(us) =	6
Calpulse delay (us) =	0.1
Calpulse width (us) =	1.0
Calpulse PRF =	1000
Range resolution (m) =	3.0
Start Scan Angle(deg) =	30
Stop Scan Angle (deg) =	195
Accumulation =	1

Table A.2. Sample DAQ Parameter File: configuration_file.dh

Data file directory :	/mnt/data
RPM :	26.0
PRF :	1.25 kHz
Coherent integration :	2
Pulse pair averages:	0 $(+)$
Azimuth coverage :	120.0 degrees
Azimuth coverage offset :	20.0 degrees
Beamwidth:	0.9 degrees
Pulse width :	1.0 us
Rx switch time:	15 ns
Sampling frequency :	50 MHz $(*)$
Number of scans:	150
Range samples :	512
Processing:	0 ($\hat{}$)

$(+)$ *Number of pairs to average*

(*) fixed, not adjustable at this time, because of hardware filter on signal coditioning board.

($\hat{}$) *0 - raw data mode, 1 - processed data mode*

APPENDIX B

POWER SUPPLY AND TEMPERATURE CONTROL

The SSDMR's rack-mountable power box generates the required voltages for all devices and/or subsystems of the radar. It houses both AC/DC converters as well as converter boards for proper voltage and current distribution. Table B.1 displays the different power converters and their correlating measured voltages at the destination point. The inputs to all converter boards are derived from the AC/DC converters. The main DC/DC converter board, Acopian, has the capability to reduce the voltage ripple by $1.5mV_{RMS}$.

Table B.1. Power Supply

Voltage Generated [V]	Voltage Measured [V]	Destination
Vicor FLAT PAK:		
15	14.61	Transceiver Box
15	14.98	Spinner Box
Vicor Mini MEGAPAK:		
12	11.53	RCU computer
Acopian Boards:		
5	4.53, 4.76, 4.7	Transceiver, RCU, and Spinner Box
15	14.61	RCU Box
-5	-4.95	RCU Box
3.3	3.02	RCU Box
Student Boards:		
-15	-15.01	Transceiver Box
-12	-12.46	Transceiver Box

All electronic equipment characteristics drift depending on the operating temperature. For example, amplifiers tend to change their gain characteristics depending upon the ambient temperature. The SSPA has an extremely high gain, thus, a large heat sink has been attached to it to aid the dissipation of heat. To aid with cooling, all operating devices are

located in the transceiver box such that the heat dissipation from the SSPA does not cause other devices to drift. Fans are also used to help with air flow circulation, and a temperature detector is connected to the side of the SSPA. The detector is routed out of the transceiver box and into the power box for display. This device is mainly used as a general reading of the amplifier temperature due to an inability to calibrate the temperature gauge.

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