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Optical Lithography Simulation using Wavelet Transform

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OPTICAL LITHOGRAPHY SIMULATION USING WAVELET TRANSFORM

A Thesis Presented

by

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ABSTRACT

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MAY 2010

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Optical lithography is an indispensible step in the process flow of Design for Manufacturability (DFM). Optical lithography simulation is a compute intensive task and simulation performance, or lack thereof can be a determining factor in time to market. Thus, the efficiency of lithography simulation is of paramount importance. Coherent decomposition is a popular simulation technique for aerial imaging simulation. In this thesis, we propose an approximate simulation technique based on the 2D wavelet transform and use a number of optimization methods to further improve polygon edge detection. Results show that the proposed method suffers from an average error of less than 6% when compared with the coherent decomposition method. The benefits of the proposed method are (i) $>$ 20X increase in performance and more importantly (ii) it allows very large circuits to be simulated while some commercial tools are severely capacity limited and cannot even simulate a circuit as small as ISCAS-85 benchmark C17. Approximate simulation is quite attractive for layout optimization where it may be used in a loop and may even be acceptable for final layout verification.

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CHAPTER 1

INTRODUCTION

Optical lithography is the process that involves the transfer of features from a mask onto a silicon wafer. During the process light is shone onto the mask pattern which makes an imprint on the resist that lies over the silicon wafer, on the image plane. The proper functioning of the circuit on the mask depends on the fidelity of the transfer of this pattern from the mask to the silicon wafer.

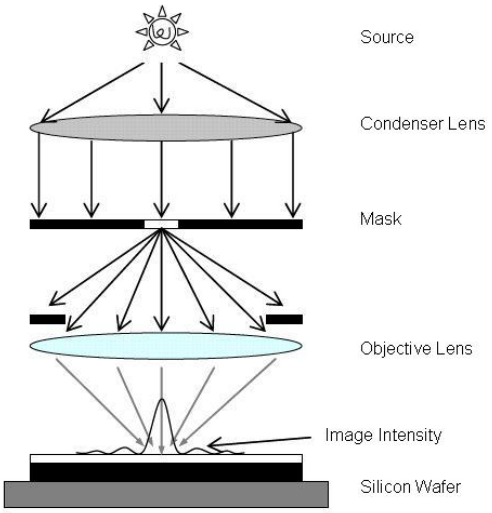

Figure 1.1. A typical lithography system

In the general lithography system as depicted in the figure 1.1 above, light from the light source passes through the condenser lens, then falls on the mask which is transparent but for the regions where the features are supposed to be. The light after passing through the mask is captured by the objective lens and then is incident onto

the resist coated silicon wafer. Depending on the chemical nature of the resist, positive or negative the incident light produces chemical changes in the exposed sections which is then etched by an acid. As a result the features on the mask are transfered to the silicon wafer.

Technology scaling in semiconductor industry is mainly driven by corresponding improvements in optical lithography technology. Lately, improvements in optical technology have been difficult and slow. Figure 1.2 shows the dawn of the sub-wavelength regime since the 0.35 micron technology . The transition to deep ultra-violet (DUV) light source (193nm) required changes in lens materials, mask blanks, light source and photoresist. Consequently, as the industry moves towards manufacturing end-of-the-roadmap CMOS devices, lithography is still based on 193nm light source to print critical dimensions of 65nm, 45nm and likely 32nm. In sub-wavelength lithography,

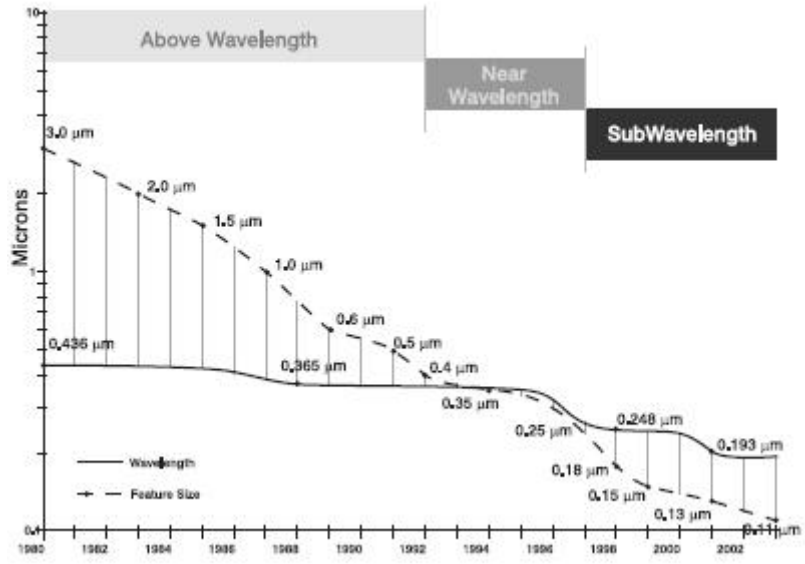

Figure 1.2. Shift to sub-wavelength lithography since the 0.35 micron technology [12]

interference and diffraction results in a corrupt pattern transfer, where proximity of other features around the feature being printed poses printability issues [12]. While

the interference effect is a function of the mask design, the diffraction effect has arised due to the ever decreasing size of features on the mask. When the smallest feature on the mask has size close to half the wavelength of light in use things get bad. The wavelength of light used for the lithography systems these days is 193nm, and with the technology nodes like the 65nm, 45nm and 32nm diffraction is bound to happen. The one way to go around this problem is the use of light sources with a smaller wavelength, but as mentioned earlier advances in light source technology have not matched those in technology scaling and as a result the 193nm light source remains the technology of choice in the near future. As a remedy to the problems posed by sub-wavelength lithography, RET's (Resolution Enhancement Techniques) are used to improve the situation. Some of the techniques available are:

- OPC (Optical Proximity Correction)
- PSM (Phase Shift Masking)
- Off Axis Illumination
- Use light of shorter Wavelength

We explain the need of a fast lithography simulator using the example of OPC. The figures have been taken from the PhD dissertation of Nick Cobb [6]. From figure 1.3 it can be seen that OPC significantly improves transfer fidelity. Also the flow of the OPC algorithm is shown in figure 1.4 where it can be seen that OPC requires a number of lithography simulations as pertubations are added to the mask in an effort to find an optimum design. The need of a fast lithography simulator cannot be stressed enough. Optical lithography simulation is used to predict distortions such that they can be corrected during design. Unfortunately, litho simulation is notoriously slow. In this thesis we explore an approximate simulation technique based on 2D wavelet transform, with the ultimate goal of improving performance and capacity of optical

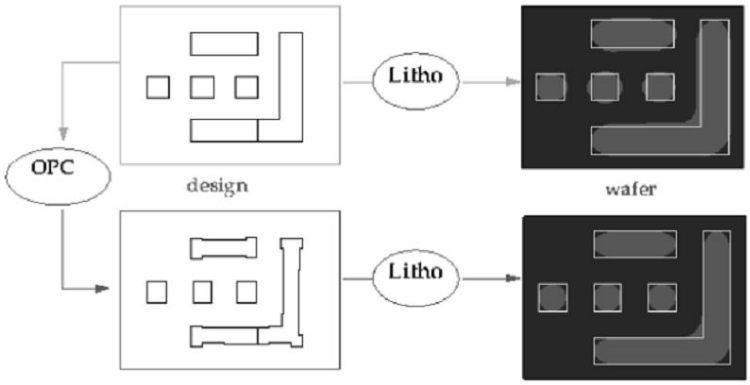

Figure 1.3. Optical proximity correction example [6]

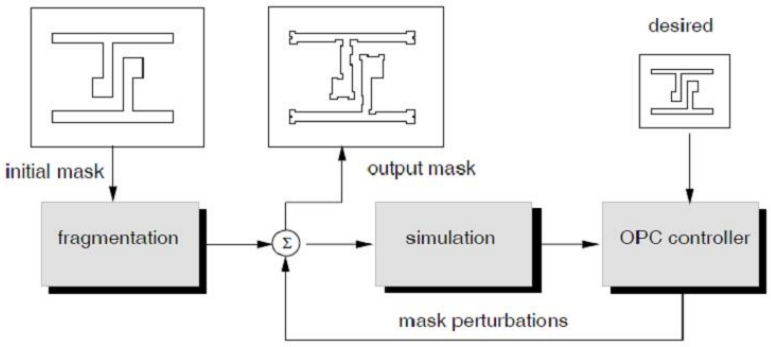

Figure 1.4. The flow of the OPC algorithm [6]

simulation. The method involves the use of a wavelet, the parameters of which are functions of the imaging system. Studies on benchmark circuits show that this approximate model achieves results within 6% of commercial tools, while significantly increasing the capacity and performance of simulation. Commercial litho simulation tools have difficulty simulating layout of entire benchmark circuits, which the approximate technique handles with ease. This method can eastical Proximity Correction (OPC), Design Rule Check (DRC) and other algorithms that involve circuit printability analysis.

CHAPTER 2

BACKGROUND

2.1 Aerial Image Formation Basics

2.1.1 Huygens Principle

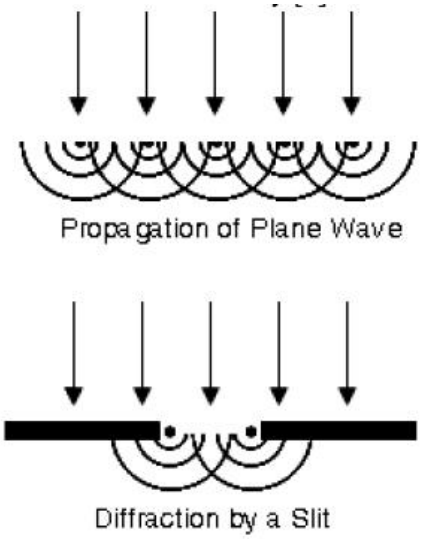

Figure 2.1. Diffraction by a slit

Consider figure 2.1 shown above which describes Huygens principle. Huygen found that any wavefront can be considered as made up of a number of radiating sources [17]. The intensity at any point in space can then be calculated by superimposing the effect of each of these point sources. What is seen here is that basically as light passes through a small aperture, a bending of light is observed termed as diffraction. As a result if light is shone on a mask having a small aperture (sections of the mask supposed to let light through in our case), the intensity profile seen at a screen (resist) does not completely lie within the extremeties of the aperture, but it spreads.

2.1.2 Fraunhofer Diffraction Integral

The Fraunhofer diffraction region is defined as the region where $z \gg \frac{\pi w^2}{\lambda}$, where z is the distance of the aperture from the screen, w is the width of the slit and λ is the wavelength of light. Optical lithography happens in this region. In the example considered in the previous section, the mask had a section that let the light through which is made of glass and the rest of it was opaque, covered by chrome. Let $t_m(x, y)$ be the mask transmittance function defined as given below in equation 2.1

$$t_m(x,y) = \begin{cases} 0 & \text{feature present} \\ 1 & \text{otherwise} \end{cases} \tag{2.1}$$

Let E_i be the electric field incident on the mask , (x', y') be the diffraction plane (i.e.

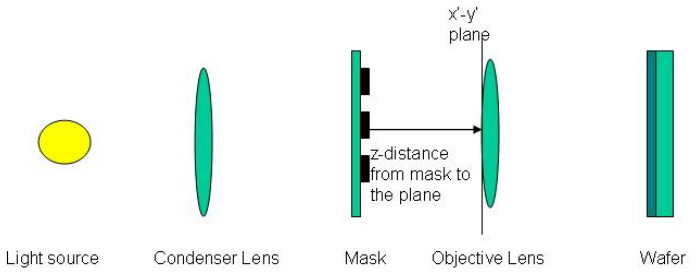

Figure 2.2. Figure explaining the Fraunhofer integral.

the entrance to the objective lens), z be the distance of the mask to the diffraction plane, λ be the wavelength of light used, n be the refractive index of the medium the entire system resides in. Also defining spatial frequencis of the diffraction pattern as scaled coordinates in the (x', y') plane defined as $f_x = \frac{nx'}{z\lambda}, f_y = \frac{ny'}{z\lambda}$, then the electric field of the diffraction pattern is given by 2.2 as described in [17]. The entire mathematics regarding the optics involved in optical lithography has been taken from [17]. For additional details please refer to it.

$$T_m(f_x, f_y) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} E_i(x,y) t_m(x,y) e^{-2\pi i(f_x x + f_y y)} dx dy \tag{2.2}$$

From the equation above it can be seen that the diffraction pattern is the Fourier transform of the mask pattern transmittance.

Let $P(f_x, f_y)$ be the objective lens pupil function, which is the transmittance of the lens from entrance to exit pupil.

$$P(f_x, f_y) = \begin{cases} 1 & \text{if } \sqrt{{f_x}^2 + {f_y}^2} < NA/\lambda \\ 0 & \text{otherwise} \end{cases} \tag{2.3}$$

In effect the product of the pupil function with the diffraction pattern is the light that passes out of the objective lens pupil. Using this and equation 2.2, we have the electric field $E(x, y)$ given by

$$E(x, y) = F^{-1}(T_m(f_x, f_y)P(f_x, f_y)) \tag{2.4}$$

which is the inverse Fourier transform. The aerial image is the intensity distribution at the silicon wafer plane and is the square of the magnitude of the electic field defined above in equation 2.4. So in summary, a fourier transform takes place at the end of the mask closer to the objective lens and an inverse fourier transform at the objective lens.

2.1.3 Partial Coherence

The equations for the electric field of the light at the resist of the mask considered so far were formed using light coming from one direction, termed as coherent light. However, this is not the case in a real lithography system. Consider the quasar light source from the figure 2.3 in which there are 4 sections from which light is incident on the mask. Here light arrives at the mask from various angles giving rise to a partially coherent imaging system. Consider the example in figure 2.4 where it can be seen that in a partially coherent imaging system, the diffraction pattern is spread

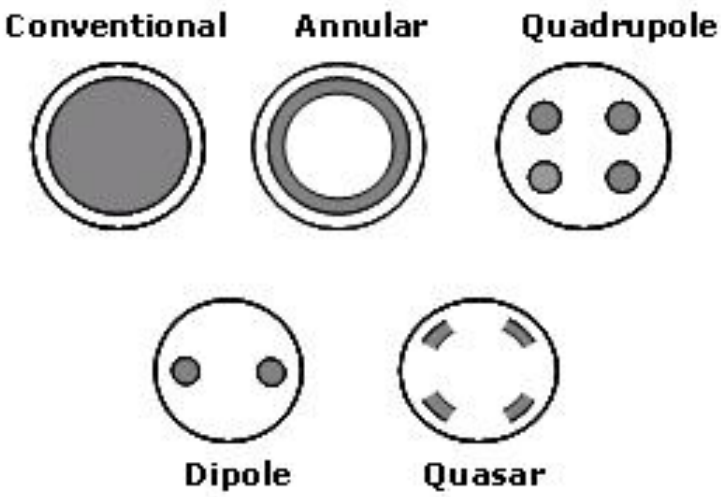

Figure 2.3. Various light sources used in an optical lithography system.

in space as compared to that of a coherent system. As a result of this the electric field equation from 2.4 undergoes a shift. Let f'_x and f'_y be spacial the shift in the diffraction pattern due to the partially coherent imaging system. As a result the new equation for the electric field of light at the resist plane is given by:

$$E(x, y, f'_x, f'_y) = F^{-1}(T_m(f_x - f'_x, f_y - f'_y)P(f_x, f_y)) \tag{2.5}$$

One way to characterize the various angles of light incident on the mask is by the

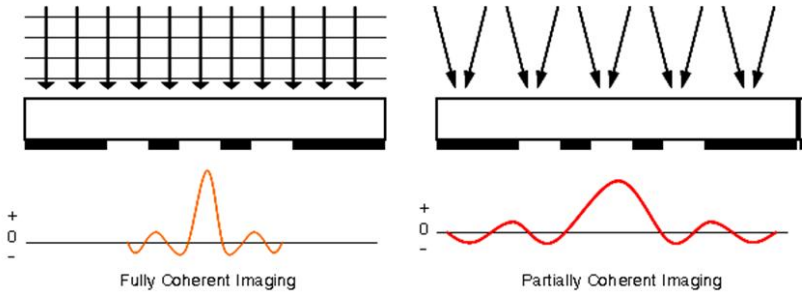

Figure 2.4. Fully and partially coherent imaging.

partial coherence factor σ defined as in equation 2.6.

$$\sigma = \frac{nsin(\theta_{max})}{NA} = \frac{\text{Source diameter}}{\text{Lens diameter}} \tag{2.6}$$

Here θ_{max} is the maximum angle of light coming from the source that is captured by the lens. So in order to find the complete aerial image, we find the the image intensity at the resist for each point source and then integrate it over the source which is know as the Abbe method of partially coherent image calculation. Defining the source as $S(f'_x, f'_y)$ the total intensity of the image is given by equation 2.7.

$$I_{total}(x, y) = \frac{\int\int I(x, y, f'_x, f'_y) S(f'_x, f'_y) df'_x df'_y}{\int\int S(f'_x, f'_y) df'_x df'_y} \tag{2.7}$$

. Further writing $\sigma_x = \frac{f_x \lambda}{NA}and\sigma_y = \frac{f_y \lambda}{NA}$ and normalizing the source shape as in equation 2.8.

$$S'(\sigma'_x, \sigma'_y) = \frac{S(\sigma'_x, \sigma'_y)}{\int\int S(\sigma'_x, \sigma'_y) d\sigma'_x d\sigma'_y} \tag{2.8}$$

Hence equation 2.7 takes the form as in equation 2.9.

$$I_{total}(x, y) = \int\int I(x, y, \sigma'_x, \sigma'_y) S'(\sigma'_x, \sigma'_y) d\sigma'_x d\sigma'_y \tag{2.9}$$

2.1.4 Hopkins Approach to Partial Coherence

Consider the one dimentional case for equation 2.5 with a change of variables.

$$E(x, f'_x) = \int P(f_x + f'_x) T_m(f_x) e^{2\pi i (f_x + f'_x)x} df_x \tag{2.10}$$

Calculating the image intensity is equalivalent to multiplying equation 2.10 with its complex congugate

$$
\begin{aligned}
I(x, f'_x) &= E(x, f'_x)E^*(x, f'_x) \\
&= (\int P(f_x + f'_x)T_m(f_x)e^{2\pi i(f_x+f'_x)x}df_x) \times \\
&\quad (\int P^*(f''_x + f'_x)T^*_m(f''_x)e^{2\pi i(f''_x+f'_x)x}df''_x) \\
&= \int\int P(f_x + f'_x)P^*(f''_x + f'_x)T_m(f_x)T^*_m(f''_x)e^{2\pi i(f_x-f''_x)x}df_x df''_x \quad (2.11)
\end{aligned}
$$

The image intensity is obtained as explained earlier by integrating over the source. In the Hopkins method, the order of integration is changed and integration over the source is done before carrying out the inverse Fourier integrals. The pupil function is a function of the source and integration over the source gives an intermediate equation as described in 2.12.

$$
TCC(f_x, f''_x) = \int P(f_x + f'_x)P^*(f''_x + f'_x)S''(f'_x)df'_x \quad (2.12)
$$

Hence we have

$$
I_{total}(x) = \int\int TCC(f_x, f''_x)T_m(f_x)T^*(f''_x)e^{2\pi i(f_x-f''_x)x}df_x df''_x \quad (2.13)
$$

The major addvantage of the intermediate variable is that it is completely independent of the mask function and hence can be precomputed and stored thus reducing much of the computational effort during lithography simulation.

2.1.5 Sum of Coherent Sources Approach (SOCS)

The (SOCS) approach is an approximate solution to the Hopkins equation and provides even fater runtimes than the storage technique described for the TCC. Defining $W(a)$ as in equation 2.14.

$$
W(a, b) = J_0(a - b)h(a)h^*(a) \quad (2.14)
$$

Where $J_0(x)$ is the fourier transform of the normalized source shape and $h(x)$ is the fourier transform of pupil function. Using the Hopkins integral in the spatial domain, we have

$$I(x) = \int\int W(x - x', x - x''')t_m(x')t_m^*(x''')dx'dx''' \tag{2.15}$$

Also let $W(a, b)$ be decomposed as a weighted sum of its eigen vectors ϕ_n

$$W(a, b) = \sum_{n=1}^{\infty} \lambda_n \phi_n(a)\phi_n^*(b) \tag{2.16}$$

Where λ_n is the eigen value for the eigenvector ϕ_n Using equation 2.16 we finally have

$$I(x) = \sum_{n=1}^{\infty} \lambda_n |\phi_n(x) \otimes t_m(x)|^2 \tag{2.17}$$

hence it can be seen that the final image is the sum of the convolution of each eigen vector with the mask transmittance function. The major use of this method is by limiting the use of the eigen vectors to some number N such that by considering these eigen vectors a reasonable accuracy can be achieved and reducing computation time considerably. This is the method of choice used so far in lithography simulators and in the next section we take a look at the overview of many such systems employing the SOCS approach for lithography simulation.

2.2 Previous Work

Optical lithography simulation involves the process of obtaining the intensity of electromagnetic waves that have propagated from the light source, diffracted through the mask patterns and projected onto the wafer. Using electromagnetic equations directly in conjunction with finite difference or finite element method [25] is costly in terms of computation time. Originally proposed by [10], the decomposition of Hopkins partially coherent equations and edge lookup for convolution was used by

Nick Cobb in his PhD thesis [6] to speed up aerial image simulation. Similar work was done by Mitra, Yu and Pan [19], in which edge lookup and decomposition of polygons in the mask into upper right corner rectangles was used to enable speedup in simulation.

In [27] and [29], the authors simplify the Optical Coherent Approximation (OCA's) [21], using the symmetric properties of the lithography imaging system. In [26], the authors show that the major source of error in generating the Transmission Cross Coefficients (TCC) is due to discontinuous boundaries of the TCC integrand. They report the use of improved numerical algorithms to dramatically improve speed and accuracy of simulation. In [20], Pati, Ghazanfarian and Pease use the incoherent sum of coherent imaging systems introduced by authors of [21], and further enhance simulation time by decomposing every mask into a set of commonly appearing shapes in IC's and then performing simulations based on the pre computations of those shapes.

Hardware based acceleration techniques have also been investigated [7] and used in commercially available lithography simulation products showing a considerable speedup over using a single CPU for the simulation. Our method is different from the TCC based methods in which we use wavelet transform to approximate the aerial image intensity and hence predict polygon edges post optical lithography.

CHAPTER 3

ON WAVELET TRANSFORM

3.1 Introduction to Wavelet Transform

Wavelet Transform is a method similar to the Fourier transform in which a convolution is performed on a signal to convert it into something that is easier to analyze [2]. It is a well known technique in image processing to achieve compression of data, data frequency analysis etc. It involves the correlation of a signal (1D Transform) or an image (2D Transform) with a wavelet.

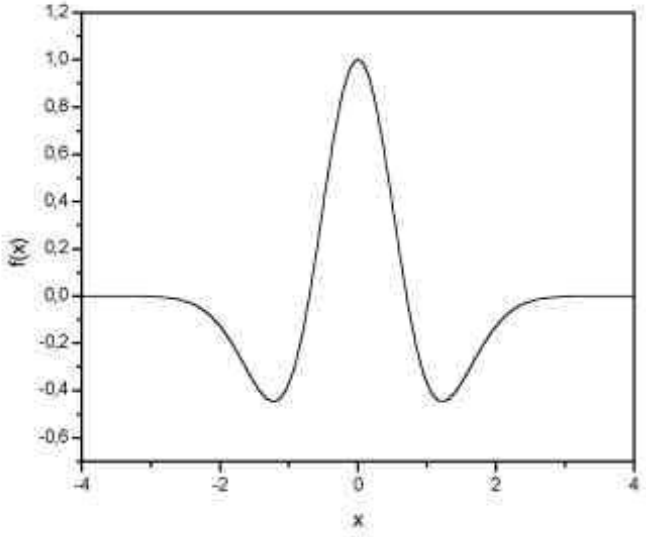

Figure 3.1. Mexican hat wavelet

A wavelet is a wave like function that is time limited. The Mexican hat wavelet is an example of such a wavelet as shown in 3.1. The equation for wavelet transform

is given in 3.1. Here $x(t)$ is the mask function and $\psi(t)$ represents the wavelet used for the transformation.

$$T(a,b) = w(a) \int_{-\infty}^{\infty} x(t)\psi^* \left(\frac{t-b}{a} \right) dt \tag{3.1}$$

Here a and b are called the scaling and translational parameters of the transform. They are used to calculate the transform at various locations of the signal b, and at various scales of wavelet a. $T(a,b)$ is the transform value or coefficient at a scale of a, location of b. $w(a)$ is called the weighing function used to ensure that the energy of the wavelet at every scale is constant [2]. Figure 3.2 illustrates the process of 1D

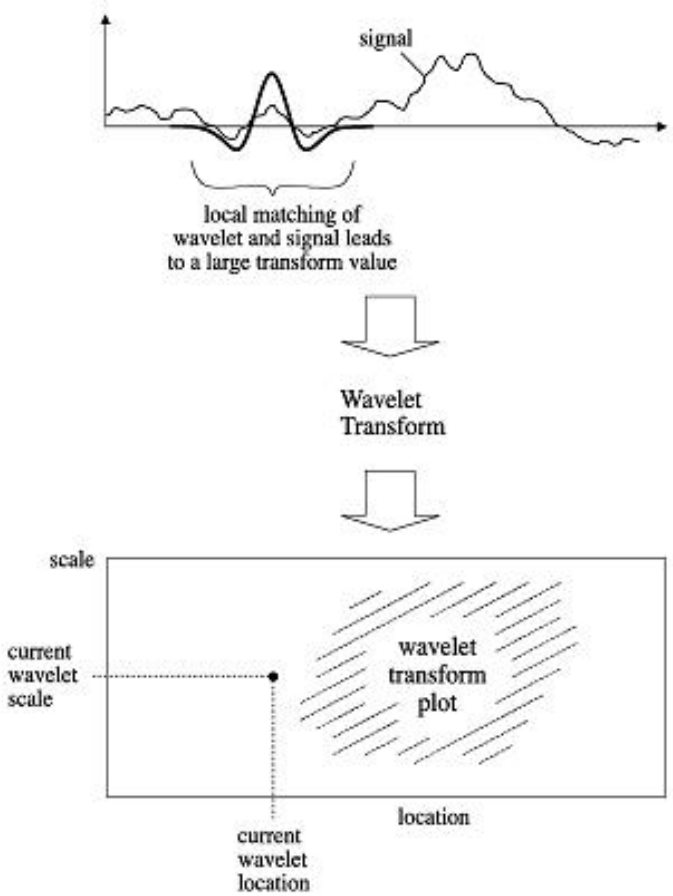

Figure 3.2. 1D wavelet transform

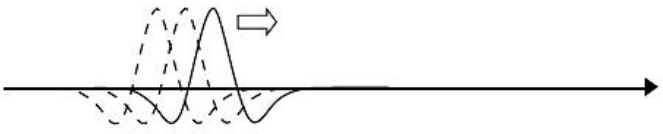

Figure 3.3. Change in location of a wavelet

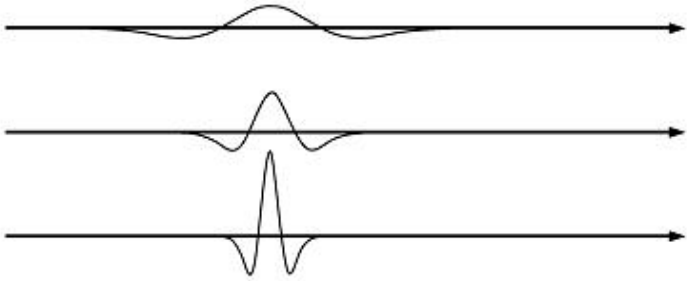

Figure 3.4. Change in scale of a wavelet

wavelet transform and the corresponding output. As it can be seen the final transform plot for a 1D transform is 2D, for values corresponding to various scales and locations of the wavelet. Initially the scale of the wavelet is kept constant and for every location on the time axis, this wavelet is correlated with the signal under scrutiny. After we are done with all locations on the time axis, we now change the scale of the wavelet and repeat the entire process. Hence the 2D transform plot. Figures 3.3 and 3.4 show the effect of the changes in the location and the scale of a wavelet.

The wavelet that has translation parameter $b = 0$ and scaling parameter $a = 1$ is called the mother wavelet. Daughter wavelets are obtained by assigning a and b values. Depending on the application, a signal or image can be broken up into wavelet coefficients using the mother and several daughter wavelets. In our method, we just use a single mother wavelet, and the wavelet used is the $sinc^2$ function, for reasons that the following section provides.

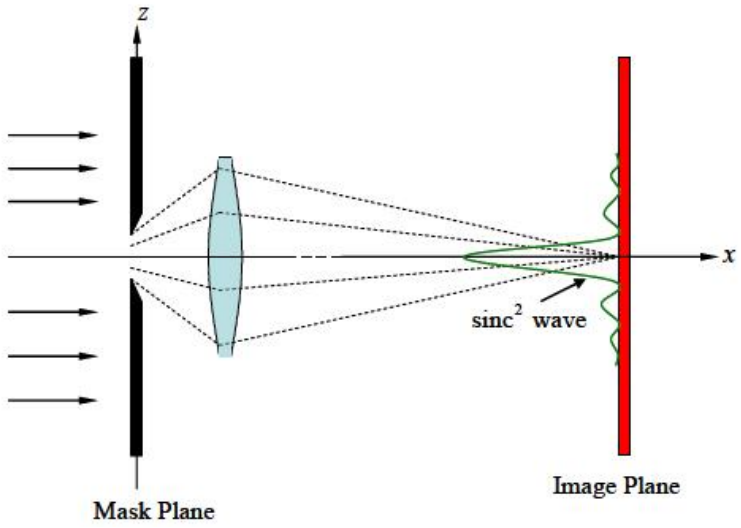

Figure 3.5. Fraunhofer diffraction due to a single slit

3.2 Choice of Wavelet for the System

Consider a setup as shown in figure 3.5. This is a simple single slit diffraction experiment. A lens of an arbitrary pupil shape is placed between mask plane and the image plane. When the rays pass through the lens, diffraction occurs and the rays then converge at the focal point of the lens. This phenomenon is called as Fraunhofer diffraction.

Due to constructive and destructive interference between the light waves, a $sinc^2$ pulse is obtained at the output instead of a rectangle. Similar wave formation is seen for masks that contain polygons. Since the aerial image of a single rectangular slit based on far-field Fraunhofer effect is a $sinc^2$ wave, we use the $sinc^2$ wavelet to approximate the aerial image at any given point. The $sinc^2$ function is then made a function of the parameters a and b, scale a chosen for the wavelet depending on the optical system parameters and b depending on the location where the aerial image needs to be calculated.

3.3 Aerial Image Intensity Calculation

Aerial image intensity calculation is the first step in the process of lithography simulation. The accuracy of the overall simulation process depends on the accuracy of this step as the final edge locations of the polygons on the silicon wafer depends on the image intensity at the photoresist. The image intensity for our method is obtained by the wavelet transform (correlation) of the mask function $t_m(x, y)$ defined earlier in 2.1 with the wavelet function $\psi(x, y)$, the 2D $sinc^2$ function in our case. The region of support for the wavelet is fixed to be equal to the optical diameter (1μm) as in figure 3.6. This parameter defines the region of influence around the current point under consideration, say (x, y) and the aerial image intensity calculated at this point is a function of the mask pattern within the optical diameter. The aerial image intensity calculation at any point b is obtained by placing the wavelet centered at that point, setting the scale of the wavelet and then a correlation of the wavelet with the portion of the mask within the optical diameter. For the purpose of our

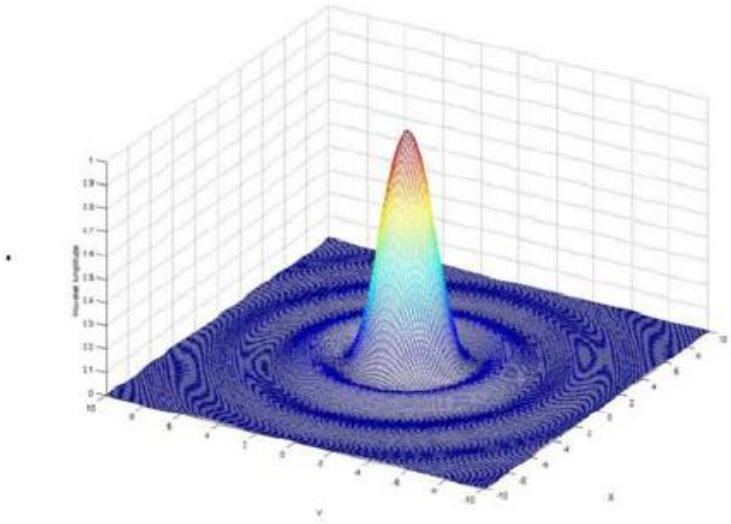

Figure 3.6. Sinc squared sunction with support over a circular region

simulation, the wavelet is stored as a 2D mesh and the magnitude at any point is a

function of the radius of the point from the point at which the center of the wavelet is placed. The mask is also stored in the same way as the wavelet. The aerial image intensity value is then calculated as in equation 3.2 given below.

$$I(x, y, a) = \sum_{x} \sum_{y} \psi(x, y, a) \times t_m(x, y) \tag{3.2}$$

Here $I(x, y, a)$ is the transform value at location (x, y) and scale of wavelet a. The wavelet is a function of the location and scale, while the mask function $M(x, y)$ is just a function of the location (x, y). The choice of wavelet scale is mentioned in the sections that follow. A pictorial description of the above equation is shown in figure 3.7. As

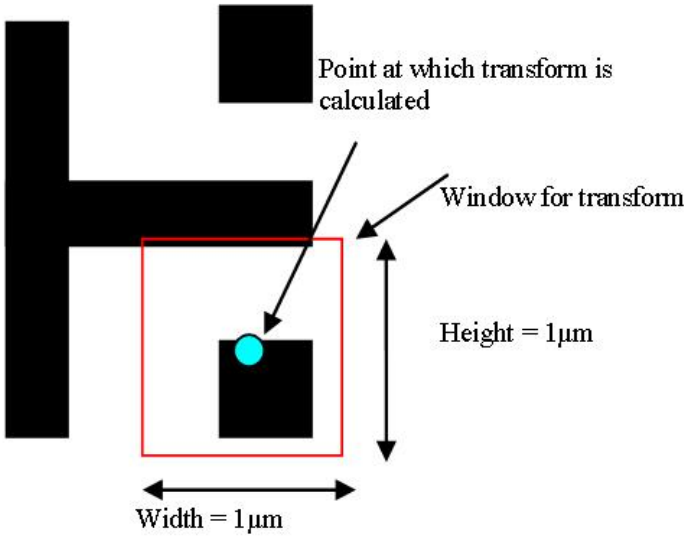

Figure 3.7. Window considered for wavelet coeffecient calculation

the wavelet function is symmetrical, just one quadrant of the wavelet is calculated and used for all four quadrants of the image to reduce unwanted computation.

3.4 Edge Detection

As mentioned earlier, the edges of the polygons printed on the silicon wafer do not match those on the mask due to a number of factors. The ultimate objective of lithography simulation is to detect accurately enough, the locations of these edges post lithography. The aerial image intensity, the key factor in edge detection, is the intensity of light just above the optical resist present over the silicon wafer. If the image intensity at a point on the resist exceeds a certain threshold, the resist is activated and undergoes chemical changes as explained earlier. The modeling of this phenomenon is done using the aerial image intensity. The constant threshold model [6] uses a single constant value, calculated from the normalized aerial image intensity profile as the Edge Detection value as defined in equation 3.3. This value is set once and then used to predict edges for the rest of the mask. We use this model also known as the 0.3 contour method. Consider the example in figure 3.8, of an aerial image obtained for a single feature.

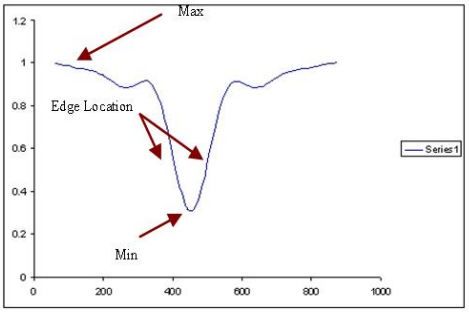

Figure 3.8. Edge detection value calculation

$$\text{Edge detection Value} = min + 0.3 \times (max - min) \tag{3.3}$$

The Max and Min values are calculated as the maximum and minimum values for the given aerial image. The edge detection value is then calculated as given as above

in equation 3.3. After we calculate the edge location value, we look for it in the aerial image and hence we get polygon edge position post optical lithography using the 0.3 contour method. In figure 3.3 min and max are calculated as explained and the points marked by edge location in the figure are the locations at which the final edge placement of the polygons happens.

CHAPTER 4

SOFTWARE SPEEDUP TECHNIQUES

Calculation of the transform coefficients is a time intensive process. In order to achieve a speed up, we use a number of software speed up techniques to try and simplify the calculation. We describe the 3 methods where the largest benefits were observed.

4.1 Reduce Computation Region

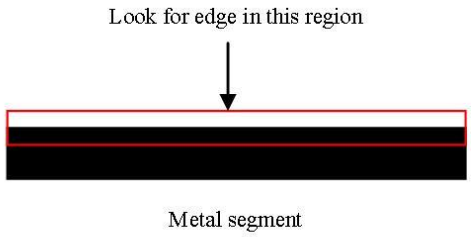

Figure 4.1. Search region for polygon edges post lithography

In calculating the final edge placement points for features on the mask, we need only a few simulation points as is seen in the 0.3 contour method for edge detection. It is observed that in most cases, the edge on the silicon wafer will lie more or less around the edge of the polygon in the mask. So the search begins around the edges of polygons in the mask for the edge detection. This is highlighted in figure 4.1. In order to further simplify the process of locating the feature edge, slope estimation method is used. We calculate the transform at 2 points and then using the slope

of the line between them, the edge location is estimated, which in turn becomes the next simulation point, until the simulation converges. This technique produces a considerable speedup without any loss in accuracy.

4.2 Use Variable Sampling to Reduce Simulation Points

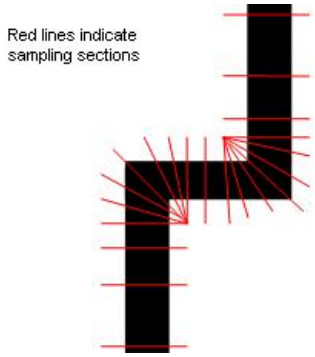

Figure 4.2. An example where selective sampling is used

In addition to limiting the region within which we search for edges, a sampling algorithm is used that determines the points along the edge of a polygon where wavelet simulation is performed to obtain the edges of the contour post lithography. Such contour approximation technique further improves the simulation time. In regions where the aerial image is expected to be affected due to additional factors like close proximity of other features or along feature corners where problems like corner rounding and variations in line width and height may occur, a higher sampling rate is used for determining the edge of the contour. Figure 4.2 and 4.3 show a couple of the many situations where variable sampling will be used along the edges of the features on the mask. At other regions where we do not have additional factors affecting the aerial image, we use a low sampling rate, as the edge location; post lithography at such locations on the mask will not vary much as we move from one point to the next. By using the sampling method, there is some loss of accuracy in the low sampling

regions, but judicious selection of sample points reduces possibility of error in edge detection, while the simulation performance gain is significant.

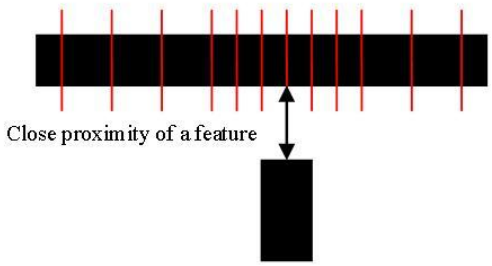

Figure 4.3. Another example where selective sampling is used.

4.3 Use Spatial Locality of Transform Coefficients

This is based on the fact that transform coefficient magnitude at a point is the function of the mask pattern in the window around the (x, y) location that we currently calculate the coefficient at. As we move from the current location to the next, unless we have a large change in x or y value, a portion of the mask pattern within the window at the next (x, y) location will be the same as before, indicating that the transform coefficient may not have changed much. Say that we are detecting an edge at a location (x_1, y_1) for a polygon edge extending in the x direction. If the edge for this point is found at a point (x_1, y_{edge}), as we move along the x-axis to the next (x_2, y_1) location, the edge at that point will most likely be found at more or less location (x_2, y_{edge}). We use this history information to speculate where the edge for the current simulation point lies.

4.4 Use Pre Computed Transform Coeffecients

The Wavelet transform as described earlier is a convolution between the wavelet and the mask, the mask described by the transmittance function $t_m(x, y)$ as described

earlier. From the experiments conducted, which are described in the later sections of this document we found that wavelet Scale is related to the focus of the optical system. Hence, once the focus in the optical system and hence the scale of the wavelet has been set, it can be computed once and the transform coeffecients can then be calculated at the required sections of the mask. Every polygon in the mask can be broken up into rectangles and by pre computing the transform coeffecients, a significant amount of computational effort can be saved, thus enabling the system to run litho simulations on very large circuits. The example shown in figure 4.4

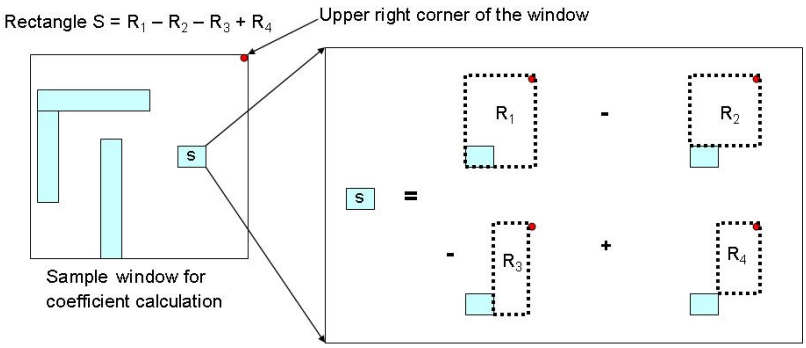

Figure 4.4. Rectangle lookup table method

illustrates the method. Consider a table that has pre computed transform coeffecient values such that the value in the lookup Table at index (x, y) holds the value for the transform coeffecient of a rectangle with lower left coordinates (x, y) and upper right coordinates as those of the window we consider for wavelet transform. So to calculate the contribution of a rectangle with lower left coordinates (x_0, y_0) and upper right coordinates (x_1, y_1), the calculation of coeffecient is as in equation 4.1 which is the method used by the author of [19].

$$R_i = L_{x_0y_0} - L_{x_0y_1} - L_{x_1y_0} + L_{x_1y_1} \tag{4.1}$$

Where R_i is the transform coeffecient calculated for the i^{th} rectangle in the Mask

L_{mn} = lookup table value at index m, n

Every rectangle in the mask can be broken up into upper right corner rectangles and hence the contribution of each rectangle can be calculated using this method. The calculation of the transform coeffecient for a window is then calculated as follows: Let $I_0(x, y, a)$ be the transform coeffecient for a window with no polygons at scale a. As a result the transform coeffecient and hence aerial image intensity $I(x, y, a)$ at any point can be calculated as:

$$\begin{aligned} I(x,y,a) &= \sum_x \sum_y \psi(x,y,a) t_m(x,y) \\ &= I_0(x,y,a) - \sum_{i=1}^{n} R_i \\ &= I_0(x,y,a) - \sum_{i=1}^{n} \left(L^i_{x_0 y_0} - L^i_{x_0 y_1} - L^i_{x_1 y_0} + L^i_{x_1 y_1} \right) \end{aligned} \tag{4.2}$$

CHAPTER 5

PROCESS VARIATION MODELING

5.1 Motivation

Printed image on silicon wafer differs from layout due to optical diffraction. OPC is a layout distortion technique to improve printed image. During manufacturing, parameters such as focus, dose and resist thickness may vary within tolerance margins. These factors contribute to additional distortion of expected printed shape, not addressed directly by OPC. So as the optical lithography system moves from one spot to another, during the wafer printing process there is always a small change in the optical parameters. The Edge detection Value, as defined earlier in equation 3.3 is a function of both the focus and dose of light considered.

As a result due to varying optical parameters, the edge detected at a point with and without variations differs and that can lead to problems in case of aggressive design strategies, where the designer has made use of every little bit of silicon area to pack the layout with polygons considering static optical parameters. In such a case there can be bridging or open circuit faults in the final layout. To ensure a robust IC, a process window consideration is extremely important while running lithography simulations as we scale the technology even further, where the sensitivity of patterns printed on silicon to process variations is very high. The major sources of variation arise from the focus and dosage of the optical system. For our System, we consider variations in focus of the optical system. In the sections that follow, the experiments conducted to relate the focus of the optical system to the scale of the wavelet system are discussed after which we arrive at the variational focus model for our System.

5.2 Previous Work

The manufacturing process undergoes variations, and the traditional models used for lithography and OPC are based on a single focus or dose thereby ignoring this fact as stated in [22]. Work has been done to incorporate process variation in OPC as seen in [22] and [5], where the process window is chosen based on extensive lithography simulations. Takase in [23] investigates the defocus impact on OPC mask layout, compares the printability of masks for various defocus conditions and gives recommendations for model building. In [28], the authors introduce Variational Lithography Modeling (VLIM) and derive an equation that shows aerial images to be a function of the in focus aerial image and the defocus. The authors of [30] and [31] extend the VLIM model to introduce the Variational-Edge Placement Error (V-EPE) model to account for variations in dosage. In [15], the authors introduce the concept of Process Window Optical Proximity Correction (PWOPC) which in addition to fulfilling the standard OPC objective of ensuring mask transfer fidelity, also ensures high yield.

5.3 Variational Focus Model

Variational focus model is easily established on the basis of single slit imaging equations. The basic idea is that as focus (parameter z in figure 5.1) changes so does the image. We would like to capture the change in image due to change in focus using a Taylor series expansion method. For small changes in focus, a first order term will suffice while for larger change, higher order terms will be necessary. Variation in dose or resist thickness changes the resist simulation model and outside the scope of pure optical simulation, which is the thrust of this paper. Referring to figure 5.1, let d be the size of the slit used in optical imaging, θ is the angle made by line OP with line OQ. Q is a general point at which we intend to find the image intensity. Point Q is at a distance y from the normal OP and the distance OP is the focal length z. The image intensity at point Q is as given by [9].

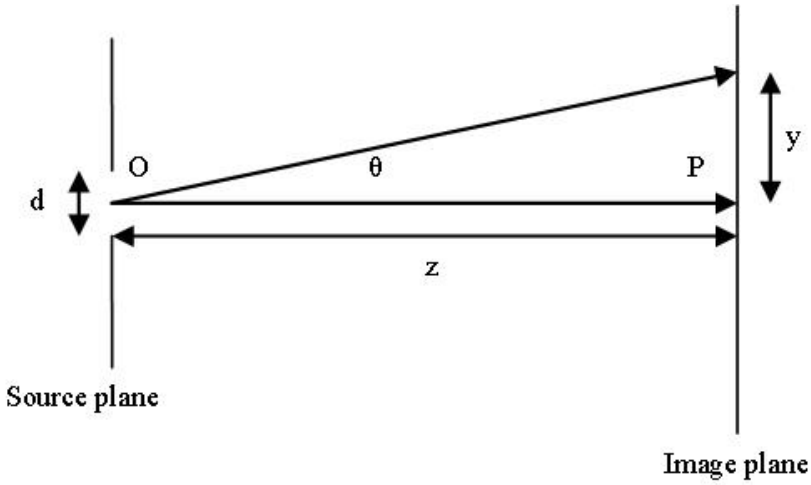

Figure 5.1. Figure explaining the variation focus model

$$I(\theta) = \frac{I(0)}{z^2}\left(\frac{sin\left(\frac{kdsin\theta}{2}\right)}{\left(\frac{kdsin\theta}{2}\right)}\right)^2 \tag{5.1}$$

Where $I(0)$ is a function of the slit width d, constant in our case, k is called the wave number $\frac{2\pi}{\lambda}$, where λ is the wavelength of light used. From the figure 5.1, it can be seen that $sin\theta = \frac{y}{\sqrt{y^2+z^2}}$, and since$z \gg y, sin\theta \approx \frac{y}{z}$ Hence equation 5.1 now takes the form

$$\begin{aligned} I(z,y) &= \frac{I(0)}{z^2}\left(\frac{sin\left(\frac{kdy}{2z}\right)}{\left(\frac{kdy}{2z}\right)}\right)^2 \\ &= \frac{4I(0)}{(kdy)^2}\left(sin\left(\frac{kdy}{2z}\right)\right)^2 \end{aligned} \tag{5.2}$$

Note here that y and z are independent variables Differentiating equation 5.2 with respect to z

$$I'(z,y) = (-1)\frac{2I(0)}{kdyz^2}sin\left(\frac{kdy}{z}\right) \tag{5.3}$$

Once again differentiating equation 5.3 with respect to z

$$I''(z,y) = \frac{2I(0)}{kdy}\left(\frac{2}{z^3}sin\left(\frac{kdy}{z}\right) + \frac{kdy}{z^4}cos\left(\frac{kdy}{z}\right)\right) \tag{5.4}$$

The Taylor series expansion for any function about a point is given by:

$$f(x) = f(x_0 + h) = f(x_0) + hf'(x_0) + \frac{h^2}{2!}f''(x_0) + ... \tag{5.5}$$

Here x_0 is the point around which the function is to be approximated and $h = x - x_0$. In our case, is the value of z for no defocus condition say z_0, and h is the defocus $h = z - z_0$. using equations 5.2, 5.3 and 5.4 in 5.5, we have:

$$\begin{aligned} I(z,y) &= \frac{4I(0)}{(kdy)^2}\left(sin\frac{(kdy)}{2z_0}\right)^2 - (z - z_0)\frac{2I(0)}{kdyz_0^2}sin\left(\frac{kdy}{z_0}\right) \\ &\quad +(z - z_0)^2\frac{2I(0)}{kdy}\left(\frac{2}{z_0^3}sin\left(\frac{kdy}{z_0}\right) + \frac{kdy}{z_0^4}cos\left(\frac{kdy}{z_0}\right)\right) \end{aligned} \tag{5.6}$$

Hence, we have the image intensity function $I(z,y)$ as a function of change in focus $h = z - z_0$. In our simulator, this image intensity that arises due to a single slit is used as the wavelet.

Equation 5.6 indicates that a wavelet at any focus around the initial chosen focus can be approximated as a function of the nominal focus value and some additional correction terms which are functions of the difference in focus. Consider the aerial images formed $I_1(x,y)$ and $I_2(x,y)$ calculated at focus values z_1 and z_2. Hence the difference in the aerial images is given by:

$$\begin{aligned} I_1(x,y) - I_2(x,y) &= \sum_x\sum_y \psi_1(x,y)t_m(x,y) \\ &\quad -\sum_x\sum_y \psi_1(x,y)t_m(x,y) \\ &= \sum_x\sum_y t_m(x,y)\left(\psi_1(x,y) - \psi_2(x,y)\right) \end{aligned} \tag{5.7}$$

Hence we conclude from equations 5.6 and 5.7, that the aerial images computed at any focus can be computed without much of a computation effort once the nominal focus aerial image is known. This is similar to VLIM model principle [30].

5.4 Relationship between the Focus and Scale

The equations described in the previous section were based on a simple distance from the apertue to the image plane. In our system, we arrive at our end result by an approximation of what actually happens as the rays of light travel through the mask and the objective lens. We dont really calculate the actual distance from the mask to the resist. Hence, the z that try to find is based on a pure experimental basis. Once that infocus z is set, the remaining aerial images at various focus values can be found out by the relation from equation 5.6. In order to establish the relation between scale and z, a number of simulations were run on sample masks considering various focii and the aerial images obtained from a commercial lithography simulator and our tool were compared. We show the analysis we performed for some of the masks considered in the experiments.

We measure the nominal focal distance from the mask plane to the top of the resist. The simulation system is designed such that any deviation from the nominal focal length of (+/-) 5nm can be handled by the system and since we use the 45nm technology for experiments, these variations are reasonable [1]. The results were generated for the sample masks moving in the described focus range in steps of 0.5 nm. For every focus in the optical system there is an equavalent wavelet scale. Consider the sample mask in figure 5.2. Here red lines indicate the sections at which we ran the simulation and compared results. We generated aerial images at those x and y locations and compared them with the results we had from the commercially available software. Figure 5.3 shows the aerial images obtained from both the simulators at a section considering a system focus at nominal. Further experiments were also run,

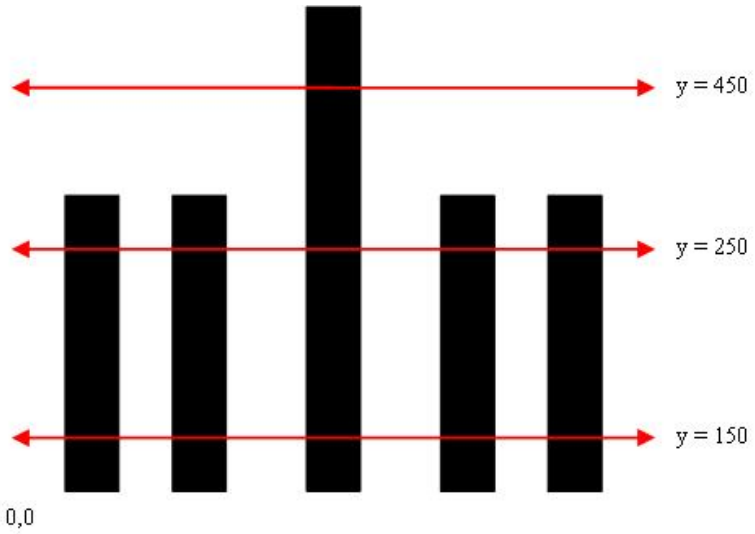

Figure 5.2. Mask considered with system focus set at nominal

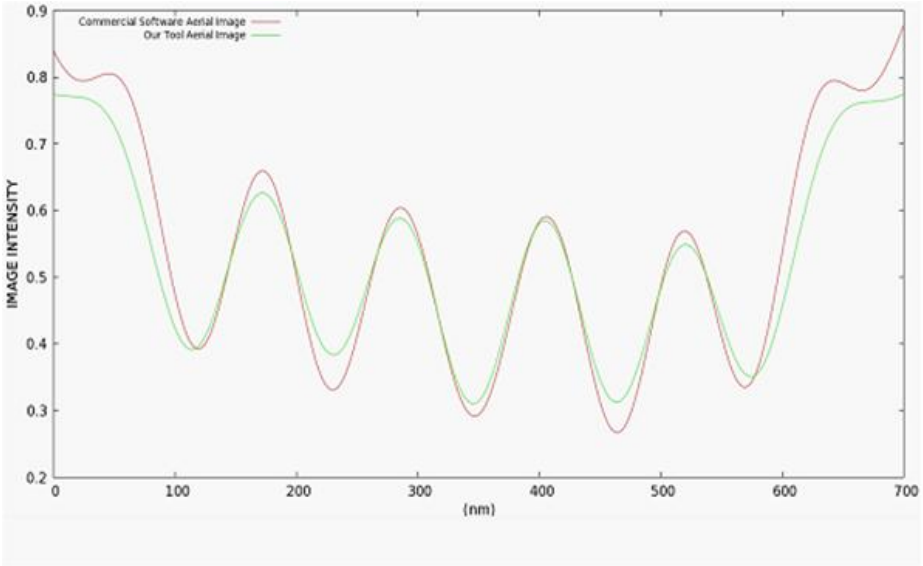

Figure 5.3. Aerial image comparison at y = 250 nm.

the results of which are shown in the results section. From our observations, we found a linear curve that relates the focus to scale given in equation 5.8.

$$Scale = 0.72(defocus) + 22.42 \tag{5.8}$$

CHAPTER 6

DOUBLE PATTERNING LITHOGRAPHY

6.1 Introduction

As mentioned earlier optical lithography is a complex process involving a number of steps, the final outcome of which is a mask pattern on the silicon wafer. There are a number of factors that affect fidelity of this process; interference and diffraction in sub-wavelength lithography are some of the problems faced in mask manufacturing. As a result what is seen on silicon in often not the exact replication of the features on the mask. This can lead to variations in expected and measured circuit parameters before and after manufacturing. These problems tend to get worse with scaling. Mask transfer fidelity issues are countered using a number of Resolution Enhancement Techniques (RET) which include Optical Proximity Correction (OPC), Phase Shift Masking (PSM), Sub Resolution Assist Features (SRAF) and Dual Patterning Lithography (DPL). In these methods the original mask is distorted in some shape or form so that the final printed image on silicon best resembles the features on the mask. In Alt-PSM, the phase of light is shifted by 180 at selected sections to ensure better mask printability; in OPC mask structures are pre-distorted such that distorted image of this mask is an accurate image for the intended structures to be printed; and in SRAF, additional dummy structures are added to the mask to control optical diffraction such that the actual intended patterns are obtained. An overview of Alt-PSM, OPC and SRAFs can be reviewed in [16]. DPL reduces wafer throughput but has become a necessity in current and upcoming technology nodes. It involves splitting patterns in a mask into two masks that are exposed separately. DPL CAD

problem is a pattern coloring problem to minimize mask edge placement error (EPE). EPE results from interaction of near field waves and any geometric solution that does not consider interaction of fields, suffers from inaccuracies.

However as we enter the 22/32nm technology era, lithography systems are pushed to its fundamental limit. The next generation of lithography known as Extreme Ultra Violet (EUV) introduction has been delayed due to the complexity involved [18] [11]. The basic metric in optical lithography is minimum printable half pitch which is given by Rayleigh criterion [16].

$$\text{half pitch} = \frac{k_1}{NA}\lambda \tag{6.1}$$

Here, k_1 is the process difficulty factor, $NA$is the numerical aperture and λ is the wavelength of light used. For the minimum half pitch to be as low as possible λ needs to be low i.e. light of smaller wavelength needs to be used and the NA needs to be high. The current technology uses 193nm light source and achieving high NA is a significant challenge [32]. This results in pushing the k_1 factor to its limit. Even at the low k_1 values ($k_1 = 0.315$) DPL becomes necessary to achieve minimum half pitch for 45nm technology [24] [3].

6.2 Motivation and Background

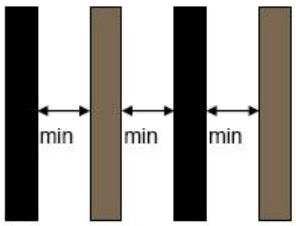

Figure 6.1. A color assignment using DPL

In traditional DPL, the layout is decomposed into two layouts such that every polygon in the new layouts is not within a certain minimum distance of one another.

In Figure 6.1, it can be seen that since the metal segments violate the minimum distance criteria, they are colored differently. Two separate exposures and etch steps are then used to print the final layout on silicon. DPL allows aggressive design using currently available lithography technology for better printing resolution, DOF (Depth of Focus) and pitch width [11] [32]. However for dense and complicated layouts, a simple solution for the entire mask as depicted in Figure 1 is not always possible. There are cases where coloring conflicts arise. An example is shown in Figure 6.2. It can be seen that a color conflict arises in Figure 6.2(a) and hence a split or stitch in required in the longer metal line as shown in Figure 6.2(b). The stitch is absolutely essential and at the same time it is not easy to control alignment during manufacturing. The stitching requires small errors in overlay control [14]. The splitting also increases the mask complexity and manufacturing cost as it increases the number of line ends, hence creating additional cases for line edge shortening and yield loss [11] [13]. So a split is something that is to be avoided unless there is no other alternative. Work has been done on the decomposition and splitting

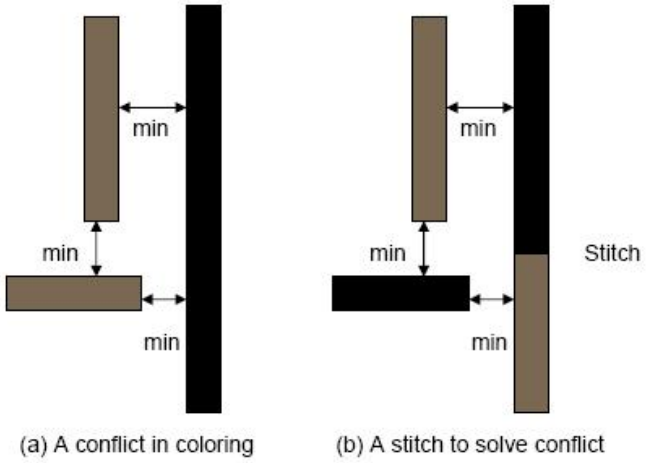

Figure 6.2. An example involving a stitch

of layouts for DPL. In [8] troublesome patterns are cut when coloring conflicts are

found. A pre-fragmentation process is done on the features in [4] for coloring. But however as mentioned in [32], these algorithms do not optimize coloring and stitching together which could make algorithm convergence faster. In [11], the authors use conflict-cycle detection and ILP to perform coloring and hence reduce line ends and design rule violations. Even in this method the optimization for irresolvable conflict cycle detection and stitch minimization is not done simultaneously leaving room for improvement. In [32], the authors use a grid model where the smallest feature in the layout fits exactly on a grid and they do simultaneous conflict cycle and stitch detection. In addition to that, they use independent component computing and layout partitioning, and a divide and conquer methodology to be able to run the simulation and achieve results in a timely manner. All these methods are based on minimum

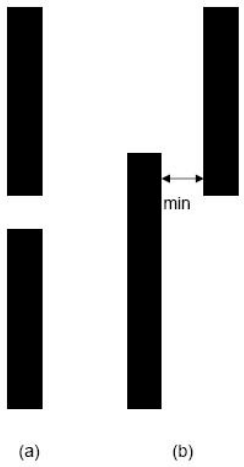

Figure 6.3. An example of a possible gain scenario in sub-wavelength lithography

distance criteria and not on lithography simulation. The methods discussed do not make use of the fact that sometimes having a net close to another in the layout may have a rewarding result. Corner rounding and line end shortening are known problems that arise in sub-wavelength lithography. The final required result is that the EPE between the edges of the nets on the mask and the corresponding nets on

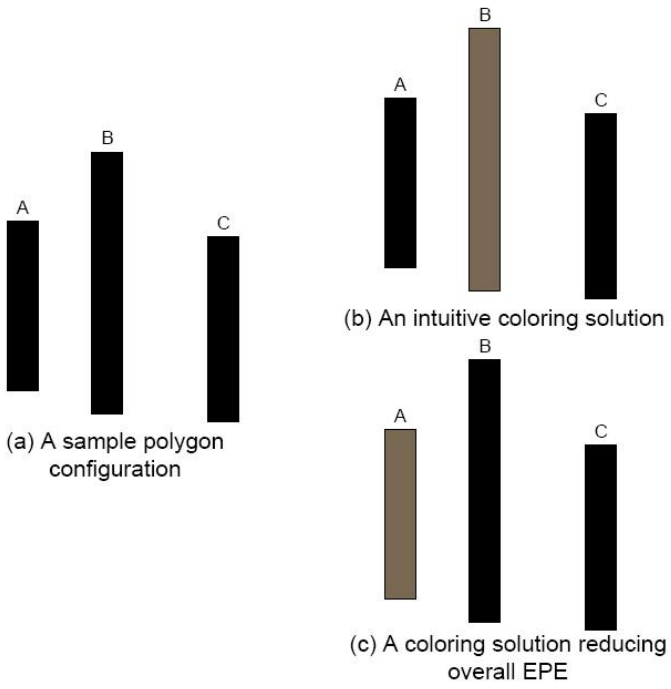

Figure 6.4. Another possible gain scenario in sub-wavelength lithography

the silicon wafer be as small as possible. A proper placement of nets may ensure that the effects of corner rounding and line end shortening are mitigated at least to some extent reducing the need for expensive RET's like OPC to ensure a low Edge Placement Error (EPE) in these sections. Consider the situations that arise in figure 6.3(a) and Figure 6.3(b), a couple of the many situations that are not considered by the existing solutions. In Figure6.3(a), the placement of the two nets very close to one another ensures that the problems of interference and diffraction in sub-wavelength lithography are used to an advantage reducing the line end shortening in this case. In 6.3(b), previously used methods may mark the nets such that they are placed on two seperate layers, however by placing these nets close to one another on the same layer, the corner rounding effect and the line end shortening can effectively be tackled in an elegant way. Another situation is depicted in Figure 6.4. In Figure 6.4(b), the intuitive solution is shown, which may result in an EPE less than the one that arises

from Figure 6.4(a), which however does not mitigate line end shortening or corner rounding. Also it may well be the case that the combined effect of having polygons A and C on the same layer as polygon B actually deteriorates the EPE of polygon B but having one of them close to polygon A may have a good effect with respect to EPE reduction. If the coloring scheme of Figure 6.4(c) is decided upon, a better overall EPE reduction may be obtained which is what our proposed method looks for.

Our work is different from previous work in that we employ the use our proven fast lithography simulator to predict layout distortion and hence partition the layout based on the observed EPE and max EPE at locations in the polygons. A detailed description of the algorithms used is discussed in sections 6.3 and 6.4.

The major contributions of toward DPL using our method includes:

- The use of a fast lithography simulator to predict feature distortion in layouts as opposed to minimum distances between features as previously used. This method increases runtime, but promises more concrete results.

- The use of algorithms in layout partitioning such that the problems arising in sub-wavelength lithography may be used to our advantage in reducing overall EPE.

- The use of a simultaneous color and split method for DPL optimization. As mentioned in [32], the color and split of polygons in a mask is highly correlated, hence we optimize moving nets to various layers performing these operations at the same time as and when needed.

- The potential reduction of stitching polygons as compared to previous work. We assign costs to moving and stitching polygons in the mask and stitching is often avoided unless the damage done is indeed catastrophic, which can be measured

with respect to EPE post lithography. A metric based on the maximum EPE error at a target location is used to decide if the stitch is indeed the best option.

6.3 Methodology

As mentioned earlier, DPL is a mask partitioning technique done to ensure printability in the sub-wavelength regime. Printability is affected by edge diffraction and interference. DPL tries to mitigate these issues by taking polygons in the mask and assigning them to separate layers, such that the sub-wavelength printability issues are minimized. Unlike previous approaches [11] [32] [8] [4], we use a system, where in addition to bad effects of having polygons close by, we also consider the good effects of having polygons close to one another in the layout in the effort to maximize gains. In this section, the initial pre-processing of the layout is described such that we have information to make well informed decisions regarding the moving of polygons to another layer, or stitching them.

6.3.1 Pre-processing

The printability of polygons on the mask is affected by close proximity of other polygons. We try to take advantage of this effect with an objective of reducing overall EPE for all polygons in the mask. There exists a region of influence called the optical diameter (a parameter that varies with the wavelength of light used and the technology node) around a target polygon, within which if another polygon exists, it will have some influence on the final edge placement of the target polygon on silicon. An initial pre-processing on the mask is performed to mark all polygons that may affect a target polygon. This is done by growing the target boundary by optical diameter to mark the optical bound of a polygon as depicted in Figure 6.5. It can be seen that the optical bound is created by taking a distance equal to the optical diameter from the edges of the polygon and creating a larger version of the target

polygon having the same shape. The other polygons within the bound are those that

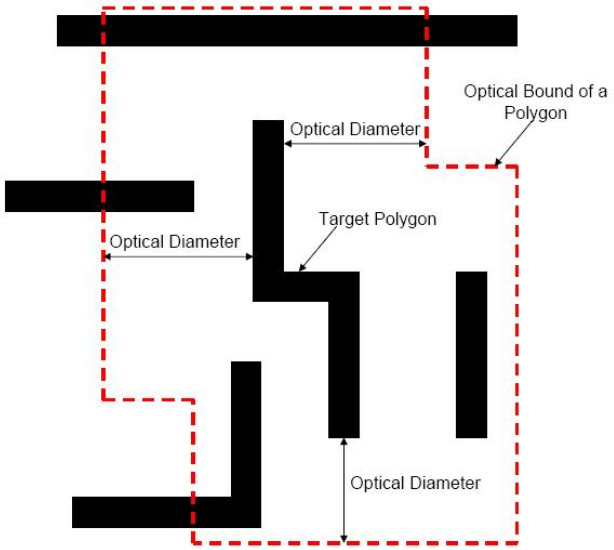

Figure 6.5. The optical bound of a target polygon and polygons within that bound

will have an effect on the edge placement of the target polygon on silicon. Once the optical bound has been created, the sections of the target polygon that fall within the optical bound of the other polygons within its bound are marked as being affected by them. This is the initial pre-processing required to find dependencies between the various polygons. This step is somewhat equivalent to the polygon coloring followed by authors of [11]. However here we have additional information that permit informed decision making based on mutual effects of polygons on one another before and after removal of any polygon in the mask in post lithography simulation.

6.3.2 Mark Possible Stitch Locations

The necessity of stitches was described earlier. Stitching allows the design to retain its complexity and at the same time have a low final EPE in the layout. Even though this process is absolutely essential, it comes at a price. As mentioned earlier, stitching requires tight overlay control and could potentially causes yield loss. We want to try

and avoid stitching as much as possible unless absolutely necessary. This is where the benefits of using a model based approach as opposed to a rule based approach become highly evident. After the decision to move a polygon is made, stitch decisions are reviewed. We measure the distortion in the target shapes and trade-off cost of a stitch against EPE cost from no stitch. This is the second half of the preprocessing where stitch candidates are marked and used later in making stitching decisions.

We know from simulation, the structures that can pose hazards like short circuit failures. This information is based on a distance metric between the two target contours. We just use this information to avoid unnecessary re-simulation. This is a candidate identification step that must not be confused with a rule based approach. In this step, we mark possibilities and eliminate them later based on EPE distortions

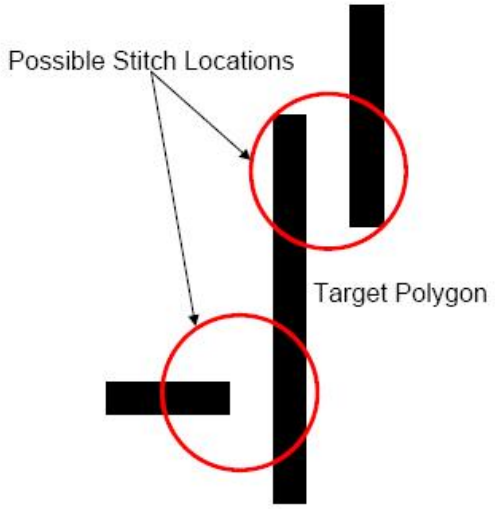

Figure 6.6. Figure depicting the marking of two polygons as stitch candidates

measured from simulation. Figure 6.6 shows a case that will be marked by our algorithm as possible stitching locations. The red circles show the locations. This step is performed along with that mentioned in section 6.3.1 as with the optical bound knowledge, we also have knowledge of stitch candidates.

6.3.3 Single Lithography Simulation Run

It is not possible to accurately predict the effects of the proximity of polygons in the mask based on distances between them. As mentioned earlier, this approach may take away some of the achievable benefits in sub-wavelength lithography. In order to accurately determine affected sections (defined as sections where the EPE is large), it is essential to run a lithography simulation on the entire mask and then rank polygons based on the EPE for those polygons. This is the third pre-processing step in our DPL algorithm. Once the dependencies between polygons are resolved, a lithography simulation is run over the entire mask and polygons are ranked in decreasing order of their EPE. Running a simulation at the granularity of the nanometer will consume too many resources and is wasteful. A discrete sampling of locations at which lithography simulation must be run is sufficient. To that end we use a sampling algorithm to indicate sections where lithography simulation is to be run. A dense sampling rate is maintained at the sections of the polygon that will be affected by neighboring polygons and at corners.

This step of lithography simulation may seem like a huge overhead at first, as polygons are continuously going to be moved from the mask and re-simulation is going to be needed. This overhead is taken care of by knowing in advance the sections of a polygon affected by another polygon in the mask, done in the pre-processing step as mentioned. Hence when a polygon is moved, only those sections of other polygons in the mask affected by that polygon are re-simulated. As a result we have an accurate picture of badly affected polygons by running incremental lithography simulation at a cheap price of re-simulation when changes are made to the layout. The cheap price of the simulation is greatly facilitated by the use of our fast and reasonably accurate lithography simulator based on wavelets.

6.4 Algorithm

Once the initial processing is complete, the DPL algorithm is fully equipped to start. In this section we describe the algorithms used for pre-processing and deciding if a polygon is to be moved to another layer, split or not moved in the first place.

6.4.1 Pre-processing

The pre-processing steps of resolving inter-polygon dependencies, stitch candidate marking and lithography simulation have already been described. The objective is to obtain a set of polygons around the target polygon that will have an influence on the final edge placement of the target polygon. We also run a single lithography simulation on the entire mask to obtain sections of polygons that have a bad EPE. The pre-processing flow is shown in Figure 6.7. In the flow charts of Figures 6.7 and 6.7, N represents the total number of polygons in the mask.

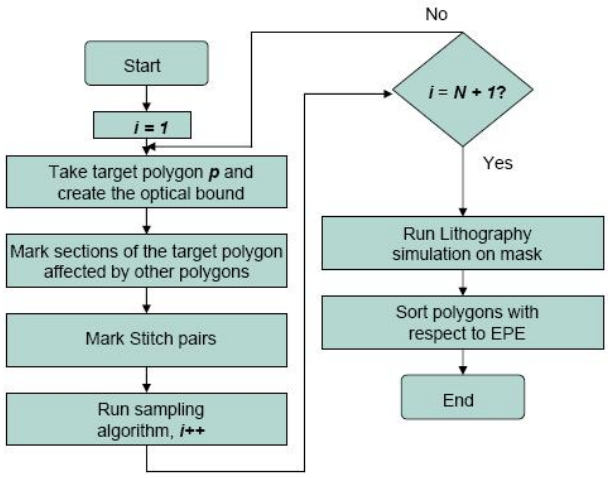

Figure 6.7. Algorithm for pre-processing

6.4.2 Decisions to Partition Layout

As discussed earlier, the move of a polygon is decided not only based on whether its current position worsens the EPE of polygons around it, but also on the beneficial

effect that this polygon may have. The pre-processing sets up the required data structures and resources needed for the DPL flow. In this sub-section the decisions involved in layout partitioning are described. The polygons to be considered for moving or splitting are arranged in a binary tree, sorted with respect to the EPE. Every time, we begin with the polygon having the worst EPE in the layout and perform tests on it to see if it needs to be moved to the next layer or if a stitch is needed in the target or another polygon to reduce EPE. Since we use a sampling

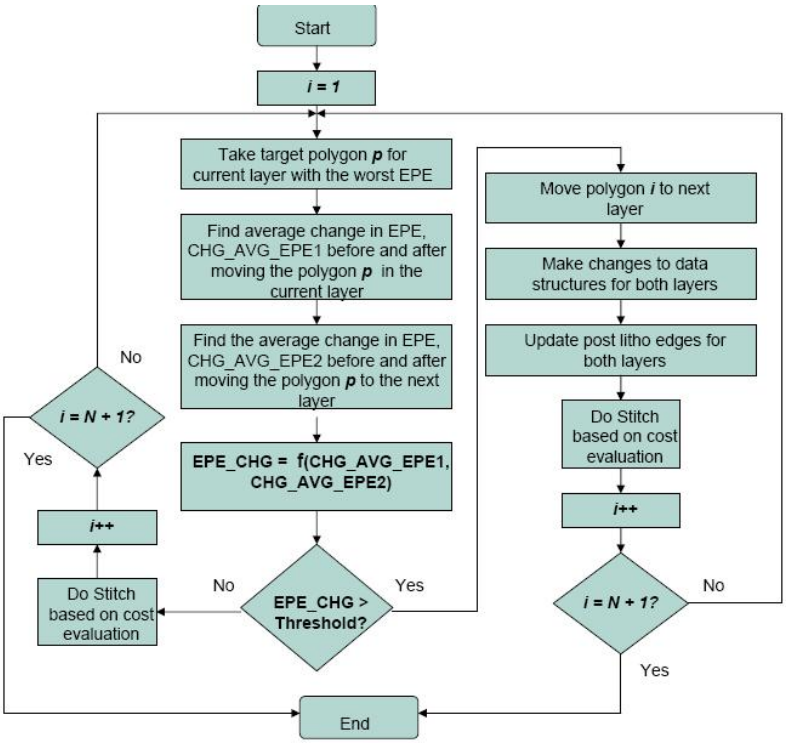

Figure 6.8. Algorithm for polygon move/stitch

algorithm, we use average change in EPE for all polygons concerned in the target and potential layer in which the target polygon is to be moved. When deciding to move a polygon, we calculate average EPE of the target polygon and the sections of all other polygons affected by this polygon before and after moving it. A similar average EPE is calculated for the layer in which the target polygon may be moved.

The overall effects on EPE of moving the polygon to the next layer and keeping it in the same layer are then compared to subsequently make a decision. Once a decision has been made for move based on reduction in EPE, the polygons within the optical bound in the layer decided are tested for stitching by means of max EPE. If we find that the max EPE in any of the stitching candidates for the target polygon is above a threshold (defined as 10% of pitch width in the particular metal layer), we stitch, else we let the EPE error exist. These sections can also be reported to designer for possible design modification if tight EPE specifications are needed. Also we have a minimum overlap of 8 nm at the stitch which is reasonable [1].The flow for polygon move and stitch is shown in Figure 6.8.

CHAPTER 7

RESULTS

In this chapter, we describe the simulation platform on which the test simulations were run. We also describe the results of simulation over a few sample masks comparing results with the commercial lithography tool used for verification of our tool. The results for focus variation are summarized by comparing change in the distribution of metal CD (Critical Dimention) and seperation between metal segments for a benchmark circuit. The DPL results include simulation runs over metal layer 2 of the ISCAS-85 benchmark circuits

7.1 Simulation Platform

The tool we developed to implement the proposed method was written in C++ and it spanned 3000+ lines. The tool was run using a HP Pavilion 6500 notebook with Fedora 10 operating system, Intel Core 2 Duo T7500 @ 2.2GHz and 2GB of RAM. The real benefit of the proposed approach can be seen in larger circuits with focus variations. For the purpose of our experiment, ISCAS-85 circuits were synthesized and mapped to a layout based on 45nm technology. We generated the GDSII layout files for the benchmarks using Cadence Encounter.

7.2 Results of Simulation

For small sample masks the results of final edge placement simulation are compared with the results obtained from the commercial software and our method. Figure

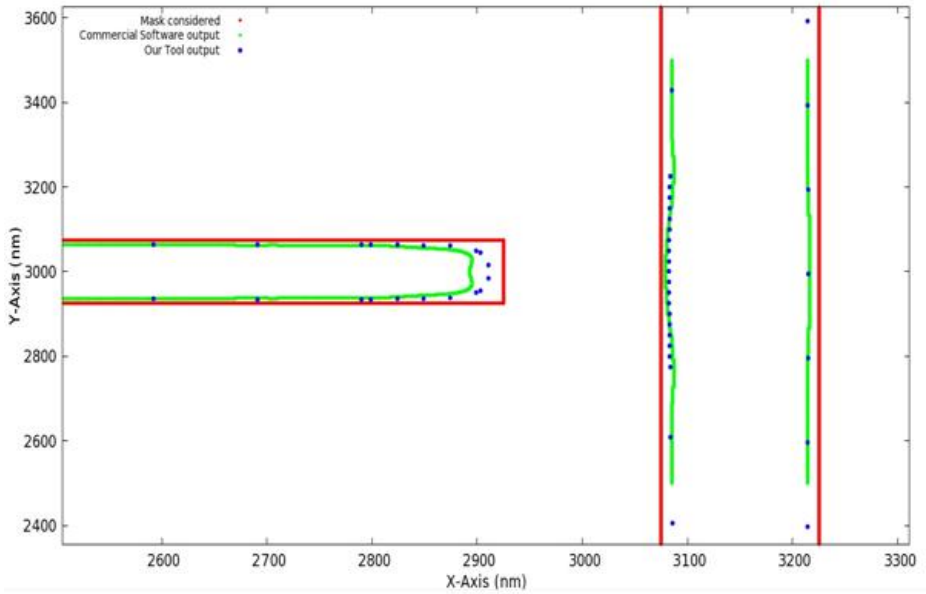

Figure 7.1. Edge placement comparison for sample mask one at nominal focus

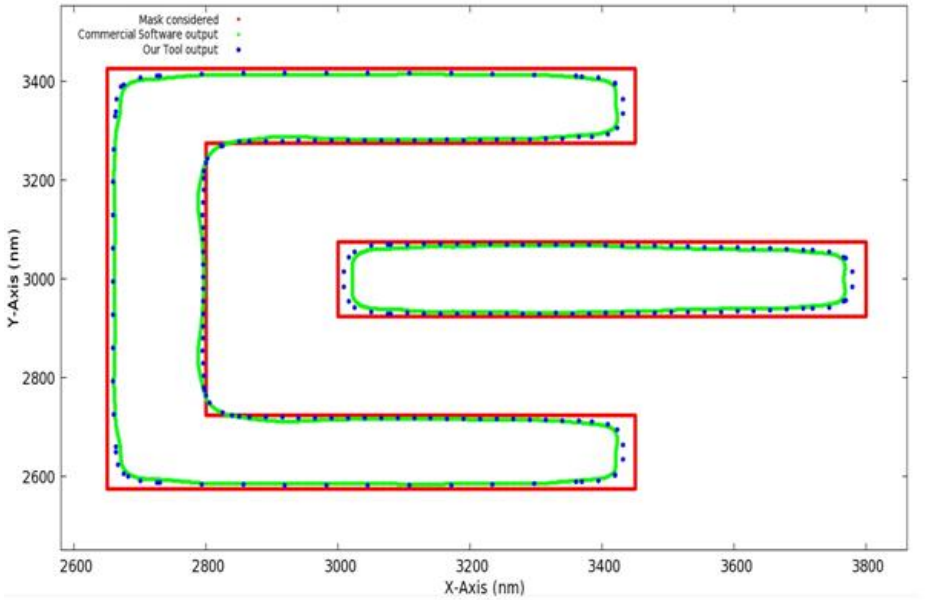

Figure 7.2. Edge placement comparison for sample mask two at nominal focus

7.1 shows the mask considered for comparison as well as the final edge placement using the two methods. From the figure it can be seen that the proposed approximate method is close. Figure 7.2 shows another sample mask we considered and the corresponding results. Once again it can be seen that the final edge placement is highly close. This experiment has been repeated for many such masks but all the image results are not included here. Consider figure 7.3, where validation of the tool is performed at a nominal focus + 5nm. It can be seen that the system approximates the commercial simulator. The results for the 3 masks have been tabulated in table 7.1. We also simulated the ISCAS-85 benchmarks and the results have been tabulated in table 7.2.

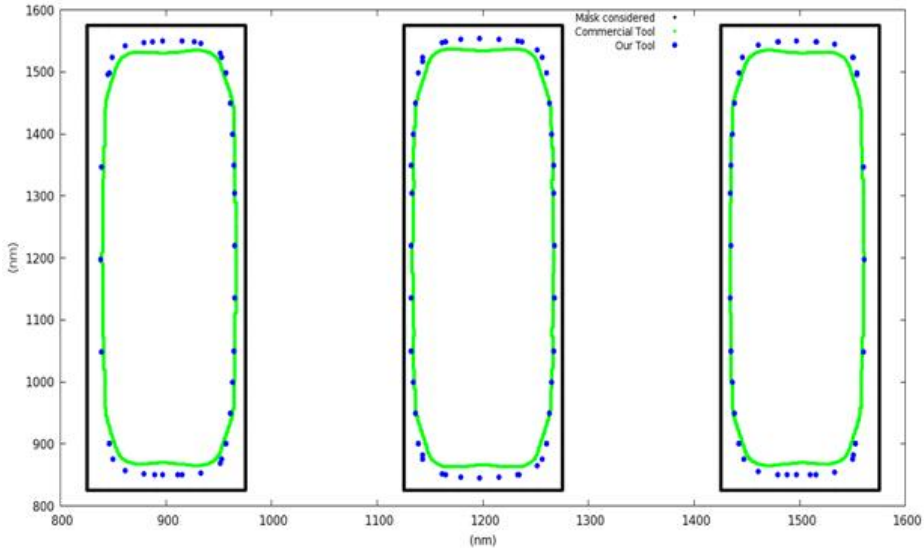

Figure 7.3. Edge placement comparison for sample mask three at focus = nominal + 5 nm

Also for the sample mask three, we show the percentage error in edge placement comparing our result to that of the commercial lithography simulator. The percentage error is defined as the percentage of the width of the metal segment considered by which the edge placement in our method differs from the commercial simulator. For the max error, we considered the largest edge placement error considering all the

Table 7.1. Performance comparison for sample masks considered.

Mask	Simulation time (sec) Proposed Method	Commercial Software	Speedup	% RMS Error
Mask 1	0.7	22	31.4	2.92
Mask 2	0.8	79	98.75	4.86
Mask 3	0.6	12	20	5.8

Table 7.2. Simulation runtime for metal layers of the ISCAS-85 benchmarks.

	C17	C432	C499	C880	C1355	C1908	C2670	C3540	C5315	C6288	C7552
1	12s	3m	2m34s	6m	3m43s	4m	6m	15m31s	15m45s	46m34s	19m16s
2	16s	13m2s	24m	26m21s	25m22s	28m27s	41m	1h33m58s	1h48m9s	3h40m23s	1h29m28s
3	14s	11m7s	21m6s	22m40s	22m	25m43s	42m6s	1h27m55s	1h53m3s	3h29m42s	1h39m11s
4	-	1m20s	4m33s	5m23s	5m	4m14s	10m11s	31m23s	31m18s	46m40s	24m29s
5	-	1s	40s	32s	37s	24s	1m40s	2m47s	10m23s	4m58s	4m40s
6	-	-	6s	1s	2s	-	21s	9s	2m6s	8s	1m47s
7	-	-	-	2s	2s	1s	4s	-	36s	12s	38s
8	-	-	-	4s	1s	-	-	-	8s	-	-

simulation points. The plots at various offset focii from the nominal are shown in figure 7.4.

7.3 Effect of Focus Variation

We ran simulations for metal layer 2 of the benchmarks and to show the effect of the variations in focus on the mask CD for the ISCAS-85 circuit C6288, we plotted a histogram for the mask CD at selected dense metal areas of the mask as well as the separation between metal segments within the optical diameter for a number of sections of the layout shown in figure 7.5 and 7.6. In the histograms, it can be seen that due to changes in focus of (+/-)5nm from the nominal, the distribution of the mask metal CD varies, especially for the 40-60 nm sections. Once again, in the figure 7.6 it can be seen that for separation between metal segments, there is a large difference in the distributions at the extreme focus values we considered. If we have a reasonable change in the focus from the optimal, it may result into bridging

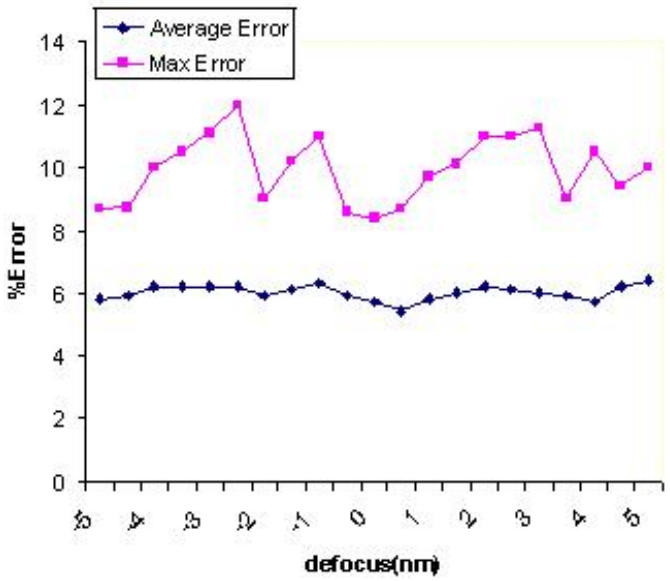

Figure 7.4. Error plot at various focii for sample mask three at focus = nominal + 5 nm

and short circuit faults. Hence the manufacturability of the circuit for a given focus window can be examined and the robustness the design can be observed.

7.4 Double Patterning

In this section the results of running our proposed DPL algorithm on the dense layer, metal layer 2 of the ISCAS-85 benchmarks are discussed. The results are summarized in Table 7.3, where we show the number of polygons in each mask, total number of moves needed, stitches needed and the simulation run time. In comparison with previous work our simulator is slow due to the lithography simulations run, but this is essential to gain the benefits we mentioned in sub-wavelength lithography. A pictorial view of a section of ISCAS C880 metal layer 2 and C432 metal layer 3 are shown in figures 7.7 and 7.8 respectively where each color used indicates a layer to which the polygon belongs. It can also be seen that the placement of polygons is such that EPE at line ends and corners will be reduced.

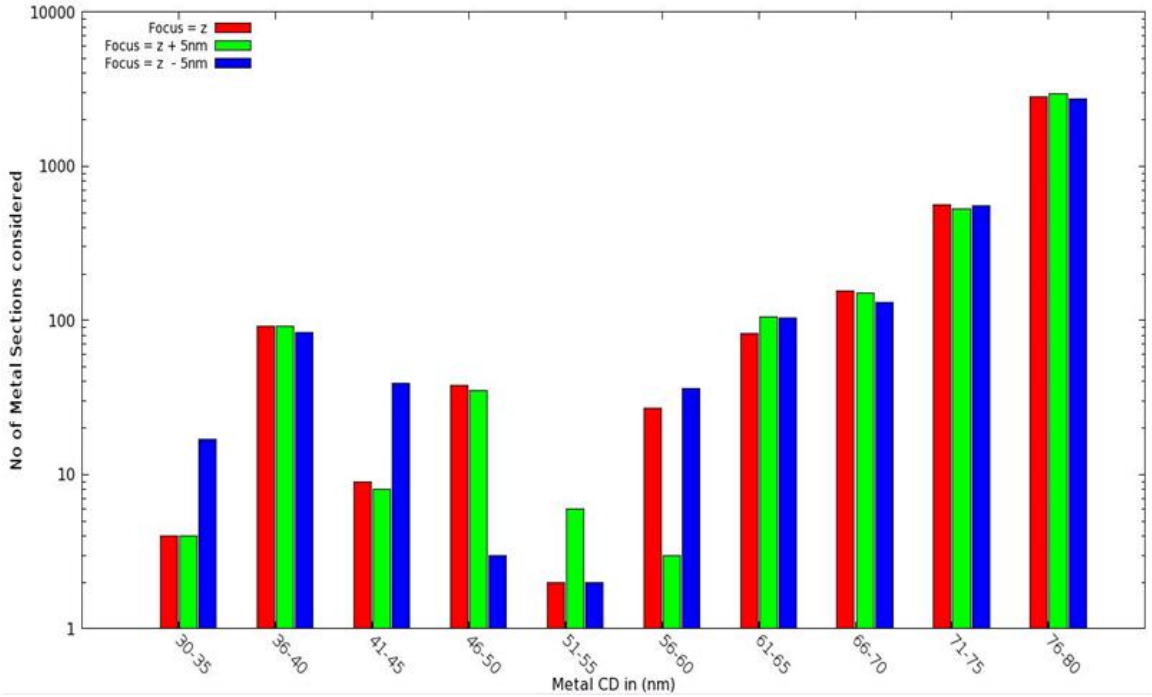

Figure 7.5. Histogram plot of metal CD at various focii

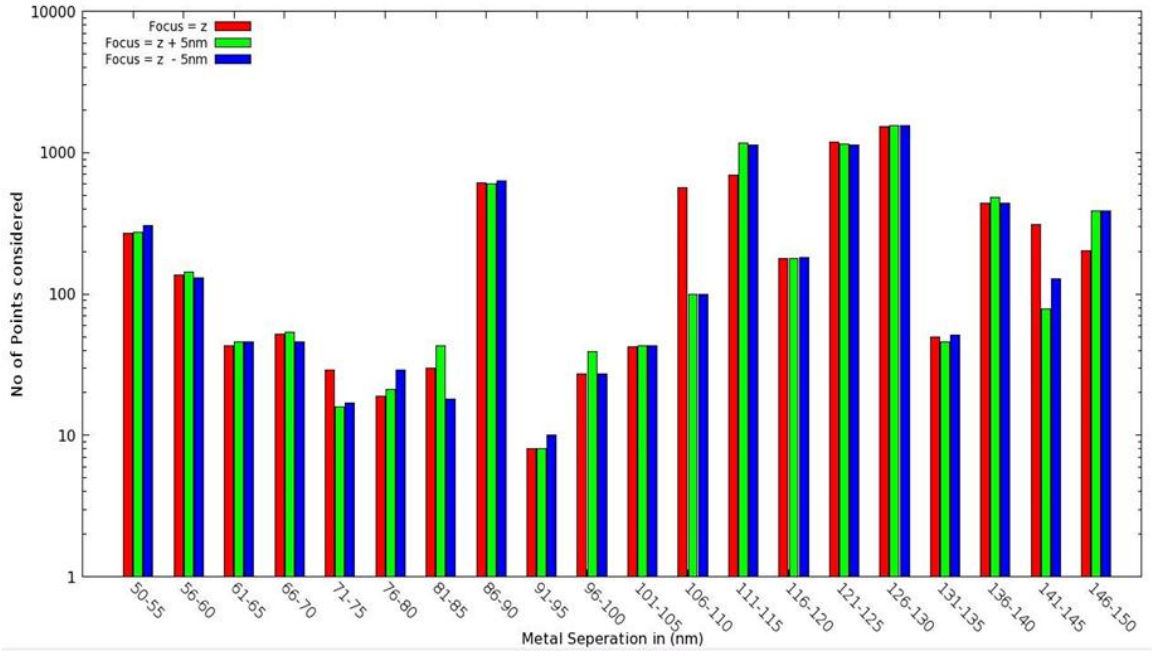

Figure 7.6. Histogram plot of metal seperation at various focii

Table 7.3. Simulation results for metal layer 2 of ISCAS-85

Circuit	Polygons	Moves	Stitches	Run time (h:m:s)
C432	338	119	2	9m14s
C499	541	189	2	27m6s
C880	600	215	3	35m32s
C1355	525	195	3	29m45s
C1908	558	228	4	33m13s
C2670	932	344	4	2h5m40s
C3540	1911	764	19	7h23m35s
C5315	2234	825	29	9h15m20s
C7552	2347	923	26	9h39m40s

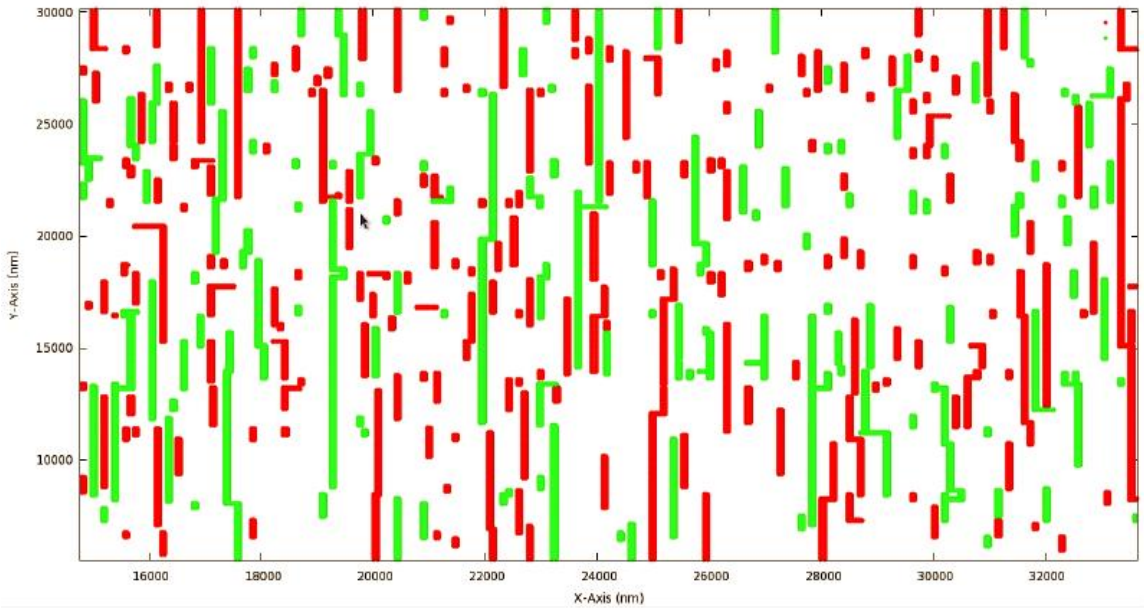

Figure 7.7. A section of ISCAS-85 C880 metal layer 2 post DPL

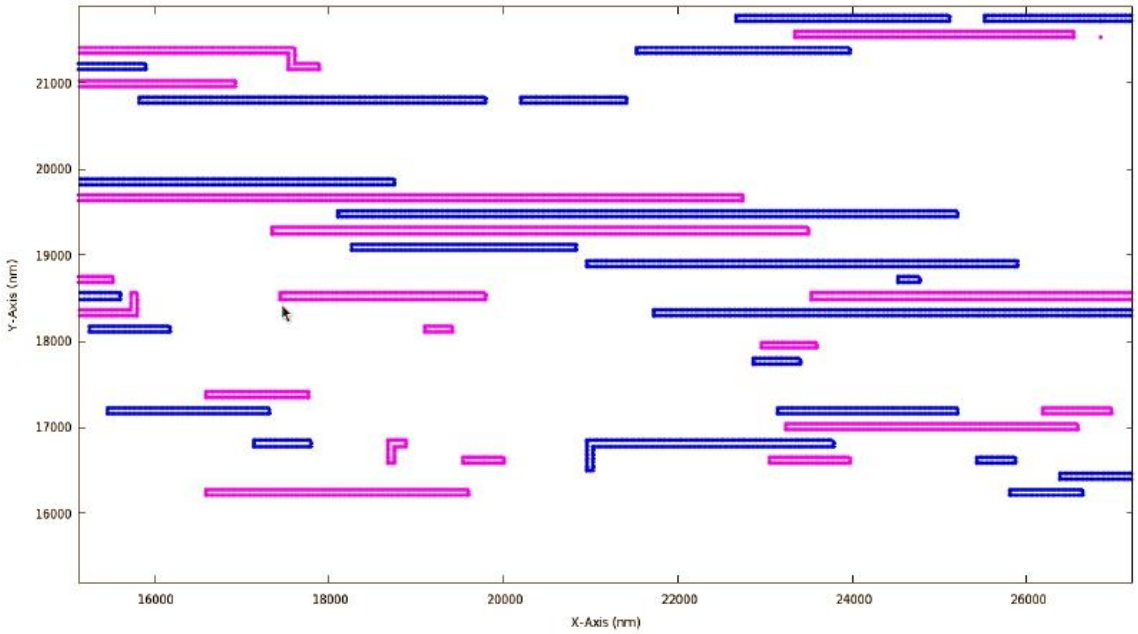

Figure 7.8. A section of ISCAS-85 C432 metal layer 3 post DPL

CHAPTER 8

FUTURE WORK

We will look forward to extend the use of our fast simulator to perform OPC. As OPC needs a number of lithography simulations, our fast simulator will prove to be a huge gain. The DPL algorithm works using a greedy approach. We plan to extend it using other approaches and then compare the results from the two methods. Stitching is a costly process causing yield issues. We plan to find such stitch locations and do an on the fly OPC to avoid the need for stitching thus incorporating OPC into DPL which would be interesting. The use or divide and conquer methodology may reduce the simulation runtime by an order of magnitude. Along with that, we plan to incorporate layout partitioning into independent sections to reduce runtime further.

CHAPTER 9

CONCLUSIONS

We have investigated a new method to perform optical lithography simulation using wavelet transform. By incorporating the focus variation model, the robustness of physical design under process variation is verified. Such verification would not have been possible without large speed-up of simulator that we have achieved. Another clear benefit of this approach is in improved capacity where the proposed method can run on much larger circuits where commercial software fails. Based on partitioning techniques we have developed, the proposed method works on arbitrarily large GDSII layout files. The DPL implementation shows that DPL by running lithography simulation as opposed to using a distance metric is a better choice in order to make use of the disadvantages of sub-wavelength lithography as a gain.

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