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Phase Synthesis Using Coupled Phase-Locked Loops

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PHASE SYNTHESIS USING COUPLED PHASE-LOCKED LOOPS

A Thesis Presented

by

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To my Parents and Grandparents

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This work is a satisfying conclusion to my graduate student life at UMASS, Amherst. It has helped me broaden my perspective both in academia and life in general.

I have been fortunate enough to have an advisor like Dr Omid Oliaei during my research work. I feel I have learnt the meaning of the word "research" under his guidance. I am grateful to him for his understanding and patience as a teacher.

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ABSTRACT

PHASE SYNTHESIS USING COUPLED PHASE-LOCKED LOOPS

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Phase Synthesis is a fundamental operation in Smart Antennas and other Phased Array systems based on beamforming. There are increasing commercial applications for Integrated Phased Arrays due to their low cost, size and power and also because the RF and digital signal processing can be performed on the same chip. These low cost beamforming applications have augmented interest in Coupled Phase Locked Loop (CPLL) systems for Phase Synthesis.

Previous work on the implementation of Phase Synthesis systems using Coupled PLLs for low cost beamforming had the constraint of a limited phase range of ±90°. The idea behind the thesis is that this phase synthesis range can be increased to ±180° through the use of PLLs employing Phase Frequency Detectors(PFDs), which is a significant improvement over conventional coupled-PLL systems.

This work presents the detailed design and measurement results for a phase synthesizer using Coupled PLLs for achieving phase shift in the range of ±180°. Several Coupled PLL architectures are investigated and their advantages and limitations are evaluated in terms of frequency controllability, phase difference synthesis control and

phase noise of the systems. A two-PLL system implementation using off the shelf components is presented, which generates a steady-state phase difference in the range ±180° using an adjustable DC control current. This is the proof of concept for doing an IC design for a Coupled Phase Locked Loop system. Commercial applications in the Wireless Medical Telemetry Service (WMTS) band motivate the design of a CPLL system in the 608-614 MHz band. The design methodology is presented which shows the flowchart of the IC design process from the system design specifications to the transistor level design. MATLAB simulations are presented to model the system performance quickly. VerilogA modeling of the CPLL system is performed followed by the IC design of the system and each block is simulated under different process and temperature corners. The transistor level design is then evaluated for its performance in terms of phase difference synthesis and phase noise and compared with the initial MATLAB analysis and improved iteratively. The CPLL system is implemented in IBM 130nm CMOS process and consumes 40mW of power from a 1.2V supply with a phase noise performance of -88 dBc/Hz for 177° phase generation.

TABLE OF CONTENTS

Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

CHAPTER 1

INTRODUCTION

1.1 CPLL Systems Literature Survey

Recently, agile beamforming technology has been finding an increasing number of commercial applications. Phase-shifting is a fundamental operation in any smart-antenna or phased-array system based on beamforming [1]. Coupled-oscillators or coupled-PLLs using analog multipliers have been proposed in the past to realize the phase-shifting operation without the need for phase shifters [1]-[6]. The coupled-PLLs approach offers the advantage of being insensitive to the output of the voltage controlled oscillator (VCO) and also providing better immunity to noise and larger lock range compared to coupled-oscillators [1]-[3]. In these systems, the array provides periodic signals with an adjustable phase progression to excite the elements of the phased-array. It is noted that the coupled-PLLs architecture is fundamentally different from the cascaded-PLL structures [7]. The coupled-PLLs system provides a better phase noise performance than the cascaded-PLLs structure, where phase noise tends to accumulate at each node, whereas the close-in phase noise of a coupled-PLL system with N elements is 1/N that of a single VCO [8]. Phased-array applications need ±180° phase shift between adjacent elements to achieve 90° beam steering from the broadside [3]. Arrays of coupled-oscillators or coupled-PLLs using analog multipliers are able to generate a variable phase progression limited to ±90°. Here, we show that utilizing phase-frequency detectors (PFDs) in a coupled-PLLs system allows for self-synchronization and also makes it possible to achieve ±180° phase shift. In addition,

using charge pumps provides better immunity to power supply variations, compared to a PLL with just PFD. It also obviates the need for active filters.

1.2 Outline of Thesis

This thesis is organized as follows:

In chapter 2, we provide an overview of the injection locking mechanism in oscillators. We present the mathematical reasons behind the phase synthesis range being constrained to ±90°. We propose two CPLL architectures to increase the phase synthesis range to ±180° and discuss the application areas for each.

In chapter 3, we present the previous work done in the area of phase synthesis using coupled oscillators and PLLs. We present the evolution of the proposed coupled PLLs system, after iterations with different PLL designs and understanding their limitations. We also show MATLAB simulations and analysis confirming the theoretical observations.

Chapter 4 shows the implementation results with a simple board design using off-the-shelf components which provides a proof of concept.

In chapter 5, we present the IC design methodology for the CPLL system. We also show the CPLL system specifications and the corresponding MATLAB simulation results.

In chapter 6, we present the IC design for each block for the CPLL system and also the VerilogA modeling of the system.We present simulation results for each block design at different process and temperature corners.

In Chapter 7, we present a conclusion of the present work and propose future work that can be carried out in this area.

CHAPTER 2

PHASE SYNTHESIS OVERVIEW AND APPLICATIONS

2.1 Injection Locking

Injection locking is a known mechanism through which one oscillator is phase-locked to an injected input signal. Adler's equation describes the dynamics of phase locking in a two-oscillator system as [9]

$$\frac{d\theta}{dt} = \omega_0 - \omega_{inj} - K\omega_0 \sin(\theta) \tag{1}$$

where θ is the phase difference between two oscillators, ω_{inj} the injection frequency, ω_o the free-running frequency of the enslaved oscillator and K is a constant. At steady state, the enslaved oscillator is phased-locked to the injected signal such that the two oscillators oscillate at the same frequency with a constant phase difference θ. The phase difference θ is obtained by setting $d\theta/dt = 0$ in (1)

$$\theta = \sin^{-1}\left(\frac{\omega_{inj} - \omega_0}{K\omega_0}\right) \tag{2}$$

So the steady state phase offset can be controlled by controlling (ω_{inj}-ω_o). Adler's equation has been the cornerstone of the techniques proposed for phase synthesis using coupled-oscillators or coupled-PLLs [1]. In both systems, a chain of oscillators or PLLs is formed through bidirectional coupling of adjacent oscillators or PLLs. A schematic of a bidirectional coupled-PLLs system and a bidirectional coupled oscillators system is shown in Figure 1 [1] and Figure 2 [1] respectively.

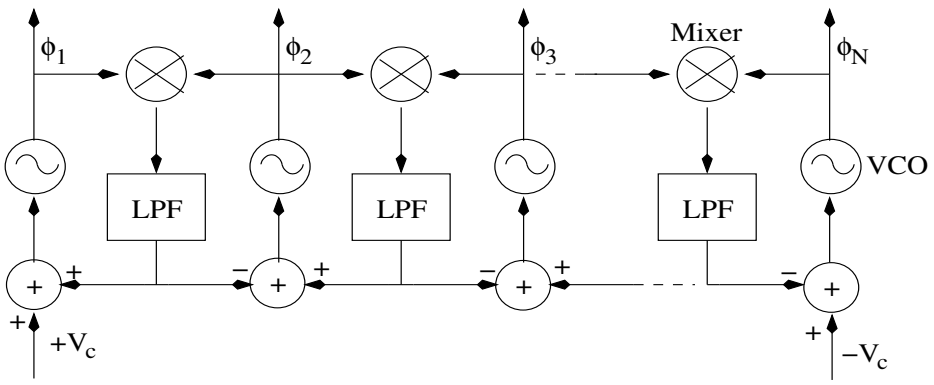

Figure 1: N-PLL system using bidirectional coupled PLLs

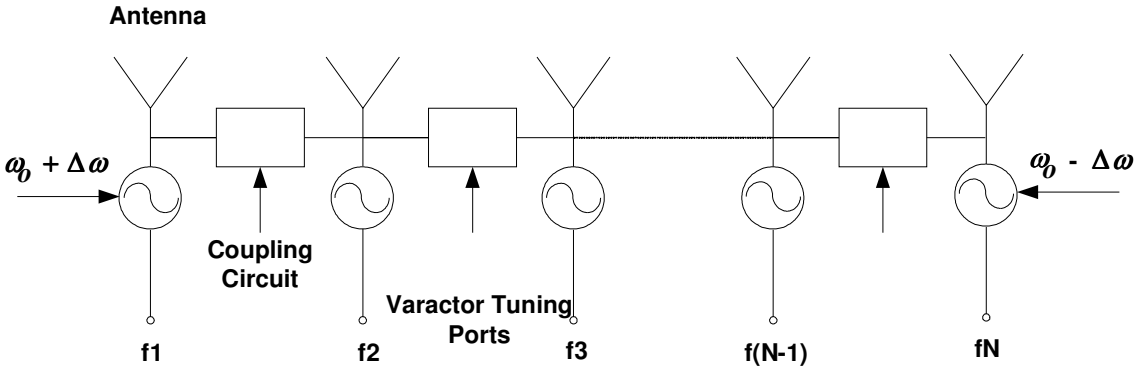

Figure 2 : N-Oscillator system using bidirectional coupled Oscillators

Upon phase locking all oscillators or VCOs oscillate at the same frequency ω_o[1]. If the oscillators at the edge of the chain are detuned by +/-$\Delta\omega$, then the phase shift between any two adjacent oscillators or VCOs will be

$$\theta = \sin^{-1}\left(\frac{\Delta\omega}{K\omega_0}\right) \qquad (3)$$

where K is a constant.

The function $\sin^{-1}$ in the above equations takes on values between –90° and +90°. This limits the phase shift between any two adjacent VCOs to the interval (–90°,+90°). This characteristic of $\sin^{-1}$ is a major drawback because it limits θ to ±90°. If the signals from such a system are used to excite the radiating elements of a phased-

array spaced one half wavelength apart, a maximum scanning beam angle of only 30° can be achieved [3]. A scanning angle of 90° requires us to generate phases that can vary in the (–180°,+180°) interval. It is noted that the $\sin^{-1}$ function in the above equations is due to the phase detection mechanism used in these architectures.

In particular, an analog multiplier-based frequency detector is responsible for the $\sin^{-1}$ function [10][11]. The chain of coupled-PLLs system discussed in [1] and [2] is a special case of PLL-neural networks described in [12].

2.2 Applications

Integrated Phase Arrays used for phase synthesis have the advantage of low cost, size, weight, power and complexity. Moreover, RF and digital signal processing can be performed on the same chip. This would find applications in emerging wireless applications. The benefits to wireless communications include increased range/coverage, improved link quality/reliability, increased capacity of wireless network, interference reduction etc.

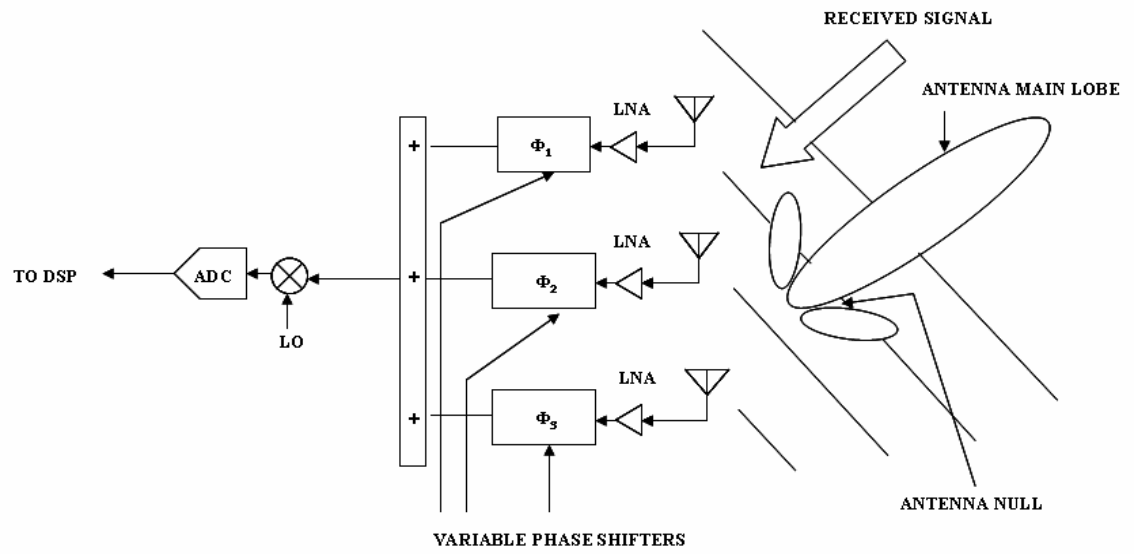

Figure 3: Typical Phased Array Receiver

Figure 3 shows the basic architecture of a typical Phased Array receiver. Beamforming is realized by adjusting the relative phases of the received or transmitted signals. This is usually done by utilizing phase shifters.

This research aims to achieve the phase shifting operation without using phase shifters. The proposed structure (Figure 4) makes use of a PLL-network where each PLL is coupled to its adjacent PLLs. A constant phase shift can be obtained by detuning the end elements of the PLL array in opposite directions. This results in a uniform phase progression from one end of the network to the other. The proposed architecture is based on digital PLLs, allowing for a phase rotation of ± 180° between any two adjacent PLLs.

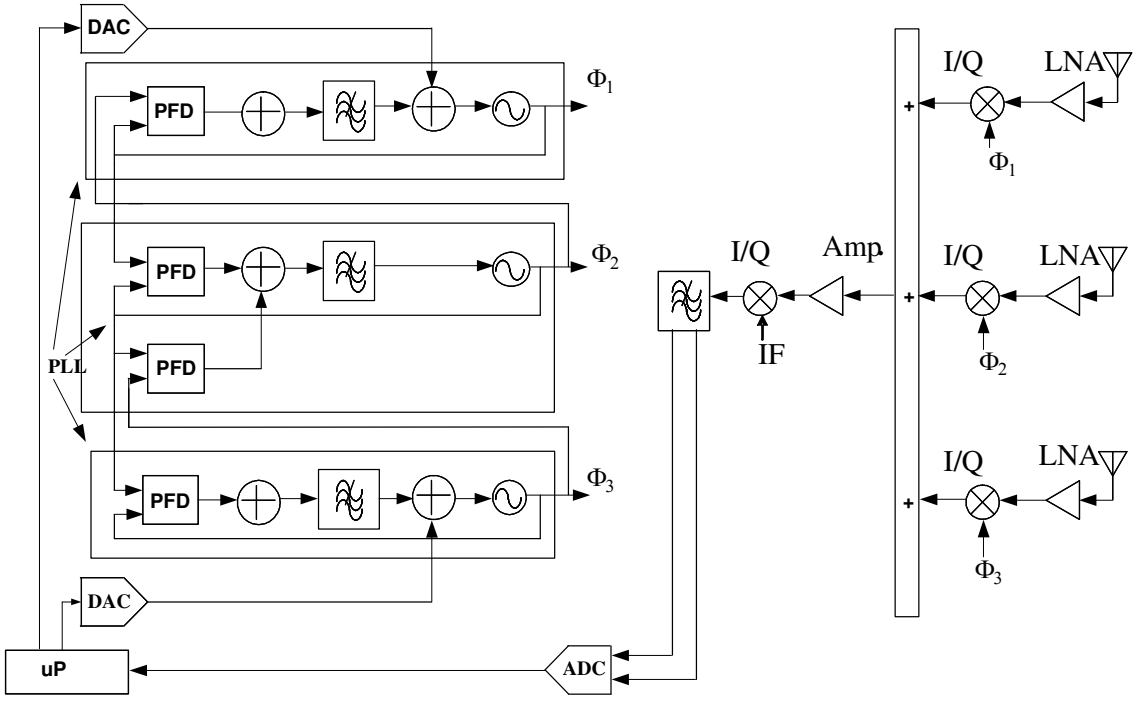

Figure 4: Proposed Receiver Architecture without Phase Shifters

The Phased Array architecture presented in Figure 4 lacks a well defined frequency of operation for phase synthesis. The frequency of operation is determined by the VCO free running frequencies. This architecture is however suitable for radar applications. For communications systems a well defined reference frequency becomes imperative. Hence the above architecture has to be modified with the addition of a reference frequency to be useful in communication system applications. Figure 5 shows the chip architecture overview diagram for the proposed PLL network with two PLLs with a reference frequency for frequency stability. The coupled-PLL VCO output phase differences are controlled using a digitally controlled current source and sink.

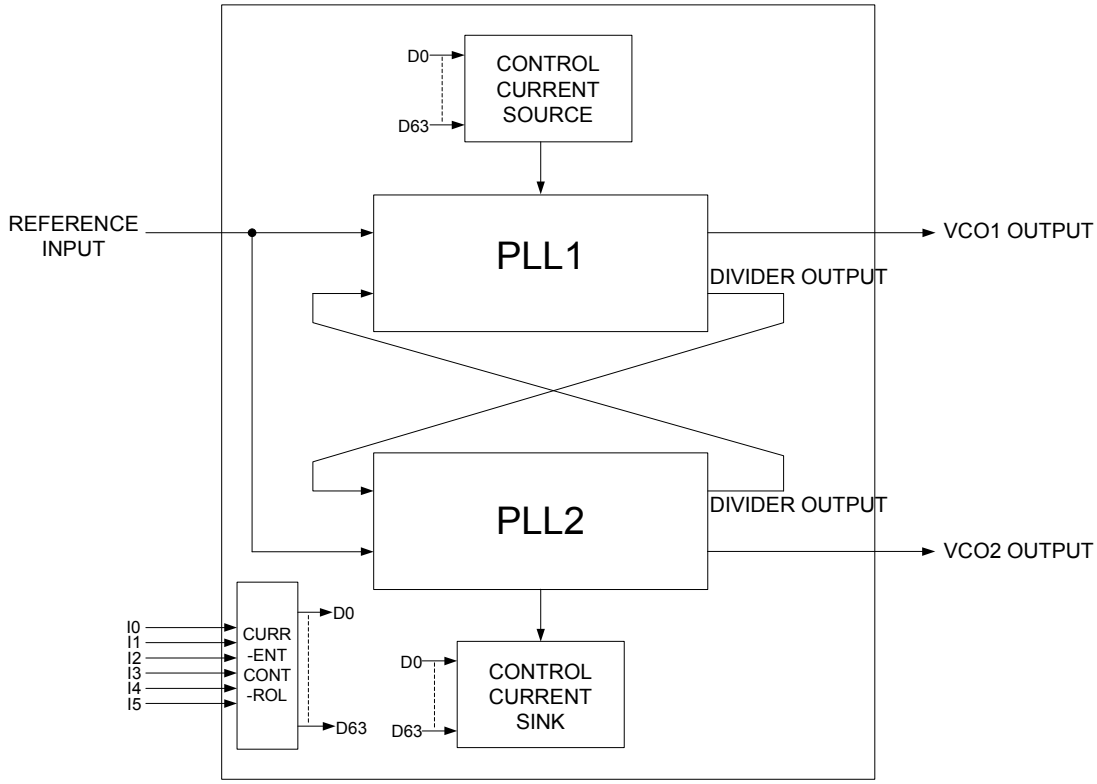

Figure 5: Architectural overview of the proposed CPLL chip implementation

2.2 Summary

This chapter presented the concept of Injection Locking which was mathematically formulated in Adler's equation which forms the basis for Phase Synthesis in Coupled PLL and coupled oscillator systems. Previous work was presented in the area of Phase Synthesis using a series of N PLL or N Oscillator chain, and the limitations mentioned. The basic architecture of a Phased Array receiver was presented and the corresponding implementation of Phase Shifters using Coupled PLL systems with and without a reference was shown.

The present implementation of coupled PLL systems for Phase synthesis are able to provide phase difference synthesis only within a range of ±90°. This presents a

serious limitation of such systems in practical applications. The next chapter focuses on techniques to overcome these present limitations of phase synthesis using coupled PLL systems by increasing the range of synthesized phase difference to ±180°.

CHAPTER 3

PHASE GENERATION USING DIGITAL COUPLED PLLS

3.1 Previous Work

Recently, it has been proposed to use phase-frequency detectors in coupled-PLL networks to remedy the limited range of the phases generated by a coupled-PLL system using analog multipliers (see Figure 6) [13]. Phase-frequency detectors are able to detect phase differences between –180° and +180° [10]. The self-synchronization dynamics of coupled-PLLs system with PFDs is not described by Adler's equations, however they can be explained on the basis of the Synchronization Theorem [12][13].

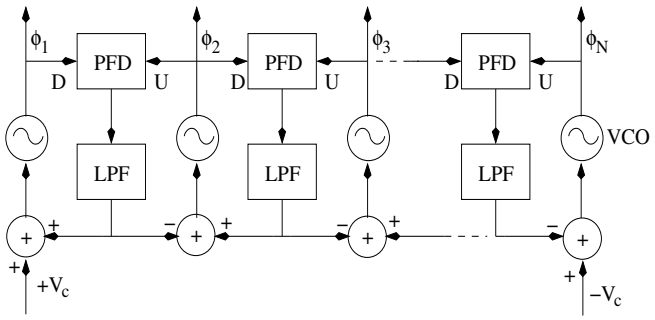

Figure 6: N-PLL system using phase-frequency detectors

An overview of the theorem is presented below using an N PLL system where each PLL is connected to each of the other PLLs through a network of gain matrix, as shown in Figure 7.

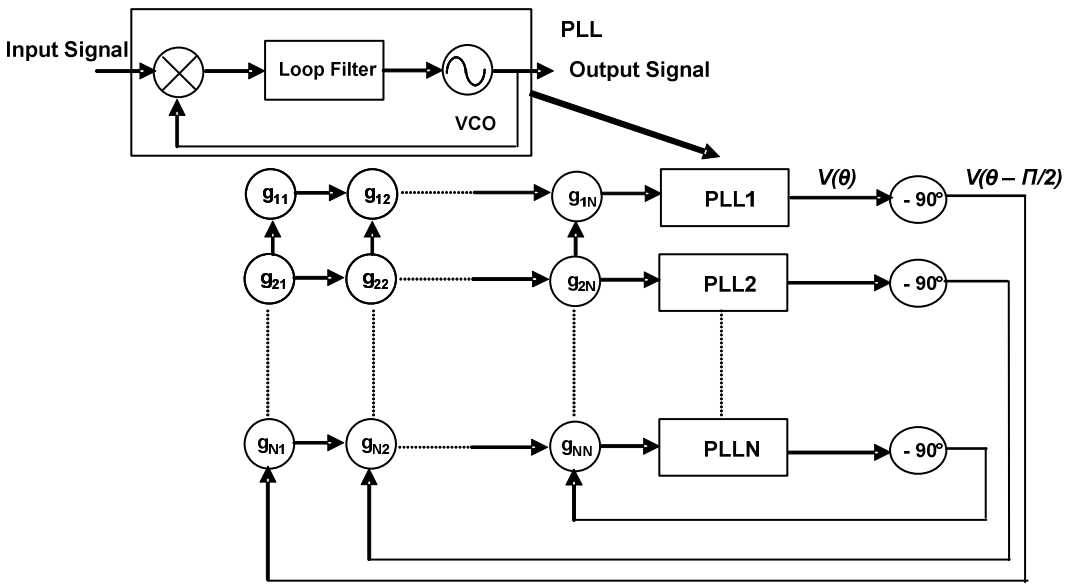

Figure 7: Generalized Coupled-PLL network

The Synchronization Theorem states that the PLL Network converges to a steady state frequency if :

a) the gain matrix are symmetrical,

$$g_{ij} = g_{ji} \quad \text{for all } i \text{ and } j \tag{4}$$

b) the waveforms V(θ) and V(θ-π/2) satisfy the following conditions:

- $V(-\theta) = -V(\theta)$: V(θ) is an odd function (5)
- $V(-\theta - \frac{\pi}{2}) = -V(\theta - \frac{\pi}{2})$: V(θ-π/2) is an even function (6)

It is possible to extend the above result to PLL-networks using phase-frequency detectors and prove their self-synchronization property based on the averaging theory [14]. Upon synchronization, all VCOs oscillate at their free-running frequency with a constant phase progression set by the DC voltage V_c. If the free running frequencies are different, the PLLs still converge to a particular frequency at steady state (which is equal to the average of the free running frequencies). However, in this case the phase relationships will be affected by the free running frequencies [4].

3.1.1 Simulation Results

To verify the above theory, a system of N PLLs was simulated in MATLAB as in Figure 8 with N = 10. The loop filter was designed as a first order passive lead-lag filter with a single pole and a zero. Five PLLs were given a free running frequency of 101Hz and the remaining five a free running frequency of 99 Hz. The transient plot for the PLL frequencies is shown in Figure 8. We observe that the PLLs converge to a steady state frequency of 100 Hz.

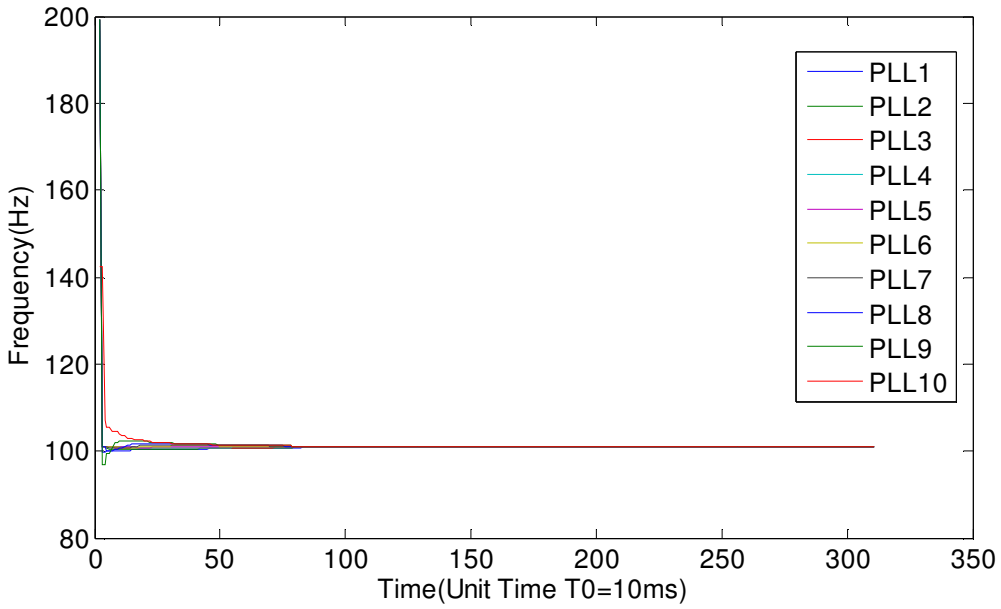

Figure 8: N PLL system frequency convergence plot

Now we keep the free running frequencies of the PLLs at 100 Hz and detune the VCO input voltages of the end elements of the 10-PLL chain by 0.04V. The MATLAB simulation shown in Figure 9 is the transient plot of the phase difference between the adjacent PLLs. We see that the phase difference between adjacent PLLs reaches a steady-state value of 90°. The Phase Difference that can be synthesized can range between +/-180° by tuning the control voltage of the end elements of the PLL chain, thus confirming the theory.

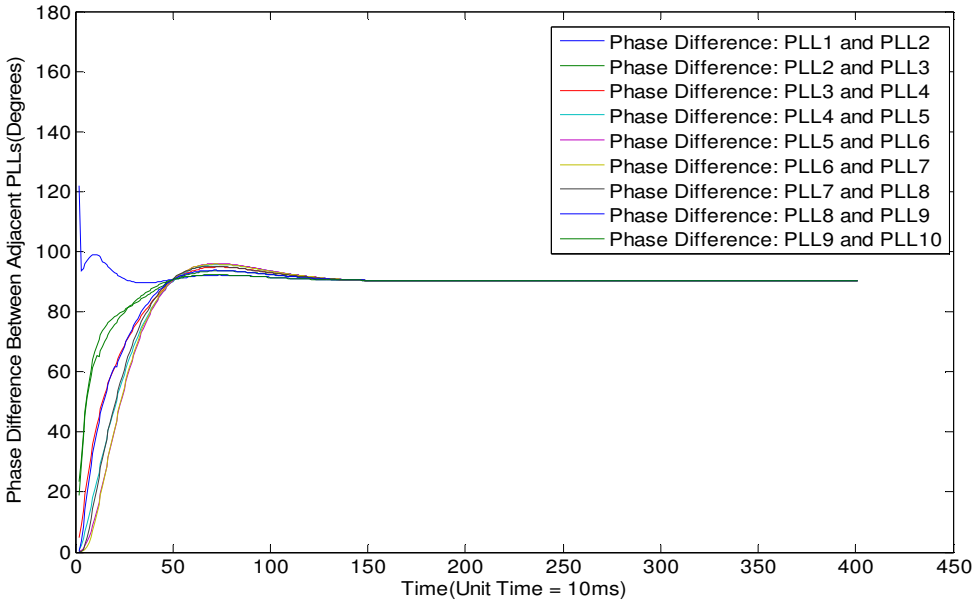

Figure 9: N PLL System Phase Synthesis between adjacent PLLs

3.2 Preliminary Implementation

Here, we consider the special case of a PLL-network comprising two identical PLLs which are symmetrically coupled to each other (see Figure 10).

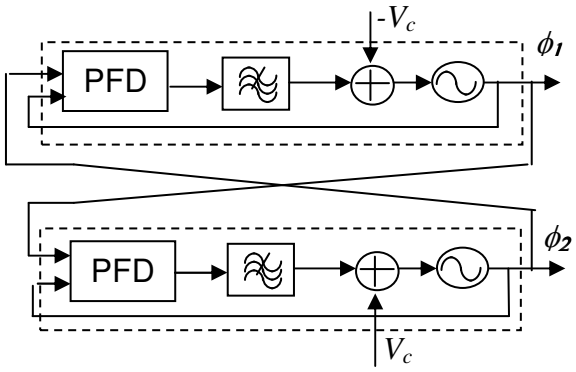

Figure 10: Coupled PLL system using phase-frequency detectors with charge pump(charge pump not shown)

Each PLL includes a DC input for detuning the VCOs in opposite directions using the DC voltages -V_c and V_c. The output current of the phase-frequency detectors(PFDs) with charge pump is proportional to the phase difference at their input.

Noting that the low pass filters remove the high-frequency signal components present at the output of the phase-frequency detectors, the equations of the system can be written as:

$$\begin{cases} \dfrac{d\phi_1(t)}{dt} = K_{v0}\left[K_d\left(\phi_2(t)-\phi_1(t)\right)*F(t)-V_c\right]+\omega_1 \\ \dfrac{d\phi_2(t)}{dt} = K_{v0}\left[K_d\left(\phi_1(t)-\phi_2(t)\right)*F(t)+V_c\right]+\omega_2 \end{cases} \tag{7}$$

where "*" represents the convolution operation, K_{v0} is the frequency sensitivity of the VCO, K_d the PFD gain, $F(t)$ the loop filter impulse response, $\phi_1(t)$ and $\phi_2(t)$ are the output phases of the VCOs and ω_1 and ω_2 are the free running VCO frequencies. Upon synchronization, both PLLs oscillate at the same frequency with a constant phase difference $\theta=\phi_1-\phi_2$. Then, subtracting the two equations and setting $d\theta/dt=0$ results in

$$K_{v0}\left[2K_d\left(\phi_2(t)-\phi_1(t)\right)*F(t)-2V_c\right] = \omega_2-\omega_1 = \Delta\omega \tag{8}$$

$$\text{or, } \left[K_d\theta(t)*F(t)-V_c\right] = \frac{\Delta\omega}{2K_{v0}} \tag{9}$$

Taking the Laplace transform of both sides we obtain,

$$K_d\theta(s)F(s)-\frac{V_c}{s} = \frac{\Delta\omega}{2sK_{v0}} \tag{10}$$

$$\text{or, } \quad s\theta(s) = \frac{\Delta\omega+2K_{v0}V_c}{2K_{v0}F(s)K_D} \tag{11}$$

Using the Final Value Theorem[10],

$$\theta(t\to\infty) = \lim_{s\to 0} s\theta(s) = \lim_{s\to 0}\frac{\Delta\omega+2K_{v0}V_c}{2K_{v0}F(s)K_D} = \frac{\Delta\omega+2K_{v0}V_c}{2K_{v0}F(0)K_D} \tag{12}$$

If the VCOs have the same free running frequencies, $\Delta\omega = 0$, and we get,

$$\theta = \frac{V_c}{K_d F(0)} \quad : -\pi \le \theta \le \pi \tag{13}$$

Thus there exists a linear relation between the phase difference θ and the amount of frequency detuning, or equivalently the DC voltage V_c. In addition to the wider angle range, this linear relationship makes this system more suitable for practical applications. Another advantage is the fact that that the frequency of the interconnection paths can be reduced by using frequency dividers in the feedback path of the PLLs [14].

Conventional loop filter design for a charge pump PLL involves designing the filter with infinite DC impedance to obtain minimum steady-state phase between input and output [10]. On the contrary, the objective of the present loop filter design is to generate phase offsets between the PLL outputs which can be tuned by controlling the free running VCO frequencies. The charge pump delivers a current of $+I_p$ when the PFD output is UP and a current of $-I_p$ when the PFD output is DOWN. This current is converted by the loop filter to a voltage to control the VCO frequency. The open loop transfer function for each PLL in the CPLL system is

$$T(s) = K_{V0} I_p Z(s) /(2\pi s) \tag{14}$$

where $Z(s)$ is a the loop filter impedance

Typically there are two poles at the origin in the open loop transfer function, one contributed by the VCO and the other contributed by the loop filter. In the present design the loop filter has two poles, so the system is third order. The first pole of the filter impedance is set at a non-zero value to avoid infinite DC impedance and thus produce a non-zero phase offset. The second pole in the loop filter reduces the high-frequency ripple at the VCO input which may cause undesired modulation of the VCO

output frequency. The zero is introduced to provide adequate phase margin in the open loop transfer function. Hence the selected driving-point impedance has the following form:

$$Z(s) = \frac{s + w_z}{C_2(s + w_{p1})(s + w_{p2})} \tag{15}$$

The choice of the poles ω_{p1} and ω_{p2} and the zero ω_z of the filter are based upon a trade-off between stability, noise suppression and lock time of the coupled PLLs system. The circuit implementation of the driving-point impedance using passive components is depicted in Figure 11. R_1 and R_2 create a path from the output of the charge pump to ground, which results in a finite DC gain for the loop filter. C_2 prevents any fast frequency variation of the VCOs.

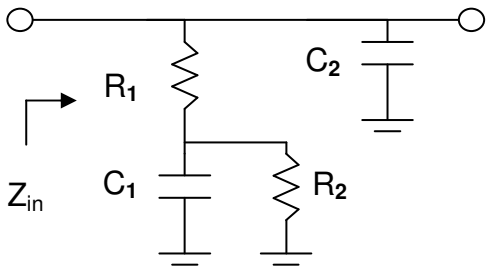

Figure 11: Loop Filter Schematic

3.2.1 Simulation Results

A 25 MHz coupled-PLL network has been designed to verify the theory and also get an insight into IC design. The VCO sensitivity is K_{v0}=40 MHz/V, the phase detector gain is $K_d = I_p/2\pi$ and the charge pump output current is I_p=2mA. The noise bandwidth is chosen to be less than 1/20 of the center frequency [10]. For second or higher order

loops with a high gain with damping factor ξ=0.707 the relation between the transition frequency ω_t and the 3dB frequency ω_{3dB} is $\omega_t \approx \omega_{3dB}/1.33$ [10]. The transition frequency for the open loop transfer function, $T(s)$, is chosen as $\omega_t = 2.013*10^6$ rad/sec such that it will be less than $0.05*\omega_c/1.33$. The pole ω_{p2} and zero ω_z are calculated from the transition frequency by ensuring sufficient ripple suppression and enough phase margin, which is taken as 60^o in the present design. The design equations yield the following values for the loop time constants: $\omega_{p2} = 5.905*10^7$ rad/sec and $\omega_z = 1.181*10^6$ rad/sec. The pole ω_{p1} is placed at $\omega_{p1} = 1.0*10^5$ rad/sec to obtain unity open loop gain at the transition frequency. The values of the components can be related to the zeros and poles of the system as:

$$\omega_z = \frac{R_1 + R_2}{C_1 R_1 R_2} \tag{16}$$

$$\omega_{p1}\omega_{p2} = \frac{1}{C_1 C_2 R_1 R_2} \tag{17}$$

$$\omega_{p1} + \omega_{p2} = \frac{1}{C_1 R_2} + \frac{1}{C_2 R_1} + \frac{1}{C_1 R_1} \tag{18}$$

The coupled PLL system is required to generate a phase of $\theta = \pi$ rad for a frequency offset of Δf = 8 MHz. The given specifications are used in equations (13), (16), (17) and (18) to obtain the values of the components: $R_1 = 8.62\Omega$, $R_2 = 91.3\Omega$, $C_1 = 10.043\ \mu F$ and $C_2 = 2$ nF. The designed coupled-PLLs system has been simulated using the SimPower toolbox in MATLAB. Figure 12 shows the frequency transient of the two PLLs with initial offset frequency of $\Delta f = 8$ MHz and random initial phase offsets. It is seen that the two PLLs become frequency-locked by converging to the steady state frequency of 25 MHz. Figure 13 shows the phase transients for various frequency

detuning values of 300 KHz, 4 MHz and 8 MHz. It appears that the phase transient is smoother for smaller frequency detuning. This observation illustrates that the lock time should be a function of initial detuning.

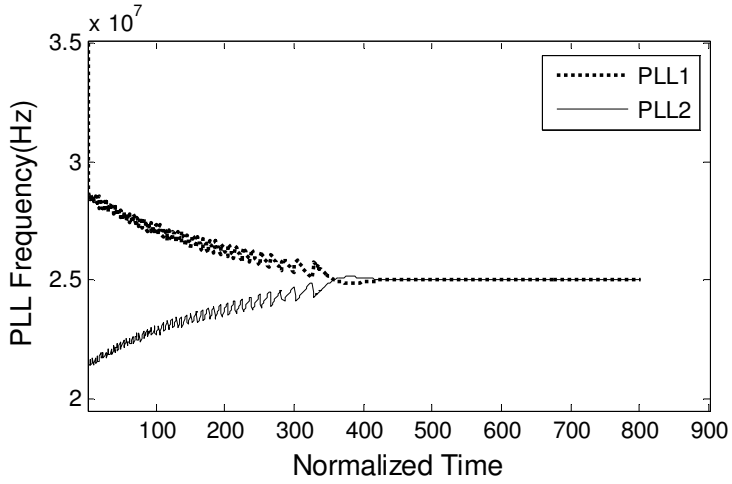

Figure 12: Frequency Convergence for a 2 PLL system for Free Running Frequency Offset of 8 MHz between the PLLs

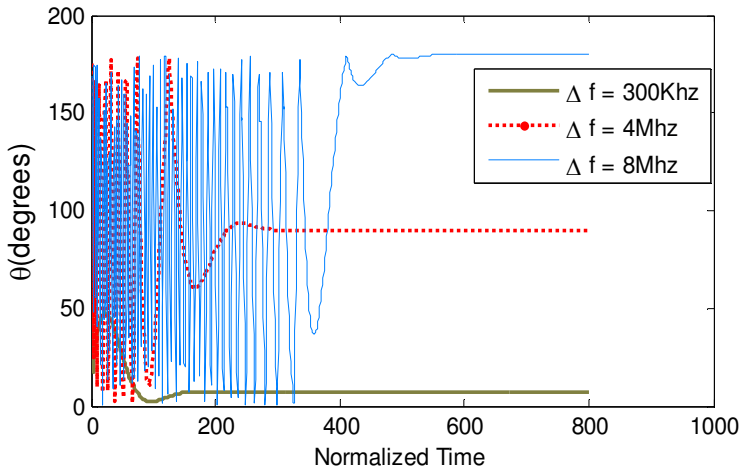

Figure 13: Phase Difference Plots for different Free Running Frequency Offsets between the PLLs

3.3 Phase Synthesizers based on Phase-Frequency Detectors

Now we consider a practical version of the PLL-network in Figure 10 comprising two identical PLLs symmetrically coupled to each other (see Figure 14).

Each PLL includes a DC current input $-I_k$ and I_k for detuning the VCOs in opposite directions. These current sources serve to adjust the phase difference between the two PLLs. In practice, these current sources can be low-speed current-mode digital-to-analog converters (DACs) for digital phase synthesis. Using charge pumps in the structure in Figure 14 facilitates phase adjustment compared with Figure 10, since the DC currents $\pm I_k$ can be easily injected into the circuit without need for an adder, an improvement over the voltage controlled version. Also the loop filter can include a pole at the origin, which is inherently contributed by the charge pump.

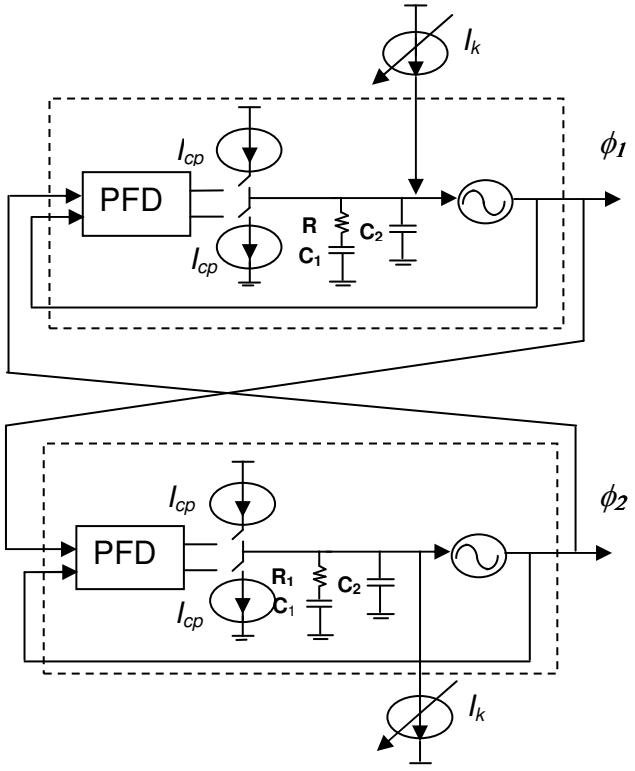

Figure 14: Proposed Coupled PLL system

These modifications make the structure much more amenable to integration. The output of the phase-frequency detectors is a square-wave signal whose duty-cycle is proportional to the phase difference at their inputs. The low pass filters remove the high-frequency signal components of the phase-frequency detector outputs and generate a

nearly DC signal proportional to phase difference between the inputs of the PFDs. Hence the equations of the system can be written as:

$$\begin{cases} \dfrac{d\phi_1(t)}{dt} = K_{v0} Z_F(t) * \left[K_d \left(\phi_2(t) - \phi_1(t) \right) + I_K \right] + \omega_0 \\ \dfrac{d\phi_2(t)}{dt} = K_{v0} Z_F(t) * \left[K_d \left(\phi_1(t) - \phi_2(t) \right) - I_K \right] + \omega_0 \end{cases} \tag{19}$$

where "*" represents the convolution operation, K_d is the PFD gain and $Z_F(t)$ is the impedance of the loop filter. The gain of the PFD is $K_d = I_{cp}/2\pi$, where I_{cp} represents the charge pump current. Upon synchronization, both PLLs oscillate at the same frequency with a constant phase difference $\theta = \varphi_1 - \varphi_2$. Then, following the same derivation process as in Section 3.2, that is, subtracting the two equations and setting $d\theta/dt = 0$ results in

$$\theta = 2\pi \frac{I_K}{I_{cp}} \quad : -\pi \leq \theta \leq \pi \tag{20}$$

Thus the steady state output phase can be varied linearly from –180° to +180° by varying I_k between $-I_{cp}/2$ and $+I_{cp}/2$. The linear dependence of θ on the control current arises from the linearity of the gain of the PFD.

3.3.1 Simulation Results

Behavioral simulations have been performed to evaluate the system performance. Figure 15 shows the frequency transient of the two PLLs with I_k = 1.5 mA and random initial phase offsets.

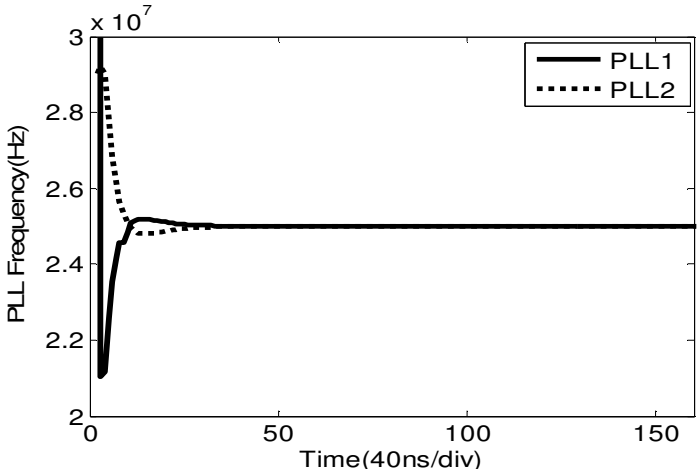

Figure 15: Frequency Convergence Plot for current input I_k = 1.5 mA

It is seen that the two PLLs become frequency-locked by converging to the steady state frequency of 25 MHz. Figure 16 shows phase difference transients for various values of the control current. It is observed that the phase difference(θ) is extended well beyond +/-90°.

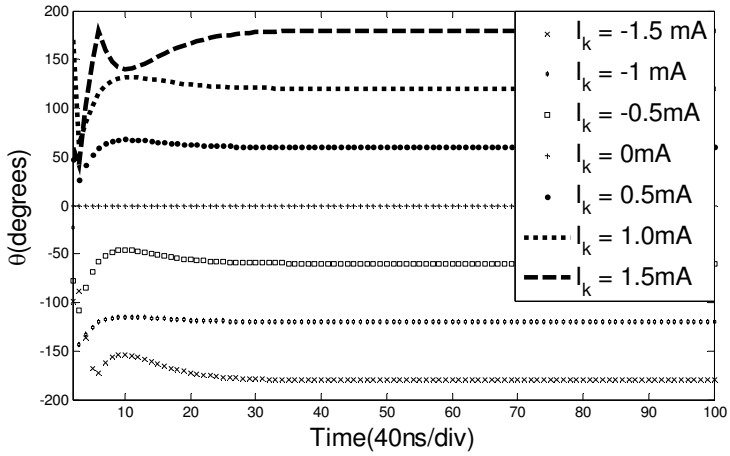

Figure 16: Phase Difference transient plots for different current inputs I_k

3.4 Phase-frequency synthesizer

The frequency of the Phase Synthesizer architecture presented above is not well-controlled because of the absence of any reference signal. Here, we propose a phase-

frequency synthesizer architecture based on CPLL system which is capable of achieving ±180° phase shift while being able to lock to a reference signal for frequency stability. Such a phase-frequency synthesizer finds application in communication systems based on the beamforming technology and also in MIMO receivers [15]. We thus aim to enhance the system in Figure 14 to enable accurate phase and frequency synthesis. The proposed phase-frequency synthesizer embedding two PLLs is depicted in Figure 17. The system employs one additional PFD/CP for each PLL to enable frequency controllability. The goal here is to accurately set the output frequency using the reference signal while still being able to vary the phase difference using the control currents $\pm I_k$. We denote the phase of the reference signal by $\varphi_{ref}(t)$, the phase of the first VCO by $\theta_1(t)$, the phase of the second VCO by $\theta_2(t)$, and the free-running frequency of the VCOs by ω_1 and ω_2, respectively.

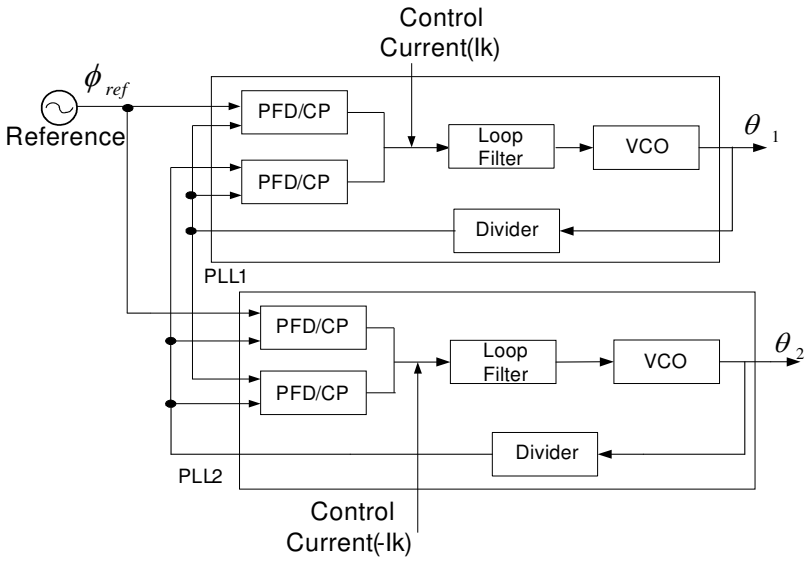

Figure 17: Phase Frequency Synthesizer using Reference and control currents

The dynamics of the system in the time domain is described by the following differential equations:

$$[(\phi_{ref}(t)-\frac{\theta_1(t)}{N})K_d+(\frac{\theta_2(t)}{N}-\frac{\theta_1(t)}{N})K_d-I_k(t)]*Z_f(t)K_v+\omega_1=\frac{d\theta_1(t)}{dt} \quad (21)$$

$$[(\phi_{ref}(t)-\frac{\theta_2(t)}{N})K_d+(\frac{\theta_1(t)}{N}-\frac{\theta_2(t)}{N})K_d+I_k(t)]*Z_f(t)K_v+\omega_2=\frac{d\theta_2(t)}{dt} \quad (22)$$

where '*' denotes convolution operation, N is the divider ratio, K_d (Amperes/rad), the PFD/CP gain, Z_f (Ω), the loop filter impedance and K_v (rad/sec/V) is the VCO sensitivity. Now we assume that the VCOs achieve frequency-lock after sufficiently long time. To obtain the steady-state phase difference $\Delta\theta(t)=\theta_2(t)-\theta_1(t)$, we subtract (21) from (22) and set $d\theta_1(t)/dt = d\theta_2(t)/dt$. So,

$$[3(\frac{\theta_2(t)}{N}-\frac{\theta_1(t)}{N})K_d-2I_k(t)]*Z_f(t)K_v=\omega_2-\omega_1=\Delta\omega \quad (23)$$

Taking the Laplace transform of both sides, we obtain

$$s\Delta\theta(s)=\frac{2NI_k}{3K_d}+\frac{N\Delta\omega}{3K_dK_vZ(s)} \quad (24)$$

Noting that $Z(s)$ is has a pole at DC, i.e., $Z(s)=F(s)/s$, (as is the case in usual Charge Pump PLL loop filter implementations as shown in Figure 14) we find the steady-state phase difference as

$$\Delta\theta(t\to\infty)=\lim_{s\to 0}s\Delta\theta(s)=\lim_{s\to 0}(\frac{2NI_k}{3K_d}+\frac{sN\Delta\omega}{3K_dK_vF(s)})=\frac{2NI_k}{3K_d} \quad (25)$$

Hence the synthesized phase difference is independent of the input reference frequency. Furthermore, it appears that the phase difference is independent of the VCO free-running frequencies, which is due to the infinite DC gain of the loop filters. This

result demonstrates the advantage of the proposed system in terms of phase accuracy. Interestingly, the phase-frequency synthesizer in Figure 17 can be extended to 3 PLLs to generate three signals with a constant phase progression controlled by the currents $\pm I_k$ injected only to the end PLLs. Extensive time-domain simulations were performed to verify that the VCOs always lock to the input frequency despite difference in their free-running frequencies. Figure 18 shows the transient response of the system when the reference frequency is 0.5 Hz and the VCO free running frequencies are 0.95 Hz and 1.03 Hz. Each PLL uses a divide-by-two divider. It is observed that upon synchronization the VCOs oscillate at 1 Hz, which is the reference frequency multiplied by two.

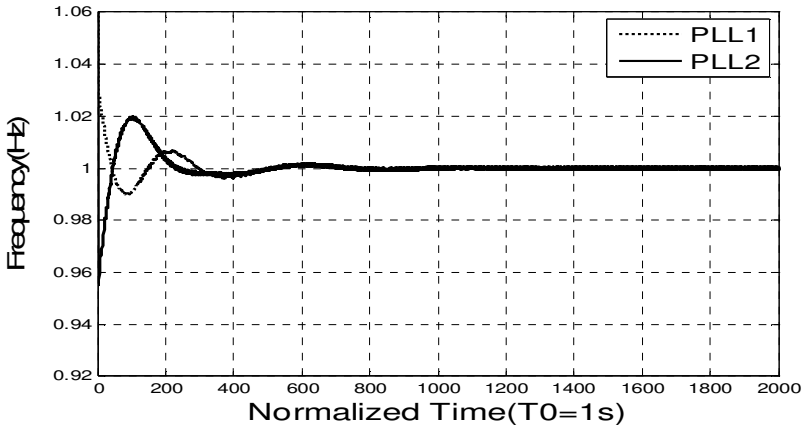

Figure 18: Frequency Convergence for the Phase Frequency Synthesizer

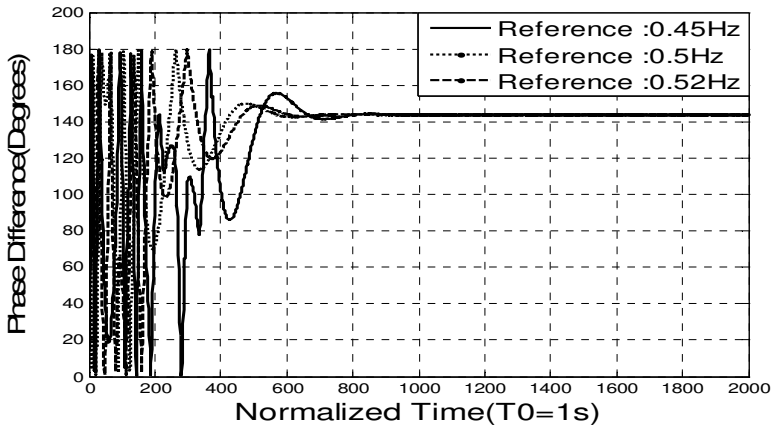

Figure 19: Phase Difference Transient for various values of the input reference frequency

The transient response of the system for a specific phase difference and various values of the input reference frequency are shown in Figure 19. In this simulation we have set f_1 = 0.95 Hz, f_2 = 1.03 Hz, and $I_k = 0.6Ip$ corresponding to a steady-state phase difference of 144°. These simulations confirm the result in (25) indicating that the synthesized phase difference is independent of the reference frequency as well as the free-running frequency of the VCOs.

3.5 Phase Noise Analysis

In this section, we analyze the phase noise performance of the phase synthesizer in Figure 14 and the phase-frequency synthesizer in Figure 17. Then, we extend the results to a system comprising larger number of PLLs. To this end, we first consider the single-PLL system in Figure 20.

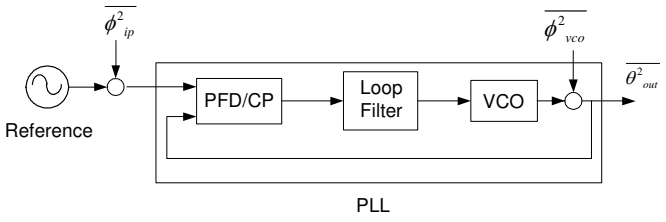

Figure 20: Single PLL with different noise sources

For the sake of simplicity, we have dropped the frequency divider. The phase noise components of the reference, charge pump and loop filter are considered to be uncorrelated and they are lumped into an equivalent input-referred phase noise, $\overline{\phi^2_{ip}}$. The input-referred phase noise sees a low pass transfer function to the PLL output given by:

$$\overline{\theta^2_{out1}} = \left|\frac{G(s)}{1+G(s)}\right|^2 \overline{\phi^2_{ip}} \tag{26}$$

Here *G(s)* is the Open Loop Gain of the system = $K_dK_vZ(s)/s$ where K_d is the PFD/CP gain, K_v is the VCO sensitivity, *Z(s)* is the loop filter impedance and $s = j\omega$. The VCO open loop phase noise $\overline{\phi^2_{vco}}$ undergoes a high pass filtering before reaching the output:

$$\overline{\theta^2_{out2}} = \left|\frac{1}{1+G(s)}\right|^2 \overline{\phi^2_{vco}} \tag{27}$$

3.5.1 Phase Synthesizer(PS)

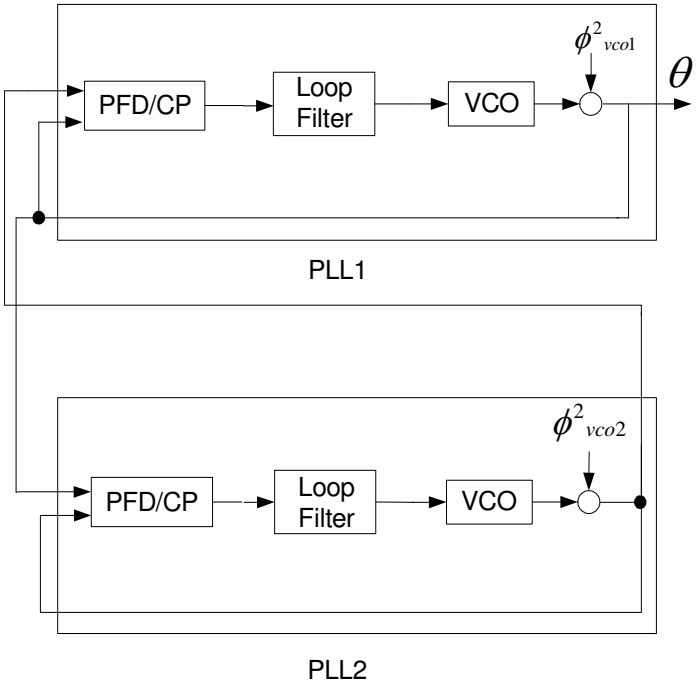

Figure 21: VCO noise sources contribution to the PS output phase noise

To analyze the phase noise of the phase synthesizer in Figure 14, we consider only the contribution of the VCOs to the output phase noise(Figure 21). Denoting the open loop phase noise of the first and second PLL by, respectively, $\overline{\phi^2_{vco1}}$ and $\overline{\phi^2_{vco2}}$, the phase noise at the output of PLL1 due to each VCO will be given by

$$\overline{\theta^2_{out1}} = \left|\frac{1+G(s)}{1+2G(s)}\right|^2 \overline{\phi^2_{vco1}} \tag{28}$$

$$\overline{\theta^2_{out2}} = \left|\frac{G(s)}{1+2G(s)}\right|^2 \overline{\phi^2_{vco2}} \tag{29}$$

The factor two in the denominator of the above equations is due to the presence of two loop filters. Since the VCOs are identical, they generate the same amount of phase noise, i.e., $\overline{\phi^2_{vco1}} = \overline{\phi^2_{vco2}} = \overline{\phi^2_{vco}}$, Thus, the total output phase noise becomes

$$\overline{\theta^2_{out}} = \left\{ \left| \frac{1+G(s)}{1+2G(s)} \right|^2 + \left| \frac{G(s)}{1+2G(s)} \right|^2 \right\} \overline{\phi^2_{vco}} \qquad (30)$$

The phase noise transfer function expressed in the above equation is plotted in Figure 22 and compared with the transfer function given in (27) for a single PLL. It is observed that the VCO phase noise at frequencies far from the carrier frequency is not attenuated but it undergoes some attenuation (3 dB) at frequencies close to the carrier. The near-carrier phase noise is obtained by letting $s \rightarrow 0$ in (30)

$$\overline{\theta^2_{out}} = \frac{1}{2} \overline{\phi^2_{vco}} \qquad (31)$$

So, for a 2-PLL phase synthesizer with no reference the output close-in phase noise due to the VCOs is half the open loop phase noise of each VCO. Further analysis shows that for an N-PLL phase synthesizer the close-in phase noise at the output of each PLL is $1/N^{th}$ of the phase noise of each VCO. This result obtained for a phase synthesizer based on phase-frequency detectors is in agreement with the results in [8] for coupled-PLLs using analog multipliers.

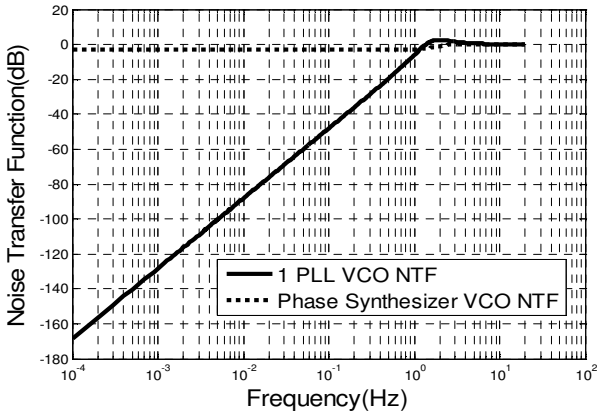

Figure 22: Single PLL and Phase Synthesizer VCO Noise Transfer functions(NTF)

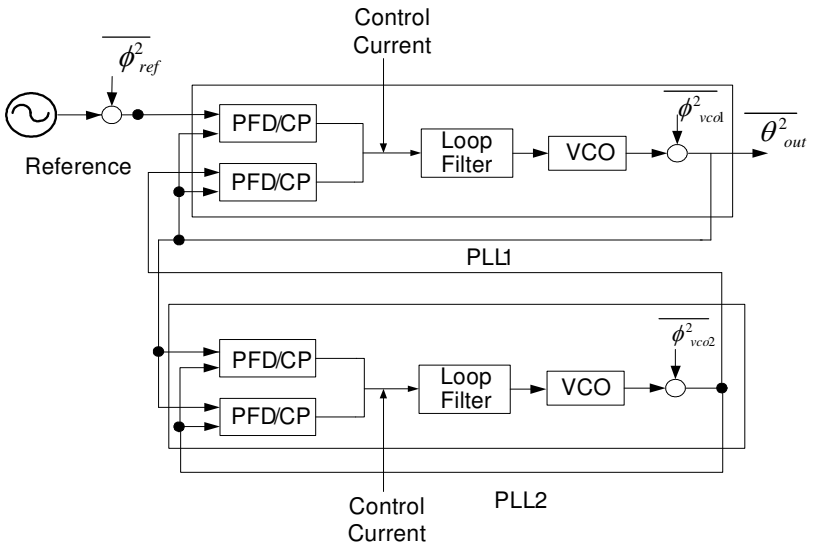

Figure 23: Noise sources contributing to the Phase Frequency Synthesizer output phase noise

3.5.2. Phase-Frequency Synthesizer

For the system in Figure 23 we need to consider the phase noise contributions of the reference and the two VCOs. The reference phase noise $\overline{\phi^2{}_{ref}}$ undergoes a low pass filtering to yield at the output,

$$\overline{\theta^2{}_{out1}} = \left|\frac{G(s)}{1+G(s)}\right|^2 \overline{\phi^2{}_{ref}} \tag{32}$$

where *G(s)* is the open loop gain of the PLL. Comparison with (26) indicates that the reference signal contributes to the same amount of output phase noise compared with a single PLL. The phase noise contribution from the VCOs is given by:

$$\overline{\theta^2{}_{out2}} = \left|\frac{1}{1+G(s)}\frac{1+2G(s)}{1+3G(s)}\right|^2 \overline{\phi^2{}_{vco1}} \tag{33}$$

$$\overline{\theta^2{}_{out3}} = \left|\frac{1}{1+G(s)}\frac{G(s)}{1+3G(s)}\right|^2 \overline{\phi^2{}_{vco2}} \tag{34}$$

where the open loop phase noise of the first and second PLL are denoted by $\overline{\phi^2_{vco1}}$ and $\overline{\phi^2_{vco2}}$ .Once again since the open loop VCO phase noise are the same, $\overline{\phi^2_{vco1}} = \overline{\phi^2_{vco2}} = \overline{\phi^2_{vco}}$, the total output phase noise due to the VCOs is obtained as:

$$\overline{\theta^2_{out}} = \left|\frac{1}{1+G(s)}\right|^2 \left(\left|\frac{G(s)}{1+3G(s)}\right|^2 + \left|\frac{1+2G(s)}{1+3G(s)}\right|^2\right)\overline{\phi^2_{vco}} \qquad (35)$$

The phase noise transfer function in (35) is plotted in Figure 24 and compared with the phase noise transfer function in (27). In a single-PLL system using a charge pump, the VCO phase noise is highly attenuated at frequencies near the carrier frequency due to the presence of a pole at DC. It is observed that this important property is preserved in the 2-PLL phase-frequency synthesizer. Moreover, the phase-frequency synthesizer exhibits 2.6dB additional phase noise attenuation. It is noticed that, as shown in Figure 22, this property was not preserved in the phase synthesizer in Figure 14. Hence in addition to frequency controllability, the phase-frequency synthesizer shows superior close-in phase noise performance compared to the phase-synthesizer. Analysis of a phase-frequency synthesizer comprising three PLLs indicates that the additional phase noise reduction increases to 3.25 dB. We do not observe a phase progression for the Phase Frequency synthesizer for more than 3 PLLs, with the current architecture.

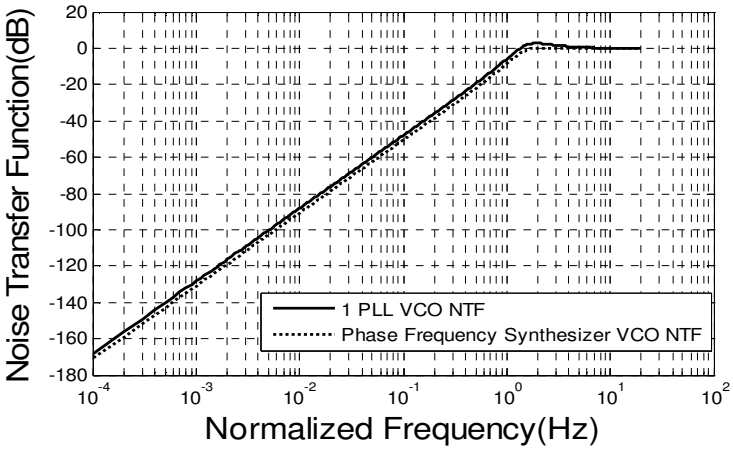

Figure 24: Comparison of VCO Noise Transfer functions (NTF) of a 1 PLL system and a Phase Frequency Synthesizer with 2 PLLs

3.6 Summary

This chapter discussed the N-PLL network design which could be used to increase the range of Phase Difference Synthesized to ±180°. MATLAB simulations for 10 PLL chain demonstrating its frequency convergence and Phase Difference generation properties were presented. The loop filter design for a Coupled PLL system was presented with in which a control voltage provides for generating the Phase Difference. An improved version of the system was presented with the control voltage replaced by a control current and the advantages mentioned. The system was further improved with the addition of a reference frequency for frequency stability. Analytical results and MATLAB simulations for the latter were presented to show that the output phase difference synthesized is independent of the reference frequency and the free running VCO frequencies, unlike the previous architectures. Extensive phase noise analyses were performed on the Phase Synthesizer and the Phase Frequency Synthesizer. Phase

Noise reduction of 3.25 dB was observed for a Phase Frequency Synthesizer comprising three PLLs compared to that of a single PLL.

A quick practical verification of the proposed design is essential before getting involved in the costly process of IC design for the whole CPLL system. This aids in refining the system level design in MATLAB and shows the practical issues, all of which may not be observed in the simulations. To this end, a board design for the Coupled PLL system was done using off-the-shelf components (TLC2932A PLLs[16]) and is presented in the next chapter.

CHAPTER 4

BOARD IMPLEMENTATION RESULTS

4.1 Coupled PLL Implementation with no Divider

The purpose of the implementation has been to demonstrate the self-synchronization phenomenon in the coupled-PLLs network using PFDs and its capability to generate a variable phase using DC inputs. A 25 MHz coupled-PLLs network has been designed using two off-the-shelf TLC2932A PLLs [16] (see Figure 25).

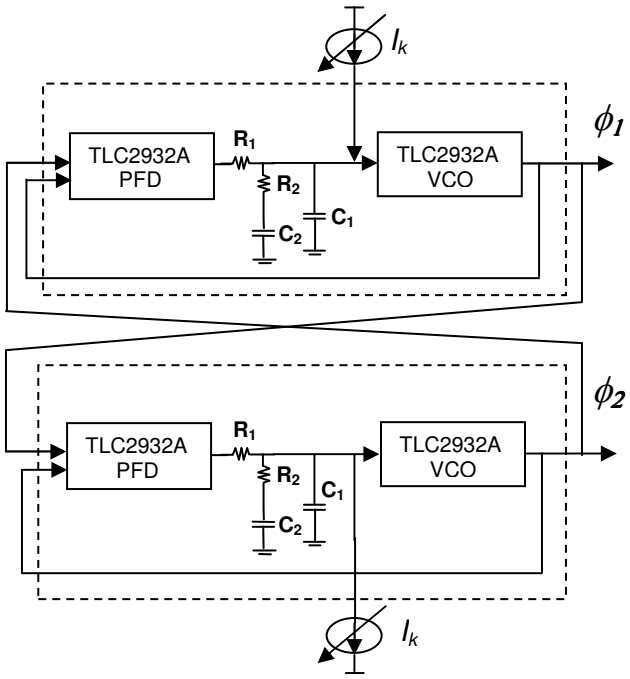

Figure 25: Implemented Coupled PLL system

The loop filter was designed as a second-order passive lead-lag filter. The VCO sensitivity is K_{v0} = 40 MHz/V and the phase detector gain is K_d = 0.1671 V/rad. The system is designed for a natural frequency [10][11][17] $\omega_n = 7.632*10^6$ rad/sec and a damping factor $\xi = 1.0$ for adequate phase margin. The loop filter values chosen were R_1

= 496 Ω, R_2 = 242 Ω, C_1 = 1 nF and C_2 = 68 pF. The steady-state phase difference θ can theoretically be varied linearly over (–180°, 180°) by varying the control current I_k with the following relation:

$$\theta = \frac{R_1 I_K}{K_d} \tag{36}$$

Figure 26 and Figure 27 show the PLL output waveforms having 50° and 160° phase difference, respectively. The measurements were obtained using a Tektronix Digital Storage Oscilloscope. The phase measurement accuracy is +/- 4°.

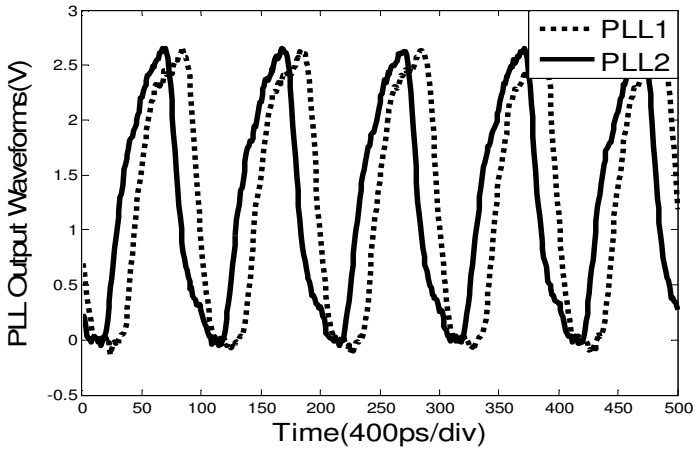

Figure 26: CPLL outputs for steady state phase offset of 50°

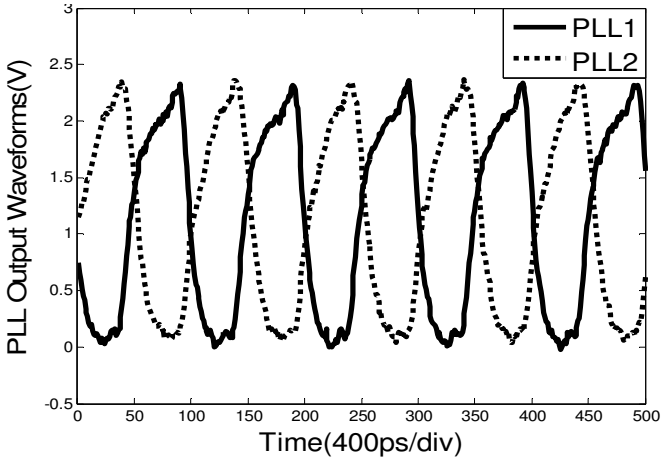

Figure 27: CPLL outputs for steady state phase offset of 160°

Figure 28 shows the average steady-state phase difference as a function of the control current. The average phase difference between the PLL outputs varies between 40° and 220° for control current tuning between 0.6 mA and 1.8 mA. Excessive jitter at low values of phase difference made the measured phase difference versus control current curve inaccurate.

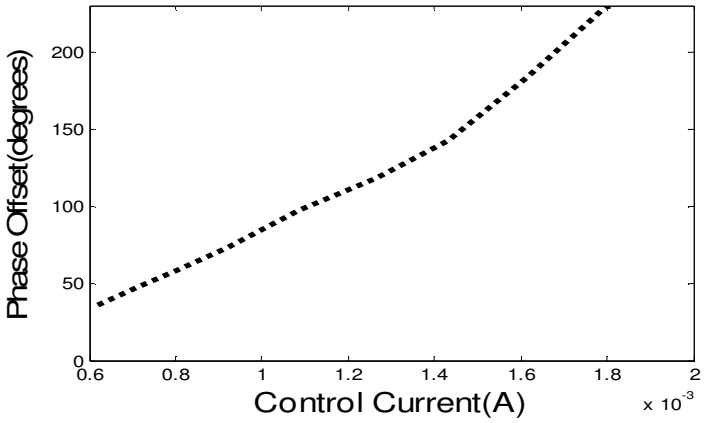

Figure 28: CPLL output phase vs. Control current

Figure 29 shows the transient waveforms at the VCO inputs when the control current is switched at 25 KHz. The waveforms depict the VCO input voltage transitions from the time the PLLs are unlocked to the time they acquire a steady lock frequency of 25 MHz. The PLLs are unlocked when the VCO input voltage is below 0.9 V and locking onto each other at other times.

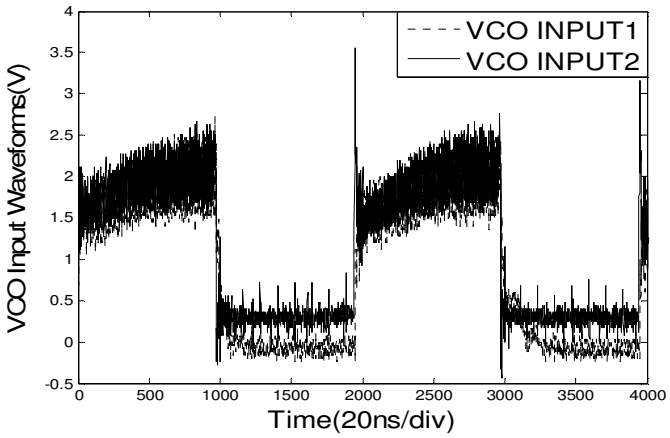

Figure 29: VCO input transients for control current switching at 25kHz

4.2 Coupled PLL Implementation with Divider

The next logical step in the implementation was the addition of frequency dividers in the feedback loop. The frequency dividers reduce the coupling frequency and also the speed requirement of the phase-frequency detectors. These enhancements make the structure suitable for integration in a CMOS or BiCMOS technology. Figure 30 shows the board schematic.

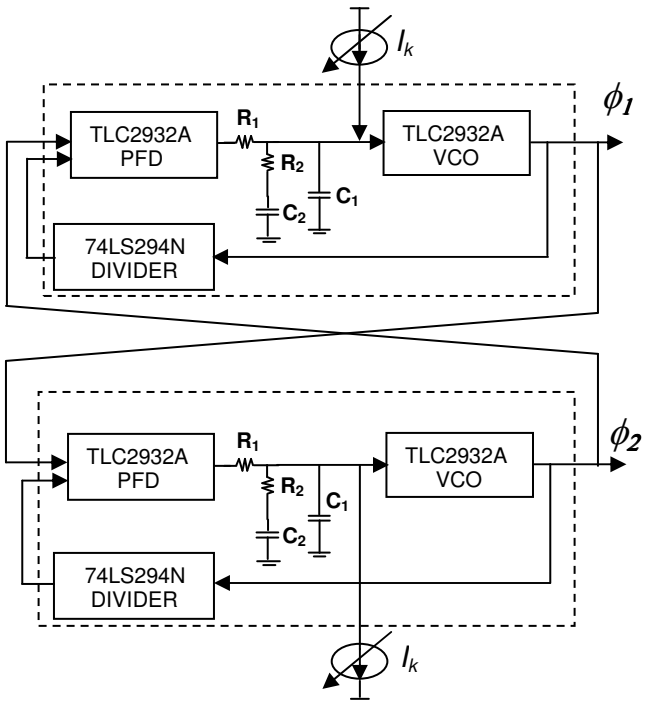

Figure 30: Implemented Coupled PLL system with dividers

The system is designed for a natural frequency $\omega_n = 598.8*10^3$ rad/sec, a divider ratio $N = 8$ and a damping factor $\xi = 1.0$ for adequate phase margin. The loop filter values chosen were $R_1 = 557\ \Omega$, $R_2 = 21\ \Omega$, $C_1 = 1$ uF and $C_2 = 97$ nF. The steady-state phase difference θ, can be varied linearly from –180° to +180° by varying the control current I_k with the following relation:

$$\theta = \frac{R_1 * I_K * N}{K_d} \tag{37}$$

Figure 31 shows the average steady-state phase difference as a function of the control current. The average phase difference between the PLL outputs varies between 20° and 200° for control current tuning between 0.06 mA and 0.23 mA.

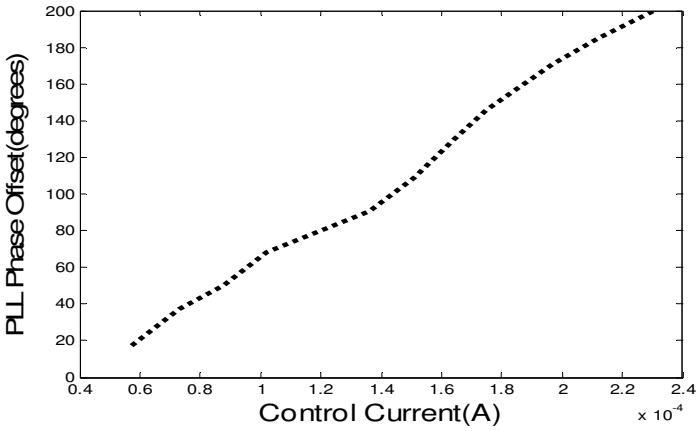

Figure 31: CPLL output phase vs. Control current

Figure 32 shows the transient waveforms at the VCO inputs when the control current is switched at 25 Hz.

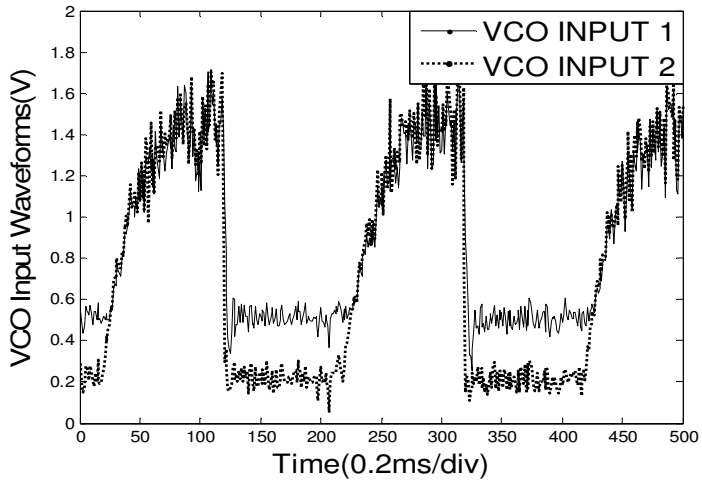

Figure 32: CPLL VCO input transient for control current switching at 25 Hz

The results prove that phase synthesis and synchronization are possible even in the presence of frequency dividers. It is noted that it would not have been possible to use frequency dividers without using PFDs.

4.3 Summary

This chapter demonstrated the implementation of the Coupled PLLs system with two PLLs to verify the theory. The implementation was done using off-the-shelf components available. The first implementation was Coupled PLLs system without dividers and the second implementation was a Coupled PLLs system including dividers. Adding dividers has the advantage of reducing the coupling frequency of the Phase Frequency Detectors.

Having verified the theory of phase difference generation in the range of ±180° using Coupled PLLs system, the next step is the IC design for a Coupled PLLs system with two PLLs. The specification and the design methodology for the same is presented in the next chapter.

CHAPTER 5

CPLL DESIGN METHODOLOGY AND SYSTEM SPECIFICATION

5.1 CPLL Design Flowchart

The CPLL design methodology can be summarized through the following flowchart:

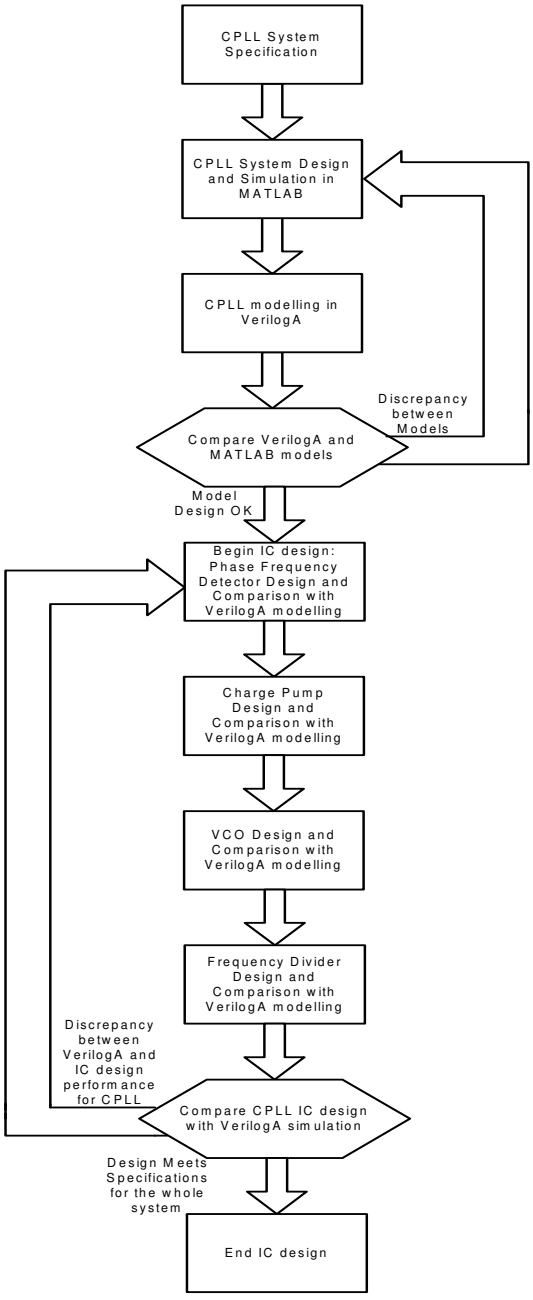

Figure 33: CPLL Design Methodology Flowchart

5.1.1 CPLL Design Methodology

This section enumerates the IC design methodology for the CPLL system as presented in the above flowchart. The methodology involes initially specifying the CPLL top level requirements and performing the necessary simulations in MATLAB. This is followed by modeling the same system in VerilogA [18]-[22] and then by transistor level design of each block. Now the final system performance is compared with that of the initial specifications in MATLAB and one(or both) of the following is performed :

a) the transistor-level design of the system is improved (if required) so that it performs on par with the initial system specifications,

b) the CPLL system-level specifications are made less stringent or practical if required.

The methodology steps are enumerated in the following steps:

1) CPLL top-level system requirements are specified. This includes the CPLL system design with the control element for phase difference generation, the CPLL operating frequency, charge pump current, divider ratio, Phase Noise requirements etc. The Phase Noise requirement is stipulated as better than -90 dBc/Hz at 1 MHz under worst case conditions for maximum phase difference synthesis of 180°.

2) The loop filter [10][11][23]-[25] is designed according to the required loop bandwith which is a critical factor in deciding the contribution of thermal and deterministic noise of various sources in

the CPLL to the total Phase Noise performance of the system. The other important factors in designing the loop filter include the phase margin of the system, the charge pump current and the VCO sensitivity.

3) The CPLL system is designed in MATLAB and the following important simulations are performed: a) frequency convergence transient for the two PLLs in the CPLL, b) variation of the output phase difference synthesized with the control element, c) the Phase Noise due to random and deterministic noise in the CPLL system is simulated and compared with the specifications. If the specifications are not met, one of the most critical elements that can be varied is the loop filter design for the PLLs.

4) The MATLAB design of the CPLL system is modeled in VerilogA in the Cadence environment. Each block in the CPLL system , viz. the Phase Frequency Detector, Charge Pump, Voltage Controlled Oscillator and Frequency Divider is modeled in VerilogA and transient simulations are performed and compared to the results obtained in MATLAB design. VerilogA modeling is helpful in context switching between the mathematical models and their transistor level designs and comparing their performance.

5) IC Design of the CPLL

a) The Phase-Frequency Detector is designed in Current Model Logic [26]-[28] instead of the usual CMOS rail-to-rail logic to

mitigate the effects of power supply and substrate noise. The operating frequency of the PFD is 38.125 MHz.

b) The Charge Pump is designed to source and sink current of 1.353mA at the PFD operating frequency = 38.125 MHz. The design is based on a DAC (Digital to Analog Converter) architecture with no poles in the signal path. It is observed that this design is a non-trivial task with a supply voltage of just 1.2 V. Also care is taken to avoid a dead zone in the PFD/CP design.

c) The VCO essentially converts the input voltage of the loop filter to output frequency. It consists of two blocks: a) the V-2-I converter, which converts the input voltage to an output current and b) the current controlled oscillator, which converts the input current into output frequency. Both the V-2-I converter and the CCO are designed differentially. The open loop phase noise requirement of the VCO is stipulated to be -90 dBc/Hz at 1 MHz offset from the carrier. The VCO sensitivity is designed as 500 MHz/V so that +/-16% open loop VCO frequency variation can be controlled by a +/-200mV variation of the VCO control voltage, around the steady state VCO input voltage of 600mV.

d) The frequency divider is designed as a four stage ripple counter, where each stage divides by two to create a divide-by-16 counter. Each stage consists of two differential latches connected in a master slave fashion and clocked by a differential inverter.

6) Simulate the transistor level design of the CPLL system and observe the phase difference generation and the phase noise performance of the system. If the specifications are not met we go back to step 4 and analyze the performance of each block and try to improve the performance if possible. Also after having performed a preliminary IC design and simulated across Process and Temperature corners if the requirements are found to be stringent and impractical we go back to step 1 and reformulate the system requirements to a more pragmatic specification.

5.2 CPLL System Specifications

Figure 34 shows the schematic of the proposed CPLL system for IC design. This system is essentially the Phase Frequency Synthesizer described in Chapter 3. In comparison to the board implementation, a reference frequency has been introduced. The symmetric nature of the system makes the synthesized output phase difference at steady state independent of the reference frequency as mentioned in Chapter 3.

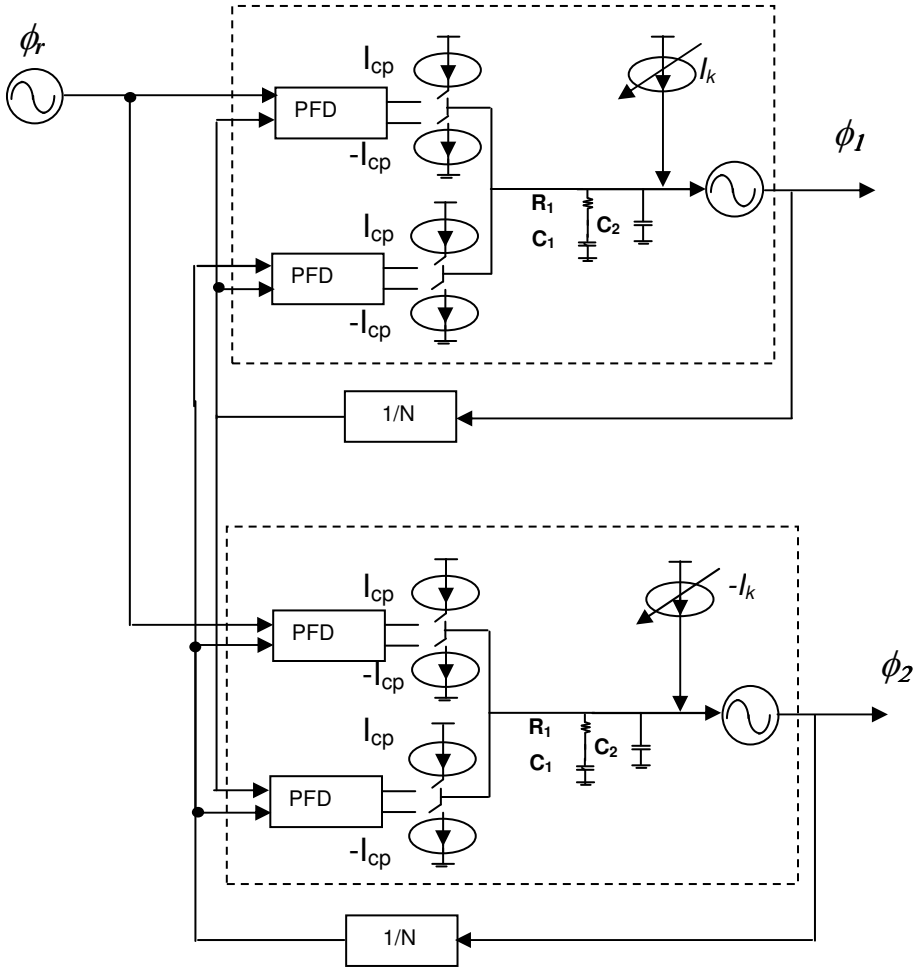

Figure 34: Proposed CPLL for IC design

The equations relating the input and output phases are as follows:

$$\begin{cases} \dfrac{d\phi_1(t)}{dt} = K_{v0} Z_F(t) * \left[(\phi_r(t) - \dfrac{\phi_1(t)}{N}) K_d + \left(\phi_2(t) - \phi_1(t)\right) \dfrac{K_d}{N} + I_K \right] + \omega_0 \\ \dfrac{d\phi_2(t)}{dt} = K_{v0} Z_F(t) * \left[(\phi_r(t) - \dfrac{\phi_2(t)}{N}) K_d + \left(\phi_1(t) - \phi_2(t)\right) \dfrac{K_d}{N} - I_K \right] + \omega_0 \end{cases} \quad (38)$$

where "*" represents the convolution operation, K_d is the PFD gain and $Z_F(t)$ is the impedance of the loop filter in the time domain. The gain of the PFD is $K_d = I_{cp}/2\pi$, where I_{cp} represents the charge pump current. Upon synchronization, both PLLs

oscillate at the same frequency with a constant phase difference $\theta=\phi_1-\phi_2$. Then, subtracting the two equations we obtain:

$$\frac{d\theta}{dt} = \frac{d(\phi_2(t) - \phi_1(t))}{dt} = Z_F(t) * K_{v0}[-\frac{3K_d}{N}(\phi_2(t) - \phi_1(t)) + 2I_K] \quad (39)$$

Hence the rate of change of the phase difference with time is independent of the reference frequency. Setting $d\theta/dt = 0$ results in

$$\theta = \frac{2NI_K}{3K_d} \quad : -\pi \leq \theta \leq \pi \quad (40)$$

Thus, as shown before, the synthesized output phase difference can be controlled linearly. In this particular design the control input is a current. The CPLL top level specifications are as follows: The VCO free running frequency is F_{vco} = 610 MHz which is chosen to fall in the WMTS (Wireless Medical Telemetry Serivce) band between 608 to 614 MHz [29]. The reference is a crystal oscillator which is commercially available for tens of MHz range. Taking this into account, the frequency divider is chosen to have a ratio of N_{div} =16. Hence the reference frequency(F_{ref}) is related to the VCO output frequency(F_{vco}) as:

$$F_{ref} = \frac{F_{vco}}{N_{div}} \quad (41)$$

Substituting the values, the reference frequency is obtained as F_{ref} = 38.125 MHz. The control current (I_k) used for phase difference generation has a resolution of $I_{k\text{-}minimum}$ =1 uA. If the DAC is to be designed for 6 bits accuracy $I_{k\text{-}maximum}$ = 64uA. The phase synthesized is related to the control and the charge pump current according to (40). Hence for a maximum phase syhthesis of 180°, the control current can be related to the charge pump current as :

$$I_{cp} = \frac{4NI_{k-\max imum}}{3} \tag{42}$$

where the charge pump gain is $K_d = I_{cp}/2\pi$. The charge pump current is obtained as I_{cp} = 1.353mA. We choose a phase margin of $\varphi_m = 60°$ and the VCO sensitivity K_{vco} = 500 MHz/V. The latter has been obtained iteratively after a transistor-level design of the VCO and observing VCO output frequency variation across process and temperature corners. The transition frequency(ω_p)[10][11][17] is chosen to be approximately 1/100th of the reference frequency:

$$\omega_p = \frac{2\pi f_{ref}}{100 * 1.3} \tag{43}$$

Also the transition frequency and the natural frequency(ω_n) have the following simple relation)[10][11][17]:

$$\omega_n = \frac{1.33\omega_p}{2.06} \tag{44}$$

Using the above information the time constants related to the pole (p_t) and zero(z_t) are calculated as follows [23][25] for a second order impedance filter:

$$p_t = (\sec(\phi_m) - \tan(\phi_m))/\omega_p \tag{45}$$

$$z_t = 1/p_t\omega_p^2 \tag{46}$$

The capacitance and resistor values can be calculated by the following equations:

$$C_1 = (\frac{z_t}{p_t} - 1) * \frac{p_t K_d K_v}{z_t \omega_p^2 N_{div}} * \sqrt{\frac{1 + \omega_p^2 z_t^2}{1 + \omega_p^2 p_t^2}} \tag{47}$$

$$C_2 = \frac{C_1}{(\frac{z_t}{p_t} - 1)} \tag{48}$$

$$R_1 = \frac{z_t}{C_1} \tag{49}$$

The above CPLL specifications are tabulated as follows:

Table Table 1: CPLL System Specifications

CPLL Parameters	Values
VCO Frequency(F_{vco})	610 MHz
Frequency Divider (N_{div})	16
Reference Frequency(F_{ref})	38.125 MHz
Charge Pump current(I_{cp})	1.353mA
Phase Margin(φ_m)	60°
VCO Sensitivity(K_{vco})	500 MHz/V
Natural Frequency(ω_n)	$1.16*10^6$ Rad/sec
Control Current(I_k)	0 to 64μA
Process	IBM 130nm
Supply	1.2V
Phase Noise	-95 dBc/Hz
Phase Difference Synthesis(θ) Range	0 to 180°

5.2.1 CPLL System Simulation

The above system was initially simulated in MATLAB to see the system response in terms of phase generation and also its phase noise performance. Figure 35 shows the transient response of the phase difference between the PLL outputs in the

CPLL system. The system was simulated with a control current of 62.3µA. This leads to a steady state phase difference of 175°.

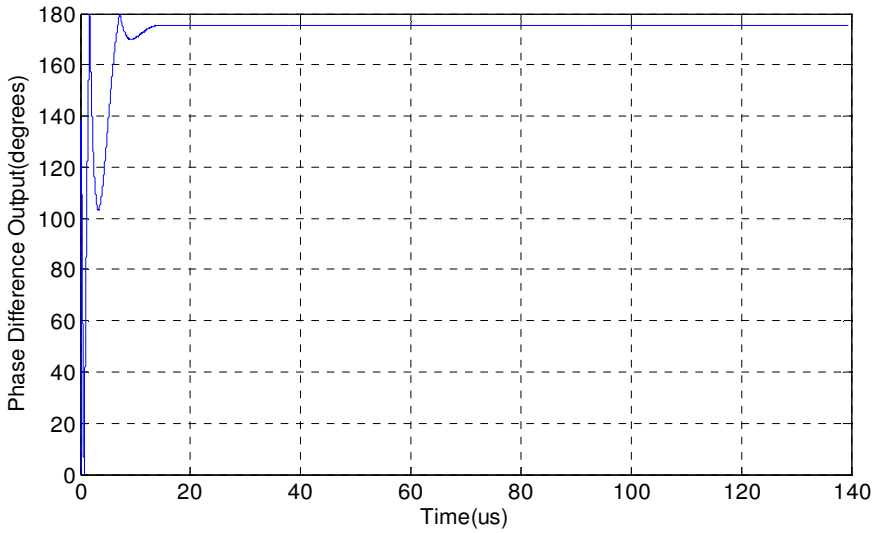

Figure 35: Phase Difference Transient for the CPLL system

Noise performance of the CPLL system was evaluated in terms of random noise and deterministic noise contributing to the CPLL phase noise[18],[30]-[33]. Random noise affecting the phase noise of the CPLL system contributed by the noise generated by the reference frequency, PFD, charge pump, divider and the loop filter have a low pass characteristic. Since all of them have the same characteristic they are conveniently measured as the input referred noise. The input referred noise from all these sources within the loop bandwidth of the PLL, is transferred from the input to the output. Outside the loop bandwidth the thermal noise accumulating from the reference frequency, PFD, charge pump, divider and the loop filter resistor is suppressed by the loop filter. Noise from the VCO has a high pass characteristic. Hence at low frequency offsets the VCO noise is suppressed by the feedback action of the loop. However at high frequencies, the phase noise of the system is essentially contributed by the VCO. In

contrast to random noise which are stochastic in nature, deterministic noise arises due to sources like supply and substrate where the noise is correlated. In the present case we are concerned with the deterministic noise arising due to charge pump activity due to a non-zero phase difference generation. The effect of this is the presense of reference spurs at an offset from the carrier frequency which is equal to the reference frequency.

Figure 36 shows the random phase noise performance of the CPLL system. The CPLL system shows a phase noise performance of -92.6 dBc/Hz at 1 MHz offset, which meets the design specifications.

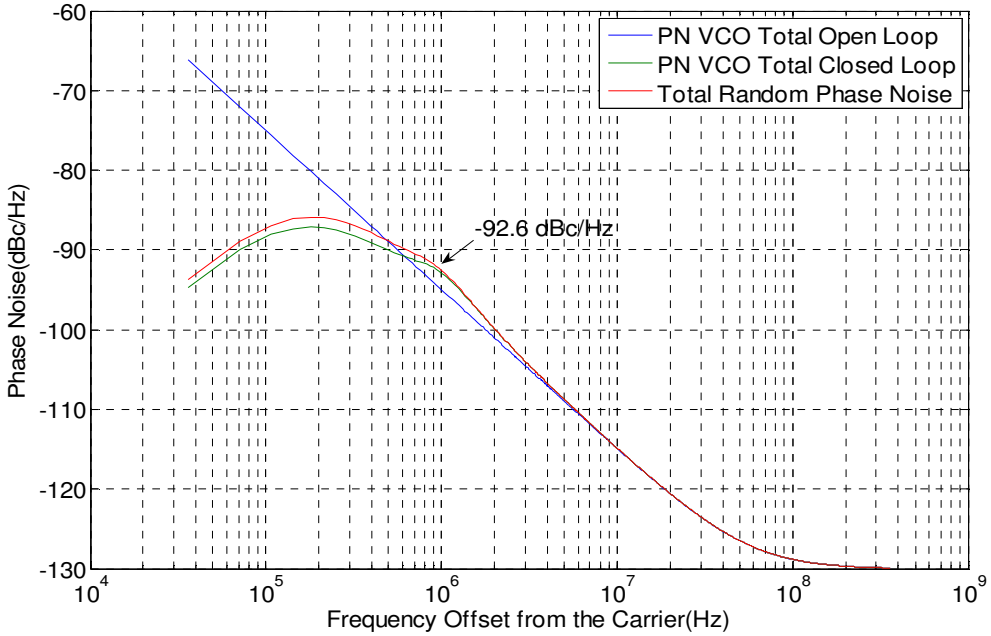

Figure 36: Random Phase noise of the CPLL system

Figure 37 shows the phase noise performance of the CPLL system including both random noise and deterministic noise caused due to reference feed through. The total phase noise due to random noise and deterministic noise is -92.5 dBc/Hz at 1 MHz

offset from the carrier. The noise due to the reference spurs is at -77 dBc/Hz at 38.125 MHz offset from the VCO operating frequency.

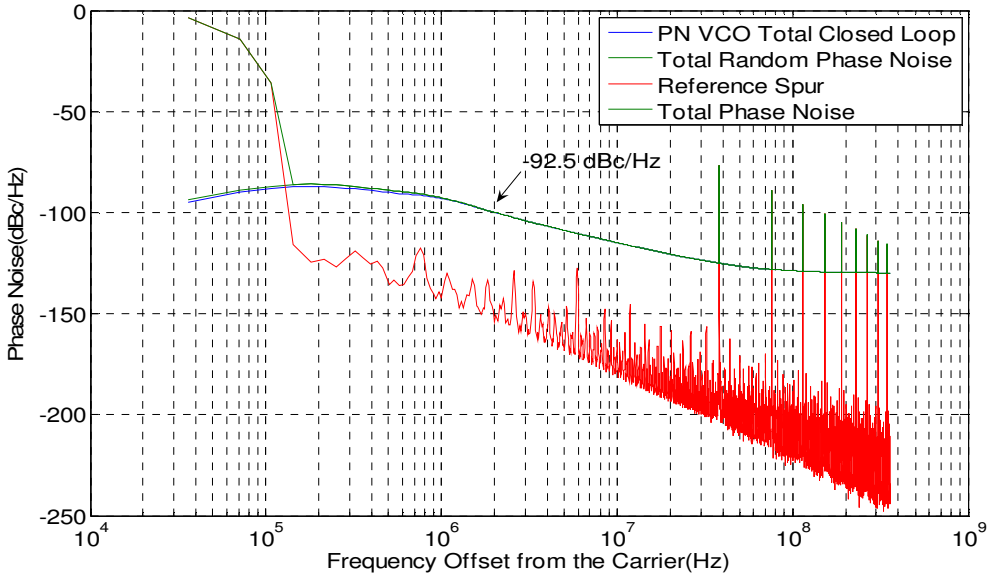

Figure 37: Deterministic and Random Phase noise of the CPLL system

5.3 Summary

This chapter presented the design methodology to be followed for implementing the IC for the Coupled PLLs system. The methodology shows the process to be followed when implementing the initial design and then improving the same iteratively. The top-level specifications for the Coupled PLLs system were mentioned. The system was implemented in MATLAB and transient simulations followed by Phase Noise Analysis of the system was performed to see the design meets the specifications.

The next chapter focuses on the IC design at the transistor level beginning with VerilogA modeling of the system.

CHAPTER 6

COUPLED PHASE LOCKED LOOP IC DESIGN

6.1 CPLL VerilogA Modelling and Simulation

The first step in the IC design process was modeling the CPLL system in VerilogA. Each block in the CPLL system is modeled mathematically in VerilogA and the system functionality is verified. Then we proceed to do the transistor level design of each block. Preliminary VerilogA modeling of the system has the advantage of fast context switching between the transistor level designs and the mathematically modeled designs to verify the proper functioning of the former with the mathematical models.

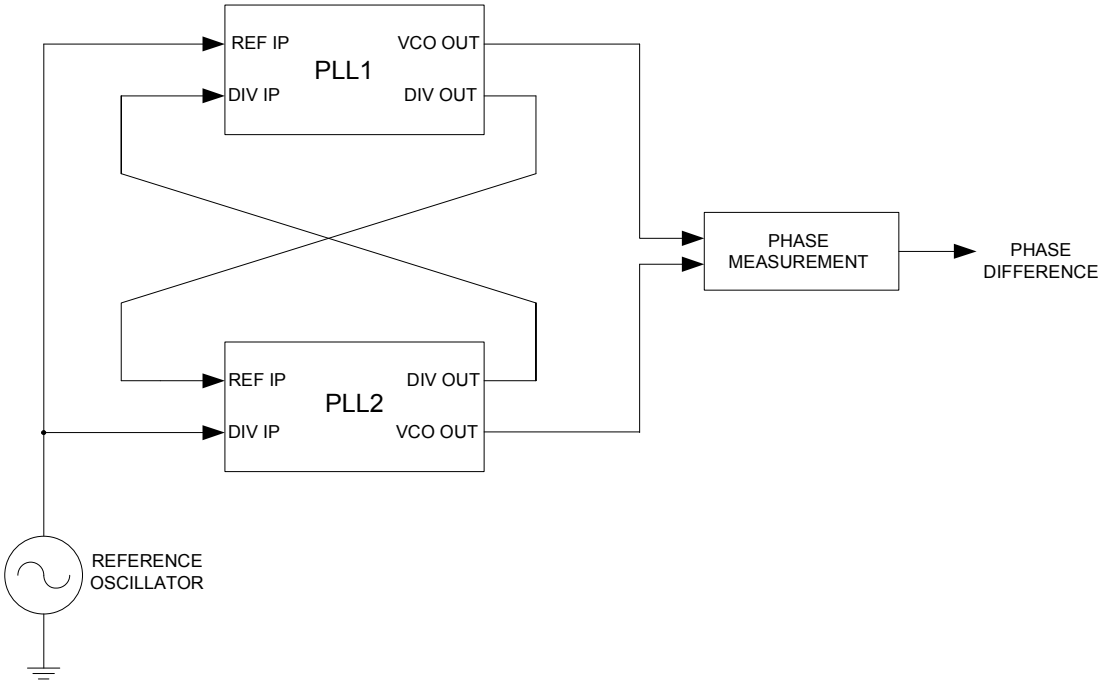

Figure 38: CPLL Top Level Block Schematic

Figure 38 shows the top level schematic of the CPLL system. It shows two PLL blocks coupled to each other and also the phase measurement block. The latter takes the VCO output waveforms from the two PLLs as its input and shows the phase difference between the two waveforms. During the IC design phase the entire CPLL is designed at the circuit level except the phase measurement blocks, for which only VerilogA models are used. Each PLL block consists of two PFDs and two CPs (each one more than in the usual PLLs), one VCO, one frequency divider and the loop filter.

Figure 39 shows the deterministic noise performance of the CPLL system when the control current is zero and hence the phase difference at the PLL outputs at steady state is zero. The phase noise performance due to deterministic noise is -175 dBc/Hz at 1 MHz offset. Also absence of reference spurs at offset of 38.125 MHz (which is the reference frequency) from the carrier frequency indicates good phase noise performance of the CPLL system in attenuating deterministic noise at zero control current.

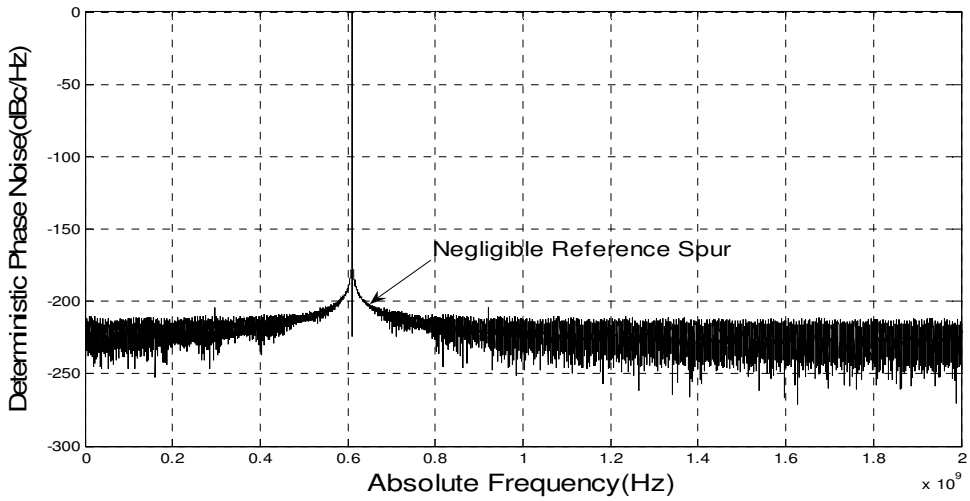

Figure 39: VerilogA deterministic phase noise simulation of the CPLL system at zero control current

Figure 40 shows the total phase noise performance of the VerilogA model when the control current is 63µA and the phase difference between the PLLs is 177.5°(near maximum). The simulation results show the cumulative result of deterministic noise from the VerilogA model and the analytical models for thermal noise from various sources in the PLL(e.g. the PFD/CP, VCO,divider etc) which have been presented in the MATLAB simulations above. The total random phase noise of the system is attenuated by the loop, at frequencies close to the carrier frequency. The deterministic spurs are present at the reference frequency offset from the carrier at -60dBc/Hz and multiples of the reference frequency. The total phase noise is -88 dBc/Hz at 1MHz offset from the carrier, which is acceptable if consideration is given to the fact that, at this phase offset the charge pump is active for 3.125% of its time period, which directly contributes to phase noise at the output.

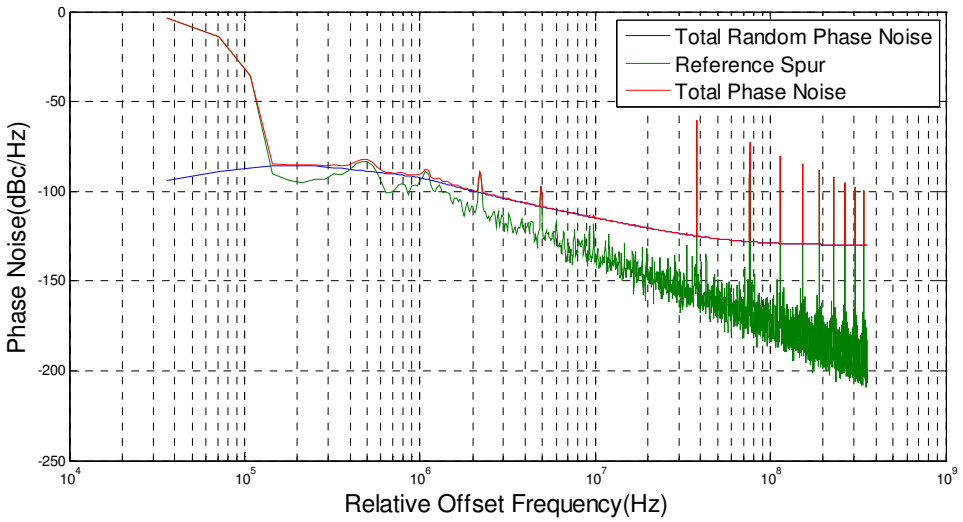

Figure 40: VerilogA total phase noise simulation of the CPLL system with 63uA control current input

6.2 CPLL IC Design and Results

6.2.1 Current Mode Logic Design

The CPLL design is a typical example of high speed mixed signal design with low switching noise requirements. If the PFD is implemented using CMOS logic, the rail-to-rail switching affects the sensitive analog blocks, like the VCO, detrimentally, thereby increasing the phase noise of the system. The same is the case with the frequency divider if implemented using CMOS rail-to-rail logic. In order to reduce the effect of the switching noise of the PFD and divider on the VCO, they can be implemented using Current Mode Logic (CML). CML circuit design involves implementing the circuits in a differential manner. Thus the noise due to logic transitions and other sources like the power supply noise, appear as common mode noise at the output of one CML gate, thereby rejected.

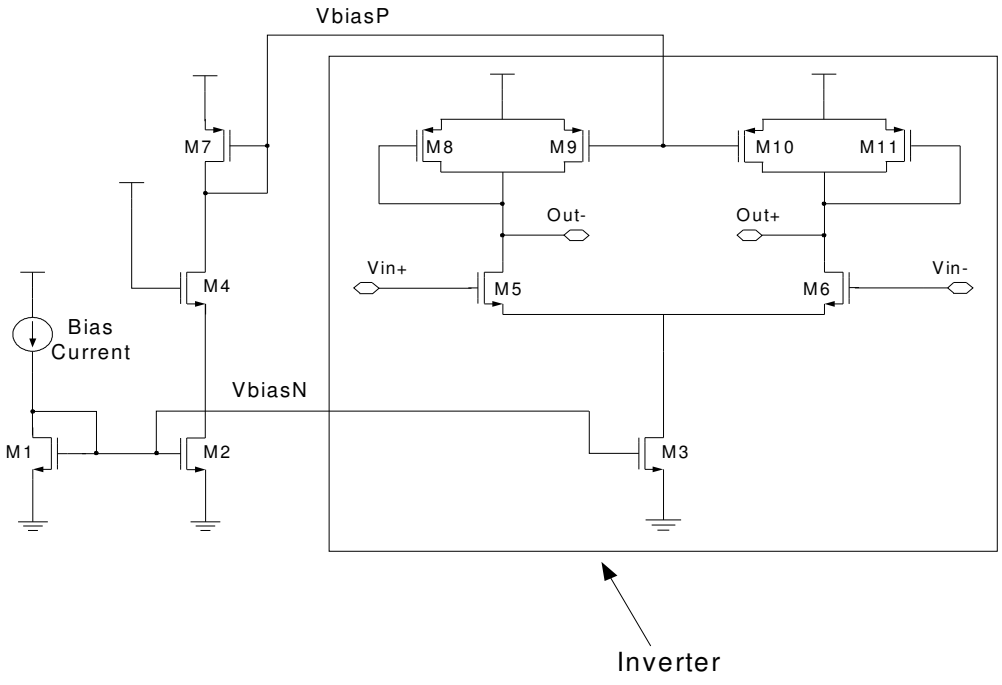

Figure 41: CML Inverter

Figure 41 shows the basic inverter implementation using CML. It is basically a differential amplifier, with tail current biasing using an NMOS transistor M3. The load is designed using two PMOS transistors; one of which is a diode connected load (M8, M11) and the other is biased as a variable current source (M9, M10). The implementation of the bias circuitry required by the NMOS and PMOS current sources (VbiasN and VbiasP respectively) is also shown. Purely differential implementation with biasing tail current sources reduces the output voltage swings and hence the switching noise affecting the analog circuitry is also reduced.

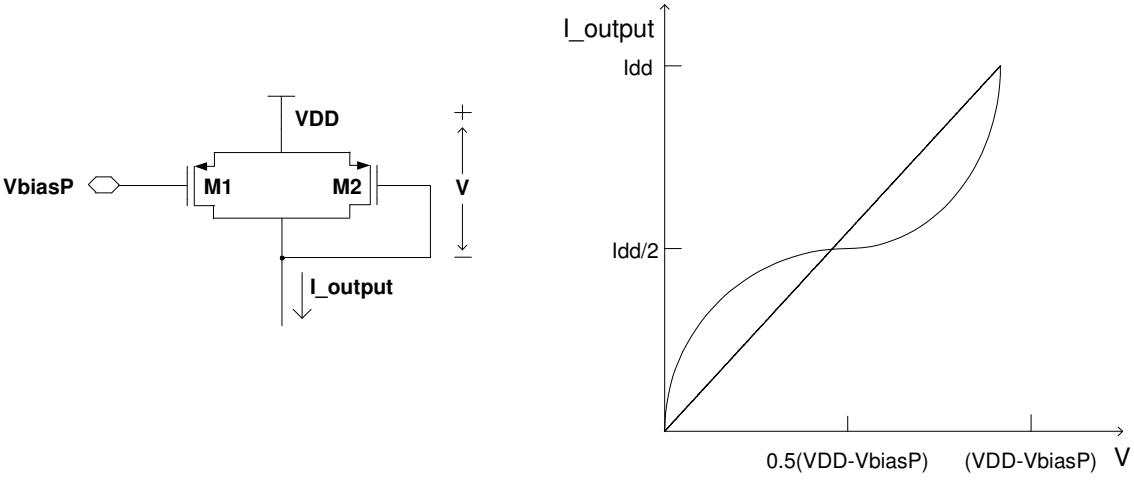

Figure 42: Symmetric load for CML circuits and I-V characteristics

The load for the CML inverter is implemented using a diode connected PMOS(M1) and a constant voltage biased current source(M2) as shown in Figure 42. The I-V characteristic of the load is also shown. The characteristics appear symmetrical and linear on the average, hence the name symmetrical load [34]. Due to the linearity of the loads the differential circuits exhibit high rejection for common mode noise.

6.2.2 Phase Frequency Detector

The block schematic of the Phase Frequency Detector (PFD) [33][35] is shown below (Figure 43). It consists of two D Flip Flops (DFF) and a differential AND gate for resetting the DFFs. The blocks in the PFD are implemented using Current Mode Logic (CML) . The DFFs have a RESET input to set the output to LOGIC LOW in addition to the CLOCK input.

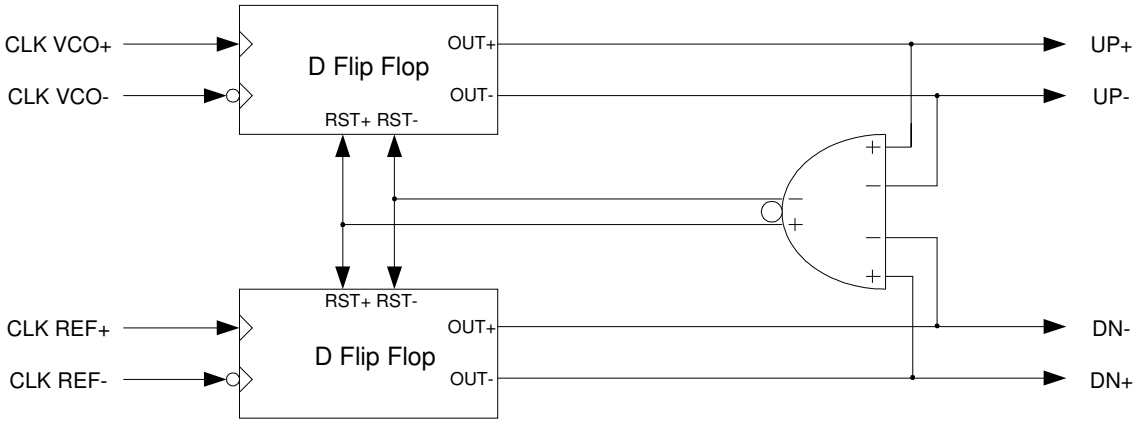

Figure 43: CML Phase Frequency Detector

The functionality of the PFD is explained in the following. If the rising edge of the REF input to the PFD arrives before the VCO rising edge, the UP input is HIGH during that duration. At the rising edge at the VCO input, the PFD DN output is HIGH. This enables the differential AND gate which RESETs the DFF outputs to LOGIC LOW.

The DFF is in turn implemented using NOR gates as in Figure 44 [35]. The DFF design has been simplified to suit the present design requirement, by assuming the D input to the Flip Flop is tied to LOGIC HIGH. Hence the output tracks the first rising edge of the clock pulse to go HIGH after which the RESET mechanism in the PFD sets the output of the Flip Flop to LOW.

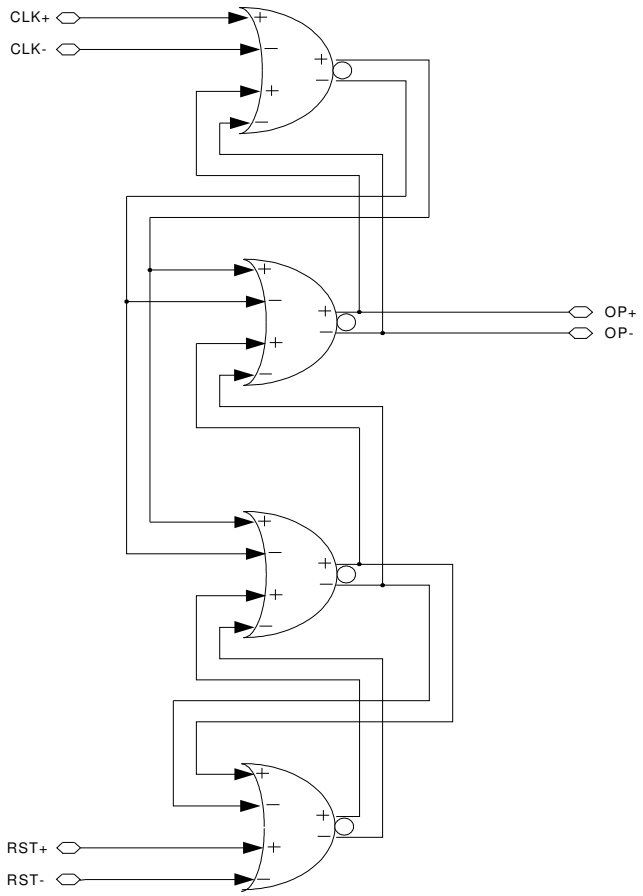

Figure 44 : CML D Flip Flop with input set to HIGH

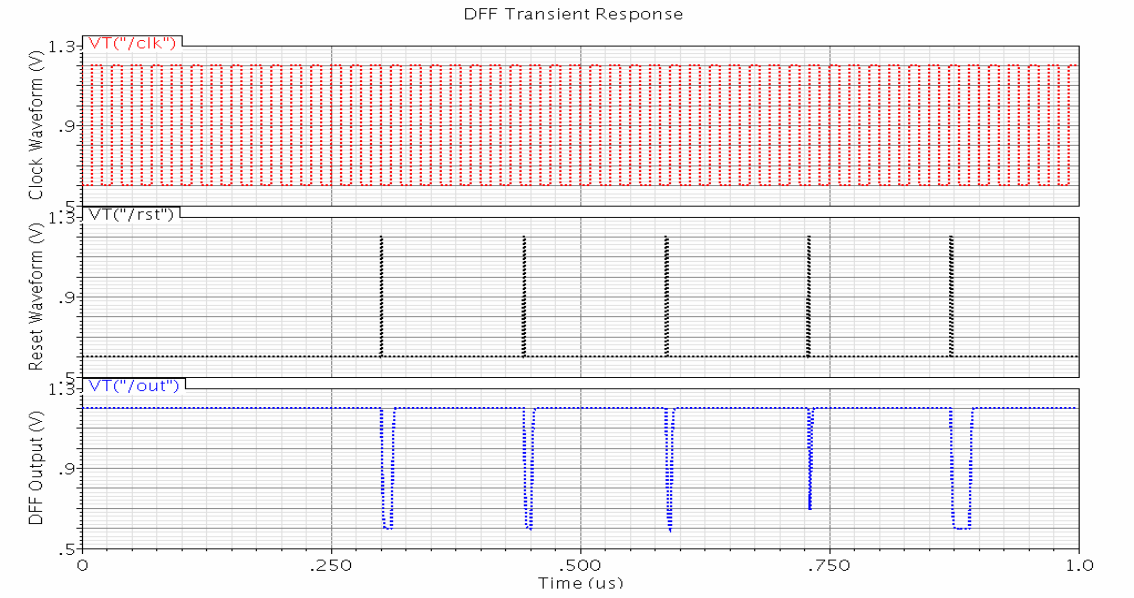

Figure 45: DFF Output Waveforms

Figure 45 shows the DFF output waveforms when the input clock to the DFF is set to a frequency of 50MHz, RESET input is set to 7 MHz and the output load is 50fF. It is observed that the DFF output is set to logic ZERO with each RESET pulse. The output goes to HIGH with the next rising edge of the clock. The average propagation delay = 952 ps, rise time = 2.45ns and fall time = 2 ns under worst case conditions of process corner = Slow-Slow and temperature = 125°C.

The implementation of NOR/OR CML gate is shown in Figure 46. An additional vertical stacking of transistors is necessary compared to the CML inverter because of one additional input for the NOR/OR gate. Reversing the inputs changes the NOR/OR gate to NAND/AND gate.

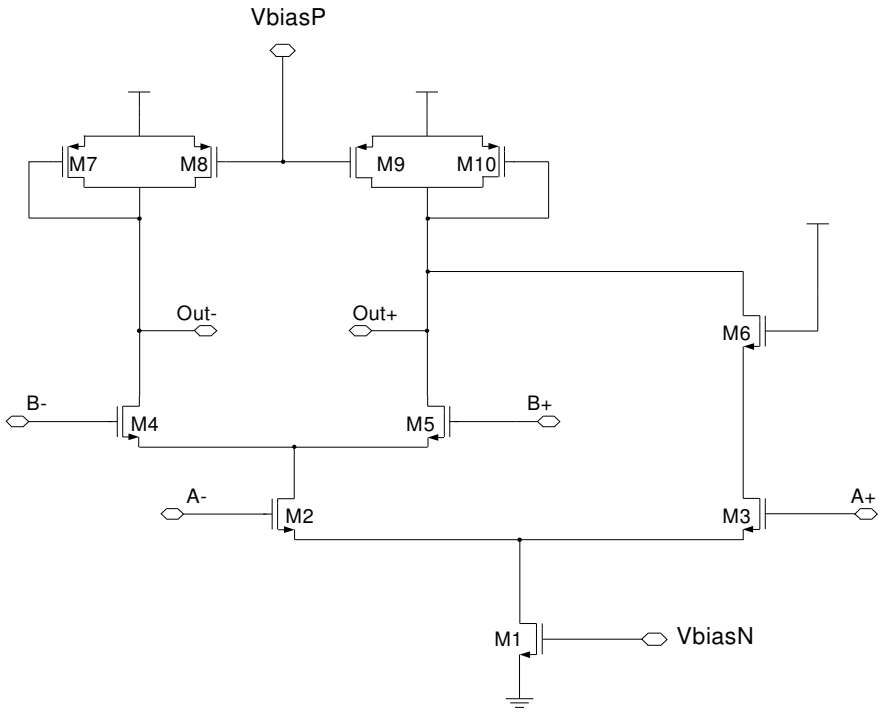

Figure 46: CML NOR Gate implementation

The PFD has been designed in CML using all the CML gates discussed above. Figure 47 shows the transient PFD waveforms. Here VCO and REF are the PFD input

waveforms and UP and DN are the output waveforms. For experimental purposes, the VCO has a frequency of 39 MHz and REF has a frequency of 38.125 MHz. Also at t = 0 the VCO has a positive phase delay compared to the REF waveform, which is indicated by the HIGH transitions of the UP output of the PFD. Due to the larger frequency the VCO gradually reduces the phase delay. This is indicated by the gradual decrease in the HIGH state of the UP waveform and the gradual increase in the HIGH state of the DN waveform. This verifies the PFD functionality.

Dead zone minimization [33][35] is an important design aspect in PFDs. Dead zone occurs when the PFD/CP combination fails to respond to a phase difference at the PFD inputs, below a certain value. Hence below this value the feed back loop is essentially open which leads to high phase noise at the output due to VCO open loop phase noise. Dead zone can be minimized by essentially keeping the charge pump active during the period, by keeping either the UP or DN output of the PFD at the HIGH state which turns the charge pump on. This is done by adjusting the delay in the feedback path in the PFD. Increasing the delay in the feedback path, increases the time to reset the PFD outputs and hence gives sufficient time for the PFD outputs to reach the HIGH state and turn on the charge pump. Careful simulations were performed to see that the delay in the feedback path was long enough to minimize the dead zone. Also the transient simulation above shows at any given transition time, the minimum voltage at the PFD outputs is a HIGH, even when the phase difference at the inputs is very small.

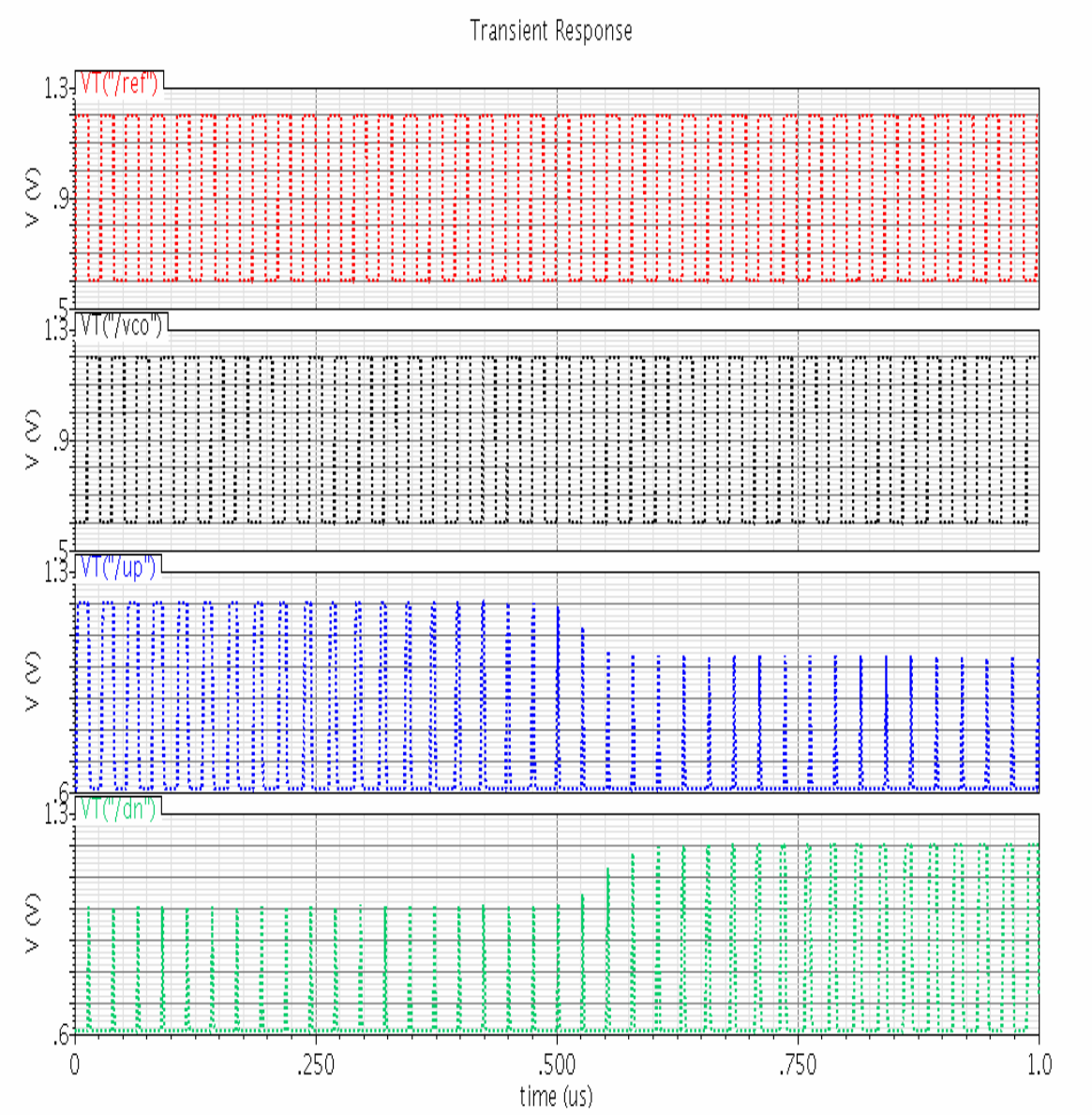

Figure 47 : PFD Input and Output Waveforms

6.2.3 Charge Pump

Figure 48 shows the charge pump [36] design which is compatible with CML PFD. The charge pump is based on Digital to Analog Converter (DAC) design. Here the output current is controlled by switches which determine the direction of flow of the charge pump current, by either sinking or sourcing current into the loop filter. The

Charge Pump inputs are controlled by the PFD outputs UP and DN (and the complementary outputs).

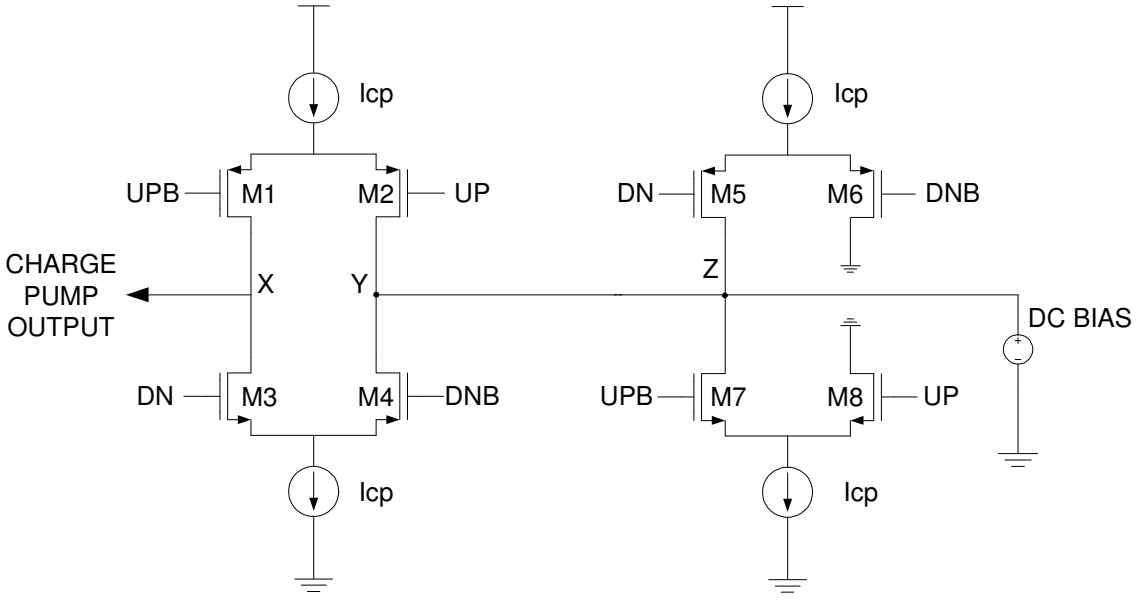

Figure 48: Charge Pump Implementation Compatible with PFD CML

The charge pump output current is taken from the drain of transistors M1 and M3 at node X. Due to the purely differential nature of the DAC stage it is necessary to keep the voltages of nodes X and Y as close as possible to maintain symmetry. This necessitates a common mode feedback implementation between nodes X and Y. To avoid amplifier implementation and the associated stability related issues a simple DC bias implemented using a diode connected load is used to fix the voltage of node Y equal to the voltage at node X at steady state. Also a second identical DAC stage implemented using switching transistors M5, M6, M7 and M8 helps to maintain a symmetric current flow in the circuit. The fixed DC bias implementation and the sourcing and sinking of current in transistors M2 and M4, by the second DAC stage helps obviate the design of the common mode feedback amplifier.

Figure 49 shows the current flows in the charge pump when the PFD outputs are UP=HIGH and DN=LOW. Under this condition the Charge Pump should source current into the loop filter. Since UP = HIGH, M1 is active and directs current to the Charge Pump output as required by the condition at the PFD outputs. Also since DN = LOW, the current in the second stage of the Charge Pump flows from M5 through M4.

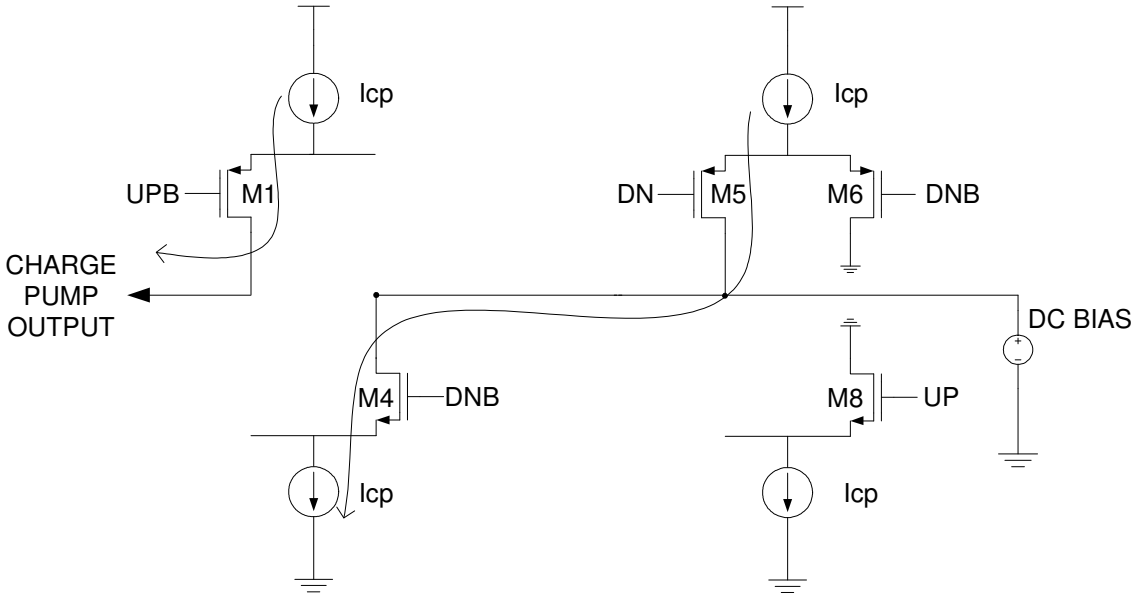

Figure 49: Charge Pump current flows when UP=HIGH and DN=LOW

Figure 50 shows the current flows in the charge pump when the PFD outputs are UP = LOW and DN = HIGH. Under this condition the Charge Pump should sink current from the loop filter. Since DN = HIGH, M3 is active and directs current into the Charge Pump as required by the condition at the PFD outputs. Also since UP = LOW, the current in the second stage of the Charge Pump flows into M7 from M2.

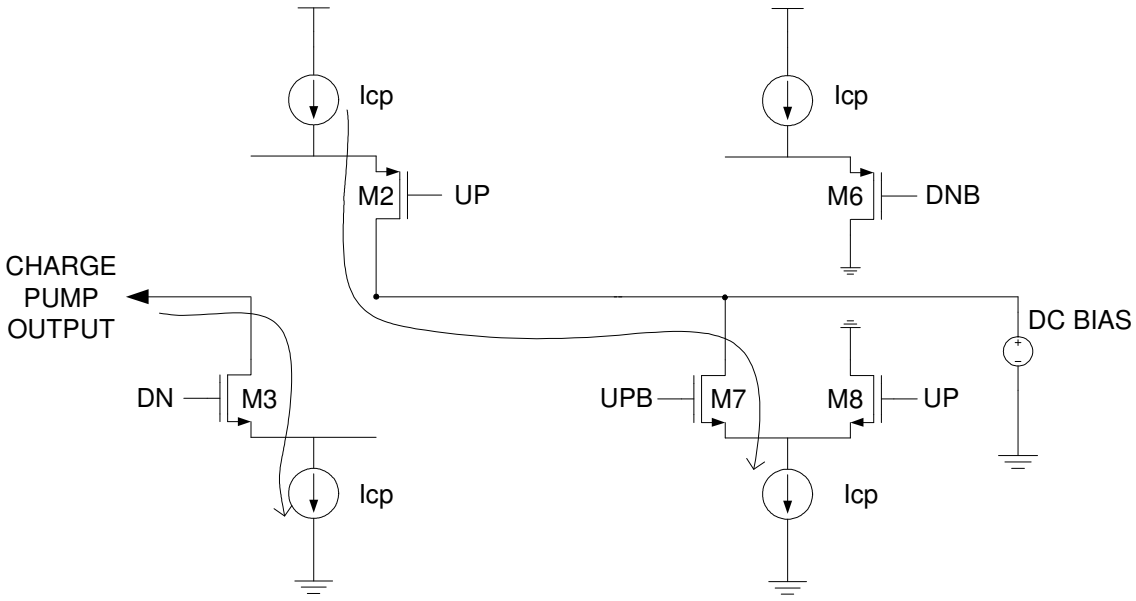

Figure 50: Charge Pump current flows when UP= LOW and DN= HIGH

Figure 51 shows the current flows in the charge pump when the PFD outputs are UP = LOW and DN = LOW. Under this condition the Charge Pump output should be at high impedance. As shown in the figure, M1 and M3 are OFF and hence the charge pump output is disconnected from the loop filter. The current in the first stage directly flows in the right branch through M2 and M4. Similarly the current in the second stage flows directly through the left branch through M5 and M7.

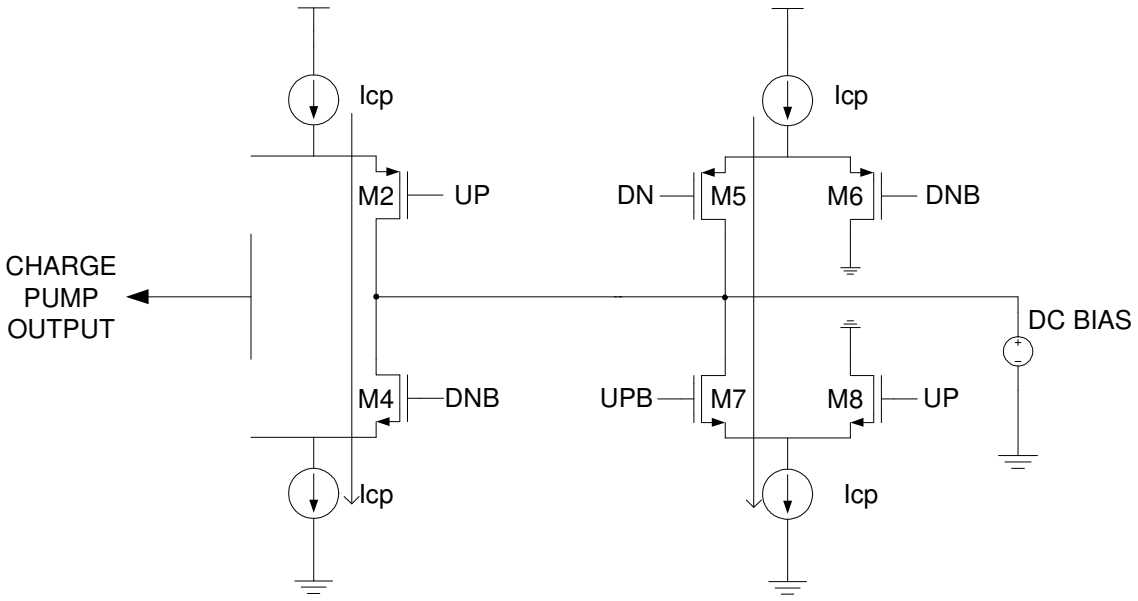

Figure 51: Charge Pump current flows when UP= LOW and DN= LOW

This charge pump is not as power efficient as the charge pumps used with CMOS rail-to-rail logic since this always consumes DC power. However the design will have good current matching since the UP and DOWN stages are symmetric. This leads to reduction in the reference spurs [33].

Figure 52 shows the CP average output current measured across different phase offsets of the waveforms at the PFD inputs. The average current is measured across several transitions at the PFD inputs and plotted across temperature and process corners. We observed a linear increase in the average charge pump current when the phase difference at the PFD inputs is varied from -180° to +180°. Hence the PFD CP gain is nearly constant across different phase differences which is a required PPFD/CP characteristic. Also we see that the average CP current curve maintains its linearity at very small phase differences at the PFD inputs. Hence dead zone is reduced to almost zero in the present PFD design.

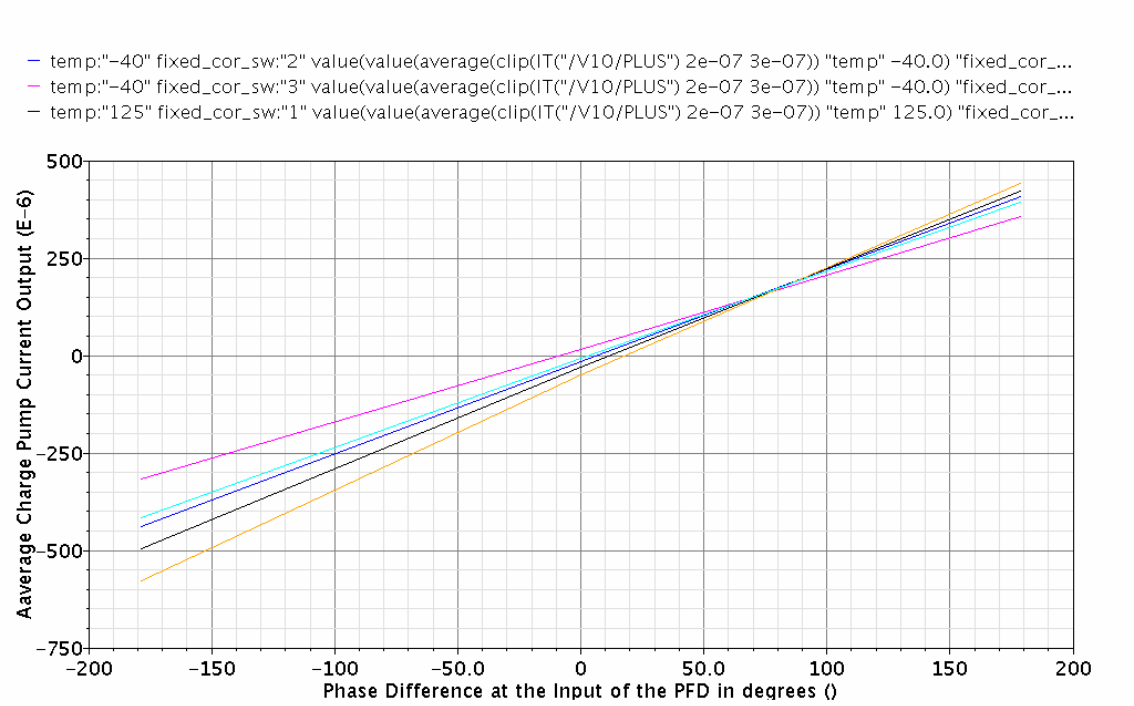

Figure 52: Average Charge Pump Output Current

Figure 53 shows the output noise current of the charge pump obtained from Periodic Noise Analysis of the charge pump in Spectre RF. The Periodic Noise Analysis has been performed for worst case conditions, that is, maximum phase offset at the PFD inputs at steady state, and across process and temperature corners. We observe a noise current of 30 pA/√Hz at 1 MHz offset and current peaks at multiples of the reference frequency of 38.125 MHz.

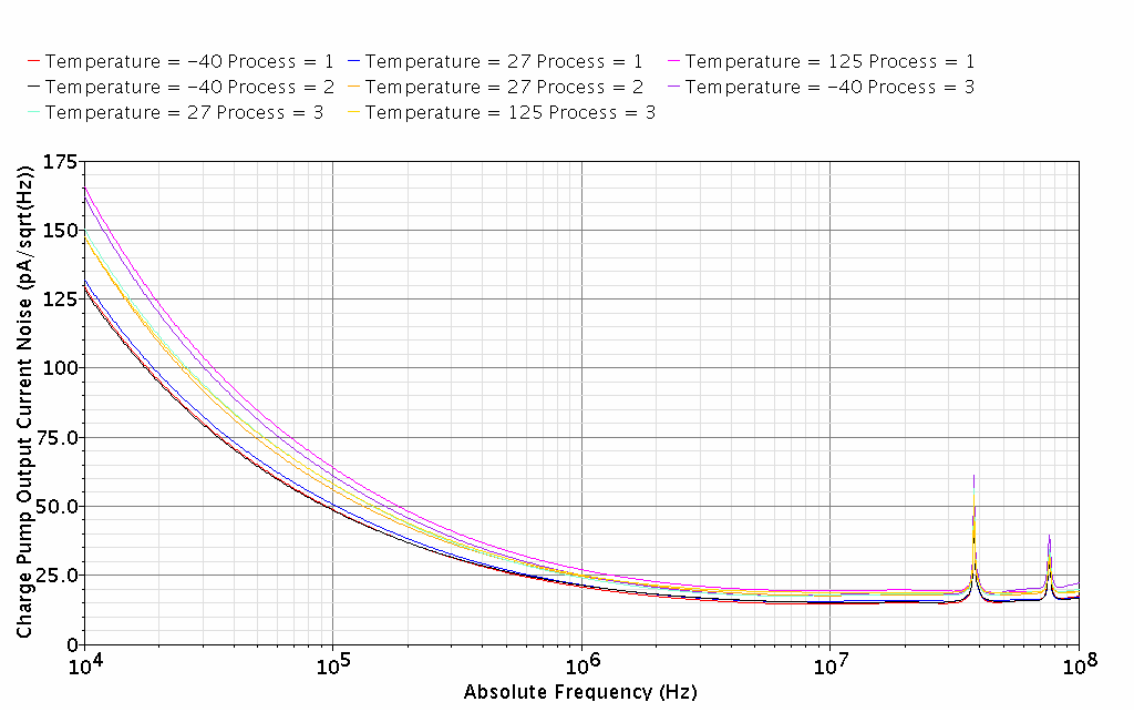

Figure 53: Charge Pump Output Current Noise(A/sqrt(Hz))

The current noise observed at the charge pump outputs can be referred to the input of the PFD by dividing the output noise current with the PFD/CP gain. The input referred PFD/CP noise is shown in Figure 54 . The input referred noise is -134 dBc/Hz at 1 MHz offset. This value is still much below the expected phase noise performance of the VCO at 1 MHz offset from the carrier which is -95 dBc/Hz and hence can be safely accepted as good performance figure. At the frequency of operation of the charge pump the input referred PFD/CP noise peaks to -127 dBc/Hz. This is because under the worst conditions for maximum phase difference synthesis, the charge pump is active for nearly 3.125% of the period. This value is arrived at as follows. For maximum phase difference synthesis of +/-180° the VCO output waveforms are offset from each other by *T/2*, where *T* is the time period of the VCO output waveforms. Since the frequency

divider divides by 16, the waveforms at the input of the charge pump are offset from each other by *T/32 = 0.03125*T*. This gives the worst case charge pump activity factor.

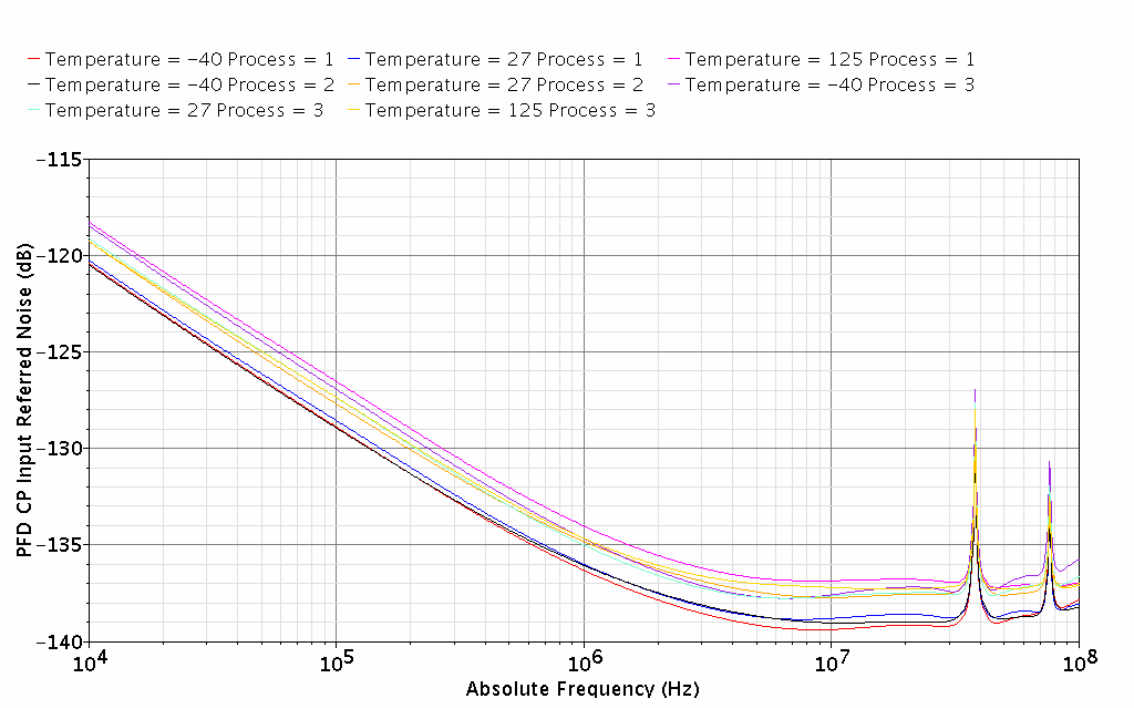

Figure 54: PFD CP Input Referred Noise(dB)

6.2.4 Loop Filter

The loop filter is a second order passive filter and has been implemented as in Figure 34 with the following values: R1 = 45.48Ω, C1 = 45.56nF and C2 = 3.524nF. The large values for the capacitors necessitate their implementation as external components, rather than being integrated on chip.

6.2.5 VCO

The VCO [33][34][35][37]-[43] is the most critical block in the CPLL design in terms of phase noise performance. Figure 55 shows the block schematic of the VCO. It consists of two sub blocks: 1) the V-to-I converter or the transconductance block which converts the input voltage from the loop filter into output current, 2) the Current Controlled Oscillator (CCO) which converts the output current of the V-to-I converter to VCO Output frequency.

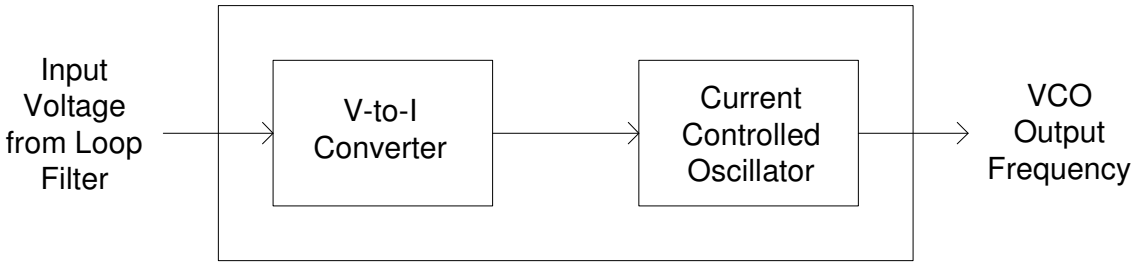

Figure 55: System Block diagram for the VCO

Figure 56 shows the detailed schematic of the V-to-I converter [44], which has been implemented in a differential form. The idea is to compare the loop filter voltage(V_{ctrl}) to a reference voltage(V_{ref}) which should be present at the VCO inputs at steady state. In the present design the reference voltage is 600mV. The upper current sources are biased at 156µA and the bottom current sources are biased at 312µA. The feedback loop controlled by PMOS transistors M3 and M4 supply the difference 156µA current. The feedback loop essentially serves to reduce the input impedance at the source of transistors M1 and M2, by the gain of the common source feedback transistors. This helps in increasing the linearity of the transconductance gain from the gates of M1,M2, that is, V_{ctrl} and V_{ref} , to the drain currents of M3,M4. This drain

current in M3,M4 is further mirrored into M5, M6. M6 essentially controls the input current to the current controlled oscillator. The dummy transistors M5, M7 are present to maintain the symmetry in the circuit.

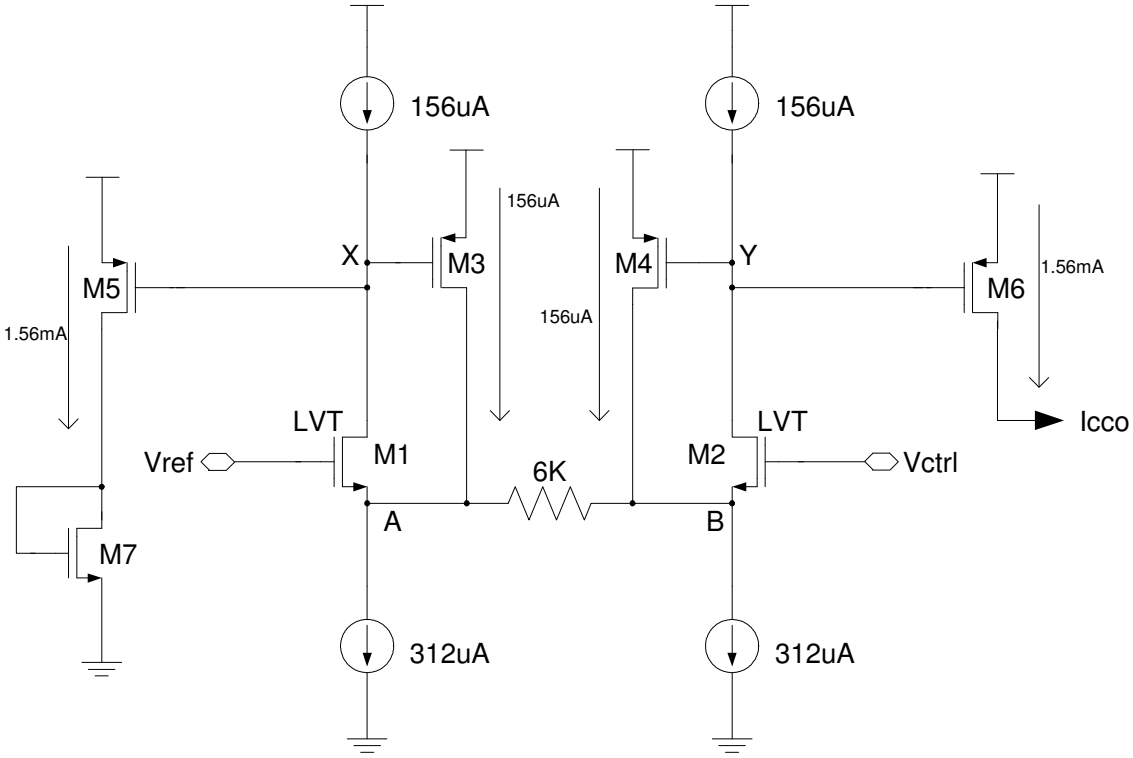

Figure 56: Circuit Schematic for the V-2-I converter

Figure 57 shows the current flows and the output current change in the V-to-I converter due to small change in the VCO input voltage. If the control voltage V_{ctrl} is increased by a small amount *v***,** this leads to an increment in the drain current of M2. This increases the gate-source voltage (V_{gs}) of M4, leading to an increase in current in M4 by,

$$i = v/(R/2) \qquad (50)$$

where R is the resistance connected between nodes A and B. In a similar way, the transient current in M3 decreases by *i*. The sizing ratio of M4 and M6 is given as:

$$(W/L)_{M6} /(W/L)_{M4} = 10 \quad (51)$$

Hence a change in current by *i* in M4 leads to a change in current by *10i* in M6 which then feeds into the CCO.

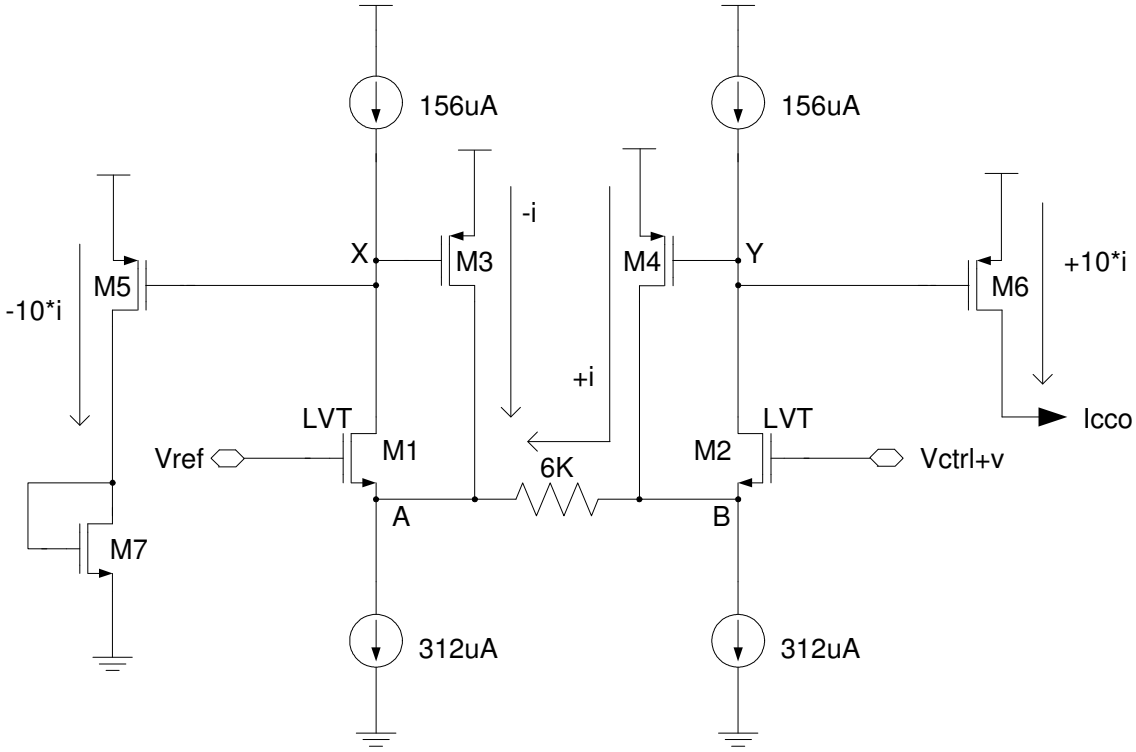

Figure 57: Small Signal current flows in the V-2-I converter

Figure 58 shows a delay block which is the basic element in the CCO. It is essentially a differential amplifier with symmetric loads and tail current biasing. The biasing for the tail current and symmetric loads is also shown in the figure.

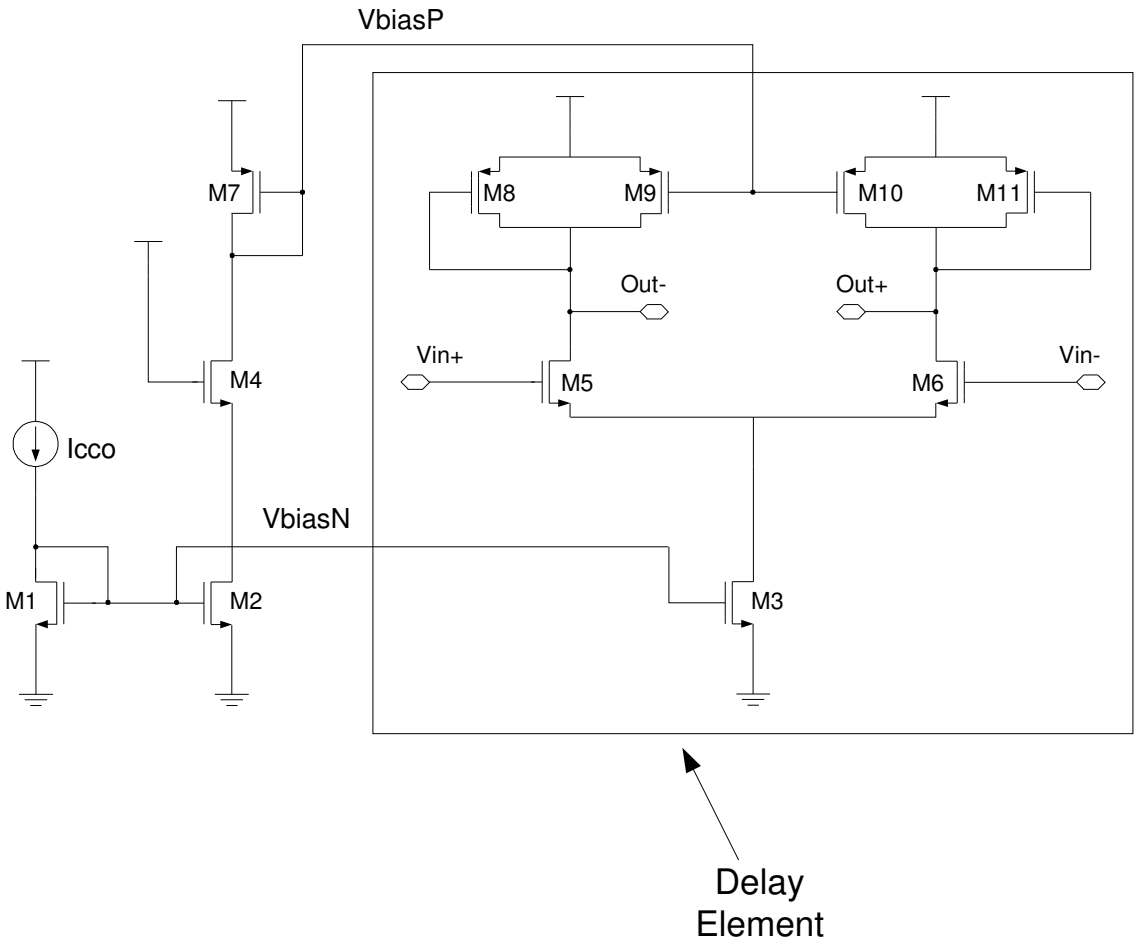

Figure 58: CCO Delay element

As mentioned before, the symmetrical loads have linear I-V characteristics like resistors. Hence any disturbance like power supply noise, appear as common mode noise at the outputs of the delay elements and is rejected by the next stage delay element. The delay in each element is controlled by the slew rate:

$$\Delta v/\Delta t = I_{tail}/C_{output} \qquad (52)$$

where C_{output} is the total capacitance at the output nodes, for example, at the drain of M6, M10 and M11. The capacitance at the output node, depends on parasitic component values which vary with process and temperature and hence not controlled accurately. This affects the frequency controllability of the VCO in open loop condition. However

this is offset by the feedback action of the loop and accurate frequency output of the reference clock [45][46].

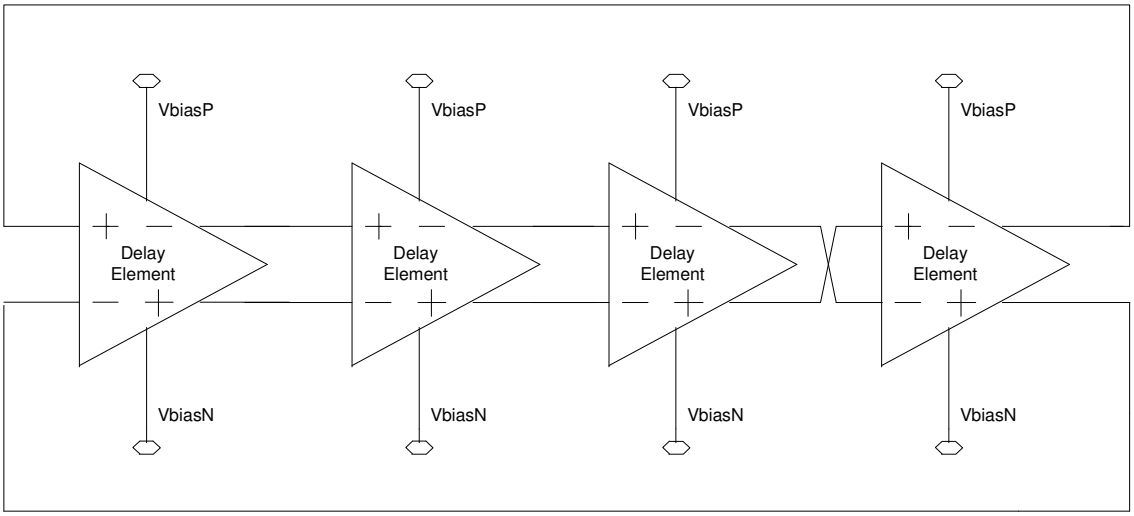

Figure 59: CCO block schematic

The delay element in Figure 58 is replicated four times and connected as shown in Figure 59 for the CCO. The four stages are used in the present design for quadrature phase generation. A first order VCO parameter design procedure is as follows [33][35]: The VCO free running frequency is assumed to be subjected to +/-16% variation due to process and temperature variations. This has been verified by simulations on the IBM 130nm process. The supply voltage being 1.2V, the +/-16% open loop VCO frequency variation is to be controlled by a +/-200mV variation of the VCO control voltage around the steady state VCO input voltage of 600mV. Hence the nominal VCO sensitivity is given by:

K_{vco} = Change in VCO Output voltage / Change in VCO control current (53)

= 16% of 610 MHz / 0.2 V = 488 MHz/V

A preliminary estimate for the biasing current required for the CCO based on the phase noise requirements is as follows:

The VCO output voltage oscillates between 0.6V and 1.2V and hence $V_{peak\text{-}to\text{-}peak}$ = 0.6V and $V_{rms} = V_{peak\text{-}to\text{-}peak}/2\sqrt{2} = 0.3/\sqrt{2} = 0.212$V. We denote T_d as the time required for each delay element to trigger the next delay element in the ring oscillator. In time T_d the maximum swing at the output of each stage is half the maximum swing, $V_{maximum\text{-}swing}$. Hence swing $\Delta V = V_{maximum\text{-}swing}/2 = (V_{DD} - V_{DD}/2)/2 = V_{DD}/4$ in time T_d.Substituting the values in equation (40) we get,

$$V_{DD}/4 = I_{tail} * T_d / C_{output} \tag{54}$$

The VCO free running frequency is given by

$$f_{vco} = 1/(2*N* T_d) \tag{55}$$

where N is the number of delay stages in the oscillator which is 4 in the present case. Substituting (42) in (41) we get,

$$f_{vco} = 2 I_{tail} /(N* C_{output}* V_{DD}) \tag{56}$$

The following equation gives a first order estimate of the open loop VCO phase noise due to thermal noise [33]:

$$PN(\Delta\omega) = \frac{2kT}{{v_{rms}}^2 \omega_{osc} C_{output}} * (\frac{\omega_{osc}}{\Delta\omega})^2 \tag{57}$$

where PN(Δω) = phase noise of the VCO = -100 dBc/Hz at 1 MHz offset,

$kT = 4*10^{-21}$ J at T = 300K,

$V_{rms} = 0.212$V,

$\omega_{osc} = 2*\pi*610*10^6$ rad/sec.,

$\Delta\omega = 2*\pi*1*10^6$ rad/sec.,

C_{output} = load capacitance of each delay element which is to be computed.

Substituting the values we obtain the load capacitance as C_{output} = 172.6 fF. Now the tail current required is given by the following:

$$I_{tail} = \frac{NC_{output}V_{DD}f_{osc}}{2} = 252uA \tag{58}$$

The VCO was initially designed and the transistors sized using these values of the tail current and the capacitance at the output of each delay element. The Spectre RF simulation was performed on the VCO to obtain the phase noise performance. It was observed that the performance was not as expected and the degradation was due to flicker noise of the biasing elements in the CCO and the V-to-I converter. The procedure to reduce flicker noise in the biasing elements is to increase the transistor area while keeping the aspect ratio constant. The latter is done so as not to disturb the bias point. Increasing the transistor area has the effect of reducing the VCO free running frequency, due to increasing parasitic capacitance. To compensate for this, the control current has to be increased. So after the initial first order design, Spectre RF analysis was used to size the transistors and arrive at the final results.

6.2.5.1 VCO Simulation Results

Figure 60 shows the differential VCO transient outputs for the final design. It is observed that the VCO reaches its maximum stable output with a peak to peak voltage of 600mV and an output frequency of 610 MHz as expected.

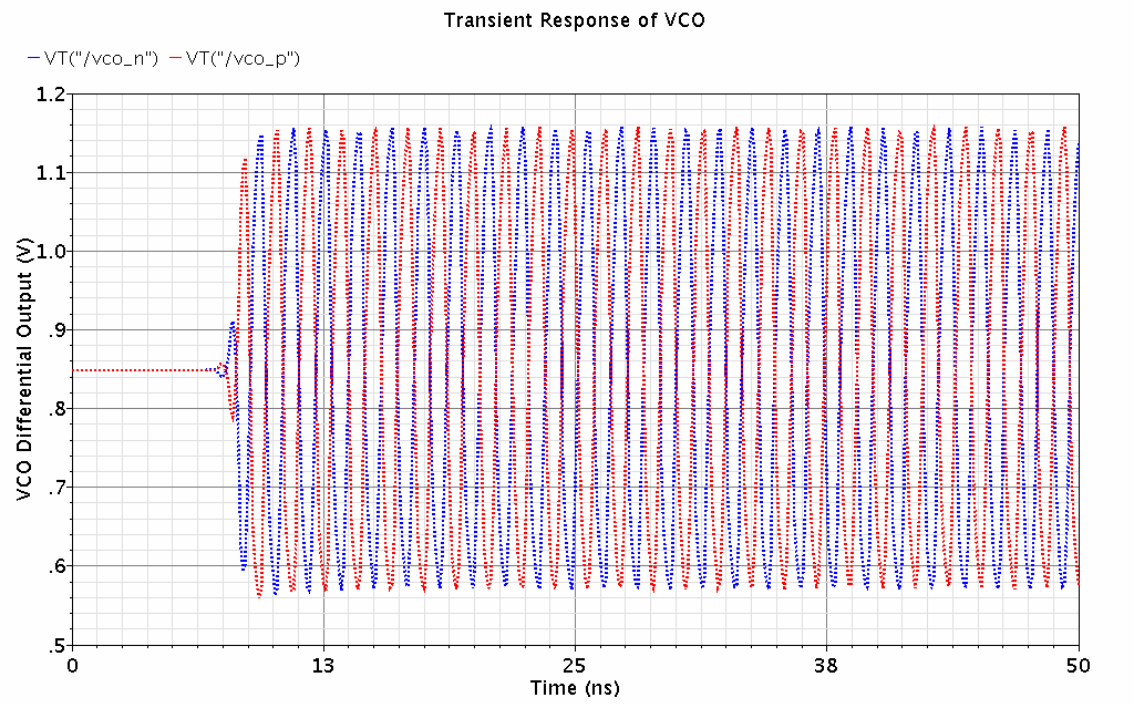

Figure 60: Open Loop VCO transient response

Figure 61 shows the open loop VCO phase noise[47]-[53] output across process and temperature variations at 610 MHz. The worst case phase noise performance obtained is -95 dBc/Hz at 1 MHz offset. Negligible difference between flicker noise and white noise contribution to the phase noise is due to poor flicker noise model of the transistors [54].

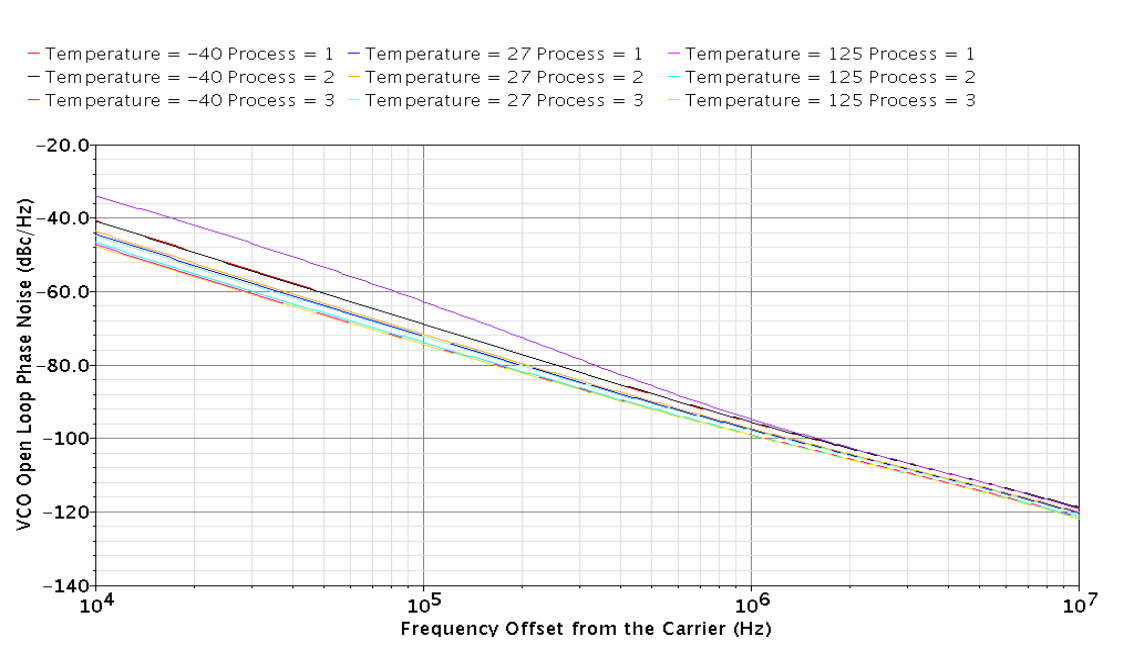

Figure 61: VCO Open Loop Phase Noise

Figure 62 shows the variation of VCO output frequency with change in the VCO input control voltage. The VCO output frequency is 613 MHz at 600mV under nominal conditions, as required.

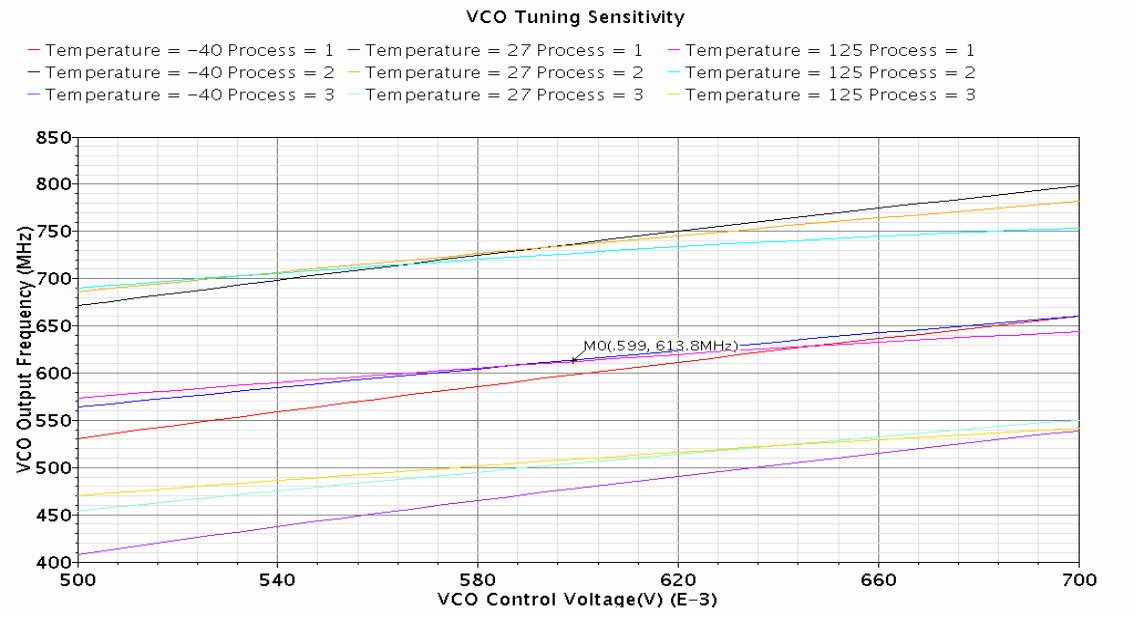

Figure 62:VCO output frequency vs control voltage

Figure 63 shows the variation of the VCO sensitivity for different values of the input control voltage. The nominal value of VCO sensitivity is 483 MHz/V at 600 mV which is close to the theoretically calculated value of 488 MHz/V.

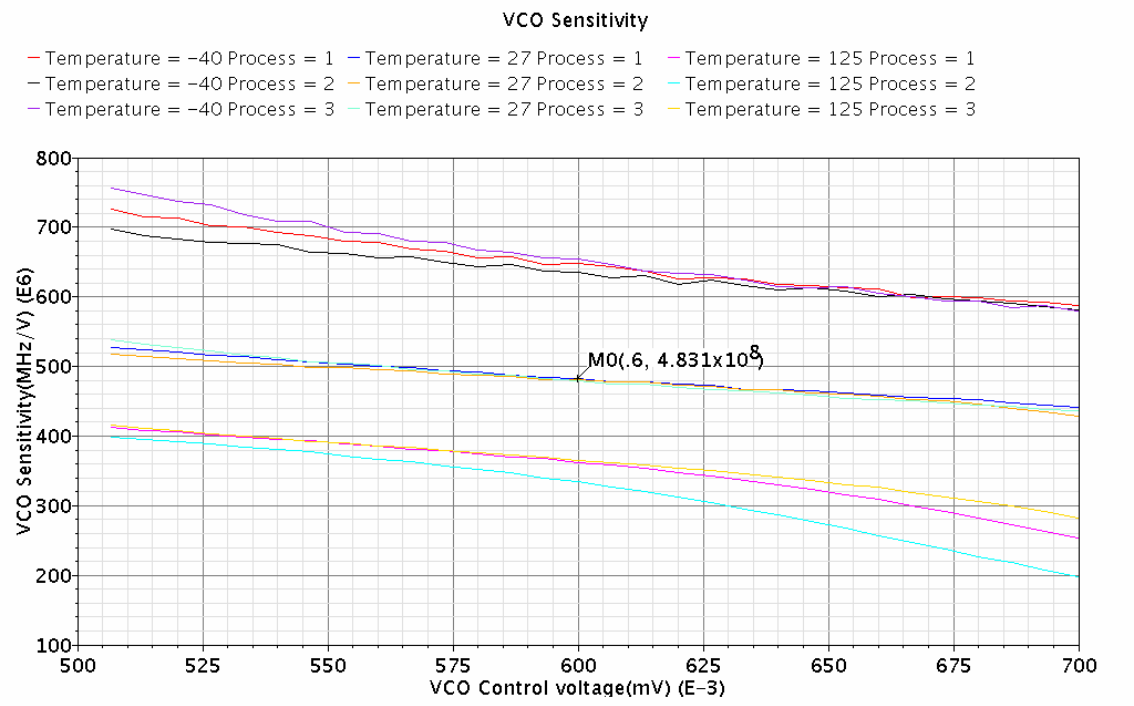

Figure 63: VCO Sensitivity vs VCO control voltage

Figure 64 shows VCO frequency pushing (variation of VCO output frequency with change in the VCO supply voltage) across PVT. The figure shows that the VCO output frequency varies between 450 MHz to 800 MHz under extreme conditions, from the nominal output frequency of 610 MHz. The nominal VCO sensitivity is kept at 500 MHz/V. This is optimal in terms of phase noise (which increases with VCO sensitivity) and for tuning the VCO back to the center frequency with minimal change in the control voltage.

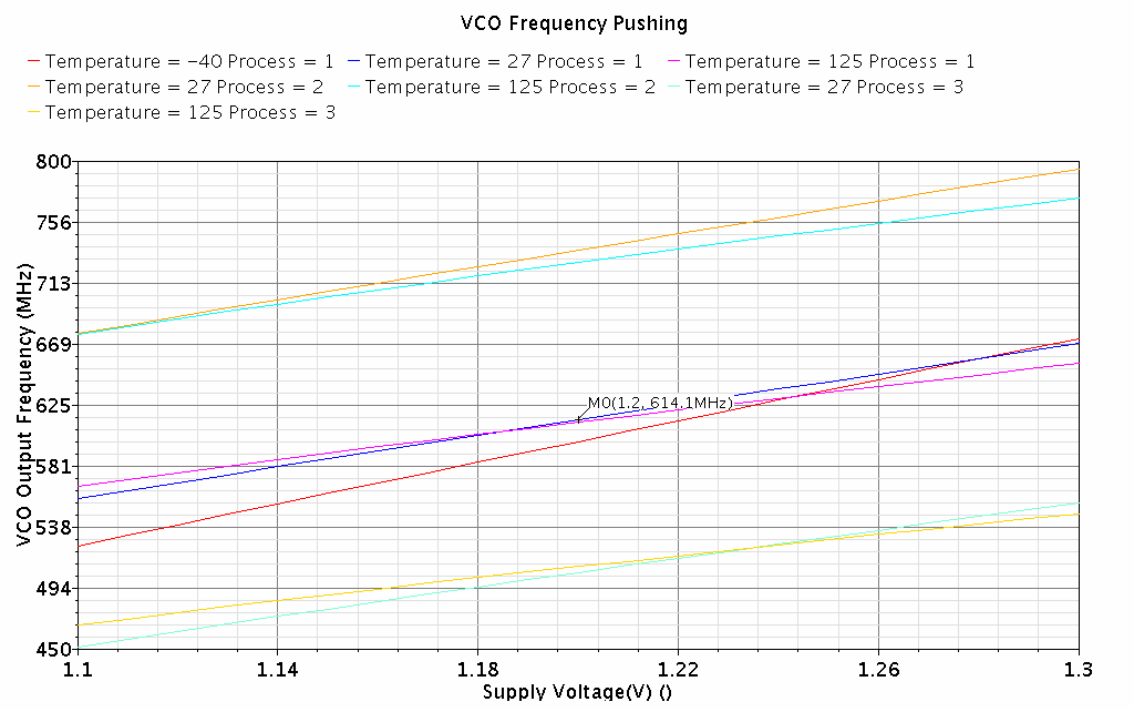

Figure 64: Frequency Pushing

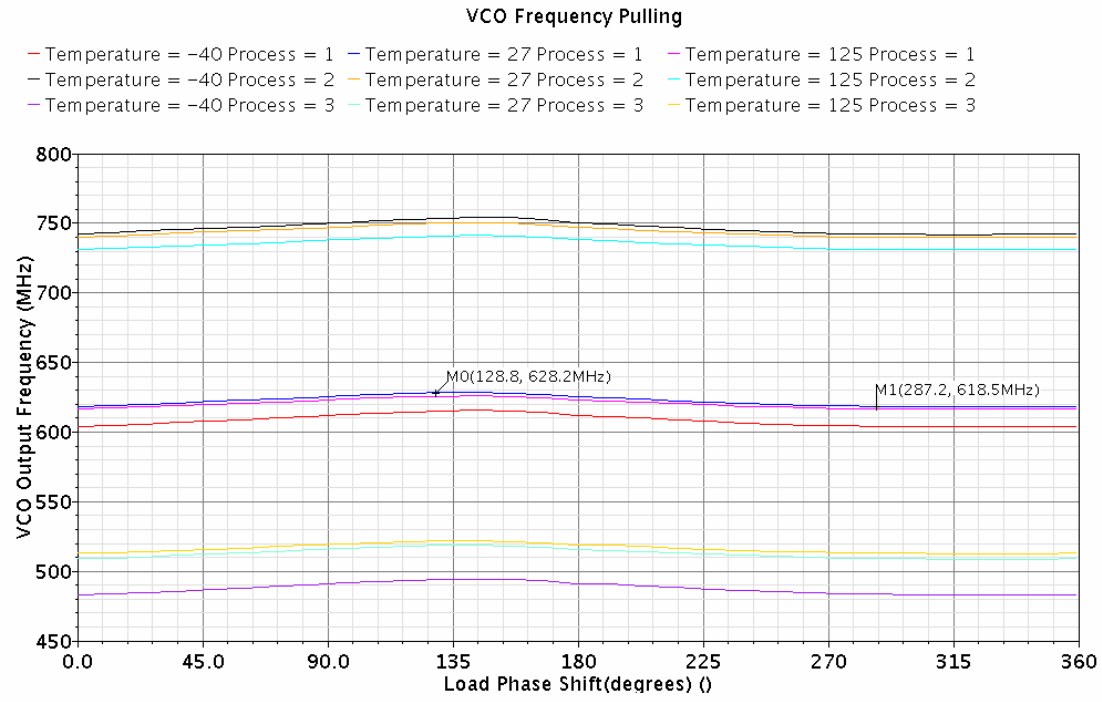

Figure 65: VCO Frequency Pulling

When the VCO output is terminated with a non ideal load it affects the VCO output frequency. This effect is called frequency pulling, which should be minimized as much as possible. Frequency pulling is measured as the change in VCO output frequency due to a load having a nominal 12 dB return loss with all possible phases. Figure 65 shows the simulation of the frequency pulling across different process and temperature. It is observed that the peak-to-peak variation of output frequency is 9MHz maximum for 360° phase shift in the load.

The VCO dissipates both static and dynamic power. Static power is consumed due to leakage and subthreshold current. Dynamic power is consumed due to the switching of transistors when the charging and discharging of parasitic capacitances takes place, and also due to the short-circuit current from the supply to ground when the NMOS and PMOS transistors are momentarily on simultaneously. Figure 66 shows the average power consumption of the VCO as -18.52 dBW or 14 mW.

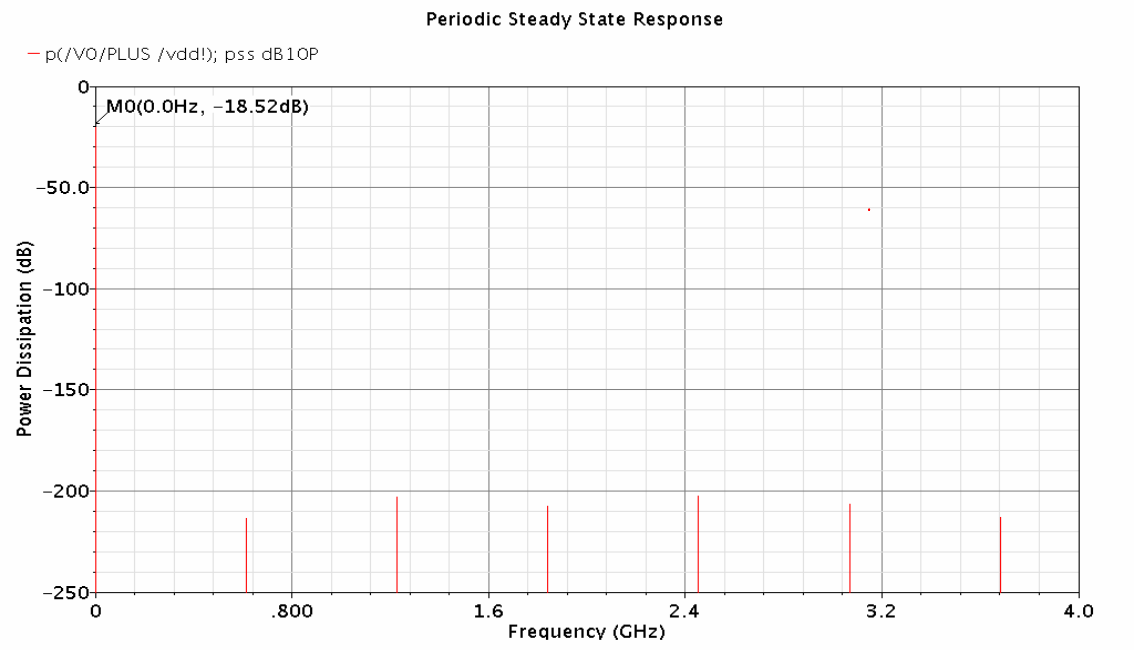

Figure 66: VCO Power Dissipation

Figure 67 shows the output power levels of the VCO. There is substantial power present in the higher harmonics of the VCO output frequency which should be filtered after downconversion by the mixer stage.

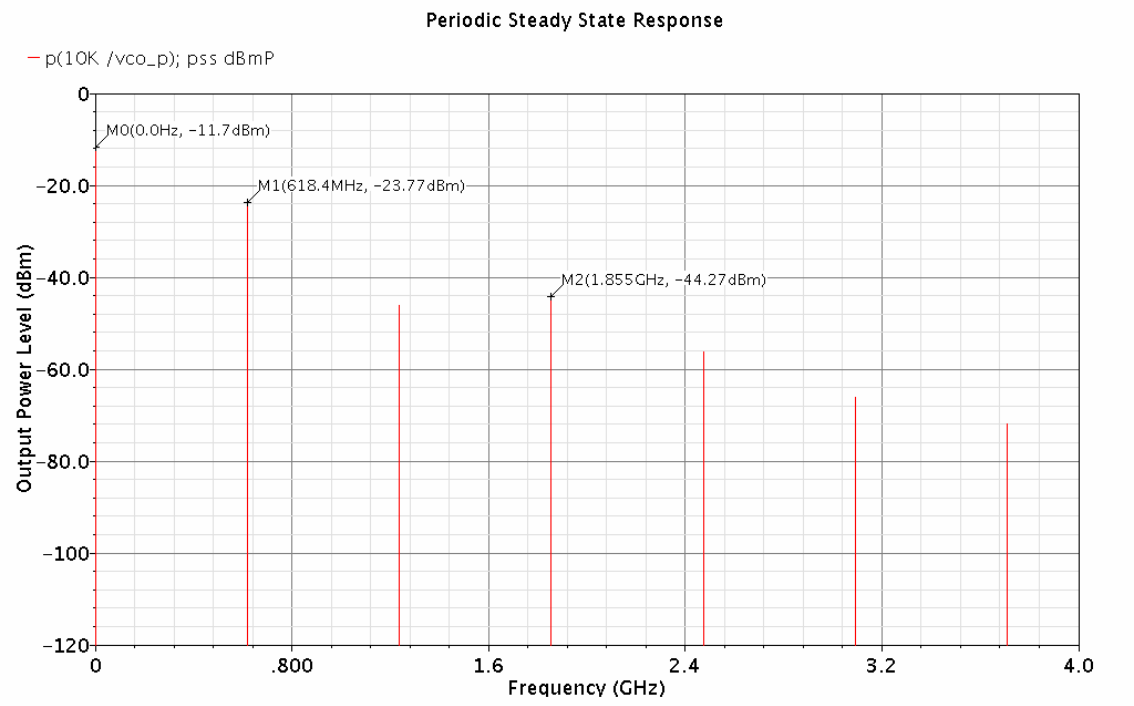

Figure 67: VCO Output Power Level

6.2.6 Frequency Divider

The frequency divider [55][56] in the present design performs a simple divide by 16 operation using a ripple counter with four stages, as shown in Figure 68. Each stage consists of a D Flip Flop with the output connected to the next stage D Flip Flop and also back to the input. This enables the toggling mechanism for the ripple counter.

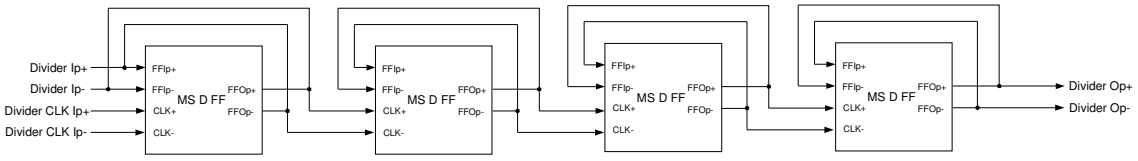

Figure 68: Frequency Divider Block Schematic

Figure 69 shows the implementation of a single stage of the frequency divider. Each stage is implemented using two D latches [57] in a master slave configuration. The master and the slave stage latches are locked to the data at the rising edges of the clock. Also since the master and slave stage have clock inputs inverted with respect to each other they are clocked at opposite phases of the reference input clock. Hence only one stage is active at a particular time.

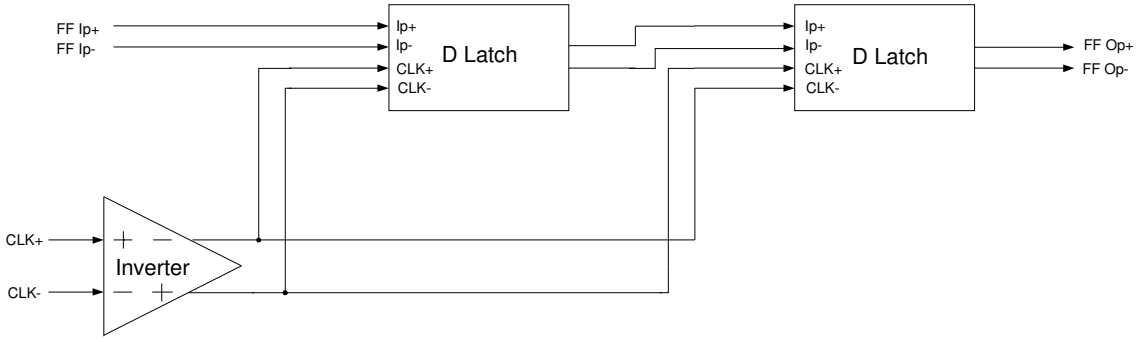

Figure 69: Schematic of Master Slave D Flip Flop

The data is latched to the master stage at the rising edge of the clock to the master input, which is obtained by the slave stage on the falling edge. However since the master and slave stages receive 180° out of phase clocks and the input clock is again inverter through the differential inverter, the data transition at the output of a single stage in the divider occurs at the falling edge of the clock.

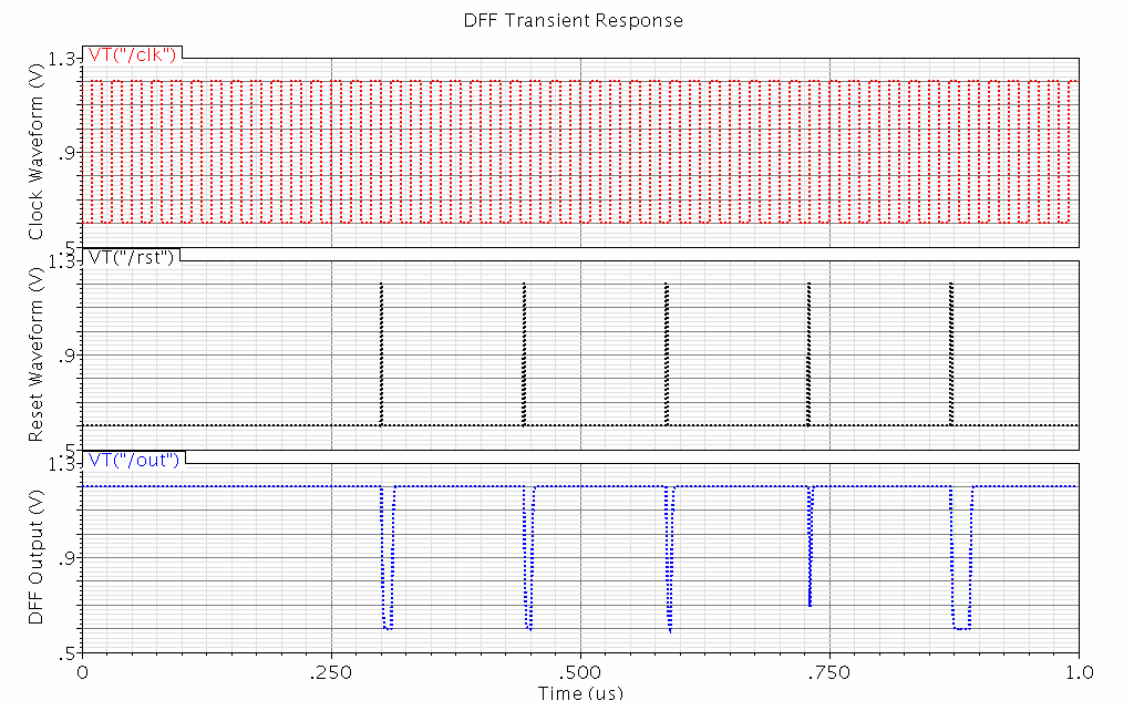

Figure 70: Master Slave DFF transient response

Figure 70 shows the DFF output transient waveforms when the input is clocked at 50 MHz, and a reset pulse frequency is 7MHz. We observe that the output is reset to LOGIC LOW at every rising edge of the RESET pulse, and set to high at the next rising edge of the clock. The DFF has an average propagation delay of 950ps, a rise time = 2.45ns and a fall time = 2.1ns under worst case conditions of process corner = Slow-Slow and temperature = 125°C.

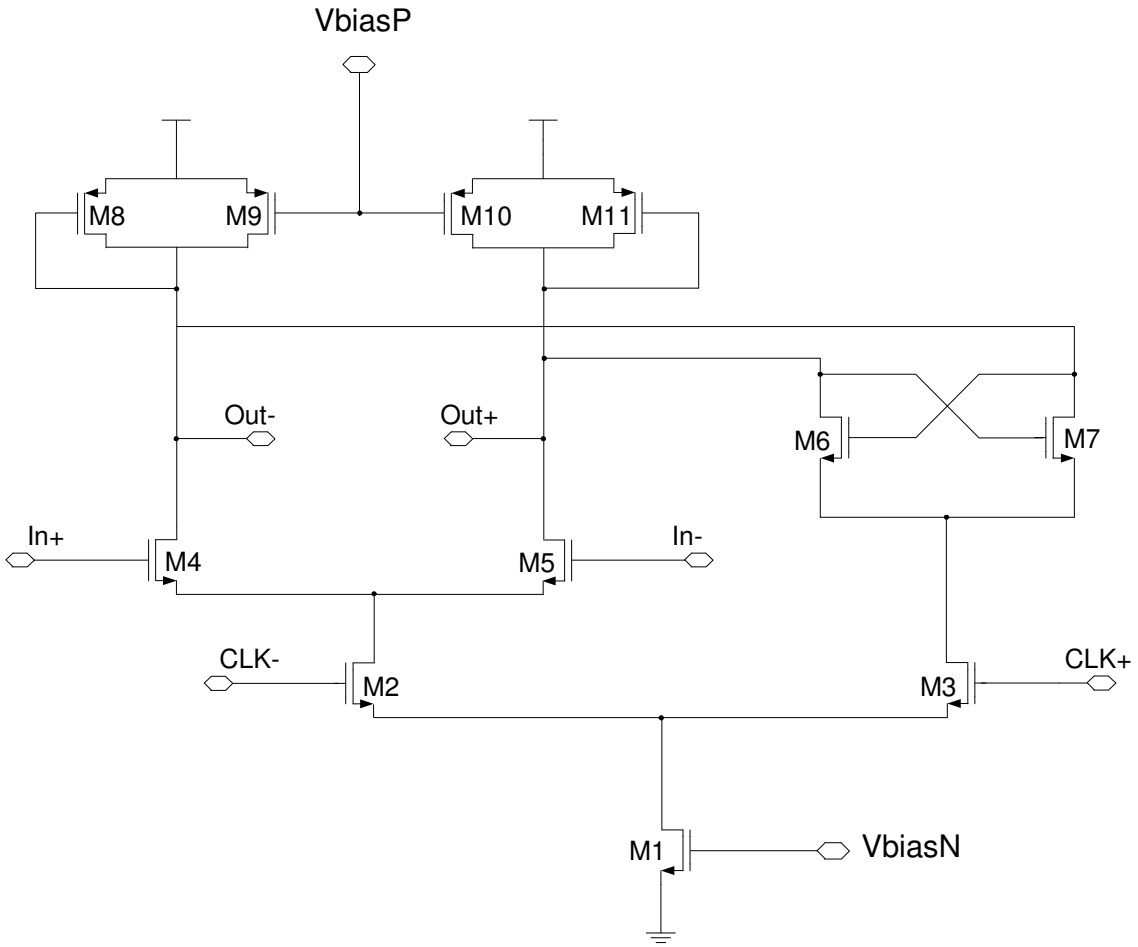

Figure 71: D Latch schematic

Figure 71 shows the schematic design of the D-latch at the transistor level. It is also implemented in a differential manner, with two different functions performed during the two phases of the input clock pulse. When the clock input is low, the differential pair (consisting of output transistors M4 and M5) becomes active and the output follows the input data transitions. When the clock input is high the differential pair is turned off and the transistors M6 and M7 are turned on. M6 and M7 are connected to each other through positive feedback, and so they latch on to the value present at the outputs at the rising edge of the clock pulse.

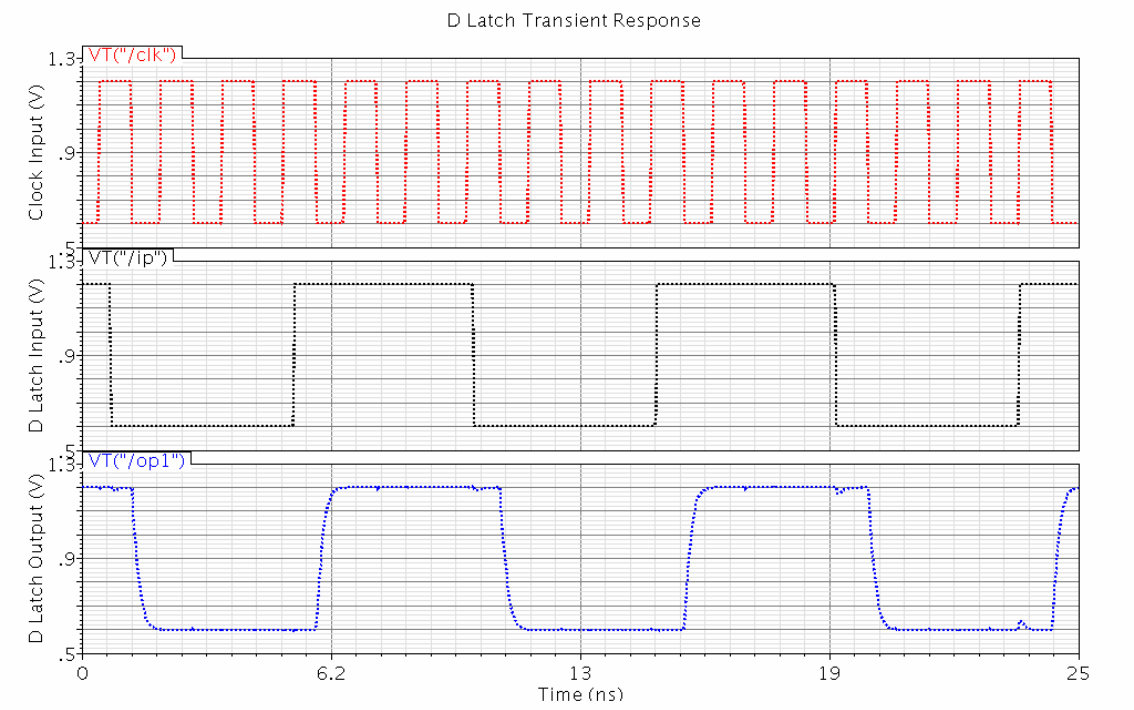

Figure 72: D Latch transient response

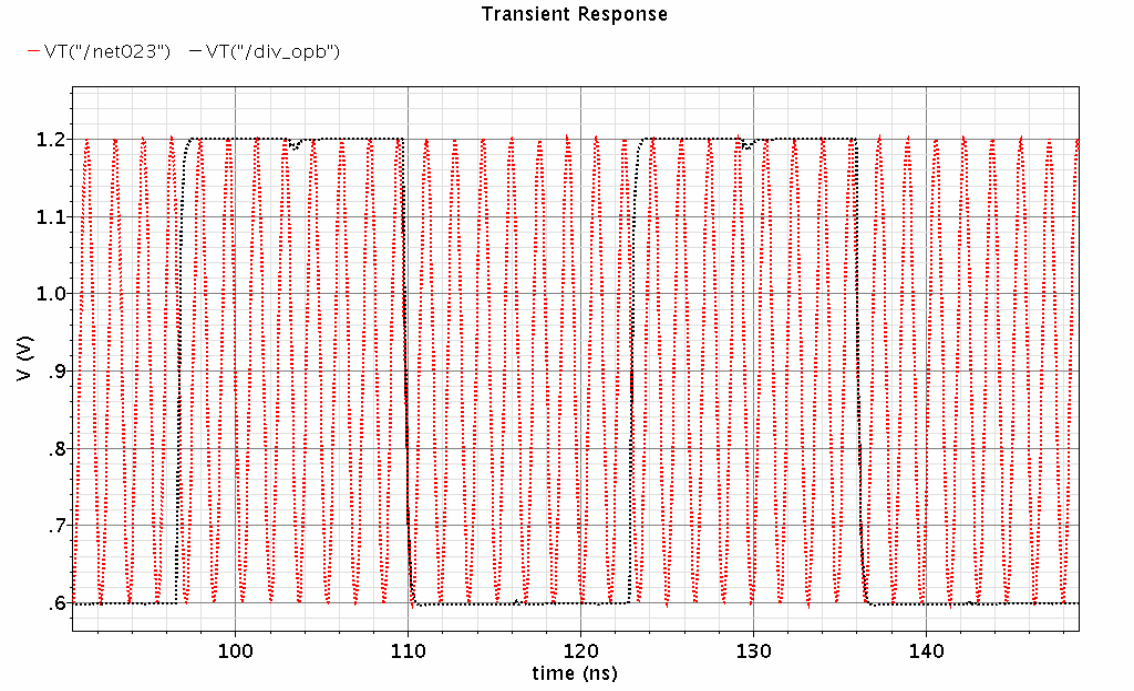

Figure 73: Frequency Divider transient response

Figure 72 shows the D-Latch transient waveforms when the input clock frequency = 650 MHz, the D-Latch input is clocked at 110 MHz. We observe that when the clock is HIGH, the output is latched to the input and when the clock is LOW the output transitions to the same logic level as the input.

Figure 73 shows the data at the input and output of the frequency divider. The data transition at the divider outputs take place at the falling edge of the input with a divide by 16 frequency. The propagation delay is given by 165 ps, rise time = 460ps and fall times = 520ps for worst case conditions given by process = Slow-Slow and temperature = 125°C.

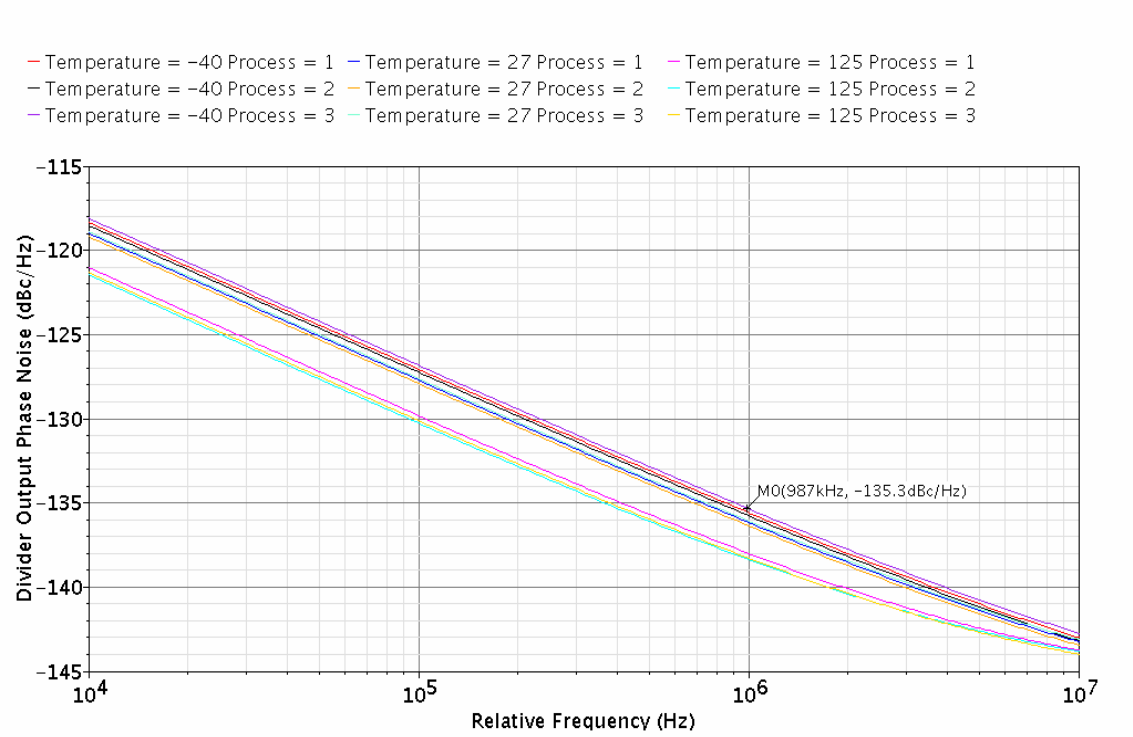

Figure 74: Frequency Divider Output Phase Noise

Figure 74 shows the divider output phase noise simulation result using Spectre RF. The fundamental frequency is measured at the output of the divider and is equal to

38.125 MHz. The divider output phase noise simulated under different process and temperature corners shows a worst case performance of -135.3 dBc/Hz at 1 MHz offset, which is negligible compared to the VCO output phase noise.

6.2.7 CPLL System simulation results

Having designed and simulated each building block of the CPLL, we perform the system level simulation for the CPLL system transistor level design. A transient simulation following by a phase noise simulation of the system was performed and the results are as follows.

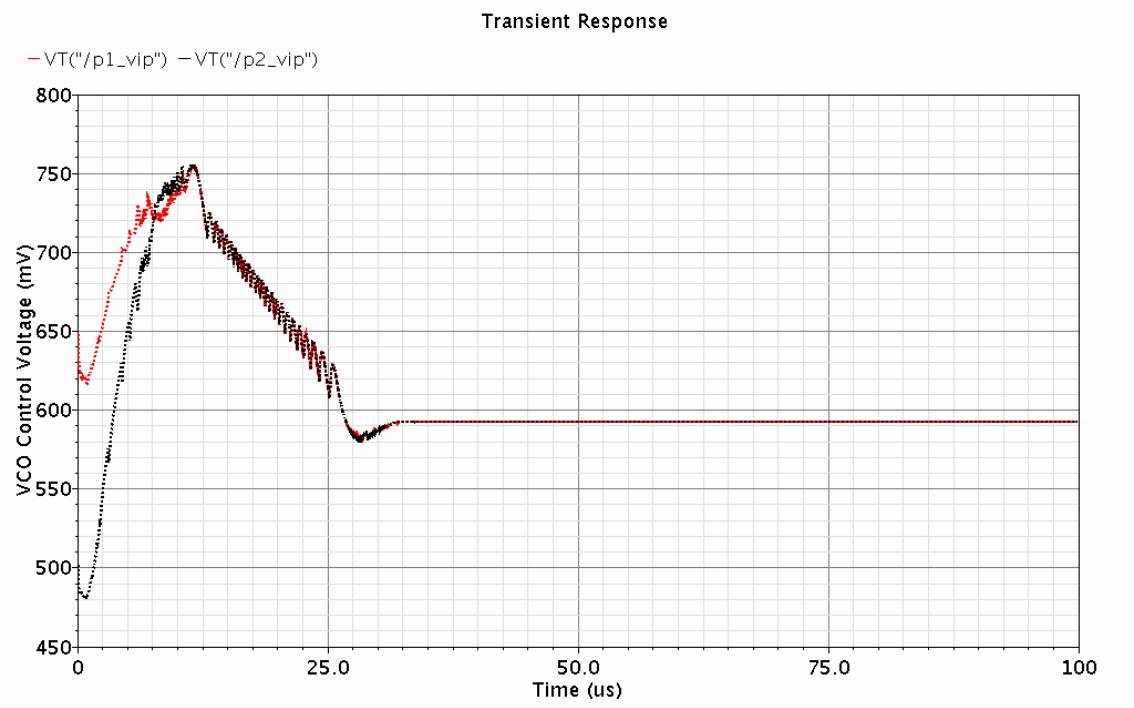

Figure 75: CPLL VCO control voltage input transient response

The CPLL system was initially simulated with a control current of 4µA for 100µs. Figure 75 shows the transient waveforms for the VCO control input voltages over time. We see the waveforms reaching a steady state output of 592.5mV in 25µs.

Figure 76 shows the output phase difference transient which settles to 11.9° at steady state.

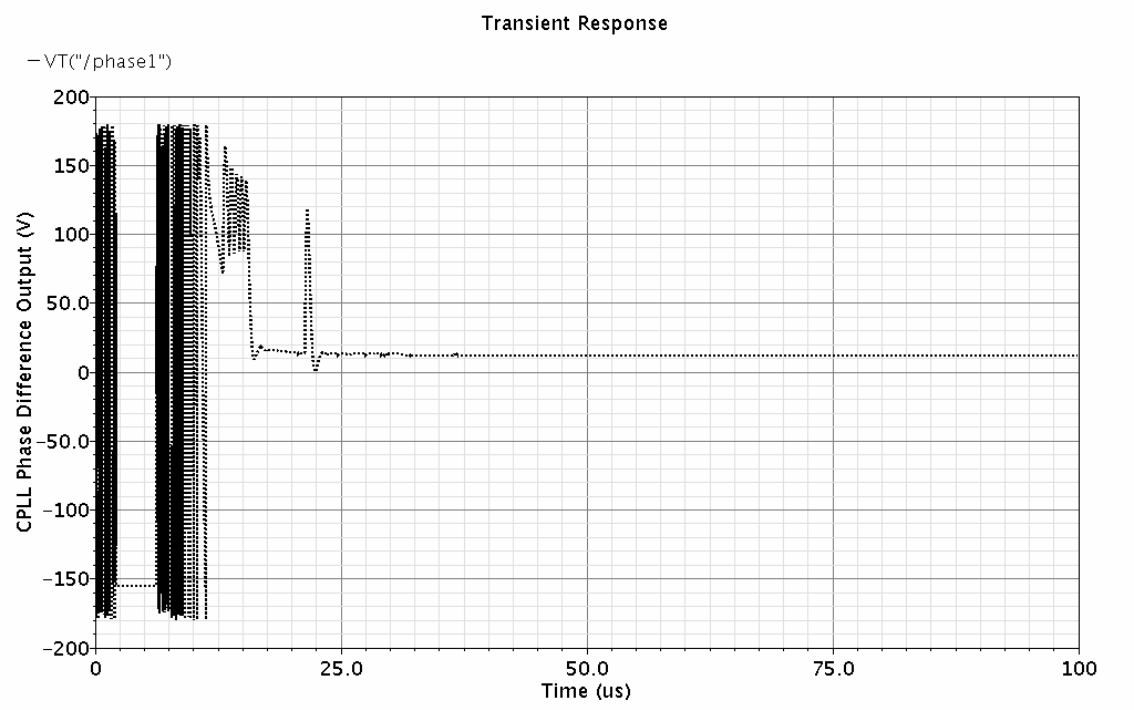

Figure 76: CPLL Phase difference output transient

Figure 77 shows the VCO transient outputs when the control current injected is 54µA.

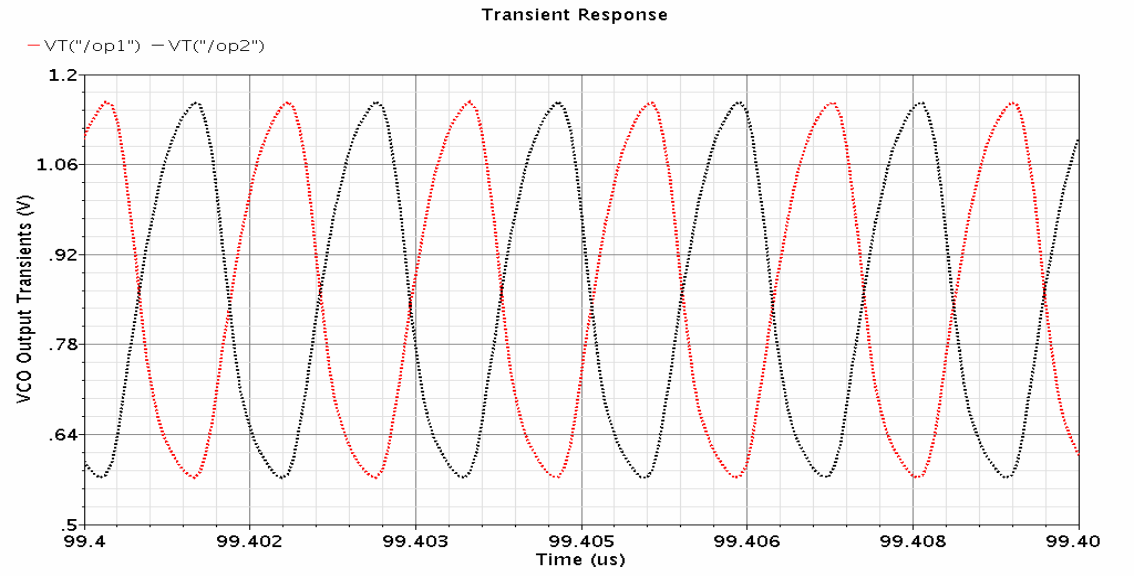

Figure 77: CPLL VCO output waveforms at steady state

Figure 78 shows the phase difference transient output of the CPLL system with 54µA control current. The phase difference generated is 176.6° at steady state.

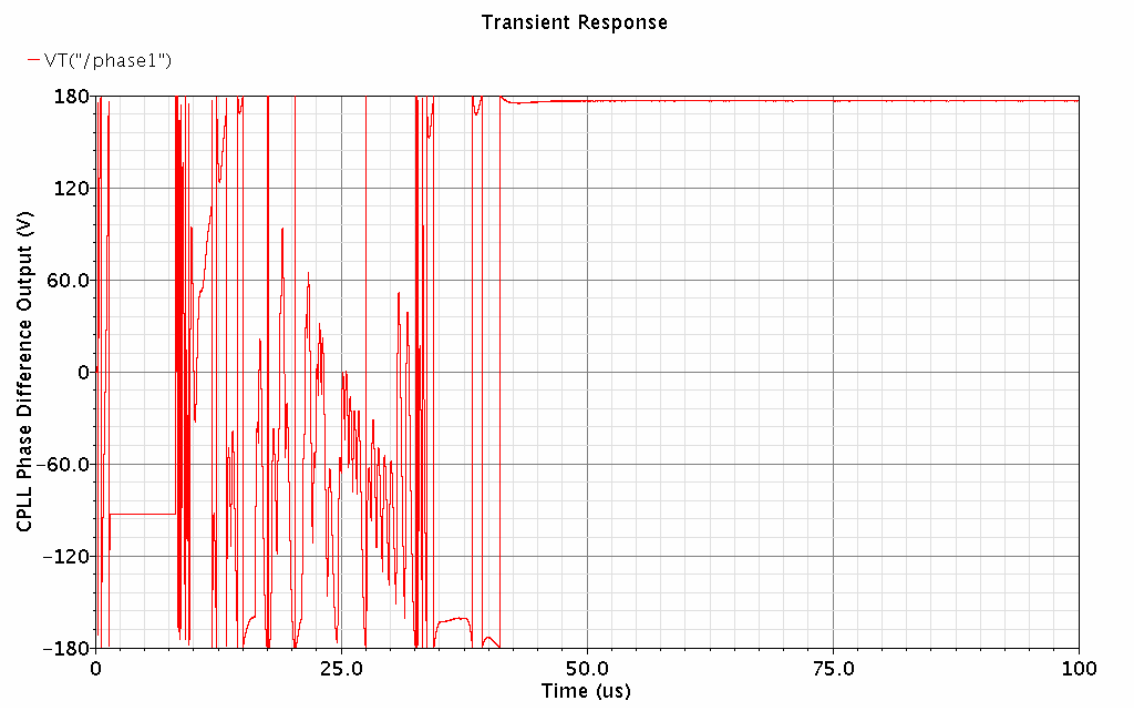

Figure 78: CPLL Phase difference output transient

Figure 79 shows the phase noise simulation of the entire CPLL system which includes both thermal noise and the deterministic noise in the system. The simulation was performed under nominal conditions of process = Typical-Typical and temperature =27°C. The control current injected is 16uA and the output phase difference at steady state is 48°. The CPLL gives a phase noise performance of -95dBc/Hz at 1MHz offset with reference spurs at -75dBc/Hz.

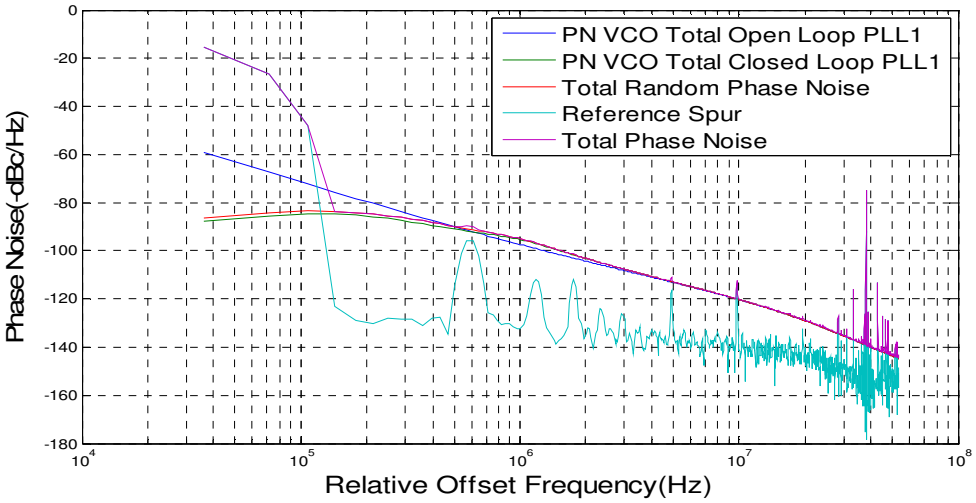

Figure 79: Plot of Phase noise of the CPLL at the transistor level with control current of 16uA and 48 degree phase generation.

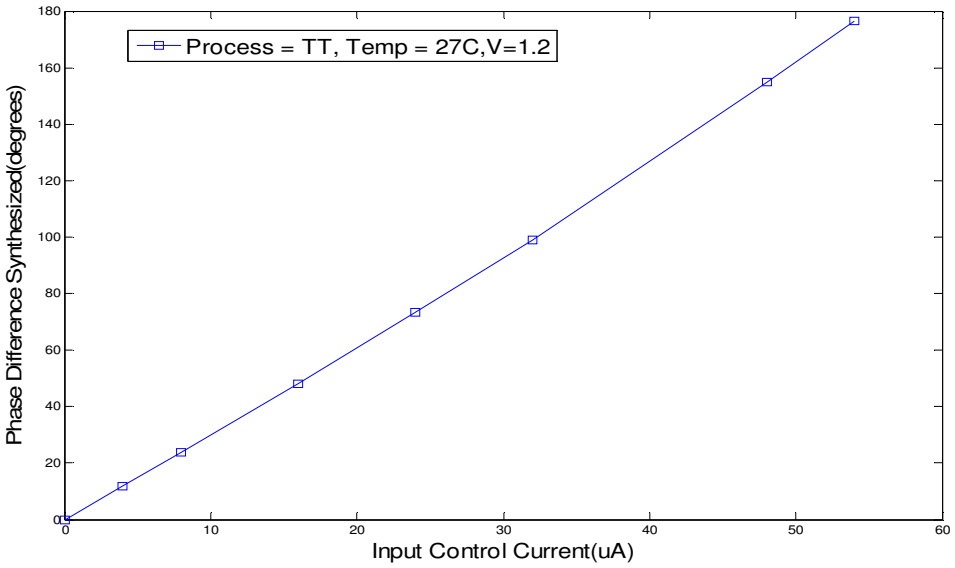

Figure 80: CPLL Phase difference output vs control current

Figure 80 shows the CPLL output phase difference generation versus the control current under nominal conditions. We observe that the output phase generated is linear with respect to the control current which is a critical requirement in the present design.

Figure 81 shows the total phase noise simulation of the entire CPLL system under nominal conditions of process = Typical-Typical and temperature = 27°C. The

control current injected is 54µA and the output phase difference at steady state is 176.6°. The CPLL gives a worst case phase noise performance of -87dBc/Hz at 1.62 MHz offset with reference spurs at -70dBc/Hz.

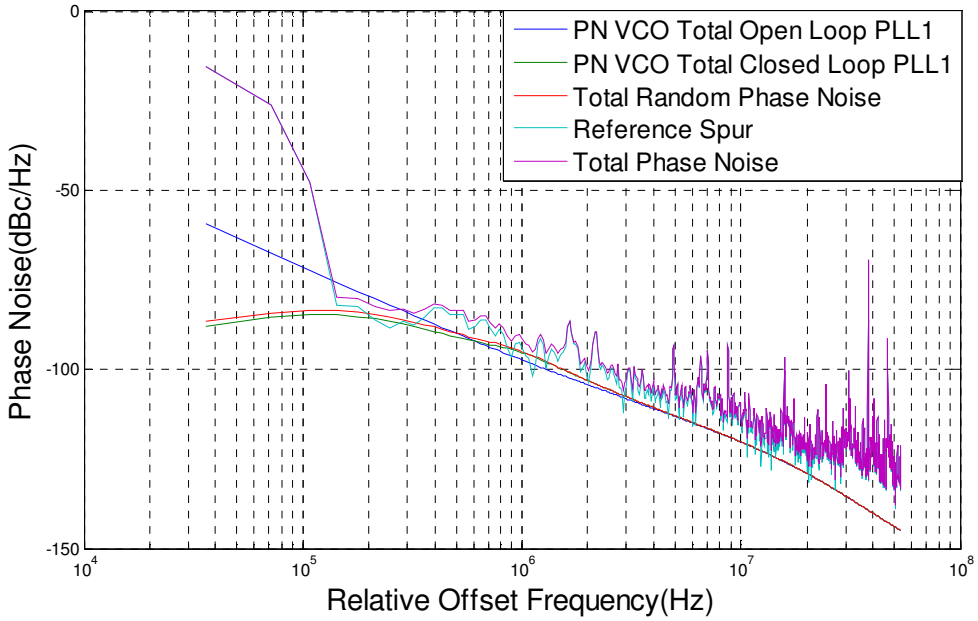

Figure 81: Plot of Phase noise of the CPLL at the transistor level with control current of 54uA and 176.6 degree phase generation

6.3 Summary

This chapter presented the VerilogA modeling of the Coupled PLLs system followed by the transistor-level design of each block, viz., the PFD, CP, VCO and the frequency divider. The PFD and the frequency divider were implemented in Current Mode Logic which is suitable for systems with low noise requirements like the present design. The CP was implemented using DAC architecture with another auxiliary DAC and a DC bias in place of an operational amplifier to maintain the symmetrical voltages between the two branches in the main DAC. Dead zone avoidance was a primary consideration in the PFD/CP design. The VCO was implemented differentially and has

two sub blocks: the V-2-I converter which converts the input loop filter voltage to output current and the Current Controlled Oscillator which converts the input current into the output frequency. Each of the blocks was simulated in Spectre across different Processes and Temperatures. The phase noise of each block was obtained and combined with the deterministic noise to obtain the total Phase Noise of the system. Also the output Phase Difference Synthesized was found to have a linear relationship with the input control current as desired.

CHAPTER 7

CONCLUSION

This thesis presented a novel idea for phase generation in the range of +/-180° using Coupled PLL systems. The wide range of phase synthesis represents double the phase synthesis range possible previously and has been possible due to the use of Phase Frequency Detectors instead of the usual multiplier type phase detectors presented in earlier works. The implementation of this system in CMOS lends itself to easy integration with the base band circuit and makes the system economically feasible. Phased Array systems using the coupled PLL systems for phase synthesis find applications in emerging gigabit wireless applications and also be beneficial in the area of wireless communications through increased range/coverage, improved link quality/reliability, increased capacity of wireless network, interference reduction etc.

To verify the theory a prototype built using off-the-shelf components proved the self-synchronization of the PLL network and its capability to generate a controllable phase difference from -180° to +180° where phase adjustment was done using charge-pumps along with DC control currents. Generating the control currents using current-mode DACs allows for digital phase control.

A phase-frequency synthesizer comprising two PLLs was presented, where the output frequency is accurately set by a reference input signal. The system allows for independent phase and frequency controllability. Mismatch between VCOs has no effect on the synthesized phase or frequency. Phase noise analysis indicates that, similar to a charge-pump PLL, the VCO phase noise is highly attenuated at frequencies near the

carrier. The proposed phase-frequency synthesizer can readily be extended to include 3 PLLs, generating a constant phase progression.

The design methodology for IC design was presented and MATLAB simulations and VerilogA modeling showed achievable system performance in terms of phase synthesis, frequency controllability and phase noise performance of the CPLL system. The transistor-level design was performed for each block and the performance of each was matched against the VerilogA models, both at the block level and also at the system level. The CPLL system is implemented in IBM 130nm process with a 1.2V supply and consumes 40mW of power with a phase noise performance of -88 dBc/Hz for 177° phase generation.

The present work can be extended in different directions depending on whether the objective is the Coupled PLL performance or its applications. In terms of performance, the idea behind the present implementation was to show a practical system implementation which provides linear phase synthesis with proper control, has accurate frequency controllability and also good phase noise performance which are easily provided by the present design. However the phase noise performance of this system can be improved easily by using LC tank oscillators depending on the system requirements. In terms of system applications, the present system can be extended to a three PLL system for phase generation with an improvement in the phase noise performance of 3.25 dB compared to a single PLL system. Also an N PLL system for phase generation can also be achieved as per the MATLAB simulations shown. Also increased frequency of operation can be easily achieved by increasing the frequency divider ratio.

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