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NOVEL METHOD FOR BROADBAND ON-CHIP NOISE CHARACTERIZATION

A Thesis Presented

by

MOHAMMAD GHADIRI-SADRABADI

Submitted to the Graduate School of the
University of Massachusetts Amherst in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

September 2014

Electrical and Computer Engineering

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To my parents and my lovely wife, Shirin

ACKNOWLEDGMENTS

I wish to thank Prof. Bardin for his unconditional support and guidance through every step of this work. I am very fortunate to have had the chance to work with such a knowledgeable person from whom I have learned many things through the past three years.

I would also like to express my gratitude towards my committee members Prof. Robert Jackson and Prof. P. Siqueira, who provided very helpful feedbacks for this thesis.

I would like to acknowledge my colleagues Ajay Subramanian and Ahmet Hakan Coskun for their contribution towards different parts of this work. I would also like to thank Matthew Conte and Sheila Werth for their great help for editing this thesis. I also want to acknowledge all my colleagues, P. Ravindran, S. Chang, M. Yogeesh, M. Conte, M. Ayata, Dr. C.Mohammed, W.Wong and S. Montazeri with whom I have worked through the past three years. They have helped me in both technical and non-technical matters, and have been amazing friends.

This work was supported by DARPA under the YFA program. Any opinions, findings, and conclusions or recommendations expressed in this thesis are those of the author and do not necessarily reflect the views of DARPA.

ABSTRACT

NOVEL METHOD FOR BROADBAND ON-CHIP NOISE CHARACTERIZATION

SEPTEMBER 2014

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A novel method for on-chip noise characterization of mm-wave circuits is presented. Different available methods for noise measurements and requirements for on-chip noise measurements are studied. The Y-factor method is chosen to be the more suitable method for in-situ applications since it does not require absolute measurements. A state of the art CMOS noise source is implemented in 32nm SOI CMOS technology to enable the in-situ noise measurements of a 20-35 GHz reconfigurable low noise amplifier.

Measurement results show that the ENR of the noise source is repeatable enough so that the calibration of the noise source is only required for one integrated circuit. Using different scenarios for the noise figure response of the LNA, the performance of the noise source is evaluated. To the authors' knowledge, this is the first time that an on-chip CMOS noise source is used for in-situ noise characterization of mm-wave frequency circuits.

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CHAPTER 1

INTRODUCTION

The focus of this thesis is the introduction of a state-of-the-art design to enable on-chip noise sensing for millimeter-wave applications. Explicitly, the following contributions will be discussed: 1) the design of a CMOS on-chip noise source suitable for mm-wave frequency applications and 2) the demonstration of a built-in self-test (BiST) for noise in 32nm CMOS technology.

The outline of the thesis is as follows:

Chapter 1- Motivation and Theory: The motivation for developing an on-chip noise measurement system is presented. The theory for noise measurements and on-chip built-in self-test, including different available methods for noise measurement, is discussed.

Chapter 2- Circuit Design: Requirements and challenges for the implementation of the on-chip noise source design are presented. In addition, the circuitry required for coupling the noise source to the device under test (DUT) is reported along with a general description of a DUT used for used to validate the proposed concept.

Chapter 3- Measurement Procedure and Results: A step-by-step measurement and processing procedure is described. In addition, measurement results of the fabricated integrated circuits are presented. Results include statistical analysis for noise measurements using the proposed method and demonstrate the accuracy of the proposed technique.

1.1 Challenges and advances in millimeter wave circuit design

The growing demand for high data rate communication systems has inspired significant research in the design of circuits operating in the millimeter-wave (mm-wave) frequency regime. The push to achieve faster data transfer has resulted in improvements in all aspects of communication systems. Demonstration of mm-wave integrated circuits has been enabled by the development of technology nodes with devices operating at hundreds of GHz. As a result, monolithic microwave integrated circuits (MMICs)— which include circuit blocks such as low noise amplifiers (LNAs), mixers, and power amplifiers— are now commonly available in the mm-wave frequency range [1–5]. Despite significant progress in this field, there are still many challenges faced by circuit designers, many of which are unique to a given technology platform.

Historically, integrated circuits fabricated in technologies such as III-V MESFET/HEMTs have been used for mm-wave applications, but the increasingly fast scaling of CMOS is enabling the use of CMOS technology for high frequency applications [1]. Generally speaking the reduction of feature size improves the f_t/f_{max} of the device. The scaling of CMOS has led to FET devices with f_t and f_{max} in hundreds of GHz, which has in turn enabled the demonstration of CMOS mm-wave integrated circuits [1]. While technology scaling has improved device speed, it also has resulted in higher variation in device parameters [6, 7]. This variability is especially troublesome in nanometer-scale CMOS technologies and makes circuits susceptible to post-fabrication failure. Nevertheless, the incrementally free number of digital transistors available in CMOS technologies enables the implementation of architectures with extensive on-chip calibration techniques to increase the yield of mm-wave CMOS ICs.

1.2 Built-In Self Test for RF applications

The increasing variation in device parameters due to continued scaling has become increasingly significant as with feature sizes now well smaller than 100 nm [7]. The associated variations can be from die to die or device to device on the same die and result in high uncertainty of the device performance after fabrication [7]. In addition to process variation, the decrease in supply voltage associated with lower break down voltage of scaled devices makes circuits more sensitive, further increasing the risk of failure [8]. Finally, the change in the temperature can significantly change device parameters and degrade the performance of an integrated circuit [7]. In the case of CMOS technology, in addition to variations, another significant issue is the lack of mm-wave models with sufficient fidelity to accurately predict the average performance of fabricated designs. This shortcoming is a result of the fact that nanometer CMOS technology platforms are mostly catered to digital applications. This can be worse in the case of noise models since they are not considered in the typical digital design flow.

One possible method for the mitigation of process, voltage, and temperature (PVT) variability and lack of suitable RF models is the use of on-chip calibration and reconfigurable systems [9–11]. In this approach, as shown in Figure 1.1, reconfigurability is built into the main RF system while the addition of a built-in self-test system and a signal processing scheme enables the measurement and optimization of different metrics of the system. Figure 1.2 shows an example of such a system that is used to improve the power added efficiency (PAE) of a power amplifier (PA) designed for mm-wave applications. There are several test schemes to sense the temperature, DC bias, and the RF performance of the PA. Signals collected from these sensing blocks are processed with an on-chip digital core, which then tunes separate parts of the PA to achieve the desired performance.

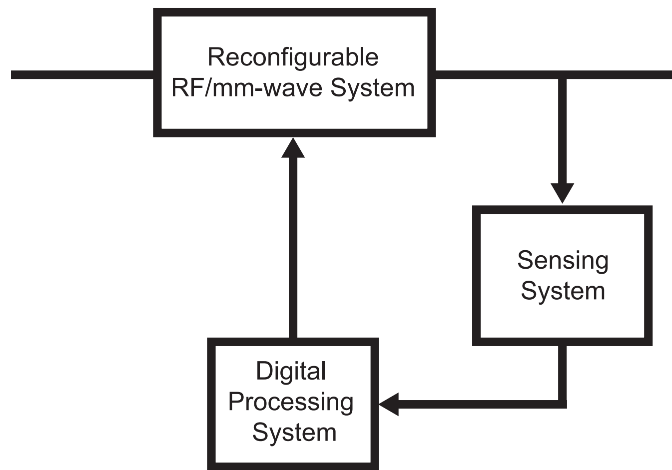


Figure 1.1. On-chip calibration and reconfigurable system block diagram

To enable the use of on-chip calibration an optimized BiST is required. The capacity to implement the additional circuitry required for this BiST gives nanometer CMOS technologies a unique advantage over other technology platforms. As a result, the employment of extensive on-chip calibration should help to overcome such issues as variation and unreliable RF models, and improve the performance of CMOS integrated circuits.

Development of a reliable BiST system requires a test signal presented to the device under test (DUT) and a way to evaluate the response of the DUT to this signal. Recently reported systems use BiST to adjust power amplifier efficiency [9] , image rejection [10] and phase [11]. However, despite the importance of noise performance, there has been limited published research on on-chip noise sensing [12]. In this work a new detailed step by step method is presented which can be used for the built in self test of noise.

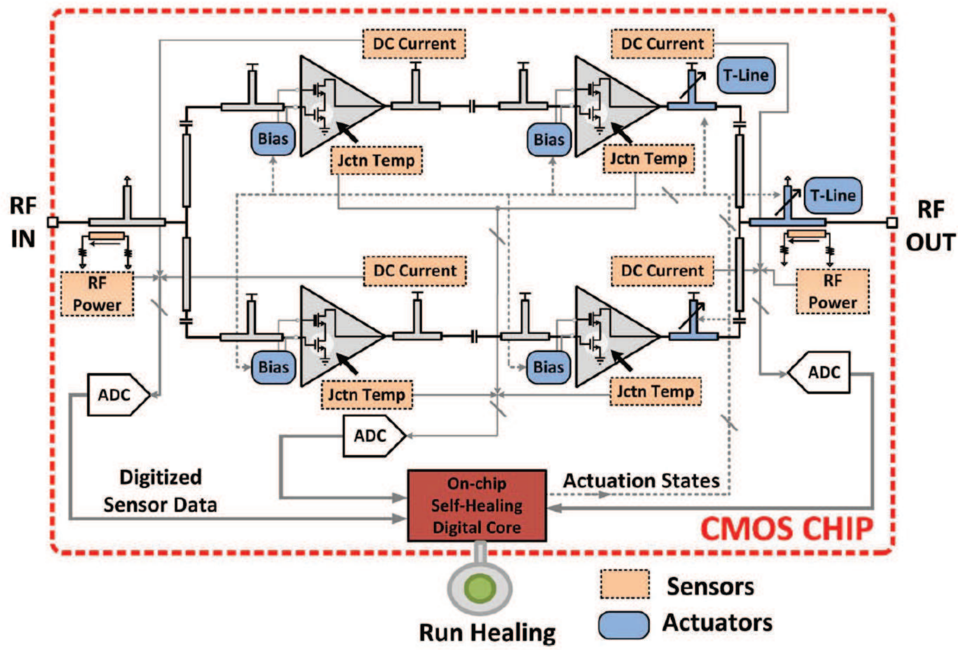


Figure 1.2. Block diagram of a Self-Healing power amplifier designed for mm-wave applications. Reproduced from [9] © 2013 IEEE.

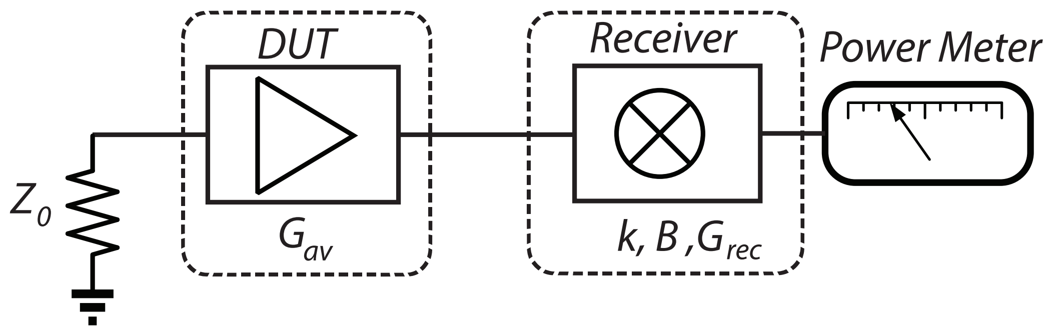


Figure 1.3. Block diagram of a conceptual cold source noise measurement. G_{av} is the available gain of the DUT terminated in Z_0 and B, G_{rec} are the same as defined in Equation 1.2.

1.3 Standard Noise Measurement Techniques

The two main techniques that are widely used for noise measurements are the cold source [13] and Y-factor methods [14]. In the cold source method, the output power of the DUT is measured while its input is terminated in a known impedance. Assuming a perfect output match and a noiseless power measurement system, the noise factor of the DUT can then be found using [15]:

$$F = \frac{N_c}{T_a k B G_{rec} G_{av}(\Gamma_{sc})} \tag{1.1}$$

where N_c is the measured output power, k is the Boltzmann constant, T_a is the ambient temperature, BG_{rec} is the gain bandwidth product of the receiver system and $G_{av}(\Gamma_{sc})$ is the small-signal available gain of the DUT measured with the required input termination impedance. The gain bandwidth product can be measured by connecting a noise source directly to the receiver system and making a hot (noise source enabled) and cold (noise source disabled) measurement as,

$$BG_{rec} = \frac{N_{h,rec} - N_{c,rec}}{k(T_h - T_0)}. \tag{1.2}$$

The available gain of the DUT terminated in the load can be found by S-parameter measurements. The cold source method is widely used to measure noise, but a challenge is to make precise absolute measurements of GB_{rec} and $G_{av}(\Gamma_S)$, which can be quite difficult and may require several calibrations.

The Y-factor method is an alternative way to characterize the noise performance of a system.Figure 1.4 shows a block diagram of a Y-factor noise measurement setup. The Y-factor is defined as:

$$Y \equiv P_{HOT}/P_{COLD} = \frac{kGB(T_e + T_{hot})}{kGB(T_e + T_{cold})} = \frac{T_e + T_{hot}}{T_e + T_{cold}}, \tag{1.3}$$

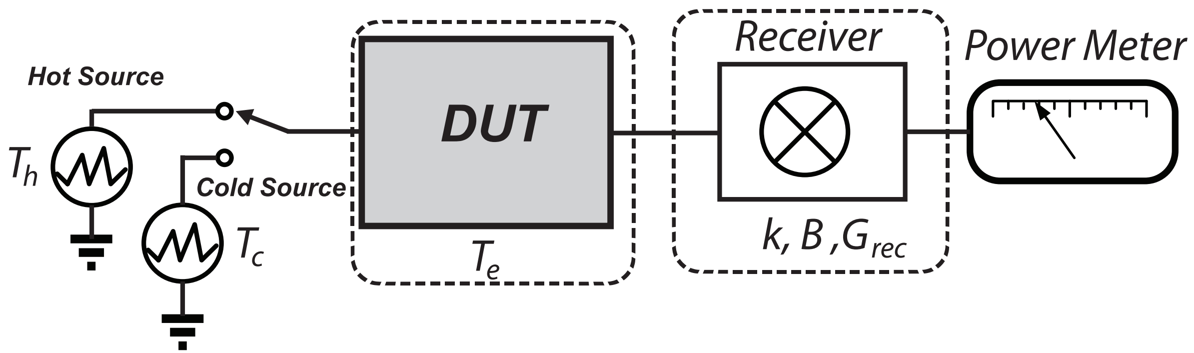


Figure 1.4. Conceptual Y-factor measurement setup

where T_e is the noise temperature of the DUT, T_{hot} is the noise temperature of the excess noise source, and T_{cold} is the ambient temperature which is usually around 290 K. When T_{hot} is known, one can measure the Y-factor and use Eq. 1.3 to find T_e. Hence, for a known T_{hot} of a noise source, only two measurements are required to find the noise figure. The benefit of this method is that only relative measurements of power are required and not the absolute values. The ratiometric measurement makes it more convenient to achieve reliable measurement results.

1.4 On-Chip Noise Measurement

Despite all the research towards implementing BiST systems, little work aimed at enabling on-chip noise characterization has been carried out. Several authors report noise source designs [16–20], however most of these designs are more suitable for the cold source method or for characterizing cryogenic devices, since in cryogenic applications, device noise temperature is much lower. In [19], a GaAs device noise matched to 50 ohms, using inductors, can produce a constant 50 K noise temperature at 1.4 GHz, and its temperature can be controlled as a function of DC bias. A similar result was reported in [18], where a TriQuint 0.5μm GaAs pHEMT device was used to achieve 90K at 1.3-1.5 GHz. In another work recently published by Diebold [21], an active hot and cold noise source for frequencies

between 75 to 110 GHz was presented. In this work an active 100nm MHEMT device is used to produce noise temperatures at 860 K (hot state) and 230 K (cold state). This noise source is useful for calibration of noise power in radiometer applications.

For accurate noise measurements at mm-wave frequencies, noise sources with noise temperatures on the same order of typical amplifier noise temperature values (around 1000 K) are required. Although there are some proposals for noise sources with higher excessive noise ratios (ENRs), such as using SiGe BiCMOS devices in avalanche mode [22] and using MOS devices in saturation [23], with the exception of the W-band noise source, reported after the completion of this work [21], to the author's knowledge there has been no demonstration of such noise sources for mm-wave applications.

Realization of a fully integrated on-chip noise measurement system consists of the development of a noise source, a receiver system to down convert the high frequency signal, and then a way to process the received signal. Figure 1.5 shows a block diagram of a conceptual on-chip noise sensing system. The noise source needs a way to be coupled into the input of the DUT, while not affecting its noise and gain performance. As an example, using lossy switches for connecting the noise source to the DUT would degrade the noise and gain performance of the LNA. The range of measurable Y-factors is related to the noise floor of the receiver system. Hence, the receiver system needs to have a reasonable NF such that there is enough dynamic range for the noise characterization.

Recently Tang reported using the cold source method to sense the noise performance of a 60 GHz 4Gb/s radio-on-a-chip [12]. While promising final results were shown in the context of a larger system, a detailed description of the noise measurement performance was not provided. Precise absolute measurements are difficult on chip and make the use of the cold source method rather challenging. The ratiometric nature of Y-factor method makes

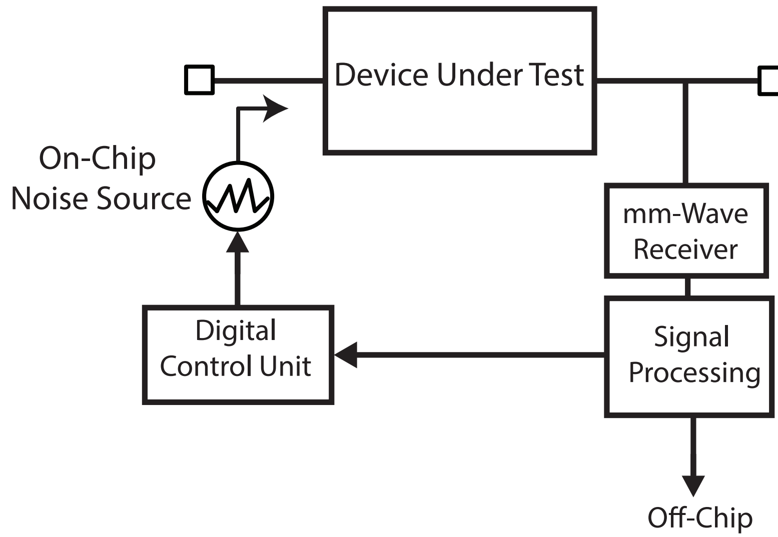


Figure 1.5. Block diagram of a conceptual on-chip noise sensing system

it easier to make precise noise measurements without the need of absolute measurements of gain and bandwidth.

For several applications only the optimization of the noise performance is required and not the absolute value of the noise figure. For these applications using the Y-factor method, the noise can be optimized without requiring the knowledge of T_{hot}. From Equation 1.3 it can be seen that:

$$T_e = \frac{T_{hot} - YT_{COLD}}{Y-1} \qquad , \qquad \frac{\partial T_e}{\partial Y} = -\frac{T_{hot} - T_{cold}}{(Y-1)^2}. \tag{1.4}$$

This shows a monotonic relation between T_e and Y. Consequently, in order to minimize noise temperature of a system it is enough to maximize Y without knowledge of T_{hot}. This is important since finding T_{hot} may require extra calibration steps which can be omitted if the absolute noise values are not required. This work focuses on the design of a noise source suitable for on-chip noise measurements with the use of Y-factor method. The detailed explanation of design decisions is presented in Chapter 2 and then measurement results of this

design fabricated in IBM 32nm CMOS technology are reported in Chapter 3.

CHAPTER 2

ON-CHIP NOISE CHARACTERIZATION

Development of built-in self-test for noise at mm-wave frequency requires the implementation of an on-chip noise source and an on-chip spectrum anlayzer. On-chip spectrum anlyzers have already been demonstrated by several authors [12, 24–27]. Hence, the focus of this thesis is on the design and implementation of an on-chip noise source suitable for mm-wave applications. The design of the noise source also includes the demonstration of circuitry required for the coupling of the source to the device under test (DUT). As mentioned in Section 1.4, the Y-factor method has the advantage of only requiring relative measurements and as a result can be a better choice for on-chip applications in comparison to alternative approaches.

In this chapter, different sources of error and their effects on noise figure measurements made using the Y-factor method are discussed. A single FET CMOS noise source is simulated and studied and it is shown that the ENR of such a source is insufficient for use in the noise measurement of mm-wave amplifiers. Moreover, the design and implementation of a state-of-the-art CMOS noise source, suitable for the in-situ noise characterization off mm-wave low noise amplifiers, is presented. The RF switch used for connection of the noise source to the DUT as well as the DUT are also presented in this chapter.

2.1 Noise source requirements

Employment of the Y-factor method for on-chip noise measurements requires a noise source with high enough ENR to achieve easily measurable Y-factors. The minimum required Y-factor is mainly set by the sensitivity and stability of the receiver system. Although a higher Y-factor means more dynamic range in the overall noise measurement, very high Y-factors can also increase the error in T_e calculations. To set the requirements on the noise source, any significant source of error resulting in uncertainty of noise measurements should be considered. Understanding the sources of error can enable ways to reduce the effect of each of these on the noise figure measurement.

2.1.1 Sources of Error in T_e Measurements Using Y-factor

The error in measurement of a quantity that is a function of multiple variables can be found with respect to the error of each of the variables using a Taylor series expansion [28]. As an example, the error in measurement of $Y = f(x_1, x_2, ..., x_n)$ can be approximated by ignoring higher order terms as,

$$|\Delta Y| = |\frac{\partial f}{\partial x_1}|.|\Delta x_1| + |\frac{\partial f}{\partial x_2}|.|\Delta x_2| + ... + |\frac{\partial f}{\partial x_n}|.|\Delta x_n|, \tag{2.1}$$

where $\Delta x_1, \Delta x_2, ..., \Delta x_n$ are the error for the measurements of variables $x_1, x_2, ..., x_n$. Using Equation 2.1 and $T_e = (T_{hot} - YT_{cold})/(Y - 1)$, the impact of error in measurement of T_{hot} on T_e can be understood independently.

One source of error in the extraction of T_e, is the error in the value of T_{hot}. Assuming that Y and T_{cold} are precisely known, the error in measurement of T_{hot} is equal to the error in the T_{ENR} where $T_{ENR} = T_{hot} - T_{cold}$. It can be shown that the relative error in noise temperature measurement as a function of relative error in T_{ENR} is equal to,

$$\frac{\Delta T_e}{T_e} = (1 + \frac{T_{cold}}{T_e})\frac{\Delta T_{ENR}}{T_{ENR}}. \tag{2.2}$$

This shows that the propagation of error in T_{ENR} is related to the ratio of T_{cold}/T_e. For the mm-wave frequency range where typical T_e values are around 1000 K, having T_{cold} at the ambient temperature creates an acceptable ratio. However, for different frequency ranges or ultra low noise applications with lower T_e values, noise sources might require active cold loads or cryogenic terminations. Active cold loads are devices with effective noise temperatures less than their ambient temperatures, an example of such noise sources is presented in [21].

In addition to errors in measuring T_{hot}, another major source of error in T_e measurements is related to error in the Y-factor measurement. To study this effect, using Equation 2.1 it can be shown that, the contribution from the Y-factor measurements on T_e is,

$$|\Delta T_e| = |\frac{T_{hot} - T_{cold}}{(Y-1)^2}||\Delta Y| \tag{2.3}$$

and the relative error in T_e can be found as,

$$|\frac{\Delta T_e}{T_e}| = |\frac{(1 + \frac{T_{cold}}{T_e})}{1 - \frac{1}{Y}}| \times |\frac{\Delta Y}{Y}|. \tag{2.4}$$

Figure 2.1, shows the percentage of relative error in T_e as a function of Y for constant values of $T_e = 1000K$, $T_{cold} = 290K$ and $\Delta Y/Y = 0.1$. Figure 2.1 shows that higher Y-factor values decrease the effect of relative error of Y in relative error of T_e. This means for a given T_e, higher noise source ENR helps to reduce the error in noise measurements using the Y-factor method. However very large values of T_{hot} can dominate the Y-factor and create more errors in measurements of T_e. This suggests that for successful noise measurements in mm-wave frequency range the noise source should be able to produce T_{hot} values higher than 1000 K throughout the band.

Another important requirement on the noise source is that it should present the same exact impedance termination in both cold and hot states. Inconsistency of the termination between the two different states can result in significant error in the overall noise measure-

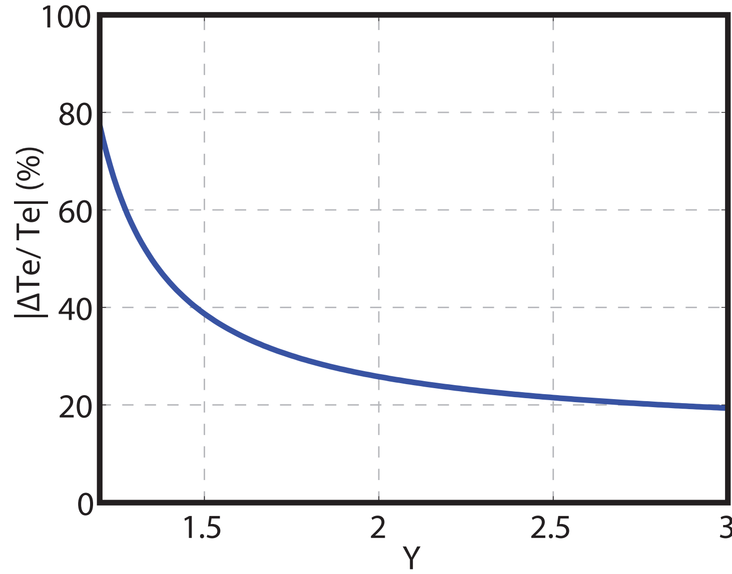


Figure 2.1. Percentage of relative error in T_e measurements as a function of Y-factor for constant values of T_e, T_{cold} and $\Delta Y/Y$

ment. Error related to different reflection coefficients in hot and cold measurement (e_{NF}) assuming perfect match at the input of the DUT ($S_{11} = 0$) can be shown as [15]:

$$e_{NF} = \frac{(\frac{T_{hot}}{T_{cold}} - 1)F(\Gamma_{sc})}{(\frac{(1-|\Gamma_{sh}|^2)}{(1-|\Gamma_{sc}|^2)}F(\Gamma_{sh}) - F(\Gamma_{sc})) + \frac{(1-|\Gamma_{sh}|^2)}{(1-|\Gamma_{sc}|^2)}(\frac{T_{hot}}{T_{cold}} - 1)} \tag{2.5}$$

where Γ_{sc} and Γ_{sh} are the noise source reflection coefficients in cold and hot states, respectively, and $F(\Gamma_{sc})$ and $F(\Gamma_{sh})$ are the noise figure of the DUT associated with these two states. Equation 2.5 suggests that the difference in reflection coefficient, even with perfect match at the input of the DUT, can create a systematic error in the noise figure measurements. To minimize this error, it is crucial that the source presents the same load both in on- and off- states.

A noise source satisfying these two main requirements, high enough ENR and constant termination, can enable the built-in self-test for noise. In addition to the design of the noise source itself there has to be circuitry designed to couple this source to the DUT without

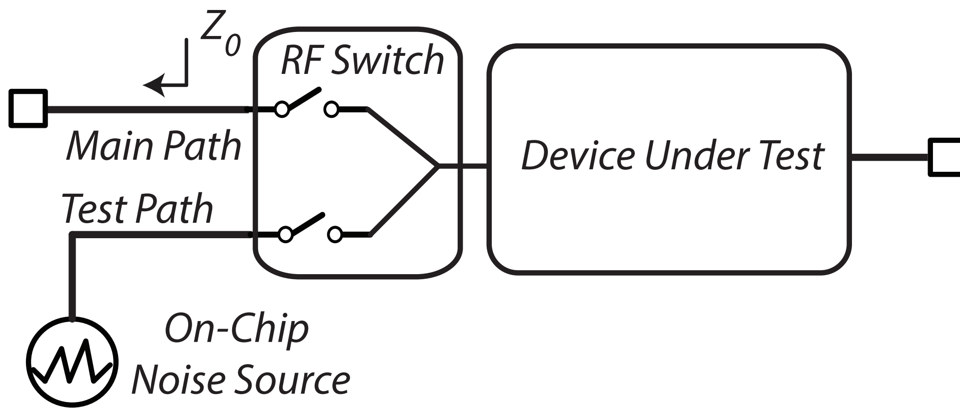


Figure 2.2. Block diagram of the on-chip noise source coupled to the DUT through a separate path as the RF input

disrupting the DUT's regular operation. The design of this coupling circuit is discussed in coming sections.

2.2 Circuit Design

The implementation of the built-in self-test system for noise, requires the integration of the noise source, an RF switch, and the DUT, as shown in Figure 2.2. Since the noise figure of a device is a function of generator impedance [29], the noise source should present the same impedance to the DUT as the main path, which in this work is assumed to be $Z_0 = 50\ \Omega$. The RF switch should have low insertion loss and high isolation. Complete characterization of the noise source requires different noise figure responses to be tested using the source. This can be achieved by the use of a reconfigurable LNA that can produce different noise figure responses.

2.2.1 Noise source design

To have a better understanding of the ENR that can be achieved by CMOS transistors, a more detailed look at the noise in CMOS is required. Understanding the contributions

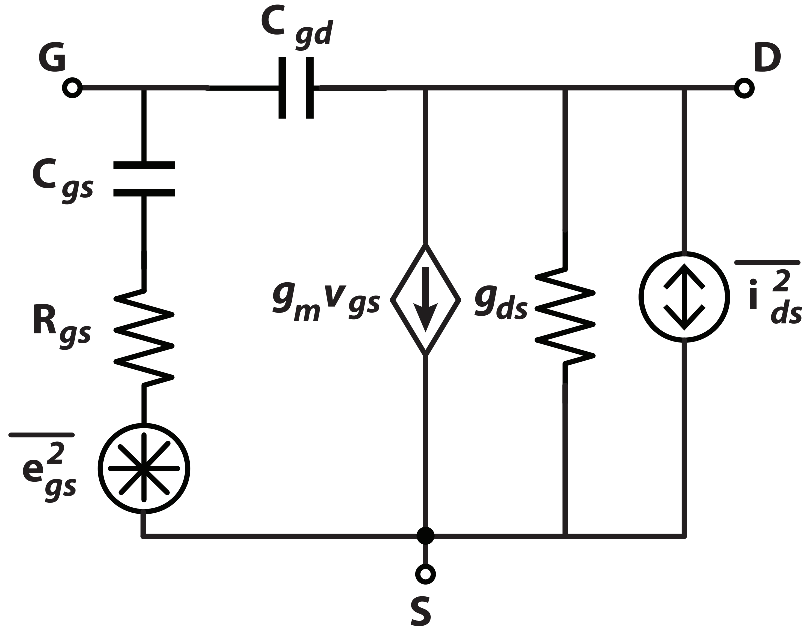


Figure 2.3. Small signal model of a FET including noise sources as presented by [30]

of different sources of noise in a CMOS device can help to improve the performance of the required noise source. This conceptual analysis can be carried out using available small signal models.

2.2.1.1 Noise in CMOS and possible noise source implementations

One of the common models used for small signal and noise characterization of field effect transistors (FETs) is the model presented by Pospieszalski in [30]. Figure 2.3 shows the small signal model of a FET device including noise parameters. Based on this model the required noise parameters of a device [31, 32], can be found with the inclusion of a voltage noise source $\overline{|e_{gs}|^2}$ in the gate and current noise source $\overline{|i_{ds}|^2}$ at the output.

The $\overline{|e_{gs}|^2}$ corresponds to the noise associated with the gate resistance at a temperature T_g (which is typically room temperature) [30], and has a spectral density of

$$\overline{|e_{gs}|^2} = 4kT_g r_{gs} \Delta f, \tag{2.6}$$

where k is the Boltzmann constant and Δf is the desired bandwidth. The current noise is associated with the excess channel noise and is associated with the small signal output conductance for the sake of modelling. The variable T_d is the equivalent noise temperature of the output impedance of a FET. T_d is usually in the order of several thousand Kelvins. The total current noise at the drain can be expressed as

$$\overline{|i_{ds}|^2} = 4kT_d g_{ds}\Delta f. \tag{2.7}$$

Knowing the parameters affecting the noise performance of a FET device can bring significant help to maximize the achievable noise from a source implemented by FET devices.

As a first design iteration, a single FET noise source was considered. Figure 2.4(a) shows the schematic diagram of the single FET noise source and Figure 2.4(b) shows the noise simulation results of the source using 32nm SOI CMOS simulation models. Results show that, the T_{hot} achieved for a 4 um device with 1 mA drain current (terminated in 50 Ω), is on the order of 500 K which is not sufficient for the desired applications.

As a second step, this noise source was simulated with higher current density through the device to study the maximum possible ENR. Figure 2.5 shows the simulation results for the output equivalent noise temperature for different DC bias points. These results show that the highest achievable noise temperature is still less than 900 K. Unfortunately,higher bias current decreases the output impedance of the source, which can load the 50 Ω termination resulting in mismatch between the on- and off- states.

Since the use of a single FET due to low output ENR and low output impedance can not satisfy the requirements for frequencies between 1 to 50 GHz, a more sophisticated design is required to achieve the desirable performance.

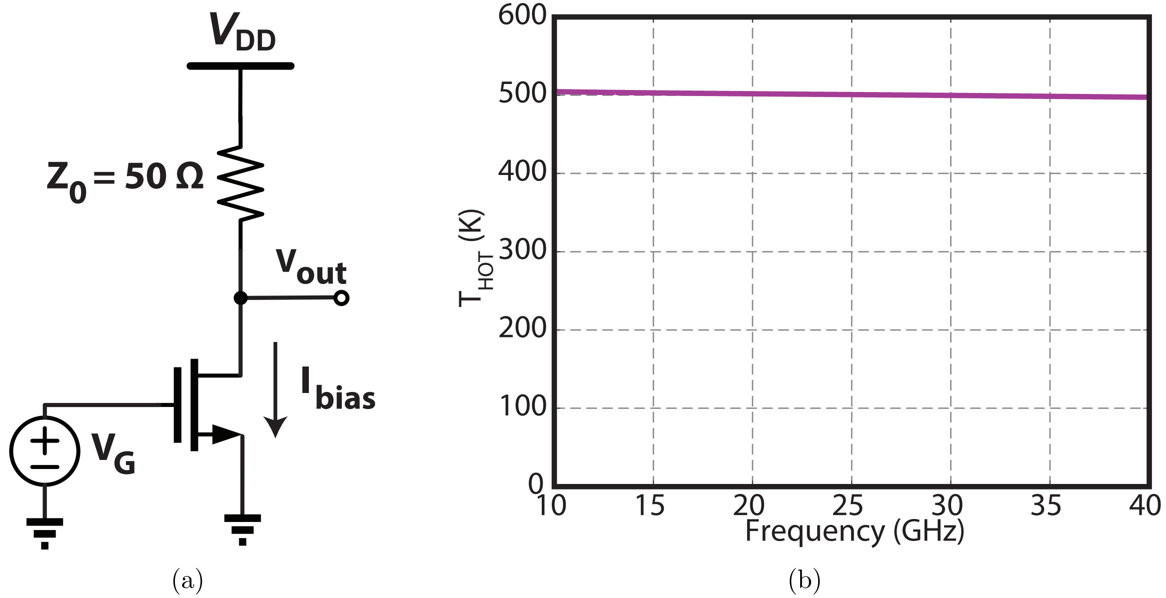


Figure 2.4. (a) Schematic diagram of the single FET noise source. (b) Simulation results of the equivalent noise temperature at the output of the single FET source for $I_{bias} = 1mA$.

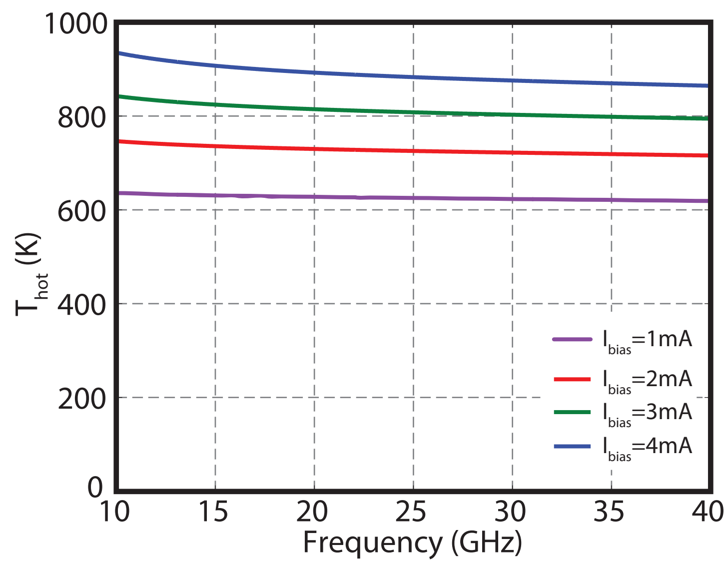


Figure 2.5. Simulation results of the equivalent output noise temperature of the single FET noise source for different I_{bias} settings, using cadence models.

(a) (b)

Figure 2.6. (a) block diagram of noise source including termination. (b) Schematic diagram of current-mode noise source.

2.2.1.2 Proposed noise source

To achieve the two main requirements of the noise source, one possible solution is to have a current-mode noise source terminated into a Z_0 load, as shown in Figure 2.6(a). Assuming high output impedance for the current mode noise source, the termination should be close to the Z_0 impedance in both cases, where the source is either on or off. Figure 2.6(b) shows one possible implementation of a current-mode noise source, where a resistor is followed by a triple cascode. A triple cascode topology was used to increase the output impedance of the circuit in order to prevent mismatch between on- and off- states. To prevent the use of a lossy switch on the noise path, the noise source is disabled by turning off all transistors. There are switches embedded into the circuit in order to prevent the break-down of the thin oxide devices used in the circuit. A programmable current-mode digital to analog converter (DAC) is used as the current reference to embed some flexibility in the biasing of the noise source.

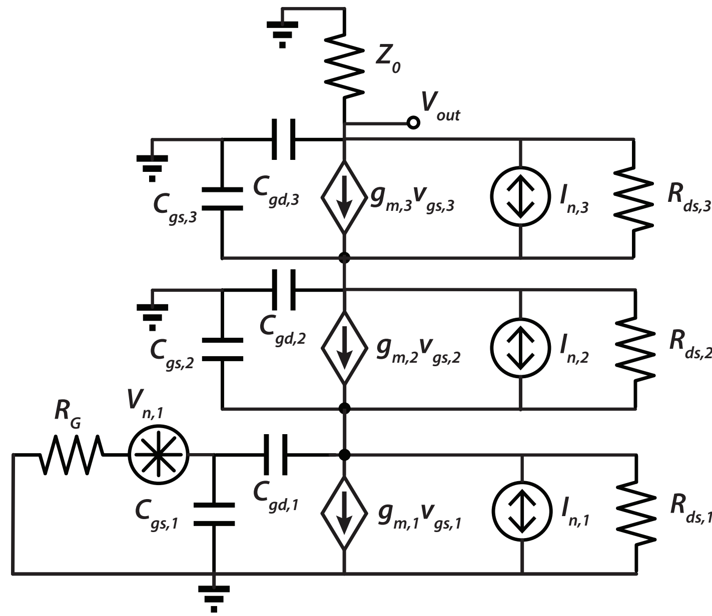


Figure 2.7. Equivalent small signal circuit model of the noise source including sources of noise (neglecting the thermal noise of the resistor r_{gs}) based on the Pospieszalski noise model [30]

Figure 2.7 shows the small-signal equivalent circuit model of the current-mode noise source. Mathematical analysis shows that at frequencies in the low tens of GHz, most of the contribution of the output ENR of the current-mode noise source is attributed to the thermal noise of the resistor R_G and the channel noise of transistor M_1. This can also be visualized by looking at the path, for each source of noise. Figure 2.8(a) shows that the current coming out of transistor M_1 has two paths through which it can flow: into the high resistance drain of M_1 or into the low resistance source of M_2. In the extreme case that r_{ds} goes to infinity the current must flow through the source of M_2. Assuming that no current flows through $C_{gs,2}$ and $C_{gd,2}$ for Kirchhoff's current law (KCL) to stand, the same current flows through transistor M_3 and then the resistive load. This means any current from transistors M_2 and M_3 will loop back through the device, as shown in Figure2.8(b). However in the real case,

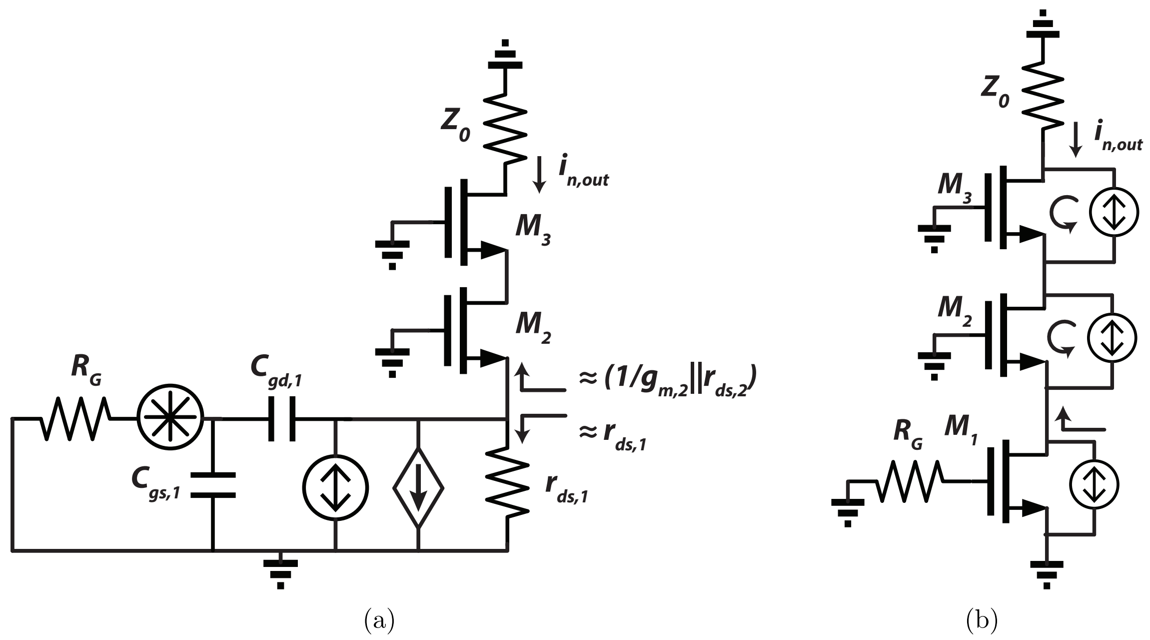


Figure 2.8. (a)Small signal model of the noise highlighting dominant sources of noise (b) Direction of the current noise for each transistor in the extreme case of $r_{ds} = \infty$

r_{ds} has a finite value that it is normally much larger than $1/g_m$. As a result, despite some effect from transistors M_2 and M_3, most of the noise contribution is from transistor M_1.

The total noise current contribution from M_1 includes the drain channel noise and the voltage noise at the gate, multiplied by $g_{m,1}$. The voltage noise at the gate of M_1 includes the voltage noise associated with the gate to source resistance as defined in (2.6), however this is insignificant compared to the thermal noise of R_G and hence is neglected. In addition, noise sources associated with r_{gs} of transistors M_2 and M_3 will have very small effect on the total ENR and therefore are not considered in this model.

Only assuming the contribution of thermal noise of R_G and channel noise of M_1, the output excess noise temperature can be approximated as

$$T_{ENR} \equiv T_{hot} - T_{COLD} \approx T_d g_{ds,1} Z_0 + \frac{T_a Z_0 R_G g_{m,1}^2}{1 + \omega^2 C_{IN,1}^2 R_G^2}, \tag{2.8}$$

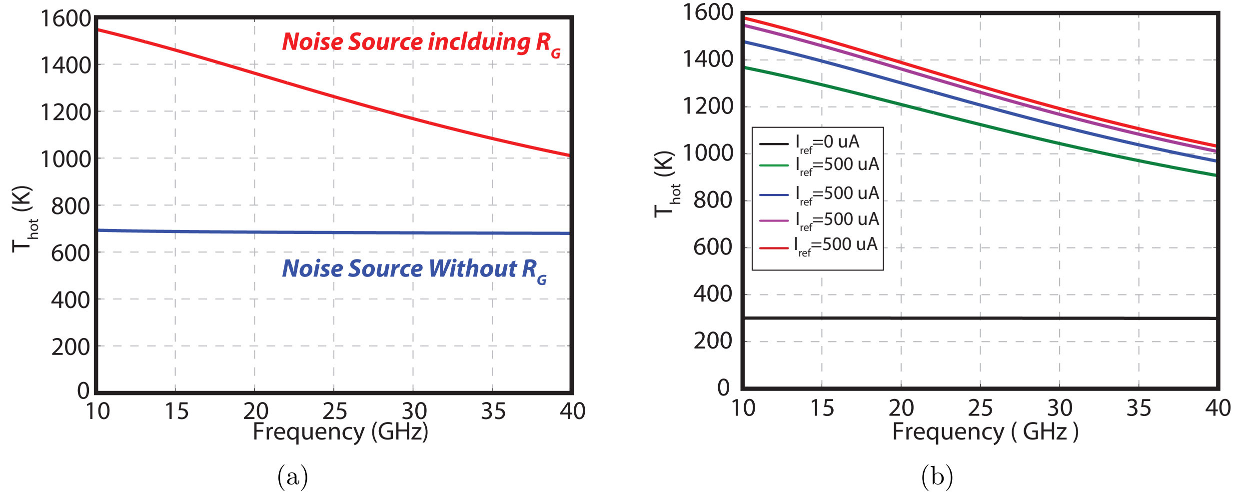


Figure 2.9. (a) Comparison between noise source performance with and without R_G . Red line showing the T_{hot} of the source with R_G and blue line the source without R_G (b)Simulation results of the proposed noise source including the Z_0 termination for different DC biases and off state.

where $C_{IN,1}$ is the total capacitance at the gate of M_1. Despite impacting the frequency response of the excess noise source, the introduction of R_G increases T_{hot} by a factor of two at frequencies between 10 to 40 GHz (See Figure 2.9(a)). Figure 2.9(b) shows the simulation results of the noise source at four different DC biases as well as the off-state. The noise of the 50 Ω termination is included. Simulation results show that the proposed noise source can achieve excess noise temperatures higher than 1000 K through the band of interest, which meets the requirement for sensing noise at mm-wave frequencies.

Since the creation of additional capacitance can cause significant roll-off on the output ENR, the layout implementation of the noise source requires careful consideration of parasitic loads at the gate of M_1. Considering these critical points, the layout of the noise source was completed in IBM 32nm SOI CMOS technology using Cadence software. The result is shown in Figure 2.10.

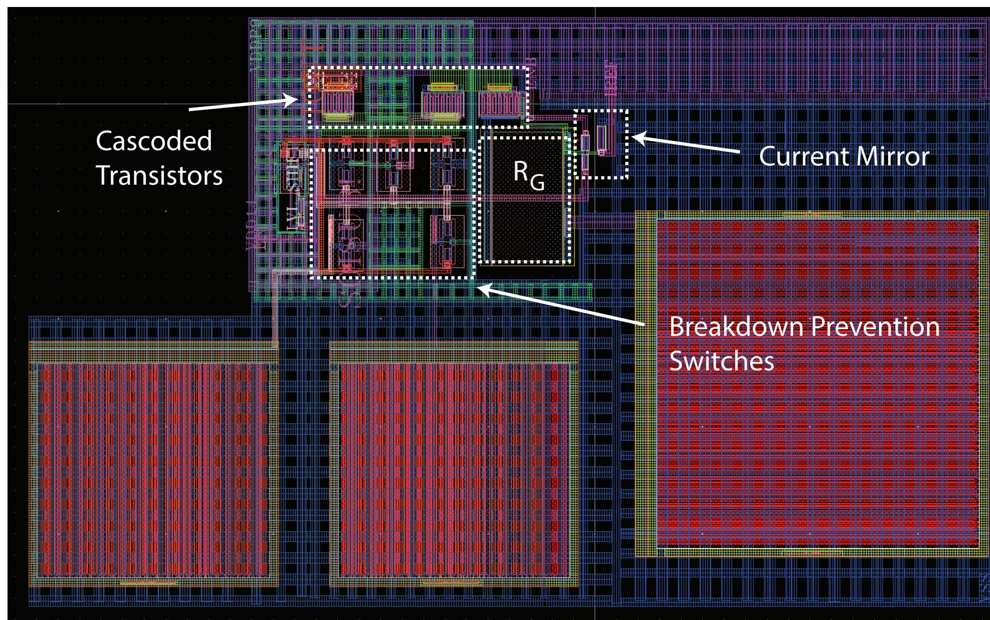


Figure 2.10. Layout implementation of the noise source in IBM 32nm SOI CMOS technology.

2.2.2 RF Switch

The integration of the noise source with the DUT on-chip, as shown in Figure 2.2, requires a switch which can select between either the main path or the test path. A simple way for implementing such a switch is the use of pass gates. However to reduce the loss of such circuits, larger devices are preferred. However, this would decrease the isolation between the two paths, which is not desirable. As a result, a more sophisticated approach was required, to increase the isolation and at the same time reduce the load on the main path.

To achieve the required isolation, a cascode transconductance amplifier that combines the two paths in current-mode was used. The schematic diagram of the G_m block is shown in Figure 2.11. The RF switch was built into the first stage of the LNA. Input devices were sized to achieve an optimal noise match (Γ_{opt}). The desired device sizes were found to be 100um (100 $\times$ 1um fingers). The use of these large devices resulted into isolations of approximately

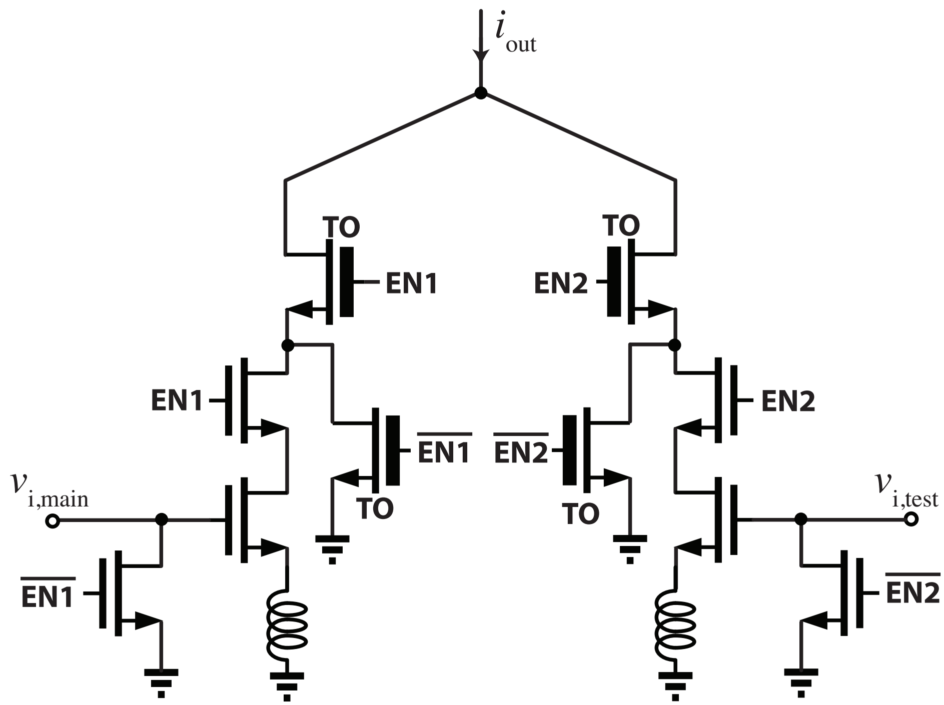


Figure 2.11. Circuit schematic diagram of the RF switch.

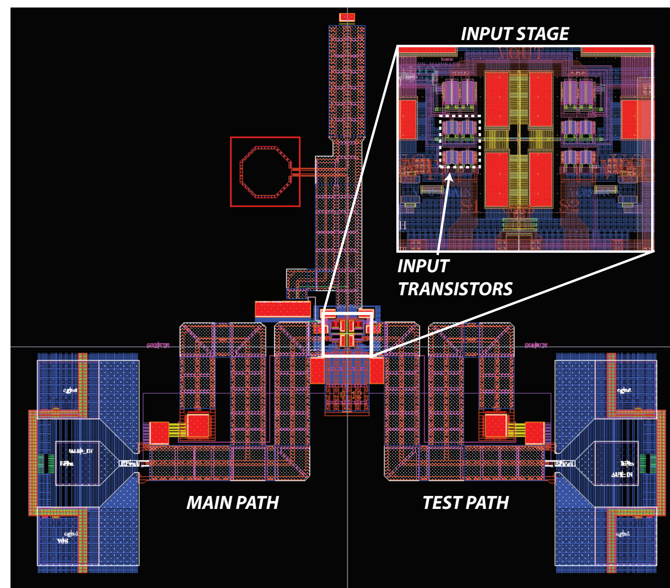


Figure 2.12. Layout implementation of the RF switch, highlighting the test path, main path and input transistors

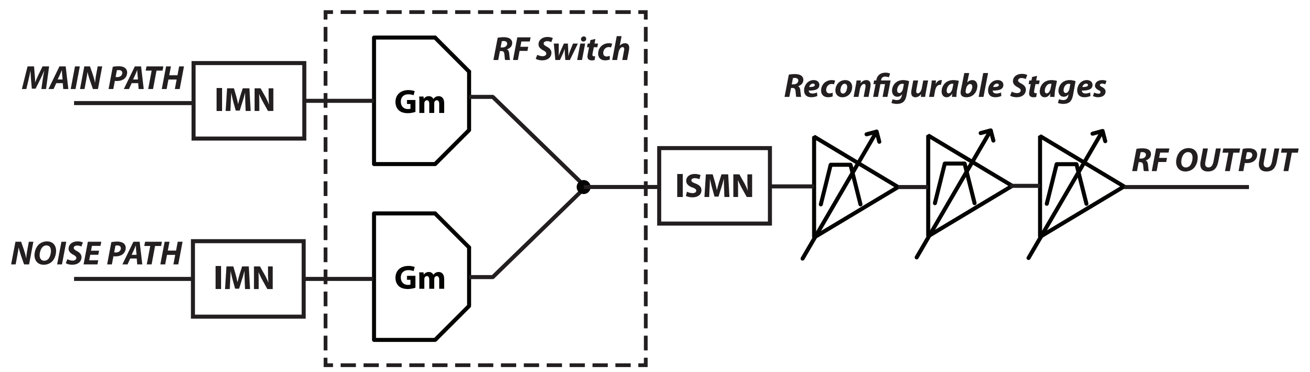


Figure 2.13. Block diagram of the reconfigurable LNA used as the device under test.

40 dB. In addition, having large devices for both paths (the main path and the test path) reduces the possible mismatch between the two paths due to process variations. To prevent breakdown of thin oxide devices, thick oxide devices (marked as TO in Figure 2.11) were used as the switching transistors. Degeneration inductors were employed in the input matching network to provide power match at the input of the LNA.

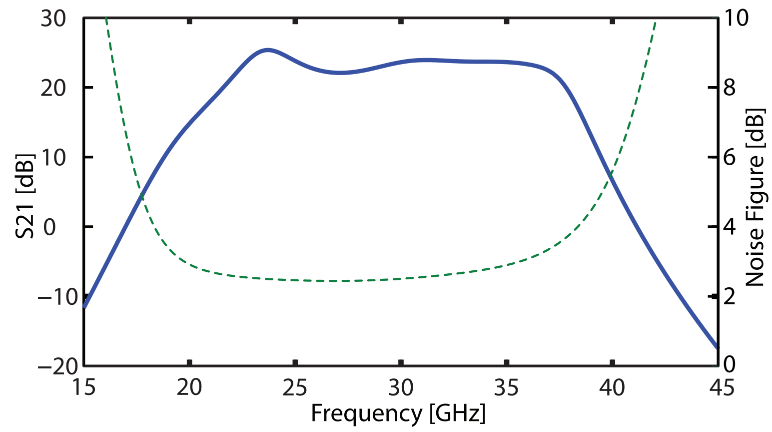
2.2.3 Device Under Test

A complete characterization of the noise source requires a way to test its performance under different scenarios. To have the ability to verify the validity of the proposed technique, a highly reconfigurable low noise amplifier (LNA)—designed by Radio Frequency Nanoelectronics Group at University of Massachusetts Amherst— was used as the DUT. The use of a reconfigurable LNA provided the opportunity to evaluate the accuracy of the proposed noise measurement technique for different noise figure values.

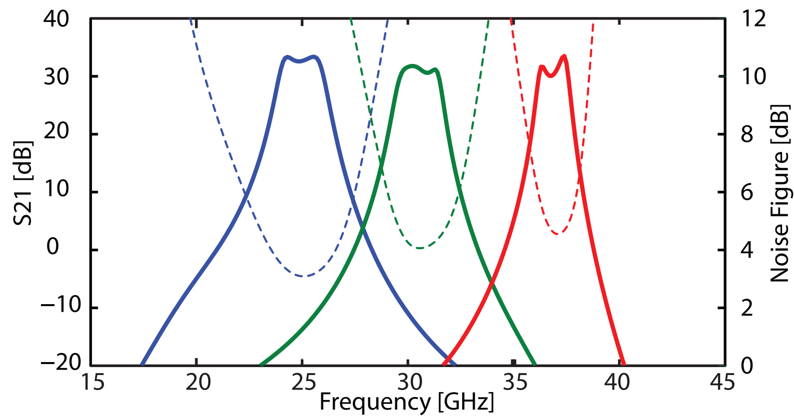
The reconfigurable LNA consists of four different stages as shown in Figure 2.13, including the RF switch presented in the previous section along with three fully reconfigurable stages. The reconfigurable stages provide great control over the frequency and noise response of the LNA. Different tuning elements in addition to tunable bias sources bring programmability to these stages.

Each of the three programmable stages in the LNA are bandpass second-order systems with two complex conjugate poles employed to create a filter response. By programming the location, the quality factor, and the magnitude of each of these three poles, variety of different responses can be achieved. Figures 2.14(a) and 2.14(b) show simulation results for the noise performance and S-parameters of the LNA for different tuning states. Figure 2.14(a) shows an example of a broadband response for which the poles associated with each stage are separated to produce a wide response. Figure 2.14(b) shows narrow responses where the pole locations of different stages are put together to create responses with a high quality factor.

These results show that with the use of different noise profiles of the LNA the accuracy of the proposed technique can be verified for different values of T_e. While the same exact response from simulation may not be achieved after fabrication of the chip, due to the large variations in device parameters , the ability to produce different noise profiles should be enough to prove the conceptual functionality of the proposed built-in self-test technique.



(a)



(b)

Figure 2.14. (a) An example of a wide band response achieving less than 4 dB noise figure. (b) Examples of different narrow band tuning responses achievable with different states. Dotted lines showing noise figure and solid lines showing S_{21} responses. Figure provided by J.C.Bardin.

CHAPTER 3

MEASUREMENT PROCEDURE AND RESULTS

This chapter discusses the detailed procedure for noise measurements using the proposed noise source. In addition, measurement results for all of the different steps are presented and discussed. It is shown how the calibration of T_{hot} using only one IC can be transformed to noise measurements of other ICs. This chapter also includes the discussion on the error calculation of noise measurements taken by the proposed technique.

To find T_e, using $T_e = (T_{hot} - YT_{cold})/(Y - 1)$, knowledge of T_{hot} is required. The extraction of T_{hot} was only performed for one IC, with the hypothesis that, despite the large variation in device parameters, due to fundamental nature of noise, the ENR of the noise source should be repeatable between different integrated circuits. To test this hypothesis the extracted T_{hot} value of one IC is used for calculations of T_e for other ICs. These results were compared to reference measurements taken with a network analyzer. Twenty different programming states of the reconfigurable LNA were developed, to evaluate the performance of the noise source. A detailed explanation of the measurement procedure along with post processing is presented in the next section. Results, obtained for these measurement steps, are presented and discussed in Section 3.2.

3.1 Measurements and Post Processing Steps

To systematically obtain the results required, a step by step measurement and processing procedure was developed. These steps were as follows:

Step 1- Scattering parameters and noise figure values were measured using a network analyzer.

Step 2- The output power of the DUT for cold (P_{cold}) and hot (P_{hot}) states were acquired by a spectrum analyzer. The Y-factor was calculated by dividing P_{hot} by P_{cold} for each measurement set.

Step 3- Using the noise figure and Y-factor values from steps 1 and 2, T_{hot} was extracted as a function of frequency for one IC.

Step 4- Using the extracted T_{hot} and Y-factor measurement results, the noise figure values of other ICs were calculated. These results were compared to the reference measurements taken with the network analyzer.

3.1.1 Reference Measurements

Reference measurements, taken with the commercial equipment, are used as a baseline to which the in-situ noise measurements will be compared. Reference data for scattering parameters and noise figure values of the LNA were acquired using an Agilent N5247A-029 vector network analyzer (VNA). The VNA is capable of performing accurate noise measurements up to 50 GHz. Wafer probing was used to perform RF measurements, as shown in Figure 3.1. A multi-step noise calibration procedure of the VNA was required, prior to taking reference measurements.

The VNA uses the cold source method for noise figure measurements. The use of this method, requires the knowledge of the DUT's available gain and the gain bandwidth product of the noise receiver system. The gain of the DUT is found using the scattering parameters collected by the VNA. An external noise source is used for calibration of the noise receiver prior to start of each measurement. In addition, to ensure a 50 Ω system and to account for losses in cables, connectors, and probes, an on wafer calibration is required. For higher precision in noise measurements a vector noise calibration was used, which employs an internal

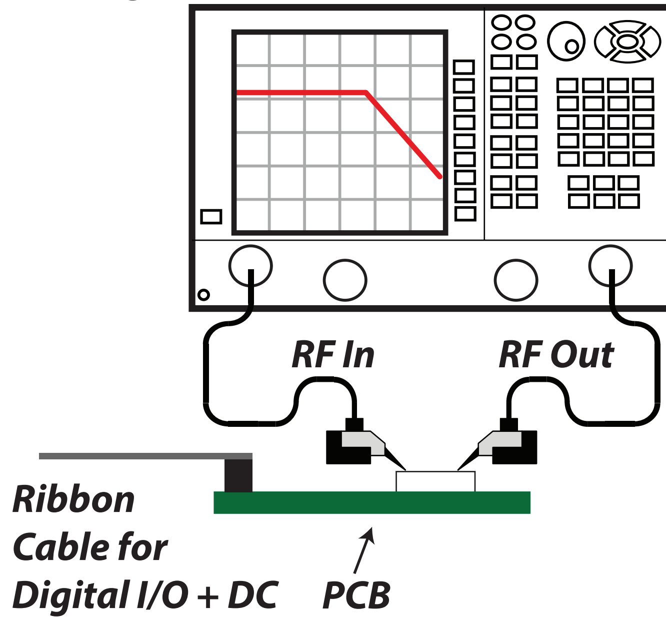


Figure 3.1. VNA measurement set up

impedance tuner to find an estimate of the noise parameters. A more detailed explanation of the VNA noise calibration is presented in Appendix A.

3.1.2 Y-factor measurements

The Y-factor calculation requires hot and cold measurements of each integrated circuit, across all different states, using the internal noise source. For these measurements only the output of the DUT was wafer probed since the input was connected to the noise source through the test path. The schematic diagram of the measurement setup for Y-factor measurements is shown in Figure 3.2. The output power was measured using an Agilent N9030A signal analyzer. A ribbon cable was used to bring the required DC and digital signals to the chip. To calibrate the measured power, a baseline measurement was taken while the IC was powered off. The baseline measurement provides the noise floor of the receiver system.

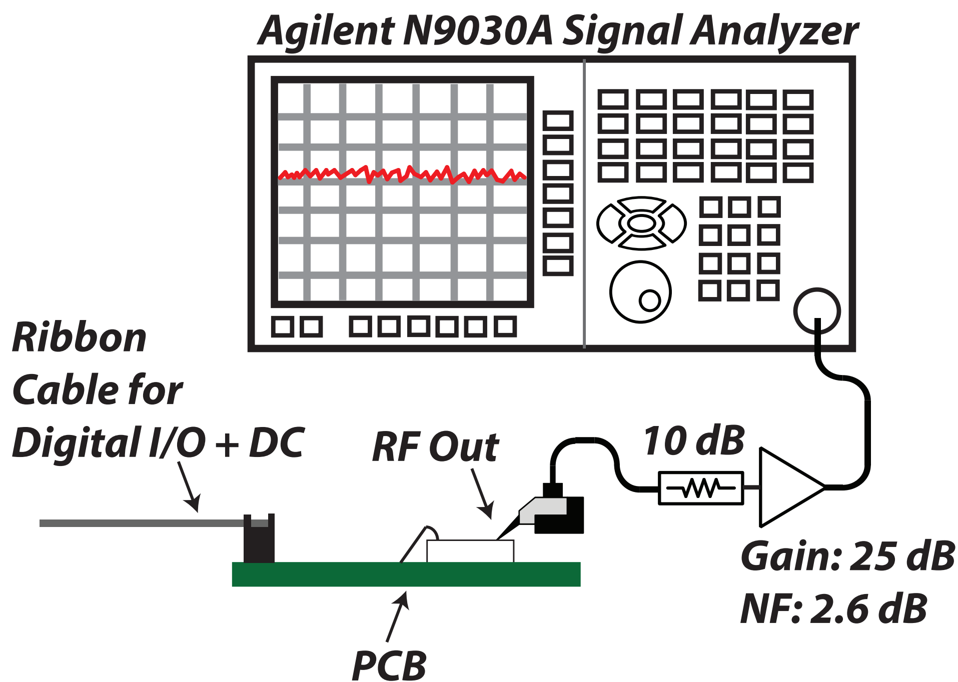


Figure 3.2. An attenuator was employed in order to set a measurement system noise figure of approximately 13 dB, which is consistent with what might be readily achieved in an integrated system.

The dynamic range, for which Y-factor values are measurable, is related to the noise floor of the receiver system. Since the final goal is to use this method for a complete built-in self-test for noise, the receiver system used for evaluation of this method should be achievable on-chip. To emulate what might be achieved on-chip, a 10 dB attenuator followed by an LNA with a 2.5 dB noise figure was connected between the output and the spectrum anlayzer. The use of the attenuator and the external LNA results in a receiver system with a noise figure value of 13 dB.

3.1.3 Calibration of T_{hot}

Conversion from Y-factor to T_e, and consequently noise figure, requires knowledge of T_{hot}. Models provided for emerging processes, such as CMOS, are geared toward digital

applications and thus the RF models are incomplete. This is especially true of noise models, which tend to be extremely optimistic. As a results of this inaccuracy, T_{hot} could not be extracted from simulation and had to be extracted from measurement results.

Using the Y-factor and noise figure measurements, T_{hot} can be found as a function of frequency using,

$$T_{hot} = (Y - 1)T_e + YT_{cold}, \tag{3.1}$$

where Y is found from the spectrum analyzer measurement results and T_e is the noise temperature of the DUT measured by the network anlyzer. This calibration procedure was only performed for one state of a single IC and the results were applied to subsequent integrated circuits.

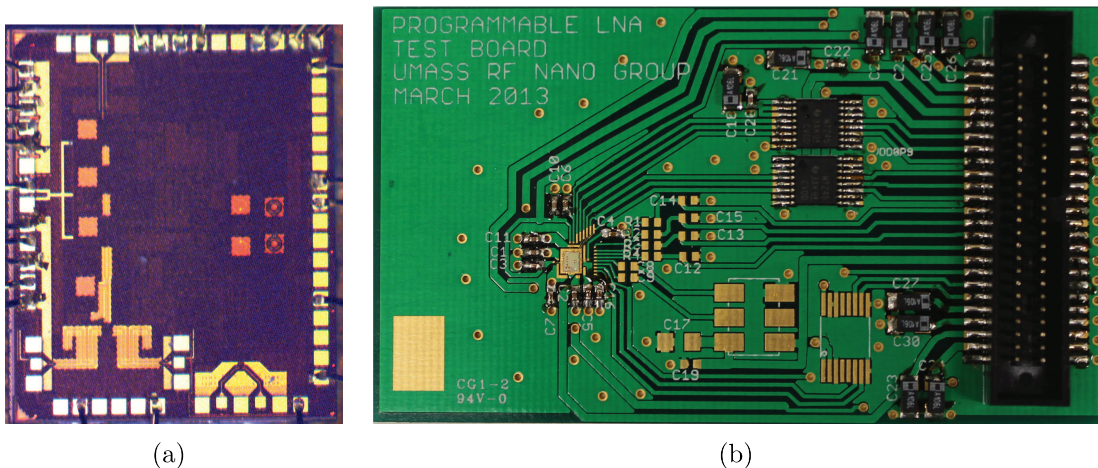
To prevent the noise in the extraction of T_{hot} from propagating to subsequent noise figure measurements, a model based on the analytical solution for the ENR of the noise source (see Equation 2.8) was fitted to the extracted T_{hot}. Using Equations 2.8 and 3.1 it can be found that

$$\overbrace{T_e\,(Y-1) + YT_c}^{\text{Measured } T_h} = \overbrace{\frac{a+bx}{1+cx}}^{T_h \text{ Model}}, \tag{3.2}$$

where $x = \omega^2$, $a = T_c + T_d g_{ds,1} Z_0 + T_a R_G Z_0 g_{m1}^2$, $b = C_{IN,1}^2 R_G^2\,(T_c + T_d g_{ds,1} Z_0)$, and $c = C_{IN,1}^2 R_G^2$. $C_{IN,1}$ is the total capacitance a the gate of the transistor M_1 in Figure 2.7. Using these steps, all required data were collected and then processed to evaluate the performance of the proposed technique. Measurement results for these steps are presented in the next section.

3.2 Results

The circuit was fabricated in IBM 32 nm SOI CMOS technology. A die photo of the chip is shown in Figure 3.3(a). The chip dimensions are 2mm $\times$ 1.6mm. The circuits reported in this work occupy 2$\times$1 mm^2 and the remaining area is used to implement a receiving system



(a) (b)

Figure 3.3. (a) The fabricated chip die photo. The dimensions of the chip are 2mm × 1.6 mm. (b) Photograph of the PCB board with the die attached.

that is beyond the scope of this thesis. The total area occupied by the LNA is approximately 1mm × 2mm, while the noise source occupies 0.1mm ×0.4mm. As shown in Figure 3.3(b) a chip-on-board approach was used for testing of all ICs. DC and digital I/Os were wire-bonded to the printed circuit board (PCB). Additional bypass capacitors were populated on the PCB to reduce the noise on DC supply lines. Digital level shifter ICs were also used on the board to present clean digital signals to the chip. A twisted-pair ribbon cable was used to reduce spikes on signals and prevent pickup on the lines.

A MATLAB controlled data acquisition box was used to generate and send the required digital signals to the chip. There were three different DC voltage sources and one reference DC current source, required for the biasing of the chip. A probe station along with single ended probes were used for RF measurements. Figure 3.4 shows a photograph of the measurement setup during the reference measurements. To reduce the measurement time for each integrated circuit, a MATLAB function was used to automate the sweep through all LNA states and record the data for both VNA and spectrum analyzer measurements.

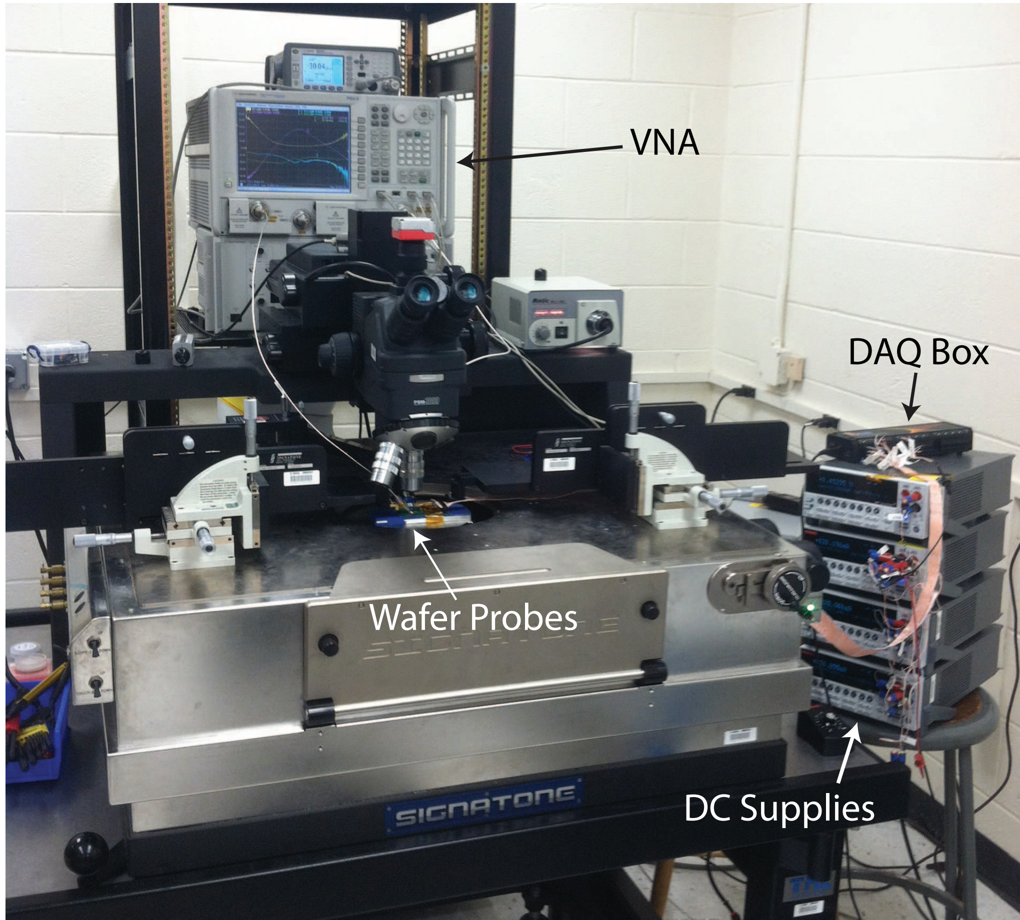


Figure 3.4. Photograph of the measurement setup including DC sources, data acquisition box , wafer probes and VNA.

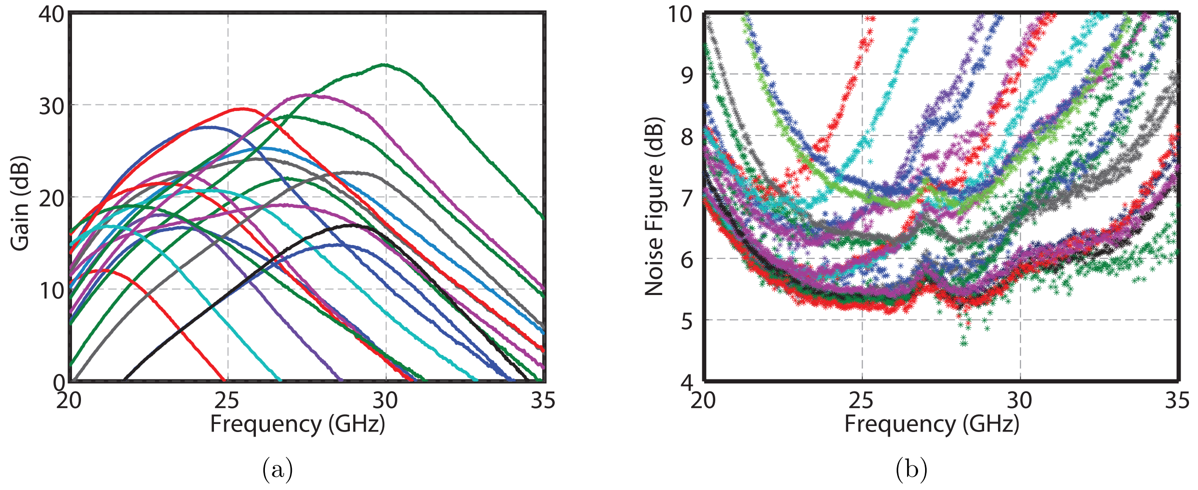


Figure 3.5. (a) Measurement results of the gain for all different states of the LNA for one chip. (b) Noise figure measurement results of all different states for one chip.

3.2.1 Reconfigurable LNA Measurements

Twenty different states of the LNA with unique responses were developed to evaluate the performance of the in-situ noise source. Figures 3.5(a) and 3.5(b) show S_{21} and noise figure measurements of all twenty different states for one IC. Figure 3.5(a) shows that the these states cover a wide range of gain values from 10 to 30 dB for the bandwidth of 20-35 GHz. This shows the versatility of the reconfigurable LNA used as the DUT for in-situ noise measurements. Figure 3.5(b) shows that these different states can collectively cover noise figure values from 5 to 10 dB. In addition, the precision of the on-chip noise source can be examined for different noise figure values throughout the whole bandwidth (20-35 GHz).

Different states of the LNA can produce relatively similar noise figure responses. The total noise of the LNA is the cascaded noise of its four different stages. The total noise factor of the LNA as a function of noise factor and gain of each stage can be found as [33],

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} \tag{3.3}$$

where F_1, F_2, F_3 and F_4 are the noise factors of first, second, third and fourth stages respectively and G_1, G_2 and G_3 are the gains of the first, second and thirds stages. Equation 3.3 suggests that for two identical gain responses, the noise figure response can be different. This is why some states in Figure 3.5, have relatively different noise figure responses despite having similar gain profiles.

High variation in device parameters after fabrication, deviates the LNA response from simulation results. As a result, to achieve matching simulation and measurement results, the LNA states had to be tweaked. The discrepancy between simulation and measurement results illustrates the importance of built-in self-test techniques for these technologies.

Forward transmission coefficient (S_{21}) and noise figure values were measured for each state of all integrated circuits. S_{21} responses of all ICs are plotted together for five sample states in Figure 3.6, to highlight the variation in responses for the same state of different ICs. As an example, measurements of state 1 in Figure 3.6(a) show that peak gain values for different ICs vary from 15 to 18 dB, despite having exact same programming state. Figure 3.6 shows that the frequency profile of the S_{21} is also changing. This deviation in gain responses from die to die is a result of the high process variation in emerging technologies such as 32nm CMOS, which changes both DC and AC characteristics of integrated circuits implemented in these technologies.

Figure 3.7 shows noise figure measurement results of five sample states. Measurement results presented in Figure 3.7 show that there is a significant difference between the noise figure responses of different ICs, despite having the same programming states. This discrepancy is another illustration of large variation in post fabricated ICs for these technologies. These measurement results are used as the reference data for calculation of the error in noise measurements and for calibration of T_{hot}.

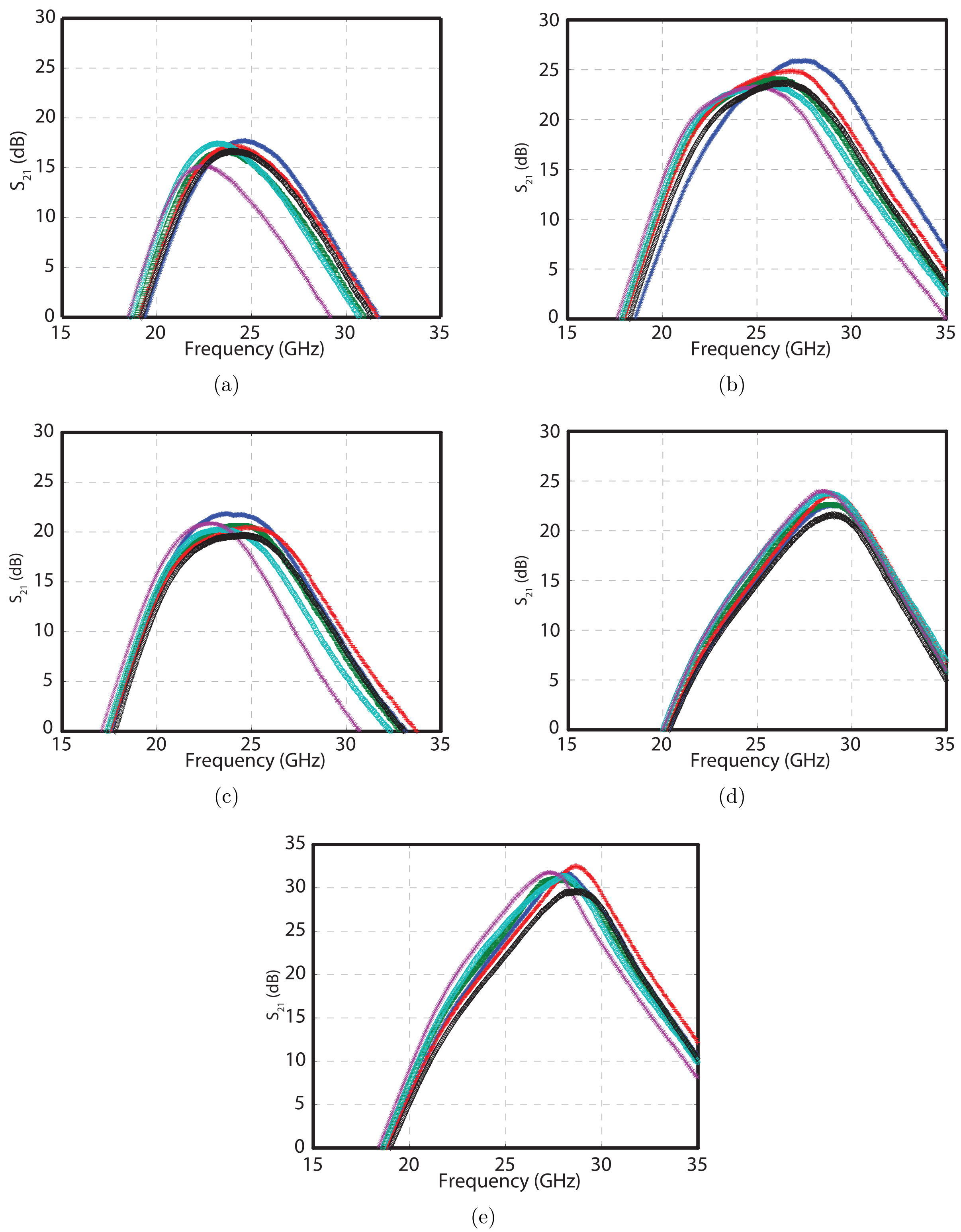


Figure 3.6. S_{21} Measurement results of the six ICs for five sample states. (a) state 1, (b) state 7, (c) state 11, (d) state 14 (e) state 19

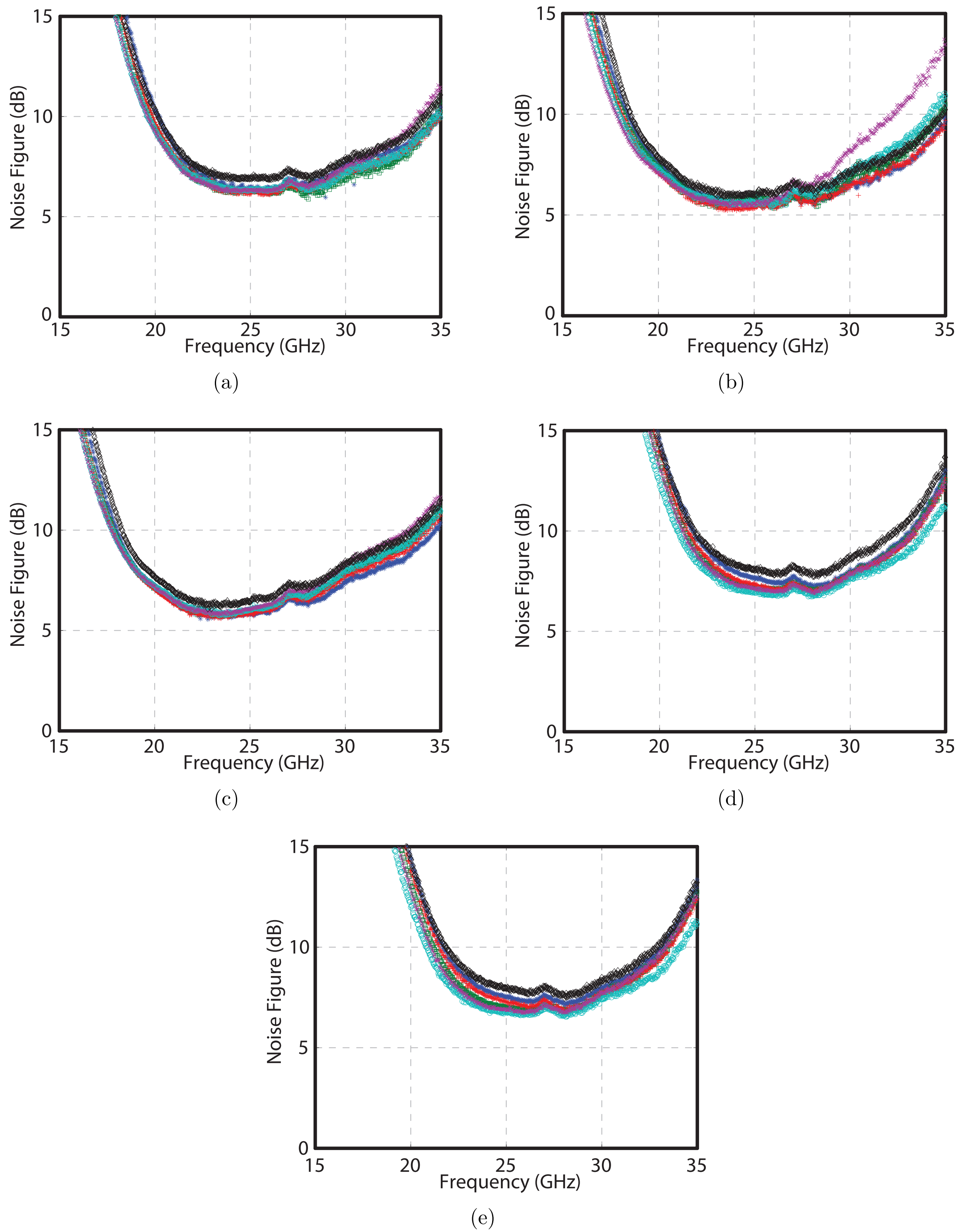


Figure 3.7. NF Measurement results of the six ICs for five different states. (a) state 2, (b) state 8, (c) state 12, (d) state 15 (e) state 20

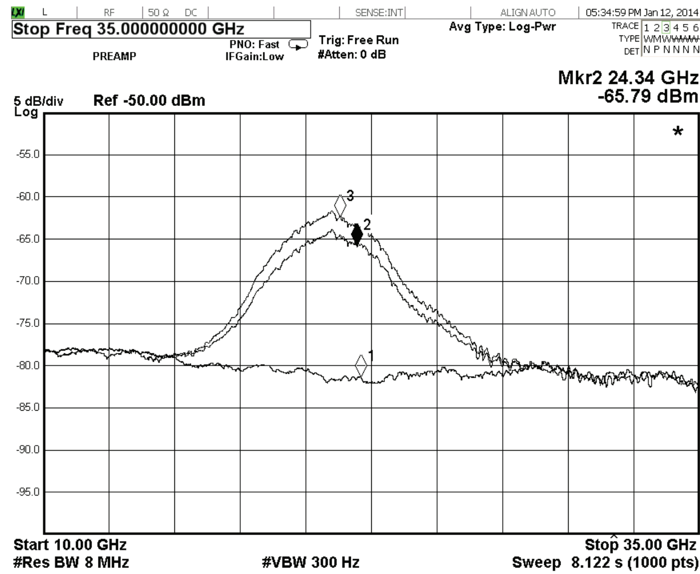


Figure 3.8. Typical Y-Factor measurement. Data marker #1 is on the baseline trace (CMOS IC powered down), whereas markers #2 and #3 identify the output for the cold and hot noise source states, respectively. The x- and y-scales are 2.5GHz/div and 5 dB/div, respectively.

3.2.2 Noise Measurements Using On-Chip Noise Source

The calculation of noise figure values for each device using the on-chip noise source, requires two measurements of power (finding Y-factor) and the extraction of T_{hot}. The Y-factor measurements were taken for all twenty different states of the LNA for each chip. In Figure 3.8, a typical hot/cold measurement, along with the baseline measurement are shown. To reduce the effect of the receiver noise, the baseline measurement results were subtracted from each hot and cold power measurement.

For measurements with spectrum analyzers there are two important settings that need to be configured: the video bandwidth (VBW) and resolution bandwidth (RBW). The video bandwidth corresponds to the signal bandwidth after the detector and sets the minimum discrimination between two power levels [34]. Lower VBW reduces the trace noise [34]. The resolution bandwidth is the bandwidth of the RF signal before the detector and sets the

minimum spacing between two recognizable tones [34]. Decreasing the RBW would decrease the noise floor of the spectrum analyzer.

For the purpose of Y-factor measurements, the desired signal is noise, thus the RBW should be set to the highest value possible to integrate more noise power. Integration of more noise power increases the signal levels resulting in better Y-factor measurements. The VBW should remain as low as possible to decrease the fluctuations on the signal. Decreasing the VBW would increase the sweep time and in order to prevent long lasting measurements, it is set to 300 Hz. The RBW is set to 8 MHz which is maximum for the analyzer used in this work. These settings result into each sweep to take less than 9 seconds for 1000 points. This time could be improved if the receiver system was to be implemented on-chip. In general the error in noise temperature measurements is a function of RBW and VBW, which can be found as,

$$\frac{\Delta T}{T} \propto \frac{1}{\sqrt{B \times \tau}} \tag{3.4}$$

where B is the RBW and τ is the integration time and is equal to 1/VBW. If the spectrum analyzer was to be implemented on-chip the RBW (IF bandwidth) could be increased. Increasing the IF bandwidth means that for the same precision in noise temperature measurements the integration time could be decreased resulting into faster measurements. Having an IF bandwidth around 100 MHz, could reduce the measurement time of each point down to less than 1ms.

3.2.2.1 T_{hot} Extraction

T_{hot} can be extracted for any LNA state of each integrated circuit using Equation 3.1, along with the Y-factor and T_e from VNA measurements. However, as was mentioned previously, the ENR of the noise source can be repeatable enough, such that the extraction of T_{hot} for one IC can be applied to subsequent samples. Nevertheless, the comparison of the extracted T_{hot} for different states for the same IC, as well as the same state for different ICs,

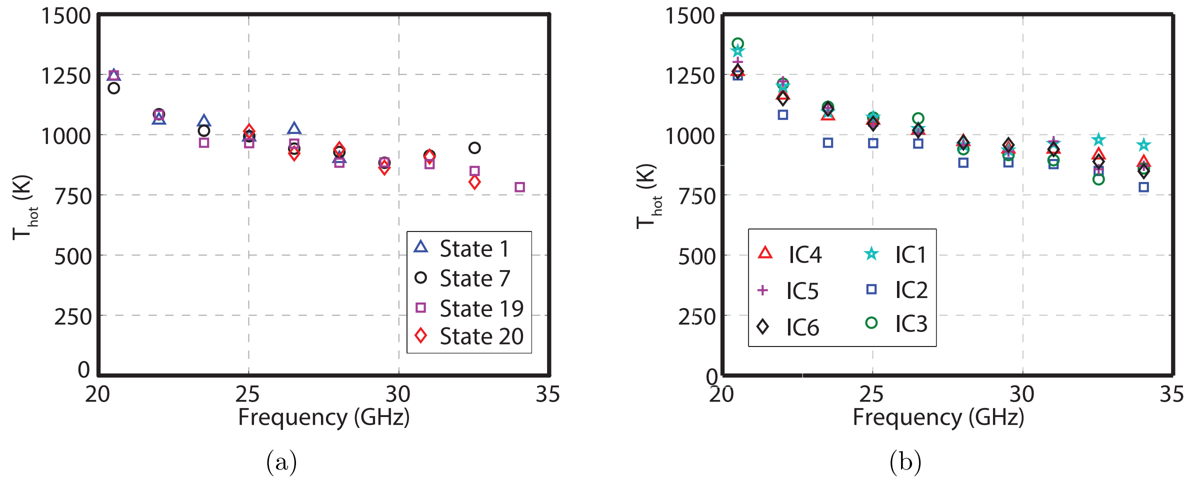


Figure 3.9. Extraction of T_{hot} for (a) different states of the same IC, and (b) different ICs for same state.

can be used to test this hypothesis. Figure 3.9(a) shows the comparison of T_{hot} extracted for four different states of IC2. Figure 3.9(b) shows the extracted T_{hot} for all ICs for state 19.

One important point is that the extraction procedure is only valid for points that are within the dynamic range of the Y-factor measurement setup. This means that the total noise power at the output of the DUT should be higher than the noise floor of the receiver system (about 13 dB). As a result, for each point to be taken within the dynamic range, the sum of the noise figure plus gain should be greater than 15 dB ($NF+Gain \geq 15dB$). Figure 3.9(b) shows only points that are within the dynamic range of the measurement, which is why there are different numbers of points for different states. To have a larger dynamic range, state 19 was chosen for comparison of different ICs. The extracted ENRs of the noise sources on different ICs are within 100 K of each other. This consistency in T_{hot} supports the aforementioned hypothesis and enables the use of only a single chip as a calibration set for measurements of other chips.

The frequency dependent T_{hot} was extracted for one state of IC1 and then used for noise measurements of subsequent samples. Using Equation 3.2, a model was fitted to T_{hot} which

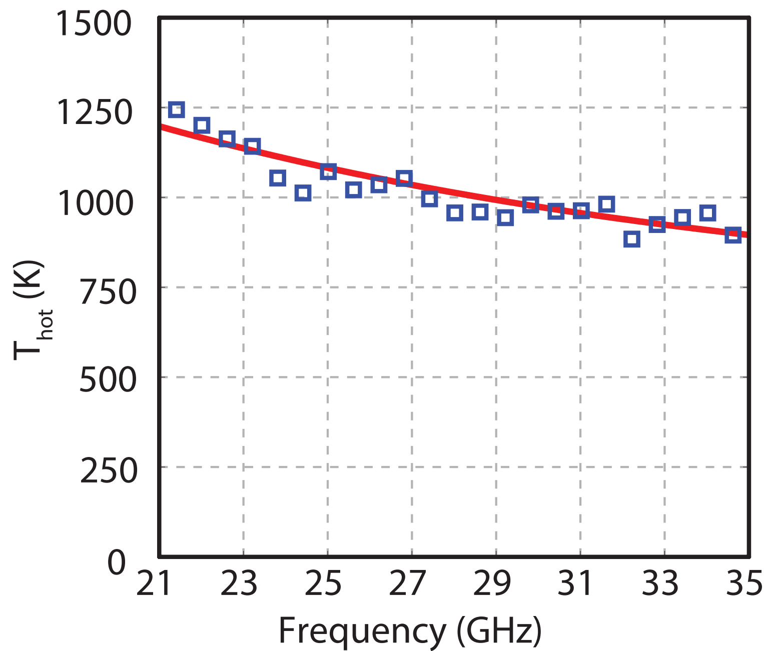


Figure 3.10. Measured (symbols) and modeled (line) T_{hot} of the noise source.

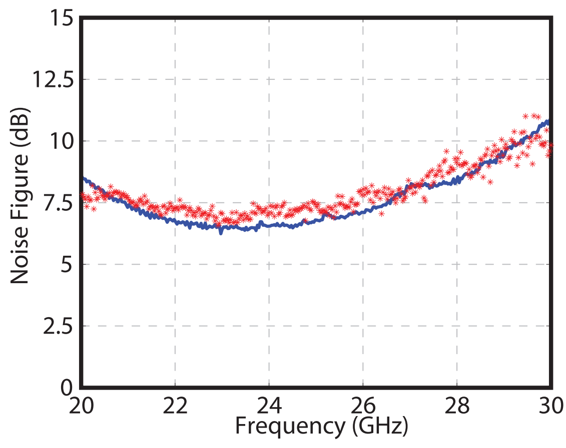
is shown in Figure 3.10. For model verification, using the simulated $g_{ds,1} = 2.5mS$ and calculated fitting parameters, $T_d \approx c/bZ_0 g_{ds,1}$ was found to be approximately 2000K. This compares very well to the value of 2400 K that has been recently reported in [35] for a device in this technology with the same current density.

3.2.2.2 Noise Figure Measurements Using On-chip Noise Source

Having the Y-factor measurement results and knowledge of T_{hot}, T_e can be calculated using Equation 1.4. This was done for all states for IC2 through IC6 and data sets were collected to be compared with the reference data from network analyzer measurements. To show the comparison between the reference data and data measured using the Y-factor method, five example plots are shown in Figure 3.11. A more complete set of comparison plots are presented in Appendix B. As discussed in previous section, for a measurement point to be within the dynamic range, noise figure plus gain should be greater than 15 dB.

Data presented in Figure 3.11 are only for points that meet this criteria and this is why the frequency span and number of points vary for different states.

The comparison between reference measurements taken by the vector network analyzer and the measurements taken by the proposed technique shows less than 1 dB difference in most points. Similarities in frequency response and closeness of the measured noise figure values prove the ability for in-situ noise characterization of mm-wave integrated circuits using the proposed noise source. Small errors in noise figure measurements of different ICs (ICs 2 to 6), while another IC (IC1) was used for calibration of T_{hot}, confirms the aforementioned hypothesis of repeatable ENR of the noise source. This enables the use of the -on-chip noise source with only requiring the calibration of one integrated circuit.



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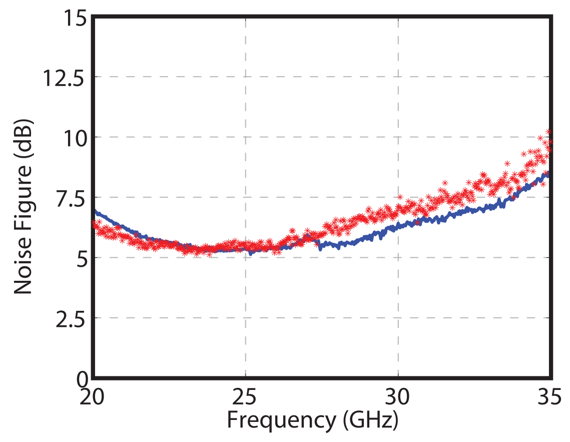

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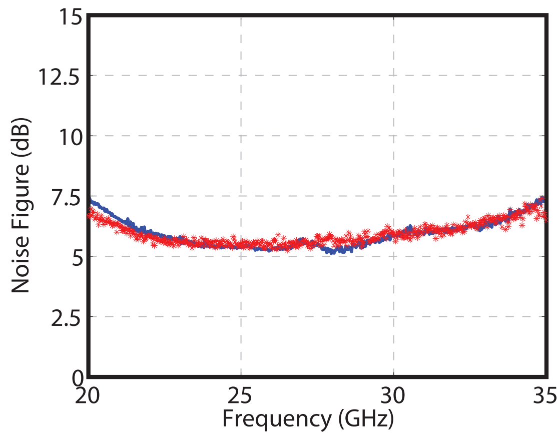

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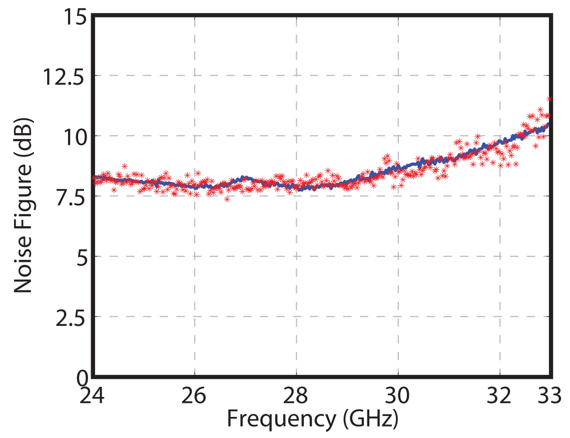

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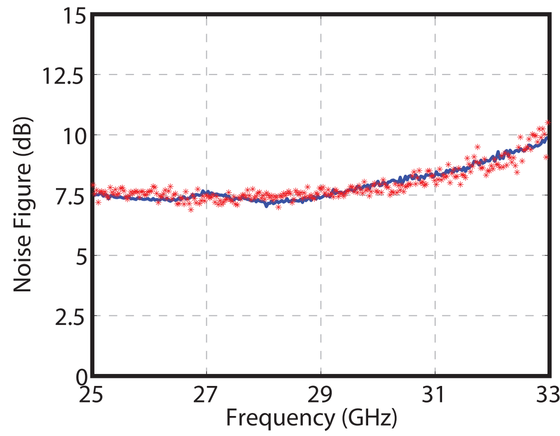


(e)

Figure 3.11. Example plots comparing the reference NF measurements with Y-factor measurements for (a) IC2 in state 1, (b) IC3 in state 2, (c) IC4 in state 3, (e) IC5 in state 5,(d) IC6 in state 4

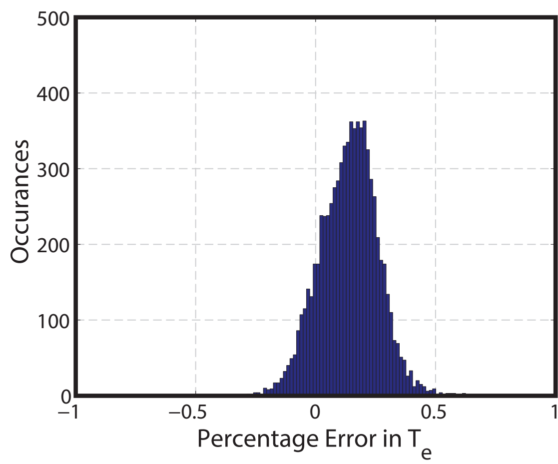
Table 3.1. Noise temperature percentage error statistics for all measured states such that Gain + NF > 15 dB.

$\epsilon \equiv 100\% \times (T_{e,VNA} - T_{e,Y})/T_{e,VNA}$

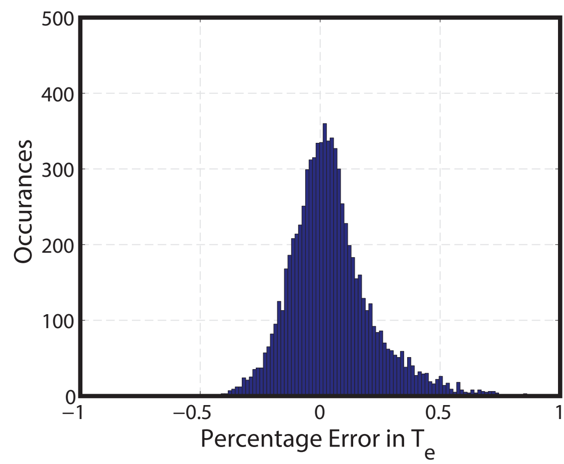
IC #	2	3	4	5	6
DATA POINTS	7,587	7,907	7,553	7,647	7,313
RMS ϵ	16%	13%	8%	7%	9%
Mean ϵ	14%	5%	-3%	4%	6%
Std. Dev. ϵ	12%	17%	9%	9%	10%

3.2.2.3 Error Calculations

To study the noise temperature (T_e) measurement error in more detail, the relative error for all data points, that were within the defined measurement dynamic range, were calculated. The histogram plots of relative errors are shown separately for each integrated circuit in Figure 3.12. Statistics for each IC are presented in Table 3.1. With mean error values less than 15 percent and standard deviation of less than 20 percent these statistics show promising results for employment of the on-chip noise source, while performing the calibration of T_{hot} for a single IC.



(a)



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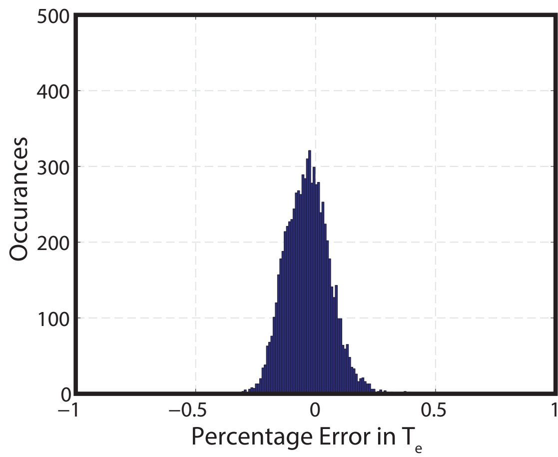

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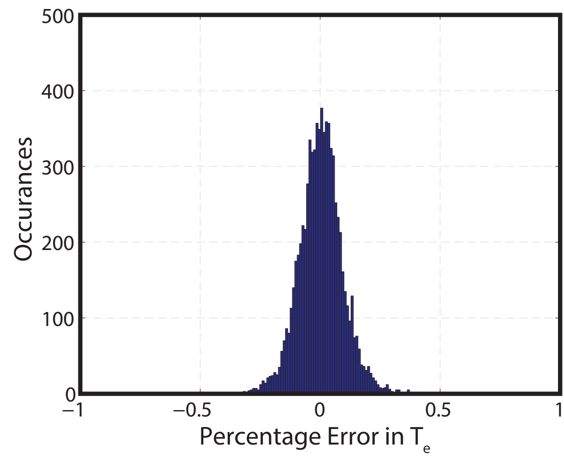

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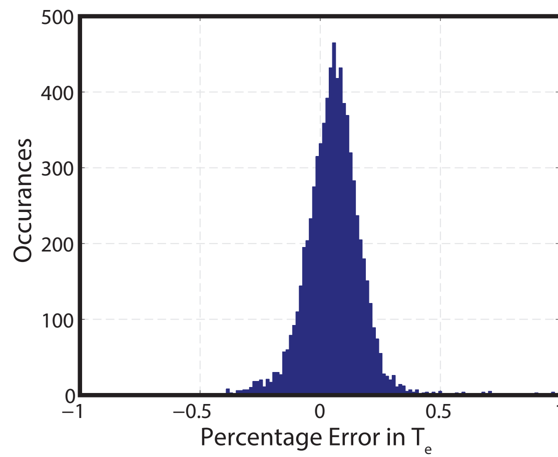


(e)

Figure 3.12. Histograms of relative errors in T_e measurements of (a) IC2, (b) IC3 , (c) IC4, (d) IC5 ,and (e) IC6

This chapter presented a step by step measurement and processing procedure for calculation of noise using the proposed noise source. Measurement results of the commercial network analyzer were used as a reference data for comparison to the results taken by the proposed technique. Using the hypothesis that the ENR of the noise source should be repeatable enough between different ICs, the calibration of T_{hot} was only performed for on IC. This hypothesis was tested by using the extracted T_{hot} for one IC, for noise measurements of other ICs. Comparison of the results using the noise source, with the reference measurements confirmed the aforementioned hypothesis. Statistical data for error in noise measurement using the in-situ noise source were presented and showed very promising results.

CHAPTER 4

CONCLUSION AND FUTURE WORK

In this thesis a new, step-by-step technique for built-in self-test of noise for mm-wave applications was presented. In the first part of the thesis, available methods for noise measurements (Y-factor and cold source method) along with their advantages and disadvantages, were discussed. This study suggested that, due to requirements for absolute measurements of power, gain and bandwidth, the cold source method is difficult to use for on-chip applications. In contrast, the Y-factor method only required relative measurements of power and is more suitable for on-chip applications. In the second chapter of the thesis, requirements for the noise source, to enable the built-in self-test of noise for on-chip mm-wave applications, were discussed. These requirements included high output ENR at frequencies in the range of 20-35 GHz and constant impedance termination in both on and off states. A state-of-the-art CMOS noise source was presented to meet these requirements. To test the performance of the noise source, a highly reconfigurable low noise amplifier was used as the device under test. An active transcoductance based input stage was employed for coupling the noise source to the input of the DUT.

The circuit was fabricated in IBM 32nm SOI CMOS technology and was tested using a step by step measurement procedure. Based on the hypothesis that the ENR of the noise source should be repeatable enough among different ICs, calibration of T_{hot} was only performed for one chip. The comparison of the noise measurements taken by the proposed technique with reference measurements from the VNA, showed promising results. The error in noise measurements using the proposed technique was calculated to be less than 0.5 dB

for the majority of measurement points. This proved the capability of the proposed noise source for on-chip noise measurements for mm-wave applications.

4.1 Future Work

As mentioned in the first chapter of this thesis, the final goal of is to implement a complete built-in self-test system for noise which includes the noise source and a spectrum analyzer on-chip. Future work should be done to enable the integration of the complete system-on-a-chip (SoC), which requires the development of a receiver system and additional IF processing circuitry. Moreover, additional digital processing on-chip and the complete system can enable the development of self-optimizng systems. It is well known that the data from Y-factor measurements can also be used for the measurement of gain [33]. Although, the calculation of gain requires absolute measurements of power, it can be done using same set of measurements. As an initial work this was done using the available data collected for this thesis.

4.1.1 Gain Measurements Using Y-factor Method

The data from Y-factor measurement can also be used for gain measurements of the DUT [33]. Assuming a linear response of the LNA, the gain can be found using the slope between hot and cold measurements as shown in Figure 4.1. This assumption is valid for gain measurements of LNAs, as the power presented by the noise source is much lower than the compression point of the amplifier.

Using the spectrum analyzer measurements the power at the output of the DUT can be found by subtracting the total gain of the attenuator in series with the external amplifier which is approximately 15 dB. The change in output powers, ΔP_{out}, can be found by subtracting linear hot/cold output powers. Similarly, the change in input power, ΔP_{in}, can also

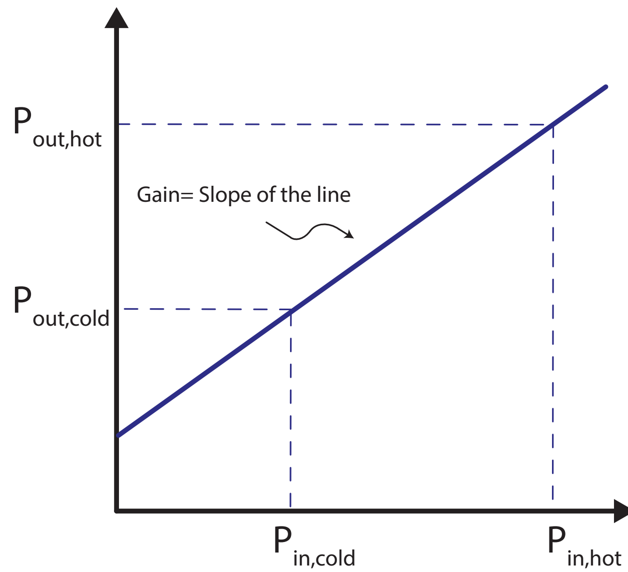


Figure 4.1. Graphical representation of the gain measured using Y-factor. Reproduced from [33]

be found by subtracting the power for the noise source in on- and off-states. To find the input power difference, the extracted T_{hot} can be used. Then, ΔP_{in} can then be found using,

$$\Delta P_{in} = 4kB(T_{hot} - T_{cold}) \tag{4.1}$$

where B is the noise bandwidth which is the resolution bandwidth of the spectrum analyzer measurement, and T_{cold} is the ambient temperature which is 290 K. Knowing the ΔP_{in} and ΔP_{out} the power gain can be found as

$$Gain = \frac{\Delta P_{out}}{\Delta P_{in}}. \tag{4.2}$$

A factor of 10 dB has been added to the calculated results to match the measurement results. This was necessary, likely due to the loss in cables and probes as well as mismatch between the output of the DUT and the receiver system.

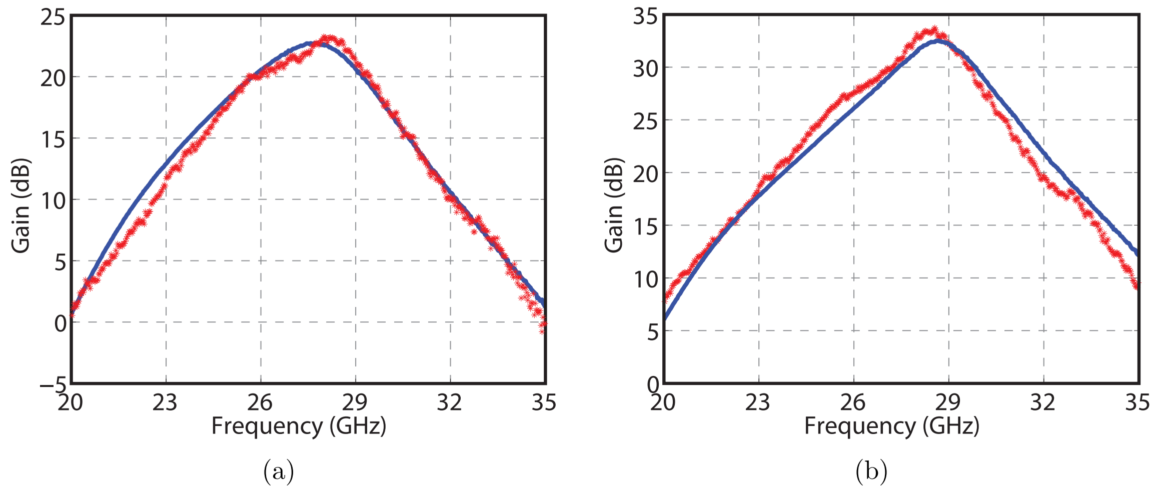


Figure 4.2. Comparison of gain measurements using the Y-factor data (red symbols) and VNA measurements (blue line) for (a) state 2 for IC3 and (b) state 19 for IC3.

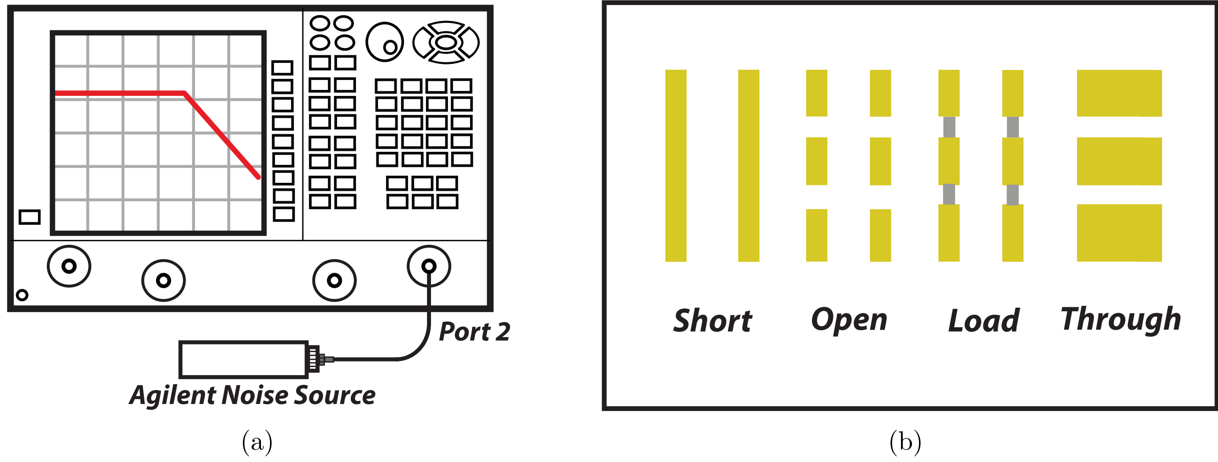
The comparison of gain measurement using the noise source and data collected by the VNA for two sample states is shown in Figure 4.2. This Comparison shows promising results despite having to use absolute measurements of power. If the spectrum analyzer was to be implemented on-chip, the calibration of the gain for absolute measurements of power could be done for more precise gain measurements. However the implementation of the noise source is primarily for on-chip noise measurements, these initial results show that the gain can be also found using the same set of measurement results. It is expected that future work will be done for development of a gain measurement procedure using the Y-factor data.

APPENDIX A

VNA NOISE CALIBRATION

The VNA used in this work, employs the cold source method for noise measurements. The cold source method requires a well known termination at the input of the DUT, thus the actual termination needs to be calibrated before each measurement. There are two types of noise calibration techniques available with the VNA used for this work, named vector noise calibration and scalar noise calibration [33]. In the scalar noise calibration, it is assumed that the impedance presented by the test fixtures is a perfect 50 Ω. This assumption may create an error in noise measurements since the impedance is usually different from 50 Ω. On the other hand, in the vector noise calibration procedure, instead of assuming a 50 Ω termination, an impedance tuner is used at the input port to characterize the deviation from perfect 50Ω match. This tuner can switch between four different known impedances. The four different measurements done with these known terminations, are used to estimate the four noise parameters as defined in [31], using four equations and four unknowns. These noise parameters are then used to find the actual noise figure value for the 50 Ω termination. Throughout this work all measurements were taken using the vector noise calibration for higher accuracy.

For the VNA to use the cold source method, the knowledge of the gain of the DUT as well as the gain bandwidth product of the noise receiver are required. The gain bandwidth product of the receiver system is found during the calibration procedure and the gain of the DUT is measured during the s-parameter measurements of the DUT. This is why for each noise figure measurement sweep, an s-parameter measurement sweep is required as well.



(a) (b)

Figure A.1. (a) Calibration of the noise receiver using a commercial noise source. (b) schematic of a calibration substrate with short, open, load and through structures, used for on wafer calibration of single ended ground-signal-ground (GSG) probes.

The actual noise calibration of the VNA includes two main steps, calibration of the noise receiver and on-wafer calibration. The calibration of the noise receiver is done with the connection of a commercial noise source, with a known ENR, to port 2 of the VNA (as shown in Figure A.1(a)). Since the noise measurements are supposed to be done with RF wafer probing, an on-wafer calibration is required for characterizing cables, connectors, adaptors and wafer probes, which is done by landing input and output probes on short, open, load, and through (SOLT) terminations on a calibration substrate. Figure A.1(b) shows a schematic diagram of a calibration substrate used for on wafer calibration. Performing these calibration steps ensures a very close to perfect 50 Ω system to the tip of the probes.

APPENDIX B

COMPLETE MEASUREMENT RESULTS

In this chapter more examples of comparison of noise measurements acquired with on-chip noise source and the network analyzer are presented. An example for each of the twenty states is shown for demonstration of different scenarios.

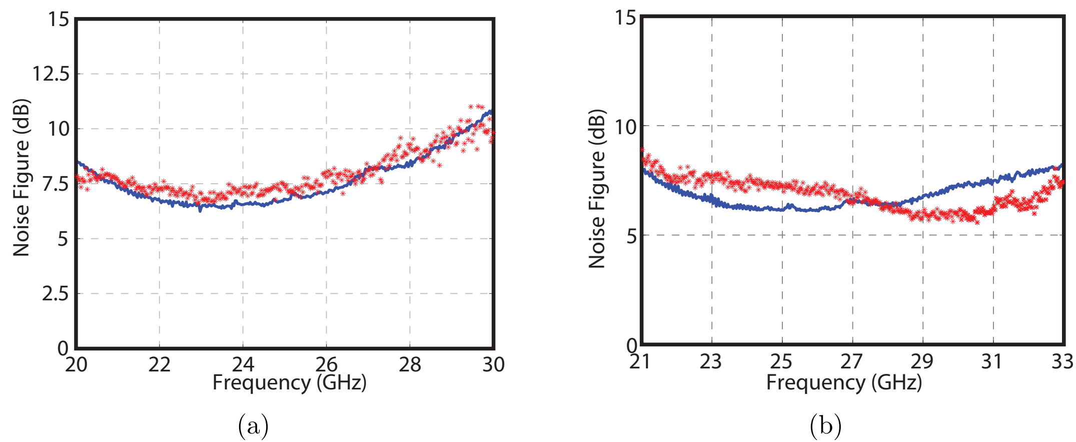
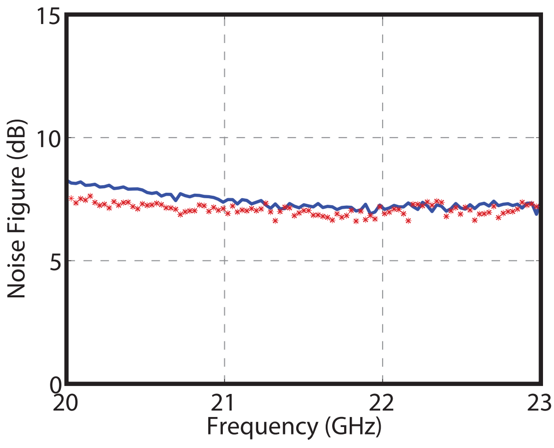


Figure B.1. Example plots comparing the reference NF measurements with Y-factor measurements for states 1 and 2



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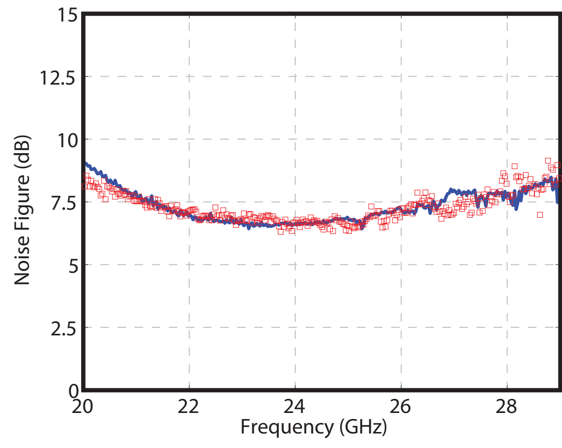

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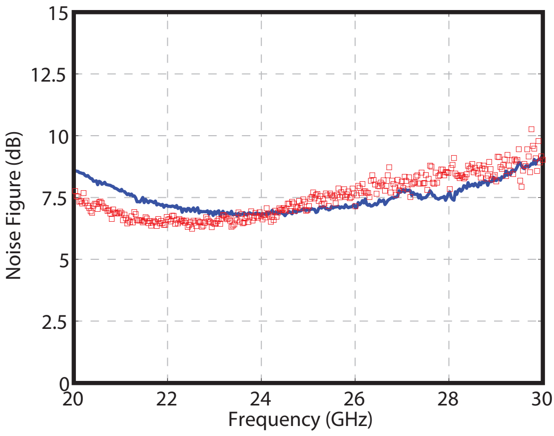

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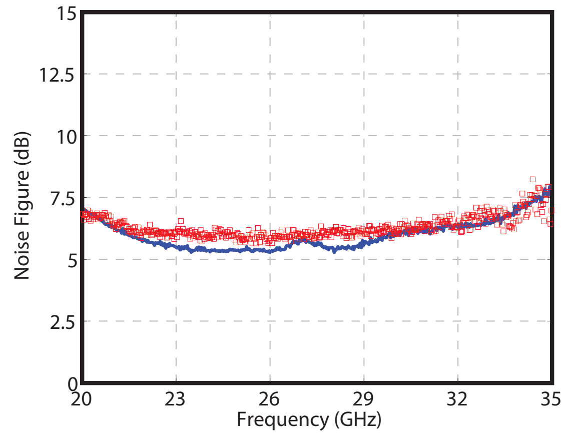

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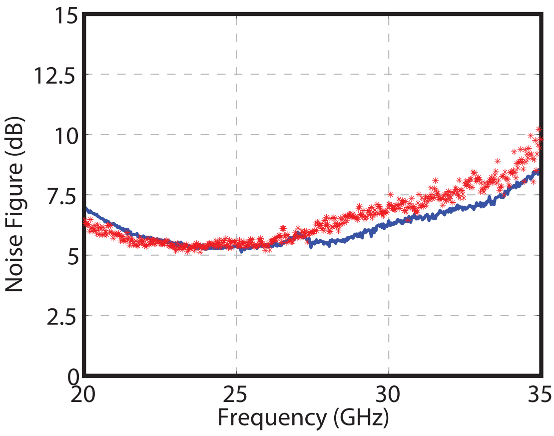

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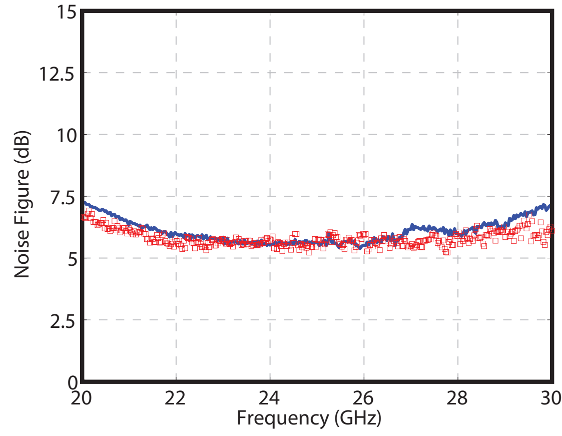
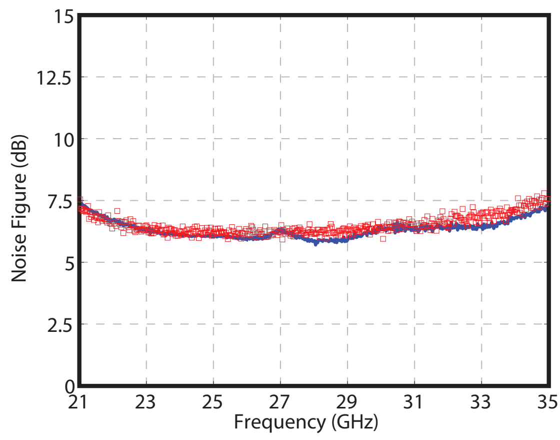


(f)

Figure B.2. Example plots comparing the reference NF measurements with Y-factor measurements for states 3 to 8



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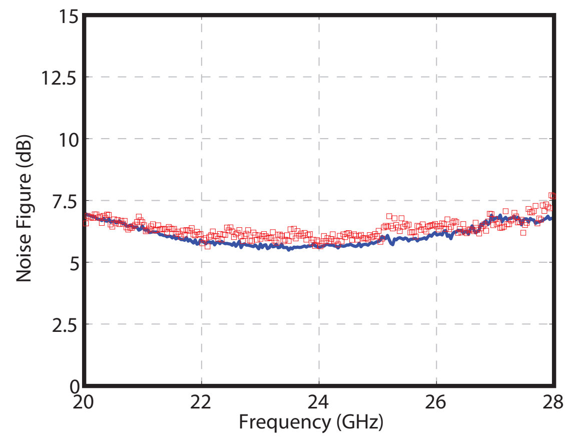

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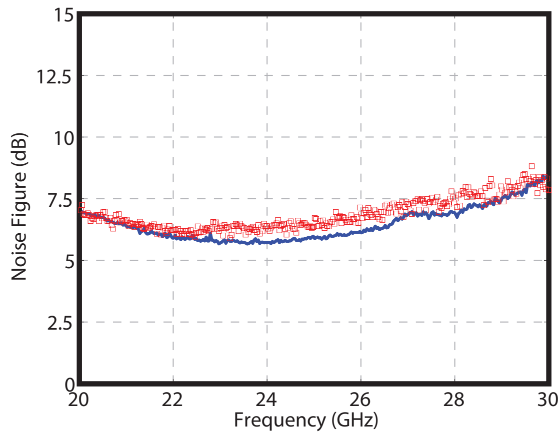

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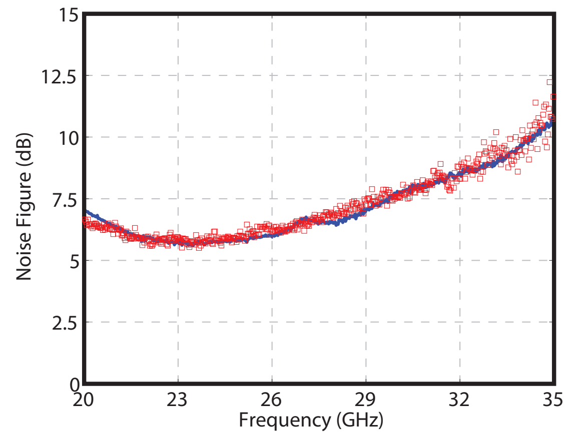

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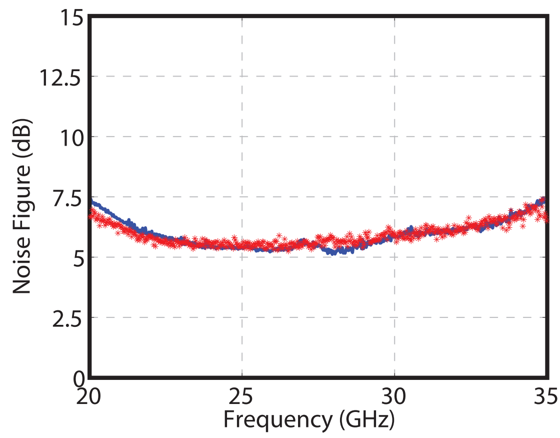

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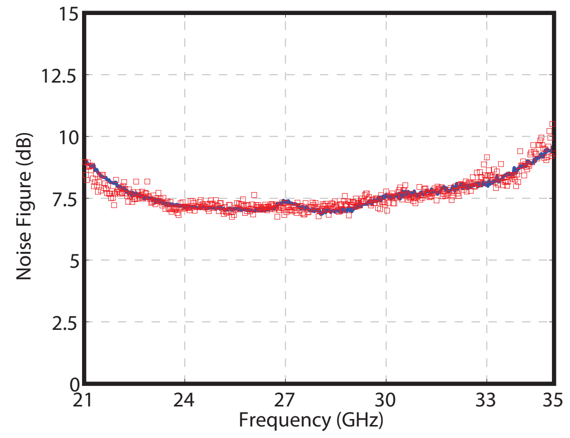

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Figure B.3. Example plots comparing the reference NF measurements with Y-factor measurements for states 9 to 14

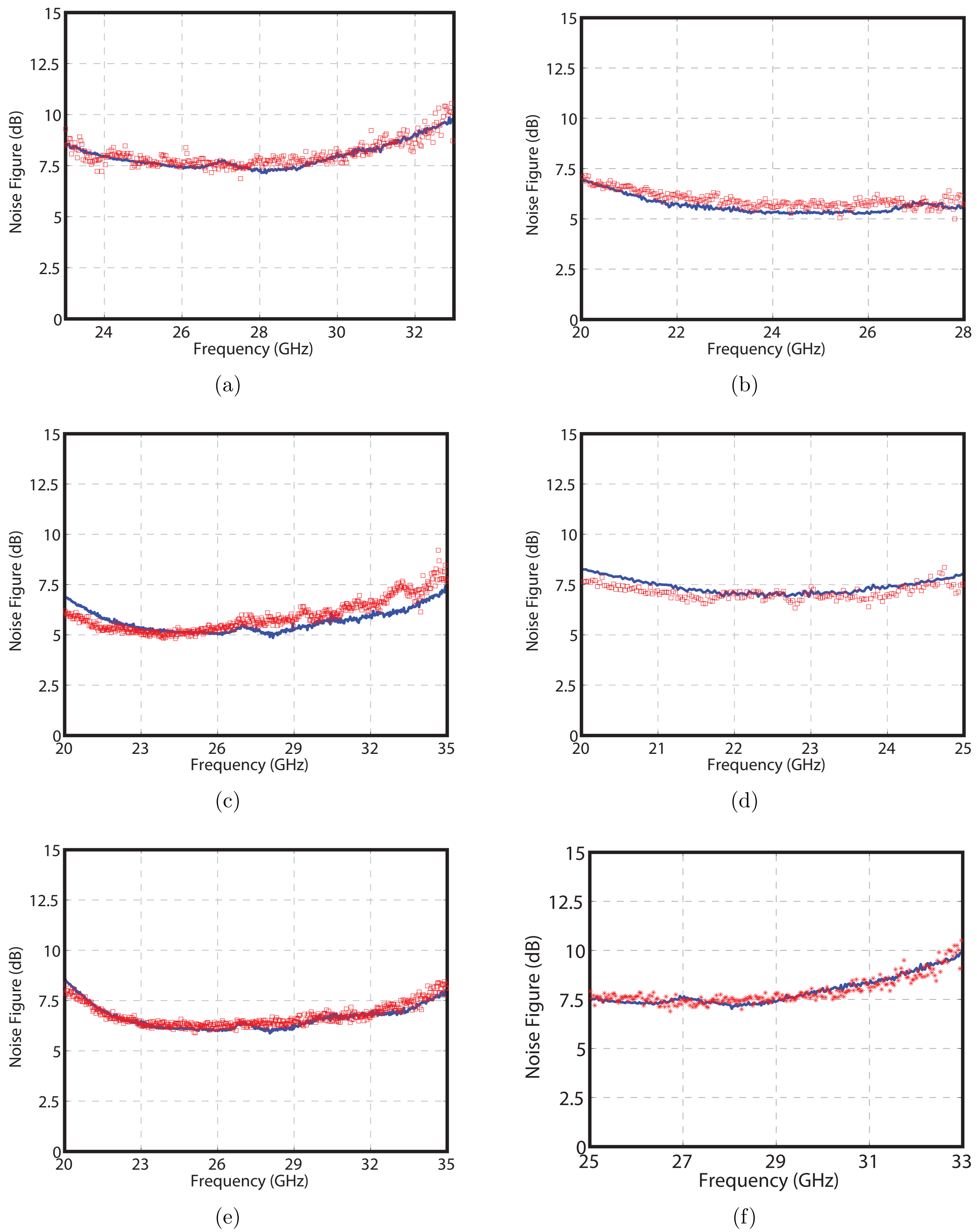

Figure B.4. Example plots comparing the reference NF measurements with Y-factor measurements for states 15 to 20

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