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Analysis of Modulation and Voltage Balancing Strategies for Modular Multilevel Converters

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ANALYSIS OF MODULATION AND VOLTAGE BALANCING STRATEGIES FOR MODULAR MULTILEVEL CONVERTERS

by

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ABSTRACT

Modular multilevel converters are an emerging voltage source converter topology suitable for many applications. The increased utilization of HVDC power transmission solutions has resulted in modular multilevel converters becoming a more common converter type. Other applications include interfacing renewable energy power sources to the grid and motor drives. Modular multilevel converters are beneficial for medium voltage motor drives because the properties of this converter topology, such as low distortion, allow for an efficient motor drive design.

Modular multilevel converters use numerous low-rated IGBTs to produce the desired voltage. The converter is made up of a series of IGBT half-bridge circuits with a capacitor across both devices. Benefits of this converter include reduced semiconductor device costs due to the ability to use more commercially available low-rated IGBTs and reduced or potentially the elimination of filter components. The number of voltage levels which corresponds to the number of submodules is what causes the harmonic reduction allowing for this omission. Other benefits include lower operating switching frequencies which also results in reduced converter losses. A drawback to using modular multilevel converters is an increase in the complexity of the control schemes and data processing requiring many more sensors and because of this a thorough understanding of the benefits and limitations of all the control strategies is desired.

One area of control flexibility is in the pulse width modulation and voltage balancing algorithms applicable to modular multilevel converters. The pulse width modulation options are multicarrier solutions that focus on two categories: phase-shifted PWM which utilizes multiple carrier waveforms with the same frequency and amplitude but a different phase shift and level-shifted techniques which utilize multiple carrier waveforms with identical frequency and amplitude but a different DC bias. An important aspect of modular multilevel converters is that the capacitor voltages need to be as closely balanced to the desired DC voltage as possible with a typical acceptable voltage ripple of 10%. In order to achieve this, various voltage balancing algorithms have been developed for modular multilevel converters with this work focusing on two common algorithms.

This work focuses on analyzing both modulation techniques and voltage balancing algorithms using a range of metrics to better understand the most applicable strategies based on the specific application of the converter. A MATLAB/Simulink model using SimPowerSystems of a 20-level three phase modular multilevel converter has been built in order to implement and analyze the various methodologies. The result will be a comprehensive analysis of the optimal approach based on capacitor voltage ripple, converter power loss, and converter voltage THD.

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LIST OF ABBREVIATIONS

PWM..... Pulse Width Modulation

IGBT..... Insulated-Gate Bipolar Transistor

SM ..... Submodule

PSC-PWM .....Phase-Shifted Carrier Pulse Width Modulation

PD-PWM ..... Phase-Disposition Pulse Width Modulation

POD-PWM.....Phase Opposite Disposition Pulse Width Modulation

APOD-PWM.....Anti Phase Opposite Disposition Pulse Width Modulation

Chapter 1

Introduction

Modular multilevel converters are an innovative technology that allows voltage source converters comprised of low voltage IGBT switches to be used in medium and high voltage applications. There are several types of multilevel converter topologies and while the fundamental concepts are similar, there are differences in the control requirements across these various topologies. The various multilevel converter topologies include: Cascaded H-Bridge, Diode-Clamped, flying capacitor and modular multilevel converters. This thesis will focus on the modular multilevel converter topology that will be explained below. With multiple device networks connected in series, modules in the sequence can be connected in or shorted out to achieve the desired voltage level. This results in a "staircase" converter voltage with the waveform quality being directly tied to the number of voltage levels utilized, which is the number of submodules in the converter, and the quality of the control approaches employed.

There has been substantial progress in the development of pulse-width modulation techniques, voltage balancing algorithms and conventional control approaches applicable to modular multilevel converters. As far as the current and voltage control, the same approach for a conventional voltage source converter can be used. This scheme uses PI controllers to control the current along with the active and reactive power. The control

that is specific to modular multilevel converters is the multicarrier pulse width modulation and voltage balancing algorithm. The number of carriers in the PWM scheme equals the number of submodules per arm of the converter. The goal of the voltage balancing algorithms is to make the selection of which submodules to switch on or off that results in the lowest capacitor voltage ripple. There are many solutions with computation complexity, power loss and equivalent switching frequency being key factors in the algorithm selection. In this thesis, various pulse-width modulation techniques and voltage balancing algorithms will be explored by analyzing key metrics to proper converter operation. The average capacitor voltage ripple, converter power loss including switching power loss, conduction power loss and arm inductor power loss and converter voltage harmonics will be analyzed for each pulse-width modulation technique and balancing algorithm to fully understand the effect of each method.

1.1 Background

Modular multilevel converters were first developed by Dr. Lesnicar in [1] to be used for high voltage applications. [2] and [3]also discuss the origin of this topology. A modular multilevel converter consists of a sequence of sub-modules connected in series for each phase of the converter. A submodule, shown in Figure 1.1, consists of two IGBTs connected in a half-bridge topology with a capacitor across the devices to be used as an energy storage and supply device. Also shown is that the output terminals that actually connect to the converter are across the lower IGBT. This shows that the capacitor across the two devices is either directly connected into the converter or shorted out depending on the state of the driving gate signals.

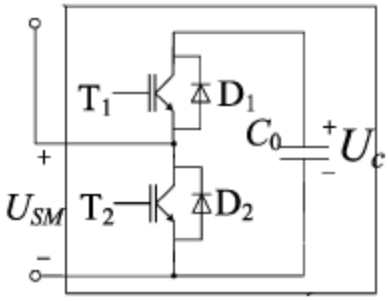

Figure 1.1 Sub-module [4]

Other properties of the converter topology are that this sequence of submodules along with an arm inductor makes an arm of the converter as shown in Figure 1.2.

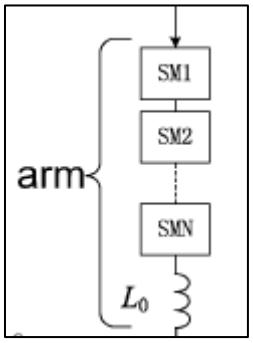

Figure 1.2 Modular Multilevel Converter Arm [4]

Two arms make up one phase of the converter, also called a phase unit, and this is shown in Figure 1.3. This phase unit connects to the DC bus via the end of the sequence of submodules. As shown, both arms also contain a series arm inductor, which is used to help limit circulating current and to filter harmonics, and is connected to the AC side via the middle point in between the two inductors.

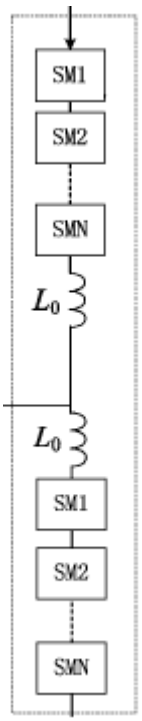

Figure 1.3 Modular Multilevel Converter Phase Unit [4]

Figure 1.4 shows a full breakdown of a three phase modular multilevel converter. Each center point between the arm inductors are connected to the AC side while the phase units are connected in parallel to the DC bus.

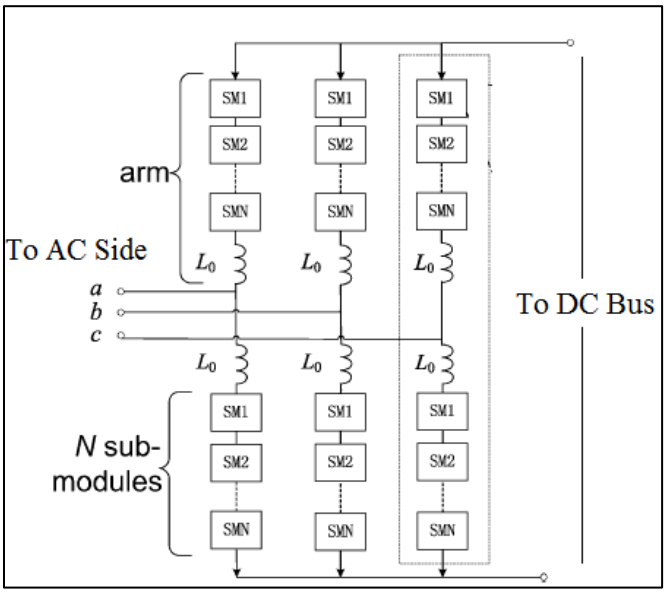

Figure 1.4 Full Modular Multilevel Converter [4]

It is important to understand the conduction paths of the submodules, which depend on whether the IGBT needs to be on or off along with the polarity of the current. Each submodule will be in one of the two states that show one IGBT switched on with the other off. Figure 1.5 shows the various conduction paths when the current polarity is positive and Figure 1.6 shows the various conduction paths with negative current polarity. This will be useful when analyzing the conduction power loss in the converter.

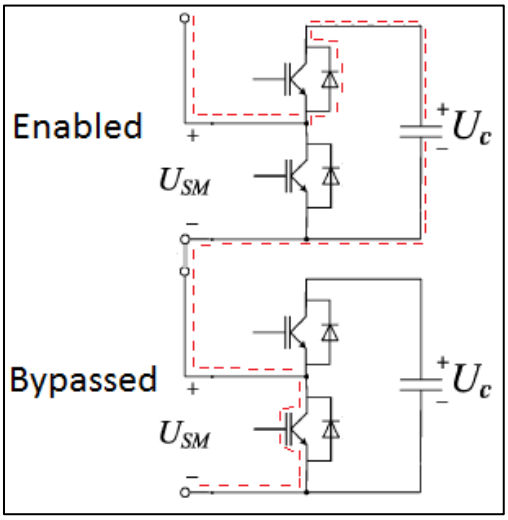

Figure 1.5 Converter Conduction Path, Positive Current

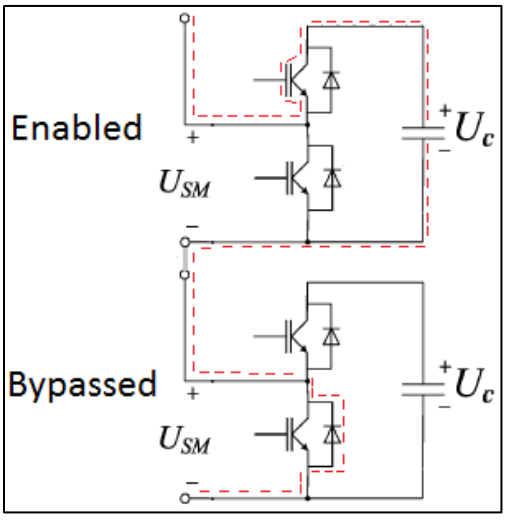

Figure 1.6 Converter Conduction Path, Negative Current

The number of submodules chosen depends on the power levels and applications that will be utilized. A typical minimum number of levels is a 5-level MMC which has four submodules per arm. If the number of submodules is equal to N, then the modular multilevel converter is described as a (N+1)-level MMC. This is because 0 volts is included as a voltage level.

1.2 Converter Operation

1.2.1 Converter Reference

The multicarrier modulation schemes used for modular multilevel converters dictate the number of submodules that need to be on in an arm. This generates a voltage level between zero and the maximum converter voltage amplitude for the upper arm of each phase unit. Two references are required per phase, one for each arm. This reference is then compared to the multiple carriers discussed and a reference is generated with an available range of values from zero to N. As an example, Figure 1.7 shows the resulting reference waveform for a 5-level MMC using a sinusoidal reference. The PWM output value here dictates the number of connected submodules in an arm.

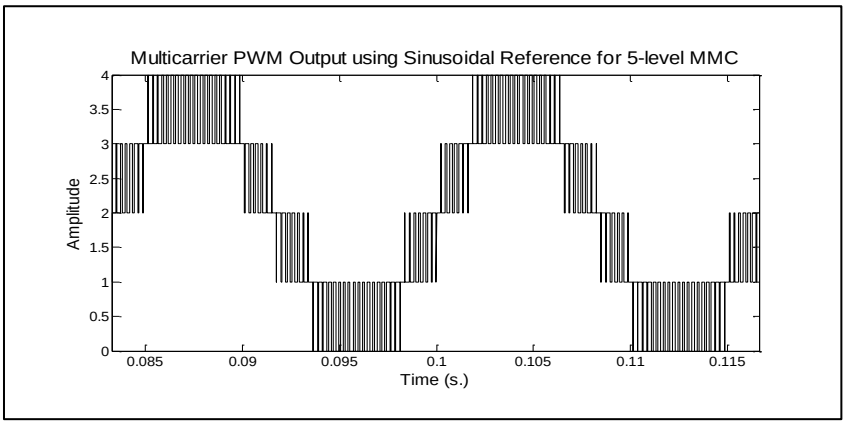

Figure 1.7 Reference Waveform 5-level MMC

A key principle to be understood is that in an ideal situation, the capacitors across each submodule can be modeled as an ideal DC voltage source. Switching in and out these DC voltage sources allows us to generate various voltage levels on the AC side. These various voltage levels allow the capability of producing an AC waveform with the resolution being directly tied to the number of submodules used in the converter. For example, Figure 1.8 shows a 5-level MMC voltage waveform and this figure shows how the various voltage levels are achieved by switching submodules on and off. In this case, a sinusoidal reference is tied to a multi-carrier PWM solution to generate this waveform.

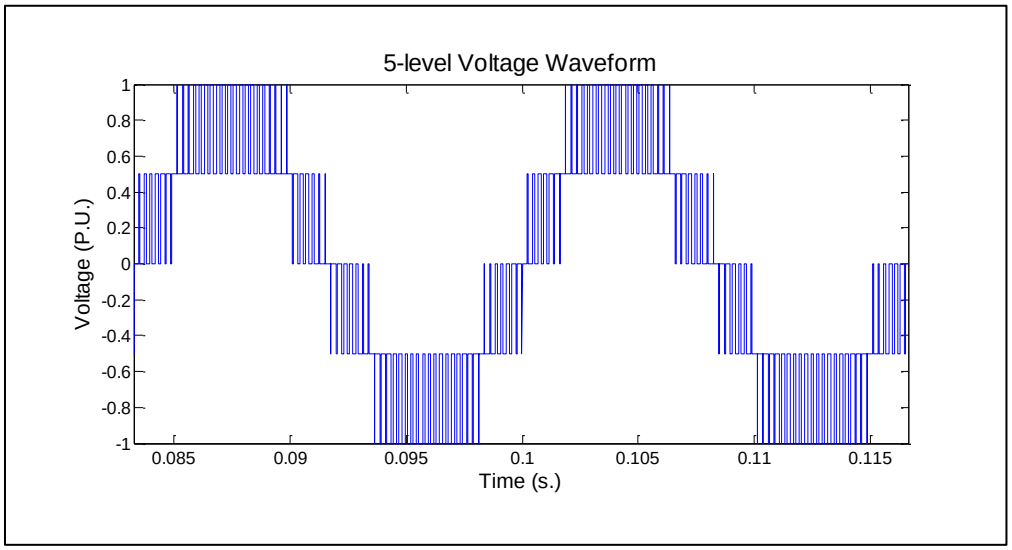

Figure 1.8 5-level Voltage Waveform

1.2.2 Relationship between arms in phase unit

Another important concept of modular multilevel converters is that in each phase unit, the number of submodules connected in the upper arm needs to be complementary to the number on in the lower arm. If we assume a converter has N number of submodules per arm and that the number of submodules connected in the upper arm is Non, then the number of submodules that need to be on in the lower arm should be equal to (N-Non). This helps to illustrate that since the submodules in the respective arms

cannot independently switch, the number of voltage levels the converter is capable of producing is in fact equal to the number of submodules in each arm.

1.3 Conventional Control Scheme

The voltage and current control schemes are identical for a three phase conventional half-bridge and for a modular multilevel converter. This converter control is discussed in [5] and [6]. In order to develop the controllers, a conventional 3-phase half-bridge voltage source converter is considered particularly the AC side voltage and impedance, as shown in Figure 1.9. A plant transfer function is required to tune these PI controllers. Here, Kirchhoff's voltage law is used to develop a state space model of this converter. Equation (1) shows the KVL equation and equations (2) and (3) show the resultant state space derivation. The next step is to convert this state space equation to the frequency domain. Equation (4) shows the s-domain plant transfer function. A MATLAB script was developed to then solve the loop transfer function to solve for the Kp and Ki parameters. This design requires choosing both a cutoff frequency and a phase margin. A typical acceptable phase margin of 60° was used. The cutoff frequency should be roughly a decade below the switching frequency so a cutoff frequency of 500 Hz was chosen. These parameters are used to design the current PI controllers.

$$Voc(t) = Es + Rs * io(t) + Ls * \frac{dio}{dt} \tag{1}$$

$$\frac{dio}{dt} = \frac{1}{Ls} * Voc - \frac{Rs}{Ls} * io - \frac{1}{Ls} * Es \tag{2}$$

$$\dot{x}1 = -\frac{Rs}{Ls} * \mathrm{x}1 + \left[\frac{1}{Ls} - \frac{1}{Ls}\right]\frac{Voc}{Es} \tag{3}$$

$$G(s) = \frac{1}{Rs} * \frac{1}{1 + s * \frac{Ls}{Rs}} \tag{4}$$

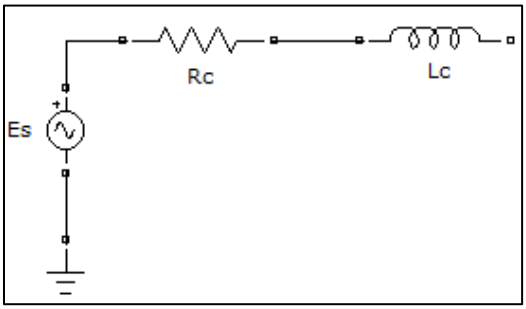

Figure 1.9 AC Voltage and Impedance

The next step was to design the voltage PI controllers used to control active and reactive power. In this case, there needs to be a term in the control loop that relates the voltage loop to the current loop. This is the gain of the current loop front the perspective of the voltage loop and is only valid when the voltage loop is much slower than the current loop. This term is simplified as a single pole at the current loop cutoff frequency. Also included is a relationship between conductance and both voltage and current. A similar MATLAB script is developed to solve for the Kp and Ki parameters. These controllers were designed considering a single phase. To move to three phase controllers, the Ki parameters need to be doubled.

Chapter 2

MMC MODULATION METHODS AND VOLTAGE BALANCING ALGORITHMS

2.1 Modulation Methods

2.1.1 Fundamentals of Modulation Methods

Conventional pulse width modulation uses one reference waveform and one carrier waveform to generate a gate driving signal. Figure 2.1 shows an example of single update sinusoidal pulse width modulation. The reference is compared to the carrier and if the carrier is lower than the reference, the PWM output is high and if the carrier is higher than the reference then the PWM output is low. Figure 2.2 shows the resultant output of the sinusoidal method. Considering the three phase half bridge circuit discussed in Chapter 1, this pulse width modulation technique can be used to control a conventional voltage source converter. The PWM waveform shown in Figure 2.2 controls one phase of the converter. This PWM signal controls the top switch in the half-bridge circuit while the inverse of this signal controls the bottom switch in the circuit. For modular multilevel converters, there are several of these half-bridge circuits in the converter that all need to be individually controlled. The solution to this issue is to use multicarrier PWM methods. A carrier waveform is required for each half-bridge circuit, or submodule, in the converter.

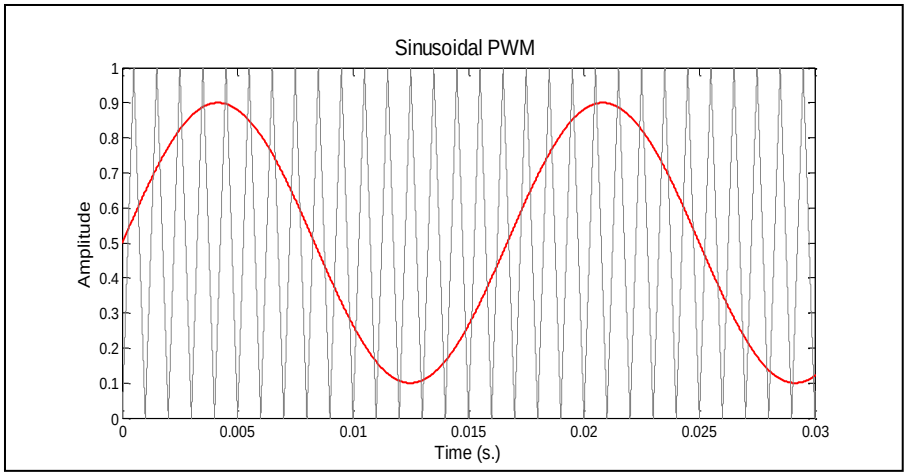

Figure 2.1 Sinusoidal PWM Example

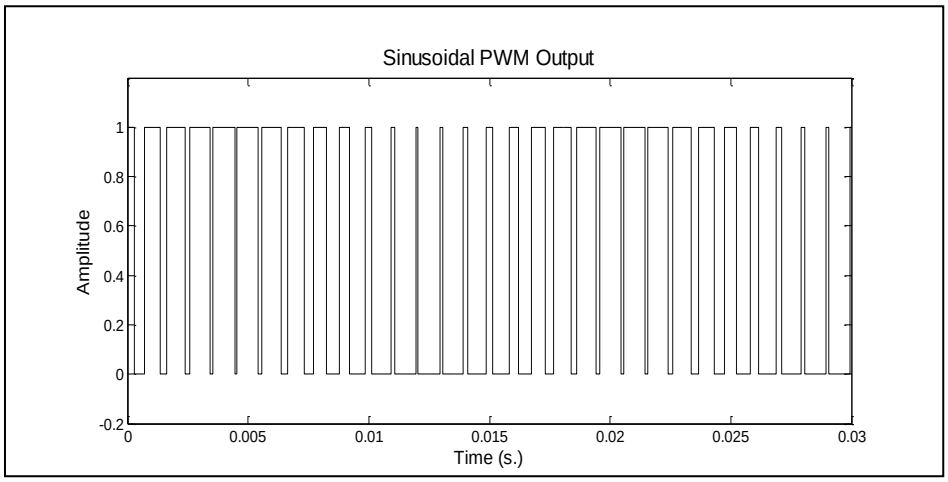

Figure 2.2 Sinusoidal PWM Output

[7] and [8] discuss multilevel converter PWM solutions. There are two main categories in regards to multicarrier modulation techniques for modular multilevel converters and they are phase-shifted and level-shifted. Both methods rely on the concept of one carrier waveform corresponding to each submodule in an arm of the converter. Phase-shifted methods apply an equal phase shift to each of the carriers while level-shifted techniques apply a varying DC bias to each carrier waveform. These multiple carrier waveforms are all compared to a single reference generated by the

voltage source converter control and the resultant reference output dictates how many submodules need to be switched on.

One goal of the results of this thesis is to clearly describe the benefits of one method compared to the other.

2.1.2 Phase Shifted Modulation Technique

Phase-shifted carrier pulse width modulation specifically for modular multilevel converters uses one carrier for each submodule in the arm. These carrier waveforms, typically triangular waveforms but saw tooth waveforms are also an option, are then equally phase shifted apart. The appropriate phase shift is calculated using (5).

$$Phase\,Shift = \frac{360}{N},\ for\ N = Number\ of\ SMs \tag{5}$$

Two key parameters are the amplitude and frequency modulation index. The equations to calculate these parameters are shown in (6) and (7). The frequency modulation index relates the device switching frequency to the fundamental frequency of the converter. In (6), fcr is the carrier frequency chosen and mf is the fundamental frequency or 60 Hz.

$$fm = \frac{fcr}{mf} \tag{6}$$

The amplitude modulation index relates the difference in deviation between the carrier and reference waveform. In (7), we can see that it is simply the relationship the amplitude of the reference to the carrier.

$$am = \frac{Dev(ref)}{Dev(car)} \tag{7}$$

Figure 2.3 shows an example of PSC-PWM with 20 carrier waveforms and 1 reference waveform. Also shown is an 18° phase shift between each carrier waveform which satisfies (5). Figure 2.4 shows the resultant reference waveform which dictates how many submodules need to be connected in the arm in order to achieve the desired voltage level.

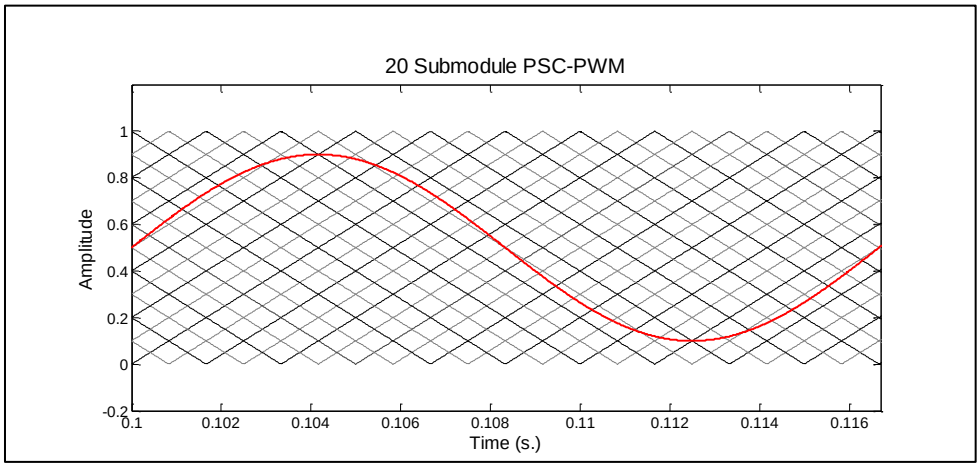

Figure 2.3 PSC-PWM

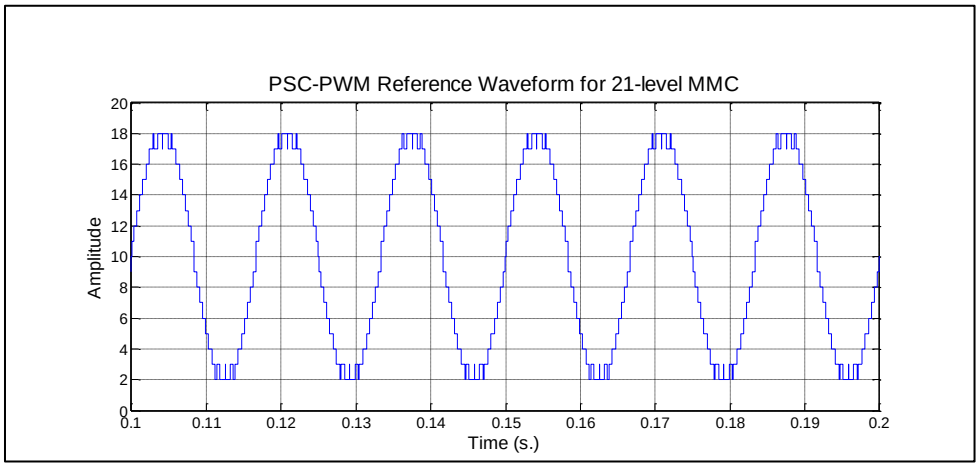

Figure 2.4 PSC-PWM Reference Waveform

2.1.3 Level-shifted Modulation Technique

Level-shifted carrier pulse width modulation is similar to the previously described methods in that again the number of carrier waveforms is equal to the number of

submodules in each arm. The difference is, for this technique, each carrier waveform has a different DC bias applied depending on the equation shown in (8).

$$Bias = \frac{1}{N},\ for\ N = \text{Submoduels per arm} \tag{8}$$

There are various types of level-shifted techniques which depend on whether or not the carrier waveforms are 0 degrees out of phase or 180 degrees out of phase. The first is phase-disposition PWM. Figure 2.5 shows an example of phase-disposition PWM by showing 20 carrier waveforms superimposed with a single sinusoidal reference waveform. Figure 2.6 shows the reference signal using PD-PWM.

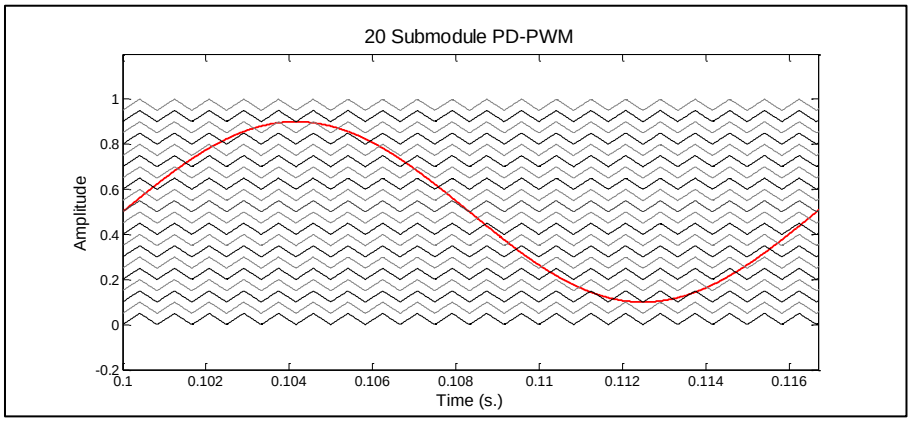

Figure 2.5 PD-PWM Carrier Waveforms

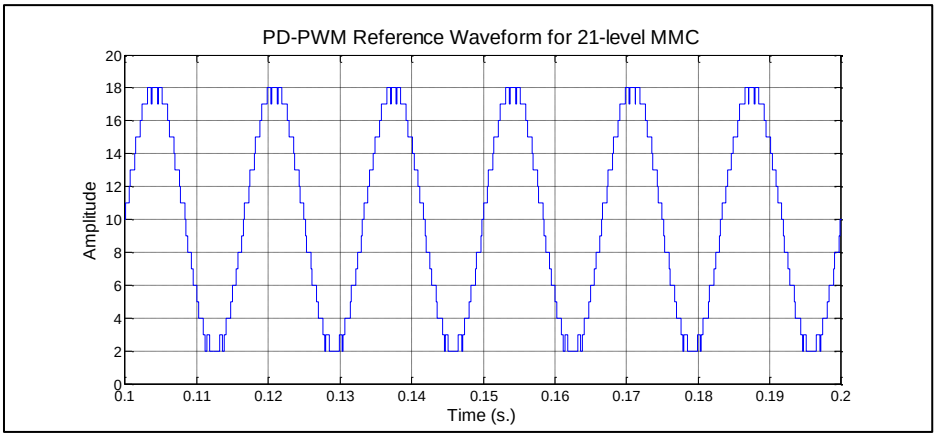

Figure 2.6 PD-PWM Reference Waveform

Here, each carrier waveform has the same frequency and phase but an equal DC bias spacing of 0.05 calculated using (8). This is assuming a normalized per unit reference waveform.

The next level-shifted technique discussed is phase opposite disposition PWM which is identical to phase-disposition PWM except that the lower half carrier waveforms are 180 degrees out of phase. Figure 2.7 shows the carrier waveforms for phase opposite disposition PWM and we can see that the bottom half carrier waveforms are 180 degrees out of phase. Figure 2.8 then shows the resultant waveform.

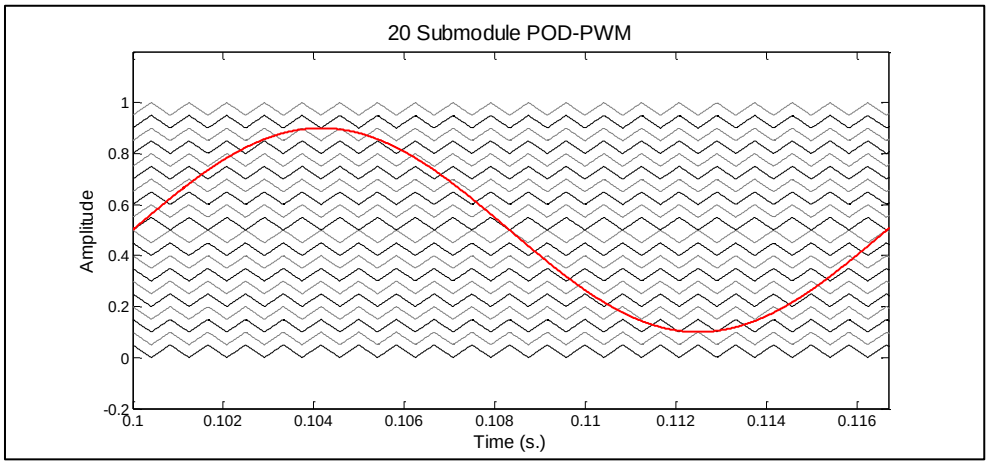

Figure 2.7 POD-PWM Carrier Waveforms

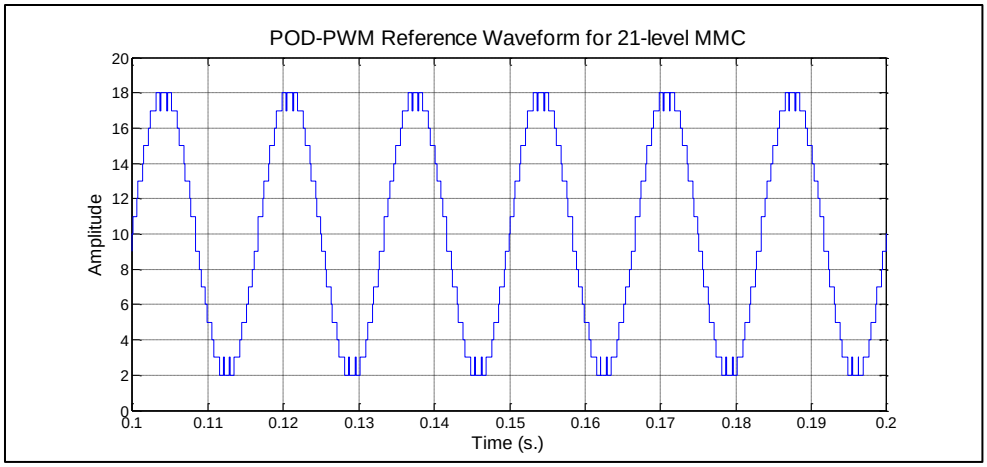

Figure 2.8 POD-PWM Reference Waveform

The final level-shifted technique to be investigated is alternating phase opposite disposition PWM in which every other carrier waveform is phase shifted 180 degrees out of phase. Figure 2.9 shows the carrier waveforms for APOD-PWM and Figure 2.10 shows the resultant waveform.

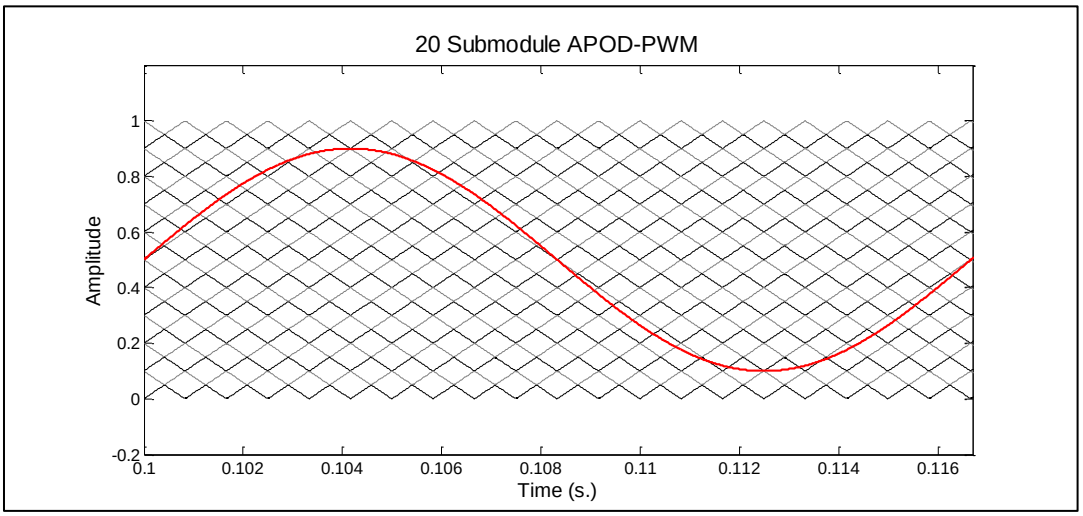

Figure 2.9 APOD-PWM Carrier Waveforms

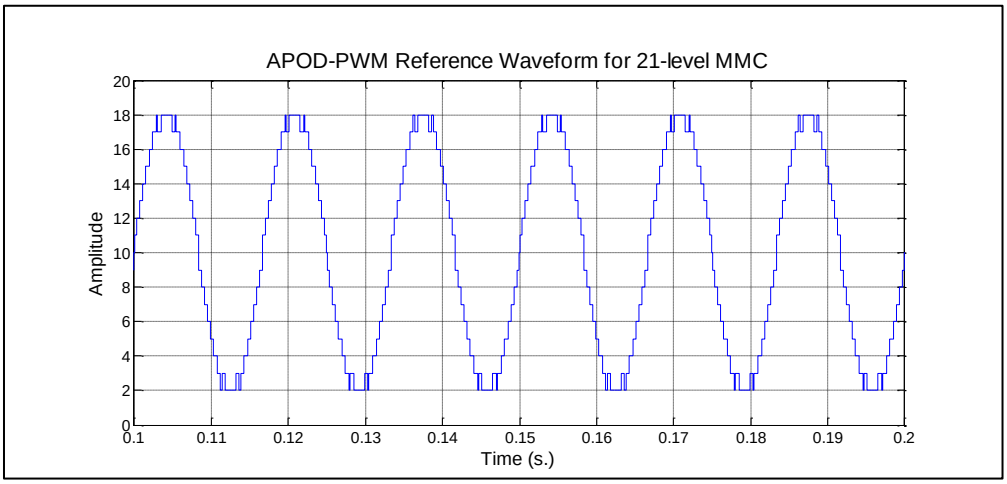

Figure 2.10 APOD-PWM Resultant Waveform

This thesis will analyze the simulation results to compare both the level-shifted techniques against each other and level-shifted techniques as a whole against the phase shifted-technique.

Since this work focuses on analyzing the converter's operation under various switching frequencies, the relationship between switching frequency and carrier frequency needs to be understood. Using a phase-shifted method, for a chosen carrier frequency, the resultant switching frequency is dependent on the number of submodules in the arm, N, and the chosen modulation index. This relationship is described in (9) with N being the number of submodules per arm and fcar is the carrier frequency chosen.

$$fsw = N * fcar \tag{9}$$

For example, for a N=20 converter with a carrier frequency of 250 Hz the switching frequency becomes 5 kHz. For the level-shifted technique, the switching frequency is directly equal to the carrier frequency. Reference [9] claims that the level-shifted methods reduce harmonics better while phase-shifted methods have a lower average capacitor voltage ripple. This will be validated or disputed in this report.

2.2 Voltage Balancing Algorithms

Another important concept to be understood for modular multilevel converters is the balancing of the capacitor voltages of each submodule. As previously described, each submodule can be idealized as an ideal DC voltage source which allows the converter to properly generate the various voltage levels to produce converter side AC voltages. There are many reasons that capacitor voltage balancing is important but fundamentally it is necessary for proper operation of the converter. Reference [1] explains the importance of voltage balancing as follows: "As a result of the SM capacitor voltage variation, the three parallel connected phase units may have different voltages. Consequently, this

leads to circulating currents that flow through the six arms and distort the sinusoidal arm current. Thus, the rms value of the arm current and the converter losses increase".

While each capacitor's voltage is not an exact DC voltage, as a group these voltages can be balanced to within an acceptable capacitor voltage deviation range of typically +- 5-10%. It is important to remember that these capacitors are either charging or discharging depending on the polarity of the arm current. The following will address the potential solutions to this issue and explain some of the obvious benefits and limitations of each method. This will then be validated via simulation results.

There are various algorithms previously designed to combat capacitor voltage deviation in modular multilevel converters. Intuitively, the basic approach would be to utilize the pulse-width modulation reference waveform, capacitor voltages and arm current as inputs to an algorithm. The capacitor voltages dictate how far each voltage is from the ideal value while the arm current shows whether or not a capacitor is charging or discharging. Finally, the reference waveform tells the control scheme the number of submodules that need to be on and the number that need to be off. From these inputs, the voltage balancing algorithm takes the reference value and turns on or off the appropriate number of submodules by selecting the submodules corresponding to the highest or lowest capacitor voltages with this based on the polarity of the arm current.

These are the fundamental principles of all voltage balancing algorithms with the difference arising in how many submodules states are changed each control step which directly affects the resultant switching frequency. The general tradeoff is switching frequency vs. maximum capacitor voltage ripple.

2.2.1 Reduced Switching Frequency Voltage Balancing Algorithm

The most common voltage balancing algorithm operates by only changing the state of 1 submodule for each reference transition. A reference transition is defined as whenever the PWM resultant output waveform changes in value. This is a widely used method that results in the lowest device switching frequency which provides minimized switching loss while still satisfying the capacitor voltage ripple requirement. This thesis will analyze the true benefit of reduced device switching frequency. The algorithm chooses the submodule to switch either on or off based on what is called a best case solution. A flow chart of this algorithm is shown in Figure 2.11.

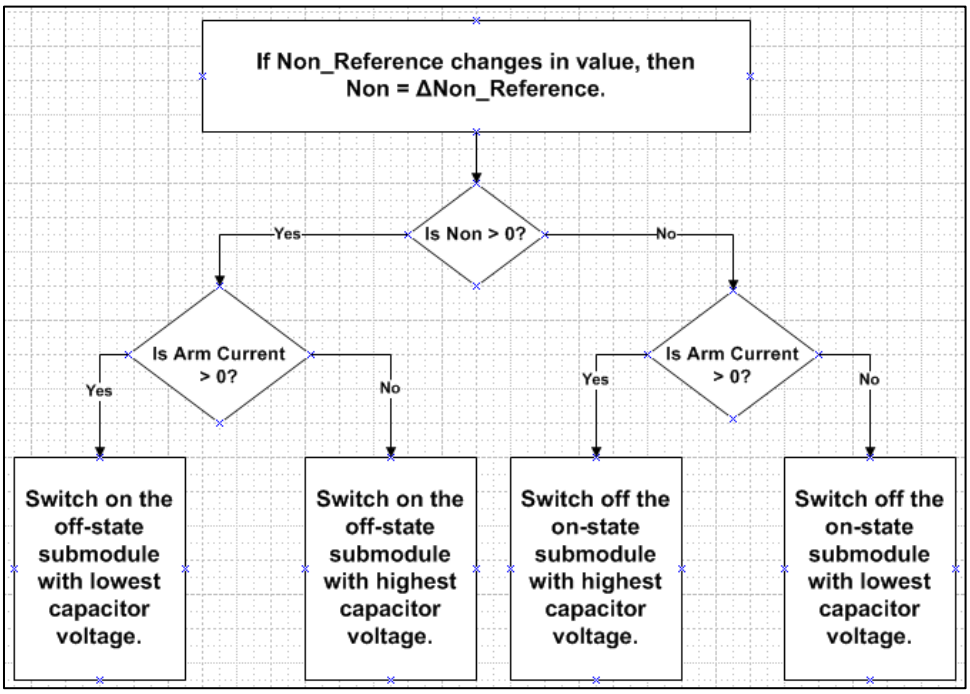

Figure 2.11 Reduced Switching Frequency Balancing Algorithm Flowchart

For the case of the reference waveform increasing if the arm current is positive the submodule that is off with the lowest capacitor voltage is switched on and if the arm current is negative the submodule that is off with the highest capacitor voltage is

switched on. Likewise, for the case of the reference waveform decreasing, if the arm current is positive the submodule that is on with the highest voltage is switched off and if the arm current is negative the submodule that is on with the lowest voltage is switched off. Using this algorithm, the result is properly balanced capacitor voltage with the device switching frequency minimized.

2.2.2 Sorting Method Voltage Balancing Algorithm

An alternative approach improves upon the voltage ripple of each capacitor voltage by increasing the resulting switching frequency. This algorithm requires the same inputs as the first with the main difference being that the algorithm is now able to change the state of as many submodules as is necessary to improve voltage balancing. The algorithm sorts all the capacitor voltages from lowest to highest and uses the pulse width modulated reference signal to dictate the number of submodules that need to be on in an arm. The same check of the arm current polarity is done at every reference transition just like the previous algorithm but for example if the submodules with the lowest voltages are required it switches on or off the submodules corresponding to the lowest capacitor voltages in the sort. The submodules switched then continue in order of capacitor voltage until the desired number dictated by the reference is reached. The result of this algorithm is the best possible voltage balancing with the drawback of significantly increased device switching frequency. This thesis will provide a true picture of the pros and cons of improved voltage balancing vs. increased switching frequency.

2.2.3 Conventional PSC-PWM without Voltage Balancing

A third solution simply directly switches the submodule tied to the carrier waveform in question without utilizing a voltage balancing algorithm. While this

simplifies the computational requirement, there is no control on the capacitor voltages and this leads to unstable capacitor voltages which reduces the efficiency of the converter.

2.2.4 Novel Approach to Voltage Balancing

A clear drawback to the voltage balancing algorithms discussed above is that there are a large number of measurements that need to be taken and inputs and outputs that need to be processed. This causes an increase in the difficulty of the physical design aspects along with the embedded control solutions required for such a large system. This complication further increases for modular multilevel converters that require a large number of submodules. This may also limit the effectiveness of the above described voltage balancing algorithms because they would require a large number of device switching state transitions. Thus, without a large bandwidth, these voltage balancing algorithms may not be able to operate properly. There are alternative voltage balancing methods that have been implemented that operate without measuring the capacitor voltages. This is discussed in [10].Instead, all these voltages are approximated based on a number of factors including arm currents, control references, converter voltages and DC bus voltage. The obvious limitation is there is an increased chance of error due to the required estimations. This approach is not explored in this work for this reason.

Chapter 3

EVALUATION METHOD

The goal of this thesis is to use key metrics in the comparison of the response of a modular multilevel converter under various PWM and voltage balancing implementations. To do this, important metrics need to be identified, explained and implemented into the converter simulation. Typical vital design criteria include: converter power loss, limiting switching frequency and harmonic reduction.

3.1 Evaluation Metrics

3.1.1 Capacitor Voltage Deviation

The analysis of capacitor voltage deviation is straightforward in that the focus is on the voltage ripple of each capacitor voltage. While the voltages of each arm should be fairly close to the same value they're not exactly the same due to this voltage ripple. This leads to an increase in circulating current and other issues. For the purpose of comparison, an average steady state voltage deviation is taken from each capacitor voltage in the model. This average is quickly calculated by running the model to steady state and finding the highest deviation for each submodule from the ideal DC voltage and then taking the average of all the capacitor voltages in the converter. This testing will be done for various load conditions and plotted to compare the various methods. As an

example, Figure 3.1 shows 20 capacitor voltages for a 21-level MMC simulation. The ideal DC voltage is 1kV and shown is a voltage ripple of approximately 10%.

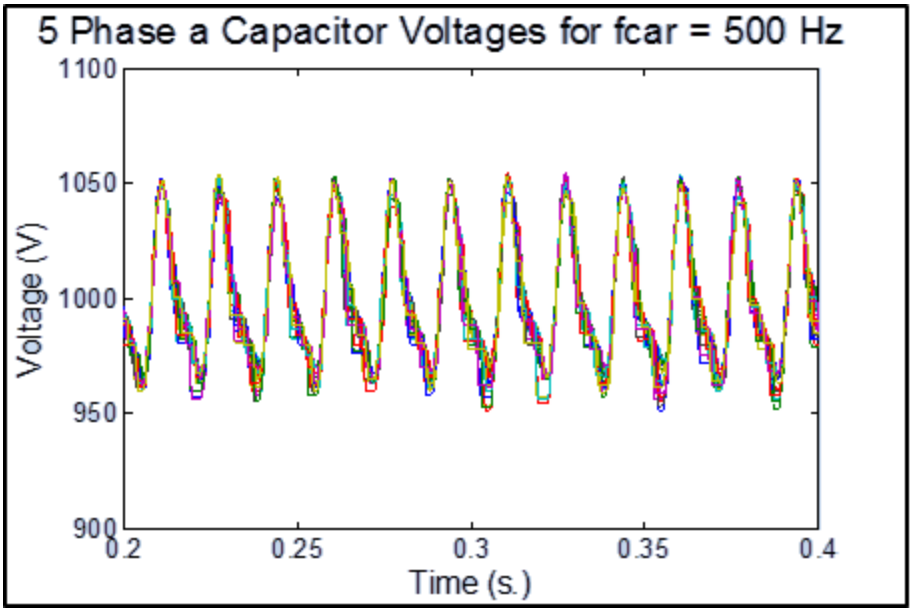

Figure 3.1 Phase a Capacitor Voltages

3.1.2 Converter Power Loss

The power loss of the converter is a key factor in analyzing the overall operation of the converter and the effect of various PWM schemes and voltage balancing algorithms. [11] and [12] discuss loss modeling for voltage source converters. Further fundaments to loss modeling are addressed in [13] and [14]. There are three main components to converter power loss and they are: arm inductor winding loss, semiconductor device conduction loss and switching loss. In this research, these three power loss values will be calculated using the modular multilevel converter model to be discussed later. This analysis requires looking at the different elements of the total power loss in order to fully understand the effects of each control implementation.

3.1.2.1 Semiconductor Device Conduction Loss

Conduction loss is a large component of the total converter loss. Each semiconductor device contributes to the conduction loss whenever they're in an on-state. Equation (10) shows a general equation for conduction power loss.

$$Pcond = Vce_{sat} * Ic, Ic = \text{collector current} \quad (10)$$

Considering the conduction paths discussed in the introduction, every IGBT in the converter is conducting one semiconductor device at all times. Whenever a device is conducting, power loss is dissipated as heat due to the saturation voltage of the device. Most IGBT datasheets give a typical IGBT collector-emitter saturation voltage. This voltage changes with both current and temperature. To simplify this power loss modeling, a junction temperature of 125°C is assumed. A range of saturation voltages can then be implemented based on the current through the device at the time of the calculation. Reference [15] is an example IGBT datasheet which shows figures for saturation voltage versus collector current. This data can be used to provide a general fitting of correct saturation voltage.

Using the knowledge of conduction paths based on current polarity, it can be quickly known how many IGBTs versus how many diodes are conducting in the converter. Then, assuming the same saturation voltage for each IGBT at the specific simulation time step a total converter power loss is calculated. In order to get the most accurate calculation, this conduction power loss is calculated at every simulation time step. A conduction power loss is calculated then divided by the simulation period to get an energy value in Joules. This calculation is then repeated at every simulation time step over one steady state cycle to get a total energy loss. Finally, this energy value is divided

by the time of one cycle, 0.016667 seconds for 60 Hz systems, to get a conduction power loss.

3.1.2.2 Switching Power Loss

Switching loss is the most difficult loss component to accurately calculate in a model of a voltage source converter. [16] describes the various switching transitions for a range of IGBTs. The calculation for switching loss will first be explained followed by how to integrate this calculation into the converter model. Typical switching loss calculations incorporate junction temperature into the calculation. While this provides a more accurate solution, this complicates the calculation so for this work a junction temperature of 125°C will be assumed.

Switching loss occurs during every off or on transition of a semiconductor device. Switching loss can be fundamentally explained as the integral of the voltage times the current during this switching time interval, as shown in equation (11).

$$W = \int_{t1}^{t2} Vce * Ic \, dt \tag{11}$$

Looking at an IGBT's switching loss, which consists of one IGBT and one anti-parallel diode, there are three contributions to the overall switching loss and they are: IGBT Turn-On, IGBT Turn-Off and Diode Turn-Off. The Diode Turn-On transition is known to be minimal compared to the Diode Turn-Off so its contribution can be neglected.

There are several methods for incorporating power loss modeling into a MATLAB/Simulink model. The goal of many loss modeling techniques focuses on the improving the accuracy of the loss calculation. This thesis is more worried about using

loss calculation as a comparison method so while using an accurate loss calculation is important, a finely tuned calculation method is unnecessary. Because of this, a simplified loss modeling technique is desired. Dr. Gole and others have developed a streamlined IGBT loss modeling technique suitable for voltage source converters in [17]. This loss modeling technique develops equations that approximate the voltage and current switching transition waveforms based on certain inputs into the calculation. A flowchart illustrating the loss calculation is shown in Figure 3.2.

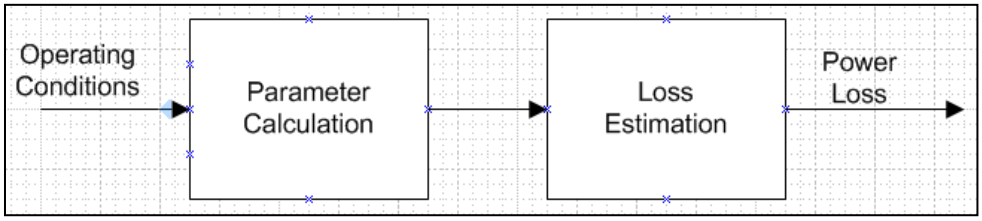

Figure 3.2 Switching Loss Calculation Flowchart

These equations were specifically chosen to reduce the calculation burden on the model and to utilize parameters that can either be found or calculated from the datasheet of the device in question. The operating condition inputs to this loss calculation are the pre-switching and post-switching voltage and current values along with datasheet parameters such as: rise time, fall time, reverse recovery time, IGBT saturation voltage, reverse recovery current and parasitic inductance.

The first step is to utilize MATLAB to verify that the time domain equations given in the reference correctly replicate these switching transitions. In [17], time domain equations for various time periods during the switching transition for voltage and current are given along with coefficients that are easily calculated from the inputs to this loss model. To validate this approach, these time domain equations were plotted using the IGBT IRG4PC40KD to ensure proper switching transition waveforms.

Figure 3.3 shows the Turn-On transition plotted using the given time domain equations and calculated coefficients and

Figure 3.4 shows the reference results for the Turn-On IGBT transition using the same IGBT. This shows the equal time domain plots and validates the derived switching equations.

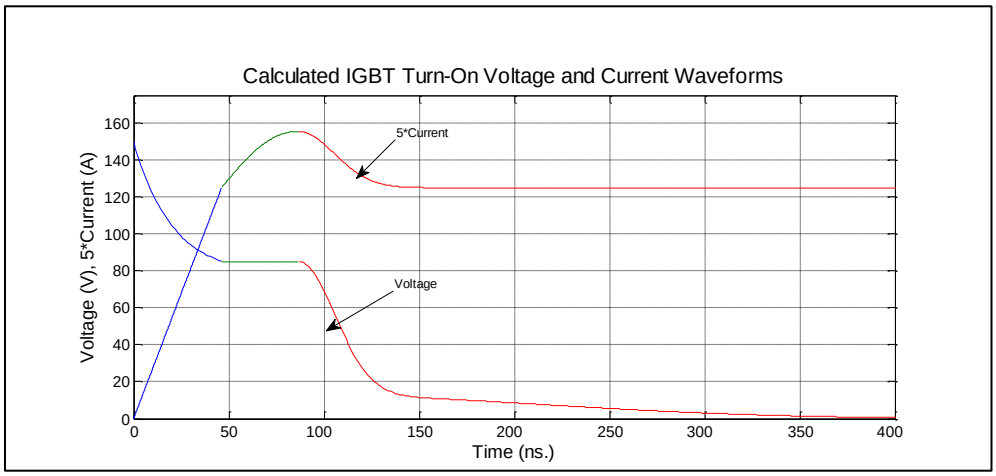

Figure 3.3 Simulated IGBT Turn-On Transition

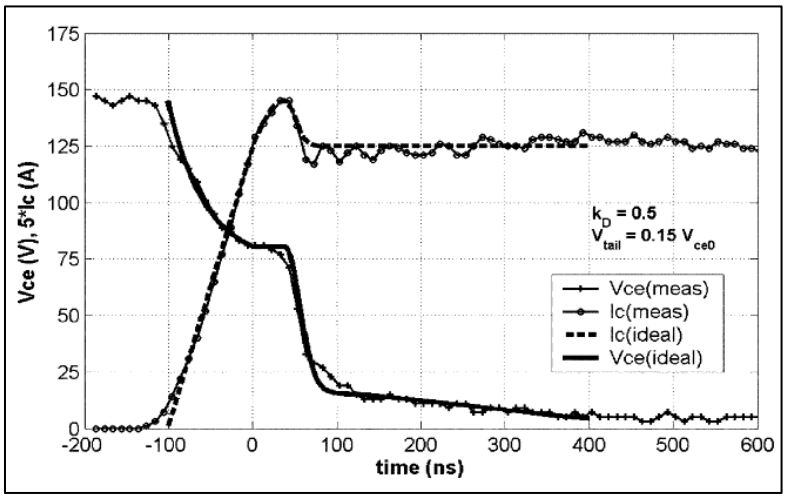

Figure 3.4 Reference Turn-On Transition

Figure 3.5 shows the simulation time domain waveforms for the IGBT Turn-Off transition and Figure 3.6 shows the equivalent reference waveform. Again, the figures match well enough to validate the designed equations.

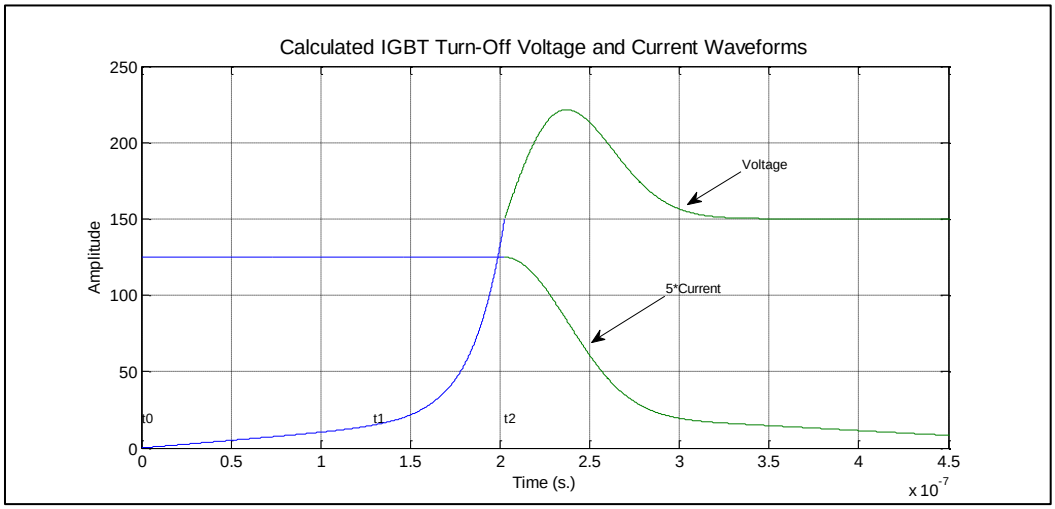

Figure 3.5 Simulated IGBT Turn-Off Transition

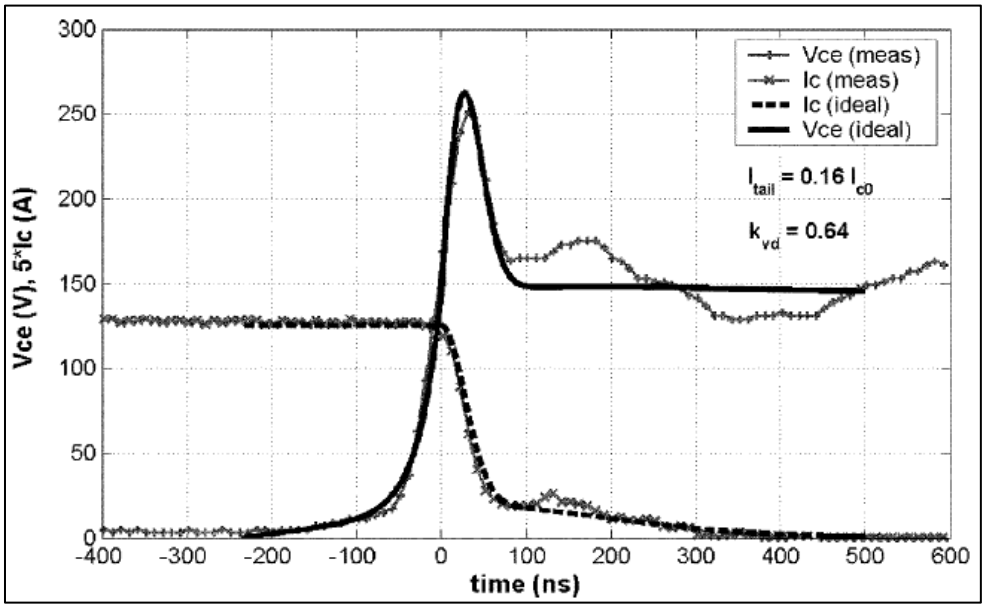

Figure 3.6 Reference IGBT Turn-Off Transition

Here we can see that the equations accurately model voltage and current during a switching transition.

The IGBT Turn-On switching transition can be analyzed in three time intervals. The first time interval is the rise time which is simply the time it takes for the collector current to increase from 10% to 90% of the steady state current value. The second time interval considers the time period where the current reaches a maximum peak value before settling down to within 10% of the steady state current value. This peak value is controlled by the parasitic inductance of the IGBT. [18] further explains the elements of parasitic inductance in an IGBT and that it is a difficult parameter to achieve a precise value. The third and final time interval is essentially the tail time and it is the time it takes for the voltage to reach the saturation voltage.

The IGBT Turn-Off switching transition is analyzed using two time intervals. The first interval is the time it takes for the voltage to go from 10% of collector-emitter voltage to the steady state value. The second interval is again the tail off time which is the time it takes for the current to reach zero.

The diode Turn-Off transition is divided into three time intervals. The first interval is the time it takes for the diode current to reach zero. The next two time intervals are portions of the diode reverse recovery time. A typical value for the reverse recovery time is given in the datasheet for a specific test case along with a graph showing the change in reverse recovery time versus collector current. A coefficient is used to divide the reverse recovery time with a typical value being 0.4 to 0.6 depending on the specific response of the diode. In general, this results in these two intervals lasting roughly half the reverse recovery time.

As previously discussed, the energy loss of a switching transition is the integral of the voltage times the current during this time period as shown in Equation (11). A key criteria of Dr. Gole's loss model is to reduce the calculation complexity thereby reducing the overall simulation time. Solving integrals real time in a simulation of a modular multilevel converter would drastically slow down the simulation itself making it impractical for analysis purposes. For this reason, these definite integrals need to be approximated. These integrals are solved in order to provide the easiest but accurate calculation. These solutions need to also be validated and [17] includes calculated values for Turn-On and Turn-Off IGBT energy loss given a specific voltage and current value. Using the same IGBT parameters for the graphical verification, the IGBT Turn-On and Turn-Off energy loss for various voltage and current values are given in the reference. The equations in the reference are then implemented into a MATLAB function and the resulting energy values are compared to the reference results. Table 3.1 shows the experimental calculated values and Table 3.2 shows the reference's calculated energy values for a range of voltages and currents. Ideally, the implemented MATLAB functions would match these values within a small error window and we can see that the energy values match within a 10-15% error. These calculations assumed the IGBT IRG4PC40KD whose datasheet is shown in [19].

Table 3.1 Implemented equations calculated using MATLAB function.

Vce0	Ic0	Won (mJ)	Woff (mJ)
150	15	0.2161	0.2327
150	20	0.319	0.31
150	25	0.41076	0.3883
120	15	0.1735	0.151
120	20	0.2503	0.2218
120	25	0.3279	0.3126

Table 3.2 Reference [17] Calculated Energy Value

TABLE I
COMPARISON OF MEASURED AND CALCULATED POWER LOSSES FOR IRG4PC40KD IGBT

V_{ce0} (V)	I_{c0} (A)	W_{on} (mJ)		Error (%)	W_{off} (mJ)		Error (%)
		Meas	Cal		Meas	Cal	
150	15	0.193	0.216	11.9	0.183	0.203	10.9
150	20	0.274	0.312	13.9	0.289	0.318	10.0
150	25	0.353	0.417	18.1	0.394	0.478	21.3
120	15	0.155	0.173	11.6	0.112	0.125	11.6
120	20	0.221	0.242	9.5	0.183	0.205	12.0
120	25	0.310	0.325	4.8	0.289	0.321	11.1

There are options available to reduce this calculation error. Many parameters vary with collector current and this data is given in graphs and figures in the device datasheet. In order to improve the calculation accuracy, many parameters are updated each calculation cycle depending on the collector current at that specific point in time.

3.1.3 Harmonics

A main benefit of the modular multilevel converter topology is that the design inherently reduces harmonics. This eliminates the requirement for an AC filter and expands the potential applications of this converter type. The harmonics that do arise are low in magnitude and centered around the switching frequency. This is therefore an important metric in this work. For the modulation methods and voltage balancing algorithms in question, the converter voltage THD will be calculated. Also, the fast fourier transform will be done to help visualize the harmonic elimination of modular multilevel converters compared to a conventional voltage source converter and compared using the various methods in question. This will visually validate any improvements in the converter voltage THD.

3.1.4 Circulating Current

Circulating current is the current that flows between one phase leg and another and the current that flows between each phase leg and the DC bus. Reference [20] explains that this circulating current is caused by differences in the voltage between each phase. Circulating current in a modular multilevel converter is a negative sequence current with a frequency twice the fundamental along with a DC component that is either positive or negative depending on the direction of power flow. Circulating current directly effects the overall efficiency because it increases the rms value of the arm current which results in increased power loss. If the circulating current can be limited this not only improves converter operation but reduces the arm inductor requirements.

3.1.4.1 Circulating Current Suppression Controller

The main reference used, [4], develops a circulating current suppression controller to help minimize this circulating current. This controller first converts these three phase circulating currents to the dq reference frame remembering that this is a negative-sequence, double fundamental frequency rotating frame. Once these currents are convertered to the dq reference frame, a reference of zero into two PI controllers is used to limit the circulating current. The resultant dq reference values are then achieved after cross coupling compensation and then converted back to the acb reference frame. These reference waveforms are then added to the reference waveforms that are routed to the modulation schemes. Figure 3.7 shows a block diagram of the circulating current suppression controller.

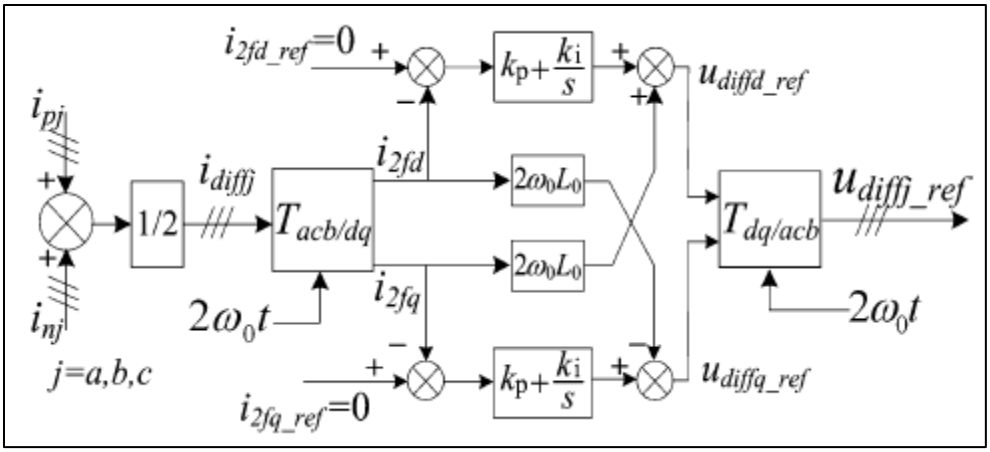

Figure 3.7 Circulating Current Suppression Controller Block Diagram [4]

3.2 Simulation Design

3.2.1 MMC Simulation Model Description

In order to complete this work, a modular multilevel converter model needed to be developed. The software MATLAB/Simulink including SimPowerSystems is used to build this model. The first step was to design the control loops in order to build an average model of a modular multilevel converter. These control loops are designed as done in the introduction. As discussed in [8], a modular multilevel converter can be modeled as shown below. Each arm of the converter can be modeled as a controlled AC voltage source with a DC voltage source supplying the DC bus. The input to these controlled AC voltage sources is simply the reference waveform generated by the control. This model matches our eventual three phase MMC model with these AC voltages being in place of the arm voltages and is used to verify the inner current controllers and outer power controllers. Ideally, this implemented control scheme should be able to be directly applied to the real modular multilevel converter model.

Figure 3.8 shows the average MMC MATLAB model. Shown is the three phase AC voltage source and the DC bus along with three phase units of the modular multilevel converter and the PI controllers. Figure 3.9 shows one phase leg of the average model and shows that the arm voltages are modeled using an AC controlled voltage source. Also shown is the arm impedance used to limit circulating current.

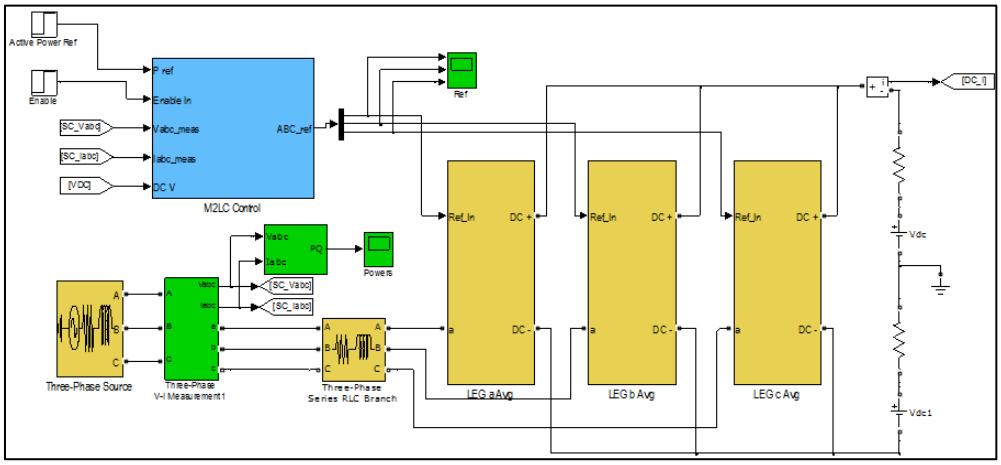

Figure 3.8 MMC Average Model

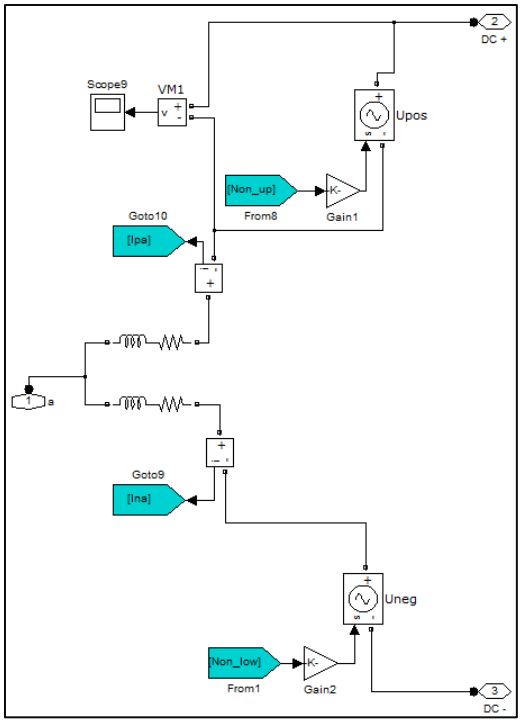

Figure 3.9 MMC Average Model Phase Unit

Once the model is built, the converter was tested using an active and reactive power step change to verify the steady state response of the converter at two different power levels along with its transient response at the step change. Results will be shown using the average model of a modular multilevel converter then a similar test will be done using the real model. If the results show proper power reversal and converter operation, then both the model implementation and the PI controllers will have been validated. For the average model test, the active power reference is changed from 10 MW to -5 MW while the reactive power reference is held at zero. Figure 3.10 shows the active and reactive power measurement for the average model showing proper step response with low overshoot and steady state error. Figure 3.11 shows the three phase currents and we can see proper current waveforms at two different power levels along with the converter

step response. Figure 3.12 shows the phase a AC voltage and current. The key note here is that after the step change we should see a change in the direction of active power flow. This is verified by ensuring that the current is 180 degrees out of phase of the voltage for a negative active power reference.

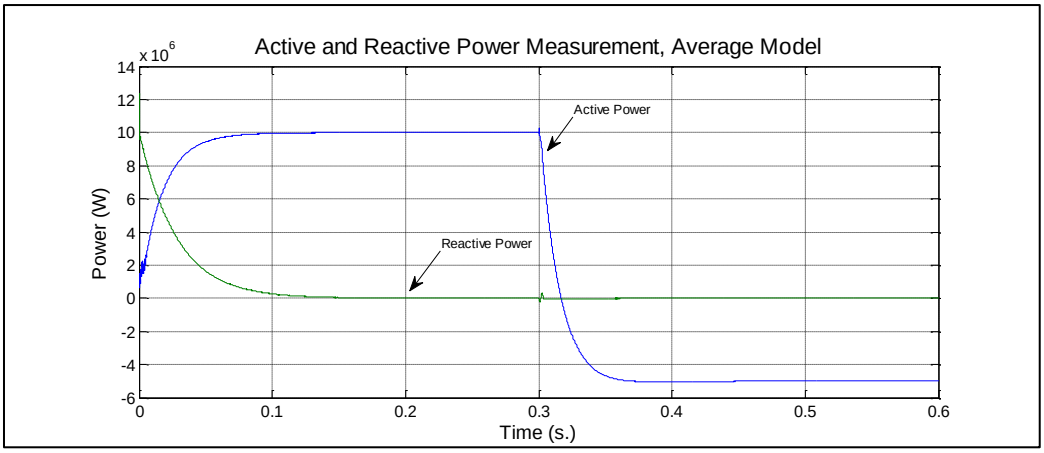

Figure 3.10 Power Reversal, Average Model

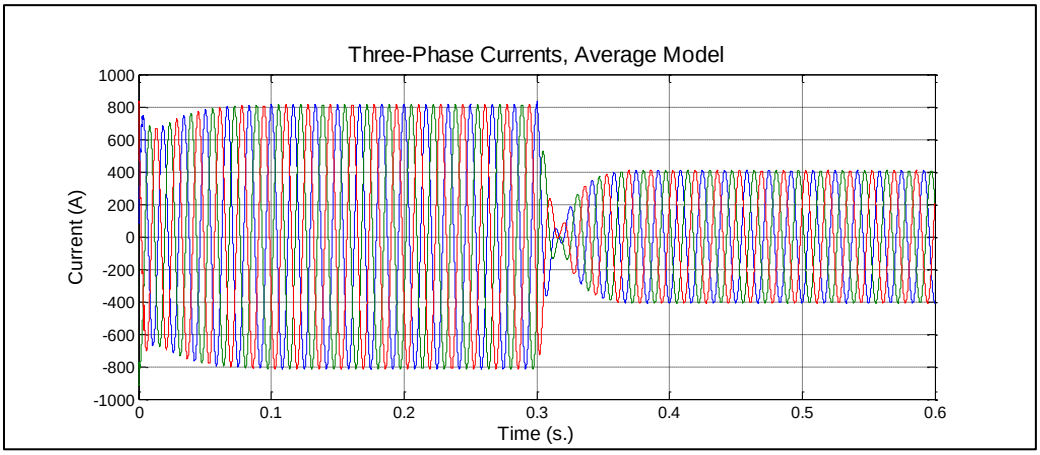

Figure 3.11 Three-Phase Currents under a Power Reversal

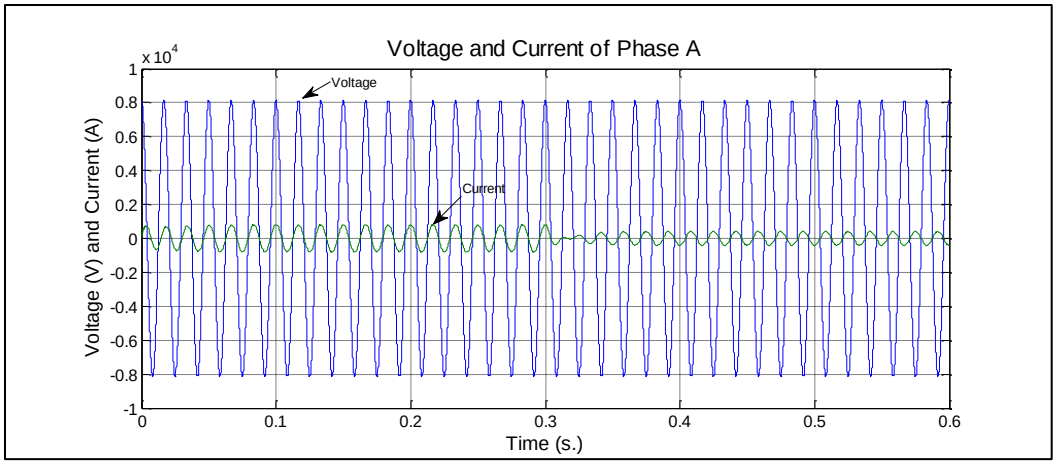

Figure 3.12 Phase a Voltage and Current, Average Model

Next a model is built with the actual implementation of the modular multilevel converter. Figure 3.13 shows a submodule in Simulink which utilizes two IGBTs in series with a capacitor across the devices. Next, Figure 3.14 shows one converter arm implemented with 20 submodules. Also shown is the routing of the gate signals to and the capacitor voltages from the submodules. Finally, Figure 3.15 shows the full three phase, 21-level modular multilevel converter including AC grid connection, DC Bus connection, the converter and the control.

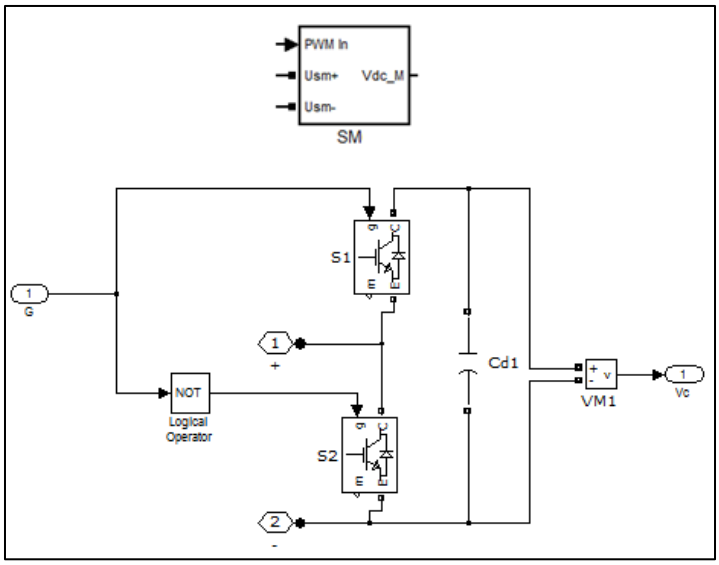

Figure 3.13 Submodule

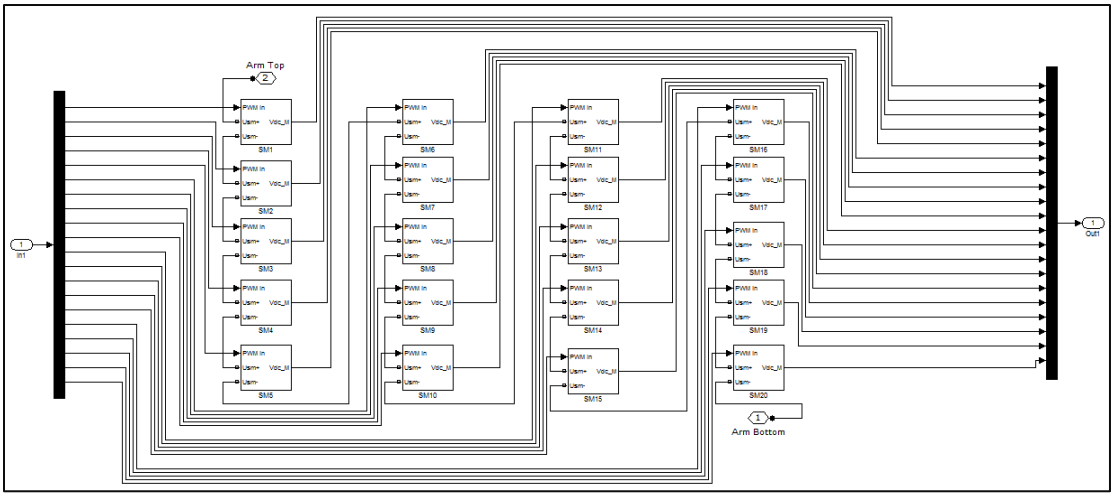

Figure 3.14 Converter Arm, Real Model

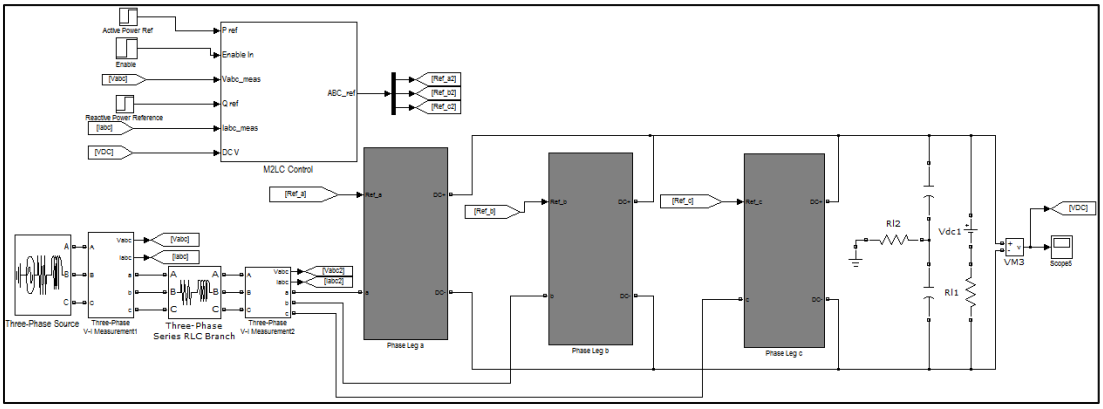

Figure 3.15 MMC Model

In this model, the values for the passive components are the same as the values used in [4] and this allows us to compare the various voltages, current and controller elements to the reference's converter implementation in order to verify proper model design. Next, the reference results and the MATLAB real MMC model will be shown and compared. For this comparison, the same modulation and voltage balancing methods will be used and later these will be changed to analyze result differences. Figure 3.16 shows the source results of 20 capacitor voltages from the upper arm of phase a and Figure 3.17 shows the same voltages using the real MMC model.

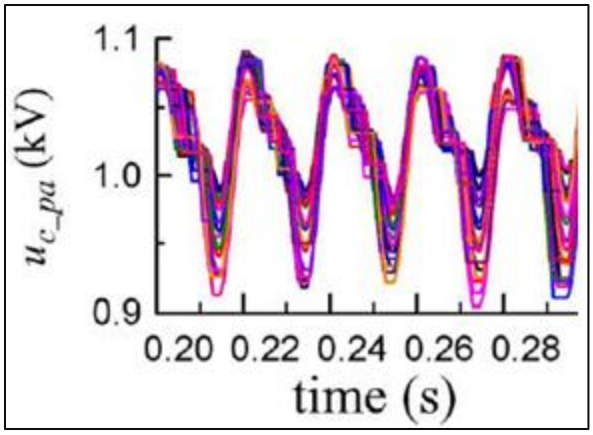

Figure 3.16 20 Capacitor Voltages, Reference Model [4]

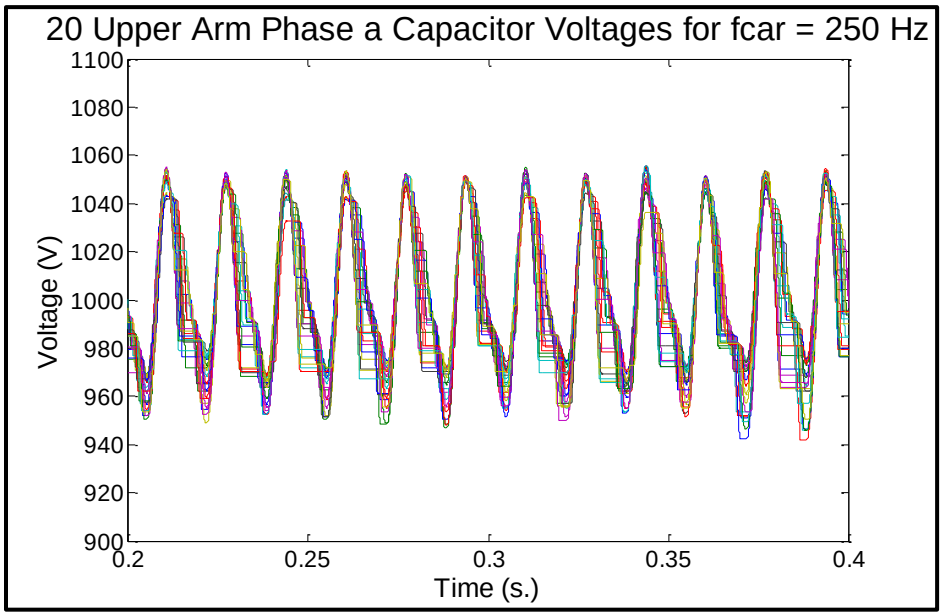

Figure 3.17 20 Capacitor Voltages, Matlab Model

Figure 3.18 shows the upper arm current of phase a and shown is a sinusoidal current with a distortion at the lower peak. This is caused by the circulating current and implementing the CCSC controller would mitigate this distortion. Figure 3.19 shows the same current in the model and we can again see the distortion caused by the circulating current.

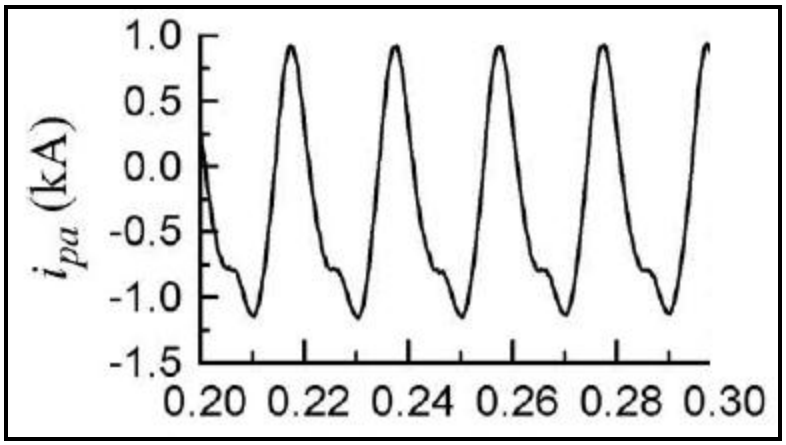

Figure 3.18 Phase a Upper Arm Current, Reference Model

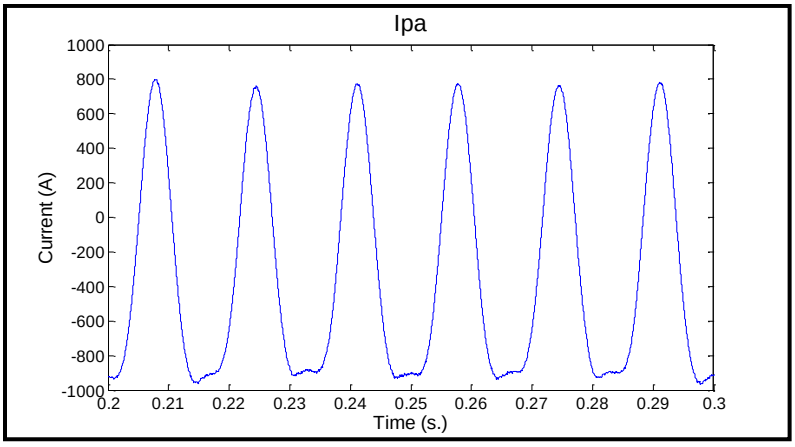

Figure 3.19 Phase a Upper Arm Current, Matlab Model

Figure 3.20 and Figure 3.21 shows the phase a circulating current for the source and MATLAB model respectively. Shown is both the DC component along with the double line frequency AC component. Figure 3.22 and Figure 3.23 show the same results for three phase currents under a step change. This result illustrates a proper transient response.

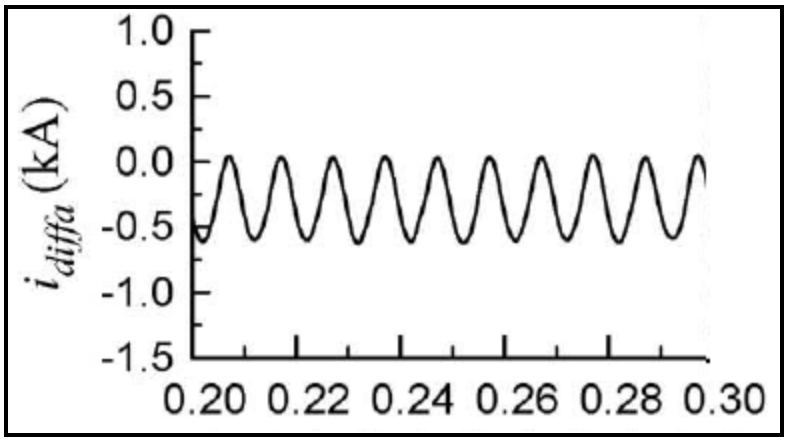

Figure 3.20 Phase a Circulating Current, Reference Model

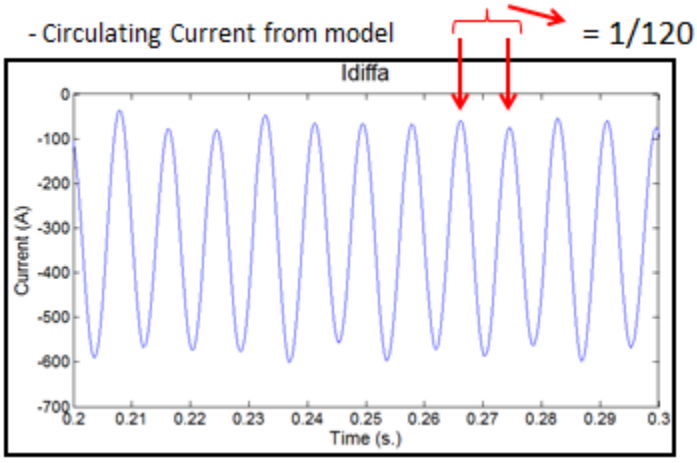

Figure 3.21 Phase a Circulating Current, Matlab Model

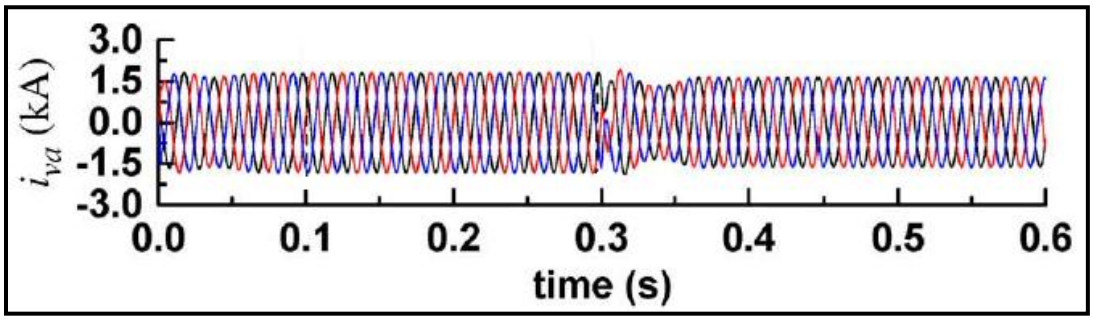

Figure 3.22 Three Phase Currents, Reference Model

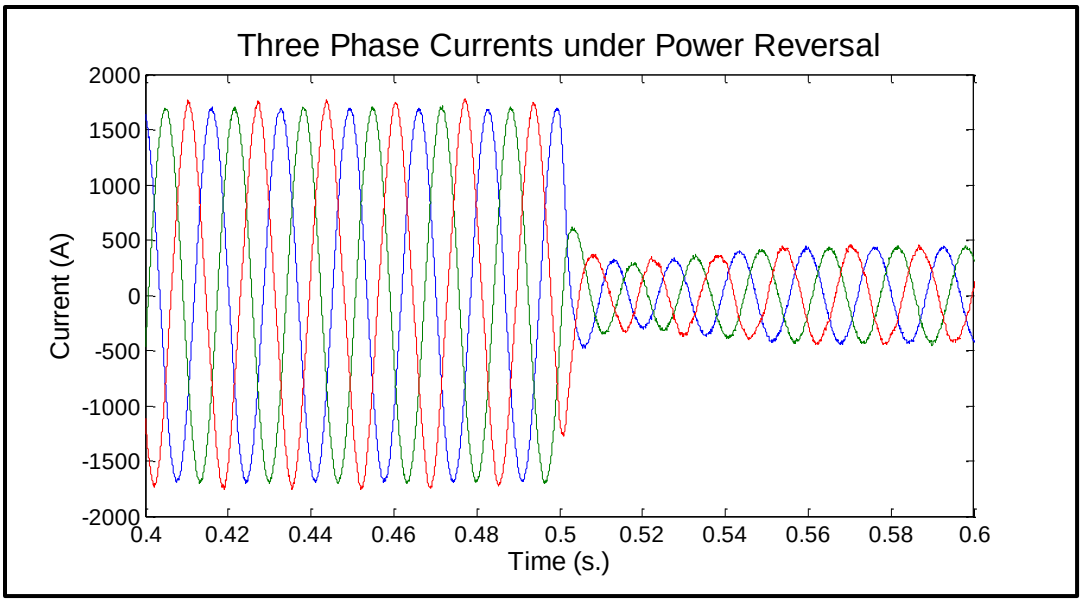

Figure 3.23 Three Phase Currents, Matlab Model

Shown below is the three phase converter voltages in Figure 3.24 and Figure 3.25. While Figure 3.24 is a zoomed out image of the converter voltages, they do in fact show the staircase shape we expect as discussed in the introduction. This is more clearly shown in the MATLAB model converter voltages.

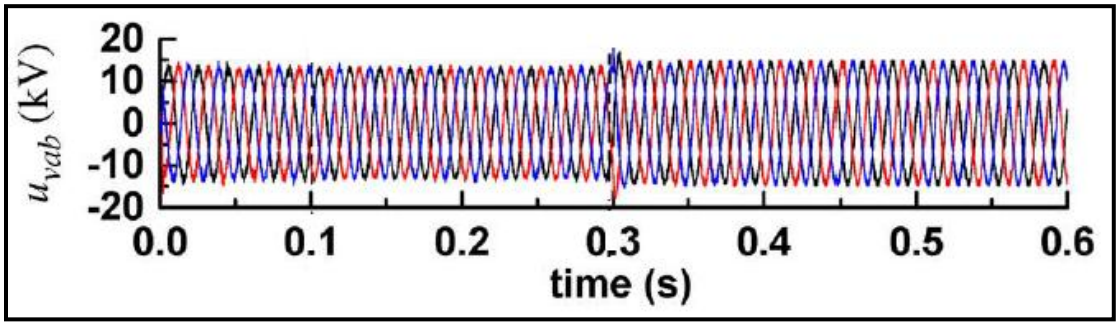

Figure 3.24 Three Phase Voltages, Reference Model

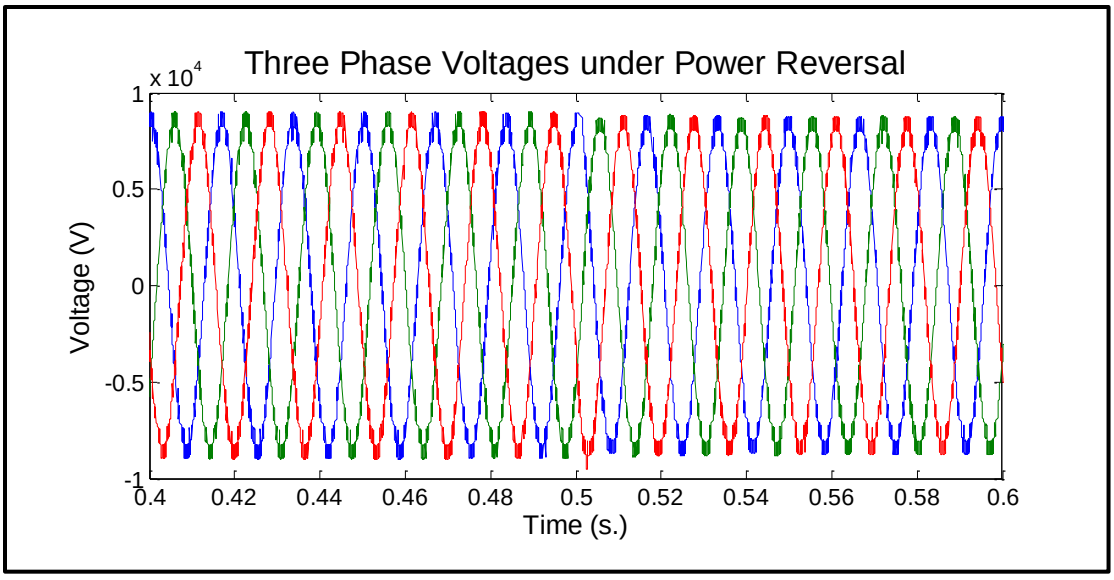

Figure 3.25 Three Phase Voltages, Matlab Model

Finally, Figure 3.26 and Figure 3.27 show the measured active and reactive power under a step change. The source measurements are in p.u. while the model measurements are in units of MW or MVar. Since the PI controllers were tuned considering a 20MW active power reference, the reference value for this model result was changed to step from 20MW to -5MW this showed the best step response for this comparison.

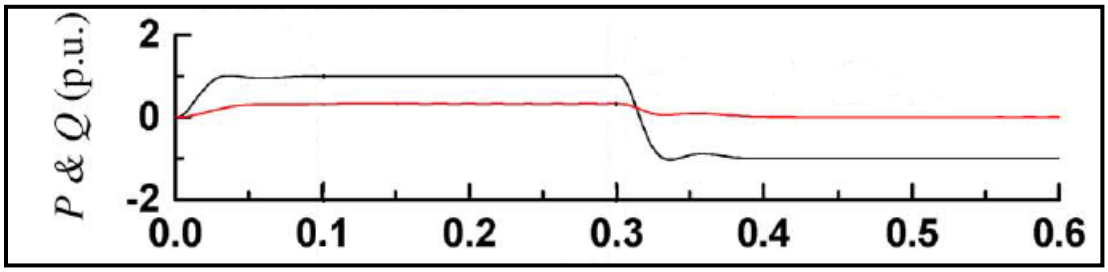

Figure 3.26 Active and Reactive Power under Step Change, Reference Model

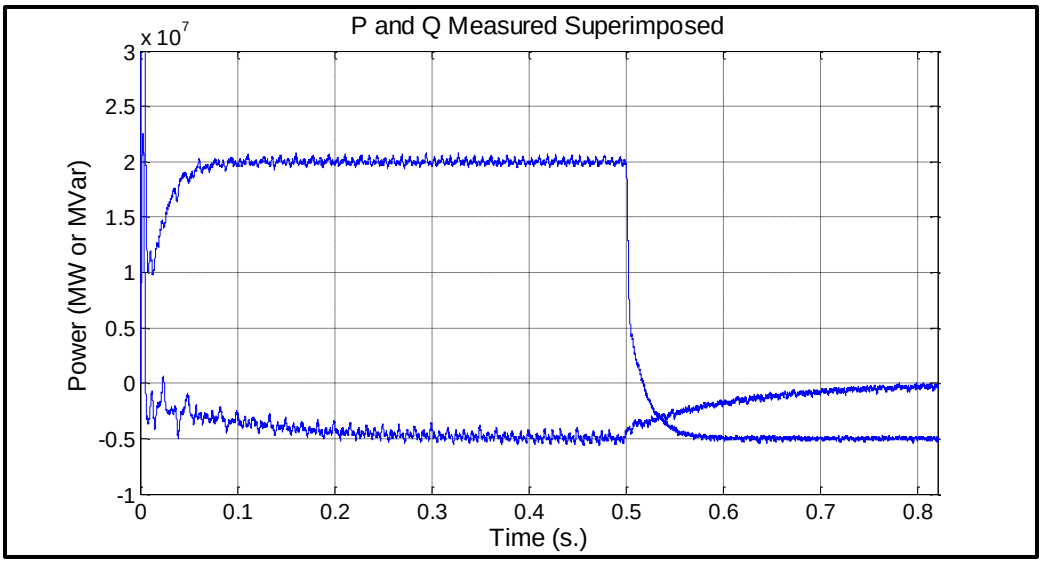

Figure 3.27 Active and Reactive Power under Step Change, Matlab Model

Looking at these results, the developed MATLAB MMC model shows proper transient response including power reversal and validates the developed model.

3.2.2 Modulation and Balancing Implementation

While the PI controllers are intuitively added to the model, careful considerations need to be made for the modulation methods and balancing algorithms discussed. To implement the PSC-PWM modulation technique, a carrier was used with fc used as an input to directly set the carrier frequency as shown in Figure 3.28. Several transport delay blocks were then used to generate the appropriate phase shift between each carrier. The level shifted techniques were implemented as shown in Figure 3.30. The carrier waveform which is normalized to a peak to peak value of 1 is scaled by the number of submodules, in this case 20 and the appropriate DC biases are applied. In the level-shifted methods that require carriers out of phase, another waveform block is simply used with the phase flipped.

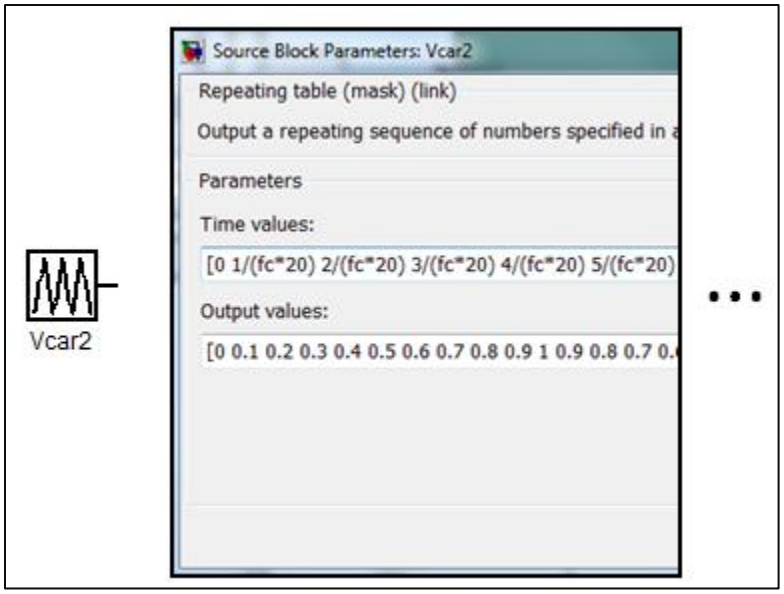

Figure 3.28 Carrier Waveform with fcar Input

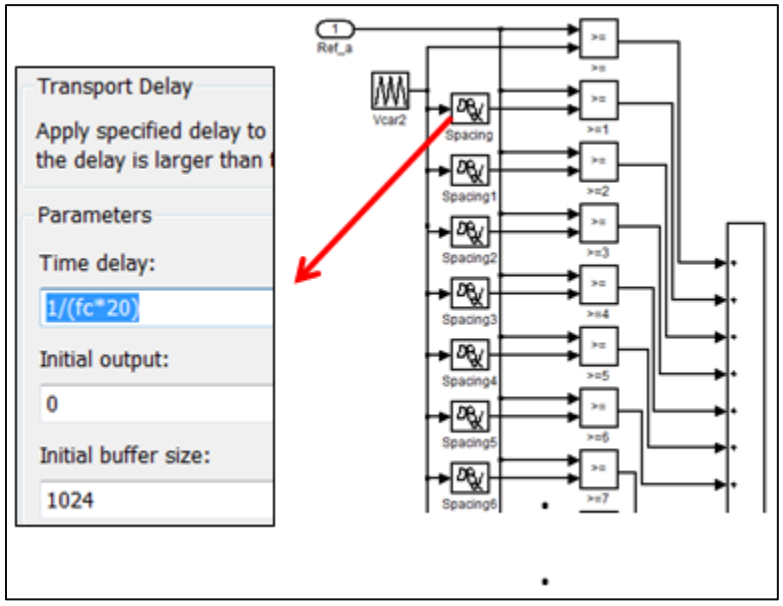

Figure 3.29 Transport Delay used to set phase shift

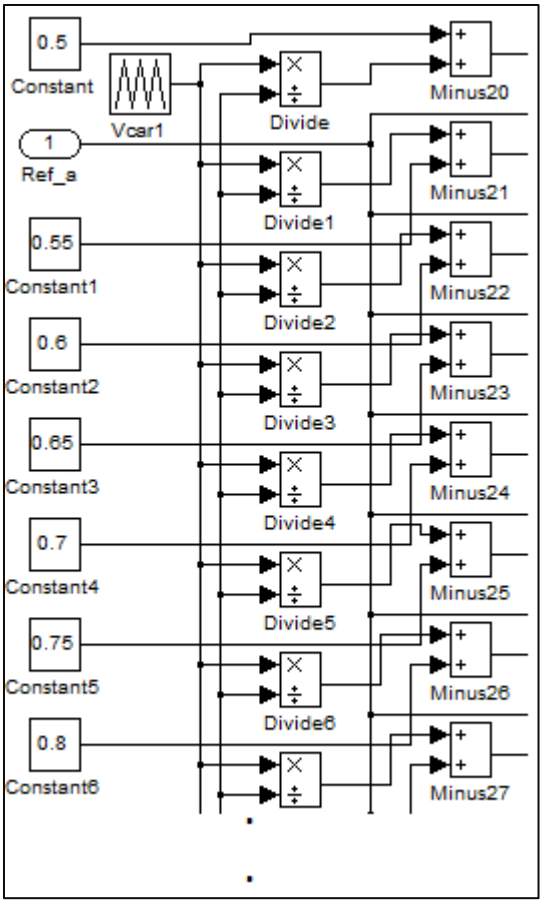

Figure 3.30 Level-shifted PWM Implementation

To implement the voltage balancing algorithms, various types of MATLAB functions are used. These algorithms were first written in a MATLAB Level-2 S-Function. Later, both the conventional voltage balancing algorithm and the reduced switching frequency algorithm were implemented in an updated model version using a Level-1 MATLAB function block. Both of these functions take in all the capacitor voltages along with the reference waveforms and arm currents as inputs and routes the appropriate gate signals to each submodule. A MATLAB function block is used for each phase of the converter.

Chapter 4

SIMULATION RESULTS

4.1 Capacitor Voltage Deviation

This test focused on calculating the maximum steady-state capacitor voltage deviation for each modulation technique. A minimal capacitor voltage ripple is essential to both converter functionality and reducing power loss. One aspect of the converter that affects this voltage ripple is the modulation methods and voltage balancing algorithms. Both of these will be varied and the voltage deviation results will be analyzed and compared.

4.1.1 Reduced-Switching Frequency Voltage Balancing Algorithm

The first test focuses on calculating the maximum steady-state voltage deviation for each modulation technique and over a range of frequencies. For this test case, the voltage balancing algorithm will remain constant, the same reduced switching frequency method discussed previously, and the carrier frequency and PWM method will be the variables in the model. Figure 4.1 shows the average maximum capacitor voltage deviation for phase-shifted carrier PWM modulation technique over a range of switching frequencies. This data was gathered for both a maximum and half load condition, P = 20MW and P = 10MW, and both are shown in Figure 4.1. Note that this is not a peak to peak ripple but instead average maximum voltage amplitude. Considering that the ideal

capacitor voltage in the model being used is 1kV, a typical maximum voltage ripple of 10% leads to acceptable maximum voltage amplitude of roughly 50V.

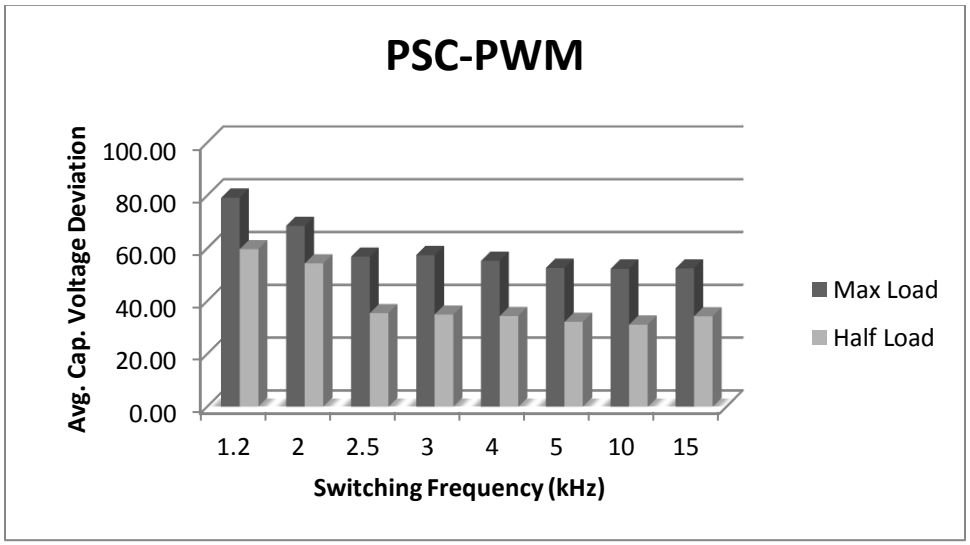

Figure 4.1 PSC-PWM Avg. Capacitor Voltage Deviation vs. Switching Frequency

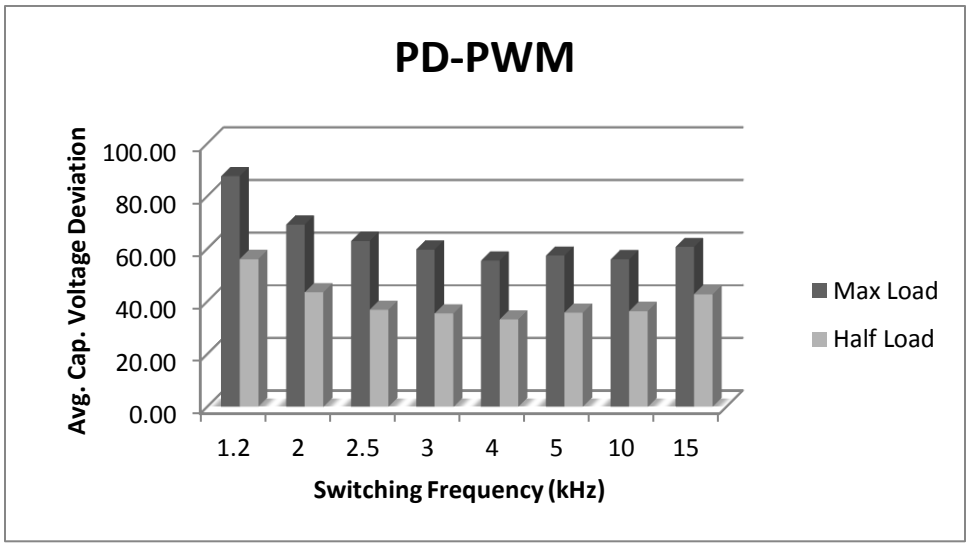

Figure 4.2 PD-PWM Avg. Capacitor Voltage Deviation vs. Switching Frequency

Figure 4.2 shows the same test results for phase-disposition PWM and a similar result is shown. Figure 4.3 and Figure 4.4 shows the same results for the other two level-shifted modulation techniques.

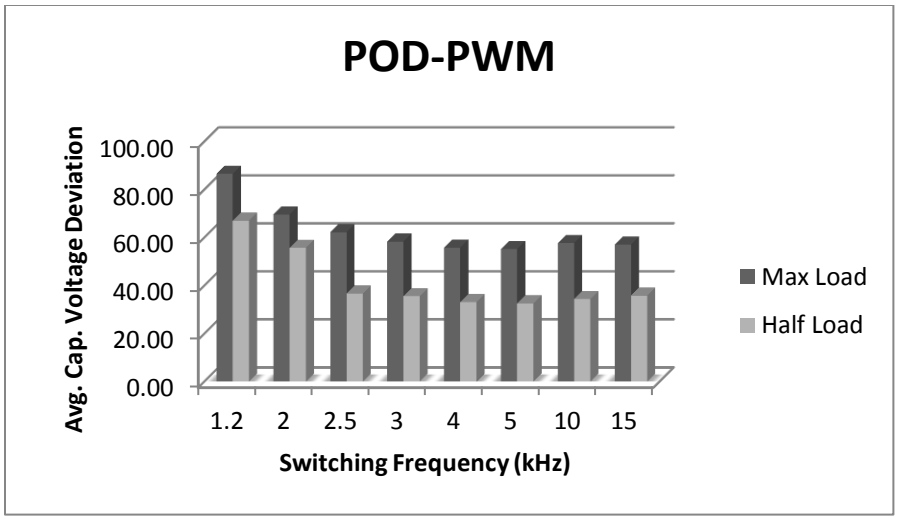

Figure 4.3 POD-PWM Avg. Capacitor Voltage Deviation vs. Switching Frequency

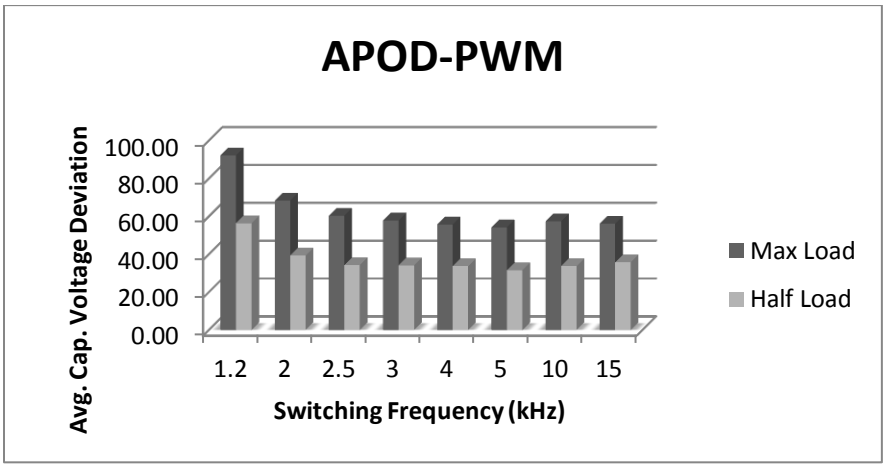

Figure 4.4 APOD-PWM Avg. Capacitor Voltage Deviation vs. Switching Frequency

A key interest in this work is how much the switching frequency can be lowered and if that has any adverse effects on other aspects of the converter.

The next step is to zoom into this data and make comparisons of the different methods at the same switching frequency. Figure 4.5 shows the voltage deviation for each modulation method at a switching frequency of 1.2 kHz. At this switching frequency, a noticeable benefit to PSC-PWM is shown for the higher power levels and appears that as the power level decreases, the difference between each method decreases.

Figure 4.6 shows the same results for a switching frequency of 2.5 kHz and here we can see the benefit of the phase-shifted modulation method has decreased although there is a still noticeable improvement.

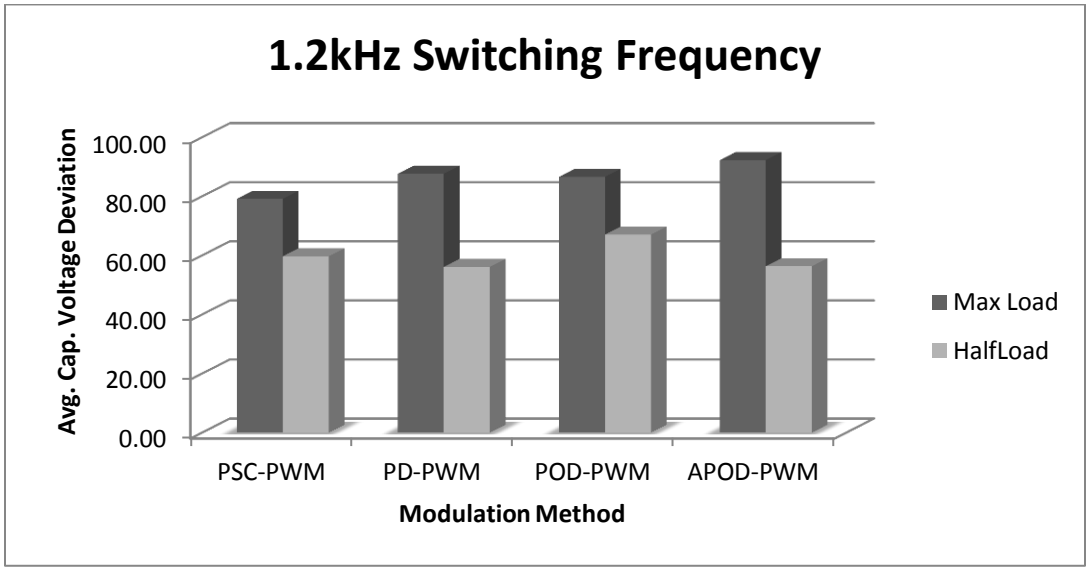

Figure 4.5 Voltage Deviation Comparison, 1.2 kHz

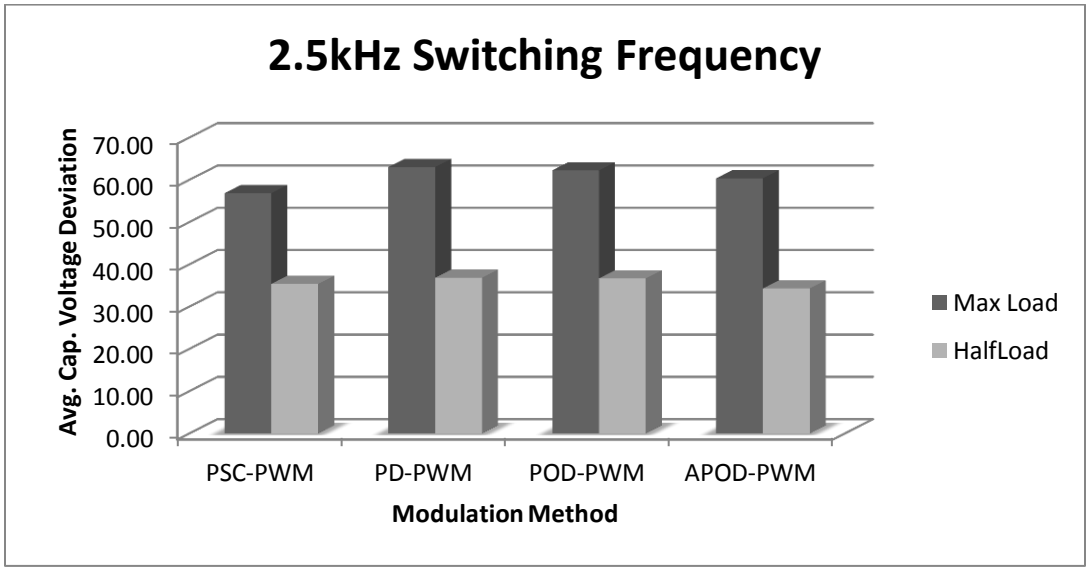

Figure 4.6 Voltage Deviation Comparison, 2.5 kHz

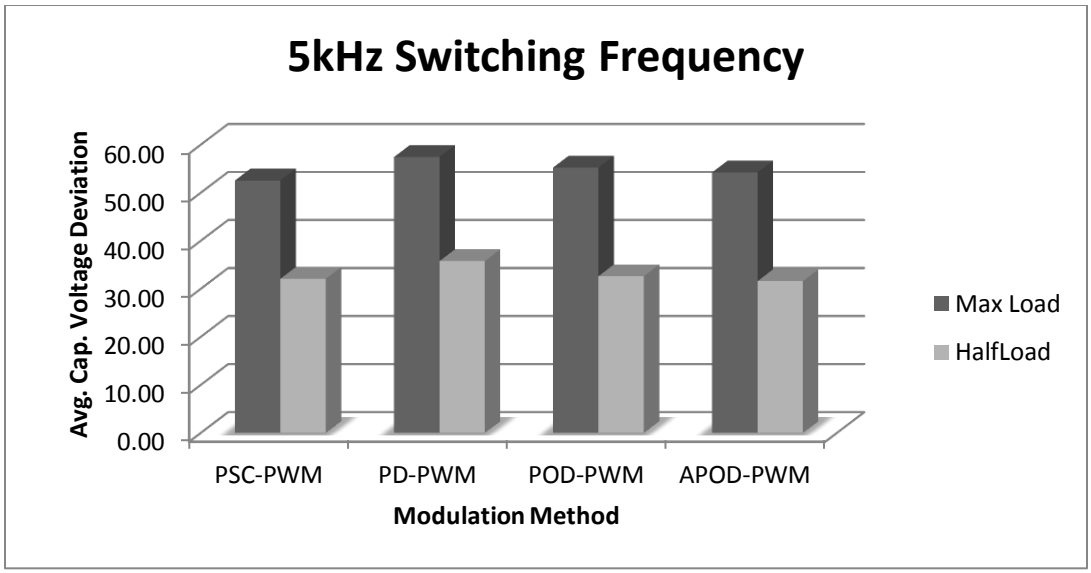

Figure 4.7 Voltage Deviation Results, 5 kHz

Figure 4.7 shows the results for a switching frequency of 5 kHz and here again see a benefit in the phase-shifted PWM method particularly for the maximum power condition. This appears to show that phase-shifted pulse width modulation has a voltage deviation benefit at lower switching frequency and at higher switching frequencies there is still voltage deviation benefit but isn't as substantial for switching frequencies above 5 kHz. This method only addresses 1 voltage balancing algorithm so this result needs to also be analyzed for the other voltage balancing options.

4.1.2 Conventional Voltage Balancing Algorithm

This testing continues for the other voltage balancing algorithm with the premise that a noticeable benefit of the phase-shifted technique will be shown. Figure 4.8 shows the voltage deviation results for phase-shifted PWM using the conventional voltage balancing algorithm and here we can already see that this algorithm shows a better capacitor voltage ripple compared to the previous section.

Figure 4.9 shows the same results for phase-disposition PWM and again a similar result is shown that the voltage ripple is reduced over a larger range of switching frequencies. This is explained by remembering that this algorithm is developed to result in the best possible capacitor voltage balancing. Figure 4.10 and Figure 4.11 show the same data for the remaining PWM options and reflect similar results.

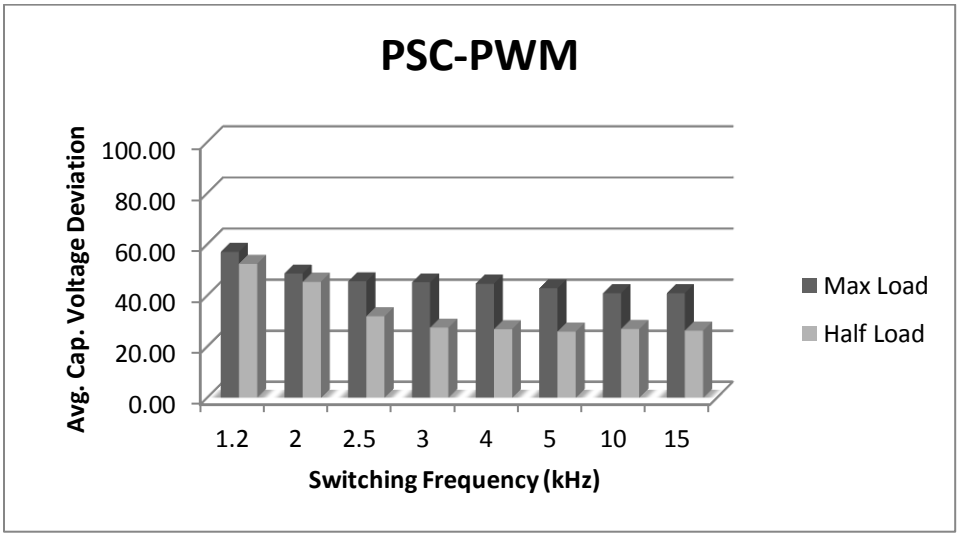

Figure 4.8 PSC-PWM Capacitor Voltage Ripple

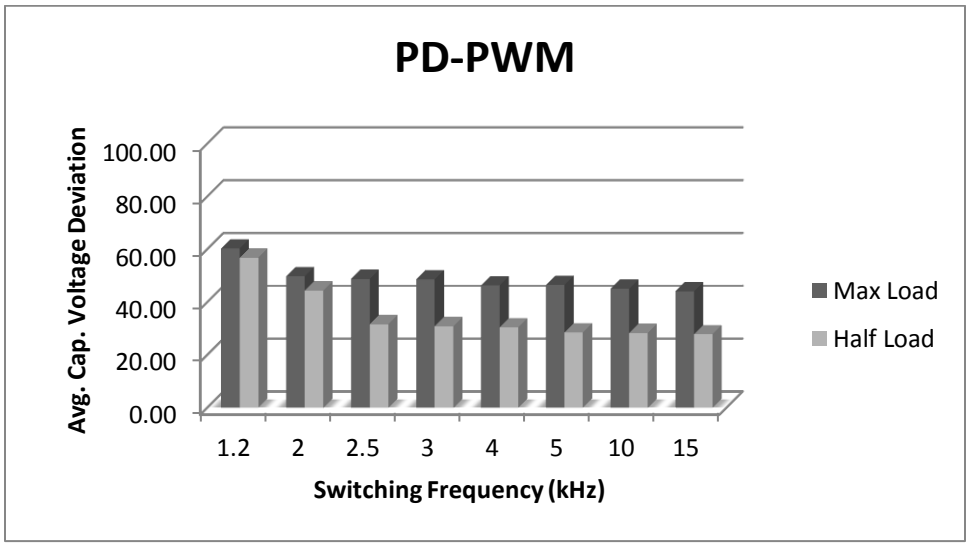

Figure 4.9 PD-PWM Capacitor Voltage Ripple

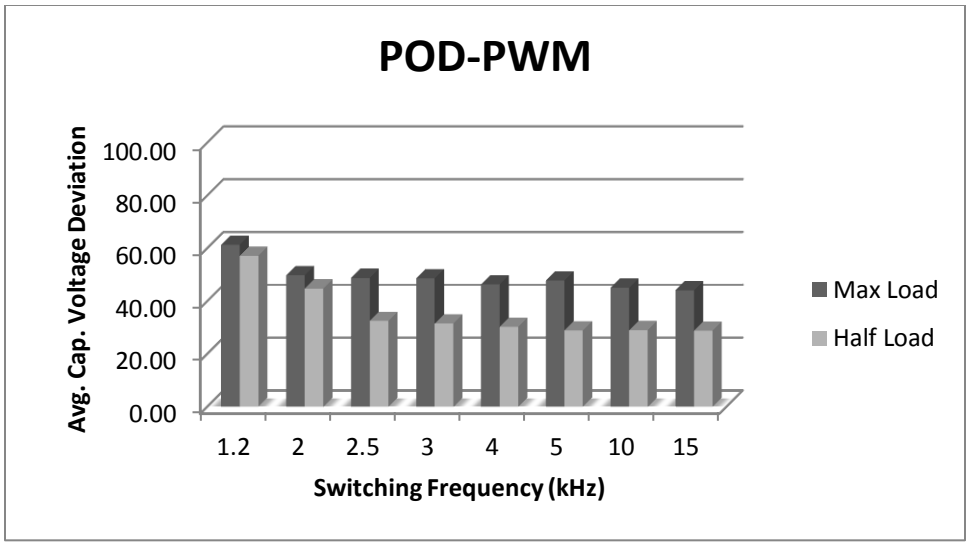

Figure 4.10 POD-PWM Capacitor Voltage Ripple

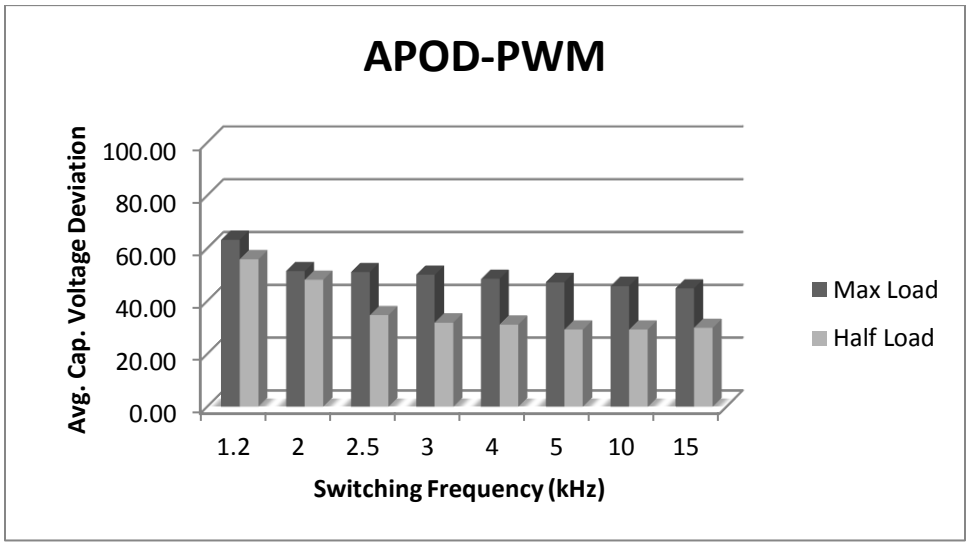

Figure 4.11 APOD-PWM Capacitor Voltage Ripple

Next a comparison will be shown at specific switching frequencies to better show the benefit of each modulation technique. Figure 4.12 shows for each pulse width modulation technique at 1.2 kHz switching frequency the voltage deviation results. For both a maximum and half load condition, the level-shifted technique shows better performance. Figure 4.13 and Figure 4.14 showed the same result at 2.5 and 5 kHz. Again, for all the methods the voltage ripple has improved compared to the reduced

switching frequency balancing methods and the level-shifted carrier shows the best capacitor voltage balancing.

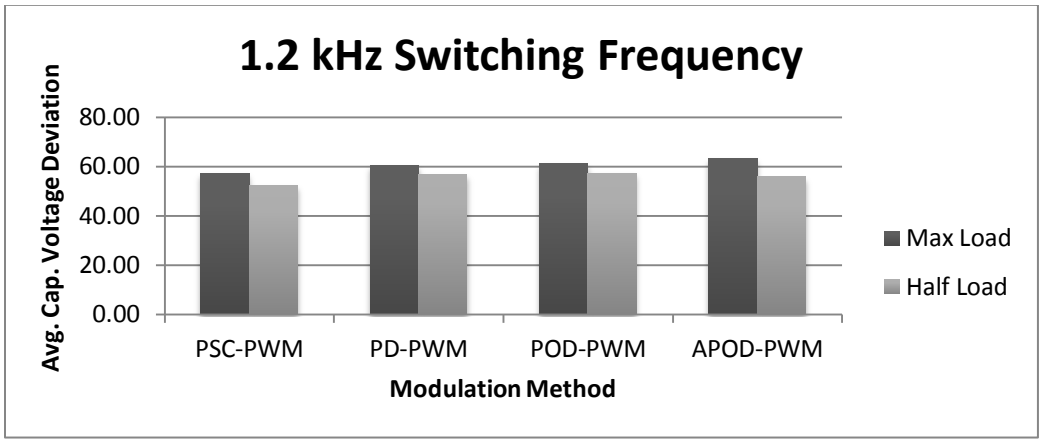

Figure 4.12 1.2 kHz Comparison, Conventional Voltage Balancing

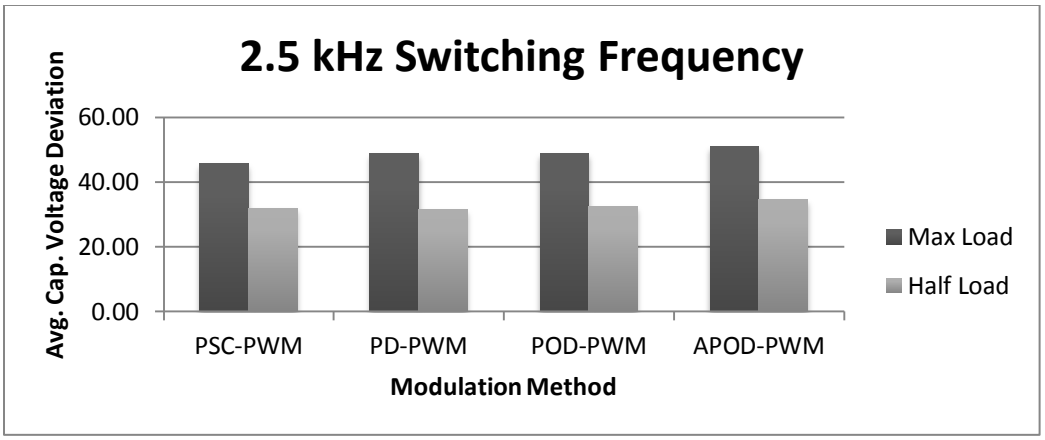

Figure 4.13 2.5 kHz Comparison, Conventional Voltage Balancing

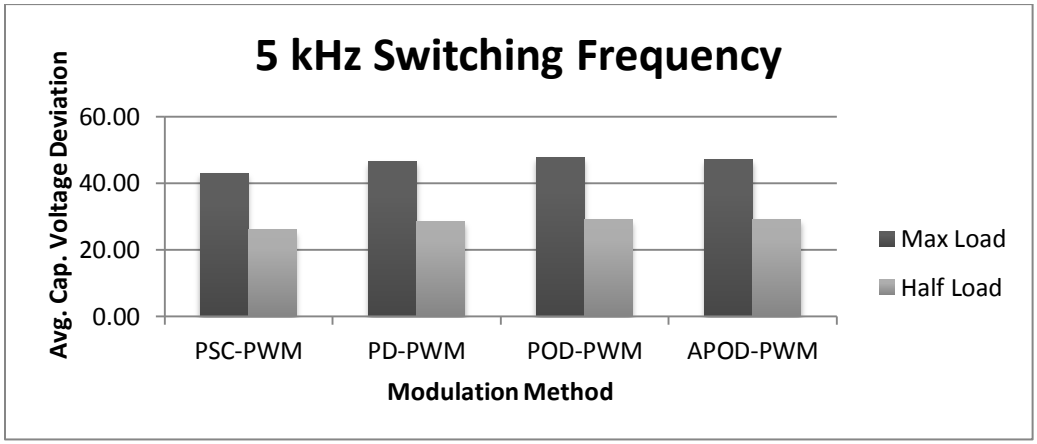

Figure 4.14 5 kHz Comparison, Conventional Voltage Balancing

From the perspective of capacitor voltage ripple minimization, these results show that phase-shifted pulse width modulation leads to a slight improvement in voltage deviation. This is the expected the result and validates the results of a basic analysis described in [9]. To visualize the benefit in regards to average capacitor voltage ripple,

Figure 4.15 to Figure 4.18 show for the maximum load conditions the voltage ripple difference between the two algorithms and in this case a roughly 10-15% improvement is shown. How much this algorithm increases the switching power loss needs to also be explored and this is important in deciding the true benefit of improved voltage balancing.

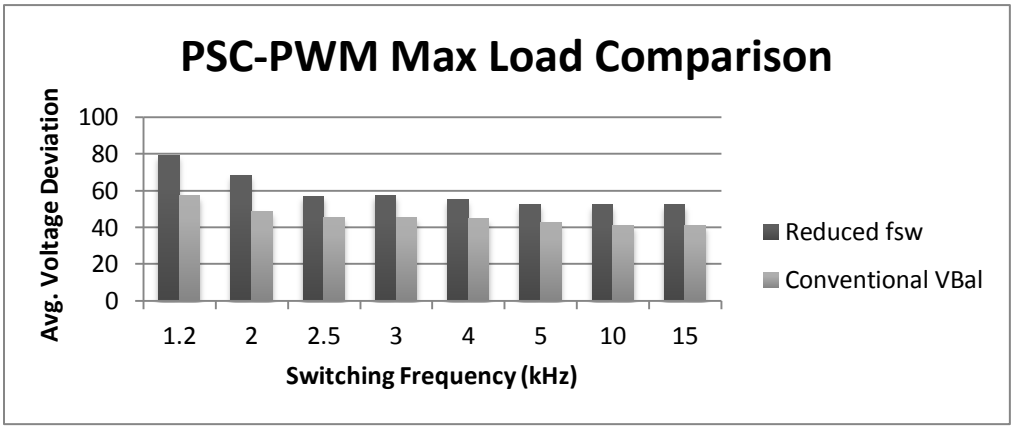

Figure 4.15 PSC-PWM Balancing Algorithm Comparison

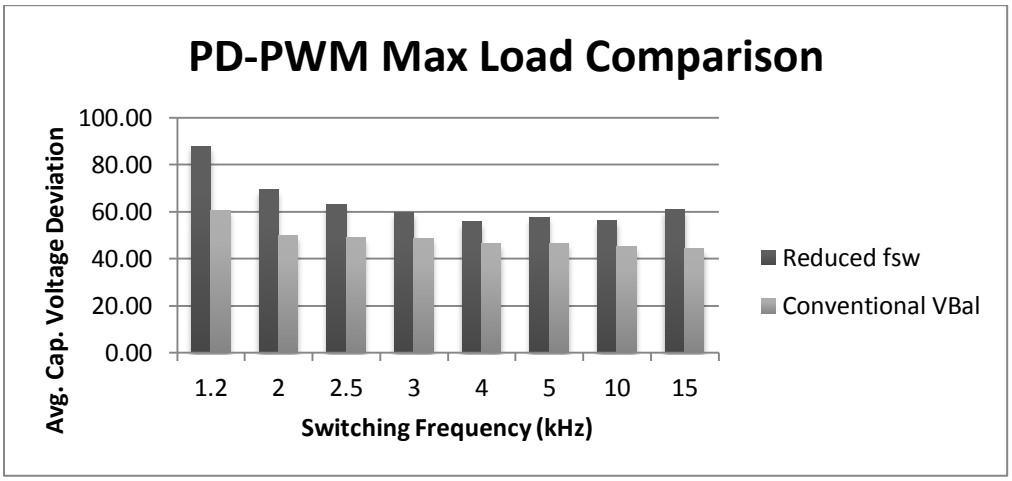

Figure 4.16 PD-PWM Balancing Algorithm Comparison

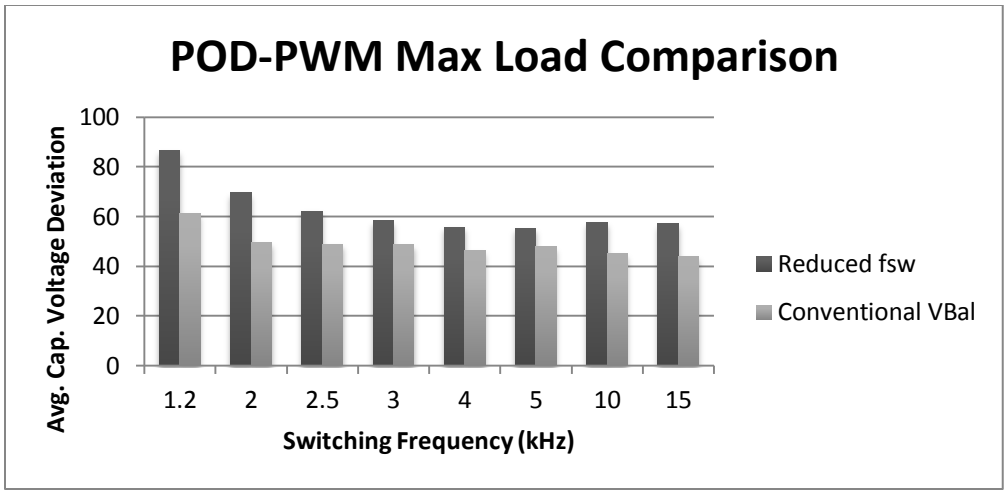

Figure 4.17 POD-PWM Balancing Algorithm Comparison

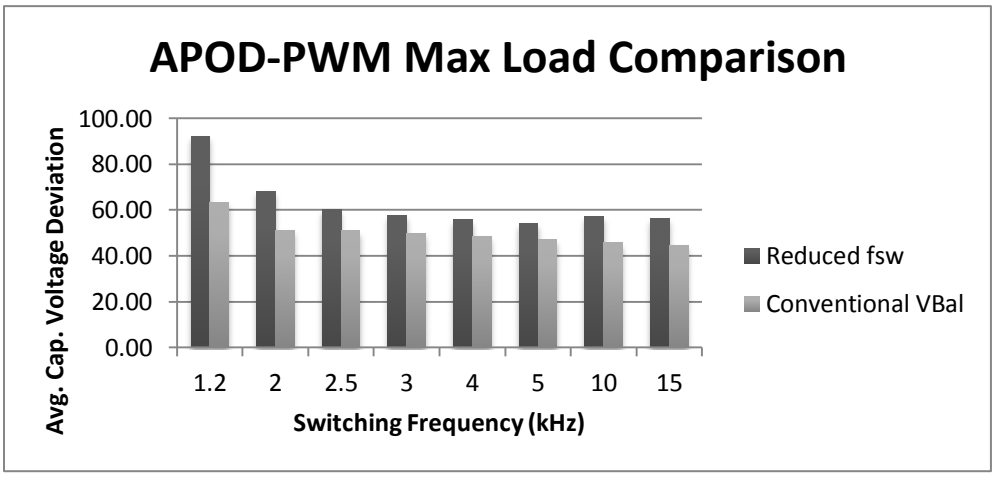

Figure 4.18 APOD-PWM Balancing Algorithm Comparison

4.2 Loss Modeling Results and Analysis

The converter loss analysis will include observing the specific results of switching power loss, conduction power loss and arm inductor windings power loss. The purpose of this is to see if for example a lower switching power loss results in an increase in another element of converter power loss. The circulating current in the modular multilevel converter will also be analyzed because it has a large effect on the overall power loss.

4.2.1 Switching Loss

As discussed previously, there are three components to switching loss: IGBT Turn-On, IGBT Turn-Off and Diode Turn-Off power loss.

Figure 4.19 shows these three power loss values for a switching frequency of 1.2kHz per submodule using the reduced switching frequency voltage balancing algorithm. Here a slightly lower power loss is shown for the phase-disposition PWM method. This is true for all three elements of switching power loss. Figure 4.20 and Figure 4.21 show similar results for switching frequencies of 5 kHz and 10 kHz respectively. Taking a look at each element of switching loss, it's expected that the IGBT Turn-Off loss would be in the range of 80% of the IGBT Turn-On loss depending on a number of factors. This was proven in the earlier description of switching power loss including the experimental calculations recorded in [17]. Also expected is that the diode loss while still significant, would be lower than the resultant losses from the IGBT.

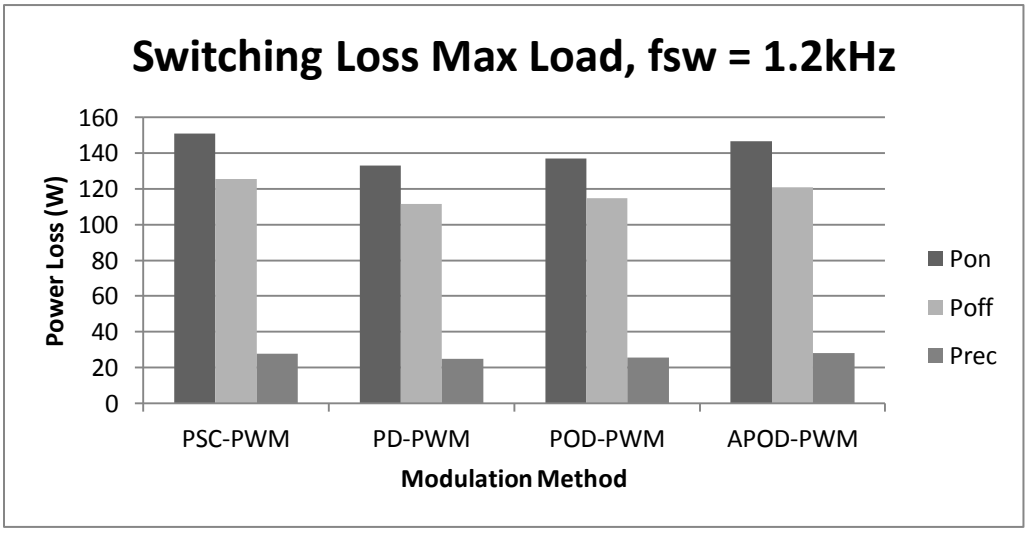

Figure 4.19 Switching Loss, Reduced fsw Voltage Balancing, 1.2 kHz

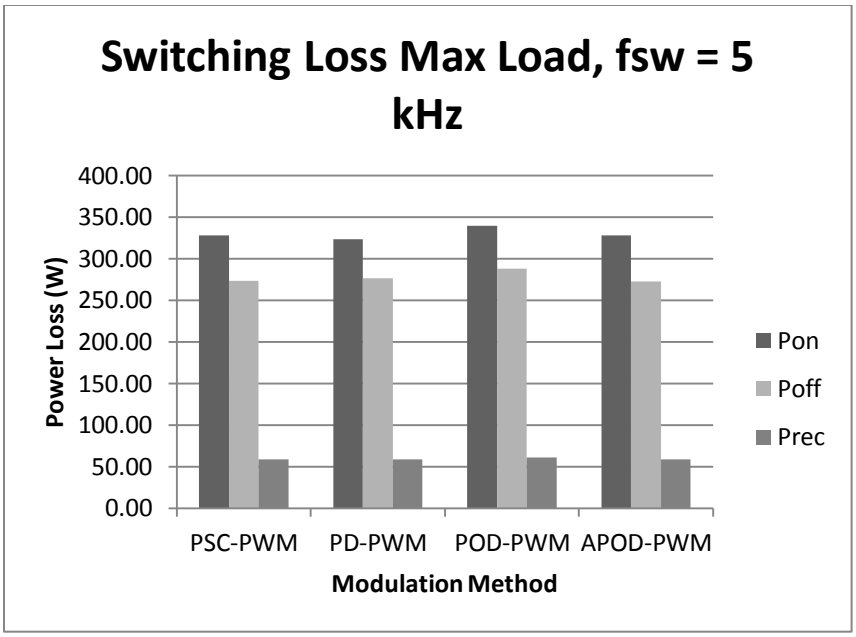

Figure 4.20 Switching Loss, Reduced fsw Voltage Balancing, 5 kHz

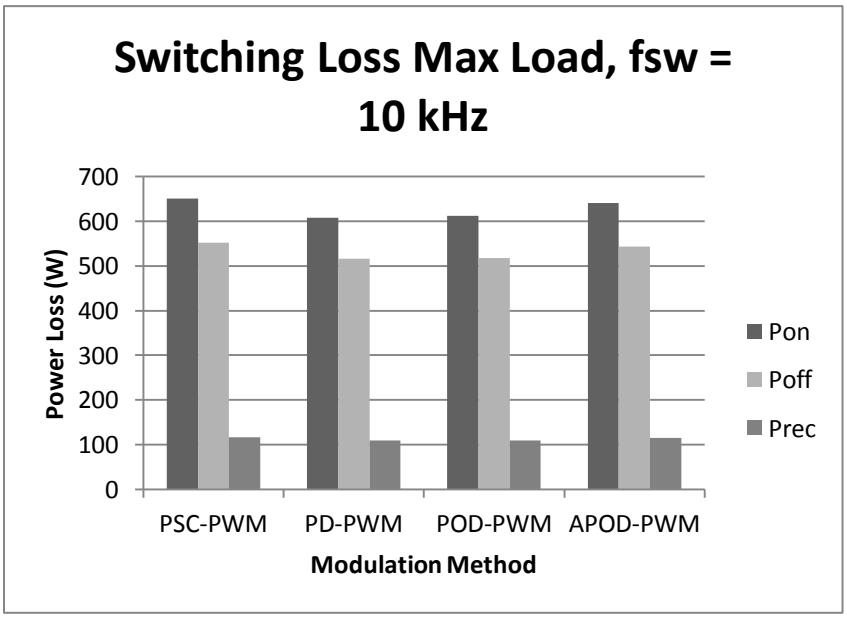

Figure 4.21 Switching Loss, Reduced fsw Voltage Balancing, 10 kHz

Figure 4.22 shows the total converter switching loss for each modulation method and this graphic shows a minimal difference between the 4 methods in question. This isn't unexpected because of the subtle differences in the resultant reference waveform

causing similar switching transitions. What is shown is a low total switching loss using this modulation and control implementation.

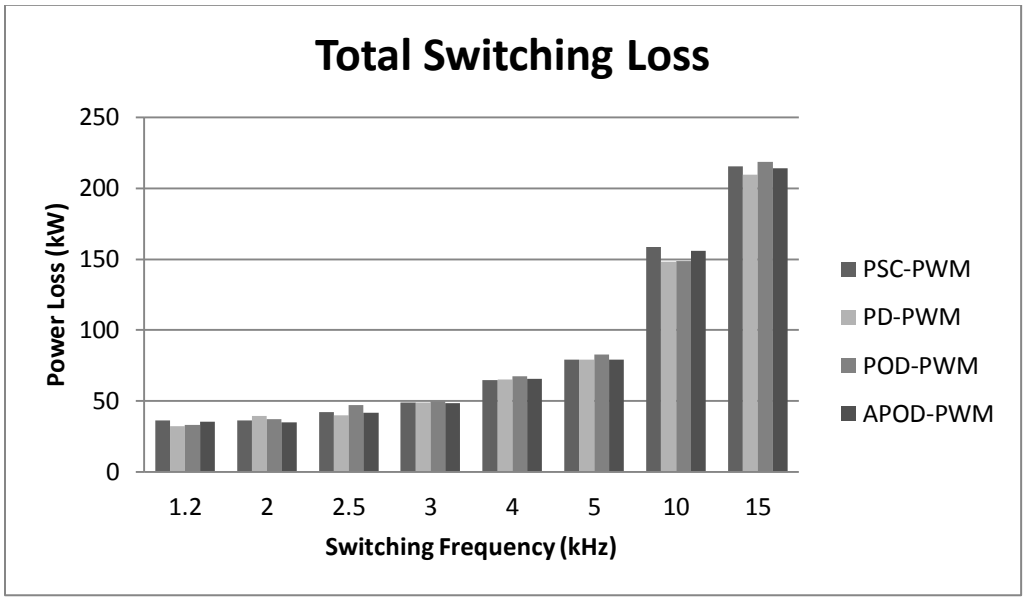

Figure 4.22 Total Converter Switching Loss, Reduced fsw Voltage Balancing

These same switching loss results will then be shown using the conventional voltage balancing algorithm. Figure 4.23 shows the switching loss under the same test conditions and a switching frequency of 3 kHz. In this case, even at the per submodule level there is a noticeable benefit to the phase-shifted modulation technique. Figure 4.24 and Figure 4.25 show the same results for switching frequencies of 5 kHz and 10 kHz. The results will then show whether or not this holds true for all switching frequencies.

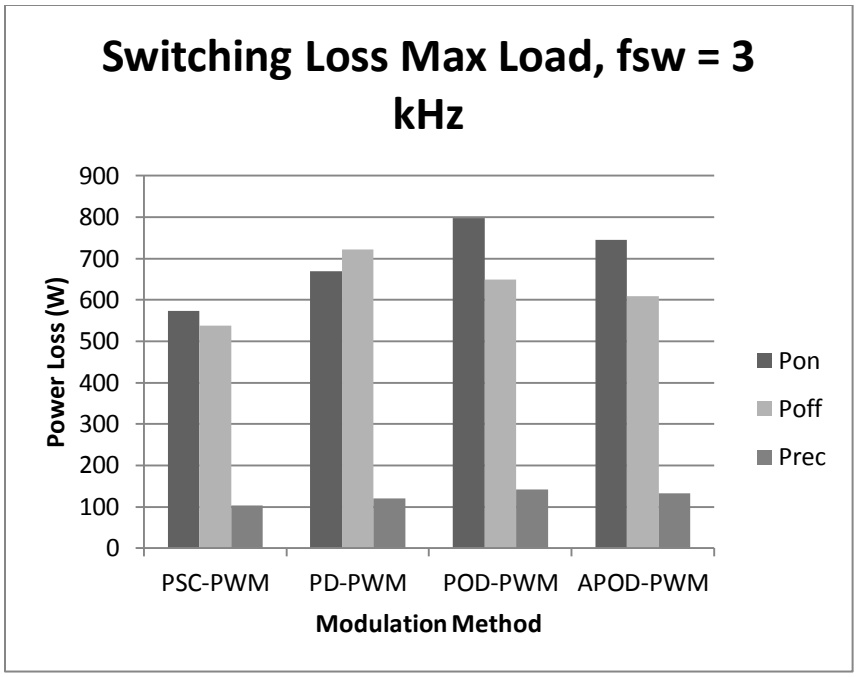

Figure 4.23 Per SM Switching Loss using Conventional Voltage Balancing, 3 kHz

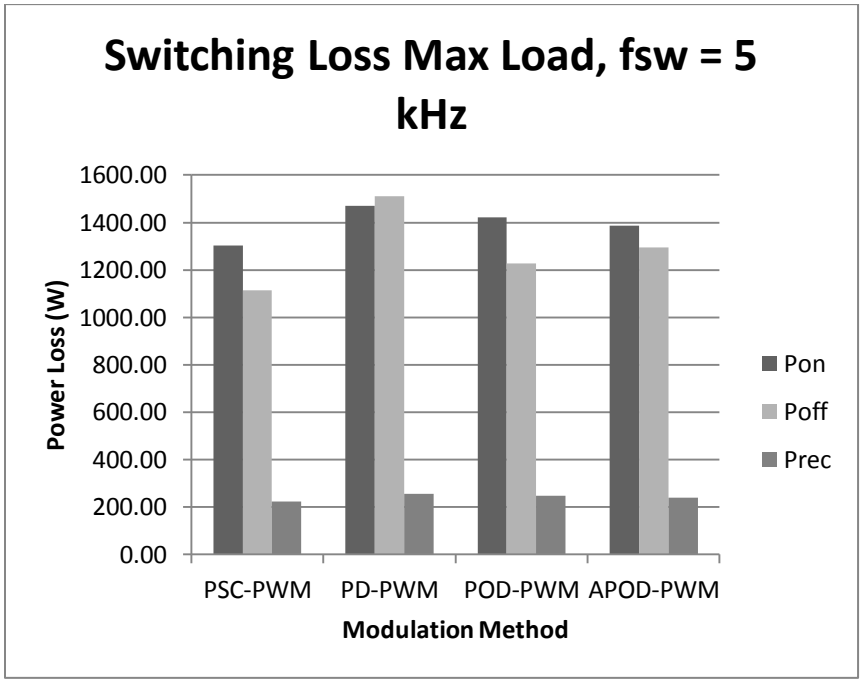

Figure 4.24 Per SM Switching Loss using Conventional Voltage Balancing, 5 kHz

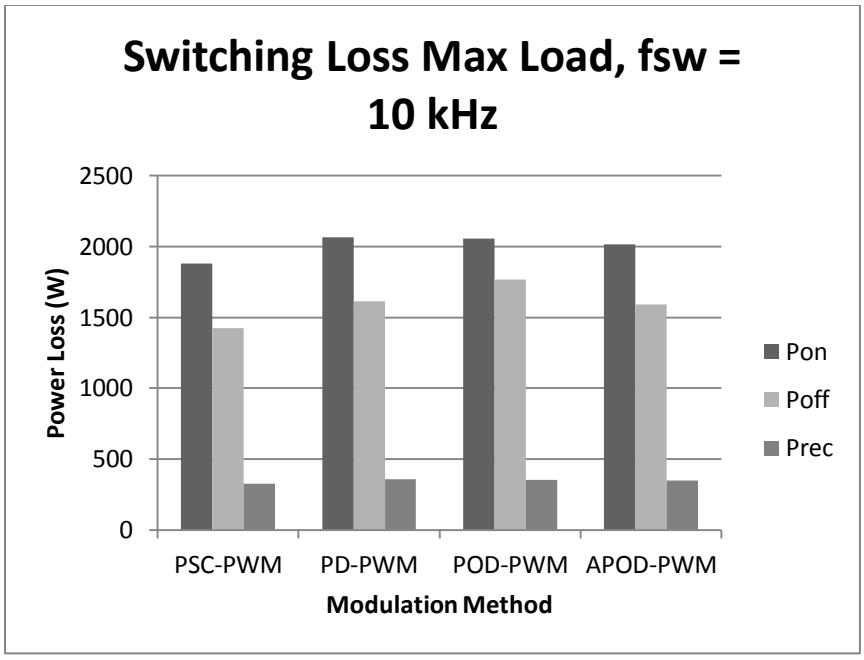

Figure 4.25 Per SM Switching Loss using Conventional Voltage Balancing, 10 kHz

Figure 4.26 shows the total switching loss using the conventional voltage balancing algorithm. Notice that the y-axis reflects power loss in terms of kilowatts. Here we see that the response between the level-shifted techniques varies depending on the switching frequency utilized. What holds true for almost all cases is that the phase-shifted technique shows a lower switching power loss. Strictly in terms of switching loss, the conclusion is that for the reduced switching frequency voltage balancing algorithm there is a minimal difference between each modulation technique but for the conventional balancing algorithm PSC-PWM shows the lowest switching loss for all switching frequencies. This cannot be the only power loss metric however, so conduction losses under the same model characteristics need to be understood.

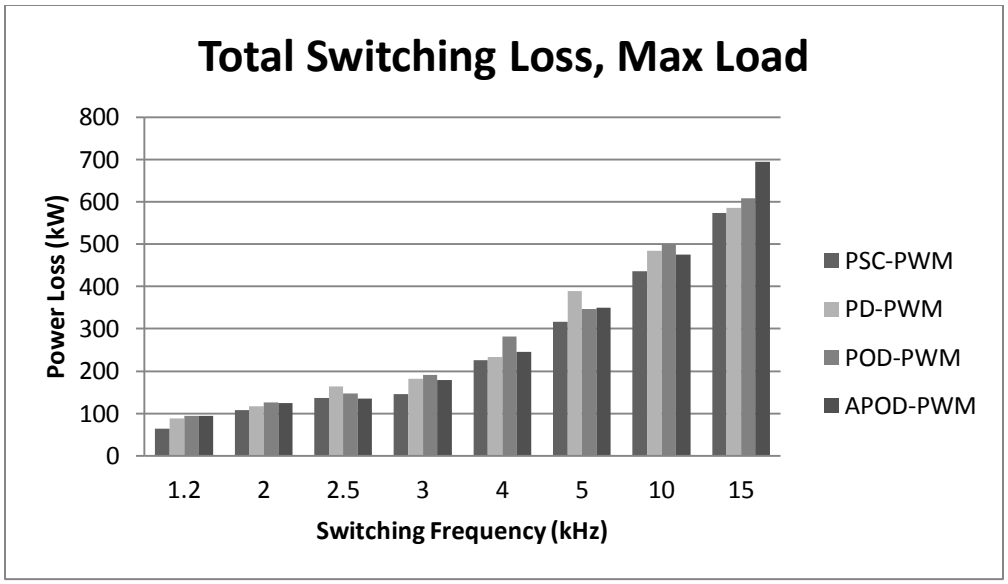

Figure 4.26 Total Switching Loss, Conventional Voltage Balancing Algorithm

4.2.2 Conduction Loss

Conduction loss occurs in a modular multilevel converter due to the on-state saturation voltage of both the IGBTs and the anti-parallel diodes. This results in heat dissipation during every time instant that the device is in an on state. This section will first look at the per submodule average conduction loss for the various test conditions then the total conduction loss will be addressed.

Figure 4.27 shows the per submodule conduction loss using an active power reference of 20 MW for each modulation method and using the reduced switching frequency voltage balancing algorithm. Figure 4.28 shows the same results but using the conventional voltage balancing algorithm. For this test case, the resultant conduction loss doesn't have a large deviation over each modulation method. If using the reduced switching frequency implementation, there appears to be slight benefits depending on the desired switching frequency. Also seen in these two figures is that for the higher switching frequencies the conduction loss decreases and this is because the total

switching time increases which thereby decreases the total on time of the semiconductor devices.

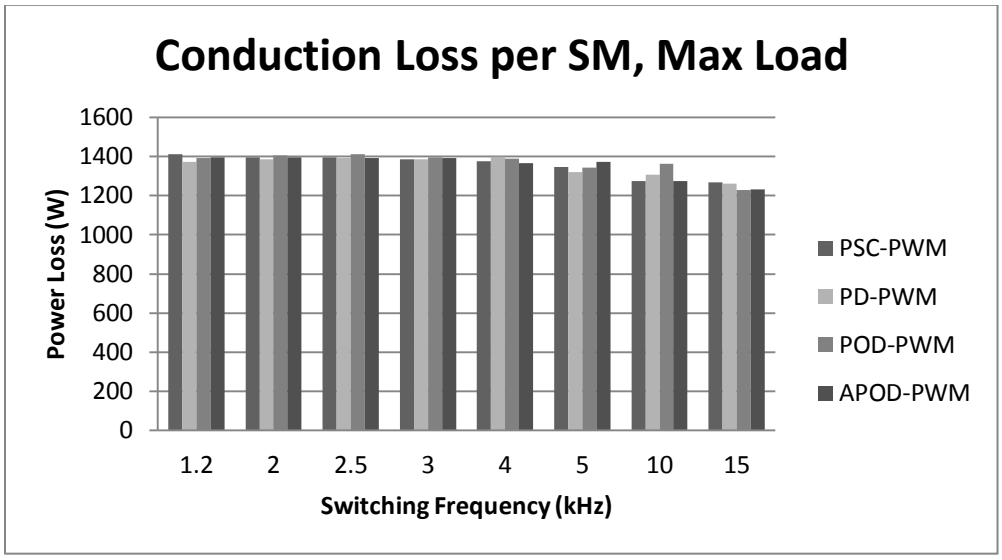

Figure 4.27 Per Submodule Conduction Loss, Reduced fsw Voltage Balancing

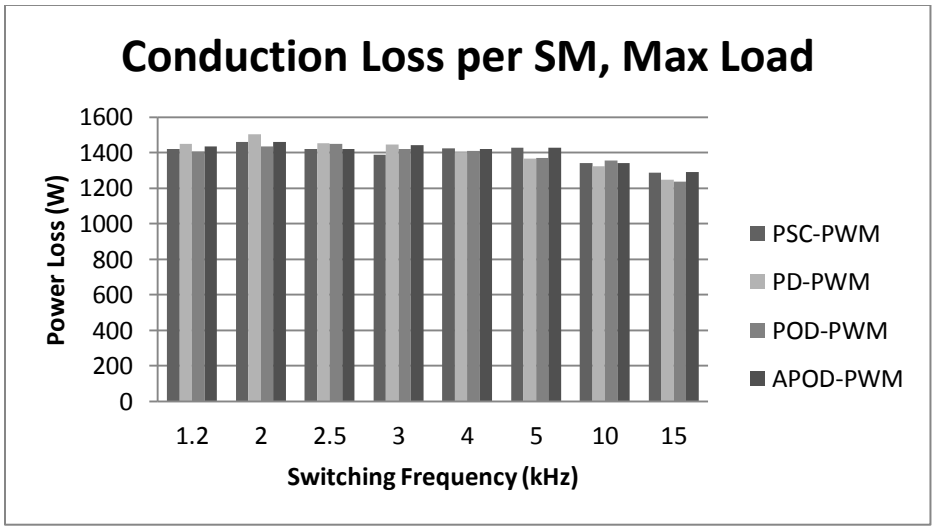

Figure 4.28 Per Submodule Total Conduction Loss, Conventional Voltage Balancing

Figure 4.29 shows the total converter conduction loss, in kilowatts, over a range of switching frequencies for each PWM method using the reduced switching frequency voltage balancing algorithm. This result shows that for switching frequencies of 5 kHz and greater, the total conduction loss is slightly reduced using the reduced switching

frequency voltage balancing algorithm. This is a different result than the conventional voltage balancing algorithm data, shown in Figure 4.30, where different level-shifted techniques show an improvement in conduction loss.

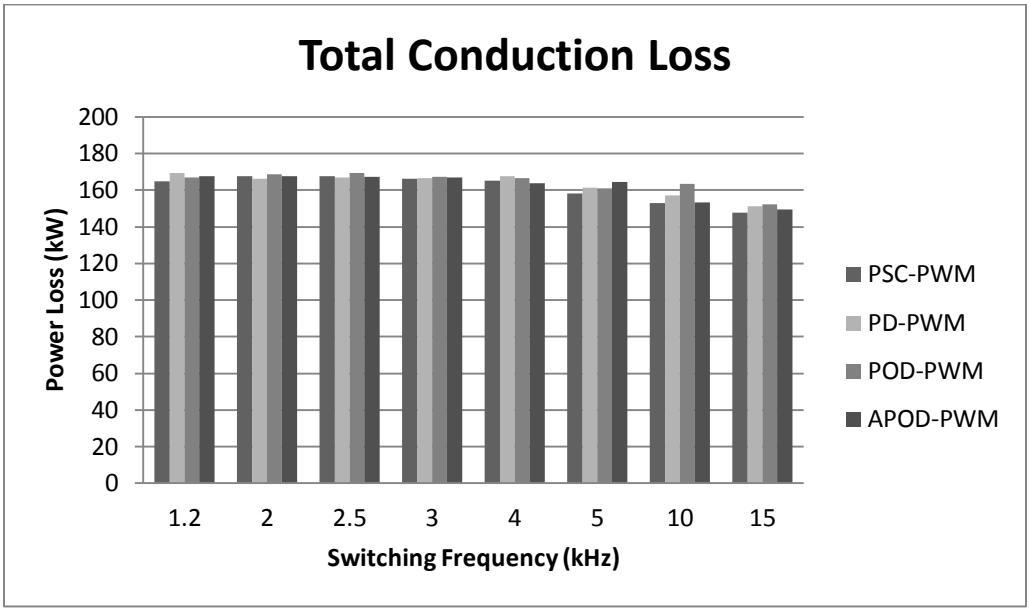

Figure 4.29 Total Converter Conduction Loss, Reduced fsw Voltage Balancing

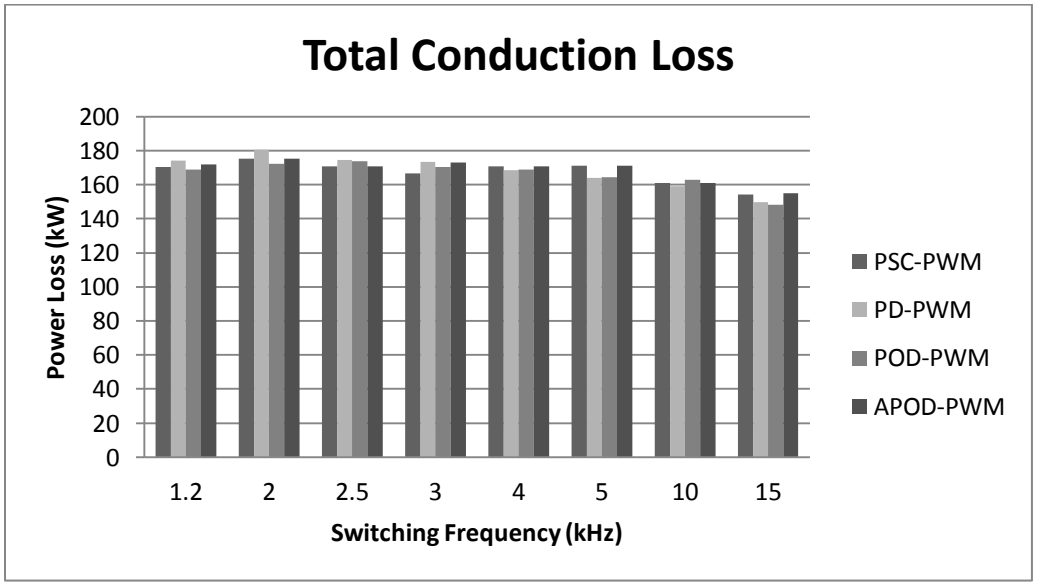

Figure 4.30 Total Converter Conduction Loss, Conventional Voltage Balancing

The next comparison of interest is how conduction loss varies with different voltage balancing algorithms. Figure 4.31 shows, using the phase-shifted PWM method, that while the conventional voltage balancing algorithm decreases the capacitor voltage deviation the conduction loss increases. Figure 4.32 shows the same results for the phase-disposition PWM method. For this level-shifted technique, the difference in conduction loss between the voltage balancing options is similar to the level-shifted PWM results. Figure 4.33 and Figure 4.34 show the same data for the remaining level-shifted PWM methods. This shows that the conventional balancing algorithm increases both the switching power loss and the conduction power loss.

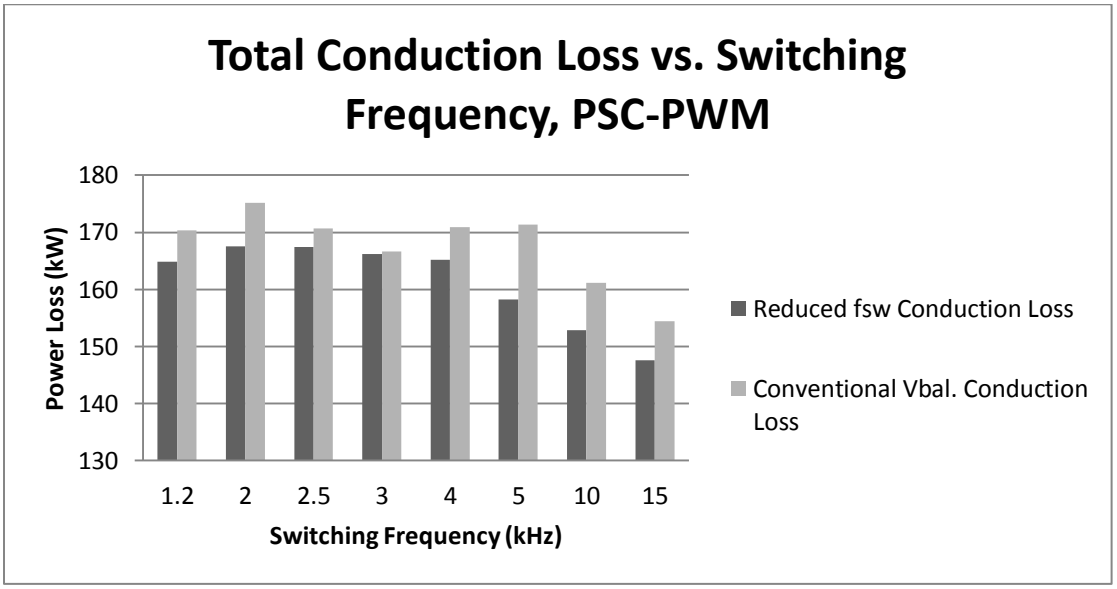

Figure 4.31 Voltage Balancing Algorithm Comparison, PSC-PWM

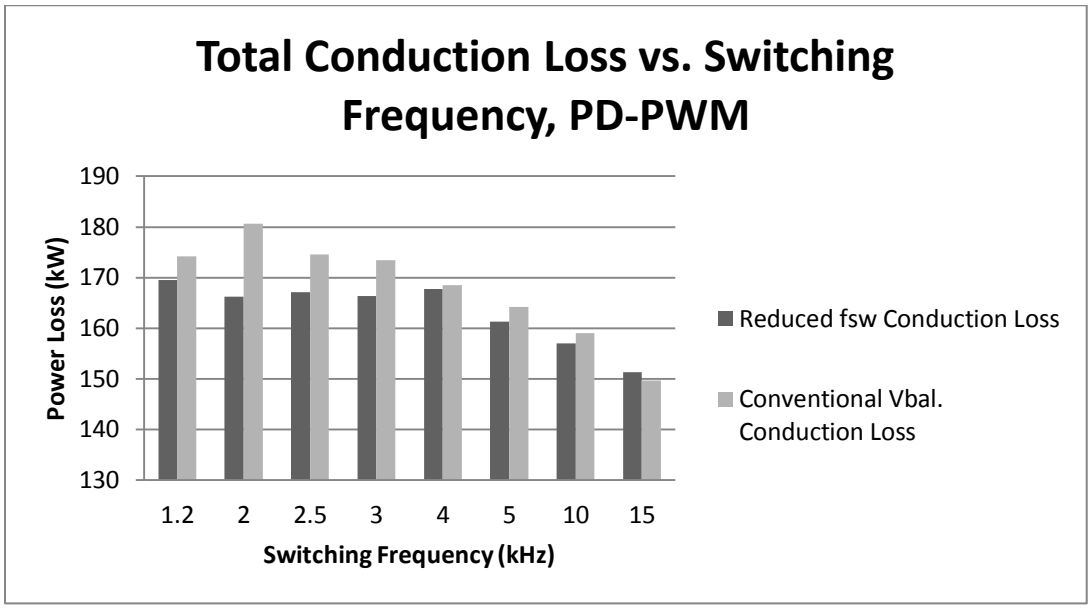

Figure 4.32 Voltage Balancing Algorithm Comparison, PD-PWM

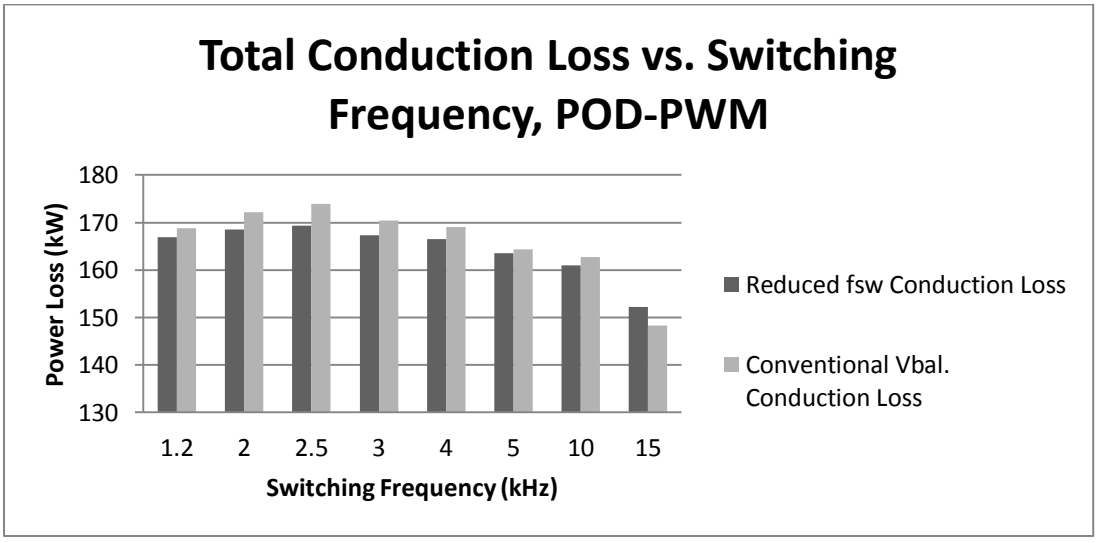

Figure 4.33 Voltage Balancing Algorithm Comparison, POD-PWM

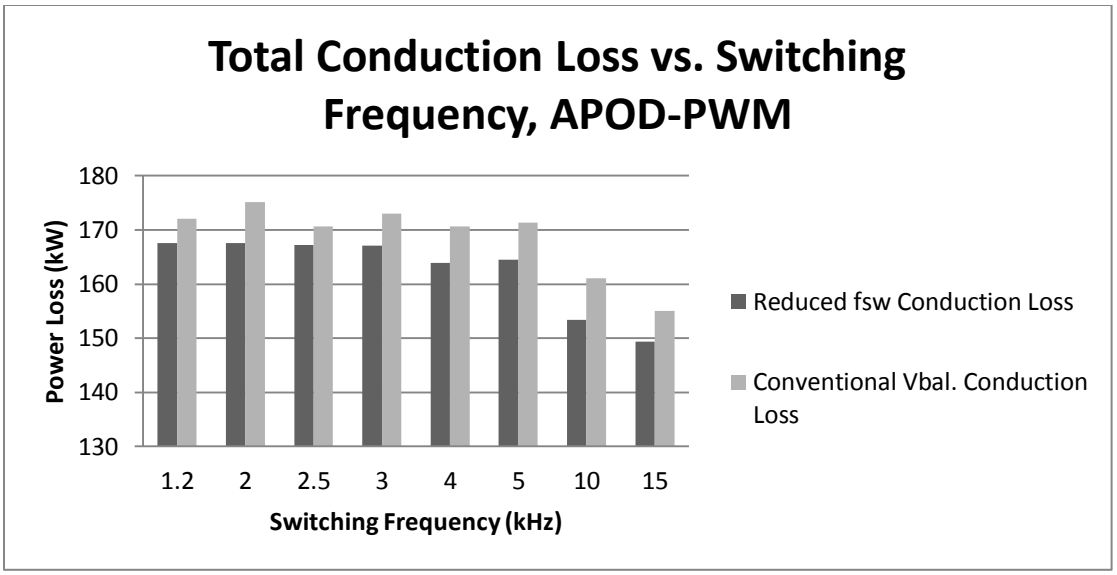

Figure 4.34 Voltage Balancing Algorithm Comparison, APOD-PWM

4.2.3 Arm Inductor Winding Loss

The final element of converter power loss is the power loss due to the arm impedance in series with each arm of the converter. This power loss occurs due to the DC resistance of the windings along with the added resistance as a result of skin effect and other factors. Figure 4.35 shows the total converter arm impedance power loss over a range of frequencies using the reduced switching frequency voltage balancing algorithm. Figure 4.35 shows mixed results in which method is the most beneficial modulation scheme. Figure 4.36 shows the same data using the conventional voltage balancing algorithm and again an inconclusive result is again shown. This data does show, however, that regardless of what control method used and switching frequency chosen the maximum difference in arm inductor winding power loss is 50 kW. While not negligible, this data is all garnered from a simulation of a 20 MW modular multilevel converter so this deviation affects the efficiency in the range of 0.25% at the most.

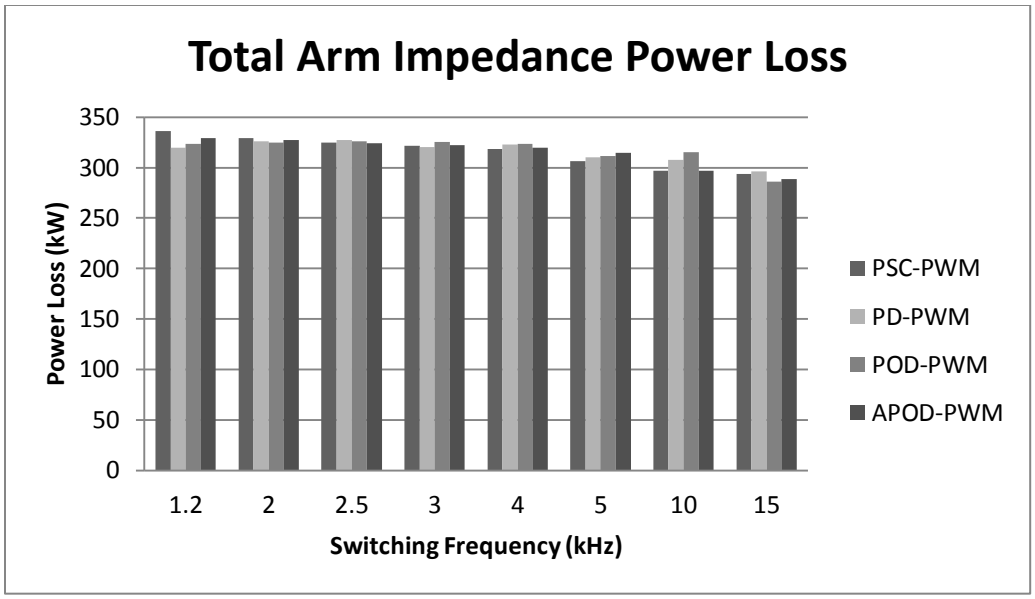

Figure 4.35 Total Arm Impedance Power Loss, Reduced fsw

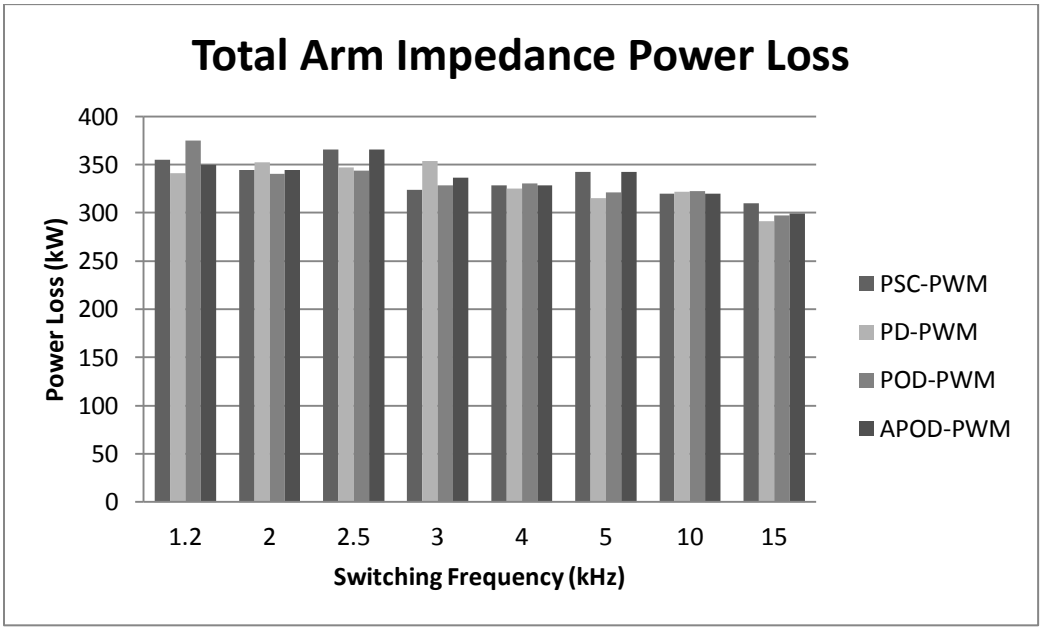

Figure 4.36 Total Arm Impedance Power Loss, Conventional Voltage Balancing

4.2.4 Total Power Loss

The next step is to observe the total power loss for these test cases and analyze the converter efficiency. Figure 4.37 shows the total converter power loss using the reduced switching frequency voltage balancing algorithm.

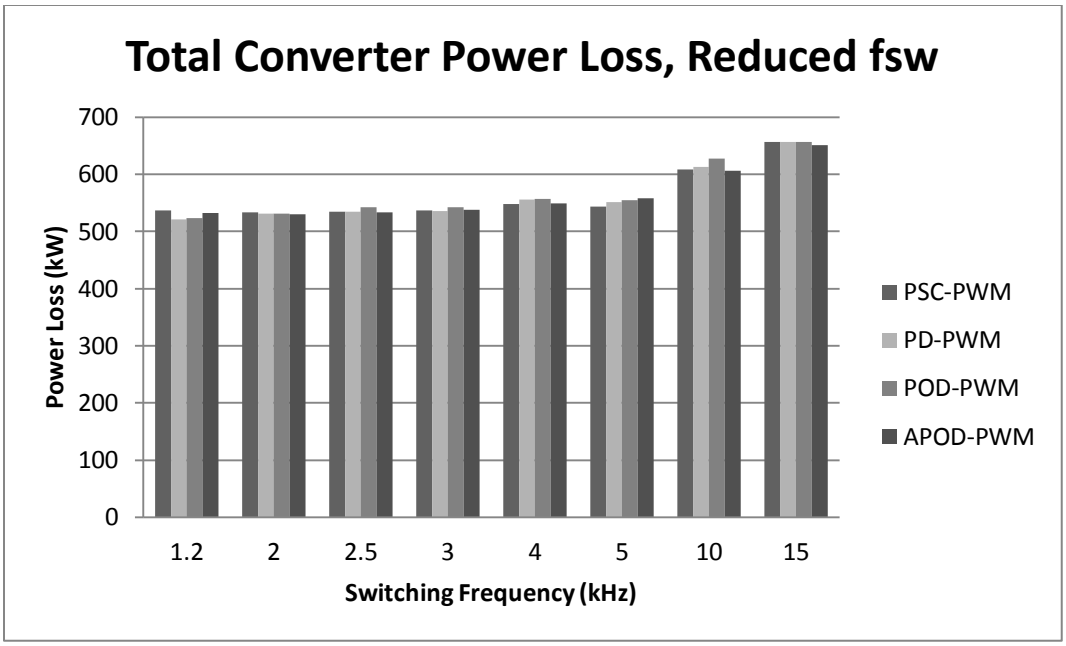

Figure 4.37 Total Converter Power Loss, Reduced fsw Voltage Balancing

Figure 4.38 shows the total converter power loss using conventional voltage balancing and shows that the phase-shifted PWM shows a slight benefit at most switching frequencies. The big difference between Figure 4.37 and Figure 4.38 is tied to the switching loss which is much larger for this conventional voltage balancing as expected particularly for switching frequencies higher than 5 kHz. An interesting result is that in this work the arm impedance power loss dominates compared to switching and conduction power loss. This shows that for lower level converters, the losses due to the arm impedance are much larger, reducing the benefit of a specific PWM technique and voltage balancing algorithm. At some point, for larger level converters the switching and conduction power loss will be much larger than the arm impedance power loss. In this case, the effect of each PWM technique and voltage balancing algorithm would prove to be much more important. For example, the result was that for the reduced switching frequency balancing algorithm PD-PWM showed an improvement in the switching power loss and could important to use this modulation technique.

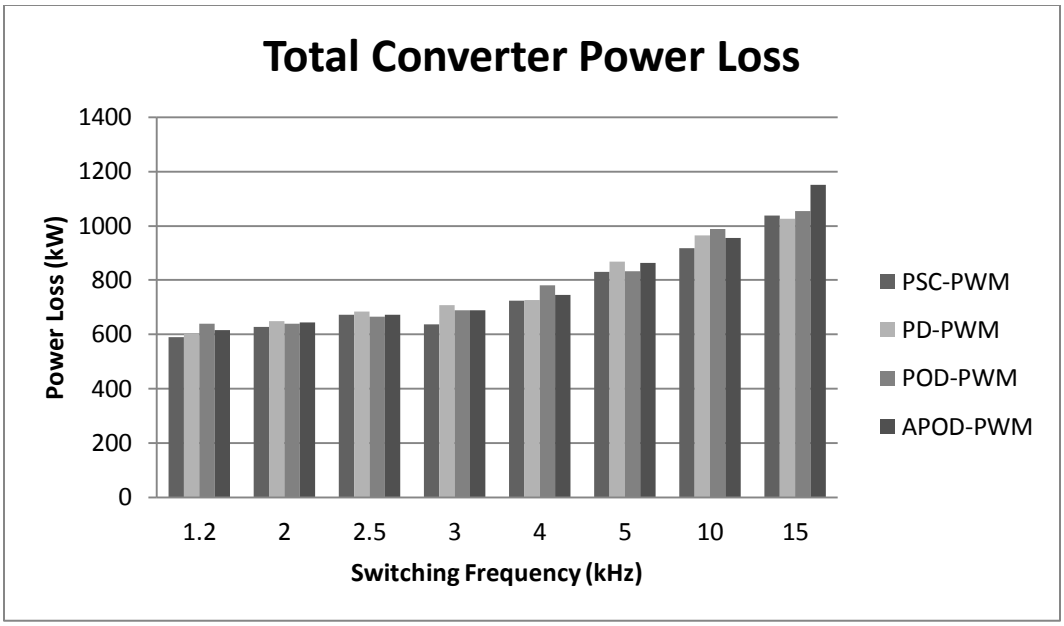

Figure 4.38 Total Converter Power Loss, Conventional Voltage Balancing

4.3 Harmonics

Reference [9] claims that level-shifted techniques provide an improvement in the reduction of harmonics compared to phase-shifted techniques. Another goal of this work is to validate or dispute this claim and determine that if true what level-shifted technique performs the best. A known benefit of the modular multilevel converter topology is an inherent reduction of harmonics reducing the AC filter burden. The harmonics that due arise are low in magnitude and centered around the switching frequency.

4.3.1 THD Analysis

Table 4.1 shows the values of the THD of the converter voltage using a 20 MW active power reference for each modulation technique and the reduced switching frequency balancing algorithm. Table 4.2 shows the same results for a 10 MW active power reference. The phase-disposition modulation technique shows a definitive

improvement in terms of converter voltage THD. An interesting result is that both the POD-PWM and APOD-PWM techniques do not show this harmonic improvement.

Table 4.1 20 MW Active Power Reference THD Analysis

20 MW				
fsw	PSC-PWM	PD-PWM	POD-PWM	APOD-PWM
1.2	5.83	3.026	5.48	5.36
2	5.67	2.984	5.417	5.3
2.5	5.6	3.057	5.521	5.294
3	5.6	3.126	5.435	5.315
4	5.53	3.097	5.331	5.285
5	5.66	3.014	5.508	5.419
10	5.7	2.86	5.6	5.48
15	5.6	3.167	5.54	5.57

Table 4.2 10 MW Active Power Reference THD Analysis

10 MW				
fsw	PSC-PWM	PD-PWM	POD-PWM	APOD-PWM
1.2	5.01	2.95	4.675	5.053
2	4.92	2.82	4.83	4.96
2.5	5.13	3.06	4.91	5.108
3	5.06	2.87	4.805	5.062
4	4.93	2.91	4.732	5.133
5	5.089	3.1	4.69	5.06
10	5.16	2.96	4.934	5.1
15	5.04	2.94	4.815	5.083

The next results show the same results but using the conventional voltage balancing algorithm. Table 4.3 shows the THD results for the 20 MW simulation and Table 4.4 shows the THD results for the 10 MW test.

Table 4.3 20 MW Active Power Reference THD Analysis, Conventional Balancing

20 MW				
fsw	PSC-PWM	PD-PWM	POD-PWM	APOD-PWM
1.2	8.31	7.7	7.2	7.49
2	7.94	7.45	7.12	7.16
2.5	6.85	6.36	7.18	6.85
3	6.583	6.691	7.01	6.91
4	6.708	6.61	6.17	6.69
5	6.58	6.29	5.8	6.15
10	6.95	6.87	6.27	6.33
15	7.18	6.93	6.72	6.77

Table 4.4 10 MW Active Power Reference THD Analysis, Conventional Balancing

10 MW				
fsw	PSC-PWM	PD-PWM	POD-PWM	APOD-PWM
1.2	7.43	6.946	8.06	7.81
2	7.38	7.09	8.13	7.55
2.5	7.31	7.16	7.94	7.24
3	7.46	6.53	6.88	6.73
4	7.18	6.4	6.59	6.54
5	6.44	5.97	6.1	5.72
10	6.88	6.03	5.86	5.95
15	7.07	6.47	6.38	6.91

For the conventional voltage balancing algorithm, there is still a THD benefit for the level-shifted methods even though the percentage benefit is reduced. In this case, all the level-shifted methods show improved converter voltage THD.

4.3.2 Frequency Spectrum Analysis

One way to visualize the harmonic benefit of one method to another is to take the fast fourier transform of the converter voltage and plotting the results. The results will show the magnitude of each harmonic over a range of frequency. The expected result

here is that there should be a large fundamental harmonic along with low-amplitude harmonics centered around the switching frequency. Also, per the literature review the level-shifted modulation techniques should provide an improved harmonic reduction. Figure 4.39 shows the frequency spectrum plot of the converter voltage using PSC-PWM and PD-PWM and using the reduced switching frequency voltage balancing algorithm. Shown off screen at 60 Hz is the fundamental harmonic along with harmonics located around the switching frequency which is 5 kHz in this case. The interesting result here is that PD-PWM significantly reduces the harmonics around the switching frequency resulting in quite a low converter voltage THD. The next step is the see if this is true for the other level-shifted modulation techniques. Figure 4.40 and Figure 4.41 show the same results comparing PSC-PWM to POD-PWM and APOD-PWM respectively. The result is that these level-shifted techniques actually show higher harmonic content around the switching frequency. Figure 4.42 and Figure 4.43 and Figure 4.44 show the same frequency spectrum plots using the conventional voltage balancing algorithm. The result is that this voltage balancing algorithm does not show the same reduction of the low frequency harmonics. It's these harmonics from 0-1kHz that cause the increase in converter voltage THD.

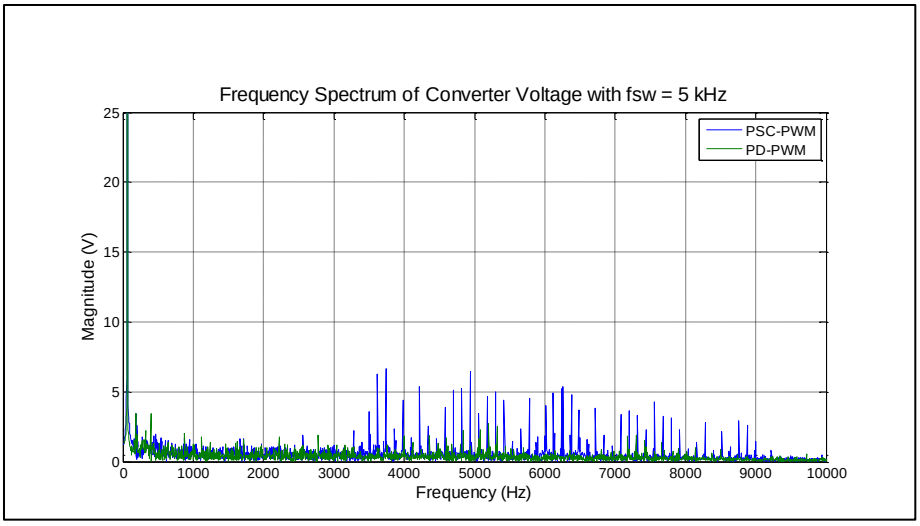

Figure 4.39 Frequency Spectrum for PSC-PWM and PD-PWM at fsw = 5 kHz

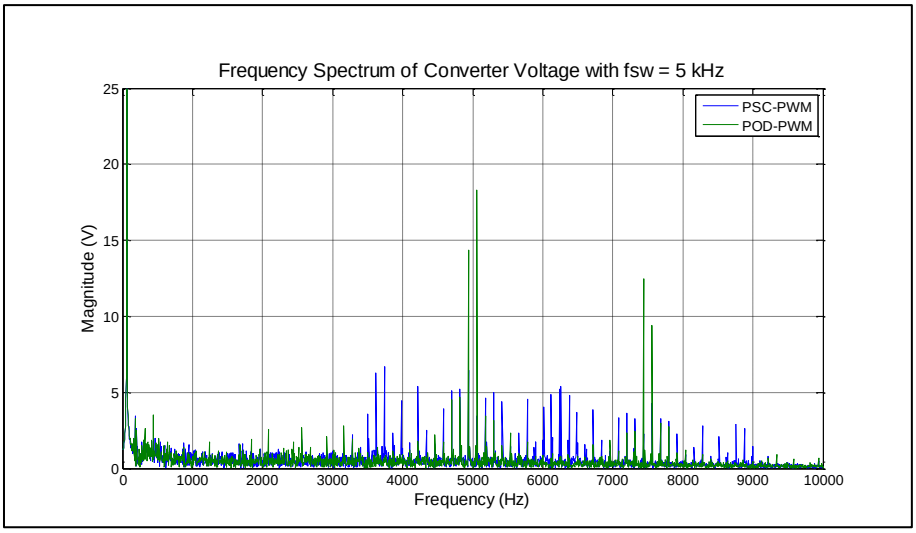

Figure 4.40 Frequency Spectrum for PSC-PWM and POD-PWM at fsw=5kHz

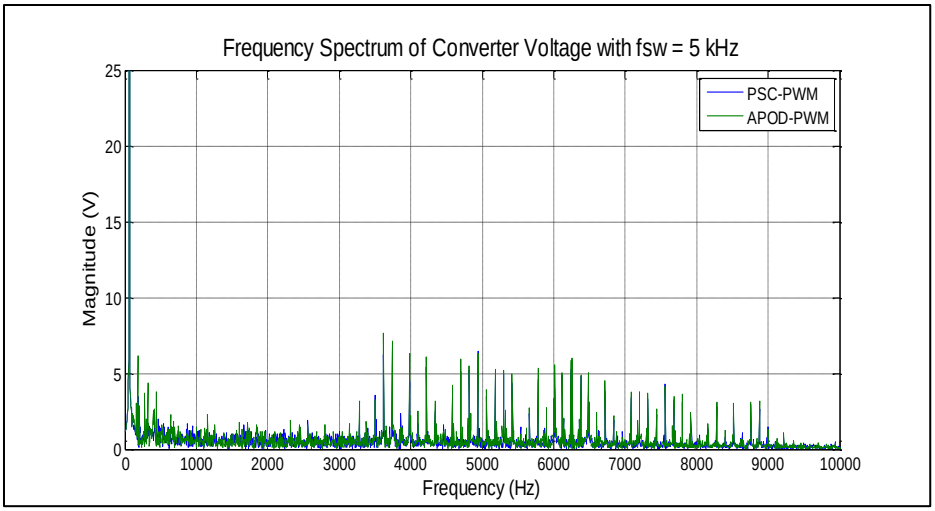

Figure 4.41 Frequency Spectrum for PSC-PWM and APOD-PWM with fsw = 5 kHz

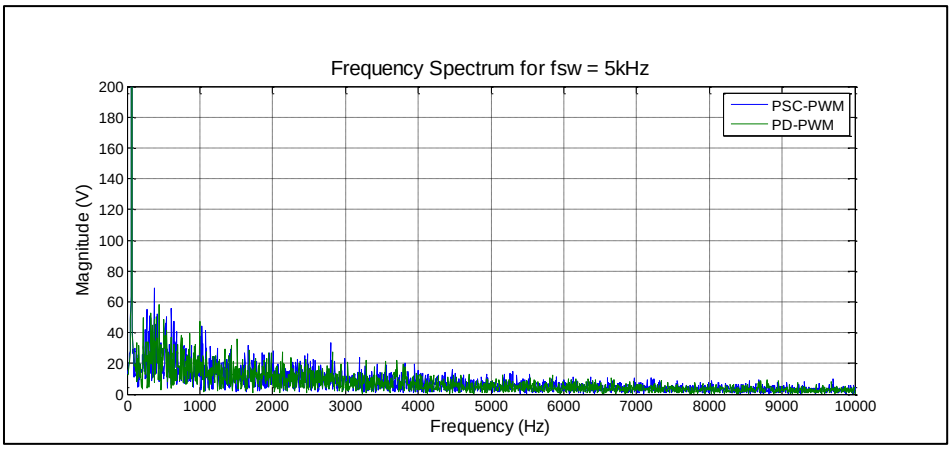

Figure 4.42 Frequency Spectrum for PSC-PWM and PD-PWM, Conventional

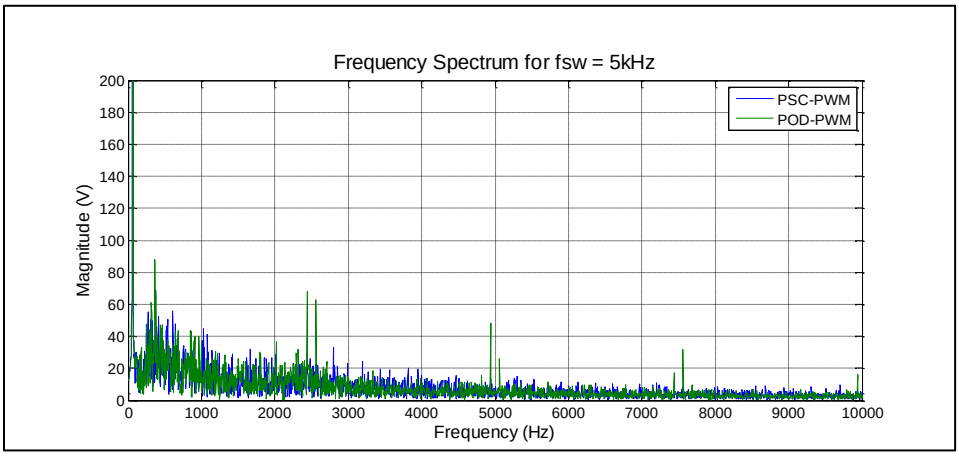

Figure 4.43 Frequency Spectrum for PSC-PWM and POD-PWM, Conventional

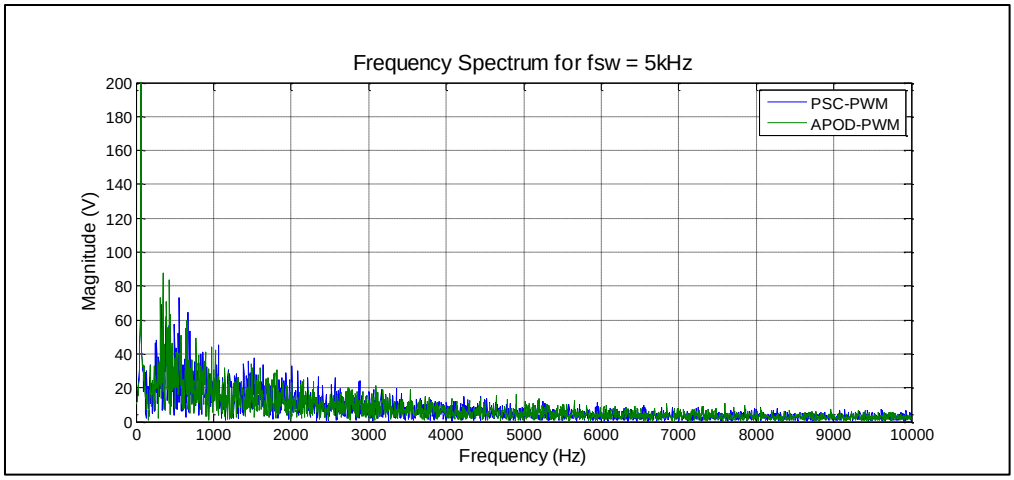

Figure 4.44 Frequency Spectrum for PSC-PWM and APOD-PWM, Conventional

Chapter 5

CONCLUSION

The goal of this research was to find the optimum pulse width modulation and voltage balancing algorithm combination for a modular multilevel converter given the end user's design requirements. This includes minimizing capacitor voltage ripple, reducing converter power losses, reducing required switching frequency and converter voltage harmonic reduction. To accomplish this goal, a three phase 20-level modular multilevel converter was developed using MATLAB/Simulink and analysis for several key metrics was performed. From these results, the best PWM and balancing algorithm can be quickly chosen for a given application.

A key to modular multilevel converter operation is limiting the ripple of the capacitor voltages. This reduces the circulating current flowing within the converter. If the goal is to achieve the lowest capacitor voltage ripple only, the conventional voltage balancing algorithm results in the lowest average voltage ripple and a roughly 20% benefit when compared to the reduced switching frequency balancing algorithm. The obvious trade-off in this selection is an increase in the switching power loss using the conventional algorithm. Also, for both balancing algorithms, phase-shifted carrier PWM provides a clear reduction in capacitor voltage ripple. This benefit is more significant at lower switching frequencies and reduces for switching frequencies above 5kHz.

Limiting the total converter power loss is an obvious concern when making this decision. There is a clear trade-off when considering that the conventional voltage balancing algorithm reduces the average voltage ripple by roughly 20% but results in a much higher switching power loss. In regards to switching power loss only, phase disposition provides a reduction in power loss using the reduced switching frequency balancing algorithm. For the conventional voltage balancing algorithm, phase-shifted PWM showed a reduction in switching power loss and was noticeable even at the per submodule level. For conduction power loss, if using the reduced switching frequency balancing algorithm, PSC-PWM provides a reduction in semiconductor device conduction power loss. With the conventional voltage balancing algorithm, the result is that the level-shifted PWM techniques reduce the total conduction loss with a similar benefit shown for each option. The power loss due to the arm inductor windings remains fairly constant for all the PWM and balancing options. Also, the arm inductor power loss in this model is much larger than the switching and conduction loss limiting the variation between PWM techniques and balancing algorithms with respect to total converter power loss. However, for converters with a higher number of levels, the switching and conduction power loss of the devices will eventually dominate compared to the arm inductor power loss. Choosing the PWM technique and balancing algorithm that results in specifically reduced switching and/or conduction power loss would then be crucial to converter efficiency for converters with a high number of levels.

Harmonic reduction is an important metric particularly when considering the potential applications of modular multilevel converters. For a motor drive system, harmonics can result in motor acoustics and vibrations that can cause many problems for

the motor and its assembly. Harmonics are present in both the converter voltage and current waveforms. The modular design of this converter topology, specifically the number of voltage levels achievable, allows for a significant reduction in harmonics. The expected remaining harmonics include the harmonic at the fundamental frequency and low amplitude harmonics centered around the switching frequency. For the reduced switching frequency balancing algorithm, phase-disposition PWM shows better converter voltage harmonic reduction for all switching frequencies. For the conventional voltage balancing algorithm, all PWM techniques show similar converter voltage harmonics.

These results, shown in Table 5.1, provide the best pulse-width modulation technique and voltage balancing algorithm to select given an end user's design requirements.

Table 5.1 PWM and Balancing Selection Table

Design Characteristic	Modulation Method	Balancing Algorithm
Minimum Capacitor Voltage Ripple	PSC-PWM	Reduced fsw
	PSC-PWM	Conventional
Minimization of Switching Power Loss	PD-PWM	Reduced fsw
	PSC-PWM	Conventional
Minimization of Conduction Power Loss	Any	Reduced fsw
	POD-PWM	Conventional
Minimization of Total Converter Power Loss	PSC-PWM	Any
Harmonic Reduction	PD-PWM	Any
Reduced Switching Frequency	Any	Reduced fsw

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