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Applications Of Impedance Identification To Electric Ship System Control And Power Hardware-In-The-Loop Simulation

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APPLICATIONS OF IMPEDANCE IDENTIFICATION TO ELECTRIC SHIP SYSTEM CONTROL AND POWER HARDWARE-IN-THE-LOOP SIMULATION

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To my parents, John and Jeanne Siegers

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ABSTRACT

Recent advances in semiconductor technology, controls, and switching converter topologies have resulted in the increasing application of power electronics in power distribution systems. Power electronic enabled distribution systems have inspired a renewed interest in DC distribution architectures as an appealing alternative to traditional AC methods due to the significant performance and efficiency gains they offer. However, the notional power electronic based DC distribution system is a complex and extensively interconnected system consisting of multiple power converters. As a result, a number of system-level challenges related to stability arise due to interaction among multiple power converters. In addition, the power distribution system is likely to undergo configuration variations as the system is subject to component upgrades, changes in power sources and loading, and even contingency scenarios involving fault conditions. The design of this type of system is difficult due to the general lack of proper analysis tools and limited understanding of the problem.

To address these design challenges, an approach to control design that accounts for converter interactions and allows for impedance based control is proposed. The use of impedance monitoring via wideband impedance identification techniques provides interesting opportunities for the development of a robust and adaptive control strategy. Power converters within the system can be adaptively adjusted to track changes in the

system bus impedance, enacting revised control strategies with the intent of stabilizing the system as its dynamics evolve over time.

Secondly, the use of Power Hardware-in-the-Loop (PHIL) simulation is investigated for early system testing. As parts of the distribution system become available in hardware, it is desirable that they be evaluated under realistic system conditions. PHIL allows for advanced studies to be performed on system interactions by virtually coupling a real-time software simulation of electrical components to a physical piece of hardware through the use of an interfacing amplifier and appropriate control algorithm. Use of a PHIL test platform allows for system interaction studies to be performed early on in hardware development and provides an enhanced ability to study potential system-level problems and develop suitable solutions. Wideband impedance identification is utilized to complement the PHIL simulation, providing additional characterization of the hardware under test as well as critical information that is used to ensure stability and fidelity of the PHIL simulation test bed.

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$\hat{i}(s)$	Hat denotes small signal perturbed quantity
C	Capacitive impedance element
$d(t)$	Time varying duty cycle. Uppercase denotes steady-state quantity.
e	Base of natural logarithms
F	Unit of electrical capacitance in farads
f	Frequency in hertz
f_0	Resonant frequency of system in hertz
$G(s)$	Small-signal transfer function of linear time-invariant system
H	Unit of electrical inductance in henries
$i(t)$	Time varying current. Uppercase denotes steady-state quantity
j	Imaginary unit; $j^2 = -1$
K_i	Integral coefficient, PI controller
K_m	Allowable Impedance Region damping margin
K_p	Proportional coefficient, PI controller
L	Inductive impedance element
$M(\vartheta)$	Boundary of the Allowable Impedance Region
Ω	Unit of electrical resistance in ohms
π	Ratio of unit circle circumference to diameter, *pi*

Q	Quality factor
R	Resistive impedance element
s	Laplace complex variable
t	Time variable
T	Small-signal loop gain of linear time-invariant system
T_{adapt}	Total duration of adaptive impedance based control algorithm
T_{ID}	Total duration of wideband impedance identification procedure
$v(t)$	Time varying voltage. Uppercase denotes steady-state quantity
ω	Frequency in radians per second
ω_0	Resonant frequency of system in radians per second
Z	Generalized complex impedance
ζ	Damping factor of system resonance

List of Abbreviations

AC ..... Alternating Current

ADC ..... Analog-to-Digital Converter

AIR ..... Allowable Impedance Region

BKI ..... Intermediate Buck Converter

BKL ..... Load Buck Converter

BKS ..... Source Buck Converter

CPL ..... Constant Power Load

DAC ..... Digital-to-Analog Converter

DC ..... Direct Current

DFT ..... Discrete Fourier Transform

DIM ..... Damping Impedance Method

FB ..... Feedback

FFFB ..... Feed-Forward, Feedback

FFT ..... Fast Fourier Transform

FPGA ..... Field Programmable Gate Array

HUT ..... Hardware Under Test

IA ..... Interface Algorithm

ITM ..... Ideal Transformer Method

KCL ..... Kirchhoff's Current Law

KVL ..... Kirchhoff's Voltage Law

LCL ..... Inductor Capacitor Inductor

LHP ..... Left Half Plane

LSF ..... Least Squares Fitting

MLG ..... Minor Loop Gain

MVDC ..... Medium Voltage Direct Current

N ..... Normalized

OL ..... Open-Loop

OP ..... Operating Point

PBSC ..... Passivity Based Stability Criterion

PCD ..... Partial Circuit Duplication

PFF ..... Positive Feed-Forward

PHIL ..... Power Hardware-in-the-Loop

PI ..... Proportional-Integral

PRBS ..... Pseudo-Random Binary Sequence

PWM ..... Pulse Width Modulation

ROS ..... Rest of System

RLC ..... Resistor Capacitor Inductor

RHP ..... Right Half Plane

VSI ..... Voltage Source Inverter

ZOH ..... Zero Order Hold

CHAPTER 1

INTRODUCTION

1.1 STABILITY AND PERFORMANCE ISSUES IN MULTI-CONVERTER DC SYSTEMS

Advances in switching power electronic converter technology have brought about a resurgence of interest in the use of DC power distribution systems for a variety of applications [1]-[4]. A growing number of both industrial and military applications are transitioning from traditional AC distribution systems to power electronic enabled DC systems. Power electronic converters act as a flexible power interface, providing a means to interconnect sources and loads having very different electrical characteristics while providing significant performance and efficiency gains over traditional AC distribution methods. This capability is becoming an important consideration as power distribution systems are now frequently required to supply a more diverse set of electrical loads, allow for on-the-fly reconfiguration, and incorporate renewable and distributed generation sources [2].

DC power distribution systems have numerous advantages over the AC distribution systems of the past. Consider the notional power electronic enabled MVDC distribution system proposed for the US Navy's all-electric ship shown in Figure 1.1. This system consists of multiple MVDC buses powered by multiple generation sources and storage devices such as turbine generators, fuel cells, and batteries. Loads connected to the distribution system include propulsion motors, radar and weapons systems, and an

array of actuators and sensors. All sources and loads are interfaced to the DC buses via power electronic converters. A distribution system of this nature is of great interest for shipboard use for a number of reasons. The large, heavy, 60 Hz isolation transformers required in an equivalent AC distribution system are replaced by smaller, high frequency transformers operating at the power converter switching frequency. Power converters partially eliminate the need for circuit breaker based fault protection as the converters themselves now limit short circuit current through their control. All power sources supply the system with a DC voltage, thus eliminating the need for generator synchronization. The increased flexibility and controllability of the power electronic converters allows for increased survivability of the system and rapid reconfiguration in the event of component failures. The overall efficiency of this type of system is also improved as a result of a reduction in the number of power stages present between the source and load elements.

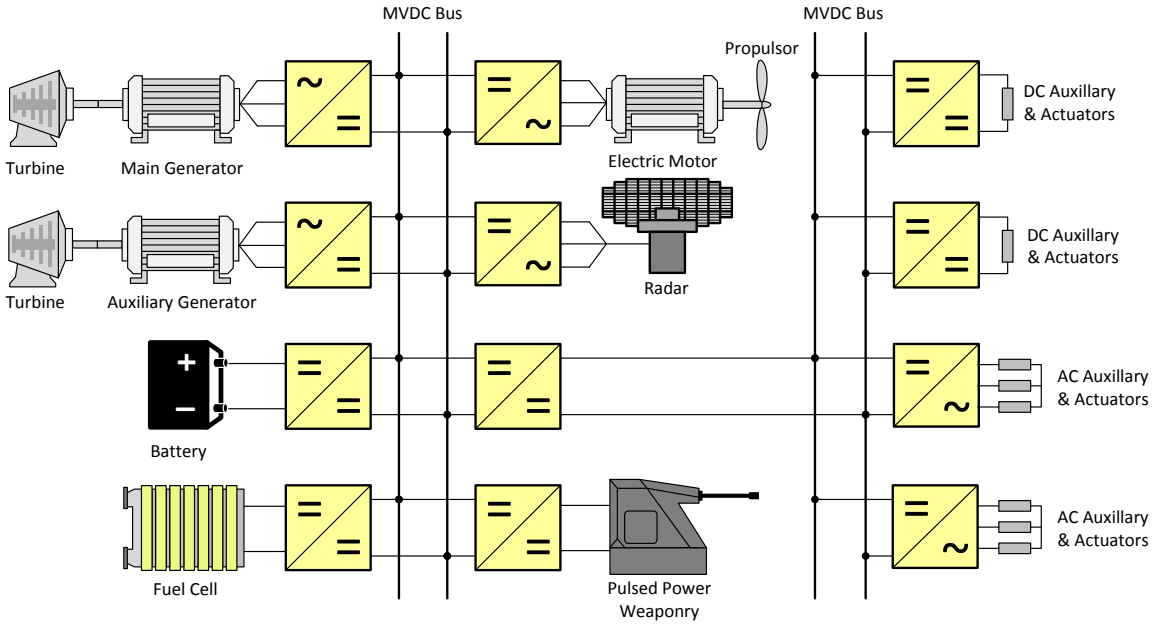


Figure 1.1. Proposed MVDC power distribution system for the US Navy's all-electric ship (simplified).

The notional power electronic enabled MVDC distribution system in Figure 1.1 is a complex and extensively interconnected multi-converter system consisting of multiple buses. As a result of interactions among the multiple power converters, system-level stability and dynamic performance issues are likely to arise [4]. These issues occur as a consequence of constant power loads (CPL) present throughout the distribution system. Feedback controlled power electronic converters behave as CPLs at their input terminals, presenting a negative incremental impedance that gives rise to system-level stability issues [5]. The cause of these stability and performance issues can also be viewed as the result of interactions among the various converter feedback loops coupled at the DC buses. In general, the design of this tightly coupled and complex system is difficult due to a lack of proper analysis and design tools.

To ensure that a MVDC distribution architecture such as that described above remains stable in operation and is robust in response to system variations, the designer needs an approach to control design that accounts for multi-converter interactions and that allows for adaptive control for survivability. This method should allow for the stability of a large, multi-converter system to be monitored in real-time using a design-oriented set of stability criteria, such that stabilizing controllers may be synthesized online to improve system performance. A large distribution system is likely to undergo system configuration changes over time, due in part to reconfiguration as a result of operating mode changes, periodic service and upgrades, and the introduction of additional sources and loads. Therefore, individual power converters within the system will see different input and output equivalent impedances over time.

Furthermore, a methodology to test and characterize power distribution system components under realistic operating conditions is desired. Such a methodology will provide engineers with the ability to analyze the overall system behavior in response to the connection of additional hardware. As power distribution components become available, they should be tested under the conditions they will experience when connected to the system. This will allow the designer to evaluate stability and performance issues arising due to the CPL effect or control interactions. This testing platform must be capable of replicating the dynamics of a switching converter based power system with both a high degree of stability and accuracy.

1.2 State of the Art

This section introduces the major conceptual components of this dissertation, including converter system modeling, impedance identification, impedance based control via a Passivity Based Stability Criterion (PBSC) and Positive Feed-Forward (PFF) control, and Power Hardware-in-the-Loop (PHIL) simulation techniques. Background information on each topic is provided and the state of the art in each area is discussed.

1.2.1 Multi-Converter System Modeling and Stability Analysis

A switching power converter is typically designed to exhibit good stability margins and achieve certain performance criteria when operating in the standalone case; the converter is fed by an ideal voltage source and supplies a simple resistive load. However, the notional MVDC distribution system consists of multiple interconnected power converters feeding other power converters, resulting in a more complex control scenario. Extensive work has been done in the past to model the low frequency dynamic behavior of switching power converters and interaction with passive input filter systems

[6]-[8]. However, analysis of the small-signal behavior of larger systems requires a converter modeling approach that allows for flexibility in the connection of a variety of sources and load subsystem impedances. A two-port model is used in [9] to represent different power units based on the well-known small-signal models for basic switching converters, which are then combined to obtain an equivalent representation of a more complex system. Typically, small-signal models are derived using a resistor as a converter load. In practice, however, it is often appropriate to treat the load as an external element, requiring the usage of unterminated models. This technique had previously been applied to analyze input filter interactions [6], and to characterize the small-signal behavior of so-called "black-box" DC-DC converters in [10].

Several stability analysis techniques have been previously proposed in the literature for the stability evaluation of coupled converter systems. One approach to address system-level stability analysis is to separate the system into a source and load subsystem at an arbitrary interface, Figure 1.2. The transfer function relating the system input to output is as follows.

$$\frac{V_{out}}{V_{in}} = G_S G_L \frac{Z_{in}}{Z_{in} + Z_{out}} = G_S G_L \frac{1}{1 + T_{MLG}} \tag{1.1}$$

where the so-called minor loop gain (MLG) T_{MLG} is defined in (1.2).

$$T_{MLG} = \frac{Z_{out}}{Z_{in}} \tag{1.2}$$

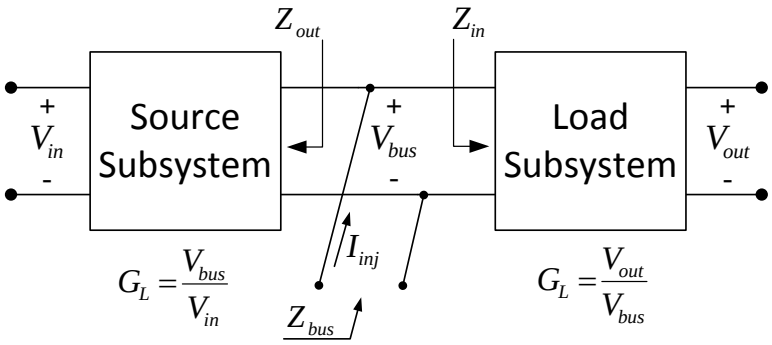


Figure 1.2. Conceptual diagram of equivalent interacting source and load subsystem.

The source and load subsystems depicted in Figure 1.2 are assumed to be stand-alone stable such that the MLG determines the stability of the coupled system. A number of stability criteria based on the MLG have been proposed such as the Middlebrook Criteria [11] and its extensions the Gain and Phase Margin Criterion [12]-[13], the Opposing Argument Criterion [14]-[16], and the Energy Source Analysis Consortium (ESAC) Criterion [17]-[18] and its extension, the Root Exponential Stability Criterion (RESC) [19]. Each of these criteria provides a sufficient condition for system stability by defining various forbidden regions in the *s*-plane for the Nyquist contour of the MLG. It has been noted in the literature that these criteria often lead to conservative system designs, are highly dependent on component grouping and power flow direction, and do not lead to straightforward stabilizing controller design formulations.

To alleviate these concerns, the Passivity Based Stability Criterion (PBSC) has been recently proposed and applied to the stability analysis of interconnected switching converter systems consisting of a single-bus [19]-[23]. It has been shown that information regarding the stability of the system may be obtained by evaluating the impedance at the system bus connection.

Consider again the equivalent interacting source and load system in Figure 1.2. When observed from the bus port, the system has a bus impedance $Z_{bus}(s) = V_{bus}(s)/I_{inj}(s)$, where $I_{inj}(s)$ is an injection current supplied by an external device to perturb the bus. The bus impedance of the network is the parallel combination of the source subsystem output impedance Z_{out} and load subsystem input impedance Z_{in}. If the bus impedance is determined to be passive, the system is stable [24].

Previous work on the PBSC has focused on applying the criterion to single-bus systems consisting of a source converter or input filter and load converter only [20]-[23]. The dynamic closed-loop behavior of these converters was derived using standard resistively terminated converter models, thus limiting the analysis to a single-bus. An extension to the more general multi-bus system case consisting of multiple power converters is necessary. Furthermore, the PBSC provides only information regarding the relative stability of an interacting coupled system. No information regarding dynamic performance is made directly available. Therefore, it is possible that a system may be determined to be passive and, therefore, stable but still exhibit oscillatory or otherwise undesirable behavior. The development of an additional level of analysis to complement the PBSC that indicates the dynamic system behavior is necessary and will aid in the design of suitable stabilizing controllers.

In this work, unterminated two-port small-signal switching converter models are used to expand the application of the PBSC to the multi-bus distribution system scenario. Unterminated converter models allow for the flexible interconnection of distribution system power conversion hardware such that the analytic bus impedances may be easily extracted for evaluation via the PBSC. Additionally, an analysis technique to complement

the PBSC, called the Allowable Impedance Region (AIR), is developed to provide information regarding the dynamic performance of the system. This supplementary level of analysis aids in the design of suitable controllers that serve to damp the system buses.

1.2.2 Positive Feed-Forward Control

The PBSC has the advantage of being a very design-oriented criterion in comparison with previous methods of determining system stability. The criterion lends itself to the design of virtual damping impedances that can be actively introduced in parallel with the existing bus impedance, effectively modifying the system bus impedance such that the overall bus impedance appears passive. In particular, a recently proposed control strategy, called Positive Feed-Forward (PFF) control, can be used to actively insert virtual damping impedances at the load side of the system bus [23]. In this approach, the switching converter employs a feedback (FB) loop to ensure the regulation of its own output and a feed-forward loop for imposing the passivity condition on the overall system bus impedance.

The PFF control technique provides a method for controlling the converter input impedance by effectively introducing an active damping impedance in parallel with the already existing converter input impedance with the goal of stabilizing the system. Given knowledge of the system bus impedance, a PFF controller may be designed to introduce an appropriate damping impedance such that the PBSC is satisfied, resulting in a stable and performing system.

In [22]-[23] it was recognized that the PBSC is typically violated around the resonant frequency of a system bus impedance. This realization has helped guide the formulation of appropriate virtual damping impedances for implementation via PFF

control using iterative methods. However, the damping impedance design remains difficult since the PBSC does not directly provide information regarding the system performance. An additional tool for analyzing the system bus impedance dynamics is needed to better facilitate the design of the virtual damping impedance and PFF controller.

The Allowable Impedance Region analysis proposed in this dissertation facilitates PFF control design by providing information regarding the relative damping of the system bus impedance. An appropriate virtual damping impedance is easily computed using a simple set of design equations to ensure that the bus impedance Nyquist contour is constrained within a specified region of the *s*-plane that guarantees a minimum level of damping. The proposed Allowable Impedance Region technique coupled with the simplified PFF control design is shown to be effective in providing good stability for both single-bus and multi-bus MVDC systems in simulation and experiment.

1.2.3 WIDEBAND IMPEDANCE IDENTIFICATION

The stability and performance of a power electronic enabled DC distribution system are predicated on appropriate converter control based on accurate knowledge of the system configuration and parameters. As the power system dynamics change over time due to cycling of generation sources, load changes, and even converter failure, the stability of the distribution system may be degraded. This work makes use of system identification techniques, which have been used in the past to estimate various converter transfer functions and system-level impedances, for online measurement of system impedances [25]-[30].

The measurement of impedance requires a voltage or current perturbation at the power interface and measurements of both voltage and current. Using a cross-correlation based technique (detailed in Appendix A), non-parametric estimations of the converter control-to-voltage, $G_{vd}(s)$, and control-to-current, $G_{id}(s)$, transfer functions may be constructed [25]. The equivalent Thévenin impedance at the interface from where these measurements are obtained may then be constructed as the ratio of these two transfer functions. This construction is shown in (1.1) and (1.2).

$$Z(s) \equiv \frac{\hat{v}[s]}{\hat{i}[s]} = \frac{\left(\frac{\hat{v}(s)}{\hat{d}(s)}\right)}{\left(\frac{\hat{i}(s)}{\hat{d}(s)}\right)} = \frac{G_{vd}(s)}{G_{id}(s)} \tag{1.1}$$

$$G_{vd}(s) \equiv \frac{\hat{v}(s)}{\hat{d}(s)}, \quad G_{id}(s) \equiv \frac{\hat{i}(s)}{\hat{d}(s)} \tag{1.2}$$

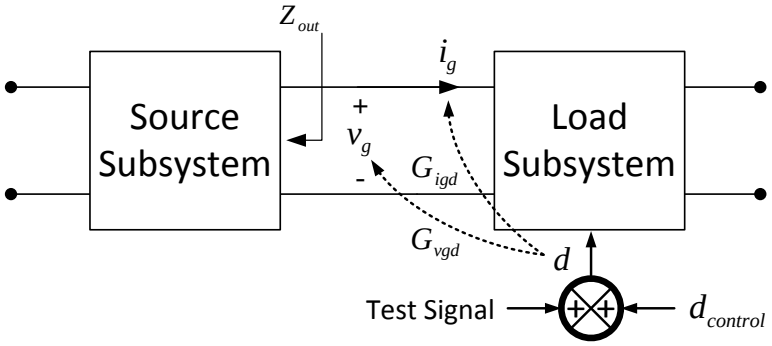


Figure 1.3. Conceptual diagram of source subsystem impedance measurement.

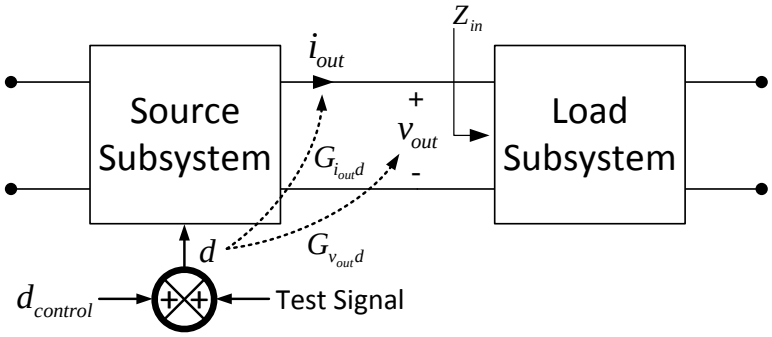


Figure 1.4. Conceptual diagram of load subsystem impedance measurement.

Wideband identification of a source subsystem may be accomplished by the introduction of a pseudo-random binary sequence (PRBS) test signal into the duty cycle command of an interfaced switching converter. This causes a small variation in the converter's input voltage and input current, which are then sampled as shown in Figure 1.3. $Z_{out}(s)$ is then constructed according to (1.1). Similarly, identification of a load subsystem, $Z_{in}(s)$, requires introduction of a perturbation and sampling of the converter output voltage and output current, as shown in Figure 1.4. An example impedance construction is shown in Figure 1.5. Note that in the logarithmic scale, the impedance may be constructed by simply taking the difference of the control-to-voltage and control-to-current transfer functions.

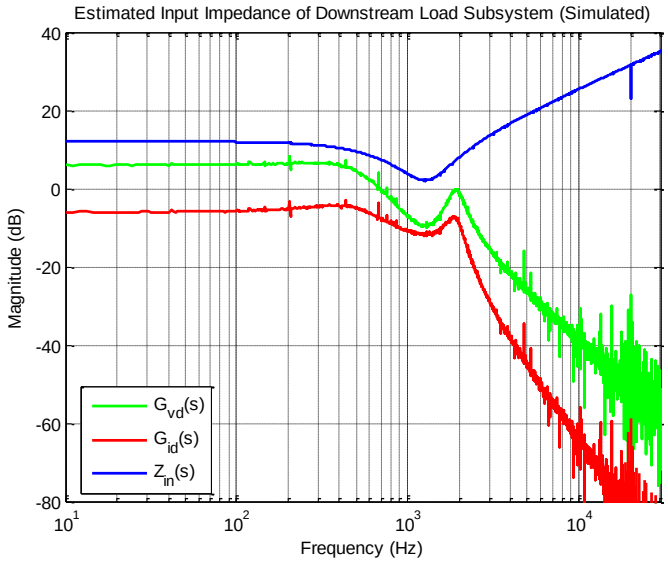


Figure 1.5. Example wideband impedance construction as the difference of control-to-voltage and control-to-current converter transfer functions.

As described, the impedance identification procedure is an online measurement that can be performed by a switching converter already existing in a power distribution system. Therefore, the technique requires no additional hardware and can occur in real-

time during normal system operation without contributing significant noise. It is desirable that the introduced perturbation have low amplitude such that the system operating point is not disturbed. Note that the measured impedance is a small-signal linearized quantity. The PRBS technique makes use of a wideband excitation, such that all frequency components of interest are excited at once. This method is therefore less likely to excite resonances in the system that may result in significant system operating point variations.

The online nature of this technique gives rise to a variety of useful capabilities regarding system monitoring and control adaptation. Usage of this technique has been reported in the literature. Impedance identification techniques were applied in [26] to allow for the estimation of the MLG of an interacting source subsystem and load subsystem formed by two interconnected power converters. The source converter was used to measure the input impedance of the load converter while the load converter was used to measure the output impedance of the source converter. This information provides the capability for a supervisory or agent based control architecture to enact adaptive converter coordination and monitor the system stability. Reference [26]-[28] provides improvements and simplifications to the correlation based system identification techniques and investigates a number of unique applications including adaptive digital deadbeat current and voltage control, active damping of LCL filters, and battery health monitoring. Extensions of the existing impedance identification techniques were also made to allow for three phase system identification techniques in [28]-[29]. However, these applications primarily focus on individual converters and do not consider the stability of interconnected systems.

Other online techniques to derive impedance information from distributed power systems have also been presented. In [31] and [32], the usage of separate, dedicated excitation sources was explored to allow for the measurement of the MLG. These excitation sources made use of an injection transformer to apply a small perturbation current into the DC bus between systems. Measurement of the bus voltage and current response allows for the construction of the desired quantity. In [33] the input and output impedances of switching converters were measured using additional, external perturbation sources. Several injection source topologies and configurations were also investigated. However, these works do not benefit from the usage of an existing converter to perform impedance identification functions, relying instead on external injection sources. Furthermore, the usage of injection transformers to achieve the required decoupling limits the capabilities of the proposed methodologies due to transformer bandwidth requirements and the need to withstand high DC bias currents in the case of series injection.

Utilization of switching converter based wideband impedance identification techniques is a common theme throughout this dissertation and is applied in several areas related to converter system control. The technique is utilized to construct estimations of single-bus and multi-bus MVDC converter system bus impedances, which are then evaluated for passivity in a determinate of overall system stability. Wideband impedance identification is also leveraged in PHIL simulation to improve the stability of the simulation platform and provide additional characterization of the device under test.

1.2.4 POWER HARDWARE-IN-THE-LOOP

Modern simulation tools and advancements in real-time computing have resulted in an increased interest in Hardware-in-the-Loop simulation methods for the development and testing of electrical components and systems [34]-[36]. Real-time simulation technology has been successfully used to evaluate the performance of power device controllers and protection apparatus using controller hardware-in-the-loop (CHIL) techniques, in which a physical electronic controller is interfaced via analog-to-digital converters (ADC) and digital-to-analog converters (DAC) to a real-time software simulation of the hardware it is destined to control. These CHIL simulations, pictured in Figure 1.6, commonly operate at low voltage signal levels and low power such that standard ADCs and DACs provide a sufficient means of interfacing the controller hardware under test to the real-time simulation of the power hardware system. CHIL simulation provides a useful tool for rapidly evaluating the performance of a novel device controller without requiring that the physical hardware system be present. This capability allows for convenient and safe testing of systems that may be physically large, hazardous, or otherwise impractical to have installed in a laboratory test bed.

An extension of this simulation technology is the emerging power hardware-in-the-loop (PHIL) simulation methodology, where a dynamic electrical system is separated into a hardware portion and software portion. Physical hardware under test (HUT) is coupled to a real-time computer simulation of the rest of the system (ROS) through the use of an appropriate interface algorithm (IA) allowing for the virtual exchange of power, as shown in Figure 1.7. Strategic separation of a power system is advantageous in the reduction of prototype development and validation costs, lessening of physical space requirements, and increased safety of laboratory personnel. Additionally, this technology

allows for the controlled reproduction of fault conditions or other contingency scenarios in which the simulated ROS would sustain serious damage or create a hazardous environment if it were an actual assembly of physical hardware components.

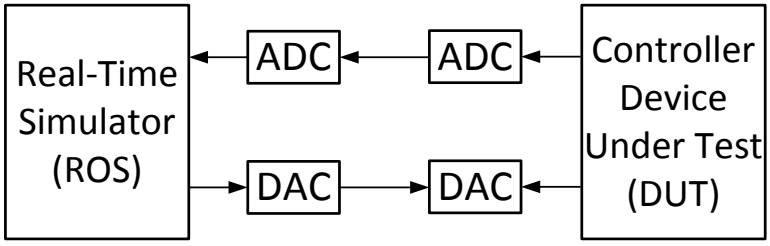


Figure 1.6. General CHIL simulation scheme including real-time software simulator, low-level signal interfacing, and controller device under test.

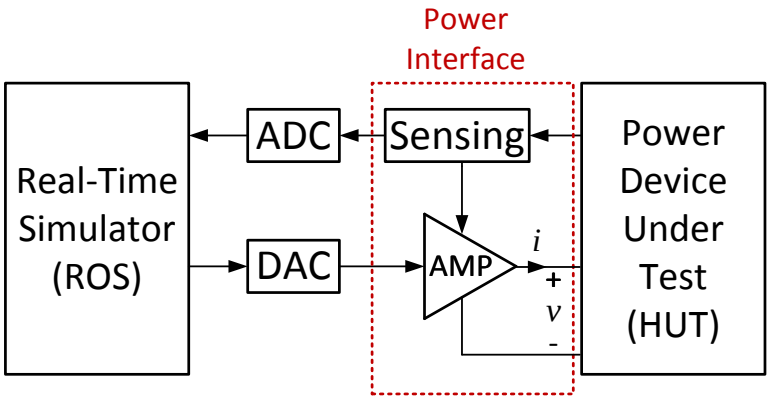


Figure 1.7. General PHIL simulation scheme including real-time software simulator, low-level signal interfacing, power interface, and the power device under test.

Although a promising simulation method, PHIL is not without technical issues. Due to the need for the exchange of power at the interface between software and hardware, a high-precision and wide power bandwidth amplifier is required. The additional power amplification equipment at the interface increases the complexity of the PHIL test platform and error arising from various non-idealities introduced at the interface may compromise the stability of the system. Therefore, the PHIL test platform must be properly designed to ensure both the overall system stability and simulation accuracy.

A variety of different IAs [34]-[36] have been proposed in the literature to model the behavior of the power interface and address accuracy and stability issues that arise. Reference [34] discusses the challenges associated with the PHIL power interface stability and provides an overview of several different IAs and the requirements to ensure their stability. The performance of these algorithms is investigated in simulation and experiment for simple, passive PHIL simulation scenarios. In [35], the author proposes combining two existing, complementary IAs to enhance the interface stability. The IA is a hybrid of the Voltage-Type Ideal Transformer Method (ITM) and Current-Type ITM: instability is avoided by switching between the V-Type ITM and the I-Type ITM by monitoring the relation of the HUT impedance to the ROS impedance and selecting the stable IA at all times.

Several authors [35]-[38] have also proposed methods to adaptively control the power interface using a unique IA called the Damping Impedance Method (DIM), the details of which are given in Section 3. By calculating the average impedance of the HUT based on the RMS values of the interface voltage and current, a simulated damping impedance located in the software simulation may be modified, thus ensuring absolute system stability. This method only provides the impedance of the HUT at a single frequency, i.e., the quiescent AC operating frequency of the power interface. In [37], this technique is improved by including a measurement of the phase shift between the voltage and current measurements such that the resistance and reactance may be extracted separately. This technique is effective in improving the impedance estimation as long as the reactive element of the HUT has a significant measurable impact on the impedance at the quiescent operating frequency. However, the actual impedance is typically frequency-

dependent and the estimate so obtained at one frequency may not be accurate at the natural system frequency, leading to reduced damping and potential instability. Furthermore, these methods for updating the value of the simulated damping impedance are only appropriate for AC PHIL interfaces since reactive impedance information cannot be ascertained for a DC interface for obvious reasons.

To address PHIL simulation stability issues, this work proposes augmenting the DIM IA with additional impedance identification capabilities to provide a wideband estimation of the HUT. The simulated damping impedance within the IA is then adjusted to reflect the results of the impedance estimation, significantly improving the stability of the PHIL system. This technique has the added benefit of being an additional tool with which the HUT may be characterized. An impedance based approach to ensuring PHIL simulation accuracy is also introduced. This analysis considers the output impedance of the interface itself relative to that of the simulated ROS in imposing conditions that ensure good PHIL accuracy.

1.3 Contents of Dissertation

1.3.1 Research Objectives

The objective of this research is to apply impedance identification techniques to ease and improve the control design of multi-converter DC distribution systems and to improve the capabilities of PHIL to allow for early stage testing of power equipment.

Stability analysis and control design for multi-converter DC distributions is accomplished by application of the PBSC coupled with PFF control. This work extends the application of the PBSC and PFF control design to converter systems consisting of multiple bus connections by employing unterminated two-port small-signal converter

models. The use of unterminated models allows for the development of a system that fully incorporates the dynamics of multiple interacting converter source and load subsystems. Information obtained from this modeling technique allows for the construction, as a function of the overall system operating point, of the distribution bus impedances, which are then evaluated for the condition of passivity in a determination of overall system stability. A technique for evaluating the dynamic performance of the system and a simplified damping impedance and PFF control design methodology are also proposed.

Online measurement of the system bus impedances via impedance identification allows for targeted and adaptive control of multi-converter systems. This work experimentally demonstrates the use of wideband impedance identification to collect estimations of the system bus impedances of a scaled MVDC system. The experimental impedance models are subsequently used in the design of appropriate damping impedances to ensure that the passivity condition is met and that the system will exhibit good dynamic performance.

PHIL simulation capabilities are expanded through the design and implementation of a highly stable and accurate PHIL testing platform. Methods to evaluate the system stability and accuracy based on the impedances of the simulated system and hardware under test are presented. Details regarding the interface amplifier design, interfacing algorithm, and real-time simulation platform are provided. Wideband impedance identification techniques are incorporated into the interface algorithm controlling the virtual exchange of power between software simulation and physical hardware. This

additional capability, implemented via the interface amplifier, improves the stability of the interface and allows for additional characterization of the hardware under test.

1.3.2 CONTRIBUTIONS

In summary, the contributions of this dissertation to the state of the art are as follows:

- Development of unterminated two-port small-signal switching converter models for simple construction of multi-converter multi-bus system models
- Extension of the PBSC to the multi-bus case
- Design of PFF controller for robust stability of multi-bus systems
- Definition of an Allowable Impedance Region to ensure good damping of passive bus impedances
- Improved and simplified design of PFF controller based on Allowable Impedance Region analysis
- Adaptive PFF control design algorithm for single and multi-bus MVDC distribution systems via online impedance identification and PBSC coupled with PFF control
- Damping Impedance Method interface algorithm coupled with wideband impedance identification techniques for enhanced stability of PHIL test platform and additional hardware under test characterization
- Impedance based design constraints for interface amplifier design and PHIL test platform accuracy analysis
- PHIL simulation of notional multi-converter system and control design synthesis via PBSC and PFF control

1.3.3 STRUCTURE OF DISSERTATION

This dissertation is organized as follows. In Chapter 2, an unterminated small-signal model is developed for a buck type switching converter and its negative feedback and positive feed-forward control system. The model development from open-loop unterminated to closed-loop unterminated is detailed in full.

The PBSC and PFF control design is discussed in Chapter 3, along with the newly proposed Allowable Impedance Region analysis and simplified damping impedance and PFF control design. Analytical design results are given for a scaled, notional multi-bus MVDC distribution system consisting of four interconnected switching converters. Two scenarios are investigated that require targeted application of PFF control in order to ensure good dynamic performance. In Chapter 4, simulated and experimental results are presented for the example system.

Chapter 5 presents enhancements to PHIL simulation platform stability and accuracy via application of wideband impedance identification. These improvements are validated with illustrative simulation results to demonstrate the efficacy of the proposed techniques. Simulation results of a PHIL test platform used to evaluate the stability and performance of an MVDC system are provided in Chapter 6. An additional piece of converter hardware is added to the system via PHIL simulation. Characterization of the simulated system behavior is accomplished using the PBSC and an appropriate PFF controller is designed to improve the system performance. Conclusions and future work are given in Chapter 7.

CHAPTER 2

MULTI-CONVERTER SYSTEM MODELING

In this chapter, a methodology for constructing unterminated switching converter models based on hybrid g-parameter two-port models is presented. These models are left unterminated to allow for flexibility in the construction of larger system models in which multiple two-port models are interconnected in either cascade, parallel, or mixed configurations. An example four-converter system is modeled at the end of the chapter to demonstrate the proposed technique.

2.1 RESISTIVELY TERMINATED MODELING

The design of a switching converter and its requisite control system for output regulation necessitate the development of a dynamic model that relates how the various input and output quantities interact. Development of this type of dynamic model is well understood [5]. Typically, the circuit is modeled under ideal conditions to simplify the derivation; the converter is supplied by an ideal voltage source and terminated in a resistive load, as in the example shown for a buck converter in Figure 2.1. The two switches are operated in complementary fashion, with the duty cycle d representing the percent for which the upper switch is closed during a switching period of length T_s. Consequently, the converter system is time-varying in nature and the averaged equivalent circuit describing the behavior over a switching period is nonlinear. Therefore, the averaged differential equations that represent the behavior of the circuit's reactive

components are linearized to allow for the derivation of the small-signal AC converter model. Transfer functions developed from the small-signal model provide insight into the basic behavior and properties of the system and are instrumental in the development of the converter control algorithm and in ensuring stability.

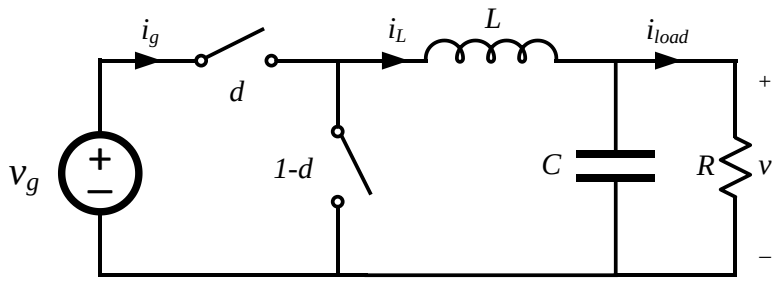


Figure 2.1. Idealized model of buck switching converter with ideal voltage source and resistive load.

For the buck switching converter of Figure 2.1, the basic equations, averaged over one switching period of length T_s, representing the DC and low frequency AC behavior of the inductor current, i_L, capacitor voltage, v, and input current, i_g, are given below in (2.1)-(2.3).

$$L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = d(t)\langle V_g(t)\rangle_{T_s} - \langle V(t)\rangle_{T_s} \tag{2.1}$$

$$C\frac{d\langle v(t)\rangle_{T_s}}{dt} = \langle i_L(t)\rangle_{T_s} - \frac{\langle V(t)\rangle_{T_s}}{R} \tag{2.2}$$

$$\langle i_g(t)\rangle_{T_s} = d(t)\langle i_L(t)\rangle_{T_s} \tag{2.3}$$

The small-signal AC model of the circuit in Figure 2.1 is developed by superimposing small AC variations about the averaged quiescent operating point of the buck converter:

$$\langle i_L(t)\rangle_{T_s} = I_L + \hat{i}_L(t)$$
$$\langle v(t)\rangle_{T_s} = V + \hat{v}(t)$$
$$\langle v_g(t)\rangle_{T_s} = V_g + \hat{v}_g(t) \tag{2.4}$$
$$\langle i_g(t)\rangle_{T_s} = I_g + \hat{i}_g(t)$$
$$d(t) = D + \hat{d}(t)$$

The resulting equations following insertion of (2.4) into (2.1)-(2.3) are linearized by elimination of the DC terms and higher order nonlinear AC terms, resulting in the desired small-signal linearized equations that describe the buck switching converter behavior.

$$L\frac{d\hat{i}_L(t)}{dt} = V_g\hat{d} + D\hat{v}_g - \hat{v} \tag{2.5}$$

$$C\frac{d\hat{v}(t)}{dt} = \hat{i}_L - \frac{\hat{v}}{R} \tag{2.6}$$

$$\hat{i}_g = I_L\hat{d} + D\hat{i}_L \tag{2.7}$$

By Laplace transformation of (2.5)-(2.7), the small-signal transfer functions relating various input and output quantities of the switching converter can be derived. The complete set of transfer functions, as well as the input and output impedances, for the idealized resistively terminated buck converter is given in (2.8)-(2.16).

$$Y_{in} = \left.\frac{\hat{i}_g}{\hat{v}_g}\right|_{\hat{i}_{load}=\hat{d}=0} = \frac{1}{Z_{in}} = \frac{D^2}{R}\frac{sCR+1}{s^2LC + s\frac{L}{R}+1} \tag{2.8}$$

$$G_{igio} = \left.\frac{\hat{i}_g}{\hat{i}_{load}}\right|_{\hat{v}_g=\hat{d}=0} = D\frac{1}{s^2LC + s\frac{L}{R}+1} \tag{2.9}$$

$$G_{igd} = \frac{\hat{i}_g}{\hat{d}}\bigg|_{\hat{v}_g=\hat{i}_{load}=0} = \frac{V_g D}{R}\left(1+\frac{sCR+1}{s^2LC+s\frac{L}{R}+1}\right) \tag{2.10}$$

$$G_{vg} = \frac{\hat{v}}{\hat{v}_g}\bigg|_{\hat{i}_{load}=\hat{d}=0} = D\frac{1}{s^2LC+s\frac{L}{R}+1} \tag{2.11}$$

$$Z_{out} = \frac{-\hat{v}}{\hat{i}_{load}}\bigg|_{\hat{v}_g=\hat{d}=0} = \frac{sL}{s^2LC+s\frac{L}{R}+1} \tag{2.12}$$

$$G_{vd} = \frac{\hat{v}}{\hat{d}}\bigg|_{\hat{v}_g=\hat{i}_{load}=0} = V_g\frac{1}{s^2LC+s\frac{L}{R}+1} \tag{2.13}$$

$$G_{ilg} = \frac{\hat{i}_L}{\hat{v}_g}\bigg|_{\hat{i}_{load}=\hat{d}=0} = \frac{D}{R}\frac{sCR+1}{s^2LC+s\frac{L}{R}+1} \tag{2.14}$$

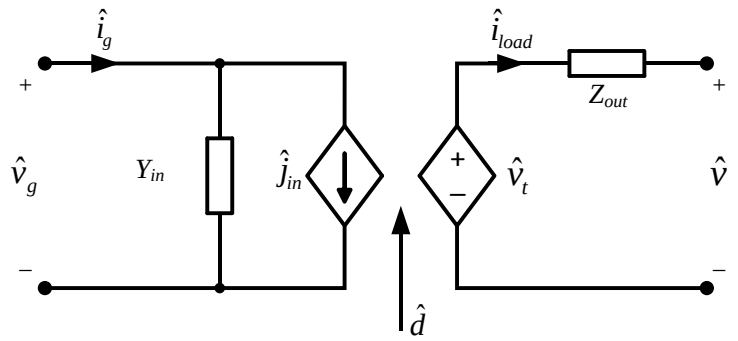
$$G_{ilio} = \frac{\hat{i}_L}{\hat{i}_{load}}\bigg|_{\hat{v}_g=\hat{d}=0} = \frac{1}{s^2LC+s\frac{L}{R}+1} \tag{2.15}$$

$$G_{ild} = \frac{\hat{i}_{L:}}{\hat{d}}\bigg|_{\hat{v}_g=\hat{i}_{load}=0} = \frac{V_g}{R}\frac{sCR+1}{s^2LC+s\frac{L}{R}+1} \tag{2.16}$$

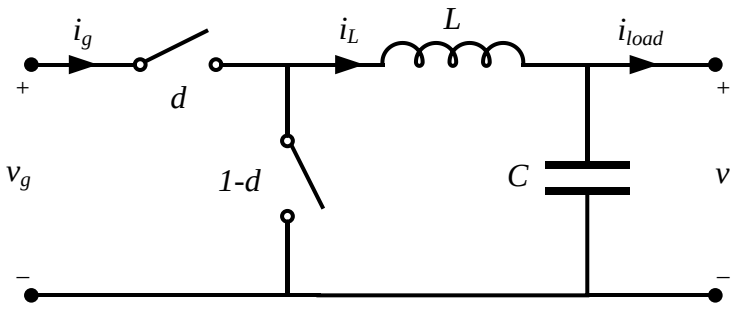
The preceding resistively terminated transfer functions may be used in the design of compensators to achieve certain control objectives and to evaluate the system for stability using a variety of analysis methods. However, it is important to note that the results of any control design and stability analysis are only applicable for the converter at the operating point which was determined at the beginning of the modeling procedure via termination of the output in a resistive load [5]. The behavior of the converter when terminated with a different type of load will differ from the model described by (2.8)-(2.16) and may result in poor performance or even instability. Additionally, interactions

of the converter with a non-ideal voltage source are not represented by the above modeling technique, leading to uncertainty when the converter is implemented in a system where the source impedance is finite [39]. Power electronics are becoming more commonplace in applications where multiple converters are interfaced at common nodes. In these types of systems, converters may feed other converters such that the resistive termination and ideal source simplifications made above are no longer appropriate and may result in inaccurate analysis and system design. An approach to provide flexible converter models with no assumptions made about the input and output terminations is presented in the following section.

2.2 UNTERMINATED TWO-PORT SMALL-SIGNAL MODELING



(a)



(b)

Figure 2.2. Model structure of (a) unterminated two-port hybrid g-parameter model and (b) buck switching converter.

The structure of the model, shown in Figure 2.2(a), is based on an unterminated two-port network of inverse hybrid parameters, or g-parameters. The small-signal model is derived for the unterminated buck converter of Figure 2.2(b). Quantities in capital letter, such as duty cycle D, input voltage V_g, and current I_{OP} represent steady-state operating point values whereas hatted quantities represent small-signal variations around the steady-state operating point where linearization is performed. The input variables of the model are the input voltage $\hat{v}_g$, load current $\hat{i}_{load}$, and duty cycle $\hat{d}$. The output variables are the output voltage $\hat{v}$, and input current $\hat{i}_g$.

In the two-port representation, these are the minimum required input and output variables that allow for interconnection with external source and load subsystems. However, for a complete representation of a switching converter, an additional output variable not depicted in Figure 2.2(a) must also be considered: the small-signal inductor current, $\hat{i}_L$. This modeling approach assumes that the converter has been linearized around an arbitrary operating point, such that its primary input and output dynamics may now be accurately represented by six transfer functions or hybrid g-parameters (2.17) where the Laplace variable s has been omitted for brevity. An additional three transfer functions are included to model the small-signal inductor current, $\hat{i}_L$. The required unterminated g-parameters for the standard buck converter of Figure 2.2(b) are easily derived from the terminated transfer functions given in (2.8)-(2.16) using the relationship of (2.18). The resulting unterminated g-parameters for the buck switching converter are given in (2.19)-(2.27). All converter g-parameters mentioned throughout the remainder of this dissertation are unterminated unless noted otherwise.

$$\begin{bmatrix} \hat{i}_g \\ \hat{v} \\ \hat{i}_L \end{bmatrix} = \begin{bmatrix} Y_{in} & G_{igio} & G_{igd} \\ G_{vg} & -Z_{out} & G_{vd} \\ G_{ilg} & G_{ilio} & G_{ild} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load} \\ \hat{d} \end{bmatrix} \tag{2.17}$$

$$G_{unt} = \lim_{R \to \infty} G_{term} \tag{2.18}$$

$$Y_{in} = D^2 \frac{sC}{s^2 LC + 1} \tag{2.19}$$

$$G_{igio} = D \frac{1}{s^2 LC + 1} \tag{2.20}$$

$$G_{igd} = \left(I_{OP} + V_g D \frac{sC}{s^2 LC + 1} \right) \Bigg|_{I_{OP}=0} \tag{2.21}$$

$$G_{vg} = D \frac{1}{s^2 LC + 1} \tag{2.22}$$

$$Z_{out} = \frac{sL}{s^2 LC + 1} \tag{2.23}$$

$$G_{vd} = V_g \frac{1}{s^2 LC + 1} \tag{2.24}$$

$$G_{ilg} = D \frac{sC}{s^2 LC + 1} \tag{2.25}$$

$$G_{ilio} = \frac{1}{s^2 LC + 1} \tag{2.26}$$

$$G_{ild} = V_g \frac{sC}{s^2 LC + 1} \tag{2.27}$$

Note the inclusion of the arbitrary operating point term, I_{OP}, in the unterminated control-to-input-current transfer function G_{igd} (2.21). This is a required addition to account for the nonlinear relationship between the converter input current, load current, and duty cycle. When placed into a larger system, this value must be updated to reflect the system operating point prior to the development of the closed-loop unterminated model.

Switching converters commonly employ negative feedback to achieve a desired output behavior. In this work, a multi-loop negative feedback control structure is used; an inner loop is designed to regulate the inductor current and an outer loop is designed to regulate the output voltage. In addition to negative feedback output regulation, a positive feed-forward controller may also be incorporated to regulate the input [22].

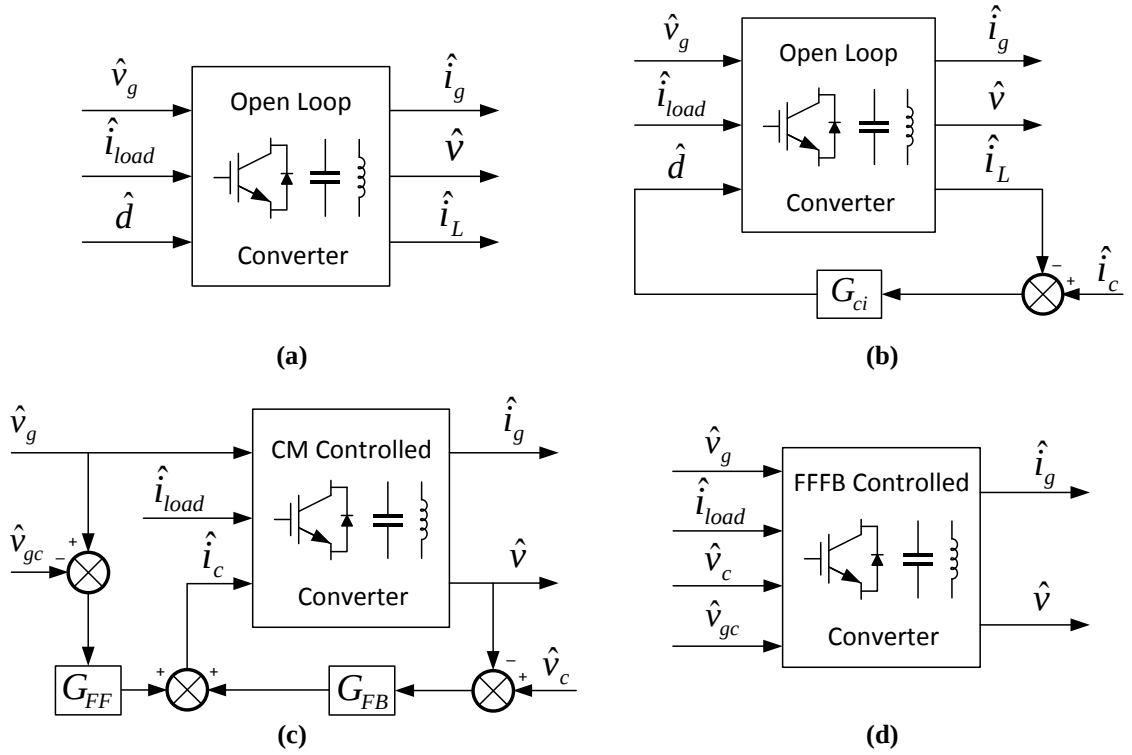


Figure 2.3. Generalized switching converter block diagram operating (a) open-loop, (b) under inductor current mode (CM) control, (c) with feedback output voltage and feed-forward input voltage control (FFFB), and (d) complete closed-loop converter.

Consider the block diagram representation of a switching converter shown in Figure 2.3(a). A converter having an inner inductor current control loop has the structure shown in Figure 2.3(b). Given an inductor current compensator G_{ci}, the inductor current feedback loop gain is $T_{CM} = G_{ci}G_{ild}$. The converter model under inductor current feedback control is of the form shown in (2.28). Note that the control input variable is

now $\hat{i}_c$, the inductor current reference. The unterminated g-parameters for the converter operating under current mode control are given in (2.29)-(2.37).

$$\begin{bmatrix} \hat{i}_g \\ \hat{v} \\ \hat{i}_L \end{bmatrix} = \begin{bmatrix} Y_{in-CM} & G_{igio-CM} & G_{igc-CM} \\ G_{vg-CM} & -Z_{out-CM} & G_{vc-CM} \\ G_{ilg-CM} & G_{ilio-CM} & G_{ilc-CM} \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load} \\ \hat{i}_c \end{bmatrix} \tag{2.28}$$

$$Y_{in-CM} = Y_{in} - \frac{G_{igd} G_{i\lg}}{G_{ild}} \frac{T_{CM}}{1+T_{CM}} \tag{2.29}$$

$$G_{igio-CM} = G_{igio} - \frac{G_{igd} G_{i\lg}}{G_{ild}} \frac{T_{CM}}{1+T_{CM}} \tag{2.30}$$

$$G_{igc-CM} = \frac{G_{igd}}{G_{ild}} \frac{T_{CM}}{1+T_{CM}} \tag{2.31}$$

$$G_{vg-CM} = G_{vg} - \frac{G_{vd} G_{i\lg}}{G_{ild}} \frac{T_{CM}}{1+T_{CM}} \tag{2.32}$$

$$Z_{out-CM} = Z_{out} - \frac{G_{vd} G_{ilio}}{G_{ild}} \frac{T_{CM}}{1+T_{CM}} \tag{2.33}$$

$$G_{vc-CM} = \frac{G_{vd}}{G_{ild}} \frac{T_{CM}}{1+T_{CM}} \tag{2.34}$$

$$G_{ilg-CM} = \frac{G_{i\lg}}{1+T_{CM}} \tag{2.35}$$

$$G_{ilio-CM} = \frac{G_{ilio}}{1+T_{CM}} \tag{2.36}$$

$$G_{ilc-CM} = \frac{T_{CM}}{1+T_{CM}} \tag{2.37}$$

Finally, the converter model with a negative feedback control to regulate the output voltage and a positive feed-forward control to regulate the input voltage may be represented as shown in the block diagram of Figure 2.3(c). Given an output voltage

compensator G_{FB}, the output voltage feedback loop gain is $T_{FB} = G_{FB}G_{vc\text{-}CM}$. Given an input voltage compensator G_{FF}, the input voltage feed-forward gain is $T_{FF} = G_{FF}G_{igc\text{-}CM}$. The resulting unterminated converter model under feedback and feed-forward (FFFB) control is given in (2.38). The final closed-loop, unterminated g-parameter expressions are given in (2.39)-(2.46). Note that the physical model outputs now consist of just the converter input current $\hat{i}_g$, and output voltage $\hat{v}$. The four model inputs now consist of two physical quantities, input voltage $\hat{v}_g$ and load current $\hat{i}_{load}$, and of two control references, output voltage reference $\hat{v}_c$, and input voltage reference $\hat{v}_{gc}$. The final complete converter block diagram incorporating both CM control of the inductor current and FFFB control of the input and output voltages is shown in Figure 2.3(d).

$$\begin{bmatrix} \hat{i}_g \\ \hat{v} \end{bmatrix} = \begin{bmatrix} Y_{in-FFFB} & G_{igio-FFFB} & G_{igc-FFFB} & -\dfrac{1}{Z_{damp}} \\ G_{vg-FFFB} & -Z_{out-FFFB} & G_{vc-FFFB} & G_{vgc-FFFB} \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load} \\ \hat{v}_c \\ \hat{v}_{gc} \end{bmatrix} \tag{2.38}$$

$$Y_{in-FFFB} = Y_{in-CM} - \frac{G_{igc-CM}G_{vg-CM}}{G_{vc-CM}} \frac{T_{FB}}{1+T_{FB}} + \frac{T_{FF}}{1+T_{FB}} \tag{2.39}$$

$$G_{igio-FFFB} = G_{igio-CM} + \frac{G_{igc-CM}Z_{out-CM}}{G_{vc-CM}} \frac{T_{FB}}{1+T_{FB}} \tag{2.40}$$

$$G_{igc-FFFB} = \frac{G_{igc-CM}}{G_{vc-CM}} \frac{T_{FB}}{1+T_{FB}} \tag{2.41}$$

$$\frac{1}{Z_{damp}} = \frac{T_{FF}}{1+T_{FB}} \tag{2.42}$$

$$G_{vg-FFFB} = \frac{G_{vg-CM}}{1+T_{FB}} + \frac{G_{vc-CM}}{G_{igc-CM}} \frac{T_{FF}}{1+T_{FB}} \tag{2.43}$$

$$Z_{out-FFFB} = \frac{Z_{out-CM}}{1+T_{FB}} \tag{2.44}$$

$$G_{vc-FFFB} = \frac{T_{FB}}{1+T_{FB}} \tag{2.45}$$

$$G_{vgc-FFFB} = \frac{G_{vc-CM}}{G_{igc-CM}} \frac{T_{FF}}{1+T_{FB}} \tag{2.46}$$

The above procedure allows for the construction of small-signal unterminated closed-loop converter models. These models are especially useful for situations in which off-the-shelf converter hardware will be interconnected to form a complex power delivery system. In this type of design, converter control parameters have been predetermined by the original equipment manufacturer to achieve a certain level of performance under specific operating conditions. The model developed above allows for converters with existing controllers to be freely interconnected, such that detailed stability studies may be performed analytically.

2.3 Example Multi-Converter System Model and Parameter Extraction

In this section, the proposed unterminated two-port small-signal modeling technique is applied to a generalized multi-bus system consisting of four switching converters. The system, depicted in Figure 2.4, is a notional MVDC power distribution system consisting of a source buck converter (BKS) feeding a DC voltage bus, to which a load buck converter (BKL) and intermediate buck converter (BKI) are connected. The intermediate buck converter supplies a second bus, to which a load voltage source inverter (VSI) is connected. All converters operate under feedback control using an inner inductor current loop and output voltage loop PI control strategy. Both the BKL and VSI have PFF controllers for regulation of their inputs.

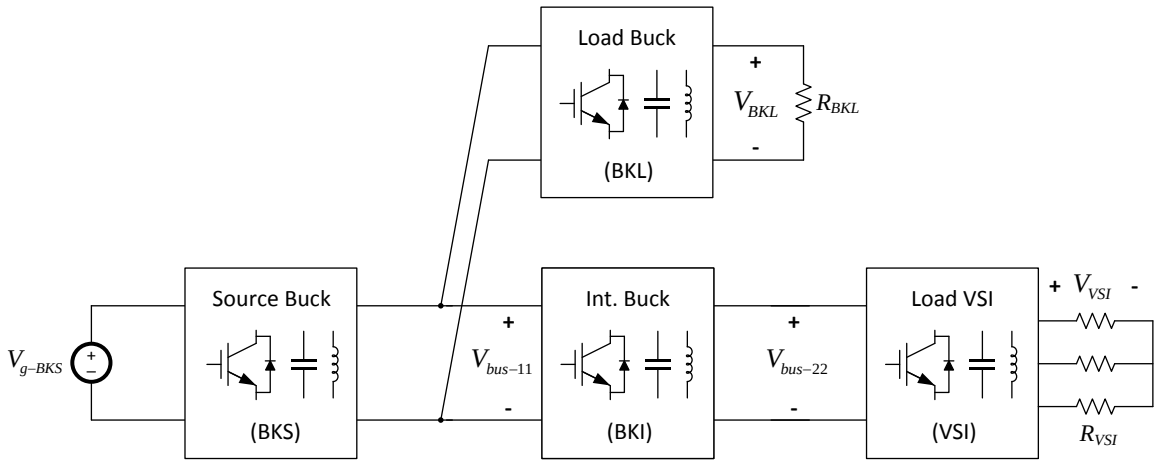


Figure 2.4. Scaled notional multi-bus MVDC distribution system.

For the development of the analytic system model, the g-parameters for all converters are computed following the establishment of the system operating point. This step will be detailed fully in Chapter 3 when the system operating parameters are explicitly stated. Here, the generalized model is simply constructed for use in later stability analysis and control design test scenarios. Construction of the overall system small-signal model is accomplished by interconnecting each individual converter model in the form shown in Figure 2.5. The VSI model is developed in the *dq0* reference frame using the Park Transformation. The model considers only the d-axis transfer functions as the q-axis voltage is controlled to be 0 V. More details on the VSI model are contained in Appendix B. Additional small-signal current source inputs i_{inj-1} and i_{inj-2} allow for small-signal perturbation of the two system buses, essential for the extraction of the analytic bus impedances. The small-signal current source inputs $i_{inj-BKL}$ and $i_{inj-VSI}$ are included to allow for extraction of the BKL and VSI output impedances, if desired. The small-signal control reference inputs for each converter are also included. The small-signal inductor current output of each converter is omitted from this model development as they are

unnecessary in the analysis of the overall system behavior. Note that the BKL and VSI converters are terminated with resistive loads.

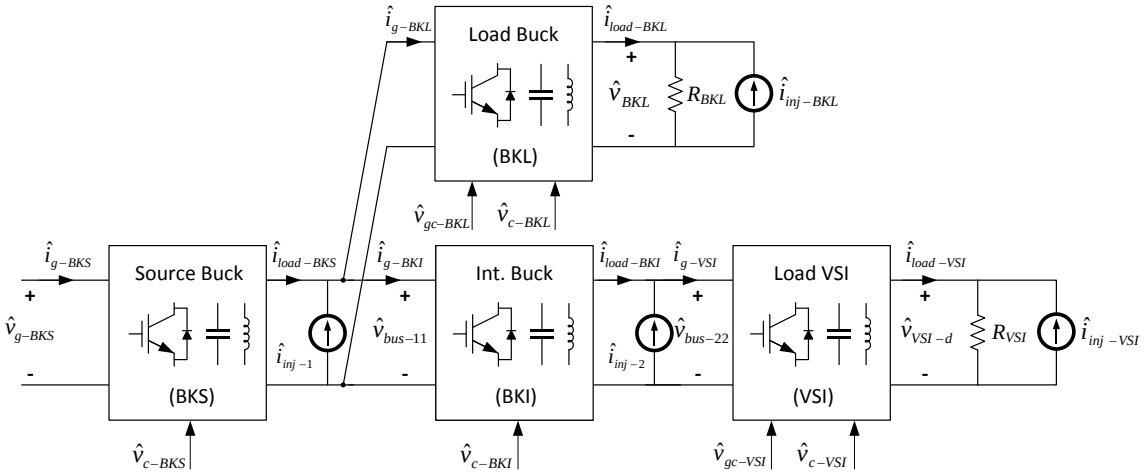


Figure 2.5. Small-signal system model construction.

Using the block diagram converter representations developed in Figure 2.3, a series of equations can be written by inspection using KCL and KVL to describe the system of Figure 2.5, (2.47)-(2.58).

$$\hat{i}_{g-BKS} - Y_{in-BKS}\hat{v}_{g-BKS} - G_{igio-BKS}\hat{i}_{load-BKS} - G_{igc-BKS}\hat{v}_{c-BKS} = 0 \tag{2.47}$$

$$\hat{v}_{bus-11} - G_{vg-BKS}\hat{v}_{g-BKS} + Z_{out-BKS}\hat{i}_{load-BKS} - G_{vc-BKS}\hat{v}_{c-BKS} = 0 \tag{2.48}$$

$$\hat{i}_{g-BKI} - Y_{in-BKI}\hat{v}_{bus-11} - G_{igio-BKI}\hat{i}_{load-BKI} - G_{igc-BKI}\hat{v}_{c-BKI} = 0 \tag{2.49}$$

$$\hat{v}_{bus-22} - G_{vg-BKI}\hat{v}_{bus-11} + Z_{out-BKI}\hat{i}_{load-BKI} - G_{vc-BKI}\hat{v}_{c-BKI} = 0 \tag{2.50}$$

$$\hat{i}_{g-VSI} - Y_{in-VSI}\hat{v}_{bus-22} - G_{igio-VSI}\hat{i}_{load-VSI} - G_{igc-VSI}\hat{v}_{c-VSI} + Y_{damp-VSI}\hat{v}_{gc-VSI} = 0 \tag{2.51}$$

$$\hat{v}_{VSI-d} - G_{vg-VSI}\hat{v}_{bus-22} + Z_{out-VSI}\hat{i}_{load-VSI} - G_{vc-VSI}\hat{v}_{c-VSI} - G_{vgc-VSI}\hat{v}_{gc-VSI} = 0 \tag{2.52}$$

$$\hat{i}_{g-BKL} - Y_{in-BKL}\hat{v}_{bus-11} - G_{igio-BKL}\hat{i}_{load-BKL} - G_{igc-BKL}\hat{v}_{c-BKL} + Y_{damp-BKL}\hat{v}_{gc-BKL} = 0 \tag{2.53}$$

$$\hat{v}_{BKL} - G_{vg-BKL}\hat{v}_{bus-11} + Z_{out-BKL}\hat{i}_{load-BKL} - G_{vc-BKL}\hat{v}_{c-BKL} - G_{vgc-BKL}\hat{v}_{gc-BKL} = 0 \tag{2.54}$$

$$\hat{i}_{load-BKS} - \hat{i}_{g-BKI} - \hat{i}_{g-BKL} + \hat{i}_{inj-1} = 0 \tag{2.55}$$

$$\hat{i}_{load-BKI} - \hat{i}_{g-VSI} + \hat{i}_{inj-2} = 0 \tag{2.56}$$

$$\hat{i}_{load-VSI} - \frac{\hat{v}_{VSI-d}}{R_{VSI}} + \hat{i}_{inj-3} = 0 \tag{2.57}$$

$$\hat{i}_{load-BKL} - \frac{\hat{v}_{BKL}}{R_{BKL}} + \hat{i}_{inj-4} = 0 \tag{2.58}$$

$$G_{sys} \cdot \begin{bmatrix} \hat{i}_{g-BKS} \\ \hat{v}_{bus-11} \\ \hat{i}_{g-BKI} \\ \hat{v}_{bus-22} \\ \hat{i}_{g-VSI} \\ \hat{v}_{VSI-d} \\ \hat{i}_{g-BKL} \\ \hat{v}_{BKL} \\ \hat{i}_{load-BKS} \\ \hat{i}_{load-BKI} \\ \hat{i}_{load-VSI} \\ \hat{i}_{load-BKL} \\ \hat{v}_{g-BKS} \\ \hat{v}_{c-BKS} \\ \hat{v}_{c-BKI} \\ \hat{v}_{c-VSI} \\ \hat{v}_{gc-VSI} \\ \hat{v}_{c-BKL} \\ \hat{v}_{gc-BKL} \\ \hat{i}_{inj-1} \\ \hat{i}_{inj-2} \\ \hat{i}_{inj-VSI} \\ \hat{i}_{inj-BKL} \end{bmatrix} = 0 \tag{2.59}$$

The above system of equations can be represented in a matrix G_{sys} taking care to arrange the elements such that all g-parameter output variable coefficients are positioned in the leftmost columns. Input variable coefficients are then positioned in the rightmost

columns. See Appendix B for the complete G_{sys} matrix for this system. For the outputs of this model, the system description is as given in (2.59). The solution of the system is obtained following reformulation of the matrix G_{sys} in reduced row-echelon form. All transfer functions and impedances of the interconnected system are easily obtained from the resulting matrix.

2.4 SUMMARY OF MULTI-CONVERTER SYSTEM MODELING

Switching converter modeling techniques were presented in this chapter. The conventional resistively terminated buck converter model was developed and small-signal transfer functions relating the various input-to-output quantities and system impedances were developed. Limitations of this type of model when applied to large interconnected systems consisting of numerous switching converters were described. To alleviate these issues, an unterminated two-port modeling technique for switching converters based on hybrid g-parameters was introduced. The unterminated buck switching converter model including multi-loop feedback and feedforward control was detailed in full. Following the same approach, unterminated models for other types of converters may be easily derived. The model for a four-converter multi-bus system that will be used throughout the remainder of this dissertation was constructed using the unterminated modeling technique.

CHAPTER 3

MULTI-CONVERTER SYSTEM STABILITY EVALUATION AND IMPROVEMENT

The Passivity Based Stability Criterion (PBSC) is introduced as a method for system level stability evaluation and control design in this chapter. Positive Feed-Forward (PFF) control is subsequently discussed as a method for stabilizing the system buses by ensuring bus impedance passivity. A new methodology is proposed for evaluating bus impedance damping and designing suitable damping impedances for implementation via PFF control. An example system based on the four-converter multi-bus distribution system modeled previously in Chapter 2 is evaluated using the proposed techniques.

3.1 PASSIVITY BASED STABILITY CRITERION FOR MULTI-BUS SYSTEMS

The Passivity-Based Stability Criterion (PBSC) has recently been proposed to address system-level stability issues [20]. This criterion is based on the passivity of the system DC bus impedance rather than on the Nyquist Criterion applied to the impedance ratio called the Minor Loop Gain. For a single-bus system, if the bus impedance of the system is determined to be passive, the system is stable.

The conceptual multi-bus power electronic-enabled distribution architecture, Figure 3.1, has *n* buses and may contain a large number of switching power converters, loads, and sources. This system can be reduced to an equivalent *n*-port network by looking into each bus port. The main difference arising between the single-bus system

and the multi-bus system is that the system bus impedance is now in the form of a matrix, as given in (3.1).

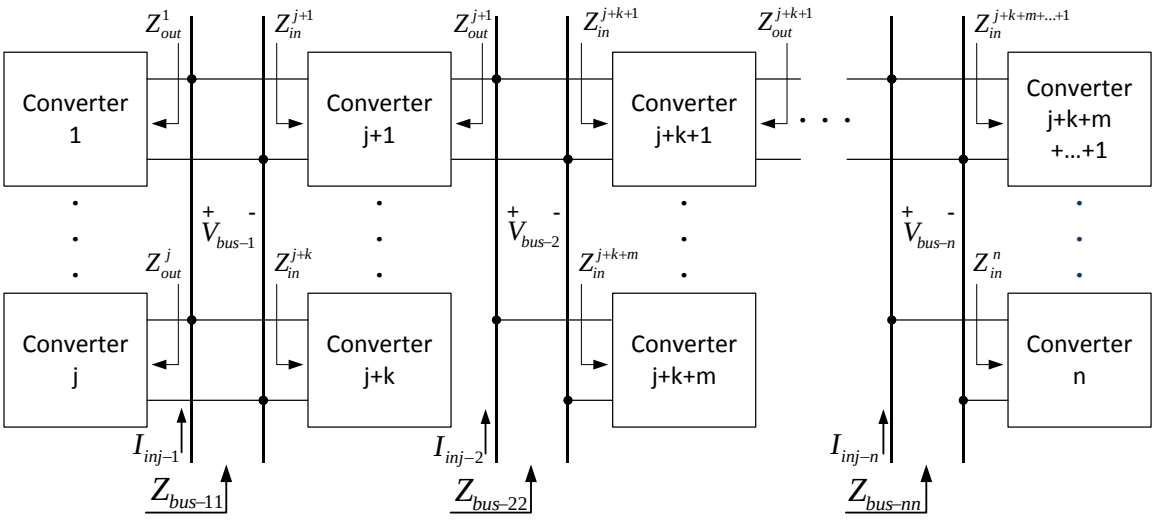


Figure 3.1. Conceptual multi-bus power distribution system showing multiple interconnections using power converter interfaces.

$$V_{bus} = Z_{bus} I_{inj}$$

$$\begin{bmatrix} V_{bus-1} \\ V_{bus-2} \\ \vdots \\ V_{bus-n} \end{bmatrix} = \begin{bmatrix} Z_{bus-11} & Z_{bus-12} & \cdots & Z_{bus-1n} \\ Z_{bus-21} & Z_{bus-22} & \cdots & Z_{bus-2n} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{bus-n1} & Z_{bus-n2} & \cdots & Z_{bus-nn} \end{bmatrix} \begin{bmatrix} I_{inj-1} \\ I_{inj-2} \\ \vdots \\ I_{inj-n} \end{bmatrix} \tag{3.1}$$

where V_{bus-1}, $V_{bus-2}, \ldots, V_{bus-n}$ are the bus voltages and I_{inj-1}, I_{inj-2}, …, I_{inj-n} are the injection currents. The impedance Z_{bus-ij} for $i=j$ is the self-impedance of the i^{th} bus, while impedance Z_{bus-ij} for $i \neq j$ is the cross-impedance between the i^{th} bus and the j^{th} bus. The self-impedance is simply the parallel combination of all source converter output impedances and load converter input impedances connected to the i^{th} bus under the condition of no current injection into any of the other buses. The cross-impedance represents the effect of a current injected into the j^{th} bus on the voltage of the i^{th} bus. This can be understood as the following, in (3.2).

$$Z_{bus-ii} = \left.\frac{V_{bus-i}}{I_{inj-i}}\right|_{I_k=0} \quad \forall k \neq i$$
$$Z_{bus-ij} = \left.\frac{V_{bus-i}}{I_{inj-j}}\right|_{I_k=0} \quad \forall k \neq j \tag{3.2}$$

A generalized passivity criterion developed in the frequency domain and applicable to *n*-port networks has been presented previously in [23], [24]. The final result of this development is as follows. A linear time-invariant *n*-port network is passive if and only if:

1. $Z_{bus}(j\omega)$ contains no right half plane poles
2. The Nyquist plot of the *n* upper left determinants of $Z_{bus}(j\omega) + Z_{bus}^{H}(j\omega)$ lie in the right half plane (RHP)

where $Z_{bus}(j\omega)$ is the bus impedance matrix and $Z_{bus}^{H}(j\omega)$ is the associated conjugate transpose. While this analysis allows for the passivity determination of a generalized *n*-port network, significant application issues exist. In particular, the criterion requires the evaluation of the *n* upper-left determinants of the sum of the impedance matrix and its conjugate transpose $(Z_{bus}(j\omega) + Z_{bus}^{H}(j\omega))$ for passivity, a computationally complex operation for systems consisting of numerous buses. The order of the resulting matrix elements can quickly become unmanageable and cause computational issues. A second issue relates to the interpretation of the stability analysis results. The first upper left determinant of the matrix $Z_{bus}(j\omega) + Z_{bus}^{H}(j\omega)$ corresponds to the passivity of the $Z_{bus\text{-}11}$ self-impedance. However, subsequent upper left determinants are not easily related back to the actual system. Accordingly, the origin of a passivity violation is difficult to trace if

any of these other upper left determinants result in a Nyquist plot that extends into the left half plane (LHP). Thus, the results of this stability analysis do not aid in the design of stabilizing controllers to improve the system response and ensure good stability margins.

In an effort to deal with the shortcomings of the generalized *n*-port passivity criterion, the following more practical approach based on the single-bus PBSC is proposed for use in multi-bus system stability analysis. Consider the notional multi-bus system, depicted in Figure 3.1. Looking into the bus 1 port, the system may be reduced to an equivalent interacting source and load subsystem network, as in Figure 3.2(a). The PBSC further combines the two systems, resulting in the equivalent 1-port network shown in Figure 3.2(b). The resulting 1-port network has, when observed from the bus port, an impedance $Z_{bus\text{-}11}(s) = V_{bus\text{-}1}(s)/I_{inj\text{-}1}(s)$, where $I_{inj\text{-}1}(s)$ is an injection current supplied by an external device to perturb the bus. The bus impedance of the network is the parallel combination of all source subsystem output impedances and load subsystem input impedances, which may be constructed using the unterminated small-signal modeling approach detailed previously. The system bus under study is passive if and only if:

1. $Z_{bus\text{–}ii}(j\omega)$ contains no right half plane poles
2. $\mathrm{Re}\{Z_{bus\text{–}ii}(j\omega)\} \geq 0, \forall\omega$

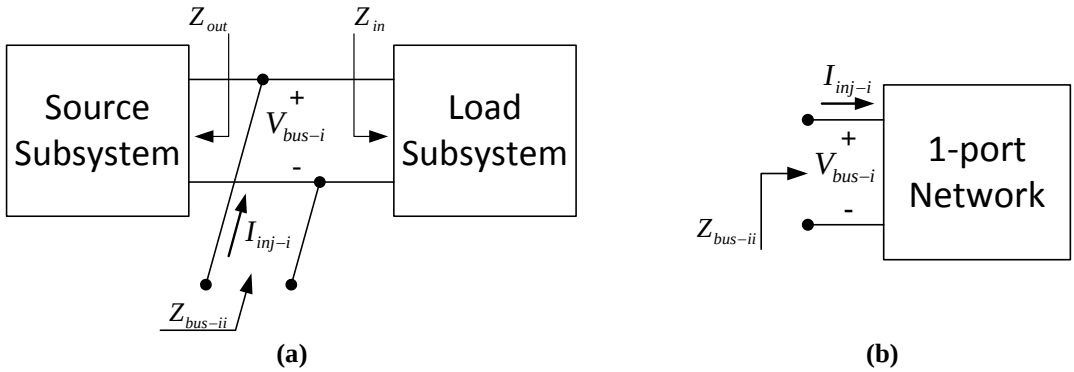


Figure 3.2. (a) Equivalent interacting source and load subsystems and (b) 1-port network.

All system bus self-impedances through $Z_{bus\text{-}nn}$(s) as indicated in Figure 3.1 may be constructed in a similar manner and individually tested for passivity. This approach is equivalent to evaluating each diagonal element in the Z_{bus} matrix (3.1) for passivity. Note that this is only a necessary condition for passivity. Applying a passivity criterion to each bus and utilizing the newly proposed Allowable Impedance Region method described below provides a design-oriented control design criterion compatible with Positive Feed-Forward control, which can then be used to improve stability and system damping. If all buses are determined to exhibit passivity with good margins, as defined by the Allowable Impedance Region method, the system is expected to be stable and well-damped.

3.2 ALLOWABLE IMPEDANCE REGION

In the form stated above, the PBSC can only be used to ascertain the general stability of the system. A system having a bus impedance contour that lies in the right half plane (RHP) is deemed passive and thus stable. However, no information is directly made available that relates the dynamic performance of the system. As a result, a system that satisfies the PBSC can exhibit undesirable oscillations and poor performance. In this scenario, the required level of additional damping via PFF control to eliminate oscillatory

behavior is unknown. A technique to gauge the system's damping is proposed to aid in the interpretation of the PBSC and design of suitable stabilizing controllers. This situation is similar to the case of feedback systems where the Nyquist criterion guarantees stability but may lead to lightly damped closed-loop systems; this has led to the development of stability margins such as the gain margin and the phase margin.

Consider the following simplified function that is representative of a feedback (FB) controlled converter system bus impedance. Note that the system in (3.3) is passive and satisfies the PBSC for damping coefficient $\zeta_{bus} > 0$.

$$Z_{bus-FB} = Z_{0-bus} \frac{\frac{s}{\omega_0}}{\frac{s^2}{\omega_0^2} + 2\zeta_{bus}\frac{s}{\omega_0} + 1} \tag{3.3}$$

In a typical coupled FB controlled converter system the bus impedance is dominated at both high and low frequencies by the output impedance of the source converter. Impedance interaction is typically confined to a small frequency range around the resonant frequency, ω_0, where the source and load bus-side impedances are comparable in magnitude resulting in decreased damping. This representative model will allow for a simplified analysis of the bus impedance damping as it relates to the Nyquist contour plot.

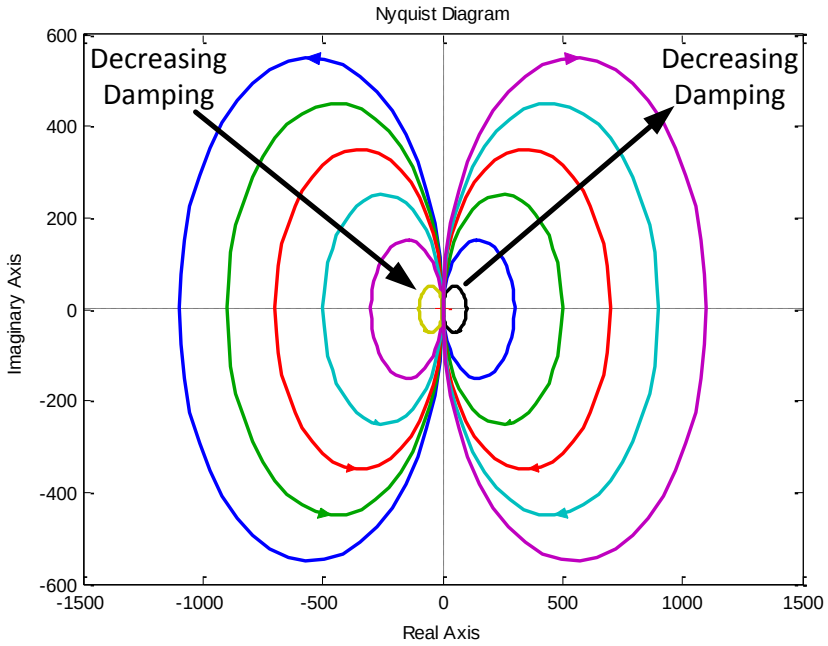


Figure 3.3. Nyquist contour of simplified bus impedance for various levels of damping.

The general behavior of the bus impedance Nyquist contour for varying levels of damping is depicted in Figure 3.3 and illustrates the effect of successive decreases in damping for the system given in (3.3). As the damping coefficient ζ_{bus} decreases from an arbitrary positive value to zero, the Nyquist contour extends further out into the RHP. When the damping becomes negative, the system becomes unstable, the bus impedance non-passive and the impedance contour flips about the imaginary axis, enters the LHP, and shrinks in size for further decreases in ζ_{bus}. When plotted, the Nyquist contour of (3.3) having a positive damping coefficient traces a circle in the RHP, intersecting the real axis at $\omega = \omega_0$ with a magnitude of $Z_{0\text{-}bus}/(2\zeta_{bus})$. This is expected since the system becomes purely real at the resonant frequency. The size of the Nyquist contour of an impedance in this form is shown to be dependent on both the constant gain $Z_{0\text{-}bus}$ and the damping ζ_{bus}. A meaningful interpretation of the system damping can therefore be made

by normalizing the observed impedance to the constant value $Z_{0\text{-}bus}$. The normalized bus impedance is defined as follows. Note that the real axis intercept of the Nyquist contour of the normalized impedance is numerically equal to $Q_{bus} = 1/2\zeta_{bus}$, the Q-factor of bus impedance (3.3).

$$Z_{bus-FB-N} = \frac{Z_{bus-FB}}{Z_{0-bus}} \tag{3.4}$$

Based on this development, an appropriate region in the s-plane may be identified in which the normalized impedance contour must lie to ensure a specified level of damping. Ideally, the area delimited by the vertical line shown in Figure 3.4(a) and the imaginary axis constitutes a suitable region for the Nyquist contour of the normalized bus impedance (3.3) that ensures a minimum damping factor ζ_{min} at the resonant frequency. For $\zeta_{bus} \leq \zeta_{min}$, the Nyquist contour (blue) will intersect the real axis at a point inside the region in Figure 3.4(a).

However, a realistic bus impedance function will exhibit a more complex frequency response than the simplified model given in (3.3). Additional poles and zeros are introduced into the bus impedance function as a result of multiple points of interaction between source and load subsystem impedances. The normalized Nyquist contour of a realistic bus impedance is therefore unlikely to be symmetrical about the real axis due to these additional points of interaction, such that the intersection of the contour with the real axis does not occur at the resonant frequency with the least damping. Thus, the shape of the normalized bus impedance (red) is different from the simplified case (3.3), as shown in Figure 3.4(a). In this scenario, the allowable region delimited by the

vertical asymptote Re = $1/(2\zeta_{min})$ erroneously indicates that the realistic bus impedance has an acceptable amount of damping at the resonant frequency.

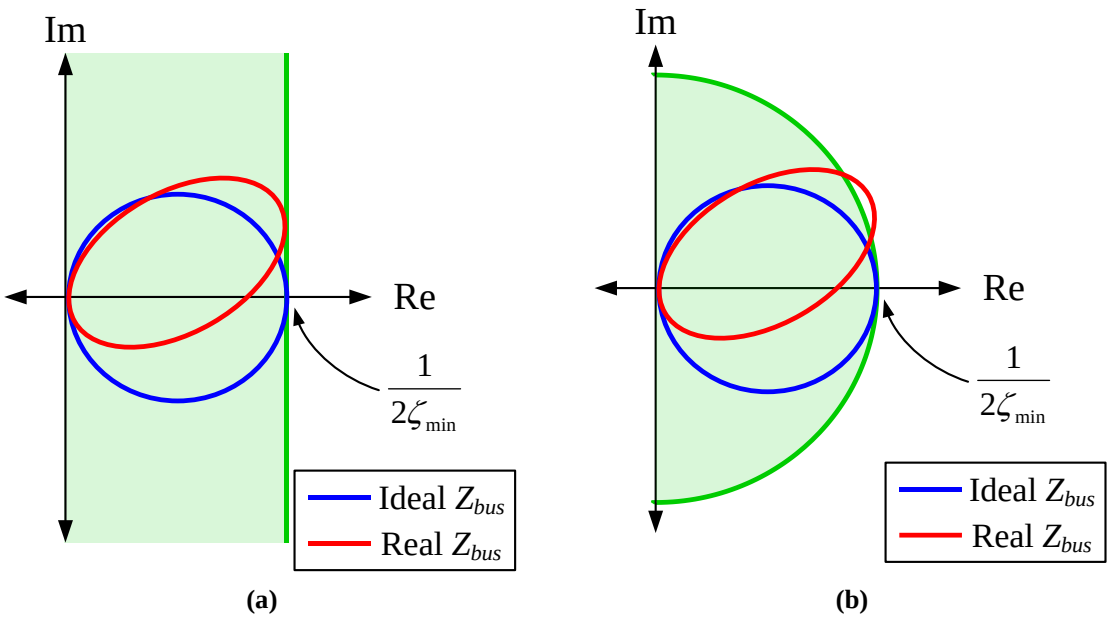


Figure 3.4. Comparison of realistic bus impedance Nyquist contour for an Allowable Impedance Region specified by (a) vertical asymptote limit and (b) semicircle centered at the origin.

In this work, the use of a semicircle centered in the origin and located in the RHP is proposed as the allowable region in which the bus impedance contour under study must be situated. This Allowable Impedance Region is defined in (3.5) and shown in Figure 3.4(b).

$$M(\vartheta) = \frac{1}{2\zeta_{\min}} e^{j\vartheta} \text{ for } -\frac{\pi}{2} \le \vartheta \le \frac{\pi}{2} \tag{3.5}$$

where ζ_{min} is the minimum desired system damping factor at the bus impedance resonant frequency. By defining an allowable region in the *s*-plane according to (3.5), an effective limit is set on the magnitude of the normalized bus impedance at all frequencies to ensure that the system resonance will be well damped. A typical choice is ζ_{min} = 0.5 resulting in

a semicircle (3.5) of unit magnitude, meaning that the system has a *Q*-factor of unity. Note that the realistic bus impedance contour is shown to now lie outside of the allowable region, indicating that the resonance is not acceptably damped. While the development of the Allowable Impedance Region is careful to consider the impact of additional dynamics that cause a real bus impedance to differ from the simplified model of (3.3), it is worthwhile to note that the bus impedance of a feedback controlled system is typically strongly dominated by a single resonance and thus exhibits the general behavior of the simplified model.

3.3 Positive Feed-Forward Control and Damping Impedance Design

The PBSC is a far more design-oriented stability criterion when compared to prior methods of evaluating system stability, lending itself to the design of virtual damping impedances that may be actively inserted into the system bus under study with the objective of damping resonances or otherwise modifying the bus impedance such that it appears passive. Previous work in [22]-[23] has shown that a control method called Positive Feed-Forward (PFF) control may be used to insert virtual damping impedances into the load subsystem of a system bus, see Figure 3.2(a). A switching converter employing this control technique includes a positive feed-forward loop for active damping control at the converter input in addition to the negative feedback loop that is typically used to regulate the converter output.

The effect of PFF control on converter behavior is shown in the model developed in Chapter 2, see equations (2.38)-(2.46). This control technique provides a way to modify the converter input impedance by effectively introducing an active damping impedance, Z_{damp}, given by (2.33), in parallel with the already existing converter input

impedance. Given knowledge of the bus impedance, a PFF controller may be designed to introduce an appropriate Z_{damp} such that the PBSC is satisfied, resulting in a stable system. A new contribution of this dissertation is the Allowable Impedance Region method described above, which gives improved damping as long as the normalized bus impedance $Z_{bus\text{-}FFFB\text{-}N}$ is contained in the semicircle defined by (3.5). However, ensuring this condition requires testing the bus impedance at all frequencies.

It is observed in practice that the Allowable Impedance Region condition (or equivalently the passivity condition) is typically violated around the resonant frequency ω_0 of the system bus impedance. It is at this frequency that the source subsystem output impedance is often comparable to or even exceeds the load subsystem input impedance, resulting in undesirable interactions. At lower and higher frequencies the bus impedance is typically dominated by the output impedance of the source subsystem. The damping impedance Z_{damp} is therefore designed to ensure damping at the resonant frequency. This can be done by enforcing the conditions in (3.6) with Z_{damp} designed such that the overall bus impedance appears passive.

$$\frac{1}{Z_{bus-FFFB}} = \frac{1}{Z_{out-FB}} + \frac{1}{Z_{in-FB}} + \frac{1}{Z_{damp}} \approx \begin{cases} \dfrac{1}{Z_{out-FB}} & at\ low\ frequencies \\ \dfrac{1}{Z_{damp}} & at\ \omega = \omega_0 \\ \dfrac{1}{Z_{out-FB}} & at\ high\ frequencies \end{cases} \tag{3.6}$$

where $Z_{out\text{-}FB}$ is the output impedance of the source subsystem and $Z_{in\text{-}FB}$ is the input impedance of the load subsystem under feedback control only.

The additional insight into the dynamic behavior of bus impedances afforded by the Allowable Impedance Region analysis results in a greatly simplified and straightforward PFF control design. The virtual damping impedance Z_{damp} may now be designed to ensure that the normalized bus impedance contour resides within the Allowable Impedance Region. For this work, a virtual damping impedance of the form $Z_{damp} = R_b + sL_b + 1/sC_b$ is selected to ensure that the bus impedance is only modified for a small bandwidth of frequencies, as described in (3.6). The general expression of the series *RLC* damping impedance frequency response is given in (3.7).

$$Z_{damp} = Z_{0-damp} \frac{\frac{s^2}{\omega_0^2} + 2\zeta_{damp}\frac{s}{\omega_0} + 1}{\frac{s}{\omega_0}} \tag{3.7}$$

The magnitude of the bus impedance when the system is operated under feed-forward and feedback (FFFB) control $Z_{bus\text{-}FFFB}$ is the parallel combination of the FB only bus impedance $Z_{bus\text{-}FB}$ and the damping impedance Z_{damp}. To ensure that the Nyquist contour of $Z_{bus\text{-}FFFB\text{-}N}$ resides within the Allowable Impedance Region, the following condition is imposed upon the bus impedance. This development only concerns the magnitudes of the bus and damping impedances at resonance since that is ideally the only point of interaction, according to (3.6).

$$\left|Z_{bus-FFFB-N}(j\omega_0)\right| = \left|\frac{Z_{bus-FFFB}(j\omega_0)}{Z_{0-bus}}\right| = \left|\frac{Z_{bus-FB}(j\omega_0) \parallel Z_{damp}(j\omega_0)}{Z_{0-bus}}\right| = |M| - K_m \tag{3.8}$$

where $|M|$ is usually chosen to be unity and K_m is an additional parameter that determines the magnitude difference between the damped normalized bus impedance Nyquist contour and the Allowable Impedance Region boundary. This parameter can be used to

impose additional damping on the bus where PFF control is applied (see Figure 3.5) and ensure good damping for all buses. Note that the Allowable Impedance Region (3.5) must be satisfied by all bus self-impedances. For the simplified model given in (3.3) and the damping impedance given in (3.7), this condition is further written as follows.

$$\left|Z_{bus-FFFB-N}(j\omega_0)\right| = \left(\frac{1}{2\zeta_{damp}} \cdot \frac{Z_{0-bus}}{Z_{0-damp}} + 2\zeta_{bus}\right)^{-1} = |M| - K_m \tag{3.9}$$

The expression given in (3.9) considers that the bus impedance has been normalized by the value $Z_{0\text{-}bus}$. Thus, the design criterion for the damping impedance is based on the constant gain $Z_{0\text{-}damp}$, as shown in (3.10).

$$Z_{0-damp} = \left[\frac{2\zeta_{damp}}{Z_{0-bus}}\left(\frac{1}{|M| - K_m} - 2\zeta_{bus}\right)\right]^{-1} \tag{3.10}$$

where $0 \leq K_m < |M|$. For the damping impedance, it is desirable that $\zeta_{damp} >> \zeta_{bus\text{-}FB}$ to minimize the potential for creating additional resonances in the bus impedance. The effect of varying K_m values on the resulting $Z_{bus\text{-}FFFB}$ is shown in Figure 3.5. Selecting K_m equal to zero results in a PFF control design in which the normalized $Z_{bus\text{-}FFFB\text{-}N}$ has a magnitude of M at resonance. In practice, it is recommended to increase K_m to ensure that the additional dynamics of a real system do not cause the Allowable Impedance Region to be violated.

Following the damping impedance design, the PFF controller may be designed for the multi-loop feedback converter derived in Chapter 2 using the following relation in (3.11). This equation is derived by substituting in (2.42) expressions for T_{FF} and T_{FB}. More details on the derivation of this expression are found in [23].

$$G_{FF} = \frac{1 + G_{FB} G_{vc-CM}}{G_{igc-CM} Z_{damp}} \tag{3.11}$$

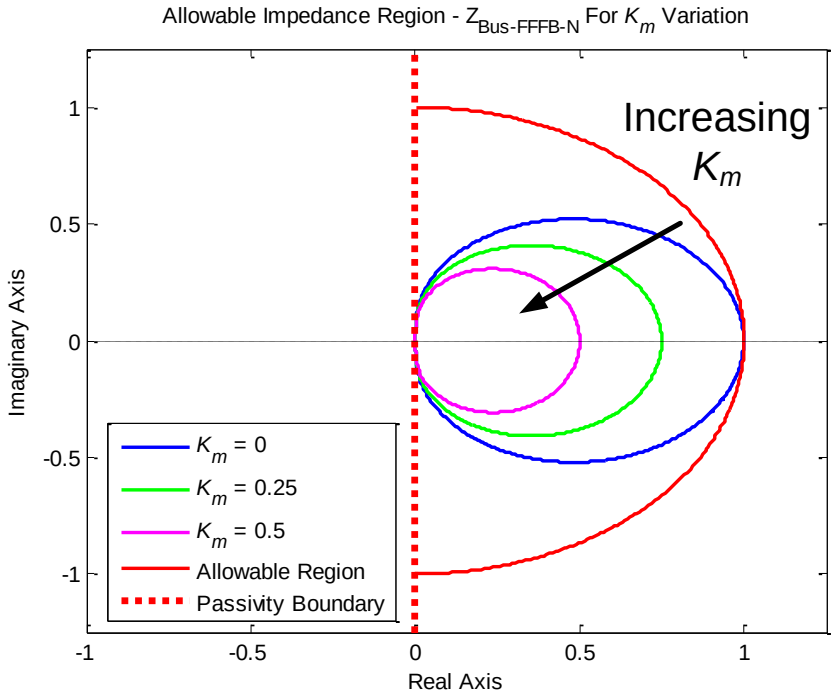


Figure 3.5. Nyquist contour of simplified bus impedance under PFF control for varying values of K_m (ζ_{min} = 0.5).

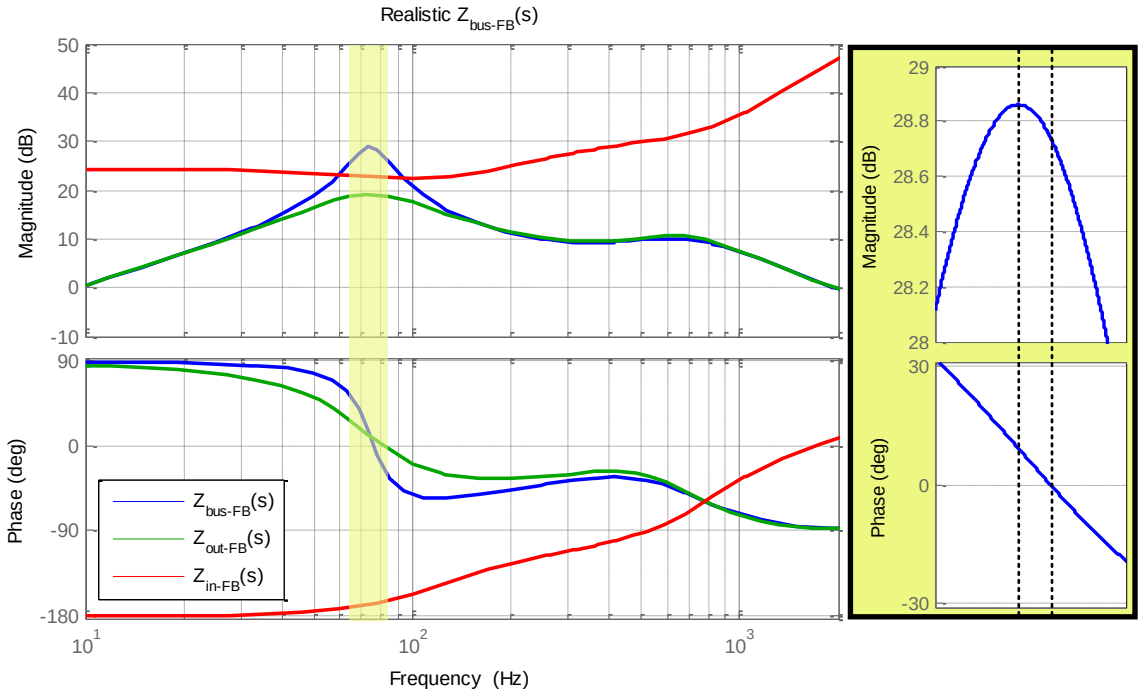
As stated previously, a real bus impedance function will exhibit a more complex frequency response than the simplified model given in (3.3) from which the damping impedance design (3.8)-(3.10) is developed. Due to additional poles and zeros introduced by multiple points of interaction between the source subsystem and load subsystem impedances, the normalized Nyquist contour of a realistic bus impedance is unlikely to be symmetrical about the real axis due to these additional points of interaction.

Consider the bus impedance function shown in Figure 3.6(a). The bus self-impedance $Z_{bus\text{-}FB}$ exhibits a similar response to the simplified system of (3.3) and is dominated by a significant resonance at 74.25 Hz. Note, however, that the phase of the

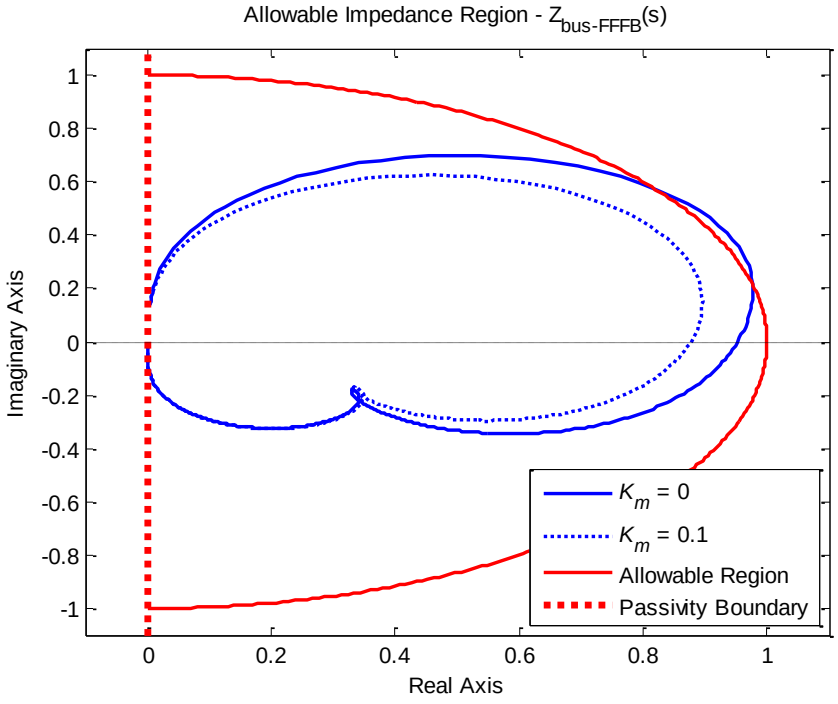
system does not pass through 0° where the magnitude of the system is greatest at the peak of the resonance (inset of Figure 3.6(a)). The high frequency behavior also exhibits multiple damped resonances around 700 Hz. As a result, the normalized Nyquist contour of $Z_{bus\text{-}FB\text{-}N}$ is asymmetrical about the real axis when plotted against the Allowable Impedance Region for $\zeta_{min} = 0.5$.

A PFF control design based on (3.10) for $K_m = 0$ results in the system depicted in Figure 3.6(b) (solid blue). The magnitude of the impedance has been reduced such that the real axis intercept of $Z_{bus\text{-}FFFB\text{-}N}$ now falls within the Allowable Impedance Region. However, the condition is still violated due to the asymmetry of the contour. A second PFF control design for $K_m = 0.1$ causes the Nyquist contour of $Z_{bus\text{-}FFFB\text{-}N}$ to lie completely within the Allowable Impedance Region, Figure 3.6(b) (dashed blue), satisfying the criterion. This demonstration illustrates the importance of the additional damping margin factor K_m in ensuring that the entire Nyquist contour of a realistic normalized system bus impedance falls within the Allowable Impedance Region.

This demonstration also validates the choice of a semicircular Allowable Impedance Region as in (3.5). The use of a semicircular boundary rather than a simple horizontal asymptote ensures that the bus impedance will have a well damped magnitude response by enforcing a magnitude limit on the bus impedance response at all frequencies rather than on just a single point of resonance.



(a)



(b)

Figure 3.6. Bode plot and Allowable Impedance Region analysis (ζ_{min} = 0.5) on realistic system bus self-impedance under FB control only.

3.4 ADAPTIVE PFF CONTROL

It can be seen that the Allowable Impedance Region (AIR) and PFF control techniques complement each other. PFF control can be used to ensure that the AIR is satisfied by shaping the converter system bus self-impedances such that their respective Nyquist contours lie within the specified region demarcated in the *s*-plane. The incorporation of impedance identification to the system controlled using these techniques facilitates online monitoring of the overall system stability and provides for adaptive control capabilities. Changes in the bus self-impedances can be tracked as the system dynamics evolve over time due to reconfigurations and different Electric Ship mission scenarios.

An example control adaptation algorithm is shown in Figure 3.7. This method uses the impedance identification procedure to monitor the system bus self-impedances. Following collection of the perturbed voltage and current data, the impedance models are parameterized using a model fitting technique called Least Squares Fitting [40]. The system stability is then evaluated by applying the PBSC and AIR analysis to the measured, normalized bus self-impedances. If the bus self-impedances under study do not meet the criteria for a user specified ζ_{min}, a PFF controller is designed to insert a virtual damping impedance according to (3.10)-(3.11) such that the system damping is improved. The adaptive nature of this control algorithm ensures system resilience and survivability.

An example timing diagram of the adaptive control algorithm is depicted in Figure 3.8. As shown, the Bus Perturbation and Impedance Construction and Parameterization steps shown in Figure 3.7 may be repeated at regular intervals for periodic monitoring of the bus self-impedances and system configuration, or in response

to measured events such as oscillations in the system bus voltage. The length of the perturbation and post-processing step, T_{ID}, is primarily dependent on the length of the injected PRBS sequence and desired bandwidth of the measurement. A complete adaptive control cycle from initial bus voltage perturbation to final confirmation that the synthesized PFF controller has successfully damped the bus impedance is the interval T_{adapt}.

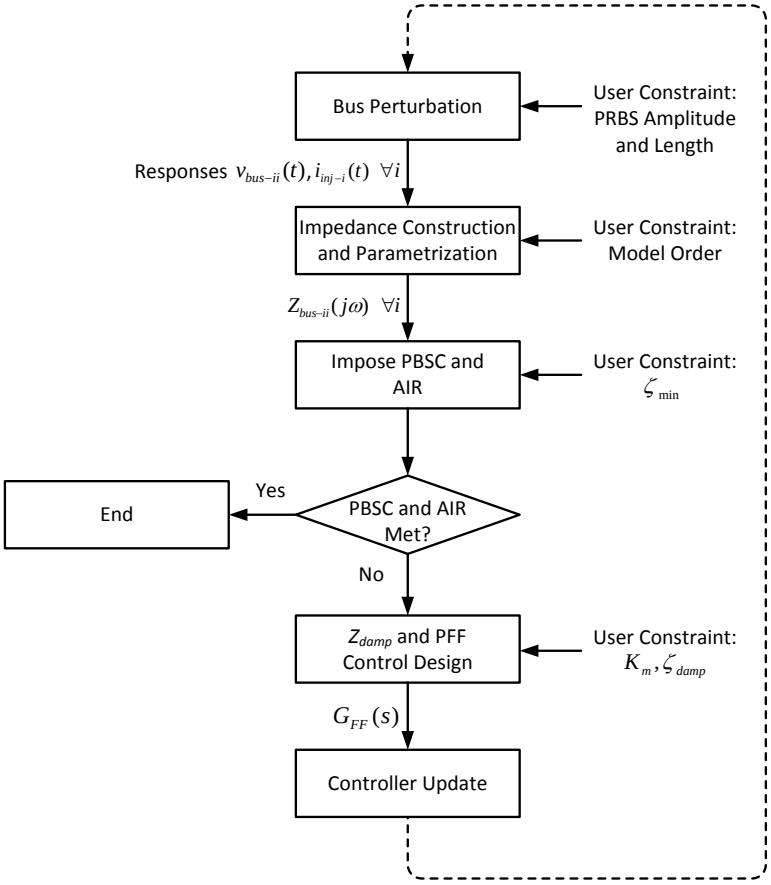


Figure 3.7. Adaptive control algorithm for MVDC distribution system combining the PBSC, AIR analysis, and PFF control techniques with online impedance monitoring.

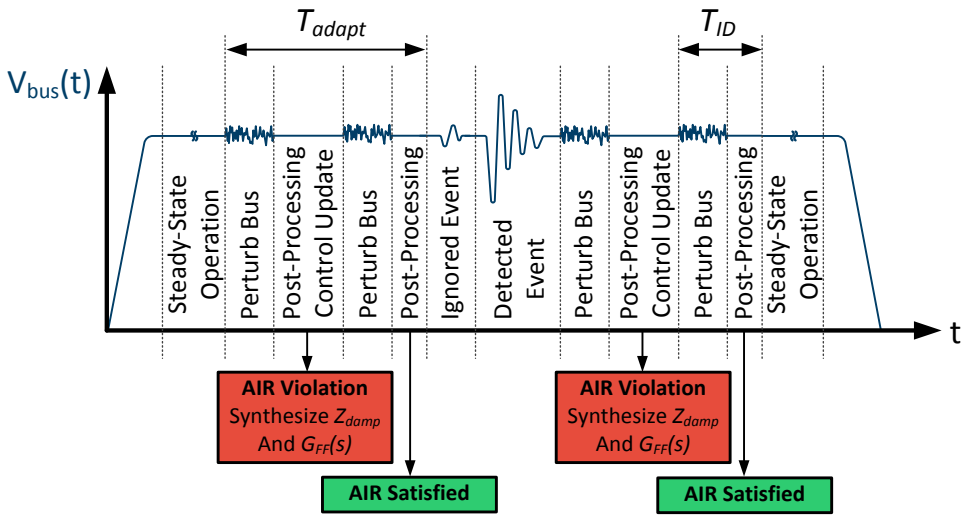


Figure 3.8. Example timing diagram of adaptive control scheme for impedance based control.

3.5 Example Analytic System Evaluation and Control Design

The proposed Allowable Impedance Region analysis and damping impedance design method given previously are now applied to the four-converter multi-bus system modeled at the end of Chapter 2. Two scenarios are evaluated for which the system bus self-impedances are deemed passive at all frequencies but require additional damping to meet the requirements of the Allowable Impedance Region. In Scenario 1, a prominent resonance is present on Bus 1. Scenario 2 considers a system where the resonance is more pronounced on Bus 2. The complete hardware and control parameters for each converter shown in Figure 3.9 are given in Table 3.1. The PI control coefficients for the inner current loop ($K_{p\text{-}il}$ and $K_{i\text{-}il}$) and outer voltage loop ($K_{p\text{-}v}$ and $K_{i\text{-}v}$) of each converter are provided for both Scenario 1 and Scenario 2.

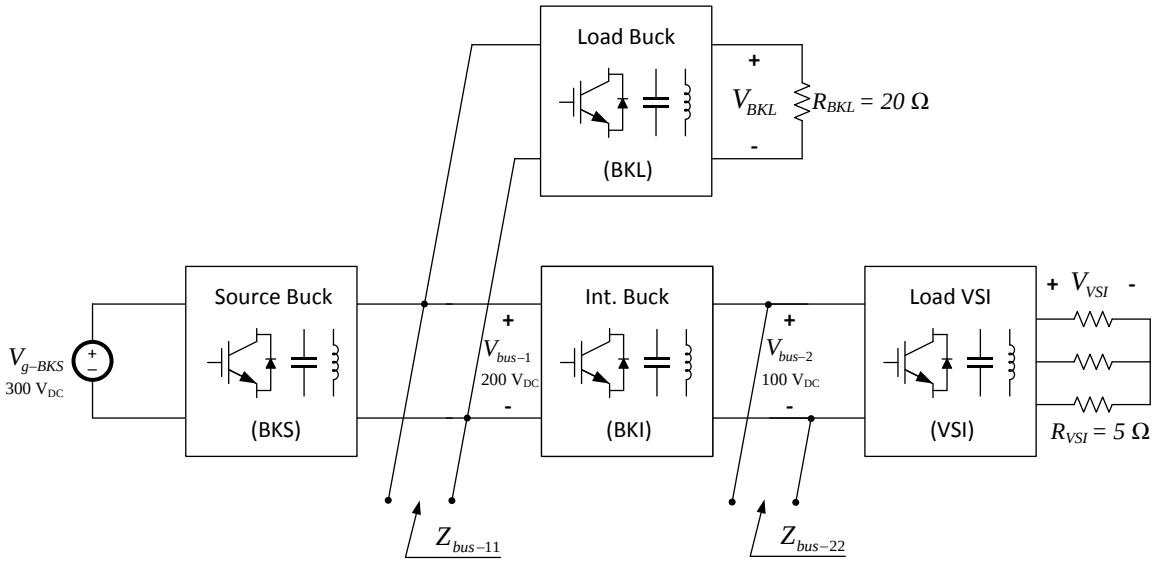


Figure 3.9. Scaled notional multi-bus MVDC distribution system.

Table 3.1. Complete Converter Hardware and Control Parameters

Parameter	**BKS**		**BKL**		**BKI**		**VSI**	
f_{sw}	20 kHz		20 kHz		20 kHz		20 kHz	
L_{filt}	3 mH		1 mH		1 mH		1 mH	
C_{filt}	85 µF		90 µF		90 µF		90 µF	
R_{load}	-		20 Ω		-		5 Ω	
PI Control	**Scen. 1**	**Scen. 2**	**Scen. 1**	**Scen. 2**	**Scen. 1**	**Scen. 2**	**Scen. 1**	**Scen. 2**
$K_{p\text{-}il}$	0.056	0.056	0.022	0.022	0.022	0.022	0.091	0.091
$K_{i\text{-}il}$	62.65	62.65	29.51	29.51	25.60	28.53	171.6	171.6
$K_{p\text{-}v}$	0.045	0.071	0.104	0.104	0.136	0.081	0.084	0.084
$K_{i\text{-}v}$	25.34	23.65	47.81	47.81	52.76	56.42	145.1	145.1

For the development of the analytic system model, the g-parameters of all converters are computed following the establishment of the system operating point. Each converter in the system of Figure 3.9 operates under a PI feedback control strategy such that, in steady-state, each converter output voltage is equal to its associated reference value. Therefore, all steady-state converter operating point currents and duty cycles may be computed according to simple steady-state equivalent circuit models. The computed

g-parameters of each converter are used to construct the complete system matrix G_{sys}, as in (2.59) and given completely in Appendix B (B.53)-(B.57).

3.5.1 Scenario 1 – Prominent Bus 1 Resonance Analytic Design and Evaluation

Table 3.2. Steady-State Operating Point Specifications for Scenario 1

Parameter	Value
$V_{out\text{-}VSI\text{-}d}$	18.26 V
$I_{load\text{-}VSI\text{-}d}$	3.65 A
$D_{d\text{-}VSI}$	0.36
$V_{out\text{-}BKI}$	100 V
$I_{load\text{-}BKI}$	1.00 A
D_{BKI}	0.50
$V_{out\text{-}BKL}$	89.44 V
$I_{load\text{-}BKL}$	4.47 A
D_{BKL}	0.45
$V_{out\text{-}BKS}$	200V
$I_{load\text{-}BKS}$	2.50 A
D_{BKS}	0.67
$V_{q\text{-}BKS}$	300V

For this scenario, the system is operated with the parameters listed in Table 3.1 and Table 3.2 for a prominent Bus 1 resonance. Note that in this scenario, the BKL converter processes 400 W whereas the BKI converter processes 100 W. This causes a resonance on Bus 1. The two analytic bus self-impedances are extracted from the constructed system model operating under feedback control only and plotted in Figure 3.10 and Figure 3.11. The Bus 1 self-impedance $Z_{bus\text{-}11\text{-}FB}$ in Figure 3.10 is shown to be a composite of the SRC output impedance $Z_{out\text{-}SRC\text{-}FB}$ and the input impedances to the BKL and BKI converters, $Z_{in\text{-}BKL\text{-}FB}$ and $Z_{in\text{-}BKI\text{-}VSI\text{-}FB}$, respectively. Note that the BKI converter is loaded by the VSI. To visually simplify the interaction about the resonance, recall that the bus impedance is composed of the parallel combination of all source converter output

and load converter input impedances present at the bus connection. At Bus 1, there is just one source converter output impedance, $Z_{out\text{-}SRC\text{-}FB}$. The load converter input impedances may be lumped into a single load subsystem impedance (see Figure 3.2) by taking the parallel combination of $Z_{in\text{-}BKL\text{-}FB}$ and $Z_{in\text{-}BKI\text{-}VSI\text{-}FB}$, resulting in the impedance denoted $Z_{in\text{-}BKL\text{-}BKI\text{-}VSI\text{-}FB}$ that is shown in solid red in Figure 3.10. Bus impedance $Z_{bus\text{-}11\text{-}FB}$ is shown to closely match the frequency response of the SRC converter output impedance at high and low frequency. However, within the range of frequencies between approximately 40 Hz and 90 Hz, $Z_{out\text{-}SRC\text{-}FB}$ and $Z_{in\text{-}BKL\text{-}BKI\text{-}VSI\text{-}FB}$ interact due to their comparable magnitude, resulting in decreased damping and a prominent resonance appearing in the bus self-impedance.

Interaction of the source converter output impedance and load converter input impedance is much less apparent on Bus 2, Figure 3.11. The source converter output impedance for Bus 2 is $Z_{out\text{-}BKS\text{-}BKL\text{-}BKI\text{-}FB}$. Note that the BKI converter is fed from the SRC converter and also experiences source interactions with the BKL converter. The load input impedance for Bus 2 is $Z_{in\text{-}VSI\text{-}FB}$. The overall bus impedance $Z_{bus\text{-}22\text{-}FB}$ closely matches that of $Z_{out\text{-}BKS\text{-}BKL\text{-}BKI\text{-}FB}$ at all frequencies since the magnitude responses of the source and load subsystem impedances are well separated for the entire observable bandwidth.

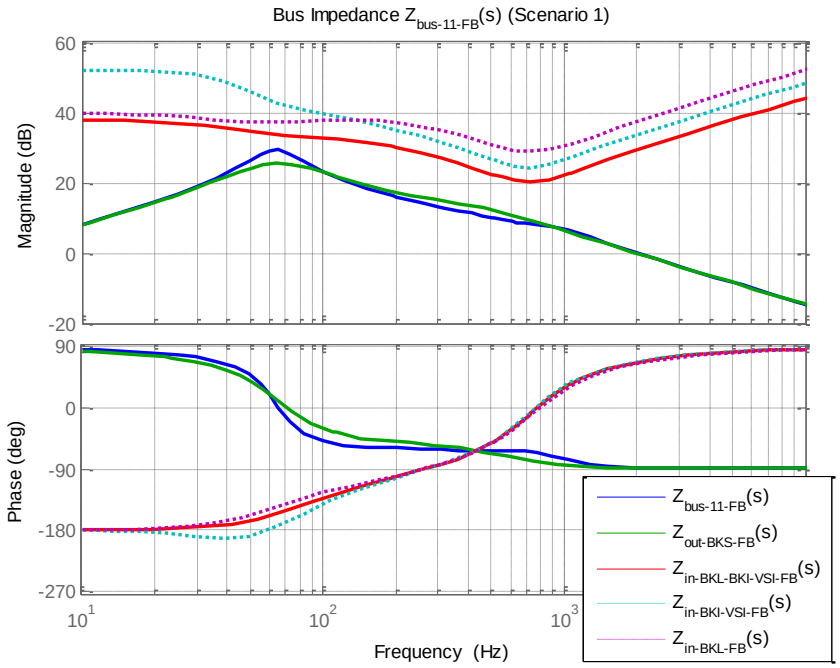


Figure 3.10. Bode plot of Scenario 1 Bus 1 analytic self-impedance and associated source and load converter impedances for system operating under feedback control only.

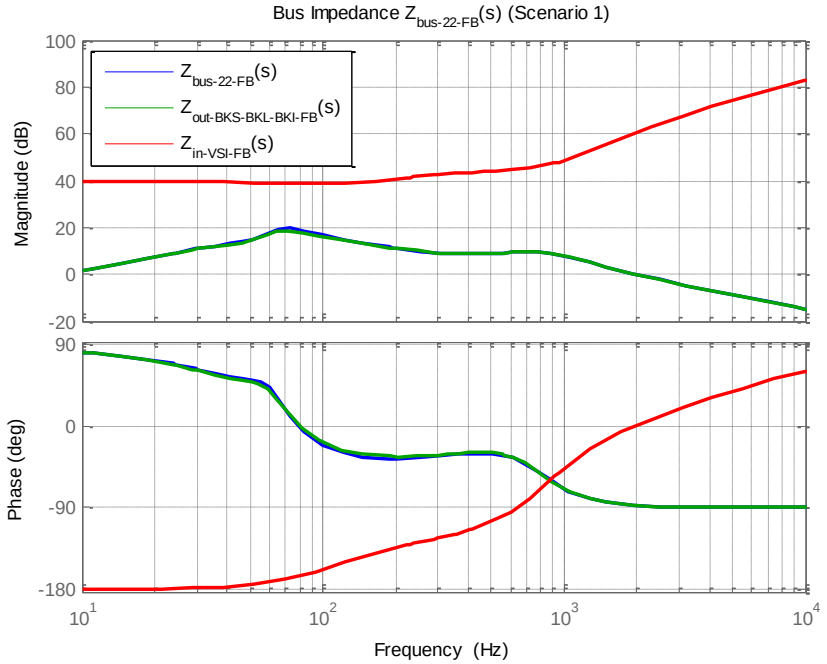


Figure 3.11. Bode plot of Scenario 1 Bus 2 analytic self-impedance and associated source and load converter impedances for system operating under FB control only.

$Z_{bus\text{-}11\text{-}FB}$ and $Z_{bus\text{-}22\text{-}FB}$ are each shown to satisfy the PBSC as set forth in Section 3.1, as each bus self-impedance has a phase between ±90° for all frequencies. However, the interaction present between the source and load converter subsystems connected to Bus 1 has resulted in a noticeable resonance in $Z_{bus\text{-}11\text{-}FB}$ that could be damped through the application of PFF control.

The proposed Allowable Impedance Region analysis technique is now applied for this system. First, the bus impedances under study are normalized to eliminate the effect of any static gain on the impedance magnitude. This was a straightforward task for the simplified bus impedance of (3.3) since the gain $Z_{0\text{-}bus}$ was explicitly stated and the bus impedance was a simple second-order system. In this system, however, the bus impedance contains additional high frequency poles and zeros that obscure the static gain associated with the resonance that dominates the magnitude response.

A simple method to estimate the static gain $Z_{0\text{-}bus}$ of each bus self-impedance for normalization is proposed by again considering the system in (3.3). The low frequency asymptote of (3.3) can be used to form an approximation of $Z_{0\text{-}bus}$, as in (3.12), when the resonant frequency and magnitude of the impedance at a sufficiently low frequency are known. Choosing a low frequency of a decade lower than the resonance ensures that the magnitude is indeed along the low frequency asymptote.

$$Z_{0-bus} \cong \left|Z_{bus-FB}(j\omega)\right| \cdot \frac{\omega_0}{\omega} \quad \text{for} \quad \omega << \omega_0 \tag{3.12}$$

Using the estimation technique of (3.12), the low frequency asymptotes are used to approximate $Z_{0\text{-}bus}$ for each bus self-impedance. For $Z_{bus\text{-}11\text{-}FB}$, $Z_{0\text{-}bus}$ is estimated to be 15.92 Ω (24.04 dBΩ) and for $Z_{bus\text{-}22\text{-}FB}$, $Z_{0\text{-}bus}$ is approximately 7.60 Ω (17.61 dBΩ). The

Nyquist contours of each bus self-impedance normalized by its associated estimated static gain are plotted in Figure 3.12.

For this system, it is desired that the resonance of each bus have a minimum desired damping factor ζ_{min} of 0.5 to ensure good dynamic performance. The Allowable Impedance Region according to (3.5) is depicted as the semicircle of unit radius in Figure 3.12 (solid red). Note that the contour of each bus self-impedance is not constrained to the specified impedance region and extends past the semicircular boundary, indicating that the system is lightly damped and will likely exhibit oscillations in response to a disturbance. Since the contour of $Z_{bus\text{-}11\text{-}FB\text{-}N}$ has the largest magnitude, and therefore the least damping, the PFF controller is designed to act directly on Bus 1 and is implemented by the BKL converter. The PFF controller design according to (3.10)-(3.11) is summarized in Table 3.3.

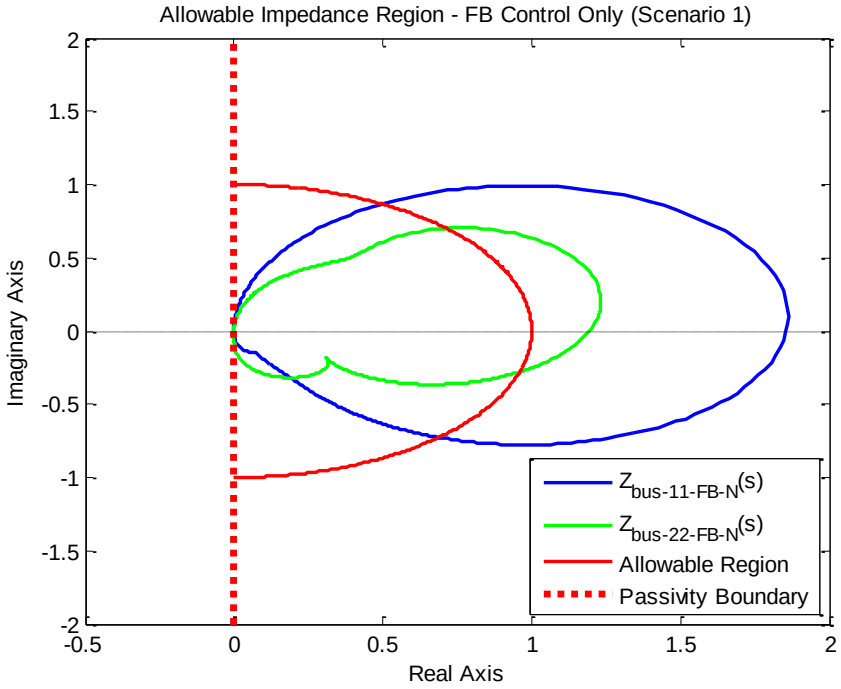


Figure 3.12. Nyquist plot of Scenario 1 normalized analytic bus impedances and Allowable Impedance Region (ζ_{min} = 0.5) for system operating under FB control only.

Table 3.3. Bus 1 Impedance and PFF Control Design Summary (Scenario 1)

Parameter	Value
$f_{0\text{-}bus\text{-}11\text{-}FB}$	63.76 Hz
$\zeta_{bus\text{-}11\text{-}FB}$	0.240
K_m	0.250
ζ_{damp}	1.000
$Z_{0\text{-}damp}$	9.328 Ω (19.40 dBΩ)

The design of Table 3.3 results in an equivalent series *RLC* virtual damping impedance placed in parallel with the BKL input terminals where R_b = 18.66 Ω, L_b = 23.29 mH, and C_b = 267.5 μF. Bode plots of the analytic bus self-impedances and associated converter input and output impedances verify the improved damping resulting from the PFF control design, Figure 3.13 and Figure 3.14. Note how the PFF control modifies the input impedance to the BKL converter in the range of frequencies about the original $Z_{bus\text{-}11\text{-}FFFB}$ resonance. In particular, the phase of $Z_{in\text{-}BKL\text{-}FFFB}$ is approximately 0° at the resonance such that the BKL input impedance behaves as a resistive element. The overall effect is to improve the damping of the bus impedance, eliminating the potential for undesirable oscillations.

The Nyquist contours of the normalized analytic bus self-impedances under PFF control, $Z_{bus\text{-}11\text{-}FFFB\text{-}N}$ and $Z_{bus\text{-}22\text{-}FFFB\text{-}N}$, are shown in Figure 3.15. $Z_{bus\text{-}11\text{-}FFFB\text{-}N}$ now lies within the Allowable Impedance Region and is expected to provide good dynamic performance in response to disturbances. The addition of PFF control via the BKL converter has significantly improved the damping on Bus 1. Note that the Nyquist contour of $Z_{bus\text{-}22\text{-}FFFB\text{-}N}$ also lies within the Allowable Impedance Region, as the PFF control enacted on Bus 1 has also resulted in an improvement of the Bus 2 damping.

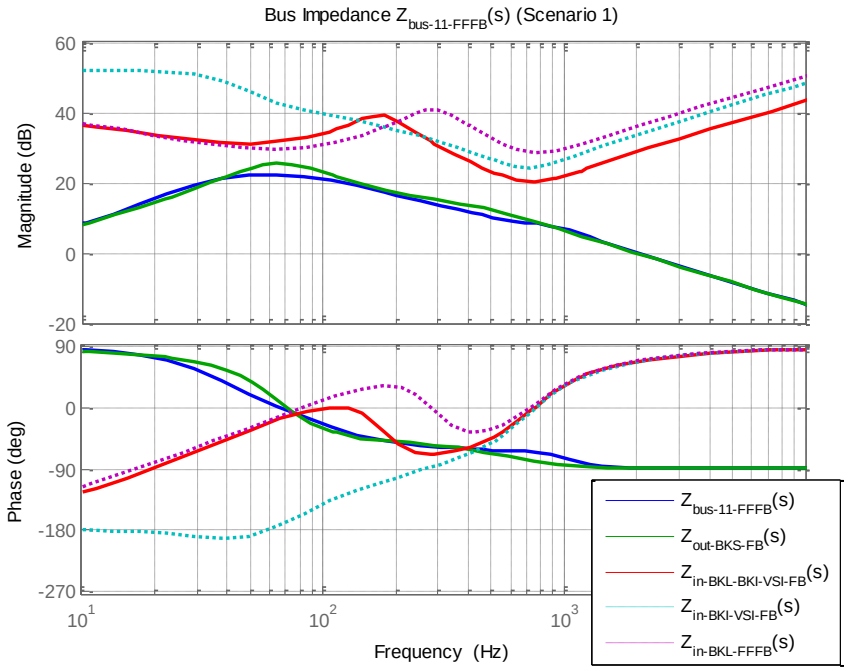


Figure 3.13. Bode plot of Scenario 1 Bus 1 analytic self-impedance and associated source and load converter impedances for system operating under FFFB control.

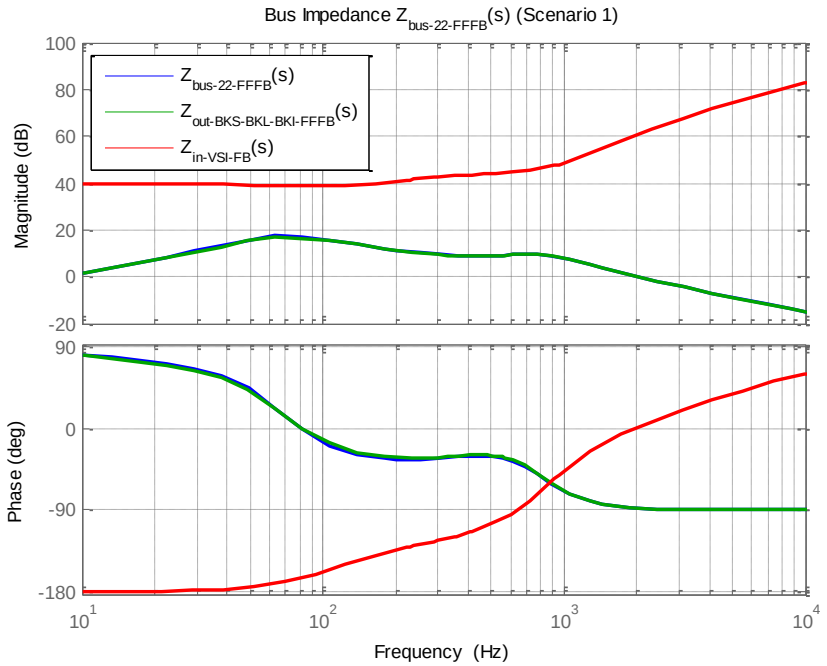


Figure 3.14. Bode plot of Scenario 1 Bus 2 analytic self-impedance and associated source and load converter impedances for system operating under FFFB control.

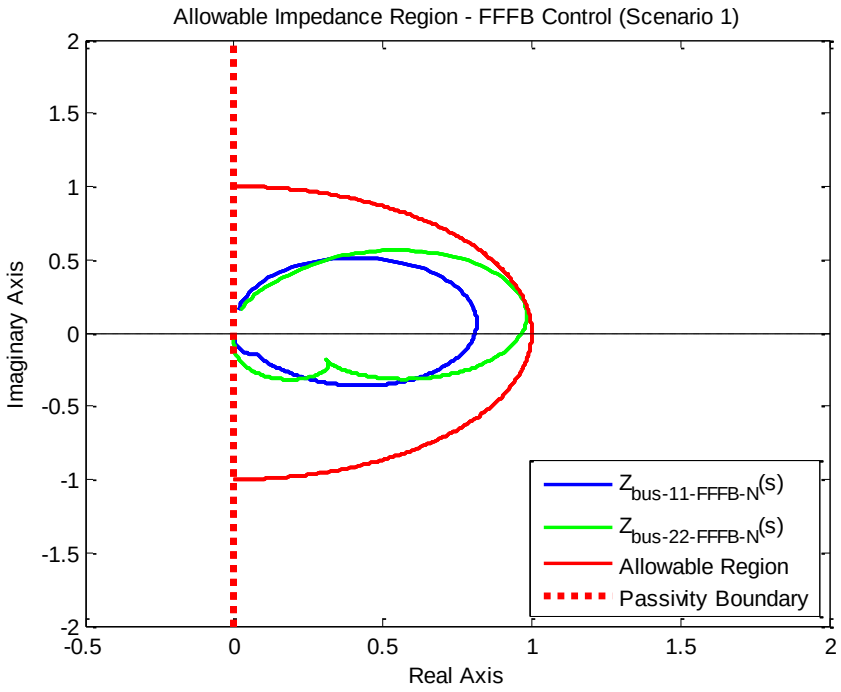


Figure 3.15. Nyquist plot of Scenario 1 normalized analytic bus impedances and Allowable Impedance Region (ζ_{min} = 0.5) for system operating under FFFB control.

3.5.2 Scenario 2 – Prominent Bus 2 Resonance Analytic Design and Evaluation

Table 3.4. Steady-State Operating Point Specifications for Scenario 2

Parameter	Value
$V_{out\text{-}VSI\text{-}d}$	36.51 V
$I_{load\text{-}VSI\text{-}d}$	7.30 A
$D_{d\text{-}VSI}$	0.72
$V_{out\text{-}BKI}$	100 V
$I_{load\text{-}BKI}$	4.00 A
D_{BKI}	0.50
$V_{out\text{-}BKL}$	44.72 V
$I_{load\text{-}BKL}$	2.24 A
D_{BKL}	0.22
$V_{out\text{-}BKS}$	200V
$I_{load\text{-}BKS}$	2.50 A
D_{BKS}	0.67
$V_{g\text{-}BKS}$	300V

For this scenario, the system is operated with the parameters listed in Table 3.4 for a prominent Bus 2 resonance. Note that in this scenario, the BKL converter processes 100 W whereas the BKI converter processes 400 W, causing a resonance on Bus 2. The two analytic self-bus impedances are extracted from the constructed system model operating under feedback control only and plotted in Figure 3.16 and Figure 3.17. The Bus 1 self-impedance $Z_{bus\text{-}11\text{-}FB}$ shown in Figure 3.16 is shown to have only slightly decreased damping as a result of interaction with the BKL and BKI input impedances. In this scenario, the BKL is a relatively light load compared to the power processed by the downstream BKI-VSI system. As a result, the composite load subsystem impedance $Z_{in\text{-}BKL\text{-}BKI\text{-}VSI\text{-}FB}$ for Bus 1 is dominated by impedance $Z_{in\text{-}BKI\text{-}VSI\text{-}FB}$. The load subsystem and BKS output impedance $Z_{bus\text{-}BKS\text{-}FB}$ are well separated in this case, such that the overall Bus 1 impedance $Z_{bus\text{-}11\text{-}FB}$ matches the SRC output impedance except for a slightly increased resonance around 70 Hz.

Interaction of the source converter output impedance and load converter input impedance is much more significant on Bus 2, Figure 3.17. The VSI converter heavily loads the BKI converter, such that its input impedance $Z_{in\text{-}VSI\text{-}FB}$ now interacts with the Bus 2 source subsystem output impedance $Z_{out\text{-}BKS\text{-}BKL\text{-}BKI\text{-}FB}$. Bus self-impedance $Z_{bus\text{-}22\text{-}FB}$ closely matches $Z_{out\text{-}BKS\text{-}BKL\text{-}BKI\text{-}FB}$ at high and low frequencies, but exhibits a significant resonance in the range of 50 Hz to 100 Hz as a result of the impedance interactions.

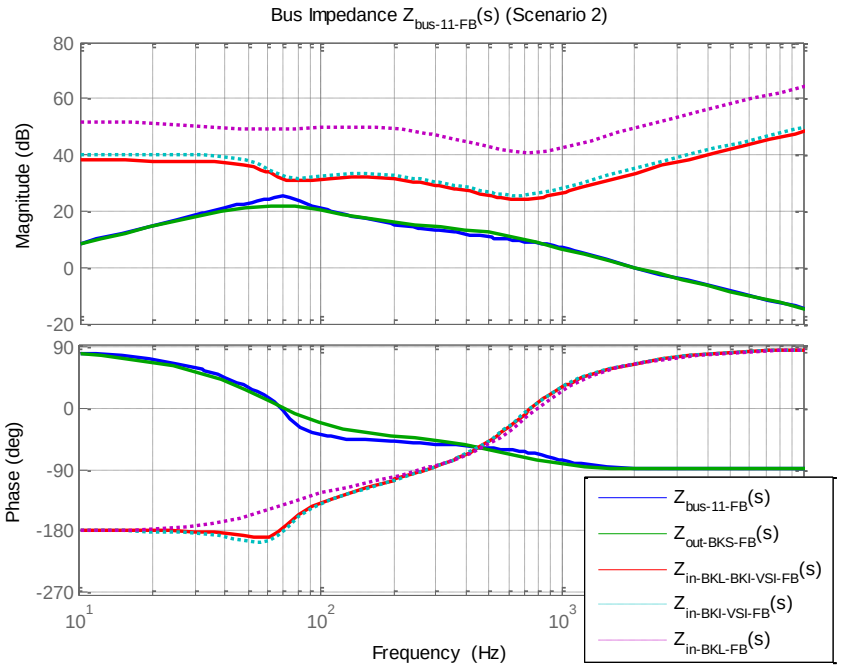


Figure 3.16. Bode plot of Scenario 2 Bus 1 analytic self-impedance and associated source and load converter impedances for system operating under FB control only.

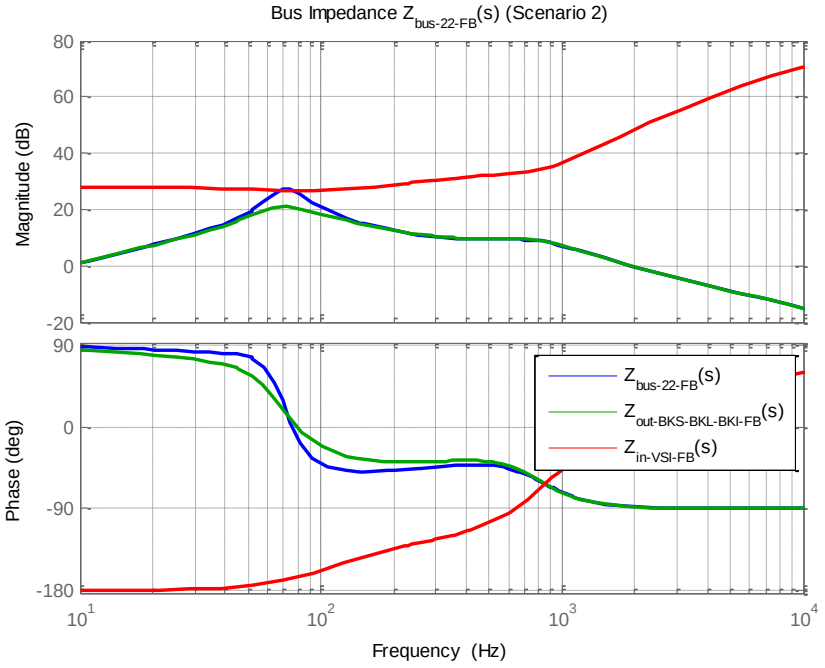


Figure 3.17. Bode plot of Scenario 2 Bus 2 analytic self-impedance and associated source and load converter impedances for system operating under FB control only.

Both $Z_{bus\text{-}11\text{-}FB}$ and $Z_{bus\text{-}22\text{-}FB}$ satisfy the PBSC as set forth in Section 3.1, as each bus self-impedance has a phase between ±90° for all frequencies. However, the impedance interaction between $Z_{out\text{-}BKS\text{-}BKL\text{-}BKI\text{-}FB}$ and $Z_{in\text{-}VSI\text{-}FB}$ leading to the resonance present in $Z_{bus\text{-}22\text{-}FB}$ will likely lead to oscillatory behavior that can be damped through application of PFF control.

The Scenario 2 system is now evaluated using the proposed Allowable Impedance Region analysis technique. Using the estimation technique of (3.12), the low frequency asymptotes are used to approximate $Z_{0\text{-}bus}$ for each bus self-impedance. For $Z_{bus\text{-}11\text{-}FB}$, $Z_{0\text{-}bus}$ is estimated to be 19.02 Ω (25.58 dBΩ) and for $Z_{bus\text{-}22\text{-}FB}$, $Z_{0\text{-}bus}$ is approximately 7.97 Ω (18.03 dBΩ). The Nyquist contours of each bus self-impedance normalized by its associated estimated static gain are plotted against the Allowable Impedance Region for ζ_{min} of 0.5 in Figure 3.18.

In this scenario, only $Z_{bus\text{-}22\text{-}FB}$ is shown to violate Allowable Impedance Region, extending past the boundary set by (3.5) into the RHP. Bus self-impedance $Z_{bus\text{-}11\text{-}FB}$ is wholly contained within the specified region and requires no additional damping to ensure the desired system performance. Accordingly, the PFF controller is designed to act directly on Bus 2 and is implemented by the VSI. The PFF controller design according to (3.10)-(3.11) is summarized in Table 3.5.

Table 3.5. Bus 2 Impedance and PFF Control Design Summary (Scenario 2)

Parameter	Value
$f_{0\text{-}bus\text{-}22\text{-}FB}$	71.21 Hz
$\zeta_{bus\text{-}22\text{-}FB}$	0.167
K_m	0.250
ζ_{damp}	1.000
$Z_{0\text{-}damp}$	4.000 Ω (12.04 dBΩ)

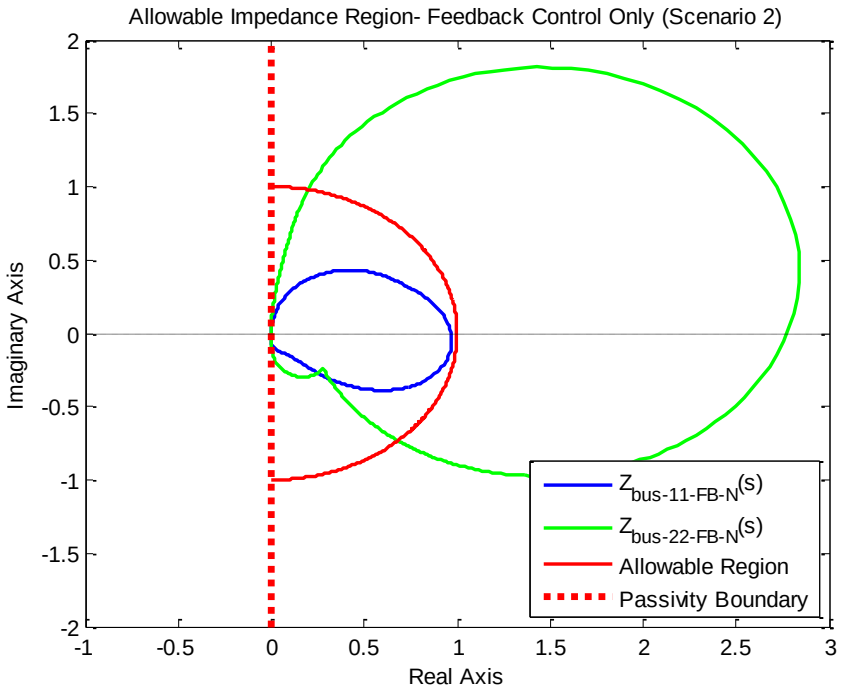


Figure 3.18. Nyquist plot of Scenario 2 normalized analytic bus impedances and Allowable Impedance Region (ζ_{min} = 0.5) for system operating under FB control only.

The PFF control design for Bus 2 in Table 3.5 results in an equivalent series *RLC* virtual damping impedance placed in parallel with the BKL input terminals where R_b = 8.001 Ω, L_b = 8.942 mH, and C_b = 558.7 µF. Bode plots of the analytic bus self-impedances and associated converter input and output impedances verify the improved damping on Bus 2 resulting from the PFF control design, Figure 3.19 and Figure 3.20. Application of PFF control modifies the VSI input impedance $Z_{in\text{-}VSI\text{-}FFFB}$ such that that the VSI input impedance appears resistive at the resonance, resulting in greatly improved bus impedance damping.

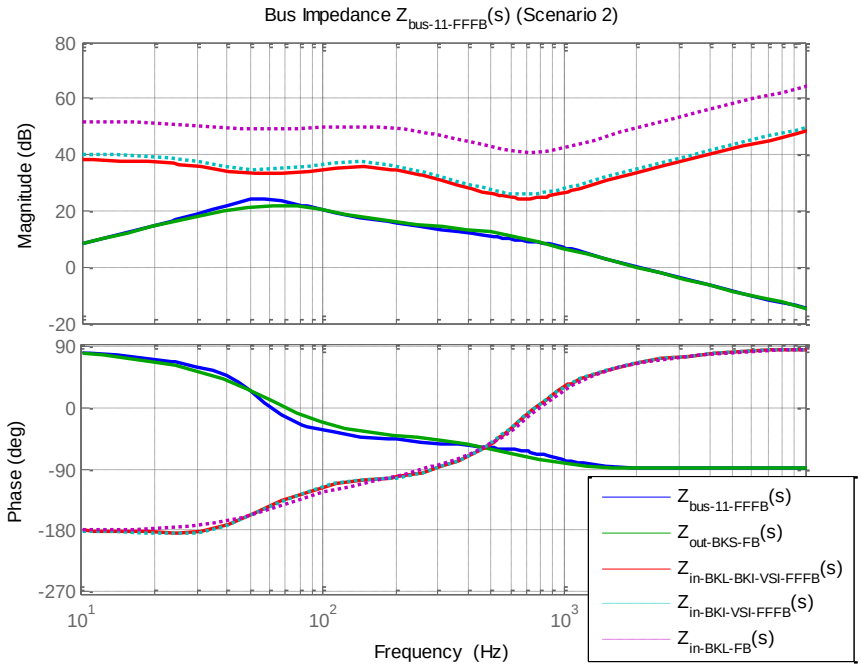


Figure 3.19. Bode plot of Scenario 2 Bus 1 analytic self-impedance and associated source and load converter impedances for system operating under FFFB control.

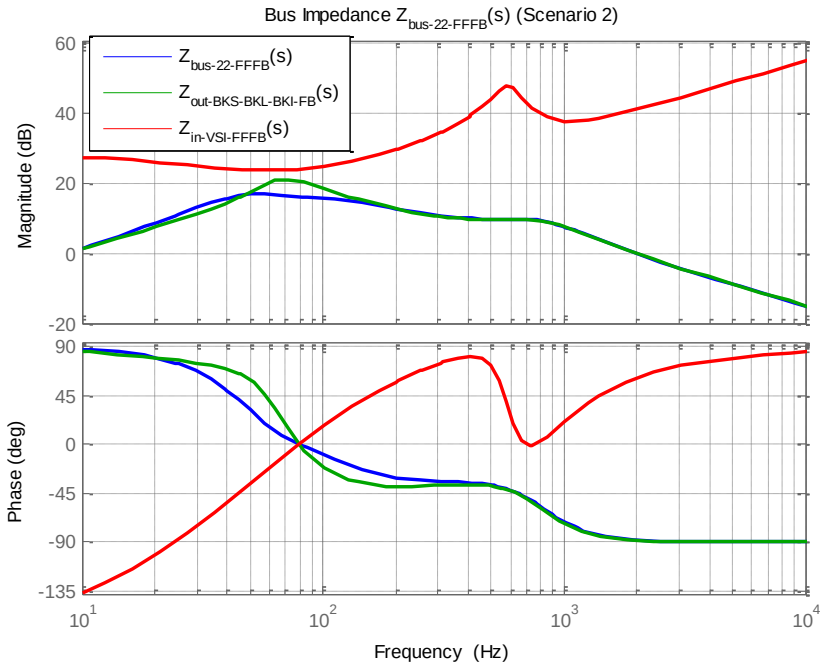


Figure 3.20. Bode plot of Scenario 2 Bus 2 analytic self-impedance and associated source and load converter impedances for system operating under FFFB control.

The Nyquist contours of the normalized analytic bus self-impedances under PFF control, $Z_{bus\text{-}11\text{-}FFFB\text{-}N}$ and $Z_{bus\text{-}22\text{-}FFFB\text{-}N}$, are plotted against the Allowable Impedance Region in Figure 3.21. $Z_{bus\text{-}22\text{-}FFFB\text{-}N}$ now lies within the Allowable Impedance Region as a result of the PFF control implementation within the VSI. The contour of $Z_{bus\text{-}11\text{-}FB}$ is also positively affected by the PFF controller, moving further inside the allowable region, which indicates increased damping, such that the entire system can be expected to provide good dynamic performance.

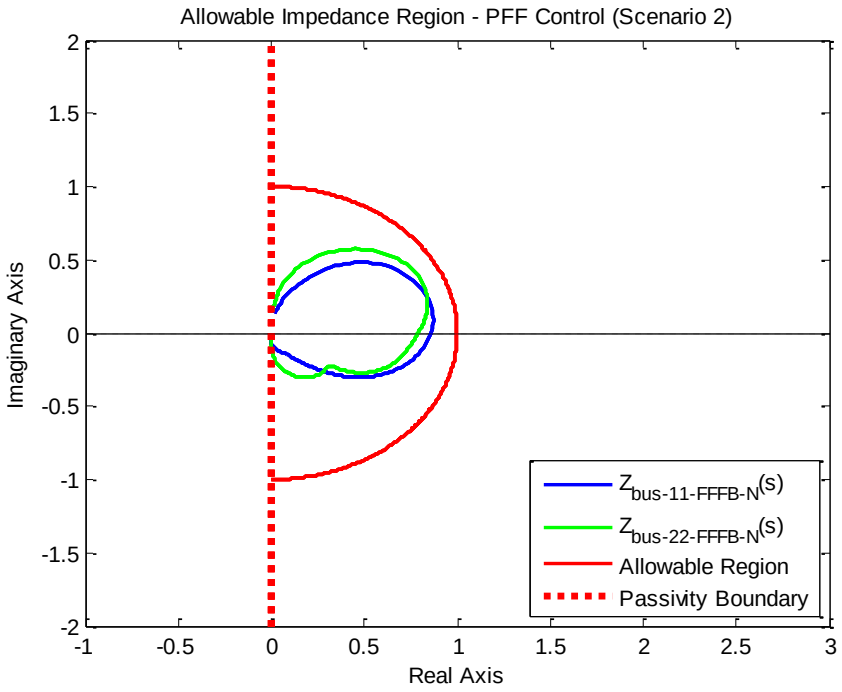


Figure 3.21. Nyquist plot of Scenario 2 normalized analytic bus impedances and Allowable Impedance Region (ζ_{min} = 0.5) for system operating under FFFB control.

3.6 Conclusion of Converter System Stability, Evaluation, and Analytic Design

In this chapter, the PBSC is extended to the multi-bus converter system case and applied to analyze the passivity of each interacting bus self-impedance present within the

MVDC system. A new technique to evaluate the damping of the system bus impedances alongside application of the PBSC is proposed. Developed from a simplified representative model, an Allowable Impedance Region is defined in the *s*-plane for the evaluation of system bus impedance damping. A method to normalize the system bus impedance is proposed to allow for extrapolation of the damping factor information. This information aids in the design of the PFF control, which can now be designed to ensure that the bus impedance Nyquist contour is contained within the boundaries of the Allowable Impedance Region for a specified minimum level of damping.

An adaptive scheme to apply the Allowable Impedance Region analysis technique and simplified PFF control design is also proposed in recognition that the notional MVDC converter-based distribution network is likely to be a highly dynamic system that experiences frequent operating point changes in response to cycling of power generation sources, load profile changes, and other system fluctuations.

The multi-bus converter system model developed at the end of Chapter 2 is analytically studied using the proposed techniques for two test scenarios involving the presence of a resonance localized either on Bus 1 or Bus 2. The Allowable Impedance Region and PFF control design techniques are shown to be successful in damping the observed resonances through the introduction of virtual damping impedances at the input terminals of the load subsystems. Validation of these proposed techniques in simulation and experiment is provided in the next chapter.

CHAPTER 4

SIMULATION AND EXPERIMENTAL RESULTS FOR MULTI-BUS STABILITY AND PERFORMANCE ENHANCEMENTS

This chapter provides simulation and experimental validation of the modeling, stability analysis, and control design techniques presented previously in Chapters 2 and 3. A notional two-bus MVDC power system consisting of four switching power converters is simulated in MATLAB/Simulink. Full switching models are implemented to provide a more realistic representation of the eventual experimental setup. In the laboratory, a system having the same specifications is constructed using custom built IGBT-based switching converter modules and two digital control platforms. The simulated and experimental systems are initially evaluated in the frequency domain using a wideband impedance identification technique to validate the unterminated two-port modeling technique presented in Chapter 2. Both frequency and time domain results are then used to validate the efficacy of the PBSC, AIR, and PFF control design techniques of Chapter 3 in ensuring the stability and enhancing the performance of the system.

Two different test scenarios are considered in simulation and experiment in which both system bus self-impedances are deemed passive at all frequencies but require additional damping to meet the requirements of the AIR as proposed in Chapter 3. The first scenario investigates the stability analysis and PFF control design for a system exhibiting a prominent resonance on Bus 1. In the second scenario, the resonance is more

pronounced on Bus 2, requiring that the PFF control be implemented differently. For both scenarios, the modeling, analysis, and control design techniques are shown to be highly effective in evaluating the performance and improving the dynamic response of the system.

Finally, the adaptive PFF control design technique is applied to both experimental system scenarios, demonstrating that the bus self-impedance models created using the wideband impedance identification technique may be used for online stability analysis and PFF control design of a "black-box" system, where no information is explicitly available regarding the system parameters. The frequency and time domain results show that the dynamic performance enhancements are very similar to those obtained for the system for which all parameters are known. This provides an interesting alternative approach for stabilizing control design based on experimental impedance characterization rather than system modeling.

4.1 Simulation Results

Figure 4.1 shows the top level diagram of the full switching model of the notional multi-bus MVDC distribution system as constructed using the PLECS block-set for Simulink. PLECS is a software simulator similar to Simulink that is especially well-suited for the simulation of switching converters. The optimized solver significantly decreases the simulation time of models consisting of numerous switching converters by using idealized switch models and a piecewise linear computation algorithm. The top level diagram depicts the four switching converters interconnected to form a distribution system with two distinct buses. The subsystem models and control system block diagrams for all converters are located in Appendix C.

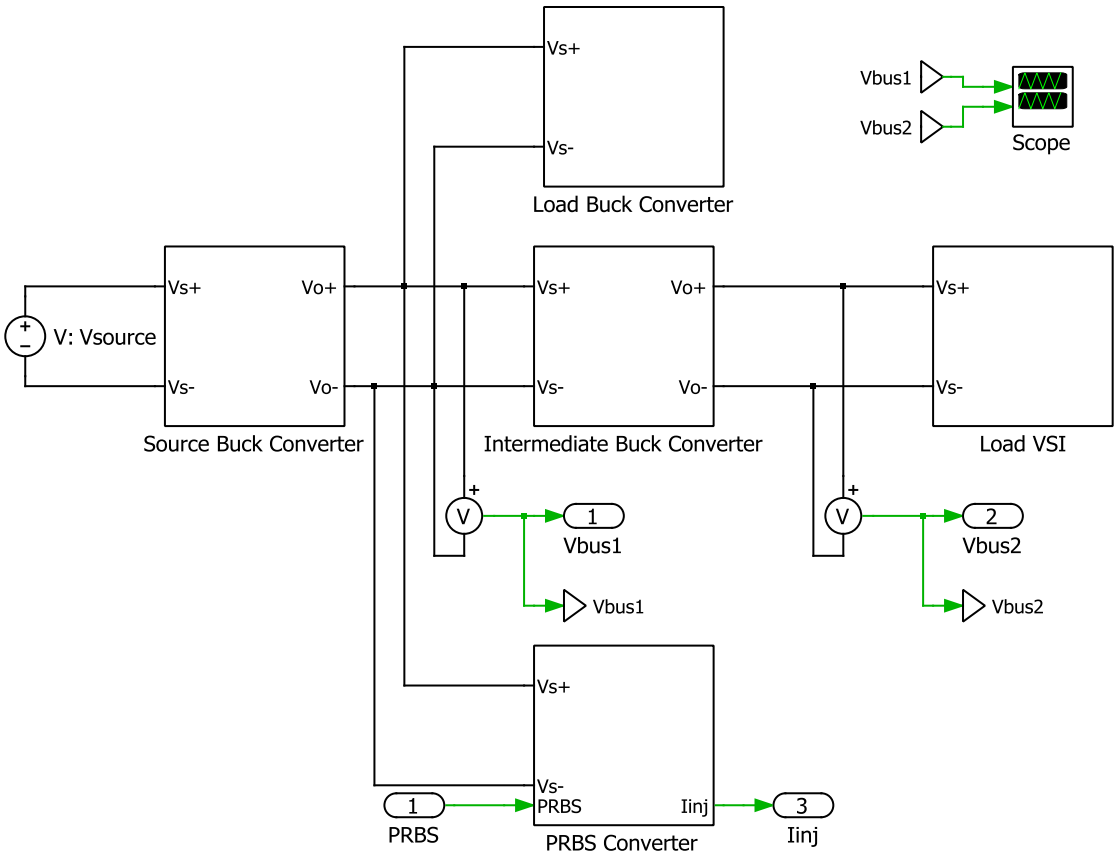


Figure 4.1. PLECS diagram of scaled notional multi-bus MVDC distribution system

An additional converter connected to the system, labeled PRBS Converter in Figure 4.1, is used as a perturbation source to excite each system bus individually with a 14-bit (16,383 terms) 20 kHz PRBS signal and allow for wideband measurements of the bus impedances while the system is operating in steady-state. This converter sinks only a few percent of the nominal system operating power (12 W or approximately 2.5%) such that interaction of its impedance with the system bus impedances, which may lead to unintentionally reduced damping, is avoided. The PRBS converter is a full-bridge buck converter that uses a unipolar modulation scheme, effectively doubling the ripple current frequency to 40 kHz (20 kHz switching frequency). The current injected into the system

buses and the bus voltages are oversampled at a rate of 2 MHz to improve the high frequency accuracy of the estimation data.

4.1.1 SCENARIO 1 – PROMINENT BUS 1 RESONANCE

The system of Figure 4.1 consists of two buses, and thus has four total bus impedances. The non-parametric bus impedance data is plotted against the analytical models in Figure 4.2 through Figure 4.5. The estimation data and analytic models demonstrate good matching for the entire observable bandwidth, validating the unterminated two-port modeling approach proposed in Chapter 2 and the previously described stability analysis and PFF control design. The impedances $Z_{bus\text{-}12}$ and $Z_{bus\text{-}21}$ are displayed solely to show that the two-port modeling technique provides accurate models for constructing the complete analytic bus impedance matrix, as in (3.1), and are not used in the stability analysis or stabilizing control design.

In this scenario, both bus self-impedances $Z_{bus\text{-}11\text{-}FB}$, Figure 4.7, and $Z_{bus\text{-}22\text{-}FB}$, Figure 4.10, are shown to be passive for all observable frequencies, having a phase between ±90°. However, the bus 1 self-impedance $Z_{bus\text{-}11\text{-}FB}$ is shown to exhibit a significant resonance at low frequency, as predicted by the previous analysis due to interaction between the source and load converter subsystems. The PFF control enacted on Bus 1 by the BKL converter significantly damps the resonance, as observed in the $Z_{bus\text{-}11\text{-}FFFB}$ frequency response. The resonance present in $Z_{bus\text{-}22\text{-}FB}$ was determined earlier to be of lesser concern and no PFF control was designed to act directly on Bus 2. However, additional damping is observed about the resonance in $Z_{bus\text{-}22\text{-}FFFB}$ as a result of the PFF implementation in the BKL converter, Figure 4.5.

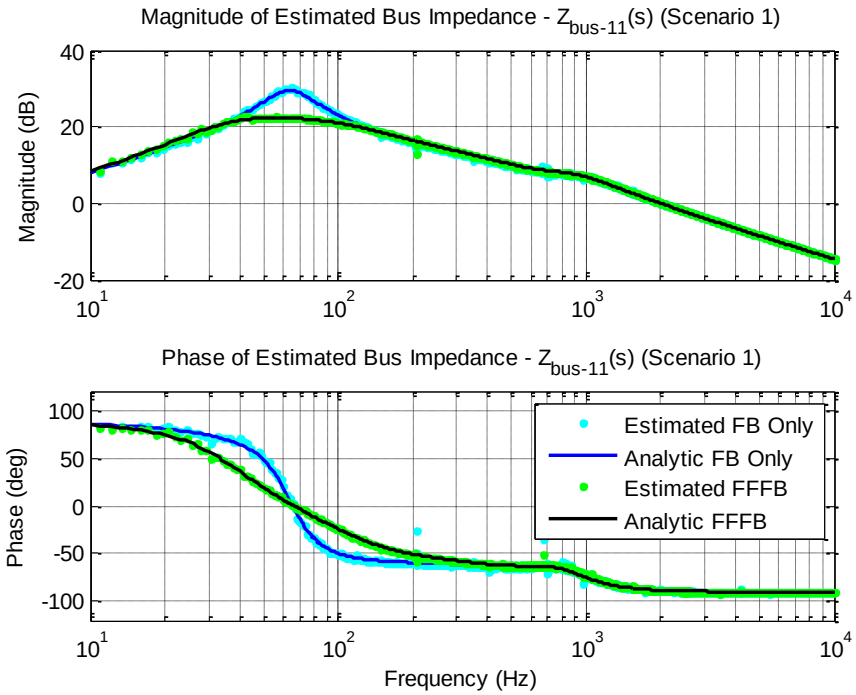


Figure 4.2. Bode plot of simulated Scenario 1 bus self-impedance Z_{bus-11} non-parametric estimation and analytic model for system operating under FB and FFFB control.

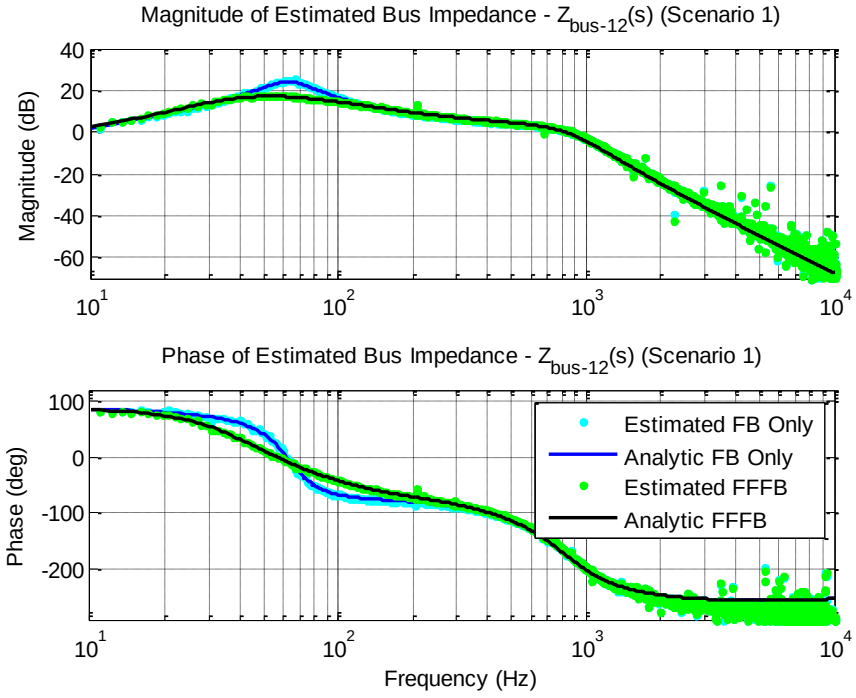


Figure 4.3. Bode plot of simulated Scenario 1 bus cross-impedance Z_{bus-12} non-parametric estimation and analytic model for system operating under FB and FFFB control.

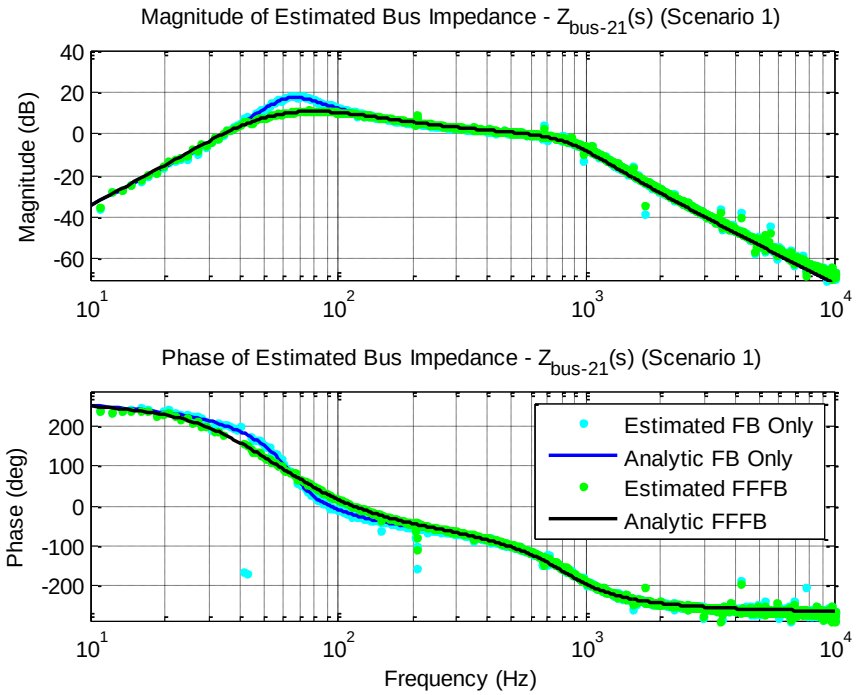


Figure 4.4. Bode plot of simulated Scenario 1 bus cross-impedance $Z_{bus\text{-}21}$ non-parametric estimation and analytic model for system operating under FB and FFFB control.

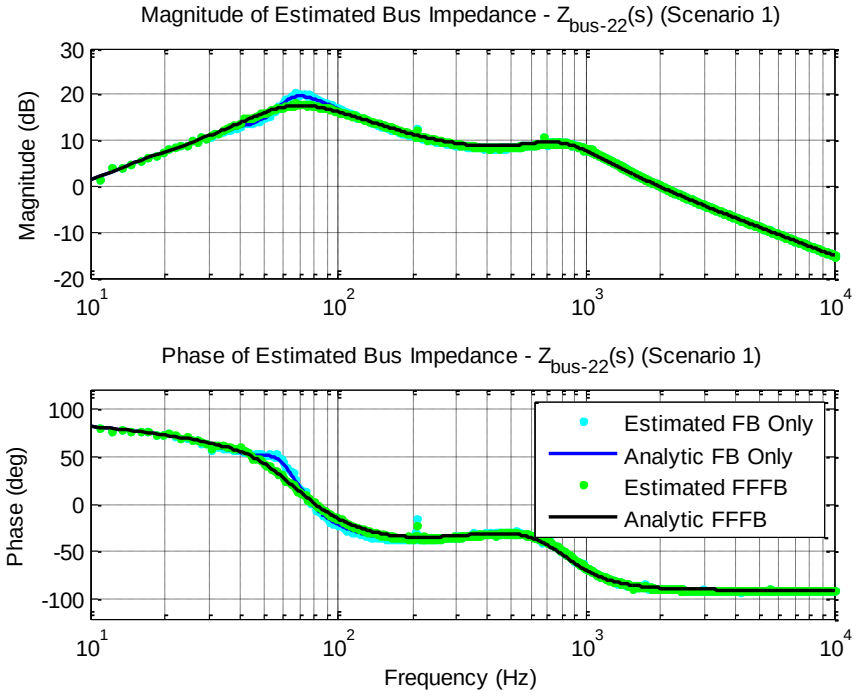


Figure 4.5. Bode plot of simulated Scenario 1 bus self-impedance $Z_{bus\text{-}22}$ non-parametric estimation and analytic model for system operating under FB and FFFB control.

Time domain simulation, Figure 4.6, reveals that the system operating under FB control only exhibits lightly damped oscillations on Bus 1 in response to a step change in the BKL output voltage reference from 67 V_{DC} to 89.44 V_{DC} (75% to 100% full output voltage), as predicted by the AIR analysis. These oscillations are well damped in the FFFB control case, as the virtual impedance introduced by the PFF controller dominates the bus impedance behavior about the resonance, markedly improving the system's dynamic response. Oscillations are also present on Bus 2 in response to the BKL reference step when the system is operated with FB control only, but are much smaller in amplitude. The PFF controller is also shown to be effective in improving the damping on Bus 2.

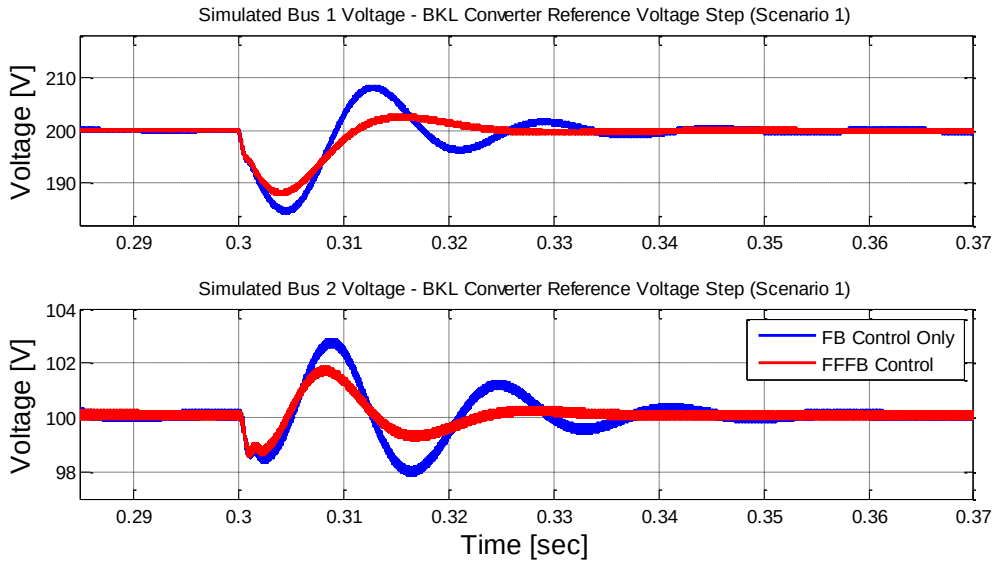


Figure 4.6. Time domain simulation of Scenario 1 MVDC bus voltages under (blue) FB control only and (red) FFFB control during BKL voltage reference step.

4.1.2 SCENARIO 2 – PROMINENT BUS 2 RESONANCE

In this scenario, the scaled notional multi-bus MVDC distribution system of Figure 4.1 exhibits a prominent resonance on Bus 2. The non-parametric bus impedance data is plotted against the analytical models in Figure 4.7 through Figure 4.10. The estimation data and analytic models demonstrate good matching for the entire observable bandwidth, again validating the unterminated two-port modeling approach proposed in Chapter 2 and the previously described stability analysis and PFF control design in providing additional bus impedance damping. The impedances $Z_{bus\text{-}12}$ and $Z_{bus\text{-}21}$ are not used in the stability analysis or stabilizing control design and are displayed solely to show that the two-port modeling technique provides accurate models for constructing the complete analytic bus impedance matrix.

Both bus self-impedances $Z_{bus\text{-}11\text{-}FB}$, Figure 4.7, and $Z_{bus\text{-}22\text{-}FB}$, Figure 4.10, are shown to be passive for all observable frequencies, having a phase between ±90°. However, $Z_{bus\text{-}22\text{-}FB}$ is shown to exhibit a significant resonance at low frequency, due to interaction between the source and load converter subsystems. The PFF control enacted on Bus 2 by the VSI converter damps the resonance significantly, as observed in $Z_{bus\text{-}22\text{-}FFFB}$ frequency response. The resonance present in $Z_{bus\text{-}11\text{-}FB}$ was determined earlier to be insignificant and no PFF control was designed to act directly on Bus 1. However, additional damping is observed about the resonance in $Z_{bus\text{-}11\text{-}FFFB}$ as a result of the PFF implementation in the VSI converter.

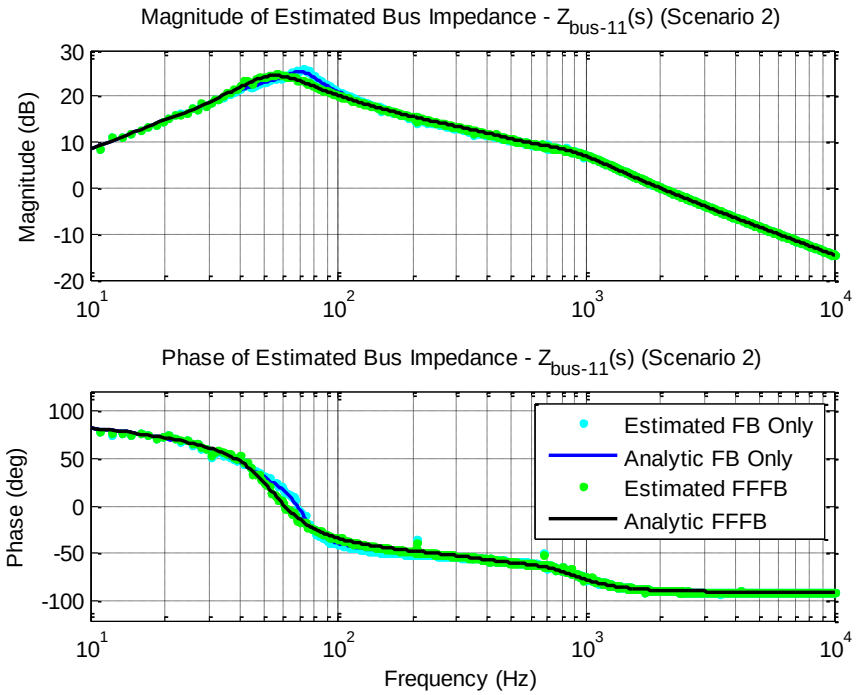


Figure 4.7. Bode plot of simulated Scenario 2 bus self-impedance $Z_{bus\text{-}11}$ non-parametric estimation and analytic model for system operating under FB and FFFB control.

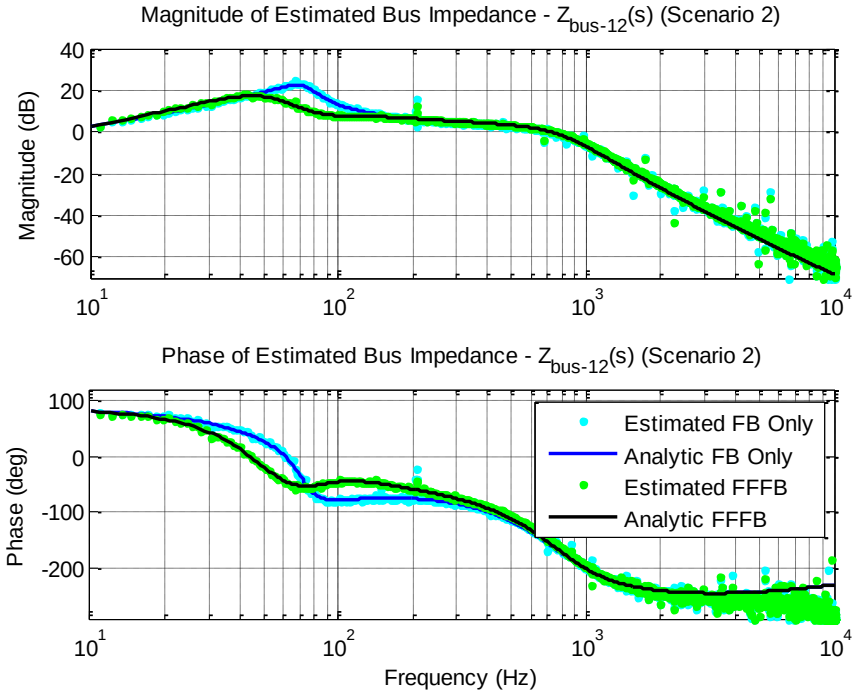


Figure 4.8. Bode plot of simulated Scenario 2 bus self-impedance $Z_{bus\text{-}12}$ non-parametric estimation and analytic model for system operating under FB and FFFB control.

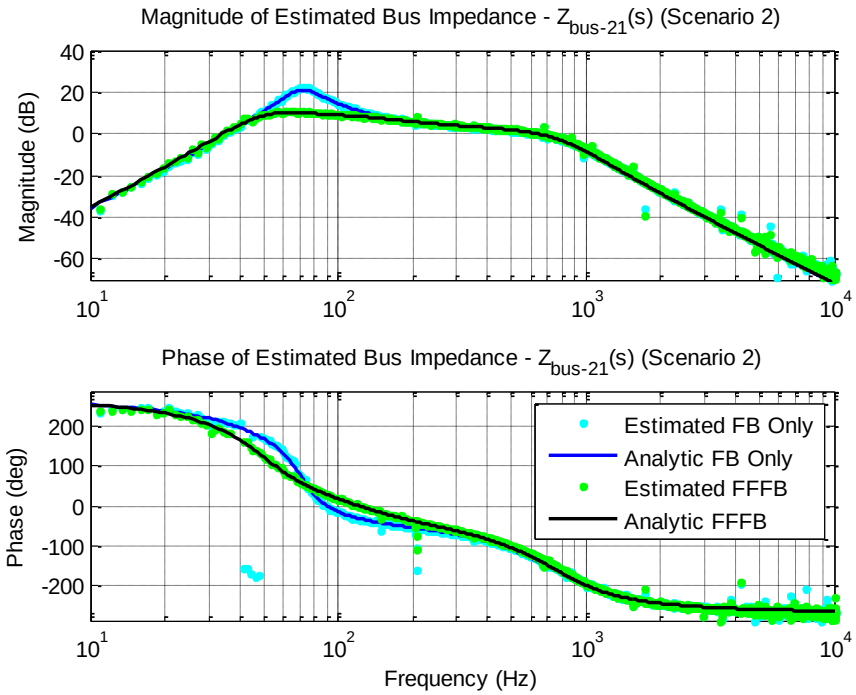


Figure 4.9. Bode plot of simulated Scenario 2 bus self-impedance $Z_{bus\text{-}21}$ non-parametric estimation and analytic model for system operating under FB and FFFB control.

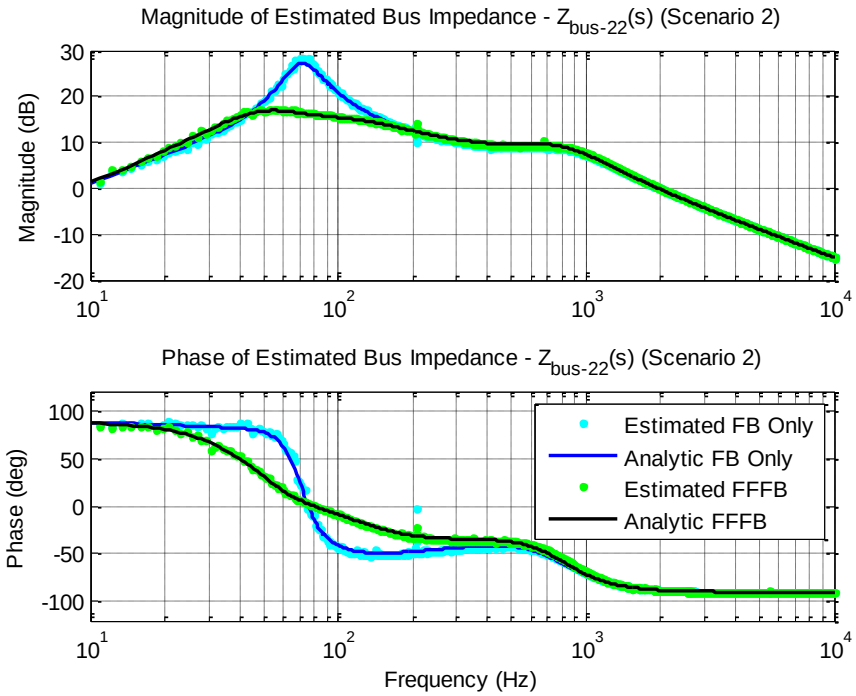


Figure 4.10. Bode plot of simulated Scenario 2 bus self-impedance $Z_{bus\text{-}22}$ non-parametric estimation and analytic model for system operating under FB and FFFB control.

Lightly damped oscillations on Bus 2 in response to a step change in the VSI output voltage reference from 18.26 V_{PK} to 36.51 V_{PK} (50% to 100% full output voltage) are observed via time domain simulation of the system operating under FB control only, Figure 4.11. This behavior is expected, as the previous analysis showed that the Bus 2 Nyquist contour extended past the AIR boundary set for a minimum damping factor of ζ_{min} = 0.5. In the FFFB control case, these oscillations are well damped, as the virtual damping impedance dominates the bus impedance behavior about the resonance. Note that the oscillations present on Bus 1 when the system is operated with FB control only are also more damped when the PFF control is implemented, such that the dynamic response of both buses is significantly improved.

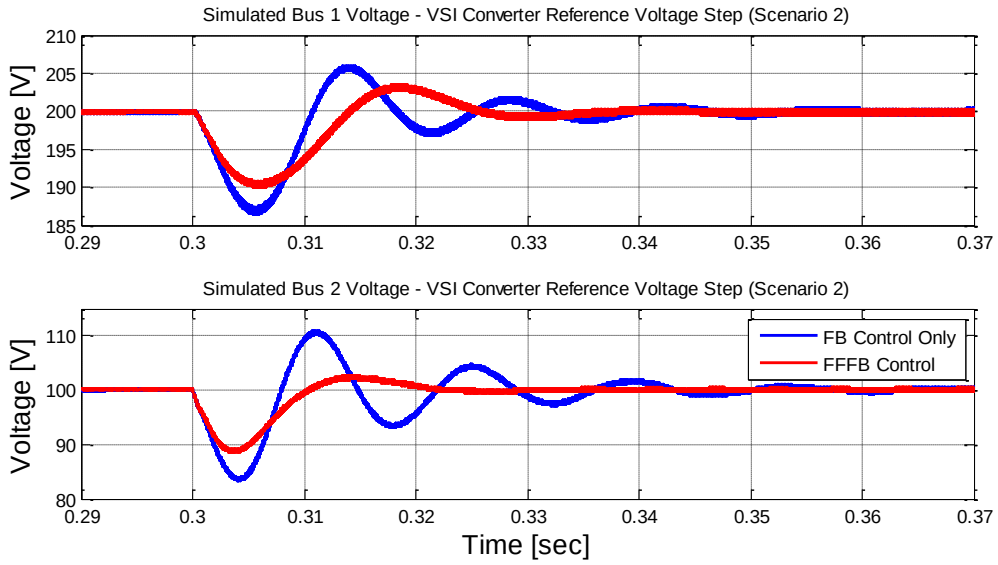


Figure 4.11. Time domain simulation of Scenario 2 MVDC bus voltages under (blue) FB control only and (red) FFFB control during BKL voltage reference step.

4.2 EXPERIMENTAL RESULTS

The scaled notional multi-bus MVDC power system depicted in Figure 4.1 was constructed in the laboratory for the experimental validation. A picture of the physically constructed system is shown in Figure 4.12. The switching converter hardware consists of custom-built, modular power IGBT switch boards and sensing/IO boards that enable a flexible configuration for testing different converter designs and control strategies. The output filter stages for all converters consist of custom wound powdered iron core inductors and off-board electrolytic capacitors. A close up picture of the PRBS converter highlights the power switches, sensing board, and external converter components in Figure 4.13.

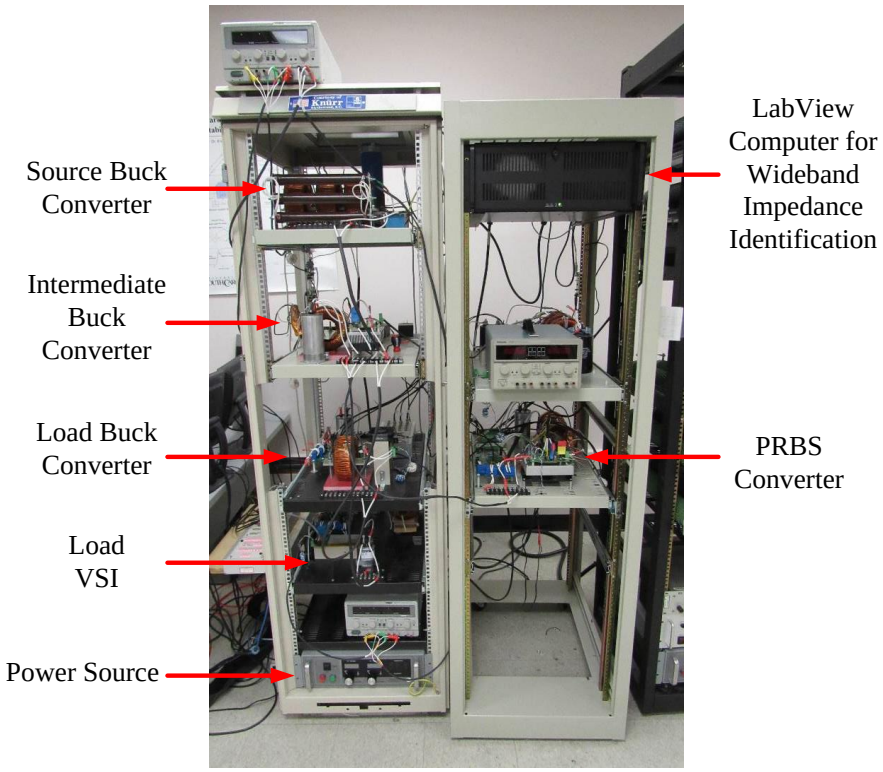


Figure 4.12. Experimental test setup for scaled notional MVDC power distribution system as built in the laboratory.

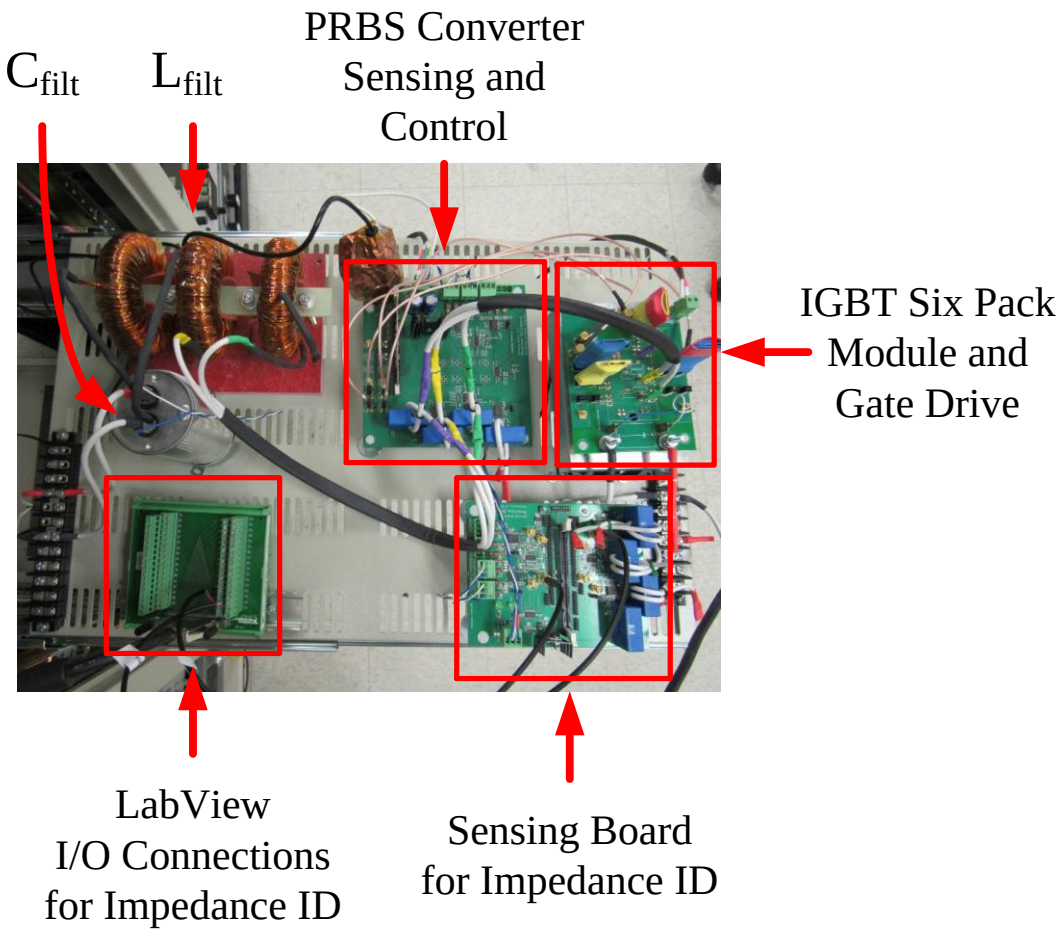


Figure 4.13. Experimental PRBS converter hardware showing power module, sensing board connections, and output filter as well as LabView sensing board and I/O for wideband impedance identification.

Discrete control of the BKS, BKI, and PRBS converters is accomplished using TI TMS320F28335 DSP control cards mounted on custom designed control interface and sensing boards. The control cards for each converter are programmed with the discretized multi-loop PI control strategy as well as a simple anti-windup scheme to prevent overflow of the voltage and current loop integrators during operation. The PRBS converter contains the additional method for performing the PRBS perturbation for the wideband impedance identification. A 14-bit PRBS test signal is internally generated and fed into the duty cycle command of the converter as a 12% perturbation. The injection

results in a modulation of the PRBS converter's input current, which is drawn from the distribution system bus and excites the system bus impedances. For measurements of $Z_{bus\text{-}11}$, the PRBS converter is directly connected at its input to Bus 1 and voltage $V_{bus\text{-}1}$ and the injection current are recorded. Measurements of $Z_{bus\text{-}22}$ are accomplished by connecting the PRBS converter input directly to Bus 2 and capturing $V_{bus\text{-}2}$ variations along with the injection current.

Due to the limited memory and ADC resolution of the TMS320F28335, the TI controller and PRBS converter are used in conjunction with a National Instruments (NI) PCI-6259 data acquisition board for measurement of the perturbed bus voltage and current signals. The voltage and current signals are oversampled at 480 kHz using two single-ended 16-bit ADCs. Preliminary post-processing of the collected time domain perturbation data is carried out by a custom NI virtual instrument (VI), providing plots of the acquired voltage and current Fast Fourier Transform (FFT) spectra and the estimated non-parametric impedance, Figure 4.14. The VI exports the current and voltage time domain data to comma separated value (CSV) text files for further processing. Parametric impedance models are constructed in MATLAB by first thinning the data logarithmically and processing with a Least Squares Fitting algorithm. This process is further detailed later in the chapter.

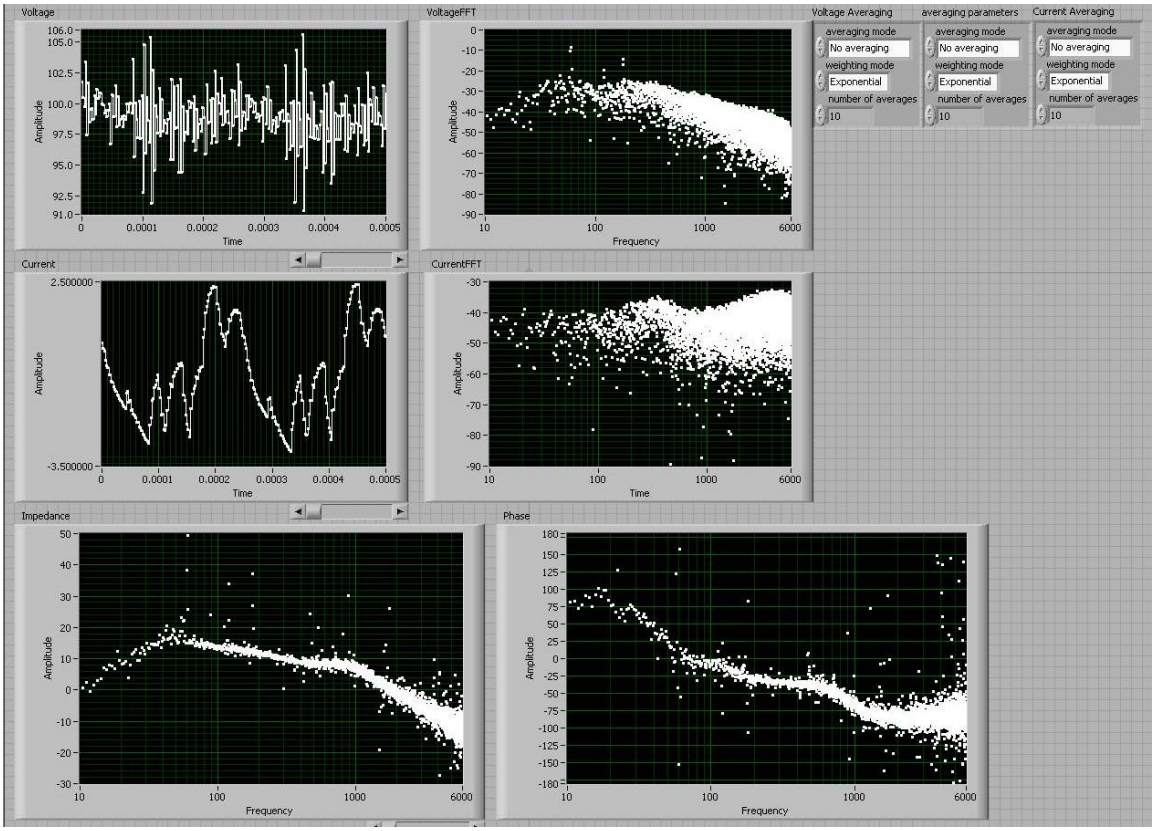


Figure 4.14. Wideband impedance identification LabView Virtual Instrument Front Panel showing preliminary voltage and current FFT results and constructed non-parametric impedance.

The BKL and VSI converters are both discretely controlled using two separate dSPACE DS1104 DSP-based rapid control prototyping platforms [41]. Software provided with this system augments the standard Simulink library with specialized real-time control blocks for interface connections, pulse width modulation (PWM), and event handling. The Real-Time Interface for dSPACE compiles the Simulink block diagram into code that is then executed in real-time on the slave DSP microprocessor [42]. The Simulink block diagrams for the BKL and VSI converters are depicted in Figure 4.15 and Figure 4.16 with the required blocks for real-time operation highlighted.

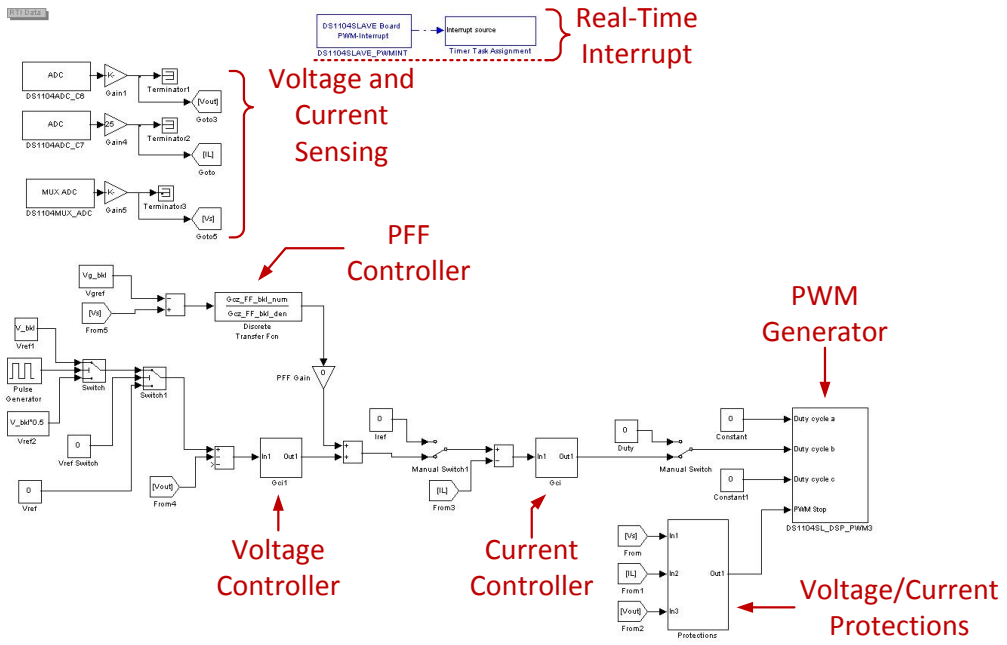


Figure 4.15. Control algorithm for load buck converter (BKL) implemented in Simulink using dSPACE block-set.

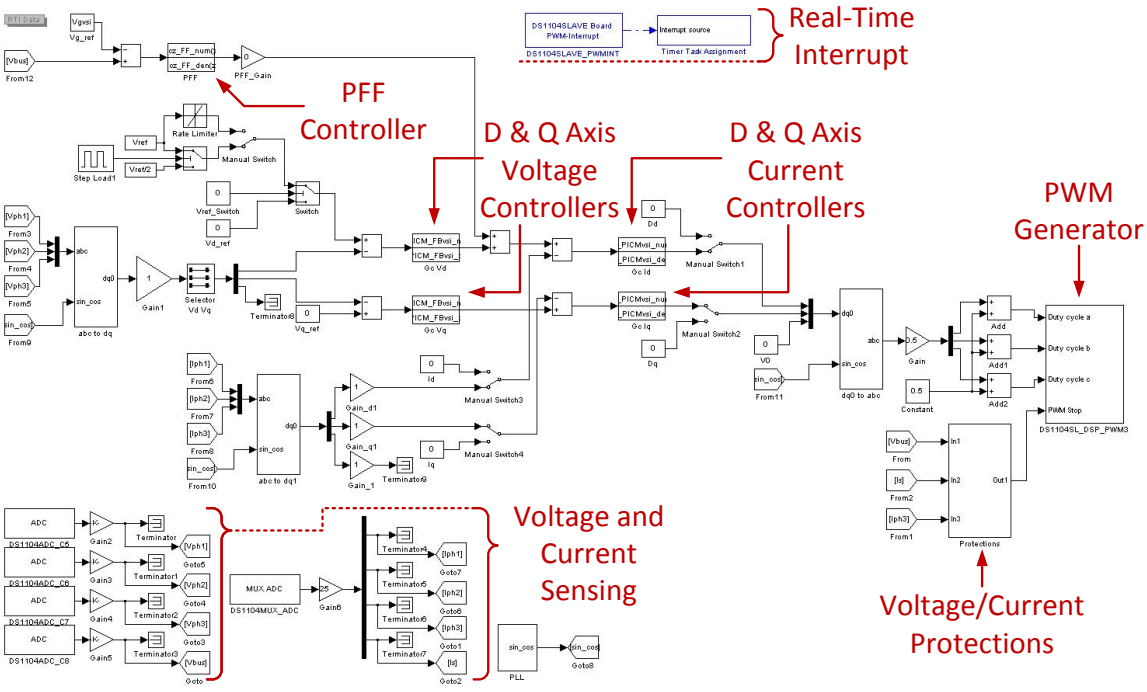


Figure 4.16. Control algorithm for voltage source inverter (VSI) implemented in Simulink using dSPACE block-set.

The compiled control block diagrams for both the BKL and VSI are controlled through the dSPACE ControlDesk software, which provides tools for monitoring the converter voltage, current, and control variables as well as taking in user inputs for changing the converter setpoint and control configurations. The ControlDesk layouts for both converters are shown in Figure 4.17 and Figure 4.18.

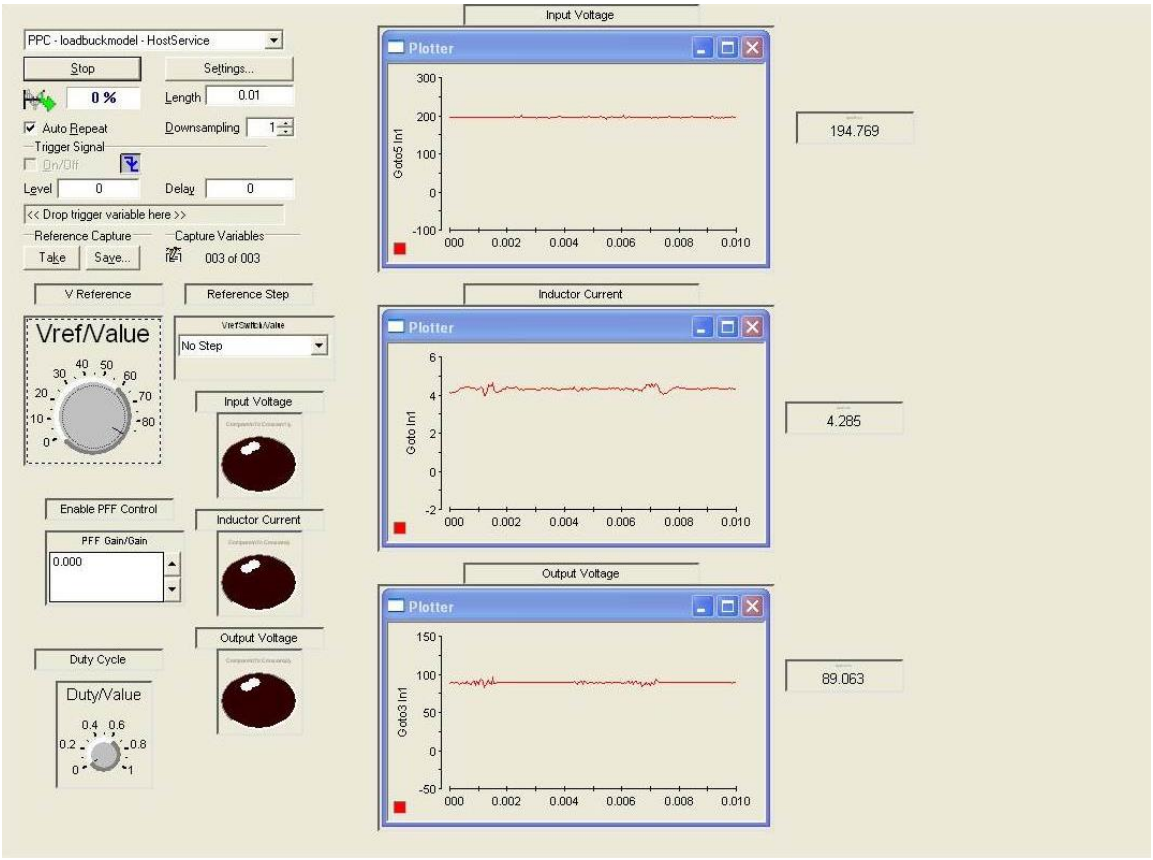


Figure 4.17. dSPACE ControlDesk layout for load buck converter (BKL).

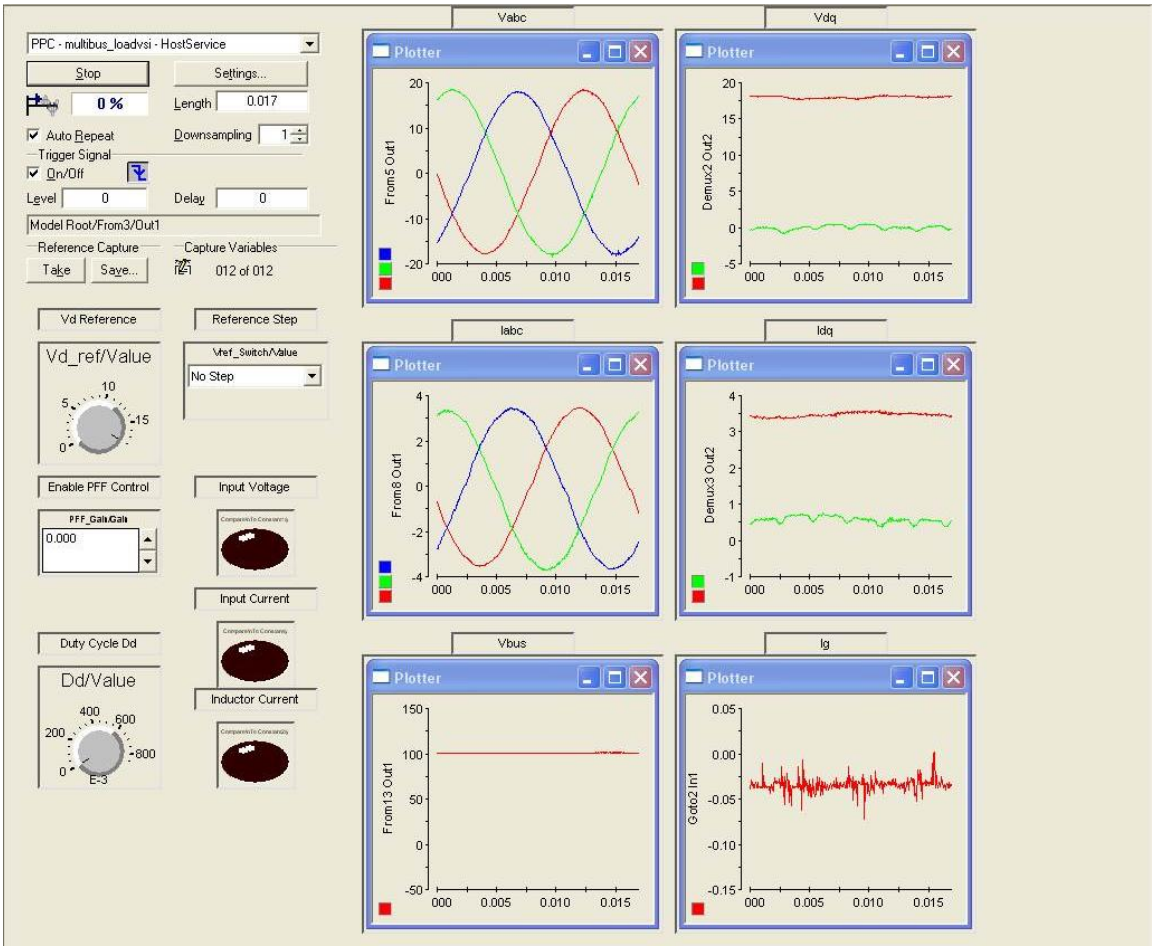


Figure 4.18. dSPACE ControlDesk layout for load voltage source inverter (VSI).

The following sections present the experimental results for the described laboratory test setup. First, the analytically designed PFF control is evaluated in the frequency and time domain for stability and performance enhancement of the multi-bus system. Experimentally obtained impedance identification results are compared to the analytically derived models using the unterminated two-port modeling technique for both the FB and FFFB controlled system in both Scenarios. The performance improvement is validated in the time domain for the same step disturbances that were investigated in simulation. Lastly, the adaptive approach described in Chapter 3 is evaluated for both Scenarios. The system is treated as a "black-box" for which no system operating

parameters are initially known. The experimentally obtained impedance identification results are used in the synthesis of an appropriate PFF control scheme to damp unwanted bus voltage oscillations. This requires that the non-parametric impedances be fit using a Least Squares Fitting algorithm [40] to create parametric models that can then be evaluated using the AIR technique. The results of the adaptive approach are presented in both the frequency and time domain.

4.2.1 SCENARIO 1 – PROMINENT BUS 1 RESONANCE

In the first set of experimental impedance measurements, the system is operated under FB control only. The Least Squares Fitting process is detailed in Figure 4.19 through Figure 4.20 for $Z_{bus\text{-}11\text{-}FB}$, including the logarithmic thinning of the non-parametric data and the creation of a parametric model that will be used later in the adaptive approach. For all other impedances, only the final parametric model is shown.

Thinning the data by creating a frequency index that is equally logarithmically spaced deemphasizes potential errors at high frequency due to the high concentration of data points in the raw non-parametric estimation, Figure 4.19 (red). The total number of points and frequency bandwidth selected for extraction from the raw non-parametric data is variable and must be adjusted appropriately to balance between capturing the required salient features of the impedance and rejecting spurious data points. The "invfreqs" MATLAB function from the Signal Processing Toolbox is used to fit the thinned non-parametric data to a candidate transfer function of a user-specified order. The command returns the numerator and denominator coefficients such that a transfer function is created that describes the estimated impedance, Figure 4.20 (green).

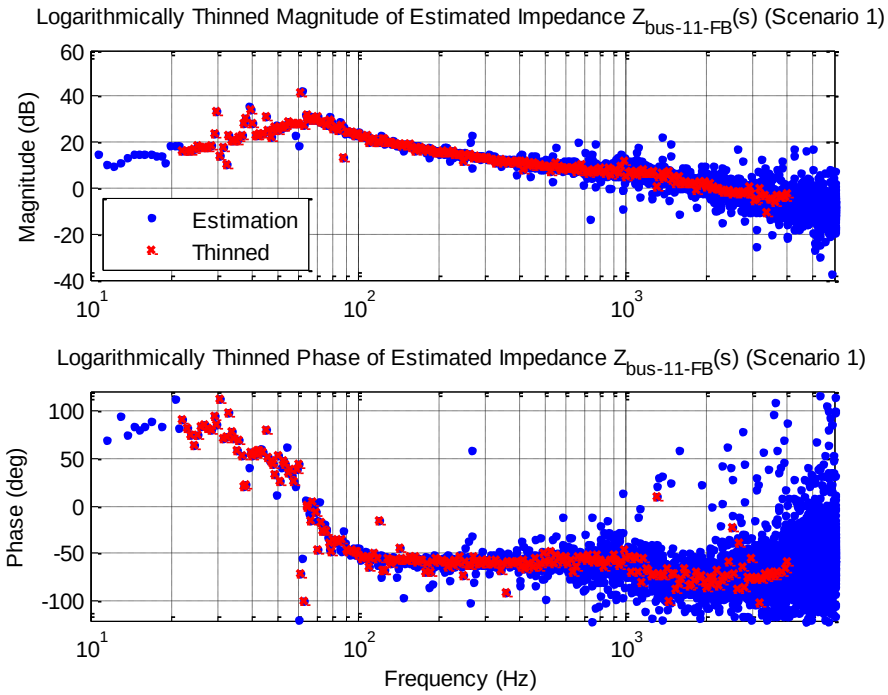


Figure 4.19. Bode plot of experimental Scenario 1 bus self-impedance $Z_{bus\text{-}11\text{-}FB}$ non-parametric estimation and logarithmically thinned data for system operating under FB control only.

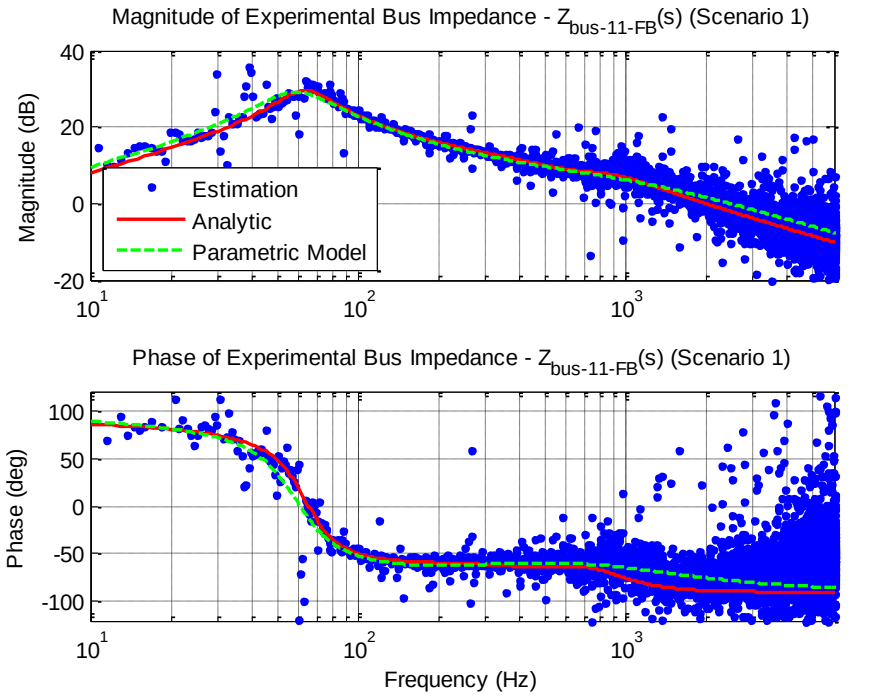


Figure 4.20. Bode plot of experimental Scenario 1 bus self-impedance $Z_{bus\text{-}11\text{-}FB}$ analytic model, non-parametric estimation and fitted, parametric model for system operating under FB control only.

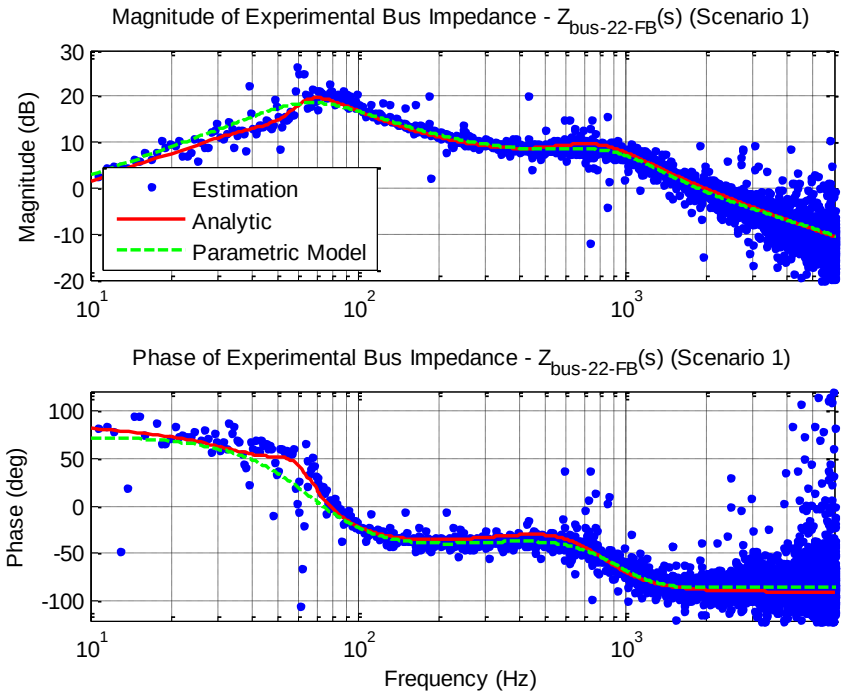


Figure 4.21. Bode plot of experimental Scenario 1 bus self-impedance $Z_{bus\text{-}22\text{-}FB}$ analytic model, non-parametric estimation and fitted, parametric model for system operating under FB control only.

The experimental impedance measurements of the system operating under FB control only show the system bus self-impedances are indeed passive, as was predicted by the analytic models. Close matching is achieved between the fitted parametric models created for both bus self-impedances and the respective analytic functions, demonstrating the validity of the two-port approach for modeling complex interconnected systems as well as the ability of the wideband impedance identification technique to accurately identify converter system impedances. A significant resonance is present on $Z_{bus\text{-}11\text{-}FB}$, as predicted analytically and shown in simulation. This dynamic feature is well captured by the parametric impedance estimation. A slight resonance is also present in $Z_{bus\text{-}22\text{-}FB}$, but is not as pronounced. The parametric model of Figure 4.21 does not capture the phase information of this dynamic feature very accurately, but otherwise demonstrates excellent

matching. This slight discrepancy does not affect the stability analysis and eventual PFF controller design. The impedance identification results of the system operating with the PFF controller designed to damp the Bus 1 resonance via implementation within the BKL converter are shown in Figure 4.22 through Figure 4.23. Since they are unnecessary, no parametric impedance models are created for these results, as the PFF control design is based on full system model.

The non-parametric data for $Z_{bus\text{-}11\text{-}FFFB}$ and $Z_{bus\text{-}22\text{-}FFFB}$ demonstrate good matching with the analytic models throughout the observable bandwidth. The designed PFF controller is shown in Figure 4.22 to damp the Bus 1 resonance such that a more robust dynamic response can be expected. The resonance on Bus 2 is also shown to be marginally improved through the action of the PFF control implemented in the BKL converter, Figure 4.23. The performance improvements shown in the frequency domain are also confirmed by the time domain results shown in Figure 4.24. The BKL output voltage reference is stepped from 67 V_{DC} to 89.44 V_{DC} (75% to 100% full output voltage), resulting in a disturbance on Bus 1 and Bus 2. Under PFF control, the system bus response to this disturbance is shown to be far less oscillatory as a result of the additional damping.

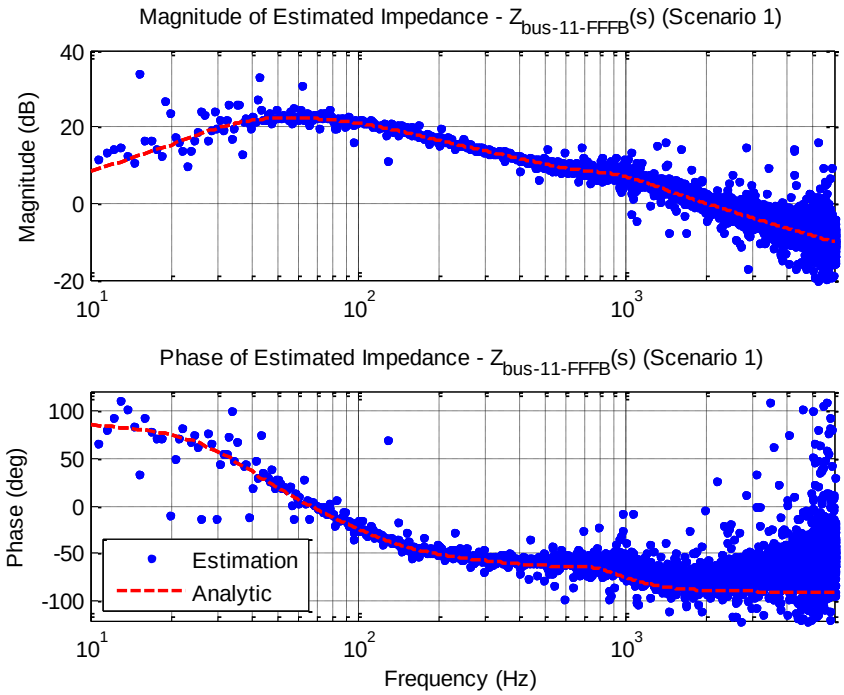


Figure 4.22. Bode plot of experimental Scenario 1 bus self-impedance $Z_{bus\text{-}11\text{-}FFFB}$ analytic model and non-parametric estimation for system operating under FFFB control.

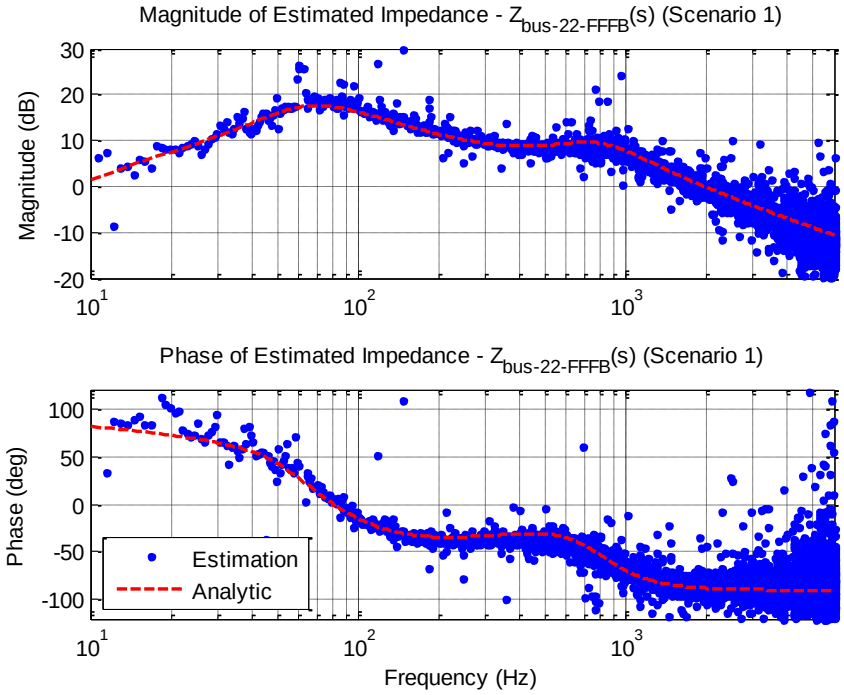


Figure 4.23. Bode plot of experimental Scenario 1 bus self-impedance $Z_{bus\text{-}22\text{-}FFFB}$ analytic model and non-parametric estimation for system operating under FFFB control.

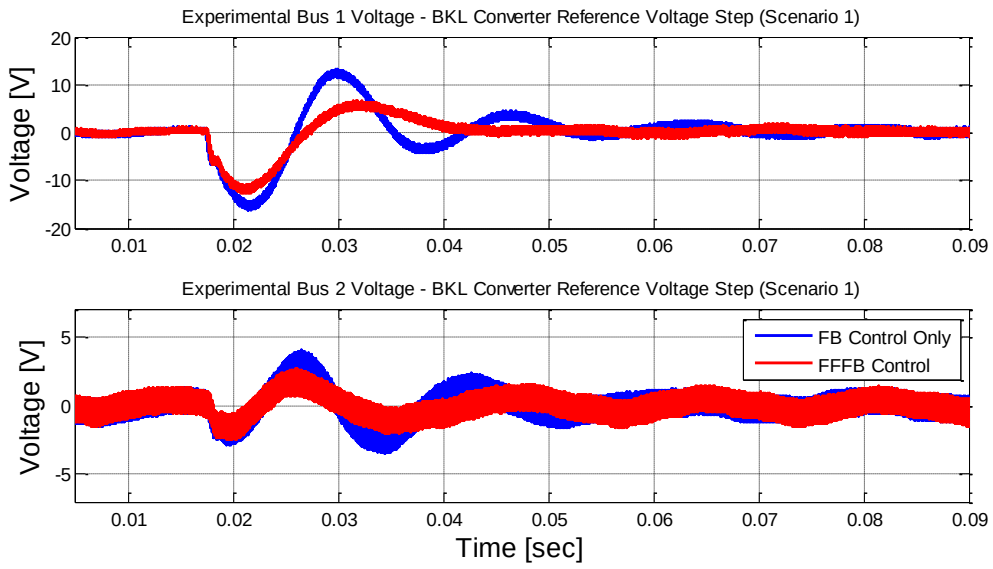


Figure 4.24. Experimental time domain results of Scenario 1 AC coupled bus voltages under (blue) FB control only and (red) FFFB control during BKL voltage reference step.

4.2.2 "BLACK-BOX" SCENARIO 1 – PROMINENT BUS 1 RESONANCE

The following results were obtained by considering the multi-bus system to be a "black-box" for which no advance knowledge of the system operating parameters is available. Thus, the control design depends entirely on the obtained wideband impedance identification results and the subsequently created parametric models. The development of the PFF control is accomplished using the AIR technique and its effectiveness is validated in the frequency and time domains.

The parametric models of $Z_{bus\text{-}11\text{-}FB}$ and $Z_{bus\text{-}22\text{-}FB}$ are depicted in Figure 4.20 and Figure 4.21, respectively. The adaptive PFF control design commences by first extracting the resonant frequencies from each bus self-impedance. Both impedances are then normalized following the estimation technique of (3.12). The Nyquist contours of the normalized bus self-impedances are shown in Figure 4.25 (dashed). The AIR analysis shows that for $\zeta_{min} = 0.5$, only $Z_{bus\text{-}11\text{-}FB\text{-}N}$ extends past the allowable region boundary. As

a result, the PFF control is designed to be implemented on Bus 1 through the BKL converter. A summary of the BKL PFF control design is presented in Table 4.1.

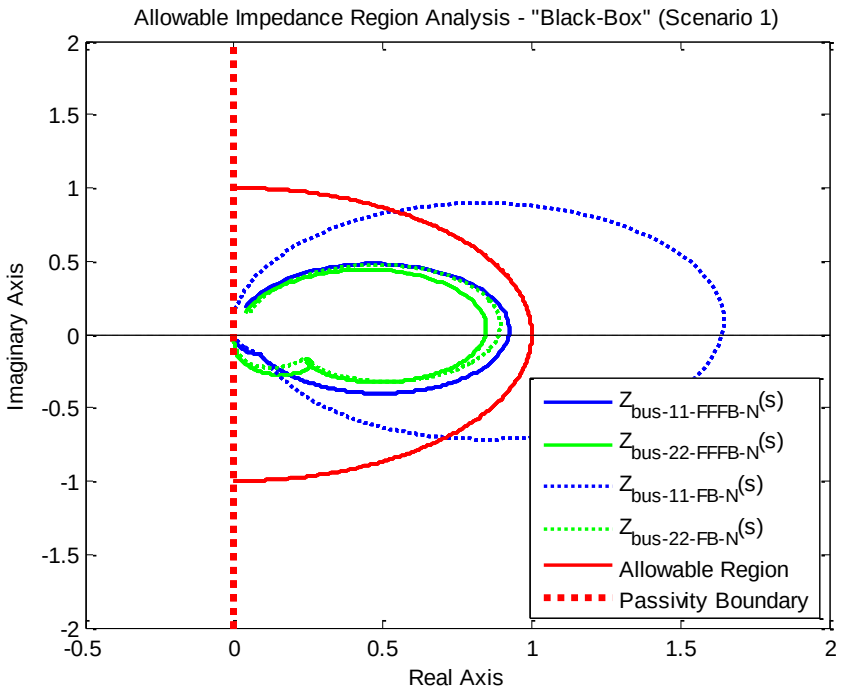


Figure 4.25. Nyquist plot of "black-box" Scenario 1 normalized estimated bus impedances and AIR (ζ_{min} = 0.5) for system operating under FB control only (dashed) and FFFB control (solid).

Table 4.1. Normalized Bus 1 Impedance and Adaptive PFF Control Design Summary (Scenario 1)

Parameter	Value
$f_{0\text{-}bus\text{-}11\text{-}FB}$	58.61 Hz
$\zeta_{bus\text{-}11\text{-}FB}$	0.302
$Z_{0\text{-}bus\text{-}11}$	17.379 Ω (24.80 dBΩ)
K_m	0.250
ζ_{damp}	1.000
$Z_{0\text{-}damp}$	16.458 Ω (24.33 dBΩ)

The designed damping impedance is equivalent to a virtual *RLC* damping impedance in parallel with $Z_{bus\text{-}11}$ having R_b = 35.81 Ω, L_b = 44.69 mH, and C_b = 139.4 µF. To complete the adaptive PFF control design routine, the bus self-impedances are estimated and parametric models created when the system is operated

under FFFB control. The results of this estimation are shown in Figure 4.26 through Figure 4.27. Following normalization of the estimated impedances, the Nyquist contours are evaluated against the AIR, Figure 4.25 (solid). The adaptively designed PFF controller is shown to adequately damp the bus 1 self-impedance resonance, such that the $Z_{bus\text{-}11\text{-}FFFB\text{-}N}$ contour lies wholly within the specified allowable region. The $Z_{bus\text{-}22\text{-}FFFB\text{-}N}$ contour is also shown to remain within the Allowable Impedance Region. Time-domain results of the "black-box" system, shown in Figure 4.28 for a BKL voltage reference step from 67 V to 89.44 V (75% to 100% full output voltage), confirm that the adaptive approach using the AIR analysis technique and simplified PFF control design is successful in synthesizing stabilizing controllers that can damp unwanted resonances and improve system performance. The performance of the adaptively designed PFF controller is nearly indistinguishable from design made using full knowledge of the system model.

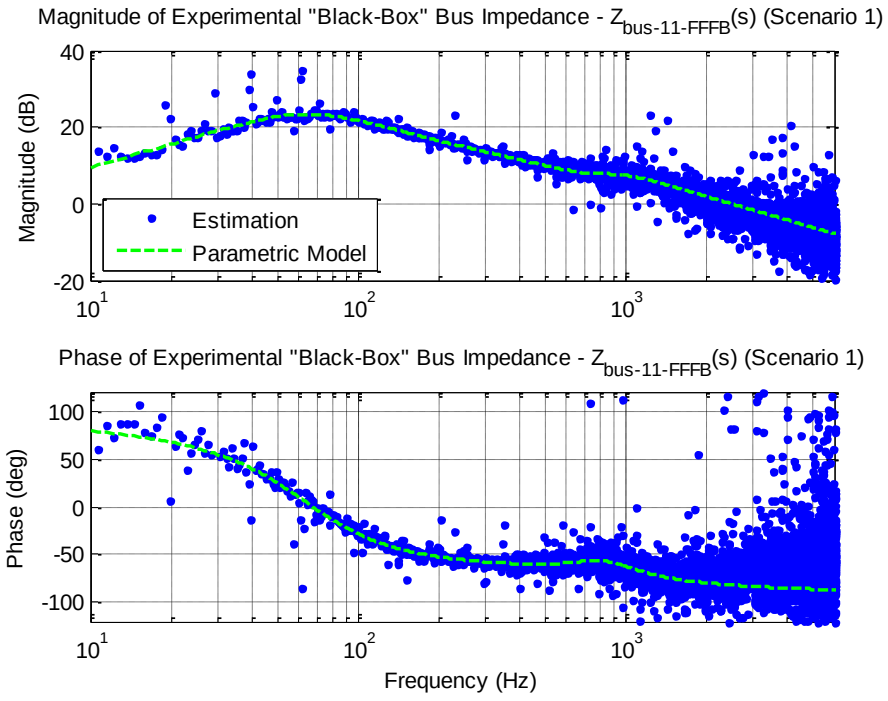


Figure 4.26. Bode plot of experimental "black-box" Scenario 1 bus self-impedance $Z_{bus\text{-}11\text{-}FFFB}$ non-parametric estimation and fitted, parametric model for system operating under FFFB control.

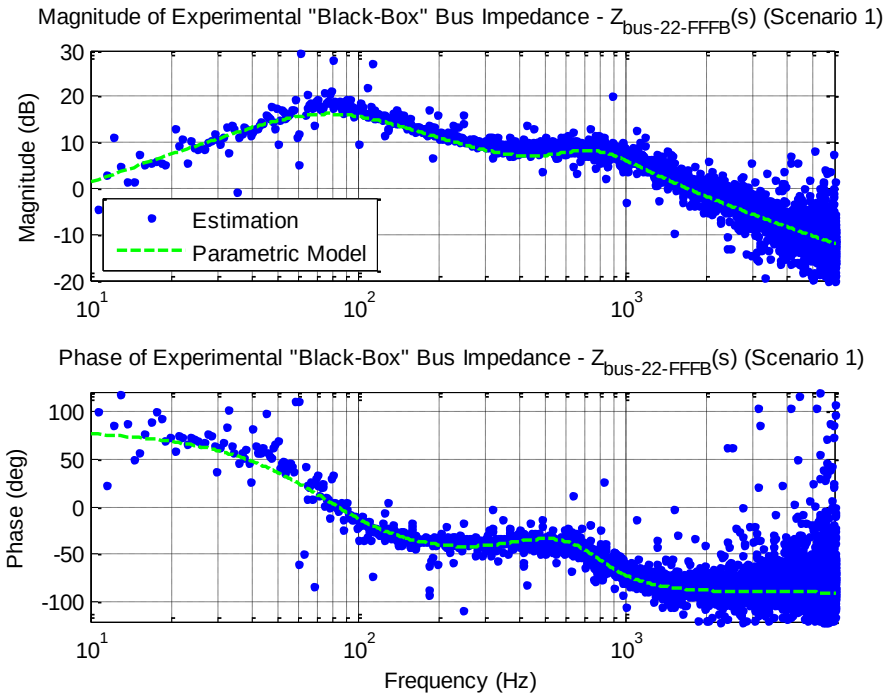


Figure 4.27. Bode plot of experimental "black-box" Scenario 1 bus self-impedance $Z_{bus\text{-}22\text{-}FFFB}$ non-parametric estimation and fitted, parametric model for system operating under FFFB control.

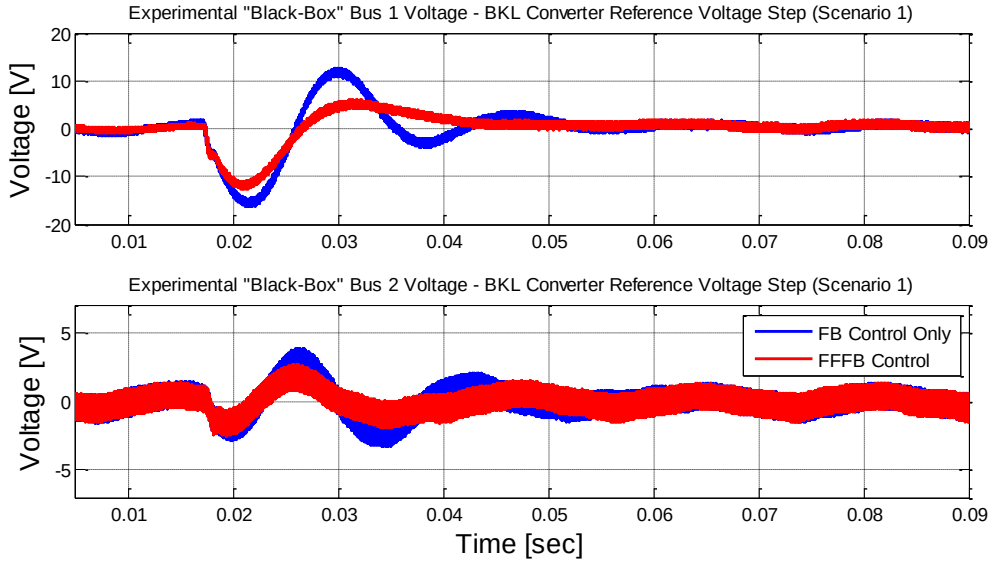


Figure 4.28. Experimental time domain results of "black-box" Scenario 1 AC coupled bus voltages under (blue) FB control only and (red) FFFB control during BKL voltage reference step.

4.2.3 SCENARIO 2 – PROMINENT BUS 2 RESONANCE

The experimental setup is reconfigured to exhibit a significant resonance on Bus 2 and operated under FB control only. The Least Squares Fitting process is again used to construct parametric models of the FB only bus self-impedances for later use in the adaptive PFF control design of the "black-box" system. Experimental impedance identification results for $Z_{bus\text{-}11\text{-}FB}$ and $Z_{bus\text{-}22\text{-}FB}$ are shown in Figure 4.29 and Figure 4.30.

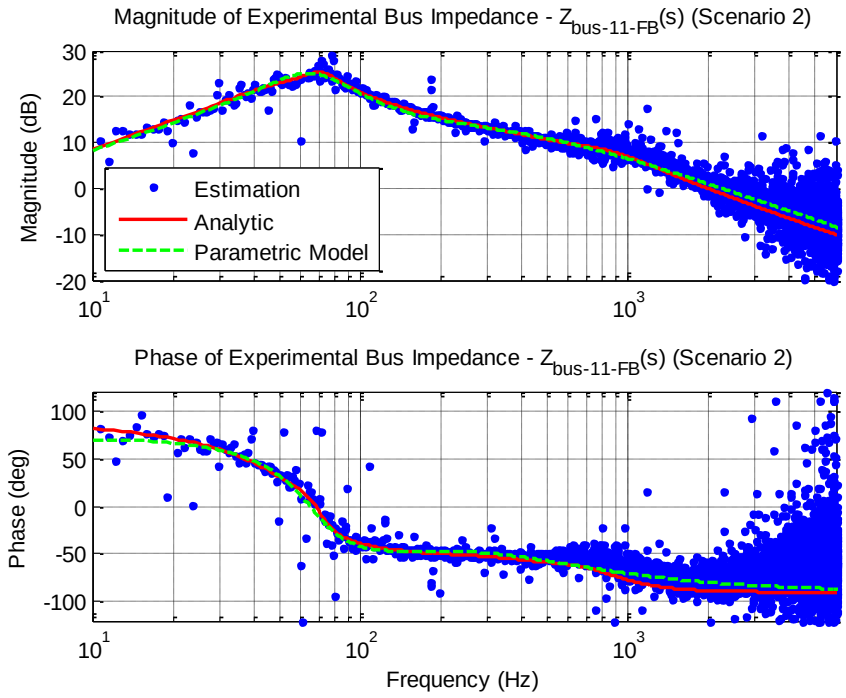


Figure 4.29. Bode plot of experimental Scenario 2 bus self-impedance $Z_{bus\text{-}11\text{-}FB}$ analytic model, non-parametric estimation and fitted, parametric model for system operating under FB control only.

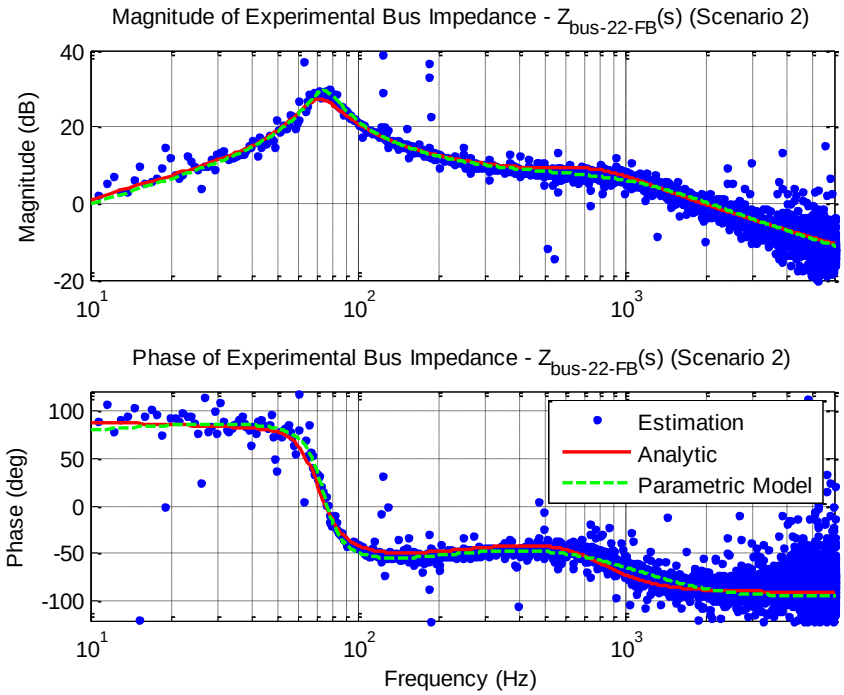


Figure 4.30. Bode plot of experimental Scenario 2 bus self-impedance $Z_{bus\text{-}22\text{-}FB}$ analytic model, non-parametric estimation and fitted, parametric model for system operating under FB control only.

The experimental impedance measurements of the Scenario 2 system operating under FB control only show the system bus self-impedances are passive for all observable frequencies, and demonstrate good matching between the fitted parametric models created for both self-bus impedances and the respective analytic functions. A significant resonance is observed on $Z_{bus\text{-}22\text{-}FB}$, as predicted analytically and in simulation. The impedance identification results of the system operating with the PFF controller designed to damp the Bus 2 resonance via implementation within the VSI converter are shown in Figure 4.31 through Figure 4.32. No parametric impedance models are created for these results, as the PFF control design is based on full system model.

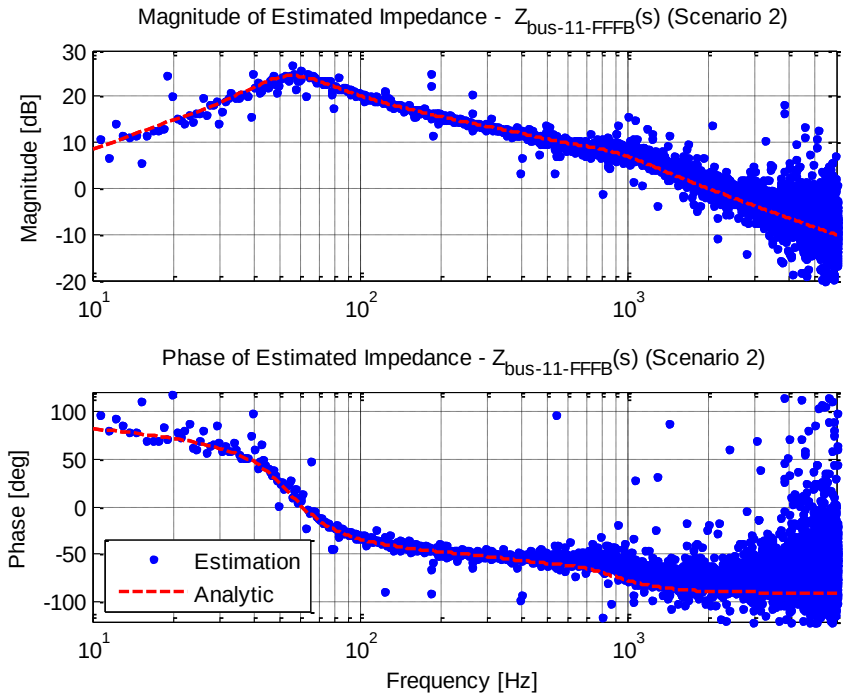


Figure 4.31. Bode plot of experimental Scenario 2 bus self-impedance $Z_{bus\text{-}11\text{-}FFFB}$ analytic model and non-parametric estimation for system operating under FFFB control.

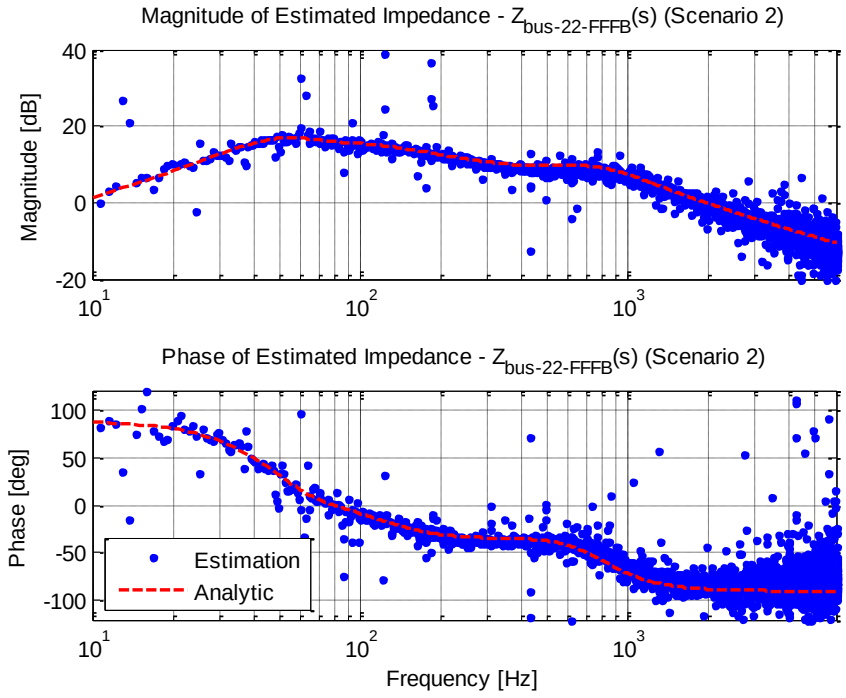


Figure 4.32. Bode plot of experimental Scenario 2 bus self-impedance $Z_{bus\text{-}22\text{-}FFFB}$ analytic model and non-parametric estimation for system operating under FFFB control.

Good matching is achieved between the non-parametric data for $Z_{bus\text{-}11\text{-}FFFB}$ and $Z_{bus\text{-}22\text{-}FFFB}$ and the analytic models throughout the observable bandwidth. The PFF controller implemented through the VSI is shown in Figure 4.32 to damp the Bus 2 resonance such that a more robust dynamic response can be expected. The resonance on Bus 1 is also shown to be improved through the introduction of the virtual damping impedance at the VSI input terminals. These results are further confirmed by the time domain results shown in Figure 4.33. The VSI output voltage reference is stepped from 18.26 V_{PK} to 36.51 V_{PK} (50% to 100% full output voltage), resulting in a disturbance on Bus 1 and Bus 2. The PFF controller is shown to be effective in damping the oscillations resulting from the disturbances.

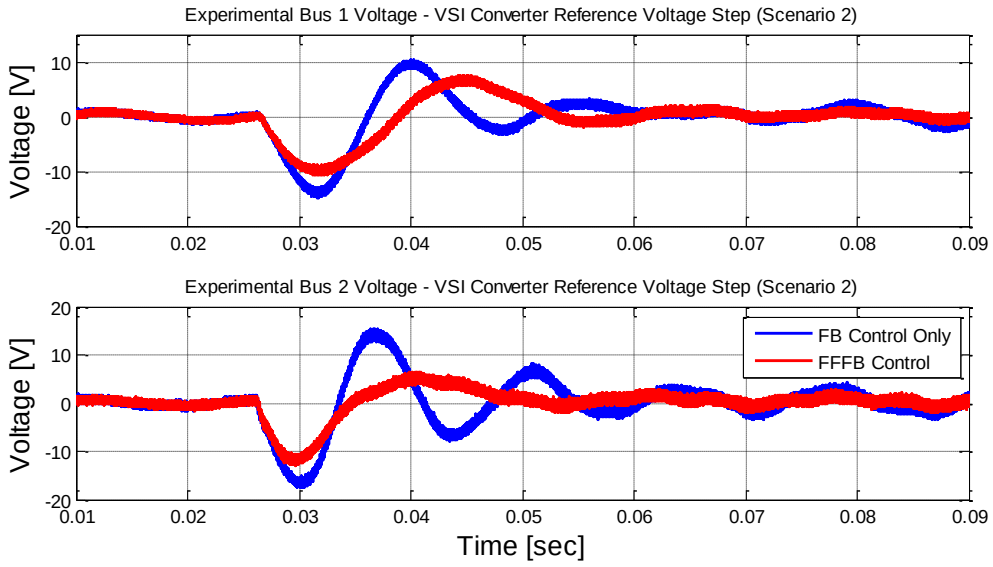


Figure 4.33. Experimental time domain results of Scenario 2 AC coupled bus voltages under (blue) FB control only and (red) FFFB control during BKL voltage reference step.

4.2.4 "BLACK-BOX" SCENARIO 2 – PROMINENT BUS 2 RESONANCE

The following results were obtained by considering the Scenario 2 multi-bus system to be a "black-box" for which no advanced knowledge of the system operating parameters is available. The PFF controller is designed based on the estimation of the system bus self-impedances and the application of the AIR technique for ensuring good dynamic behavior from passive systems. Results are presented demonstrating the effectiveness of the adaptive design method in the time and frequency domain.

The parametric models of $Z_{bus\text{-}11\text{-}FB}$ and $Z_{bus\text{-}22\text{-}FB}$ are depicted in Figure 4.29 and Figure 4.30, respectively. The resonant frequencies and normalization factors are extracted from both impedances for the PFF control design. The Nyquist contours of the normalized bus self-impedances are shown in Figure 4.34 (dashed). The AIR analysis shows that for ζ_{min} = 0.5, both $Z_{bus\text{-}11\text{-}FB\text{-}N}$ and $Z_{bus\text{-}22\text{-}FB\text{-}N}$ extend past the AIR boundary. However, the PFF controller is designed for implementation on Bus 2 via the VSI since the Nyquist contour magnitude of $Z_{bus\text{-}22\text{-}FB\text{-}N}$ extends furthest past the boundary. A summary of the VSI PFF control design is presented in Table 4.2.

Table 4.2. Normalized Bus 2 Impedance and Adaptive PFF Control Design Summary (Scenario 2)

Parameter	Value
$f_{0\text{-}bus\text{-}22\text{-}FB}$	74.30 Hz
$\zeta_{bus\text{-}22\text{-}FB}$	0.128
$Z_{0\text{-}bus\text{-}22}$	7.477 Ω (17.47 dBΩ)
K_m	0.250
ζ_{damp}	1.000
$Z_{0\text{-}damp}$	3.768 Ω (11.52 dBΩ)

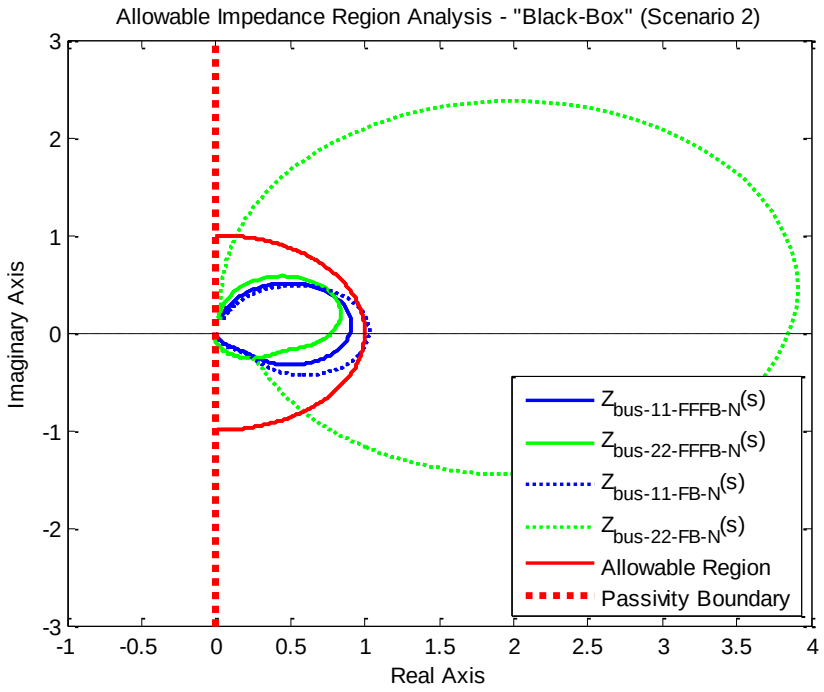


Figure 4.34. Nyquist plot of "black-box" Scenario 2 normalized estimated bus impedances and AIR (ζ_{min} = 0.5) for system operating under FB control only (dashed) and FFFB control (solid).

The designed PFF controller places an equivalent *RLC* virtual damping impedance in parallel with the VSI input terminals having R_b = 7.217 Ω, L_b = 8.065 mH, and C_b = 619.4 μF. To complete the adaptive PFF control design routine, the bus self-impedances are estimated and parametric models created when the system is operated under FFFB control, Figure 4.35 through Figure 4.36. Following normalization of the estimated impedances, the Nyquist contours are evaluated against the AIR, Figure 4.34 (solid). The adaptively designed PFF controller is shown to damp the bus 2 self-impedance resonance, such that the $Z_{bus\text{-}22\text{-}FFFB\text{-}N}$ contour lies wholly within the specified region. Note also that, although the PFF control was enacted on Bus 2 through the VSI, the additional damping has resulted in a reduction of the magnitude of $Z_{bus\text{-}22\text{-}FFFB\text{-}N}$ such that its contour also lies within the specified allowable region.

Time domain results of the "black-box" system, shown in Figure 4.37 for a VSI voltage reference step from 18.26 V_{PK} to 36.51 V_{PK} (50% to 100% full output voltage), confirm that the adaptive approach using the AIR analysis technique and simplified PFF control design is successful in synthesizing stabilizing controllers that can damp unwanted resonances and improve system performance. The performance of the adaptively designed PFF controller is nearly indistinguishable from the PFF controller designed using full knowledge of the system model.

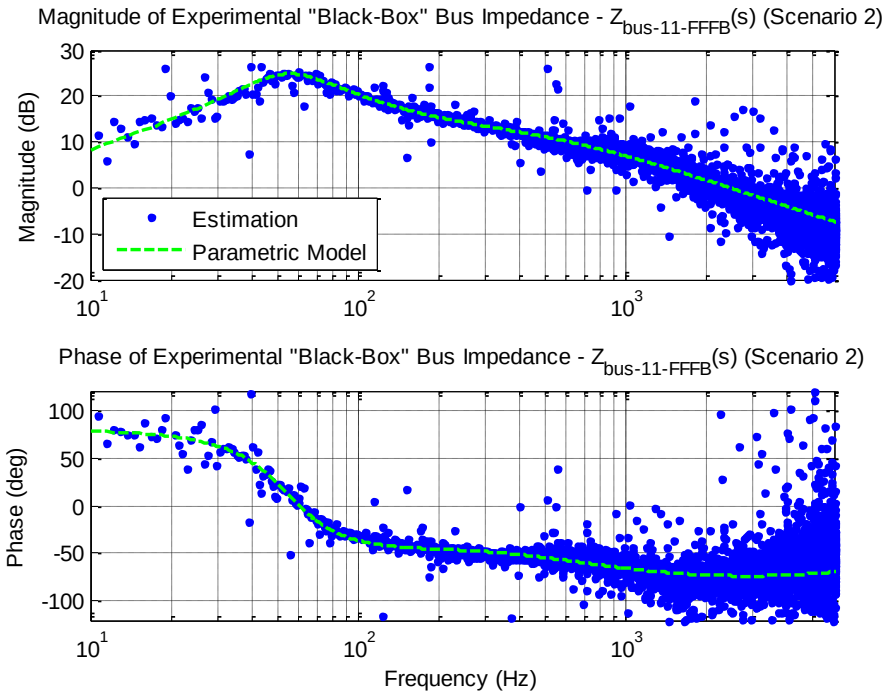


Figure 4.35. Bode plot of experimental "black-box" Scenario 2 bus self-impedance $Z_{bus\text{-}11\text{-}FFFB}$ non-parametric estimation and fitted, parametric model for system operating under FFFB control.

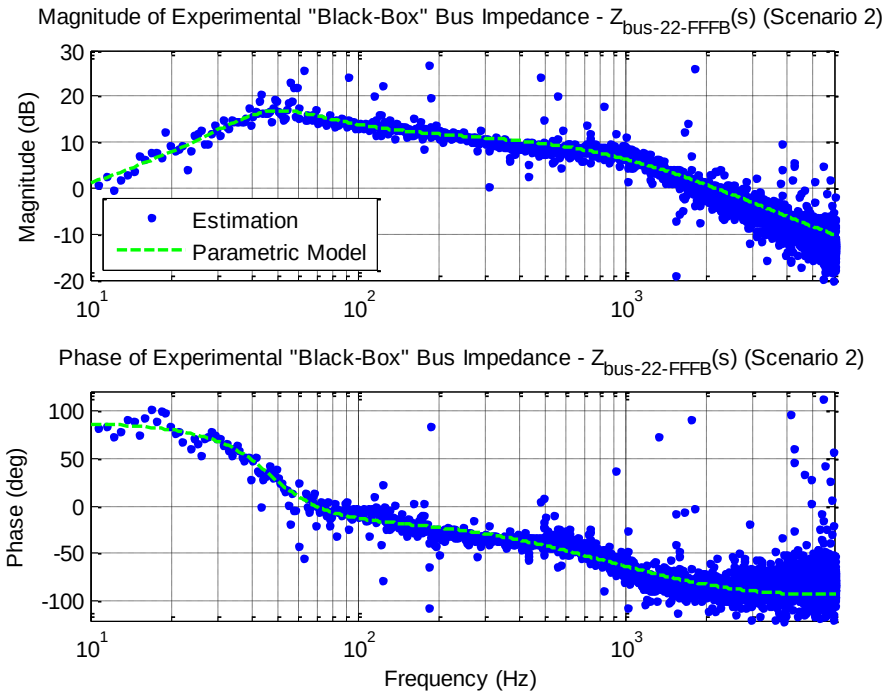


Figure 4.36. Bode plot of experimental "black-box" Scenario 2 bus self-impedance $Z_{bus\text{-}22\text{-}FFFB}$ non-parametric estimation and fitted, parametric model for system operating under FFFB control.

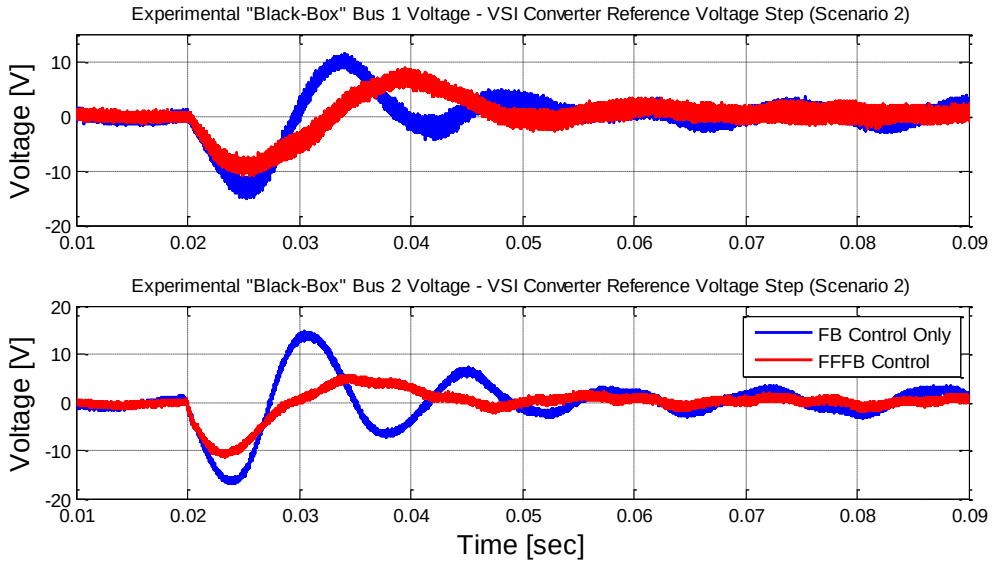


Figure 4.37. Experimental time domain results of "black-box" Scenario 2 AC coupled bus voltages under (blue) FB control only and (red) FFFB control during BKL voltage reference step.

4.3 Conclusion of Simulation and Experimental Results

This chapter demonstrated the modeling, stability and performance analysis, and control design techniques presented previously in Chapter 2 and Chapter 3. A scaled notional multi-bus MVDC distribution system was evaluated in both simulation and in the laboratory for two scenarios in which additional bus damping ensured a stable and performing system. The wideband impedance identification technique was successfully used to construct both non-parametric and fitted parametric models of the system bus self-impedances to assist in the evaluation of the system dynamics and design of stabilizing PFF controllers.

Two scenarios were considered in which either Bus 1 or Bus 2 exhibited a prominent resonance. While both systems were passive and, therefore, stable to begin with, the AIR technique showed that additional bus damping could be implemented to improve the system's dynamic response to a disturbance. An adaptive design approach using the AIR technique coupled with the simplified PFF control design was also shown to be successful in improving the dynamic response of the system when considered as a "black-box" for which no system operating parameters were explicitly known. The wideband impedance identification tool is an enabling technology that is very well suited for application in adaptive system control for large switching converter-based networks.

CHAPTER 5

POWER HARDWARE-IN-THE-LOOP SIMULATION

Power Hardware-in-the-Loop (PHIL) provides a promising solution for dealing with the design challenges encountered in a complex MVDC distribution system. PHIL simulation techniques may be very useful for examining the behavior of large systems when an additional hardware component is added, Figure 5.1. Portions of the MVDC distribution system are simulated in software and interfaced via a power amplifier to the hardware under test. This technique allows for advanced studies to be performed on the overall system's stability when a new piece of equipment is connected and provides a unique opportunity to characterize the component in a realistic operating environment.

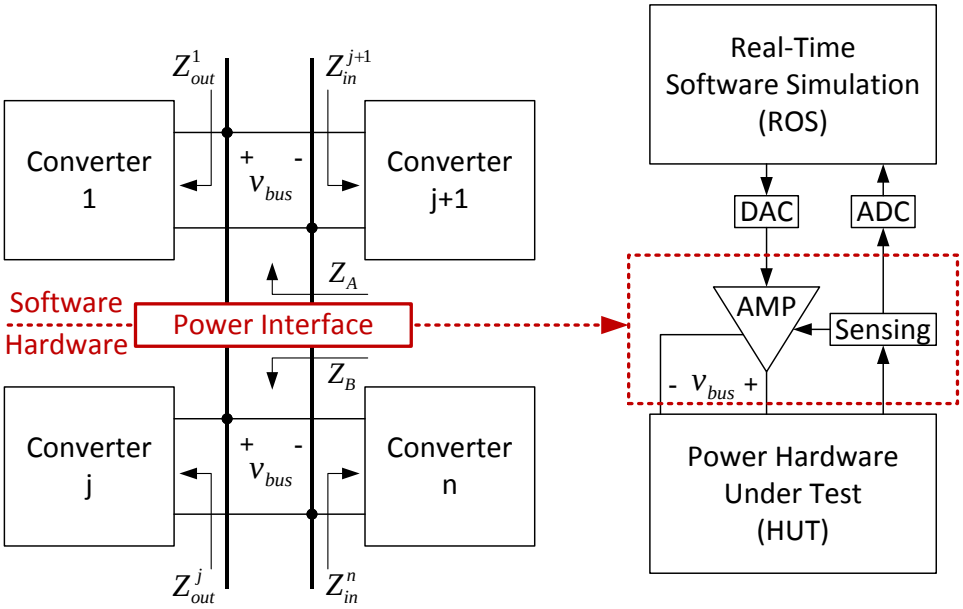


Figure 5.1. PHIL representation of a multi-converter system showing separation of software simulated components and physical hardware.

This chapter examines some of the implementation issues related to PHIL simulation stability and accuracy and proposes techniques for ensuring a robust test bed. The wideband impedance estimation technique is applied as a tool for monitoring the impedance of the hardware-under-test connected to the PHIL test bed and for enhancing the stability of the power interface between software simulation and the physical equipment. Impedance based design constraints are developed for the power interface amplifier to guarantee accurate PHIL simulation results. Illustrative simulation results are presented to demonstrate the efficacy of the proposed techniques.

5.1 INTERFACE STABILITY

In a PHIL simulation, the software simulated rest-of-system (ROS) components and hardware-under-test (HUT) components are coupled via a power interface. The power interface consists of a power amplifier that imposes the electrical conditions present at a user-specified node in the ROS upon the HUT. Information from the HUT in the form of sensed voltage and/or current quantities is transmitted back through the power interface to the ROS, such that power is virtually exchanged between software simulation and hardware. The method in which this virtual exchange of power is accomplished is referred to as the Interface Algorithm (IA).

The choice of IA must be carefully evaluated with regard to the overall PHIL simulation closed-loop stability to prevent possible damage to the testing apparatus and HUT while also ensuring accurate results. A variety of different IAs have been proposed in the literature to model the behavior of the power interface and address accuracy and stability issues that may arise [34]-[36], [38]. Of these proposed algorithms, the Damping Impedance Method (DIM) exhibits the highest stability and accuracy. This IA also

possesses the unique capability to be adaptively controlled to ensure absolute stability of the power interface by adjusting the value of a simulated damping impedance to match that of the interfaced HUT impedance. Due to the general stability and accuracy, as well as the ability to adapt the IA in real-time, the DIM is selected for use in this work.

5.1.1 DIM Interface Algorithm Stability

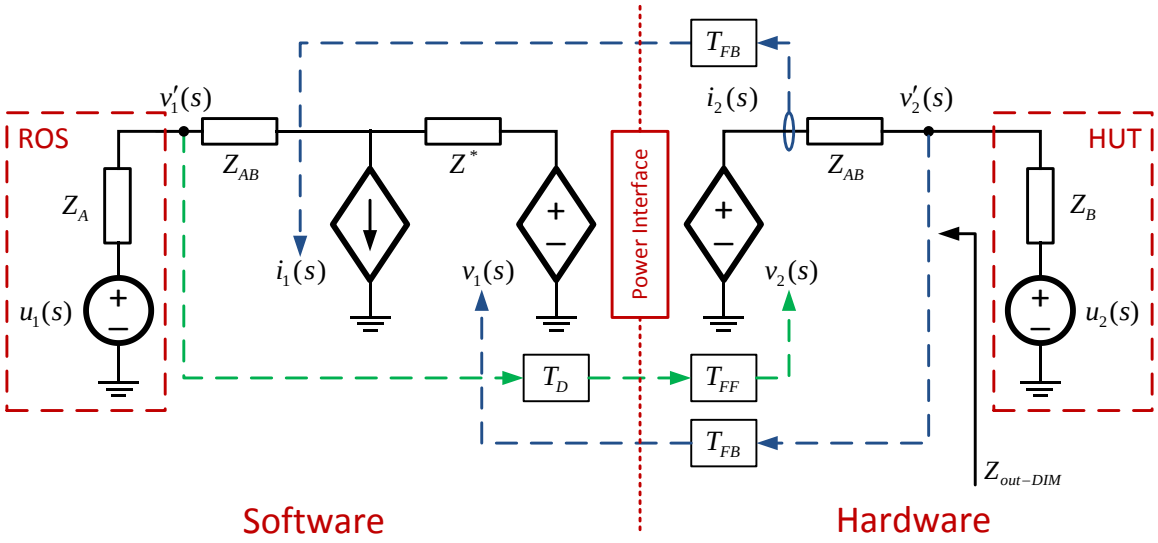


Figure 5.2. Damping Impedance Method (DIM) interface algorithm.

Shown in Figure 5.2, the DIM combines the accuracy of the voltage-type Ideal Transformer Method with the stability of the voltage-type Partial Circuit Duplication (PCD) method with transient damping provided by an additional damping impedance Z^*. The Laplace variable, *s*, has been omitted for brevity. The DIM circuit diagram is split into a software side implementation and hardware implementation at the power interface. On the software side, the ROS is designated as a voltage source, u_1, and the equivalent Thévenin impedance of the simulated components, Z_A. On the hardware side, the HUT consists of a voltage source, u_2, and the equivalent Thévenin impedance of the hardware components, Z_B. A feed-forward loop provides the real-time software-computed voltage

reference for the interface amplifier, v_2. This loop contains a time delay, T_D, representing the execution time of the real-time computation platform. The interface amplifier bandwidth is included as the gain T_{FF}. A linking impedance on the hardware side, designated as Z_{AB}, exists as a consequence of the power amplifier output impedance. This impedance is also included on the software side.

Note the presence of two feedback loops from the hardware side to software side. The current i_2 is fed back through a sensor gain T_{FB} and drives the dependent current source i_1. The HUT voltage is also scaled by T_{FB} and fed back to drive the dependent voltage source v_1. The damping impedance, Z^*, is connected in series between these two simulated sources. It can be seen that, under steady-state operating conditions, ideal interface behavior would result in the voltage v^* across dependent current source i_1 equaling v_2' and no current flowing through Z^*. Under transient conditions, voltages v^* and v_2' are unequal, resulting in a current through Z^*. This behavior can effectively damp undesired oscillations of the interface. The proper value for Z^* is determined by evaluating the block diagram of the DIM, shown in Figure 5.3. The loop gain of the IA is given in (5.1).

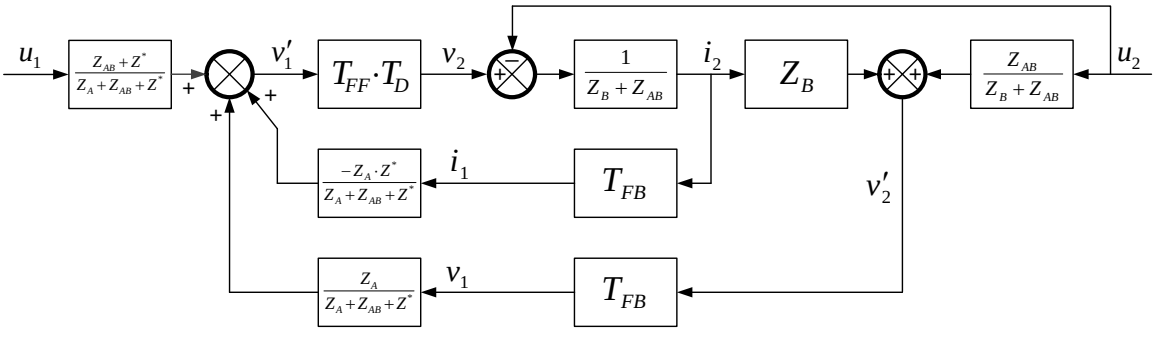


Figure 5.3. Damping Impedance Method (DIM) interface algorithm block diagram.

$$G_{OL-DIM}(s) = \frac{Z_A(Z_B - Z^*)}{(Z_B + Z_{AB})(Z_A + Z_{AB} + Z^*)} T_D T_{FF} T_{FB} \tag{5.1}$$

Inspection of the open-loop transfer function reveals that absolute stability is guaranteed when the impedance Z^* is equal to Z_B, the impedance of the HUT. Under this condition, the magnitude of (5.1) becomes zero, such that the loop gain has infinite phase margin (no crossing of the unit circle). Notice that, according to the Nyquist criterion, a sufficient stability condition is that $\left|G_{OL-DIM}(j\omega)\right| < 1$ for all ω.

This unique property allows for the interface to be adapted as the PHIL simulation is performed such that stability is guaranteed over a wide range of operating conditions. Several methods to monitor the HUT impedance and actively adjust the simulated damping impedance to improve the DIM interface stability have been previously proposed in the literature [34]-[38]. However, these methods are limited in application and only provide the HUT impedance at the quiescent operating point. In this work, a method based on wide bandwidth system identification techniques is proposed to address this deficiency. An accurate, wideband estimation of the HUT impedance can be constructed utilizing system identification techniques. The measurement of impedance requires a high bandwidth voltage or current perturbation at the power interface. Shown in Figure 5.4, this perturbation is accomplished by injection of a finite-length, digital approximation of white noise via a Pseudo-Random Binary Sequence (PRBS) into the duty cycle command of the switching converter serving as the power interface amplifier. Cross-correlation techniques applied to both the output current and output voltage result in wideband estimations of the control-to-output current, $G_{i_{out}d}$, and control-to-output

voltage, $G_{v_{out}d}$, transfer functions. The HUT impedance may then be constructed as the ratio of these two transfer functions [27].

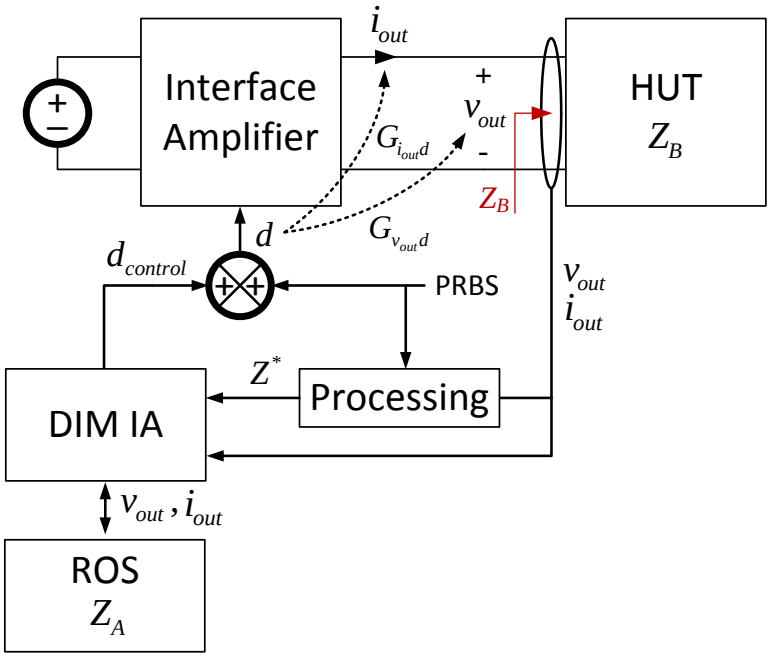


Figure 5.4. Damping Impedance Method (DIM) including wideband impedance identification.

The identification procedure results in a non-parametric estimation of the HUT impedance. To employ the obtained information in the IA, the data is fit to a candidate transfer function having a user-specified number of poles and zeroes using Least Squares Fitting. Finally, Z^* is updated to reflect the measured HUT impedance data such that interface stability is guaranteed. This HUT identification procedure is particularly well-suited for use in PHIL simulation, as it is an online measurement that can be performed by the power converter already serving as the interface amplifier.

5.1.2 Simulation of Damping Impedance Method Stability Improvement

Initial simulation results of a PHIL test platform employing impedance identification as a means to improve interface stability are presented for the case of a

scaled MVDC distribution system PHIL experiment. In this experiment, the HUT is considered as a "black-box" load, for which no detailed model of the hardware is known. The initial value of the simulated damping impedance Z^* allows for a stable PHIL interface. However, the mismatch between Z^* and the actual HUT impedance Z_B results in oscillations of the interface voltage, compromising the simulation accuracy. This PHIL test case is simulated in MATLAB/Simulink and consists of the PHIL interface and a naturally coupled reference system for comparison.

The scaled MVDC distribution system, shown in Figure 5.5, consists of a source buck converter (BKS) feeding a DC bus, to which a load three-phase voltage source inverter (VSI) and load buck converter (BKL) are connected. All converters switch at 10 kHz and operate under feedback control using an inner current loop and outer voltage loop PI strategy. The system is fed by a 400 V_{DC} source, establishes 200 V_{DC} at the bus connection, and operates at a nominal power level of 1 kW. Complete system parameters are given in Table 5.1.

Table 5.1. Complete PHIL System Converter Hardware and Control Parameters for PHIL System Stability Evaluation

Parameter	BKS	BKL	VSI
f_{sw}	10 kHz	10 kHz	10 kHz
L_{filt}	3 mH	1 mH	1 mH
C_{filt}	90 µF	90 µF	90 µF
R_{load}	-	20 Ω	19.2 Ω
$K_{p\text{-}il}$	0.138	0.022	0.057
$K_{i\text{-}il}$	458.3	29.51	129.9
$K_{p\text{-}v}$	0.164	0.190	0.067
$K_{i\text{-}v}$	100.5	213.2	44.05

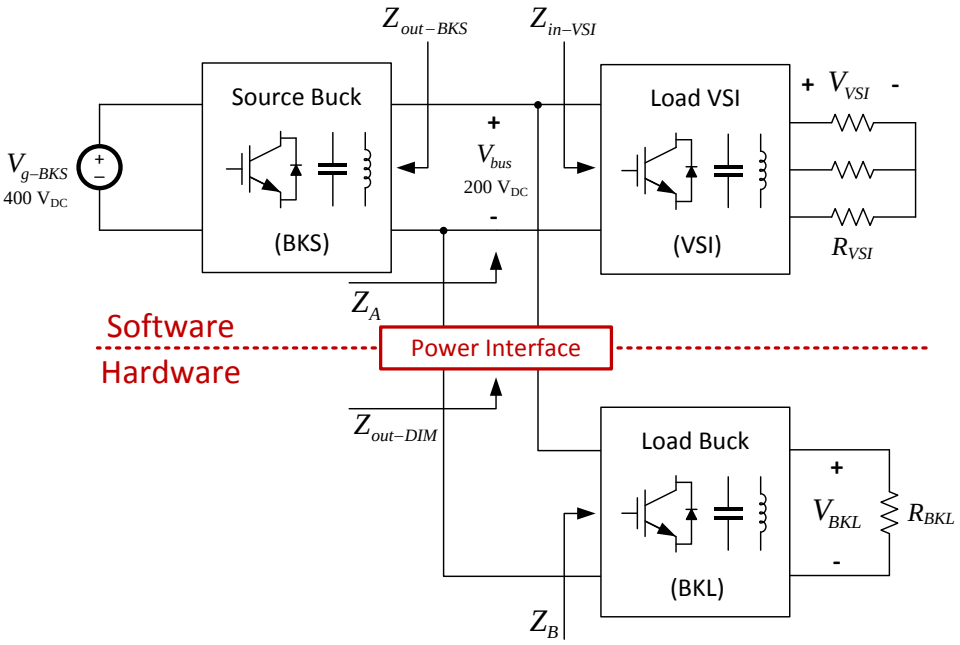


Figure 5.5. Scaled MVDC distribution system PHIL test scenario comprised of an interconnected source buck converter and load VSI and load buck converter.

For PHIL testing, the power interface between simulation and hardware is defined at the bus connection of the load buck converter. Using the impedance notation of Figure 5.2, Z_A is the parallel combination of the source buck converter output impedance $Z_{out\text{-}BKS}$ and load VSI input impedance $Z_{in\text{-}VSI}$. The HUT impedance Z_B is the input impedance of the BKL. A time delay of 200 µs is assumed to exist at the power interface. The linking impedance Z_{AB} has a low value of 0.01 Ω to improve simulation accuracy. An initial value of Z^* may be approximated from the 500 W power level of the BKL as an 80 Ω resistor. A Nyquist plot, Figure 5.6 (blue), of the loop gain $G_{OL\text{-}DIM}$ shows that the interface is not unstable for this rough estimate, but has a low phase margin that may result in inaccurate simulation results and oscillations.

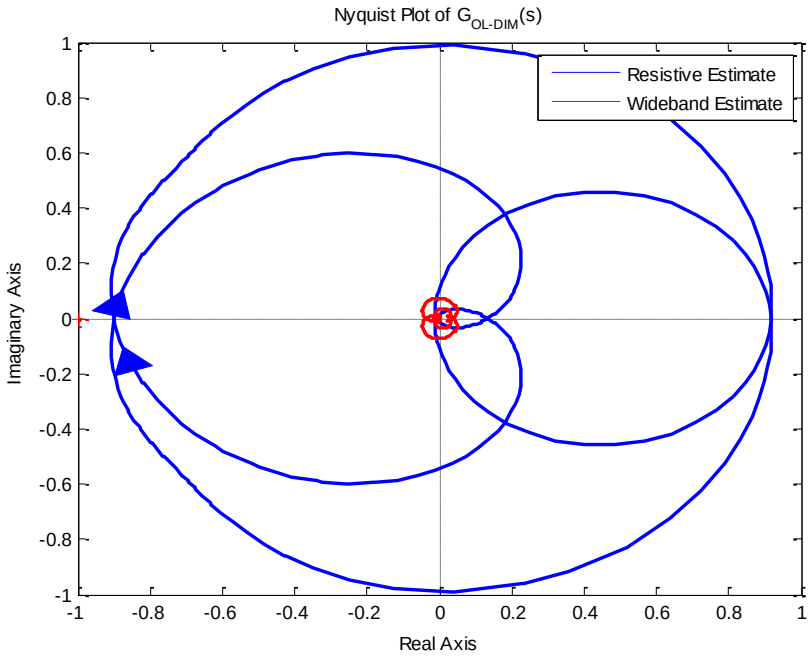
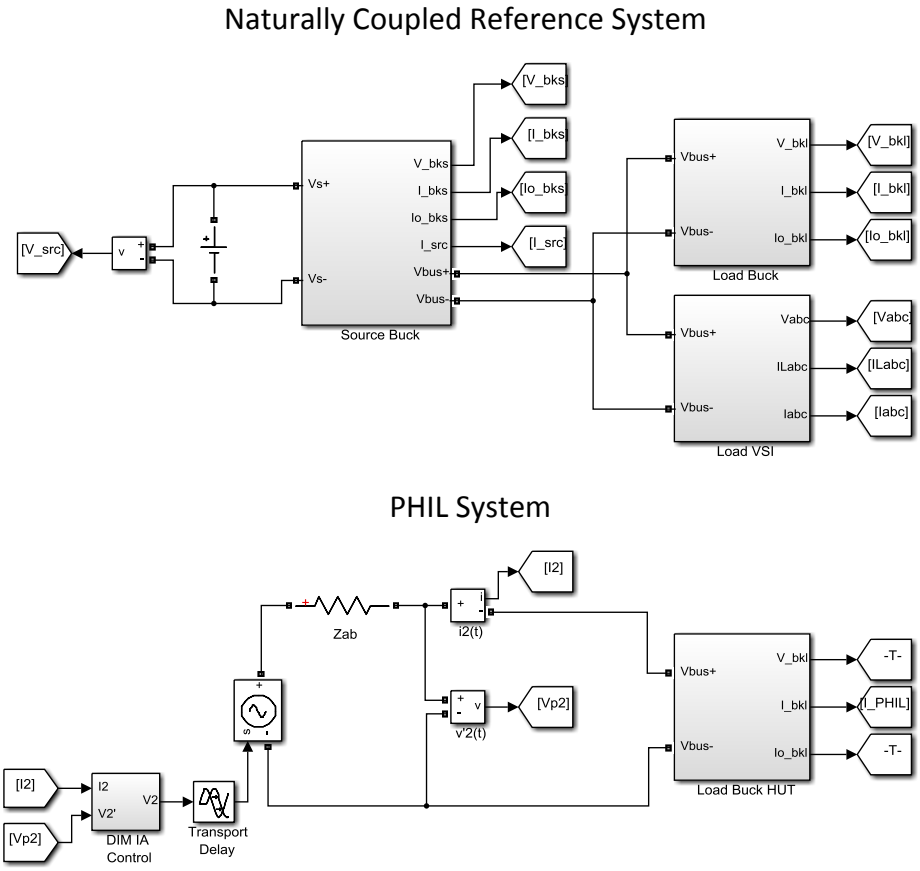
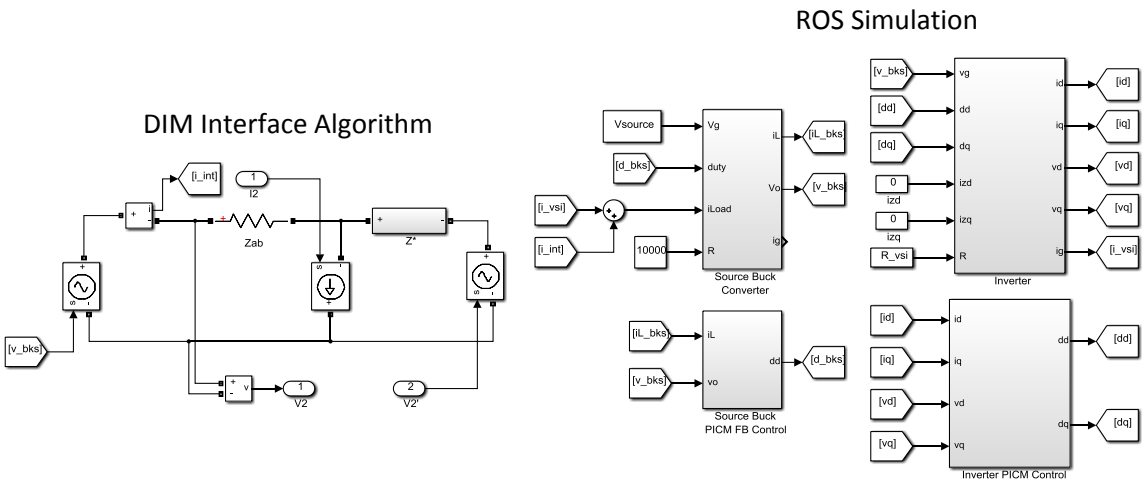


Figure 5.6. Nyquist plot of DIM IA loop gain using resistive estimate of Z^* (blue) and wideband estimate (red) for MVDC system

A model of the naturally coupled reference system and PHIL simulation was constructed in MATLAB/Simulink, Figure 5.7. A time-domain simulation of the bus voltage for the PHIL system and for a reference, naturally coupled system is shown in Figure 5.8. At t = 0 sec, the source buck converter ramps up, supplying 200 V_{DC} at the bus. Beginning at t = 0.05 sec, the load buck converter (HUT) starts up, ramping its output voltage to 100 V_{DC}. This action causes a sag in the bus voltage, which ends at approximately t = 0.08 sec when the converter reaches steady-state operation. The load VSI begins operation at t = 0.1 sec, also resulting in a bus voltage sag until a steady-state output voltage of 80 V_{PK} is achieved. At t = 0.15 sec, the load buck converter (HUT) output voltage is stepped to 50 V_{DC} (half the rated value), resulting in a brief oscillation of the bus voltage.



(a)



(b)

Figure 5.7. Simulink diagram of simulated PHIL test platform showing (a) naturally coupled MVDC system and PHIL simulation with HUT connection, and (b) DIM IA and ROS simulation

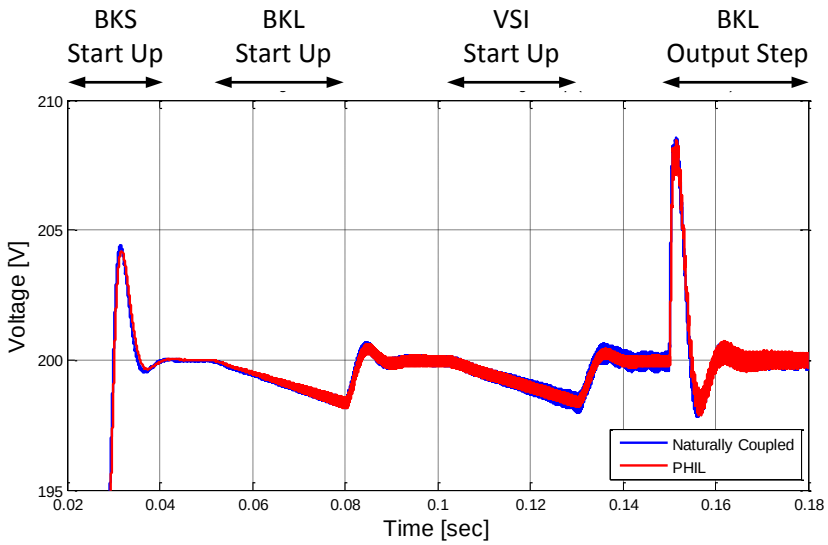


Figure 5.8. Overview of bus voltage time-domain simulation showing converter startup and load step change for a reference system (blue) and PHIL system (red).

For this series of events, the results of the PHIL system demonstrate good matching to that of the reference system. The interface algorithm correctly incorporates the ROS impedance Z_A into the PHIL system, such that the load buck startup results in a bus voltage sag that closely resembles the naturally coupled reference system. Also, note that for the PHIL system, the load VSI startup event occurs in the simulated ROS. The interface amplifier correctly reproduces this transient bus voltage condition and imposes it at the output. The DIM interface algorithm is demonstrated to accurately model simulated events and HUT imposed events.

Closer inspection of the bus voltage waveform during the load buck (HUT) output voltage step change, Figure 5.9, reveals an oscillation in the PHIL simulated bus voltage that is not present for the reference system. This disparity is a result of the inaccurate resistive approximation of Z^* in the DIM IA. To improve the accuracy of the PHIL simulation, a wideband estimation of the HUT impedance is required. A 16-bit, 20 kHz PRBS test signal is added to the steady-state 200 V_{DC} interface amplifier output to

perturb the HUT. Measurements of the output voltage and current are used to construct a non-parametric estimation of the impedance Z_B via cross-correlation techniques, Figure 5.10 (blue). The estimation is then fit to a candidate transfer function using Least Squares Fitting [40], Figure 5.10 (dashed green). The fitted model demonstrates a slight error in magnitude at low frequency in the parametric model with respect to the analytic HUT impedance (red), but is otherwise a good wideband estimate.

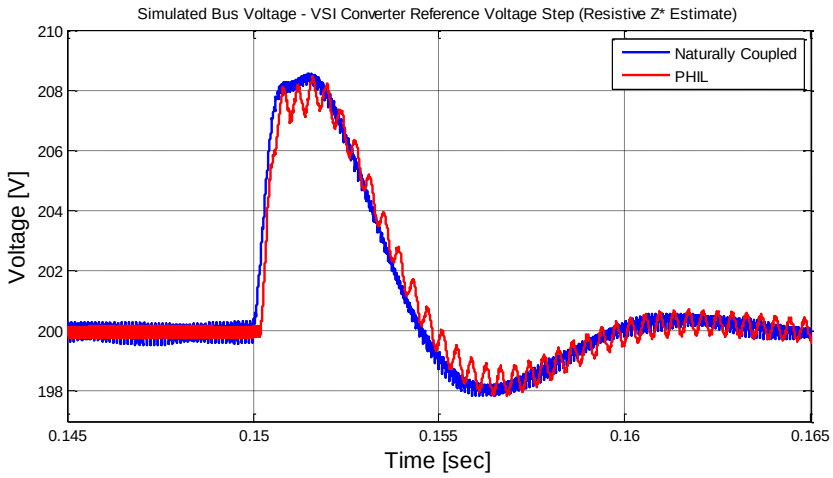


Figure 5.9. Zoom of load step change for a reference system (blue) and PHIL experiment (red) showing oscillation in PHIL system.

The simulated Z^* damping impedance is updated with the obtained identification results. See Appendix C for details concerning the implementation of complex Thévenin impedance models within Simulink. The gain and phase margin of the interface loop gain is significantly improved, evidenced by the Nyquist plot in Figure 5.6 (red). The previous bus voltage oscillations present in the PHIL simulation during a step change in the HUT buck converter output voltage have been eliminated as a result of employing the wideband estimation of the HUT impedance in the IA, Figure 5.11. Also, note the presence of the time delay in the PHIL system interface voltage response.

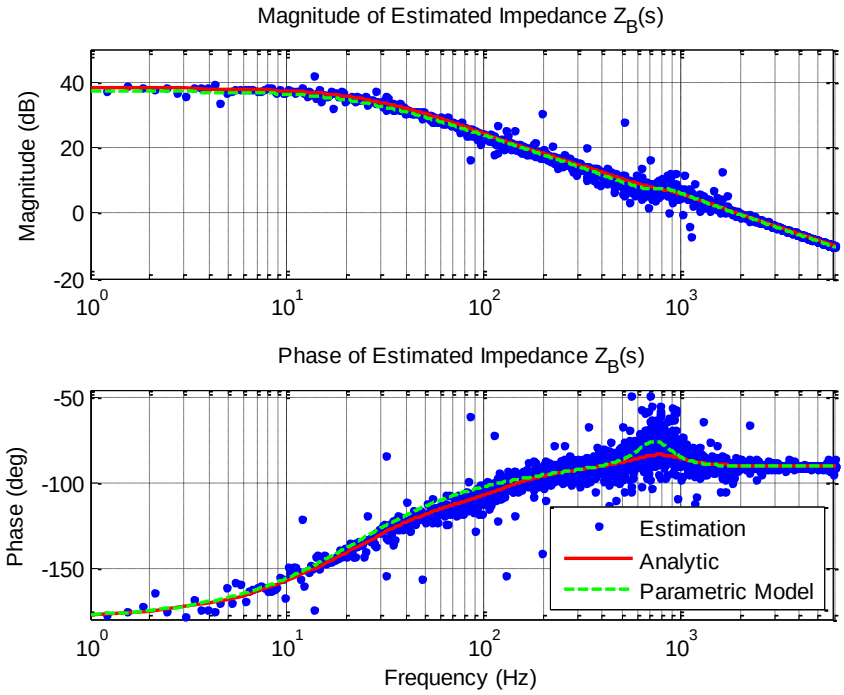


Figure 5.10. Bode plot of the HUT impedance non-parametric estimation data (blue), analytic model (red), and (b) fitted parametric model of the HUT impedance (dashed green) for MVDC system.

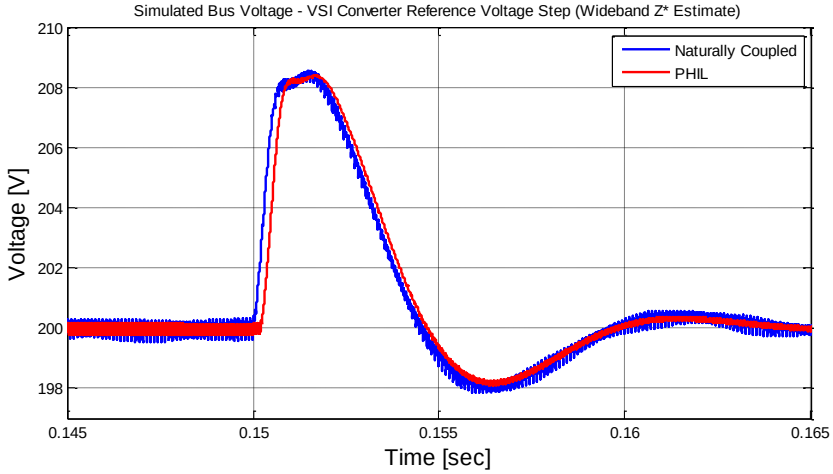


Figure 5.11. Zoom of load step change for a reference system (blue) and PHIL experiment (red) showing elimination of interface oscillations.

5.2 PHIL SYSTEM ACCURACY

In order to provide meaningful simulation data, the PHIL interface must be capable of accurately coupling the ROS software simulation to the HUT. Ideally, the power interface is transparent to all dynamics of interest between the ROS and HUT such that the full system is realized as if it were naturally coupled. However, in a real PHIL implementation, this interface is prone to error as a result of execution time limitations of the real-time computing platform and the interface amplifier characteristics. The significance of these error sources may be evaluated from two different perspectives: the voltage conversion ratio from the ROS to the HUT and the effect of the linking impedance, Z_{AB}, on the power interface output impedance.

Referencing the block diagram shown in Figure 5.3, the voltage conversion ratio from the ROS source voltage, u_1, to power interface output voltage, v_2' is given in (5.2). The ideal voltage conversion ratio obtained by a natural coupling of the ROS and HUT is given in (5.3). For this analysis, u_2 is zero.

$$G_{V-DIM}(s) = \frac{v_2'(s)}{u_1(s)} = \frac{\frac{Z_{AB}+Z^*}{Z_A+Z_{AB}+Z^*}\frac{Z_B}{Z_B+Z_{AB}}T_{FF}T_D}{1-G_{OL-DIM}} \tag{5.2}$$

$$G_{V-Ideal}(s) = \frac{Z_B}{Z_A+Z_B} \tag{5.3}$$

Based upon the previous discussion of stability, the damping impedance, Z^*, is ideally equal to Z_B, the HUT impedance. Thus, the IA loop gain is equal to zero, resulting in absolute stability. Equation (5.2) may be simplified under this assumption, resulting in (5.4).

$$G_{V-DIM}(s) = \frac{Z_A + Z_B}{Z_A + Z_B + Z_{AB}} T_{FF} T_D \frac{Z_B}{Z_A + Z_B} \tag{5.4}$$

Taking the ratio of (5.4) and (5.3) provides an expression for computing the interface error as a result of the linking impedances, computation delays, and interface amplifier bandwidth, (5.5).

$$E_V(s) = \frac{G_{V-DIM}(s)}{G_{V-Ideal}(s)} = \frac{Z_A + Z_B}{Z_A + Z_B + Z_{AB}} T_{FF} T_D \tag{5.5}$$

From this result, it is observed that the linking impedance will have little effect on the ROS to HUT voltage error as long as its value is significantly less than the sum of the ROS and HUT impedances. The error in the voltage conversion ratio is dominated by the interface amplifier bandwidth, T_{FF}, and real-time computation delay, T_D. The necessity for a wide power bandwidth interface amplifier and a real-time computation platform capable of fast execution times is readily apparent.

While the above analysis gives some insight into how to achieve an accurate PHIL test platform, it requires explicit knowledge of the HUT impedance to evaluate. The HUT impedance may also not be constant during the simulation, such that the anticipated error from (5.5) is difficult to quantify. Disturbances on the hardware side are also not considered and would require an additional set of equations, also requiring explicit HUT knowledge. An impedance based approach to ensuring accurate interface behavior that requires only knowledge of Z_A and Z_{AB} is presented below.

Accurate reproduction of the HUT loading effect on the simulated system requires that the impedance seen looking into the PHIL interface amplifier terminals (indicated as

$Z_{out\text{-}DIM}$ in Figure 5.2 be equal to Z_A, the ROS impedance. This fact can be shown as follows. The output impedance of the DIM IA is given in (5.6).

$$Z_{out-DIM}(s) = \frac{Z_{AB} + \dfrac{Z_A Z^* T_{FF} T_D T_{FB}}{Z_A + Z_{AB} + Z^*}}{1 - \dfrac{Z_A T_{FF} T_D T_{FB}}{Z_A + Z_{AB} + Z^*}} \tag{5.6}$$

Consider the following properties of an ideal power interface:

1. The interface amplifier has infinite power bandwidth; $T_{FF} = 1$.
2. No time delay associated with computation delay exists; $T_D = 1$.
3. The voltage and current sensors in the feedback path have an infinite bandwidth; $T_{FB} = 1$.
4. The linking impedance $Z_{AB} = 0$.

Application of these ideal properties to (5.6) results in the following simplification seen in (5.7).

$$Z_{out-DIM}(s) = \frac{Z_A Z^*}{Z_A + Z^* - Z_A} = Z_A \tag{5.7}$$

It is thus shown that, for an ideal interface exhibiting no amplifier or sensor bandwidth limitations, no time delay, and zero output impedance, the IA forces the interface power amplifier to have an output impedance $Z_{out\text{-}DIM}$ that is equal to the ROS impedance Z_A. Accordingly, the PHIL simulation will accurately reproduce the loading effect of the HUT upon the simulated ROS. In a real PHIL implementation, however, the interface power amplifier will have a fixed bandwidth (T_{FF}) and finite output impedance

(Z_{AB}). The voltage and current sensors will also exhibit limited bandwidth capabilities (T_{FB}) and the real-time simulator computing the ROS behavior and interface voltage reference will have a finite execution time (T_D). It is clear that these parameters must be optimized such that the resulting error incurred in $Z_{out\text{-}DIM}$ does not significantly alter the PHIL simulation results.

5.2.1 Interface Amplifier Design

Design of the interface power amplifier must consider the general overall dynamics of the experiments that the PHIL test platform is expected to perform. Quite simply, PHIL experiments are not a 'plug and play' simulation technology due to the variable stability of the power interface and inherent non-idealities in the simulated system configuration. Additionally, the above discussion of interface impedance demonstrates that the simulated ROS may require that the interface amplifier have an exceptionally low output impedance. This is especially important when the ROS is comprised of power converters whose control algorithms typically result in very small output impedances at low frequency, as is the scenario investigated in this work. However, a reasonably flexible PHIL platform may be designed if the interface power amplifier design is conceived under the constraints of requiring a low output impedance and high bandwidth and some knowledge of the test case system dynamics is available. This PHIL platform will be used to simulate the 1.5 kW MVDC distribution system described below.

The MVDC distribution system under study is of the same structure as that shown in Figure 5.5, consisting of a source buck converter (BKS) feeding a DC bus to which a load three-phase voltage source inverter (VSI) and load buck converter (BKL) are

connected. All converters operate under feedback control using an inner current loop and outer voltage loop PI strategy. The system is fed by a 400 V_{DC} source, establishes 200 V_{DC} at the bus connection, and operates at a nominal power level of 1.5 kW. For PHIL testing, the interface between simulation and hardware is defined at the bus connection of the load buck converter. Using the impedance notation of Figure 5.2, Z_A is the parallel combination of the source buck converter output impedance $Z_{out\text{-}BKS}$ and load VSI input impedance $Z_{in\text{-}VSI}$. The HUT impedance Z_B is the input impedance of the BKL. A time delay of 200 μs is assumed to exist as a result of computation delays within the real-time simulator. The complete converter parameters are given in Table 5-2.

Table 5.2. Complete Converter Hardware and Control Parameters for PHIL System Accuracy Evaluation

Parameter	BKS	BKL	VSI
f_{sw}	10 kHz	10 kHz	10 kHz
L_{filt}	3 mH	1 mH	1 mH
C_{filt}	50 μF	90 μF	90 μF
R_{load}	-	10 Ω	6.075 Ω
$K_{p\text{-}il}$	0.039	0.022	0.022
$K_{i\text{-}il}$	48.65	34.30	40.07
$K_{p\text{-}v}$	0.066	0.110	0.093
$K_{i\text{-}v}$	62.95	92.57	125.9

Both the accuracy and stability of the PHIL test platform are affected by control of the simulated damping impedance Z^* in the DIM IA. As previously discussed, interface stability can be ensured by setting the simulated damping impedance Z^* equal to the HUT impedance Z_B. In practice, this is accomplished using the impedance identification technique. For simplicity, consider that Z^* is equal to Z_B, such that the loop gain (5.1) goes to zero and the interface accuracy is affected only by the interface time delay, T_D, power amplifier bandwidth, T_{FF}, and interface amplifier output impedance, Z_{AB}

as shown in (5.6). The amplifier design is carried out in an effort to minimize Z_{AB}, the interface amplifier output impedance, such that the overall interface output impedance, $Z_{out\text{-}DIM}$, best approximates Z_A.

Since the ROS impedance is a known quantity and must be modeled in software, the interface amplifier may be designed to ensure that the amplifier output impedance Z_{AB} is significantly less than Z_A for all frequencies of interest. Two interface amplifier designs are carried out to demonstrate PHIL accuracy associated with interface amplifier output impedance. The output impedance of the first interface amplifier is called $Z_{AB\text{-}HIGH}$ and the impedance of the second amplifier is called $Z_{AB\text{-}LOW}$.

The first amplifier design is composed of a simple buck converter. This converter employs a multi-loop control strategy: an inner PI current loop and outer PI voltage loop to regulate the output voltage. The major parameters of this converter are shown in Table 5.3. The ouput impedance of this power amplifier, $Z_{AB\text{-}HIGH}$, is not significantly lower than the ROS impedance Z_A, resulting in interactions in the overall DIM interface impedance $Z_{out\text{-}DIM}$ shown in Figure 5.12. At low frequency, $Z_{AB\text{-}HIGH}$ is slightly larger than $Z_{A,}$ resulting in significant error in the interface output impedance ($Z_{out\text{-}DIM}$ and Z_A are different). At high frequency, the error shown is a result of the limitations of T_{FF}; $Z_{out\text{-}DIM}$ becomes equal to $Z_{AB\text{-}HIGH}$ as the amplifier is driven outside of its controllable bandwidth. Therefore, it is expected that this amplifier will contribute significant error to the simulation as a result of the inaccurate interface output impedance over a wide frequency range.

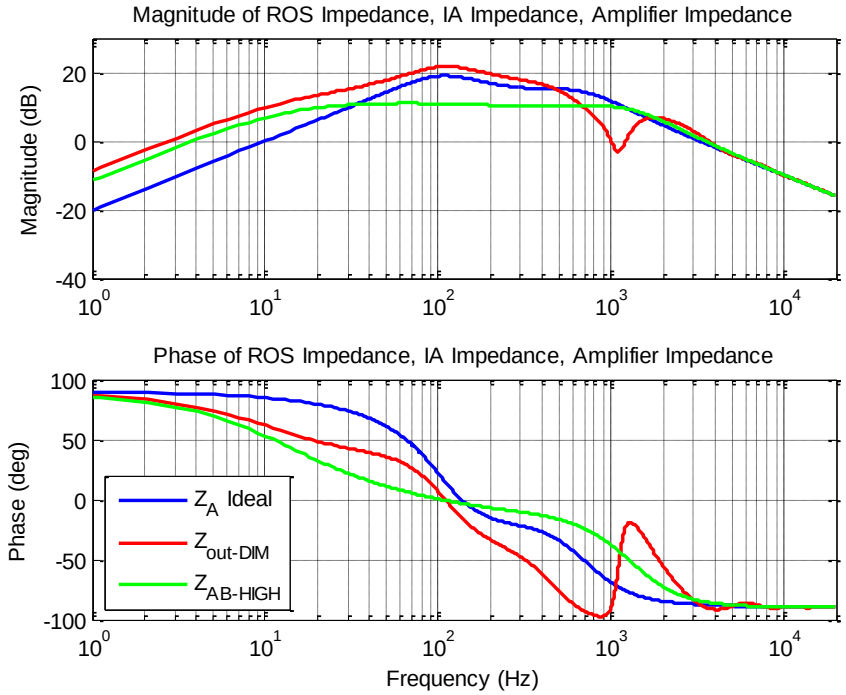


Figure 5.12. Comparison of ROS impedance (blue), DIM IA output impedance (red), and interface amplifier output impedance $Z_{AB\text{-}HIGH}$ (green).

A second interface amplifier design based on a three-leg interleaved buck converter was evaluated due to a number of benefits afforded by the topology. Converter interleaving has the advantage of reducing the output current ripple as well as increasing the ripple frequency. The interleaved topology also allows for a very low converter output impedance to be achieved using reasonably sized filtering components; a significant benefit in this application. A multi-loop control strategy was employed: each phase leg current is deadbeat controlled while an outer PI compensator regulates the output voltage. Let this amplifier output impedance be denoted as $Z_{AB\text{-}LOW}$. This impedance, along with Z_A and the resulting interface impedance, is shown in Figure 5.13. At low frequency, $Z_{AB\text{-}LOW}$ is much lower in magnitude than Z_A, such that the impedance seen looking into the interface amplifier terminals, $Z_{out\text{-}DIM}$, is equal to the ROS

impedance Z_A. This is the condition for good interface accuracy. At high frequency, $Z_{AB\text{-}LOW}$ is also lower than Z_A. However, the time delay present in the interface, T_D, results in a slight magnitude variation and significant phase lag in $Z_{out\text{-}DIM}$. $Z_{out\text{-}DIM}$ eventually becomes equal to $Z_{AB\text{-}LOW}$ as the effects of T_{FF} become apparent. Nonetheless, the dominance of the ROS impedance at the output terminals of the interface amplifier over a wide frequency range leads one to expect that the dynamics of the switching converter serving as the amplifier will contribute little error to the PHIL simulation.

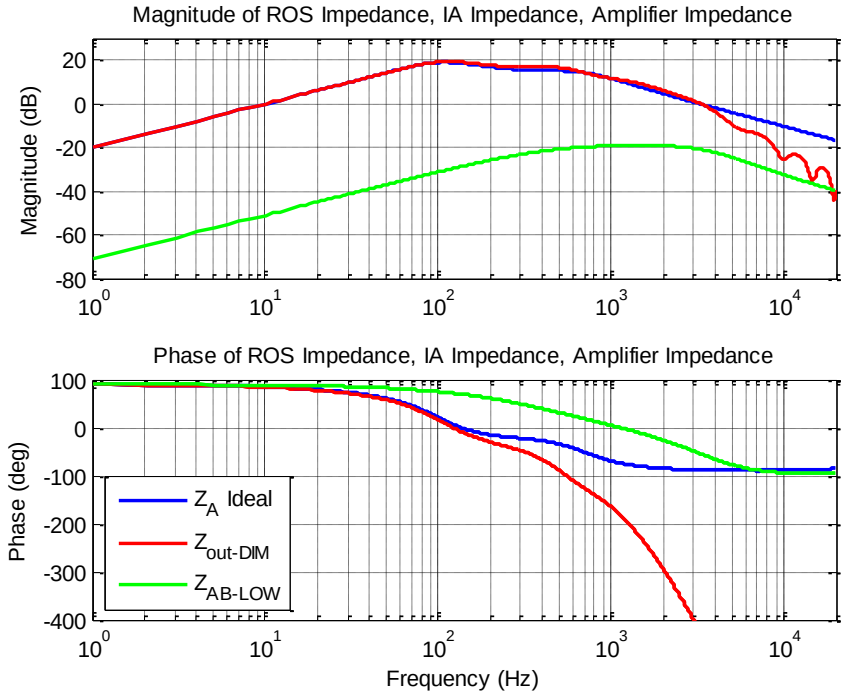


Figure 5.13. Comparison of ROS impedance (blue), DIM IA output impedance (red), and interface amplifier output impedance $Z_{AB\text{-}LOW}$ (green).

The major parameters of both interface amplifiers are given in Table 5.3. The feedback sensor bandwidth T_{FB} was assumed to be sufficiently high and was neglected in both cases.

Table 5.3. Interface Amplifier Design Parameters

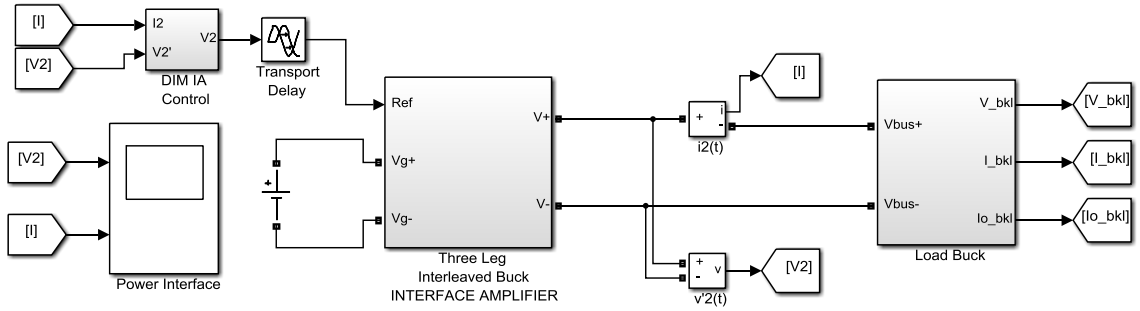
Parameter	Interface Amplifier Design	
	Amplifier Design #1 ($Z_{AB\text{-}HIGH}$)	Amplifier Design #2 ($Z_{AB\text{-}LOW}$)
V_g	400 V_{DC}	400 V_{DC}
L_{filt}	5 mH	1 mH
C_{filt}	50 µF	820 µF
f_{sw}	50 kHz	50 kHz
f_c	800 Hz	2 kHz
φ_m	75°	52°

5.2.2 Simulated Evaluation of Interface Amplifier Accuracy

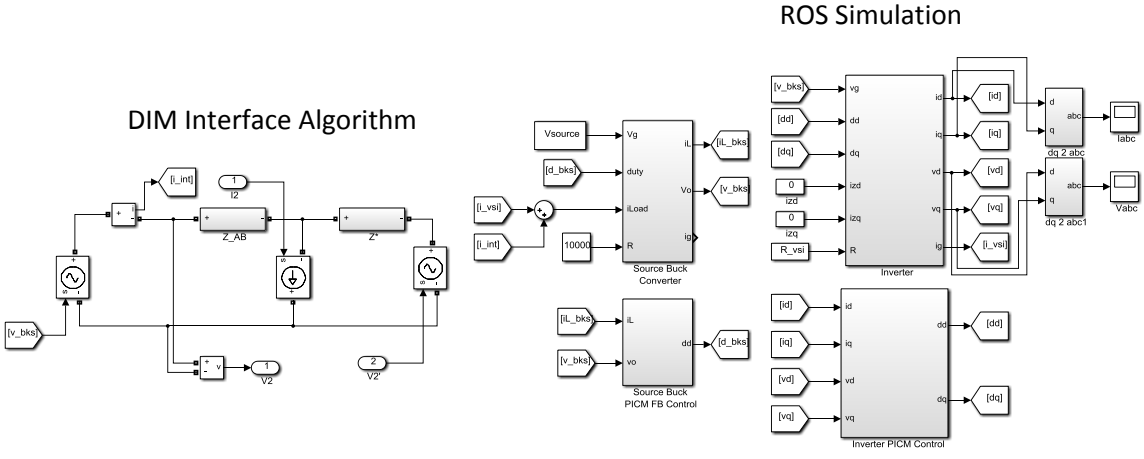
In this section, simulation results are provided for the PHIL test scenario of a scaled MVDC distribution system, shown in Figure 5.14. In order to demonstrate PHIL simulation inaccuracy as a result of interface amplifier output impedance, the two interface amplifier designs of the previous section are evaluated. A full switching model of the PHIL test platform including the interface amplifier was constructed in MATLAB/Simulink, Figure 5.14(a). The interface controller is modeled in Figure 5.14(b), and includes the DIM IA implementation and an averaged model of the ROS (source buck converter and load VSI). Note also that the interface amplifier output impedance Z_{AB} is included in the IA model. Simulink diagrams of the interface amplifier converter and control subsystems are contained in Appendix C.

To ensure stability of the PHIL interface, the impedance of the HUT is first estimated using the impedance identification procedure discussed in Section 5.1.1. To properly estimate the HUT impedance, the PHIL system must be operated at its intended steady-state operating point. To alleviate stability concerns during the identification procedure, an initial resistive estimate of the HUT impedance is implemented as the

simulated damping impedance, Z^*. The load buck converter HUT draws 1 kW from the 200 V_{DC} bus in steady-state operation, resulting in an initial value for Z^* of 40 Ω. While this value of Z^* allows for the PHIL simulation to be performed, it is not the ideal choice to ensure the system stability. The HUT impedance is likely to vary with frequency, resulting in the interface exhibiting reduced damping and, potentially, instability, as discussed previously. A Nyquist plot of the loop gain $G_{OL\text{-}DIM}$, Figure 5.15, shows that the interface is not unstable for the initial resistive Z^* estimate (blue), but could be further improved, i.e., reduced in magnitude (see (5.1)), if a wideband model of the HUT were available.



(a)



(b)

Figure 5.14. Simulink diagram of simulated PHIL test platform showing (a) interface amplifier and HUT interconnection and (b) DIM IA and ROS simulation

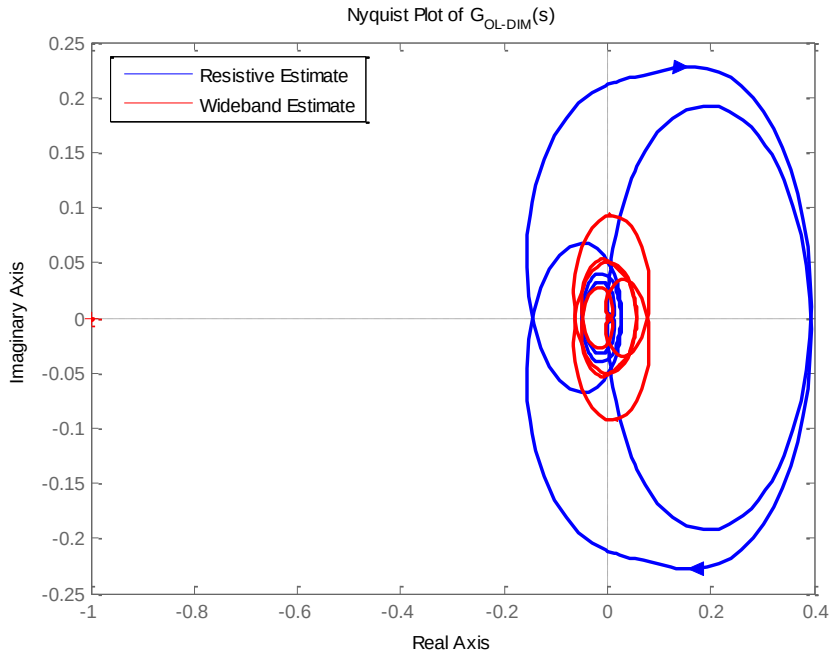


Figure 5.15. Nyquist plot of DIM IA loop gain using resistive estimate (blue) and wideband estimate (red) of Z^*.

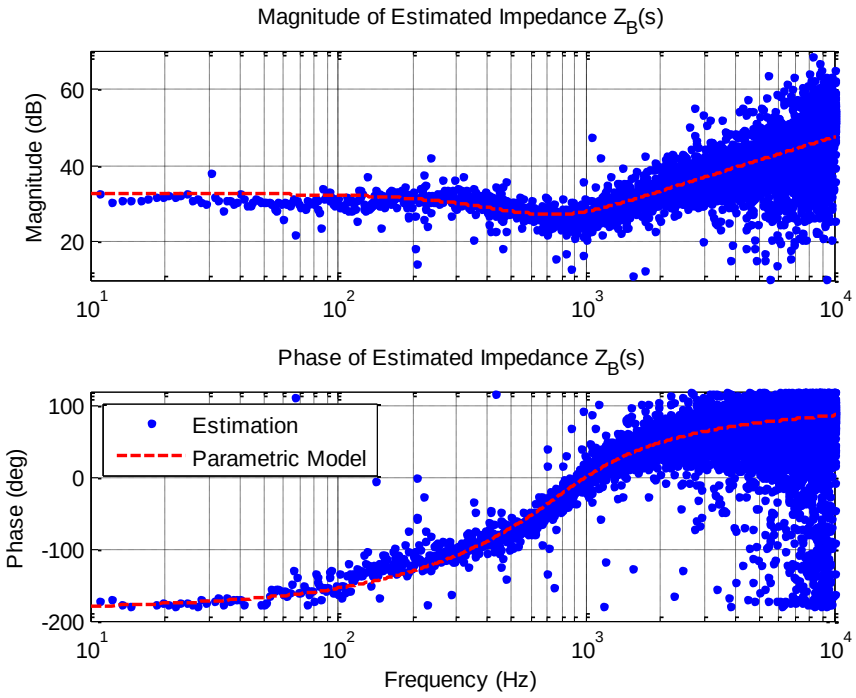


Figure 5.16. Bode plot of non-parametric estimate HUT impedance (blue) and parametric model (red).

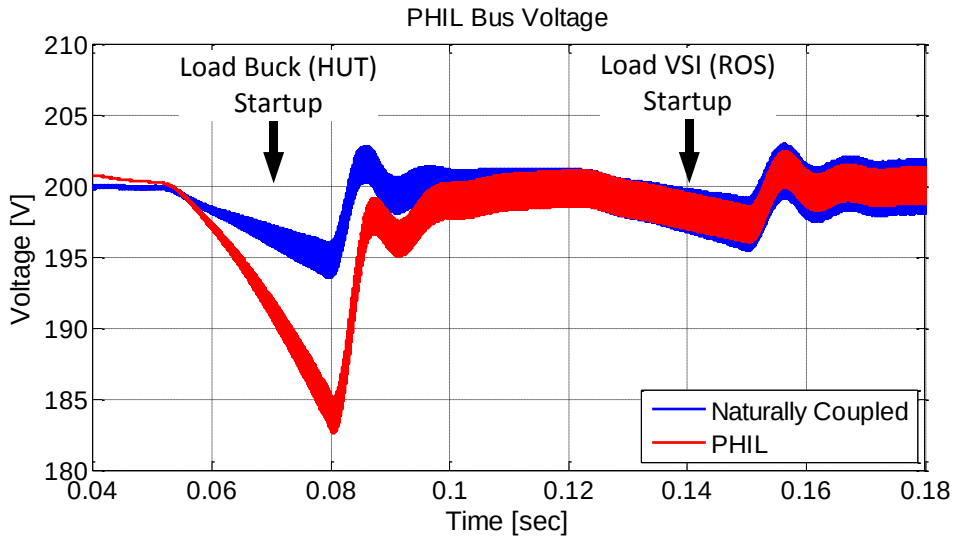
Following the establishment of the system bus voltage, the HUT is brought to steady-state operation. A 14-bit, 20 kHz PRBS test sequence is injected into the steady-state duty cycle command of the power interface converter and the resulting voltage and current perturbations at the interface output are captured such that a non-parametric estimation of the impedance Z_B may be constructed using cross-correlation based techniques. A parametric model of the estimation is then computed using Least Squares Fitting. The non-parametric estimation data and fitted impedance model are shown in Figure 5.16. This data is then used to update the simulated value of Z^*, resulting in the stability improvement evident in the Nyquist plot of Figure 5.15 (red). See Appendix C for details concerning the implementation of complex Thévenin impedances within Simulink. The IA damping has been increased, such that oscillations are unlikely to disturb the PHIL simulation results.

In the previous section, two interface amplifier designs were considered with particular attention paid to the resulting output impedance of the interface amplifier. The following transient simulation results demonstrate the importance of considering the interface amplifier output impedance during the design of a PHIL test platform.

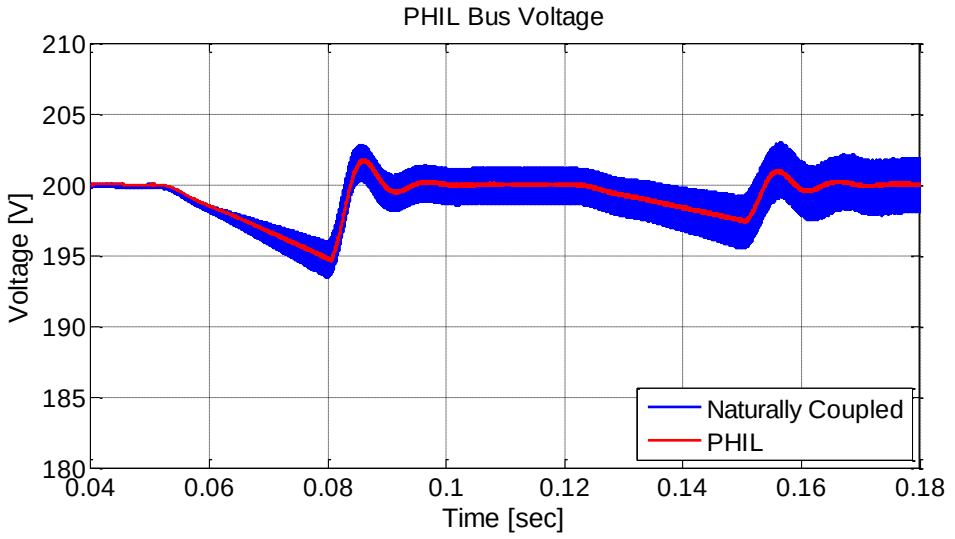
Consider first the interface amplifier design having an output impedance of $Z_{AB\text{-}HIGH}$. A transient simulation of the PHIL platform (red) for two test events is shown in Figure 5.17(a) and compared with the results of a naturally coupled reference system (blue). Beginning at t = 0.05 sec, the load buck converter (HUT) ramps up, establishing 100 V_{DC} at its output. This action results in an observable sag in the system bus voltage that recovers once the HUT has entered steady-state operation. At t = 0.12 sec, the load VSI (ROS) begins operation, ramping its output to 80 V_{PK}. Again, a sag is introduced in

the system bus voltage. As a result of the high interface amplifier output impedance, a significant error is shown to occur during the HUT turn on procedure. The interface amplifier is unable to accurately reproduce the loading effect the HUT has on the ROS due to the interaction of its own output impedance. This behavior was predicted by the Bode plot of Figure 5.12, which depicted an overall interface output impedance with significant deviations from that of the ROS. The error shown in the transient simulation confirms the notion that accurate PHIL results are predicated on the ability of the interface to reproduce the ROS impedance at the power amplifier terminals. The second event represents a change in the behavior of the simulated ROS resulting in a variation of the bus voltage. Accordingly, the PHIL simulation exhibits good matching with the naturally coupled reference, as the transient is caused by an event within the ROS simulated part of the system rather than by a loading effect at the software-hardware interface.

The accuracy improvements afforded by the interface amplifier having an output impedance of $Z_{AB\text{-}LOW}$ are evident in the simulation results of Figure 5.17(b). Under the same test conditions as previously shown, the PHIL platform exhibits excellent matching with that of the naturally coupled reference system. The system now accurately models the bus voltage sag as a result of the HUT startup transient, a condition where significant error was previously observed. The VSI (ROS) startup event is also simulated with great accuracy, such that the PHIL test platform can now produce accurate simulation results for both HUT and ROS imposed transient events.



(a)



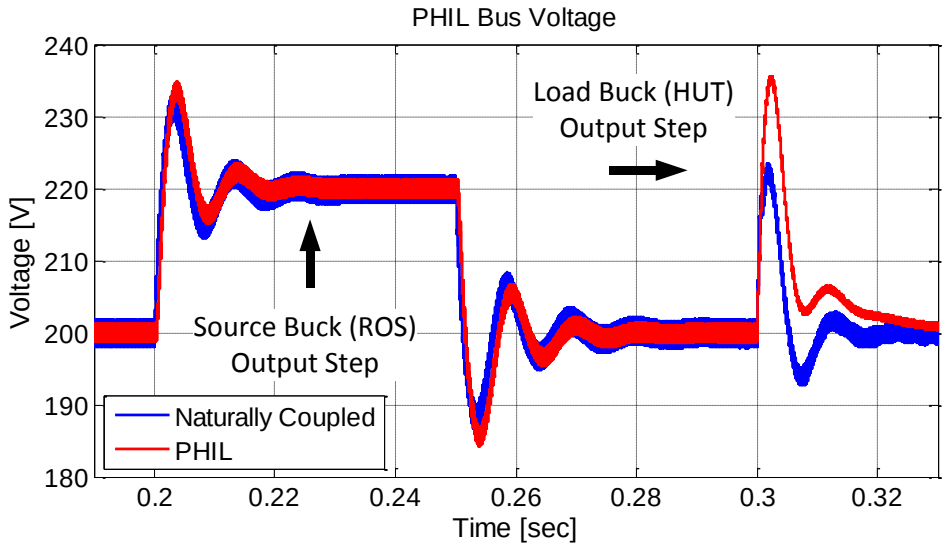
(b)

Figure 5.17. Transient simulation of HUT startup and ROS startup for PHIL interface using (a) high output impedance interface amplifier $Z_{AB\text{-}HIGH}$ and (b) low output impedance interface amplifier $Z_{AB\text{-}LOW}$.

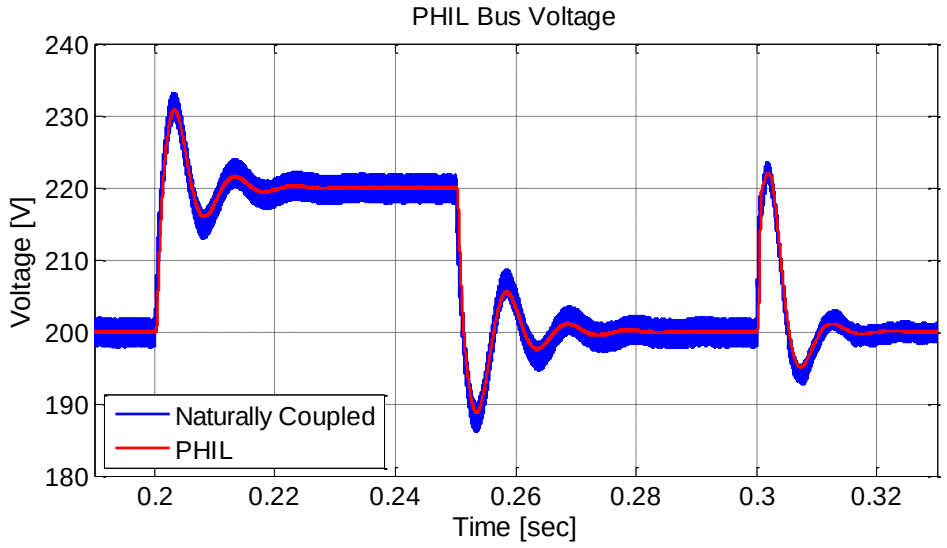
Consider a second set of PHIL test scenarios shown in Figure 5.18(a) for the interface amplifier having an output impedance $Z_{AB\text{-}HIGH}$. At t = 0.2 sec, the source buck converter (ROS) initiates a ±20 V_{DC} step voltage change of its output, which ends at t = 0.25 sec. Finally, at t = 0.3 sec, the load buck converter (HUT) steps its output voltage to 50 V_{DC}, half the nominal value. During the step voltage change, the PHIL simulation

results demonstrate good matching with the reference system. The resulting bus voltage oscillation is accurately modeled according to the results of the reference system simulation. However, a significant error is evident during the load buck converter (HUT) output voltage step change. The resulting bus voltage oscillation has significantly higher amplitude with respect to the reference system results. The PHIL system also requires a significantly longer amount of time to return to steady-state operation. This error is again attributed to the higher interface amplifier output impedance. The interface amplifier is unable to accurately model the loading effect of the HUT upon the ROS due to the inaccurate interface output impedance. However, it was again shown that the interface may still accurately model ROS imposed events upon the HUT, since the transient is not caused by a loading effect that exercises the feedback loop present at the PHIL interface.

The above test scenarios were performed again, Figure 5.18(b), using the interleaved interface amplifier having the output impedance $Z_{AB\text{-}LOW}$. As a result, the accuracy of the PHIL platform is significantly improved. The PHIL simulation results demonstrate excellent matching with those of the reference system for both the ROS imposed bus voltage step and HUT imposed bus voltage oscillation. The interface amplifier now models the ROS impedance more accurately, resulting in the improved simulation results.



(a)



(b)

Figure 5.18. Transient simulation of ROS reference step and HUT reference step for PHIL interface using (a) high output impedance interface amplifier $Z_{AB\text{-}HIGH}$ and (b) low output impedance interface amplifier $Z_{AB\text{-}LOW}$.

5.3 Conclusion of PHIL Stability and Accuracy Improvements

This chapter proposed techniques to improve both the stability and accuracy of PHIL test platforms used for early testing of MVDC system hardware. A PHIL interface algorithm is augmented with wideband impedance identification capabilities. The

interface power amplifier is used to perturb the connected HUT such that a model of the hardware can be incorporated into the DIM IA. This is shown to significantly increase the stability margins of the IA and eliminate undesirable oscillations originally present in the interface. The stability improvement is confirmed in the time domain through simulation of a scaled MVDC distribution system PHIL experiment.

Impedance based design constraints for the construction of a PHIL interface amplifier are developed. It is shown that a highly accurate PHIL simulation may be obtained given that the interface amplifier is designed with knowledge of the ROS impedance and dynamics. Maintaining an interface amplifier output impedance lower than that of the ROS impedance is crucial in obtaining accurate simulations. Two example interface amplifiers are evaluated in regard to this requirement in both the frequency and time domain. The accuracy improvement afforded by adherence to the developed constraints is observed in the PHIL simulation of a scaled MVDC power distribution system.

CHAPTER 6

SIMULATED MVDC PHIL STABILITY EVALUATION AND IMPEDANCE BASED CONTROL DESIGN

PHIL simulation techniques may be very useful for examining the behavior of large systems when an additional hardware component is added. In this chapter, the stability of a scaled notional MVDC power distribution system is assessed via PHIL simulation when an additional converter is connected. The stability analysis is accomplished by application of the proposed PBSC and AIR stability analyses presented previously in Chapter 3 to the measured system bus impedance. A PFF controller is designed based on the bus impedance identification results for the new piece of hardware, thereby ensuring that the system bus impedance is well damped and will not result in unstable or oscillatory behavior. Stability and accuracy evaluations of the PHIL test platform itself are also performed using the techniques presented in Chapter 5. Simulation results from a full switching model of the PHIL simulation platform and distribution system components are presented to validate the hardware and control design tools.

6.1 MVDC SYSTEM DESCRIPTION

A functional schematic of the notional DC power distribution system for PHIL simulation is shown in Figure 6.1. The notional system consists of a source buck converter (BKS) feeding a DC bus, to which a load three-phase voltage source inverter

(VSI) and load buck converter (BKL) are connected. All converters operate under feedback control using an inner current loop and outer voltage loop PI strategy. The system is fed by a 400 V_{DC} source, establishes 200 V_{DC} at the bus connection, and operates at a nominal power level of 1.5 kW. The complete parameters for each converter in the system are given in Table 6.1.

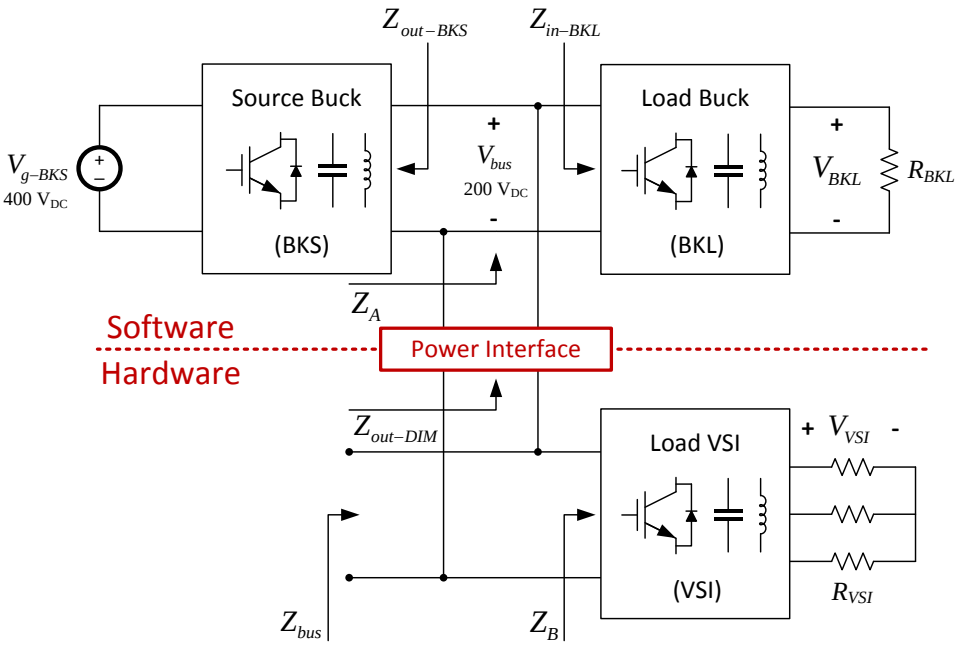


Figure 6.1. Scaled MVDC distribution system PHIL test scenario comprised of an interconnected source buck converter, load buck converter, and load VSI.

Table 6.1. Complete PHIL Simulated Converter Parameters

Parameter	BKS	BKL	VSI
f_{sw}	10 kHz	10 kHz	10 kHz
L_{filt}	3 mH	1 mH	1 mH
C_{filt}	50 µF	90 µF	90 µF
R_{load}	-	10 Ω	6.075 Ω
$K_{p\text{-}il}$	0.035	0.022	0.022
$K_{i\text{-}il}$	109.6	34.30	40.07
$K_{p\text{-}v}$	0.042	0.110	0.093
$K_{i\text{-}v}$	60.48	92.57	125.9

For PHIL testing, the interface between simulation and hardware is designated at the bus connection of the VSI. Using the impedance notation of Figure 5.2, Z_A is the parallel combination of the BKS output impedance and the BKL input impedance. The HUT impedance Z_B is the input impedance of the load VSI. A time delay of 40 μs is assumed to exist as a result of I/O and internal computation delays of the real-time simulator.

6.2 PHIL Interface Algorithm Accuracy and Stability Evaluation

As discussed in Chapter 5, accuracy of the PHIL test platform can be guaranteed by imposing impedance based constraints on the design of the interface power amplifier. Since the ROS impedance is a known quantity and must be modeled in software, the interface amplifier may be designed to ensure that the amplifier output impedance Z_{AB} is significantly less than Z_A for all frequencies of interest. The power interface amplifier design considered in this work is a three-leg interleaved buck converter, as discussed in Chapter 5. A multi-loop control strategy is employed: each phase leg current is deadbeat controlled while an outer PI compensator regulates the output voltage. The complete parameters of the interface amplifier are given in Table 6.2.

Table 6.2. Complete PHIL Interface Amplifier Parameters

Parameter	Value
V_g	400 V_{DC}
L_{filt}	1 mH
C_{filt}	900 μF
f_{sw}	50 kHz
$K_{p\text{-}v}$	3.4348
$K_{i\text{-}v}$	7447.8

The amplifier output impedance, along with the ROS impedance and the resulting interface impedance, is plotted in Figure 6.2. At low frequency, Z_{AB} is much lower in magnitude than Z_A, such that the impedance seen looking into the interface amplifier terminals, $Z_{out\text{-}DIM}$, is equal to the ROS impedance, Z_A. This is the condition for good interface accuracy. At high frequency, Z_{AB} is also lower than Z_A. However, the time delay present in the interface, T_D, results in a slight magnitude reduction and significant phase lag in $Z_{out\text{-}DIM}$ with respect to Z_A. Eventually, $Z_{out\text{-}DIM}$ becomes equal to Z_{AB} as the effects of the converter finite bandwidth, T_{FF}, become apparent. Nonetheless, the dominance of the ROS impedance at the output terminals of the interface amplifier over a wide frequency range leads one to expect that the dynamics of the switching converter serving as the interface amplifier will contribute little error to the PHIL simulation.

To ensure stability of the PHIL interface, the impedance of the HUT is first evaluated according to the method discussed in Chapter 5. To properly estimate the HUT impedance, the PHIL system must be operated at its intended steady-state operating point. To alleviate stability concerns during the identification procedure, an initial resistive estimate of the HUT impedance is implemented as the simulated damping impedance, Z^*. The load VSI converter (HUT) draws 500 W from the 200 V_{DC} bus in steady-state operation, resulting in an initial value of $Z^* = 200^2/500 = 80\ \Omega$. While this value of Z^* allows for the PHIL simulation to be performed, it is not the ideal choice of $Z^* = Z_B$ that would ensure system stability. The HUT impedance Z_B actually varies with frequency, resulting in the interface exhibiting reduced damping, and, potentially, instability.

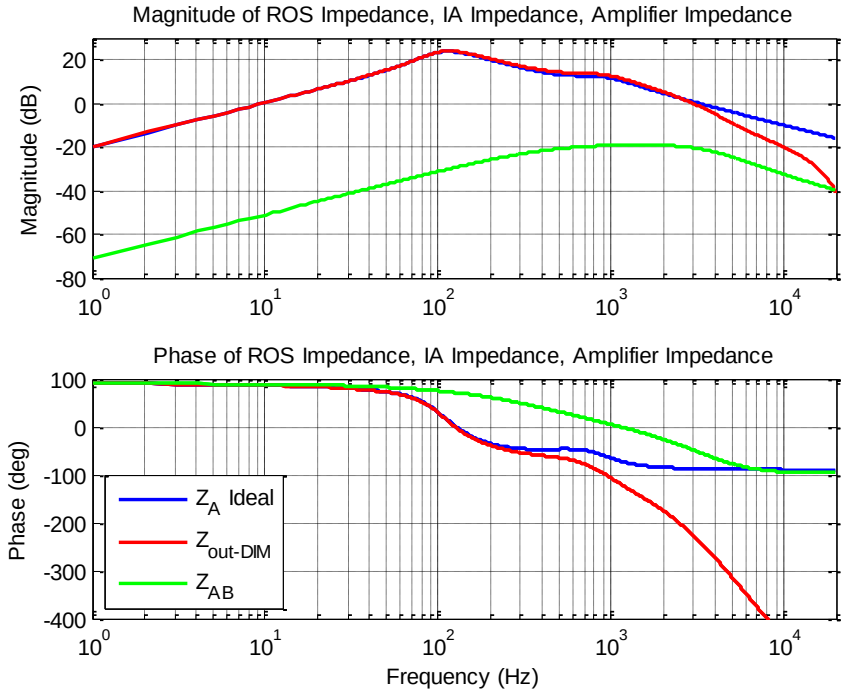


Figure 6.2. Comparison of ROS impedance (blue), DIM IA output impedance (red), and interface amplifier output impedance (green).

A Nyquist plot of the loop gain $G_{OL\text{-}DIM}$, Figure 6.3, shows that the interface is not unstable (no encirclement of the (-1, 0) point) for the initial resistive Z^* estimate (blue), but could be further improved (the maximum amplitude of the Nyquist plot could be reduced). Identification of HUT impedance is accomplished by injecting a 16-bit, 20 kHz PRBS test sequence into the steady-state duty cycle command of the power interface converter. The resulting current and voltage perturbations at the interface are captured such that a non-parametric estimation of the impedance Z_B may be constructed using cross-correlation techniques [26]. Notice the -80 Ω value at low frequency due to the output feedback and the inductive asymptote at high frequency related to the VSI output filter. A parametric model of the estimation is then computed using Least Squares Fitting [40]. The non-parametric estimation data and fitted impedance model are shown in

Figure 6.4. This data is then used to update the simulated value of Z^*, resulting in the stability improvement evident in the Nyquist plot of Figure 6.3 (red). See Appendix C for more details regarding implementation of complex impedances within Simulink.

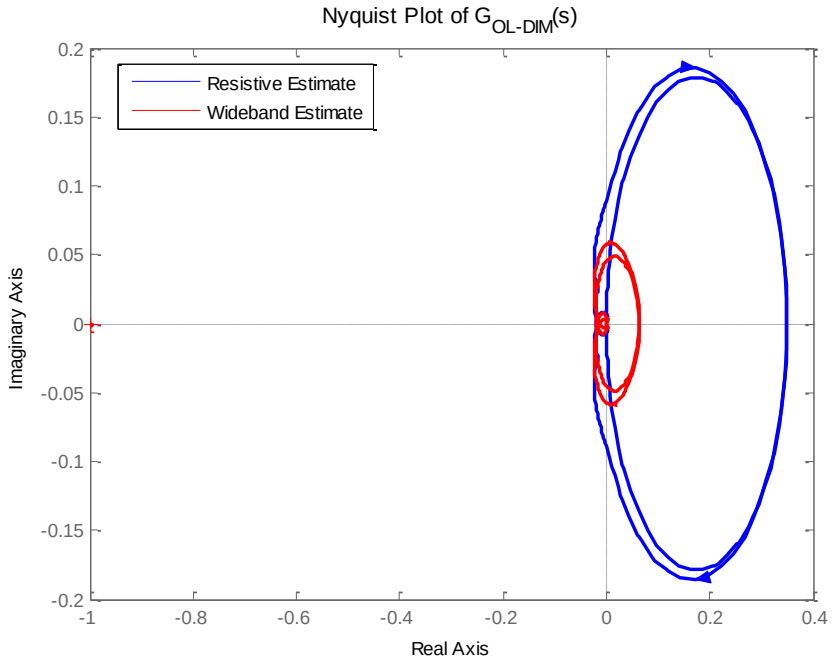


Figure 6.3. Nyquist plot of DIM IA loop gain using resistive estimated (blue) and wideband estimate (red) of Z^*.

The IA damping has been increased, such that IA oscillations are unlikely to occur and affect the PHIL simulation results. Stability analysis of the scaled notional MVDC system can now be performed with assurance that the PHIL test bed does not significantly contribute dynamics of its own into the simulation results, which could lead to an incorrect assessment of the system-under-test behavior.

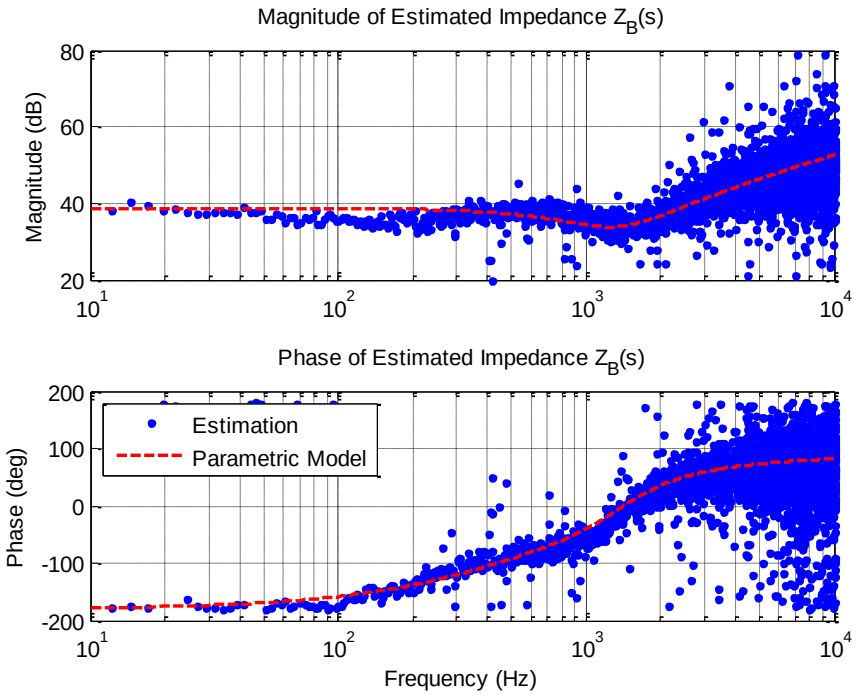


Figure 6.4. Bode plot of non-parametric estimated HUT impedance (blue) and parametric model (red).

6.3 MVDC System Stability Analysis and Controller Design

Stability analysis of the PHIL simulated MVDC system begins with identification of the system bus impedance $Z_{bus\text{-}FB}$, indicated in Figure 6.1. An additional converter, not shown in Figure 6.1, is included in the system and used to conduct measurements of the system bus impedance. This converter is used as a perturbation source to excite the system bus and allow for measurement of the bus impedance while the system is operating in steady-state. The converter sinks only a few percent of the nominal operating power from the bus such that interaction of its input impedance with the system bus impedance, leading to reduced damping, is avoided. The non-parametric and fitted parametric models of the bus impedance under feedback control only, $Z_{bus\text{-}FB}$, are shown in Figure 6.5. The bus impedance is shown to have a phase within the range of ±90° from

10 Hz to approximately 600 Hz. The additional phase lag at higher frequencies, due to the interaction of the interface amplifier dynamics with the PHIL simulation results, occurs significantly above the IA bandwidth and therefore does not affect stability. This notion is confirmed by the previous accuracy analysis shown in Figure 6.2 where $Z_{out\text{-}DIM}$ exhibits significant phase deviation from Z_A at high frequency.

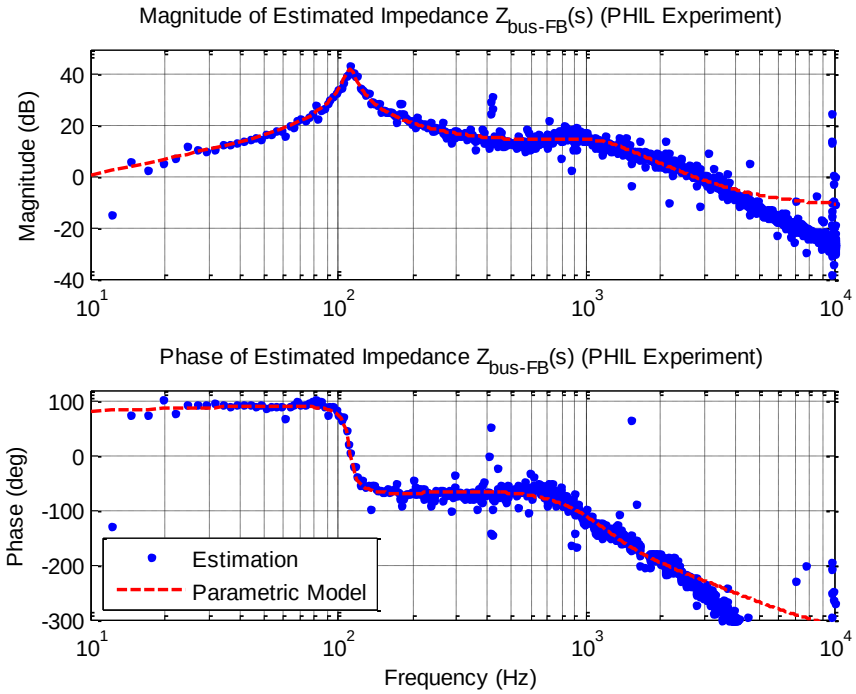


Figure 6.5. Bode plot of non-parametric estimated bus impedance (blue) and fitted parametric model (red) of PHIL simulated system.

A significant resonance is present on $Z_{bus\text{-}FB}$. The resonant frequency and normalization factor $Z_{0\text{-}bus}$ (see (3.12)) are extracted from the parametric model of the bus impedance for the PFF control design. The Nyquist contour of the normalized bus impedance (3.4) is shown in Figure 6.6 (dashed). The contour is shown to extend past the Allowable Impedance Region boundary for a desired system bus damping of $\zeta_{min} = 0.5$. A summary of the PFF control design according to (3.10)-(3.11) is given in Table 6.3.

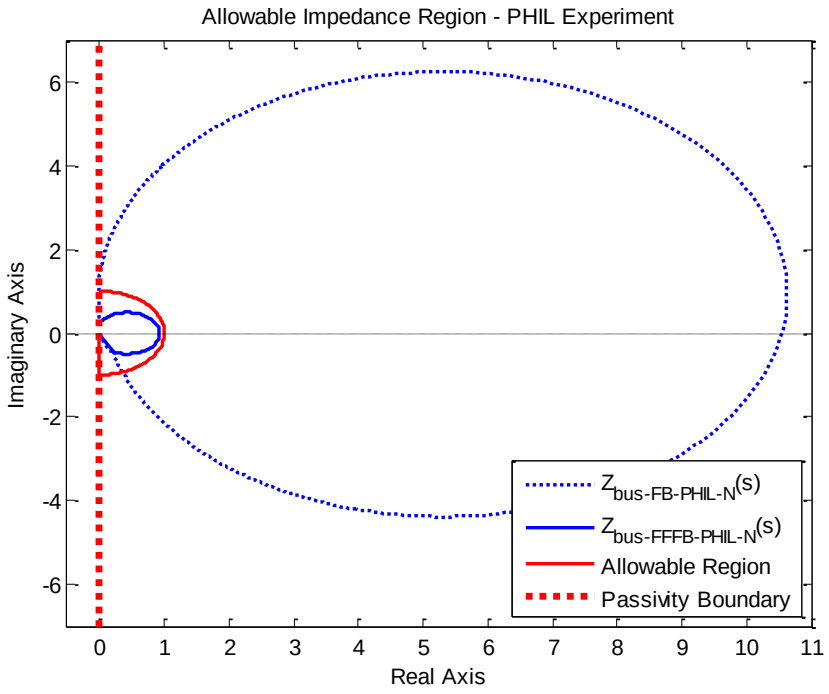


Figure 6.6. Nyquist plot of normalized estimated PHIL simulated bus impedance and AIR (ζ_{min} = 0.5) for system operating under FB control only (dashed) and FFFB control (solid).

Table 6.3. Bus Impedance and PFF Control Design Summary

Parameter	Value
$f_{0\text{-}bus\text{-}FB}$	111.4 Hz
$\zeta_{bus\text{-}FB}$	0.0485
$Z_{0\text{-}bus}$	11.86 Ω (21.48 dBΩ)
K_m	0.250
ζ_{damp}	1.000
$Z_{0\text{-}damp}$	4.796 Ω (13.62 dBΩ)

The design of Table 6.3 results in an equivalent *RLC* virtual damping impedance placed in parallel with the HUT VSI input terminals where R_b = 9.592 Ω, L_b = 6.849 mH, and C_b = 297.8 µF. A Bode plot of the non-parametric and fitted parametric system bus impedance when operated under FFFB control is shown in Figure 6.7. Following normalization, the bus impedance Nyquist contour is evaluated against the Allowable Impedance Region, Figure 6.6 (solid). The designed PFF controller is shown to damp the

previously observed resonance such that the contour lies completely within the specified region.

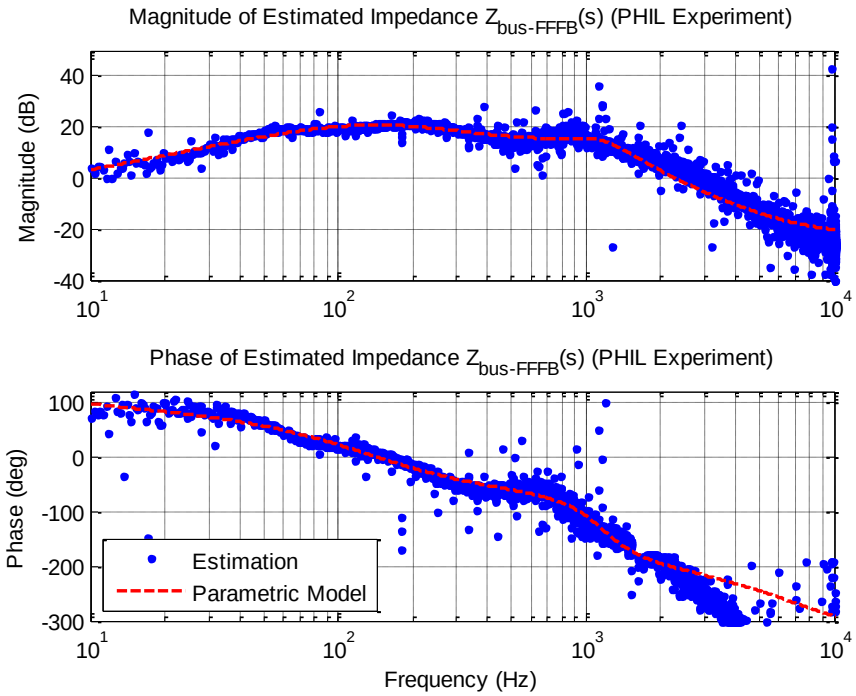


Figure 6.7. Bode plot of non-parametric estimated bus impedance (blue) and fitted parametric model (red) of PHIL simulated system.

Time domain results of the system operating under FB only (blue) and FFFB control (red) are shown in Figure 6.8 for a HUT VSI output voltage reference step of 22.5 V_{PK} to 45 V_{PK} (50% to 100% full output voltage). The PFF controller designed using the wideband bus impedance estimation from the PHIL simulation is shown to improve the system response by eliminating undesired bus voltage oscillations.

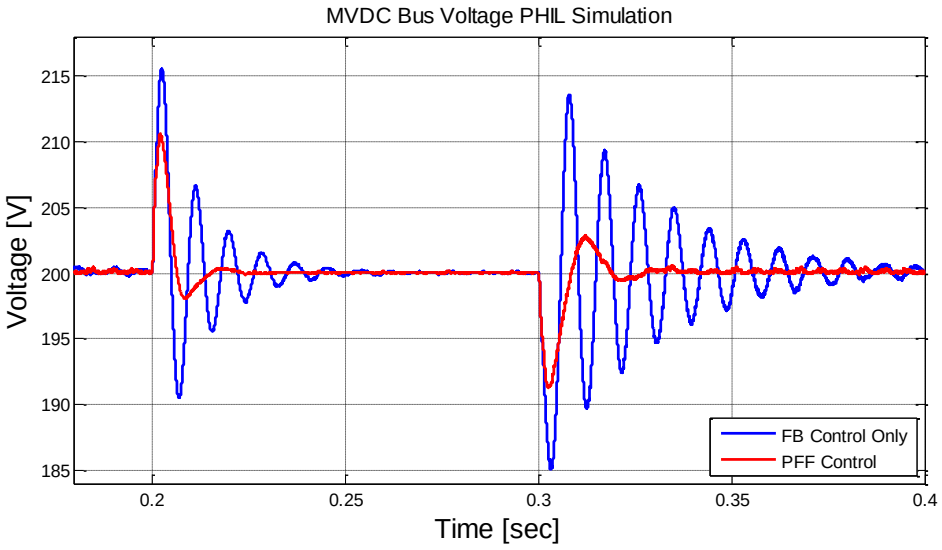


Figure 6.8. Transient simulation of MVDC bus voltage under feedback control only (blue) and FFFB control (red) during VSI output voltage reference steps.

6.4 Conclusion of MVDC System Design Using PHIL Simulation

This chapter provides simulated results of a PHIL test bed used for MVDC distribution system stability analysis and control design. The presented PHIL simulator provides design engineers with increased capabilities to perform thorough testing and analysis of new hardware prior to commissioning within an actual power system.

A PHIL test bed employing the highly stable and accurate DIM interface presented in Chapter 5 is used in simulation to perform a stability analysis on a scaled 1.5 kW MVDC distribution system consisting of three converters interconnected at a single-bus. System stability is evaluated using the PBSC and AIR analysis techniques presented in Chapter 3. A PFF control is designed to damp the system bus impedance such that the normalized contour of the bus impedance fits within the specified allowable region, thereby ensuring good dynamic behavior of the system. Time domain simulation

confirms that the PFF control implementation drastically improves the system response to disturbances.

The successful simulation results demonstrate both the capabilities of the PHIL test bed in the evaluation of complex and interacting systems as well as the effectiveness of the PBSC, AIR, and PFF control techniques in stabilizing controller design.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 CONCLUSIONS

This work was motivated by the increasing presence of power electronic converters in DC distribution systems and the related challenges of ensuring system stability and designing appropriate controllers to achieve good operating performance. Modeling and analysis of the switching converter interactions leading to instability and dynamic performance issues is a difficult and not fully understood problem. A design oriented methodology is necessary for the development of a targeted control approach such that these types of systems function reliably and perform well under a wide range of operating conditions.

In Chapter 2, an unterminated two-port small-signal model for a buck type switching converter was developed. The converter model is left unterminated to allow for multiple converter models to be interconnected such that large distribution networks may be studied analytically. The model was first developed in the open-loop case to highlight the necessity of determining the system operating point. Closed-loop controls were then incorporated into the model so that off-the-shelf converters can be easily modeled and incorporated into multi-converter system models.

Chapter 3 extends the application of the Passivity Based Stability Criterion (PBSC) and Positive Feed-Forward (PFF) control techniques to multi-bus systems. This

application to more general converter-based distribution networks requires the evaluation of all system bus self-impedances for the passivity condition in a determination of overall system stability. A new technique for analyzing the system's dynamic behavior was proposed by specifying a region in the *s*-plane in which the Nyquist contour of the system bus impedance must reside. If the Nyquist contour is observed to lie wholly in the Allowable Impedance Region (AIR), the system can be expected to be well damped. This additional level of analysis leads to a simplified PFF control design, as the virtual damping impedance is now synthesized to ensure that the bus impedances lie within the specified region.

In Chapter 4, the effectiveness of the PBSC, AIR, and PFF control design were evaluated in simulation and experiment for a scaled multi-bus system consisting of four switching converters. Two test scenarios were evaluated in which a prominent bus impedance was observed, requiring additional damping via PFF control. The system bus self-impedances of the experimental system were estimated using wideband impedance identification techniques. The experimentally obtained models were then evaluated using the proposed AIR analysis method to characterize the nature of the bus impedance resonances. PFF controllers were designed based on the obtained data in a demonstration of impedance based adaptive control of MVDC distribution systems.

The application of PHIL simulation techniques was explored in Chapter 5. The Damping Impedance Method interface algorithm was specifically studied due to its robust stability and accuracy. The incorporation of wideband impedance identification into the algorithm provides enhanced stability of the PHIL test platform as well as additional capabilities for characterization of the connected hardware under test. An

analysis of the accuracy based on the interface algorithm output impedance was conducted, leading to the development of impedance based design constraints for the interface amplifier for ensuring accurate PHIL simulations.

Finally, in Chapter 6 the improved PHIL test platform was used in simulation to evaluate the stability of an interconnected multi-converter system. This scenario is similar to what is envisioned as a potential role for PHIL simulation in the early evaluation of hardware components destined for use in MVDC distribution systems. The PHIL simulation results are used to characterize the stability and performance of the system via wideband impedance identification of the bus impedance. A suitable PFF control is designed using the impedance estimation results following evaluation using the proposed AIR analysis. The PHIL simulator was shown to be capable of accurately replicating the dynamic behavior of a complex, coupled converter system.

7.2 Future Work

7.2.1 Full Online Implementation of Impedance Based Control Techniques

The development and implementation of a full online robust adaptive control utilizing these impedance monitoring and impedance based control techniques is desired. Due to the simultaneous need of speed in calculation and the large amount of memory required to store the sampled impedance data, an embedded controller implementation using a Field Programmable Gate Array (FPGA) will be investigated. This platform benefits from a naturally parallel execution architecture and foregoes the system overhead and background computations commonplace on microprocessor based embedded platforms. A high performance computation platform can be constructed to

perform the various tasks required to achieve a full online implementation of adaptive impedance-based control.

To achieve a true online and adaptive system, refinements to the impedance identification procedure to facilitate hardware implementation must be made. Currently, obtaining accurate impedance identification results is paramount. For this reason, 14-bit PRBS injection sequences (16,383 terms) are used in the laboratory. The technique of oversampling the voltage and current quantities to improve the high frequency accuracy of the measurement [27] then increases the number of measured data points far beyond this number. Utilization of injection sequences of this length and oversampling require a significant amount of memory be available to store the measured data. The length of the injection is related to the lowest frequency that can be identified from the measurement. Thus, it would be beneficial to determine the injection sequence length based on the anticipated system bus impedance dynamics where it is expected that impedance information will be useful and necessary to obtain. Measurement of low frequency saliencies requires longer injection sequences and, typically, more memory. However, decreasing the number of terms in the perturbation sequence and the injection frequency will reduce the amount of sampled data required while still allowing for good low frequency estimation of impedances. This consideration will reduce the computation load of the system and lower the associated memory requirements. Other excitation sources, including Discrete Interval Binary Sequence (DIBS) and sinusoidal excitation methods will be explored.

An algorithm to perform data thinning and Least Squares Fitting on an embedded platform must be developed. The theory behind these techniques has been well explained

[21], but remains to be implemented on an embedded platform. Following the capture of voltage and current data from the perturbed bus, a procedure is followed to logarithmically thin the data to a specified number of points. A Least Squares Fitting technique is then used to fit the estimated non-parametric impedance data to a candidate transfer function having a user-specified number of poles and zeroes. It has been observed in simulation that the accuracy of the resulting parametric model is highly dependent on both the number of data points available after thinning and the order of the candidate transfer function. The use of candidate transfer functions that overestimate the order of the actual system typically results in parametric models in which the extraneous poles and zeroes are placed at very high frequencies. If this occurs for non-parametric data that has been excessively thinned, the low frequency fitting is typically compromised. More investigation to refine these techniques and implement them in hardware is needed.

7.2.2 Extension of Impedance Based Control Techniques to More Complex MVDC Distribution System Scenarios

Application of the PBSC and PFF control design technique for stabilizing multi-converter systems has thus far been limited in application to simple converter systems with resistive loads. Expansion of this testbed to include a more diverse set of power electronic enabled equipment will allow for a more thorough investigation of the proposed techniques and their efficacy in solving the design challenges encountered in the MVDC distribution system proposed for the all-electric ship. An example expanded hardware test bed is shown in Figure 7.1.

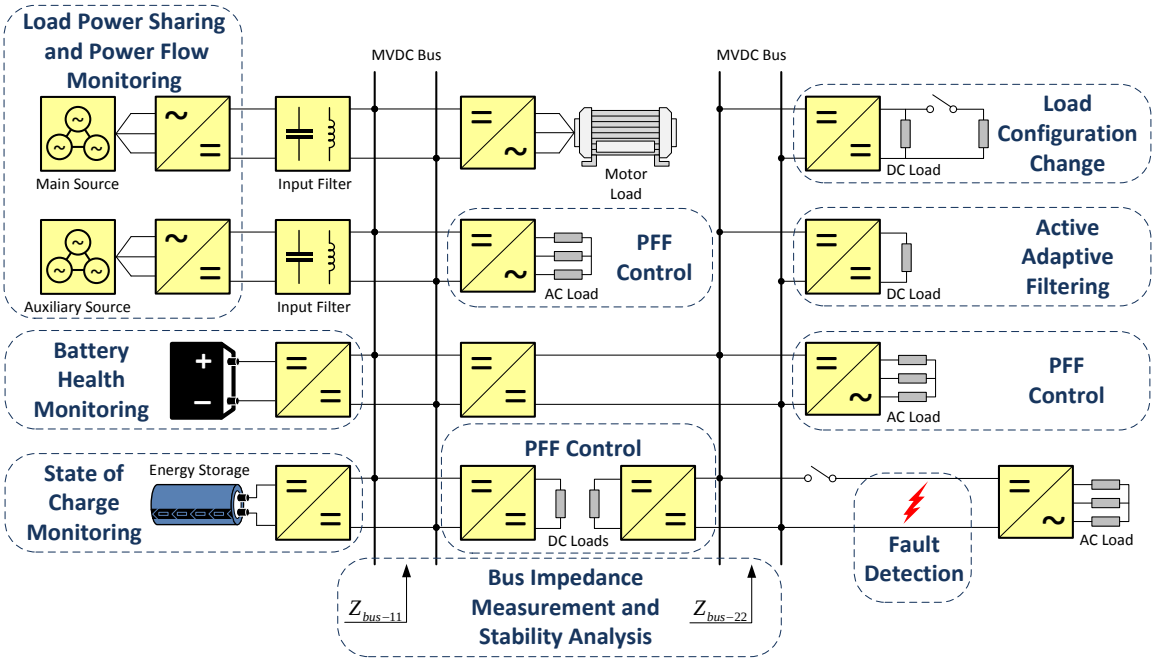


Figure 7.1. Expanded MVDC distribution system test bed.

The expanded test bed includes additional power electronic converters and equipment that are likely to appear on the MVDC distribution system of an electric ship. These items include multiple three-phase power sources, input filters, energy storage in the form of batteries or capacitors, and a three phase drive and electric motor. This test bed will allow for more advanced studies to be performed on the capabilities of the proposed impedance based adaptive control technique.

The presence of additional converters within the system also allows for studies regarding the role of power converters in the overall stability of the system. In the simple MVDC representations investigated thus far, a single load converter has enacted PFF control in order to meet the requirements of the PBSC and stabilize the bus. However, in a decentralized system multiple load converters are connected to the bus and each must be capable of stabilizing the system through the use of PFF control. However, not all load converters should attempt to concurrently enact a PFF control; recall that a converter with

a PFF control incurs a performance tradeoff in the regulation of its own output voltage. Thus, each converter must provide PFF control only when required. An algorithm to assign each converter a role in the overall system stability monitoring scheme is required to ensure a true, decentralized system control.

Demonstration of this algorithm would involve a test scenario as follows. The system in Figure 7.1 is initially operating in steady-state. The system is stable and meets the conditions of the PBSC/AIR as a result of a PFF control of the DC/AC converter present on Bus 1 of the system. No other converter in the system has enacted a PFF control to stabilize the bus. A simulated failure then causes the DC/AC converter to shut down, resulting in the loss of the converter and PFF control and causing a significant change in the system dynamics as a result of the modified bus impedances. According to the system control algorithm, another load converter present in the system will then undergo the adaptive control procedure detailed in Figure 3.7. The system bus impedance is measured, evaluated according to the AIR technique, and passivated using an appropriate PFF controller applied to a different load converter within the system.

Additional system level monitoring capabilities afforded by the wideband impedance identification technique will also be evaluated in the expanded MVDC system including battery health monitoring, state of charge monitoring for energy storage systems, active adaptive filtering, and fault detection.

7.2.3 Experimental Validation of Improved PHIL Interface Algorithm

The stability improvement offered by the application of impedance identification techniques to PHIL simulation has thus far been demonstrated in simulation only. Construction of a PHIL test platform to perform experimental validation of the proposed

techniques is necessary. To ensure a performing system, a high performance real-time computation platform is required. Several options are commercially available and have been used with reasonable success in the literature including systems produced by OPAL-RT, RTDS Technologies, and dSPACE. However, these systems are generally expensive and contain many more features than are necessary for an effective PHIL implementation. The use of an FPGA as a real-time simulation platform will also be evaluated due to the inherent flexibility and high computing performance of the platform.

The PHIL test platform also requires a wide power bandwidth amplifier to serve as the power interface between software simulation and the hardware under test. Impedance based design considerations in the design of a suitable interface amplifier have been demonstrated in simulation. The hardware construction of a high performance, wide bandwidth switching converter is currently being investigated. A new modular switching converter platform has recently been developed around the TI TMS320F28377D digital control platform. This high performance DSP provides additional capabilities for high performance switching converter control not previously available on the control platform used throughout this work. Additional linear power amplifiers and power operational amplifiers are also being investigated for use in a PHIL test platform.

A conceptual block diagram of a proposed PHIL test platform is shown in Figure 7.2. Optimization of the converter control parameters is necessary to achieve a high performance interface amplifier capable of reproducing a variety of PHIL scenarios.

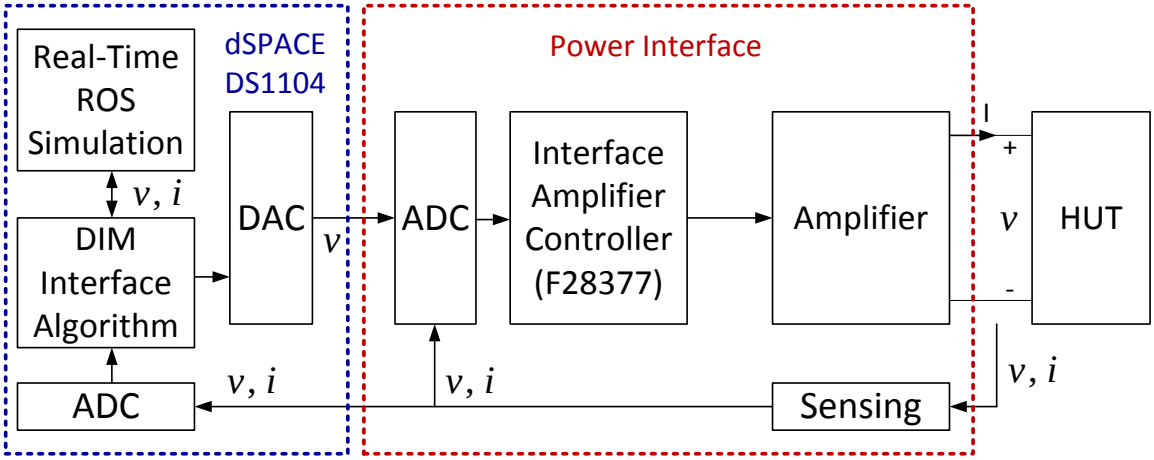


Figure 7.2. Conceptual block diagram of proposed PHIL laboratory test platform.

7.2.4 Expansion of PHIL Test Scenarios

The capabilities of PHIL are to be extended to simulate a more diverse set of source and load electrical subsystems. An example system for PHIL simulation could be based off of that shown in Figure 7.1. In particular, PHIL representations of electrical motors will be investigated. Electrical motors are a nearly ubiquitous load and find a variety of applications in electric and hybrid-electric automobiles, all-electric ships, and grid-connected systems. Electric motors are typically implemented with the capabilities for variable speed and torque control, with power converters acting as front-ends to enforce the desired motor behavior. Thus, the electric motor and drive is a highly dynamic hardware component that presents a unique challenge for PHIL simulation. Electric motors may be employed in applications where the resulting speed-torque characteristic is nonlinear, such as when driving a fan or operating as a propulsion motor driving a hydrodynamic load. The nonlinear characteristic of the motor may result in degraded PHIL performance as a result of difficulties in maintaining interface stability and accuracy. The application of system identification techniques to improve the PHIL

capabilities will be investigated in these types of scenarios. Monitoring of the motor HUT throughout this simulation will allow for IA to be adaptively tuned to ensure good simulation results.

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APPENDIX A

CROSS-CORRELATION BASED SYSTEM IDENTIFICATION TECHNIQUE

A.1 CROSS-CORRELATION METHOD

A switching converter operating in steady-state may be considered a linear time-invariant system to small-signal disturbances [5], described by:

$$y[n] = \sum_{k=0}^{\infty} h[k]u[n-k] + v[n] \tag{A.1}$$

where y[n] is the convolution of the impulse response of the system $h[k]$ and the input $u[n]$ plus noise $v[n]$.

The cross correlation of the input to the output, $R_{uy}[m]$, can be shown as (A.2), where $R_{uu}[m]$ is the auto-correlation of the input signal and $R_{uv}[m]$ is the input-to-disturbance cross-correlation [27].

$$\begin{aligned} R_{uy}[m] &\equiv \sum_{n=0}^{\infty} u[n]y[n+m] \\ &= \sum_{n=0}^{\infty} h[n]R_{uu}[m-n] + R_{uv}[m] \end{aligned} \tag{A.2}$$

Choosing white noise as the input to the system satisfies the following properties:

$$R_{uu}[m] = \delta[m] \quad \text{and} \quad R_{uv}[m] = 0 \tag{A.3}$$

where $\delta[m]$ is defined as the discrete impulse signal. The white noise input is assumed to be uncorrelated to the noise $v[n]$ present in the system, allowing for simplification of (A.2) such that the input-to-output cross correlation is equal to the discrete-time system impulse response [43]. This can be transformed into the system frequency response using a Discrete Fourier Transform (DFT).

$$\begin{aligned} R_{uy}[m] &= h[m] \\ G_{uy}[e^{j\omega}] &= DFT\{h[m]\} \end{aligned} \tag{A.4}$$

As described, the cross-correlation method allows for estimation of system transfer functions from the point of perturbation injection to a measured output [29]-[30]. In pulse width modulated switching converters, the control signal is usually the duty cycle. A pseudo-random binary sequence (PRBS) test signal is added to the duty cycle signal from the feedback controller via a summing block. Applying the cross-correlation technique allows for the identification of quantities internal to the converter, such as control-to-output transfer functions $G_{vd}(s)$ and $G_{id}(s)$, loop gain $T_{loop}(s)$, and of quantities looking outward from the converter, such as source system impedance $Z_{source}(s)$ and load system impedance $Z_{load}(s)$.

A.2 Improvements to Cross-Correlation Method

The properties asserted in (A.3) that allow for the simplifications made in (A.4) assume purely random white noise, which is impossible to create in practice using a finite-length sequence. Several techniques to mitigate the effects of using a non-ideal PRBS test sequence, particularly at high frequencies near the desired closed-loop bandwidth have been proposed [26]-[28].

The first technique delays sampling of the output voltage by half the sequence clock period to offset the phase shift resulting from the Zero-Order-Hold (ZOH) interface. The second method addresses spurious high-frequency content resulting from non-ideal autocorrelation of the perturbation test sequence by employing an improved circular cross-correlation technique that reduces the need to window the measured response and average multi-period injections. Third, test sequences other than white noise may be used to improve accuracy. For example, in systems exhibiting low-pass characteristics, obtaining an accurate estimation at high frequencies can be challenging with finite resolution ADC units. A test sequence with enhanced high frequency content, such as blue noise, may be used to excite the system such that the response is distinguishable from the noise floor. Finally, a correction is made to the estimated control-to-output transfer function by dividing by the non-ideal spectrum of the injected perturbation to improve phase uncertainty and correct for colored noise if used in place of white noise.

APPENDIX B

CONVERTER SYSTEM MODELING

The small-signal model of a four-converter multi-bus MVDC system was developed in Chapter 2. This model consisted of three buck switching converters and a voltage source inverter. The open-loop unterminated g-parameters representing the small-signal behavior of the buck converter were given previously in full detail. The g-parameters of the open-loop VSI are given here. The complete matrix G_{sys} used in the full system model of Chapter 2 and Chapter 3 is also contained in this Appendix.

B.1 OPEN-LOOP UNTERMINATED VSI G-PARAMETERS

The complete linearized, small-signal, open-loop model for a resistively wye-terminated three-phase voltage source inverter using the *dq0* transformation is given in Figure B.1 through Figure B.3. In this work the decoupling technique presented in [22], [44] is utilized, such that the converter is equivalent to two independent buck converters. The resulting small-signal converter transfer functions are given in (B.1)-(B.26).

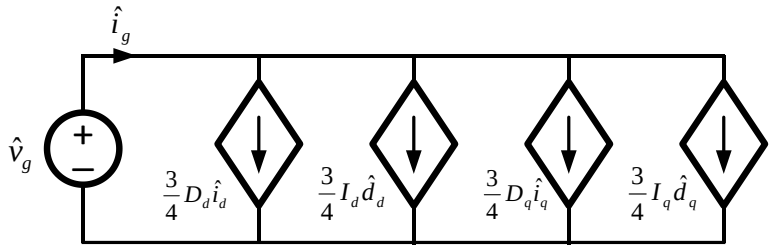

Figure B.1. Small-signal VSI input model.

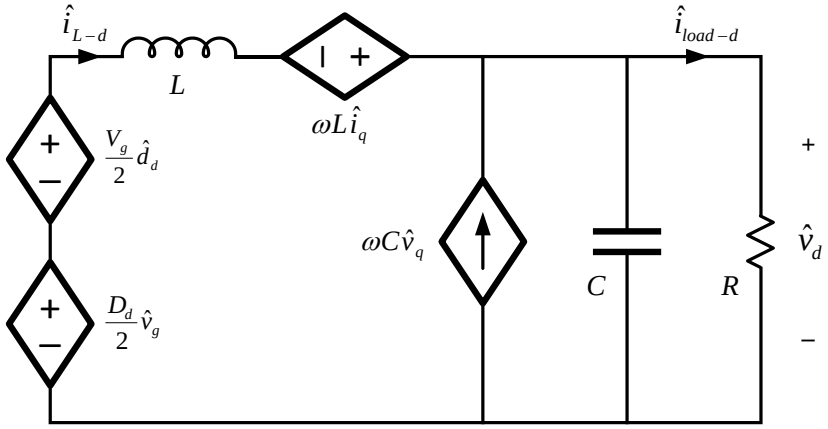

Figure B.2. Small-signal VSI *d*-axis model.

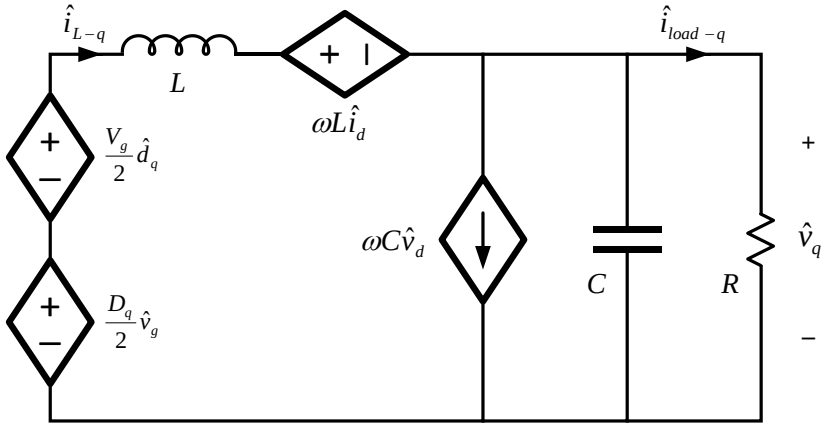

Figure B.3. Small-signal VSI *q*-axis model.

$$\begin{bmatrix} \hat{i}_g \\ \hat{v}_d \\ \hat{v}_q \\ \hat{i}_{L-d} \\ \hat{i}_{L-q} \end{bmatrix} = \begin{bmatrix} Y_{in} & G_{igio-d} & G_{igio-q} & G_{igd-d} & G_{igd-q} \\ G_{vg-d} & -Z_{out-dd} & -Z_{out-dq} & G_{vd-dd} & G_{vd-dq} \\ G_{vg-q} & -Z_{out-qd} & -Z_{out-qq} & G_{vd-qd} & G_{vd-qq} \\ G_{ilg-d} & G_{ilio-dd} & G_{ilio-dq} & G_{ild-dd} & G_{ild-dq} \\ G_{ilg-q} & G_{ilio-qd} & G_{ilio-qq} & G_{ild-qd} & G_{ild-qq} \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load-d} \\ \hat{i}_{load-q} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \tag{B.1}$$

$$Y_{in} = \frac{3D_d^{\,2}}{8R} \frac{sCR+1}{s^2LC + s\frac{L}{R} + 1} \tag{B.2}$$

$$G_{igio-d} = \frac{3D_d}{4} \frac{1}{s^2LC + s\frac{L}{R} + 1} \tag{B.3}$$

$$G_{igio-q} = \frac{3D_q}{4} \frac{1}{s^2 LC + s\frac{L}{R} + 1} \tag{B.4}$$

$$G_{igd-d} = \frac{3}{4} I_d + \frac{3V_g D_d}{8R} \frac{sCR + 1}{s^2 LC + s\frac{L}{R} + 1} \tag{B.5}$$

$$G_{igd-q} = \frac{3}{4} I_q + \frac{3V_g D_q}{8R} \frac{sCR + 1}{s^2 LC + s\frac{L}{R} + 1} \tag{B.6}$$

$$G_{vg-d} = \frac{D_d}{2} \frac{1}{s^2 LC + s\frac{L}{R} + 1} \tag{B.7}$$

$$Z_{out-dd} = \frac{sL}{s^2 LC + s\frac{L}{R} + 1} \tag{B.8}$$

$$Z_{out-dq} = 0 \tag{B.9}$$

$$G_{vd-dd} = \frac{V_g}{2} \frac{1}{s^2 LC + s\frac{L}{R} + 1} \tag{B.10}$$

$$G_{vd-dq} = 0 \tag{B.11}$$

$$G_{vg-q} = \frac{D_q}{2} \frac{1}{s^2 LC + s\frac{L}{R} + 1} \tag{B.12}$$

$$Z_{out-qd} = 0 \tag{B.13}$$

$$Z_{out-qq} = \frac{sL}{s^2 LC + s\frac{L}{R} + 1} \tag{B.14}$$

$$G_{vd-qd} = 0 \tag{B.15}$$

$$G_{vd-qq} = \frac{V_g}{2} \frac{1}{s^2 LC + s\frac{L}{R} + 1} \tag{B.16}$$

$$G_{ilg-d} = \frac{D_d}{2R} \frac{sCR+1}{s^2LC + s\frac{L}{R} + 1} \tag{B.17}$$

$$G_{ilio-dd} = \frac{1}{s^2LC + s\frac{L}{R} + 1} \tag{B.18}$$

$$G_{ilio-dq} = 0 \tag{B.19}$$

$$G_{ild-dd} = \frac{V_g}{2R} \frac{sCR+1}{s^2LC + s\frac{L}{R} + 1} \tag{B.20}$$

$$G_{ild-dq} = 0 \tag{B.21}$$

$$G_{ilg-q} = \frac{D_q}{2R} \frac{sCR+1}{s^2LC + s\frac{L}{R} + 1} \tag{B.22}$$

$$G_{ilio-qd} = 0 \tag{B.23}$$

$$G_{ilio-qq} = \frac{1}{s^2LC + s\frac{L}{R} + 1} \tag{B.24}$$

$$G_{ild-qd} = 0 \tag{B.25}$$

$$G_{ild-qq} = \frac{V_g}{2R} \frac{sCR+1}{s^2LC + s\frac{L}{R} + 1} \tag{B.26}$$

The unterminated VSI g-parameters may be calculated according to (B.27) and are given in (B.28)-(B.52).

$$G_{term} = \lim_{R\to\infty} G_{term} \tag{B.27}$$

$$Y_{in} = \frac{3D_d^{\,2}}{8} \frac{sC}{s^2LC+1} \tag{B.28}$$

$$G_{igio-d} = \frac{3D_d}{4}\frac{1}{s^2LC+1} \tag{B.29}$$

$$G_{igio-q} = \frac{3D_q}{4}\frac{1}{s^2LC+1} \tag{B.30}$$

$$G_{igd-d} = \left(\frac{3}{4}I_{OP-d} + \frac{3V_gD_d}{8}\frac{sC}{s^2LC+1}\right)\Bigg|_{I_{OP-d}=0} \tag{B.31}$$

$$G_{igd-q} = \left(\frac{3}{4}I_{OP-q} + \frac{3V_gD_q}{8}\frac{sC}{s^2LC+1}\right)\Bigg|_{I_{OP-q}=0} \tag{B.32}$$

$$G_{vg-d} = \frac{D_d}{2}\frac{1}{s^2LC+1} \tag{B.33}$$

$$Z_{out-dd} = \frac{sL}{s^2LC+1} \tag{B.34}$$

$$Z_{out-dq} = 0 \tag{B.35}$$

$$G_{vd-dd} = \frac{V_g}{2}\frac{1}{s^2LC+1} \tag{B.36}$$

$$G_{vd-dq} = 0 \tag{B.37}$$

$$G_{vg-q} = \frac{D_q}{2}\frac{1}{s^2LC+1} \tag{B.38}$$

$$Z_{out-qd} = 0 \tag{B.39}$$

$$Z_{out-qq} = \frac{sL}{s^2LC+1} \tag{B.40}$$

$$G_{vd-qd} = 0 \tag{B.41}$$

$$G_{vd-qq} = \frac{V_g}{2}\frac{1}{s^2LC+1} \tag{B.42}$$

$$G_{ilg-d} = \frac{D_d}{2}\frac{sC}{s^2LC+1} \tag{B.43}$$

$$G_{ilio-dd} = \frac{1}{s^2LC+1} \tag{B.44}$$

$$G_{ilio-dq} = 0 \tag{B.45}$$

$$G_{ild-dd} = \frac{V_g}{2}\frac{sC}{s^2LC+1} \tag{B.46}$$

$$G_{ild-dq} = 0 \tag{B.47}$$

$$G_{ilg-q} = \frac{D_q}{2}\frac{sC}{s^2LC+1} \tag{B.48}$$

$$G_{ilio-qd} = 0 \tag{B.49}$$

$$G_{ilio-qq} = \frac{1}{s^2LC+1} \tag{B.50}$$

$$G_{ild-qd} = 0 \tag{B.51}$$

$$G_{ild-qq} = \frac{V_g}{2}\frac{sC}{s^2LC+1} \tag{B.52}$$

B.2 Complete Four-Converter System Model

This section includes the complete four-converter multi-bus system description matrix as constructed in Chapter 2. The large 23-by-12 matrix is subdivided into four parts and finally combined in (B.57).

$$G_{sys-A} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & -Y_{in-BKI} & 1 & 0 & 0 & 0 \\ 0 & -G_{vg-BKI} & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -Y_{in-VSI} & 1 & 0 \\ 0 & 0 & 0 & -G_{vg-VSI} & 0 & 1 \\ 0 & -Y_{in-BKL} & 0 & 0 & 0 & 0 \\ 0 & -G_{vg-BKL} & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_{VSI}} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{B.53}$$

$$G_{sys-B} = \begin{bmatrix} 0 & 0 & -G_{igio-BKS} & 0 & 0 & 0 \\ 0 & 0 & Z_{out-BKS} & 0 & 0 & 0 \\ 0 & 0 & 0 & -G_{igio-BKI} & 0 & 0 \\ 0 & 0 & 0 & Z_{out-BKI} & 0 & 0 \\ 0 & 0 & 0 & 0 & -G_{igio-VSI} & 0 \\ 0 & 0 & 0 & 0 & Z_{out-VSI} & 0 \\ 1 & 0 & 0 & 0 & 0 & -G_{igio-BKL} \\ 0 & 1 & 0 & 0 & 0 & Z_{out-BKL} \\ -1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & -\frac{1}{R_{BKL}} & 0 & 0 & 0 & 1 \end{bmatrix} \quad \text{(B.54)}$$

$$G_{sys-C} = \begin{bmatrix} -Y_{in-BKS} & -G_{igc-BKS} & 0 & 0 & 0 \\ -G_{vg-BKS} & -G_{vc-BKS} & 0 & 0 & 0 \\ 0 & 0 & -G_{igc-BKI} & 0 & 0 \\ 0 & 0 & -G_{vc-BKI} & 0 & 0 \\ 0 & 0 & 0 & -G_{igc-VSI} & Y_{damp-VSI} \\ 0 & 0 & 0 & -G_{vc-VSI} & -G_{vgc-VSI} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad \text{(B.55)}$$

$$G_{sys-D} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -G_{igc-BKL} & Y_{damp-BKL} & 0 & 0 & 0 & 0 \\ -G_{vc-BKL} & -G_{vgc-BKL} & 0 & 0 & 0 & 0 \\ & & 0 & 1 & 0 & 0 & 0 \\ & & 0 & 0 & 1 & 0 & 0 \\ & & 0 & 0 & 0 & 1 & 0 \\ & & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad \text{(B.56)}$$

$$G_{sys} = [G_{sys-A} \quad G_{sys-B} \quad G_{sys-C} \quad G_{sys-D}] \quad \text{(B.57)}$$

APPENDIX C

ADDITIONAL SUBSYSTEM BLOCK DIAGRAMS

C.1 FOUR-CONVERTER MULTI-BUS SYSTEM

This section contains PLECS block diagrams of the additional components used in the four-converter multi-bus system simulation. Representations of the individual system converters and their respective control systems, as well as the PRBS converter, are given in Figures C.1 through C.6.

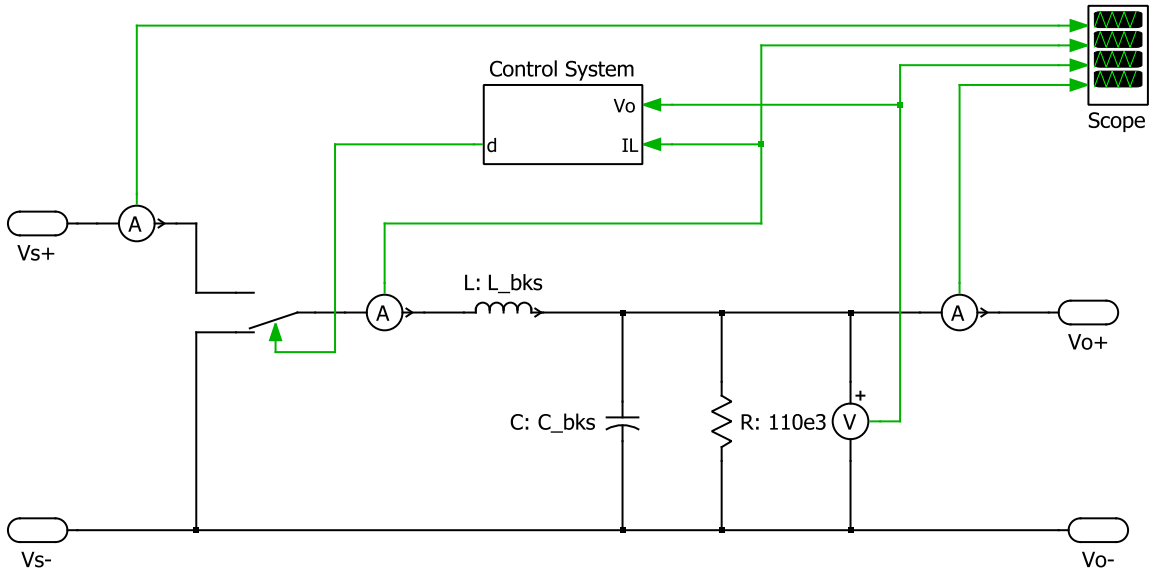

Figure C.1. PLECS diagram of source buck converter (BKS) subsystem (also applies to BKI and BKL converters).

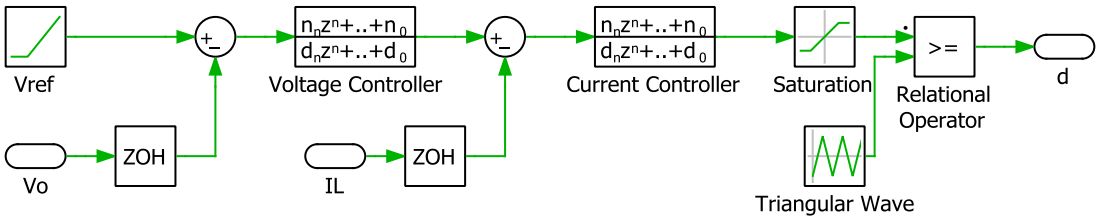

Figure C.2. PLECS diagram of source buck converter (BKS) control subsystem (also applies to BKI and BKL converters).

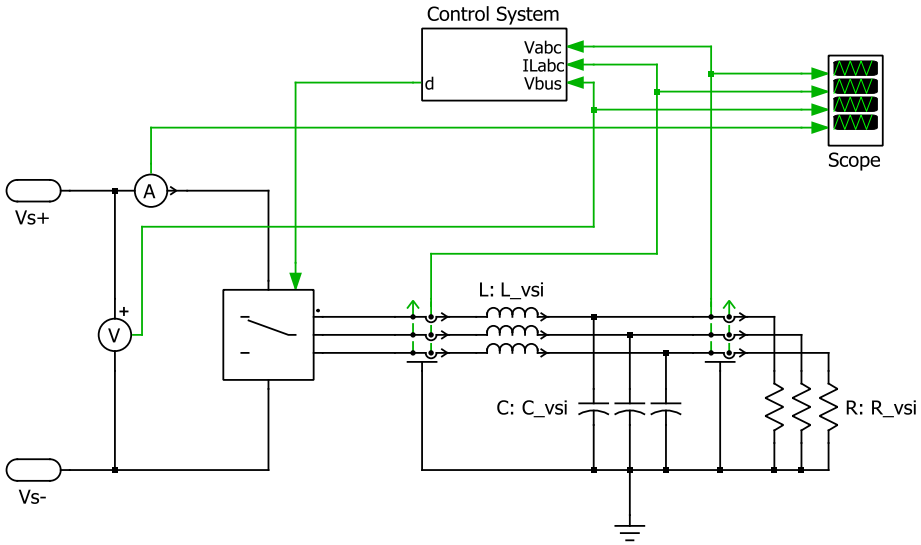

Figure C.3. PLECS diagram of load voltage source inverter (VSI) subsystem.

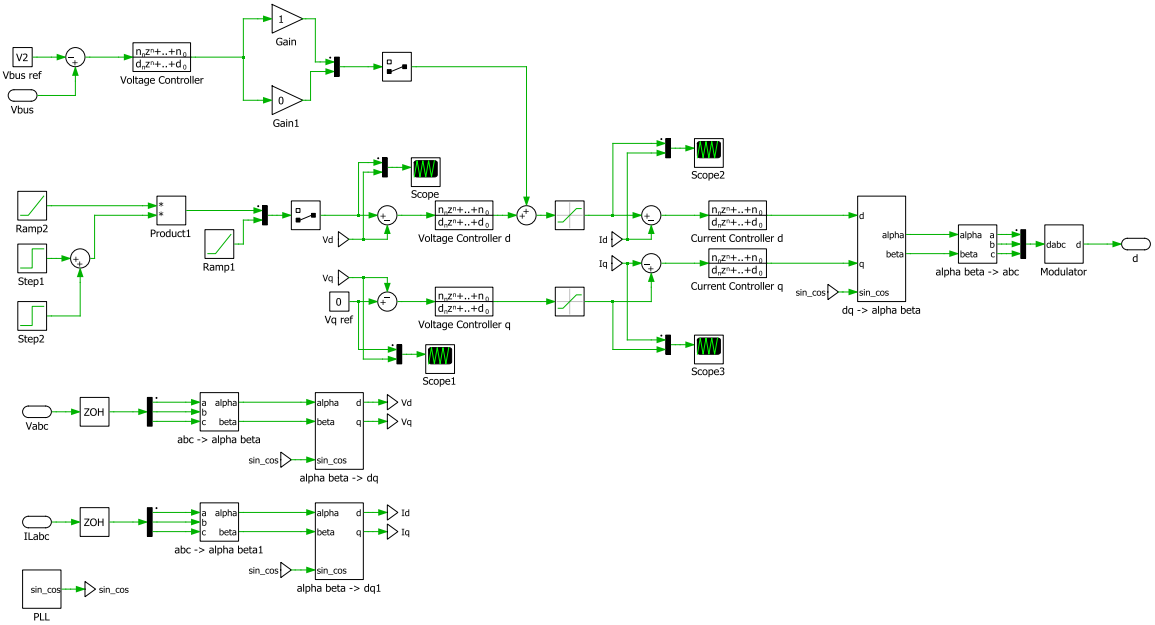

Figure C.4. PLECS diagram of load voltage source inverter (VSI) control subsystem.

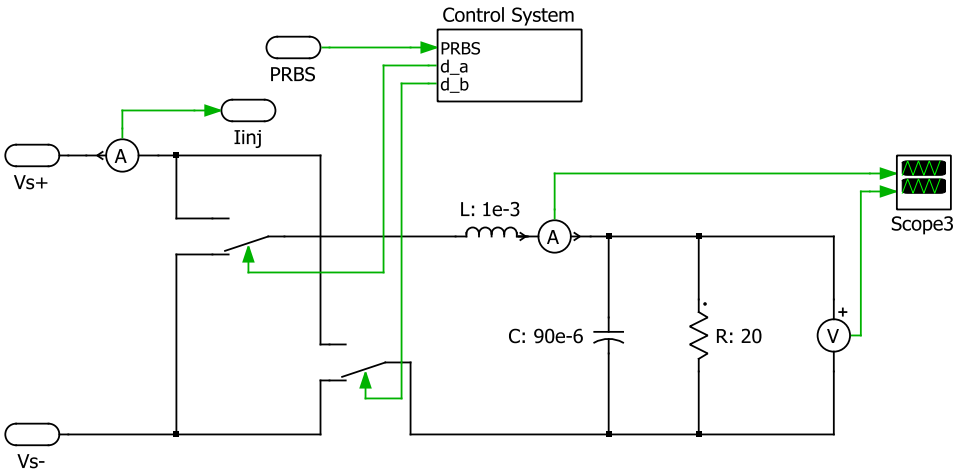

Figure C.5. PLECS diagram of PRBS injection converter subsystem for wideband impedance measurement.

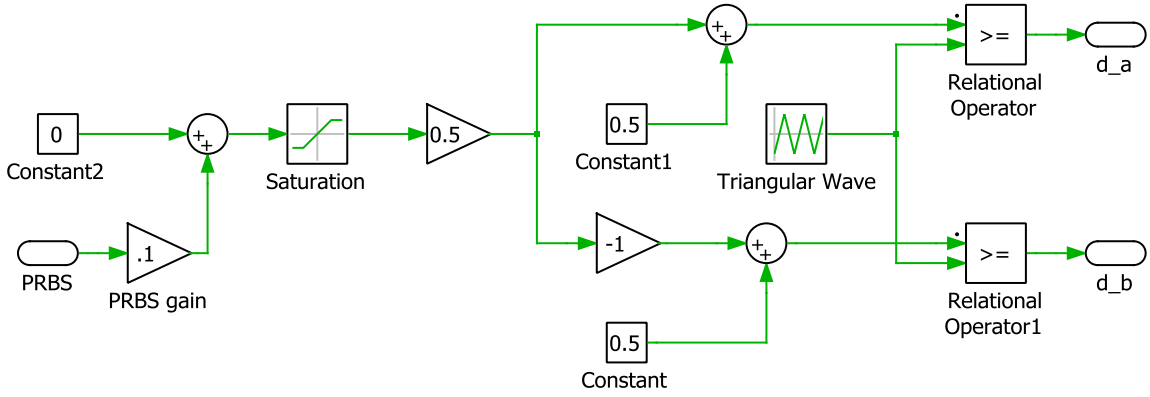

Figure C.6. PLECS diagram of PRBS injection converter control subsystem.

C.2 PHIL INTERFACE AMPLIFIER

This section provides additional Simulink block diagrams of the PHIL interface amplifier and its control system.

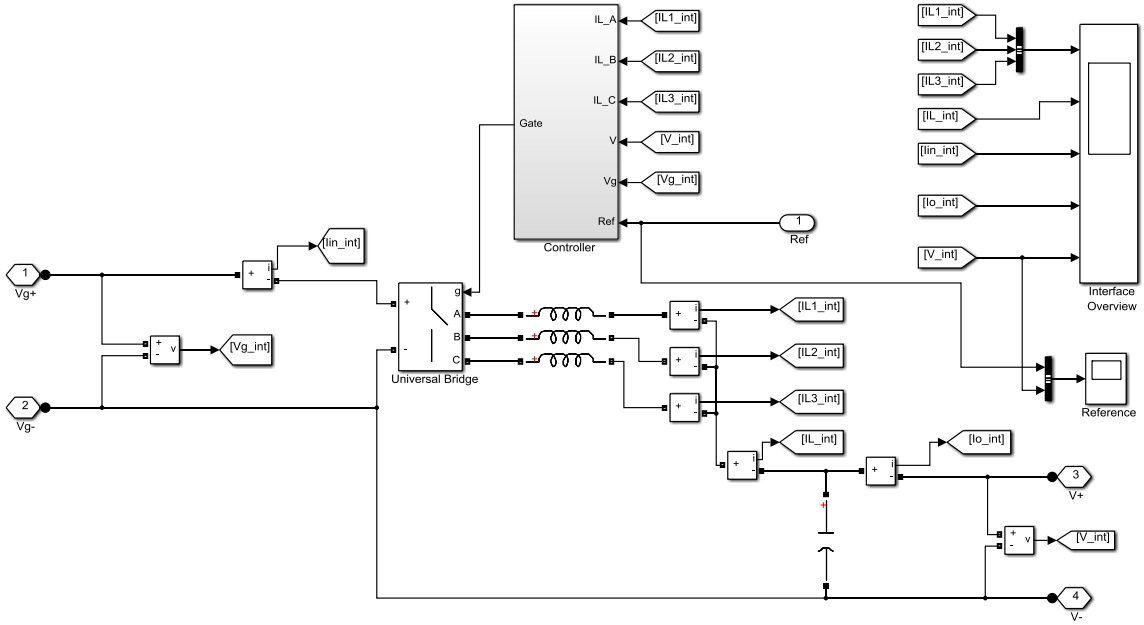

Figure C.7. Simulink diagram of three leg interleaved switching converter interface amplifier.

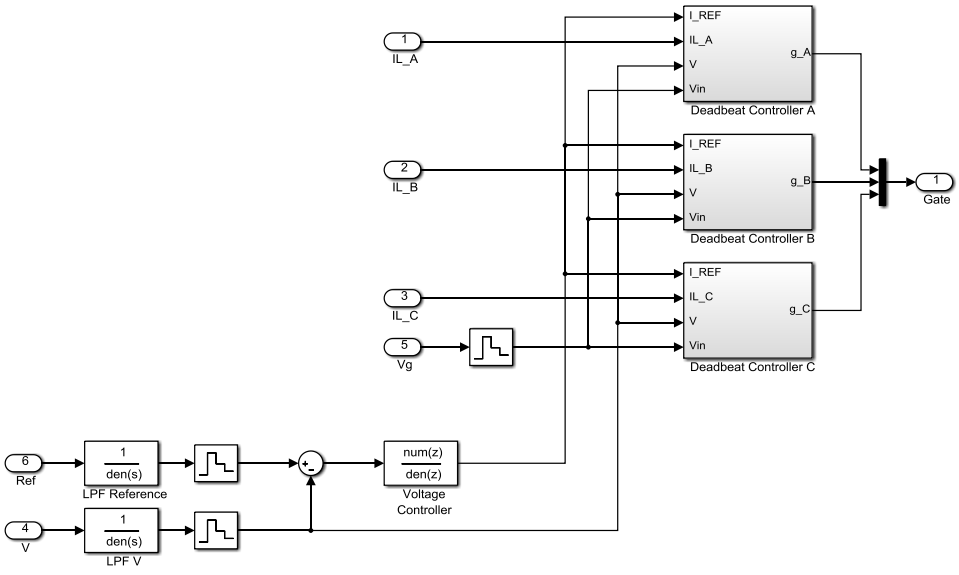

Figure C.8. Simulink diagram of interface amplifier control subsystem.

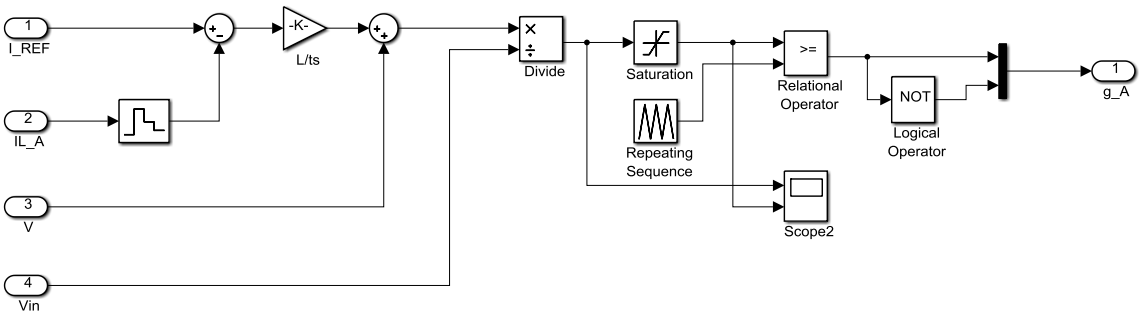

Figure C.9. Simulink diagram of interface amplifier deadbeat inductor current controller for phase leg A.

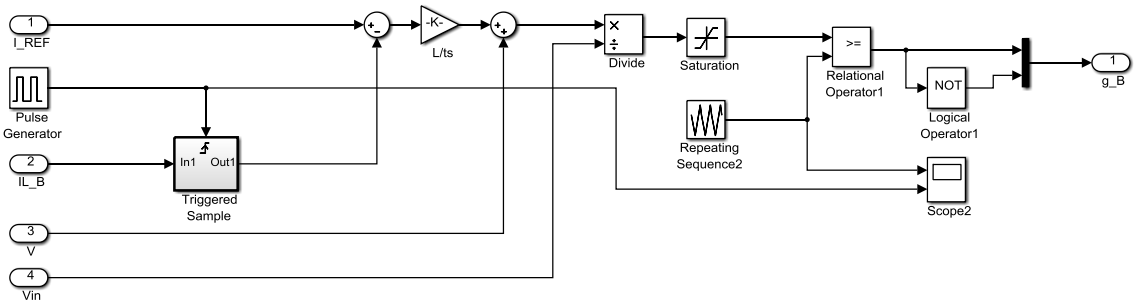

Figure C.10. Simulink diagram of interface amplifier deadbeat inductor current controller for phase leg B showing use of triggered subsystem for synchronization of ZOH inductor current sampling with phase shifted PWM (phase leg C is similar in structure).

C.3 COMPLEX IMPEDANCE IMPLEMENTATION IN SIMULINK

In Chapter 5 it is shown that the stability of the DIM IA can be significantly improved by utilizing wideband system identification techniques to estimate the impedance of the HUT. Following the creation of a parametric impedance model using Least Squares Fitting, a complex ratio of polynomials of order *n* representing the HUT Thévenin impedance is obtained, (C.1).

$$Z(s) = \frac{B(s)}{A(s)} = \frac{B_m s^m + B_{m-1} s^{m-1} + \ldots + B_0}{A_n s^n + A_{n-1} s^{n-1} + \ldots A_0} \tag{C.1}$$

Using this parametric model, the value of the damping impedance Z^* is updated in the DIM IA, resulting in a stability improvement. The Simulink SimPowerSystems block library does not contain a component for modeling a general complex impedance in the form of (C.1), necessitating the following workaround.

For a complex impedance having a proper ($n = m$ in (C.1)) or strictly proper transfer function ($n > m$ in (C.1)), such as the output impedance of a FB controlled switching converter, the following method based on a current controlled voltage source may be used to create a SimPowerSystems compatible impedance element. The current through the element is measured and multiplied by the impedance transfer function. The resulting quantity provides the input for the controlled voltage source (CVS).

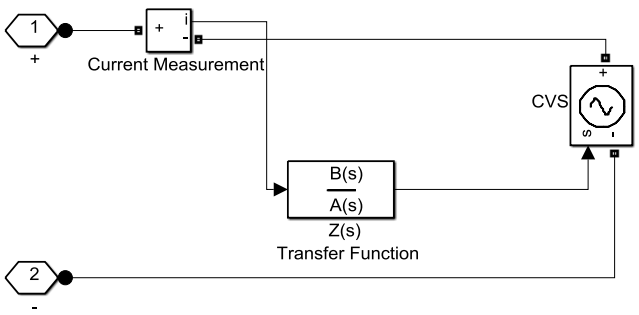

Figure C.11. Simulink diagram of general complex impedance representation based on proper or strictly proper transfer function.

Complex impedances having an improper transfer function ($n < m$ in (C.1)), such as the input impedance of a FB control switching converter, must be inverted before implementation within a Transfer Function block. The following method based on a voltage controlled current source may then be used to represent the impedance. The voltage across the element is measured and multiplied by the inverse of the impedance

transfer function. The resulting quantity provides the input for the controlled current source (CCS).

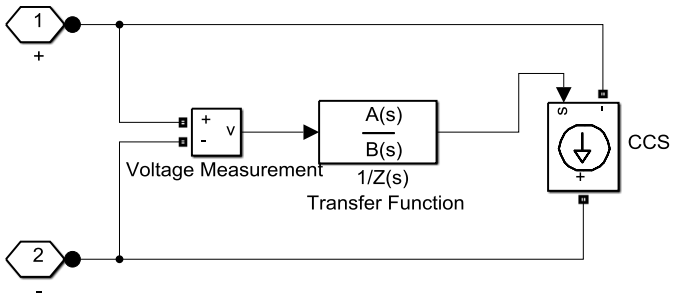

Figure C.12. Simulink diagram of general complex impedance representation based on an improper transfer function.