THERMAL MANAGEMENT OF 3-D STACKED CHIPS USING THERMOELECTRIC AND MICROFLUIDIC DEVICES

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THERMAL MANAGEMENT OF 3-D STACKED CHIPS USING THERMOELECTRIC AND MICROFLUIDIC DEVICES

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My child, listen to what I say, and treasure my commands.

Tune your ears to wisdom, and concentrate on understanding.

Cry out for insight, and ask for understanding.

Search for them as you would for silver; seek them like hidden treasures.

Proverbs 2:1-4

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NOMENCLATURE

Symbols

A	Area
Br	Brinkman Number
c_p	Specific heat
D_h	Hydraulic diameter
Ec	Eckert number
f	Friction factor
G	Gap measurement
h	Convection coefficient
H	Height
I	Electric current
k	Thermal conductivity
L	Microchannel length
l	Thermoelectric material thickness
$\dot{m}$	Mass flow rate
M	Non-dimensional axial wall conduction number
n	Number of experimental measurements
N	Number of thermoelectric elements
Nu	Nusselt number
p	Perimeter
P	Power
Pe	Peclet number
$\dot{Q}$	Volumetric heat generation

q	Heat
q''_{max}	Maximum heat-flux pumping capacity
Re	Reynolds number
r_h	Hydraulic radius
s	Standard deviation of a sample
t	Statistical value found in a t-table
T	Temperature
U	Absolute uncertainty
u	Relative uncertainty
V	Voltage
v	Velocity
W	Width
x	Axial length along microchannel
$x_{fd,h}$	Hydrodynamic entry length
$x_{fd,t}$	Thermal entry length
Z	Dimensional figure-of-merit for a thermoelectric device
α	Seebeck coefficient
η	Fin efficiency
μ	Viscosity
π	Peltier coefficient
ρ	Density
σ	Electrical conductivity

Subscripts

1	Junction 1

2	Junction 2
avg	Average
b	Bottom chip
cc	center to center
c	Cold side of thermoelectric cooler
cs	Cross section
csc	Cross section of the channels
gen	Generated
H	Heater
h	Hot side of thermoelectric cooler
i	Thermoelectric material interface
in	Channel inlet
k	Thermal conductivity
m	Mean
out	Channel outlet
PCB	Printed Circuit Board
t	Top chip
tot	Total
trns	Transported
μ	Viscosity

Abbreviations

3-D	Three dimensional
CFD	Computational fluid dynamics
CMOS	Complementary metal oxide semiconductors
COP	Coefficient of performance

DAQ	Data acquisition system
MEMS	Microelectromechanical systems
PCB	Printed circuit board
RTD	Resistive temperature detector
RTG	Radioisotope thermoelectric generators
TEC	Thermoelectric cooler
TIM	Thermal interface material
ZT	Non-dimensional figure of merit for a device
zT	Non-dimensional figure of merit for a material

CHAPTER 1

INTRODUCTION

As microelectronic device size continues to be reduced, a physical limit to the component size will eventually be reached. Current research efforts focus on new ways to improve the performance of microelectronic devices without reducing component size. One such avenue, three dimensional (3-D) stacked chips, involves stacking several active dies interconnected through silicon vias (TSVs). This novel architecture may reduce microelectronic form factor, improve performance by reducing interconnect delay, and provide a more energy-efficient chip design [1].

However, the electrical and packaging benefits of 3-D stacked chips may be offset by thermal concerns. It is expected that widespread adoption of 3-D technology will bring severe thermal management challenges at the package level [2]. This is not a new issue; thermal concerns were mentioned as early as 1965 by Moore for two dimensional chips [3]. The 2011 International Technology Roadmap for Semiconductors (ITRS) projects that average power dissipation will soon reach levels up to 200 W/cm^2 [4]. In addition, non-uniform power dissipation may cause hotspots with heat fluxes of up to 500 W/cm^2 [5]. An infrared image of two microelectronic chips with hotspots is shown in Figure 1. These hotspots can degrade chip performance and reliability, and can limit chip design [6]. Effective thermal management of chips requires both heat removal of the overall power dissipation to control the package temperature, and heat spreading of non-uniform power dissipation to control excessive rise in localized temperatures [7].

Currently, heat is removed from microelectronic packages using a heat spreader made of a high conductivity material such as copper paired with an air cooled heat sink.

When a smaller form factor is required, such as in laptops, heat pipes can be used as an alternative to heat spreaders. Efforts are underway to develop new methods of cooling for both 2D and 3-D electronics which are energy efficient, reliable, and have a smaller form factor than traditional cooling methods. Examples of these efforts include the use of microchannels, which have a very low form factor and the ability to remove large amounts of heat, and solid state thermoelectric coolers (TECs), which can be turned on and off as necessary for localized cooling. Hybrid cooling systems utilizing both microchannels and TECs also have been investigated.

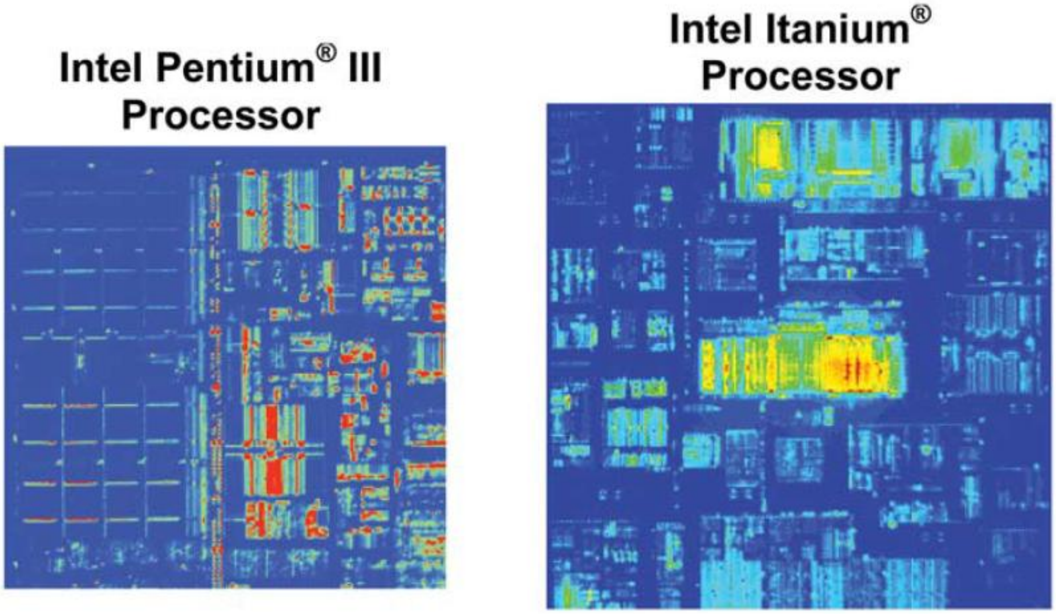

Figure 1: Infra-red images of two microelectronic chips with hotspots due to non-uniform power distributions. Adapted from Reference [7].

This thesis will use computational and experimental methods to explore the use of thermoelectrics and/or microfluidics for cooling stacked chips.

In Chapter 2, a detailed literature review of both microchannels and thermoelectric coolers is presented. Specific focus is given to practical methods of using these devices to cool a chip. System level requirements, fabrication, and performance are discussed as they are important for commercial production of computer chips. Although many researchers have proposed systems which perform well, it is much more difficult to achieve satisfactory performance which meets system constraints and can be fabricated reliably.

In Chapter 3, the computational and experimental methodology used in this thesis is presented. In this chapter, a detailed explanation is given for 3-D thermal model of two stacked dies with four ultrathin (~100µ) TECs. This model is used to investigate the performance of TECs in providing steady state and on demand transient cooling at hot spots in stacked chip architecture. Microchannels are investigated through an experimental study, and the experimental setup and procedure used to measure pressure drop and heat transfer behavior is described in detail. A series of computational models with varying complexity is also developed to compare the experimental results to computational results for microchannel cooling.

In Chapter 4, the steady state performance of the TECs in both active and passive state with varying current magnitudes is first explored and the coupling between TECs is investigated. This study is the first of its kind for TECs in stacked chip packaging. Additionally, the effectiveness of TECs in providing cooling at different hot spot locations on stacked dies during their simultaneous operation is studied. Next, variation of the thermal contact resistances between dies, inside the TEC module, and between the TEC and heat spreader is examined. The transient performance of the TECs under varying current amplitudes and pulse shapes is also explored. Finally, optimum geometry and operating conditions are determined in order to achieve either maximum cooling, or maximum cooling efficiency.

In Chapter 5, the results of hydrodynamic and heat transfer experiments on microchannels are presented and compared to previous empirical results. The experimental results are also compared to theory and the developed computational models for microchannels. Possible sources of error are explored through an experimental uncertainty analysis and a sensitivity study. The sensitivity study yields new insight about the fabrication method used and suggests changes for future experimental studies. Finally, the accuracy and computational expense of an empirical correlation based modeling method for heat transfer in microchannels is compared to existing models which are widely used in literature.

Chapter 6 presents the conclusions of this work and a discussion of possible future work.

CHAPTER 2

LITERATURE REVIEW

In this chapter, a detailed literature review of both thermoelectric coolers and microchannels is presented. The chapter is split into two parts: first thermoelectric materials and devices are discussed, followed by microchannels. Specific focus is given to practical methods of using these devices to cool a chip. System level requirements, fabrication, and performance are discussed as they are important for commercial production of computer chips. Although many researchers have proposed systems which perform well, it is much more difficult to achieve satisfactory performance which meets system constraints and can be fabricated reliably.

2.1 Thermoelectric Cooling for Microelectronics

2.1.1 History, Theory, and Application of Thermoelectricity

The thermoelectric effect was discovered by a variety of individuals over a period of time during the 1800's. Thomas Seebeck first observed the thermoelectric effect when he noticed that a magnetic needle moved when it was placed nearby a closed loop made of two opposing materials in 1823 [8]. The Seebeck coefficient is named in his honor. Jean Peltier later observed that temperature gradients near the junction of two different materials could be induced by passing a current through the material junction. Although this phenomenon is known as the Peltier effect, it was first properly explained by Lenz who used the effect to freeze and melt water using an electric current [8]. The theoretical description of thermoelectricity was completed in 1851 by Thompson when he used thermodynamics to develop a relationship between the Seebeck and Peltier coefficients as well as to predict and observe the existence of a 3^{rd} thermoelectric effect, which we today call the Thompson effect [8].

The Seebeck, Peltier, and Thompson effects can be described in mathematically precise terms. The Seebeck effect states that when two conductors of different materials are connected electrically in series and thermally in parallel with a temperature difference applied to the junctions, a voltage will be generated [9]. This voltage is described by Equation 1 and depicted in Figure 2, where V is voltage, α is the Seebeck coefficient, and T_1 and T_2 are the temperatures of the different junctions.

$$V = \alpha(T_1 - T_2) \tag{1}$$

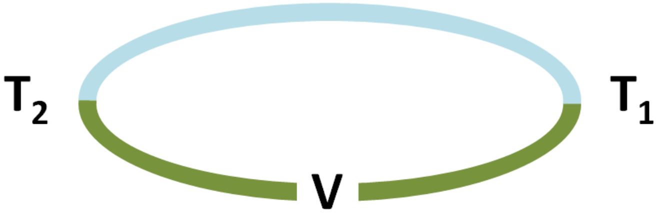

Figure 2: Schematic depicting the Seebeck effect.

The Peltier effect is simply the reverse case of the Seebeck effect. It states that when a voltage is applied across the same circuit (Figure 2), heat will be transported from one junction to the other, depending on the direction of the current, according to Equation 2 [10].

$$q_{trns} = \pi I \tag{2}$$

In this equation, q_{trns} is the heat transported, I is electric current, and π is the Peltier coefficient. The Seebeck and Peltier coefficients are related through the Kelvin relation, $\pi = \alpha T$, leading to Equation 3 for the heat transport due to the Peltier effect [10].

$$q_{trns} = \alpha I T \tag{3}$$

Finally, the Thompson effect states that when a current is passed through a single conductor with a temperature difference, heat is generated in the conductor according to Equation 4 [9].

$$q_{gen} = B I \Delta T \tag{4}$$

In this equation, q_{gen} is heat generated, B is the Thompson coefficient, I is current, and ΔT is the temperature difference across the conductor. The Thompson effect has a minor influence on temperature and voltage distributions compared to the Seebeck and Peltier effects and is often neglected in engineering practice [9].

Thermoelectric are most widely used in applications where a heater, cooler, or generator is needed which is silent, reliable, scalable, and/or has no moving parts [8]. To date, they have been widely used in remote locations for electrical generation or on spacecraft [8]. Spacecraft have successfully relied upon radioisotope thermoelectric generators (RTGs) for missions to most of the planets and solar system exploration; the Mars Science Laboratory rover currently in operation uses an RTG [11]. Thermoelectric generators also have been proposed as a replacement to an alternator on cars by using the waste heat from exhaust to generate electricity [12]. More recently, they have been used in a solar energy harvester achieving 4.6% efficiency using a bulk nano-structured thermoelectric material with a spectrally selective absorber [13]. Small scale thermoelectric coolers have been developed which use nano-engineered superlattice materials for cooling on-chip hotspots [14]. Thermoelectric materials technology continues to advance and there are many prospects for future applications of thermoelectrics.

2.1.2 Thermoelectric Materials

The suitability of a material for use in thermoelectric applications is quantitatively described by its non-dimensional figure of merit, given by Equation 5.

$$zT = \frac{\alpha^2 \sigma T}{k} \tag{5}$$

In this equation, zT is the non-dimensional figure of merit of a material, α is the Seebeck coefficient, T is temperature, and k is the thermal conductivity. The figure of merit for several bulk thermoelectric materials is shown as a function of temperature in Figure 3. A higher figure-of-merit in a thermoelectric material leads to more efficient cooling in thermoelectric coolers (TECs) and more efficient power generation in thermoelectric generators (TEGs) [15].

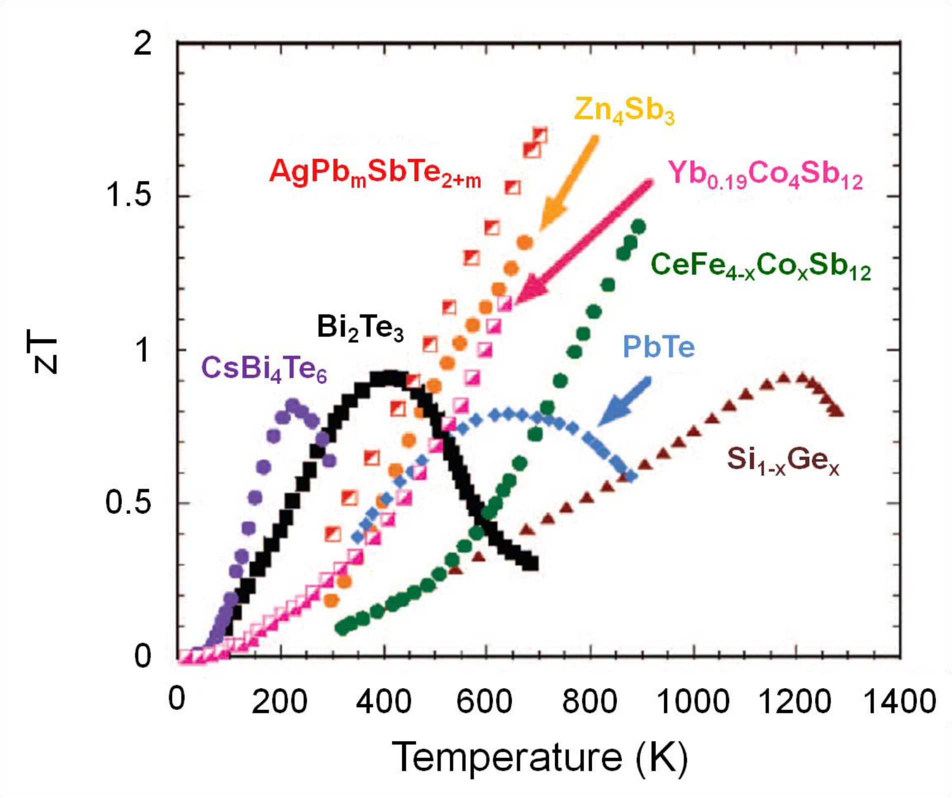

Figure 3: Non-dimensional figure of merit (zT) for several bulk thermoelectric materials as a function of temperature. Adapted from Reference [16].

The strong influence of a material's figure-of-merit on its efficiency in cooling and generation has led to a push to engineer improved thermoelectric materials. This is not a simple task as an improvement in some thermoelectric material properties often causes a decline in other thermoelectric properties. Doping can be used as a tool to improve the thermoelectric properties of a material, but doing so requires careful optimization of a material's figure-of-merit. The ability to optimize a material's figure of merit by varying carrier concentration and the conflicting nature of thermoelectric material properties is illustrated by the material properties of Bi_2Te_3 in Figure 4.

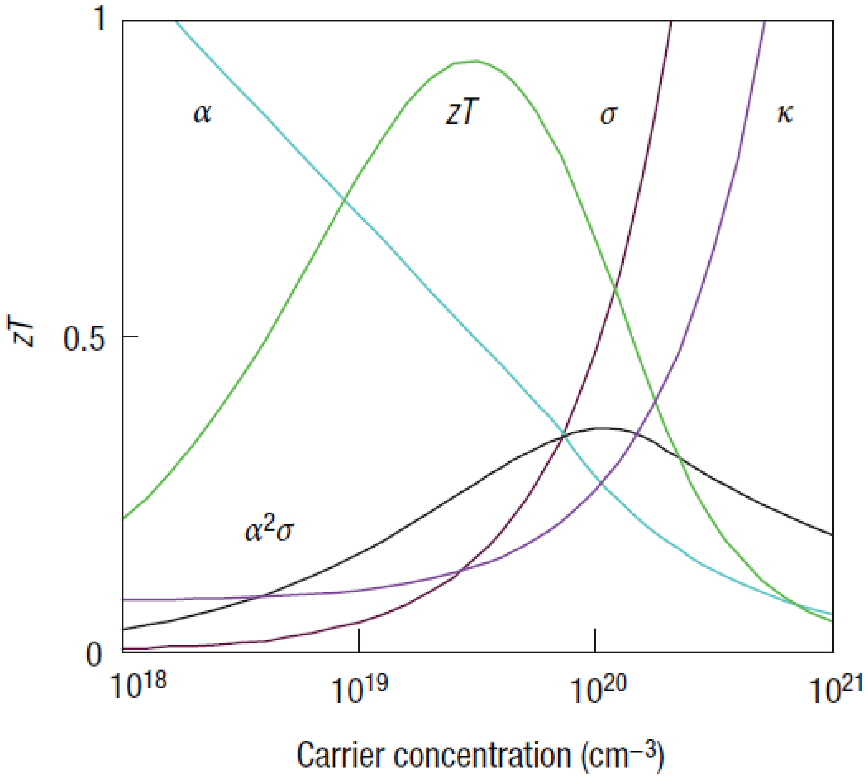

Figure 4: The ability to optimize Bi_2Te_3 figure of merit by varying carrier concentration displays the conflicting nature of thermoelectric material properties. Adapted from Reference [15].

Another strategy which has been used to engineer thermoelectric materials is to reduce the thermal conductivity of the material, but this also causes negative externalities to other thermoelectric properties related with the figure of merit in Equation 5. Thermal transport occurs in two ways: from electronic transport (electrons and holes) or from vibrations (phonons and lattice vibrations) [15]. If the electronic transport is restricted, the electrical conductivity will detrimentally decrease. This means that in order to create a better thermoelectric material by lowering the thermal conductivity, the vibrations in the material structure need to be targeted. Researchers have been successful in targeting these vibrations in skutterudites and clathrate materials [17, 18]. These materials scatter phonons within the unit cell by creating rattling structures or point defects [15]. Superlattices, nanostructured materials, and nanowires, which scatter phonons at their interfaces to reduce their thermal conductivity, also have been successfully fabricated by various research groups [19-21]. In particular, room temperature ZT values as high as 2.4 for p-type superlattices and as high as 1.4 in n-type superlattices have been achieved using MOCVD thin film fabrication [19]. This material was subsequently used to fabricate some of the highest performing thermoelectric devices to date [14].

2.1.3 Thermoelectric Devices

Macro-scale thermoelectric devices have been commercially available for years, and micro-scale thermoelectric devices have recently become a reality. Both macro- and micro-scale devices often contain similar components. A schematic of a thermoelectric device is shown in Figure 5. The device itself is made up of a number of n- and p-type thermoelectric elements, which often come in pairs and are connected in an electrical series with metal interconnects. When a current is applied from an external electrical connection, positive hole charges transport heat in the p-type material and negative electron charges transport heat in the n-type material. This causes heat to be absorbed from one side of the device and transported to the other side of the device.

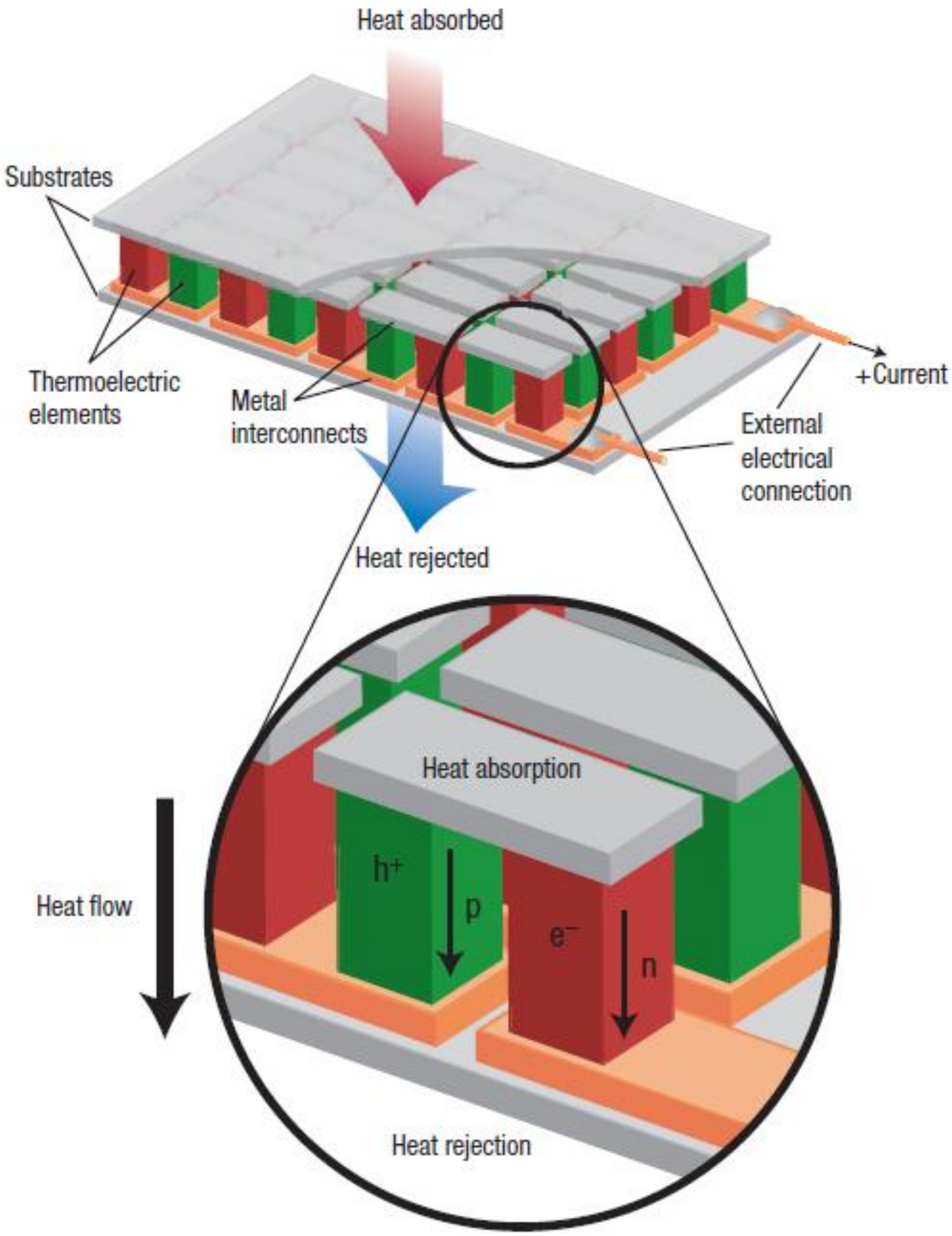

Figure 5: Schematic of a thermoelectric device. Adapted from Reference [15].

Micro-scale TECs have an advantage over macro-scale devices because the heat-flux pumping capacity of a thermoelectric device is inversely proportional to its thickness [14, 22]. This quality is especially important in microelectronics cooling applications, and is part of the reason that macro-scale devices have normally been deemed inappropriate for microelectronics cooling applications [22]. Other advantages of micro scale TECs include a reduction in the volume of raw material, less power consumption, and a smaller form factor than macro-scale TECs [22].

Micro-scale thermoelectric devices are often made using the same manufacturing processes used to make microelectromechanical systems (MEMS). These processes can be used to produce either thermoelectric generators (TEGs) or coolers (TECs) using batch processing techniques like those used in computer chip manufacture [23]. This is advantageous for manufacturing. Several micro-scale TECs which show potential in the application of microelectronics cooling have been fabricated and are summarized in Table 1. Numerous other thermoelectric devices have been fabricated using MEMS processes, but they are either intended for use as TEGs or have geometries which are not suitable for microelectronics cooling [24-33].

The devices listed in Table 1 have been arranged in order of highest to lowest non-dimensional figure-of-merit for a device (ZT). This is the most commonly used measure to compare the performance of thermoelectric devices. It should be noted that this is different than the non-dimensional figure-of-merit for a material (zT) because implementing a thermoelectric material into a device introduces additional inefficiencies. For some cases, the non-dimensional figure-of-merit of the device was not reported and was estimated by either multiplying the reported dimensional figure-of-merit (Z) by

300K, or by the use of Equation 6. It is important to note that this is not the only measure of importance in a micro-scale thermoelectric cooler. Other measures, such as the maximum temperature difference given by Equation 6, or heat-flux pumping capacity given by Equation 7, may be more important in some situations, but these measures either contain or are related to the non-dimensional figure of merit of a TEC [34]

$$\Delta T_{max} = 0.5ZT_c^2 \tag{6}$$

$$q''_{max} = \frac{1}{l}\left((0.5\alpha^2\sigma T_c^2) - \left(k(T_h - T_c)\right)\right) \tag{7}$$

In these equations, ΔT_{max} is the maximum temperature difference between the hot and cold sides of the TEC, Z is the figure-of-merit, T_c is the cold side temperature, q''_{max} is the maximum heat flux pumping capacity, l is the thickness of the thermoelectric material, α is the Seebeck coefficient, σ is the electrical conductivity, k is the thermal conductivity, and T_h is the hot side temperature. It is important to note that although Equation 7 would seem to suggest that an infinitesimal TEC will have infinite pumping power, at very small scales additional factors must be considered. For very small devices thermal bypass, heat losses, and contact resistances (both thermal and electrical) become important [35].

Table 1: Summary of fabricated micro-scale TECs to date

Thermoelectric element manufacturing technique	**Number of thermoelectric elements**	**P-type chemistry**	**N-type chemistry**	**Thermoelectric material thickness (μ)**	**TEC thickness (μ)**	**TEC area (mm^2)**	**Non-dimensional figure-of-merit (ZT) at 300K**
Metal oxide chemical vapor deposition [14]	98	Bi_2Te_3/Sb_2Te_3 *	$Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ *	5-8	100	3.5^2	2
Extrusion technique [22, 36]	100	Alloys of Bi_2Te_3, Sb_2Te_3, and Bi_2Se_3		25	25-50	3.3^2	1
Co-sputtering [37]	6	$(Bi,Sb)_2Te_3$	Bi_2Te_3	10	20	0.7^2 ǂ	0.45-0.9 ǂ
Low pressure chemical vapor deposition [38, 39]	62,500	B-doped poly-Si	P-doped poly-Si	1.5	9 ǂ	10^2	0.037 ǂ
Molecular beam epitaxy [40, 41]	1	$Si_{0.7}Ge_{0.3}/Si$ *§		3	3.5 ǂ	0.03^2 - 1.5^2	0.028 ǂ
Molecular beam epitaxy [42]	1	$Si_{0.89}Ge_{0.1}C_{0.01}/Si$ *§		2	2.1 ǂ	0.04^2 - 0.1^2	0.017 ǂ
Electrochemical deposition [23, 43]	126	Sb_2Te_3	Bi_2Te_3	20	40	1.7^2	0.011
Silicon etching [44]	1	Doped Si §		0.5	3.2 ǂ	0.04^2 - 0.1^2	0.01 ǂ
Electrochemical deposition [38]	200	Sb_2Te_3	Bi_2Te_3	8	15 ǂ	6^2	0.008 ǂ
Electrochemical deposition [45]	100	Sb_2Te_3	Bi_2Te_3	5	7 ǂ	0.5^2 ǂ	0.006 ǂ

* superlattice material
§ only a single material was used and the doping (n- or p-type) is unspecified
ǂ not explicitly reported in the literature, but can be estimated based on details which are reported

Many of the micro-scale TECs fabricated to date have poor figures-of-merit, but a few have exhibited figures-of-merit as high as 2 (Table 1). However, successful fabrication alone does not mean the TEC could be practically used for chip cooling. Integration of TECs into a microelectronics package is just as important as fabrication of TECs. This can be done by either cooling the entire chip, or cooling hotspots selectively using TECs placed in the high power regions of the electronic package.

2.1.4 TECs for Entire Chip Cooling

Using TECs to cool the entire chip can be advantageous for numerous reasons. Using a TEC to reduce the thermal resistance of a system can have many benefits including: reducing fan speed, shrinking the size of the heat sink, and lower the operating temperature of the chip [22, 46, 47]. Reducing the fan speed allows for quieter operation and shrinking the size of the heat sink can improve the form factor of an electronic system. Reducing the temperature of the die may be most important as it can improve chip performance and longevity [47]. Thermoelectric devices are also advantageous because they can be turned on and off on demand. TECs can cool the chip when the cooling load is high, and can generate electricity when the cooling load is low. The generated electricity can even be used to power a fan [48].However, TECs should not be used without caution. Adding a TEC to the electronic package increases the size and cost of the package. More importantly, TECs add thermal resistance to the system when not in use, and in some instances detrimentally affect performance during operation [22]. Ultimately, all the power from the system must be dissipated through the heat sink. Thus, it is important that TECs have a high coefficient of performance (COP) [22]. The COP for a TEC is defined by Equation 8:

$$COP = \frac{q_c}{P_{tot}} \tag{8}$$

where q_c is the amount of heat that enters the cold side of the TEC, and P_{tot} is the total electrical consumption of the thermoelectric device.

There are a variety of configurations which could be used in an electronic package to cool a chip with a TEC. Two of the most common configurations are shown in Figure 6. The TEC is placed between the chip and heat sink in both configurations. However, in Configuration A, the TEC has a smaller area and is placed next to the chip. This configuration has the advantage of requiring a smaller and potentially less expensive TEC. In Configuration B, the TEC has a larger area and is placed in between the heat sink and heat spreader. In this configuration, the TEC contributes less to the net thermal resistance of the system and has lower heat flux pumping requirements [22]. Regardless of which configuration is used, it is imperative to optimize the geometry of the thermoelectric device [22]. The importance of optimization has been demonstrated by previous researchers comparing performance of off-the-shelf components with optimized components [46, 47].

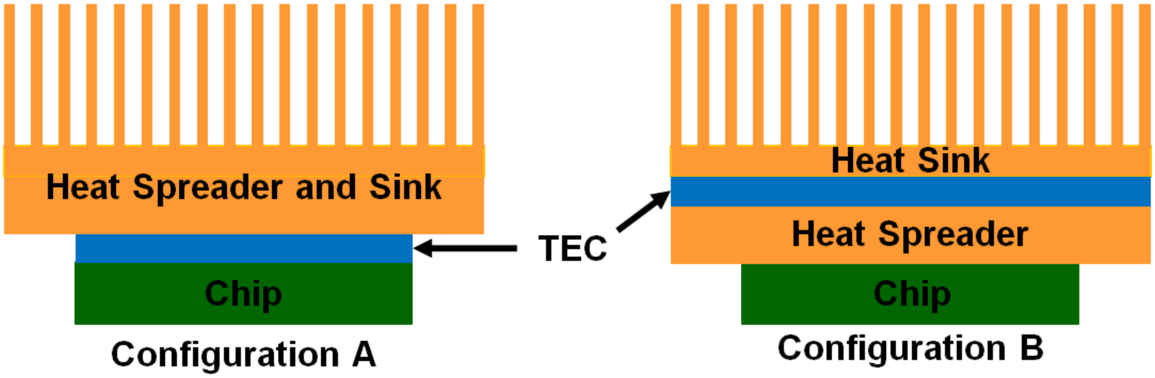

Figure 6: Common configurations used to cool an entire chip with a TEC.

In a typical TEC, the independent variables for an optimization include the thermoelectric material, thermoelectric element thickness, thermoelectric element packing density, and operating current. Although counter-intuitive, the number of thermoelectric elements in a device does not affect its performance and can be used to adjust the operating voltage as desired [49, 50]. Normally, optimizations seek to either maximize COP, or minimize the cold side temperature, however it is possible to simultaneously maximize the COP and minimize the cold side temperature when both the heat load and heat sink thermal resistance are known and constant [51]. Although less common, optimizations also have been performed to minimize the purchase and operational costs of a TEC [52]. The effects of thermal and electrical contact resistances, which become important for micro-scale TECs, also have been accounted for in recent optimization studies [49, 53, 54]. However, it is important to note that all the optimization studies referenced here assume the sides of the thermoelectric cooler are thermally insulated and that the heat flux through the TEC is uniform. While the resulting optimizations are still very useful, these assumptions are not valid when embedded TECs are used for hotspot thermal management and 3-D effects become relevant. A new optimization approach is needed for embedded TECs which considers 3-D effects.

2.1.5 TECs for Hotspot Thermal Management

In modern microelectronics, it is the hotspot temperature which often governs the chip design. Using TECs to control the hotspot temperature is often more practical than entire chip cooling as it is a much more efficient use in terms of both power consumption and cost [22, 55]. By controlling local hotspot temperatures, the total power consumption may be reduced since chip leakage current is temperature dependant [55]. Local control of hotspot temperatures can be accomplished by embedding TECs into the electronic package. This has been accomplished by previous researchers by recessing TECs into the heat spreader [55]. Ideally, these TECs would be micro-scale devices capable of pumping large heat fluxes and would have thin substrates to minimize the additional thermal resistance caused by adding the TEC to the package. However, successful TECs are not constrained to the micro-scale; mini-TECs with thickness of greater than 1 mm also have been successfully demonstrated [22, 56]. No matter the exact geometry of a TEC, thermal expansion effects between the TEC and packaging, electrical and thermal contact resistances, and placement of the TEC inside the package must be considered to ensure that the thermal resistance of the package does not increase with the addition of the thermoelectric device [22, 55]. Despite persisting challenges in TEC fabrication, attachment, compatibility with thermal interface materials (TIM), and power delivery, numerous research groups have demonstrated that hotspot cooling using embedded thermoelectric coolers can become a reality.

Some of the most successful demonstrations of on chip hotspot cooling have been performed using bulk Bi_2Te_3-based macro-scale TEC devices which were carefully placed inside the TEC package. Even though macro-scale TEC devices do not have the same heat pumping capabilities as micro-scale devices, impressive heat pumping capacity was predicted analytically through the use of mini-contacts [57]. Mini-contacts could be achieved by placing a TEC in limited contact with the chip. The TEC pumps the same amount of heat from a reduced area, improving the heat removal near hotspots while allowing the TEC to operate efficiently. The results of the analytical model indicated that the proposed design would reduce the hotspot temperature by approximately 19 °C [57].

This mini-contact design was experimentally demonstrated using commercially available TECs. The commercially available TECs had a total thickness of around 1 mm with a thermoelectric material thickness of either 200 or 130 µm [56, 58]. These TECs were able to cool a hotspot by 7.1 and 8 °C, respectively [56, 58]. Further studies indicated that the thermal resistance was a limiting factor for these experiments and that hotspot cooling on a 500 µm chip could be increased to 13.8 °C if the thermal resistance was lowered [59].

Effective hotspot cooling on chip has also been demonstrated using Silicon (Si) based materials rather than Bi_2Te_3-based materials. Si based materials are appealing because Si is already widely used in the microelectronics industry. Although Si has a *zT* value of only ~0.01, it has a similar power factor as Bi_2Te_3, which means it can pump just as much heat flux as Bi_2Te_3. Analytical studies have been conducted for planar TECs applied to the backside of a Si wafer for hotspot cooling. These TECs would transport heat laterally from the center of the backside of a Si wafer (above the hotspot) to the periphery of that wafer. The doping concentration and size of the cooler were investigated and it was determined that a cooler of a size 5-6 times larger than the wafer thickness would be optimal [60]. Such a cooler would be able to produce 2 °C of cooling at hotspots on 100 µm thick dies, and 3 °C cooling at hotspots on 500 µm thick dies [61]. Analytical studies of planar Si TECs modified to include a micro-scale SiGe TEC as a part of the electronic package have also been investigated [56]. These studies concluded that the addition of the micro-scale TEC cools the backside of the wafer but does not cool the hotspot any more than the in-plane Si cooler alone [58].

Analytical studies also have been performed for SiGe superlattice coolers. These studied determined that a 1 °C temperature drop is achievable on a hotspot with a heat flux of 300 W/cm^2 [62]. In addition, it was concluded that the amount of energy needed to cool the hotspot using the TEC was less than the amount of energy needed to increase the fan speed and maintain the same maximum chip temperature [62]. Furthermore, an identical cooler was experimentally demonstrated to have a response time of 20-40 μs [63]. Such a cooler could have potential for transient cooling of on-chip hotspots, which arise on the order of microseconds.

Perhaps the most impressive demonstration of hotspot cooling to date was performed in collaboration with Intel in 2009 [14]. Superlattices made of p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ were used to fabricate a micro-scale TEC device. These devices were attached to a heat spreader and successfully achieved 7.3 °C of active cooling on 1300W/cm^2 hotspots in addition to the passive cooling caused by a less thermal interface material (TIM) in the package [14]. The study concluded that despite the performance achieved, electrical and thermal contact resistances within the TEC and at the interface of the TEC and heat spreader greatly reduced the performance of the device [14]. This study did not consider that transient operation of the TECs which may improve hotspot cooling compared to the steady state operation.

2.1.6 Pulsed Thermoelectricity

The transient operation of thermoelectric coolers was first reported by Stilbans and Fedorovich and has been studied theoretically as for the past 50 years [64-67]. Experimental work also has been performed which verified that the use of current pulses can cool thermoelectric elements below their minimum steady state temperature [68-70]. When a current pulse is applied to a TEC, the cold side of the TEC experiences the Peltier effect immediately while the Joule heating occurring within the TEC takes a longer time to propagate to the surface. This causes a temporary supercooling effect, shown in Figure 7, which is followed by an overshoot in temperature once the cooling load is removed.

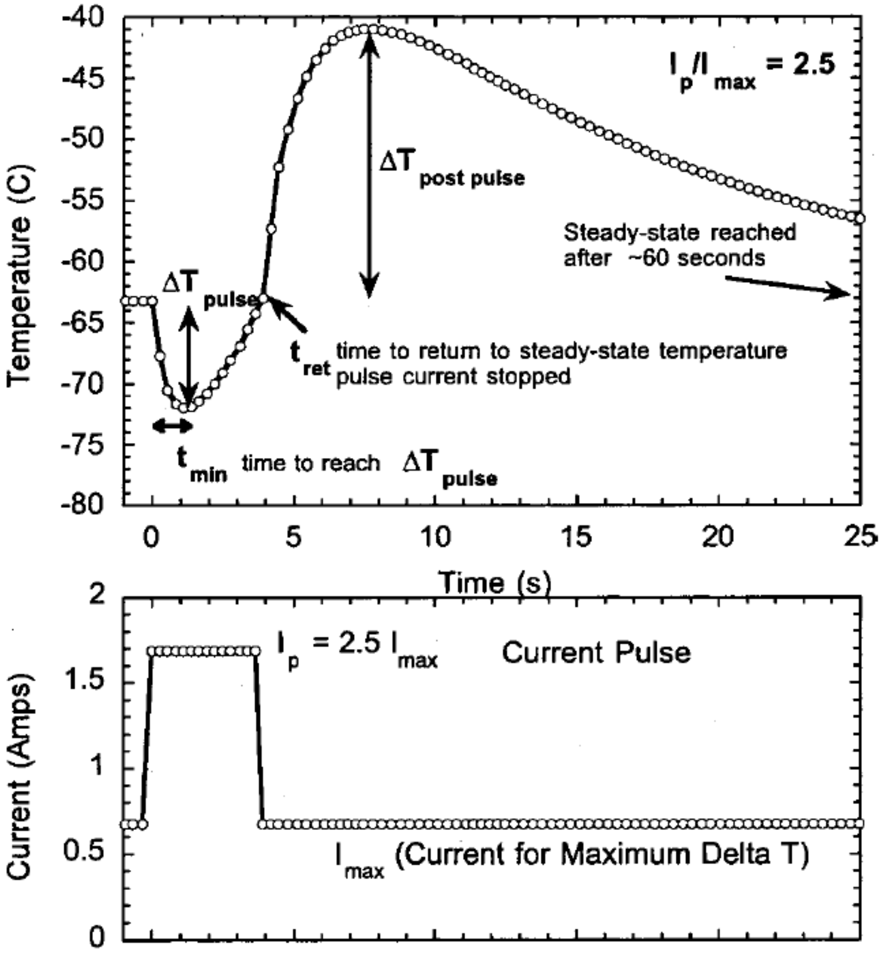

Figure 7: Illustration of current pulse cooling which is greater than what can be achieved with steady state cooling. After the current pulse is applied, a temperature overshoot ensues. Adapted from Reference [68].

This supercooling effect provided by transient TEC operation can eliminate the need for multistage coolers in applications where the duration of cooling is short [68]. A current magnitude of approximately three times the optimum current magnitude for steady state cooling has been reported as the near optimum for transient current pulse cooling [68].

Experimental research has been conducted to improve the amount of cooling which can be obtained through the use of a current pulse. Although it is possible to utilize a current pulse to cool an object starting from an applied current of 0 A, most current pulses are applied once the cold side of the TEC has already reached its minimum temperature [68]. This ensures that the maximum cooling possible is obtained with the current pulse. Other techniques which have been used to improve the degree of cooling include the use of variable cross section thermoelectric elements, shaped current pulses, and optimally graded electrical conductivity profiles [65, 71, 72]. The use of shaped current pulses is especially promising because the shape of the current pulse can be optimized to increase the cooling effect and reduce the temperature overshoot.

The use of current pulses for microelectronics cooling has also been investigated analytically [73, 74]. These studies were based on the previously discussed experimental work demonstrating the use of micro-scale TECs for steady state hotspot cooling. The first study demonstrated that a single TEC operating on chip was capable of obtaining an additional 6-7 °C hotspot cooling over steady state cooling with the use of a transient pulse [73]. It also expounded on the detrimental effects of thermal and electrical contact resistance on TEC performance in steady state and transient operation. The second study was performed for an array of TECs and also concluded that the transient cooling of TECs could obtain additional cooing over steady state, but was only efficient for short duration, and infrequent hotspots [74]. It noted that the use of current pulses with specific shapes improves energy efficiency and reduce the temperature overshoot while sacrificing only small amounts of cooling performance.

Supercooling using current pulses becomes even more effective when micro-scale thermoelectric devices are used. At the micro-scale, extremely fast response times are obtainable [19, 63]. These fast responses times and micro-scale TECs are essential for on-demand, localized cooling of hotspots.

2.1.7 TECs in Stacked Chips

Although the use of TECs for thermal management in both steady state and transient operation has been widely studied, very little attention has been given to the application of these coolers for thermal management of stacked chip architecture. One study envisioned the used of thermoelectric heat spreading using lateral Peltier devices in stacked chips [75]. In another study, a TEC is combined with a silicon interposer to cool hotspots on chip [76]. This study concluded that at low power dissipations the TEC can improve the cooling in a stacked chip, but at high power dissipation levels it would be better to use a copper spreader without a TEC to cool the package. Despite these studies, a detailed investigation of the application of TECs in a 3-D stacked chip package for hotspot thermal management has not yet been performed.

Exact configuration of 3-D stacked chips and bonding technology is still an area of active research. The commercial applications of 3-D technology are currently confined to imaging sensors and DRAMs. Even so, it is expected that there will be sufficient space to mount micro-scale TECs on the different dies of a 3-D package. There are numerous die bonding techniques available for 3-D stacking, including oxide, adhesive, copper, and solder bonding [77]. All these bonding techniques leave a gap between the top and bottom dies ranging from 2 to 70 µm [78]. This is in the same range as state of the art micro-scale thermoelectric (TE) devices, which have been fabricated at total device thicknesses of 100 µm or less using both superlattices and bulk materials (Table 1). However, the TE material thickness of these devices, and others, ranges from only 5 – 20 µm (Table 1). If TECs were fabricated directly on-chip using MEMS processes, the thickness would be closer to the thickness of the TE material which is about only 20 µm or less. For this reason, it is believed that a computational analysis of TEC cooling in a 3-D package is a useful tool to determine what role, if any, micro-scale TECs might play in the hotspot cooling of stacked chips.

2.1.8 Hybrid Cooling Schemes

Although TECs are normally proposed for use with air cooled heat sinks, it is possible that they could also be used in conjunction with water cooled heat sinks. If a TEC were paired with a microchannel heat sink, it could reduce the total thermal resistance of the package or allow for a reduction of the necessary pumping power for that heat sink. Thermoelectric devices could also be used in conjunction with water cooled heat sinks to generate power for the pump.

TECs have been paired with microchannel heat sinks for microelectronics cooling purposes in a variety of ways. The simplest, but least efficient, way would be to cool the entire chip using a TEC sandwiched in between the chip and a microchannel heat sink. A similar system has been built and demonstrated in [79]. Such a system in practice would be used to cool the entire chip and not focus solely on hotspots. Other methods have been demonstrated which use TECs to cool hotspots, and microchannels to cool the background heat flux, which utilize either a single phase or a two-phase implementation

[80]. In the single phase implementation, TECs are placed directly on the hotspots, providing localized cooling. In two-phase implementation, microstructures provide enhanced heat transfer at the hotspots and TECs are used to internally condense the resulting vapors.

Hybrid cooling schemes have the ability to combine the best aspects of both microchannels and TECs. Microchannels can remove high heat fluxes in a small space compared to air cooled heat sinks while TECs provide on-demand, localized cooling of hotspots. To our knowledge, TECs and microchannels have not yet been studied for hybrid and localized cooling of stacked chips.

2.2 Microchannel Cooling for Microelectronics

2.2.1 History, Theory, and Application of Microchannels

Ever since the first demonstration of microchannel cooling, significant research has gone into developing fluid cooling systems for microelectronics. Microchannel cooling was first demonstrated by Tuckerman and Pease in 1981 when they used microchannels to remove up to 790 W/cm^2 heat flux from a silicon substrate [81]. Shortly thereafter, the transition from bi-polar junction transistors to complementary metal oxide semiconductor (CMOS) transistors greatly reduced the cooling load placed on microelectronics systems, eliminating the need for microchannels [82]. In time, however, even CMOS transistors began to generate too much heat and microchannels were again explored as a method for high heat flux removal.

The main advantage of microchannel cooling over traditional air cooling technology is its ability to remove very high heat fluxes from a package. Equation 9 explains the theoretical basis for why microchannel cooling is capable of such high rates of heat removal. Assuming that the Nusselt number for fully developed flow remains approximately constant, reducing the diameter of a pipe to the micron-scale will result in an extremely high convection coefficient, according to Equation 9 [83].

$$Nu = \frac{hD}{k_f} \tag{9}$$

In this Equation, Nu is the Nusselt number, h is the convection coefficient, D is the pipe diameter, and k_f is the thermal conductivity of the working fluid.

Microchannels could be used in many applications. To date, microchannels have been used to cool supercomputers and the Apple G5 desktop [82]. However, they have also have been used in military applications and space systems where large heat flux removal is required to keep components near room temperature [84]. More imaginative applications of microchannels include fuel cells, biomedical devices, and milk pasteurization processes [82, 85].

2.2.2 System Level Requirements for Microchannel Cooling

The heat removal rate using microchannels is limited only by the amount of fluid which can be supplied to them [86]. However, one major challenge is the high pumping pressure needed to pump sufficient fluid through small channels. [87, 88]. Pumps must be capable of providing both enough pressure to force fluid through microchannels and enough flow to remove the necessary heat from the electronic package. Pumping power is often used to express both of these requirements as one because it is equal to the pumping pressure times flow rate. Macro-scale pumps can meet these requirements, but take up an enormous amount of space. Micro-scale pumps have been demonstrated which can provide adequate flow rates, but not all of them produce sufficient pumping power for microchannel integration [88, 89]. Pump reliability is also critical. It is for this reason that pumps which use electric fields to pump fluids and have no moving parts, such as EHD and electroosmotic pumps, tend to be attractive [86, 90]. Even though these technologies are promising, commercial systems remain expensive and unreliable [86]. In order for microchannels to become commercially feasible, pumps and microchannels need to be integrated into the system and possibly even fabricated on chip. Some researchers have looked at ways in which the pumping requirements could be reduced to decrease the burden on pumps.

Several ideas have been explored to find a way to reduce the pressure drop requirements for microchannel cooling. Lowering the flow rate reduces both the pressure drop and pumping power, however this severely limits the amount of heat that can be removed from the package. Increasing the size of the microchannels can also reduce pumping pressure and power requirements but inhibits the convective heat transfer at the channel walls according to the previously discussed Equation 9. Optimization of the pumping power has indicated that using multi-level microchannel heat sinks could reduce pumping requirements, although it has not been shown experimentally and could be difficult to manufacture [91]. Fractal-like branching networks have also been suggested to reduce pressure drop [92, 93]. Another strategy which has been proposed to reduce pumping requirements is the use of liquid phase change [86]. The latent heat of evaporation is greater than the change in enthalpy from room temperature to just below boiling point for many liquids. Thus, two phase flow would remove the same amount of heat as single phase flow while using a smaller flow rate. Some researchers have indicated that the pumping power requirements actually can be higher for two phase flow than single phase flow due to the acceleration of fluid as it changes from liquid to gas [94]. Furthermore, two phase flow can result in flow instabilities and varying pressure drops and heat transfer rates along a passage [94]. Although two phase flow has great potential to remove even higher heat fluxes than single phase flow in microchannels, it also has the greatest challenges.

Although much of the literature on microchannels is devoted to the analysis of microchannels for cooling uniform power dissipation, when a microelectronic chip has highly non-uniform power dissipation, the temperature of the hot spot will often drive the thermal cooling solution. As a result, recent optimizations have been undertaken which take the non-uniform power dissipation of modern chips into account [95]. The inefficiency of uniformly cooling a chip with hotspots has also been demonstrated experimentally [96]. Some strategies which have been developed to preferentially cool hotspots include the use of jet impingement, a MEMS device called a perspiration nanopatch, and a cooling scheme with uses two fluids loops: one too cool hotspots and another to cool the background heat [90, 97, 98].

As industry transitions from 2D planar chips to 3-D stacked chips, microchannels are being considered for cooling in this new technology. Recent analytical studies have been performed on the use of microchannels and micro pin-fin structures for cooling 3-D stacked chips with hotspots [99]. In 3-D technology, packaging and fabrication constraints become even more important than in planar chips and are possibly the most important factors when choosing a cooling technology for 3-D stacked chips [100]. Many previous studies have failed to address these requirements. However, one study demonstrated the integration of micro pin-fin heat sinks with through silicon vias (TSVs) positioned on the pin-fin axis [101]. This geometry would be ideal for a 3-D electronic package. This study considered both thermal requirements along with electrical requirements including signal latency and power consumption. Another study reported a novel fabrication technique for the integration and interconnection of microchannels onto 2D or 3-D chips, with a focus on thermal and packaging requirements [102]. It is clear that any cooling solution needs to take into account not only thermal requirements, but must consider other competing system requirements.

2.2.3 Microchannel Fabrication

Fabrication of microchannels has traditionally been performed using photolithography. In this process, a mask is made using a photoresist. Then, wet etching or reactive ion etching is used to etch away channels from a substrate, which is normally made of silicon. Alternatively, micro-machining can be used if the substrate is made of metal. Finally, a cover plate is bonded to the substrate, forming channels. Bonding can be performed using anodic bonding or polymers. There are multiple variations of these processes [81, 90, 96, 103-105]. One problem with these techniques is that the cover plate must be attached serially. Microchannel manufacture with MEMS processing shows more promise because of its compatibility with MEMS processing for microelectronics.

A monolithic CMOS compatible fabrication technique has been recently demonstrated by my collaborators at Middle East Technical University (METU) and the process flow for manufacturing a single microchannel using this technique is shown in Figure 8 [106]. A titanium/gold seed layer is first deposited onto the substrate. Next, a thick photoresist layer is spun and exposed. A copper electroplating process is used to grow the channel walls, and a 20 μm thick parylene coating is then applied. Finally, the channels are released in an acetone bath, producing channels with a gold base, copper side walls, and a parylene seal. The microchannels fabricated using this method are the subject of the experimental and numerical analysis of microchannels in this thesis.

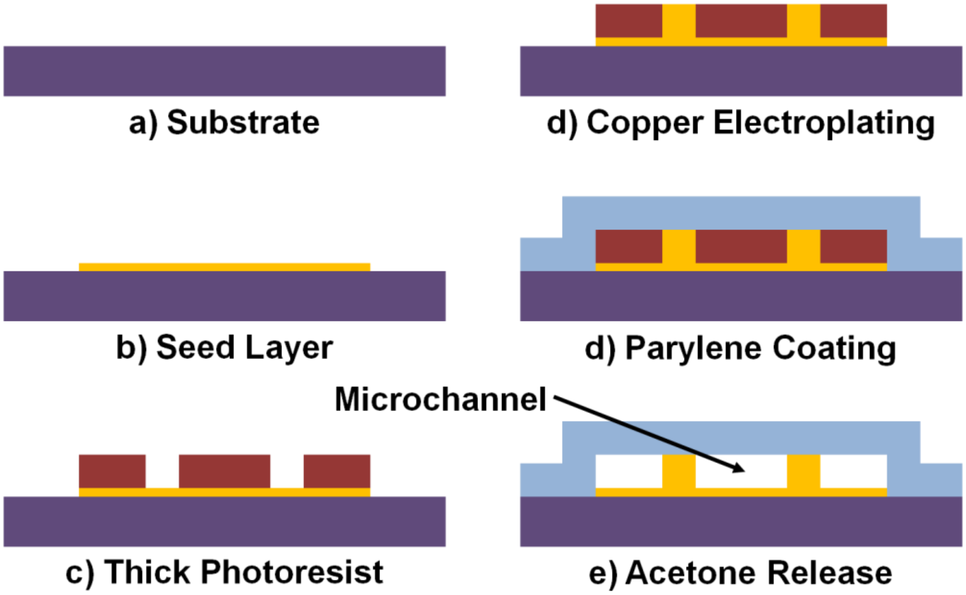

Figure 8: Process flow for manufacturing a single microchannel using a CMOS compatible electroplating method.

2.2.4 Fluid Flow and Heat Transfer in Microchannels

The fluid flow and heat transfer analysis in the microchannels has been the subject of intense research for the past three decades, and continues to be a topic of interest. A significant number of researchers have reported friction factors less than or larger than the theoretically predicted friction factor for laminar flow [107]. Additionally, the Nusselt number of microchannels has been reported to be above or below those found in macro-scale pipes [107]. The goal of this section is to describe how previous experiments indicate that the fluid flow and heat transfer in microchannels typically adhere to conventional theory and to review some of the possible mechanisms which are known or suspected to influence microchannel heat transfer.

The discrepancy between the various experimental results for pressure drop has been addressed and explained in multiple review papers. Discrepancies in the measured friction factor were largely attributed to the experimental uncertainty in the determination of channel diameter [108]. When the uncertainty in diameter measurement was taken into account for channels with a diameter of between 15 and 150 μm, the experimental deviations fell within the range of uncertainty of the experimental setup [108]. A different review paper also concluded that incorrectly assessing the boundary condition of the experiment had led to the unexpected results [113]. It was determined that when experimental conditions were consistent to the theoretical ones for microchannels of greater than 50 μm diameter, the results matched hydrodynamic theory [109]. Other studies indicate that good agreement between experiment and theory for both heat transfer and fluid flow can be found for microchannels with a hydraulic diameter of 250 μm or greater and attributed much of the discrepancies in the literature to mismatched entrance and boundary conditions or difficulties with the instrumentation [86]. Still others have attributed the discrepancies to poor fabrication and have suggested that the newer literature is more reliable because improved fabrication techniques have led to a reduction in surface roughness and improved precision in channel dimensions [107].

For Nusselt number measurements, the boundary conditions for microchannel walls are especially important, and often fall somewhere in the middle of three boundary conditions[110]. In the first boundary condition, the wall temperature is constant in both the axial and circumferential directions. In the second, the wall temperature is constant in the circumferential direction, but the heat flux is constant in the axial direction. In the third, the heat flux can be constant in both the axial and circumferential directions. All sides do not have to have the same boundary condition. Microchannels are often constrained to have three heated sides due to the use of a cover plate during fabrication. The reality is that all practical situations, especially for microchannels, fall somewhere in the middle of these three stated boundary conditions [110].

There is no doubt that heat transfer and pressure drop experiments with microchannels are very difficult to conduct. Although many studies found in literature claim their results contradict conventional theory, some carefully constructed experiments have shown remarkable agreement with conventional theory. Two carefully designed experiments have investigated scaling effects in parallel plate flow. Both experiments used a single setup with an adjustable gap between parallel plates in order to keep the surface conditions constant for various gap sizes. One paper varied the gap between 100 and 1000 μm, and observed a decrease in the Nusselt number for gap sizes of less than 400 μm [111]. The other varied the gap between 50 and 500 μm and found that conventional correlations for heat transfer were applicable to microchannels [112]. Both studies reported that the transition from laminar to turbulent flow followed conventional theory.

When the experimental and theoretical results for Nusselt number are compared, it is still difficult for a carefully designed experiment to verify that the theory matches experiment, or to develop a new, appropriate theory. Many of the initial “new micro-scale effects” reported in literature turned out to be simple scaling effects which are always present, but do not play an important role in macro-scale fluid flow and heat transfer.

These effects include the surface roughness, viscous dissipation, and axial heat conduction [113, 114].

Many researchers have used roughness to explain their unconventional results. They argue that roughness becomes very important at the micro-scale because the relative roughness can be much larger than in conventionally sized channels. However, the effect of roughness is not highly influential on Nusselt number, even though it can affect the friction factor in microchannels. This fact has been proved using numerical studies. Two dimensional computational fluid dynamics (CFD) studies were performed on planar and circular microchannels to determine the effect of roughness on pressure drop and Nusselt number [115]. Both rectangular and triangular roughness peaks were used, with a relative roughness of between 0 and 5.3 % for the channels. It was found that the roughness caused an increase in pressure drop for all the geometries [115]. However, the effect of roughness on Nusselt number was tempered because the heat transfer coefficient increased at roughness peaks, but decreased in the roughness valleys. In fact, the roughness increased the Nusselt number in the circular microchannel, yet decreased the Nusselt number in the rectangular channel. Although the influence of roughness was overestimated due to the two-dimensional modeling, the influence of roughness on the channels was within the experimental uncertainty of most experiments [115]. A follow up three-dimensional CFD simulation also was performed for a flat plate only and confirmed the results of the two-dimensional simulations [116].

Another scaling effect observed in microchannel experiments arises because the channels have a very large length to hydraulic diameter ratio. This means the fluid properties can change significantly along the length of the channel. In addition, viscous dissipation can become important for such channels. Viscous dissipation has been shown to become relevant when Equation 10 is satisfied [117, 118].

$$\frac{Ec}{Re}(fReL/D_h) \geq 1 \tag{10}$$

In this equation, Ec is the Eckert number, f is the friction factor, Re is the Reynolds number, L is the length of the microchannel, and D_h is the hydraulic diameter of the microchannel.

The Brinkman number has been proposed as a non-dimensional number which could be used in correlations for microchannel heat transfer because viscous heating can be more important in microchannels than in conventional ones [119, 120]. This number is the ratio of heat produced by viscous dissipation and heat transported by conduction and is defined by Equation 11.

$$Br = \frac{\mu v_{avg}^2}{k\Delta T} \tag{11}$$

In this equation, Br is the Brinkman number, μ is the fluid viscosity, v_avg is the average fluid velocity, k is the thermal conductivity of the fluid, and ΔT is the temperature difference between the mean fluid temperature and wall temperature. The Brinkman number can be shown to appear in the energy balance from a dimensional analysis of a microchannel, even though it is usually very small [119]. It has also been suggested that the Brinkman number may capture the effects of the increase in velocity due to a change in fluid properties [120]. However, other researchers have warned that using the Brinkman number in an empirical correlation is physically unrealistic when the viscous dissipation in a microchannel flow is small [114].

Although surface roughness and viscous dissipation can sometimes be neglected in microchannel heat transfer, axial heat conduction is an effect that can almost never be neglected. In conventional channels, the walls are very thin relative to the channel cross section, but in microchannels, this relation is often reversed. As a result, conjugate heat transfer is exceedingly important. Many researchers have shown that assuming axial heat conduction is negligible can lead to an incorrect calculation of Nusselt number [113, 114, 121]. As in conventional channels, axial heat conduction in the microchannel fluid can be eliminated if the Peclet number is sufficiently large. Even if the Peclet number is sufficiently large, axial conduction in the fluid should be taken into account in the entrance length when Equation 12 is satisfied [114].

$$\frac{xPe}{r_h} \leq 20 \tag{12}$$

In this equation, x is the axial distance along the microchannel, Pe is the Peclet number, and r_h is the hydraulic radius of the microchannel. Axial heat conduction in the channel walls needs to be taken into account for most microchannel experimental setups. The non-dimensional axial conduction number, M, describes the ratio between conductive heat flux parallel to the channel and convective heat flux into the channel and is given by Equation 13 [122].

$$M = \frac{kA_{cs}\frac{dT}{dx}}{\rho c_p v_{avg} A_{csc}(T_{out} - T_{in})} \tag{13}$$

In this equation, M is the non-dimensional axial conduction number, k is the thermal conductivity of the substrate, A_cs is the channel wall cross sectional area, $\frac{dT}{dx}$ is the axial channel wall temperature gradient, ρ is the fluid density, c_p is the specific heat of the fluid, v_{avg} is the average fluid velocity, A_csc is the channel cross sectional area, T_{out} is the fluid outlet temperature, and T_{in} is the fluid inlet temperature. Axial conduction along the channel walls can be neglected when $M < 0.01$ [122].

The various scaling effects present in microchannel heat transfer and the challenges associated with the measurement of microchannel heat transfer lead to a set of recommendations for future experiments, adapted from [114] :

1. Viscous heating is normally negligible but should be checked
2. Axial heat conduction can be significant in microchannels
3. Measurement of inlet and outlet fluid temperature is not sufficient information for determining the heat transfer coefficient.
4. Heat losses need to be taken into account
5. The heat transfer coefficient should be calculated numerically in addition to the experimental calculations
6. Thermal entry lengths need to be considered both theoretically and numerically

Ultimately, the Nusselt number in fully developed laminar flow is expected to be constant as predicted by conventional theory [110]. Even so, numerous experiments have been performed where the Nusselt number is reported to vary with Reynolds number in fully developed, laminar flow [110]. It should also be noted that there are still various phenomena which are still under investigation which may influence the fluid flow and heat transfer in microchannels [123]. These include the effects of hydrophobic or hydrophilic microchannel walls, the effect of charged particles, also known as the electric double layer (EDL) on microchannel fluid flow and heat transfer, and the presence of micro or nano-scale bubbles at channel walls [123].

2.2.5 Empirical Correlations for Rectangular Microchannels

The focus of this thesis is primarily measuring the heat transfer and fluid flow in rectangular microchannels fabricated using a method previously described [106]. In this section, the previously reported empirical correlations for rectangular microchannels with hydraulic diameters ranging from 50 to 200 μm are reviewed.

To date, there have been only four heat transfer experiments performed on rectangular microchannels with hydraulic diameters under 200 μm. These experiments and the methods used to obtain experimental data are summarized in Table 2.

Table 2: Summary of experiments performed on rectangular microchannels with a hydraulic diameter of less than 200 µm.

Author	**D_h (um)**	**Re**	**Aspect Ratio**	**Channel Length (mm)**
Peng and Peterson, 1996 [105]	133 – 367	50 - 4000	0.333 – 1	45
Jeung and Kwak, 2008 [104]	100 – 133	55 - 330	0.5 – 1	15
Park and Punch, 2008 [103]	106 – 307	69 – 800	0.2 – 0.94	10
Koyuncuoglu, *et al.*, 2012 [106]	67, 80	25 – 160	0.25 – 0.5	10

Peng and Peterson constructed an array of microchannels by micromachining a stainless steel plate and applying an insulating cover plate [105]. This geometric configuration produced a constant heat flux boundary for the three walls of the channel when the stainless steel plate was uniformly heated by an electric voltage applied across the entire plate. Thermocouples at the inlet and outlet sumps were used to measure the water temperature, and six thermocouples on the back of the stainless steel plate measured the wall temperature and ensured that the flow rate was equally distributed between the channels. In order to calculate the convection coefficient, Equation 14 was used.

$$h = \frac{\dot{Q}}{A \Delta T_{lm}} \tag{14}$$

In this equation, the heat generation, $\dot{Q}$, was modified using an energy balance to represent the losses in the system, the area, A, was the area of the steel plate rather than the area of the three non-insulated channel walls, and the log mean temperature difference, ΔT_{lm}, was calculated based on the temperature difference between the channel walls and water at the inlet and the outlet of the channel, shown in Equation 15:

$$\Delta T_{lm} = \frac{\Delta T_{in} - \Delta T_{out}}{\ln\left(\frac{\Delta T_{in}}{\Delta T_{out}}\right)} \tag{15}$$

The Nusselt number in the laminar regime was correlated to Equation 16:

$$Nu = 0.1165 \left(\frac{D_h}{W_{cc}}\right)^{0.81} \left(\frac{H}{W}\right)^{-0.79} Re_{Dh}{}^{0.62} Pr^{\left(\frac{1}{3}\right)} \tag{16}$$

In this equation, D_h is the hydraulic diameter of the channel, W_{cc} is the channel center to center width, H is the channel height, and W is the channel width. It is important to note that the Reynolds number is calculated using inlet properties in this empirical relationship. The authors did not report at what temperature the Prandtl number was calculated, but it was probably evaluated at the mean fluid temperature. The correlation reported by these authors suggests a strong correlation between the Nusselt number and the channel aspect ratio and hydraulic diameter, however a second analysis of their data suggest that this is actually not the case [124].

Jeung and Kwak etched 100 μm deep microchannels on a silicon wafer and bonded a glass cover plate to the wafer, insulating the top channel wall [104]. They reportedly used a localized heater to produce a one dimensional temperature profile which varied only in the axial channel direction. Two thermocouples were used to measure the inlet and outlet fluid temperatures and seven poly-silicon resistors were used to measure wall temperatures along the axial channel direction. Flow rate was reported to be non-equally partitioned, so the average Reynolds number was used in the representation of the results. Equation 17 was used to calculate the convection coefficient.

$$h = \frac{\dot{Q}}{A\,\Delta T_{lm}} \tag{17}$$

In this equation, $\dot{Q}$ is the heat generation minus losses and is calculated using the inlet and outlet fluid temperatures, the area, A, is equal to the wall area for the three non-insulated walls, and the log mean temperature difference, ΔT_{lm}, is calculated using Equation 18:

$$\Delta T_{lm} = \frac{\left((T_w - T_{in}) - (T_w - T_{out})\right)}{\ln\left(\frac{T_w - T_{in}}{T_w - T_{out}}\right)} \tag{18}$$

In this equation, T_w is the channel wall temperature, T_{in} is the inlet fluid temperature, and T_{out} is the outlet fluid temperature. The Nusselt number in the laminar regime was correlated by Equation 19:

$$Nu = 0.00058\, Re_{Dh}^{1.15} \mathrm{Pr}^{\frac{1}{3}} \left(\frac{\mu(T)}{\mu(T_{in})}\right)^{2.76} \left(\frac{W}{H}\right)^{0.3} \tag{19}$$

In this equation, W is the channel width, H is the channel height, $\mu(T)$ the viscosity at mean fluid temperature, and $\mu(T_{in})$ is the fluid temperature at the inlet. Although the paper does not directly state at what temperature the Reynolds or Prandtl number should be calculated, a personal correspondence verified that they were evaluated at the mean fluid temperature [125].

Park and Punch etched microchannels of various dimensions on a silicon wafer and bonded a Pyrex cover plate to the wafer, insulating the top channel wall [103]. They uniformly heated the backside of the wafer using a thin film heater. Because the channel walls were thin, the temperature and heat flux profile on the three non-insulated walls were not uniform, but non-uniformity was accounted for by integrating the fin equation. In their experiments, thermocouples were used to measure the inlet and outlet fluid temperatures, and an infrared imaging camera was used to detect the backside heater temperature. Special manifolds were designed to ensure a uniform flow distribution in the microchannels. Equation 20 was used to calculate the convection coefficient:

$$h = \frac{\dot{Q}}{A\,(\mathrm{T_w} - \mathrm{T_m})} \tag{20}$$

In this equation, A represents the fin area of the microchannels, and T_w is the silicon wall temperature wetted by water, found by integrating the solution to the fin equation, and T_m is the mean water temperature. The explicit value used for $\dot{Q}$ is not reported, however the actual supplied power was compared to the energy carried away by the water. The Nusselt number was correlated to the Reynolds, Prandtl, and Brinkman numbers, even though viscous dissipation was negligible. The resulting correlation is shown in Equation 21:

$$Nu = 0.015\,Re^{0.62}Pr^{0.33}Br^{-0.22} \tag{21}$$

The variation in the mean water properties was reported, so it is thought that all non-dimensional numbers and fluid properties were evaluated at the mean water temperature.

Koyuncuoglu, *et al.* developed a novel MEMS technique to produce microchannels with a height of 50 μm on a glass slide with copper side walls and parylene as a cover layer [106]. The area under the microchannels and side walls is uniformly heated using five thin film resistors covered with a thin parylene layer for electrical insulation, justifying a 3 sided uniform heat flux assumption. Thermocouples were used to measure the inlet and outlet fluid temperatures and the five thin film heaters serve the dual purpose of RTDs to measure channel wall temperature. The effects of unequal flow in different channels were considered by experimenting with both single and multichannel devices. Equation 22 was used to calculate the local convection coefficient between the 2nd and 4th heaters in the channel:

$$h = \frac{\dot{Q}}{A(T_w - T_m)} \tag{22}$$

In this equation, $\dot{Q}$ is calculated based on the temperature rise of the water between the 2nd and 4th heaters, A is the area of the three non-insulated channel walls and T_{w} is the average wall temperature between the 2nd and 4th heaters. T_{m}, the mean water temperature between the 2nd and 4th heaters, is estimated using an extrapolation technique where the mean fluid temperature is assumed to increase from the inlet at the same rate as the heater temperature increases in the fully developed region of the channel. A correlation between the Nusselt, Reynolds, and Prandtl number was developed and reported as Equation 23:

$$Nu = 0.032\, Re^{0.804} Pr^{0.03} \tag{23}$$

All fluid properties were evaluated at the mean fluid temperature. They also reported a correlation for Nusselt number including the ratio of height to width, however only two aspect ratios were tested and the influence of height to width on Nusselt number was very weak.

It is important to note that the empirical correlations reviewed in this section differ from those used in conventional pipes and channels. They are not expected to be more reliable than conventional correlations, since the reviewed experiments did not always use best practices for measuring microchannel heat transfer and are rather limited in scope. However, they are included here primarily for comparison against the experimental results found in this work.

CHAPTER 3

COMPUTATIONAL AND EXPERIMENTAL METHODOLOGY

In this chapter, the computational methodology for TEC modeling is first discussed. This includes a detailed description of the model geometry, material properties, and modeling technique used to represent the thermoelectric phenomenon. Second, the experimental and computational methods used for experiments and simulations of microchannels are discussed. Third, the experimental setup, procedure, and data analysis are detailed. Finally, an empirical correlation based modeling method for the computational analysis is introduced. This modeling method is compared to resistor network and CFD models in Chapter 5.

3.1 Computational Methodology for TECs

3.1.1 Geometric and Material Parameters

In order to analyze the effect of TECs on hotspot temperature reduction in a stacked die, a computational model of four TECs integrated into a stacked chip electronic package was developed. A schematic of the electronic package, TECs, and hotspot locations are shown in Figure 9. A bottom chip is mounted on a substrate and a top chip is attached to the bottom chip. The bonding method of the chips is left unspecified because bonding in 3-D stacked chips has been proposed using many different methods [77, 78]. For generality, the bond is represented by a thin effective resistance layer (ERL) and an infill layer (Figure 9). The thermal conductivity of the effective resistance layer can be varied so the effect of different bonding techniques on the thermal performance of an electronic package with integrated TECs can be investigated. The infill is presumed to be a compliant polymer, similar to modern underfill or TIM, which enhances both mechanical stability and thermal performance of the electronic package. Four TECs, each 100 µm thick and composed of 7x7 p-n couples, are paired with two hotspots on the bottom and two hotspots on the top chip. The top TECs are attached to the heat spreader while the bottom TECs are attached to the ERL. The computational domain includes the heat spreader, chips, TIM, ERL, infill, hotspots, and TECs (Figure 9).

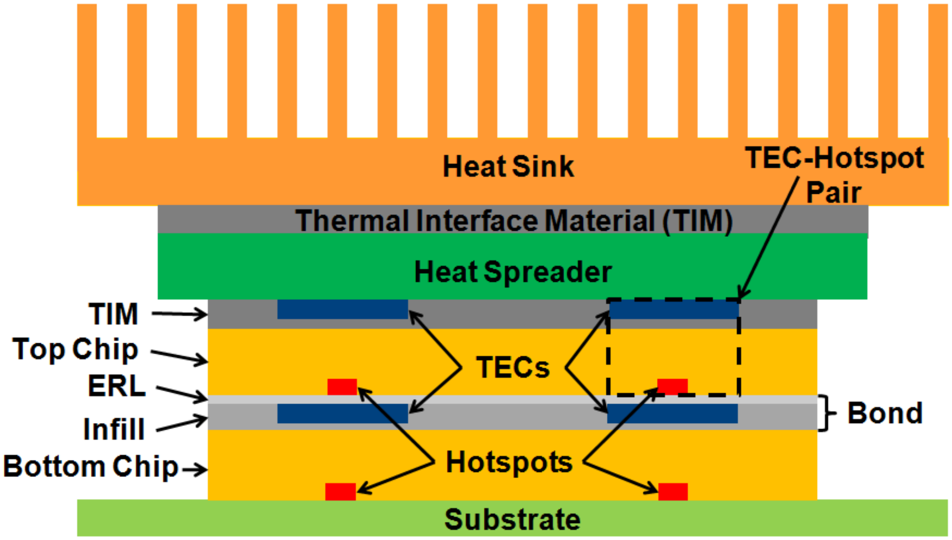

Figure 9: Schematic of the electronic package. Heat sink, heat spreader, chip, thermal interface material (TIM), effective resistance layer (ERL), infill, hotspot locations, thermoelectric coolers (TECs), and substrate are shown [126].

The effective thermoelectric properties of the Bi_2Te_3 based thin film superlattice material are considered for modeling thermoelectric (TE) material in the 100 µm thick TEC modules. In each TEC module, an 8 µm thick Bi_2Te_3 based TE material is sandwiched between two copper layers. The effective thermal conductivity of this TE material was experimentally measured to be 1.2 W/m-K in [14]. The thermal conductivity of the TIM was also determined experimentally to be 1.75 W/m-K in [14]. Electrical and thermal resistances at the interface of the TE-copper layers (10^{-11} Ωm^2; 1x10^{-6} m^{2}K/W) inside the TEC module and at the interface of the TEC-spreader (8x10^{-6} m^{2}K/W) are also taken from the experimental measurements in [14]. Selected dimensions and material properties for the model are listed in Table 3.

Table 3: Dimensions and material properties for the stacked chip TEC model.

Component	**Thermal Conductivity (W/m-K)**	**Dimensions (mm x mm x mm)**
ERL	**5**	**12 x 11 x 0.025**
Chip	**140**	**12 x 11 x 0.5**
Heat Spreader	**400**	**30 x 30 x 1**
Infill	**1.75**	**12 x 11 x 0.125**
TEC, copper	**400**	**3 x 3 x 0.046**
TEC, superlattice	**1.2 [14]**	**3 x 3 x 0.008**
TIM	**1.75 [14]**	**12 x 11 x 0. 125**

3.1.2 Modeling Method

In the model, the substrate is considered as an adiabatic interface, and the heat sink is represented by a 2050 W/m^2-K convective boundary condition with ambient temperature of 300 K for computational simplicity. The four hotspots are represented by four high heat flux sources of magnitude 1000 W/cm^2 and area 500 µm x 500 µm located at the bottom of their respective chips. A uniform heat flux of 14.5 W/cm^2 is considered for the rest of the chip area. The total power dissipation is 29.0 W per chip, or 58.1 W for the electronic package. The effective heat flux of the top and bottom chips are described by Equation 24.

$$q"=\begin{cases}1000\frac{W}{cm^2}\ at\ the\ hot\ spots\\ 14.5\frac{W}{cm^2}\quad elsewhere\end{cases} \tag{24}$$

Peltier cooling is a surface effect which is incorporated by adding heat (~αIT_h) at the hot side and subtracting heat (~αIT_c) from the cold side of the TE material. Here, T_h and T_c are the hot and cold junction temperatures and I is the applied current. The Seebeck coefficient, α, is taken as 300 µV/K based on the experimental measurement in [14]. Joule heating inside the TEC module and at the interfaces (~electrical contact resistance at TE-copper interface) is modeled by adding source terms of magnitude I^2R at the corresponding volumes and interfaces.

The Peltier and Joule effects are implemented in the model with a volumetric heating approach. Although the Peltier effect and the Joule contact heating effect are interfacial phenomena, they are represented by thin volume elements on either side of the TEC in our model. The total power due to Joule heating in the bulk thermoelectric material is defined by Equation 25. The Peltier effect is implemented using a negative heat source at the cold side of the TEC and a positive heat source at the hot side of a TEC according to Equation 26 and 26. The Joule contact heating power for a single contact is given by Equation 28.

$$P_{bulk}=\frac{I^2(2N)^2l}{A\Phi\sigma} \tag{25}$$

$$P_c=-2N\alpha IT_c \tag{26}$$

$$P_h=+2N\alpha IT_h \tag{27}$$

$$P_{contact}=\frac{I^2(2N)^2R_{elec}"}{A\Phi} \tag{28}$$

In these equations, I is applied electrical current, N is the number of TE elements, l is the TE material thickness, A is the total TEC area, Φ is the packing factor, σ is the electrical conductivity of the TE material, α is the Seebeck coefficient, T_c is the cold side temperature, T_h is the hot side temperature, and R_{elec}" is the electrical contact resistance.

This method of modeling a TEC has been validated against experimental results for a 2D electronic package using finite volume method based commercial software package Fluent [73]. An identical 2D electronic package model was developed using the finite element method based commercial software package Comsol as an alternative to Fluent modeling. Comsol has more flexibility and allows for easier parametric optimization of model parameters than Fluent. Figure 10 depicts the validation of the Comsol and Fluent TEC modeling techniques used in this paper. They are validated based on the data from the hotspot cooling experiment and model described in [14].

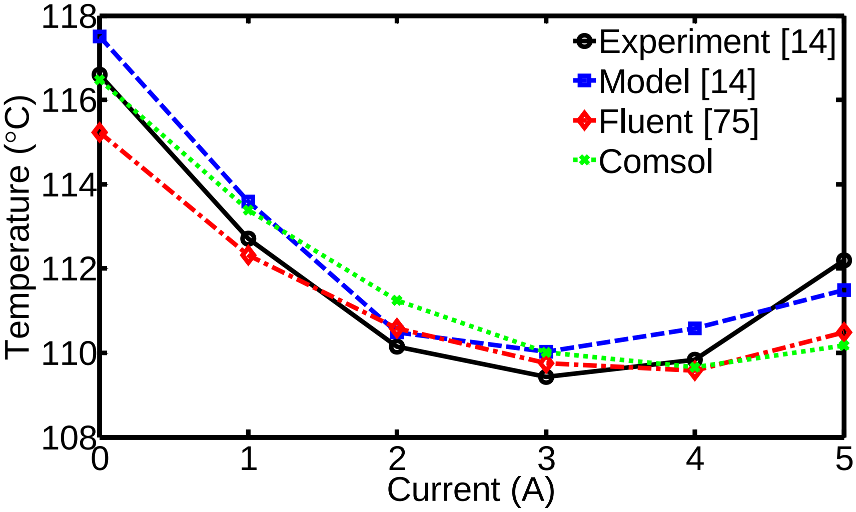

Figure 10: Validation of the Fluent and Comsol TEC modeling techniques against the experimental data and modeling results reported in [14].

Most simulations in this thesis are performed using the finite volume based commercial solver Fluent. User defined functions (UDFs) are developed to evaluate the temperature at the hot and cold junctions. The junction temperatures are used to estimate the temperature dependent Peltier cooling and heating terms (~αIT) in Equations 26 and 27. For steady state, the temperature is solved iteratively until convergence in a self-consistent fashion to ensure that the Peltier cooling terms use the right values of the hot and cold junction temperatures. For the transient simulations, the explicit temperature of the hot and cold junction was used for the duration of a time step. The present computational model contains 158,000 cells. Grid independence tests are performed using 2.9 million cells, which yield very small changes (<1%) in the temperature distribution and verify that 158,000 cells are sufficient for the numerical simulations. Typical steady state temperature contour plots in a horizontal plane through the bottom chip and in a vertical cross section of the electronic package are shown in Figures 11 and 12.

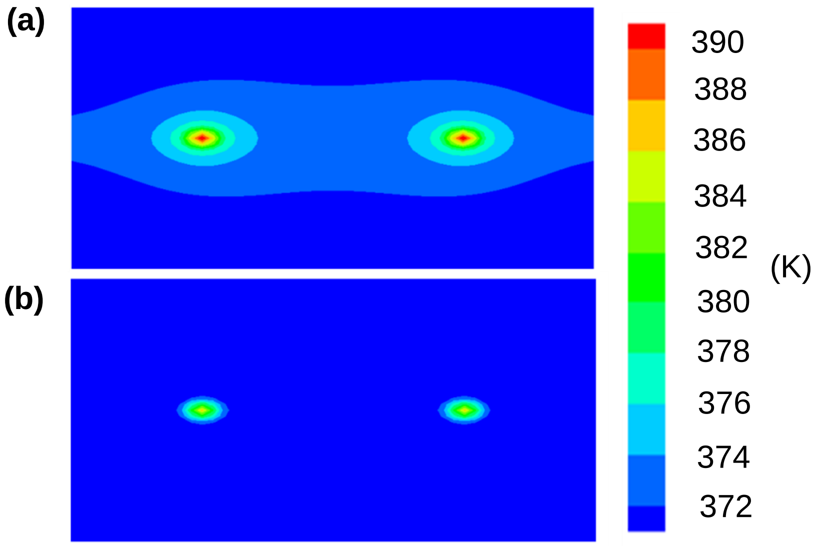

Figure 11: Temperature contour plot in a horizontal plane through bottom chip showing hotspot temperatures. (a) Temperature contour with 0 A through all four TECs. (b) Temperature contour with 1.75 A through all four TECs [126].

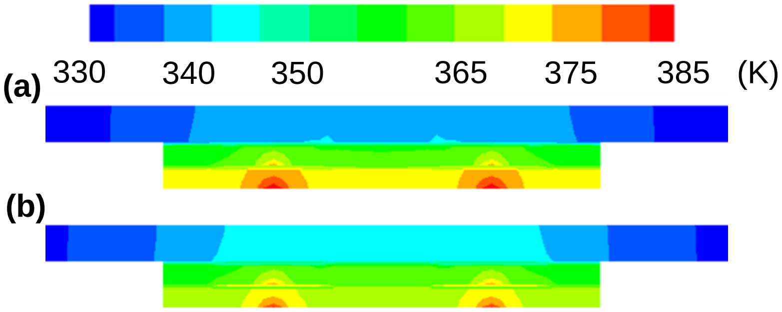

Figure 12: Temperature contour in a vertical cross section of electronic package. (a) Temperature contour with 0 A current through all four TECs. (b) Temperature contour with 1.75 A current through all four TECs [126].

3.1.3 Optimization Method

The finite element method based commercial solver Comsol was used to perform an optimization of TE material thickness and operating current. In this model, quadratic elements are employed. The present computational model contains 69,695 cells. Grid independence tests are performed using 176,208 cells yield very small changes (<1%) in temperature distribution and verify that 69,695 cells are sufficient for the numerical simulations. A total of four independent variables are considered for this optimization: the current of the top TEC (I_t), current of the bottom TEC (I_b), thermoelectric material thickness of the top TEC (l_t), and thermoelectric material thickness of the bottom TEC (l_b). The geometry, boundary conditions, material properties, and contact resistances are all held constant for this optimization, and are the same as those used in the Fluent model.

A large variety of optimization methods exist, but two of the most common methods include the gradient descent method and Newton's method [127]. The gradient descent method is a first order method and uses a function's gradient to find local extrema, while Newton's method is a second order method which uses the 2nd derivative of a function to find its local extrema. Both these methods are very effective for optimization problems where the gradient is continuous and differentiable. However, for non-continuous or non-differentiable gradients, the optimization method can oscillate around the extrema or become unstable. Both Comsol and Fluent have optimization features as a part of their software which use gradient based optimization techniques. [128, 129].

An alternative class of "direct search" optimization methods also exists. These methods can be especially useful for problems where the objective function or its gradient is non-differentiable or discontinuous. One of the simplest methods to implement is the Luus-Jaakola method [130]. In this method, the solution space is sampled and the size of the space is incrementally decreased. As the sample space size is decreased, the center of the sample space tracks the minimum or maximum point which has been sampled so far.

In this thesis, both the gradient descent method and the Luus-Jaakola method will be used. The gradient descent method is computationally efficient, but is limited in accuracy if the objective function has a discontinuous derivative or if there are multiple local minima. The Luus-Jaakola method is more computationally expensive, but also more robust, as discontinuous gradients do not affect the solution and the entire solution space is sampled. This increases the likelihood that the global, rather than local, extrema are found.

3.2 Experimental and Computational Methodology for Microchannels

3.2.1 Experimental Setup

Microchannels were fabricated by Aziz Koyuncuoglu using the fabrication method described in [106]. All other aspects of this thesis, including the experimental setup, were constructed by the author based on the previous design in [106]. For these experiments, a total of seven titanium heaters were first fabricated on a glass substrate. These heaters served the dual purposes of heat generation and temperature measurement due to their resistance varying as a function of temperature. Non-heater resistive temperature detectors (RTDs) were also fabricated on the substrate near the channel inlet and outlet. In total, these devices allowed for the temperature measurement at 9 substrate locations. The electrical leads and pads for these titanium heaters and RTDs were coated in gold so that the heaters themselves provided a majority of the electrical resistance. The titanium heaters and gold leads are shown in Figure 13.

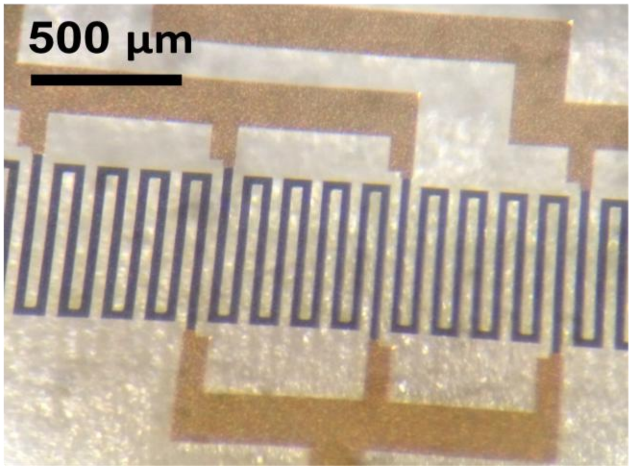

Figure 13: Titanium heaters and gold leads on glass microchannel substrate. A total of 7 heaters were fabricated along the length of the microchannels.

After the heaters were fabricated, 1or 3 microchannels were fabricated on top of the heaters according to the fabrication process described in Section 2.2.3 [106]. The microchannels were 1.42 cm long and had cross sections with dimensions 70 µm x 50 µm, 100 µm x 50 µm, or 200 µm x 50 µm. The microchannel walls were held at a constant thickness of 20 µm, and the base area of the microchannels and walls were equal to the heated area for all of the microchannel devices. One unique aspect of the microchannel devices used in these experiments is that they have up to four heated walls. The original fabrication method was developed to produce three wall microchannel devices with a gold base wall and two side walls made of copper, but it was found that additional heat transfer area could be obtained if the electroplating process duration was increased. As a result, some of the microchannel devices had a gap where the parylene layer composed part of the fourth wall, but other microchannel devices had no gap and had a base wall made of gold and three walls composed completely of copper. A microchannel cross section with and without a gap is shown in Figure 14.

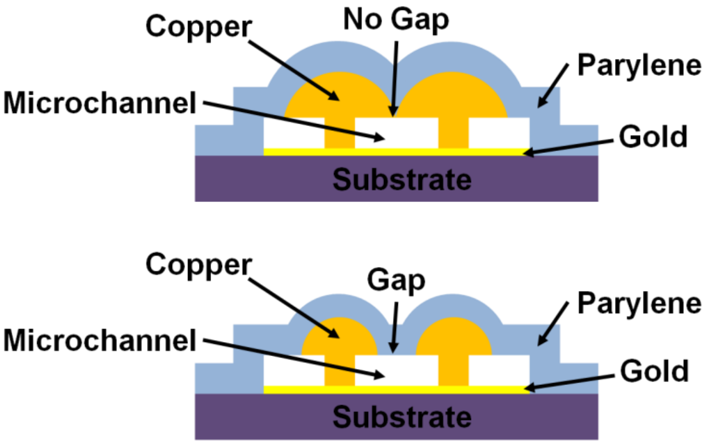

Figure 14: Microchannel cross section with more than three heated walls. The top microchannel cross section has four heated walls and the bottom cross section has nearly

four heated walls due to the gap. The 200 μm channels always had a gap, the 100 μm channels sometimes had a gap, and the 70 μm channels never had a gap.

After the heaters and microchannels were fabricated, inlet and outlet ports were attached. The inlet and outlet ports were purchased from Upchurch and were attached using epoxy. A picture of a single 70 μm microchannel and attached inlet and outlet ports is shown in Figure 15.

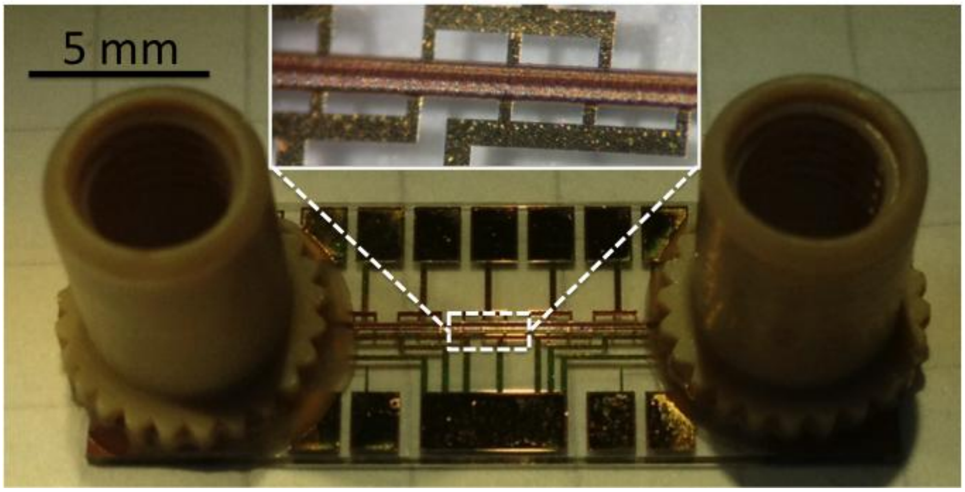

Figure 15: Image of a single microchannel with inlet and outlet ports attached.

An experimental setup, based on the design in [106], also was constructed. A printed circuit board (PCB) was used to organize the electrical wiring and enable experimental measurements on all seven heaters. One limitation of the available data acquisition system (DAQ) is that it could only measure two electrical currents directly. As a result, an electrical circuit was designed to enable indirect current measurements on the other 5 heaters. The circuit served secondary purposes of scaling down the supplied voltage during heater calibration to reduce heat generation and allowing individual heaters to be turned on or off as desired. The electrical circuit is shown in Figure 16.

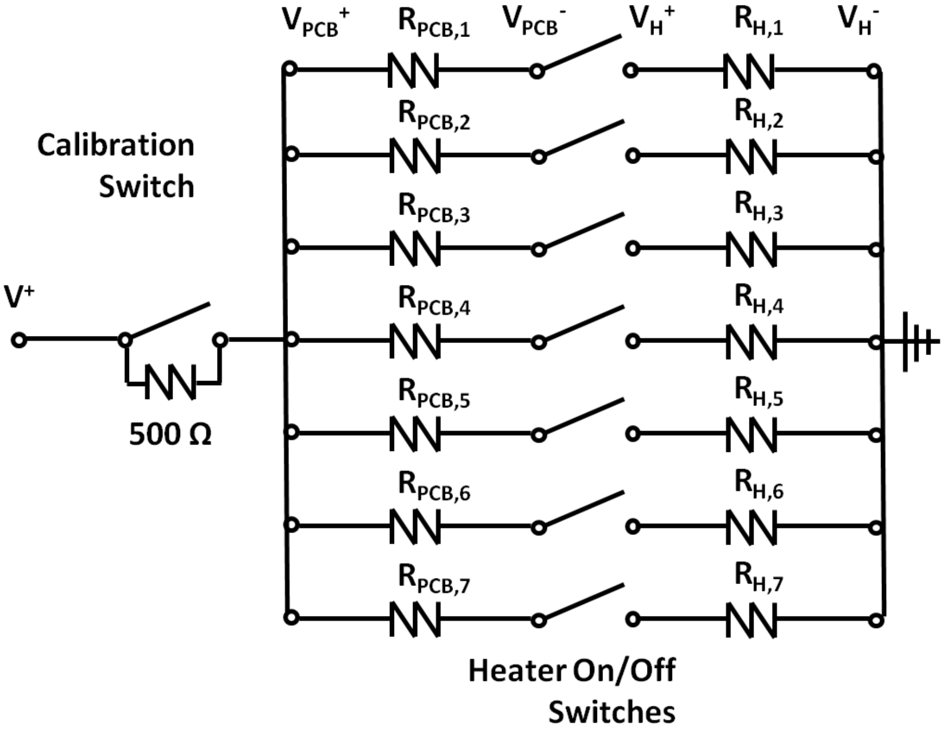

Figure 16: The electrical circuit used to enable current measurements on all seven microchannel heaters.

In this Figure, seven PCB resistances ($R_{PCB,1\text{-}7}$) are wired in with the seven microchannel heaters ($R_{H,1\text{-}7}$). These PCB resistors have a resistance of approximately 4.1 Ω. The calibration switch and 500 Ω resistor allows a very small voltage to be applied across the circuit so that four wire resistance measurements can be obtained during heater calibration with only negligible heat generation within the heaters. The 500 Ω resistor is necessary because the minimum voltage output of the power supply is 0.2 V and the resistance of the heaters ranged from 15 to 100 Ω. The heater on/off switches allow the seven PCB resistances to be measured ($R_{PCB,1\text{-}7}$) prior to an experiment and allow heaters to be turned on or off during an experiment. A picture of the experimental setup and PCB is shown in Figure 17.

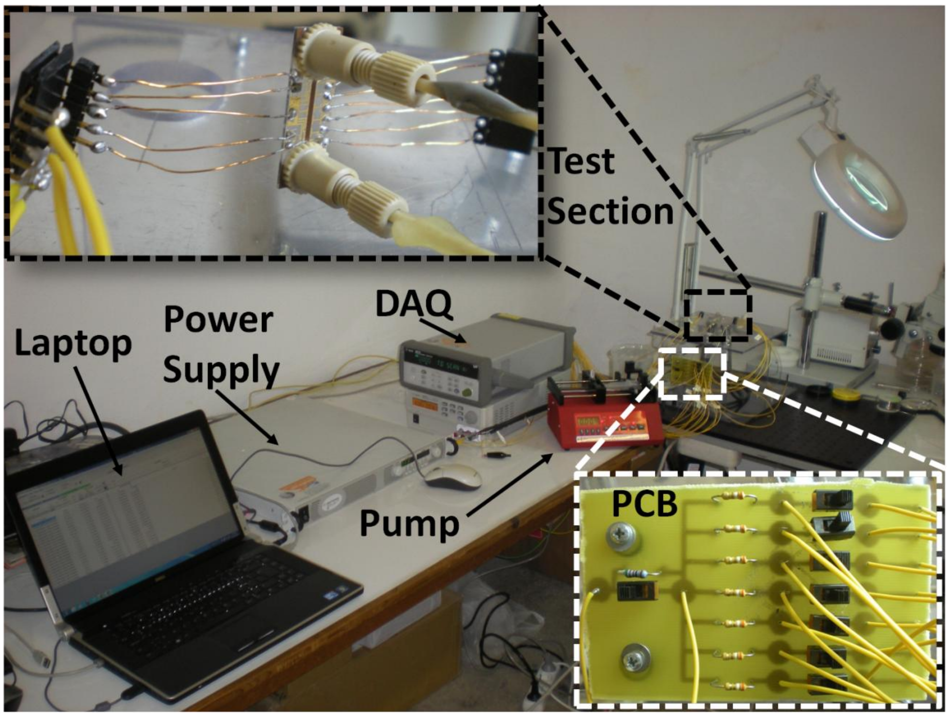

Figure 17: Experimental setup and PCB.

In this setup, the power supply provides a constant DC voltage (V^+) to the entire electrical circuit. The data acquisition system (DAQ) is used to measure the voltage drop across each resistor $(V_{PCB}^+ - V_{PCB}^-)_{1\text{-}7}$ and each heater $(V_H^+ - V_H^-)_{1\text{-}7}$. The electrical current passing through heaters 3 and 5 is also measured directly by the DAQ. A digital syringe pump (NewEra NE-4000) is used to supply de-ionized water at a constant flow rate to a microchannel test section and cool the on-chip heaters. The pressure drop across the test section is measured using two Omega absolute pressure transducers. The inlet and outlet fluid temperatures are measured using T-type thermocouples placed near the inlet and outlet ports of the test section. All data is recorded using the DAQ and sent to a laptop for data analysis.

3.2.2 Procedure

Before experimentation, each microchannel chip was first tested using a hand-held multimeter to ensure that the seven resistive heaters had approximately equal resistance. The microchannels were also inspected under a visible microscope to check for channel blockage. Inlet and outlet ports were glued to microchannel chips and were then screwed into to the experimental setup. After preparation, calibration and experimentation was performed. The experiments were performed in three phases: Nusselt number and friction factor experiments, calibration, and maximum heat flux removal experiments.

During the Nusselt number and friction factor experiments, a flow rate between 50 and 100 μL/min was supplied to the microchannels and the heater resistances were recorded before a voltage was applied. This voltage caused the generation of 12.5 W/cm^2 heat flux from the heaters. The flow rate was initially set to the minimum flow rate required to ensure that the calculated outlet temperature of the water remained below 95 °C. The outlet temperature of the water was estimated using Equation 29.

$$T_{out} = T_{in} + \frac{P_{elec}}{\dot{m}c_p} \tag{29}$$

In this equation, T_{in} is the inlet water temperature, P_{elec} is the electrical power supplied to the heaters, $\dot{m}$ is the mass flow rate of the water, and c_p is the specific heat capacity of the water.

The flow rate was incrementally increased until the pressure drop across the microchannels approached 75 kPa. This constraint was necessary to prevent damage of the pump. The pump was capable of producing pressures higher than 75 kPa, but at these pressures the internal gears of the pump would sometimes slip, which could harm the pump. In addition, at pressures of greater than 100 kPa, the tubing supplying the microchannels and the microchannels themselves were prone to leaks.

After the pressure drop was increased to 75 kPa, the sample was allowed to reach a steady state temperature. A series of voltage and current measurements were recorded in order to enable calculation of heater resistance and temperature. Measurements were also taken for the inlet and outlet temperature and pressure using thermocouples and pressure transducers. After measurements had been taken at a range of flow rates, the heaters were turned off and their resistances were measured a second time with a flow rate of between 50 and 100 μL/min. This was done to ensure that the heater resistance had not changed during the heating process. This entire procedure was repeated for the applied heat fluxes of 25 W/cm^2 and 50 W/cm^2 for each microchannel chip.

After the Nusselt number and friction factor experiments had been performed, the RTDs and heaters were calibrated. Calibration was performed in-situ by enclosing the experimental setup with a cardboard box acting as an oven. Hot air was supplied to the oven using a hair dryer with adjustable temperature and fan speed. The temperature of the oven was held constant and the sample allowed to reach steady state at six different temperatures varying from 20 to 80 °C. The oven temperature was monitored using two thermocouples at different locations in the oven. A calibration curve for two heaters is shown in Figure 18. It is interesting to note that the calibration curves for each heater are slightly different because both heaters have slightly different resistances, but the relative increase in resistance as a function of temperature for both heaters is actually the same.

This relative increase in resistance as a function of temperature can be clarified by introducing a normalized resistance value defined by Equation 30.

$$R_{normalized} = \frac{R_T}{R_{T_o}} \tag{30}$$

In this equation, R_T is the resistance at temperature T, and R_{T_o} is the resistance at room temperature. The relative increase in resistance as a function of temperature for both heaters is shown in Figure 19.

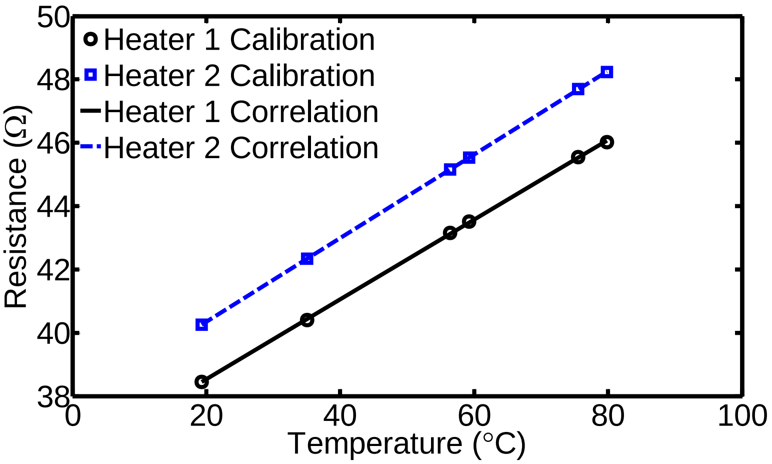

Figure 18: Calibration curve for two heaters.

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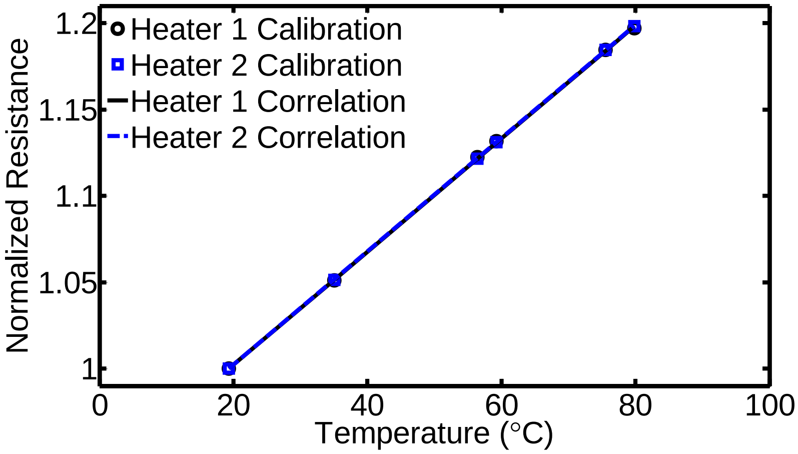

Figure 19: When the heater resistances are normalized, it is evident that the relative change in heater resistance with temperature is constant for both heaters.

After the calibration, the microchannel devices were tested to determine the maximum heat flux they were capable of removing from the chip. This was done by alternating an increase in the heat flux supplied by the heaters and an increase in the flow rate to ensure that the expected outlet temperature of the water remained below 95 °C. Again, the pressure drop was monitored to ensure that it remained below 75 kPa. The heat flux removal by the microchannels was limited by this pressure drop requirement because it prevented adequate fluid supply to the microchannels under a high heat flux. During these maximum heat flux removal experiments, the heaters began to change resistance as they approached their breaking point. As a result, the inlet and outlet thermocouples were used to determine the inlet and outlet fluid temperatures as well as calculate the heat flux removed using Equation 31.

$$q'' = \dot{m}c_p(T_{out} - T_{in})/A_{heated} \tag{31}$$

In this equation, $\dot{m}$ is the mass flow rate, c_p is the specific heat, T_{in} and T_{out} are the inlet and outlet temperatures measured by the thermocouples, and A_{heated} is the base microchannel area where the heaters were located.

3.2.3 Data Analysis

The pressure drop is measured using two pressure transducers connected to the inlet and outlet ports of the microchannels using 10 cm length and 1.5 mm diameter plastic tubes. Calculations show that the pressure drop in this tube for the experimental flow rates tested in this work is less than 0.1% of the pressure drop in the microchannels; so it is neglected. However, minor losses due to contraction and expansion at the microchannel inlet and outlet should not be neglected as they can account for up to 5% of the pressure drop measured by the pressure transducers. The measured pressure drop across the microchannels is corrected with Equations 32 and 33 and the friction factor in the microchannels is calculated using Equation 34 [104].

$$\Delta P = \Delta P_{measured} - \Delta P_{minor} \tag{32}$$

$$\Delta P_{minor} = K_{in}\left(\frac{\rho_{in}u_{in}^2}{2}\right) + K_{out}\left(\frac{\rho_{out}u_{out}^2}{2}\right) = 0.5\left(\frac{\rho_{in}u_{in}^2}{2}\right) + \left(\frac{\rho_{out}u_{out}^2}{2}\right) \tag{33}$$

$$f = \frac{2\Delta P D_h}{L\rho_{avg}v_{avg}^2} \tag{34}$$

In these equations, ΔP is the pressure drop, K_{in} is the k-factor for sudden contraction, K_{out} is the k-factor for sudden expansion, ρ is the density, v_{avg} is the mean fluid velocity, D_h is the hydraulic diameter, and L is the length of the microchannel. K-factors are used to determine pressure losses due to pipe bends, expansion, and contraction. Similar corrections were performed in [103-105]. For comparison, the theoretical friction factor for fully developed flow can be calculated using Equation 35 [103].

$$f = \frac{4.7 + \frac{19.64(\gamma^2 + 1)}{(\gamma+1)^2}}{Re} \tag{35}$$

In this equation, Re is the Reynolds number, f is the friction factor, and γ is the aspect ratio of the channel. Fully developed flow is a good approximation for these experiments because a Reynolds number of 150 will result in an entrance length of only 0.7 mm. This is only 5% of the total channel length.

The determination of the Nusselt number is a much more complicated calculation. In order to calculate Nusselt number, it is necessary to first calculate the heat transfer coefficient in the channel. This has been done previously using a variety of methods which were summarized in Chapter 2 [103-106]. These calculations require knowledge of the channel wall temperature, fluid temperature along the channel, and heat flux from the substrate to the microchannel. In this experiment, these values can be calculated using the following process.

The temperature of the seven microchannel heaters can be determined based on the voltage and current measurements taken during the experiment. The voltage and current of PCB resistances 3 and 5, and heaters 3 and 5 are measured directly. Their resistances are easily calculated using the well-known V=IR relationship. The other PCB and heater resistances are calculated using a different method because the DAQ hardware had only two ports capable of direct current measurement. First, the resistance of the PCB resistors (~4.1 Ω) is measured at room temperature. These resistors had the same resistance at the beginning and end of the experiments, although temperature variation may have occurred during the experiment. The resistance of these resistors during the experiment is calculated using Equation 36. This equation is simply an adjustment which assumes that the percent change in a PCB resistor number *N* is equal to the average percent change of the PCB resistors 3 and 5. This equation is meant to account for the possible change in resistance of the constant resistors, because it could not be measured directly.

$$R_{PCB,N} = R_{PCB,N_o}\left(1 + \frac{\frac{R_{PCB,3} - R_{PCB,3_o}}{R_{PCB,3_o}} + \frac{R_{PCB,5} - R_{PCB,5_o}}{R_{PCB,5_o}}}{2}\right) \tag{36}$$

In this equation, R is resistance, the subscript PCB indicates that it is a PCB resistor, the number *N* stands for any resistor numbered 1, 2, 4, 6, or 7, and the subscript *o* indicates it was measured at room temperature before or after the experiment.

Following this logic, the current I_N through the heaters and resistances is calculated indirectly based on the constant PCB resistance and the voltage measured across it as shown in Equation 37.

$$I_N = \frac{V_{PCB,N}}{R_{PCB,N}} \tag{37}$$

Finally, the resistance of the heater is calculated based on the calculated current and the measured voltage drop across the heater during an experiment, shown in Equation 38.

$$R_{HN} = \frac{V_{H,N}}{I_N} \tag{38}$$

The temperature of the heaters is determined based on the calibration curve described previously. The heat generated, Q_H, along with the heat flux, q''_{HN}, produced by heater number *N* is calculated using Equations 39 and 40.

$$Q_{H,N} = I_N V_{H,N} \tag{39}$$

$$q"_{H,N} = \frac{Q_{H,N}}{A_{heated}} \tag{40}$$

The temperature of the microchannel walls is extremely close to the temperature of the heaters. This is because a 0.45 μm layer of parylene and a 0.4 μm layer of gold is placed between the titanium heater and the channel walls. The thermal resistance of the gold layer is less than 0.1 % of the thermal resistance of the parylene layer, so it is neglected in these calculations. A simple one-dimensional correction is used to determine the temperature of the channel walls above a heater, shown in Equation 41.

$$T_{wall,N} = T_{heater,N} - q"_{H,N} \frac{l_{parylene}}{k_{parylene}} \tag{41}$$

This wall temperature is considered to be equal to the temperature for the bottom wall of the microchannel, and it is assumed to be the same for the channel side walls and the copper portion of the top of the microchannel. This assumption is justified because the copper side walls have a minimum fin efficiency of 99%. Other assumptions made in the calculation of the Nusselt number include neglecting axial heat conduction in both the water and the substrate, and neglecting viscous heating in the microchannels. Calculations justifying these assumptions are detailed in Appendix A, but it is important to note that negligible axial heat conduction is a necessary assumption, but one which is only true for some of the experimental conditions. This is addressed by discarding experimental data points where axial heat conduction cannot be neglected in Section 5.1.2. It is also important to note that 3-D CFD simulations suggest that the base temperature of the channels can vary by as much as 1 °C, which is discussed in Section 5.3.3.

After calculation of the axial heat flux and channel wall temperatures, it is necessary to determine the water temperatures in the microchannels. Thermocouples in the inlet and outlet ports and RTDs located within 150 μm of the channel inlet and outlet can be used to measure the fluid inlet and outlets. However, during experimentation, it was determined that the close proximity of the heaters to the inlet and outlet RTDs were causing the RTDs to read temperatures that were higher than the actual fluid temperature. It would have been possible to correct this by using only 5 heaters, rather than 7, but turning off the end heaters would have the undesirable effects of introducing unheated lengths to the microchannel and reducing the amount of data collected. The purpose of using 7 heaters was to avoid these undesirable effects.

In previous experiments, which were detailed in Section 2.2.5, there were generally three ways to calculate the Nusselt number. In the first method, the log mean temperature difference was used to compare the inlet and outlet wall temperature to the inlet and outlet fluid temperatures [104, 105]. In this thesis, it is called the LMTD method. In the second method, the average wall temperature along the entire channel was compared to the average fluid temperature in the entire channel [103]. In this thesis, it is called the Average method. And in the third, the local wall temperature at the channel mid-point was compared to the local fluid temperature at the channel mid-point [106]. In this thesis, it is called the mid-point method. These three methods all result in slightly different Nusselt numbers.

The determination of the inlet, outlet, average, and mid-point fluid temperatures for use in Nusselt number calculations is difficult. In previous experiments, one method used to calculate these fluid temperatures assumed that the water temperature varied linearly between the inlet and outlet temperatures as measured by thermocouples [103-105]. In this thesis, it is called the thermocouple (TC) method. The other assumed that the water temperature increased at the same rate as the wall temperature in the fully developed region of the flow [106]. In this thesis, it is called the fully developed (FD) method.

Although the TC method requires no further explanation, the FD method is not as simple. In this method, the inlet temperature is determined using the inlet thermocouple, and the outlet temperature is determined by assuming that the water temperature increases at the same rate as the wall temperature in the fully developed region of the flow. Figure 20 demonstrates this method using data from a single 200 μm width channel. In this figure, the fully developed region is taken as the wall temperature above heaters 2-7 and the average slope of the wall temperature vs. position is determined using linear regression.

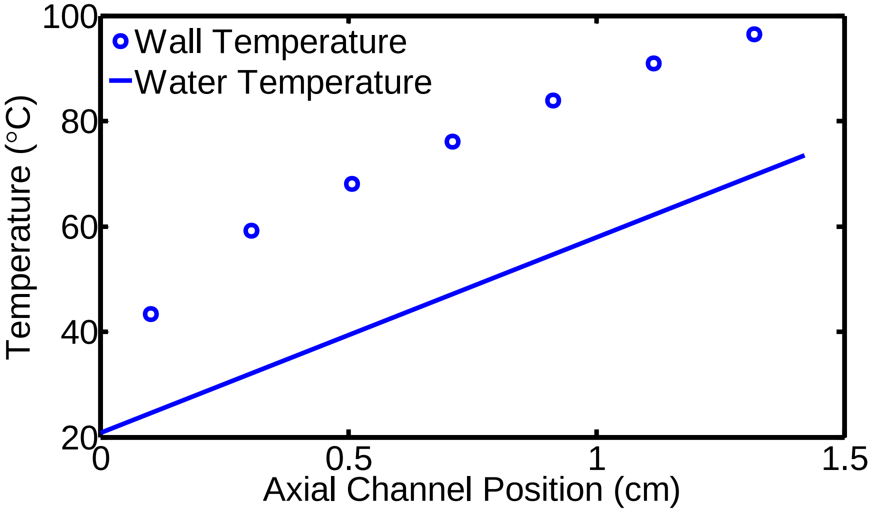

Figure 20: When using the fully developed (FD) method, the axial water temperature inside the microchannel and at the outlet is determined using the measured inlet temperature and by assuming that the water temperature increases at the same rate as the channel wall temperature in the fully developed region.

The combination of the two methods for determining water temperature and the three methods for determining Nusselt number leads to a total of six methods which could be applied to the experimental data obtained in this study. All six methods were used to calculate Nusselt number on a three channel device with 100 µm channel widths. The calculated Nusselt numbers are shown in Figure 21.

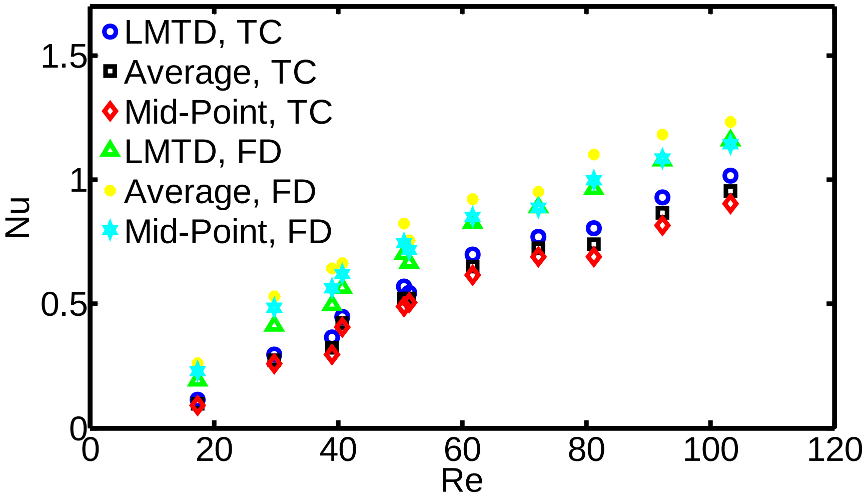

Figure 21: Experimentally determined Nusselt numbers for a three channel, 100x50 um cross section device. A total of six different methods were used to calculate these Nusselt numbers. Various combinations of these methods have been used in previous microchannel experiments [103-106].

This chart was very useful in choosing the best method to rely on to calculate the Nusselt number. It is clear that using the TC method to determine water temperature results in lower Nusselt numbers than the FD method. This is because the thermocouple is located downstream from the actual microchannel outlet. As a result, heat losses occur between the actual channel outlet and the thermocouple. This effect is even more pronounced for the single channel devices, and suggests that the FD method should be used.

Another important observation which can be made is that the LMTD and Average method generally result in higher calculated Nusselt numbers than the Mid-point method. This is because the Mid-point method only calculates the Nusselt number at the center of the microchannel where the flow is hydrodynamically and thermally fully developed. The LMTD and Average methods include the developing region in their calculation of Nusselt number, leading to higher calculated Nusselt numbers.

Based on these observations, the Mid-Point and Fully Developed (FD) methods will be used in this work to calculate the Nusselt number. First, the heat removal by the working fluid between the 3rd and 5th heaters is calculated. This calculation is shown in Equation 42.

$$\dot{Q} = \dot{m} c_p (T_{m,5} - T_{m,3}) \tag{42}$$

In this equation, $\dot{m}$ is the mass flow rate, c_p is the specific heat of the fluid, $T_{m,5}$ is the mean fluid temperature at a location corresponding to the 5th heater location, and $T_{m,3}$ is the mean fluid temperature at a location corresponding to the 3rd heater location.

It is important to note that only the heat removed by the fluid was considered when calculating the Nusselt number in this work. The same technique was used in [106]. Other experiments have subtracted the losses from the heat generation in order to determine the heat transport from the substrate to the fluid [103-105]. The result of Equation 42 is affected by whether the TC or FD method is used to determine the water temperature.

Next, the weighted mean wall temperature between heaters 3 and 5 is calculated using Equation 43.

$$T_w = \frac{T_{w,3}}{4} + \frac{T_{w,4}}{2} + \frac{T_{w,5}}{4} \tag{43}$$

In this equation, $T_{w,3}$, $T_{w,4}$, and $T_{w,5}$, are the wall temperatures above heater 3, 4, and 5, respectively. The convection coefficient at the channel mid-point is calculated using Equation 44.

$$h = \frac{\dot{Q}}{A(T_w - T_m)} \tag{44}$$

In this equation, $\dot{Q}$ is obtained from Equation 42, A is the area of the microchannel walls between the 3rd and 5th heaters, T_w is obtained from Equation 43, and T_m, is the mean water temperature between the 3rd and 5th heaters.

Finally, the Nusselt number is calculated using Equation 45.

$$Nu = \frac{hD_h}{k} \tag{45}$$

In this equation, h is the convection coefficient, D_h is the hydraulic diameter, and k is the thermal conductivity of water. All fluid properties are evaluated at the mean fluid temperature.

The total heat losses from the sample to the ambient are calculated by considering the energy generated in the heaters and the temperature gain of the working fluid according to Equation 46.

$$Losses = 1 - \left(\frac{\dot{m}c_p(T_{out} - T_{in})}{Q_{gen}}\right) \tag{46}$$

In this equation, $\dot{m}$ is the mass flow rate, c_p is the specific heat of the working fluid, T_{out} is the fluid outlet temperature, T_{in} is the fluid inlet temperature, and Q_{gen} is the electrical heat generation in the microchannel heaters obtained by summing the product of current and voltage for each of the seven heaters.

3.2.4 Computational Fluid Dynamics (CFD) Model

A computational fluid dynamics (CFD) model of the three channel devices for 70, 100, and 200 μm channel widths was built using the commercial finite element solver Comsol. This model was built to compare the obtained experimental results with those using a 3-D coupled heat transfer and fluid flow simulation. This is important to help determine whether the assumptions used in the calculation of Nusselt number are correct [114]. It also serves as a useful model for comparison against the experimental results and against other modeling methods. The model geometry was built according to the dimensions of three microchannel devices tested during the experiments. A cross section schematic of the model is shown in Figure 22.

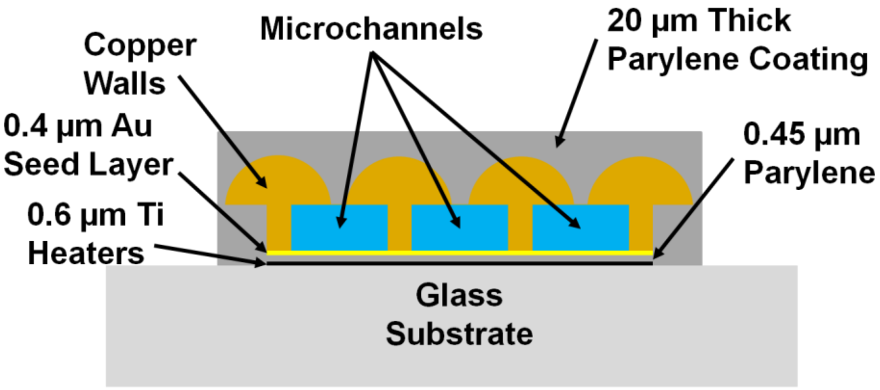

Figure 22: A schematic of the computational domain for the microchannel simulations.

In this model, a glass substrate 500 μm thick, 1.42 cm long and 1 cm wide is modeled with three microchannels each of length 1.42 cm and varying cross sections. A 0.6 μm thick titanium heater is modeled in three dimensions on top of the glass substrate.

In addition, a 0.45 μm thick parylene layer is modeled as a thermal boundary resistance sandwiched between the titanium heater on one side, and a 0.4 μm thick gold seed layer on the other side. Copper walls are deposited using electroplating on top of the seed layer. The 20 μm thick copper walls extend nearly all the way around the microchannel, leaving a gap at the top of the microchannel. A thick (~20 μm) parylene coating was deposited as the final step in the fabrication process to seal the channels and is included in the model. The model uses temperature and pressure dependent material properties for de-ionized water. The material properties for other portions of the model are shown in Table 4.

Table 4: Material properties used in microchannel computational model.

Component	**Thermal Conductivity (W/m-K)**
Glass Substrate	1.38
Parylene	0.082
Titanium	21.9
Copper	400
Gold	317

The conservation equations for mass and heat are fully coupled with the Navier Stokes equations in this model. The inlet boundary condition is a constant temperature and velocity boundary condition corresponding to the inlet temperature (T_{in}) and flow rate (f) in the experiment. The outlet boundary condition is a constant pressure outflow boundary condition. The boundary conditions on the interior channel walls are no slip and heat continuity is satisfied on all internal boundaries in the model. The titanium heaters have uniform volumetric heat generation specified using the total power generation measured in the experiment (Q_{tot}). All exterior surfaces in the model are modeled with a 10 W/m^2K convection boundary condition, corresponding to natural convection in air. Table 5 contains the channel dimensions and boundary conditions for each of the three models. It should be noted that the exact channel height does not match the nominal height of 50 μm. This best estimate of channel height was found by measuring the channel height at five different locations on the fabrication wafer. For the 70 μm wide channels, the absence of a channel gap was approximated by assigning a gap of only 1 μm.

Table 5: Channel dimensions and boundary conditions for computational models.

Number of Channels N	**Channel Height H (μm)**	**Channel Width W (μm)**	**Gap G (μm)**	**Total power generation Q_{tot} (W)**	**Inlet Temperature T_{in} (°C)**	**Flow rate, f (μL/min)**
3	47.57	70	1	2.30	19.56	500
3	47.57	100	10	1.46	18.60	750
3	47.57	200	67	1.00	18.84	900

The three different geometries use the same meshing algorithm which results in a total of between 81,660 and 87,030 linear mesh elements for each model. A majority of these elements are concentrated in the microchannel, fins, seed layer, and heater portions of the computational domain. Mesh independence was verified for the 100 μm wide channel model using up to 213,930 mesh elements. The pressure drop between the 83,370 element and 213,930 element meshes differs by 3%. The axial heater temperatures for three different mesh sizes on the 100 μm wide channel model are compared in Figure 23. Since all three geometries use the same meshing algorithm, all of them should also be mesh independent.

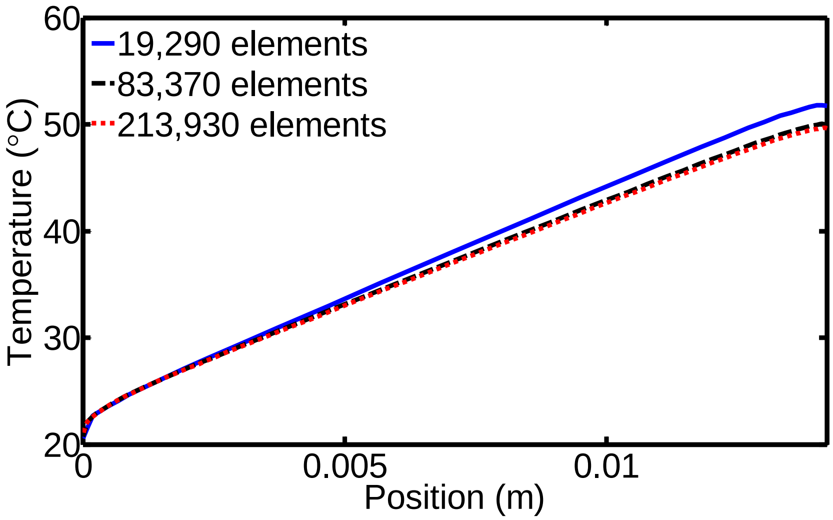

Figure 23: Comparison of the axial heater temperature using the fully coupled CFD simulation for three different mesh sizes. The 83,370 element mesh is used in this work.

3.2.5 Empirical Correlation Based Model

The microchannels tested with de-ionized water as a working fluid are well within the continuum regime, and are expected to match with the CFD results [111, 112]. However, 3D CFD models can be very computationally expensive, so less computationally intensive modeling methods were explored. It is possible to perform a 2D CFD simulation for the microchannel cross section in the fully developed region of the channel, but the models do not allow accurate consideration of thermal and fluid flow development like in a 3D CFD simulation [131-133]. The most common microchannel modeling method is the resistor network model, which was popularized by Phillips and accounted for heat spreading, fin efficiency, and thermal interface resistance in the IC package [134-136]. These studies rely on classical fin analyses and provide a simple way to evaluate microchannel heat transfer [133, 137]. Resistor network models are sufficient to predict microchannel heat transfer, but neglect some conduction effects which may affect solution accuracy or insights into the physics of the problem. For this reason, an empirical correlation based model is proposed.

Previous efforts to simplify CFD models have used a thin wall to represent conduction in the microchannel walls and have modeled the fluid flow explicitly [138]. The proposed empirical correlation based model does the reverse. It uses finite element analysis to model conduction in the microchannel substrate and channel walls. Convection from the wall to the fluid is represented by a convection boundary condition with convection coefficient determined by an empirical correlation. The mean fluid temperature is assumed to be linear from the channel inlet to outlet with the temperature rise determined using an energy balance. This allows the water portions of the model to be removed, reducing the number of elements in the model and eliminating the need to solve the Navier Stokes Equations. This significantly reduces the solution time of the simulation.

The convection coefficient of the channel walls can be determined using correlations for fully developed or developing flow for four walls. A four wall correlation is used because nearly all four walls of the experimentally tested microchannels act as heat transfer surfaces, even though there is a small gap on the top wall where parylene acts as an insulator. The correlation for fully developed flow is given by Equation 47 [139].

$$Nu = 8.235\left(1 - \frac{2.0421}{\alpha} + \frac{3.0853}{\alpha^2} - \frac{2.4765}{\alpha^3} + \frac{1.0578}{\alpha^4} - \frac{0.1861}{\alpha^5}\right) \tag{47}$$

In this Equation, α is the channel aspect ratio. For developing flow, a correlation has been obtained in [140], which can be expressed as:

$$Nu = \frac{1}{C_1(z^*)^{C_2} + C_3} + C_4 \tag{48}$$

This Equation is valid in the developing region, which is defined as x < $x_{fd,t}$, and for aspect ratios, α, of between 1 and 10. The constants $C_{1\text{-}4}$ are defined according to Equations 49-52, and $x_{fd,t}$ is given by Equation 53.

$$C_1 = -3.122 * 10^{-3}\alpha^3 + 2.435 * 10^{-2}\alpha^2 + 2.143 * 10^{-1}\alpha + 7.325 \tag{49}$$

$$C_2 = 0.6412 \tag{50}$$

$$C_3 = 1.589 * 10^{-4}\alpha^2 - 2.603 * 10^{-3}\alpha^3 + 2.444 * 10^{-2} \tag{51}$$

$$C_4 = 7.148 - \frac{13.28}{\alpha} + \frac{15.15}{\alpha^2} - \frac{5.936}{\alpha^3} \tag{52}$$

$$x_{fd,t} = -1.275 * 10^{-6}\alpha^6 + 4.709 * 10^{-5}\alpha^5 - 6.902 * 10^{-4}\alpha^4 + 5.014 * 10^{-3}\alpha^3 - 1.769 * 10^{-2} * \alpha^2 + 1.845 * 10^{-2}\alpha + 5.691 * 10^{-2} \tag{53}$$

In the empirical correlation based model, the de-ionized water in the channels is assumed to be incompressible with constant fluid properties evaluated at the mean fluid temperature for the length of the channel. Radiation heat transfer is neglected. These assumptions are frequently used in resistor network analyses [95, 137, 141]. Two empirical correlation based models have been proposed. In the first, the flow is assumed to be fully developed and Equation 47 is used to determine the convection coefficient throughout the channel. In the second, thermally developing flow is considered using Equations 48-53. These two empirical correlation based models are compared with the CFD model described in Section 3.2.4, and the resistor network model described in the following section.

3.2.6 Resistor Network Model

A resistor network model is employed to compare the predicted temperature distribution of the package to the predictions using 3D CFD model and the empirical correlation based models. The resistor network model uses the same assumptions as the previously described empirical correlation based models which are also commonly used in resistor network models in literature [134, 137, 141]. The flow is steady state, laminar, with constant fluid properties, and with radiation heat transfer neglected. These assumptions are frequently used in the resistor network analyses [95, 137, 141]. Two resistor network models are used. In the first, the flow is assumed to be fully developed and Equation 47 is used to determine the convection coefficient throughout the channel. In the second, thermally developing flow is considered using Equations 48-53.

The resistor network model employed in this work is a 2D network considering 100 equally spaced nodes in the axial channel direction and three nodes in the direction normal to the substrate. The three nodes in the direction normal to the substrate are used to determine the heater temperature, channel wall temperature, and fluid temperature. The resistor network employs the iterative Gauss-Siedel method with a relative error tolerance of 10^{-9} to solve for temperature.

A schematic of the resistance network is included in Figure 24. In the axial direction, conduction in the substrate and walls is considered between heater and wall temperature nodes. Axial conduction in the water is neglected, but thermal resistances representing the flow of water and advective heat transfer are included. In the direction normal to the substrate, the thermal resistance from the heater nodes to channel wall nodes considers the resistance of the titanium, parylene, and gold layers between the heater and channel wall. The temperature of the gold channel base and the copper channel walls is assumed to be constant because the fin efficiency is very near to 100%, as is shown in Appendix A. Lastly, the thermal resistance between the channel wall and water is calculated using Equations 47-53.

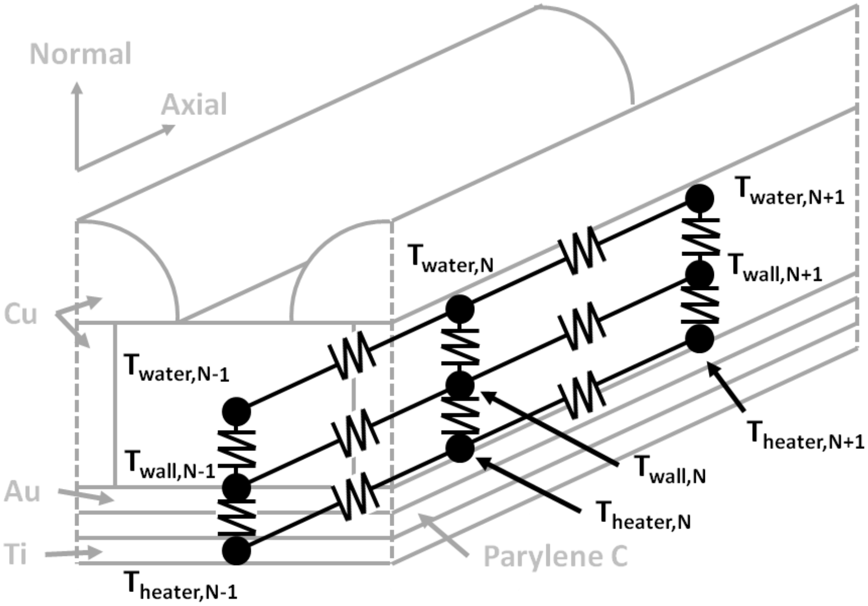

Figure 24: A schematic of the resistance network for microchannel modeling. The resistor network is in black, and geometric microchannel features are in gray.

CHAPTER 4

HOT SPOT COOLING USING THERMOELECTRIC DEVICES

In this chapter, the steady state performance of the TECs in both active and passive state with different current magnitudes is first explored and the coupling between TECs integrated with the stacked dies is investigated. This study is the first of its kind for TECs integrated into a stacked chip package. Next, the effectiveness of TECs in providing cooling at different hot spot locations on dies during their simultaneous operation is studied. The variation of the thermal contact resistances between dies, inside the TEC module, and between the TEC and heat spreader is examined. Then, the transient performance of the TECs under varying current amplitudes and pulse shapes is explored. Finally, optimum geometry and operation conditions are determined in order to achieve either maximum cooling, or maximum cooling efficiency.

4.1 Steady State Hotspot Cooling

4.1.1 Active and Passive Cooling

A benchmark analysis was performed to see the variation in maximum temperatures on the chip without TECs, with TECs, and with 100 µm thick copper blocks in place of the TECs. A significant amount of passive cooling, or cooling without an applied current, was observed in [14] due to the high thermal conductivity of copper making up a large portion of the device. In our model, integrating TECs causes passive cooling of 8.9 ºC at the bottom hotspots and a passive cooling of 8.1 ºC at the top hotspots compared to the chip without TECs. However, the passive cooling by 100 µm thick copper blocks is larger (12.5 ºC at the bottom hotspots and 10.7 ºC at the top hotspots) than passive cooling by TECs as the effective conductivity of the TEC module is lower than copper. The value of integrating a TEC in a package cannot come from its passive cooling, but must come from its ability to provide active, on-demand cooling.

Next, a steady state analysis was performed by applying the same current to all four TECs in the range of 0 – 4 A. Figure 25 shows that maximum active cooling at the top hot spot is only 0.9 °C corresponding to 0.75 A current through all four TECs. Active cooling of 5.6 °C is observed at the bottom hotspots when 1.75 A current is applied through TECs. As the applied current magnitude increases, the Peltier cooling effect is eventually overcome by the detrimental Joule heating effect occurring within the TECs and the contacts. It is important to notice that the top chip experiences small amounts of active cooling with all four TECs active at an equal constant current. Later sections of this paper show that this is due to heating of the top hotspots by the bottom TECs.

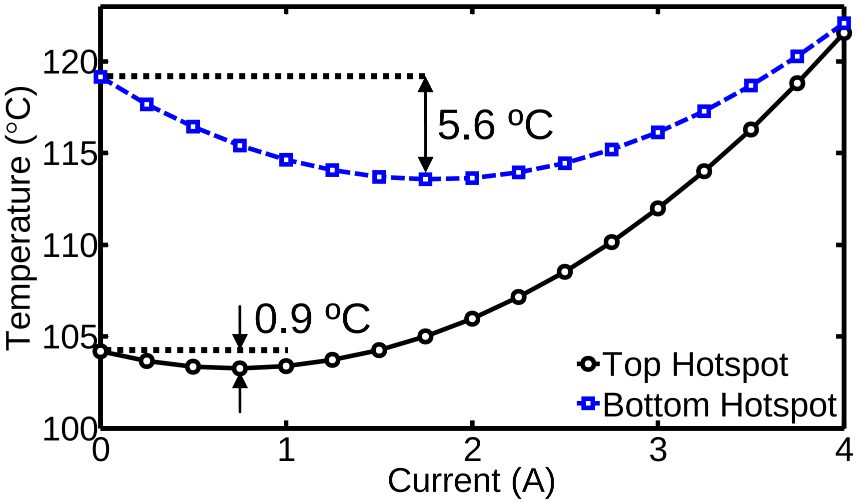

Figure 25: Hotspot temperature variation with applied current in TECs. Current through all four TECs is the same [126].

In order to explore the best possible cooling at top and bottom hot spots by TECs, we next apply current with different magnitudes in top and bottom TECs in the range of 0

– 3 A rather than keeping them at the same value. The maximum total cooling at the top hotspots was observed to be 12.6 °C (~ 4.5 °C active). This cooling was observed for a top current, I_t, equal to 2.5 A and a bottom current, I_b, equal to 0 A. The maximum total cooling at the bottom hotspots was observed to be 14.6 °C (~ 5.6 °C active). This cooling was observed for a top current, I_t, equal to 2.0 A and a bottom current, I_b, equal to 1.75 A. These results are similar in magnitude to those observed in [14, 73, 74]. Figure 26 compares the maximum total cooling (active + passive) obtained by TECs to the passive cooling obtained by TECs or copper blocks. It is clear that the active cooling achieved using TECs is higher than the passive cooling using copper blocks. Furthermore, TECs can be fabricated directly on chip using MEMS processes, or the thickness of a TEC can be further decreased. This would diminish the passive cooling effects of both TECs and copper blocks while the active cooling effects of the TECs would remain approximately the same.

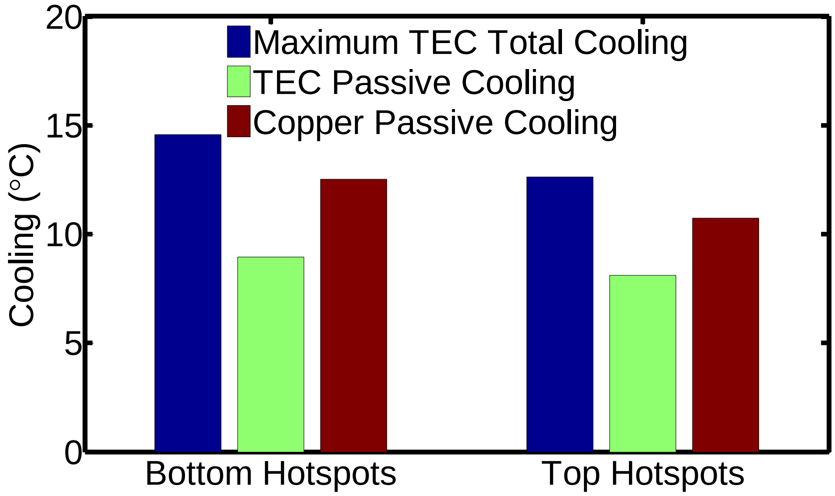

Figure 26: Comparison of maximum TEC total cooling (active + passive), TEC passive cooling, and passive cooling by 100 µm thick copper pieces [126].

It was also observed that small changes in the applied currents yielding maximum active cooling did not significantly change the observed cooling. It is desirable to use applied currents as small as possible in an effort to reduce energy consumption in TECs. Using 20% less current in the top TECs (2.0 vs. 2.5 A) and no current in bottom TECs leads to only a 5% decrease in active cooling of the top hotspots (4.3 vs. 4.5 °C). Similarly, reductions of top and bottom TEC current by 0.5 A (1.5 vs. 2.0 A for top current; 1.25 vs. 1.75 A for bottom current) results in only a 6% decrease in active cooling for the bottom hotspot (5.3 vs. 5.6 °C). This suggests that lower currents might be used to obtain similar cooling performance with significant energy savings as Joule heating is proportional to current magnitude squared.

The goal of these studies was not to optimize the current through the TECs, but to explore the effects of different current magnitudes. These studies suggest that, in steady state, current magnitudes of 1.75 A provide a balance of cooling and energy consumption. For this reason, 1.75 A current magnitudes are extensively used in the steady state portion of this study.

4.1.2 Effect of TEC Location on Hotspots

A study was performed to determine the contribution to hotspot cooling by a TEC at various locations relative to the hotspot. Beginning with zero applied current to all TECs, a 1.75 A current was applied to a single TEC under consideration. Temperature drops or rises were recorded for all hotspots along with the locations of the hotspots and activated TEC. This was repeated for all four TECs. This same procedure was performed for starting configurations where 1, 2, or 3 of the TECs already had an applied current of 1.75 A, and a 1.75 A current was applied to a non-active TEC. *It was observed that the* *cooling at a single hotspot was dependent only on the activated TEC's location and independent of the starting configuration or magnitude of applied current to other TECs*. This can be explained using the superposition principle which applies to linear systems. TECs caused negligible horizontal (0.05 °C) and diagonal (0.3 °C) cooling (see Figure 9 for TEC locations). However, significant vertical coupling between TECs and hotspots was observed as shown in Figure 27.

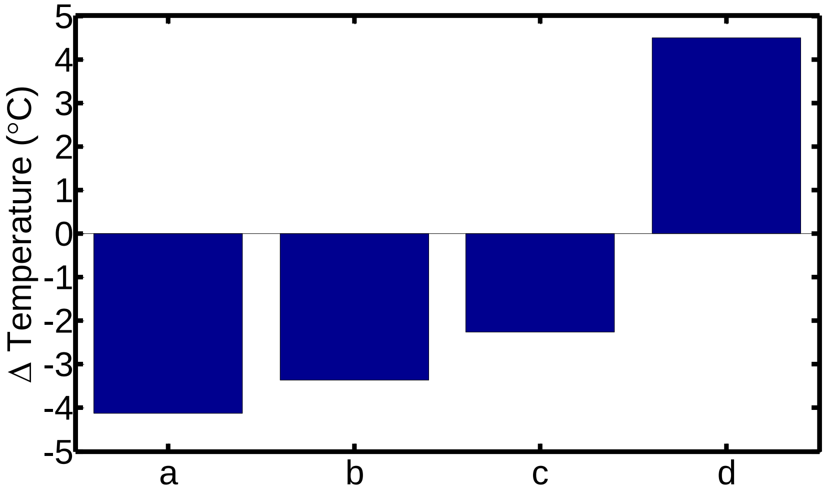

Figure 27: Change in peak hotspot temperature as a result of activating additional TECs with 1.75 A current. (a) Cooling on top hotspot caused by activating top TEC. (b) Cooling on bottom hotspot caused by activating bottom TEC. (c) Cooling of bottom hotspot caused by activating top TEC located at same horizontal location. (d) Heating of top hotspot caused by activating bottom TEC located at the same horizontal location (see Figure 9 for TEC locations) [126].

As expected, applying a current to a TEC causes a cooling effect to the hotspots below that TEC and a heating effect above that TEC. For example, if a 1.75 A current is applied to the top TEC it cools both the top and bottom hotspots (Figure 27, a & c). However, if a 1.75 A current is applied to the bottom TEC it cools the bottom hotspot

(Figure 27, b), but heats the top hotspot (Figure 27, d). It is important to ensure that the heating of the top hotspot is not too severe. In the case of the modeled electronic package, the bottom hotspot temperatures are much higher than the top hotspot temperatures, so cooling the bottom hotspots at the cost of heating the top hotspots is acceptable.

4.1.3 Unequal Power on Chips

In stacked chip architecture, it is possible to have different functionalities (e.g., logic, memory etc.) equivalently located on different dies which will lead to equal power dissipation on different stacked dies or chips. Alternatively, a die can be dedicated to memory and another die to logic leading to unequal power dissipation on different dies. From a thermal perspective, it is advantageous to place the higher power chip or die near the heat sink in order to reduce peak temperatures of the electronic package. We modeled the electronic package with the top chip having higher power. The bottom chip power was varied as a percentage of the top chip power while the top chip power was held constant. The current through all four TECs was set to either 0 A or 1.75 A, and hotspot temperatures were investigated. The results of this analysis are shown in Figure 28. If no current is applied to the TECs, bottom and top chip peak temperatures are equal when the bottom chip dissipates about 50% power of the top chip (arrow in Figure 28). If the applied current through all four TECs is 1.75 A, bottom and top chip peak temperatures are equal when the bottom chip power is about 70% of the top chip power (arrow in Figure 28). The TECs in stacked chip architecture can provide cooling necessary to increase bottom chip power.

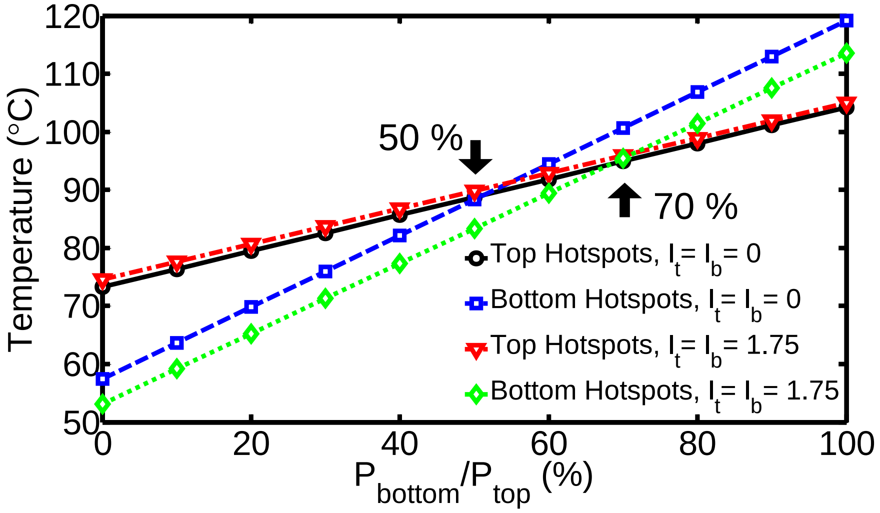

Figure 28: The top chip power is held constant and the power of the bottom chip is varied as a percentage of the top chip power. Same current is applied through all four TECs [126].

4.2 Effect of ERL and Thermal Contact Resistances

4.2.1 Effective Resistance Layer (ERL)

Different die bonding techniques in 3-D stacked chips has been investigated in previous studies [1, 78]. A thin (25μ) effective resistance layer (ERL) was considered between the top and bottom die (see Figure 9) in order to study how the thermal resistances of bonding materials and interfaces may affect the thermal performance of TECs. The thermal conductivity of the ERL was varied between 1 and 10 W/m-K and the current through all four TECs was set to 0 A or 1.75 A. The ERL conductivity had a negligible effect on the top hotspot temperatures (<0.3 °C). Figure 29 shows the results of this analysis for the bottom hotspot temperature. Changing the ERL conductivity from 1 to 10 W/m-K results in a 4.73 °C reduction of bottom hotspot temperature when all four TECs are inactive (0 A applied current) and a 6.72 °C reduction of bottom hotspot temperature when all four TECs are active with 1.75 A applied current. A majority of this cooling is observed as the ERL conductivity is changed from 1 to 5 W/m-K.

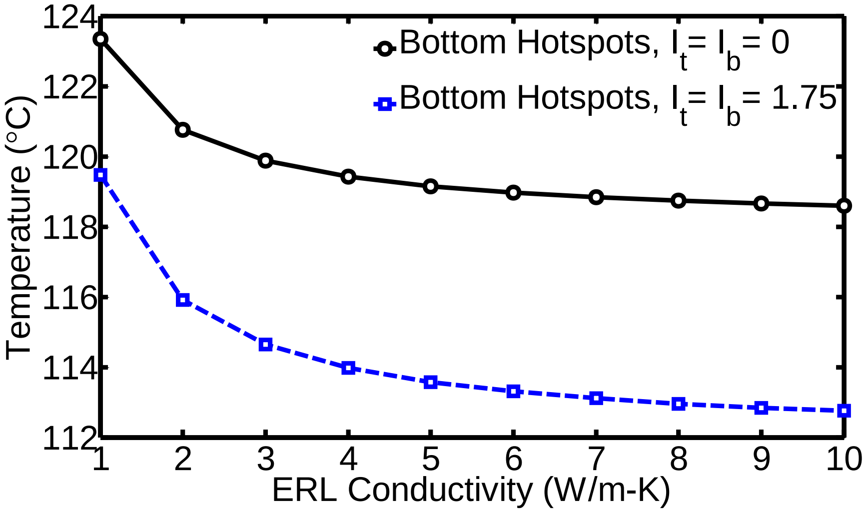

Figure 29: Bottom hotspot temperature with varying ERL conductivity. The applied current to all four TECs is the same [126].

4.2.2 Superlattice-Copper Contact Resistance

The superlattice-copper contact resistance inside a TEC module is dependent on the fabrication process. This contact resistance, R_c, is measured to be on the order of 1×10^{-6} m^2K/W in [14]. New technologies can reduce the contact resistance while fabrication defects can increase the contact resistance. In order to quantify these effects, the superlattice-copper contact resistance was varied by one order of magnitude higher and lower from the value reported in [14]. The current through all four TECs was set to 0 A or 1.75 A. The results of this analysis are shown in Figure 30. The superlattice-copper contact resistance, R_c, has a more dramatic effect on temperature at higher applied currents (1.75 A vs. 0 A). An increase in the contact resistance by one order of magnitude to 1×10^{-5} m^2K/W can result in 8 °C increase in the bottom hotspot temperature, but decreasing contact resistance by an order of magnitude to 1x10^{-7} m^2K/W results in only 1-2 °C decrease in hot spot temperature.

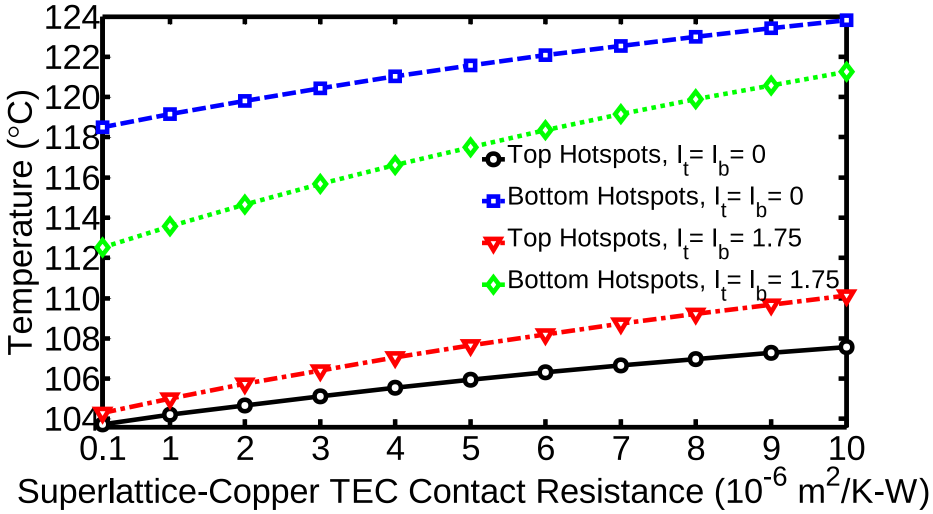

Figure 30: Bottom and top hotspot temperatures with varying superlattice-copper contact resistance. The current through all four TECs is set at 1.75 A or 0 A [126].

The Coefficient of Performance (COP) of the bottom and top TECs were also determined for two superlattice-copper thermal contact resistances at various applied currents. The COP for a TEC is defined as the difference in the amount of heat flux at the cold end of the TEC with and without an applied current divided by the power consumed by that TEC. The power consumed by a TEC consists of Joule heating (bulk and contacts) and the power required to create the Peltier cooling effect. The Joule heating power is a function of only electrical resistances and the current, but the power required to create the Peltier cooling effect is dependent on both electrical and thermal inputs, and is described by Equation 54.

$$P_{Peltier} = \alpha IN(T_h - T_c) \qquad (54)$$

In the equation, α is the Seebeck coefficient, I is the applied current, N is the number of thermoelectric elements, and T_h and T_c are the hot and cold junction temperatures. This calculation is explained in more detail in [50]. The electrical contact resistance of the superlattice-copper interface was held constant. An increase in the superlattice-copper thermal contact resistance from 1x10^{-6} m^2K/W to 1x10^{-5} m^2K/W resulted in decreased COP, shown in Figure 31. Furthermore, the top TECs had higher COP than the bottom TECs. This is likely because the top TECs are closer to the heat spreader than the bottom TECs and are better able to reject heat. Thermal resistance can have a crucial effect on COP.

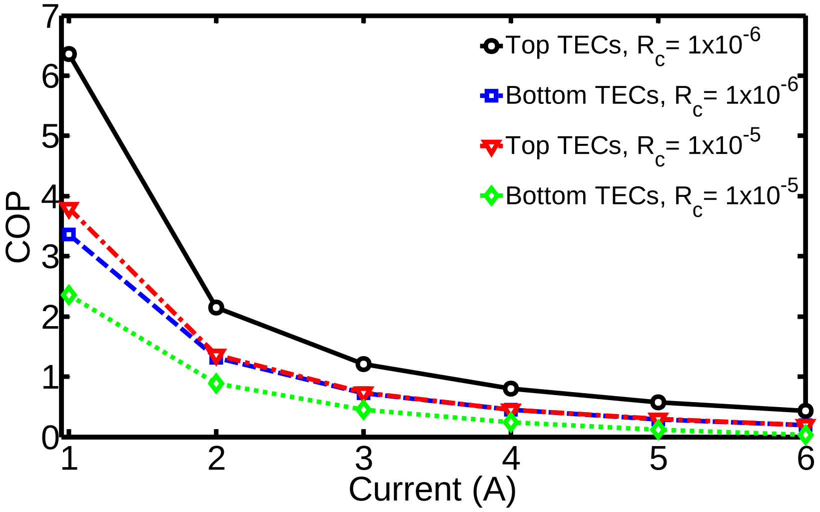

Figure 31: Bottom and Top TEC COPs with varying current. The superlattice-copper contact resistance is either 1x10-6 m^2K/W or 1x10^{-5} m^2K/W [126].

4.2.3 TEC-Spreader Contact Resistance

The TEC-spreader contact resistance can have a significant effect on the operation of TECs inside an electronic package. In order to quantify these effects, the TEC-spreader contact resistance was varied by one order of magnitude higher and lower from its value of 8x10^{-6} m^{2}K/W observed in [14]. The current through all four TECs was set to 0 or 1.75 A, respectively. The results of this analysis are shown in Figure 32. Similar to the superlattice-copper contact resistance, the TEC-spreader contact resistance has a more dramatic effect on temperature at higher applied currents (1.75 A vs. 0 A). Increasing the TEC-spreader contact resistance to 8x10^{-5} m^{2}K/W results in up to an 18.6 °C increase in bottom hotspot temperature. In addition, reducing the TEC-spreader contact resistance to 8x10^{-7} m^{2}K/W, can result in a 4.8 °C reduction in bottom hotspot temperature. Hotspot temperatures are observed to be more sensitive to the TEC-spreader contact resistance compared to the superlattice-copper contact resistance because the contact resistance at the TEC-spreader interface is higher. The contact resistance at the TEC-spreader interface can become so large, that it is better to keep the TECs off. Significant attention is deserved to find ways to reduce this contact resistance in order to effectively utilize TECs in stacked chips.

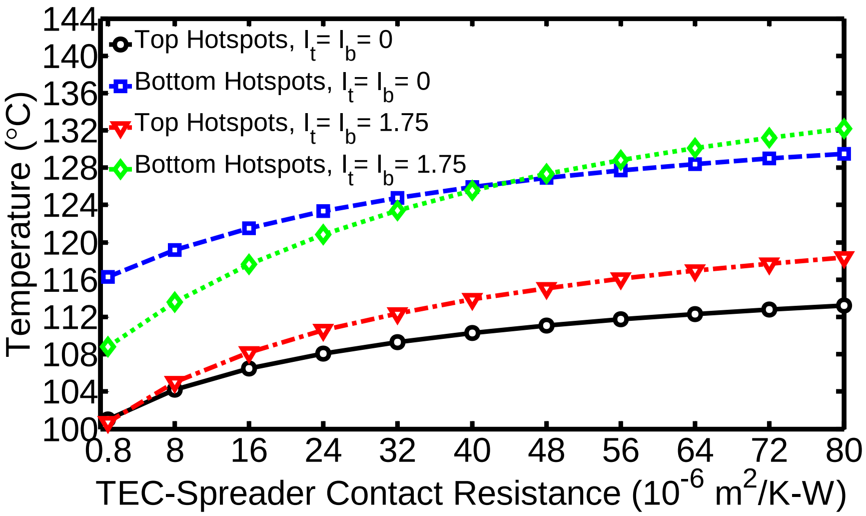

Figure 32: Bottom and top hotspot temperatures with varying TEC-spreader contact resistance. The current through all four TECs is set at 1.75 A or 0 A [126].

4.3 Transient Pulse Analysis

4.3.1 Transient Cooling with Step Input Currents

A transient current pulse through a TEC has been shown to provide cooling to a greater extent than the steady state cooling by a TEC [68, 72-74]. The steady state temperature distribution of the electronic package with zero current through the TECs was used as an initial state for this analysis. A time step of 0.002 s was used for the initial transient simulations. It is observed that the application of the same current magnitude to all four TECs leads to cooling in the bottom hotspots, but heating at the top hot spots. This top hotspot heating is prohibitive (>2 °C) when large currents are applied to bottom TECs, even though these large current pulses can lead to a high degree of cooling at the bottom hotspots. Larger applied currents produce a faster response than smaller currents, but are accompanied by Joule heating resulting in a large temperature overshoot after the minima in temperature is achieved. The temperature minimum at the bottom hotspots occurs between 0.05 and 0.1 seconds depending on the magnitude of the applied current. A fast response time is desirable for transient cooling of hotspots because hotspots can appear and disappear on the order of milliseconds.

In an effort to find TEC current amplitudes appropriate for use in this model, two measures were defined to quantify the suitability of the current magnitude used in cooling. The amount of cooling at bottom hotspots that occurs 0.05 s after the application of a step input current was used to quantify the degree of cooling that occurs quickly enough to be useful in transient heat removal from an electronic package. The maximum amount of heating at the top hotspots within 0.05 s after applying a step current in TECs quantified the negative effects the TECs may have on the top hotspots. The objective here was to find the maximum cooling of the bottom hotspot while preventing top hotspot heating of more than 2 °C. With these objectives, the transient performance of TECs in the electronic package was modeled using current amplitudes between 2 and 4 A on the bottom TECs while the current amplitude of the top TEC were varied between 2 and 10 A. The two measures previously defined were used to quantify the results. The maximum heating that occurs at the top hotspots within the first 0.05 s is shown in Figure 33a. The cooling at the bottom hotspots at 0.05 s is shown in Figure 33b. Based on the criterion described above, a bottom TEC current of 3 A and a top TEC current of 8 A provides the maximum bottom hotspot cooling and limits top hotspot heating to under 2 °C. These current amplitudes are used in the pulse shape analysis in the next section.

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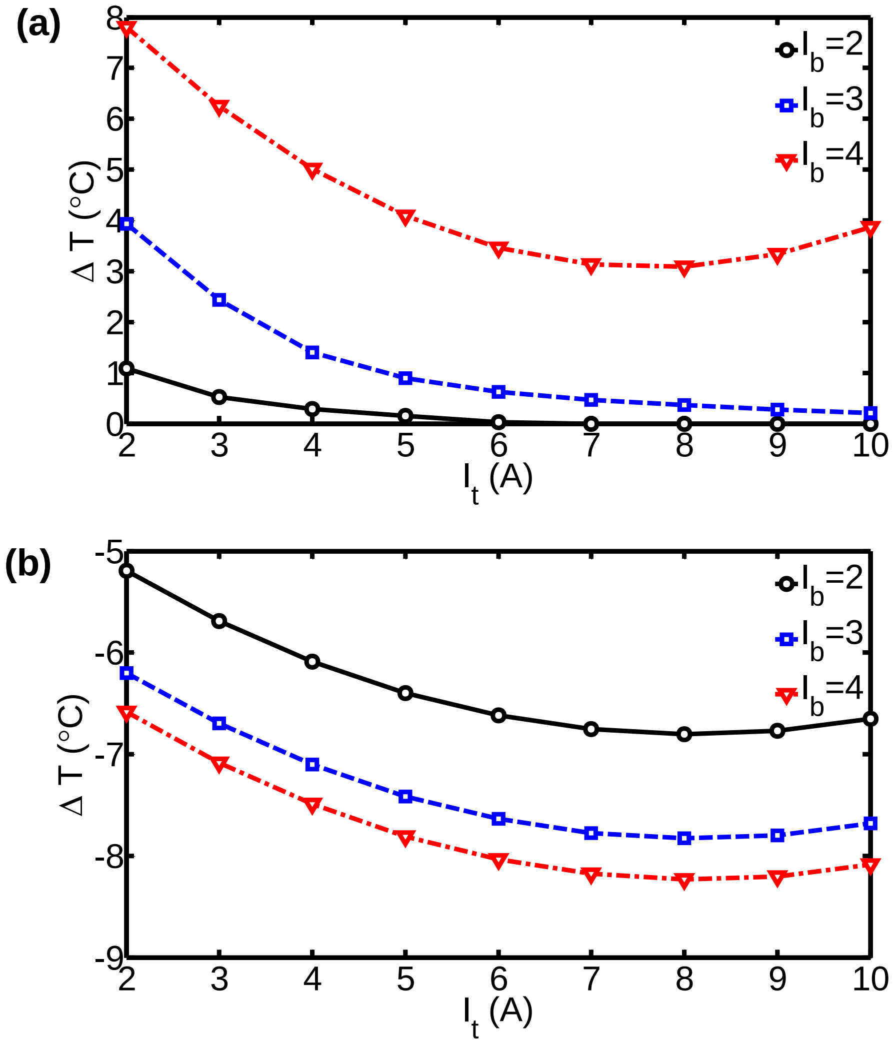

Figure 33: The bottom TEC current (I_b) is varied between 2 and 4 A, while the top TEC current (I_t) is varied between 2 and 10 A.(a) Maximum heating on the top hotspots within the first 0.05 s. (b) Cooling on the bottom hotspots at 0.05 s [126].

4.3.2 Pulse Shape Investigation

Using a top TEC current amplitude of 8 A and a bottom TEC current amplitude of 3 A, various current pulse shapes of duration 0.05 s were investigated for use in bottom chip cooling. In this analysis, a time step of $2\text{x}10^{-4}$ s was used to calculate the hotspot temperature profiles. This time step is one order of magnitude smaller than that used in the previous section. The pulse shapes under consideration were: constant (t^0), linear (t^1), quadratic (t^2), and square root ($t^{1/2}$). These pulse shapes have been discussed in detail in [74].

The results of this investigation are shown in Figure 34. The constant current pulse provided the maximum cooling at the bottom hotspot with a 7.9 °C temperature drop at 0.05 s. The square root pulse provided a slightly smaller (~7.4 °C) temperature drop (Figure 34b). None of the current pulses produced a significant amount of heating on the top hotspot, although it should be noted that the constant current pulse is the only pulse that causes a temperature spike (< 1 °C) at the top hotspot just after the application of current pulse, (Figure 34a). This temperature spike is similar to that observed by the constant current step inputs applied in the previous section.

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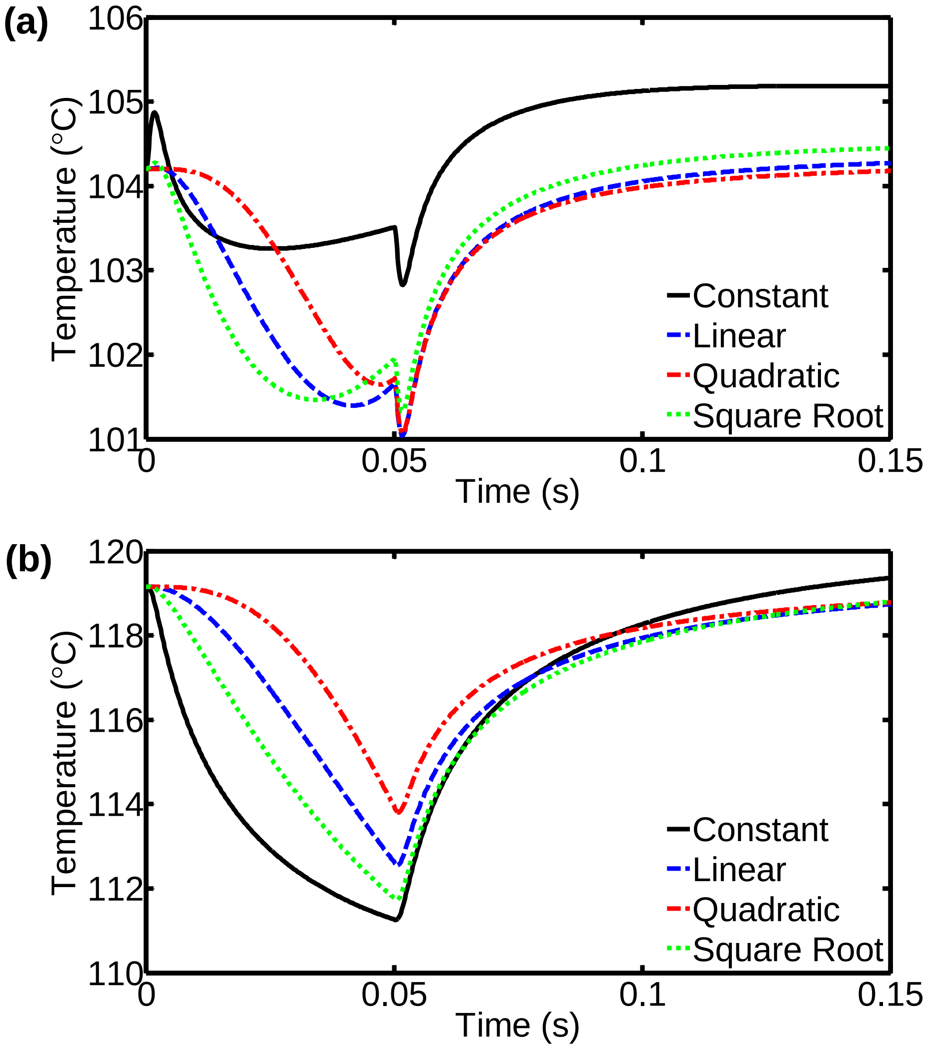

Figure 34: Hotspot temperature as a function of time with a 0.05 s duration and 8 A pulse applied to the top TEC simultaneously with a 0.05 s duration and 3 A pulse applied to the bottom TEC. Both pulses have the same shape. (a) Temperature of the top hotspot. (b) Temperature of the bottom hotspot [126].

Interesting behavior is observed for the top hotspot temperatures for all pulse shapes. During the first 0.05 s period, the top hotspot temperature first decreases due to Peltier cooling at the surface, and then begins to rise due to Joule heating within the TECs. This is due to the shorter response time of the Peltier cooling surface effect compared to Joule heating within the TECs. However, when the TECs become inactive at 0.05 s, a temperature drop ensues as the temperature at the bottom TEC hot side instantly decreases because the Peltier effect is removed. This temporary temperature drop quickly disappears, and a temperature overshoot above the initial temperature appears, as expected. The overshoot is greatest for the constant current pulse (Figure 34a).

The coefficient of performance (COP) of TECs is typically low, especially at large current amplitudes, and energy consumption throughout the current pulse needs to be carefully considered. A constant current pulse produces 50 % more Joule heating than a square root pulse of the same amplitude [74], but the maximum degree of cooling is nearly the same for these two pulses. This energy saving quality of square root pulses in particular, combined with their similar performance to constant current pulses, reduced top hotspot heating and reduced overshoot make them a good choice for hotspot thermal management of stacked chips.

4.4 Optimization of TE Material Thickness and Current Magnitude

An optimization of the TE material thickness and current magnitude was performed using Comsol. Four independent variables were optimized: top TEC current (I_t), bottom TEC current (I_b), top TE material thickness (l_t), and bottom TE material thickness (l_b). Two different optimizations were performed, each with a unique objective. In the first optimization, the objective was to minimize the maximum temperature occurring at any point in the computational domain. This maximum temperature always occurred on either the top or bottom hotspot. In the second optimization, a combined temperature and power optimization was performed using the active cooling divided by the energy consumption of the TECs as the objective function. Active cooling was defined as the decrease in the maximum temperature beyond that achievable with 100 μm copper blocks which corresponds to replacing the TECs by passive thermal vias.

Constraints were imposed on the optimization problem in order to ensure that results were physically realistic and to reduce the size of the solution space. The current through the TECs was limited to between 0 and 3 A because extremely large currents are difficult to supply to TECs. The thickness of the top and bottom TECs was constrained by a lower limit of 0 μm and an upper limit of 50 μm. Even though the total TEC thickness is 100 μm, it is expected that about 25 μm copper on each side of the TEC would be necessary for structural integrity and to aid in the fabrication of the device. A special case of this four variable optimization occurs when the thickness of the top TECs is equal to zero. In this case, the top TECs were effectively replaced with 100 μm copper blocks and the bottom TECs can be optimized for two variables alone: bottom TEC current (I_b), and bottom TE material thickness (l_b). .

The desired resolution for the optimum operating current was 0.05 A and 1 μm for the TE material thickness. With these resolutions, the top and bottom TEC optimization geometry (4 independent variables) has 9 million possible combinations, but the case when the thickness of the top TECs equals zero only has 3000 combinations. This special case (bottom TECs only) serves as a useful tool for determining an appropriate optimization method for use on the geometry containing both top and bottom TECs because a parametric sweep can be performed to find the true optimum at the desired resolution. This is then compared to the results of the gradient descent and Luus-Jaakola methods. A summary of the optimizations performed is shown in Table 6. A total of two objective functions (Maximum Temperature and Active Cooling/Power), two geometries (Bottom TECs only and Top and Bottom TECs), and three optimization methods (Parametric Sweep, Gradient Descent, and Luus-Jaakola) were used. Of all the possible combinations, the only one not performed was using the parametric sweep optimization for the Top and Bottom TECs geometry.

Table 6: Summary of the optimizations performed.

	Bottom TECs Only		Top and Bottom TECs	
	Maximum Temperature	Active Cooling/Power	Maximum Temperature	Active Cooling/Power
Parametric Sweep	Yes	Yes	No	No
Gradient Descent	Yes	Yes	Yes	Yes
Luus-Jaakola	Yes	Yes	Yes	Yes

4.4.1 Bottom TEC Only Optimization

For the special case where the thickness of the top TE material thickness is equal to zero, the gradient descent method, Luus-Jaakola direct search method, and a parametric sweep of the solution space were all used to optimize the variables according to both objective functions. In the gradient descent method, the initial guess was 1.75 A and 8 μm for current and TE material thickness, respectively, because these values were used extensively in Sections 4.1 and 4.2. From this starting point, the partial derivative of the objective function with respect to each independent variable was calculated and the independent variables were subsequently changed by taking steps in the direction of the negative gradient of the objective function until a minima was reached. For the Luus-Jaakola method, the solution space was sampled with a total of 25 points (5 in each dimension). The solution space dimensions were reduced in size by 33% in each direction and centered on the extrema found in the previous step. This process was repeated until the specified resolution was achieved. The parametric sweep used the same resolution to sweep the solution space in search of an extrema.

The first of two optimizations for the model was the temperature-only optimization. Results from each of the three methods were obtained and are shown with a maximum temperature contour plot in Figure 35. Out of all three methods, the lowest maximum temperature was found to be 106.14 °C with a bottom TEC current of 1.18 A and a bottom TEC thickness of 38.8 μm by the Luus-Jaakola method. Even though the independent variables determined to be optimum by all three methods were quite different, the maximum temperature in all three solutions is similar. This is because the lowest maximum temperature occurs along a long, thin region, represented by a dashed curve in Figure 35. This agrees with expected behavior since the objective was to minimize the maximum temperature of the package, which occurs when the top and bottom hotspots are equal in temperature. A parametric sweep of the solution space revealed that the bottom and top hotspot temperatures can be represented by two smooth surfaces which intersect each other. The objective function is the maximum of these two surfaces, and is non-differentiable at the surfaces' intersection. This intersection is shown in Figure 36. This gives insight as to why the gradient descent method gave the least accurate optimization, since the gradient was discontinuous in the region of the lowest maximum temperature.

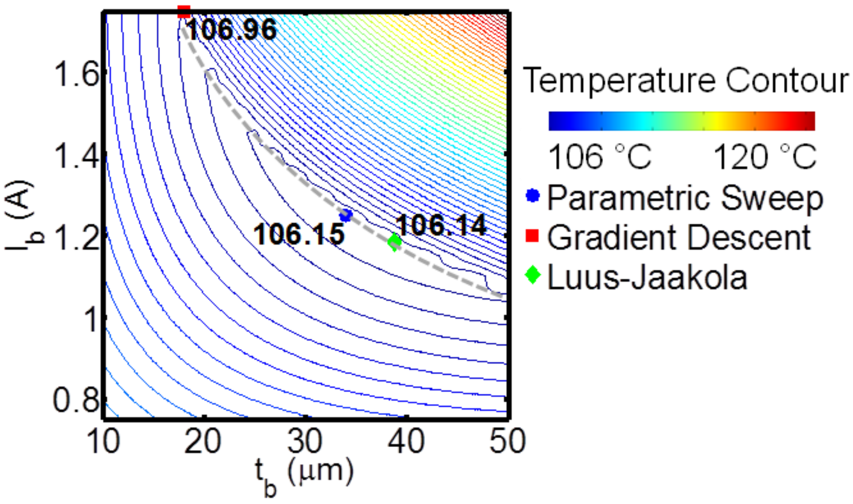

Figure 35: Contour plot of objective function (maximum temperature) for the temperature only optimization. Maximum temperature (ºC) for the optimum point found by the gradient descent method, Luus-Jaakola method, and parametric sweep have been indicated. The dashed line represents the long thin region where the lowest maximum temperature occurs.

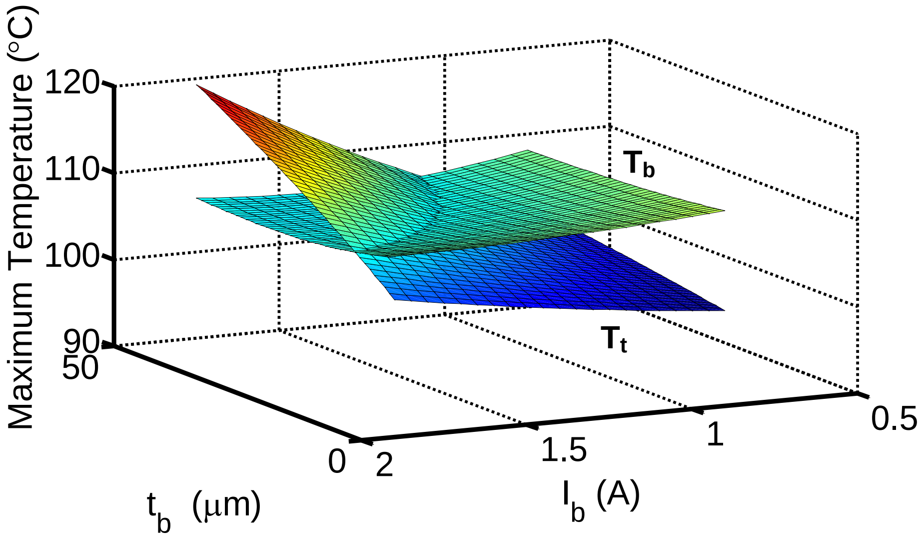

Figure 36: Intersection of the top and bottom hotspot temperatures in the region of the optimum solution.

The second of the two optimizations performed for the model was to maximize the active cooling divided by power consumption. In this optimization, the results obtained by the gradient descent method, Luus-Jaakola method, and parametric sweep were all within the study's resolution of 0.05 A and 1 μm of one another. The optimum points, along with a contour plot of the objective function, are shown in Figure 37. In this region, the temperature of the top hotspot is cooler than the temperature of the bottom hotspot, creating a smooth objective function. Since the gradient is continuous, both the gradient descent and Luus-Jaakola methods achieve similar accuracy.

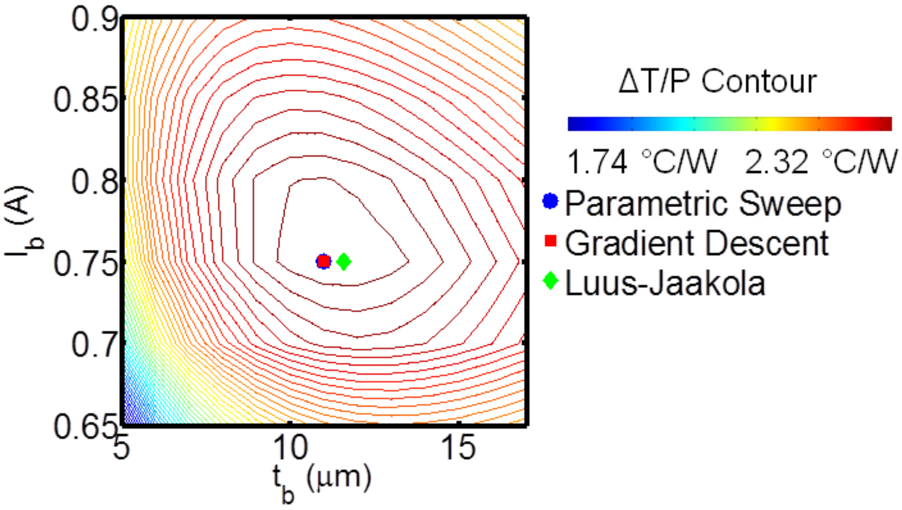

Figure 37: Contour plot of the objective function (active cooling divided by power consumption). Optimum points found by the gradient descent method, Luus-Jaakola method, and parametric sweep have been indicated.

4.4.2 Top and Bottom TEC Optimization

The first optimization, which considered only temperature, cannot be solved using a parametric sweep for the model considering both the bottom and the top TECs because the solution space is so large. Furthermore, the gradient descent method is expected to yield an inaccurate optimization result due to the discontinuous derivative found when the top and bottom hotspots are equal, as discussed in the previous section. As a result, the Luus-Jaakola method was used for the temperature only optimization considering both the top and the bottom TECs.

In order to give more confidence in the optimization, the Luus-Jaakola method is used twice with two different criteria. In the first (Criterion A), a total of 625 points are sampled in the solution space (5 in each direction), and the solution space dimensions are decreased by 33% in each iteration. In the second (Criterion B), a total of 256 points are sampled in the solution space (4 in each direction), and the solution space dimensions are decreased by 25% in each iteration.

Both sets of criterion produced very similar optimization results, even though the path to the solution for each criterion was quite different. The path to solution along with the result for each criterion is shown in Figure 38. Since both optimizations yielded similar results, there is a great deal of confidence in the robustness of this solution. The minimum temperature that can be achieved is found to be 108.08 °C using 6.27 W of cooling power.

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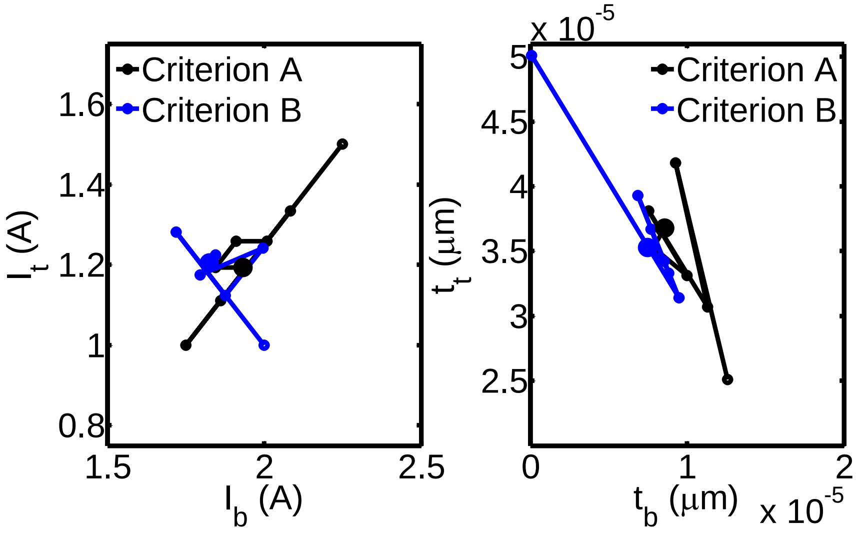

Figure 38: The temperature only optimization path for the Luus-Jaakola method using two different criteria. The similar results with different criteria and solution paths gives confidence in the robustness of this solution. The small circles represent intermediate steps and the large circles represent the optimum.

For the second optimization, considering both cooling and power consumption, the gradient descent method can be utilized. Both the gradient descent method and the Luus-Jaakola methods indicate that the optimum TE material thickness of the top TEC approaches 0 μm. This solution represents the special case discussed in the previous Section 4.4.1.

4.4.3 Comparison and Discussion of the Optimization Results

The results of the optimizations performed are compared and summarized in Figure 39. Using a copper block in place of the top TEC reduced the maximum chip temperature, and increased the heat pumping capacity of the bottom TEC. This result suggests that using TECs on each layer of a stacked chip can actually be detrimental for chip performance. This holds true when considering both maximum cooling and energy efficient cooling. TECs should be used primarily to cool only the hottest portion of a package, which would be the bottom chip in a stacked chip package. It is expected that as the number of chips in the package increases past two, this trend will not change.

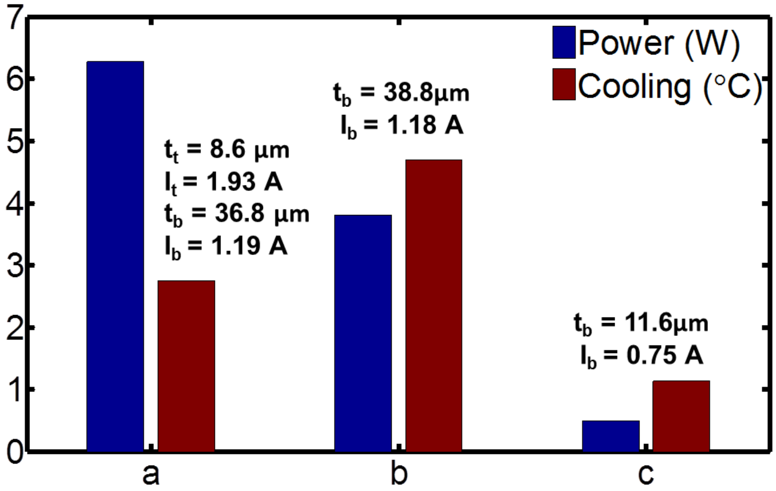

Figure 39: Cooling and power consumption achieved in comparison to using 100 μm thick copper blocks in place of all four TECs. The optimums are labeled with the independent variables which produce them (a) Temperature-only optimization with TECs on the top and bottom. (b) Temperature-only optimization with copper blocks on the top chip and TECs on the bottom chip. (c) Combined temperature and power consumption optimization with copper blocks on the top chip and TECs on the bottom chip.

4.5 Summary

This numerical analysis suggests that TECs can be used for on demand cooling of hotspots in 3-D stacked chip architecture. A strong vertical coupling is observed between the top and bottom TECs and it is found that the bottom TECs can detrimentally heat the top hotspots. As a result, TECs need to be carefully placed inside the package to avoid such undesired heating. Thermal contact resistances between dies, inside the TEC module, and between the TEC and heat spreader are shown to have a crucial effect on the TEC performance. The use of transient cooling and copper blocks as thermal vias can further improve both the thermal performance and energy consumption of TECs.

CHAPTER 5

HIGH HEAT FLUX REMOVAL USING MICROCHANNELS

In this chapter, the results of hydrodynamic and heat transfer experiments on microchannels are presented and compared to previous empirical results. This study is one of the first experimental studies on microchannels with more than three heat transfer walls, as most microchannel experiments have one insulated wall. The experimental results are also compared to theory and the developed computational models for microchannels. Possible sources of error are explored through an experimental uncertainty analysis and a sensitivity study. The sensitivity study yields new insight about the fabrication method used and provides guidance for future experimental studies. Finally, the accuracy and computational expense of an empirical correlation based modeling method for heat transfer in microchannels is compared to existing models which are widely used in the literature.

5.1 Experimental Fluid Flow and Heat Transfer in Microchannels

5.1.1 Pressure Drop

Experiments were performed, as described in Section 3.2.2. The pressure drop was measured across the microchannel setup and the friction factor, corrected for sudden contraction and expansion, was calculated as described in Section 3.2.3. The measured friction factor is compared to the theoretical friction factor for fully developed flow, and the results are shown in Figure 40. It is reasonable to neglect the additional pressure drop caused by the flow development because the maximum hydrodynamic entry length encompasses only 2.7 % of the microchannel length in these experiments. The experimentally observed pressure drop is in good agreement with theory, especially when variations in channel width and height are considered. The experimental uncertainty in measured friction factor is 10.4 %, as determined in Appendix B.

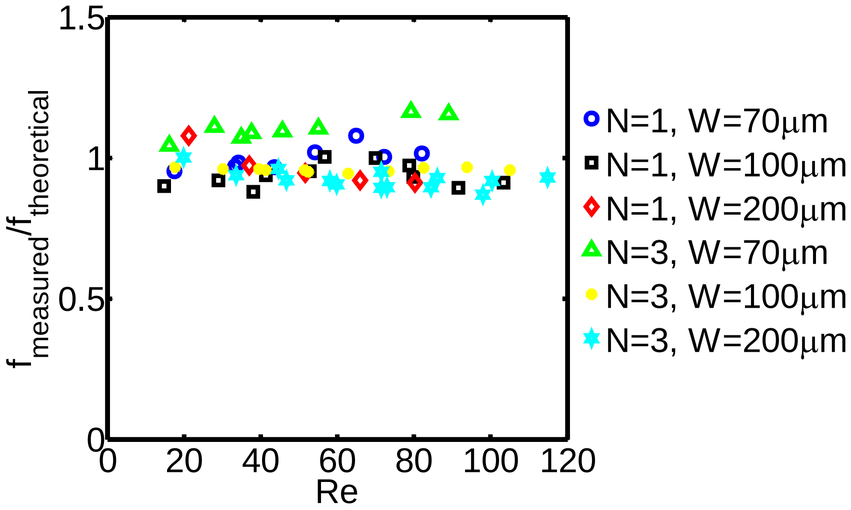

Figure 40: The measured friction factor compared against the theoretical friction factor for fully developed flow. The experimentally observed pressure drop is in good agreement with theory when variations in channel dimensions are considered.

5.1.2 Nusselt Number

Experiments were performed according the experimental procedure described in Section 3.2.3. The Nusselt numbers in the microchannels were measured for a variety of flow rates and microchannel dimensions as shown in Figure 41. A trend of increasing Nusselt number as a function of Reynolds number is apparent, which is similar to what has been observed in much of the previous literature for microchannels [104-106].

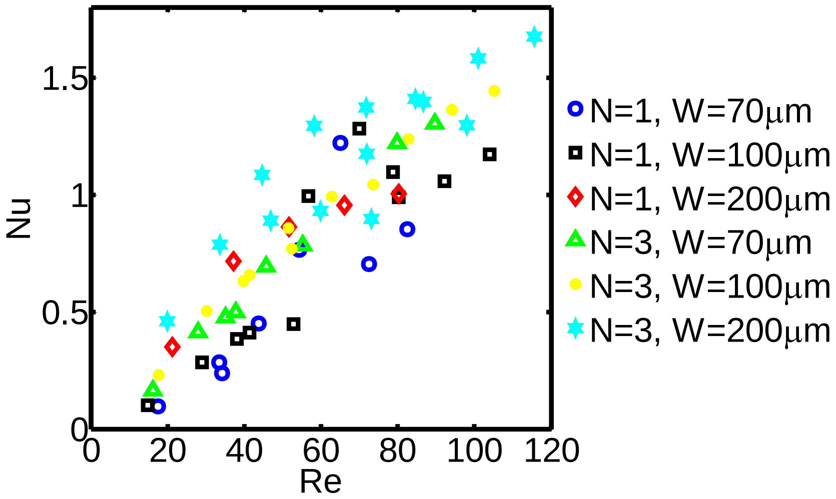

Figure 41: Experimentally measured Nusselt number for a variety of flow rates and microchannel dimensions.

The data from the present experiments can be compared to the experimental correlations for Nusselt number from the previous experiments [103-106]. The Nusselt number predicted by the previous empirical correlations is plotted along with data from the present experiment in Figure 42. This is done for each data point in the present experiments because some of the predictions from previous correlations do not follow a linear trend line. When calculating the Nusselt number based on previous empirical correlations, input parameters were obtained in the manner described in the particular study. For example, if a study used the inlet water temperature to calculate the Reynolds number for a correlation, then the inlet Reynolds number was used in the correlation to determine the corresponding Nusselt number, even though the average water temperature was used to calculate the Reynolds number in the present study.

It should be noted that the Nusselt number reported in [105] was calculated using the base area of the microchannels rather than the wall area. Their correlation has been modified in order to represent the wall area for a more appropriate comparison and is included in Figure 42 and marked as "[105] modified." Another point of interest is the extremely low values of Nusselt number predicted by the correlation reported in [104]. It is suspected that this correlation contains an error, but the exact nature of this error is unknown.

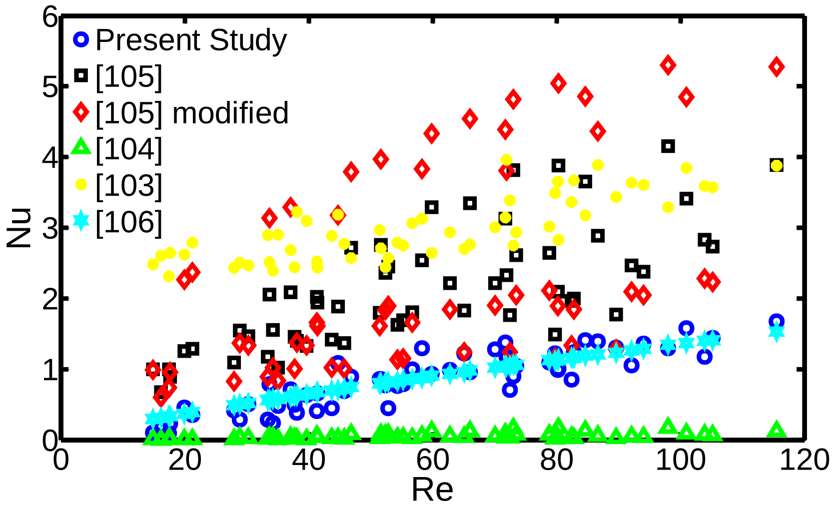

Figure 42: Comparison of experimental Nusselt number results from the present experiment compared to the empirical correlations from the previous work.

From this figure, it is clear that the order of magnitude of the measured Nusselt number in this experiment is similar in magnitude to the previous work, but there is a large degree of discrepancy in the literature. Some of this discrepancy may be due to the different methods which were used to calculate Nusselt number in these experiments. This was previously discussed in detail in Section 3.2.3 of this work.

Additionally, variation may be due to the different boundary conditions assumed by the researchers. The boundary condition in axial direction in these experiments was maintained as a constant heat flux for all the experiments except [104], where a constant temperature was assumed. Furthermore, the circumferential boundary condition was considered constant temperature by some [104], constant heat flux by others [105, 106], and a method to integrate the fin equation to account for non-uniform temperature and heat flux boundaries was employed by [103]. In the present work, the circumferential boundary condition is considered as a constant temperature boundary condition due to the high fin efficiency, which has been shown to be approximately correct by the computational results presented in Section 5.3.3.

Another important difference between the previous experiments is the hydrodynamic and thermal entrance length in the experiments. These entry lengths are commonly approximated using Equations 55 and 56 [110, 135, 137].

$$x_{fd,h} = 0.1ReD_h \tag{55}$$

$$x_{fd,t} = 0.1ReD_hPr \tag{56}$$

In these equations, Re is Reynolds number D_h is the hydraulic diameter, and Pr is the Prandtl number. It is important to note that the exact point at which a flow becomes fully developed is difficult to define; as a result these expressions are approximate. The key distinction is whether the developing flow becomes “fully developed” when it is within 5%, 1%, or even 0.1% of what is theoretically expected of developing flow. The thermal entry length described by Equation 53 corresponds to when the local Nusselt number is within 5% of the fully developed value. Equations 55 and 56 tend to be more conservative (i.e., longer entry lengths and a smaller percent error) than Equation 53.

The average hydrodynamic and thermal entry length as a percentage of the total microchannel length is shown for each experiment in Table 7. The present experiment and the experiment by Koyuncuoglu, *et al.* are the only experiments which measured the

Nusselt number in the fully developed region. The other experiments measured the Nusselt number in the developing region.

Table 7: Average hydrodynamic and thermal entry length as a percentage of the total microchannel length for the present and prior experiments.

	Hydrodynamic Entry Length, $x_{fd,h}/L$	**Thermal Entry Length, $x_{fd,t}/L$**
Present Work	1.9%	11.1%
Peng and Peterson, 1996 [105]	14.6%	102.0%
Jeung and Kwak, 2008 [104]	11.6%	81.4%
Park and Punch, 2008 [103]	67.6%	472.9%
Koyuncuoglu, *et al.*, 2012 [106]	3.2%	20.6%

Finally, axial heat conduction in the substrate is likely to have played a role in the variation of results. Axial heat conduction has been shown to cause the Nusselt number in a microchannel to increase as a function of Reynolds number [114, 122]. The substrates used for most of the previous experiments was highly conductive silicon or stainless steel [103-105], unlike the substrate used in the present work and [106]. The possible effects of axial heat conduction are examined in detail for the present work. In order to do this, the axial heat conduction number, M, is used.

A plot of all the obtained experimental data points with $M < 0.015$ is shown in Figure 43. This represents experimental data points where axial heat conduction is unlikely to significantly influence experimental results, since axial heat conduction can be neglected for $M < 0.01$ [114, 122]. The increase in Nusselt number as a function of Reynolds number is not as pronounced in this plot (Figure 43) as for the entire experimental data set (Figure 41). This is likely because lower Nusselt numbers are obtained when axial heat conduction is significant [113, 114, 122].

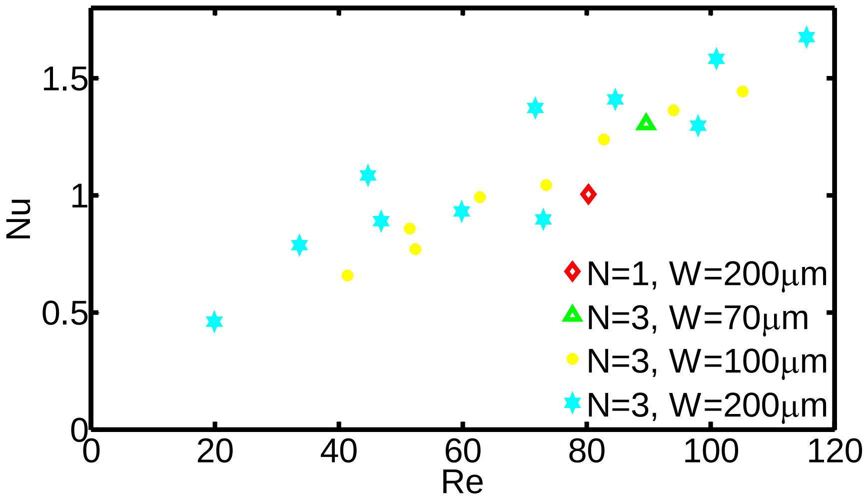

Figure 43: Measured Nusselt number vs. Reynolds number for axial heat conduction number M < 0.015.

5.1.3 Maximum Heat Removal

After the Nusselt number and pressure drop experiments were completed for a microchannel chip, the chip was tested to remove the maximum heat flux possible. Most of the chips could have removed a higher heat flux if the flow rate was increased. This is because at a higher flow rate, the maximum chip temperature would be reduced. However, the pressure drop was limited to 75 kPa in order to keep the experimental setup in a safe operating range. The maximum heat flux removal rates, pressure drop, pumping power, and the heat loss for the maximum heat flux removal experiments are shown in Table 8. The channels with a larger width are able to remove a higher heat flux with the pressure drop limited to below 75 kPa than those with a smaller width. Also, it is interesting to note that the chips with a single channel and with small channel dimensions have a higher heat loss than those for multiple channels and larger channel dimensions. This is most likely because at lower mass flow rates, the outlet water loses enthalpy between the channel outlet and the outlet thermocouples. A comparison of these results compared to previous heat removal rates is given in [142].

Table 8: Maximum microchannel heat removal rates.

Number of Channels	**W (um)**	**H (um)**	**Maximum Heat Flux Removed (W/cm^2)**	**Pressure Drop (kPa)**	**Pumping Power (mW)**	**Total Heat Loss**
1	70	50	41.23	77.44	0.28	44.7%
3	70	50	66.47	72.91	0.73	25.1%
1	100	50	81.04	71.28	0.45	36.9%
3	100	50	92.65	74.11	1.48	16.7%
1	200	50	134.73	76.39	1.27	25.5%
3	200	50	143.36	72.92	4.01	12.8%

5.2 Comparison of Experimental and Computational Results

The experimentally obtained temperature profile of three channel devices were compared to the profiles obtained by Comsol based CFD simulations which is described previously in Section 3.2.4. The experimental and computational pressure drops for the various microchannel geometries are compared in Table 9. The uncertainty in experimental pressure drop is 3.2%, as discussed in Appendix B. Minor discrepancies in results may be due in part to the mesh size of the model, as the pressure drop in computational model varied by about 3% based on the tests described in Section 3.2.4.

Table 9: Comparison of experimental and fully coupled CFD pressure drop.

	Experimental Pressure Drop (kPa)	**CFD pressure drop (kPa)**
3 channel, 70 μm wide channels	67.96	60.00
3 channel, 100 μm wide channels	69.27	70.79
3 channel, 200 μm wide channels	36.77	39.48

The axial temperature distribution in the heaters of the microchannel devices are compared to the computational results is shown in Figures 44-46. The experimental uncertainty in temperature was about 1 °C, as discussed in Appendix B. It is clear that the CFD results are not within the experimental uncertainty in temperature, suggesting that either the CFD simulations do not include all the relevant thermal resistances, the experimental dimensions have more uncertainty than expected, or the experiments were improperly conducted. A sensitivity analysis to help identify possible causes of uncertainty is included in Section 5.3.

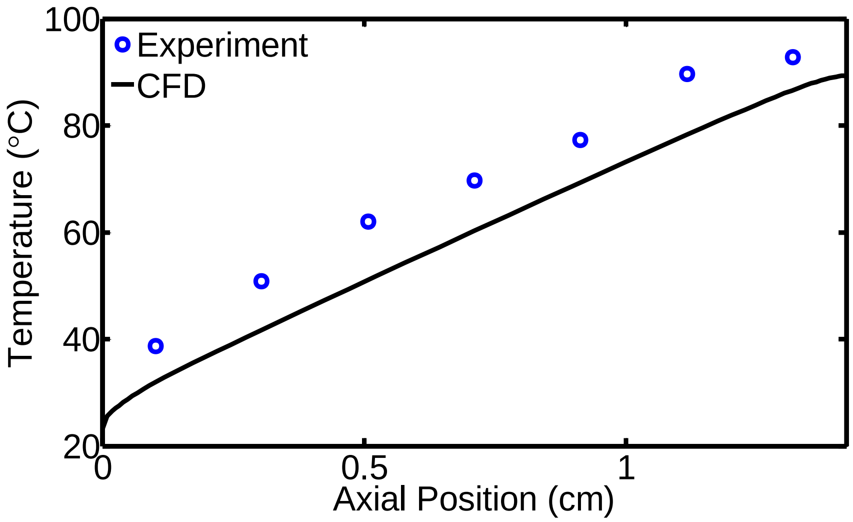

Figure 44: Comparison of axial heater temperature from experiment to a fully coupled CFD simulation for a three channel device of 70 μm wide channels.

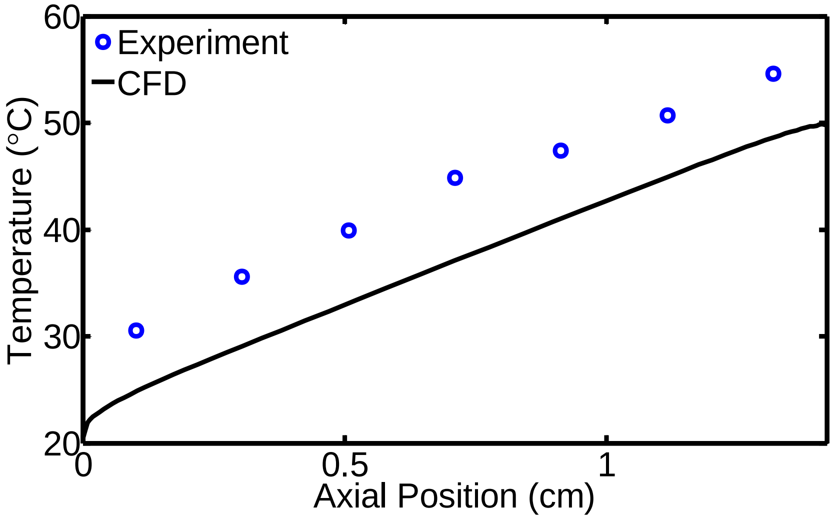

Figure 45: Comparison of axial heater temperature from experiment to a fully coupled CFD simulation for a three channel device of 100 μm wide channels.

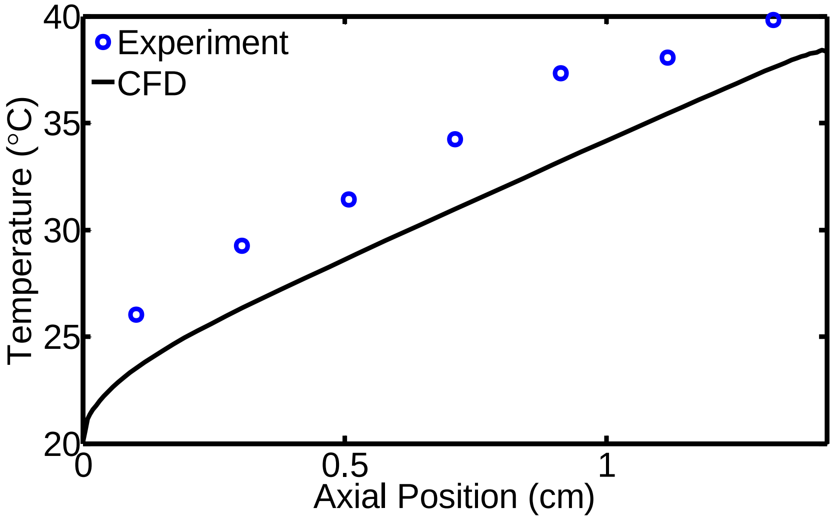

Figure 46: Comparison of axial heater temperature from experiment to a fully coupled CFD simulation for a three channel device of 200 μm wide channels.

5.3 Sensitivity Analysis

A sensitivity analysis was conducted to determine if uncertainties in microchannel dimensions or unidentified thermal contact resistances could be the cause of the discrepancy between the experimental and computational results. The device with three channelsand100 μm channel width was used for this sensitivity analysis. It was determined that the channel height, channel width, and parylene thickness between the heater and microchannels had a negligible effect on heater temperature within their expected uncertainty. To determine this, the channel height and width were both varied by ±4 μm, and the parylene thickness between the heater and microchannels was varied by ±0.2 μm. The variation of parylene thickness was taken as two times its expected uncertainty since the parylene thickness was measured to an uncertainty of ±0.1 μm.

In addition, the effect of tapered channel walls was considered and determined to be negligible. It is possible that the channel walls could have a smaller base due to the photoresist exposure and the electroplating process. This means that the walls and channels would have a trapezoidal cross section with the channel bottom being larger than 100 μm, and the channel walls being smaller than 20 μm. In this exercise, the channel bottom width was varied from 100 – 115 μm and the channel wall base width was varied from 20 – 5 μm. All the cross sectional geometry changes considered in this work assumed that the geometry remained constant in the axial channel direction.

In summary, the parameters that could have a significant effect on the heater temperature include the thermal contact resistance at the parylene-Ti interface, gap size, and the thickness of the gold layer.

5.3.1 Thermal Interface Resistance at the Parylene-Ti heater interface

Of the parameters considered, the thermal contact resistance at the parylene interface is most likely to influence the experimental results. There is a thin, 0.45 μm layer of parylene electrically isolating the Ti heaters from the Au electroplating seed layer. A thermal interface resistance exists at the interface of polymers and metals due to lattice vibration mismatch in the materials. Furthermore, perfect bonding is unlikely because delamination between parylene and other materials during MEMS processing is known to be a serious problem [143]. It is plausible that delamination could have occurred in the microchannel devices, introducing significant contact resistances. A parametric study of the effect of a thermal resistance at the interface of the Ti heater and parylene was performed for values between 1 x 10^{-7} and 5 x 10^{-5} m^2K/W for three different three channel devices with 70, 100, and 200 μm channel widths. These high thermal resistances correspond to the thermal resistance caused by delamination. The results, shown in Figures 47-49, indicate that introducing a thermal interface resistance of approximately 2 x 10^{-5} m^2K/W to the CFD model produces a good match to the experimental results for axial heater temperature.

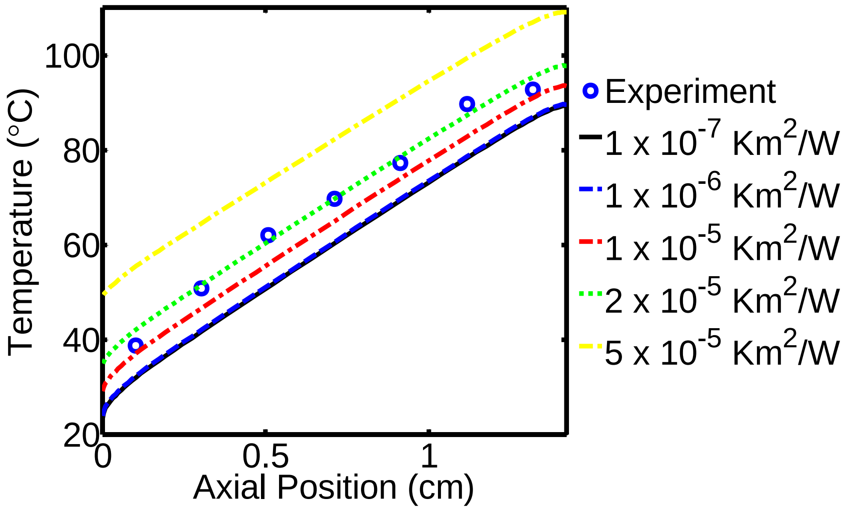

Figure 47: Comparison of axial heater temperature from experiment to a fully coupled CFD simulation for a variety of thermal contact resistances between the Ti heater and parylene layer for a three channel device of 70 μm wide channels.

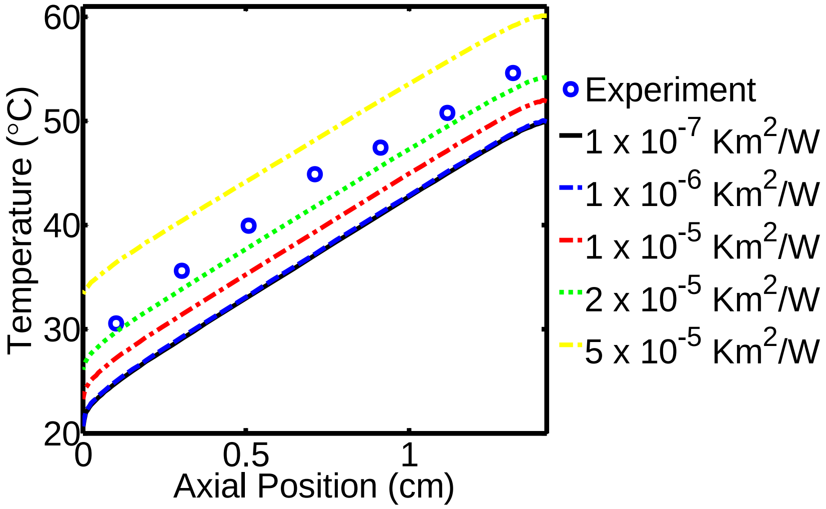

Figure 48: Comparison of axial heater temperature from experiment to a fully coupled CFD simulation for a variety of thermal contact resistances between the Ti heater and parylene layer for a three channel device of 100 μm wide channels.

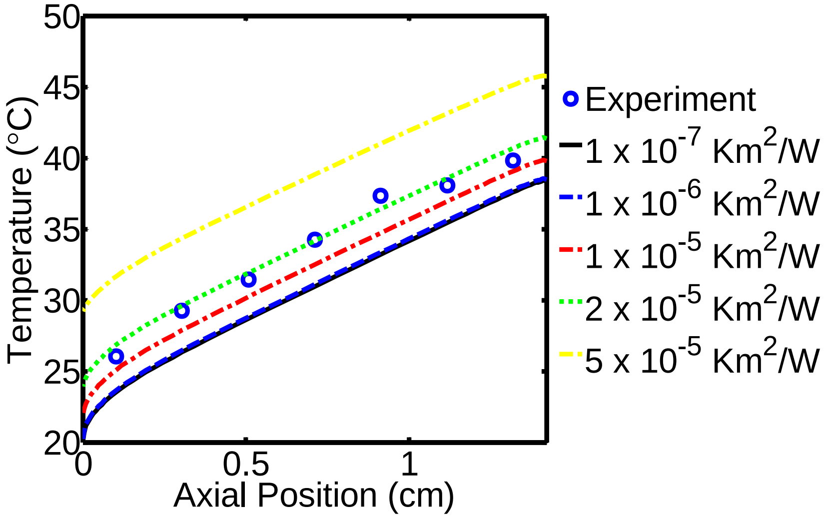

Figure 49: Comparison of axial heater temperature from experiment to a fully coupled CFD simulation for a variety of thermal contact resistances between the Ti heater and parylene layer for a three channel device of 200 μm wide channels.

5.3.2 Channel Gap

Some of the microchannel devices have a gold base and three full copper walls which transfer heat to the fluid, but many have a gold base, two full copper walls, and a fourth wall composed partially of copper and partially of parylene. The portion of the wall composed of parylene is visible under a microscope as a “gap”, since the parylene is transparent. This gap width varies depending on the duration of the copper electroplating process during microfabrication. The total thermal resistance of the microchannel device is lower when the gap is smaller because the heat transfer area is greater. It is difficult to measure the channel gap visually under a microscope and measurements produce an uncertainty of 10 - 20 μm. A parametric study, where the gap is varied from 10 to 50 μm showed that the gap size can change the heater temperature by ~1 °C, with larger gap sizes having higher temperatures.

5.3.3 Gold Thickness

The fully coupled CFD model also suggested that the base temperature could vary by as much as 1 °C in the circumferential channel direction depending on the thickness of the Au electroplating seed layer. This suggests that assuming uniform circumferential temperature profile for the microchannels may introduce some error. This was investigated by examining the temperature profile of the gold layer at the channel mid-point. The gold layer is the base of the microchannels, so the gold layer temperature is the base temperature for the channel walls. The base temperature in the fin regions is less than the base temperature underneath the microchannels. This effect is not caused by poor fin efficiency, but is instead caused by the low conductivity of the glass substrate and combined with the small thickness of the gold layer. Heat generated directly underneath the microchannel does not have an efficient path to the channel walls. This effect is present in the experimental setup since the heaters are located directly underneath the microchannels and the substrate is made of glass. If the substrate were silicon, or if the heaters were on the backside of the substrate, heat spreading would ensure the base temperature was uniform.

The base and wall temperature could be made more uniform for this experiment if the gold layer thickness was increased. This is shown by a parametric study for the 100 μm wide channels where the gold layer is varied from 0.4 to 5 μm in Figure 50. It is important to note that increasing the gold layer thickness from 0.4 to 5 μm does not significantly decrease the average base temperature compared to the uncertainty in temperature measurement, which is 1 °C. This suggests that increasing the gold thickness would not significantly improve the measurement capabilities of this setup.

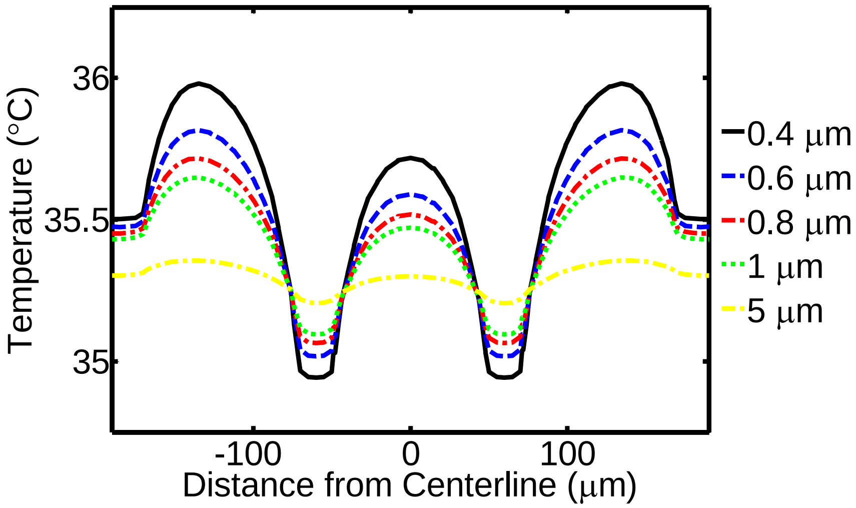

Figure 50: Base temperature profile at the mid-point of the microchannels for a variety of gold layer thicknesses. Increasing the gold layer thickness increases the temperature uniformity but does not significantly decrease the average base temperature compared to the uncertainty in temperature measurement, which is 1 ºC.

5.3.4 Suggestions for Future Experiments

In Sections 5.3.1-5.3.3, numerous potential sources of error have been identified which may be responsible for the disagreement between experimental and computational results. It is suggested that using Si_3N_4 or SiO_2 as an electrical insulator instead of parylene could reduce the possibility of delamination and the magnitude of thermal contact resistances in the microchannel device. Si_3N_4, SiO_2 and parylene all have similar breakdown voltages (~ 1-4 MV/cm), but Si_3N_4 and SiO_2 have higher thermal conductivities than parylene. It is also suggested that the gold thickness could be increased to help improve heat spreading to the channel walls and improving wall temperature uniformity. Finally, more precise measurements should be taken during the fabrication process. Gap size could be more accurately measured using a contact profileometer than using a visual microscope as was done during the fabrication of the chips for this experiment.

5.4 Comparison of Modeling Techniques

Two common methods used to model microchannel heat sink performance include CFD and resistor network models. The CFD model can give very accurate results, but it is computationally expensive. Resistor network results are less accurate, but take much less time to compute. An empirical correlation based model, where conduction in the channel walls is modeled using the finite element method and convection at the microchannel walls is represented using empirical relations, was described in Section 3.2.5. It is thought that this method will provide a balance of accuracy and simplicity, while still retaining the ability to model complex conduction effects in the substrate.

CFD modeling was compared with both the empirical correlation based model and a resistor network model for a three microchannel device with channel widths of 100 μm. Two empirical correlation based models were used: one which assumed fully developed flow throughout the channel, and one which considered developing flow at the channel entrance. Likewise, two resistor network models were used: one which assumed fully developed flow throughout the channel, and one which considered developing flow at the channel entrance. The axial heater temperatures found using these models are compared in Figure 51.

All the models adequately predict axial heater temperature. The empirical correlation based model and CFD results were a near perfect match, with an error of less than 0.2 ºC for a majority of the channel length. The resistor network model slightly overpredicted axial heater temperature compared to the CFD results and the empirical correlation based model. This is likely because the resistor network model neglects the effects of air free convection cooling of the device and heat spreading in the microchannel walls and substrate. The CFD and empirical correlation based models include both of these effects. Using the developing flow correlation instead of the fully developed correlation only affected heater temperature in the developing region.

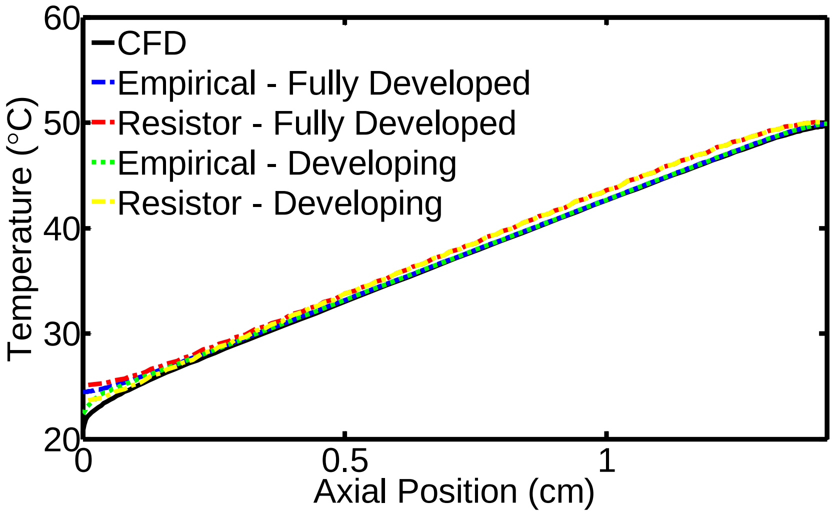

Figure 51: The axial heater temperature found using the CFD model, empirical correlation based model, and resistor network model are compared and are very close.

Although the results were similar, the amount of time needed to solve the various models varied significantly. The models were run on a desktop computer with a 2.66 GHz processor and 8 Gb RAM and the solution times are compared in Table 10. The CFD models took longest to solve and the resistor network models solved in the shortest amount of time.

Table 10: Comparison of solution time for various modeling techniques.

Model	**Solution Time (seconds)**
CFD	190
Empirical – Fully Developed	70
Empirical – Developing	72
Resistor – Fully Developed	1.38
Resistor – Developing	1.40

Although the empirical correlation based model takes less time to solve than the CFD model, it does not solve as quickly as the resistor network model, which still gives very good results for axial heater temperature. However, the resistor network model is not able to resolve complex conduction effects in the microchannel substrate like the empirical correlation based model. For example, the temperature profile of the gold layer (base temperature at the channel walls) at the midpoint of the microchannel is resolved quite well by the empirical correlation based model. The resistor network model does not model conduction in this direction. The fidelity of both empirical correlation based models is compared to the CFD model in Figure 52. The minor difference in the temperature profile is probably caused by the circumferentially uniform convection coefficient used on the microchannel walls in the empirical correlation based model. This is not the case in reality. Even so, the overall cross section temperature profile of the empirical correlation based model using the developing flow correlation and the CFD model is compared in Figures 53 and 54, and matches well.

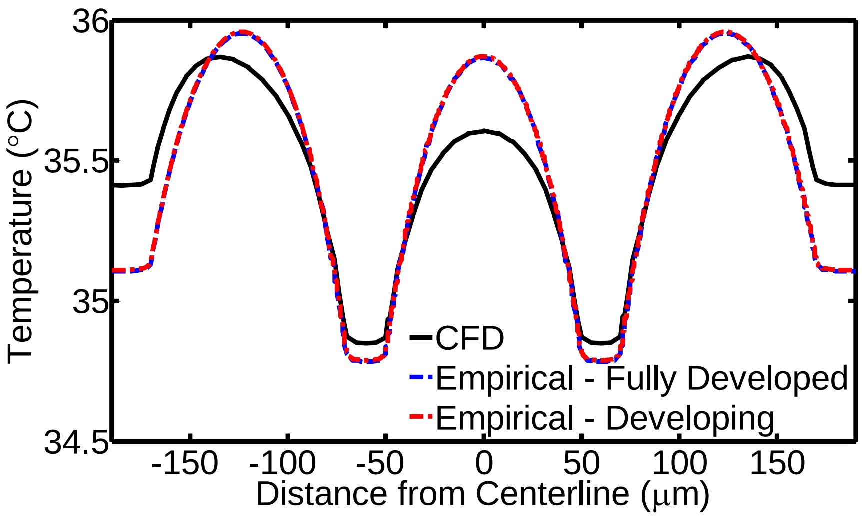

Figure 52: Temperature profile of the gold layer (base temperature at the channel walls) at the midpoint of the microchannel is resolved quite well by the empirical correlation based model. The difference in the temperature profile is probably caused by

the circumferentially uniform convection coefficient on the microchannel walls, which is not the case in reality.

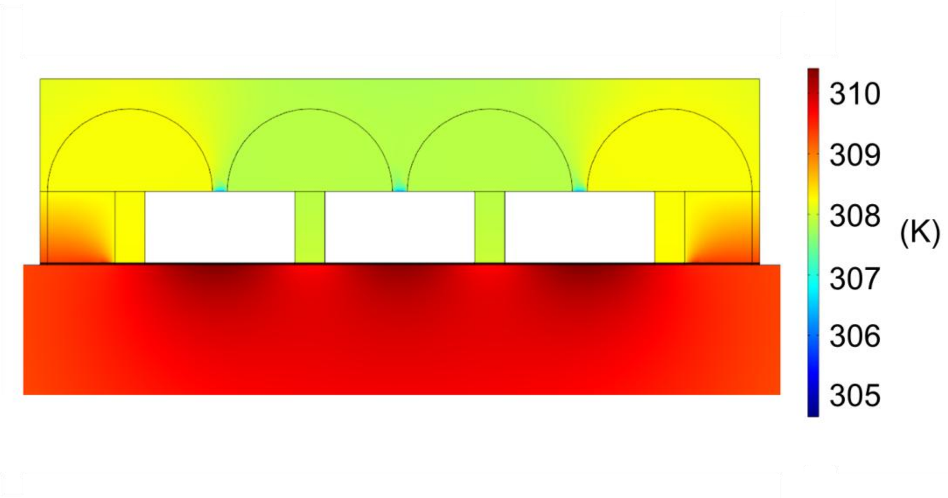

Figure 53: Cross section temperature profile estimated by an empirical correlation based model of a three channel device of 100 μm channel width. The model uses empirical correlations for developing flow to determine the convection coefficient at the microchannel walls.

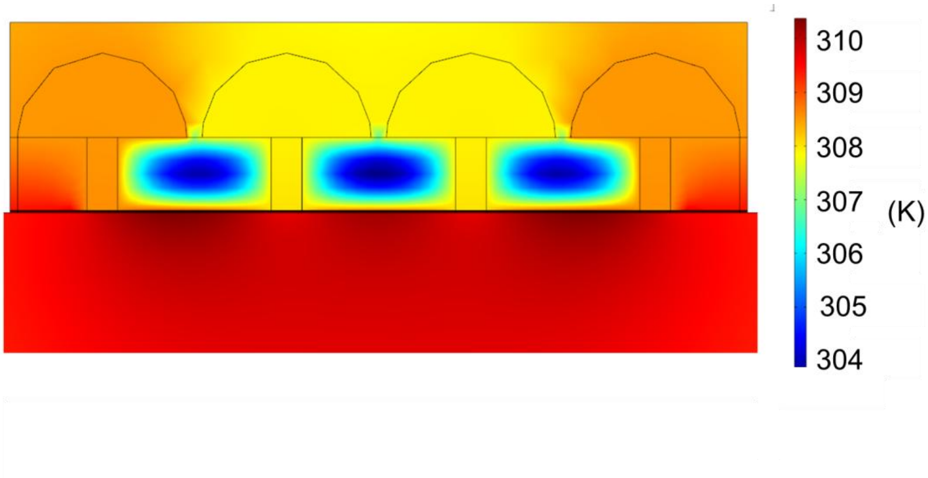

Figure 54: Cross section temperature profile estimated by a 3-D fluid flow and heat transfer coupled model of a three channel device of 100 μm channel width.

5.5 Summary

The pressure drop in the tested microchannels is in good agreement with conventional theory. The microchannels with more than three heat transfer walls are shown to remove heat fluxes greater than 100 W/cm^2 under a pressure drop of less than 75 kPa, which could be used in microelectronic cooling. Differences in the axial heater temperature in experiments and CFD are studied using a sensitivity analysis, and are likely due to uncertainty in thermal contact resistance at the interface of the parylene and Ti heater. Future experiments could be improved by using Si_3N_4 or SiO_2 as an electrical insulator instead of parylene, and by better characterization of experimental geometry and thermal contact resistances. Finally, an empirical correlation based modeling technique has been introduced which is able to model complex conduction effects while still solving in 60% less time than fully coupled CFD.

CHAPTER 6

CONCLUSION

Computational and experimental methods were utilized to explore the use of thermoelectrics and/or microfluidics for cooling hotspots or removing high heat fluxes in stacked chips. A detailed thermal model of a 3-D stacked chip with two dies (top and bottom) and embedded ultrathin (~100 µ) thermoelectric coolers was developed. The numerical analysis suggests that TECs can be used for on demand cooling of hotspots in 3-D stacked chip architecture. Passive cooling of up to 9 °C was observed at the hot spot locations on bottom chip without an applied current. Steady state active cooling caused an additional temperature drop of 5.6 °C due to an applied current in the TEC, yielding a total of up to 14.6 °C steady state cooling. A strong vertical coupling was observed between the top and bottom TECs. It was also determined that bottom TECs can detrimentally heat the top hotspots in both steady state and lead to poor transient performance. Furthermore, the effect of contact resistances was deemed very significant in stacked chip architecture and can extensively decrease the COP of TEC devices. It was observed that the TEC-spreader thermal contact resistance can have a dominant effect on TEC performance due to the large magnitude of the TEC-spreader contact resistance compared to the contact resistances inside the TEC module at the thermoelectric-copper interface. Finally, the transient operation of TECs provided more cooling than steady state operation. A square root current pulse with 0.05 s duration provides 7.4 °C of active cooling (1.8 °C more cooling than steady state) on the bottom hotspot and uses less energy than a constant current pulse. Square root pulses also cause less top hotspot heating than constant current pulses and smaller temperature overshoots. The analysis showed that TECs can be effective in hot spot thermal management for 3-D packages. However, TECs need to be carefully placed in an electronic package and the applied current though these TECs need to be optimized for energy efficient operation. Future developments in the fabrication of ultrathin TEC modules will further encourage efforts on integration of these modules in 3-D packages.

Several microchannel geometries for chip cooling were investigated using experimental methods. This includes geometries where more than three walls transfer heat to the fluid, which is uncommon in microchannels due to fabrication restrictions. The pressure drop in the tested microchannels is in good agreement with conventional theory, and the microchannels with more than three heat transfer walls are shown to remove heat fluxes greater than 100 W/cm^2 under a pressure drop of less than 75 kPa, which could be used in microelectronic cooling. A trend of increasing Nusselt number as a function of Reynolds number was apparent, which is similar to what has been observed in much of the previous literature. Differences between the Nusselt number results in this work and previous works is likely due to different methods used for calculating the Nusselt number, differences in boundary conditions, inclusion or exclusion of the entrance length, and heat conduction in the substrate. Differences in the axial heater temperature in experiments and CFD were studied using a sensitivity analysis, and are likely due to the uncertainty in the estimation of thermal contact resistance at the interface of the parylene and Ti heater. Future experiments could be improved by better characterization of microchannel geometry and thermal interface resistances. Finally, an empirical correlation based modeling technique has been introduced which is able to model complex conduction effects while still solving in 60% less time than fully coupled CFD.

Future work could consist of TEC and microchannel simulations on 3-D stacked chip packages where TECs cool hotspots and microchannels cool the background heat flux. This could be accomplished using the TEC modeling technique used in this work and the empirical correlation based modeling technique for microchannels. In addition, the influence of varying cross sectional geometry along the axial channel direction on heat transfer and fluid flow should be investigated.

In the grand scheme of thermal management, the areas of greatest influence include developing new fabrication methods. For thermoelectrics, future work should focus on developing new CMOS compatible and on-chip fabrication techniques for high figure-of-merit thermoelectric devices. This work should include experimental characterization of thermal contact resistances for thermoelectric materials due to its influence on TEC performance. For microchannels, developing new on-chip fabrication techniques for microchannel and pumping systems which meet the various manufacturing, packaging, thermal, and electrical system requirements would have the greatest impact in the field.

APPENDIX A

NUSSELT NUMBER CALCULATION ASSUMPTIONS

A.1 Fin Efficiency

The fin efficiency can be calculated using Equations 57 [83].

$$\eta = \frac{\tanh(mL)}{mL} \tag{57}$$

Where *m* is defined using Equation 58 and *L* is the fin length

$$m = \sqrt{\frac{2hp}{kA_{cs}}} \tag{58}$$

In this equation, *h* is the convection coefficient, *p* is the fin perimeter, *k* is the thermal conductivity of the fin, and A_{cs} is the cross sectional area of the fin. If we consider that a microchannel has a very long fin width, *w*, compared to fin thickness, *t*, the expression for *m* reduces to Equation 59.

$$m = \sqrt{\frac{2h}{kt}} \tag{59}$$

For all the experimental conditions, the fin thickness and thermal conductivity are held constant at 20 μm and 400 W/m-K, respectively. The maximum convection coefficient observed in the experiment was around 12,000 W/cm^2-K for the 70 μm wide channels at a high flow rate. The maximum length of the fin is approximated to be around 150 μm. This is a conservative approximation corresponding to a 70, 100, or 200 μm wide channel with copper fully covering the top channel wall. Using these values for a conservative approximation, the fin efficiency is found to be 99.01 %.

A.2 Neglecting Axial Fluid Heat Conduction

Axial heat conduction in a fluid can generally be neglected if the Peclet number is sufficiently large. Specifically, the axial fluid conduction only needs to be taken into account when Equation 60 is satisfied [114].

$$\frac{x}{r_h} Pe < 20 \tag{60}$$

In this equation, x is the axial distance along the channel, r_h is the hydraulic radius of the channel, and Pe is the Peclet number. For the experiments described in this work, the minimum Peclet number divided by hydraulic radius was $2\text{x}10^6$. This suggests that axial heat conduction only needs to be considered in the first 10 μm of the channel, which is only a very small fraction of the entire channel length.

A.3 Neglecting Axial Substrate Heat Conduction

Axial heat conduction in the substrate can only be neglected under certain circumstances. Specifically, the axial heat conduction in the substrate can be neglected if the non-dimensional number M is less than about 0.01. M is given by Equation 61 [122].

$$M = \frac{k A_{cs} \frac{dT}{dx}}{\rho c_p v_{avg} A_{csc} (T_{out} - T_{in})} \tag{61}$$

In this equation, M is the non-dimensional axial conduction number, k is the thermal conductivity of the substrate, A_{cs} is the channel wall cross sectional area, $\frac{dT}{dx}$ is the axial channel wall temperature gradient, ρ is the fluid density, c_p is the specific heat of the fluid, v_{avg} is the average fluid velocity A_{csc} is the channel cross sectional area, T_{out} is the fluid outlet temperature, and T_{in} is the fluid inlet temperature. The value of M must be calculated for each experimental condition separately because it can vary. For some of the experiments, it is less than 0.01, for others, it is more than 0.01.

A.4 Neglect Viscous Heating

Viscous heating can be confirmed to be negligible in our regime, based on Equation 62 [118].

$$\frac{\Delta\theta_b}{\Delta\theta_{\mathrm{ref}}} = 4\frac{\mathrm{Ec}}{\mathrm{Re}}[\mathrm{fReL}^*] \tag{62}$$

In this equation, $\Delta\theta_b$ is the temperature rise due to viscous heating, $\Delta\theta_{\mathrm{ref}}$ is a reference temperature rise along the microchannel, *Ec* is the Eckert number, *Re* is the Reynolds number, f is the friction factor, and L^* is the non-dimensional length of the channel.

Alternatively, a much simpler conservative estimation can be made by considering that the maximum energy dissipated due to viscous heating is limited by the pumping power of the system. The pumping power is defined by Equation 63.

$$P = \Delta P A v_{avg} \tag{63}$$

In this equation, P is power, ΔP is the pressure drop, A is the total cross sectional channel area, and v_{avg} is the average fluid velocity. If the pumping power is much less than the power dissipated by the heaters, then viscous dissipation is negligible. It can be confirmed that the pumping power reaches a maximum of 0.16 % of the heater power for the experiments in this work, suggesting that viscous dissipation is negligible. Furthermore, the maximum Brinkman number observed in the experiments is 0.00027, further reinforcing this claim.

APPENDIX B

EXPERIMENTAL UNCERTAINTY ANALYSIS

Experimental uncertainty plays an important role in any experiment. Generally, there are two types of experimental uncertainty: uncertainties due to instrumentation and uncertainties related to the random variation in measured results. Data from the three channel device of 100 μm wide channels and a coolant flow rate of 750 μL/min is used to demonstrate the experimental uncertainty for the measurements in this work because this device is one of the devices used to compare the experimental and computational results from this work in Section 5.4. The calibration and procedure used in this work were designed to eliminate experimental bias to the greatest extent possible. In this uncertainty analysis, uncertainties from the calibration procedure are neglected, unless specified otherwise. However, instrumentation uncertainty and uncertainties due to random variation in measured results are considered. Instrumentation uncertainties are calculated using equations given in the Agilent 34401A User Guide and from a technical data sheet for the Omega pressure transducers. In this work, the experimental measurements were taken 10 times and the average value was used in the calculations in order to reduce the random variation in the measured results. For a small number of measurements, the uncertainty of the sample mean is defined by Equation 64:

$$U_r = t\left(\frac{s}{\sqrt{N}}\right) \tag{64}$$

In this equation, U_r is random variation uncertainty, t takes the value of 2.26 according to statistics tables for a 10 sample mean and a 95% confidence interval, s is the standard deviation of the sample, and N is the number of measurements in the sample. Finally, the total uncertainty of a measurement can be calculated using Equation 65:

$$U = U_i + U_r \quad (65)$$

In this equation, U is total uncertainty, U_i is the instrument uncertainty, and U_r is the random variation uncertainty. The relative uncertainty is denoted by the symbols u_r and u_i, respectively. Table 11 summarizes the experimentally recorded values, total uncertainty for each of the measured values, and the relative uncertainty for each measured value.

Table 11: Experimentally recorded values for a three channel device of 100 µm wide channels and total experimental uncertainty for each measurement.

Variable	Experimentally Measured Value	Total Experimental Uncertainty	Total Relative Uncertainty
Flow rate (µL/min)	750	7.5	1.00%
Tin (°C)	18.6	1.016	5.46%
$V_{H,1}$ (V)	2.21	8.7×10^{-4}	0.04%
$V_{H,2}$ (V)	2.23	7.8×10^{-4}	0.03%
$V_{H,3}$ (V)	2.21	8.6×10^{-4}	0.04%
$V_{H,4}$ (V)	2.23	8.8×10^{-4}	0.04%
$V_{H,5}$ (V)	2.23	9.2×10^{-4}	0.04%
$V_{H,6}$ (V)	2.20	8.0×10^{-4}	0.04%
$V_{H,7}$ (V)	2.23	8.8×10^{-4}	0.04%
$V_{PCB,1}$ (V)	0.39	1.7×10^{-4}	0.04%
$V_{PCB,2}$ (V)	0.38	1.5×10^{-4}	0.04%
$V_{PCB,3}$ (V)	0.39	1.7×10^{-4}	0.04%
$V_{PCB,4}$ (V)	0.38	1.4×10^{-4}	0.04%
$V_{PCB,5}$ (V)	0.37	1.8×10^{-4}	0.05%
$V_{PCB,6}$ (V)	0.39	1.9×10^{-4}	0.05%
$V_{PCB,7}$ (V)	0.38	1.5×10^{-4}	0.04%
I_3 (mA)	78.75	0.071	0.09%
I_5 (mA)	79.71	0.077	0.10%
P_{in} (kPa)	161.15	1.98	1.23%
P_{out} (kPa)	91.36	0.99	1.09%

Uncertainty in the dimensions of the microchannels can also have an important effect on the results. During fabrication, the dimensions of the microchannels and walls cannot be controlled exactly. Generally, the microchannels are slightly trapezoidal, with larger base widths. Consequently, the channel walls tend to be tapered on the bottom. This variation is due to the photoresist exposure and electroplating fabrication process. The variation of microchannel width could not be measured directly, but is thought to be around 4 μm. On a single fabrication wafer, the variation in microchannel height is measured to be between 46.1 and 49.5 μm, with an average height of 47.57 μm. The height of each microchannel was not measured directly, only average measurements for an entire wafer were recorded. These measurements suggest an uncertainty in the microchannel height of about 2.5 μm. For Nusselt number calculations, the gap size also has an effect. The gap size was measured using an optical microscope and camera for each microchannel sample tested. For the three channel device of100 μm wide channels, the gap size was recorded as 10 μm with an uncertainty of 10 μm. From the camera measurement, it was clear that a gap was present, but the true length of the gap was difficult to determine. The lengths of the microchannels were 1.42 cm with an estimated uncertainty of about 0.02 cm. Additionally, some of the microchannels may have defects which were not noticed under optical inspection of the channels prior to experiment. This would introduce additional uncertainty which is not taken into account in this analysis.

Uncertainties in the presented results may be calculated using a propagation of error analysis. The uncertainty, U_F, of the variable F, which is a function of the independent variables x_1, x_2, …, x_n, where n is the number of variables and U_n is the uncertainty of a variable, can be described by Equation 66 [106]:

$$U_F = \sqrt{\sum_{i=1}^{n}\left(\frac{\partial F}{\partial x_i}U_i\right)^2} \tag{66}$$

This equation can be simplified to give two basic rules for propagation of uncertainty. When a function is defined by only summation or subtraction of *n* independent variables, the absolute uncertainty of that function is described by Equation 67. When a function is defined by only multiplication or division of *n* independent variables, the relative uncertainty of that function is described by Equation 68.

$$U_F = \sqrt{\sum_{i=1}^{n} U_i^2} \tag{67}$$

$$u_F = \sqrt{\sum_{i=1}^{n} u_i^2} \tag{68}$$

In the uncertainty analysis, Equations 67 and 68 are primarily used due to their simplicity.

First, we seek to determine the uncertainty of the friction factor, described in Equation 34 from Section 3.2.3. For simplicity, we neglect the uncertainty related to correction for expansion and contraction effects and uncertainties in the calculation of material properties, which are evaluated at the mean fluid temperature. The uncertainty of the measured pressure drop is calculated using Equation 67 and is found to be 2.21 kPa (3.17%). The uncertainty of the hydraulic diameter can be calculated using Equation 69 [106]. In this equation, *U* is absolute uncertainty, *W* is channel width, and *H* is channel height. It is found to be equal to 2.39 μm (3.59%).

$$U_A = \sqrt{U_H^2\left(\frac{2W(W+H) - 2(WH)}{(W+H)^2}\right)^2 + U_W^2\left(\frac{2H(W+H) - 2(WH)}{(W+H)^2}\right)^2} \tag{69}$$

Considering that the average fluid velocity is equal to the volumetric flow rate divided by channel cross sectional area, the relative uncertainty of the friction factor can be calculated using Equation 68 and is found to be 10.4 %. Neglecting uncertainty in material properties, the relative uncertainty in the Reynolds number is found to be 12.7 % using Equation 68.

Next, it is desired to determine the uncertainty in the heater temperature measurements. These measurements were compared to a computational simulation in Section 5.2. The uncertainty of the measured voltages, currents, and resistance in Table 11 are very low (< 0.1%). As a result, the main uncertainty in the heater temperature measurement is due to the calibration. During the calibration of heater resistances, two type-T thermocouples are used to determine the calibration temperature. These thermocouples have an absolute uncertainty of about 1 °C. Therefore, it is reasonable to assume that the uncertainty of the RTD measurements is limited by the thermocouples, not the voltage and current measurements. The RTD measurements therefore have an uncertainty of about 1 °C.

Finally, the uncertainty of the calculated heat transfer coefficient and Nusselt number is determined. The Nusselt number is calculated using Equations 44-45, described previously in Section 3.2.3. The uncertainties in this calculation come from the heat removed by water between heaters 3 and 5, temperature difference between the wall and fluid at the channel mid-point, and the channel wall area between heaters 3 and 5.

The uncertainty for the amount of heat removed by water is dominated by the relative flow rate uncertainty (1%) if material property uncertainties are neglected. The temperature difference between substrate heaters has a very low uncertainty because they were calibrated at the same temperature with the same thermocouples, and the errors in electrical measurements are very small (< 0.1 %). As a conservative estimate, the relative uncertainty of the heat removed by water is taken as 2%, which is twice the relative uncertainty of the flow rate alone.

The uncertainty in the wall temperature is 1 °C, due to the uncertainty in calibration, as described previously. The water temperature in the center of the channel is calculated using a linear regression method, as described in Section 3.2.3. The slope of this linear regression is expected to have a negligible uncertainty because all the heaters were calibrated at the same temperature with the same thermocouples and the relative uncertainties in electrical measurements are very small (< 0.1 %). Therefore, the absolute uncertainty in water temperature is assumed to be 1 °C, since the water temperature uncertainty is dominated by the uncertainty of the inlet thermocouple. Using Equation 67, it is clear that the absolute uncertainty for the wall and water temperature difference is approximately 1.41 °C. Since the measured temperature difference was 13.52 °C, the relative uncertainty in the temperature difference is 10.0%.

The uncertainty of the channel wall area between heaters 3 and 5 can be found by considering that the channel wall area is described by Equation 70.

$$A = \frac{2}{7}L(2H + 2W - G) \tag{63}$$

In this equation, L is length, H is channel height, W is channel width, and G is the measured channel gap. The uncertainty of the expression (2H + 2W – G) is found to be 10.6 µm (3.7%) using Equation 67. The relative uncertainty in the wall area, *A*, is then found to be 3.9% using Equation 68.

Finally, the uncertainty for convection coefficient and Nusselt number can both be calculated using Equation 68. Uncertainties due to material property variation are neglected. The relative uncertainty of the convection coefficient is found to be 11.3 %

and the relative uncertainty of the Nusselt number is found to be 11.9%. The main results of this uncertainty analysis are summarized in Table 12.

Table 12: Relative uncertainty results.

	Relative Uncertainty (%)
Pressure Drop, ΔP	3.2
Hydraulic Diameter, D_h	3.6
Mass Flow Rate, $\dot{m}$	1.0
Friction Factor, f	10.4
Reynolds Number, Re	12.7
Convection Coefficient, h	11.3
Nusselt Number, Nu	11.9

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