RESPONSE OF MULTI-PATH COMPLIANT INTERCONNECTS SUBJECTED TO DROP AND IMPACT LOADING

A Thesis
Presented to
The Academic Faculty

by

Anirudh Bhat

In Partial Fulfillment
of the Requirements for the Degree
Master of Science in the
G. W. Woodruff School of Mechanical Engineering

Georgia Institute of Technology
December 2012

RESPONSE OF MULTI-PATH COMPLIANT INTERCONNECTS SUBJECTED TO DROP AND IMPACT LOADING

Approved by:

Dr. Suresh K. Sitaraman, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Rao R. Tummala
School of Material Science and Engineering
Georgia Institute of Technology

Dr. I. Charles Ume
School of mechanical Engineering
Georgia Institute of Technology

Date Approved: August 20, 2012

Dedicated to my parents, for always being the supporting light in my life.

ACKNOWLEDGEMENTS

I would initially like to thank my parents for their countless sacrifices and for providing for me in every possible way. Without their guidance and help, I would not be the person I am today.

I would like to thank my advisor, Prof. Suresh K. Sitaraman for giving me constant guidance and support throughout my master's program. His encouragement and advice have greatly helped me in the completion of the thesis and I am greatly appreciative of the opportunity he has provided. I would like to thank Prof. Rao R Tummala and Prof. Charles Ume for serving on my thesis committee and providing valuable guidance and suggestions.

I would like to thank Prof. David W. Rosen for allowing me to use the facilities of the Rapid Prototyping and Manufacturing Institute (RPMI) laboratory for fabrication purposes. I would like to thank Prof. Jonathon S. Colton for allowing me to use the Instron® Dynatup 8250 drop weight impact testing machine to conduct experimental testing. I gratefully acknowledge the support of the National Science Foundation in providing funding for this project under Grant No. ECCS-0901679.

I would also like to thank my fellow lab mates in the Computer Aided Simulation of Packaging Reliability (CASPaR) laboratory, especially Raphael Okereke, Sathanarayanan Raghavan, Christine Taylor and Justin Chow, for providing me with helpful input at various stages of the project. Their insight was crucial in understanding several keys concepts and I am highly indebted to them for their help.

I would like to thank my older brother, Arjun, whose reassuring words helped me throughout the project and encouraged me to do my best.

Finally, I would like to thank all my friends and family for always supporting me and believing in me. Thank you one and all!

TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	iv
LIST OF TABLES	x
LIST OF FIGURES	xi
LIST OF SYMBOLS AND ABBREVIATIONS	xv
SUMMARY	xvii
CHAPTER	
1 INTRODUCTION	1
2 LITERATURE REVIEW	3
2.1 Interconnects	3
2.1.1 Wire-bonding	4
2.1.2 Tape Automated Bonding (TAB)	5
2.1.3 Flip Chip	6
2.2 Compliant Interconnects	7
2.2.1 Sea of Leads	8
2.2.2 FormFactor's MicroSpring MOST™	9
2.2.3 Helix Interconnects: β-Helix and G-Helix	9
2.2.4 Parallel-Path FlexConnect	10
2.2.5 Multi-path Fan-shaped Compliant Interconnects	11
2.3 Drop Testing	12
2.3.1 JEDEC Standard for drop testing	13
3 OBJECTIVES AND METHODOLOGY	18
4 DROP TESTING OF COMPLIANT INTERCONNECTS	21

4.1 Sample Fabrication 23
4.1.1 Stereolithography 23
4.1.2 Viper® SLA^2 Stereolithography machine 26
4.1.3 Stereolithography material: RenShape™ SL 7510 27
4.1.4 Model Geometry 29
4.1.5 Actual sample fabrication procedure 31
4.1.6 Post-fabrication treatment and processing 33
4.2 Experimental setup 36
4.2.1 Instron ® Dynatup 8250 drop weight impact tester 36
4.2.2 Drop test fixture 38
4.2.3 Data Acquisition Module: NI® 9215 DAQ 39
4.2.4 Measurement device: Strain gauges 40
4.2.5 Power Supply 42
4.2.6 Measurement device: Accelerometer 42
4.2.7 Analysis software: LabView® 43
4.3 Drop test setup and procedure 44
4.3.1 Drop heights and sample selection 49
4.3.2 Three-arc compliant interconnect model drop testing 51
4.3.3 Bump-model interconnect assembly drop testing 54
5 FINITE-ELEMENT SIMULATION OF DROP TESTING 59
5.1 Traditional drop testing simulation 59
5.2 Input-G Method 60
5.2.1 Impact pulse 61
5.2.2 Displacement equation 63
5.3 Modeling geometry 66

5.3.1 Basic dimensions 66

5.3.2 Meshing 66

5.3.3 Material properties 68

5.3.4 Boundary conditions 69

5.3.5 Damping and damping ratio ξ 70

5.4 Three-arc interconnect drop test simulations 72

5.4.1 Boundary condition input 73

5.4.2 Basic results 75

5.5 Bump interconnect drop test simulations 76

5.5.1 Boundary condition input 77

5.5.2 Basic results 79

6 RESULTS AND COMPARISON 81

6.1 Multi-path three-arc compliant interconnect experimental results 81

6.1.1 Acceleration data 84

6.1.2 Strain data 86

6.2 Bump interconnect experimental results 88

6.2.1 Acceleration data 89

6.2.2 Strain data 90

6.3 Comparison of experimental response of three-arc interconnects and bump interconnects 93

6.4 Three-arc compliant interconnect finite-element simulation results 96

6.5 Bump interconnect finite-element simulation results 98

7 PROPOSED COPPER-SILICON INTEROCNNECT-DIE ASSEMBLY SIMULATION 100

7.1 Scaled-up Copper-Silicon interconnect-die assembly 101

7.1.1 Model geometry 101

7.1.2 Material properties 102

7.1.3 Boundary conditions 102

7.1.4 Results 104

7.2 True scale Copper-Silicon Interconnect-Die assembly 105

7.2.1 Model geometry 105

7.2.2 Material properties 108

7.2.3 Boundary Conditions 108

7.2.4 Results 109

8 CONCLUSIONS AND FUTURE WORK 111

8.1 Conclusions 111

8.2 Future Work 112

APPENDIX A: Experimental drop testing acceleration data 114

APPENDIX B: Experimental drop testing strain data 120

APPENDIX C: Finite-element drop testing simulation strain data 126

REFERENCES 130

LIST OF TABLES

Page

Table 4.1: RenShapeTM SL 7510 polymer resin material properties 28

Table 4.2: Impulse times recorded from experiment for three-arc interconnect drop test samples 52

Table 4.3: Impulse times recorded from experiment for bump interconnect drop test samples 56

Table 5.1: Polymer material properties 68

Table 5.2: Damping ratios for three-arc interconnect model for different drop heights 75

Table 5.3: Damping ratios for bump interconnect model for different drop heights 78

Table 6.1: Peak acceleration and impact times for three-arc interconnect drop test sample 85

Table 6.2: Experimental strain data for three-arc interconnect drop test sample 87

Table 6.3: Peak acceleration and impact times for bump interconnect drop test sample 90

Table 6.4: Experimental strain data for bump interconnect drop test sample 91

Table 6.5: Experimental data comparison between three-arc and bump interconnect samples 94

Table 6.6: Experimental strain data comparison between three-arc and bump interconnect samples 95

Table 6.7: Experiment versus simulation strain data comparison for three-arc interconnect 97

Table 6.8: Experiment versus simulation strain data comparison for bump interconnect 99

Table 7.1: Material properties used in simulation 102

LIST OF FIGURES

Page

Figure 2.1: Stacked dies with wire-bonds 5

Figure 2.2: Tape Automated Bonding 6

Figure 2.3: Schematic of a typical flip-chip package 7

Figure 2.4: Sea of Leads (SoL) interconnect with air gap 8

Figure 2.5: FormFactor® MicroSpring MOST™ 9

Figure 2.6: Micrograph of 100 µm pitch G-Helix interconnects 10

Figure 2.7: Parallel-Path FlexConnects at 100 µm pitch 11

Figure 2.8: Multi-path fan-shaped compliant interconnects 12

Figure 2.9: JEDEC standard drop test schematic 14

Figure 4.1: Virtual slicing of input CAD model 23

Figure 4.2: Stereolithography/Rapid Prototyping process 24

Figure 4.3: Viper® SLA^2 stereolithography machine 26

Figure 4.4: FEM model used to generate 3D CAD model for stereolithography input 30

Figure 4.5: Side view schematic of three-arc interconnect with dimensions 31

Figure 4.6: Support structure layout used for stereolithographic fabrication 32

Figure 4.7: Fabrication process flow 34

Figure 4.8: Three-arc interconnect drop test sample 35

Figure 4.9: Three-arc interconnect drop test sample 35

Figure 4.10: Bump interconnect drop test sample 36

Figure 4.11: Instron® Dynatup 8250 drop weight impact tester 37

Figure 4.12: Custom drop test fixture 39

Figure 4.13: NI® 9215 Data Acquisition Module 40

Figure 4.14: Mounted strain gauges 41

Figure 4.15: HP® Harrison 6201B DC power supply 42

Figure 4.16: Mounted PCB® 352B01 accelerometer next to a linear single-axis strain gauge 43

Figure 4.17: Drop test setup schematic 44

Figure 4.18: Drop test setup schematic layout 45

Figure 4.19: Drop test procedure flowchart 46

Figure 4.20: Accelerometer and strain gauge positions and orientations 47

Figure 4.21: Acceleration plot for 100mm three-arc interconnect model drop test (sample 1) 51

Figure 4.22: Acceleration plot for 100mm three-arc interconnect model drop test (averaged) 52

Figure 4.23: Strain data plot for 100mm three-arc interconnect model drop test (sample 1) 53

Figure 4.24: Strain data plot for 100mm three-arc interconnect model drop test (averaged 53

Figure 4.25: Acceleration plot for 200mm bump interconnect model drop test (sample 1) 55

Figure 4.26: Acceleration plot for 200mm bump interconnect model drop test (averaged) 56

Figure 4.27: Strain data plot for 100mm bump interconnect model drop test (sample 1)57

Figure 4.28: Strain data plot for 100mm bump interconnect model drop test (averaged)57

Figure 5.1: Schematic of Input-G Method showing applied boundary conditions 61

Figure 5.2: Sine and square impact pulses used to calculate input boundary conditions 62

Figure 5.3: Accelerometer mount location to determine impact pulse during drop test 63

Figure 5.4: Acceleration and calculated displacement curves for 536.1G drop event from 500mm drop height 65

Figure 5.5: Simulation model for three-arc interconnects 67

Figure 5.6: Applied boundary conditions 69

Figure 5.7: Acceleration curve for 100mm drop test 71

Figure 5.8: Simulation model for three-arc interconnects 73

Figure 5.9: Calculated displacement curves 74

Figure 5.10: Strain response curve for 500mm drop height three-arc interconnect model simulation 76

Figure 5.11: Bump interconnect simulation model 76

Figure 5.12: Calculated bump interconnect model displacement curves 78

Figure 5.13: Strain response curve for 500mm drop height bump interconnect model simulation 79

Figure 6.1: Sample inside custom drop test fixture 82

Figure 6.2: Strain gauge and accelerometer mounted on three-arc drop test sample 83

Figure 6.3: Strain gauge and accelerometer mounted on bump interconnect drop test sample 83

Figure 6.4: 100mm height drop test acceleration response for three-arc interconnect sample 84

Figure 6.5: Accelerometer mounted on three-arc interconnect sample 85

Figure 6.6: Strain data from 100mm drop test for three-arc interconnect sample 86

Figure 6.7: Acceleration response for 200mm height drop test for bump interconnect sample 89

Figure 6.8: Strain data for 200mm height drop test for bump interconnect sample 91

Figure 6.9: Acceleration response for 200mm height drop test for bump interconnect sample 92

Figure 6.10: Strain data for 100mm height drop test for bump interconnect sample 93

Figure 6.11: Strain data for 100mm height drop test simulation for three-arc interconnect sample 96

Figure 6.12: Strain data for 200mm height drop test simulation for bump interconnect model 98

Figure 7.1: Three-arc Cu interconnect/Si die assembly model 101

Figure 7.2: Acceleration and calculated displacement curves for 536.1G drop event from 500mm drop height 103

Figure 7.3: 500mm drop height finite-element simulation strain data for 150-scale Cu/Si three-arc assembly model 104

Figure 7.4: Three-arc compliant interconnect simulation model 106

Figure 7.5: SOLID versus BEAM force-displacement studies 107

Figure 7.6: True-scale compliant interconnect simulation geometry 107

Figure 7.7: Extended BEAM elements used for ‘zippering’ the interconnect to surrounding elements 108

Figure 7.8: 500mm drop height finite-element simulation for true scale copper-silicon interconnect-die assembly model 110

LIST OF SYMBOLS AND ABBREVIATIONS

G	Acceleration magnitude in terms of Acceleration due to Gravity
h	Drop height in mm
ε	Strain
GF	Gauge Factor
Rl	Lead resistance in Ohm
Rg	Gauge resistance in Ohm
Vr	Voltage Ratio
Vo	Output voltage in Volt
Vex	Excitation voltage in Volt
T	Impulse time in Seconds
π	Pi (3.142)
Gm	Peak acceleration magnitude in terms of Acceleration due to Gravity
d	Displacement in mm
t	Time in seconds
δ	Logarithmic decrement
ξ	Damping ratio
α	Rayleigh damping coefficient
β	Rayleigh damping coefficient
ω	Natural frequency in Hertz
JEDEC	Joint Electron Devices Engineering Council
CAD	Computer-Aided Design
I/O	Input/Output
CTE	Coefficient of Thermal Expansion

SG1	Strain gauge 1
SG2	Strain gauge 2
SG3	Strain gauge 3
DAQ	Data Acquisition System

SUMMARY

Conventional solder balls used in microelectronic packaging suffer from thermo-mechanical damage due to difference in coefficient of thermal expansion between the die and the substrate or the substrate and the board. Compliant interconnects are replacements for solder balls which accommodate this differential displacement by mechanically decoupling the die from the substrate or the substrate from the board and aim to improve overall reliability and life of the microelectronic component. Research is being conducted to develop compliant interconnect structures which offer good mechanical compliance without adversely affecting electrical performance, thus obtaining good thermo-mechanical reliability. However, little information is available regarding the behavior of compliant interconnects under shock and impact loads.

The objective of this thesis is to study the response of a proposed multi-path compliant interconnect structure when subjected to shock and impact loading. As part of this work, scaled-up substrate-compliant interconnect-die assemblies will be fabricated through stereolithography techniques. These scaled-up prototypes will be subjected to experimental drop testing. Accelerometers will be placed on the board, and strain gauges will be attached to the board and the die at various locations. The samples will be dropped from different heights to different shock levels in the components, according to Joint Electron Devices Engineering Council (JEDEC) standards. In parallel to such experiments with compliant interconnects, similar experiments with scaled-up solder bump interconnects will also be conducted. The strain and acceleration response of the

compliant interconnect assemblies will be compared against the results from solder bump interconnects. Simulations will also be carried out to mimic the experimental conditions and to gain a better understanding of the overall response of the compliant interconnects under shock and impact loading. The findings from this study will be helpful for improving the reliability of compliant interconnects under dynamic mechanical loading.

CHAPTER 1

INTRODUCTION

Due to alternating periods of operation and idling, a typical microelectronic package undergoes thermal cycling by means of repetitive heating and cooling. The different materials comprising the package have different Coefficients of Thermal Expansion (CTE) and therefore, expand and contract to different extents during operation. This differential expansion and contraction of package materials leads to the development of stresses, which are transferred to the package die by means of the interconnecting solder bumps. The amount of stress transferred is also increased by the presence of underfill material surrounding the solder bumps. Under the effect of the developed and transferred stresses, the die tends to crack and fail leading to package failure. In addition, any low-K dielectric materials used in the package may also undergo cracking due to stress development and may be subjected to subsequent delamination due to these stresses. These problems are among the primary reasons for microelectronic package failure.

The main cause of this stress transfer is the use of rigid solder bumps, which act as stress transfer conduits. In order to overcome the drawbacks of the solder bump, a proposed alternative is the compliant interconnect. Compliant interconnects are elastically deformable interconnect structures which possess the ability to absorb and reduce stress developed in the package during operation. They aim to prevent the failure of a package by compensating for the differential displacement of the die and the substrate caused due to thermal cycling induced by operation. Compliant interconnects

additionally aim to provide other advantages including reduction in the overall chip or die stresses. They allow easier use of low-K dielectric materials by reducing the stresses which cause low-K dielectric cracking and delamination. Also, the compliant nature of the interconnects removes the need for underfill material, which leads to stress transfer and increase in die stresses.

Till date, researchers have developed numerous compliant interconnect structures to account for the drawbacks of solder bumps. These complaint interconnect structures have been studied in detail from a thermo-mechanical reliability aspect. However, not much has been done to understand the effect of drop and impact on these structures. This area of microelectronic package reliability is in dire need and must be addressed in order to understand the feasibility of using compliant interconnects as operational first level interconnects.

CHAPTER 2

LITERATURE REVIEW

A preliminary background on conventional interconnects, compliant interconnects and drop testing will be given in the following sections.

2.1 Interconnects

Interconnects are the electrical pathways in electronic packages through which power and signals are transmitted between the chip and the underlying substrate, and between the electronic package and the surrounding board and related hardware. They usually consist of low resistance electrical conduits which allow transfer of electrical signals at very high rates. Based on location and function, interconnects can be classified as given below.

- On-chip interconnects: Used to connect devices within a single chip.
- Off-chip interconnects: Used to connect an individual chip to the underlying substrate as well as beyond the substrate, such as connecting the chip directly to the underlying printed circuit board. These are also referred to as first-level interconnects.
- Interconnects connecting the electronic package to the underlying printed circuit board.
- Interconnects connecting different printed circuit boards.
- Interconnects connecting different sub-assemblies and systems

Of the above, the interconnect design dealt with in the currently presented work will be a first-level interconnect, that is, an interconnect that connects the chip to the underlying substrate. First-level interconnects have evolved over the years due to varying demands and requirements imposed on them. This level of interconnects is usually designed keeping several key features in mind. Although the first-level interconnects function as power, ground, and signal interconnects between the chip and the substrate, they must also be able to account for problems in the electronic package that arise during operation of the entire system. They must be mechanically reliable and must be able to take the differential displacement that occurs in the package due to differing coefficients of thermal expansion (CTE) between the chip or die and the substrate, at the same time displaying good electrical characteristics and mechanical reliability. They must be able to account for the low-K dielectric material properties of the various layers used in the microelectronic package and must not create high stresses in the chip or near any brittle material or weak interface. At the same time, they must be cost effective and easily repeatable in fabrication.

Taking into account the above requirements, various first-level interconnects have been designed, of which few are in actual use today. Tummala's book on *Fundamentals of Microsystems Packaging* provides a good overview of typical first-level interconnect technologies in use today [Tummala, 2001].

2.1.1 Wire-bonding

Shown in Figure 2.1, wire-bonding is a basic chip-to-package interconnection methodology wherein fine metal wires are attached between the chip and substrate using ultrasonic bonding techniques. Originating with AT&T's beam lead bonding in the

1950's, wire-bonding is typically done using thin 25 μm thick gold wires. These wires are ultrasonically bonded to the pads available on the chip and the substrate. This technique is largely popular due to the highly flexible interconnection process, low defect rates and large well-established industrial infrastructure.

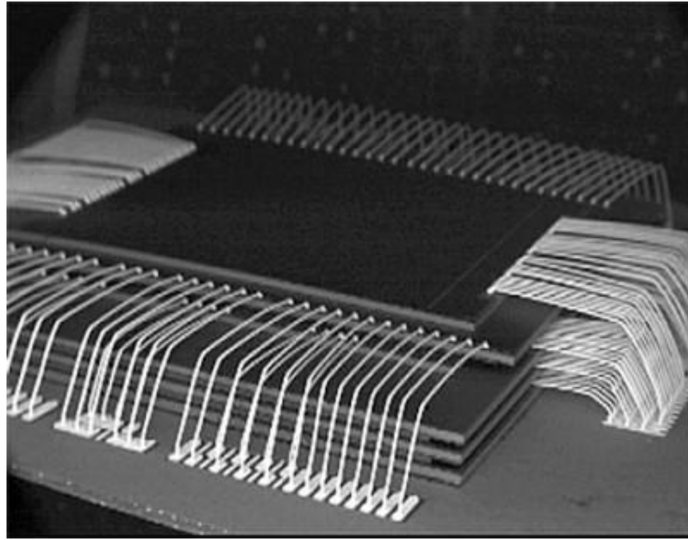


Figure 2.1: Stacked dies with wire-bonds (Courtesy of SOCcentral)

However, these interconnections suffer from poor electrical performance, large footprint size, slow point-to-point attachment process as well as wire-sweep possibility during encapsulation. Despite these drawbacks, wire-bonding is still the most widely preferred means of interconnecting the chip and the substrate [Tummala, 2001].

2.1.2 Tape Automated Bonding (TAB)

Tape automated bonding, better known as TAB, makes use of flexible polymer tapes for providing the interconnection paths. Figure 2.2 shows a top-down view a Tape Automated Bonded strip.

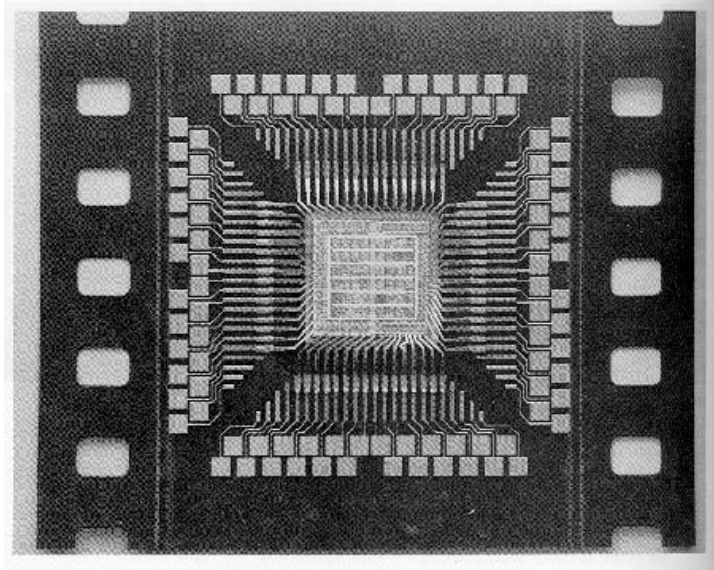


Figure 2.2: Tape Automated Bonding (Courtesy of Westinghouse ESG)

The polymer tapes used in this process are multi-layered, with metal layers within the tape providing the electrical pathways. The fabrication process for TAB is fully automated and thus is able to handle very-large-scale-integration (VLSI) as well as high I/O (input/output) densities. The presence of the polymer tapes prevents wire-looping, a problem present in wire-bonded connections. However, this new interconnection design presents several new problems, including increased package size with increasing I/O counts, necessary peripheral attachment, difficulty of rework, and most of all, large capital investment with very little infrastructure already existing for fabrication and implementation.

2.1.3 Flip Chip

Invented in 1962 by IBM as the Solid Logic Technology, and later converted to Controlled Collapse Chip Connection (C4) in 1970, flip chip technology is one of the most upcoming first-level interconnection techniques. It involves flipping the chip upside down and then bonding the chip directly to the substrate using suitable interconnections.

Known for its rapid fabrication techniques, high I/O counts, low stand-off distance between chip and substrate and good electrical characteristics, flip chip packages usually make use of solder-bumps as the interconnections. While this particular interconnection technique has many advantages, it suffers from other problems such as solder bump failure due to creep and fatigue during operation, delamination between adjacent layers as well as cracking at different locations due to accumulated stresses during operation. Figure 2.3 shows a schematic of a basic flip-chip package.

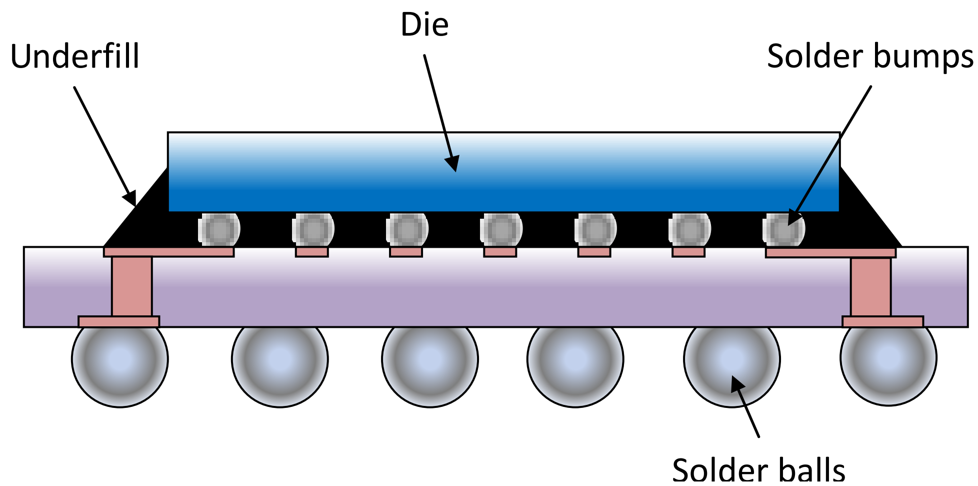


Figure 2.3: Schematic of a typical flip-chip package

2.2 Compliant Interconnects

In order to overcome the problems discussed in the above sections, the concept of the compliant interconnect was developed. Compliant interconnects can be defined as elastically deformable structures which mimic springs and are designed with the main purpose of compensating for the differential displacement or mismatch between the die and substrate during thermal cycling and operation. Simultaneously, they aim to reduce die stresses and due to their compliant nature, try to reduce delamination and cracking by preventing excessive stress concentration at various interfaces within the package. Given

below are some of the compliant interconnect designs which have been developed in the past, along with their advantages and disadvantages. The following sections provide an overview of various compliant interconnects and are based on, among other references, the book chapter by Sitaraman and Kacker [2009].

2.2.1 Sea of Leads

The sea of leads (SoL) is a compliant interconnect design which aimed to rectify package failure due to high mechanical stresses in the low-k interlayer dielectric material of a microelectronic package [Bakir et al, 2005]. Designed for the Wafer Level Package (WLP), these interconnects comprised of compliant leads fabricated on top of a polymer film deposited on a silicon wafer. Solder bumps were deposited on the compliant leads and served as the connecting pathway between the lead and the substrate. The main drawback of this compliant interconnect design was in the use of the underlying polymer layer, which reduced the overall compliance of the compliant lead. Thus, the inherent design of the compliant lead posed limitations on achievable compliance.

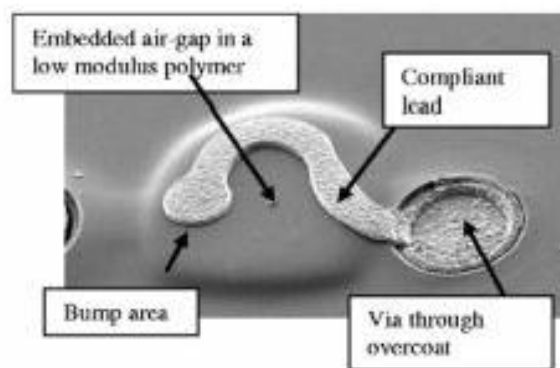


Figure 2.4: Sea of Leads interconnect with air gap [Bakir et al, 2003]

2.2.2 FormFactor's MicroSpring MOST™

Initially designed for probe card applications, FormFactor's MicroSpring wafer scale package MOST™ (**M**icroSpring contact **O**n **S**ilicon **T**echnology) had limited success as an interconnect of the first-level [Novitsky and Pederson, 1999]. Its unique shape was fabricated by controlling the motion of the wire-bonder used for its fabrication. But due to the serial nature of this fabrication process, large I/O density could not be achieved. Figure 2.5 depicts an SEM image of Formfactor® MOST™.

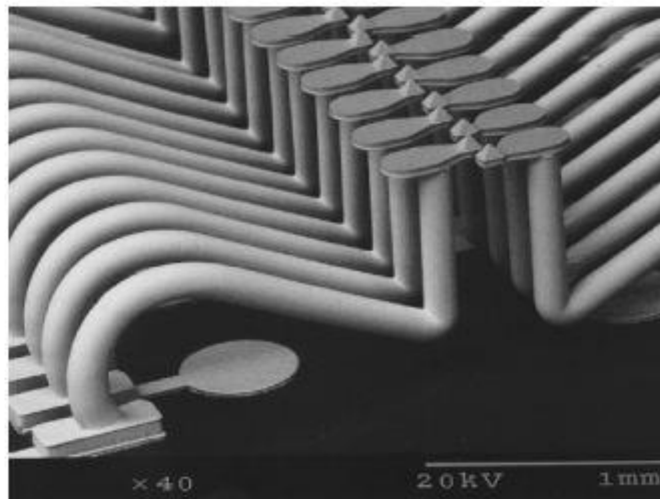


Figure 2.5: FormFactor® MicroSpring MOST™ [Novitsky and Pederson, 1999]

2.2.3 Helix Interconnects: β-Helix and G-Helix

Designed at Georgia Institute of Technology, the helix group of compliant interconnects consisted of spring-like copper-based structures fabricated using a multilayer photolithographic process. The initial design was the β-Helix structure, which was found to have directional problems as well as multiple fabrication steps [Zhu et al, 2003]. In an effort to overcome the drawbacks of the β-Helix, the G-Helix compliant interconnect was designed [Lo et al, 2004].

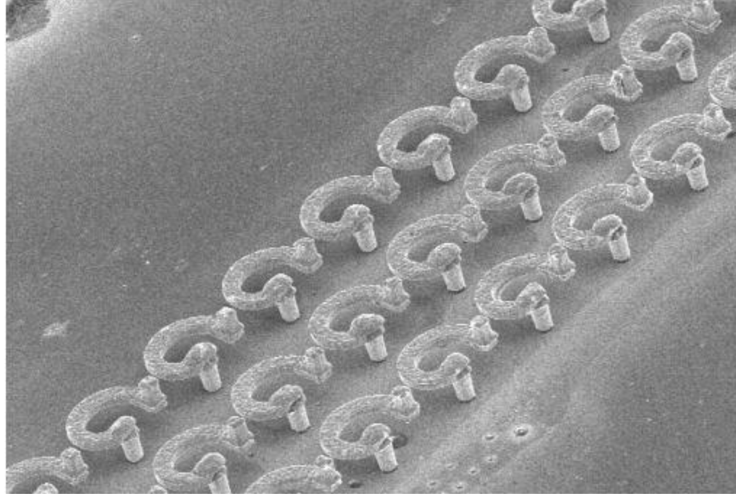


Figure 2.6: Micrograph of 100 µm pitch G-Helix interconnects [Lo et al, 2004]

Shown in Figure 2.6, the G-Helix compliant interconnect consisted of a three-layer copper interconnect. The compliant nature of this compliant interconnect was due to the arcuate beam which connected the posts. The two posts were intentionally offset in order to obtain directional compliance and ensure proper differential displacement in all three *X*, *Y* and *Z* directions. On comparing the two, it was observed that the β-Helix had better mechanical compliance, while the G-Helix displayed better electrical characteristics than the β-Helix. However, both designs were directionally challenged and offered different compliance values in different directions and each design had at least the very least three photolithographically fabricated layers, making fabrication cumbersome.

2.2.4 Parallel-path FlexConnect

In an effort to overcome the problems observed in the β-Helix and G-Helix, FlexConnect compliant interconnects were designed at Georgia Institute of Technology [Kacker et al, 2007]. Shown in Figure 2.7, the FlexConnect compliant interconnect consisted of a two layer structure with mirrored arcuate beams. Requiring a two layer

photolithographic fabrication procedure, the FlexConnect addressed the electrical concerns of the G-Helix by providing opposing electrical pathways, thereby reducing electrical parasitics and providing redundant electrical pathways in case one of failure of one of the arms. The main drawback of this structure was again the directional compliance of the structure, with compliance values being higher along one direction than the other.

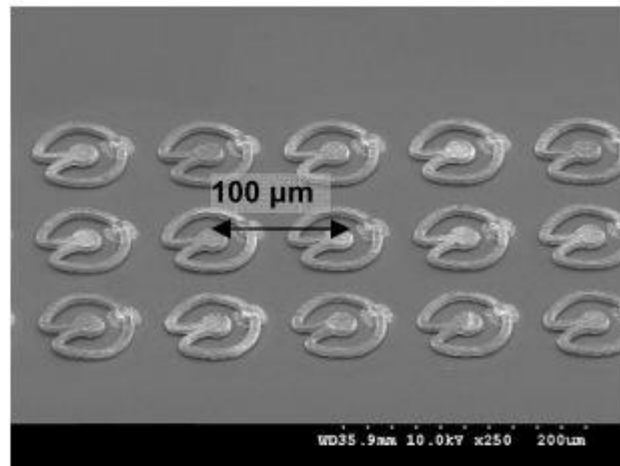


Figure 2.7: Parallel-Path FlexConnects at 100 µm pitch [Kacker et al, 2008]

2.2.5 Multi-path fan-shaped compliant interconnects

The drawback of the FlexConnect lay in the differential directional compliance that was seen in its design. The multi-path fan-shaped compliant interconnects, designed at Georgia Institute of Technology, aimed to address this problem by making use of radially repetitive designs [Lee at al, 2011]. Shown in Figure 2.8, these interconnects possessed compliant arms (two, three or four in number) which were supported on posts. These arcuate beams would take the differential displacement induced during operation,

thereby reducing chip stresses. The radial nature of these compliant interconnects enabled the same compliance value in all in-plane directions.

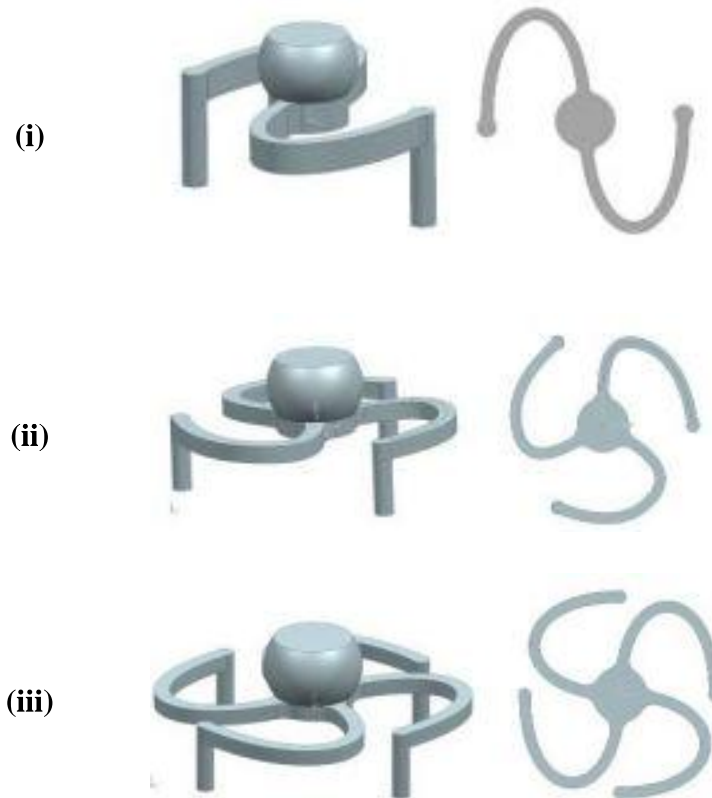


Figure 2.8: Multi-path fan-shaped compliant interconnects – (i) Two-arc interconnect (ii) Three-arc interconnect (iii) Four-arc interconnect [Lee et al, 2011]

The current research work being conducted will make use of the three-arc multi-path compliant interconnect design for all its experimental tests and simulations.

2.3 Drop testing

As was mentioned in the previous chapter, drop testing is a very important aspect of microelectronic package reliability. Drop testing allows one to determine the response of the given package when subjected to extremely high loads over very short durations of time. In effect, impulse loads are applied on the package and its performance is studied

before, during and after the impulse load has been applied. A reliable microelectronic package will not display any adverse effect due to the impulse load and will function with at least the same or slightly reduced efficiency, but will not stop working all together. Drop testing also allows the determination of the maximum stresses and strains which the package will experience during the impulse loading event, allowing the replacement of currently used materials for more robust, impact-resistant ones.

2.3.1 JEDEC Standard for drop testing

For many years, there was no set standard for conducting repeatable and reliable drop tests on microelectronic components. To address this issue, in July 2003, the Joint Electron Devices Engineering Council (JEDEC) established a standard for board-level drop test reliability (JESD22-B111) which specified the conditions for conducting repeatable drop tests. The basic procedure involved the mounting the sample to be tested on top of a drop test table. The drop test table would be raised to a suitable height and dropped under free-fall along guide rods and be made to impact a rigid surface underneath it. The resultant impact would create a shock, which would travel upward through the drop test table and into the sample, simulating a drop event. This technique was called the 0° JEDEC standard drop test. The specific impulses that had to be imparted were specified in a subsequent standard last revised in November 2004, called Subassembly Mechanical Shock (JESD22-B110). The above two standards combined would pave the way for what the industry deemed reliability in drop testing. Shown in Figure 2.9 is a schematic of the basic JEDEC standard drop test setup.

Before JEDEC established the currently used drop test standards, attempts were made to quantify drop testing in terms of mathematical equations. Drop testing is a highly

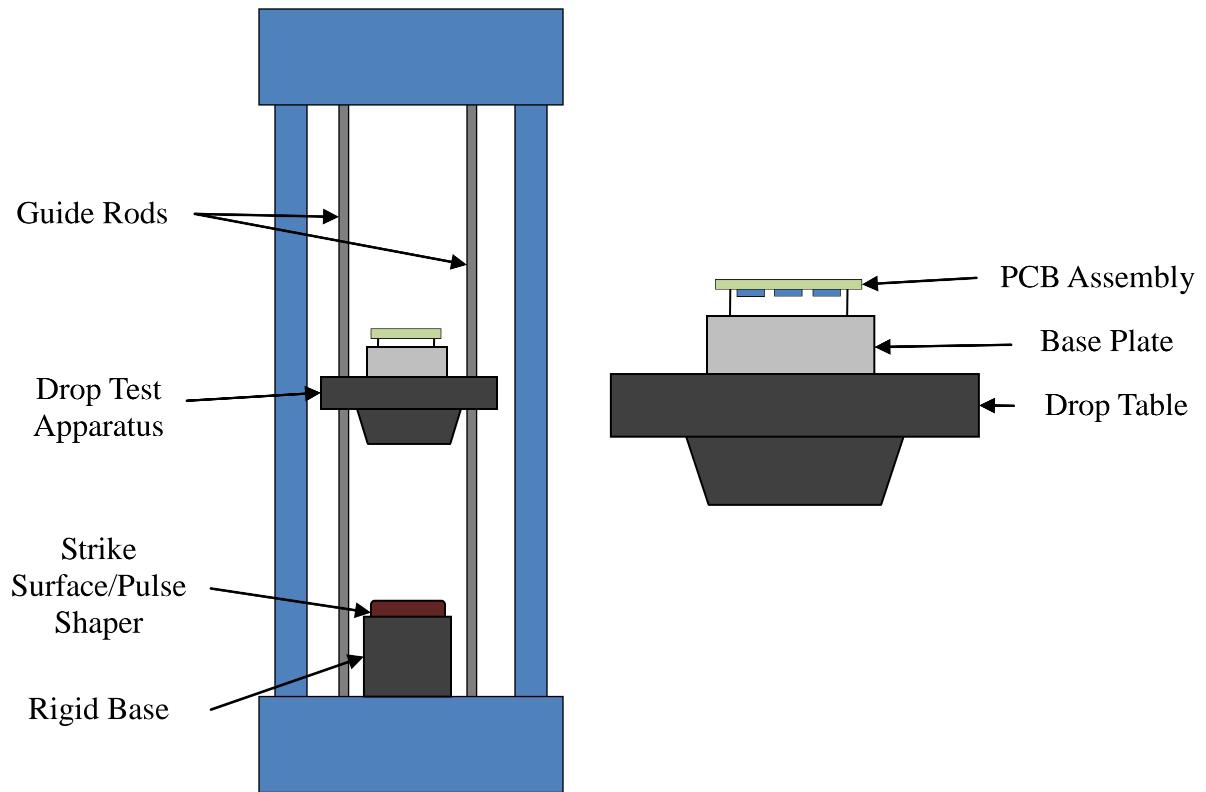


Figure 2.9: JEDEC standard drop test setup schematic

nonlinear event, involving large deformation occurring over very short durations of time. To understand this, researchers at AT&T Bell Laboratories developed a basic mathematical formulation to explain nonlinear dynamic response of printed circuit boards, when subjected to shock loading [Suhir, 1991]. While this mathematical formulation seemed correct, it was not until after the JEDEC standards were established that these formulations could be verified. The last revision of this formulation allowed the understanding of impact pulse generation as seen in the JEDEC standard [Suhir, 2010].

While mathematical formulation by and of itself was validation enough, experimental proof allowed a better visual understanding of the drop test phenomena. Several researchers have undertaken the task of conducting and understanding drop tests experimentally. These experiments generally take a very long time to setup and conduct,

due to the complex nature of the parts fabricated, the pre-calibration of the machine and the associated post-processing of data needed after the tests are conducted. It was generally agreed that conducting simulations of the drop test event would speed up the understanding of the drop test phenomena for microelectronic packages.

Drop testing, being a highly nonlinear event, required that any simulation that was done should be able account for the extremely large deformation experienced by the package over a short duration of time. For this purpose, explicit finite-element simulation solvers were found to be more suitable compared to implicit solvers. Thin-profile fine-pitch BGA (TBGA) and very-thin-profile fine-pitch BGA (VTBGA) packages were experimentally tested by Tee and others, using the JEDEC-specified 1500G impact acceleration, the results being used to validate explicit simulations conducted using ANSYS®/LS-DYNA® [Tee et al, 2003]. Drop tests on ball-grid arrays (BGA) , quad-flat no-lead packages (QFN) and conduction-cooled ball-grid arrays (C2BGA) were conducted based on the testing methods given in JEDEC standards and subsequently used to validate explicit finite-element simulation data obtained using ABAQUS® explicit software [Lall et al, 2004, 2006]. Chip-scale packages (CSP) were studied for varying pad configurations like NSMD (non-solder mask defined) [Pan et al, 2006]. The CSP experimental results were validated using ANSYS®/LS-DYNA® explicit solvers. Reliability models based on failure envelopes, Digital Image Correlation (DIC) and explicit submodeling were developed and studied for various BGA configurations [Lall et al, 2005, 2009]. Some researchers departed from the drop test sample dimensional specifications specified by JEDEC to conduct their drop testing. It was claimed that using the circular drop test printed circuit board assembly (instead of the rectangular board

specified in JEDEC standard JESD22-B111) would lead to more uniform stress and strain levels during the drop event. Nevertheless, these experimental results were used to validate finite-element simulations conducted on BGA packages using ABAQUS® Explicit.

While the data obtained from explicit simulations was accurate and found to be sufficient, there existed the case in industry of lack of access to explicit solvers. Finite-element simulation software usually came with only the implicit solver, the explicit solvers being an expensive add-on feature. To try and make use of available resources, researchers at STMicrolectronics, Singapore developed an implicit finite-element formulation for conducting drop tests. The JEDEC standard was used to develop mathematical equations which would allow one to use readily available implicit solvers to conduct drop tests [Luan et al, 2004]. Known as the Input-G Method, this technique gave rise to several studies on drop test reliability of microelectronic packages. Luan and Tee showed how simplification of the JEDEC standard drop test model would allow the use of implicit formulations in conducting drop test simulations. Fueled by this, Tee and others also developed several other drop test simulation techniques, weighing the pros and cons of each and proving the reliability of the Input-G Method [Tee et al, 2005]. They conducted drop tests on electronic devices such as PDAs as well as BGA packages and determined the location of critical solder joints. Around the same time, Irving and Liu developed their own implicit transient dynamics methodology to conduct drop test simulations on the Fairchild 6 lead Micropak™ [Irving et al, 2004].

While all the above drop testing methodologies are valid and have been proven, a general trend can be seen. There is next to no information on drop test reliability of

compliant interconnects themselves. Indeed, one of the only studies done on compliant interconnect drop testing is by Yuan and others at Guilin University of Electronic Technology, China, where they studied the effect of drop testing on Compliant Wafer Level Packages (CWLP) [Chaoping et al, 2009]. They combined the Input-G Method and explicit ANSYS®/LS-DYNA solvers to obtain their drop test results, stating that their design allowed the compliant nature of their copper arm interconnects to relieve stress between the chip and bump pad, effectively increasing assembly reliability.

CHAPTER 3

OBJECTIVES AND METHODOLOGY

As can be seen from the previous chapter, a lot of drop testing research has been conducted on BGAs, CSPs and other variants of solder-bump based packages. Very little information is available in published literature on response of compliant interconnects when subjected to drop testing. Thus, there is a definite need to understand the drop test reliability of such compliant interconnects. With this in perspective, the objectives of this thesis are as follows:

- Develop a drop testing methodology which can be applied to any compliant interconnect structure
- Understand and establish the drop test reliability of the three-arc multi-path compliant interconnect in particular
- Develop an alternative drop test method which can provide a quick low cost preliminary alternative to drop testing of photolithography-based structures
- Develop finite-element models to mimic drop testing and to validate the results of the FE models with experimental data Suggest improvements in the compliant interconnect structure by parametric comparison against other common designs
- Determine possible alternative uses for the given three-arc multi-path compliant interconnect structure

To achieve the objectives of this work, the following approach or methodology was employed.

- Drop test prototypes of the compliant interconnects with associated die and substrate were fabricated using stereolithography. This was done since the cleanroom-based fabrication steps needed for photolithographic fabrication of the compliant interconnects were still in development.
- The prototypes were appropriately scaled up to preserve the width, thickness, height, pitch and other dimensions of the compliant interconnect. The substrate and die dimensions were decided based on the scaling of the interconnects, limitations of the testing machine and appropriate standards.
- A drop test setup was developed which would accommodate the fabricated samples. Drop tests were conducted for different drop heights using the fabricated samples. Accelerometers and strain gauges mounted on the sample were used to measure and collect output data.
- Simultaneously, finite-element simulations were carried out to obtain numerical drop test data for the fabricated interconnects. The finite-element results were validated using the obtained experimental data.
- Comparisons were made between the proposed compliant interconnect structures and conventional bump interconnects, keeping the dimensional scaling in mind.

The following chapters present different aspects of the research work conducted. Chapter 4 deals with stereolithographic fabrication and experimental drop testing of the complaint interconnects. Chapter 5 presents the methodology behind the drop test finite-element simulations conducted. Chapter 6 presents the results obtained from both experimental drop testing and finite-element drop test simulations, with appropriate comparisons and validation of data. Chapter 7 will deal with finite-element simulation of the proposed compliant interconnect structure using the original scale and materials. Finally, conclusions and future work will be given in Chapter 8.

CHAPTER 4

DROP TESTING OF COMPLIANT INTERCONNECTS

The experimental aspect of this thesis research work involved conducting drop test experiments on interconnect samples fabricated using suitable techniques. The testing procedure used for the experimental testing aimed to follow basic JEDEC guidelines [JESD22-B111, JESD22-B110a] suitably modified to take into account availability of fabrication equipment and testing limitations. The basic JEDEC standard board-level drop test consists of a controlled 0° drop of a given board with assembled packages, where the 0° notation refers to the orientation of the board with respect to the underlying drop table. The schematic for this type of 0° drop test is given in Figure 2.9 and is based on JEDEC standards

In a typical drop test, the PCB test board with assembled packages is mounted on a drop test table using spacers. The spacers raise the board above the drop table. By doing this, the test sample is supported at its four corners, allowing the rest of the sample to flex freely during the actual drop event due to experienced acceleration and inherent inertia of the board material and assembled packages. This also isolates the effect of the acceleration experienced by the board during the drop event, allowing higher accelerations to be obtained from different drop heights. The board is mounted in such a way that the assembled packages are below the board, closer to the drop table than the board itself. Suitable accessories needed for measurement and data collection are attached to the sample to be tested. These include strain gauges mounted at appropriate locations (to measure changes in strain along different directions of the board and package

surface), accelerometers (to measure acceleration and board deflection) and electrical probes (to measure resistance change in the actual package). The drop table with mounted test sample is then raised to specified drop heights and then released under controlled free- or accelerated-fall onto a rigid surface. Uniformity of the free-fall is maintained by making use of guide rods which allow the drop table to fall in only one orientation. The impact of the drop table on the rigid block beneath it creates a mechanical shock, which travels upwards through the drop table material, through the base-plate, through the mounting spacers used to support the board and then to the test sample. In order to relieve the shock, and additionally due to its own inertia, the test board will flex about its mean position. This flexing action takes place over a very short duration of time (typically over 5 ms to 100 ms, depending on the board material under test) and is of very high frequency. This high frequency flexing leads to the generation of stresses and strains in the packages mounted on the underside of the board. This entire process makes up a single drop event. This is the basic procedure behind a JEDEC standard 0° board-level drop test [JESD22-B111].

The above explained drop test procedure makes use of a fully assembled package, with suitable wiring for the interconnections to be powered through. The work presented in this thesis aims to determine the drop test reliability of the multi-path three-arc compliant structures used as first-level interconnects by fabricating, assembling and subsequently testing the actual copper-silicon interconnect-die assembly package. However, the fabrication of the actual copper-silicon interconnect-die assembly package is still underway. Therefore, in order to understand the drop test behavior of this particular compliant interconnect design in the interim, an alternative test sample was

fabricated and utilized to conduct the drop test. The methodology, reasoning and procedure used to obtain this alternative sample will be explained in the following paragraph.

The original copper-based multi-path compliant interconnects are supposed to be fabricated using a multi-layer photolithography process using basic cleanroom tools. This cleanroom-based fabrication process is still under development. In order to develop an alternative to understand the drop test behavior of the multi-path compliant interconnects, an alternative to the photolithographic fabrication procedure used in the cleanroom was sought. It was determined that stereolithography (or rapid prototyping) could be used to fabricate faithful replicas of the required test samples. However, this process could be used to fabricate samples only out of stereolithographic polymer, which would allow the samples to mimic the physical behavior of the required compliant interconnects due to similar geometry, deeming rapid testing and experimentation of the interconnect geometry's behavior possible. The process of stereolithography is explained in more detail in the following sections.

4.1 Sample fabrication

4.1.1 Stereolithography

Stereolithography (also known as Rapid-Prototyping) is a rapid fabrication technique used in industry and research to develop prototypes of three-dimensional models in order to gauge response behavior that cannot be predicted through mathematics, simulation or other numerical techniques. The process of stereolithography requires the use of a three-dimensional computer-aided design (CAD) model of the prototype to be fabricated. This CAD model is used as input into the stereolithography

machine by suitably converting it into the required file format, usually an .STL file. The .STL file, upon being entered into the stereolithography machine's software, gets manipulated and altered by the software. The associated CAD model gets cut up into virtual 'slices' or layers as shown in Figure 4.1. These layers when stacked on top of each other form the whole CAD model.

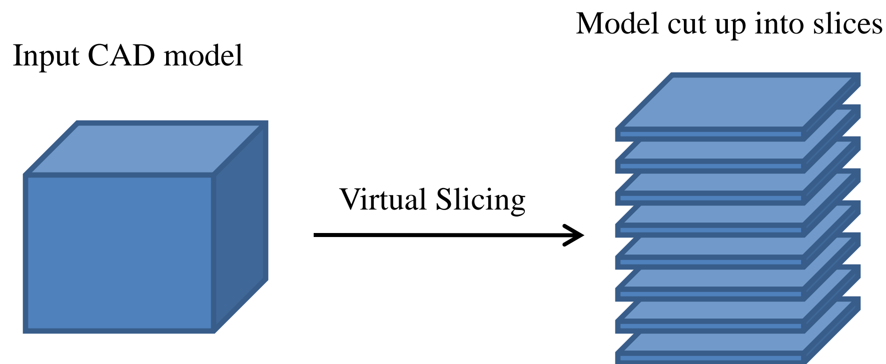


Figure 4.1: Virtual slicing of input CAD model

The stereolithography machine utilizes a light-sensitive polymer resin as raw material for building is prototypes. This light-sensitive polymer is reacts to the beam of a computer-controlled UV light source, usually a laser, which focuses its beam on the liquid polymer and partially polymerizes it, allowing the resin to harden and take on the required three-dimensional shape. This procedure is used to build each layer or 'slice' of the CAD model using a bottom-up approach. After the first layer or 'slice' of the CAD model is fabricated, the second layer is built directly on top of it. This process is continued till the entire three-dimensional part is fabricated. This procedure allows for the generation of complex three-dimensional shapes using the machine's homogenous polymer resin material. Free floating surfaces can also be generated by making use of suitable support structures, which are usually automatically generated by the stereolithography machine's software. After generation of all the layers, a workable

three-dimensional replica of the input CAD model is obtained, though it is still unfinished and cannot be used directly for testing. This polymer model is removed from the fabrication chamber, cleaned using solvents to dissolve unwanted liquid polymer resin left on the polymer prototype and subjected to ultraviolet (UV) light to fully polymerize, cure and obtain the required prototype. The accuracy of the part's dimensions depends on the resolution of the given stereolithography machine; this resolution is a function of the workability of the polymer resin raw material (specified in terms of part build layer thickness in the material property data sheet for the given polymer resin) and the resolution of the UV light source used to partially polymerize the light-sensitive polymer resin (diameter of the UV laser beam).

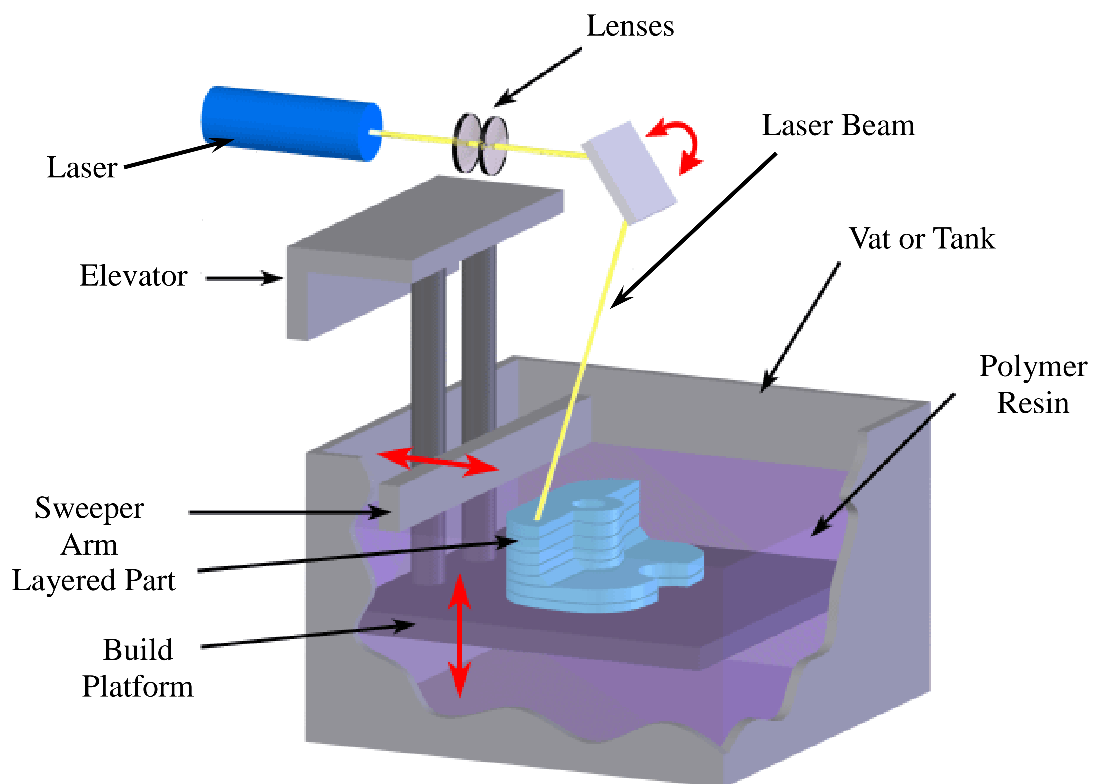


Figure 4.2: Stereolithography/Rapid Prototyping process (courtesy CustomPartNet)

In the current research on drop testing of three-arc compliant interconnects, it was proposed that stereolithography be used to fabricate these complex three-dimensional compliant interconnect structures using an overall package geometry that takes into account the limit of resolution of the available machine, repeatability of the fabrication process, material used for fabrication and ease of testing of the fabricated model used in the actual drop test. The following sections are devoted to explaining the various tools, processes and procedures involved in the actual sample fabrication process.

4.1.2 Viper® SLA^2 Stereolithography machine

The machine selected for the purpose of stereolithographic fabrication of the compliant interconnects was the Viper® SLA^2 series stereolithography machine. Similar

Figure 4.3: Viper® SLA^2 stereolithography machine

to most stereolithography and rapid prototyping setups, this machine makes use of an ultraviolet (UV) sensitive polymer resin and a computer-controlled UV laser to generate three-dimensional replicas of the input CAD models.

The machine consists of a fabrication chamber which houses a tank containing the UV-sensitive resin, a moveable and detachable fabrication plate with drain holes is held within the tank (the drain holes allow excess resin to flow out after fabrication is completed), associated guide frames to allow the fabrication plate to move up and down inside the chamber and within the resin-tank and a computer-controlled UV laser used to generate the three-dimensional geometry of the model. The fabrication chamber has a safety door to prevent operation of the machine when being loaded or unloaded and an exhaust system to drive out the fumes given out by the polymer resin. The fabrication chamber is linked to a computer with appropriate software, which is used to manipulate the CAD model before being used for fabrication and to control the operation of the entire machine. Figure 4.3 shows the Viper® SLA2 stereolithography machine used for the fabrication of the currently studied interconnect samples.

4.1.3 Stereolithography material: RenShape™ SL 7510

The Viper® SLA^2 series of stereolithography machines makes use of a specific light-sensitive polymer resin created specifically for its use, known as RenShape™ SL 7510. The material properties associated with this polymer resin are given in Table 4.1 and were obtained from the RenShape™ Material Database [RenShape™ MSDS]. Held in the tank lying within the fabrication chamber, this polymer resin can achieve a layer thickness of as small as 0.025 mm. While this layer thickness would lead to extremely accurate features, the small value of the layer thickness would lead to exceedingly large

fabrication times and was found to be unnecessarily fine. The required drop test samples could be fabricated just as easily with larger part layer resolution. Therefore, a layer thickness of 0.1016 mm (101.6μ) was utilized as the part build layer thickness. This was done by setting the step height of the fabrication table movement to 0.1016 mm using the attached computer interface. Incidentally, this was the smallest achievable step height for the given model of the Viper® SLA[2] stereolithography machine.

One drawback noticed during fabrication and subsequent testing was that the material properties of the UV-exposed polymer tended to degrade with time. In other words, polymer ageing was an issue over long durations of sample storage [Hutchinson, 1995]. The fabricated parts would become more brittle with the passage of time, typically a time frame of several weeks when the parts were left idle in an aerated container maintained at room temperature. To ensure this time-dependent deterioration of material properties did not affect the results of the drop test, the samples were

Table 4.1: RenShapeTM SL 7510 polymer resin material properties [Courtesy RenShape™]

Liquid Polymer Resin		
Measurement	Condition	Value
Appearance	-	Amber
Density	@ 25°C (77°F)	1.17g/cm^3
Viscosity	@ 28°C (82°F)	400cps
Part building layer thickness	-	Minimum 0.025mm (0.001in)
Post-cured Polymer Material		
Measurement	Test method	Value (90-minute UV post-cure)
Hardness, Shore D	ASTM D 2240	87
Tensile Modulus	ASTM D 638	2282MPa (331 KSI)
Density	-	1.18g/cm^3

fabricated approximately 24 hours before conducting the drop tests. Data obtained from the drop tests were compared between samples fabricated in the same batch, as well as between different batches. Just the time from fabrication completion to testing was maintained constant between compared samples.

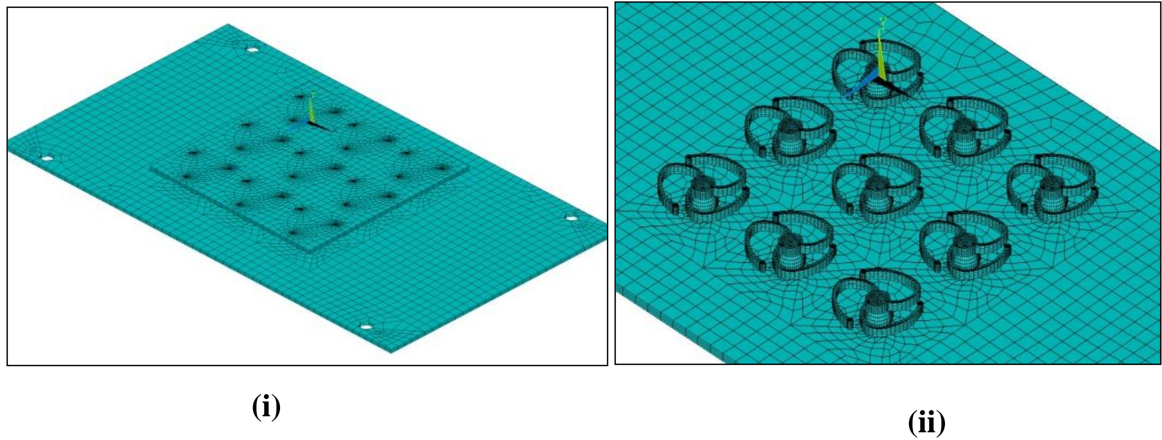
4.1.4. Model Geometry

In order to obtain accurate readings, the three-arc interconnects had to be designed as close to the original size and shape as possible. The compliant interconnects used in the copper-silicon interconnect-die assembly had a footprint of 0.14 mm (140μ) with a pitch of 0.2 mm (200μ). While these dimensions could easily be attained using basic cleanroom photolithographic fabrication, the machine being used here for stereolithography would not allow such small dimensions to be fabricated, without loss of part accuracy.

It was thus apparent that the compliant interconnects could not be fabricated at such a small pitch and footprint using the stereolithography machine at hand. In order to accommodate this, it was decided that the compliant interconnect structures would be suitably scaled up to accommodate the resolution limits of the machine. A scaling factor of 75 was used to scale up the dimensions of the compliant interconnects. This scaling factor was deemed suitable and well within the resolution limits of the Viper® SLA^2 stereolithography machine being used. Therefore, the new interconnects, to be fabricated using stereolithography, had a footprint of 10.5 mm with a pitch of 15 mm.

In order to conform to drop test standards set by JEDEC, the board used for drop testing was selected to be 110 mm long, 64 mm wide and 1 mm thick. The scaled up interconnects were meant to be sandwiched between this board and a 45 mm by 45 mm

square die. Thus, taking into account the new dimensions of the scaled up compliant interconnect structures, a 3 by 3 area array of interconnects was found to be sufficient for fabrication and testing. The board and die dimensions were decided taking into account the dimensions of the testing machine, the scaling of the interconnects and referenced JEDEC standards.



(i) **(ii)**

Figure 4.4: FEM model used to generate 3D CAD model for stereolithography input

(i) **Full model with die and board**

(ii) **Close-up of area-array of interconnects with die removed**

For the sake of uniformity between experimental samples and numerically solved models, the model geometry used for the numerical simulation was exported directly from the finite-element simulation software, ANSYS®, to create the required CAD model needed as input to the stereolithography machine. The final geometry of the proposed sample was taken from the finite-element model depicted in Figure 4.4. It should be noted that the ANSYS® model was also designed with homogenous polymer resin material properties, as was the case of the fabricated experimental test samples

4.1.5. Actual sample fabrication procedure

The process of fabricating the polymer-based drop test samples made use of all the above mentioned tools and processes. As mentioned, the initial CAD model, needed for generation of the .STL file, was exported from ANSYS® in the form of an .IGES file. Using computer-aided design software like SolidEdge®, this .IGES file was converted to the required .STL format, the preferred file format for stereolithography machines.

The .STL file was opened using Buildstation v13, a stereolithography machine software used to control and modify CAD models, where the CAD model was spliced into 'slices' or layers. At this point in the process just before the stereolithography machine would start fabrication, an appropriate support structure had to be determined to support the free-standing portions of the required prototype to be fabricated. Typically, stereolithography models which have free standing structures are fabricated by generating removable supports under the free standing regions. In the case of the current compliant interconnect model, the support structures generated had to be manually selected in order to ensure repeatability and ease of removal. This was extremely important as the gap between the compliant interconnect arms and the board below was 2.25mm, while the gap between the compliant interconnect arms and the die above them was 1mm.

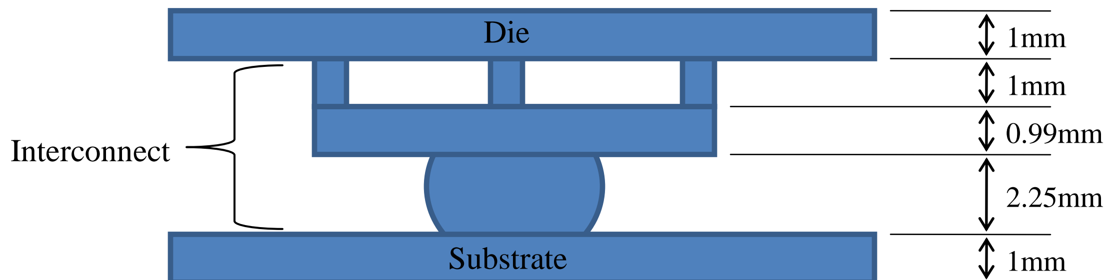


Figure 4.5: Side view schematic of three-arc interconnect with dimensions

After multiple trials, it was determined that the appropriate orientation for fabrication required the support structures to be built between the compliant interconnect arms and the board below them, rather than between the arms and the die. This ensured easy removal of the supports below the arms. Additionally, the computer generated area array pattern of supports for the free standing portions of the die was replaced with a manually entered peripheral arrangement of supports. This was deemed sufficient to prevent the collapse of the die itself during fabrication as well as easy removal post-fabrication of the sample. The support structure pattern used in fabrication is shown in Figure 4.6.

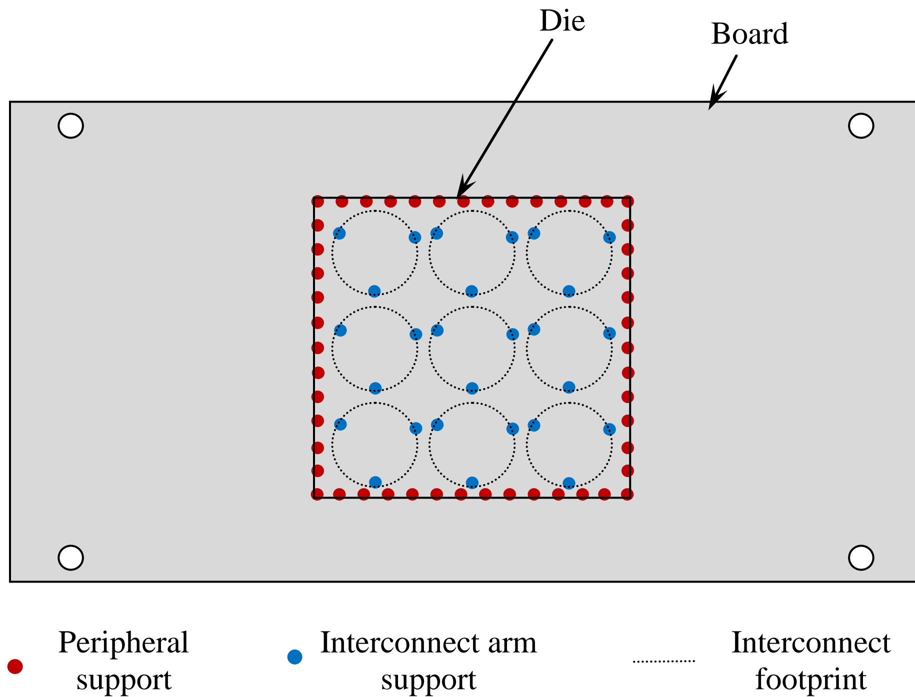


Figure 4.6: Support structure layout used for stereolithographic fabrication

Once the support structure was defined, the part was ported to the computer console of the Viper® SLA^2 stereolithography machine and the required step height and fabrication resolution were selected. Next, the fabrication plate inside the stereolithography machine was removed, cleaned and replaced back into the fabrication

chamber. The level of the polymer resin in the tank inside the fabrication chamber was checked and topped up if necessary. Finally, the safety door was closed and locked and the computer console was used to start the fabrication process.

4.1.6 Post-fabrication treatment and processing

After the sample fabrication procedure was over, the samples were removed from the fabrication plate using a flat chisel. Precision scissors were used to cut away the support structure below the entire sample, followed by the cutting of the supports below the die and the compliant interconnect arms. This was followed by immediate immersion in a methyl alcohol bath for 5 minutes, allowing the excess unpolymerized resin left on the sample to dissolve and wash away. Care had to be taken at this point to prevent the sample from being submerged in the methyl alcohol bath for too long, as this would cause the polymer material to breakdown and soften, rendering the sample useless for testing.

After removal from the methyl alcohol bath, all the samples were washed with running water and scrubbed with a cleaning brush to remove any precipitate formed on the samples. Finally, the samples were patted dry and placed in a UV oven for curing. Each sample was subjected to a 90 minute post-fabrication UV bake to cure the polymer completely and finish the entire fabrication process. A flowchart depicting the fabrication process is given below.

The required time for fabrication of a single sample was approximately 2.5 hours. With optimum settings, it took 4 hours to fabricate a given sample from the initial input of the CAD model into the stereolithography machine, all the way to the end of the post-fabrication UV-exposure step. This time was optimized by fabricating up to 3 samples in

each run. This was done in order to save overall fabrication time and also to ensure uniformity of material properties of the samples used in a single drop test run. This allowed easy removal of samples and reduced the overall fabrication time. The latter was possible because each sample fabrication required the machine to build a support structure with a height of 0.4 inch (10.16mm) below the actual part geometry to be

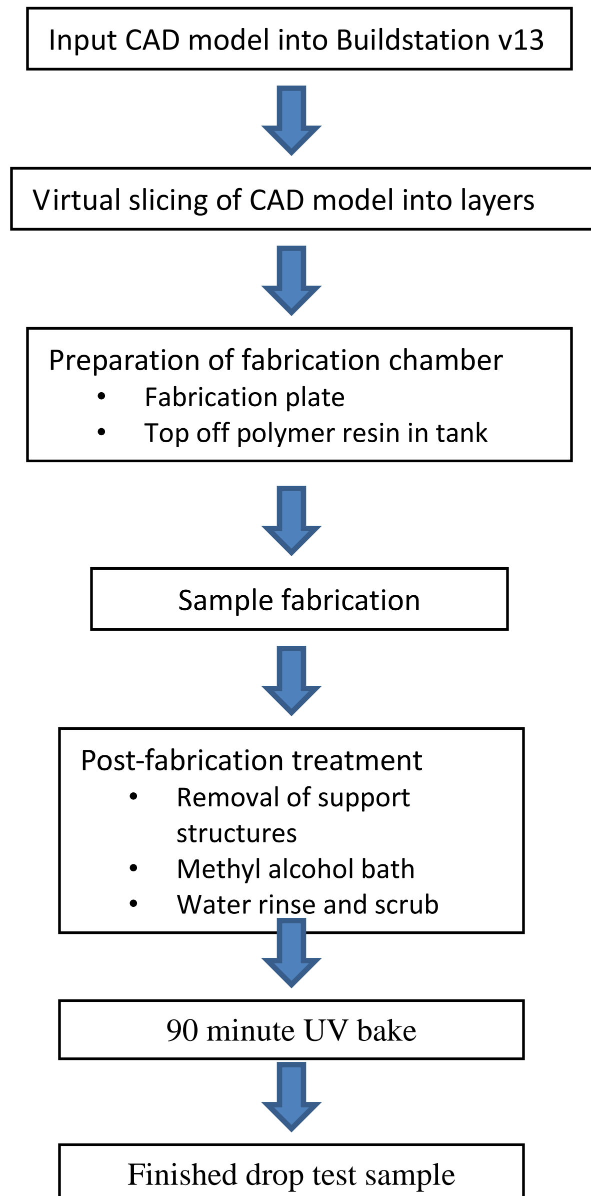


Figure 4.7: Fabrication process flow

fabricated. By fabricating multiple samples together, the time required to fabricate the initial support structure was saved for individual samples.

Figure 4.8 shows the fabricated three-arc interconnect drop test sample. Figure 4.9(i) shows an inverted die with attached three-arc interconnects while Figure 4.9(ii) shows a single interconnect attached to the board. Figure 4.10 shows the fabricated bump interconnect drop test sample.

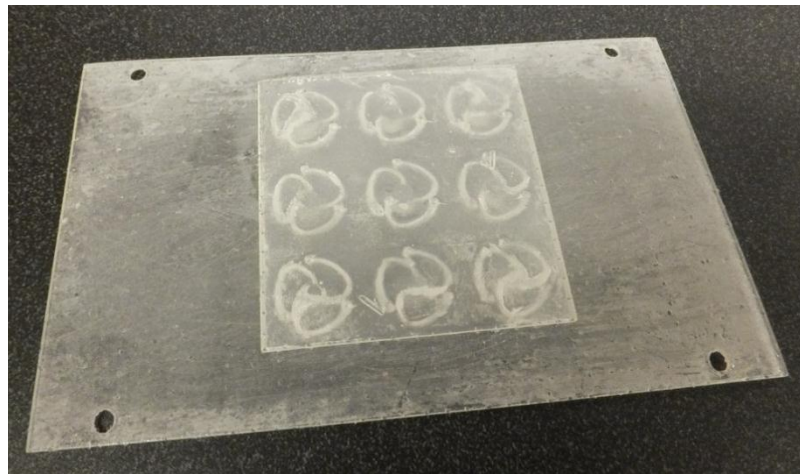
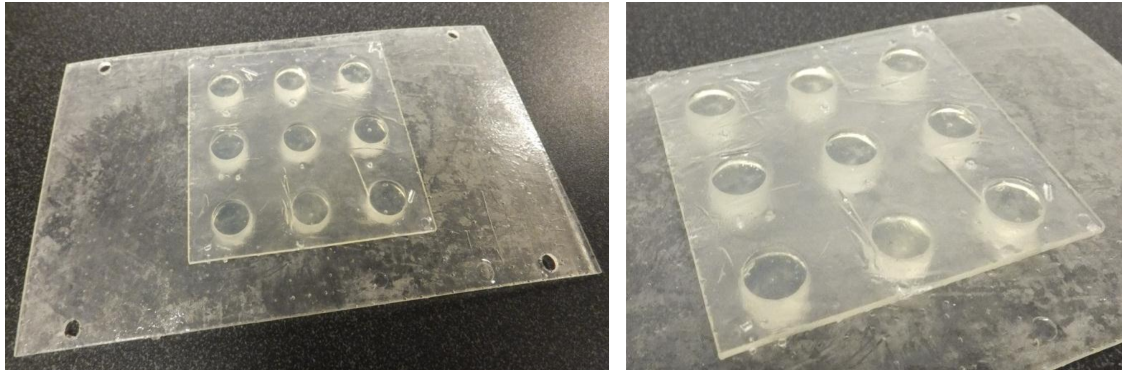


Figure 4.8: Three-arc interconnect drop test sample

(i)

(ii)

Figure 4.9: Three-arc interconnect drop test sample – (i) Inverted die with attached three-arc interconnects (ii) Close up of a single three-arc interconnect



(i) **(ii)**

Figure 4.10: Bump interconnect drop test sample – (i) Drop test sample (ii) Close-up of bump interconnect package

4.2 Experimental setup

Once the samples had been fabricated, the actual drop testing was conducted. The various aspects of the experimental setup used for the drop testing are explained below in the subsequent sections.

The traditional drop test for board-level microelectronic packages is performed using the JEDEC standard for board-level drop testing (JESD22-B111). As explained in the literature review, the board-level drop test standard requires the use of a drop tester which can impart the required acceleration impulse on impact and suitably control the damping of the sample after the impact. Alongside the drop tester, appropriate measurement accessories are required which can adequately measure and record the drop test data, without aliasing the information collected from the sample during the drop test event. Finally, filtering techniques may be used to remove the high filter noise present in the output data. Each aspect of the drop test setup is explained in the following sections.

4.2.1 Instron® Dynatup 8250 drop weight impact tester

The Instron® Dynatup 8250 drop weight impact tester is a testing machine designed to conduct impact reliability testing of a given material. Shown in Figure 4.11,

the Instron® Dynatup 8250 consists of a central chamber with built in crosshead and tup. The impacting action can be accelerated by altering the amount of weight that is attached to the crosshead. The crosshead, tup and weight are housed within a safety chamber to prevent accidents. Below the crosshead and tup, a rigid surface is available which can be used to place and mount suitable clamping devices for different models to be tested. This chamber is supported underneath by rigid supports bolted firmly to the ground to transfer excessive shock to the ground, and prevent damaging the other movable parts of the system. In the current experimental setup, foam cushions were used to obtain the required damping of the test sample after the drop event.

Figure 4.11: Instron® Dynatup 8250 drop weight impact tester

The working procedure of the Instron® Dynatup 8250 is as follows. The material whose impact strength is to be determined is placed on the stand provided inside the testing chamber. The crosshead with attached tup (which impacts the material to be

tested) is raised to a known height using the provided control pendant, which can manually raise, lower and release the crosshead and attached tup. Once raised to the appropriate height, the crosshead is released through the action of a pneumatic clamp, and the crosshead with attached tup falls under gravity. The tup impacts the material to be tested with a force that is relative to the height from which the crosshead is dropped. A built-in load cell inside the tup measures the impact force values, while a tab fixed to the side of the crosshead activates a detector which is used to determine the velocity of the tup just before impact. The results are ported to the Instron® Dynatup 8250 software module where calculations can be done to obtain whichever data item is needed.

While the above mentioned procedure is the typical standard test method used to determine impact strength, the Instron® machine had to be modified in order to be used for the JEDEC standard drop test required for the current research study.

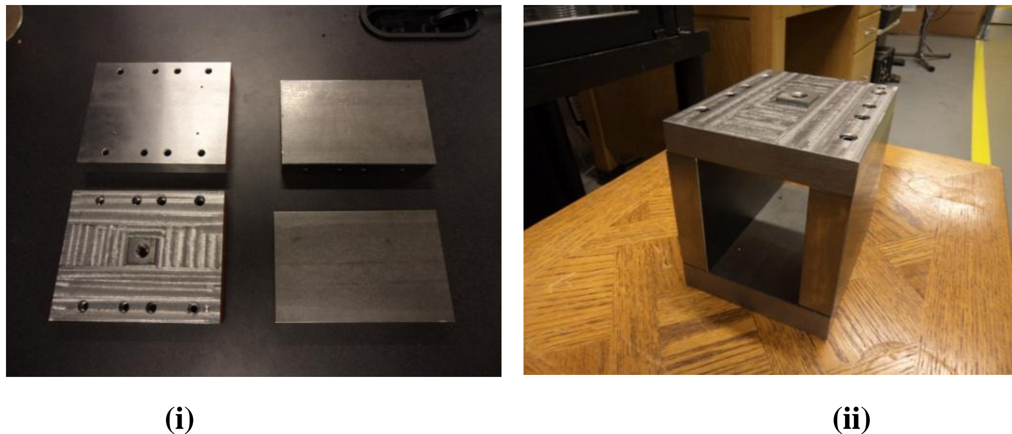
4.2.2 Drop test fixture

The JEDEC standard states that an appropriate drop-table surface must be available in order to faithfully perform a drop test on microelectronic components. The Instron® 8250 Drop Weight Impact tester explained in the previous section is normally used to conduct impact tests on material slabs and structures. As such, the machine had to be modified in order to accommodate a JEDEC-standard drop test.

It was proposed that the drop-weight action of the Instron® machine could be used to perform the standard JEDEC drop test if an appropriate surface for mounting the samples could be attached to the machine. In order to accomplish this, a custom drop test fixture was designed and fabricated, which would act as the drop table surface. A similar

method has been used by Zhou et al to conduct drop tests using the Instron® impact testing system [Zhou et al, 2009 IEEE].

The drop test fixture that was designed consisted of four slabs of impact-resistant Chromium-Molybdenum steel. The dimensions of the fabricated test fixture were decided keeping in mind the space available inside the Instron® machine chamber. The final structure formed a box with a base used for mounting the samples using screwed-in stud mounts or spacers, an upper surface with a built-in attachment step for attaching the custom fixture to the Instron® machine's drop-weight crosshead, and two side walls which held the entire structure together and prevented the upper surface from crashing into the sample mounting base. The walls and upper and lower surfaces were held together using 1.5in hardened steel hex bolts. The various parts of the fixture and the assembled fixture itself are shown in Figure 4.12.



(i) **(ii)**

Figure 4.12: Custom drop test fixture – (i) Drop test fixture parts (ii) Assembled drop test fixture

4.2.3 Data Acquisition Module: National Instruments® 9215 DAQ

A National Instruments® 9215 Data Acquisition Module (NI 9215 DAQ) was used in the drop test experimental setup to record the output data. The NI 9215 DAQ has

a 4-channel interface and is able to record up to 100,000 samples per second. This sampling rate was deemed sufficient in order to prevent aliasing of the output signal and would allow even minute changes in strain and voltage to be recorded. The NI 9215 DAQ interfaced directly through a Universal Serial Bus (USB) port with a LabView® program, which was be used to post-process and visualize data as soon as the drop tests were conducted.

Figure 4.13: NI® 9215 Data Acquisition Module

4.2.4 Measurement device: Strain gauges

Strain gauges are measurement accessories used to determine strain changes at a given location. They are usually mounted close to the surface of interest using thin-layered adhesives. In operation, when the surface on which the strain gauge is mounted deforms, the strain gauge undergoes a slight change in dimensions. The electrical pathways present in the strain gauge subsequently deform, giving rise to a change in overall resistance of the strain gauge. This change in resistance is used to obtain strain values using appropriate conversion from output voltage to strain, using equations such as [Murray et al, 1992]-

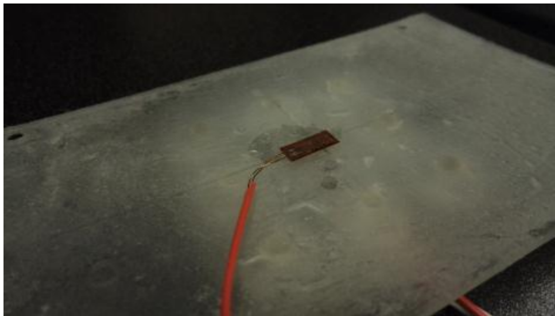
$$\varepsilon = \frac{-4Vr}{GF(1+2Vr)}\left(1 + \frac{Rl}{Rg}\right)$$ **-Equation 4.1**

where ε is Strain, *GF* is Gauge Factor, *Rl* is Lead Resistance in Ω, *Rg* is Gauge Resistance in Ω and *Vr* is a ratio given by the relation-

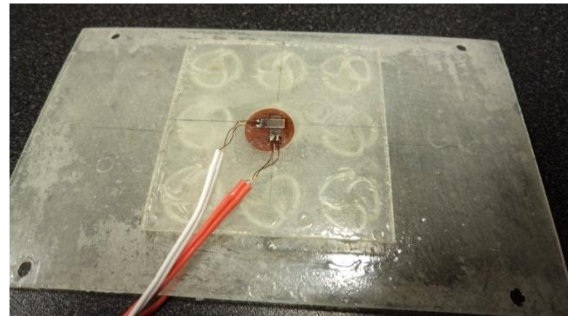
$$Vr = \frac{Vo(strained) - Vo(unstrained)}{Vex}$$ **–Equation 4.2**

where *Vo* denotes Voltage Output and *Vex* denotes Excitation Voltage. The above relations are for a half-bridge Wheatstone network, which was the electrical setup used in the currently presented work.

The strain gauges used for measuring of strains in the current work were of two types. First, linear single-axis strain gauges (with a gauge length of 5 mm, gauge factor of 2.1 and gauge resistance of 351.2 Ω) were mounted at the center of the board. Next, bi-linear 90° rosette strain gauges (with gauge length 3 mm, gauge factor 2.09 and gauge resistance of 350 Ω) were mounted on the chip or die. Figure 4.14 shows both strain gauges in their mounted states.



(ii)



(iii)

Fig 4.14: Mounted strain gauges - (ii)Linear single axis strain gauge mounted on board (SG1) (iii)Bi-axial Tee-rosette strain gauge mounted on die/package assembly(SG2, SG3)

Both strain gauges were pre-wired and were subjected to stress relief during the test by the use of a strain relief bondable pad at the other end of the strain gauges wires.

4.2.5 Power supply

A Hewlett-Packard® Harrison 6201B DC power supply was utilized for powering the strain gauges. The above mentioned strain gauges were powered with a 10V input voltage, which was monitored during the actual impact event. The output from the power supply was fed into the NI 9215 DAQ alongside the strain gauge output voltage data, to allow accurate calculation of the strains reported by the strain gauges.

Figure 4.15: HP Harrison 6201B DC power supply

4.2.6 Measurement device: Accelerometer

A PCB® brand ICP® (Integrated Circuit – Piezoelectric) 352B01 accelerometer was used to determine the impact pulse generated during the drop test from different drop heights. This was done by attaching the accelerometer to the drop test table next to one of the supports used for mounting the drop test samples to measure the impact time. Later on, the accelerometer was relocated onto the board, in order to determine the acceleration experienced by the board during the drop test event. The accelerometer was powered separately using a PCB® Model 480C02 battery-powered ICP® sensor signal conditioner

unit, which would deliver the correct amount of input current to the accelerometer while preventing any extraneous noise from entering the input current signal into the accelerometer. Figure 4.16 shows the PCB® 352B01 accelerometer in its mounted state

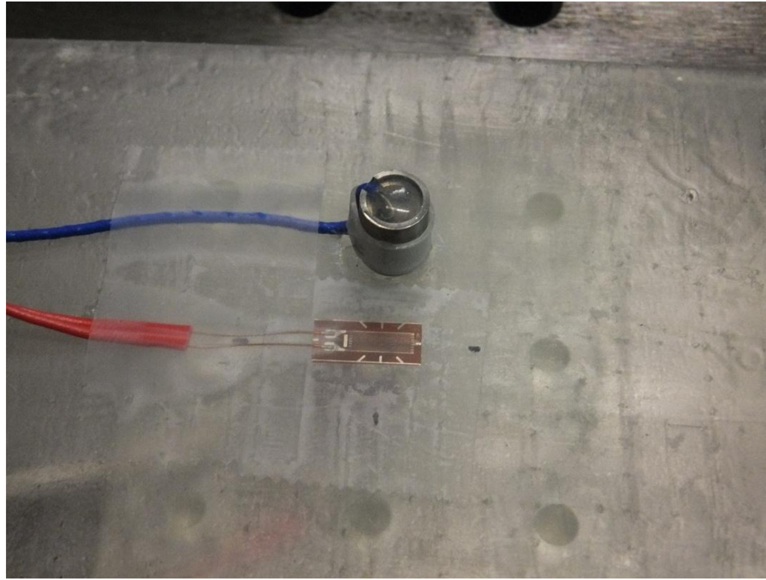


Figure 4.16: Mounted PCB® 352B01 accelerometer next to a linear single-axis strain gauge

alongside a mounted linear single-axis strain gauge.

4.2.7. Analysis software: LabView®

A basic program was written in LabView® to control the NI 9215 DAQ and record the output data. While the NI 9215 DAQ output data was initially recorded in the form of text files, it was determined that some preliminary filtering might give a good idea of the response curve of the strain gauges during the drop test event. A 1000Hz low-pass filter was employed to remove unnecessary high frequency noise for initial visualization and to confirm the proper working of the experimental setup. This gave an idea of the response behavior of the strain gauges, allowing for immediate corrective action in case of faulty readings.

4.3 Drop test setup and procedure

A schematic of the experimental drop test setup is shown in Figure 4.17 with a schematic layout of the setup given in Figure 4.18. As can be seen, the main components are the drop weight testing machine, the measurement devices (strain gauges and accelerometers), the data acquisition module and the analysis software which collects the output from the data acquisition module.

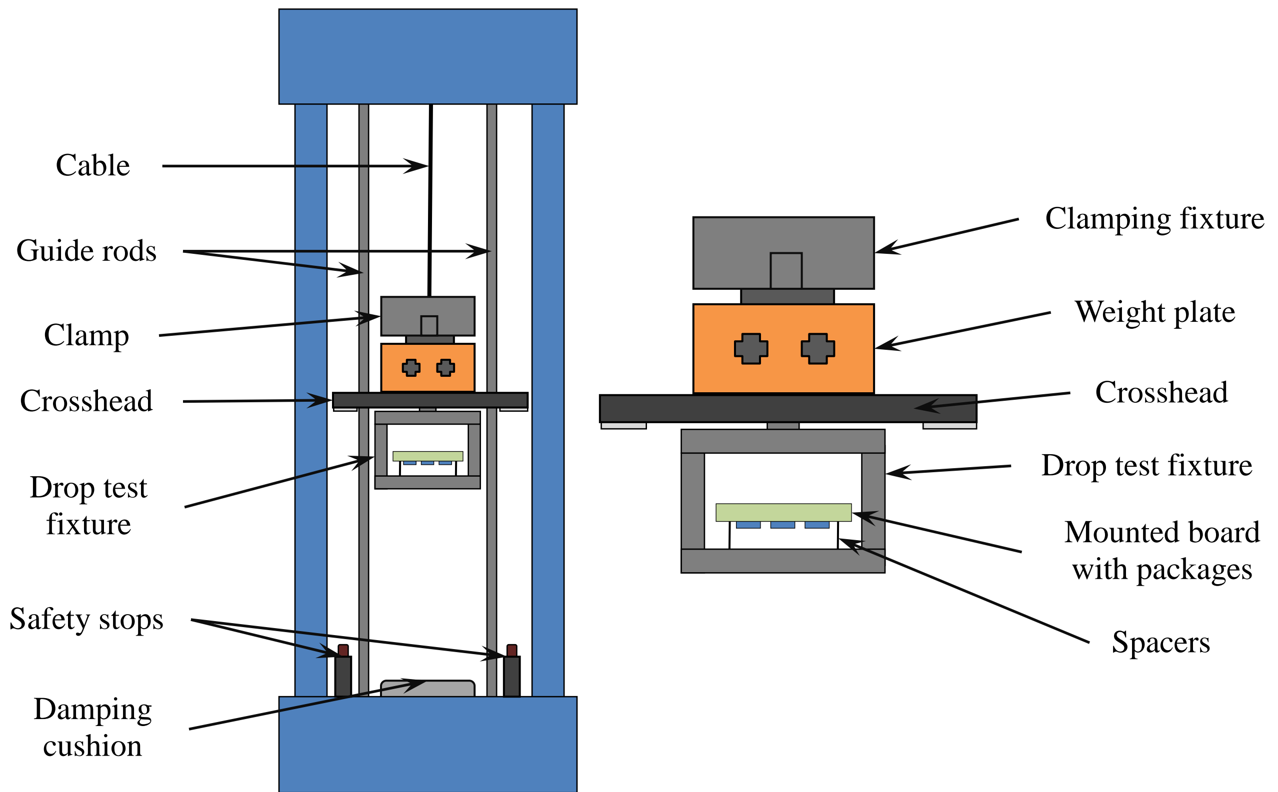


Figure 4.17: Experimental drop test setup schematic

The actual drop test process involved the steps shown in Figure 4.19, which is a flowchart depicting the entire drop test process. The test samples were subjected to an

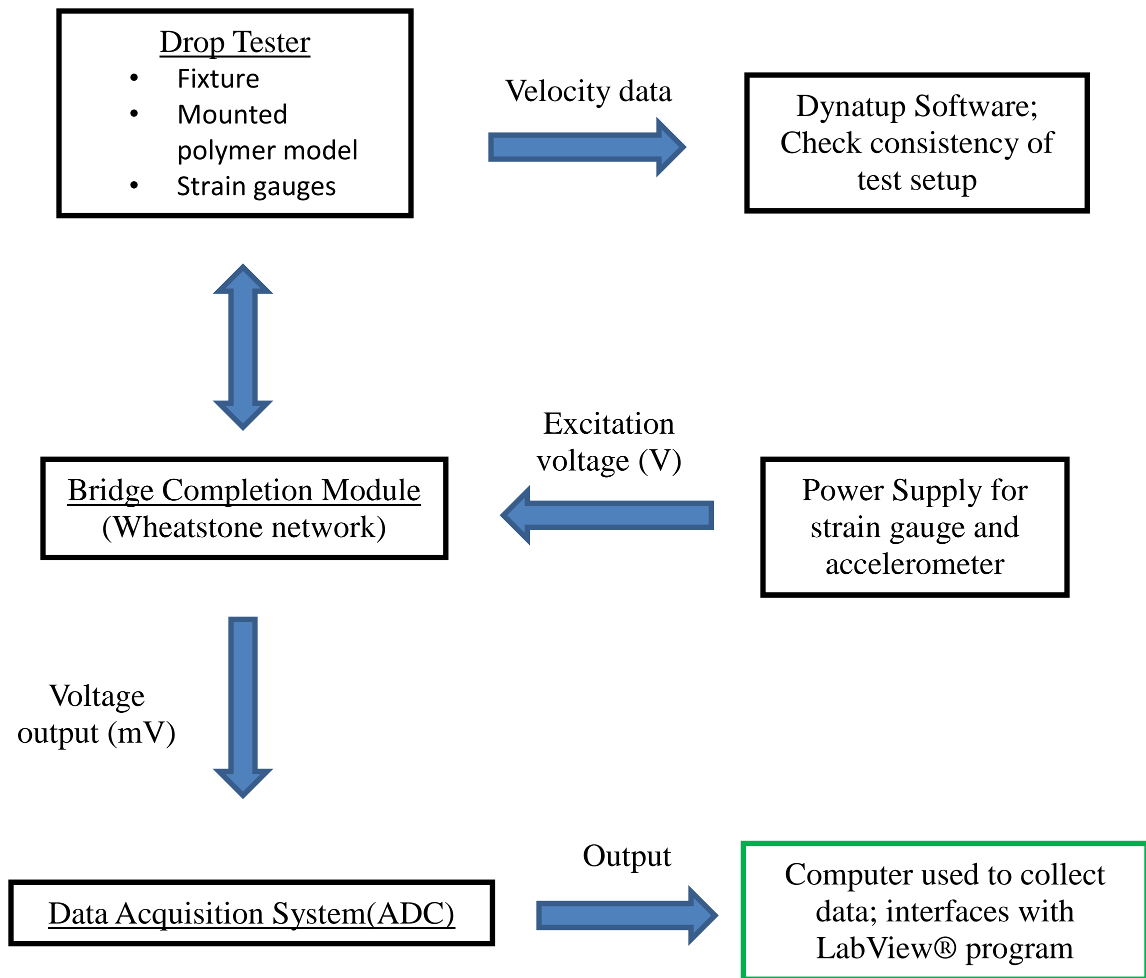


Figure 4.18: Drop test setup schematic

isopropyl alcohol rinse prior to testing, to remove any leftover residue from the fabrication process and clean the surface properly for additional processing. This was followed by a quick 10 minute UV-bake to remove any traces of the isopropyl alcohol and prepare the sample for mounting of strain gauges and accelerometers.

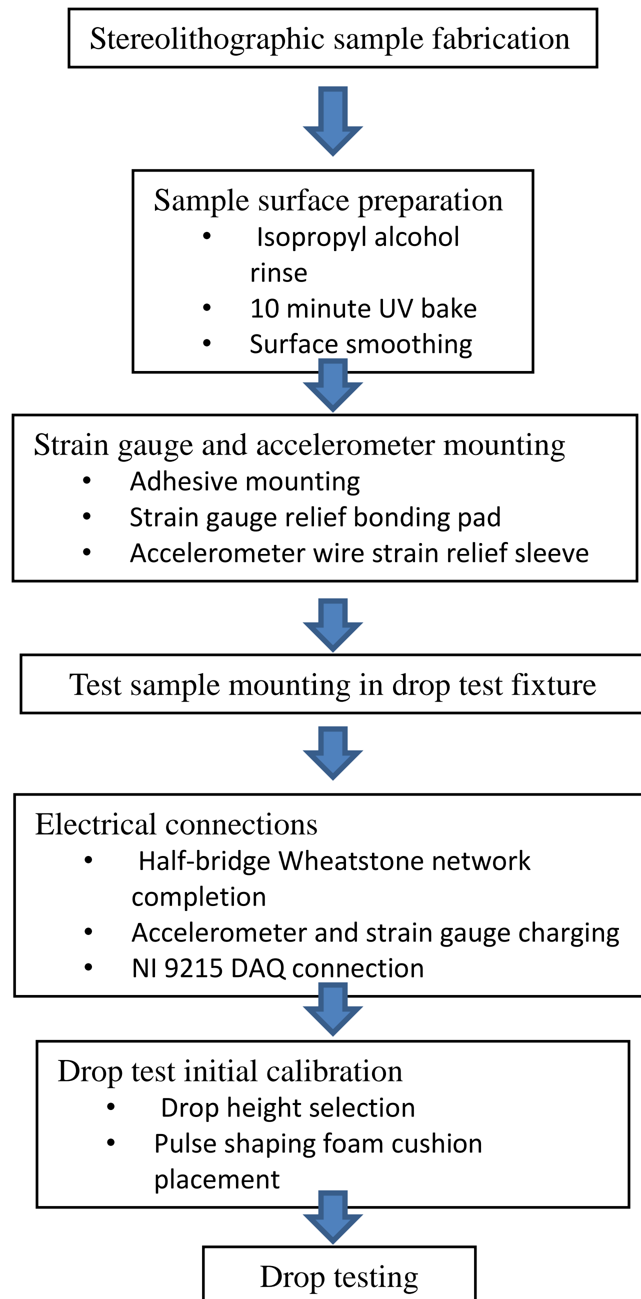


Figure 4.19: Drop testing procedure flowchart

Two locations, as shown in Figure 4.20, were selected for mounting of the strain gauges and accelerometer. Both locations were located on the central region of the sample; one on the die and the other on the board. A linear single-axis strain gauge was mounted on the board with its axis along the longitudinal direction while a bi-directional 90° tee rosette strain gauge was attached at the center of the die, with one strain gauge

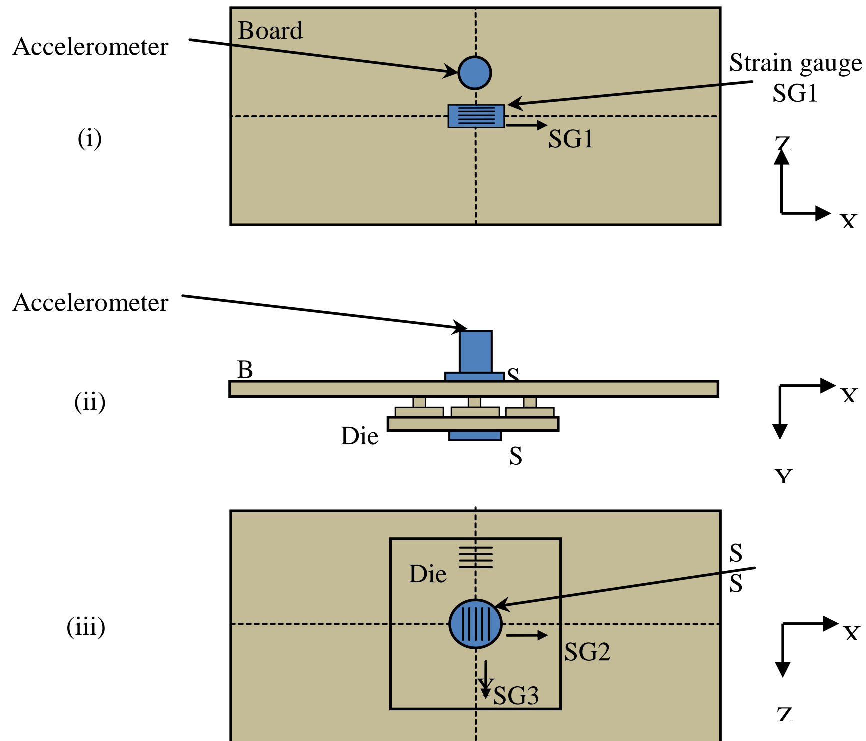


Figure 4.20: Accelerometer and strain gauge positions and orientations

(i) Accelerometer and Linear single-axis strain gauge mounted on board (top view)

(ii)Side view of mounted accelerometer and strain gauges

(iii)Bi-axial Tee-rosette strain gauge mounted on die (bottom view)

axis being parallel and the other strain gauge axis being perpendicular to the longitudinal axis of the board. The mounting surfaces were initially prepared with 21.8 µm / P800 grit sandpaper and cleaned using an ethanol wipe. Loctite® 496 was used as the mounting adhesive for the strain gauges, due to its quick setting time and flexible nature. In order to determine the acceleration experienced by the board, an accelerometer was attached to the sample as well, using Loctite® 454 adhesive.

The sample with attached strain gauges and accelerometer was then mounted on the drop test table base plate using four support spacers, which raised the drop test sample

to the required height above the drop test table. This space allowed the sample to flex above and below its mean position during the actual impact. The drop test fixture was attached to the crosshead of the Instron® machine using appropriate bolts. Using half-bridge Wheatstone networks, the electrical output of the strain gauges was converted to a suitable microvolt output, which was recorded by the NI 9215 DAQ. At the same time, the accelerometer output was also passed into the NI 9215 DAQ so that it could be converted to a digital signal and recorded, similar to the strain gauge output data. The NI 9215 DAQ output was controlled using a Lab View® program written specifically to record, filter and possibly display the output waveforms of the different strain gauges and accelerometers. The voltage output of the power supply used to power the strain gauges was also monitored, in order to get more accurate voltage input readings for calculating the strain output.

Once the connections were completed, the entire drop test fixture was raised to varying drop heights using the controller pendant of the Instron® machine. In order to ensure repeatability of drop heights, a linear graduated scale was attached along the side of the drop test chamber. A movable metal tab was locked into place at different drop heights along this scale and was used to obtain repeatable drop heights. The automatic feature available on the Instron® machine controller pendant allowed the drop test fixture to be raised to a given drop height by using a magnetic sensor mounted on the crosshead. In automatic mode, the crosshead would essentially lift the drop test fixture until the mounted magnetic sensor sensed the metal tab on the graduated scale. Once the metal tab was detected, the crosshead would stop moving, allowing repeatable drops from the same height. This feature also allowed rapid drop testing without further calibration.

Once raised to the required drop height, the controller pendant would be ‘armed’ and the crosshead latch would be released, allowing the drop test fixture to fall under gravity, guided along a vertical path by guide rods passing through the crosshead. Simultaneously, the Lab View® program would be manually activated and allowed to record any and all readings from the strain gauges, accelerometer and power supply. The NI 9215 DAQ readings recorded over a duration of three seconds, and contained data obtained from the measurement accessories during free-fall (before impact), during impact and also after impact.

The identification of the actual impact in the raw data recorded by the DAQ was done in two ways; by manually sifting through the raw data and by the application of filters. During manual sifting, the raw data was plotted without any post-processing and suitable peaks and troughs were determined based on visual inspection. However, this procedure was very cumbersome as the NI 9215 DAQ had a sensitivity of 100,000 readings per second, thereby providing 300,000 data points over three seconds. However, this method was found to be suitable for the determination of impact pulse, since this just involved the determination of the first peak in the data. The usage of filters, on the other hand, made it easier to detect the total impact event in the raw data. The data was initially normalized and then passed through a 1000hz low-pass filter to remove high frequency noise. This allowed one to obtain very distinct curves for the strain output.

4.3.1 Drop heights and sample selection

Based on the capability of the Instron® drop weight impact tester, heights ranging from 100mm to 600mm in steps of 100mm were selected as suitable drop heights for the packages being tested. A graduated ruler was fixed to the frame of the Instron® machine

and was used to calibrate and obtain each drop height for every drop event. For continuous drop testing from the same height, the automatic return feature of the Instron® machine's crosshead was utilized, which would return the crosshead (and attached components) to a specified drop height automatically after each drop event. This maintained the consistency of results obtained from subsequent drops of the same height.

To obtain a proper trend line and prove consistency of results, multiple samples with the multi-path three-arc compliant interconnect design were fabricated and tested. Each sample was prepared using the same method, tools and equipment. All the measurement devices such as strain gauges and accelerometers were mounted in the same locations carefully marked on the specimens. The locations of the strain gauges and accelerometer were explained previously in Section 4.2 of this chapter. Additionally, all the samples were tested at approximately the same times after their fabrication, to ensure polymer aging did not affect the consistency of observed output data.

Of the multiple samples tested, the output strain data was observed and the three samples with the clearest data were used to obtain averaged results. The remaining samples were not considered for averaging due to inconsistencies during the testing procedure, which included incorrect strain gauge and accelerometer mounting (due to insufficient or excessive adhesive usage), insufficient stabilization of the accelerometer output and strain gauge initialization data, and inherently flawed samples which broke within a few drop tests and rendered further drop tests impossible.

4.3.2 Three-arc compliant interconnect model drop testing

As mentioned above, results obtained from three consistent samples were used to obtain strain results from experiment. Each sample was tested at different drop heights, with one drop test at each drop height. The output data obtained from each drop event

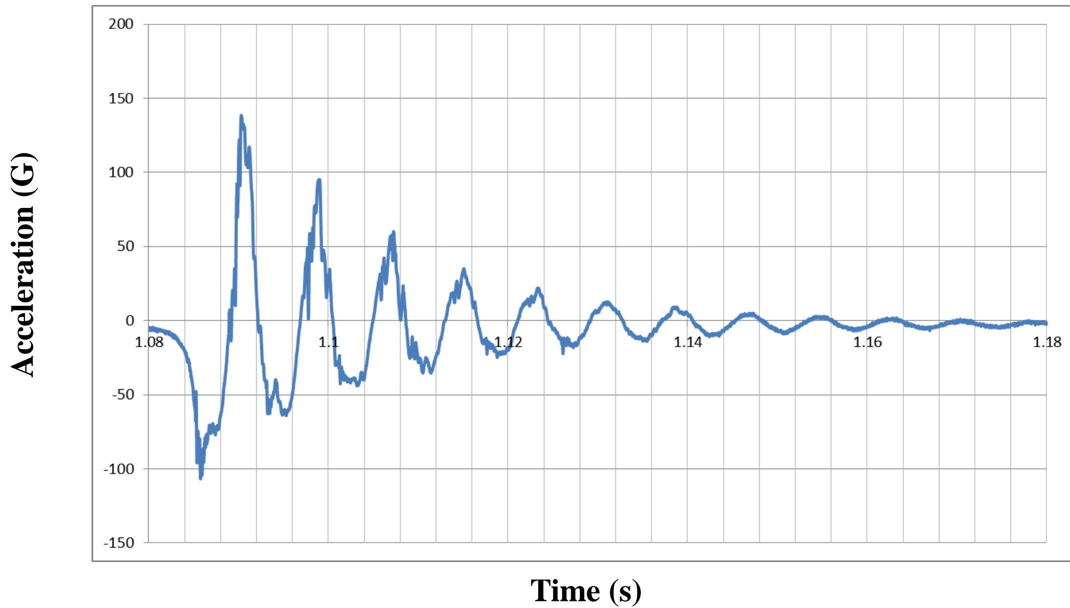


Figure 4.21: Acceleration plot for 100mm three-arc interconnect model drop test (trial 1)

consisted of two plots.

The first plot was obtained from the recorded data of the accelerometer and displayed the acceleration experienced by the sample during the impact event. This data was used to obtain the impact pulse for the given drop height, the magnitude of peak acceleration and the exact damping ratio for that particular drop height and sample. As an example, the acceleration data obtained from a 100mm drop test event is given in Figure 4.21 for a single trial, while Figure 4.22 shows the averaged acceleration data for the 100mm drop test event.

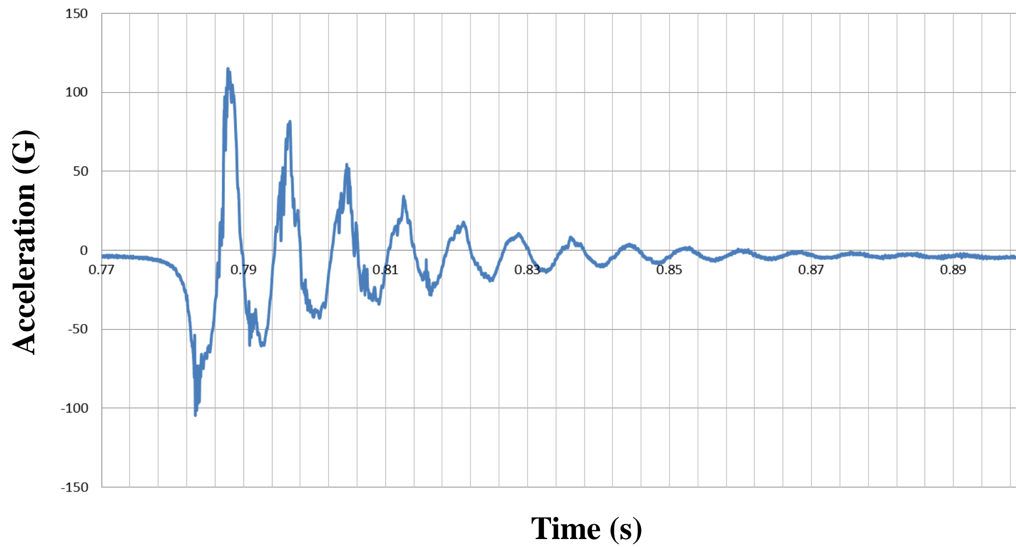


Figure 4.21: Acceleration plot for 100mm three-arc interconnect model drop test (averaged over three samples)

In this plot, the first peak was used to obtain both the magnitude of the impact peak acceleration and the experienced impact pulse for the given drop height. The impact pulses obtained from different drop heights are given in Table 4.2. Dominant frequencies and damping ratio were calculated using subsequent peaks of the acceleration plots. These values were used in subsequent finite-element simulations, and will be explained in the following chapter on numerical simulation.

Table 4.2: Impulse times recorded from experiment for three-arc interconnect drop test samples

Drop Height (mm)	100	200	300	400	500	600
Impulse Time (s)	0.01	0.008	0.005	0.003	0.002	0.0015

The second plot obtained from the experiments showed the magnitudes of strain recorded using the strain gauges mounted on both the board and the die-interconnect

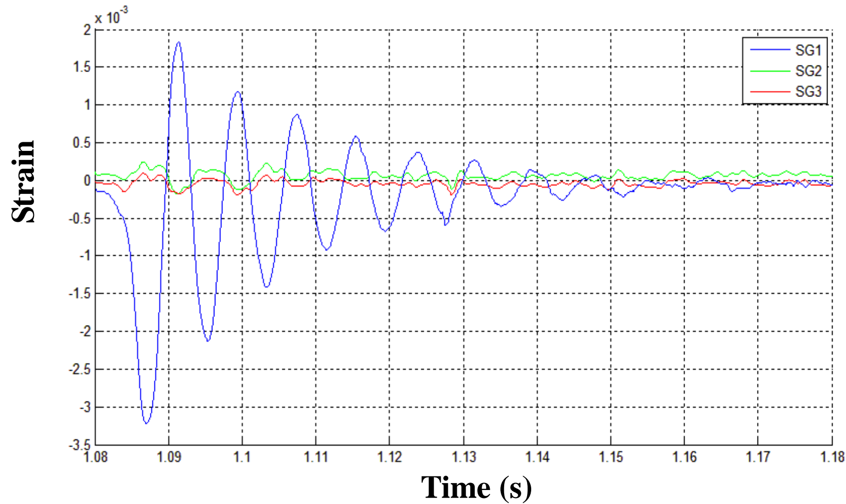


Figure 4.23: Strain data plot for 100mm three-arc interconnect model drop test (sample 1); SG1 refers to strain in the board while SG2 and SG3 refer to strain in the die

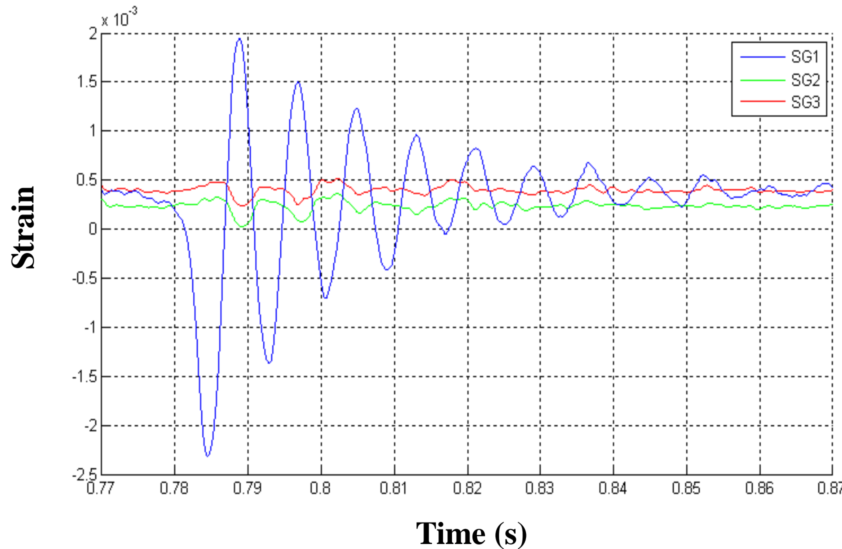


Figure 4.24: Strain data plot for 100mm three-arc interconnect model drop test (averaged over three samples); SG1 refers to strain in the board while SG2 and SG3 refer to strain in the die

assembly. Figure 4.23 shows the strain data plot for a 100mm height drop event for a particular trial while Figure 4.24 shows the averaged strain data plot.

The given strain data plot consists of three data sets, each data set corresponding to a given strain gauge output. The strain data denoted by SG1 (Strain Gauge 1) refers to the output of the single-axis strain gauge mounted on the board. At the same time, SG2 (Strain Gauge 2) refers to the output of the strain gauge mounted on the die, with its axis parallel to that of SG1 while SG3 refers to the strain gauge data from the strain gauge mounted on the die with its axis perpendicular to that of SG1. This system allowed studying the effect of the compliant interconnects on strain transfer from the board to the attached die possible as well as giving the transverse effect of the drop test event on the die-interconnect assembly. It should be noted that the strain gauge mounted on the die was a bi-axial 90°tee rosette strain gauge, with strain gauge SG3 perpendicular to strain gauge SG2. Therefore, there were three strain gauges mounted on each sample; a linear single axis strain gauge mounted on the board (SG1) with its axis parallel to the length of the board and a combined bi-axial tee rosette strain gauge mounted on the die, with one strain gauge (SG2) parallel to SG1 and another (SG3) at right angles to SG1. The peak strain from each strain gauge was obtained by studying the strain data plot for each sample.

The acceleration and strain data plots for all the samples are given in Appendix A with associated peak strain values given in Chapter 6.

4.3.3 Bump interconnect assembly drop testing

While the three-arc interconnect models gave experimental data on their behavior when subjected to drop testing, it was thought to be prudent to compare the response behavior of these three-arc compliant interconnect structures with other more conventional models. For this purpose, a bump interconnect was designed with the same

footprint as that of the three-arc interconnects. This bump interconnect model was assembled and fabricated in the same 3x3 area array pattern used for the three-arc interconnect design. The bump interconnect samples were prepared much the same way as the three-arc interconnect samples, with strain gauges and accelerometers mounted in the same locations as before.

Drop tests for these bump interconnect samples were conducted and associated acceleration and strain data were obtained using the same procedure enumerated in the previous sections. Again, as in the case of the three-arc models, multiple samples were tested and the three samples with the most consistent and repeatable results were used to obtain strain values for comparison.

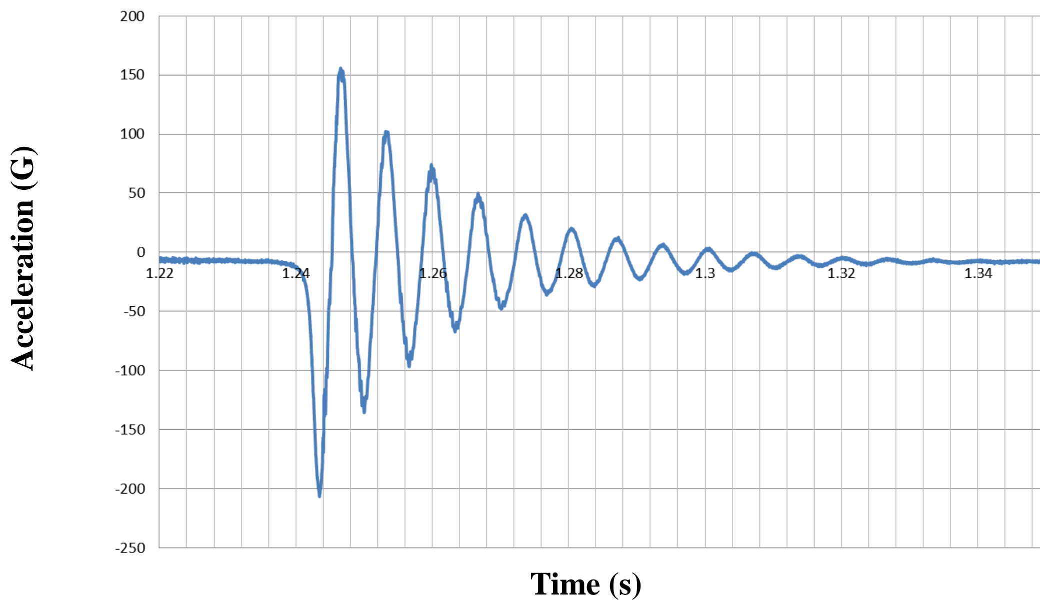


Figure 4.25: Acceleration plot for 200mm bump interconnect model drop test (sample 1)

As before, two plots were obtained from the bump-model interconnect drop test experiments. The first plot was the acceleration data obtained from the accelerometer mounted on the board of the sample. An example of this data plot is shown in Figure

4.25, which depicts the acceleration plot for a 200mm drop height for a particular trial. The first peak of this plot was used to obtain the peak acceleration value experienced by the sample, as well as the impact pulse time for the given drop height. The impact pulse times recorded for different drop heights are given in Table 4.3. Again, the damping ratio was calculated for each drop height using the acceleration plot and will be dealt with further in the next chapter.

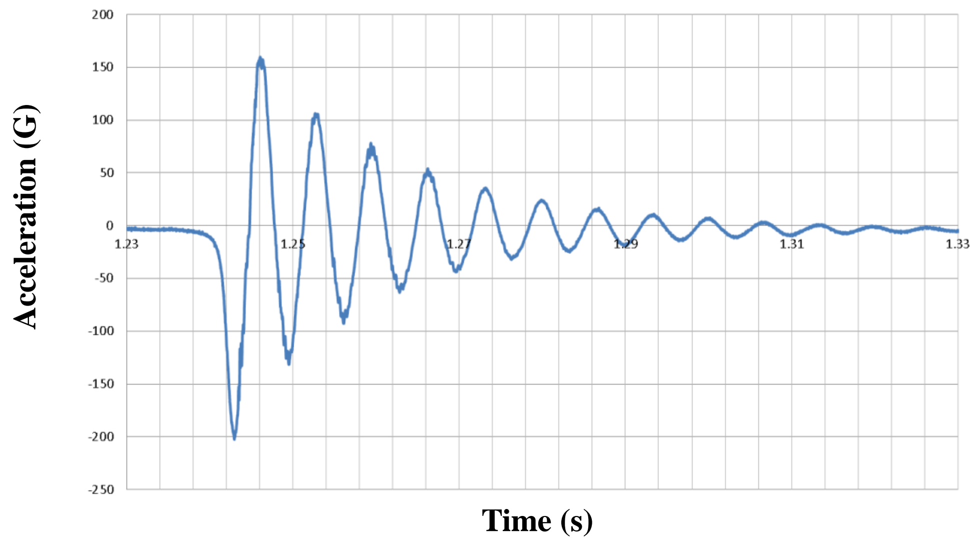


Fig 4.26: Acceleration plot for 200mm bump interconnect model drop test (averaged)

Table 4.3: Impulse times recorded from experiment for bump interconnect drop test samples

Drop Height (mm)	100	200	300	400	500	600
Impulse Time (s)	0.008	0.007	0.006	0.005	0.004	0.003

The second plot, as before, showed the strain data gathered from the different strain gauges mounted on the sample. The same naming convention (SG1, SG2 and SG3) which was used in the three-arc interconnect model was used here to obtain the strain

experienced at the location of the strain gauge mounts on the bump interconnect samples. Figure 4.27 shows a typical strain data plot for the bump interconnect, for a drop test height of 200mm.

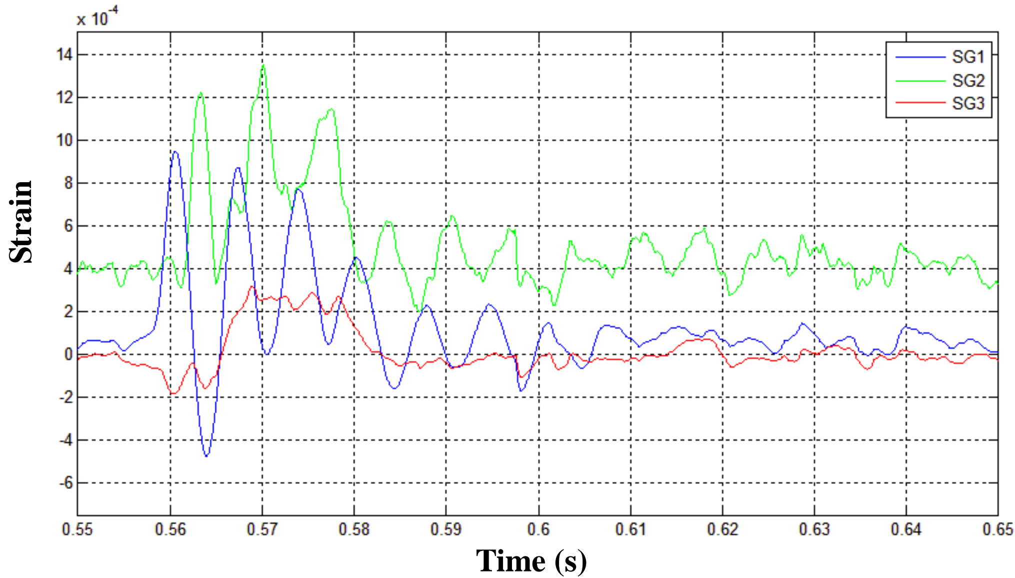


Figure 4.27: Strain data plot for 100mm bump interconnect model drop test (sample 1); SG1 refers to strain in the board while SG2 and SG3 refer to strain in the die

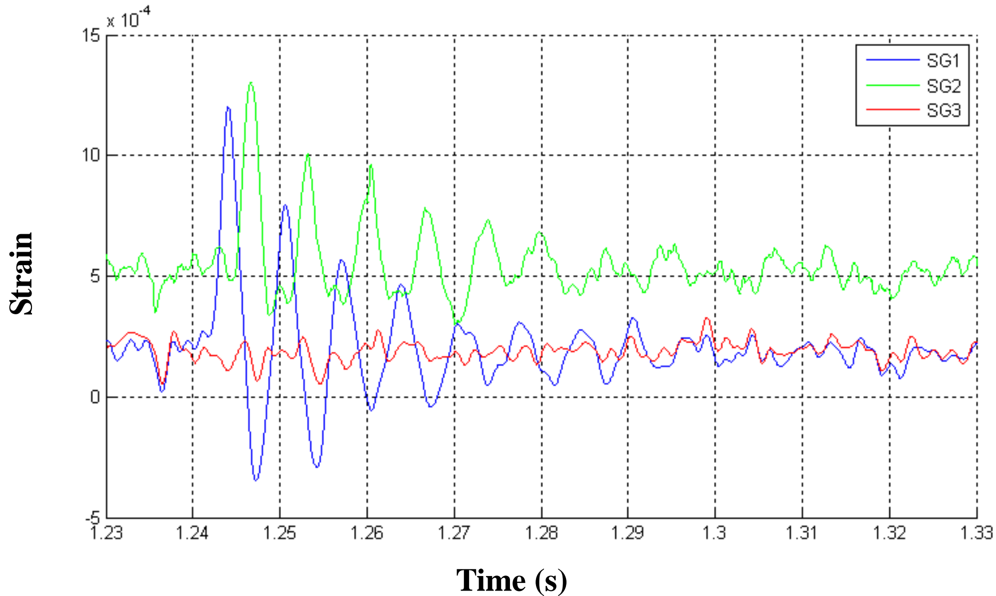


Figure 4.28: Strain data plot for 100mm bump interconnect model drop test (averaged over three samples); SG1 refers to strain in the board while SG2 and SG3 refer to strain in the die

The acceleration plots for different drop heights for the bump interconnect samples are given in Appendix A, while the averaged peak strain values are given in Chapter 6.

CHAPTER 5

FINITE-ELEMENT MODELING OF DROP TEST

While the experimental aspect of drop testing of the compliant interconnects provided physical behavioral evidence, it is still seen that the time it took to understand, set up and conduct these tests was very long. Industrial requirement of quick turnover necessitates the need for faster realization of drop testing results. Keeping this requirement in mind, numerical finite-element simulations of the three-arc compliant interconnect model were conducted using ANSYS®. This was done in order to obtain a quick yet physics-based assessment of the effects of drop testing on the compliant interconnects. At the same time, comparative simulations were run for the bump interconnect model. The following sections enumerate the finite-element modeling and simulation of the current drop testing process.

5.1 Traditional drop testing simulation

Drop testing simulation has been widely accepted as a quick means to understand the effect of shock and impact loads on microelectronic packages. Drop testing of microelectronic components generally involves large-scale deformation of entities within extremely short periods of time. Such type of large-scale deformations over short time durations necessitates the use of extremely small solution steps in the used finite-element model, known as time steps. Essentially, the time step size must be optimized for the given model and boundary conditions. Additionally, the smaller the time step size, the more accurate the result, although this will unfortunately also increase the total solution time. The traditional means of conducting drop testing simulations is by means of explicit

solvers, which are mathematical solvers used by finite-element simulation software to solve large-scale deformation problems. Explicit mathematical solvers are inherently more stable for large-scale deformation problems, such as in the case of drop testing. Researchers have, thus, usually turned towards numerical solvers which make use of explicit formulations. In comparison, basic finite-element simulation software come equipped with implicit solvers. Such implicit solvers typically see a large amount of divergence when used for large-scale deformation problems and are thus harder to use for solution of large strain rate problems such as drop testing simulation. While this may make a valid case for explicit solvers to be used, it stands to reason that the use of explicit solvers is restricted to those who have access to explicit solvers. This is because basic finite-element packages are not equipped with explicit solvers and are usually expensive add-ons. Implicit solvers are therefore a more economical option for finite-element simulation solution. With this in mind, an implicit approach to drop testing which would allow easy drop testing simulations was needed. A method which aimed to satisfy this requirement in implicit drop testing was the Input-G Method, proposed by Tee and Luan in 2004 [Tee et al, 2004].

5.2 Input-G Method

The Input-G Method is a drop testing simulation technique that was derived based on Joint Electron Device Engineering Council (JEDEC) standards for board level drop testing of microelectronic components [JESD22-B110a, JESD22-B111]. It is a technique which makes use of acceleration data or 'G value' gathered from a drop test experiment. The acceleration or 'G value' is the magnitude of acceleration experienced by a given object, in terms of multiples of acceleration due to gravity. In other words, a 150G value

represents an acceleration magnitude which is 150 times greater than the acceleration due to gravity. Thus, 150G is equal to 1471.5 m/s^2. The Input-G Method makes use of this acceleration value as input. Using basic mathematical equations, this acceleration value is converted into suitable displacement values. These displacement values can then be used as input boundary conditions to implicit simulations. The advantage of this Input-G Method lies in the conversion between acceleration and displacement. This is because an implicit solver can only take displacement values as input, and the Input-G Method caters to this need. Shown in Figure 5.1 are the locations for applying the displacement boundary conditions using the Input-G Method.

5.2.1 Impact pulse

The Input-G Method obtains the required acceleration data from the impact pulse

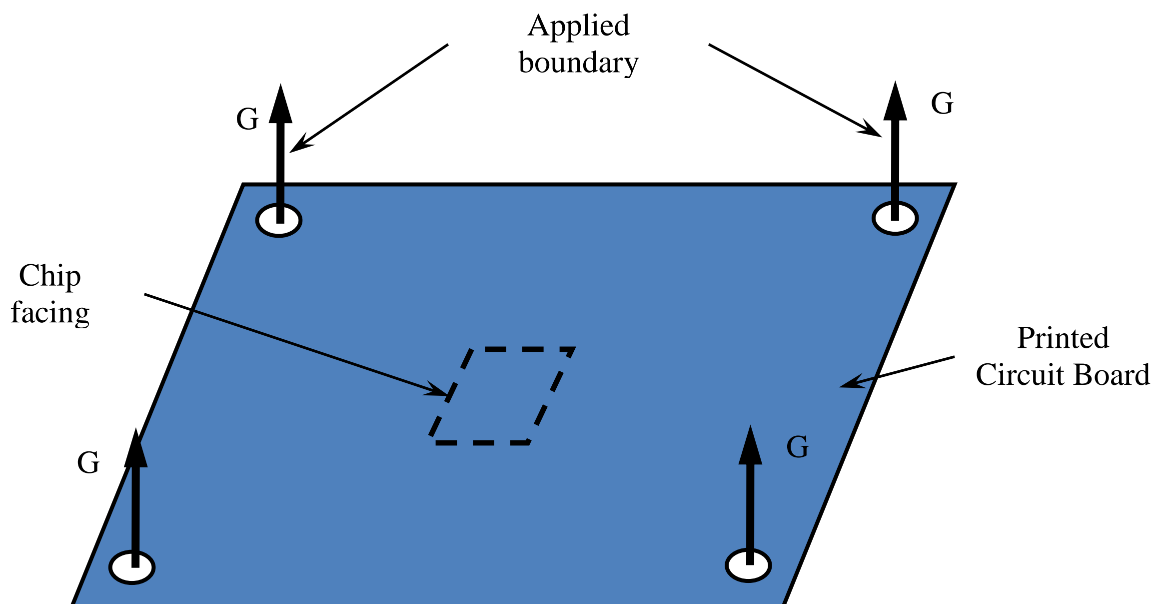


Figure 5.1: Schematic of Input-G Method showing applied boundary

generated during a drop event in a drop test experiment. The impact pulse is defined as

the first peak observed in the acceleration curve experienced by any component subjected to (in this case) drop testing. Typical acceleration impact pulses are given in Figure 5.2.

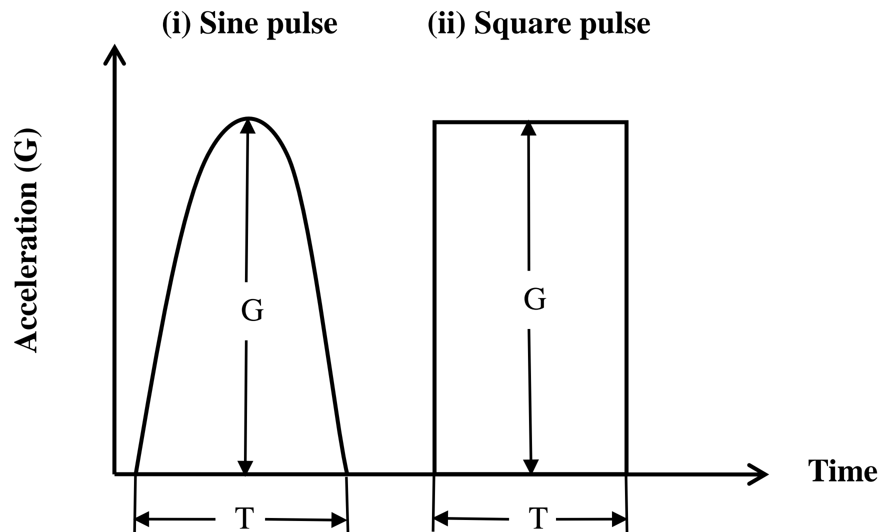


Figure 5.2: Sine and square impact pulses used to calculate input boundary conditions

The impact pulse observed from experiment is usually approximated as a sine curve. However, during simulation, the impact pulse can be suitably modified to obtain different types of loading conditions. Shown in Figure 5.2(ii) is a square impact pulse, wherein the impact pulse instantaneously jumps to a given value, then drop down after a given time. While this may be simple to model, it has been observed that the square pulse gives rise to unnecessary deformation during drop test simulation. For that purpose, an ideal sine curve is used to replace the simple-to-model square impact pulse. This is shown in Figure 5.2(i). The sine impact pulse requires multiple load steps to define in a simulation, but allows for better response of the model under study. Additionally, the sine impact pulse is the closest approximation to the acceleration impact pulse observed in experiment. The actual acceleration impact pulse is obtained by placing accelerometers at suitable locations on the sample to be drop tested. The location that was used in the

current research work to determine the impact pulse from experiment is shown in Figure 5.3. This location can be seen to be on the board, on the side opposite to the attached interconnects and die. The accelerometer location is given schematically in Figure 4.20.

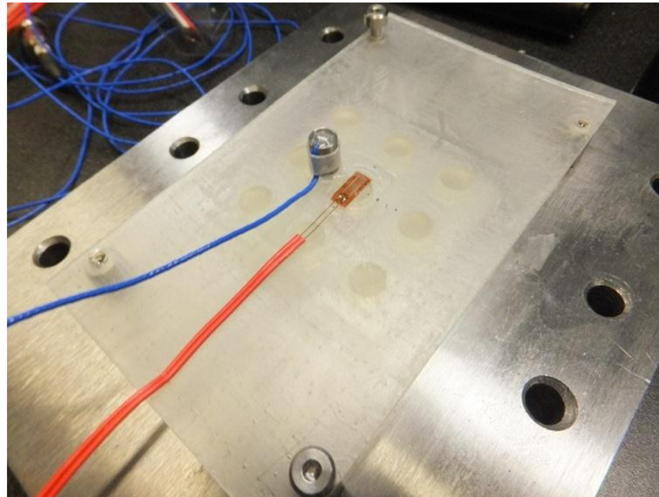


Figure 5.3: Accelerometer mount location to determine impact pulse during drop test

Once the impact pulse is clearly obtained, the peak acceleration (*G*) recorded during experiment can be obtained. At the same time, the overall duration for the impact pulse is also noted and is known as impulse time (*T*). Knowing these two quantities, it is easy to convert the acceleration conditions experienced by the test sample during drop testing into displacement boundary conditions needed as input for the implicit finite-element model based on the Input-G Method.

5.2.2 Displacement equation

The simplicity with which the Input-G Method converts the acceleration input boundary conditions obtained from experimental drop testing into usable displacement boundary conditions can be seen if one studies the mathematical equation used for his conversion. Given in Equation 5.1 is an example equation used for obtaining

displacement values from experimental acceleration data for a sine impact pulse [Tee et al, 2004].

$$d(t) = \int_0^t G_m \frac{T}{\pi}\left(1 - \cos\frac{\pi}{T}\tau\right) d\tau = G\frac{T}{\pi}\left(t - \frac{T}{\pi}\sin\frac{\pi}{T}t\right)$$ **- Equation 5.1**

In the above equation, *d(t)* is the displacement, G_m is the mean acceleration value, *G* is the peak acceleration value, *T* is the impulse time and *t* is time elapsed during the acceleration curve. The peak acceleration value *G,* as a function of time *t*, is given in terms of the mean acceleration value G_m by Equation 5.2 [Tee et al, 2004].

$$G(t) = G_m \sin\frac{\pi}{T}t$$ **- Equation 5.2**

From experiment, the value of peak acceleration value (*G*) and impulse time (*T*) are obtained. Then, using Equation 5.1, the required displacement boundary conditions are obtained from the acceleration input. Given in Figure 5.4 are the acceleration and displacement curves for a 500mm drop height test, with a peak acceleration of 536.1G and an impulse time of 2ms recorded from experiment.

It should be noted that taking the impact pulse from the experiment into consideration during the calculation of displacement boundary conditions invariably takes into account any extraneous effect from other components used during the drop test experiment [Tee et al, 2004]. This is because impact pulse is a function of every material and equipment used during the drop test experiment. Thus, using the impact pulse directly from experiment negates the need to model the impact surfaces during the finite-element model creation needed for the implicit Input-G Method. This is an advantage over explicit simulation, as explicit simulation requires the modeling of the surfaces undergoing impact during the drop event.

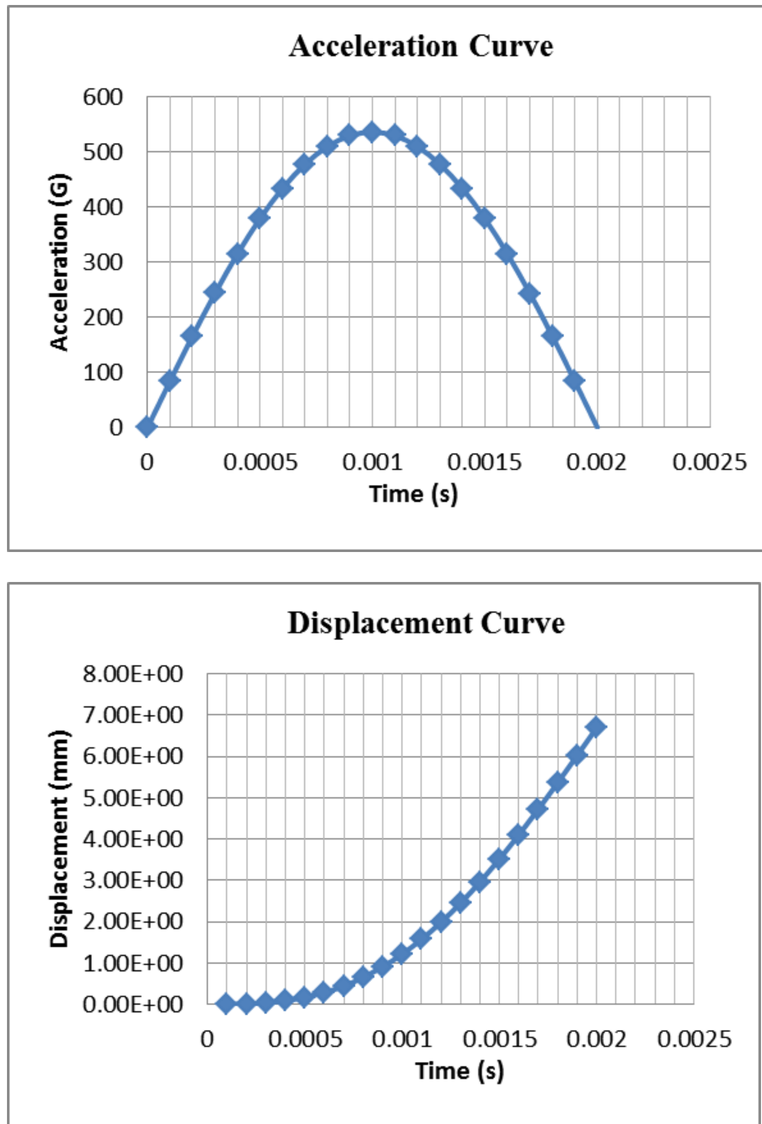


Figure 5.4: Acceleration and calculated displacement curves for 536.1G drop event from 500mm drop height

Keeping the above information in mind, it can be seen how the information presented in Chapter 4 on experimental drop testing could serve as input for the finite-element simulations conducted. In summary, the basic acceleration impact pulse experienced by the drop test samples in experiment is obtained for different drop heights by making use of an accelerometer mounted on the base plate of the drop test setup and

on the drop test sample itself. The first peak observed in each acceleration plot is used to obtain the peak acceleration value as well as the impact pulse experienced by the samples for the given drop height. This acceleration data (*G*) and impulse time (*T*) are then used in the acceleration-to-displacement conversion equation given by Equation 5.1 to obtain the displacement boundary conditions needed as input for the implicit finite-element simulation based on the Input-G Method.

5.3 Modeling geometry

As in the experiments, two different models were created. The first model was based on the multi-path three-arc compliant interconnect geometry while the second model was based on the bump interconnect geometry.

5.3.1 Basic dimensions

Since the experimental test samples were fabricated using geometries ported from the finite-element simulation models, the geometry used for simulation and the geometry of the experimental samples matched to a very close degree. Each model consisted of a board with dimensions 110mm by 64mm by 1mm. A die of dimensions 45mm by 45mm by 1mm was used in all the geometries. A 3 by 3 area array of scaled-up interconnects (three-arc compliant interconnect or bump interconnect, depending on the model being studied) were sandwiched between the die and the board. This geometry closely matched the experimental test samples.

5.3.2 Meshing

In implicit simulations, the fineness or coarseness of the mesh plays a very vital role in deciding whether the simulation successfully converges to an acceptable solution

or not. The mesh required for each model was varied depending on the areas of interest. The mesh was made fine near the interconnects and coarse away from the package itself, in order to reduce computation time and improve efficiency of the solution. 8-noded SOLID 185 elements were used to build both the three-arc interconnect and the bump interconnect models. At least three elements were used along the thickness of both the board and the die, to ensure the applied transverse boundary conditions could be properly transferred. Figure 5.5 shows the meshed finite-element model boundary conditions.

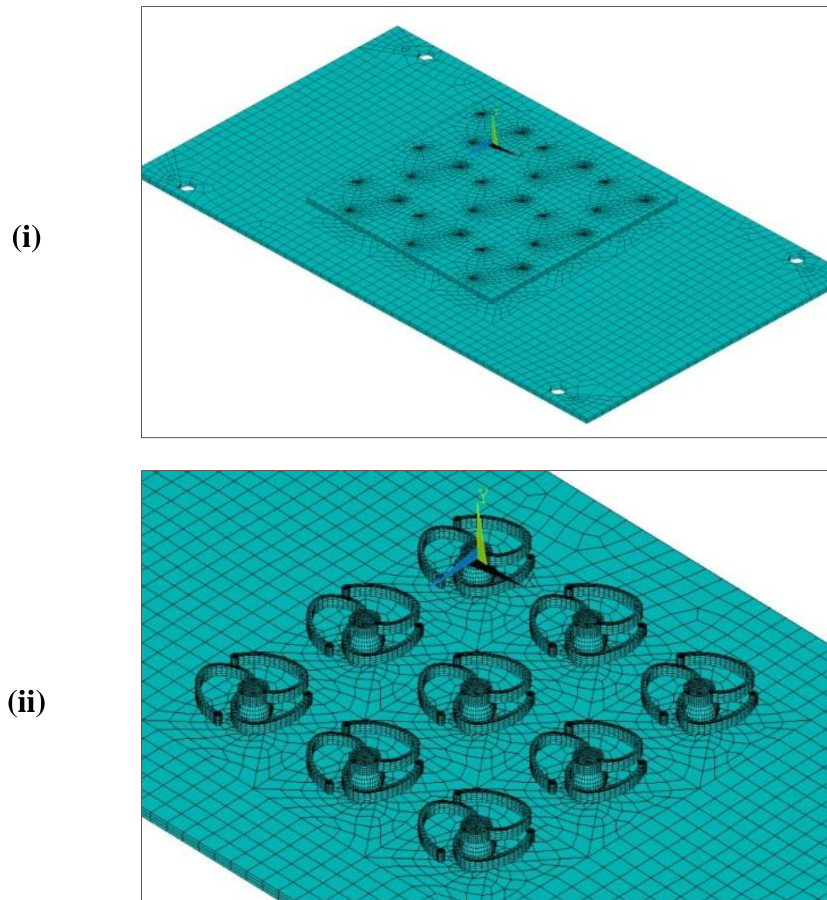


Figure 5.5: Simulation model for three-arc interconnects – (i) Full model with die and board (ii)Close-up of area-array of interconnects with die removed

5.3.3 Material properties

Both simulation models made use of a single homogenous polymer resin as in the actual experiments. The material properties for the given polymer resin used in experiment are given in Table 5.1.

Table 5.1: Polymer material properties

Material	Young's Modulus	Density	Poisson's Ratio
SL7510 polymer resin	**2282 MPa**	**1.18 g/cm^3**	**0.3**

The material properties used in the simulation were assumed to be linear elastic and isotropic in nature. This material model was deemed sufficient in order to understand the high strain rate response of the drop test sample, as well as to represent the polymer material properties of the drop test samples used in experiment. This material model was selected because the experiments were conducted at room temperature. Therefore, there was little or no creep or viscoelastic deformation. The simulations were also carried out at room temperature. Thus temperate effect on material properties could be ignored. Additionally, the experimental acceleration and strain data were obtained in less than 110ms, and thus, time-dependent creep effects could be ignored. It should be noted that at high strain rates, plastic effects are minimal and thus were not included in the simulations.

5.3.4 Boundary conditions

As seen in Figure 5.5, four screw holes are present in the both models used for simulation. These holes designate the locations were the test sample was screwed onto the base plate. Therefore, these are the locations were the boundary conditions must be applied in the simulations. Figure 5.6 shows the screw holes with applied displacement boundary conditions. These boundary conditions are applied in such a way as to mimic the inverted orientation of the drop test sample used in the experiment, as specified in the JEDEC standard [JESD22-B111].

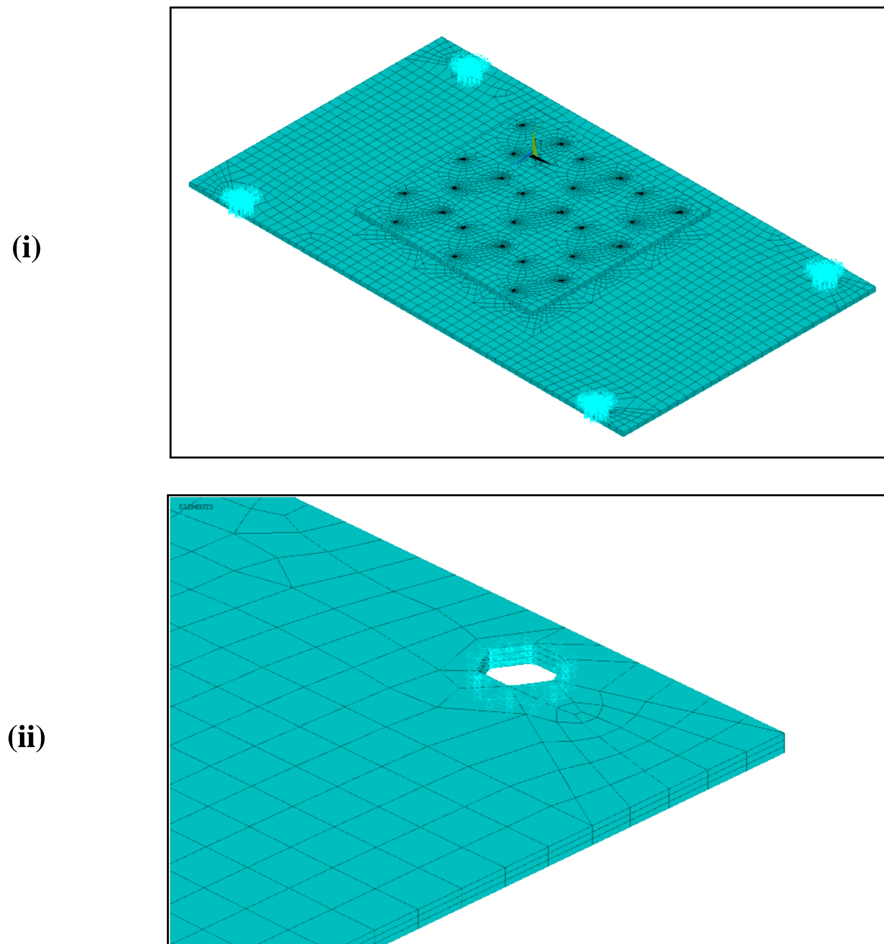


Figure 5.6: Applied boundary conditions– (i) Full model with displacement boundary conditions at four screw holes (ii)Close-up of applied boundary conditions at one loading screw hole

The boundary conditions needed for the simulations were taken based on the acceleration values taken directly from experiment, as explained in Section 5.2. After conversion to displacement, these boundary conditions were used as input to the finite-element model under study.

5.3.5 Damping and Damping ratio ξ

If allowed to solve without any additional input, a linear elastic model subject to a transient analysis, as was the case in the current research project, will keep on deforming indefinitely. The response of the system will either oscillate about the mean value indefinitely or will exponentially increase in magnitude until the model fails. The former type of response is seen only in ideal systems, while the latter is improbable and does not happen in nature.

In order to ensure the response of the finite-element model followed the same trend as the experimental results, the concept of damping was introduced into the model. Damping, when applied in any finite-element model, will periodically and rhythmically reduce or 'damp out' the response of the system, so that it comes to rest at a mean value. This type of response is seen in real world phenomena and is a necessary part of conducting dynamic finite-element analysis [Park et al, 2009].

In the currently presented research work, numerical damping was applied to the finite-element model using data gathered from the acceleration plot recorded during experiment for different drop heights. Shown in Figure 5.7 is the acceleration curve for a 100mm drop height test sample.

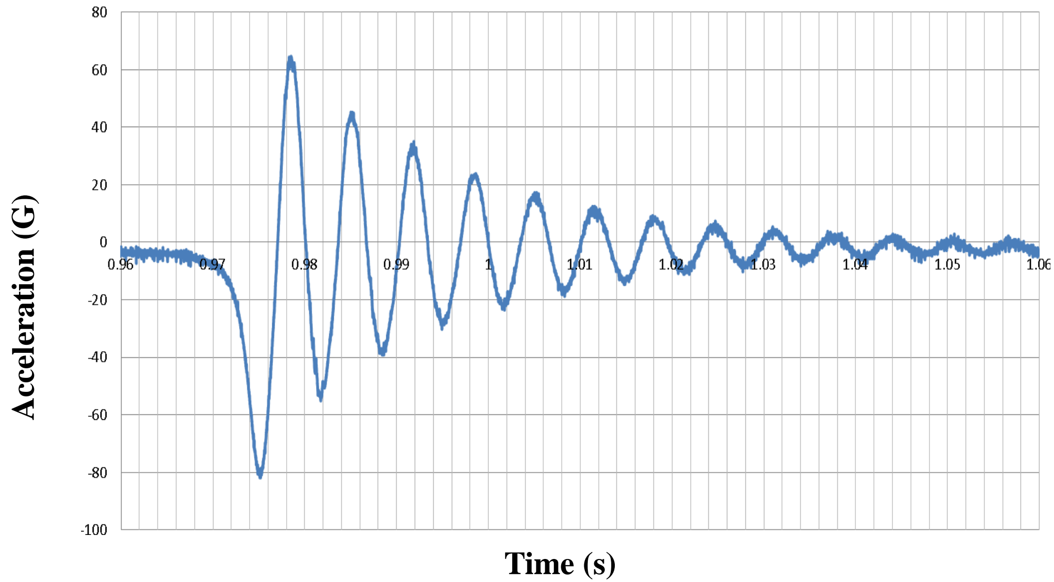


Figure 5.7: Acceleration curve for experimental 100mm drop test

Using the values obtained from consecutive peaks, the damping ratio of the system could be calculated using the following procedure [Ginsberg, 2001]-

1. Determine acceleration values at two consecutive peaks. Denote them as *x1* and *x2*.
2. Using Equation 5.3, the logarithmic decrement δ is calculated.

$$\delta = \ln\left(\frac{x1}{x2}\right)$$ **-Equation 5.3**

3. The logarithmic decrement δ is then used in Equation 5.4 to calculate the damping ratio ξ for the given acceleration curve.

$$\xi = \frac{1}{\sqrt{\left(1+\left(\frac{2\pi}{\delta}\right)^2\right)}}$$ **-Equation 5.4**

ANSYS® specifies damping in any implicit finite-element simulation by either making use of material damping parameters or numerical damping to damp out the

results. Equation 5.5 gives the relation for numerical damping which was used in the conducted finite-element simulations [ANSYS® reference manual, 2010].

$$\xi = \frac{\alpha}{2\omega_i} + \frac{\beta\omega_i}{2}$$ **-Equation 5.5**

In Equation 5.5, α and β are known as Raleigh's damping coefficients while ω_i stands for the circular natural frequency [ANSYS® reference manual, 2010]. Knowing any two dominant values for the natural frequency ω_i, and the value for damping ratio ξ, the values for damping coefficients α and β can be calculated. The value of damping ratio ξ was, thus, determined from experiment for different drop heights and samples. The dominant natural frequencies were determined by running a modal analysis on the finished finite-element model. Once ω_1 and ω_2 were known, two simultaneous equations were solved as given below.

$$\xi = \frac{\alpha}{2\omega_1} + \frac{\beta\omega_1}{2}$$ **-Equation 5.7**

$$\xi = \frac{\alpha}{2\omega_2} + \frac{\beta\omega_2}{2}$$ **-Equation 5.8**

Therefore, using Equations 5.7 and 5.8, the values for damping coefficients α and β were determined and used as input into the implicit finite-element model to damp out the response of the system in a fashion similar to that observed in experiment.

5.4 Three- arc interconnect drop test simulations

The first geometry studied in the current research work was the multi-path three-arc interconnect model. Shown in Figure 5.8, the three-arc interconnect geometry consists of a 3 by 3 area-array of multi-path compliant interconnects sandwiched between a board and a die. The three-arc interconnects were scaled up 75 times from their original dimensions, with the final dimensions meant for a pitch of 15mm.

(i)

(ii)

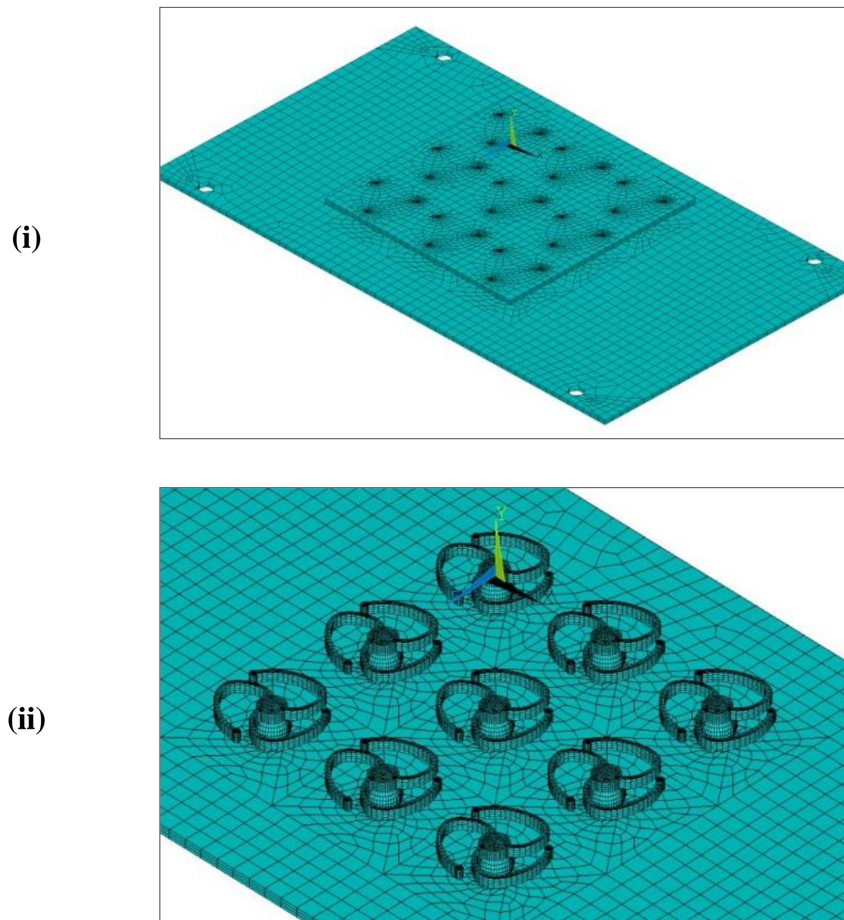
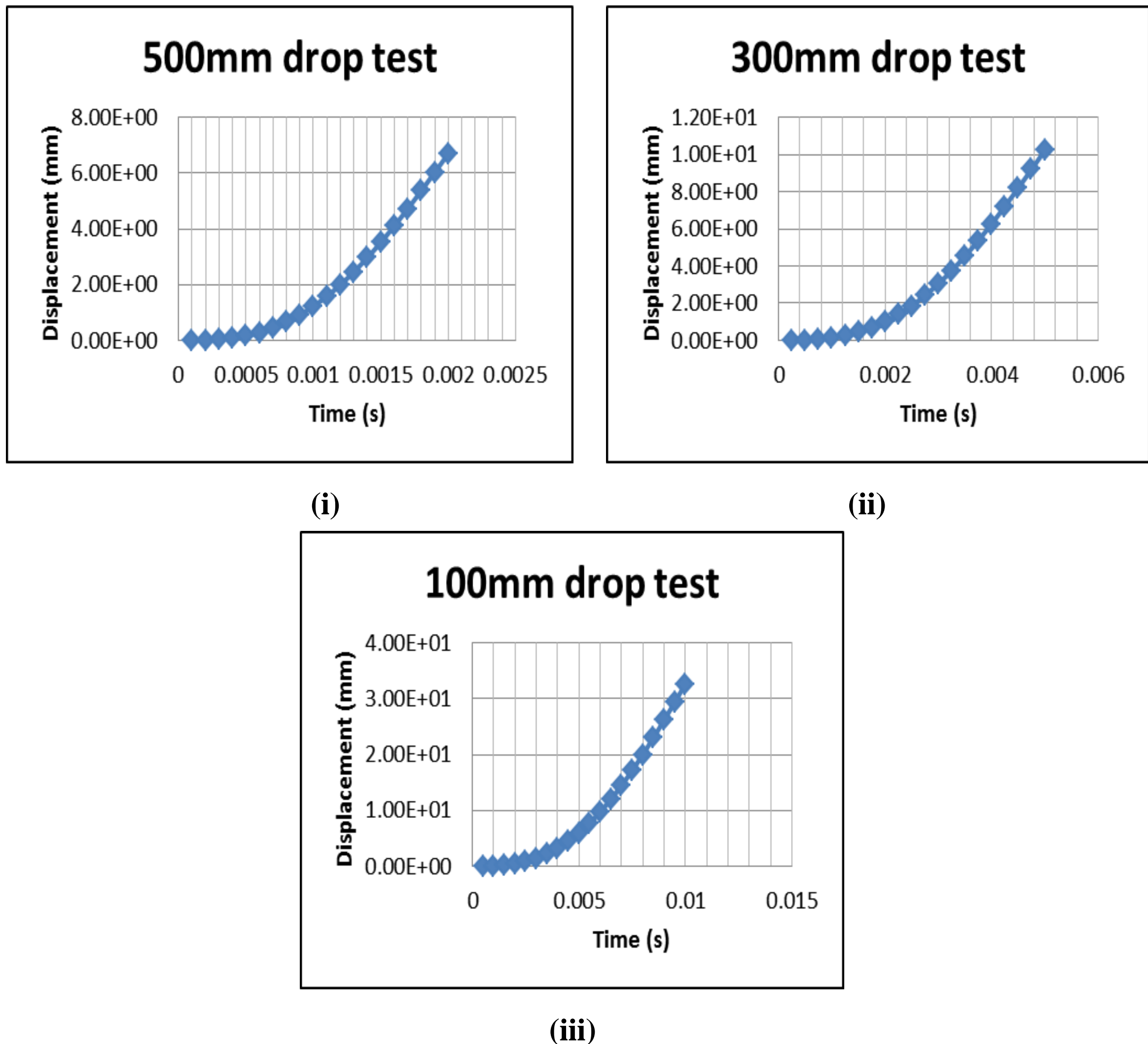


Figure 5.8: Simulation model for three-arc interconnects – (i) Full model with die and board (ii)Close-up of area-array of interconnects with die removed

5.4.1 Boundary condition input

As explained in Section 5.3, the input displacement boundary conditions were obtained by converting the acceleration curve values recorded in experiment. Figure 5.9 shows a typical displacement curves for 100mm, 300mm and 500mm drop test events used as input boundary conditions, and were calculated from acceleration values obtained in experiment.



(iii)

Fig 5.9: Calculated three-arc interconnect model displacement curves – (i) 500mm drop height displacement curve with 2ms impulse time (ii) 300mm drop height displacement curve with 5ms impulse time (iii) 100mm drop height

At the same time, damping was applied numerically using the procedure enumerated in Section 5.3.5. Modal analysis was carried out to determine the natural frequencies of the three-arc interconnect model. The two dominant natural frequencies selected were 109.89Hz and 215.98Hz. Damping ratios were then calculated from acceleration curves recorded in experiment. Table 5.2 gives the damping ratios observed for various drop test heights.

Table 5.2: Damping ratios for three-arc interconnect model for different drop heights

Drop height	100mm	200mm	300mm	400mm	500mm	600mm
Damping Ratio ξ	0.0887	0.09238	0.09735	0.09248	0.09487	0.11418

The damping ratios given in Table 5.2 were used to calculate the Rayleigh damping coefficients α and β for different drop heights. These values were applied to the finite-element simulations.

5.4.2 Basic results

Given in Figure 5.10 is a typical response curve for a drop test simulation. Three curves were obtained from the finite-element model. Each curve represented an averaged strain value, and corresponded to the strains measured during experiment and explained in Section 4.3.2. The notations used in experiment for different strain values (SG1, SG2 and SG3) were the same notations used in the presented simulation data. Therefore, SG1 represents strain recorded on the board surface, along the length of the board. SG2 and SG3 refer to strains recorded on the die, one along the length of the board and the other along the width of the die respectively. The detailed results for the three-arc interconnect drop test simulations are given in the Chapter 6.

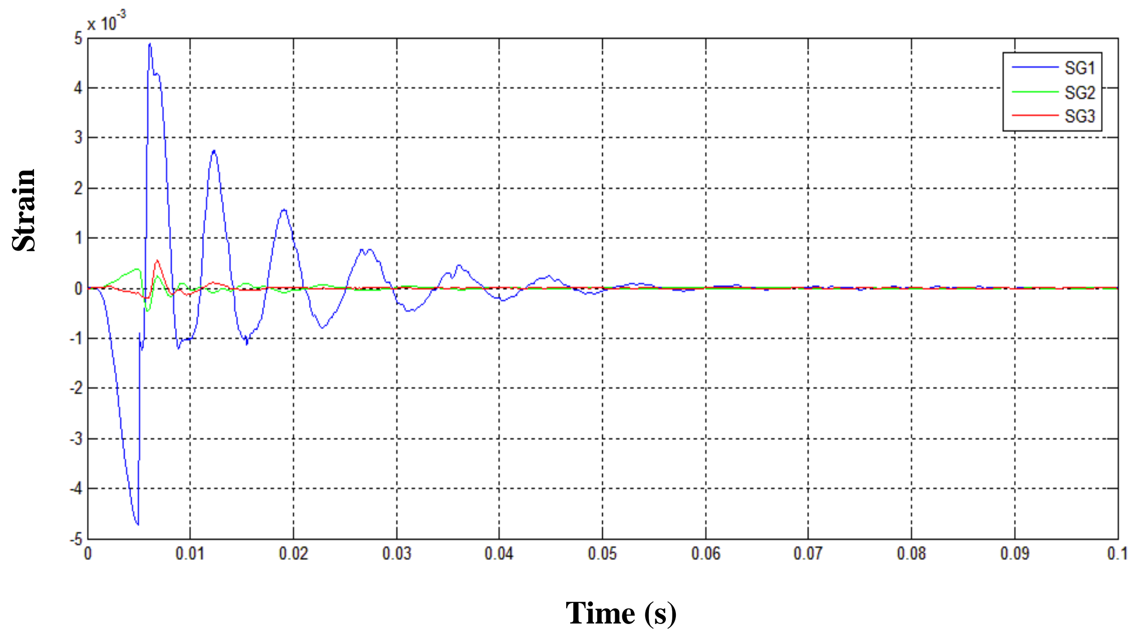


Figure 5.10: Strain response curve for 500mm drop height three-arc interconnect model simulation

5.5 Bump interconnect drop test simulations

The second geometry studied in the current research work was the bump interconnect model. Shown in Figure 5.11, the bump interconnect geometry consists of a

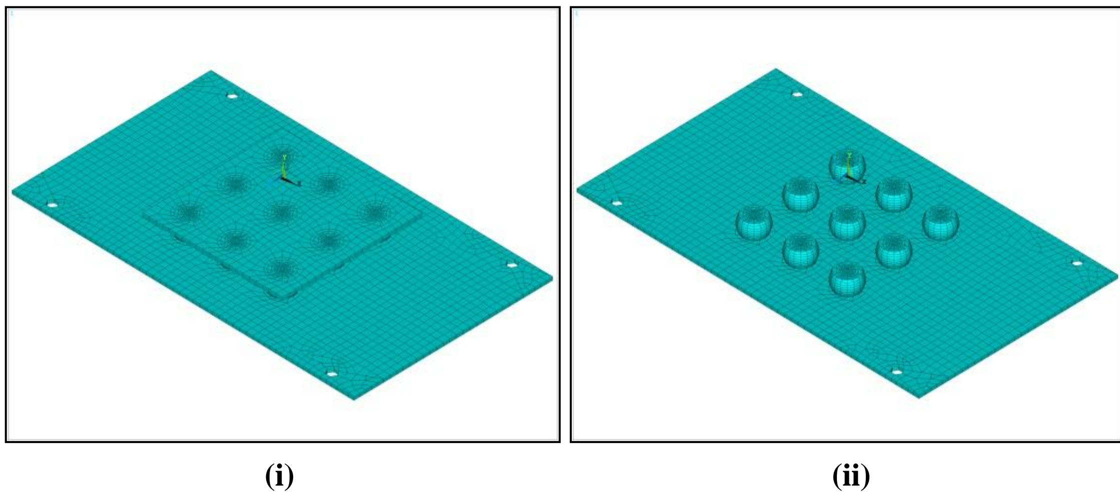


Figure 5.11: Bump interconnect simulation model – (i) Full model showing die and board (ii) Bump interconnect exposed by removing the die

3 by 3 area-array of multi-path compliant interconnects sandwiched between a board and a die, similar to the geometry arrangement in the three-arc interconnect model.

A pitch of 15mm was utilized with a footprint size of each bump interconnect equal to that of the corresponding three-arc interconnect. The main purpose of the bump interconnect model was to provide comparative results for the strain response of the three-arc interconnect model.

5.4.1 Boundary condition input

Figure 5.12 shows the typical displacement curves for 200mm, 300mm and 500mm drop test events used as input boundary conditions in the bump interconnect model, and were calculated from acceleration values obtained in experiment.

It can be seen that the final applied values seemed to greatly increase in comparison to the three-arc interconnect displacement curves. This was attributed to the larger impulse times and the lower peak acceleration values recorded for the bump interconnect model. The strain response of the samples was the focus of these finite-element simulations.

Damping was applied numerically using the procedure enumerated in Section 5.3.5, similar to what was done for the three-arc interconnect model. Modal analysis was carried out to determine the natural frequencies of the bump interconnect model. The natural frequencies found to be dominant for this model were 413.56Hz and 937.8Hz. Next, damping ratios were calculated from acceleration curves recorded in experiment. Table 5.3 gives the damping ratios observed for various drop test heights for the bump interconnect model.

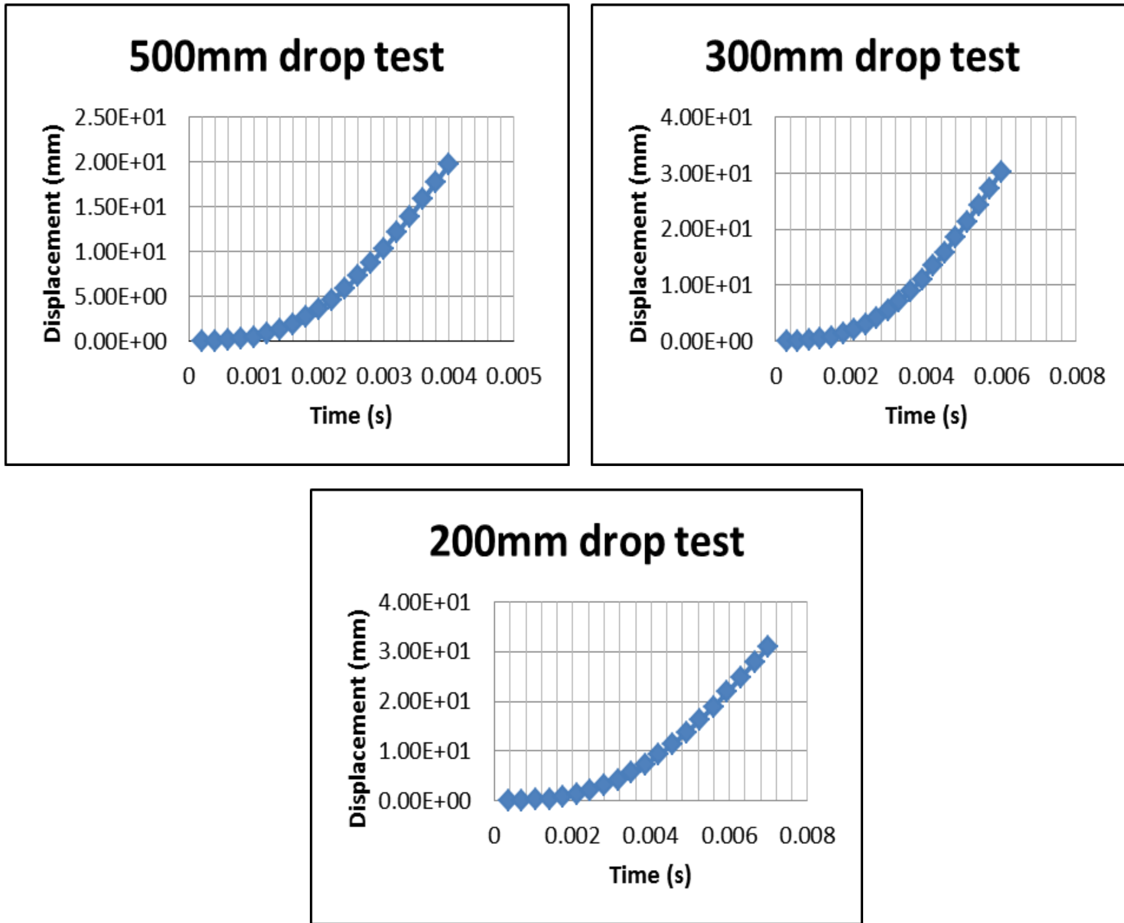


Figure 5.12: Calculated bump interconnect model displacement curves – (i) 500mm drop height displacement curve with 4ms impulse time (ii) 300mm drop height displacement curve with 6ms impulse time (iii) 200mm drop height displacement curve for 7ms impulse time

Table 5.3: Damping ratios for bump interconnect model for different drop heights

Drop height	100mm	200mm	300mm	400mm	500mm	600mm
Damping Ratio ξ	0.05249	0.06694	0.07127	0.08657	0.09359	0.09861

Finally, using the natural frequencies and the damping ratios given in Table 5.2, the Rayleigh damping coefficients α and β were determined for different drop heights and were used as input damping parameters for the finite-element simulations.

5.4.2 Basic results

Given in Figure 5.13 is typical response curve for a bump interconnect model drop test simulation. Three curves were obtained from the finite-element model. Each curve represented an averaged strain value, and corresponded to the strains measured during experiment and explained in Section 4.3.3. The notations used in experiment for

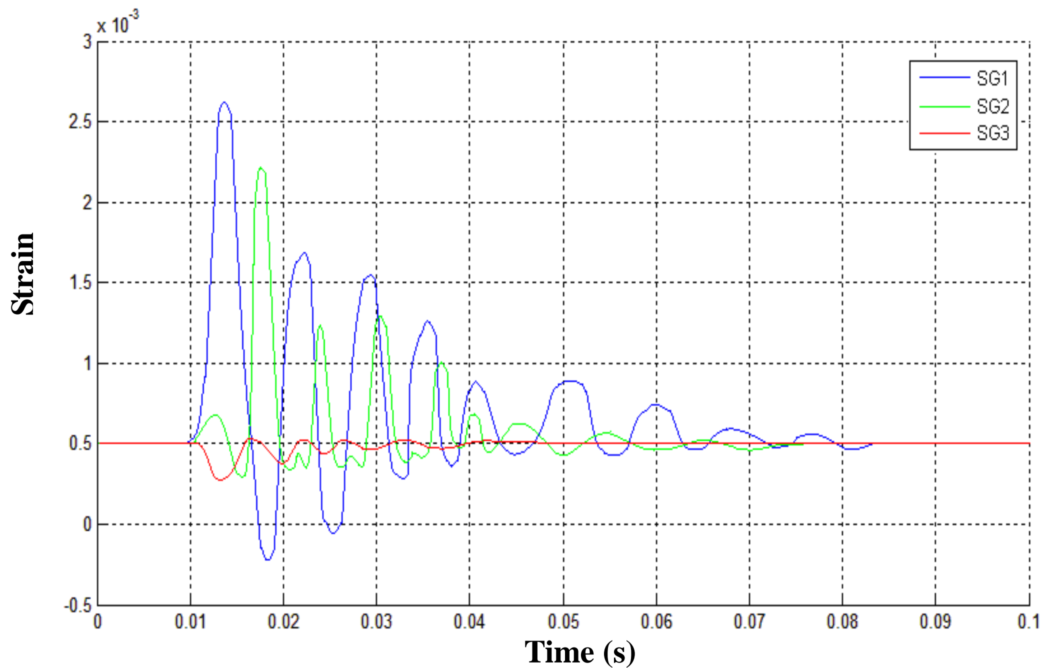


Figure 5.13: Strain response curve for 500mm drop height bump interconnect model simulation

different strain values (SG1, SG2 and SG3) were the same notations used in the presented simulation data.

Here, SG1 represents strain recorded on the board surface, along the length of the board. SG2 and SG3 refer to strains recorded on the die, one along the length of the board and the other along the width of the die respectively. The detailed results for the bump interconnect drop test simulations are given in the Chapter 6. In addition, it should be noted that the bump interconnect geometry finite-element simulations used slightly reduced material properties for the polymer resin. A Young's Modulus of 1882MPa was

used to conduct the bump interconnect simulations, as compared to the 2282MPa, which was the original material property value.

CHAPTER 6

RESULTS AND COMPARISON

In the Chapter 4, we have seen the various methods and processes used to conduct drop test experiments on two different interconnect designs, the multi-path three-arc compliant interconnect and the bump interconnect for comparison. In Chapter 5, the methodology behind conducting implicit finite-element simulations for the purpose of quick estimation of drop test response behavior of the interconnects was given. The current chapter will present the results obtained from the various drop test experiments conducted on the stereolithography-based drop test samples for both interconnect designs studied. The first section will present experimental results obtained from drop testing of the multi-path three-arc compliant interconnect. This will be followed by a section on experimental drop test results obtained from drop testing of the bump interconnect geometry. The purpose of this model will be to provide a comparative estimate of the response behavior of the three-arc compliant interconnects. Comparisons between the two interconnect designs will be given in subsequent sections. Finally, the experimental results will be used to validate the finite-element simulations conducted.

6.1 Multi-path three-arc compliant interconnect experimental results

One of the main objectives of this presented research work was to understand the drop test response and reliability of the proposed multi-path compliant interconnect design. Since the fabrication of the actual copper-silicon interconnect-die assembly was still under way, an alternative fabrication technique was used to fabricate the required three-arc interconnect geometry. Stereolithography was used to generate scaled up

versions of the complaint interconnects. These samples were used to obtain information on the response behavior of the three-arc compliant interconnects.

A number of samples were fabricated and tested using the methods explained in Chapter 4 on experimental drop testing procedures. The samples were mounted in a custom drop test fixture as shown in Figure 6.1.

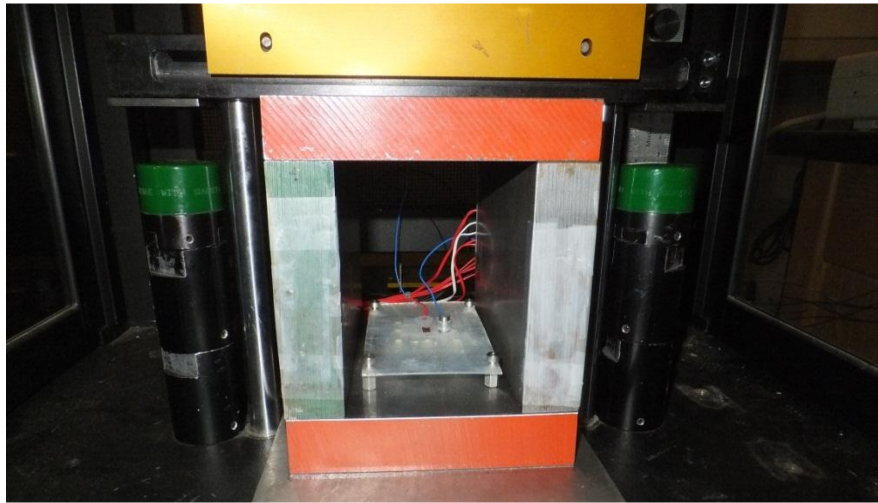


Figure 6.1: Drop test sample mounted inside fixture

The samples were then raised to dropped from different heights (100mm, 200mm, 300mm, 400mm, 500mm and 600mm), with the maximum drop height restricted by the height of the Instron® drop weight impact testing machine used to conduct the drop tests. The strain and acceleration experienced by the samples for different drop heights were measured by means of mounted strain gauges and accelerometers as shown in Figure 6.2 and Figure 6.3.

Output from the strain gauges, accelerometer and power supply were recorded using a Data Acquisition System. The data was ported to LabView®, where preliminary observations of the recorded strain and acceleration values were done. Finally, the data was filtered using a 1000Hz low pass Butterworth filter using Matlab®. Given in the

following sections are the results from the drop testing of the three-arc compliant interconnect geometry.

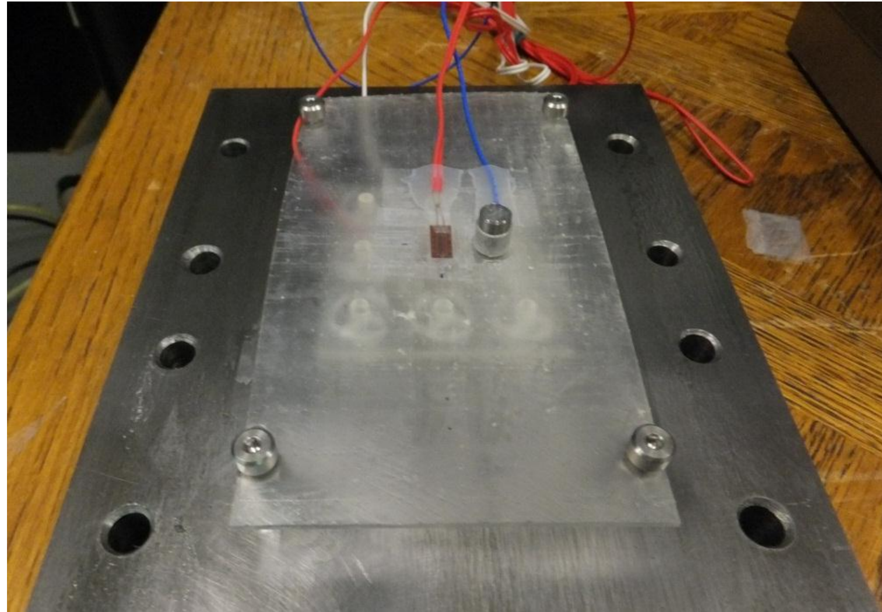


Figure 6.2: Strain gauge and accelerometer mounted on three-arc interconnect drop test sample

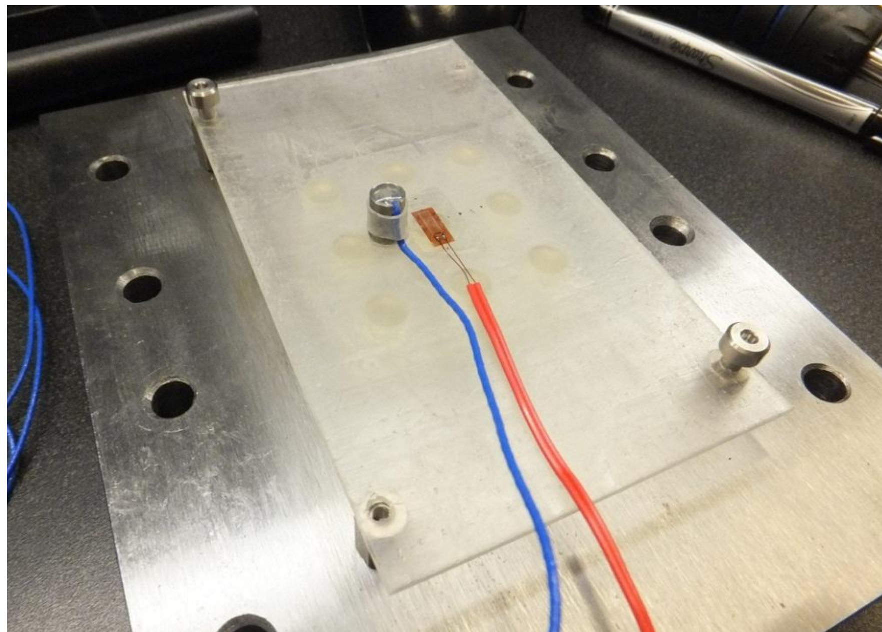


Figure 6.3: Strain gauge and accelerometer mounted on bump interconnect drop test sample

6.1.1 Acceleration data

After the three-arc compliant interconnect drop test samples were prepared and mounted for drop testing, initial observations were made on the acceleration imparted to the samples by the drop event, as well as the acceleration experienced by the sample itself. Shown in Figure 6.4 is the acceleration data obtained from a 100mm height drop test of the three-arc interconnect sample.

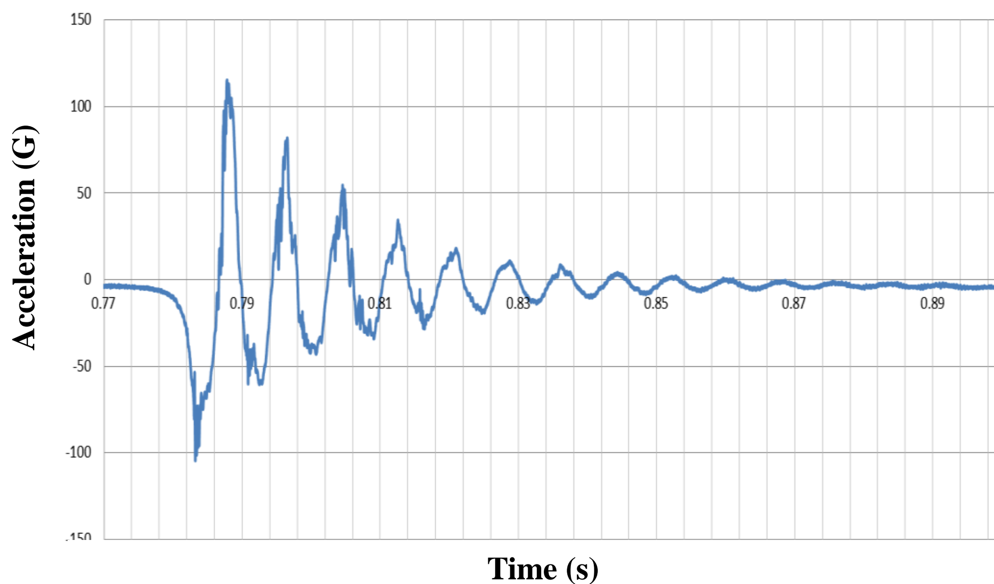


Fig 6.4: 100mm height drop test acceleration response for three-arc interconnect sample

The above acceleration versus time plot was obtained from the accelerometer mounted on the sample, as shown in Figure 6.5.

The acceleration response of the sample could be seen to clearly damp out from a first peak maximum value of 105G to 0G over a duration of 100ms for a 100mm height drop test. The first peak was also used to determine the required impact pulse duration, necessary for conducting finite-element drop test simulations. Subsequent peaks were used to determine the damping ratio using Equation 5.3 and Equation 5.4, as mentioned

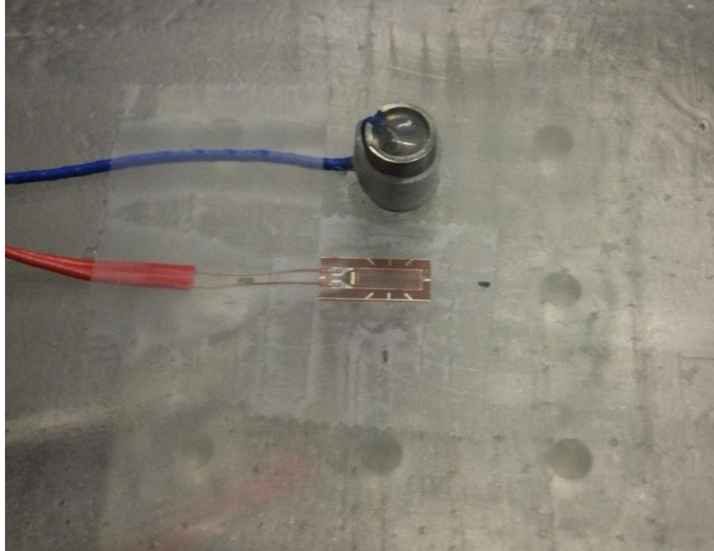


Figure 6.5: Accelerometer mounted on three-arc interconnect sample

in Chapter 5 on finite-element simulation. Given in Table 6.1 are the first measured peak acceleration values and the impact times for the multi-path three-arc interconnect geometry, over drop heights ranging from 100mm to 600mm.

Table 6.1: Peak acceleration and impact times for three-arc interconnect assembly under drop testing

Drop Height (mm)	100	200	300	400	500	600
Measured Peak Acceleration (G)	104.5	182.41	130.9	391.8	536.1	1056.8
Impact Time (s)	0.01	0.008	0.005	0.003	0.002	0.0015

The 200mm drop height tests seem to not follow the trend. This was attributed to faulty damping material used for all the 200mm drop height tests of the three-arc interconnect. The acceleration plots obtained from drop testing of the three-arc geometry for different drop heights are given in Appendix A. The scatter shown in the acceleration plots is due to the use of raw data directly, without any filtering. It was decided that filtering the acceleration plot data at this stage would lead to compromised results, with

the maximum acceleration value getting reduced. By not filtering, the acceleration plots could be used effectively to obtain proper input boundary conditions for the simultaneously conducted finite-element simulations.

Based on the acceleration plots, it could be seen that the peak acceleration value or the maximum ‘G value’ tended to increase exponentially from 104.5G at a drop height of 100mm to 1056.8G at a drop height of 600mm. The exponential behavior of the acceleration recorded can be attributed to the fact that the acceleration experienced is a function of the drop height (h), the velocity before impact (v) as well as the material used to obtain the required damping and output pulse shaping. These variables when put together give rise to decreasing impact times with increasing height. The higher drop test height impact time values for the conducted drop test experiments also seemed to converge towards the drop test height specifications given in the JEDEC standard on board level drop testing.

6.1.2 Strain data

The strain gauges mounted on the three-arc interconnect drop test samples were used to measure the amount of strain experienced in the board and the mounted interconnect-die assembly. As has been mentioned before, the strains shown in the following plots are based on three values recorded per sample. The first strain value, SG1, refers to the longitudinal strain recorded from the board, at the center and along its length. Value SG2 refers to the strain at the die center, again along the length of the board. SG2 values were recorded parallel to SG1. SG3 refers to the strain values again recorded on the die, but in a direction transverse to both SG1 and SG2. The data shown

was normalized and filtered using a 1000Hz low-pass Butterworth filter which was deemed sufficient to filter most of the high frequency scatter and noise.

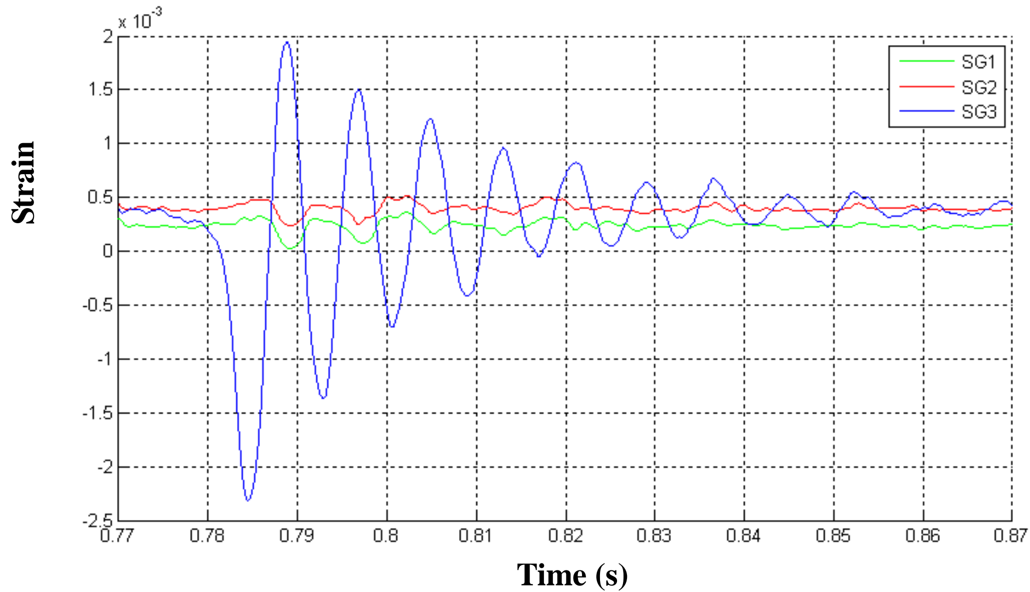


Figure 6.6: Strain data from 100mm drop test for three-arc interconnect sample

Figure 6.6 shows the strain data obtained from a 100mm height drop test of the three-arc compliant interconnect geometry. The strain data plots for the remaining drop heights can be found in Appendix B. The peak strain values for different drop heights are given in Table 6.2 and were calculated by taking the maximum difference from the mean of each strain plot.

Table 6.2: Experimental microstrain data for three-arc interconnect drop test

Drop Height (mm)	100	200	300	400	500	600
SG1	2256	3964	4291	5673	5774	6258
SG2	312	495	879	1006	1008	1069
SG3	250	305	692	646	562	441

The strain in the board, SG1, can be seen to monotonically increase as the drop height increases from 100mm to 600mm. At the same time, it can be observed that the strain in the die recorded by SG2, remains fairly constant around 1000 after a drop height of 400mm. The strain in the die along the transverse direction, recorded by SG3 is reported as nearly half that of SG2. From these, we can gather that the board strains are heavily dependent on the drop height, which linearly increases. At the same time, the die strains (SG2 and SG3) seem to be much smaller in magnitude than the board strains (SG1). This can be attributed to the presence of the three-arc compliant interconnects, which are able to absorb and damp out most of the strain being transferred from the board to the die. The ratio of board strain to die strain is averaged to 5.85:1, displaying the impact-isolating nature of the flexible arms of the three-arc compliant interconnects.

6.2 Bump interconnect experimental results

While the three-arc compliant interconnect geometry experimental results gave good insight into the behavior of these structures when subjected to drop testing, it was thought that a comparative estimate of the response behavior of these compliant interconnects would be useful. For this reason, an interconnect design based on the conventional solder bump was designed. The bump interconnect was designed to have the same footprint as the scaled-up three-arc compliant interconnect. The drop test samples for this particular interconnect design were also fabricated using the stereolithography process, as the three-arc compliant interconnect. The sample preparation, testing procedure, acceleration and strain measurement, collection and post-processing of data for the bump interconnect were all done in the same fashion as that for the three-arc interconnect.

The bump interconnect drop test samples were also dropped from various heights ranging from 100mm, 200mm, 300mm, 400mm, 500mm to 600mm. The drop test strain data collected from the various drop tests was filtered using a 1000Hz low-pass Butterworth filter to remove any extra noise and filter the data.

6.2.1 Acceleration data

Initial understanding of the response of the bump interconnect models to drops from various heights was done by obtaining acceleration data from accelerometers mounted on the sample. Given in Figure 6.7 is the acceleration response recorded from a 200mm height drop test of a bump interconnect test sample. The various acceleration plots for different drop heights are given in Appendix A.

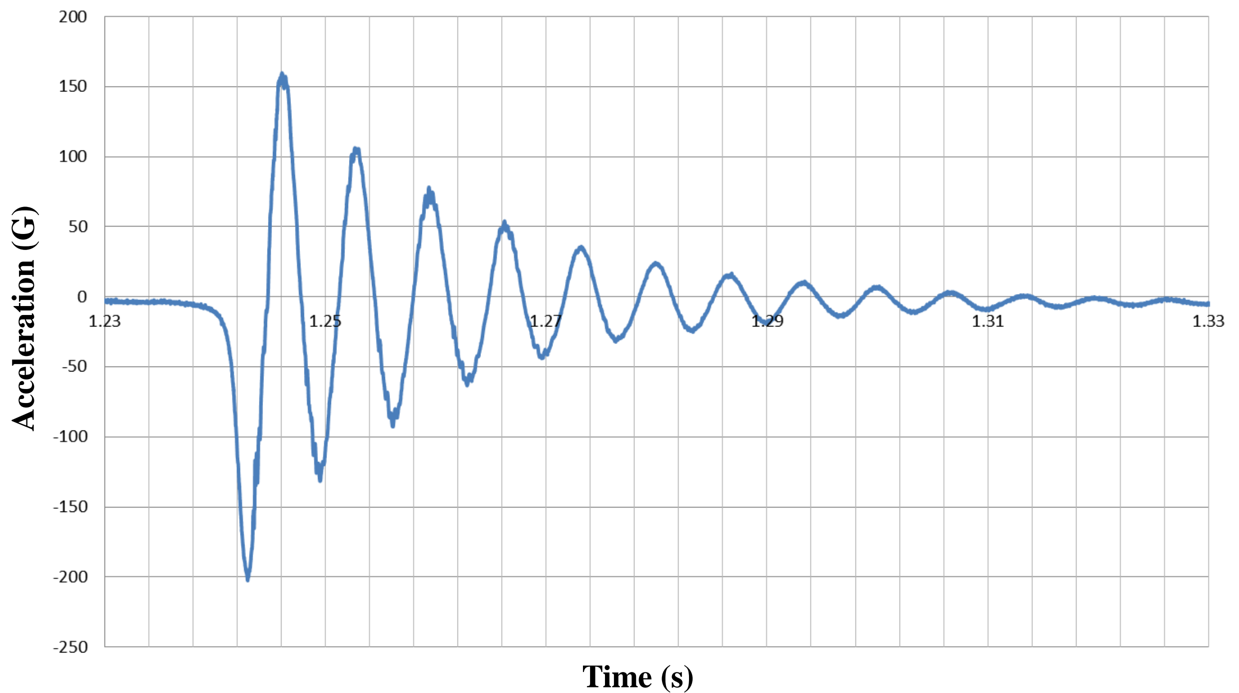


Figure 6.7: Acceleration response for 200mm height drop test for bump interconnect sample

The maximum acceleration value according to the Figure 6.7 is 202.6G for a drop height of 200mm. This value increases to a magnitude of 766.7G for a 600mm height drop test. Using the acceleration versus time plots, the impact times for the bump interconnect sample for various drop heights was determined. The acceleration values were observed to increase with drop height, as was expected. The different peak acceleration values and associated impact times recorded for the bump interconnect drop tests are given in Table 6.3.

Table 6.3: Peak acceleration and impact times for bump interconnect drop test

Drop Height (mm)	**100**	**200**	**300**	**400**	**500**	**600**
Measured Peak Acceleration (G)	**81.87**	**202.6**	**269.49**	**352.9**	**394.9**	**766.7**
Impact Time (s)	**0.008**	**0.007**	**0.006**	**0.005**	**0.004**	**0.003**

Appropriate finite-element simulations were carried out, using the acceleration peak values and impact times shown in Table 6.3 as input boundary conditions.

6.2.2 Strain data

Alongside the acceleration response collected and shown in Section 6.2.1, strain data was obtained for the various bump interconnect geometry drop tests. The location and arrangement of strain gauges used was the same as for the three-arc samples. SG1 refers to the longitudinal strain in the board, SG2 refers to the strain in the die parallel to SG1 and SG3 refers to strain in the die transverse to SG1 and SG2. Figure 6.8 shows the strain data plot for a 200mm height drop test for the bump interconnect sample geometry.

The various maximum strains for different drop heights recorded from experiment are given in Table 6.4.

Table 6.4: Experimental strain data for bump interconnect drop test sample

Drop Height (mm)	100	200	300	400	500	600
SG1	-	1094	1334	1624	1853	1765
SG2	-	748	1109	1408	1566	1542
SG3	-	203	324	275	407	496

The strain observed during the drop testing of the bump interconnect samples was found to increase monotonically from the lowest to the highest drop height, and tended to level out at higher drop heights. One thing to note was that the strain SG2 in the die seemed to be either equal in magnitude to or greater than the strain SG1 observed in the board. This means that the bump interconnect model was transferring almost all the strain

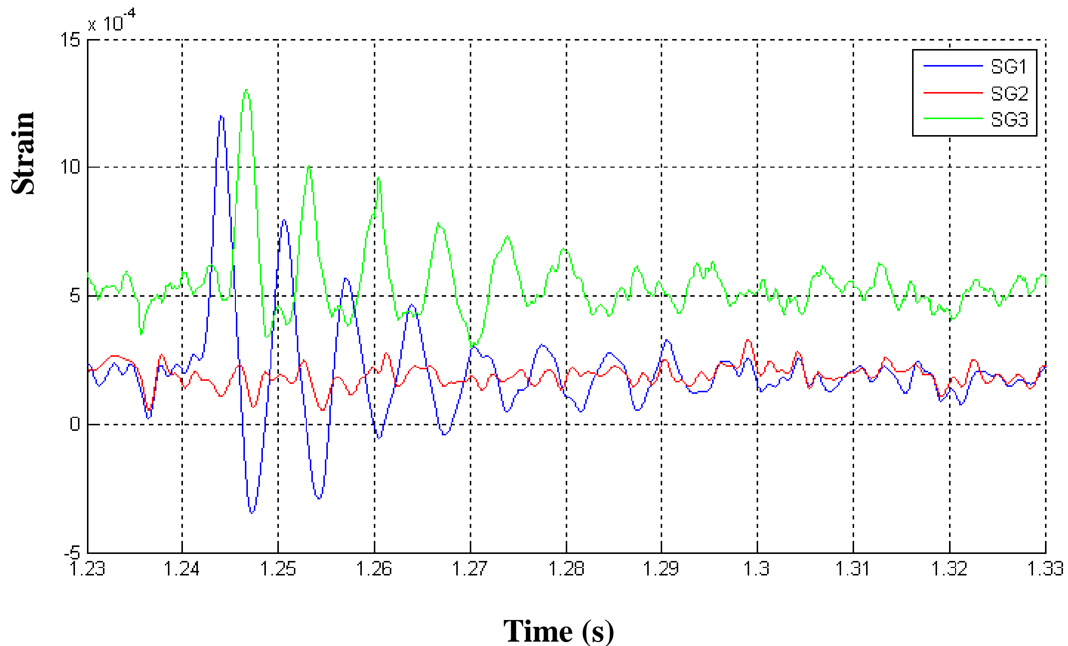


Figure 6.8: Strain data for 200mm height drop test for bump interconnect sample

from the board to the die due to the low compliance of the bump interconnects. At the same time, the transverse strain in the die SG3 seemed to be an average 26.8% of the strain SG2 in the die. Although this transverse strain response was expected, it still did not change the fact that the bump interconnects did not reduce the strain in the die compared to that in the board.

One thing to note is that the results for the 100mm height drop tests did not give out any strain value. The conclusion was that 100mm drop height was not sufficient to incite any large observable strain response which could be detected with the setup used, although the acceleration response was observed. Both the acceleration plot and strain data plot for the 100mm height drop test of the bump interconnect model are given in Figure 6.9 and Figure 6.10 respectively. Strain data plots for different drop heights are given in Appendix B.

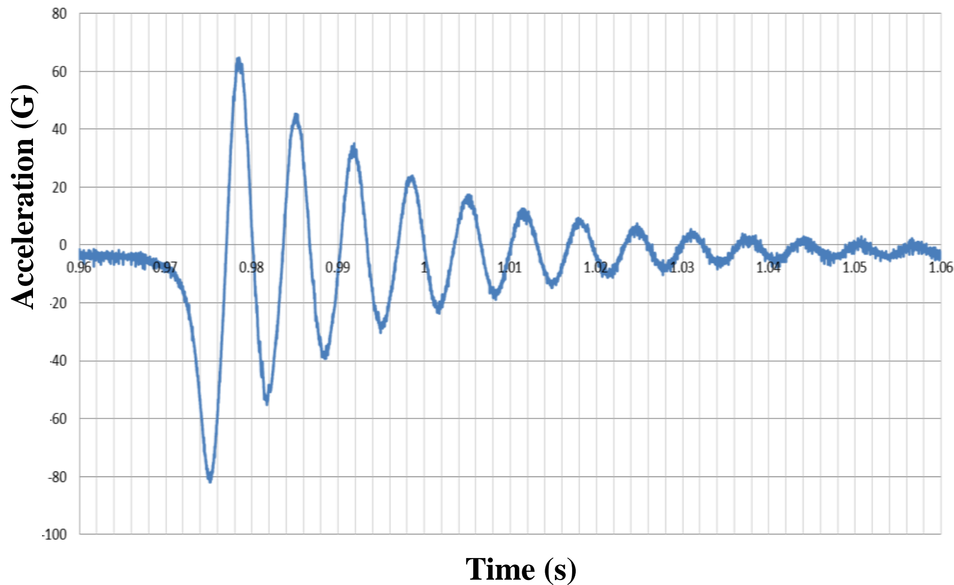


Figure 6.9: Acceleration response for 200mm height drop test for bump interconnect sample

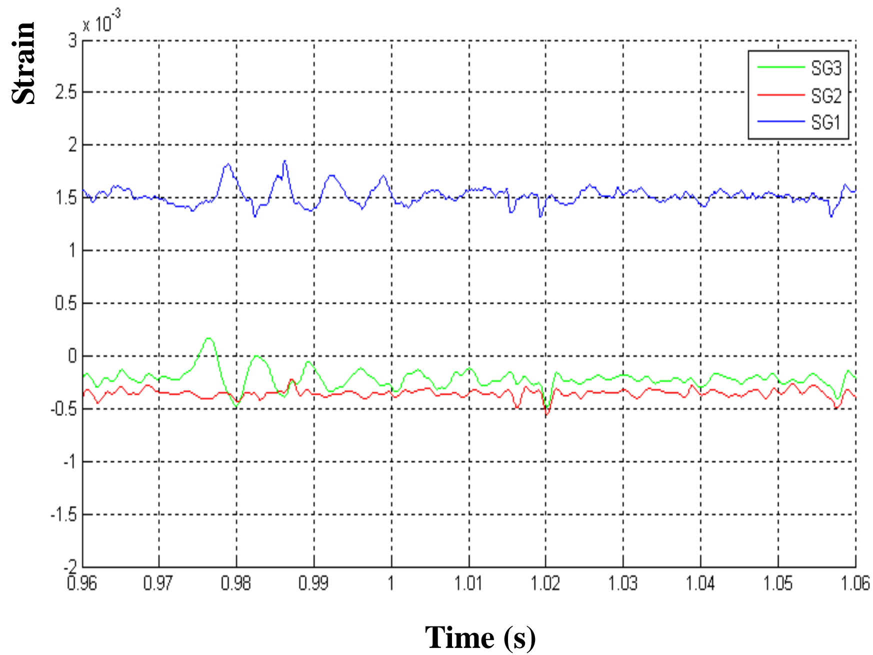


Figure 6.10: Strain data for 100mm height drop test for bump interconnect sample

6.3 Comparison of experimental response of three-arc interconnects and bump interconnects

On comparing the acceleration response of the three-arc compliant interconnects versus that of the bump interconnects, it can be seen that the compliant interconnects are subjected to higher peak acceleration values than the bump interconnects for the same drop heights. This is due to the overall higher rigidity of the bump assembly compared to the three-arc compliant interconnect assembly. At the same time, the impact times observed in the board for the three-arc interconnect assembly were found to be shorter for

higher drop heights. The acceleration peaks values and impact times for both interconnect geometries are given in Table 6.5.

Table 6.5: Experimental data comparison between three-arc and bump interconnect samples

Drop Height (mm)		100	200	300	400	500	600
Three-arc	Peak G	104.5	182.41	130.9	391.8	536.1	1056.8
	Impact Time (s)	0.01	0.008	0.005	0.003	0.002	0.0015
Bump	Peak G	81.87	202.6	269.49	352.9	394.9	766.7
	Impact Time (s)	0.008	0.007	0.006	0.005	0.004	0.003

The difference in acceleration response can be explained by considering the rigidity of the bump interconnects, which are much stiffer than the three-arc compliant interconnects due to the larger bump cross section (for the same footprint size). The bump interconnects prevent the board from flexing to a greater extent due to their rigid nature, while the compliant interconnects having much smaller bumps and flexible arms, allow the board to flex more easily. This allows the compliant interconnect drop test samples to undergo higher strains in the board, compared to the board strains in the bump interconnect drop test samples. This allows for higher acceleration values experienced by the three-arc compliant interconnect samples. This flexing nature also contributes to the change in impact times observed for both interconnect samples, with higher flexing leading to smaller impact times.

Table 6.6: Experimental strain data comparison between three-arc and bump interconnect samples

Drop Height (mm)		100	200	300	400	500	600
SG1	Three-arc	2256	3964	4291	5673	5774	6258
	Bump	-	1094	1334	1624	1853	1765
SG2	Three-arc	312	495	879	1006	1008	1069
	Bump	-	748	1109	1408	1566	1542
SG3	Three-arc	250	305	692	646	562	441
	Bump	-	203	324	275	407	496

On comparing the strain response of both interconnect geometries, as shown in Table 6.6, it can be seen that the bump interconnect samples underwent lower board strains compared to the three-arc interconnects, which was expected based on the lower peak acceleration values experienced as shown in Table 6.5. However, the amount of strain transferred from the board to the die (SG1 versus SG2) is much smaller in the case of the three-arc interconnects compared to the bump interconnects. The SG2 strain values are actually lower in the three-arc interconnect drop test samples compared to the bump interconnect samples, despite the higher board strains in the former. The strain ratio (board strain to die strain) is on average 5.85:1 for the three-arc compliant interconnect samples versus 1.22:1 for the bump interconnect samples. This strain ratio response displays the excellent strain absorption capability of the three-arc compliant interconnect structure versus the rigid bump interconnect geometry, which is used in conventional microelectronic packages.

6.4 Three-arc compliant interconnect finite-element simulation results

Alongside the experimental drop tests, finite-element simulations based on the Input-G Method were conducted, in an effort to obtain drop test response behavior of the three-arc compliant interconnects through numerical simulation. By obtaining this numerical data, the response of the compliant interconnects could be understood in a much faster manner than conducting the actual experimental drop tests.

Simulations were carried out for three out of the six drop heights used in experiment. The drop test heights used for obtaining simulations results were 100mm, 300mm and 500mm. The impact times and peak acceleration data were taken from experiment and applied to the finite-element simulation model. The nature of the implicit formulation used for the finite-element simulation allowed the strain response data to be used as a comparative estimate versus the experimental results.

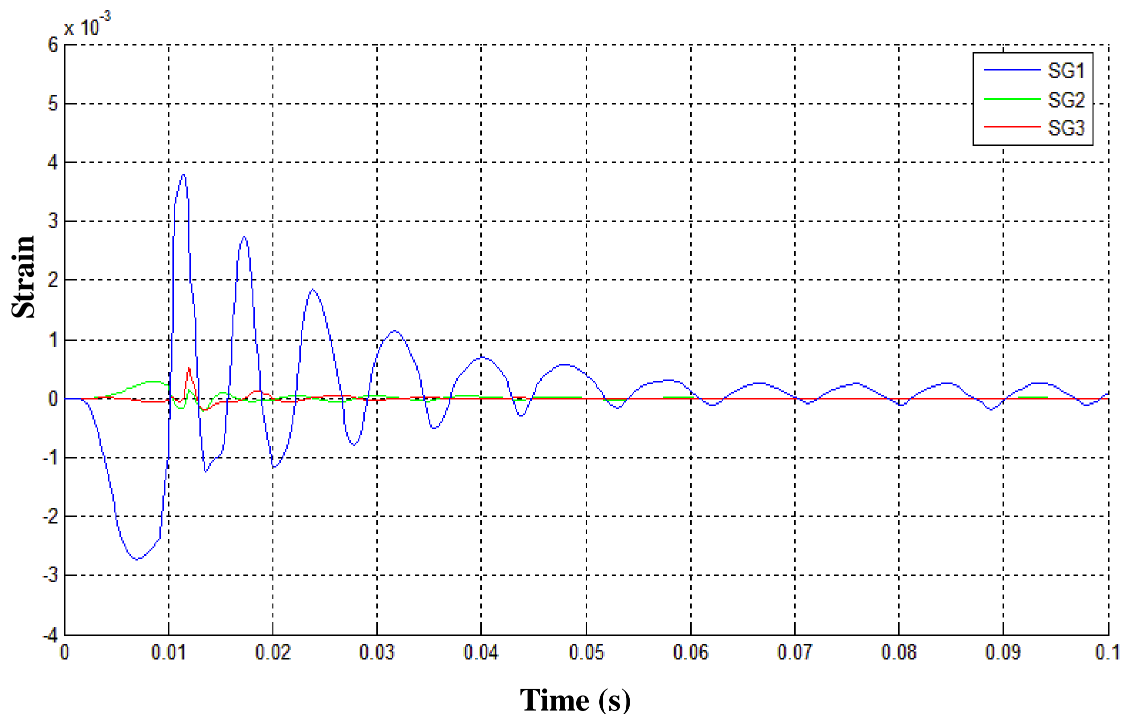


Figure 6.11: Strain data for 100mm height drop test simulation for three-arc interconnect model

Shown in Figure 6.11 is the strain response plot for a 200mm drop test simulation conducted for the three-arc compliant interconnect geometry. The various strain response plots are given in Appendix C.

The strain data observed from finite-element simulations are given in Table 6.7, where the values are compared against the experimental results obtained. It can be seen that the peak strain values obtained through simulation were within reasonable error, when compared with the experimental results. In most cases, the finite-element simulations under-predicted the strain response of the three-arc compliant interconnect models. This could be attributed to the effect of polymer ageing in the experimental drop test samples. The finite-element simulations were conducted using the original material property values for the polymer resin, thus leading to lower strains displayed in simulation. At the same time, the damping ratio applied during simulation was obtained from experiment. The amount of strain absorbed by the compliant interconnects in simulation, however, seemed to be in the same ratio as in experiment. Additionally, both experiment and simulation data were seen to damp out within the same amount of time, the time being dependent on the drop test height, but always within 100ms.

Table 6.7: Experiment versus simulation strain data comparison for three-arc interconnect

Drop Height (mm)		100	300	500
SG1	Experimental	2256	4291	5774
	Simulation	2754	4675	5026
SG2	Experimental	312	879	1008
	Simulation	257	504	689
SG3	Experimental	250	692	562
	Simulation	201	302	442

It was concluded that the finite-element simulation by implicit Input-G Method could be used to obtain preliminary data on drop test response of the three-arc compliant interconnects. The amount of time taken by each simulation was in excess of 20 hours due to the size of the simulation model and the small time step used for solution. This time was still much smaller than the amount of time it took to design, fabricate, set up and test the three-arc interconnect samples through experiment.

6.5 Bump interconnect finite-element simulation results

Finite-element simulations of the bump interconnect model were also conducted using the same Input-G Method as in the case of the three-arc interconnects. Again,

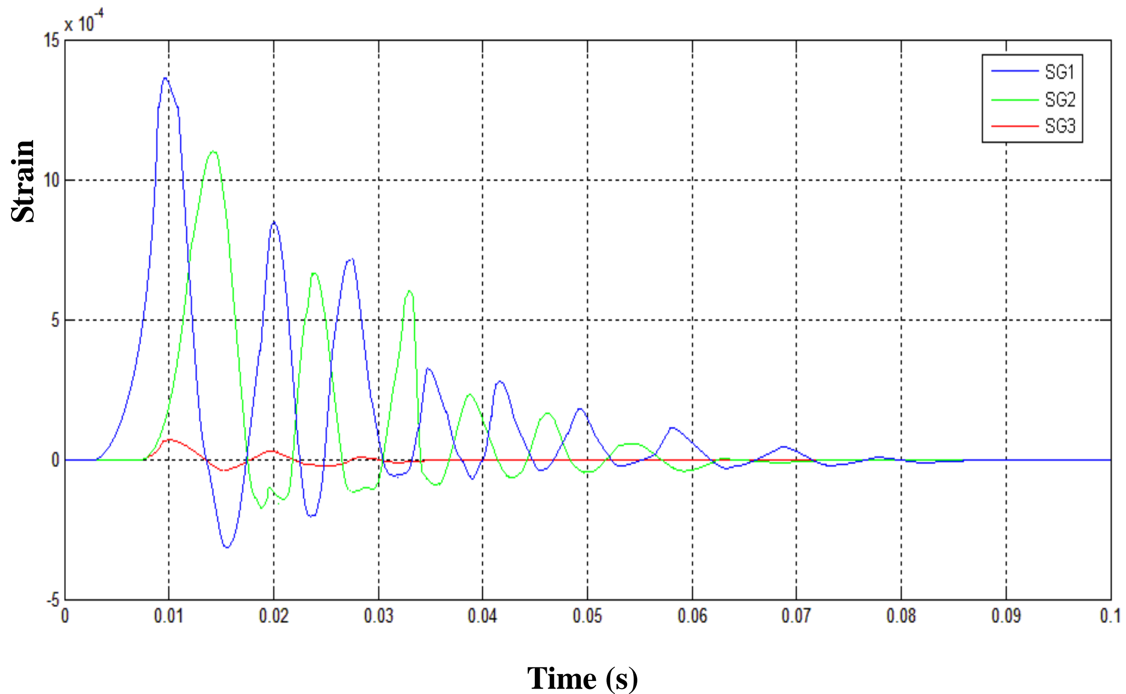


Figure 6.12: Strain data for 200mm height drop test simulation for bump interconnect model

200mm, 300mm and 500mm drop height experimental test data was used to conduct the simulations for the bump interconnect geometry. Shown in Figure 6.12 is the 200mm height drop test strain response of the bump interconnect. The peak strain values obtained from this and other strain response plots (given in Appendix C) are given in Table 6.8 alongside the experimental results obtained for the same drop heights.

Table 6.8: Experiment versus simulation strain data comparison for bump interconnect

Drop Height (mm)		200	300	500
SG1	Experimental	1094	1334	1853
	Simulation	1329	1586	2071
SG2	Experimental	748	1109	1566
	Simulation	1166	1387	1731
SG3	Experimental	203	324	562
	Simulation	105	253	407

It was seen that the finite-element simulation strain values for various drop heights was within reasonable error. The finite-element simulations conducted overpredicted the strain results due to change in the material properties, as given in Chapter 5 for the bump interconnect. The finite-element simulation data seemed to follow the same trends as the experimental results, with the strain in the die being shown to be close to the strain in the board, as was seen in experiment. The strain ratio from the board to the die was 1.16:1.

It was concluded that the implicit Input-G Method used to conduct numerical simulations of the drop testing of the bump interconnect model was sufficient to obtain preliminary data on drop test behavior of the bump interconnect models used to obtain comparative strain data.

CHAPTER 7

PROPOSED COPPER-SILICON INTERCONNECT-DIE ASSEMBLY SIMULATION

In previous chapters, experimental and numerical data gathered from scaled up compliant interconnects was presented. These data were based on the drop test samples fabricated by stereolithography and made use of the stereolithographic polymer resin. While the data obtained from such samples gave good insight into the mechanical behavior of the compliant interconnects, response of the original interconnects when subjected to drop testing is yet to be understood. This chapter will deal with finite-element simulation data for two compliant interconnect geometry sizes. The first size will deal with the scaled up geometry, but with the material properties used in the true package. The second size will deal with the true scale complaint interconnects, again modeled using the original copper-silicon interconnect-die assembly material properties. As no experimental drop test data is yet available for copper interconnect/silicon die /FR4 board assembly, the discussion presented in this chapter is preliminary and needs to be validated with experimental data, as outlined in the next chapter. However, this chapter provides certain insight into the drop impact behavior of compliant copper interconnects.

As was given in Chapter 4, the compliant interconnect geometry studied up until now was scaled up by a factor of 75. The new scaled up pitch used for fabrication was 15mm. This scaling up was done in order to comfortably fabricate the three-arc geometry using stereolithography without losing any dimensional accuracy, and also to take the resolution of the stereolithography machine into account. However, the original scale or true scale multi-path three-arc compliant interconnects are meant to be fabricated at a

pitch of 200μm. Such small dimensions necessitate the need for photolithographic fabrication. The steps needed to fabricate this compliant interconnect geometry are currently under development. It should be noted that all the other dimensions of the multi-path three-arc compliant interconnect such as width, length, thickness and height are calculated based on the provided pitch, making this interconnect geometry truly scalable.

7.1 Scaled-up copper-Silicon Interconnect-Die assembly

In order to transition from the scaled up compliant interconnect geometry with polymer material properties used till now to the true scale copper-silicon interconnect-die assembly model, an intermediate model was studied, using the scaled up geometry of the compliant interconnects with the material properties of the true scale copper-silicon interconnect-die assembly.

7.1.1 Model geometry

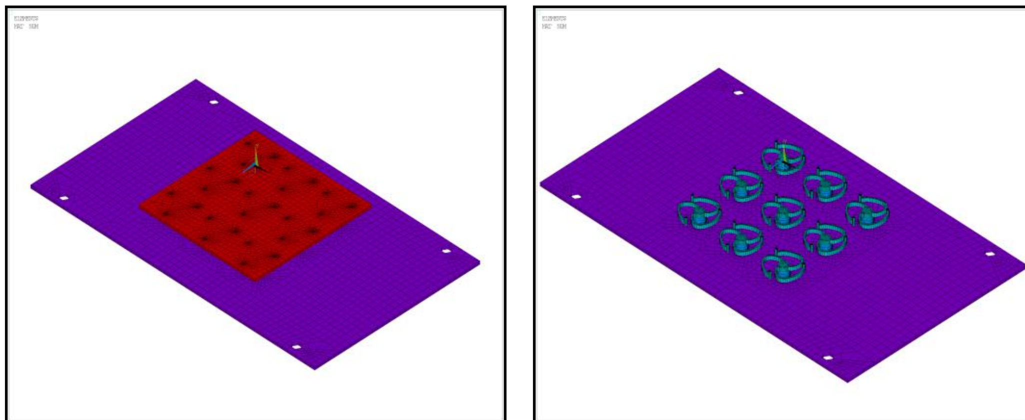


Figure 7.1: Three-arc Cu interconnect/Si die assembly model

Shown in Figure 7.1 is the scaled-up geometry used for finite-element simulation of the three-arc compliant interconnects. As has been given before, this geometry consists

of a board (110mm by 64mm by 1mm) and a die (45mm by 45mm by 1mm) sandwiching a 3 by 3 area-array of scaled up three-arc compliant interconnects. The geometry for this simulation was thus the same geometry used in previous simulations. The entire geometry as modeled using 8-noded SOLID185 elements, with finer mesh closer to the interconnects and coarser mesh away from the package.

7.1.2 Material Properties

As a transition model, the currently presented geometry was modeled using material properties meant to be used in the true scale copper-silicon interconnect-die assembly model. The various material properties used for this simulation as well as the parts modeled using the same are given in Table 7.1.

Table 7.1: Material Properties used in simulation [Lall et al, 2009]

Material	Geometry	Young's Modulus (GPa)	Poisson's Ratio	Density (Kg/m^3)
Copper	Interconnect	129	0.34	8900
FR4 (substrate)	Substrate/Board	16	0.3	2243
Solder	Solder bump	49.229	0.4	7420
Silicon	Die	117.61	0.25	2329

7.1.3 Boundary Conditions

The scaled-up compliant interconnect model with copper-silicon material properties specified in Table 7.1 was loaded using boundary conditions that were obtained from the 500mm drop height test of the experimental three-arc compliant interconnect polymer model. Figure 7.2 gives the acceleration and displacement curves applied to the currently presented geometry. As before, the displacement boundary

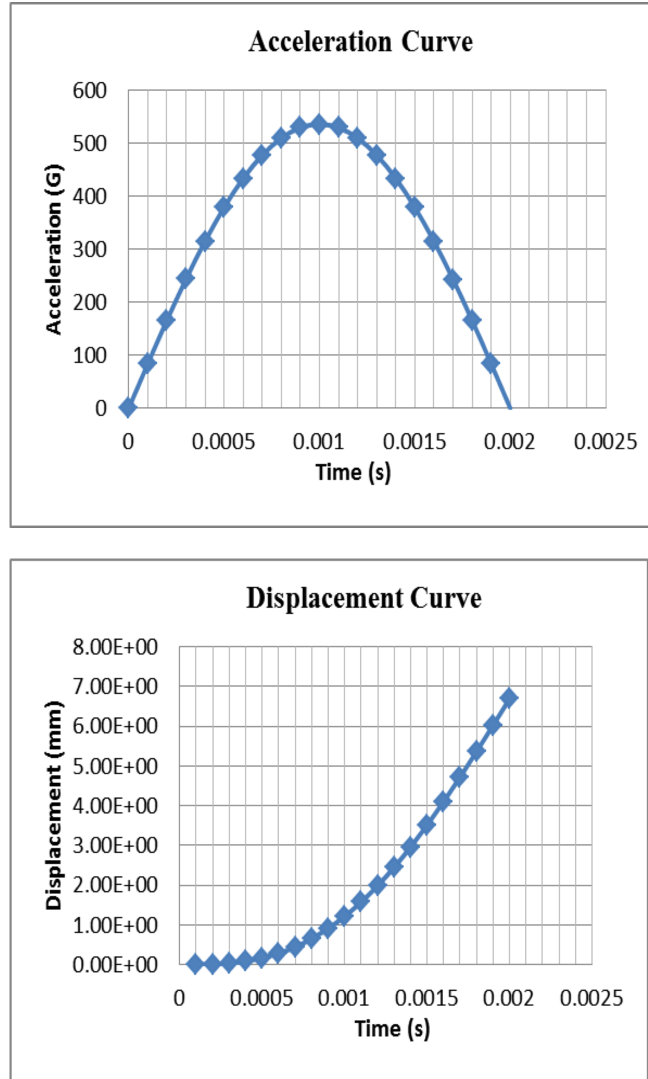


Figure 7.2: Acceleration and calculated displacement curves for 536.1G drop event from 500mm drop height

conditions were applied at the four screw holes provided in the model to mimic the presence of supports. A damping ratio of 0.095 was applied to the model in order to mimic real world response. This damping ratio was used to calculate the corresponding Rayleigh damping coefficients, α and β, which were then used in the finite-element simulation to obtain the required damping.

7.1.4 Results

On running the finite-element simulation of the above explained model, it was seen that the overall response of the structure damped out within 15ms. This was much smaller in duration compared to the approximately 100ms it took for the polymer samples to damp out and can be explained due to the higher stiffness of the FR4 material used to model the board. The strain response of the model was studied using the same technique as in previously studied finite-element drop test simulation models.

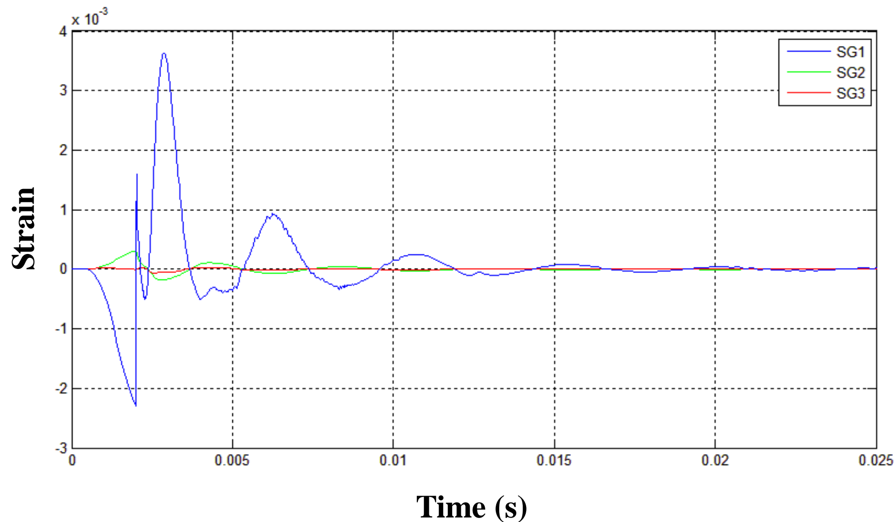


Figure 7.3: 500mm drop height finite-element simulation strain data for 150-scale Cu/Si three-arc assembly model

The strain in the board along the longitudinal direction (given by SG1) was found to peak at a maximum of 3633.9 microstrain. In comparison, the peak strain in the die parallel to the length of the board (given by SG2) was 308 microstrain, an order smaller than SG1. Additionally, the transverse strain in the die (SG3) was found to be 64.1 microstrain. Comparing the strain values for SG1 and SG2, it can be seen from Figure 7.3 that the board to die strain ratio was 11.8:1. The scaled-up copper compliant interconnects were thus able to reduce the amount of strain transferred to the die by a

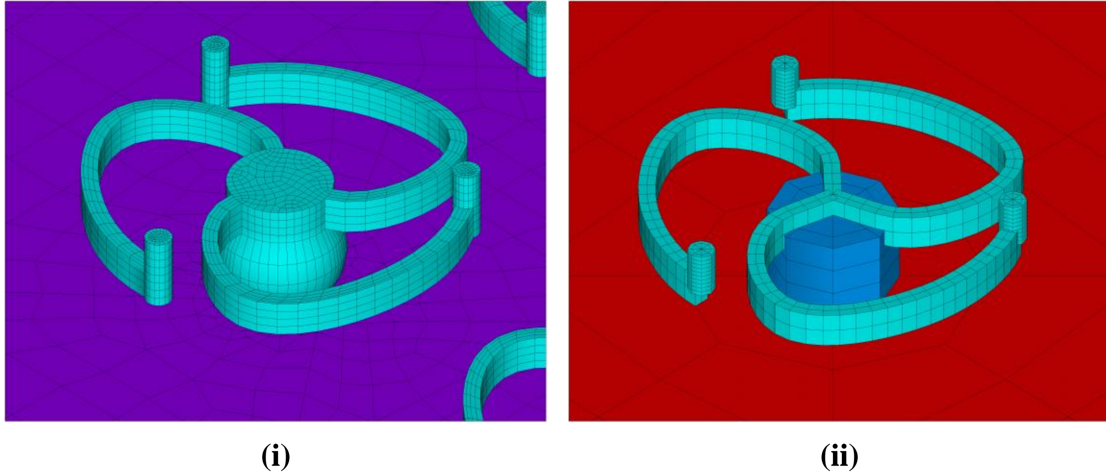
factor of 10. This response is roughly twice as much as what was seen with the polymer interconnects. Although the polymer interconnects are more compliant than the copper interconnects, the current simulations use a silicon die which is much stiffer than the polymer die used in earlier simulations. Therefore, the increase in interconnect stiffness is offset by the increase in die stiffness to result in reduced transfer of board strain to die strain.

7.2 True scale Copper-Silicon Interconnect-Die assembly

In order to understand the behavior of the true scale compliant interconnects, a finite-element simulation using the true scale dimensions of the compliant interconnects was run.

7.2.1 Model Geometry

The true scale compliant interconnect geometry necessitates a pitch of 200µm, with the other dimensions of the compliant interconnect structure suitably related to this pitch. The amount of time it took to solve the scaled-up compliant interconnect geometry models gave a fair estimation of exactly how long the true scale geometry might take to solve. Therefore, in order to reduce computational time and improve efficiency, the true scale compliant interconnects were modeled using 3-noded BEAM189 elements. A force and moment study was done between the interconnect geometry modeled at true scale using both SOLID188 elements and BEAM189 elements, in order to understand the differences that may arise during solution. Given in Figure 7.4 is the three-arc compliant interconnect geometry modeled using solid elements and beam elements.



(i) (ii)

Figure 7.4: Three-arc compliant interconnect simulation model built using – (i) SOLID elements (ii) BEAM elements

It can be seen from Figure 7.4 that the number of elements needed to model each interconnect using beam elements was much lower than that needed when modeling using solid elements. This approach would make the overall simulation more efficient by reducing the number of elements required. Care was taken to ensure that the dimensions of both the models were kept the same. Then, using material properties as specified in Table 7.1, the compliance of both structures was studied. Figure 7.5 compares the compliance values for both the interconnect structures.

From the comparison, it was seen that the compliant interconnect modeled with solid elements had a compliance of 1.7mm/N out-of-plane while the compliant interconnect modeled using beam elements had a compliance of 1.91mm/N out-of-plane. This difference in compliance values was kept in mind when using the beam elements for the following simulation.

The geometry used for conducting the finite-element simulation of the true scale compliant interconnect geometry is given in Figure 7.6. A quarter symmetry model was used to reduce computational time. The interconnects were modeled as beams using

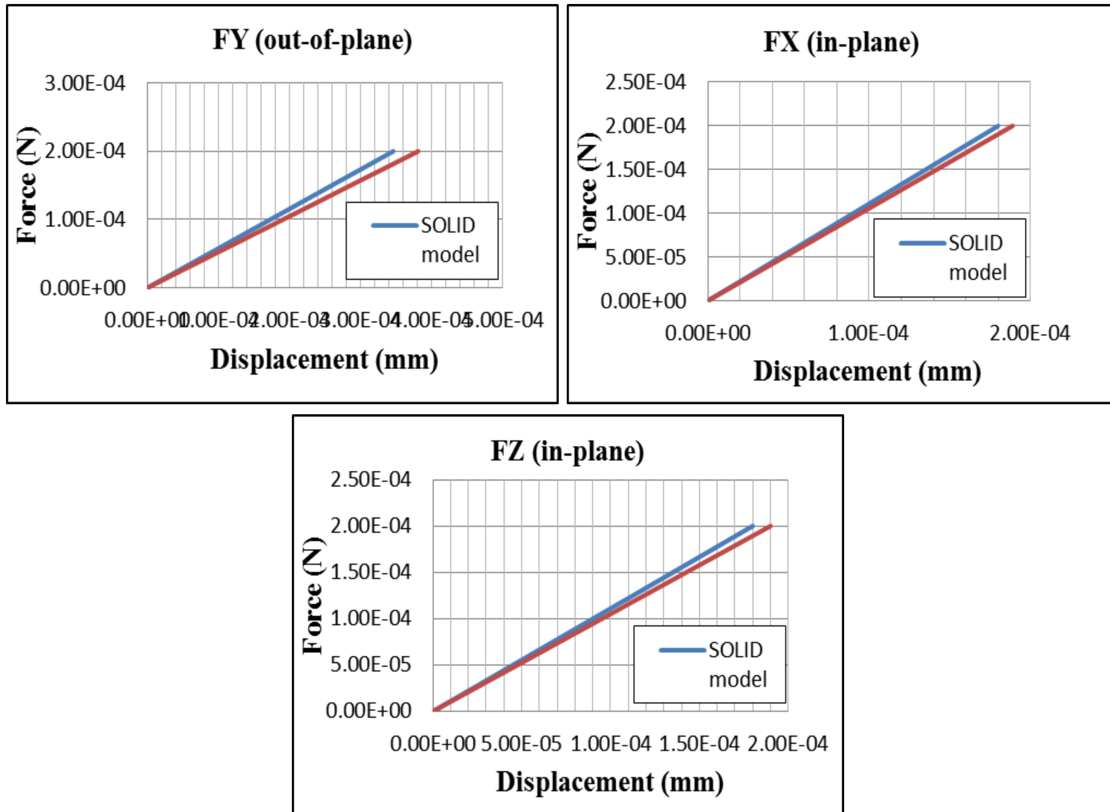
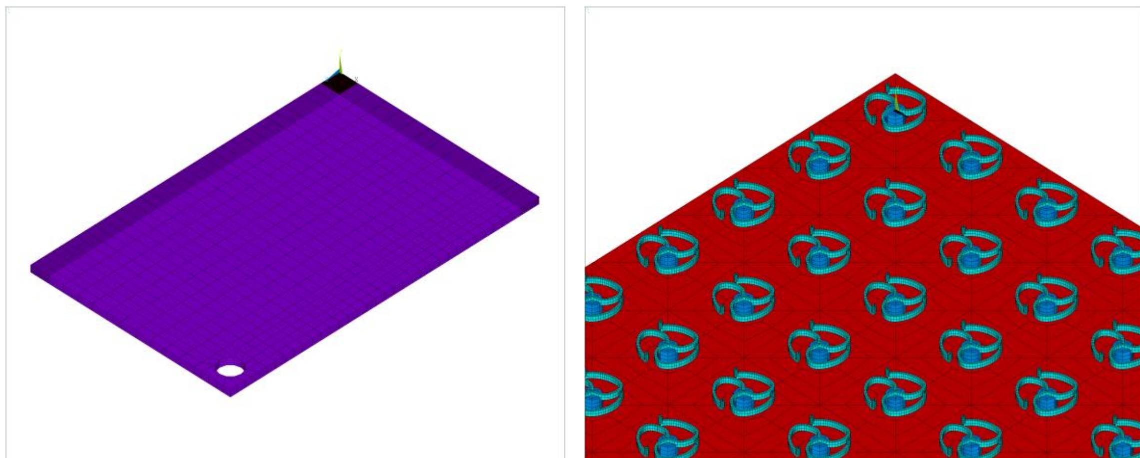


Figure 7.5: SOLID versus BEAM force-displacement studies



(i) **(ii)**

Figure 7.6: True scale complaint interconnect simulation geometry - (i) Quarter symmetry model (ii) Close-up of three-arc compliant interconnects modeled using BEAM elements

BEAM189 elements with a pitch of 200μm. A 5mm by 5mm die was used above the interconnects, although the die thickness was reduced to 400μm compared to previous

simulations. The substrate/board used for the simulation was 110mm in length, 64mm in width and 1mm in thickness.

7.2.2 Material Properties

The material properties used for the true scale compliant interconnect model comprised of BEAM element interconnects were the same as the ones used for the scaled up copper-silicon assembly model. The material properties are given in Table 7.1.

7.2.3 Boundary Conditions

Unlike other simulations, the interconnects used in the current simulation were modeled using BEAM189 elements. Beam elements inherently contain 6 degrees of freedom. Therefore, to prevent rotation about the three orthogonal axes, the beam

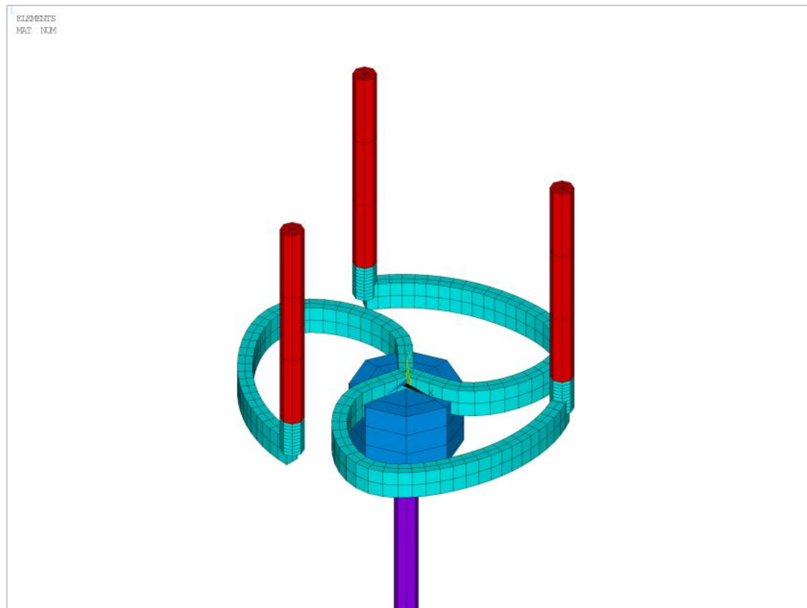


Figure 7.7: Extended BEAM elements used for 'zippering' the interconnect to surrounding elements

elements used to model the interconnects were rotationally constrained in the three directions. In addition, the posts of the interconnect as well as the beam element representing the solder bump were extended into the solid elements surrounding the interconnects. This, in effect, 'zippered' the beam elements to the surrounding solid elements, thus preventing any sort of nodal rotation about any of the three axes. Shown in Figure 7.7 are the extended arms and solder bump element used for 'zippering' the interconnect to the surrounding elements.

Being a quarter symmetry model, the free symmetry edges of the model were bound using symmetry boundary conditions. All the boundary conditions mentioned so far were utilized throughout the solution of the model.

The actual displacement boundary conditions that create the drop test were applied to the screw hole present in the model as shown in Figure 7.6. A 500mm drop height with a peak acceleration of 536G was used, with an impulse time of 2ms. The acceleration and displacement boundary conditions applied are the same as that used for the previously studied finite-element model and are given in Figure 7.2.

7.2.4 Results

The obtained averaged strain data plot is shown in Figure 7.8. It was observed that the board strain along the longitudinal direction of the board was approximately 650.6 microstrain (SG1). In comparison, the strain in the die along the same direction as the board strain was 60.5 microstrain (SG2) while the transverse die strain was approximately 29.3 microstrain (SG3).

It can be seen that the die strains were an order of magnitude lower than the corresponding board strains. The board to die strain ratio observed for this simulation was

10.75:1, displaying the excellent strain absorbing capability of the multi-path three-arc compliant interconnect used in the package.

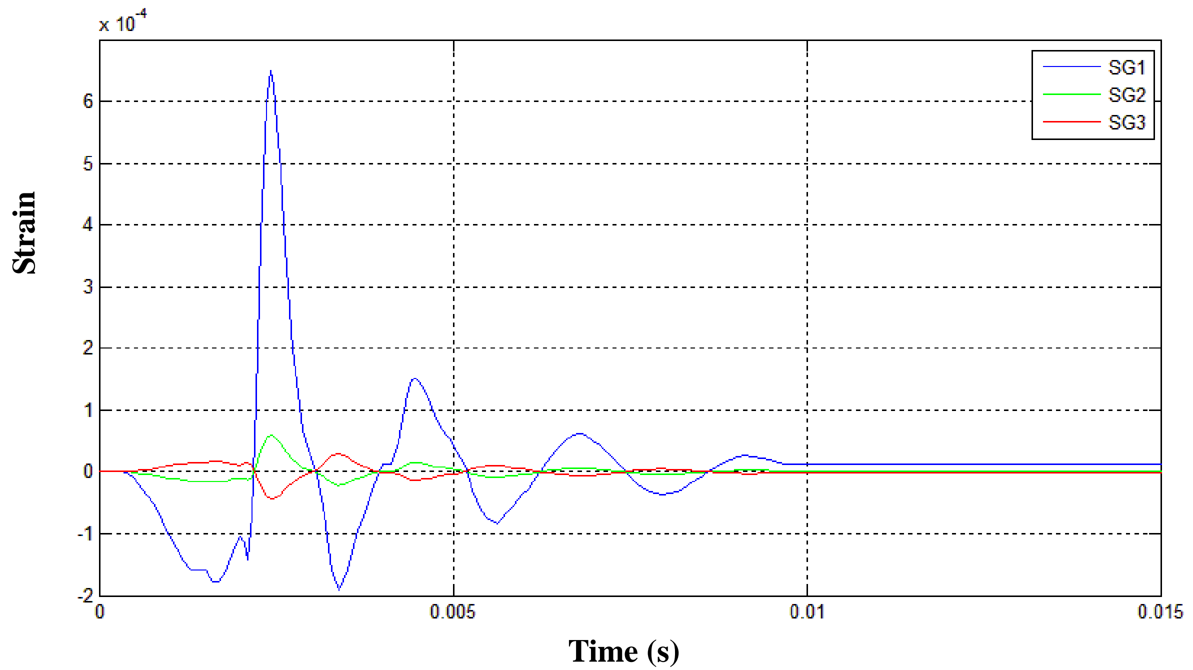


Figure 7.8: 500mm drop height finite-element simulation for true scale copper-silicon interconnect-die assembly model

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

The purpose of this thesis was to understand the response of a proposed compliant interconnect design when subjected to drop and impact loading. The following conclusions were arrived at after conducting the experimental and numerical analysis presented in this thesis.

- The JEDEC standard drop test can be adequately conducted using impact testing machines by suitably modifying the available components.
- Stereolithography is a quick low-cost alternative to photolithographic fabrication, in order to understand response behavior of packaged structures subjected to drop and impact loading.
- The Input-G Method provides an accessible solution method for conducting finite-element simulation studies on drop testing using commonly available implicit solvers.

Of the compliant interconnects themselves, the following conclusions could be made.

- The multi-path three-arc compliant interconnect geometry is capable of reducing die strains by acting as a damper. It absorbs the strains being transferred from the board to the die and thus, will prevent excessive stress development in the die.
- Compared to more conventionally used rigid bump interconnects, the three-arc compliant interconnect is capable of reducing die strains to values less than that

seen in packages with bump interconnects having the same footprint as the three-arc interconnect considered.

- Based on the observed data, a possible use for the three-arc compliant interconnect geometry is in the form of vibration isolators. The three-arc compliant interconnect geometry showed excellent damping abilities and thus may be used as a vibration isolator in MEMS devices, or at the second-level interconnect stage.

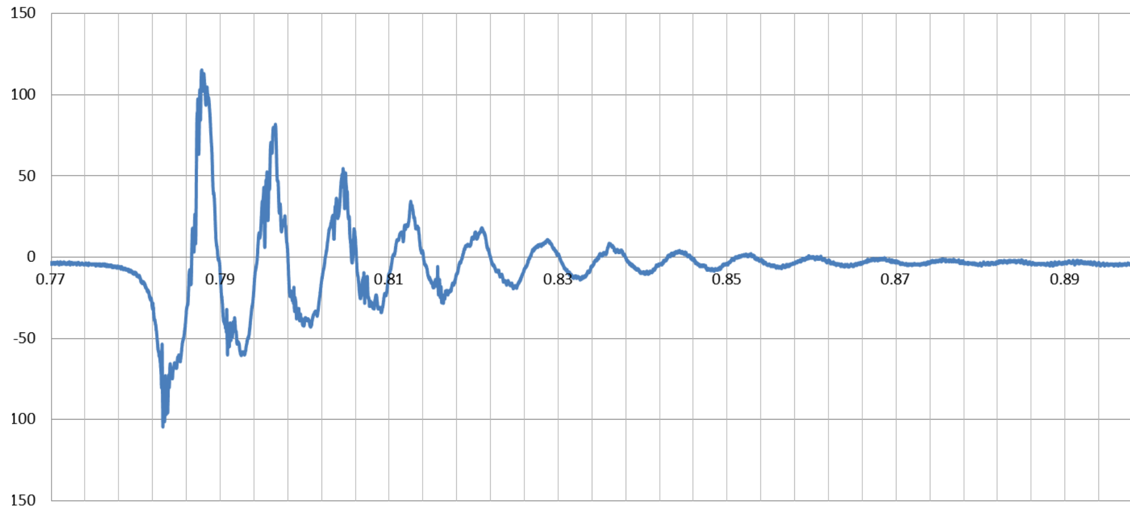
8.2 Future Work

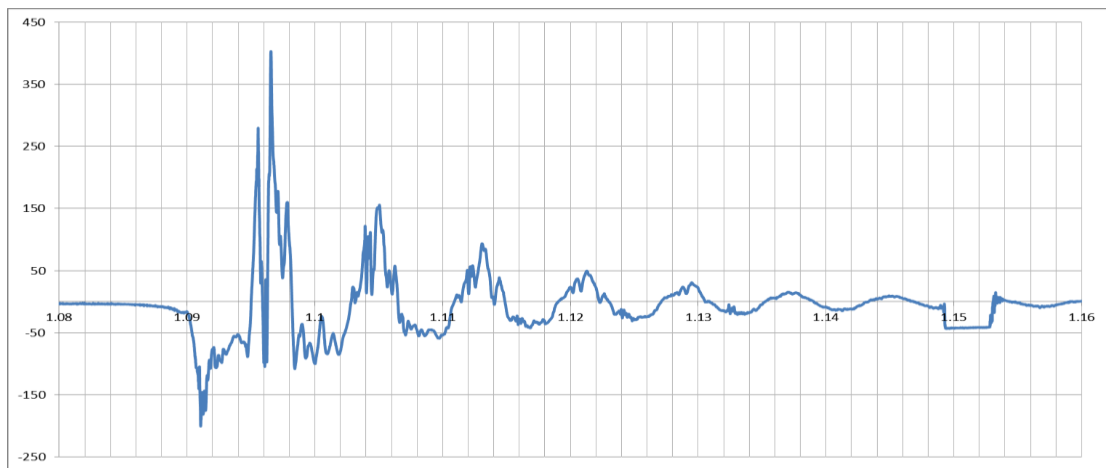
The following are recommendations for future work:.

- Conduct experimental drop testing of true-scale copper-silicon interconnect-die assembly and validate results from the finite-element simulations
- Conduct drop testing for heights and impulse times as specified in JEDEC standards, using appropriate damping mechanisms [JESD22-B110a].
- Perform numerical simulations using explicit solvers to provide comparative validation of conducted implicit finite-element simulations.
- Investigate the effect of different damping mechanisms to freely control impact time.
- Study the effect of drop testing using orientations other than the 0° drop.
- Study the effect of clattering and multiple consecutive impacts due to free-fall.
- Study the effect of varying geometry parameters of the compliant interconnect on the amount of strain transferred from the substrate to the die.
- Study the drop test reliability of other compliant interconnect geometries.

APPENDIX A

EXPERIMENTAL DROP TESTING ACCELERATION DATA





Time (s)

Fig A1.2: 200mm drop height acceleration data for three-arc interconnect sample

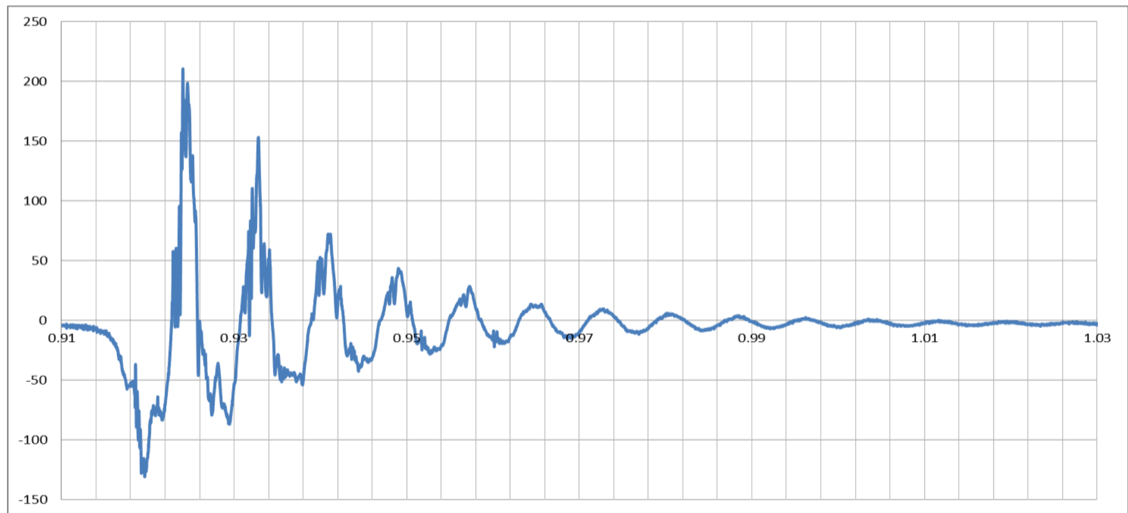


Fig A1.3: 300mm drop height acceleration data for three-arc interconnect sample

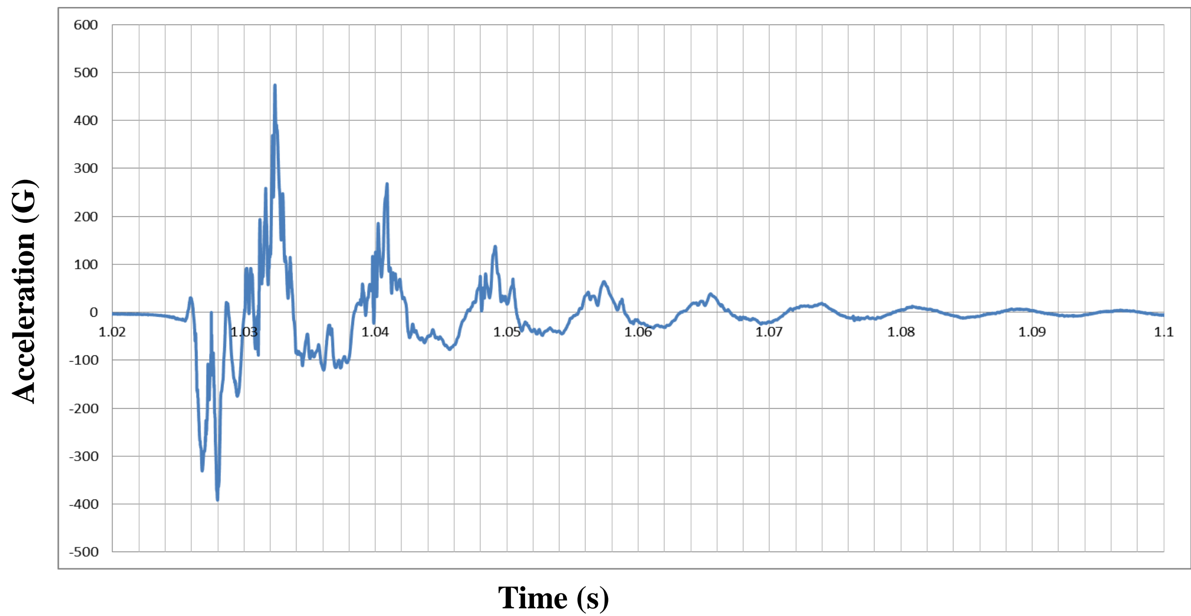


Fig A1.4: 400mm drop height acceleration data for three-arc interconnect sample

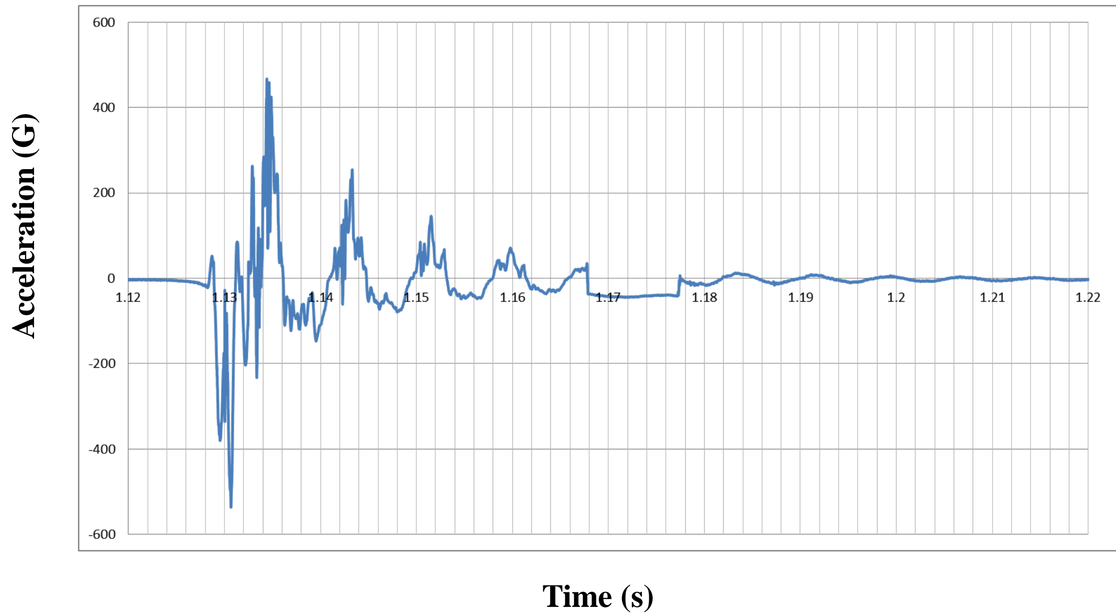


Fig A1.5: 500mm drop height acceleration data for three-arc interconnect sample

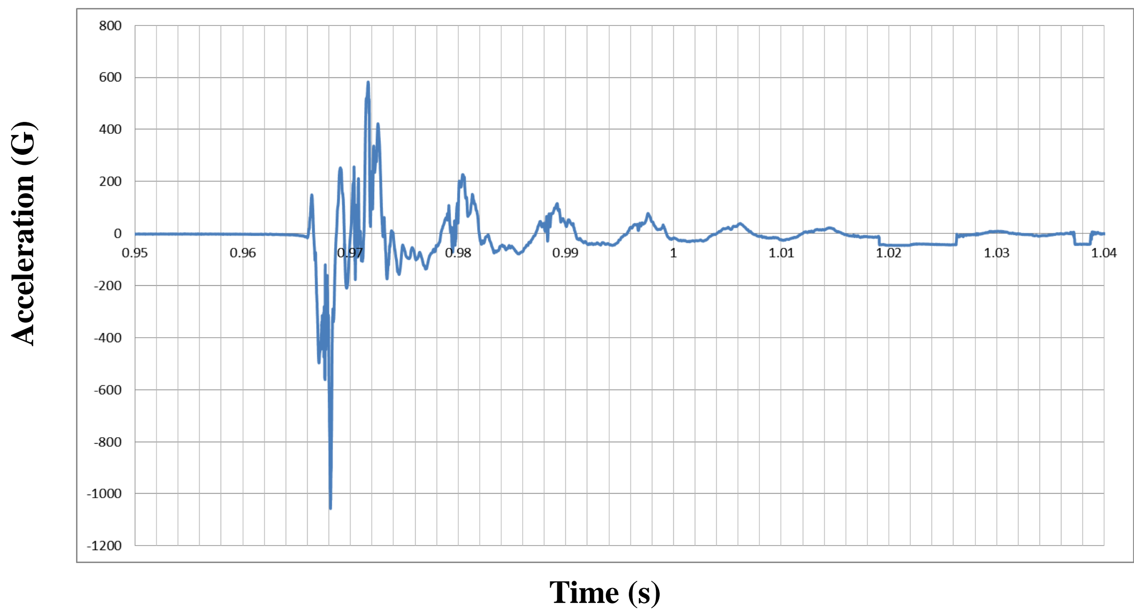


Fig A1.6: 600mm drop height acceleration data for three-arc interconnect sample

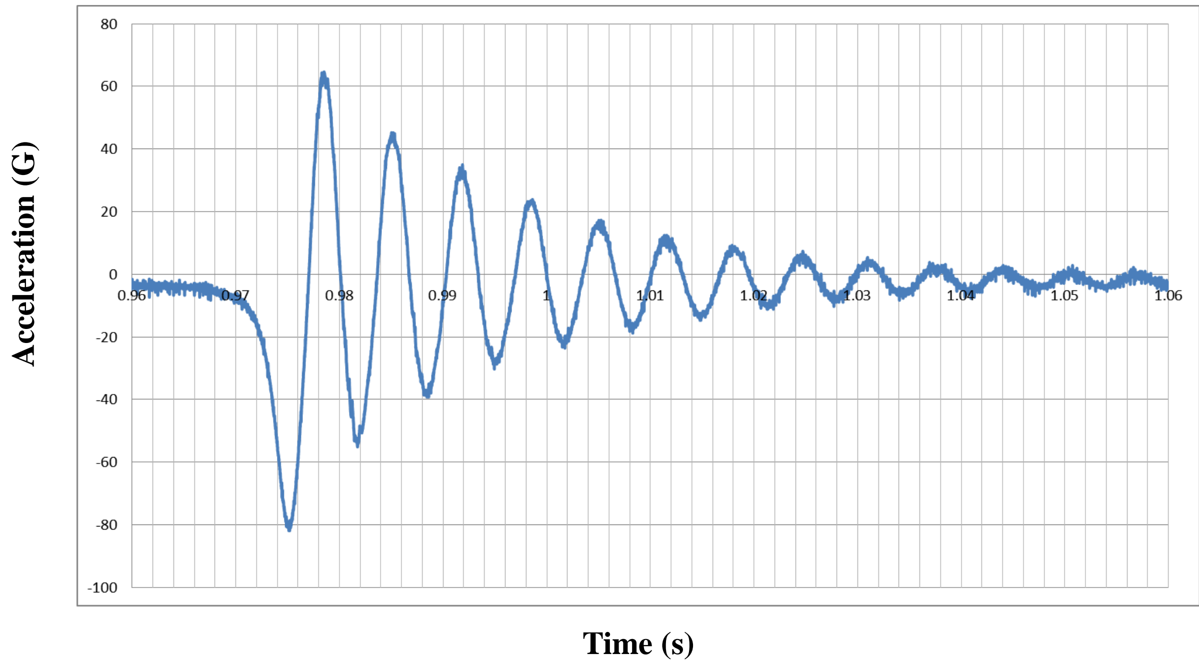


Fig A1.7: 100mm drop height acceleration data for bump interconnect sample

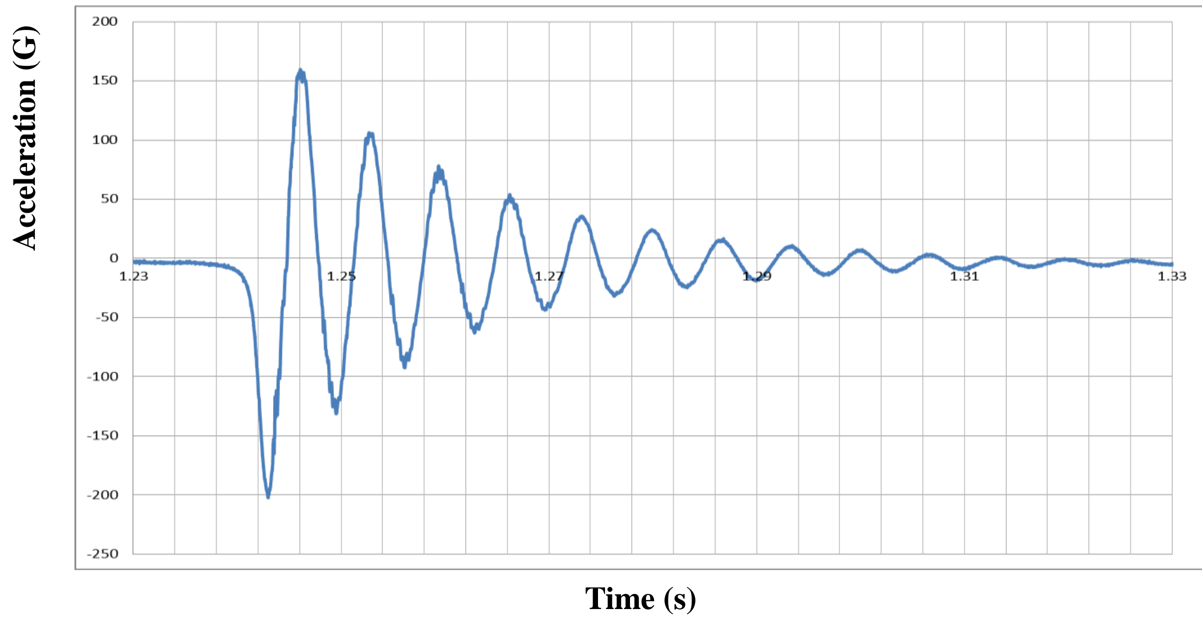


Fig A1.8: 200mm drop height acceleration data for bump interconnect sample

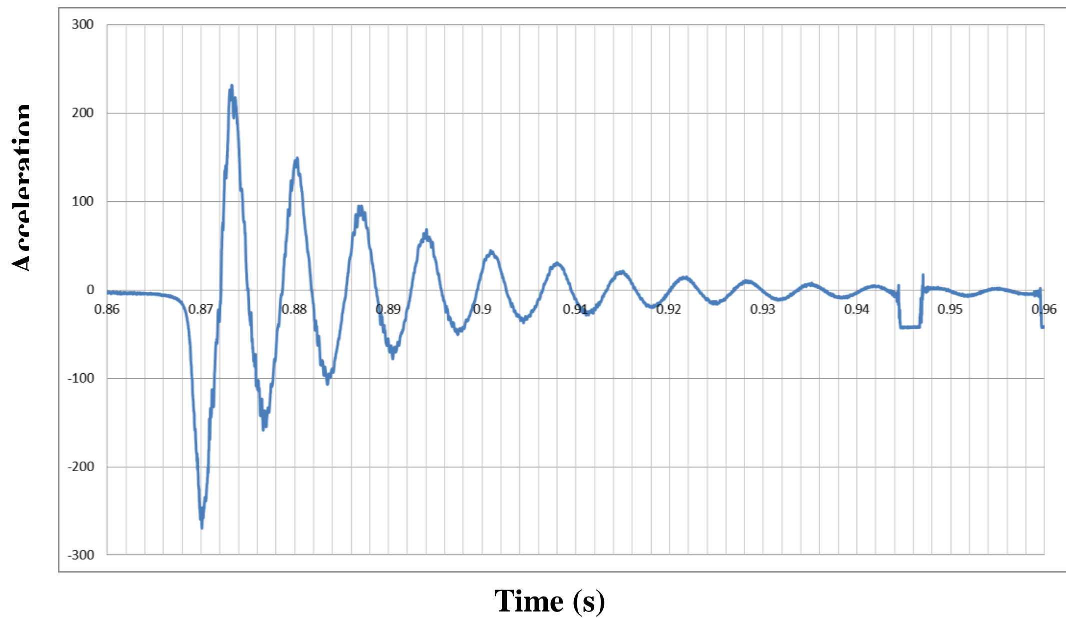


Fig A1.9: 300mm drop height acceleration data for bump interconnect sample

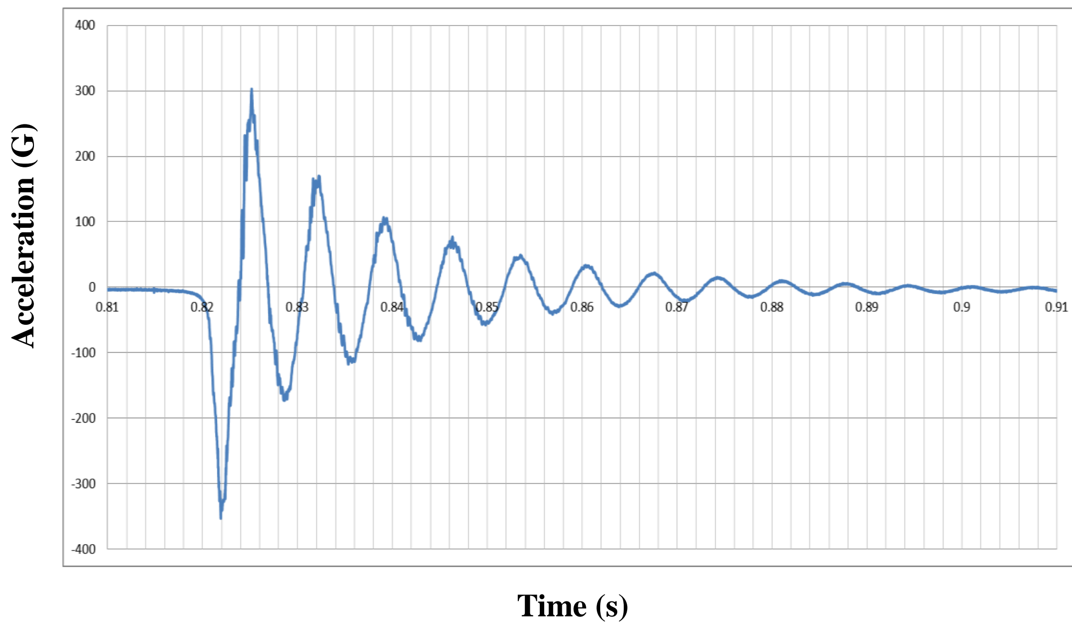


Fig A1.10: 400mm drop height acceleration data for bump interconnect sample

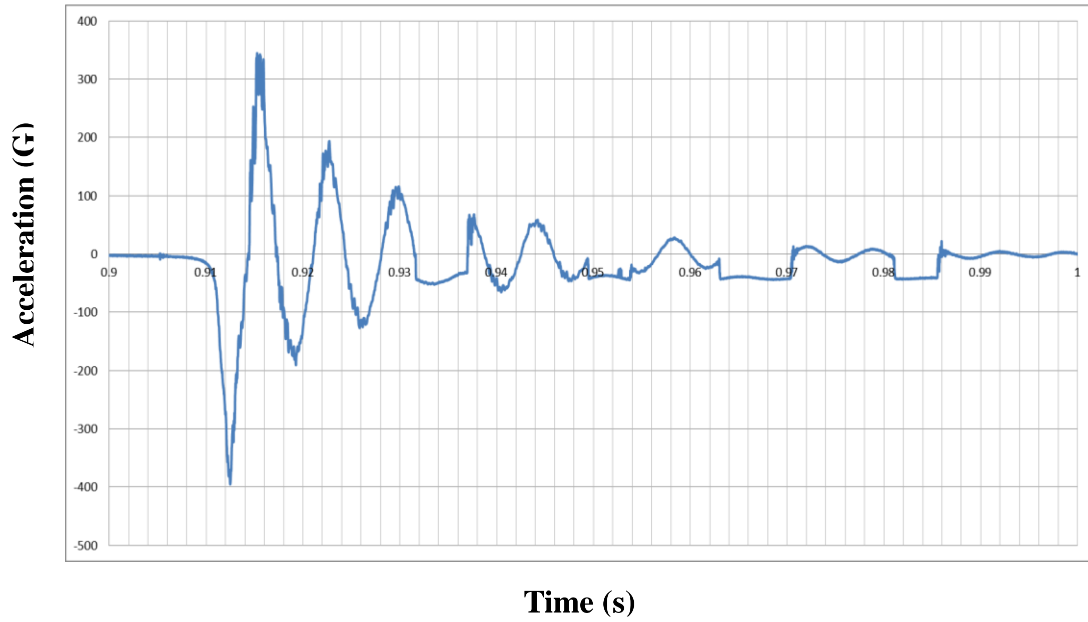


Fig A1.11: 500mm drop height acceleration data for bump interconnect sample

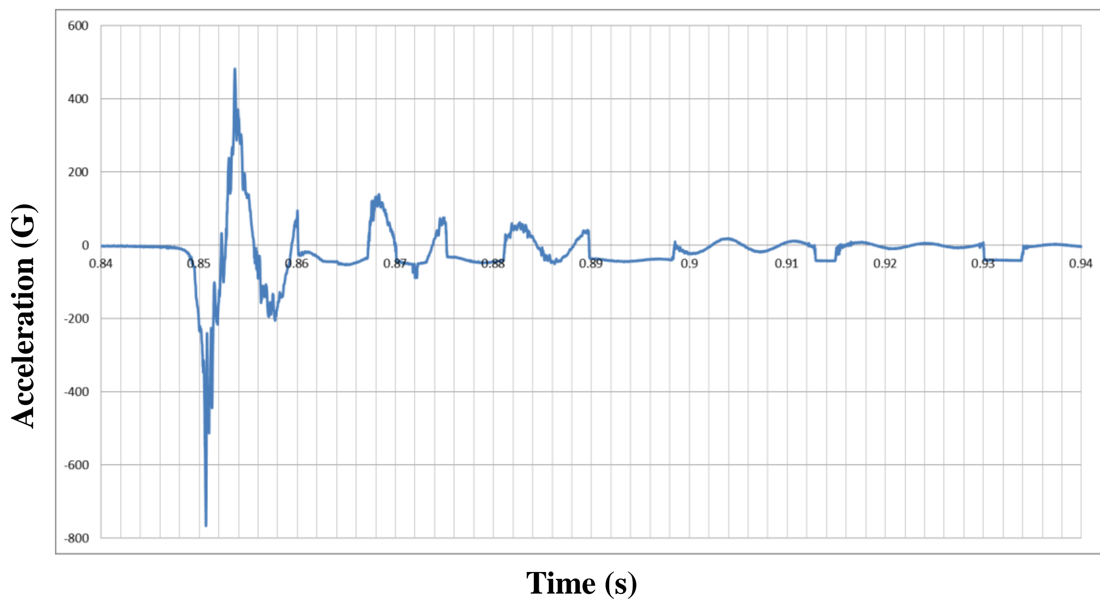


Fig A1.12: 600mm drop height acceleration data for bump interconnect sample

APPENDIX B

EXPERIMENTAL DROP TESTING STRAIN DATA

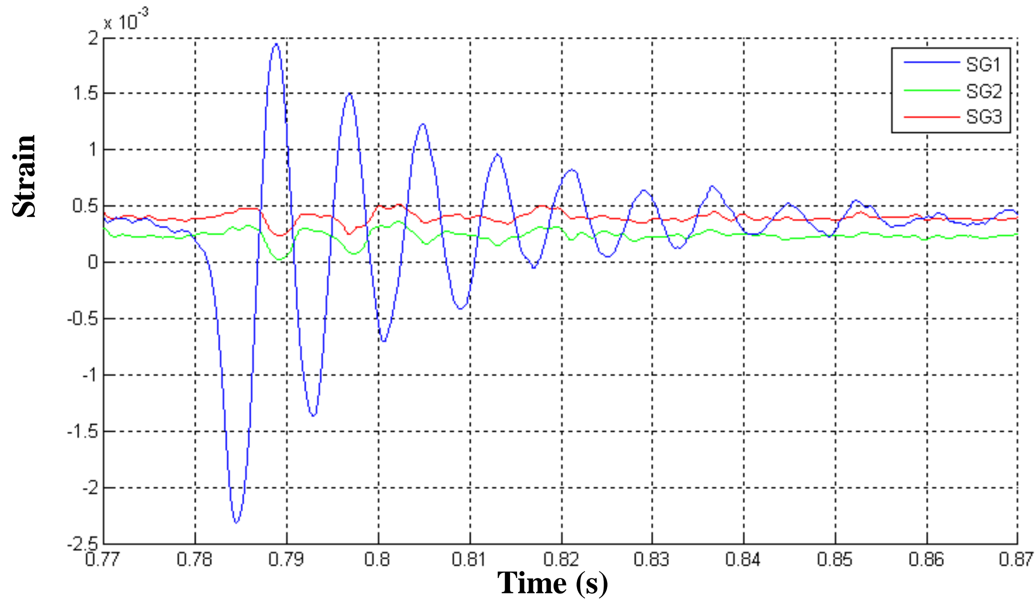


Fig A2.1: 100mm drop height strain data for three-arc interconnect sample

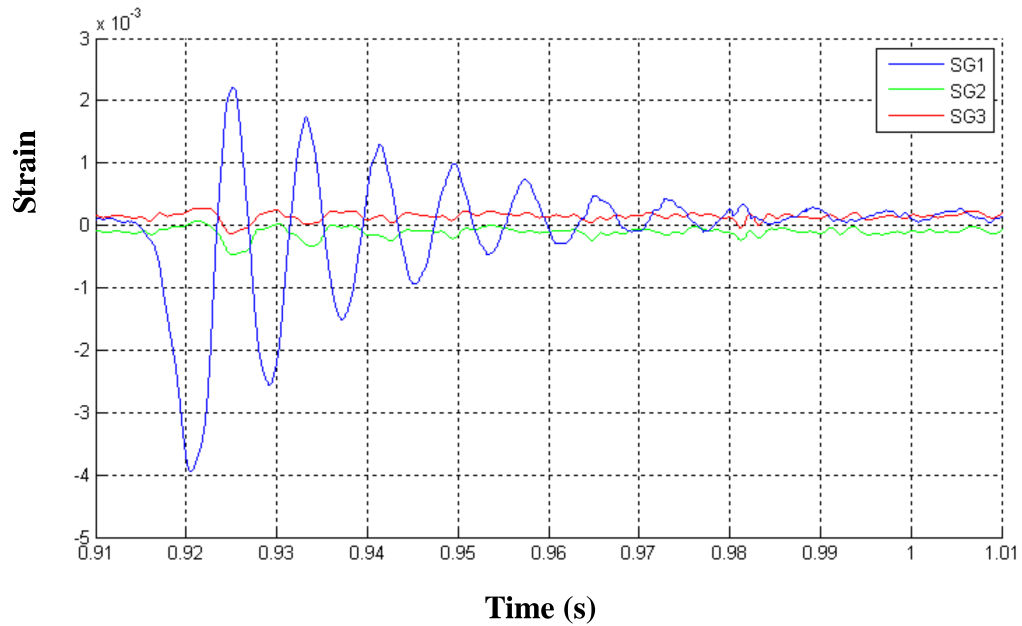


Fig A2.2: 200mm drop height strain data for three-arc interconnect sample

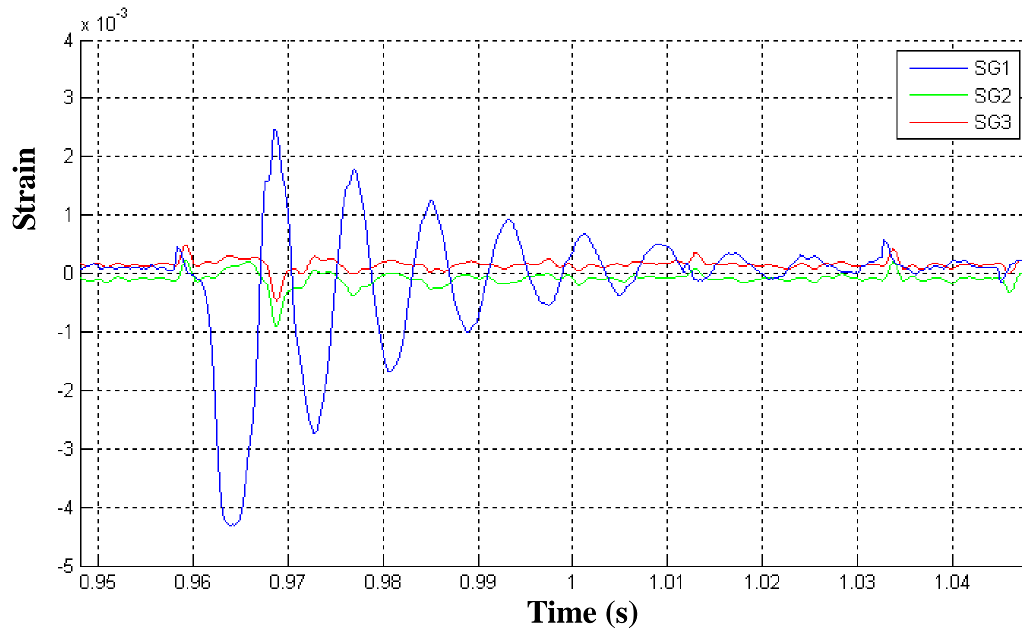


Fig A2.3: 300mm drop height strain data for three-arc interconnect sample

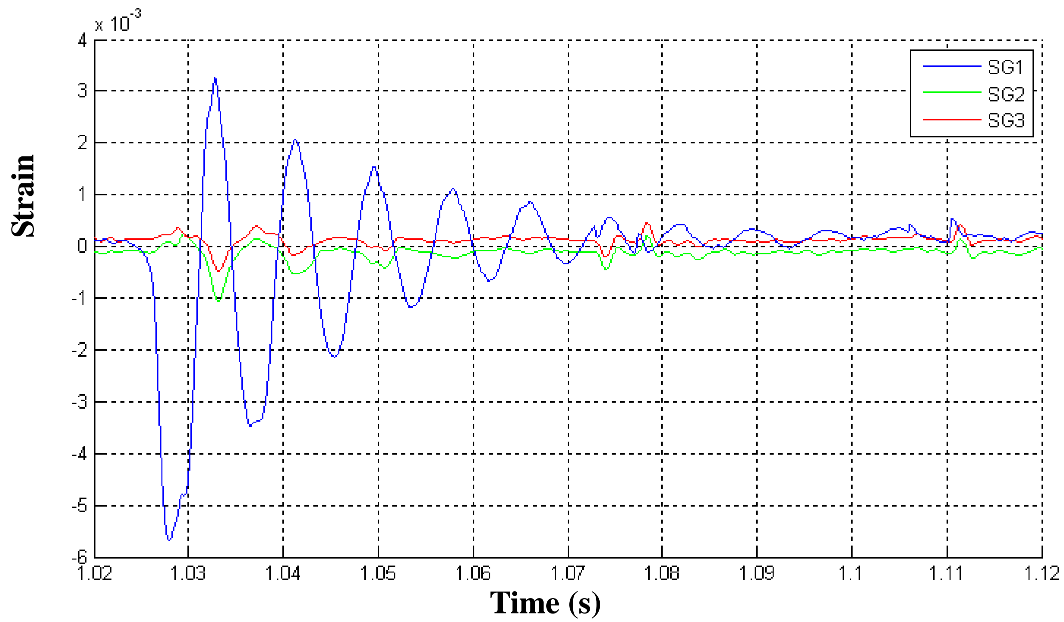


Fig A2.4: 400mm drop height strain data for three-arc interconnect sample

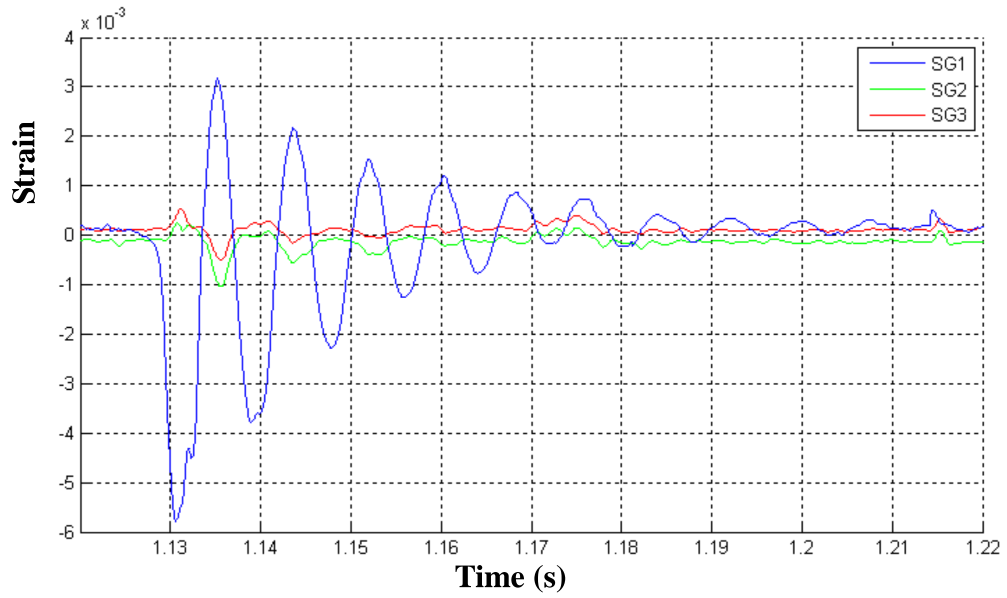


Fig A2.5: 500mm drop height strain data for three-arc interconnect sample

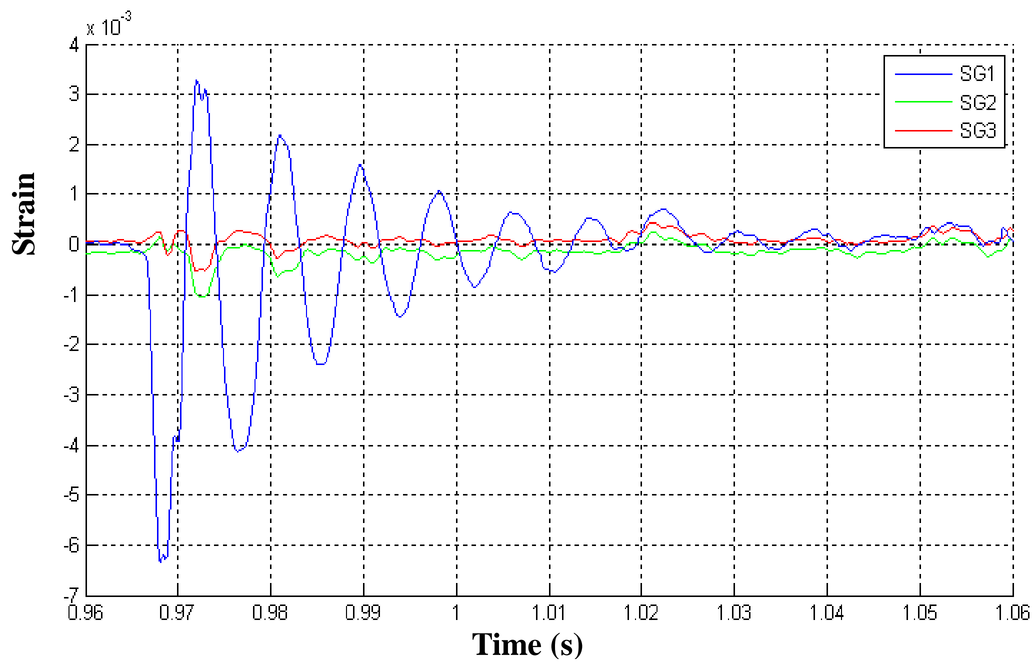


Fig A2.6: 600mm drop height strain data for three-arc interconnect sample

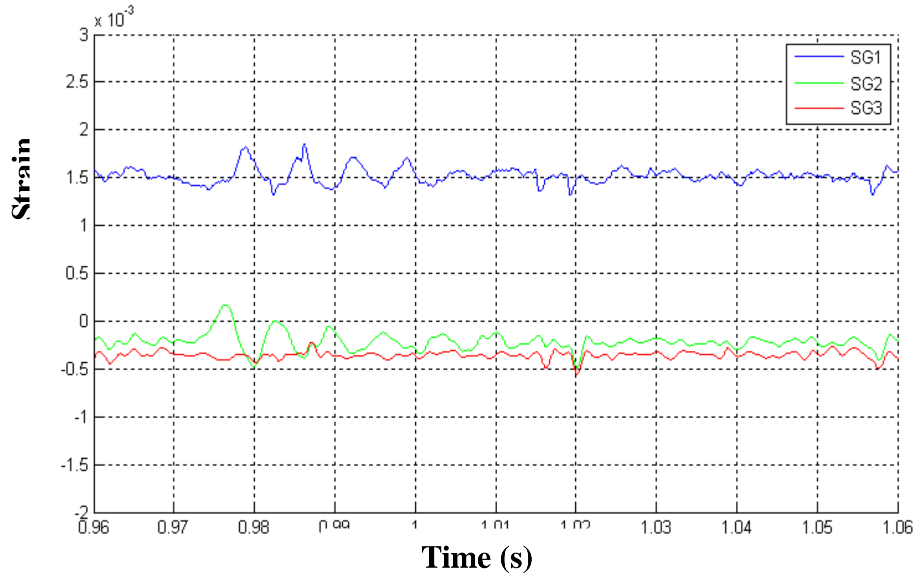


Fig A2.7: 100mm drop height strain data for bump interconnect sample

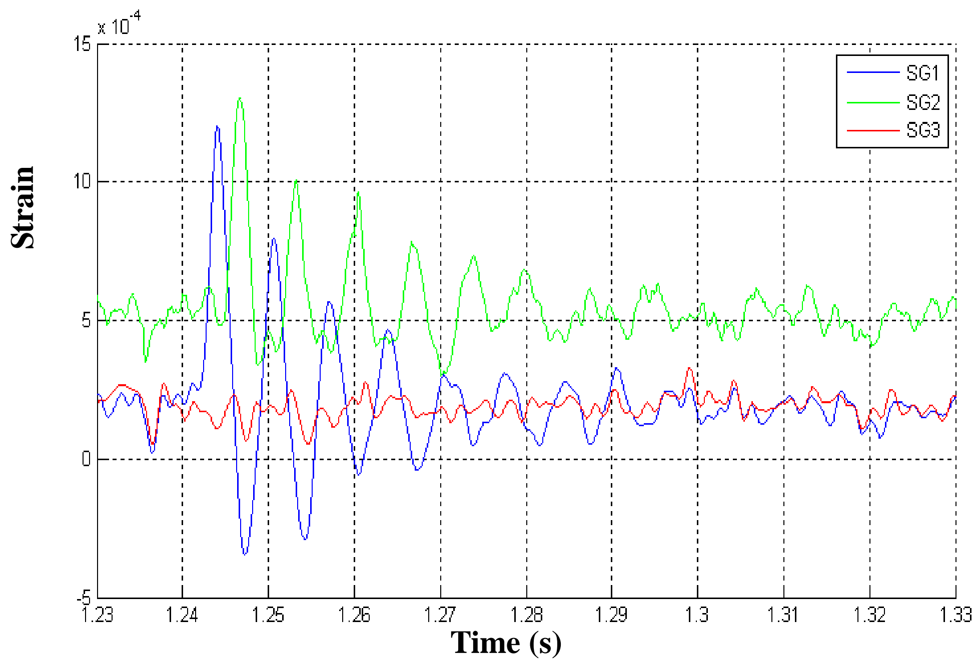


Fig A2.8: 200mm drop height strain data for bump interconnect sample

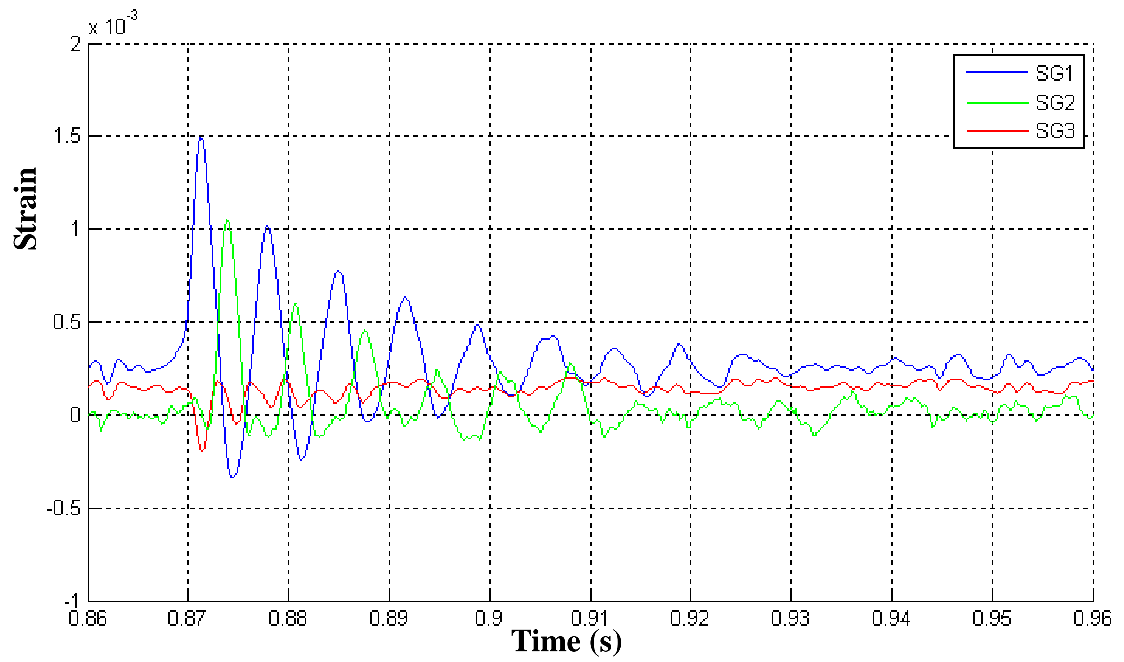


Fig A2.9: 300mm drop height strain data for bump interconnect sample

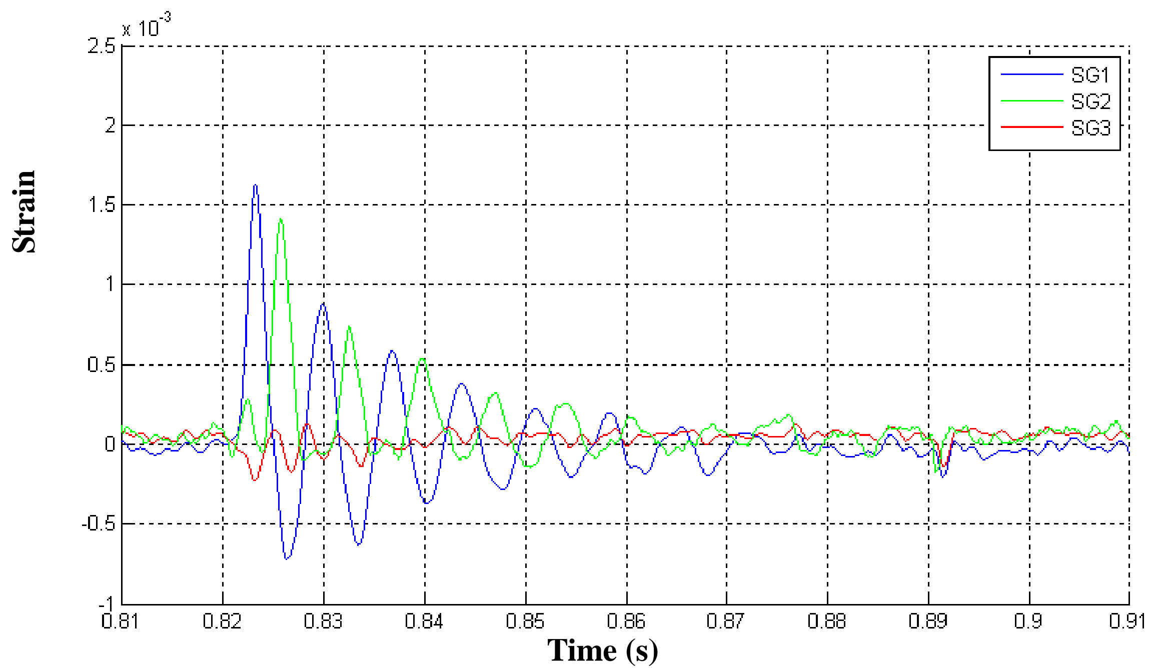


Fig A2.10: 400mm drop height strain data for bump interconnect sample

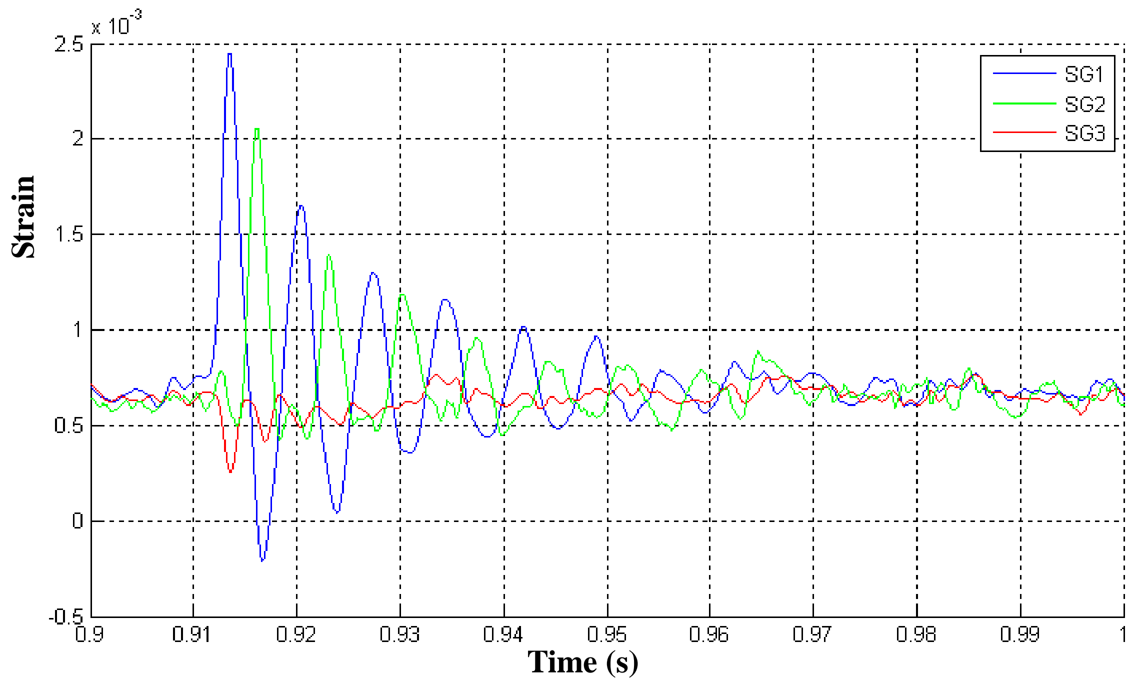


Fig A2.11: 500mm drop height strain data for bump interconnect sample

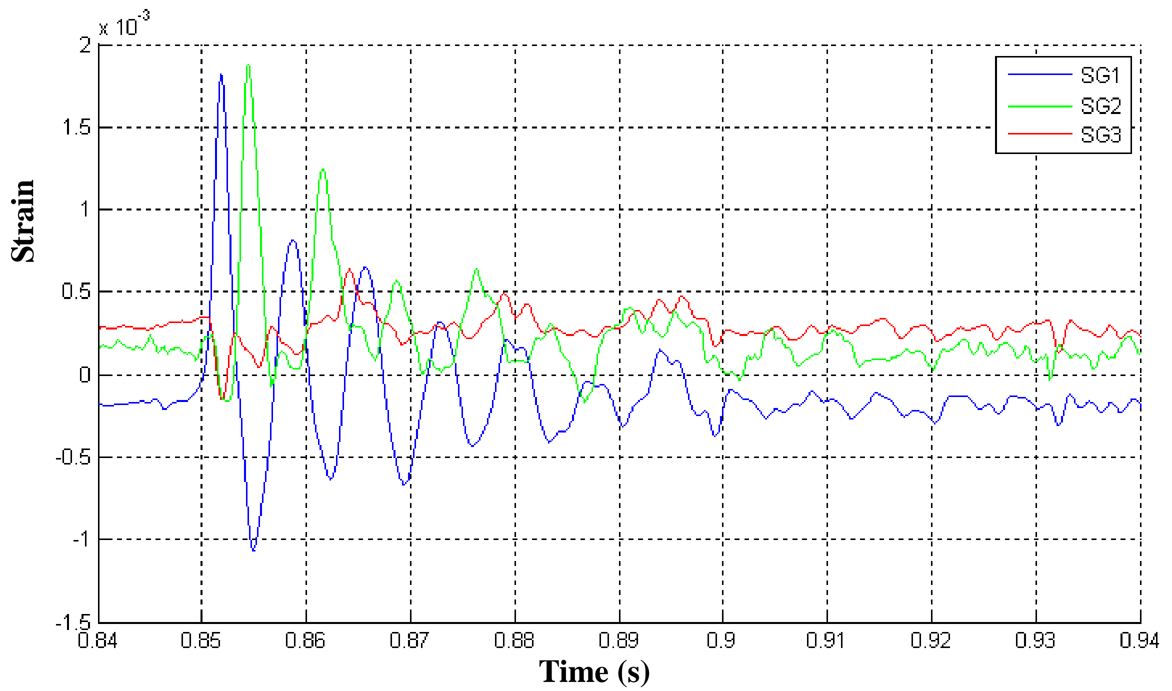


Fig A2.12: 600mm drop height strain data for bump interconnect sample

APPENDIX C

FINITE-ELEMENT DROP TEST SIMULATION STRAIN DATA

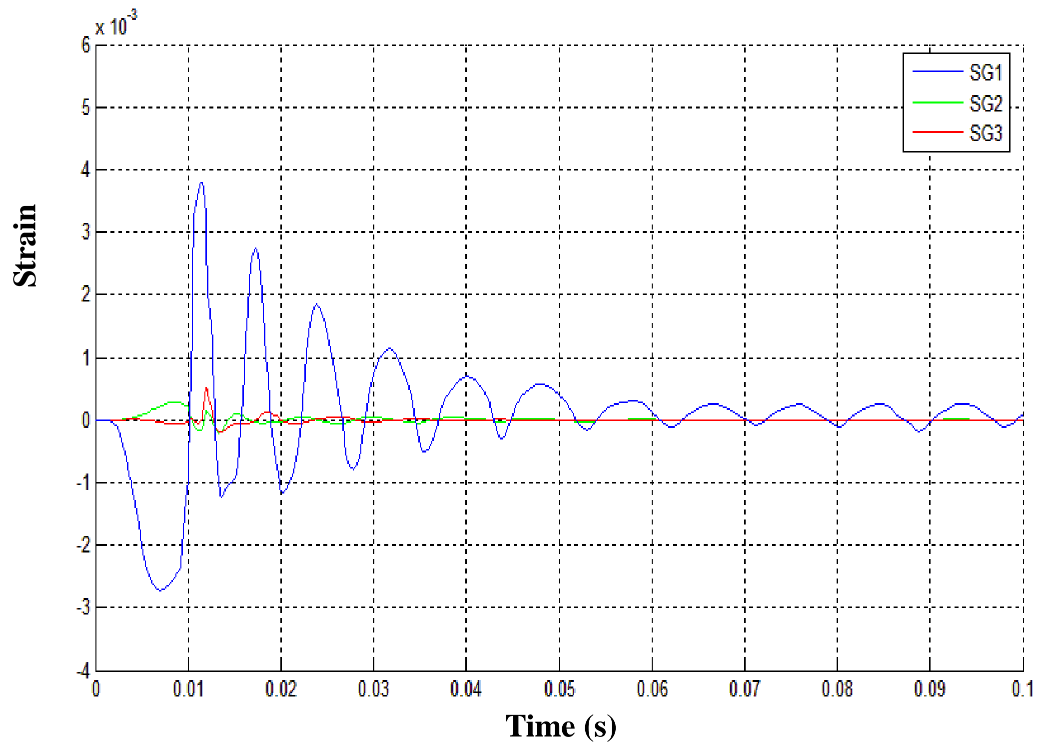


Fig A3.1: 100mm drop height simulation strain data for three-arc interconnect model

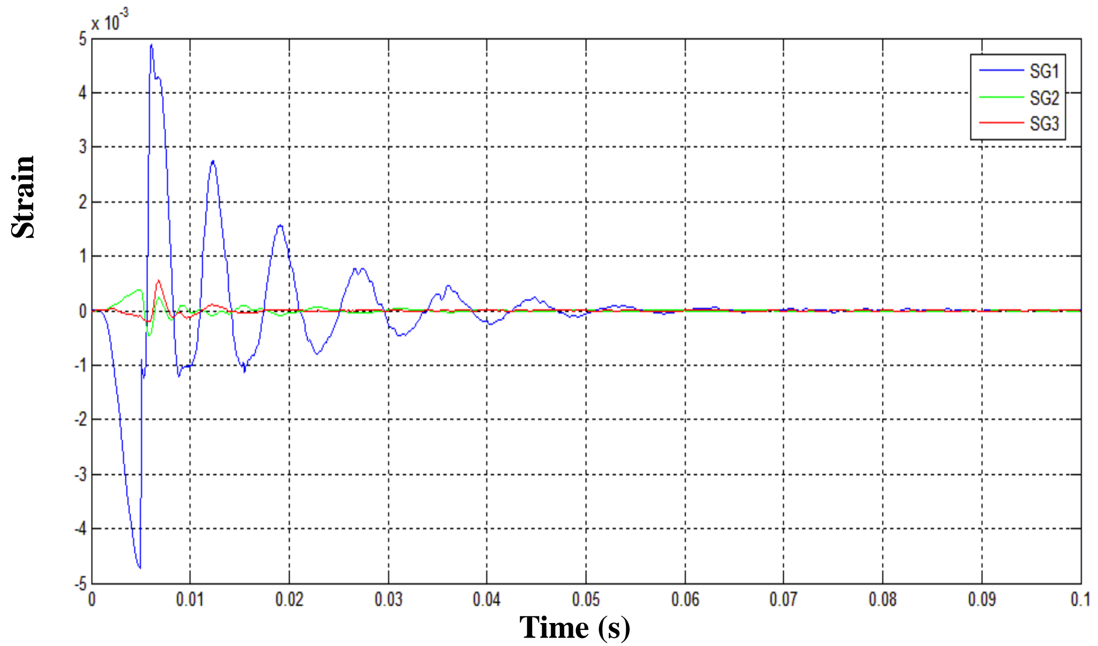
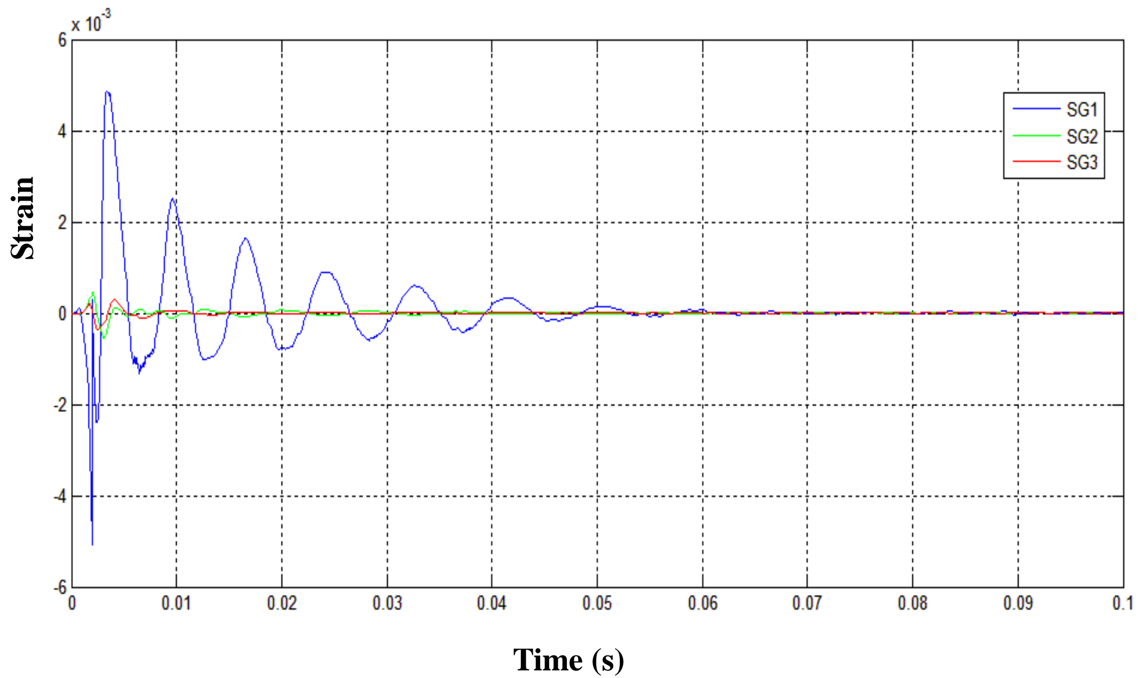


Fig A3.2: 300mm drop height simulation strain data for three-arc interconnect model



Time (s)

Fig A3.3: 500mm drop height simulation strain data for three-arc interconnect model

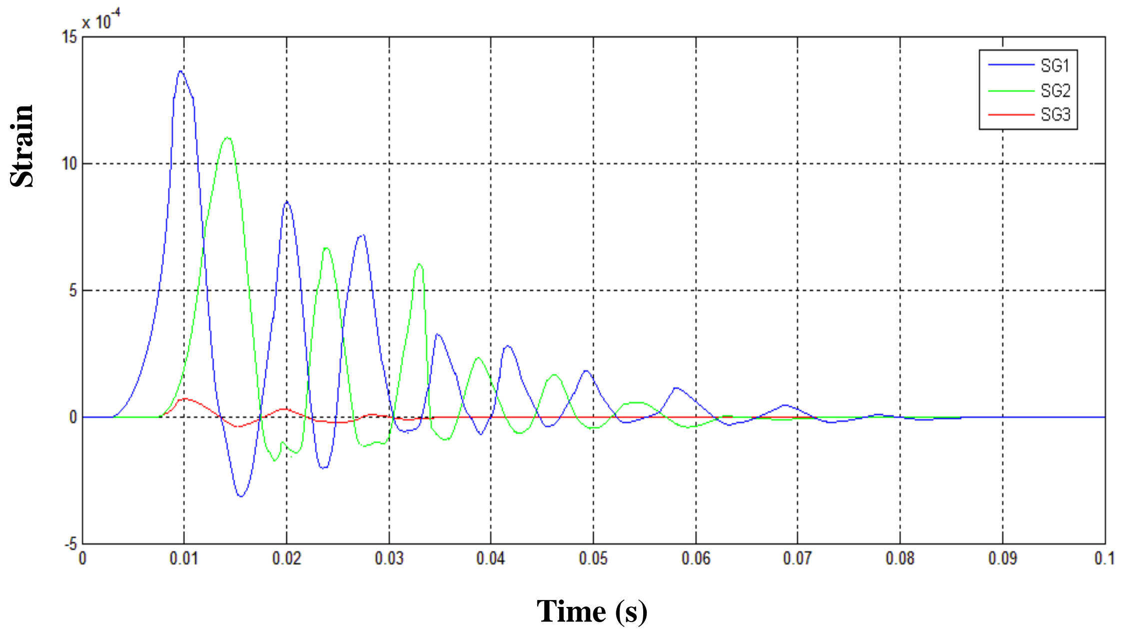


Fig A3.4: 200mm drop height simulation strain data for bump interconnect model

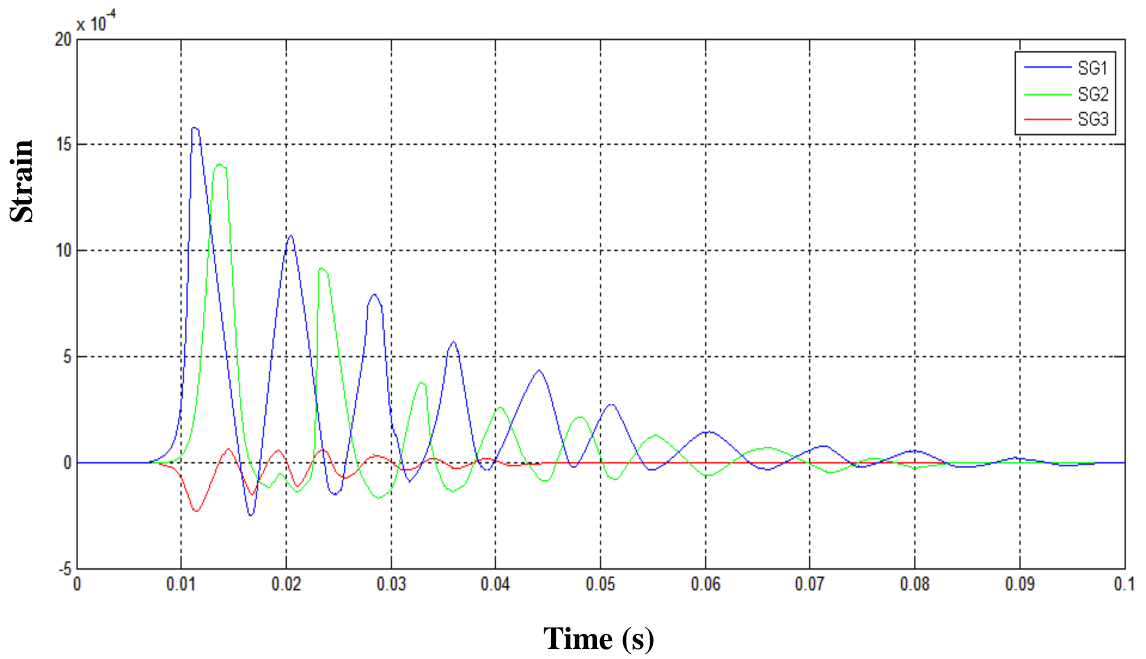


Fig A3.5: 300mm drop height simulation strain data for bump interconnect

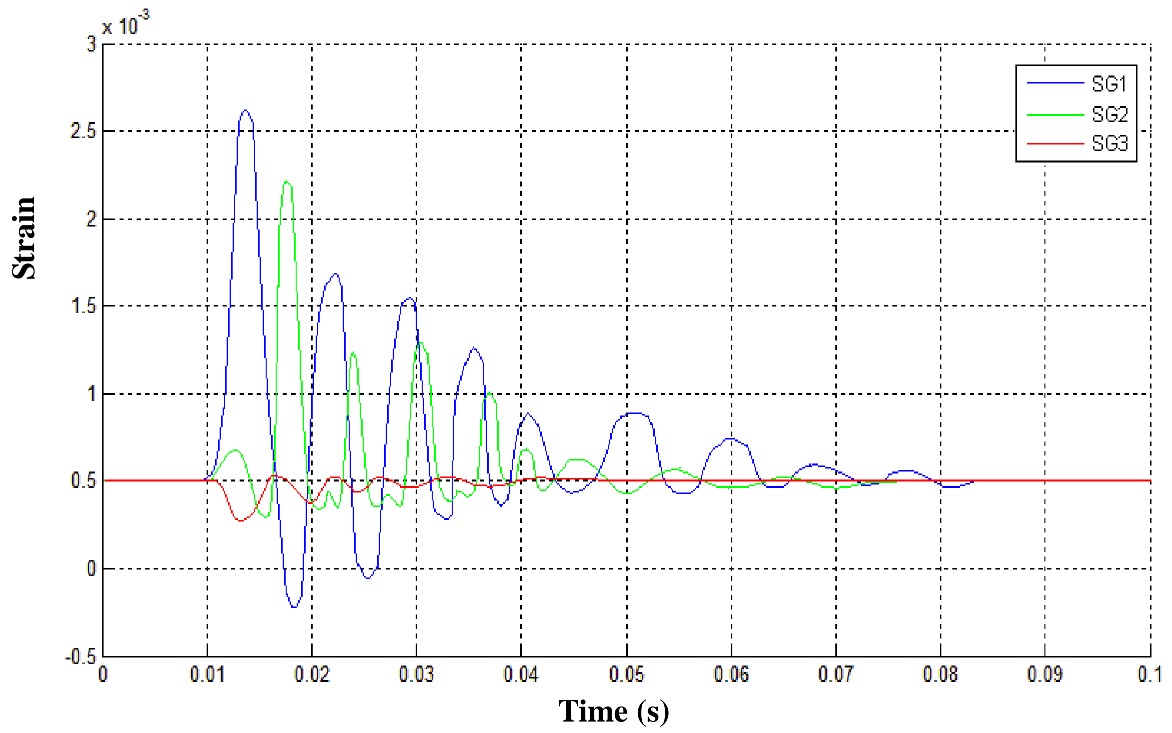


Fig A3.6: 500mm drop height simulation strain data for bump interconnect model

REFERENCES

ANSYS®, Inc. Theory Manual, Release 13.0, 2010

Bakir, M. S., B. Dang, R. Emery, G. Vandentop, P. A. Kohl, and J. D. Meindl. "Sea of Leads Compliant I/O Interconnect Process Integration for the Ultimate Enabling of Chips with Low-Interlayer Dielectrics." *Advanced Packaging, IEEE Transactions on* 28, no. 3 (2005): 488-494.

Bakir, M. S., A. L. Glebov, M. G. Lee, P. A. Kohl, and J. D. Meindl. "Mechanically Flexible Chip-to-Substrate Optical Interconnections Using Optical Pillars." *Advanced Packaging, IEEE Transactions on* 31, no. 1 (2008): 143-153.

Braunisch, H., Hwang Kyu-Pyung, and R. D. Emery. "Compliant Die-Package Interconnects at High Frequencies." In *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2, 1237-1243 Vol.2, 2004.

Chaoping, Yuan, K. L. Pan, Qiu Weiyang, and Liu Jing. "Board Level Drop Impact Reliability Analysis for Compliant Wafer Level Package through Modeling Approaches." In *Electronic Packaging Technology & High Density Packaging, 2009. ICEPT-HDP '09. International Conference on*, 398-402, 2009.

Chow, E. M., D. K. Fork, C. L. Chua, K. Van Schuylenbergh, and T. Hantschel. "Wafer-Level Packaging with Soldered Stress-Engineered Micro-Springs." *Advanced Packaging, IEEE Transactions on* 32, no. 2 (2009): 372-378.

Dudek, R., H. Walter, R. Doering, B. Michel, T. Meyer, J. Zapf, and H. Hedler. "Thermomechanical Design for Reliability of Wafer-level packages with Compliant Interconnects." In *Electronic Packaging Technology Conference, 2005. EPTC 2005. Proceedings of 7th*, 1, 7 pp., 2005.

Dudek, R., H. Walter, R. Doering, B. Michel, T. Meyer, J. Zapf, and H. Hedler. "Thermo-Mechanical Design of Resilient Contact Systems for Wafer Level Packaging." In *Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, 2006. EuroSime 2006. 7th International Conference on*, 1-7, 2006.

Fong Kuan, Ng, Lim Chwee Teck, E. Pek, Luan Jing-En, and Tee Tong Yan. "Study of Pcb Strains and Component Position under Board Level Drop Test." In *Electronic*

Packaging Technology Conference, 2005. EPTC 2005. Proceedings of 7th, 1, 7 pp., 2005.

Ginsberg, Jerry H. “Mechanical and Structural Vibrations.” John Wiley and Sons Inc., 2001.

Hun Shen, Ng, Tee Tong Yan, and Luan Jing-en. "Design for Standard Impact Pulses of Drop Tester Using Dynamic Simulation." In *Electronics Packaging Technology Conference, 2004. EPTC 2004. Proceedings of 6th*, 793-799, 2004.

Irving, S., and Y. Liu. "Free Drop Test Simulation for Portable IC Package by Implicit Transient Dynamics Fem." In *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 1, 1062-1066 Vol.1, 2004.

Ishihara, S., A. J. McEvily, T. Goshima, K. Kanekasu, and T. Nara. "On Fatigue Lifetimes and Fatigue Crack Growth Behavior of Bone Cement." *Journal of Materials Science: Materials in Medicine* 11, no. 10 (2000): 661-666.

JEDEC. JESD22-B111. "Board Level Drop Test Method of Components for Handheld Electronic Products ", 1-14, July 2003.

JEDEC. JESD22-B110a. "Sub-Assembly Mechanical Shock ", 1-14, November 2004.

Jiang, Zhou. "Analytical Analysis on the Effect of Time Duration of Acceleration Pulse to a JEDEC Board in Drop Test." In *Electronic Packaging Technology & High Density Packaging, 2008. ICEPT-HDP 2008. International Conference on*, 1-6, 2008.

Jing-en, Luan, and Tee Tong Yan. "Novel Board Level Drop Test Simulation Using Implicit Transient Analysis with Input-G Method." In *Electronics Packaging Technology Conference, 2004. EPTC 2004. Proceedings of 6th*, 671-677, 2004.

Jing-en, Luan, and Tee Tong Yan. "Analytical and Numerical Analysis of Impact Pulse Parameters on Consistency of Drop Impact Results." In *Electronics Packaging Technology Conference, 2004. EPTC 2004. Proceedings of 6th*, 664-670, 2004.

Jing-en, Luan, and Tee Tong Yan. "Effect of Impact Pulse Parameters on Consistency of Board Level Drop Test and Dynamic Responses." In *Electronic Components and Technology Conference, 2005. Proceedings. 55th*, 665-673 Vol. 1, 2005.

Jing-En, Luan, Tee Tong Yan, E. Pek, Lim Chwee Teck, Zhong Zhaowei, and Zhou Jiang. "Advanced Numerical and Experimental Techniques for Analysis of Dynamic Responses and Solder Joint Reliability During Drop Impact." *Components and Packaging Technologies, IEEE Transactions on* 29, no. 3 (2006): 449-456.

Johannessen, R., F. Oldervoll, H. Kristiansen, H. Tyldum, H. V. Nguyen, and K. Aasmundtveit. "Investigation of Compliant Interconnect for Ball Grid Array (BGA)." In *Microelectronics and Packaging Conference, 2009. EMPC 2009. European*, 1-6, 2009.

Kacker, K., and S. K. Sitaraman. "Design and Fabrication of FlexConnects: A Cost-Effective Implementation of Compliant Chip-to-Substrate Interconnects." *Components and Packaging Technologies, IEEE Transactions on* 31, no. 4 (2008): 816-823.

Kacker, K., T. Sokol, and S. K. Sitaraman. "FlexConnects: A Cost-Effective Implementation of Compliant Chip-to-Substrate Interconnects." In *Electronic Components and Technology Conference, 2007. ECTC '07. Proceedings. 57th*, 1678-1684, 2007.

Kailin, Pan, Zhou Bin, and Yan Yilin. "Simulating Analysis of Dynamic Responses for CSP under Board Level Drop Test." In *Electronic Packaging Technology, 2006. ICEPT '06. 7th International Conference on*, 1-5, 2006.

Kim Yong, Goh, Luan Jing-en, and Tee Tong Yan. "Drop Impact Life Prediction Model for Wafer Level Chip Scale Packages." In *Electronic Packaging Technology Conference, 2005. EPTC 2005. Proceedings of 7th*, 1, 8 pp., 2005.

Lall, P., D. Panchagade, D. Iyengar, S. Shantaram, J. Suhling, and H. Schrier. "High Speed Digital Image Correlation for Transient-Shock Reliability of Electronics." In *Electronic Components and Technology Conference, 2007. ECTC '07. Proceedings. 57th*, 924-939, 2007.

Lall, P., D. Iyengar, S. Shantaram, D. Panchagade, and J. Suhling. "Development of Survivability Envelopes for Snag Lead-free Packaging Architectures under Shock and Vibration." In *Thermal and Thermomechanical Phenomena in Electronic Systems, 2008. ITHERM 2008. 11th Intersociety Conference on*, 822-835, 2008.

Lall, P., D. R. Panchagade, D. Iyengar, S. Shantaram, and H. Schrier. "High Speed Digital Image Correlation for Transient-Shock Reliability of Electronics." *Components and Packaging Technologies, IEEE Transactions on* 32, no. 2 (2009): 378-395.

Lee, R. E., R. Okereke, and S. K. Sitaraman. "Multi-Path Fan-Shaped Compliant Off-Chip Interconnects." In *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2141-2145, 2011.

Liao, E. B., A. A. O. Tay, S. S. T. Ang, H. H. Feng, R. Nagarajan, V. Kripesh, R. Kumar, and M. K. Iyer. "A MEMS-Based Compliant Interconnect for Ultra-Fine-Pitch

Wafer Level Packaging." In *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 5 pp., 2006.

Liao, E. B., A. A. O. Tay, S. S. T. Ang, H. H. Feng, R. Nagarajan, V. Kripesh, R. Kumar, and G. Q. Lo. "Planar Micro spring; a Novel Compliant Chip-to-Package Interconnect for Wafer-Level Packaging." *Advanced Packaging, IEEE Transactions on* 32, no. 2 (2009): 379-389.

Lo, G., and S. K. Sitaraman. "G-Helix: Lithography-Based Wafer-Level Compliant Chip-to-Substrate Interconnects." In *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 1, 320-325 Vol.1, 2004.

Lunyu, Ma, Zhu Qi, T. Hantschel, D. K. Fork, and S. K. Sitaraman. "J-Springs - Innovative Compliant Interconnects for Next-Generation Packaging." In *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, 1359-1365, 2002.

Lunyu, Ma, Zhu Qi, S. K. Sitaraman, C. Chua, and D. K. Fork. "Compliant Cantilevered Spring Interconnects for Flip-Chip Packaging." In *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 761-766, 2001.

Murray, William, Miller, William R.. “The Bonded Electrical Resistance Strain Gage: An Introduction.” Oxford University Press, pp. 187-190, 1992.

Muthukumar, S., C. D. Hill, S. Ford, W. Worwag, T. Dambrauskas, P. C. Challela, T. S. Dory, N. M. Patel, E. L. Ramsay, and D. S. Chau. "High-Density Compliant Die-Package Interconnects." In *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 6 pp., 2006.

Novitsky, J., and D. Pedersen. "Formfactor Introduces an Integrated Process for Wafer-Level Packaging, Burn-in Test, and Module Level Assembly." In *Advanced Packaging Materials: Processes, Properties and Interfaces, 1999. Proceedings. International Symposium on*, 226-231, 1999.

Ostrowicki, G. T., N. T. Fritz, R. I. Okereke, P. A. Kohl, and S. K. Sitaraman. "Domed and Released Thin-Film Construct—an Approach for Material Characterization and Compliant Interconnects." *Device and Materials Reliability, IEEE Transactions on* 12, no. 1 (2012): 15-23.

Seungbae, Park, Yu Da, A. Al-Yafawi, Kwak Jae, and J. Lee. "Effect of Damping and Air Cushion on Dynamic Responses of Pcb under Product Level Free Drop Impact." In *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 1256-1262, 2009.

Qi, Zhu, Ma Lunyu, and S. K. Sitaraman. "Beta;-Helix: A Lithography-Based Compliant Off-Chip Interconnect." *Components and Packaging Technologies, IEEE Transactions on* 26, no. 3 (2003): 582-590.

Renshape™ SL 7510, "asolid.com/info/SL7510_7000.pdf" (Accessed March 9, 2012)

Sitaraman, S. K. and Kacker, K., "Mechanically Compliant I/O Interconnects and Packaging," Chapter 3, *Integrated Interconnect Technologies for 3D Nanoelectronic Systems,* Ed. Muhannad S. Bakir and James D. Meindl, Artech House, 2009.

Shubin, I., A. Chow, J. Cunningham, M. Giere, N. Nettleton, N. Pinckney, J. Shi, J. Simons, R. Hopkins, J. Mitchell, D. Douglas, E. M. Chow, D. DeBruyker, B. Cheng, and G. Anderson. "A Package Demonstration with Solder Free Compliant Flexible Interconnects." In *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 1429-1435, 2010.

Stereolithography (image), www.custompart.net (Accessed June 12, 2012)

Suhir, E. "Nonlinear Dynamic Response of a Flexible Printed Circuit Board to a Shock Load Applied to Its Support Contour." In *Electronic Components and Technology Conference, 1991. Proceedings., 41st*, 388-399, 1991.

Suhir, E. "Analytical Modeling of the Dynamic Response of a Printed Circuit Board (Pcb) to an Impact Load." In *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on*, 480-488, 2010.

Su-Tsai, Lu, Lin Yu-Min, Chuang Chun-Chih, Chen Tai-Hong, and Chen Wen-Hwa. "Development of a Novel Compliant-Bump Structure for ACA-Bonded Chip-on-Flex (COF) Interconnects with Ultra-Fine Pitch." *Components, Packaging and Manufacturing Technology, IEEE Transactions on* 1, no. 1 (2011): 33-42.

Tong Yan, Tee, Ng Hun Shen, Lim Chwee Teck, E. Pek, and Zhong Zhaowei. "Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications." In *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*, 121-129, 2003.

Tong Yan, Tee, Luan Jing-en, and Ng Hun Shen. "Development and Application of Innovational Drop Impact Modeling Techniques." In *Electronic Components and Technology Conference, 2005. Proceedings. 55th*, 504-512 Vol. 1, 2005.

Tong Yan, Tee, Luan Jing-en, E. Pek, Lim Chwee Teck, and Zhong Zhaowei. "Novel Numerical and Experimental Analysis of Dynamic Responses under Board Level Drop Test." In *Thermal and Mechanical Simulation and Experiments in*

Microelectronics and Microsystems, 2004. EuroSimE 2004. Proceedings of the 5th International Conference on, 133-140, 2004.

Tong Yan, Tee, Luan Jing-en, E. Pek, Lim Chwee Teck, and Zhong Zhaowei. "Advanced Experimental and Simulation Techniques for Analysis of Dynamic Responses During Drop Impact." In *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 1, 1088-1094 Vol.1, 2004.

Tummala R. Rao. “Fundamentals of Microsystems Packaging.” McGraw Hill, 2001.

Woo, M. S. S., and E. H. Wong. "Analytical Solution of the Dynamic Response of Printed Circuit Board to Support Excitation." In *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 386-390, 2007.

Zhu, Q. (2003). “Design, Fabrication and Thermo-mechanical Reliability of compliant interconnects for High I/O density Packaging ", PhD Thesis, Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, Georgia.