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Fault Protection In DC Distribution Systems Via Coordinated Control of Power Supply Converters and Bus Tie Switches

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FAULT PROTECTION IN DC DISTRIBUTION SYSTEMS VIA COORDINATED CONTROL OF POWER SUPPLY CONVERTERS AND BUS TIE SWITCHES

by

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DEDICATION

To my lovely wife, Cristina

&

To my dear parents, brothers, and friends

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ABSTRACT

A new fault protection method responds to the current needs of emerging dc power distribution systems by coordinating electronic power converters and mechanical contactors to rapidly isolate short circuit faults while maintaining continuity of power to loads.

This work is important because the increasing performance, higher efficiency, and decreasing cost of electronic power converters have spurred a rediscovery and proliferation of dc power distribution systems. Although dc distribution offers advantages such as higher transmission efficiency, higher power density, higher reliability, and ease of interfacing asynchronous sources, enthusiasm for adopting dc technologies suffers from widespread concern over the means to protect dc distribution systems against short-circuit faults.

The developed fault protection method rapidly limits the fault current, de-energizes the main distribution bus, reconfigures the bus via mechanical contactors, and re-energizes the system. The entire process can be accomplished fast enough to comply with the requirements of CBEMA and IEEE standards on power quality.

A fast and reliable fault detection method has been developed in order to coordinates power converters and contactors. With this method the source power converters independently enter into current-limiting mode as soon as they recognize a fault condition. The bus segmentizing contactors autonomously decide whether to open or not

based on their local interpretation of time-to-trip curves as functions of apparent equivalent circuit resistance. This method allows converter and contactors to coordinate to provide fault protection for dc distribution systems independently on communication failures.

Simulation and experimental results show that fault current can be limited within few milliseconds, faults can be isolated within 20 ms and that the system can be re-energized within 100 ms. Moreover, this work provides system design considerations and limitations on components and system parameters.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AC.....Alternating Current

ADC.....Analog to Digital Converter

DSP..... Digital Signal Processor

DC.....Direct Current

ESRDC..... Electric Ship Research and Development Consortium

ETO.....Emitter Turn Off thyristor

IGBT..... Insulated Gate Bipolar Transistor

IGCT.....Integrated Gate Commutated Thyristor

MOSFET..... Metal Oxide semiconductor Field Effect Transistor

MOV.....Metal Oxide Varistor

MVDC..... Medium Voltage Direct Current

PWM.....Pulse Width Modulation

SSCB..... Solid State Circuit Breaker

VSC.....Voltage Source Converter

CHAPTER 1

INTRODUCTION

The objective of developing a fault protection method answers to the urgency of new effective fault protections that are suitable for DC distribution system for a number of emerging applications. The contributions of this research are twofold. On one hand, we provide a fast isolation of short-circuit faults and limitation of fault currents. On the other hand, coordination of the devices that contribute to the protection of the system is guaranteed without relying on communication.

1.1 RESEARCH OBJECTIVE

The main objective of this research was to develop a method for protecting DC distribution systems against short circuit faults. We achieved this by coordinating the action of controllable power supply converters with the action of bus tie switches and mechanical contactors.

This objective involves the design of an appropriate detection algorithm that permit both a reliable detection of faults and coordination between the different elements involved in the protection of the system. The protection method was implemented in simulation at the medium voltage and megawatt level, and also proved with a scaled low voltage hardware test bench.

Finally, this work provides design guidelines for implementing the protection scheme in a variety of power systems, and the boundary of operation and applicability of the developed method.

1.2 CONTRIBUTIONS OF THIS RESEARCH

The contribution of this research can be divided in two aspects. The first aspect focuses on the development of a fault protection method for DC distribution systems that can substitute the use of circuit breakers. This contribution can be summarized as:

- Fast isolation of short-circuit faults. The isolation of the faulted section of the system can be accomplished faster or at a comparable speed compared to circuit breakers
- Low amplitude of the fault currents. Fault currents can be actively limited by controllable power converters and thus fault currents result to be tens to hundreds time smaller that the fault perspective currents (fault current without active limitation)
- Low normal operation losses. Losses in normal operation are comparable to the losses caused by the presence of circuit breakers. In fact, the devices used for reconfiguration of the system are mechanical contactors and not semiconductor-based switches.
- Ride-through capability for healthy parts of the system. Healthy load do not suffer for power interruptions.
- High power quality according to IEEE standards. Fault currents and voltage sags can be contained within the tolerance limits for equipment manufactured according

to the standard IEEE 1709 – Recommended Practice for 1kV to 35kV Medium Voltage DC Power System on Ship [40].

The second aspect focuses on the development of a detection method for short-circuit faults in multi-terminal dc systems powered by current and power limited sources. This method provides the following advantages:

- Fast and reliable identification of short-circuit fault conditions against normal operation transients.
- Coordination between feeding power converters, bus tie switches, and contactors. This coordination permits the isolation of the smallest section of the system after a fault.
- Fault coordination without relying on the communication between the elements involved in fault protection.
- Reliability of the detection method depending on the parameters of the systems and the measurement accuracy of the detection devices.
- Boundaries of application of the fault detection method.

1.3 PROJECT SIGNIFICANCE

The US navy is interested in renewing the combatant vessels power distribution system in order to meet the constantly increasing power demand on ship and the conversion of all the loads on board into electrical loads [1]. For this reasons, the Electric Ship Research and Development Consortium (ESRDC) is exploring different baseline models for ship design including a medium voltage direct current (MVDC) power distribution system [2]. Although dc distribution system provides great advantages in

terms of efficiency, reliability, and flexibility, enthusiasm for adopting dc technologies suffers from widespread concern over the means to protect dc distribution systems against short-circuit faults, ground faults, and open-circuit faults, especially at the medium voltage level [3]. In fact, traditional fault protection schemes based on circuit breakers are not applicable for MVDC distribution systems. Thus, our proposal to develop a method for detecting faults, protect the system from damage, and yet guarantee ride through capability for the healthy sections of the system is of prime importance.

In addition to the benefits of introducing a solution that enables the development of advanced shipboard electrical power architectures, the work presented here answer to the need for a more efficient and flexible distribution system for multiple emerging industrial applications. In fact, terrestrial microgrids with high prevalence of renewable power sources, data and communication centers, and other increasingly-common industrial applications that have no inherent 50/60 Hz ac nature are calling for distribution systems that can provide high availability, efficiency, and flexibility. Even in this case, a dc distribution system is a great candidate once a reliable method for fault protection eliminates the safety concerns of dc systems.

1.2.1 DC distribution systems for ships

The increasing performance, higher efficiency, and decreasing cost of electronic power converters have spurred a rediscovery and proliferation of dc power distribution systems. These are especially of interest in dc zonal power systems for ships, in terrestrial microgrids, in data and telecom centers, in renewable energy systems, and in other

increasingly-common industrial applications that have no inherent 50/60 Hz ac nature [4]-[9].

A multi-zonal MVDC architecture has been identified by the US Navy as one of the possible architectures for the shipboard power distribution. The zonal electrical system architecture eliminates all switchboard feeder cables transitioning watertight bulkheads, except the port and starboard cableways [10], [11]. The ever-increasing high-power loads on ships, which need highly reliable and very high-quality power supply, made conventional AC systems very hard to maintain.

The system envisioned by the Navy is illustrated in Figure 1.1. Two or more generators supply power to the DC distribution bus through power electronic converters, which rectify AC to DC and regulate the DC bus voltage. Lower voltage buses are served through dc-dc converters that isolate the loads in the zone from the rest of the system, and thus, any fault and disturbance within a zone can be confined within that zone. The DC bus also simplifies the cabling for power distribution, as more power can be transferred on a cable with DC than AC [4].

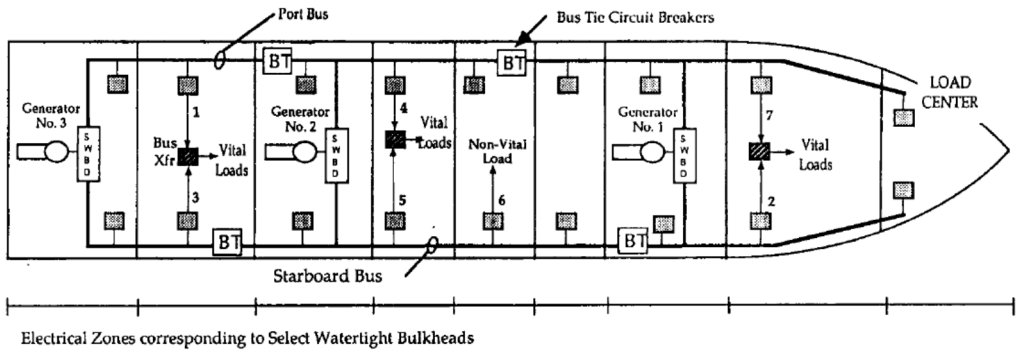

Figure 1.1 Zonal electrical distribution system onboard a typical surface combatant [8].

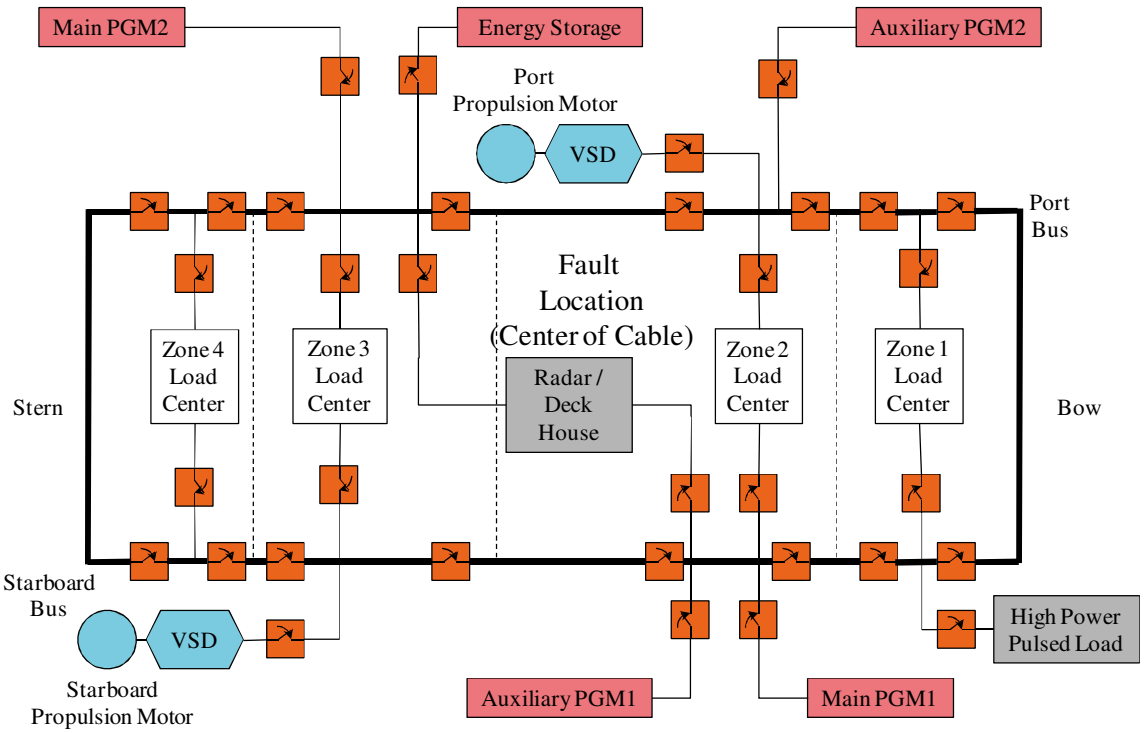

Figure 1.2 ESRDC Baseline System Model for MVDC shipboard distribution system

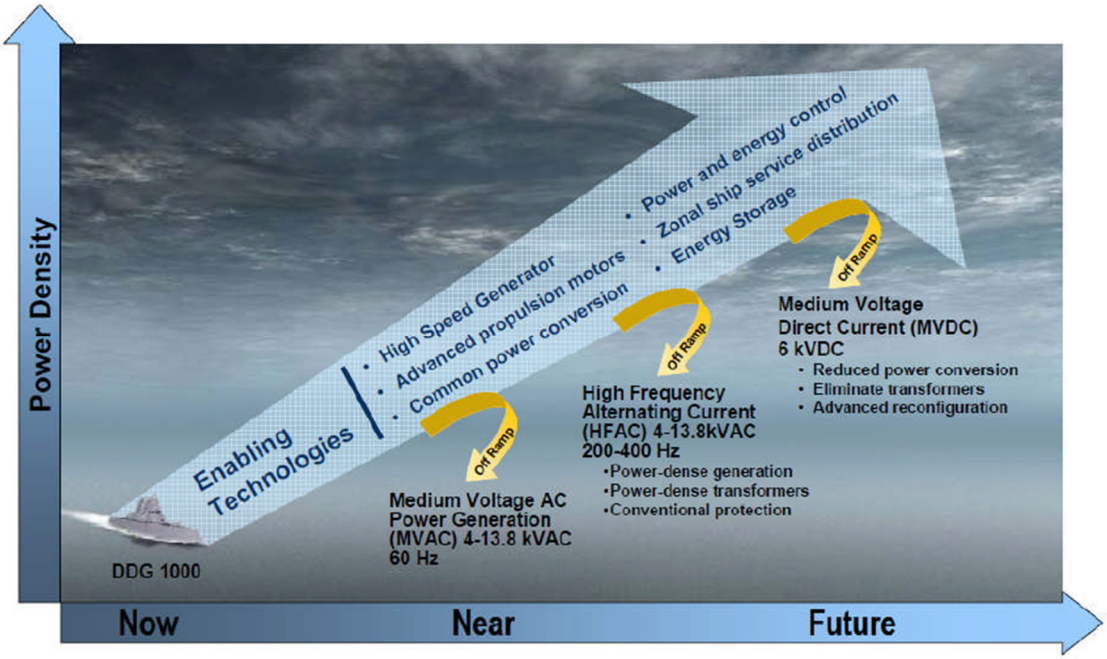

Figure 1.3 Next Generation Integrated Power System Technology Development Roadmap 2007 [10].

Additional benefits provided by MVDC system architecture include enhancement of ship productivity, flexibility in connecting and disconnecting multiple power sources, and ease of future ship modernization.

Figure 1.2 illustrates the ESRDC Baseline System Model for MVDC shipboard distribution system and Figure 1.3 shows the direction that the Navy is pursuing for the next generation destroyers [10].

1.2.2 DC distribution systems for terrestrial microgrids

DC distribution systems are also important in terrestrial microgrids with high prevalence of renewable power sources and load with an inherent dc nature. Even in this case, sources and loads can be easily interfaced with a DC bus through controllable power converters. This can provide extreme flexibility, higher efficiency, and intelligent power management for a best use of these emerging power systems [12]-[14]. An example of renewable microgrid is shown in Figure 1.4.

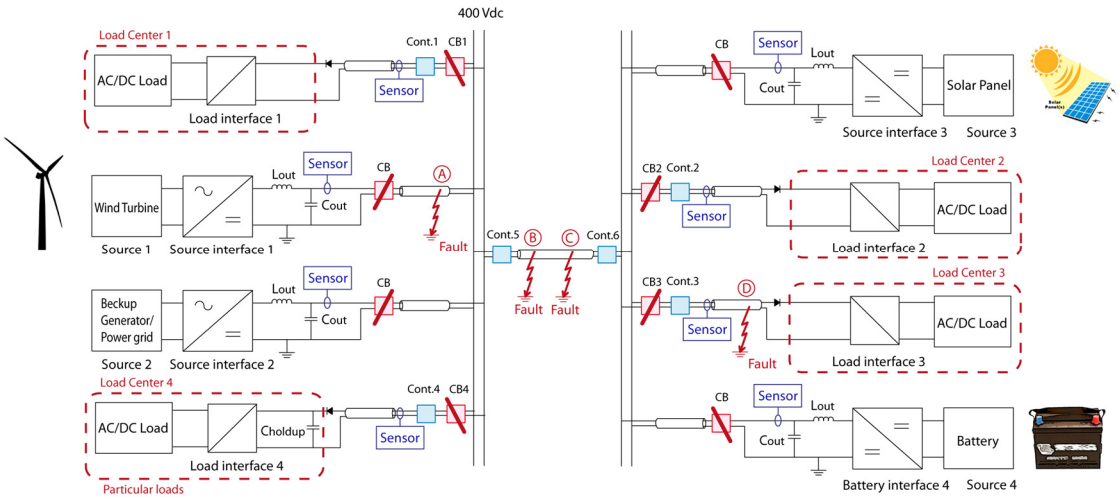

Figure 1.4 Structure of a notional dc microgrid, showing location of circuit protection elements, circuit breakers (CB) and contactors (Cont.), and representative locations of possible faults

The sources in a microgrid are usually small (< 1 MW) compared to terrestrial national wide distribution grids and often use renewable energy. Example of such sources are microturbines, fuel cells, photovoltaic, hydro plants, and wind turbines. Batteries, super capacitors, and flywheels can be used as energy storage. These types of sources and energy storage devices produce either DC voltage or AC voltage with different amplitude and frequency than the grid, and therefore need a power electronic converter to interface to a distribution bus and the grid [19]. When the microgrid is operated in island mode, the sources must regulate the voltage and frequency. In a DC microgrid asynchronous sources can be connected without the need of synchronization providing higher flexibility and higher overall efficiency [12].

Datacenters provide management for various types of server applications, such as for web hosting, internet, and telecommunication. As the development of computing technologies progresses, the size of servers is becoming smaller but their capacity increases. This leads to an increase of power density in data centers. One way to improve the efficiency and reliability of datacenters is to use a DC distribution system. The reason is that sources, energy storage devices, and loads are connected to the grid through power electronic interfaces: DC/AC converters and AC/DC/AC converters. By using a dc distribution system, one converter step can be eliminated, and energy storage devices can be directly connected to the distribution bus [19]. On top of this, in a dc system sources can connect to the distribution bus without the need of synchronization as in an AC grid. This is a great advantage for grids that have multiple sources that constantly share power depending on atmospheric and economic conditions.

In conclusion, the introduction of DC microgrid for renewable grid, datacenters, and many other industrial applications provides higher efficiency, reliability and flexibility compared to AC systems. In the next sections, the challenges related to fault detection and protection in DC distribution systems and the importance of finding a solution is explained in details.

1.2.3 Fault protection in DC distribution systems

DC systems for power distribution introduce great opportunities and challenges for power systems designers. Although distribution of power in dc form, rather than ac, offers multiple advantages such as higher transmission efficiency, higher reliability, and ease of interfacing asynchronous sources, enthusiasm for adopting dc technologies suffers from widespread concern over the means to protect dc distribution systems against short-circuit faults, ground faults, and open-circuit faults, especially for multi-terminal dc lines and multisource distribution systems.

Traditionally, arcing-type mechanical circuit breakers are the most common form of protection for any power system. The success of mechanical circuit breakers is largely attributable to the fact that alternating currents naturally cross zero at every half-period, thereby creating conditions for self-extinction of arcs between the parting contacts. In a dc system, however, there are no natural zero crossings so arc recovery demands that currents be forced to zero by additional means. Within limited voltage and current ranges, dc circuit breakers can be made functional by incorporating special structures, such as arc chutes, to dissipate and cool the arc sufficiently so that the arc voltage eventually exceeds the system voltage, forcing the current to zero. But this approach requires larger and more

expensive devices, and is ineffective at higher voltages. Moreover, in dc systems, fault currents are likely to be limited by the current limiting action of power converters; this can impede the functionality of magnetic arc-blowing devices [15]. As a consequence the fault current continues to flow, perhaps with destructive arc erosion effects at the fault location, system-wide collapse of the bus voltage, and loss of power to otherwise unfaulted parts of the system. Alternatively, semiconductor devices can be integrated into mechanical circuit breakers either as part of an external counter-pulse network to generate an artificial current zero, or as an alternative arc-less quenching path for the fault current. Many alternatives of this kind have been presented, but all of them imply the introduction of additional devices that have to be protected and monitored [16]-[19]. A third approach is to directly control the converters that interface sources and loads to the grid [20].

In case of a dc distribution system, in which the sources are interfaced to the distribution bus through electronic power converters, the energy and current that feed the faults can be limited. In fact, converters with current limitation mode can supply a first form of fault protection by limiting the current emission in case of overload or a faulted condition.

In conclusion, the proposal of an innovative method for fault protection in MVDC distribution systems answers to the unsolved problem of fault protection in dc distribution systems that is compromising reliability and safety of these power systems.

1.2.4 Fault detection in multi-terminal dc distribution systems

Electric Ship Research and Development Consortium (ESRDC) is proposing a power distribution system for ships oriented to systems with a variety of power sources, including renewable sources, and energy storage systems, connected to the distribution bus through controllable electronic power converters. This solution represents a big change in the management of power distribution and creates new unexplored challenges, particularly related to protection and control [21], [22]. In fact, on one hand multi-terminal dc distribution systems allow short circuit faults to be fed from multiple sources or storage elements, on the other hand sources interfaced by means of controllable converters are able to limit the fault current when compared to the case of traditional land-distribution grids.

The current limitation capability of power converters generates new opportunities and challenges in terms of protection against short circuit faults. Although the available energy of fault currents is limited, this makes detection of faults more difficult because fault current amplitude and gradient are very close to inrush current, overcurrents, and load connection to the distribution bus. For this reason, traditional fault detection methods are not readily applicable to multi-terminal dc distribution systems [23]-[25].

Figure 1.5 shows the baseline model for ship MVDC distribution system designed by ESRDC where we can observe the presence of multiple sources, load zones, distribution cables, and contactors or bus tie switches that can serve for isolation of part of the system and reconfiguration.

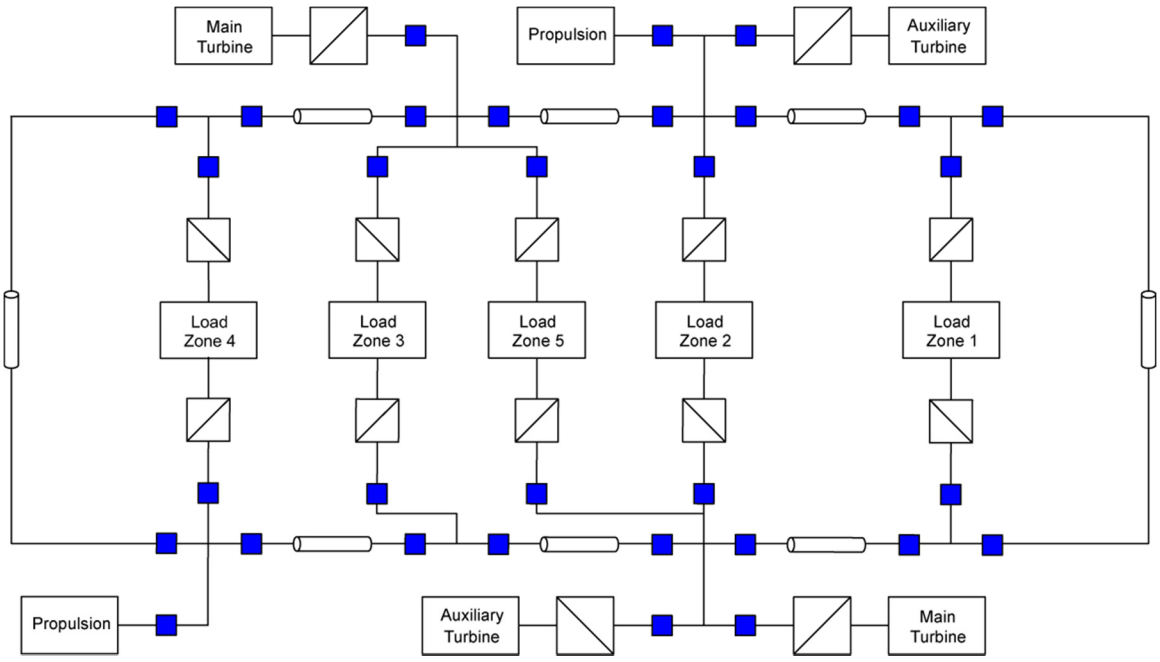

Figure 1.5 Multi-terminal zonal MVDC distribution system on a ship

In conclusion, for all the above reasons, the importance of this work consists in the developing of an enabling technology for the proliferation of dc distribution system for both ship and industrial applications.

SUMMARY

The main objective of this research consists in the development of a fault protection method that answers to the problem of fault protection in DC distribution systems for emerging applications. The significance of this project is twofold. On one hand several electrical applications need a more advanced power system that can be identified as DC distribution system. On the other hand the proposed protection method represents the enabler for the proliferation of DC distribution systems. Moreover, the contributions of this research consist in both the validation of the developed protection method and the

definition of design guidelines, and boundaries of operation for a variety of power systems.

Next, we provide a thorough overview of the problem of fault protection and detection in DC distribution systems, and a review of the protection methods that are at the state of the art.

CHAPTER 2

LITERATURE REVIEW AND BACKGROUND

2.1 FAULT PROTECTION IN DC SYSTEMS

In spite of many advantages, DC distribution systems are partially hindered by lack of appropriate circuit protection strategies and equipment [4],[5],[26]. In fact, protection of DC distribution systems against short circuit, especially at the Medium-Voltage level, is widely perceived to be a significant challenge because it can entail interrupting of large DC currents [27].

2.1.1 Interruption of short circuit fault currents in DC systems

Direct current presents different problems in comparison to alternate current. That is because of different phenomena associated with the interruption of high currents and the arc extinction. While alternating current has a natural crossing through zero every semi-period, this crossing does not exist for direct current (Figure 2.1). In AC systems the arc extinction happens when the current crosses zero during the opening of the circuit (Figure 2.2). In DC circuits, the current has to decrease down to null to guarantee arc extinction (forcing the current passage through zero).

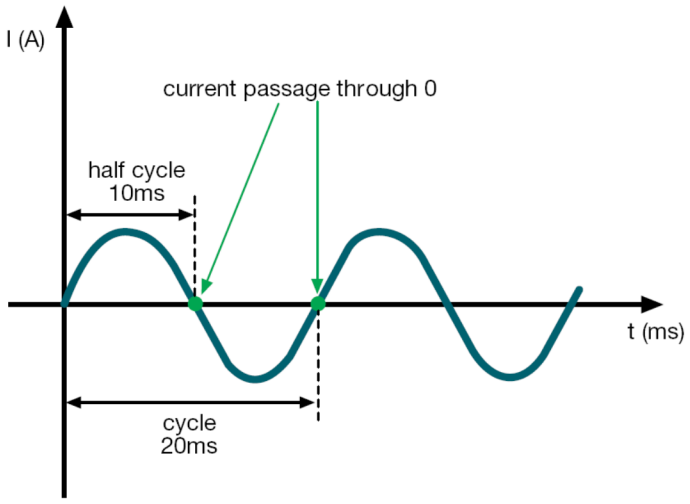

Figure 2.1 Point where is possible to extinguish the alternating current

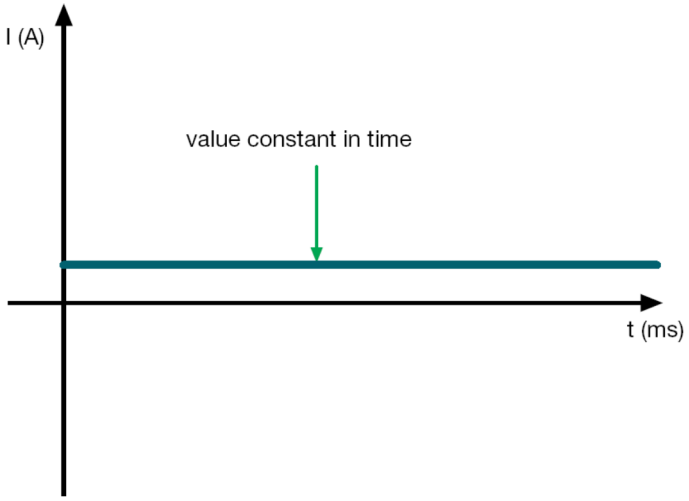

Figure 2.2 Non-existence of a natural zero-crossing in the direct current

Figure 2.3 illustrates a DC circuit that has to be opened by a circuit breaker. The resistance R and the inductance L represent equivalent parameters of the circuit. The following expression describes the voltage balance of the DC circuit: V is the rated voltage of the supply source, i is the current that has to be interrupted, and V_a is the arc voltage.

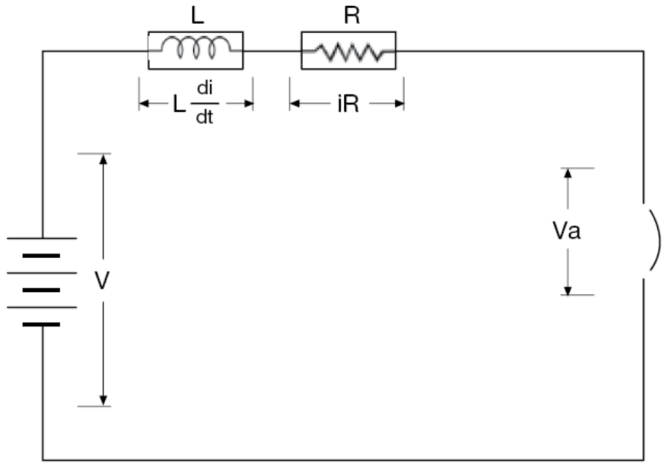

Figure 2.3 Equivalent circuit of a DC line

$$V = L\frac{di}{dt} + Ri + V_a \quad (1)$$

The formula can be written also as:

$$L\frac{di}{dt} = V - Ri - V_a \quad (2)$$

To guarantee arc extinction, it is necessary that:

$$\frac{di}{dt} < 0 \quad (3)$$

This relationship shall be verified when the arc voltage (V_a) is so high that the first part of the formula (2) becomes negative. It is possible to conclude that the extinction time of a direct current is proportional to the time constant of the circuit $\tau = L/R$ and to the difference between the arc voltage and the circuit supply voltage as shown in (2).

Figure 2.4 shows the graph of the opening of a short circuit by means of a circuit breaker. I_p is the short circuit making current, I_{cn} is the prospective short circuit current,

V_a the maximum arc voltage between the contacts of the circuit breaker, V_n the network voltage, T the time constant, t_o the instant of beginning of short circuit, t_s the instant of beginning of separation of the circuit breaker contacts, t_a the instant of quenching of the fault current.

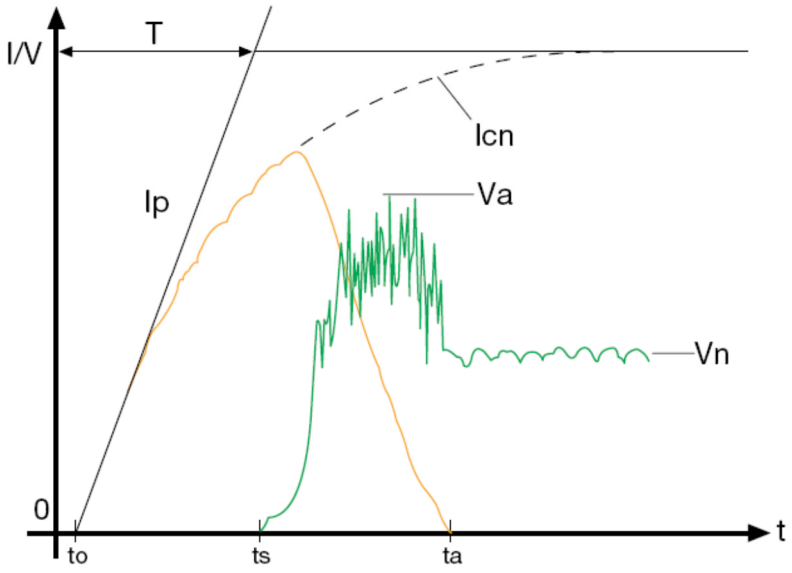

Figure 2.4 Oscillogram of the opening of a short circuit with a circuit breaker

When a short-circuit occurs in correspondence to the instant t_o, the current starts rising according t_o the time constant of the circuit. The circuit breaker contacts begin to separate, thus an arc starts from the instant t_s. The current keeps on rising for a short period after the beginning of contacts opening, then decreases depending on the increasing value of the arc resistance progressively introduced in the circuit. As can be noticed in Figure 2.4, during the arc interruption (t_s to t_a), the arc voltage remains higher than the supply voltage of the circuit. In correspondence of t_a, the current is completely quenched. As the graph in Figure 2.4 shows, the short-circuit current represented by the orange line is extinguished without abrupt interruptions which could cause high voltage

peaks. As a consequence, to obtain a gradual extinction, it is necessary to cool and extend the arc with arc eliminating equipment, so that increasing arc resistance is inserted in the circuit (with the consequent increase of the arc voltage V_a). This extinction involves energetic phenomena which depend on the voltage level of the system (V_n) and require circuit breakers to be connected in series to optimize performance during short circuit conditions. The higher is the number of contacts opening the circuit, the higher the breaking capacity of the circuit breaker [28].

Thus, one of the solutions to the problem of opening direct currents is the employment of traditional circuit breakers with the addition of specific devices to extinguish arcs. There are many kinds of arc eliminating equipment for circuit breakers. One of the most used is the arc chute that extinguishes the arc by fragmenting it. When contacts of the circuit breaker open, a magnetic device driven by the fault current blows the arc through the arc chute, the arc is fragmented in many parts, and is finally extinguished. Figure 2.5 shows an example of DC circuit breaker with arc chute on the top.

The method of increasing the arc voltage by extending and cooling the arc works as long as the voltage is in the low voltage range, but it becomes exceedingly difficult to increase the arc voltage to the medium voltage level. In fact the distance between contacts or the arc extending mechanisms get increasingly bigger at higher voltage for arcs with high current contents. Figure 2.6 shows the electric arc characterization across two contacts. Figure 2.7 shows how the distance between contacts in air increases with the current and voltage [34], [44]. Even if this picture represents the arc behavior for voltages and currents smaller than those at medium voltage and MW level, it is clear that high fault currents the distance between contacts to generate a significant voltage across

an arc increases drastically. For this reason, arc blowing mechanisms at the MW level becomes significantly big compared to the size of equivalent AC breakers. Figure 2.8 shows the position of circuit breakers on a DC shipboard electrical system to protect bus and components against faults.

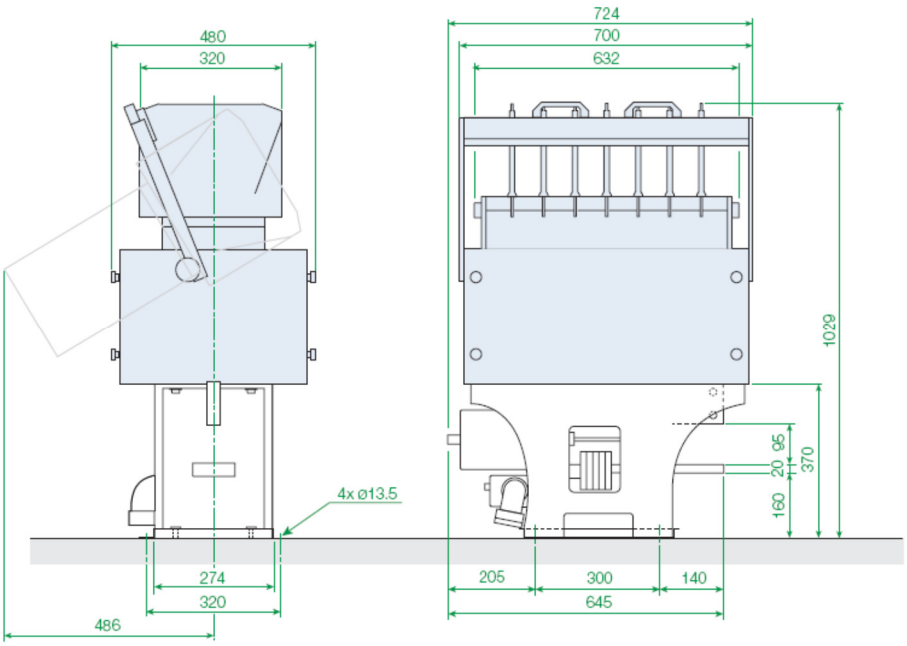

Figure 2.5 Example of arc chute over a DC circuit breaker (Grey section)

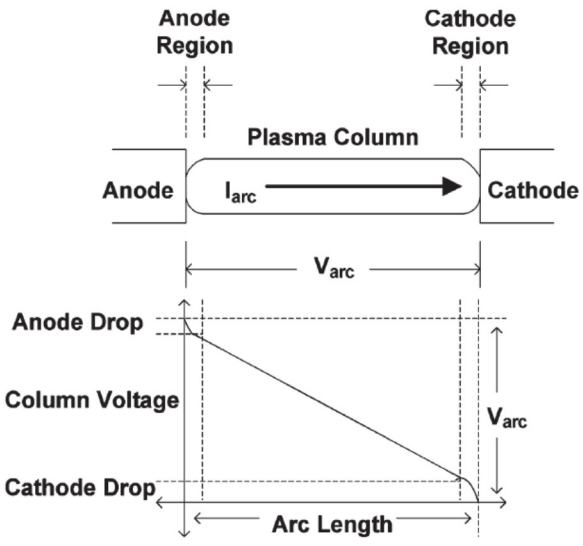

Figure 2.6 Electric arc characterization across two contacts

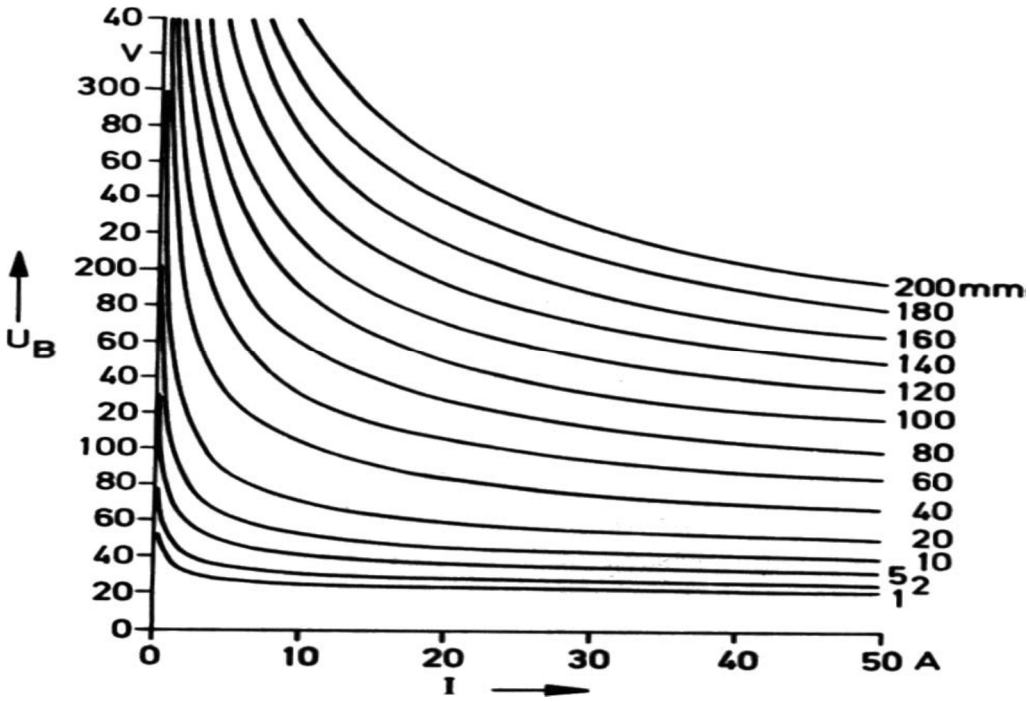

Figure 2.7 Arc voltage as function of both the arc current and the distance between copper contacts in air [31].

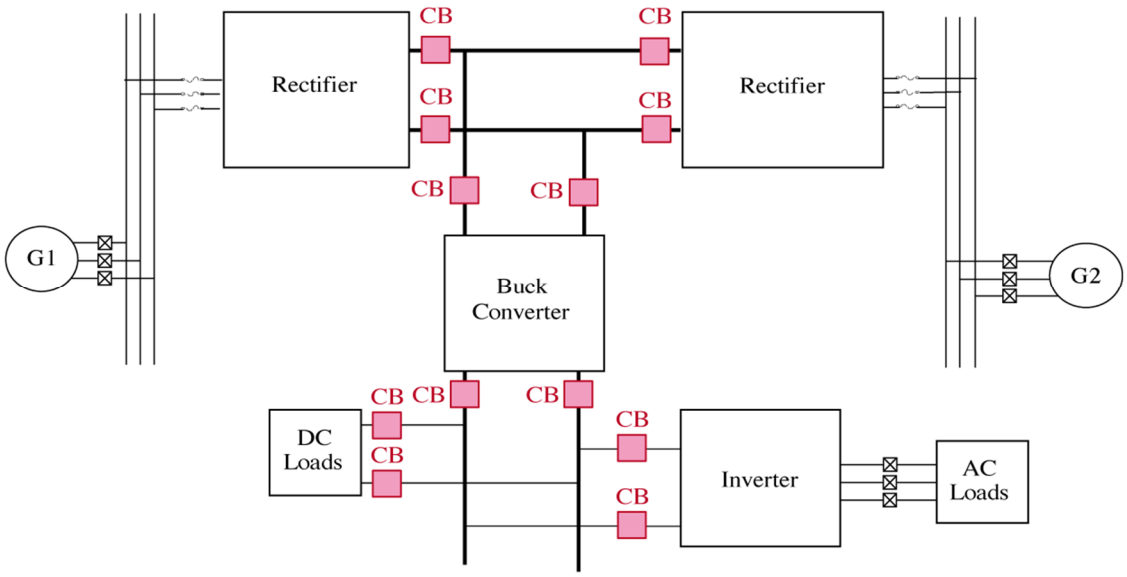

Figure 2.8 DC Circuit breakers (CB) needed at many locations on a DC shipboard electrical system to protect components against faults.

This solution is widely employed in DC systems such as DC electric traction up to 3600 Vdc [28], [58], [59], but circuit breakers and their arc eliminating equipment need a lot of space and weight, and are very expensive, especially for MVDC and HVDC. A further disadvantage of DC breakers is that in order to open a fault current the arc voltage between the contacts of the breaker has to become bigger than the system nominal voltage. This is important, especially in power systems that use semiconductor devices because it requires that all the components be rated for higher voltage than nominal operating voltage.

In the following paragraph, we have shortly analyzed different solutions that aim to solve the fault protection problem in DC distribution systems.

2.1.2 Approaches for protection against fault in DC distribution systems

Other solutions to solve the protection of DC systems are current oscillating equipment to turn off thyristors of the upstream rectifier, the use of the rectifier as a crowbar in order to open the circuit by means of the AC side circuit breaker, the employment of solid state based circuit breakers, the introduction of an oscillating equipment that assists an AC circuit breaker and the use of converters composed by turn-off switches that allow to limit and interrupt the current flow.

Many techniques have been proposed in the literature to induce an oscillating current to lead the current to zero, and thereby interrupt the current. These methods typically involve opening or closing of selective switches and charging or discharging of capacitors. The main drawback of all such methods is that they involve additional devices in series to the system component that needs to be protected. Also, these devices are slow

and bulky and may require extra charging circuits and power supplies [29], [30]. The approach presented in Figure 2.9 proposes to induce an artificial zero crossing in the fault current and utilize a conventional AC circuit breaker to interrupt the fault current.

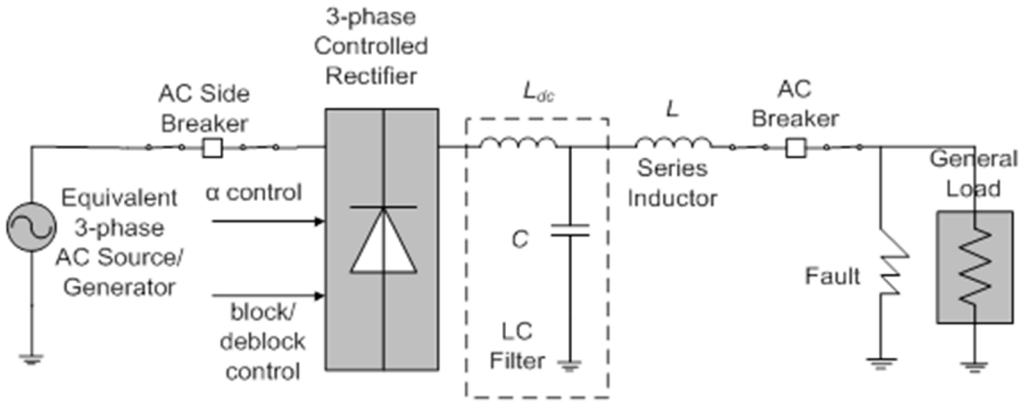

Figure 2.9 Series inductor to induce an artificial zero crossing in the fault current

Figure 2.10 illustrate the effect of inducing an artificial zero crossing in the fault current.

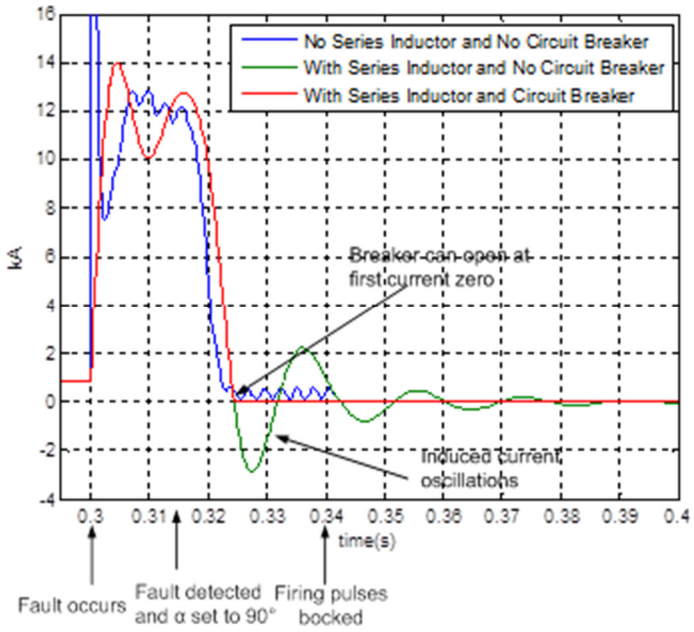

Figure 2.10 Fault current and artificial zero crossing caused by the introduction of a series inductor at the output of the supply power converter.

A resonant circuit made out the output filter of the converter and the addition of a series inductance forces the DC current to oscillate around zero. As soon as the current crosses zero a conventional AC breaker can interrupt the fault current. There are two main disadvantages introduced by this approach. First of all, this resonant circuit that makes the current oscillate can only be used in proximity of a supply power converter. In case of fault, this approach isolates the converter provoking the outage of the distribution system. Second of all, the added series inductor constitutes the introduction of extra losses and limitation of the controllability of the power converter.

Currently, commonly used approaches to isolate faults on the DC bus involve the use of VSC as a crowbar. The crowbar shorts the input and thus protects the converter from high currents, and the fault current is then interrupted by the AC circuit breaker on the source side. Despite this is an interesting solution, shorting of the AC side by means of switches of the bridge provides high current stress on switches during the fault. Another aspect of this technique is that the AC breaker has to be matched with the filtering inductors of the converters. In fact, a certain filtering inductor provides a specific limitation to the increasing of the current (*di/dt* limitation) and the AC breaker has to open before the fault current reaches the ratings of IGBT and diodes. Often common AC breakers are not fast enough to open before diodes brake. Moreover, the possibility to use this method only with a converter having an AC side limits this fault protection method.

Another interesting solution is the employment of solid state based circuit breakers (SSCBs). These are composed by one or more solid state switches, such as an IGBT or IGCT thyristor or ETO thyristor, and a snubber circuit that can be composed by a combination of resistances, capacitors, and metal oxide varistors (MOVs). Thanks to

recent developments, SSCBs offer the possibility of interrupting fault currents very fast. A SSCB can be placed at DC terminals of the VSC or on the downstream side of a dc-dc converter to interrupt the fault current as shown in Figure 2.11, and isolate the fault [20], [29], [31].

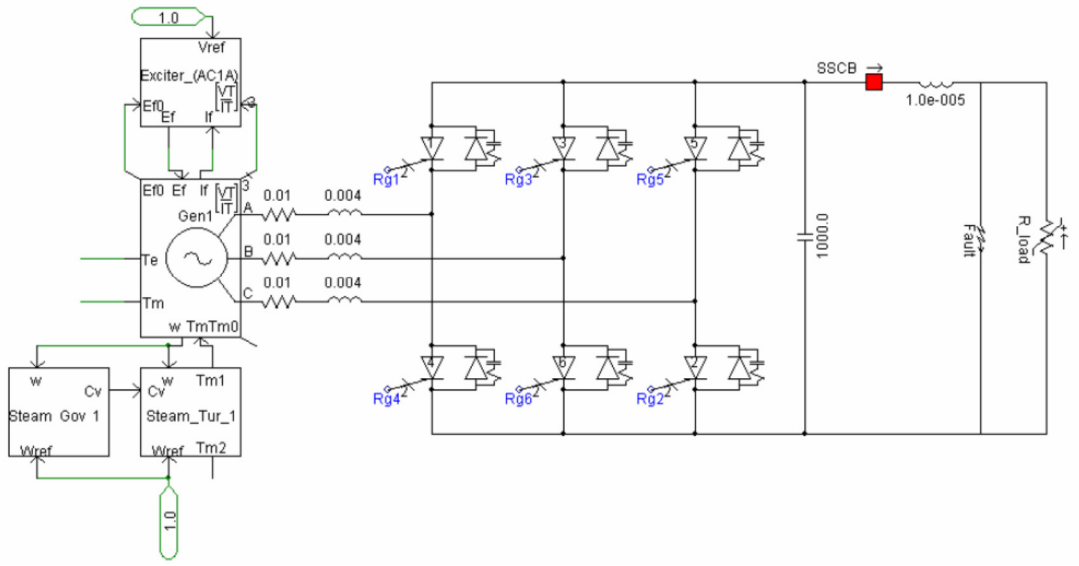

Figure 2.11 Protection against faults using solid state circuit breaker

The development of such devices is becoming more and more interesting, but some drawbacks make the employment of SSCB disputable. First of all, this kind of circuit breaker is limited by the maximum current and the maximum voltage that the solid state device can stand. In the case of semiconductor devices, compared to mechanical contacts, overrating of the solid state switch can imply exponential increase of costs. Secondly, the resistance of solid state devices is much larger than the resistance of a mechanical circuit breaker. This implies more losses during the on-state and thus the reduction of the overall system efficiency. Thirdly, since semiconductor devices have non-zero leakage current a positive disconnect (i.e. contactor, bus tie switch, disconnect) is also needed to physically isolate the faulted section and servicing the system. Fourthly, the solid state device must

withstand whatever voltage is required to drive the current to zero, and dissipate whatever energy is involved in driving the current to zero. In principle, solid state devices can drive the current to zero very quickly with high overvoltages.

A novel type of DC circuit breaker based on semiconductor devices utilizes a Z-source LC circuit in order to automatically commutate a main-path SCR Thyristor during a fault (Figure 2.12) [60]. This SSCB can provide a fast fault current interruption that consists with the opening of the SCR (less than 1 ms). Despite the fact that this device is very fast in breaking the fault current, the resonant circuit that commutate the thyristor effectiveness strongly depends on the fault characteristics and the parameters of the components connected upstream and downstream. Moreover, this resonant circuit introduces voltage oscillations that can lead to overvoltages on other components in the system. A common drawback of SSCBs is that they introduce conduction losses, thus reducing the efficiency of the system, and they provide a non-physical isolation due to leakage currents of the semiconductor device.

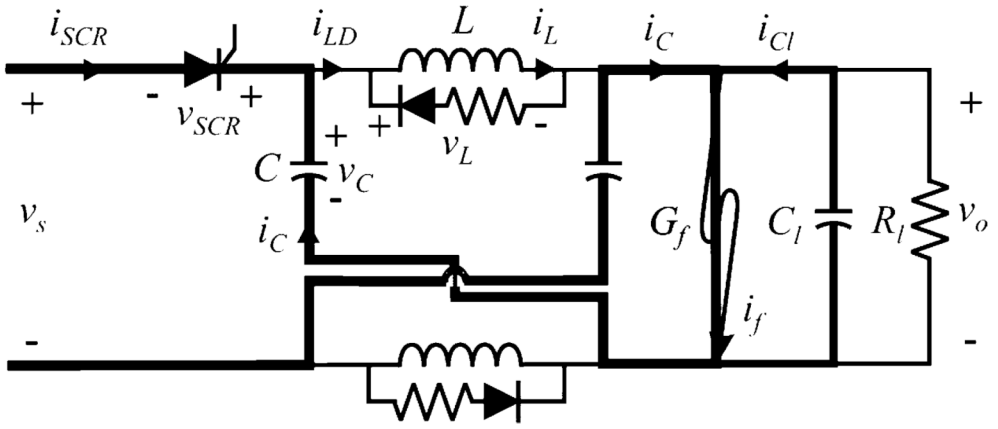

Figure 2.12 Conduction path of a fault current in a Z-source circuit breaker.

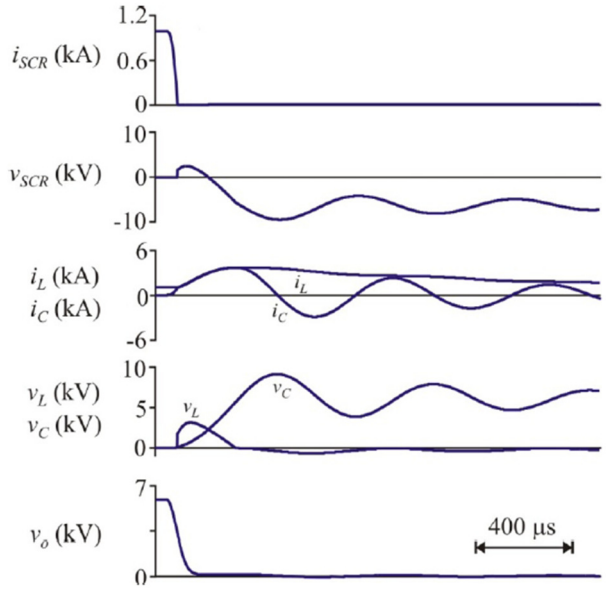

Figure 2.13 Currents and voltages of the Z-source breaker

In practice, the speed is limited by the voltage that can be developed across the solid state device (max withstand voltage). Furthermore, another drawback of solid state based breakers is that multiple reclosing and reopening are limited by the ability of dissipating heat by the MOV or other devices that are coupled to the solid state device for limiting overvoltages. In fact, in every opening-reclosing cycle, the varistors that is limiting the voltage on the SSCD has to be able to dissipate a certain amount of energy until it reaches saturation. At this point, the device is not able to operate until it cools down.

New approaches rely on controlling the converter duty cycle to limit and quench fault currents [20]. Fully controllable electronic power converters composed by switches with turn-off capability (IGBT, MOSFET, GTO, etc.) can perform fault current limitation and fault current interruption when properly designed. Figure 2.14 shows an example of switching power converter that can be controlled in voltage and current mode and that can provide fault current limitation.

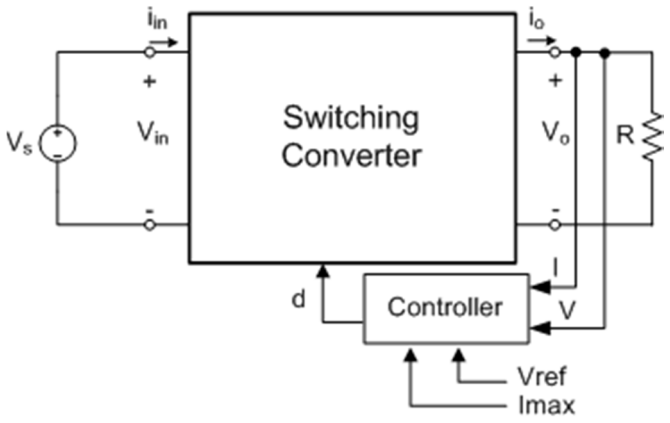

Figure 2.14 Controllable switching power converter that can perform current limitation and fault current interruption.

After fault detection on the downstream side, the converter can provide a protection action by either actively limiting the fault current or turning off the converter switches. The action of hard turn off of switches interrupts the current from the primary side immediately, but the current on the load side does not cease immediately. The energy stored in the output inductor is freewheeled through the freewheeling diodes of the converter. When this energy is completely dissipated, the fault is completely interrupted. In case of a current limiting action of the power converter, the fault current can be either limited to a certain safe value or driven to zero and definitely interrupted.

Chapter 3 explores the potentials of using power converter as a mean for limiting and interrupting fault currents in DC distribution systems. Moreover, it explains how the combination of the fault current limiting capability of power converters and mechanical contactors can provide and effective and reliable fault isolation.

Despite the fact that power converters can provide fault current limitation and thus participate to the protection of the system, the current limiting capability of power converters makes detection of faults more difficult. The next section gives an overview

on the challenges of fault detection in DC systems that are fed by controllable power converters.

2.2 FAULT DETECTION IN DC SYSTEMS

Multi-terminal DC distribution systems have been indicated as one of the best candidates for systems that need high efficiency, reliability and flexibility. In fact that can easily provide power sharing between multiple sources, low voltage drop among the distribution bus, and can be reconfigured to provide redundancy of power delivery [49].

On the one hand, multi-terminal dc distribution systems offer the threat that multiple sources or storage elements might feed fault currents, but on the other hand, each of these sources will be interfaced by means of fully controllable converters and so each is able to limit its own contribution to any fault current. Although the energy available to drive fault currents can be actively limited, this makes detection of faults more difficult because the fault current amplitude and gradient may be not much different from the normally-expected values of circuit currents. For this reason, traditional fault detection methods are not readily applicable to multi-terminal dc distribution systems [21], [52], [53].

2.2.1 Traditional methods for fault detection

Overcurrent relays, distance relays, differential current relays, minimum voltage relays as fault detection systems for traditional ac distribution systems are widely studied and provide a reliable way of coordinating fault protections in order to isolate the smallest portion of the system neighboring a fault. Many of these relays can be easily adapted to

work in a correspondent dc distribution system powered by sources with small internal impedances and thus capable of providing fault currents much bigger than their nominal current in the event of short circuit.

In the case of dc distribution systems powered by sources interfaced to the distribution bus through current limited power converters, some of the traditional detection methods used in ac are not readily applicable because fault currents limited by converters are not so much larger than normal operating currents.

In fact, methods based on current thresholds and current derivative threshold cannot be effective because of the similarity of nominal operation currents (load steps, load connections, capacitor connections, etc.) with short circuit fault currents since the current contributions coming from the sources can be limited by power converters.

Methods based on voltage sag (minimum voltage) measurement might be good for tripping the converters off-line when a fault happens but they cannot discriminate between faults in different locations. For this reason coordination of converters and contactors can be difficult [54].

Methods based on impedance or distance relays are widely used in traditional distribution and transmission systems with a radial configuration and the presence of multiple sources in different locations. In fact, if there are too many radial lines and buses, the time delay for breakers closest to the source become excessive if the protection system is based on current-time tripping curves. Instead relays that respond to a voltage-to-current ratio are more sensitive to faults than current alone [55]. In case of fault, the impedance relay sees the impedance shifting from a dominantly resistive impedance to a smaller and dominantly inductive impedance typical of the line impedance. In this way

the impedance relay permits discrimination between faults in different locations [37]. Figure 2.15 illustrates an example of impedance relay and how the relay can discriminate between normal operation conditions, fault conditions, and whether the fault is in Zone 1, 2, or 3.

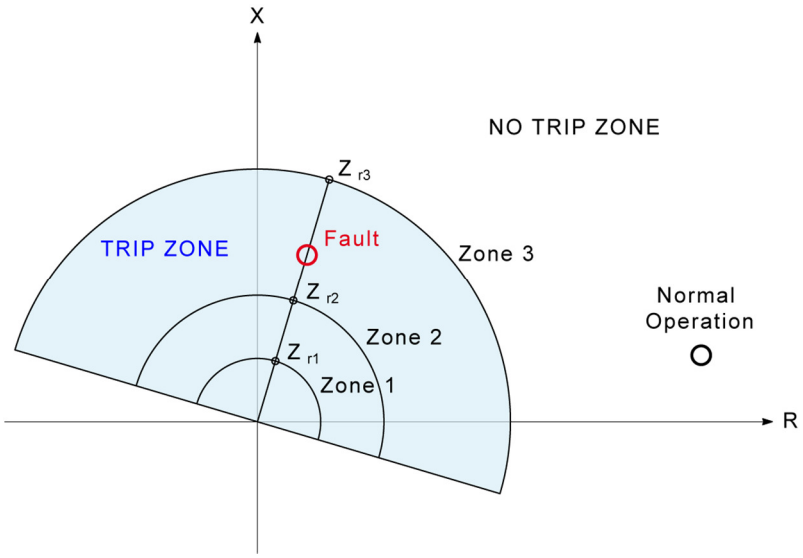

Figure 2.15 Impedance relay with directional constraint for protection of ac radial distribution systems

Whereas in ac systems the relay reacts to impedance changing, in dc systems direct measurement of the impedance is not possible because of the absence of a fundamental frequency on which to base impedance.

2.2.2 Emerging methods for fault detection

Some emerging methods propose to measure the impedance spectrum of the bus by injecting a broad-spectrum current perturbation and then measuring the resulting voltage perturbation and extracting the associated impedance magnitude and phase spectrum [24], [25]. Figure 2.16 illustrates an example of wideband impedance spectrum measurement by injecting a broad-spectrum perturbation in the distribution bus.

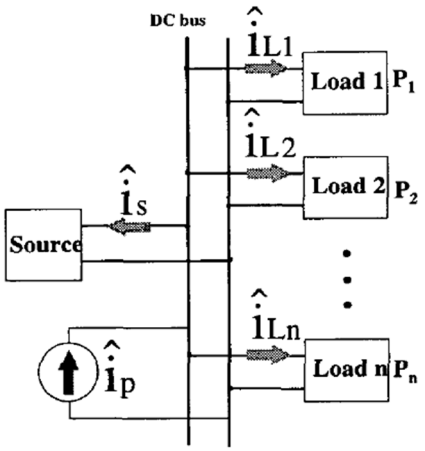

Figure 2.16 Fault location through wideband impedance spectrum measurement by injecting a broad-spectrum perturbation

Figure 2.17 shows magnitude and phase of the bus impedance with open loop converters. Figure 2.18 shows magnitude and phase of the bus impedance in the case of current and voltage controlled source converters feeding the distribution bus. In both cases, the graphs compares the impedance measurement in the case of a healthy distribution bus (blue), bus affected by a short-circuit fault at 50 m from the measurement point (red), and bus affected by a short-circuit fault close to the measurement point (green). Even though the measurement of the distribution bus impedance gives very detailed information about the state of the bus, we can notice that the low frequency value of the impedance is not always an interesting variable for discerning between a healthy system and short-circuit faults at different distances. In fact, whereas in the case of open loop source converters feeding the bus the difference between healthy and fault condition is clear (Figure 2.17 a), in the case of current and voltage controlled feeding converters the distinction between healthy and faulty can be challenging. This is mostly due to the controlled converters effect of actively reducing the output impedance for stability and control purposes [56].

On top of the computational challenge, methods based on impedance measurement through injection might lead to uncertain results in case of arcing faults, since the calculation of the impedance is based on linear assumptions.

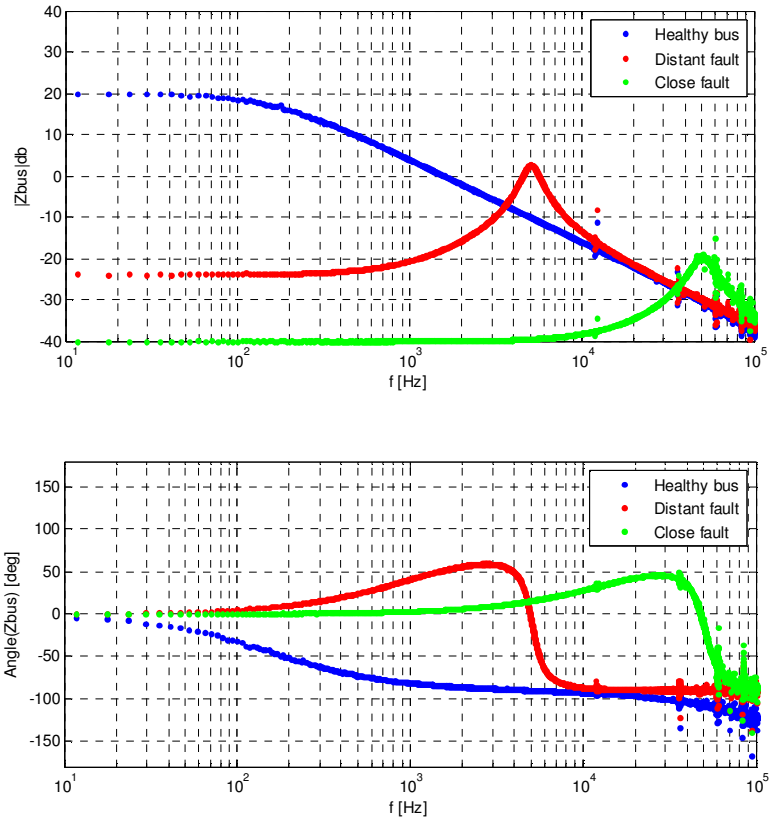

Figure 2.17 Bus impedance measurement through signal injection in the case of open loop source converters feeding the distribution bus.

Although impedance estimation through noise injection can collect valuable information about the system, it requires high bandwidth measurements and intense computing capability and may therefore be more suitable for identifying a fault location after the system has been protected than for detecting a fault in order to protect against it.

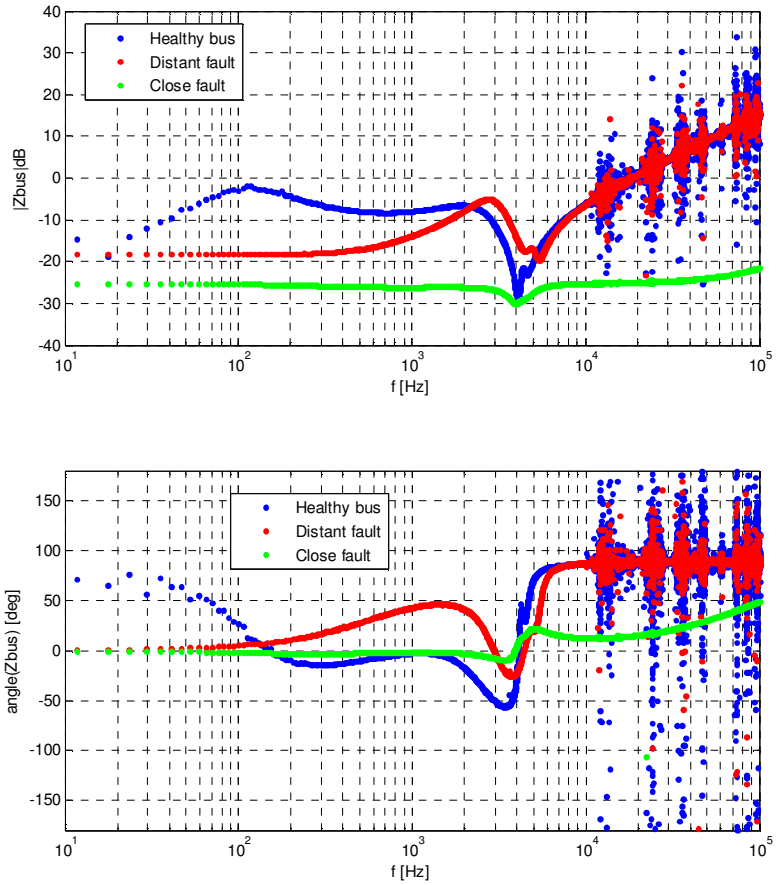

Figure 2.18 Bus impedance measurement through signal injection in the case of current and voltage controlled source converters feeding the distribution bus.

SUMMARY

Fault protection against ground and short-circuit faults is one of biggest challenges of DC power distribution systems. On one hand, traditional circuit breakers are not easily to implement beyond a certain voltage level and need to be replaced with alternative technologies. On the other hand, traditional fault detection relays are not readily applicable to multi-terminal DC distribution systems that are fed by current and power limited sources.

The following chapters describe new solutions for both aspect of fault protection in dc distribution systems: fault isolation and fault detection. Chapter 3 demonstrates how the

combined control of power converters and mechanical contactors can provide a reliable fault protection and isolation of the faulted part of the system. Chapter 4 illustrates a fault detection method that is suitable for multi-terminal DC and that coordinates the action of power converters and contactors with local measurement only.

CHAPTER 3

FAULT PROTECTION FOR DC DISTRIBUTION SYSTEMS

The approach that we describe and analyze here eliminates DC circuit breakers in favor of simpler, smaller grid segmentizing contactors by coordinating the action of these contactors with the action of fully controllable electronic power converters. While this method has been experimentally proven for DC-DC converters, it can also be applied to fully-controllable AC-DC converters that may interface AC sources to the DC power system. We emphasize that the converters must be fully controllable; they cannot be of topologies that contain, for example, diode pass elements such as simple diode rectifiers or simple DC-DC boost converters. According to this method, power converters are commanded to briefly de-energize the distribution grid so that the contactors can open to isolate the faulted branch and reconfigure the remaining network without breaking large currents.

This chapter presents an analysis of fault dynamic in DC distribution systems, together with experimental validation of the fault protection method, and bounds the performance of the protection technique. We first provide more details of the protection technique, and we present an analysis of the system dynamics during a fault and provide mathematical estimates of fundamental parameters, such as current peak, time for a safe tripping of contactors, complete isolation of the fault, and time for power restoration, and parametric estimates of system performance.

Then, with the help of a more complex simulation model, we explore the fault dynamics and the dependence of fault current behavior on physical dimensions of the grid, system nominal voltage, and number of power sources. Simulations confirm the validity of the mathematical expressions, and experiments with a scaled down DC distribution system validate both the theory and the simulation model. Finally, we summarize the influence of system parameters on the performance of the protection scheme, present design considerations and limitations on components and system parameters, as well as considerations on selection of contactors for reconfiguring the distribution system, on ride-through capability for loads, and on power quality.

3.1 OPERATION OF THE PROTECTION METHOD

According to the approach defined here, after a fault is identified, power converter settings and contactor activation signals should be operated according to the following sequence:

1) The current limit set points of converters that feed the affected bus should be reset to zero.

2) As soon as the initial discharge fault current decays to the rated opening current of the mechanical contactor or bus tie switch, but before the current is actually zero, appropriate contactors should be actuated to reconfigure the system and to isolate the faulted branch. This operating mode takes advantage of the forward voltage of the low-current inter-contact arc to more-rapidly drive the system current to zero. But during this time, the current is small enough so as not to damage the contactor.

3) After the current is driven to zero and any other contactors are repositioned to effect any desired system reconfiguration, converter set points are reset so as to re-energize the system.

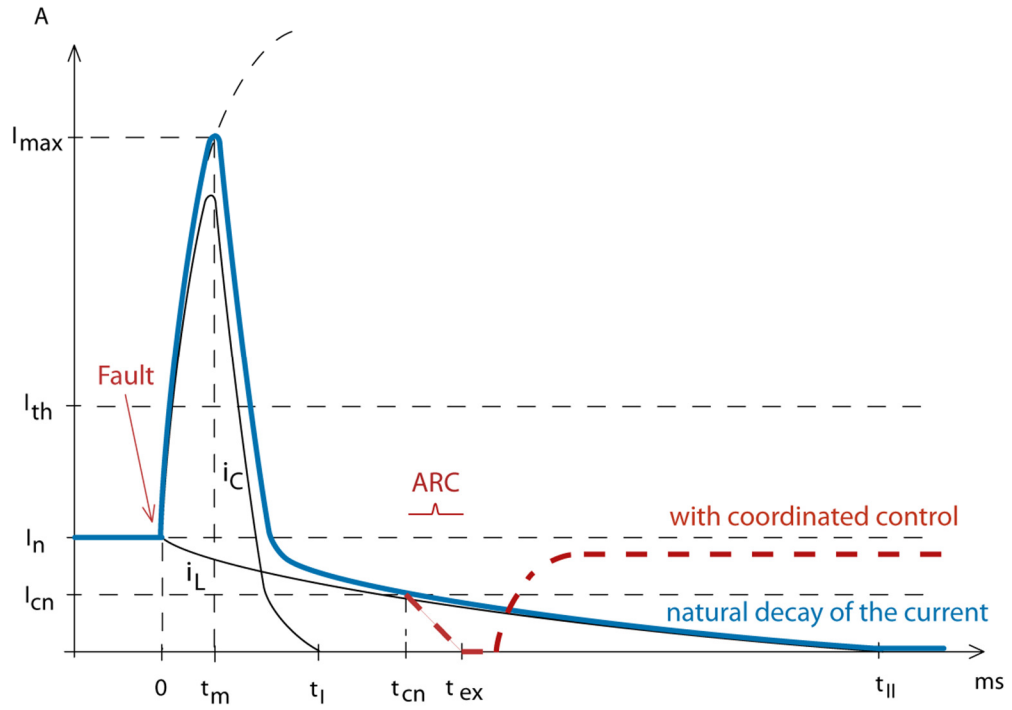

Figure 3.1 Fault currents, showing capacitive iC and inductive iL contributions to the currents and the faster extinction of fault current by coordinated action of the power converter and the bus tie switch (dashed line), as compared to longer current decay if contactor is not opened to take advantage of the arc voltage drop (solid line).

Figure 3.1 shows notional current waveforms associated with this controlled power sequencing approach corresponding to the case when a short circuit occurs in the cable of the distribution bus (e.g. bus serving load center 3 of Figure 3.2). The thick dashed waveform shows how rapidly the system can be reconfigured and power can be restored to a healthy branch of the system, whereas the thick solid line shows the longer time that would be needed to recover system operations if the controlled sequencing was not used to take advantage of the forward arc voltage of the contactor to help in driving the current

to zero. Without this arc voltage, the current decay rate is determined only by the equivalent *RL* time constant of the fault path.

The fault current exhibits two main transient behaviors, as illustrated by the thin black lines in Figure 3.1: a fast peak i_C due to the discharge of filter capacitors and a slow decaying behavior i_L due to the discharge of filter inductors. During the first interval ($0 \leq t < t_I$), the current increases rapidly as energy stored in the output capacitors of the converters is discharged through the resistive component of the fault. After this rapid discharge during the second time interval ($t_I \leq t \leq t_{II}$), the current decays more slowly, as the filter inductor of the main converter is discharged. According to the protection method, once the fault current drops below the rated opening current of contactor 3 (t_{CN}), contactor 3 opens and when the current stops flowing through the contactor the fault is isolated (t_{ex}). At this point, the output reference of the converters that interface the sources to the bus can be reset from zero current to the desired bus voltage. I_n is the nominal current of the distribution system, I_{cn} is the nominal opening current rating of mechanical contactors, I_{th} is the current threshold for fault detection, I_{max} is the value of the fault current peak.

Two important features of the proposed protection scheme are (1) the reduction of the fault current by limiting the energy discharged into the fault to only that energy stored in the filter components of the converters, and (2) the shortening of the out of service time via coordination and control of converters and contactors (segmentizers and bus tie switches).

3.1 SYSTEM DYNAMICS DURING A FAULT IN DC SYSTEMS

In general, multi-source power systems exhibit complex dynamics and transient responses that depend on the system parameters. In this section, we use simplifying assumptions to estimate important parameters, such as peak fault current, time for safe contactor opening, and total fault current extinction time. Then, using a detailed model of the system, we verify the obtained estimates by simulation of a dc distribution system. Simulation results reveal how the performance varies with parameters such as cable length, nominal operating voltage, and number of connected power sources.

3.1.1 System model during a fault

Consider the dc distribution system shown in Figure 3.2. Following a short-circuit fault in the power system, the system control must go through a number of operation phases:

- fault identification (from the moment of fault until fault is identified)
- bus de-energizing (fault identified and power converter operation is blocked)
- faulty branch isolation (a contactor opens to physically isolate the part of the system affected by a short circuit fault)
- bus re-energizing (converters are turned back on and loads are re-energized)

Each of these operation phases can be represented with a particular system model. For simplicity of the analysis, we assume that time for identifying the fault is negligible, i.e. it is much less than the time constant of the power supply output filter. Then the system goes directly into the second phase; and a linear model of the system can be used, as shown in Figure 3.3.

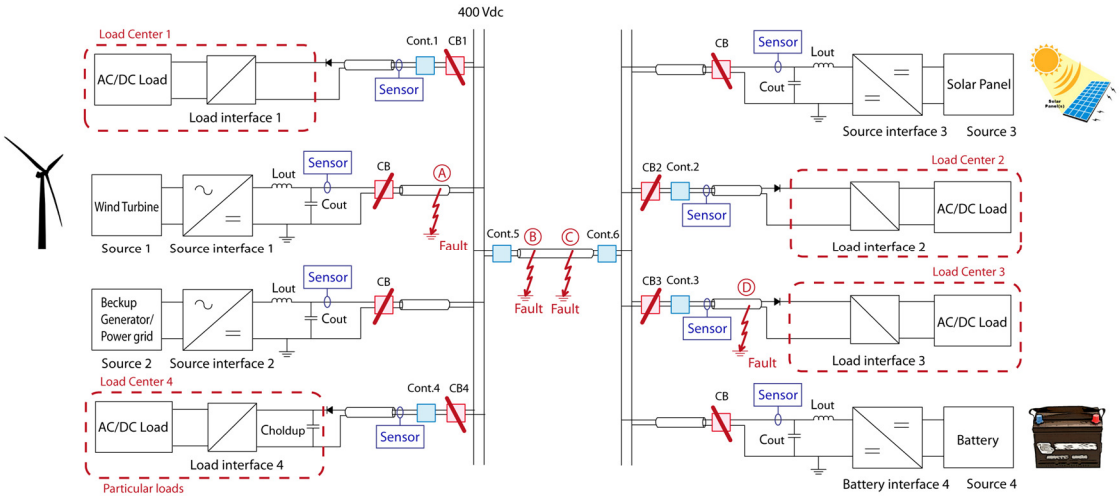

Figure 3.2 Structure of a notional dc microgrid, showing location of circuit protection elements, circuit breakers (CB) and contactors (Cont.), and representative locations of possible faults

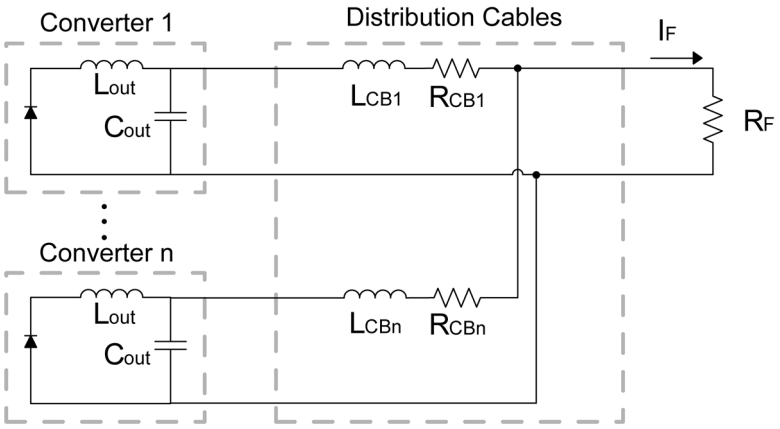

Figure 3.3 DC distribution system equivalent circuit during a fault when converters are in cut-off mode.

Here, cables are represented only by their inductive and resistive characteristics under the assumption that the highest frequency of the pulse characteristic of the transient discharge event of filter capacitors and inductors has a wavelength much longer than the length of the transmission line. This approximation is valid for systems of size less than approximately 10 km, and in different cases a distributed parameter model of the cable should be used [32], [33]. Appendix B analyzes the validity of this assumption.

The dynamic model of the simplified system can be written as follows

$$\begin{cases} \frac{di_{Loutj}}{dt} = \frac{1}{L_{outj}}\left(V_{gj} - V_{Coutj}\right) \\ \frac{dv_{Coutj}}{dt} = \frac{1}{C_{outj}}\left(i_{Loutj} - i_F\right) \\ \frac{di_{Fj}}{dt} = \frac{1}{L_{CBj}}\left(V_{Coutj} - R_{Fj}i_F\right) \end{cases} \quad (1)$$

$$i_F = \sum_{j=1}^{n} i_{Fj} \quad (2)$$

where V_{gj} is the equivalent source on the upstream side of each converter and n is the number of supplying converters, and R_F is the equivalent resistance of the fault. L_{out} and C_{out} are the values of the output filter elements of converters connected to the microgrid, and L_{CBn} and R_{CBn} are the parameters of the section of cable between converter n and the fault. Equation (2) expresses that the fault current (i_F) is composed of elements from each of the individual converters. Moreover, as can be seen from Figure 3.1, the fault current (i_F) consists of two components having fast (i_{Ff}) and slow (i_{Fs}) dynamics, respectively, as expressed in (3)

$$i_F = i_{Ff} + i_{Fs} \quad (3)$$

In our analysis we use this separation of the system dynamics to simplify the obtained results.

3.1.2 Peak fault current

During the second phase of operation, the converters are shut off so the energy dissipated in the fault is limited to the energy that was previously accumulated in the reactive components of the system – the output filter capacitors C_{OUT}, inductors L_{OUT}, and the cable inductance L_{CB}. It is clear that the peak fault current depends on the configuration of the system, the location of the fault, and the operating conditions when the fault happens. In this section, we first analyze the response for a single-source system and then for a multisource system.

For a one source system, the system model can be written as:

$$\begin{cases} \frac{di_{Lout}}{dt} = \frac{1}{L_{out}}\left(V_g - V_{Cout}\right) \\ \frac{dv_{Cout}}{dt} = \frac{1}{C_{out}}\left(i_{Lout} - i_F\right) \\ \frac{di_F}{dt} = \frac{1}{L_{CB}}\left(V_{Cout} - R_F i_F\right) \end{cases} \quad (4)$$

where R_F is the resistance of the fault current path that includes the resistance of the fault contact and the resistance of that part of the cable between the fault and the power source as

$$R_F = R_{Fault} + R_{CBj}.$$

To simplify the analysis we assume that output filter inductance of the converter is significantly larger than the cable inductance and that the fault current consists of fast and slow dynamics as shown in (3). This assumption reduces the system (4) to that shown in

(5) and allows us to consider the fast and slow transients separately. The fast transient corresponds to discharge of the output capacitor through the fault, and the slow transient to discharge of the output filter inductance.

$$\begin{cases} \frac{di_{Ff}}{dt} = \frac{1}{L_{CB}}\left(v_{Cout} - i_{Ff}R_F\right) \\ \frac{dv_{Cout}}{dt} = -\frac{1}{C_{out}}\left(i_{Ff}\right) \\ \frac{di_{Fs}}{dt} = -\frac{1}{(L_{out}+L_{CB})}i_{Fs}R_F \end{cases} \quad (5)$$

Arranging system (5) as a single second order equation with respect to i_{Ff} we get

$$L_{CB}C_{out}i''_{Ff} + C_{out}R_F i'_{Ff} + i_{Ff} = 0 \quad (6)$$

$$(L_{out} + L_{CB})i'_{Fs} + R_F i_{Fs} = 0. \quad (7)$$

The evolution of the fault current is defined by the following expressions

$$i_{Ff}(t) = C_1 e^{p_1 t} + C_2 e^{p_2 t} \quad (8)$$

$$i_{Fs}(t) = C_3 e^{p_3 t} \quad (9)$$

where:

$$p_{1,2} = \frac{-C_{out}R_F \pm \sqrt{(C_{out}^2 R_F^2 - 4L_{CB}C_{out})}}{2L_{CB}C_{out}}$$

$$p_3 = -\frac{R_F}{(L_{out}+L_{CB})}$$

$$C_1 = i_{Ff}(0) - C_2$$

$$C_2 = \frac{(v_{Cout}(0)-i_{Ff}(0)R_F-i_{Ff}(0)L_{CB}p_1)}{L_{CB}(p_2-p_1)}$$

$$C_3 = i_{Fs}(0).$$

Using equations (8) and (9), the maximum fault current i_{Fmax} and the time the peak occurs t_m can be found as

$$t_m = \frac{ln\left(-\frac{C_1 p_1}{C_2 p_2}\right)}{p_2-p_1} \tag{10}$$

$$i_{Fmax} = i_{Fs}(t_m) + i_{Ff}(t_m). \tag{11}$$

Expressions (8), (9), (10) and (11) clearly show the dependency of peak fault current on the system reactive components. From (7) it follows that the rate of increase of fault current is inversely proportional to the cable inductance.

Applying a similar procedure to the multi-source system, and assuming that all the primary sources are interfaced to the power system through converters having output filters with similar characteristics, we can approximate the fault current for the case of *n* parallel power sources as

$$i_{Fmax} = \sum_{j=1}^{n} i_{Fmaxj}(t_m). \tag{12}$$

3.1.3 Proper contactor opening time and dynamics

For coordination between power converters and contactors, the important factors are the time the contactor starts opening, the time for the contacts to reach an appreciable distance to generate an arc, the arcing process time, and the voltage imposed across the contacts of the contactor by the arc.

Opening the contactor at precisely the right time is one of the key elements of this scheme. The proper time can be found by solving equation (8) and (9) for the time at which the slow part of the current decreases to the desired operating current of the contactor, depending on the designer choice in the trade-off between power restoration time and lifetime of contactors. We find the desired opening time by solving the following equation

$$i_{Fs}(t_{cn}) = C_3 e^{p_3 t} = I_{cn} \tag{13}$$

where I_{cn} is the chosen current at which it is safe to open the contactor. The solution of (13) is presented in (14)

$$t_{cn} = \frac{(L_{out}+L_{CB})}{R_F} \cdot ln\left(\frac{i_{Fs}(0)}{I_{cn}}\right) \tag{14}$$

where $i_{Fs}(0)$ stands for initial fault current that is equal or less than the rated current of the system (i_r).

In case of multisource systems, the time for safe opening of the contactor on the faulted branch (t_{cn}), depends on the combination of dynamics of the circuit between the fault and the different sources, and can be found by solving equation (15) for t_{cn}

$$\sum_{i=1}^{n} C_{3i} e^{p_{3i} t_{cn}} = I_{cn}. \quad (15)$$

This formula gives an estimation of the tripping time of the contactor. After power converters are set to zero current, the tripping command is sent by the controller to the contactor on the faulted branch as soon as the current goes under the defined threshold.

Since the contactor is opened before the current is zero, an arc will be established between the contacts. The arc voltage opposes the inductive voltage to cause the fault current to decrease faster than the natural decay rate for the equivalent *RL* circuit of the fault current path. We approximate this arc voltage as 100 V, though of course it is a (weak) function of electrode materials, current, electrode spacing and other parameters [34]. The decay of fault current during the slow dynamic phase, and the influence of the contactor voltage [35], can be analyzed using the equivalent circuit of Figure 3.4.

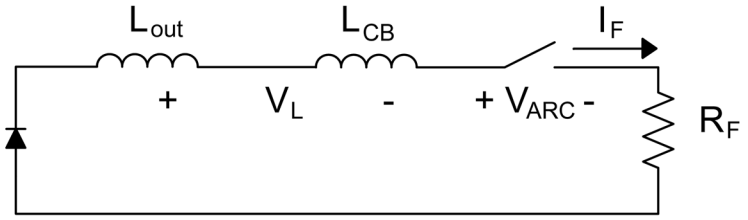

Figure 3.4 Equivalent circuit during contactor opening.

During the opening of the contactor the current must satisfy the following equation

$$v_L = (L_{out} + L_{CB}) \frac{di_F}{dt} = -R_F i_F - V_{ARC} \quad (16)$$

which has solution

$$i_F(t) = C_4 e^{p_4 t} - \frac{V_{ARC}}{R_F} \tag{17}$$

where:

$$C_4 = I_{cn} + \frac{V_{ARC}}{R_F}$$

$$p_4 = -\frac{R_F}{(L_{out}+L_{CB})}.$$

The duration of the arcing process (t_{ARC}) is defined by expression (18). In case of multisource systems, the arc voltage opposes to the components of the fault current coming from different sources, and the duration of the arcing process (t_{ARC}) can be calculated by solving equation (19) for t_{ARC}.

$$t_{ARC} = \frac{1}{p_4} ln\left(\frac{V_{ARC}}{C_4 R_F}\right) \tag{18}$$

$$\sum_{i=1}^{n} C_{4i} e^{p_{4i} t_{ARC}} - \sum_{i=1}^{n} \frac{V_{ARC}}{R_{Fi}} = 0 \tag{19}$$

The time to totally extinguish the fault current (t_{ex}) is shown by equation (20). In (20) we also consider the time for the contacts to reach an appreciable distance to generate an arc (t_{mech}) that is dependent on the mechanical design of the contactor. For example, the contactor used in our simulations and experiments had a mechanical delay of about 3 ms [42]. Other kinds of contactors can be faster, as shown in Section 3.2.2. The minimum

time for power restoration (t_{rest}) can be estimated by (21), where I_n is the nominal current of power converters and $I_{overload}$ is the overload current capability of power converters.

$$t_{ex} = t_{cn} + t_{mech} + t_{ARC}. \tag{20}$$

$$t_{rest} = t_{ex}\left(1 - \frac{I_n}{I_{overload}}\right) \tag{21}$$

The estimate of the time to totally extinguish the fault current and the time for power restoration represent important components of the performance of the protection method, and it is compared to the result of simulations and experiments in section 3.2.

For example, using the parameters shown in Table 3.1 in the power system studied later in simulations and experiments, we can estimate the value of the current peak (I_{Fmax}), the current peak time (t_m), the time for safe opening of the contactor (t_{cn}), the arcing process time (t_{arc}), the time for total extinction of the fault (t_{ex}), and time for power restoration (t_{rest}) as shown in Table 3.2.

TABLE 3.1

PARAMETERS OF THE POWER SYSTEM

V [V]	I_n [A]	C_{out} [µF]	L_{out} [mH]	L_{CB} [mH]	R_{CB} [Ohm]
400	80	600	1.5	0.06	0.15

The system in the example has one source connected to the distribution cable, overload capability of 150%, an equivalent resistive load of 32 kW, and a fault at 200 m from the source. Table 3.2 illustrates the results of the analysis for this scenario, and also gives an estimation of typical operation times of the protection method.

TABLE 3.2

ESTIMATION OF CHARACTERISTIC VALUES OF THE FAULT DYNAMIC

I_{Fmax} [A]	t_m [ms]	t_{cn} [ms]	T_{ARC} [ms]	t_{mech} [ms]	t_{ex} [ms]	t_{rest} [ms]
495	0.13	0.7	0.97	3	4.8	8

3.1.4 Simulation-based validation of analysis

Using a 400 Vdc, 40 kW dc power system similar to the one presented in Figure 3.2, we compare analytic estimates of peak current (i_{Fmax}) and safe time for contactor opening (t_s) with simulation results obtained using a more detailed system model developed in Mathworks Matlab/Simulink®. Moreover, a parametric study has been carried out since simulations provide a wide set of results for different system configurations. The power system under study is composed of four different types of sources each having a rated power of 20 kW. Each source is connected to the distribution bus through an electronic power converter. While a number of means for fault detection can be found in the literature, in our simulations we used a simple threshold-based scheme for detecting faults.

In the model, we use an R-L representation of the cable (since the capacitance of the cable is negligible compared to the capacitance of filters for a system smaller than roughly 10 km). We consider different values of output filter inductance and capacitance of the feeding converters, different number of converters connected to the distribution bus, and different system sizes (cable lengths). Loads are aggregated at the load centers to an equivalent resistance.

Table 3.3 shows the cable parameters for different lengths of the dc distribution bus, where *r* and *l* are the resistance and the inductance per unit length respectively [36]. Cables were sized by allowing a maximum voltage drop at rated load current of $\Delta V = 5\%$ for each of the two conductors. This leads to a constancy of the resistance component and a consistent increasing of the inductance component with increasing length of the cable.

TABLE 3.3

CABLE PARAMETERS

length [m]	section [mm^2]	ΔV [V]	r [Ohm/m]	l [mH/m]	R_{CB} [Ohm]	L_{CB} [mH]
50	6	5%	0.00371	0.000455183	0.1855	0.022759
70	10	5%	0.00224	0.000429718	0.1568	0.03008
100	16	5%	0.00141	0.000356507	0.141	0.035651
200	25	5%	0.000889	0.000337408	0.1778	0.067482
300	50	5%	0.000473	0.000321493	0.1419	0.096448
500	70	5%	0.000328	0.000307169	0.164	0.153585
1000	120	5%	0.000188	0.000298893	0.188	0.298893
1500	185	5%	0.000125	0.000236186	0.1875	0.354279
2000	240	5%	0.0000966	0.000239369	0.1932	0.478738

The length of the cable strongly influences the fault current behavior. The linear increase of L_{CB} with cable length causes the peak current to decrease with cable length and the current pulse duration to increase with cable length. Figure 3.5 shows the discharge current right after a fault for different lengths of the distribution line. Although a spatially large grid limits the peak magnitude of the fault current, the time for the first current peak to fall below the nominal current of a specific branch increases, and thus the time for a safe tripping of the contactor increases. However, even for large area grids (up to 2 km), the time for a safe tripping of contactors remains less than 4 ms.

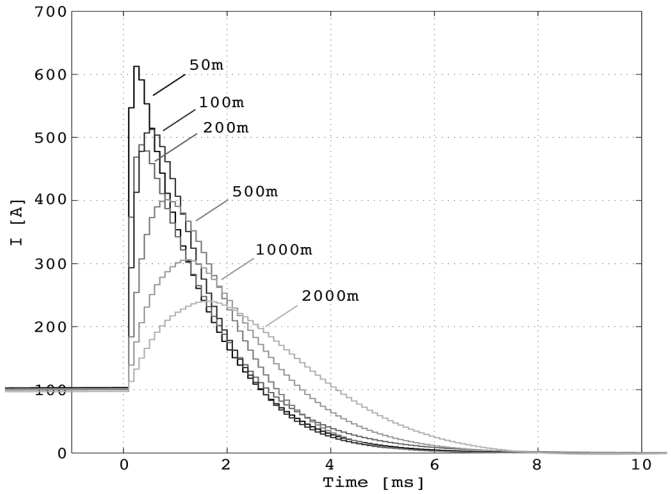

Figure 3.5 Fault current dependence on the length of the transmission line.

Considering a multisource power system of roughly 200-meter size, we tested the performance of the system for different values of system nominal voltage. Despite the fact that the first current peak increases with increasing system voltage, we can observe that after 2 to 4 ms, for each voltage level, the fault current falls to a value less than the nominal current of each branch connected to a load center.

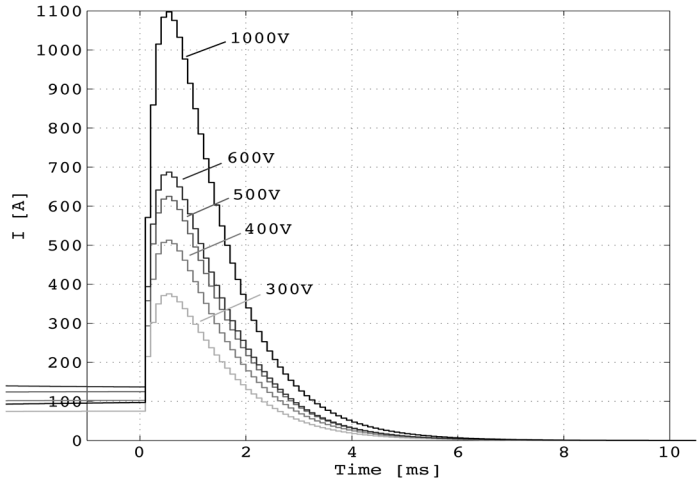

Figure 3.6 Fault current dependence on bus nominal voltage.

Figure 3.6 shows the behavior of the fault current for nominal voltages between 300 to 1000 Vdc at constant rated load power. Figure 3.7 shows the behavior of the fault current for nominal voltages between 1 kV to 10 kV at constant rated load power.

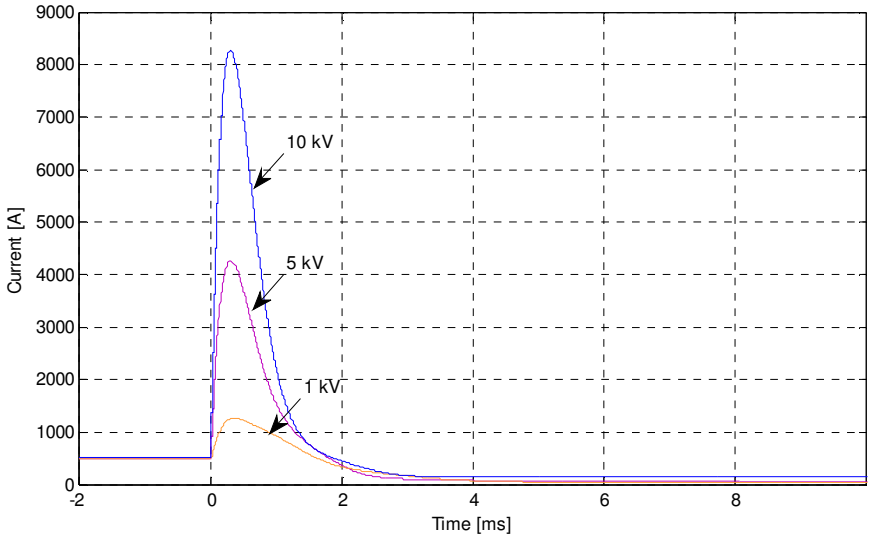

Figure 3.7 Fault current dependence on bus nominal voltage Medium Voltage range (1 kV to 10 kV).

Moreover, the current peak due to a short circuit fault is strongly influenced by the size of filter capacitance and inductance connected to the bus, and thus on the number of sources feeding the bus at the moment of the fault. Figure 3.8 illustrates the fault current dynamic for an increasing number of paralleled power sources, each of those connected through an electronic power converter. There is a linear relationship between the number of connected sources and the time to cross the appropriate value of the current at which the contactor should be opened. On the other hand, a bigger number of connected sources increases the re-energizing capability and the speed with which the bus and the storage elements can be re-excited.

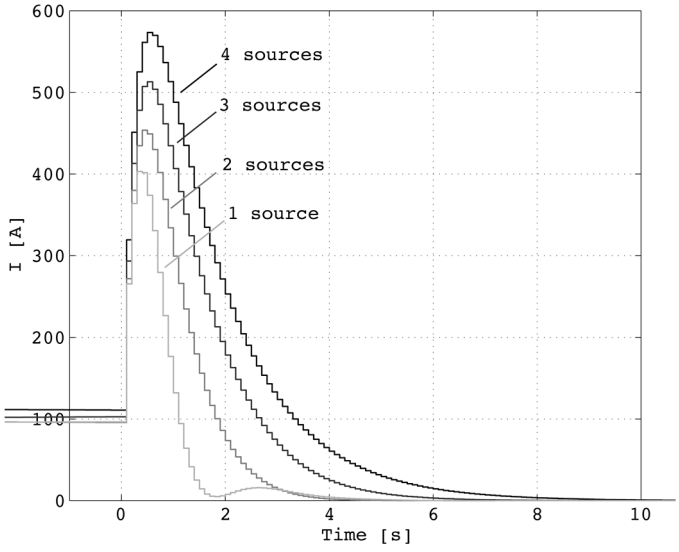

Figure 3.8 Fault current dependence on number of sources connected to the distribution bus.

3.2 PROTECTION SCHEME PERFORMANCE

Utilizing the dc power system simulation model presented in the previous section, we verified the performance of the protection method in terms of time for fault isolation and of duration of the voltage outage during a fault. At the same time we implemented the method of this paper in a scaled down dc zonal power distribution experimental setup and we compared simulation and experimental results. This comparison validates the system models, especially the current dynamic during a fault, contactor and arc dynamics, and the operation of the control that implements the protection method.

In simulations, dc-dc power converters are represented by switching models implemented with the natural port components of the SimPowerSystem™ library of Simulink®. The contactor was represented as an ideal switch in parallel with a constant voltage source (V_{ARC}) and a diode that activates the voltage source when the opening of the switch induces a forward current through the diode, as shown in Figure 3.9. As a first approximation this represents the arc voltage as a constant 100 V forward drop in the

direction of current flow. This ignores more complicated dependencies on arc current, electrode materials, or the existence of any particular arc extinguishing device [34], [35], [37], [38].

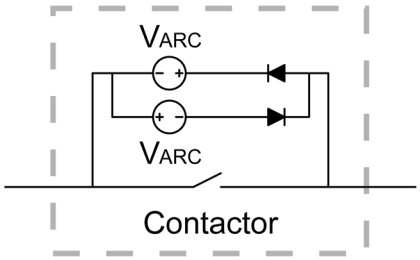

Figure 3.9 Contactor arc voltage model valid only during arcing phase.

Also, an operation delay of 3 ms accounts for the finite actuation time of the fast mechanical contactor, as consistent with the experimental study described in [39].

Simulations were validated by reference to a smaller-scale experiment. The simulation model having bus-side nominal ratings of 400 V, 80 A was scaled down by eight times in voltage and in current, thus 64 times in power, as shown in Figure 3.10.

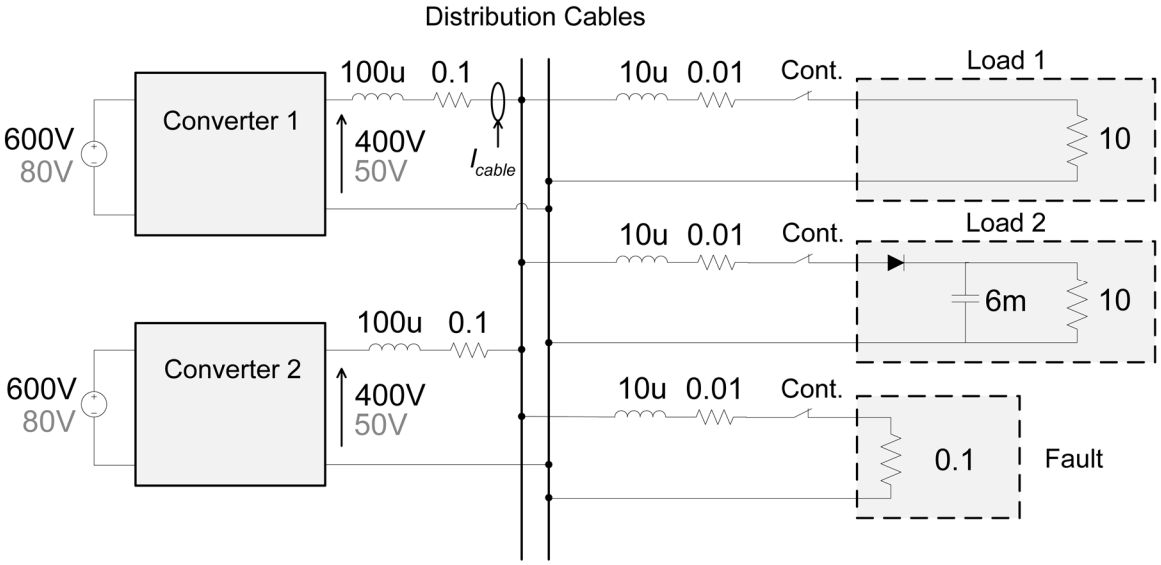

Figure 3.10 Circuit diagram of the system. Values in black are for the simulation system, and values in grey are for the scaled down experimental system.

Figure 3.10 illustrates the circuit diagram of the system for both simulation and experimental setup. PWM-type dc-dc converters feed the distribution cables, which are represented by R-L circuits. The distribution cables supply power to two loads and one of the loads has a clamping diode and a shunt hold-up capacitor on the upstream side, as illustrated in Figure 3.10. An adjustable fault resistance (0.05 to 1 Ohm) is also connected to the dc bus and it is driven by a power MOSFET with external command. Each load, or the load in the faulty branch in this specific picture, is connected to the bus through a *Kilovac Lev200* mechanical contactor [42]. A microcontroller board, current and voltage sensors are also part of the prototype. The power rating of the system is 1 kW, working at a bus voltage of 50 V. More details on the experimental setup can be found in Appendix A.

3.2.1 Comparison of simulation and experimental results

Our purpose here is to validate the operation of the protection technique through comparison between simulation and experimental results. In order to accomplish this comparison, we scaled back up the measurements coming from the scaled down experimental setup (x8). This operation gives us a very confident comparison except for small deviations due to the inherent voltage and current influence on the fault dynamics as shown in the analysis in Section 3.1.

The oscillograms of Figure 3.11 show the peak current when a short circuit fault happens on the dc bus at t = 0 s. The controller, implemented on a TI DSP microprocessor, detects the fault, turns off the converter by forcing the duty cycle to 0, and when the sensed current goes under the rated current of the mechanical contactor, the

DSP sends a tripping signal to isolate the faulted part of the system. As the contacts separate, an appreciable arc voltage forces the remaining fault current to 0 (t = 4.5 ms).

Figure 3.11 shows a favorable comparison between simulation and reduced-scale experiment for both the current on the distribution cable and the current through the filter inductance of a converter. The small differences between the traces can be attributed to several different factors, each acting at different times. These factors include discrepancies between marked sizes of capacitors or inductors and actual values, nonlinear effects of current on inductance values, or inconsistent opening time of the contactors. But in either case, we can observe that the fault is isolated within 5 ms.

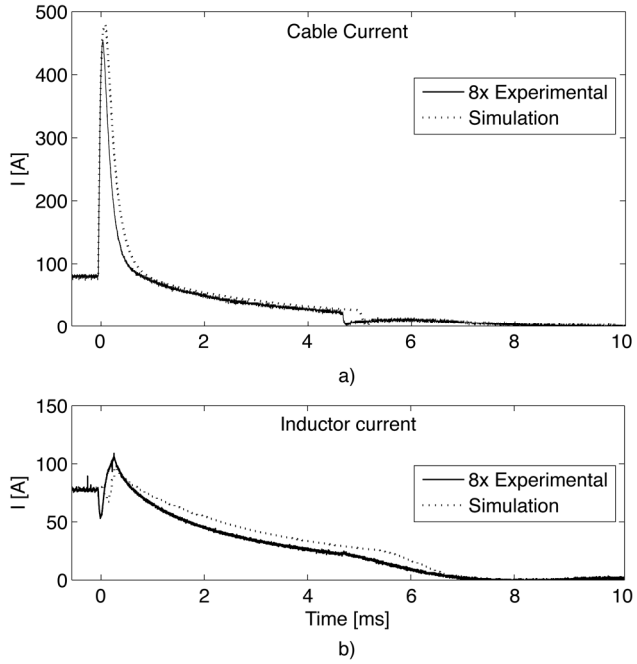

Figure 3.11 Fault detection, current limitation, and fault isolation by coordinated action of the power converter and the grid segmentizer switch, comparison between experimental and simulation results. In a) cable current Icable , and b) current of the filter indu

Table 3.4 compares several key characteristics as determined by analysis, simulation, and experiment, and the discrepancies between them. These results confirm that the derived mathematical expressions yield valid estimates of system characteristics. Finally,

hardware experiments confirm that both analysis and simulations are correct, and that assumptions and approximations are properly done.

TABLE 3.4

COMPARISON OF RESULTS FROM ANALYTICAL, SIMULATION AND EXPERIMENTAL ANALYSIS

	I_{MAX} [A]	t_{MAX} [ms]	t_{CN} [ms]	t_{ARC} [ms]	t_{MECH} [ms]	t_{EX} [ms]	t_{rest} [ms]
Analytical	495	0.12	1.0	0.97	3	4.8	8
Simulation	500	0.1	1.0	0.8	3	4.9	8.2
Experimental	453	0.1	0.9	0.6	3.2	4.8	7.9
error A-S	-1%	20%	0%	18%	0%	-2%	1.3%
error E-S	10%	0%	10%	25%	-6%	2%	3.6%

After the fault current is extinguished and the fault is isolated, the converters turn back on, the bus is re-energized, and loads resume to normal operation. Figure 3.12 shows the rest of this sequence, which was not shown in Figure 3.11.

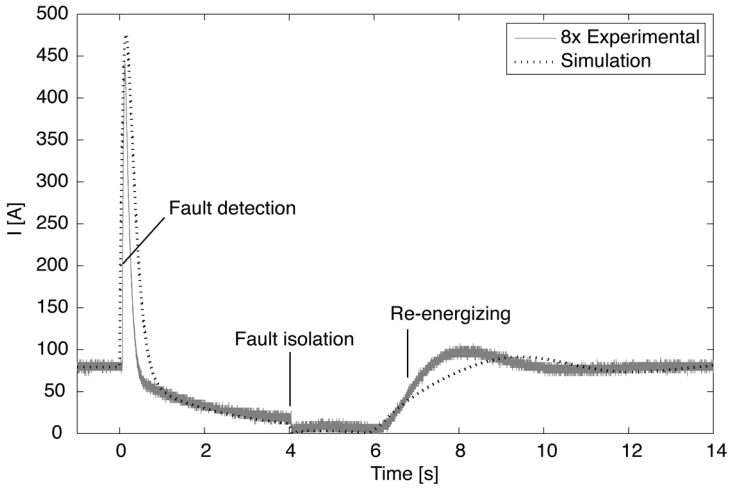

Figure 3.12 Fault isolation and re-energizing of the dc bus after a fault

Figure 3.13 illustrates the ride-through capability for a load powered via a diode-clamped hold-up capacitor. Even though the bus voltage collapses momentarily after the

fault, the load hold-up capacitor continues to supply power until the bus voltage returns to normal. The grey line represents the voltage on the main bus and on loads without hold-up capacitors (V_{Load1} in Figure 3.10), and the black line shows the behavior of the voltage on a load with a hold-up capacitor installed and isolated by a diode (V_{Load2} in Figure 3.10). The measured results match the simulation results with an error less than 5%.

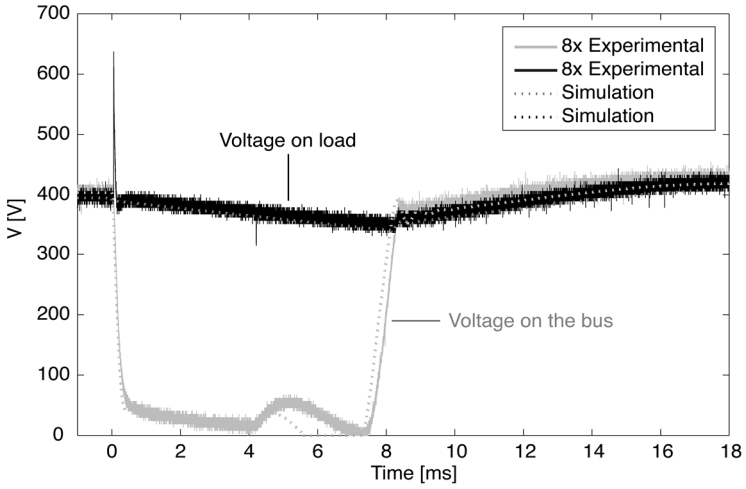

Figure 3.13 Bus voltage collapses momentarily after a fault, but load is sustained by a diode-clamped hold-up capacitor.

The diode-clamped load hold-up capacitor is essential for uninterruptable loads. Equation (22) defines the minimum size of the hold-up capacitor in order to provide power to the load for a voltage outage of duration t_{out} and assuming that the load can operate down to 70% of the nominal supply voltage [40].

$$C_{hold-up} = \frac{2P_{load}t_{out}}{V_n^2(1-0.7)} \tag{22}$$

where V_n is the nominal voltage of the dc bus, P_{load} is the power request of the load at that load center, and t_{out} is the out-of-service time estimated through analysis of the system parameters or equation (23).

$$t_{out} = t_{ex}\left(1 - \frac{I_n}{I_{overload}}\right) \tag{23}$$

where t_{ex} is the time to extinguish a fault, I_n is the combined nominal current of the source converters, and $I_{overload}$ is the overload capability of the source converters. The 0.7 coefficient takes into account minimum operating voltage of the load (70% of the nominal supply voltage), and thus the energy that can be removed from the hold-up capacitor during the momentary bus outage. If it is necessary to withstand longer outages, it would obviously be necessary to increase the size of the hold-up capacitors.

3.2.2 Contactor operating time

The time needed to completely isolate the fault depends on the operating speed of the contactor. Contactor operation times range from a few milliseconds for solid state or hybrid contactors to about ten milliseconds for off-the-shelf mechanical contactors. Despite the fact that solid state solutions provide very high opening speed, they still need some sort of mechanical contacts for physical isolation of the faulted zone [41]-[43]. Figure 3.14 shows a comparison between different types of contactors and their opening times.

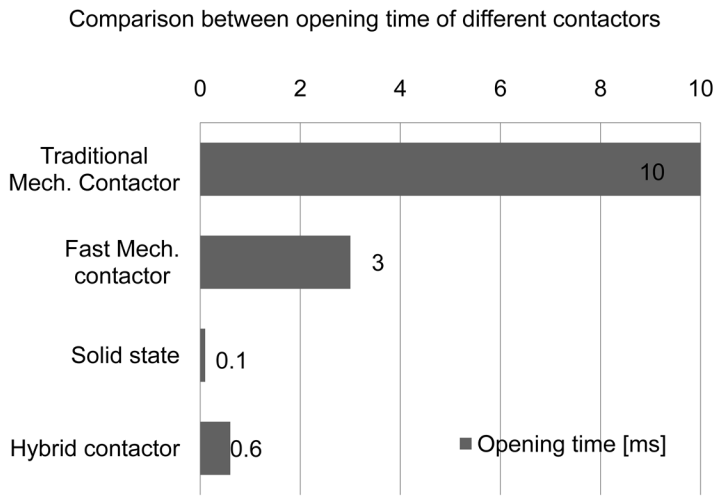

Figure 3.14 Opening time for different kind of contactors.

Figure 3.15 illustrates how the sum of time components de-energizing time before contactor opening (t_{cn}), fault elimination time (t_{ex}), and power restoration time (t_{rest}), defined by equations (14), (20), and (21) aggregate to define the total time to power restoration after a fault.

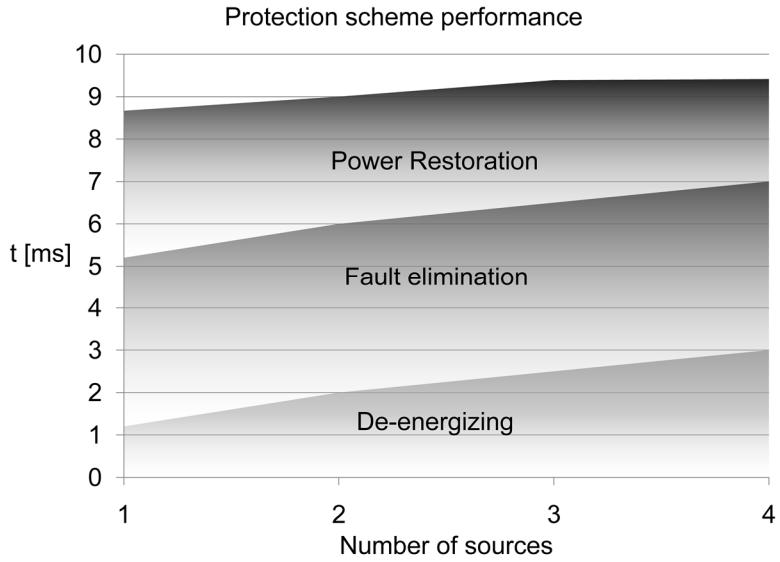

Figure 3.15 Total power restoration time and duration of the three components of the fault protection process.

It is essential to choose fast mechanical contactors in cases where the system should be protected and reconfigured within 10 ms. Slower mechanical contactors might be suitable for larger-area distribution systems, systems where power continuity to loads is not essential, or systems where larger hold-up capacitors are acceptable to supply non-interruptible loads.

3.2.3 Power quality

The short out of service time provided by this technique allows very short power interruptions that fall within allowable power quality requirements. Figure 3.16 shows the design characteristics of common AC loads and load voltage tolerance for DC distribution systems.

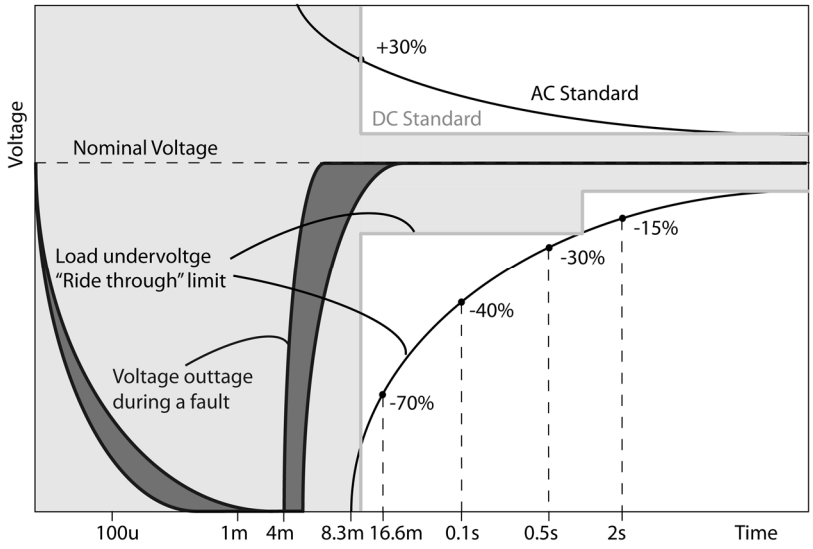

Figure 3.16 Envelope of expected operation of the protection method (dark band). Outages are sufficiently brief that they fall within the acceptable voltage envelope according to CBEMA and IEEE standards on power quality.

The black line shows the limit for a voltage variation to affect the load performance in a traditional ac system (AC standard), and the light gray zone (DC standard) identifies the

boundaries of voltage sag and overvoltage for the operation of DC loads [32], [40]. The black lines labeled “Voltage outage during a fault” represent the range of voltage outage durations when the system is protected with the method described here. We can observe the variation range of the duration of voltage outages (dark gray area). The shorter duration is for a system with short distribution lines and few sources connected to the dc bus; the longer duration is for a system with longer distribution lines or a higher number of sources connected at the moment of the short circuit fault.

SUMMARY

In this chapter, we have shown that the combination of power converters and bus tie switches can protect and reconfigure a DC distribution bus in response to short circuit faults. Results of our study show that it is possible to depower the bus, eliminate the fault, and then re-energize the bus faster than an AC grid can be protected and reconfigured using traditional circuit breakers, and fast enough to remain within power quality requirements according to IEEE standards [40].

Effective fault detection and reliable coordination of power converters and mechanical switches are fundamental in order for the presented protection method to isolate the smallest section of the system after a fault. The next chapter illustrates a short-circuit fault detection method that coordinates power converters and bus tie switches in order to provide a fast and reliable isolation of faults.

CHAPTER 4

FAULT DETECTION IN MULTI-TERMINAL MVDC DISTRIBUTION SYSTEMS

Fault detection and coordination of the protection devices is a fundamental aspect of fault current limitation and fault isolation. In this chapter we developed a new method that uses the time evolution of apparent resistance as the characteristic that provides a fast and effective method for detecting and identifying short circuit faults in medium voltage DC power distribution systems. This method allows source converters, bus tie switches, and mechanical contactors to use only local measurements when discerning whether or not to trip into fault isolation mode. We first provide a comparison with other fault detection techniques and we explain the challenges of fault detection in multi-terminal DC distribution systems. Then we explore the theoretical aspects of the developed fault detection method. Finally, we validate the method through simulation and experimental results and we define the boundaries of effectiveness depending on system parameters.

4.1 APPARENT EQUIVALENT RESISTANCE MEASUREMENT FOR FAULT DETECTION

Figure 4.1 shows a ring configuration for a MVDC distribution system in which multiple sources are connected to a ring bus. In this configuration power can flow in any direction and switches that tie separate buses together must open against full bus voltage and current in order to break the ring into segments.

This multi-terminal dc power distribution system comprises a variety of power sources and energy stores, all connected to the distribution bus through controllable (and often bi-directional) electronic power converters [49].

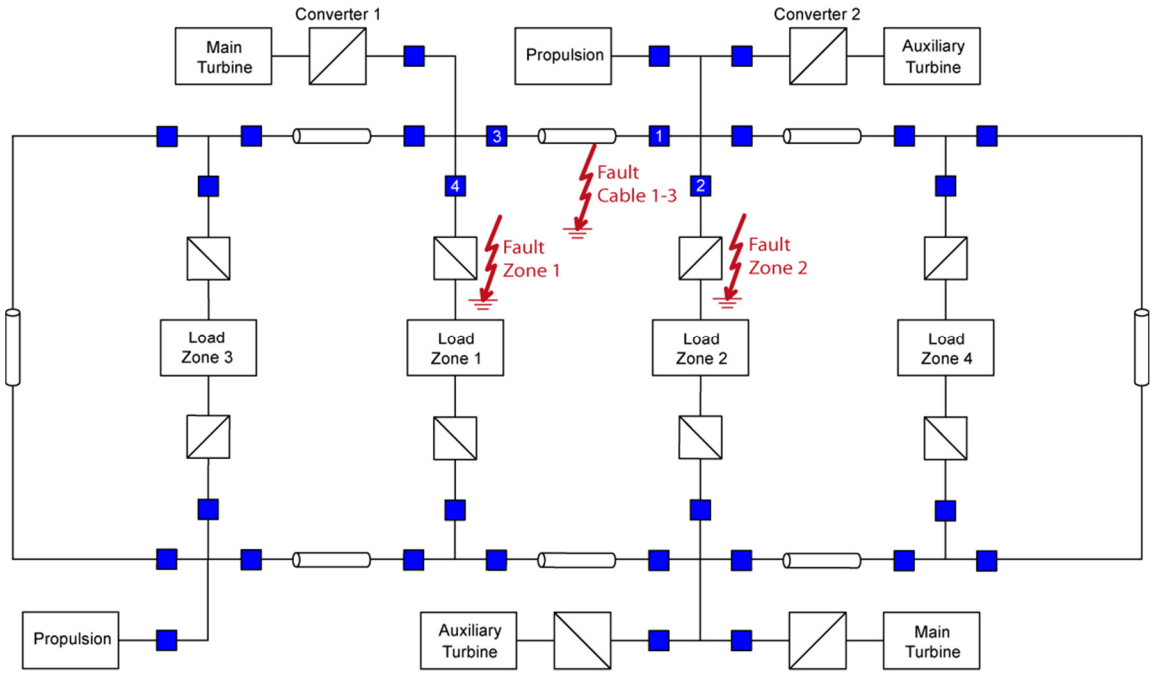

Figure 4.1 Multi-terminal zonal MVDC distribution system. The blue squares are mechanical contactors. They can be either contactors or no-load bus tie switches and they are not required to open on sustained fault current like circuit breakers.

Time domain measurement of only the voltage-current ratio entails minimal computational burden and is thus suitable for fast fault detection [49], [61] - [63]. Figure 4.2 shows the equivalent circuit of a section of the multi-terminal zonal MVDC distribution system during a short circuit fault condition close to load zone 2. Loads are represented by an equivalent resistance R_L, C_h are the hold-up capacitors in each load zone. These capacitors are interfaced to the bus through a diode and they can serve as short term local storage for sensitive loads as shown in Chapter 3. R_{Cable} and L_{Cable} are resistance and inductance parameters of each section of the power distribution bus cable, R_F represents the equivalent resistance of the short circuit fault. Converters 1 and 2 are

each represented as controlled voltage sources V_o and the output filter inductances L_{out} and having output capacitances C_{out}. S1 to S6 are the contactors or bus tie switches at which terminals we measure voltage and current as well as for Converter 1 and 2.

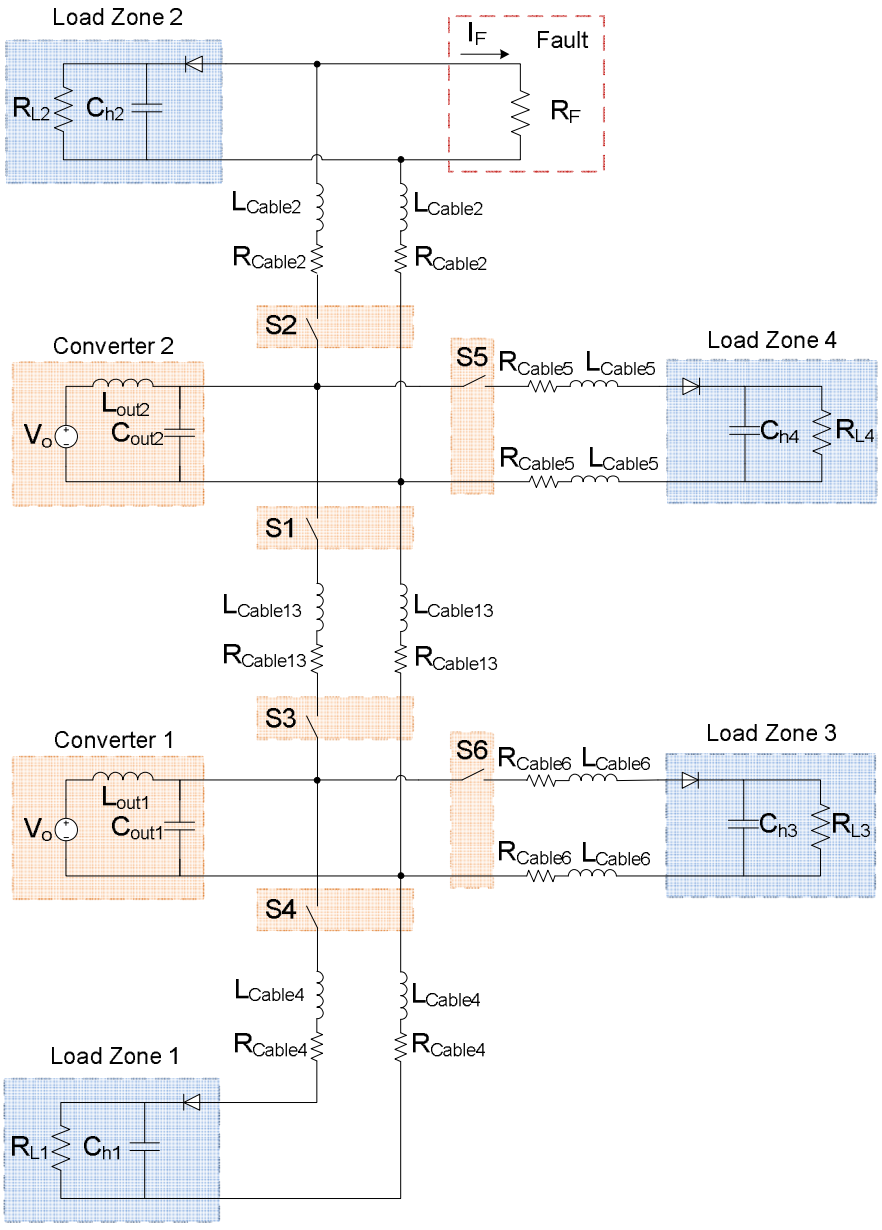

Figure 4.2 Equivalent circuit of a section of the multi-terminal zonal MVDC distribution system during a short circuit fault condition. Measurements of voltage and current are taken at the terminals of both converters 1 and 2, and of the contactors S1 to S6.

Considering a fault close to Load Zone 2 and taking into account the measurement of voltage and current at the terminals of Converter 2, we can define the equivalent impedance $Z_{eq}(s)$ as the parallel of the faulted path with the n load paths connected to Converter 2 as in (23):

$$Z_{eq}(s) = \frac{1}{\frac{1}{R_{cable}+R_F+sL_{cable}}+\sum_{i=1}^{n}\frac{1}{R_L+\left(R_{cable\_i}+sL_{cable\_i}\right)}} \tag{23}$$

Assuming that the fault resistance has a much smaller impedance than the parallel combination of the load paths at low frequencies (24), the faulted path impedance dominates in the definition of the equivalent impedance and thus we can neglect the contribution of the load paths as in (25):

$$R_{cable} + R_F + sL_{cable} \ll \frac{1}{\sum_{i=1}^{n}\frac{1}{R_L+\left(R_{cable\_i}+sL_{cable\_i}\right)}} \tag{24}$$

$$Z_{eq} = R_{cable} + R_F + sL_{cable} \tag{25}$$

Figure 4.3 illustrates the reduced model of the equivalent impedance seen at the terminals of the device (Converter n) when the bus is affected by a short circuit. If we consider that the inductive component of this impedance can be noticed only at high frequency, we can neglect the influence of the cable inductance at low frequency. This leads the voltage-current ratio to be equal to the equivalent resistance seen at the terminal of the device, as shown in (26).

$$R(t) = \frac{V_n(t)}{I_n(t)} = R_{cable} + R_F \tag{26}$$

Figure 4.4 shows the validity of the approximation given in (25). The bode plot of the broad spectrum impedance shows the comparison between the simplified impedance Z_{eq} in equation (25) and the parallel of all the impedances connected to the measurement point given by equation (23).

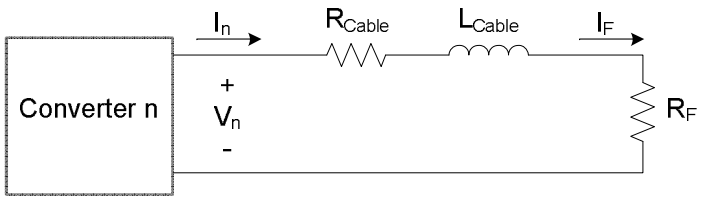

Figure 4.3 Equivalent circuit at the terminals of converter *n* when the distribution bus is affected by a short circuit fault.

The parameters of the cable start affecting the impedance above about 200Hz (within 5ms) and become relevant above 1kHz (within 1ms).

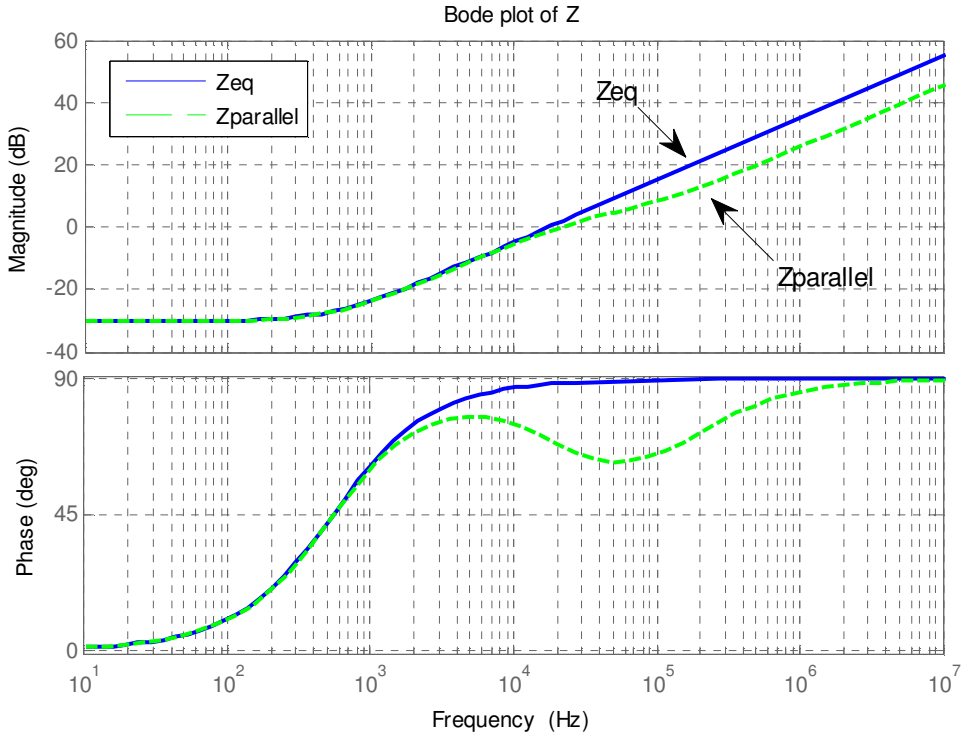

Figure 4.4 Comparison between the simplified impedance Zeq in equation (25) and the parallel of all the impedances connected to the measurement point Zparallel given by equation (23).

Being that the equivalent resistance between the device (e.g. converter *n* in Figure 4.2) and the fault is different from one device to another, this allows a protection algorithm to differentiate between faults close to or far from the device and take appropriate action.

4.2 FAULT DETECTION ALGORITHM

Each converter is equipped with a controller that is capable of measuring current and voltage, and calculating the value of the equivalent resistance at the output terminals at each sample time from the relationship in (27):

$$R_n(t) = \frac{V_n(t)}{I_n(t)} \tag{27}$$

Where V_n and I_n are the values of voltage and current after filtering and discretizing, and R_n is the calculated equivalent resistance at the terminals of device n. The measurement is then used by the controller decision algorithm that gives to the converter a current limiting reference or an enabling signal, as shown in Figure 4.5. In fact, when the converter recognizes an equivalent resistance lower than a pre-defined threshold, it goes into current limiting mode bringing the current down to a minimum value. The converter stays in current limiting mode until the equivalent resistance returns above a pre-defined threshold after a pre-defined time delay (*Delay_Setup* in Figure 4.5). In this way the hysteresis of the algorithm avoids oscillations between fault and non-fault conditions. The resistive threshold for fault detection R_{th} has to be smaller than the equivalent resistance corresponding to the heaviest load that the system is designed to accept (system rated load), as shown in (28), where V_r is the rated voltage and P_r is the rated power of the system. In the case study that we analyze, we chose a resistive threshold corresponding to double the rated power of the system since it gives a 100% margin between normal operation conditions and fault conditions. The minimum current value can be chosen to be as small as the power converter can permit, but enough to allow the measurements at the terminals of contactors. For example, the value that we

chose for the experiments was 1 A, which corresponds to 5% of the nominal rated current of our low-power testbed.

$$R_{th} < \frac{V_r^2}{P_r} \tag{28}$$

A similar fault detection algorithm is present in the controller of each contactor that segments the dc bus and each contactor between dc bus and loads as shown in Figure 4.1.In this case, the decision-making algorithm has multiple statuses due to the fact that contactors in different locations have different priorities for opening, and each contactor is allowed to open when the current value falls below its own rated safe opening current. Since the contactor is not designed to open the prospective maximum fault current (as a circuit breaker would), each contactor is allowed to open only after the current falls below its rated opening current. In these conditions the contactors can open the remaining current without damage. The complete algorithm is illustrated in Figure 4.6. Whereas for converters the threshold of the resistance is set to a value described by (28), for contactors the threshold varies with time after exceeding a trigger value, together with a current direction condition ($I > 0$) that allows contactors connected at the same node (e.g. Contactor S1 and S2) to distinguish between different directions of the fault current.

Figure 4.7 illustrates the resistance-time trip characteristic for contactors that tie the main distribution bus. When the measured equivalent resistance falls below the threshold for some defined time after the alarm condition, and the current is positive, the contactor is responsible for opening. This time interval can be determined by the distribution bus time constant and by the control bandwidth of the connected power converters as shown in the previous analysis in Chapter 3.

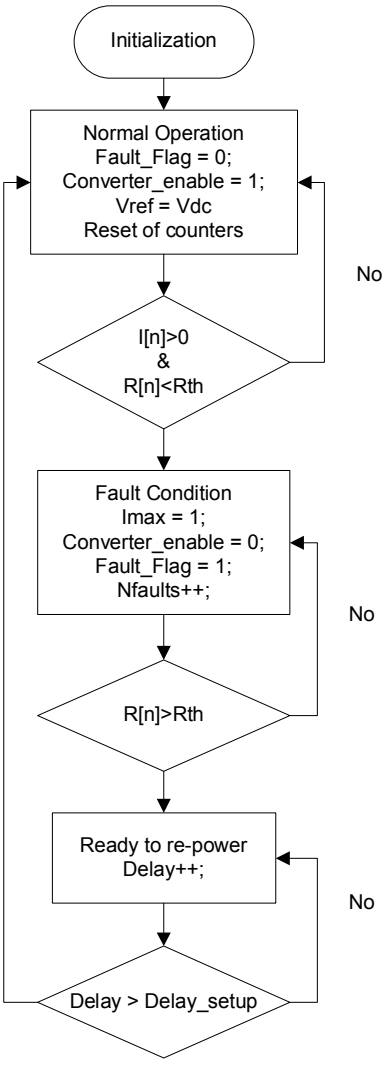

Figure 4.5 Fault detection algorithm at each converter

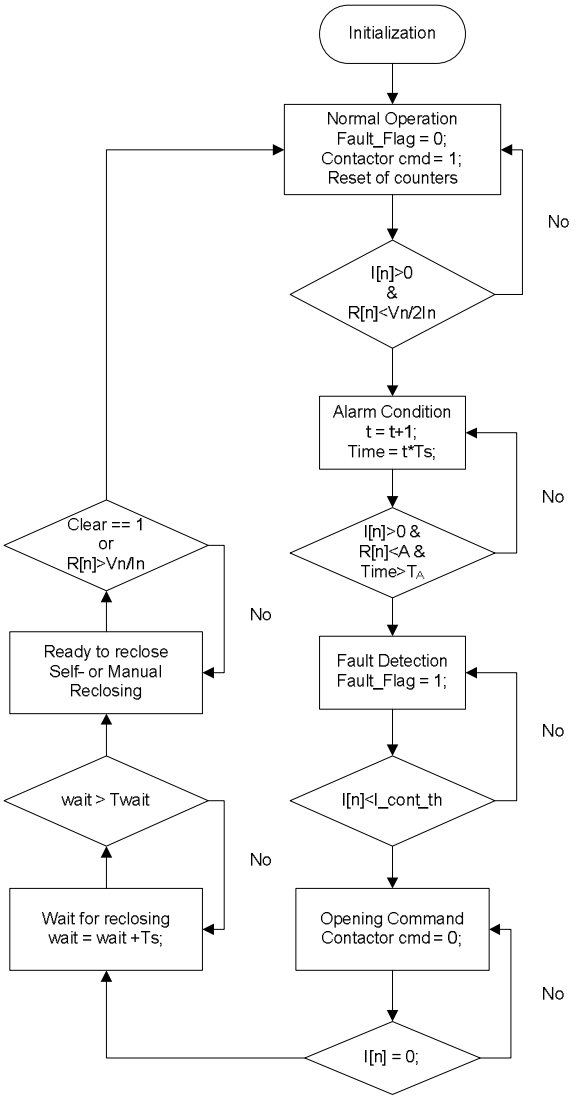

Figure 4.6 Fault detection algorithm at each contactor

In the case of contactors that connect load zones to the main distribution bus, the contactor can trip within a shorter period of time if the fault is close to the contactor. Another difference between contactors that follow the characteristic of Figure 4.7 is that the main bus contactors have an additional tripping delay to give priority of opening to the contactors that interface the loads in order to provide higher robustness of power continuity. In case of regenerative loads, these have to be considered as power sources

since they can contribute to the fault current. In this case contactors between regenerative loads and the main bus have the same tripping curve as bus contactors. Figure 4.8 illustrates how the resistive thresholds can be selected for each contactor. Considering contactor 1 in Figure 4.8, we can observe that threshold A has to be smaller than the resistance of section 1-2 ($R_{1\text{-}2}$), threshold B has to be smaller than the resistance of section 1-3 ($R_{1\text{-}3}$), and so on. The fact that the thresholds A, B, C, … have to be smaller than some percentage of the resistance of the corresponding section of the bus assures selectivity between different contactors. In this way contactor 1 provides primary protection for a fault on section 1-2, and backup protection for faults on sections 2-3, 3-4, etc. In order to provide selectivity and redundancy between contactors the time interval between one threshold and the next threshold can be defined depending on the time constant of the distribution bus and on the opening speed of the segmentizing contactors. In the case tested in the lab, we used contactors with opening time of about 3 ms and we choose the length of the time intervals between one resistive threshold and the other to be 10 ms, as can be seen in Figure 4.7. The time intervals can be chosen depending on the time constant of the distribution system and the opening time of contactors (In the case tested 0.5 ms and 3 ms respectively). This means that time intervals will be longer for systems having a longer time constant and longer opening time of contactors. Of course, the same process can be applied to any contactor and for different bus configurations. As we can see from Figure 4.7, the margin between the resistance of one bus section and the corresponding resistive threshold has been chosen to be 20% of the resistance of each section of the distribution bus (red area).

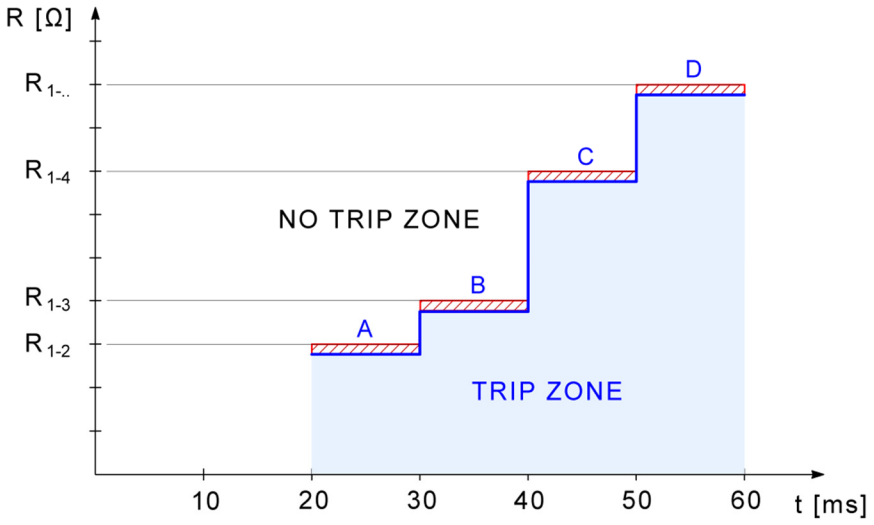

Figure 4.7 Resistance-time trip characteristic for contactors that tie the main distribution bus

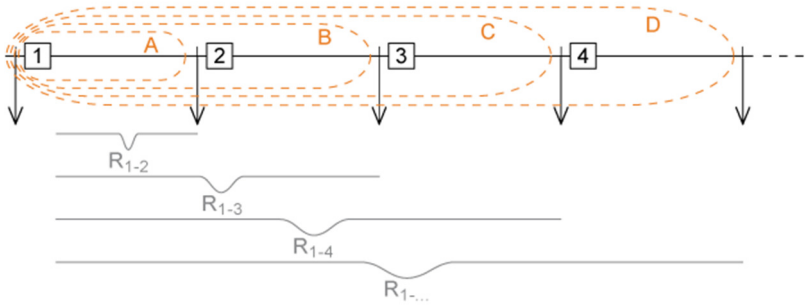

Figure 4.8 Main distribution bus resistive threshold and cable resistance of each section of the bus

On top of guaranteeing selectivity, the margin between the resistance of one section of the bus and the resistive threshold for fault detection determines the maximum error allowable in measurement of the apparent resistance. Since the measurement error has to be smaller than this margin (20%), this determines the accuracy of the measurement devices. Whereas for the case of a symmetrical distribution bus with sections of the same length and parameters, in the case of an asymmetrical distribution bus maximum allowable error can vary. Table 4.1 gives a reference on the error variation depending on

how different are the sections of the distribution bus. R_{min} and R_{MAX} represent the resistances of the shortest and longest sections, respectively.

TABLE 4.1

ERROR VARIATION DEPENDING ON THE ASYMMETRY OF THE BUS

R_{min} / R_{MAX}	*Allowed Measurement Error [%]*
1	3%
0.5	1.5%
0.2	0.6%
0.1	0.3%
0.05	0.15%

Cable resistance introduces another limitation on the resistance measurement for the distinction of faults in different sections. Of course cable resistance depends on the design constraints for power flow. In fact, in order to have a low voltage drop on the cables and to respect the ampacity constraints of cables, the sectional area of cables at the MW level becomes big and the resistance becomes small. This means that for cable sections having a very small resistance compared to the expected fault resistance the accuracy requirements for the measurement device can be too high and they can lead to excessive costs. Equation (29) gives a good indication of the limitation of the detection method depending on the measurement accuracy of the devices, the rated voltage V_r, and the rated power P_r of the system.

$$R_{min} > Measurement\ Accuracy \cdot \frac{V_r^2}{P_r} \tag{29}$$

Both in case of very small cable resistance and in case of high resistance faults the resistance measurement provides a reliable means for power converters to detect the existence of faults, but it might not be reliable to distinguish locations of faults. If this is a

critical concern, we recommend to combine this method with a differential current measurement that can provide a more accurate fault detection with the help of communication between protection devices.

4.3 SIMULATION-BASED VALIDATION OF THE FAULT DETECTION METHOD

Simulations confirm that that the fault detection method is effective for a wide range of operating conditions and scenarios. Figure 4.9 illustrates a representative section of a representative multi-terminal MVDC system. This representative section allows us to consider all the relevant scenarios. The MVDC system under study operates at a rated voltage of 5 kV and a rated power of 40 MW, with two power sources interfaced to the dc bus through controllable power converters. In the model, we use an R-L representation of the cable, according to the assumptions in Appendix B, with parameters shown in Table 4.2 for typical cable length [48], [54].

TABLE 4.2

CABLE PARAMETERS

length [m]	*section* [mm^2]	ΔV [%]	*r* [Ohm/km]	*l* [mH/km]	R_{Cable} [Ohm]	L_{Cable} [mH]
5	223	0.7%	0.426	0.183	0.0043	0.0018
10	223	1.4%	0.426	0.183	0.0085	0.0037
25	223	3%	0.426	0.183	0.0213	0.0092
50	223	6%	0.426	0.183	0.0426	0.0183

Figure 4.10 shows voltage and current on the main power bus at the points where Converter 1 and Converter 2 connect to the bus as the system operates through several power and fault incidents.

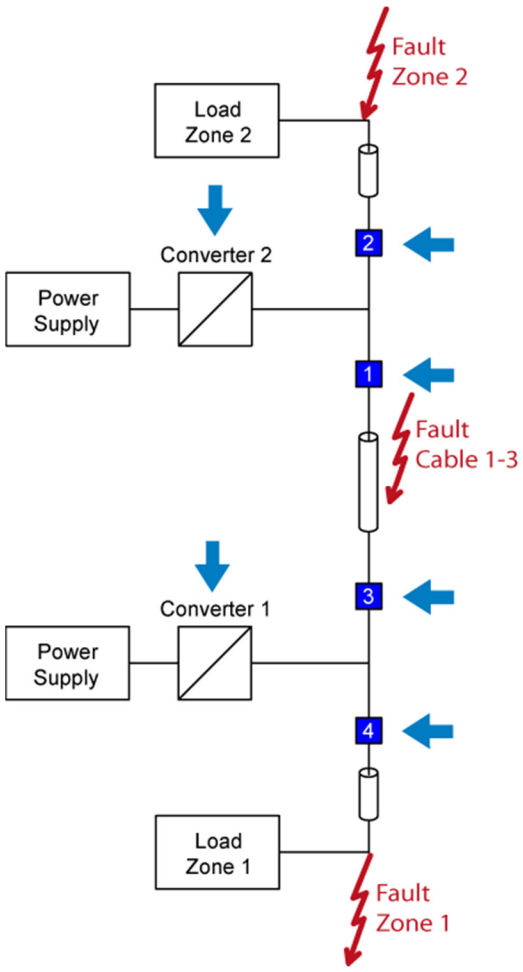

Figure 4.9 Section of the systems explored in simulation. Typical fault locations are highlighted. The arrows point to the devices that have local measurement of current and voltage.

As we can notice, fault currents can be very similar to load currents. The several incidents include a step increase of load power at t = 0.05 s, connection of a capacitive load at t = 0.15 s, a step increase of a constant power load at t = 0.22 s, and onset of short circuit faults at t = 0.3 s and t = 0.5 s. Whereas it is difficult to distinguish these events based on their currents, the equivalent resistance measured at the terminals of the two feeding converters (Figure 4.11) shows a clear distinction between fault conditions and normal operations. Once the fault current reaches steady state – after t = 0.3 s and t = 0.5 s – the value of the equivalent resistance measurement matches the value of the

sum of the cable resistance between the device and the fault and the equivalent fault resistance.

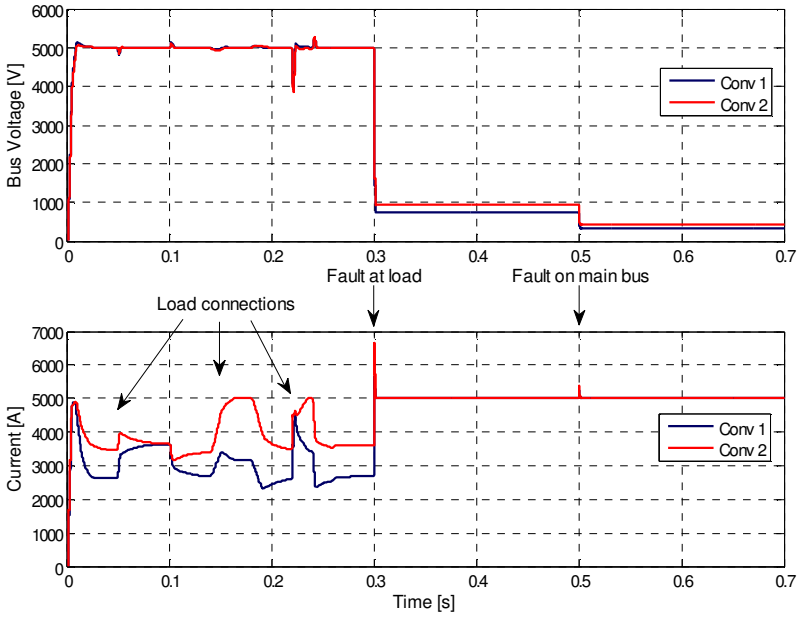

Figure 4.10 Voltage and current on the main bus during a short circuit fault close to the load (t = 0.3 s) and during a fault on the main bus (t = 0.5 s).

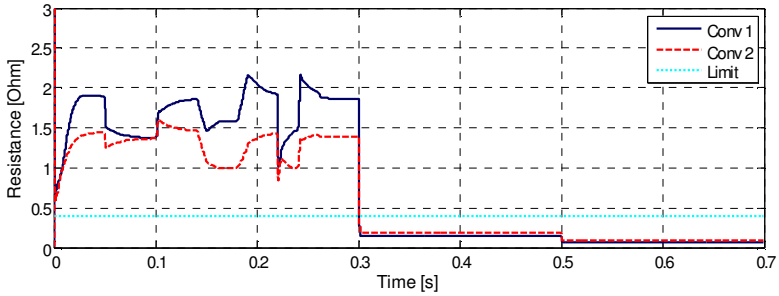

Figure 4.11 Equivalent resistance at the terminals of Converter1 and 2 during a fault close to the load (t = 0.3 s) and on the main bus (t = 0.5 s).

By utilizing the measurement of the equivalent resistance at the terminals of both power converters and segmentizing contactors we can distinguish short circuit faults so that the system can be protected from damage. On top of that, the measurement of resistance allows the contactors to discriminate whether or not to open so that they can

isolate the faulted section of the system. Figure 4.12 shows voltage and current on the main power bus at the points where Converter 1 and Converter 2 are connected to the bus. Both in the case of a fault close to one of the loads (Fault Zone 2 at t = 0.3 s) and in the case of a fault on the main bus (Fault Cable 1-3 at t = 0.5 s) the converters are briefly de-energized, then re-energized as soon as the faulted part of the system is isolated. At load connections (t = 0.05 s, 0.15 s, 0.23 s) the protection does not trip as it would if a current gradient detection scheme had instead been used.

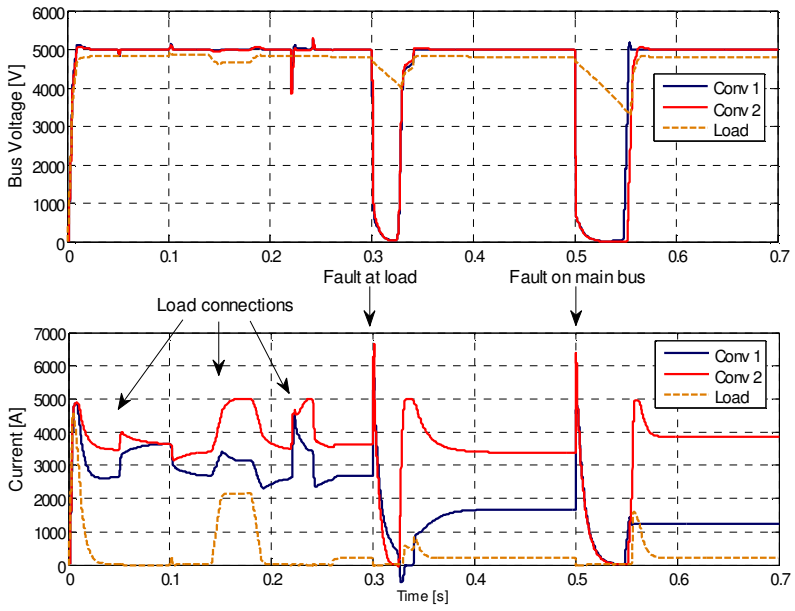

Figure 4.12 Voltage and current on the main bus during a short circuit fault close to the load (t = 0.3 s to t = 0.34 s) and during a fault on the main bus (t = 0.5 s to t = 0.56 s).

Figure 4.13 illustrates the equivalent resistance measured at the output terminals of the feeding converters. When the resistance drops below a certain limit (e.g. $R_n < V_n/2I_n$) the converters trip into current limiting mode so that they can de-energize the distribution bus. Figure 4.14 summarizes the decision making process of each contactor (Contactor 1, 2, 3, 4 in Figure 4.9) by plotting the equivalent resistances (R1 to R4 at the terminals of the respective contactors). In the case of the fault in Fault Zone 2 at time t = 0.3 s, only

resistance R2 measured by contactor 2 crosses the resistance-time tripping curve. Contactor 1, 3, 4 (R1, 3, 4) measure a bigger resistance since the fault is farther than in the case of Contactor 2. In the case of a fault on Cable 1-3 at time t = 0.5 s, both Contactor 1 and 3 (R1, R3) cross the tripping curve whereas Contactor 4 is not affected.

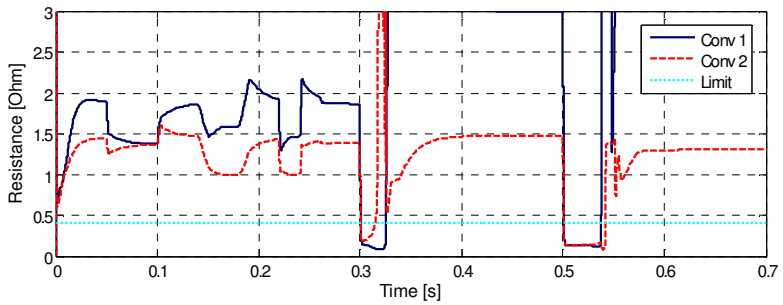

Figure 4.13 Equivalent resistance at the terminals of Converter1 and 2 during a short circuit fault close to the load (t = 0.3 s to t = 0.34 s) and during a fault on the main bus (t = 0.5 s to t = 0.56 s).

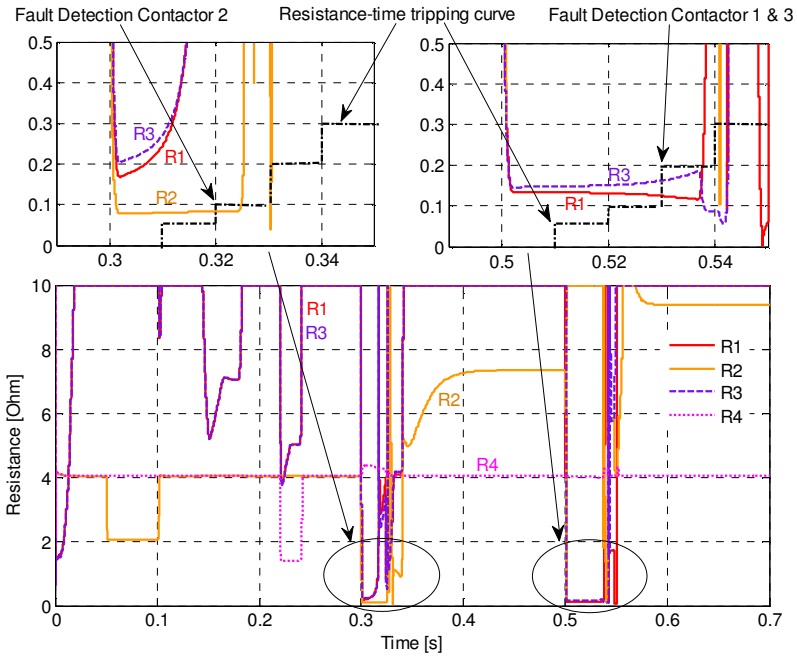

Figure 4.14 Equivalent resistance at the terminals of the contactors (R1, 2, 3, 4). For a fault in Fault Zone 2 only contactor 2 (R2) trips, and for a fault in Fault Cable 1-3 only contactor 1 and 3 (R1 & R3) trip.

These simulation results demonstrate that our proposed detection method using time-to-trip curves as a function of apparent circuit resistance properly coordinates the feeding power converters with the main bus tie contactors, and with the load zone contactors to quickly and efficiently protect the system against short circuit faults. As shown in Figure 4.12, the fault was detected and isolated within 10 to 20 ms and the distribution bus was re-energized within 40 to 60 ms. The sampling time of the data observer of each component is 50 μs for both Simulink simulations and for the digital microcontroller used in the experiments illustrated in the next section. The reliability and the boundaries of operation of this detection method are explored in Section 4.5 for different system parameters and accuracy of the measurements.

4.4 LVDC EXPERIMENTAL VALIDATION

In this section we present experimental results obtained from a dc test bed that is approximately $1/50^{th}$ the current and voltage of the expected MVDC power distribution system. Using the same system configuration as in Figure 4.9, the test bed system operates at a rated voltage of 100 V and a rated power of 4 kW. Cable sections of the dc bus were chosen in order to match the lumped resistance and inductance values of the cable in the MVDC simulation, as in Table 4.2.

Figure 4.15 illustrates the current sensed by contactors 1 through 4 in Figure 4.9 during a fault in Load Zone 2. When the fault is detected (t = 0.003 s) the converters trip in current limitation and the bus is de-energized. Once contactor 2 decides to open (t = 0.014 s), the faulted part of the system is isolated and the bus can be re-energized (t = 0.026 s).

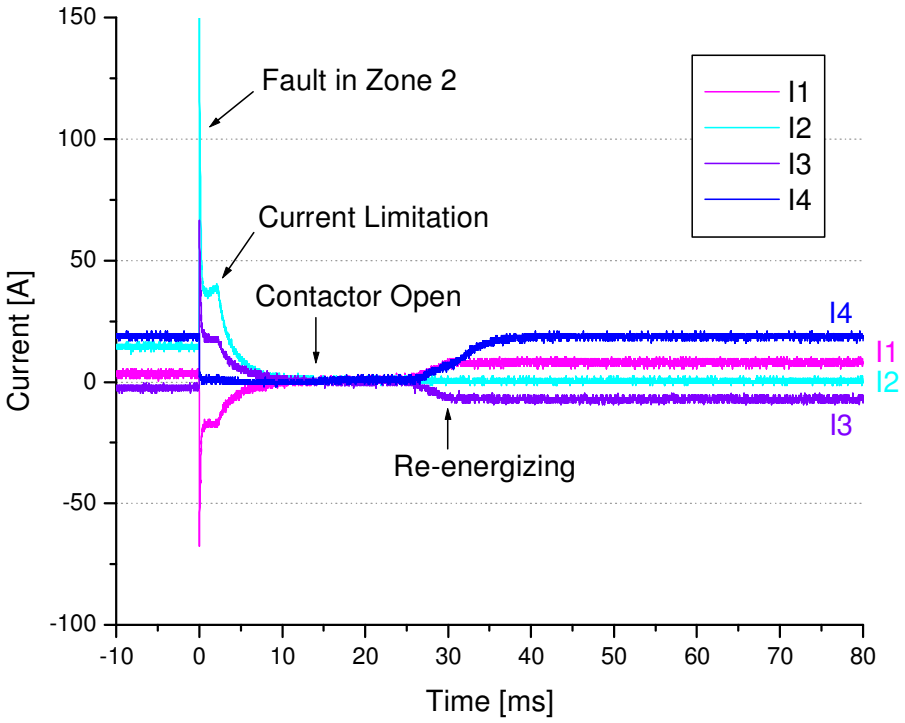

Figure 4.15 Currents sensed by contactors 1 to 4 during a short circuit fault close to one of the loads. The fault was detected (t = 0 s) and the system was reconfigured (t = 0.014 s).

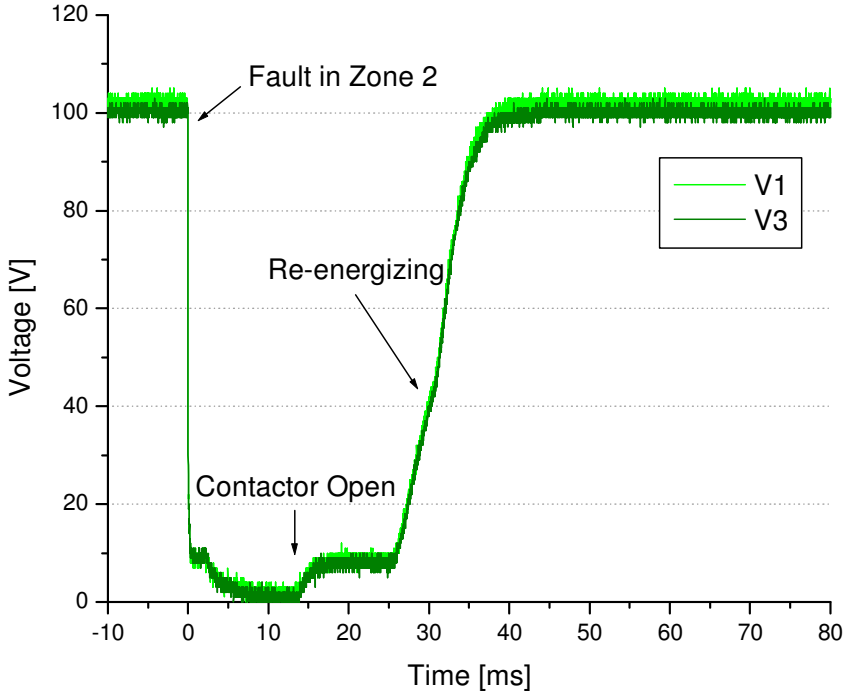

Figure 4.16 Voltage sensed at two different points (at the terminals of contactors 1 and 3) of the main distribution bus. The fault was detected (t = 0.003 s) and the system was reconfigured (t = 0.014 s).

Figure 4.16 shows the voltage sag during the same fault on the main dc distribution bus measured at the terminals of the two feeding converters. At time t = 0 the voltage on the bus collapses immediately when the fault happens. The voltage remains at about 10 V for about 3 ms before the converter goes in fault protection mode and it limits the current to the predetermined residual value de-energizing the bus. As soon as the faulted section of the system is isolated, the bus is re-energized.

Figure 4.17 compares the apparent resistance calculated at the terminals of contactors 1 through 4. It also shows that contactor 2 is the only one that opens after a fault in Zone 2 because the apparent resistance measured at its terminals (R2) crosses the apparent resistance-time tripping characteristic (dashed line). In this example all the contactors have the same tripping curve. In the case of asymmetrical distribution bus, each contactor measurement is compared with its own tripping curve. The fault is detected when the resistance measured by contactor 2 crosses the tripping curve (t = 10 ms).

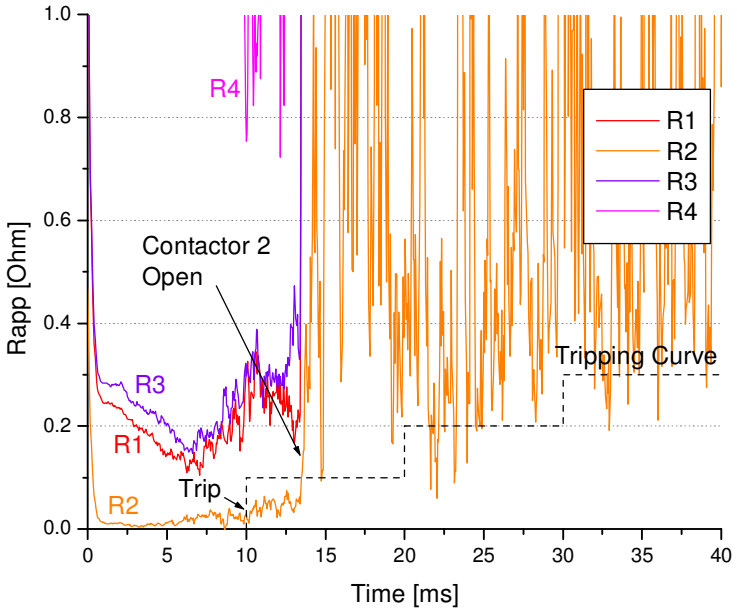

Figure 4.17 Apparent resistance calculation at the terminals of 4 contactors during a short circuit fault close to Load Zone 2. The fault was detected when the resistance measured by contactor 2 crossed the tripping curve (t = 10 ms).

Figure 4.18 and Figure 4.19 summarize the decision-making process of the four contactors for other three fault scenarios.

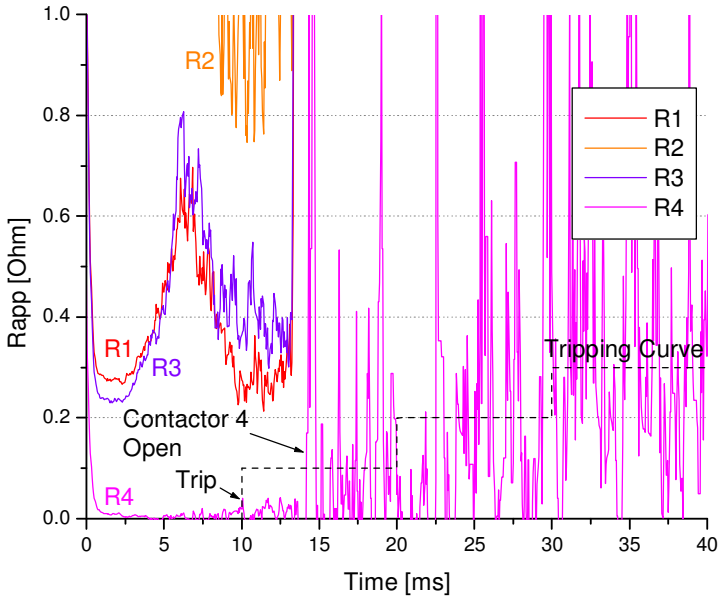

Figure 4.18 Apparent resistance calculation during a fault at Load Zone 1.

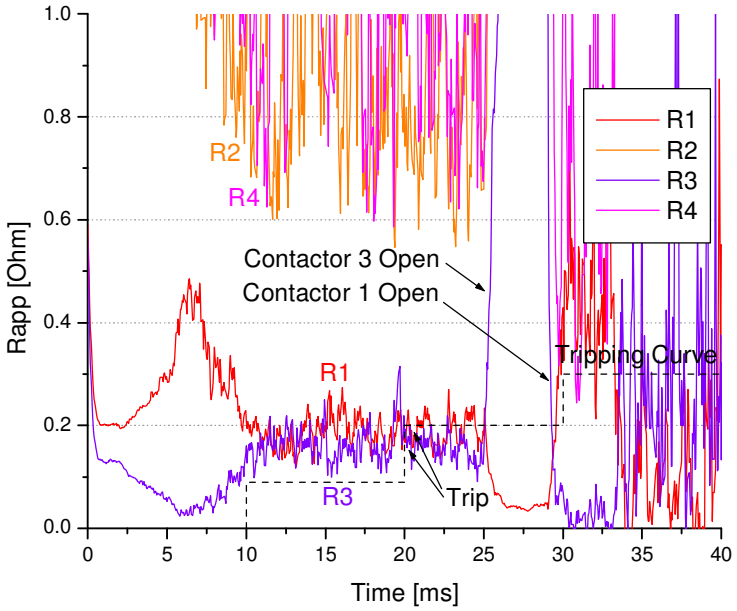

Figure 4.19 Apparent resistance calculation during a fault on Cable 1-3.

Figure 4.18 shows the detection of a fault close to Load Zone 1, where Contactor 4 is the one responsible for isolating the fault. Figure 4.19 shows that only the values of resistance calculated at the terminals of Contactor 1 and Contactor 3 cross the tripping curve for a short circuit fault on cable 1-3 of the distribution bus.

The results shown in this section are only few representative examples among the tens of scenarios that were tested in both simulation and experiments. In most of the cases, the fault was detected and isolated within 10 to 20 ms and the distribution bus was re-energized within 40 to 60 ms. In a few cases, in which we had excessive measurement noise or failure of opening of the contactors, the contactors with secondary priority opened within 20 to 30 ms and the bus was re-energized within 50 to 70 ms. We can observe that the low voltage experiments match with the medium voltage simulation in terms of fault dynamics, and in terms of response of the fault detection scheme. In fact, this gives confidence that the same scenario can be applied at the medium voltage level. Measurement errors and failure of opening in the desired conditions are explored in Section 4.5 for different system parameters and accuracies of the measurements.

4.5 FAULT DETECTION RELIABILITY

In this section we explored the operating boundaries of the developed fault detection method. In fact, the reliability of this method depends on both system parameters and on measurement accuracy of the devices used for implementing the fault detection. Errors in the resistance measurement arise from quantization in the analog to digital conversion process and from the accuracy and calibration of current and voltage sensors. The net error is shown in (30), where Δr is the error of the resistance measurement, Δv is the error

of the voltage measurement, Δi is the error of the current measurement, and I_r and V_r are the rated current and voltage respectively.

$$\Delta r = \frac{1}{I_r}\Delta v + \frac{V_r}{I_r^2}\Delta i \qquad (30)$$

Table 4.3 shows the achievable resistance measurement accuracy for some combination of common ADC resolutions and sensor accuracies.

TABLE 4.3

COMBINED RESISTANCE MEASUREMENT ACCURACY [%]

		ADC resolution			
		8bit	12bit	16bit	24bit
Sensors Accuracy	5%	10.78431	10.04884	10.00305	10.0000119
	2%	4.784314	4.04884	4.003052	4.00001192
	1%	2.784314	2.04884	2.003052	2.00001192
	0.5%	1.784314	1.04884	1.003052	1.00001192
	0.10%	0.984314	0.24884	0.203052	0.20001192
	0.01%	0.804314	0.06884	0.023052	0.02001192

The measurement accuracy has to be compared with the maximum error that the system parameters allow. In case of a symmetrical configuration of the main distribution ring bus (e.g. all sections of 25 m) we can observe that the maximum allowable error is defined by the 20% margin that we chose to guarantee selectivity between contactors, as mentioned in section 4.2. In case of asymmetrical configuration the maximum allowable error decreases as shown in Table 4.1. In order to validate the relationship between the asymmetry of the system and the reliability of the fault detection method, we ran multiple simulations with the addition of random noise with different amplitudes (0.1%, 0.5%, 1%, 2%) on the measurement of voltage and current measurement.

The results shown in Figure 4.20 to Figure 4.25 were realized by collecting a population of 100 tripping time of the detection device per 8 different positions along the

distribution bus, both in the case of a bus with sections of the same length (Figure 4.20, Figure 4.22, Figure 4.24) and in the case of bus with sections of different lengths (Figure 4.21, Figure 4.23, Figure 4.25).

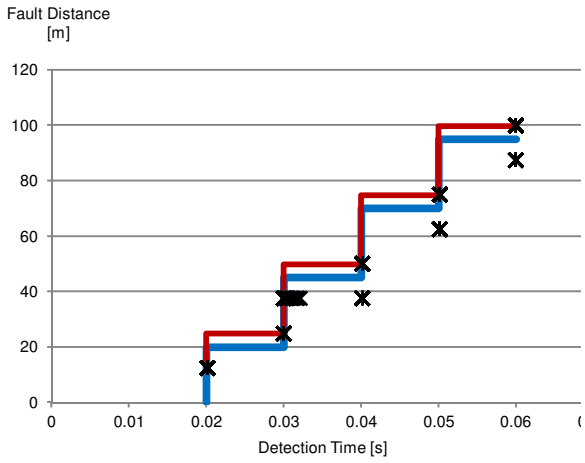

Figure 4.20 Detection time distribution for fault at different distances with 0.2% measurement accuracy for a symmetrical bus

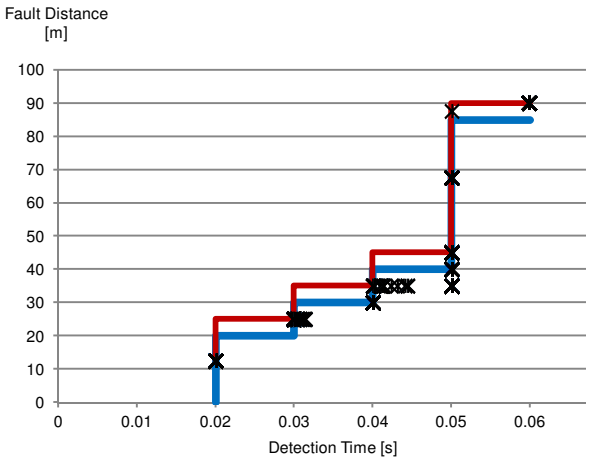

Figure 4.21 Detection time distribution for fault at different distances with 0.2% measurement accuracy for an asymmetrical bus

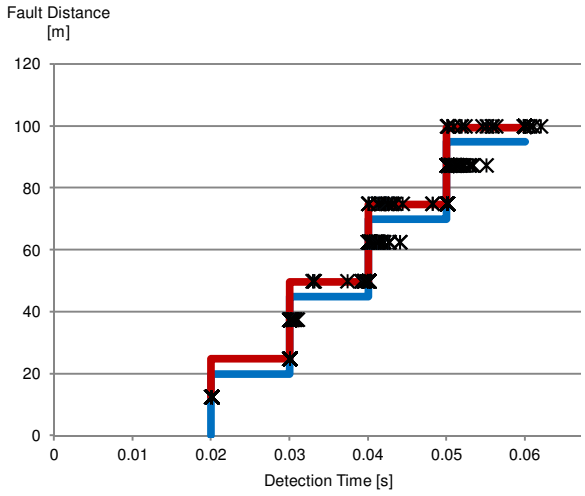

Figure 4.22 Detection time distribution for fault at different distances with 1% measurement accuracy for a symmetrical bus

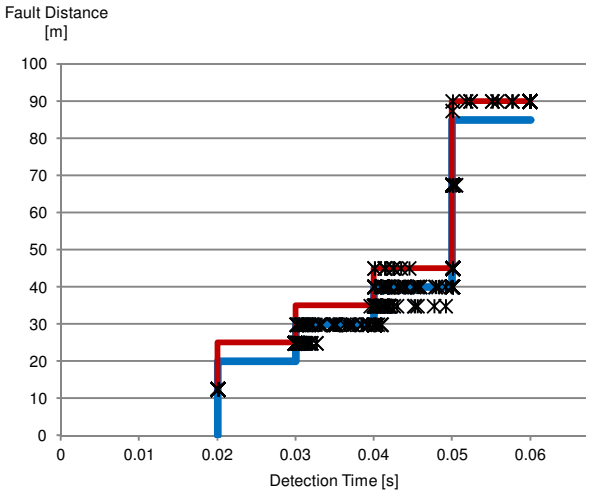

Figure 4.23 Detection time distribution for fault at different distances with 1% measurement accuracy for an asymmetrical bus

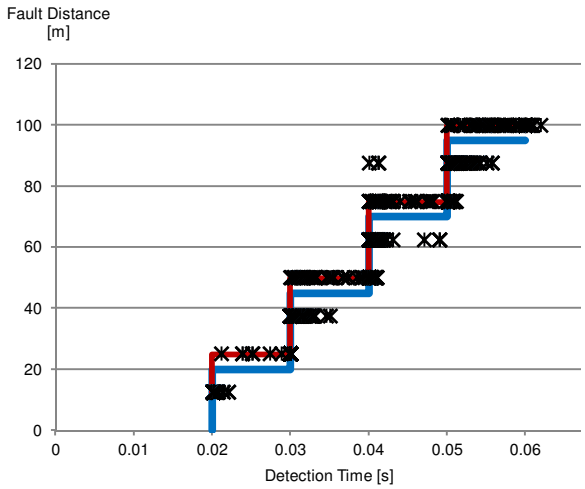

Figure 4.24 Detection time distribution for fault at different distances with 2% measurement accuracy for a symmetrical bus

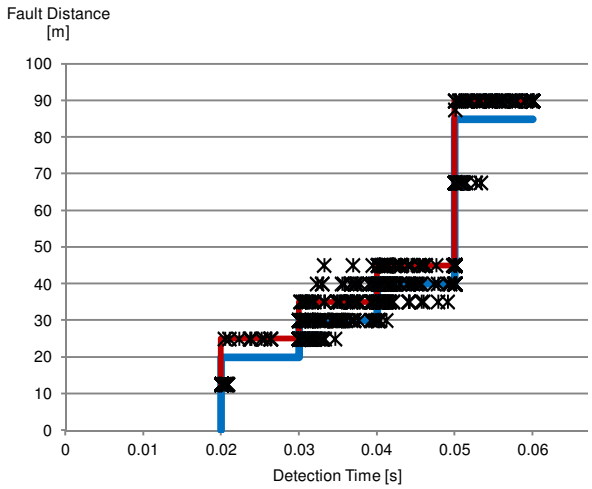

Figure 4.25 Detection time distribution for fault at different distances with 2% measurement accuracy for an asymmetrical bus

In the examples the bus is divided into sections of 25 m in the case of symmetrical bus, and of 25 – 10 – 10 – 45 m in the case of asymmetrical bus.

From these results we can observe that the device trips with a probability of 100% for all the different scenarios, but the probability to trip out of the desired range of time depends on the accuracy of the measurements and on the asymmetry of the system.

Table 4.4 shows how the probability of tripping out of range varies for the different scenarios.

TABLE 4.4

PROBABILITY OF TRIPPING OUT OF RANGE [%]

Resistance Measurement Accuracy	*Symmetrical Case*	*Asymmetrical Case*
0.20%	0%	0%
1%	0%	0.50%
2%	0.38%	2.88%
4%	29.50%	41.50%

Figure 4.20 to Figure 4.25 show the distribution of the time to trip after a fault detection (black stars) compared to the desire tripping curve characteristic of the device (red and blue lines).

In conclusion, this analysis gives a good indication of the reliability of the detection method depending on measurement accuracy and system parameters. In systems with a short distribution bus and a high nominal current, we observed that the low cable resistance (< 1% of the value of resistance corresponding to the rated system power) increases the probability for the devices to trip out of the desired range. The same effect happens for a distribution bus that is very asymmetrical (e.g. 1:10 length ratio between bus sections). This means that the contactors are not able to isolate the smallest portion of the distribution bus after a fault and one or more healthy sections of the system are disconnected.

A further important outcome of this work is the limitation of using the measurement of resistance for fault detection. In fact, in case of high impedance faults this method is not effective for the distinction of fault locations and does not provide selectivity between contactors. In the case of cable sections having a very small resistance compared to the expected fault resistance the accuracy requirements for the measurement device increase and can go beyond the range of technical feasibility. In these situations we recommend to combine this method with a differential current measurement that can provide a more accurate fault detection with the help of communication between protection devices. In this way the resistance-time detection method can provide backup protection in case of communication failure.

SUMMARY

In this chapter we presented a fault detection method that provides coordination between current limit set points of power converters, main bus tie contactors, and load zones contactors to protect MVDC systems against short circuit faults. This method not only defines trip characteristic curves based on measurements of the equivalent resistance at the terminal of each device, but also gives a detection algorithm that gives each element a decision capability that does not rely on communication between the elements. Simulation and experimental results show that faults can be isolated within 20 ms and the system can be re-energized within 100 ms. A further important outcome of this chapter is the limitation of using the measurement of resistance for fault detection. In case of high impedance faults, and cables sections having a very small resistance this method is not effective for the distinction of fault location and does not provide selectivity between contactors. Future research will focus on the integration of this fault detection method with techniques that rely on communication for a more accurate localization of faults.

The next chapter presents the conclusions of this work, summarizes the contributions of this dissertation, and provides guidelines for future work.

CHAPTER 5

CONCLUSION AND FUTURE WORK

This chapter summarizes the contributions of this dissertation and provides references for continuing this work in the future.

5.1 CONCLUSION

This work develops a new method for protecting MVDC distribution systems against short-circuit faults and provides a valid substitute for circuit breakers.

We first show how the combination of controllable power converters and bus tie switches can protect and reconfigure a DC distribution system in response to a short circuit fault. The results of the study show that is possible to depower the main distribution bus, isolate the fault and then re-energize the bus faster than an AC grid can be protected and reconfigured using traditional circuit breakers, and fast enough to remain within power quality requirements.

We show how the de-energizing and reconfiguration times depend on the size of the power system, the number of sources connected to the grid, the nominal system voltage, and the speed of contactors that isolate faulted parts of the system. Mathematical expressions for approximate system characteristics give a quick estimate of important parameters, such as time to peak current, time to safe opening of contactors, time to fault isolation, and time to power restoration.

Secondly, we developed a fault detection method that provides coordination between power converters, main bus tie contactors, and load zones contactors. This method not only defines trip characteristic curves based on measurements of the equivalent resistance at the terminal of each device, but also gives a detection algorithm that gives each element a decision capability that does not rely on communication between the elements. In this way, converters and contactors coordinate to isolate the smallest portion of the system after a short circuit fault.

We provide a comparison with other fault detection techniques, and we present the simulation and experimental validation of the developed method. A further important outcome of this work is the limitation of using the measurement of resistance for fault detection. In case of high impedance faults, and cables sections having a very small resistance this method is not effective for the distinction of fault location and does not provide selectivity between contactors.

The results of this dissertation provide essential guidelines for design of fault protection for dc microgrids and dc multi-terminal distribution systems, such as renewable energy distribution grids, data and telecommunication centers, or shipboard power systems and they illustrate how to achieve specified reaction times of the protection scheme.

5.2 FUTURE WORK

5.2.1 Medium voltage validation of the fault protection method

The fault protection method has been verified in both simulations at the medium voltage level and experimentally at the low voltage, low power level. These results

provide confidence that the protection method can be tested for a higher voltage and power level. Future work will require the validation of this fault protection method with appropriate experiments at the medium voltage and megawatt level.

5.2.2 Integration of the fault detection method with techniques that relies on communication

This work illustrates the capability of the evaluation of apparent equivalent resistance as a discriminant between fault conditions in a multi-terminal dc system. One of the outcomes of this research is the limitations of using this detection method for high impedance faults, and for certain system parameters. Future work will have to investigate the integration of this fault detection method with techniques that relies on communication for a more accurate localization of faults. The combination of different methods can increase the reliability of the system even in the harshest conditions.

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APPENDIX A – EXPERIMENTAL SETUP

HARDWARE TESTBED

A representative LVDC distribution system was constructed to validate the results obtained in the simulation environment. Figure A.1 illustrates the distribution system that is composed by 2 main power converters, 2 load centers, and a main distribution bus with 4 contactors as in Figure 4.9. The main power converters is a custom built 10 kW interleaved PWM buck converter derived by a IGBT 3 phase bridge module as in Figure A.2. The 3 phase bridge module has the characteristic of being a very modular converter and it is usually used for Voltage Source Converter (VSC) applications, such as 3 phase active rectifiers, inverters, and motor drives, an can also be configured to be used as DC/DC converter. This choice was taken especially because of the modularity and easy to scalability as showed in many power distribution projects that use Power Electronics Building Block (PEBB) modules as basic unit. Each converter is fed by a power supply that provides 3 kW DC power at the DC link of the converter as in Figure A.2. Figure A.3 shows a schematic of the CIPOS IGCM20F60GA power module used to build the DC/DC converters for a typical motor drive application. As in Figure A.2 the 3 phase bridge module is interfaced with a sensing board and a TI DSP Microcontroller. The sensing board measures the input and output differential voltages of the DC/DC converter as well as the currents going through the 3 filtering inductances.

The analog measurements are then converted by the Analog to Digital Converter (ADC) inside the microcontroller and for feedback control and fault protection as floating point variables. The converters are controlled with a dead-beat predictive current control inner loop, and a PI voltage control outer loop. In this way the converters can regulate the output voltage, limit the output current and the output power, as well as turning off and stop the power flow from the input to the output.

The two load centers are composed by a resistive load that can be stepped from 10 Ohm to 5 Ohm, a shunt capacitor that is connected to the load and is connected to the DC bus through a diode that prevents the capacitor to discharge into the main distribution bus.

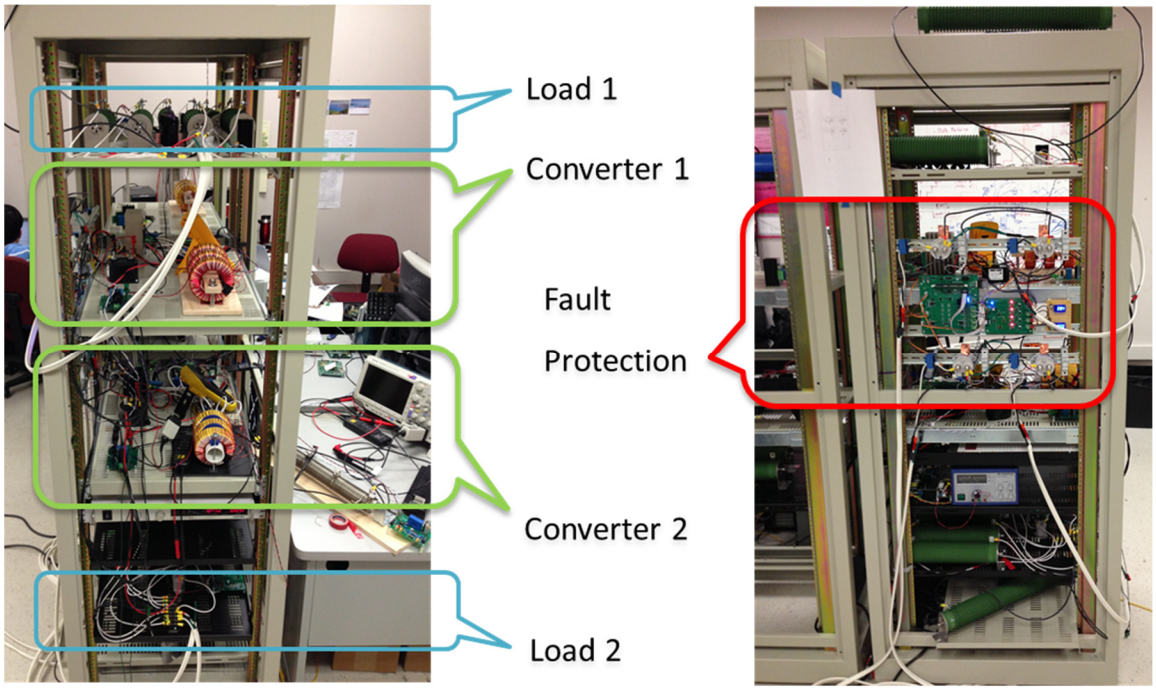

Figure A.1 LV experimental setup

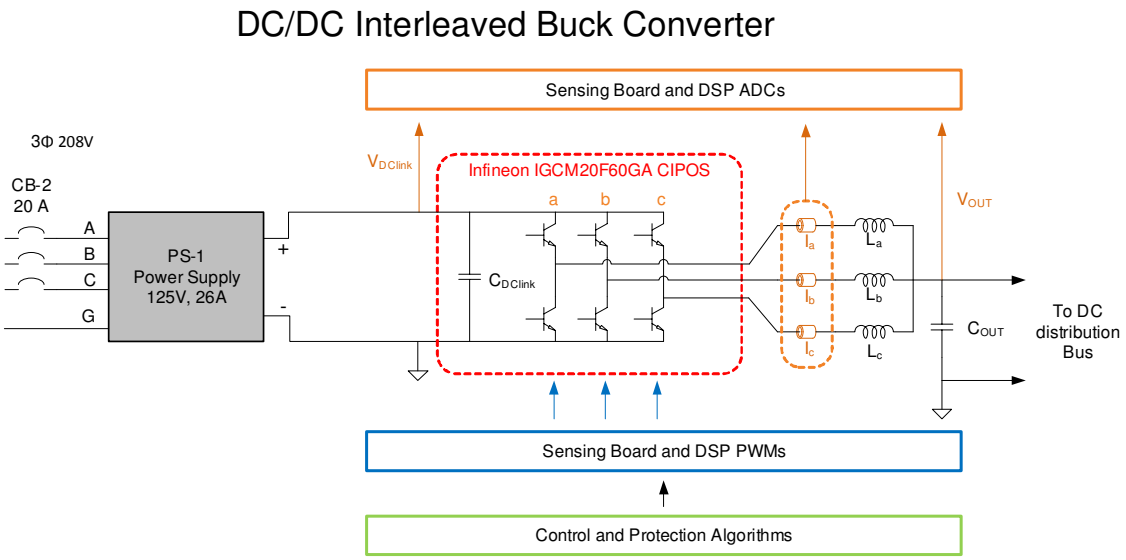

Figure A.2 DC-DC Interleaved buck converter schematic, measurements and control

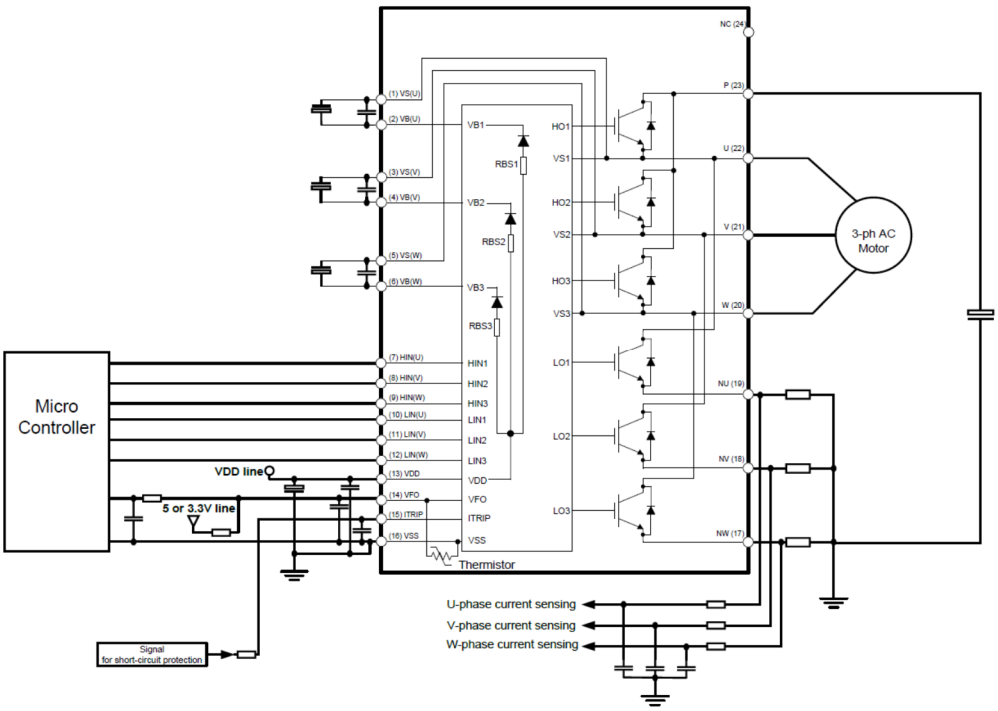

Figure A.3 CIPOS IGCM20F60GA Circuit of a typical application

The four contactors are LVDC mechanical contactors of the series Kilovac Lev200 rated up to 900 Vdc and 500 A [42]. These contactors are commanded by an auctioning

board driven by power MOSFET that is interfaced with a DSP microcontroller. This microcontroller is programmed with the fault detection algorithms that control the opening of the mechanical contactors. Even though the fault detection algorithms are programmed in the same microcontroller, they have independent measurements and decision capability.

A power resistor that can be varied from about 20 mΩ to 1 Ω is triggered by a power MOSFET in order to produce short circuit faults of different resistance. This fault resistance can be connected to multiple points of the DC distribution bus in order to study multiple fault scenarios.

APPENDIX B – DISTRIBUTION BUS CABLES MODELING

In this section we analyze the effects of the presence of a cable for power distribution in a MVDC system. Whereas in steady-state condition the literature suggests to neglect many of the effects of cables characteristic that we can find in long high voltage transmission lines, in the fault dynamics this approximation is not granted because of the high frequency components of the fault event. For this reason, we build a case for the MVDC system we are interested in, and we verify which kind of approximation is permissible.

According to the transmission line theory, for high voltage AC lines longer than 250 km the employment of uniformly distributed parameters is recommended for studying of the dynamics of the system. In fact, distributed parameters take into account EM effects of a voltage that varies along the line (at an instant) as in the case of microwave transmission lines or in the case of very long power transmission lines. In both cases the wavelength of the voltage is close to the length of the transmission line and it is usually considered if the length is bigger than 1/20 of the wave length [30], [52].In a MVDC ship system cable length are within 1 km, and by considering a 50 - 100 MW power system at +/- 5 kV, the parameters of cables can be summarized in the range illustrated by Table B.1.

TABLE B.1

CABLE PARAMETERS FOR 100MW MVDC SYSTEM

R [Ohm/km]	L [mH/km]	C [nF/km]	G [S/km]
0.05-0.5	*0.05-0.5*	*10-500*	*0*

Figure B.1 shows a generic transmission line that can be represented as a two-port network in different ways, but mainly it can be represented by means of lumped elements or distributed elements. The following analysis is a comparison of the influence of on the sending-end of the line voltage V_S and current I_S.

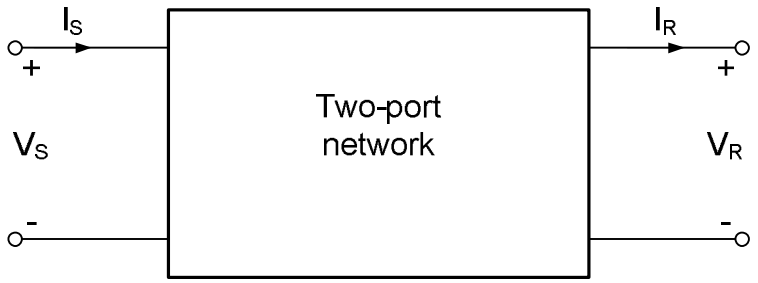

Figure B.1 Generic representation of a transmission line as a two-port network

The relationship between the sending-end and the receiving-end quantities can be written as:

$$\begin{bmatrix} V_S \\ I_S \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_R \\ I_R \end{bmatrix} \tag{B.1}$$

where A, B, C, D are parameters that depend on the transmission-line constants R, L , C, and G. Different level of approximation can be applied to a transmission line, Table B.2 shows three of them that are suitable for our study.

TABLE B.2

TRANSMISSION LINE: A, B, C, D PARAMETERS IN MATRIX FORMAT

Circuit	Matrix
Series impedance	$\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$
Pi circuit	$\begin{bmatrix} \left(1+\frac{YZ}{2}\right) & Z \\ Y\left(1+\frac{YZ}{4}\right) & \left(1+\frac{YZ}{2}\right) \end{bmatrix}$
T Circuit	$\begin{bmatrix} \left(1+\frac{YZ}{2}\right) & Z\left(1+\frac{YZ}{4}\right) \\ Y & \left(1+\frac{YZ}{2}\right) \end{bmatrix}$
Distributed parameters	$\begin{bmatrix} \cosh(\gamma x) & Z_C \sinh(\gamma x) \\ \frac{1}{Z_C}\sinh(\gamma x) & \cosh(\gamma x) \end{bmatrix}$

Where:

$$z = R + j\omega L \tag{B.2}$$

$$y = G + j\omega C \tag{B.3}$$

$$Z = z \cdot l \tag{B.4}$$

$$Y = y \cdot l \tag{B.5}$$

$$Z_C = \sqrt{\frac{z}{y}} \tag{B.6}$$

$$\gamma = \sqrt{zy} \tag{B.7}$$

In the distributed parameters circuit V_S and I_S in equation (B.1) can be also seen as $V(x)$ and $I(x)$ at point x of the distribution line. V_S and I_S correspond to the voltage and current when x is equal to the entire length of the line l. Figure B.2 explains the meaning of the uniform distributed parameters concept for differential sections of line δx.

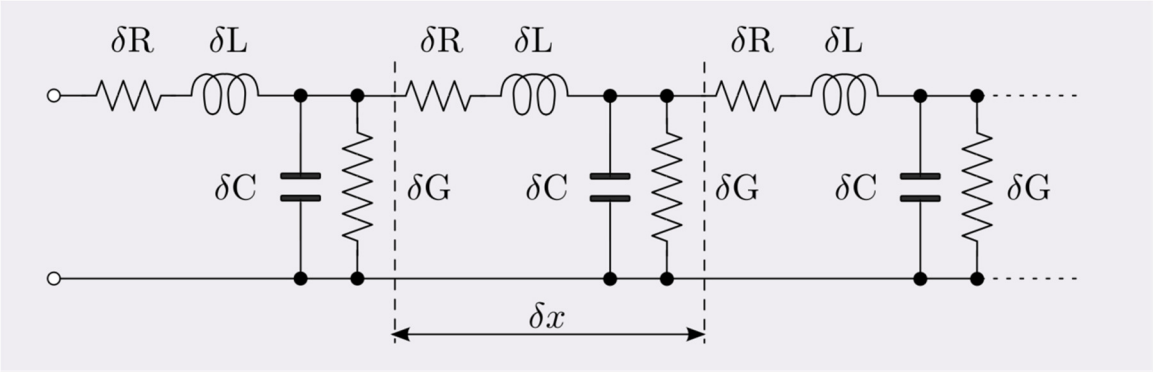

Figure B.2 Representation of a distributed parameters transmission line

COMPARISON BETWEEN PI REPRESENTATION AND DISTRIBUTED PARAMETERS

The comparison between different transmission line representations allows us to understand what could be the best model for the distribution cables of the MVDC ship distribution system during faults.

In this case, we consider a scenario where the maximum frequency of disturbances in a 1000 meters distribution line is about 50 kHz. Figure B.3 and Figure B.4 show how the voltage and current respectively change with the length of the line (increasing length or position x). The blue points represent the voltage or current variation according to a *pi* model and the green points correspond to the voltage variation according the distributed parameters model. In the second case, the matrix ABCD components of the line, and thus, the voltage and current at position x are influenced by the distance from the

receiving-end of the transmission line for a disturbance of 50 kHz, with *x* varying between 0 and 1000 meters.

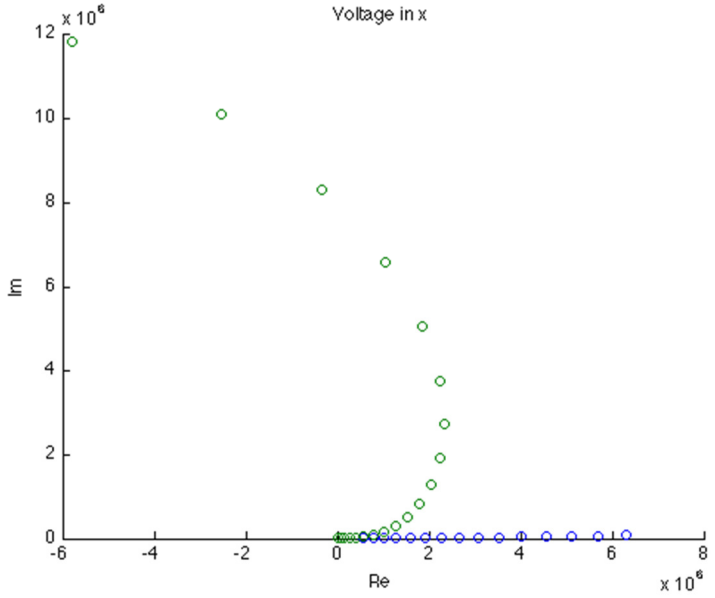

Figure B.3 Voltage along the line from x = (0 – 1000 m) for a pi-model (blue) and a distributed parameters model (green)

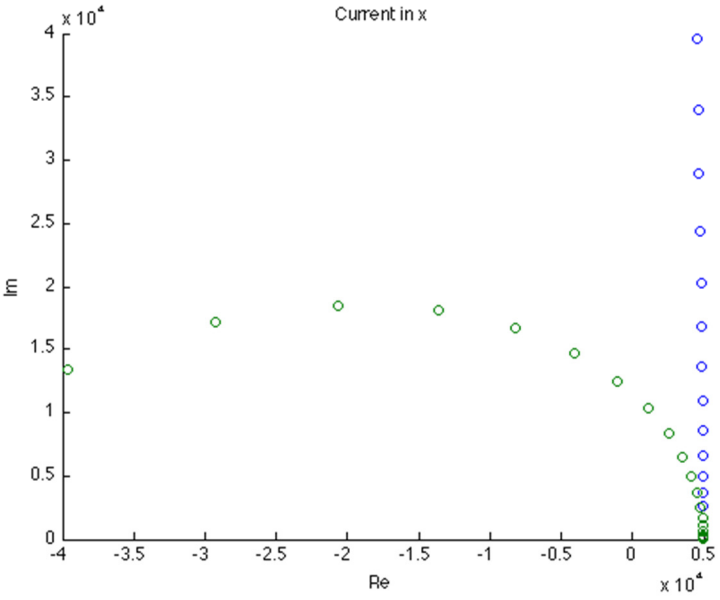

Figure B.4 Current along the line from x = (0 – 1000 m) for a pi-model (blue) and a distributed parameters model (green)

In a second case, we consider a scenario with the same transmission line characteristics, but with disturbances due to load steps and faults with a maximum frequency of 1-2 kHz. In this case the difference between the two models is less evident. Whereas in the voltage there is a slight change between the two models, the current has the same behavior especially if the cables stay within 500 meters of length.

This comparison shows that for cables within the kilometer or less, and a disturbance frequency within 1-2 kHz the pi model is still valid to analyze the dynamics of faults and fast transients. This would not be true in case of longer lines or higher frequencies as shown in Figure B.5 and Figure B.6.

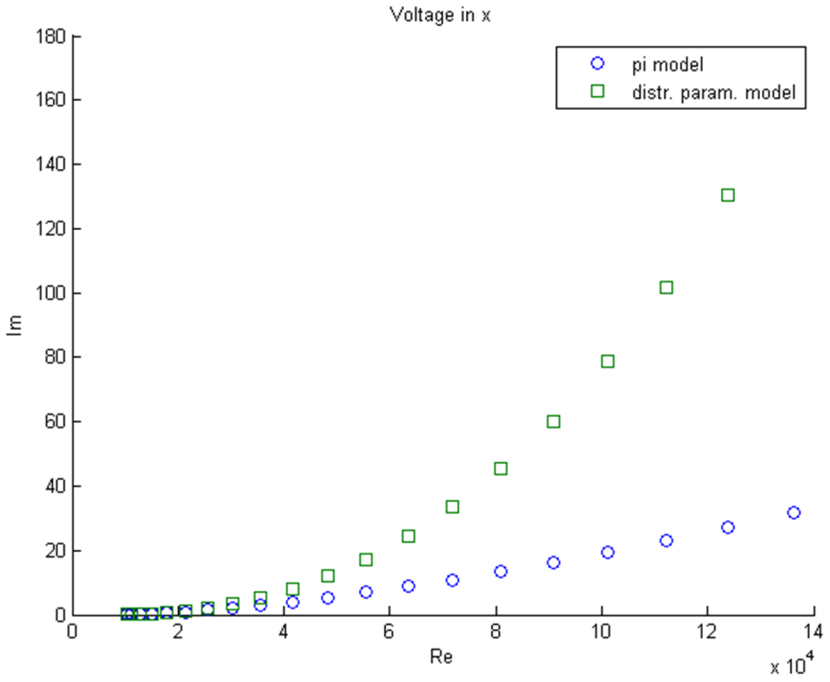

Figure B.5 Voltage along the line from x = (0 – 1000 m) for a pi-model (blue) and a distributed parameters model (square green) at a frequency of 1 kHz

Furthermore, in case of distributed capacitance of the cable smaller than 50 nF/km and frequency smaller than 5 kHz, the model can be simplified to a series impedance with the corresponding parameter matrix in Table B.2.

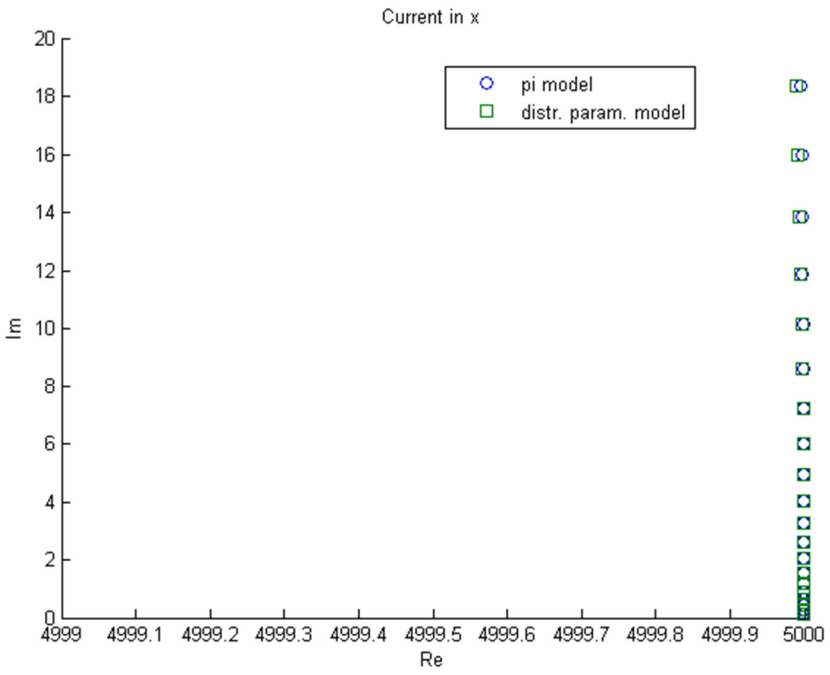

Figure B.6 Current along the line from x = (0 – 1000 m) for a pi-model (blue) and a distributed parameters model (square green) at a frequency of 1 kHz

The series impedance model is also valid for a distributed capacitance smaller than 400 nF/km for a disturbance frequency smaller than 1 kHz. In case of distribution lines shorter than 1 km, this approximation acquires even more validity because the effect of the shunt admittance components becomes negligible. This last model can be really useful in case of solving of differential equations of the dynamics of fault events, and in case of modeling for complex simulations.

CABLE PARAMETERS

In this section we summarize some cable parameters that can be useful for implementing models for simulations as illustrated in Table B.3.

TABLE B.3

COMPARISON OF COMMERCIAL CABLES FOR 100MW MVDC SYSTEM

Prysmian DOUBLESEAL15kV

Section [mm2]	R [Ohm/km]	L [mH/km]	C [nF/km]
223	0.426	0.183	-

Synergy Cables LTD – Medium Voltage Power Cables 12 kV

Section [mm2]	R [Ohm/km]	L [mH/km]	C [nF/km]
630	0.0283	0.277	670

Generalcavi Medium Voltage 15kV

Section [mm2]	R [Ohm/km]	L [mH/km]	C [nF/km]
240	0.0754	0.318	440

Theoretical

Section [mm2]	R [Ohm/km]	L [mH/km]	C [nF/km]
223	0.077	0.35	40