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PASSIVE EQUALIZER TOPOLOGY ANALYSIS FOR SIGNAL INTEGRITY APPLICATIONS

by

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Bachelor of Science

Ming Chuan University, 2006

Submitted in Partial Fulfillment of the

Requirements for the Degree of Master of Science in

Electrical Engineering

College of Engineering and Computing

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2013

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ACKNOWLEDGEMENTS

First, I would like to thank my professor Dr. Yinchao Chen who gives me this opportunity to work on research in signal integrity as a member of the group. It is highly appreciated for his dedication to instruct me during my master research in signal integrity. I have acquired a lot of useful and valuable knowledge from working with him who also is passionate for helping students to find a job.

Also, I would like to thank for my parents for their financial support that allowed me to complete my master degree at University of South Carolina. Their great spiritual support from long distance at Taiwan has encouraged me whenever I ran into problems or difficulties from completing my thesis topics. They have kept talking me and comforting me such that I am able to achieve my academic goals. I have to deeply acknowledge Mrs. Kimvak Jen, who not only helped as my mother's travels in the U.S, and but also always cooked many delicious dishes and provided valuable advices when I visited her home at Texas.

Last but not least, I would like to thank my other group members for sharing some research experience and knowledge with me such that I can greatly improve my research and successfully obtain my M.S. degree.

ABSTRACT

In high-speed, high density PCB bus systems, high frequency signal losses and crosstalk can have great impacts on signal integrity and digital timing, which can distort transmitted signals, worsen eye diagrams, and attenuate signal amplitudes. Also, these impacts make digital signals and their energy smearing over multiple bit positions as known as jitters, and cause the phenomenon of inter-symbol interference (ISI) in digital signal transmissions.

The main objective of this thesis is to analyze and develop efficient topology circuits for compensating bus system high frequency losses by using equalization techniques. The thesis has focused on study of various practical and efficient circuit topologies in order to improve its digital signals at receiver ends. The investigated equalization topologies include a shunt RC, series RL, Maxim's, Agilent's, and proposed equalizer circuits. It is found that with the application of the proposed equalization techniques, the quality of digital signals and eye diagrams is really improved up to the 50 inch lossy channels by using both the post-emphasis and de-emphasis compensation techniques.

Signal Integrity is an important research area in high-speed, high density digital transmission systems, and many factors, such as transmission line loss, circuit discontinuities, and non-linearity of passive and active components can easily distort signal quality to make them becomes unreliable in particular at high frequencies. Equalization is a powerful technique to restore distorted signals, which employs passive component as an equalizer applied to wired transmission channels.

A distorted signal can be resulted from different sources. One of dominant contributions is transmission line contains loss, including both conductor and dielectric losses. For a digital signal, jitter is an important characterization of distorted signals, which describes the signal turbulence in the time domain and time delay makes the signal postponed in a communication system.

This thesis mainly focuses the topology analysis, improvement, and development of passive equalizers, including shunt RC and series RL circuit equalizers. It is found these circuits can be applied to an interconnection solely, or combined with these two circuits as a RLC circuit. With this topology, the eye probe receives higher signal quality and less jitters. The delay and jitter are minimized after the compensation circuit applied. After the optimization, relocate the equalizer circuit before the transmission line and discuss the different influence on the signal.

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Chapter 1

Introduction

1.1 Motivation

For a PCB circuit or interconnects system, high frequency is preferable in order to get wide bandwidth and meanwhile keeping compact circuit size in digital and analog communications; But in comparison to low frequency communication operation, high frequency signals can much easily become distorted, such as signal irregular time delay, crosstalk, and ground bounce. Transmission lines printed on a PCB board are considered as ideal at a low frequency; however, their behavior at high frequency can be significantly distorted it is an important research to obtain good quality signals at receiver end for modern high speed digital circuit design.

The primary AC losses of transmission Lines are from conductor loss, which includes not only DC loss, but also that from the high frequency resistivity of conductors. At high frequencies, the currents flow mainly in the conductor surface area which is known as “Skin Effect”. A much smaller current conduction area along

transmission line at high frequencies leads to its high resistance or high loss due to this skin effect. On the other hand, dielectric loss is due to that its dielectric constant is not pure real and it contains an imaginary part that results in a dielectric loss, which is commonly found in a PCB substrate such as FR4.

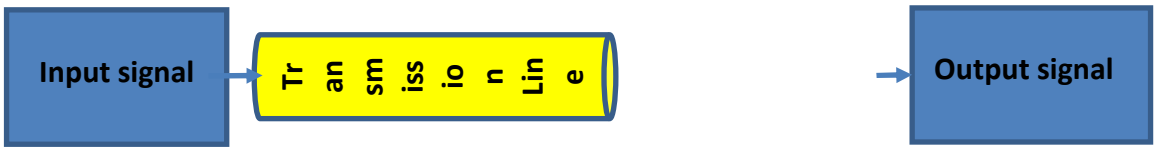


Figure 1.1 Lossy channel

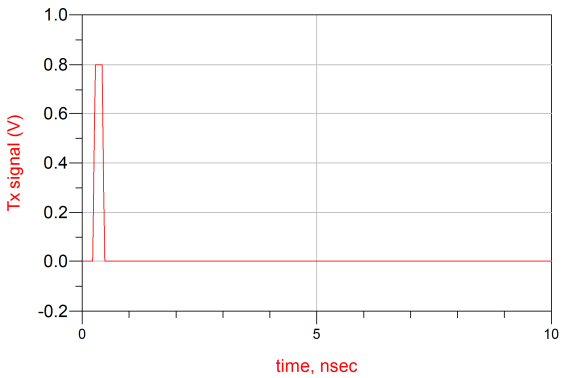


Figure 1.2 Input waveform

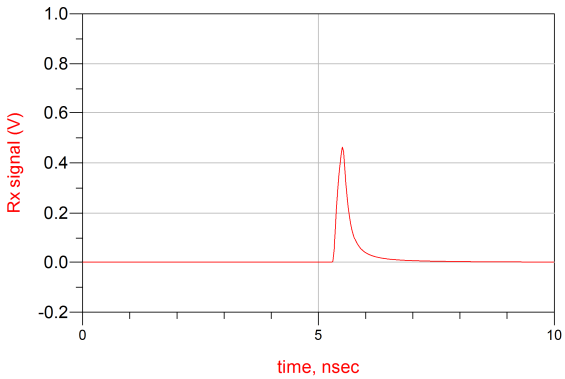


Figure 1.3 Output waveform

It is found that both conductor loss and dielectric loss can cause signal distortion in particular at high frequencies. Moreover, those losses prolong the rise time of signals, reduce signal levels, and worsen signal quality. For instance, a unit pulse signal input to a transmission line system shown as Figure 1.1, where the transmission line is a lossy channel. A distorted signal is generated after passing through this lossy transmission channel. The amplitude of the signal is reduced unevenly as a function of frequency and

the signal is delayed by the lossy media. As a result, it is hard to determine the signal logically at the receiver end of the system. For design of signal traces of high speed digital circuits, the signal integrity techniques for ensuring signal quality becomes more and more essential nowadays. In common practice of signal integrity engineers, the eye diagram is a very efficient tool to determine the quality of signal and performance of a digital communication system in order to make the system working properly.

1.2 Outline of the Thesis

There are total seven chapters in this thesis. After a brief introduction in Chapter1, Chapter 2 reveals the possible resources of signals' distortion when they are propagating along a high speed transmission line; it also summarizes composition of various losses inside high speed interconnects. In Chapter 3, high speed signal jitter is defined and illustrated, and the Inter-Symbol Interference (ISI) in a multiple trace system is explained. Next, Chapter 4 shows different solutions to eliminate ISI in a high speed transmission system and explains various equalizers concepts. In Chapter 5, the various equalizer models and topologies are investigated, developed, and compared for practice signal integrity applications. Finally, Chapter 6 summarizes the proposed passive equalizers and their corresponding circuit layouts to be implemented in the proposed design. The last chapter briefs the conclusions as well future work.

Chapter 2

Transmission Line Concepts

One of the major differences between the transmission line and the conventional electric circuit theories is that lump circuit components are used in the circuit theory with a low frequency approximation while in the transmission line theory the dimensions of the circuit components are comparable to the guided wavelength of operation frequency. In general, when the dimensions of a circuit component are much shorter than the guided wavelength of its associated circuit devices, it is appropriate to use electric circuit theory to estimate the effect on the device. In practice, the maximum size of a device by accurately using the circuit “lumped element” model is one twentieth of the guided wavelength; otherwise, if a component size is comparable to the guided wavelength, it is named as “distributed element” because the amplitude and phase are variable at different locations on the component.

As the operation frequency of communication becomes higher, the guided wavelength is conversely getting shorter. Therefore, at high frequencies, it is inaccurate to accomplish a circuit design by using the lumped element concept. Instead,

it is an inevitable choice to use distributed elements to design any high frequency communication circuits.

2.1 Fundamental Transmission Line Concepts

Micro-strip line is a quasi-static TEM structure, whose filed distribution is shown in Figure 2.1 where the current flows through its transmission trace.

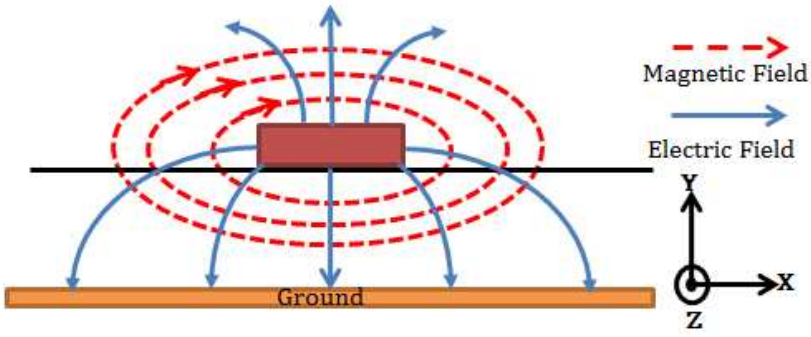


Figure 2.1 Field distribution for a microstrip line

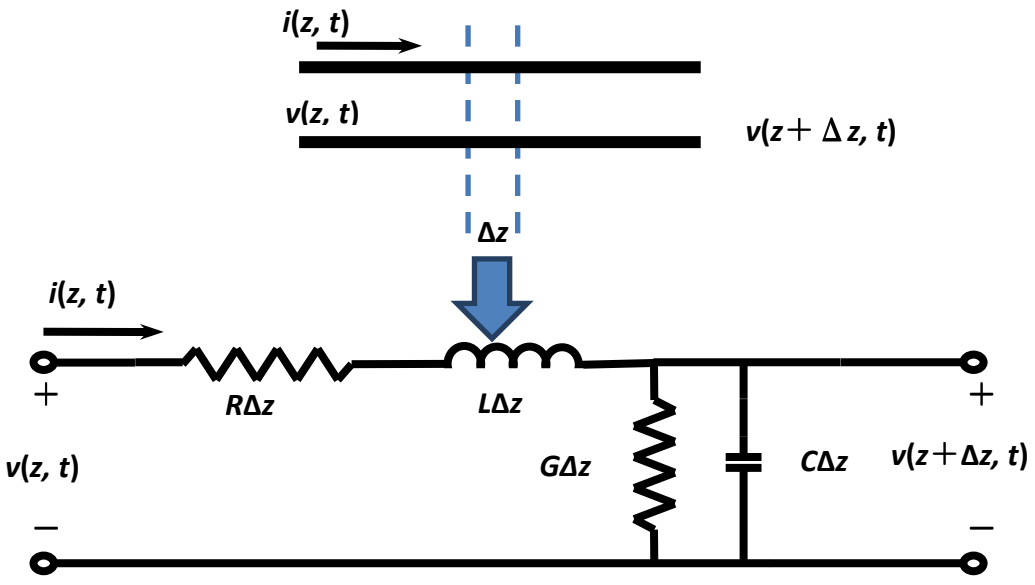


Figure 2.2 Transmission Line

As seen in Figure 2.2, two wires represent the schematic circuit of the transmission line, and one differential segment of this transmission line can be modeled as lumped elements. From Kirchhoff's voltage law (KVL) and current law (KCL), and by setting the segment length Δz, approaching zero, namely Δz→0, we derive following transmission line equation pair:

$$\frac{\partial \upsilon(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \tag{2-1}$$

$$\frac{\partial i(z,t)}{\partial z} = -G\upsilon(z,t) - L\frac{\partial \upsilon(z,t)}{\partial t} \tag{2-2}$$

The above equations are also called "telegrapher equations" historically. In the phasor domain, the time independent $e^{j\omega t}$is assumed, and the above time domain equations can be simplified as

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2-3}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2-4}$$

Decoupling the above transmission line combine equations yields the voltage and current wave equations:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2-5}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{2-6}$$

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \text{ [1]} \tag{2-7}$$

where γ is the propagation constant, which is a function of transmission line parameter R, L, G, C, as well as function of the operation frequency. The standard solution solutions for the voltage and current waves are derived as follows:

$$V(z) = V_0^{+} e^{-\gamma z} + V_0^{-} e^{\gamma z} \tag{2-8}$$

$$I(z) = I_0^{+} e^{-\gamma z} + I_0^{-} e^{\gamma z} \tag{2-9}$$

where both the voltage and current waves are composed of two signals propagating in opposite directions, $e^{-\gamma z}$ represents a wave propagating in the +z direction, and $e^{\gamma z}$ represents another wave propagating in the -z direction. The characteristic impedance Z_0 is defined as the as the ratio between the positive traveling voltage and current, namely,

$$Z_0 = \frac{V_0^{+}}{I_0^{+}} = -\frac{V_0^{-}}{I_0^{-}} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \text{ [1]} \tag{2-10}$$

2.2 Conductor DC Loss

Transmission lines are made from metal traces and dielectric substrates. Since a trace and ground metals are not a perfect electric conductor, and the metal traces' conductivity is finite, the corresponding trace resistance at DC as well as low frequency can be approximately evaluated using a DC model. The effective cross sectional area on which the current can flow through determines the metal trace DC loss. As seen in Figure 2.4, the DC current uniformly distributes along the cross section area of the microstrip line.

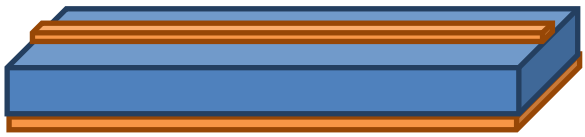


Figure 2.3 Geometry of microstrip line

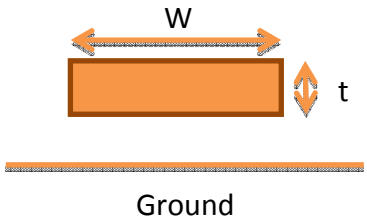


Figure 2.4 Cross-sectional view for a microstrip line

The DC resistance loss for a microstrip line as shown in Figure 2.4 can be evaluated as

$$R_{DC} = \frac{\rho \mathrm{L}}{\mathrm{A}} = \frac{\rho L}{Wt}\ \Omega \qquad (2\text{-}11)$$

where ρ is the resistivity constant of the trace, W,t, and L are the width, thickness, and length of the metal trace considered in the figure. Sometimes, a DC loss along the trace could be ignored, if a good conductor trace is used at high frequencies.

2.3 Conductor AC Loss (Skin effect)

If a system bus system at a low frequency, it only needs to consider DC. However, when operation frequency is high, the AC resistance has to be evaluated in terms of high frequency characteristics of transmission lines. Precisely, the AC resistance is estimated by using the effective cross section dimensions determined by conductor skin depth δ [2]seen in Figure 2.5, which is quantitatively given as follows

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} = \sqrt{\frac{\rho}{\pi f \mu}}\, m \qquad (2\text{-}12)$$

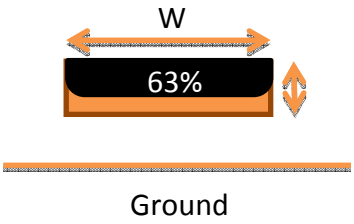


Figure 2.5 Skin effect[2]

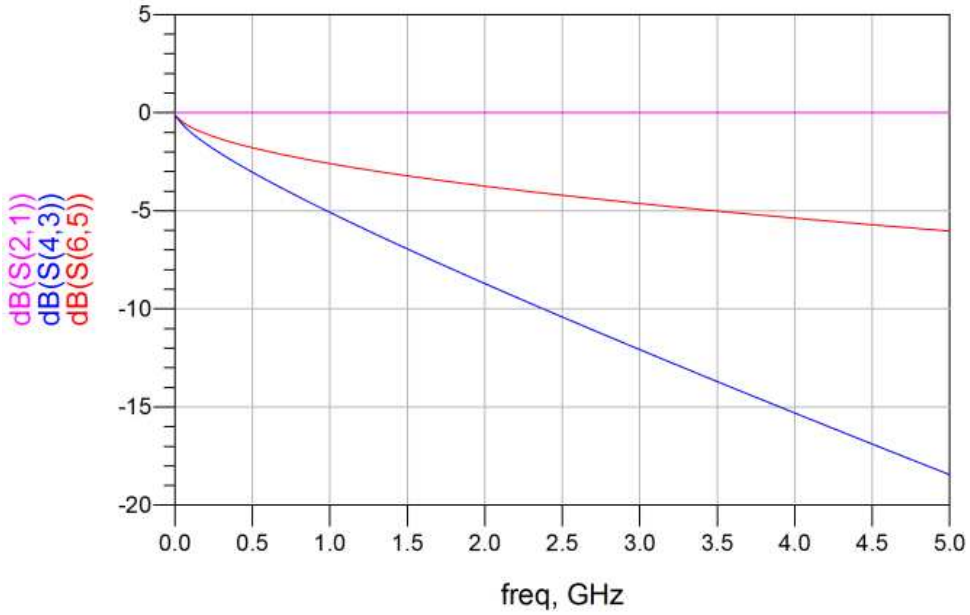


Figure 2.6 Insertion loss for a microstrip 35 inch line with AC loss; where pink line is for lossless line, red for including the conductor loss, and blue for including conductor and dielectric loss.

At a low frequency, dc resistance and ac resistance are similar, that's because the skin depth is much deeper than the height of conducting trace t. As long as the skin depth δ is smaller than the thickness of the wire t, then the skin depth replaces the thickness of the trace. Thus, we can arrive the approximated AC loss [2]as follows:.

$$R_{ac} = \frac{\rho}{W\delta}\frac{\Omega}{m} \tag{2-13}$$

As a result, in signal integrity engineering practice, the approximation of total resistance can be combined with R_{ac} and R_{dc} as give as

$$R_{total} \approx \sqrt{R_{ac}^2 + R_{dc}^2} \tag{2-14}$$

The skin effect for a metal trace occurs at high frequencies, in which the current flows close to the surface of the conductor. Herein, it is assumed that the surface of conductor is smooth in the current DC and AC analysis. In fact, the surface of conductor is rough, which is particularly significant when the frequency is 10 GHz or higher. If a signal operates at a higher frequency, the skin effect and roughness of conductor can not be ignored. The roughness can result in extra resistance at a higher frequency, in other words, we should account for additional amount of the resistance when the ac resistance is analyzed.

2.4 Dielectric Loss

At low frequencies, dielectric loss can be ignored in most PCB designs, because the dominant distortion comes from conductors. However, as increment of operation frequency, the assumption is no longer suitable. The dielectric loss at high frequencies becomes much important, which can significantly affect performance of a communication system..

Considering the influence of dielectric loss, the permittivity becomes a complex as seen below

$$\varepsilon = \varepsilon' - \mathrm{j}\varepsilon'' \tag{2-15}$$

where the imaginary part of the permittivity represents dielectric loss while its real part remains relatively stable as that at low frequencies. The equivalent conductivity of a lossy dielectric [2] material is given as

$$\frac{1}{\rho} = 2\pi f \varepsilon'' \tag{2-16}$$

where ρ is the effective resistivity of dielectric substrate and f is the operation frequency. In the communication engineering, the "loss tangent" is define as a parameter to characterize the lossy level of the medium, which is given as

$$\tan|\delta_d| = \frac{1}{2\rho f \varepsilon} = \frac{\varepsilon''}{\varepsilon'} \tag{2-17}$$

In a transmission line model, the RLGC parameters are frequently used to characterize this transmission line, and in particular, the shunt resistance G[2] is mainly derived from the substrate features, which is given as

$$\mathrm{G} = \frac{\varepsilon''}{\varepsilon'}(2\pi f C_{11})\ (s) \tag{2-18}$$

Chapter 3

Introduction to Jitter

3.1 Introduction

The previous chapter has discussed the effect on the physical layer of high speed interconnect circuits. This chapter starts with a typical digital communication system model as shown in Figure 3.1, which consists of a transmitter, a receiver, and a transmission line medium as the signal propagation channel.

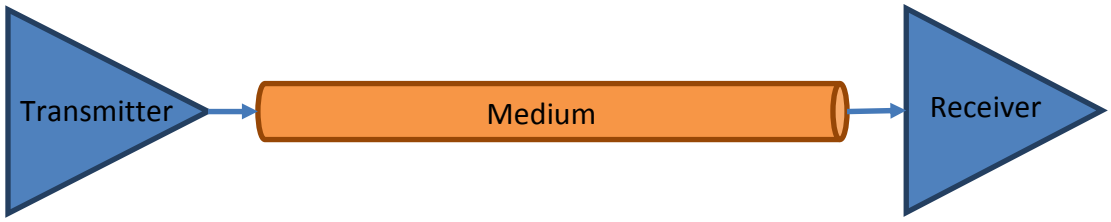


Figure 3.1 Communication system block diagram

Noise is an unwanted input added to desirable signals in the communication system. Jitter is a signal noise generated as a perturbation added to signals. Noise is the amplitude addition to digital signals, while jitter represents the time deviation of digital

signals. Moreover, it usually can be predicted from a deterministic model by a statistical approach.

There are different sources that can result in jitters in a communication system, such as temperature, spatial distribution of current flow, or flick noise.

Table 3-1 Equation of noise[3]	
$A(t) = A_0(t) + \Delta A(t)$	$\Delta t(t) = \frac{\Delta \mathrm{v}}{\left(\frac{dA_0(t)}{dt}\right)} = \frac{\Delta t}{k}$
A small signal with noise($\Delta A(t)$) added	The perturbation of noise (Jitter)

As shown in Table 3-1, a noise($\Delta A(t)$) is added to signal ($A_0(t)$), and correspondingly, the small signal Jitter ($\Delta t(t)$) is introduced. The phenomenon is explained in Figure 3.2.

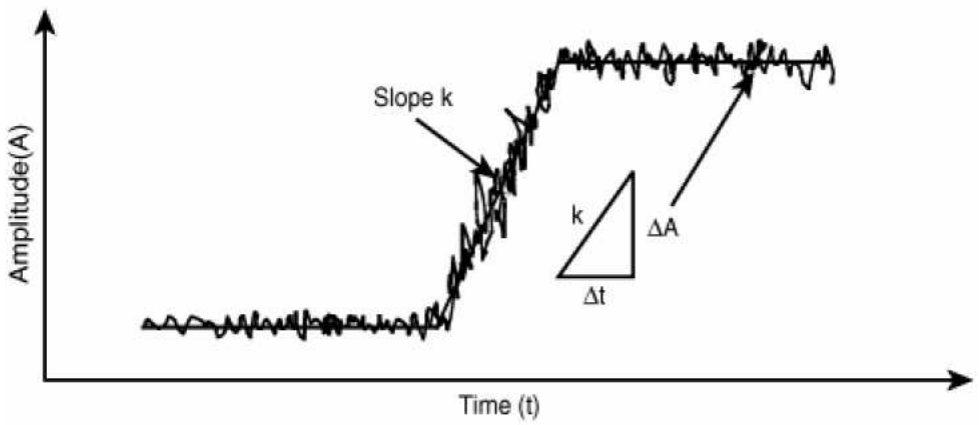


Figure 3.2 The signal with noise added in time domain with small signal perturbation[3]

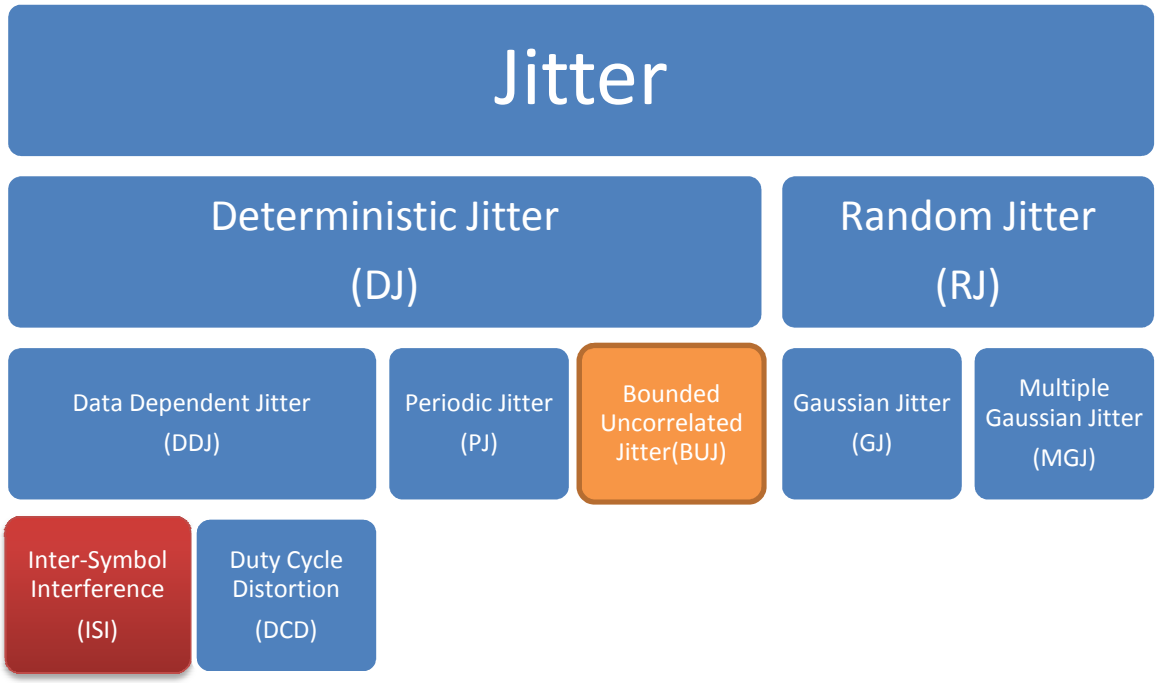


Figure 3.3 Jitter classification[3]

All of the jitters are classified as summarized in Figure 3.3. In general, jitter can be classified by two different kinds of noise: deterministic jitter and random one. The former is continually added to signal waveforms and it can be predicted analytically by signal propagation characteristics, while the random jitter is hard to predict and is

naturally generated from the random system sources. The equalizer can restore the distorted signals from the transmission channels, which are deteriorated by Inter-symbol interference (ISI). Usually, the convolution calculations of the power density functions of signals can be used for estimating the total jitter effects as summarized in Table 3-2. It shows the convolution relation among the power density functions (PDF, or f), where the different subscripts indicate the different jitter source of PDF. For example, the deterministic Jitter can be calculated by data dependent jitters, periodic jitter, and bonded uncorrelated jitter through convolution operation. The BUJ is caused by crosstalk. The other portion of jitter is random jitter which is combined with random gaussian jitter and multi-gaussian jitter. The total jitter is the product of deterministic jitter and random jitter.

Table 3-2 Evaluation of jitters from statistic method

Deterministic jitter	$f_{DJ} = f_{DDJ} * f_{PJ} * f_{BUJ}$
Radom jitter	$f_{RJ} = f_{RGJ} * f_{RHJ}$
Total jitter	$f_{TJ} = f_{DJ} * f_{RJ} = f_{DDJ} * f_{PJ} * f_{BUJ} * f_{RGJ} * f_{RHJ}$

3.2 Determinist Jitter

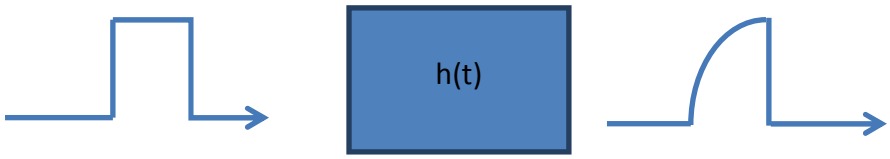


Figure 3.4 Square signal transform[3]

Deterministic Jitters are controllable and predictable deviations of signals at a receiver end, such as Inter-symbol interference (ISI) or duty cycle distortion (DCD).

3.2.1 Inter-Symbol Interference (ISI)

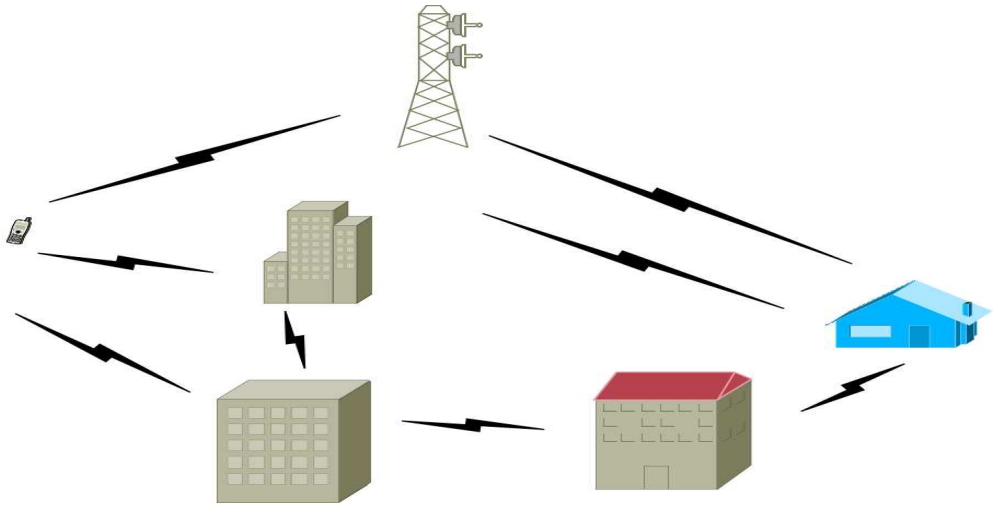


Figure 3.5 ISI effect by multipath communication

The concept of inter-symbol interference (ISI) can be illustrated by that in wireless communications. In a wireless communication system, multipath propagation[4] is a big issue in telecommunication as displayed in Figure 3.5. If transmission power is large enough to transmit communication signals, the receiver can easily receive these signals from a multi-path system. However, they are not recognizable because the time delays of signals from a multipath signal propagation channels, which is the ISI phenomenon in wireless communications. In a multi-transmission line system, signals received at one of the receiver ends are the superposition of the transmitted signals and crosstalk signals from the adjacent propagation channels.

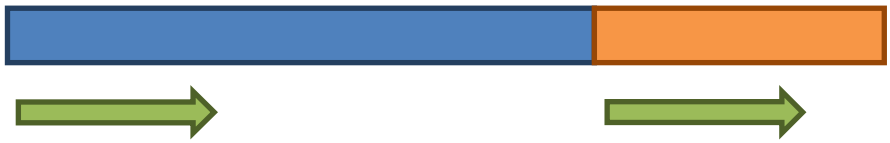


Figure 3.6 Impedance match

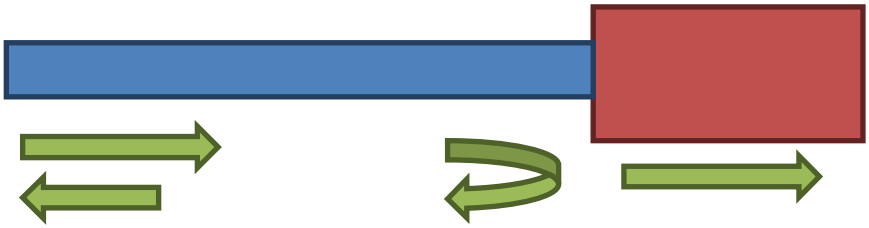


Figure 3.7 Impedance mismatch

Figure 3.6 and Figure 3.7 show two propagation channels to transmit, a series digital signal "00000101001110010111101111" which input to a system with 5 GHz data rate. There are two different channels considered: one is ideal channel without loss, and the other is a lossy channel.

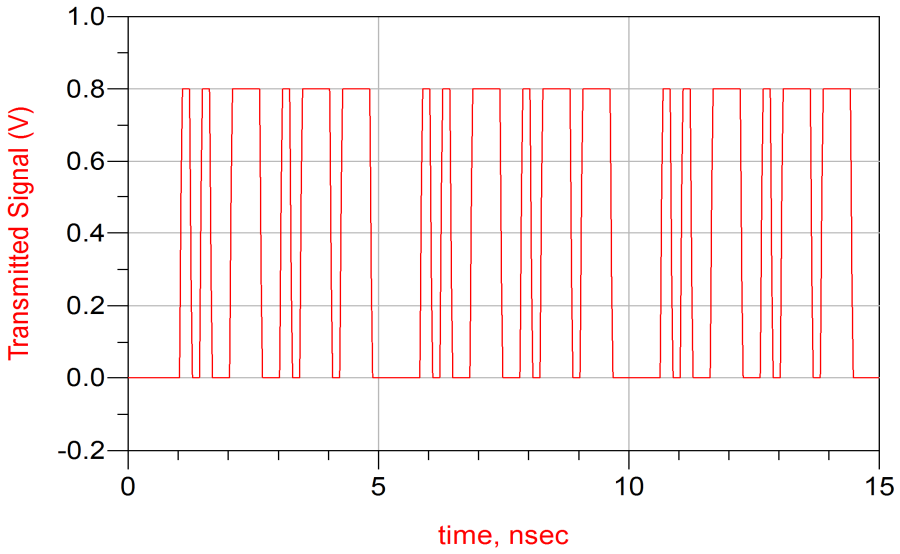


Figure 3.8 Waveform of ideal transmission line at 5GHz

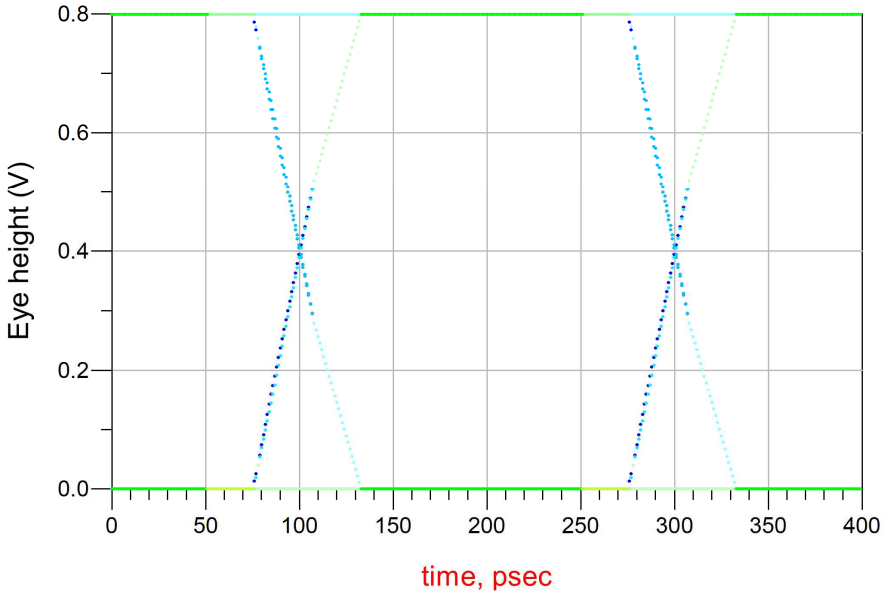


Figure 3.9 Eye diagram of ideal transmission line at 5GHz

For the ideal channel, as seen in Figure 3.8 and Figure 3.9, the generated eye diagram is very clean with high good quality. While for the lossy propagation channel, as displayed in Figure 3.10 and Figure 3.11, the transmitted signals encounter signal delays, the received

signals display signals display with jitters at the signals' rise and fall edges, and the eye diagram of the signals shows a serious jitter phenomenon for distorted signals with a small eye opening.

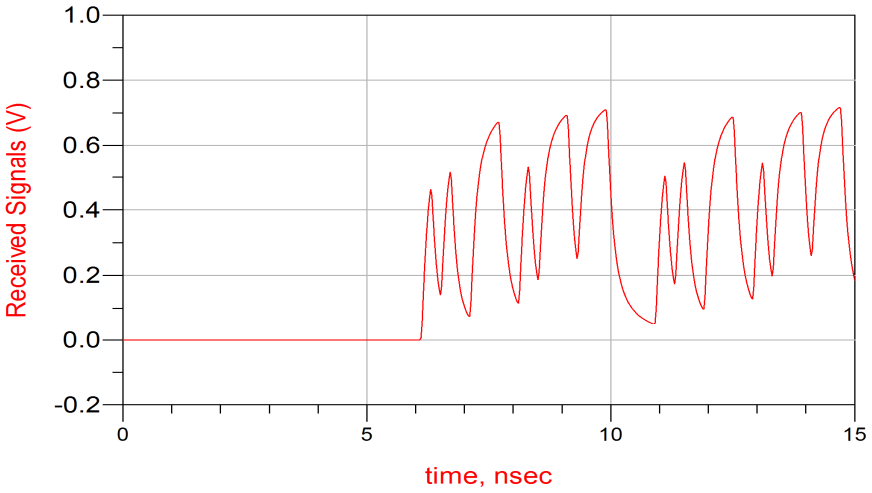


Figure 3.10 Received waveform of real transmission line at 5GHz

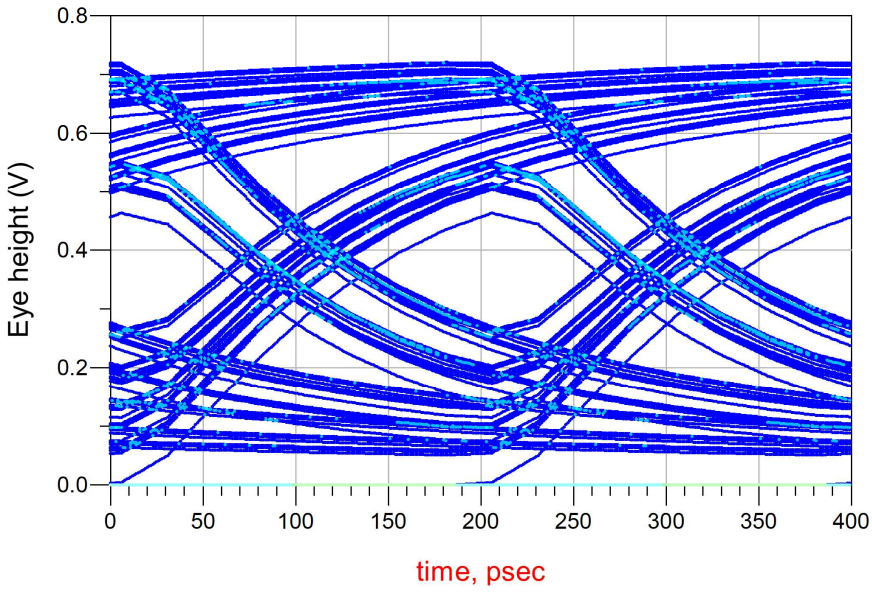


Figure 3.11 Eye diagram of real transmission line at 5Ghz

Chapter 4

Equalizer Fundamentals

High frequency loss for transmission line is determined by its associated attenuation constant. In general, the transmission line is characterized as a low pass filter, which can be seen as constructed by RLGC parameters. Consequently, compensation for high frequency attenuation of the transmission is a key technique used in equalizer circuits. The common practice is either, to amplify high frequency oscillated wave or to reduce the signal magnitude at low frequencies wave, in order to compensate and balance the high frequency loss, which is usually referred as “equalization” by using these two compensations. Most commonly equalization devices can be sorted as: active and passive equalizers, dependent on the passive and active components used in building up equalizers.

4.1 Active Equalizers

An active equalizer[5] usually consists of a passive equalizer and an amplifier, where the passive equalizer is designed for compensating and balancing high frequency

signals while the amplifier is used for enhancing signal levels in the whole frequency band. The disadvantages of active equalizers are to add more active and passive circuit components, increase circuitry costs, and require large circuit dimensions, which are not interest of this thesis.

4.2 Passive Equalizers

The frequency characteristics of a transmission line behave like a low pass filter. When the transmission channel is connected to an equalizer, an equalizer compensates the propagation channel for high frequency loss that are resulted from conductor and dielectric losses, in order to make the frequency response flat in the frequency range of interest. In the frequency domain, it is expected that the decreasing rate of the output signal frequency response through a transmission line is comparable to that of increasing for the compensation equalizer circuits. As seen in Figure 4.1, the multiplication of the transmission line frequency response and that of the equalizer shows relatively level performance. As a consequence of such frequency characteristics of the system, in the time domain, the output waveforms of the system is good replica of its input waveforms with differences in terms of time shifts and amplitude decrements. In general, high pass filter performance can be realized by RC, RL or RLC passive components.[6, 7]

4.2.1 Equalization Concept

The scattering parameters are frequently used in RF, microwave, and signal integrity for characterizing a two-port network frequency response. Herein, the known transmission line coefficient, S_{21} is defined as the system transfer function $H_{TL}(f)$. If $H_{TL}(f)$ and $H_{eq}(f)$ represent the transfer function for the transmission line and equalizer, respectively, $H_{comp}(f)$ is the overall transfer function after plugging the compensated circuit into the system. These three transfer functions[6] are related as given as follows:

$$H_{eq}(f) = \frac{H_{comp}(f)}{H_{TL}(f)} \tag{4-1}$$

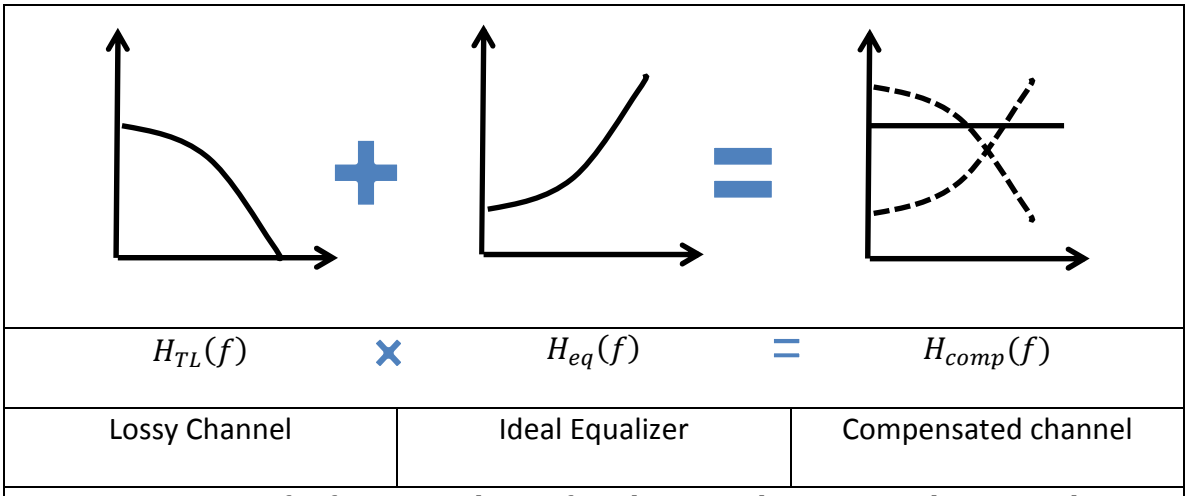


Figure 4.1 Transfer function relation for a lossy media connected to a equalizer

Mathematically, the overall transfer function $H_{comp}(f)$ is the multiplication of the transfer functions $H_{TL}(f)$ and $H_{eq}(f)$ in the frequency domain, although its time domain version is the convolution of the corresponding time domain impulse functions.

The demonstration is simulated by a 35inch lossy channel at 5 GHz and a RLC equalizer circuit. Figure 4.2 and Figure 4.3 represent the S_{21} of lossy channel and equalizer, respectively, and Figure 4.4 shows the S_{21} of the channel compensated by the equalizer. Figure 4.2 through Figure 4.4 are summarized in Figure 4.5.

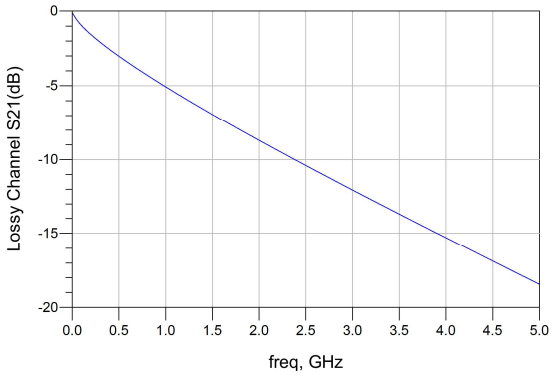


Figure 4.2 S_{21} of lossy channel

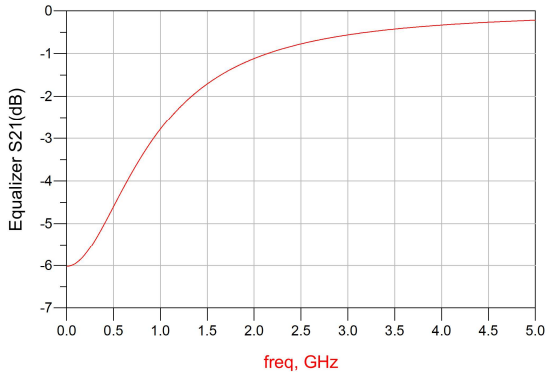


Figure 4.3 S_{21} of equalizer

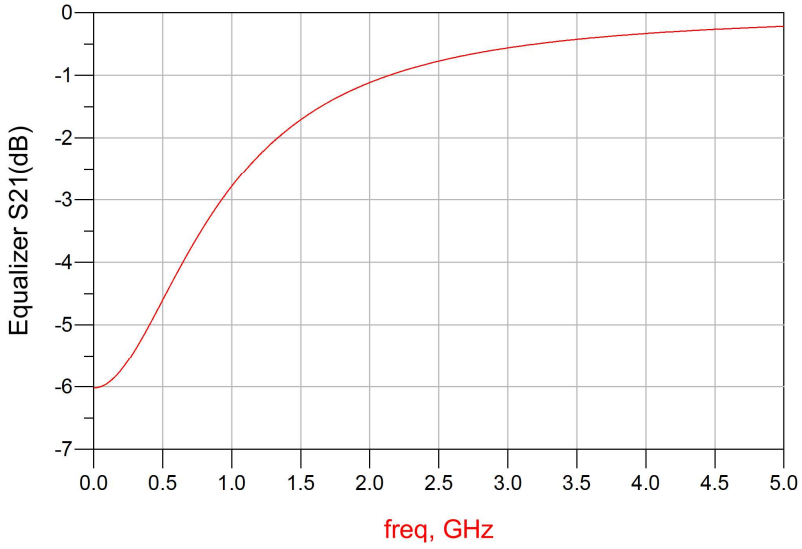


Figure 4.4 S_{21} of equalized channel

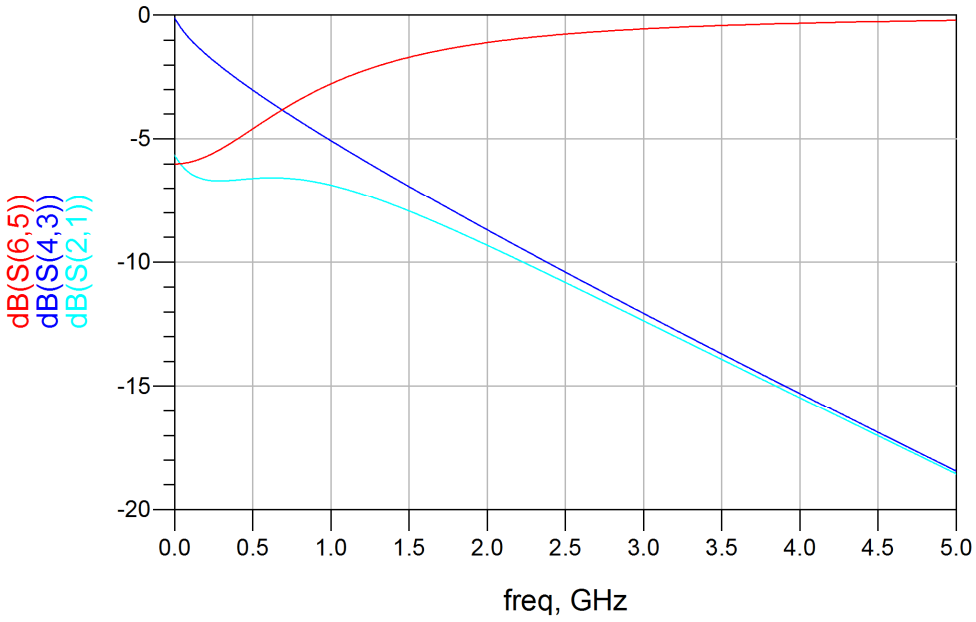


Figure 4.5 Comparison of S_{21}

4.3 Post-Emphasis:

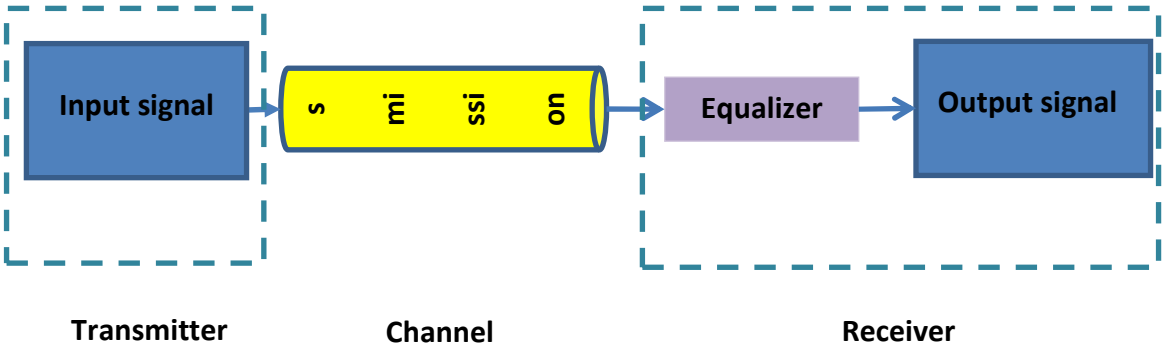


Figure 4.6 Post-emphasis block diagram

Figure 4.6 shows the block diagram for a post-emphasis signal extracting system, where the signals are compensated after losing high frequency signals in the transmission section.[3]

4.4 Pre-Emphasis:

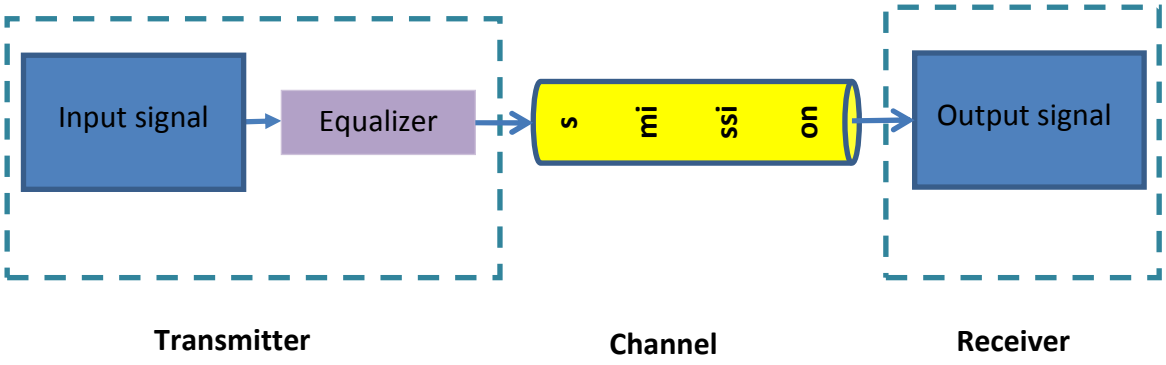


Figure 4.7 Pre-Emphasis block diagram

If a boost circuit designed at the transmitter part is placed at the beginning of the transmission line to pre-compensate the magnitude of a signal, this technique equalizes the signal for a lossy channel. As displayed in Figure 4.7, this equalization technique is called “pre-emphasis. Sometimes it is also called “de-emphasis.”[5]

Chapter 5

PCIe Bus system and eye diagram

5.1 PCI Express

PCI (Peripheral Component Interconnect) express, also named as PCI-E, or officially as PCIe, is one of high-speed serial bus standards on the computer motherboard. It is designed to replace older bus such as AGP (Accelerated Graphics Port), and PCI bus standards. Intel leads this standard to the third generation (PCIe 3.0) of bus systems. PCIe 3.0 is compatible to previous generation, and it provides better transmitting speed and higher power supply after raising the configuration to 3.3 V/3 A + 12 V/5.5A.

Table 5-1 PCIe Version[15]

Ver.	Bus bandwidth	Unidirectional Single channel bandwidth	Bidirectional16 channel bandwidth	Transfer rate
1.0	2Gb/s	250MB/s	8GB/s	2.5GT/s
1.0a	2Gb/s	250MB/s	8GB/s	2.5GT/s
1.1	2Gb/s	250MB/s	8GB/s	2.5GT/s
2.0	4Gb/s	500MB/s	16GB/s	5.0GT/s
2.1	4Gb/s	500MB/s	16GB/s	5.0GT/s
3.0	8Gb/s	1GB/s	32GB/s	8.0GT/s
4.0	16Gb/s	2GB/s	64GB/s	16.0GT/s

The characteristics of different version PCIe bus systems are summarized in **Error! Reference source not found.**Table 5-1, where the PCIe bandwidths are calculated in the following way:

The PCIe serial bus bandwidth (MB/s) is equal to the serial bus clock frequency (MHZ) multiplying the serial bus bit width (bit/8=B), multiplying the number of lane, multiplying the encode method, and multiplying the cycle per clock.

For example, PCIe 1.0 X1 bandwidth = 2500×1/8×1×8/10×1×2=500 MB/s

5.2 Eye diagram

Eye diagram is a powerful time domain analysis tool for digital signals, which looks like a human eye. It can show digital signal errors in time and power, respectively, because it is hard to quantify the digital errors in the real world, such as jitter, due to their rapid change in timing bit positions and amplitudes.

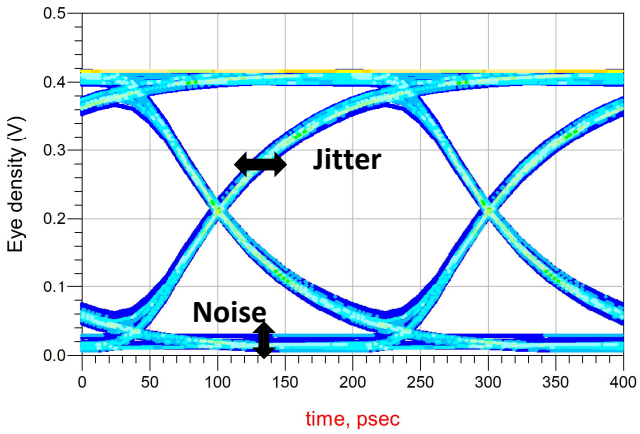


Figure 5.1 Jitter and noise

When the jitter error increases, the eye opening becomes smaller. There are two definitions of the white space as plotted in Figure 5.1: one is the eye width and the other one is the eye height.[8]

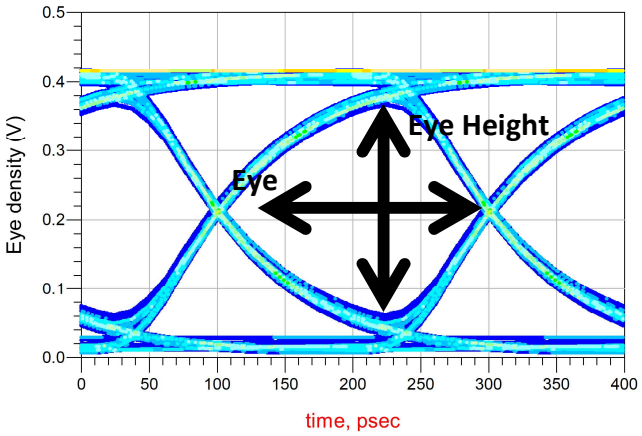


Figure 5.2 Eye height and eye width

The width of this white space is defined as the eye width, which shows how the unit interval data transits. The eye height is named as the height of this white space,

which implies the VIH and VIL level of a digital signal receiver. These definitions provide the fundamental information to judge digital signals and to build up better digital data transition and quality.

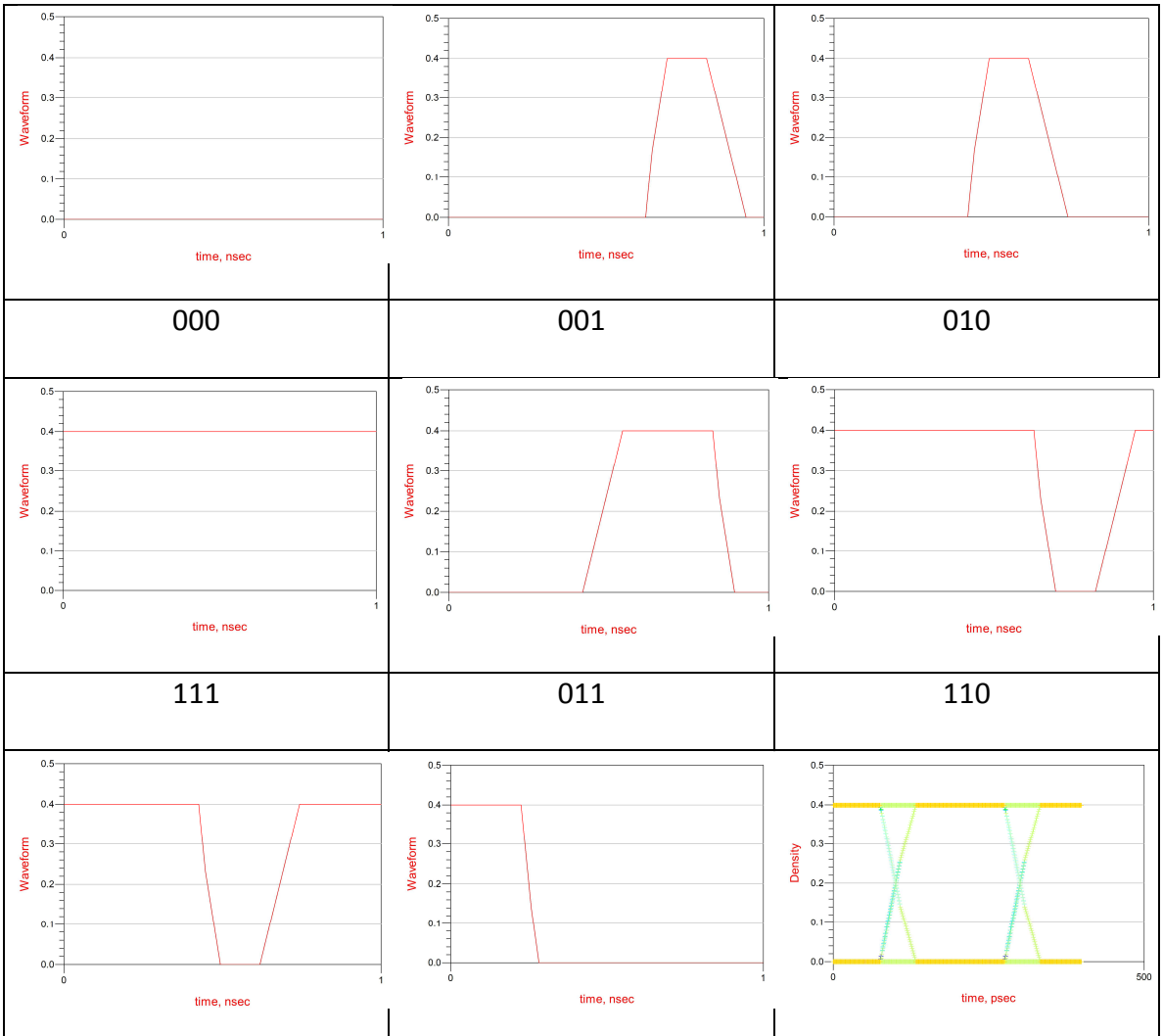


Figure 5.3 Conformation of eye diagram

The high frequency circuit design usually uses “eye diagram” and “jitter” to evaluate received digital signals. Figure 5.3 shows the different transitions of three bits

and these are the basic structures of the eye diagram data bit combinations. The bit patterns shown above, all the possibility of transition of data “0” and “1” and digital signals overlaps for a long period of time.

The reliability and accuracy of digital communication is based on the quality of digital signals, which can be clearly represented in an eye diagram.

5.3 PRBS

PRBS is an abbreviation for the Pseudo Random Binary Sequence, which is a “fake” random binary sequence. PRBS contains random binary signals “0” and “1”, and it is derived from a linear feedback shift register (LFSR) that connects with a multiple shift register.

The main idea of LFSR is a shift of the serial digital binary signals based on the first data set.

5.3.1 LFSR

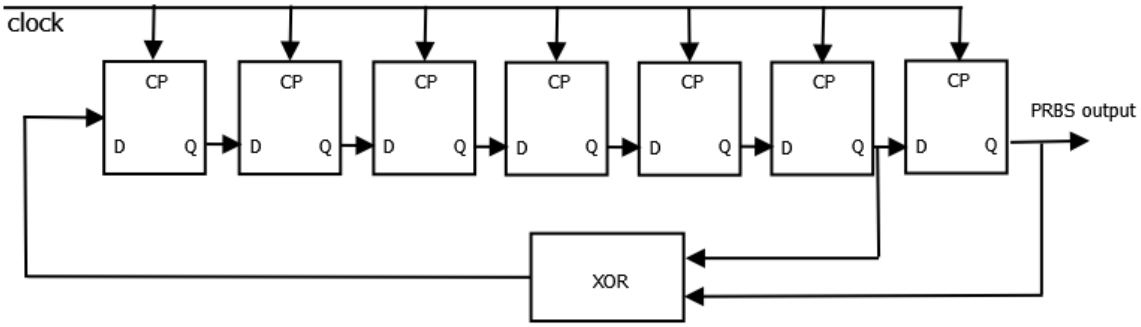


Figure 5.4 2^7-1 PRBS generator

LFSR is the real logical circuit for the PRBS generator, and its structure is built in shift registers and XOR gates as seen in Figure 5.4. Figure 5.5 shows a PRBS generator built in ADS system, which is frequently used in this research

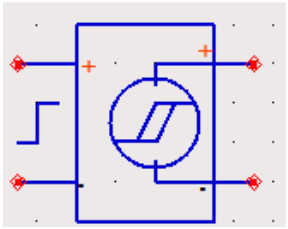


Figure 5.5 PRBS generator in ADS[14]

5.4 Digital signal analysis

Digital signals can be classified as pulse, step, and trapezoidal signals, and the trapezoidal signal pulse is frequently used as an input signal in most cases. The spectrum amplitude of trapezoidal signal is expressed as below:

$$C_0 = A\frac{\tau}{T} \qquad (5\text{-}1)$$

$$C_n = A\frac{\tau}{T}\frac{\sin\left(\frac{n\omega_0\tau}{2}\right)}{\frac{n\omega_0\tau}{2}}\frac{\sin\left(\frac{n\omega_0\tau_r}{2}\right)}{\frac{n\omega_0\tau_r}{2}}\mathrm{e}^{-\frac{\mathrm{j}n\omega_0(\tau+\tau_r)}{2}} \quad (5\text{-}2)$$

The spectrum distribution is shown as Figure 5.6. The spectrum decays 20dB/dec after the frequency is $\frac{1}{\pi\tau}$, and it decades 40dB/dec after the frequency is $\frac{1}{\pi\tau_r}$.

Figure 5.6 Envelope of trapezoidal signal spectrum[9]

Chapter 6

Passive Equalizer Topology Analysis

6.1 RLC equalizer analysis

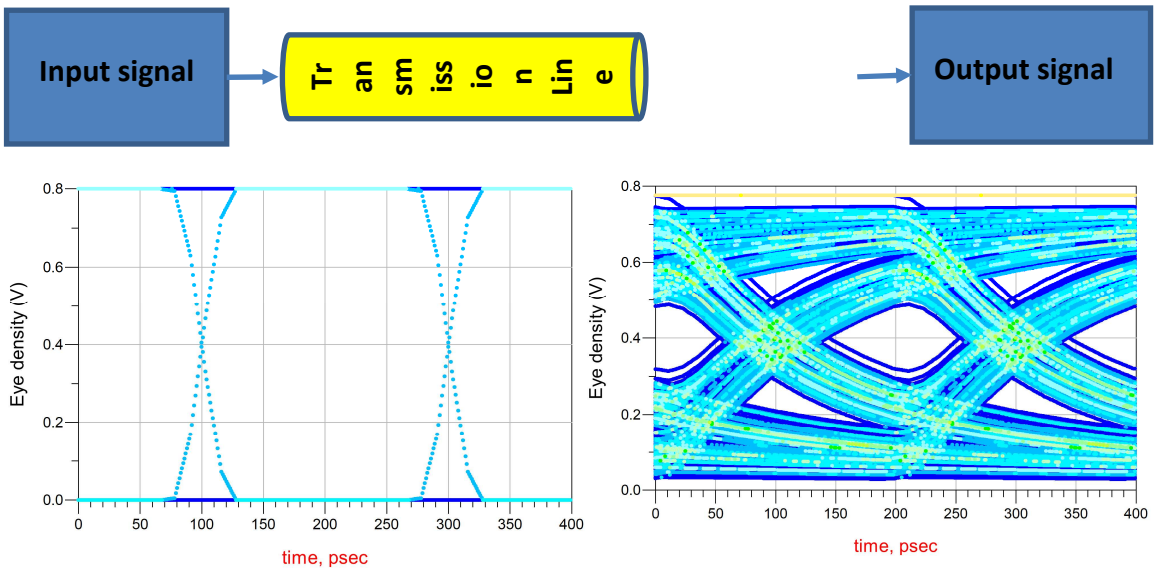


Figure 6.1 Schematic diagram of a lossy channel

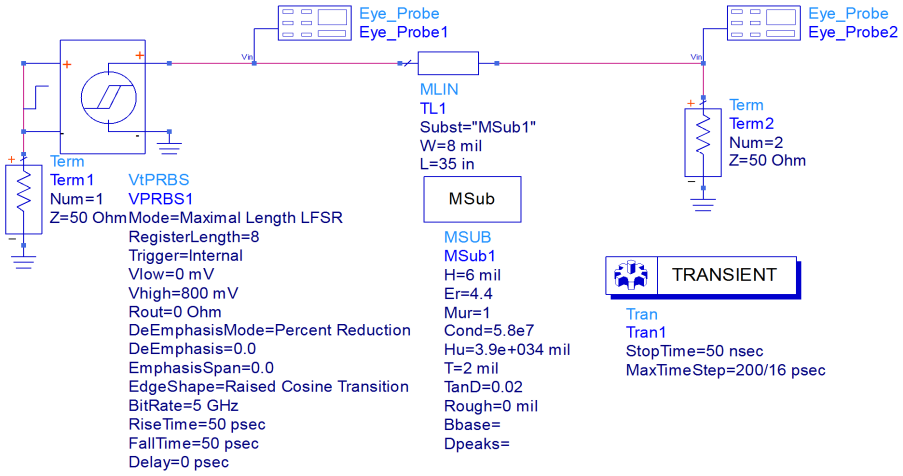
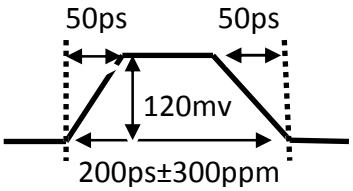


Figure 6.2 Simulation setup in ADS

The equalizer analysis system is set up as shown in Figure 6.1 and Figure 6.2, and PCIe Gen2 standard is used in the simulation model as briefly summarized in Table 6-1.

Table 6-1 Standard for the PCIe Gen2.0 channel[10]

TX(800 mv, 5Gbps)	RX	
Unit Interval	200ps±300ppm	
Eye Width	0.4 UI=80ps	
Jitter	0.6 UI=120ps	
Eye Height	120 mv	
Rise time	50ps	
Fall time	50ps	

In simulation, the amplitude of input signal is set to be 800 mV, and total number of digital signals is a $2^8 - 1$ PRBS data set in 5Gps transmission rate. Moreover, in order to make the digital signals readable by receivers, the unit intervals of signals are limited to be 200ps±300ppm, the eye width of 0.4 UI (unit interval) is required, and the eye height of 120mv is needed.

The channel is built up with the microstrip line structure, and the substrate is FR4.

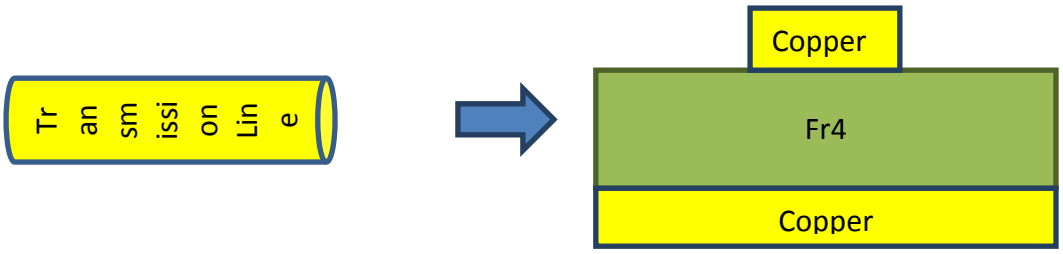


Figure 6.3 Schematic diagram of the transmission line

Table 6-2 Parameters of transmission line[11]	
ε_r	4.4
μ_r	1
conductivity	5.8e7
tanD	0.02
Height of substrate	5 mil
Thickness of transmission line	2 mil
Width of transmission line	8 mil

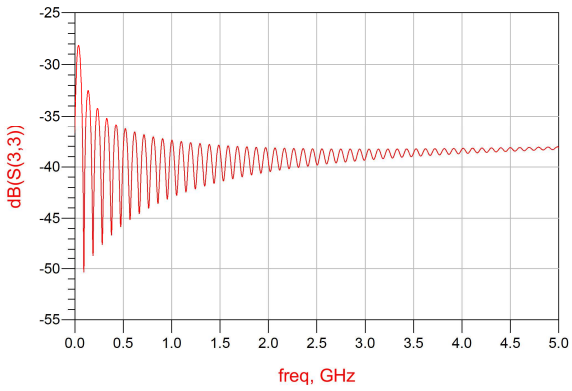


Figure 6.4 S_{11} of transmission Line

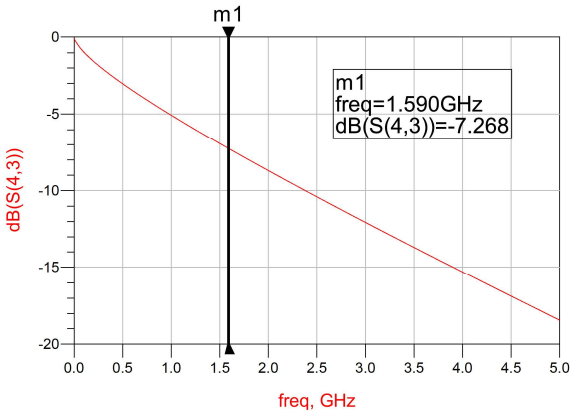


Figure 6.5 S_{21} of transmission Line

An important characteristic for a propagation channel is S_{21}, which determines the propagation and attenuation of the channel. It can also help us to understand matching level between a bus transmission line and a load. The cutoff frequency is $\frac{1}{\pi\tau}$(1.59GHz) because the 20 dB decay occur after $\frac{1}{\pi\tau}$.

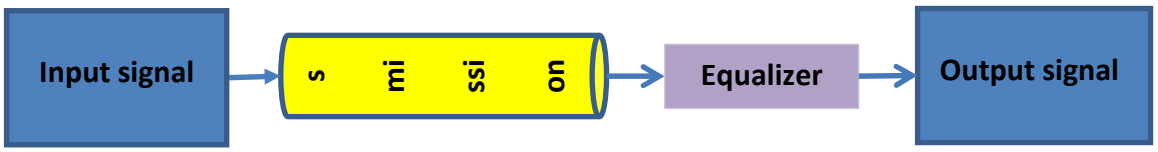


Figure 6.6 Schematic diagram of simulation

6.1.1 RC equalization circuit

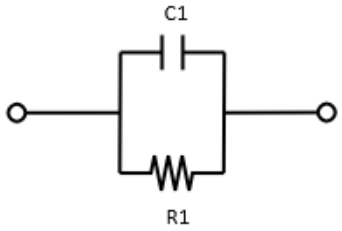


Figure 6.7 Shunt RC circuit

First, a simple RC[12] equalization circuit is studied, where the shunt RC circuit is applied as equalizer to cancel ISI. By tuning the values of the capacitance and resistance, a better matching can be achieved in order to meet the eye height of the standard.

Table 6-3 Data set of RC circuit

Eye height (mv)	105	142	173	198	216
Eye width(ps)	136	154	158	168	164
R(Ω)	50	50	50	50	50
L(nH)	1	2	3	4	5

It is found that the desirable eye height can be achieved by increasing the capacitance when R is fixed at 50 Ω. Meanwhile, it is also found that reflection increases as capacitance increment as shown in Figure 6.8 and Figure 6.9. As a result, the eye opening becomes improved when the capacitance increases from 1 pF to 5 pF.

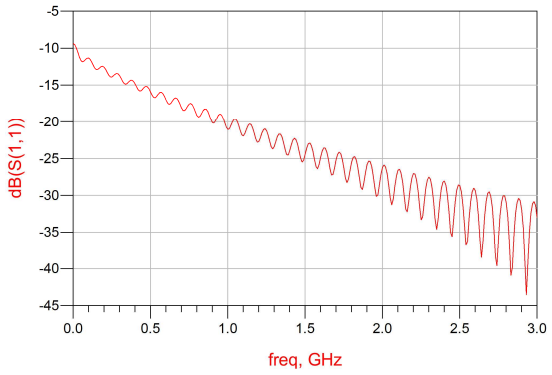


Figure 6.8 S_{11} of RC equalizer(C=1pF)

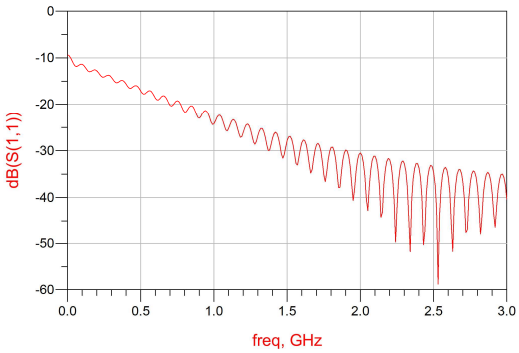


Figure 6.9 S_{11} of RC equalizer(C=5pF

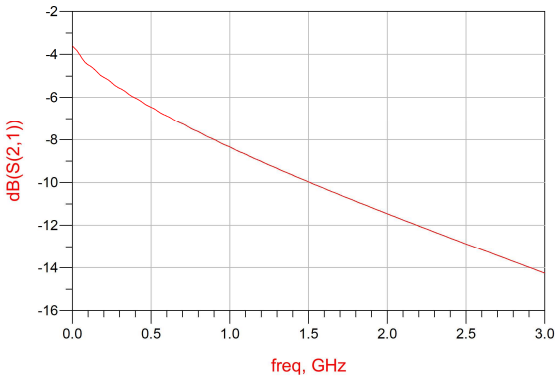


Figure 6.10 S_{21} of RC equalizer(C=1pF)

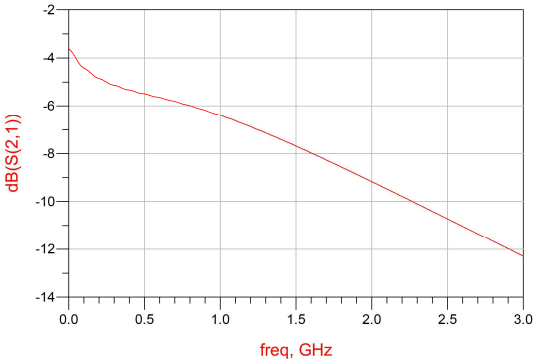


Figure 6.11 S_{21} of RC equalizer(C=5pF)

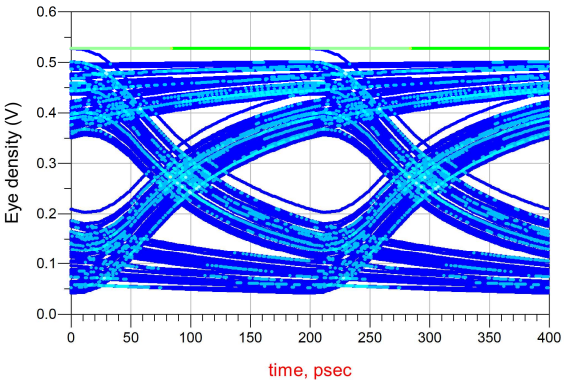


Figure 6.12 Eye diagram of RC equalizer(C=1pF)

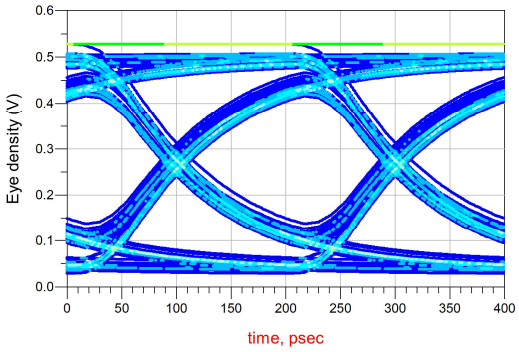


Figure 6.13 Eye diagram of RC equalizer(C=5pF)

6.1.2 RL equalization circuit

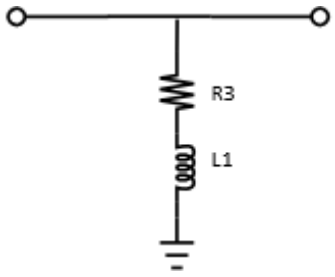


Figure 6.14 Series RL circuit

A RL equalizer circuit[11] is shown in Figure 6.14, where assume R_3 is mainly used for matching the connected transmission line. And the series connected inductance is for compensation of high frequency loss. The parameters of the RL circuit are summarized in Table 6-4.

Table 6-4 Data set of RL circuit

Eye height (mv)	101	140	157	160	158
Eye width(ps)	155	171	181	176	174
R(Ω)	50	50	50	50	50
L(nH)	5	10	15	20	25

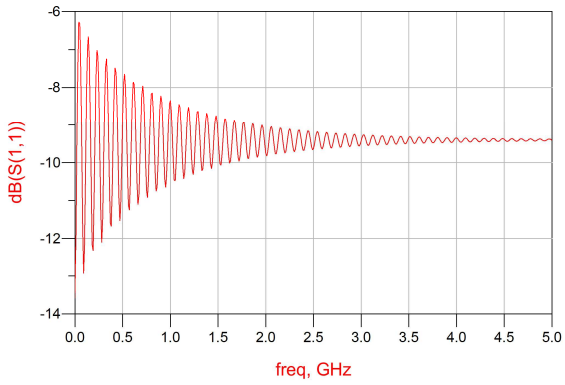


Figure 6.15 S_{11} of RL equalizer(L=5nH)

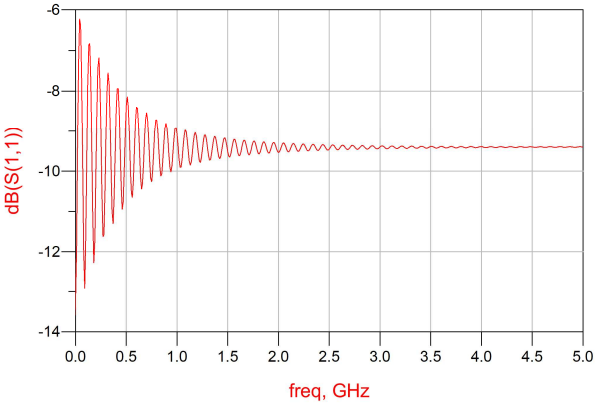


Figure 6.16 S_{11} of RL equalizer(L=25nH)

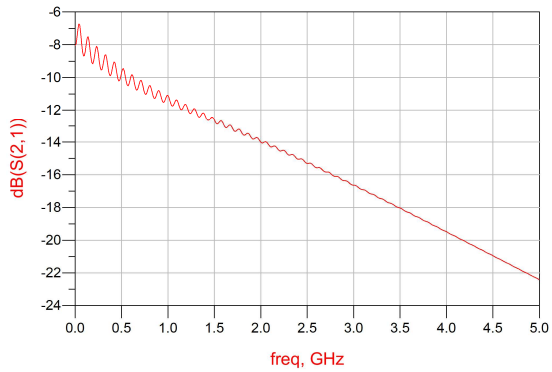


Figure 6.17 S_{21} of RL equalizer(L=5nH)

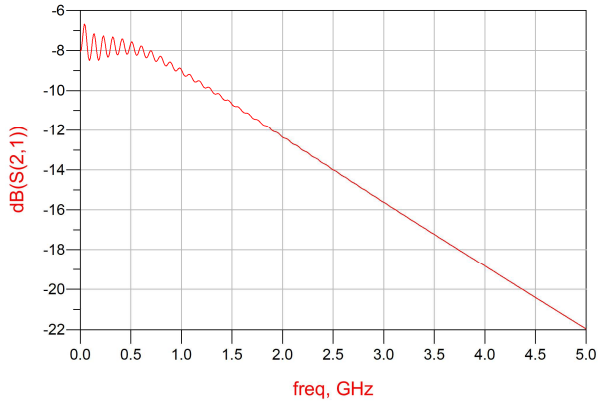


Figure 6.18 S_{21} of RL equalizer(L=25nH)

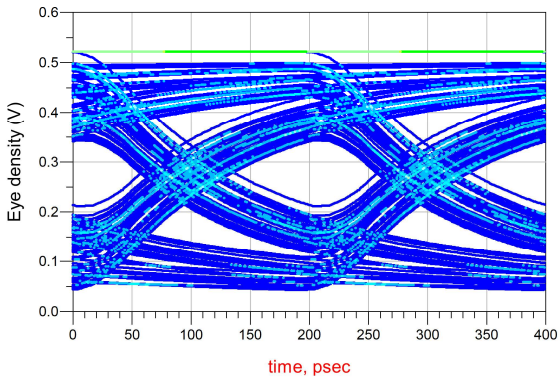


Figure 6.19 Eye diagram of RL equalizer(L=5nH)

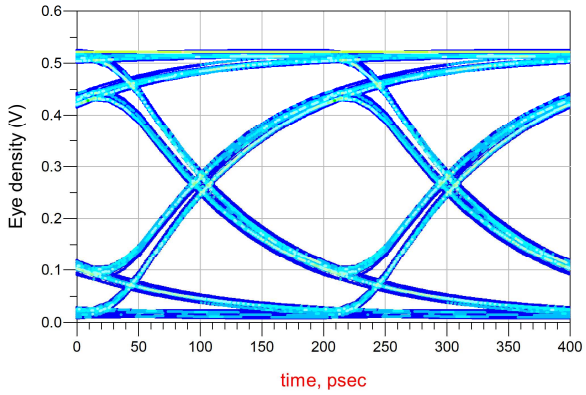


Figure 6.20 Eye diagram of RL equalizer(L=25nH)

It is found that as increasing inductance, the reflection can be reduced less after extensive simulation experiments. However, it still not meets the standard of eye height. An equalizer is designed with combination of shunt RC and series RL circuits, as seen Figure 6.21 and Figure 6.22, as a new topology as displayed Figure 6.23, to improve eye diagram.

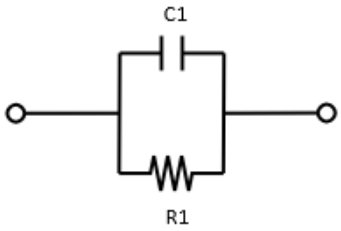


Figure 6.21 RC circuit

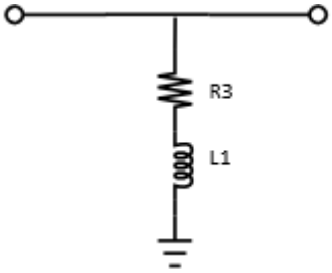


Figure 6.22 RL circuit

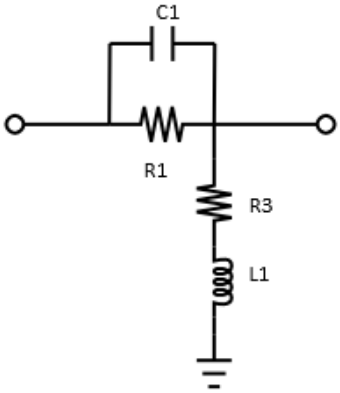


Figure 6.23 RLC circuit

The T network[1] circuit shown in Figure 6.24 is often used to determine the transfer function of equalizer system, and equation (6-1) is the transfer function of T network represented in the ABCD matrix.

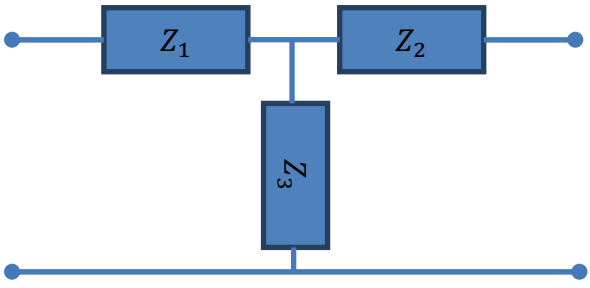


Figure 6.24 T network

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1+\frac{Z_1}{Z_3} & Z_1+Z_2+\frac{Z_1Z_2}{Z_3} \\ \frac{1}{Z_3} & 1+\frac{Z_2}{Z_3} \end{bmatrix} \quad (6\text{-}1)$$

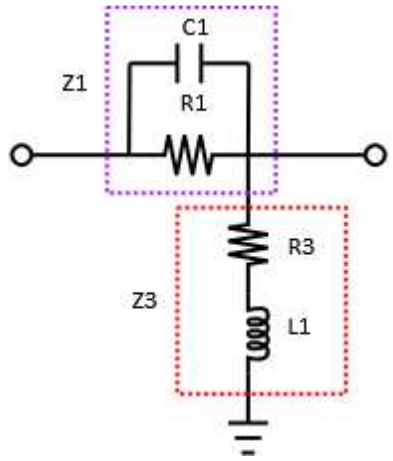


Figure 6.25 Z_1 and Z_3

Table 6-5 S_{11} and S_{21} of RLC Design

	S_{11}	S_{21}
Maxim	$\frac{R_1(z_0+z_3)-{z_0}^2}{2z_0z_3+R_1(z_0+z_3)+{z_0}^2}$	$\frac{2z_0z_3}{2z_0z_3+R_1(z_0+z_3)+{z_0}^2}$
Agilent	$\frac{2z_1z_3+{z_1}^2-{z_0}^2}{2z_0z_3+2z_1z_0+2z_1z_3+{z_1}^2+{z_0}^2}$	$\frac{2z_0z_3}{2z_0z_3+2z_1z_0+2z_1z_3+{z_1}^2+{z_0}^2}$
This design	$\frac{z_1(z_0+z_3)-{z_0}^2}{2z_0z_3+z_1(z_0+z_3)+{z_0}^2}$	$\frac{2z_0z_3}{2z_0z_3+z_1(z_0+z_3)+{z_0}^2}$

It is noted that the first design idea is referenced to a Maxim similar topology[13], the second one is comparable Agilent's circuit[6], and the third topology is purely

combination of RC and RL equalization circuits. After optimization tests, the derived parameters summarized as shown in Table 6-6.

Table 6-6 Parameter of equalizer designs

	R1(Ohm)	R2(Ohm)	R3(Ohm)	C1(pF)	L1(nH)
Maxim	70		450	6	
Agilent	18	18	55	6	18
This Design	23		55	7	18

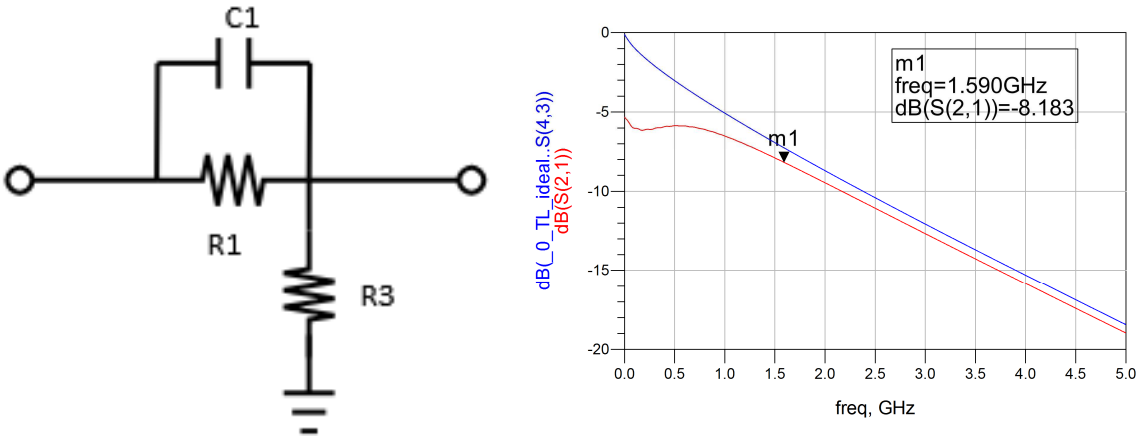


Figure 6.26 Maxim equalizer circuit with the topology and S_{21}.

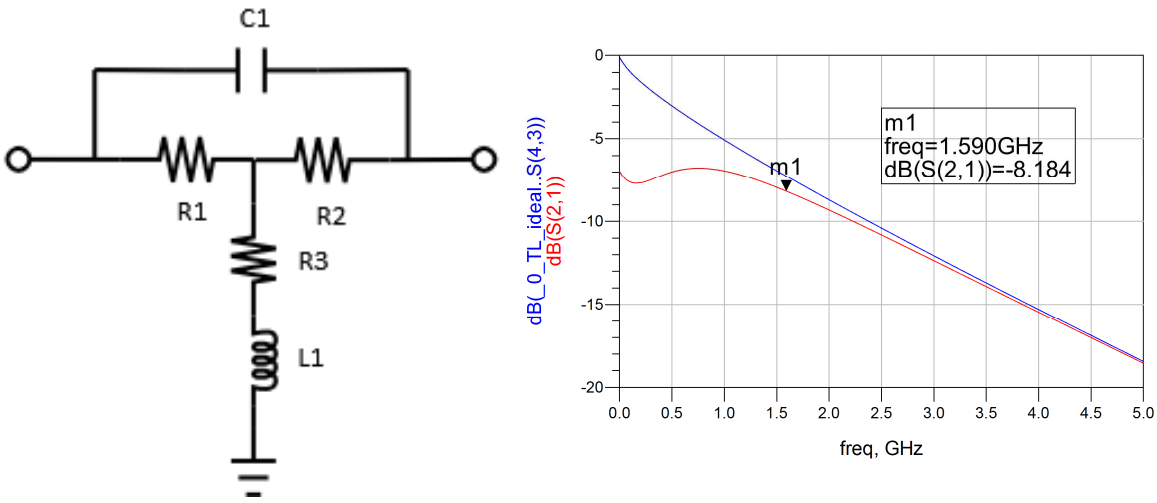


Figure 6.27 Agilent equalizer circuit with the topology and S_{21}.

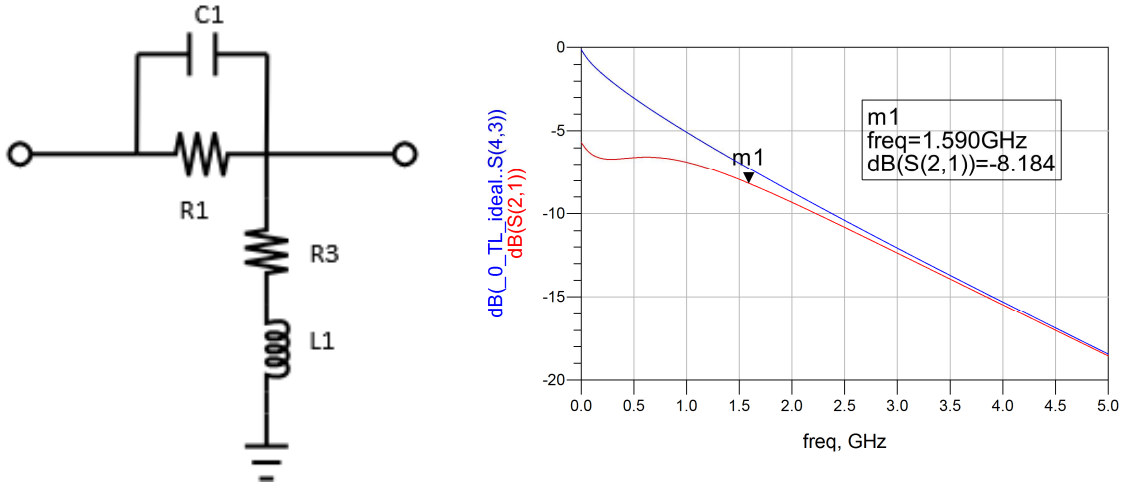
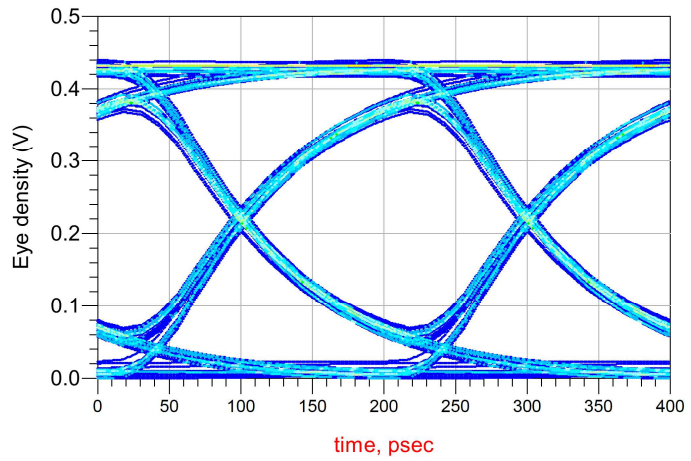


Figure 6.28 This design's topology and S_{21}.

Level 0	0.044
Level 1	0.406
Eye height	0.241
Eye width	1.86E-10



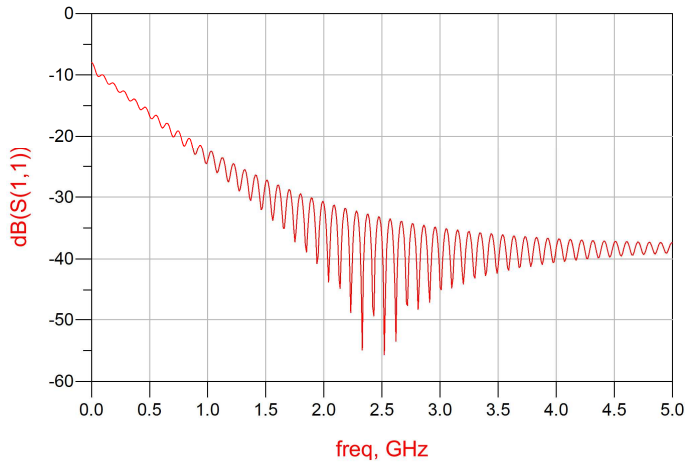
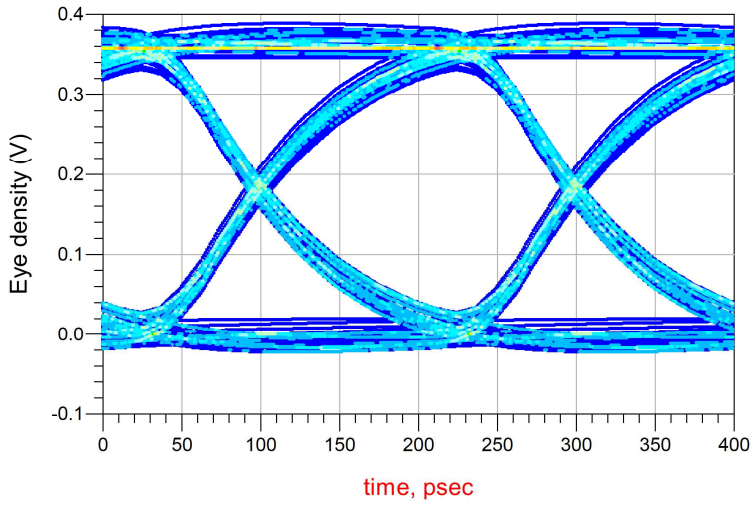


Figure 6.29 Maxim (eye diagram and S_{11})

Level 0	0.014
Level 1	0.352
Eye height	0.245
Eye width	1.83E-10



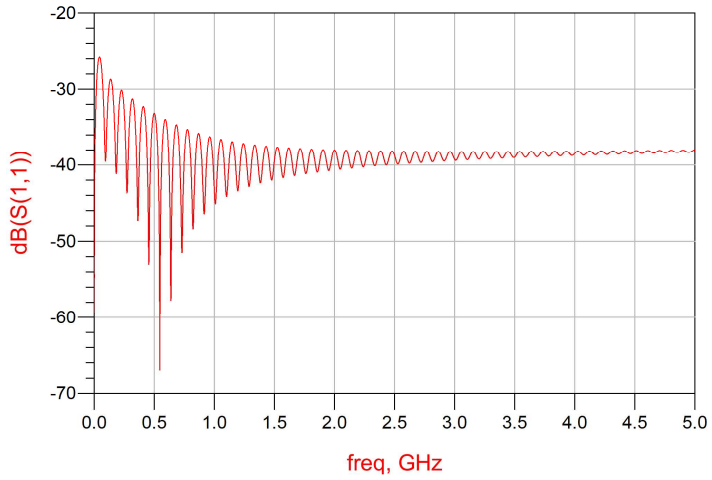
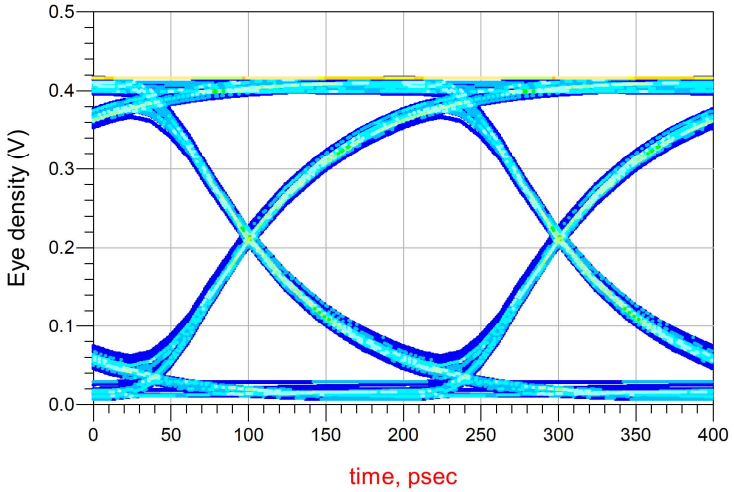


Figure 6.30 Agilent (eye diagram and S_{11})



Level 0	0.041
Level 1	0.393
Eye height	0.243
Eye width	1.90E-10

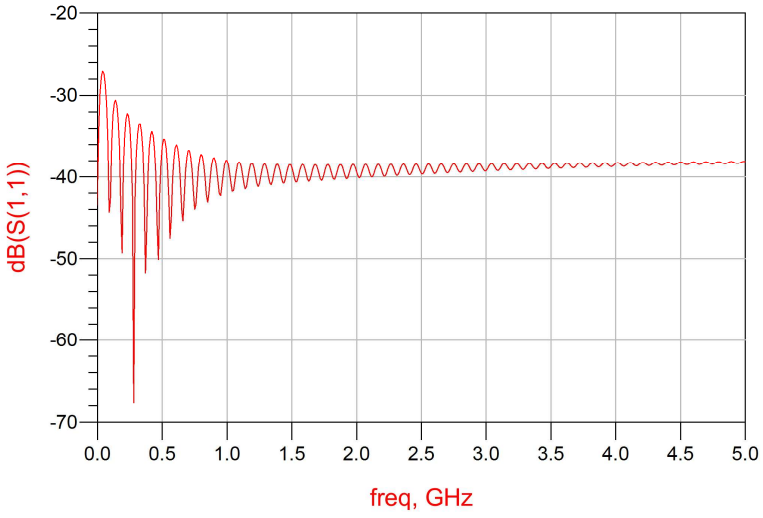


Figure 6.31 This design (eye diagram and S_{11})

As seen fromTable 6-6, the introduce of inductance to the equalizers makes the resistance values become smaller and easily applicable in the circuits. It is also found that the added inductance reduces the reflection from the terminal interconnects. The proposed design in the research provides less reflection without adding resistance R_2.

6.2 Length tolerence estimation

In this section, the cross section configuration of the transmission lines remain the same parameters as those discussed previously the lossy propagation channel is integrated with a shunt RC and a series RL as a compensation circuit as seen Figure 6.32.

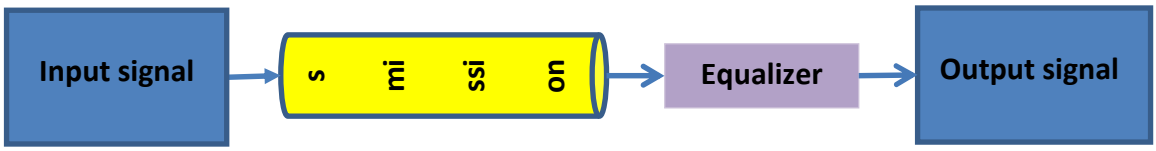


Figure 6.32 Block diagram of simulation model

In the simulation tests with different lengths of transmission lines, it is found that even with the longest length of the transmission line up to 50 inches digital signals are still readable for the equalized systems.

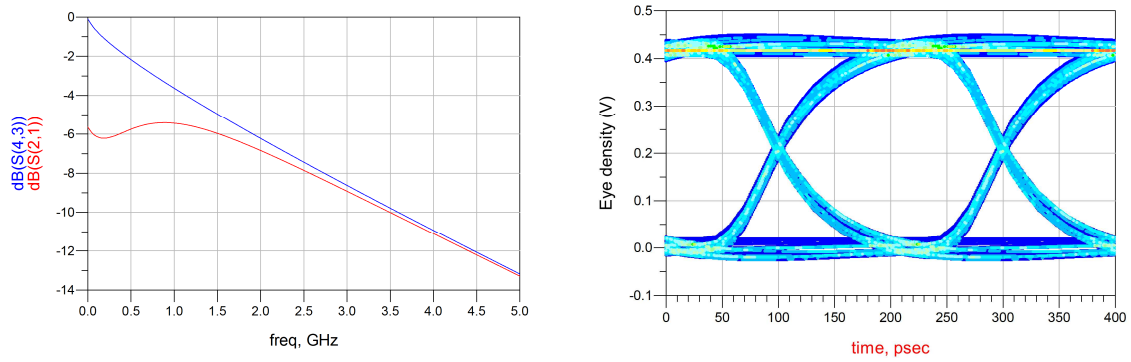


Figure 6.33 S_{21} and eye diagram of 25 inch

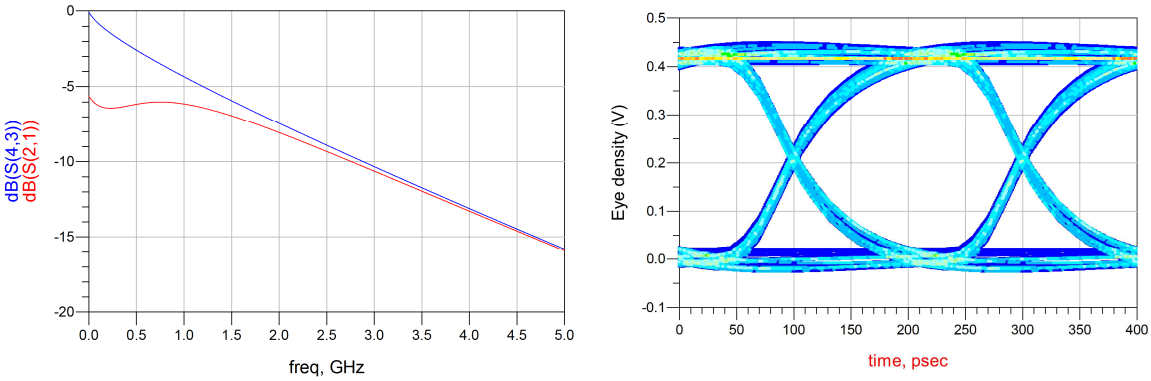


Figure 6.34 S_{21} and eye diagram of 30 inch

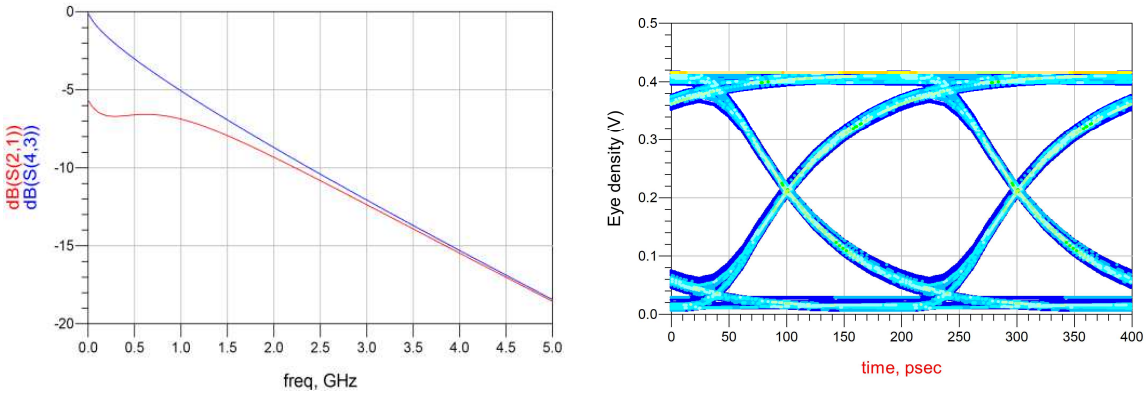


Figure 6.35 S_{21} and eye diagram of 35 inch

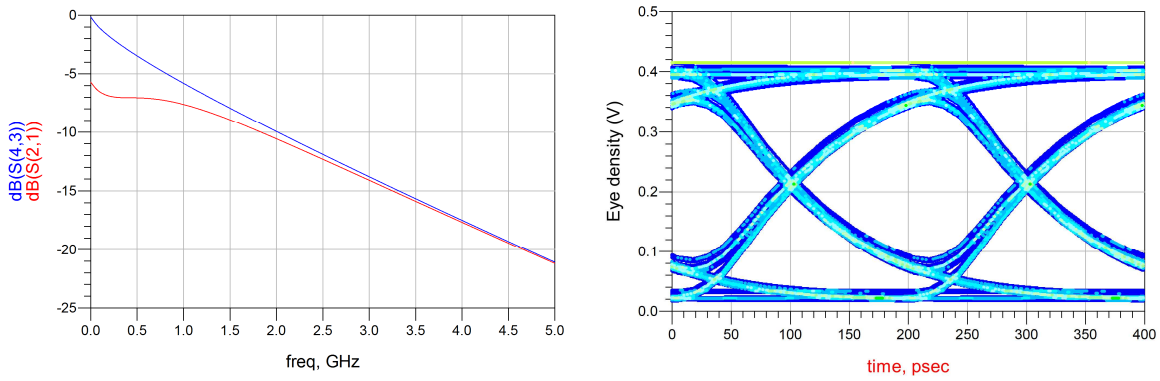


Figure 6.36 S_{21} and eye diagram of 40 inch

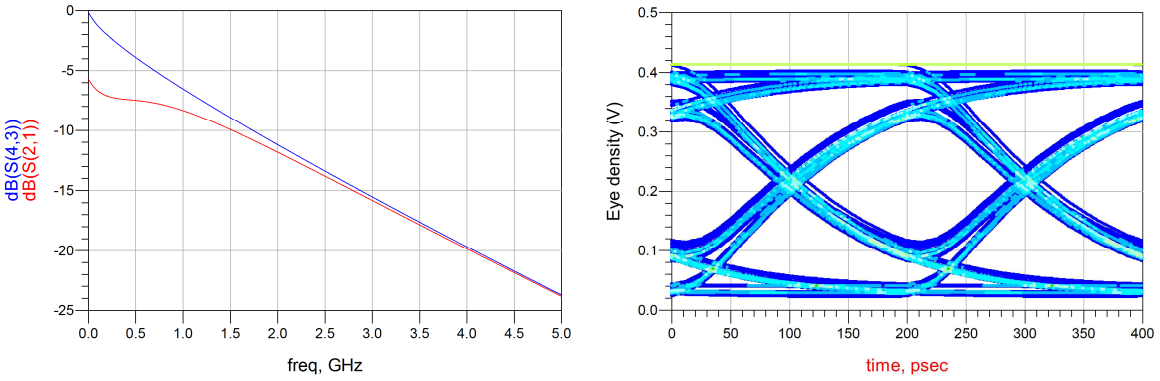


Figure 6.37 S_{21} and eye diagram of 45 inch

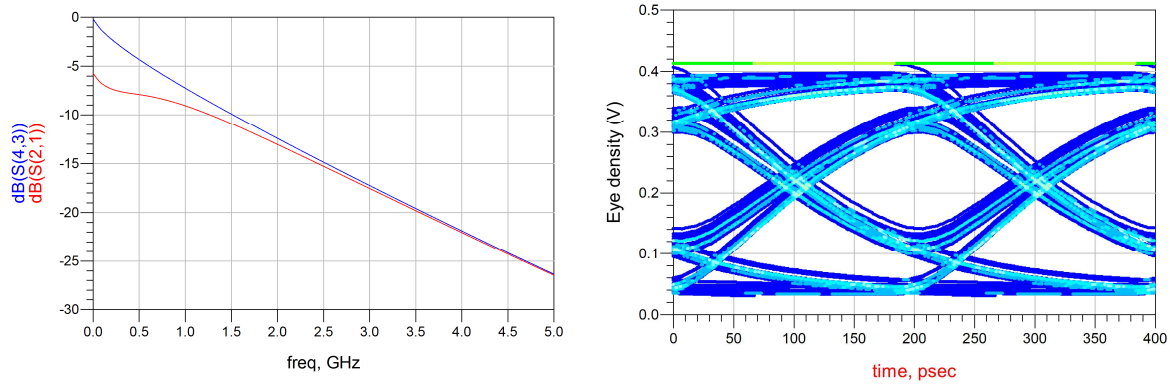


Figure 6.38 S_{21} and eye diagram of 50 inch

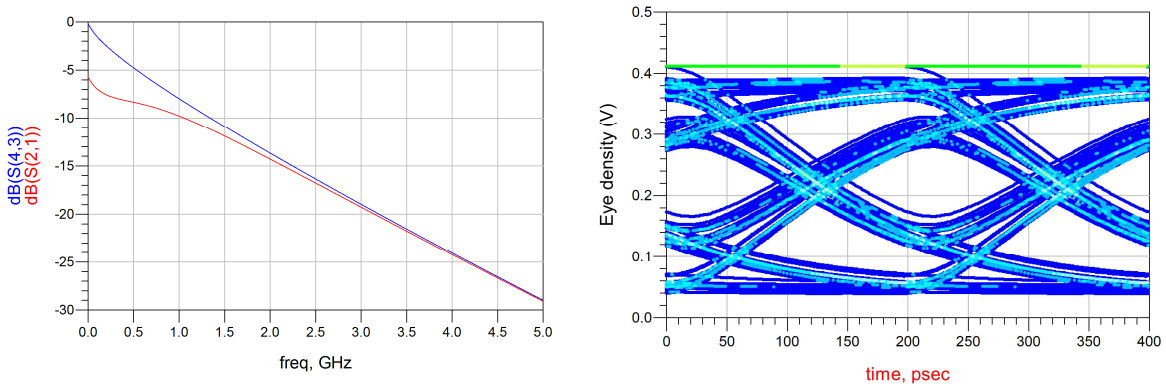


Figure 6.39 S_{21} and eye diagram of 55 inch

From the eye digram for different lengths of transmission lines, it is easily seen that logger lengths of the transmission lines can distort the signals are hard to recognize received digital signal. Figure 6.33 presents the 25 inch channel showing a better quality of the eye diagram, which apparently shows that a shorter media present less loss and the associated digital signals are readable with using the equalizer. When the lossy channel length increase more signal loss and time delay of data signals are observed, by comparing the S_{21} curves from Figure 6.33 through Figure 6.39.

Furthermore, from the table on the left of Figure 6.33 to Figure 6.38, it is seen that the total S_{21} for each case becomes skewer from the top to the bottom because the equalizer cannot provide the function of equalization for the system. The blue line is the limit where the eye is closed, and the red is away from the blue line which means the distortion increase by the distance of interconnects.

Table 6-7 Simulation result of different distance

	Eye Height	Eye Width	Eye Level 0	Eye Level 1

25 inch	0.342	1.91e-10	0.005	0.417
30 inch	0.285	1.93e-10	0.024	0.404
35 inch	0.243	1.90e-10	0.041	0.393
40 inch	0.212	1.83e-10	0.056	0.386
45 inch	0.170	1.65e-10	0.070	0.378
50 inch	0.138	1.46e-10	0.084	0.372
55 inch	0.096	1.40e-10	0.100	0.367

6.3 Equalizer's pre-emphasis

The same topology as given Figure 6.28 and same parameters summarized in Table 6-6 are used to investigate the pre-emphasis and post-emphasis techniques.

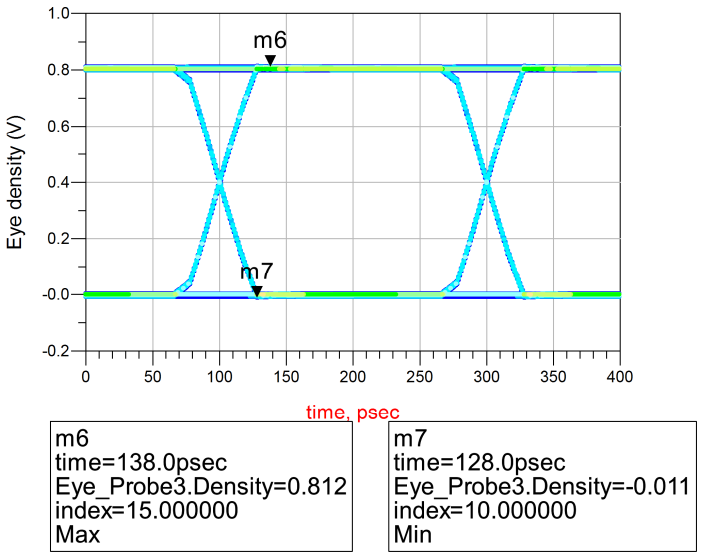


Figure 6.40 PRBS input signal

Post-emphasis

In the post emphasis, an equalizer is placed after the propagation channel as displayed in Figure 6.41.

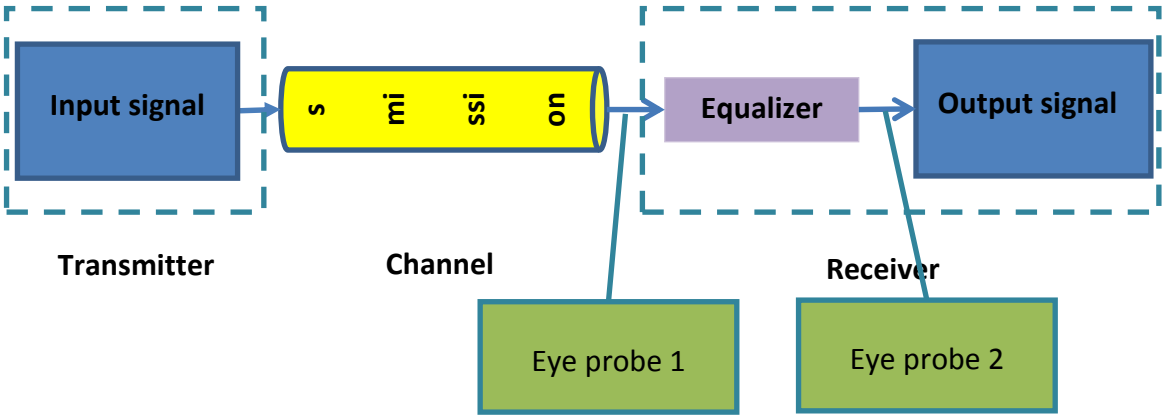


Figure 6.41 Post-emphasis

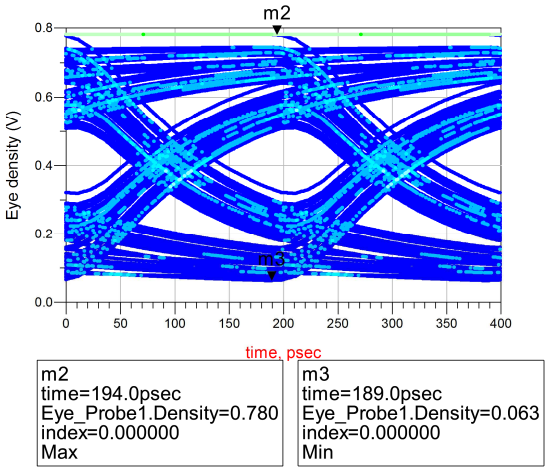


Figure 6.42 Eye diagram of input port of the channel(Eye probe 1)

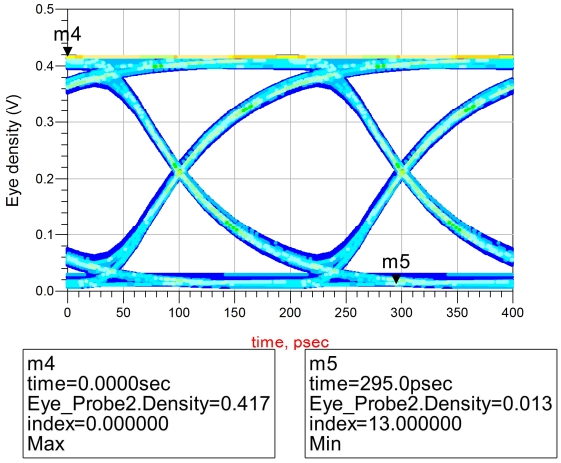


Figure 6.43 Eye diagram of output port of the channel(Eye probe 2)

The previous topology circuits primarily use the post-emphasis technique to improve the signal and correct the eye in order to acquire the best performance of the system. The same qaualizer can locate before the transmission channel in the system as Figure 6.44, which is called as the de-emphasis or pre-emphasis.

Pre-emphasis

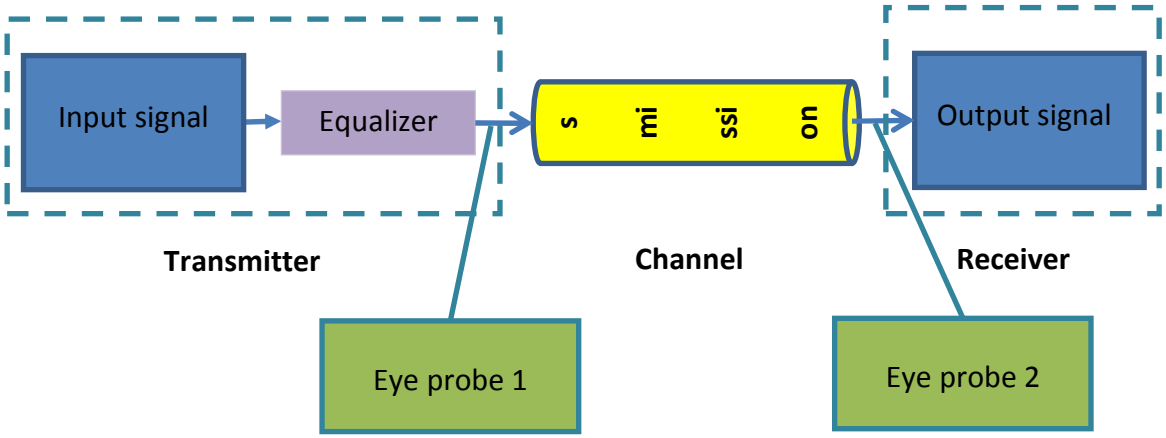


Figure 6.44 Block diagram of Pre-emphasis

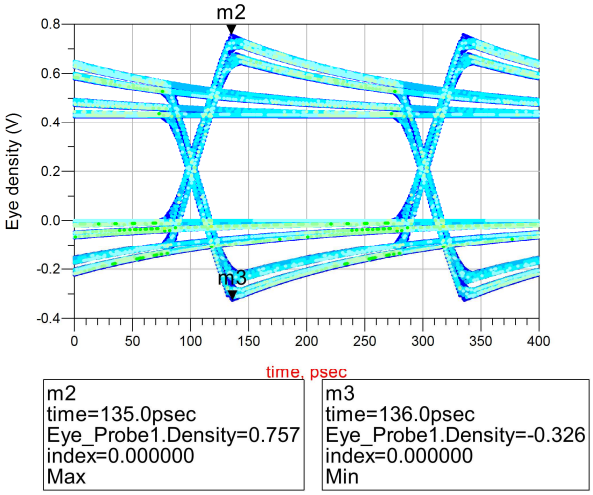


Figure 6.45 Eye diagram of input port of the channel (Eye probe 1)

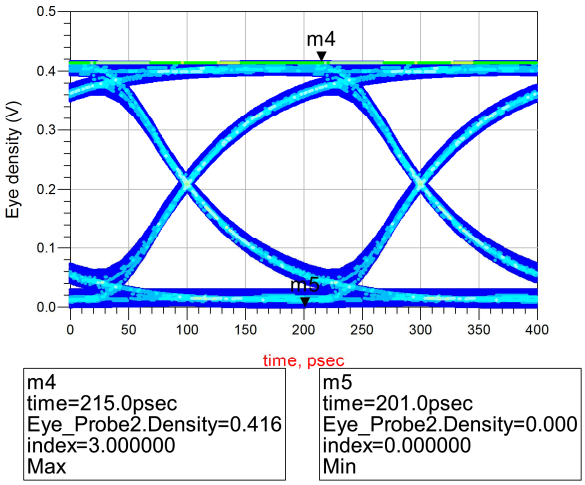


Figure 6.46 Eye diagram of output port of the channel (Eye probe 2)

As seen Figure 6.45, signals are to input the equalizer first and the corresponding eye diagram is boosted in high frequency. The max value is 0.757v and the min value is -0.326v. 1.083v is the summation of these two values. By comparing the PRBS generator,

0.283 mv is the difference from generator. Moreover, the signal increased 0.283mv (35.3%) from the original signals.

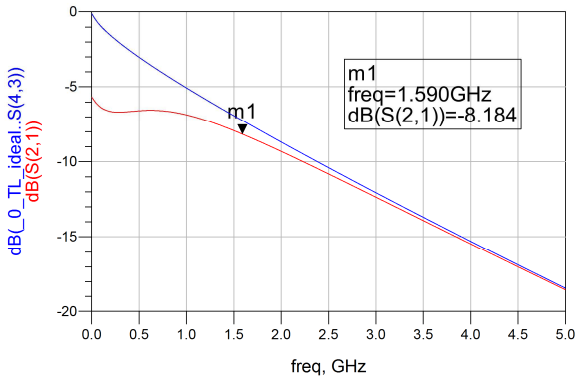


Figure 6.47 S_{21} for Post-emphasis system

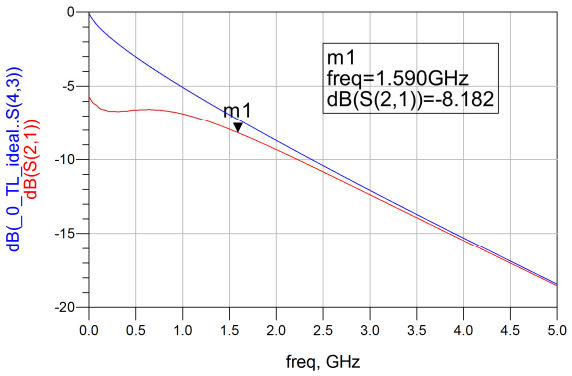


Figure 6.48 S_{21} for Pre-emphasis system

Chapter 7

Conclusion

In this thesis, the various RC equalization schematic topology circuits are analyzed and compared for signal integrity applications. The proposed RC equalizer reaches the expected eye height and width, and it is found that the signal levels with the RC equalizer are reduced due to addition of signal reflection at the receiver end. It is also found that the RL equalization circuit provides clear eye opening but the improvement is not significant. The combination of RC and RL equalizers exhibits a better eye diagram along a lossy transmission channel while remaining less signal terminal reflection. It has to be mentioned that the inductance added to the design can effectively decrease the reflection, but it increases the dimensions of PCB design.

The proposed equalizer design not only gets the less reflection from the device, but also reduces the number of components. For a more complicated or lengthy trace, it needs adding amplifiers to achieve higher data rates and improve signal integrity.

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