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Technology Development and Characterization of AlInN/GaN HEMTs for High Power Application

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ABSTRACT

AlInN has attracted much attention only recently as a material due to its unique and superior material properties, which is however known to be difficult to be grown among the III-nitride ternary compounds. The electrons confined at the heterointerface of coherently grown AlInN on GaN buffer layers determine crucial electronic properties. This dissertation has been designed targeting the lattice matched AlInN/GaN investigation with very detail to optimize the design, fabrication process, and electronic properties to realize AlInN/GaN HEMTs. Each single step of this process was optimized in order to improve device performance.

The work started with establishing the main features of AlInN/GaN heterostructure in a HEMT configuration through optimizing the device fabrication and investigation of the DC characteristics of planar HEMTs. The study included heterostructures with variable barrier thicknesses along with barrier cap layer. A series of experiments were conducted to analyze the impact of barrier thickness on breakdown and threshold-voltage by fabricating devices with different gate to drain separation and incorporating field plated gate design. In addition, a series of experiments were conducted on barrier scaling study of the heterostructure to develop plasma based selective area recess etching to obtain and demonstrate, first ever reported, normally off high threshold voltage AlInN/GaN metal-insulator HEMTs with high current density of 0.7A/mm and high breakdown voltage of 350V and the highest reported threshold voltage of +1.5V. Moreover, investigation of substrate influence was also performed by

fabricating and characterizing AlInN/GaN HEMTs on SiC substrate with different gate dimensions and the transport properties of the devices were discussed.

Next, the device performance has been studied by incorporating Ga in AlInN barrier. Introducing 2% Ga at the AlInN barrier layer is found to increase the current density of about 15% compared to the LM AlInN/GaN HEMTs. This issue has been studied intensively and the preliminary results indicated that even slightest deviations from atomically perfect interfaces leads to the creation of huge piezoelectric fields, increasing the carrier density at the AlInN/GaN interface.

Finally, multifinger AlInN/GaN HEMTs were fabricated to obtain large periphery (LP) devices for high power application. The heart of this work was the design and development of a high yield process technology for high performance LP AlInN/GaN HEMTs. The study of large periphery devices presented the problem of large heat dissipation. Therefore, for future work, new device fabrication and packaging processes for efficient heat dissipation from the top of the device was also proposed.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Silicon semiconductor devices have replaced many conventional electrical parts in the past four decades in a wide spectrum of applications ranging from military applications to civil applications and consumer products. Although silicon is expected to remain as the dominant semiconductor of choice in many applications, wide band gap semiconductors (usually defined as having a band gap larger than 1.7 eV), like GaN, SiC, and Diamond are being investigated as a replacement for silicon technology in some applications, where silicon is reaching its physical limit. These limits are imposed by an increased market need for electronics that are faster, more thermally stable, more robust and more miniaturized and compact, in an era that witnesses the wide spread application of wireless communications like in radars and base stations, and energy conversion like lightening, and optical communication, and information transmission, while at the same time trying to reduce the overall energy consumption and losses. These needs can be met using wide bandgap semiconductors, the properties of which are summarized in Figure 1.1 and Table 1.1.

The difference in the crystal structure and the composition gives rise to different widths of the bandgap, dielectric constants, electron and hole mobilities and saturation velocities and thus fundamentally different electronic properties. But in general, the

properties listed address the fundamental needs mentioned earlier. For example, the wide bandgap of GaN, SiC allows for a higher break down voltage (VBr) enabling the application of higher supply voltages, which makes these materials attractive for high power applications (see Figure 1.2) [1]. Moreover, the larger bandgap makes these materials less susceptible for thermal noise (if the material can be grown with a low trap concentration) and allows operation at higher temperatures [2].

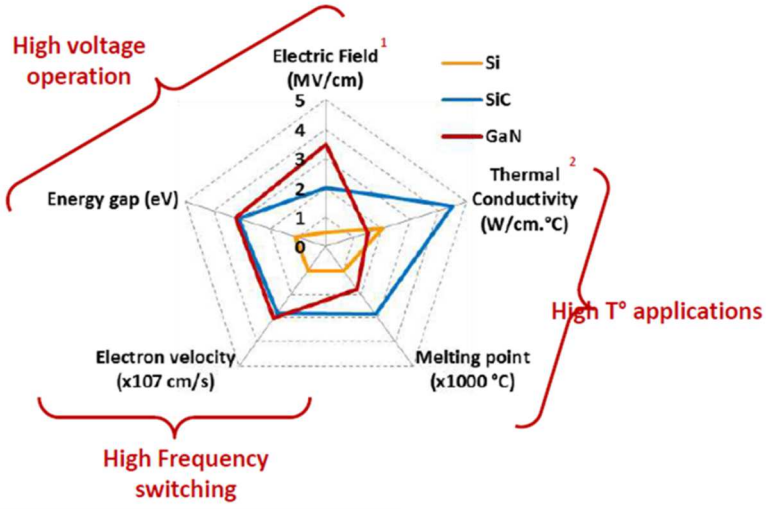


Figure 1.1: GaN material merit compared to Si and SiC.

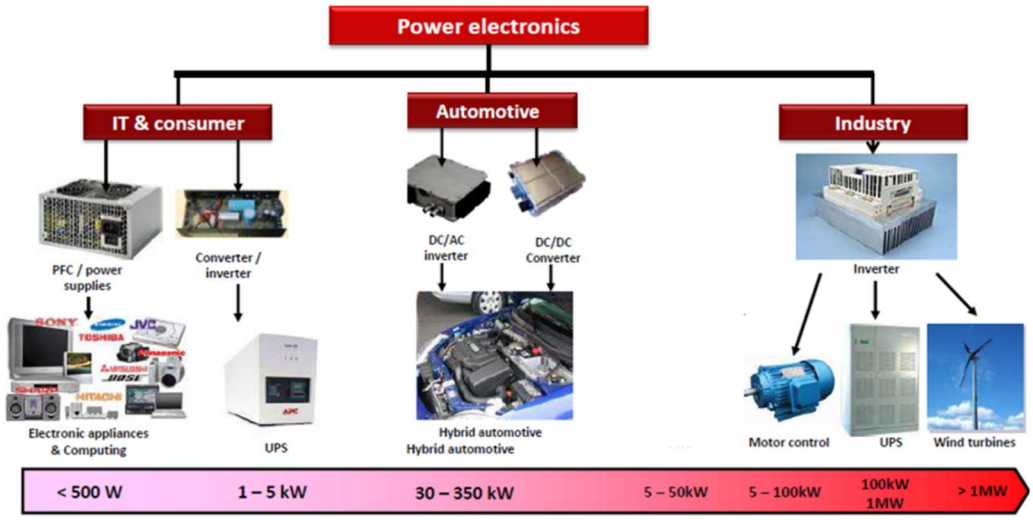


Figure 1.2: Applications of GaN-based power transistors.

Table 1.1: Semiconductor material properties at 300 K.

Properties	Si	SiC	GaN
Bandgap Eg (eV)	1.12	3.25	3.40
Breakdown field EB (MV/cm)	0.25	3.0	4.0
Electron mobility μ (cm2/V s)	1350	800	1300[a]
Maximum velocity υs (10^7 cm/s)	1.0	2.0	3.0
Thermal conductivity χ (W/cm K)	1.5	4.9	1.3
Dielectric constant ε	11.8	9.7	9.0
CFOM[b] $\chi\varepsilon\mu\upsilon sEB^2/ (\chi\varepsilon\mu\upsilon sEB^2)_{Si}$	1	458	489

[a]This is the bulk mobility. Heterostructural-2DEG mobility will be higher.

[b]CFOM: combined figure of merit for high temperature, high power and high frequency applications.

In addition, the higher thermal conductivities of GaN and SiC allow better thermal management for high power applications, where device self-heating is coupled with output power. Thus GaN, SiC seem to provide the best compromise for achieving high power/high frequency operation, power switching and high temperature applications.

In 1930, the gallium nitride material was synthesized first and then in 1969, it was grown epitaxially by means of hydrid phase vapour epitaxy (HVPE) by Maruska *et al.* [3]. Later an important breakthrough was achieved with the realization of the growth *via* metal organic chemical vapor phase epitaxy (MOVPE) [4] and the first optical studies on

high-quality GaN crystal [5]. Since then the scientific work done on this material system is exploding as depicted in Figure 1.3(a) according to *Web of Science* statistics [6]. The discovery of the *p*-type doping in 1980´s leading to the first high-brightness light emitting diode (LED) [7] and the development of the InGaN ternary alloy was pushed forward and consequently the blue laser diode [8]. In the next decade the AlGaN ternary alloy was perceived as a candidate for high power electronics. More recently, AlInN has come to the attention of the nitride community as the last of the ternary alloys owing to the difficulties in growth. Indeed, it is an attractive candidate for optical and electronic devices, with a bandgap covering an unprecedented spectral range from ultraviolett (UV) to infrared (IR). The interest for this peculiar alloy manifests in the steep increase in publication rate since 2000.

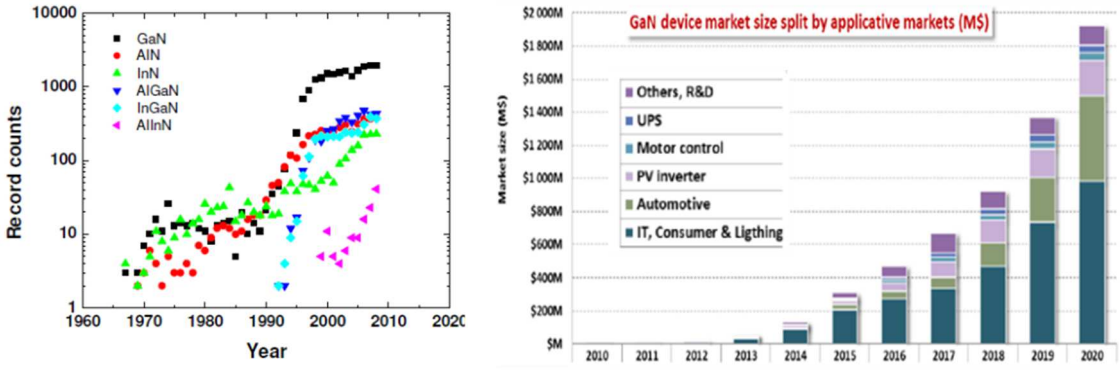


Figure 1.3 (a) Record counts containing the acronyms of the nitride compound in the tittle versus year of publication according to Ref [6]. (b) Nitride device market revenues and forecast, after [9]

Since its emergence in the early 1990s, GaN has attracted attention as highly promising material system for both optical and electronic applications due to their wide-bandgap, excellent transport properties, high critical field and high thermal stability. The III-nitride alloys of GaN, AlN, and InN are especially attractive for electronic

applications due to the unique property of obtaining large polarization fields, which promotes the ability to form heterostructures with large carrier densities at the interface as a two dimensional electron gas (2DEG) with high mobility. GaN based heterostructures, like the traditionally used AlGaN/GaN, having a high breakdown voltage and a large carrier density with high mobility, made it firstly ideal for high frequency/high power applications. The first report on the fabrication and operation of AlGaN/GaN HFETs (Heterostructure Field Effect Transistor), also called HEMTs (High Electron Mobility Transistor) was by Khan *et al* in 1993 [10]. Figure 1.4 shows the cross-sectional diagram of an AlGaN/GaN HEMT and the energy band diagram under the gate electrode, respectively. The AlGaN/GaN HEMTs is a three terminal device in which the current flowing between the ohmic source and the drain contacts is modulated by the Schottky metal gate contact. The majority carriers, electrons, are traveling through the highly conductive 2DEG channel and their number is modulated by the electric field resulting from the gate bias.

Many demonstrations of GaN based HEMTs have already shown the capability to exceed what is achieved by Si technology [11] in terms of output power and operation frequency, particularly beyond what is reached by Silicon LDMOS (Laterally Diffused Metal-Oxide-Semiconductor) power amplifiers and above 2 GHz. In addition, these heterostructures are expected to operate more reliably than Si in harsh environment like elevated temperatures above 200 °C, or in chemical sensing environments that are aggressive to Si.

One of the main drawbacks of III-nitrides is that the binary compounds namely GaN, AlN and InN exhibit large lattice-mismatch with each other preventing arbitrary

combinations of epitaxial layers and thicknesses for the growth of heterostructures. AlInN offers a new degree of freedom in designing nitride heterostructures for a wide range of applications by growing strain-free, lattice-matched (LM) heterostructures on GaN templates. In 2001, Kuzmik [12] pointed out that the combination of strain-free AlInN epi-layers together with a high polarization discontinuity over the heterointerface would lead to superior device performance with respect to AlGaN/GaN heterostructures. Therefore, AlInN/GaN HEMTs have emerged as an ideal candidate and a strong contender for the realization of high-power and high-frequency electronics for commercial and military applications. They are in fact widely expected to outperform their AlGaN/GaN HEMT counterparts due to the system unique electronic properties such as a high polarization charge and the possibility to grow the materials lattice-matched.

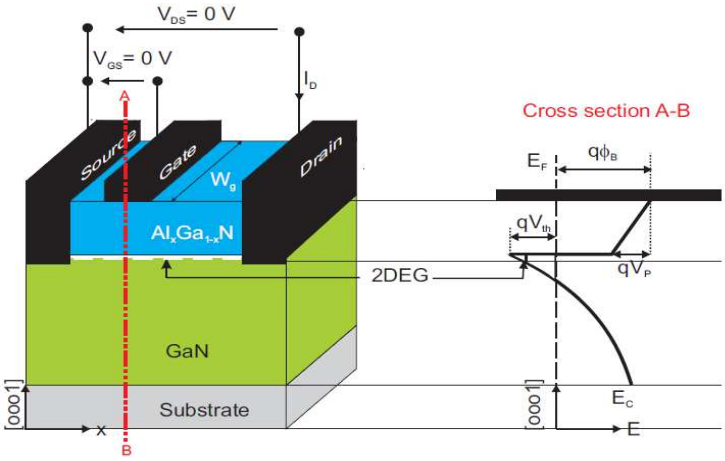


Figure 1.4: A planar gate AlGaN/GaN based HEMT structure and the energy band diagram under the gate electrode.

There was only scarce information on the AlInN alloy properties at the beginning of this thesis, in 2010 as can be seen from Figure 1.3(a). AlGaN/GaN was the well established material system for high power devices. These structures exhibit typical 2D electron gas (2DEG) density confined at the heterointerface in the order ~1.0×10^{13} cm^{-2}.

Especially, high electron mobility transistors (HEMTs) operating at GHz frequencies processed from these heterostructures already reached market maturity (see Figure 1.3(b)) and are successfully commercialized [13] with a special interest in communication technologies such as "Worldwide Interoperability for Microwave Access" (WiMAX) [14].

On the other hand, there is a serious interest on AlInN/GaN heterostructures for the next generation of high power electronics as it was found that AlInN/GaN heterostructures exhibit more than twice the amount of electrons confined at the heterointerface, *i.e.* in of the order of 2.6×10^{13} cm^{-2}. Unfortunately these electrons forming the so-called 2DEG suffer from poor inplane transport properties. Therefore, insertion of an AlN interlayer was used, an approach also explored already with the AlGaN system that helps to keep the electrons confined in the GaN and less scattered by alloy composition fluctuations. The variation of the interlayer thickness thereby results in a 'high mobility window' with a maximum of 1200 cm^2/Vs at an interlayer thickness of ~1 nm and a 2DEG density of $\sim 2.6 \times 10^{13}$ cm^{-2} at room temperature (RT) [15].

The absence of stress contributes greatly to the high mechanical/thermal stability of the heterostructure avoiding stress related degradation which is observed in AlGaN/GaN heterostructure [16, 17]. This is the most prominent advantage of this heterostructure which enabled very high temperature storage/operation of the HEMT above 500 °C and up to 1000 °C [18]. In fig 4(a), it is shown that the AlInN can be grown lattice matched on GaN with 83% Al. The high Al-content yielded high Ns values of above 2 x 10^{13} cm^{-2} (fig 4b) and high I_{DS} (above 0.5 A/mm) for barriers thinner than 15 nm in [12]. This has enabled high aspect ratio devices with high cut-off frequencies and

the ability to use gate dielectrics without compromising the aspect ratio [19], and high performance enhancement mode (E-mode) devices to be realized [14]. The high current densities allowed demonstration of high power densities at high frequencies and low drain voltages, promoting the lattice matched-AlInN as an alternative barrier material to the conventional AlGaN barrier [20, 21].

1.2 Thesis Outline

The scope of this thesis is manifold. On one hand, there is a general aspect, *i.e.* to investigate general properties of the AlInN alloy ranging from structural and electronic properties. On the other hand, physical phenomena are discussed, which are closely related to the device operation such as transport properties and thermal effects on device characteristics. One of the purposes of this thesis is to improve the device performance of this brand new heterostructures for next generation power devices thus at the end of the thesis, potential of the heterostucture has been explored and a new device fabrication and packaging designed has been proposed for future work.

This thesis is divided in 8 chapters.

In Chapter 1 an overview over the most important structural and electrical properties, which are (partially) unique to III-nitrides is given. After an historical introduction to GaN research, the main physical properties of the material are discussed and emphasizing the reason why GaN is a suitable material for high power and high frequency device. An brief mention to the substrates used for the growth (Al2O3, SiC and Si) is also given.

Chapter 2 is focused on the properties of the AlInN/GaN heterostructures starting with the crystal structure and the electronic properties of the material (like its band gap,

its spontaneous polarization, etc.) In the first part, after a brief introduction on the crystal structure, the formation of the 2DEG in semiconductor heterostructures is explained, with special attention to the case of an AlInN/GaN systems. In the second part, the working principle of the GaN-based High Electron Mobility Transistors (HEMTs) along with its performance limitations below the ideal expectations is briefly discussed.

In Chapter 3 advantages of using lattice matched AlInN/GaN HEMT is discussed in this chapter starting with summarizing the advantages of the lattice matched (LM) AlInN/GaN HEMT followed by the basic heterostructure growth and HEMT fabrication technology. Finally barriers scaling properties of AlInN/GaN HEMTs ranging from 3 nm to 33 nm were investigated and discussed. In this context, it has been pointed out that among the possible approaches for the fabrication of enhancement mode transistors using AlInN/GaN heterostructures, the recessed gate etching technique is seems to be the most interesting one. Hence, a detailed investigation on recessed gate etching is discussed in the next chapter.

Chapter 4 discussed the technological steps needed to achieve the first ever reported enhancement mode (E-mode) AlInN/GaN MISHEMTs with a threshold voltage of above 1.5V. The excellent performance of the E-mode device and the fabrication process applied to realize the normally off device is discussed along with other techniques and their advantages and challenges.

In Chapter 5, the transport properties of SiO_2/AlInN/AlN/GaN MOSHEMTs on SiC substrate is investigated. The 2DEG density was deduced from high-frequency capacitance–voltage (*C–V*) measurements. Analytical study in this chapter predicted the zero bias drain saturation current density to be increase by ~23% with the realization of

100 nm gate length MOSHEMTs, which would thus bring their dc characteristics in line with those of the best devices reported in the literature.

Chapter 6 discussed the preliminary comparative studies on dc performance of quaternary AlInGaN/GaN MOSHEMTs with (2% Ga incorporated in the barrier layer) with ternary LM-AlInN/GaN MOSHEMTs to fully explore the potential of the AlInN/GaN heterostructure. Incorporation of Ga composition from 0% to 2% increased the room temperature equivalent 2DEG density from 1.96×10^{13} cm^{-2} to 2.03×10^{13} cm^{-2} which is also confirmed by self-consistent Poisson Schrödinger simulation. The 2DEG mobility was enhanced by introducing Ga in the lattice matched AlInN barrier layer with good pinch-off characteristics. In conclusion, AlInGaN MOSHEMT devices exhibited a better performance in terms of maximum saturation drain current, threshold voltage shift as compared to that of standard AlInN MOSHEMT fabricated similarly.

In Chapter 7, at the first part, the first study of multi-gate AlInN/InN/GaN depletion mode (D-mode) and enhancement mode (E-mode)/normally off MOSHEMTs over sapphire substrate with gate widths varying from 0.15 mm to 0.9 mm is discussed. Both the D-mode and E-mode devices were fabricated using a 3-4 nm thick SiO_2 dielectric film and a novel Si_3N_4-based bridging approach for source contacts interconnections. The maximum saturation output current and the maximum extrinsic transconductance appear to scale nearly linearly with the gate width, which make the corresponding MOSHFETs very promising for high-voltage, high power operation and digital ICs can be constructed combining these devices. To fully explore the potential of this heterostructure as a large-periphery device, a detailed investigation on the study of multi-gate with gate widths varying from 0.25mm to 5mm is discussed next in the second

part. The maximum saturation output current and the maximum extrinsic transconductance appear to scale nearly linearly with the gate width up to 1mm beyond which joule heating dominates. In this context, it has been pointed out that at high output power densities, device self heating is the main limiting factor for stable operation of the device. Especially when the heat sources are located close to one another, the temperature rise due to thermal crosstalk between the sources may be much greater than the heat source alone. With high power and small chip size, the thermal effect will degrade the reliability and efficiency of GaN device. To maintain good switching characteristics in operation, the junction temperature should be limited within a permissible range. Thus efficient heat dissipation and management is a key to enable reliable and efficient GaN HEMT power operation which is discussed in the next chapter.

Finally, Chapter 8 discussed an evaluation of two approaches for heat dissipation (bottom and top heat dissipation) together with the challenges presented and the technological steps to realize it. Thermal simulation of the device showed that reduction in the maximum device temperature for different power dissipation can be achieved by adding a thermally conductive epoxy heat spreader and a heat sink on top instead of extracting the heat from the bottom of the device using a heat sink. Extracting heat from the top is similar to a flip-chip configuration but adding heat sink and the heat spreader on top of the device is however not straight forward. To be able to flip-chip the device and add the heat spreader requires additional device processing steps and the device design and packaging plays an important role in the thermal management of the device. Hence, a packaging technique has been proposed using the flip-chip technology to extract

the heat efficiently from the top of the device which enables an even higher HEMT thermal stability are presented followed by a summary and conclusion of the work.

The research activity presented in this work of thesis was carried out using the clean room and others characterization facilities of PML (Photonics and Microelectronics Lab) in University of South Carolina. The LM-InAlN/GaN with 83% Al-content is difficult to grow due to the high stress between the AlN barrier and the GaN buffer hence the work involved a high level of cooperation with the growth teams, and a constant feedback with the characterization teams in order to optimize the heterostructure growth. The thesis outline will thus follow the rout taken to optimize, apply and characterize these technologies.

CHAPTER 2

WORKING PRINCIPLE OF HEMTs

Fundamental background on GaN-based HEMTs material system, devices and technology are introduced in this chapter. First, the basic material properties and parameters of Gallium Nitride (GaN)-based semiconductors, the advantages and challenges of GaN based heterostructure will be discussed. Polarization effects in GaN-based semiconductor particularly for $Al_xIn_{1-x}N$/GaN heterostructures are introduced. Physical principal of operation of the GaN-based High Electron Mobility Transistors (HEMTs) along with its performance limitations below the ideal expectations will be briefly discussed.

2.1 Material Structure and Polarization in Wurtzite GaN-Based Semiconductors

The III-nitrides material group can crystallize in the Wurtzite crystal structure or zincblende crystal structure. At ambient condition Al/In/Ga-N retain the stable Wurtzite structure. Figure 2.1(a) shows a schematic of the hexagonal Wurtzite lattice of III-nitrides. The Wurtzite structure has a hexagonal unit cell and consists of two intercepting Hexagonal Closed Packed (HCP) sub-lattice. The lattice parameters are defines as a_0, c_0 and u_0, where a_0 denotes the length of the basal hexagon, c_0 is the height of the hexagonal prism and u_0 is the anion-cation bond length along the c-axis. The ideal Wurtzite crystal is composed of two hexagonal lattices shifted ideally by a ratio of $c_0/a_0 = \sqrt{(8/3)} = 1.633$ and $u_0 = 3/8$. This will result in symmetrical tetrahedrons (each atom is bonded with four

nearest neighbor's atoms) of equal side lengths and equal angles (Figure 2.1b). In this unit cell each plane is composed of the same atom type (cation or metal) while the next plane is composed of nitrogen atoms (anions) meaning that the unit cell lacks the inversion symmetry (non-centrosymmetric). Because of their Wurtzite structure, GaN-based and group III-N based semiconductors can have different polarities, resulting from uneven charge distribution between neighboring atoms in the lattice. The polarity of the crystal is related to the direction of the group III-N dipole along the <0001> direction. Figure 2.2 shows the two possible polarities, in cation-face, i.e. Ga-face (0001) (a), structures the polarization field points away from the surface to the substrate, while in anion-face, i.e. N-face $(000\bar{1})$ (b), structures the direction of the polarization field is inverted. In both cases of polarity the high electronegativity of nitrogen shifts the negative charge centroid towards it and away from the metal and creates a local polarization along the c-axis plane and the basal plane. Due to this electronic charge redistribution inherent to the crystal structure the group III-N semiconductors exhibit exceptionally strong polarization. This polarization refers to spontaneous polarization, *P*sp, [22]. If the crystal structure has inversion symmetry and an ideal c0/a0 ratio of 1.633 (ideality factor) the resultant polarization vectors will compensate each other but the III-nitrides with its non-centrosymmetry deviate from this ideality factor. Because of the different metal cations, the bond lengths and the resultant *c*0/*a*0 ratios of the common nitride compounds AlN, GaN, and InN and their alloys are different. As the lattice non-ideality increases, *c*0/*a*0 ratio moves away from 1.633 of the ideal lattice and the strength of the spontaneous polarization (P_{sp}) depends on the c0/a0 ratio. Bernardini et al. presented a calculation of the spontaneous polarization in relation with the lattice

parameter. All the III-nitride binary alloys (GaN, AlN, InN), ternary alloys (In_xGaN_{1-x}, In_xAlN_{1-x}) and ternary alloys (In_xGaN_{1-x}, In_xAlN_{1-x}) with different bandgaps has different spontaneous polarization values.

Ambacher et al [23] presented an extensive review of the III-nitrides properties and the formulas presented in this review will be adopted here. Figure 2.3a shows the relation between the composition of the alloy and its lattice parameters for a crystal with Ga face polarity. It is worth noting that an AlInN alloy with 83% Al content has the same lattice constant a0 as GaN meaning it is lattice matched to GaN in the plane of growth direction [0001]. The variation in the lattice parameters leads to a variation in the bandgap (Figure 2.3b) and the spontaneous polarization values (

Figure 2.5a). The negative sign of polarization indicates that the polarization vector points towards the substrate, from Ga atom to N atom, opposite to the [0001] direction. It is to be noted that all III-nitride alloys have a negative spontaneous polarization.

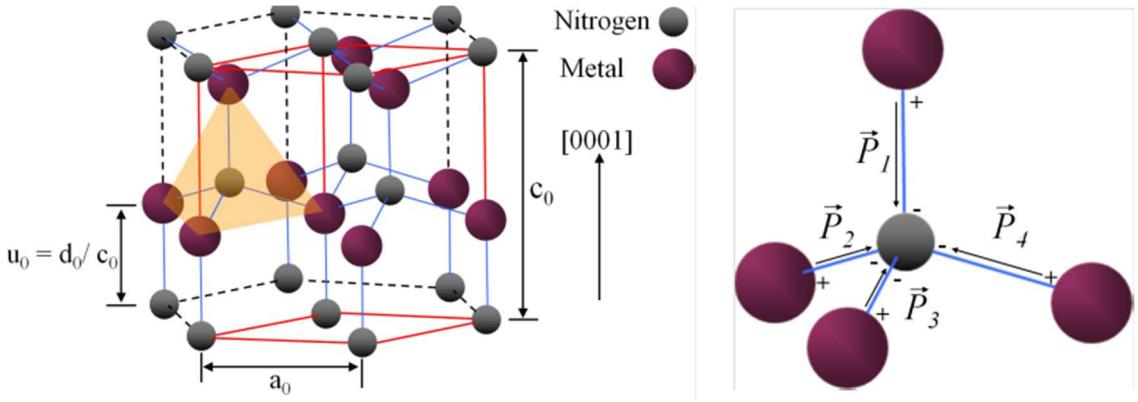


Figure 2.1 A schematic of (a) the ideal hexagonal lattice of III-nitride and (b) the tetrahedron shaded in (a) with the polarization vectors induced by the difference in electronegativity of the constituent nitrogen and metal atoms.

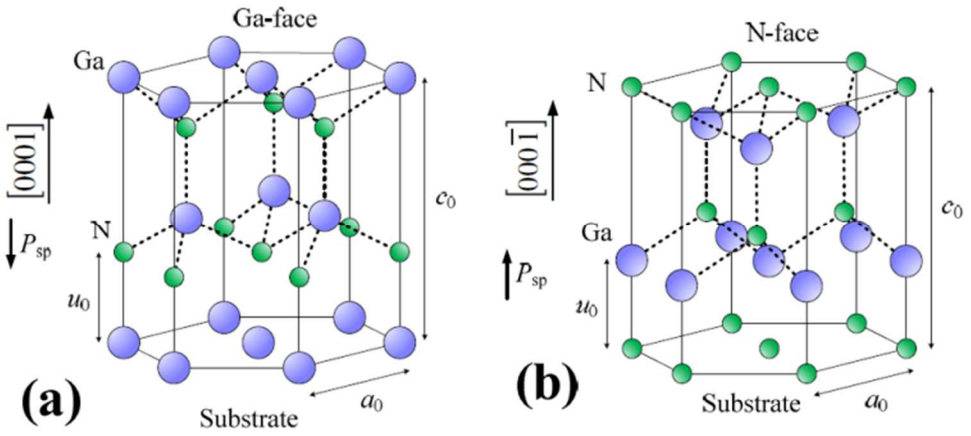


Figure 2.2 Illustration of (a) Gallium-face (b) Nitrogen-face ideal Wurtzite GaN lattice structure.

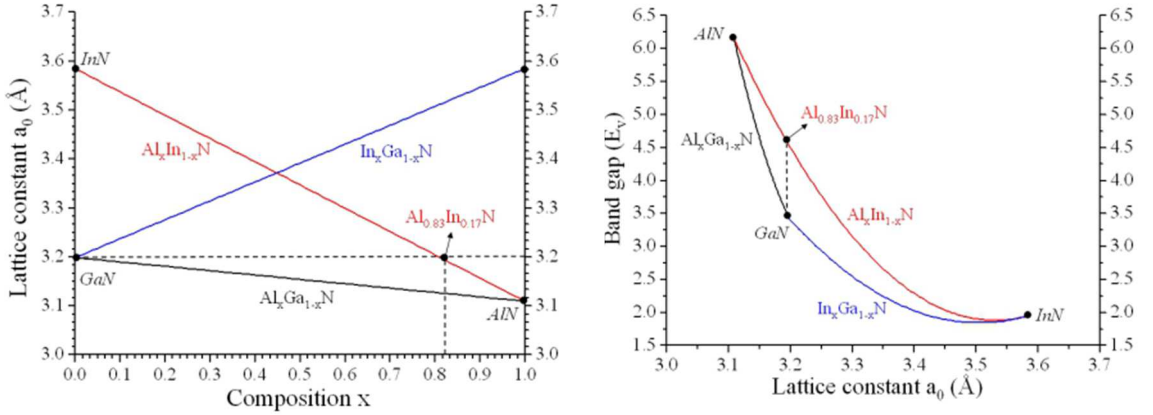


Figure 2.3 (a) Lattice constant a0 in dependence of alloy composition. A LM-InAlN alloy with 83% Al content has the same lattice constant a0 as GaN. (b) Alloy bandgap in dependence of the lattice constant a0 [23].

The lattice parameters can also be changed by applying external mechanical forces in form of strain. The ideal lattice parameters *c*0 and *a*0 of the III-N crystal structure will change to the applied stress along the <0001> direction to accommodate the stress. Therefore, the polarization strength will be changed. This additional polarization is called piezoelectric polarization, (P^{pz}) [22]. For example, the lattice constant *a*0 will decrease and the lattice constant *c*0 will increase if the nitride crystal is under

compressive stress. Hence, the *c*0/*a*0 ratio will increase towards 1.633 of the ideal lattice. The piezoelectric polarization P^{pz} is described by Hook's law as in equation (2.1):

$$P_i^{pz} = \sum_j e_{ij}\epsilon_{ij} \tag{2.1}$$

where e_{ij} are the piezoelectric coefficients and ϵ_j is the strain in direction j. Neglecting the shear strain and employing the non zero piezoelectric coefficients (e_{33}, $e_{31}$and e_{15}) the piezoelectric polarization along the c-axis is then described by equation 2.2:

$$P_3^{pz} = e_{33}\epsilon_{33} + e_{31}(\epsilon_1 + \epsilon_3) \tag{2.2}$$

where $e_{33} = (c - c_0)/c_0$ is the strain along the c-axis and $\epsilon_1 = \epsilon_2 = (a - a_0)/a_0$, with a_0 the lattice constant of the relaxed alloy and a the lattice constant of the strained heteroepitaxially grown alloy. The strain along the c-axis is connected to the strain along the basal plane by the elastic constants C_{13} and C_{33} through equation (2.3):

$$\epsilon_3 = -2\frac{C_{13}}{C_{33}}\epsilon_1 \tag{2.3}$$

Thus the piezoelectric polarization along the c-axis can be written in terms of the strain in the basal plane only as equation (2.4):

$$P_3^{pz} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{2.4}$$

Since e_{31} is always negative and e_{33}, C_{13} and C_{33} are always positive [22] then as a consequence, the value of piezoelectric polarization (P^{pz}) in group III-N is always negative for a tensile stress (a > a0) and for compressive stress (a < a0) P^{pz} is always positive. As spontaneous polarization in group III-nitrides is always negative, it can be concluded that for layers under tensile stress, spontaneous and piezoelectric polarizations are parallel to each other (as shown in Figure 2.4b) and for layers under compressive stress the two polarizations are anti-parallel (see Figure 2.4a)

The piezoelectric polarization of LM-InAlN on GaN is implicitly zero. The net polarization (Ptot) in an alloy is then the summation of the spontaneous polarization and the piezoelectric polarization as in equation (2.5):

$$P^{tot} = P^{sp} + P^{pz} \quad (2.5)$$

Polarization and the gradients in polarization at interfaces and surfaces of AlInN/GaN heterostructures induce fixed sheet charges, which in turn cause strong electric fields inside every heterostructure and therefore enhance electron or hole accumulation at the interfaces. This accumulation is known as the Two-Dimensional Electrons Gas (2DEG) that will be discussed in the following section.

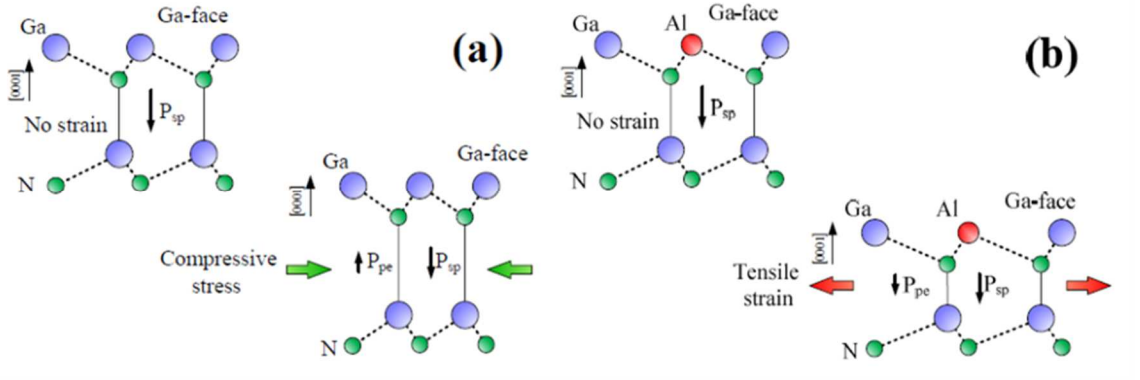


Figure 2.4:(a) Illustration of (a) GaN Wurtzite Ga-face compressive stress. (b) AlGaN Wurtzite Ga-face tensile strain.

2.2 AlInN/GaN Heterostructure and the formation of 2DEG

Two-Dimensional Electrons Gas (2DEG) is the most unique feature of the HEMT. The channel formed in a quantum well from carrier (electrons in this case) accumulation along a heterojunction is called 2DEG [24]. These electrons have high mobility because they are separated from the top donor layer and suffer less Coulomb

scattering. In addition, the quantum well is inside the unintentionally doped (UID) GaN layer which enhances the mobility further more because of the significantly reduced impurity scattering. The key difference between the HEMTs and the FETs is the enhanced electron mobility. To understand the formation of 2DEG in III-N HEMTs, the most commonly used GaN based heterostructures is shown in Figure 1.4 where a III-nitride alloy, AlGaN (usually called a barrier) is grown pseudomorphically on top of a relaxed GaN buffer. Both layers are assumed to be undoped and grown with Ga-face polarity. N-face polarity will follow the general rules presented here and details can be found in [23, 25]. The Fermi levels *E*F of the two semiconductors (barrier and the buffer layer) are at different level and they do not coincide in

Figure 2.5a. To have one common Fermi level, the energy band will bend and reach the thermodynamic equilibrium (see

Figure 2.5b). A discontinuity in the conductance (*E*C) and valence (*E*V) band at the heterojunction results in this process and a triangular quantum well emerges. Electrons from barrier layer diffuse into the quantum well and create strongly localized 2DEG. The term 2DEG refers to the condition in which electrons have quantized energy levels in one spatial direction but are free to move in the other two directions, parallel to the interface.

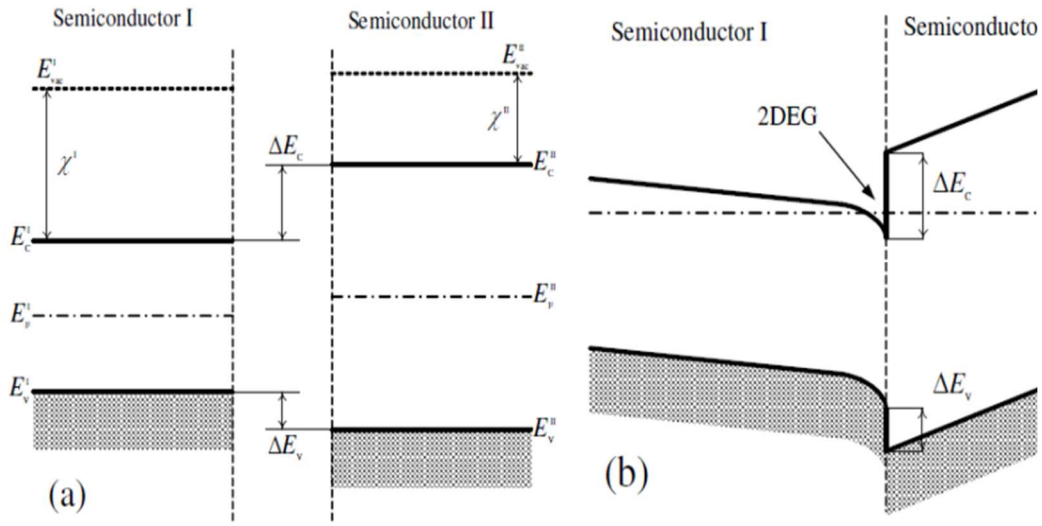


Figure 2.5: Band diagram of the heterostructure formed by polarized-piezoelectric narrow gap semiconductor I (GaN) and polarized-piezoelectric wide gap semiconductor II (AlGaN) (a) and together in thermo-dynamical equilibrium where semiconductor II is tensile strained (b).

The nitride epitaxial layers show both spontaneous and piezoelectric polarization fields under stress. In general, if the polarization field $\vec{P}$ changes in space, there will be a bound charge density (σ_P) associated with it to preserve charge neutrality. The polarization induced bound sheet charge density (σ_P) from the gradient of Ptot in GaN or its alloys is given by:

$$\sigma_P = -\nabla.\vec{P} \qquad (2.6)$$

Holes would then accumulate at the Ga-face and electrons at the N-face. This is illustrated in

Figure 2.6. Similarly an abrupt change in the polarization would occur at the interface if two III-nitride materials are grown pseudomorphically which will lead to an excess bound sheet charge density at the interface ($\sigma_{pol,interface}$) and given by equation (2.7):

$$\sigma_{pol,interface} = P_{GaN}^{tot} - P_{alloy}^{tot} \quad (2.7)$$

where P_{GaN}^{tot} is given by equation (2.5).

A counter charge of the same magnitude but with opposite sign should form at the interface as a 2DEG in the buffer to preserve charge neutrality. The difference in the total polarization of both materials would then be the generated sheet charge density (Ns). It is noted that the sheet charge density can be a 2DEG or 2DHG depending on the polarization discontinuity between the GaN buffer and the barrier.

Now the expected generated Ns for different barriers grown on GaN buffer depends on the barrier layers. Theoretically large Ns values are predicted for $(Al,In)_xGa_{1-x}N$ alloys with increasing the Al-content (see

Figure 2.7a), like in the case of LM-AlInN (~2.7×10^{13} cm^{-2}) and AlN (~6.8×10^{13} cm^{-2}).

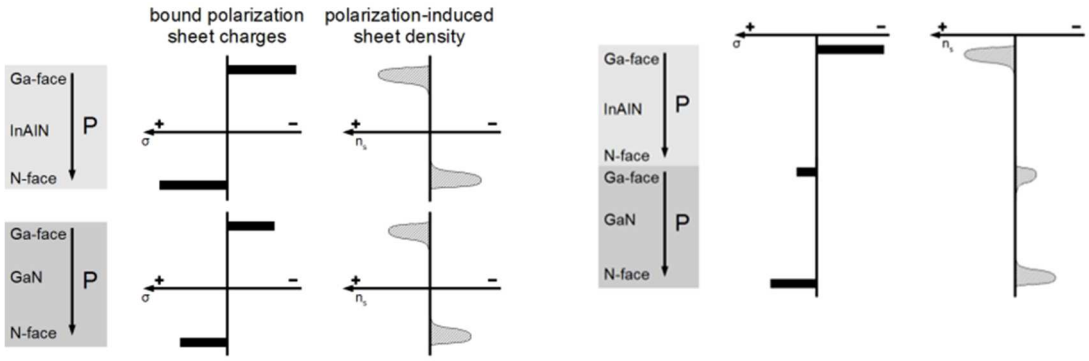


Figure 2.6: Schematic of polarization-induced interface charge in pseudomorphically grown heterostructure.

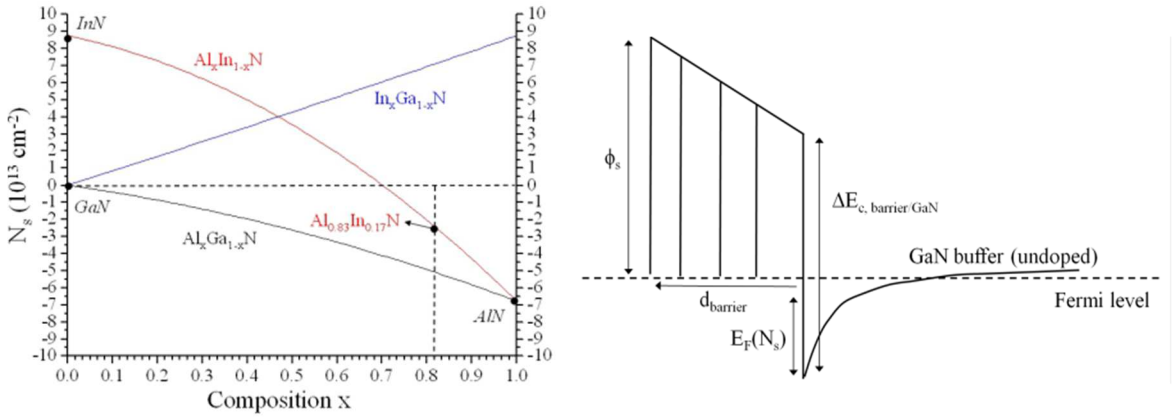


Figure 2.7: (a) Theoretical maximum 2DEG sheet charge density (Ns) for III-N alloys grown on relaxed GaN buffer with Ga-face polarity in dependence of alloy composition (left). (b) Band diagram of a GaN based HEMT with barrier of thickness dbarrier and an unpinned surface potential, Φ_s (right).

Considering the general case of a GaN HEMT band diagram as sketched in Figure 2.7b, the maximum sheet charge density Ns [47] can be written as:

$$N_s = \sigma_{pol,interface} - \left[\frac{\varepsilon_{barrier}}{d_{barrier} \cdot q}\left(\Phi_s + E_F\,(N_s) - \Delta E_{C_{barrier/GaN}}\right)\right] \qquad (2.8)$$

where $d_{barrier}$is the barrier thickness, q the elementary charge, Φ_s is the surface potential, $E_F\,(N_s)$ is the energy difference between the Fermi level and the conduction band at the bottom of the 2DEG and $\Delta E_{C_{barrier/GaN}}$ is the conduction band offset between the barrier and the GaN buffer. The energies are in Volts. The charge concentration and polarization discontinuity are in cm^{-2}.

2.3 Basic model of GaN HEMTs

The first report on the fabrication and operation of AlGaN/GaN heterojunction FETs, also called HEMTs, was by Khan *et al.* in 1993. Figure 2.8 shows the cross-sectional diagram of an AlGaN/GaN HEMT.

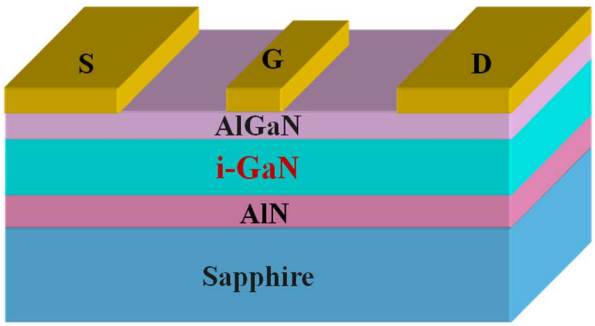


Figure 2.8: A planar gate AlGaN/GaN based HEMT structure.

The basic level analysis of the I-V characteristics of a HEMT is similar to a Metal-Oxide- Semiconductor FET (MOSFET) using a gradual channel approximation [26] taking into account two variations:

- According to equation 2.8, the charge carriers Ns can be modulated by altering the built-in field in the barrier. The surface potential Φ_S in equation (2.8) is written as:

$$\Phi_S = \Phi_{SB} + V_g \qquad (2.9)$$

- The pinch-off voltage (Vp) is defined for the case that Ns equals zero (see also Figure 2.9b). This can be derived by replacing equation (2.9) in equation (2.8) and setting it to zero noting that E_F (Ns) equals zero at pinch-off, yielding:

$$V_p = V_{Built-in} - \frac{q.d_{barrier}.\sigma_{pol,interface}}{\varepsilon_{barrier}} \qquad (2.10)$$

where $V_{Built-in}$ is the built-in voltage, and is equal to $\Phi_{SB} - \frac{\Delta E_{C_{barrier/GaN}}}{q}$, and is defined by the gate and heterostructure material parameters. Thus Vp for a given GaN HEMT can be changed by changing $d_{barrier}$ as will be shown later in chapter 3 for LM-AlInN/GaN HEMT.

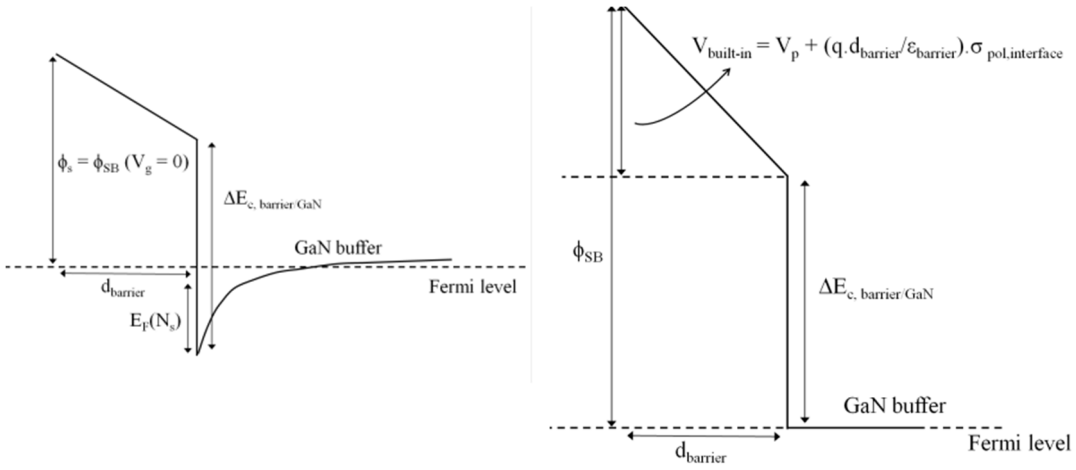


Figure 2.9: Schematic of HEMT band diagram under the gate (a) in case of no applied gate voltage Φ_S equals the contact potential Φ_{SB} (left), and (b) Φ_S is controlled by the gate voltage, as shown here for the case of a pinched-off channel (right).

Now following the gradual channel approximation as in a MOSFET, the drain-source current (I_{DS}) can be written as:

$$I_{DS} = \mu C_{GS} \frac{W_G}{L_G} \left[(V_{GS} - V_p).V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.11}$$

where C_{GS} is the gate-source capacitance and given by:

$$C_{GS} = \frac{\varepsilon_{barrier} W_G L_G}{d_{barrier}} \tag{2.12}$$

where W_G and L_G are the gate width and gate length respectively.

The saturation drain current (I_{DSS}) can be obtained by deriving equation (2.11) with respect to V_D and setting it to zero yielding:

$$I_{DSS} = \mu C_{GS} \frac{W_G}{L_G} (V_G - V_p)^2 \tag{2.13}$$

and thus the transconductance (g_m) in the saturation region is a function of $1/L_G$, expressed by:

$$g_m = \frac{dI_{DSS}}{dV_G} = \mu C_{GS} \frac{W_G}{L_G} (V_G - V_p) \tag{2.14}$$

However, these equations represent the long channel approximation and are valid only in the constant mobility regime where the electron velocity is below the saturation velocity. Due to the high mobility in GaN HEMTs, the saturation velocity can be reached even for small drain biases and hence the device will operate in the velocity saturation mode. I_{DSS} can be then written using a two-piece linear approximation [27] as:

$$I_{DSS} \approx W_G C_{GS}(V_G - V_p)\vartheta_{sat} \tag{2.15}$$

and the transconductance is expressed by:

$$g_m = W_G C_{GS}\vartheta_{sat} \tag{2.16}$$

thus the linear dependence of the transfer characteristics on V_G, in contrast to long channel devices. Moreover, the cut-off frequencies of the device, neglecting extrinsic parameters, can be approximated by [26]:

$$f_t \approx \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2.17}$$

and

$$f_{max} = \frac{g_m}{2\pi C_{GS}\sqrt{4(R_S + R_i + R_G)\left(g_d + g_m\left(\frac{C_{GD}}{C_{GS}}\right)\right)}} \tag{2.18}$$

which for the case of small resistances can be reduced to:

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi R_G C_{GD}}} \tag{2.19}$$

The natural way to increase the device cut-off frequencies in GaAs HEMTs is to aggressively scale down the device dimensions [28] in addition to better channel confinement [29]. From equation (2.17) and (2.14), it can be seen that f_t is inversely proportional to L_G (neglecting the parasitic capacitances), thus reducing L_G would yield higher f_t. However, this approach is limited by the short channel effects known for

MOSHEMTs [26]. In the case of GaN HEMTs, the lateral field at the drain side makes the effective gate length asymmetric, and in total larger than the metallurgical gate length [30]. Thus to maintaining a certain aspect ratio L_G / $d_{barrier}$ to keep the internal field distribution the same, down scaling of the barrier is also required. A universal minimum aspect ratio of 15 was found to be a limit to avoid short channel effects by simulation of AlGaN/GaN HEMTs and observed experimentally in [31]. For power amplifiers, increased operation frequency has another limitation on the output power due to current collapse effect that will be discussed separately.

For linear operation of a class-A amplifier the output power (Pout) can be estimated as [32]:

$$P_{out} = \frac{1}{8} I_{DS_{max}} \left(V_{DS|_{V_{BR}}} - V_{knee} \right) \tag{2.20}$$

where V_{knee} is the knee voltage defined at the onset of current saturation.

Before discussing the power performance of GaN HEMTs, it is necessary to describe the breakdown mechanisms, in on-state and in off-state. The breakdown occurs through an increased gate leakage current in on-state. The gate leakage mechanisms in GaN HEMTs are dominated by trap-assisted tunneling and these traps can be located at the barrier/GaN interface or in the barrier due to un-intentional barrier doping or can be due to defects. A general expression of the tunneling current between the gate contact and the source contact across the barrier, conducted by the 2DEG is given by:

$$J_T = qnv_eT(E) \tag{2.21}$$

where J_T is the tunneling current density, n is the electron concentration, v_e is the electron velocity and T(E) is the transmission probability. Equation (2.21) is sufficient to describe the main features of the gate diode characteristics shown in Figure 2.10.

In forward bias direction, increasing the gate voltage modulates the barrier height making a flat band condition in the barrier. T(E) in eqn. (2.21) will then decrease but is counter balanced by an increase in the electron concentration in the channel. However, since v_e increases with voltage, J_T will eventually increase, until sufficiently high enough leakage current destroys the gate contact.

The same behavior is expected but here when reverse biasing the gate, T(E) will be increasing, counter balanced by a decreasing electron concentration and the reverse leakage current will increase up to the point where the channel is pinched-off.

The on-state breakdown and reverse bias leakage current are vertical field phenomena up to pinch-off and the surface properties will dominate the HEMT behavior once the channel is pinched-off. The diode characteristics exhibit a current limiter behavior and the leakage current is conducted laterally at the surface of the barrier, through hopping mechanism after pinch-off. At this stage, off-state breakdown will occur through an avalanche mechanism, occurring at the high field region at the gate edge toward the drain. A maximum of $I_{DSmax}.V_{BR}$ should be targeted to maximize the power.

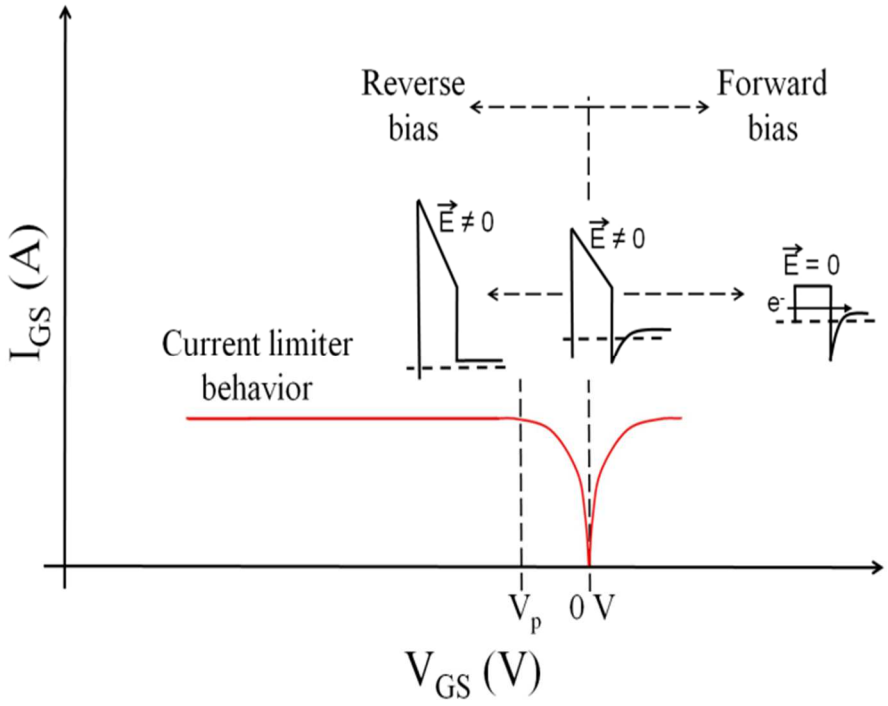


Figure 2.10: Schematic of gate diode characteristics for a single barrier HEMT. The leakage current in the forward direction follows a tunneling mechanism, and similarly in the reverse bias direction up to channel pinch-off, where the characteristics resemble a current limiter.

GaN HEMTs faces two types of limitations, technological limitations and intrinsic limitations. There are several solutions that can be addressed to overcome the technological limitations such as, design modifications, recesses, barrier or buffer doping, cap layers, field plates, gate dielectrics, which can be applied to all polar heterostructures regardless of the composition. On the other hand, the intrinsic limitations, namely the current collapse and self heating, apply to all heterostructures (regardless of composition) and cannot be eliminated but rather compromised by controlling the high field region near the gate, by optimizing the surface electronic conditions, and designing an efficient heat management solution.

2.4 Technological limitations: Barrier scaling, thermal and chemical limitations

According to the previous sections, most of the technological limitations and can be summarized as the following:

- $I_{DS_{max}} \propto N_s \propto d_{barrier}$ and $V_p \propto \frac{1}{d_{barrier}}$
- $f_t \propto \frac{1}{d_{barrier}}$
- $P_{out} \propto I_{DS_{max}}.V_{BR}$

This is a conflict in design rules to aim at maximizing P_{out} and f_t using the same barrier thickness and planar HEMTs design. To achieve maximum P_{out} and f_t product, using a thin barrier of an alloy with a high polarization discontinuity is the solution; in this case the LM-AlInN provides such an advantage. Other solutions have been applied to many GaN HEMT designs, like using AlN as a barrier material [33], maximizing V_{BR} by spreading the high field near the gate region using a T-gate or a slanted gate [34] and by reducing parasitic leakage currents in the buffer [35]. Yielding highly insulating buffers [36] through the optimization of buffer growth conditions will suppress the buffer leakage. To suppresse the gate-source leakage currents, increasing the Schottky barrier height either by using a metal with a higher barrier height [37] or by increasing the barrier height through changing the surface potential using plasma or wet chemical treatment [38] is used. The most popular approach is to use a gate dielectric [39] to form a MOSHEMT [40] but this would increase the total barrier height again, contrary to the aim. In addition, reducing V_{knee} is also essential in terms of power. This can be done by reducing the contact resistance (Rc) and by reducing the gate-source resistance (R_{GS}) by reducing the gate-source distance. A contact recess could be employed to reduce the contact resistance due to the tunneling nature of the ohmic contacts. Another approach

used was the selective doping of the access regions, or using an n+-GaN cap or ohmic contact region regrowth.

To increase the frequency performance of the device in planar technology with high current densities above 1A/mm, a thinner barrier (like LM-AlInN) or a higher polarization discontinuity (like AlN) could be used. These approaches however have their own limitations. Increasing the Al-content increases the piezoelectric polarization (see

Figure 2.7), which leads to an increase in barrier strain and strain relaxation and a drop in the electron mobility. For example, in AlGaN/GaN this occurs when the Al content exceeds s 30%. Lattice matched AlInN/GaN heterostructure is an exception in this case.

The thermal and chemical limitations are also considered technological. These limitations can be avoided by choosing a proper heterostructure design, and depend largely on the device operation environment. The thermal limitations appear during high power operation at room temperature (self-heating effects as will be discussed later), or if the device is operated at high temperature. The chemical stability limitations will present itself, if the HEMT devices will be used as sensors for chemical signals or if the HEMT is subjected to chemically and thermally harsh environment during processing. In the case of self heating thermal management is the key solution, but in the case of high temperature operation the heterostructure used has to be a priory thermally stable at the operation temperature.

2.5 Intrinsic limitations: Current collapse and device self heating

All of the above mentioned limitations can be addressed by choosing a proper heterostructure and device design. What cannot be avoided however, are the intrinsic limitations presented next, which are the main concern for device reliability.

2.5.1 Main power limitation: Current collapse

Current collapse (called also dispersion effects or lag effects) describes the fact that the power performance of the devices falls short of the predicted values of the equation 2.20 when measured at microwave frequencies or under pulsed conditions [41-46]. Figure 2.11 schematically shows this behavior by comparing the DC and pulsed I-V characteristics of a transistor. The pulsed characteristics are measured at a special bias point which is indicated by the blue circle. It is a inherit phenomena in GaN devices since all will have a polarization counter charge residing on the surface, responsible for the channel sheet charge density. This phenomenon is not observed for the small signal case, and not reflected on f_t or f_{max}, but appear only during power operation mode.

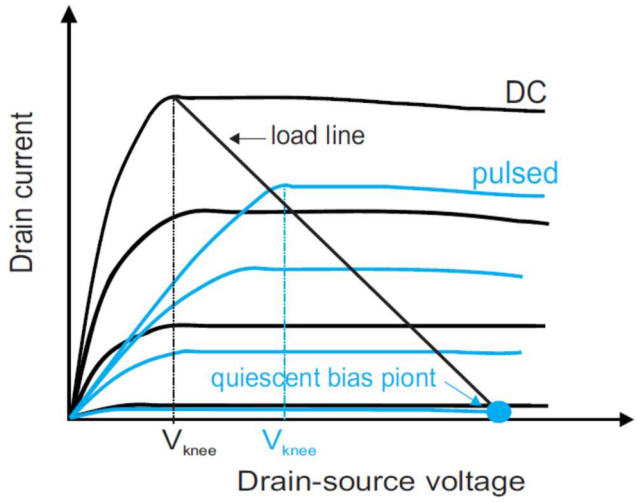


Figure 2.11: Typical DC and pulsed I-V characteristics of an AlGaN/GaN HFET. The pulsed I-V curves are measured at a special quiescent bias point marked by the blue circle.

The principal of current collapse is explained in Figure 2.12 that shows a schematic of IV-characteristics of a HEMT in on-state and off-state when the device is operated in DC or RF along a load line between V_{knee} at on-state and V_{BR} at off-state. During the device off-state with a high lateral field near the gate edge [47, 48], charge

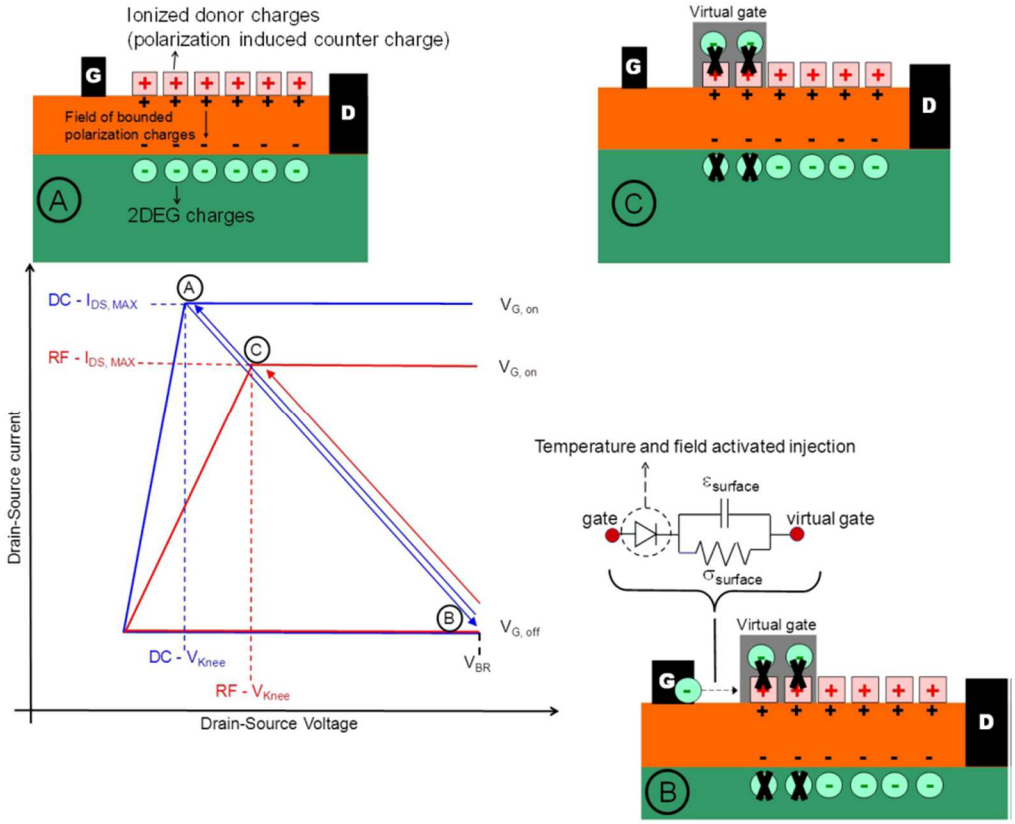


Figure 2.12: Schematic of I-V characteristics of GaN based HEMT under DC operation and under current collapse conditions. The surface configuration that leads to the current collapse, due to lateral charge injection in the surface donor traps is also shown (marked a,b,c), image taken from [49].

injection into surface states occurs. Electrons get trapped in the donor-like surface traps in the free region next to the gate and disturb the charge neutrality balance. This creates a virtual gate and reduces the sheet channel charge density in that region (see inset at point B in figure). The amount of injected charge depends on the mobility of the electrons on

the surface and on the applied voltages (mainly the gate-drain voltage), which follows a hopping mechanism [41, 42].

Now, during on-state, the biases and fields are reversed and the surface donor traps have to be discharged for the virtual gate to follow. The detraping of electrons is controlled by the RC time constant of the charging path. In DC operation time periods are large enough to allow the full trapping and detrapping to occur and the device will go back to the state depicted at point A. But the modulation of the virtual gate lags behind that of the actual gate if the RC time constant of the charging/discharging element is larger than the applied frequency. Then, the virtual gate will not be removed and the device will suffer from current collapse, as depicted at point C in the

Figure 2.12, with lower maximum current and an increased Vknee thus providing output powers below expected values. Surface passivation is used to reduce the current collapse by making the injected charges inaccessible to the surface [47, 50]. Typically used passivation schemes for GaN HEMTs are PCVD Si3N4 [24], in-situ or exsitu MOCVD Si3N4 [51, 52, 53]. In addition, used as both passivation and gate dielectric ALD-Al2O3 [54] and other high dielectric constant oxides (high-k oxides) [55] like ZrO2, HfO2 and MgO [56, 57, 58, 59] have been tested with varying degrees of current collapse reduction.

2.5.2 Device self-heating

Device self-heating is a major concern for GaN HEMTs due to its impact on the device performance and reliability. The dissipated power increase with increasing device output power that leads to an increase in the device temperature. Measurements and simulations have shown that self-heating causes a reduction in mobility and drift

velocities affecting both the output current and the operation frequency [60, 61]. Moreover, the increased device temperature affects the reliability of the device [62]. Thus efficient heat dissipation and management is a key to enable reliable and efficient GaN HEMT power operation.

The device design and packaging plays an important role in the thermal management of the device. But all sources agree a substrate with a higher thermal conductivity is more efficient in managing the heat for example SiC is the most efficient in terms of thermal management due to its superior thermal conductivity. The heat can also be extracted from the top of the device if the device is coated with a highly thermally conductive material. An evaluation of those two approaches for heat dissipation (bottom and top heat dissipation) will be presented in chapter 7 together with the challenges presented in each case and the technological steps to realize it. But first an overview of the HEMTs used in this work, their fabrication technology and temperature stability tests are given in the next chapter.

CHAPTER 3

BARRIER SCALING AND BREAKDOWN VOLTAGE ENHANCEMENT

Material properties of GaN HEMT, its design, performance and limitations were discussed in previous chapter. Advantages of using lattice matched AlInN/GaN HEMT will be discussed in this chapter. We will start with summarizing the advantages of the LM-AlInN/GaN HEMT followed by the basic heterostructure growth and HEMT fabrication technology. Finally scaling properties of AlInN/GaN HEMTs will be discussed.

3.1 State-of-the-Art of LM-AlInN/GaN HEMTs

The LM-AlInN/GaN heterostructure has the following advantages:

• Lattice matched relaxed barrier suffers no stress, thus avoids stress related degradation like what was presented by Joh et. al in [63] (see section 3.4). It was shown that such stress related degradation mechanism is not seen for the case of LM-AlInN [64]. The absence of stress contributes greatly to the high mechanical/thermal stability of the heterostructure.

• High temperature operation (above 500 °C and up to 1000 °6 [65, 66]) of the LM-AlInN/GaN HEMT is the most prominent advantages and it comes from the high thermal and mechanical stability.

• High Ns values (above 2 x 10^{13} cm^{-2}) [67] and high I_{DS} (above 0.5 A/mm) with thin barrier (less than 10 nm) is achieved because of high Al-content (83%) (discussed in

sections 2.3.1 and 3.3.1 and appears in [68]). This has enabled to use gate dielectrics without compromising the aspect ratio [69] and the ability to realize devices with high cut-off frequencies (summarized below), and high performance enhancement mode (E-mode) devices [70].

• The high current densities allowed demonstration of high power densities at high frequencies (summarized below) and low drain voltages, promoting the LM-InAlN as a an alternative barrier material to the conventional AlGaN barrier.

3.2 Heterostructure Growth

Metal Organic Chemical Vapor Deposition (MOCVD) or Molecular Beam Epitaxy (MBE) can be used to grow the heterostructure. The main difference between the two techniques is that MOCVD has a faster growth rate at a higher temperature (typically 1050 °C) than MBE (max. 800 °C at a much slower growth rate) [71]. Details of these techniques can be found in [72]. The difference in the growth temperature might prefer some substrates to others due to the lattice and thermal mismatch between GaN buffers and the typically used. Table 3 summarizes these parameters.

Table 3.1: Lattice and thermal mismatch to substrates used for GaN growth. After [9,14]

Material	GaN	SiC	Sapphire	Si
Themal Expansion Coefficient (10^{-6} K^{-1})	5.59	4.2	7.5	2.59
Lattice Mismatch (GaN/Substrate in %)	-	+3.5	-16	-17
Thermal Mismatch (GaN/Substrate in %)	-	+25	-24	+54

The thermal mismatch to the substrate and the difference in thermal expansion coefficient causes defects and cracking of the grown GaN. The lattice mismatch causes rotated GaN domains. The dislocations affect the thermal conductivity of the buffer. The growth on non-polar substrates (Si, Sapphire or Diamond) can cause mixed polarity and inversion domains. The mixed polarity affects the polarization and in turns the sheet charge density. AlN would be the best choice as a substrate because of the material properties mention above (see Table 3.1) but it is limited by the availability. High temperature grown AlN buffer is used between the substrate and the GaN buffer as a nucleation layer to reduce the mismatch effects that can be found in [73] with other growth technique. Because of the high cost of the SiC substrate, growth techniques were optimized for GaN on Sapphire but the state of the art data showed that the performance of GaN on SiC is superior to Sapphire and Si. The performance of the case of GaN on SiC is discussed in chapter 5.

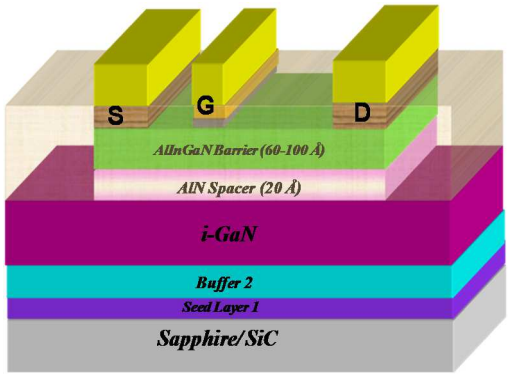


Figure 3.1: Cross section of the typically used heterostructure.

The AlInN/GaN heterostructures used here were grown by MOCVD on Sapphire and SiC. The GaN buffer thickness used is 2-3 µm grown on an AlN nucleation layer. A thin 1 nm AlN spacer is introduced before the AlInN barrier layer. This spacer reduces

the alloy interface scattering thus increasing the mobility up to 2 fold. Mobility up to 1500 cm^2/Vs are reached in the used heterostructures.

Figure 3.1 shows a cross section of the typically used heterostructure in this work along with the device dimensions routinely fabricated. Barriers ranging from 3 nm to 20 nm were investigated but most of the work was performed using a 6 nm barrier on Sapphire substrate. To achieve the lattice match configuration, the Al content varied slightly between 81% and 84% depending on the AlN buffer template, confirmed by the growers using High Resolution X-Ray Diffraction (HRXRD). The defining features of the heterostructure and the device dimensions will be pointed out later.

The material characterization before the device fabrication includes: sheet resistance of AlInN/GaN layer will be obtained by Lehighton contactless sheet resistance measurement system. The surface morphology of AlInN layer will be evaluated by atomic force microscopy (AFM). The non destructive mercury probe CV measurements will be performed to check the quality of the epilayer and determine whether the the epilayer has a leaky path or not. Backscattered Scanning electron microscopy (SEM) will be used to study the defects in the epilayer layer. The structural properties, such as strains in the epilayers will be characterized by x-ray diffraction (XRD) measurements using a high resolution Philips Materials Research Diffractometer. The Hall measurement will also be performed to find out the mobility and 2DEG carrier concentration.

3.3 HEMT Basic Fabrication Technology and Characterization

To define the potential and the limit of AlInN/GaN heterostructure, a simple planar fabrication technology with variable barrier thickness was used at the early stages of the work using. This was used for comparison and qualification between the different

heterostructures. Later on, a decision to concentrate on using the 6nm barrier AlInN/GaN grown on Sapphire substrates was made. This choice was based on the heterostructure properties, which will be discussed in this chapter.

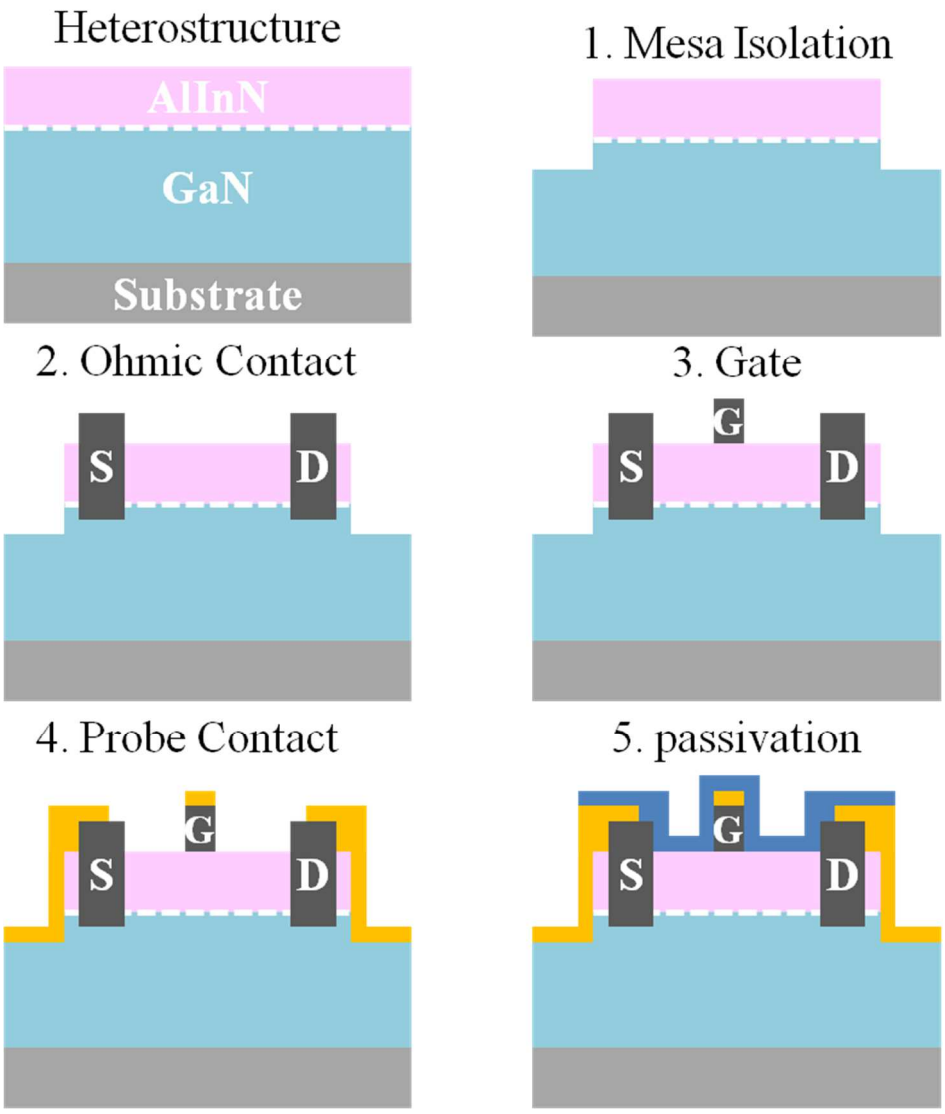


Figure 3.2: Cross section of the steps of fabrication process of a AlInN/GaN device.

The following is a summary of the standard HEMT fabrication steps used routinely. All fabrication steps are performed in a continuous routine and thus the choice of the technology is limited by the available technological facilities. Modifications of this process according to the technological needs will be mentioned in place. Except for the

optical lithography resist developer, the use of acidic or basic solutions was avoided (unless intentionally applied as will seen shortly) to avoid changing the heterostructure properties through uncontrolled modification of the surface potential.

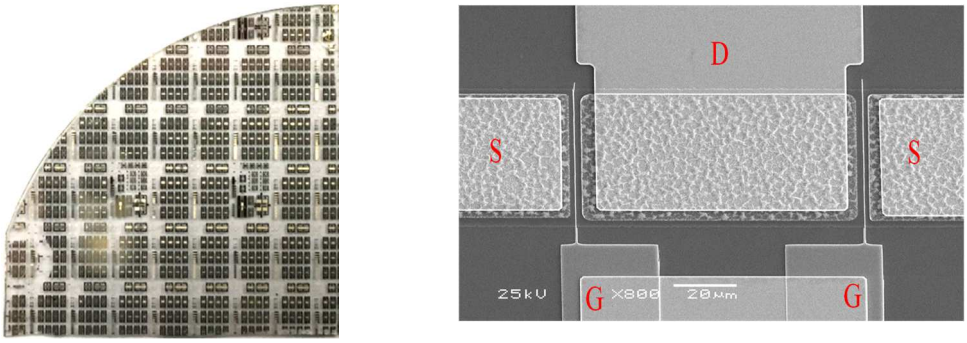


Figure 3.3: SEM image of a fabricated AlInN/GaN device.

The mask set used enabled the fabrication of a matrix of devices with variable width (2 x 50 μm, 2 x 100 μm and 2 x 150 μm), variable source-drain distance (6 μm, 8 μm and 12 μm) and variable gate lengths (1 μm, 1.2 μm, and 1.8 μm). Dedicated measurements structures (TLM structure, Gated-TLM structure, vertical and circular diodes and open and short calibration pads for RF measurements) are also on the same mask set. Mostly used was the device dimensions shown in Figure 3.1.

Step by step device fabrication process has been shown in the Figure 3.2. First step of the fabrication is the mesa isolation which was achieved by Chlorine based Ar-dry etching in an Inductively Coupled Plasma (ICP) etch chamber. An etch depth of 200 nm to 250 nm was used to enable proper mask alignment in the next optical lithographic step. Ohmic contacts were patterned by lift-off optical lithography. The samples were then dipped for 15 minutes in HCl:H_2O solution (1:1 ratio) for native surface oxide removal to ohmic metallization deposition. Ti/Al/Ti/Au (15 nm/70 nm/30 nm/50 nm) metallization was deposited in an electron beam (E-beam) evaporator. After lift-off the

ohmics were annealed in a Rapid Thermal Annealing (RTA) chamber in nitrogen atmosphere at 850 °C for 30 seconds. Due to the tunneling nature of the ohmic contact, provided by TiN surface defects generated at the annealing step, the contact resistance depends largely on the barrier thickness. E-beam evaporated 70 nm Ni / 50 nm Au gates were defined by photo lithography. Our DoD technique [75, 76] was used to deposit low temperature SiO_2 as the gate oxide in the Plasma Enhanced Chemical Vapor Deposition (PECVD) chamber using SiH_4 and N_2O as the gas precursors before the gate metal deposition. The oxide layer exists only under the gate. Ti/Ni/Au (70 nm/70 nm/50 nm) metallization was deposited in an E-beam evaporator to realize the probe contact. Devices were passivated with PCVD Si3N4 films deposited at 300 °C with varying thicknesses between 30 nm and 100 nm using Silane and Ammonia precursors. Contacts pads were opened in a Reactive Ion Etching (RIE) chamber using CF4 plasma. Scanning Electron Microscopic (SEM) image of a fabricated device has been shown in the Figure 3.3.

DC measurements and pulsed measurements were monitored to characterize the fabricated HEMTs. After technology optimization, selected devices were characterized by small signal s-parameter.

3.4 Barrier Scaling Properties

The HEMT properties due to barrier scaling effects are presented experimentally and will be discussed here. The scaling properties with barrier thickness of the AlInN/GaN HEMT used in this work are discussed in [74] but the main features of the barrier down-scaling will be presented here. Figure 3.4 and Figure 3.5 summarize the barrier down-scaling effect on HEMTs grown on Sapphire substrates with 2 μm GaN

buffer and 1 nm AlN spacer with variable AlInN barrier thicknesses down to 3 nm. The material properties of the AlInN/GaN heterostructure with different barrier thickness have been shown in Table 3.2. The planar device fabrication followed the steps described previously.

Table 3.2: Material properties with different barrier thickness for AlInN/GaN heterostucture grown on Sapphire substrate.

AlInN Barrier thickness (nm)	Sheet resistance (ohm/sq.)	Mobility (cm^2/v.s.)	Carrier density (cm-2)
3	308	999	1.37×10^{13}
6	204	1388	2.35×10^{13}
9	210	1219	2.73×10^{13}
14	213	1113	2.65×10^{13}
20	211	1107	2.76×10^{13}

The dependence of I_{DSmax} (gate bias, Vg = +2 V) on barrier thickness is shown in Figure 3.5(a) follows the trend of Ns dependence on $d_{barrier}$ shown in Figure 3.4(a). For thick barriers of 9 nm I_{DSmax} is approx. 1.1 A/mm and decreases to 0.3 A/mm for the 3.0 nm barrier which is still significantly high. Thin barriers can provide a reduction in the sheet resistance (see Figure 3.4 c), but barrier thickness lower than 6 nm shows increased sheet resistance and the 2DEG carrier concentration decreases. Moreover, the 2DEG carrier mobility drops to a low value as the barrier gets thinner than 6 nm (see Figure 3.4 b) resulting lower current density with very thin barrier. Usually the trend for mobility is

that it decreases with increasing carrier concentration as the thickness of the barrier increases due to increased carriers scattering.

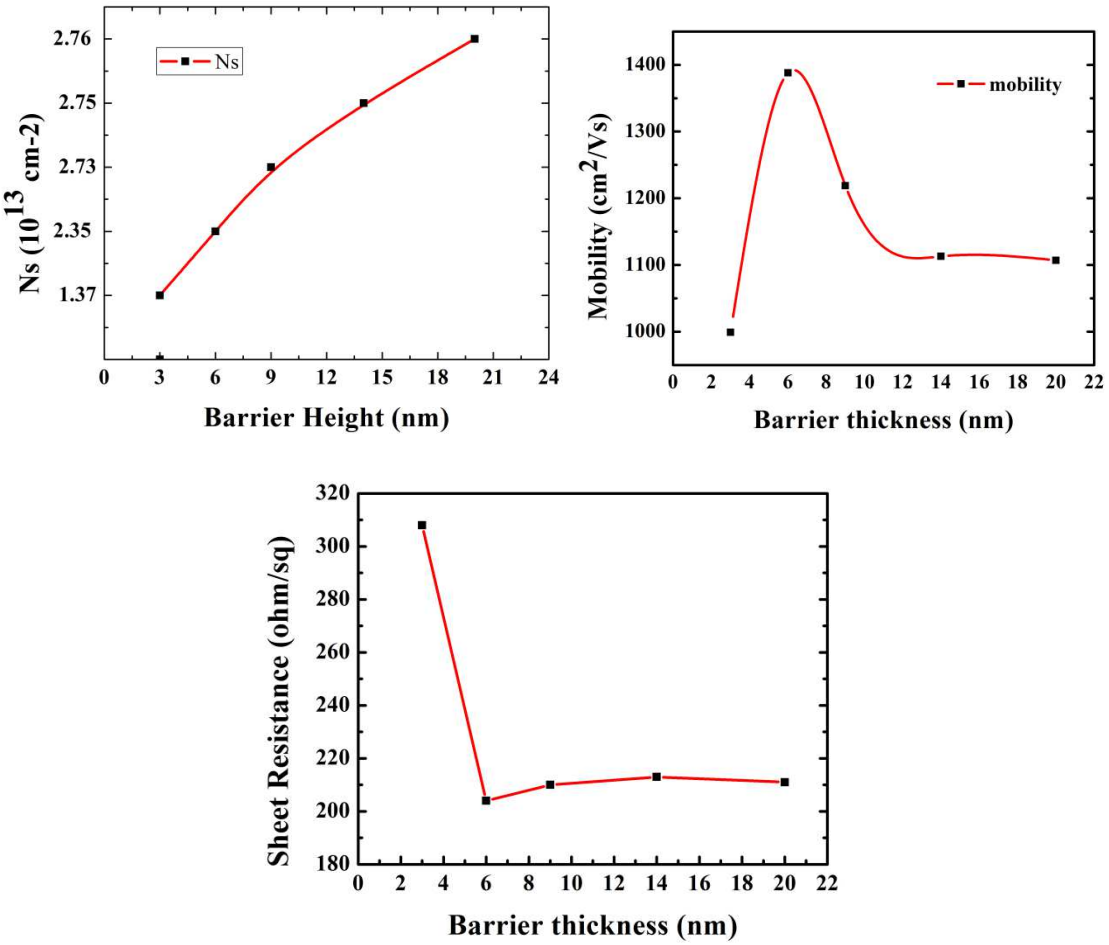


Figure 3.4: The barrier down-scaling also causes a (a) decrease in the 2DEG carrier density (top left) (b) increase in the 2DEG carrier mobility (top right) and (c) decrease in the sheet resistance (bottom).

V_P scales linearly with the barrier thickness (see Fig. 15b) and an enhancement mode of operation would be reached for a total barrier thickness of less than 3 nm. Indeed, we were able to show that this is the case by demonstrating an E-mode MOSHEMT with a barrier thickness of 2 nm which will be discussed in the next chapter.

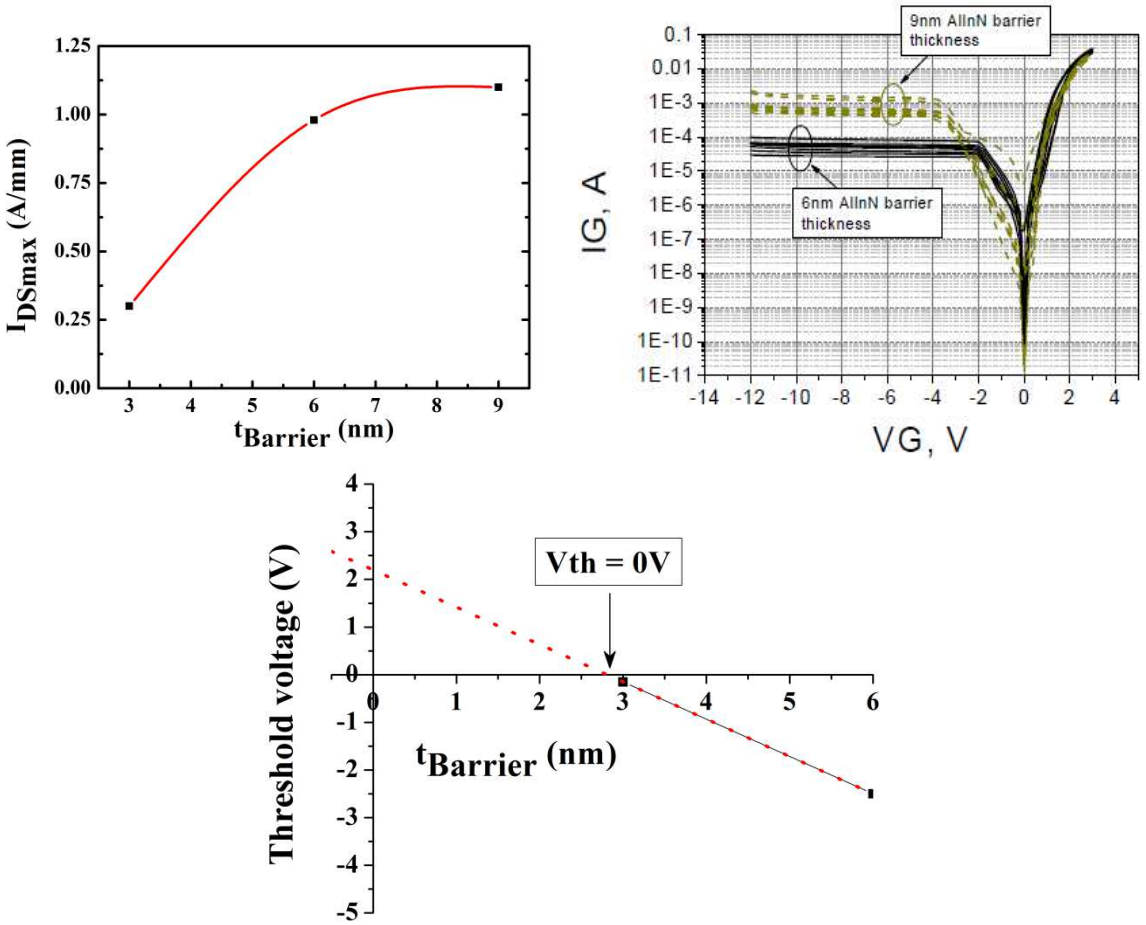


Figure 3.5: The barrier down-scaling also causes a (a) decrease in the drain current density (top left) (b) decrease in the reverse gate leakage current (top right) and (c) decrease in the pinch-off voltage (bottom).

The barrier scaling properties presented in here lead to the choice of 6 nm and 9 nm barriers to be largely used for subsequent power HEMT fabrication. The 6 nm barrier is thick enough to provide high Ns close to the maximum value but not too thick for a relatively low contact resistance and the device has a transconductance around 300 mS/mm which is sufficient for operation frequency in the GHz regime. The drawback of thicker barrier would be the increase in the gate leakage current as shown in Fig. 15b. In this work a novel method of digital oxide deposition (DoD) technique was used to obtain a high quality gate dielectric that allowed a reduction in the gate leakage current. The

gate leakage and the surface passivation were optimized using the DoD method and enhancement of the breakdown voltage was done by experiment and will be discussed in section 0.

3.5 Enhancement of the Breakdown voltage

As discussed in the previous section, considering the AlInN/GaN HEMTs performance 6 nm barriers has been considered as optimum barrier thickness. Although the drain current is higher for 9 nm thick barrier devices suffer from high gate leakage current (see Figure 3.5b) which reduces the reliability and efficiency of the devices. High gate leakage current prevents the GaN HEMTs from reaching their potential for high power level. Increasing the barrier thickness introduce more defects in the barrier that leads to the increased leakage current as Yu *et al.*[3] have shown that the dislocations are the source of gate leakage on an unpassivated GaN sample grown by MOCVD. Considerable interest in this issue has initiated the exploration of dielectrics to reduce the gate leakage. It is necessary that the gate dielectrics explored for GaN transistors should incorporate surface passivation to maintain high power performance. AlN cap layer has been introduced to mitigate the problem. AlN cap layer was grown at high temperature (> 950◦C) in-situ in MOCVD reactor after finishing the growth of HEMT epitaxy. The sample had AlN of 2 nm thicknesses on the surface of the HEMT expitaxy (see Figure 3.6a) which was then fabricated following the standard fabrication process. In Figure 3.6b, the performance of the AlInN/GaN HEMTs with AlN cap layer shows improved device performance.

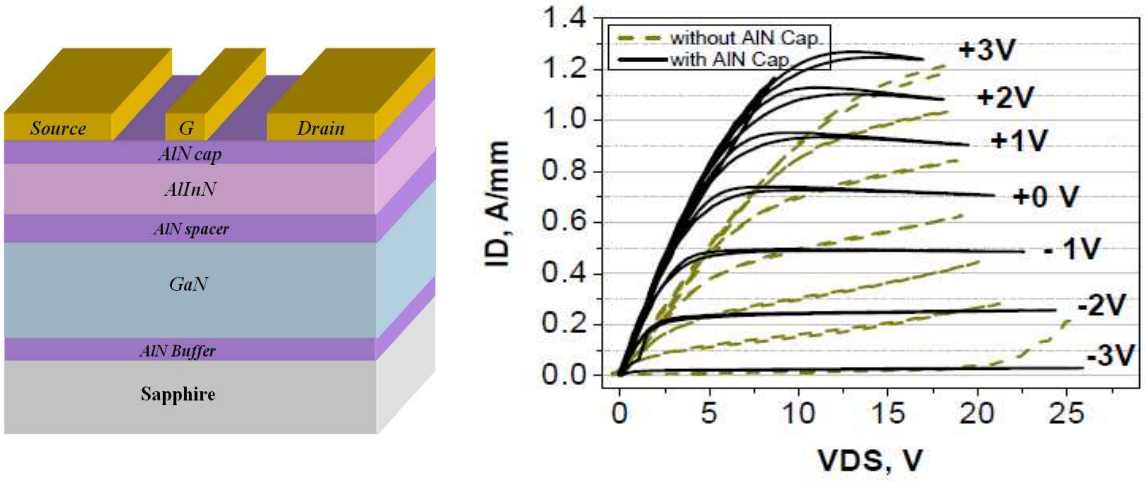


Figure 3.6: (a) Schematic cross section of AlInN/GaN HEMTs with 2 nm AlN cap layer (left) (b) Drain-source currents for AlInN/GaN HEMTs without AlN cap layer (right).

Gate leakage is measured after passivation as a two terminal measurement between gate and drain with source left floating. Gate leakage does not depend on the L*gd* spacing [77] but scales faithfully with device width (will be discussed in chapter 6) and the leakage path is through the AlInN barrier layer at the drain end of the gate. Factors that limit GaN transistor performance are primarily dispersion and gate leakage. Electric field lines which concentrate at the drain-side edge of the gate cause charge injection into the surface traps. This reduces the field concentration at the drain side edge of the gate, but leads to high-frequency current dispersion because the surface traps respond slowly to gate bias. Dispersion is eliminated by an effective surface passivation which leads to electric fields concentrating at the drain-side edge of the gate [78]. Hence low dispersion and high field concentration and hence high gate leakage are linked.

It is known that when the device is at pinch-off the maximum electric field occurs at the drain side edge of the gate [79]. Before passivation the surface states adjacent to the gate fill up with electrons thereby extending the depletion region width. This reduces the peak electric field that is seen at the edge of the gate thus enhancing the breakdown

voltage [Figure 3.7]. However there is dc to rf dispersion in the IV curves as the surface states do not respond fast to the changes in gate bias. The high frequency dispersion is eliminated by passivating the surface with SiN*x* film. After passivation the electric field lines peak at the drain side edge of the gate thereby reducing the breakdown voltage. Engineering low gate leakage while maintaining low dispersion is critical and conveniently achieved by the field-plate technology [80].

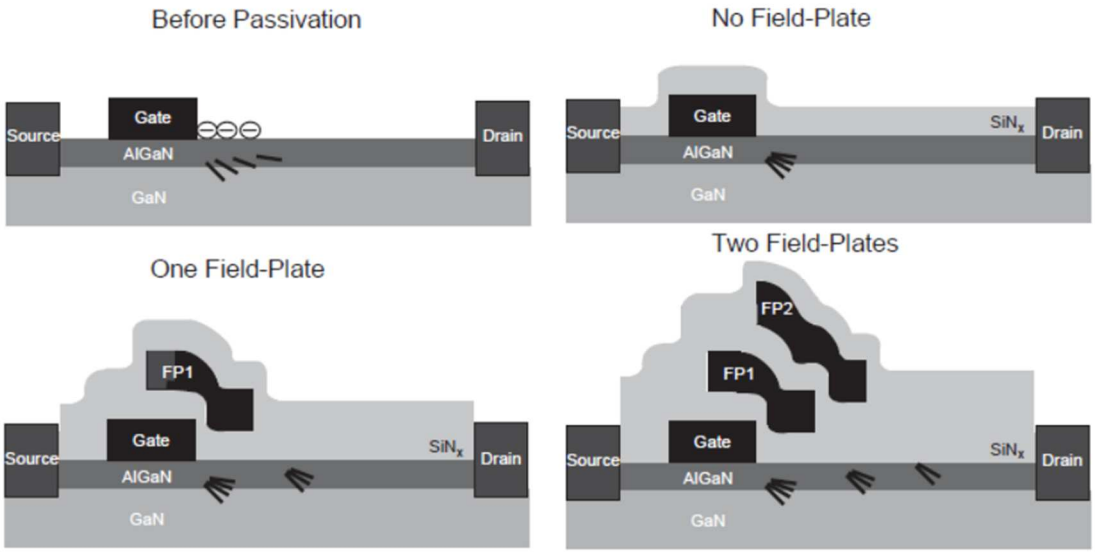


Figure 3.7: Various device scheme with field plates, figure taken from [77]

A field-plate is a metal electrode which offers an additional edge for the electrical field lines to terminate at higher drain bias [Figure 3.7]. This leads to the reduction in the peak electric field at the gate edge. Since the field-plate is a metal electrode the response time is much faster than that of the surface states. The field-plate can be electrically connected either to the source or to the gate. The advantage with gate connected field-plates is that it enables to make them self-aligned to the gate and it allows a better control in tailoring the electric field. This enables a much higher drain bias to be supported

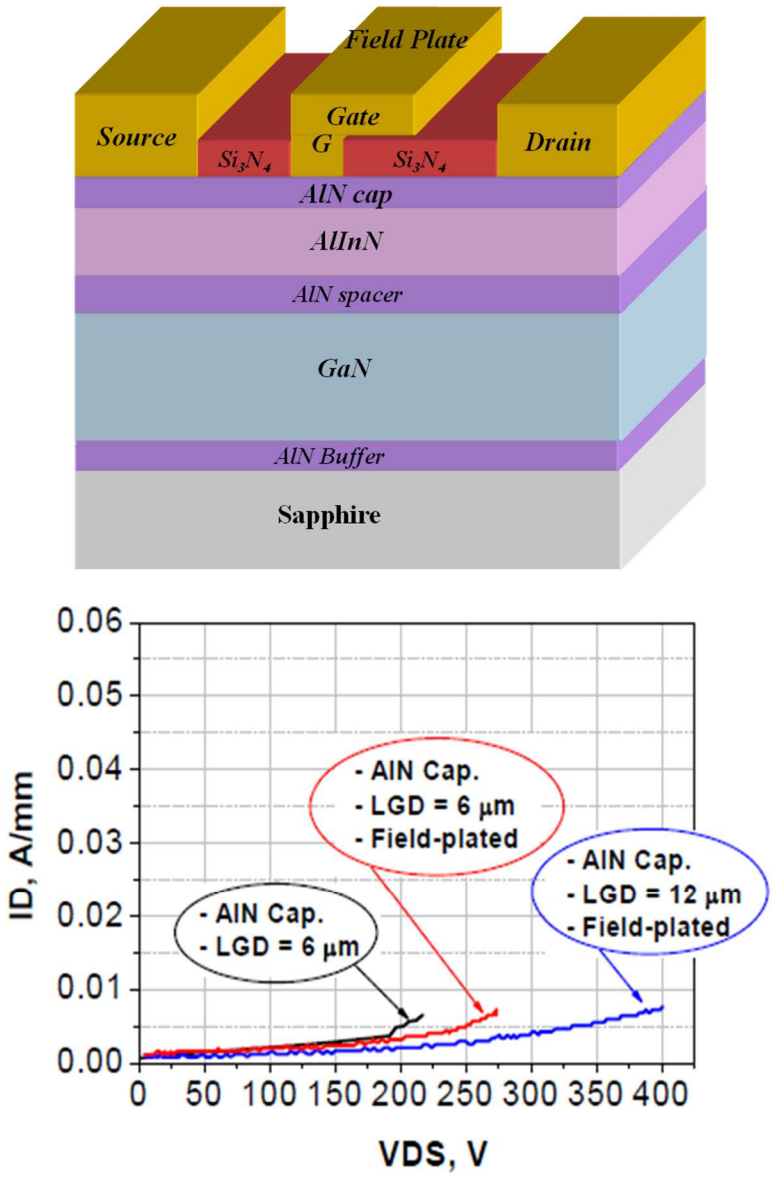


Figure 3.8: (a) Schematic cross section of AlInN/GaN HEMTs with field plate (top) (b) breakdown voltage with different L*gd* spacing and filed plate (bottom).

without exceeding the critical electrical field at which breakdown happens. In this case, after standard device fabrication a surface passivation is done by depositing about 100 nm SiN by PECVD. Field-plate was patterned by photolithography and standard liftoff process. The field-plate (Ni/Au 30/400) is connected to the gate at the gate pad region (see Figure 3.8 a). Devices were then tested using tek370A curve tracer. An increase in the breakdown voltage was observed. They were found to have the three terminal

breakdown voltage increased with increasing gate-drain spacing [Figure 3.8Figure 3.8 b]. For L*gd*=12 μm the breakdown voltage was between 300-400 V. The measured three terminal breakdown voltages at various processing steps are shown in Figure 3.8b. This technique of using field-plate over the passivation dielectric uses simple and well controlled processing steps. The active device area is protected from possible damages in the subsequent processing steps by the passivation dielectric, thereby not affecting the processing yield. The need for using field plate to achieve high breakdown voltage was presented. A strategy for optimizing the parameter space for the field-plates was presented. Fabricated devices with field-plates showed a higher breakdown voltage than the devices without field-plates. With field-plate and 12 um gate drain spacing a breakdown voltage of 400 V was obtained [81].

CHAPTER 4

E-MODE AlInN/GaN MISHEMTs

This chapter will discuss the technological steps needed to achieve the first ever reported enhancement mode (EMOD) AlInN/GaN MISHEMTs with a threshold voltage of above 1.5V. The excellent performance of the EMOD device and the fabrication process applied here to realize the normally off device will be discussed along with other techniques and their advantages and challenges.

4.1 Advantages and Challenges of Enhancement mode AlInN/GaN MOSHEMTs

In a HEMT, the sheet carrier density in the 2DEG channel is modulated by the application of a bias to a Schottky metal gate. These devices are depletion mode (*normally-on*), i.e., a negative bias must be applied to the gate in order to deplete the electron channel and turn. Surely, the most challenging aspect in the present research activity on GaN devices is the development of a reliable way to achieve an enhancement mode (*normally-off*) HEMT. In fact, enhancement mode GaN HEMTs would offer a simplified circuitry (eliminating the negative power supply), in combination with favorable operating conditions for device safety.

From chapter 2, we know that the threshold voltage can be expressed as

$$V_{th} = \Phi_B - \Delta E_c/q - dP_{total}/\varepsilon \qquad (4.1)$$

where Φ_B is the Schottky barrier height (SBH), ΔE_c is the conduction band discontinuity at the heterojunction, P_{total} is the total polarization charge and ε is the dielectric

constant, and d is the barrier layer thickness. According to the equation (4.1), following are the four ways to shift the threshold voltage towards positive,

1. Increasing the Schottky barrier height, Φ_B. Schottky gate metals with higher work functions can be used to increase the SBH. By using Pt-gate instead of Ni-gate, N. Miura et al. achieved a 0.6 V increase in Vth.6 However, the choice of suitable metals is quite limited, and its impact on Vth shift is not significant.
2. Decrease the conduction band discontinuity, ΔE_c between AlInN and GaN by reducing the Al composition in the barrier layer. This will create a lattice mismatch and the purpose of using lattice matched AlInN/GaN for device reliability will not be achieved. Moreover, it will reduce the 2DEG concentration resulting lower drain currents.
3. Fluorine ions (F-) implantation under the gate is a smart option and has been used to achieve normally off AlGaN/GaN HEMTs. Incorporated Fluorine ions act as immobile negative charges that can deplete the 2DEG and positively shift Vth (see Figure 4.1a). Ideally, all the F- ions should reside in the AlGaN barrier. In reality, however, due to the strong channeling effect for the F ions in GaN lattice structure, as well as the non-uniformity in F- ion energy distribution, there is a high chance for some F ions to be deeply implanted into the 2DEG channel, which degrade the electron mobility by impurity scattering. Generally, when converting from D-mode to E-mode, IDS,max drops by more than 40%.
4. The most popular method is to reduce the barrier layer thickness under the gate. Down scaling of barrier layer decreases the pinch off voltage meaning the thinner the barrier layer the lesser the 2DEG carrier concentration would be thus small

applied negative bias would deplete the channel. The drawback of this approach is that the drain-source output current is drops too (see Table 4.1). The selective thinning of the barrier layer just under the gate instead of scaling down the whole barrier is the best way to realize the enhancement mode AlInN/GaN HEMTs. The selective thinning of the barrier can be realized by ICP dry etching, resulting in a recessed-gate structure. With a deep-enough gate-recess etching, the 2DEG can be completely depleted at zero gate bias and E-mode HEMTs are formed (see Figure 4.1b).

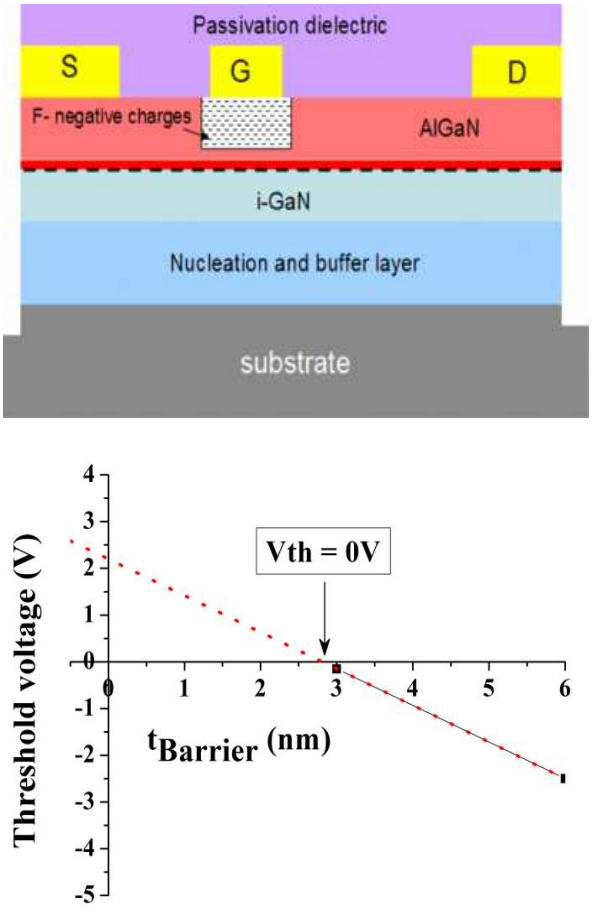


Figure 4.1 : (a) Emode AlGaN/GaN HEMTs using fluorine ion (F-) implantation (left), (b) barrier down scaling causes decrease in the pinch off voltage and shifts the threshold voltage towards positive (right).

Table 4.1 : Down scaling of barrier layer shifts threshold voltages towards positive and decreases the drain current.

Barrier thickness (nm)	Threshold voltage, V_{th} (V)	I_{DSmax} (A/mm)
9	-3.2	1.1
6	-2.8	0.98
3	-0.15	0.3

In the case of the AlGaN/GaN system, various approaches such as gate recessing [83], fluoride plasma treatment [84], p-type gate injection [85] and surface potential engineering with dielectrics [86] have been developed to realize devices with normally Off behavior. However, these approaches are in general not capable of simultaneously achieving low On-resistance; high Off-state breakdown voltage (Vbr), large threshold voltage (Vth), and high drain currents (IDS). Therefore, many of the reported HEMTs showed pinch-off of the channel at gate voltages close to 0V despite the high values for IDS [87,88] A few other research groups have implemented gate-recessed AlGaN/GaN metal insulator semiconductor field-effect transistors (MIS-FETs) to achieve E-mode operation with low gate leakage[89,90]. The devices exhibited threshold voltages that were better than +2.5V and breakdown voltages of 400 V. On the other hand, the drain current density was limited to 200mA/mm when up to 12V bias was applied to the gate. Thus far, Fujitsu Laboratories [91] have realized the best E-mode MIS-HEMTs using a thin three-layer cap structure. They reported a high output current of 800 mA/mm along with a Vth = +3V and a Vbr = 320 V.

Recently, Wang et al. have demonstrated the first enhancement mode AlInN/GaN HEMTs on SiC substrates using plasma-based gate recess etch [82]. The reported pinch-off voltage was only 0.2–0.8 V. In this work, we for the first time report E-mode

AlInN/GaN MOS-HFETs using SiON as the gate insulator. For a gate length of 1.5 um and an 8 um source–drain opening, the devices attained a maximum dc output current density of 0.7 A/mm and a threshold voltage of 1.8 V, respectively. Three-terminal off-state breakdown voltage greater than 345V was observed at 0V gate bias.

4.2 Fabrication process of Normally of AlInN/GaN MISHFETs

Electrical characterization of the as-grown heterostructure showed room-temperature (RT) sheet carrier density and mobility of $2.1 \times 10^{13} cm^{-2}$ and 1338 $cm^2/V.s$, respectively. The corresponding sheet resistance was 204Ω/sq.

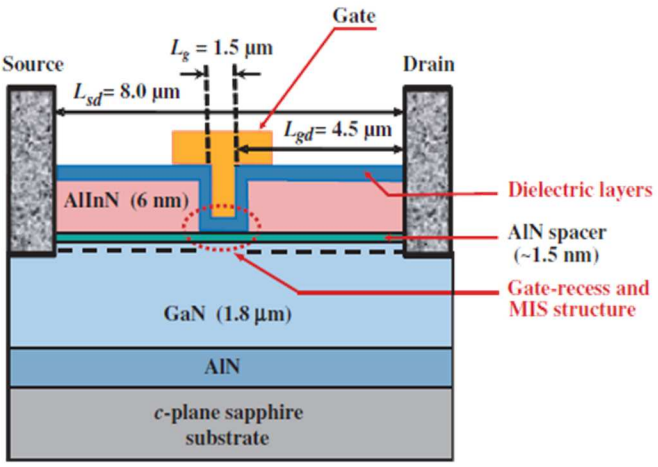


Figure 4.2 : Schematic cross-section of the AlInN/AlN/GaN MOS-HEMT with a recessed-gate geometry and SiON gate dielectric. The gate–drain distance is 4.5um for a channel length of 8 um.

To fabricate the MOS-HFETs, source and drain ohmic contacts separated by a distance of 8 µm were formed on isolated mesas. Measurements of transmission line method (TLM) test structures showed that the contact resistance for this non-optimized Ti-based metal stack was 0.7 Ωmm. After the realization of the source and drain contacts, a SiN passivation layer was deposited in the access region using PECVD. To form the gate footprint, a 1.8 µm long and 100 µm wide trench was first etched in the SiN layer. The

exposed section of the AlInN barrier layer was then removed all the way down to the AlN surface using a controlled and low-power BCl_3 based inductively coupled plasma (ICP) etching and reactive ion etching (RIE) process. A previously reported DoD technique [76] was subsequently used to deposit 30 nm of a high-quality SiON layer within the gate recess region. A 1.5 µm long Ni/Au metallization was finally deposited in the gate recess region on top of the dielectric layer. The gate was placed asymmetrically between the drain and source, with the source–gate spacing being set to 2 µm. A schematic of the fabricated MOS-HFET is illustrated in Figure 4.2. The devices were not passivated after gate definition.

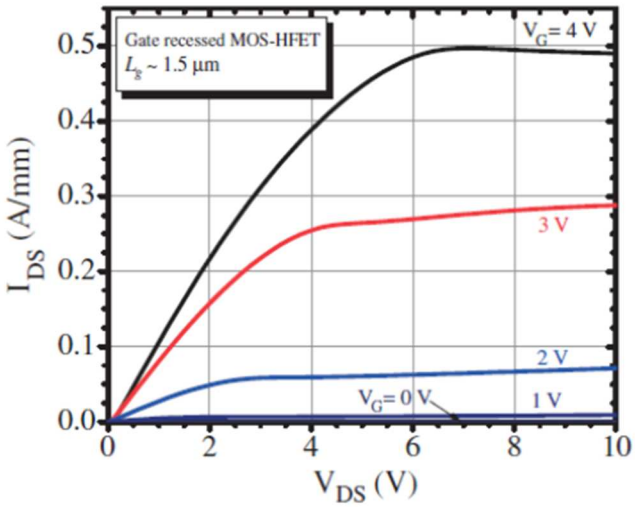


Figure 4.3 : Representative dc source–drain characteristics for the fabricated 1 µm x 100 µm gate recessed AlInN/GaN MOS-HFET. The gate bias VG was varied from 0 to +4V in 1V step.

4.3 Results and Discussion

Typical RT output characteristic curves for the gate recessed MOS-HFET are shown in Figure 4.3. The measurements were performed in dc mode, and the gate bias (V_G) was varied from 0 to +4V in 1V step. The maximum saturation current density for these devices was 0.5 A/mm at V_G = 4 V. In Figure 4.4(a), we plotted the transfer curves

for both the gate-recessed MOS-HFET and the conventional Schottky gate device fabricated from the same wafer and of identical geometry. The results obtained at a drain bias (V_{DS}) of 10V (saturation regime) indicate a large shift of the pinch-off voltage as a result of gate recess, and without noticeable degradation of I_{DS}. More importantly, the 1.5 μm gate MOS-HFET operates in normally off mode with a threshold voltage between +1.5 and +2.0 V, as extracted from the linear extrapolation of the I–V curve. The drain current density at VG = 0V was close to 1mA/mm, and in a few other devices it was as high as 33 mA/mm, due to charge carriers leakage through the GaN buffer. The maximum drain current was 700 mA/mm at VG = 6 V. Figure 4.4(a) also shows the V_{th} for the non-recessed Schottky gate HFET to be about -2.3 V, which corresponds to a depletion-mode operation. The gate-recessed MOS structure has thus caused an about 4V shift in V_{th} owing to the contribution of both the barrier layer thinning and the insertion of a relatively thick dielectric layer between the gate and the channel. The peak extrinsic transconductance (g_{me}) of the Emode device was measured to be 272 mS/mm as compared to a 200 mS/mm for the conventional Schottky gate HFET [see Figure 4.4(b)]. It is interesting to note that g_{me} also increased after the insertion of the 30 nm thick gate insulating layer.

Figure 4.5(a) depicts the gate–source leakage current, I_G, as a function of the gate–source voltage for the AlInN/GaN reference HFET and gate-recessed MOS-HFET. The current was measured both under reverse and forward dc bias. As opposed to Schottky gate E-mode and D-mode HEMTs where, for gate voltage values over +2 V, there is an appreciable increase in the leakage current, our insulating gate MOS-HFETs can easily withstand a gate voltage well over +5 V, while I_G remained significantly below

the µA/mm level. Even at VG = 6 V, the gate current was only about 4.3 nA/mm. Under reverse bias the gate leakage current was found to be better than 550 pA/ mm. Such device performance is attributed to the deposition of a relatively thick gate insulator.

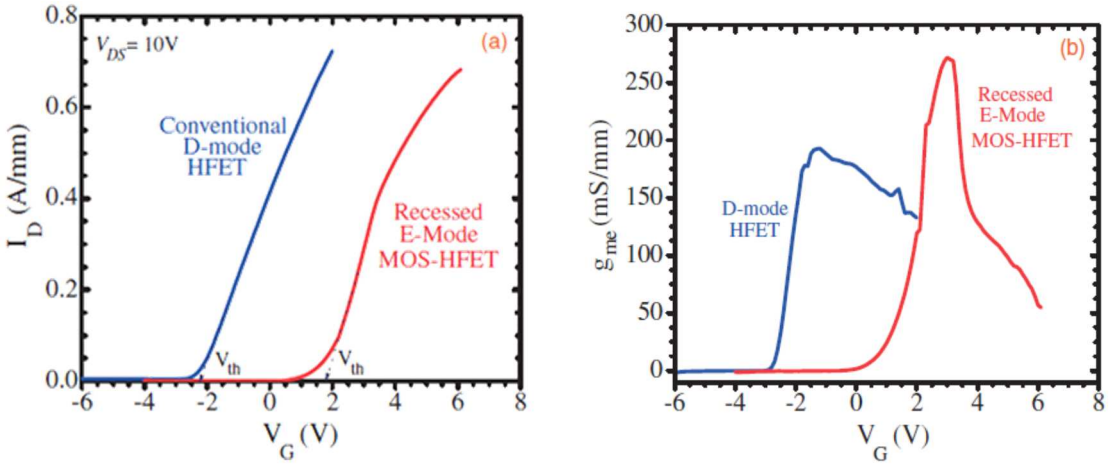


Figure 4.4 : RT transfer characteristics (a) and extrinsic transconductance (b) of identical geometry AlInN/GaN D-mode HFET and E-mode insulating-gate HFET processed from the wafer. V_{DS} = 10 V.

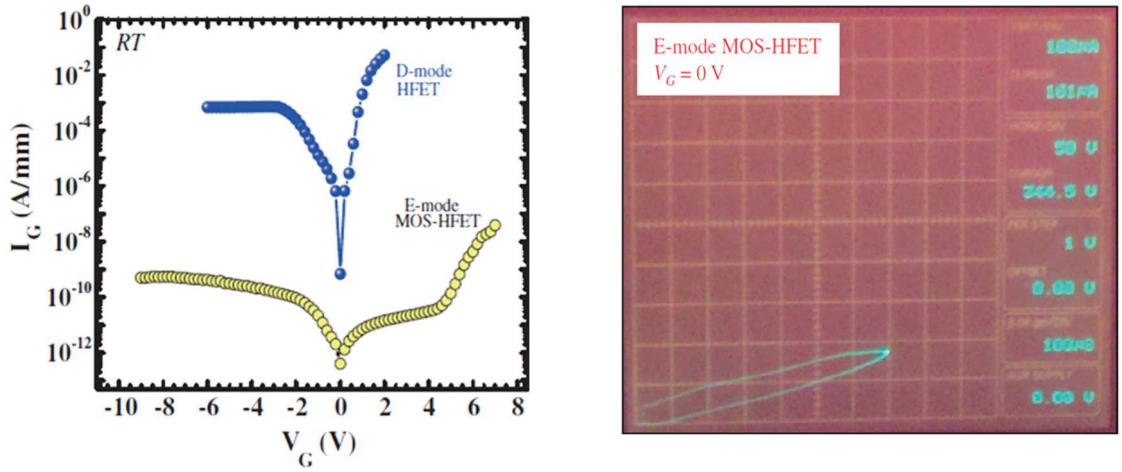


Figure 4.5 : (a) Gate-leakage current I_G as a function of V_G for the 1.5 µm E-mode insulating-gate HFET and a conventional D-mode HFET, (b) Three-terminal Off-state current–voltage characteristic for the E-mode MOS-HFET acquired at VG = 0 V. The gate width was 100 µm and the gate–drain spacing L_{gd} was 4.5 µm.

Three-terminal Off-state breakdown characteristics measurements were also carried out at Vgs = 0V without immersing the samples in Fluorinert. A typical behavior is included in Figure 4.5(b), which shows that the devices with a gate-drain spacing of 4.5

μm sustained drain bias up to 345 V. The drain current was seen to first rise rapidly to ~0.8 mA/mm and then tends to saturate. We believe the initial current rise is due to a buffer leakage issue in our samples. The value of Vbr can be further increased by reducing the buffer leakage and improving the surface passivation process.

To conclude, this work demonstrates AlInN/AlN/ GaN enhancement-mode insulating-gate HFETs. The devices fabrication process involved gate recess etch step and deposition of SiON dielectric layers under the gate. MOS-HFETs with a 1.5x100 μm^2 gate geometry and an 8 μm source-to-drain opening exhibited a maximum dc output current density of ~0.7 A/mm and a threshold voltage in the range of 1.5–2.0 V. The peak extrinsic transconductance was 272 mS/mm measured at VG = 3:0 V.

The gate recessed MOS structure led to about 4V shift in Vth as compared with that of a conventional D-mode HFET. Furthermore, the gate leakage current was suppressed to less than ~4.3 nA/mm at VG = 6V owing to the relatively thick gate insulator. The results of this study clearly show the potential of normally off AlInN-GaN MOS-HFETs as next generation devices for the realization of power electronics systems.

CHAPTER 5

INVESTIGATION OF THE TRANSPORT PROPERTIES OF AlInN/GaN MOSHEMTs ON SiC SUBSTRATE

In this chapter, we investigated the transport properties of SiO_2/AlInN/AlN/GaN MOSHEMTs on SiC substrate. The 2DEG density was deduced from high-frequency capacitance–voltage (*C–V*) measurements. The MOSHEMTs with $L_G < 2.0$ μm are shown to exhibit high drain currents densities of 1.6–1.8A/mm. MOSHMETs investigated in this work received no subsequent surface coating for device passivation. Analytical study in this chapter predicted the zero bias drain saturation current density to be increase by ~23% with the realization of 100 nm gate length MOSHEMTs, which would thus bring their dc characteristics in line with those of the best devices reported in the literature.

5.1 Experiments

The AlInN/GaN epilayer structure was grown on a SiC substrate by MOCVD with a ~4.0 nm thick top barrier layers (including AlN nucleation layer). The devices under investigation in this experiment were realized by standard transistor fabrication process (described in chapter 3). A schematic drawing of the device is depicted in the inset of the Figure 5.1. Small gate length devices (*L*G = 1.8–2.0μm) as well as devices with *L*G varying from 10 to 100 μm were processed from the same wafer. The resulting contact resistance (*R*c) was determined to be 1.35 Ω-mm from the on-wafer transmission

line method (TLM) test patterns measurements. The epiwafer exhibited a sheet resistance *R*sh of 250 ± 4 Ω/sq, which was in good agreement with the results obtained using Lehighton RF contactless mapping system. Room temperature (RT) current–voltage (*I–V*) and *C–V* measurements were carried out using Agilent 4516B semiconductor parameter analyzer and Agilent 4284A LCR-meter, respectively.

5.2 Investigation of The Transport Properties

Figure 5.1 shows a *C–V* curve measured at 1MHz for a MOS heterostructure device with an 80 × 200 μm^2 gate contact area. As the gate bias is raised above −4V, the gate-to channel capacitance per unit area *C* rapidly increases to reach the value of *C*tot ~ 350 nF/cm^2, which corresponds to the series capacitances of SiO_2 (C_{ox}) and the (AlN+AlInN) barrier layers (C_b). When the gate bias is increased towards more positive values and above 0.7V, a second step-like increase in the diode capacitance manifests itself. The occurrence of such a bump in the *C–V* curves reflects the electrons real space transfer from the AlN/GaN interface to the SiO_2/AlInN interface and measures the unit area capacitance of the SiO_2 film [102, 103]. The oxide thickness d_{ox} was extracted to be 8.8±0.3 nm using $d_{ox} = \varepsilon_0\varepsilon_{ox}/C_{ox}$ with ε_{ox} = 3.9 (SiO2 film dielectric constant [75,76]), which is in fair agreement with the targeted value. The AlInN barrier thickness (d_{AlInN}) was next determined from the value of C_b using the relationship: $d_{AlInN} = (\varepsilon_0\varepsilon_{AlInN}/C_b) - (d_{AlN}\varepsilon_{AlInN}/\varepsilon_{AlN})$. Assuming ε_{AlInN} (17% In) = 11.5 [104] and ε_{AlInN} ~ 9.0 [105], the average value of d_{AlInN} was found to be ~3.0 nm.

For any given gate voltage, the electron sheet density was next estimated from the *C–V* characteristic according to the equation:

$$n_s(V_G) = \frac{1}{q}\int_{V_T}^{V_G} C(V_G)dV_G \tag{5.1}$$

where q is the elementary charge and V_G the gate voltage. As depicted in Figure 5.1, the results show a linear dependence of ns versus V_G when the gate bias is varied from the threshold value up to about +1V. The curve then takes a different slope with the onset of real space charge transfer. This behavior is similar to that observed in SiO_2/AlGaN/GaN MOSHEMTs [102], and the curve offset from the straight solid line (shown in blue) represents the density of the electrons accumulated at the dielectric/AlInN barrier interface. After testing several devices, the average value of ns at V_G = 0V is found to be ~7.4×10^{12} cm^{-2}.

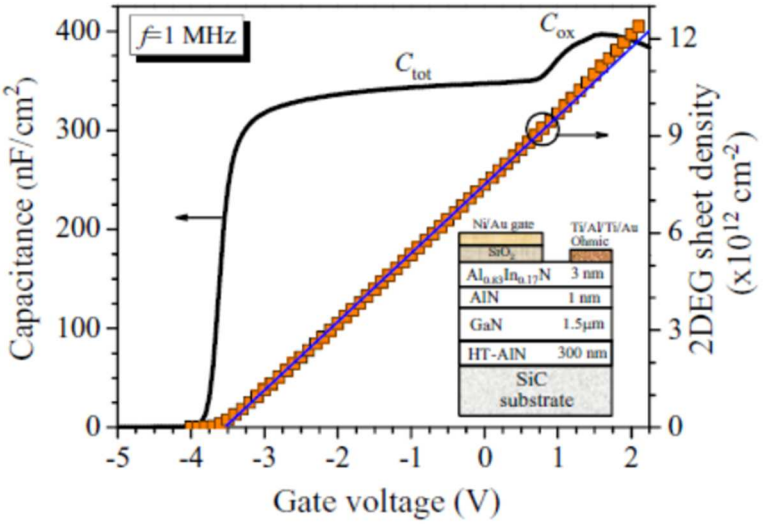


Figure 5.1: *C–V* characteristic of the SiO2/AlInN/GaN heterostructure device measured at 1MHz and the corresponding gate-bias dependence of the channel sheet carrier density.

Figure 5.2 displays the conduction band profile and carrier distribution for the $Al_{0.83}In_{0.17}$ N/AlN/GaN heterostructure with 4 nm total barrier thickness, obtained using a one dimensional self-consistent Schrödinger–Poisson equations solver. The materials parameters were mostly taken from [104,105] and the barrier height of Ni/AlInN was estimated assuming it is equal to the difference between the metal work function and the

semiconductor electron affinity. The calculated sheet carrier density for the HEMT structure is ~1.2×10^{13} cm^{-2}, which is very close to the data of $(1.0 \pm 0.1) \times 10^{13}$ cm^{-2} obtained both theoretically [96] and experimentally (Hall measurement) [97, 106] for lattice-matched heterostructures with a 3 nm thick AlInN barrier layer. The aforementioned MOSHEMT channel sheet carrier density thus seems to be much lower than the 2DEG charge density reported for the Schottky gate counterparts. Note that it is not uncommon to measure a lower *n*s for nitride-based insulated gate transistors when this parameter is deduced from *C*–*V* characteristics [102, 107] whose profiles can be strongly affected by the frequency of the ac input signal selected during the measurement. When this occurs, it usually suggests the presence of trap sites, and the higher the density of these defects the larger is the difference between the expected and measured values of *n*S. In the case of our MOSHEMTs, the interface trap density (*D*it) estimated using the low- and high-frequency capacitance method [108] was indeed relatively high, i.e. ~5.3×10^{12} cm^{-2} eV^{-1} at V_G = 0V. There was also evidence of a large current dispersion after acquiring current–voltage curves in pulsed mode for a MOSHEMT with a 2×100 μm^2 gate geometry, as shown in Figure 5.3. The dynamic *I*–*V* experiments were carried out using a DIVA™ system at three quiescent bias points (*V*DS0, *V*GS0): zero-field (0V, 0 V), gate lag (0V, −6 V), and drain lag (20V, −6 V). The pulse width and pulses separation were set to 200 ns and 1 ms, respectively. Drain current density reductions by about 59% (gate lag) and ~50% (drain lag) were measured in our sample at V_{DS} = 13V and V_{GS} = +2V, and both factors approached the 70% levels at *V*GS = 0V (*V*DS = 10 V). Compared to unpassivated AlInN/GaN HEMTs [26], the gate and drain lag effects appear to be much more pronounced in our MOSHEMTs.

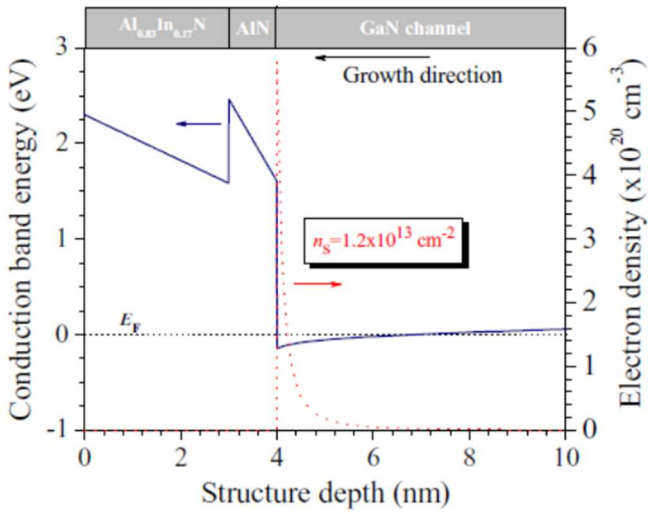


Figure 5.2: Band diagram and 2DEG distribution along the growth direction for the Al0.83In0.17N/AlN/GaN heterostructure.

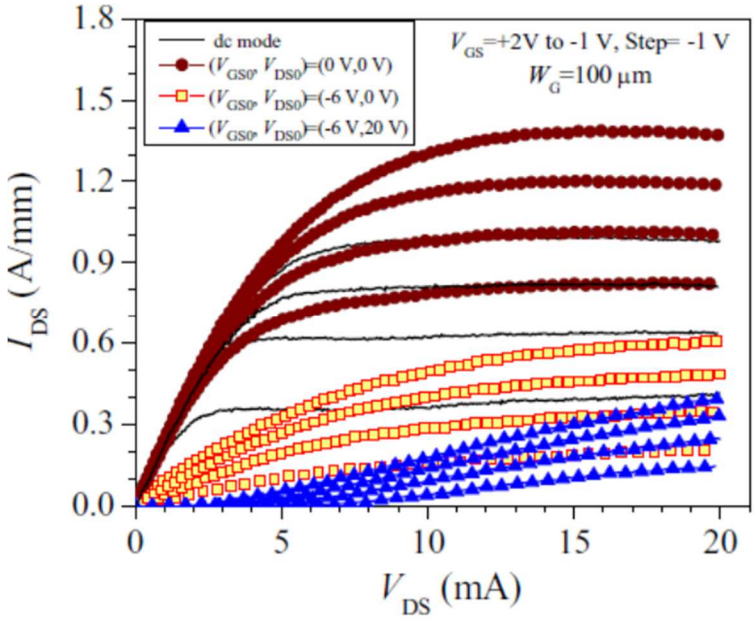


Figure 5.3: Static and pulsed *I–V* characteristics measured for a 2.0 × 100 μm2 MOSHEMT. The dynamic *I–V* curves were acquired using 200 ns pulses with the following quiescent points (*V*DS0, *V*GS0): (0V, 0 V), (0V, −6V) and (20V, −6 V).

Figure 5.4(*a*) shows the static output characteristics of SiO_2/AlInN/GaN MOSHEMTs with a gate width, W*g* = 50 μm, a source-to-drain distance, L_{SD} = 7μm and L_G = 1.8μm. All devices that were tested were completely pinched-off at −4V gate bias, and their maximum drain–source saturation currents (I_{DSmax}) were in the range 1.2–

1.4A/mm at *V*GS = +2V and 1.6–1.8A/mm at *V*GS = +4V (for devices with similar gate width and length). It is worth nothing that there have not been many reports on thin barrier AlInN/GaN heterostructures due to the basic fact that the channel sheet carrier density as well as the electron mobility decrease with reducing thickness of the AlInN layer [96,97]. Yet, the devices investigated in this work exhibited excellent dc characteristics even in the presence of a relatively large *D*it. Such behaviour reflects the improved epilayer crystal quality, the excellent interface between AlN and GaN buffer and the epiwafer low sheet resistance [94, 110]. Furthermore, our MOSHEMTs dc performance appears to exceed that of the majority of the insulated gate HEMTs reported in the literature, which are generally fabricated using high-*k* dielectrics (for example Al_2O_3 , ZrO_2 or HfO_2 [99]) for both device passivation as well as gate insulator.

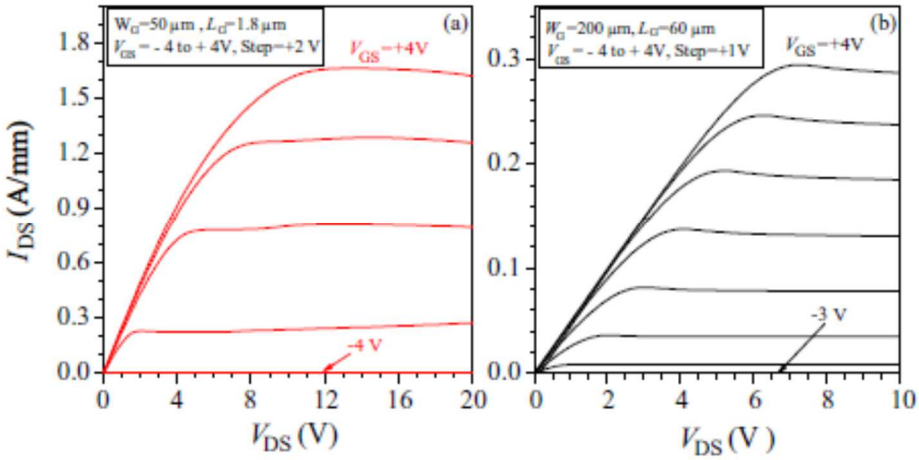


Figure 5.4: Representative static output *I–V* characteristics for MOSHEMTs on SiC with 1.8 × 50 μm2 (*a*) and 60 × 200 μm2 (*b*) gate geometries.

Figure 5.5 compares the maximum dc current density measured for our MOSHEMTs with the state-of-the-art dc results reported in the literature for Schottky gate HEMTs and MISHEMTs. The majority of these (reference) devices were passivated and fabricated using sub-micrometer gate lengths (L_G = 500 nm), primarily as candidates

for high frequency applications. As seen from the survey in Figure 5.5, the highest drain current density measured to date for AlInN/GaN MISHEMTs has been demonstrated by Alomari *et al* [101]. Their 250 nm gate length device, with a 9.5 nm total barrier layer and a 1.5 nm thick native-oxide filled recess as the dielectric, exhibited a 2.4A/mm drain current density at V_{GS} = +2.5V. For AlInN/GaN HEMTs, the record for I_{DSmax} currently stands at 2.5A/mm, which was achieved for a 100 nm device with an 8.4 nm barrier layer [95]. Interestingly, the performance of our MOSHEMT does seem to fairly follow the trend represented by the dotted line despite exhibiting a relatively larger gate size.

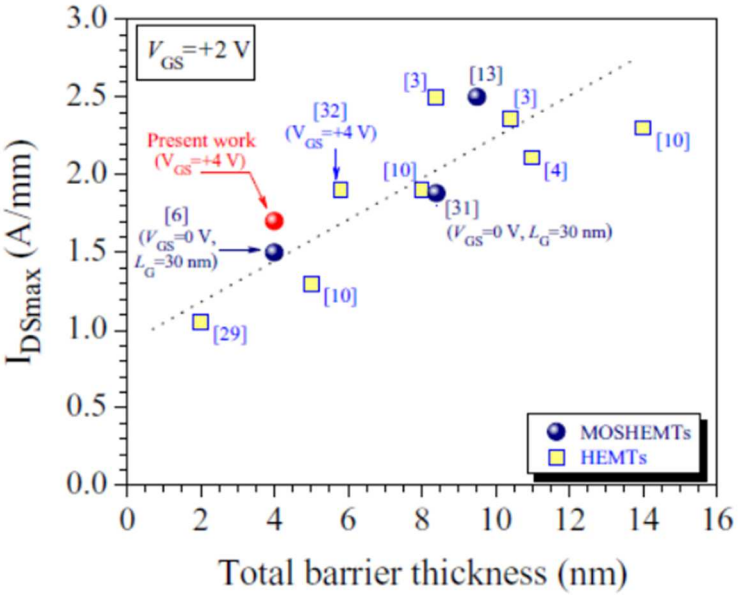


Figure 5.5: Survey of the maximum dc drain current density reported for the state-of-the-art HEMTs and MISHEMTs. The result obtained for our MOSHEMT is also included for comparison.

Channel conductance (*G*ch) measurements were next implemented to determine the variation of the electrons effective mobility (also known as the low-field drift mobility μd) as a function of the sheet carrier density. For this purpose, a MOSHEMT with *L*G = 60 μm and drain-to-gate (*L*DG) and source-to-gate (*L*SG) openings of 8μm were used. The device corresponding *I*–*V* characteristics are shown in Figure 5.4(*b*),

indicating a maximum drain saturation current density of ~0.3A/mm at VGS = +4V. μd was calculated using the equation:

$$\mu_d(V_{GS}) = \frac{G_{ch}(V_{GS})L_G}{qW_G n_s(V_{GS})} \tag{5.2}$$

where L_G = 60 μm and W_G = 200 μm. For a given V_{GS} (and so ns), G_{ch} represents the slope of the I_{DS}-V_{DS} curve measured at V_{DS} = 100 mV. The 2DEG density is known for the different gate voltages from the integration of the C–V characteristic measured at 1 MHz.

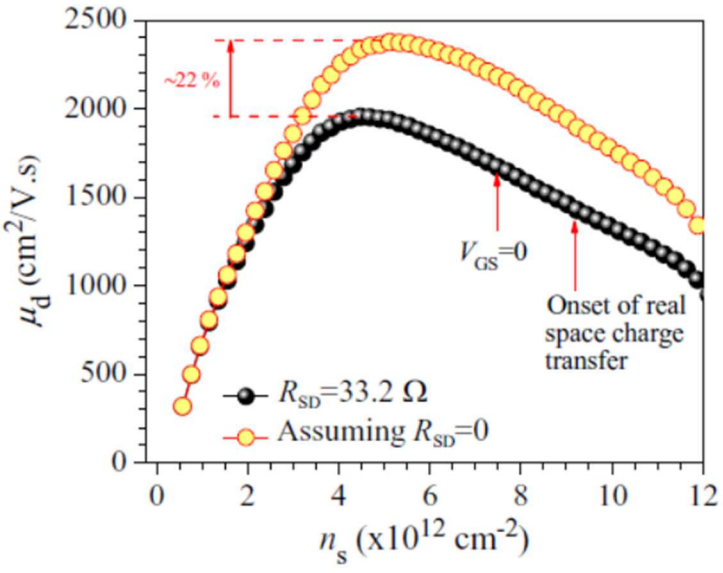


Figure 5.6: Sheet carrier density dependence of the drift mobility derived from the channel conductance measurements for a fat-gate MOSHEMT (LG = 60 μm) and corrected for the series resistance effects.

Since the drain current also depends on the source–drain series resistance R_{SD}, μd is also affected by the value of R_{SD}. The channel conductance in the presence of R_{SD} can be expressed as [111]

$$G_{Ch}(R_{SD}) = \frac{G_{ch0}}{1 + G_{ch0}R_{SD}} \tag{5.3}$$

G_{ch0} is the drain conductance for R_{SD} = 0. R_{SD} consists of the source and drain contact resistances plus the sheet resistance of the access regions. It can be written as follows:

$$R_{SD}W_G = 2R_C + R_{sh}(L_{DG} + L_{SG}) \quad (5.4)$$

where R_{sh} is the channel sheet resistance. Given $L_{DG} = L_{SG} = 8\mu m$ for our devices, R_{SD} is determined to be equal to 33.2Ω.

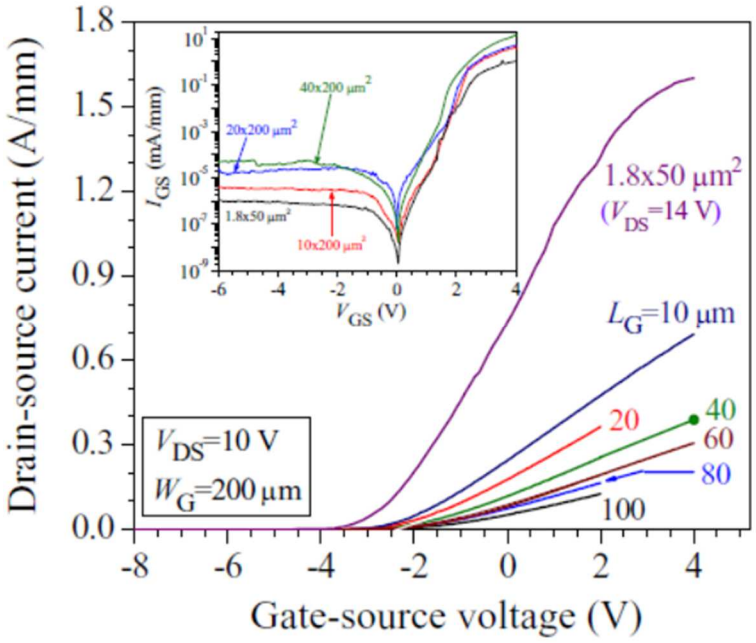


Figure 5.7: Transfer characteristics measured in the saturation region for MOSHEMTs with different gate lengths. The inset depicts the associated gate leakage currents acquired for some of the devices.

Figure 5.6 illustrates the channel carriers drift mobility as a function of *n*s. Mobility is found to increase with decreasing channel sheet carrier density until it reaches a peak value of 1954 $cm^2V^{-1}s^{-1}$ for *n*s = 4.5× 10^{12} cm^{-2} (attained at *V*GS = −1.4V*)*. The zero-bias mobility (μ_{d0}) is 1670 $cm^2V^{-1}s^{-1}$, which appears to be identical to the value reported for Al_2O_3/AlGaN/GaN MOSHEMTs exhibiting a similar 2DEG sheet density [112]. Furthermore, the mobility remains overall in excess of 1000 $cm^2V^{-1}s^{-1}$ when the device is biased above the threshold voltage and up to +2V. Next, we simulated the variation of μd versus *n*s for the same MOSHEMT when the influence of R_{SD} is neglected (i.e. $R_{SD} = 0$), which is usually a valid assumption when the gate length is designed very large compared to L_{DG} and L_{SG}. The drain–source resistance can be further reduced with

surface passivation. For our MOSHEMT design, Figure 5.6 shows that not taking into account the source resistance and drain resistance effects would lead to an overestimation of the maximum mobility by approximately 22% and the shift between the two curves becomes more important (up to 33%) at higher *n*s.

Figure 5.7 shows the transfer characteristics of the insulated gate HEMTs with different gate lengths measured in the saturation regime. As seen from the figure, at any given V_{GS} greater than the threshold voltage, the drain saturation current increases with decreasing L_G. Moreover, *Vth*, which was determined from the linear extrapolation of the $(I_{DS})^{0.5}$–V_{GS} curve to zero drain current, shows a small roll-off of about 0.5V (from −3.1 to −3.5 V) when the gate length is reduced from 100μm down to 10μm (W_G = 200 μm). For the smaller gate length device (1.8 × 50 μm^2), *Vth* was about −3.6V. One should also mention that a small hysteresis (~200 mV) was observed when the I_{DS}–V_{GS} curves were acquired using a forward, followed by a reverse, gate voltage sweep.

The inset of Figure 5.7 depicts the insulated gates *I*–*V* characteristics obtained for some of the MOSHEMTs. The drain contact was kept floating during these experiments. Because of the insertion of the oxide layer, the gate leakage currents, I_{GS}, were very low and also much better than the characteristics of our AlInN/GaN HEMTs [81, 100]. Under reverse bias, the absolute value of I_{GS} ranged between 4 nA/mm and 13μA/mm at V_{GS} = −6V for the devices with gate lengths of 10μm, and these levels remain reproducible down to −10V. The reverse leakage current, on the other hand, was ∼1 nA/mm for the MOSHEMTs with L_G = 2μm and W_G = 50 μm. Under forward bias, the characteristics of the insulated gate diodes exhibited leakage currents that increased from 17μA/mm (L_G = 10 μm) to 0.8mA/mm (L_G = 80 μm), at *V*GS = +2V. Here again, I_{GS} is lower for the 1.8 ×

50 μm^2 device with 10μA/mm, and is of the same order of magnitude as the values reported for AlInN/GaN MOSHEMTs fabricated using different dielectric materials [98-101]. At V_{GS} = +4V, it can be seen that I_{GS} further increases to reach 4.3–29.7mA/mm for the large gate devices versus ~1mA/mm for the 1.8μm device. Overall, I_{GS} is found to scale with the gate length, which was expected given the fact that the gate leakage current per unit area J_{GS} *(I_{GS} = J_{GS} ∗ L_G)*, exhibited a similar dependence on gate voltage, irrespective of the gate dimensions (not shown here).

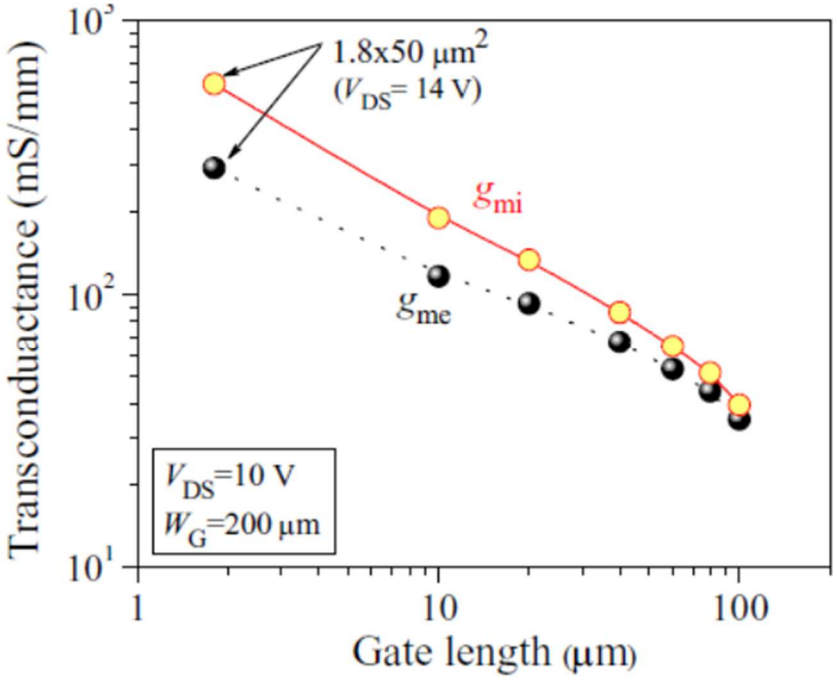


Figure 5.8: Maximum extrinsic transconductance (*g*me) and intrinsic transocnductance (*g*mi) for MOSHEMTs with different gate length. *g*mi = *g*me*/(*1 − *g*me*R*s*)*, where *R*s is the series resistance on the source side.

A close look at the I_{GS}–V_{GS} curves reveals a rapid increase in the current for all devices when the gate bias is raised from 1.4 to 2.4V, similar to the behavior observed with Schottky gate transistors. Earlier studies have shown that the forward current transport in AlInN/AlN/GaN Schottky [113] and MIS diodes [114] is initially dominated by carrier tunneling via defects before other current components such as thermionic

emission and generation recombination may become important. The relatively large gate leakage current observed in our MOSHEMTs at high gate bias is believed to be device process-related, i.e. is closely associated with the lower SiO_2 film quality.

The extrinsic transconductance (g_{me}) of AlInN/GaN HEMTshas previously been shown to increase with decreasing barrier thickness [99] due to a resulting increase of the gate to source capacitance. The gate length appears to have a noticeable influence on g_{me} magnitude as well. As seen in Figure 5.8, the maximum extrinsic transconductance is found to increase with decreasing L_G, reaching 290mS/mm for the MOSHEMT with L_G = 1.8μm. To account for the difference between some of the MOSHEMTs series resistances, we also plotted in log–log scale the intrinsic conductance, g_{mi}, defined as $g_{mi} = g_{me}/(1 - g_{me}.R_s)$. A similar trend is again observed for g_{mi}, but in this case the curve exhibits a much linear profile for smaller gate lengths compared to g_{me} data, and more importantly is consistent with the expected parameter decrease inversely proportional to L_G [115,116]. To further evaluate the potential of our MOSHEMTs, we studied the gate-length dependence of the maximum dc drain saturation current density at zero gate bias (I_{DS0}) using an analytical model we had previously applied to the AlGaN/GaN system [117]. The experimental data acquired at VGS = 0V were thus fitted using the following approximation:

$$I_{SD0} = \beta \frac{V_T^2}{1 + \beta R_S V_T + \sqrt{1 + 2\beta R_S V_T + \frac{V_T^2}{V_L^2}}} \tag{5.5}$$

where V_T is taken = −3.3V, $\beta = C\mu_e/L_G$ and $V_L = v_s L_G/\mu_e$, μ_e being the electron mobility and v_s the electron saturation velocity. μ_e and v_s were selected as the fitting parameters. Good agreement between the analytical curve (depicted by dotted line in Figure 5.9) and

the measured I_{SD0} (solid circles) was achieved for μ_e = 1460 cm^2/Vs and v_s = 4.7 × 10^6 cm/s. The electron mobility is ~12% lower that the experimental value derived from both the channel conductance and 1MHz *C–V* curves. Given the small discrepancy between the outcomes of the two methods, the simulation results were able to provide a reliable insight into the drain saturation current rating for downscaled devices, predicting an increase of I_{SD0} by about 23% when the gate length is reduced from ~1.8μm down to 100 nm. Our MOSHEMTs capability to achieve such output current enhancement is very realistic if one considers the experimental work by Palacios's group [95], wherein improvements of I_{SDmax} by 15% to 20% have been demonstrated in unpassivated InAlN/GaN HEMTs by just reducing the gate length from 250 to 100 nm (see solid star symbols in Figure 5.9).

Furthermore, Figure 5.9 also illustrates the variation of the maximum drain current density versus L_G for V_{GS} = +2V and +4V. The experimental data seem to follow the same trend as the plot of I_{SD0} and therefore one could assume that a similar enhancement in the maximum output current can also be reprodued in the submicrometre MOSHEMT devices for *V*GS > 0V.

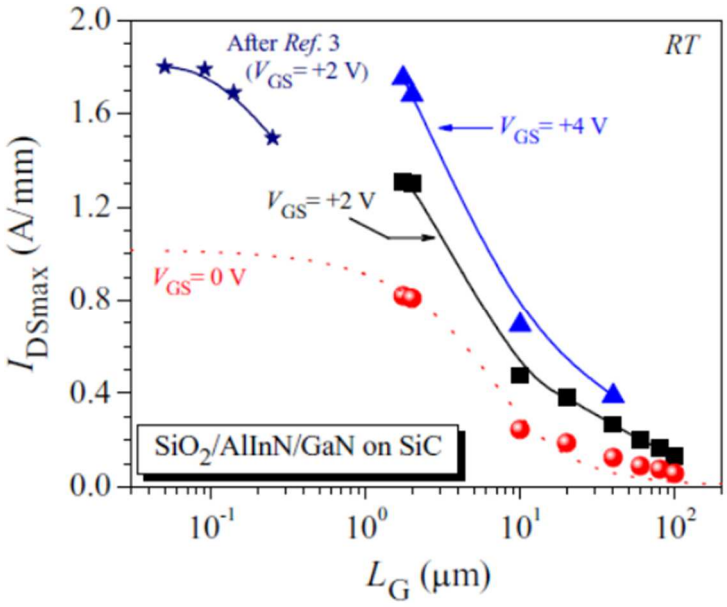


Figure 5.9: Gate length-dependence of the SiO2/AlInN/GaN MOSHEMT maximum drain saturation current density for *V*GS = 0, +1V and +2V. Symbols represent the experimental data. The dotted line represents the fitting curve of the zero-gate bias data obtained using the analytical model described by equation (5.5). The solid lines serve as a guide to the eye only.

5.3 Discussion and Conclusion

We investigated the transport properties of charge carriers in AlInN/AlN/GaN MOSHEMTs fabricated using SiO_2 as the gate insulator. In spite of the thin top barrier thickness the epiwafer exhibited a sheet resistance of ~250Ω/sq that is a clear evidence of the high epilayers crystal quality and smooth heterointerfaces. Unpassivated devices with different gate lengths ranging from 1.8 to 100μm were processed and characterized using *I–V* and *C–V* measurements. A threshold voltage of −3.6V, drain saturation current densities as high as ~1.8A/mm at V_{GS} = +4V and low reverse gate leakage currents were measured for the devices with L_G = 2.0 μm. The levels of I_{SDmax} are predicted to attain higher values by further reducing L_G down to 100 nm. The zero-bias electron drift mobility was ~1670 cm^2/Vs, which was extracted using the channel conductance of a 60μm MOSHEMT device and taking into account the drain–source resistance.

Furthermore, like in the AlGaN/GaN system, the gate length was found to significantly affect the extrinsic transconductance of the MOSHEMTs, causing it to increase with decreasing L_G. The highest *g*me value was 290mS/mm measured for 1.8×50 μm2 gate geometry devices. However, improvements of the barrier surface preparation process and the oxide layer quality to reduce interface traps density, here estimated to be $\sim 5.3 \times 10^{12}$ cm^{-2} eV^{-1} at $V_G = 0V$ must be pursued to unlock the full potential of these MOSHEMTs for high power applications in the RF and microwave frequencies and match the performance previously demonstrated by insulated gate AlInN barrier HEMTs fabricated using high-*k* dielectrics or a thermal native oxide.

CHAPTER 6

QUATERNARY BARRIER AlInGaN/GaN HEMTs GROWN ON SAPPHIRE SUBSTRATE

In this chapter, the growth and characterization of nearly lattice matched quaternary AlInGaN/GaN heterostructure is described, analyzed and discussed. A comparative study of the standard AlInN/GaN HEMTs and AlInGaN/GaN is presented here that shows an enhanced DC performance for the heterostructure with quaternary barrier layer. Crack-free lattice-matched $Al_{0.85}In_{0.15}N$/GaN heterostructures were grown on sapphire substrates with barrier thicknesses up to 6 nm with 2-3% Ga in the barrier layer which exhibit very high polarization-induced electron sheet density located at the hetero-interface. Incorporation of Ga composition from 0% (AlInN) to 2-3% (AlInGaN) increased the 2DEG density from 1.96×10^{13} cm^{-2} to 2.03×10^{13} cm^{-2} with corresponding electron mobilities of 1309 cm^2 /V s and 1454 cm^2 /V s, respectively. The AlInGaN/GaN heterostructure exhibited a low sheet resistance of 211 ohm/sq at room temperature. The MOSHEMTs having 1.8 μm long gate dimensions and a 8μm source-drain separation exhibited a maximum transconductance of 200 mS/mm and the maximum saturation drain current density was 700 mA mm^{-1} at +2 V gate bias with good pinch-off characteristics. Fewer reports are available on AlInGaN material properties concerning RF application [7, 8] and features like high electron mobility, high sheet carrier concentrations or polarization matching motivates this material issue with impressive potential for both RF and optoelectronics.

6.1 Nearly lattice-matched AlInGaN barrier layer

The AlInN/GaN HEMT structure was grown by MOCVD on a 2 in. diameter (0001) sapphire substrate consisting of an AlN nucleation layer, 1.8 μm of semi-insulating GaN buffer layer, 15 Å of AlN spacer and an $Al_{1-x}In_xN$ barrier layer grown to a thickness of 6 nm with 17% In content with 2-3% Ga incorporated in the $Al_{1-x}In_xN$ barrier layer as confirmed by X-ray diffraction measurements. For comparison, a conventional ternary $Al_{1-x}In_xN$ HFET structure was utilized without any Ga in the barrier layer. One of the problems is the difficulty of growing AlInN with low Ga incorporation and uniform In concentration [119] making the growth of AlInN a challenging task.

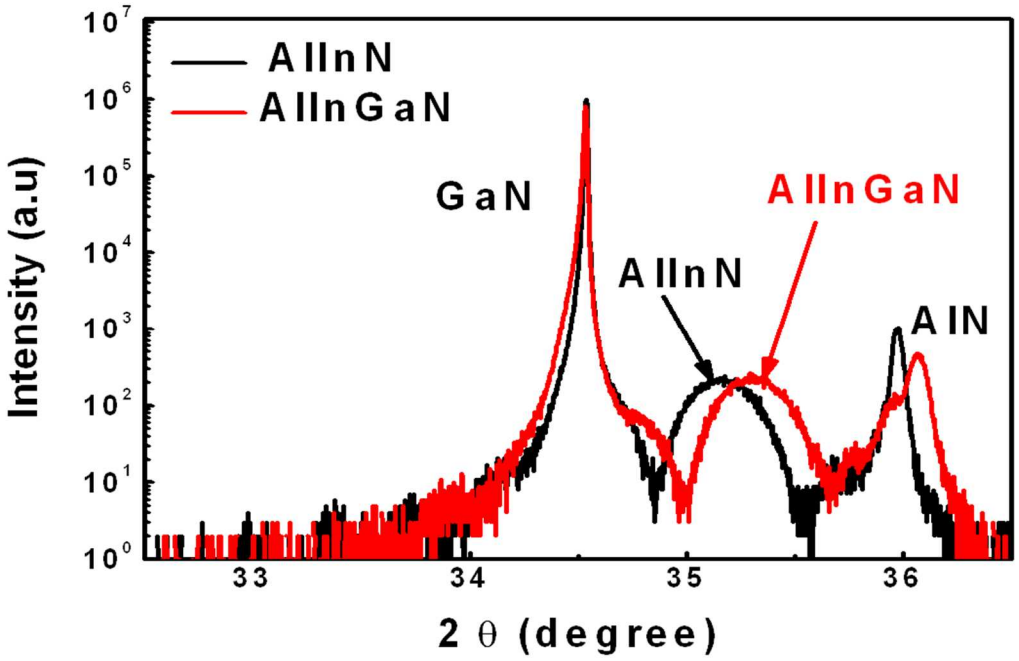


Figure 6.1: XRD ω~2θ scan of quaternary AlInGaN/GaN and ternary AlInN/GaN heterostructures.

The growth conditions of two heterostructures were exactly same except for the barrier layers. Figure 6.1 shows the XRD ω−2u scan for both HFET structures. Electrical characterization of the as-grown heterostructure showed averaged room-temperature (RT)

sheet carrier density and Hall mobility of 1.8×10^{13} cm^{-2} and 1595 $cm^2\ V^{-1}\ s^{-1}$ respectively for the sample with 2-3% Ga in the barrier layer.

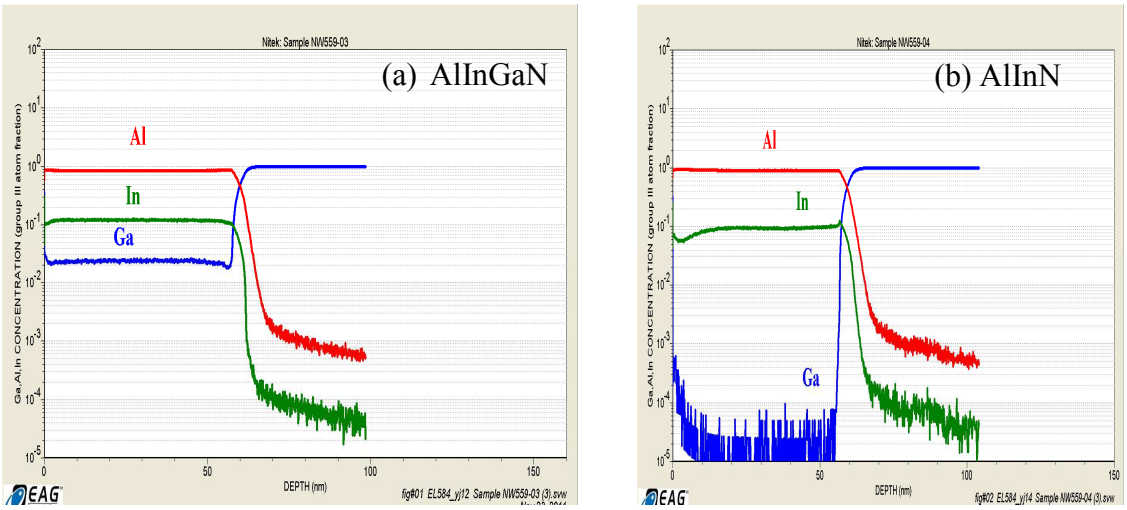


Figure 6.2: SIMS depth profiles of shows (a) about 2% Ga in AlInGaN barrier layer and (b) AlInN barrier layer with Ga in it.

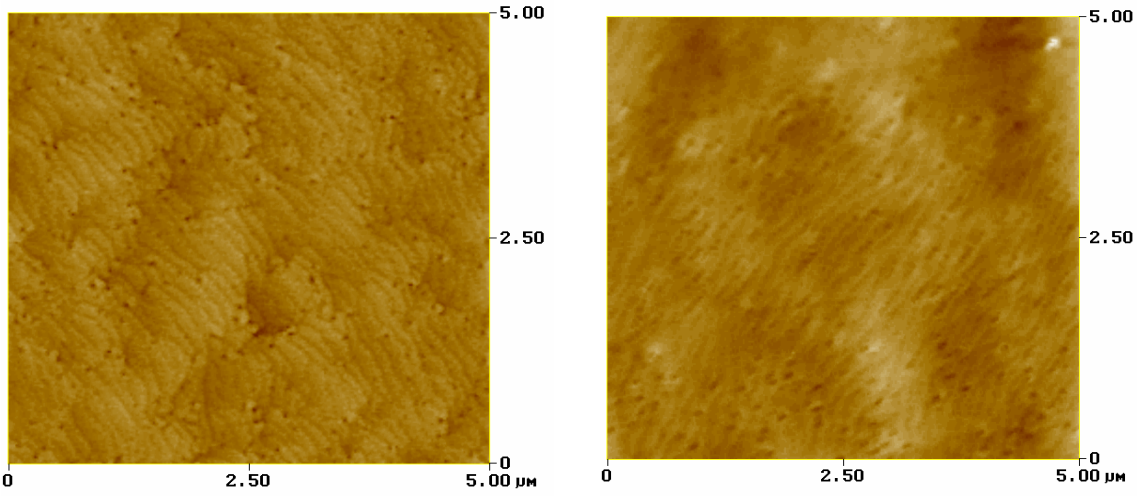


Figure 6.3: Atomic force microscopic image of (a) AlInGaN/GaN heterostructure with rms roughness of about 2-3A° and (b) AlInN/GaN heterostructures with rms roughness ~3-4 A°.

The Ga incorporation is concealed if XRD is used to determine composition. Therefore, other methods such as XPS, SIMS, or RBS were used to detect the presence of Ga. Figure 6.2 shows the SIMS profiles of the AlInGaN barrier layer along growth direction where the barrier layers were grown in bulk with a thickness of 100nm prior to the growth of the heterostructure and the SIMS analysis was done. In the AlInGaN profile, presence of Ga can be observed corresponding to the 2-3% Ga incorporation in the barrier layer where as there is no Ga signal is found for the standard AlInN/GaN heterostucture which agrees well with the XRD result.

The surface morphology for both AlInGaN and standard AlInN heterostructures is shown in Figure 6.3 using a typical atomic force microscopic image. The rms roughness across the 2" wafers was less than 3 Å. Fine surface steps were observed over the surface of AlInGaN barrier layer with the presence of Ga whereas the surface of AlInN barrier layer is not as smooth as AlInGaN barrier layer.

Table 6.1: Hall measurement data comparing the heterostructure with quaternary and the ternary barrier layers.

Design	Barrier thickness (nm)	R_{SH} (ohm/sq)	Mobility (cm^2/v-sec)	N_S (cm^{-2})
AlInGaN	6	211	1454	$2.03x10^{13}$
AlInN	6	230	1309	$1.96x10^{13}$

6.2 Enhanced dc performance of AlInGaN/GaN MOSHEMTs

Hall measurements were carried out for these heterostuctures. Table 6.1 shows the comparative Hall measurement and sheet resistance measurement data for both AlInGaN/GaN and AlInN/GaN heterostuctures. The average sheet resistance was 211Ω/sq for 6nm AlInGaN barrier and it's across wafer standard deviation was less than 4.5%. Typical sheet carrier concentrations of 2.03×10^{13} cm^{-2} which agrees with the

numerical calculation presented in this chapter. The mobility of 1454 $cm^2 V^{-1} s^{-1}$ were obtained at room-temperature for this heterostucture which is also higher than the standard AlInN heterostructure.

The impact of the polarization-induced charges on the conduction band profile can be calculated numerically. A self-consistent solution of coupled Poisson and Schrödinger equations is required to calculate the polarization induced charges. Figure 6.4 shows the result of such a simulation for an AlInGaN/GaN and AlInN/GaN heterostructure using the software BandEng [125]. This program is a one-dimensional Schrödinger-Poisson solver originally designed for the use with the Group III nitrides. As can be seen, for AlInN/GaN heterostructure, even without any intentional doping in the barrier layer, a nearly triangular quantum well is formed below the Fermi level EF, thus realizing a 2DEG at the GaN side of the heterointerface and the calculated sheet carrier concentration for this heterostructure is 1.25×10^{13} cm^{-2} which is a little lower than the measured value. But for the quaternary barrier layer of AlInGaN/GaN heterostructure, it was found that any deviation from the homogenous case will give a background polarization additional to the polarization discontinuities at the heterointerfaces. This would indeed lead to an increase of the total polarization and consequently to an increase of the 2DEG density. The calculated sheet carrier concentration is found to be 2.01×10^{13} cm^{-2}, almost twice of the standard AlInN/GaN heterostructure for 6nm of barrier layer.

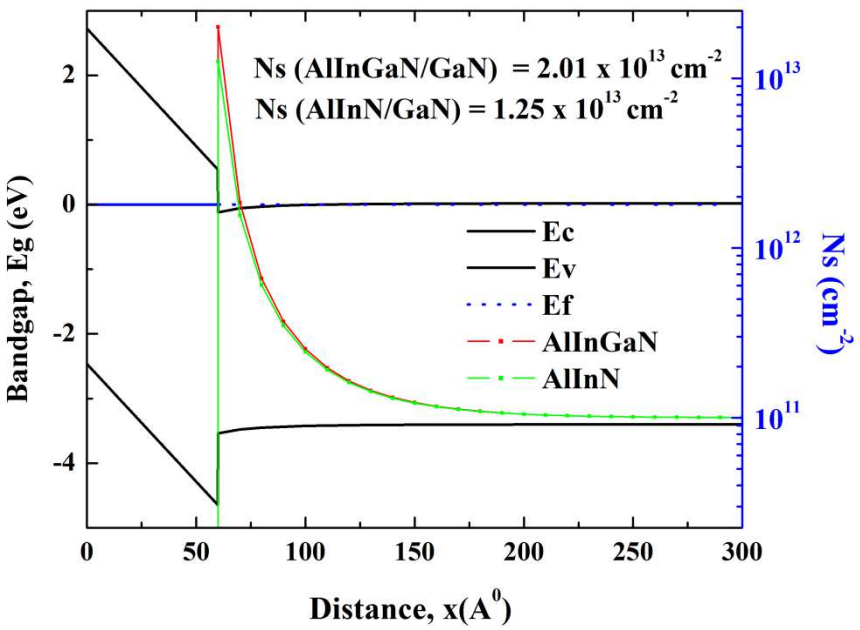


Figure 6.4: Self-consistent Poisson Schrödinger simulation of an LM-AlInN/GaN and AlInGaN/GaN heterostructure using the software BandEng [125]. The conduction band and the valence band profile as well as the sheet carrier concentration are shown.

To fabricate the MOSHEMTs, the procedure was overall similar to the one detailed in [120,121]. It encompasses inductively coupled plasma dry mesa etching for device isolation, ohmic contacts were formed using Ti/Al/Ni/Au layers and annealed in an N_2 ambient using a rapid thermal anneal (RTA) system, the average contact resistance, as measured by linear transmission line model (TLM), for the sample was 0.59 Ω·mm. Material sheet resistance measured by TLMs structures was 265 Ω/□ for the sample with AlInGaN barrier layer. Pulsed PECVD of SiO_2 under the gate was used before depositing gate metal [75,76]. The Ni/Au Schottky gates were patterned using ebeam lithography to obtain a gate length of L_G = 1.8 μm. The source-drain spacing was measured to be 8 μm whereas the source to gate separation was 1 μm. A schematic cross section and an SEM image of the resulting devices are shown in Figure 6.5. The gate width was 100 μm. For comparison, AlInN/GaN Schottky gate HEMTs were also processed from the same wafer

and to an identical geometry as the MOSHEMTs. HP 4156B semiconductor parameter analyzer was used to measure the devices dc current–voltage (*I–V*) characteristics.

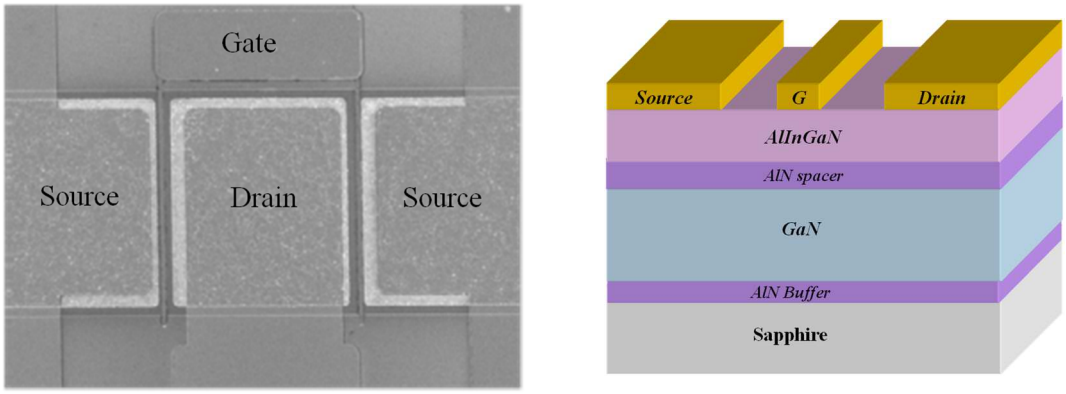


Figure 6.5: (*a*) SEM image of the processed MOSHEMT (*b*) Schematic cross section of the AlInN/GaN HEMTs on Sapphire substrate with L_{DS} = 8 μm.

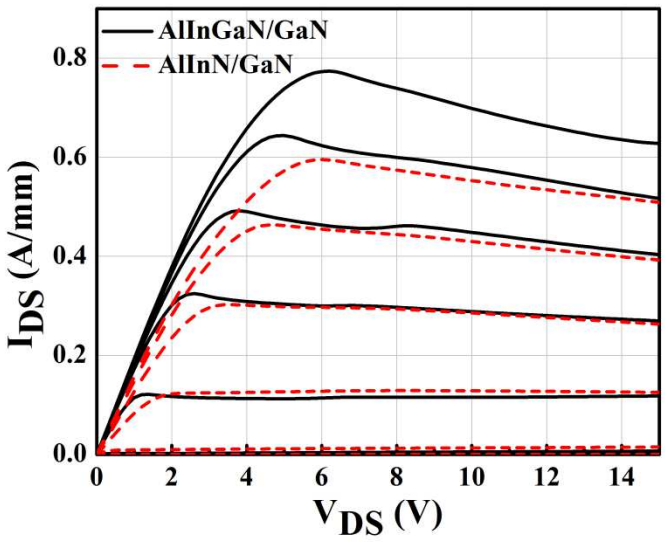


Figure 6.6: Typical static output *I–V* characteristics of a 1.8×100 μm^2 standard AlInN/GaN MOSHEMT and AlInGaN/GaN MOSHEMT for Vgsmax = +2V with -1V step size.

Figure 6.6 shows typical dc output current–voltage (*I–V*) characteristics of the AlInN/GaN MOSHEMT with 2-3% Ga measured at various gate voltages (V_{GS}) ranging

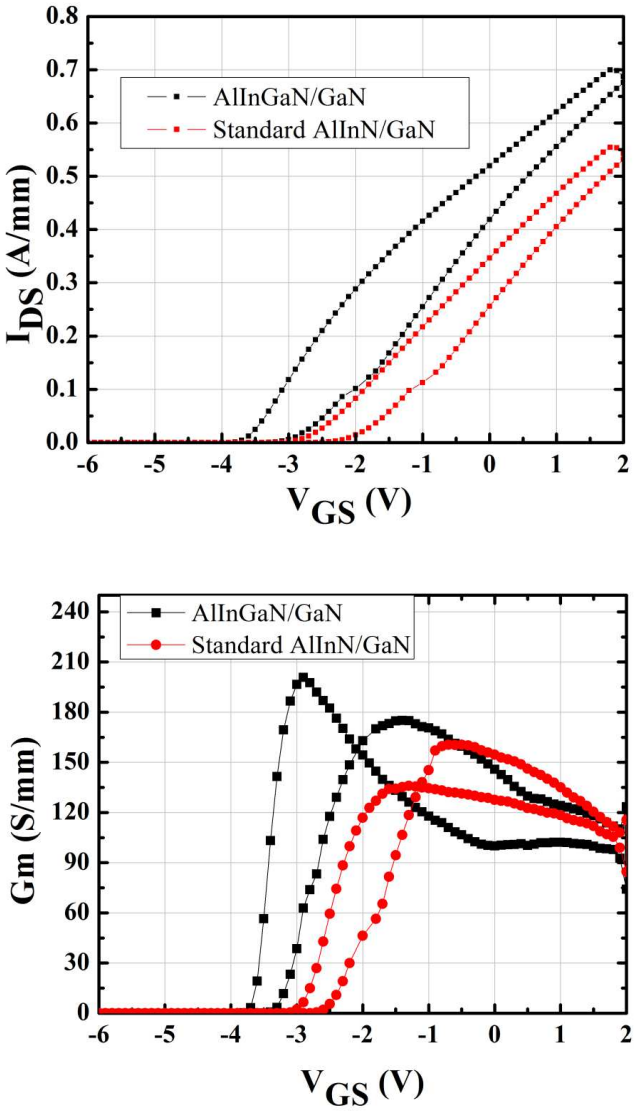


Figure 6.7: (a) Transfer curves of the AlInGaN/GaN and AlInN/GaN MOSHEMTs (top). (b) Transconductance curves for both the MOSHEMTs (bottom) derived from the transfer curves. To evaluate the devices surface and interface quality, the gate bias double sweep mode at V_{DS} = 10 V is used.

from +2V to −4V. The depletion-mode device was completely pinched off at V_{GS} = −3 V and a maximum drain current density (I_{DSmax}) of 700 mA mm^{-1} versus 540 mA mm^{-1} for the standard MOSHEMT was obtained with +2 V on the gate. Because of the increased 2DEG in the AlInGaN/GaN heterointerface, the output drain current is higher for this heterostructure than the standard AlInN/GaN MOSHEMTs.

To assess the quality of the SiO_2 layer underneath the gate, static transfer characteristics of the MOSHEMT and HEMT were measured under forward and reverse gate bias sweeps, as shown in Figure 6.7a. This double sweep measurement approach represents a quick, although not always conclusive, way to qualitatively study the current dispersion phenomenon in nitride-based transistors [122,123]. To acquire the experimental data, the drain–source voltage was held constant at 10 V, while V_{GS} was varied from −4 V up to +2 V and then reversed back to the starting value. Unlike Schottky gate devices, for which the forward and reverse *I–V* characteristics overlapped each other (negligible hysteresis), a notable shift of the threshold voltage from -3.5V to -2.8 V was observed in the AlInGaN MOSHEMT with 2-3% Ga in the barrier layer compared to the threshold voltage shift of standard AlInN MOSHEMT is from -2.6 V to -1.9 V.

The transistors extrinsic tranconductances are derived from their respective transfer characteristics (see Figure 6.7b), also revealed similar hysteresis effects. Since the surface properties between the metallic probes were the same for both types of devices, the shift in V_{th} for the insulated gate HEMT toward a more negative value points at the presence of trap states and/or oxide charge introduced by the SiO_2 layer. Here it worth adding that the maximum transconductance was about 200 mS mm^{-1} for the AlInGaN MOSHEMT and 175 mS mm^{-1} for the AlInN MOSHEMT.

Since the diode forward current plays a key role in determining the stability of the III-nitride transistors at the maximum rf powers [124], the gate diode characteristics for the two devices of interest are measured and illustrated in

Figure 6.8. It can be seen that the MOSHEMTs provided a significantly lower gate leakage current than the HEMTs (see

Figure 6.8a) for both the heterostructures. In both cases the gate-source leakage current is lower for the standard AlInN/GaN heterostructure than the quaternary AlInGaN/GaN heterostructure. For the standard AlInN/GaN heterostructure the gate leakage current is found to be limited to less than 45pA at gate bias of 4V. Although for the quaternary heterostructure, the increase in the leakage current is very sharp but is found to be less than 5nA for gate bias of 4V. The presence of Ga in the barrier layer might have introduced some defects that have increased the gate leakage currents for the quaternary AlInGaN/GaN heterostructure. The increased gate leakage has also impacted the breakdown voltages of this heterostructure. For the standard AlInN barrier layer the breakdown voltage V_{BR} is measured to be around 218V whereas for quaternary AlInGaN barrier layer, the breakdown voltage was 190V.

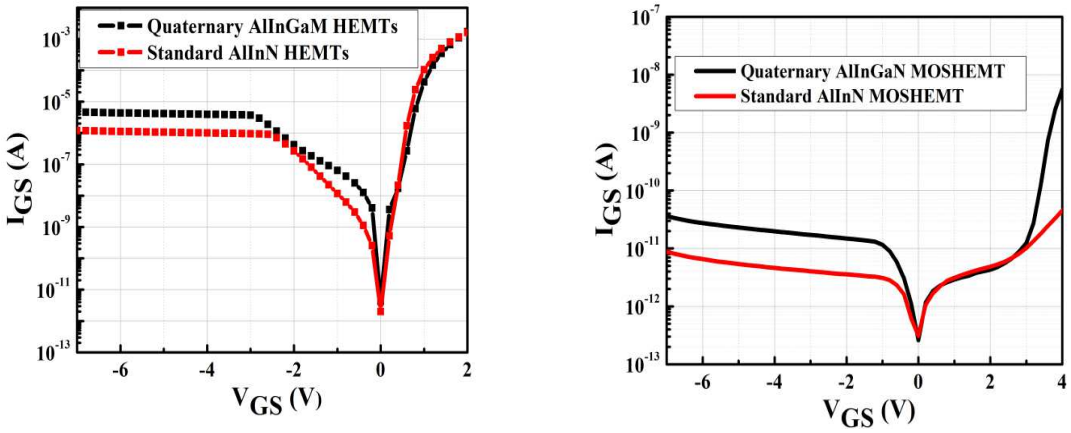


Figure 6.8: Gate leakage current of the AlInN/GaN MOSHEMT and a reference Schottky gate HEMT with 2-3% Ga and without any Ga incorporated in the barrier layer.

6.3 Conclusion

In conclusion, high electron mobility and low sheet resistance were realized in the lattice-matched AlInGaN/ GaN heterostructure. The 2DEG mobility was enhanced by introducing Ga in the lattice matched AlInN barrier layer. We investigated the dc performance of AlInGaN/GaN insulated gate high electron mobility transistor and compared the performance with standard AlInN/GaN MOSHEMT. AlInGaN MOSHEMT devices with a 1.8 μm gate length exhibited a better performance in terms of maximum saturation drain current, threshold voltage shift and sub-threshold current as compared to that of standard AlInN MOSHEMT. But in terms of gate leakage current and the breakdown voltage, the performance of the standard AlInN/GaN is better than the quaternary barrier layer. This achievement is attributed to the good crystalline quality of the epilayers associated with a good quality SiO_2 film deposited by the pulsed plasma-enhanced chemical vapor deposition technique.

CHAPTER 7

MULTI-FINGER AlInN/AlN/GaN D-MODE AND E-MODE MOSHEMTs ON SAPPHIRE SUBSTRATE

Most of the research works on AlInN/GaN HEMTs and MISHEMTs have so far focused on small periphery devices with deep sub-micrometer gate technology, targeting primarily high speed electronics applications. But there is also an interest on multi-finger structure of GaN HEMTs to increase the power density of RF amplifier MMICs (Monolithic Microwave Integrated Circuit) or for the application of high power switch. The first study of multi-gate AlInN/InN/GaN depletion mode (D-mode) and enhancement mode (E-mode) or normally off MOSHEMTs over sapphire substrate with gate widths varying from 0.15 mm to 0.9 mm will be discussed in in the first part of this chapter. Both the D-mode and E-mode devices were fabricated using a 3-4 nm thick SiO_2 dielectric film and a novel Si_3N_4-based bridging approach for source contacts interconnections. The maximum saturation output current and the maximum extrinsic transconductance appear to scale nearly linearly with the gate width, which make the corresponding MOSHFETs very promising for high-voltage, high power operation and digital ICs can be constructed combining these devices. In the second part of this chapter, the study of large periphery AlInN/GaN MOSHEMTs over sapphire substrate with gate widths varying from 0.25mm to 5mm is discussed. A high saturation output current of ~1.3A and a maximum extrinsic transconductance of 210mS are demonstrated for the 5mm wide device with a gate length of 1.8μm and a source-drain spacing of 12μm. The

maximum saturation output current and the maximum extrinsic transconductance appear to scale nearly linearly with the gate width up to 1mm beyond which joule heating dominates. These results show the potential of these MOSHFETs for high-voltage and high power operation.

7.1 Width Scaling of the of AlInN/AlN/GaN MOSHEMTs

GaN HEMTs have the potential to be used to construct ICs to perform reliable operations at high temperature that have not be possible for silicon- or GaAs-based technologies [126]. The high-temperature digital ICs can provide the enabling technology for intelligent control and sensing units used in automotive, aviation, chemical reactor, and oil exploration systems [127]. A circuit configuration similar to that based on CMOS cannot be implemented yet due to the lack of p-channel GaN HEMTs. It is challenging to fabricate E-mode AlInN/GaN HEMT with high-performance characteristics including high transconductance, low on-resistance, low knee voltage, and large input voltage swing, all of which are required for digital applications. Most of the research works on AlInN/GaN HFETs and MOSHFETs have so far focused on small periphery devices with deep submicrometer gate technology, targeting primarily high speed electronics applications. On the other hand, and to the best of our knowledge, there has been only one study of large periphery AlInN-based HFETs for power electronics applications. However, these devices with ~ 7 nm barrier layer, a 250 nm gate length and a 2.5 mm gate width (W_G) delivered a low dc drain current density of 248 mA/mm and exhibited a high leakage current of 1mA/mm under reverse bias [133].

In this section, we investigated for the first time the DC performance of large periphery InAlN/GaN MOSHEMTs over sapphire substrate. The devices were fabricated

using a 3-4 nm SiO_2 gate dielectric and a unique Si_3N_4 bridging dielectric layer for source interconnections. To ensure both a precise film thickness control and improved film quality and device viability, the SiO_2 layer was deposited using the pulsed PECVD technique [75]. Like in our previous study on large periphery insulated gate AlGaN/GaN HFETs [134], the AlInN/GaN MOSHFETs were found to exhibit a nearly linear dependence of both dc and pulsed saturation output currents on the total device gate width, which was varied from 150 μm to 900 μm. The same behavior was also observed for the maximum static extrinsic transconductance along with a very little change in the gate-source current-voltage characteristics.

The heterostructure studied here was grown by low-pressure MOCVD on a 2-in diameter sapphire substrate. It consists of 1.8 μm thick unintentionally-doped GaN buffer layer, 1 nm-thick AlN spacer layer and ~ 6 nm thick InAlN barrier with a nominal Al content of 83 %. The thin AlN interlayer is introduced to reduce alloy disorder scattering and thus improve the transistors transport properties [135]. Room temperature Hall effect measurements yielded a two-dimensional electron gas (2DEG) sheet charge density of 2.4 x 10^{13} cm^{-2} and Hall mobility of 1036 cm^2/V.s. The wafer sheet resistance was ~248 Ω/ .

The device geometry consisted of an interlaced source-gate-drain electrode design. The gate electrode exhibits a multi-finger pattern and the source-to-source connections go over the drain electrodes with a SiN layer in between for metals isolation.

Figure 7.1 shows a CCD image of the largest MOSHFET device with a six-finger gate. Device fabrication process began with mesa isolation, which was achieved in an

inductively coupled plasma (ICP) etching reactor using a BCl_3/Cl_2 gas mixture. Ti(15nm)/Al(70nm)/Ti(30nm)/Au(50nm) metal stacks were then evaporated and alloyed at 850 °C for 30 sec in nitrogen gas ambient to form the source and drain ohmic contacts. Prior to the gate fabrication, a 30-40 Å of silicon-oxide dielectric material was deposited at 300ºC using PECVD technique [76]. Ni (70nm)/Au (70nm) gate electrodes were next deposited in between the source–drain contacts. Each single gate electrode (1 finger) measured 1.8 µm in length and 150 µm in width. After the contact pads formation, we again used PECVD and RIE dry etching processes to realize 250 nm-thick SiN isolation "islands" at the drain-source intersections for the MOSHFETs with more than 2 finger-gates. Ti/Au metal electrodes were finally deposited to form two low resistance source section interconnections. All devices were not passivated.

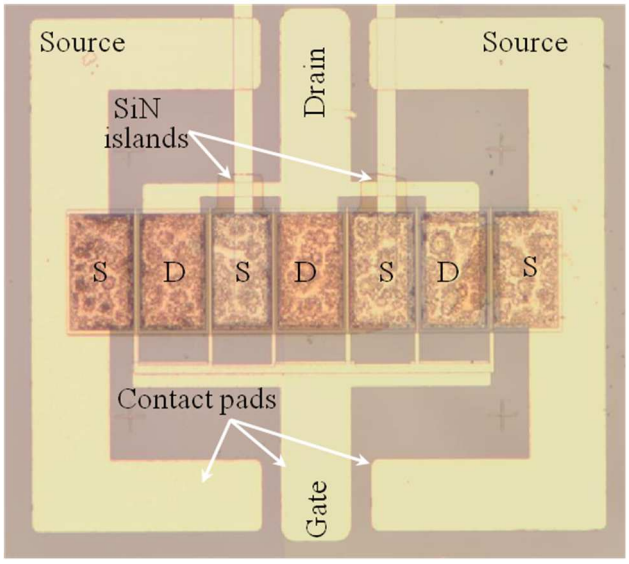


Figure 7.1: Microscopic image of the large periphery AlInN/GaN MOSHFET (six-finger gate pattern) fabricated using SiN bridges for source electrodes interconnections.

7.2 Multi-Finger AlInN/GaN D-mode MOSHEMTs

The dc characteristics of the depletion-mode (D-mode) AlInN/GaN MOSHFETs were measured with an Agilent 4155B semiconductor parameter analyzer. Figure 7.2(a) shows typical output characteristics of 1x(1.8x150) μm^2 and 6x(1.8x150) μm^2 D-mode devices. Maximum drain currents (I_{DSmax}) of 102 mA and 420 mA were obtained at V_{GS}=+2 V and V_{DS}=+7 V for the small and large periphery MOSHFETs, respectively.

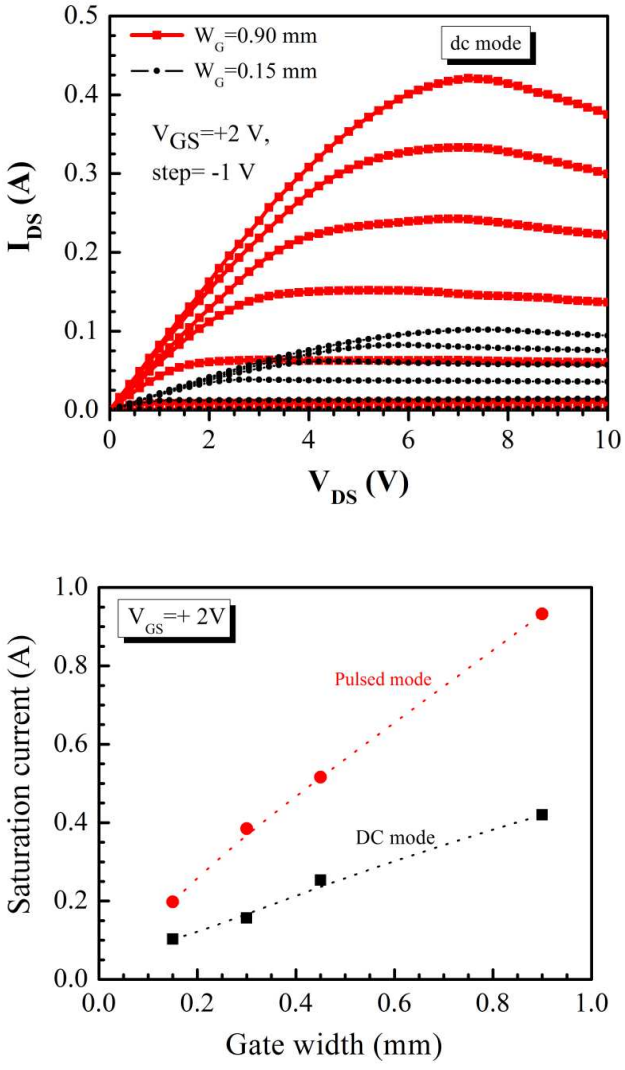


Figure 7.2: (a) Typical dc output characteristics of 0.15 mm and 0.90 mm AlInN/GaN D-mode MOSHFETs (top), and (b) gate width-dependence of the maximum dc and pulsed saturation drain current measured at V_{GS}=+ 2V (bottom).

Note that the devices were completely pinched-off below -4 V gate bias. While the self-heating effects seem to be negligible for the 0.15mm device up to +2 V gate bias and V_{DS}=10 V, the 0.90 mm devices exhibited drain currents drop with increasing the drain-source voltage beyond ~7 V and for a gate-source bias greater than 0 V.

The dc and pulsed current-voltage (I-V) curves (pulsed signal width=0.2 μs) for different multi-gate (MG) D-mode devices were then compared. The dependence of the saturation drain current on the total gate width for our AlInN/GaN D-mode MOSHFETs at V_{GS} = + 2 V is shown in Figure 7.2(b). As can be seen from the plot, the pulsed data show an almost linear behavior, which suggests a possible scaling of the MOSHFETs I-V characteristics. The maximum pulsed current value of 930 mA was attained for the 0.9 mm device. In contrast, the dc peak current values were limited to about 420 mA as they appear to follow a smaller slope with increasing the device periphery beyond 0.50 mm. This behavior is most likely due to self-heating effects, which are further exacerbated by sapphire substrate with its low thermal conductivity.

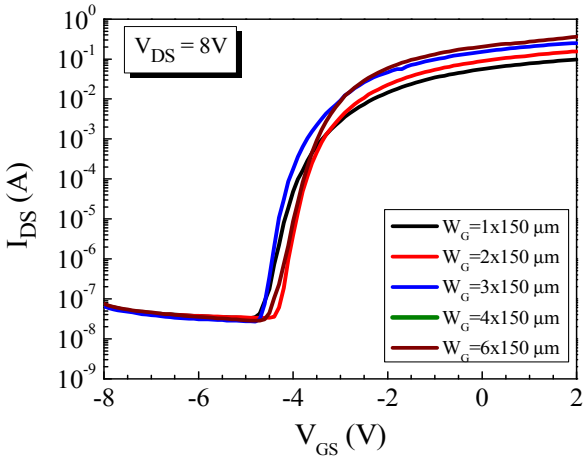


Figure 7.3: DC Transfer characteristics for AlInN/GaN MOSHFETs with different gate peripheries.

Theoretically the output current should linearly increases with the gate width which agrees with the experimental data shown in Figure 7.2(b) but the output current is different for DC and pulsed mode operation. The maximum drain current in pulsed mode operation is twice the output current of the devices while operating in DC mode because of the device self-heating. At high output power densities, device self heating is the main limiting factor for stable operation of the device. This problem will be discussed more in the next chapter.

Figure 7.3 illustrates typical transfer characteristics measured at V_{DS}=8 V for all devices studied here. The sub-threshold current levels were almost identical for all MOSHFETs, reaching ~70 nA at V_{GS}= -8 V versus ~30 nA at V_{GS}=-5 V. There were no significant changes in the on-off ratios as well with increasing the gate width given that the maximum dc output currents varied only by a factor of ~3.5. The threshold voltage of the different periphery devices was next extracted from the slope of the $I_{DS}^{0.5}$-V_{GS} curves. A small change in V_{Th}, by ~0.24 V, was observed when the gate periphery was varied in the range 0.15-0.90 mm. For the largest device, the threshold voltage was -3.68 V while V_{Th}=-3.86 V was measured or the 0.15 mm MOSHFET.

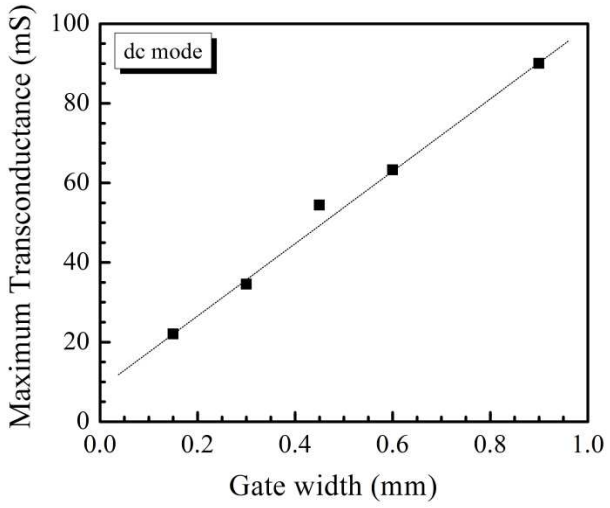


Figure 7.4: Variation of the maximum transconductance of AlInN MOSHEMTs as a function of gate width measured in the saturation regime.

The variation of the maximum extrinsic transconductance (g_{mM}) as a function of the gate width is depicted in Figure 7.4. The data were derived from the transfer characteristics measured in dc mode (see Figure 7.3). Like with the other dc parameters, the results indicate an almost linear scaling with gate width up to the largest value of 0.90 mm. For this latter gate width, g_{mM} was about 90 mS (or 100 mS/mm) whereas it was 22 mS for W_G=0.15 mm.

7.3 Multi-Finger AlInN/GaN Enhancement mode MOSHEMTs

After successfully demonstrating the D-mode large periphery AlInN/GaN MOSHEMTs, the target was to achieve E-mode MOSHEMTs with a threshold voltage of more than 1.5V with high current density. The most popular way to achieve normally off AlInN/GaN HFET is to selectively and precisely etch the AlInN barrier layer under the gate of the device to remove the 2DEG (discussed in the previous chapter). Since the barrier thickness is very thin (~ 6nm-8nm), it is very crucial to etch the AlInN barrier

layer up to a certain thickness to achieve the desired threshold voltage. It was difficult to control the etching depth which gives different threshold voltages and if the barrier layer is etched too deep into the buffer layer then the current density would be very low. To achieve the required etching depth we used the reactive ion etching (RIE) process after the ICP etching process. After the standard ICP mesa isolation and ohmic metallization and annealing was done, a couple of combination of both the ICP and RIE dry etching processes was done to precisely etch the barrier layers under the gate. Below are some optimized etching processes that are used to achieve the desired threshold voltage Vth for the E-mode AlInN/GaN MOSHEMTs.

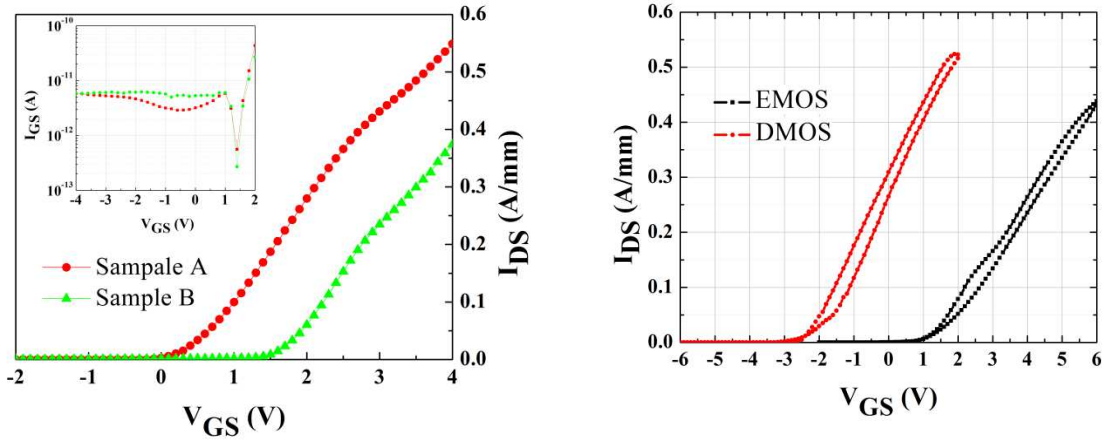


Figure 7.5: (a) Sample B shows a higher threshold voltage of 1.5 V than sample A due to thinner barrier thickness under the gate (left), 15nm of SiN gate dielectric shows similar gate leakage current for both the sample (inset). (b) Comparative threshold voltage for D-mode and E-mode MOSHEMTs fabricated from the same wafer (right).

In Figure 7.5, the DC transfer characteristics are shown where two separate etching processes were used on two pieces of the same wafer. The threshold voltage, V_{th} = 0.4 V was measured for sample A whereas for sample B, the threshold voltage is 1.5V with reduced current density. The gate length is 1.8um and the gate width for these samples is 100um. We also have to optimize the thickness of the gate dielectric. From our

previous experiment, we have observed that the optimum thickness of the SiON gate dielectric is about 13nm. For the above processing steps all the devices showed almost the same gate leakage currents (see inset of Figure 7.5(a)) which is about 0.4nA at gate voltages of 2V. In Figure 7.5(b), the shift of the threshold voltage is shown in the transfer curve where the DMOS and EMOS devices are fabricated from the same wafer. EMOS device shows the threshold voltage of ~1.5V with 0.45A/mm of maximum current density and minimum hysteresis.

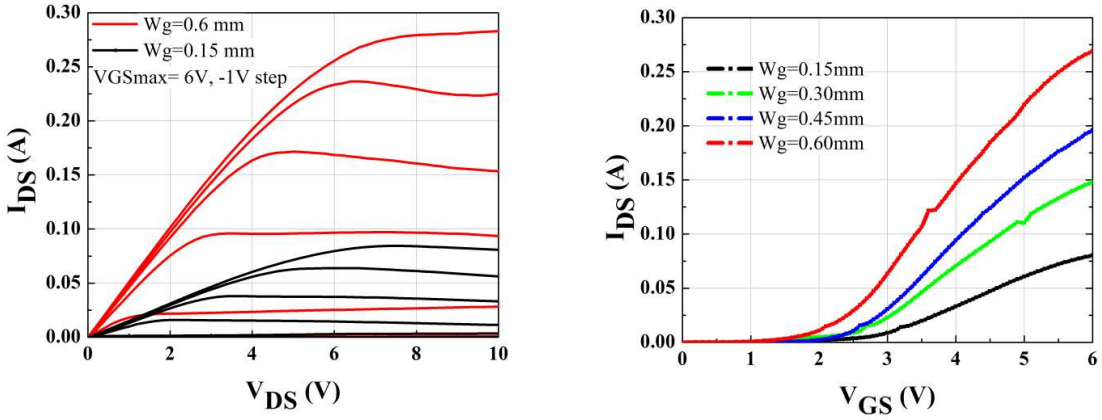


Figure 7.6: (a) The drain-source current for EMOS multifinger for gate width of 0.6mm and 0.15mm (b) The transfer curves shows that the current increases almost linearly with increasing gate width.

Multifinger E-mode MOSHEMTs were fabricated using the optimized etching process that was achieved after several trail of E-mode MOSHEMTs fabrication. The fabrication step are similar to the fabrication process of the D-mode multifinger devices except there is one addition steps of barrier layer etching under the gate before the gate metal deposition.

The family of curve is shown in Figure 7.6(a) for gate width of 0.6mm and 0.15mm where the maximum saturation current at Vgs= 6V are 280 mA and 90 mA respectively. In Figure 7.6(b), the transfer curve of the multifinger EMOS device was

shown where all the gates with different gate width have almost the same threshold voltage. The threshold voltages for all the gate fingers were not exactly same. There is a small deviation (~0.3V) of threshold voltage for mulifinger devices were measured. It is very difficult to precisely etch the same thickness under the gate to achieve the same threshold voltages for all the gate fingers. The maximum current and the transconductance increases as the gate width of the devices increase as expected but the gate leakage currents (not shown here) for different gate width was found not be increased with the increasing gate width. Further investigation is necessary to find out the reason behind it.

This experiment was the first attempt to fabricate and characterize the large periphery device. However, the varied range was only from 0.15 to 0.9 mm. To fully explore the potential of these large periphery devices, a complete new set of device with gate width up to 5mm is designed. Characterization of large periphery devices and the technological limitations are discussed in the next chapter.

In this chapter, for the first time a large periphery lattice-matched AlInN/GaN D-mode and E-mode MOSHFET on sapphire fabricated using a multi-finger gate pattern and SiN-based air-bridging approach for source contacts interconnections is demonstrated. High drain currents of 420 mA and 930 mA were measured for a 6x(1.8x150 μm^2) gate D-mode MOSHFET in dc and pulsed mode, respectively, while maintaining a very low gate leakage of less than 42 nA at -10 V gate bias. High drain current 0f 280mA was measured for E-mode multi-finger device for the gate width of 0.6mm with a threshold voltages of about 1.5V. These results show an excellent potential

of MG insulated gate AlInN/GaN HFETs for high power electronics applications involving switches, inverters and converters.

7.4 Large Periphery AlInN/AlN/GaN MOSHFETs

In this section, the study of multi-gate AlInN/InN/GaN metal-oxide semiconductor field-effect transistors over sapphire substrate with gate widths varying from 0.25mm to 5mm is discussed. A high saturation output current of ~1.3A and a maximum extrinsic transconductance of 210mS are demonstrated for the 5mm wide device with a gate length of 1.8μm and a source-drain spacing of 12μm. The maximum saturation output current and the maximum extrinsic transconductance appear to scale nearly linearly with the gate width up to 1mm beyond which joule heating dominates. Device self-heating issue has been addressed in this section. To improve the device performance by reducing the device self-heating has also been discussed. These results show the potential of these MOSHFETs for high-voltage and high power operation.

Semiconductor power converters are key building blocks for various applications which run the spectrum of powers from a few watts to mega-watts. To date majority of the applications use power converters that are based on silicon. For the very high power applications several groups are now exploring GaN based converters as an alternative to silicon especially when higher operation temperatures are needed. Our group reported the low to the moderate power converter applications by using AlGaN/GaN metal-oxide semiconductor field - effect transistors (MOSHFET) based power switch [136]. Since then rapid progress has been made and several groups including ours have reported on kilovolt switching using AlGaN based HEMTs with Schottky gates [137]. In this chapter, the performance of depletion mode, multifinger-gate AlInN/GaN metal-oxide-

semiconductor HFETs (MOSHFETs) over sapphire substrate as a building block for power switching applications has been reported for the first time. Unlike in our previous study on large periphery insulated gate AlGaN/GaN HFETs on SiC [141], the AlInN/GaN MOSHFETs grown on sapphire were found to exhibit a nearly linear dependence of both dc and pulsed peak output currents on the total device gate width up to W_G = 1 mm only, before they saturate. The same behavior was also observed for the maximum static extrinsic transconductance (g_m) along with a limited change in the gate-source current-voltage characteristics.

The device with gate widths ranging from 0.25 mm to 5 mm have been fabricated and studied for their characteristics. Several innovations were implemented to realize these devices. First, a complete new set of mask has been designed (see

Figure 7.7) with device size varying from 50um gate width to 5mm gate width. The source-drain ohmic-contacts were separated by a distance of 12 μm. Each gate electrode was 1.8 μm long and 250 μm wide. The mask also contains TLM structure, C-V measurement structure and some test structures that are useful in different fabrication steps.

The large periphery device geometry consists of an interlaced source-gate drain electrode structure using SiN dielectric bridge. More description will be found in the fabrication steps. Next, Novel pulsed atomic layer epitaxy technique was used to grow a high quality AlInN barrier layer with a thickness of about 4.5 nm and the digital oxide deposition (DoD) technique [77] to deposit an ultra-thin silicon dioxide layer as the gate dielectric has been utilized. Moreover, the same DoD technique was also used to deposit silicon nitride dielectric material needed for surface passivation as well as the realization

of metal bridging electrodes for source pads interconnections. This technique enabled us to prevent damages to the thin barrier structures, thus providing an excellent method to block the gate leakage currents.

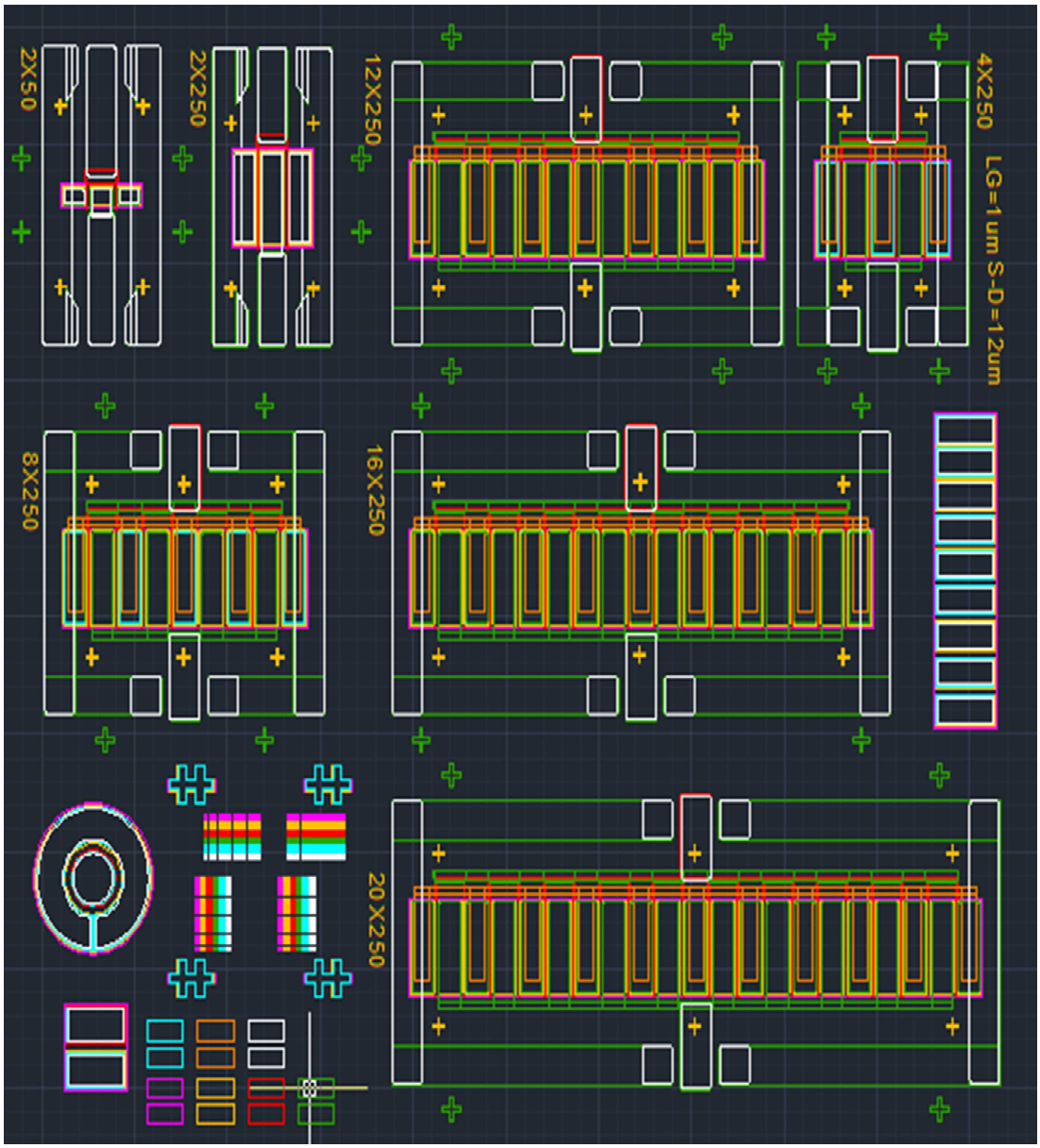
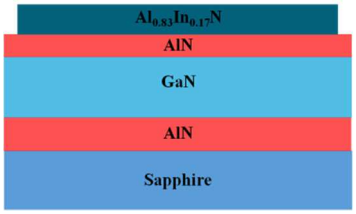
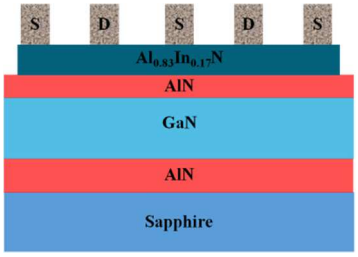


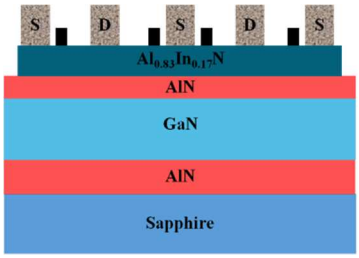
Figure 7.7: New set of mask that contains different sizes of devices with gate width of 50um to 5mm.



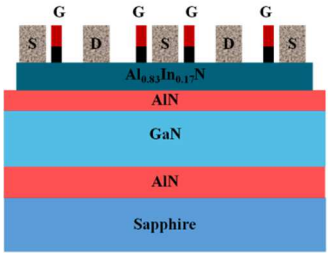
1. Mesa Isolation



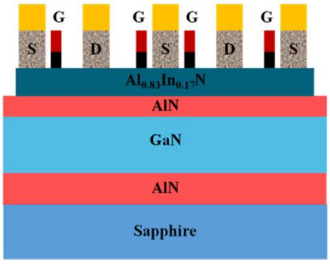
2. Ohmic Contact formation



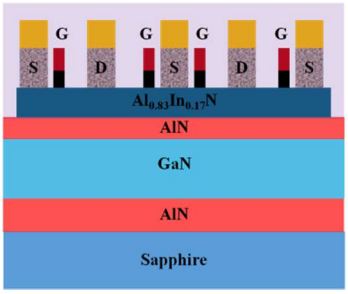
3. Gate oxide deposition



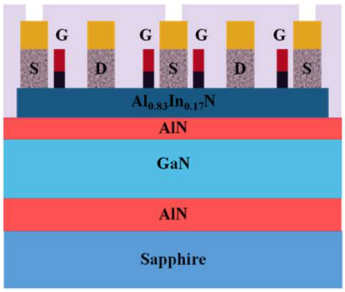
4. Gate metal deposition



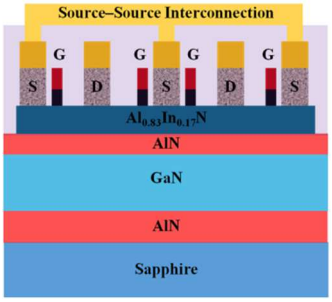
5. Probe Contact



6. Dielectric Layer Deposition



7. Opening of Source Contact



8. Source Contact Interconnection

Figure 7.8: Schematic of the different steps of fabrication for the large periphery devices.

The epilayer heterostructure studied here was grown by low-pressure metal organic chemical vapor deposition (MOCVD) on a 2-in diameter sapphire substrate. It consists of 1.8 μm thick unintentionally-doped GaN buffer layer, 1 nm-thick AlN spacer layer and ~ 5 nm thick AlInN barrier with a nominal Al content of 83 %. The thin AlN interlayer is introduced to reduce alloy disorder scattering and thus improve the transistors transport properties [135]. Room temperature Hall effect measurements yielded a two-dimensional electron gas (2DEG) sheet charge density of 1.86 x 10^{13} cm^{-2} and Hall mobility of 1569 cm^2/V.s. The wafer sheet resistance was ~228 Ω/ .

The dc characteristics of the depletion-mode (D-mode) AlInN/GaN MOSHFETs were measured with an Agilent 4155B semiconductor parameter analyzer. Figure 7.10 shows typical output characteristics for 1x(1.8x250) μm^2 and 8x(1.8x250) μm^2 devices. Maximum drain currents (I_{DSMax}) of 116 mA and 483 mA were obtained at V_{GS}=+2 V and V_{DS}=+7 V for the small and large periphery MOSHFETs, respectively.

Note that the devices were completely pinched-off below -4 V gate bias. While the self-heating effects seem to be negligible for the 0.25 mm device up to +2 V gate bias (V_{GS}) and V_{DS}=10 V, the 2 mm devices exhibited drain currents drop with increasing the drain-source voltage beyond ~7 V and for VGS greater than -1 V.

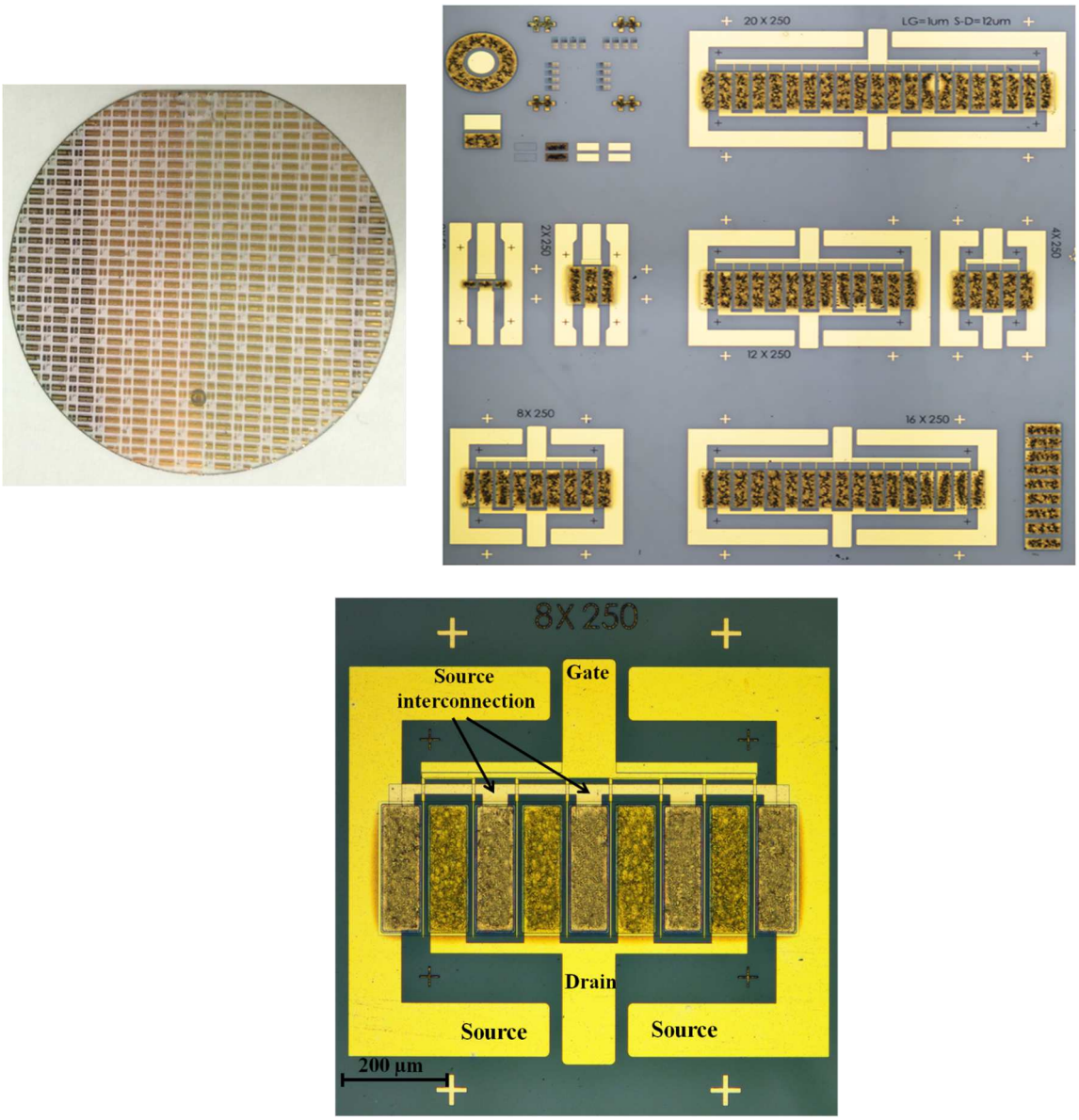


Figure 7.9: CCD image of fabricated (a) Large periphery devices in a 2inch wafer that repeats (b) the one block of the devices containing all the devices with gate width of 50um to 5mm and (c) a 2mm gate width AlInN/GaN MOSHFET (eight-finger gate pattern) fabricated using SiN bridges for source electrodes interconnections.

With increasing gate width the devices suffer severe self heating problem because of the larger power dissipation (P_{diss}). The P_{diss} of the MOS-HFET/HFET can be expressed as [142]

$$P_{diss} = I_{DS}V_{DS} + I_{G}V_{GS}.$$

The corresponding effective temperature, Teff of the device can be described by [143]

$$Teff = R_{TH}(I_{DS}V_{DS} + I_G V_{GS}) + T_{Sub}$$

where R_{TH} is the thermal resistance and T_{sub} is the temperature of the substrate. Higher Teff are expected in larger devices since larger devices suffer from severe self-heating due to much higher $I_{DS\ max}$ than smaller device. Kuball et al. [144] has showed a liner relationship of power dissipation vs maximum temperature rise where it was reported that channel temperature is about 180° C for 0.65W of power dissipation of AlGaN/GaN HFETs on sapphire whereas for AlGaN/GaN HFETs on SiC the temperature was about 120° C for 1.75W of power dissipation. In our case the dissipated power for 2mm device is 4.4W (I_{DS} = 440mA at V_{DS} = 10V) which increases the channel temperature significantly. The lattice-scattering-limited conductivity due to the thermal vibrations of the atoms limits the electron conduction in the metal and the enhanced carrier-carrier scattering phenomenon due to the elevated temperature degraded $I_{DS,max}$. Furthermore, the increased temperature decreases the mobility, μ [145], which directly affects the I_{DS}.

We then compared the dc and pulsed (pulse width = 0.2 μs, 1 ms pulse separation) current-voltage (I-V) curves for different multi-gate (MG) devices. The dependence of the saturation drain current on the total gate width for our AlInN/GaN MOSHFETs at V_{GS} = + 0 V is shown in Figure 7.11. As can be seen from the plot, the results reveals nearly a linear scaling of I_{DSsat} versus W_G up to ~1 mm gate width before Joule heating effects start impacting the devices behavior with further increasing the gate size. The maximum dc and pulsed drain output currents appear to saturate at ~0.57 A and 1.30 A, respectively, for $W_G \geq 4$ mm. The maximum drain current did not scale up as expected due to the joule heating, resulting lower current density. This behavior is due to self-

heating effects, which are further exacerbated by sapphire substrate with its low thermal conductivity.

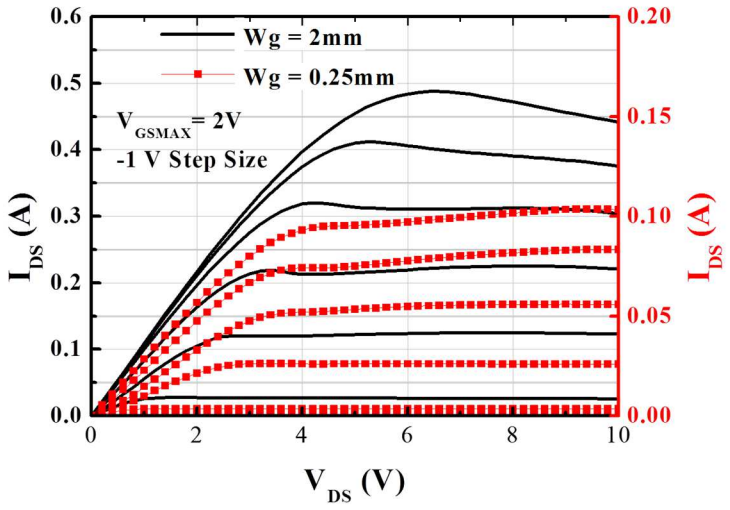


Figure 7.10: Typical dc output characteristics of 0.25 mm and 2 mm AlInN/GaN MOSHFETs.

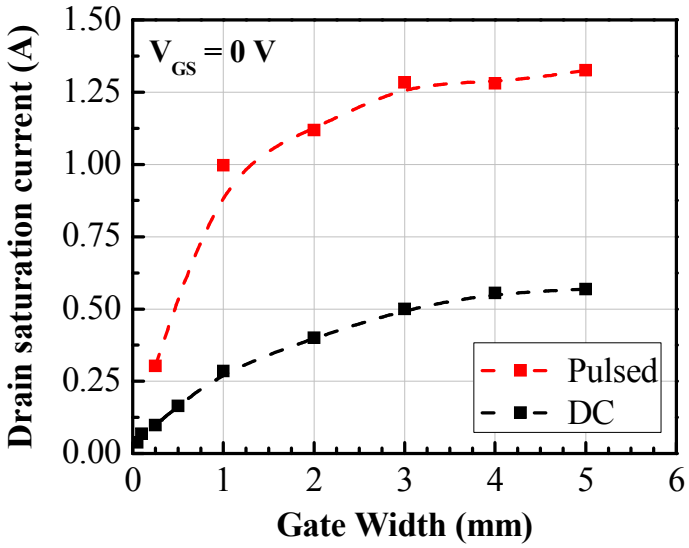


Figure 7.11: Gate width-dependence of the maximum dc and pulsed saturation drain current measured at V_{GS}= 0V.

Study using micro-Raman scattering technique for temperature distribution of self-heating in multi-finger AlGaN/GaN HFETs [146] revealed the fact that the heat is more concentrated in the center of the device and the temperature decreases sharply at

location away from the central channel region. The reason for the higher temperature in the central area of the multi-finger device is the thermal crosstalk. Increasing the channel to channel spacing reduces the thermal crosstalk thus decrease the temperature. It is also found that the junction temperature increases with increasing gate width. Therefore, to mitigate the self-heating effects, it is suggested that reducing the width of a single finger is more effective than reducing the finger numbers for devices with the same total gate width. This self-heating problem can be resolved by optimizing the design of the device since the finger width, number of fingers and the spacing is critical factors for thermal management and by the use of SiC substrates [139] as well.

Figure 7.12 illustrates typical dc transfer characteristics measured at V_{DS}=8 V for MG MOSHFETs with varying gate widths and HFET with W_G = 0.25mm. There is very small threshold voltage shift of less than ~0.4 V between MOSHFET and HFET of the same W_G= 0.25 mm. The threshold voltage of the different periphery devices was next extracted from the slope of the $I_{DS}^{0.5}$-V_{GS} curves.

A small change in the threshold voltage (V_{Th}), by ~0.12 V, was observed when the gate periphery was varied in the range 0.25-5 mm. For the largest device, the threshold voltage was -3.76 V while V_{Th}= -3.69 V was measured for the 0.25 mm MOSHFET. The sub-threshold current levels increases with the increasing gate width for all MOSHFETs but still are below the sub-threshold current of HFET with 0.25 mm gate width. Since the Vth depends on the 2DEG carrier density [147], the increased n_{2DEG} due to the passivation effect might be the reason why the larger devices have slightly more negative Vth and increasing sub-threshold currents.

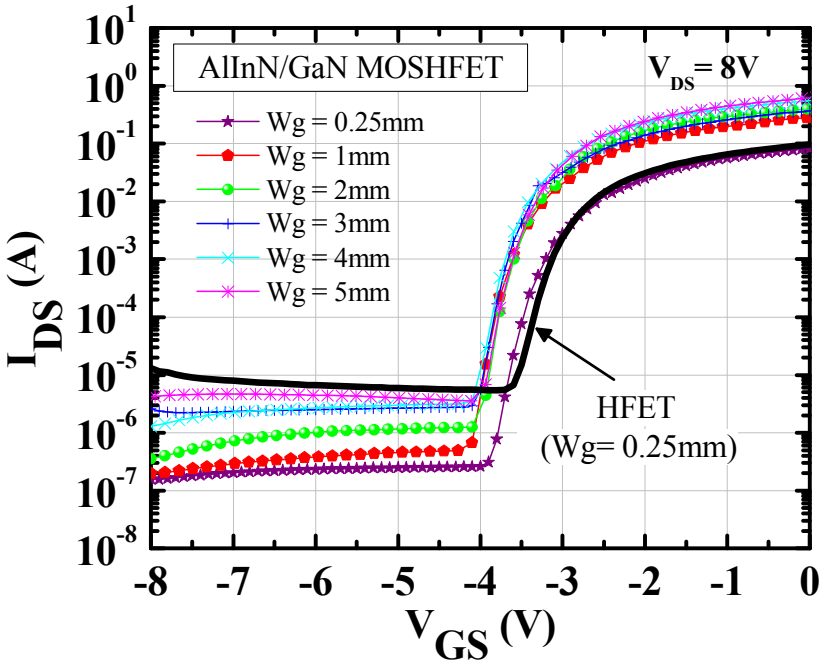


Figure 7.12: DC transfer characteristics for AlInN/GaN MOSHFETs with different gate peripheries. The result obtained for 0.25mm HFET is also shown for comparison.

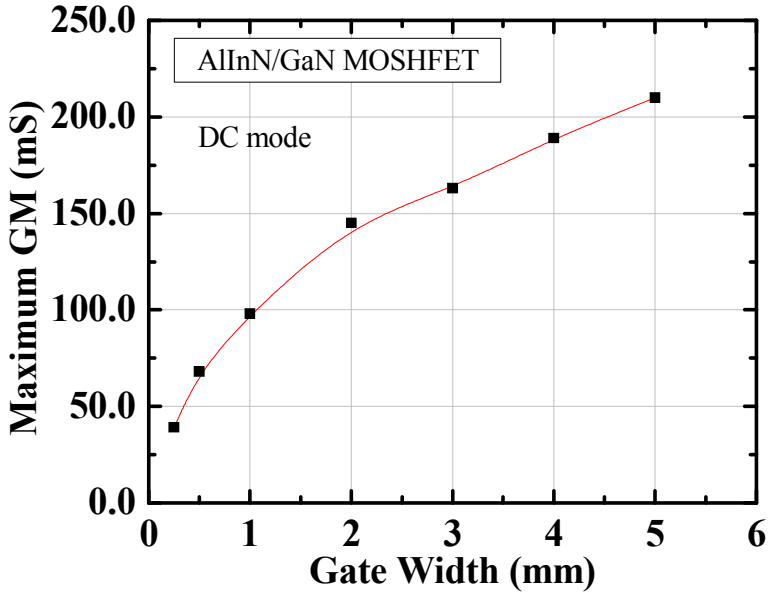


Figure 7.13: Variation of the maximum dc transconductance of AlInN/GaN MOSHEMTs as a function of gate width measured in the saturation regime at V_{DS}= 8 V.

The variation of the maximum extrinsic transconductance (g_{mMax}) as a function of the gate width is depicted in Figure 7.13. The data were derived from the transfer

characteristics measured in dc mode (see Figure 7.12). Like with the other dc parameters, the results indicate an almost linear scaling with gate width up to 1 mm. For 5mm gate width, g_{mMax} was about 210 mS whereas it was 39 mS for gate width for W_G=0.25 mm. The reason of MG large periphery devices have lower g_{mMax} might be the enhanced phonon scattering due to increased channel temperature [148].

In Figure 7.14 we investigated the insulated gate characteristics for the MG devices. All curves seem to exhibit similar profiles with increasing the gate width. Also, despite the thin oxide layer the current levels were suppressed to below the ~20 μA under both reverse and forward biases. The thermionic emission (TE) and thermionic field emission (TFE) are the dominant conduction mechanisms for the forward bias [149] and for the reverse bias, there are many possible conduction mechanisms such as trap-assisted tunneling (TAT), Poole–Frenkel (PF) emission, and TFE [150]. Since the MOS-gate structure provides barrier height and thickness to suppress carrier transportation in the forms of TE and TFE, it is reasonable for MOSHFETs to have lower gate leakage at forward bias.

More importantly, the gate leakage current seem to show a very weak dependence on the device periphery as it is found to vary between 0.5 μA and 5.7 μA at V_{GS}=-10 V and in the range 3-19 μA under +2 V gate bias for gate width of 1-5mm, still below the gate leakage current of 7 μA at -10V and 3mA at 2V gate bias for the HFET with 0.25mm gate width. This is due to the thin SiO_2 gate dielectric layer. It is worth mentioning here that the subthreshold slope (SS) of MG MOSHFETs has not degraded (in Figure 7.12). J. W. Chung et al. [151] observed that the SS is related to the gate

leakage. The larger gate leakage makes SS worse. Due to the gate leakage suppression, large peripheries MOSHFETs SS have not degraded.

It was previously shown that the gate leakage current per unit area in AlGaN/GaN HFETs [77] and AlInN/GaN MOSHFETs [138] remains the same when either the gate width or gate length is varied, respectively. This was not the case for the devices studied in the present work. IGS was found to substantially increase when WG was increased from 250µm to 1mm, then no clear dependency with further increasing the gate width was observed. What is causing this behavior is still not well understood at this moment, but material and/or process non uniformity might be a factor. It is also known that the leakage current can originate from i) the parasitic leakage of the mesa regions or in the region where the gate feed runs over the mesa wall or ii) the presence of the SiN passivation layer which degrades the gate diode characteristics by introducing surface leakage current in the SiN layer or at its interface.

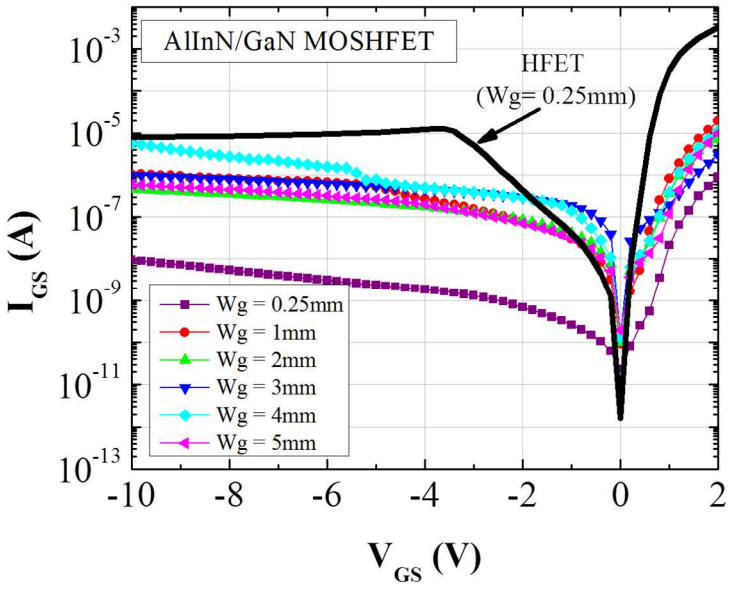


Figure 7.14: DC measurements of the gate leakage currents for the 0.25mm HFET and MOSHFETs with up to twenty-finger gates showing a weak dependence of I_{GS} on the device periphery.

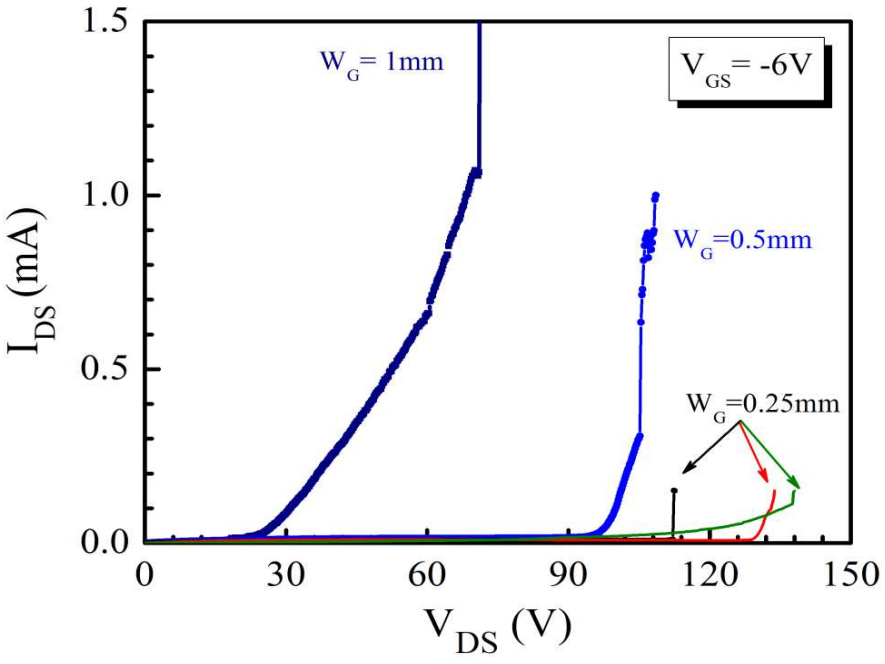


Figure 7.15: Three terminal breakdown voltage measurements for different devices.

The three terminal off-state breakdown voltages were measured for several MOSHFET devices (see Figure 7.15) using the 1mA/mm criteria. The gate-source bias applied was -6 V, which was about 2 V lower than the threshold voltage and no fluorinert solution, which usually prevents surface flashover and prevents to a premature device breakdown, was used. The breakdown voltage was found to be 110-137 V for the 0.25 mm devices and dropped down to 70 V for the large periphery MOSHFET with W_G ~1 mm. Note that the surface passivation drastically increases the peak electric field at the drain side of the gate which can cause the local Schottky-barrier breakdown at the lower drain bias.

It is well known that the use of SiN passivation suppresses the rf dispersion for AlGaN/GaN HFETs by removing the surface states which relives the channel depletion as well [152]. Therefore, with less surface states on the access region the higher ns–μ

product is obtained to exhibit the higher $I_{DS,max}$ and g_{mMax}. However it also results in increase in gate-leakage currents. More investigation about the quality of gate dielectric and the effect and methods of reducing such leakage currents along with the study of the interface traps and defects are currently underway.

In this chapter, we demonstrate for the first time a large periphery lattice-matched AlInN/GaN MOSHFET on sapphire fabricated using i) a very thin SiO_2 layer as the dielectric material for gate insulation, ii) a multi-finger gate pattern and iii) SiN-based air-bridging approach for source contacts interconnections. High drain currents of 0.57 A and 1.3 A were measured for a 20x(1.8x250 μm^2) gate MOSHFET in dc and pulsed mode, respectively. To the best of our knowledge, these data represent the highest output currents delivered by a single AlInN/GaN MOSHFET on sapphire substrate, while maintaining a very low gate leakage of less than 6 μA at -10 V gate bias. The threshold voltage and extrinsic transconductance for the largest device (W_G=5 mm) were -3.69 V and 210 mS, respectively. Furthermore, our experimental data also reveal a nearly linear scaling of the devices dc characteristics with gate width up to 1 mm before self-heating effects occurs while a weak increase in the leakage current was observed for all MOSHFETs. These results show an excellent potential of MG insulated gate AlInN/GaN HFETs for high power electronics applications involving switches, inverters and converters.

CHAPTER 8

FUTURE DIRECTIONS

An evaluation of two approaches for heat dissipation (bottom and top heat dissipation) is proposed together with the challenges presented and the technological steps to realize it. The heart of this work is the design and development of a processing and packaging technology for high performance LP AlInN/GaN MOSHEMTs. This chapter will focus on developing a new process flow for the flip-chip of LP AlInN/GaN MOSHEMTs and propose a new device fabrication and packaging processes for better thermal management of the device.

8.1 Thermal Management of LP AlInN/GaN MOSHEMTs

In the previous chapter, it was shown that the DC output current is lower than the drain current measured in pulsed mode. Theoretically the output current should linearly increase with the gate width but the output current is different for DC and pulsed mode operation. The maximum drain current in pulsed mode operation is twice the output current of the devices while operating in DC mode because of the device self-heating. At high output power densities, device self-heating is the main limiting factor for stable operation of the device. Especially when the heat sources are located close to one another, the temperature rise due to thermal crosstalk between the sources may be much greater than the heat source alone. With high power and small chip size, the thermal effect will degrade the reliability and efficiency of GaN device. To maintain good

switching characteristics in operation, the junction temperature should be limited within a permissible range.

Measurements and simulations have shown that self heating causes a reduction in mobility and drift velocities because of phonon scattering effect affecting both the output current and the operation frequency [153, 154, 155]. Temperature-induced gate leakage deteriorates the device's RF performance also limits high-temperature applications. Moreover, the increased device temperature affects the reliability of the device through accelerated aging and accelerated electromigration of the device metallization leading to device failure [156, 157]. Thus efficient heat dissipation and management is a key to enable reliable and efficient GaN HEMT power operation.

With increasing the device output power, the dissipated power eventually increases leading to an increase in the device temperature. It was shown that the high currents of the device can lead to very high device temperatures. It was reported that temperatures above 200 °C were reached in AlGaN/GaN HEMTs with dissipated power of 4 W/mm [156] and a channel temperature up to 700 °C was estimated, using lateral resolved microphotoluminescence, in AlInN/GaN HEMTs with drain bias of only 20 V due to the high current levels (around 2 A/mm) [157]. In Figure 8.1, simulated results of a device maximum temperature during high power operation and the heat dissipation effect of the substrate with an attached heat sink on the bottom is shown. Sapphire, SiC substrates were used for bottom heat spreading, and the device maximum temperature is greatly influenced by the type of substrate since it is the major heat path component connected to the package heat sink thus SiC is the most efficient in terms of thermal management due to its superior thermal conductivity. But despite its very high thermal

conductivity (340 W/mK at R.T.) the device temperature can still reach high values. For example the device temperature will reach 100 °C at a power loss of approximately 3 W/mm using SiC and will reach 100 °C at 1.5 W/mm when using Sapphire (the most commonly used substrate in this work). The bottle neck for heat extraction from the bottom is the GaN buffer (ranging from 1 μm to 3 μm in thickness) and its thermal interface resistance with the substrate.

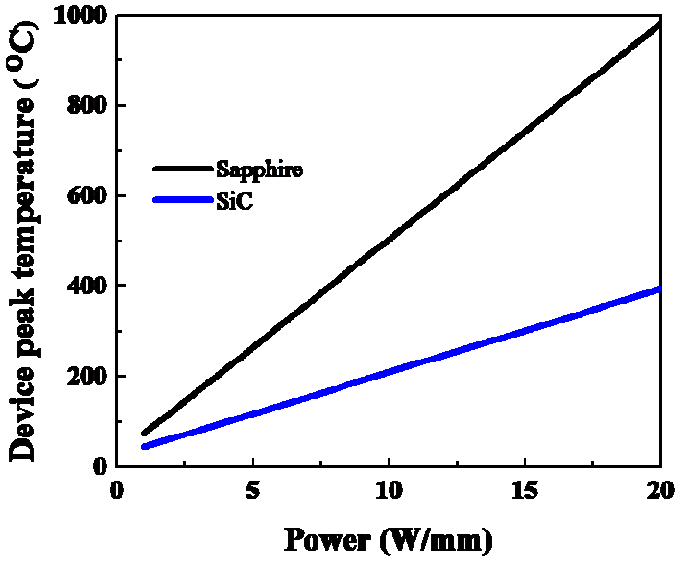
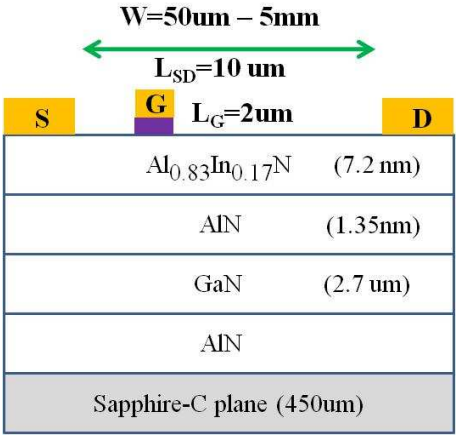


Figure 8.1: HEMT maximum channel temperature as a function of power loss for different heat dissipation configurations [158]. For bottom heat sink, the device temperature depends on the substrate type.

8.2 Proposed Technique

In the case of self-heating the substrate type determines the efficiency of heat extraction from the bottom of the device, but heat can also be extracted from the top of the device if the device is coated with a highly thermally conductive material. The later approach puts the heat sink in close proximity to the channel, providing a shorter thermal path for the heat to dissipate. Thus there are two possible combinations for heat management.

1. The first approach would be using SiC, Sapphire, Si as substrates, with an attached heat sink for bottom heat extraction.
2. The second approach would be combining the same set of substrates with a high thermally conductive epoxy on top as heat spreader and with attaching the heat sink to the top layer, instead of attaching it to the substrate, thus extracting the heat from the top of the device.



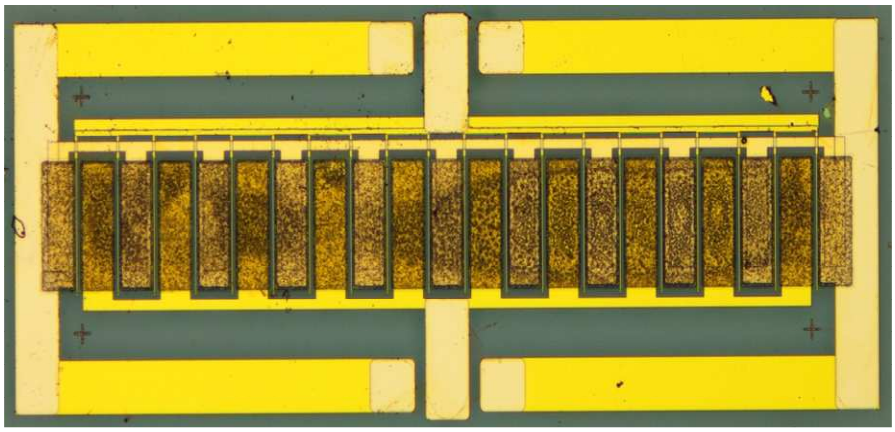


Figure 8.2: (a) Schematic of AlInN/GaN heterostructure that is fabricated for LP devices (top) and (b) Optical microscopic image of a passivated large periphery device (bottom) with a gate width of 5mm (20x250um).

8.3 Preliminary Results of Thermal Management

To study the thermal effect on device performance, a new set of large periphery devices is fabricated on sapphire substrate using the same fabrication steps mention in the

previous chapter. Figure 8.2a shows the schematic of the heterostructure that has been fabricated with gate width ranging from 50um to 5mm. A passivated 5mm device that has 20 gate fingers and each gate finger has a gate length of 2um with a gate width of 250um has been shown in Figure 8.2b. The TLM measurement showed that the sheet resistance for this heterostructure is 346Ω/sq.

It is difficult to extract the heat from the bottom of the large periphery devices that are fabricated on sapphire substrate since sapphire is a poor thermal conductive material. Therefore, to compare the difference in device performance due to thermal effect, the sapphire substrate has been thinned down by mechanical grinding and then the devices were measured in DC and pulse mode. Before grinding the sapphire substrate was measured to be 450um thick and after grinding the thickness of the sapphire was 200um.

Comparative DC and pulsed measurements of a 1mm device in Figure 8.3 shows that the output drain current increases with a thinner sapphire substrate in both cases. Although the device still suffers from device self-heating in DC mode operation. In addition, the Vknee walkout in pulsed mode (see Figure 8.3b) is due to the surface passivation issue. These passivation layers can only partially mitigate trapping-related current dispersion effects. It was shown that a further reduction of this dispersion can be achieved by implementing a field-plated gate structure which was taken into consideration but improved the Vknee very slightly (not shown here). This means that for the next generation of lithography, the surface passivation needs to be optimized.

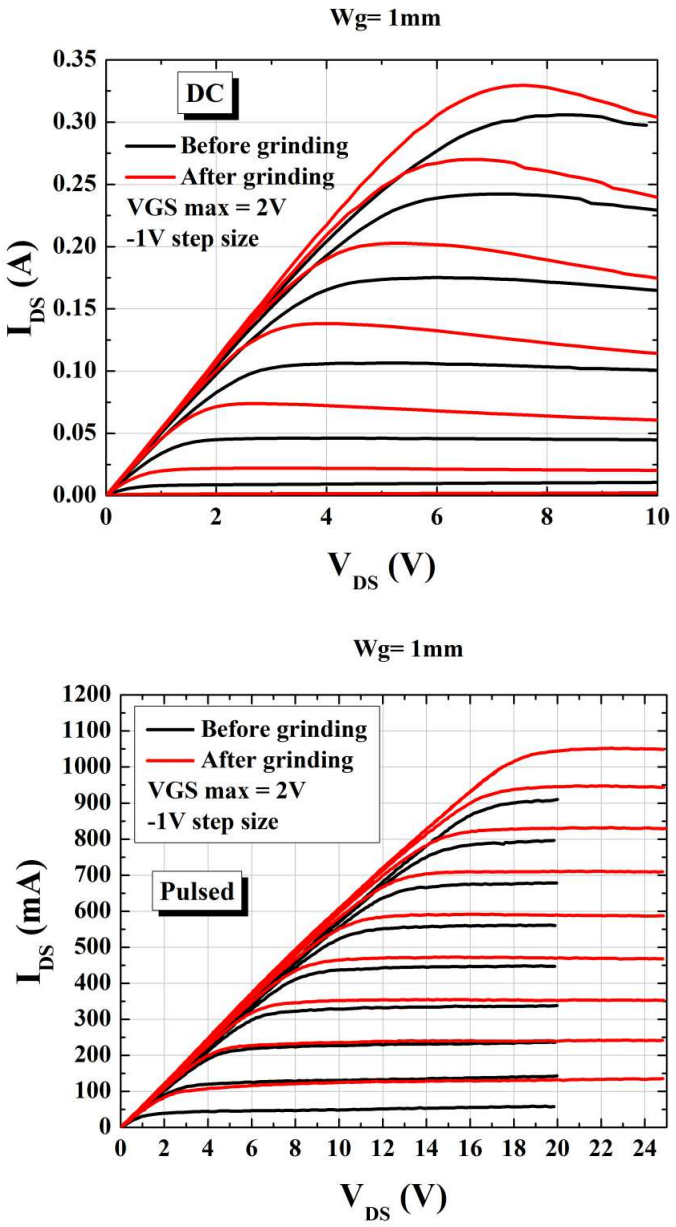


Figure 8.3: Typical I-V characteristics of 1mm device comparing the drain current before and after the sapphire substrate was thinned down to 200um in (a) DC mode (top) and (b) Pulsed mode (bottom).

Comparative DC and pulse measurements for the large periphery devices (see Figure 8.4) ranging from 0.25mm to 5mm gate width also showed that with thinner substrate, the output current is higher because the device can be cooled down easily with thinner substrate. Unfortunately, the reason for maximum drain current saturation at

pulse mode at larger gate width is still unknown as of now and needs to be explored further.

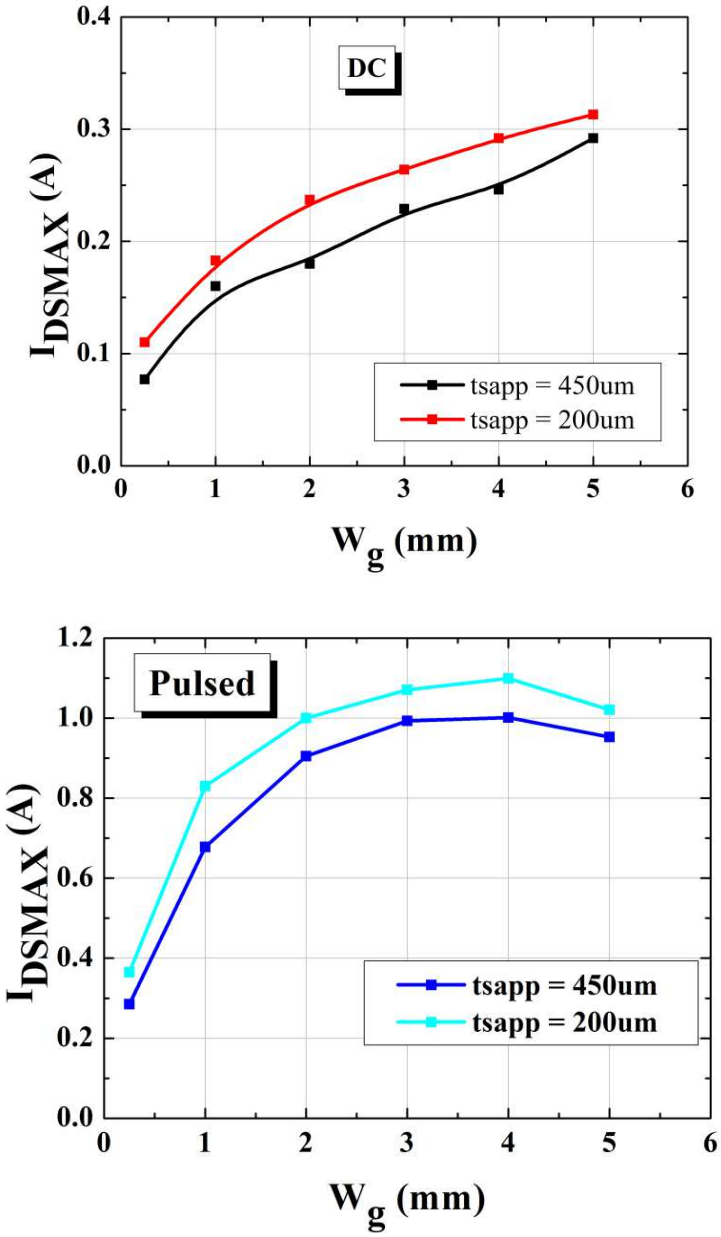


Figure 8.4: Comparative maximum output drain current I_{dsmax} versus gate width for the same devices with a sapphire substrate thickness of 450um and after thinning down to 200um in (a) DC mode and (b) Pulsed mode at gate bias, Vg = 0V shows increased drain currents in both measurements due to better thermal managements.

8.4 Future Work

To appreciate the difference between the heat dissipation methods and the temperature distribution in the HEMT for the different configurations is shown in Figure 8.5. Where thermal simulations are performed using Finite Element Method (FEM) software (COMSOL) with a 2D model to evaluate the efficiency of both approaches (bottom and top heat spreading), and to estimate the maximum HEMT temperature as a function of the power loss in the device.

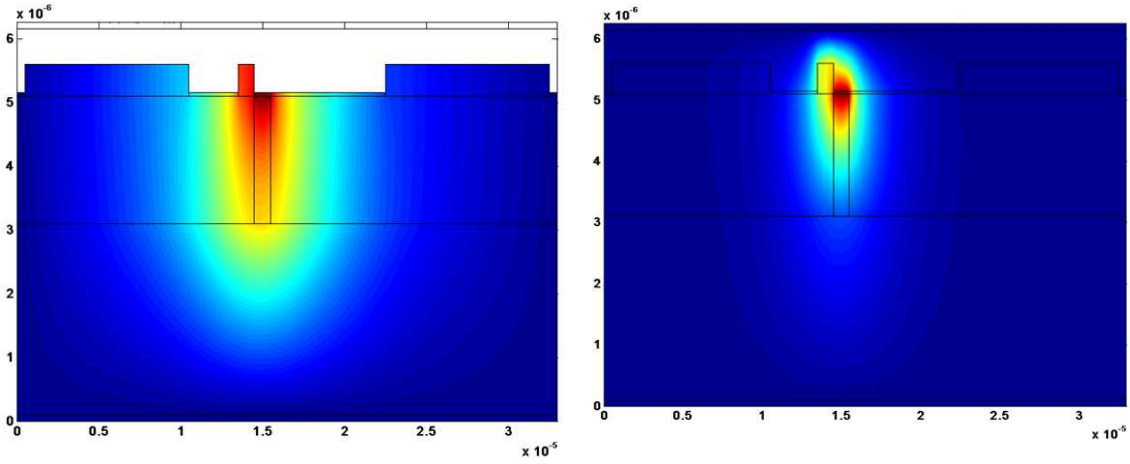


Figure 8.5: Temperature distribution in the simulated HEMT structure on sapphire substrate using different heat spreading configurations at a power loss of 20 W/mm (a) with heat spreader and heat sink on bottom (b) with top heat spreader with an attached heat sink.

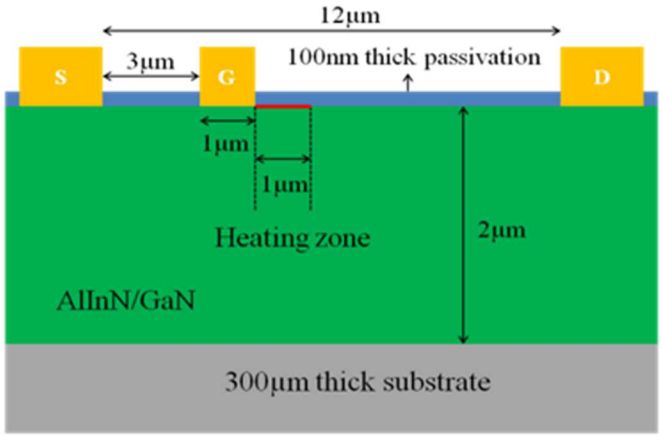


Figure 8.6: GaN HEMT device geometry used in the 2D FEM simulation.

In Figure 8.5a, it is shown that the device maximum temperature is still very high during high power operation though there is a heat sink attached to the sapphire substrate where as Figure 8.5b shows the effect of adding a 1 μm thick thermally conductive epoxy layer as a heat spreader with a heat sink on top. The heat spreader on top of the device distributes the heat across the surface of the device, which is then removed by the top heat sink.

Table 8.1: Material parameters used in the thermal simulations.

Material	Thickness (μm)	κ (W/mK)
GaN	2	130
Cu metallization	0.2	340
Si3N4 passivation	0.1	15
Sapphire	300	40
epoxy	1	12
SiC	300	340

The simulated structure is based on the building blocks of a HEMT as shown in Figure 8.6, with GaN buffer thickness of 2 μm, 6 nm thick AlInN barriers, Cu as metallization for ohmics and gate, and 100 nm Si3N4 as passivation. The source-gate distance is 3 μm and the gate-drain distance is 8 μm. The simulator assumes a 1 μm width of the device for purposes of unit normalization. The thermal properties of the used materials used in this simulation are listed in Table 8.1. The 6 nm InAlN barrier is ignored since it does not significantly influence the heat spreading compared to the buffer or the passivation. The device self heating is simulated by introducing a 1-dimensional heating zone, representing the hot spot region in the channel between gate and drain (1

μm long) adjacent to the gate metal contact stripe, as was demonstrated also for AlGaN/GaN HEMTs [160, 161]. This is done by introducing an inward heat flux (in units of W/m^2) across the heating zone area shown in Figure 8.6. The heat flux is calculated by dividing an assumed RF power loss, ranging between 1 and 20 W/mm, by the heat zone area. Thus, the simulations do not calculate the device self heating as a function of the output power but rather introduces a pre-calculated amount of power loss, which is expected to be generated during device operation.

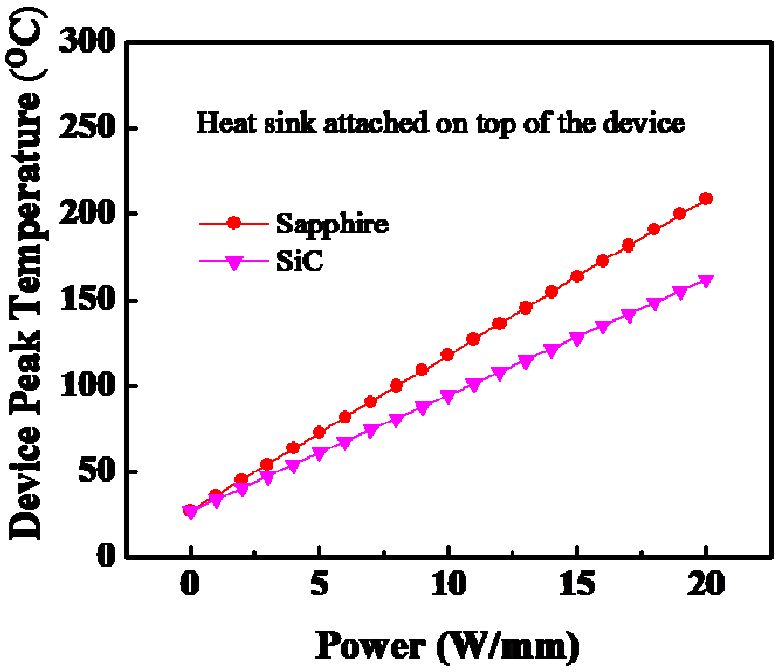


Figure 8.7: HEMT maximum channel temperature as a function of power loss for different substrate with a 1 μm thick thermally conductive epoxy as heat spreader with an attached heat sink on top, the device temperature is significantly.

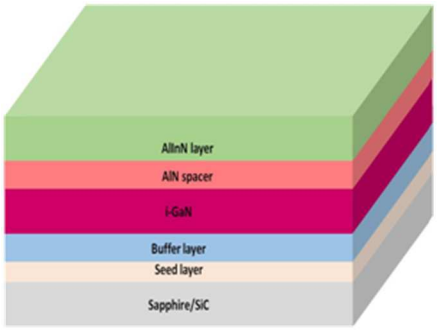
Figure 8.7 shows the simulated result of the maximum device temperature for different power dissipation with a top heat sink for both SiC and sapphire substrate where a reduction in the maximum temperature of the device is achieved by adding a thermally conductive epoxy heat spreader and a heat sink on top. Heat dissipation is simulated

using the aforementioned configurations of a heat spreader on bottom or on top. At the bottom (when the simulated heat sink is placed at the substrate side), or at the top (when the simulated heat sink is placed above the top heat spreading layer) an isothermal boundary condition is assumed with T=25 °C (i.e. the heat sink is considered an ideal heat sink at a constant temperature of 25 °C obtained by forced cooling). The simulator will calculate the peak channel temperature in the HEMT as a function of the power loss (dissipated heat flux) for each different substrate.

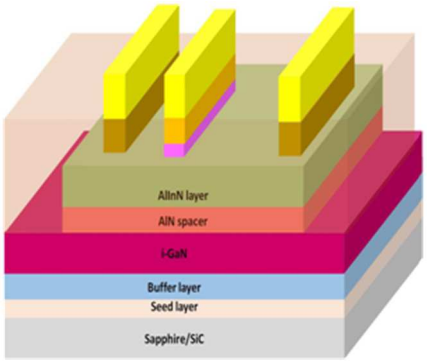
8.4.1 Flip-chip Technology

Extracting heat from the top is similar to a flip-chip configuration. In this configuration the device temperature is only marginally influenced by the GaN buffer. The key factor for efficient heat extraction in the later configuration is the close proximity of the heat source to the ideal heat sink. Thus, using heat spreader on top of the HEMT structure with an attached ideal heat sink presents the most efficient method of heat dissipation.

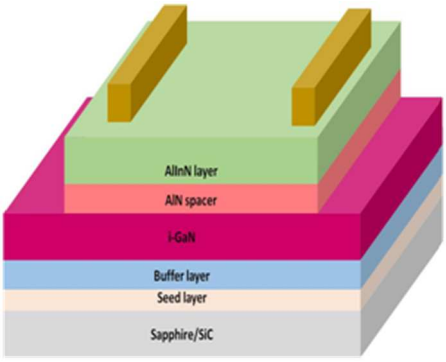
Adding heat sink and the heat spreader on top of the device is however not straight forward. To be able to flip-chip the device and add the heat spreader requires additional device processing steps. The single gate device fabrication and the packaging steps are shown in Figure 8.8. Device fabrication process will starts with mesa isolation, which is achieved in an inductively coupled plasma (ICP) etching reactor using a



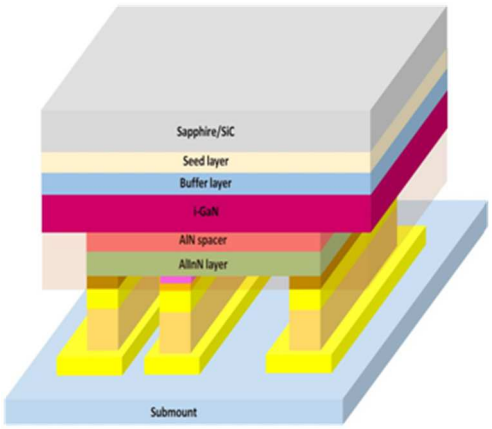
1. Device Epilayers



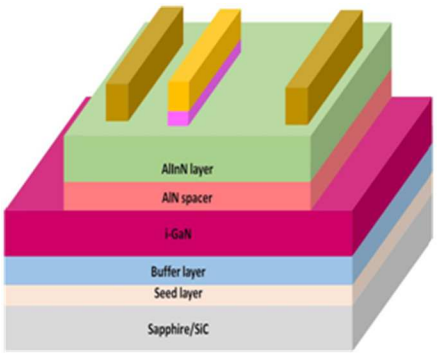
4. Probe Contact metallization & Si3N4 Passivation



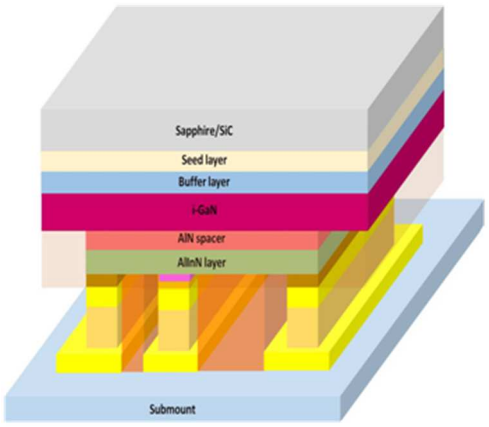
2. Mesa Isolation & ohmic Contact



5. Flip-chip on submount



3. Gate Oxide and Metallization



6. Epoxy

Figure 8.8: Step by step fabrication and packaging process to achieve thermally stable AlInN/GaN MOSHEMT for better performances.

BCl_3/Cl_2 gas mixture. Ti(150Å)/Al(700Å)/Ti(300Å)/Au(500Å) metal stacks will then be evaporated and alloyed at 850 °C for 30 sec in nitrogen gas ambient to form the source

and drain ohmic contacts. Next, Ni (70nm)/Au (70nm) gate electrodes will be deposited between the source–drain contacts, with (for MOSHEMTs) and without (for HEMTs) SiO_2 gate dielectric. The 30-40 Å of silicon-oxide dielectric material will be deposited using pulsed plasma enhanced chemical vapor deposition (PECVD) technique. After the contact pads formation, we will again use pulsed PECVD processes to realize 100 nm thick SiN passivation layer. Next, the device will be flip-chipped on AlN submount and then the thermal epoxy will be introduced and cured in-between the gap of the device and the submount to distribute and extract the heat from the top of the device.

8.5 Conclusion

Since the device design and packaging plays an important role in the thermal management of the device, the new device fabrication and packaging processes need to be well designed and developed for this heat extraction process. Thus future works to improve the device performance include the following key tasks:

- Developing a mask set to package large periphery (LP) AlInN/GaN MOSHEMTs.
- Packaging of the of the LP devices after fabrication.
- A detailed study of DC and pulsed Characterization of the device before and after the flip-chip to compare the device performance to establish whether the approach works.
- Determining problem areas to be used as the focus for the follow up work.

The effectiveness of a SiN passivation layer for AlInN/GaN material systems needs to be studied in detail. In the case of AlGaN as a barrier layer, it was demonstrated that PECVD SiN layer could alleviate surface-related trapping effects. Unfortunately, that was not the case for AlInN-based HEMTs. Additionally, it was speculated that similar

bandgaps of PECVD SiN and AlInN/GaN influence passivation properties via charge transfer from the barrier into the passivation layer. Thus a sophisticated process step in order to provide a charge neutral-interface with the AlInN has to be developed.

In conclusion, after all processing and packaging steps are completed; device characterization of the LP AlInN/GaN MOSHEMTs needs to be carried out to evaluate their performance. DC and pulsed current-voltage (I-V) characteristics of devices with bottom heat sink and after the device flip-chip will provide information about whether the device performances have been improved or not. Furthermore, the devices reliability and thermal management data needs to be presented and discussed to prove that heat extraction from the top of the device is the most efficient way of thermal management of the device especially during high power operation.

REFERENCES

[1] C. Raynaud et al. Diamond and Related Materials, 19(1):1–6, 2010.

[2] C. Buttay et al. Materials Science and Engineering B, 2010.

[3] B. J. Baliga, IEEE Electron Device Lett. 10, 455 (1989).

[4] K. Takahashi et al. Wide bandgap semiconductors: fundamental properties and modern photonic and electronic devices (Springer Verlag, 2007).

[5] R. Waser, Nanoelectronics and information technology : advanced electronic materials and novel devices (Wiley-VCH, Weinheim, 2005).

[6] C. Kocabas et al. Proceedings of the National Academy of Sciences 105, 1405 (2008).

[7] D. A. Frickey et al. Microwave Theory and Technique, IEEE Transaction on 42, 205 (1994).

[8] G. Meinke, Taschenbuch der Hochfrequenztechnik, (1987).

[9] B. Kumar et al. Electronic devices and circuits (PHI Learning Pvt. Ltd.,2007)

[10] M. Asif Khan et al. Appl. Phys. Lett. 63 (1993), 1214–1215.

[11] W. Nagy et al. IEEE Transactions on, 51(2):660 – 664, Feb. 2003.

[12] F. Medjdoub et al. IEEE Electron Device Letters, 29(5):422–425, 2008.

[13] J. Kuzmik et al. IEEE Transactions on Electron Devices, 55(3):937–941, 2008.

[14] Daniel Morgan et al 2011 Appl. Phys. Express 4 114101

[15] Sylvain L. Delage et al. MIKON, 2010, pages 1 –5, June 2010.

[16] J.H. Leach et al. Proceedings of the IEEE, 98(7):1127 –1139, July 2010.

[17] G. Meneghesso et al. IEEE Trans. on Dev. and Materials Reliability, 8(2):332–343, 2008.

[18] F. Medjdoub et al. 2007 (ISDRS 2007), pages 1 –2, dec. 2007.

[19] F. Medjdoub et al. Electronics Letters, 42(13):779–780, 2006.

[20] F. Medjdoub et al. International Electron Devices Meeting, IEDM, pages 927–930, 2006.

[21] C. Gaquiere et al. The Open Electrical & Electronic Engineering Journal, 2:1–7, 2008.

[22] F. Bernardini, et al. Phys. Rev. B, vol. 56, no. 16, p. R10024, Oct.1997.

[23] C. Miskys A et al. J. Phys.: Condens. Matter, 14:3399, 2002.

[24] Y.-F. Wu et al. IEEE Electron Device Letters, 25(3):117–119, 2004.

[25] O. Ambacher et al. physica status solidi (b), 216(1):381–389, 1999.

[26] S.M. Sze. Physics of Semiconductor Devices. John Wiley & Sons, 3rd edition edition, 2007.

[27] M. Shur. GaA Devices and Circuits. Plenum Press, New York, 1987.

[28] K. Shinohara, et al. Electron Device Letters, IEEE, 32(8):1074 –1076, aug. 2011.

[29] Dong Seup Lee et al. Electron Device Letters, IEEE, 32(5):617 –619, may 2011.

[30] Yuh-Renn Wu et al. IEEE Transactions on, 53(4):588 – 593, april 2006.

[31] G.H. Jessen, et al. IEEE Transactions on Electron Devices, 54(10):2589–2597, 2007.

[32] J. M. Golio, "RF and Microwave Semiconductor Device Handbook". CRC Press, 2003.

[33] T. Zimmermann et al. Electron Device Letters, IEEE, 29(7):661 –664, july 2008.

[34] Huili Xing et al. Electron Device Letters, IEEE, 25(4):161 – 163, april 2004.

[35] S.L. Selvaraj et al. Electron Device Letters, IEEE, 30(6):587 –589, june 2009.

[36] S. Haffouz et al. Solid-State Electronics, 49(5):802–807, 2005.

[37] Guowang Li et al. Electron Device Letters, IEEE, 31(9):954 –956, sept. 2010.

[38] Chao Chen et al. Electron Device Letters, IEEE, 32(10):1373 –1375, oct. 2011.

[39] Yee-Chia et al. IEEE Transactions on, 50(4):1027 – 1035, april 2003.

[40] F. Medjdoub et al. Electronics Letters, 43(12):691 –692, 7 2007.

[41] E. Kohn et al. Microwave Theory and Techniques, IEEE Transactions on, 51(2):634 – 642, feb 2003.

[42] R. Vetury et al. Electron Devices, IEEE Transactions on, 48(3):560 –566, mar 2001.

[43] G. Simin et al. Applied Physics Letters, 79(16):2651–2653, 2001.

[44] E. Kohn et al. Electronics Letters, 35(12):1022 –1024, jun 1999.

[45] E. Kohn et al. Electronics Letters, 38(12):603 –605, jun 2002.

[46] G. Meneghesso et al. IEEE Transactions on, 51(10):1554 – 1561, oct. 2004.

[47] H. Kim et al. IEEE Electron Device Letters, 24(7):421–423, 2003.

[48] M. Faqir et al. IEEE Transactions on Electron Devices, 55(7):1592–1602, 2008.

[49] M Alomari, PhD Thesis, University of Ulm, 2012.

[50] Yi Pei et al. Electron Device Letters, IEEE, 30(4):313 –315, april 2009.

[51] H. Behmenburg et al. physica status solidi c, 7:2104, 2010.

[52] M. Higashiwaki et al. IEEE Electron Device Letters, 27(9):719–721, 2006.

[53] X. Hu et al. Applied Physics Letters, 79(17):2832–2834, 2001.

[54] C. Ostermaier et al. Physica Status Solidi (C), 5(6):1992–1994, 2008.

[55] J. Robertson et al. Chemistry of Materials, 14(10):4350–4358, 2002.

[56] S. Abermann et al. Semiconductor Science and Technology, 22(12):1272– 1275, 2007.

[57] S. Abermann et al. Electronics Letters, 45(11): 570–572, 2009.

[58] S. Abermann et al. ECS Transactions, 25(4):123–129, 2009.

[59] Y. Irokawa et al. Applied Physics Letters, 84(15):2919–2921, 2004.

[60] R. Gaska et al. Electron Device Letters, IEEE, 19(3):89 –91, mar 1998.

[61] Jeong Park et al. IEEE Trans on Electron Device, 51(11):1753 – 1759, nov. 2004.

[62] M. Gonschorek et al. Journal of Applied Physics, 109(6):063720 –063720–8, mar 2011.

[63] J. Joh et al. IEEE Electron Device Letters, 29(4):287–289, 2008.

[64] J. Kuzmik et al. Journal of Applied Physics, 106(12), 2009.

[65] D. Maier et al. IEEE Transactions on, 10(4):427 –436, dec. 2010.

[66] D. Maier et al. DRC, 2011 69th Annual, pages 73 –74, june 2011.

[67] M. Gonschorek et al. Applied Physics Letters, 89(6):062106 –062106–3, aug 2006.

[68] Haifeng Sun et al. Electron Device Letters, IEEE, 30 (8):796 –798, aug. 2009.

[69] J. Kuzmik et al. IEEE Transactions on Electron Devices, 55(3):937–941, 2008.

[70] J. Kuzmik et al. IEEE Transactions on Electron Devices, 57(9):2144–2154, 2010.

[71] L Liu et al. Materials Science and Engineering R, 37:61–127, 2002.

[72] A Yoshikawa et al. Wide Bandgap Semiconductor. Springer, 2007.

[73] T Detchprohm et al. JJAP, 40(Part 2, No. 1A/B):L16–L19, 2001.

[74] F. Medjdoub et al. DRC, 2007 65th Annual, pages 109 –110, june 2007.

[75] S. Rai PhD Thesis University of South Carolina, USA 2006.

[76] Adivarahan V et al. Applied Physics Letter, 88 182507 2006.

[77] Y. Dora, PhD Thesis University of California, Santa Barbara, USA 2006.

[78] R. Vetury et al. IEEE Electron Device Letters, vol 48, pp 560-566, March 2001.

[79] Robert Coffie, PhD thesis, University of California, Santa Barbara, 2003.

[80] S. Karmalkar et al. IEEE Transactions on Electron Devices, vol.48, no.8 pp.1515-1521, Aug 2001.

[81] Q. Fareed et al. P hys. Status Solidi C **8**, No. 7–8, 2454–2456 (2011)

[82] R. Wang et al. IEEE Electron Device Lett. 31 (2010) 1383.

[83] W. B. Lanford et al. Electron. Lett. 41 (2005) 449.

[84] Y. Cai et al. IEEE Trans. Electron Devices 53 (2006) 2207.

[85] Y. Uemoto et al. IEEE Trans. Electron Devices 54 (2007) 3393.

[86] M. Higashiwaki et al. IEEE Trans. Electron Devices 54 (2007) 1566.

[87] C. S. Suh et al. IEDM Tech. Dig., 2006, p. 911.

[88] T. Adachi et al. Proc. Device Research Conf., 2008, p. 129.

[89] T. Oka et al. IEEE Electron Device Lett. 29 (2008) 668.

[90] W. Lim et al. Electrochem. Solid-State Lett. 14 (2011) H205.

[91] M. Kanamura et al. IEEE Electron Device Lett. 31 (2010) 189.

[92] H. Sun et al. IEEE Electron Device Lett. 31 (2010) 957.

[93] W. Mao et al. Chin. Phys. Lett. 27 (2010) 128501.

[94] Gonschorek M et al. Appl. Phys. Lett. 89 062106

[95] Wang H et al. Phys. Status Solidi c 7 2440 2010

[96] S. Guo et al Phys. Status Solidi a 207 1348 2010

[97] F. Medjdoub et al. IEEE Electron Device Lett. 29 422 2009.

[98] Medjdoub F et al. 2008 Open Electr. Electron. Eng. J. 2 1

[99] Kuzmik J et al. 2008 IEEE Trans. Electron Devices 55 937

[100] Morgan D et al. 2011 Appl. Phys. Express 4 114101

[101] Alomari M et al. 2009 IEEE Electron Device Lett. 30 1131

[102] Saygi S et al. 2005 Appl. Phys. Lett. 87 043505

[103] Mizue C et al. 2011 Japan. J. Appl. Phys. 50 021001

[104] Gonschorek M et al. 2010 Int. J. Microw. Wireless Technol. 2 13

[105] Gould R D et al. 2004 Thin Solid Films 469–470 184

[106] Medjdoub F et al. 2011 Appl. Phys. Lett. 98 223502

[107] Kordoš P et al. 2012 J. Electron. Mater. 41 3013

[108] Liu H Y et al. 2013 IEEE Trans. Electron Devices 60 2231

[109] Medjdoub F et al. 2007 Int. J. High Speed Electron. Syst. 17 91

[110] Xie J et al. 2008 Proc. SPIE 6894 68941R

[111] Schroder D K 2006 Semiconductor Material and Device Characterization (Hoboken, NJ: Wiley)

[112] Liu Z H et al. 2009 Appl. Phys. Lett 95 223501.

[113] Arslan E et al. 2009 Semicond. Sci. Technol. 24 075003

[114] Eickelkamp M et al 2011 J. Appl. Phys. 110 084501

[115] Ketteniss N et al. 2012 Semicond. Sci. Technol. 27 035009

[116] Sze S M 1981 Physics of Semiconductor Devices (Hoboken, NJ: Wiley)

[117] Koudymov A et al. 2002 Appl. Phys. Lett. 80 3216

[118] A. M. Dabiran et al. Appl. Phys. Lett. 93, 082111 (2008).

[119] Khan M A et al. Appl. Phys. Lett. 77 1339 (2000).

[120] Simin G et al. 2001 IEEE Electron Device Lett. 22 53

[121] Chabak K D et al 2010 IEEE Electron Device Lett. 31 561

[122] Wang R et al. 2010 IEEE Electron Device Lett. 31 1383

[123] Simin G et al. 2005 Electron. Lett. 41 774

[124] Chung J W et al. IEEE Electron Device Lett. 29 1196

[125] http://my.ece.ucsb.edu/mgrundmann/bandeng.

[126] H. Wang et al. Phys. Status Solidi C 7, 2440 (2010).

[127] Yue Y Z et al. IEEE Electron Device Lett. 33 988 (2012)

[128] N. Sarazin et al. IEEE Electron Dev. Lett. 31, 11 (2011).

[129] V. Adivarahan et al. IEEE Electron Device Lett. 26, 535 (2005).

[130] M. Eickelkamp et al. Journal of Applied Phys. 110, 084501 (2011).

[131] D. S. Lee. X et al. IEEE Electron Dev. Lett. 32, 1525 (2011).

[132] M. Asif Khan et al. Appl. Phys. Lett. 77, 1339 (2000).

[133] X. Sheng et al. Inter. Conf., pp. 1 – 2 (2011).

[134] G. Simin et al. IEEE Electron Dev. Lett. 22, 53 (2001).

[135] M. Gonschorek et al. Appl. Phys. Lett. 89, 062106 (2006).

[136] G Simin et al IEEE Electron Dev. Lett., 26, 56 (2005)

[137] Tipirneni, N, IEEE Electron Dev. Lett., 27, 716 (2006)

[138] M Lachab et al. J. Phys. D. 47, 135108 (2014).

[139] D S Lee. X Gao et al. IEEE Electron Dev. Lett. 32, 1525 (2011).

[140] V Adivarahan et al. Appl. Phys. Lett. 88, 182507 (2006).

[141] G Simin et al. IEEE Electron Dev. Lett. 22, 53 (2001).

[142] X. Chang et al. Solid-State Electron., vol. 54, no. 1, pp. 42–47, Jan. 2010.

[143] S. Vitanov et al. Solid-State Electron., vol. 54, no. 10, pp. 1105–1112 (2010).

[144] M. Kuball et al. IEEE Electron Dev. Lett. 23, 7 (2002)

[145] J. D. Albrecht et al. J. Appl. Phys., vol. 83, pp. 4777–4781 (1998).

[146] Yang Liyuan et al. Journal of Semiconductors, Vol. 34, No. 7, (2013).

[147] F. Schwierz et al. Modern Microwave Transistors. Hoboken, NJ, USA: Wiley, ch. 5 (2003).

[148] R. Menozzi et al., IEEE Trans. Device Mater. Rel., vol. 8, no. 2, pp. 255–264, Jun. 2008.

[149] B. S. Eller et al. J. Vac. Sci. Technol. A, vol. 31, no. 5, pp. 050807-1–050807-29 (2013).

[150] S. Turuvekere et al. IEEE Trans. Elec. Dev., vol. 60, no. 10, pp. 3157–3165(2013).

[151] J. W. Chung et al. IEEE Electron Device Lett., vol. 29, no. 11, pp. 1196–1198 (2008).

[152] R. Vetury et al. IEEE Transactions on Electron Devices, vol. 48, NO. 3 (2001).

[153] R. Gaska et al. Electron Device Letters, IEEE, 19(3):89 –91, mar 1998.

[154] J Park et al. IEEE Transactions on Electron Devices, 51(11):1753 – 1759, Nov. 2004.

[155] S. Nuttinck et al. Microwave Theory and Techniques, IEEE Transactions on, 51(12):2445 – 2452, Dec. 2003.

[156] M. Kuball et al. 60th DRC Conference Digest, pages 99 – 100, 2002.

[157] M. Gonschorek et al. Journal of Applied Physics, 109(6):063720 –063720–8, mar 2011.

[158] Mohammed Alomari, PhD thesis, Ulm University, Dec. 2012.

[159] M. Neuburger et al. physica status solidi (c), 0(6):1919–1939, 2003.

[160] A. Sarua et al. Electron Devices, IEEE Transactions on, 53(10): 2438 –2447, Oct. 2006.

[161] S. Rajasingam Electron Device Letters, IEEE, 25(7):456 – 458, July 20