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Wireless Channel Modeling For Networks On Chips

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WIRELESS CHANNEL MODELING FOR NETWORKS ON CHIPS

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DEDICATION

Every challenging work needs dedicated self-efforts as well as guidance of people whom we hold very closely to our hearts. I dedicate this dissertation to my father, my mother, my brother, and my sister and her husband along with their lovely family of three beautiful girls. Their constant words of encouragement that still ring in my ears helped me tremendously throughout my doctorate. I will be forever grateful.

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ABSTRACT

The advent of integrated circuit (chip) multiprocessors (CMPs) combined with the continuous reduction in device physical size (technology scaling) to the sub-nanometer regime will result in an exponential increase in the number of processing cores that can be integrated within a single chip. Today's CMPs already support tens to low hundreds of cores and both industry and academic roadmaps project that future chips will have thousands of cores. Therefore, while there are open questions on how to harness the computing power offered by CMPs, the design of power-efficient and compact on-chip interconnection networks that connects cores, caches and memory controllers has become imperative for sustaining the performance of CMPs.

As the limited scalability of bus-based networks degrades performance by reducing data rates and increasing latency, the Network-on-Chip (NoC) design paradigm has gained momentum, where a network of routers and links connects all the cores. However, power consumption of NoCs is a significant challenge that should be addressed to capitalize on the scaling advantages of multicores.

Also, improvements in metal wire characteristics will no longer satisfy the power and performance requirements of on-chip communication. One approach to continue the performance improvements is to integrate new emerging technologies into the electronic design flow such as wireless/RF technologies, since they provide unique advantages that make them desirable in a NoC environment. First, wireless technologies are ubiquitous and offer a wide range of options in communication, and there exists a vast body of

knowledge for the design and implementation of wireless chipsets using RF-CMOS technology. Second, wireless communication, unlike wired transmission, can be omnidirectional, which can facilitate one-hop unicast, multicast, and broadcast communication that can result in a reduction in power consumption while allowing for faster communication. Third, wireless communication can increase the communication data rate by the combination of Frequency Division Multiplexing (FDM) and Time Division Multiplexing (TDM) (and in the future, potentially spatial division multiplexing (SDM)). Therefore, Wireless NoC (WiNoC) interconnects have recently emerged as a viable solution to mitigate power concerns in the short to medium term while still providing competitive performance metrics, i.e., low power consumption, tens of Gbps data rates, and minimal circuit area (or volume) within the chip. Worth noting is that wireless links are not envisioned as replacing all wired links, but rather as augmenting the wired interconnection network.

In this dissertation, we employ simulations in HFSS from Ansys® to present accurate wireless channel models for a realistic WiNoC environment. We investigate the performance of these models with different types of narrowband and wideband antennas. This entails estimation of the scattering parameters for the channels between multiple antenna elements in the WiNoC, from which we derive channel transfer functions and channel impulse responses. Using these results, we can estimate the throughput of the various WiNoC links, and this allows us to design effective multiple access (MA) schemes via FDM and TDM. For these MA schemes, we provide estimates of maximal throughput. To further the feasibility study, we investigate the performance of a simple binary transmission scheme--On-Off Keying (OOK)--through the resulting dispersive

channels, which can facilitate one-hop unicast, multicast, and broadcast communication that can result in a reduction in power consumption while allowing for faster communication.

Our investigation of the performance of On-Off Keying modulation (OOK) also includes an analytical expression for bit error ratio (BER) that can be evaluated numerically. This enables us to provide the equalization requirements needed to achieve our target BERs. Finally, we provide recommendations for WiNoC design and future tasks related to this research.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AWGN ..... Additive White Gaussian Noise

BER ..... Bit Error Rate

BW ..... Bandwidth

CIR ..... Channel Impulse Response

C-MESH ..... Concentrated Mesh

CMOS ..... Complementary Metal Oxide Semiconductor

CMP ..... Chip MultiProcessor

CNT ..... Carbon Nanotube

DFE ..... Decision Feedback Equalizer

DFVS ..... Dynamic Frequency and Voltage Scaling

EM ..... Electromagnetic

EMC ..... Electromagnetic Coupling

EMI ..... Electromagnetic Interference

ERC ..... Error Correction Code

FDM ..... Frequency Division Multiplexing

FEM ..... Finite Element Method

FIFO ..... First In First Out

HFSS ..... High Frequency Structure Simulator

IE ..... Integral Equation

ISI ..... Inter Symbol Interference

ITRS ..... International Roadmap for Semiconductors

MA ..... Multiple Access

MaxSCBW ..... Maximum Single Channel Bandwidth

MEMS ..... Microelectromechanical Systems

MoM ..... Method of Moments

MOSFET ..... Metal Oxide Semiconductor Field Effect Transistor

MPC ..... Multipath Component

MWCNT ..... Multi-walled Carbon Nanotube

NOC ..... Network on Chip

NSF ..... National Science Foundation

OOK ..... On Off Keying

PDP ..... Power Delay Profile

RC ..... Resistive-Capacitive

RCS ..... Radar Cross Section

RF ..... Radio Frequency

RF-CMOS ..... Radio Frequency Complementary Metal Oxide Semiconductor

RFID ..... Radio Frequency Identification

RMS-DS ..... Root-Mean-Square Delay Spread

S2S ..... Side to Side

SDM ..... Spatial Division Multiplexing

SNR ..... Signal to Noise Ratio

TDM ..... Time Division Multiplexing

WiNoC ..... Wireless Network on Chip

Chapter 1

Introduction

1.1 Overview on Wired Networks on Chips

The emergence of chip multiprocessors (CMPs) coupled with aggressive technology scaling in the sub nanometer regime will result in a dramatic increase in the number of cores, the processing units that read and execute instructions that can be integrated on a single chip [1-3]. Some of today's CMPs that employ tens to low hundreds of cores include Intel's 80-core TeraFlops processor [4], NVIDIA's 512-core Fermi [5], Tilera's 72-core CMP [6], and the 256-core programmable many-core Kalray [7]. In addition, both academic and industry projections talk about future chips having thousands of cores [1, 2, 7]. Therefore, the design of power-efficient[1] and compact on-chip interconnection networks plays a crucial role to harness the computing power offered by CMPs [8]. These interconnection networks substantially affect the overall system performance.

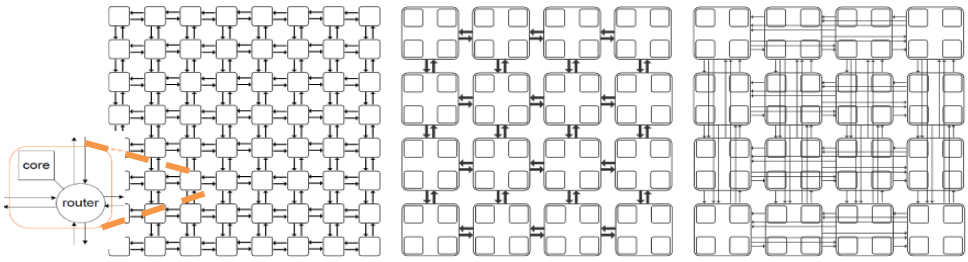
1.2 Existing On-Chip Interconnect Solutions

The most prevalent approach to interconnecting multi-core CMPs is through wired structures. Two dimensional meshes and rings are two common topologies that are used, and they are suitable for planar silicon dies due to their low dimensionality (2D vs. 3D). The benefits of two dimensional meshes (Figure 1(a)) are the short wire lengths and

[1] We address the power efficiency in Chapter 4.

the low router complexity. This low complexity comes from the fact that a data packet arriving at an intermediate router is forwarded to the next router until it reaches its destination, typically according to a simple routing algorithm. However, the 2D mesh network diameter, defined as the longest of the shortest path lengths from any node to any other node, is proportional to the mesh size. For an $N \times N$ mesh, the network diameter is 2 ($N^{1/2}$ - 1). Thus, meshes suffer from long network diameter, and this induces high network latencies.

The concentrated mesh, shown in Figure 1.1 (b), reduces the total number of network nodes by grouping multiple cores to share a network interface. For example, a 4-way concentration would lead to reducing the number of effective nodes by a factor of 4. Compared to the two dimensional mesh, the concentrated mesh has a smaller network diameter and better resource sharing but still suffers from poor scalability. Due to physical limitations that limit the degree of concentration, a concentrated mesh with for example, 1024 cores with 4-way concentration would have a network diameter of 30 hops and consequently still high and undesirable network latency. A "hop" is defined as a transition point that packets traverse on the path between source and destination.



(a) Mesh (b) Concentrated Mesh (c) Flattened Butterfly

Figure 1.1 Mesh, Concentrated Mesh and Flattened Butterfly topologies.

Recent efforts [9] proposed at "flattening" what is known as a conventional butterfly topology onto a two dimensional substrate. A butterfly topology consists of $(k+1)2^k$ nodes arranged in $k+1$ ranks (rows), each containing $n=2^k$ nodes where k is the order of the network. The resulting topology, referred to as a flattened butterfly (see Figure 1 (c)), along with the concentration technique used in the concentrated mesh, reduces the network diameter to only two hops. This can be achieved by using dedicated links to connect the concentrated nodes in all dimensions. However, in this flattened butterfly topology, the number of channels in each dimension increases quadratically with the number of nodes present, leading to very complex wiring layouts. Moreover, long wires connecting distant routers are undesirable since on-chip Resistive-Capacitive (RC) wires require frequent repeaters to propagate signals over long distances in order to avoid considerable signal level attenuation.

1.3 Scalability

Since it is only a matter of time until CMPs feature hundreds or thousands of cores, it is important to consider how the aforementioned interconnect solutions will scale when applied to CMPs with thousands of cores. In this context, minimizing the hop count is essential since intermediate routers are a significant source of delay. In addition, long wires are undesirable since on-chip RC wires require repeaters every few millimeters to maintain a detectable signal level over long wire spans. Thus, it is critical to see how the above interconnect solutions fair when accommodating CMPs with several hundreds or thousands of cores.

Even though simple ring arrangements are very cost effective, they are the least scalable since the hop count and consequent latency and energy grow linearly with the

number of cores. Most of the energy expenditure in Network on Chips (NOC) is due to overcoming attenuation in channels, router FIFOs(first-in first-out) buffers and router crossbar (switch) fabrics. Meshes perform better as the hop count scales with the square root of the mesh size. However, because a very significant amount of latency and energy is due to the intermediate router at each hop, it is clear that a more scalable solution is needed. As for the concentrated mesh (C-mesh) topology, it represents a significant improvement over the basic mesh by reducing the total effective node count and network diameter; it also diminishes the area footprint of this topology by reducing the effective node count by a concentration factor, *k*, and leads to better resource sharing. However, the concentration factor is restricted due to physical limitations such as router cross bar complexity and the size and energy required to support large numbers of input and output ports and so a large network C-mesh does not scale very well, and would still exhibit unacceptable network latency. On the other hand, even though low-diameter topologies such as the flattened butterfly reduce the network diameter to two, the high number of dedicated point to point links and long wires connecting distant routers cause complicated wiring problems and high attenuations (yielding an energy penalty). This makes the flattened butterfly topology also not very scalable since the link count increases quadratically in each dimension with the number of cores. Hence, the flattened butterfly topology is also not a very desirable topology for a thousand core network.

1.4 Wired Network Limitations and WiNoC Benefits

According to the International Roadmap for Semiconductors (ITRS), enhancements in metallic interconnects will no longer meet the power and performance requirements of on-chip communication [8]. This is mainly due to the limited scalability

offered by those metallic buses in addition to the RC delay caused by disproportionate scaling of transistors [9]. Both limitations have led to the emergence of Network-on-Chips architectures that employ shorter wires that improve throughput and reduce latency [10-15]. However, power dissipation due to routers and links in addition to losses incurred with lower technology node size can still cause bottlenecks for NoCs. In the 64-core Tilera mentioned earlier, it has been shown that NoCs consume 36 percent of total chip power while routers alone consume 40 percent of the individual tile power coming from core, cache, and router power. (A tile is an entity that combines a processor and its associated cache in addition to a switch.) Even though the router in Intel's Teraflops processor employs several power efficient techniques, it still consumes 28 percent of tile power, considerably higher than the targeted 10 percent of tile power [16]. Thus, as seen in Figure 1.2, power dissipation is the biggest hurdle for the NoC paradigm, as agreed by industry and academia [17, 18]. We can see from Figure 1.2 that at 45 nm, the communication and computation energy are almost equal. At a technology size of 7 nm, the computation energy decreases by a factor of 6 from that of the 45 nm technology, but the interconnection energy only decreases by a factor of 1.6. Also at 7 nm, the interconnection power is around 4 times that of the computation power. This means that future chip designers have to make optimizing the power-performance efficiency of communications a priority. To reduce power consumption, several concepts, such as dynamic frequency and voltage scaling (DFVS) techniques [19, 20], topology optimizations [21-23], router and crossbar optimizations [24-26], and encoding and signaling techniques [27], have been proposed. However, these techniques come at a price in terms of performance reduction (encoding, topology), or area overhead (router

optimization). Hence, the issues of power consumption, performance and area overhead have to be addressed *together* in order to improve future CMP system performance.

In an effort to reduce power consumption in NoCs, new methods of integrating emerging technologies have been proposed for the interconnection design of NoCs, such as silicon nanophotonics [28-32], 3D integration [10, 33-35], and wireless/RF technologies [36] . Although silicon nanophotonics and 3D interconnects have power and performance advantages, they still face considerable technological (fabrication) barriers, require innovative material advances and significant paradigm shifts in design. On the other hand, relatively mature wireless technologies can provide unique advantages that make them very desirable in a NoC environment. The first advantage that wireless technologies bring is the wide range of options they provide in various communications applications.

A large amount of information exists for the design and implementation of wireless chipsets, utilizing RF-CMOS technology. Second, wireless communication offers different degrees of flexibility in the spatial, temporal and frequency domains; unlike wired transmission, wireless communication can be omnidirectional, which can enable one-hop unicast, multicast and broadcast communication that can reduce power utilization while yielding faster communication. Third, wireless interconnects can increase the communication data rate by a combination of Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), and Spatial Division Multiplexing (SDM). Subsequently,Wireless NoC (WiNoC) interconnects have as of late developed as a potential solution for power consumption concerns in the short to medium term. Notwithstanding, the design of efficient and compact WiNoC architectures for

ultrashort (1-10 mm) wireless separations with different multiplexing alternatives is not trivial, given the high capacity required of wired interconnects (very high data rates, e.g., 10 Gbps), the diverse inter-core traffic patterns involved, the number and dimensions of antennas needed, and the often severe channel dispersion in the WiNoC environment. Therefore, the focus of this dissertation is the wireless communication aspect of this multi-faceted problem; the other two major research areas involved in this WiNoC project are efficient transceiver circuits and devices, and computer architecture and networking design. These areas have been investigated by our colleagues in this project.

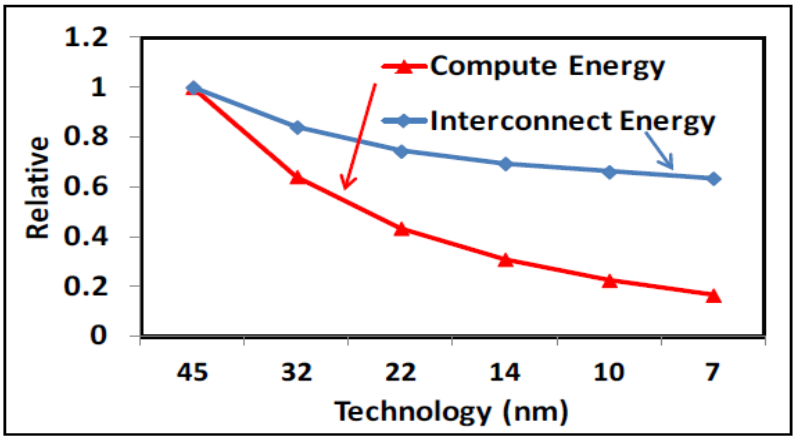


Figure 1.2. Relative compute and interconnect energy scaling with technology [37].

1.5 Spectral Bands for WiNoC's

In order for wireless links to truly enhance NoC performance, they must provide high throughputs (e.g., tens of gigabits per second), utilize power- and area-efficient transceivers, and employ efficient multiple access (MA) across the shared spatial channel. Providing tens of gigabits per second among multiple cores is a challenging task especially when frequency spectrum is limited. This limited spectrum is due to the fact that devices can operate over a finite frequency range; in addition there may also be

regulatory limitations. Although link distances are very short, wireless transceivers must have minimal power consumption, and in the low mmwave frequency range, antennas will be inefficient due to their small electrical size (required to physically fit on the chip). The high data rate requirement also challenges circuit design, as most digital circuits cannot currently operate at these rates, and required serial-parallel conversions may introduce additional and unacceptable power consumption and complexity, so very simple modulation/demodulation schemes may be required. Since spectrum is limited (primarily by devices), time and frequency division must be used to allow sharing of the wireless medium. Spatial-division multiplexing (SDM) can provide valuable spatial reuse of time-frequency resources, but this is very challenging at millimeter wave frequencies because of the small and simple antennas that must be employed.

Thus, trades among various options in the three design areas must be made, and for this it is of interest to look at frequency bands higher than the millimeter wave bands. Increasing the carrier frequencies would provide more bandwidth but also introduces other challenges. In Table 1.1 [38] we provide a summary of these considerations in three broad frequency bands. We considered the frequency bands in three broad categories: circuits/devices, antennas/propagation, and system/architecture. The "best" band is not obvious, although selecting the frequency band of 150–500 GHz may satisfy the largest number of design criteria in the near term. It is clear that although a very challenging task, to design and implement a complete solution for WiNoCs, all three design areas have to be considered and optimized.

Table 1.1. WiNoC technology challenges in three potential frequency bands [38].

Technology/Design Area	Frequency Band		
	50-150 GHz	**150-500 GHz**	**500 GHz-3 THz**
Circuits, Devices	Status: currently feasible Technology: RF-CMOS, substrate SOI	Status: encouraging Technology: SiGe-BiCMOS, substrate SOI	Status: immature Technology: III-V/Si hybrid, substrate alumina
Antennas, Propagation	Status: very challenging Issues: electrically-small (inefficient) antennas, near field coupling	Status: challenging Issues: nearing conventional antennas, far-field conditions	Status: reasonable Issues: at highest *f*'s, propagation analysis conventional, antennas immature
System, Architecture	Issues: throughputs too low, SDM very difficult Area: Low-Q inductors, large antenna size Power: Manageable	Issues: sufficient throughput, SDM challenging Area: Very lossy substrates, ultra-low Q Power: challenging	Issues: ample throughput, SDM possible Area: limited by waveguides & sources Power: Very challenging

1.6 Dissertation Objectives

In this section, a list of the dissertation objectives is presented.

1. [Chapter 2]: Perform a literature review of state of the art characterization of the WiNoC propagation channel. We also review existing work on WiNoC channel

and antenna modeling and look at their performance in terms of bandwidth, impedance matching, gain, and efficiency. Finally, we point out the gaps that we fill in the dissertation.

2. [Chapter 3]: We present a description of the numerical methods that HFSS®, the 3-Dimensional software we use for our simulations and designs, uses and discuss the advantages and disadvantages of each method. Finally, we show example results for a monopole antenna including its return loss and radiation pattern.
3. [Chapter 4]: We present the first two types of simple antennas we simulated in HFSS inside the WiNoC environment—quarter wavelength monopoles and printed dipoles. We present results on the antenna themselves, such as return loss and radiation pattern, in addition results for the wireless channels the communication signals must traverse, in terms of insertion losses and dispersion measures, which are critical to quantify for the design of efficient and reliable wireless communication links. We also present results for the throughput of frequency division multiple access schemes based upon the wireless channel (and antenna) characteristics.
4. [Chapter 5]: We investigate and present results of inherently wideband antennas inside the WiNoC environment. Similar to the treatment in chapter 4, we show results on the antennas themselves and the wireless channels between them, in addition to the throughput of frequency division multiple access schemes based upon the wireless channel characteristics.
5. [Chapter 6]: We investigate, through an analysis, the performance of a basic binary modulation, on-off keying (OOK) through a generic dispersive channel

and find an analytical expression for BER that can be evaluated numerically. We also present the performance improvements attainable with equalization of highly dispersive channels that exhibit bit error rate floors.

6. [Chapter 7]: Summarize the dissertation and indicate future work.

1.7 Dissertation Contributions

The project "Power-Efficient Reconfigurable Wireless Network-on-Chips (NoC) Interconnects for Future Many-core Architectures" was funded by the National Science Foundation (NSF) - ECCS Division, and began in September 2011. The research group consists of a collaborative effort between two Ohio University faculty members and their students and my advisor Dr. David Matolak and myself. The group has three journal publications and seven conference publications; I am an author on the three journal papers and four of the six conference publications. The notations J and C used in the following list denote journal paper and conference paper, respectively. Ultimately, our contribution in this dissertation is the illustration of practical WiNoC channel, antenna, and communication link performance characteristics, along with observations and results useful for future research in this area.

[J1] D. DiTomaso, A. Kodi, D. W. Matolak, S. Kaya, S. Laha, and W. Rayess, "A-WiNoC: Adaptive Wireless Network-on-Chips (NoCs) Architecture for Future Multicores," *IEEE Transactions on Parallel and Distributed Systems*, vol. 26, no. 12, pp. 3289 – 3302, December 2015.

[J2] S. Laha, S. Kaya, D. W. Matolak, W. Rayess, D. DiTomaso, and A. Kodi, "A New Frontier in Ultra-low Power Wireless Links: Network-on-Chip and Chip-to-Chip

Interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 2, pp. 186-198, February 2015.

[J3] D. Matolak, A. Kodi, S. Kaya, D. DiTomaso, S. Laha, and W. Rayess, "Wireless Networks-on-Chips: Architecture, Wireless Channel, and Devices," *IEEE Wireless Communications Magazine,* Special Issue on Wireless Communications at the Nanoscale, October 2012.

[C1] M.A.I, Sikder, A. Kodi, D. DiTomaso, S. Kaya, W. Rayess, D. Matolak., "Exploring Wireless Technology for Off-Chip Memory Access", *IEEE 24th Annual Symposium on High-Performance Interconnects (HOTI*, Aug. 2016

[C2] A. Kodi, A. Sikder, D. DiTomaso, D. W. Matolak, S. Kaya, S. Laha and W. Rayess, "Kilocore Wireless Network-on-Chips (NoCs) Architecture," *2nd ACM International Conference on Nanoscale Computing and Communication (NanoCom)*, Boston, Massachusetts, 21-22 September 2015.

[C3] S. Kaya, S. Saha, D. DiTomaso, A. Kodi, D. W. Matolak, and W. Rayess, "On Ultra-short Wireless Interconnects for NoCs and SoCs: Bridging the 'THz Gap'," *56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, Columbus, Ohio, 4-7 August 2013.

[C4] D. DiTomaso, A. Kodi, D. Matolak, S. Kaya, S. Laha, and W. Rayess, "Energy-efficient Adaptive Wireless NoCs Architecture," *7th International Symposium on Networks-on-Chip*, Tempe, Arizona, 21-24 April 2013.

Other Project Conference Papers (on which I am not a co-author)

[C4] S. Laha, S. Kaya, A. Kodi, D. DiTomaso, and D. Matolak, "A 60 GHz tunable LNA in 32 nm Double Gate MOSFET for a Wireless NoC Architecture," *IEEE Wireless and Microwave Technology Conference*, 7-9 April 2013.

[C5] D. DiTomaso, S. Laha, A. Kodi, S. Kaya, and D. Matolak, **"**Evaluation and Performance Analysis of Energy Efficient Wireless NoC Architecture," *55th International Midwest Symposium on Circuits and Systems,* Boise, Idaho, 5-8 August 2012.

[C6] D. DiTomaso, S. Laha, S. Kaya, D. Matolak, and A. Kodi, "Energy-Efficient Modulation for a Wireless Network-on-Chip Architecture," *10th IEEE International NEWCAS Conference,* Montreal, Canada, 17-20 June 2012.

I also have a publication under review in the *Wireless Personal Communications Journal*:

W. Rayess, D. W. Matolak, S. Kaya, A. Kodi, "Antennas and Channel Characteristics for Wireless Networks on Chips," submitted November 2015.

Chapter 2

Literature Review

We have divided this review into three categories: intra-chip antennas, inter-chip antennas, and papers that deal with carbon nanotubes and metamaterials. The first category is directly applicable to WiNoCs; the second may be suitable if the structures can be modified (reduced in size); and the third category represents more novel or speculative designs. Table 2.1 contains a summary of the results from the literature review.

2.1 Intra-Chip Antennas

As a result of rapidly expanding applications for sensor networks, Radio Frequency Identification (RFID) tags and system-on-chip integration, intra-chip antennas have recently drawn attention. In [39], the authors analyzed several antenna structures and produced simulation results for transmission gain at microwave frequencies. Although these frequencies are too low for most WiNoC applications, we provide results for completeness. The transmission gain is the decibel sum of transmit and receive antenna gains plus the path gain; when measured it is essentially the scattering parameter S_{21}, which quantifies gain from port one to port two. As expected, meander, zigzag, and folded structures showed higher gains than linear dipoles (all structures are planar, printed on substrate material). It is difficult to separate with precision the actual antenna

gains and channel attenuations from these transmission gain values, since this requires an assumption for the path gain (or loss). Thus our antenna gain estimates cited throughoutare of limited accuracy, since we employ only the very simplest of path loss models, but the *relative* gain values among the different antenna types is accurate. The transmission gain for the linear dipole pair in [39] was between approximately -70 to -50 dB for the frequency range 1-8 GHz with maximum gain occurring near 6 GHz. The meander dipole had a gain between 10-15 dB larger, with the peak value occurring at around 5.8 GHz, and the folded dipole had a gain between 0 and 25 dB larger than the dipole, with its peak value occurring near 6.5 GHz. If we employ the free space loss model, the transmission gains cited would yield maximum antenna gains of approximately -16.9, -13.9, and -24.3 dB for the meander, folded dipole, and linear dipole, respectively. The size of these antennas ranged from 8-9 mm and the link distance was 4.7 mm, hence far-field conditions are not attained for our (absolute) antenna gain estimates. The simulations in [39] were done using Sonnet® Suites™.

In [40], the authors investigated the effect on the transmission properties of an on-chip dipole antenna when a diamond layer was inserted between a silicon substrate and its heat sink. The size of the antenna simulated in HFSS was 2 mm. The range of simulation frequencies was 5-40 GHz. The transmission gain of the on-chip dipole antennas was estimated for different link distances. It was concluded that a higher gain could be achieved with a diamond layer (0.35 mm thick) atop the substrate than without the layer. Transmission gain was largest from 15-40 GHz with the 0.35 mm thick diamond layer; link distance was less than 3 mm. The corresponding antenna gain, assuming a free space model, with the lower resistivity silicon substrate (10 Ω-cm) would

be -7.9 dB. With a higher resistivity substrate (100 Ω-cm), the corresponding antenna gain would be -2.9 dB. A complication here again is that the link distance of 1 mm is *not* in the far field at 26 GHz—nonetheless, the relative antenna gain between the cases is accurate. Additional impedance matching networks are needed in the configuration in [40] since throughout the simulation, the resistances were above 50 ohms. In addition, adding a diamond layer would increase the overall chip implementation cost and complexity.

The authors in reference [41] investigated meander antennas with different pitches, lengths, widths, and numbers of turns. These antennas are printed conductors that resemble "square wave" shapes fabricated on a P-type SiO_2 substrate. HFSS was used to conduct simulations. The authors found that increasing the pitch length and number of turns while decreasing the antenna width did increase the radiation efficiency. Table 2.1 has additional specifications.

In a very early paper in the field, the authors of [42] investigated short linear, meander, and zigzag dipole antennas experimentally. These antennas were formed on a silicon wafer. Table 2.1 summarizes results. In [43], two kinds of antennas were realized, the inverted-F and dipole. Their characteristics were also investigated via simulations (HFSS) and are shown in Table 2.1.

In [44], the author investigated the effect of using a metamaterial crystal substrate with*in* the dielectric layer on which a rectangular microstrip patch antenna was mounted. This reference employs simulations (CST Microwave Studio) to determine antenna characteristics (Table 2.1) for operation at THz frequencies. For interested readers,

references [45]-[47] report on designs in the high mm-wave and sub-THz frequency ranges.

The authors of [48] compared the performance of a dipole antenna pair with a phased array pair for on-chip communication. The array consisted of four orthogonal quarter wave monopole linear arms that are fed differentially. Their simulations were done using CST Microwave Studio, with results again in Table 2.1.

Reference [49] described a WiNoC in which printed zig-zag antennas are used. The authors discussed at length the required connectivity and routing, but also described the main antenna features. Antenna gains were approximately -18.5 dB with a center frequency near 63 GHz.

Reference [50] presented four designs for on chip antennas operating at 90 GHz and 140 GHz, and compared their performance; see Table 2.1. The antennas were a bowtie-shaped slot antenna, a cavity-backed slot antenna, an extremely flat waveguide slot antenna, and an E-shaped patch antenna.

The authors of [51] designed, fabricated and measured the performance of a dual band Buckled Cantilever Plate triangular fractal antenna on flexible polyamide at 60 GHz and 77 GHz. The movable plate enables horizontal and vertical polarization on the same chip. An increase of 6 dB in gain was observed in the vertical position compared to the horizontal.

2.2 Inter-Chip Antennas

Due to the availability of unlicensed bands in the 60-90 GHz range for several upcoming applications such as vehicular radars and in-room multimedia links, as well as commercially available RF-CMOS processes in the mm-wave regime, inter-chip antennas are also relevant for the WiNoC problem. For instance, reference [52] reported on results using an ultra wide band triple “twiggy” antenna that was developed using 65 nm complimentary metal-oxide semiconductor (CMOS) technology. No explicit antenna parameters were provided.

In [53] the authors proposed the design of a two-antenna array at 60 GHz for chip-to-chip communication, with simulations done using HFSS. Despite the fact that the array antenna offers an increase in gain of 5 dB in the horizontal direction over a single antenna, a crucial characteristic not reported in [53] is the physical size of these antennas. A similar design in [54] consists of a four-element array that achieves 8 dB increase in gain over the single antenna in the diagonal direction with a 30 GHz bandwidth at 60 GHz.

In [55], a dielectric waveguide with a high dielectric constant was used under a silicon chip to improve the efficiency and transmission gain of the on-chip antenna. Efficiency and gains were investigated as functions of the silicon resistivity and thickness. The gain increased with a thinner silicon substrate. Efficiency and transmission gain improvements of 50% and 25 dB, respectively, were seen at a transmission distance of 20 mm with the thinner substrate. Thus the paper notes an important fabrication point that large relative permittivity dielectrics found in sub-45 nm metal–oxide–

semiconductor field-effect transistor (MOSFET) gate stacks may also be used as the top insulator/passivation layers before the antennas are fabricated.

Reference [56] presents results for different patch antennas that were designed with various gap configurations; simulated values of return loss were provided. Two of the five types of patch antennas with different gap configurations were fabricated, and the experimental results showed a difference of 1.5 GHz in the resonant frequency between measurements and simulations. A worst case transmission gain of -47 dB for a chip-to-chip link of distance 35 mm yields an estimate of approximately -3.75 dB for the antenna gain (again assuming free space).

The authors of [57] designed a wireless inter-chip link using bond-wire antennas. The chip was fabricated using 180 nm SiGe technology. Data rates of 2 to 6 Gbps were achieved over distances from 0.5 to 4 cm, at a center frequency of 43 GHz. Antenna gains were measured to be approximately -1.4 dB.

In [58], the authors reviewed the use of on-chip antennas for over the air communication and presented ways to increase communication range. To achieve this, the authors suggest using 6 mm monopole antennas operating at 5.8 GHz instead of 3 mm dipole antennas operating at 24 GHz in addition to thinning the silicon substrate below the antennas from 670 μm to 100 μm. Note that decreasing the operating frequency increases range naturally, but also generally has the undesirable effect of reducing bandwidth. The antenna gains are highly dependent on their height from the ground plane; for example, gains drop by 20 dB when the height decreases from 52 cm to 5 mm. With the original (“unthinned”) substrate, the antenna gains are approximately -12 dB

whereas in the thinner substrate case, the on-chip 24 GHz dipole and 5.8 GHz monopole gains are -7 dB and -11 dB, respectively. Interested readers who would like more insight on this topic are referred to [59].

2.3 Carbon Nanotubes and Metamaterial Antennas

Reference [60] is a nice overview paper on the properties of carbon nanotubes. It shows that nanotubes have very unique electrical, mechanical, thermal, and optical properties, which make them very good candidates for on chip antennas. Fabricating them in a scalable manner and integrating them with CMOS circuits is though currently expensive and challenging, hence we present these results as a potential future option for WiNoC antenna design.

The authors of [61] have some interesting results, with good radiation patterns for plasmonic antennas. One issue is that these plasmonic antennas must be illuminated by a laser beam to resonate. This consumes substantial power, and this is problematic in WiNoC systems that aim to be as power efficient as possible.

In [62] the authors show some promising results for multi-walled carbon nanotubes (MWCNTs). Again, required excitation through a laser would consume a considerable amount of energy, disadvantageous in a NoC environment. Also, the high temperatures used to grow the MWCNT's could make it very challenging to integrate these structures with CMOS devices.

Reference [63] explored antennas for a relatively low frequency range (up to 10 GHz). The size of the antennas (10 mm × 10 mm and 20 mm × 20 mm) is large—almost as large as the entire integrated circuit (IC) in many cases. Also, integration with CMOS

may be questionable especially when the process of fabricating these antennas involves temperatures as high as 720 degrees Celsius.

Another interesting paper on Carbon Nanotubes (CNTs) is [64], in which the authors describe the use of CNT "forests" for antennas. A very nice analysis is performed for OOK performance, but for the applications described, the center frequency is extremely low (~15 MHz), which limits data rates to below 1 Mbps.

2.4 Additional Remarks

From Table 2.1 we can draw several conclusions regarding WiNoC antenna design:

1. research to date has been focused on microwave and low-millimeter wave frequencies, which is likely not high enough to support future WiNoC data rates.

2. most antenna gains found in the literature, except for [44], [49], [53],and [53] are less than 0 dB, which means that the antenna adds *losses* to the transmission.

3. printed antenna structures are most common, with non-monotonic effects vs. frequency for substrate thickness.

4. impedance matching of the antenna to the transceiver/transmission line is often required, although exceptions exist, e.g., in [59] a co-design approach canceled the need for a matching network by optimizing the antenna and IC for conjugate matching. However, when present, matching networks still occupy valuable WiNoC transceiver area.

5. antenna efficiencies may be very low (part of this may be attributable to impedance mismatching), which means that additional transmission power is required compared to the impedance-matched case.

6. reported results for transmission gain obscure the specification of antenna gain itself, making antennas used within such transmission gain results not "portable" to other physical settings.

7. reported bandwidths are in many cases larger than our minimum estimated bandwidth of 10 GHz, which is promising.

Given the novelty of the WiNoC environment, for WiNoC antennas, we may need to deviate from conventional antenna theory meant for 3D far-field communication since the actual WiNoC antenna requirements differ substantially from those used in conventional designs. It is our belief that the challenges in WiNoC antennas also provide unique opportunities to design novel on-chip antennas using perhaps revolutionary innovations in nanotechnology and nanomaterials. Some of these solutions are very likely to broaden the concept of on-chip antennas significantly, and some rely on novel materials (e.g., [39]), unique insights on nanotechnology, and micro integration. What follows is a non-exhaustive list of ideas that we have found in the literature for novel compact antenna designs. Such ideas would be very valuable in the future design and manufacturability of WiNoC systems and environments.

- **Inductive Coupling**: commonly used for power transmission over short distances, laterally and vertically coupled inductances may be used to communicate between the closest transceivers [65].
- **Metamaterials**: as also suggested by [39], metamaterials designed for mm wave performance can be used to isolate and focus radiation, especially in the higher bands of interest. They may also be used to reduce the antenna size, especially in the higher end of the frequency range considered, i.e., the THz regime.
- **Pulse-Driven Antennas**: although only demonstrated for HF transmission [66] thus far, the idea of actual pulses driving antennas without impedance matching is a very promising and intriguing possibility for WiNoCs, as it can further reduce area/power requirements and minimize circuitry required for modulation.
- **Plasmonic (Yagi-Uda) Antennas**: plasmonics, another by-product of nanophotonics and nanomaterials, provide extremely novel radiation mechanisms to enable electromagnetic radiation using plasmon coupled waves on metal nanostructures. A recent paper on this idea [67] claims that the concept can be extended to THz radiation, and this would be a very promising way to build compact antennas with moderate gain.
- **Bonding-wire Antennas**: another unique possibility for WiNoCs is the use of existing bond wires at the perimeter of the chip as antennas for on-chip communication (e.g., [57]). While this would require unique optimizations to the geometry of the wires and an infrastructure to (de)-couple radiation, it is possible that some of the (dummy) IC bond-wires could be reserved for this purpose.

- **MEMS/3D Structures**: over the last 20 years, the Microelectromechanical Systems (MEMS) community has amassed many CMOS compatible fabrication options to build folding/assembling 3D (strictly speaking 2.5D) metal structures that can reach 100's of microns in length [68]. It may be possible to borrow ideas to build folded or vertical antenna structures that can liberate area constraints substantially.
- **2D reflectors/directors**: on-chip antennas can benefit from planar and/or vertically stacked reflector/director metal structures (once again built using largely MEMS technology) to improve the antenna directivity and efficiency. Actually, this would be easier to implement for planar structures than fully 3D cases in conventional large antennas.

While some of these ideas and concepts may be difficult and challenging to implement in a WiNoC environment, an innovative combination of these ideas will be needed to bring the sought after performance promised by WiNoCs. Promising and rapid advancements in technology would be very helpful in bringing these methods and ideas into fruition and facilitating the actual manufacturing of the WiNoC components and landscape. Moreover, these innovative concepts would allow to extract the performance gains that WiNoCs present in future multi core chips and systems.

Table 2.1. Summary of WiNoC antenna characteristics from the literature

Ref	Antenna Size	Bandwidth B, Center Freq f_c Frequency Range Δf	Antenna Gain (dB)	Impedance (Ω)	Efficiency	Comments
[39]	8.9 mm	Δf= 1.8 GHz f_c= 4 GHz	-16.9, -13.9, -24.3	N/A	N/A	• Gains: meander, folded dipole, linear dipole, respectively • Gains estimated from free-space (not in far field) • Simulation results (Sonnet)
[40]	2 mm	Δf= 5 – 40 GHz f_c= 25 GHz	-7.9, -2.9	~75	N/A	• Gain estimated from free-space for 10Ω-cm, 100 Ω-cm substrates, respectively, each w/0.35 mm diamond layer beneath (not in far field)
[41]	2.9 mm	Δf=1-12.4 GHz (VNA) Δf=1-20 GHz (HFSS) f_c= 10 GHz	-27- -21 (measured) -14 - -22 (simulated)	N/A	3-6 %	• bandwidth ~ frequency range in which S_{11} < -10 dB • multiple designs yielded several smaller frequency ranges, bandwidth up to 11.4 GHz • gain estimated from free-space (not in far field
[42]	2 mm	Δf=6-18 GHz, f_c= 12 GHz	-19 (meander)	~150	N/A	• bandwidth not quantified in terms of S_{11} or S_{21} • gain estimated from free-space (not in far field)
[43]	0.45 mm	B_1=14 GHz, f_c= 60 GHz B_2=7 GHz, f_c= 60 GHz	-8 (inverted F) -14 (dipole)	50	9% (inverted-F) 2% (dipole)	• bandwidth ~ frequency range in which S_{11} < -10 dB • inverted-F ~51-65 GHz; dipole ~58-65 GHz
[44]	1 mm × 1 mm	B=120 GHz, f_c= 800 GHz	8.25 at 852 GHz	matched with feed	88.3 % at 852 GHz	• bandwidth ~ frequency range in which S_{11} < -10 dB • resonates at 693.45, 797.4, and 852 GHz • size is 2D since patch antenna
[48]	4 mm	B=8.5 GHz (dipole pair) B=25 GHz (phased array) f_c= 16 GHz (dipole pair) f_c= 22 GHz (phased array)	-11.51 (phased array) -21.6 (aligned dipole pair) -32.2 (opp. dipole pair)	N/A	N/A	• bandwidth ~ frequency range in which S_{11} <-10 dB • dipole pair 14.5-23 GHz, resonating at ~16 GHz, phased array resonating at ~22 GHz • $\lambda/2$ dipole length 4 mm; array of four $\lambda/4$ monopoles arranged in square of side length 2 mm
[49]	0.3 mm	B_{3dB}=16 GHz, f_c= 62.5 GHz	3.9	N/A	N/A	• Center frequency 62.5 GHz • 16 GHz 3dB bandwidth from S_{21}
[50]	1.4 x 0.9 mm 1.2 x 0.6 mm 0.6 x 2 mm 0.7 x 0.7 mm	B_{3dB}=72-120 GHz, f_c= 90 GHz B= 5 GHz, B_{3dB}=20 GHz, f_c= 140 GHz B_{3dB}= 3 GHz, f_c=140 GHz B=10 GHz, f_c= 140 GHz	-1.5 -1.4 -1 -2	N/A 50 50 50	N/A N/A N/A N/A	• bandwidth is 3dB gain bandwidth; peak at 90 GHz • bandwidth ~ frequency range in which S_{11} <-10 dB, resonating at 140 GHz; B_{3dB}=136-156 GHz • peak gain at 140 GHz • bandwidth ~ frequency range in which S_{11} <-10 dB, from 138 GHz to 148 GHz, and resonating at 141 GHz and 146 GHz
[51]	2 x 2.3 mm	B=50-85 GHz for horizontal case, B=60-65 GHz and B=75-85 GHz for vertical case f_c= 60 GHz	-3("H" & 60 GHz) 3.5 ("V" & 60 GHz) -2.1 ("H" & 77 GHz) 4.8 ("V" & 77 GHz)	N/A	N/A	• bandwidth ~ frequency range in which S_{11} <-10 dB • "H" denotes horizontal position and "V" vertical polarization

2.5 Gaps in the WiNoC Literature

Most of the papers in the literature focus on antennas, as mentioned earlier in the remarks, operating in the microwave and low-millimeter wave range. In order to deliver the high throughput and data rates required by WiNoC's, antennas should be operating at much higher frequencies in order to benefit from the higher bandwidth available in that part of the spectrum. It is understandable that the technology to fabricate such structures is still immature and if even possible, it would be very expensive. Also, the fabrication of RF components, such as oscillators and amplifiers, operating at such high frequencies, remains very challenging.

As for WiNoC wireless channel modeling, the vast majority of papers found in the literature use very simplistic models—mostly the free space model. This is a gross simplification since the WiNoC landscape is complex, with different layers of substrates and metals that the electromagnetic waves, travelling between transmitting and receiving antennas, interact with. Therefore, more precise models are imperative in order to better estimate attenuation, dispersion, and consequent error rates in the WiNoC environment.

Chapter 3

Simulation Description

3.1 Introduction

Computer techniques have revolutionized the way electromagnetic (EM) problems are analyzed. Radio Frequency (RF) and microwave engineers rely heavily on computer simulations to analyze and help evaluate new designs or design specifications. Although most EM problems consist of solving a set of partial differential equations subject to specific boundary conditions, very few practical problems can be solved without the aid of a computer or cluster of machines.

Computer methods for analyzing problems in electromagnetics generally are divided into two categories --analytical techniques or numerical techniques. Analytical techniques make simplifying assumptions about the geometry of a problem in order to apply a closed-form or tabulated solution. Numerical techniques attempt to solve fundamental field equations directly, subject to the boundary conditions set by the geometry.

Numerical techniques generally require more computation than analytical techniques, but they are very powerful EM analysis tools. Without making assumptions about which field interactions are most significant, numerical techniques analyze the entire geometry provided as input. They calculate the solution to a problem based on a full-wave analysis.

For our simulations and designs we use the 3-Dimensional full wave EM solver High Frequency Structure Simulator (HFSS®) from Ansys. In what follows, we present a description of the numerical methods HFSS uses, discuss the advantages and disadvantages of each method, and finally show example results for a monopole antenna including its return loss and radiation pattern.

3.2 Finite Element Method

Engineers from different disciplines have used finite element methods to solve different types of problems. Civil and mechanical engineers use this method to analyze material and structural problems. Electrical engineers, on the other hand, use this numerical method to solve complex problems in magnetism and electrostatics. Only recently has the finite element method started being used to model and solve three dimensional electromagnetic radiation problems. This is due to the fact that three dimensional problems are more complicated and require more computational power than two dimensional or scalar problems. However, an increasing availability of computer resources has resulted in a renewed interest to solve complex electromagnetic problems using the finite element method.

In order to generate an electromagnetic field solution, the first step that HFSS® employs, using the finite element method, consists of dividing the full problem physical space into a large number (typically, thousands) of smaller regions and representing the field in each sub-region (element) with a local function. In HFSS®, the geometric model is divided into a large number of tetrahedra, where a tetrahedron is a 4 sided pyramid. This set of tetrahedra is referred to as the finite element mesh. An example of a finite

element mesh produced by HFSS® is shown in Figure 3.1. This structure consists of a microstrip line above a substrate that in turn lies atop a ground plane.

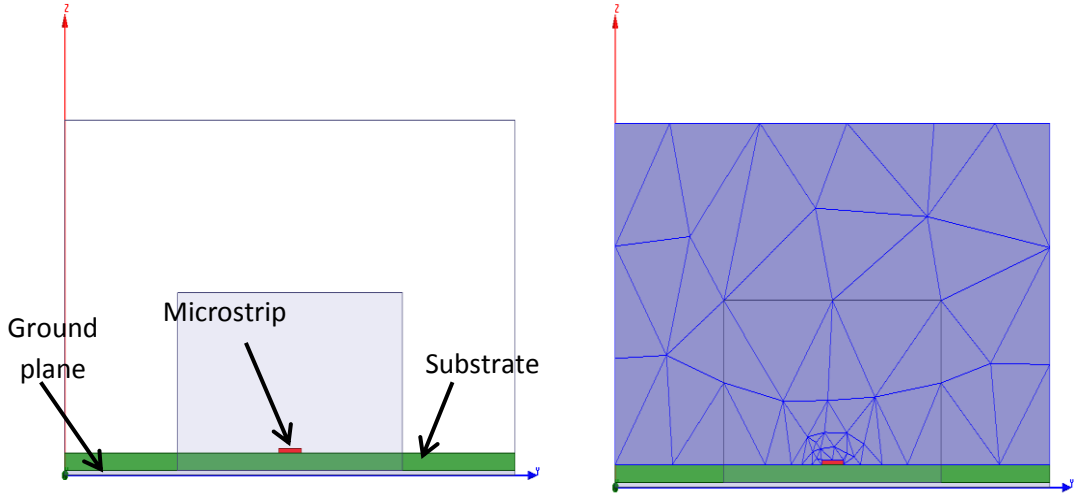


Figure 3.1 Finite Element Mesh Example

The value of a vector field quantity (such as electric or magnetic field), inside each tetrahedron of the mesh, is interpolated from values at the vertices of the tetrahedron. At every vertex, HFSS® stores the components of the field (electric or magnetic field) that are tangential to the three edges of the tetrahedron. Also, HFSS® can store the component of the vector field at the midpoint of selected edges that is tangential to the face and normal to the edge. This is shown in Figure 3.2 [69].

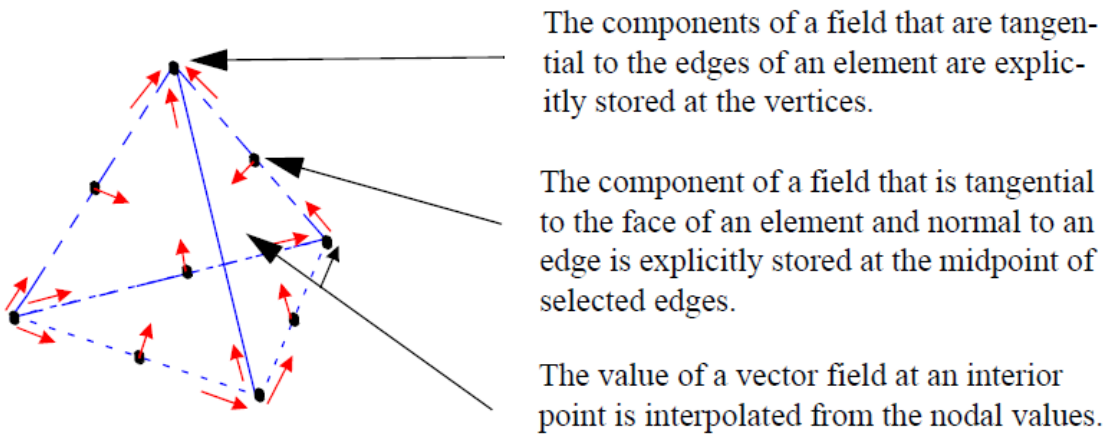


Figure 3.2 Representation of a Field Quantity in HFSS®.

Mathematically, HFSS® solves for the electric field ***E,*** using equation (1) , known as the Helmholtz equation for the time harmonic form of the electric field, subject to excitations and boundary conditions [70].

$$\nabla\times\left(\frac{1}{\mu_r}\nabla\times\boldsymbol{E}\right)-{k_0}^2\varepsilon_r\boldsymbol{E}=\boldsymbol{0} \qquad (1)$$

where $\mu_r=\frac{\mu}{\mu_0}$, $\varepsilon_r=\frac{\varepsilon}{\varepsilon_0}$, ${k_0}^2=\omega^2\varepsilon_0\mu_0=\frac{\omega^2}{c^2}$, where μ, ε, and ω are the permeability , permitivitty, and radian frequency, respectively.

Then HFSS® calculates the magnetic field ***H*** using equation (2), one of Maxwell's equations for a source-free medium.

$$\boldsymbol{H}=\frac{j}{\omega\mu}\nabla\times\boldsymbol{E} \qquad (2)$$

The remaining electromagnetic quantities are derived using constitutive relations. It is important to note that HFSS® utilizes electric and magnetic fields as opposed to more common quantities such as voltages and currents. In practice, HFSS® derives a finite

element matrix using the above two equations. The procedure that HFSS® employs is described in the following sequence of steps.

1. Divide the geometry into a finite element mesh consisting of tetrahedral elements.
2. Define testing functions W_n for each tetrahedron, resulting in thousands of basis functions that are interpolation schemes used to interpolate field values from nodal values.
3. Multiply equation (1) by a W_n and integrate over the whole solution volume yielding

$$\int_V \left(W_n . \nabla \times \left(\frac{1}{\mu_r} \nabla \times \boldsymbol{E} \right) - {k_0}^2 \varepsilon_r W_n . \boldsymbol{E} \right) dV = 0 \qquad (3)$$

This results in thousands of equations for n=1, 2, … , N, where n is the tetrahedron index. Then, using Green's theorem and the divergence theorem, yields

$$\int_V \left((\nabla \times W_n) . \frac{1}{\mu_r} \nabla \times \boldsymbol{E} - {k_0}^2 \varepsilon_r W_n . \boldsymbol{E} \right) dV = \int_S (\text{boundary terms})\, dS, \qquad (3a)$$

for n=1, 2, …, N. Writing $\boldsymbol{E} = \sum_m^N x_m W_n$, n=1, 2 , …, M (4)

where x_m is …, results in (3a) becoming

$$\sum x_m \int_V \left((\nabla \times W_n) . \frac{1}{\mu_r} \nabla \times \boldsymbol{E} - {k_0}^2 \varepsilon_r W_n . \boldsymbol{E} \right) dV = \int_S (\text{boundary terms})\, dS \quad (5)$$

for n=1, 2, …, N

Equation (5) then becomes of the form

$$\sum x_m A_{n,m} = b_n \text{ , } n = 1, 2, \dots, N \qquad (6)$$

Or $Ax = b$ (7)

Equation (7) now is in matrix form and A is a known $N \times N$ matrix that includes any applied boundary condition terms, while b consists of the port excitations. Once x is solved from (7), $\boldsymbol{E}$ would be known. For example, the tangential component of the electric field on the surface of a metal is zero.

The above procedure implies that the solution process used by HFSS® is straightforward and reasonably simple. However, this is not usually the case, and it is very important to note that the field solution process utilized by HFSS® is actually an iterative process. HFSS® uses the above process repeatedly, modifying the mesh in a very specific manner, until the "correct"(satisfying the convergence criterion) field solution is found. This repetitive process is known as the adaptive iterative solution process and is a key to the highly accurate results that HFSS® provides. For example if the "Delta S" option in HFSS® is set to 2 percent, then HFSS® continues to refine the mesh until the magnitude of the complex delta of all S-parameters changes by less than 2 percent, or until the requested number of iterations is completed.

The adaptive solution process is the method by which HFSS® guarantees an accurate answer to a certain electromagnetics problem. It is an essential part of the solution process and a primary reason why a user can have confidence in the highly accurate results that HFSS® generates. In what follows, the steps in the adaptive solution process are outlined [70]:

1. HFSS® generates an initial mesh

2. Using this mesh, the electromagnetic fields, found inside the structure and resulting from exciting the structure at the desired (input) solution frequency, are computed.

Based on the current finite element solution, HFSS® determines the regions of the problem domain where the exact solution exhibits a high degree of error. A pre-defined percentage of tetrahedra in these regions are refined.

2.1 The refinement process consists of creating a number of smaller tetrahedral regions that replace the original larger ones in the high error regions.

2.2 A new solution is generated using the newly refined mesh

2.3 The error is recomputed and the iterative process of solving, determining the error, and refining the mesh gets repeated until the convergence criterion is satisfied.

3. If a frequency sweep is needed, HFSS® solves the problem at the other frequency points without further mesh refinement.

The convergence criterion that we use in HFSS® is maximum “delta S” and it is defined as the change in magnitude of the S-parameters between consecutive iterations [69]. If the S-parameter magnitude and phase vary by less than the maximum delta S value, set by the user during the solution setup, from one iteration to the next, then the adaptive analysis stops. Otherwise, it continues until the criterion is met or the requested number of iterations is completed. An illustration of the adaptive process is shown in Figure 3.3.

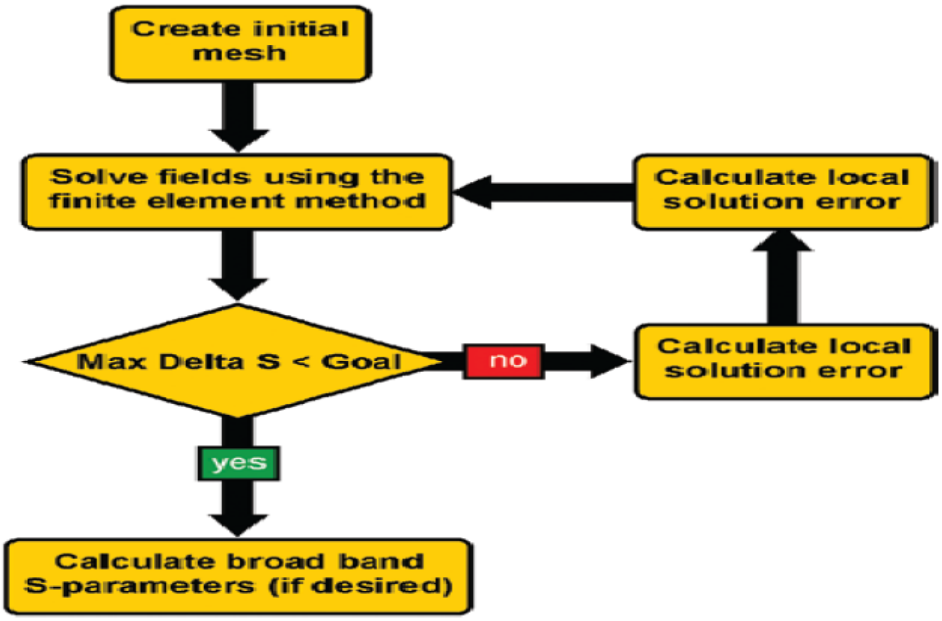


Figure 3.3 Adaptive Solution Process in HFSS®. (Note that the two blocks on the right side are listed as doing the same things—a single block would suffice, but this diagram is what appears in the HFSS documentation.)

3.3 Other Numerical Methods in HFSS®

As discussed previously, the main numerical method HFSS® uses is the finite element method, a frequency domain method, where the whole simulation domain gets discretized into tetrahedral elements and fields inside of these subdivisions are computed to generate a solution for the whole structure. However, the finite element method is not the only numerical method used by HFSS®. HFSS-IE® (Integral Equation), is a full wave integral equation solver that uses the Method of Moments (MoM) to solve for currents on surfaces of objects. This method creates a triangular surface mesh, as opposed to the tetrahedral mesh HFSS® uses, on all objects to solve for currents on conducting and dielectric objects. This solver is suitable for open model simulations, ones that allow electromagnetic energy to radiate away, such as Radar Cross Section (RCS) applications,

stand-alone antennas, and Electromagnetic Compatibility (EMC) and Electromagnetic Interference (EMI) problems. We have used this solver to verify two known propagation models—Free Space and Two Ray—and we provide the verification process and results in Appendix A. Infinite ground planes are supported in HFSS-IE® and this option was critical in verifying the two-ray model where we placed two dipole antennas over an infinite ground plane. The results generated were in excellent agreement with theory.

Physical optics is another method used by HFSS® to provide quick performance estimates of certain electrically large problems when a full wave solution is beyond the computation resources. Electrically large refers to when the physical size of the structures being simulated is very large compared to the wavelength corresponding to the center frequency of operation. In this method, a radiation source is used to illuminate the model, inducing currents that in turn reradiate. Currents are approximated in illuminated regions and set to zero in (optical) shadow regions. Illuminated regions are ones that are exposed to the incident wave whereas shadow regions are ones where there is a blockage of the wave due to the structure and the direction of propagation. This asymptotic method is very useful when solving very large electromagnetic radiation and scattering problems such as large reflector antenna simulations and radar cross sections (RCS) of large objects like ships and aircraft. We show in Table 3.1 a comparison between three major numerical methods used in solving electromagnetic problems [71].

Table 3.1. Comparison of Different Numerical Methods used by HFSS®.

	Method of Moments (MoM)	**Finite Element Method (FEM)**	**Finite Difference Time Domain (FDTD)**
Discretization	Only wires or surfaces	Entire Domain (tetrahedron)	Entire Domain (Cube)
Solution Method	Frequency Domain, linear equations, full matrix	Frequency Domain, linear equations, sparse matrix	Time Domain, iterations
Boundary Conditions	No need for boundary conditions	Absorbing boundary conditions	Absorbing boundary conditions
Numerical Effort	$\sim N^3$	$\sim N^2$	$\sim N$

In summary, numerical methods form the base of electromagnetic simulators that allow engineers to solve real world electromagnetic problems with high levels of accuracy. However, understanding electromagnetic phenomena and having a strong knowledge of radio engineering are essential to generating meaningful and reasonable results from such simulators. Also, being knowledgeable about the underlying numerical method is essential in determining the accuracy, performance and limitations of electromagnetic simulators that are used in microwave, digital high speed, mixed signal design, and signal integrity applications.

3.4 Example Results from HFSS®

In this section, we provide example results, generated by HFSS®, of a monopole antenna operating at center frequency of 150 GHz with a ground plane. Table 3.2 provides the dimensions of this problem. There is teflon between the inner and outer conductors. The HFSS® interface and project tree, return loss of the monopole, and radiation pattern in the elevation and azimuth planes are shown in Figures 3.4 through 3.6 respectively.

Table 3.2. Monopole dimensions

Parameter	**Dimension (mm)**
Monopole length	0.46
Coax Inner Diameter	0.02
Coax Outer Diameter	0.05

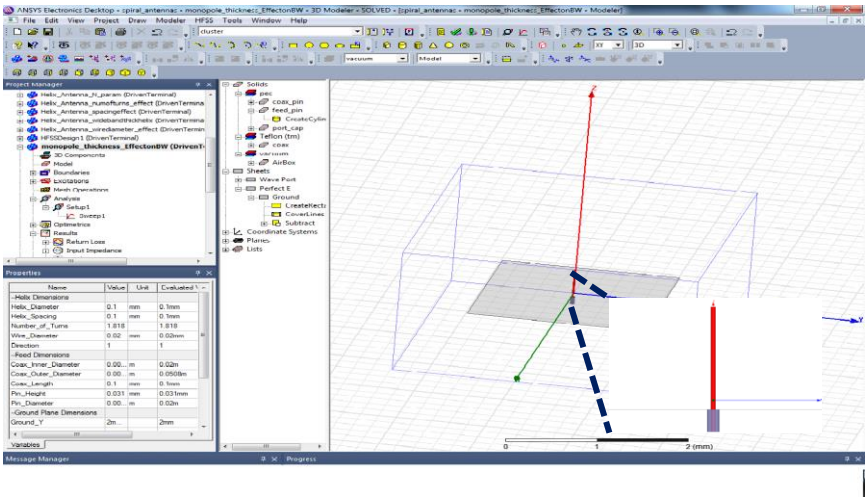


Figure 3.4 HFSS® interface with inset showing a “zoom in” of the monopole.

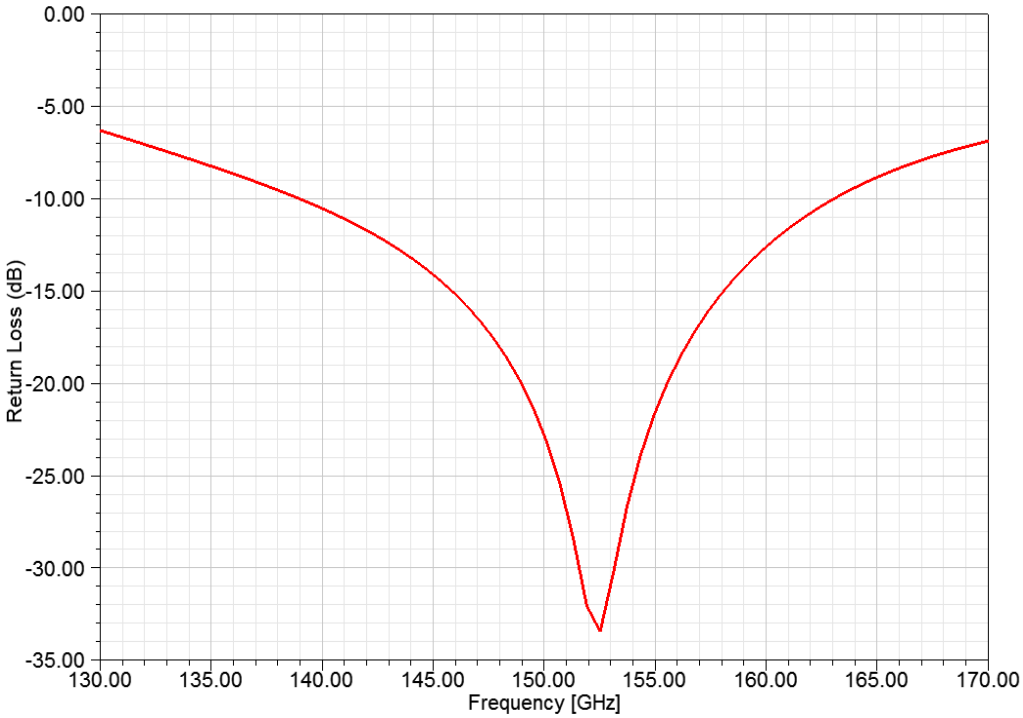


Figure 3.5 Return loss of HFSS® example design monopole.

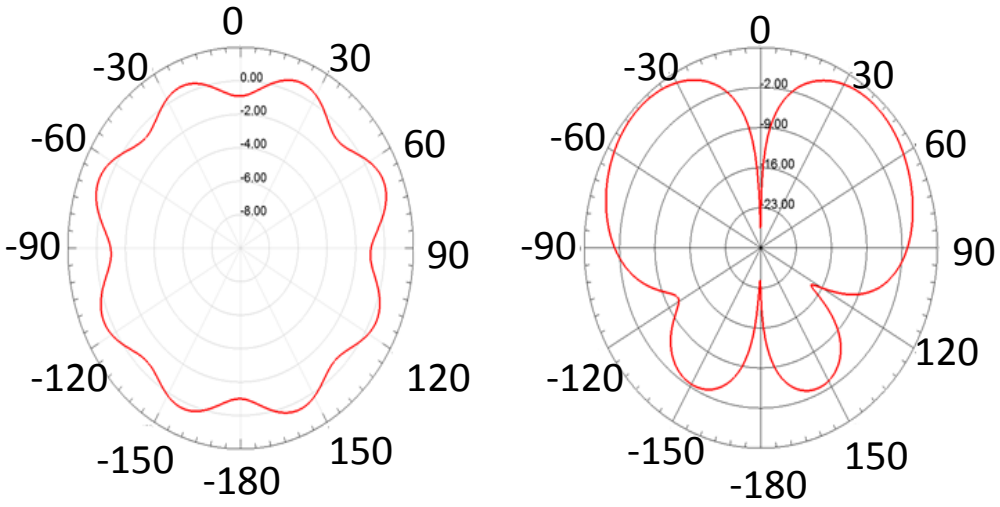


Figure 3.6 Azimuth (left) and Elevation(right) plane radiation pattern

The results agree with theory considering that the ground plane is small and finite.

Chapter 4

Monopole and Dipole Model Results

4.1 Introduction

In this chapter, we present the first two types of antennas simulated in HFSS® inside the WiNoC environment—quarter wavelength monopoles and printed dipoles. We present results on the antenna themselves, such as return loss and radiation pattern, in addition results for the wireless channels the communication signals must traverse, in terms of insertion losses and dispersion measures. We also present results for the throughput of frequency division multiple access schemes based upon the wireless channel characteristics.

4.2 Monopole Antenna Model and Results

In this model, we have conducted full-wave simulations in HFSS®. Here we describe the design, and show its performance in terms of impedance match, overall channel path loss (which incorporates antenna gains), and wireless channel dispersion, which can limit usable bandwidth[2]. This design employs a center frequency of 150 GHz, and we considered performance over a total frequency span of 40 GHz. This design that we consider here consists of upright quarter-wavelength monopoles. The design is enclosed in a ceramic casing, and there is a ground plane beneath the polyimide substrate slab. A depiction of the design is shown in Figure 4.1.

[2] We first assess this "usable bandwidth" assuming no equalization at the receiver, then discuss potential equalization schemes.

The design is for a chip of size 20 mm by 20 mm, with four antennas—one at each corner. The distance between monopoles is 16 mm for the side-to-side pairs, and $16\sqrt{2} \approx 22.63$ mm for the diagonal pairs. The dielectric slab atop the ground plane is polyimide with relative dielectric constant ε_r=3.5. We have used a ceramic casing for thermal reasons, and also because a metal casing would induce stronger and more reflections, causing more severe multipath distortion; polyimide was used because it is a common dielectric for these applications.

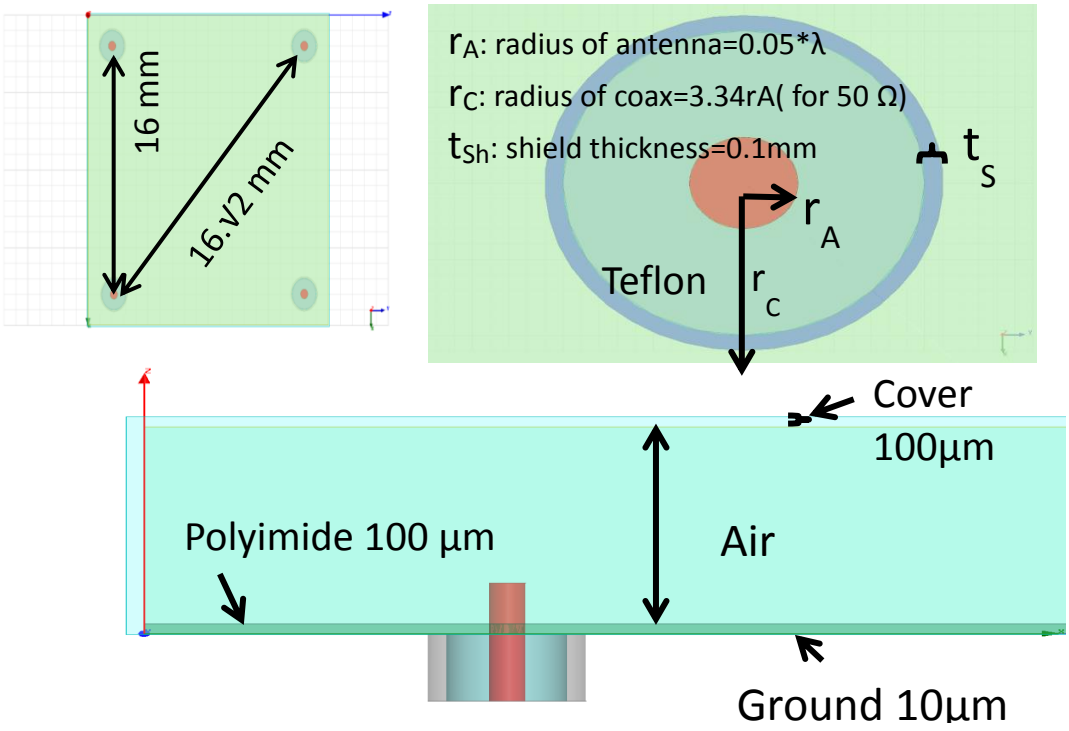


Figure 4.1. Monopole model. Bottom left: cross-section; upper left: top view showing monopoles near corners of chip; and, upper right: close-up top view of quarter wave monopole.

For this design, the impedance matching is quantified by the scattering parameter S_{ii}, for i=1, 2, 3, 4 for our four antenna design. The S_{ii} values are lower than -13 dB for the full frequency range of 130-170 GHz as seen from Figure 4.2.

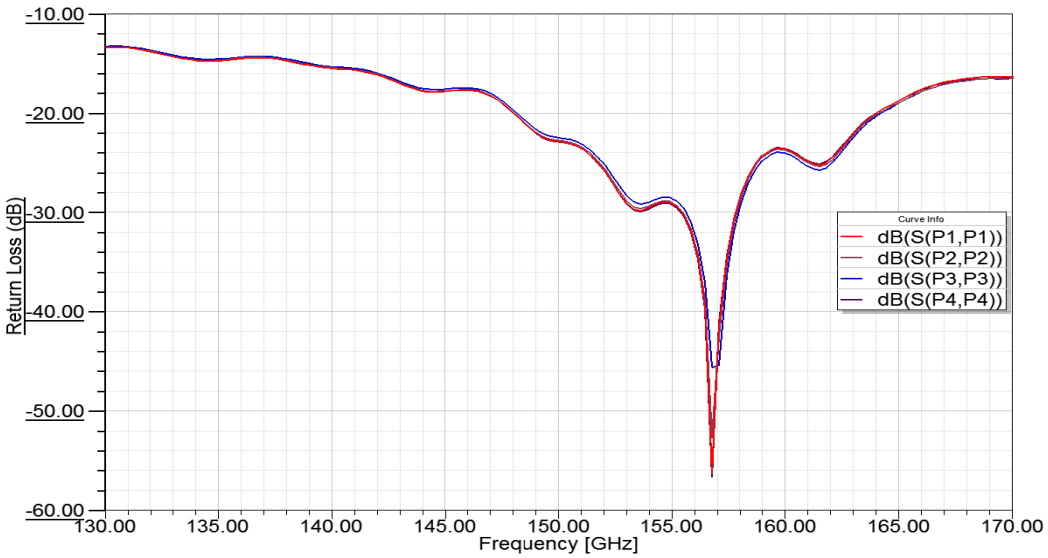


Figure 4.2. Return loss for the monopole design in dB (*S(Pi,Pi)* is $20log_{10}(S_{ii})$, i=1,2, 3, 4.

We show in Figure 4.3 the channel attenuation vs. frequency for the monopole design. Note that insertion loss is positive but we plot the reciprocal of this quantity. Here the side-to-side channel results are denoted S_{21}, whereas the diagonal channel results are S_{31}. If we define bandwidth as the range of frequencies where $\Delta|S_{i1}|$<2 dB[3] for i=2, 3, we can observe that for the side-to-side monopole channel, the maximum single-channel bandwidth available is 8 GHz (158-165 GHz), whereas for the diagonal channels the maximum single-channel bandwidth is 18 GHz (148-166 GHz).

[3] The 2 dB threshold is our approximate value for a "non-distoring" channel; additional values can be used depending upon requirements.

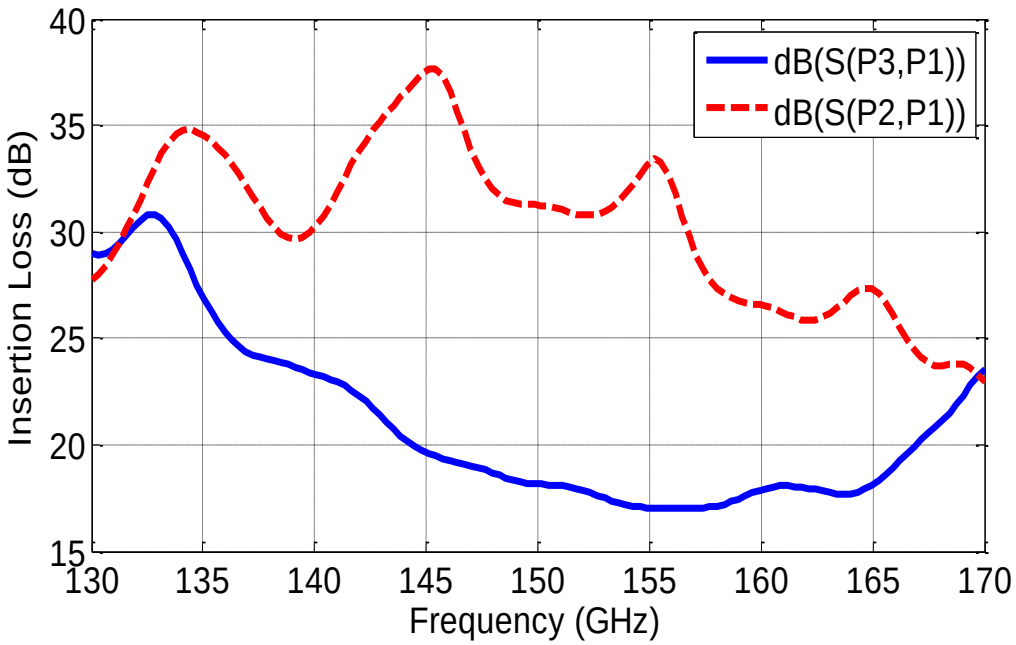


Figure 4.3. Insertion Loss for the monopole design in dB (*S(Pi,Pj)* is $20log_{10}(S_{ij})$, i=2, 3, j=1.

Figure 4.4 shows the unequalized (original) channel impulse responses in terms of power delay profiles (PDPs) for the side and diagonal channels between 150 and 160 GHz. The measure of dispersion we use is the root-mean square delay spread (RMS-DS) [72], the reciprocal of which is a rough measure of usable bandwidth. From this figure, the worst (largest) RMS-DS pertains to the side-to-side channel, in agreement with what we expect from the results in Figure 4.3, where the side-to-side channel's response shows larger variation in insertion loss than the diagonal channel across that 10 GHz band. We show in Figure 4.5 the elevation radiation pattern and in Figure 4.6 the azimuth radiation pattern of the monopoles at three different frequencies. The different radiation patterns help explain the difference between the side-to-side and diagonal insertion losses at those specific frequencies. The patterns are strongly affected by the environment in which the antennas are placed and also affected by the relative location of the monopoles to the

finite ground plane. The azimuth coordinate ϕ starts at zero and rotates counterclockwise in the xy-plane so a side-to-side channel for the antenna closest to the origin would be at ϕ=0° and ϕ=90° whereas a diagonal channel would be at ϕ=45°

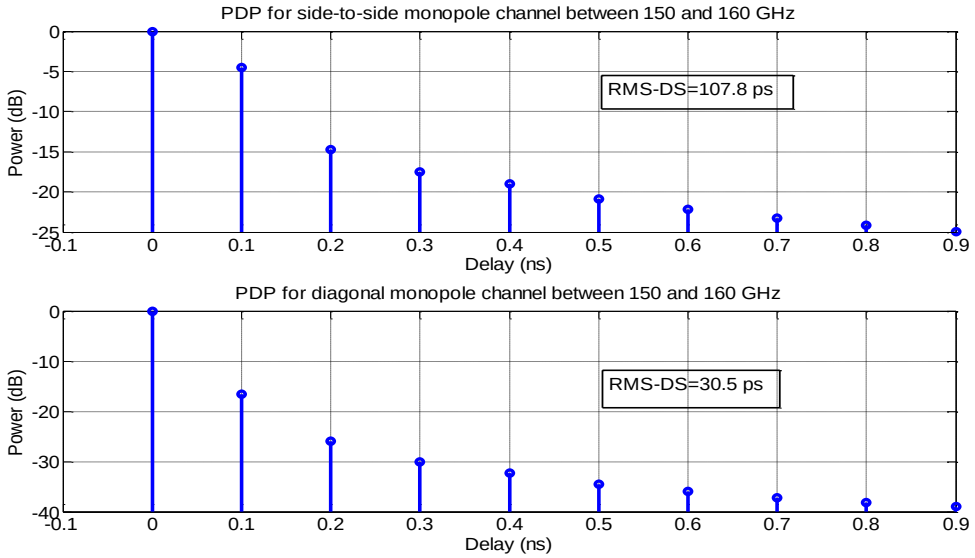


Figure 4.4. Unequalized power delay profiles of monopole channels in specific frequency band 150-160 GHz.

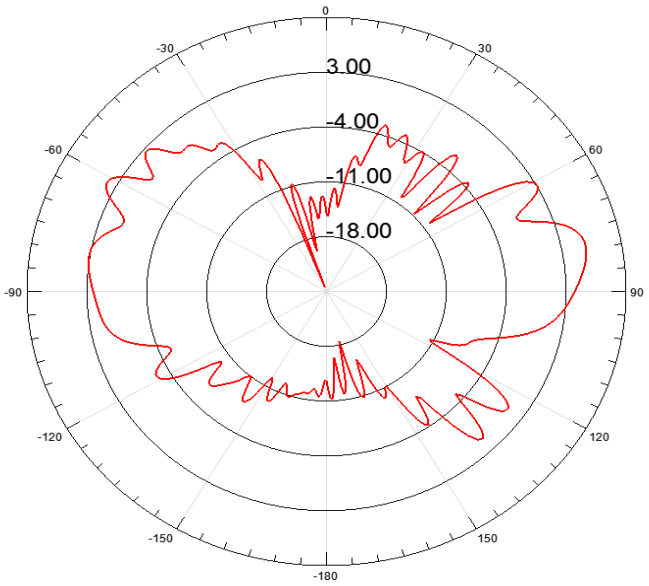


Figure 4.5. Monopole elevation radiation pattern at polar coordinate ϕ=0°.

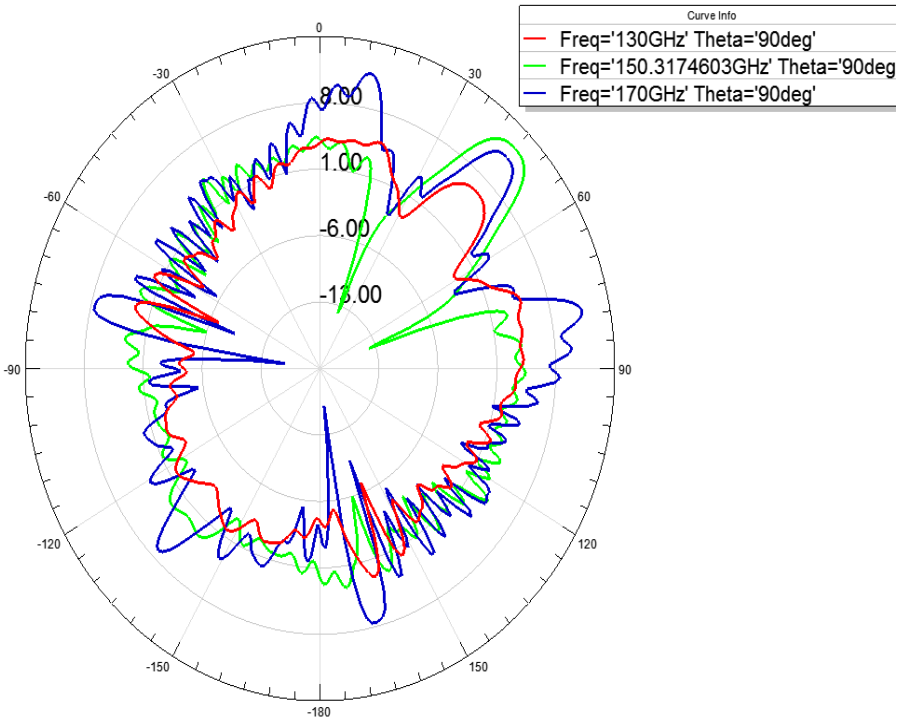


Figure 4.6. Monopole azimuth radiation pattern at polar coordinate θ=90°.

4.3 Example Link Budget

From Figures 4.3 and 4.4, we can deduce that for an example 10 GHz channel, from 150-160 GHz, the diagonal channels incur minimal attenuation and dispersion. From analyses and simulations for binary OOK modulation (Chapter 6), we can estimate that a required signal-to-noise ratio (SNR) for an error probability of 10^{-14} is SNR_{min}=24 dB. This enables us to conduct a link budget analysis to estimate the required transmit power and bit energy.

First, the noise power is given by

$$P_n = -174\ dBm/Hz + 10\log_{10}(BW) + NF\ , \quad (4.1)$$

where BW is the bandwidth and NF is the noise figure in dB. Then the minimum received signal power is computed by

$$P_r = P_n + SNR_{min}. \quad (4.2)$$

Finally, the transmitted power is

$$P_{Tx} = P_r + IL \quad (4.3)$$

where IL is the channel insertion loss. The corresponding bit energies at the transmitter and receiver are then computed as

$$E_{b,r} = p_r/R_b \ , \quad (4.4)$$

$$E_{b,t} = p_t/R_b \ , \quad (4.5)$$

where p_r and p_t are powers in watts, and R_b is the bit rate in bits per second (bps).

As an example, if NF= 10 dB and the insertion loss of the 10 GHz channel under consideration from Figure 4.3 is 18 dB, solving (4.1)-(4.5) yields $E_{b,t} = 6.3\times10^{-16}$ Joules, p_t = 6.3 μW, $E_{b,r} = 10^{-17}$ Joules, and p_r =0.1 μW. For WiNoC systems to be competitive with wired links, we target an energy expenditure of 1 pJ/bit for our designs. The values for our transmitted and received bit energies for our "near best case channel" are well below this level. For the maximum value of IL (our "near worst case" channel in Figure 4.3), attenuation is nearly 30 dB larger, which would yield $E_{b,t} = 6.3\times10^{-13}$ Joules, p_t = 6.3 mW, $E_{b,r} = 10^{-14}$ Joules, and p_r =0.1 mW. The 1 pJ/bit target pertains to the energy required for the entire transmission and reception, which includes energy expenditures by all the transceiver devices. The design of the transceiver elements, which includes the power amplifier, local oscillator, and switch at the transmitter, and a low noise amplifier and (passive) envelope detector at the receiver, were done by our other collaborators on the WiNoC team. This example does though illustrate that with our designs, we can operate links that should reach the 1 pJ/bit goal.

4.4 Printed Dipole Model and Results

We show in Figure 4.7 the printed dipole model. It also consists of four antennas: four half-wavelength printed dipoles—one at each corner of the 20 mm × 20 mm chip. The ground plane, polyimide thickness, and ceramic cover are identical to the ones in the monopole design. The distances between the side-to-side and diagonal antenna pairs are the same as in the monopole design and are measured from the dipole centers. This design also employs a center frequency of 150 GHz, and we consider performance—in terms of impedance mismatch, channel path loss and wireless channel dispersion—over a total frequency span of 40 GHz.

Figure 4.8 shows that the S_{ii} values are lower than -10 dB for the frequency range between 154-156 GHz. This is *much* narrower than the range for the monopole antennas. We show in Figure 4.9 the channel attenuation vs. frequency for the printed dipole design. Still adopting the same designation for the side-to-side and diagonal channels and the same definition of bandwidth, we can observe that for the side-to-side printed dipole channel, the maximum single-channel bandwidth available is 7 GHz (154-161 GHz), whereas for the diagonal channels the maximum single-channel bandwidth is 6 GHz (153-159 GHz). Note the very high insertion loss numbers compared with the monopole design (e.g., ~ 18 to 38 dB for the monopoles, ~50 to 125 dB for the dipoles). It is expected that the printed dipoles perform worse than the monopoles because they do not normally operate parallel to a ground plane and because they radiate broadside, roughly "upward" and not necessarily toward each other.

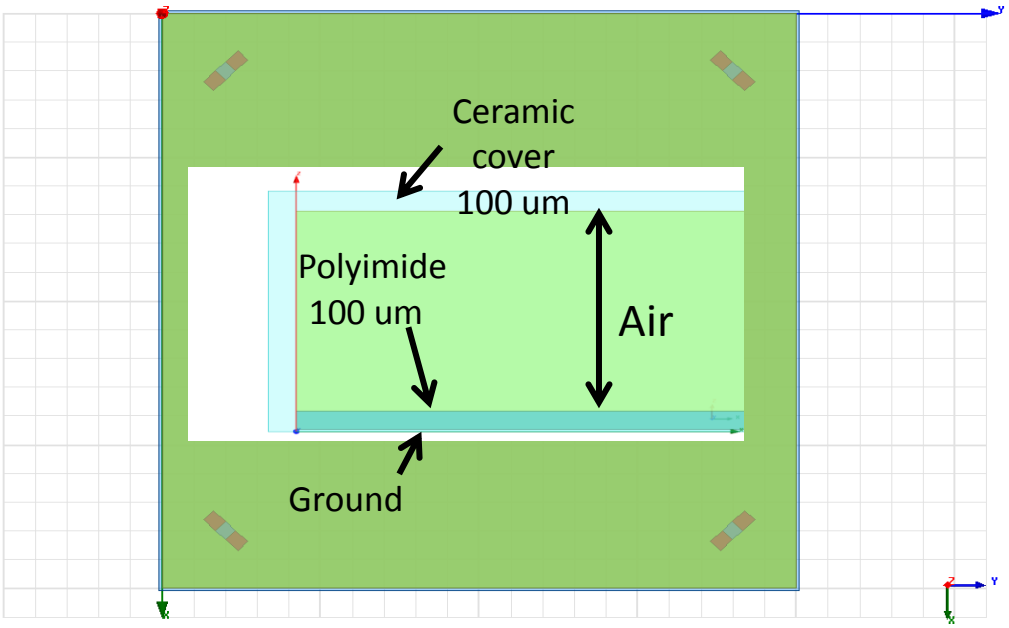


Figure 4.7. Printed dipole model design showing top view and cross section.

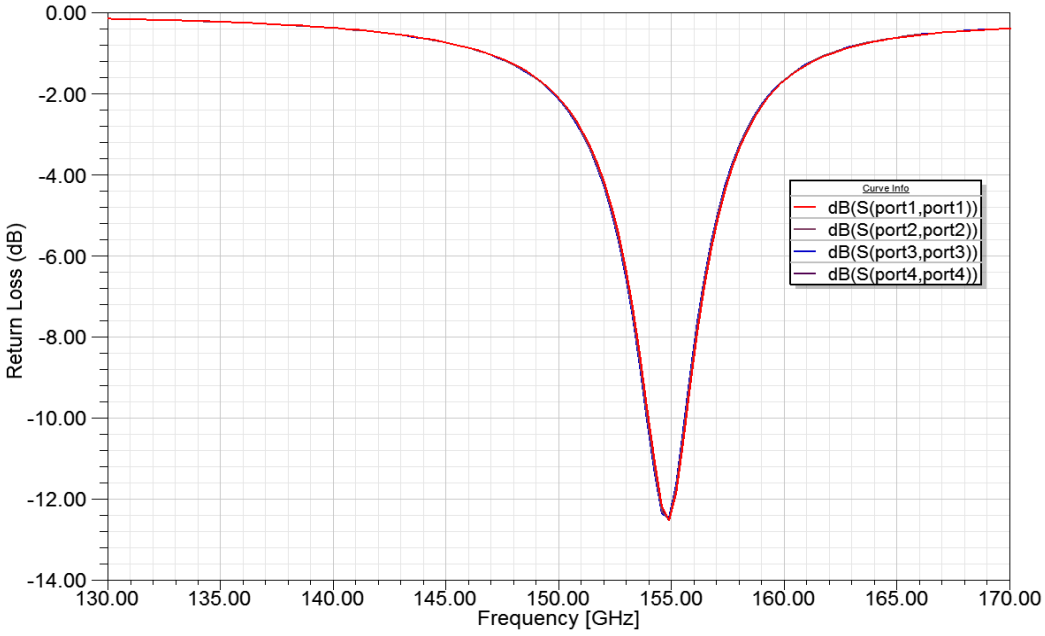


Figure 4.8. Return loss for printed dipole design in dB(*S(Pi,Pi)* is $20log_{10}(S_{ii})$, i=1, 2, 3, 4.

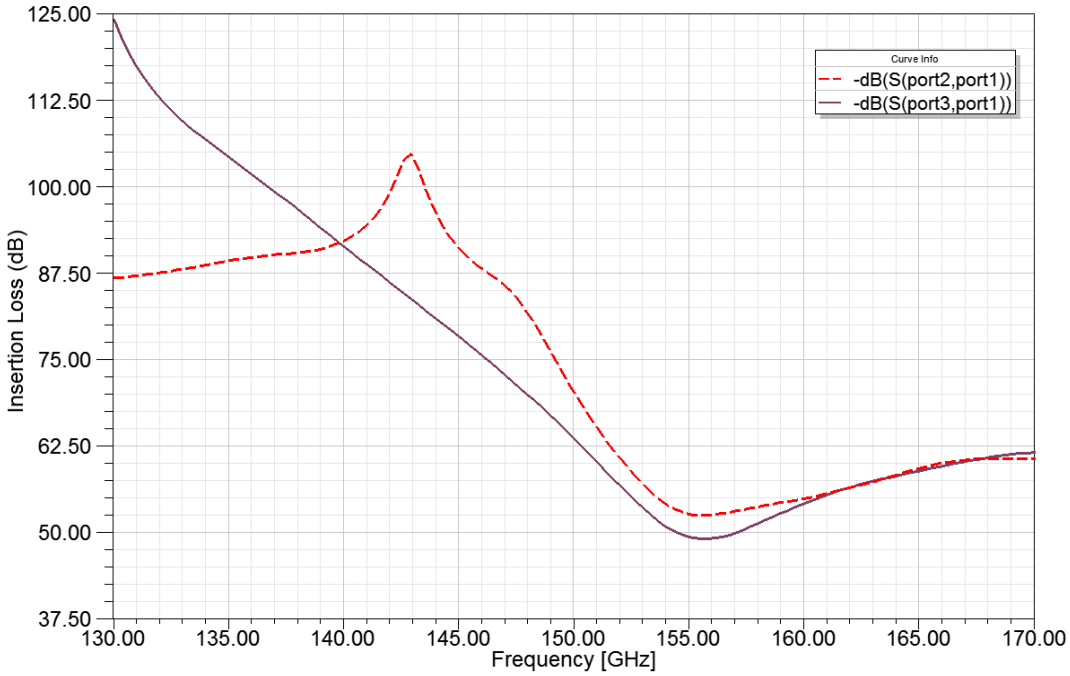


Figure 4.9. Insertion loss for printed dipole design in dB(*S(Pi,Pj)* is $20log_{10}(S_{ij})$, i=2, 3, j=1.

From Figure 4.10, the worst (largest) RMS-DS pertains to the side-to-side channel, in agreement with what we expect from the results in Figure 4.9. Also note the much higher delay spread values in the dipole model compared to the monopole model, which indicates more dispersion and a "richer" multipath environment in the dipole model. Since both the monopole and dipole simulation "landscapes" are the same, the higher dispersion induced by the dipoles comes from their multi lobed radiation pattern in this specific environment. The elevation and azimuth patterns are shown in Figures 4.11 and 4.12 respectively.

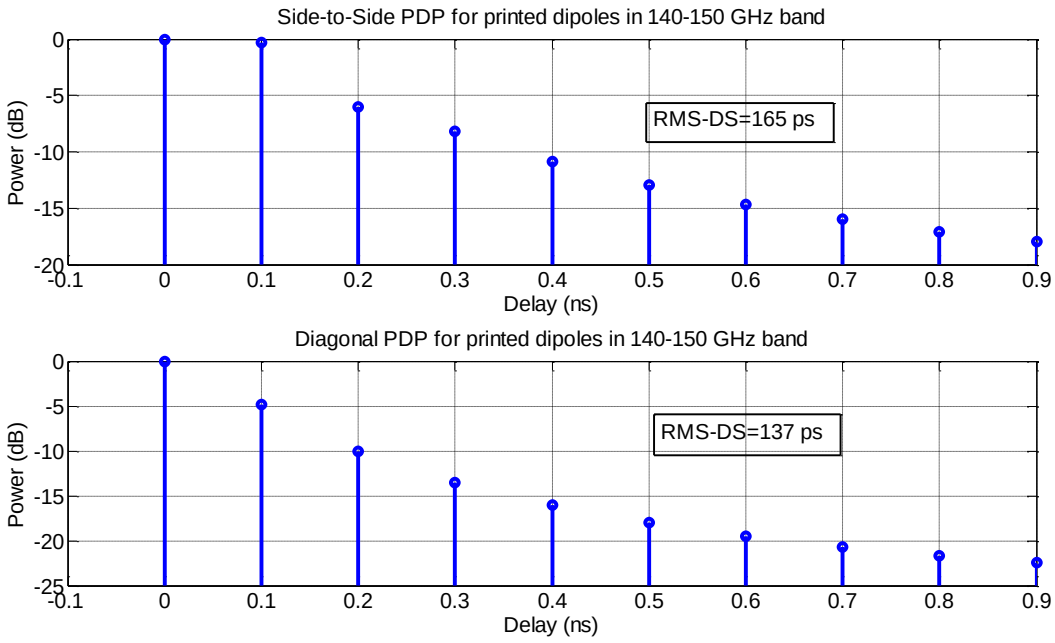


Figure 4.10. Unequalized power delay profiles of printed dipole channels in a specific frequency band.

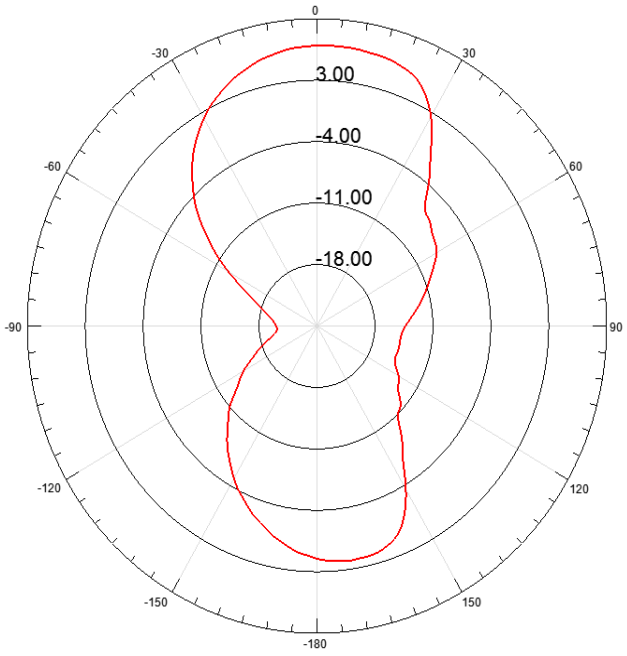


Figure 4.11. Printed dipole with ground plane elevation radiation pattern at polar coordinate ϕ=0°.

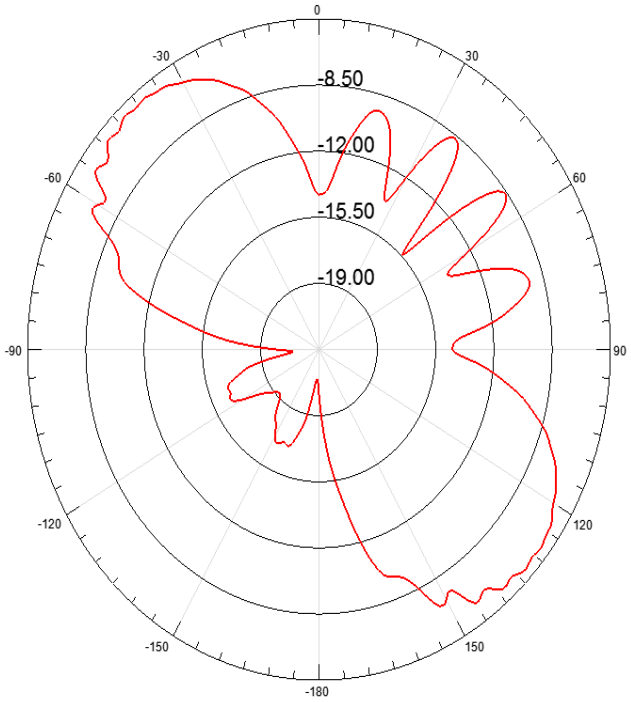


Figure 4.12. Printed dipole with ground plane azimuth radiation pattern at polar coordinate θ=90°.

4.5 Combined Monopole/Dipole Network Results

The design shown in Figure 4.13 again is for a chip of size 20 mm by 20 mm, with five monopole antennas—one at each corner and one in the center—in addition to three printed dipole antennas. Dimensions are in Figure 4.13. The dielectric slab atop the ground plane is also polyimide with a dielectric constant of 3.5, and in addition to the ceramic cover, all have the same dimensions as in the two previous simulation models. For this design, the impedance matching is also quantified by the scattering parameter S_{ii}, for i=1, 2, 3, 4, 5, 1H, 2H, 3H, with the "H" denoting horizontal polarization of the three dipoles. The S_{ii} values are lower than -10 dB for the frequency range of 153-155 GHz and 130-170 GHz for the planar dipoles and monopoles, respectively (again note the relatively very narrow bandwidth of the dipoles).

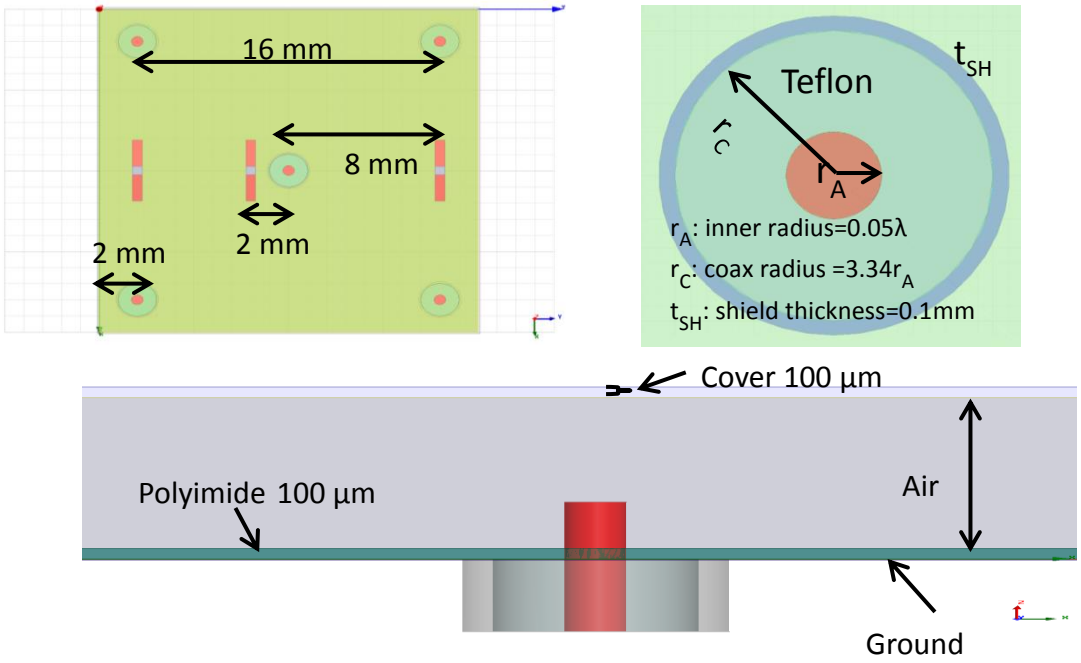


Figure 4.13. Simulation model. Bottom left: cross-section; upper left: top view showing monopoles near corners of chip; and, upper right: close-up top view of quarter wave monopole.

We show in Figure 4.14 the channel attenuation vs. frequency for the two types of antennas in the design. Here the side-to-side monopole channel results are denoted S_{21}, whereas the diagonal monopole channel results are denoted S_{31}. We observe that for the 1H-2H dipole link, the 2H-3H dipole link, and the 1H-3H dipole link, the maximum single-channel bandwidths available are approximately 15 GHz (155-170 GHz), 5 GHz (165-170 GHz), and 6 GHz (157-163 GHz), respectively. For the monopoles, the maximum side-to-side single channel-bandwidth is 10 GHz (150-160 GHz). For the monopole diagonal channels, the maximum available single-channel bandwidth is 20 GHz (145-165 GHz). Excepting the monopole channels, approximately 3 channels of bandwidth on the order of 3 GHz are available for use from the dipoles-only network in a frequency division arrangement. However, the dipole channels exhibit a much higher

insertion loss than the monopole channels. It is also important to note that in order to use the dipole and monopole channels simultaneously, sufficient isolation and filtering is needed so that the channels do not interfere with each other.

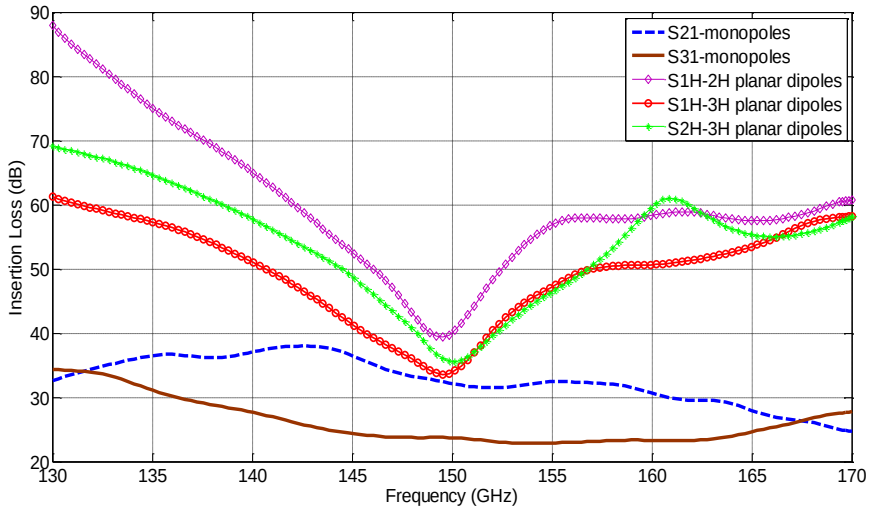


Figure. 4.14. Insertion losses for various antenna pairs in the design of Figure 4.13.

The obvious frequency selectivity of the channels illustrated in Figure 4.14 has led us to evaluate remedial measures, specifically equalization. Since the "ideal" channel is distortionless—having a flat amplitude and linear phase response across the frequency band—equalizers can be used to perform signal processing to transform the response to one closer to the ideal. Equalizers for wired transmissions on long microstrip or striplines on circuit boards can currently run at 10-25 Gb/s [73], [74], and these often consist of transmitter pre-filters as well as decision feedback equalizers (DFEs) at the receiver. Equalizer lengths (# filter coefficients) are presently at least 16 [73].

In Figure 4.15, we show the unequalized (original) channel impulse responses in terms of power delay profiles for the side, diagonal, and center-to-corner channels in

different frequency bands of the monopole design. We still use the root-mean square delay spread (RMS-DS) as a measure of dispersion. From this figure, the worst (largest) RMS-DS pertains to the side-to-side monopole channel between 140 and 150 GHz.

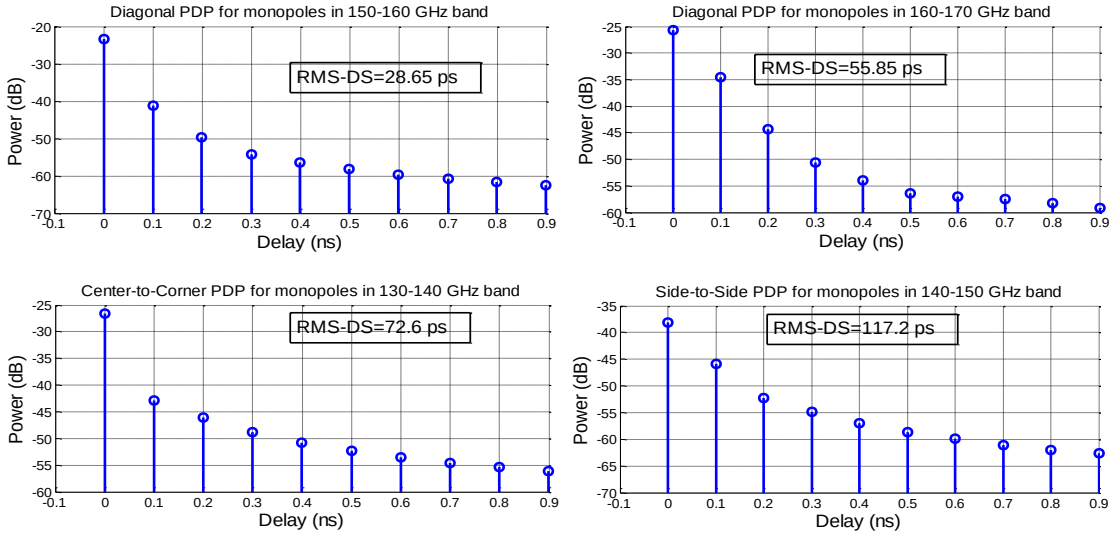


Figure 4.15. Unequalized power delay profiles of monopoles channels in different frequency bands.

It is worth mentioning that there is a very large number of permutations for placing the monopoles and dipoles on the chip. The specific placement, shown in Figure 4.13, was adopted after multiple trial and error steps, and also since it produced "reasonable" insertion losses. Also, it is important to comment on the manufacturability of these antennas. The printed antenna technology is very mature and evolving quickly, and printed dipoles would be easier to manufacture. It would be more challenging to manufacture such small and thin monopoles with sufficient rigidity and uprightness.

4.6 Dipoles without Ground Plane Model Results

In all previous models we simulated the WiNoC environment with a ground plane assuming that the antennas are going to be located at the uppermost layer of the chip.

Thus, in order to avoid radiation towards the lower layers where the transceiver active components are located, we use a metallic reflector for that purpose. However, just like some antennas inherently need a ground plane for proper operation, other antennas such as horizontal dipoles do not. We hence decided to simulate the dipole antennas in the same environment but without the ground plane. We show below in Figure 4.16 and 4.17 the return loss and insertion loss of the dipole antennas in the same environment but in the absence of a ground plane.

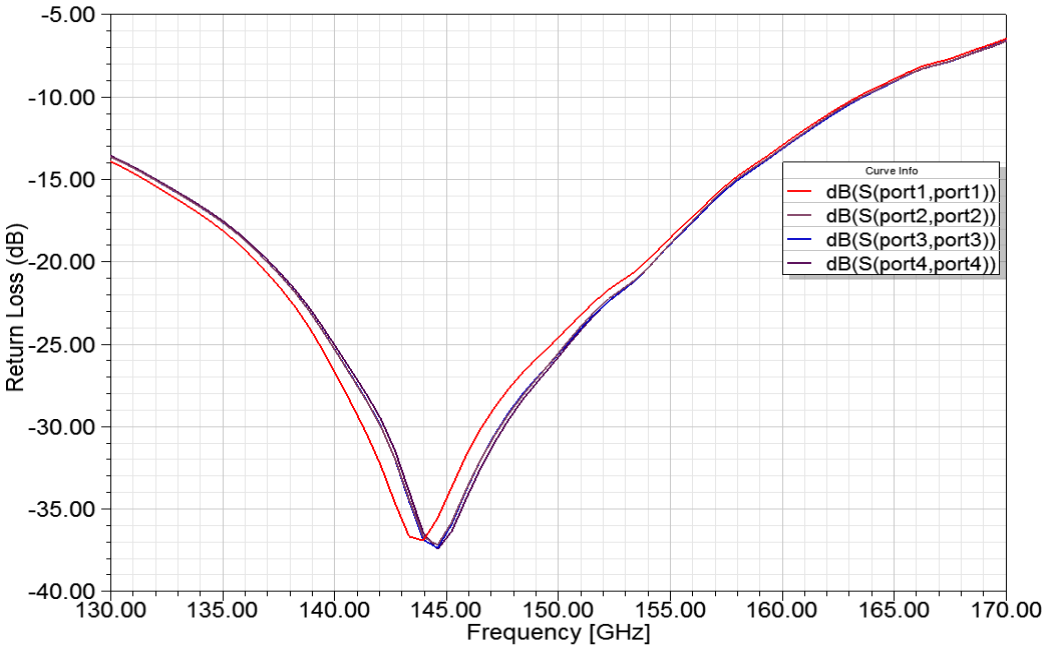


Figure 4.16. Return loss for printed dipole design without a ground plane in dB (*S(Porti,Porti)* is $20log_{10}(S_{ii})$, i=1, 2, 3, 4.

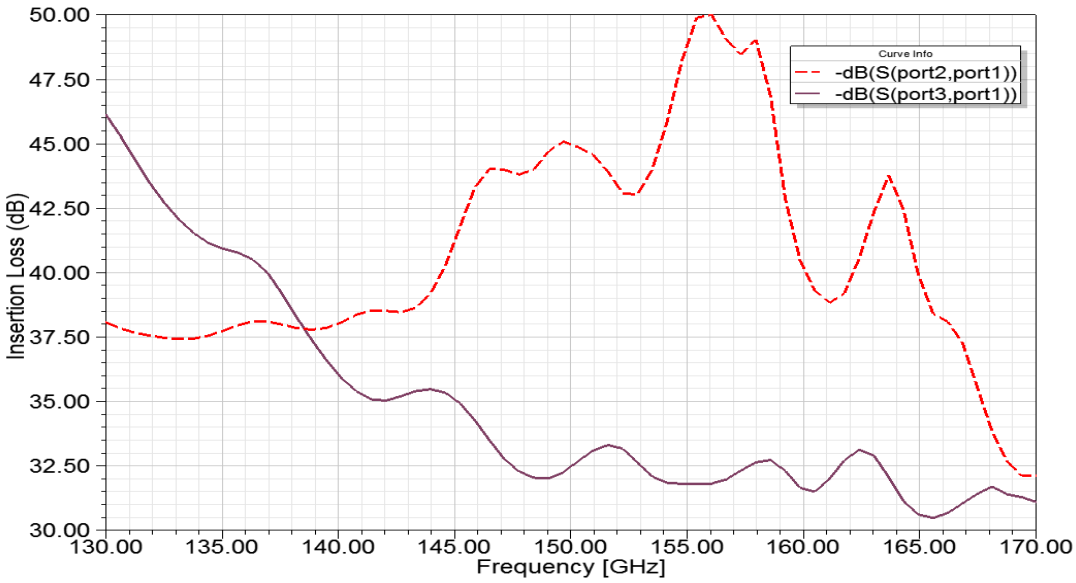


Figure 4.17. Insertion loss for printed dipole design without a ground plane in dB (*S(Porti,Portj)* is $20log_{10}(S_{ij})$, i=2, 3, j=1.

As seen from Figure 4.17, the insertion losses exhibited by the dipole antenna pairs when simulated in an environment without a ground plane are much smaller than those with the ground plane, as expected. For the case without the ground plane, the dipoles insertion loss ranges between 31 dB and 46 dB (compared to 50-125 dB for the case with a ground plane) for the diagonal channels and between 32 dB and 50 dB (compared to 60-104 dB for the case with a ground plane) for the side-to-side channels. The higher insertion losses are likely due to the coupling present due to the proximity of the antennas to the ground plane [51]. When the ground plane is removed, that coupling is no longer present and the antennas perform better. Even though removing the ground plane improves the performance of the printed dipoles, the monopoles are still better.

4.7 Multiple Access

In this section, we present frequency division multiplexing (FDM) schemes for the monopole and dipole models. We also calculate the bandwidth achieveable by each model.

A. Monopole Model

We show in Figure 4.18 the insertion loss for the diagonal and side-to-side links from the monopole model in addition to the maximum channel bandwidth (according to our 2 dB slope criterion) achieved in each of the eight 5 GHz channels that consistute the 40 GHz frequency span. The numbers in black (top) are for the diagonal link whereas the numbers in red (bottom) are for the side-to-side link. We show in Figure 4.19 the calculated bandwidths (~histogram) of each of the 8 channels that span the frequency range of 10 GHz for this case. The S2S, BW, and MaxSCBW abbreviations denote “side-to-side”, “bandwidth”, and “maximum single channel bandwidth,” respectively. We will adopt these abbreviations in addition to the definition of bandwidth used at the beginning of this chapter throughout this section.

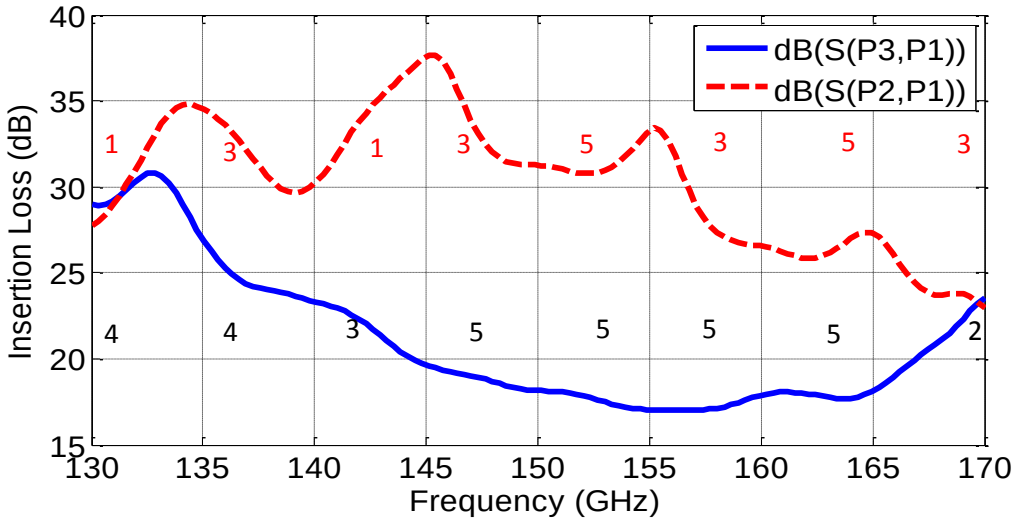


Figure 4.18. Insertion loss for monopole model with channel bandwidths, in GHz.

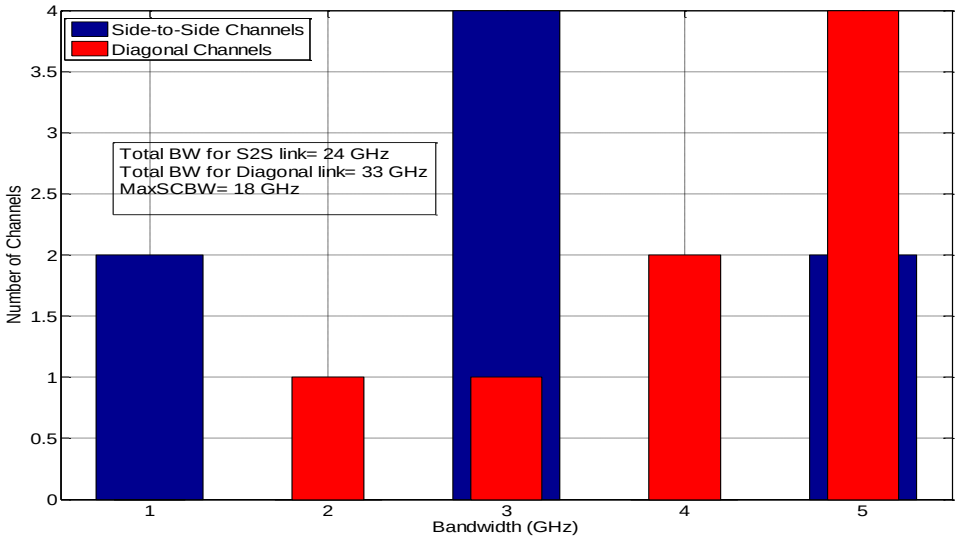


Figure 4.19. Channel bandwidths for monopole design.

The entries “d_S”, “d_D”, and “d_E” in Figure 4.20 stand for the side-to-side separation between the antennas, diagonal separation between the antennas, and the separation of the antenna from the edges of the chip, respectively. The parameter B_{xy}

denotes the bandwidth of the channel between antennas *x* and *y*. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 33 GHz with perfect filtering. This bandwidth is achieved by using a specific transmission/reception scheme represented by the dashed arrows in Figure 4.20. The maximum single channel bandwidth of 18 GHz is achieved from the diagonal link and occurs between 148 GHz and 166 GHz. We show in Table 4.1 the channels that achieve the maximum bandwidth and their frequency spans.

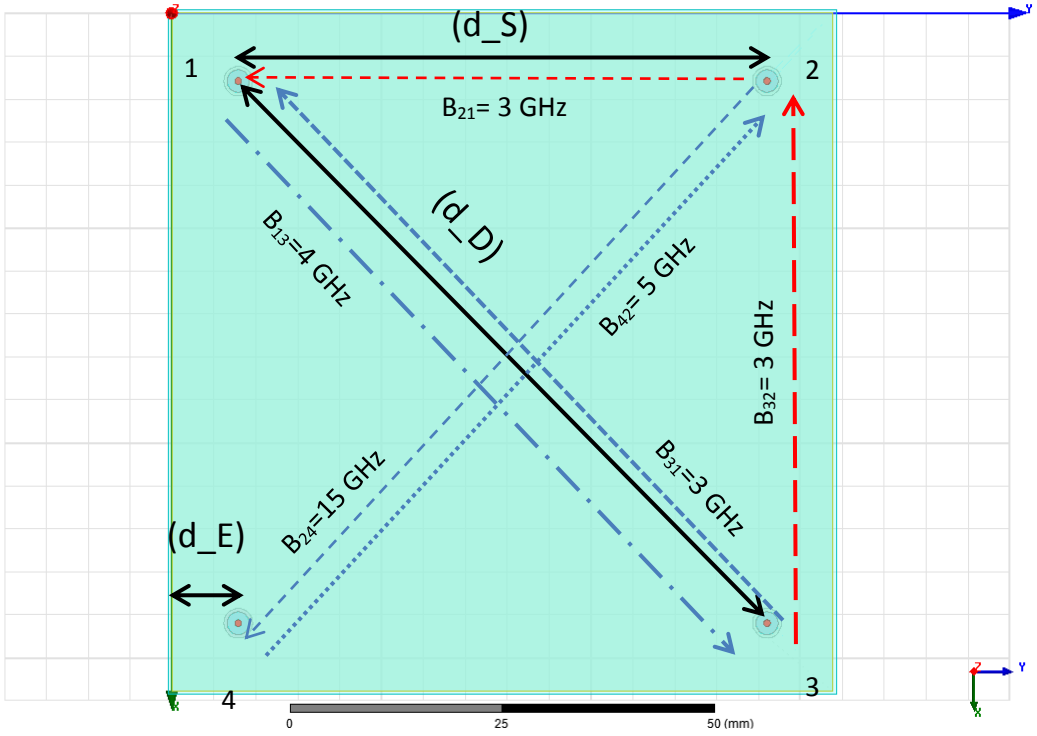


Figure 4.20. Channel assignment for monopole model

Table 4.1. Maximum bandwidth channel allocation for monopole model

Channel	Bandwidth (GHz)	Frequency range (GHz)
C_{13}	4	130-135
C_{32}	3	135-140
C_{31}	3	140-145
C_{42}	5	145-150
C_{24}	15	150-165
C_{21}	3	165-170

B. Printed Dipole Model

We present a similar multiple access scheme analysis for the printed dipole model. Figure 4.21 shows the insertion loss for the diagonal and side-to-side links from the printed dipole model, in addition to the maximum channel bandwidth achieved in each of the eight 5 GHz channels. Again, the numbers in black (top) are for the diagonal link whereas the numbers in red (bottom) are for the side-to-side link. We also adopt all the abbreviations previously mentioned. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 28 GHz with perfect filtering. This bandwidth is achieved by using a specific transmission/reception scheme represented by the dashed arrows in Figure 4.23.

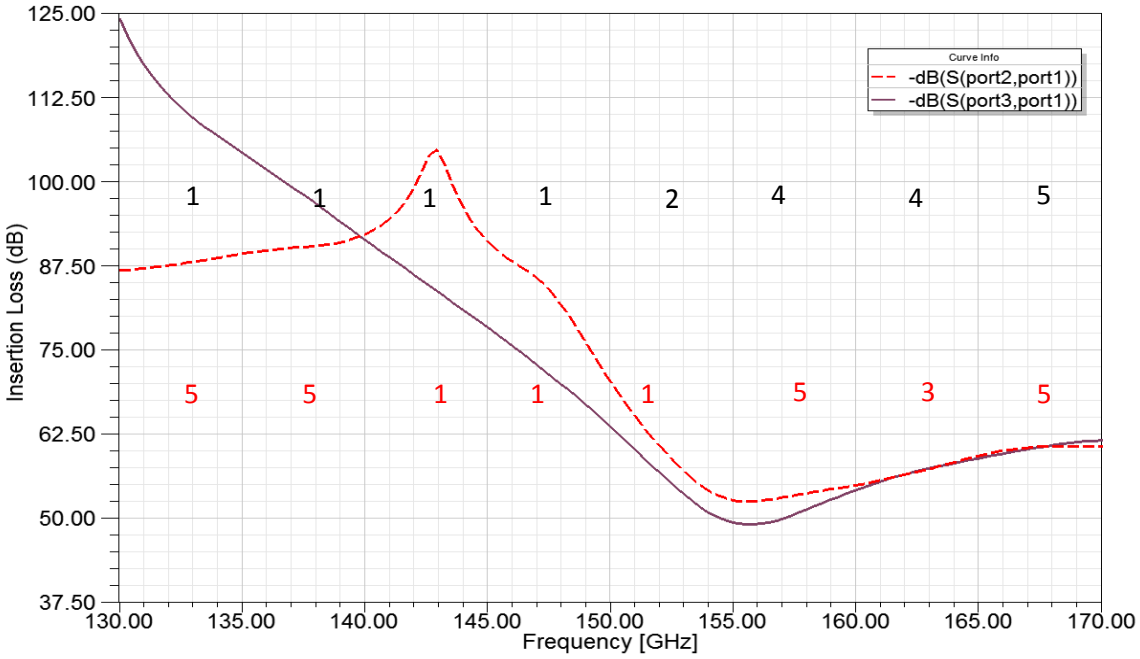


Figure 4.21. Insertion loss for printed dipole model with channel bandwidths.

Figure 4.22 shows the bandwidth allocation (~histogram). The maximum single channel bandwidth of 5 GHz is achieved from either the diagonal or the side-to-side link and occurs between 165 GHz and 170 GHz. The total bandwidth of 28 GHz is achieved by using a specific transmission/reception scheme represented by the dashed arrows in Figure 4.23.

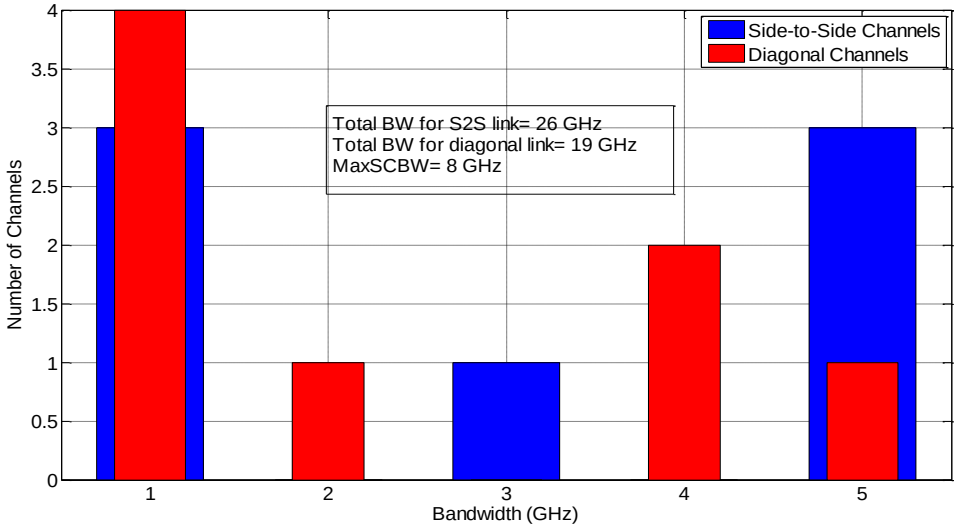


Figure 4.22. Channel bandwidths for printed dipole design.

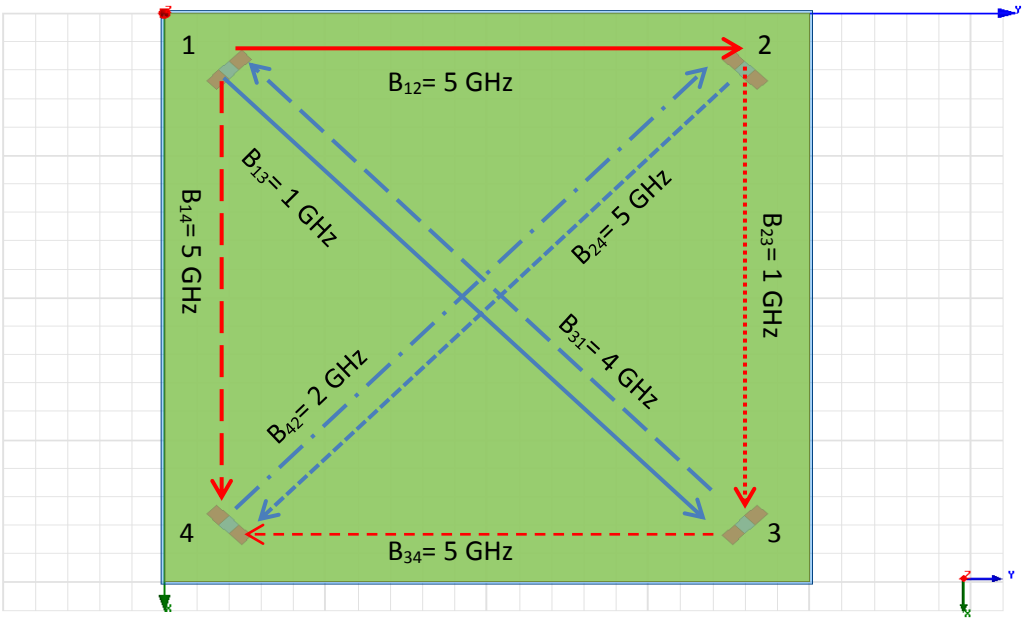


Figure 4.23. Channel assignment for the printed dipole model.

We show in Table 4.2 the channels that achieve the maximum bandwidth with their corresponding bit rates and frequency spans. It should be noted that even though the

total bandwidth from the dipole model is comparable to the one achieved by the monopole model, the channels exhibit a very large insertion loss (~ 90 dB higher in the worst case) and the maximum single channel bandwidth is less than half of that achieved by the monopoles. Also, the printed dipole's best case insertion loss channel occurs at ~51 dB compared to monopole's best case insertion loss channel that occurs at ~18 dB.

Table 4.2. Maximum bandwidth channel allocation for printed dipole model

Channel	**Bandwidth (GHz)**	**Frequency range (GHz)**
C_{12}	5	130-135
C_{34}	5	135-140
C_{13}	1	140-145
C_{23}	1	145-150
C_{42}	2	150-155
C_{14}	5	155-160
C_{31}	4	160-165
C_{24}	5	165-170

Chapter 5

Wideband Antennas

5.1 Introduction

We discussed in the previous chapter the performance of quarter wavelength monopoles and half wavelength printed dipoles in the WiNoC environment. This also enabled us to estimate the channel bandwidths and data rates that can be achieved between different pairs of these antennas. In this chapter, we investigate more inherently wideband antennas and discuss their performance in the WiNoC environment. We consider two types of vertically polarized antennas and two types of printed antennas. Similar to the analysis done in the previous chapter, we present results on the antennas themselves, including return loss and radiation pattern, in addition to results for insertion losses and dispersion of the wireless channels. We also present results for the throughput of frequency division multiple access schemes based upon the wireless channel characteristics.

5.2 Helical Antenna Model

As in the previous chapter, we also have conducted full-wave simulations in HFSS. In this section, we describe the design and show its performance in terms of impedance match, insertion loss, and channel dispersion, in addition to showing the antenna radiation patterns. This design employs a center frequency of 150 GHz, and we

Parameter	Dimension (mm)
Helix Diameter	0.1
Helix Spacing	0.112
Feed Pin Height	0.0785
Wire Diameter	0.095

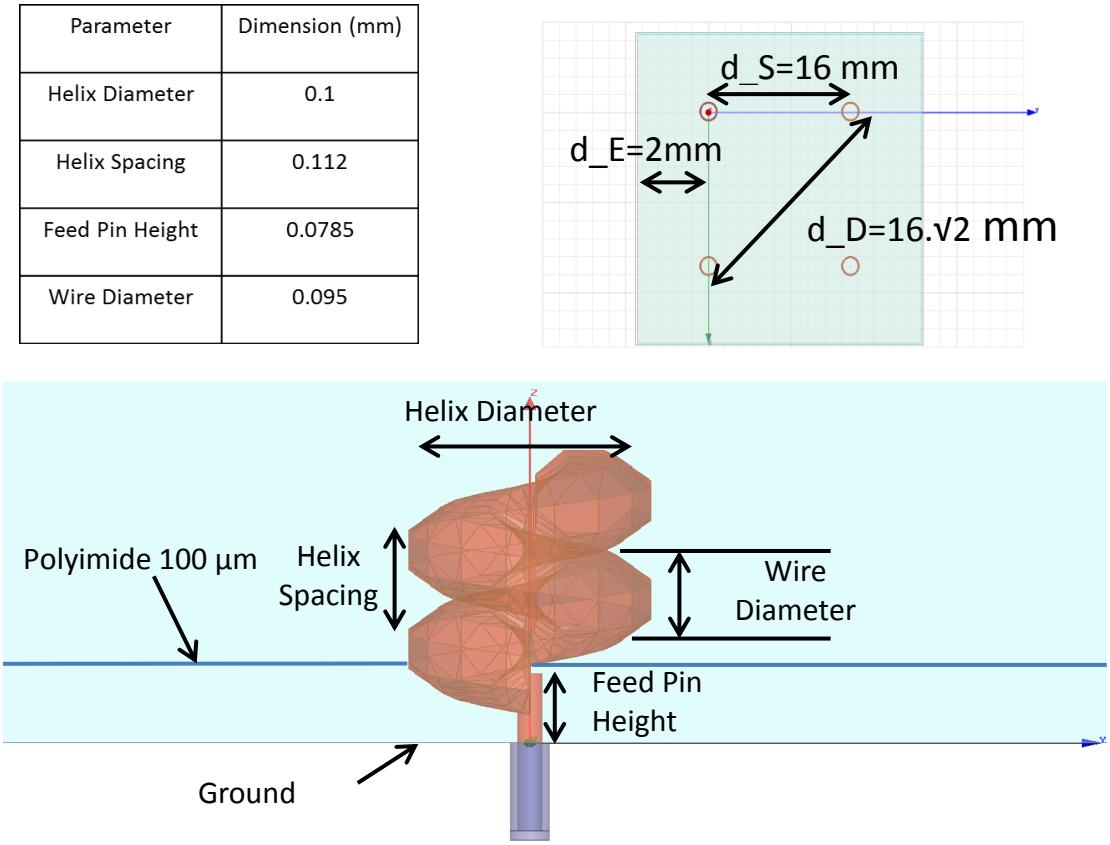


Figure 5.1. Helix model. Bottom: cross-section; upper left: dimensions of various parameters of the helix; and, upper right: top view showing helixes near corners of chip.

considered performance over a total frequency span of 40 GHz. This design that we consider here consists of normal mode helical antennas. The design is enclosed in a ceramic casing, and there is a ground plane beneath the polyimide substrate slab. A depiction of the design is shown in Figure 5.1.The design is for a chip of size 20 mm by 20 mm, with four antennas—one at each corner. The entries “d_S”, “d_D”, and “d_E” in Figure 5.1 stand for the side-to-side separation between the antennas, diagonal separation between the antennas, and the separation of the antenna from the edges of the chip, respectively. The dielectric layer above the ground plane is polyimide with relative dielectric constant ε_r=3.5. We again use a ceramic material for the cover for thermal

reasons and also to reduce the severe multipath distortion that would result if a reflective metallic cover were used. The *Sii* values are lower than -10 dB for the frequency range between 135-170 GHz, as seen in Figure 5.2. This shows the inherent wideband property of the helical antennas.

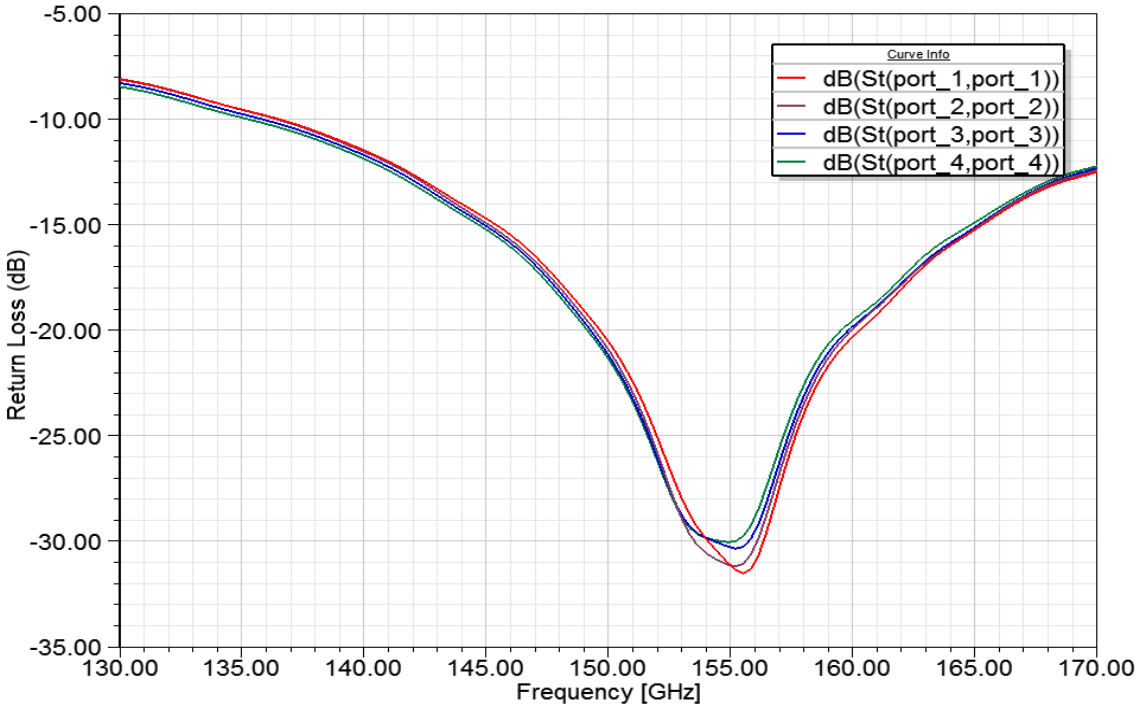


Figure 5.2. Return loss for helical antenna design in dB (*St(Port_i,Port_i)*) is $20log_{10}(S_{ii})$, i=1, 2, 3, 4.

We show in Figure 5.3 the channel attenuation vs. frequency for the helical antenna design. Still adopting the same designation for the side-to-side and diagonal channels and the same definition of bandwidth from the previous chapter, we can observe that for the side-to-side helix channel, the maximum single-channel bandwidth available is 10 GHz (132-142 GHz), whereas for the diagonal channels the maximum single-channel bandwidth is 21 GHz (145-166 GHz). These single channel bandwidths are the

highest we have obtained so far among all the different models we have considered in the previous chapter, although at a higher insertion loss (~ 15 dB).

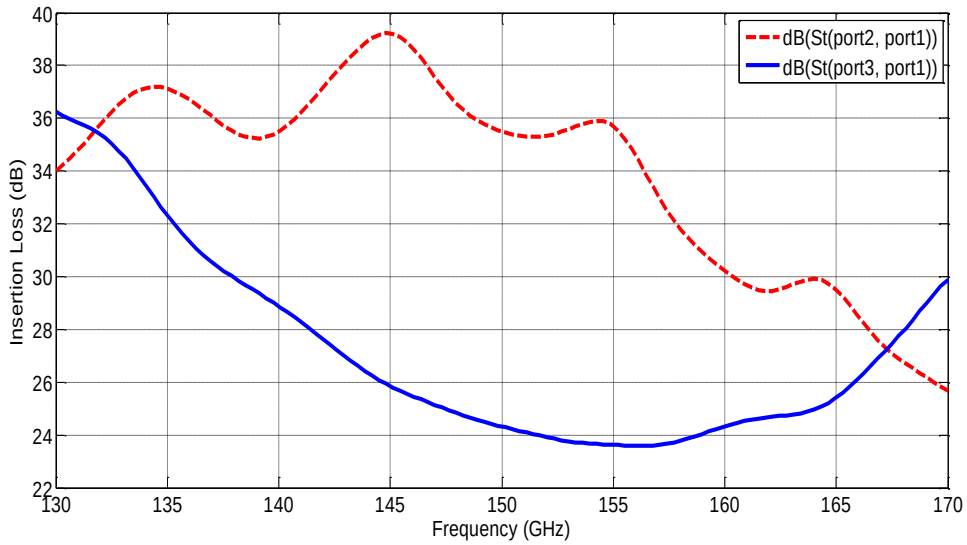


Figure 5.3. Insertion loss for helical antenna design in dB (*St(Port_i,Port_j)*) is $20log_{10}(S_{ij})$, i=2, 3, j=1.

Figure 5.4 shows the unequalized (original) channel impulse responses in terms of power delay profiles (PDPs) for the side-to-side and diagonal channels between 150 and 160 GHz. Again, we use the root-mean square delay spread as a measure of dispersion. From this figure, the worst (largest) RMS-DS pertains to the side-to-side channel, in agreement with what we expect from the results in Figure 5.3, where the side-to-side channel's response shows larger variation in insertion loss than the diagonal channel across that 10 GHz band. We show in Figures 5.5 and 5.6 the elevation and azimuth radiation patterns of the helical antennas in the simulated WiNoC environment. Note the similarity of the helix radiation patterns to the monopoles' patterns shown in the previous

chapter. This shows again the strong effect of the WiNoC landscape on their radiation properties and patterns.

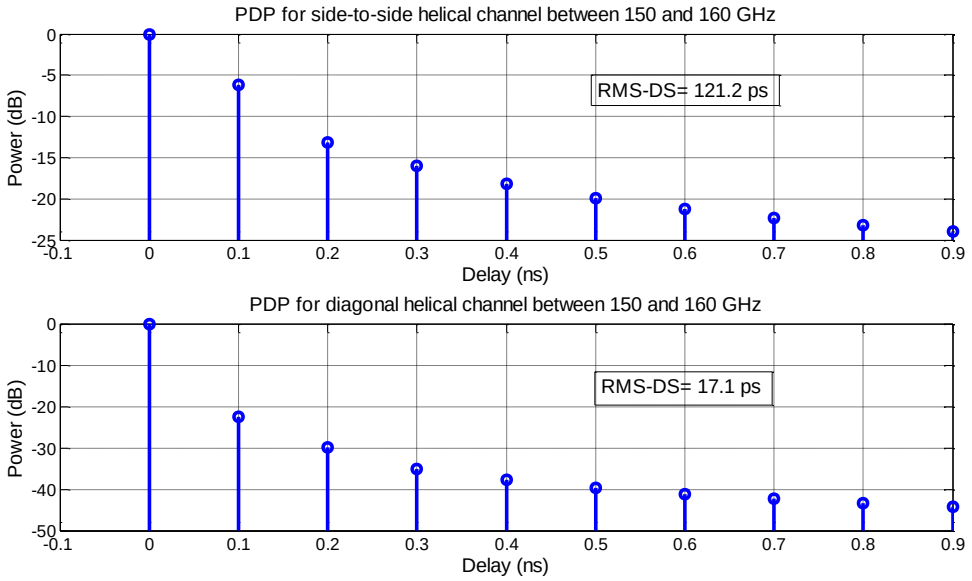


Figure 5.4. Unequalized power delay profiles of helix channels in specific frequency band 150-160 GHz.

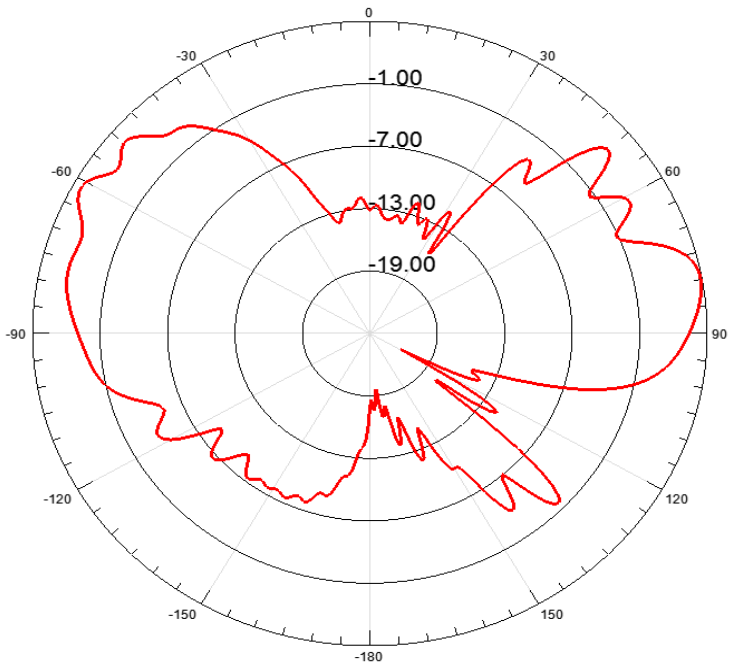


Figure 5.5. Helix elevation radiation pattern at polar coordinate ϕ=0°.

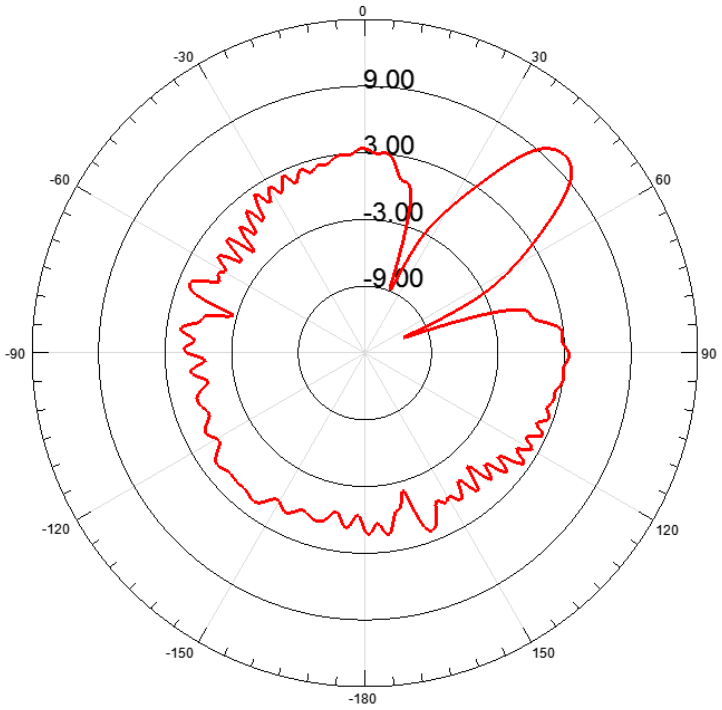


Figure 5.6. Helix azimuth radiation pattern at polar coordinate θ=90°.

5.3 Discone Model

The next type of vertically polarized wideband antenna that we consider in this section is the discone. As done previously, we will describe the design and show its performance in terms of impedance match, insertion loss, and channel dispersion in addition to showing the antenna radiation patterns. We still simulate the model in HFSS at the same center frequency of 150 GHz and use a 40 GHz frequency band. The model consists of four discone antennas--one at each corner of a 20 mm by 20 mm chip, containing a ground plane that lies beneath a polyimide substrate slab. Figure 5.7 depicts the design.

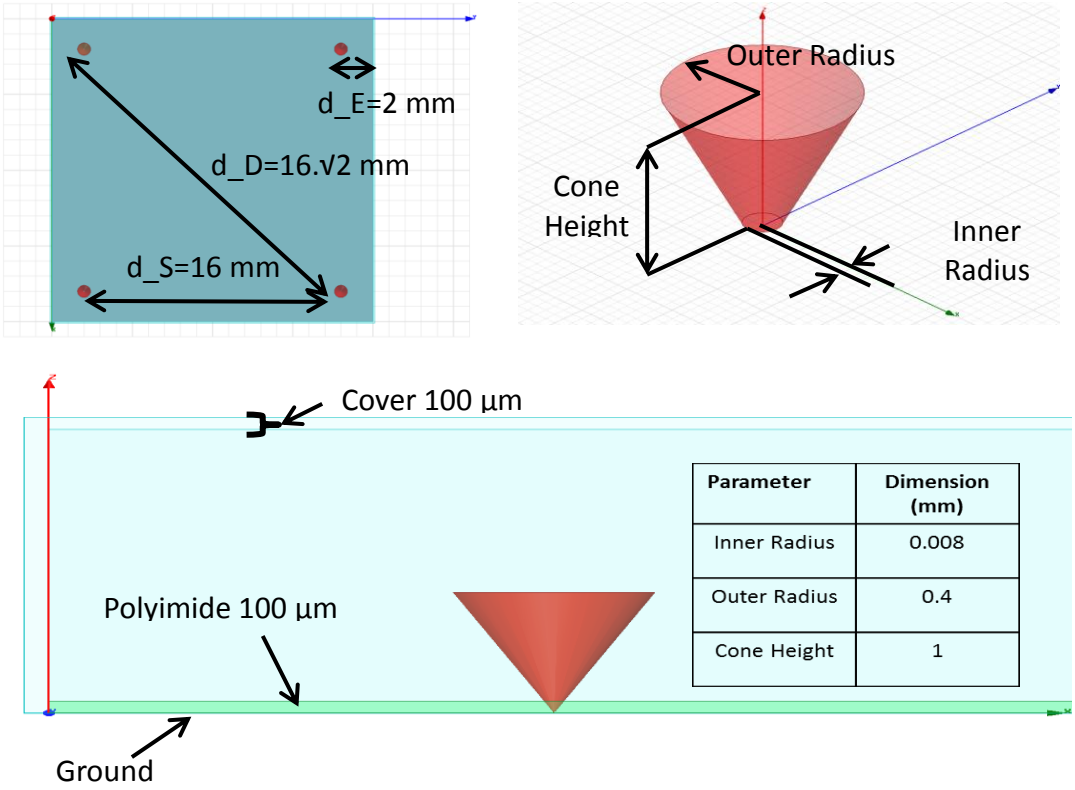


Figure 5.7. Discone model. Bottom: cross-section with inset table showing dimensions of the discone parameters; upper right: parameters of the discone; and, upper left: top view showing discones near corners of chip.

We still adopt the same definitions and dimensions for the entries “d_S”, “d_D”, and “d_E”. The *Sii* values are lower than -10 dB for the whole frequency range as seen in Figure 5.8. This result confirms the intrinsic wideband characteristic of the discone.

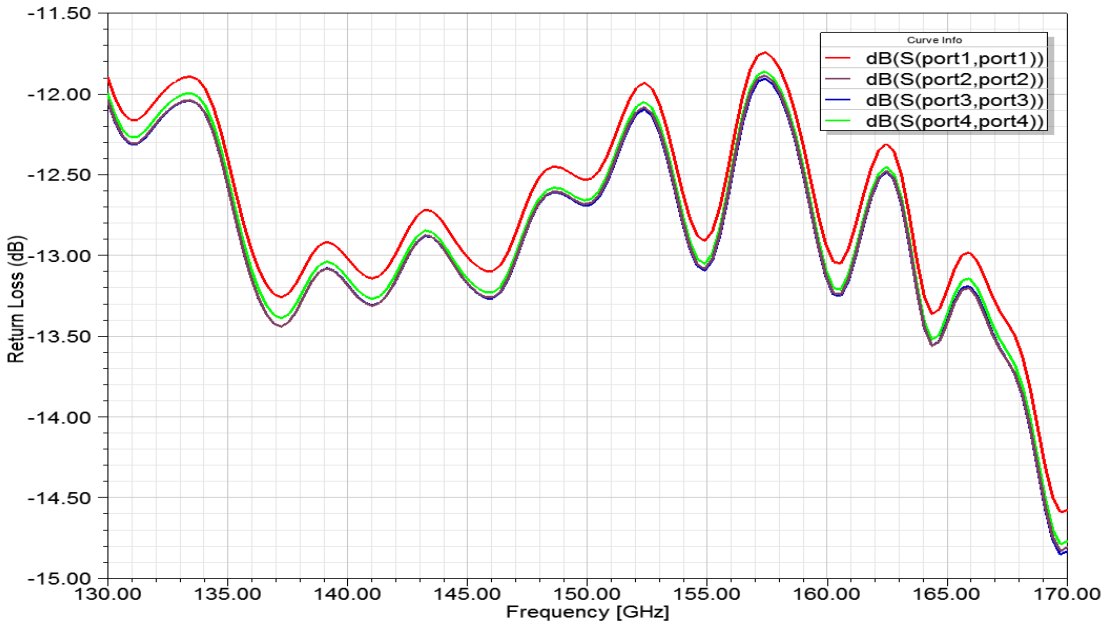


Figure 5.8. Return loss for discone antenna design in dB (*S (Porti,Porti)*) is $20log_{10}(S_{ii})$, i=1, 2, 3, 4.

We show in Figure 5.9 the channel attenuation vs. frequency for the discone antenna design. Still employing the same designation for the side-to-side and diagonal channels (S_{21} and S_{31}) and the same definition of bandwidth from the previous chapter, we can observe that for the side-to-side discone channel, the maximum single-channel bandwidth available is 6 GHz (147-153 GHz), whereas for the diagonal channels the maximum single-channel bandwidth is 22 GHz (143-165 GHz). This diagonal channel bandwidth is the highest we have obtained so far among all the different models we have previously considered in the current and previous chapters. Also, this channel exhibits around 7 dB less insertion loss compared to the maximum single-channel bandwidth achieved by the helix model.

As for the side-to-side channels in the discone model, their maximum insertion loss variation is 13 dB in the frequency range between 130 and 155 GHz compared to a 5 dB maximum variation for the helix side-to-side channels in the same frequency range. In the frequency range from 155 to 170 GHz, the side-to-side discone channels have a maximum variation in insertion loss of 14 dB compared to 10 dB for the helix side-to-side channels.

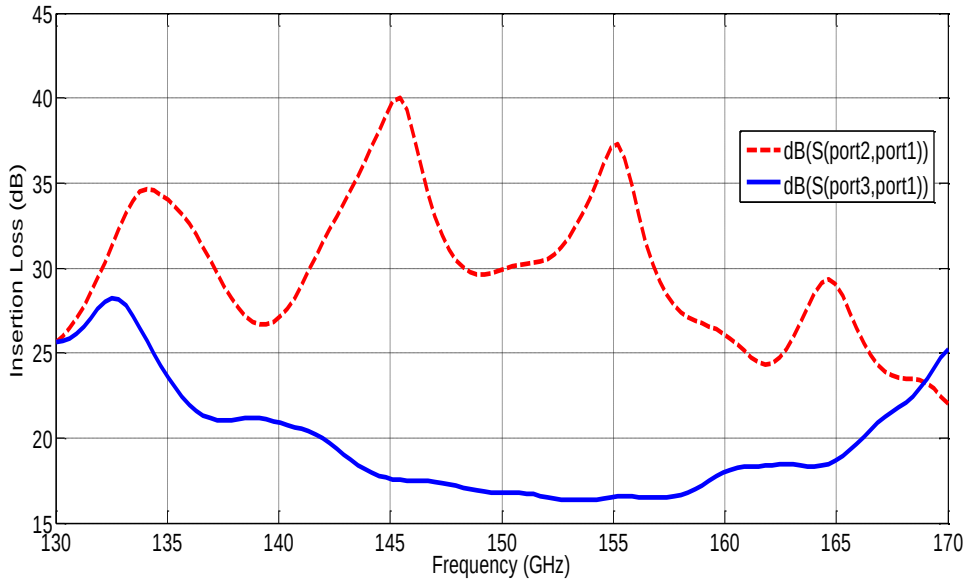


Figure 5.9. Insertion loss for discone antenna design in dB (*S (Porti,Portj)*) is $20log_{10}(S_{ij})$, i=2, 3, j=1.

Figure 5.10 shows the unequalized (original) channel impulse responses in terms of power delay profiles (PDPs) for the side-to-side and diagonal channels between 140 and 150 GHz. From this figure, the worst (largest) RMS-DS pertains to the side-to-side channel, in agreement with what we expect from the results in Figure 5.9, where the side-to-side channel's response shows larger variation in insertion loss than the diagonal channel across that 10 GHz band. We show in Figures 5.11 and 5.12 the elevation and

azimuth radiation patterns of the discone antennas in the simulated WiNoC environment. Note the similarity of the discone radiation patterns to the monopoles patterns shown in the previous chapter. We once again emphasize the strong effect of the landscape in which the antennas are placed on their radiation properties.

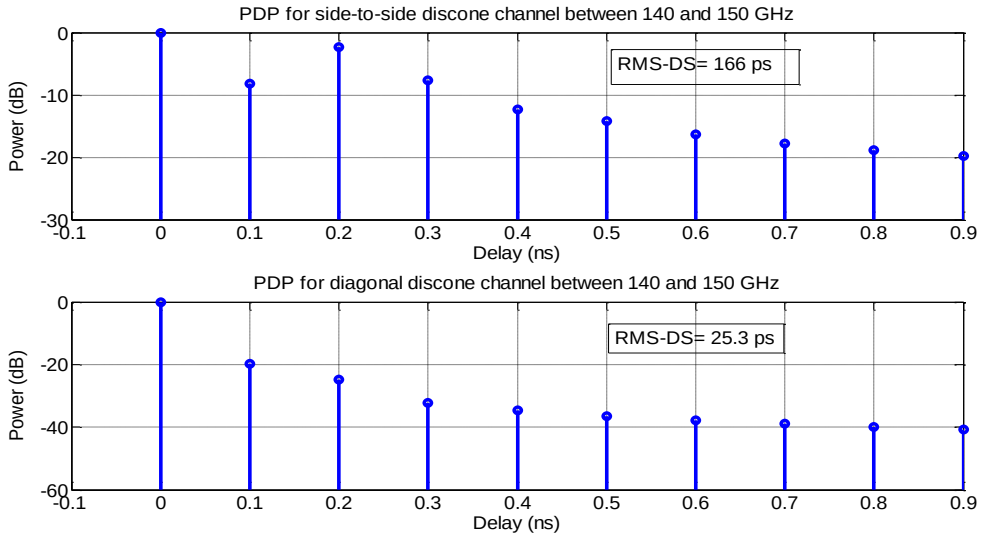


Figure 5.10. Unequalized power delay profiles of discone channels in a specific frequency band.

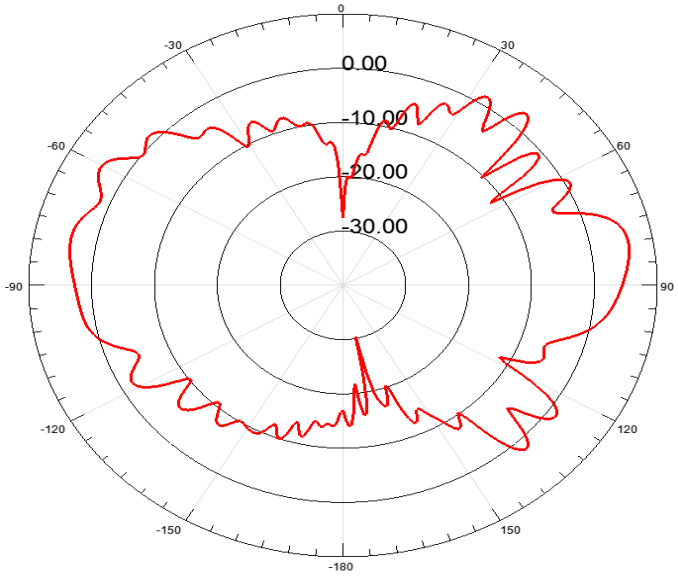


Figure 5.11. Discone elevation radiation pattern at polar coordinate ϕ=0°

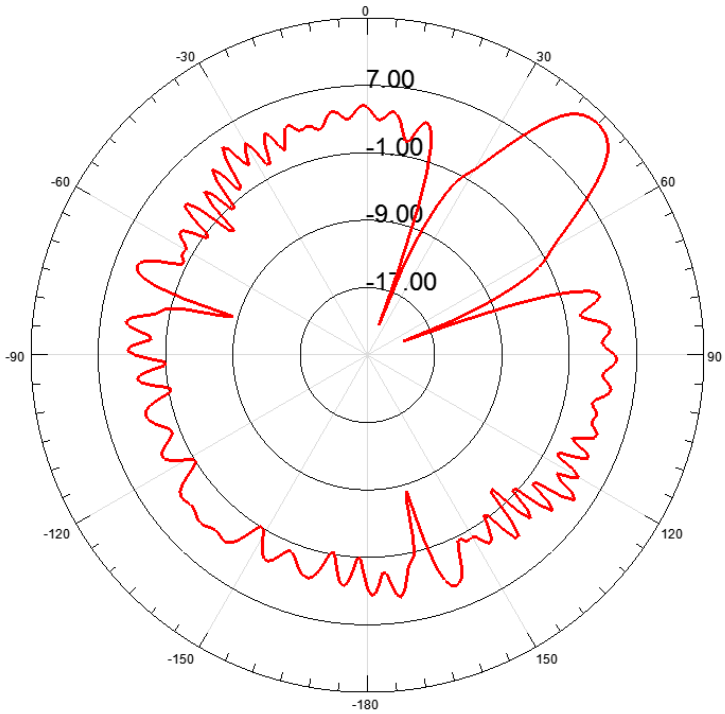
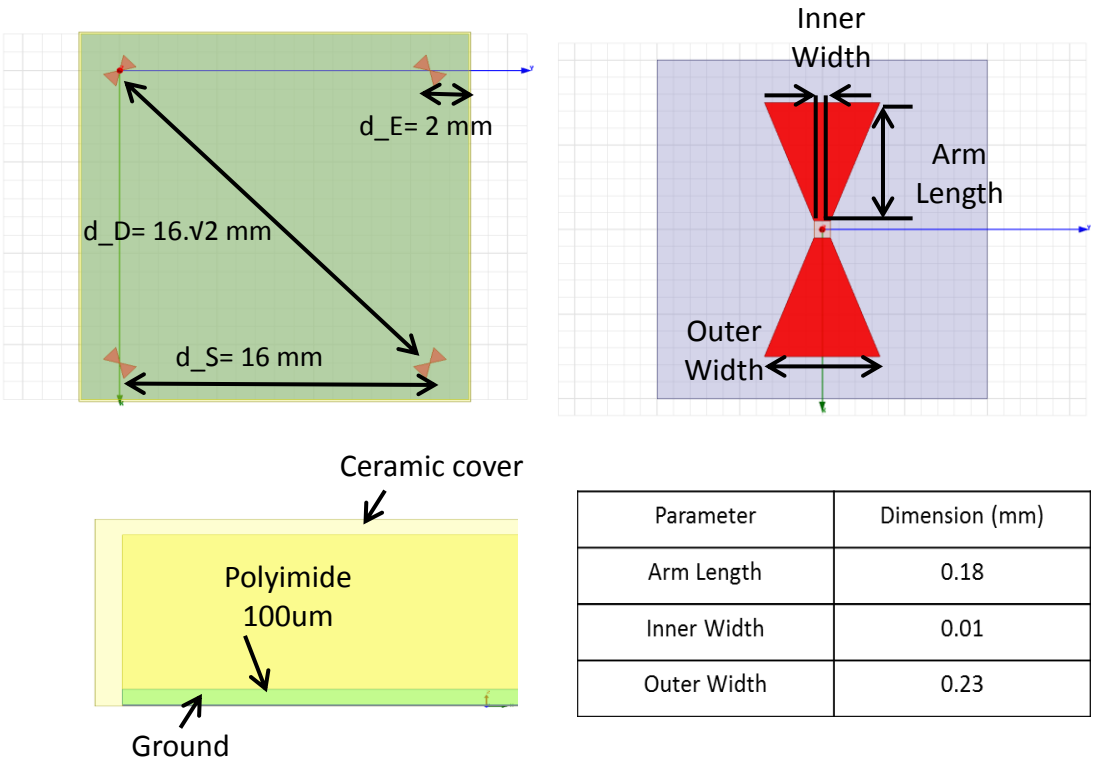


Figure 5.12. Discone azimuth radiation pattern at polar coordinate θ=90°.

5.4 Bowties Model

We consider in the two following sections printed wideband antennas. In this section, we consider the printed bowtie. The results shown are analogous to those shown for the previous wideband antennas, again at the same center frequency of 150 GHz with a 40 GHz frequency band. The model consists of four bowtie antennas--one at each corner of the 20 mm by 20 mm chip, containing a ground plane that lies beneath a polyimide substrate slab. Figure 5.13 shows a depiction of the design.



Parameter	Dimension (mm)
Arm Length	0.18
Inner Width	0.01
Outer Width	0.23

Figure 5.13. Bowtie model. Bottom left: cross-section; bottom right: table showing dimensions of the bowtie parameters; upper right: parameters of the bowtie; and, upper left: top view showing bowtie near corners of chip.

We use the same definitions and dimensions for the entries “d_S”, “d_D”, and “d_E”. The *Sii* values are lower than -10 dB for the frequency range between 148-153 GHz as seen in Figure 5.14. Although this result is around a factor of 2.5 larger than that of the printed dipoles, it is still considered narrow in comparison to the upright antennas. The ground plane affects to a large extent the performance of these broadside antennas that do not typically use one for normal operation; as noted, we require the ground plane in our model to isolate the active devices located in the lower layers of the stackup.

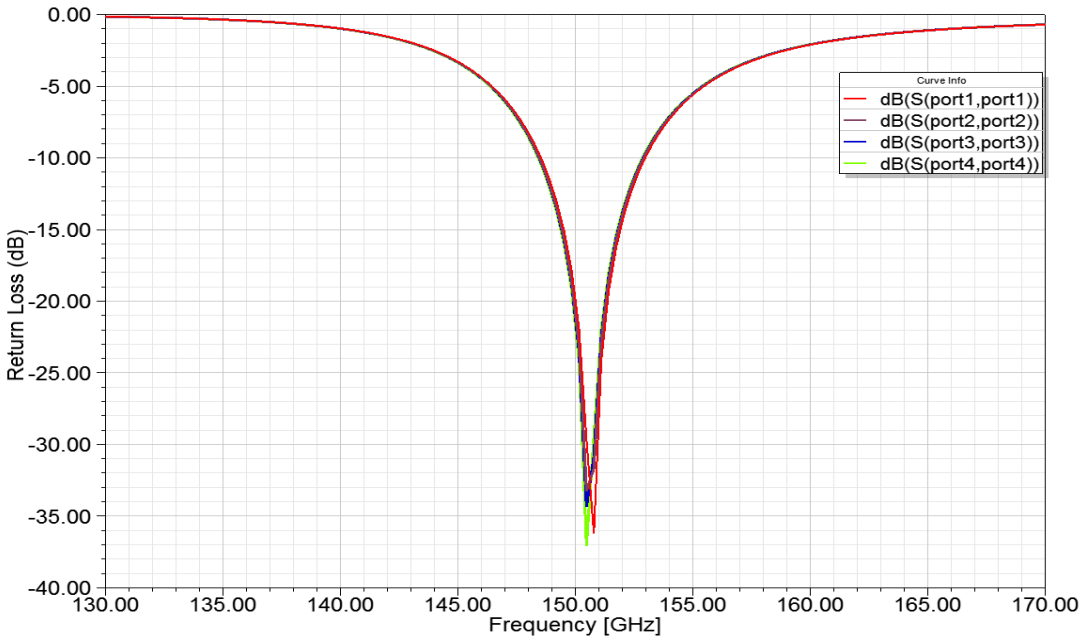


Figure 5.14. Return loss for bowtie design in dB(*S (Porti,Porti)*) is $20log_{10}(S_{ii})$, i=1, 2, 3, 4.

We show in Figure 5.14 the channel attenuation vs. frequency for the bowtie antenna design. Still adopting the same designation for the side-to-side and diagonal channels (S_{21} and S_{31}) and the same definition of bandwidth from the previous section, we can observe that for the side-to-side bowtie channel, the maximum single-channel bandwidth available is 8 GHz (147-155 GHz), whereas for the diagonal channels the maximum single-channel bandwidth is 9 GHz (148-157 GHz). These channel bandwidths are comparable to the ones achieved by the printed dipoles—6 GHz and 7 GHz for the diagonal and side-to-side channels, respectively—in Chapter 4. Note the similar high insertion loss numbers as well, where this metric ranges between 45 dB and 90 dB for the bowties, and between 50 dB and 125 dB for the printed dipoles. The maximum single-

channel bandwidths for the side-to-side and diagonal bowtie links correspond to an insertion loss of around 45 dB and 58 dB, respectively. In comparison, the maximum single-channel bandwidths for the side-to-side and diagonal dipole links have an insertion loss of around 55 dB and 53 dB.

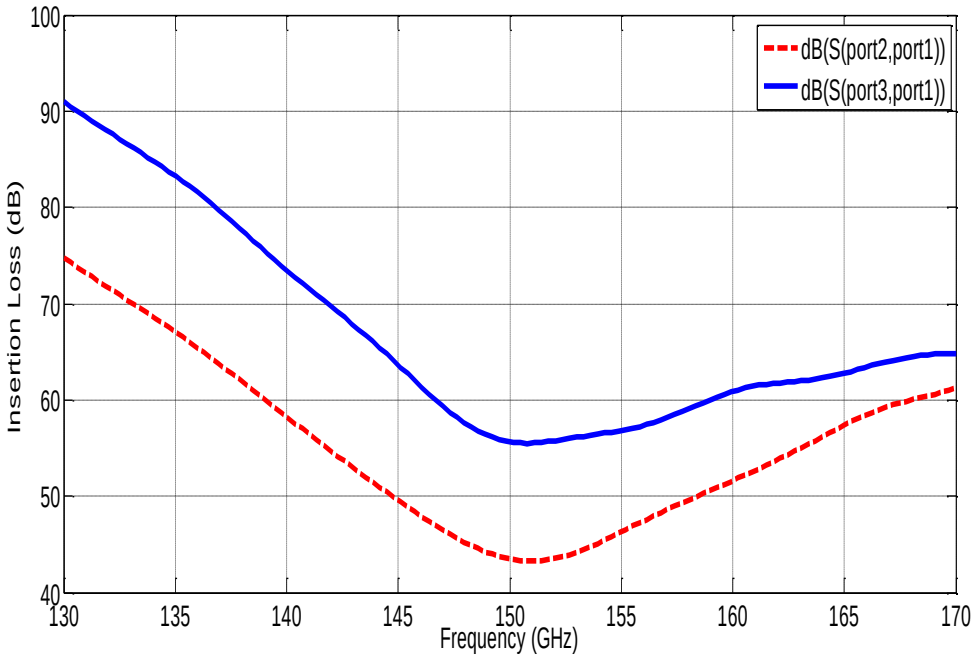


Figure 5.15. Insertion loss for bowtie antenna design in dB (*S (Porti,Portj)*) is $20log_{10}(S_{ij})$, i=2, 3, j=1.

We show in Figure 5.16 the unequalized (original) channel impulse responses in terms of power delay profiles (PDPs) for the side-to-side and diagonal channels between 140 and 150 GHz. From this figure, the worst (largest) RMS-DS pertains to the diagonal channel, in agreement with what we expect from the results in Figure 5.15, where the diagonal channel's response shows a larger variation (18 dB) in insertion loss than the side-to-side channel (14 dB) across that 10 GHz band. Figure 5.17 and 5.18 show the elevation and azimuth radiation patterns of the bowtie antennas in the simulated WiNoC

environment. Note the similarity between these patterns and the ones pertaining to the printed dipoles. Compared to the printed dipoles, the bowtie azimuth pattern has a wider lobe in the direction of maximum radiation and around 3 dB higher gain in that direction.

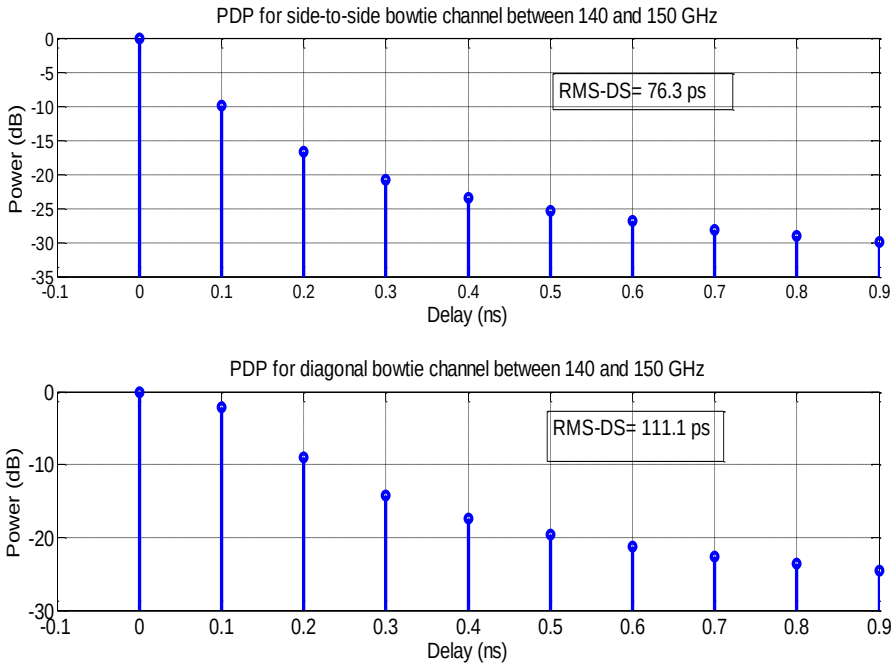


Figure 5.16. Unequalized power delay profiles of bowtie channels in specific frequency band 140-150 GHz.

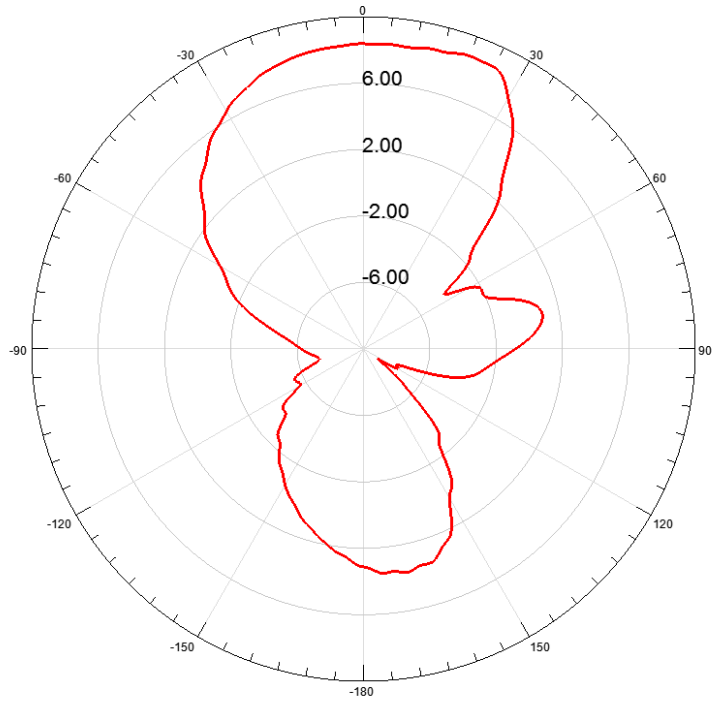


Figure 5.17. Bowtie elevation radiation pattern at polar coordinate ϕ=0.

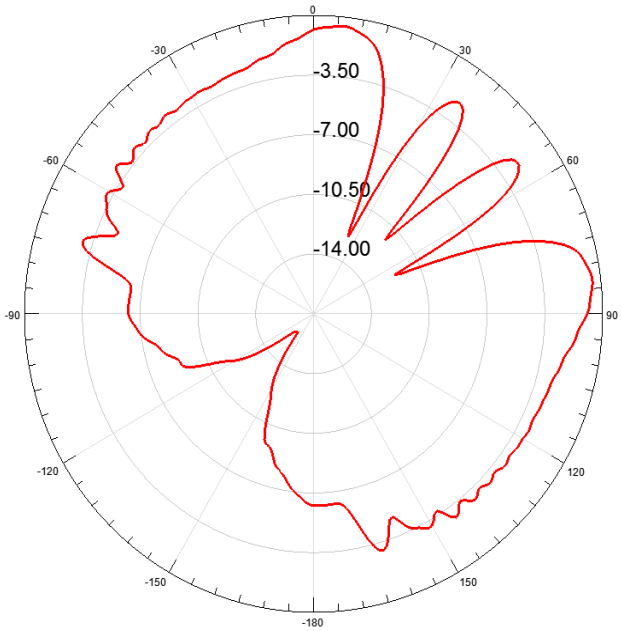
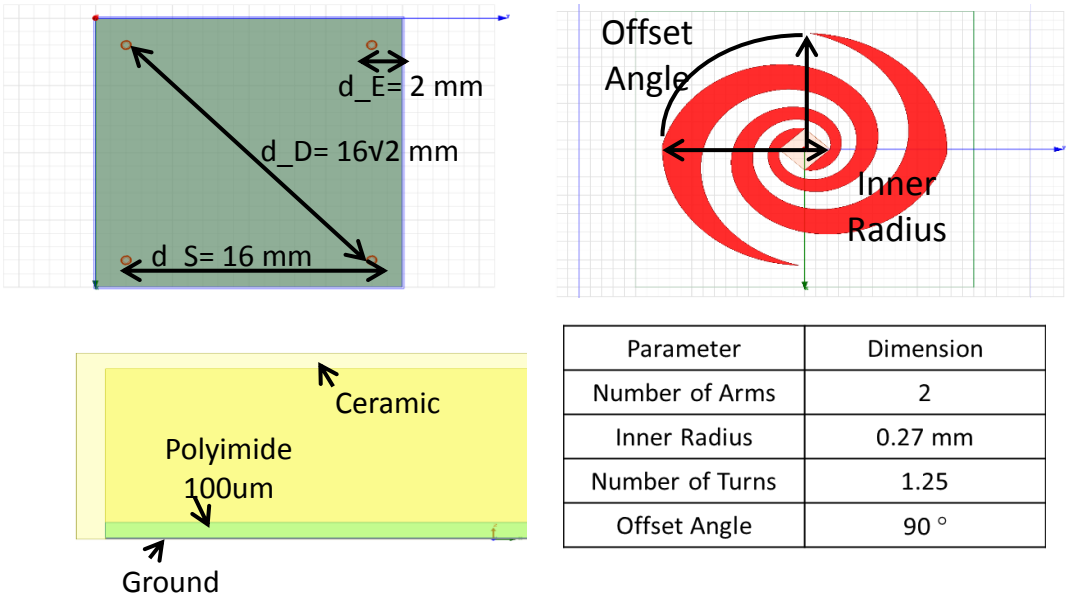


Figure 5.18. Bowtie azimuth radiation pattern at polar coordinate θ=90°.

5.5 Log-spiral Model

In this section, we consider the second type of printed wideband antenna, the printed log-spiral antenna. Our discussion is analogous to that in previous sections, with the same center frequency of 150 GHz and 40 GHz frequency band. The model consists of four printed log spiral antennas--one at each corner of a 20 mm by 20 mm chip, containing a ground plane that lies beneath a polyimide substrate slab. Figure 5.19 shows the design.



Parameter	Dimension
Number of Arms	2
Inner Radius	0.27 mm
Number of Turns	1.25
Offset Angle	90 °

Figure 5.19. Log-spiral model. Bottom left: cross-section; bottom right: table showing dimensions of the log-spiral parameters; upper right: parameters of the log spiral; and, upper left: top view showing bowtie near corners of chip.

The terms “d_S”, “d_D”, and “d_E” still have the same definitions and dimensions as the ones we used previously. The *Sii* values are lower than -10 dB for the

frequency range between 145-150 GHz as seen in Figure 5.20. This result is very similar to the one achieved by the bowties and it is still considered narrow. Here again, the ground plane affects to a large extent the performance of antennas that do not require one for normal operation.

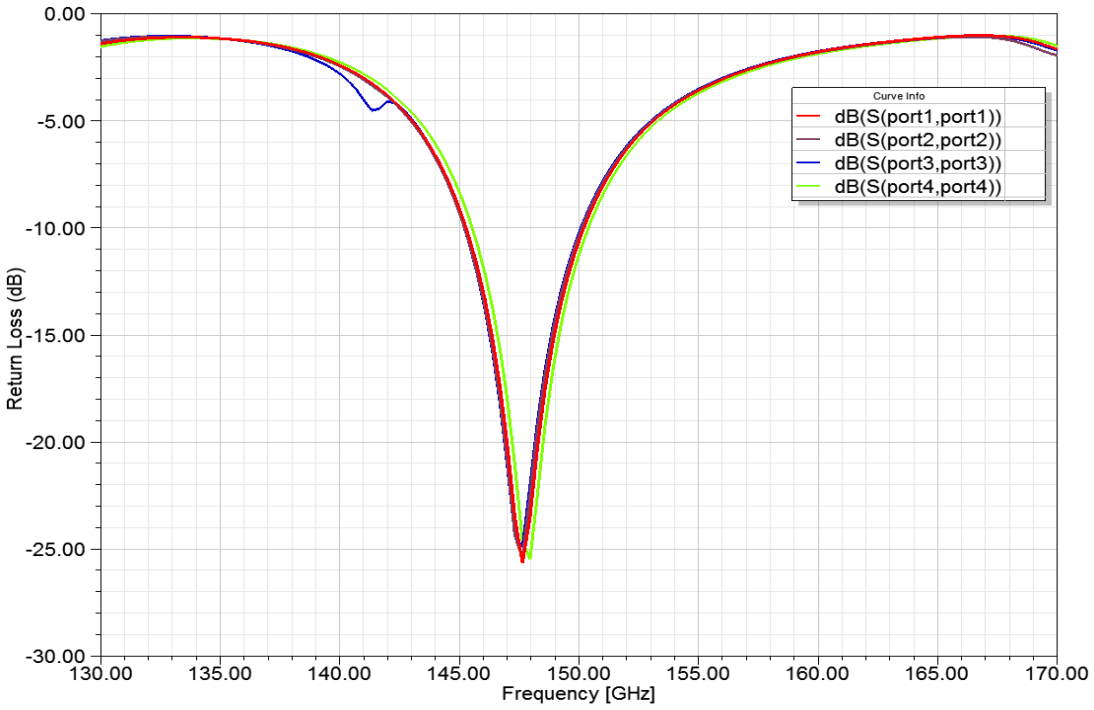


Figure 5.20. Return loss for log-spiral design in dB(*S (Porti,Porti)*) is $20log_{10}(S_{ii})$, i=1, 2, 3, 4.

We show in Figure 5.21 the channel attenuation vs. frequency for the bowtie antenna design. Still employing the same designation for the side-to-side and diagonal channels (S_{21} and S_{31}) and the same definition of bandwidth from the previous sections, we can observe that for the side-to-side bowtie channel, the maximum single-channel bandwidth available is 14 GHz (146-160 GHz), whereas for the diagonal channels the maximum single-channel bandwidth is 10 GHz (159-169 GHz). These channel

bandwidths are the highest achieved by any *printed* model we have considered previously--6 GHz and 7 GHz for the diagonal and side-to-side dipole channels, respectively, and 9 GHz and 8 GHz for the respective bowtie diagonal and side-to-side channels. Note the lower insertion loss numbers, ranging between 43 dB and 66 dB (for the entire frequency range), whereas this metric is between 45 dB and 90 dB for the bowties, and between 50 dB and 125 dB for the printed dipoles.

The maximum single-channel bandwidths for the side-to-side and diagonal log-spiral links have an insertion loss of around 44 dB and 50 dB. In comparison, the maximum single-channel bandwidths for the side-to-side and diagonal bowtie links have an insertion loss of around 45 dB and 58 dB respectively. As for the printed dipoles, the maximum single-channel bandwidths for the side-to-side and diagonal dipole links have an insertion loss of around 55 dB and 53 dB.

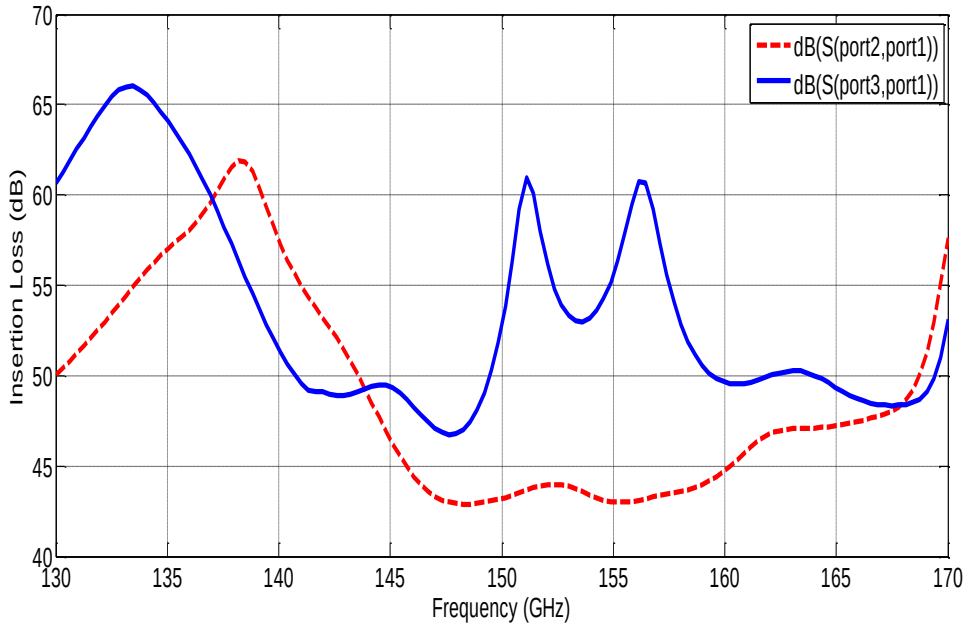


Figure 5.21. Insertion loss for log-spiral antenna design in dB (*S (Porti,Portj)*) is $20\log_{10}(S_{ij})$, i=2, 3, j=1.

We show in Figure 5.22 the unequalized (original) channel impulse responses in terms of power delay profiles (PDPs) for the side-to-side and diagonal channels between 150 and 160 GHz. From this figure, the worst (largest) RMS-DS pertains to the diagonal channel, in agreement with what we expect from the results in Figure 5.15, where the diagonal channel's response shows multiple lobes and a larger variation (11 dB) in insertion loss than the side-to-side channel (2 dB) across that 10 GHz band. Figures 5.23 and 5.24 show the elevation and azimuth radiation patterns of the log-spiral antennas. Those patterns are noticeably different than the bowtie and dipole patterns. The log spirals achieve an appreciable gain of 5 dB in the direction of maximum radiation.

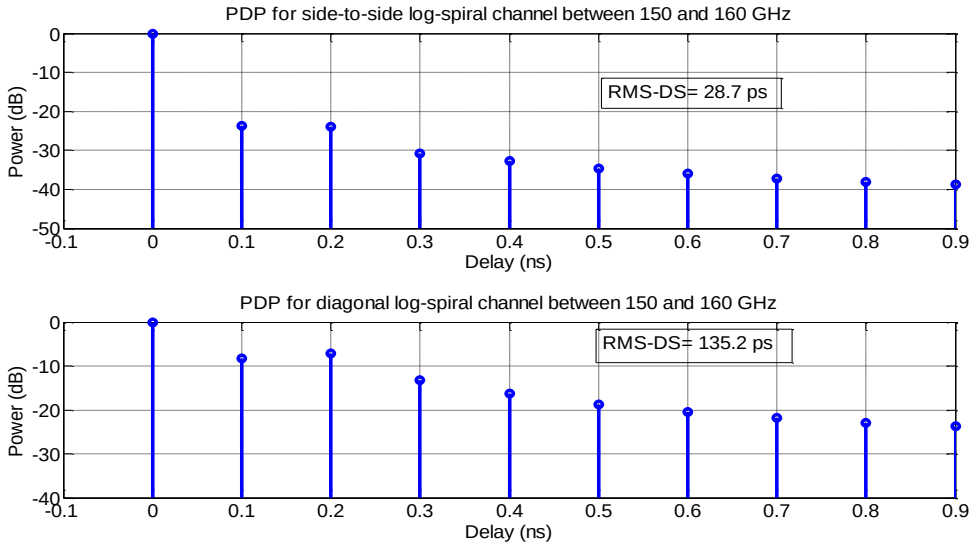


Figure 5.22. Unequalized power delay profiles of log-spiral channels in specific frequency band 150-160 GHz.

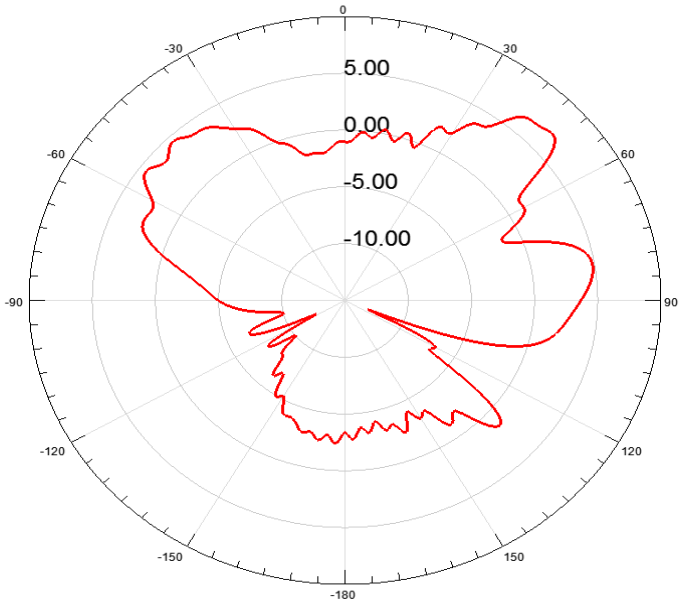


Figure 5.23. Log-spiral elevation radiation pattern at polar coordinate ϕ=0.

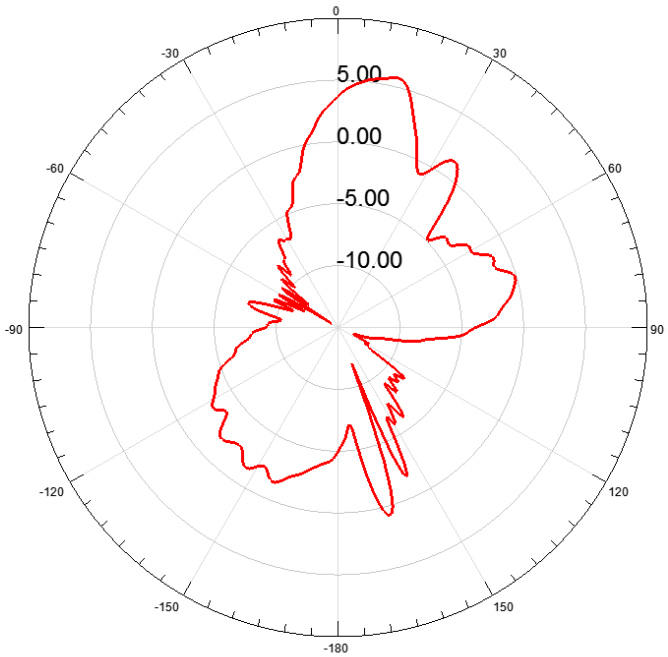


Figure 5.24. Log-spiral azimuth radiation pattern at polar coordinate θ=90°.

5.6 Wideband Multiple Access Schemes

We show in Figure 5.25 the insertion loss for the diagonal and side-to-side links from the helix model in addition to the maximum channel bandwidth (according to our 2 dB slope criterion) achieved in each of the eight 5 GHz channels that consistute the 40 GHz frequency span. The numbers in black (top) are for the diagonal link whereas the numbers in red (bottom) are for the side-to-side link.

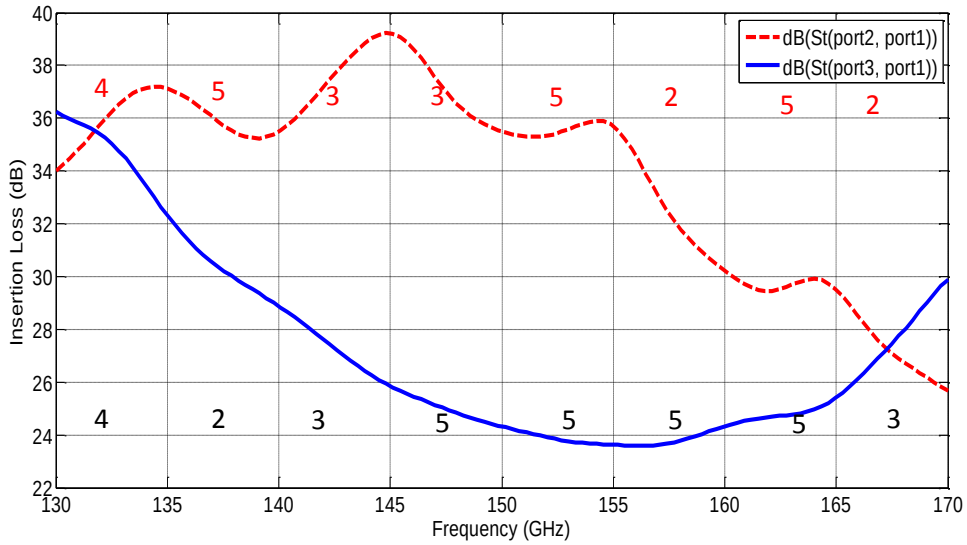


Figure 5.25. Insertion loss for helix model with channel bandwidths per each 5 GHz channel.

We show in Figure 5.26 the calculated bandwidths (~ histogram) of each of the 8 channels that span the frequency range of 40 GHz for this case. The S2S, BW, MaxSCBW abbreviations again denote "side-to-side", "bandwidth", and "maximum single channel bandwidth," respectively.

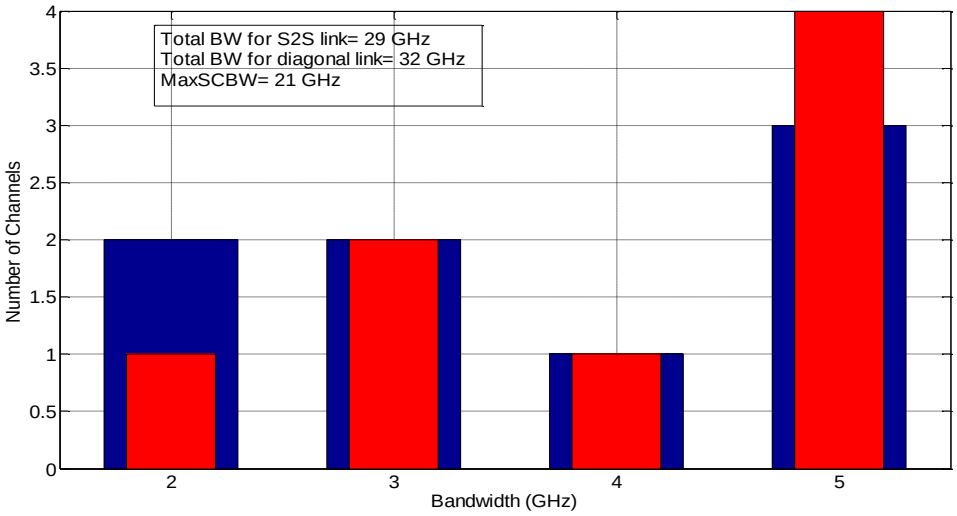


Figure 5.26. Channel bandwidths for helix design.

For clarity and in order to make Figure 5.27 less crowded, the entries "d_S", "d_D", and "d_E" used in the previous chapter still stand for the side-to-side separation between the antennas, diagonal separation between the antennas, and the separation of the antenna from the edges of the chip, respectively. These also represent the same dimensions. Parameter B_{xy} again denotes the bandwidth of the channel between antennas x and y. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 35 GHz with perfect filtering. This bandwidth is achieved by using a specific transmission/reception scheme represented by the dashed arrows in Figure 5.27. The maximum single channel bandwidth of 21 GHz is achieved from the diagonal link and occurs between 145 GHz and 166 GHz. We show in Table 5.1 the channels that achieve the maximum bandwidth and frequency spans.

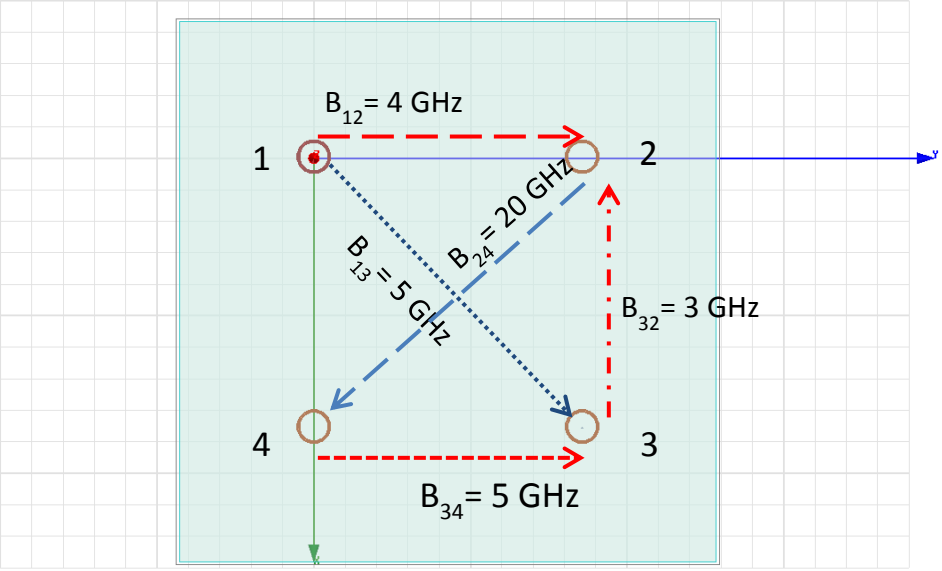


Figure 5.27. Channel assignment for helix model.

Table 5.1. Maximum bandwidth channel allocation for helix model

Channel	Bandwidth (GHz)	Frequency range (GHz)
C_{12}	4	130-135
C_{34}	5	135-140
C_{13}	3	140-145
C_{24}	20	145-165
C_{32}	3	165-170

B. Discone Multiple Access

Following the same analysis, we show in Figure 5.28 the insertion loss for the diagonal and side-to-side links from the discone model in addition to the maximum channel bandwidth (according to our 2 dB slope criterion) achieved in each of the eight 5 GHz channels that consistute the 40 GHz frequency span. As before, the numbers in black (top) are for the diagonal link whereas the numbers in red (bottom) are for the side-to-side link. In Figure 5.29, we show the calculated bandwidths of each of the 8 channels that span the frequency range of 40 GHz.

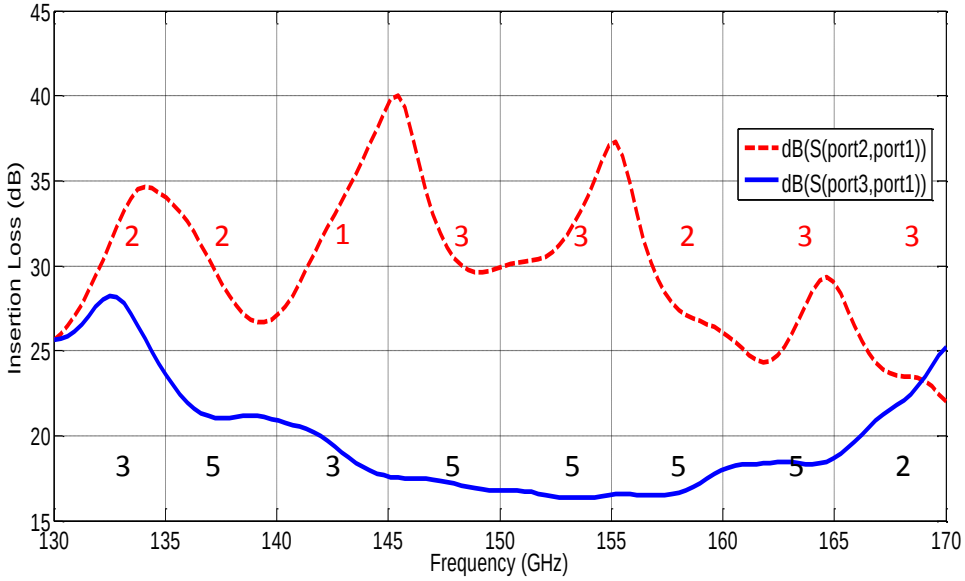


Figure 5.28. Insertion loss for discone model with channel bandwidths for each of the 5 GHz channels.

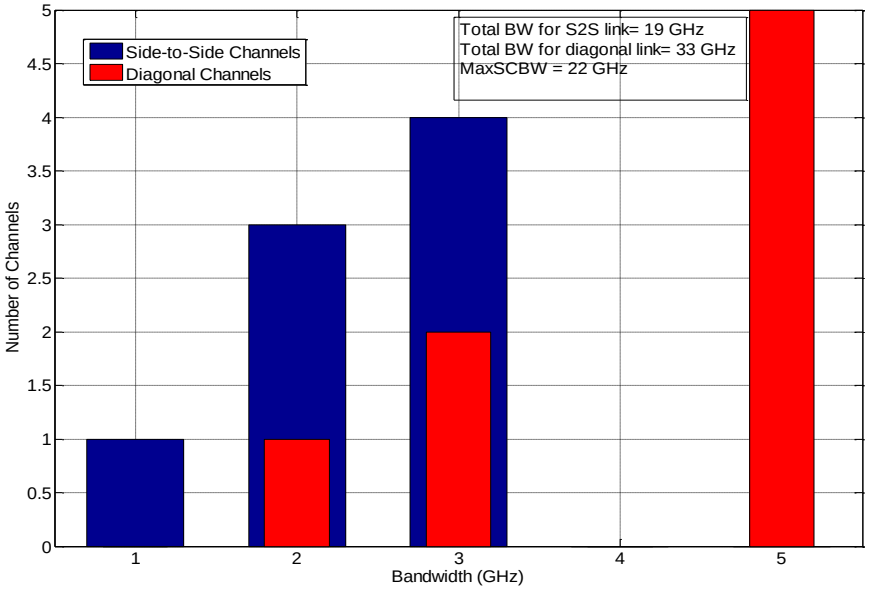


Figure 5.29. Channel bandwidth for discone design.

We show in Figure 5.30 a specific transmission/reception scheme, represented by the dashed arrows, that achieves a bandwidth of 33 GHz. This bandwidth can be achieved

by using the side-to-side and diagonal channels simultaneously, presuming perfect filtering. The acronyms and distances between the antennas are the same as the ones used in previous sections and chapters. The maximum single channel bandwidth of 22 GHz is achieved from the diagonal link, and occurs between 144 GHz and 166 GHz. We show in Table 5.2 the channels that achieve the maximum bandwidth along with the frequency spans.

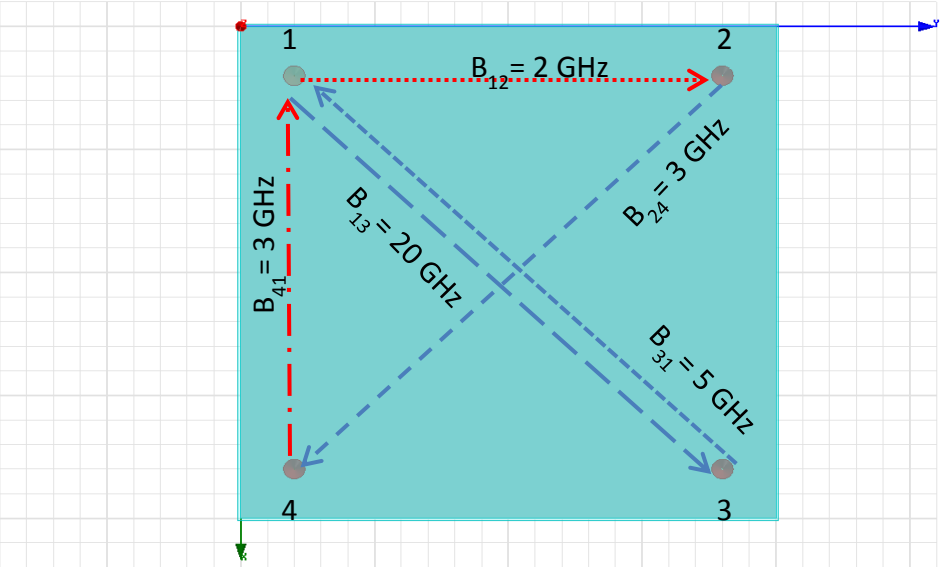


Figure 5.30. Channel assignment for discone model

Table 5.2. Maximum bandwidth channel allocation for discone model

Channel	Bandwidth (GHz)	Frequency range (GHz)
C_{12}	2	130-135
C_{31}	5	135-140
C_{24}	3	140-145
C_{13}	20	145-165
C_{41}	3	165-170

C. Bowtie Multiple Access

Continuing with the same procedure to analyze the multiple access schemes, we show in Figure 5.31 the insertion loss for the diagonal and side-to-side links from the bowtie model in addition to the maximum channel bandwidth (according to our 2 dB slope criterion) achieved in each of the eight 5 GHz channels that consistute the 40 GHz frequency span. The numbers in black (bottom here) are for the diagonal link whereas the numbers in red (top here) are for the side-to-side link. In Figure 5.32, we show the calculated bandwidths of each of the 8 channels that span thefrequency range of 40 GHz.

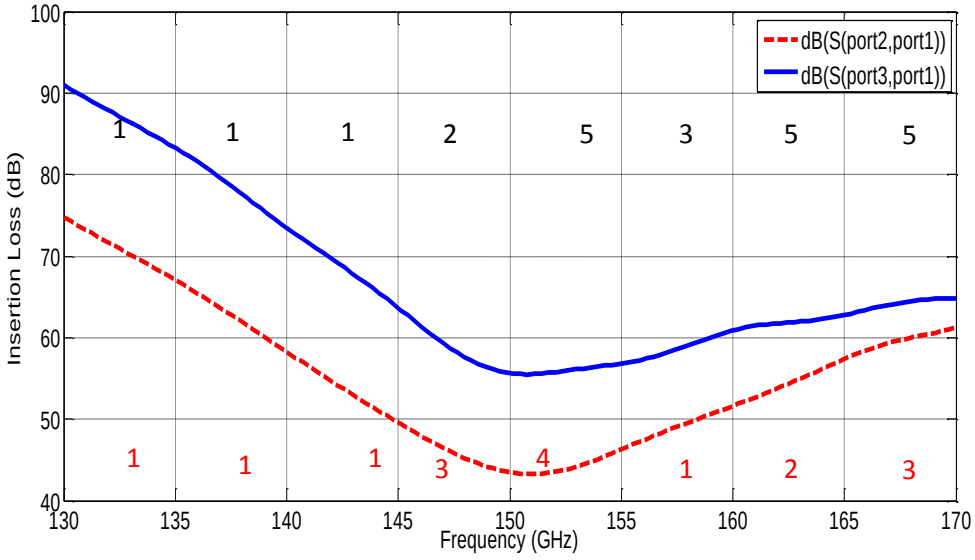


Figure 5.31. Insertion loss for bowtie model with channel bandwidth s for each of the 5 GHz channels.

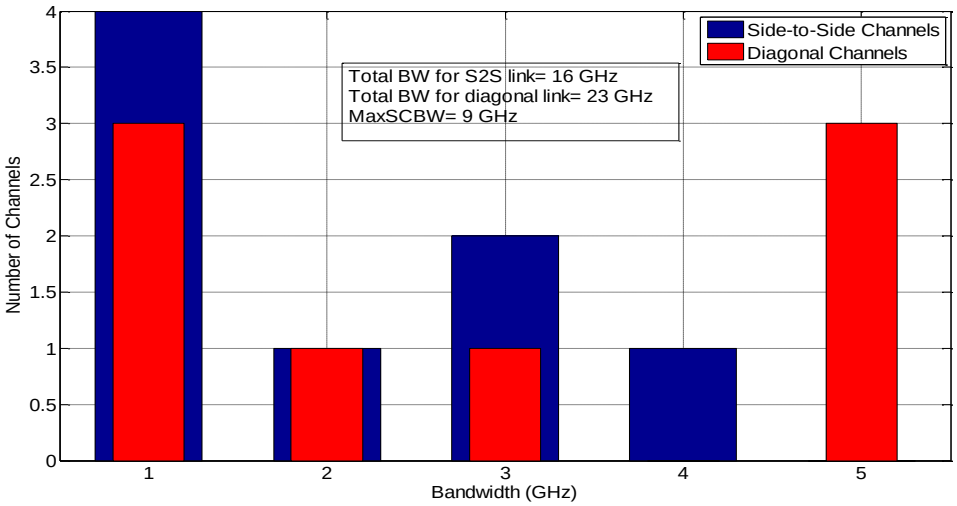


Figure 5.32. Channel bandwidth for bowtie design.

Figure 5.33 shows a specific transmission/reception scheme, represented by the dashed arrows, that achieves a bandwidth of 24 GHz. This bandwidth can be achieved by using the side-to-side and diagonal channels simultaneously, presuming perfect filtering. All acronyms and distances between the antennas are the same as used in previous sections and chapters. The maximum single channel bandwidth of 9 GHz is achieved from the diagonal link and occurs between 148 GHz and 157 GHz.

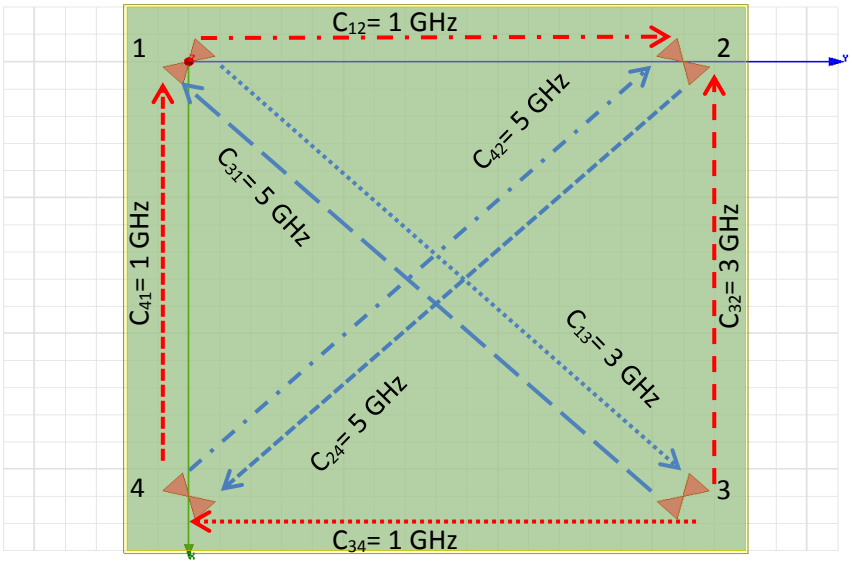


Figure 5.33. Channel assignment for bowtie model.

We show in Table 5.3 the channels that achieve the maximum bandwidth and their frequency spans. Compared to the printed dipoles, the bowtie network achieves 4 GHz less bandwidth than the dipoles. However, the side-to-side bowties channels between 130 GHz and 150 GHz exhibit an insertion loss between 45 dB and 75 dB whereas the same channels in the dipole network exhibit an insertion loss between 65 dB and 105 dB. For the frequency range between 150 GHz and 170 GHz, the side-to-side bowtie channels' insertion loss varies between 45 dB and 60 dB compared to a variation between 52 dB and 70 dB for the dipole antennas. As for the diagonal channels from the bowtie design, their insertion loss varies between 55 dB and 90 dB for the frequency range of 130 GHz- 150 GHz compared to a variation from 62 dB to 125 dB in the same frequency range for the printed dipoles. As for the frequency range of 150 GHz-170 GHz, the diagonal channels from the bowtie model exhibit an insertion loss between 55 dB and 65 dB compared to a variation from 50 dB to 62 dB for the printed dipoles in that span. It is obvious that both models perform better in the frequency range of 150 GHz-170 GHz but they still underperform compared to the monopoles, helixes, and discones.

Table 5.3. Maximum bandwidth channel allocation for bowtie model

Channel	**Bandwidth (GHz)**	**Frequency range (GHz)**
C_{12}	1	130-135
C_{34}	1	135-140
C_{41}	1	140-145
C_{32}	3	145-150
C_{42}	5	150-155
C_{13}	3	155-160
C_{24}	5	160-165
C_{31}	5	165-170

D. Log-spiral Multiple Access

Figure 5.34 shows the insertion loss for the diagonal and side-to-side links from the bowtie model in addition to the maximum channel bandwidth (according to our 2 dB slope criterion) achieved in each of the eight 5 GHz channels that consistute the 40 GHz frequency span. As previously, the numbers in black (bottom) are for the diagonal link whereas the numbers in red (top) are for the side-to-side link. In Figure 5.35, we show the calculated bandwidths of each of the 8 channels that span thefrequency range of 40 GHz.

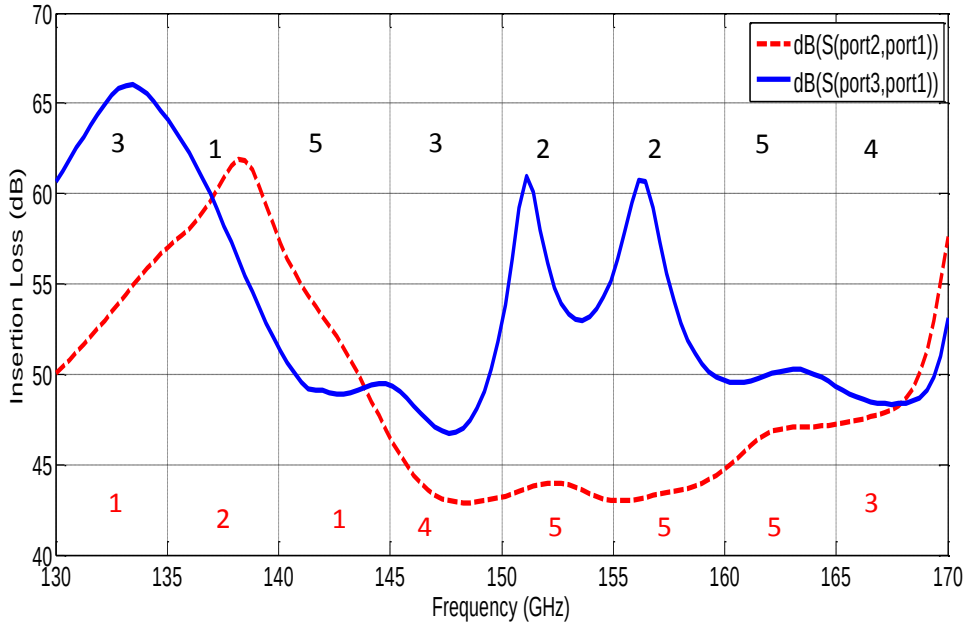


Figure 5.34. Insertion loss for log-spiral model with channel bandwidths for each of the 5 GHz channels.

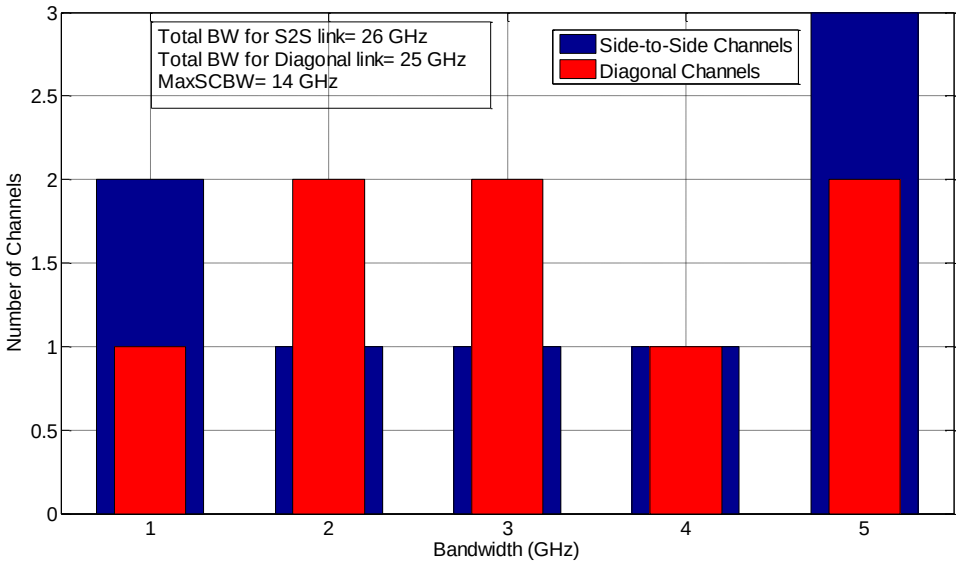


Figure 5.35. Channel bandwidth for log-spiral design.

We show in Figure 5.36 a specific transmission/reception scheme, represented by the dashed arrows, that achieves a bandwidth of 33 GHz. This bandwidth can be achieved by using the side-to-side and diagonal channels simultaneously, presuming perfect

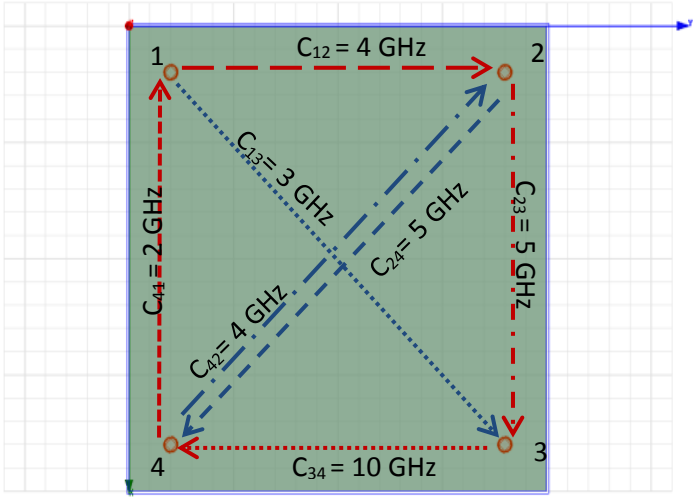


Figure 5.36. Channel assignment for log-spiral model

filtering. All acronyms and distances between antennas are the same as used previously. The maximum single channel bandwidth of 14 GHz is achieved from the side-to-side link and occurs between 146 GHz and 160 GHz.

We show in Table 5.4 the channels that achieve the maximum bandwidth along with their frequency spans. The log-spirals achieve the highest maximum total bandwidth of 33 GHz among all the printed designs (24 GHz for bowtie, and 28 GHz for dipoles) and this bandwidth is on par with the one achieved by the vertically polarized designs. Clearly, the log-spiral design outperforms its printed counterparts in almost all performance metrics.

Table 5.4. Maximum bandwidth channel allocation for log-spiral model

Channel	**Bandwidth (GHz)**	**Frequency range (GHz)**
C_{13}	3	130-135
C_{41}	2	135-140
C_{24}	5	140-145
C_{12}	4	145-150
C_{34}	10	150-160
C_{23}	5	160-165
C_{42}	4	165-170

We show in Table 5.5 a summary of the performance of all the wideband models. It is clear that vertically polarized antennas outperform their printed counterparts. They achieve a higher total bandwidth and maximum single channel bandwidth and also exhibit a smaller insertion loss variation. For the printed models, the log-spiral model is a clear winner in all the criteria. As for the wideband vertically polarized models and from a power efficiency standpoint, a highly desirable characteristic for WiNoC's, the discone

performs better than the helix by having 8 dB less insertion loss over which the maximum single channel bandwidth occurs. The bandwidth figures are very comparable between the discone and helix models. Note also the very comparable performance between the monopole model and the best upright wideband models, especially the discones. The monopole's maximum single channel bandwidth of 18 GHz is the only criterion where it is outperformed by the discones and helixes. It clearly outperforms the printed wideband models.

Table 5.5. Comparison between all wideband models and the monopole model.

	Helix	**Discone**	**Bowtie**	**Log-spiral**	**Monopoles**
Maximum total bandwidth (GHz)	35	33	24	33	33
MaxSCBW (GHz)	21	22	9	14	18
Insertion Loss over MaxSCBW (dB)	25	17	58	44	18
Minimum insertion loss (dB)	24	16	44	43	17
Maximum insertion loss (dB)	39	40	90	66	38

Chapter 6

OOK Bit Error Ratio as a Function of the Channel Impulse Response

6.1 Analysis

The performance of on off keying (OOK) in the presence of additive white Gaussian noise (AWGN) through a *non*-dispersive channel is well known. The purpose of this analysis is to investigate the performance of OOK through a dispersive channel and find an analytical expression that can be evaluated numerically.

A block diagram of the system is shown in Figure 6.1. The input signal is *s(t)*, the channel impulse response is *h(t)*, the AWGN signal is *w(t)*, and the n^{th} bit decision at the receiver output is $\widehat{s_n}$.

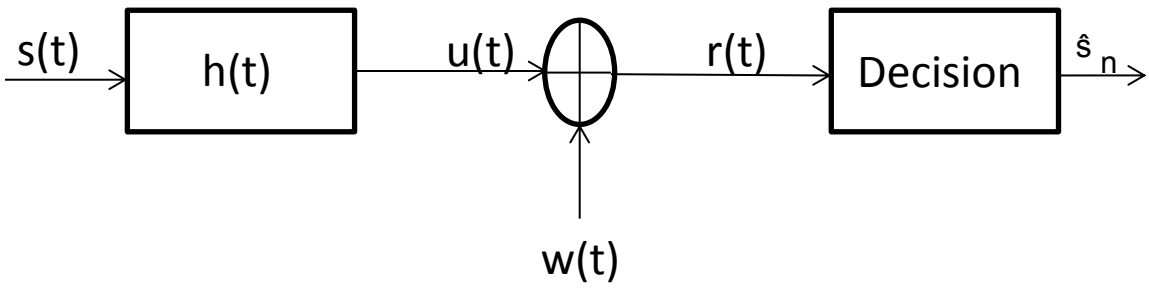


Figure 6.1. Block diagram for OOK analysis.

We have

$$s(t) = \sum_k d_k \, p(t - kT), \quad (1)$$

where the k^{th} source bit is $d_k \in \{0,1\}$, the pulse shape is defined as

$$p(t)=\begin{cases}1, 0 \le t \le T \\ 0, else\end{cases}, \quad (2)$$

and the channel impulse response is given by

$$h_s(t)=\sum_{i=0}^{L-1} h_i\, \delta(t-iT) \quad . \quad (3)$$

This response is that obtained from sampling the actual channel with samples taken every $T_{sample}=T$. The channel output waveform (in the absence of noise) is

$$u(t)=\sum_k d_k\, g(t-kT),$$

where $g(t)=p(t)*h(t)$, and the received signal is then given by $r(t)=u(t)+w(t)$. The AWGN $w(t)$ is zero mean, with two-sided spectral density $N_0/2$.

The bit decision is made by sampling $r(t)$ and then comparing with a threshold V. Since the bit stream and pulse shaping waveform, d_k and $p(t)$, take values of 0 and 1, the optimal threshold value, V, would be equal to 0.5 (assuming a unity-gain channel[4]). The sampled received sequence is $r(nT)=r(nT_{sample})=u(nT)+w(nT)$ or

$$r_n=\sum_k d_k\, g(nT-kT)+w_n$$

$$=\sum_k d_k\, g_{n-k}+ w_n$$

$$=d_n g_0+\sum_{k\neq n} d_k\, g_{n-k}+ w_n \quad (4)$$

where the three consecutive terms in (4) represent the desired component, the intersymbol interference component, and noise component, respectively.

[4] Even when the channel's gain is not unity, we can arbitrarily scale at the receiver in analysis since both signal and noise will be scaled equally, hence not changing performance.

For our model, we have $g(t)= \sum_{i=0}^{L-1} h_i\, p(t - iT)$. We choose the sampling time to be in the middle of each bit. Thus, the ISI term becomes $d_{k-1}g_1+d_{k-2}g_2+\ldots$, where $g_1=g(T+T/2)$, $g_2=(2T+T/2)$,... and since $|g_i|=|h_i|$ due to the fact that $|p(t)|=1$, the ISI component can be written as $\sum_{i=1}^{L-1} d_{n-i}\, g_i$ and (4) becomes

$$r_n= d_n h_0+ \sum_{i=1}^{L-1} d_{n-i}\, h_i + w_n \qquad (5)$$

Note that we have assumed that $|g_0|$= maximum $\{g_i\}$ for i=0, 1,.., L-1. However, if some other g_i is maximum, then we select as the "desired" bit the one associated with max$\{|g_i|\}$. As a result, the ISI term becomes $\sum_{\substack{i=0 \\ i\neq m}}^{L-1} d_{n-i}\, g_i$, with m being the index of max$\{|g_i|\}$. Analogously, this applies for the *h's*.

For the bit error probability, we have two cases:

$$P_{b1}=P(\hat{s}_n=0|d_n=1)=P(r_n<0.5|d_n=1) \qquad (6)$$

and

$$P_{b0}= P(\hat{s}_n=1|d_n=0)=P(r_n\geq 0.5|d_n=0) \qquad (7)$$

where V=0.5 is the threshold used to make a decision. First, let's consider $P_{b1.}$ From (5) and (6), $P_{b1}=P(h_0+ \sum_{i=1}^{L-1} d_{n-i}\, h_i + w_n<V)$

$$=P(w_n<V- h_0- \sum_{i=1}^{L-1} d_{n-i}\, h_i)$$

$$=P(w_n<\zeta)$$

Since w_n is a zero-mean Gaussian random variable with variance $\sigma^2=N_0/2$, with $N_0/2$ the noise spectral density, P_{b1} has a Q-function form, where $Q(x) = \int_x^\infty \exp(-u^2/2)du/\sqrt{2\pi}$. We can show that,

$$P_{b1}=\begin{pmatrix} Q\left(\frac{|\zeta|}{\sigma}\right), if\ \zeta<0 \\ 1-Q\left(\frac{|\zeta|}{\sigma}\right), if\ \zeta\geq 0 \end{pmatrix}=\begin{pmatrix} Q\left(\frac{-\zeta}{\sigma}\right), if\ \zeta<0 \\ 1-Q\left(\frac{\zeta}{\sigma}\right), if\ \zeta\geq 0 \end{pmatrix}= Q\left(\frac{-\zeta}{\sigma}\right) \text{ so}$$

$$P_{b1=}\, Q\left(\frac{-\mathrm{V}+h_0+\sum_{i=1}^{L-1} d_{n-i}h_i}{\sigma}\right) \qquad (8)$$

The next step is to incorporate $E_{b,avg}$ and N_0 into (5). To begin, the noise has a variance $\sigma^2=N_0/2$, so $\sigma = \sqrt{\frac{No}{2}}$. Since we are using OOK, $E_{b,avg}=0.5E_1+0.5E_0$ and $E_0=0$ because when a digital zero is input, nothing is transmitted.

For our sampled model, the energy is the square of the sample, i.e., d_k^2. Strictly, the received energy is $g_0^2 d_k^2=h_0^2\ d_k^2$ in the non-dispersive case, and is $d_k^2 \cdot \sum_{i=0}^{L-1} {h_i}^2$ in the dispersive case. We will normalize the CIR such that it has unit energy, i.e. $E_h=\sum {h_i}^2=1$.

Thus, we have $E_{b,avg}=0.5E_1=0.5d_k^2$ (for $d_k=1$). We can write $d_k=\sqrt{2E_{b,avg}}$, which would multiply all the ISI and d_n terms in (8). Also, so that performance is not a function of *absolute* noise level N_0 but a function of $E_{b,avg}/N_0$, the threshold value, V, would also be multiplied by $\sqrt{2E_{b,avg}}$. This yields $P_{b1=}\, Q\left(\frac{\left(-\mathrm{V}+h_0+\sum_{i=1}^{L-1} d_{n-i}h_i\right)\sqrt{2E_{b,avg}}}{\sqrt{\frac{\mathrm{N_0}}{2}}}\right)$ which leads to

$$P_{b1}= Q\left(\left[h_0+\ \sum_{i=1}^{L-1} d_{n-i}\, h_i - \mathrm{V}\right]\sqrt{\frac{4.E_{b,avg}}{\mathrm{N_0}}}\right) \qquad (9)$$

As a check, for the non-dispersive case, h_0=1 and h_i=0 $\forall$ $i\neq0$, (6) reduces to $Q\left(\sqrt{\frac{E_{b,avg}}{\mathrm{N}_0}}\right)$, which is the correct result for coherent OOK. Finally, for the average value of P_{b1}, we need to average over the random data vector $\underline{\boldsymbol{d}}_{n-1}=[d_{n-1},\ d_{n-2,}\ldots d_{n-(L-1)}]$ which has $2^{\mathrm{L-1}}$ possible values. Thus, if we denote each possible value of $\underline{\boldsymbol{d}}_{n-1}$ as $d_{n-1}{}^{(j)}$, then we get

$$P_{b1}=\frac{1}{2^{L-1}}\sum_{j=1}^{2^{L-1}} Q\left(\left[h_0+\sum_{i=1}^{L-1} d_{n-1}{}^{(j)}\, h_i-\mathrm{V}\right]\sqrt{\frac{4.E_{b,avg}}{\mathrm{N}_0}}\right) \qquad (10)$$

An analysis analogous to the one presented can be conducted to obtain an expression for P_{b0}. From (7), we get P_{b0}= $P(w_{\mathrm{n}}\geq \mathrm{V}-\sum_{i=1}^{L-1} d_{n-i}\, h_i)$

$$= P(w_{\mathrm{n}}\geq\zeta)$$

$$= 1- P(w_{\mathrm{n}}<\zeta).$$

This leads to,

$$P_{b0}=\begin{pmatrix} 1-Q\left(\frac{|\zeta|}{\sigma}\right), if\ \zeta<0 \\ Q\left(\frac{|\zeta|}{\sigma}\right), if\ \zeta\geq0 \end{pmatrix}=\begin{pmatrix} 1-Q\left(\frac{-\zeta}{\sigma}\right), if\ \zeta<0 \\ Q\left(\frac{\zeta}{\sigma}\right), if\ \zeta\geq0 \end{pmatrix}= Q\left(\frac{\zeta}{\sigma}\right) \text{ so}$$

$$P_{b0}= Q\left(\frac{\mathrm{V}-\sum_{i=1}^{L-1} d_{n-i}h_i}{\sigma}\right) \qquad (11)$$

In terms of $E_{b,avg}/\mathrm{N}_0$, (11) becomes

$$P_{b0}= Q\left(\mathrm{V}-\sum_{i=1}^{L-1} d_{n-i}\, h_i\right]\sqrt{\frac{4.E_{b,avg}}{\mathrm{N}_0}}\Bigg) \qquad (12)$$

Again, (12) reduces to $Q\left(\sqrt{\frac{E_{b,avg}}{\mathrm{N}_0}}\right)$ for the non-dispersive case.

When averaging over the data vector, the analogous expression for (10) becomes,

$$P_{b0}=\frac{1}{2^{L-1}}\sum_{j=1}^{2^{L-1}} Q\left([\mathrm{V}-\sum_{i=1}^{L-1} d_{n-1}{}^{(j)}\, h_i]\sqrt{\frac{4.E_{b,avg}}{\mathrm{N_0}}}\right). \quad (13)$$

Finally, the total bit error probability would be $P_b=\frac{1}{2}P_{b0}+\frac{1}{2}P_{b1}$ as shown below in (14).

$$\mathrm{P_b}=\frac{1}{2}\left\{\frac{1}{2^{L-1}}\sum_{j=1}^{2^{L-1}} Q\left([\mathrm{V}-\sum_{i=1}^{L-1} d_{n-1}{}^{(j)}\, h_i]\sqrt{\frac{4.E_{b,avg}}{\mathrm{N_0}}}\right)\right\}+\frac{1}{2}\left\{\frac{1}{2^{L-1}}\sum_{j=1}^{2^{L-1}} Q\left([h_0+\sum_{i=1}^{L-1} d_{n-1}{}^{(j)}\, h_i - V]\sqrt{\frac{4.E_{b,avg}}{\mathrm{N_0}}}\right)\right\} \quad (14)$$

This equation enables us to find the bit error probability of OOK for an arbitrary dispersive channel, at any SNR, given the channel's discrete-time equivalent impulse response.

6.2 Simulation Results

To verify the analysis, we developed a Monte Carlo simulation in Matlab where we send 80 million bits through a channel and make hard bit decisions and count the number of bit errors at the receiver side. The channels we employ are represented by the channel impulse response coefficients extracted from HFSS simulations. The channel coefficients represent specific channels from the discone, log-spiral, and monopole wideband models that were analyzed in the previous chapter, and which showed the best performance. We have chosen a low dispersion and a high dispersion channel from both models for illustration.

In Figure 6.2, the error probability equation (14) was numerically evaluated and plotted (green dots) on the same graph with the theoretical bit error rate for OOK for a non dispersive channel (solid red curve) and the Monte-Carlo simulated error probability (blue curve) vs. E_b/N_0 for a 10 GHz diagonal discone channel in the frequency range 140-

150 GHz. A SNR of 23 dB is needed to achieve a BER of 10^{-14}. We can see that the analytical and simulated curves are in excellent agreement. The delay spread for this "low dispersion" channel is one fourth the bit time *T*.

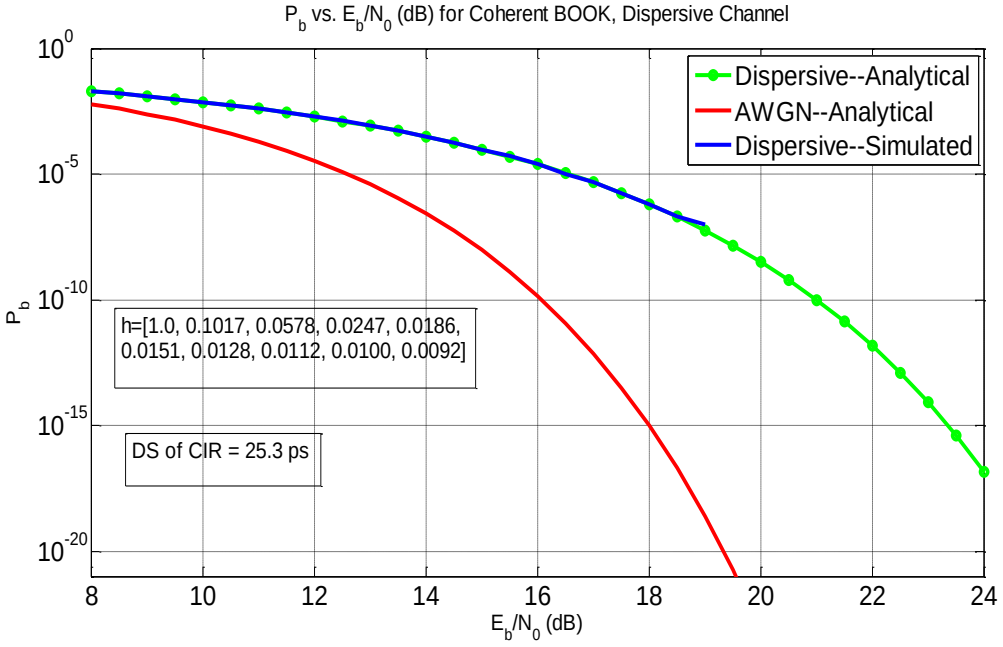


Figure 6.2. Simulated and analytical probability of bit error vs. E_b/N_0 for a 10 GHz "low dispersion" discone diagonal channel.

Figure 6.3 shows error probability vs. E_b/N_0 for high the high dispersion side-to-side discone channel. From Figure 6.3, we can see that for this channel, where the RMS-DS is larger than *T*, the bit error rate does NOT improve with a higher SNR and actually remains constant at a very high value of around 0.4. The theoretical and simulation results are again in very good agreement. The results of Fig. 6.3 clearly show that for some WiNoC channels, equalization must be used to make the link quality acceptable.

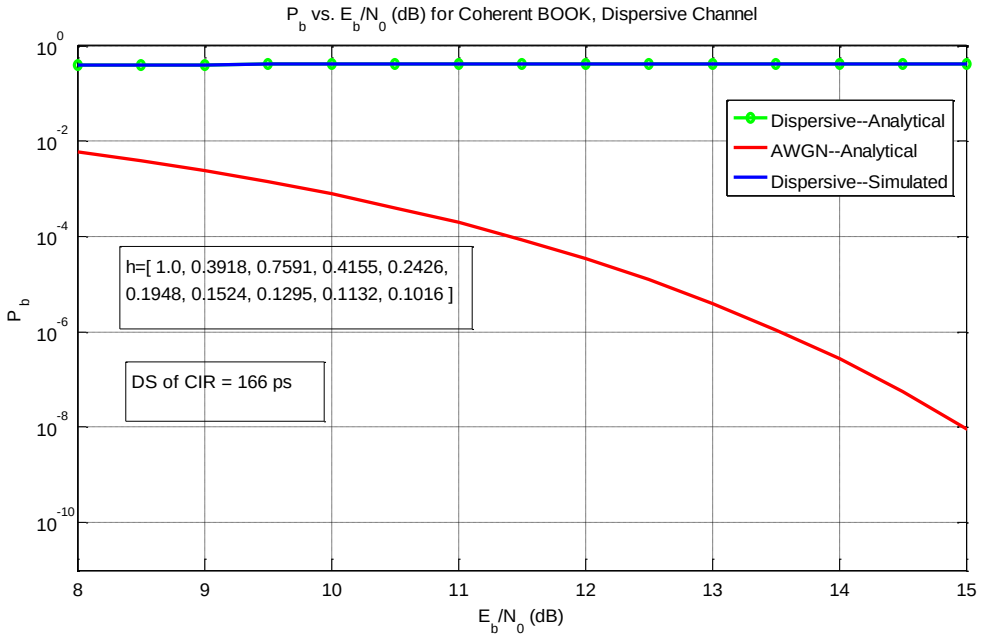


Figure 6.3. Simulated and analytical probability of bit error vs. Eb/N0 for a 10 GHz "highly dispersive" discone side channel.

Next, we present the probabilty of error results of channels from the log-spiral model. We see in Figure 6.4 that the low-dispersion *side-to-side* channel achieves a similar probability of error compared with the discone's *diagonal* channel and also requires around 23 dB to achieve a BER of 10^{-14}. Similarly, the channel delay spread is around one fourth the bit time *T*. Figure 6.5 shows that for the diagonal high dispersion log-spiral channel, where the RMS-DS is ~ 1.5*T*, the bit error rate also does NOT improve with a higher SNR and actually remains constant at a very high value of around 0.34. As before, the theoretical and simulation results for the low and high dispersion log-spiral channels are in very good agreement.

Note that for Figures 6.2 and 6.4, the simulation curve does not cover the whole SNR range. This is simply because at higher SNR levels, the probability of bit error decreases to values that mandate a *very* large number of bits in order to obtain reliable

error probability estimates. Due to memory limitations, this is not feasible. It is important to note that for these low-dispersion channels, compared to the non-dispersive AWGN channel, we need around 5 dB more power (or, bit energy) to attain our BER goal of 10^{-12} to 10^{-14}. The corresponding SNR levels to attain our BER goal hence have to be from 22 to 23 dB and from 21.5 to 22.5 dB, according to the analysis, for the "low-dispersion" diagonal discone channel and "low-dispersion" side-to-side log-spiral channel, respectively. Such levels might be challenging to achieve since power consumption should be minimized, in keeping the WiNoC as power efficient as possible.

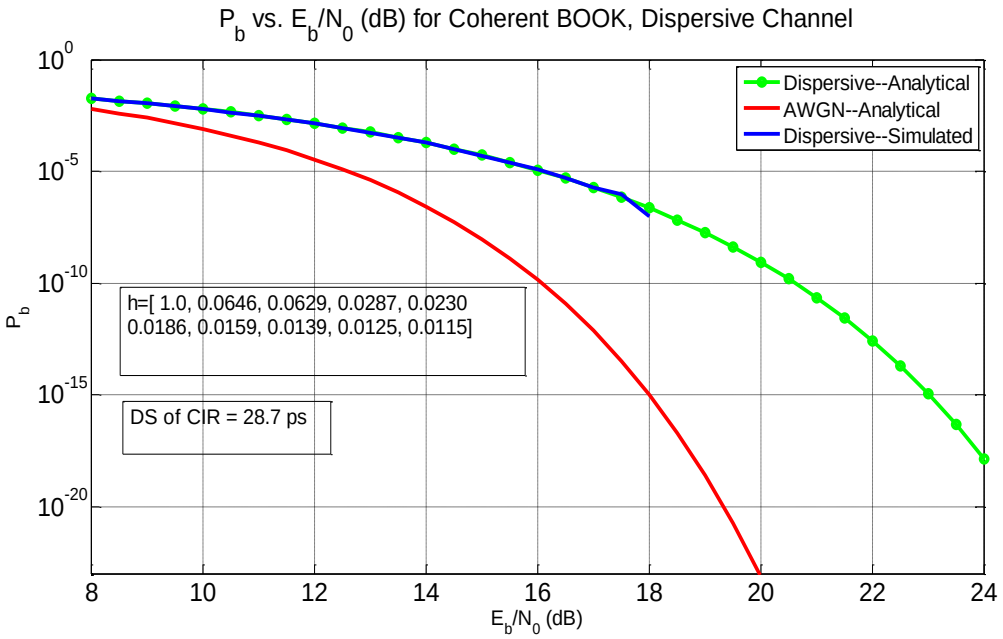


Figure 6.4. Simulated and analytical probability of bit error vs. Eb/N0 for a 10 GHz "low dispersion" log-spiral side-to-side channel.

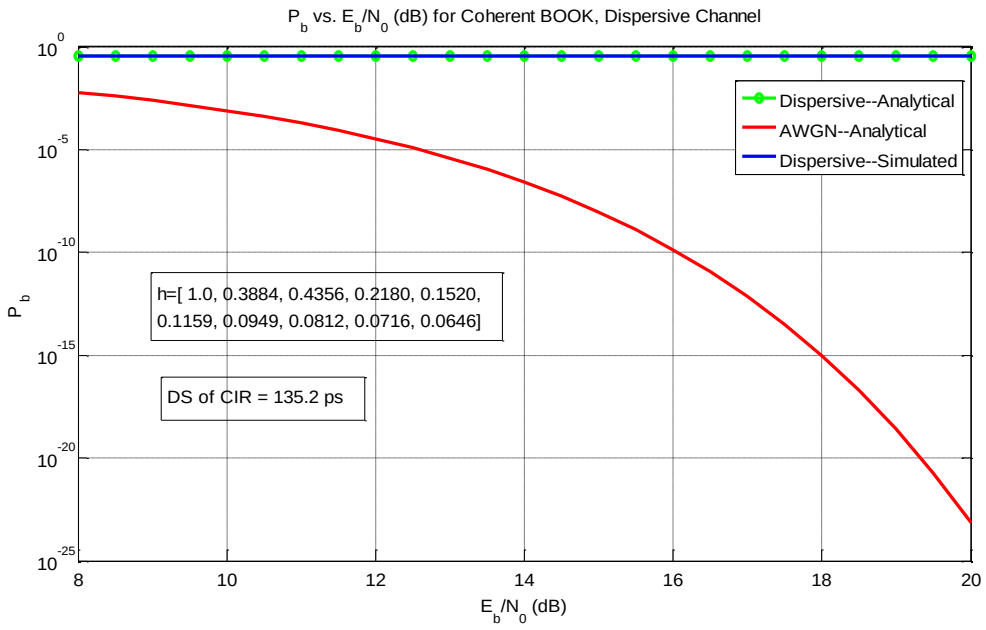


Figure 6.5. Simulated and analytical probability of bit error for a 10 GHz "high dispersion" log-spiral diagonal channel.

We show next the probability of error performance for channels from the monopole model. In Figure 6.6, the low-dispersion diagonal channel, whose delay spread is around one third the bit time *T*, requires an SNR between 23.5 dB and 24.5 dB to achieve our BER goal of 10^{-12} to 10^{-14}. Figure 6.7 shows that for the diagonal high dispersion monopole side channel, where the DS is slightly larger than the *T*, the bit error rate also does NOT improve with a higher SNR and actually remains constant at a very high value of around 0.28. As before, the theoretical and simulation results for the low and high dispersion monopole channels are in excellent agreement.

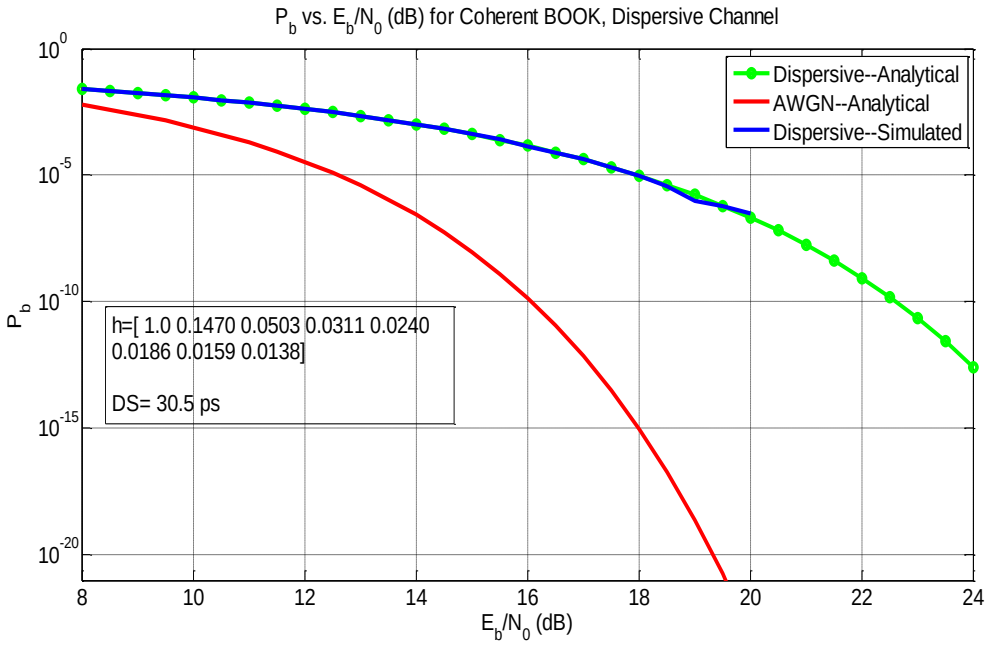


Figure 6.6. Simulated and analytical probability of bit error vs. E_b/N_0 for a 10 GHz "low dispersion" monopole diagonal channel.

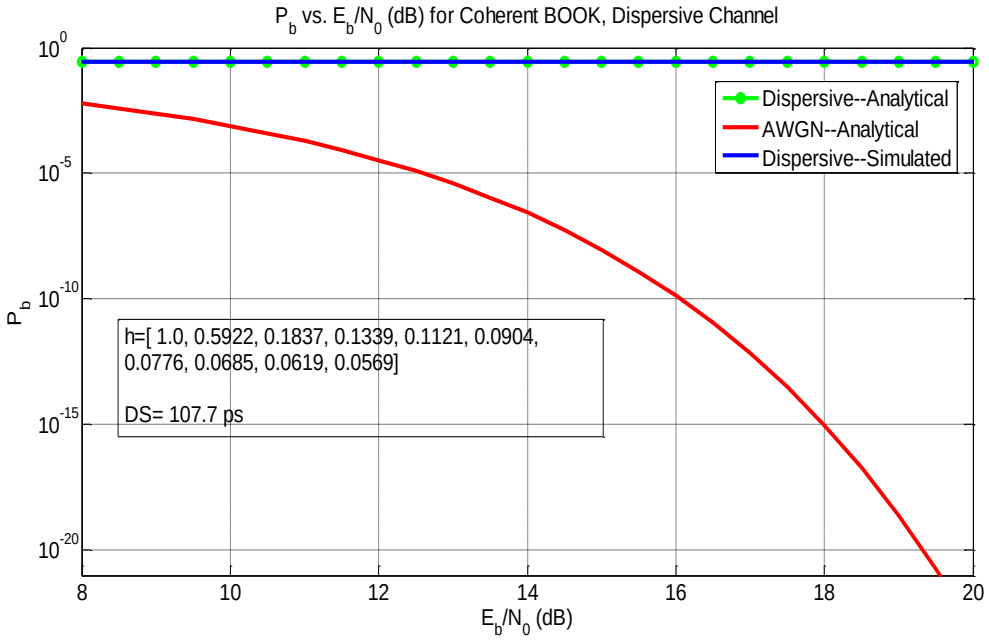


Figure 6.7. Simulated and analytical probability of bit error vs. Eb/N0 for a 10 GHz "high dispersion" monopole side channel.

6.3 Equalization Effect

For the high data rates we are targeting (≥ 10 Gb/s), even small amounts of dispersion can be performance limiting. As was shown in the previous section, delay spreads greater than or equal to the bit time *T*, (≥ 100 ps) can cause major distortion and lead to BER floors. In order to remedy this performance degradation caused by the high dispersion, we investigate the use of zero-forcing equalization. Other means of decreasing the dispersion and suppressing the multipath components (MPC) include decreasing the channel bandwidth and using more directive antennas, but since equalizers operating at these bit rates are currently feasible (although not necessarily implemented on WiNoCs), our focus here is on equalization. One other method is the use of multicarrier modulation, with subcarrier bandwidth selected to incur a flat channel response over each subcarrier. Such modulations are commonly used, but induce other challenges, including a high peak-to-average power ratio and the power consumption of discrete Fourier transformations at both transmitter and receiver. These power considerations likely preclude the use of multicarrier modulations in the near term.

Since the low-dispersion example channel's attained reasonably good performance without equalization (albeit with an energy penalty), we consider herein the highly dispersive channels from the monopole, discone, and log-spiral models that were analyzed in the previous section.

In Figure 6.8, a 21 tap zero-forcing equalizer decreases the delay spread of the highly dispersive unequalized channel, exhibiting the BER floor, to 33.4 ps. As for our goal BER of 10^{-12} to 10^{-14}, the 21 tap equalizer achieves those values—with an SNR between 17.5 dB and 19.5 dB—2 dB less SNR than that required by the 15 tap equalizer.

We can see in Figure 6.9 that an equalizer of at least 21 taps is needed to remove the BER floor, and a 41 tap ZF equalizer is required to decrease the RMS-DS of this specific channel to 36.2 ps. A 15 tap Decision Feedback Equalizer (DFE) equalizer, consisting of 10 feed-forward taps and 5 feedback taps, achieves the same delay spread. An SNR level between 17 dB and 18 dB is needed to achieve our BER goal with the 41 tap ZF equalizer. This SNR is ~ 5 dB higher for the 25 tap ZF equalizer and it ranges between 21.5 and 22.5 dB. From Figure 6.10, we see that a 25 tap ZF equalizer reduces the delay spread of the highly dispersive unequalized channel to 22.7 ps and that a SNR level between 17 dB and 18 dB is needed to achieve our goal BER of 10^{-12} to 10^{-14}. As for the 15 tap DF equalizer, it reduces the channel delay spread to 71.4 ps and requires a SNR level between 19.5 dB and 20.5 dB to achieve our targeted BER.

This analysis shows the importance of equalization for the WiNoC design. Even though equalizers will occupy valuable area and consume some amount of power, they are mandatory to remedy the intersymbol interference caused by the highly dispersive channels and to achieve the rather challenging BER of 10^{-12} to 10^{-14}. It is important to note that forward error correction codes (FEC) can be used by encapsulating the data stream in "code words" with extra bits so that the decoder can reduce or correct errors at the output of the receiver [75]. The improvement in the performance of a digital system that uses FEC can be very valuable and significant, at the expense of either throughput or bandwidth. A large coding gain—the reduction in E_b/N_0 when coding is used compared to the E_b/N_0 needed for the uncoded case at some specific BER—could not only help to decrease the overall power consumption but would also relax the performance

improvement needed by the equalizers. The study of FEC would be a component of future work.

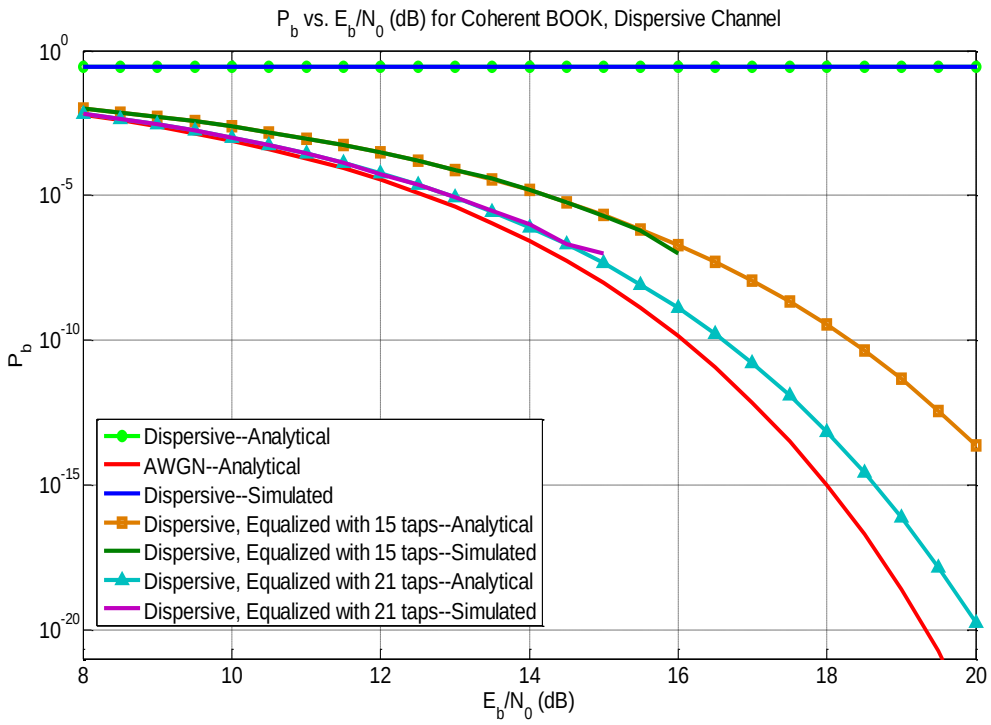


Figure 6.8. Simulated and analytical probability of bit error vs. Eb/N0 for a 10 GHz "high dispersion" monopole side channel with equalization.

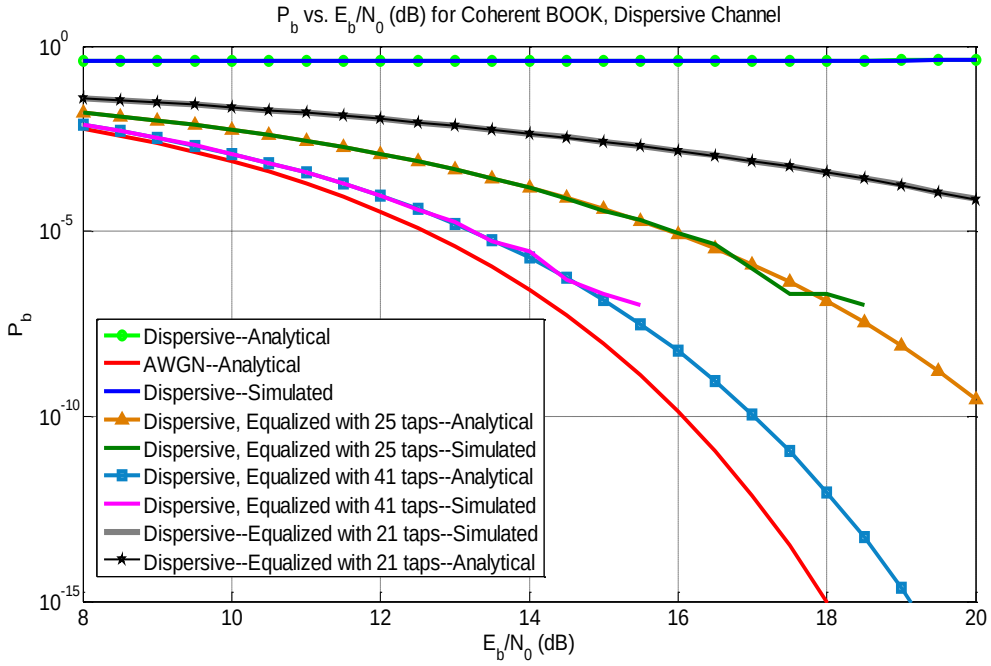


Figure 6.9. Simulated and analytical probability of bit error vs. E_b/N_0 for a 10 GHz "high dispersion" discone side channel with equalization.

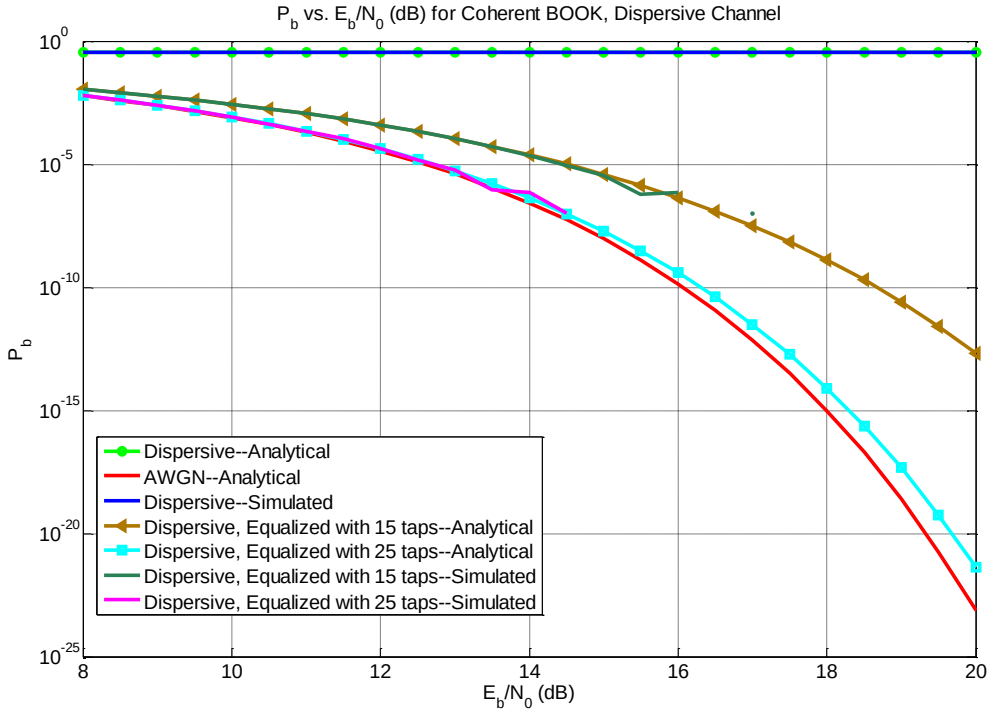


Figure 6.10. Simulated and analytical probability of bit error vs. E_b/N_0 for a 10 GHz "high dispersion" log-spiral side channel with equalization.

Chapter 7

Conclusions and Future Work

In this dissertation, we have investigated the topic of intra-chip wireless channel modeling and resulting link performance for WiNoC applications. Our analysis employed primarily simulations in HFSS®, the 3-Dimensional full wave simulation software from Ansys®, in addition to a theoretical analysis and simulations in Matlab® that allow us to quantify performance metrics pertaining to the WiNoC. In this chapter, the main conclusions and discussion of possible future research areas for academia and industry are presented.

7.1 Dissertation Conclusions

The main objective of our research was to present realistic wireless channel characteristics, specifically path loss and dispersion, in the WiNoC setting, in addition to analyzing the performance of several antenna types in the intra chip environment. We also presented results for the throughput of frequency division multiple access schemes based upon the wireless channel and antenna characteristics. These results were used by the other members of our research group for their work on realistic transceiver devices and computer architecture, to enable some of the first available, practical, WiNoC designs.

For our channel and antenna work, the analysis was carried out by setting up specific models and simulating them in HFSS®. Moreover, we presented a theoretical analysis that enables us to compute the bit error rates that correspond to a given known channel represented by its impulse response. We also showed the efficacy of equalization through zero forcing (and some decision feedback) equalizers on specific highly dispersive channels in order to reach acceptable delay spread (RMS-DS) values to ensure ISI-free communication.

We simulated six antenna models in HFSS with horizontally and vertically polarized antennas. The printed and upright antennas that were used consisted of inherently narrowband and inherently wideband types. The printed narrowband antennas were half wavelength dipoles, whereas the wideband printed antennas were bowties and log spirals. For the vertically polarized "narrowband" antennas, we chose quarter wavelength monopoles, whereas the vertically polarized wideband antennas simulated were discones and helical antennas. A seventh hybrid system model consisting of monopoles and printed dipoles together was simulated in order to investigate the possibility of using both types of antennas at the same time by taking advantage of the cross polarization isolation between them.

For the narrowband antennas, the monopoles clearly outperform the printed dipoles. They achieve a higher total bit rate of 33 Gb/s, 5 Gb/s more than that of the printed dipoles, and their insertion loss variation across the 40 GHz frequency span is 20 dB compared to 75 dB for the printed dipoles. The frequency range where the printed dipoles' return loss is under -10 dB is only 2 GHz compared to the whole frequency span of 40 GHz for the monopoles. This can be explained by the fact that the monopoles we

simulated are thicker than a “thin wire” at the operating frequency of 150 GHz, yielding a rather wideband characteristic. We also observed that the diagonal channels between the monopoles exhibit less insertion loss variation and consequently less dispersion than the side-to-side channels. The opposite is true for the printed dipoles.

As for the wideband antennas, the performance of the discones and helixes is comparable. Although both achieve approximately the same total bandwidth—33 GHz for the discones and 35 GHz for the helixes—the maximum single channel bandwidth for the discones occurs at an insertion loss of 17 dB compared to an insertion loss of 25 dB for the helix’s maximum single channel bandwidth. Thus, the discones are the more power efficient of the vertically polarized wideband antennas. Power efficiency is a very valuable and sought after characteristic in the WiNoC environment and for that reason the discones are superior to the helixes.

On the other hand, there is a clear winner among the printed wideband antennas and it is the log-spiral. Not only does it achieve a higher total bandwidth (33 GHz to the bowtie’s 24 GHz) but it is also considerably more power efficient than the bowtie. Its maximum single channel bandwidth of 14 GHz occurs at an insertion loss of 44 dB whereas the bowtie’s maximum single channel bandwidth of 9 GHz incurs an additional 14 dB of insertion loss. It is important to note that manufacturability of the upright antennas is a challenging task at such high operating frequencies, especially if we want to keep them rigid. From this standpoint, a winding helix or discone would be more complicated to fabricate than a cylindrical monopole that just consists of an upright wire with a certain thickness and length. Thus, with their high performance and power efficiency traits in this environment, we believe the monopoles would be a preferred

candidate for a possible manufacturing process or empirical test in the future. As for the printed antennas, with the abundance and advancements in printed technologies, we believe that the horizontally polarized antennas might be more easily manufactured, but due to their inferior performance and power efficiency, vertically polarized antennas are superior candidates in the WiNoC setting.

The analysis we have done to investigate the performance of OOK through a dispersive channel, where we found an analytical expression that was evaluated numerically, showed the importance and need for equalization in the WiNoC. It is known that highly dispersive channels with large delay spreads exhibit BER floors. Equalization remedies the ISI caused by such highly dispersive channels and decreases the delay spread. However, some channels require a fairly large number of ZF equalizer taps to achieve the targeted BER of 10^{-14}. Equalizers would certainly occupy valuable area and consume additional power but are necessary for the highly dispersive channels. Our main focus in this research was using ZF equalization, and we showed that with more effective non-linear equalization such as a DFE, the equalizers needed to achieve our targeted BER would be significantly less complex (require a smaller number of taps) and hence consume less power and area.

In all of our designs that we have simulated, the center frequency was 150 GHz with a frequency range of 40 GHz. Scaling this center frequency upwards would not only achieve higher desired data rates in the WiNoC (as we have shown in Appendix D) but also make the structures even smaller and thus, consume less area. However, with such frequency increase comes several challenges: first, the technology to design RF devices and circuitry that operate at several hundreds of GHz to a few THz is still maturing and

second, the actual fabrication of such systems might need the use of non-coventional and innovative methods that are currently still under research.

7.2 Future Work

Possible extensions of this dissertation work are listed below:

- HFSS® simulations to represent the WiNoC environment were very helpful in gathering this dissertation data. Setting up our models and simulating them in another EM solver software, e.g. FEKO®, to compare with the results produced by HFSS®, would provide an opportunity to cross check and validate the results. Also, this process would allow us to compare the performance and solution time of different EM solvers and decide which one is more suitable for specific environments.
- An even better way of validating the HFSS® results is by fabricating one of the models and measuring the insertion and return losses with a vector network analyzer (VNA). At our chosen design frequency of 150 GHz, the cost of such an empirical setup can be very high. Even by halving the center frequency to 75 GHz, this procedure can still be quite expensive. This would be the optimal option to verify the HFSS® results we generated. Our models might have to be re-simulated by replacing the potentially difficult-to-manufacture air gap in our layer stack up by one or several dielectric layers. We used an air gap because it provided the best results and because additional dielectric layers would increase the numerical solution time dramatically.

- In our FDMA scheme, we assumed perfect filtering. Designing actual filters and reassessing the total throughput would be required for a realistic assessment of WiNoC throughput. Filters with a sharp cutoff would be of a high order and hence would possibly occupy valuable area, and these would also induce additional insertion loss. Thus, quantifying how much area and power these filters would consume would be of paramount importance for the overall power efficiency and area footprint of the WiNoC. Studying the use of companion (high-rate) digital filtering to augment the RF filtering would also be of value. Finally on this, use of a more stringent criterion than our "2 dB amplitude slope" would be of value to assess practical WiNoC attainable bandwidths.
- Equalization is crucial to mitigate the highly dispersive channels in the WiNoC. It is also important to actually design and evaluate the power consumption and area consumed by the equalizers. DFE's perform better than ZF equalizers and generally require a smaller number of taps to achieve a certain target delay spread, but because of the feedback part of the equalizers can be more challenging to design and maintain their stability. A complete characterization of equalizers for WiNoC's would be a very valuable addition to this research.
- The modulation scheme we use in this research is BOOK. This modulation scheme is very simple and power efficient. In future research, other modulation schemes, such as DPSK, QPSK, or even higher-order and multi-carrier modulations should be investigated. Channel coding is also a valuable

future topic to be investigated. It would relax the requirements that need to be satisfied by the equalizers and would allow achieving the target BER at a much lower signal to noise ratio, at the expense of some power dissipation and circuit area.

- Multipath dispersion in the WiNoC environment is performance limiting. A future venue that would be worthwhile exploring is simulating models with more inherently directional antennas such as horn antennas or arrays of them. We envision that a micro electromechanical system (MEMS) horn array would provide a very narrow beam that can be steered in any desired direction and that would result in a very low dispersion communication.
- The multiple access schemes that we have presented were for the maximum data rate cases. Devising simultaneous time division (TD) and frequency division (FD) multiple access schemes would be more practical and an important WiNoC-multiple access topic to be researched in the future.
- Since with our ceramic cover design there will be radiation leaking beyond the chip, quantifying this leakage and ways to mitigate it would be a valuable future research topic especially to allow operation with future chip-to-chip wireless communications applications. Moreover, the high gain and low beam-width characteristics of quadrupole and octupole antennas might make them attractive candidates for future research pertaining to WiNoCs.

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Appendix A-Verifying the Free Space Propagation Model in HFSS

The free space propagation model is the simplest model that describes the propagation of electromagnetic waves in an unbounded medium. The Friis transmission equation describes this model and is as follows:

$$G = \frac{P_r}{P_t} = G_t G_r (\frac{\lambda}{4\pi d})^2 \quad (1)$$

where G is the transmission gain of the channel, P_r is the received power, P_t is the transmitted power, G_t and G_r are the transmitter and receiver gains, respectively, d is the distance between the antennas and λ is the wavelength of the electromagnetic wave.

The antennas are assumed to be perfectly aligned and thus no polarization losses are included. Also, the antennas are perfectly matched with no impedance mismatch losses.

To verify this model in HFSS [76], two half-wavelength dipoles operating at 60 GHz were used; we also verify the result at 600 GHz. The simulated dipoles were fed through a lumped port, a type of waveguide or transmission line that supports a single TEM mode with a uniform electric field on its surface and this is used to excite the structures in HFSS. The impedance of the port was 72 Ω and this resulted in a very small return loss (scattering parameter S_{11}) of approximately -40 dB meaning that the reflected power would be 0.01 percent (10^{-4}) of the incident power. The dimensions of the feeding port were 0.037 mm ×0.074 mm, where the width of the port is λ/133 from the HFSS

design kit specifications. The length of the port is the diameter of the dipole. The dipoles are simulated as being made of perfect electric conductor (PEC) material. An optimetric analysis, a procedure in HFSS that allows the variation of parameters and variables, is performed where the distance between the transmitter and receiver was varied: distance ranged from 30 to 80 mm with a 1 mm increment for the antennas operating at 600 GHz, and from 50 to 100 mm with a 1 mm increment for the 60 GHz case.

The simulated and theoretical path loss results versus distance are shown in Figure A.1. As can be seen from the figure, agreement between theory and simulated results is excellent. Table A.1 quantifies this agreement for several values of distance.

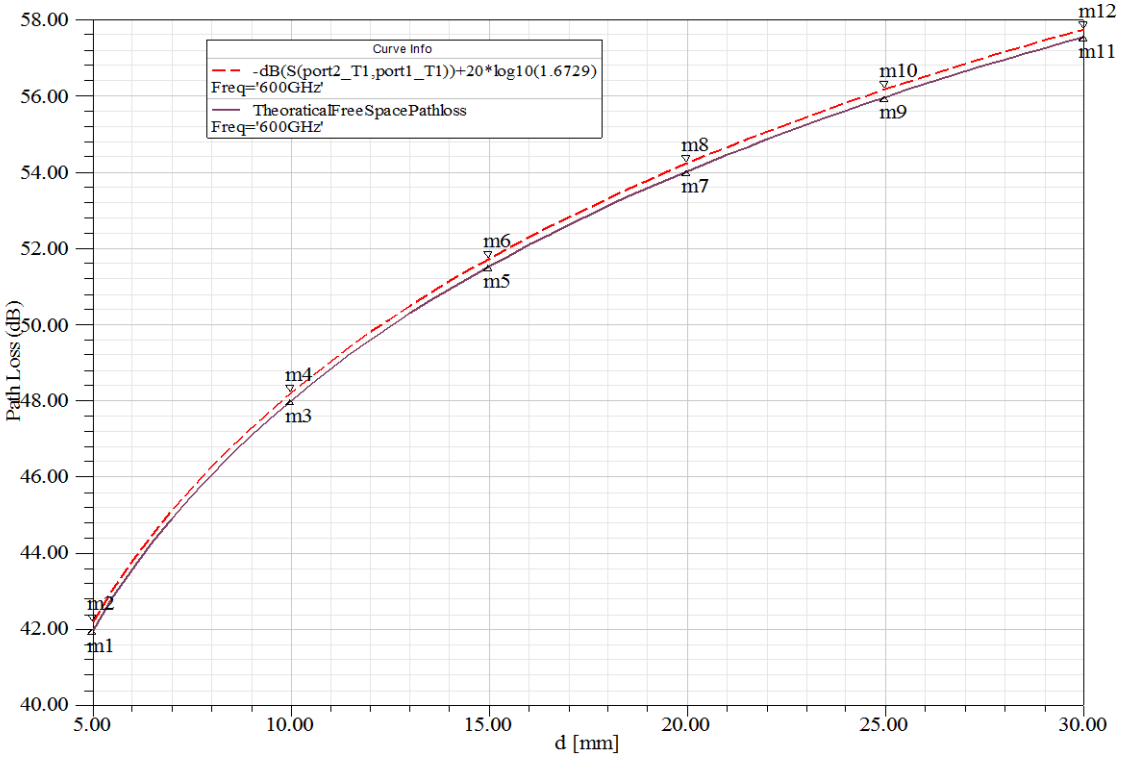

Figure A.1. Path loss vs. distance, both simulated (dashed) and theoretical (solid) for 600 GHz frequency, two half-wavelength dipoles.

Table A.1. Difference between Analytical and Simulation Results for different distances at 600GHz

Distance (mm)	Analytical Loss (dB)	Simulated Loss (dB)	Difference (dB)
5	41.99	42.11	0.12
10	48.01	48.21	0.2
15	51.53	51.73	0.2
20	54.03	54.23	0.2
25	55.96	56.16	0.2
30	57.55	57.75	0.2

According to [39], the transmission gain (reciprocal of path loss) in terms of the scattering (*S*) parameters is

$$G_a = \frac{Pr}{Pt} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} = G_t G_r \left(\frac{\lambda}{4\pi r}\right)^2 e^{-2\alpha r}, \quad (2)$$

Since the antennas are in vacuum, the material loss parameter α=0. The simulated antenna gains were 1.6729=2.23 dBi. As seen from Figure A.1, the simulated and theoretical curves are in very good agreement and within are within 0.1-0.2 dB of each other. Also from Figure A.2 and Table A.2, the simulation and analytical results are in very good agreement and within 0.2 dB for the 60 GHz frequency.

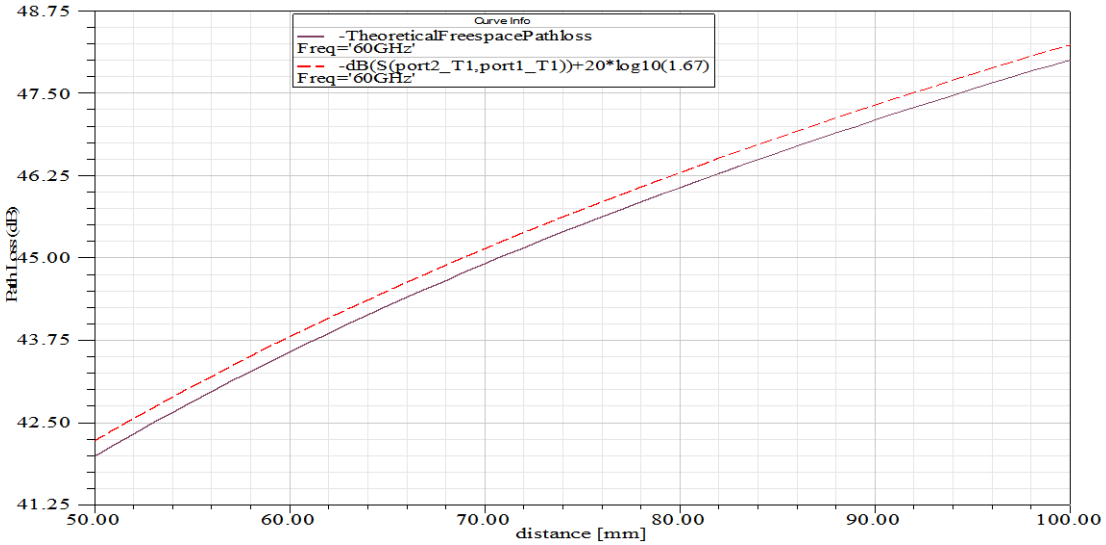

Figure A.2. Path loss vs. distance, both simulated (dashed) and theoretical (solid) for 60 GHz frequency, two half-wavelength dipoles.

Table A.2. Difference between Analytical and Simulation Results for different distances at 60 GHz

Distance (mm)	Analytical Loss (dB)	Simulated Loss (dB)	Difference (dB)
50	41.99	42.22	0.23
60	43.57	43.8	0.23
70	44.91	45.14	0.23
80	46.07	46.29	0.22
90	47.09	47.32	0.23
100	48.01	48.23	0.22

The simulated (elevation) radiation pattern of the half-wave dipole is shown in Figure A.3. This result is in perfect agreement with the theoretical gain of a half wavelength dipole, equal to 1.67=2.22 dBi. Since the free space model assumes that the environment through which the electromagnetic waves propagate is a vacuum, it has limited applicability in practical applications where there are almost always obstructions in the propagation path.

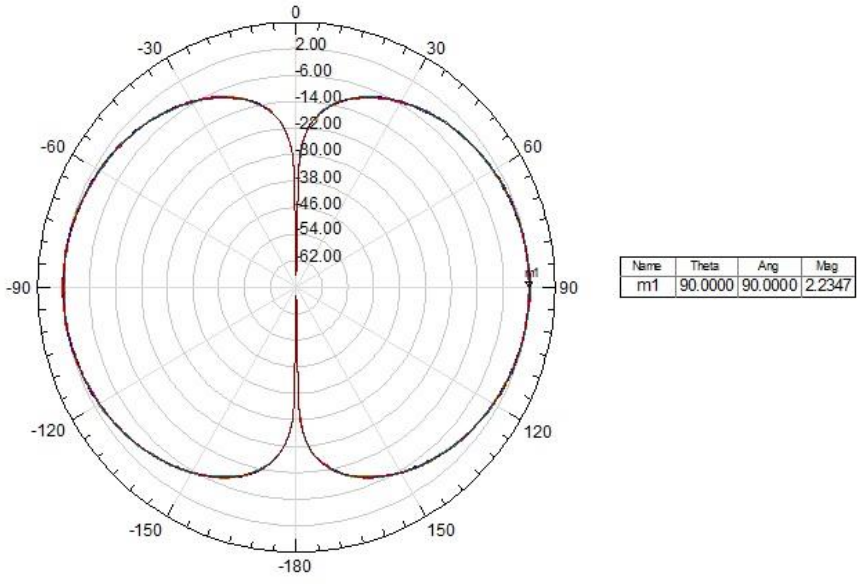

Figure A.3. Dipole radiation pattern in dBi.

Appendix B-Verifying the Two-Ray Propagation Model in HFSS

1. Analysis

Since the free space propagation model applies only under certain specific conditions, it is rarely used in practical situations. A more practical model in many cases is the two-ray model, where the propagation occurs between two elevated antennas over a reflecting surface. In typical terrestrial communication settings this reflecting surface is the ground. This model considers both a line-of-sight (LOS) and ground reflection path between the transmitting and receiving antennas. Fig B.1 (adapted from [77]) depicts the two-ray model where E_i is the incident electric field impinging on the surface, E_g is the ground reflected component of the electric field, E_{LOS} is the line of sight component, θ_i and θ_o are the incidence and reflection angles that are equal according to Snell's law, h_t and h_r are the heights of the transmitting and receiving antennas, respectively, and d is the separation between them.

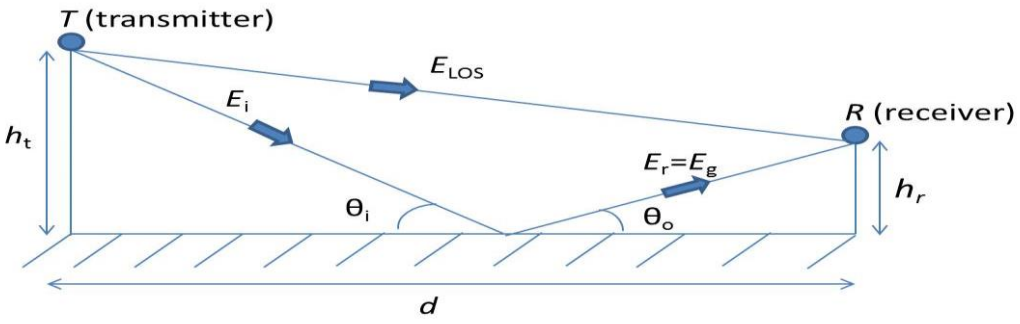

Figure B.1 Two-ray ground reflection model.

From [78], the total electric field at the receiver is

$E_{TOT}=E_{LOS}(1+\rho exp(-j\Delta\phi))$ (1)

where $\rho=|\rho|\exp(j\Phi)$ is the complex reflection coefficient of the reflecting surface and $\Delta\phi$ is the phase difference between the line-of-sight and reflected components at the receiver.

However, a more general form of (1) takes into account the antenna gains of the transmitter and the receiver in the respective directions and thus, (1) becomes

$$E_{TOT}=\left(\sqrt{Gain(\theta_{LOS})}\right)^2 \frac{E_{LOS}}{d}+\left(\sqrt{Gain(\theta_i)}\right)^2 \frac{E_{LOS}}{d+\Delta R}\rho exp(-j\Delta\phi), \quad (2)$$

where $Gain(\theta_{LOS})$ is the antenna gain at the declination angle along the direct path and $Gain(\theta_i)$ is the antenna gain at θ_i in the direction of the surface reflection. Note that each component of the total electric field is scaled by two gain terms, one at the transmitter and one at the receiver.

Via basic trigonometry, the length of the direct path is $R_1=\sqrt{(h_t-h_r)^2+d^2}$ and the length of the reflected path is $R_2=\sqrt{(h_t+h_r)^2+d^2}$.The corresponding path length difference is then $\Delta R= R_2 - R_1$ and from this the phase difference between the two components is

$$\Delta\phi=\frac{2\pi\Delta R}{\lambda}=\frac{2\pi(\sqrt{(h_t+h_r)^2+d^2}-\sqrt{(h_t-h_r)^2+d^2})}{\lambda}. \quad (3)$$

For our verification procedure in the HFSS simulation, we assume a perfect electric conductor (PEC) ground surface and vertically polarized antennas; this yields ρ=1. Equation (1) becomes

$$|E_{TOT}|=2|E_{LOS}|.cos\frac{\Delta\phi}{2} \quad (4)$$

where $\Delta\phi$ is given by (2). The received power is proportional to $\frac{|E|^2}{\eta}$ and thus $P_R=4|E_{LOS}|^2cos^2(\frac{\Delta\phi}{2})\frac{1}{\eta}$, where we obtain $|E_{LOS}|^2$ from the Friis transmission equation: $|E_{LOS}|^2=\eta P_T(\frac{\lambda}{4\pi d})^2 G_T G_R$, where G_T and G_R are the respective gains of the transmitting and receiving antennas. The reflected component also follows the Friis equation both before and after the reflection, thus the total power received relative to the transmit power P_t can be written as

$$\frac{P_R}{P_t} = 4(\frac{\lambda}{4\pi d})^2 G_T G_R \cos^2(\frac{\Delta\phi}{2}) \quad (5)$$

where we have incorporated the antenna gains according to (2).

2. Simulation Results

2.A Path Loss and Antenna Patterns

The simulation configuration consisted of two half-wavelength dipoles operating at 600 GHz above a smooth, infinite PEC ground plane. As with the free-space simulation, the dipoles were fed through lumped ports with an impedance of 72 ohms to insure very low impedance mismatch losses. The antennas were at a height of 10 mm above the ground plane, and the distance ranged from 50 to 500 mm with a 0.5 mm increment. The path loss simulation results and theoretical results are plotted on the same graph in Figure B.2. As seen in Figure B.2, the curves are in very good agreement. The radiation pattern of one of the antennas is shown in Figure B.3 (via symmetry, since the antennas are identical, the patterns are also identical).

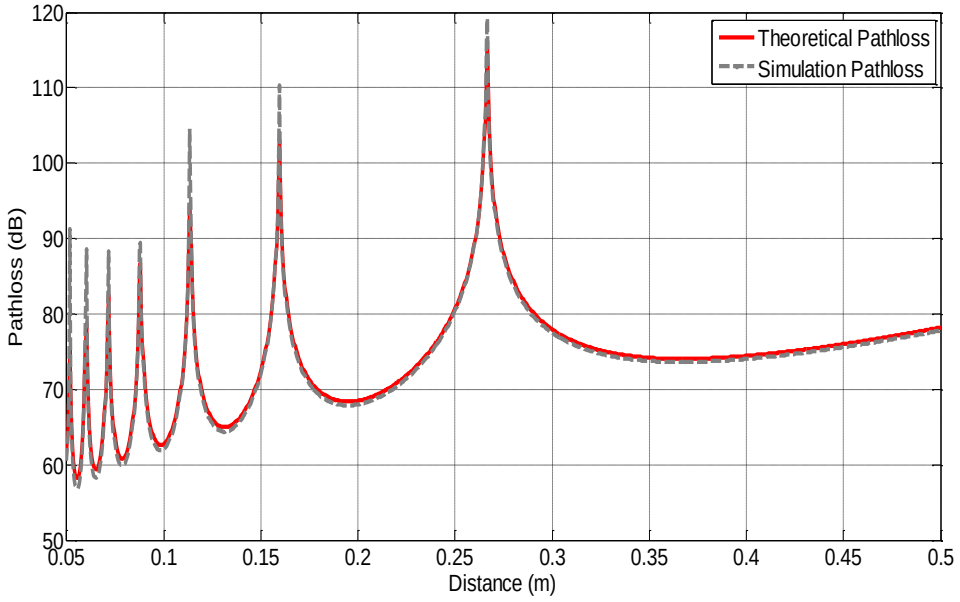

Figure B.2. Path loss vs. distance, both simulated (solid) and theoretical (dashed) for 600 GHz frequency, two half-wavelength dipoles above an infinite PEC ground plane.

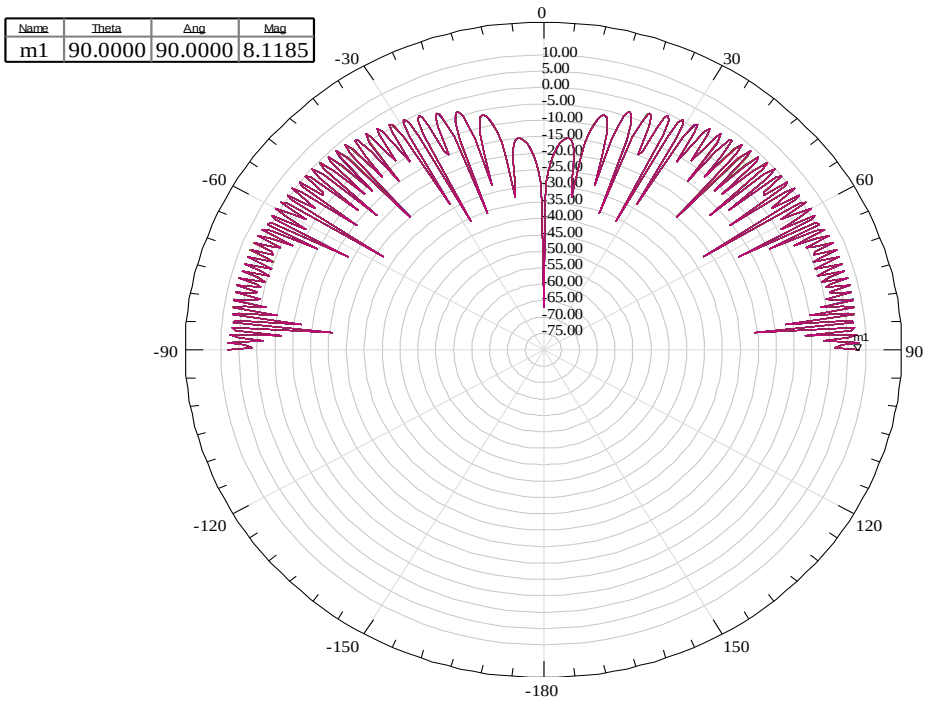

Figure B.3. Radiation pattern (elevation, dBi) for 600 GHz, two half-wavelength dipoles elevated 10 mm above an infinite PEC ground plane.

From [79], the number of lobes N in the pattern of a vertical infinitesimal dipole above a perfect electric conductor plane is,

$$N=\frac{2h}{\lambda}+1. \quad (5)$$

For our case, the height of 10 mm is 20λ. Thus, the total number of lobes would be 41. If counted accurately in Figure B.3, the number of lobes is indeed 41. Moreover, for the sake of clarity and in order to be able to view the lobes more clearly, another simulation was conducted where the heights were 1 mm (2λ); the corresponding radiation pattern is shown in Figure B.4. As seen from Figure B.4, there are 5 lobes, and this is again in agreement with (5).

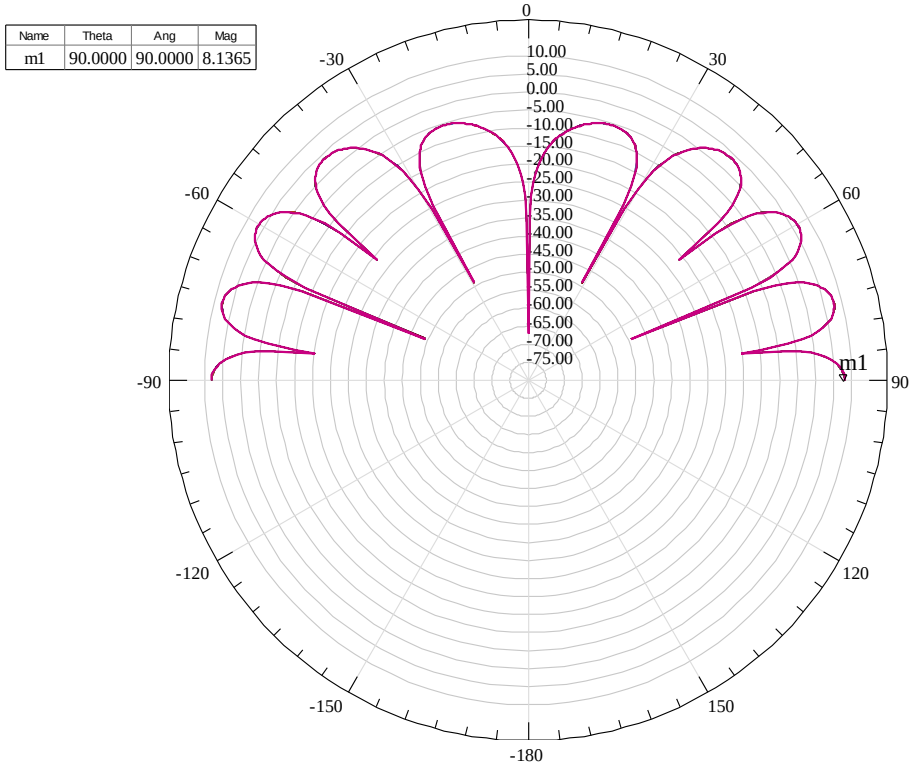

Figure B.4. Radiation pattern (elevation, dBi) for 2 half-wavelength dipoles at 600 GHz, elevated 1 mm above a PEC ground plane.

2.B Time Domain Analysis

The path loss versus distance behavior is a very distinct characteristic of the two ray propagation model. However, another important characteristic of this channel or propagation model is the impulse response. This response should ideally consist of two delayed impulses of appropriate amplitudes. The relative delay depends on the path length difference between the line of sight and reflected components, whereas the amplitudes depend on the antenna gains at the specific heights and distances, and the amplitude of the ground reflection coefficient[5]. We next computed impulse responses versus time for two simulation setups with different distances between the antennas and different heights above the PEC ground plane.

In order to verify the simulation results against the theoretical results, we use (2) since it takes into account the antenna gains at different heights and distances. In its original form, (1) is applicable for grazing incidence situations. Grazing incidence occurs when the incidence angle is very small. Typically, grazing incidence occurs when $d >> h_t$, h_r.

Our first simulation case consists of two half-wavelength dipoles, operating at 600 GHz, at a height of 40 mm above an infinite PEC ground plane and at a separation of d=75 mm. The impulse response is obtained via the inverse Fourier transform of the vector of transmission coefficients (S_{21}) over a certain frequency band. In this case, the bandwidth of this frequency sweep was set to 400 GHz, from 400 to 800 GHz, using a frequency increment of $\Delta f \approx$ 98MHz. This yields a total number of points in the insertion

[5] If the path lengths are substantially different, the LOS and reflected components would also incur different free-space losses; generally this can be ignored when far-field conditions pertain.

loss vector (and impulse response) equal to 4096. Figure B.5 illustrates the impulse response for this case.

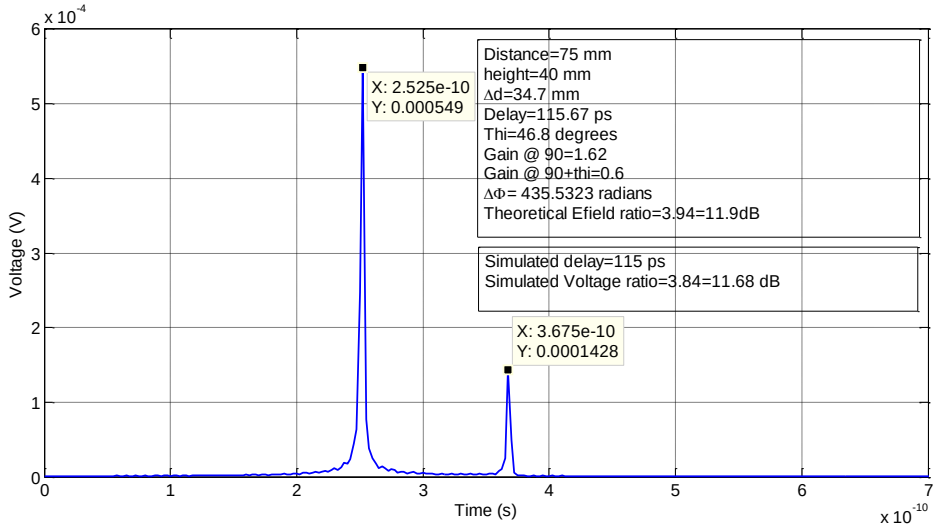

Figure B.5. Impulse response of a channel between two half-wavelength dipoles operating at 600 GHz at a height of 40 mm above an infininte PEC ground plane and a separation of 75 mm.

From Figure B.5, the simulated time delay difference between the components is 115 ps, and the amplitude ratio of the LOS to reflected components is 3.84 or 11.68 dB. For the theoretical values, the path difference for this setup is ΔR=0.0347 m. Consequently the theoretical time delay difference is $\Delta R/c$, which is equal to 115.6 ps. The simulation result is in very good agreement with the theoretical one. For computing the theoretical amplitude ratio of the LOS to reflected components, we take the ratio of the amplitudes of the two terms in (2), i.e., $\frac{\left(\sqrt{Gain(0)}\right)^2 . \frac{E_{LOS}}{d}}{\left(\sqrt{Gain(\theta_i)}\right)^2 \frac{E_{LOS}}{d+\Delta R}} = \frac{\left(\sqrt{Gain(0)}\right)^2 .(d+\Delta R)}{\left(\sqrt{Gain(\theta_i)}\right)^2 .(d)}$. For this geometry setup, the simulation amplitude ratio of 11.68 dB is in excellent agreement with the theoretical ratio of 11.9 dB.

For the second case, we consider the same half-wavelength antennas operating at 600 GHz but this time at heights of 15 mm and a separation of 150 mm. Again the

bandwidth of the frequency sweep was set to 400 GHz, from 400 to 800 GHz, with 4096 points in the insertion loss and impulse response vectors. The impulse response for this case is shown in Figure B.6.

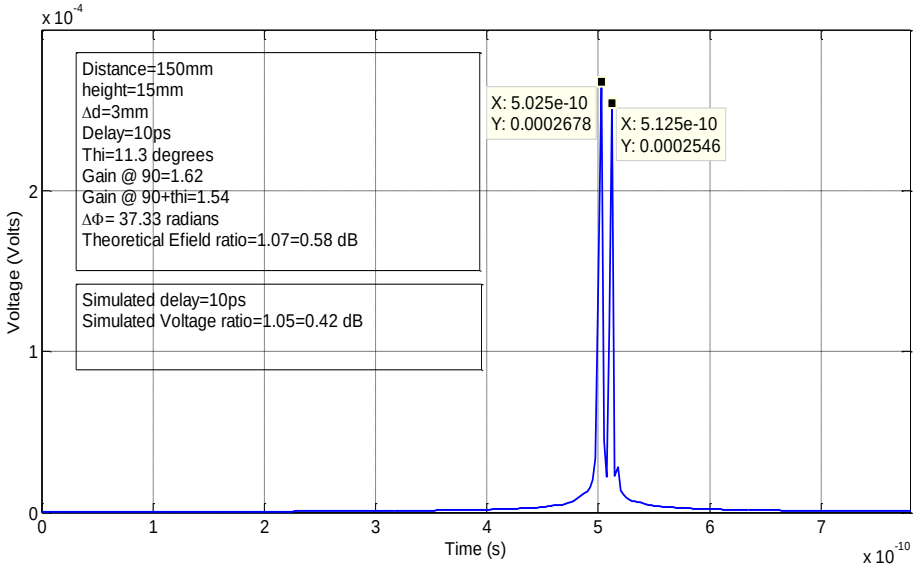

Figure B.6. Impulse response of two half-wavelength dipoles operating at 600 GHz at height of 15 mm above an infininte PEC ground plane and at separation 150 mm.

From Figure B.6, the simulated time delay is 10 ps, and the amplitude ratio of the LOS to reflected components is 1.05 or 0.42 dB. For the theoretical values, the path difference for this setup is ΔR=3 mm and the theoretical time delay is $\frac{\Delta R}{\mathrm{C}}$ and yields a delay difference of 10 ps. We notice that as the distance to antenna height ratio increases, the path length difference decreases and consequently the time delay between the LOS and reflected components also decreases. The theoretical amplitude ratio is 1.07 or 0.58 dB. Again, the simulation and theoretical results are in excellent agreement.

Appendix C-Effect of Insertion Loss Slope variation on RMS Delay Spread

We have in this dissertation used a rather qualitative metric to estimate channel bandwidth when looking at insertion loss (IL) curves. We have adopted the following definition of bandwidth: the range of frequencies where the variation in the insertion loss in less than 2 dB. In this report, we investigate a more quantitative approach to this topic.

Seen in Fig. C.1 is an insertion loss curve for an HFSS® model that consists of 5 monopoles inside of a 20 mm × 20 mm chip with 4 monopoles at each corner and one in the middle of the chip. This specific curve, between two diagonal monopoles, was chosen since it exhibits several and different slope changes which would help us in our investigation. The boxes numbered 1 through 8 represent eight different channels that have different insertion loss changes.

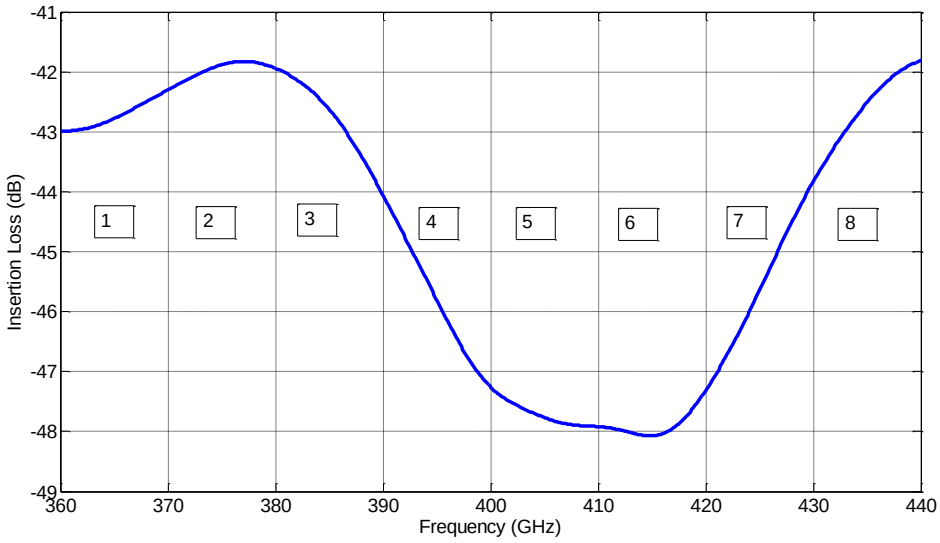

Figure C.1: Insertion loss example

We used 64 frequency points in every 10 GHz frequency span, which sums up to a total of 512 frequency points for the whole 80 GHz range. In Matlab, taking the IFFT of each "10-GHz section" of this transfer function gives us the channel impulse response (CIR) of each of the eight sections which we represent in terms of power delay profiles. With the power delay profiles of each section, we are able to compute the RMS-delay spread pertaining to each section, the reciprocal of which is an approximate measure of bandwidth known as the coherence bandwidth.

For our investigation, we construct an artificial complex insertion loss response to compare it with the simulated one. For the amplitude of the artificial insertion loss curve, we use a straight line approximation with a certain slope over a certain frequency span. As for the phase, we use the same slope as the one exhibited in the simulated insertion loss, hence the phase response is realistic. Once we have the amplitude and phase vectors, we construct the complex artificial insertion loss function and follow the same algorithm to compute the resulting delay spread . It should be noted that the artificial and simulated insertion loss curves have the same length of 64 points. The results are shown in Table C.1.

Table C.1: RMS-DS values for insertion loss curve of Figure C.1.

Channel number	**RMS-DS of simulated IL (in ps)**	**RMS-DS of artificial straight line (in ps)**	**IL slope amplitude over 10 GHz channel (in dB)**
1	0.438	0.436	1
2	0.378	0.440	1
3	0.39	0.393	2
4	0.532	0.529	3.5
5	0.57	0.57	1
6	0.604	0.592	1
7	0.534	0.532	3
8	0.416	0.42	2

Observations:

- First, we see very good agreement between the delay spread numbers resulting from the simulated insertion loss curves and the ones resulting from the artificial linear insertion loss functions.
- Second, we notice a slight variation of delay spread among the eight channels although some channels exhibit a considerably larger insertion loss amplitude variation.
- Third, examining the phase slope of each channel, we notice that it ranges from 1.38 π/10 GHz to 1.62 π/10 GHz for all 8 channels.

To further investigate the effect of the phase slope, we vary the artificial phase slope for different insertion loss slopes and frequency spans. We show the results in Table II and the phase plot, corresponding to the insertion loss curve in Figure C.1, in Figure C.2.

We notice that for the small variations in phase (e.g 0.1π), the rate of increase in delay spread, corresponding to an increase in insertion loss variation, is higher than that for cases where the variation in phase is high (e.g 0.8π). Also, for a fixed insertion loss slope, the delay spread decreases proportionally as the bandwidth increases. We conclude that the phase slope of the insertion loss has a larger effect than the amplitude slope on the delay spread of a specific channel with a certain bandwidth.

Table C.2. Delay Spread for different Insertion Loss Phase and Amplitude Slopes.

phase slope / IL slope	BW=5 GHz RMS-DS (ns)	BW=10 GHz RMS-DS (ns)	BW=20 GHz RMS-DS (ns)
0.1π / 1 dB	3.316	1.65	0.829
0.1 π / 2 dB	3.81	1.9	0.952
0.1 π / 4 dB	5.27	2.63	1.31
0.2 π / 1 dB	6	3	1.51
0.2 π / 2 dB	6.25	3.12	1.56
0.2 π / 4 dB	7	3.5	1.75
0.4 π / 1 dB	10.48	5.24	2.62
0.4 π / 2 dB	10.53	5.26	2.63
0.4 π / 4 dB	10.73	5.36	2.68
0.8 π / 1 dB	14.77	7.38	3.69
0.8 π / 2 dB	14.75	7.37	3.68
0.8 π / 4 dB	14.67	7.33	3.66

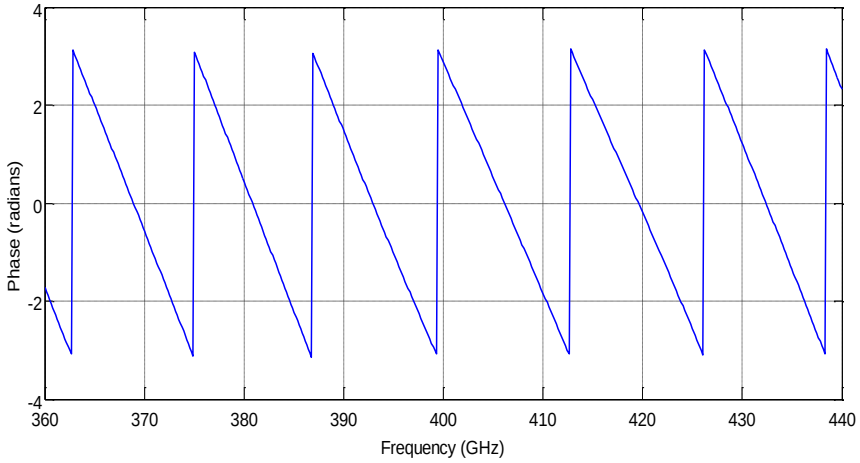

Figure C.2. Phase of Insertion Loss

Appendix D-Bandwidth Scaling of Monopole Model

All results we have simulated for our models pertained to a center frequency of 150 GHz with a frequency span of 40 GHz. We chose this part of the spectrum as a "middle-ground" option to satisfy the largest number of challenges in the three design areas of the WiNoC project—circuits/devices, antennas/propagation, and system/architecture [38]. Here we investigate how the bandwidth achieved by our models, specifically the monopole model, scales with higher/lower center frequencies and larger/smaller frequency spans.

Procedure

We choose the monopole design since it runs faster on HFSS and also because its solution converges at higher center frequencies, especially with the limited computational resources that we have at our disposal. The monopole models also attained some of the best (smallest) insertion losses and delay spreads. The design, simulated at a center frequency of 150 GHz, is the same one depicted in Figure 4.1 except that the substrate thickness is 10 μm and not 100 μm.

We simulate this model at center frequencies (f_0) of 38 GHz, 75 GHz, 300 GHz, and 600 GHz, with frequency spans of 10 GHz, 20 GHz, 80 GHz, and 160 GHz respectively—bandwidth is directly scaled with center frequency. The chip area is 20 mm × 20 mm at 150 GHz and these side dimensions also scale up with decreasing center

frequency and scale down with increasing center frequency. For example, the chip size for the design simulated at 75 GHz is 40 mm x 40 mm, whereas the chip size for the design simulated at 300 GHz is 10 mm x 10 mm. What follows are the results in terms of insertion loss and bandwidth achieved for the monopole model at the center frequencies mentioned.

Monopole Model Design at f_0= 38 GHz

A top view of the design with all its dimensions is shown in Figure D.1. We show in Table D.1 the dimensions for all models simulated at different center frequencies. The entries "d_S", "d_D", and "d_E" stand for the side-to-side separation between the antennas, diagonal separation between the antennas, and the separation of the antenna from the edges of the chip respectively. Parameter B_{xy} denotes the bandwidth of the channel between antennas x and y.

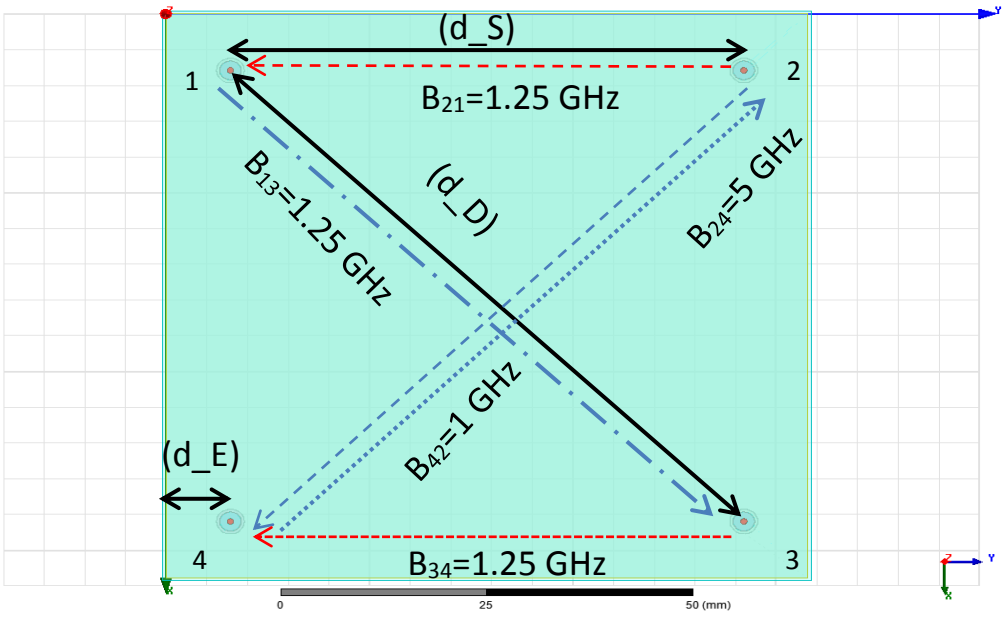

Figure D.1. Monopole model simulated at 38 GHz.

We employ the same definition for bandwidth as used for our 150 GHz designs: specifically, it is the range of frequencies for which $\Delta|S_{i1}|<2$ dB[6] for i=2, 3. This translates into around 1 ns in terms of delay spread using a straight line with a 2 dB slope (over a 10 GHz span) and a linear phase response. Also, we divide the frequency span into 8 equal bandwidth channels and calculate how much bandwidth can be achieved in each channel according to our definition of bandwidth. This frequency division multiplexing (FDM) scheme presupposes perfect filtering, which is not possible in real applications but will be addressed later. The results hence denote upper bounds on the achievable channel bandwidths. The main purpose here is to investigate the effects of frequency and bandwidth scaling with the supposition of "perfect" filtering. Shown in Figure D.2 are the insertion loss curves of the side-to-side (i=2) and diagonal (i=3) channels of the monopole model simulated at a center frequency of 38 GHz. In this case, the frequency span, 10 GHz, is divided into eight channels where the maximum (ideal-case) bandwidth of each channel is 1.25 GHz.

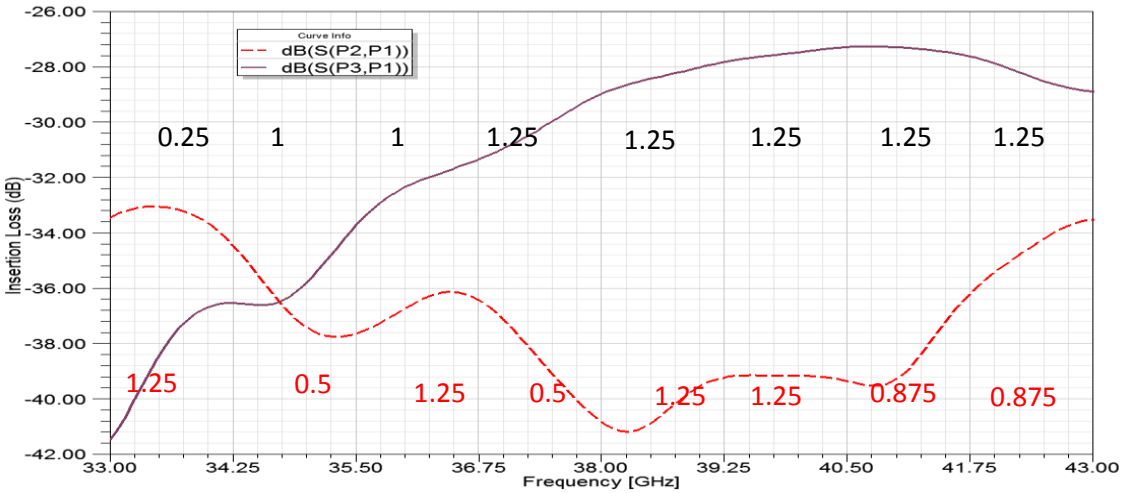

Figure D.2. Insertion Loss at f_0=38 GHz in dB ($S(Pi,Pj)$ is $20log_{10}(S_{ij})$, i=2, 3, j=1.

[6] *The 2 dB threshold is an initial "working" value that may be refined later.

We show in Figure D.3 the calculated bandwidths of each of the 8 channels that span the frequency range of 10 GHz for this case. The S2S, BW, MaxSCBW abbreviations denote “side-to-side”, “bandwidth”, and “maximum single channel bandwidth” respectively. We adopt these abbreviations throughout. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 9.75 GHz, again with perfect filtering. This bandwidth is achieved by using a specific transmission/ reception scheme represented by the dashed arrows in Figure D.1. There are several permutations for assigning such schemes and they are subject to connectivity, architecture and technology limitations. Such technology limitations manifest themselves especially at the higher center frequency designs where the channel bandwidth reaches tens of gigahertz, posing significant challenges for modulator and demodulator devices and hardware to attain such rates. The maximum single channel bandwidth is achieved from the diagonal link and occurs between 38 GHz and 43 GHz.

Table D.1. Model dimensions at different center frequencies

Center frequency (f_0) in GHz	**d_S in mm**	**d_D in mm**	**d_E in mm**
38	64	64.√2	8
75	32	32. √2	4
150	16	16. √2	2
300	8	8.√2	1
600	4	4.√2	0.5

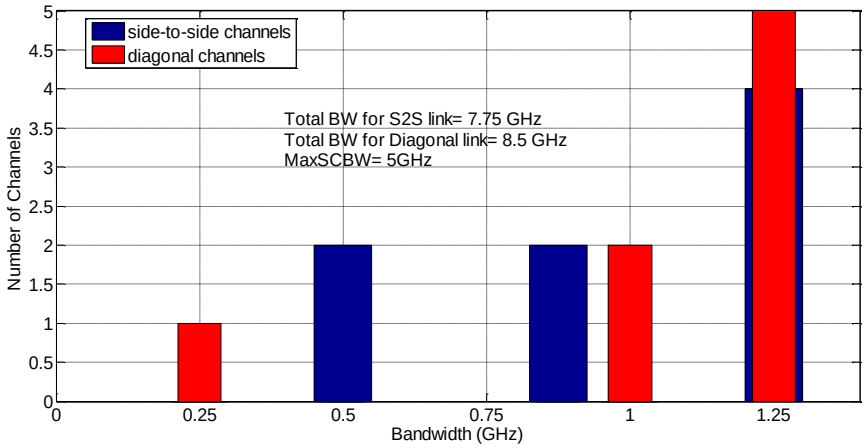

Figure D.3. Channel bandwidth for the design at f_0=38 GHz

Monopole Model Design at f_0= 75 GHz

Next, we show the results for the monopole model simulated at a center frequency of 75 GHz. The chip size is 40 mm x 40 mm and we show in Table D.1 the dimensions for all models simulated at all center frequencies. The insertion losses for the side-to-side and diagonal links are shown in Figure D.4. Note the similarity to the results in Figure D.2. For this case, the 20 GHz frequency span is divided into eight channels where the maximum bandwidth per channel is 2.5 GHz. In Figure D.5, we present the calculated bandwidths of each of the 8 channels that span the frequency range of 20 GHz. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 18.5 GHz, again with perfect filtering. This is almost twice as the total bandwidth from the previous model simulated at 38 GHz with a frequency span of 10 GHz. The maximum single channel bandwidth of 10 GHz is achieved from the diagonal link and is between 75 GHz and 85 GHz. We show in Table D.2 the channels that achieve the

maximum bandwidth with their corresponding bit rates and frequency spans. C_{xy} denotes the channel between antennas x and y.

Table D.2. Maximum Bandwidth Channel Allocation for Model at f_0= 75 GHz.

Channel	Bandwidth (GHz)	Frequency range (GHz)
C_{24}	10	75-85
C_{34}	5	70-75
C_{13}	1	67.5-70
C_{41}	2.5	65-67.5

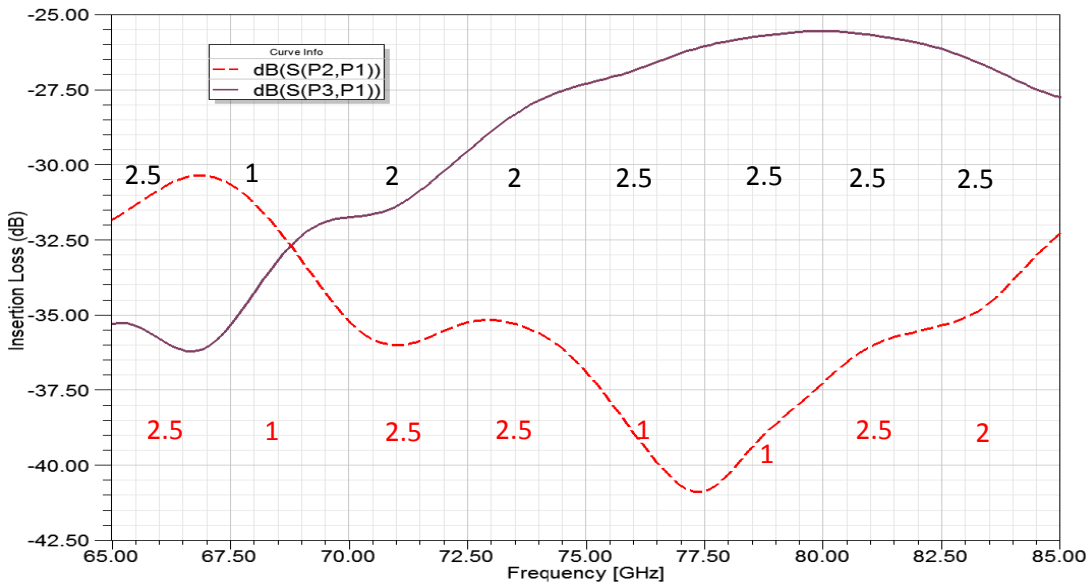

Figure D.4. Insertion Loss at f_0=75 GHz in dB (*S(Pi,Pj)* is $20log_{10}(S_{ij})$, i=2, 3, j=1.

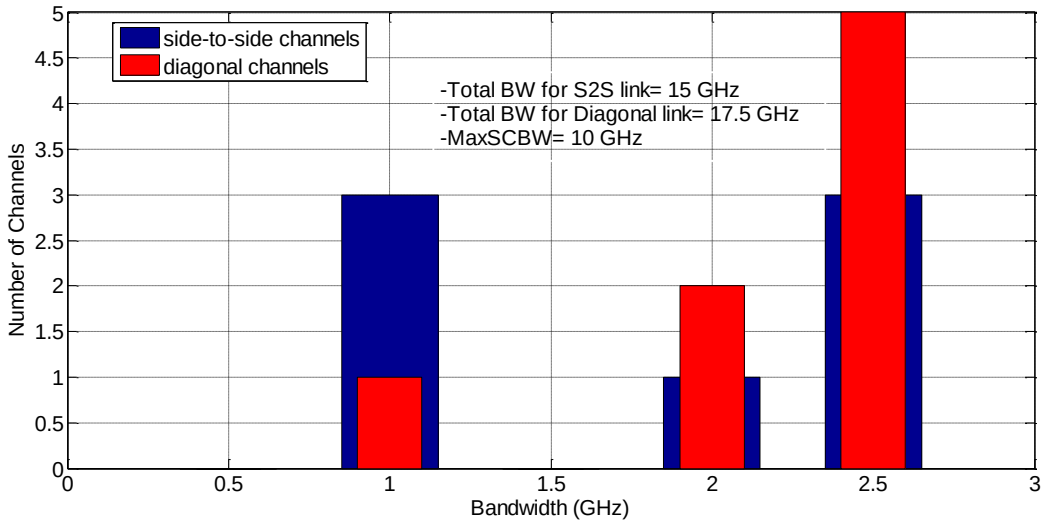

Figure D.5. Channel bandwidth for the design at f_0=75 GHz

Monopole Model Design at f_0=150 GHz

Note that we have already provided the monopole design and multiple access results in Chapter 4. The results are repeated here for completeness in this appendix on frequency scaling. We show in Figure D.6 the insertion loss for the monopole design at a center frequency of 150 GHz. For this case, the 40 GHz frequency span is divided into eight channels where the maximum bandwidth per channel is 5 GHz. In Figure D.7, we present the calculated bandwidths of each of the 8 channels that span the frequency range of 40 GHz. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 38 GHz, again with perfect filtering. This is almost twice as the total bandwidth from the previous model simulated at 75 GHz with a frequency span of 20 GHz. The maximum single channel bandwidth of 20 GHz is achieved from the diagonal link and is between 150 GHz and 170 GHz. We show in Table D.3 the channels that achieve the maximum bandwidth with their corresponding bit rates and frequency spans.

Table D.3. Maximum Bandwidth Channel Allocation for Model at f_0= 150 GHz

Channel	Bandwidth (GHz)	Frequency range (GHz)
C_{24}	20	150-170
C_{13}	4	145-150
C_{34}	5	140-145
C_{42}	4	135-140
C_{21}	5	130-135

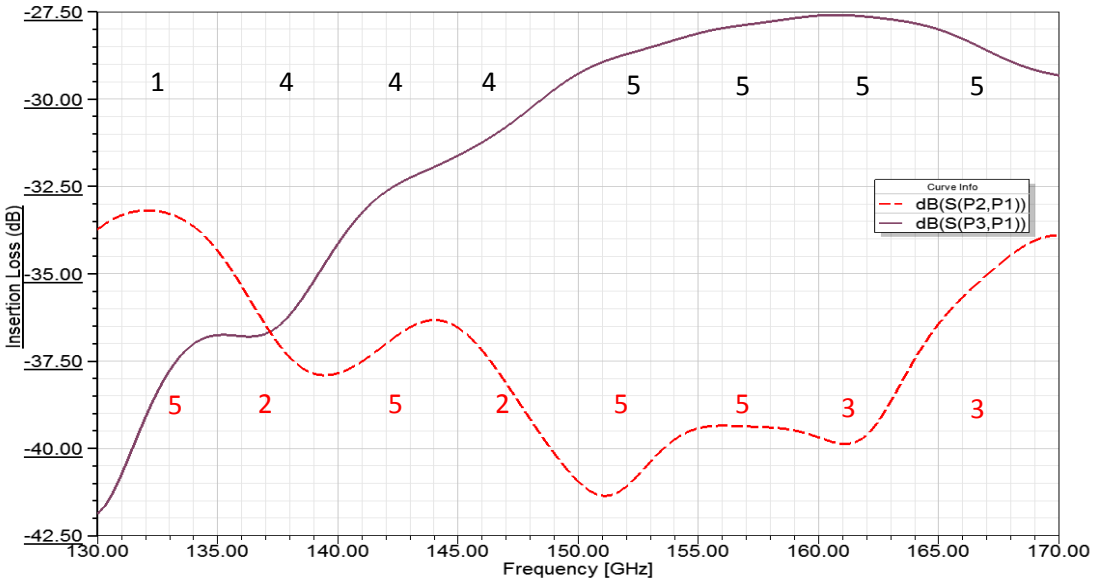

Figure D.6. Insertion Loss for the monopole design in dB (*S(Pi,Pj)* is $20log_{10}(S_{ij})$, i=2, 3, j=1.

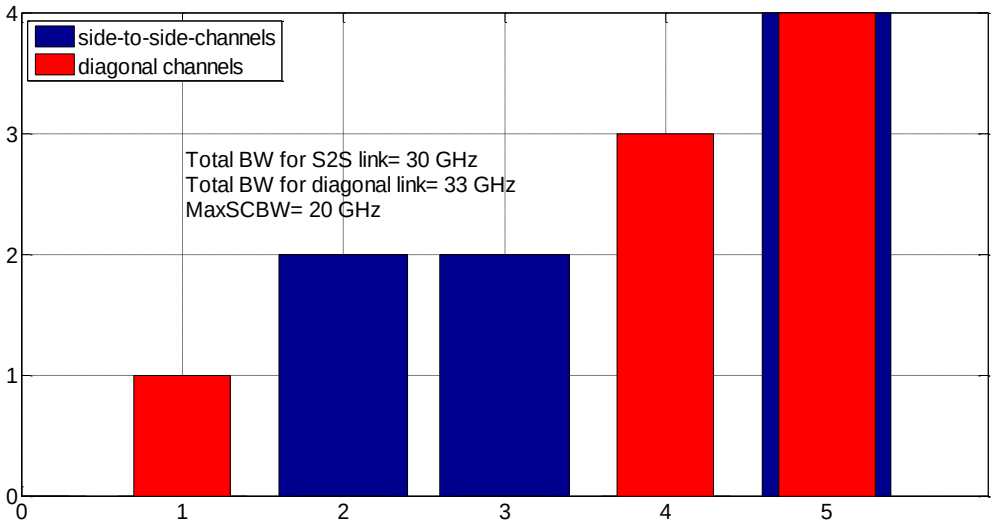

Figure D.7. Channel bandwidth for the design at f_0=150 GHz

Monopole Model Design at f_0= 300 GHz

The next design shows results for the monopole model simulated at a center frequency of 300 GHz. The chip size is now 10 mm ×10 mm and the model dimensions are shown in Table D.1. The insertion loss for the side-to-side and diagonal links is shown in Figure D.8. For this case, the 80 GHz frequency span—double the span that we use for our models simulated at 150 GHz—is divided into eight channels where the maximum bandwidth per channel is 10 GHz. In Figure D.9, we present the calculated bandwidths of each of the 8 channels that span the frequency range of 80 GHz. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 74 GHz, again with perfect filtering. This is (again) approximtely double the total bandwidth from the previous model simulated at 150 GHz with a frequency span of 40 GHz. The maximum single channel bandwidth of 40 GHz is achieved again from the diagonal link and is between 300 GHz and 340 GHz. We show in Table D.4 the channels

that achieve the maximum bandwidth with their corresponding bit rates and frequency spans.

Table D.4. Maximum Bandwidth Channel Allocation for Model at f_0= 300 GHz

Channel	Bandwidth (GHz)	Frequency range (GHz)
C_{24}	40	300-340
C_{13}	6	290-300
C_{34}	10	280-290
C_{42}	8	270-280
C_{21}	10	260-270

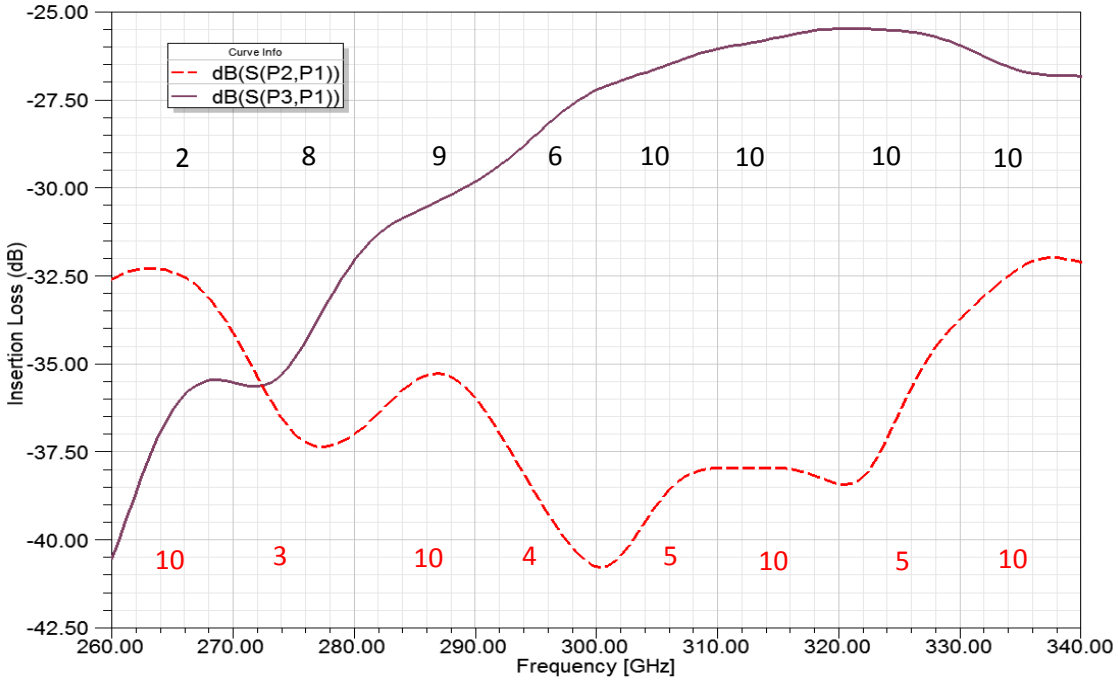

Figure D.8. Insertion Loss at f_0=300 GHz in dB (*S(Pi,Pj)* is $20log_{10}(S_{ij})$, i=2, 3, j=1.

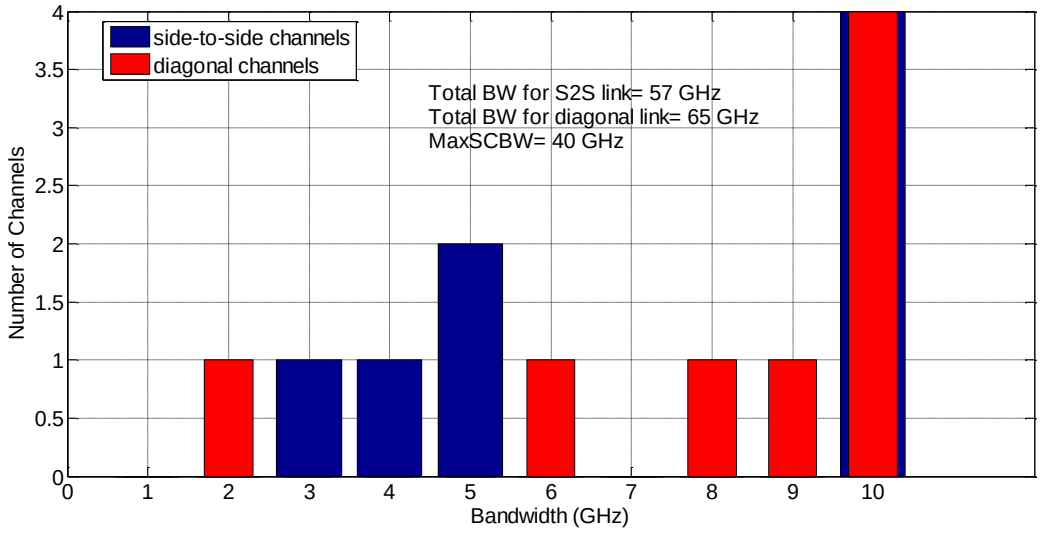

Figure D.9 Channel bandwidth for the design at f_0=300 GHz

Monopole Model Design at f_0= 600 GHz

For our last example, we present the results for the monopole model simulated at center frequency of 600 GHz. The insertion loss for the side-to-side and diagonal links is shown in Figure D.10. For this case, the 160 GHz frequency span—quadruple the span that we use for our models simulated at 150 GHz— is divided into eight channels where the maximum bandwidth per channel is 20 GHz. In Figure D.11, we present the calculated bandwidths of each of the 8 channels that span the frequency range of 160 GHz. The total bandwidth that can be used from the side-to-side and diagonal channels simultaneously is 142 GHz, again with perfect filtering. This is once again almost double the total bandwidth from the previous model simulated at 300 GHz with a frequency span of 80 GHz. The maximum single channel bandwidth of 80 GHz is achieved again from the diagonal link and is between 600 GHz and 680 GHz. We show in Table D.5 the

channels that achieve the maximum bandwidth with their corresponding bit rates and frequency spans.

Table D.5. Maximum Bandwidth Channel Allocation for Model at f_0= 600 GHz

Channel	Bandwidth (GHz)	Frequency range (GHz)
C_{24}	80	600-680
C_{13}	12	580-600
C_{34}	20	560-580
C_{42}	12	540-560
C_{21}	18	520-540

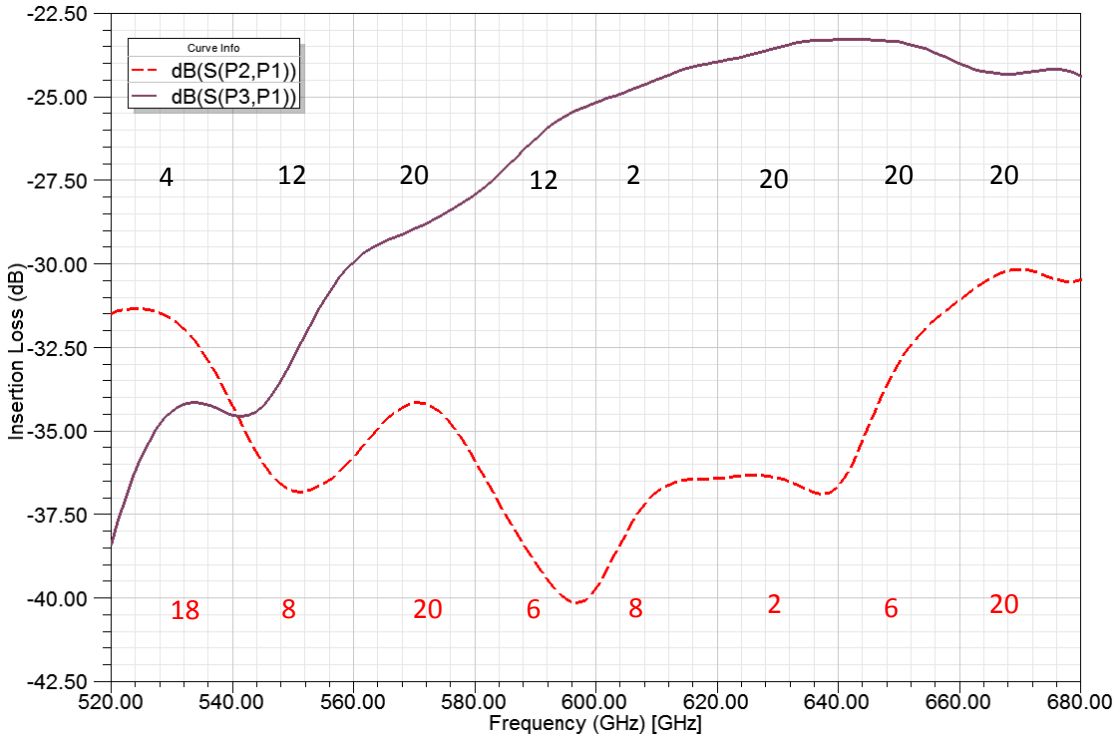

Figure D.10. Insertion Loss at f_0=600 GHz in dB (*S(Pi,Pj)* is $20log_{10}(S_{ij})$, i=2, 3, j=1.

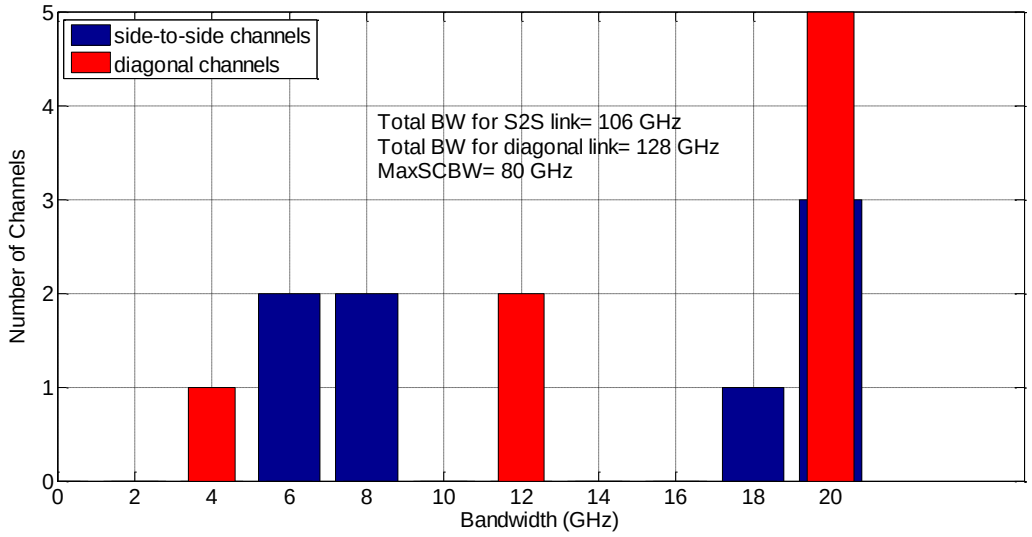

Figure D.11. Channel bandwidth for the design at f_0=600 GHz

In conclusion, the bandwidth achieved from this model does indeed scale with center frequency and frequency span. Obviously designing the model around a center frequency of a few terahertz would provide the bandwidth, 512 GHz, sought after by the computer architecture team of the WiNoC project. However, the actual design of the hardware and components remains very challenging. It should also be noted that choosing a lower insertion loss variation to define bandwidth (we used 2 dB) would naturally decrease the amount of bandwidth that we can achieve from any model shown above. Even though the delay spread corresponding to the insertion loss variation of 2 dB results from a straight line approximation to the actual insertion loss curve, delay spreads in nanoseconds would be severely performance limiting and almost certainly would require us to utilize equalization at the receiver side Also, the aspect of perfect filtering is unrealistic and we would envision allocating guard bands between channels to prevent interference in our FDM scheme. This would decrease both the spectral efficiency and

the amount of usable. It is also worth noting that in all the simulations that were done, the return loss of all the channels was less than or equal to -13 dB.