Linköping Studies in Science and Technology
Dissertations, No. 1093

Implementation of Flash Analog-to-Digital Converters in Silicon-on-Insulator CMOS Technology

Erik Säll

Linköping University
INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering
Linköping University, SE–581 83 Linköping, Sweden

Linköping 2007

Implementation of Flash Analog-to-Digital Converters in Silicon-on-Insulator CMOS Technology

eriks@isy.liu.se
http://www.es.isy.liu.se
Division of Electronics Systems
Department of Electrical Engineering
Linköpings universitet
SE–581 83 Linköping
Sweden

ISBN 978-91-85715-18-3 ISSN 0345-7524

Printed by LiU-Tryck, Linköping 2007

Abstract

A 130 nm partially depleted silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) technology is evaluated with respect to analog circuit implementation. We perform the evaluation through implementation of three flash analog-to-digital converters (ADCs). Our study indicate that to fully utilize the potential performance advantages of the SOI CMOS technology the partially depleted SOI CMOS technology should be replaced by a fully depleted technology. The manufacturing difficulties regarding the control of the thin-film thickness must however first be solved. A strong motivator for using the SOI CMOS technology instead of bulk CMOS seems to be the smaller gate leakage power consumption.

The targeted applications in mind for the ADCs are read channel and ultra wideband radio applications. These applications requires a resolution of at least four to six bits and a sampling frequency of above 1 GHz. Hence the flash ADC topology is chosen for the implementations. In this work we do also propose enhancements to the flash ADC converter. Further, this work also investigates introduction of dynamic element matching (DEM) into a flash ADC. A method to introduce DEM into the reference net of a flash ADC is proposed and evaluated.

To optimize the performance of the whole system and derive the specifications for the sub-blocks of the system it is often desired to use a top-down design methodology. To facilitate the top-down design methodology the ADCs are modeled on behavioral level using MATLAB and SpectreHDL. The modeling results are used to verify the functionality of the proposed circuit topologies and serve as a base to the circuit design phase.

The first flash ADC implementation has a conventional topology. It has a resistor net connected to a number of latched comparators and employs a ones-counter thermometer-to-binary decoder. This ADC serves as a reference for evaluating the other topologies. The measurements indicate a maximum sampling frequency of 470 MHz, an SNDR of 26.3 dB, and an SFDR of about 29 to 35 dB.

The second ADC has a similar topology as the reference ADC, but its thermometer-to-binary decoder is based on 2-to-1 multiplexers buffered with inverters. This gives a compact decoder with a regular structure and a short critical path. The measurements show that it is more efficient in terms of power consumption than the ones-counter decoder and it has 40 % smaller chip area. Further, the SNDR and SFDR are similar as for the reference ADC, but its maximum sampling frequency is about 660 MHz.

The third ADC demonstrates the introduction of DEM into the reference net of a flash ADC. Our proposed technique requires fewer switches

in the reference net than other proposals. Our technique should thereby be able to operate at higher sampling and input frequencies than compared with the other proposals. This design yields information about the performance improvements the DEM gives, and what the trade-offs are when introducing DEM. Behavioral level simulations indicate that the SFDR is improved by 11 dB in average when introducing DEM. The transistor level simulations in Cadence and measurements of the ADC with DEM indicates that the SFDR improves by 6 dB and 1.5 dB, respectively, when applying DEM. The smaller improvement indicated by the measurements is believed to be due to a design flaw discovered during the measurements. A mask layer for the resistors of the reference net is missing, which affects their accuracy and degrades the ADC performance. The same reference net is used in the other ADCs, and therefore degrades their performance as well. Hence the measured performance is significantly lower than indicated by the transistor level simulations. Further, it is observed that the improved SFDR is traded for an increased chip area and a reduction of the maximum sampling frequency. The DEM circuitry impose a 30 % larger chip area.

Acknowledgments

First I thank my supervisor Professor Mark Vesterbacka for giving me the opportunity to do this work and for his guidance and support during the work. I also thank him for the valuable help in proofreading this thesis.

I also thank my past and present colleagues at the Division of Electronics Systems for their support, friendship, and for providing an inspiring environment. For the same reasons I thank the rest of my colleagues I have had cooperation with at the Department of Electrical Engineering.

I also thank Per-Erik Fägerman at Mandalon Technologies AB, who bonded the chips, for the the chip photos of the ADCs.

I thank all my friends for helping me to recharge my batteries when I am not at work. I will hopefully see some of you in a strong thermal to the sound of a happy variometer, climbing for the final glide after a day in the sky.

A special thank to my parents Lennart and Birgitta, and my sisters Ann-Sofie and Josefine for their support through the years. Even though you might think you know what I have been doing for the past 4.5 years, maybe this thesis can give you some more insight.

This work was supported by the MEDEA+ program, which financed the chip manufacturing, and financially supported by STRINGENT and the Swedish Research Council.

Erik Säll

Linköping, March 22, 2007

Abbreviations and Notation

This section lists the abbreviations and notation used in this thesis.

Abbreviations

ADC	Analog-to-digital converter
BiCMOS	Bipolar complementary metal oxide semiconductor
BOX	Buried oxide
BSIM3SOI	Berkeley short-channel IGFET model for SOI
CD	Compact disc
CLK	Clock
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
DC	Direct current
DEM	Dynamic element matching
DUT	Device under test
DVD	Digital versatile disc
ENOB	Effective number of bits
ERBW	Effective resolution bandwidth
ESD	Electrostatic discharge
FA	Full adder
FD	Fully depleted
FoM	Figure of merit
GaAs	Gallium arsenide
GSM	Global system for mobile communications
HDD	Hard disk drive
IGFET	Insulated-gate field effect transistor
LNA	Low noise amplifier
LPF	Low-pass filter
LSB	Least significant bit
MiM	Metal insulator metal
MOSFET	Metal oxide semiconductor field effect transistor
MSB	Most significant bit
MUX	Multiplexer

NMOS	Negative-channel metal oxide semiconductor
PCB	Printed circuit board
PD	Partially depleted
PLL	Phase locked loop
PMOS	Positive-channel metal oxide semiconductor
PRBS	Pseudo-random bit stream
Q	Quality factor
RF	Radio frequency
ROM	Read-only memory
SFDR	Spurious-free dynamic range
SH	Sample-and-hold
Si	Silicon
SiO_2	Silicon dioxide
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
SOI	Silicon-on-insulator
SOS	Silicon-on-sapphire
SQNR	Signal-to-quantization noise ratio
SSN	Simultaneous switching noise
TH	Track-and-hold
VGA	Variable gain amplifier

Notation

A_0	DC gain
$C_{ch,b}$	Parasitic capacitance between channel and body
$C_{comp,in}$	Parasitic capacitance between the comparator inputs
C_{db}	Parasitic bottom junction area capacitance at the drain
$C_{g,ch}$	Parasitic capacitance between gate and channel
C_{gs}	Parasitic capacitance between gate and source
$C_{j,d}$	Parasitic drain junction capacitance
$C_{j,s}$	Parasitic source junction capacitance
$C_{j,sw}$	Parasitic sidewall junction capacitance

C_{L}	Load capacitance
C_{ox}	Gate oxide capacitance per unit area
C_{sb}	Parasitic bottom junction area capacitance at the source
C_{tot}	Total $C_{\mathrm{comp,in}}$ on the ADC input
D_3	Third order distortion
d_i	Bit i in the digital output
D_{out}	Digital output
dR	Statistical deviation of the resistance
dV_{ref}	Statistical deviation of the reference net supply voltage
f_{amp}	Preamplifier -3 dB bandwidth
f_{in}	Input frequency
$f_{\mathrm{in,max}}$	Maximum input frequency
f_{s}	Sampling frequency
$f_{\mathrm{s,max}}$	Maximum sampling frequency
f_{T}	Unity gain frequency
g_{ds}	Small signal drain-source conductance
g_{m}	Transistor transconductance
I_{ch}	Channel current
I_{d}	Total drain current
I_{D}	DC drain current
$I_{\mathrm{D,sat}}$	Drain saturation current
I_{ref}	Reference bias current
k	Boltzmann's constant
L	Channel length
M	Total number of output samples
M_{n}	Rate of metastable states
n	Body factor
N	Total number of output bits, i.e., ADC resolution
$\mathrm{N}(0,\sigma)$	Gaussian distribution with zero mean and σ standard deviation
p_{dec}	Reference net decoupling period, used in (5.6)
$P_{\mathrm{distortion}}$	Distortion power

P_{noise}	Noise power
P_{signal}	Signal power
$P_{\text{spurious,max}}$	Power of the largest spurious
q	The charge of an electron, i.e., the elementary charge
q_{e}	Quantization error
q_{LSB}	Feedthrough from input to reference net measured in number of LSBs
q_{s}	Quantization step
R_{tot}	Total reference net resistance
R_{u}	Unit resistance of a resistor in the reference net
Δt	Timing difference between the clock and input signals wires
T	Temperature in Kelvin
t_{MUX}	Propagation delay of a 2:1 MUX
t_n	Sample time instants
t_{ox}	Oxide thickness
Δt_{s}	Sampling time uncertainty
$t_{\text{CP,folded}}$	Critical path of the folded Wallace tree decoder
$t_{\text{CP,MUX-decoder}}$	Critical path of the MUX-based decoder
$t_{\text{CP,Wallace}}$	Critical path of the Wallace tree decoder
t_{XOR}	Propagation delay of an XOR gate
V_{A}	Early voltage
V_{bias}	Bias voltage
V_{DD}	Supply voltage
V_{ds}	Voltage between drain and source
V_{ESD}	ESD stress voltage
V_{FS}	Full-scale voltage
V_{gs}	Voltage between gate and source
V_{in}	Input voltage
ΔV_{in}	Uncertainty in the sampled input voltage
V_{lr}	Linear range of the preamplifier
V_{LSB}	Voltage equivalent to one LSB

V_{mid}	Magnitude of the middle reference net output voltage with respect to the input voltage magnitude
V_{offset}	Comparator input offset voltage
V_{ref}	Reference net supply voltage
$V_{\text{ref},m}$	Reference generator output voltage m
V_{s}	Sampled input voltage
ΔV_{s}	Uncertainty in the sampled input voltage
V_{SS}	Negative supply voltage
V_{T}	Threshold voltage
W	Transistor width
y_n	Output sample n
$\tilde{y}_n$	Sinusoid to fit to the output samples at sample n
Γ_{folded}	Hardware cost of the folded Wallace tree decoder
Γ_{MUX}	Hardware cost of a 2:1 MUX
$\Gamma_{\text{MUX-decoder}}$	Hardware cost of the MUX-based decoder
Γ_{Wallace}	Hardware cost of the Wallace tree decoder
μ	Surface channel charge carrier mobility
ω	Angular frequency
Ψ	Squared error between fitted output samples and sinusoid
σ_{offset}	Standard deviation of the input referred comparator offset voltage
σ_{R}	Standard deviation of the reference net unit resistor deviation
σ_{ref}	Standard deviation of the reference net supply voltage deviation
σ_{t}	Standard deviation of the time difference between the clock and the input signal
$\langle . \rangle$	Mean value

Contents

Chapter 1

Introduction

As the technologies are scaled down into the sub 100 nm the static leakage power start to become more important. To reduce the static leakage power and improve the device performance in terms of, e.g., device speed, latch-up, and cross talk, interest in other technologies than the mainstream technologies have increased in the latest years. One of these emerging technologies is the silicon-on-insulator (SOI) technology. Even though the SOI technology has been around since 1964 [62], it has so far mostly been used for digital [2, 38, 84, 86] or pure RF [77, 78, 100, 103] applications. Many of these designs are often targeted for special applications, e.g., military, space, high-temperature [30], low-voltage sensor circuits [102], or highly radiant environments [21, 27, 56]. Hence, it has been used mainly for low volume production. The manufacturing cost was therefore high. In the latest years, more circuits designed in SOI technologies have been used in high volume production. Most of those are digital circuits. Only a few are analog RF circuits [22]. The increased volume of production reduces the manufacturing cost and the technology has now become competitive with more mainstream technologies in terms of the manufacturing cost.

This work is a part of the industry-initiated pan-European program for advanced cooperative research and development in microelectronics, called

MEDEA+. One of the around 30 projects in the MEDEA+ program is the T206 project, and this work is a part of that project. The purpose of the T206 project it to find out if the SOI technology is suitable for implementation of a range of mobile and networking devices. The targeted applications of this work are ultra wideband (UWB) radio applications, presented in Section 1.2.1, and in read channel applications, presented in Section 1.2.2. The ADC used in these applications requires a resolution of four to six bits, and a sampling frequency of above 1 GHz. These requirements can be fulfilled if using the flash ADC topology. Hence, in this work we focus on the design and implementation of flash ADCs in the 130 nm partially depleted (PD) SOI complementary metal oxide semiconductor (CMOS) technology provided by MEDEA+.

Another reason for choosing to design analog circuits in SOI CMOS technology is to investigate how the analog circuits are affected by the unwanted effects appearing when using the technology, presented in Chapter 2. It is also desired to develop design guidelines that consider these effects. Examples on the unwanted effects appearing when implementing circuits in this technology are the kink, history, and self-heating effects. Digital circuits are also affected by these effects, but they are more problematic for analog circuits.

As mentioned, when the integrated circuit technologies are continuously scaled down the performance of the digital circuits are increasing. At the same time more functionality can be built into the digital circuits since the circuit area is scaled with the devices. Unfortunately the technology scaling does not have the same impact on the analog circuits. Hence, people today want to do as much of the signal processing as possible in the digital domain instead of the analog domain. However, before the signals can be processed in the digital domain the analog signals must first be converted to digital signals, which is done by the analog-to-digital converter (ADC). One application for ADCs is illustrated by Figure 1.1, showing the conversion of sound to a digital signal that can be stored on, e.g., a hard disk drive (HDD) or a compact disc (CD). The microphone converts the sound into an electrical signal, which is amplified (AMP), filtered by an anti-aliasing filter (LPF) and then converted to the digital domain by the ADC. The ADC output is processed by some digital signal processing (DSP) algorithm, and the result is stored onto the storage device.

There are numerous different ADC topologies. Which one to chose depends to a large extent on the requirements on the ADC set by the targeted application, e.g., conversion speed and resolution. For an audio application

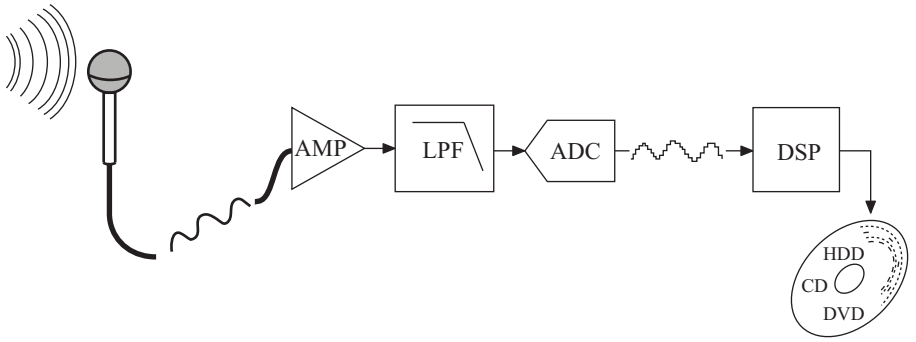


Figure 1.1: Illustration of an audio application.

the frequency range of the audio signal is not very wide, only up to about 20 kHz. The requirement on the conversion speed of the ADC is therefore low. However, when you play your CD you probably want a good sound quality, i.e., the digitized sound should contain precise information about the original sound. The amplitude of the analog signal should thereby be represented by many levels by the ADC, i.e., it should have many quantization levels. Hence, the requirement on the resolution of the ADC, i.e., number of output bits, is high when the ADC is used for audio applications. The sigma-delta ADC topology is therefore commonly used for this case. For other applications having other requirements on the ADC, another ADC topology is chosen. What ADC topology that are suited for different requirements on sampling frequency and resolution is found in Figure 1.2. In this work the applications are assumed to have high requirements on the conversion speed, i.e., data rate, but the requirements on the resolution is low. Based on these requirements Figure 1.2 shows that the flash ADC topology is an appropriate choice, which is why this topology is commonly used for high-speed ADCs, and also why it is chosen for this work.

The flash ADC topology is illustrated in Figure 1.3. Such ADCs are used for a number of applications, e.g., UWB radio applications and in read channel applications. They are also often used as a component in, e.g., pipelined ADCs [55, 65, 121], or multi-bit sigma-delta ADCs [39, 71, 122]. As seen in Figure 1.3 the input signal V_{in} of a flash ADC is applied to the positive comparator inputs. Their negative inputs are connected to a resistor net that generates the reference voltages. The output pattern of the comparator corresponds to thermometer code, which is decoded to, e.g., binary code by the $(2^N - 1)$-to-N decoder in Figure 1.3, where N is the resolution of the ADC in number of bits. Since the number of comparators,

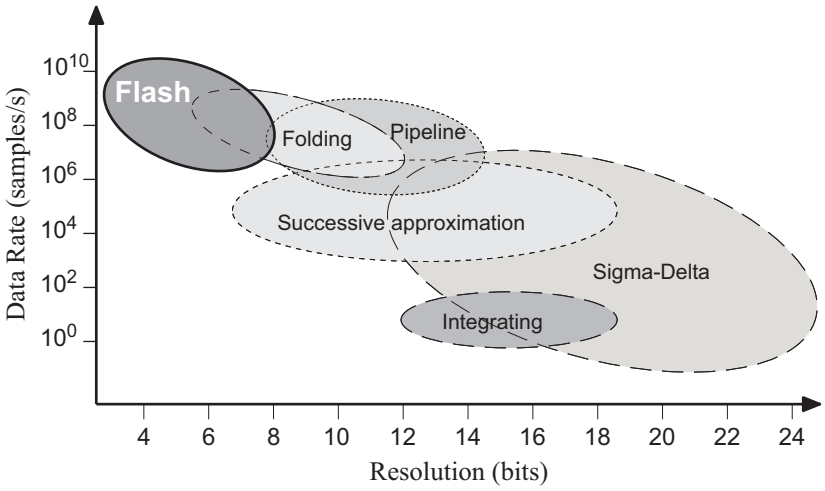


Figure 1.2: Overview of ADC topologies and their performance.

and thereby the chip area, grows as 2^N with the number of bits N, the resolution is generally in practice limited to at most eight bits for flash ADCs, as also is seen from Figure 1.2. For larger resolutions, the large number of required comparators would limit the input bandwidth of the converter, consume a large chip area, and have a high power consumption [108]. However, for low resolutions the flash ADC topology can be used to yield fast ADCs [104, 108].

The major part of this work concerns the evaluation of a partially depleted SOI technology and the design of three different ADC topologies. One serves as a reference ADC used for comparing the other two topologies, and for comparing the design and implementation strategies. A second flash ADC employs a new decoder based on multiplexers (MUXs). The third ADC demonstrates an improved way of introducing dynamic element matching (DEM) into the reference net of the flash ADC, thereby enhancing its output spectral properties.

An efficient design methodology used in this work is the top-down methodology. Using this methodology the system is first modeled on a behavioral level, allowing fast simulation of the whole system. Although the simulation is not as accurate as a transistor level simulation, the results yield information that is valuable in the design of the subsequent steps in the design flow, e.g., insight in different trade-offs. The first model is gradually refined and finally the circuit topology of each sub-circuit in the system can be decided, e.g., what type of comparators to use in the flash ADC, what

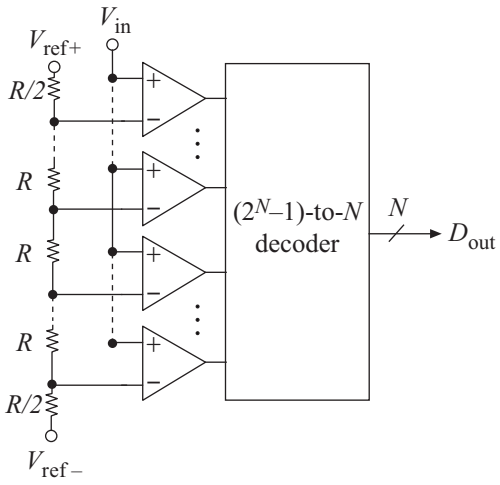


Figure 1.3: Illustration of a flash ADC.

type of preamplifiers, and what decoder topology to use. A number of behavioral level models of the ADCs are presented in this work, whose results are used in the circuit design phase. During the behavioral level modeling of the ADCs the effect of the thermometer-to-binary decoder topology on the ADC performance is studied. Two new decoder topologies are studied, a modified Wallace tree decoder [52] and a MUX-based decoder [92]. The latter is used as the decoder in one of the implemented ADCs presented in this work.

Another proposal is a flash ADC where DEM is introduced. The ADC with DEM is also first modeled on the behavioral level. The behavioral level simulation and the later transistor level simulation showed promising results. The flash ADC with DEM is therefore manufactured. Although the measurements show that the performance is far from the simulated, the results support some of the benefits indicated by the simulations. Suggestions for improvements of the design are also given.

1.1 Design Flow

The design flow used in the design of the circuits in this work is illustrated by Figure 1.4 and Figure 1.5. Figure 1.4 illustrates the design flow from the behavioral level modeling stage to the circuit assembly layout. The design flow in Figure 1.5 illustrates the design flow from the circuit assembly layout

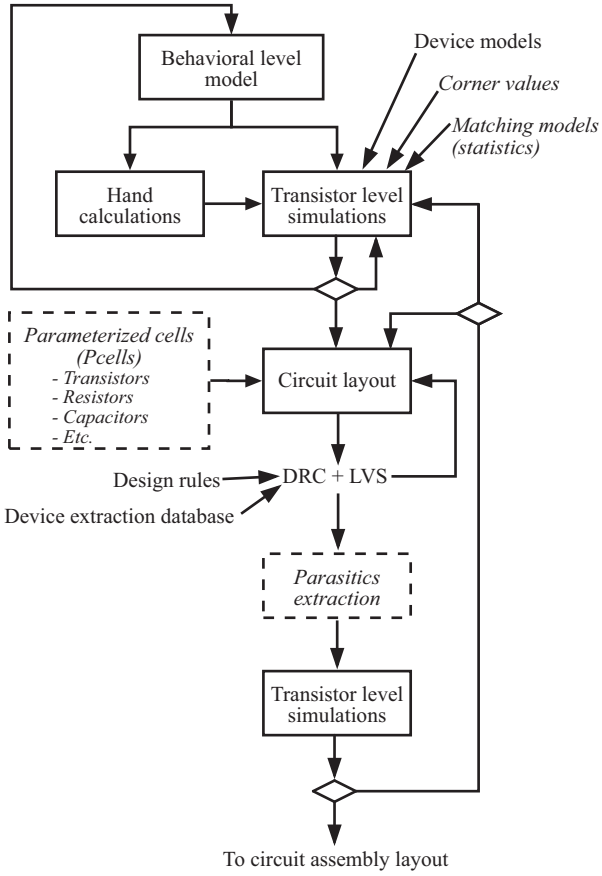


Figure 1.4: The design flow from the behavioral level model to circuit assembly layout used for the designs in this work.

to the stage when the design is sent for manufacturing. The dashed blocks and parts indicated in italic font in Figure 1.4 and Figure 1.5 are parts that should be included in a complete design kit, but are unfortunately not available in the provided design kit for the technology used in this work.

The first step is the behavioral level modeling. In this phase the topology of the system and subcircuits is chosen. As the models are refined the requirements on the subcircuits are extracted, such as gain and bandwidth of the preamplifiers for the comparators. The next step is to design each subcircuit, which is done using iterative transistor level simulations, where the initial values are derived from hand calculations. From the hand calculations the designer also get insight into what parameter that needs to be

adjusted to, e.g., increase the gain or bandwidth of the circuit. The simulations are performed using Cadence and the Eldo simulator. To simulate the circuit the simulator requires information about the device models, which in this case are BSIM3SOI Eldo models provided by the foundry. Further, when all devices are sized so that the circuit fulfills the requirements the manufacturing yield should be enhanced.

When the circuits are manufactured various deviations caused by imperfections in the manufacturing process result in a circuit behavior other than the simulated. Hence not all manufactured circuits will fulfill the requirements. The yield is therefore less than 100 %. To enhance the yield the design kits commonly contain mismatch models and corner values for the devices. These are however not available in the provided design kit. The circuits in this work are therefore only simulated using the typical device models.

If the circuit does not fulfill the requirements after the steps above, another topology might be required and the behavioral level modeling step has to be iterated again. When the circuit fulfill the requirements, and has acceptable performance after the yield enhancement, the circuit is transformed into a layout, i.e., the blueprint used for manufacturing the circuit. In this phase the parameterized cells (Pcells) of the transistors, resistors, capacitors, etc., are placed and connected according to the schematic by considering the design rules, and also considering, e.g., layout rules for having good matching between critical devices. The Pcells are generally provided in the design kit, but not in this case. This work therefore contains an extra loop where the Pcells are created and verified by the design rule check (DRC). The loop is however excluded in Figure 1.4.

After layout, the layout is run through the DRC to verify that it complies with the design rules provided by the vendor. In addition the layout is compared with the schematic to ensure that the layout realizes the same function as the circuit defined by the schematic, i.e., the layout versus schematic (LVS) check.

When the layout passes the DRC and LVS checks the parasitics are extracted and inserted into the schematic to verify that the circuit still fulfills the requirements. Neither of these steps could be performed in this work, since the rules for the parasitics extraction are not available in the design kit. Instead some rough estimates of the parasitic capacitance in sensitive nodes are made from the layout and inserted into the schematic for verification.

When all subcircuits have passed the DRC and LVS checks and the

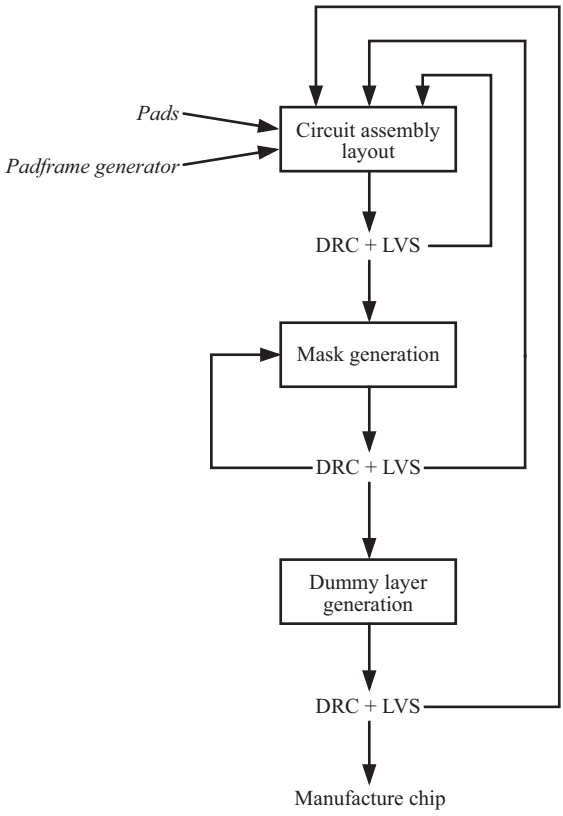


Figure 1.5: The design flow from circuit assembly layout to chip manufacturing used for the designs in this work.

circuit including the extracted parasitics fulfill the requirements it is time to connect the circuits together, i.e., the circuit assembly layout stage in Figure 1.5. To connect the external circuits to the circuitry on the chip the pads also have to be added. In this work they are placed as a frame around the circuits, but other strategies do also exist. To assist in this step the pads are generally provided as standard cells in the design kit and are often placed by a pad frame generator. Since the used design kit were under development during this work neither the pads nor the pad frame generator are included. As a part of this work the circuitry associated with the pads, i.e., electro-static discharge (ESD) protection circuits and buffers, had to be designed, and a pad frame generator is developed to assist in the layout.

When the circuitry including the pad frame has been verified by the DRC and LVS checks the masks are generated by the provided scripts. The

script generates various elements required for manufacturing of the chip, e.g., patterns for alignment of the masks during the photo lithography. To verify that the scripts did not introduce errors the layout is checked by the DRC and LVS tools once more.

The last step is the generation of dummy layers that are required since each layer must cover the chip with a certain density according to the design rules. Fortunately the dummy generation is performed by running a script provided by the foundry. After a final verification by the DRC and LVS tools the design is ready for manufacturing.

1.2 Applications

In this section the targeted applications for the implemented ADCs are described. The requirements on the ADCs, set by the respective application, is used as input to the behavioral level model, i.e., the first step of the design flow shown in Figure 1.4.

1.2.1 Ultra Wideband Radio

Ultra wideband (UWB) is defined as any signal that occupies a bandwidth of more than 500 MHz in the unlicensed band from 3.1 to 10.6 GHz, and that meets the requirements on UWB signal spectrum mask [1]. The block diagram of a UWB radio receiver is given in Figure 1.6 [68]. In this figure the input signal from the antenna is first amplified by the low noise amplifier (LNA) and then by the variable gain amplifier (VGA). The latter is controlled by the baseband digital signal processor (DSP) via a digital-to-analog converter (DAC). The purpose of the VGA is to ensure that the ADC receives an appropriate input voltage. If the ADC input signal magnitude is too large the ADC is saturated. If the signal magnitude is too low the quantization noise of the ADC would instead be too large relative to the signal, yielding a lower signal-to-noise and distortion ratio (SNDR). The output of the VGA is converted by the ADC, whose output is processed by the baseband DSP. The DSP also controls the clock (CLK) generator, which controls the sampling by the ADC.

The expected applications for UWB radio are short-range wireless communication over a distance of about 10 m. Wireless transceivers employing the UWB technique are scalable and adaptive [1], which is why UWB is expected to be the technique used in the coming IEEE 802.15.3a standard for wireless personal area networks [1, 50]. The main requirements on the transceivers are low complexity, low cost, and low power consumption. The

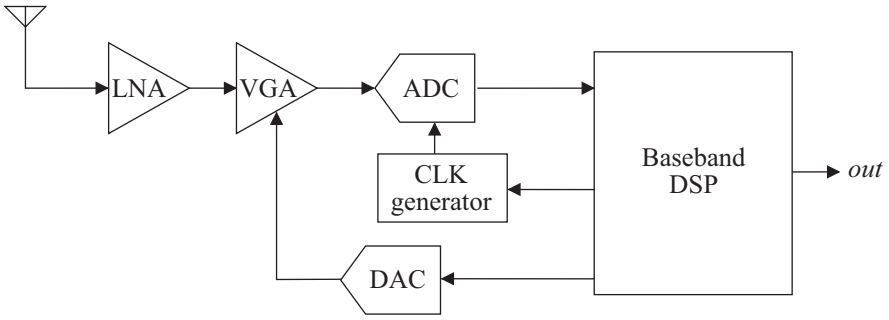


Figure 1.6: Block diagram of a UWB radio receiver.

requirement of low cost generally restricts the technology used to a cheap mainstream bulk CMOS technology. However, use of a bulk CMOS technology yields implementation challenges regarding, e.g., the wideband LNA, the phase locked loop (PLL), and the ADC [1]. Studies have shown that an ADC with a resolution of four bits is sufficient for reliable UWB reception [68]. Hence, a 6-bit flash ADC with an input bandwidth of more than 500 MHz could be used for this application.

1.2.2 Read Channel

The data recovery circuit, i.e., the read channel, of, e.g., a DVD player, a CD player, or a hard disk drive (HDD) converts the stored data into a digital bit stream [67]. A read channel is illustrated by the block diagram in Figure 1.7. Here the input to the read channel is amplified by the VGA. By adjusting its gain, the signal level of the VGA output can be adjusted so that it is within the range set by the ADC, i.e., it has the same purpose as for the UWB transceiver. The next stage of the read channel adjusts the direct current (DC) offset of the signal. Before the signal enters the ADC it is filtered by the anti-aliasing low-pass filter (LPF). The output of the ADC is processed by digital signal processing (DSP) before the output of the read channel is generated. The digital signal processing unit controls the VGA, the offset adjustment unit, and the ADC.

The high data rates in, e.g., hard disks, set high demands on the conversion speed of the read channel. The ADC in the read channel must therefore be able to operate at high sampling rates. The requirement on its resolution is about six bits [17]. These requirements yield that the flash ADC topology is suitable for the converter in the read channel [106].

The above-mentioned CD, DVD, and HDD applications are now appear-

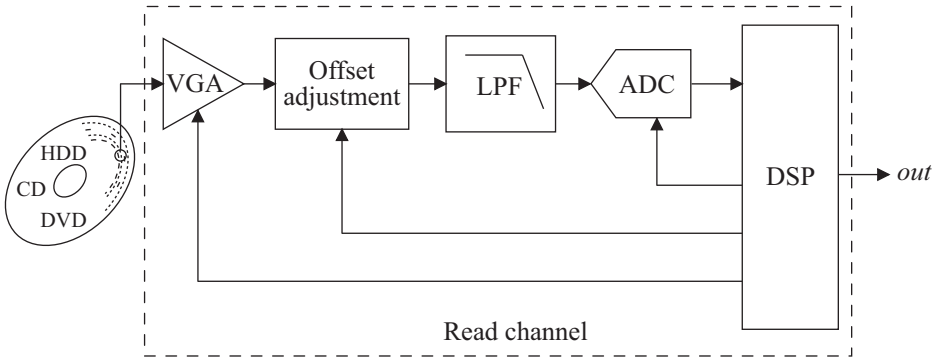


Figure 1.7: Block diagram of a read channel application.

ing in different hand-held applications, where the demand on low power consumption is important. The hand-held applications are therefore an application domain where the SOI technology can be valuable, since it is suited for low-power applications at a low power supply voltage, especially the fully depleted SOI technology [32]. In addition, the power consumption due to increased leakage current of the devices becomes dominant as the device technologies are continuously downscaled. The leakage current of fully depleted SOI CMOS is shown to be two to three times lower than for mainstream bulk CMOS technologies [64]. The lower leakage current is an important factor to why the SOI technology is expected to become increasingly more common in the future [15], and therefore motivates a study on how to implement mixed signal circuits in such a technology.

1.3 Scope of the Work

This work focuses on design and implementation of flash ADCs in a partially depleted SOI CMOS technology provided in the framework of the MEDEA+ program, with the purpose of evaluating the technology. The targeted applications are read channel and UWB radio applications, which are in line with the goals of the T206 project of the MEDEA+ program. The ADC used in read channel and UWB radio applications must have a high sampling rate and a resolution of four to six bits. Hence, the resolution of the ADCs in this work is six bits. The ADCs are designed using the top-down design methodology. To facilitate that methodology the ADCs are modeled on the behavioral level. The modeling is described in this thesis. The converters have also been implemented and evaluated by measurements. This work

also demonstrates the concept of introducing DEM into the reference net of a flash ADC. Further, different thermometer-to-binary decoder topologies are studied and evaluated with respect to the performance of the ADC.

1.4 Contributions

This thesis is a result of my research during the period from November 2002 through February 2007 at the division of Electronics Systems, Department of Electrical Engineering, Linköping University, Sweden.

My main contributions to the field of analog-to-digital converters are modeling, design, and implementation of flash analog-to-digital converters, and the evaluation of the suitability to implement mixed-signal circuits in a partially depleted SOI CMOS technology provided by ST Microelectronics through the MEDEA+ program.

In this work I propose a thermometer-to-binary decoder based on multiplexers. I also propose an approach to reduce the hardware cost and propagation delay of a ones-counter based decoder, e.g., Wallace trees. Further, I evaluate the choice of thermometer-to-binary decoder topology and its effect on the converter performance both during the design and by measurements. During the design I evaluated the decoder topologies both by system level simulations in MATLAB and by transistor level simulations using Cadence. I have also implemented the ADCs and evaluated their performance by measurements.

In this work I also propose and demonstrate an approach for incorporating dynamic element matching in the reference net of a flash analog-to-digital converter. I evaluated this method both during the design phase, by system level and transistor level simulations, as well as by measurements of the implemented circuits.

I implemented all converters in the same PD SOI CMOS technology. This work therefore also contains some conclusions from my experience of using this type of technology for implementation of mixed-signal circuits.

My research work described above has resulted in the following publications related to the thesis work.

- Erik Säll and Mark Vesterbacka, "Silicon-on-Insulator CMOS technology for system-on-chip," in *Proceedings of Swedish System-on-Chip Conference*, Båstad, Sweden, Apr. 2004.

- Erik Säll, Mark Vesterbacka, and K. Ola Andersson, "A study of digital decoders in flash analog-to-digital converters," in *Proceedings*

of IEEE International Symposium on Circuits and Systems, vol. 1, pp. 129–132, Vancouver, Canada, May 2004.

- Erik Säll, K. Ola Andersson, and Mark Vesterbacka, "A dynamic element matching technique for flash analog-to-digital converters," in *Proceedings of Nordic Signal Processing Symposium*, pp. 137–140, Espoo, Finland, June 2004.

- Erik Säll and Mark Vesterbacka, "Design of a comparator in CMOS SOI," in *Proceedings of IEEE International Workshop on System-on-Chip for Real-Time Applications*, pp. 229–232, Banff, Canada, July 2004.

- Erik Säll and Mark Vesterbacka, "A multiplexer based decoder for flash analog-to-digital converters," in *Proceedings of IEEE TENCON*, Chiang Mai, Thailand, Nov. 2004.

- Erik Säll and Mark Vesterbacka, "Mixed signal design in SOI CMOS technology," in *Proceedings of Swedish System-on-Chip Conference*, Tammsvik, Sweden, Apr. 2005.

- Erik Säll and Mark Vesterbacka, "Design and evaluation of a comparator in CMOS SOI," in *Proceedings of National Conference on Radio Science (RVK)*, Linköping, Sweden, June 2005.

- Erik Säll and Mark Vesterbacka, "6 bit 1 GHz CMOS silicon-on-insulator flash analog-to-digital converter for read channel applications," in *Proceedings of European Conference on Circuit Theory and Design*, Cork, Ireland, Aug. 2005.

- Erik Säll and Mark Vesterbacka, "Comparison of two thermometer-to-binary decoders for high-performance flash ADCs," in *Proceedings of IEEE NorChip Conference*, Oulu, Finland, Nov. 2005.

- Erik Säll, *Implementation of Flash Analog-to-Digital Converters in Silicon-on-Insulator Technology*, Linköping Studies in Science and Technology, Thesis No. 1213, Linköping University, Linköping, Sweden, Dec. 2005.

- Erik Säll and Mark Vesterbacka, "6-bit flash ADC with dynamic element matching," in *Proceedings of IEEE NorChip Conference*, vol. 1, pp. 159–162, Linköping, Sweden, Nov. 2006.

I have also been involved in other research work generating the following publications falling outside the scope of this thesis.

- Erik Säll, "A 1.8 V 10-bit 80 MS/s low power track-and-hold circuit in a 0.18 µm CMOS process," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 53–56, Bangkok, Thailand, May 2003.
- Erik Backenius, Erik Säll, and Oscar Gustafsson, "Bidirectional conversion to minimum signed-digit representation," in *Proceedings of IEEE International Symposium on Circuits and Systems*, Kos Island, Greece, May 2006.
- Erik Backenius, Erik Säll, K. Ola Andersson, and Mark Vesterbacka, "Programmable reference generator for on-chip measurement," in *Proceedings of IEEE NorChip Conference*, pp. 89–92, Linköping, Sweden, Nov. 2006.

1.5 Thesis Outline

This thesis is organized as follows. An introduction to the SOI technology is given in Chapter 2. In Chapter 3 an introduction and background to analog-to-digital conversion is presented together with the performance measures used in this thesis. The proposed circuit topologies in this work are presented in Chapter 4. In Chapter 5 the modeling of the flash ADCs is presented. The simulation results of these models are used in the design of the converters presented in Chapter 6. The transistor level simulations results from the design phase of the ADCs are given in Chapter 7, together with the results of the measurements of the implemented ADCs. The results are discussed in Chapter 8. Here are also the SOI CMOS technology discussed based on what is presented in Chapter 2 and the experiences from the design and implementation of the ADCs. The main conclusions are given in Chapter 9, together with some suggestions for future work.

Chapter 2

Silicon-on-Insulator Technology

In SOI technology the thin silicon layer where the devices are laid out is placed on top of an insulating layer. The insulator can be, e.g., sapphire, as for silicon-on-sapphire (SOS) devices, or an oxide layer, as for the SOI CMOS technology used in this work. Devices laid out on top of an insulating layer will be referred to as SOI devices in this work, independent of what type of insulator that is used.

This chapter gives a brief background to the development of the SOI technology. Two different types of SOI CMOS devices, partially depleted (PD) and fully depleted (FD), are presented, followed by a comparison of the SOI CMOS technology with the bulk CMOS technology. A comparison between partially and fully depleted SOI CMOS devices is presented in Section 2.5. In Section 2.6 are electrostatic discharge (ESD) protection circuits for SOI CMOS presented.

2.1 Background

The first SOI substrates were of silicon-on-sapphire type [62], but the first substrates was of poor quality and could therefore not be used for commercial manufacturing of devices. The development advanced thanks to the interest from the military and space industry for radiation hard devices and devices that could operate at high temperatures. From the beginning of the 1980s through the 1990s, the SOI devices, based on silicon-on-sapphire substrates, were mostly used for radiation-hardened and high-temperature applications [21], i.e., low-volume production. In the end of the 1990s, the market for the silicon-on-sapphire based devices increased as they started to be used for RF applications [77, 78]. Consequently, the silicon-on-sapphire has in the latest years become cheaper, which is also due to improved wafer quality and wafer production efficiency. However, since the materials and manufacturing methods are different from what is used for low-cost bulk CMOS production, the cost is still significantly higher than for bulk CMOS.

In 1989 research on the possibility to convert cheap bulk CMOS technologies into SOI CMOS technologies was initiated [83]. One of the goals was to reduce the production cost of the SOI CMOS devices. As a result a few low volume SOI CMOS technologies were in use in the mid 1990s for research purpose [83], using similar materials and manufacturing methods as for bulk CMOS production. The similarities are illustrated by Figure 2.1 where the cross section of a bulk CMOS device and an SOI CMOS device are illustrated. Figure 2.1 shows that the main difference between these two types of devices is the buried oxide (BOX) layer that is used as an insulator below the device, as illustrated in Figure 2.1(b). The introduction of the buried oxide layer creates the thin-film structure that is characteristic for all SOI devices. In 1998 the SOI CMOS technology development took another important step towards the goal of becoming a mature technology, as the first microprocessor manufactured in an SOI CMOS technology become commercially available [83].

As the development advanced, promising properties of the SOI CMOS technology became obvious for future scaled technologies in the sub 100 nm region [7, 49, 72]. It became clear that the SOI CMOS technology really could be a strong competitor to bulk CMOS. In the latest years, it has become widely accepted that the SOI CMOS technology will become one of the future mainstream technologies [7]. In fact, many of the latest mainstream CMOS technologies are SOI CMOS technologies [15], used for several mainstream products. Motivation to why the SOI CMOS technologies are expected to be more common in the future is presented in this chapter.

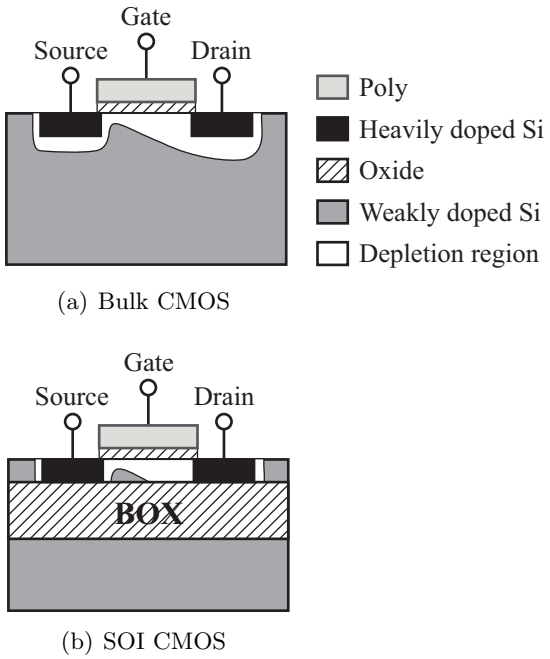


Figure 2.1: Illustration of the cross section of (a) a bulk CMOS and (b) an SOI CMOS device.

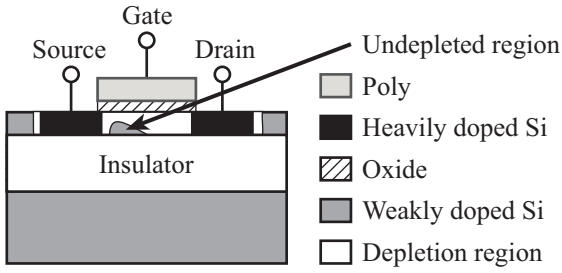
A disadvantage of the technology is that the wafers are more expensive than the wafers used for bulk CMOS production [21]. The more expensive wafers make the total cost for manufacturing higher for SOI CMOS compared with bulk CMOS technologies, even though the processing steps are slightly fewer for SOI CMOS, since, e.g., deep trenches are not necessary in SOI CMOS [21]. The difference in cost between the two technologies has however been reduced over the last years as the quality and yield of the wafer production have improved. The yield is now the same as for regular bulk CMOS [41]. The improved yield reduces the price of the SOI wafers. As a result, a partially depleted SOI CMOS chip was in year 2001 less than 10 % more expensive to manufacture compared with bulk CMOS having a 0.13 μm channel length [88]. Although the difference in cost now is small, the price is, of course, still one of the trade-offs to consider when choosing the technology to use.

2.2 Partially and Fully Depleted SOI

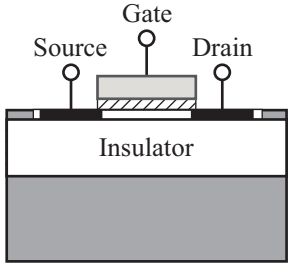
The SOI MOSFET device is a thin-film device that is either partially depleted (PD) or of fully depleted (FD) type. An illustration of the cross section of a partially depleted and a fully depleted SOI device is depicted in Figure 2.2(a) and Figure 2.2(b), respectively.

An undepleted region is present in the body region of the device if the thickness of the thin-film silicon layer where the devices are formed, i.e., the active silicon, is thicker than the depletion depth of the device, as indicated in Figure 2.2(a). The body is therefore only partially depleted. Hence, these devices are referred to as partially depleted SOI devices. The undepleted body region can be charged during operation, giving rise to several unwanted effects, of which the most important are presented later in this chapter, e.g., the kink and history effects.

If the thin-film is made thinner than the depletion depth, typically about 100 nm or less, the whole body region is depleted [64]. This type of devices is referred to as fully depleted devices. Consequently, the body region of the



(a) PD SOI



(b) FD SOI

Figure 2.2: Cross section of (a) a partially depleted and (b) a fully depleted SOI MOSFET device.

device cannot be charged, and several of the unwanted effects appearing in the partially depleted devices are thereby avoided. However, other obstacles exist of which the difficulty of manufacturing is the most important [64]. Since the active thin-film silicon layer must be very thin, its statistical variation of relative thickness over the chip is large. Further, the threshold voltage of the device depends on the thin-film thickness. Consequently, the thin-film thickness variation results in varying threshold voltages over the chip [20]. The thickness must therefore be accurately controlled during manufacturing, which is difficult.

2.3 SOI CMOS vs Bulk CMOS Devices

S comparison between the SOI CMOS technology and the mainstream bulk CMOS technology is presented in this section.

2.3.1 Doping Density and Leakage

When downscaling the bulk CMOS technology the channel doping is increased to avoid the formation of a current path between the drain and source. The current path can be formed by electrostatic coupling between the junctions beneath the channel [15]. The increased doping density reduces the mobility, and as a result, the current drive capability of the device. To compensate for the reduced current drive capability the gate oxide thickness is reduced. The parasitic gate capacitance, which is inversely proportional to the oxide thickness, is thereby increased together with the gate leakage. If the gate leakage is too high, another gate-dielectric with higher permittivity than silicon dioxide (SiO_2) could be used. The gate oxide capacitance for a fixed gate oxide thickness, t_{ox}, would then increase, thereby increasing the gate coupling to the channel. Because of the increased permittivity, a thicker gate oxide can be used, reducing the gate leakage [15].

Since the partially depleted SOI CMOS devices have an undepleted body region below the channel, the electrostatic coupling of the junctions under the channel occurring in the bulk CMOS technology as a result of downscaling can also occur in partially depleted SOI [15]. As in bulk CMOS, the electrostatic coupling in the downscaled partially depleted SOI CMOS technologies is compensated for by increasing the doping density and reducing the gate oxide thickness.

For fully depleted SOI CMOS technologies, the complete depletion of the channel region prevents the formation of the current path below the channel. Hence, the doping density does not need to be increased as much

as for bulk CMOS and partially depleted SOI CMOS technologies [56]. Due to the lower doping density the mobility is higher in fully depleted SOI CMOS compared with bulk CMOS and partially depleted SOI CMOS. In addition, the gate leakage is lower for fully depleted SOI CMOS devices, since a thicker gate oxide can be used. As a result, the parasitic gate capacitance is reduced [15]. The fully depleted SOI CMOS technology is expected to become increasingly more common in the future as the devices are scaled [16], much due to the reduced gate leakage. The difficulties of manufacturing must however first be addressed before the fully depleted SOI CMOS technology can be used for commercial production.

As mentioned, several studies have shown that the leakage can be reduced by about 40 to 90 % if the circuits are implemented in an SOI technology instead of a bulk CMOS technology [15, 59, 64]. In [59] circuits implemented in the SOI technology used in this work are compared with the same circuits implemented in a similar bulk CMOS technology. The study shows that both the dynamic power consumption and the static power consumption is reduced by about 40 % when implementing the circuits in the SOI technology. Further, the two technologies are also evaluated when the method for reducing the static power described in [66] is applied, i.e., the multithreshold-voltage CMOS (MTCMOS) technique. When the MTCMOS technique is applied to the circuits implemented in both technologies the static power consumption is reduced by almost 90 % for the SOI technology compared with the bulk CMOS technology. The area overhead using the MTCMOS technique was the same for both technologies.

The main reason for why the leakage current are reduced in the SOI technology is that the devices are, for these dimensions, dominated by the junction leakage and subthreshold currents [59, 80]. Since the SOI technology has less junction area the junction leakage currents will be lower. At the same time the subthreshold currents are also lower due to lower threshold voltage roll-off, i.e., short-channel effect [18, 59].

2.3.2 Effect of Scaling on Speed Performance

The maximum operating frequency of a bulk CMOS device is in large determined by the magnitude of the total parasitic drain and source junction capacitances, $C_{\mathrm{j,d}}$ and $C_{\mathrm{j,s}}$, respectively. These capacitances consist of the parasitic sidewall junction capacitance $C_{\mathrm{j,sw}}$ and the bottom drain and source area parasitic junction capacitances, C_{db} and C_{sb}, respectively, according to

$$C_{\mathrm{j,d}} = C_{\mathrm{j,sw}} + C_{\mathrm{db}} \tag{2.1}$$

for the drain junction capacitance, $C_{\mathrm{j,d}}$, of the bulk CMOS devices.

In the case of a bulk CMOS device the distance between the charged areas of the parasitic bottom-area junction capacitances is the width of the junction. The charged areas are the areas where the charges accumulates in the drain, source, and substrate. When introducing the buried oxide the distance between these charged areas is increased by the thickness of the buried oxide. Consequently, the contribution from the bottom-area drain and source junction capacitances to the total drain and source parasitic junction capacitance is significantly reduced. The total drain and source parasitic capacitances for SOI CMOS devices are thereby reduced by a factor of four to seven compared with a bulk CMOS technology of the same dimensions [20, 56, 86]. The speed of the SOI CMOS devices are therefore increased compared with the bulk CMOS devices of the same size. Hence, the SOI CMOS technology is about one generation ahead of the bulk CMOS technology in terms of device speed [21, 56]. The same conclusion can not generally be drawn for the whole circuit, since the parasitics of the interconnects will reduce the maximum operation frequency.

Now consider partially depleted SOI CMOS devices in relation to bulk CMOS devices, both having the body tied to the source. The speed enhancement of the partially depleted devices is then entirely due to the reduction of the parasitic bottom-area drain and source junction capacitances [20, 72]. When the devices are downscaled, the drain and source bottom-areas are reduced for both types of devices, which reduces the parasitic drain and source bottom junction area capacitances. As these capacitances are reduced, the relative performance enhancement of the partially depleted devices diminishes. The performance advantage, in terms of speed for digital circuits over bulk CMOS, is thereby reduced to less than 10 % for body tied devices when the technology scaling approaches a gate length of 70 nm [72]. Hence when approaching a minimum gate length of 70 nm, fully depleted SOI CMOS should be preferred to utilize the advantages of SOI CMOS over bulk CMOS, due to, e.g., the improved current drive capability, as explained next.

2.3.3 Current Drive Capability

The body factor n of a bulk CMOS or SOI CMOS device is given by [19]

$$n = 1 + \frac{C_{\mathrm{ch,b}}}{C_{\mathrm{g,ch}}}, \tag{2.2}$$

where $C_{\mathrm{ch,b}}$ is the parasitic capacitance between the channel and body, and $C_{\mathrm{g,ch}}$ is the parasitic capacitance between the gate and channel. In fully depleted SOI devices, the insulating layer and the complete depletion of the body reduce the channel to body capacitance $C_{\mathrm{ch,b}}$. As seen from (2.2), reducing $C_{\mathrm{ch,b}}$ reduces the body factor of the fully depleted SOI CMOS devices, compared with both bulk CMOS devices and partially depleted SOI CMOS devices. As an effect, the coupling between the gate and the channel improves. Studies have shown that the body factor n can be as low as 1.05-1.1 for fully depleted SOI CMOS, compared with 1.3-1.5 for bulk CMOS and partially depleted SOI CMOS [19, 20, 32, 33]. The current drive capability, given by the saturation current $I_{\mathrm{D,sat}}$, which is proportional to $1/n$, is thereby higher in fully depleted SOI CMOS compared with a bulk CMOS or partially depleted SOI CMOS technology [21]. Further, the ratio between the transconductance g_{m} and the DC drain current I_{D} is given by (2.3a) for weak inversion and (2.3b) for strong inversion [19]. In equation (2.3a) q is the electron charge, k is Boltzmann's constant, and T is the temperature in Kelvin. The channel charge carrier mobility is denoted μ in (2.3b). Further, C_{ox} is the gate oxide capacitance per unit area, W is the width of the transistor, and L is its channel length.

$$\left.\frac{g_{\mathrm{m}}}{I_{\mathrm{D}}}\right|_{\text{weak inversion}} = \frac{1}{n}\frac{q}{kT} \tag{2.3a}$$

$$\left.\frac{g_{\mathrm{m}}}{I_{\mathrm{D}}}\right|_{\text{strong inversion}} = \frac{1}{\sqrt{n}}\sqrt{\frac{2\mu C_{\mathrm{ox}} W/L}{I_{\mathrm{D}}}} \tag{2.3b}$$

The lower body factor n of fully depleted SOI CMOS devices yields a larger $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio compared with bulk CMOS and partially depleted SOI CMOS devices. Hence for the same drain bias current I_{D} the transconductance g_{m} is larger for devices implemented in fully depleted SOI CMOS than in a bulk CMOS or partially depleted SOI CMOS technology. The larger transconductance also improves the device speed, in addition to the reduced parasitic drain and source bottom-area junction capacitances. It is worth noting that the $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio is proportional to $1/\sqrt{n}$ in strong inversion, while it is proportional to $1/n$ in weak inversion. Due to the lower body factor n in fully depleted SOI, its advantage over bulk CMOS and partially depleted SOI CMOS devices is even larger when they operate in weak inversion. Fully depleted SOI CMOS circuits are therefore especially suited for low-voltage and low-power applications [19, 32].

2.3.4 Unity-Gain Frequency

For analog circuits the DC open loop voltage gain, A_0, and unity-gain frequency, f_T, of the devices, are of importance for the overall circuit performance. Consider the transistor in the common source configuration, illustrated in Figure 2.3, biased with the drain bias current I_D delivered from an ideal current source. If the load is C_L, the expression for the DC gain A_0 (2.4) and unity-gain frequency f_T (2.5) becomes [85]

$$A_0 = -\frac{g_m}{I_D} V_A \tag{2.4}$$

and

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_L}, \tag{2.5}$$

where V_A is the Early voltage

$$V_A = \frac{I_D}{g_{ds}}, \tag{2.6}$$

i.e., the ratio between the DC current and the small-signal output conductance g_{ds}.

The DC gain and the unity-gain frequency are the same for partially depleted SOI CMOS as for bulk CMOS devices of the same dimension, since the body factor and consequently the ratio g_m/I_D are the same. For fully depleted SOI CMOS devices, the body factor is lower, yielding a larger g_m/I_D ratio. The DC gain A_0 and unity-gain frequency f_T is therefore improved when using fully depleted SOI CMOS compared with using bulk CMOS and partially depleted SOI CMOS devices. The improvement of A_0 and f_T is between 9 % and 20 % in strong inversion, and between

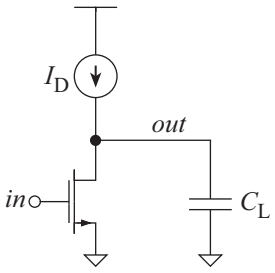


Figure 2.3: Transistor in common source configuration.

18 % and 43 % in weak inversion. These are the main reasons why circuits implemented in a fully depleted SOI CMOS technology are expected to outperform the bulk CMOS counterpart in terms of gain, speed, and power consumption, especially for low-voltage and low-power applications [33].

2.3.5 Latch-Up and Device Density

In an SOI CMOS transistor the drain and source junctions reach through the silicon thin-film to the buried oxide. Hence, the buried oxide isolates the thin-film silicon from the substrate. This SOI CMOS technology characteristic prevents the formation of parasitic bipolar transistors in the SOI CMOS technologies due to the isolation of the negative-channel metal oxide semiconductor (NMOS) and positive-channel metal oxide semiconductor (PMOS) devices [21, 45, 56]. The latch-up effect in bulk CMOS is therefore absent in SOI CMOS.

In bulk CMOS, the latch-up effect is avoided by ensuring that the minimum distance between the NMOS and PMOS devices is sufficiently large, by adjusting the doping level where the transistors are introduced, and by controlling the substrate voltage by using substrate contacts. For SOI CMOS technologies, having no latch-up effect, the minimum distance between the devices can be smaller. In addition, the deep oxide filled trenches often used in bulk CMOS technologies to achieve a good isolation between the devices can be replaced by shallow trenches in SOI CMOS technologies due to the thin-film structure on top of the buried oxide [21, 45]. The minimum space between the devices in an SOI CMOS technology is thereby only dependent on the technology constraints on the minimum width of the shallow oxide filled trenches [56]. The device density can therefore be higher in SOI CMOS technologies than in bulk CMOS technologies, which is an advantage in digital circuits, especially in, e.g., memories.

For analog circuits the layout must be done so that the self-heating, discussed in Section 2.5.2, and other thermal effects are minimized [101]. It is thereby more difficult to make any general conclusion on the device density when comparing bulk CMOS technologies with SOI CMOS technologies for analog circuits.

2.3.6 Radiation Hardness

Radiation particles incident upon a silicon wafer ionize some of the silicon atoms. If the silicon is replaced by a thin-film silicon layer, like in SOI CMOS devices, the radiation particles are more likely to pass through the silicon

thin-film without ionizing the silicon atoms in the thin-film [93]. In the case of an SOI CMOS technology, the particles may still ionize some of the silicon atoms in the substrate, but since the active silicon layer is separated from the substrate by the buried oxide, the devices implemented in an SOI CMOS technology are less affected by the incident radiation [27, 56]. For that reason, the radiation hardness is better for SOI CMOS than for bulk CMOS technologies [27]. Hence, using an SOI CMOS technology for implementing, e.g., memories, would reduce their soft-error rate, compared with if they were implemented in a bulk CMOS technology [21, 56].

There is the possibility that some of the incident particles are trapped in the buried oxide, which could turn on the back channel, and thereby reduce the threshold voltage of the device [56]. The back channel is an unwanted channel that can be formed in the bottom of the active silicon [56]. The effect of the incident radiation on the SOI CMOS devices is however still much less, compared with its effect on bulk CMOS devices.

The incident radiation particles can also ionize the oxide atoms in the buried oxide layer. The ionized oxide atoms can form a conducting trace through the oxide. Some of the incident radiation particles can then travel back to the silicon thin-film on top of the insulating oxide, thereby causing soft-errors. To avoid the formation of conducting traces through the insulator, the more radiation hard SOS substrates could be used instead. The better radiation hardness is why SOS often is used for, e.g., space applications.

2.3.7 Crosstalk

One of the methods to reduce the latch-up effect in bulk CMOS technologies is to use a substrate with sufficiently low resistivity [51]. The use of a substrate with too low resistivity would give too high crosstalk, poor noise performance, and reduced quality of the implemented passives, such as resistors, capacitors, and inductors. The resistivity is therefore chosen from several trade-offs, and is therefore often limited to about 2 kΩm [21].

In SOI CMOS technologies the latch-up effect is not present. The lack of latch-up effect can be utilized by using different resistivity in the silicon above and below the insulator. The resistivity of the substrate below the insulator can be increased and the resistivity of the silicon on top of the insulator can be maintained on the same level as before, or even reduced [56]. If the substrate resistivity is increased the crosstalk is significantly reduced, compared with bulk CMOS technologies. SOI CMOS with high resistivity substrate actually seems to be a good candidate for future high frequency

mixed signal integrated circuits [76]. Further crosstalk improvements can be reached if guard rings are introduced into the silicon thin-film and the substrate [48]. These issues are discussed in more detail in Section 2.4.

2.3.8 Passives

In addition to a reduced crosstalk, the quality factor (Q) of on-chip inductors is also improved when increasing the resistivity of the substrate [28, 43, 61, 78]. For bulk CMOS with a substrate resistivity of about 2 kΩm the Q factor of inductors is about four to six [21]. If using SOI CMOS with high resistivity substrate, the Q factors of the inductors can be significantly increased. Single metal layer inductors with a Q factor of 11 for a substrate resistivity of 1 MΩm [29], and a Q factor of 50 for a substrate resistivity of 20 kΩm and multiple metal layers have been reported [75]. The SOI CMOS technology therefore has the potential of being used for digital, mixed signal, and RF circuits implemented on the same chip [20]. Hence, the SOI CMOS technology is a good candidate as a mainstream technology for future system-on-chip implementations.

2.4 Substrate Noise

In this section a brief introduction to the dominant sources of substrate noise is given together with comments on the main differences between bulk CMOS and SOI CMOS in terms of substrate noise. The dominant substrate noise sources are presented first with comments on their effect in bulk CMOS and SOI CMOS technologies.

2.4.1 Substrate Noise Sources

The term substrate noise refers to all unwanted potential variations introduced in the substrate. They can be caused by, e.g., the switching of digital circuits or due to currents injected into the substrate through the substrate contacts [24]. The analog parts of a circuit are especially vulnerable to the substrate noise.

There is basically three different dominant sources of substrate noise. These are noise coupled from the digital power supplies, noise coupled from switching source and drain nodes, and noise due to impact ionization in the channel of the transistors, as explained in Section 2.5.1. The first noise source is also often classified as an indirect cause of substrate noise, and the latter two is classified as direct causes of substrate noise [24]. The

coupling of the simultaneous switching noise (SSN) on the power supplies contributes most to the substrate noise. The noise coupled from switching source and drain nodes and the impact ionization contribute only by about 10 % and 1 % of the total noise, respectively [9]. The noise coupled from the power supplies is predicted to be even more dominant in the future as the technologies are continuously scaled [5].

Power Supply Noise

Most of the noise coupled from the supply is due to the noise on the digital ground [109]. The digital ground is directly connected to the substrate by the substrate contacts. Due to the large amount of substrate contacts the impedance between the digital ground and the substrate is low. Much of the noise on the digital ground is thereby coupled to the substrate. The noise on the power supplies is in turn mainly due to the di/dt-noise due to the inductance and resistance of the power supply connections [109]. The inductance on the power supply in combination with the on-chip capacitance give rise to damped oscillations on the power supply, known as simultaneous switching noise (SSN). The di/dt-noise is mainly due to the inductance of the bond wires and the printed circuit board (PCB) to which the chip is attached. The effect of the latter cannot be completely eliminated, but it can be reduced by proper decoupling of the power supplies on the PCB [4].

In an SOI technology, especially a fully depleted SOI technology, the coupling from the supplies to the substrate is weaker. The reason is the lack of substrate contacts. Instead the coupling has the same mechanism as the coupling from switching nodes, mentioned below, i.e., capacitive coupling through the buried oxide down to the substrate below the oxide. Hence, the coupling is weaker than compared with having resistive coupling through substrate contacts.

Noise from Switching Nodes

In a CMOS technology the pn-junction between the drain or source region and the substrate forms a reverse biased diode. Since the diode is reverse biased a depletion region between the negatively doped and the positively doped regions is present, as illustrated by Figure 2.1(a). In the case of an NMOS device the drain and source regions would be heavily negatively doped and the substrate would be weakly positively doped. The depletion region thereby works as the insulator between the plates of a capacitor, where the positively and negatively doped areas are the plates of the capac-

itor. Hence there will be a capacitive coupling between the source or drain and the substrate. When the device is switching the potential on the source or drain varies and due to the capacitive coupling to the substrate these variations will also show up as a varying substrate potential [109]. Since it is unwanted it is considered to be noise, i.e., substrate noise.

For the SOI technology the situation is different. As illustrated by Figure 2.1(b) the device is placed on top of the insulator. The insulating layer is much thicker than the depletion region of the parasitic diode in the bulk CMOS case. The parasitic capacitance between the drain or source nodes, and the substrate is therefore smaller. The smaller parasitic capacitance yield that less noise is coupled from the drain and source to the substrate in the case of an SOI technology.

Impact Ionization

The channel current of a device consists of the charge carriers in the channel that are accelerated by the electric field in the channel and travel from the source to the drain. The magnitude of the electric field is set by the voltage between the drain and the source of the device, and also by the physical length of the channel. If the drain-source voltage (V_{ds}) is increased or the channel length is decreased the electric field in the channel increases, and the charges accelerate to a higher velocity, i.e., have more energy [21, 93]. The charges that travel through the channel always have a certain likelihood to collide with the atoms of the crystal lattice. As the charges gain more energy the likelihood that they will knock out charges from the lattice when they collide is increased, hence some of the atoms in the lattice will be ionized. The process is called impact ionization, and is illustrated by Figure 2.5(a). The figure illustrates a transistor implemented in an SOI CMOS technology, but the same principle applies for transistors implemented in a bulk CMOS technology. Note also that since the charges will have the highest velocity near the drain, it is most likely that the impact ionization occurs near the drain.

The charges generated by the impact ionization yield a substrate current, i.e., they generate substrate noise. However, for an SOI CMOS device the current (charges) generated by the impact ionization will remain in the device and not affect the surrounding devices through the substrate. Hence, for an SOI CMOS technology the impact ionization will have an important effect on the individual device, but it will affect neighboring devices little. The effects of the impact ionization is discussed in more detail in Section 2.5.1.

2.4.2 Substrates and Substrate Modeling

In this section the differences between the substrate models for different type of substrates is presented and commented. The substrates considered are heavily and lightly doped bulk CMOS substrates, and SOI CMOS substrates. The models are used to highlight some of the differences between the substrates in terms of substrate noise and coupling through the substrate.

Heavily and Lightly Doped Bulk CMOS Substrates

In a mainstream bulk CMOS technology the substrate is heavily doped to achieve a low substrate resistance to counteract latch-up, as explained in Section 2.3.7. The region where the devices are located are somewhat lighter doped. For such substrates the low substrate resistivity implies that it is a good approximation to consider the whole substrate as one node. For this approximation, and under the assumption that the operating frequency is relatively low (less than 1 GHz) [109], the model in Figure 2.4 is a good approximation for the coupling between the two nodes (A and B) through the substrate. The common substrate node is the node S in Figure 2.4 [109]. Since the substrate has a low resistivity the substrate potential will be similar over the whole chip. The drawback is however that the noise injected in the substrate will also spread through the whole chip. To avoid the noise from spreading through the substrate, or at least reduce the magnitude of the noise, there are also substrates that are lightly doped, i.e., their resistivity is higher. Since the resistivity is higher the noise coupling is reduced, i.e., the noise is dampened more per unit distance. However, for

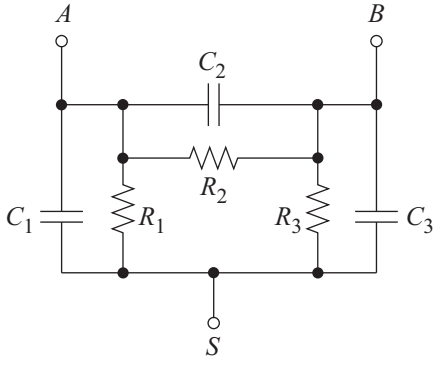


Figure 2.4: Illustration of the substrate coupling model for a lightly doped bulk CMOS substrate.

short distances the noise coupling is similar for heavily and lightly doped substrates [46]. A drawback with a reduced doping density is also that slip lines can form during the creation of the shallow trench isolation [120], which degrades the yield of the manufactured circuits. The slip lines are dislocations in the silicon crystal lattice caused by the furnace processing step. The slip lines may form if, e.g., the temperature distribution is uneven, or if materials with different thermal properties are used. The latter is the case for the shallow trenches since these are oxide (SiO_2) filled wells introduced into the silicon.

When the resistivity of the substrate is increased a distributed model of the substrate must be used. There are different methods to derive the substrate model, e.g., solving Poisson's equations numerically with Green's equations and boundary element method, or extracting the network from a 3-dimensional mesh [107].

Silicon-on-Insulator CMOS Substrates

For SOI CMOS substrates the area where the devices are introduced is separated by an insulating layer, e.g. SiO_2 layer as in the technology used in this work, as illustrated by Figure 2.1(b). The insulator yields a better isolation than for bulk CMOS between the device and the substrate, hence the device is less affected by the substrate noise for low frequencies. If the substrate below the insulator is highly doped and the frequency is above about 1 GHz (the exact frequency depends on the insulator thickness and the circuit area), the noise performance is similar to a bulk CMOS technology [3, 113]. The similar noise performance at high frequencies is due to the capacitive coupling between the device and the substrate through the insulator. In addition, when comparing the noise performance of SOI CMOS with the noise performance of a twin-well bulk CMOS technology the performance is similar even for frequencies below 1 GHz [113].

As for a bulk CMOS technology the substrate noise performance is improved if the resistivity of the substrate is increased, i.e., reducing the doping density of the substrate. Studies show that an increase in the resistivity from 2 kΩm to 500 kΩm yields a better noise performance of the SOI CMOS technology than for lightly doped bulk CMOS up to about 10 GHz [113]. A disadvantage with lightly doped bulk CMOS is that slip lines may form during the creation of the shallow trenches used for isolation [120]. However, for SOI CMOS the trenches are formed in the active silicon on top of the insulator, which is highly doped silicon, and not in the high resistivity substrate below the insulator. Hence there will be less yield degradation

due to the formation of slip lines when using SOI CMOS.

2.5 Partially vs Fully Depleted SOI

In this section we go into more details regarding the differences between fully depleted and partially depleted SOI CMOS technologies. The most important unwanted effects of SOI compared with bulk CMOS are presented. Most of them does only appear in partially depleted SOI technologies, but the thermal effects are affecting both types of devices.

2.5.1 Kink and History Effect

Due to the high electric field in the pinched-off region of the channel, impact ionization occurs in the saturation operating region of an SOI MOSFET [21]. Electron-hole pairs are generated by the impact ionization, which are separated by the electric field near the drain. In a partially depleted SOI NMOS device the electrons drift towards the drain and the holes are injected into the undepleted body region [21, 93], as illustrated in Figure 2.5(a).

Since there is a potential barrier between the body and source, the body potential increases rapidly to a value equal to the built-in potential of the body-source junction [56]. The increase in body potential reduces the threshold voltage of the device via the body effect. The reduction of threshold voltage can be observed in the I_d/V_{ds} characteristic as a sharp increase, a kink, in the drain current at the onset of impact ionization, as illustrated in Figure 2.5(b) [56, 93, 96]. The effect is called the kink effect.

The partially depleted SOI device has an undepleted body region where charges generated by gate-to-body tunneling, impact ionization, or diode leakage, may accumulate, due to a limited recombination time constant [56]. The charge accumulation alters the body potential, and thereby the threshold voltage of the device. As a result, the threshold voltage, and hence gate delay for digital circuits, will vary depending on the frequency, bias conditions, and the switching history. This is the history effect [64]. The history effect will give different behavior in DC and transient operation, which is a cumbersome property for analog applications, where the DC bias should set the transient characteristics.

The lack of undepleted body region in fully depleted SOI yields that neither the history effect nor the kink effect exists in such devices [56, 119]. In partially depleted SOI, these effects can be reduced by using body contacts. The body contacts remove the accumulated holes in the body, and stabilize

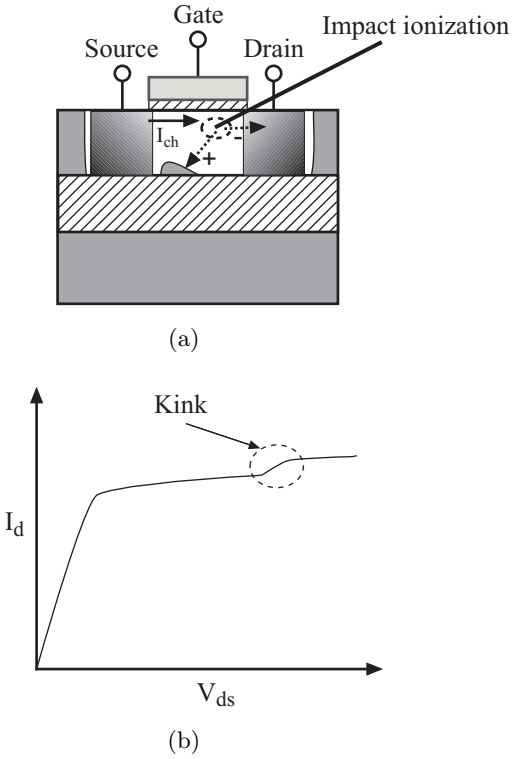


Figure 2.5: Partially depleted SOI NMOS device during (a) impact ionization giving rise to (b) the kink effect.

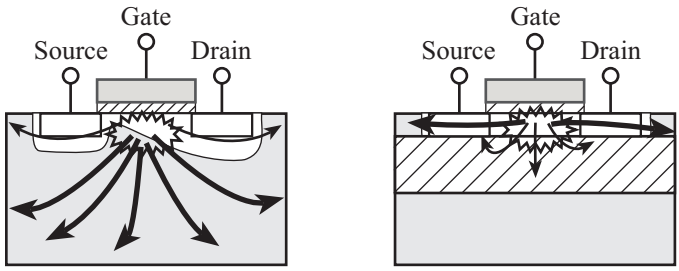
the body potential, i.e., it is the same method used in bulk CMOS technologies to avoid having a floating body. However, this method is somewhat less efficient in the SOI technology since the body and thereby the body contact area is smaller. Hence the body contact has a higher resistance. Two other methods for reducing the kink effect are either to use cascodes, or to optimize the bias point and transistor sizes so that the transistors that sets the gain and current operates outside the kink region [13, 14]. However, as the devices are scaled the body contact area is reduced, which increases the body contact resistance. Hence, for future SOI CMOS technologies, other methods or fully depleted SOI CMOS instead of partially depleted must be used.

2.5.2 Self-Heating and Thermal Coupling

Due to the buried oxide layer in SOI CMOS technologies the thermal conductivity is about 100 times lower for these devices compared with bulk CMOS devices [101]. Most of the heat generated in a bulk CMOS device is transferred to the substrate below the device and only little heat is transferred to neighboring devices.

For an SOI CMOS device the situation is different. Due to the poor thermal conductivity of the insulating layer, more of the heat generated by the device will remain in the device, which increases its temperature. In addition, more heat is transferred to neighboring devices, which increases their temperature as well. The heat transfer is illustrated by Figure 2.6. As a result, the local device temperature can vary significantly during operation when the power dissipation of the device changes. The effect is known as self-heating and it depends on several parameters. The most important parameter is the power consumption of the device, since this corresponds to the generated heat. The increased device temperature yields a decrease of the electron and hole mobility, which in turn results in a decrease of drain current. The variation of the drain current due to self-heating can be as much as 20-25 % [56]. For bulk CMOS, the device temperature is both lower and more evenly distributed compared with SOI CMOS circuits.

The self-heating effect has a time constant in the order of a microsecond [57], hence the variation becomes less important for fast switching logic circuits, since the circuit will reach a thermal equilibrium [56, 101]. The characteristics of the devices are then approximately constant.



(a) Bulk CMOS (b) SOI CMOS

Figure 2.6: Illustration of the heat transfer in (a) bulk CMOS and (b) SOI CMOS.

Thermal Effects in Analog Circuits

Considering analog circuits, the effects of self-heating are more severe than for digital circuits. The reason is that the self-heating in combination with poor thermal coupling between the devices on the chip degrade the matching between the devices, and worse, the thermal coupling may introduce new feedback paths, i.e. thermal feedback [57]. Hence unexpected instability can occur that may not be visible in circuit simulations during the design if the thermal coupling is excluded. The thermal related matching and potential instability issues must be considered when designing analog circuits, e.g., by finding methods to reduce the unwanted thermal effects. A few methods to reduce the thermal effects are touched upon in this section.

To improve the device matching, the devices can be placed in the same well to equalize the local temperature. This applies well to the general layout strategies for bulk CMOS, e.g., the layout of the input pair of a differential amplifier, or a current mirror. However, placing the input and output transistors of a current mirror with several outputs close together causes the heat generated by the output transistors to be more easily transferred to the input transistors than if they are separated by a large distance. The output transistors closest to the input transistor therefore affect the input transistor more than the output transistors further away. This generates a mismatch between the output transistors since they do not have the same effect on the input transistors [101]. The heat flow of a current mirror is illustrated in Figure 2.7, which also is the floor plan of the current mirror. The heat flow Φ_1 from the output transistor M1 causes a voltage shift $\Delta V_{\mathrm{ds},0}$ of the input transistor M0. The voltage shift results in the current shift ΔI_1 of the output transistor Mx. Since the transistor Mx is further away from the input than M1 the heat flow from Mx, Φ_x, has less effect on the input transistor M0. Consequently, since Mx and M1 have different effect on M0 this results in a mismatch between the output transistors M1 and Mx.

The ability to simulate the thermal coupling in analog circuit design in SOI technology is important, especially when the technology is scaled down [57, 101]. The thermal effects must therefore be included in the models. Today the self-heating effect is easily included [87]. However, the thermal heat transfer is also important to include, if not even more important, since the heat transfer can result in the unwanted feedback paths [57, 101]. Models and simulators that can fully simulate the thermal effects, both self-heating and thermal heat transfer, are required. In addition, for accurate simulation of the thermal coupling the floor plan must be known.

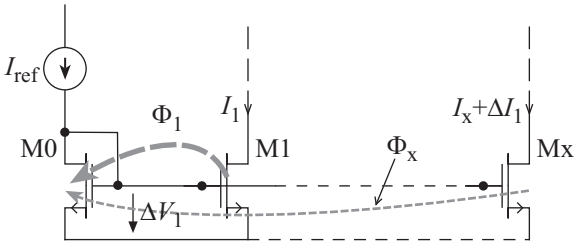


Figure 2.7: The heat transfer in a current mirror.

2.6 ESD Protection

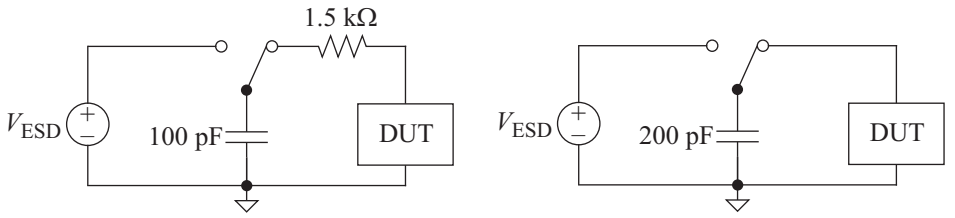
During the manufacturing, transport, and later handling of the circuits by the end user, electrostatic charges may build up. An electrostatic discharge (ESD) can then occur which can seriously damage the circuits if they are not properly protected. The protection in bulk CMOS is commonly accomplished by bypassing the ESD currents through a diode network [56]. Hence their purpose is to prevent the ESD current from entering the core of the chip and damage the circuits. Many ESD protection circuits implemented in SOI are also based on diode networks. Due to the thin-film structure the diodes must however be realized in different ways than for bulk CMOS. Some of the ESD protection circuits used in SOI CMOS technologies are presented in Section 2.6.2.

2.6.1 ESD Models

As long as the ESD currents are not large enough to damage the ESD protection circuits, the circuits in the core of the chip are protected if the ESD is within the specified values. To design the ESD protection circuits, the sources of the ESD have to be modeled to get an idea of the magnitude of the currents or voltage pulses that the protection circuits must withstand. The two models illustrated in Figure 2.8 are commonly used for this purpose [53].

The first model is the human body model, shown in Figure 2.8(a). In this model, the discharge of the human to the device is modeled by the discharge of a 100 pF capacitor through a 1.5 kΩ resistor. The capacitor is charged by the ESD voltage V_{ESD}.

The machine model models the discharge of charge built up on machines during the manufacturing, and is illustrated by Figure 2.8(b). The difference from the human body model is the absence of the human body resistance,



(a) Human body (b) Machine

Figure 2.8: Illustration of (a) the human body model and (b) the machine model for ESD testing and design.

and that the capacitance of the capacitor is increased to the double. The absence of the resistance implies that this model yields higher ESD currents compared with the human body model for the same V_{ESD}.

2.6.2 ESD Protection Circuits for SOI CMOS

The ESD protection circuits designed for bulk CMOS can in general not be used for SOI CMOS. In bulk CMOS technologies it is easy to get sufficiently large area of the vertical junctions between the positively and negatively doped areas (pn-junctions) to remove the ESD currents. In SOI CMOS the use of a thin-film separated from the substrate by the insulating layer results in a higher current density in the pn-junctions, since the pn-junction area is small due to the thin-film structure. In addition, no vertical pn-junctions are available due to the buried oxide layer. The power density is thereby higher, yielding a higher device temperature. The temperature rise is not desirable due to the poor heat dissipation of SOI CMOS compared with bulk CMOS. The larger peak temperature of the devices can do serious damage, which is one reason to why many of the ESD protection approaches used for bulk CMOS technologies cannot directly be used in SOI CMOS technologies [56, 96]. Another reason is the difficulty to accomplish a sufficiently large pn-junction area on a small chip area in SOI CMOS compared with bulk CMOS technologies. Bulk CMOS ESD protection circuits therefore consume a larger area in an SOI CMOS technology compared with a bulk CMOS technology [114, 115].

In a partially depleted SOI CMOS technology, the gated double-diode networks using CMOS, PMOS, or NMOS devices shown in Figure 2.9 can be used [93, 115]. These ESD protection circuits are directly mapped from bulk CMOS ESD protection circuits, based on high perimeter diode struc-

tures [115]. The body contact of the transistors serves as the anode or cathode, and the device realizes a diode-like structure for the ESD protection. The ESD protection circuit in Figure 2.9(c) is the one used in this work.

When ESD occurs the channel is turned on, causing not only the body to source and drain path to conduct, but also the body to channel path [56]. The gated double-diode approach thereby provides a low resistivity ESD bypass path, which can allow a higher ESD current than many of the diode structures used in bulk CMOS technologies. The performance is therefore close to what it is in bulk CMOS. The ESD robustness can be above 4 kV for 500 μm wide and about 4 μm long partially depleted SOI CMOS devices using the human body ESD model [115]. The gated double-diode approach can however not be used if body contacts are not available.

For fully depleted SOI CMOS technologies other approaches have to be used. One is to use lateral unidirectional bipolar type insulated gate tran-

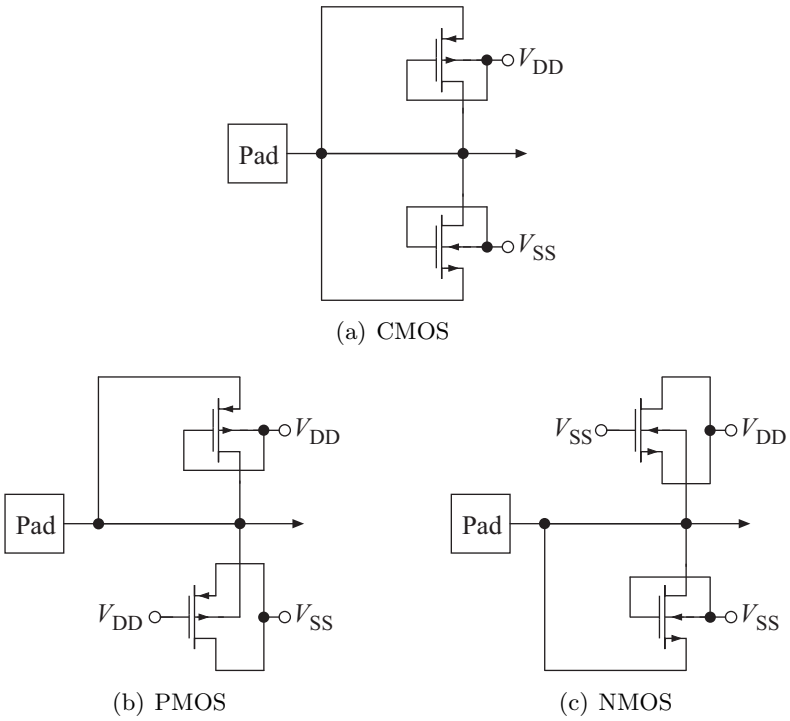


Figure 2.9: Gated double-diode networks with (a) CMOS, (b) PMOS, and (c) NMOS body contacted SOI CMOS devices.

sistors, also known as Lubistors [56, 114, 115]. No body contact is required using the Lubistor approach and the lateral structure of the Lubistors make them especially suited to fully depleted SOI technologies. In Figure 2.10(a) a cross section of a Lubistor is shown, and its schematic symbol is shown in Figure 2.10(b). An SOI CMOS ESD protection circuit for an input pad is depicted in Figure 2.10(c) for a technology with different I/O and core supply voltages [114]. The circuit uses Lubistors instead of the diodes used in bulk CMOS technologies, or the gated double-diode networks in Figure 2.9. The circuit is in fact directly mapped from an ESD protection circuit used in a bulk CMOS technology [114]. The ESD protection diodes in the bulk CMOS technology are simply exchanged for Lubistors. The circuit in Figure 2.10(c), implemented in SOI CMOS, can withstand ESD pulses exceeding 6.5 kV using the human body model, while the bulk CMOS implementation failed at 4.3 kV in the experiment presented in [114]. The ESD robustness of the Lubistor based circuits is not their only advantage. In addition, studies have shown that the ESD protection properties of the Lubistors improve with technology scaling [114]. Hence it is a promising approach for the future as well.

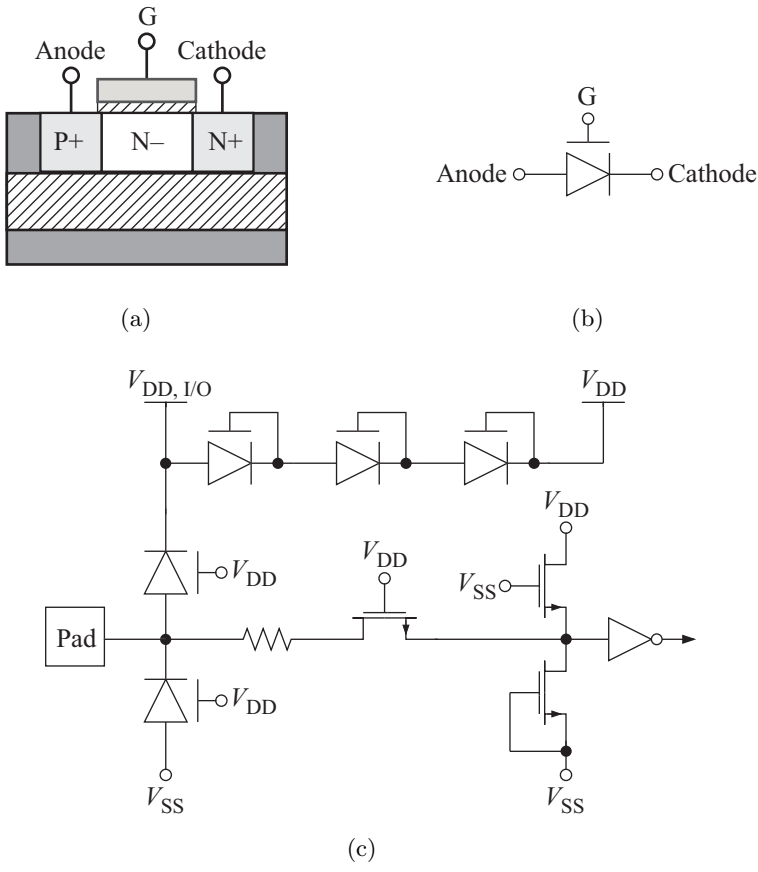


Figure 2.10: Illustration of (a) the cross section of a Lubistor, (b) the Lubistor schematic symbol, and (c) an SOI CMOS ESD protection circuit implemented using Lubistors.

Chapter 3

Analog-to-Digital Conversion

In this chapter an introduction to analog-to-digital conversion is given and the performance measures used in this work to evaluate the ADC performance are defined. The flash ADC topology is presented in more detail, followed by an introduction to some of the error sources encountered in flash ADCs, and methods to compensate for these error sources. In the last part of this chapter it is explained how dynamic element matching (DEM) can be introduced in flash ADCs.

3.1 ADC Function

The ADC can be modeled as a sample-and-hold (SH) circuit followed by a quantizer, as illustrated by Figure 3.1(a), where the dashed frame illustrates the schematic symbol of an ADC. The SH circuit samples the input voltage V_{in} and generates the sampled voltage V_{s}. The sampled voltage is held

while the quantizer converts the sampled voltage V_s to the digital output D_{out}. The conversion is illustrated by Figure 3.1(b), where a ramp input is converted. The result of the conversion is the digital output D_{out} given by (3.1a) [108], where q_s is the quantization step and q_e is the quantization error. The number of bits in the digital output, denoted N, is the resolution of the ADC.

$$\frac{V_s}{q_s} = D_{out} + q_e \tag{3.1a}$$

$$D_{out} = \sum_{i=0}^{N-1} d_i 2^i \tag{3.1b}$$

The quantization step size q_s is equivalent to one least significant bit (LSB) and is given by the ratio between the full-scale voltage of the ADC, V_{FS} and the number of quantization steps according to (3.2). The full-scale voltage is the maximum input voltage that can be applied to the converter input without saturating the converter.

$$q_s = \frac{V_{FS}}{2^N} \tag{3.2}$$

The quantization error q_e is the difference between V_{in}/q_s and the quantized digital signal D_{out}, and is shown in Figure 3.1(b) for a ramp input. The absolute quantization error should be within one LSB for correct operation [108], i.e.,

$$-\frac{q_s}{2} < q_e \leq \frac{q_s}{2}. \tag{3.3}$$

3.2 Quantization Noise

Assuming that the quantization error is uniformly distributed on the interval given by (3.3), the mean-squared value of q_e can be calculated according to (3.4) [108].

$$\langle q_e^2 \rangle = \frac{1}{q_s} \int_{-\frac{q_s}{2}}^{\frac{q_s}{2}} q_e^2 \, d(q_e) = \frac{1}{12} q_s^2. \tag{3.4}$$

The mean-squared value of q_e, given by (3.4), can be used to derive the well known expression in (3.5b), which is the signal-to-quantization noise ratio (SQNR) for an N-bit ADC with a sinusoid input. The root mean-squared value of a sinusoid with an amplitude of $V_{FS}/2$ is $V_{FS}/(2\sqrt{2})$, where

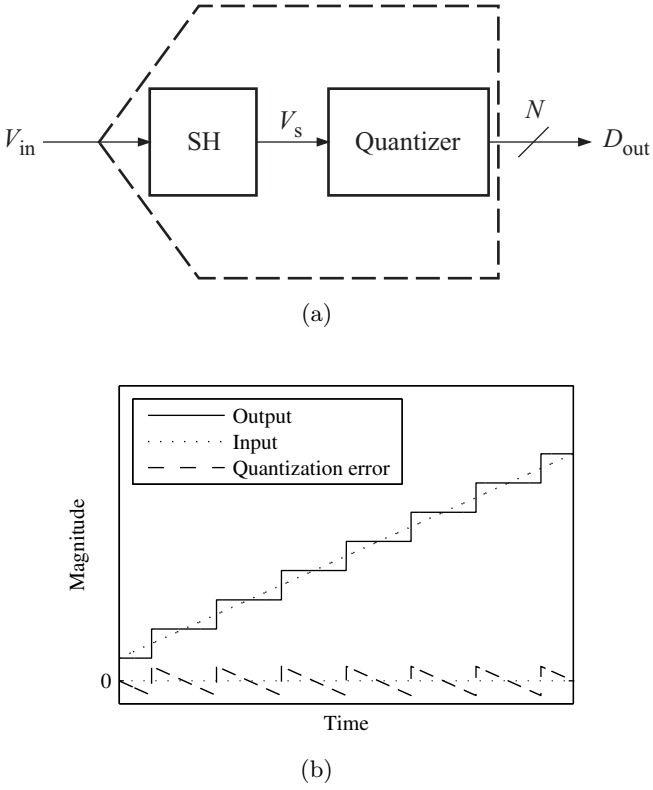


Figure 3.1: (a) The block diagram of an ADC with (b) the ADC input and output, as well as its quantization error for a ramp input.

$V_{FS} = q_s 2^N$ [51, 108]. The SQNR for an N-bit quantized full-scale sinusoid signal can then be calculated by the ratio of the root mean-squared value of the input over the root mean-squared value of the quantization noise, according to

$$\text{SQNR} = \frac{\frac{V_{FS}}{2\sqrt{2}}}{\frac{1}{\sqrt{12}} q_s} = \frac{\sqrt{12}}{2\sqrt{2}} \frac{q_s 2^N}{q_s}, \tag{3.5a}$$

which in log-domain becomes

$$\text{SQNR} = 6.02N + 1.76 \text{ dB}. \tag{3.5b}$$

3.2.1 Quantization Noise of a One Bit ADC

It is worth noting that assuming that the quantization error is uniformly distributed is only an approximation. The approximation becomes poor if the resolution is low, which is obvious if we go to one extreme and assume that we have a 1-bit ADC, i.e., a comparator. The transfer function of a comparator is strongly nonlinear, as seen from the example in Figure 3.2(a). In this example the input is within zero to one and the threshold of the comparator is 0.5. The comparator output will therefore be one for inputs larger than 0.5, and zero otherwise. The gain is therefore nonlinear, as seen from Figure 3.2(b). The gain is zero for inputs below 0.5 and gradually decreasing from two to one as the input increases from 0.5 to one. If, e.g., a sinusoid is applied to the comparator input the output will contain several tones, since the transfer function is nonlinear. This is illustrated by Figure 3.3(a), where you clearly see the tones generated by the nonlinearities of the comparator. Hence to say that the output resembles uniformly distributed noise is not a good approximation in the case of a 1-bit ADC. When increasing the resolution of the ADC the tones in the output will spread over the whole spectrum, as would be the case for a uniformly distributed quantization error. This is illustrated by Figure 3.3(b), which is the output spectrum for an 8-bit ADC. As the resolution increases the assumption of uniformly distributed quantization noise therefore becomes more accurate.

The question is now, how large resolution should the ADC have for the assumption of uniformly distributed quantization error to be good? This may be answered by deriving the quantization noise from high level ADC

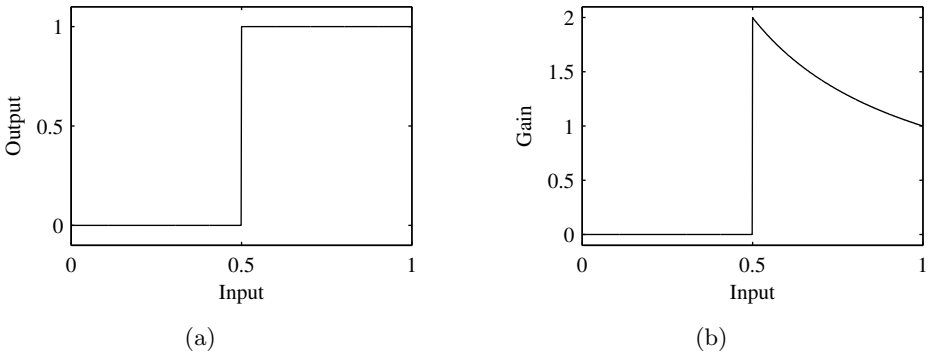


Figure 3.2: Example of (a) the transfer function of a 1-bit ADC, i.e., a comparator, and (b) its gain as a function of the input.

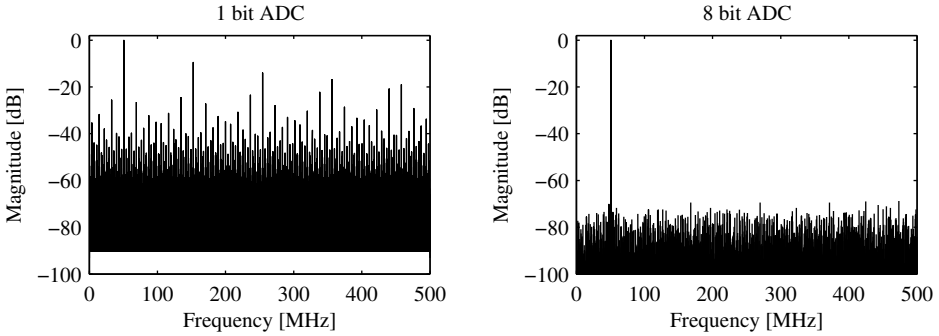


Figure 3.3: The output spectrum of (a) a 1-bit ADC and (b) an 8-bit ADC, for a 50.91 MHz sinusoid input at a sampling frequency of 1 GHz.

models of different resolution and compare each result with the expression derived in (3.4). That expression is derived by assuming a uniformly distributed quantization error. Consider a ramp input to the ADC. In Figure 3.4(a) the squared quantization error from the model of a 1-bit ADC is plotted over one quantization step, together with the mean-squared quantization error given by (3.4). Compare this expression to the squared quantization error of an 8-bit ADC, shown in Figure 3.4(b). Note that since the quantization step is given by (3.2) the absolute scale of the x-axes in Figure 3.4 are different. As can be seen from Figure 3.4 the mean-squared quantization error given by (3.4) is not a good approximation for low resolutions of the ADC. However, as the resolution increases the approximation is better, as seen from Figure 3.4(b). Since (3.4) is derived under the assumption that the quantization error is uniformly distributed this means that for low resolutions the error is not uniformly distributed, but as the resolution increases the assumption of uniformly distributed quantization error is better. To get some idea of how good the approximation of uniformly distributed quantization error is for different resolutions the relative error is calculated and plotted for different ADC resolutions. The relative error is given by

$$\text{Relative error} = \frac{\langle q_{\text{e}}^2 \rangle - \frac{1}{12} q_{\text{s}}^2}{\langle q_{\text{e}}^2 \rangle}, \tag{3.6}$$

and the result is plotted in Figure 3.5. As seen from this figure the approximation of uniformly distributed quantization error, and hence, quantization noise, seems to be good for resolutions above about ten bits.

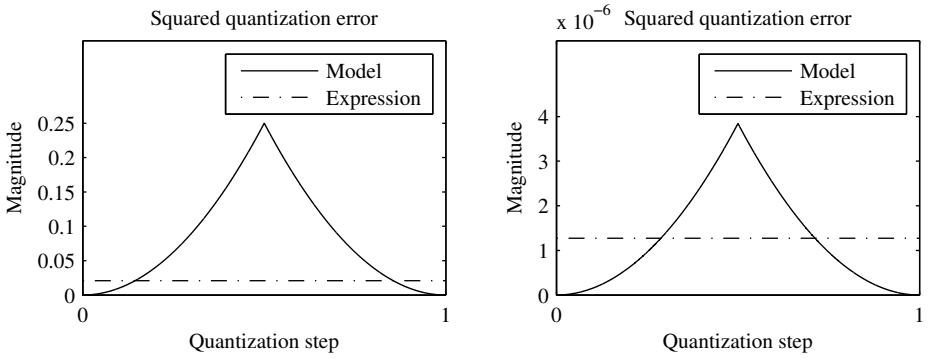


Figure 3.4: The squared quantization error for one quantization step of (a) a 1-bit ADC and (b) an 8-bit ADC, for a ramp input.

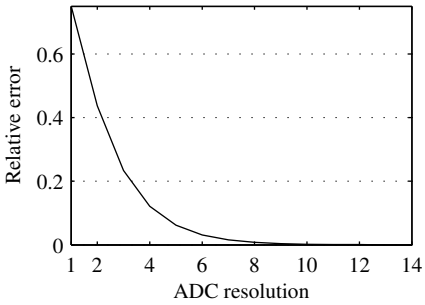


Figure 3.5: The relative quantization error as a function of the ADC resolution.

3.3 ADC Performance Measures

3.3.1 Resolution and Accuracy

As mentioned in Section 3.1, the resolution N of an ADC is the number of bits d_i in the digital output D_{out} of the converter. This is different from the accuracy of the converter. Instead, the accuracy reveals how much of the output that is significant after accounting all the non-ideal behavior and errors appearing during the conversion [35].

3.3.2 Input Bandwidth

The input bandwidth of an analog-to-digital converter is defined by the time constant given by the total input capacitance and the total input resistance. In a flash ADC the input capacitance is to a large extent determined by the parasitic input capacitances of the comparators, to which the input signal is applied. Reducing the parasitic capacitance of the comparators therefore yield a larger input bandwidth.

The interconnect of the input signal to the comparators also contribute to the total input capacitance, which can be reduced by using narrow on-chip wires. However, narrowing the wires increases the total input resistance of the converter, which counteracts the increase of the input bandwidth.

3.3.3 Differential and Integral Nonlinearity Error

The differential nonlinearity error (DNL) is the difference in quantization step from the ideal q_s, illustrated by Figure 3.6(a). Calculating the DNL as the difference between the transition points yields, in terms of LSB,

$$\mathrm{DNL}_d = \frac{V_{\mathrm{in},\,d+1} - V_{\mathrm{in},\,d} - q_\mathrm{s}}{q_\mathrm{s}}, \tag{3.7}$$

where $V_{\mathrm{in},\,d}$ is the input level for the code threshold between the digital output code d and $d+1$.

A missing code is a specific digital output that is never produced by the converter regardless of what the input is. A missing code yields a DNL of -1 LSB, which should never occur to obtain a desired resolution [35]. Hence $|\mathrm{DNL}_d| \leq 1$ LSB for all d should be fulfilled.

The integral nonlinearity error (INL) is the deviation of the output from an output of a corresponding converter with a linear transfer function [35]. The INL is measured as the difference between the transition point of the ideal converter, $V^i_{\mathrm{in},\,d}$, and the real converter, $V_{\mathrm{in},\,d}$, for each output code d, according to (3.8). The INL is illustrated by Figure 3.6(b).

$$\mathrm{INL}_d = \frac{V_{\mathrm{in},\,d} - V^i_{\mathrm{in},\,d}}{q_\mathrm{s}} \tag{3.8}$$

The INL can also be calculated from the DNL, according to (3.9).

$$\mathrm{INL}_d = \sum_{m=1}^{d} \mathrm{DNL}_m \tag{3.9}$$

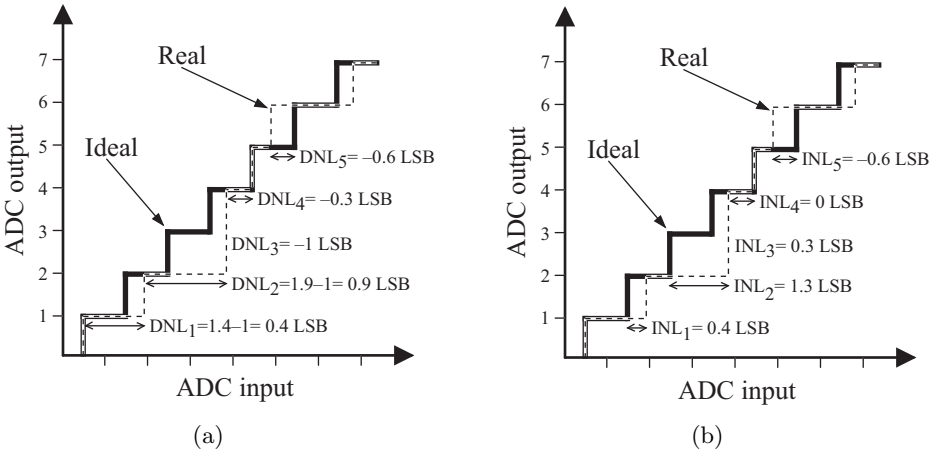


Figure 3.6: Illustration of (a) DNL and (b) INL.

The INL and DNL can be derived using histogram measurements of a repeated ramp input signal, or a sinusoidal input signal [8, 25, 110]. However, in this work the INL and DNL are calculated by applying a constant input to the ADC and gradually increase its value.

The remainder of this section presents and explains some different methods to derive the INL and DNL from measurements of a converter. The derivation of the INL and DNL using a ramp and sinusoidal input is explained, followed by the method used in this work.

Calculation of INL and DNL Using a Ramp Input

One way to measure the INL and DNL of a converter is to apply a ramp input signal or a sinusoid input and calculate a histogram of the output codes. Preferably the input signals should be repeated to get enough data to analyze. The information from the histogram of the output codes can then be used to calculate the INL and DNL [8, 25, 110]. The derivation of the INL and DNL using a ramp input is first explained.

During the measurements the data from several runs are collected using the same ramp input. The histogram of the collected data is then used to calculate the DNL and INL. For a ramp input signal it is straightforward to calculate the DNL. For an ideal ADC each code will occur the same number of times, i.e., they do all have the same code frequency f_{c0},

$$f_{c0} = \frac{M}{2^N}, \tag{3.10}$$

where M is the total number of collected data samples. Further, the size of each quantization interval for the ideal ADC, i.e., the code bin width Q, equals

$$Q = \frac{V_{FS}}{2^N}, \tag{3.11}$$

which using (3.10) becomes

$$Q = \frac{V_{FS} f_{c0}}{M}. \tag{3.12}$$

For the non-ideal ADC, which is measured, the code frequency f_i for each code i will most probably deviate from the ideal f_{c0}, and thereby also the code bin width Q_i from the ideal Q. Hence the code bin width Q_i can be calculated according to

$$Q_i = \frac{V_{FS} f_i}{M}, \tag{3.13}$$

that in units of LSB becomes

$$q_i = \frac{Q_i}{Q} = \frac{f_i}{f_{c0}}. \tag{3.14}$$

Calculation of INL and DNL Using a Sinusoid Input

When using a sinusoid input signal it is utilized that the probability density function, $f(y)$, of a sinusoid $y(t) = A \cdot \sin(\omega t) + B$ is given by [110]

$$f(y) = \frac{1}{\pi\sqrt{A^2 - (y - B)^2}}. \tag{3.15}$$

The transition levels are normalized by setting A equal to one. The transition levels $T[k]$ can be estimated by using (3.15) according to [25, 110]

$$T[k] = B - A\cos\left(\frac{\pi \cdot \sum_{i=0}^{k-1} h[i]}{\sum_{i=0}^{2^N-1} h[i]}\right), \tag{3.16}$$

where $h[i]$ is the number of samples in code bin i of the histogram of the output codes.

The transition levels are used to estimate the gain G and offset V_{os} of the ADC. The estimation is done by minimizing the squared residual error $\epsilon[k]$, i.e., the deviation from the ideal transfer curve, given by

$$\epsilon[k] = -G \cdot T[k] - V_{\text{os}} + (k-1) \cdot Q + T[1], \tag{3.17}$$

where Q is the average code bin width given by

$$Q = \frac{T[2^N - 1] - T[1]}{2^N - 2}. \tag{3.18}$$

The squared error becomes

$$E = \sum_{k=1}^{2^N-1} \epsilon[k]^2 = \sum_{k=1}^{2^N-1} \Big(-G \cdot T[k] - V_{\text{os}} + (k-1) \cdot Q + T[1]\Big)^2. \tag{3.19}$$

The error is then minimized by setting the partial derivatives with respect to the fit parameters, G and V_{os}, to zero.

$$0 = \frac{\partial E}{\partial G} = -2 \sum_{k=1}^{2^N-1} \Big(-G \cdot T[k] - V_{\text{os}} + (k-1)Q + T[1]\Big) \cdot T[k] \tag{3.20a}$$

$$0 = \frac{\partial E}{\partial V_{\text{os}}} = -2 \sum_{k=1}^{2^N-1} \Big(-G \cdot T[k] - V_{\text{os}} + (k-1)Q + T[1]\Big) \tag{3.20b}$$

By solving the system of equations above the gain G and offset V_{os} of the ADC can be calculated.

When the gain and offset is estimated the residual error $\epsilon[k]$ can be calculated. The derived G, V_{os}, and $\epsilon[k]$ is then used to calculate the DNL and INL according to the equations below [8], where the DNL and INL are defined in units of LSB.

$$DNL[k] = \big(G \cdot (T[k+1] - T[k]) - Q\big) \cdot 2^{(N-1)} \tag{3.21a}$$

$$DNL = \max\{|DNL[k]|\} \tag{3.21b}$$

$$INL[k] = \epsilon[k] \cdot 2^{(N-1)} \tag{3.21c}$$

$$INL = \max\{|INL[k]|\} \tag{3.21d}$$

INL and DNL Derivation in This Work

The method used in this work to extract the INL and DNL is somewhat similar to the first method. To minimize the dynamic effects on the static performance the sampling frequency is chosen very low, only 7 MHz. A DC input is connected to the converter input and its DC level is gradually increased during the measurement, sweeping over the whole full-scale range of the ADC. For each DC input level the logic analyzer collected and saved

the converter output, containing about 1400 samples from the ADC for each input level.

After the measurement the collected data is analyzed in MATLAB. First the data from each input level is averaged. Hence, for each input level the corresponding average ADC output level is calculated. In this work we chose to do a least-squares curve fit to the data. Hence we assume that the ADC is calibrated with respect to offset and gain errors. Other methods also exist, e.g. where the offset and gain errors are included in the curve fit. The data is also interpolated to yield approximate values between the measured data points, used by the MATLAB program when calculating the INL and DNL. The estimated least-squares curve fit and the interpolated data are used to calculate the input level for each transition level. The transition level is the level in the middle between two neighboring output levels.

The DNL is calculated by taking the difference between the input levels of two neighboring transition levels of the interpolated data. This is done for each input level, which is used to plot the DNL for each output code.

The INL is instead calculated by the difference of the input level of the interpolated data and the least-squares curve fit. This is repeated for each input level, which yield the complete INL of the converter, and is plotted for each output code.

3.3.4 Offset and Gain Error

The offset error V_{offset} of a converter, illustrated by Figure 3.7, is the average of all the errors in the converter [42]. Each error is the difference between the ideal analog input $V^i_{\text{in},\,d}$ at the ideal threshold point and the actual analog input $V_{\text{in},\,d}$ at which the threshold really is. In Figure 3.7 the best fit of the ideal ADC transfer function is plotted together with the best fit of the real measured ADC transfer function.

$$V_{\text{offset}} = \frac{1}{2^N} \cdot \sum_{d=0}^{2^N-1} \left(V^i_{\text{in},\,d} - V_{\text{in},\,d} \right) \tag{3.22}$$

The offset error can be calculated from the INL by observing that

$$\text{INL}_d \cdot q_{\text{s}} = V^i_{\text{in},\,d} - V_{\text{in},\,d}, \tag{3.23}$$

which yield

$$V_{\text{offset}} = \frac{q_{\text{s}}}{2^N} \cdot \sum_{d=0}^{2^N-1} \text{INL}_d. \tag{3.24}$$

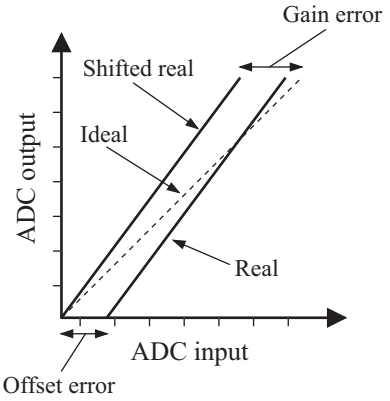


Figure 3.7: Illustration of the offset and gain error of an ADC.

The gain error of a converter, as illustrated by Figure 3.7, can be both linear and non-linear. If the converter has non-linear gain error the output is distorted. This is not the case for a linear gain error as long as it does not result in clipping of the output. A converter with linear gain and offset error has a digital output

$$V_{\text{out}} = G \cdot V_{\text{in}}^{i} + V_{\text{offset}}. \tag{3.25}$$

The linear gain G and the offset V_{offset} can be calculated using the least squares method [42]

$$G = \frac{\langle V_{\text{in},\,d} \cdot V_{\text{in},\,d}^{i} \rangle - \langle V_{\text{in},\,d} \rangle \cdot \langle V_{\text{in},\,d}^{i} \rangle}{\langle (V^{i}{}_{\text{in},\,d})^2 \rangle \cdot \langle V_{\text{in},\,d}^{i} \rangle^2} \tag{3.26a}$$

$$V_{\text{offset}} = \langle V_{\text{in},\,d} \rangle - G \cdot \langle V_{\text{in},\,d}^{i} \rangle, \tag{3.26b}$$

where $\langle . \rangle$ is the mean value.

3.3.5 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio of the power of the fundamental tone to the total noise power [42, 51, 108]. The total noise power is calculated by integrating the noise over the frequency band from DC up to the Nyquist frequency, i.e., half the sampling frequency f_{s}. In the integration the DC and harmonics components are excluded [40]. The SNR is often measured in decibel and is given by

$$\text{SNR} = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{noise}}} \right) \text{ dB}. \tag{3.27}$$

Assuming an ideal system without noise, the SNR is equal to the SQNR, given by (3.5b). Hence the SQNR is the maximum achievable SNR for an N-bit ADC.

3.3.6 Signal-to-Noise and Distortion Ratio

The signal-to-noise and distortion ratio (SNDR) is the ratio of the signal power to the total noise and distortion power, i.e., the SNR plus harmonics. As for the SNR, the SNDR is also measured in the frequency band from DC to $f_s/2$, excluding the DC component [40]. In log-domain it becomes

$$\mathrm{SNDR} = 10\log_{10}\left(\frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}} + P_{\mathrm{distortion}}}\right) \mathrm{dB}. \tag{3.28}$$

3.3.7 Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the difference between the amplitude of the desired output signal and the amplitude of the largest output tone that is not present in the input [40]. Measurements with the signal power instead of the amplitude yield that the SFDR is the ratio between the power of the desired output tone P_{signal} and the power of the largest output tone that is not present in the input, i.e., the power of the largest spurious tone $P_{\mathrm{spurious,max}}$. Hence the SFDR is given by (3.29) and is illustrated in Figure 3.8 where an output spectrum is plotted. As seen in Figure 3.8 the SFDR is calculated by taking the difference between the power of the fundamental tone and the largest spur. The SFDR of a converter may reveal some information about its INL performance, since a converter with a good INL generally yields an SFDR that is larger than the SNR of the converter [108].

$$\mathrm{SFDR} = 10\log_{10}\left(\frac{P_{\mathrm{signal}}}{P_{\mathrm{spurious,max}}}\right) \mathrm{dB} \tag{3.29}$$

3.3.8 Effective Number of Bits

The effective number of bits (ENOB) is the SNDR scaled according to (3.30), i.e., the ENOB contains the same information as the SNDR. By rearranging (3.5b) the ENOB is calculated as

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02}, \tag{3.30}$$

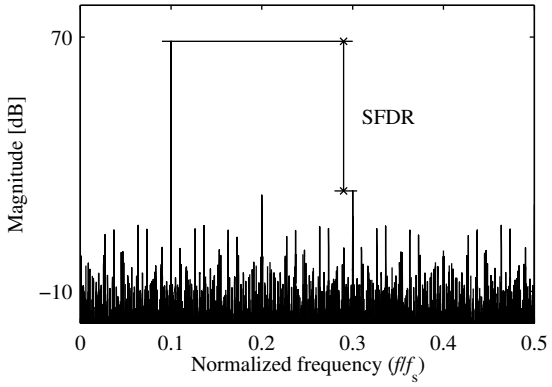


Figure 3.8: Illustration of SFDR.

which can be used to calculate the lower bound of the required ADC resolution for a specified SNDR.

The ENOB can also be calculated by fitting a fixed frequency sine wave in MATLAB to the sampled output data of the ADC [36, 47, 54]. The sinusoid to fit to the output data is

$$\tilde{y}_n = A\cos(\omega t_n) + B\sin(\omega t_n) + C, \tag{3.31}$$

where ω is the input angular frequency, t_n is the sample times, and A, B, and C are the fit parameters. The squared error Ψ between the output samples y_n and the sinusoid to fit, $\tilde{y}_n$, is

$$\Psi = \sum_{n=1}^{M}(y_n - \tilde{y}_n)^2 = \sum_{n=1}^{M}\left(y_n - A\cos(\omega t_n) - B\sin(\omega t_n) - C\right)^2, \tag{3.32}$$

where M is the number of output samples. The squared error given by (3.32) is then minimized by setting the partial derivatives with respect to the fit parameters A, B, and C to zero. This operation yields a linear equation system that is solved using MATLAB, which gives the fit parameters. The ENOB is then given by expression (3.33) [54],

$$\text{ENOB} = N - \frac{1}{2}\log_2\left(\frac{12\Psi}{q_s M}\right). \tag{3.33}$$

3.3.9 SFDR-Bits

Sometimes not only the SNDR is scaled to get the equivalent number of bits, but also the SFDR. By dividing the SFDR by 6.02 you get the SFDR-

bits [116], according to

$$\text{SFDR-bits} = \frac{\text{SFDR}}{6.02}. \tag{3.34}$$

3.3.10 Maximum Sampling Frequency

To find the maximum sampling frequency, $f_{\text{s,max}}$, a low frequency input is applied and the sampling frequency is swept. The maximum sampling frequency is reached when the SNDR is 3 dB lower than for low sampling frequencies. The 3 dB reduction of SNDR is equivalent to a 0.5 bit lower ENOB. Hence by plotting the ENOB as a function of the sampling frequency the maximum sampling frequency is obtained when the ENOB is 0.5 bit lower than for low sampling frequencies, as illustrated in Figure 3.9.

3.3.11 Effective Resolution Bandwidth

The effective resolution bandwidth (ERBW) is defined as the input frequency at which the ENOB is reduced by 0.5 bit compared with the ENOB at low input frequencies. Hence, by sweeping the input frequency instead of the sampling frequency the ERBW can be derived by the same method as for the maximum sampling frequency, as illustrated by Figure 3.10. In addition, it is measured at, or near, the maximum sampling frequency $f_{\text{s,max}}$.

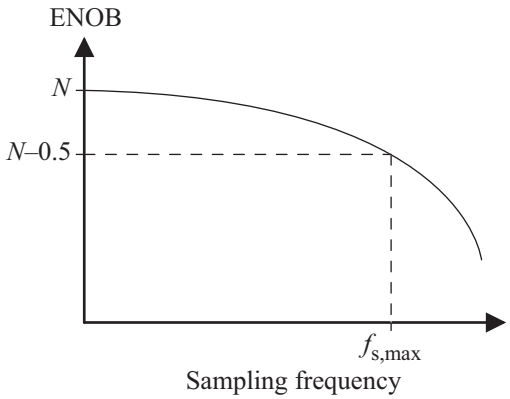


Figure 3.9: Illustration of how to derive the maximum sampling frequency.

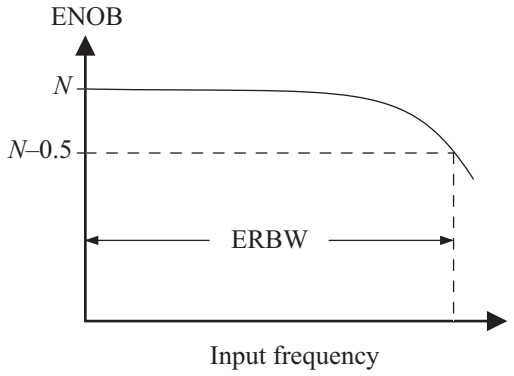


Figure 3.10: Illustration of the effective resolution bandwidth.

3.3.12 Figure of Merit

To compare the efficiency of different ADC designs a figure of merit (FoM) is required. The figure of merit can be defined in several ways [37, 81, 116]. In this work the FoM considers the power consumption of the converter, as well as the ENOB, the sampling frequency f_s, and the input frequency f_{in}, according to

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot \sqrt{f_{in} \cdot f_s}} \text{ J}, \tag{3.35}$$

which yields the energy per conversion step.

Another often used performance measure for ADCs is the product of the effective number of reference levels times the sample rate, $2^{\text{ENOB}} \cdot f_s$ [116, 117]. It is however not used in this work.

3.4 Flash ADC Topology

High speed ADCs are often based on a flash structure [52, 104, 108]. In an N-bit flash ADC, the input signal is applied to the inputs of $2^N - 1$ comparators, where N is the resolution of the converter. Each comparator is connected to a reference voltage that commonly is generated by a resistor net. The generation of the reference voltages is described in more detail in Section 3.4.1.

The output of a comparator is high if the input voltage is larger than the reference voltage at the reference input of the comparator. Otherwise the output is low. Hence the output pattern of the comparators corresponds to thermometer code. The comparators can be implemented in several different

ways, which will be discussed further in Section 3.4.2 where the comparator topology used in this work is presented.

In Figure 3.11 the thermometer code is decoded to the binary output code by the $(2^N - 1)$-to-N decoder, i.e., the thermometer-to-binary decoder. More details on the thermometer-to-binary decoder are found in Section 3.4.3. The comparators in Figure 3.11 are numbered, and the number corresponds to the thermometer output position m later used in Section 3.4.3.

3.4.1 Reference Generator

The reference generator used in flash ADCs usually consists of one or two strings of resistors [42]. Two strings are required when differential comparators are used. In this design the input signal is single ended, hence only one string of resistors is used, as illustrated by Figure 3.11. The behavioral level modeling of the reference generator is presented in Section 5.2. The results of the modeling are used for the design of the reference generator for the flash ADC with MUX-based decoder in Section 6.3.1 and the reference generator for the DEM flash ADC in Section 6.4.1.

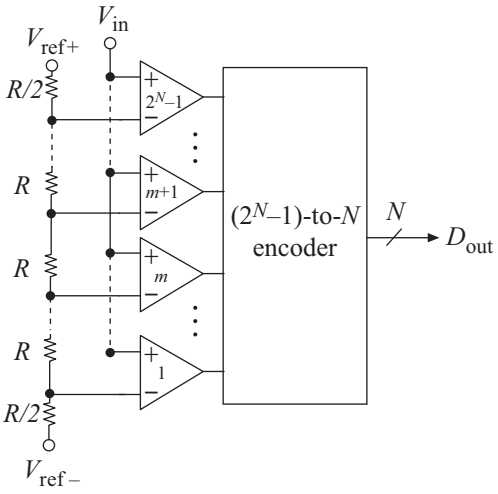


Figure 3.11: Illustration of a flash ADC.

3.4.2 Comparator

The comparators compare two signals on their inputs. Since the ADC input is single ended, the comparators do only have two inputs, i.e., the positive signal input and the negative reference input. If the input signal is larger than the reference signal the output should be logic one. In Figure 3.12 an illustration of the comparator used in this work is shown. As seen the comparator has a differential output, i.e., each comparator has two outputs. These outputs are connected to D flip-flops that holds the outputs for a clock period, which gives the thermometer-to-binary decoder enough time to convert the outputs of the comparators to the binary output of the ADC. In this work, only the D flip-flops connected to the positive output of the comparators serve as input to the decoder. The purpose of the D flip-flops connected to the negative comparator outputs is to load the two comparator outputs the same.

There are numerous different comparator topologies. For low requirements on resolution and speed, an operational amplifier can be used as the comparator [51]. For high-resolution applications the voltage corresponding to an LSB (V_{LSB}) is small. The gain of the comparator then has to be high to be able to amplify an input voltage of magnitude V_{LSB} to an output voltage that can be interpreted as a logic one or zero. If in addition the requirement on the conversion rate of the ADC is high, the comparator has to detect whether the difference between its inputs is positive or negative within a short time period. This implies that the bandwidth of the comparator must be high.

The requirements on high gain and high bandwidth of the comparators generally require the use of comparators based on cascaded amplifiers [51], as illustrated in Figure 3.13(a). At very high speed, the fast latched comparator topology is most commonly used [42, 108]. It is often combined with a number of cascaded preamplifiers as illustrated in Figure 3.13(b) [51]. Another advantage of the latched based comparators is that they can operate at a low supply voltage [106], which is the case in this work where the used

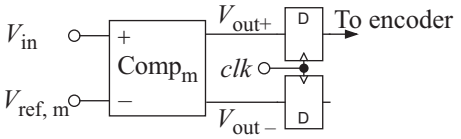


Figure 3.12: Block diagram of a comparator with D flip-flops on the outputs.

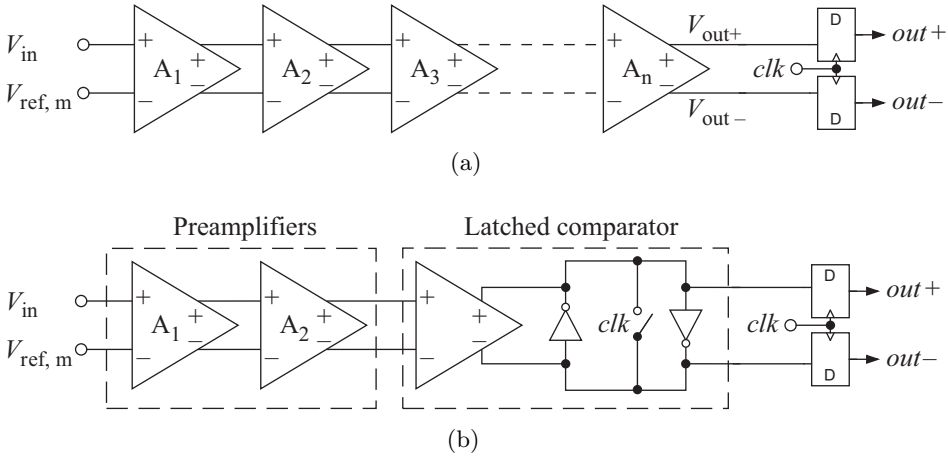


Figure 3.13: Illustration of (a) a cascaded amplifier based comparator and (b) a latch based comparator with cascaded preamplifiers.

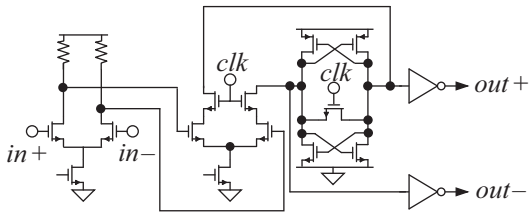


Figure 3.14: Illustration of the comparator circuit used in this work.

SOI CMOS technology limits the maximum supply voltage to 1.2 V.

In the target applications of this work the requirement on conversion speed is high, but the required resolution is only about six bits. The speed of the comparators is therefore more important than their accuracy. Consequently, a latched comparator with only one preamplifier is used in this work. The chosen comparator topology is shown in Figure 3.14. As seen in this figure the preamplifier has a passive load. If it instead employed an active load, it could be designed for a higher gain, which would improve the accuracy of the comparator. Since the speed of the comparator is more important than the accuracy in this work, the gain is however traded for speed by choosing a passive load instead of an active [106, 108].

3.4.3 Thermometer-to-Binary Decoder

As mentioned earlier the output pattern of the comparators corresponds to thermometer code. The thermometer code is generally decoded to binary code, but other output codes may also be used, such as gray code [81, 105, 106, 111]. There are also examples where the decoding is divided into two steps. First thermometer-to-gray decoding followed by gray-to-binary decoding, which can improve the bit error rate due to a reduction of an effect called bubble errors [17, 60, 82], explained below.

For low-resolution and low-speed converters the input to the decoder will indeed be a perfect thermometer code. However, as the resolution is increased the bubble error rate increases, especially if the sampling rate of the ADC is increased as well. The "bubbles" in the thermometer code are digital zeroes present in the string of ones, or digital ones present in the string of zeroes. The bubbles are mainly present near the transition level in the thermometer code [51]. They are caused by the uncertainty of the effective sampling instant due to, e.g., the global signal propagation over a long distance of the input signals and clock signals. The signal propagation over a long distance incurs a timing difference between the input signal lines and the clock lines. Hence, the clock and input signal paths should be closely matched by, e.g., using a buffer tree for the clock distribution. Other bubble error sources are the comparator metastability, the comparator offset, cross talk, noise, and limited preamplifier bandwidth [51, 52, 92, 99]. In the remainder of this section two different decoder topologies are presented, the read-only memory (ROM) decoder topology and the ones-counter decoder topology.

ROM Decoder

A common approach to decode the thermometer code is to use a gray or binary-encoded ROM. The appropriate row m in the gray encoded ROM is selected by using a row decoder that has the output of comparators m and $m+1$ as inputs. The output m of the row decoder, connected to memory row m, is high if the output of comparator m is high and the output of comparator $m+1$ is low. The row decoder can be realized by, e.g., a number of 2-input NAND gates, where one input to each NAND gate is inverted. However, this type of row decoder selects multiple rows if a bubble error occurs, which causes large errors in the output of the decoder [52, 104]. If only single bubble errors occur, these errors can be corrected by using 3-input NAND gates, as shown in Figure 3.15. The 3-input NAND gates

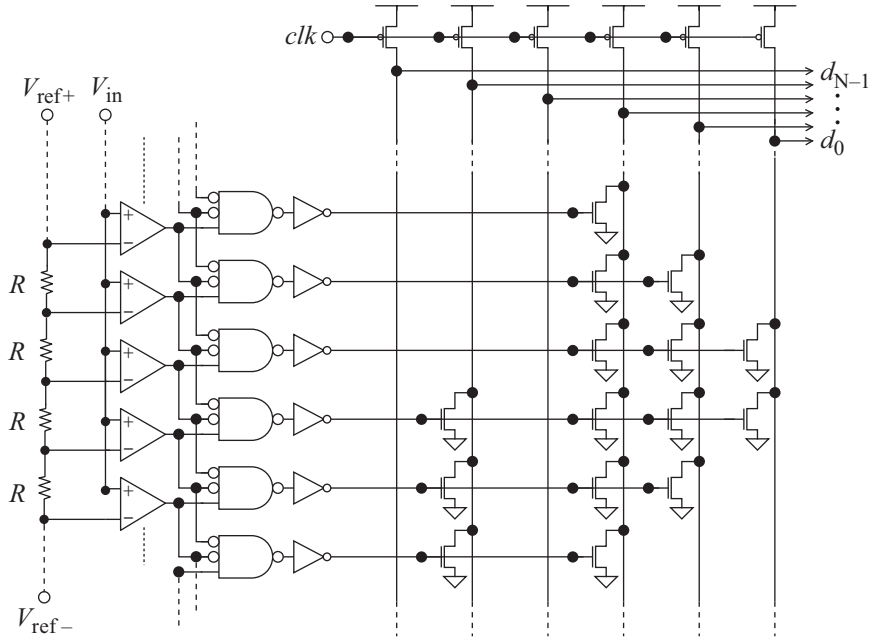


Figure 3.15: Illustration of a flash ADC with gray encoded ROM decoder.

remove all bubble errors if they are separated by at least three bits in the thermometer scale.

The main advantage of the ROM decoder approach is its regular structure that is straightforward to design. As the conversion speed increases a disadvantage is that more bubble errors occur and a more advanced bubble error correction scheme is generally required. As the complexity of the bubble error correction circuit increases, its propagation delay does in general also increase. The longer propagation delay reduces the speed of the overall decoder if not pipelining is applied. The increased complexity of the circuit increases the chip area, and it will likely consume more power [92, 99].

Ones-Counter Decoder

The numerical value of the output of a thermometer-to-binary decoder is the number of ones on the input, which could be represented in, e.g., gray or binary code. Hence a circuit counting the number of ones in the thermometer code, i.e., a ones-counter, can be used as the decoder [95]. The use of a ones-counter yields global bubble error suppression [52, 95, 99]. Another benefit of the approach is that a suitable ones-counter topology may

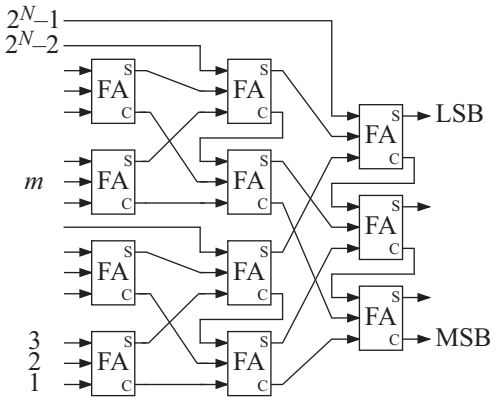


Figure 3.16: Wallace tree decoder for an N-bit flash ADC where $N = 4$.

be selected by trading speed and power. From this trade-off the Wallace tree topology [118], illustrated in Figure 3.16, is one good candidate as an decoder for high-speed converters [52, 73, 99].

3.5 Error Sources and Error Correction in Flash ADCs

As mentioned earlier the input signal of the flash ADC is connected to the inputs of $2^N - 1$ comparators, where N is the number of bits. Each comparator is also connected to a reference voltage, commonly generated by a resistor net. All these parts of the converter cause errors due to their non-ideal behavior due to, e.g., component mismatch. The errors caused by these parts are discussed in more detail in Section 3.5.2 and Section 3.5.3. The effects of sampling time uncertainty are presented first.

3.5.1 Sampling Time Uncertainty

Consider an input that is sampled by a sample-and-hold circuit. Due to clock jitter, the instant where the clock is changing is varying from clock cycle to clock cycle, i.e., it has a varying clock period. The exact sampling time instants are therefore unknown. The sampling time uncertainty, Δt_s, yields an uncertainty in the sampled value, ΔV_s, [108], as illustrated by Figure 3.17. If ΔV_s is too large the ADC performance is significantly degraded. The maximum allowable sampling time uncertainty for a certain resolution N and maximum input frequency $f_{in,max}$ are derived below.

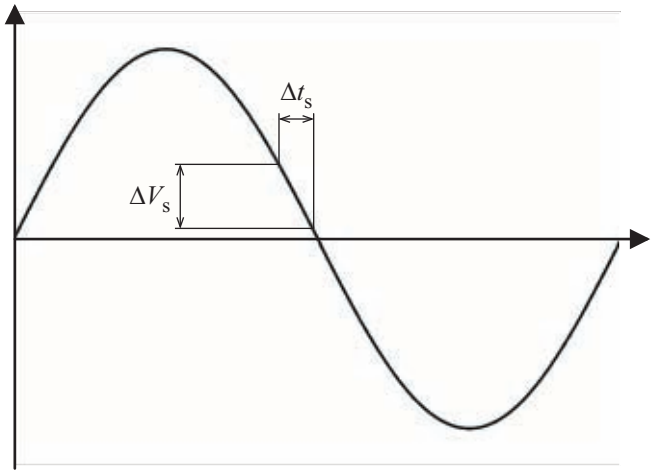


Figure 3.17: The uncertainty in the sampled value ΔV_s caused by the sampling time uncertainty Δt_s.

Consider a sinusoidal input with an amplitude equal to half the full-scale voltage V_{FS}, and a frequency equal to the maximum input frequency $f_{in,max}$,

$$V_{in} = \frac{V_{FS}}{2} \sin\left(2\pi f_{in,max} t\right). \tag{3.36}$$

The maximum rate of change for the input signal occurs at the zero crossing of V_{in}, i.e., where the derivative of (3.36) is largest. The uncertainty in the sampled value is therefore largest at the zero crossing, since deviations of the sampling time instant yield the largest deviation in the sampled value when the derivative has its maximum. The maximum ratio of ΔV_s to Δt_s can be approximated by the maximum derivative of the input according to

$$\max\left\{\left|\frac{\Delta V_s}{\Delta t_s}\right|\right\} \approx \max\left\{\left|\frac{dV_{in}}{dt}\right|\right\} = \pi f_{in,max} V_{FS}. \tag{3.37}$$

Requiring an uncertainty in the sampled value of less than 0.5 LSB, i.e., ΔV_s should be less than half the quantization step q_s, yields the relation in (3.38) for the maximum sampling time uncertainty by using (3.37) [108].

$$\Delta t_s < \frac{0.5 q_s}{\pi f_{in,max} V_{FS}} = \Big/ V_{FS} = q_s 2^N \Big/ = \frac{1}{\pi 2^{N+1} f_{in,max}} \tag{3.38}$$

In Table 3.1 the maximum sampling time uncertainty is listed for ADCs with resolutions of four, six, and eight bits. The maximum input frequency is assumed to be 500 MHz.

N	Δt_s
4 bits	20.0 ps
6 bits	5.0 ps
8 bits	1.2 ps

Table 3.1: Maximum sampling time uncertainty for different resolutions and an input frequency of 500 MHz.

3.5.2 Resistive Reference Generator

Due to mismatch, the resistance of the resistors in the reference net deviate from their nominal values by dR. The deviation can often be assumed to have a Gaussian distribution with zero mean and σ_R standard deviation, i.e.,

$$dR \sim \mathrm{N}(0, \sigma_R). \tag{3.39}$$

An effect of the resistor mismatch is that the reference levels also deviate from their nominal levels. The reference level deviation results in a nonlinear transfer function of the ADC, giving rise to harmonics in its output. These effects are included in the behavioral models of the ADCs implemented in this work. The models are presented in Chapter 5.

Another error source in flash ADCs is the signal feedthrough of the input signal to the reference generator outputs. The feedthrough occurs due to the parasitic capacitance between the inputs of the comparators. The effect of the feedthrough can be reduced by designing the reference net to have a sufficiently high bias current to obtain reference output voltages stable enough to reduce the harmonics to acceptable levels. Hence the total resistance of the reference net should be designed sufficiently low. However, if it is too low it consumes unnecessarily high power, i.e., there is a trade-off to make. More on the signal feedthrough is given in Section 5.2. In that section models are presented where the error sources above are included. In the models the voltage fluctuations of the reference generator power supplies are also modeled.

3.5.3 Comparator

The timing errors of an ADC mainly originate from four major timing error sources [108]. First we have the signal dependent delay, which is caused by the comparators. Second, the sampling clock jitter depends on the quality of the off-chip clock signal. The third source is the rise and fall times of the

on-chip clock signal. If these are too long, the noise from the clock buffers cause additional problems with clock jitter [108].

The last of the four error sources is the skew between the clock signal and the input signal. The skew originates from the routing of the signals over large distances on the chip. As an example, the distance from the bottom comparator to the top comparator of the converters implemented in this work is about 1 mm. Hence the timing difference between the clock signals of the bottom comparator compared to the top comparator is about 10 ps, assuming the on-chip signal propagation speed is about one third of the speed of light, and that the clock signal is routed from the bottom to the top of the comparator array. It is therefore important to carefully route the clock and input signal so that these signal paths are closely matched in terms of propagation delay.

Another method to reduce the effect of the signal dependent delay and the clock skew is by introducing a sample-and-hold circuit on the converter input. Ideally the output of the SH circuit is constant. Hence all comparators compare the same input independent on the exact sampling time of each comparator, i.e., the effect of clock skew between the comparators is reduced. Further, the signal dependent delay is reduced by increasing the ratio of the bandwidth to the input signal frequency of the preamplifiers in the comparators [108]. This ratio is maximized by applying a DC input signal, i.e., the SH output signal. Maximizing the ratio of the preamplifier bandwidth to the input signal frequency therefore minimizes the signal dependent delay. The drawback of this solution is that since the SH circuit has the total input parasitic capacitance of the comparators as load, which usually is large, the power consumption of the SH circuit will be high [70]. However, the results from MATLAB simulations of the model presented in Section 5.1 indicate that a clock skew of between 4 and 5 ps can be tolerated and still having an ENOB of 5.5 bit without using a SH circuit. This clock skew requirement can be tolerated, and the power consumption of the implemented ADCs in this work should hence be low. No SH circuit is therefore used for the ADCs implemented in this work. A study presented in [70] also shows that no SH circuit is required for flash ADCs with resolutions up to six bits. In that study they included restrictions on the maximum allowable differential nonlinearity, but allowed an ENOB degradation of one bit from the maximum.

The SH circuit reduces the effect of the signal dependent delay and the clock skew. Since no SH circuits are used in the converter designs in this work, the signal dependent delay increases the third order distortion on

the converter output. To reduce the signal dependent delay, and thereby the third order distortion, the preamplifiers must be designed to have a sufficiently high bandwidth [108], which is be explained in the distortion section below.

Distortion

As mentioned earlier the signal dependent delay of the preamplifiers of the comparators yields third order distortion on the converter output. The third order distortion of the converter can however be reduced by designing the preamplifiers of the comparators to have a sufficiently high bandwidth. An expression is derived in Section 5.5 of [108], which yield that the third order distortion D_3 is given by (3.40). The expression is used in Section 6.1, where the design of a comparator is presented. In (3.40) f_{amp} is the -3 dB bandwidth of the preamplifier and f_{in} is the input frequency of the ADC. The linear range of the preamplifier, V_{lr}, is the difference between the gate-source voltage V_{gs} of the input transistors and their threshold voltage V_{T}.

$$\mathrm{D}_3 = 20\log_{10}\left(\frac{2}{3\pi\frac{f_{\mathrm{amp}}}{f_{\mathrm{in}}}}e^{-\left(\frac{V_{\mathrm{lr}}}{V_{\mathrm{FS}}}\frac{f_{\mathrm{amp}}}{f_{\mathrm{in}}}-1\right)}\right) \tag{3.40}$$

Offset Error

The differential stage on the input of a comparator has one input connected to the reference input. The other input is connected to the single ended ADC input signal. Since the input stage of the comparator is differential, it is sensitive to mismatch between the two transistors to which the inputs are connected. The mismatch is due to the statistical variations during manufacturing and gives rise to the offset error of the comparator, as illustrated by the model in Figure 3.18. Careful layout of the input stage is therefore required to reduce the mismatch between the input transistors.

The input offset of the subsequent stages in the comparator, e.g., additional amplifiers or latches, also adds to the input offset of the comparator. The input offset of the comparator is however reduced by designing the first stages of the chain to have high gain. However, there is a trade-off with the -3 dB bandwidth of the preamplifier. The bandwidth should be as large as possible to reduce the signal dependent delay, and thereby the third order distortion of the converter. The gain of the preamplifiers is therefore generally limited to below 10 [42, 51].

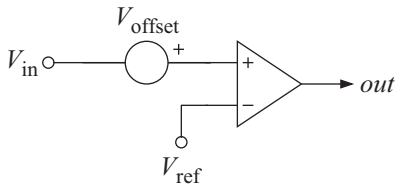


Figure 3.18: Model of the offset error of the differential input stage of a comparator.

Latched Comparator

This section presents methods to reduce the metastability errors and kick-back noise of latched comparators, illustrated by Figure 3.19. Consider a comparator based on cascaded amplifiers, as illustrated by Figure 3.13(a). If the output voltage level of a comparator is in between the logic one and logic zero levels the comparator is said to be in its metastable state [108]. Metastable states can happen if, e.g., the gain of the comparator is too low, or, equivalently, when the voltage difference between the inputs of the comparator is too low. The metastable states must be avoided, and hence the comparators must be designed accordingly.

The latched comparators often encountered in high-speed ADCs also suffer from metastability errors like comparators based on cascaded amplifiers.

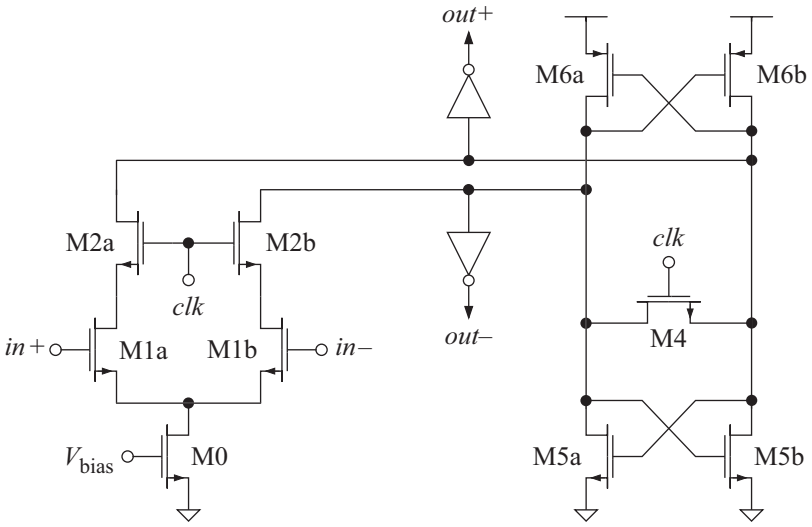


Figure 3.19: Schematic of a latched comparator.

By proper comparator design the metastability errors can be reduced. One alternative is to design the preamplifiers to have a high enough gain, which thereby reduces the metastability error rate [104], i.e., the same method used for the comparators based on cascaded amplifiers. However, the signal dependent delay is reduced by designing for a sufficiently high bandwidth. The requirement of a high bandwidth generally limits the possibility to design the preamplifier for a sufficiently high gain to have a lower metastability error rate. Instead we note that the latch used in a latched comparator can be considered as two negative gain amplifiers in a feedback loop. From this observation the expression in (3.41) can be derived. That expression gives the number of metastable states per second, M_{n}, as a function of the sampling frequency f_{s}, the unity gain frequency f_{T} of the negative gain amplifiers in the latch, and their DC gain A_0 [108],

$$M_{\mathrm{n}} = f_{\mathrm{s}} e^{-\left(1-\frac{1}{A_0}\right)\frac{f_{\mathrm{T}}}{f_{\mathrm{s}}}\pi}. \tag{3.41}$$

From (3.41) it is seen that the other ways to reduce the metastability error rate are to increase the ratio f_{T} over f_{s}, increase the DC gain A_0, or a combination of those methods.

A benefit of using fully depleted SOI CMOS technology compared with a bulk CMOS technology for the implementation of high-speed ADCs is found in expression (3.42) for the regeneration pole of the latch, p_{reg} [105],

$$p_{\mathrm{reg}} = \frac{g_{\mathrm{m}_5} + g_{\mathrm{m}_6}}{C_{\mathrm{gs}_5} + C_{\mathrm{gs}_6} + C_{\mathrm{db}_5} + C_{\mathrm{db}_6} + C_{\mathrm{db}_2}}. \tag{3.42}$$

The maximum sampling frequency of the latch is related to the regeneration pole p_{reg} of the latch. Hence (3.42) shows a benefit of using a fully depleted SOI CMOS technology compared with a bulk CMOS technology for the implementation of high-speed ADCs. As mentioned in Chapter 2 the body factor of fully depleted SOI CMOS is larger than for a bulk CMOS technology, which yields a higher current drive capability and therefore a higher g_{m}. Hence g_{m_5} and g_{m_6} is larger in a fully depleted SOI CMOS technology than in a bulk CMOS technology. In addition, the parasitic capacitances C_{db_5}, C_{db_6}, and C_{db_2} are smaller for SOI CMOS than for bulk CMOS, which further improves the speed. The latter performance advantage diminishes as the technology is scaled. For a partially depleted SOI CMOS technology the body factor is the same as bulk CMOS, and as the technology is scaled, the advantage of the reduced parasitic capacitances is reduced. There is therefore little advantage of using a partially depleted SOI CMOS technology over a bulk CMOS technology for the implementation of the flash ADC,

considering the speed of the latch. Since the technology used for the implementation of the converters in this work has a minimum channel length of 130 nm there should however still be an advantage in terms of reduced parasitic capacitance over bulk CMOS.

During the sample phase the outputs of the latched comparator are connected through the transistor switch M4 in Figure 3.19. The latch then enters its metastable state. To ensure that the outputs of the comparator are not in a metastable state during the sample phase the outputs are buffered by inverters sized to have a higher threshold voltage than the latch [104]. Hence the outputs of the comparator are at a high level during the sample phase. To reduce the metastable errors further, the comparator output buffers are connected to D flip-flops to further increase the regeneration gain of the comparator. Thereby the probability of having metastability errors is reduced [63].

The use of latched comparators results in another error, namely the kick-back noise. When the latch goes from the sample phase to the evaluation phase the comparator outputs change rapidly. These rapidly varying signals are fed through to the inputs of the comparator, i.e., the reference net and the converter input, as illustrated by Figure 3.20. Hence, the kick-back noise affects the input signal and brings noise to the reference net. The latter can however be somewhat reduced by further increasing the bias current in the reference net, which is the same approach that is used to reduce the input signal to reference net feedthrough.

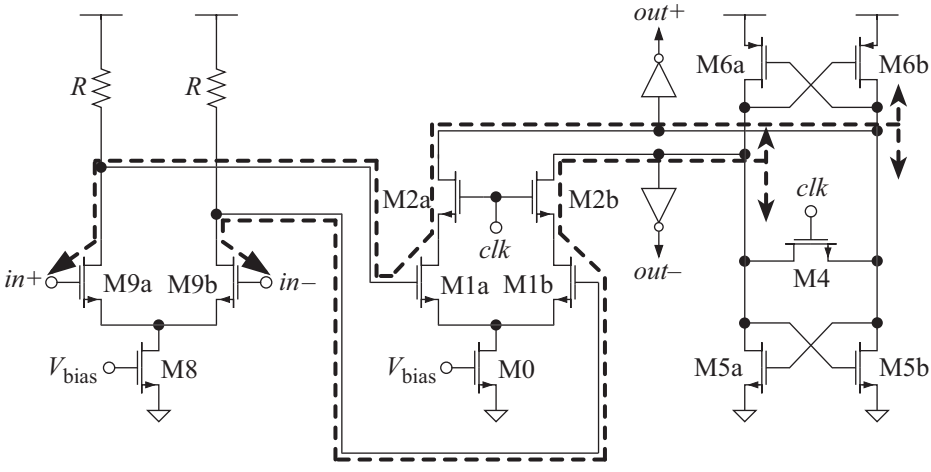


Figure 3.20: Feedthrough of the kick-back noise from the outputs to the inputs.

Different circuit architectural approaches can be applied to reduce the effect of the kick-back noise on the input and hence reduce its effect on the reference net [31, 106]. The approaches used in this work are to use a preamplifier and to introduce the NMOS transistors M2a and M2b in Figure 3.20. These transistors are connected to the clock signal. When the comparator is in its sample phase they are turned on. However, when the clock goes low and the comparator enters its evaluation phase, M2a and M2b are turned off. When they are turned off, they introduce a high impedance in the path from the comparator outputs to the comparator inputs for the kick-back noise. The increased impedance in the path reduces the kick-back noise on the inputs of the comparators.

3.6 DEM in Flash ADCs

Due to process variations, mismatch errors are introduced during the manufacturing of the circuits. To compensate for mismatch errors both static as well as dynamic matching techniques can be employed [90]. In static matching the components are placed close together in certain patterns and made sufficiently large to yield small relative errors, i.e., to reduce the variation between the components [26, 101]. A complementary approach is dynamic element matching (DEM), which has been used for a couple of decades in digital-to-analog converters (DACs) [108]. It has been used in stand alone DACs as well as DACs used in ADCs [6, 34, 44, 58]. In the past years some attempts have been made to introduce DEM in ADCs as well, such as pipelined ADCs [79], sigma-delta ADCs [34], and flash ADCs [11, 12, 89]. As with DACs, the introduction of DEM in ADCs improves the spectral properties of the converters [12, 89].

The dynamic element matching in the flash ADC is accomplished by introducing a number of switches between each adjacent resistor in the reference generator of the converter [11, 12], as illustrated in Figure 3.21, where the reference output with the lowest index has the lowest reference voltage. Hence the voltage on each output of the reference generator can be changed during operation by changing the state of the switches in the reference net. A specific comparator thereby compares different input levels in different sample instants. If the switches are connected to a random generator, which updates the reference voltages each sample, the spurious tones in the output caused by the uncertainties in resistor values and offset voltages of the comparators are reduced.

The drawback with the prior solutions in [11, 12] is that a large num-

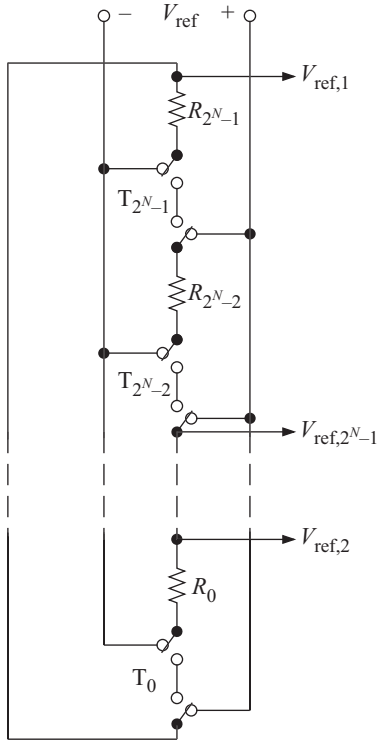


Figure 3.21: The reference generator of a flash ADC with DEM [12].

ber of switches are connected in series with the resistors in the reference generator. The on-resistance associated with the switches therefore adds to the total resistance of the reference generator. Hence the overall reference net resistance is increased, which increases the input signal to reference net feedthrough [94, 112], as shown in Section 5.2.1. The proposed DEM in [11, 12] therefore limit the maximum input frequency of the converter more than the proposal in this work, presented in Section 4.3. In addition, a large number of switches in the reference net causes large parasitic capacitances. Hence the settling time of the reference net is increased, which limit the conversion rate of the ADC.

To improve the speed of the ADC with DEM, a DEM circuit with less complexity is presented in Section 4.3 [90]. The circuit should be able to operate at higher frequencies compared with the circuits proposed in [11, 12]. The circuit is used in the ADC with DEM that is implemented in this work.

Chapter 4

Proposed Circuits

In this chapter the new circuits and approaches proposed in this work are presented. The first circuit is the folded Wallace tree decoder. This circuit uses an approach where the hardware cost and the propagation delay of a Wallace tree decoder are reduced by using the same Wallace tree for several intervals of the thermometer code [99]. In Section 4.2 a thermometer-to-binary decoder based on multiplexers is presented, i.e., the MUX-based decoder, a compact and fast decoder with low power consumption [92, 97]. This is followed by the proposed DEM flash ADC topology in Section 4.3 where the purpose of applying DEM is to improve the output spectral properties of the converter [90, 98].

4.1 Folded Wallace Tree Decoder

For a Wallace tree thermometer-to-binary decoder the size of the Wallace tree and the delay is depending on the number of added bits, i.e., the width of the base of the tree. To approximate the hardware cost, we note that a full adder (FA) may be built from three two-to-one (2:1) multiplexers (MUXs), according to Figure 4.1 [69]. Consider an N-bit flash ADC, where

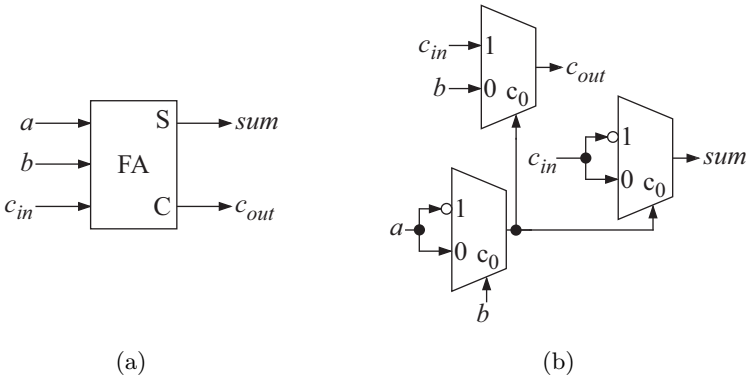


Figure 4.1: Illustration of (a) a full adder and (b) how it can be realized by three 2:1 MUXs.

the resolution N is larger than one. The hardware cost of its Wallace tree decoder, Γ_{Wallace}, in units of 2:1 MUX cost, Γ_{MUX}, is then approximated with [52, 99]

$$\Gamma_{\text{Wallace}} = 3\sum_{i=1}^{N}(i-1)2^{N-i}\Gamma_{\text{MUX}}. \tag{4.1}$$

The length of the critical path of the Wallace tree decoder expressed in units of the propagation delay of a 2:1 MUX, t_{MUX}, approximately becomes [52, 99]

$$t_{\text{CP,Wallace}} = (4N-6)t_{\text{MUX}}. \tag{4.2}$$

From the above rough cost estimates we note that the hardware cost and the propagation delay of the Wallace tree decoder decrease as the resolution N decreases, as expected. Now we split the thermometer code into several intervals where each interval is decoded by a Wallace tree decoder that is reduced in size compared with the original decoder. Each of the smaller Wallace tree decoders has a shorter critical path and lower hardware cost than the full decoder that decodes the whole thermometer code. If the same Wallace tree decoder are used for all intervals, achieved by introducing a multiplexer, the overall hardware cost would be reduced. This is the idea behind the folded Wallace tree decoder, shown in Figure 4.2 [99].

Using the folded Wallace tree decoder approach the thermometer code is split into 2^k different intervals. The different intervals of the thermometer code are multiplexed to a single Wallace tree decoder that is reduced in size compared with the original Wallace tree [99]. Its hardware cost and critical path is thereby reduced. The new costs can be calculated by exchanging N

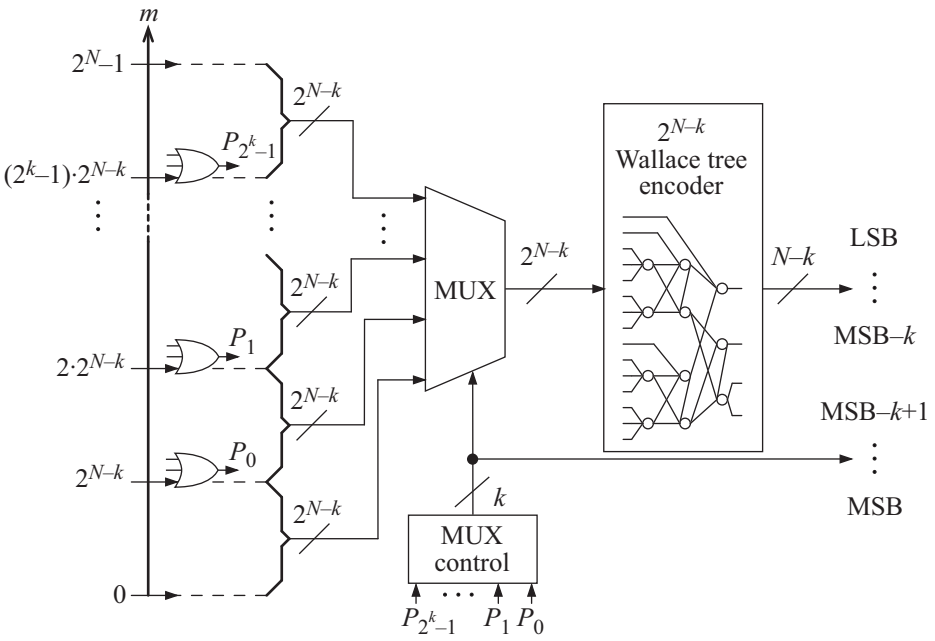


Figure 4.2: Illustration of the folded Wallace tree decoder.

with $N - k$ in (4.1) and (4.2) under the assumption that $N - k$ is larger than one. To derive the total hardware cost of the folded decoder and its propagation delay, the hardware cost and propagation delay of the MUX in front of the Wallace tree in Figure 4.2 must also be considered, and added to Γ_{Wallace} and $t_{\text{CP,Wallace}}$. The number of multiplexers required for the folded Wallace tree decoder is 2^{N-k}, where each MUX is of the type 2^k-to-1 (2^k:1) [99], which can be built up from $2^k - 1$ number of 2:1 MUXs. An example of how a 4:1 MUX can be realized from three 2:1 MUXs is shown in Figure 4.3. Inclusion of the MUX in the derivation of the hardware cost Γ_{folded} and the critical path $t_{\text{CP,folded}}$ of the folded Wallace tree decoder yields the following expressions for $N - k$ larger than one,

$$\Gamma_{\text{folded}} = \left(3 \sum_{i=1}^{N-k} \left((i-1)\, 2^{N-k-i} \right) + 2^{N-k} \left(2^k - 1 \right) \right) \Gamma_{\text{MUX}}, \tag{4.3a}$$

$$t_{\text{CP,folded}} = (4N - 3k - 6) t_{\text{MUX}}. \tag{4.3b}$$

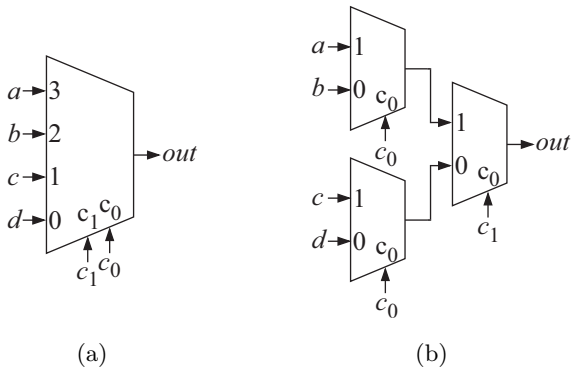


Figure 4.3: Illustration of (a) a 4:1 MUX and (b) an example of how it can be realized by three 2:1 MUXs.

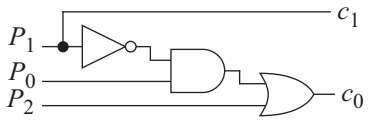


Figure 4.4: MUX control circuit for 4-level folding.

For a folding above four, i.e. $2^k > 4$, the MUX control circuit, depicted in Figure 4.4 for a 4-level folded decoder, will limit the critical path of the decoder [99]. A folding of four ($k = 2$) therefore seems to be a practical restriction. The hardware cost is however still reduced for folding above four. The decoder topology is evaluated by the behavioral level simulation presented in Section 5.4.

4.2 MUX-Based Decoder

Consider a 4-bit flash ADC with the thermometer output code to the left in Figure 4.5. The most significant bit (MSB) of the thermometer-to-binary decoder output is a logic one if more than half of the outputs in the thermometer scale are one. Hence the MSB is the same as the thermometer output at level 2^{N-1}, which is logic one in the example in Figure 4.5, i.e., $d_3 = 1$. To find the value of the second most significant bit, MSB $-$ 1, the original thermometer scale is divided into two partial thermometer scales, separated by the output at level 2^{N-1}. To find MSB $-$ 1 the appropriate partial thermometer scale must be decoded. If MSB equals one the upper

partial thermometer scale needs to be investigated, otherwise the lower partial thermometer scale is the one of interest. In the example in Figure 4.5 the upper scale is chosen. The MSB $-$ 1 is decoded in the same way as the MSB, i.e., by assigning it the value of the middle output in the selected partial thermometer scale. In this example the middle output is a logic zero, i.e., d_2 in Figure 4.5. This decomposition is continued according to Figure 4.5, until all output bits d_i are assigned the proper logic level. In the example in Figure 4.5, the binary output, D_{out}, becomes 1011_2, which equals 11_{10}, i.e., the number of ones in the decoder input.

The algorithm above can be realized by the MUX-based decoder in Figure 4.6 [92, 94]. As seen from Figure 4.6 the MSB (d_3) is generated from the thermometer output at position $m_0 = 2^{N-1}$. The position equals eight when N is four. The same output is also connected to the control inputs of the MUXs in the first decoder column. Hence if d_3 is one the upper part of the thermometer scale is chosen as the partial thermometer scale, otherwise the lower part of the scale is chosen. This is continued recursively until only one MUX remains. Its output is the LSB of the binary output of the decoder, i.e., d_0.

Due to the regular structure of the decoder, it can easily be expanded to operate in a system of higher resolution than four bits [94], which is explained below. The regular structure is also beneficial when doing the

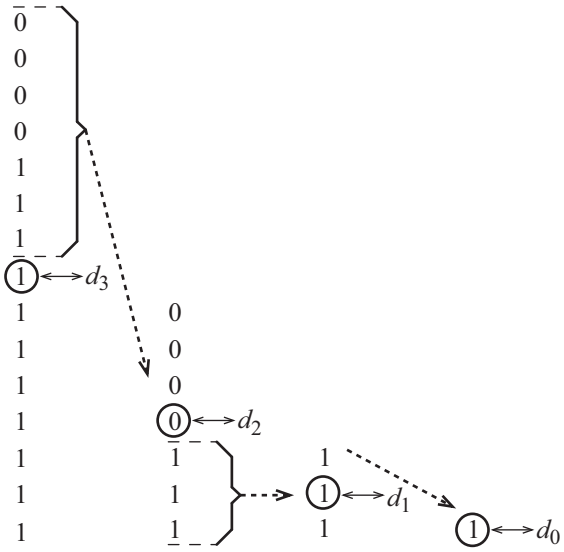


Figure 4.5: Example of the MUX-based decoder algorithm.

physical layout of the circuit [92, 97].

In general, the outputs d_i are the bits in the binary output, D_{out}, of the thermometer-to-binary decoder, where $i = 0, 1, \ldots, N-1$. Column one is the first MUX column, as shown in Figure 4.6. Further, the thermometer code outputs, i.e., the inputs to the decoder, and the MUX outputs in column i are denoted m_i for $i = 0$, and $i > 0$, respectively. For an N-bit flash ADC the thermometer output has $2^N - 1$ levels, i.e., $m_{i=0} = 0, 1, \ldots, 2^{N-i} - 1$. The thermometer outputs, $m_{i=0}$, or MUX outputs, $m_{i>0}$, are connected to the MUX at level m_i modulo 2^{N-i-1} and column $i+1$. If $m_i < 2^{N-i-1}$ they are connected to the "0" input of the MUX, or the "1"-input if $m_i > 2^{N-i-1}$. The remaining output $m_i = 2^{N-i-1}$ is connected to the control input of the MUXs in column $i+1$, and is the decoder output d_{N-i-1}. The decoder therefore has the hardware cost

$$\Gamma_{\text{MUX-decoder}} = \Gamma_{\text{MUX}} \sum_{i=1}^{N-1} \left(2^{N-i} - 1\right). \tag{4.4}$$

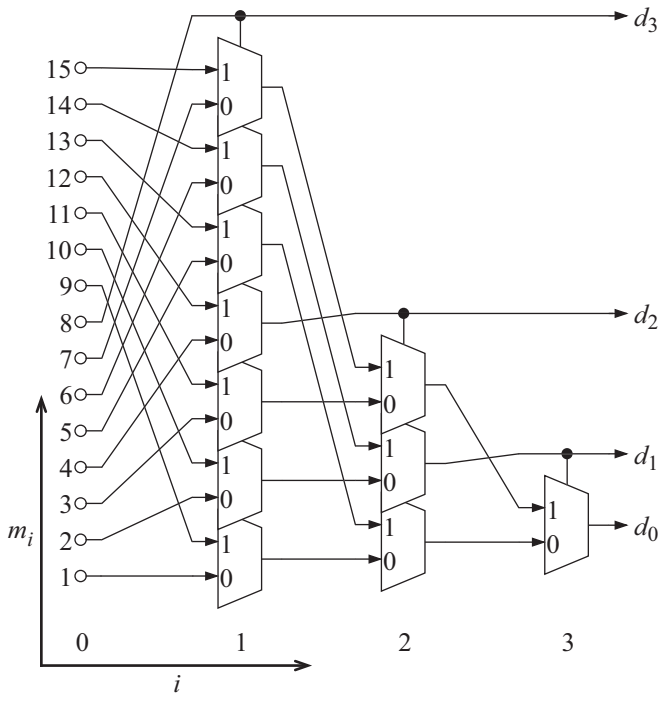


Figure 4.6: A MUX-based decoder for a 4-bit flash ADC.

Type of decoder	Hardware cost	Critical path
Wallace tree	171 Γ_{MUX}	18 t_{MUX}
4-level folded Wallace tree	81 Γ_{MUX}	12 t_{MUX}
MUX-based	57 Γ_{MUX}	5 t_{MUX}

Table 4.1: Hardware cost and length of the critical path of the Wallace tree decoder, the 4-level folded Wallace tree decoder, and the MUX-based decoder, for a 6-bit flash ADC.

The critical path $t_{\text{CP,MUX-decoder}}$ in units of t_{MUX} is

$$t_{\text{CP,MUX-decoder}} = (N-1)t_{\text{MUX}}. \tag{4.5}$$

A comparison of the hardware cost and the critical path is shown in Table 4.1 for a 6-bit flash ADC. The comparison shows that the hardware cost is significantly reduced if the 4-level folded Wallace tree decoder is used instead of the Wallace tree decoder. In addition, the propagation delay is shorter. Using the MUX-based decoder yield a significant reduction of the hardware cost and propagation delay compared with the other decoders [97].

4.3 DEM Flash ADC

In [12] DEM is introduced into the ADC by adding three switches at each reference level of the reference level generator, as illustrated in Figure 3.21. Two of the switches are connected to the reference generator supply and the third is connected between adjacent resistors. The reference generator therefore consists of several resistors and switches in series.

Since the resistance of the reference generator should be small enough to reduce the feedthrough of the input signal [94, 112], which will be further discussed in Section 5.2, the switches must be designed to have a low on-resistance. For a MOSFET switch, low on-resistance implies that it should be made wide. For example, in [104] the total reference net resistance, R_{tot}, of the single resistor string, given by

$$R_{\text{tot}} = R_{\text{u}}\left(2^N - 1\right), \tag{4.6}$$

is 120 Ω, where R_{u} is the unit resistance in the reference net, and the resolution N is six. To approximate the maximum on-resistance of the switches the resistance R_{u} is assumed to be zero, i.e., disregarding the reference net

resistors. This approximation yields for a resolution of six bits, i.e., 63 reference levels and 65 switches, that the maximum on-resistance of each switch should be less than 2 Ω. Such a low switch on-resistance is not feasible in practice, since it would require a very wide transistor, which would add excessive parasitic capacitance and consume excessive chip area. The parasitic capacitance of the switches increases the settling time of the reference net, which reduces the maximum operating speed of the ADC. The increased area may require a larger physical separation of the reference generator outputs, depending on the physical separation prior to the introduction of the switches. The physical separation of each output of the reference generator is set by the pitch of the comparators, which is minimized to reduce the clock and input signal skew [104]. The introduction of the switches therefore increases the clock and input signal skew, which is a reason to why the circuit in [12] is only usable for low speed applications, where a large R_{tot} can be tolerated.

The principle of the DEM proposed in [11] is the same as the one proposed in [12], but the resistors in the reference generator are replaced by the switch transistors. The switch transistors are charged by a fixed amount at each sample instant, which determines the on-resistance of the switch transistors. However, the circuit in [11] has the same disadvantage as the one proposed in [12], i.e., in high-speed applications the size of the switches would be too large. The circuit is also somewhat complex and contains ten transistors for each reference level, which adds a large parasitic capacitance at the reference generator outputs, thereby further reducing the speed of the circuit.

The proposed DEM reference circuit in this work aims at avoiding the switch connected between adjacent resistors [90]. This is accomplished by doubling the number of unit resistors and connecting them in a loop, demonstrated by Figure 4.7(a). The blocks denoted R are defined by Figure 4.7(b). By connecting $V_{\mathrm{ref+}}$ and $V_{\mathrm{ref-}}$, respectively, to different diagonally opposite pair of blocks R, the output voltages of the reference generator can be interchanged. Interchanging the reference outputs, e.g., every sample period, gives dynamic element matching of the resistors. In addition, a reference voltage is connected to the reference input of a comparator. Since the reference voltage changes every sample, the effect of the comparator offset on the transfer function is also reduced by the DEM.

To control what pair of blocks R to connect to $V_{\mathrm{ref+}}$ and $V_{\mathrm{ref-}}$, respectively, a DEM control unit is used. The unit controls the signals $c_{\mathrm{p},i}$ and $c_{\mathrm{n},i}$, that opens or closes the switches in the blocks R. Since only one pair of

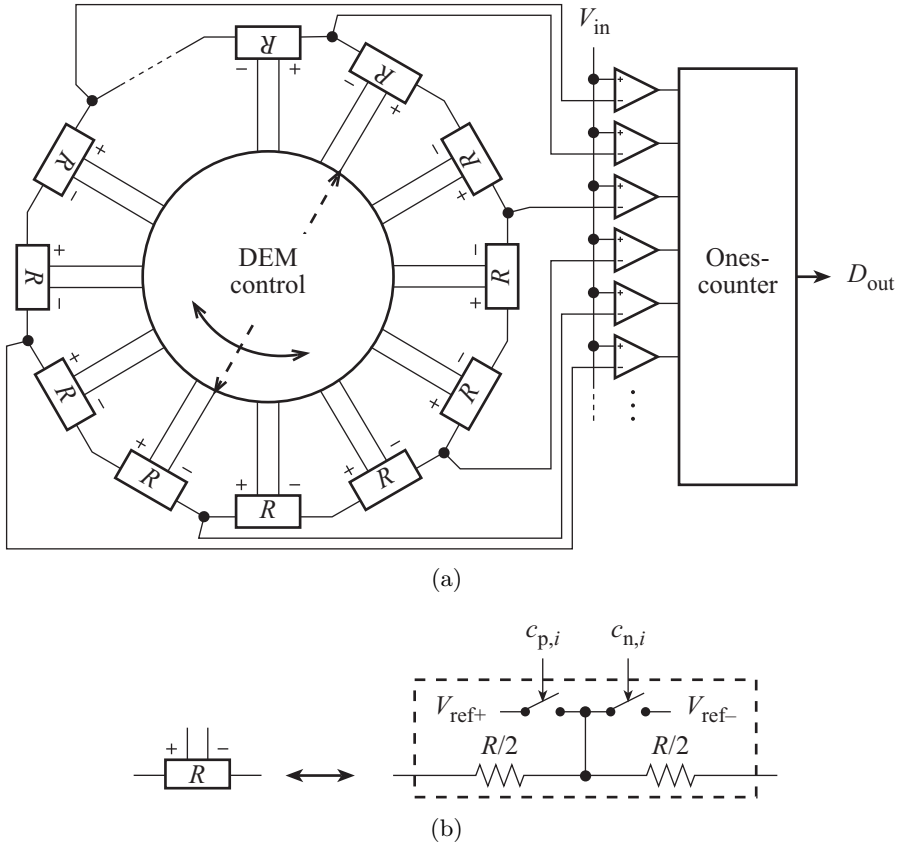


Figure 4.7: Illustration of (a) the DEM flash ADC, and (b) the block R.

diagonally opposite blocks R are connected to V_{ref+} and V_{ref-} at the same instant, there will only be two switches in series with the resistors between the reference supply V_{ref+} and V_{ref-} at any time. This scheme yields a significant reduction of the number of switches introduced into the reference net compared with the solutions in [11, 12]. The DEM circuit proposed in this work should thereby allow a higher maximum input frequency and a higher sampling frequency compared with the circuits in [11, 12]. The DEM flash ADC topology is described in more detail next.

In Figure 4.8(a) a block diagram of the DEM flash ADC is shown, displaying its different building blocks. In Figure 4.8(b), the circular structure of the resistor net can be seen for a special case of five quantization levels. Figure 4.8(b) also shows that the topology requires the double amount of unit resistors compared with a conventional flash ADC topology. Further,

the reference net supply V_{ref} is connected to one pair of nodes in the resistor net, dividing it into two strings of resistors with equal resistance.

The reference net supply is distributed to the resistor loop by the set of MOSFET switches displayed in Figure 4.8(b). Only one pair of switches is active at the same time. To ensure proper activation the switches are controlled by a 1-of-M decoder, where M is eight in this example, and $2^{N+1} - 2$ in the general case. The 1-of-8 decoder activates one pair of switches by setting one of its outputs to logic zero, keeping the others at logic one. The 1-of-8 decoder is controlled by a random generator. The random generator generates a random binary number that is decoded to a digital zero on one of the outputs of the 1-of-8 decoder. The position of the zero determines where $V_{\text{ref+}}$ and $V_{\text{ref-}}$ are connected on the circular resistor net, which determines the set of reference voltages. Hence the reference voltages are randomly interchanged each sample. The advantage of this solution compared with prior work is that the total resistance of the string of resistors, R_{tot}, can be chosen sufficiently low to meet the requirements on input signal feedthrough. A limitation is the series resistance of the two switches connected to the reference net.

A MATLAB model of the proposed DEM architecture has been developed and the ADC incorporating DEM has been implemented in a 130 nm partially depleted SOI CMOS technology. The results of the MATLAB simulations and the transistor-level circuit simulations are presented in Section 5.5 and Section 7.5.1, respectively. In Section 7.5.2 the measurement result are presented.

4.3.1 The 1-of-M Decoder

If the logic zero on one of the 1-of-M decoder outputs is allowed to change position to any of the M decoder outputs every sample, the reference voltages could change by as much as the full-scale voltage V_{FS} every sample. Such a large voltage fluctuation could limit the speed of the overall converter, since the reference voltages must settle before the output of the ADC can be used. To reduce the settling time only neighboring comparators should be allowed to interchange their reference voltages in high-speed applications. This reduces the reference voltage changes to one V_{LSB}, and therefore the settling time is also reduced [90]. In Section 5.5 the behavioral level simulation results show that restricting the interchange of reference voltage to neighboring comparators still reduces the spurious tones significantly compared with not using DEM.

The 1-of-M decoder in Figure 4.8 is designed with an M stage circular

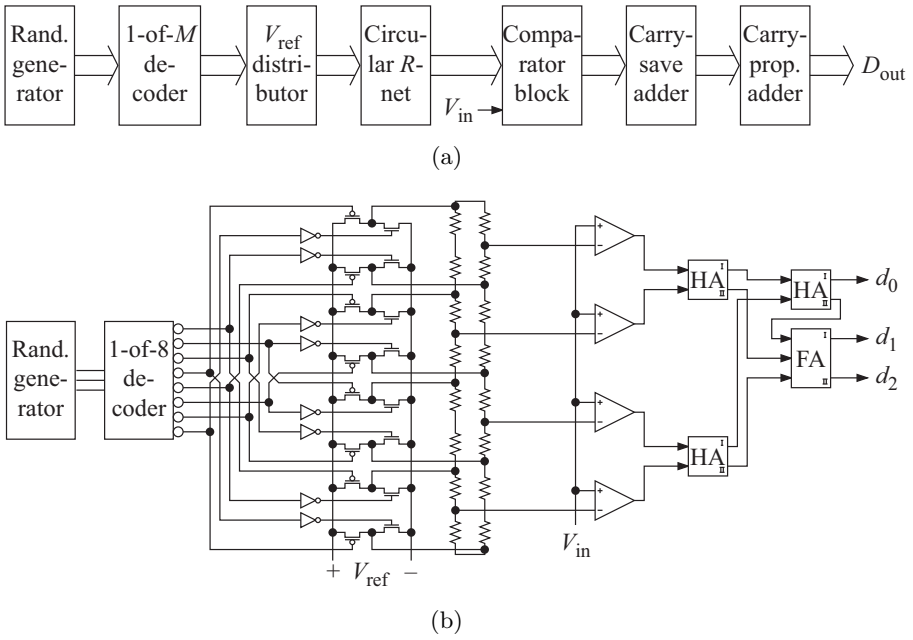


Figure 4.8: (a) The block diagram of the proposed DEM flash ADC and (b) an example of the schematic of the proposed DEM flash ADC for five quantization levels.

shift register capable of shifting one position in either direction. One of its stages is initiated to logic zero and the others to logic one. Hence one of the M outputs of the 1-of-M decoder will always be zero. The zero is shifted one position each clock cycle with a direction dependent on the output of the random generator.

4.3.2 The Thermometer-to-Binary Decoder

If a ROM decoder would be used with the suggested DEM circuit, a switch net has to be added between the comparators and the decoder to connect the comparator connected to the lowest reference voltage to the decoder input with the lowest weight, etc. A better approach is to use a ones-counter decoder [52, 90, 99]. The ones-counter decoder can be used since the number of ones in the thermometer code before the introduction of DEM is the same as after introducing DEM. They are only in a different order.

Chapter 5

Modeling of Flash ADCs

The behavioral model simulations of a system yield information and input to the design phase and circuit specification, e.g., for the comparators or the reference generator. The behavioral level models are gradually refined. In the end the design can be verified and fine-tuned by a few transistor level simulations [10, 23]. Hence the behavioral level models enable the top-down methodology, which is crucial for designing a large system.

5.1 Clock Skew

As mentioned in Section 3.5.3 the problems of the clock skew between different comparators can be alleviated by applying a sample-and-hold (SH) circuit on the input of the ADC. This will however increase the power consumption, since the SH circuit has to drive a large load capacitance and therefore will consume much power [70]. This section presents a behavioral

model of an ADC with clock skew. The model is illustrated by Figure 5.1 where the input is sampled at the nominal sample time instants t_n plus the sampling time uncertainty Δt_s. Each comparator is modeled individually according to Figure 5.1. The comparators will thereby have different sampling time uncertainties Δt_s, and hence there will be a clock skew between different comparators. The ADC model is used to compute the yield as a function of the standard deviation of the clock skew by simulation in MATLAB. The simulation result is then used to determine the need of a SH circuit.

When no SH circuit is present at the input, every comparator samples the input signal on inaccurate time instants due to the clock skew. This effect is modeled in MATLAB assuming a Gaussian distributed clock skew with zero mean value. The model is simulated in MATLAB with a 1 GHz 0.5 V full-scale sinusoid input and a sampling frequency of 2.1 GHz. The design target in this simulation is an ENOB larger than 5 bits.

The result of the MATLAB simulations is presented in Figure 5.2(a), where the yield is plotted as a function of the standard deviation of the clock skew, and in Figure 5.2(b), where the same plot is shown, but magnified. These simulation results show that the standard deviation of the clock skew can be slightly above 4 ps and still result in an ENOB larger than 5 bits. This requirement on clock skew is possible to achieve without a SH circuit on the input [70]. Hence since a low power consumption of the ADC is required a SH circuit is not used in the test ADCs in this work. Higher resolution or input frequency of the ADC would require a SH circuit on the input.

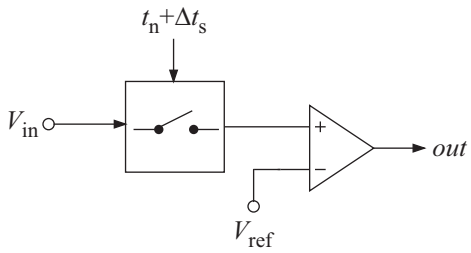


Figure 5.1: Model for the clock skew.

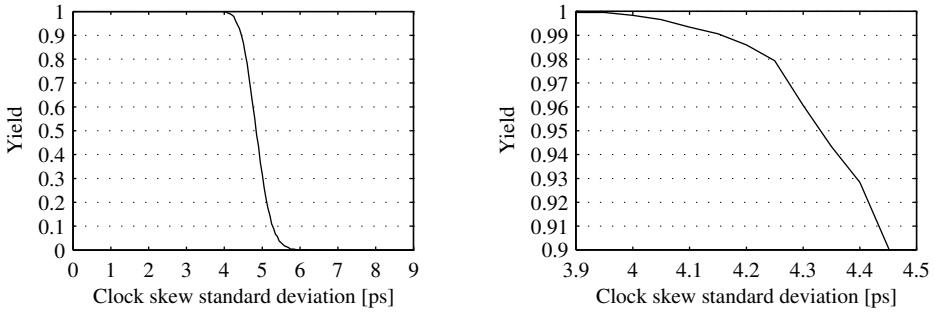


Figure 5.2: (a) The yield as a function of the clock skew where the targeted ENOB should be larger than 5 bits for the 6-bit ADC, and (b) a magnification of a part of the plot.

5.2 Reference Generator

Two of the major error sources related to the resistive reference generator are the input-to-reference signal feedthrough and the effect of mismatch between the resistors in the reference net. Another error source is the fluctuations of the reference net supply. These error sources are modeled prior to the circuit design of the test ADCs of this work. In Section 5.2.1 a model of the input-to-reference signal feedthrough is presented and a method to reduce the power consumption of the reference net is discussed. In Section 5.2.2 the effect of mismatch between the resistors in the reference net is modeled together with the effect of the reference net fluctuations.

5.2.1 Input-to-Reference Signal Feedthrough

There is a parasitic capacitance between the comparator inputs, $C_{\text{comp,in}}$, due to the parasitic capacitance between the gate and the source, C_{gs}, of the preamplifier input transistors. This is indicated in the input stage in Figure 5.3. In Figure 5.4 the reference net and comparators for a 2-bit flash ADC is shown. The parasitic capacitors between the inputs of the comparators are shown in this figure, which couple the input signal to the reference net. Hence the input is fed through to the resistive net generating the reference voltages.

The input-to-reference signal feedthrough causes a variation of the reference voltages. The reference voltage variation can be too large if the

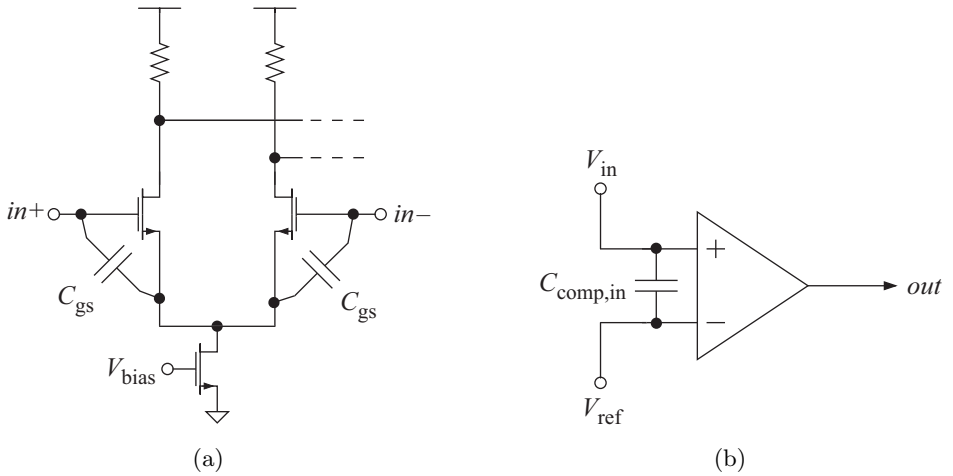


Figure 5.3: (a) The input stage of the comparator with the parasitic capacitors between the gate and the source indicated, and (b) the comparator including the parasitic capacitor between the inputs.

resistance of the resistors is not low enough. However, if the resistance is chosen too low the reference net consumes unnecessarily high power [112]. An expression for the maximum allowable total reference net resistance is derived below. The model, derived from Figure 5.4, of the resistor net is shown in Figure 5.5 for three comparators and the assumption that $V_{\text{ref}+}$ and $V_{\text{ref}-}$ are perfectly decoupled.

After expanding the model in Figure 5.5 to the general case of $2^N - 1$ comparators, R and C are given by

$$R = R_{\text{tot}}/(2^N - 1) \tag{5.1}$$

and

$$C = C_{\text{tot}}/2^N, \tag{5.2}$$

where R_{tot} is the total reference net resistance and C_{tot} is the total $C_{\text{comp,in}}$ on the ADC input. The ratio between each reference output and the input signal V_{in} is calculated using the symbolic solver in MATLAB. The resolution of the ADC is assumed to six bits in the derivation. From the results it is seen that the middle reference net output V_{mid} is affected the most by the input signal feedthrough. The same result is obtained in [112]. Under the assumption that $2\pi f_{\text{in}} RC \ll 1$ the following expression for R_{tot} is obtained

$$R_{\text{tot}} \leq 4.1 \frac{V_{\text{mid}}}{V_{\text{in}}} \frac{1}{\pi f_{\text{in}} C_{\text{tot}}}, \tag{5.3}$$

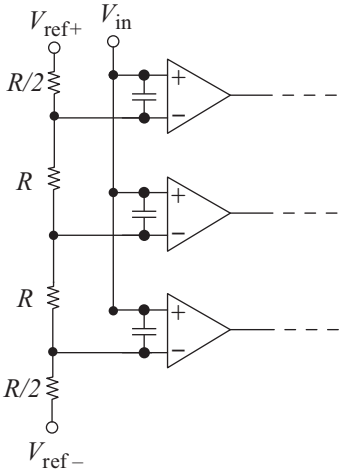


Figure 5.4: Reference net and capacitors with the parasitic capacitors between the comparator inputs included.

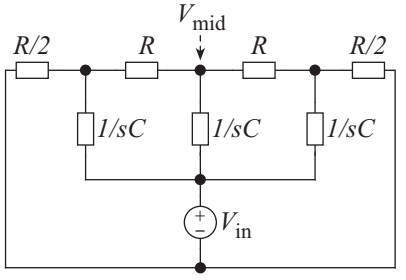


Figure 5.5: Model of the input-to-reference signal feedthrough for a resolution of two bits.

which also is validated by transistor level simulations in Cadence. To express (5.3) as a function of the feedthrough in number of LSBs the ratio of V_{mid} over V_{in} is assumed to be q_{LSB} number of LSBs, i.e.,

$$\frac{V_{\text{mid}}}{V_{\text{in}}} = \frac{q_{\text{LSB}}}{2^N}, \tag{5.4}$$

which yields the expression for the input-to-reference signal feedthrough,

$$R_{\text{tot}} \leq \frac{4.1 q_{\text{LSB}}}{\pi f_{\text{in}} C_{\text{tot}} 2^N}. \tag{5.5}$$

The expression in (5.5) is used in the design of the reference net, discussed

Section 6.3.1, after extracting the input capacitance of the comparators, which is discussed in Section 6.1.

Decoupling of the Reference Net Outputs

As mentioned above the expression in (5.5) can be used to calculate the maximum allowable total reference net resistance. For high-speed ADCs this resistance is generally low. Consider, e.g., a flash ADC with a resolution of six bits and a maximum input frequency, f_{in}, of 500 MHz. The input capacitance of each comparator in this work is 13 fF, which yields a total input capacitance C_{tot} of 0.83 pF. Requiring a maximum feedthrough lower than one LSB yields a maximum total reference net resistance of 50 Ω, which imply that each resistor in the reference net should be 0.8 Ω. Further, assuming a full-scale voltage of 1 V, i.e., the reference net supply V_{ref} is 1 V, yields a 20 mW power consumption of the reference net. To reduce this power consumption the total resistance of the reference net must be increased, but as discussed above this would yield a higher input-to-reference signal feedthrough. The question now is how the reference net can be modified so that the feedthrough is not increased when increasing the resistor values of the resistors in the reference net?

In the example above the resolution is six bits, i.e., the reference net has 63 outputs, as illustrated by Figure 5.6(a). Each of the outputs is connected to the reference input of a comparator. A model of the input-to-reference signal feedthrough of the 6-bit flash ADC is shown in Figure 5.6(b). Now assume decoupling by an on-chip capacitor at every fourth reference output. This distance is defined as the decoupling period p_{dec}, which is equal to four in this example. Also assume that the decoupling is perfect. The modified reference net can now be illustrated by Figure 5.7(a) and its input-to-reference signal feedthrough can be modeled by Figure 5.7(b). From Figure 5.7(b) it is seen that the effect of the decoupling is that the original reference net model in Figure 5.6(b) is divided into 16 parts, each similar to the model in Figure 5.5. The difference is that the edge resistors of the middle sub-nets have the value R instead of $R/2$, which is the case the previous model shown in Figure 5.5. By the decoupling the new worst-case feedthrough occur at the $V_{\text{mid},m}$ nodes, i.e., at the reference outputs m, where $m = 2, 6, \cdots, 62$ in this case. As a result of the decoupling the N in (5.5) is reduced from six to two, i.e., the reference net decoupling period p_{dec} is reduced from 64 to four. Hence N in (5.5) can be exchanged for $\log_2(p_{\text{dec}})$, or 2^N can be exchanged for the reference net decoupling period p_{dec}. The

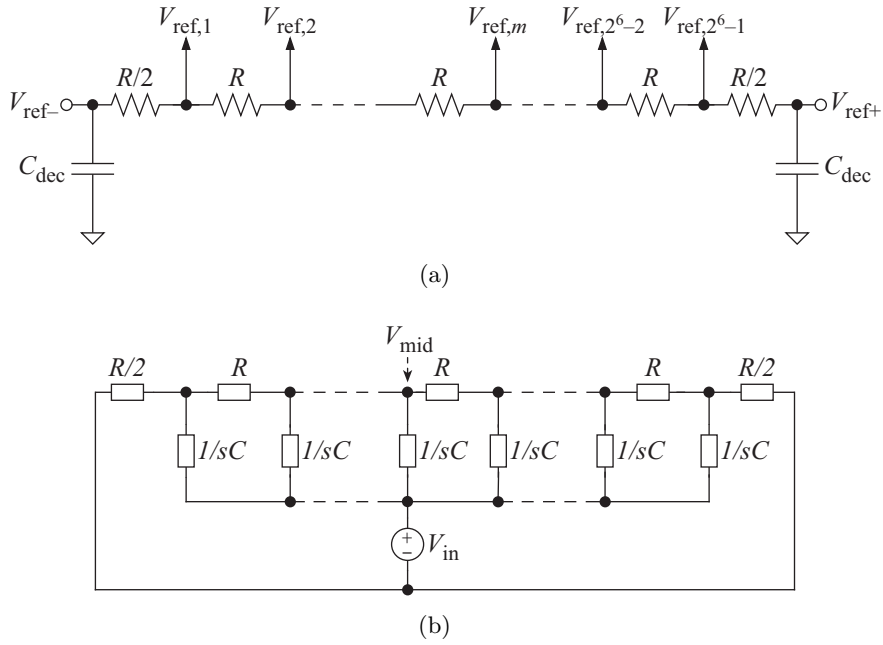


Figure 5.6: Illustration of (a) the reference net for a 6-bit flash ADC, and (b) the model of the input-to-reference signal feedthrough of the reference net in (a).

new expression for the input-to-reference feedthrough then becomes

$$R_{tot} \leq \frac{4.1 q_{LSB}}{\pi f_{in} C_{tot} p_{dec}}, \tag{5.6}$$

where $p_{dec} \leq 2^N$.

Using (5.6) for a p_{dec} of four yield that the maximum reference net resistance is increased to 790 Ω, which reduces the reference net power consumption to 1.3 mW. This power consumption is significantly lower than the original 20 mW. However, the reduction of power consumption comes with a cost since the decoupling capacitors require additional chip area.

5.2.2 Resistor Mismatch and Reference Net Supply Fluctuations

Due to mismatch, the resistance of the resistors in the reference net deviate from their nominal values. The reference levels thereby also deviate from their nominal levels. To investigate the effects of the mismatch a model is developed in MATLAB. In this model the deviation from the nominal

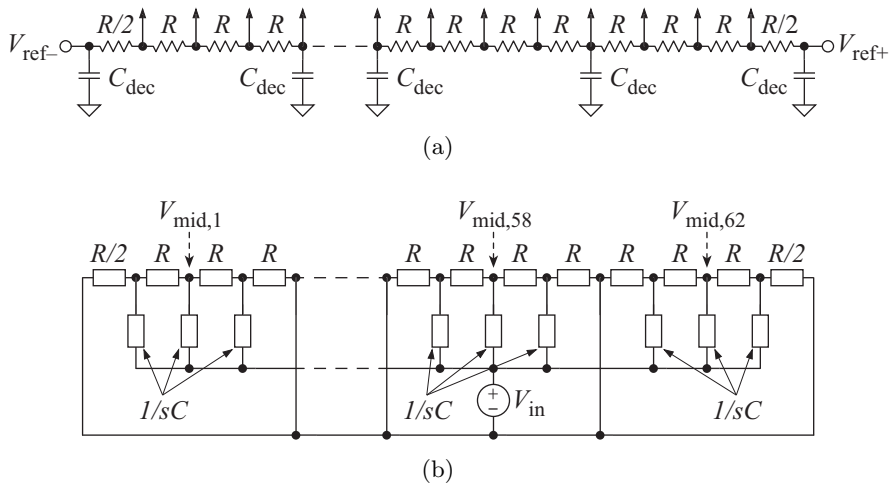


Figure 5.7: Illustration of (a) the decoupled reference net for a 6-bit flash ADC, and (b) the model of the input-to-reference signal feedthrough of the decoupled reference net in (a).

resistor values, dR, is assumed to have a Gaussian distribution with zero mean value and a standard deviation σ_{R},

$$dR \sim \mathrm{N}(0, \sigma_{\mathrm{R}}). \tag{5.7}$$

In addition to the resistor mismatch, the fluctuations of the reference net supply voltage V_{ref} are also modeled. The fluctuations are caused by, e.g., crosstalk. The V_{ref} fluctuations is modeled by calculating the reference net supply voltage deviation, dV_{ref}, in each sample, and then dV_{ref} is added to the nominal reference net supply voltage V_{ref}. New reference voltages are thereby calculated every sample. In this model, the reference net supply voltage deviation is assumed to have a Gaussian distribution with zero mean value and a standard deviation σ_{ref} in units of LSB,

$$dV_{\mathrm{ref}} \sim \mathrm{N}(0, \sigma_{\mathrm{ref}}). \tag{5.8}$$

The model of the resistor mismatch and the supply voltage fluctuations is illustrated in Figure 5.8. As seen the reference net supply voltage variations is included on both the positive, as well as the negative supply. The results of the simulations are presented in Figure 5.9. In Figure 5.9(a) and Figure 5.9(b) the average ENOB is plotted as a function of the standard deviation of the resistor mismatch, σ_{R}, and the standard deviation of the

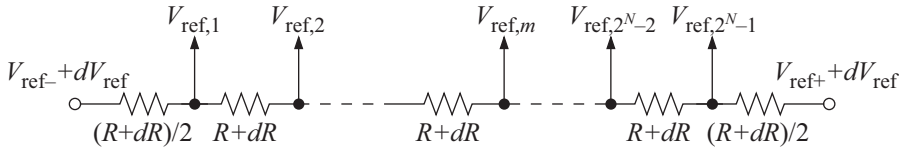


Figure 5.8: Reference net model used for the MATLAB simulations of the resistor mismatch and reference net supply fluctuations.

reference voltage supply fluctuations, σ_{ref}. In Figure 5.9(c) the yield is plotted as a function of the standard deviation σ_R with an ENOB design target of 5.5 bits for a 6-bit flash ADC with a full-scale voltage of 0.5 V. Finally, Figure 5.9(d) shows the yield plotted with the same design target, but as a function of σ_{ref}.

As seen in Figure 5.9(a) the standard deviation of the resistor mismatch should be less than 5 % to yield an average ENOB equal to the maximum of six bits. Assuming an ENOB design target of 5.5 bits it is seen from the yield in Figure 5.9(c) that σ_R should be less than 7 % to obtain a yield of about 99 %. For the reference supply fluctuations it is seen from Figure 5.9(b) that σ_{ref} should be around 0.1 LSB for an average ENOB equal to the maximum of six. Finally, Figure 5.9(d) shows that a yield of about 99 % can be accomplished for a σ_{ref} of 0.4 LSB at an ENOB design target of 5.5 bits.

The INL and DNL are also important performance measures. In Figure 5.10 the yield is plotted having a design target of |INL|< 1 LSB and |DNL|< 0.5 LSB. In this simulation the reference net resistance values are assumed to be within $\pm dR_{ref}$. The probability of a Gaussian distributed random variable to be within six standard deviations σ is close to 100 %. The standard deviation of the reference net resistances in the simulation yielding the results in Figure 5.10 is therefore $dR_{ref}/300$.

5.3 Comparator

After manufacturing, the process variations over the chip cause mismatch between devices. This is especially serious for the differential inputs of amplifiers, since these generally are assumed to have identical properties during the design. The mismatch between the input transistors results in an input offset voltage of the differential amplifier. Since comparators have a differential pair in the input stage, they also suffer from mismatch, causing an offset voltage between the inputs. The input offset voltage is also modeled

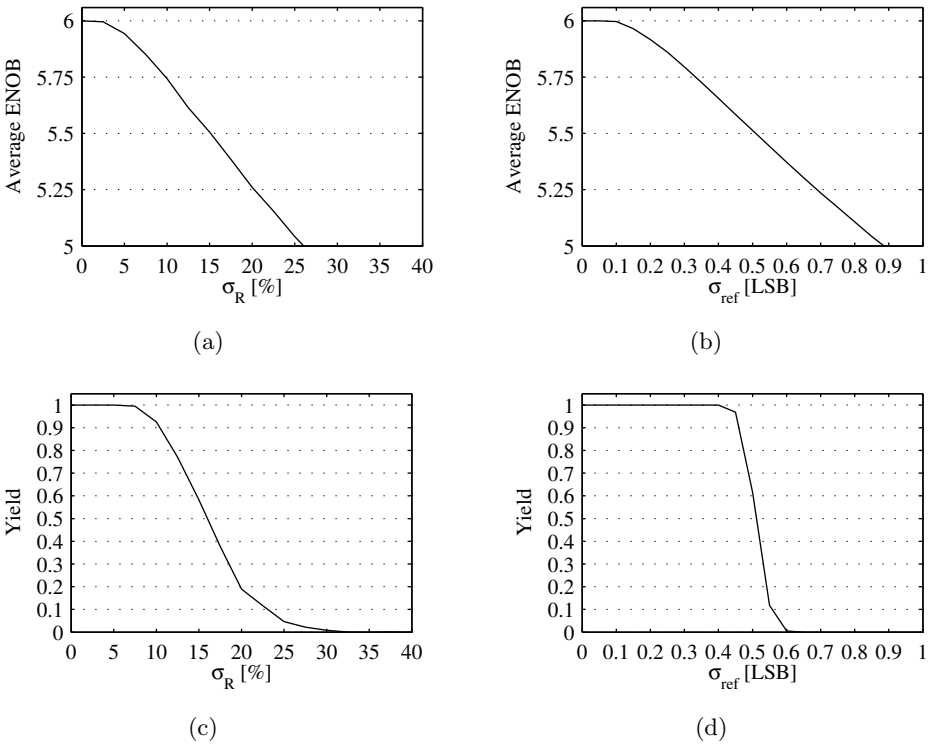
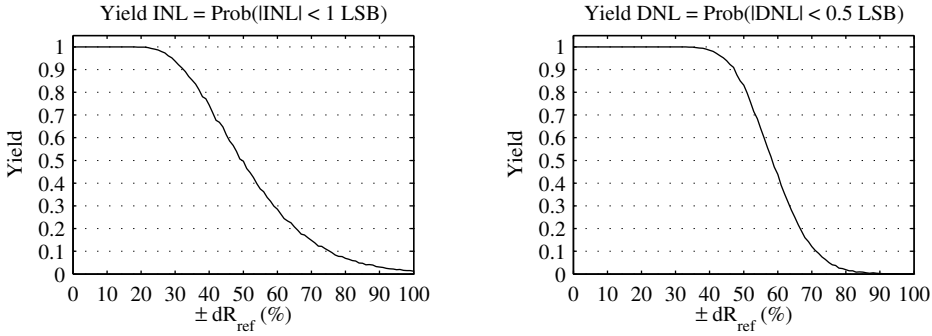


Figure 5.9: The average ENOB plotted as a function of (a) σ_{R} and (b) σ_{ref} for a 6-bit flash ADC with a full-scale of 0.5 V. The yield is plotted as a function of the same variables for the same ADC with the design target ENOB of 5.5 bits, in (c) and (d) respectively.



(a) (b)

Figure 5.10: The yield for the design target of (a) |INL|< 1 LSB and (b) |DNL|< 0.5 LSB.

and simulated in MATLAB. The offset voltage V_{offset} is assumed to have a zero mean value Gaussian distribution with a standard deviation of σ_{offset}. The input offset is modeled by adding this random voltage to one of the terminals of the comparators, as illustrated in Figure 5.11. The results of the simulations are presented in Figure 5.12, where the average ENOB and the yield is plotted as a function of σ_{offset} in units of LSB.

Figure 5.12(a) shows the average ENOB as a function of σ_{offset}. From the plot it is seen that σ_{offset} should be less than 0.1 LSB to obtain the maximum ENOB of six bits. Figure 5.12(b) shows further that for an ENOB design target of 5.5 bits the requirement on σ_{offset} can be increased to 0.2 LSB and still obtain a yield of 99 % or more.

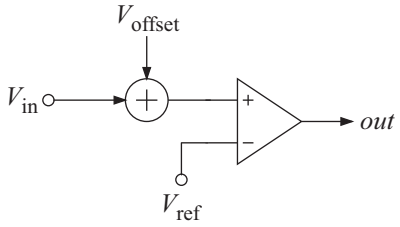


Figure 5.11: The comparator model used in the MATLAB simulations with a mismatch offset.

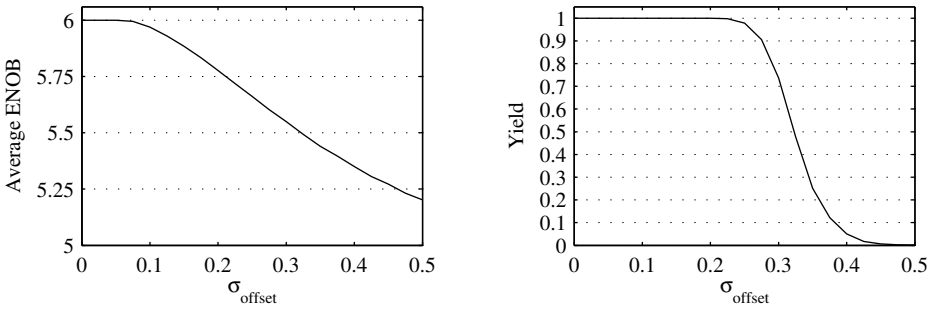


Figure 5.12: (a) The average ENOB and (b) the yield plotted as a function of the comparator-offset standard deviation, σ_{offset}, for a 6-bit flash ADC with a full-scale of 0.5 V and a design target ENOB of 5.5 bits.

5.4 Thermometer-to-Binary Decoder

The bubble errors in the comparator outputs are due to the timing difference between the clock signal and the input signal. The timing difference causes an uncertainty in the effective sampling instant of each comparator, which is of concern if no SH circuit is used. The bubbles the uncertainty gives rise to can have significant effect on the ENOB of the ADC. Different thermometer-to-binary decoder topologies are able to suppress these bubble errors to a varying degree. To evaluate their performance in terms of bubble error suppression, a MATLAB model is developed for each topology of interest, i.e., the ROM decoder [92, 106], ones-counter decoder [52, 92], folded Wallace tree decoder [99], and the MUX-based decoder [92]. These models are presented in this section, together with the simulation results.

The uncertainty in sampling instant due to the timing difference between the clock and input signal lines, Δt, is modeled by a Gaussian distribution with zero mean value and a standard deviation σ_{t},

$$\Delta t \sim \text{N}(0, \sigma_{\text{t}}). \tag{5.9}$$

The input signal is assumed to be a sinusoid with the peak-to-peak magnitude equal to the full-scale voltage, and with the frequency f_{in},

$$V_{\text{in}} = \frac{V_{\text{FS}}}{2} \sin\left(2\pi f_{\text{in}} t\right). \tag{5.10}$$

The maximum of the time derivative of the input can then be calculated in the same way as in (3.37). An approximation of the maximum time

derivative of the input is

$$\frac{\Delta V_{\text{in}}}{\Delta t} \approx \max\left\{\left|\frac{dV_{\text{in}}}{dt}\right|\right\} = \pi f_{\text{in}} V_{\text{FS}}. \tag{5.11}$$

The effect of the timing difference is therefore an uncertainty in the sampled input voltage, ΔV_{in}. Using (5.11), the maximum uncertainty in the sampled input voltage have a Gaussian distribution according to

$$\Delta V_{\text{in}} \sim \text{N}(0, \sigma_{\text{t}}\sqrt{\pi f_{\text{in}} V_{\text{FS}}}). \tag{5.12}$$

The uncertainty ΔV_{in} is added to the input V_{in} in the simulations. The sampling time uncertainty is therefore modeled as an offset voltage on the input of the comparators, given by (5.12), which yields the comparator model shown in Figure 5.13.

Note that the inherent input referred offset of the comparators due to mismatch is modeled in the same way as the effect of the timing difference. Compare, e.g., Figure 5.11 and Figure 5.13. Hence the input referred offset of the comparators is also a source to the bubble errors.

The comparator model in Figure 5.13 is used in the MATLAB simulations of a flash ADC with the four different decoders, i.e., the ROM decoder with 3-input NAND gates for bubble error correction, the ones-counter decoder, the MUX-based decoder, and the 4-level folded Wallace tree decoder. The results of the simulations are shown in Figure 5.14 and Figure 5.15.

In Figure 5.14 the average ENOB of the ADC is plotted as a function of the standard deviation of the timing difference between the clock lines and the signal lines, i.e., σ_{t}. As seen in the figure the performance of the MUX-based decoder is about the same as for the ROM decoder, with 3-input NAND gates used for the bubble error correction. Note that the MUX-based decoder has no special bubble error correction circuits. It is also seen that the ones-counter decoder has better performance than both the ROM

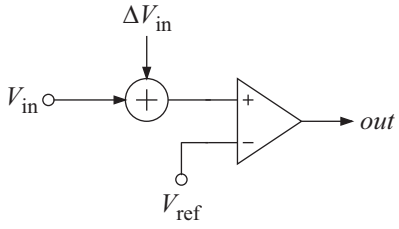


Figure 5.13: Comparator model used in the MATLAB simulations of the thermometer-to-binary decoders.

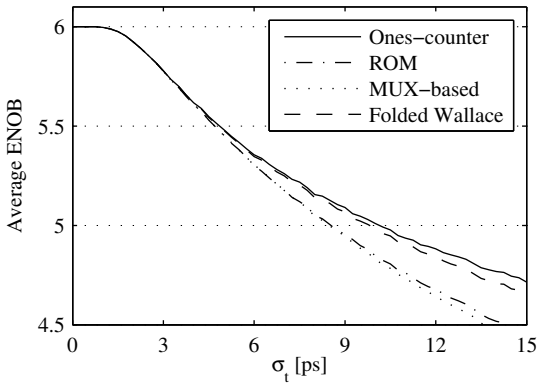


Figure 5.14: Average ENOB as a function of σ_t for the ROM decoder with 3-input NAND gates, the ones-counter decoder, the MUX-based decoder, and the 4-level folded Wallace tree decoder.

decoder and the MUX-based decoder. Finally, the 4-level folded Wallace tree decoder has a slightly lower average ENOB than the ones-counter. The reason for this is that the folded Wallace tree topology is more sensitive to bubble errors at the thermometer input levels connected to the 3-input OR gates shown in Figure 4.2, since these signals controls the MUX seen in the same figure.

In Figure 5.15 the yield of the ADC is plotted as a function of σ_t. The design target is an ENOB of 5.5 bits. As seen in this figure the differences in yield between the topologies are small. However, Figure 5.15 indicates that the ones-counter and folded Wallace tree decoders result in a slightly higher yield than the ROM and MUX-based decoders.

5.5 DEM Flash ADC

To evaluate the performance of the proposed DEM flash ADC in Section 4.3, a behavioral model of the topology is developed in MATLAB with one modification compared with the topology shown in Figure 4.8. The random generator is replaced by a pseudo-random bit stream (PRBS) generator, shown in Figure 5.16. The PRBS generator consists of a 15 stage shift register where the first stage is initiated to logic one and the other stages to logic zero. The outputs of the last and the first stage of the shift register are connected to an XOR gate, whose output is connected to the input of the first stage. This configuration yields a PRBS with a maximum sequence

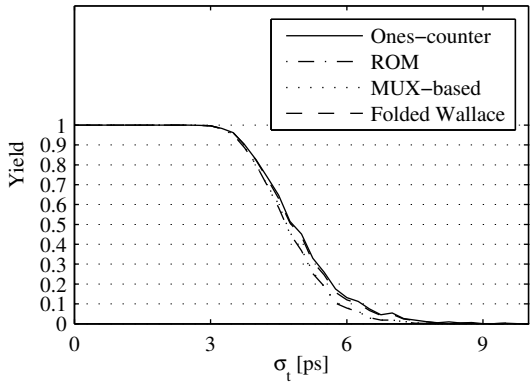


Figure 5.15: The yield as a function of σ_t for ROM decoder with 3-input NAND gates, ones-counter decoder, MUX-based decoder, and 4-level folded Wallace tree decoder. The design target is an ENOB of 5.5 bits.

length, i.e., $2^{15} - 1$ long, before it is repeated, which is verified by the simulations in MATLAB of the PRBS.

As mentioned in Section 4.3.1 the 1-of-M decoder consists of an M stage circular shift register where one position is set to logic zero and the rest to logic one. The zero is shifted one position each clock cycle. The shift direction is set by the output of the random generator, which in this case is the PRBS generator. This approach ensures that the reference voltages changes are equal to V_{LSB}, which should reduce the settling time of the reference generator compared with the circuits proposed in [11, 12]. The reduced settling time improves the speed of the flash ADC.

In the behavioral model an uncertainty in the resistor values in the reference net as well as the offset of the comparators are included. The resistor uncertainty is considered to be Gaussian distributed with a standard deviation σ_{R} in value of 10 %. The comparator offset is also assumed to have a Gaussian distribution with a standard deviation σ_{offset} of 15 mV. V_{ref} is 1 V and the resolution is six bits. The output spectrum from a MATLAB simulation is depicted in Figure 5.17. The number of clock cycles is 2^{16}.

In Figure 5.17(a) the output spectrum of one simulation is shown when no DEM is applied. In this simulation the spurious tones are clearly visible, and the SFDR is about 37 dB. Applying fully random DEM, i.e., the zero on one of the 1-of-M decoder outputs is allowed to be shifted to any of the M decoder outputs each sample, the spurious tones are distributed over the spectrum. This is shown in Figure 5.17(b). Note that when the

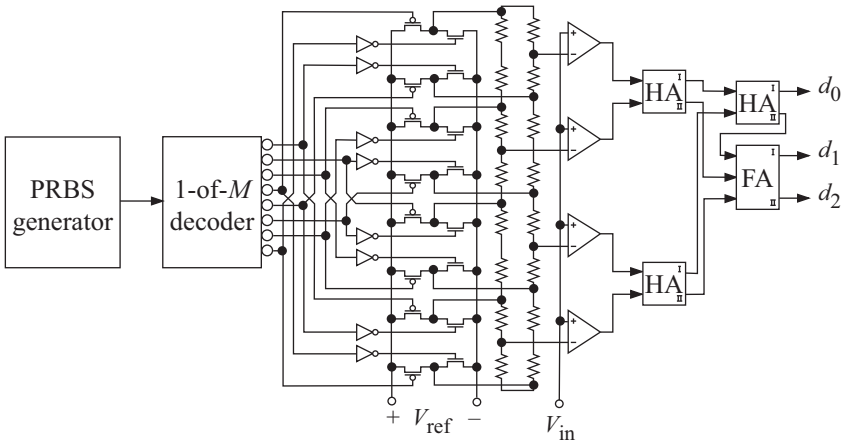


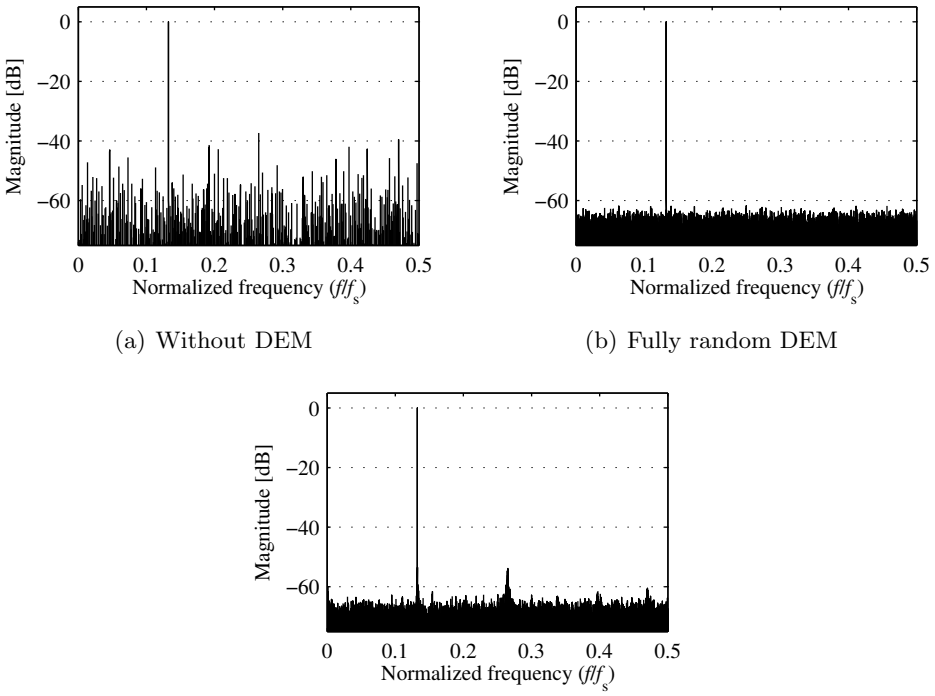
Figure 5.16: Illustration of the proposed DEM flash ADC with five quantization levels and a PRBS generator.

spurious tones are distributed over the spectrum the noise floor is raised. The SFDR is however significantly improved, and is for the fully random DEM increased to 62 dB. However, as mentioned earlier, this is not a viable approach for a high-speed ADC due to the settling time of the reference voltages, which would reduce the conversion rate significantly. In this case the random generator is realized by a PRBS, with its simulation results shown in Figure 5.17(c).

A histogram of the position of the zero in the output of the 1-of-126 decoder is shown in Figure 5.18. As seen the zero position is not uniformly distributed like in the case of fully random DEM. Not having a uniform distribution is intentional since the DEM is restricted to only shift the zero a single position. If the zero position would have been uniformly distributed it would mean that the decoder shifts the zero one step in the same direction each clock cycle, i.e., there would be no randomization of the shift direction.

The output spectrum of the DEM flash ADC with the PRBS generator is shown in Figure 5.17(c). This figure shows that spurious tones are still present, and the SFDR is 54 dB. However, the SFDR is improved by as much as 17 dB, compared with the spectrum for the ADC without DEM in Figure 5.17(a).

The simulation results in Figure 5.17 are taken from a single simulation, and do therefore not show the statistical variation. A simulation of the yield for the three different cases above is also made. The results of the yield simulations are shown in Figure 5.19. In this figure the yield is plotted as a



(a) Without DEM

(b) Fully random DEM

(c) PRBS DEM

Figure 5.17: Simulated output spectrum (a) without DEM, (b) with fully random DEM, and (c) with PRBS DEM for six bits of resolution, a σ_{R} of 10 %, and a σ_{offset} of 15 mV.

function of the SFDR design target, $\mathrm{SFDR}_{\mathrm{target}}$. The yield is therefore the probability that the SFDR is larger than $\mathrm{SFDR}_{\mathrm{target}}$. In the simulations the standard deviation of the comparator input offset voltage, σ_{offset}, is 15 mV with a full-scale voltage of 1 V. The standard deviation of the resistor values, σ_{R}, is 10 %. In addition, the number of clock cycles is 2^{16}. As seen in Figure 5.19(a) the yield is significantly improved when applying DEM, especially if fully random DEM is applied. From Figure 5.19(b) it is seen that for a yield of 99 % the SFDR design target is increased by about 11 dB if PRBS DEM is applied, and almost 26 dB if fully random DEM is applied, compared with the ADC without DEM.

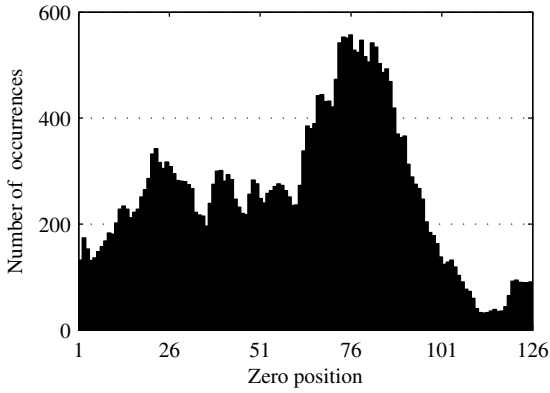
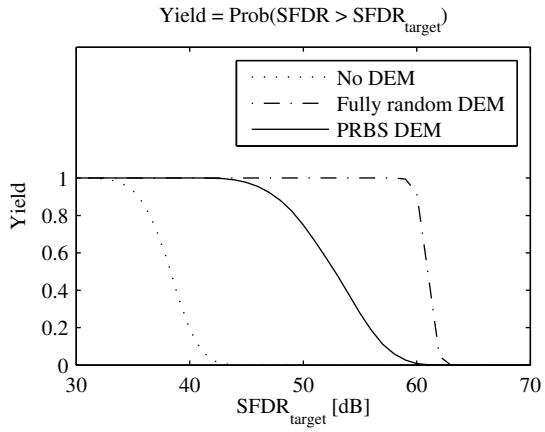
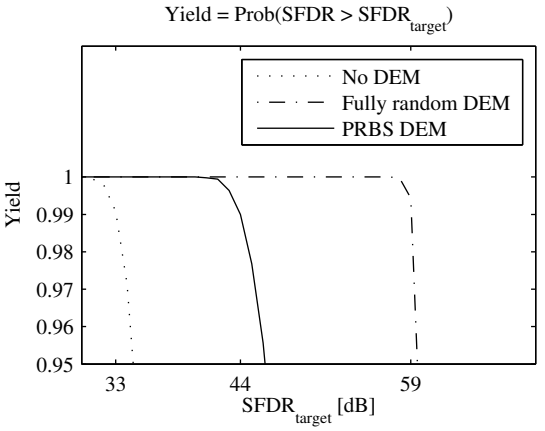


Figure 5.18: Histogram of the position of the logic zero in the output of the 1-of-126 decoder.



(a)



(b)

Figure 5.19: In (a) the yield for the flash ADC is plotted as a function of the design target SFDR without DEM, with fully random DEM, and with PRBS DEM, for a resolution of six bits, a σ_{R} of 10 %, and a σ_{offset} of 15 mV. In (b) a part of the plot has been magnified.

Chapter 6

ADC Experiments

In this chapter the design of three ADCs is presented. In Section 6.1 the design of a latched comparator used in the designed ADCs is presented. The design of the reference ADC is presented in Section 6.2. The purpose of the reference ADC is to enable comparison of the different topologies by relating them to the reference design. In Section 6.3 a design of a 6-bit flash ADC with the proposed MUX-based thermometer-to-binary decoder is presented. In Section 6.4 the design of a flash ADC with the proposed DEM is presented. Hence the section contains the design of the reference generator, the PRBS, a 1-of-126 decoder, and the thermometer-to-binary decoder. The topologies of the digital circuits used in the ADC designs are presented in Section 6.5. Some comments on the design of the circuits are also made. In the last section, Section 6.6, the design of the ESD protection circuits is presented.

The results of the modeling in Chapter 5 are used in the design considerations. As an example, the modeling of the clock skew in Section 5.1 indicate that a flash ADC with resolution of up to six bits and an input frequency of 1 GHz can be operated without a SH circuit on the input. The ADCs in this chapter are therefore designed without SH circuits. The elimination of the SH circuit saves power, but the comparator must be designed

for a higher bandwidth, i.e., their power consumption is increased instead. The result of the modeling of the reference generator in Section 5.2 is used to calculate the maximum reference net resistance of the reference generator in the flash ADC as well as the DEM flash ADC. The behavioral level simulations of the ADC performance for different decoders in Section 5.4 indicated that the chosen decoder topology in the respective ADC design would not affect the overall ADC performance adversely. Finally, the results from simulations of the DEM flash ADC behavioral models presented in Section 5.5 demonstrates the concept of introducing DEM into the reference generator of flash ADCs and estimates the SFDR improvement. The behavioral level model of the PRBS circuit is used to decide the type of PRBS circuit, whose design is presented in Section 6.4.2, which is a part of the design of the DEM flash ADC, presented in Section 6.4.

6.1 Comparator

This section describes the design of the comparator used in the implemented ADCs. The measurement results of the designed comparator are presented in Section 7.1. The chosen comparator topology is shown in Figure 6.1. As seen from this figure the comparator consists of a latched comparator with a preamplifier having resistive loads. As mentioned in Section 3.5.3, the use of a preamplifier reduces the input referred offset of the comparator and reduces the kick-back noise caused by the latched comparator.

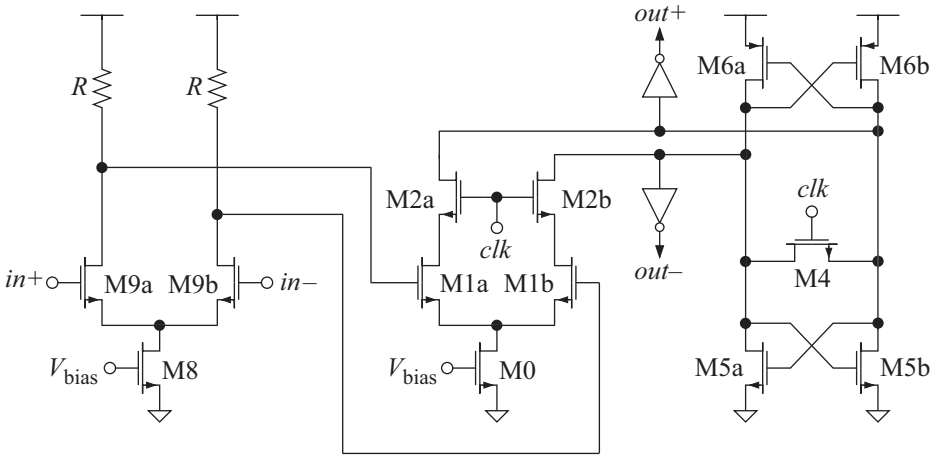


Figure 6.1: The comparator topology used in the designed ADCs.

6.1.1 Preamplifier

In Figure 6.1 it is seen that the preamplifier consists of the bias transistor M8, the differential input M9a and M9b, and the two resistors R as passive load. An amplifier with an active load could be designed for a higher gain than with a passive load. However, the requirement on the bandwidth of the preamplifiers is high. The bandwidth is thereby traded for a lower gain [106]. The differential preamplifier therefore has resistive loads, where the resistors are implemented with the unsilicided high value polysilicon layer available in the used partially depleted SOI CMOS technology. This choice yields a preamplifier gain less than three.

As mentioned in Section 3.5.3 it is important to design the preamplifiers of the comparators so that their signal dependent delay is minimized, otherwise the third order distortion on the converter output would be too large. The third order distortion due to the signal dependent delay is given by the expression in (3.40) [91]. This is plotted in Figure 6.2 as a function of the $f_{\mathrm{amp}}/f_{\mathrm{in}}$ ratio for different linear ranges V_{lr}, where $V_{\mathrm{lr}} = V_{\mathrm{gs}} - V_{\mathrm{T}}$. The full-scale voltage V_{FS} is 0.5 V. This plot is used in the trade-off to find suitable values for their linear range and bandwidth.

The third order distortion should be below the quantization noise floor, which is given by (3.5b). Since the resolution N of the ADCs is six, the third order distortion should be below -38 dB, as seen from using (3.5b). The linear range V_{lr} is chosen to 175 mV. Figure 6.2 then gives that the third order distortion requirement is fulfilled for an $f_{\mathrm{amp}}/f_{\mathrm{in}}$ ratio of 2.5.

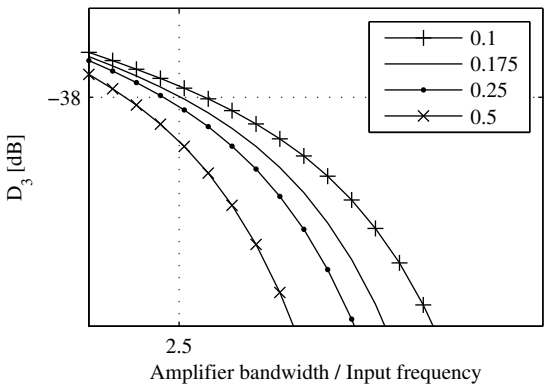


Figure 6.2: Third order distortion as a function of the $f_{\mathrm{amp}}/f_{\mathrm{in}}$ ratio for linear ranges $V_{\mathrm{lr}} = 0.1$, 0.175, 0.25, and 0.5 V.

An f_{amp}/f_{in} ratio of three is chosen to obtain a design margin. A sampling frequency of 2 GHz yields a Nyquist frequency of 1 GHz, i.e., the maximum input frequency of the ADC. Hence, the -3 dB bandwidth of the preamplifier should be 3 GHz.

To reduce the mismatch of the input transistors, M9a and M9b in Figure 6.1, due to the self-heating, the transistors are placed in the same well during layout. The temperature difference between the input transistors should thereby be reduced compared with a placement in separate wells, as explained in Section 2.5.2.

6.1.2 Latched Comparator

In Section 3.4.2 it is stated that for high speed ADCs the comparators generally are based on a regenerative latch, which gives a very fast comparator that can operate at a low power supply voltage. The comparator in this design, depicted in Figure 6.1, therefore consists of a differential input pair, a regenerative latch and inverters as buffers at each output. The differential input pair is the transistors M1a and M1b, which are connected to the bias transistor M0. M2a and M2b are used to reduce the kick-back noise, as explained in Section 3.5.3. The regenerative latch consists of the transistors M4, M5a, M5b, M6a, and M6b.

The transistor pairs M6a/M5a and M6b/M5b realizes the two inverters, or negative gain amplifiers, of the regenerative latch. The outputs of the inverters are connected to the input of the other inverter. A fifth transistor, M4, is connected between the outputs of the two inverters. When the clock goes high, the transistor M4 sets the latch in its metastable state. The input stage of the comparator is at the same time turned on. The input stage causes an imbalance between the currents through the two metastable inverters of the latch. This imbalance is dependent on the signal on the input of the comparator. When the clock goes low, the transistor M4 is turned off and the latch enters its evaluation phase. The current imbalance in the latch caused by the input stage then steers the latch to one of its stable states.

In Section 2.5.2 it is stated that fast switching circuits are less affected by the self-heating effect. As mentioned the reason is that since they are constantly switched on and off they will reach a thermal equilibrium at a certain device temperature that is lower than if they are on the whole time. Since the input stage of the comparator is off when M2a and M2b are off, the self-heating should have less effect on the input stage than if it is always on. To further reduce the effect of the self-heating the transistors M1a and

M1b are placed in the same well for the same reason as for M9a and M9b, i.e., to reduce the temperature difference between the input transistors of the differential input stage.

As mentioned in Section 3.5.3 the metastability error rate can be reduced by designing the inverters, i.e., buffers, on the output of the latch to have a higher threshold voltage than the latch. This is accomplished by making the ratio between the size of the PMOS and NMOS transistors of the inverters larger than the ratio of the PMOS and NMOS transistors of the regenerative latch [105]. The output is then logic one when the latch is in the reset phase, which should reduce the metastability errors on the outputs of the comparator.

The comparator output buffers are each connected to a D flip-flop, which holds the output of the comparator for a clock period. This gives the thermometer-to-binary decoder more time to perform the conversion. The D flip-flops also increase the regeneration gain of the latched comparator. The increased regeneration gain further reduces the metastability error rate of the comparators [63].

6.2 Reference Flash ADC

A reference flash ADC is implemented in order to improve comparison between the different decoder topologies and ADCs with and without DEM. The ADC thereby reuses building blocks from both the ADC with MUX-based decoder, as well as the ADC with DEM. More details on the design are presented in Section 6.3 and Section 6.4.

The reference generator of the reference ADC is the same as for the ADC with MUX-based decoder, i.e., it is designed for a high input frequency and is decoupled according to Section 6.3.1. The thermometer-to-binary decoder used in the reference ADC is based on a ones-counter and is the same as the one used in the ADC with DEM. The design of the ADC with DEM is described in Section 6.4.4. The comparator used in this ADC is the same as for the other two types of ADCs.

6.3 Flash ADC with MUX-Based Decoder

This section presents the design of the reference generator and the thermometer-to-binary decoder for the flash ADC with MUX-based decoder, starting with the reference generator. The ADC topology is illustrated by Figure 3.11. The design of the comparators used in the ADC is presented in Section 6.1.

The results of the manufactured and measured ADC are presented in Section 7.4 and discussed in Section 8.4.

6.3.1 Reference Generator

As seen in Figure 3.11 the reference generator of the ADC with MUX-based decoder consists of a string of equally sized resistors, except for the resistors on the top and bottom of the string. These resistors have a resistance value that is half compared with the other resistors. This choice of resistance yield that a ramp input would yield the quantization error shown in Figure 3.1.

As mentioned in Section 3.5.2 the parasitic capacitors result in input signal feedthrough to the resistor ladder generating the reference voltages. This feedthrough may cause too large reference voltage variations if the resistance of the resistors is too large. The reference net is therefore modeled to yield the reference net resistance that obtain sufficiently low input-to-reference feedthrough at the lowest power consumption. The model is presented in Section 5.2 where the expression (5.6) is derived. That expression is used to calculate the maximum reference net resistance.

To have some design margin to other error sources the reference net is designed for a maximum feedthrough of 0.25 LSB, i.e., q_{LSB} in (5.6) is 0.25. The maximum input frequency is set to be 1 GHz. After designing the comparator its parasitic input capacitance is derived, which is 13 fF. The total number of comparators is 63, hence C_{tot} in (5.6) becomes 0.83 pF, which is the total converter input capacitance excluding the input routing capacitance. Inserting these values into (5.6) gives that the maximum total reference net resistance, R_{tot}, should be 6 Ω. This low resistance would yield a reference net power consumption of about 42 mW. To reduce the power consumption the method discussed in Section 5.2.1 is applied, i.e., some of the reference net outputs are decoupled.

In Section 5.2.1 it is concluded that by decoupling a number of the reference net outputs the effect of input-to-reference net feedthrough can be further reduced, or the feedthrough can be traded for lower power consumption by increasing the total reference net resistance. This is utilized by decoupling every thirteenth reference net output by a 45 pF on-chip capacitor. The total reference net resistance R_{tot} could thereby be increased to 30 Ω and still having a feedthrough of less than 0.25 LSB. This choice of total resistance would reduce the power consumption of the reference net for the specified feedthrough. However, to obtain some design margin the resistance is chosen to 16 Ω. This still reduces the power consumption by more than 60 % compared with not decoupling the reference net outputs,

for the same input-to-reference feedthrough.

In the implementation the decoupling capacitors are realized by 45 pF on-chip capacitors, but the decoupling is assumed ideal in the derivation of (5.6). A model of the reference net with an R_{tot} of 16 Ω is therefore simulated on transistor level in Cadence to verify that the worst-case feedthrough still is below the design target of 0.25 LSB. In this model the reference net including its decoupling capacitors and the parasitic capacitors of the comparators are included. A reference net with only the reference net supplies decoupled is also simulated. The results of these simulations are presented in Figure 6.3. In both simulations the reference net supplies are assumed to be decoupled by 10 μF off-chip capacitors.

In Figure 6.3 the simulation result of the decoupled reference net is plotted together with the case where the reference net is not decoupled. As seen from this figure the magnitude of the worst-case input-to-reference signal feedthrough is below 0.25 LSB at input frequencies up to more than 15 GHz for the decoupled case. Hence the design target is fulfilled.

For comparison the input-to-reference feedthrough is simulated with only the reference net supplies decoupled by 10 μF off-chip capacitors. Comparing the curves plotted in Figure 6.3, we find the feedthrough to be 0.6 LSB at the 1 GHz input frequency for the case where the reference net is not decoupled. In addition the feedthrough is increasing for higher input frequencies.

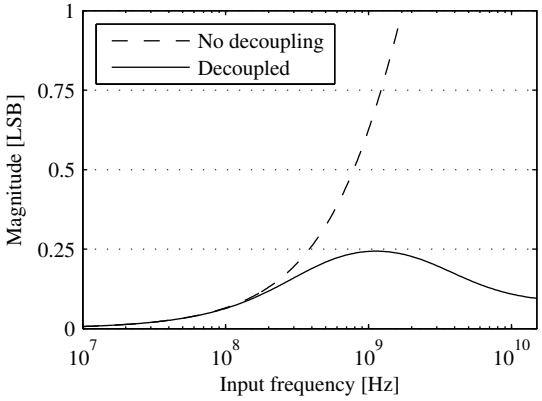


Figure 6.3: The worst-case input-to-reference signal feedthrough as a function of the input frequency with only the reference net supply decoupled and with every thirteenth reference output decoupled.

6.3.2 Thermometer-to-Binary Decoder

The thermometer-coded output of the comparators is converted to binary code by a thermometer-to-binary decoder. The decoder is implemented using the MUX-based decoder presented in Section 4.2. Since the 2:1 MUXs used in the decoder are buffered with one inverter on their output, as explained in Section 6.5.2, the decoder topology is slightly changed compared to the topology shown in Figure 4.6 for a resolution of four bits. The modified topology is shown in Figure 6.4 for the same resolution. As seen in that figure, a number of inverters are added to the decoder outputs with zero or even indices. In addition, the MUX inputs in the even columns i are interchanged, i.e., the input signals are connected to the "0"-input instead of the "1"-input, and vice versa. Compare, e.g., the MUXs in column one and two in Figure 6.4.

The reason for choosing the MUX-based decoder is that it has a shorter critical path and a lower hardware cost than the ones-counter decoders, as seen in Table 4.1, and that it is expected to consume less power than the

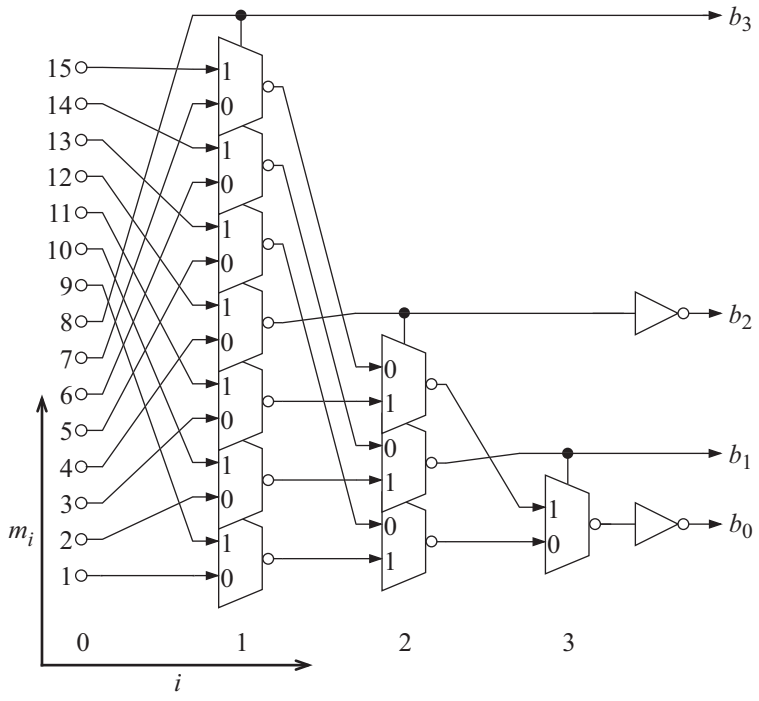


Figure 6.4: The modified MUX-based decoder topology for four bits.

ones-counter decoders [92, 95]. In addition, it has a more regular structure than the other decoders, which is an advantage when doing the layout. The bubble error suppression of the MUX-based decoder is however slightly worse than for the ones-counter decoders, as seen in Figure 5.14.

6.4 DEM Flash ADC

This section presents the design of the DEM flash ADC, whose topology is illustrated by Figure 4.8(b). The purpose of this design is to demonstrate the DEM technique. The focus is therefore not on the speed performance in this design. As mentioned in Section 4.3 the requirement on maximum input frequency will affect the required MOSFET switch size. Hence the maximum input frequency is limited to about 130 MHz, which yield around 100 μm wide switch transistors at minimum gate length.

The design of the reference generator will be presented first, followed by the design of the PRBS circuit, and then the DEM control circuit. The results of the design of the DEM flash ADC are presented and discussed in Section 7.5.

6.4.1 DEM Flash ADC Reference Generator

The reference generator of the DEM flash ADC consists of two resistor strings connected in a circular structure according to Figure 4.8(b). Although they are connected in a circular structure, they can each be seen as individual resistor strings connected in parallel with the same reference supply voltage V_{ref}. The maximum total resistor value of each resistor string can therefore be calculated using the same method as for the flash ADC with MUX-based decoder, i.e., by using (5.6).

In this design, the same comparator is used as in the previously presented design. Hence C_{tot} is still equal to 0.83 pF. The maximum feedthrough in this design is one LSB, i.e., q_{LSB} is one. The maximum input frequency is limited to about 130 MHz. Using (5.6) yields that the maximum total reference net resistance R_{tot} of each of the two resistor strings should be less than 190 Ω. Further, since the settling time of the reference net limits the speed of the DEM flash ADC the parasitic capacitance on the reference net output nodes should be minimized. This implies that decoupling of the reference net output cannot be used to reduce the input-to-reference feedthrough further, or to reduce the power consumption of the reference net.

6.4.2 PRBS

On-chip random generators can use the thermal noise of resistors to generate the random signals [74]. In this work a PRBS generator is used. Although it does not give a true random output signal, the result of the behavioral level models show that DEM with a PRBS generator as random signal source still yield a performance improvement compared with not using DEM, as shown in Figure 5.17 and Figure 5.19. From these behavioral level models the PRBS circuit is extracted. The floor plan of the PRBS consisting of 15 D flip-flops and an XOR gate is shown in Figure 6.5

Connecting the D flip-flops of the shift register in one row during the layout would give a long routing distance from the last D flip-flop to the XOR gate, assuming the XOR gate is placed near the first D flip-flop. Having a single-row shift register floor plan would require a routing distance of about 700 μm in this design, i.e., the propagation delay of the signal along this path would be about 7 ps, assuming that the signal propagates with a speed equal to a third of the speed of light. In addition, the parasitic capacitance of the wire would also add to the signal propagation time. The propagation delay of the signal between the other stages would be much lower. To balance this delay the D flip-flops are placed in two rows, as illustrated by the floor plan of the PRBS in Figure 6.5. This floor plan yields similar signal propagation times between every stage of the PRBS.

6.4.3 1-of-126 Decoder

To minimize the settling time of the reference generator the DEM is restricted by only allowing neighboring comparators to exchange their reference voltages. In the behavioral level model of the 6-bit DEM flash ADC this is accomplished by implementing the 1-of-126 decoder by a 126-stage circular shift register. The shift register shifts a single zero, and it is capable

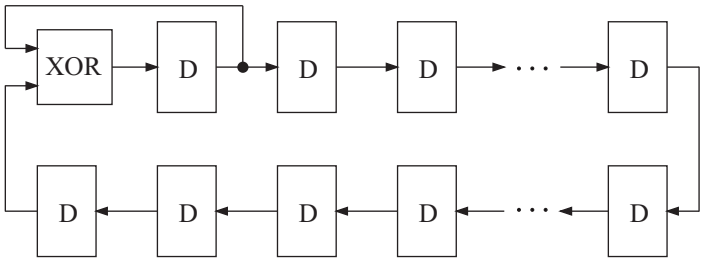


Figure 6.5: The floor plan of the PRBS generator.

of shifting its content one position in either direction. The results of the behavioral level simulations in Figure 5.17 and Figure 5.19 show that this restriction reduces the SFDR compared with the fully random DEM flash ADC. The performance enhancement of the restricted DEM flash ADC is however still significant, compared with the ADC without DEM.

As for the shift register of the PRBS generator, the shift register of the 1-of-126 decoder also has a floor plan where the shift register cells, i.e., the D flip-flops, are placed in multiple rows. The reason is the same as for the shift registers of the PRBS, i.e., to get minimum and equal signal propagation times between each stage. The floor plan of the 1-of-126 decoder is shown in Figure 6.6. One of the D flip-flops have a reset input and the other 125 D flip-flops have a set input. Hence the 1-of-126 decoder can be initiated to have only one zero on its outputs.

6.4.4 Thermometer-to-Binary Decoder

The thermometer-coded output of the comparators is converted to binary code by a thermometer-to-binary decoder, which can be implemented by various approaches, e.g., a ROM or a ones-counter [95]. In this case a ones-counter should be used, since the comparators are connected to different reference levels during each clock period, as determined by the PRBS and the 1-of-126 decoder. The reference level connected to each comparator therefore varies. The number of ones on the comparator outputs are however the same for the same input, but in a different order. A carry-save adder is therefore chosen as the decoder. It reduces the 63 inputs to 10 outputs, as illustrated by Figure 6.7. The numbers in parentheses in Fig-

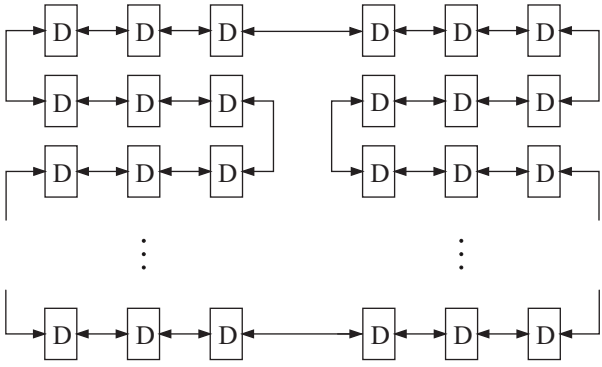


Figure 6.6: The floor plan of the 1-of-126 decoder.

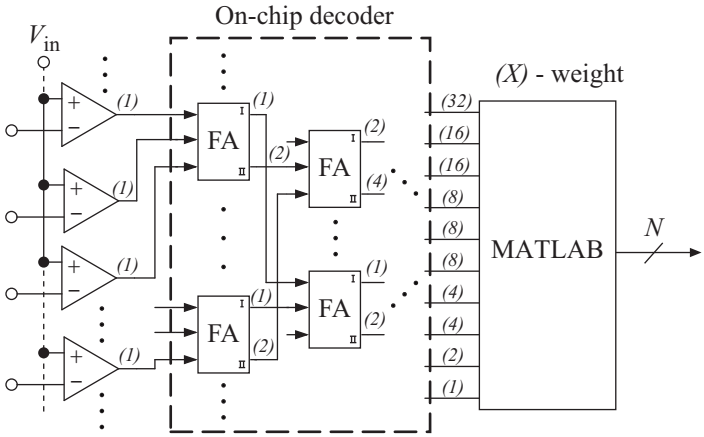


Figure 6.7: Illustration of the thermometer-to-binary decoder used for the 6-bit DEM flash ADC.

ure 6.7 indicate the relative weight of the bits on the different nodes. The decoding of the 10 remaining outputs to the binary value is subsequently performed by post-processing in MATLAB. The depth of the tree is thereby limited to six levels, which ensures that the decoder will not limit the speed performance of the ADC for sampling frequencies up to 800 MHz [95], according to the simulation results. In future designs the complete decoding to a binary output can be accomplished on-chip by introducing pipelining in the decoder. Further optimization during the sizing of each full adder can also improve the performance. To balance the propagation delay of the 10 output signals each of them pass through the same number of full adders. This approach causes some of the full adders to always have a digital zero on one or two of their three inputs.

6.5 Digital Circuits

In addition to the analog circuits used in the converter, the required digital circuits also had to be designed in the implementations, since no predefined standard cells are available in the design kit. This section presents some of the various digital circuits used in the designs and briefly describes the design of each of these circuits.

6.5.1 Full Adder

The full adders are realized by the static CMOS logic circuit depicted in Figure 6.8 [53]. They are designed to have a propagation delay of about 200 ps. In addition, each of their two outputs is designed to drive a load equal to the input of a similar full adder. Hence, they are designed for a load of about 150 fF.

6.5.2 2:1 MUX

The depth of the MUX-based decoder is five layers of 2:1 MUXs. Since the MUXs are based on transmission gates a slow decoder circuit would be obtained if the MUXs are unbuffered. To improve the maximum operation frequency of the decoder an inverter is introduced as an output buffer in the MUXs. A single inverter is introduced to have a low output-buffer propagation delay. The use of a single inverter is only lead to a minor modification of the original MUX-based decoder circuit, as seen by comparing Figure 4.6 and Figure 6.4.

The symbol of a transmission gate and its transistor level implementation are shown in Figure 6.9. The buffered 2:1 MUX schematic topology is shown in Figure 6.10, where the output buffer is included. The MUXs are designed with a similar MUX as the load. The design yields a propagation delay of 50 ps from the "0" or "1"-input of the MUX to its output, and

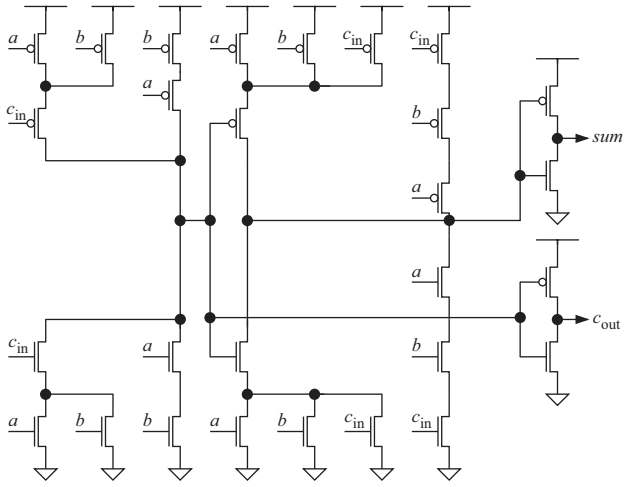


Figure 6.8: Full adder circuit.

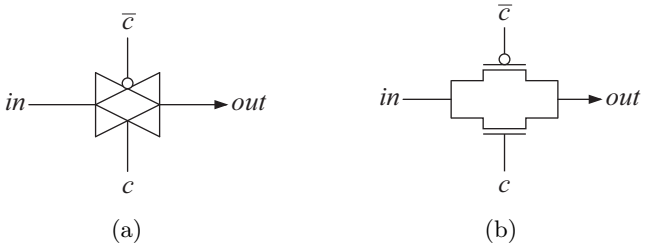


Figure 6.9: (a) Schematic symbol of a transmission gate and (b) its transistor level implementation.

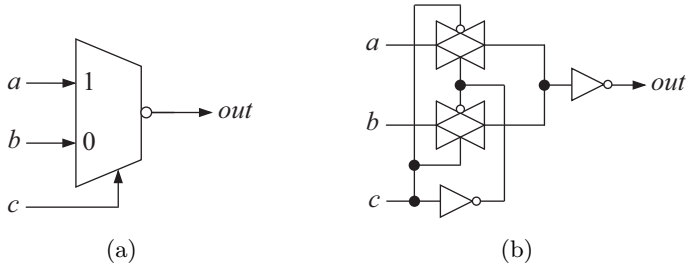


Figure 6.10: (a) Schematic symbol of a 2:1 MUX including the output buffer, and (b) the MUX circuit.

70 ps from the control input to the output.

6.5.3 D Flip-Flop

The D flip-flops are realized with transmission gates as depicted in Figure 6.11. The topology is the same for the D flip-flops with set as for those with reset. The only difference is the logic level of the "1"-input of the 2:1 MUX that is logic one for set and logic zero for reset. In Figure 6.11 the local clock buffer is also included.

The D flip-flops are designed for a 100 fF load and a propagation delay of 70 ps. In addition, the input must be stable at least 20 ps before the positive clock edge.

6.5.4 Digital Buffers

The digital buffers used throughout the design are all based on the same straight forward topology. A number of inverters are connected in series and sized to minimize the delay of the buffer and at the same time to drive

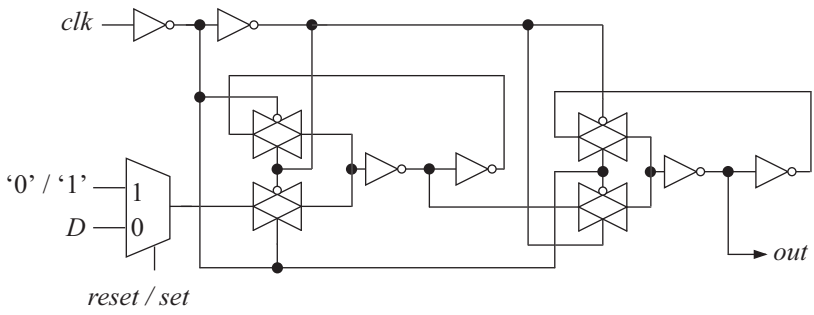


Figure 6.11: The D flip-flop circuit.

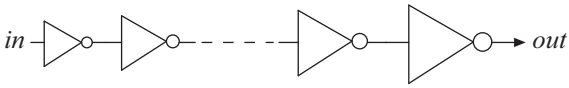


Figure 6.12: Illustration of the digital buffer topology.

the load on the output of the buffer. The buffer topology is illustrated by Figure 6.12 where the different drawn sizes of the inverters illustrates that the size of the inverters is gradually increased. The number of inverters in the buffers differs depending on the load it is designed for. The smallest buffer consists of two inverters. The largest buffers, i.e., the output pad buffers, consist of eight inverters.

6.6 ESD Protection Circuit Design

The technology used for the ADC implementations was still much on the test stage during this work. Very little was therefore included in the design kit. As an example, parameterized transistor cells used for generating the layout of the transistors were not included, nor were the pads. The ESD protection circuits of the pads therefore also had to be designed, which is presented in this section.

The used technology is a 130 nm partially depleted SOI CMOS technology. Hence two stages of the CMOS gated double-diode network, discussed in Section 2.6.2, are used as the the ESD protection for the input pads. The circuit is depicted in Figure 6.13. The purpose of the resistor R in this figure is to limit the ESD current to the second stage.

The circuit is designed for a maximum V_{ESD} of 1.5 kV using the human body model depicted in Figure 2.8(a). The -3 dB bandwidth of the

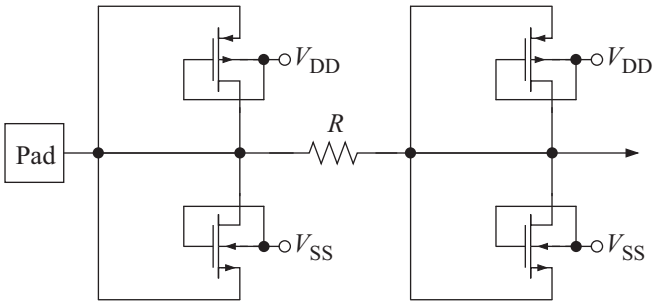


Figure 6.13: The circuit topology of the ESD protection circuits for the input pads.

ESD protection circuit is 8 GHz and should therefore not notably affect the performance of the ADCs.

Chapter 7

Results

The designed ADCs have all been manufactured in the 130 nm PD SOI technology provided in the framework of MEDEA+. The results presented in this chapter is therefore based on both measurements on three different ADCs, and transistor level simulations in Cadence using the foundry provided Berkeley short-channel insulated-gate field effect transistor (IGFET) model for SOI (BSIM3SOI) Eldo models. The provided models do only contain the typical transistor parameters. Hence no corner simulation are possible. In the simulations only the parasitic capacitances of the transistors are included. The interconnect parasitics are excluded since the provided design kit does not support extraction of the interconnect parasitics. Hence the interconnect parasitic capacitances are approximated by 200 pF/m as a rule of thumb during the design of the sub-circuits of the ADCs. The approximate interconnect distances are extracted from the floorplan and from the layout.

The inductance of the bond wires causes supply voltage variations, which can be large for high-speed circuits. The power supply is therefore simulated with the bond wires modeled as inductors. For the simulations of the power supply, the bond wires are assumed to have an inductance of 1 μH/m and a length of 2 mm.

As will be evident, some of the results presented in this chapter deviate much from the results derived from the simulations. A close examination of the designs eventually revealed a design flaw. A mask layer required for the definition of high-precision resistors is unfortunately missing in the layout of the resistors in the reference nets of the manufactured ADCs, which seriously degrades the spread of the nominal resistance value and the matching between the resistors.

This chapter is organized as follows. Some measurement results of a comparator used in the ADCs are presented in Section 7.1. In Section 7.2 the measurement setups used for characterizing the ADCs in terms of static and dynamic performance are presented. In Section 7.3 the measurement results of the reference ADC are presented. In Section 7.4 the simulation and measurement results for the flash ADC with MUX-based decoder are presented. Section 7.5 presents the simulation and measurement results of the ADC with DEM. The results presented in this chapter are discussed in Chapter 8.

7.1 Comparator

The comparator is designed and simulated using the BSIM3SOI models provided by the foundry. To reduce the third order distortion the preamplifier is designed for a -3 dB bandwidth of 3 GHz. The large bandwidth imposed a trade-off on the preamplifier DC gain, which is 9.2 dB. The resolution is derived by applying a ramp input to the simulated comparator for different sampling frequencies. These simulations yield that the resolution is better than 0.25 LSB up to sampling frequencies of 1.5 GHz.

The comparators have been manufactured, but due to limitations in the measurement set-up the comparators have only been tested for sampling frequencies of up to 500 MHz. These measurements yield a power consumption of 9.6 mW, including the output buffers, measured at a sampling frequency of 400 MHz and a constant input signal. A chip photo of the comparator chip is shown in Figure 7.1. The power supply fluctuation is reduced by having multiple power supply pads and by decoupling. The chip area is pad limited due to the large number of supply pads. Hence, after placing the comparator, the clock buffer, and the output buffers the remaining chip area is used for the decoupling capacitors. Those are the squares inside the pad frame in Figure 7.1. As seen from that figure the decoupling capacitors consume most of the chip area. The comparator is indicated in Figure 7.1 and has an area of 0.0018 mm^2. The total chip area is 0.7 mm^2.

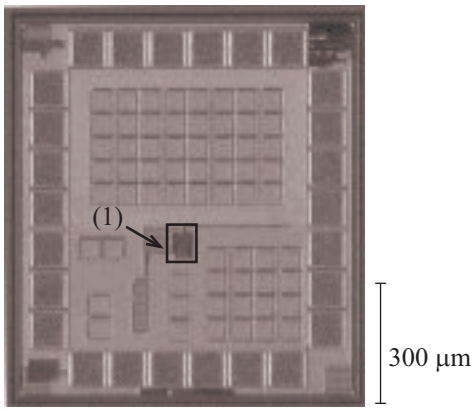


Figure 7.1: Chip photo of the comparator evaluation chip, where (1) indicates the outline of the comparator.

7.2 ADC Measurement Setup

This section describes the measurement setup used for characterizing the static and dynamic performance of the ADCs. Before the measurements the mounting method had to be decided, i.e., directly bonding the chip onto the printed circuit board (PCB) or into a package that is mounted onto the PCB. The main advantage with the latter is that it is easier to replace a malfunctioning chip without having to bond a new one onto the PCB. However after contacting several package manufacturers it is obvious that the size of the cavity where the chip is placed in the package are too large on all available packages. A too large cavity would result in long bond wires, which would degrade the performance too much. It is therefore decided to bond the chips directly onto the PCB.

For all measurements the ADC output are sampled by a Tektronix TLA721 logic analyzer having a maximum acquisition frequency of 8 GHz. The output data is then analyzed using MATLAB. The clock for the converters is generated by a HP E4432B signal generator that can generate sinusoidal signals in the frequency range from 100 kHz up to 3 GHz. The same type of signal generator is used to generate the input signal for the measurements of the dynamic performance.

7.2.1 Static Measurements

The static performance is first characterized. To reduce the dynamic effects as much as possible a low sampling frequency in the range of 10 MHz is

used for all ADCs. These measurements yielded the INL and DNL of the converters, and also the offset and gain errors. The measured offset is later used to adjust the input bias in the dynamic measurements.

The measurement setup for the static measurements is illustrated in Figure 7.2. The computer running MATLAB controls the DC power source that sets the DC level of the converter input. The DC level is then gradually increased until the whole input range is covered. The computer also controls when the logic analyzer samples the output. The logic analyzer samples the output and stores 1400 samples at each input level. The data is then used by the MATLAB program to calculate the average output, since the output was fluctuating somewhat around the ideal output code. When the measurement is done the resulting file containing the average output for each DC input level is analyzed by another MATLAB program that calculates the offset error, gain error, INL and DNL.

7.2.2 Dynamic Measurements

The offset error obtained from the static measurements is used to decide the input DC level to use for the dynamic measurements. In addition, the magnitude of the input signal is chosen for a maximum SNDR, i.e., a magnitude of about 90 % of the full-scale.

The measurement setup for the dynamic measurements is illustrated in Figure 7.3. The same logic analyzer as before is used to sample the output data from the converters, and the same signal generator is used to generate the clock signal. A second signal generator of the same model is used to generate the single tone sinusoidal input. The generated data is analyzed using MATLAB. A Hanning window is used to reduce the spectral leakage when calculating the power spectra of the ADC output, from which

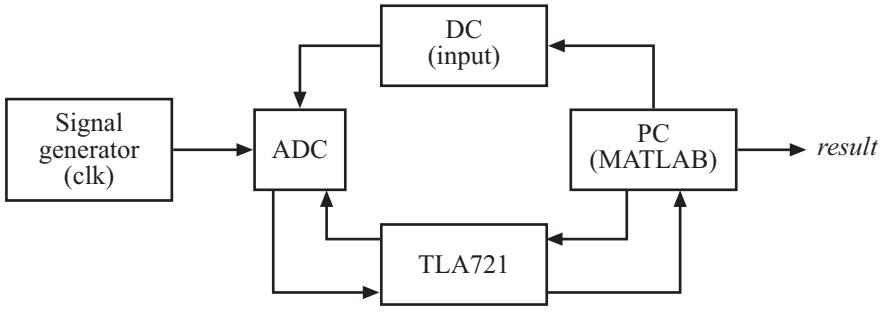


Figure 7.2: Illustration of the setup for the static performance measurements.

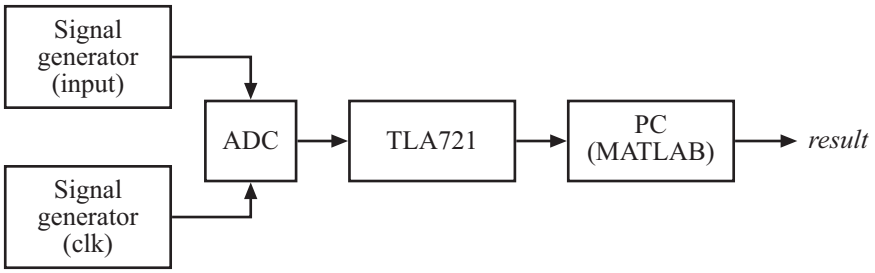


Figure 7.3: Illustration of the setup for the measurement of the dynamic performance.

the dynamic performances of the converters are extracted, i.e., SNDR and SFDR.

7.3 Reference ADC

7.3.1 Measurement Results

The total chip area of the reference ADC is 4.1 mm^2, and its core area is 0.7 mm^2, excluding the decoupling capacitors. A chip photo of the reference ADC is shown in Figure 7.4, where the main parts of the ADC are indicated. The remaining part of this section presents the static and dynamic measurement results.

Static Measurements

The offset and gain errors, together with the INL and DNL, are measured by applying a constant input that is gradually increased. Around 1400 samples are collected for each input level and the average of those samples is used to calculate the transition levels from which the INL and DNL is extracted, as described in Section 3.3.3. To minimize the dynamic effects the sampling frequency (f_s) is chosen to 7 MHz. The static measures are shown in the plots in Figure 7.5. In this figure the ADC transfer function is depicted in Figure 7.5(a). The INL and DNL are depicted in Figure 7.5(b) and Figure 7.5(c), respectively. The INL is within $2.1/-1.9$ LSB and the DNL is within $2/-0.6$ LSB. The offset error and gain error are also extracted from the measurements. From the measurement results depicted in Figure 7.5 the offset error is 6.2 LSB and the gain error is -6.7 LSB. For comparison with the ADC with DEM the INL and DNL are also calculated when disregarding the three levels closest to each edge of the reference net. The result is shown

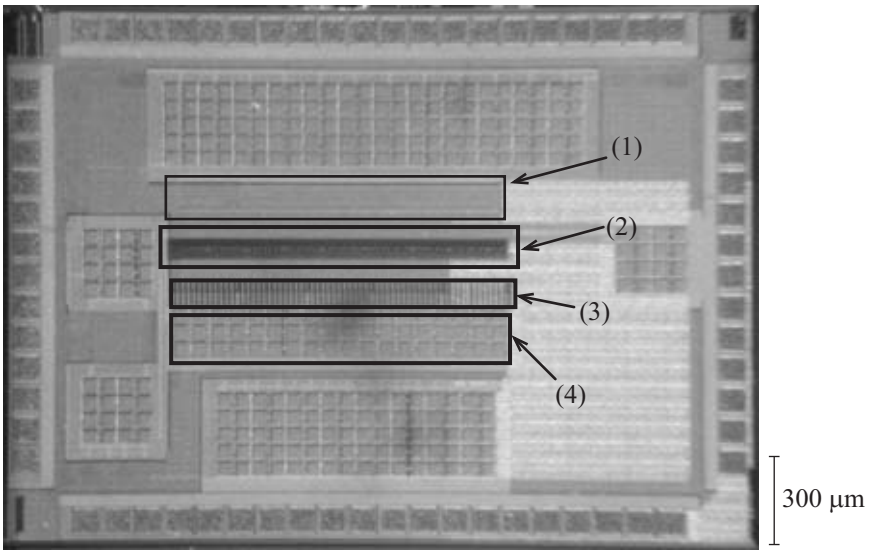


Figure 7.4: Chip photo of the reference flash ADC. Indicated parts are (1) ones-counter decoder, (2) comparators including the D flip-flops, (3) reference generator, and (4) reference net decoupling capacitors.

in Figure 7.6. The INL in Figure 7.6(a) is within 1.7/−1.6 LSB, and the DNL in Figure 7.6(b) is within 1.6/−0.7 LSB.

Dynamic Measurements

The dynamic performance is evaluated by applying a single tone sinusoidal input to the ADC and obtaining its spectral measures from a plot of the output spectrum. An estimate of the maximum sampling frequency, $f_{\mathrm{s,max}}$, is first derived. With a low frequency (495 kHz) sinusoidal input the sampling frequency is swept from 7 MHz up to sampling frequencies above 1 GHz. The result of these measurements is shown in Figure 7.7, where the SNDR in Figure 7.7(a) and the ENOB in Figure 7.7(b) are plotted as functions of the sampling frequency. The maximum SNDR is according to Figure 7.7(a) 26.3 dB, which is equivalent to an ENOB of about 4.1 bit. Further, the results in Figure 7.7 indicate that the maximum sampling frequency is about 470 MHz. The performance degradation in the frequency range from 500 MHz to about 900 MHz is believed to be due to the propagation delay through the thermometer-to-binary decoder that makes it difficult to sample the output properly with the used measurement setup.

In Figure 7.8(a) an input frequency of 27 MHz and a sampling frequency

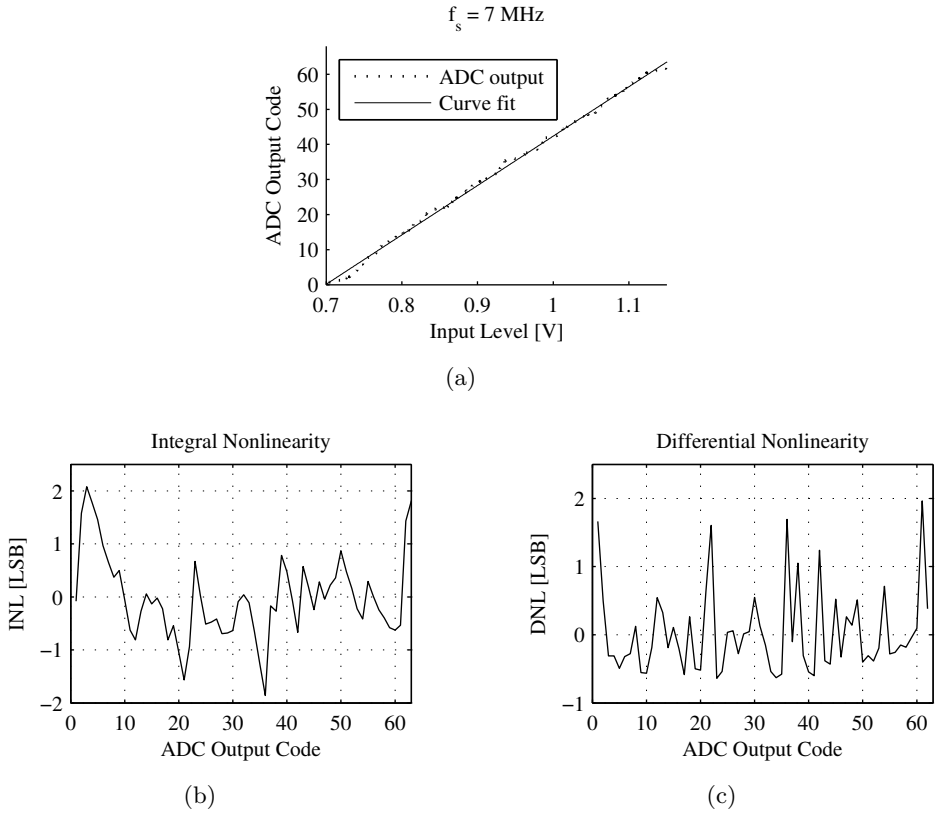
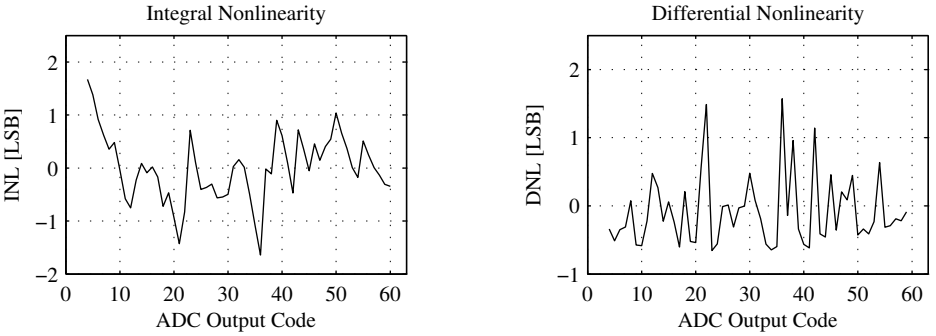


Figure 7.5: Static measurement results of the reference ADC at $f_s = 7$ MHz, where (a) shows the transfer function, (b) and (c) shows the INL and DNL, respectively.

of 440 MHz is used. The SFDR is then estimated to 35.3 dB, which corresponds to about 5.9 SFDR-bits according to (3.34). In Figure 7.8(b) the sampling frequency is also 440 MHz. The input frequency is however increased to 77 MHz. The SFDR is in this case estimated to 32.2 dB, which corresponds to about 5.3 SFDR-bits. In Figure 7.8(c) the input frequency is increased further, to 120 MHz, but the sampling frequency is still kept at 440 MHz, which yield an SFDR of 28.7 dB, corresponding to 4.8 SFDR-bits.

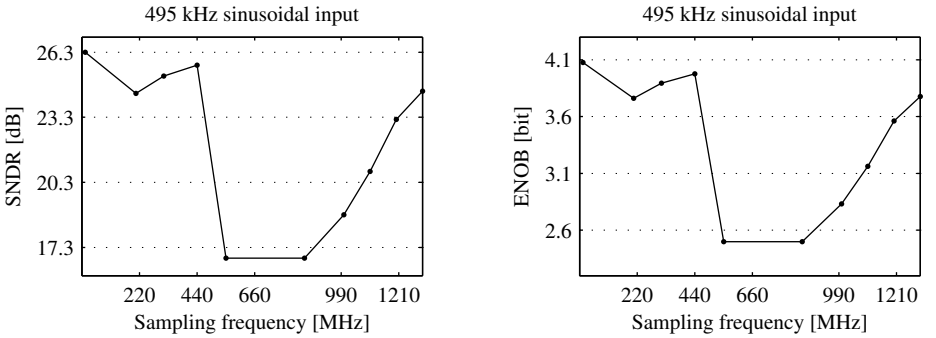
The power consumption of the ADC in the three cases in Figure 7.8 are 146 mW, 174 mW, and 175 mW, respectively, excluding the power consumption of the input and output buffers. Including the power consumption of the buffers the total power consumption becomes 246 mW, 294 mW, and 312 mW, respectively.

The thermometer-to-binary decoder is not complete, six more full adders



(a) (b)

Figure 7.6: The measured (a) INL and (b) DNL of the reference ADC at f_s = 7 MHz when disregarding the three reference levels closest to the edges of the reference net.



(a) (b)

Figure 7.7: The measured (a) SNDR and (b) ENOB of the reference ADC with a sinusoidal input of frequency f_{in} = 495 kHz as a function of the sampling frequency.

are required to decode the thermometer code completely. The power consumption of these six full adders is therefore estimated from simulations. These results yield an added power consumption of about 2 mW. The contribution from the digital part is about 70 % of the total power consumption, excluding the input and output buffers.

The figure of merit of the ADC is calculated disregarding the power consumption of the input and output buffers. For the 27 MHz input the ENOB is 3.8 bit, which yield a figure of merit of about 98 pJ. Increasing the

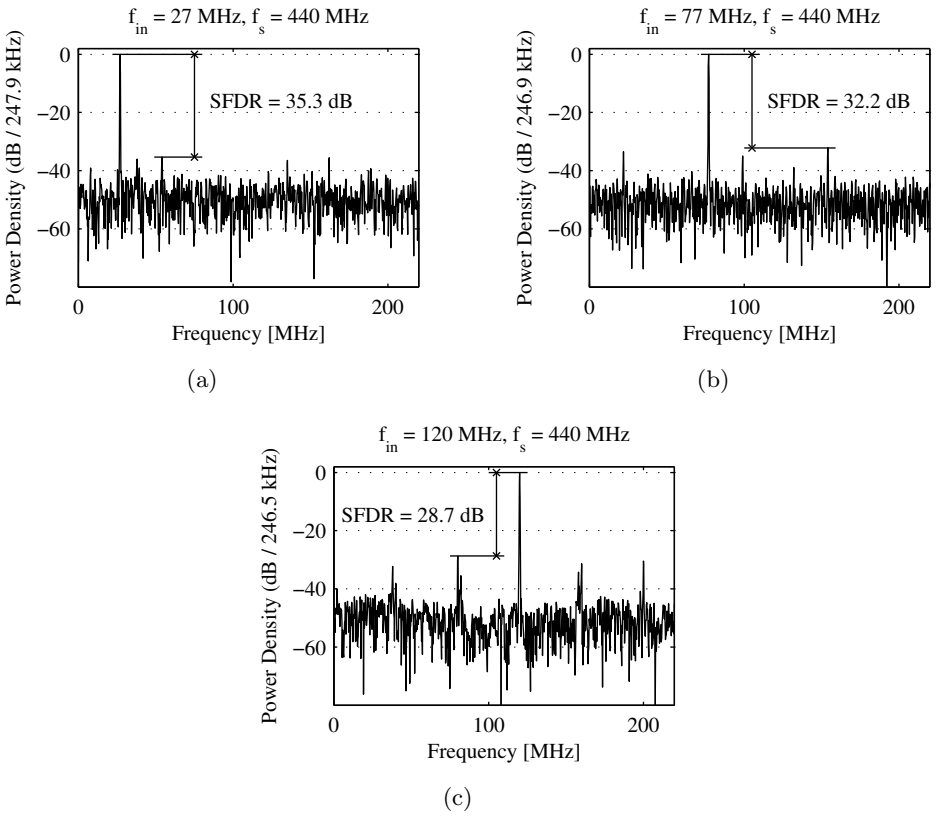


Figure 7.8: The measured SFDR for the reference ADC at a sampling frequency of 440 MHz and a sinusoidal input of frequency (a) 27 MHz, (b) 77 MHz, and (c) 120 MHz.

input frequency to 77 MHz yields an ENOB of 3.7 bit, and hence a figure of merit of 75 pJ. The last measurement yields an ENOB of 3.1 bit, which gives a figure of merit of 87 pJ. The measurement results of the ADC are summarized in Table 7.1.

7.4 Flash ADC with MUX-Based Decoder

7.4.1 Simulation Results

In Section 6.3 the design of a 6-bit flash ADC with a MUX-based decoder is presented. The decoder consists entirely of a number of 2:1 MUXs, giving a compact and regular structure, which is a benefit when laying out the

	Measurement
Supply voltage	1.2 V
Full-scale voltage	0.5 V
Resolution	6-bit
$f_{s,max}$	470 MHz
SFDR	32.2 dB [a]
Total input capacitance	0.83 pF
Average power consumption	174 mW[b]
FoM	75 pJ[c]
Total chip area	4.1 mm^2
Core area	0.7 mm^2

[a] $f_s = 440$ MHz and $f_{in} = 77$ MHz.
[b] $f_s = 440$ MHz and $f_{in} = 77$ MHz.
[c] $f_s = 440$ MHz, $f_{in} = 77$ MHz, and $P_{avg} = 174$ mW.

Table 7.1: Performance summary of the 6-bit reference ADC.

decoder.

To find the maximum sampling frequency $f_{s,max}$ the ENOB is plotted as a function of the sampling frequency for a 9 MHz 0.5 V full-scale sinusoidal input. The plot is shown in Figure 7.9(a). An analysis of the plot yields a maximum sampling frequency of slightly above 1 GHz. The ENOB at low input frequencies for a sampling frequency of 1 GHz is 5.8 bits. The plotted ENOB is calculated from a sine wave curve fit, according to the method described in Section 3.3.8. In Figure 7.9(b) the simulated ENOB is plotted as a function of the input frequency for a 1 GHz sampling frequency, i.e., close to the maximum sampling frequency. The input is also in this case a full-scale sinusoidal. The test yields an ERBW of 390 MHz.

To illustrate the ADC output spectrum a plot of the simulated output power spectrum at 1 GHz sampling frequency and a 359 MHz full-scale sinusoidal input is shown in Figure 7.10. The plot indicates that the SFDR is 39 dB. Further, the power consumption is 170 mW. Hence the figure of merit in terms of energy per conversion step, defined according to (3.35), is 5.1 pJ.

The simulated ADC performance is summarized in Table 7.2, together with the measurement results. The total input capacitance in the table only considers the parasitic input capacitance of the comparators. Adding

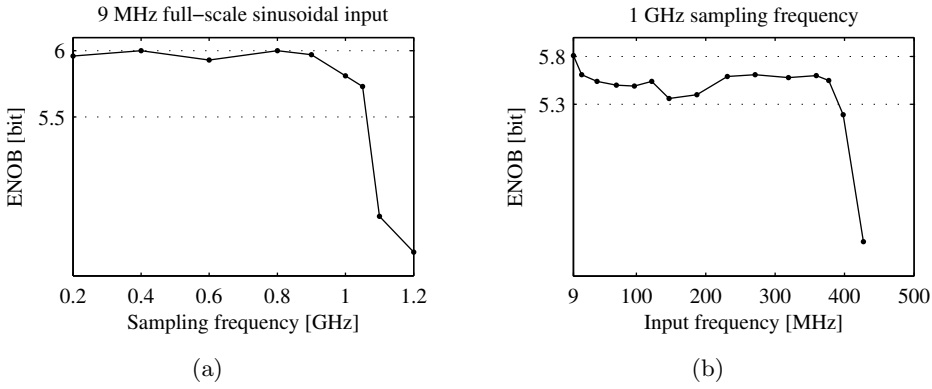


Figure 7.9: Simulated ENOB as a function of (a) the sampling frequency and (b) the input frequency for the flash ADC with MUX-based decoder.

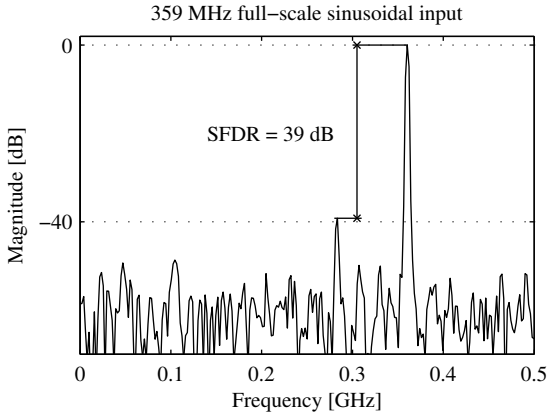


Figure 7.10: Simulated output power spectrum of the flash ADC with MUX-based decoder for a 359 MHz full-scale sinusoidal input at $f_{\mathrm{s,max}}$.

the parasitic capacitance of the input interconnect increases the total input capacitance by about 0.2 pF.

7.4.2 Measurement Results

In this section the measurement results of the static and dynamic characterization of the ADC with MUX-based decoder (MUXADC) is presented. The ADC occupies a total chip area of 2.9 mm^2 and a core area of about 0.4 mm^2 without the decoupling capacitors. A chip photo of the ADC is

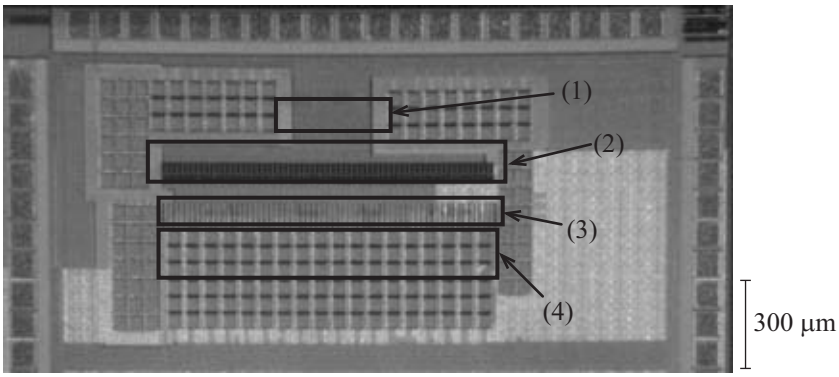


Figure 7.11: Chip photo of the flash ADC with MUX-based thermometer-to-binary decoder. Indicated parts are (1) MUX-based decoder, (2) comparators including the D flip-flops, (3) reference net, and (4) reference net decoupling capacitors.

shown in Figure 7.11, where the different parts are indicated. On the top, indicated by (1), the MUX-based decoder is shown. Below the decoder are the stacked comparators indicated by (2). The reference net and the decoupling capacitors for the reference net are indicated by (3) and (4) respectively. Some of the other capacitors are used for decoupling of the analog power supply, and some are used for decoupling of the digital power supply. In Figure 7.11 the lower half of the chip is missing. The missing part contains the ADC with DEM, which is shown in Figure 7.19.

Static Measurements

The INL and DNL are measured by applying a constant input which is gradually increased, i.e., the same method used as when characterizing the previous ADC. The results of these measurements are depicted in Figure 7.12 for a sampling frequency of 7 MHz.

The offset and gain errors are extracted from the plot of the transfer function in Figure 7.12(a), yielding an offset error of 5.3 LSB and a gain error of −6.5 LSB. The INL and DNL are also calculated from the result shown in Figure 7.12(a). The method used for calculating the INL and DNL from the transfer function is described in Section 3.3.3, and the resulting plots of the INL and DNL are shown in Figure 7.12(b) and Figure 7.12(c), respectively. These figures show that the INL is within 3.2/−2.3 LSB, and the DNL is within 3.0/−1.0 LSB.

To facilitate a comparison of the results of this ADC with the ADC using DEM and the reference ADC, the transfer function together with the

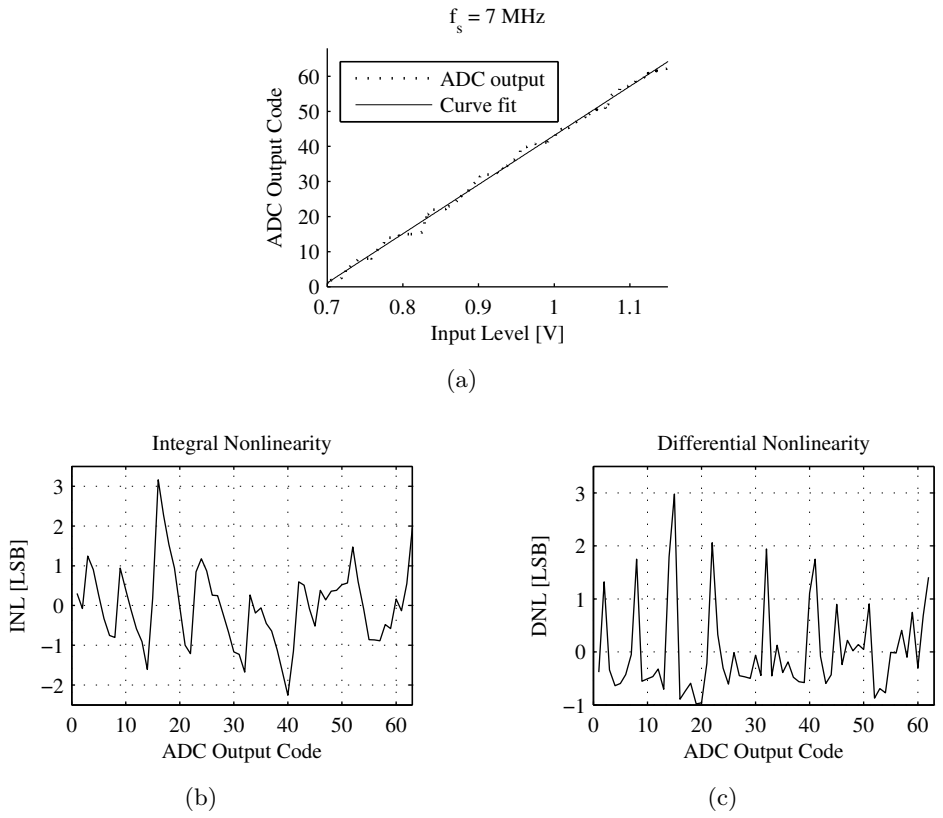


Figure 7.12: In (a) the measured transfer function of the MUXADC for a sampling frequency of 7 MHz is plotted. In (b) and (c) the INL and DNL of the MUXADC is plotted, respectively.

INL and DNL are also plotted when disregarding the three levels closest to the each edge of the reference voltage range. Disregarding the levels closest to each edge yield information of the impact of mismatch at the edges, i.e., the edge effect. The plot is found in Figure 7.13. The offset and gain error, extracted from Figure 7.13(a), now becomes 5.1 LSB and -6.5 LSB, respectively. Hence they are approximately the same as for the case when all reference levels are included. The INL is somewhat better. It is now within $3.0/-2.0$ LSB. Also the DNL is slightly better and is within $2.8/-1.0$ LSB.

For completeness the INL and DNL are also measured using higher sampling frequencies as well, from 7 MHz to 1 GHz. During the measurements of the INL and DNL it is observed that the INL and DNL are dependent on

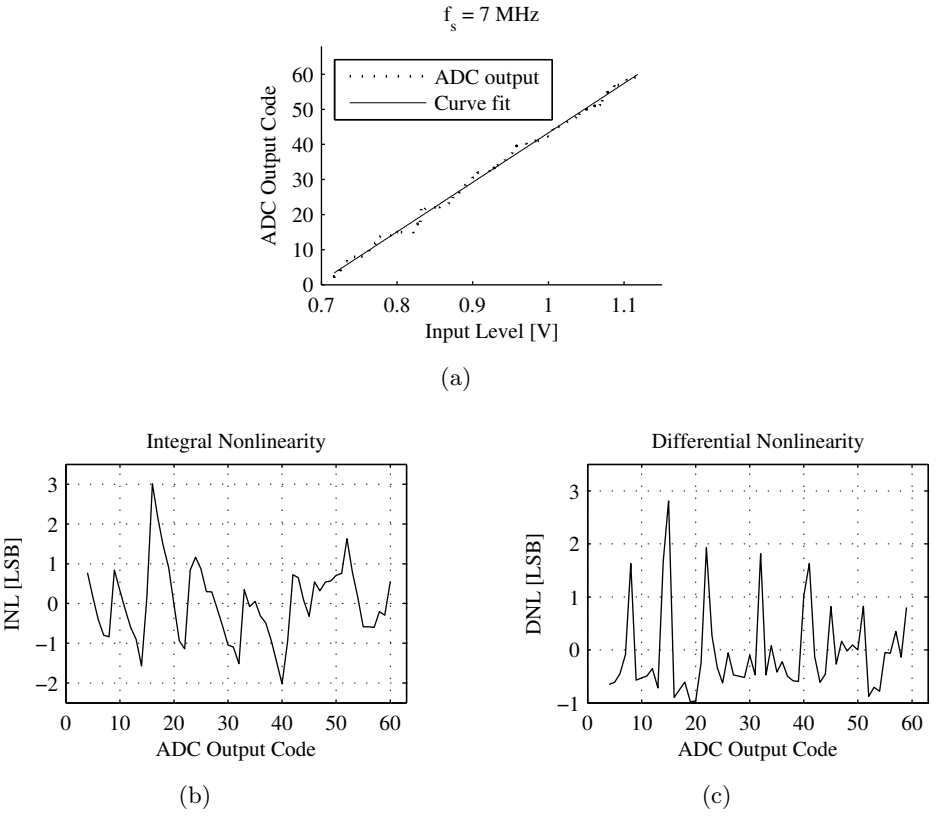


Figure 7.13: In (a) the measured transfer function of the MUXADC for a sampling frequency of 7 MHz is plotted when disregarding the three levels closest to each edge of the reference voltage range. In (b) and (c) the INL and DNL of the MUXADC is plotted, respectively.

the sampling frequency. For sampling frequencies in the range from about 600 MHz to 900 MHz the INL and DNL are degraded compared with sampling frequencies below this range and also degraded compared with when the sampling frequency is 1 GHz.

To investigate the delay through the decoder, the time from when the rising edge of the clock on the clock input to when each output is changing its value is measured. This measurement gives the delay through the input buffer, clock buffer, D-flip-flop, MUX-decoder, and output buffer. The delay for the '0' to '1' transition is measured by applying a 1.2 V input to ensure that all comparator outputs would always be logic one. The input to the D-flip-flops on the output of the comparators is therefore always logic one.

Between each measurement the D-flip-flops are reseted and the reset signal is released before the D-flip-flops are triggered by the clock. Hence the ADC outputs are all zero. When the clock triggers the D-flip-flops on the rising edge their outputs become logic one and the ADC outputs goes from logic zero to logic one. A similar method is used to measure the '1' to '0' transition. The reset signal is instead applied before the clock is triggering the D-flip-flops. Hence the ADC outputs goes from logic one to logic zero. The result of the measurement showed that the delay from the ADC clock input to the ADC outputs is in the range from 2.8 ns to 3.2 ns.

Dynamic Measurements

During the measurements of the dynamic performance the input is a single tone sinusoidal. The output data is saved to a file by the logic analyzer and the data is later evaluated in MATLAB, which resulted in the power spectral plot presented in this chapter.

To find the maximum sampling frequency a low frequency (495 kHz) sinusoidal input is applied to the ADC input and the ADC output data is analyzed for different sampling frequencies. These measurements gave the results shown in Figure 7.14. From Figure 7.14(a) it is estimated that the SNDR at about $f_s = 660$ MHz is 3 dB below the SNDR at low sampling frequencies. Hence the maximum sampling frequency is estimated to 660 MHz at which the SNDR is 23.6 dB. An SNDR of 23.6 dB is equivalent to an ENOB of about 3.6 bit, as seen from Figure 7.14(b).

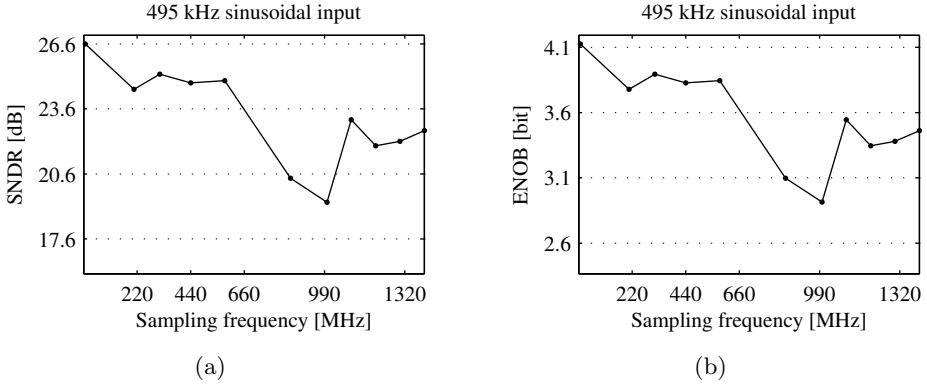


Figure 7.14: The measured (a) SNDR and (b) ENOB of the MUXADC with a sinusoidal input of frequency $f_{in} = 495$ kHz as a function of the sampling frequency.

The ADC is also characterized with respect to SFDR for different input and sampling frequencies. In Figure 7.15(a) the spectrum is plotted for an input frequency of 120 MHz and a sampling frequency of 440 MHz, which yields an SFDR of 29.9 dB. In Figure 7.15(b) the input frequency is 50 MHz and the sampling frequency is 550 MHz, yielding an SFDR of 32.2 dB. The power consumption in the two cases shown in Figure 7.15 are 182 mW, and 168 mW, respectively, excluding the power consumption of the input and output buffers. The power consumption of the analog part is in all three cases 55 mW. The power consumption including the input and output buffers are 271 mW and 266 mW, respectively, for the two cases above. The figure of merit is calculated using (3.35) and the performance extracted from the measurement results presented above. The effective number of bits in the first case, Figure 7.15(a), is 3.7 bit. These numbers yield a figure of merit of 61 pJ. The measurement in Figure 7.15(b) yields an ENOB of 4.2 bit, and a figure of merit of 56 pJ. Hence the figure of merit seems to be around 60 pJ for the ADC. The measurement results of the ADC are summarized in Table 7.2, together with the corresponding simulation results.

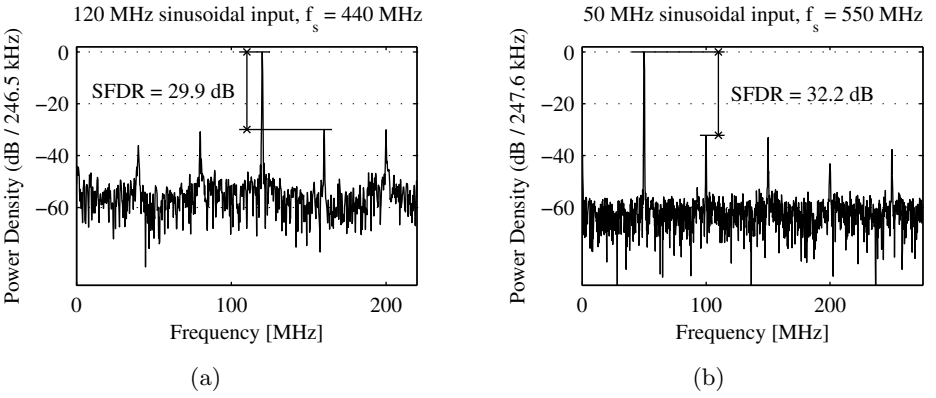


Figure 7.15: The measured SFDR for the MUXADC at (a) $f_{\text{in}} = 120$ MHz and $f_{\text{s}} = 440$ MHz, (b) $f_{\text{in}} = 50$ MHz and $f_{\text{s}} = 550$ MHz.

	Simulation	Measurement
Supply voltage	1.2 V	1.2 V
Full-scale voltage	0.5 V	0.5 V
Resolution	6-bit	6-bit
$f_{s,max}$	1.05 GHz	660 MHz
SFDR	39 dB [a]	32.2 dB [b]
Total input capacitance	0.83 pF	0.83 pF
Average power consumption	170 mW[c]	168 mW[d]
FoM	5.1 pJ	56 pJ
Total chip area	2.9 mm^2	2.9 mm^2
Core area	0.4 mm^2	0.4 mm^2

[a] $f_s = 1$ GHz and $f_{in} = 359$ MHz.
[b] $f_s = 550$ MHz and $f_{in} = 50$ MHz.
[c] $f_s = 1$ GHz and $f_{in} = 359$ MHz.
[d] $f_s = 550$ MHz and $f_{in} = 50$ MHz.

Table 7.2: Performance summary of the 6-bit flash ADC with MUX-based decoder.

7.5 DEM Flash ADC

7.5.1 Simulation Results

In Section 6.4 the design of a 6-bit flash ADC with DEM (DEMADC) is presented. During the evaluation of the ADC with DEM by simulations in Cadence the ADC is allowed to settle for 1.25 µs at start-up before using the data and the input is 90 % of full-scale, i.e., 225 mV amplitude.

The ENOB as a function of the sampling frequency for a low frequency, 9 MHz, sinusoidal input is plotted in Figure 7.16 when the DEM is disabled. From this figure it is seen that the maximum sampling frequency $f_{s,max}$ is above 550 MHz for the ADC. Allowing a longer settling time before using the data indicated an improved ENOB. However, due to the very long simulation time, more than two weeks on a Sun Fire 280R with UltraSPARC III processors, this could not be fully evaluated. Although the ADC is allowed to settle for 1.25 µs at start-up the reference net did not completely settle within this time period. During the circuit simulations, it is observed that increasing the sampling frequency increased the simulation time for the same number of samples. To reduce the simulation time when

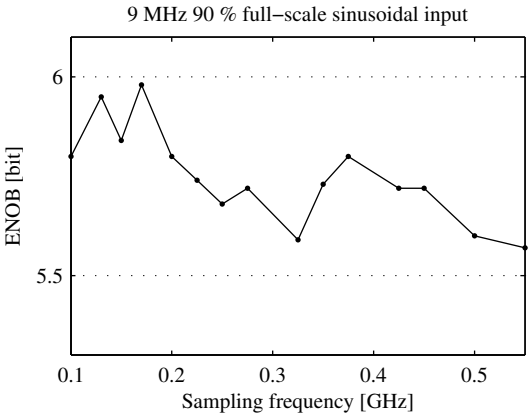


Figure 7.16: Simulated ENOB as a function of the sampling frequency for the DEMADC with a 9 MHz sinusoidal input at 90 % of full-scale with DEM disabled.

simulating the output spectrum the sampling frequency of the ADC with DEM is limited to 130 MHz. Although the number of samples is about 1100, the simulation time still is nearly a month on a Sun Fire 280R with UltraSPARC III processors.

The spectrum with and without DEM are plotted in Figure 7.17 for frequencies up to 65 MHz, i.e., the Nyquist frequency. The resulting data is used without allowing the ADC to settle completely at start-up, resulting in the low-frequency component seen in the plots in Figure 7.17. In addition, the uncertainty in the resistor values is assumed Gaussian distributed with a standard deviation of 10 % in the simulation. The simulated output power spectrum in Figure 7.17(a) yields an SFDR of 39 dB when not using DEM. When DEM is used the SFDR is increased to 45 dB, as shown in Figure 7.17(b). The average power consumption for a 77 MHz 0.5 V full-scale sinusoidal input and a 440 MHz sampling frequency is 92 mW when the DEM circuitry is activated. As mentioned above the number of samples is limited to 1100 in the simulation of the spectrum. The histogram of the position of the zero in the output of the 1-of-126 decoder is shown in Figure 7.18.

The same comparators are used in the design of the flash ADC with DEM as in the design of the flash ADC with MUX-based thermometer-to-binary decoder. Hence the total input capacitance is the same in both designs, excluding the parasitic capacitance of the input interconnect. The simulated and measured performance are summarized in Table 7.3.

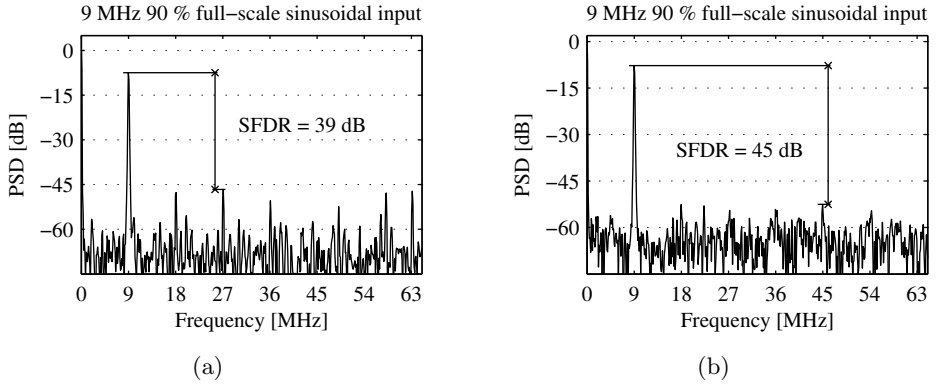


Figure 7.17: Simulated output power spectrum at 130 MHz sampling frequency (a) without DEM and (b) with DEM.

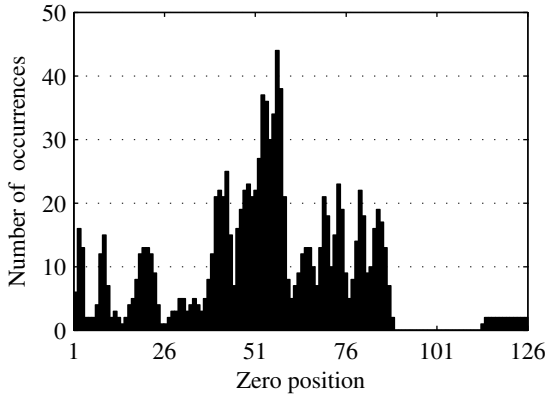


Figure 7.18: Histogram of the position of the zero in the output of the 1-of-126 decoder for the transistor level simulations.

7.5.2 Measurement Results

The flash ADC with DEM has also been evaluated by measurements. The results of these measurements are presented in this section. The ADC occupies a total chip area of 3.9 mm^2, including the pad frame. The core area is 0.9 mm^2, excluding the decoupling capacitors. A chip photo of the ADC is shown inFigure 7.19 where the different parts of the ADC are indicated. In Figure 7.19 the upper half of the chip is missing. The missing part contains the ADC with MUX-based decoder, which is shown in Figure 7.11.

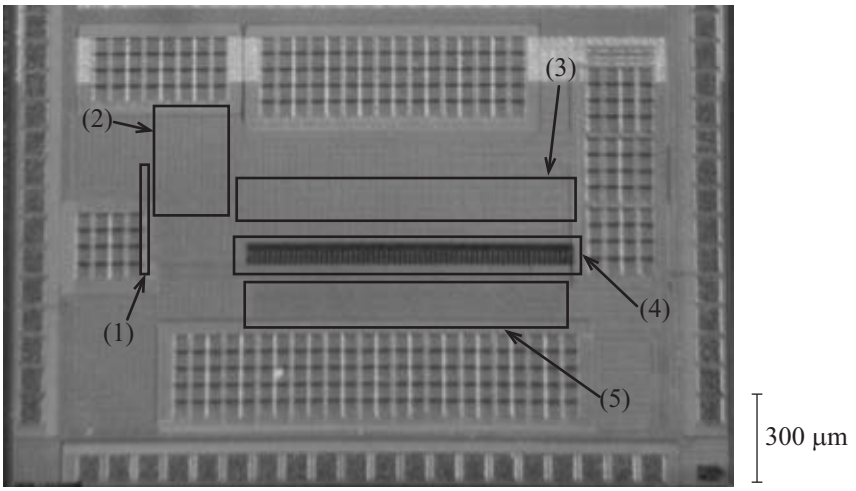


Figure 7.19: Chip photo of the DEMADC. Indicated parts are (1) PRBS, (2) 1-of-126 decoder, (3) reference generator and switches, (4) comparators including the D flip-flops, and (5) ones-counter decoder.

Static Measurements

The INL and the DNL are measured by the same method as for the other two converters. The sampling frequency is 7 MHz during the measurements. As mentioned before, the motivation to the low sampling frequency selection is to minimize the dynamic effects. Hence mainly the static defects of the ADC should be present in its INL and DNL.

During the measurements it is seen that the switches connecting the reference net supplies to the reference net causes a nonlinearity in the ADC transfer function at the edges, i.e., for low and high input levels. The nonlinearity is evident from Figure 7.20, where the transfer function together with the INL and DNL is plotted for the DEMADC with the DEM circuitry activated. Since the DEM circuitry is activated other nonlinearities, e.g., due to matching errors of the comparators and the resistors are averaged out. However, the lowest and highest reference net output are always closest to the switches connecting the reference supply to the reference net. Hence errors in switch resistance and nonlinearities of the switches will always be more significant at the edges. The measurements yield an INL of 2.8/−3.9 LSB, and a DNL of 3.1/−0.5 LSB.

A method to avoid the edge effects is to add more reference levels, and thereby more comparators, but only use the $2^N - 1$ levels in the middle. The method is investigated in Figure 7.21. In this figure the ADC transfer

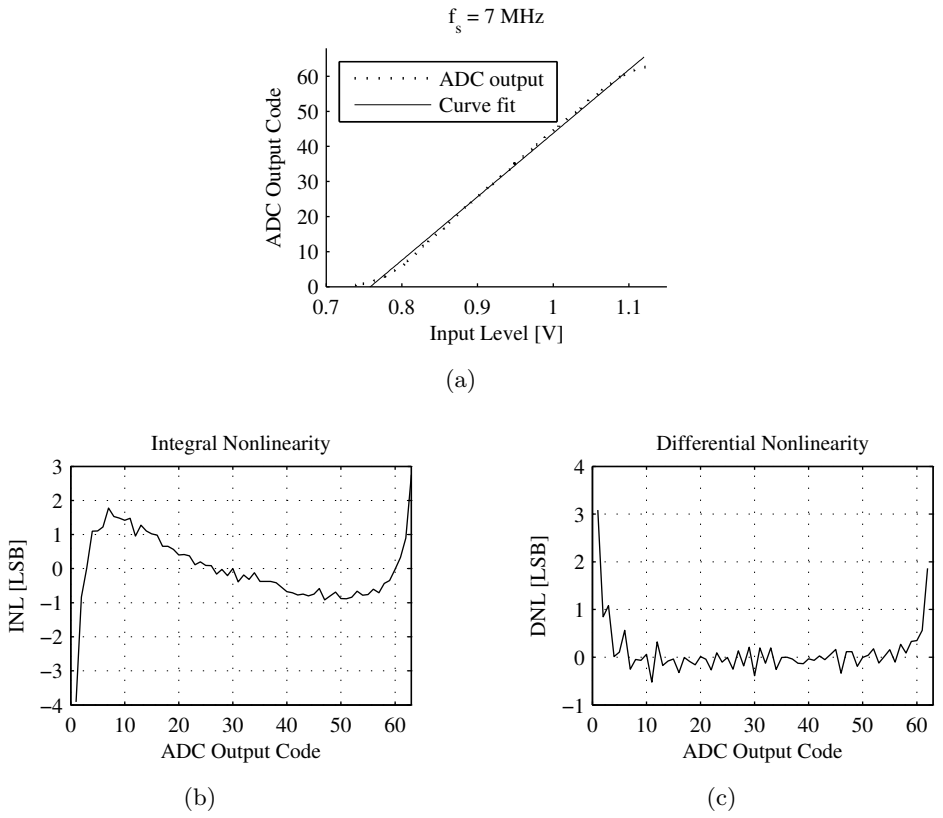


Figure 7.20: Plot of the measured (a) transfer function, (b) INL, and (c) DNL for the DEMADC at $f_s = 7$ MHz with the DEM circuitry activated.

function is plotted together with the INL and DNL, but disregarding the three lowest and the three highest levels. The INL is now within $1/-0.5$ LSB and the DNL is within $0.5/-0.5$ LSB.

To evaluate the effect of applying our dynamic element matching technique with respect to the dynamic performance, the INL and DNL are derived both without DEM and with the DEM circuitry activated. To minimize the edge effects discussed above, the three levels closest to the edges of the reference net are disregarded during the comparison, which can be seen in the INL and DNL plots in Figure 7.22. Further, the sampling frequency is 7 MHz, as before, to minimize the dynamic effects. In Figure 7.22(a) and Figure 7.22(b) the INL and DNL is plotted, respectively, without DEM. This case yields an INL of $1.4/-1.5$ LSB, and a DNL of $1.8/-0.8$ LSB. The INL and DNL using DEM is shown in Figure 7.22(c)

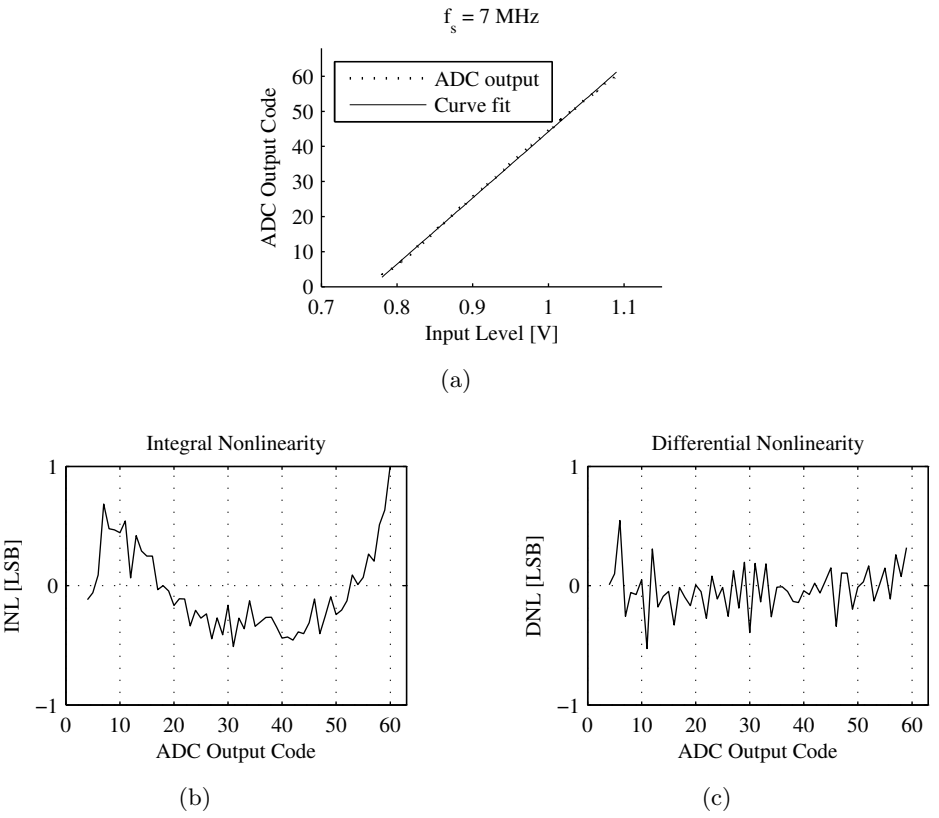


Figure 7.21: Plot of the measured (a) transfer function, (b) INL, and (c) DNL for the DEMADC at $f_s = 7$ MHz with DEM activated, but disregarding the three lowest and three highest levels.

and Figure 7.22(d), respectively. The INL becomes $1/-0.5$ LSB and the DNL becomes $0.5/-0.5$ LSB.

Dynamic Measurements

The SFDR is measured using the same method as in Section 7.4.2. The measurement yields the plots in Figure 7.23 at a sampling frequency of 440 MHz and a sinusoidal single tone input at 77 MHz. In Figure 7.23(a) the spectrum is plotted without DEM, yielding an SFDR of 25.1 dB. Applying DEM improves the SFDR by 1.5 dB to 26.6 dB, as seen from Figure 7.23(b).

The power consumption, excluding the input and output buffers, at the input frequency of 77 MHz is 162 mW without DEM, and 174 mW applying

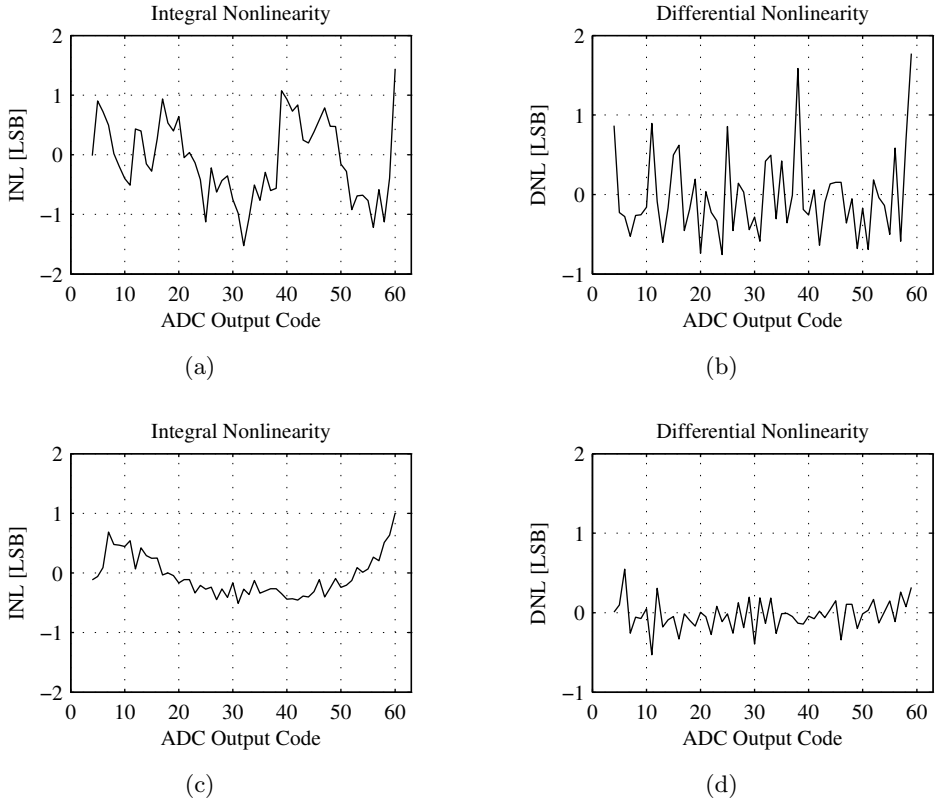


Figure 7.22: Plot of the measured (a) INL and (b) DNL for the DEMADC at $f_s = 7$ MHz without DEM activated, and (c) INL and (d) DNL at $f_s = 7$ MHz with DEM activated.

DEM. This data yield a figure of merit, according to (3.35), of 134 pJ without DEM and 163 pJ with DEM. Including the power consumption of the input and output buffers yields the power consumption 342 mW and 359 mW, respectively.

From the measurements it is also observed that for sampling frequencies above 440 MHz the performance with respect to SFDR is worse when DEM is used. The maximum sampling frequency of this ADC is therefore about 440 MHz. The measurement results are summarized in Table 7.3, together with the simulation results.

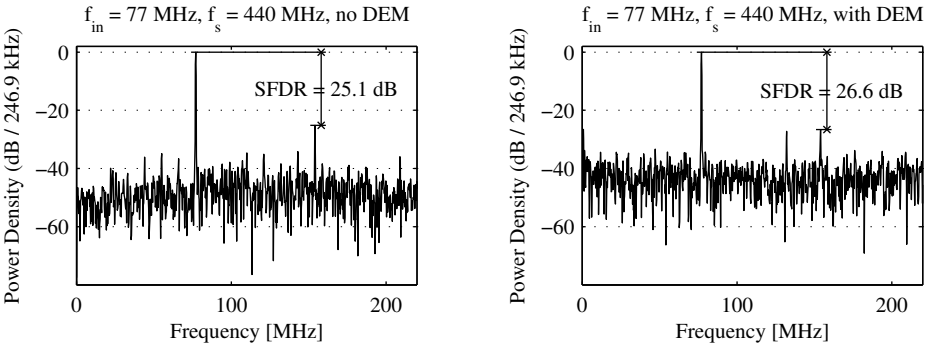


Figure 7.23: The measured SFDR for the DEMADC at $f_s = 440$ MHz and the sinusoidal input frequency $f_{in} = 77$ MHz (a) without DEM and (b) with DEM.

	Simulation	Measurement
Supply voltage	1.2 V	1.2 V
Full-scale voltage	0.5 V	0.5 V
Resolution	6-bit	6-bit
$f_{s,max}$	> 550 MHz	440 MHz
SFDR improvement with DEM	6 dB [a]	1.5 dB [b]
Total input capacitance	0.83 pF	0.83 pF
Average power consumption	92 mW[c]	174 mW[d]
Total chip area	3.9 mm^2	3.9 mm^2
Core area	0.9 mm^2	0.9 mm^2

[a] $f_s = 130$ MHz and $f_{in} = 9$ MHz.
[b] $f_s = 440$ MHz and $f_{in} = 77$ MHz.
[c] $f_s = 440$ MHz, $f_{in} = 77$ MHz with DEM.
[d] $f_s = 440$ MHz, $f_{in} = 77$ MHz with DEM.

Table 7.3: Performance summary of the 6-bit flash ADC with DEM.

Chapter 8

Discussion

The aim of this work is twofold. The first aim is the evaluation of a partially depleted silicon-on-insulator CMOS technology by implementation of three different flash ADCs. The second aim is a study on how to model, design and implement flash ADCs, and evaluation of a few different circuit topologies that are proposed in this work. This chapter starts with a discussion of the SOI CMOS technology in Section 8.1. The discussion is based on the material presented in Chapter 2 and on experiences from the design and implementation of the ADCs in this work. An unfortunate design flaw that are discovered during the evaluation of the ADCs is discussed in Section 8.2. Three 6-bit flash ADCs are presented in this work. In Section 8.3 the reference ADC is discussed. The reference ADC is used as a reference in comparisons. The ADC with MUX-based decoder is discussed in Section 8.4 and the ADC with DEM is discussed in Section 8.5. In Section 8.6 the different implemented ADC topologies are compared and further discussed.

8.1 SOI CMOS Technology

As presented in Chapter 2, the SOI CMOS technology has several advantages, but also several disadvantages over bulk CMOS technologies. This section discusses the benefits and drawbacks of SOI CMOS compared with bulk CMOS, and the differences between the partially depleted and fully depleted SOI CMOS technologies. From this discussion a few conclusions regarding the SOI technology are presented in Chapter 9.

Maybe the most obvious advantage of SOI is the reduced parasitic capacitance, which implies that the devices and circuits can operate at a higher speed. In addition there are some other less obvious advantages, as mentioned in Chapter 2. They are, e.g., a reduced doping density, and improved current drive capability due to a reduced body factor n, which also imply that the DC-gain and unity gain frequency improve. However, all above listed properties are only true for fully depleted SOI CMOS technologies, except for the reduction of parasitic capacitance. The latter is at least also true for partially depleted SOI CMOS technologies with minimum gate lengths larger than 100 nm. As the partially depleted SOI CMOS technology is scaled below 100 nm the advantage diminishes, and is predicted to be almost completely gone when approaching 70 nm, as mentioned in Chapter 2. Hence there seems to be no apparent advantage of using a partially depleted SOI CMOS technology over a bulk CMOS technology for analog circuit design. In addition, considering the adverse kink effect, history effect and the self-heating, the bulk CMOS technology even seems to be a better choice. The first two effects can however be avoided by using body contacts.

Apart of what is discussed above there are still a few advantages of using the partially depleted SOI CMOS technology. Due to the buried insulator and the thin-film structure of the partially depleted SOI CMOS technology the latch-up effect is eliminated and the device density can be higher in a partially depleted SOI CMOS technology compared with a bulk CMOS technology, at least for digital circuits. For analog circuits no general conclusions can be drawn regarding the device density, since other parameters also must be considered during layout, e.g., matching and self-heating. For digital circuits the self-heating is less important, and therefore generally does not impose restrictions on the device density of digital circuits. The exception is parts where close matching of the propagation delays are required, since the matching is affected by temperature variations. Further, the radiation hardness is improved due to the buried insulator, an advantage for radiation hard applications. The radiation hardness reduces the soft error rate of radiation sensitive circuits, e.g., memories. In addition, the crosstalk

is reduced and, e.g., inductors can be implemented having higher Q factor than for bulk CMOS technologies, and the effects of substrate noise can be reduced.

For the fully depleted SOI CMOS technologies the future situation is predicted to be different. The required doping density is lower, and a reduced body factor yields that the DC-gain and unity gain frequency improve, which are important properties when used in, e.g., analog circuits. As for the partially depleted SOI CMOS technology the fully depleted SOI CMOS technology benefit from the elimination of the latch-up effect, improved radiation hardness, reduced crosstalk, and the possibility of designing inductors with higher Q factors than in bulk CMOS technologies. In addition, devices implemented in a fully depleted technology do not suffer from the kink and history effects due to the complete depletion of their bodies. However, the thermal effects are still present in fully depleted SOI, and will be more severe since the thin-film thickness is thinner than for partially depleted SOI. A major obstacle is the difficulty of manufacturing the FD SOI devices, since the thin-film thickness must be controlled accurately to minimize threshold voltage variations over the chip.

Another advantage of the SOI technology is the reduction of the power consumption to about 40 % compared with a bulk CMOS technology implementation, as reported in several other works [15, 59, 64]. Further, application of techniques that reduce the static power consumption yields an even larger benefit of SOI over bulk CMOS. A reduction of the static power consumption of almost 90 % have been reported [59] for a PD SOI technology, compared with the same circuit implemented in a similar bulk CMOS technology and applying the same method for reducing the static power consumption. Since the problem of static power consumption is increasing as the technologies are scaled this is an important reason for why the SOI CMOS technology should be a strong competitor to the bulk CMOS technology in the future. Hence if the thin-film thickness can be accurately controlled and if the thermal effects can be managed in the design flow, the fully depleted SOI CMOS technology seems to be a good candidate for the future mainstream sub 100 nm technologies compared with bulk CMOS technologies.

8.2 Design Errors

As is mentioned in Chapter 7 some of the measurement results deviated much from the values derived by transistor level simulations. A close ex-

amination of the designs eventually revealed a design flaw. A mask layer required for high-precision resistors is unfortunately missing in the layout of the resistors in the reference nets of the manufactured ADCs. The missing mask layer seriously degrades the spread of the nominal resistance value and also the matching between the resistors. Preferably, the ADCs should have been manufactured again, but unfortunately it is not possible since the T206 project of the MEDEA+ program ended shortly after the return of the manufactured ADCs. With the missing mask included the matching is expected to be much improved, which should reduce the nonlinearity of the ADCs. Hence the INL, DNL, SFDR, and SNDR are improved and thereby the figure of merit. The expected improvement is supported by the behavioral level simulation results shown in Figure 5.9 and Figure 5.10.

8.3 Reference ADC

As seen in Figure 7.5(a) there clearly are nonlinearities in the transfer function. The nonlinearities are also evident from the large peaks in the INL and DNL plots in Figure 7.5(b) and Figure 7.5(c), respectively. These nonlinearities are most probable due to matching errors of the resistors in the reference net, and also due to matching errors between the comparators. The same resistors are used in the reference net of the reference ADC, as for the other converters, i.e., with a missing mask layer. This is believed to be the main contributor to the poor static performance. When disregarding the three reference levels closest to the edges of the reference net the INL and DNL is then somewhat improved, as seen in Figure 7.6. The improvement indicates that the matching errors caused by the edge effects also contributes to the nonlinearity.

The poor performance in terms of SNDR, and ENOB, is believed to be due to the poor linearity of the converter, as seen from the static measurement results. The nonlinearities yield too much distortion, i.e., extra tones in the output spectrum, which degrades the SNDR. Hence the errors due to the resistors in the reference net are also visible in the dynamic measurements. In addition, as seen from Figure 7.7 the reference ADC has a reduced SNDR, and ENOB, within a certain frequency range, which limited the maximum sampling frequency to 470 MHz. The performance degradation within the frequency range seen in Figure 7.7 is believed to be due to the propagation delay of the thermometer-to-binary decoder.

The SFDR is expected to be larger than the maximum theoretical SNDR, or equivalent, the number of SFDR-bits is larger than the resolution of the

ADC. For the measurements presented here the SFDR-bits is lower than the resolution of the reference ADC, which is believed to be due to the strongly nonlinear transfer function of the ADC, as seen in Figure 7.5(a). Still, the SFDR is larger than the maximum measured SNDR, which is 26.3 dB.

8.4 Flash ADC with MUX-Based Decoder

In Section 6.3 the design of a 6-bit flash ADC with a MUX-based decoder is presented. The decoder consists entirely of 2:1 MUXs, giving a compact and regular structure, which is shown to be a benefit when doing the layout of the decoder. Other benefits of this decoder, compared with other solutions, are the low hardware cost and the short critical path.

The static measurements revealed that the ADC suffers from poor static performance in terms of INL and DNL. The latter indicated missing codes. The INL and DNL are also measured for higher sampling frequencies. These measurements showed that the INL and DNL are degraded in a frequency range from about 600 MHz to 900 MHz. The degradation is suspected to be due to the propagation delay through the thermometer-to-binary decoder. For sampling frequencies below a certain frequency all outputs have data from the same sample. However as the frequency increases data from different samples can be on the outputs at the same time, yielding large errors. For an increased sampling frequency the delay may be a multiple of the sampling period for certain frequencies, and the outputs will again have data from the same samples, which reduces the errors on the output. This effect is what is believed seen in these measurements. The delay of the ADC from its clock input to its outputs is therefore also measured. The delay is in the range from 2.8 ns to 3.2 ns, which could explain the static performance degradation. Note that little emphasis is made on minimizing the spread during the design. It should thereby be possible to further reduce the propagation delay difference between the decoder outputs. The MUX-based decoder topology should then be able to operate at even higher sampling frequencies than in this work.

The INL and DNL are also derived excluding the three levels closest to each edge of the ADC input range. This yielded a small improvement of the INL and DNL, which shows that they are somewhat degraded by mismatch at the edges, i.e., the edge effects. One method to reduce the edge effects is to add a few extra dummy comparators at each edge. The method improves the matching between the comparators that are used, but is not applied in this work. The same method can be used for the reference

net. The edge effect did not completely explain the poor static performance either. A close examination of the designs eventually revealed the design flaw with a missing mask layer, discussed in Section 8.2.

The static errors yield a nonlinear ADC transfer function. The static errors therefore also affects the dynamic performance. For example, in Figure 7.14 it is seen that the SNDR is degraded in about the same sampling frequency range as the INL and DNL. The propagation delay of the decoder is probably contributing to this degradation. The low maximum SNDR is most likely due to the poor matching in the reference net, which yields a nonlinear transfer function, with, e.g., missing codes. However, the results can still be used to compare the different topologies, but it is not fair to use the results in comparisons with other ADCs. To do that the ADCs in this work should be manufactured again to remove the large errors in the reference nets.

In the design of the comparators the target for the sampling frequency is 2 GHz to obtain some design margin. The maximum sampling frequency is thereby expected to be somewhat higher than the 1 GHz obtained from the simulations. Limitations in either the MUX-based thermometer-to-binary decoder or the latches in the comparators are believed to be the reason for not reaching a maximum sampling frequency of more than 1 GHz when simulating on transistor level.

The measurements of the dynamic performance indicate that the maximum sampling frequency, $f_{\mathrm{s,max}}$, is about 660 MHz. This number is lower than the $f_{\mathrm{s,max}}$ from the simulations. A measure to increase $f_{\mathrm{s,max}}$ is to reduce the delay through the decoder and the whole ADC, i.e., to avoid the performance loss in the sampling frequency range between 600 MHz and about 900 MHz. The maximum SNDR is about 26.6 dB, which is equivalent to an ENOB of 4.1 bit. The SFDR is also characterized and plotted in Figure 7.15. The plot reveal an SFDR of between 29.9 dB and 32.2 dB, which is equivalent to 5.0 and 5.3 SFDR-bits. Hence the SFDR is larger than the SNDR, as expected.

At an input frequency of 50 MHz and a sampling frequency of 550 MHz the power consumption and ENOB is 168 mW and 4.18 bit, respectively. These numbers yield a figure of merit in terms of energy per conversion step of 56 pJ. This number can be compared with the figure of merit derived from the simulations, which is 5.1 pJ. The large difference between the two numbers is once again much due to the static errors, which results in a low ENOB. Another contributor is the fact that $f_{\mathrm{s,max}}$ extracted from the measurements is lower than $f_{\mathrm{s,max}}$ derived from the simulations. As mentioned

above, $f_{s,max}$ should be improved if the delay through the ADC is reduced, or if the ADC outputs are sampled at optimal time instants. Another reason for the higher figure of merit in the simulations is that the power consumption relative to the sampling frequency is higher. The sampling frequency is nearly the double in the simulations, compared with the measurements, and the power consumption is still the same as in the measurement. Some of the extra power consumption in the physical circuit can be explained by glitches that are not visible in the simulations. Another contributor is the power consumption due to the parasitics of the interconnects. In the measurements of the ADC the digital power consumption is about 60 % of the total power consumption, excluding the input and output buffers.

8.5 DEM Flash ADC

In Section 6.4 the design of a 6-bit flash ADC with DEM incorporated in the reference net is presented. The functionality of the designed ADC is evaluated by simulations in Cadence using the foundry provided BSIM3SOI models. The simulations yield that the ADC has an average power consumption of 92 mW for a 77 MHz sinusoidal input and a 440 MHz sampling frequency. The power consumption obtained from the measurement at those frequencies is about 170 mW. The power consumption of the input and output buffers are not included in the two power consumption estimates above, but the DEM circuitry is active in both. The difference between the numbers must be due to effects that are not present in the simulations, e.g., extra power consumption due to interconnect parasitics and glitches. The measured power consumption of the digital part is 75 % of the total, excluding the input and output buffers. The measurements shown in Figure 7.23 had a figure of merit according to (3.35) of about 130 pJ without DEM and 160 pJ with DEM. The poor figure of merit is mostly due to the poor ENOB, which is only about 2.70 bit and 2.50 bit in the respective case.

After designing the DEMADC it is obvious that even the introduction of only two switches in series with the reference net also imposes a major limitation on the maximum input frequency. This result indicates that the solutions in [11, 12] would be even more limited in terms of maximum input frequency. The DEM circuits proposed in [11, 12] would also have a longer settling time since the larger number of switches in the reference net would increase the parasitic capacitance. The larger number of switches would also yield a larger chip area of the circuit.

The simulations indicate that the maximum sampling frequency is above

550 MHz. The maximum sampling frequency estimated by the measurements shows that it is about 440 MHz. The fact that it is lower than the estimate from the simulations is not surprising, since the simulations does not include mismatch and interconnect parasitics. The total chip area of the ADC is 3.9 mm^2 and its core area is 0.9 mm^2.

The behavioral level simulations indicated a 17 dB improvement of the SFDR in the simulations shown in Figure 5.17 and 11 dB in average according to Figure 5.19. The transistor level simulation yields an SFDR improvement of 6 dB according to Figure 7.17. The improvement of the SFDR is expected to be larger if more samples are used, i.e., by increasing the simulation time, since using more samples would further distribute the signal power of the spurious tones over the frequency range. For practical reasons this could not be evaluated by simulation.

The number of samples is limited to 1100 in the simulation of the spectrum, a limitation that yields the histogram of the position of the zero in the output of the 1-of-126 decoder according to Figure 7.18. As seen, several of the positions are never visited, and the histogram differs much from the histogram in Figure 5.18. The 1100 samples includes just above 3 % of the whole PRBS sequence, which is one likely reason to why the SFDR improvement is only 6 dB in the circuit simulations. Another reason may be that more non-ideal behavior of the circuits is causing this effect in transistor level simulation compared with the behavioral level simulations.

The improvement of the SFDR indicated by the measurements is even lower than indicated by the transistor level simulations, only about 1.5 dB. The absolute SFDR values are also lower for the measured ADC than for the simulated ADC. The likely explanation for the difference between the measured and simulated SFDR is first that the reference net suffer from too large mismatch errors and errors in the nominal resistor values due to the missing mask layer. These errors therefore partly explain why the absolute SFDR values are significantly lower. Mismatch on other parts may also contribute. A second cause could be that the time constant of the reference net is too high, i.e., it takes too long for the reference values to settle. For sampling frequencies above 440 MHz the performance with respect to SFDR is worse when DEM is used. The cause is believed to be that the DEM circuitry cannot work at that high sampling frequencies. The main limiting part is probably the reference net, i.e., the charge redistribution in the reference net is not fast enough. The limitations imposed by the DEM circuitry therefore limits the maximum sampling frequency to 440 MHz.

However, the designed and implemented circuit still demonstrates the

working concept of introducing DEM into the reference net of a flash ADC. Further, both the transistor level simulations as well as the measurements verify that the proposed circuit yields an improved SFDR compared to when it is disabled, as expected from the behavioral level simulations. In addition, the static measurements show that the INL and especially the DNL also benefits from using this DEM technique. The measurements also show that the switches connected to the reference net yield large errors at the edges of the ADC input range, which cannot be eliminated by applying DEM. The edge effect could also be a reason for why the SFDR is much lower than expected from the simulations. The above errors do also degrade the SNDR, and thereby also the ENOB, of the converter. Further, the result of the study of the edge effects in Figure 7.21 shows that adding only three extra levels at each edge of the reference net would significantly improve the static performance of the converter.

In future work the design of the reference net and especially the switches connected to it should be investigated in more detail. A study is motivated by two main reasons. First, the fact that the SFDR improvement is not as large as expected. Second, the result from the static measurements, which indicates that the switches yield a large static error, even when DEM is applied.

Another drawback with introducing switches into the reference net became evident during the simulations. When the switches are added a settling time larger than 1.25 μs is imposed at start-up of the circuit. The incomplete settling is believed to be the reason for the reduction of the ENOB for low frequencies seen in Figure 7.16.

8.6 ADC Comparison

Disregarding the three levels closest to the edges of the input range of the reference ADC, it is seen that the INL and DNL are improved less as for the DEMADC. The smaller improvement of INL and DNL shows that the nonlinearity and resistance error of the switches in the DEMADC reference net is a larger contributor to the overall static performance degradation than the edge effects. However, when disregarding the three levels closest to the edges, the DEMADC with the DEM circuitry activated has significantly better static performance compared with the reference ADC. Note also that the voltage step equivalent to one LSB is 5.6 mV for the DEMADC, but it is 7.4 mV for the reference ADC. The smaller voltage step for the DEMADC even further shows that the DEMADC with DEM activated gives a

significant improvement of the static performance.

The frequency range where the performance degradation occurs for the reference ADC starts at a lower frequency (470 MHz) than for the ADC with MUX-based decoder (600 MHz). Hence this indicate that the propagation delay of the ones-counter decoder is longer than for the MUX-based decoder. Further, the performance degradation is larger for the ones-counter, which can be motivated by noting that for the MUX-based decoder the outputs having higher significance level pass through fewer MUXs than the outputs having lower significance levels. For example, the MSB output does not pass through any MUX at all, but before the correct LSB output is delivered the signal must pass through five levels of MUXs. The outputs with higher significance level will therefore not suffer as much from the propagation delay as the outputs with lower significance level. Hence the performance degradation will slowly become worse as the frequency increases. More and more of the outputs will thereby have the wrong output, starting with the LSB output. For the ones-counter decoder the situation is different. The propagation delay through this decoder is more balanced, e.g., the MSB output will be dependent on outputs of lower significance level. Hence the performance degradation is worse for the ones-counter decoder, which is evident by studying the slopes of the curves in Figure 7.14 and Figure 7.7. This observation shows one of the benefits of the MUX-based decoder over the ones-counter decoder.

The performance in terms of SFDR of the reference ADC is about the same as for the ADC with MUX-based thermometer-to-binary decoder. Further, the core area of the ADC with MUX-based decoder is about 40 % smaller than for the reference ADC, which is entirely due to the smaller area of the MUX-based thermometer-to-binary decoder. However, the figure of merit is somewhat higher for the reference ADC, 87 pJ compared with 61 pJ for the ADC with MUX-based decoder, at $f_s = 440$ MHz and $f_{in} = 120$ MHz. The lower figure of merit shows that the MUX-based decoder is more efficient in terms of power consumption and performance than the ones-counter decoder. The measurements also show that they both have about the same power consumption, which is a bit surprising since the hardware cost, estimated in Table 4.1, is much lower for the MUX-based decoder, but could be explained by a difference in glitches. However, better efficiency for the ADC with MUX-based decoder and a small chip area makes it interesting for future designs.

Worth noting here is that according to the behavioral level simulation results in Section 5.4 the ones-counter decoder will always have the same

or better performance in terms of ENOB, compared with the MUX-based decoder. The difference is however not large, which is seen in Figure 5.14. In summary, the measurements show that most of the poor static performance is due to mismatch, but also that some is due to the propagation delay of the decoder.

Regarding the ADC with DEM it is more than twice as large as the ADC with MUX-based decoder, and about 30 % larger than the reference ADC, which uses the same thermometer-to-binary decoder as the DEMADC. The chip area comparison show that the DEM circuitry impose approximately a 30 % larger chip area, which has to be considered when deciding if this approach should be used.

Chapter 9

Conclusions

9.1 The SOI CMOS Technology

The main advantages of the SOI CMOS technology over bulk CMOS technology is the elimination of the latch-up effect, increased device density, reduced soft-error rate of circuits implemented in SOI CMOS, reduced crosstalk, which reduces substrate noise, an improved quality factor Q of inductors, and reduced gate leakage. The partially depleted SOI CMOS technology is however predicted to show little advantage in speed over the bulk CMOS technology as the technologies are scaled below 100 nm gate length. Fully depleted SOI CMOS technology, on the other hand, has several advantages even unscaled. It requires a lower doping density and has lower body factor, which improves the DC gain and unity gain frequency of the devices. Further, it does not suffer from the kink and history effects. The effect of the self-heating and the difficulty of manufacturing must however be solved. If this is solved the fully depleted SOI CMOS technology is a promising contender as a future mainstream technology. This conclusion is further strengthened when considering that the leakage power consumption is significantly reduced when using SOI CMOS instead of bulk CMOS.

As the technologies are scaled the leakage power becomes more important. Hence the smaller leakage power consumption of the SOI CMOS technology might in the future be the strongest motivator for using the SOI CMOS technology instead of the bulk CMOS technology.

9.2 The ADCs

Behavioral level models of flash ADCs are presented. The models are used to facilitate the top-down design methodology. MATLAB simulations of these models yield that the thermometer-to-binary decoder will affect the overall ADC performance, e.g., limit the SNDR. Further, these models gave insight and aided the design phase. The models are also used to explore the potential SFDR improvement of applying DEM in flash ADCs.

The implementation of three 6-bit flash ADCs is presented. One is used as a reference, one has a MUX-based decoder and the last is a flash ADC with DEM. The layout is done in a 130 nm partially depleted SOI CMOS technology. The ADCs are manufactured. Hence the ADC results presented in this thesis are both based on measurements and on simulations in Cadence using the foundry provided BSIM3SOI models for Eldo. The measurement results are however much degraded due to an unfortunate design flaw regarding the resistors in the reference nets of the converters. A mask layer is missing, which affects the accuracy of the resistor values. Hence the static and dynamic performance of the ADCs are adversely affected. The static performance could however be somewhat improved by adding three dummy comparators on each edge of the ADC input range, i.e., reducing the edge effects.

The measurements show that the MUX-based thermometer-to-binary decoder is more sensitive to bubble errors, but it can operate at a higher sampling frequency than the ones-counter decoder. Further, the MUX-based decoder is more efficient in terms of power consumption and has about 40 % smaller chip area than the ones-counter decoder. The spread of the propagation delay of the separate outputs of the MUX-based decoder is limiting its maximum speed. Hence finding ways to reduce the spread would make the MUX-based decoder seem interesting for future designs.

The dynamic measurements of the reference ADC show that it has a maximum sampling frequency of 470 MHz, SNDR of at most 26.3 dB, and an SFDR between 29 to 35 dB. The SNDR and SFDR are comparable to the SNDR and SFDR of the ADC with MUX-based decoder. However, the ADC with MUX-based decoder had a maximum sampling frequency of

660 MHz.

Regarding the ADC with DEM, this work demonstrates that DEM can be introduced into the reference net of a flash ADC. Further, simulations and measurements show that applying DEM improves the SFDR compared with when the DEM circuits are disabled. In addition, the measurements also indicate an improvement of the static performance when applying DEM compared with when it is disabled. The improvements comes to the cost of a larger chip area. In addition, the simulation and measurement results show that the current implementation of DEM increases the power consumption and reduces the maximum sampling frequency. Further, the introduction of the switches impose a reference net settling time at start-up, and increases the total reference net resistance. The latter will reduce the maximum input frequency. Some of the performance degradation can however be explained by the missing mask layer for the poly-silicon resistors in the reference net. Hence at this moment it is still an open question if the presented DEM technique is a viable approach. However, in future work a redesign of, in the first place, the switches could improve the performance to such degree that using this DEM technique would be motivated.

9.3 Suggestions For Future Work

This section lists some suggestions for future work related to the presented ADCs and to the evaluation of the SOI CMOS technology. First of all, the ADCs ought to be manufactured again with the missing mask layer included. This would enable a more fair evaluation of their true performance.

The design of the MUX-based decoder should be studied in more detail, especially how to reduce the spread between the propagation delay of its individual outputs. If in addition its overall propagation delay could be reduced it would also increase its maximum frequency of operation. Pipelining could also be used to enhance the performance.

The sizing of the MOSFET switches in the reference net of the ADC with DEM should be investigated in more detail. The goal should be to find a good trade-off between the start-up settling time of the reference net, the maximum input frequency, and the maximum sampling frequency by proper sizing of the switches. This study would then reveal how much performance degradation the DEM circuitry causes, which would reveal the feasibility region of this approach.

Further studies of the performance improvement of using SOI CMOS technology in analog design should also be performed. This can be accom-

plished by design of common analog building blocks in both the partially depleted SOI CMOS technology, as well as in the bulk CMOS technology that the partially depleted SOI CMOS technology is based on. The performance of the designed circuits could then serve as a benchmark of the partially depleted SOI CMOS technology compared with the bulk CMOS technology.

In the future, the implementation of analog circuits in fully depleted SOI CMOS technologies should be investigated to validate the expected good properties.

References

[1] G. R. Aiello, "Challenges for ultra-wideband (UWB) CMOS integration," in *Proceedings of IEEE International Microwave Symposium Digest*, 2003, pp. 361–364.

[2] A. G. Aipperspach, D. H. Allen, D. T. Cox, N. V. Phan, and S. N. Storino, "A 0.2-μm, 1.8-V, SOI, 550-MHz, 64-b PowerPC microprocessor with copper interconnects," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 11, pp. 1430–1435, Nov. 1999.

[3] S. Ardalan and M. Sachdev, "An overview of substrate noise reduction techniques," in *Proceedings of International Symposium on Quality Electronic Design*, 2004, pp. 291–296.

[4] M. Badaroglu, S. Donnay, H. J. De Man, Y. A. Zinzius, G. G. E. Gielen, W. Sansen, T. Fondén, and S. Signell, "Modeling and experimental verification of substrate noise generation in a 220-kgates WLAN system-on-chip with multiple supplies," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1250–1260, July 2003.

[5] M. Badaroglu, P. Wambacq, G. Van der Plas, S. Donnay, G. G. E. Gielen, and H. J. De Man, "Evolution of substrate noise generation mechanisms with CMOS technology scaling," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 53, no. 2, pp. 296–305, Feb. 2006.

[6] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[7] K. Bernstein, C.-T. Chuang, R. Joshi, and R. Puri, "Design and CAD challenges in sub-90nm CMOS technoligies," in *Proceedings of International Conference on Computer Aided Design*, Nov. 2003, pp. 129–136.

[8] J. Blair, "Histogram measurement of ADC nonlinearities using sine waves," in *IEEE Transactions on Instrumentation and Measurement*, vol. 43, no. 3, June 1994, pp. 373–383.

[9] J. Briaire and K. S. Krisch, "Principles of substrate crosstalk generation in CMOS circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 6, pp. 645–653, June 2000.

[10] S. Brigati, V. Liberali, and F. Maloberti, "Precision behavioural modelling of circuit components for data converters," in *Proceedings of IEE Advanced A/D and D/A Conversion Techniques and their Applications*, July 1994, pp. 110–115.

[11] M. Caciotta, P. Carbone, and V. O. Cencelli, "Design and characterization of a stochastic-flash ADC," in *Proceedings of IEEE Instrumentation and Measurement Technology Conference*, vol. 1, May 1998, pp. 92–95.

[12] P. Carbone and M. Caciotta, "Stochastic-flash analog-to-digital conversion," *IEEE Transactions on Instrumentation and Measurement*, vol. 47, no. 1, pp. 65–68, Feb. 1998.

[13] D. Chang, J. G. Fossum, S. K. Reynolds, and M. M. Pelella, "Kink-free analog circuit design with floating-body NFD/SOI CMOS: A current-steering D-A converter," in *Proceedings of IEEE International SOI Conference*, Oct. 1997, pp. 158–159.

[14] D. Chang, J. G. Fossum, S. K. Reynolds, and M. M. Pelella, "Kink-free SOI analog circuit design with floating-body/NFD MOSFET's," *IEEE Electron Device Letters*, vol. 18, no. 12, pp. 602–605, Dec. 1997.

[15] L. Chang, Y.-K. Choi, J. Kedzierski, N. Lindert, P. Xuan, J. Bokor, C. Hu, and T.-J. King, "Moore's law lives on," *IEEE Circuits and Devices Magazine*, vol. 19, no. 1, pp. 35–42, Jan. 2003.

[16] L. Chang, K. J. Yang, Y.-C. Yeo, I. Polishchuk, T.-J. King, and C. Hu, "Direct-tunneling gate leakage current in double-gate and ultrathin

body MOSFETs," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2288–2295, Dec. 2002.

[17] M. Choi and A. A. Abidi, "A 6-b 1.3-Gsamples/s A/D converter in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1847–1858, Dec. 2001.

[18] J.-P. Colinge, "Thin-film SOI technology: The solution to many submicron CMOS problems," in *Proceedings of the International Electron Devices Meeting*, 1989, pp. 817–820.

[19] J.-P. Colinge, "Fully-depleted SOI CMOS for analog applications," *IEEE Transactions on Electron Devices*, vol. 45, no. 5, pp. 1010–1016, May 1998.

[20] J.-P. Colinge, "SOI devices and circuits," in *Proceedings of International Conference on Microelectronics*, vol. 2, 2000, pp. 407–414.

[21] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 3rd ed. Kluwer Academics Publishers, 2004.

[22] E. Compagne, J. Sevenhans, and C. Raynaud, "A GSM receiver base band in 0.25μ, 1.8V fully depleted SOI including a 4^{th} order serial $\Sigma\Delta$ A/D converter," in *Proceedings of European Solid-State Circuits Conference*, Sept. 2001, pp. 551–554.

[23] J. Compiet, P. de Jong, P. Wambacq, G. Vandersteen, S. Donnay, M. Engels, and I. Bolsens, "High-level modeling of a high-speed flash A/D converter formixed-signal simulations of digital telecommunication front-ends," in *Proceedings of Southwest Symposium on Mixed-Signal Design*, Feb. 2000, pp. 135–140.

[24] M. De Wilde, W. Meeus, P. Rombouts, and J. Van Campenhout, "A simple on-chip repetitive sampling setup for the quantification of substrate noise," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1062–1072, May 2006.

[25] J. Doernberg, H.-S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," in *IEEE Journal of Solid-State Circuits*, vol. 19, no. 6, Dec. 1984, pp. 820–827.

[26] P. G. Drennan and C. C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 450–456, Mar. 2003.

[27] C. F. Edwards, W. Redman-White, M. Bracey, B. M. Tenbroek, M. S. L. Lee, and M. J. Uren, "A multibit ΣΔ modulator in floating-body SOS/SOI CMOS for extreme radiation environments," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 937–948, July 1999.

[28] J.-P. Eggermont, D. Flandre, J.-P. Raskin, and J.-P. Colinge, "Potential and modeling of 1-μm SOI CMOS operational transconductance amplifiers for applications up to 1 GHz," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 640–643, Apr. 1998.

[29] D. Eggert, P. Huebler, A. Huerrich, H. Kueck, W. Budde, and M. Vorwerk, "A SOI-RF-CMOS technology on high resistivity SIMOX substrates for microwave applications to 5 GHz," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 1981–1989, Nov. 1997.

[30] M. N. Ericson, J. M. Rochelle, M. Bobrek, C. L. Britton, A. Bobrek, B. J. Blalock, R. Schulz, and J. A. Moore, "2^{nd}- and 4^{th}-order ΣΔ modulators fabricated in 3.3 V 0.5μm SOS-CMOS for high-temperature applications," in *Proceedings of IEEE International SOI Conference*, Oct. 2002, pp. 75–77.

[31] P. M. Figueiredo and J. C. Vital, "Low kickback noise techniques for CMOS latched comparators," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 1, May 2004, pp. 537–540.

[32] D. Flandre, J.-P. Eggermont, D. De Ceuster, and P. G. A. Jespers, "Comparison of SOI versus bulk performances of CMOS micropower single-stage OTAs," *Electronics Letters*, vol. 30, no. 23, pp. 1933–1934, Nov. 1994.

[33] D. Flandre, B. Gentinne, J.-P. Eggermont, and P. G. A. Jespers, "Design of thin-film fully-depleted SOI CMOS analog circuits significantly outperforming bulk implementations," in *Proceedings of IEEE International SOI Conference*, Oct. 1994, pp. 99–100.

[34] E. Fogleman and I. Galton, "A dynamic element matching technique for reduced-distortion multibit quantization in delta-sigma ADC's," *IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing*, vol. 48, no. 2, pp. 158–170, Feb. 2001.

[35] K. Fowler, "Part 7: Analog-to-digital conversion in real-time systems," *IEEE Instrumentation and Measurement Magazine*, pp. 58–64, Sept. 2003.

[36] B. J. Frohring, B. E. Peetz, M. A. Unkrich, and S. C. Bird, "Waveform recorder design for dynamic performance," *Hewlet-Packard Journal*, vol. 39, pp. 39–47, Feb. 1988.

[37] G. Geelen, "A 6b 1.1GS/s CMOS A/D converter," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2001, pp. 128–129, 438.

[38] D. Goldman, K. DeGregorio, C. S. Kim, M. Nielson, J. Zahurak, and S. Parke, "0.15um SOI DRAM technology incorporating sub-volt dynamic threshold devices for embedded mixed-signal & RF circuits," in *Proceedings of IEEE International SOI Conference*, Oct. 2001, pp. 97–98.

[39] G. Gomez and B. Haroun, "A 1.5V 2.4/2.9mW 79/50dB DR $\Sigma\Delta$ modulator for GSM/WCDMA in a 0.13µm digital process," in *Proceedings of IEEE International Solid-State Circuits Conference*, vol. 1, 2002, pp. 306–307, 468.

[40] N. Gray, *ABCs of ADCs: Analog-to-Digital Converter Basics*, 2nd ed., National Semiconductor Corporation, Aug. 2004.

[41] D. Greenlaw, G. Burbach, T. Feudel, F. Feustel, K. Frohberg, F. Graetsch, G. Grasshoff, C. Hartig, T. Heller, K. Hempel, M. Horstmann, P. Huebler, R. Kirsch, S. Kruegel, E. Langer, A. Pawlowitsch, H. Ruelke, H. Schuehrer, R. Stephan, A. Wei, T. Werner, K. Wieczorek, and M. Raab, "Taking SOI substrates and low-k dielectrics into high-volume microprocessor production," in *Proceedings of the International Electron Devices Meeting*, 2003, pp. 277–280.

[42] M. Gustavsson, J. J. Wikner, and N. N. Tan, *CMOS Data Converters for Communications*. Kluwer Academics Publishers, 2000.

[43] F. Hameau and O. Rozeau, "Radio-frequency circuits integration using CMOS SOI 0.25µm technology," in *RFIC Design Workshop*, Mar. 2002.

[44] A. A. Hamoui and K. W. Martin, "High-order multibit modulators and paeudo data-weighted-averaging in low-oversampling ADCs for broad-band applications," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 51, no. 1, pp. 72–85, Jan. 2004.

[45] M. J. Hargrove, S. Voldman, R. Gauthier, J. Brown, K. Duncan, and W. Craig, "Latchup in CMOS technology," in *Proceedings of IEEE International Reliability Physics Symposium*, Mar. 1998, pp. 269–278.

[46] S. Hazenboom, T. S. Fiez, and K. Mayaram, "A comparison of substrate noise coupling in lightly and heavily doped CMOS processes for 2.4-GHz LNAs," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 3, pp. 574–587, Mar. 2006.

[47] K. Hejn and A. Pacut, "Effective resolution of analog to digital converters," *IEEE Instrumentation and Measurement Magazine*, pp. 48–55, Sept. 2003.

[48] Y. Hiraoka, S. Matsumoto, and T. Sakai, "New substrate-crosstalk reduction structure using SOI substrate," in *Proceedings of IEEE International SOI Conference*, Oct. 2001, pp. 107–108.

[49] D. Hisamoto, "FD/DG-SOI MOSFET," in *Proceedings of the International Electron Devices Meeting*, Dec. 2001, pp. 19.3.1–19.3.4.

[50] IEEE 802.15 WPAN high rate alternative PHY task group 3a (TG3a). IEEE. [Online]. Available: http://www.ieee802.org/15/pub/TG3a.html

[51] D. A. Johns and K. W. Martin, *Analog Integrated Circuit Design*, 1st ed. John Wiley & Sons Inc., 1997.

[52] F. Kaess, R. Kanan, B. Hochet, and M. Declercq, "New encoding scheme for high-speed flash ADC's," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 1, June 1997, pp. 5–8.

[53] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 2nd ed. McGraw-Hill Book Co, 1999.

[54] W. Kester, "Designer's guide to flash-ADC testing—part 2: DSP test techniques keep flash ADCs in check," Analog Devices application note 215B, Tech. Rep., 1990.

[55] H.-C. Kim, D.-K. Jeong, and W. Kim, "A 30mW 8b 200Msamples/s pipelined CMOS ADC using a switched-opamp technique," in *Proceedings of IEEE International Solid-State Circuits Conference*, 2005, pp. 284–285, 598.

[56] J. B. Kuo and S.-C. Lin, *Low-Voltage SOI CMOS VLSI Devices and Circuits*. John Wiley & Sons Inc., Sept. 2001.

[57] M. S. L. Lee, B. M. Tenbroek, W. Redman-White, J. Benson, and M. J. Uren, "A physically based compact model of partially depleted SOI MOSFETs for analog circuit simulation," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 1, pp. 110–121, Jan. 2001.

[58] B. H. Leung and S. Sutarja, "Multibit Σ–Δ A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing*, vol. 39, no. 1, pp. 35–51, Jan. 1992.

[59] N. L'Hostis, O. Thomas, S. Haendler, A. Amara, P. Flatresse, and M. Belleville, "Silicon characterization of standby leakage reduction techniques in a 0.13µm low power partially-depleted silicon-on-insulator technology," in *Proceedings of IEEE International Conference on Integrated Circuit Design and Technology*, May 2006, pp. 1–4.

[60] J. H.-C. Lin and B. Haroun, "An embedded 0.8 V/480 µW 6B/22 MHz flash ADC in 0.13-µm digital CMOS process using a nonlinear double interpolation technique," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1610–1617, Dec. 2002.

[61] S. Maeda, Y. Wada, K. Yamamoto, H. Komurasaki, T. Matsumoto, Y. Hirano, T. Iwamatsu, Y. Yamaguchi, T. Ipposhi, K. Ueda, K. Mashiko, S. Maegawa, and M. Inuishi, "Impact of 0.18µm SOI CMOS technology using hybrid trench isolation with high resistivity substrate on embedded RF/analog applications," in *Proceedings of Symposium on VLSI Technology*, June 2000, pp. 154–155.

[62] H. M. Manasevit and W. I. Simpson, "Single-crystal silicon on a sapphire substrate," *Journal of Applied Physics*, vol. 35, no. 4, pp. 1349–1351, Apr. 1964.

[63] C. W. Mangelsdorf, "A 400-MHz input flash converter with error correction," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 184–191, Feb. 1990.

[64] A. Marshall and S. Natarajan, "PD-SOI and FD-SOI: A comparison of circuit performance," in *Proceedings of IEEE International Conference on Electronics, Circuits and Systems*, Sept. 2002, pp. 25–28.

[65] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-rate CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 318–325, Mar. 2000.

[66] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 8, pp. 847–854, Aug. 1995.

[67] T. Ndjountche, F.-L. Luo, and C. Bobda, "A CMOS front-end architecture for hard-disk drive read-channel equalizer," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 3, May 2005, pp. 2184–2187.

[68] P. P. Newaskar, R. Blazquez, and A. P. Chandrakasan, "A/D precision requirements for an ultra-wideband radio receiver," in *Proceedings of IEEE Workshop on Signal Processing Systems*, Oct. 2002, pp. 270–275.

[69] N. Ohkubo, M. Suzuki, T. Shinbo, T. Yamanaka, A. Shimizu, K. Sasaki, and Y. Nakagome, "A 4.4 ns CMOS 54 x 54-b multiplier using pass-transistor multiplexer," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 251–257, Mar. 1995.

[70] S. Park and M. P. Flynn, "Design techniques for high performance CMOS flash analog-to-digital converters," in *Proceedings of European Conference on Circuit Theory and Design*, Aug. 2005.

[71] Y.-I. Park, S. Karthikeyan, W. M. Koe, Z. Jiang, and T.-C. Tan, "A 16-bit, 5 MHz multi-bit sigma-delta ADC using adaptively randomized DWA," in *Proceedings of IEEE Custom Integrated Circuits Conference*, Sept. 2003, pp. 115–118.

[72] M. M. Pelella and J. G. Fossum, "On the performance advantage of PD/SOI CMOS with floating bodies," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 96–104, Jan. 2002.

[73] P. Pereira, J. R. Fernandes, and M. M. Silva, "Wallace tree encoding in folding and interpolation ADCs," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 1, May 2002, pp. 509–512.

[74] C. S. Petrie and J. A. Connelly, "A noise-based IC random number generator for applications in cryptography," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 47, no. 5, pp. 615–621, May 2000.

[75] J.-O. Plouchart, "SOI nano-technology for high-performance system on-chip applications," in *Proceedings of IEEE International SOI Conference*, Sept. 2003, pp. 1–4.

[76] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Transactions on Electron Devices*, vol. 44, no. 2, pp. 2252–2261, Dec. 1997.

[77] R. Reedy, J. Cable, and D. Kelly, "Single chip wireless systems using SOI," in *Proceedings of IEEE International SOI Conference*, Oct. 1999, pp. 8–11.

[78] R. Reedy, J. Cable, D. Kelly, M. Stuber, F. Wright, and G. Wu, "UTSi CMOS: A complete RF SOI solution," in *Analog Integrated Circuits and Signal Processing*. Springer Science+Business Media B.V., Nov. 2000, vol. 25, no. 2, pp. 171–179.

[79] P. Rombouts and L. Weyten, "Dynamic element matching for pipelined A/D conversion," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 2, Sept. 1998, pp. 315–318.

[80] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," in *Proceedings of the IEEE*, vol. 91, no. 2, Feb. 2003, pp. 305–327.

[81] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6bit, 1.2GSps low-power flash-adc in 0.13µm digital CMOS," in *Proceedings of European Solid-State Circuits Conference*, Sept. 2004, pp. 339–342.

[82] P. C. S. Scholtens and M. Vertregt, "A 6-b 1.6-Gsamples/s flash ADC in 0.18-µm CMOS using averaging termination," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1599–1609, Dec. 2002.

[83] G. G. Shahidi, "SOI technology for the GHz era," *IBM Journal of Research and Development*, vol. 46, no. 2, pp. 121–131, Mar. 2002.

[84] N. Shibata, M. Watanabe, Y. Sato, T. Ishihara, and Y. Komine, "A 2-V 300-MHz 1-Mb current-sensed double-density SRAM for low-power 0.3-μm CMOS/SIMOX ASICs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1524–1537, Oct. 2001.

[85] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g_m/i_d based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sept. 1996.

[86] P. Simonen, A. Heinonen, M. Kuulusa, and J. Nurmi, "Comparison of bulk and SOI CMOS technologies in a DSP processor circuit implementation," in *Proceedings of International Conference on Microelectronics*, Oct. 2001, pp. 107–110.

[87] D. Sinitsky, S. Tang, A. Jangity, F. Assaderaghi, G. G. Shahidi, and C. Hu, "Simulation of SOI devices and circuits using BSIM3SOI," *IEEE Electron Device Letters*, vol. 19, no. 9, pp. 323–325, Sept. 1998.

[88] J. G. Spooner. (2001, Mar.) IBM touts chipmaking technology. [Online]. Available: http://news.com.com/IBM+touts+chipmaking+technology/2100-1001_3-254983.html

[89] P. Stubberud and J. W. Bruce, "An analysis of flash dynamic element matching analog to digital converters," in *Proceedings of IEEE Midwest Symposium on Circuits and Systems*, vol. 2, Aug. 2000, pp. 684–687.

[90] E. Säll, K. O. Andersson, and M. Vesterbacka, "A dynamic element matching technique for flash analog-to-digital converters," in *Proceedings of Nordic Signal Processing Symposium*, June 2004, pp. 137–140.

[91] E. Säll and M. Vesterbacka, "Design of a comparator in CMOS SOI," in *Proceedings of IEEE International Workshop on System-on-Chip for Real-Time Applications*, July 2004, pp. 229–232.

[92] E. Säll and M. Vesterbacka, "A multiplexer based decoder for flash analog-to-digital converters," in *Proceedings of TENCON*, Nov. 2004.

[93] E. Säll and M. Vesterbacka, "Silicon-on-insulator CMOS technology for system-on-chip," in *Proceedings of Swedish System-on-Chip Conference*, Apr. 2004.

[94] E. Säll and M. Vesterbacka, "6 bit 1 GHz CMOS silicon-on-insulator flash analog-to-digital converter for read channel applications," in *Proceedings of European Conference on Circuit Theory and Design*, Aug. 2005.

[95] E. Säll and M. Vesterbacka, "Comparison of two thermometer-to-binary decoders for high-performance flash ADCs," in *Proceedings of IEEE Norchip Conference*, Nov. 2005.

[96] E. Säll and M. Vesterbacka, "Design and evaluation of a comparator in CMOS SOI," in *Proceedings of RadioVetenskap och Kommunikation (RVK)*, June 2005.

[97] E. Säll and M. Vesterbacka, "Mixed signal design in SOI CMOS technology," in *Proceedings of Swedish System-on-Chip Conference*, Apr. 2005.

[98] E. Säll and M. Vesterbacka, "6-bit flash ADC with dynamic element matching," in *Proceedings of IEEE Norchip Conference*, vol. 1, Nov. 2006, pp. 159–162.

[99] E. Säll, M. Vesterbacka, and K. O. Andersson, "A study of digital decoders in flash analog-to-digital converters," in *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 1, May 2004, pp. 129–132.

[100] Y. Tan, M. Kumar, J. K. O. Sin, L. Shi, and J. Lau, "A 900-MHz fully integrated SOI power amplifier for single-chip wireless transceiver applications," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1481–1486, Oct. 2000.

[101] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, R. J. T. Bunyan, and M. J. Uren, "Impact of self-heating and thermal coupling on analog circuits in SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 1037–1046, July 1998.

[102] J. Terada, Y. Matsuya, S. Mutoh, and Y. Kado, "A 1-V cyclic ADC using FD-SOI sample/hold circuits for sensor networks," in *Proceedings of IEEE International SOI Conference*, Oct. 2002, pp. 126–127.

[103] C. Tinella, J. M. Fournier, D. Belot, and V. Knopik, "A high-performance CMOS-SOI antenna switch for the 2.5-5-GHz band," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1279–1283, July 2003.

[104] K. Uyttenhove, A. Marques, and M. Steyaert, "A 6-bit 1 GHz acquisition speed CMOS flash ADC with digital error correction," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 2000, pp. 249–252.

[105] K. Uyttenhove and M. Steyaert, "A CMOS 6-bit, 1 GHz ADC for IF sampling applications," in *Proceedings of IEEE International Microwave Symposium Digest*, vol. 3, 2001, pp. 2131–2134.

[106] K. Uyttenhove and M. Steyaert, "A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1115–1122, July 2003.

[107] O. Valorge, C. Andrei, F. Calmon, J. Verdier, C. Gontrand, and P. Dautriche, "A simple way for substrate noise modeling in mixed-signal ICs," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 53, no. 10, pp. 2167–2177, Oct. 2006.

[108] R. J. van de Plassche, *Integrated analog-to-digital and digital-to-analog converters*. Kluwer Academics Publishers, 1994.

[109] M. van Heijningen, J. Compiet, P. Wambacq, S. Donnay, M. G. E. Engels, and I. Bolsens, "Analysis and experimental verification of digital substrate noise generation for epi-type substrates," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1002–1008, July 2000.

[110] M. Vanden Bossche, J. Schoukens, and J. Renneboog, "Dynamic testing and diagnostics of A/D converters," in *IEEE Transactions on Circuits and Systems*, vol. 33, no. 8, Aug. 1986, pp. 775–785.

[111] J. Vandenbussche, K. Uyttenhove, E. Lauwers, M. Steyaert, and G. Gielen, "Systematic design of a 200 MS/s 8-bit interpolating/averaging A/D converter," in *Proceedings of Design Automation Conference*, June 2002, pp. 449–454.

[112] A. G. W. Venes and R. J. van de Plassche, "An 80-MHz, 80-mW, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1846–1853, Dec. 1996.

[113] A. Viviani, J.-P. Raskin, D. Flandre, J.-P. Colinge, and D. Vanhoenacker, "Extended study of crosstalk in SOI-SIMOX substrates," in

Proceedings of the International Electron Devices Meeting, Dec. 1995, pp. 713–716.

[114] S. Voldman, D. Hui, L. Warriner, D. Young, J. Howard, F. Assaderaghi, and G. G. Shahidi, "Electrostatic discharge (ESD) protection in silicon-on-insulator (SOI) CMOS technology with aluminum and copper interconnects in advanced microprocessor semiconductor chips," in *Proceedings of Electrical Overstress/Electrostatic Discharge Symposium*, Sept. 1999, pp. 105–115.

[115] S. Voldman, R. Schulz, J. Howard, V. Gross, S. Wu, A. Yapsir, D. Sadana, H. Hovel, J. Walker, F. Assaderaghi, B. Chen, J. Y.-C. Sun, and G. G. Shahidi, "CMOS-on-SOI ESD protection networks," in *Proceedings of Electrical Overstress/Electrostatic Discharge Symposium*, 1996, pp. 291–301.

[116] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

[117] R. H. Walden, "Performance trends for analog-to-digital converters," *IEEE Communications Magazine*, pp. 96–101, Feb. 1999.

[118] C. S. Wallace, "A suggestion for a fast multiplier," *IEEE Transactions on Electronic Computers*, pp. 14–17, Feb. 1964.

[119] A. Wei, M. J. Sherony, and D. A. Antoniadis, "Transient behavior of the kink effect in partially-depleted SOI MOSFET's," *IEEE Electron Device Letters*, vol. 16, no. 11, pp. 494–496, Nov. 1995.

[120] W.-K. Yeh, S.-M. Chen, and Y.-K. Fang, "Substrate noise-coupling characterization and efficient suppression in CMOS technology," *IEEE Transactions on Electron Devices*, vol. 51, no. 5, pp. 817–819, May 2004.

[121] S.-M. Yoo, T.-H. Oh, J.-W. Moon, S.-H. Lee, and U.-K. Moon, "A 2.5V 10b 120 MSample/s CMOS pipelined ADC with high SFDR," in *Proceedings of IEEE Custom Integrated Circuits Conference*, 2002, pp. 441–444.

[122] J. Yu and F. Maloberti, "A low-power multi-bit $\Delta\Sigma$ modulator in 90nm digital CMOS without DEM," in *Proceedings of IEEE International Solid-State Circuits Conference*, vol. 1, Feb. 2005, pp. 168–169, 591.