Intel® 64 and IA-32 Architectures Software Developer Manuals

Updated December 29, 2016 Translate

These manuals describe the architecture and programming environment of the Intel® 64 and IA-32 architectures.

Electronic versions of these documents allow you to quickly get to the information you need and print only the pages you want. The Intel® 64 and IA-32 architectures software developer's manuals are now available for download via one combined volume, a four volume set or a ten volume set. All content is identical in each set; **see details below**.

At present, downloadable PDFs of all volumes are at version 062. The downloadable PDF of the Intel® 64 and IA-32 architectures optimization reference manual is at version 035. Additional related specifications, application notes, and white papers are also available for download.

Note: If you would like to be notified of updates to the Intel® 64 and IA-32 architectures software developer's manuals, you may utilize a third-party service, such as http://www.changedetection.com (http://www.changedetection.com) to be notified of changes to this page (please reference 1 below).

Note: We are no longer offering the Intel® 64 and IA-32 architectures software developer's manuals on CD-ROM. Hard copy versions of the manual are available for purchase via a print-on-demand fulfillment model through a third-party vendor, Lulu (please reference 1 and 2 below):http://www.lulu.com/spotlight/IntelSDM (http://www.lulu.com/spotlight/IntelSDM).

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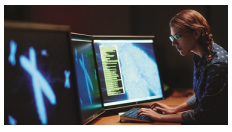


Combined Volume Set of Intel® 64 and IA-32 Architectures Software Developer's Manuals

Document	Description
Intel® 64 and IA-32 architectures software developer's manual combined volumes: 1, 2A, 2B, 2C, 2D, 3A, 3B, 3C, 3D, and 4 (/sites/default/files/managed/39/c5/325462-sdm-vol-1-2abcd-3abcd.pdf)	This document contains the following: **Volume 1:** Describes the architecture and programming environment of processors supporting IA-32 and Intel® 64 architectures. **Volume 2:** Includes the full instruction set reference, A-Z. Describes the format of the instruction and provides reference pages for instructions. **Volume 3:** Includes the full system programming guide, parts

Document	Description
	1, 2, 3, and 4. Describes the operating-system support environment of Intel® 64 and IA-32 architectures, including: memory management, protection, task management, interrupt and exception handling, multi-processor support, thermal and power management features, debugging, performance monitoring, system management mode, virtual machine extensions (VMX) instructions, Intel® Virtualization Technology (Intel® VT), and Intel® Software Guard Extensions (Intel® SGX). **Volume 4:** Describes the model-specific registers of processors supporting IA-32 and Intel® 64 architectures.
Intel® 64 and IA-32 architectures software developer's manual documentation changes (/sites/default/files/managed/3e/79/252046-sdm-change-document.pdf)	Describes bug fixes made to the Intel® 64 and IA-32 architectures software developer's manual between versions. **NOTE:** This change document applies to all Intel® 64 and IA-32 architectures software developer's manual sets (combined volume set, 4 volume set, and 10 volume set).

Four-Volume Set of Intel® 64 and IA-32 Architectures Software Developer's Manuals

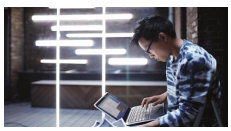
This set consists of volume 1, volume 2 (combined 2A, 2B, 2C, and 2D), volume 3 (combined 3A, 3B, 3C, and 3D), and volume 4. This set allows for easier navigation of the instruction set reference and system programming guide through functional cross-volume table of contents, references, and index.

Document	Description
Intel® 64 and IA-32 architectures software developer's manual volume 1: Basic architecture (/sites/default/files/managed/a4/60/253665-sdm-vol-1.pdf)	Describes the architecture and programming environment of processors supporting IA-32 and Intel® 64 architectures.
Intel® 64 and IA-32 architectures software developer's manual combined volumes 2A, 2B, 2C, and 2D: Instruction set reference, A-Z (/sites/default/files/managed/a4/60/325383-sdm-vol-2abcd.pdf)	This document contains the full instruction set reference, A-Z, in one volume. Describes the format of the instruction and provides reference pages for instructions. This document allows for easy navigation of the instruction set reference through functional cross-volume table of contents, references, and index.
Intel® 64 and IA-32 architectures software developer's manual combined volumes 3A, 3B, 3C, and 3D: System programming guide (/sites/default/files/managed/a4/60/325384-sdm-vol-3abcd.pdf)	This document contains the full system programming guide, parts 1, 2, 3, and 4, in one volume. Describes the operating-system support environment of Intel® 64 and IA-32 architectures, including: Memory management, protection, task management, interrupt and exception handling, multi-processor support, thermal and power management features, debugging, performance monitoring, system management mode, virtual machine extensions (VMX) instructions, Intel® Virtualization Technology (Intel® VT), and Intel® Software Guard Extensions (Intel® SGX). This document allows for easy navigation of the system programming guide through functional cross-volume table of contents, references, and index.
Intel® 64 and IA-32 architectures software developer's manual volume 4: Model-specific registers (/sites/default/files/managed/22/0d/335592-sdm-vol-4.pdf)	Describes the model-specific registers of processors supporting IA-32 and Intel® 64 architectures.

Ten-Volume Set of Intel® 64 and IA-32 Architectures Software Developer's Manuals

This set contains the same information as the four-volume set, but separated into ten smaller PDFs: volume 1, volume 2A, volume 2B, volume 2C, volume 2D, volume 3A, volume 3B, volume 3C, volume 3D, and volume 4. This set is better suited to those with slower connection speeds.

Document	Description
Intel® 64 and IA-32 architectures software developer's manual volume 1: Basic architecture (/sites/default/files/managed/a4/60/253665-sdm-vol-1.pdf)	Describes the architecture and programming environment of processors supporting IA-32 and Intel® 64 architectures.
Intel® 64 and IA-32 architectures software developer's manual volume 2A: Instruction set reference, A-L (/sites/default/files/managed/ad/01/253666-sdm-vol-2a.pdf)	Describes the format of the instruction and provides reference pages for instructions (from A to L). This volume also contains the table of contents for volumes 2A, 2B, 2C, and 2D.
Intel® 64 and IA-32 architectures software developer's manual volume 2B: Instruction set reference, M-U (/sites/default/files/managed/7c/f1/253667-sdm-vol-2b.pdf)	Provides reference pages for instructions (from M to U).
Intel® 64 and IA-32 architectures software developer's manual volume 2C: Instruction set reference, V-Z (/sites/default/files/managed/7c/f1/326018-sdm-vol-2c.pdf)	Provides reference pages for instructions (from V to Z).
Intel® 64 and IA-32 architectures software developer's manual volume 2D: Instruction set reference (/sites/default/files/managed/7c/f1/334569-sdm-vol-2d.pdf)	Includes the safer mode extensions reference. This volume also contains the appendices and index support for volumes 2A, 2B, 2C, and 2D.
Intel® 64 and IA-32 architectures software developer's manual volume 3A: System programming guide, part 1 (/sites/default/files/managed/7c/f1/253668-sdm-vol-3a.pdf)	Describes the operating-system support environment of an IA-32 and Intel® 64 architectures, including: memory management, protection, task management, interrupt and exception handling, and multi-processor support. This volume also contains the table of contents for volumes 3A, 3B, 3C and 3D.
Intel® 64 and IA-32 architectures software developer's manual volume 3B: System programming guide, part 2 (/sites/default/files/managed/7c/f1/253669-sdm-vol-3b.pdf)	Continues the coverage on system programming subjects begun in volume 3A. Volume 3B covers thermal and power management features, debugging, and performance monitoring.
Intel® 64 and IA-32 architectures software developer's manual volume 3C: System programming guide, part 3 (/sites/default/files/managed/7c/f1/326019-sdm-vol-3c.pdf)	Continues the coverage on system programming subjects begun in volume 3A and volume 3B. Volume 3C covers system management mode, virtual machine extensions (VMX) instructions, and Intel® Virtualization Technology (Intel® VT).
Intel® 64 and IA-32 architectures software developer's manual volume 3D: System programming guide, part 4 (/sites/default/files/managed/7c/f1/332831-sdm-vol-3d.pdf)	Volume 3D covers system programming with Intel® Software Guard Extensions (Intel® SGX). This volume also contains the appendices and indexing support for volumes 3A, 3B, 3C, and 3D.
Intel® 64 and IA-32 architectures software developer's manual volume 4: Model-specific registers (/sites/default/files/managed/22/0d/335592-sdm-vol-4.pdf)	Describes the model-specific registers of processors supporting IA-32 and Intel® 64 architectures.



Software Optimization Reference Manual

Document	Description
Intel® 64 and IA-32 architectures optimization reference manual (/sites/default/files/managed/9e/bc/64-ia-32-architectures-optimization-manual.pdf)	Intel® 64 and IA-32 architectures optimization reference manual provides information on Intel® Core™ processors, NetBurst microarchitecture, and other recent Intel® microarchitectures. It describes code optimization techniques to enable you to tune your application for highly optimized results when run on Intel® Atom™, Intel® Core™ i7, Intel® Core™, Intel® Core™2 Duo, Intel® Core™ Duo, Intel® Xeon®, Intel® Pentium® 4, and Intel® Pentium® M processors.

Related Specifications, Application Notes, and White Papers

Document	Description
Intel® architecture instruction set extensions programming reference (/sites/default/files/managed/c5/15/architecture-instruction-set-extensions-programming-reference.pdf)	This document covers new instructions slated for future Intel® processors.
5-Level Paging and 5-Level EPT white paper (/sites/default/files/managed/2b/80/5-level_paging_white_paper.pdf)	This document describes planned extensions to the Intel 64 architecture to expand the size of addresses that can be translated through a processor's memory-translation hardware.
Timestamp-Counter Scaling for Virtualization (/sites/default/files/managed/c5/15/timestamp-counter-scaling-virtualization-white-paper.pdf)	This paper describes an Intel® Virtualization Technology (Intel® VT) enhancement for future Intel® processors. This feature, referred to as timestamp-counter scaling (TSC scaling), further extends the capability of virtual-machine monitor (VMM) software that employs the TSC-offsetting mechanism by allowing that software finer control over the value of the timestamp counter (TSC) read during guest virtual machine (VM) execution.
Intel® 64 architecture x2APIC specification (/sites/default/files/managed/c5/15/64-architecture-x2apic-specification.pdf)	Extensions to the xAPIC architecture are intended primarily to increase processor addressability. The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendability for future Intel platform innovations.
Intel® 64 and IA-32 architectures application note TLBs, paging-structure caches, and their invalidation	The information contained in this application note is now part of Intel® 64 and IA-32 architectures software developer's manual volumes 3A and 3B.
Intel® carry-less multiplication instruction and its usage for computing the GCM mode white paper (/sites/default/files/managed/af/98/carry-less-multiplication-instruction.pdf)	This paper provides information on the instruction, and its usage for computing the Galois Hash. It also provides code examples for the usage of PCLMULQDQ, together with the Intel® AES New Instructions (Intel® AES-NI) for efficient implementation of AES in Galois Counter Mode (AES-GCM).
Intel® 64 architecture memory ordering white paper	This document has been merged into Volume 3A of Intel® 64 and IA-32 architectures software developer's manual.
Performance monitoring unit sharing guide (/sites/default/files/managed/c5/15/performance-monitoring-unit-sharing-guide.pdf)	This paper provides a set of guidelines between multiple software agents sharing the PMU hardware on Intel® processors.
Intel® Virtualization Technology FlexMigration (Intel® VT FlexMigration) application note (/sites/default/files/managed/c5/15/virtualization-technology-flexmigration-application-note.pdf)	This application note discusses virtualization capabilities in Intel® processors that support Intel® VT FlexMigration usages.
Intel® Virtualization Technology for Directed I/O architecture specification (/sites/default/files/managed/c5/15/vt-directed-io-spec.pdf)	This document describes the Intel® Virtualization Technology for Directed I/O.
Page Modification Logging for Virtual Machine Monitor white paper (/sites/default/files/managed/c5/15/page-modification-logging-vmm-white-paper.pdf)	This paper describes an Intel® Virtualization Technology (Intel® VT) enhancement for future Intel® processors.
Secure Access of Performance Monitoring Unit by User Space Profilers (/sites/default/files/managed/c5/15/secure-access-performance-monitoring-unit-paper.pdf)	This paper proposes a software mechanism targeting performance profilers which would run at user space privilege to access performance monitoring hardware. The latter requires privileged access in kernel mode, in a secure manner without causing unintended interference to the software stack.

For more complete information about compiler optimizations, see our Optimization Notice (/en-us/articles/optimization-notice#opt-en).

Comments (3)

Matthias H. (Intel) said on Wed, 02/22/2017 - 00:34

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English

could you pls add a "last updated" or "version" information for the various docs on this page - maybe also some notes what has been added from version to version?

al helal said on Tue, 12/13/2016 - 05:12

Thanks. I have found the index in the 'Combined Volume Set of Intel® 64 and IA-32 Architectures Software Developer's Manuals'

al helal said on Tue, 12/13/2016 - 01:40

If there is a combined index file for all volume then students can be benefited.

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