Bert Serneels
Michiel Steyaert

ACSP
Analog Circuits And Signal Processing

Design of High Voltage xDSL Line Drivers in Standard CMOS

Springer

DESIGN OF HIGH VOLTAGE XDSL LINE DRIVERS IN STANDARD CMOS

ANALOG CIRCUITS AND SIGNAL PROCESSING SERIES

Consulting Editor: Mohammed Ismail. *Ohio State University*

Titles in Series:

ULTRA LOW POWER CAPACITIVE SENSOR INTERFACES
Bracke, W., Puers, R. (et al.)
ISBN: 978-1-4020-6231-5

BROADBAND OPTO-ELECTRICAL RECEIVERS IN STANDARD CMOS
Hermans, C., Steyaert, M.
ISBN: 978-1-4020-6221-6

CMOS MULTICHANNEL SINGLE-CHIP RECEIVERS FOR MULTI-GIGABIT OPTICAL DATA COMMUNICATIONS
Muller, P., Leblebici, Y.
ISBN: 978-1-4020-5911-7

SWITCHED-CAPACITOR TECHNIQUES FOR HIGH-ACCURACY FILTER AND ADC...
Quinn, P.J., Roermund, A.H.M.v.
ISBN: 978-14020-6257-5

LOW-FREQUENCY NOISE IN ADVANCED MOS DEVICES
von Haartman, M., Östling, M.
ISBN: 978-1-4020-5909-4

CMOS SINGLE CHIP FAST FREQUENCY HOPPING SYNTHESIZERS FOR WIRELESS MULTI-GIGAHERTZ APPLICATIONS
Bourdi, Taoufik, Kale, Izzet
ISBN: 978-1-4020-5927-8

ANALOG CIRCUIT DESIGN TECHNIQUES AT 0.5V
Chatterjee, S., Kinget, P., Tsividis, Y., Pun, K.P.
ISBN-10: 0-387-69953-8

IQ CALIBRATION TECHNIQUES FOR CMOS RADIO TRANCEIVERS
Chen, Sao-Jie, Hsieh, Yong-Hsiang
ISBN-10: 1-4020-5082-8

FULL-CHIP NANOMETER ROUTING TECHNIQUES
Ho, Tsung-Yi, Chang, Yao-Wen, Chen, Sao-Jie
ISBN: 978-1-4020-6194-3

THE GM//ID DESIGN METHODOLOGY FOR CMOS ANALOG LOW POWER INTEGRATED CIRCUITS
Jespers, Paul G.A.
ISBN-10: 0-387-47100-6

PRECISION TEMPERATURE SENSORS IN CMOS TECHNOLOGY
Pertijs, Michiel A.P., Huijsing, Johan H.
ISBN-10: 1-4020-5257-X

CMOS CURRENT-MODE CIRCUITS FOR DATA COMMUNICATIONS
Yuan, Fei
ISBN: 0-387-29758-8

RF POWER AMPLIFIERS FOR MOBILE COMMUNICATIONS
Reynaert, Patrick, Steyaert, Michiel
ISBN: 1-4020-5116-6

ADVANCED DESIGN TECHNIQUES FOR RF POWER AMPLIFIERS
Rudiakova, A.N., Krizhanovski, V.
ISBN: 1-4020-4638-3

CMOS CASCADE SIGMA-DELTA MODULATORS FOR SENSORS AND TELECOM
del Río, R., Medeiro, F., Pérez-Verdú, B., de la Rosa, J.M., Rodríguez-Vázquez, A.
ISBN: 1-4020-4775-4

SIGMA DELTA A/D CONVERSION FOR SIGNAL CONDITIONING
Philips, K., van Roermund, A.H.M.
Vol. 874, ISBN: 1-4020-4679-0

CALIBRATION TECHNIQUES IN NYQUIST A/D CONVERTERS
van der Ploeg, H., Nauta, B.
Vol. 873, ISBN: 1-4020-4634-0

ADAPTIVE TECHNIQUES FOR MIXED SIGNAL SYSTEM ON CHIP
Fayed, A., Ismail, M.
Vol. 872, ISBN: 0-387-32154-3

WIDE-BANDWIDTH HIGH-DYNAMIC RANGE D/A CONVERTERS
Doris, Konstantinos, van Roermund, Arthur, Leenaerts, Domine
Vol. 871, ISBN: 0-387-30415-0

METHODOLOGY FOR THE DIGITAL CALIBRATION OF ANALOG CIRCUITS AND SYSTEMS: WITH CASE STUDIES
Pastre, Marc, Kayal, Maher
Vol. 870, ISBN: 1-4020-4252-3

HIGH-SPEED PHOTODIODES IN STANDARD CMOS TECHNOLOGY
Radovanovic, Sasa, Annema, Anne-Johan, Nauta, Bram
Vol. 869, ISBN: 0-387-28591-1

Design of High Voltage xDSL Line Drivers in Standard CMOS

By

BERT SERNEELS
KU Leuven, Belgium

and

MICHIEL STEYAERT
KU Leuven, Belgium

Springer

A C.I.P. Catalogue record for this book is available from the Library of Congress.

ISBN 978-1-4020-6789-1 (HB)
ISBN 978-1-4020-6790-7 (e-book)

Published by Springer,
P.O. Box 17, 3300 AA Dordrecht, The Netherlands.

www.springer.com

Printed on acid-free paper

Preface

TODAY, the worldwide DSL market penetration has surpassed all other forms of broadband access technologies. However, still less than 5% of the world's phone lines are connected to DSL networks. At over 173 million DSL subscribers, as of September 2006, the majority of the world remains thus "unconnected". The opportunity of DSL is to reuse the billions of available twisted pairs of the classical plain old telephone service (POTS) to offer a triple play of high-speed Internet, voice over IP (VOIP) and multichannel television to your home.

The Discrete MultiTone (DMT) modulation was developed to provide bit-rates close to the Shannon limit for the lossy transmission medium. In this modulation technique, the used bandwidth is divided into several carriers, spaced at 4.3125 kHz. Each carrier is modulated by a quadrature amplitude modulation. A large disadvantage of this technique is the high Crest Factor (CF) of the signals in the time domain, requiring linear amplifiers for a broad range of input signal amplitudes. This results in line drivers with very low efficiencies.

It is known that the Self-Oscillating Power Amplifier (SOPA) is a highly efficient line driver for xDSL applications. However, in the nano-electronic era, the line driver remains more than ever the major bottleneck for lowering the cost and power of the xDSL modem. The low supply voltages coming from nanometer technologies increase the current density in the line driver for a constant output power. This results in a low efficiency and reliability problems.

To solve these low voltage issues, high voltage design techniques are discussed in this book using the principle of stacking standard nanometer devices. Two realisations are analysed to demonstrate the feasibility of this principle. A first high voltage driver is implemented in a standard 2.5 V 0.25 µm CMOS technology. Although the supply voltage of the high voltage driver is set at three times the nominal supply voltage, none of the transistors in the circuit is stressed by applying too large voltages, resulting in reliable operation and guaranteed minimum lifetime of operation described by the foundry.

An output swing of 6.46 V at a frequency of 10 MHz is measured over a 50 Ω load. With the second high voltage driver, the boundaries of the stacking principle are even further explored. The chip is implemented in a standard 1.2 V 130 nm CMOS technology. With five stacked transistors and a supply voltage of 5.5 V an output swing of 4.2 V at a frequency of 40 MHz is measured over a 4 Ω load with an efficiency of 79%.

To prove the usefulness of this stacking principle, a high voltage driver is integrated in the SOPA architecture, which leads to a fully integrated high voltage line driver. Again, two test chips were developed in a standard 1.2 V 130 nm CMOS technology to materialize this concept. The first, zeroth order, SOPA complies with the aDSL-Lite specification with its 1.1 MHz bandwidth and 42 dB Missing Tone Power Ratio (MTPR). The efficiency is 40%. The second, first order, SOPA faces the two challenges of line drivers in wireline communications: increasing the signal's bandwidth while maintaining a high efficiency. The circuit complies with the aDSL2+ specifications. A MTPR of 58 dB is reached for a DMT signal with a CF of 15 dB. The efficiency for driving a 100 mW aDSL2+ signal is 42%.

Heverlee, August 2007

Bert Serneels
Michiel Steyaert

List of Abbreviations and Symbols

Abbreviations

ADC	Analog-to-Digital Converter
aDSL	Asymmetric Digital Subscriber Loop
AFE	Analog Front-End
AM	Amplitude Modulation
AMI	Alternate-Mark Inversion
AWG	American Wire Gauge
BER	Bit-Error Rate
CAD	Computer Aided Design
CF	Crest Factor
CMOS	Complementary Metal-Oxide-Semiconductor
CO	Central Office
CPE	Customer Premises Equipment
DAC	Digital-to-Analog Converter
DC	Direct Current
DFE	Digital Front-End
DIDF	Dual Input Describing Function
DMT	Discrete MultiTone modulation
DSL	Digital Subscriber Line
DSP	Digital Signal Processing
ESD	Electrostatic Discharge
FEXT	Far-End Crosstalk
FFT	Fast Fourier Transform
G-Lite	less performing ADSL-Lite
GBW	Gain Bandwidth
HCD	Hot Carrier Degradation
HD_2	Second-order Harmonic Distortion Term
HD_3	Third-order Harmonic Distortion Term
HDSL	High-speed Digital Subscriber Line
HDTV	High Definition Television

HPF	High-Pass Filtering
IC	Integrated Circuits
IM_2	Second-order Intermodulation Distortion Product
IM_3	Third-order Intermodulation Distortion Product
IP_3	Third-order Intercept Point
ISDN	Integrated Service Digital Network
ISP	Internet Service Provider
ITU-T	International Telecommunications Union - Telecommunications standardization sector of ITU
ITRS	International Technology Roadmap for Semiconductors
LD	Line Driver
LDDMOS	Laterally Double Diffused MOS
LDMOS	Laterally Diffused MOS
LPF	Low-Pass Filtering
MIM	Metal-Insulator-Metal
MOSFET	MOS Field Effect Transistor
MTPR	Missing Tone Power Ratio
NEBS	Network Exploitation Board Specifications
NEXT	Near-End Crosstalk
NOS	Non-Overlapping Switching
ONU	Optical Network Unit
OSR	Over Switching Ratio
PAR	Peak-to-Average-Ratio
PCB	Printed Circuit Board
PON	Passive Optical Network
POTS	Plain Old Telephone Service
PSD	Power Spectral Density
PSTN	Public Switched Telephone Network
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
RF	Radio-Frequency
rms	root mean square
Rx	Receive
SHDSL	Symmetric HDSL
SFDR	Spurious Free Dynamic Range
SLIC	Subscriber Line Interface Circuit
SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SOI	Silicon On Insulator
SOPA	Self-Oscillating Power Amplifier
TDDB	Time-Dependent Dielectric Breakdown
THD	Total Harmonic Distortion
TSIDF	Two Sinusoid Describing Function
Tx	Transmit
VDMOS	Vertical integrated Diffused MOS

vDSL	Very high-speed Digital Subscriber Loop
VGA	Variable Gain Amplifier
VLSI	Very Large-Scale Integration
VOIP	Voice-over IP
xDSL	Digital Subscriber Loop

Symbols

${}_2\mathrm{F}_1(a,b;c;z)$	The 2-1 hyper-geometric function in the variable z with factors (a,b) and (c) [-]
α	Coupling factor between two coupled SOPAs [-]
$\alpha(\omega)$	Gain term of the complex propagation constant [-]
A	Limit cycle amplitude [V]
$(a)_n$	The Pochhammer symbol, a notation for $\Gamma(x+n)/\Gamma(x)$ [-]
$\beta(\omega)$	Phase term of the complex propagation constant [-]
C_{gate}	Gate capacitance of a MOSFET [F]
C_{int}	Integrator capacitance [F]
C_{in}	Input capacitance [F]
C_j	Junction capacitance of a diode [F]
C_{ox}	Oxide capacitance of a MOSFET [F]
C_{well}	Well-capacitance [F]
d	Cable length [km]
dx	Unit length [-]
e	Euler's number 2.72 [-]
f_{fil}	Cut-off frequency of a loop filter [Hz]
f_{int}	Unit-gain frequency of an integrator [Hz]
f_{lc}	Limit cycle frequency [Hz]
$\gamma(\omega)$	Complex propagation constant [-]
g_m	Transconductance of a MOSFET [S]
I	$\sqrt{-1}$ [-]
I_q	Quiescent current [A]
I_{DS}	Drain-source current [A]
I_{rms}	Rms current [A]
$\mathcal{I}m(z)$	The imaginary part of the complex number z [-]
$J_n(x)$	Besselfunction of the first kind and order n [-]
k	Boltzmann constant $1.3807 \cdot 10^{-23}$ [J/K]
k_R	Material-dependent factor for calculating the skin-effect [-]
L	Length of a MOS transistor [µm]
$L(s)$	Transfer function of a linear loop filter [-]
L_{min}	Minimal gate length of a specified CMOS technology [µm]
η	Total power efficiency of a power amplifier [-] or [%]
N	Number of tones in a DMT signal [-]

n	Voltage multiplication factor [-] Number of stacked transistors [-]
$N_A(A)$	The single input describing function of a non-linearity with one sinusoidal input with amplitude A [-]
$N_B(A, B)$	The dual input describing function for a non-linearity with two sinusoidal inputs with amplitudes A and B, describing the gain of the signal with amplitude B [-]
$O(\phi)$	The Landau symbol also called big-O, which denotes that there exists a positive value A so that if $f = O(\phi)$, $\|f\| < A\phi$ [-]
P_{out}	Output power [W] or [dBm]
R_L	Load resistance [Ω]
R_S	Switch resistance [Ω]
R_{on}	On-resistance of a MOSFET [Ω]
$\mathcal{R}e(z)$	The real part of the complex number z [-]
σ_n^2	Noise energy [dBm]
s	Laplace variable = $I2\pi f$ [1/s]
$\Gamma(x)$	Gamma function [-]
t_{d0}	Delay time of a unit inverter [s]
μ	Mobility [cm^2/Vs]
V_{BD}	Junction breakdown voltage [V]
V_T	MOS threshold voltage [V]
V_{DD}	Nominal supply voltage [V]
V_{DS}	Drain-source voltage [V]
V_{GB}	Gate-bulk voltage [V]
V_{GD}	Gate-drain voltage [V]
V_{GS}	Gate-source voltage [V]
ω	Pulsation [rad/s]
W	Width of a MOS transistor [μm]
x	Scaling factor of an inverter chain [-]
y	Transformer ratio [-]
Z_0	Characteristic line impedance [Ω]

Contents

1

Introduction

IN 1874, while Alexander Graham Bell (who considered himself to be a teacher of the deaf, more than the inventor of the telephone) was working on the harmonic telegraph, the telephone and hearing aids for the deaf, he built a device called phonoautograph. The device was made with Frankensteinian ingenuity out of a dead man's ear (It is not recorded just where the ear came from, volunteered or otherwise.). Speaking into the device caused the ear to operate ... like an ear. The ear's membrane vibrated according to the intensity of the voice, more for louder voices or sounds, less for quieter sounds or whispers. This in turn caused a lever attached to the ear to "write" a wave pattern on smoked glass; bigger waves for louder sounds and smaller for quieter sounds. This inspired Bell. He thought that, by using a membrane to convert sounds of varying intensity into electrical current of varying intensity (instead of just the working of the lever) and then reversing the process on the other end with another membrane, he could replicate speech over long distances. It took him two years to put this idea into practice, but it became the founding principle of telephony.

Once the variable current is generated, it has to have some way to travel to the receiving end, where it is converted back to sounds. From the beginning, copper wire has been the carrier of choice. But, how many wires are needed? The first phones did just use one wire, carrying both the transmitter's and receiver's current and grounding each end in the earth to complete the circuit. However, this created a lot of static interference, since everyone was using the earth to ground their phones. This was fixed when Bell invented a two-wire circuit in 1881. It meant that a phone conversation would require two wires creating a complete circuit, where grounding in the earth was not needed. The two-wire circuit is considered as the start of the billions of twisted pairs for the Plain Old Telephone Service (POTS) that are laying in the ground at this moment.

The history of data-transmission began thus with Alexander Graham Bell, a pioneer who developed the idea that data could be transmitted through

copper wire. Of course, he had no idea of the scope of his findings or where they would actually lead to. However, the principles had been established.

In the course of history, many people improved the telephone. The invention of the microphone by David Hughes, with further improvements by Thomas Edison who introduced the carbon granule transmitter, made the telephone into an instrument that was much more sensitive than Bell's Aluminium alloy diaphragm. By the early 1960s, low-cost transistors and associated circuit components made the introduction of touch-tone into home telephones possible. Extensive human factors tests determined the position of the buttons to limit errors and increase dialing speed even further.

Also in the 1960s, the telephone system gradually began converting its internal connections to a packet-based, digital switching system, whereas the earlier phone systems were purely analog causing great inefficiency. It was very prone to breakdown and noise and did not lend itself well to long distance connections. Today, most voice switching in the world is digital with the exclusion of the final connection from the local Central Office (CO) to the Customer Premises Equipment (CPE). This final connection is an analog POTS line, also called *The Last Mile*.

From the 1950s on, people started experimenting sending digital data over the copper wires. However, while the theoretical capacity of copper to transmit data was long known, mathematician Claude Shannon presented in 1948 its theory of channel-information capacity, the practical use of telephone wires for high-speed data was first demonstrated in the late 1980s. Joseph Lechleider demonstrated, through mathematical analysis, the feasibility of sending broadband. The first efforts, to make use of this capacity, created Integrated Service Digital Network (ISDN). The ISDN vision was very ambitious: to construct a global network for data communications and telephony.

In 1986 the early concept definition of High-speed Digital Subscriber Line (HDSL) started. Digital Subscriber Line (DSL) technology was originally implemented as part of the ISDN specifications. Under the impulse of Joseph Lechleider, asymmetry, between up- and downstream data-rates, was introduced in the DSL spectrum, representing the *a* in aDSL. He understood that many users would benefit from the higher data rates possible in one direction.

In the early years of DSL, the economic benefit was not present. However, the *.com* boom of the mid-1990s created a viable market for DSL. Nowadays, multiple standards for DSL are emerging, grouped under the term xDSL. The reason is the ever-increasing demand for more bandwidth. Latest developed standards, such as aDSL2+ and vDSL2, have the opportunity to offer a triple play of high-speed Internet, Voice-over IP (VOIP) and High Definition Television (HDTV). As such, DSL can preserve its market position between cable and Passive Optical Network (PON) in the field of last mile access solutions.

Figure 1.1 shows a timeline with some interesting aspects of wireline communications from the invention of the telephone to the latest DSL standards.

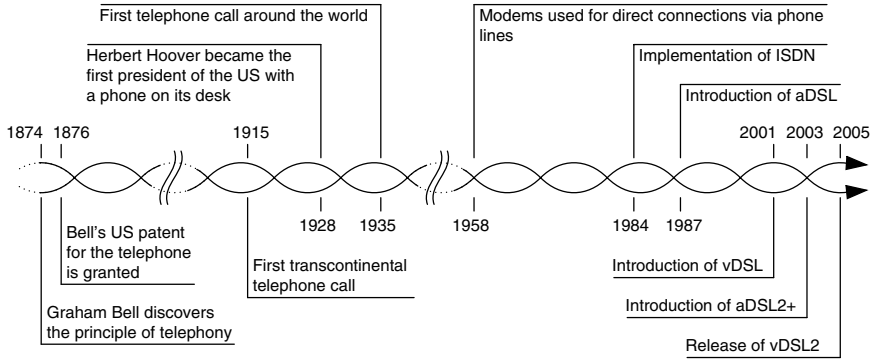


Fig. 1.1. Timeline of telephone wireline communications

1.1 Motivation of the Work

Today, the worldwide DSL market penetration has surpassed all other forms of broadband last mile access technologies combined. The resulting xDSL standards and the prospects of the vDSL2 system have proven the expectations for millions of broadband users. The implementations of these techniques had, however, a big drawback from a power consumption point of view, certainly at the CO side. Its line drivers, the final building block between the modem and the telephone line, consume an enormous amount of power.

A typical CO modem architecture for xDSL is shown in Figure 1.2 [Sto06]. Coding and modulation is done in the digital interface by digital signal processing. The analog part of the Transmit (Tx) channel contains a Digital-to-Analog Converter (DAC), Low-Pass Filtering (LPF) and a Line Driver (LD). The function of the hybrid is to separate the strong transmitted signals from the weak received signals and thus prevent saturation of the Receive (Rx) path. In the Rx channel High-Pass Filtering (HPF) is used to reduce the out-of-band signals such as the echo from the transmit signal. A Variable Gain Amplifier (VGA) is used in order to ensure that the Rx signal optimally fits into the input of the Analog-to-Digital Converter (ADC). This converter is preceded by an anti-alias filter. With the advent of the nano-electronic era, the line driver remains more than ever the bottleneck for lowering cost and power of the Analog Front-End (AFE).

The presented research activities are aimed at improving this building block, to design aDSL/aDSL2+ compliant line drivers with a high voltage output buffer in a low voltage mainstream Complementary Metal-Oxide-Semiconductor (CMOS) technology and at the same time, maximize its efficiency. In this chapter the importance of this work will be motivated and an overview of the contents of this book is given to guide the reader through this work.

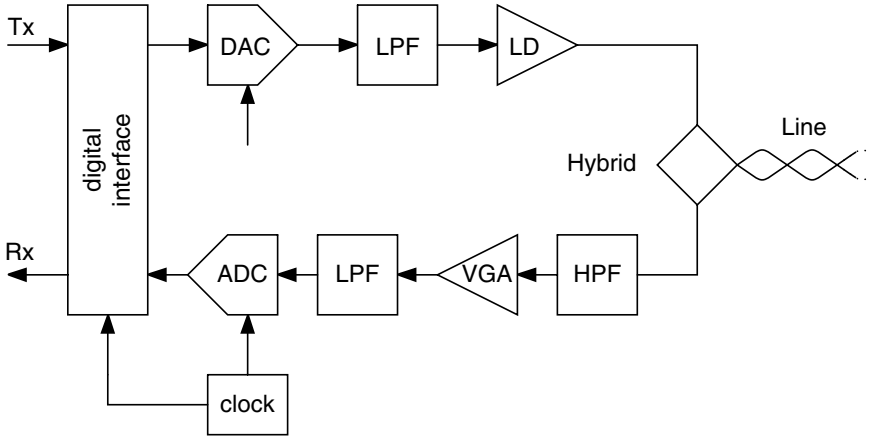


Fig. 1.2. Simplified block diagram of an AFE CO modem for xDSL applications

1.1.1 xDSL Technologies: The Market Opportunities

DSL's subscriber base went up to more than 173 million, while global broadband subscribers reached more than 263 million in the 12 months to 30 September 2006. Each week, 1.25 million people signed up to broadband according to the latest statistics prepared for the international DSL Forum by industry analyst Point Topic. Two-thirds of new subscribers are choosing DSL technology, that delivers broadband over telephone lines. [source: `www.dslforum.org`]

DSL is by far the most popular broadband access technology in the world at 65.6% market share, rising to 82% in the European Union, the world's largest broadband region. Of the remaining broadband access technologies, cable and fiber-to-the-home deliver respectively 23% and 10% of the world's broadband subscribers. Less than 1% of broadband is delivered by satellite, accounting for less than one million subscribers. However, there are still large opportunities for DSL since less than 5% of the phone lines are connected to DSL networks. The majority of the world remains thus "unconnected". DSL reuses the billions of available twisted pairs of the classical POTS. Today vDSL2 with a bandwidth of 30 MHz can offer 100 Mbit symmetrical data rate and enables real triple play. In this point of view, DSL is complying to the need-for-speed on the web for the millions of broadband users.

1.1.2 xDSL Technologies: The Gap

The reuse of the billions of copper wires in the ground for last mile access is a good choice from a market point of view. However, the implementation of those xDSL systems has brought engineers and analog designers a lot of worries. The transmission line characteristics of the twisted pair telephone wires are far from good at higher frequencies. Therefore, specialized modulation techniques

Table 1.1. Overview of the most important driver architectures in relation to the maximum number of lines per 500 cm^2 board

Lines per 500 cm^2 board	24	48	72	96	120
Class AB 740 mW					
Class G 400 mW			NOT NEBS COMPLIANT		
$\Delta\Sigma$ Class D 200 mW					
SOPA 100 mW	NEBS COMPLIANT				

are necessary to reach high bandwidths in Asymmetric Digital Subscriber Loop (aDSL). aDSL signals have a noise-like look with several voltage peaks. This large Crest Factor (CF), meaning the ratio between the maximum voltage and the root mean square (rms) signal voltage, render traditional class AB power amplifiers to be low efficient line drivers.

The importance of high efficiency can be easily observed by taking a look at the Network Exploitation Board Specifications (NEBS) norms. The NEBS prescribe the maximal amount of power that can be dissipated on a 500 cm^2 modem board. If the efficiency of the line drivers is taken into account, the power dissipation will fix the maximum number of lines that can be served by a single board. The result of these calculations is depicted in Table 1.1 [Sev02]. The cost per served line thus increases with decreasing efficiencies of the line drivers. The modem-board density is, nowadays, not only limited by the number and size of the components, but also by thermal limitations.

If a complete modem-board is split in an AFE, Digital Front-End (DFE) and a line driver, one can say that, when scaling the technology to a next node, the power dissipation for the DFE and AFE decreases with roughly 50% and 30% respectively. However, the power savings in the line driver is only a few percent. Today, the line driver represents about 80% of the total power dissipation per served line. The goal is to design highly efficient line drivers such that the cost per line can be lowered. Table 1.1 shows also that traditional architectures do not suffice. Therefore, the presented research activities are based on a relatively novel, highly efficient architecture for xDSL line drivers: the Self-Oscillating Power Amplifier (SOPA) [Pie04].

1.1.3 Power or High Voltage in Nanometer CMOS?

An important research topic of this work is high voltage design in mainstream nanometer CMOS for designing analog power building blocks. The nanometer technologies provide an answer to the increasing integration density of Very Large Scale Integration (VLSI) circuits and the low power requirements of

complex signaling processing applications. For mass-production, the integration of the power amplifier within the digital part of the system could lead to a lower production cost and smaller products [Rey05].

A major issue when integrating power amplifiers in CMOS technologies is the fact that for nanometer technologies, the supply voltage drops to nearly 1 V or even below 1 V. This is done to limit the electric field across the transistor's channel, such that the foundry reliability targets are met. However, the output power is coupled with the square of the maximum voltage swing by $P = V^2/R_L$, and the output swing is of course limited by the supply voltage. Another problem is that the load impedance R_L is fixed by physical constraints, which are very difficult to change. For instance, the characteristic impedance of free space, also called the Z_0 of free space, is an expression of the relationship between the electric-field and magnetic-field intensities. The Z_0 of free space is, like the characteristic impedance in general, expressed in ohms. It is considered as a physical constant and its exact value is $120\pi\ \Omega$. Therefore, the load impedance needs to be converted or transformed into a lower value for achieving a constant output power. This is typically done by an impedance matching network, resulting in extra power losses. On the one hand, these are losses in the impedance network itself. On the other hand, these are losses due to the large current densities in the amplifier driving a low ohmic resistance. After all, when driving high currents, small parasitic resistors can lower the overall efficiency drastically. Moreover, reliability becomes an issue, since electro-migration effects can occur at these current densities. For an xDSL system, the impedance transformation is performed by the line transformer, which is depicted in Figure 1.3.

New power amplifier architectures, such as the SOPA, addresses these issues up to some point, but when entering in the nano-electronic era more has to be done. A 1 V supply is too low for designing an xDSL CO modem. The transformer ratio of the impedance matching network becomes too large such that it becomes impossible to meet the noise specifications of an xDSL system. Moreover, the received signal in the modem will be attenuated with this ratio, resulting in Signal-to-Noise Ratio (SNR) specifications for the building blocks in the Rx path (Figure 1.2) that appeals to one's imagination. The low voltage issues can be elevated by going to higher voltages. This can be done in three ways:

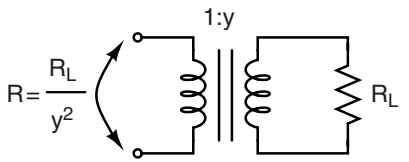


Fig. 1.3. Schematic of the line transformer as an impedance matching network

1. By using a separate high voltage output stage comprised of power transistors. This is a very costly solution, since this requires extra *costly* components on the line card.
2. By using a technology that is able to deal with higher voltages, like DMOS or BiCMOS technologies. These technologies can be integrated in a low cost CMOS process at, of course, a higher cost. After all, this integration requires extra process steps and mask sets. When scaling towards nanometer lengths, the price of these mask sets is increasing exponentially.
3. By using drain source engineering and circuit techniques in a standard CMOS technology. This technique ensures that the devices never encounter a voltage as high as the breakdown voltage over their gate capacitance, while the output swing is higher than this value.

These solutions are ordered from an easy implementation to a very difficult one, but also from a high cost to a low cost implementation. It is only the third and last solution that results in a fully integrated, low cost modem for xDSL applications. Therefore, an important part of the research in this book is dedicated to high voltage circuit design in a mainstream, low voltage nanometer CMOS technology.

These high voltage techniques can also be used for other (low power) applications when using (sub) 1 V CMOS technologies. After all, such low supply voltages put serious restrictions on the design of analog circuits, such as limited gain and SNR.

1.2 Organisation of the Book

The presented work aims for a high efficiency, high voltage line driver in a mainstream nanometer CMOS technology. It is a contribution to a fully integrated low cost, high efficiency AFE for xDSL CO modems.

Chapter 2 starts with an investigation of the required specifications for an xDSL line driver. Since these requirements are a direct consequence of the used channel, a short overview of the channel properties is given. From that, it will become clear why Discrete MultiTone modulation (DMT) is used as the modulation technique. The DMT signals pose severe requirements on the line drivers. A brief overview of the most important reported architectures is given. The conclusion of this overview is that a self-oscillating switching structure is necessary for a high efficient xDSL line driver.

The high voltage techniques developed in this work are applied on the output stage of the SOPA architecture for it is the most efficient line driver for xDSL applications. Therefore, a summary of the behavioral model of the SOPA is given in Chapter 3. The SOPA is characterized by the limit cycle oscillation. Techniques to calculate its amplitude and frequency are discussed. The limit cycle oscillation will act as a natural dither in the non-linear system. Formulas are derived to calculate the possible distortion and Missing Tone

Power Ratio (MTPR) levels. The limitations of the SOPA system, due to the low supply voltages of nanometer technologies, will be explained by means of the behavioral model and the improvements of inserting a high voltage output stage in the self-oscillation structure will be discussed.

Chapter 4 elaborates further on the SOPA architecture in a low voltage technology. The chapter is divided into two major parts. In the first part, the effects of CMOS scaling on the SOPA line driver are further investigated. It will be shown that the efficiency and reliability of the driver will seriously degrade due to the low supply voltages coming from nanometer CMOS technologies.

In the second part of Chapter 4, the principle of stacking mainstream CMOS transistors, as a solution for designing high voltage circuits, is described. Through high level calculations of the power losses, a comparison is made between a high voltage solution in a mainstream low voltage technology and a technology from a previous generation with a high nominal supply voltage. It will be shown that the stacking of standard low voltage transistors is more advantageous in terms of power dissipation and integration prospects.

Chapter 5 provides a materialization for the principle of stacking devices for designing high voltage circuits. Two different implementations are presented. The most important design issues are given and the obtained measurement results are described and compared with the present state of the art. The first design is a 7.5 V output buffer in a 2.5 V 0.25 μm CMOS technology. Using three stacked transistors, an output swing of 6.46 V is measured in a 50 Ω load. With the second design, the boundaries of the stacking principle are further explored. An output stage comprised of five stacked transistors resulted in a 5.5 V buffer realized in a 1.2 V 130 nm standard CMOS technology. An output swing of 4.2 V at a frequency of 40 MHz is measured in a 4 Ω load. The efficiency of this buffer is 79%.

While Chapter 5 gives a materialization of the principle of stacking standard CMOS devices for designing high voltage circuits, Chapter 6 goes one step further. In this chapter, two implementations of the SOPA line driver with a high voltage output buffer in a mainstream 1.2 V 130 nm CMOS technology are presented. The realized prototypes are compared with the present state of the art and they serve as a proof that the stacking principle can be used, even in high-end applications. The first design is a zeroth order SOPA line driver. Measurements point out its compliance with the aDSL-G.Lite specifications and this for a measured efficiency of 40%. With the second design, the goal was set more ambitiously. A first-order SOPA is chosen to comply with the aDSL2+ specifications. A MTPR of 58 dB is measured for a DMT signal with a CF of 15 dB. The total power dissipation for an average output power of 100 mW is 237 mW, resulting in an efficiency of 42%. The presented chips serve as a proof that the superior efficiency of the SOPA line driver can be maintained in nanometer CMOS, thanks to the inclusion of a high voltage output buffer based on the stacking principle.

Chapter 7 concludes with the major contributions and achievements of this research work.

URLs

- http://www.telcomhistory.org/vm/sciencePhonesWork.shtml
- http://www.thehistoryof.net/history-of-dsl.html
- http://www.ralphb.net/ISDN/history.html
- http://isdn.totalaccess.net/history.html
- http://www.fullnet.net/news/0106.html

2

Digital Subscriber Line: Signals, Specifications and Driver Solutions

UNLIKE competing technologies, DSL eliminates the need for extensive and expensive infrastructure upgrades – improvements that are hard to measure in terms of time or money. Where original telephone company strategies centered on the time consuming and costly task of fiber installation, demand for multimegabit services has forced them to evaluate approaches that leverage the existing infrastructure and provide a quicker time to market. That is one of the DSL technology's chief advantages: the ability to transform the nearly 700 million phone lines installed worldwide into multimegabit data pipes capable of speeding digital voice and data to homes and businesses. [Par00].

The first section of this chapter gives an introduction to the DSL technology. Wading through an alphabet soup of acronyms, the history and working principle of a DSL-system will be discussed. This knowledge is mandatory for understanding the various inherited constraints to design an AFE for a Digital Subscriber Loop (xDSL) system.

DSL uses the twisted pair telephone cable to bridge the last mile. This is, however, a very poor channel for high data-rate communication. In the second section an overview of the channel properties is given. With a lumped parameter model of the twisted pair cable, the huge losses of this channel at high frequencies and large loop lengths will be shown. Moreover, cable impairments like bridged taps, cross talk and radio frequent interference will further limit the throughput through the channel. Therefore, specialized modulation techniques will be necessary to allow for the high data-rates of xDSL.

By applying DMT modulation in xDSL-systems, bit-rates close to the Shannon limit can be achieved. DMT splits the channel into several carriers and by loading every carrier with a bit-rate that is proportional to the measured SNR in that frequency bin, the full capacity is usable. Moreover, DMT is easy to implement in an all-digital domain, especially with the increasing processing power and modern Digital Signal Processing (DSP) techniques in nanometer CMOS. In this section, the basics of DMT-modulation and its specifications for an xDSL-system will be explained.

In the last section, traditional solutions for constructing an xDSL line driver are discussed. The large CF of DMT-signals limits the design of high efficiency line drivers. The widely used class AB line driver provides a very linear solution for driving xDSL-signals, but it suffers from an extremely high power dissipation. An improvement to this class AB line driver results in the class G and class H line drivers. By using multiple supplies for a class AB topology, higher efficiencies can be reached. However, for further decreasing the power consumption, switching type line drivers have to be used. This leads to the SOPA line driver, which will form the basis of this research work.

2.1 DSL in a Nutshell

2.1.1 History

Running data and voice traffic over copper wires is nothing new, but during the 1990s new technology has been applied that has made copper into gold. Within the existing copper wire network, that is used for telephony, lies the promise of the need for speed.

The start of DSL is given in the early 1980s. Equipment vendors were working aggressively to develop Basic Rate ISDN, which would provide up to two 64 kb/s B-channels, plus a 16 kb/s D-channel used for signaling and packet data. The information payload, plus other overhead associated with implementation, resulted in 160 kb/s in total transmitted information. A key requirement of ISDN was that it had to reach customers over the existing copper wire loops, equating to 18 kft.[1] However, an Alternate-Mark Inversion (AMI) encoding implementation of Basic Rate ISDN would require use of the lower 160 kHz, which resulted in too much signal attenuation and would fall short of the required 18 kft loop reach.

By 1988, advancements in signal processing and line coding doubled the effectiveness of legacy AMI code by sending two bits of information with each cycle of an analog waveform or baud. The line code was called 2 Binary, 1 Quaternary (2B1Q). A 2B1Q implementation of Basic Rate ISDN uses frequencies ranging from 0 to approximately 80 kHZ, which has less attenuation and results in the desired 18 kft loop reach.

In the early 1990s, some vendors encouraged the use of 2B1Q at higher speeds as an alternate way to provide T1 and E1 services, without repeaters. The technique consisted of splitting the 1.544 Mb/s service into two pairs (four wires), which each ran at 784 kb/s. This technique was referred to as HDSL. The result was a HDSL-based service, specifying loops of up to 12 kft. [Par00].

Further improvement of HDSL has resulted in a single pair HDSL, which is known under the generic name Symmetric HDSL (SHDSL). In a second generation (HDSL2), more improved modulation schemes were used. The spectra

[1] 18 kft corresponds with approximately 5.5 km.

of HDSL mostly remained symmetric, which is favourable for normal data traffic, but is unusable for more recreative applications.

A possible entertainment application was video-on-demand, due to the development of new compression standards for video like MPEG. Video-on-demand needs a high downstream bit-rate (from CO to CPE), but requires a very limited upstream (from CPE to CO). This resulted in aDSL, making use of the power of asymmetry. However, video-on-demand never fulfilled its prospects. However, through the course of these video-on-demand trials, the industry has come to recognize that many data applications were actually asymmetric in nature. The best example of this is Internet access. Typically, Internet users send a small stream of data to a distant server requesting the download of a particular data, graphic, audio or video file. In response, the server begins sending the file at the data-rate that can be supported across the network to the distant workstation. This transaction is extremely asymmetric in nature. During this same time, the Internet evolved into a whole new phenomenon with unheard of growth rates of new Internet service subscribers. The biggest complaints across all users was that it took too long to download files at dial modem or even ISDN data-rates. Hence, a new service and a new technology have soon been married, and aDSL was re-focused to support Internet access. [Par00].

2.1.2 How it Works

The deployment topology of a generic aDSL network is depicted in Figure 2.1. The aDSL technology was aimed at the non-professional user, so a new subscriber should be able to use aDSL out-of-the-box and without modifications on its existing communication network, i.e. the POTS system. The local loop conveys simultaneously the following signals through one pair of wires [Pie04]:

- Downstream bit-rates of up to 8 Mb/s
- Upstream bit-rates of up to 1 Mb/s
- POTS, i.e. analog voice signals

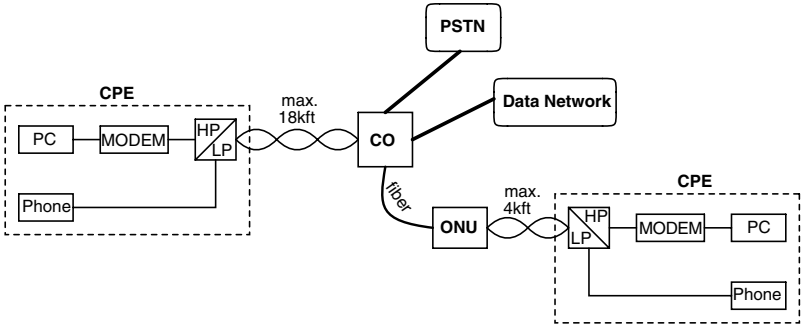


Fig. 2.1. Topology of an aDSL/vDSL network

This is done by the use of frequency division multiplexing without overlap. Voice, arriving from the Public Switched Telephone Network (PSTN) and data, arriving from the data network or Internet Service Provider (ISP) are brought together in the CO and transfered over the telephone line to the CPE. The splitting function for separating the POTS with the aDSL-signals is performed by a splitter consisting of mere low- and high pass filters. For an aDSL system, the loop length between the CO and the CPE is typically limited to 18 kft to ensure a minimal downstream rate of 1.5 Mb/s. To reach the maximum downstream rate of 8 Mb/s the loop must be shorter than 9 kft.

At the high data-rates of a Very high-speed Digital Subscriber Loop (vDSL) system, the loops must be so short that optical fiber will be used until the last few thousand feet (or the last mile), which is also shown in Figure 2.1. vDSL will be primarily used for loops fed from an Optical Network Unit (ONU), which is typically located less than 3 kft from the customer. Few vDSL loops will be served directly from a CO. Optical fiber connects the ONU to the CO. The maximum loop length of a vDSL system reaches 4,000 ft to deliver a data rate of 13 Mb/s. Maximum downstream rates of 55 Mb/s are possible over lines up to 1,000 ft. At this high data-rates, a combination of fiber cables, feeding neighborhood ONUs (fiber-to-the-curb), and last-leg-premises connections by existing copper through a vDSL system provides an attractive alternative for the costly fiber-to-the-home system solution.

2.1.3 Continuing Developments in DSL

The onslaught of new vendors is sure to bring continued variations in DSL technology. Even as mass deployments of aDSL and SHDSL reach the market, new variants are being developed and marketed to fulfill the needs of certain segments of the DSL market [Par00]. The ultimate goal is to increase data-rate and reach for offering a triple play of high speed Internet, VOIP and HDTV.

The main improvements over the original aDSL standard, leading to aDSL2, can be summarized as follows. The speed and reach increases in aDSL2 are largely owed to improved performance on long lines in the presence of interference. aDSL2 can deliver a maximum of 12 Mb/s while extending the reach of the original aDSL by 900 ft.

The new aDSL2 Recommendation also realigns the voice channels and offers providers the ability to combine multiple aDSL2 lines for faster bandwidth to certain customers. In addition, aDSL2 systems can enter an “all digital” mode where voice channels are reassigned to data. This is especially important for business lines that may not need voice services over the aDSL2 line.

The aDSL2+ standard builds further on the aDSL2 standard, increasing the bandwidth by extending the usable frequencies on the line. While both technologies use the same frequencies for telephone calls and uploading data, the download channel is extended from a maximum of 1.1 MHz for aDSL2 to 2.2 MHz for aDSL2+. This increases the maximum downstream rate to 24 Mb/s.

vDSL is the latest member of the xDSL family, which was already mentioned in the previous section. vDSL offers a maximum downstream rate of 55 Mb/s over very short distances. vDSL was originally named vaDSL, but the *a*, for asymmetric, was dropped because vDSL can support both symmetric as asymmetric transport. These connections can be very fast because the physical distances are kept very short, allowing for maximum throughput. As fiber-optic networks continue to move closer to communities around the world, vDSL will become increasingly important as a way to bridge the last mile.

With the aDSL2+ en vDSL standards, the downstream rates are fit to deliver high-speed Internet and video-on-demand, but multiple HDTV channels are still not in reach. The newly standardized vDSL2 (second generation vDSL) enables very high transmission rates up to symmetrical 100 Mb/s (both up- and downstream) on loops of about 300 ft by using a bandwidth of 30 MHz. vDSL2 is able to support multi-channel HDTV using the existing ubiquitous copper telephone line infrastructure. That capability combined with the capacity for multimode implementations enabling interoperability with existing aDSL equipment, means that vDSL2 will integrate readily into legacy and next generation telecommunication networks.

Figure 2.2 shows an overview of the maximum downstream bit-rates versus the year of ratification for various xDSL standards. One can clearly notice the increase in bit-rate following the customer needs. The way these bit-rates are achieved will be more elaborated in the following sections. However, while reading the techniques involved with xDSL, one should always keep in mind

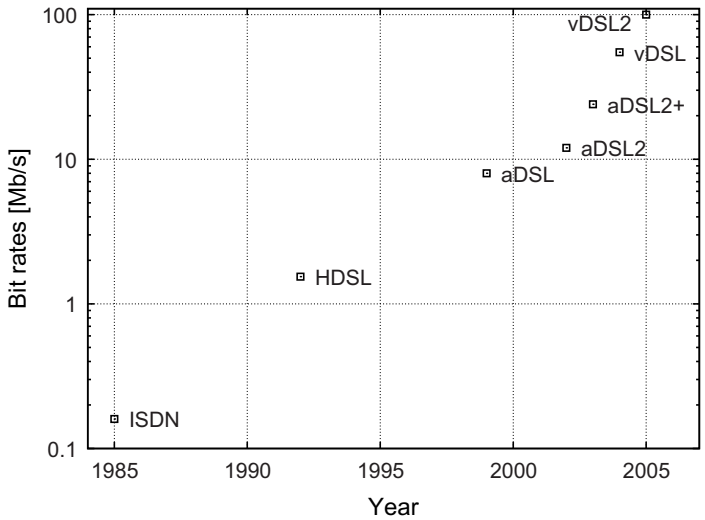


Fig. 2.2. Maximum downstream bit-rate versus year of ratification for various xDSL standards

the legacy of POTS. One of the big advantages of xDSL is its compatibility with POTS, nevertheless it costs flexibility and increased building block specifications.

2.2 The Channel

2.2.1 Cable Technology

As was already mentioned in the introduction of Chapter 1, early telephone systems did use only one wire. The loop was closed by ground. Since the earth acts as a gigantic magnet, the grounded loop picked up various magnetic signals. In 1881 a solution was found by Graham Bell with its invention of the two-wire telephone circuit.

By the use of two wires, the lines became more "quiet", but it only last for a short time. As business bloomed and more people subscribed to the telephone system, the lines again produced unexpected noises. This was due to crosstalk between parallel telephone lines by inductive coupling of the wires. This problem became more prominent in large cities. Due to the advent of the skyscraper, more wires were needed to be put into the ground. Crosstalk seemed to be inevitable. But is was also Bell again who came up with a solution to this problem in 1881: he invented the twisted pair. By twisting the wires, the disturbing signal becomes common mode to the wires and is, in that way, heavily suppressed. Although the twisting schemes evolved, present telephone wires are still built on the same principle [Pie04].

The twisting improves the egress and ingress properties of the wire: it reduces the electromagnetic radiation as well as the pick up of unwanted signals if submerged in an electric field. Wire pairs are combined in cables of different sizes ranging from a couple to a few hundreds of pairs. The cable structure can vary considerably. In Europe, the pairs are often combined in quads that consists of two pairs twisted around each other. These quads constitute binders of some tens of pairs. Finally, several binders are grouped in a single cable [Cor99].

Another cabling issue is the choice of material. Copper seemed to be the best choice from an electrical point of view but it was too soft and too weak. The strength issue was solved by using hard-drawing copper wires. The major problem however is, as always, cost. Therefore, thin copper wires were preferred to save copper. But, thin wires have a higher resistance than thick wires, which in turn means more attenuation. Thus the distance over which a signal can travel is reduced. Therefore, telephone companies have designed their cable plant using the thinnest gauge wire that could support the required services.

In the USA, wire thickness is represented by the denominator composed of the fraction of an inch in wire size, assuming a numerator of 1. Therefore, a wire that is 1/24 inch in diameter is referred to as 24 American Wire

Gauge (AWG). Wire gauges of 24, and more often 26, are present in most North American cable plants. The design rules used by nearly all telephone companies provided for a change in wire gauge with a thinner gauge used near the entrance of a CO to minimize physical space requirements and changing to thicker gauges over long loops to maximize loop reach.

In most markets outside of North America, wire gauges are referred to by their diameter in millimeters. For example, 0.4 mm, which is comparable to 26 gauge, and 0.5 mm, which is comparable with 24 gauge, are the most common; although in many developing countries, heavy gauges of 0.6 mm to 0.9 mm can be found in newly urbanized areas. This variation in wire gauge adds to the challenge of determining a particular DSL system's performance over a particular loop. [Par00].

2.2.2 Twisted Pair Cable Modeling

A twisted pair cable is modeled as a transmission line and can be described using four primary parameters: R, G, L and C [Joh97]. These four parameters are shown in Figure 2.3, where, in terms of "per unit length", R is the internal resistance, G is the conductance, L is the inductance and C is the capacitance. Due to the skin-effect for ac-signals, the internal resistance is actually a complex impedance and can be modeled by

$$R(\omega) = k_R(1+j)\sqrt{\omega}\ \Omega/km \tag{2.1}$$

where k_R is a constant determined by the diameter and the material of the wires. Note that $R(\omega)$ is proportional to the square root of the frequency. Parameters L and C are relatively constant at higher frequencies (larger than 100 kHz) and $G \cong 0$ in modern cables.[2] Typical values for these parameters are $k_R = 0.2$, $L = 0.6mH/km$ and $C = 0.05\mu F/km$ for a 24AWG cable at frequencies higher than 100 kHz.

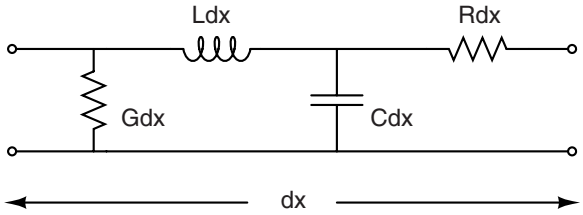


Fig. 2.3. A lumped parameter model for a short section of twisted pair cable

[2] The conductance does not equal zero in cables with a poor quality, which leads to a term proportional to f in the transfer function.

Characteristic Impedance

The characteristic impedance of a transmission line can be shown to equal

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.2}$$

Substituting $G = 0$ and using the approximation $\sqrt{1+x} \cong 1 + x/2$ for $x \ll 1$, equation (2.2) becomes

$$Z_0 \cong \sqrt{\frac{L}{C}} + \frac{k_R(1-j)}{2\sqrt{\omega LC}} \tag{2.3}$$

Thus, for high frequencies $Z_0 = \sqrt{L/C}$. In other words, since L and C are relatively constant, the characteristic impedance of the line is more or less a constant at higher frequencies. Using the typical values above, Z_0 equals 110 Ω for frequencies larger than 100 kHz. At lower frequencies, the characteristic impedance has an extra term, which is inverse proportional to $\sqrt{f}$.

Transfer Function

The transfer function of a twisted pair cable can be modeled by

$$H(d, \omega) = e^{-d\gamma(\omega)} = e^{-d\alpha(\omega)} \cdot e^{-jd\beta(\omega)} \tag{2.4}$$

where $\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$ and is given by

$$\gamma(\omega) = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.5}$$

α and β are the attenuation and phase constants respectively and d is the cable length. Setting $G = 0$ and substituting equation (2.1) into equation (2.5), one becomes

$$\gamma(\omega) = j\omega\sqrt{LC}\sqrt{1 + \frac{k_R(1-j)}{L\sqrt{\omega}}} \tag{2.6}$$

Now using the approximation $\sqrt{1+x} \cong 1 + x/2$ for $x \ll 1$ and making use of $\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$, the following results are obtained:

$$\alpha(\omega) = \frac{k_R}{2}\sqrt{\frac{\omega C}{L}} \tag{2.7}$$

$$\beta(\omega) = \omega\sqrt{LC} + \frac{k_R}{2}\sqrt{\frac{\omega C}{L}} \tag{2.8}$$

Combining equations (2.4) and (2.7), one can see that for a given length d, the cable's transfer function gain (in dB) is given by

$$H_{dB}(d,f) = 20\log_{10}|H(d,f)|$$
$$= -4.343d \cdot k_R\sqrt{\frac{2\pi fC}{L}} \tag{2.9}$$

Thus, the gain in dB is inverse proportional to the square root of f.

In terms of the cable's transfer function phase, combining equations (2.4) and (2.8) one can see that most of the phase is linear, which is a result of delay through the length of the cable, while a nonlinear component is proportional to the square root of the frequency.

Finally, using the typical primary constants above for the 24AWG cable, one can find the gain for a typical twisted pair cable to be approximately

$$H_{dB}(d,f) \approx -0.02d\sqrt{f} \tag{2.10}$$

where d is in km and f is in Hz. Note that equation (2.10) is only useful in estimating the loss in a typical cable as it depends on the primary constants of the cable, which in turn depend on the physical construction such as wire gauge, twist lengths, insulation types and thickness.

A graphical representation of equation (2.10) is depicted in Figure 2.4. The figure shows the line attenuation in the aDSL2+ frequency spectrum for different loop lengths. It can be seen that, e.g., for a loop length of 3 km the attenuation of the signal is −60 dB at a frequency of 1.0 MHz. This results in a division of the received signal by a factor of 1,000 compared to the transmit signal. From this calculation, the importance of a small transformer ratio becomes once again clear. After all, the transformer ratio leads to a further attenuation of the received signal, which requires extremely low noise specifications of the building blocks in the Rx path.

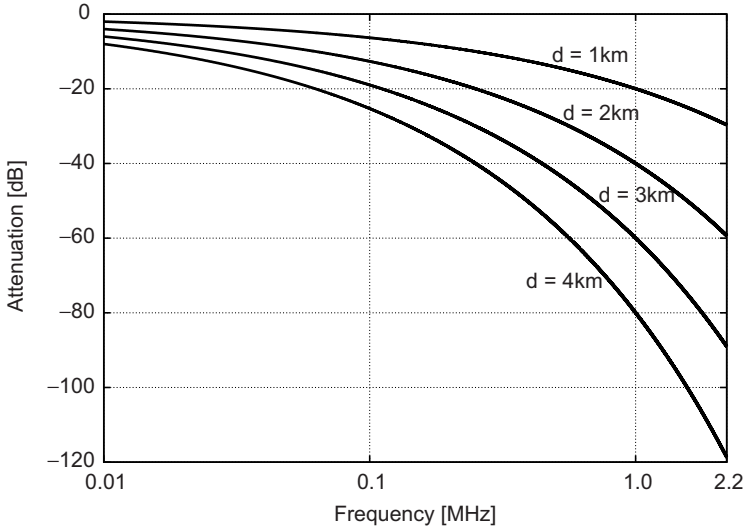


Fig. 2.4. Line attenuation in the aDSL2+ frequency spectrum for different loop lengths

2.2.3 Cable Impairments

The transmission channel capacity depends highly on the twisted pair characteristics, as described in the previous section, but it also suffers from a number of impairments [Cor99].

- Load coils have been used in the early days of telephony to boost and flatten the frequency response of the line at the upper edge of the voice band. As these coils give an unacceptable attenuation at higher frequencies they should be removed, if still present, to allow for DSL services.
- The frequency-dependent attenuation and dispersion leads to pulse distortion and inter-symbol interference. In multi-carrier systems, like DSL, also inter-carrier interference occurs.
- Between different wires in the same cable, there exists capacitive and inductive coupling. The coupling increases as the wires are closer together. It causes unwanted cross talk between the pairs. The cross talk between wire pairs in the same binder or adjacent binder groups is a main noise source contribution. Two types of cross talk can be distinguished, as depicted in Figure 2.5. Near-End Crosstalk (NEXT) occurs at the receiver that is collocated with the disturbing source, while Far-End Crosstalk (FEXT) occurs at a remote receiver. FEXT is attenuated by propagation through the loop, while NEXT is not. Therefore, NEXT dominates FEXT by far for echo canceled systems.
- Some subscriber loops have open-circuited wire pairs tapped onto the main wire pair, called bridge taps. This is mostly due to a subscriber that is disconnected or still has to be connected to the service. The existence of bridged taps in the loop differs from country to country and depends upon the cabling rules in the past. Their presence causes reflections and affects the frequency response of the cabling leading to pulse distortion and inter-symbol interference.
- A loop can also be built up of wires with different diameters, leading to reflections and distortion as well.
- As a result of the cable unbalance, Radio-Frequency (RF) signals can be picked up during propagation over the wire and interfere with the transmitted data at the receiving side. The balance of the cable decreases

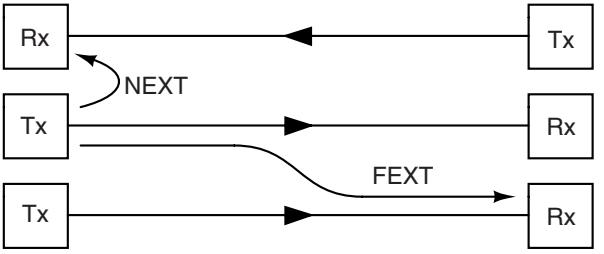


Fig. 2.5. Illustration of NEXT and FEXT

as the frequency goes up. The aerial drop-wires, the vertical cables in high-rise buildings and the in-house wires are the most vulnerable for RF ingress. This ingress can come from a variety of sources such as Amplitude Modulation (AM), radio amateur communication and public safety and distress bands.

2.3 Modulation Techniques

2.3.1 The Shannon Limit

In a communication system, achieving a high bit-rate with a very low probability of bit-error at the same time, is wanted. These parameters can be improved if the transmission power is increased and/or the bandwidth is increased and/or the system's complexity is increased. Of course, a minimum of power, bandwidth and complexity is desirable. But, in fact, the communication system itself puts a limit on these parameters [Alc].

One of these limits is described by the Shannon–Hartley capacity theorem, which provides a theoretical limit for the capacity of a channel that is limited by white Gaussian noise. This limit can be regarded as the maximal achievable bit-rate through a channel. It is given by

$$\text{Capacity [b/s]} = BW \log_2(1 + SNR) \tag{2.11}$$

BW [Hz] stands for the channel's bandwidth and SNR [dB] is the signal-to-noise ratio in the channel. For a band-limited and frequency depended transfer function, the capacity limit becomes

$$\text{Capacity [b/s]} = \int_{f_{min}}^{f_{max}} \log_2(1 + SNR) df \tag{2.12}$$

For long loops, it is shown that a DMT based aDSL system approaches the Shannon limit. For short distances, the departure from the Shannon limit increases. But, by using available techniques, such forward error correction, the gap with the Shannon limit can be closed. However, the cost will increase exponentially.

2.3.2 DMT Modulation

DMT is a form of multicarrier modulation. DMT splits the bandwidth into several discrete channels. In the initialization phase of the modem, the SNR is measured for every channel. Every channel is then modulated by an m-bit Quadrature Amplitude Modulation (QAM)-signal. The constellation size is determined by the measured SNR in accordance with Shannon's theorem (2.11). The use of DMT modulation for xDSL systems has several benefits [Reu96]:

- DMT achieves near optimum use of the line capacity because it can adaptively allocate information and transmit power across the available bandwidth.
- Bit-rates can be adjusted in small increments of a few tens of kilobits per second, enabling DMT hardware to be programmed to support a wide range of data rates in both directions with the possibility of changing these rates "on the fly".
- Power spectral density can be adjusted very flexibly. Forbidden bands (e.g. amateur radio band) can thus be avoided simply by imposing a suitable frequency mask.
- DMT is good at coping with interference from multiple radio frequency sources.
- DMT is the more cost-effective option on complex lines with numerous bridged taps.
- The multi-carrier modulation and demodulation is easy to implement in an all-digital domain by exploiting Fast Fourier Transform (FFT) methods.

Figure 2.6 shows an illustration of the frequency spectrum used for an aDSL system. The DMT modulation consists in this case of 20 carriers constructing the upstream band and 221 carriers constructing the downstream band.

The time domain representation of a DMT-modulated aDSL signal is shown in Figure 2.7(a). Since in the frequency domain the spectrum is flat, the signal in the time domain will have a noise-like nature. An important property of a DMT signal can be clearly seen in this figure. For an aDSL system using a DMT implementation, there is a maximum of 255 discrete subcarriers all transmitting at the same time. Each subcarrier is at a different frequency and phase. When the phases of several carriers align in constructive interference, a voltage spike occurs in the signal. A measure for this voltage spike is the Crest Factor (CF) of the signal. It is defined as the maximum voltage over the rms voltage:

$$CF = \frac{V_{max}}{V_{rms}} \tag{2.13}$$

Sometimes, the Peak-to-Average-Ratio (PAR) is used as a measure for the voltage spike. It is defined as peak power over the rms power of the signal.

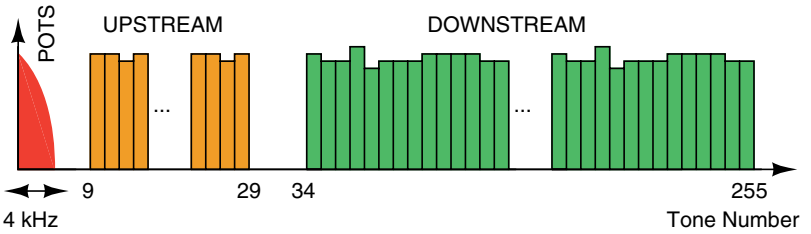
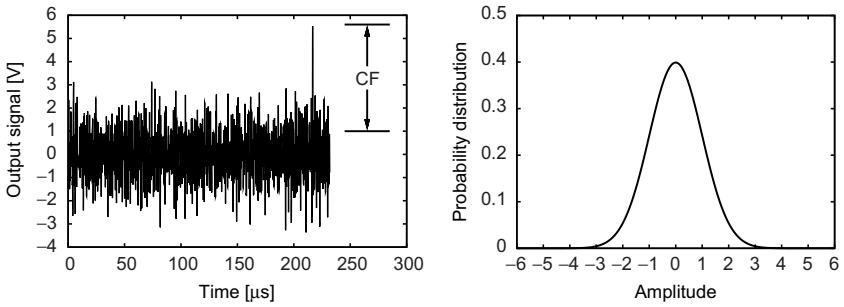


Fig. 2.6. Spectrum of a DMT-modulated aDSL signal



(a) Time domain representation

(b) Associated probability distribution

Fig. 2.7. Time domain representation of a DMT-modulated signal and its associated probability distribution

The downstream time-domain aDSL signal can be represented by [Pie04]

$$x(t) = \sum_{n=34}^{255} a_n s(t - nT)\cos(2\pi n f_i) + \sum_{n=34}^{255} b_n s(t - nT)\sin(2\pi n f_i) \qquad (2.14)$$

In this equation, a_n and b_n represent the constellation point of the m-bit QAM modulation. Note that the constellation size m is on itself function of the carrier number n. $s(t)$ is an envelope function used to normalize the average energy per channel. The carrier spacing f_i is set to 4.3125 kHz for the aDSL system. An aDSL symbol has thus a length of $1/f_i$. During this time the constellation points stay fixed.

A DMT-modulated aDSL signal is thus the sum of N independent QAM symbols, each being carried over a distinct carrier frequency. In equation (2.14) N equals $255 - 34$. For large numbers of N ($N \geq 10$), the amplitude distribution f_A of the DMT-signal can be accurately modeled as a Gaussian random process [Mes93]:

$$f_A = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{A^2}{2\sigma^2}\right) \qquad (2.15)$$

with σ representing the rms-voltage of the signal. This is graphically represented in 2.7(b). It can be seen from Figure 2.7 and equation (2.15) that large amplitude spikes arise very rarely because of statistical averaging. Therefore, it is advantageous to accept some clipping in the DMT signal to make a trade-off between the resulting SNR loss against a gain in lowering the quantization noise of the used ADC and DAC and their power consumption. However, allowing too much clipping results in a steep decrease of the Bit-Error Rate (BER).

To satisfy the system requirement of voltage clipping occurring with a probability of less than $1 \cdot 10^{-7}$, the circuitry must pass the peak voltages corresponding to this probability. To do this, the system must accommodate a

CF of 5.6 or 15 dB. The exact value depends on a combination of hardware and software capabilities. Due to the nature of the DMT-signal, a direct relation between SNR and MTPR cannot be calculated without information on the nature of the non-linearity.

2.3.3 DMT Specifications

Missing Tone Power Ratio

The MTPR is an important feature in the evaluation and design of DMT-based xDSL systems. Better MTPR performance in both the transmission and receive paths results in higher data-rates in the xDSL system.

The MTPR is the ratio of the power in one subcarrier to the noise power in another selected empty subcarrier. There are no data bits assigned to the selected empty subcarrier in a DMT modulation. The MTPR indicates the degree to which a subcarrier QAM signal is corrupted by distortion from all other subcarrier QAM signals. The measurement and evaluation for this kind of corruption are different from that for traditional single-tone distortion. Signal-to-Noise and Distortion Ratio (SINAD), Spurious Free Dynamic Range (SFDR), single-tone harmonic distortion, two-tone harmonic distortion, third-order Intercept Point (IP_3) and Total Harmonic Distortion (THD) are only used for expressing single- or two-tone signal integrity and spectral properties.

The MTPR on the other hand, indicates how the tested device (such as line driver, receiver, line transformer, Tx- and Rx-filter or DAC and ADC) responds to the discrete multitone signal, which is not one or two tones, but may be up to 256 tones or more. One of the design tasks for an xDSL modem is to maintain the fidelity of the DMT signal. All the analog components used on the modem must be designed such that they cause minimal corruption of the DMT signal.

The MTPR of a tested device can be measured as the dynamic range from peak power in a subcarrier to the peak distortion in an empty tone. This is illustrated in Figure 2.8. The MTPR figure is the average of the measurements with several symbols. Since all non-linearities add up in the empty tones at higher frequencies, the MTPR figure will be the worse at those tones. Also, together with an MTPR measurement, the CF of the symbol needs to be reported. [Wu03].

Spectral Masks

The other specifications of an xDSL system are summarized in the following spectral masks. Figure 2.9 shows the downstream spectral mask of an aDSL system as stated by the International Telecommunications Union – Telecommunications standardization sector of ITU (ITU-T) Recommendation G.992.1. To allow POTS compatibility, the generated spurious peaks should be below -97 dBm/Hz in the POTS-band. Since NEXT is a major issue in

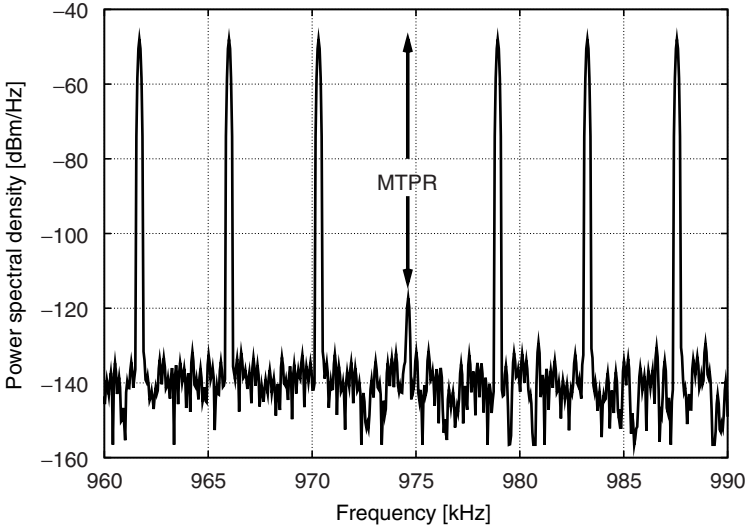


Fig. 2.8. Illustration of the definition for the MTPR

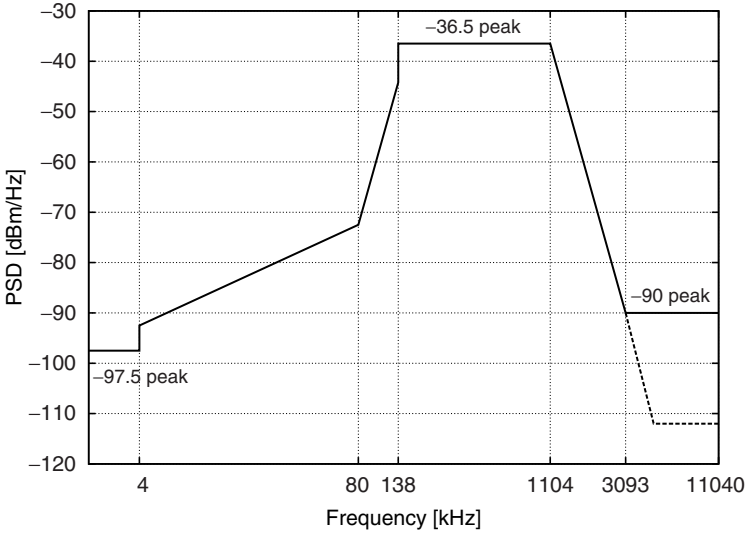


Fig. 2.9. Downstream aDSL spectral mask according the ITU-T Rec. G.992.1

aDSL systems, the Power Spectral Density (PSD) is limited to −72 dBm/Hz peak at 80 kHz in the upstream band in order to lower the received NEXT power. The nominal power PSD in the downstream band is −40 dBm/Hz with a margin of 3 dB. Above 3 MHz, the peaks should be below −90 dBm/Hz, and the integrated power in a 1 MHz sliding window should be below −50 dBm. The latter is shown by the dashed line in Figure 2.9.

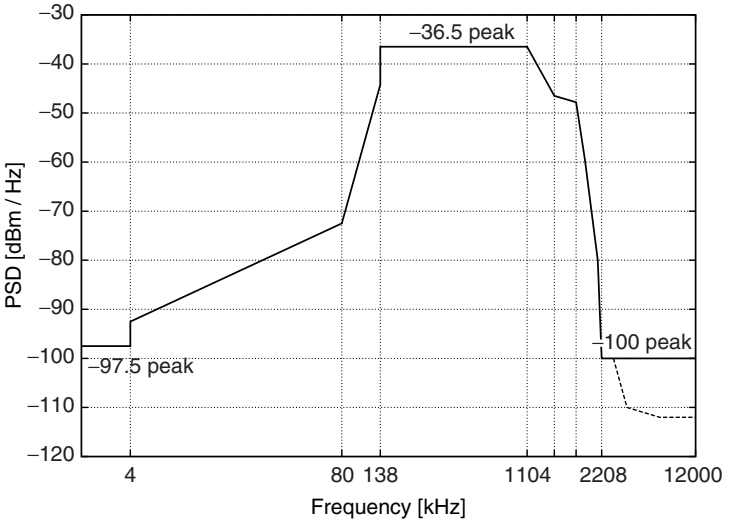


Fig. 2.10. Downstream aDSL2+ spectral mask according the ITU-T Rec. G.992.5

The downstream spectral mask of an aDSL2+ system as stated by the ITU-T Recommendation G.992.5 is shown in Figure 2.10. For allowing POTS compatibility and for reduced NEXT, the spectral mask is the same as the one of the aDSL system up to 138 kHz. The downstream band is now defined as the band between 138 kHz and 2208 kHz, which is twice as much as the aDSL's downstream band. The nominal PSD in that band is −40 dBm/Hz with a margin of 3 dB. Above 3175 kHz, the peaks should be below −100 dBm/Hz in a 10 kHz window. The peak PSD in a 1 MHz window should be below −112 dBm/Hz, which is shown by the dashed line.

2.4 Solutions for xDSL Line Drivers

2.4.1 Line Driver Requirements

In Table 2.1 the most important properties of aDSL (G-Lite) and aDSL2+ systems for line driver design are summarized. The bandwidth is the downstream bandwidth of the xDSL system. With these figures, one can calculate the output voltage that the line driver has to deliver to the line by using a 1:1 transformer ratio. The peak output line power is rated 20 dBm, while the POTS line impedance is typically 100 Ω. Therefore, the rms output voltage is 3.16 V. Multiplying this rms voltage with the CF, the peak-to-peak differential output voltage becomes 33.52 V. This results in a peak current of 167.6 mA [Par03]. The line driver has to deliver these peak voltages and currents with a very high linearity. However, from equation (2.15) it is known that these peaks arise very rarely. Most of the time, the line driver is thus over-dimensioned

Table 2.1. Summary of the most important xDSL requirements for line driver design

	MTPR	Crest Factor	Bandwidth	Output power
aDSL G-Lite	>34 dB	5.6	418.3 kHz	16.3 dB
aDSL	>55 dB	5.6	966 kHz	20 dB
aDSL2+	>55 dB	5.6	2070kHz	20 dB

for driving the xDSL-signals, resulting in very low efficiencies. This causes the low NEBS number for most amplifiers, as was already discussed in Chapter 1.

For the choice of a process technology, one has to bear in mind that the twisted pair is also shared with the POTS. On the telephone wires high voltages occur due to the POTS system. A Subscriber Line Interface Circuit (SLIC) that is able to handle POTS and xDSL on the same die, has to take these high voltages into account [Zoj97, Ben01].

A summary of the high performance requirements of an xDSL line driver is enumerated in the following list. The line driver has to

- Drive a relative large power to the line with a high linearity in a high bandwidth
- Have a minimal power dissipation to increase the NEBS number
- Comply with very stringent out-of-band specifications (<-100 dBm/Hz), which can be derived from the spectral mask
- Deal with the high voltages of the POTS signaling
- Preferably be integrated in a low cost CMOS technology, allowing for a fully integrated AFE

2.4.2 Class AB

The majority of deployed aDSL ports utilize class AB power amplifiers as CO line drivers. Numerous reference designs exists with various voltage supplies, transformer turn ratios and output impedance synthesis factors, all trying to minimize power consumption [Pet03]. In this type of amplifier, the active elements will conduct the output currents while there is an output voltage over these elements. This results in a very high heat dissipation and thus a very low efficiency.

The class AB operation of a power amplifier is a combination of class A and class B operation. Class A is the most linear type of power amplifier. This is due to the fact that the active element (the driving transistor) is never turned off. This results, however, in a very low efficiency.

Class A operation is depicted in Figure 2.11(a). Class A power amplifiers amplify over the whole of the input cycle such that the output signal is an exact scaled-up replica of the input with no clipping. Class A amplifiers are the usual means of implementing small-signal amplifiers. A theoretical maximum

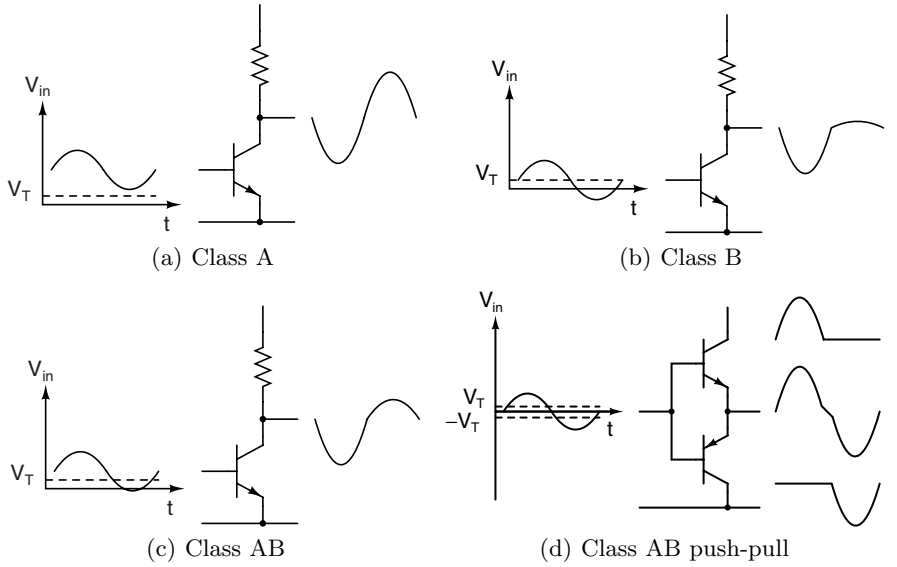


Fig. 2.11. Simplified schematics of class A, B and AB operation

efficiency of 50% is obtainable, but when the CF of the signal is taken into account, this efficiency becomes $<\frac{50\%}{CF}$. Thus for a CF of 5.6, the maximum efficiency will be lower than 9%, resulting in a power dissipation of more than 1 W for driving DMT modulated aDSL-signals. Therefore, class A operation is completely unacceptable for xDSL systems.

Class B amplifiers only amplify one half of the input wave cycle, which is shown in Figure 2.11(b). As such they create a large amount of distortion, but their efficiency is greatly improved. With inclusion of the signal's CF, the maximum theoretical efficiency becomes $<\frac{\pi}{4CF}$. A maximum efficiency of 14% can thus be reached for an aDSL-system, resulting in a minimum total power dissipation of 614 mW. A single class B element is rarely found in practice, though it can be used in RF power amplifiers where distortion is unimportant.

A practical circuit using class B elements is the complementary pair or "push–pull" arrangement. Here complementary devices are used and each amplify the opposite halves of the input signal, which is then recombined at the output. However, this arrangement suffers from crossover distortion. Due to the threshold voltage (V_T) of a transistor, the two active elements of the push–pull stage are both turned off around the zero-crossing. A solution to this is to bias the active elements just on, rather than off altogether when they are not in use. At the zero-crossing, a small current, the quiescent current, flows then through both the active elements. This is called class AB push–pull operation, which is shown in Figure 2.11(d). A single class AB operation is shown in Figure 2.11(c). By applying feedback the crossover distortion can

be further reduced. For a DMT-signal the efficiency for a class AB power amplifier without quiescent current can be calculated as [Pie02a]:

$$\eta = \sqrt{\frac{\pi}{2}} \frac{1}{CF} \tag{2.16}$$

Therefore, the theoretical maximum efficiency becomes 22%.

The quiescent current (I_q) has to be accurately controlled. An I_q which is too low, will generate too much distortion, bringing the amplifier close to class B operation. The higher the I_q, the closer the amplifier will get to class A operation, thus the lower the efficiency. For the calculation of the overall efficiency the power consumption of the quiescent current control circuitry (P_{qcc}) has to be added as well:

$$\eta = \frac{V_{rms}^2 \sqrt{\pi}}{V_{DD}(V_{rms}\sqrt{2} + I_q\sqrt{\pi}) + P_{qcc}\sqrt{\pi}} \tag{2.17}$$

Assuming a rail-to-rail output and a fixed CF for DMT-modulation, the efficiency for a class AB line driver can be written as

$$\eta = \frac{V_{DD}^2 \sqrt{\pi}}{CF\ V_{DD}(V_{DD}\sqrt{2} + CF\ I_q\sqrt{\pi}) + CF\ P_{qcc}\sqrt{\pi}} \tag{2.18}$$

The efficiency for a class AB line driver increases with increasing supply voltage. This however requires a more expensive, high frequent, high voltage technology. By using a high voltage technology and active back termination, the best class AB drivers now consume roughly 740 mW [Sab02], which is very close to the theoretical minimal power consumption. However, the power consumption is still too high for xDSL systems, so there is little chance that class AB line drivers will continue to dominate the market.

2.4.3 Class G/H

The class G power amplifier provides an answer to the efficiency problem related to class AB power amplifiers. In a class G design, multiple supplies are connected to a class AB line driver to cover the voltage peaks of a DMT-signal. For this discussion, the focus is set on the case where two supply voltages are used [Pie02a]: one scaled for the main signal, $V_L = V_H/n$ and one higher for the peak amplitudes, V_H. Figure 2.12 shows a principle schematic of a class G power amplifier with two supply voltages.

The efficiency for an ideal two-supply class G amplifier can be calculated as follows [Pie02a]:

$$\eta = \frac{n\ V_{rms}\sqrt{\pi}}{V_H\sqrt{2}\left(\left(1 - \exp\left(\frac{-V_H^2}{2n^2V_{rms}^2}\right)\right) + n\exp\left(\frac{-V_H^2}{2n^2V_{rms}^2}\right)\right)} \tag{2.19}$$

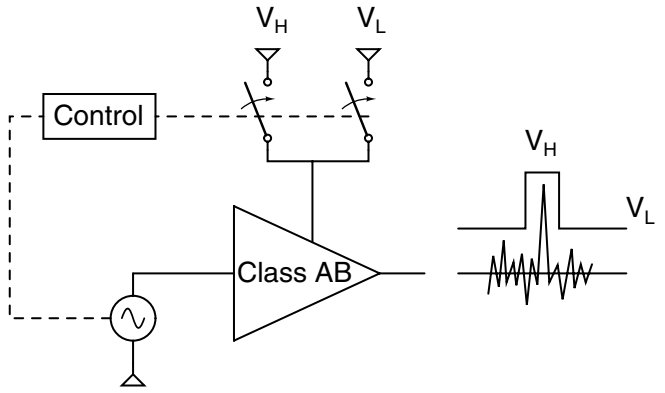


Fig. 2.12. Principle schematic of a two-supply class G power amplifier

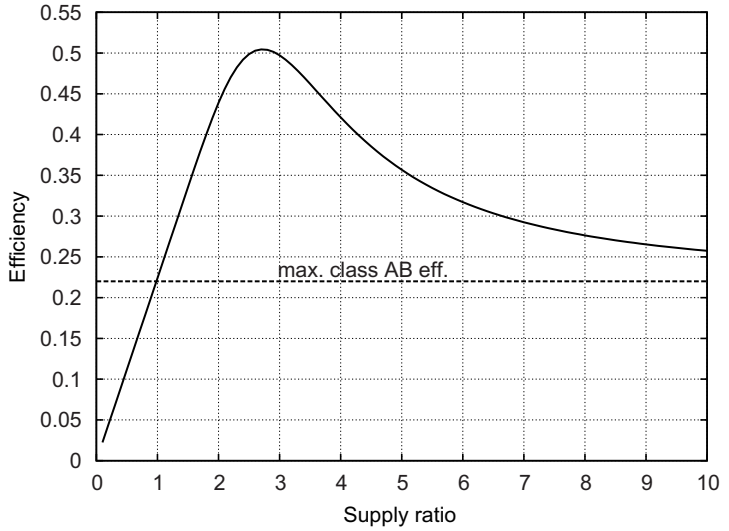


Fig. 2.13. Ideal efficiency versus V_H/V_L ratio for a DMT modulated aDSL signal

Figure 2.13 shows the obtained efficiency for different values of n and with $V_H = V_{rms} \cdot CF$. For $n < 1$, V_L becomes too high resulting in extremely low efficiencies. At $n = 1$, the class AB efficiency is obtained. The class G efficiency reaches a maximum around $n = 3$. This maximum is around 50% for a two supply class G line driver. For higher values of n, V_L becomes too low and the major part of the aDSL-signal is amplified using V_H. Ultimately, the class AB efficiency is reached.

A drawback of the class G amplifier is the additional pair of supplies, so the efficiency of the DC–DC converter has to be added in the total power budget. Furthermore, it is very difficult to achieve the severe linearity specifications due to hard switching and related crossover points. The generation of the

switching signal is very critical. The detection of the input signal at the trigger level for the switches has to be accurate enough to avoid unnecessary supply switches.

The class H amplifier is similar in power consumption compared to the class G approach. Instead of hard switching, the supply voltage is progressively following the output signal. It can be seen as a class G power amplifier with an infinite number of supply rails. This avoids the need for good power supply rejection but of course requires additional circuitry for generating the driver supply. The supply generation can be done for instance by a capacitive boosting of the voltage applied. Power consumption compared to class G remains however equal, but only one pair of supplies is required, so no extra DC–DC converter is necessary. But, the number of capacitors on board is not reduced and one should be aware of signals exceeding the applied supply voltage.

The most common implementation is that of a class AB line driver with a fixed supply that is capacitive boosted with the input signal [Bic03], resulting in a total power dissipation of 700 mW. While this technique is very attractive for high performance, high efficiency audio amplifiers, for xDSL line drivers the class H does not provide a real improvement on the class AB power amplifiers.

2.4.4 Class D

Basic Class D Configuration

A typical class D amplifier consists of a modulator that converts an analog signal into a high frequency Pulse Width Modulation (PWM) signal. This PWM signal is then applied to the output stage, which are often large output switches. These switches deliver the current to the output load. Finally, a LPF removes the high frequency switching signals. A principle schematic is shown in Figure 2.14. The distinction is made between synchronized and

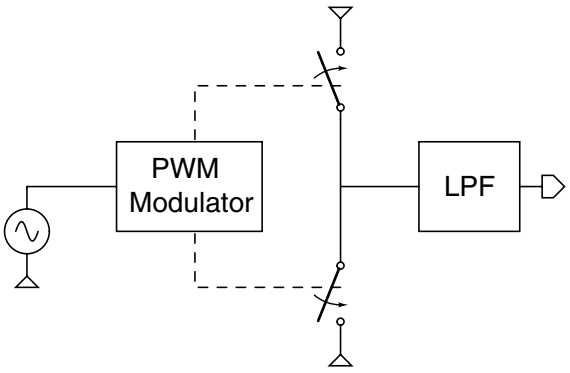


Fig. 2.14. Principle schematic of a class D power amplifier

self-oscillating (a-synchronized) class D amplifiers whether the modulator is clocked or not. In this section the synchronized class D power amplifier is discussed.

The class D power amplifier can achieve very high efficiencies, since it makes use of a switching output stage. If the on-resistance of the output switches is neglected, there is no simultaneous current through and voltage over the switch or active element. So there is no heat dissipated in the switch, resulting in a maximum efficiency of 100%. This type of power amplifier is very popular in the audio application field for its high efficiency and high linearity when amplifying low frequent signals. After all, audio signals have a small bandwidth, <20 kHz, compared with a switching frequency between 200 kHz and 500 kHz [Pie04].

For applications with a high bandwidth, like xDSL, the design of a class D line driver is not so obvious. The high bandwidth (up to 30 MHz for vDSL2) and the very stringent out-of-band specifications of xDSL requires a very steep output filter or a high Over Switching Ratio (OSR). The OSR is defined as the mean switching frequency divided by the signal bandwidth. The output filter needs to be a passive filter. For xDSL line driver applications, extra passive components are thus required, lowering the integration density and increasing the cost. Increasing the switching frequency results on the other hand in increasing switching losses. Therefore, the switching frequency must be carefully chosen in order to still gain in efficiency.

Self-Oscillating Class D Configuration

The principle of the self-oscillating class D amplifier originates from the open loop modulation technique, also called natural sampling, which is shown in Figure 2.15. The problem is reduced to the generation of a triangular waveform. The block schematic of a self-oscillating class D amplifier is shown in

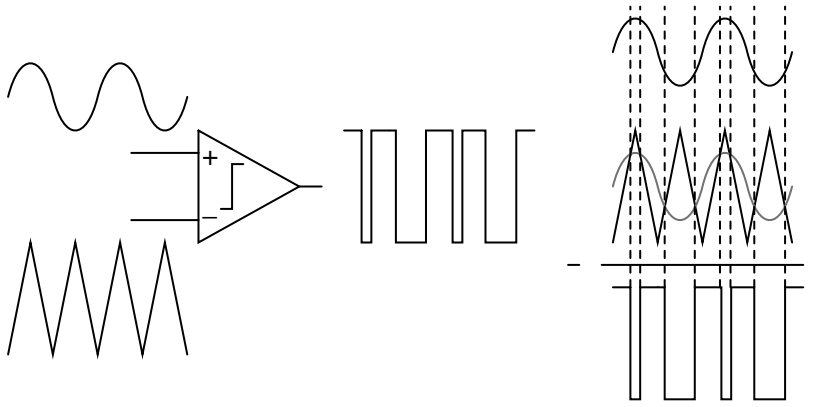


Fig. 2.15. Principle schematic of natural sampling

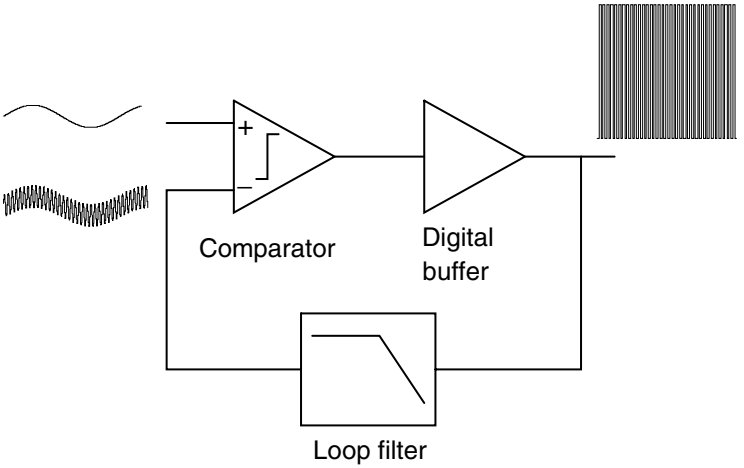


Fig. 2.16. Block schematic of a self-oscillating power amplifier

Figure 2.16. In the same figure, the waveforms on the different nodes are plotted. They can be interpreted as follows: A filtered version of a square wave is a triangular wave. Due to the feedback, the input signal can be considered as a shift in bias point, so a triangular approximation of the input signal resides at the negative input node. Since for in-band signals, the system is in unity feedback and the loop filter is assumed to be linear, the in-band frequency content of the output square wave will thus be the same as that of the triangular wave and thus as the input signal [Pie04].

The circuit received much credits in the audio field for saving components. However, its applicability for xDSL is far from trivial due to the high bandwidth and linearity constraints. An extensive description of the self-oscillating class D line driver for xDSL applications can be found in [Pie04]. The presented line drivers in that work outperformed all existing class AB and class G line drivers in terms of efficiency.

As already being pointed out, the use of higher output voltages is beneficial for improving the efficiency. Chapter 4 of this book will give a thorough explanation of the design considerations for increasing the output voltage of a class D line driver in a mainstream CMOS technology.

2.4.5 Class K and Other Combined Structures

A basic schematic of a class K power amplifier is shown in Figure 2.17. It consists of a linear amplifier whose output current is monitored. When its output current and as such also its power consumption exceeds a certain threshold, an extra current source is switched in. The main current is then delivered via high efficiency switching. This topology has been successfully implemented in the audio world [vdZ99], however, its principle still has to be proven for xDSL applications.

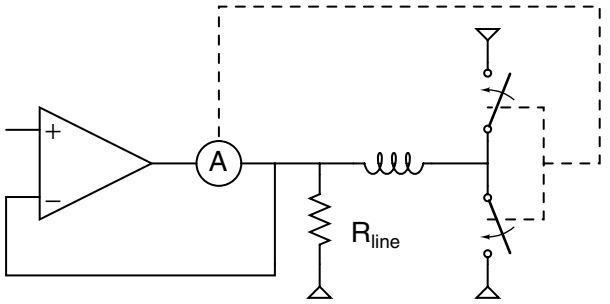


Fig. 2.17. Principle schematic of a class K power amplifier

The concept of combined structures is based on the idea to combine the advantages of linear drivers and switched mode drivers. Why not deliver the main power via switching techniques, while monitoring and correcting the output via a linear amplifier, similar to the class K structure? This concept is given the name "Beauty and the Beast".

The "Beast" or power driver is delivering most of the power with high efficiency, but moderate linearity. It can be a class B, G or switching amplifier in which quiescent current or losses are minimized. The "Beauty" or correction amplifier can then deliver a limited power to linearize the signal before it reaches the line. It can be a high bandwidth, low noise, low power class AB amplifier. The "Beauty" corrects in this way the deviations imposed from the "Beast", while limiting itself to low power operation. It can even reduce the filter requirements needed when implementing a switched line driver. It is expected that power consumption will be below 550 mW [Moo03].

2.5 Conclusions

The big opportunity of DSL for last-mile Internet access is that it makes reuse of the billions of twisted pair wires in the ground. However, the unshielded telephone wires are far from ideal for high bit-rate applications. The most important telephone cable impairment is the large attenuation in function of frequency and distance. That is why DSL is a "real" last-mile access technology. However, DSL promises to turn copper into gold. By making use of DMT modulation techniques, data-rates close to the Shannon limit could be achieved. DMT modulation, however, turned out to be a nice example of the difference between theory and implementation. The smart modulation technique puts severe requirements on the line driver of the AFE. DMT-signals are characterized by high voltage peaks, or a large CF, in the time domain representation. The line driver has thus to be able to deal with this large CF.

The majority of the deployed aDSL ports utilize class AB power amplifiers as line drivers. By using high voltage technologies and by gradual

improvements, the best class AB line drivers reach an efficiency of 12%, which is very close to their theoretical limit. But still, it is unacceptable low.

New circuit techniques lead to class G and class H topologies. Although they can reach a theoretical efficiency up to 50%, the efficiency of practical implementations does not really exceed that of a class AB topology. Other techniques like class K and combined line drivers have been proposed, but none of them have been realized so far.

A really high efficiency can be achieved with switching line driver topologies. Traditional synchronous class D and self-oscillating class D power amplifiers have proven their effectiveness in low bandwidth applications, such as audio amplifiers. For xDSL applications, their design is far from straightforward. One has to deal with the stringent out-of-band specifications, high switching frequencies and high linearity requirements. It is proven in [Pie04] that the self-oscillating power amplifier is a highly efficient line driver for xDSL applications.

URLs

- `http://people.deas.harvard.edu/~jones/cscie129/nu_lectures/lecture13/DSL/DSL.html`
- White Paper: aDSL2/aDSL2+: `http://www.dslforum.org/learndsl/pdf/ADSL2_wp.pdf`
- `http://www.itu.int/osg/spu/ip/chapter_seven.html`
- `http://www.dslforum.org/dslnews/pdfs/2005/0513%20VDSL2%20for%20website.pdf`

3

The SOPA xDSL Line Driver

SINCE the high voltage line drivers presented in this book are based on the self-oscillating class D principle, the behavior model of the SOPA [Pie04] is refurbished in this chapter. This model provides fast architectural explorations for the designer of highly efficient power amplifiers based on the self-oscillating principle. For a mass product, like xDSL, in a dynamic market, time-to-market is a crucial parameter. Therefore, fast architectural exploration is very important, especially when technology migrates from one node to another.

The methods described in this chapter to model the frequency response and distortion of a hard non-linearity are based on the describing function method. Therefore this chapter starts with the basics of this methodology. In the next part, the behavioral model of the SOPA is described based on its reference model. The limitations of this structure, due to the low supply voltage of nanometer technologies will be discussed. The final section of this chapter shows the possible improvements of inserting a high voltage output stage in the self-oscillating structure.

3.1 The Describing Function Analysis Method

3.1.1 Nonlinear Systems

A system whose performance obeys the principle of superposition is defined as a linear system. This principle states that if the input $r_1(t)$ produces the response $c_1(t)$ and the input $r_2(t)$ yields the response $c_2(t)$, then for all a and b the response to the input $ar_1(t) + br_2(t)$ will be $ac_1(t) + bc_2(t)$; and this must be true for all inputs. A system is defined as time-invariant if the input $r(t + \tau)$ produces the response $c(t + \tau)$ for all input functions $r(t)$ and all choices for τ.

The simplest class of systems to deal with analytically is of course the class of linear time-invariant systems. For such systems the choice of time origin is of no consequence since any translation in time of the input simply

translates the output through the same interval of time and the response to simple input forms can be superimposed to determine the response to more complex input forms. This permits in principle to generalize from the response for any input to the response for all other inputs. The elementary input function, most commonly used as the basis for this generalization is the unit-impulse function. The response to this input is often called the system weighting function. All possible modes of behavior of a linear invariant system are represented in its weighting function. Once having determined this function, which is just the response to one in particular, the performance of such a system can hold no surprises.

Any system for which the superposition principle does not hold, is defined to be nonlinear. In this case, there is no possibility of generalizing from the responses for any class of inputs to the response for any other input. This constitutes a fundamental and important difficulty which necessarily requires any study of nonlinear systems to be quite specific. One can attempt to calculate the response for a specific case of initial conditions and input, but make very little inference based on this result regarding response characteristics in other cases. [Gel68].

3.1.2 The Describing Function Viewpoint

The technique used to describe the behavioral model of the SOPA is the describing functions method [Gel68]. The goal of this method is to provide a mathematical description for systems which contain hard non-linear blocks. With this mathematical description, the designer gains more insight in the working principle of the system. The method will only work for systems which have localized non-linearities.

The describing function method is schematically represented in Figure 3.1. The input signal is split into several input signals $x_i(t)$. For each input signal the non-linear operation is replaced by a linear one which depends on the amplitude of the input. This is called quasi-linearization. The $w_i(t)$ are the weighting functions or describing functions for the different input signals. After summation, the obtained approximation $y_a(t)$ needs to match the output $y(t)$ as close as possible. According to the describing function method, the mean-squared error should be minimized:

$$\overline{e(t)^2} = \overline{y_a(t)^2} - 2\overline{y_a(t)y(t)} + \overline{y(t)^2} \tag{3.1}$$

The weighting functions $w_i(t)$ need thus to be chosen so that the mean-squared error is minimal. If the input signals are uncorrelated, the weighting functions must fulfill the following condition:

$$\int_0^\infty w_i(\tau_2)\overline{x_i(t)x_i(t+\tau_1-\tau_2)}d\tau_2 = \overline{y(t)x_i(t-\tau_1)} \qquad \tau_1 \geq 0, i = 1, 2, \ldots, n \tag{3.2}$$

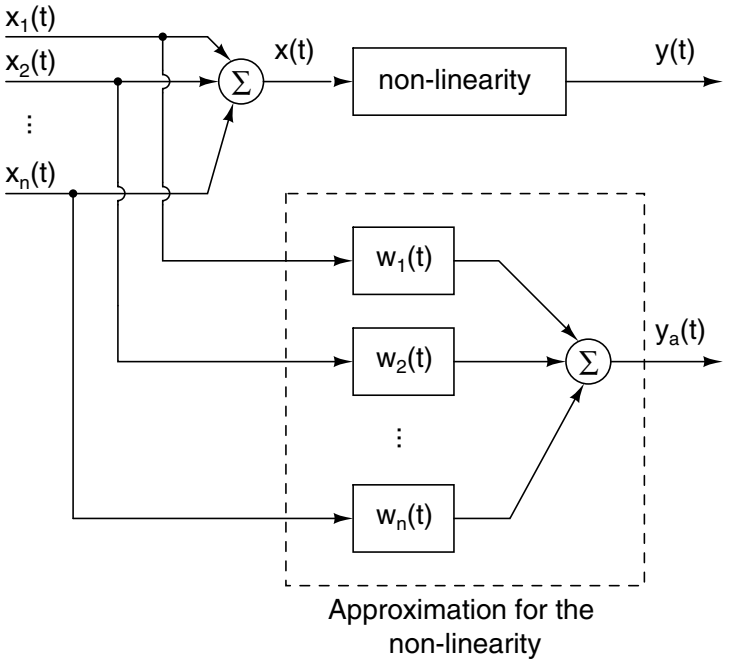


Fig. 3.1. General linear approximation for a non-linear operator

The weighting functions can thus be calculated by equating the cross correlation between the filtered input (the input multiplied by its weighting function) and the input itself with the cross correlation between the output of the non-linearity and the specified input.

In the case of the SOPA system, the non-linearity is the comparator. The most important describing functions related to this system are the single sinusoid describing function and the two sinusoid describing function [Gel68].

- **The Single Sinusoid Describing Function:**
  For a sinusoidal signal $x_i(t) = Asin(\omega t + \theta)$ with A and ω determined and the phase θ being a uniformly distributed random variable between 0 and 2π, the single sinusoid describing function for an ideal comparator with a V_{DD} supply equals
  $$N(A) = \frac{2V_{DD}}{\pi A} \tag{3.3}$$

- **The Two Sinusoid Describing Function (TSIDF):**
  There are now two describing functions, one for each input sine wave. For an ideal comparator and for two sine waves of which the amplitudes fulfill $B \ll A$, the two sinusoid describing function equals
  $$N_B(A, B) \approx \frac{V_{DD}}{\pi A} = \frac{N(A)}{2} \tag{3.4}$$

3.2 Behavior Model of the SOPA

3.2.1 Reference Model

Figure 3.2 shows the reference model of a SOPA. The reference model is a general structure from which every SOPA structure can be defined. This model provides a mathematical description of a SOPA. In this way, the results of the behavior model can be cross checked with the numerical calculations of the reference model.

A complete SOPA consists of two of these building blocks that are differentially driven and coupled at the outputs by the line transformer, giving galvanic isolation towards the line. A basic SOPA building block consists of a non-linear element, the comparator, which is in a feedback loop by a loop filter $L(\omega)$ of order m and with a cut-off frequency of f_{fil}. This loop filter will determine the mean switching frequency of the system. The n integrators with unity-gain frequency f_{int} form, together with the feedback coefficients β_i, the forward filter $G(\omega)$. This filter is used to increase the SNR by introducing noise-shaping into the system. From Figure 3.2 every possible SOPA configuration can be derived by selecting the number of integrators n and the order of the loop filter m. A n^{th}-order SOPA is defined as a SOPA with n integrators in the forward path, giving a forward filter of order n. If no forward filter is present, the SOPA is of zeroth order. The functionality of the different feedback coefficients β_i can be explained as follows:

- β_1, the first feedback branch, sets the output signal level. It is the main feedback branch and its linearity and noise level will determine the complete system behavior.
- β_n, the feedback branch closest to the comparator, introduces mathematical zeros at f_{int}/β_n in the transfer function of the complete system. f_{int} is the unity-gain frequency of the integrators. The reason for this is that for low loop gains the feedback branch β_n short circuits the other integrators. In this way, the last feedback branch β_n will determine the oscillation frequency for low values of f_{int}.
- The $\beta_{i\neq 1,\ n}$ terms are introduced to set the signal levels at the outputs of the different integrators.

The numerical verification of the models described in this chapter has been done using the *dassl*-routine [Bre89], which is compiled in the OCTAVE numerical computation program [Eat97]. Table 3.1 shows the default values for the numerical simulator. All examples in this chapter use these values, except otherwise noted. The default value of the nominal supply voltage is set at 1.2 V, the supply voltage of the technology of the two SOPA implementations in chapter 6. This will reveal more clearly the limitations of a SOPA xDSL line driver in a low voltage nanometer technology and the importance of the research performed in this work towards a high voltage output stage.

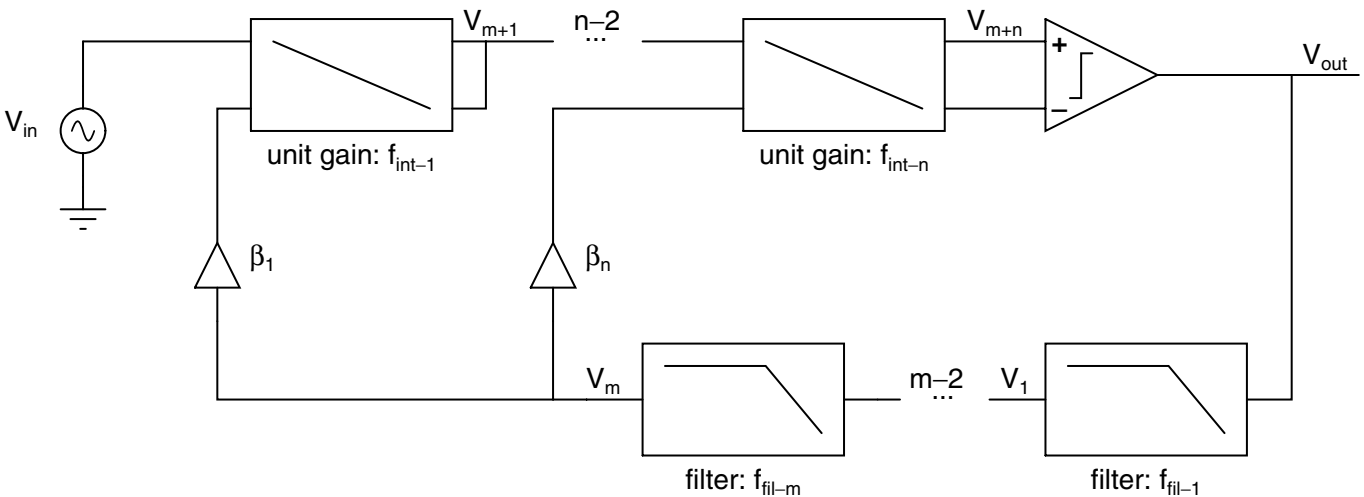


Fig. 3.2. Schematic of a general basic self-oscillating class D amplifier building block

Table 3.1. Default parameters of the numerical simulator

	Parameter	Value
Simulator		
	algorithm	dassl
	start time	0 s
	step time	1 ns
	stop time	10 ms
	initial values	all state variables = 0 except $V_1 = 0.1$
Signal		
	waveform	sine wave
	amplitude	0.1
	frequency	1 MHz
SOPA-parameter		
	order	0
	loop filter order	3
	loop filter cut-off frequency	10 MHz
	integrator unit gain frequency	1 MHz
	supply voltage V_{DD}	1.2 V
	comparator gain	10^6
	β_i	1
	coupling factor α	0.25

3.2.2 Limit Cycle Oscillation

The SOPA is an un-clocked switching power amplifier, which means that it has to generate the mean switching signal by itself. It is shown in [Pie04] that the oscillation is a property of the system and does not depends on initial conditions. Such an oscillation may be viewed as a trajectory in the state space of the system which closes by itself and thus repeats. This is called a limit cycle oscillation.

To perform the analysis of the system in the frequency domain, a describing function analysis is used as mentioned in Section 3.1. In the describing function method, the non-linear comparator is described as a quasi-linear gain block which depends on the input amplitude if only one sinusoid is present. The single sinusoid describing function for an ideal comparator is given by equation 3.3. The limit cycle frequency f_{lc} and amplitude A can be calculated by solving the Barkhausen criterion: $L(s) N_A(A) + 1 = 0$. $N_A(A)$ is the describing function of the comparator and $L(s)$ is the loop filter of order m. If the cut-off frequencies of the loop filters are taken the same, i.e. $f_{fil-1} = f_{fil-2} = \cdots = f_{fil-m} = f_{fil}$, than the loop filter can be modelled in the frequency domain as

$$L(s) = \left(\frac{2\pi f_{fil}}{s + 2\pi f_{fil}} \right)^m \tag{3.5}$$

The equation resulting from the Barkhausen criterion can be split into two real equations: an amplitude-balance and a phase-balance:

$$\mathcal{R}e\left(L_f(s)N_A(A)\right) = -1 \tag{3.6}$$

$$\mathcal{I}m\left(L_f(s)N_A(A)\right) = 0 \tag{3.7}$$

Solving this set of equations leads to the limit cycle frequency and limit cycle amplitude of the SOPA:

$$f_{lc} = f_{fil}\tan\left(\frac{\pi}{m}\right) \tag{3.8}$$

$$A_{lc} = \frac{2V_{DD}}{\pi}\cos^m\left(\frac{\pi}{m}\right) \tag{3.9}$$

In the remaining of the text A_{lc} will be denoted as A. Equation (3.9) reveals the linear dependency of A on the supply voltage V_{DD} of the comparator. This will have an effect on the dithering character of the SOPA line driver, which will be explained in Section 3.2.4.

The results that are obtained with the describing function method are based on approximations. Therefore the analytical results should always be checked by numerical simulations to see if the approximations hold.

Figure 3.3 shows the comparison between numerical calculations, indicated by a square and the results from the describing function analysis (3.8) and (3.9). The limit cycle amplitude and frequency are calculated for different values of the loop filter's cut-off frequency and order. An almost perfect match can be observed.

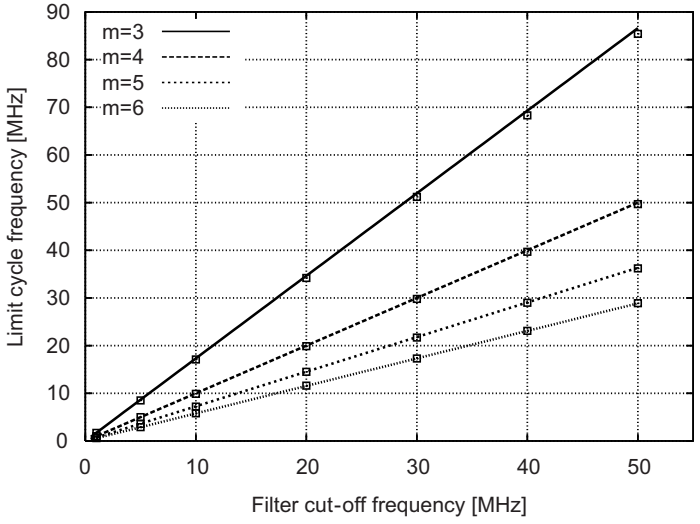
3.2.3 The Coupled System

An important aspect of the SOPA system is the coupling of two SOPA building blocks via the load. Figure 3.4 shows a schematic representation of two differentially coupled SOPA amplifiers. If the load R_L is assumed to be resistive and the output buffer is non-ideal with an output resistance r_{out}, the coupling factor α equals

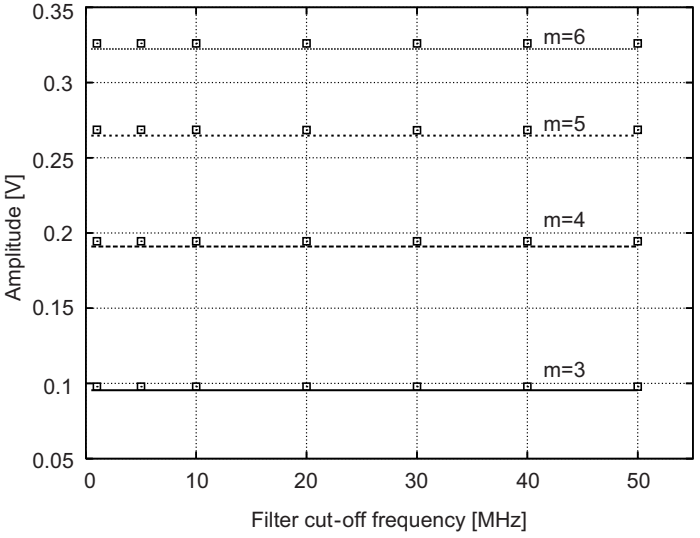
$$\alpha = \frac{r_{out}}{2r_{out} + R_L} \tag{3.10}$$

The coupling factor α is, in case of a resistive load, always between 0 and 0.5. The coupling is modeled by a cross-coupled amplification factor that splits the signal in a forward coupling factor $(1-\alpha)$ and a cross-coupling amplification factor α. The comparator is modeled by its describing function $N(A)$ and the loop filter is represented by its transfer function $L(\omega)$. Via the calculation of the loop gain of the coupled system, the Barkhausen criterion is given by

$$\frac{\alpha^2(N(A)L(\omega))^2}{(1+(1-\alpha)N(A)L(\omega))^2} = 1 \tag{3.11}$$



(a) Limit cycle frequency



(b) Limit cycle amplitude

Fig. 3.3. Numerical verification (squares) of the results obtained using the describing function analysis (solid line)

This equation can be further simplified to

$$(1 + N(A)L(\omega))\,(1 + (1 - 2\alpha)N(A)L(\omega)) = 0 \tag{3.12}$$

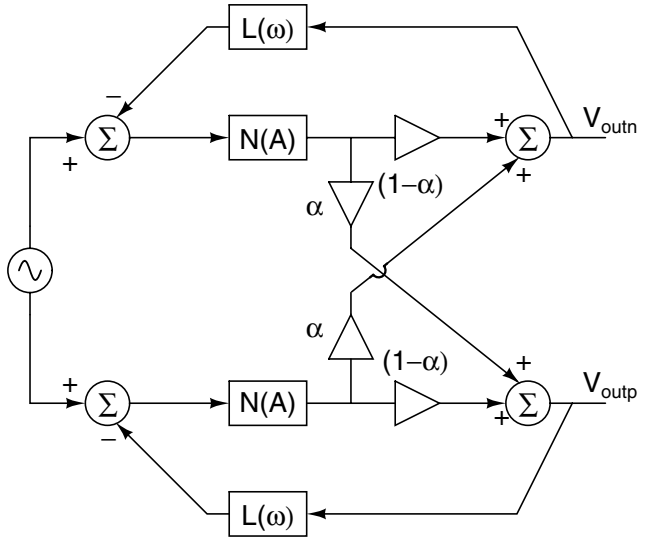


Fig. 3.4. Schematical representation of a coupled differential SOPA amplifier

From equation (3.12) it is clear that two oscillation modes exist in the coupled system.

- One is the solution of $(1 + N(A)L(\omega)) = 0$ and represents an in-phase oscillation of the two coupled SOPA amplifiers. This equation is the same as the Barkhausen criterion of the single SOPA system (3.6) and (3.7). This means that the in-phase oscillation has the same limit cycle frequency and amplitude as in the single SOPA case. In this mode the two SOPAs oscillate as if they were not coupled. This has an important effect that the oscillation of the system is common mode for the differential load. Therefore, the power consumption is heavily reduced, which increases the efficiency. Moreover, the extra filtering in the output power path to remove the limit cycle becomes obsolete.
- The other is the solution of $(1 + (1 - 2\alpha)N(A)L(\omega)) = 0$ and represents the case where the two SOPAs oscillate in counterphase. This mode is unwanted since limit cycle is transferred to the load.

To determine which mode or modes will occur in the coupled system, a stability analysis has to be performed. In [Pie04] an extensive stability analysis has been performed for a resistive, inductive and capacitive load, to cover the complete impedance behavior of a real telephone line. In all cases the in-phase or common mode oscillation is dominant. This means that two coupled SOPAs will always oscillate in-phase.

3.2.4 The Forced System

Dithering Effect of the Limit Cycle Oscillation

In this section the response of a zeroth order SOPA to an external sinusoidal input is described. To calculate the behavior of the comparator in the SOPA system when an external signal is applied, the Dual Input Describing Function (DIDF) is used. For an ideal comparator, the gain of a sinusoidal input signal, which causes an error amplitude B at the input of the comparator in the presence of a limit cycle oscillation with amplitude A, the TSIDF (3.4) can be used and equals [Pie04]

$$\begin{aligned} N_B(A,B) &= \frac{V_{DD}}{\pi B}\left(\frac{B}{A}\right)\ {}_2\mathrm{F}_1\left(\frac{1}{2},\frac{1}{2};2;\left(\frac{B}{A}\right)^2\right) \\ &\approx \frac{V_{DD}}{\pi A} = N(A)/2 \\ &\qquad \text{when } 0 < B \ll A \end{aligned} \tag{3.13}$$

In which ${}_2\mathrm{F}_1(a,b;c;z)$ denotes the 2-1 hyper-geometric function in the variable z with factors (a,b) and (c). It can be calculated as

$$\begin{aligned} {}_2\mathrm{F}_1(a,b;c;z) &= \sum_{n=0}^{\infty} \frac{(a)_n (b)_n}{(c)_n}\frac{z^n}{n!} \\ \text{with } (a)_n &= \frac{\Gamma(x+n)}{\Gamma(x)} \end{aligned} \tag{3.14}$$

Equation 3.13 shows the dithering character of the limit cycle oscillation. As long as the amplitude B is sufficiently smaller than the limit cycle amplitude, the comparator's gain will be independent of the amplitude B. This means that the comparator acts as a linear gain block. The limit cycle oscillation thus linearizes the system for small input signals.

However, from equation (3.9) it is known that the limit cycle oscillation amplitude A is linear proportional to the supply voltage of the comparator. A lowering of the supply voltage, due to a technology migration results in a lower A. As a consequence, the range of input signals for which the linearization effect of the limit cycle oscillation still holds, is severely reduced. This means that it becomes very difficult to reach the distortion specifications of an xDSL system for the desired output power.

Dynamic Range Calculation

In order to estimate the in-band distortion, the second term of 3.13 is also taken into account.

$$N_B(A,B) = \frac{V_{DD}}{\pi\ A} + \frac{V_{DD}B^2}{8\pi\ A^3} + O\left(\frac{B^4}{A^4}\right) \tag{3.15}$$

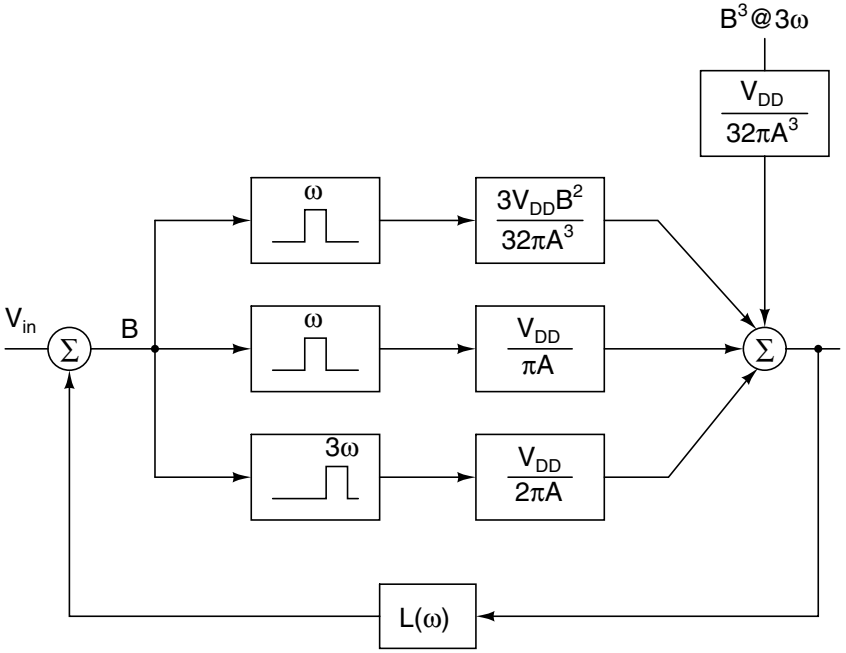


Fig. 3.5. Block schematic of the SOPA for the calculation of the third-order distortion

Since the second gain term is dependent on the input referred error amplitude B, third-order distortion will be generated by $B \cdot N_B(A, B)$, because

$$\sin^3(x) = 3/4 \sin(x) - 1/4 \sin(3x) \tag{3.16}$$

To calculate the third-order distortion of the system, the block schematic of Figure 3.5 is used. The third-order gain factor (upper branch) is split from the first-order gain factors of the error-signal B. The different frequency components (ω and 3ω) are separated from each other by bandpass filters. The describing function for the comparator in the 3ω branch is given by $N(A)/4$. Since in that branch three signals are present (the limit cycle, the signal at frequency ω and its third-order distortion signal at 3ω), the three sinusoid describing function needs to be used. The distortion at three times the frequency ω can be considered as a distortion signal which is injected behind the comparator.

The division in different describing functions of the comparator for different signals and frequencies allows to calculate the third-order distortion term in three consecutive steps:

1. First, the limit cycle signal can be calculated. This is the largest signal in the system, so the other signals, the applied input signal and its third-order

harmonic, can be neglected. For the calculation, the single sinusoid describing function (3.3) is used.

2. Second, the error signal B at the input of the comparator caused by the input signal is calculated. For this the TSIDF must be used, since the limit cycle oscillation cannot be neglected compared to the input signal. The third-order distortion signal can still be neglected, since it is the smallest signal in the system. For the TSIDF the first two terms are taken into account, because a third-order term will also generate a signal at the input frequency (3.15). The calculation of the error signal B is represented in the block scheme by closing the loops with the bandpass filters at frequency ω.
3. Finally, the distortion signal is calculated. The value of this signal is given by the calculated error signal B in step two and the second term of the TSIDF approximation. This distortion signal is assumed to be injected at the output of the comparator and is suppressed by the loop gain of the system which is represented by closing the loop through the bandpass filter at frequency 3ω. The describing function of the comparator is now given by the three sinusoid describing function.

In the following paragraph, a formula for the third-order distortion term will be derived, using these three consecutive steps and Figure 3.5.

First, the limit cycle amplitude is given by equation (3.9). In the next step, the error signal B is calculated at the input frequency ω. This is done by closing the loop through the bandpass filters at ω.

$$\frac{V_{DD}}{\pi\ A} B\ L(\omega) + \frac{3\ V_{DD}}{32\pi\ A^3} B^3\ L(\omega) + B = V_{in} \tag{3.17}$$

Solving this equation for B leads to

$$B = \frac{A\pi}{(V_{DD} L(\omega) + \pi A)} V_{in} + O(V_{in}^3) \tag{3.18}$$

Finally, calculating the loop transfer function for the distortion signal at 3ω gives

$$\mathrm{S} \cdot \mathrm{HD}_3 = \frac{V_{DD}}{32\pi\ A^3 \left(1 + \frac{V_{DD}}{2\pi\ A} L(3\omega)\right)} B^3 \tag{3.19}$$

with S the signal power at the output

$$\mathrm{S} = \frac{N(A)/2}{1 + N(A)/2L(\omega)} V_{in} \tag{3.20}$$

Figure 3.6 shows a comparison of the third-order distortion term calculated by the behavioral model with numerical simulations for a supply voltage of 1.2 V and 3.3 V. A good match can be observed between the model and the simulation. The ratio of the third-order distortion for a 3.3 V on a 1.2 V implementation equals to the square of the ratio of the two supply voltages

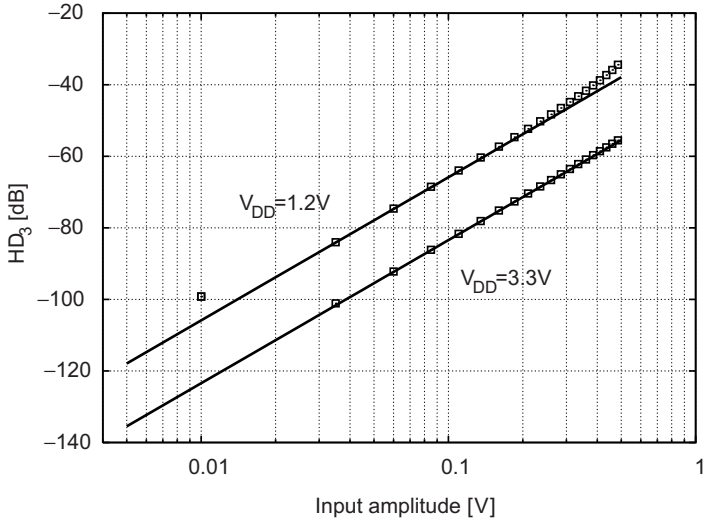


Fig. 3.6. Evaluation of the third-order distortion term (solid line) compared with numerical simulations (squares) for a supply voltage of 1.2 V and 3.3 V

$(3.3/1.2)^2$. This results in a difference of 17.6 dB between the two implementations, which can clearly be seen in Figure 3.6. The limit cycle amplitude is linearly dependent on the supply voltage (3.9). Thus, a lower supply voltage results in a lower limit cycle amplitude. For a 3.3 V implementation A equals 0.26 V and for a 1.2 V implementation A equals 0.10 V. Since the third-order distortion component generated by the non-linear gain of (3.15) decreases with the third power of A, the third-order distortion term is inversely proportional to V_{DD}^2.

A possible solution to circumvent the low limit cycle amplitude caused by the low supply voltage is to increase the order m of the loop filter (3.9). However, the loop gain will drop with increasing m. This is due to a lower linear gain with increasing limit cycle amplitude since the linear gain in (3.15) is inversely proportional to A. Also, the loop gain at the third-order distortion decreases for higher filter orders, because of the higher roll-off of the loop filter at 3ω in (3.19). The combination of these effects results in a weak dependence of the filter order m on the distortion. The results of the stability analysis about the oscillator pulling and the coupling for different filter orders and line conditions described in [Pie04] lead to an optimum filter order of three.

The linearity performance of an aDSL system is expressed in the MTPR. To calculate the MTPR of the SOPA line driver one has to keep in mind that a signal with a power of 20 dBm has to be delivered on a 100 Ω line. This is equivalent with a rms-voltage of 3.17 V. This rms-voltage needs to be multiplied with the CF to determine the full signal swing. To be able to reach these high voltage levels a signal transformer with a transformer ratio

of y is used. Increasing the transformer ratio results in a lower third-order distortion term, since the input signal amplitude can be kept low for the same output power. According to Figure 3.6 the transformer ratio thus needs to be larger for the 1.2 V SOPA system than for the 3.3 V SOPA system to achieve the same distortion levels. However, this results in an increased up-transformed noise. The noise level at the output of the SOPA line driver is multiplied with the transformer ratio. The total noise level at the output, after the transformer, has to be below -100 dBm/Hz (or 3.2 $\mu V/\sqrt{Hz}$) for an aDSL system. An even more important effect of a large transformer ratio is the attenuation of the Rx signals superimposed on the already huge attenuation caused by the line characteristics. As a result, very low signals have to be detected in the Rx-path, leading to extremely difficult noise specifications to meet for the building blocks constructing the Rx-side.

Since a DMT symbol can be assumed to be a signal with an ideal Gaussian distribution of the amplitude, the distortion induced MTPR degradation as function of the rms-voltage σ can be calculated as

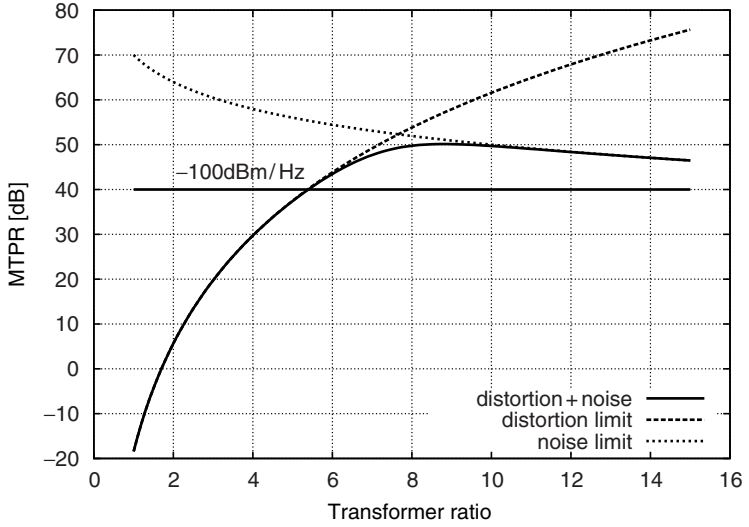
$$\mathrm{MTPR}_{\mathrm{disto}} = 2N \int_0^{\frac{CF\cdot\sigma}{y}} \frac{2y\left(\mathrm{HD}_3(x)\right)^2 \; e^{\left(-\frac{x^2y^2}{\sigma^2}\right)}}{\sqrt{2\pi}\sigma} dx \tag{3.21}$$

N and CF respectively stands for the number of tones and the crest factor of the DMT signal. $\mathrm{HD}_3(x)$ is the distortion function calculated in (3.19). From equation (3.21) and Figure 3.6 it can be concluded that a high MTPR value can be reached when the transformer ratio is increased, since the input signal level can be relaxed for high transformer ratios. It was clear that for the 1.2 V SOPA system the y value should be higher than for the 3.3 V SOPA system to achieve the same MTPR. The maximum achievable MTPR however, is a combination of the distortion and the noise energy σ_n^2 at the output of the SOPA amplifier. Therefore, an approximation of the upper limit of the achievable MTPR of a SOPA system with the noise energy taken into account can be calculated as

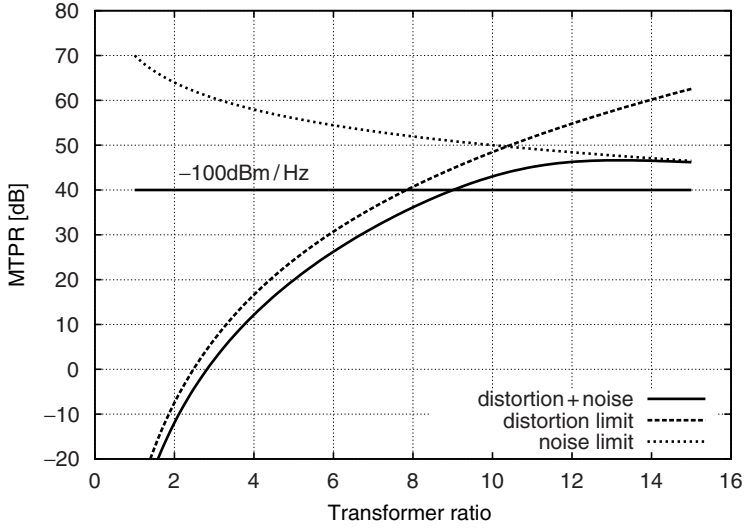
$$\mathrm{MTPR} = 10\log\left(\frac{20\ \mathrm{dBm}}{\mathrm{MTPR}_{\mathrm{disto}}(y) + y^2\sigma_n^2}\right) \tag{3.22}$$

The result of this equation is shown in Figure 3.7 for an output noise level of the line driver of -130 dBm/Hz (or 0.1 $\mu V/\sqrt{Hz}$) and for two different nominal supply voltages, 3.3 V and 1.2 V, of the SOPA system. The horizontal line shows the -100 dBm/Hz output noise specification of an aDSL system. Increasing the transformer ratio, to improve the distortion induced MTPR value, results in an increased up-transformed noise level which causes the MTPR value to drop. From this figure it is clear that the linearity specifications for an aDSL system with a zeroth order SOPA architecture cannot be achieved, unless one is able to reach superior noise specifications of the line driver. The results get even worse if the supply voltage of the line driver is lowered as

can be seen in Figure 3.7(b) for a 1.2 V system. For a low supply voltage the transformer ratio needs to be increased to reduce the distortion. This comes at the cost of an increased up-transformed noise. The combination of these two effects results in a lower upper limit of the MTPR. Moreover, the output currents will increase inverse proportional with the square of the transformer



(a) $V_{DD} = 3.3V$



(b) $V_{DD} = 1.2V$

Fig. 3.7. Evaluation of the upper limit of the achievable MTPR, taken the distortion and noise influences into account

ratio. As a consequence the supply and substrate noise will increase since this is a switching power amplifier. The large currents will also infect the reliability and the efficiency of the line driver. The raised current density will increase the hot carrier generation and the electro-migration in the output stage. The efficiency will be reduced due to increased conduction and switching losses of the driver. The influence of the transformer ratio on the reliability and efficiency of the line driver will be further elaborated in Chapter 4. Another problem is the return signal attenuation, as was already mentioned in the previous paragraph. The larger the transformer ratio, the more the received signal is attenuated. This requires extremely low noise levels of the receiver circuit, limiting the practical use of the line driver. Therefore, the SOPA line driver does not benefit from the continuous technology scaling.

In Section 3.2.5 an improved architecture will be discussed that introduces noise shaping into the system which relaxes the noise specifications. However, the problem of the large transformer ratio due to the low supply voltage still exists. A high voltage output buffer, integrated in the SOPA system will alleviate this problem. The inclusion of the high voltage buffer will be the topic of Section 3.3.

Signal Bandwidth

The signal bandwidth of the SOPA line driver can be described in two different manners [Pie04]. The first concerns the maximum frequency of the input signal. What is the maximum frequency for which the approximation of the SOPA dithering no longer holds? The result is the solution of the following inequality:

$$\tau_{min} \geq \frac{2\sqrt{2}}{2\pi f_{lc}} \approx 3\tau_{lc} \tag{3.23}$$

Or: the maximum bandwidth for a zeroth-order SOPA is a third of the limit cycle frequency. This low OSR is a major advantage compared to other oversampling techniques like discrete time $\Delta\Sigma$-modulation.

The second manner concerns the modulation terms around the limit cycle frequency. Since the input signal modulates the square output wave, inter-modulation tones arise around the limit cycle frequency. The maximum bandwidth can then be seen as the maximum frequency for which the inter-modulation tones within the bandwidth become too large with respect to the noise floor. The i_{th} harmonic band, this is the i_{th} harmonic of the limit cycle frequency with the inter-modulation tones caused by the input signal, can be described by the following equation [Pie04]:

$$s_i(t) = \frac{V_{DD}}{i\pi} \sum_{l=-\infty}^{\infty} \frac{1-(-1)^{i+l}}{2} B(i,l)\cos(\omega(i,l)t + \phi(i)) \tag{3.24}$$

Where

$$\omega(i,l) = i\omega_c + l\omega_{\text{sig}} \tag{3.25}$$

$$B(i,l) = \sum_{p=-\infty}^{\infty} J_p\left(i\frac{\omega_{lc}B^2}{4\omega_{\text{sig}}V_{DD}^2}\right) J_{(l-2p)}\left(i\frac{B\pi}{2V_{DD}}\right) \tag{3.26}$$

$$\phi(i) = i\frac{\pi}{2} \tag{3.27}$$

$$\omega_c = \left(1 - \frac{B^2}{2V_{DD}^2}\right)\omega_{lc} \tag{3.28}$$

B and ω_{sig} are respectively the amplitude and the frequency of the input signal. Figure 3.8 shows the comparison between the power in the inter-modulation tones calculated by the model (depicted as dirac impulses) and by simulation of the output spectrum. Because of the $\left(1-(-1)^{i+l}\right)/2$ factor it can be concluded that around the odd harmonics of the limit cycle oscillation only even harmonic inter-modulation products occur. This is one of the most important properties of a SOPA architecture. For the coupled SOPA system it is shown that the oscillation frequencies become a common mode signal for the output. Since the input signal, applied to the coupled system, is differential, the even harmonics become also common mode at the output. As a result, the odd harmonic bands are not transferred towards the load. This relaxes the output filter specifications, since the energy in the even harmonic bands is much lower than in the odd bands.

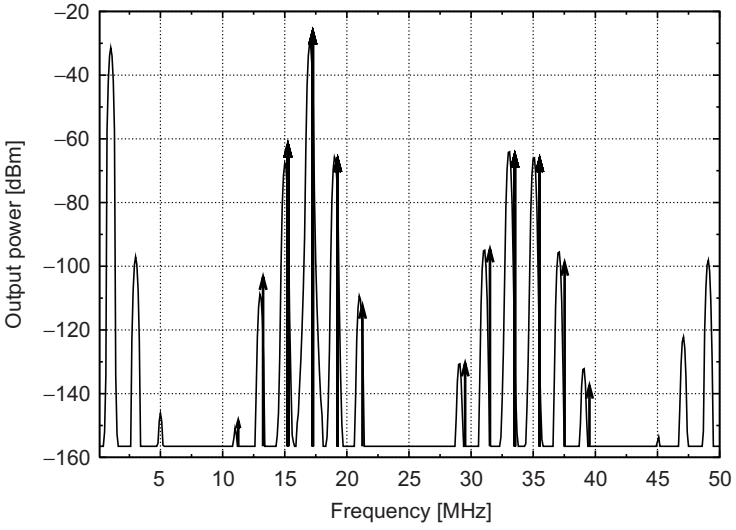


Fig. 3.8. Comparison between the calculated power in the inter-modulation terms (arrows) and the simulated output spectrum (solid line)

3.2.5 Higher Order SOPA Amplifiers

In Section 3.2.4 it was shown that for the zeroth-order SOPA very small input signals are needed to obtain very low distortion ratios. As a consequence, a large transformer ratio is necessary to deliver the desired output power to the load. However, a large transformer ratio severely increases the noise specifications of the line driver. The situation even deteriorates when the supply voltage drops as a result of the technology scaling. In order to relax these specifications, a noise shaping technique like the one used in $\Delta\Sigma$ converters is integrated in the SOPA architecture. The main difference between the SOPA architecture and continuous time $\Delta\Sigma$ converter is the topology of the comparator. The SOPA architecture uses a non-clocked comparator. The output waveform is thus a square wave with a duty cycle modulation whereas in a continuous time $\Delta\Sigma$ converter the output signal is sampled [Pie04].

Figure 3.9 shows a simplified model, with a linearized comparator, to explain the noise shaping technique. $H(\omega)$, the filter in the forward path, represents the transfer function of an n$^{\text{th}}$ order integrator. The relationship between input and output equals

$$\frac{V_{out}}{V_{in}} = \frac{\frac{H(\omega)N(A_{lc})}{2}}{\frac{H(\omega)L(\omega)N(A_{lc})}{2}+1} \tag{3.29}$$

It is assumed that the TSIDF holds for this analysis. Since the limit cycle oscillation fulfills the Barkhausen criterion and $H(\omega)$ has a higher gain for lower frequencies, the term $H(\omega)L(\omega)N(A_{lc})/2$ will always be larger than $1/2$ for frequencies lower than the limit cycle frequency. The input output relation thus can be approximated by a unity-gain function. The transfer function of the distortion term, $d\,(V_{in})$ to the output results in

$$\frac{V_{out}}{d(V_{in})} = \frac{1}{\frac{H(\omega)L(\omega)N(A_{lc})}{2}+1} \tag{3.30}$$

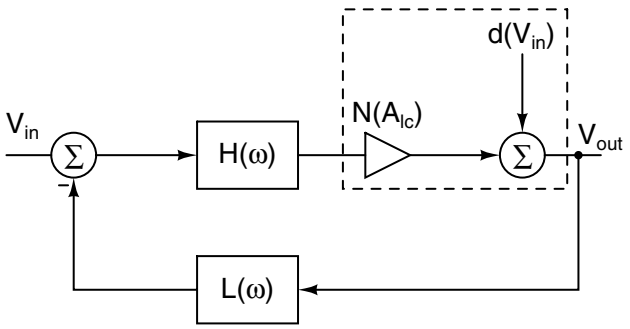


Fig. 3.9. Simplified model of a SOPA with a linearized model for the comparator (dashed rectangle)

The result of this transfer function will tend to go to zero for a high gain of the forward filter $H(\omega)$ and frequencies below the limit cycle frequency. Since a DMT signal contains a large number of tones which are uncorrelated, the distortion distribution to the DMT signal can be approximated as a white noise source σ_n. The output can thus be calculated as

$$\begin{aligned} V_{out} &= \frac{\frac{H(\omega)N(A_{lc})}{2}}{\frac{H(\omega)L(\omega)N(A_{lc})}{2}+1}V_{in} + \frac{1}{\frac{H(\omega)L(\omega)N(A_{lc})}{2}+1}\sigma_n \\ &= \frac{H(\omega)}{H(\omega)L(\omega)+2\ H(\omega_{lc})L(\omega_{lc})}V_{in} + \frac{2\ H(\omega_{lc})L(\omega_{lc})}{H(\omega)L(\omega)+2\ H(\omega_{lc})L(\omega_{lc})}\sigma_n \end{aligned} \tag{3.31}$$

Since $L(\omega)$ is a low pass filter, its gain can be approximated to be 1 for low frequencies. Taking into account that $H(\omega)L(\omega) \gg 2H(\omega_{lc})L(\omega_{lc})$, equation 3.31 can be simplified to

$$V_{out} \approx V_{in} + \frac{H(\omega_{lc})}{H(\omega)}\ \sigma_n \tag{3.32}$$

The output distortion is thus shaped by the inverse of the forward filters. As a result, an integrator is an ideal forward filter for its high in-band gain. In the following, an nth-order SOPA is defined as a SOPA with n integrators in the forward path. In [Pie04], the calculations of the zeroth order SOPA concerning the limit cycle oscillation, the coupling and the forced system are repeated for the higher order SOPA system.

The inclusion of integrators in the forward path of the SOPA architecture relaxes the noise specifications of the line driver. However, the problem of the large transformer ratio still exists. The reduced supply voltage of nanometer technologies results in an increased current density in the driver infecting the reliability and efficiency. Moreover, the large transformer ratio attenuates the return signal which results in extremely hard noise specifications for the receiver circuit.

The next section will describe the influence of the integration of a high voltage output buffer in the SOPA architecture on the behavior model.

3.3 High Voltage SOPA Amplifiers

In this section, the effects of including a high voltage output buffer into the SOPA architecture is described. This section serves also as an introduction to the following two chapters where the design, implementation and measurements of high voltage output buffers in a standard CMOS technology are explained. Figure 3.10 shows the model of a zeroth order SOPA with a high voltage output buffer. The function of the high voltage buffer is to convert the binary output of the comparator to high voltage levels with a voltage gain

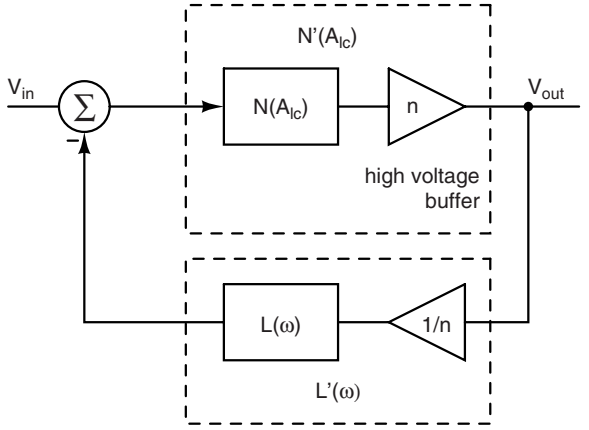


Fig. 3.10. Model of a zeroth-order SOPA amplifier with a high voltage output buffer

factor n. The output of this buffer is fed back to the input of the comparator through the loop filter. The comparator operates at the nominal supply voltage of the technology used. Therefore, the voltage levels of the high voltage output buffer need to be downscaled with at least the same factor n as it upscales the output of the comparator. The division factor is usually taken the same as the multiplication factor. If the voltage division in the loop filter is too large, the loop gain drops which results in an increased distortion.

In the following paragraphs the influence of including a high voltage output buffer into the SOPA architecture on the behavior model is described. It will be shown that the models do not change since the voltage multiplication in the forward path and the voltage division in the feed back path cancel each other out.

Transfer Function

The transfer function of the zeroth-order SOPA becomes now

$$\text{TF'} = \frac{\frac{N'(A)}{2}}{1 + \frac{N'(A)}{2} L'(\omega)} \tag{3.33}$$

With

$$N'(A) = \frac{2nV_{DD}}{\pi A} = n \cdot N(A) \tag{3.34}$$

the single sinusoid describing function of an ideal comparator with an n times V_{DD} supply and

$$L'(\omega) = \frac{1}{n} L(\omega) \tag{3.35}$$

This results then in the following transfer function:

$$\text{TF'} = \frac{\frac{nN(A)}{2}}{1 + \frac{nN(A)}{2}\frac{L(\omega)}{n}} = n \cdot \text{TF} \tag{3.36}$$

Therefore, the inclusion of a high voltage output buffer and as a consequence, the reduction of the loop gain, results in a gain of the input signal with a factor n compared to a basic zeroth-order SOPA. This is a very important aspect since the input signal can now be reduced with this factor n in order to obtain the same output power. The reduction of the input signal amplitude results in better distortion specification as can be seen from Figure 3.6.

Limit Cycle Oscillation

As described in Section 3.2.2 the limit cycle frequency f_{lc} and amplitude A can be found by solving the Barkhausen criterion

$$L'(\omega)N'(A) + 1 = 0 \tag{3.37}$$

With the equations (3.34) and (3.35) this results in

$$L(\omega)N(A) + 1 = 0 \tag{3.38}$$

which is the same equation as if there was no high voltage buffer included. Therefore, the equations (3.8) and (3.9) for the limit cycle frequency and amplitude remain valid and are, as such, not influenced by the voltage multiplication factor n.

Coupling

The high voltage output buffer has also no effect on the coupling of two SOPA systems. The voltage multiplication factor n in the forward path and the voltage division $1/n$ in the loop filter cancel each other out. The r_{out} in equation (3.10) is now the output resistance of the high voltage buffer. It is important that this resistance is low enough to minimize the conduction losses of the driver.

Dynamic Range

The same cancellation effect of the voltage multiplier in the forward path and the voltage division in the feedback path can be seen in the dynamic range calculation of Section 3.2.4. The results in Figure 3.6 do not depend on the voltage multiplication factor n. The main advantage of the high voltage buffer however, is the gain that is introduced in the SOPA architecture. This allows lower input voltage levels for the same output power which results in a lower third-order distortion term. Taking a closer look at the distortion induced MTPR degradation of equation (3.21), the transformer ratio can then be

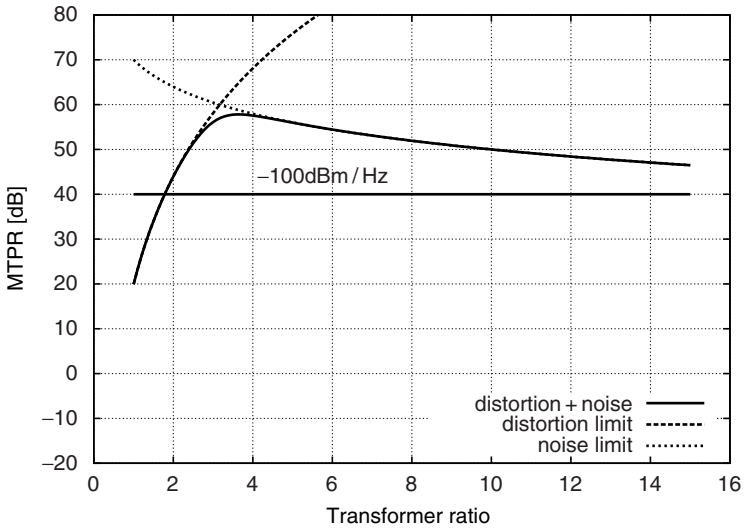


Fig. 3.11. Evaluation of the upper limit of the MTPR for a 1.2V SOPA system with a voltage multiplication of 5

lowered to obtain the same MTPR results. In Figure 3.7(b) this corresponds to a shift to the left of the distortion limit curve. The problem of the 3.3V and especially the 1.2V SOPA system was a low upper limit of the MTPR due to the up-transformed noise. This resulted in the fact that the aDSL linearity specifications could not be met with a basic zeroth-order SOPA architecture.

Figure 3.11 shows the evaluation of the upper limit of the achievable MTPR according to equation (3.22) for a 1.2V SOPA system with a high voltage output buffer resulting in a voltage multiplication factor of 5. The upper limit of the MTPR is increased compared to the 3.3 V and 1.2 V system of Figure 3.7. And, more important, this upper limit is now obtained with a lower transformer ratio. One can see from this graph that the necessary MTPR specification of 55 dB is just met for an output noise level of −130dBm/Hz of the line driver. This figure illustrates that the linearity and noise specifications of an aDSL system can be met with a zeroth-order SOPA if a high voltage buffer is integrated into the architecture. However, to obtain a safe noise and distortion margin a combination of a higher order SOPA with a high voltage buffer has to be used.

The low transformer ratio results in a reduced output current improving the efficiency and reliability. The effect on efficiency and reliability will be further elaborated in Chapter 4. Since the SOPA is a switching amplifier, this will reduce also the supply and substrate noise. Moreover, the noise specifications of the receiver circuit can be relaxed since the return signal attenuation is reduced.

Signal Bandwidth

The calculation of the modulation terms around the limit cycle frequency according to equation (3.24) can still be used under the condition that the input signal levels are reduced with the voltage multiplication factor n. This can intuitively be seen since the high voltage buffer introduces a gain with a factor n.

3.4 Conclusions

A concise overview of the Self-Oscillating Power Amplifier is given in this chapter. The basics of the describing function methodology are mentioned for it gives a good mathematical approximation of the hard non-linear SOPA. Models for the frequency response, distortion and signal bandwidth are derived from a reference model from which every SOPA architecture can be constructed. The models are verified with numerical simulations to prove their usefulness. To visualize the performance degradation of the SOPA architecture in low voltage nanometer technologies, all simulations are performed with a supply voltage of 1.2 V. This will also be the nominal supply voltage for the two SOPA line driver implementations in Chapter 6. It is shown that the linearity specifications of an xDSL system can not be met with the basic SOPA architecture due to the large transformer ratio. Since the output current is inversely proportional to the square of the transformer ratio, the supply and substrate noise will increase. The high current density will also affect the efficiency and the reliability of the line driver. Moreover, the xDSL modem will suffer from large return signal attenuation caused by the transformer ratio. This results in noise specifications for the building blocks in the Rx-path that are impossible to implement. Higher order architectures can relax the noise specifications of the line drivers, but, the problem of a large transformer ratio still exists.

It is demonstrated that the inclusion of a high voltage output buffer into the SOPA architecture improves the distortion and noise specifications because of a lower transformer ratio. Chapters 4 and 5 will discuss the design, implementation and verification of high voltage buffers in a standard CMOS technology compatible with the SOPA architecture. It will be shown that the SOPA xDSL line driver, implemented in a low voltage nanometer CMOS technology, will benefit with a high voltage output stage improving all parameters: linearity, efficiency and reliability.

4

High Voltage Design Considerations

IN Chapter 3 it is demonstrated, by high-level modeling, that the SOPA amplifier does not benefit in terms of distortion and noise from the low supply voltages originating from nanometer CMOS technologies. It was also proved that these low voltage issues can be circumvented by operating the critical path of the SOPA line driver, the power delivering output stage, at higher voltages. In this chapter, the influence of low supply voltages on the SOPA line driver design will be further elaborated in terms of efficiency and reliability and possible solutions will be discussed.

The chapter is divided into two major parts. The first part starts with an introduction on Moore's Law, which predicts already for more than 40 years the CMOS scaling trend. A pertinent question is how this continued reduction in feature size influences the operating characteristics and properties of the MOS transistor, and indirectly, the critical design metrics, such as switching frequency and power dissipation. Different CMOS scaling laws are explained and the influence of scaling on switching amplifiers in general, and the SOPA design in particular, is discussed. It will be shown that the efficiency and reliability of the SOPA line driver will seriously degrade due to the low supply voltage. Therefore, a high voltage output stage becomes necessary to improve the performance of the SOPA line driver. One way to deal with high voltages is to use customized CMOS technologies. However, these technologies can only be integrated in a digital CMOS technology at a higher cost, since extra process steps and mask sets are necessary. Moreover, in nanometer CMOS technologies, the prices of mask sets are increasing exponentially with every technology migration. In this book a solution in a standard CMOS technology is chosen, since it leads to a full integration of the high voltage line driver within the AFE resulting in a compact and low cost single chip solution.

The second part describes this principle of a high voltage solution in a standard low voltage CMOS technology. Through the calculation of the power dissipation of the output stage, a comparison is made between a high voltage solution in a mainstream low voltage technology and a solution in a technology from a previous generation with a higher nominal supply voltage.

It will be shown that the stacking of standard low voltage transistors is more advantageous in terms of power dissipation and integration prospects.

4.1 CMOS Scaling

4.1.1 Introduction: Moore's Law

In a section about technology scaling, it is almost unthinkable not to mention the famous paper in the microelectronic field: "Cramming more components onto integrated circuits" by Gordon E. Moore [Moo65]. *The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer.* Under the assumption that complexity is proportional to the number of transistors, regardless of what they do, this statement, better known as Moore's Law is already valid for more than 40 years for the CMOS technology. Nowadays, several millions of CMOS transistors can be integrated on a single chip and, as such, it becomes the cheapest technology available today.

The evolution in CMOS technology is motivated by decreasing price-per-performance for digital circuitry. Its pace is determined by Moore's Law [Nau05]. The reason that Moore's Law is still valid today, is probably due to the reaction of the technology industry on this law to make it come true. This can also be seen in the International Technology Roadmap for Semiconductors (ITRS). ITRS conferences are held twice each year. The objective of the ITRS is to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices, thereby continuing the health and success of this industry. Anyhow, the continuous scaling is a blessing for the increasing integration density of the VLSI circuits and the low power requirements of complex signal processing applications.

4.1.2 CMOS Scaling Laws

According to Moore's Law, the technology migrates from one node to another every two years. Scaling of the devices has an influence on the performance of every component in the system. The design of analog circuits will speed up if the right choice of technology is made from the start. Scaling rules give the circuit designer insight in the evolution of the technology parameters. This provides him a guideline for the right technology choice.

In order to design a new device suitable for smaller values of L, the device is scaled by a transformation in three variables: dimension, voltage and doping.

Table 4.1. CMOS scaling laws

Parameter	Relation	Full scaling	General scaling	Fixed voltage scaling
$W,\ L,\ t_{ox}$		$1/S$	$1/S$	$1/S$
V_{DD},		$1/S$	$1/U$	1
N_{SUB}		S	S^2/U	S^2
C_{ox}	$1/t_{ox}$	S	S	S
β	$\mu C_{ox} W/L$	S	S	S
C_{gate}	$C_{ox} WL$	$1/S$	$1/S$	$1/S$
R_{on}	$1/(\beta V_{DD})$	1	U/S	$1/S$
f_T	g_m/C_{gate}	S^2	S^2	S^2
C_{gate} @ $fixed\ W$	$C_{ox} L$	1	1	1
R_{on} @ $fixed\ W$	$L/(\mu C_{ox} V_{DD})$	$1/S$	U/S^2	$1/S^2$

Table 4.1 gives an overview of three different CMOS scaling rules [Rab96]: Full scaling, General scaling and Fixed voltage scaling.

The fixed voltage scaling was the dominant scaling law for gate lengths longer than 0.7 μm. When going to smaller dimensions, the supply voltage needs to scale with the gate length and the oxide thickness to avoid reliability issues like hot carriers and oxide breakdown.

For deep-submicron CMOS technologies, the full scaling has to be used. In full scaling, all of the horizontal and vertical dimensions are scaled with the power supply to maintain constant electric fields throughout the device.

As scaling continues towards nanometer dimensions, the nominal supply voltage cannot scale with the technology dimensions. This departure from the full scaling model is motivated by the following points [Rab96]:

- Some of the intrinsic device voltages, such as the silicon bandgap and the built-in junction potential, are material parameters and thus cannot be scaled.
- The scaling potential of the transistor threshold voltage is limited. Making the threshold too low makes it difficult to turn off the device completely.

Therefore, a more general scaling model is needed with dimensions and voltages scaled independently. In this general scaling model device dimensions are scaled by a factor S, while voltages are reduced by a factor U. When the voltage is held constant, $U = 1$, the scaling model reduces to the fixed voltage model.

For the three different scaling laws described in Table 4.1, the device dimensions are scaled by a factor S. By comparing different CMOS technology nodes (..., 0.25 μm, 0.18 μm, 0.13 μm, ...) the factor S equals roughly $\sqrt{2}$.

4.1.3 Influence of CMOS Scaling on Switching Amplifiers

Important parameters for switching type power amplifiers like the SOPA amplifier are the gate capacitance C_{gate} and the on-resistance R_{on}, since they respectively determine the switching and conduction losses. Figure 4.1(a) shows transfer characteristic of an nMOS switch. When the transistor is in the cut-off region, no current flows through the device and the switch is off. When the transistor is in the linear region, the switch is on. A transistor in the linear region acts as a linear resistor as can be seen in Figure 4.1(b). This figure shows the $I_{DS} - V_{DS}$ characteristic of an nMOS transistor for different values of V_{GS}. One can clearly see the linear behavior of these curves near the origin. Using a first order CMOS transistor model, the on-resistance is given by

$$R_{on} = \frac{1}{\mu C_{ox} W/L \, (V_{GS} - V_T - V_{DS})} \tag{4.1}$$

The input- or gate capacitance of a CMOS transistor equals

$$C_{gate} = C_{ox} W L \tag{4.2}$$

Looking at the constant field scaling law, C_{gate} @ fixed W remains unchanged and R_{on} @ fixed W is reduced with a factor $\sqrt{2}$ for scaling the technology to the next node. This is verified by simulating these parameters for CMOS transistors in the linear region with a fixed width of 1000 μm and minimum length in four consecutive technology nodes (0.35–0.13 μm). Figure 4.2(a) shows the evolution of the on-resistance in function of the gate length. A scaling factor

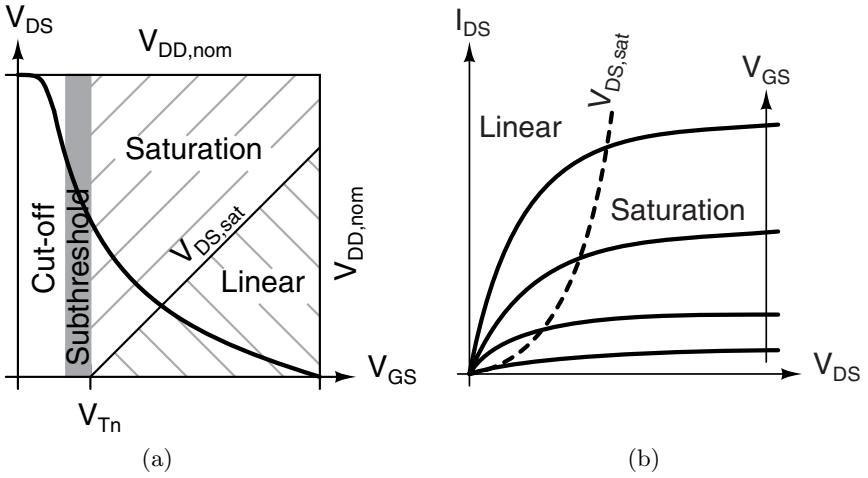
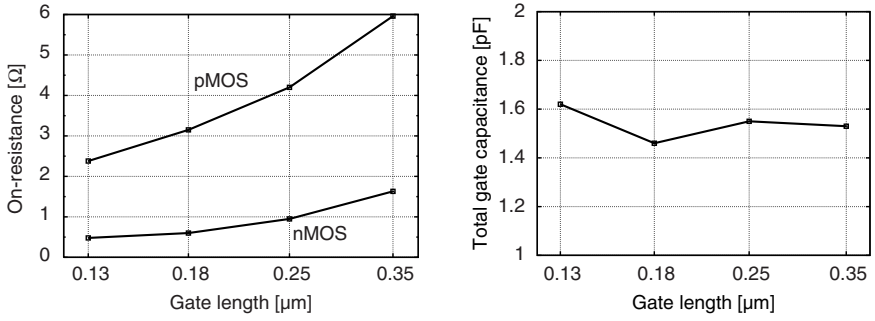


Fig. 4.1. Transfer characteristic of an nMOS switch (a) and the $I_{DS} - V_{DS}$ curve of an nMOS transistor (b)



(a) On-resistance (b) Total gate capacitance

Fig. 4.2. Simulation of the on-resistance and total gate capacitance of submicron CMOS technologies for a 1000 μm wide transistor in the linear region

of $1/\sqrt{2}$ can be observed. Figure 4.2(b) shows the total gate capacitance in function of the gate length. The gate capacitance remains more or less constant at 1.55 pF for a minimum length CMOS transistor with a fixed width of 1,000 μm. The fact that the value of C_{gate} is not changed, still results in a reduction of the switching losses since the dynamic power dissipation $P_{dyn} = fV_{DD}^2C$ is quadratic dependent on the supply voltage which does scale with the technology. The lowering of R_{on} results in a reduction of the conduction losses, since the static power dissipation equals $P_{stat} = I_{rms}^2 R_{on}$ with I_{rms} the rms current drawn from the supply voltage V_{DD}.

From the previous paragraph, one can conclude that scaling is beneficial for switching power amplifiers, since the on-resistance and the voltage is scaled. However, while the reduced voltage supply of constant field scaling is an advantage for the power dissipation of digital circuits, this is not the case for power delivering analog circuits. The output levels of a power amplifier depend on the maximum applicable supply voltage. Since $P_{out,max} = V_{DD}I_{rms} = V_{DD}^2/R = I_{rms}^2 R$, a migration of the technology to the next node results in a decrease of the load resistance with a factor 2 and an increase of the output current with a factor $\sqrt{2}$. The increased current density in the power amplifier affects its efficiency and reliability. For most applications, the load resistance has a fixed value. Therefore an impedance matching network has to be used to convert the reduced load resistance to the required value, which introduces extra losses into the system. For an xDSL system the line driver has to deliver 20 dBm to a 100 Ω twisted pair telephone line. In this system, the line transformer performs the function of the impedance matching network.

CMOS power amplifiers suffer the most from the low supply voltage of nanometer technologies. In [Nau05], however, two technology issues are described concerning CMOS scaling, which are also of major importance in

analog CMOS design. The first is the lower output conductance with newer CMOS technologies and as a result a lower voltage gain. Therefore, to achieve sufficient gain, circuit techniques such as current bleeding [Yao04] or gain boosting [Bul90, Fla96] are necessary. A disadvantage of these techniques is that they affect the stability of the circuit. A second technology issue is the gate-leakage. In nowadays ultradeep-submicron and nanometer CMOS technologies gate-leakage may be a serious problem for analog circuit design because [Nau05]

- It poses a lower limit to the usable frequency range for integrator circuits, e.g. for filters and sample & hold-circuits.
- It introduces a strong relation between DC-current gain and transistor length, which effectively limits accuracy.
- Its mismatch introduces a new limit to achievable accuracy.
- It results in shot-noise which is equivalent to the noise from the base-current in bipolar transistors.

While CMOS scaling is mainly driven by the low power requirements of complex digital signal processing applications and the increasing integration density of VLSI circuits, analog circuits do not benefit from this (voltage) scaling. However, there is a ray of hope. According to the prediction of the ITRS [ITR05], the supply voltage remains more or less constant at 1 V from the 90 nm technology on. Figure 4.3 shows the evolution of the nominal supply voltage in function of the minimum gate length. Nevertheless, this is more than unsatisfactory to design highly efficient and reliable power amplifiers. This statement is emphasized in the next section where the influence of technology scaling on the SOPA performance is discussed.

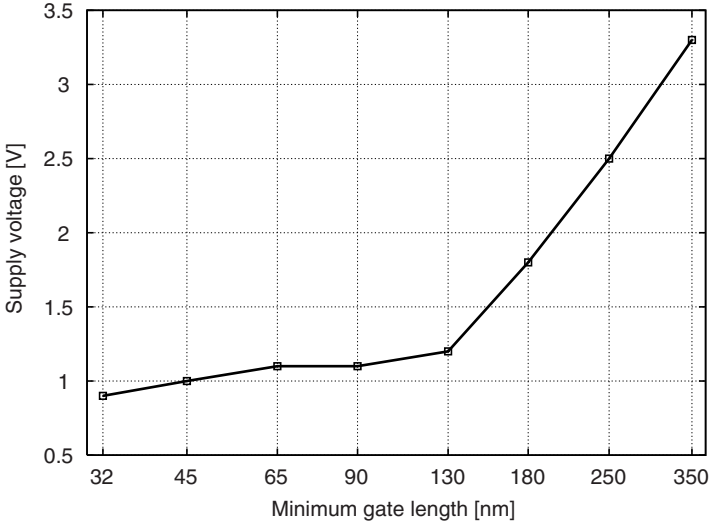


Fig. 4.3. Nominal supply voltage in function of the minimum gate length of the technology plotted on a logarithmic x-scale

4.1.4 Influence of CMOS Scaling on SOPA Design

In this section the influence of CMOS technology scaling on the SOPA design is discussed. As the SOPA is a power amplifier, the scaling of the supply voltage has the largest impact on its design parameters and more in particular, the parameters of the power delivering output stage. The voltage requirements of the output stage are derived for a basic aDSL system. From these voltage requirements the dependency of the transformer ratio, the load resistance and rms output current on the nominal supply voltage of the technology can be calculated. Abstraction of noise and distortion considerations in function of the supply voltage is made since it was discussed in Section 3.3.

Requirements of a SOPA Line Driver

An aDSL system requires 20 dBm or 100 mW being delivered to a 100 Ω twisted pair telephone line. The rms voltage needed to deliver this 100 mW is thus 3.16 V. The necessary CF of an aDSL system is typically set at 15 dB which equals a factor of 5.6. The peak voltage is thus 17.7 V. In Section 3.2.4 it was described that the limit cycle amplitude should be higher than this peak voltage. For a practical implementation, a factor of 3 has been chosen for the maximal voltage range. Since two SOPAs are differentially coupled through the line transformer, the total required voltage has to be divided by 2. A single SOPA has to be able to cope with a maximum voltage of 26.6 V. With these numbers, the output driver of the SOPA can be designed following the rules of a regular class D amplifier.

According to equation (3.23) the limit cycle frequency has to be at least three times larger than the bandwidth of the aDSL system in order to benefit from the dithering effect. It is assumed that the process technology will limit the maximum switching frequency. From this point of view, the SOPA benefits from the technology scaling, since the cut-off frequency f_t of a single transistor is scaled with a factor S^2.

Relationship Between V_{DD} and the Output Stage Parameters

Figure 4.4 shows a schematic representation of a single-ended SOPA. R_L, y and R respectively represent the load resistance, the transformer ratio and the resistance seen by the SOPA amplifier after transformation by the impedance matching network, which is, in this case, the line transformer. I_{rms} is the rms current that the line driver has to deliver in order to provide an average output power of 100 mW. R_{on} equals the on-resistance of the output buffer and nV_{DD} is the supply voltage with V_{DD} the nominal supply voltage of the used technology. n is the voltage multiplication factor, which was introduced in Section 3.3. The implementation of a device or a series of devices together that can withstand a voltage of nV_{DD} is the topic of Sections 4.1.6 and 4.2.

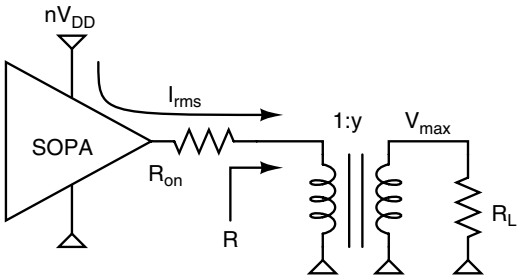


Fig. 4.4. Schematic of a single-ended SOPA architecture. R_{on} is the on-resistance of the output buffer

The following set of equations determine the transformer ratio, the load resistance after transformation and the rms current.

$$y \approx \frac{V_{max}}{nV_{DD}} \tag{4.3}$$

$$R = \frac{R_L}{y^2} = \frac{100\Omega}{y^2} \tag{4.4}$$

$$I_{rms} = \sqrt{\frac{P_{out}}{R}} = \sqrt{\frac{100mW}{R}} \tag{4.5}$$

With $V_{max} = 26.6V$, the maximum voltage that the SOPA has to deal with. For the calculation of the transformer ratio, the voltage drop over R_{on} is ignored. These equations result in the following relationship:

$$n \nearrow \Rightarrow\ y \searrow \Rightarrow\ R \nearrow \Rightarrow\ I_{rms} \searrow \tag{4.6}$$

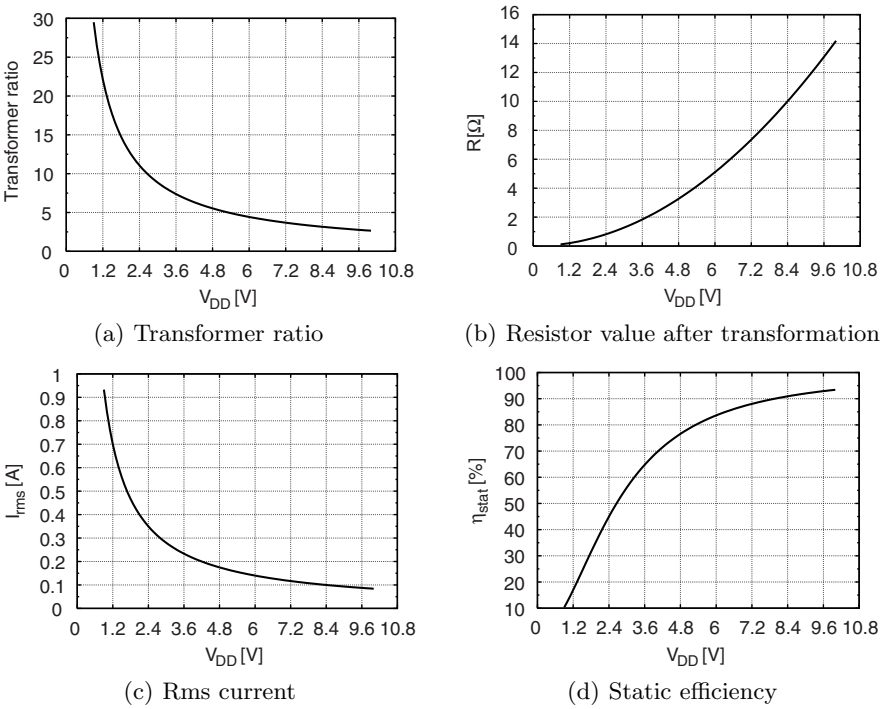
Increasing the supply voltage results thus in an increased load resistance, seen by the SOPA amplifier and hence a decreased rms current. Figure 4.5 shows a graphical representation of the relationships stated by equation (4.6). The nominal supply voltage is set at 1.2 V for a 0.13 μm CMOS technology. The x-scale is divided into multiples of V_{DD} to show the dependency on the voltage multiplication factor n. Figure 4.5(d) depicts the static efficiency η_{stat} of the class D type output buffer in function of its supply voltage. The static efficiency is defined as

$$\eta_{stat} = \frac{P_{out}}{P_{total}} = \frac{P_{out}}{P_{cond} + P_{out}} \tag{4.7}$$

Only the conduction losses (P_{cond}), which are caused by the voltage drop over R_{on}, are taken into account for the static efficiency.
With:

$$P_{out} = I_{rms}^2 R \tag{4.8}$$

$$P_{cond} = I_{rms}^2 R_{on} \tag{4.9}$$



(a) Transformer ratio

(b) Resistor value after transformation

(c) Rms current

(d) Static efficiency

Fig. 4.5. Relationship of V_{DD} or n on the transformer ratio, R, rms current and the static efficiency

This results in a simple resistive division between the on-resistance of the output buffer and the transformed load resistance:

$$\eta_{stat} = \frac{R}{R + R_{on}} \tag{4.10}$$

Equations (4.6), (4.10) and (4.7) show that an increased supply voltage results in a higher static efficiency and thus lower conduction losses for the same on-resistance of the output buffer. One could also lower the on-resistance to reduce the conduction losses. However, lowering the on-resistance will result in increased switching losses which will degrade the overall efficiency. Section 4.2 will clarify the relationship between the conduction and switching losses. For Figure 4.5(d), R_{on} was set at 1 Ω. According to Figure 4.2(a), this is a reasonable choice to restrict the width of transistors.

From Figure 4.5 one can conclude that SOPA architectures with a supply voltage lower than 3.6 V (or a voltage multiplication factor lower than three) become impractical and highly inefficient. This is further argued by the following statements:

- Supply voltages lower than 3.6 V require a transformer ratio larger than 7.4. The output signal of the line driver is up-transformed with a factor

7.4, but the return signal is attenuated with the same factor. This puts severe noise requirements on the receiver circuit. From Figure 3.7 it is also known that a large transformer ratio results in high output noise levels and so lowers the MTPR of the SOPA line driver.

- For supply voltages lower than 3.6 V, a resistance lower than 1.8 Ω has to be driven by the line driver. This results in an rms current of more than 236 mA to obtain the average output power of 100 mW. High current densities lead to long term reliability issues like hot carrier degradation an electro-migration, which are explained in the next section. The only solution to prevent this is to increase the transistor's dimensions. But, this will result in an intolerable increase in dynamic power losses, as will be seen later on.
- Due to the low resistance that the amplifier has to drive, the static efficiency and as a consequence the total efficiency will be lower than 64% for an on-resistance of 1 Ω of the output buffer.

It is clear that the SOPA line driver benefits from a high voltage output stage. However one has to take in mind that with the arrival of nanometer technologies, the supply voltage has dropped to nearly 1 V. Therefore, the complexity of the output buffer will increase dramatically if a supply voltage higher than 3.6 V is wanted.

4.1.5 Reliability Issues

CMOS foundries are strongly motivated to mitigate any physical mechanism that may cause Integrated Circuits (IC) to fail due to some know physical failure mechanism within a specific reliability target. That target is typically in the neighborhood of 20–40 years. This large target time to fail is chosen because the physical wear out mechanisms are governed by a stochastic process with a random distribution of failure times. The choice of fail time target is selected such that a consumer product nominal service lifetime (typically less than 10 years) will fall somewhere far out in the tails of the failure mechanism probability distribution function.

In order to achieve this goal, a foundry must understand the physics of each failure mechanism and identify any wafer processing step that may detrimentally influence each mechanism. Once the wafer processing is optimized for maximum lifetime set by each physical mechanism, the foundry develops design rules intended to prevent IC designers from over-stressing the devices and cause the expected lifetime to fall below foundry targets. These design rules will be embodied in the form of maximum operating voltage, transistor channel length constraints for service under certain bias conditions, maximum current per unit line width in metal interconnects, maximum current per contact or via and certain constraints upon interconnect layout of very wide metal lines. Failure to comply with the reliability design rules may lead to unpredictably shorter IC lifetime.

There are a number of physical failure mechanisms that can affect the reliability of a CMOS IC. The next paragraphs will outline the most common physical failure mechanisms. They can be divided into two groups: long-term failure mechanisms and breakdown mechanisms. Long-term failure mechanisms, such as Time Dependent Dielectric Breakdown (TDDB), Hot Carrier Degradation (HCD) and electro-migration, slowly degrade the device parameters until failure of the IC. The device degradation can be: a shift in the threshold voltage V_T, a shift in the transconductance g_m and a shift in the subthreshold slope ΔS. On the other hand, most of the breakdown mechanisms are destructive and result in an immediate and permanent failure of the IC.

A common general misconception is that the physics of failure is thoroughly understood and that mathematical models exist that permit designers to tune IC reliability to their specific product lifetime. Most mathematical models for physical failure mechanisms are based upon observations of accelerated reliability tests performed at elevated temperature and at higher than normal voltage or current density. These accelerated tests can produce some unrealistic stresses upon the materials resulting in failure statistics that do not represent stresses experienced at nominal operating conditions. There is great temptation to extrapolate accelerated test results, using these mathematical models developed from accelerated test data, back to "at-use" conditions to predict IC reliability in typical applications. [MOS].

TDDB: Time Dependent Dielectric Breakdown

TDDB is wear-out of the insulating properties of silicon dioxide in the CMOS gate, leading to the formation of a conducting path through the oxide to the substrate. With a conducting path between the gate and the substrate, it is no longer possible to control current flow between the drain and source by means of the gate electric field. TDDB lifetime is strongly affected by the number of defects in the gate oxide produced during wafer fabrication.

TDDB occurs at all gate voltage bias conditions. The goal of the foundry is to trade off gate oxide thickness with operating voltage specifications to achieve both speed and lifetime targets for the technology. The lifetime of a particular gate oxide thickness is determined by the total amount of charge that flows through the gate oxide by tunneling current. [MOS].

HCD: Hot Carrier Degradation

Carriers in a channel traveling from source to drain experience an electric field magnitude that varies depending upon the transistor bias conditions. As the transistor channel is formed at low drain-source voltage the electric field is uniformly divided over the length of the channel by the presence of the inverted channel. When the drain-source voltage is increased the channel begins to pinch off. This principle is shown in Figure 4.6. In Figure 4.6(a) the

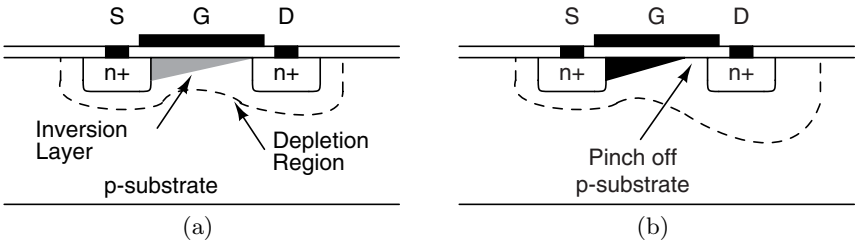


Fig. 4.6. Cross section of an n-MOS transistor. (a) shows the inversion layer of a transistor in saturation. (b) shows a pinched off inversion layer due to a large drain-source voltage

transistor is in saturation and the inversion layer ends at the drain side. In Figure 4.6(b) the drain voltage is increased and the inversion layer is pinched off. A point is reached when the electric field is largely confined to the region between the pinched-off channel edge and the drain diffusion. This causes the magnitude of the electric field to reach high values and causes the channel carriers to accelerate through the pinched off region reaching a high velocity that is greater than thermally limited diffusion drift velocity, hence the term "hot carrier". If a channel hot carrier collides with a crystal atom near the drain region, it may produce an electron-hole pair in an impact ionization event.

Carriers generated by impact ionization are subjected to the same large electric field that had lead to their formation. In an n-channel transistor, for example, the electrons are accelerated to the drain while the holes are driven into the substrate by the gate electric field. Energy imparted to the carriers formed in an impact ionization event can cause electrons (and holes) to be scattered toward the gate oxide interface and the substrate resulting in gate and substrate currents respectively. This substrate current is a measurable quantity that serves as an indicator of the amount of impact ionization that is occurring at a specific set of bias conditions. As with TDDB, these scattered carriers can generate interface states that will degrade channel carrier mobility and reduce the transconductance of the transistor. Scattered electrons with the highest energy may be injected into the gate oxide producing a trapped charge that will also degrade the transistor performance [MOS].

Hot carrier damage rate is highest in a transistor with channel length at minimum design rule length and when drain-source voltage is maximum permitted voltage while the gate-source voltage is around of half of the drain-source voltage [Sak86, Leb96].

Electro-migration

Electro-migration refers to the gradual displacement of the metal atoms of a conductor as a result of the current flowing through that conductor. The process of electro-migration is analogous to the movement of small pebbles in a stream from one point to another as a result of the water gushing through the pebbles.

Because of the mass transport of metal atoms from one point to another during electro-migration, this mechanism leads to the formation of voids at some points in the metal line and hillocks or extrusions at other points. It can therefore result in either: an open circuit if the void formed in the metal line becomes big enough to sever it; or a short circuit if the extrusions become long enough to serve as a bridge between the affected metal and another one adjacent to it. [Sil].

As a rule of thumb to prevent the electro-migration process, a width of 1 μm per 1 mA DC current for the metal lines is used.

Breakdown Mechanisms

The previous sections described physical mechanisms that cause long-term reliability problems, resulting in a slow degradation of the devices. When the bias voltages are pushed beyond the voltage limits or when the devices are scaled down without reducing the supply voltage, destructive breakdown mechanisms can occur [Bal99].

Junction Breakdown:

The electric field in a reverse biased p-n junction increases with increasing reverse bias. At large electric fields, mechanisms become operative that break down the junction and a large reverse current flows through the junction. The most important physical mechanism leading to junction breakdown is avalanche breakdown.

As described in the hot carrier degradation section, if a channel hot carrier collides with a crystal atom, it can generate an electron-hole pair by impact ionization. In turn, the generated electron-hole pair can maintain the impact ionization if it acquires enough energy from the electric field across the channel. Avalanche breakdown is then defined as the condition under which the impact ionization rate becomes infinite. As a result of such avalanche multiplication, the reverse diode current increases dramatically with increasing reverse bias over the junction. This is shown in Figure 4.7. At a certain voltage V_{BD} the current reaches infinity. This condition is called breakdown. For a mainstream 130 nm CMOS technology the breakdown voltages for different types of junctions are shown in Table 4.2.

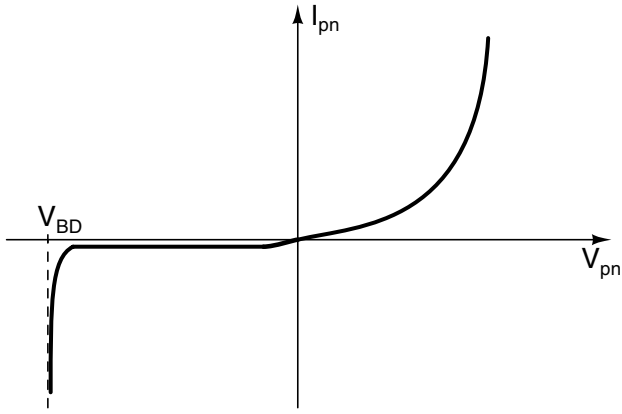


Fig. 4.7. p-n junction current-voltage characteristic showing avalanche multiplication and breakdown

Table 4.2. Junction breakdown voltage

	n+/p-well	p+/n-well	n-well/p-substrate
V_{BD}	10 V	−10 V	14.5 V

Gate Oxide Breakdown:

Avalanche breakdown is a breakdown mechanism in the silicon part of the MOS Field Effect Transistor (MOSFET). Gate oxide breakdown is also possible if the voltage across the oxide (drain-gate or gate-source) is pushed beyond the supply voltage limit. Such a bias condition would first lead to channel hot carrier effects. If the stress condition is further increased, the oxide integrity degradation may cause catastrophic failure.

In modern standard CMOS technologies, the gate oxide can withstand electric fields as high as 1.2 V/nm before breaking down instantaneously [Bal99]. Such dielectric strength is only possible in SiO_2 films that are defect-free, which is unfortunately not always the case. To calculate the absolute maximum rating, which corresponds to the maximum voltage value that can be applied to a minimum gate length device without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown), an electric field strength of 1.0 V/nm is taken. For a 130 nm CMOS technology with an oxide thickness of 2.3 nm this voltage value becomes 2.3 V. However, one has to keep in mind that this voltage will definitively degrade the MOS parameters and will affect the reliability of the device.

One of the goals in this work is to design high voltage circuits in mainstream CMOS such that the voltage over the gate oxide never crosses the nominal supply voltage of the used technology. In this way, the single device

as well as the whole circuit meet the reliability performances. For the 130 nm CMOS technology the nominal supply voltage equals 1.2 V.

4.1.6 Customized Silicon Technologies

One way to achieve higher breakdown voltages is to modify the technology or to use device techniques. In this section, only "customized" technologies based on the CMOS technology are discussed, since the increasing analog and digital complexity of the applications has pushed the technology to more CMOS compatibility and to lower dimensions. Three commonly used CMOS-based high voltage devices are described in this section: Thick Oxide, Laterally Diffused MOS (LDMOS) and Vertical integrated Diffused MOS (VDMOS). The roadmap of these customized technologies also follows Moore's Law but due to the limited market size and the very high safety requirements, the roadmap is roughly two generations behind the mainstream CMOS roadmap [Cas04]. And as the doping levels increase by scaling to the next technology node, integration of high voltage devices in deep-submicron or nanometer CMOS technologies becomes less straightforward.

An alternative solution is the stacking of mainstream CMOS devices to tolerate the high supply voltage. No extra process steps or mask sets are necessary, which makes this solution very attractive in terms of cost and integration prospects. The stacking of standard CMOS transistors is further elaborated in Section 4.2.

At this moment, there is a large architectural, structural and material diversity in high voltage MOS devices. Only a concise explanation of basic versions of these devices is given, since one of the goals in this work is a design in a mainstream CMOS technology without the use of specialized technologies.

Thick Oxide

Increasing the oxide thickness of a transistor is by far the most simple method to increase its breakdown voltage and to remain compatible with standard CMOS. The thick oxide device can be seen as a device from a previous generation implemented in an advanced technology. These devices are primarily used in I/O buffers of digitals circuits where low power consumption is combined with high voltage interface circuits.

LDMOS: Laterally Diffused MOS

The LDMOS is an asymmetric power MOSFET designed for low on-resistance and high blocking voltages. These features are obtained by creating a diffused p-type channel region in a low-doped n-type drain region. The low doping on the drain side results in a large depletion region with a high breakdown voltage [Zeg04]. The channel and the source of this transistor are made in

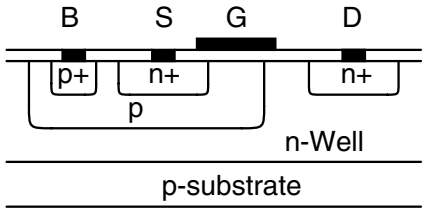


Fig. 4.8. Simplified cross section of an LDMOS

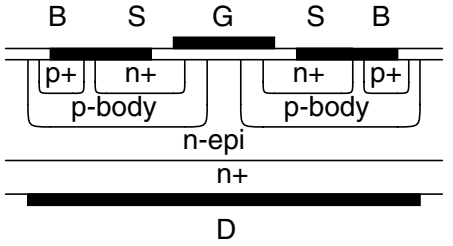


Fig. 4.9. Simplified cross section of an VDMOS

two successive diffusion steps. This is the reason these devices are also called Laterally Double Diffused MOS (LDDMOS). These two diffusion steps can be defined with the same mask, which results in a short channel with high current handling capabilities. A typical cross section of an LDMOS is shown in Figure 4.8.

VDMOS: Vertical Integrated Diffused MOS

The vertical double diffused MOS structure fuses together the concept of vertical power structures and the one of lateral double diffusion. Figure 4.9 shows a simplified cross section of the VDMOS. The channel length does not depend on the resolution of the photolithography, but on the control of the lateral spreads of successive phosphorus and boron diffusions through the same oxide window [Ang04]. The drain current is vertically supported by the n-epilayer. The current flows laterally from the source through the channel, parallel to the silicon surface, and then turns to a right angle to flow vertically down through the drain epilayer to the substrate and the drain contact. The channel length can be controlled to submicrometer dimensions. Because of the relative doping concentrations in the diffused p-channel region and the n-epilayer, the depletion layer extends down in the epilayer rather than laterally into the channel, resulting in a large breakdown voltage.

As the maximum impact ionization is located in the bulk of the silicon, away from the Si/SiO_2 interface, it is believed that VDMOS transistors are more robust against power transients and Electrostatic Discharge (ESD) pulses than LDMOS devices [Cas04]. However, the VDMOS does not match

low voltage MOSFETs as the LDMOS where the drift extension is made lateral, the drain is placed at the surface and the current flows in the lateral direction. Therefore the LDMOS is the better candidate for building hybrid high/low voltage circuits from the integration point of view.

4.2 Stacking Devices: The High Voltage CMOS Solution

4.2.1 Introduction

The devices discussed in the previous section all use modifications of a standard technology to handle high supply voltages. They can be integrated in a mainstream CMOS technology, but, at a higher cost, since extra mask sets and process steps are required. However, there exists an alternative low-cost solution by using only standard CMOS devices. The principle is shown in Figure 4.10. The maximum voltage across the terminals of a transistor is limited by its nominal supply voltage such that the expected lifetime of the device falls within the foundry targets. If two or more transistors are stacked, which means that the source of one transistor is connected with the drain of the next one, the drain-source voltages add up to a multiple of the nominal supply voltage. In Figure 4.10(b) an example of two stacked devices is given. The drain-source voltage of a single device is limited by V_{DD}, but the resulting drain-source voltage for two stacked devices, from the drain of the uppermost device to the source of the lowermost device can rise up to two times the nominal supply voltage without affecting the transistors reliability. Needless to say that the gate biasing of these devices becomes extremely important. After all, during operation, each transistor has to be biased in such a way that the voltage across its terminals remains within the nominal supply voltage.

To limit the gate-bulk voltage of stacked transistors, their source and bulk terminals are shorted. Since the sources and thus also the bulks of these transistors can raise to multiples of the nominal supply voltage, the use of a triple well technology is advisable. However, Chapter 5 will reveal that a design in a twin well technology is also possible if the substrate currents can

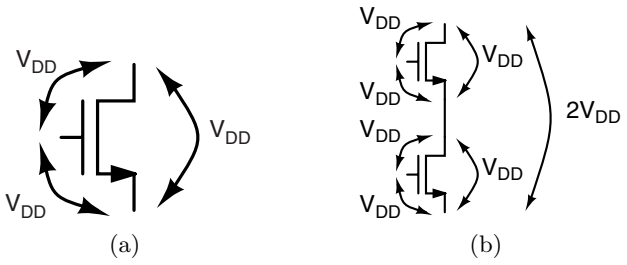


Fig. 4.10. Principle of stacking standard CMOS devices

be accurately modeled. A consequence of this source bulk short is that the number of transistors that can be stacked is now limited by the breakdown voltage of the n-well/p-substrate junction.

Since the SOPA is a switching type amplifier, another point that has to be carefully investigated is the presence of transient voltage peaks, which can easily go beyond the nominal supply voltage during the switching of these devices. The implementation of a dedicated bias circuit and techniques to limit the voltage transients will be discussed in Chapter 5.

There are several advantages for using a high voltage output stage comprised of standard CMOS stacked devices instead of customized silicon techniques. They are enumerated in the following list:

- The most decisive argument is the cost. A high voltage implementation in a pure digital CMOS technology results in a compact, low-cost single chip solution. An implementation in a specialized technology on the other hand requires extra process steps and mask sets which increases the cost. In a worst-case scenario, the high voltage technology is not compatible with the CMOS technology so that two separate chips are necessary. A two chip solution increases the system size which results again in extra cost.
- For the design of specialized high voltage devices a thorough knowledge of the different process steps, doping profiles, etc., of the technology is necessary. Technology foundries are not always very keen on giving this kind of information, since they want to maintain their competitive position in the world. By using only standard CMOS devices, no additional information is required from the foundry.
- For a switching power amplifier, the on-resistance of the output stage determines the conduction losses. The lower this resistance, the lower the conduction losses are. The DMOS transistors described in the previous section, make use of a lowly doped region to increase their breakdown voltage. This, however, increases the on-resistance significantly.
- The behavior and parasitics of standard CMOS devices are very well modeled resulting in a good resemblance between simulation and measurements. This is not the case for specialized high voltage devices.

The principle of stacking is traced back to [Pet82] where this technique is used to allow high voltage outputs, in the range of 60 V, to be integrated with low voltage control logic (15 V) in common CMOS processes without special processing steps. Typical applications were then ICs that interface to displays, thermal print heads, relays and incandescent lamps. Recently, the principle of stacking devices has regained interest, because of the low nominal supply voltages originating from the continuous technology scaling. The low supply voltage poses several problems for the direct interface between chips. The required I/O supply voltage scales more slowly due to peripherals, which are build in mature technologies with a higher supply. Therefore, high voltage I/O buffers integrated on-chip become necessary. Examples of high voltage I/O buffers in a standard CMOS technology can be found in [Pel95], [Sin99],

[San99a], [Ann01] and more recently in [Ker05]. Most of these buffers are designed to be able to receive two or three times the nominal supply voltage, but are not able to drive this high voltage.

In this work, the principle of stacking devices will be applied on the SOPA output stage. Figure 4.11 shows a principle schematic of the SOPA amplifier. The PWM output signal of the SOPA is applied to large switches which deliver the current to the load.[1] These switches can either be implemented as n stacked transistors comprised of a modern CMOS technology with a nominal supply voltage of V_{DD}, as single CMOS transistors from a previous generation or as single specialized high voltage devices. The different implementations are schematically shown in Figure 4.11. The high supply voltage is defined as n times V_{DD}, the nominal supply voltage of the modern CMOS technology. The upper switch, which pulls the output to the high supply voltage, is implemented with pMOS devices. The lower switch on the other hand, which pulls the output to the ground, is implemented with nMOS devices. If the transistor or stacked transistors are in the linear region, thus representing a small resistance, the switch is on. If they are in the cut-off region, the switch is off.

By using a switching amplifier, the functionality of the CMOS transistors thus returns to their original digital nature. When the technology is scaled to

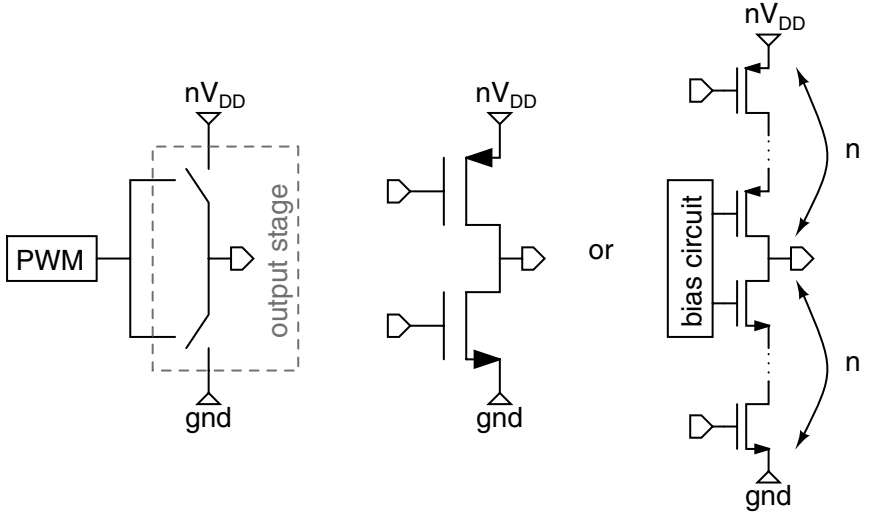


Fig. 4.11. Principle schematic of the SOPA amplifier (left figure) with a high voltage (nV_{DD}) output stage. Implementation of the high voltage output stage with a specialized high voltage technology or a CMOS technology from a previous generation (middle figure). Implementation of the output stage with n stacked standard CMOS transistors with a nominal supply voltage of V_{DD} (right figure)

[1] In a practical SOPA implementation the output stage is included in the loop that generates the PWM signal.

Table 4.3. Technology Parameters

	0.13 µm	0.13 µm thick oxide
V_{DD}	1.2 V	2.5 V
L_{min}	0.13 µm	0.28 µm
t_{ox}	2.3 nm	5.0 nm
C_{ox}	$1.5e^{-2}$ F/m^2	$6.8e^{-3}$ F/m^2
$C_{ox}@L_{min}$	1.9n F/m	1.9n F/m

nanometer dimensions, this kind of switching amplifier architectures becomes even more advantageous compared to classical amplifier implementations. After all, the strong inversion region where the gain of a transistor in saturation is the highest becomes smaller and smaller by scaling the technology [San06]. Therefore, analog design, as we know it, will become more and more difficult in the nanometer era.

In the next section the power dissipation of a high voltage switching output stage comprised of standard stacked CMOS devices will be calculated. The technology used for this calculation is a mainstream 1.2 V 0.13 µm CMOS technology. A comparison is made with an implementation in a 2.5 V 0.13 µm thick oxide CMOS technology. The parameters of these two technologies are shown in Table 4.3. The thick oxide transistor resembles a 0.25 µm technology, two generations behind the 0.13 µm technology. The next section will point out if stacking is beneficial for the output stage concerning the power dissipation. In the remaining of this chapter, the 0.13 µm thick oxide technology will be shortly called the thick oxide technology to avoid confusion with the mainstream 0.13 µm technology.

4.2.2 Power Dissipation

The Power dissipation can be split into two terms: the static power dissipation and the dynamic power dissipation. The static power dissipation covers the losses due to biasing currents, voltage drops over parasitic resistances, etc. The dynamic power dissipation covers the losses due to charging and discharging capacitors.

The power dissipated in the dedicated bias circuit for the stacked transistors is not taken into account for this calculation. No general expression can be given for the power dissipation given in the bias circuit since it is implementation-dependent. However, this does not degrade the results of the following sections. In Chapter 5, where different implementations of the bias

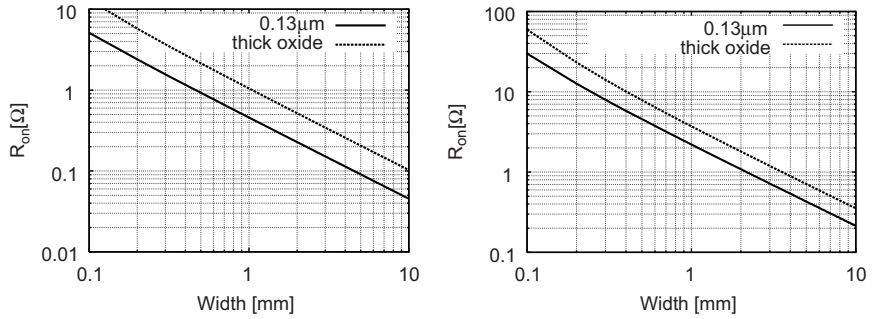
circuit are explained, it will be shown that the power dissipation of the bias circuit can be neglected compared to the power dissipated in the stacked transistors.

Static Power Dissipation

The static power dissipation of a switching output stage is equal to the power dissipated in the on-resistance of the switch. The static power dissipation of a switching amplifier is also called the conduction losses and the expression was given in equation (4.9):

$$P_{cond} = I_{rms}^2 R_{on} \tag{4.11}$$

Following Table 4.1 and Figure 4.2(a), it is known that the on-resistance scales with a factor 2 between a 0.25 µm and a 0.13 µm CMOS technology for minimum length transistors with the same width. Figure 4.12 shows a simulation of the on-resistance for a 0.13 µm and a thick oxide n- and pMOS minimum length transistor in the linear region in function of the width. The factor 2 can be clearly observed. This is a very important result, since it means that two stacked minimum length 0.13 µm transistors in the linear region have the same total on-resistance as one minimum length thick oxide transistor in the linear region with the same width. From Figure 4.10 it is known that the supply voltage of two stacked transistors can be doubled. This means that two stacked 0.13 µm transistors can handle the same supply voltage as one thick oxide transistor. According to equations (4.3), (4.4) and (4.5), the two structures thus have to deliver the same rms current to the load. As a consequence, two stacked minimum length 0.13 µm transistors have equal conductions losses as one minimum length thick oxide transistor with the same width. Or more general, n stacked 0.13 µm minimum length transistors with a width W have equal conduction losses as $n/2$ minimum length stacked thick oxide transistors with the same width W. This statement is schematically represented in Figure 4.13.



(a) nMOS on-resistance (b) pMOS on-resistance

Fig. 4.12. Simulation of the on-resistance for the 0.13 µm and the thick oxide technology in function of the transistors' widths

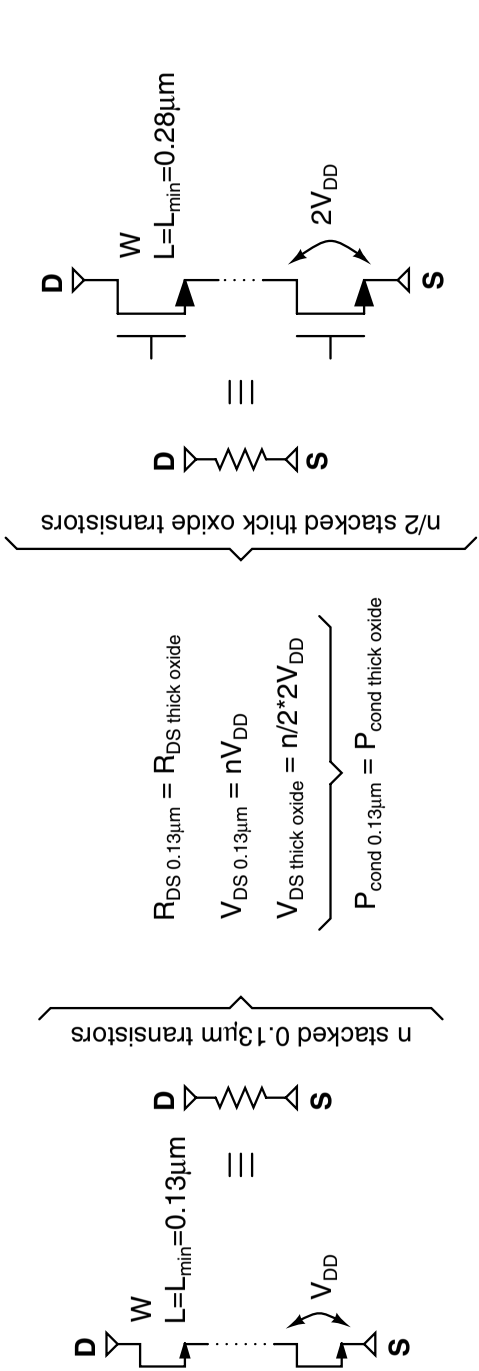
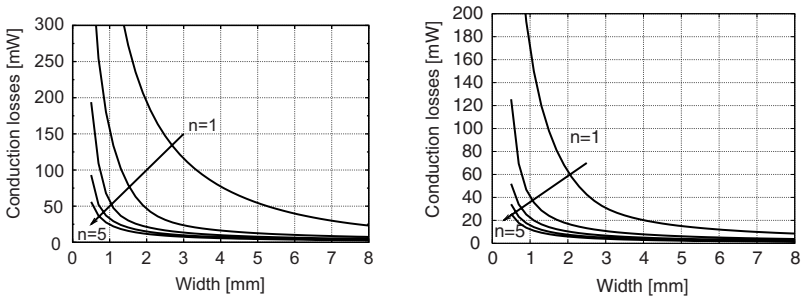


Fig. 4.13. Schematic representation of the fact that n stacked 0.13 µm transistors in the linear region have the same on-resistance and can handle the same supply voltage as $n/2$ stacked thick oxide transistors in the linear region



(a) 0.13 µm (b) thick oxide

Fig. 4.14. Simulation of the conduction losses for the 0.13 µm and the thick oxide technology in function of the transistors' widths

From equation (4.1) and Figure 4.12 it is clear that the on-resistance drops with increasing width. As a consequence, the conduction losses could be made very low just by increasing the transistors' widths. This is also shown in Figure 4.14, where the conduction losses are simulated for $n = 1..5$ stacked nMOS 0.13 µm and thick oxide transistors. One can notice the good resemblance between the curves $n = 2$ and $n = 4$ of the 0.13 µm technology conduction losses and the curves $n = 1$ and $n = 2$ of the thick oxide technology conduction losses respectively. However, increasing the transistors' dimensions for lowering the on-resistance, will increase the dynamic power dissipation as will be seen in the next section.

Figure 4.14 also shows that stacking more devices, thus increasing the supply voltage will lower the conduction losses. This means an improvement in static efficiency as was already demonstrated in Figure 4.5(d).

Dynamic Power Dissipation

The calculation of the dynamic power dissipation of a high voltage output stage comprised of stacked transistors covers the charging and discharging of parasitic capacitors of the transistors and the power dissipated in the tapered buffers driving the output stage. The global expression for the dynamic power dissipation equals: $CV_{DD}V_{swing}f$, with C the capacitor's value, V_{swing} the voltage range over which the capacitor is (dis)charged and f the switching frequency. For this implementation V_{swing} equals V_{DD}. The switching frequency in the SOPA system equals the limit cycle frequency f_{lc}. For the simulation of the switching losses, a limit cycle frequency of 40 MHz has been chosen.

Since this kind of power dissipation is caused by switching transistors, it is also called by the term switching losses. Figure 4.15 shows n stacked nMOS transistors and their parasitic capacitances that are taken into account for the calculation of the switching losses. The expression for the switching losses is split into three terms:

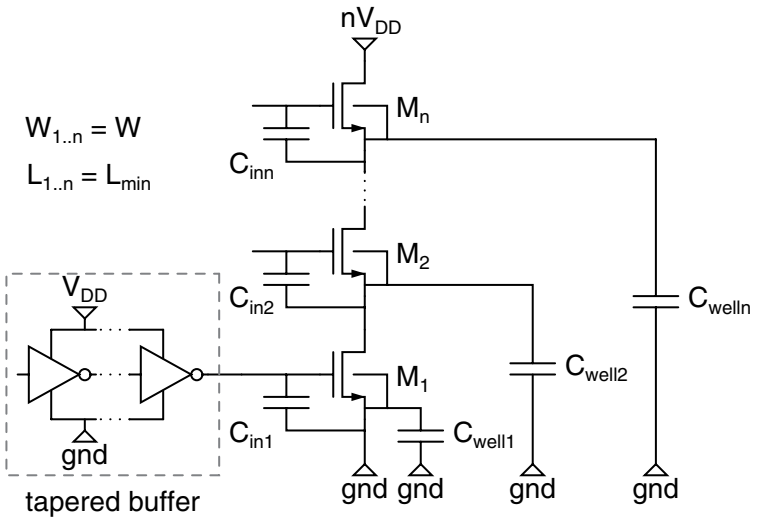


Fig. 4.15. Schematic of n stacked nMOS transistors with the elements that lead to the calculation of the switching losses

1. The first term is the power dissipated in the tapered buffer which drives transistor M_1. For a tapered buffer, optimized for speed, this term equals

$$P_{buffer} = \frac{C_{in_1} V_{DD}^2 f_{lc}}{e-1} \tag{4.12}$$

2. The second term covers the losses due to the charging and discharging of the input capacitors of the stacked transistors. Since the voltage across the terminals of the stacked transistor does not exceed V_{DD} due to the dedicated bias circuit, the maximum power loss by switching the inputs of the stacked transistors equals

$$P_{C_{in}} = V_{DD}^2 f_{lc} \sum_{i=2}^{n} C_{in_i} \tag{4.13}$$

   The power loss by switching transistor M_1 is already taken into account in the expression for the power dissipation in the tapered buffer.
3. The third term covers the losses due to the charging and discharging of the well-capacitors of the stacked transistors. These capacitors originate from the fact that each stacked nMOS transistor has its own separate p-well. This p-well is lying in an n-well, to isolate the device from the substrate. As such, a large junction capacitor is present between the bulk of the transistor and the substrate. This capacitor is called the well-capacitor C_{well}. Without this triple well structure a DC-path would exist from the bulk-source connection of every stacked transistor to the ground resulting

in substrate currents which can lead to latch-up. The power loss due to the charging and discharging of the well-capacitors equals

$$P_{well} = f_{lc} \sum_{i=1}^{n} C_{well_i} \left[(i-1) V_{DD} \right]^2 \tag{4.14}$$

Since the drain-source connections of the stacked transistors can be charged-up to a multiple of V_{DD}, this term will have a large contribution in the total power loss and will eventually be the limiting factor for stacking more transistors in terms of power dissipation. The well-capacitance of a transistor is defined as

$$C_{well} = \alpha c_j W L \tag{4.15}$$

With c_j the junction capacitance between the bulk of the nMOS transistor and the n-well. α is a layout-dependent correction factor such that the value of the well-capacitor can be calculated from the width and the length of a transistor.

The total switching losses thus equals

$$P_{switching} = P_{buffer} + P_{C_{in}} + P_{well} \tag{4.16}$$

For simplicity reasons, the widths and the lengths of the transistors are taken the same. This results in equal input- and well-capacitances for all stacked transistors $C_{in_1} = \ldots = C_{in_n} = C_{in}$ and $C_{well_1} = \ldots = C_{well_n} = C_{well}$.

A comparison of the switching losses between n stacked minimum length 0.13 µm nMOS and $n/2$ stacked minimum length thick oxide nMOS transistors with the same width is made for each term. It is known from Section 4.2.2 that such a configuration has the same total on-resistance and can handle the same supply voltage, resulting in the same conduction losses.

Table 4.3 shows that the total input capacitance of an 0.13 µm and a thick oxide minimum length transistor are equal if they have the same width. If V_{DD} is the nominal supply voltage of the 0.13 µm technology, equation (4.12) becomes

$$P_{buffer\ 0.13\ \mu m} = \frac{C_{in} V_{DD}^2 f_{lc}}{e-1} \tag{4.17}$$

$$P_{buffer\ thick\ oxide} = \frac{4 C_{in} V_{DD}^2 f_{lc}}{e-1} \tag{4.18}$$

The nominal supply voltage of the thick oxide technology is two times larger than V_{DD}. Therefore, the power dissipated in the tapered buffer is lowered with a factor of 4 by scaling the technology from 0.25 µm to 0.13 µm:

$$P_{buffer\ 0.13\ \mu m} = \frac{1}{4} P_{buffer\ thick\ oxide} \tag{4.19}$$

The losses due to charging and discharging of the input capacitances of the stacked transistors can be written as

$$P_{C_{in\ 0.13\ \mu m}} = (n-1)\, C_{in} V_{DD}^2 f_{lc} \tag{4.20}$$

$$P_{C_{in\ thick\ oxide}} = (n/2-1)\, C_{in} 4 V_{DD}^2 f_{lc} \tag{4.21}$$

$$= 2\,(n-2)\, C_{in} V_{DD}^2 f_{lc} \tag{4.22}$$

If $n \geq 3$, then

$$P_{C_{in\ 0.13\ \mu m}} \leq P_{C_{in\ thick\ oxide}} \tag{4.23}$$

One has to bear in mind that n must be an even number if one wants to compare n stacked 0.13 µm transistors with $n/2$ thick oxide transistors. Thus it becomes more advantageous to stack four or more 0.13 µm devices to increase the supply voltage of the output stage in terms of $P_{C_{in}}$ than to stack half as many thick oxide devices for achieving the same supply voltage.

The expression for the losses due to charging and discharging of the well capacitances of the stacked transistors for the two technologies becomes

$$P_{C_{well\ 0.13\ \mu m}} = C_{well} f_{lc} \sum_{i\,=\,1,\ i\ \text{even}}^{n} \left[(i-1)\, V_{DD}\right]^2 \tag{4.24}$$

$$P_{C_{well\ thick\ oxide}} = C_{well} f_{lc} \sum_{i\,=\,1,\ i\ \text{even}}^{n} \left[(i/2-1)\, 2\ V_{DD}\right]^2 \tag{4.25}$$

$$= C_{well} f_{lc} \sum_{i\,=\,1,\ i\ \text{even}}^{n} \left[(i-2)\, V_{DD}\right]^2 \tag{4.26}$$

Under the assumption that the well capacitances of minimum length transistors with the same width are equal for the two technologies and with

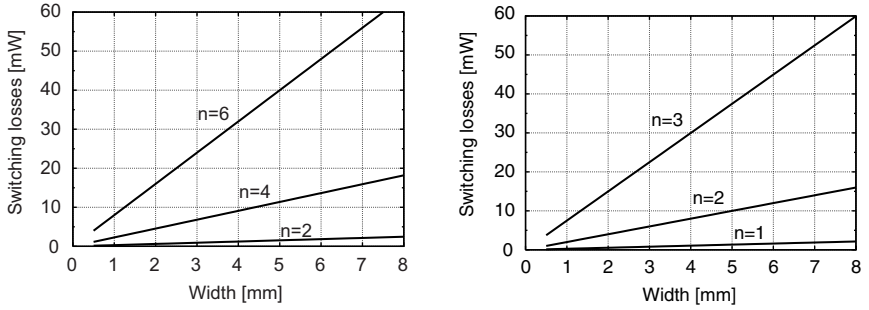
$$\sum_{i\,=\,1,\ i\ \text{even}}^{n} (i-a)^2 = \frac{n\,(n/2+1)\,(n+1)}{3} - 2a\frac{n}{2}\left(\frac{n}{2}+1\right) + a^2\frac{n}{2} \tag{4.27}$$

one can calculate that for every value of n,

$$P_{C_{well\ 0.13\ \mu m}} > P_{C_{well\ thick\ oxide}} \tag{4.28}$$

Or the power loss by charging and discharging the well capacitances will always be larger for n stacked 0.13 µm than for $n/2$ stacked thick oxide transistors.

Figure 4.16 shows the total switching losses in function of the width of the transistors for the 0.13 µm and the thick oxide technology for different numbers of n nMOS stacked transistors. From this figure some conclusions can be drawn. Increasing the width of the transistors results in larger parasitic capacitances according to equations (4.2) and (4.15). Following the equations (4.12), (4.13) and (4.14) this leads to increased switching losses. Secondly,



(a) 0.13 µm (b) thick oxide

Fig. 4.16. Calculation of the switching losses for the 0.13 µm and the thick oxide technology in function of the transistors' widths

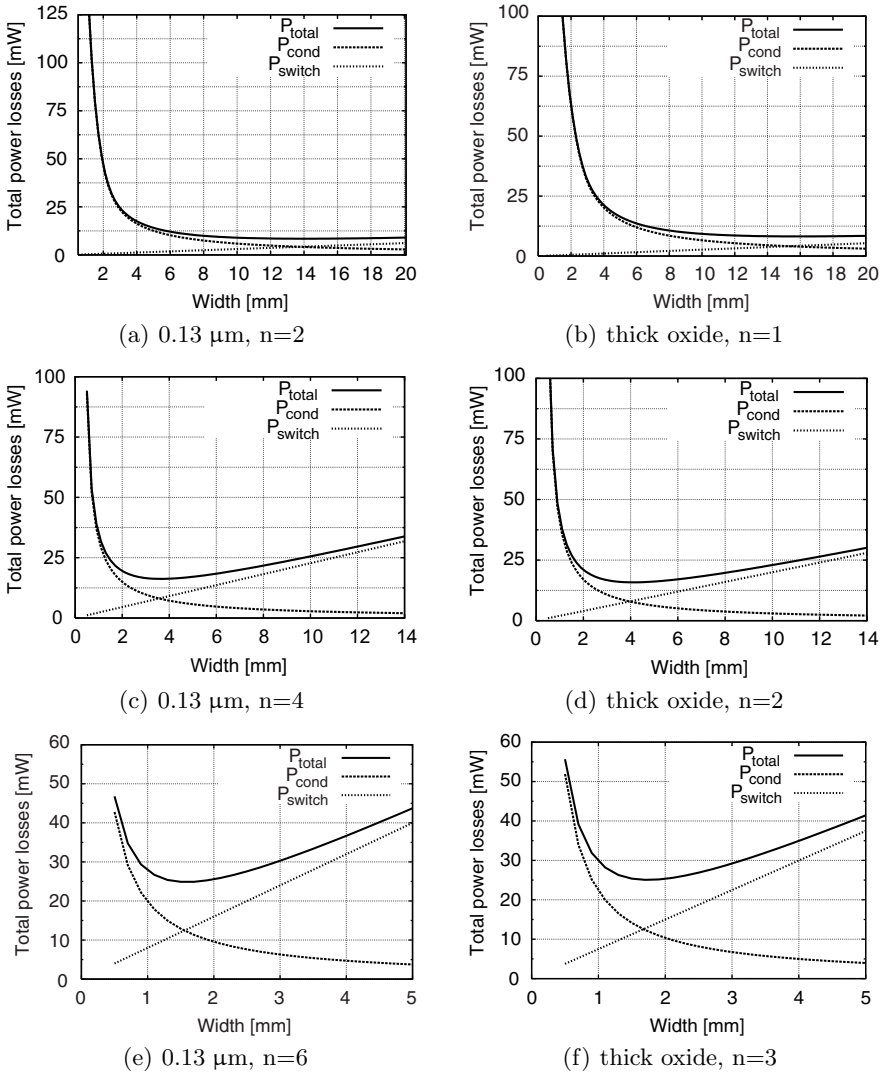
stacking more devices results in more parasitic capacitive elements, leading again to higher switching losses. Moreover, the well-capacitances at the drain-source connections of the stacked transistors will be charged to higher voltages, resulting in a strong rise of the switching losses. These two conclusions are exactly the opposite as those of the static power dissipation. Therefore, an optimum in the total power dissipation can be found as will be seen in the next section.

Figure 4.16 also shows that a configuration of n stacked minimum length nMOS 0.13 µm transistors has comparable switching losses as $n/2$ stacked minimum length nMOS thick oxide transistors. The switching losses are slightly higher for the configuration with 0.13 µm devices. This is due to the large junction capacitance c_j between the bulk of the nMOS devices and the n-well which isolates the nMOS devices from the p-substrate. Therefore, the $P_{C_{well}}$ losses have the largest contribution in the total switching losses and as such they cancel out the results of equations (4.19) and (4.23).

Total Power Dissipation

Figure 4.17 shows the combination of the conduction and the switching losses, leading to the total power losses for different numbers of n stacked nMOS transistors in the 0.13 µm and the thick oxide technology. Careful observation of these figures leads to the following remarks:

- As the conduction losses drop and the switching losses rise with increasing transistor widths, a minimum in the total power losses can be found, which is clearly visible.
- There is a good resemblance between the losses of n stacked 0.13 µm nMOS transistors and $n/2$ stacked thick oxide transistors, as was already mentioned in the previous sections.



(a) 0.13 µm, n=2 (b) thick oxide, n=1

(c) 0.13 µm, n=4 (d) thick oxide, n=2

(e) 0.13 µm, n=6 (f) thick oxide, n=3

Fig. 4.17. Simulation of the total power losses for the 0.13 µm and the thick oxide technology in function of the transistors' widths for different values of n

- The minimum of the total power losses increases for increasing the number of stacked transistors. This is due to the strong increase in switching losses for higher numbers of n in spite of the lower conduction losses.
- The minimum of the total power losses is reached for lower values of the width of the stacked transistors for higher numbers of n. Stacking more transistors results in more parasitic capacitances which leads to a higher and steeper curve of the switching losses. As a consequence the point where

the switching losses becomes higher than the conduction losses is reached for lower transistor widths. On the other hand, this is a good result in terms of area, since it means that the area will not increase exponentially by stacking more transistors.

Until now the power losses were discussed for nMOS stacked transistors. The same results are obtained for pMOS stacked transistors. The output stage of the SOPA amplifier is comprised of nMOS and pMOS stacked transistors to implement the switches, which was shown in Figure 4.11. Figure 4.18 shows the minimum total power losses in function of the number of nMOS and pMOS stacked transistors for an implementation in a 0.13 µm technology. In fact, the figure shows the total power loss of the SOPA output stage, without inclusion of the dedicated gate-bias circuit of the stacked transistors. To make a comparison with an implementation in the thick oxide technology, the total power losses of the output stage comprised of $n/2$ stacked thick oxide transistors is plotted (squares) on the n scale instead of $n/2$ in the same figure. For example: an implementation of eight stacked 0.13 µm devices has a total power loss of 60 mW, whereas an implementation of four stacked thick oxide devices has a total power loss of 61 mW.

Figure 4.18 shows that an implementation of the output stage with n stacked 0.13 µm devices is slightly more efficient than an implementation with $n/2$ stacked thick oxide transistors. The real advantage lies in the fact that the low voltage issues due to scaling the technology to ultradeep-submicron or nanometer technologies can efficiently be circumvented by stacking devices. It is thus possible to design a high voltage output stage in a low volt-

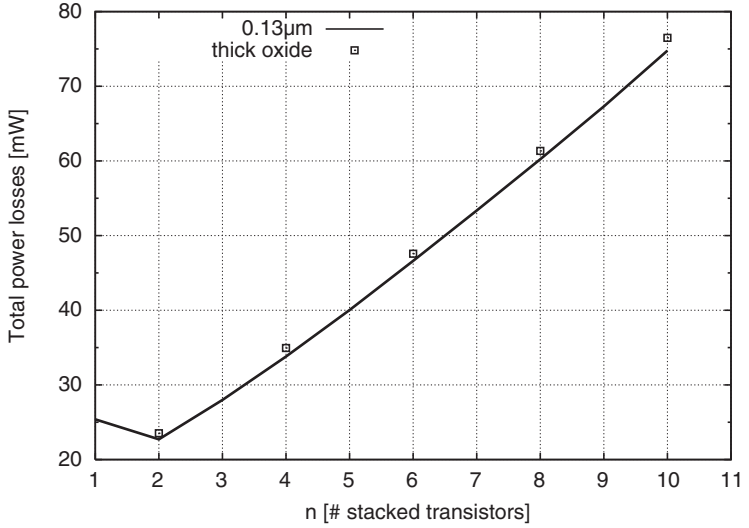


Fig. 4.18. Minimum total power losses of the SOPA output stage in function of the number of stacked transistors

age technology, resulting in a compact low-cost single chip solution, without degradation compared to an implementation in a technology from a previous generation which has a higher nominal supply voltage.

A final remark that can be made with this figure, which was already clear from Figure 4.17, is that the minimum total power loss increases when more transistors are stacked. One can conclude that using only two stacked 0.13 μm devices for this structure has the lowest power losses. However, one must bear in mind that only two stacked devices results in a rather low supply voltage. As a consequence, previously discussed problems like large transformer ratios, high distortion, high rms currents, reliability, etc. will arise. For the design of the SOPA line driver one must thus carefully choose the number of stacked transistors to alleviate these problems while not over-designing the output stage.

4.3 Conclusions

Under the impulse of the low power requirements of digital circuits, the end of CMOS scaling is not yet in sight. Therefore, the influence of scaling the devices to nanometer dimensions on the SOPA design was investigated in this chapter. First, an overview of the different scaling laws and their applicability on the current CMOS scaling trend was given. The influence of this scaling on switching type amplifiers in general and the SOPA amplifier in particular was discussed. It is shown that the efficiency and reliability of the line driver will seriously degrade due to the low supply voltages coming from nanometer technologies. A high voltage output stage thus becomes mandatory for the SOPA. Several customized CMOS based high voltage technologies were described for increasing the output stage supply voltage.

An alternative solution, however, is proposed in this chapter. By stacking standard CMOS devices, a fully integrated AFE with a high voltage line driver becomes reality, resulting in a compact and low-cost single chip solution. Through the calculation of the total power dissipation of the high voltage output stage, a comparison is made between an implementation in a standard low voltage technology and a technology from a previous generation with a higher nominal supply voltage. It is proved that a high voltage output stage design in a low voltage CMOS technology is feasible, without any performance degradation.

5

High Voltage Implementations in Standard CMOS

THE stacking of devices is a very promising technique for designing high voltage circuits in a low voltage standard CMOS technology. However, to prove its credibility, the technique needs to be verified by practical implementations. For this, two test chips were designed in respectively a 0.25 μm and 130 nm mainstream CMOS technology.

The first test chip is a 7.5 V output driver in a 2.5 V 0.25 µm CMOS technology, which proved the feasibility of high voltage design, with the stacked devices principle, in standard CMOS. It is the first output driver able to operate at three times the nominal supply voltage with only three stacked mainstream transistors.

With the second test chip, the boundaries of the stacking principle are even further explored. With five stacked transistors, a supply voltage of 5.5 V is reached in a 1.2 V 130 nm standard CMOS technology. Moreover, this high voltage driver is used as the output stage in the SOPA architecture, leading to a highly efficient aDSL2+ CO line driver. The design, layout and measurements of this line driver are discussed in Chapter 6.

For every chip, the implementation of all building blocks will be thoroughly discussed. Since higher voltages than the nominal supply voltage of the technology are applied to the chips, special attention is also given to the layout in order to preserve reliable operation.

The presented prototypes will validate the principle of stacking transistors. Therefore, a low-cost solution is provided to circumvent the low voltage issues of recent nanometer CMOS technologies.

5.1 A 7.5 V Output Driver in a 2.5 V 0.25 µm CMOS Technology

5.1.1 Introduction

The goal of this first test chip was to prove the concept of a high voltage switching type output driver in a low voltage standard CMOS technology by

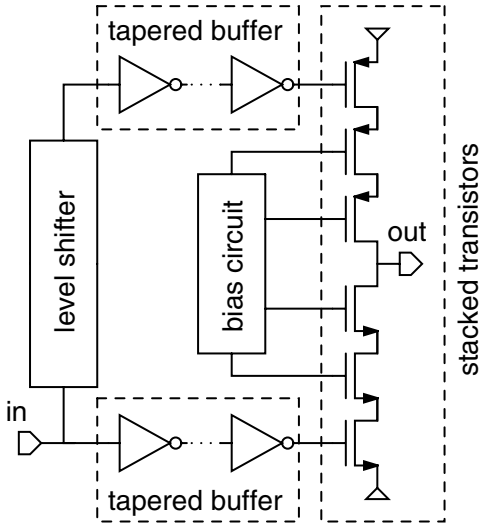


Fig. 5.1. Block schematic of the first test chip

using the stacked devices principle. Therefore, it was not the intention from the start on to design a high voltage output stage to be used for the SOPA line driver, fully compatible with the aDSL specifications. The prototype was implemented in a 0.25 μm 1P5M twin well CMOS technology with a nominal supply voltage of 2.5 V.

The block schematic of the realized high voltage driver is given in Figure 5.1. The driver consists of four building blocks: the stacked transistors, the bias circuit, the tapered buffers and a level-shifter. The output of the driver is controlled by the outer stacked transistors, which are driven by the tapered buffers. The gates of the other stacked transistors are controlled by a dedicated bias circuit to keep the voltage across their terminals within the technology limits. The level-shifter provides the correct offset voltage for the tapered buffer driving the upper pMOS stacked transistor.

Every block is integrated on the same die and is comprised of standard CMOS devices. In the next section, the design of each building block is explained.

5.1.2 Building Block Design

The Stacked Transistors

The stacked transistors form the switches which charge or discharge the load. When the transistors are in the linear region, the switch is on and is characterized by its switch-resistance, which equals the total on-resistance of the stacked transistors in the linear region. When the transistors are in the cut-off

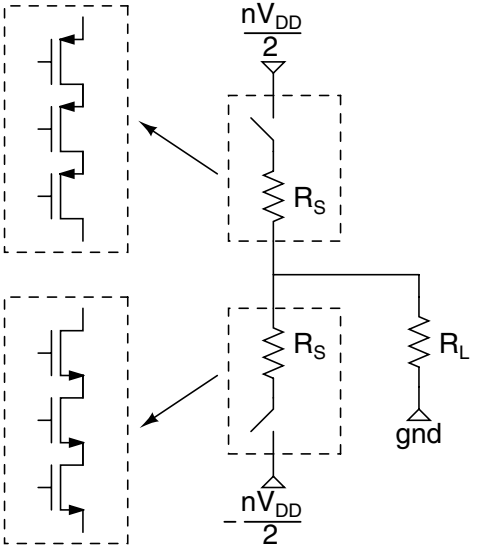


Fig. 5.2. Schematic representation of the stacked transistors as a switch

region, the switch is off and is characterized by an infinitely large resistance. There are three stacked transistors used for each switch. This means that the voltage multiplication factor n can raise up to three and that the maximum supply voltage thus equals 7.5 V. Figure 5.2 shows a schematic representation of the stacked transistors as a switch with a switch-resistance R_S. The load is represented by a resistor R_L. The upper switch, responsible for charging the load, is comprised of pMOS stacked transistors. The lower switch on the other hand, responsible for discharging the load, is comprised of nMOS stacked devices.

As discussed in Section 4.2.2, the static efficiency depends on the total on-resistance of the stacked transistors. The lower the on-resistance, the larger the static efficiency, but also the lower the dynamic efficiency. However, since there is no benchmarking yet for estimating the transistor's well-capacitances,[1] a first design choice is made to design for a static efficiency of 90%. For the next high voltage output drivers the well-capacitances can be estimated from the layout of this first test chip. The static efficiency was defined in equation (4.10):

$$\eta_{stat} = \frac{R_L}{R_L + R_S} = 90\% \tag{5.1}$$

[1] The well-capacitance is calculated from the width and the length of the transistors multiplied by a layout dependent factor α. Since this is a first test chip, α can only be calculated after layout.

The second design choice, is the total output power that the high voltage driver has to deliver. Since the SOPA is a power amplifier, its output stage has to be able to deliver a considerable amount of power. For this an output power of 200 mW is chosen which corresponds to the necessary output power of a basic aDSL system (100 mW) with a passive resistive termination. To provide a certain margin an extra 10% of power is taken as the start point for the calculations. The total power delivered to the load R_L by a switching amplifier with a supply voltage of nV_{DD} equals

$$P_{out} = \frac{\left(\frac{R_L}{R_L+R_S}\frac{nV_{DD}}{2}\right)^2}{R_L} = 220mW \tag{5.2}$$

Equations (5.1) and (5.2) lead to: $R_L = 52\ \Omega$ and $R_S = 5.8\ \Omega$. Since each switch is implemented by three stacked transistors the switch-resistance has to be divided by three to obtain the on-resistance of the transistors. This results in an on-resistance of 1.9 Ω. By rearranging equation (4.1) the W/L value can be calculated:

$$\frac{W}{L} = \frac{1}{\mu C_{ox} R_{on} \left(V_{GS} - V_T - V_{DS}\right)} \tag{5.3}$$

With the technology parameters of an UMC 0.25 µm technology, this leads to a W/L ratio of 7,824 for the pMOS and a W/L ratio of 1908 for the nMOS transistor. These values are rounded to 8,000 and 2,000 respectively.

According to Section 4.1.5 the effect of hot carriers is lowered by reducing the electric field across the channel of the transistor. This can be done by increasing the channel length. Therefore, the length of the stacked transistors is arbitrarily chosen at 0.8 µm. However, one has to bear in mind that this is merely an extra precaution step. After all, the voltage across the terminals of the active elements is limited to one V_{DD}, so minimum length devices are also possible. The resulting W and L values of the stacked transistors are given in Table 5.1 together with their input capacitance.

Now the values of the input capacitances of the stacked transistors are known, the power losses in these capacitances and the tapered buffers can be calculated. The switching frequency, that is aimed for in this design, is set at 10 MHz. It is important to calculate the dynamic losses in order check if the design choice for a static efficiency of 90% was not too optimistic, resulting in a large dynamic power dissipation. As already mentioned the power losses due

Table 5.1. Stacked transistor sizing

	pMOS	nMOS
W	6.400 mm	1.600 mm
L	0.80 µm	0.80 µm
C_{in}	34.8 pF	9.1 pF

to the well-capacitances can not be taken into account in this stadium of the design. If the dynamic losses turn out to be higher than the static losses, the design choice for the static efficiency has to be re-evaluated. In a worst-case scenario this iteration process has to be redone for this first test chip after layout when the value of the well-capacitances is known.

The Tapered Buffer

The W/L ratio of the pMOS over the nMOS transistor for a unit inverter was set to 4.2, leading to the following dimensions of $W = 2.00\ \mu m$, $L = 0.24\ \mu m$ for the pMOS transistor and $W = 0.48\ \mu m$, $L = 0.24\ \mu m$ for the nMOS transistor. The input capacitance of a unit inverter for these values equals $C_{io} = 5.23\ fF$, which leads to an intrinsic delay t_{d0} of about 50 ps. The optimal tapered buffer would thus respectively have the following number of stages for the pMOS and nMOS input capacitance:

$$N_{opt,p} = \left\lceil \ln\left(\frac{C_{L,p}}{C_{io}}\right) - 1 \right\rceil = 8 \tag{5.4}$$

$$N_{opt,n} = \left\lceil \ln\left(\frac{C_{L,n}}{C_{io}}\right) - 1 \right\rceil = 7 \tag{5.5}$$

This leads to the scaling factors $x_p = 2.66$ and $x_n = 2.45$, resulting in an optimized delay of 0.7 ns for the tapered buffer driving the nMOS gate and 1.0 ns for the tapered buffer driving the pMOS gate. Since this delay is more than low enough for a 10 MHz switching frequency, larger scaling factors are chosen to reduce the number of inverter stages, in order to save area, and to lower the short circuit power dissipation as described in [Vee84].

The last stages of the inverter chain become quite large, resulting in large current spikes during switching. Therefore, the gate lengths of the transistors in the tapered buffers are arbitrarily set at 0.4 μm to reduce the effects of hot carrier degradation. The sizing of a basic inverter becomes now $W = 3.36\ \mu m$, $L = 0.4\ \mu m$ for the pMOS transistor and $W = 0.80\ \mu m$, $L = 0.4\ \mu m$ for the nMOS transistor. This results in an input capacitance C_{i0} of 12.6 fF.

For the tapered buffer driving the nMOS transistor a scaling factor of 4 is chosen. A scaling factor of 5 is taken for the tapered buffer driving the pMOS transistor. Both buffers are then comprised of 5 inverter stages. The resulting dimensions are shown in Tables 5.2 and 5.3. The delays for the tapered buffers driving the nMOS and the pMOS gate are now 0.95 ns and 1.2 ns respectively, which is only a minor rise compared to the delay by using the optimum scaling factors for speed.

The total power consumption of the inverter chain is proportional with the total capacitance in the chain:

$$P = V_{DD}^2 f \sum_{i=1}^{N} x^i C_{i0} \tag{5.6}$$

Table 5.2. Transistor dimensions of the inverter chain driving the nMOS gate

		inv 1	inv 2	inv 3	inv 4	inv 5
pMOS	W	3.36 µm	13.44 µm	53.76 µm	215.04 µm	860.16 µm
	L	0.40 µm	0.40 µm	0.40 µm	0.40 µm	0.40 µm
nMOS	W	0.80 µm	3.20 µm	12.80 µm	51.20 µm	204.80 µm
	L	0.40 µm	0.40 µm	0.40 µm	0.40 µm	0.40 µm

Table 5.3. Transistor dimensions of the inverter chain driving the pMOS gate

		inv 1	inv 2	inv 3	inv 4	inv 5
pMOS	W	3.36 µm	16.80 µm	84.00 µm	420.00 µm	2100.00 µm
	L	0.40 µm	0.40 µm	0.40 µm	0.40 µm	0.40 µm
nMOS	W	0.80 µm	4.00 µm	20.00 µm	100.00 µm	500.00 µm
	L	0.40 µm	0.40 µm	0.40 µm	0.40 µm	0.40 µm

With x the scaling factor and N the number of inverter stages. For a supply voltage of 2.5 V and a switching frequency of 10 MHz this leads to a total power dissipation of about 4.2 mW for the two inverter chains. Together with the power losses, due to the switching of the gate capacitances of the stacked transistors, the total switching losses (without inclusion of the well-capacitances) equals 9.7 mW, which is less than 5% of the total output power. Therefore, the design choice of a static efficiency of 90% still holds. So there is no iteration step necessary in this stadium of the design.

The Bias Circuit: Analytical Description

The bias circuit sets the correct bias voltages for the stacked transistors such that their gate-source, gate-drain and drain-source voltages are within the technology limits during operation. Figure 5.3 shows the node voltages of the switch implemented by three nMOS stacked transistors. Two regions of operation have to be considered: steady state (high and low) and transient operation (high-to-low and low-to-high). For each mode the bias voltages have to follow the voltages on the internal nodes in order to preserve reliable operation. Figures 5.3(a) and 5.3(b) show the voltages for the steady state region. Figure 5.3(c) shows an approximation of the node voltages for the onset of a transient high-to-low transition of the output.

Figure 5.4 depicts an implementation of the bias circuit for the three nMOS stacked transistors. In the next two paragraphs the operation of this circuit is analyzed for the two operation regimes, steady state and transient operation. The implementation and analysis of the bias circuit for the pMOS stacked transistors is the same, since the nMOS switch and the pMOS switch are each

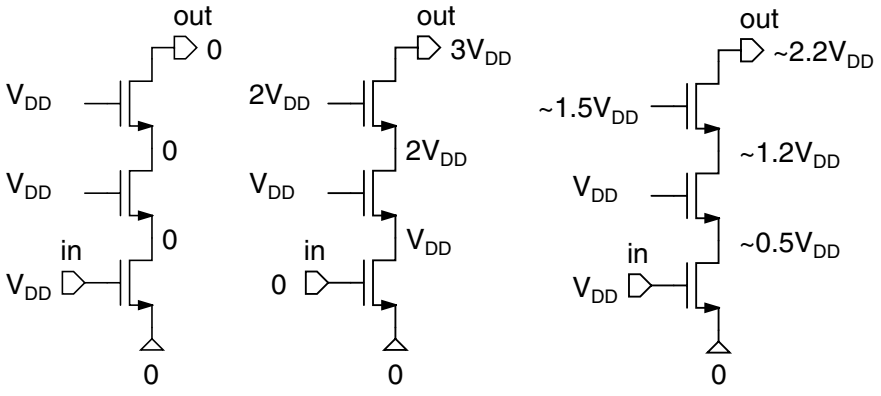


Fig. 5.3. Node voltages of a high voltage nMOS switch with three stacked transistors in three different modes

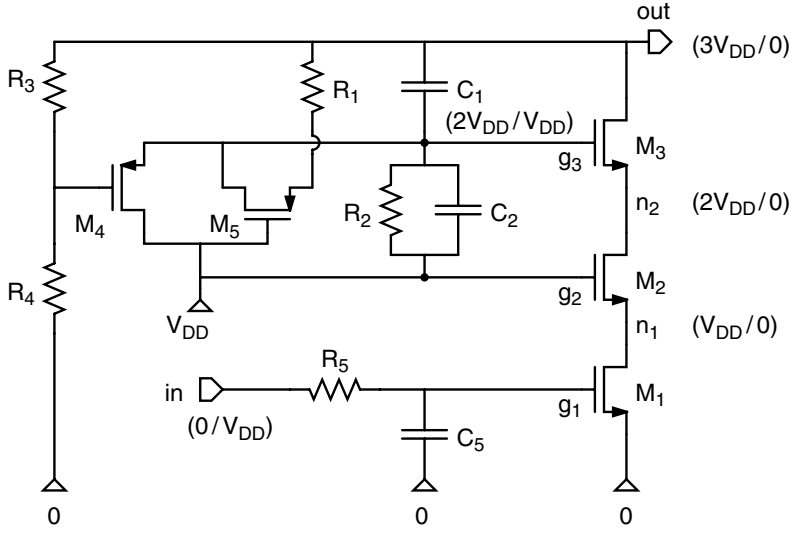


Fig. 5.4. Circuit schematic of the bias circuit for the nMOS stacked transistors

others complement. All voltages on the internal nodes of the bias circuit and stacked transistors are written in function of multiples of V_{DD} from 0 to $3V_{DD}$. For reasons of simplicity, the resistive division between the on-resistance of the stacked transistors and the output resistance is not taken into account for the analytical description of the steady state operation.

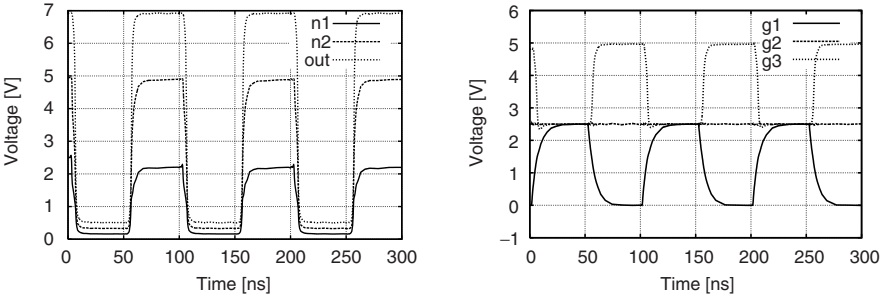
Steady State Operation

First consider the case in which the output voltage switches from low (0) to high (3 V_{DD}). In the previous state, when the output was low, the transistors M_1, M_2 and M_3 were in the linear region and the internal nodes n_1 and n_2 were discharged. The signal arriving from the tapered buffer switches M_1 off. As a consequence, node n_1 is charged to $V_{g_2} - V_{Tn}$ and then slowly rises to V_{g_2} due to the subthreshold current. To prevent breakdown mechanisms in M_1, V_{g_2} is set at a fixed voltage of V_{DD}. Transistor M_2 is now in the cut-off region. Consequently, node n_2 is charged to $V_{g_3} - V_{Tn}$. Again, the subthreshold current results in a further charging of this node up to V_{g_3}. To prevent breakdown mechanisms, now in M_2, the maximum voltage on g_3 is 2 V_{DD}. Transistor M_3 is now in the cut-off region. Since M_1 and M_2 both have a voltage drop of V_{DD} from drain to source, the theoretical maximum output voltage will thus be 3 V_{DD} as mentioned before. However, during operation the drain-source voltage of M_3 will be lower than V_{DD} in the high-output state. Since in this state the output voltage level is defined by a resistive division between the on-resistance of the pMOS stacked transistors, which are in the linear region, and the load resistance R_L. As discussed in the previous sections, it is this resistive division that determines the static efficiency of the high voltage output driver. This voltage headroom will become useful to set off transient voltage peaks as will be seen in the next section.

The bias voltage of transistor M_3 is, in this case, set by a resistive division between the output at 3 V_{DD} and the fixed bias voltage of transistor M_2 at V_{DD}. This resistive division, comprised of the resistors R_1 and R_2, is triggered on by M_5, which is in the linear region. The resistive division comprised of the resistors R_3 and R_4 between the output and the ground sets transistor M_4 in the cut-off region such that there is no low-ohmic path between the nodes g_2 and g_3.

Secondly, consider the case in which the output switches from high (3 V_{DD}) to low (0). In the previous state, M_1, M_2 and M_3 were in the cut-off region and the output was high. First, transistor M_1 is set in the triode region. As a consequence, node n_1 is discharged. Since the bias voltage of transistor M_2 was set at a fixed value of V_{DD}, M_2 enters the linear region. Node n_2 is now discharged through M_1 and M_2. When the gate-source voltage of transistor M_3 is larger than its V_{Tn} the output is discharged. To reduce the oxide stress in M_3 its bias voltage has to be lowered from 2 V_{DD} to V_{DD}. The bias voltage of M_3 is now directly given by the fixed bias voltage of M_2, which passes through M_4. Transistor M_5 is now in the cut-off region and consequently breaks the resistive division comprised of R_1 and R_2.

Figure 5.5 shows a transient simulation of the voltages on the terminals of the stacked transistors. A square wave with a frequency of 10 MHz defined between 0 and V_{DD} is applied to the high voltage driver. The load is 52 Ω. It is clear that for the steady state case the bias circuit provides the correct gate voltage for the stacked transistors.



(a) Drain voltages of M_1, M_2 and M_3 (b) Gate voltages of M_1, M_2 and M_3

Fig. 5.5. Transient simulation of the voltages on the terminals of the stacked transistors

Transient Operation

This section describes the problems and solutions during transient switching of the high voltage output driver. The most critical transition for a nMOS switch implementation, with respect to reliability, is the high-to-low transition of the output. A transition from 0 to V_{DD} of node g_1, switches M_1 from cut-off to the linear region. The faster the transition of g_1 occurs, the faster M_1 enters the linear region and the faster node n_1 is discharged. Since the gate voltage of M_2 is set at a fixed value of V_{DD}, its gate-source and, as a consequence, its state of operation is completely determined by the voltage on node n_1. To avoid hot carrier degradation and breakdown mechanisms to occur in M_2, resulting from a too large drain-source voltage, node n_2 must be discharged with the same speed as node n_1. This is possible for a relatively slow transition of n_1. But, for a fast transition, the delay of transistor M_2 for entering from cut-off to the linear region results in an overshoot on its drain-source voltage. Therefore, a low-pass filter comprised of R_5 and C_5 is added to soften the transitions at node g_1.

The same problem also occurs with transistor M_3. The transient voltage peaks on the terminals of M_3 are prevented in two ways. First, the voltage headroom, originating from the resistive division of the on-resistance of the stacked transistors with the output load, covers partially the delay of M_3 for the transition from the cut-off region into the linear region. Second, an extra capacitor C_1 is added on top of the already quite large gate-drain capacitance of M_3. During a high-to-low transition of the output, the voltage on node g_3 switches from 2 V_{DD} down to V_{DD}. Therefore, the switching of node g_3 helps to discharge the output node due to the strong capacitive coupling. However, during a low-to-high transition of the output, the increased gate-drain capacitance of M_3 acts together with the resistors R_1 and R_2 as a high-pass filter. This results in an overshoot on the steady-state voltage of node g_3. Therefore, capacitance C_2 is added, which acts as a low pass filter

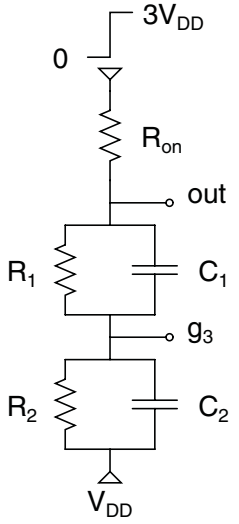


Fig. 5.6. Model of the bias circuit of transistor M_3 for the low-to-high transition

for the transient voltage overshoot on g_3. The necessary capacitance value of C_2 can be calculated in two ways: the time-domain approach and frequency domain approach.

Time Domain For the time-domain approach consider Figure 5.6, which shows a model of the bias circuit of transistor M_3 for the low-to-high transition of the output. The assumption is made that the pMOS stacked transistors are already in the linear region and, as a consequence, they can be represented by their accumulative on-resistance. The same assumption is made for the nMOS stacked output transistors which are in the cut-off region. $V_{C_1}(t)$ is the voltage across C_1 and $V_{C_2}(t)$ is the voltage across C_2. These two voltages define the gate voltage of M_3 (node g_3). For reasons of simplicity, the non-linear gate-capacitors of the transistors M_2 and M_3 on the nodes g_2 and g_3 are incorporated in the values of C_1 and C_2. The electrical network can then be described by the following system of differential equations:

$$V'_{C_1}(t) = -\frac{G_{on}+G_1}{C_1}V_{C_1}(t) - \frac{G_{on}}{C_1}V_{C_2}(t) + 2V_{DD}\frac{G_{on}}{C_1}\ \delta(t) \qquad (5.7)$$

$$V'_{C_2}(t) = -\frac{G_{on}}{C_2}V_{C_1}(t) - \frac{G_{on}+G_2}{C_2}V_{C_2}(t) + 2V_{DD}\frac{G_{on}}{C_2}\ \delta(t) \qquad (5.8)$$

With $G_{on} = R_{on}^{-1}$, $G_1 = R_1^{-1}$ and $G_2 = R_2^{-1}$ and with the following starting conditions: $V_{C_1}(0) = V_{C_2}(0) = V_{DD}$. In matrix form

$$\begin{bmatrix} V'_{C_1}(t) \\ V'_{C_2}(t) \end{bmatrix} = \begin{bmatrix} -\frac{G_{on}+G_1}{C_1} & -\frac{G_{on}}{C_1} \\ -\frac{G_{on}}{C_2} & -\frac{G_{on}+G_2}{C_2} \end{bmatrix} \begin{bmatrix} V_{C_1}(t) \\ V_{C_2}(t) \end{bmatrix} + \begin{bmatrix} 2\,V_{DD}\,\frac{G_{on}}{C_1} \\ 2\,V_{DD}\,\frac{G_{on}}{C_2} \end{bmatrix} \qquad (5.9)$$

Or

$$\mathbf{V}'(t) = \mathbf{A}\mathbf{V}(t) + \mathbf{B} \tag{5.10}$$

The steady-state solution of this system of differential equations is the solution of (5.11).

$$\mathbf{A}\mathbf{V}(t) = -\mathbf{B} \tag{5.11}$$

Therefore the steady-state solution is

$$\begin{bmatrix} V_{C_1,\ Steady-state} \\ V_{C_2,\ Steady-state} \end{bmatrix} = \begin{bmatrix} -2\,V_{DD}\frac{G_2}{G_1+G_2} \\ -2\,V_{DD}\frac{G_1}{G_1+G_2} \end{bmatrix} \tag{5.12}$$

Assume that λ_1 and λ_2 are the eigenvalues of matrix $\mathbf{A}$ with eigenvectors $\mathbf{E}_1$ and $\mathbf{E}_2$. The global solution of (5.10) can then be described by the following equation:

$$\mathbf{V}(t) = \mathbf{V}_{Steady-state} + \alpha_1 \exp^{(\lambda_1 t)} \mathbf{E}_1 + \alpha_2 \exp^{(\lambda_2 t)} \mathbf{E}_2 \tag{5.13}$$

With, after some simplification, ($G_{on} \gg G_1, G_2$):

$$\lambda_1 = -\frac{G_1C_2 + G_2C_1}{2C_1C_2} \tag{5.14}$$

$$\lambda_2 = -\frac{G_{on}C_2 + G_{on}C_1}{C_1C_2} \tag{5.15}$$

and

$$\mathbf{E}_1 = \begin{bmatrix} 1 \\ -1 \end{bmatrix} \tag{5.16}$$

$$\mathbf{E}_2 = \begin{bmatrix} 1 \\ C_1/C_2 \end{bmatrix} \tag{5.17}$$

From (5.12), (5.13), (5.16) and the initial conditions the constants α_1 and α_2 can be found:

$$\begin{bmatrix} \alpha_1 \\ \alpha_2 \end{bmatrix} = \begin{bmatrix} V_{DD}\frac{C_2G_1 - C_1G_2}{(C_1+C_2)(G_1+G_2)} \\ -2\ V_{DD}\frac{C_2}{C_1+C_2} \end{bmatrix} \tag{5.18}$$

The voltage on node g_3 corresponds with $V_{C_2}(t)$ in this model. For a positive step function, the exponential terms in the solution of (5.13) can lead to an overshoot if the signs of the products $\alpha_1\mathbf{E}_{12}$ and $\alpha_2\mathbf{E}_{22}$ are positive. One can see that the exponential term corresponding with λ_2 always has a negative sign. This means that the contribution of this term in the solution of $V_2(t)$ in (5.13) never leads to an overshoot on the steady-state solution. The exponential term of $V_2(t)$ corresponding with λ_1 has a negative sign if the following condition for α_1 holds:

$$V_{DD}\frac{C_2G_1 - C_1G_2}{(C_1 + C_2)\,(G_1 + G_2)} \geq 0 \tag{5.19}$$

Which results in

$$C_2 G_1 \geq C_1 G_2 \tag{5.20}$$

One can see from equation (5.18) that the exponential term of $V_{C_2}(t)$ corresponding with λ_1 can even be completely cancelled out if $C_2 G_1 = C_1 G_2$ is chosen.

Frequency Domain For the frequency domain approach consider the transfer function from *out* to g_3 in Figure 5.6:

$$\mathrm{TF} = \frac{R_2 \left(1 + sR_1 C_1\right)}{R_1 + R_2 + s\left(R_1 R_2 C_1 + R_1 R_2 C_2\right)} \tag{5.21}$$

For DC-operation this becomes

$$\mathrm{TF} = \frac{R_2}{R_1 + R_2} \tag{5.22}$$

Therefore, $V_{g_3} = \mathrm{TF} \cdot V_{out}$ gives the same result as the steady-state solution obtained from the time domain approach. For the frequency behavior one must consider the following pole and zero:

$$f_z = \frac{1}{2\pi R_1 C_1} \tag{5.23}$$

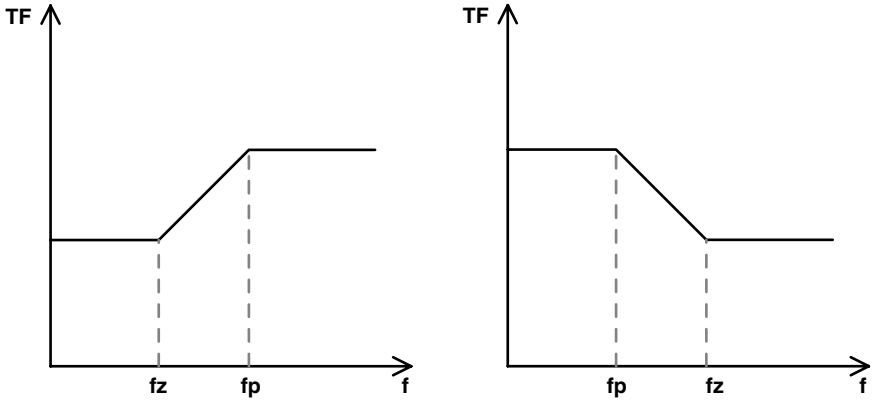
$$f_p = \frac{R_1 + R_2}{2\pi\left(R_1 R_2 C_1 + R_1 R_2 C_2\right)} \tag{5.24}$$

A small C_2 results in $f_p > f_z$ which leads to the bode plot of Figure 5.7(a). In this graph one can see that the gain for high frequencies is larger than the DC-gain which can lead to voltage overshoots during transients. On the other hand if C_2 is large enough the situation as shown in Figure 5.7(b) is applicable. The high frequency gain is now lower than the DC-gain which results in a suppression of high frequency transients. The requirement for a stable voltage on g_3 can be rewritten as: $f_p \leq f_z$. After some calculation this results in

$$R_2 C_2 \geq R_1 C_1 \tag{5.25}$$

Which is the same condition as the one obtained from the time domain approach in equation (5.20).

Figure 5.8 demonstrates the importance of the analysis results of the equations (5.20) and (5.25). It shows a transient simulation of the gate voltage of transistor M_3 for three different cases: $R_1 C_1 << R_2 C_2$, $R_1 C_1 = R_2 C_2$ and $R_1 C_1 >> R_2 C_2$. One can see that the cases $R_1 C_1 << R_2 C_2$ and $R_1 C_1 >> R_2 C_2$ results in a wrong operation point voltage, which stresses transistor M_3 and finally will result in a breakdown of its gate oxide. Therefore, the case $R_1 C_1 = R_2 C_2$ is chosen.



(a) $f_p > f_z$ (b) $f_p < f_z$

Fig. 5.7. Bode plot of the transfer function from *out* to g_3

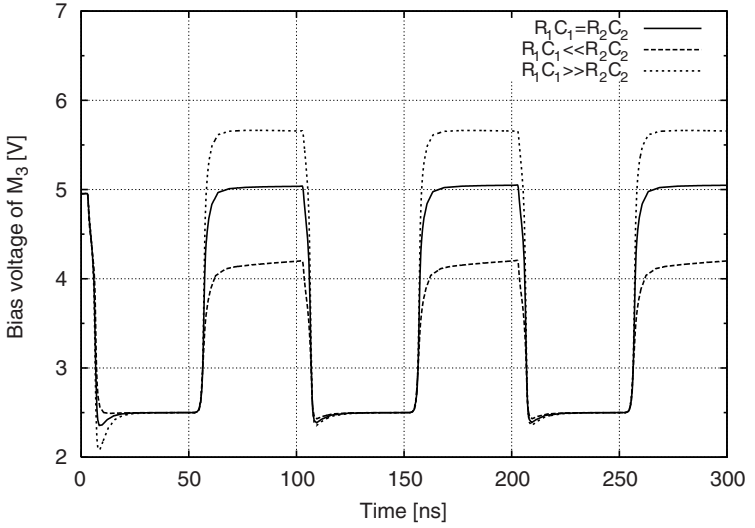
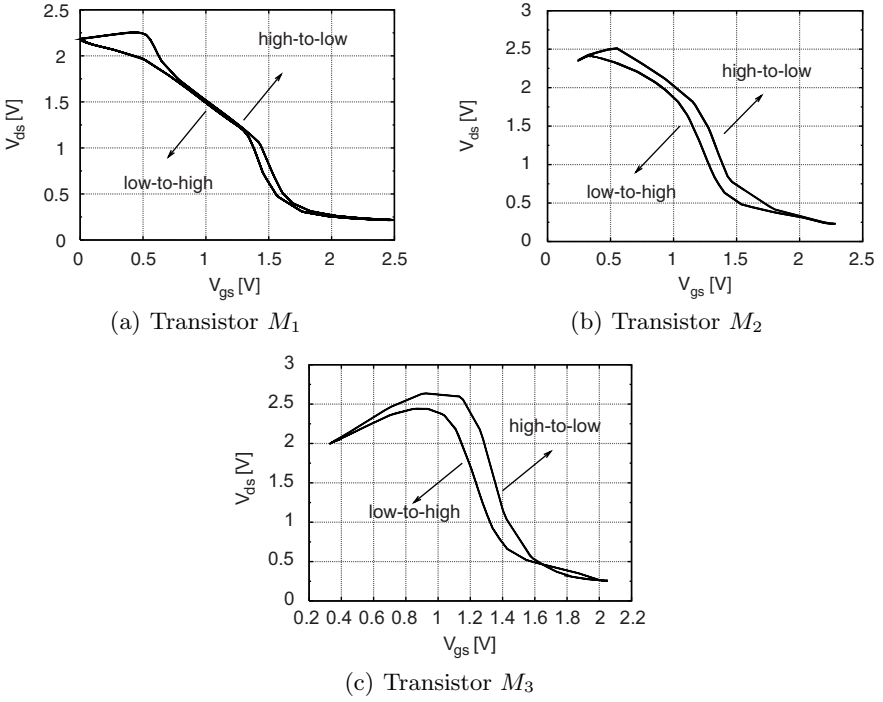


Fig. 5.8. Transient simulation of the gate voltage of transistor M_3 for the cases: $R_1C_1 = R_2C_2$, $R_1C_1 << R_2C_2$ and $R_1C_1 >> R_2C_2$

Figure 5.9 shows a transient simulation of the drain-source to gate-source voltage transfer characteristic of the transistors M_1, M_2 and M_3 as they were defined in Figure 5.4. Since the nominal supply voltage of 2.5 V is only slightly crossed by the drain-source voltage of transistor M_3 in transient operation, the risk of hot carrier degradation and breakdown mechanisms in the stacked transistors is minimized.



(a) Transistor M_1

(b) Transistor M_2

(c) Transistor M_3

Fig. 5.9. Simulation of the drain-source to gate-source voltage transfer characteristic of the stacked nMOS transistors

The more the curves lean towards the bottom-left corner of the figures, the lower the risk of hot carriers and vice versa. This can intuitively be explained by the transistor biasing conditions. A large drain-source voltage creates a large electric field across the channel resulting in hot carriers. For low gate-source voltages, the transistor is "off" resulting in no current and hence no hot carriers. One can see that transistor M_3 thus will suffer the most from hot carrier effects compared to M_1 and M_2. However, since its drain-source voltage overshoot during the high-to-low transition of the output is less than 10% of V_{DD} and since its channel is not minimal length, the hot carrier generation in transistor M_3 is kept low. This low voltage overshoot is due to the voltage headroom, originating from the resistive division of the on-resistance with the output load.

Figure 5.9 also shows that the high-to-low transition of the output for the nMOS switch implementation is more critical than the low-to-high transition, since the high-to-low path leans more to the upper-right corner than the low-to-high path. Moreover, the voltage overshoot is larger with high-to-low transitions than with low-to-high transitions. This can clearly be seen in Figure 5.9(c).

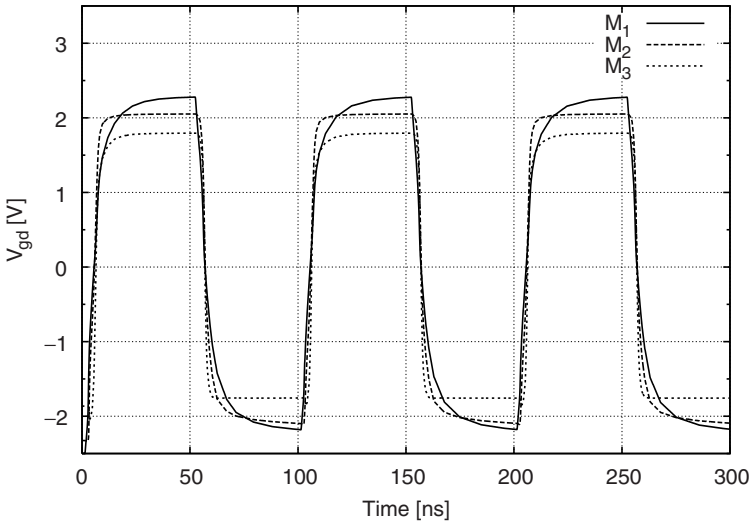


Fig. 5.10. Transient simulation of the gate-drain voltage of the nMOS stacked transistors

Finally, Figure 5.10 shows a transient simulation of the gate-drain voltages of the nMOS stacked transistors M_1, M_2 and M_3. Together with Figure 5.9 one can see that the voltages across the terminals of the stacked nMOS transistors remain within the limits of a standard 0.25 µm CMOS technology. The same results are obtained for the pMOS stacked transistors. One can conclude then that the bias circuit provides the correct gate voltages for the stacked transistors such that design rules of the used technology are fulfilled and reliable operation of the high voltage driver is guaranteed.

The Bias Circuit: Sizing

The complete bias circuit together with the stacked transistors is shown in Figure 5.11. The explanation for the sizing of the bias circuit is, like the analytical description, split into two parts: the steady state operation and the transient operation. Again, the calculations are solely given for that part of the bias circuit that drives nMOS stacked transistors. The results for the pMOS stacked transistors can be obtained in the same manner.

Steady State Operation

For the steady state, the resistors $R_{np1..4}$ and transistors M_{np45} are involved. The absolute resistor values are chosen high-ohmic in order to reduce the power dissipation.

First, consider the case when the output is high. The gate voltage $2\,V_{DD}$ of transistor M_3 is then given by the resistive division comprised of R_{n1} and

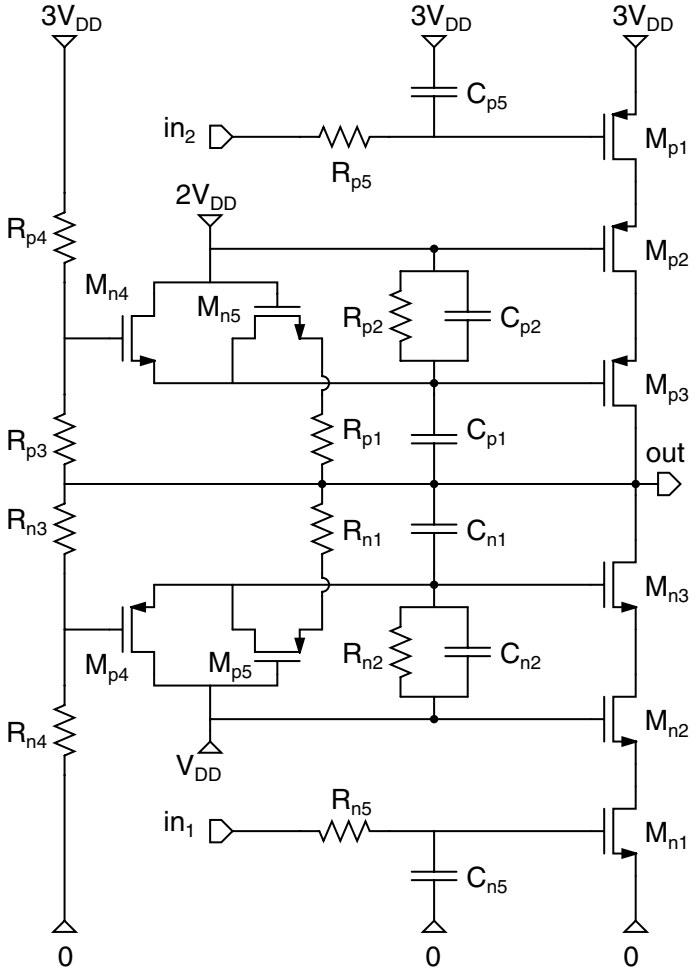


Fig. 5.11. Circuit schematic of the complete bias circuit with the nMOS and pMOS stacked transistors

R_{n2}, which is triggered on by transistor M_{p5}. The resistive division is defined between the high output voltage and the fixed gate voltage of transistor M_{n2}, V_{DD}. This leads to the ratio of the two resistors from which their values can be calculated. Transistor M_{p4} has to be in the cut-off region in this state. Since the gate of M_{n3}, which is also the source of M_{p4}, is at $2\,V_{DD}$ and the drain of M_{p4} is at V_{DD}, the gate of M_{p4} is set at $2\,V_{DD}$. This is done by the resistive division comprised of R_{n3} and R_{n4} between the high output voltage and the ground node. In this way, M_{p4} is set in the cut-off region and the voltage across its terminals remains within the technology limits. For the calculation of the resistive divisions the static efficiency of 90% is taken into account, which

Table 5.4. Resistor values of the bias circuit

R_{np1}	R_{np2}	R_{np3}	R_{np4}
85 kΩ	100 kΩ	42.5 kΩ	100 kΩ

Table 5.5. Transistor dimensions of the bias circuit

	M_{p4}	M_{p5}	M_{n4}	M_{n5}
W	24 µm	3.84 µm	14.4 µm	0.96 µm
L	0.24 µm	0.24 µm	0.24 µm	0.24 µm

means that the output is not completely charged or discharged to $3\,V_{DD}$ or *gnd* respectively. The ratio of R_{np1} on R_{np2} and R_{np3} on R_{np4} equals 0.850 and 0.425 respectively. The resulting resistor values are summarized in Table 5.4.

The dimensions of the transistors M_{np5} are determined by their maximum drain-source voltage drop in the linear region. This voltage drop is set low enough at 50 mV to minimize their influence on the resistive division $R_{np1} - R_{np2}$. The current through these transistors in the linear region can be approximated by $7.5/\left(R_{np1} + R_{np2}\right)$. Now the current through and the voltage over the transistors M_{np5} is known, one can calculate their on-resistance in the linear region. Using equation (4.1) one can calculate then the transistors widths.

Secondly, consider the case when the output is low. The gate voltage of V_{DD} for transistor M_{n3} is now directly given by the fixed gate voltage of transistor M_{n2} through transistor M_{p4}. In this state, transistor M_{p5} is in the cut-off region and as such, the resistive division $R_{n1} - R_{n2}$ is broken. Since the current for charging and discharging the gate of M_{n3} is mainly originating from the capacitors C_{n1} and C_{n2}, transistor M_{p4} only has to provide a fixed voltage to a high impedance node. Therefore, the on-resistance of M_{p4} does not have to be very low. A comparative assessment has been made between the on-resistance of M_{p4} and the RC-delay at its gate due to the resistors R_{n3}, R_{n4} and the input capacitance of M_{p4}. The resulting dimensions of the transistors M_{np45} of the bias circuit are given in Table 5.5.

Transient Operation

For the transient operation, the capacitors C_{np12} and the low-pass filters $R_{np5} - C_{np5}$ provide a solution to the transient voltage peaks on the terminals of the stacked transistors. The equations (5.20) and (5.25) derived in the previous section can be used as a guideline to determine the capacitor values of C_{np12}. The problem lies in the fact that the capacitors C_{np1} are connected in parallel with the gate-drain capacitances of the transistors M_{np3}, which are not constant during operation. The resulting capacitor values can be found in Table 5.6.

Table 5.6. Capacitor values of the bias circuit

C_{n1}	C_{n2}	C_{p1}	C_{p2}
3.5 pF	8.0 pF	6.0 pF	30.0 pF

Table 5.7. Parameter values of the low-pass filters

R_{n5}	C_{n5}	R_{p5}	C_{p5}
150 Ω	30 pF	100 Ω	10 pF

The parameters of the low-pass filters $R_{np5} - C_{np5}$ are arbitrarily chosen since the relationship between a step function at the input of a transistor's gate and the transient drain-source voltage peak of the transistor above it is not straightforward. If no low-pass filter is placed before the gates of the transistors M_{np1}, the transient voltage overshoot can be approximated by a triangular wave in the time domain. When the cut-off frequency of the low-pass filter is one decade lower than the fundamental frequency of this triangular wave, the transient voltage overshoot is sufficiently suppressed. The fundamental frequency is determined by simulation. The resulting parameter values of the low-pass filters are shown in Table 5.7.

The Bias Circuit: Power Dissipation

In Section 4.2.2 it was assumed that the power dissipation of the dedicated bias circuit can be neglected compared to the power dissipation of the stacked transistors. For a switching frequency of 10 MHz, the power dissipated in the bias circuit equals 5.5 mW. This is only 2.5% of the total output power of 220 mW, whereas the power dissipated in the stacked transistors reaches almost 30 mW, which is more than 13.4% of the total output power. The dynamic power losses due to the switching of the well-capacitors are still not included. However, this does not affect the calculation of the power dissipation for the bias circuit since the dimensions of the transistors in the bias circuit are small resulting in small well-capacitances. Therefore, this practical implementation proves this assumption.

The Level Shifter

Two control signals in_1 and in_2 are necessary for respectively switching the stacked transistors M_{np1} on or off as can be seen in Figure 5.11. For transistor M_{n1} the signal in_1 is defined between gnd and V_{DD}. For transistor M_{p1} the signal in_2 is defined between $2\,V_{DD}$ and $3\,V_{DD}$. The signal in_1 is externally applied to the circuit, so in_2 has to be derived by the level-shifter

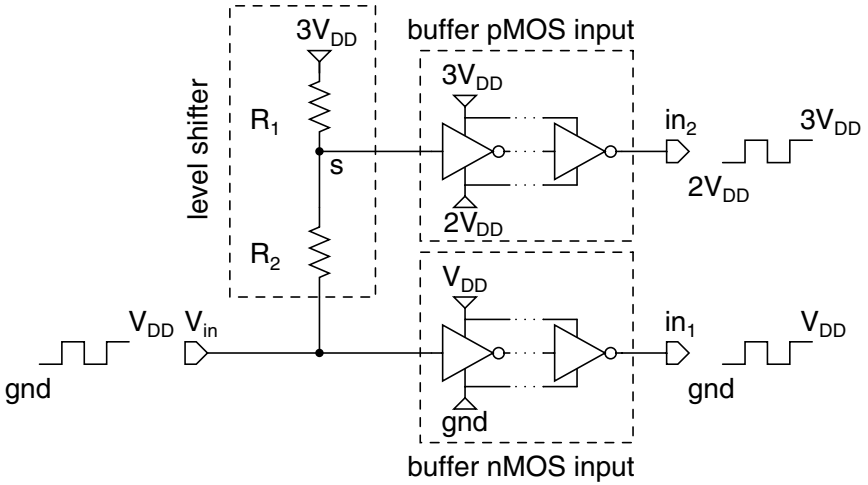


Fig. 5.12. Schematic of the level-shifter with the driving circuit and signals of the stacked transistors

from the signal in_1 on-chip. Since both transistors are driven by a tapered buffer, the requirements of the level-shifter translate into an output signal s that switches between the threshold voltage of the tapered buffer driving the pMOS transistor M_{p1}. This can be achieved with a resistive division between the high supply voltage at $3\,V_{DD}$ and the input signal V_{in}. A schematic of the level-shifter with the tapered buffers driving the transistors M_{np1} is shown in Figure 5.12.

The threshold voltage of the tapered buffer was chosen at half the supply voltage to maximize its noise margin. For the buffer driving the pMOS transistors the threshold voltage V_T equals thus $3\,V_{DD} - V_{DD}/2 = 5/2\,V_{DD}$. Therefore, the level-shifter must comply with the following inequalities:

$$3V_{DD}\frac{R_2}{R_1+R_2} = 3V_{DD} - V_{low} < V_T \tag{5.26}$$

$$V_{in} + (3V_{DD} - V_{in})\frac{R_2}{R_1+R_2} = 3V_{DD} - V_{high} > V_T \tag{5.27}$$

with V_{low} and V_{high} the voltage drop over R_1 when the input voltage V_{in} is at *gnd* or V_{DD} respectively. Elimination of the factor $\frac{R_2}{R_1+R_2}$ results in

$$3V_{DD}\frac{V_{high}}{3V_{DD} - V_{in}} = V_{low} \tag{5.28}$$

which leads to

$$3V_{DD} = V_{in}\frac{V_{low}}{V_{low} - V_{high}} \tag{5.29}$$

Assume now:

$$n = \frac{V_{low}}{V_{low} - V_{high}} \tag{5.30}$$

$$= \frac{3V_{DD}}{V_{in}} \tag{5.31}$$

with n a real number and $n > 1$. As V_{in} is defined at V_{DD}, n is the same as the voltage multiplication factor of the high voltage driver. In the case of the first test chip n equals 3. Equation (5.30) leads to the following relation between V_{low} and V_{high}:

$$V_{low} = \frac{n}{n-1} V_{high} \tag{5.32}$$

According to the equations (5.26) and (5.27) the following inequalities must be satisfied for a correct operation of the level-shifter:

$$3\ V_{DD} - V_{low} < \frac{5}{2}\ V_{DD} \tag{5.33}$$

$$3\ V_{DD} - V_{high} > \frac{5}{2}\ V_{DD} \tag{5.34}$$

Filling in equation (5.32) in (5.33) results in the following relationship:

$$\frac{V_{DD}}{2}\frac{n-1}{n} < V_{high} < \frac{V_{DD}}{2} \tag{5.35}$$

This relationship determines the value of V_{high} and with equation (5.30) V_{low} is also known. From equation (5.26) one can calculate now the ratio of the resistors R_1 and R_2 from the level-shift circuit.

$$\frac{R_1}{R_2} = \frac{V_{low}}{3V_{DD} - V_{low}} \tag{5.36}$$

One chooses now for R_1 (or R_2) a high-ohmic value, to minimize the power dissipation of the level-shift circuit. According to equation (5.36) one can calculate R_2 or (R_1). V_{low}, V_{high}, R_1 and R_2 are now determined for a specific high supply voltage.

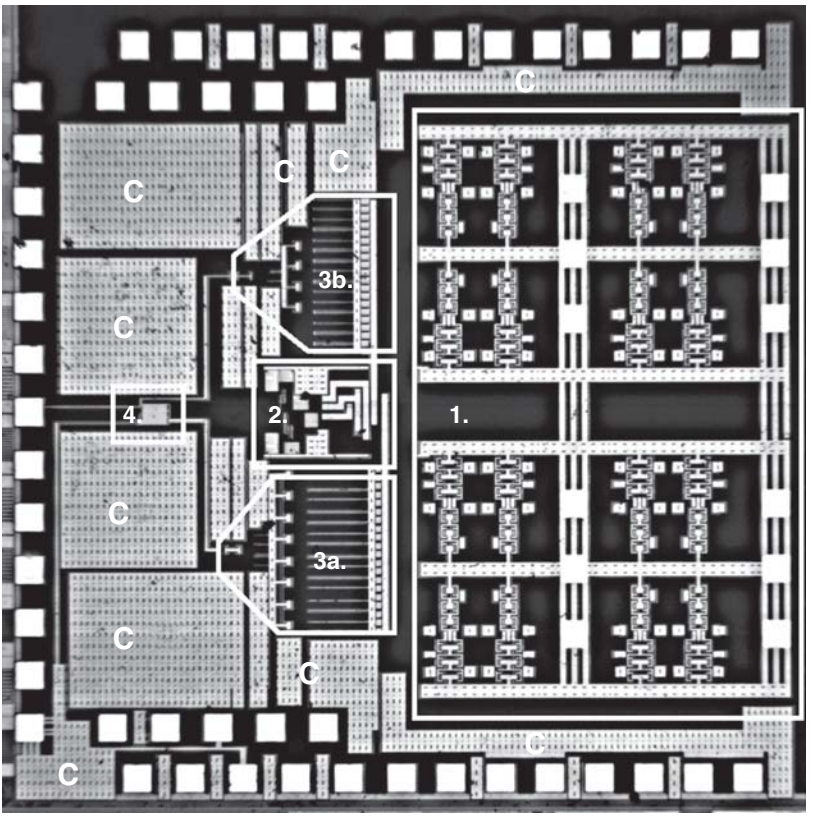
The design plan for the level-shift circuit can be summarized in three consecutive steps:

- Determine the voltage multiplication factor n.
- Calculate V_{low} and V_{high} from the voltage multiplication factor n using the equations (5.32) and (5.35).
- Calculate R_1 and R_2 from equation (5.36).

The voltage multiplication factor of the first test chip was set at 3, leading to a high supply voltage of 7.5 V. Following the design plan of the level-shift circuit, the ratio of R_1 on R_2 is about 0.23. This resulted in resistor values of 23 kΩ and 100 kΩ for R_1 and R_2 respectively.

5.1.3 Layout Aspects

The chip photograph of the high voltage driver is depicted in Figure 5.13. All the described building blocks are clearly visible. The remaining area is filled with decoupling capacitors. For this switching high voltage driver, it was aimed towards a decoupling of every (sub-) building block separately and as close to the building block as possible to maximize the decoupling effect. The stacked transistors occupy one half of the chip area. This area is determined by the on-resistance of the driver and the electro-migration rules of the technology for the metal layers. The chip area is 2.4 x 2.4 mm^2. The technology used was a 1P5M 2.5 V 0.25 µm twin well CMOS technology.



Legend:
1: Stacked Transistors, 2: Bias Circuit, 3ab: Tapered Buffers
4: Level Shifter, C: Decoupling Capacitances

Fig. 5.13. Chip photograph of the high voltage driver in a 2.5 V 0.25 µm CMOS technology

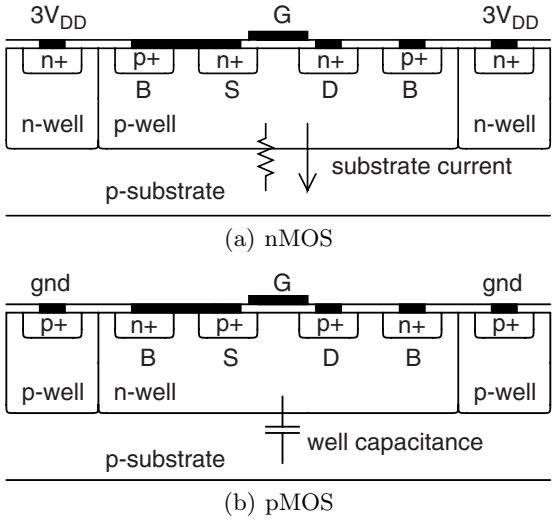


Fig. 5.14. Cross section of the layout of a typical n- and pMOS transistor

To limit the gate-bulk voltages, the bulk and source of every transistor is shorted. A disadvantage of this principle in a twin well technology is that it results in substrate currents near each nMOS transistor and a well-capacitance near each pMOS transistor. Since the substrate is high-ohmic (20 Ωcm), special attention went to the prevention of latch-up. First, every transistor is surrounded by a full guard ring to make a good well contact. Second, all nMOS transistors are encircled by an n-well biased at the highest supply voltage and all pMOS transistors are encircled by a p-well biased at the lowest supply voltage. In this way, substrate currents are drained by the wells and the interaction between the transistors is minimized. A cross section of the layout of a typical nMOS and pMOS transistor is shown in Figure 5.14 with their parasitic substrate resistor or well-capacitor pointed out.

Layout of the Stacked Transistors

The layout of the stacked transistors is not straightforward. A first issue that has to be solved is how to layout these large transistors. According to Table 5.1 the widths of the p- and nMOS stacked transistor equals 6.4 mm and 1.6 mm respectively. Therefore, the output stage is divided into 16 parallel output stages. One such output stage is laid out in a subcell in a way that all conductors have a sufficient width to cope with 1/16 of the total current. Figure 5.15 shows the mirror and copy operation of the subcell to form the complete output stage. The subcell is mirrored and copied four times to form an array of four by four subcells, which form together the 16 parallel output stages.

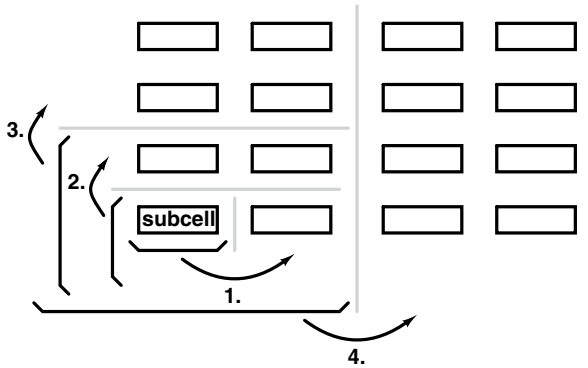


Fig. 5.15. Mirror and copy operation of the subcell

By using this technique, a symmetrical layout is obtained, despite the large difference in widths between a nMOS and pMOS stacked transistor.

A second issue that has to be taken into account is the presence of substrate currents. The intermediate nodes of the nMOS stacked transistors can be charged up to a multiple of V_{DD} due to the bulk-source connection. Therefore, the nMOS transistor with the highest bulk voltage in the subcell is placed as far as possible from the nearest ground contact to maximize the substrate resistance of that path. In this way, the losses due to the substrate resistance can be minimized. A cross section of the layout of a subcell is shown in Figure 5.16. The naming conventions of the stacked transistor are taken from Figure 5.11. However, their order in the circuit schematic does not match the order in layout. Since the bulk voltage of transistor M_{n3} can raise up to $2\,V_{DD}$, it is thus placed as far as possible from the nearest ground contact, which is in this case the bulk of transistor M_{n1}. The order of the nMOS stacked transistors is then copied to the pMOS stacked transistors to preserve a symmetrical layout.

Since the bulks of the stacked transistors are not on the same potential during operation, they have to be separated from each other by wells, as mentioned earlier in this paragraph. A p-well is used to separate the pMOS transistors and an n-well is used to separate the nMOS transistors. The highest voltage across a pn-junction is $3\,V_{DD}$ as can be seen in Figure 5.16. A rule of thumb to determine the width d of the wells is that the width of the space charge region in the n- or p-well must be lower than this width. The width of the space charge region is proportional to the root of the reverse bias voltage across the junction. Therefore, a safe margin is obtained if the widths of the wells are taken one order of magnitude larger than the minimum width described by the technology. Eventually, the limitation of stacking more transistors to increase the supply voltage will be limited by the breakdown voltage of a pn-junction of the used technology.

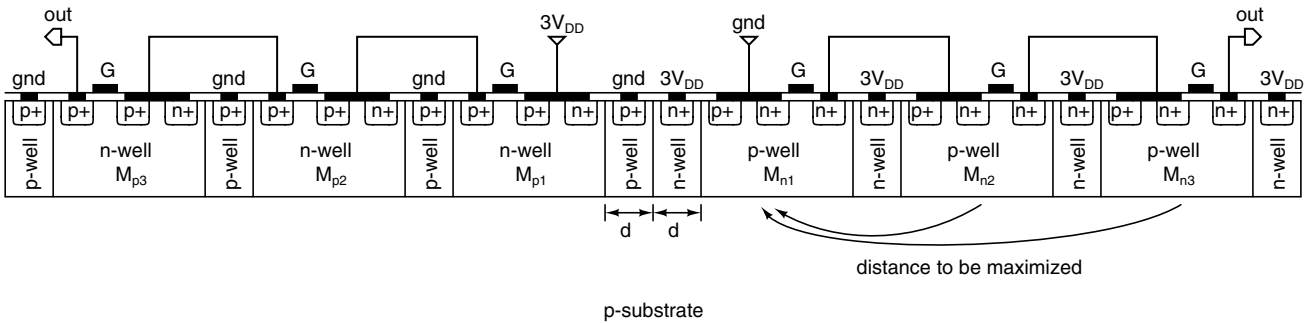


Fig. 5.16. Cross section of the layout of a subcell

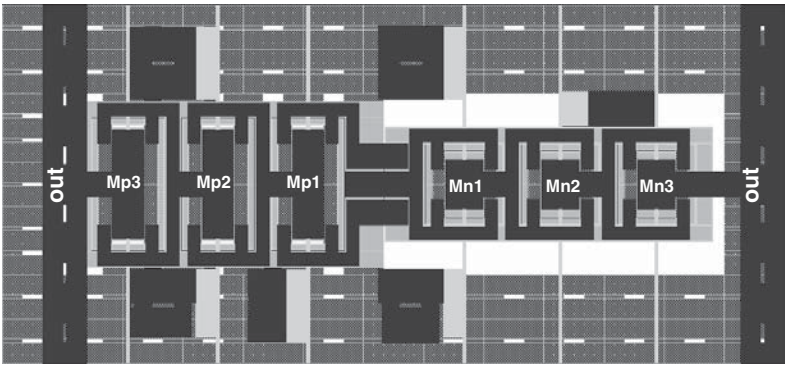


Fig. 5.17. Layout of a subcell

Figure 5.17 shows a screen-shot of the layout of the subcell with the order of the stacked transistors indicated. The area of the subcell measures 390 µm x 178 µm. The ground conductor of the subcell uses metal 1 to provide substrate shielding, while the $3\,V_{DD}$ supply voltage is laid out on top of the ground conductor using metal 2. This provides a parasitic decoupling capacitance distributed over the complete output stage. The output signal, is by means of a maximum number of vias, directed to metal 4 and 5. Both metals will form the output conductor. In this way its width can be limited. The widths of all the metal conductor lines are determined in such way to minimize the electromigration process. As a rule of thumb, a width of 1 µm per 1 mA DC-current is taken.

Other Aspects

For the layout of the tapered buffers, the same principle is used as for the stacked transistors. The tapered buffers are split into several parallel tapered buffers to lower the current densities per subcell and to ease the layout of the large transistors in the final stages of these buffers. The bias circuit is placed central between the two tapered buffers to provide matched delay paths for the gates of the stacked transistors.

Now the layout of the stacked transistors is finished, the well-capacitances can be calculated. The area of the junction between the n-well and the p-substrate of a pMOS stacked transistor in the subcell measures $2.34 \cdot 10^{-9}\ \mathrm{m}^2$. 16 of these subcells in parallel results thus in a total junction area of $3.75 \cdot 10^{-8}\ \mathrm{m}^2$. With a junction capacitance c_j of $3.13 \cdot 10^{-4}\ \mathrm{F/m}^2$ this leads to a well-capacitance of 11.7 pF. Following equation (4.15) the α-factor equals 7.3. With this factor, one can estimate the well-capacitances for the next designs. By using equation (4.14) one can calculate a power loss of 3.6 mW due to the charging and discharging of the well-capacitances.

5.1.4 Power Dissipation

The total power dissipation of the high voltage driver depends on the dimensions of the stacked transistors. The static efficiency of the driver was set at 90% leading to the dimensions of these transistors. From Section 4.2.2 it is known that there exists an optimum between the static and dynamic power dissipation in function of the width of the stacked transistors. Too large dimensions results in a high dynamic power dissipation. Too small dimensions results in a high static power dissipation. Since most terms of the dynamic power dissipation are only known after design, or in the case of the well-capacitances, after layout, a continuous iteration process is necessary to determine the dimensions for the stacked transistors.

Now the design and layout of the first test chip is completed, a final comparison between the static and dynamic power dissipation can be made. The total dynamic power losses, including the contributions of the tapered buffers, the gate capacitances of the stacked transistors, the bias circuit and the well-capacitances, equals 18.8 mW, which is lower than, but in the same order of magnitude, as the static power losses of 22 mW. Therefore, the design choice for a static efficiency of 90% was not too optimistic and as such there is no iteration step necessary. The overall efficiency, including static and dynamic power losses, equals now 84%.

5.1.5 Measurements

Measurement Setup

The chip is wire bonded on a ceramic thick film substrate. The substrate was mounted in a copper beryllium box for better shielding. An example is shown in Figure 5.18. All the supply lines were decoupled on the substrate.

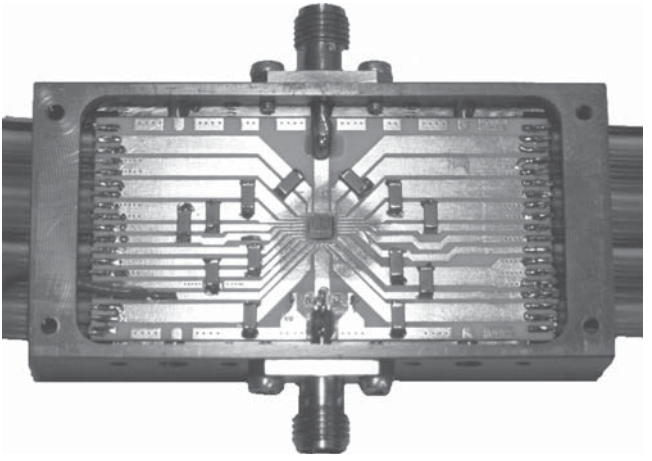


Fig. 5.18. Photograph of the chip, wire bonded on a ceramic substrate

The test signals were generated using a Sony Tektronix arbitrary waveform generator. Time domain measurements were performed with the Tektronix 7854 oscilloscope. For the spectral measurements, a Hewlett Packard 3585B spectrum analyzer was used. The three supply voltages, V_{DD}, $2\,V_{DD}$ and $3\,V_{DD}$ are decoupled by a parallel connection of several off chip capacitors, all mounted on a Printed Circuit Board (PCB).

Unmodulated Square Wave Input

First the response to an unmodulated square wave has been measured. A square wave, defined between *gnd* and V_{DD}, with a frequency of 10 MHz and a duty cycle of 50%, is applied to the high voltage driver. The result is shown in Figure 5.19. An output swing of 6.46 V is measured over a 50 Ω load in parallel with a capacitance of 20 pF. This corresponds to an output power of 208 mW. The measured on-resistance is 5.9 Ω. Using equation (5.1) this results in a static efficiency of 89%, which is very close to the presupposed design choice of 90%. The total power dissipation is 520 mW. This results in an overall efficiency of 40%. The deviation of this result compared to the calculated efficiency is due to the substrate losses. This topic is discussed in Section 5.1.6. The delay of the high voltage driver is 16 ns.

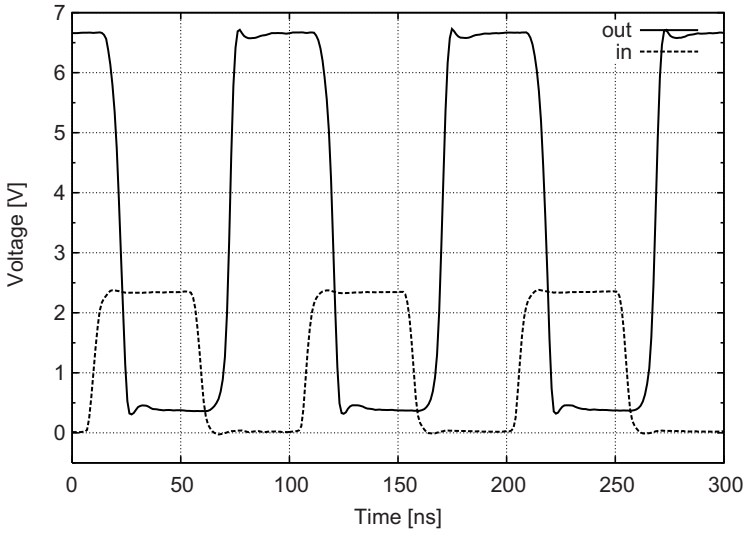


Fig. 5.19. Time domain measurement with an input square wave of 10 MHz

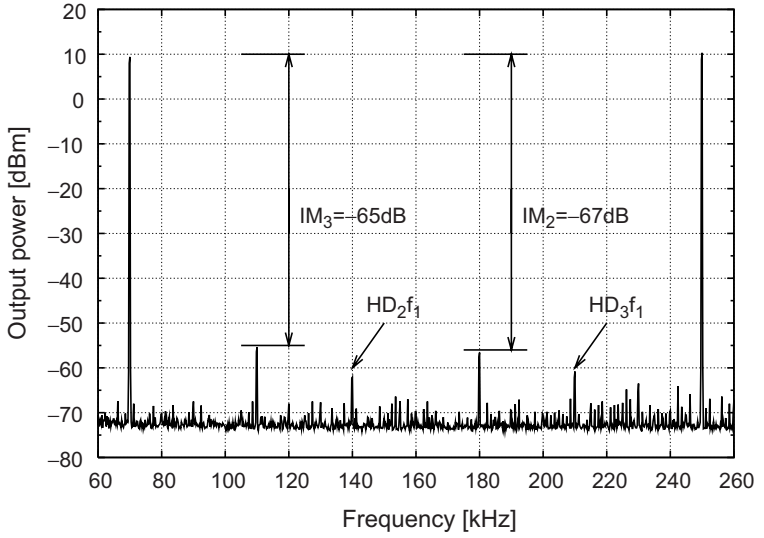


Fig. 5.20. Distortion measurement with a dual-tone sinusoid at 70 kHz and 250 kHz

Pulse Width Modulated Square Wave Input

Figure 5.20 depicts the intermodulation distortion performance of the high voltage driver by applying a PWM signal at the input of the chip. The PWM test-signal was generated by a fourth-order $\Delta\Sigma$ single-bit ADC with a sample rate of 20 MS/s. The input of this converter is a dual-tone sine wave at 70 kHz and 250 kHz. This intermodulation distortion measurement is a true distortion measurement and is preferred above a harmonic distortion measurement with a single sine wave input. After all, the intermodulation products of a dual-tone sine wave generates in-band distortion terms which cannot be filtered out. The second-order Intermodulation Distortion Product (IM_2) is defined as the ratio of the signal amplitude and the distortion peak, generated at $f_1 \pm f_2$ and the IM_3 is defined as the same ratio, but with distortion peaks generated at $2f_1 \pm f_2$ and $f_1 \pm 2f_2$. An IM_3 of -65 dB and an IM_2 of -67 dB is obtained for the high voltage driver. The other spurious, marked in Figure 5.20, are the second-order Harmonic Distortion Term (HD_2) and the HD_3 of the 70 kHz sine wave. It can be clearly seen that these spurious are lower than the intermodulation products, which underlines the importance of an intermodulation distortion measurement. The measured spurious are also in accordance with the results derived in [San99b] which state that $IM_2 = 2HD_2$ and $IM_3 = 3HD_3$.

Overview

Table 5.8 gives a summary of the measurement results.

Table 5.8. Measured performance and process specifications

Parameter	Measured
Technology	0.25 µm CMOS
Nominal supply voltage	2.5 V
Supply voltage	7.5 V
Load resistance	50 Ω
Output swing	6.46 V
Delay	16 ns
on-resistance	5.9 Ω
Square wave performance	
Frequency	10 MHz
P_{out}	208 mW
Efficiency	40%
PWM performance	
IM_3	−65 dB
IM_2	−67 dB

5.1.6 Discussion of the Results

Strong Points

The most remarkable results of this test chip included:

- The feasibility of a high voltage driver processed in a standard 2.5 V 0.25 µm CMOS technology without the use of extra mask sets or process steps. This opens the possibility to integrate high voltage power amplifiers in mainstream deep-submicrometer CMOS technologies.
- A supply voltage of 7.5 V is reached with an absolute minimum of 3 stacked transistors per switch. Using less stacked transistors would result in reliability issues as described in Section 4.1.5.
- The chips have proven to be reliable and no electro-migration and hot carrier degradation effects were noted during measurements.

Efficiency Issues

The measured efficiency of 40% deviates seriously from the calculated efficiency of 84%. This is due to an incorrect calculation of the resistances through the substrate between the bulks of the nMOS transistors and their nearest ground contacts. This resistance can be calculated as follows:

$$R = \frac{R_{substr} L}{A} \tag{5.37}$$

With $R_{sub} = 20\Omega cm$, A the area of the junction between the p-well of the nMOS transistor and the substrate and L the distance of the center of this junction area to the nearest ground contact.

The most important resistances are located at the sources of the stacked transistors M_{n2} and M_{n3} and at the sources of the nMOS transistors in the tapered buffer driving the pMOS input. This results in the resistors R_{S1}, R_{S2} and R_{S3} as shown in Figure 5.21. For the resistors R_{S1} and R_{S2} equation (5.37) is used to calculate the resistance through the substrate for one subcell. One has to divide this resistor value through 16, since the stacked transistors are laid out in 16 parallel subcells. The same principle can be followed to calculate R_{S3}. Table 5.9 shows the resulting resistor values extracted from the layout of the test chip.

If the resistances through the substrate are calibrated out, an efficiency of 73% is obtained, which is much closer to the calculated efficiency of 84%. One can conclude then if one wants to use the principle of stacked devices

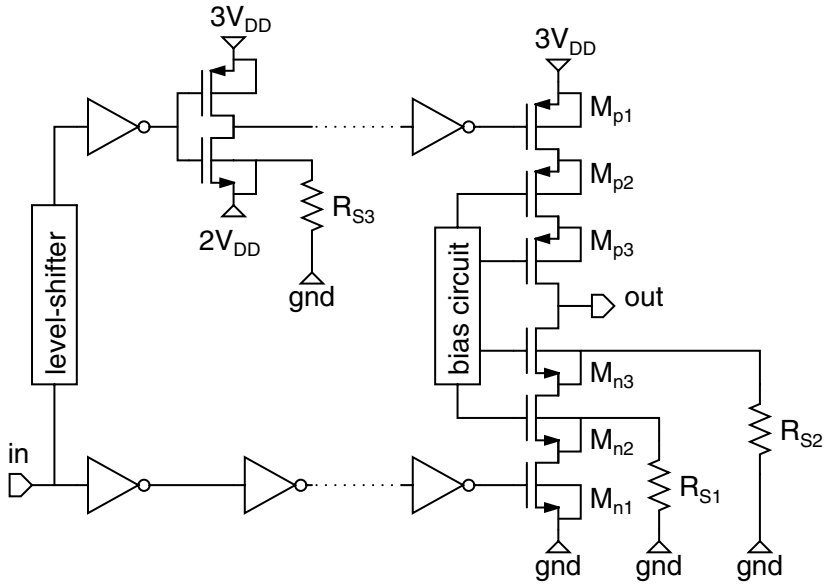


Fig. 5.21. Schematic of the high voltage buffer with the different resistances through the substrate pointed out

Table 5.9. Substrate resistances

R_{S1}	R_{S2}	R_{S3}
81 Ω	470 Ω	224 Ω

in a twin-well technology for going towards high voltage operation, one must organize the layout as such that the resistances through the substrate are at least larger than 1 kΩ. If this results in a too large area waste in layout, one should consider the use of a triple-well technology.

Needed Improvements

As stated in the beginning of this chapter, the goal of the first test chip was to prove the concept of stacked devices to design a high voltage switching type output driver in a standard low voltage CMOS technology. So it was not the ambition to design a high voltage output stage for the SOPA architecture, which is fully compatible with the aDSL system. The feasibility of the technique is demonstrated with this first test chip. However, several improvements can be made:

- The bias circuit is largely comprised of passive elements for which the sizing is not straightforward. A simplified architecture, where the resistors are replaced by active elements in the linear region, should ease the extension of the bias circuit to $4\,V_{DD}$ or $5\,V_{DD}$ buffers.
- The relative large delay is mainly due to the low-pass filtering in the bias circuit. These filters are placed before the nMOS and pMOS inputs. If the high voltage buffer is integrated into the SOPA structure, a reduction of the delay becomes necessary. After all, to make sure that the SOPA's oscillation frequency is determined by the cut-off frequency of the loop filter, the delay in the forward path of the SOPA has to be about one order of magnitude smaller than switching period.
- If the delay of the high voltage buffer can be sufficiently reduced, the short circuit currents through the stacked transistors should be minimized. By integrating a non-overlapping switching circuit, the power dissipation can be further reduced.
- The level-shifter does not generate a full-swing square wave signal. Instead, it switches between two levels just above and just below the threshold voltage of the tapered buffer that drives the pMOS input. Therefore, the buffer has to convert the output of the level-shifter to a full-scale square wave signal with $2\,V_{DD}$ and $3\,V_{DD}$ as low and high levels respectively. This results in unmatched delay paths between the nMOS and pMOS input causing distortion at the output.
- The use of a twin-well technology results in large losses through the substrate. In order to minimize these losses and still preserve a relative compact layout, it is better to use a triple-well technology.

5.2 A 5.5 V Output Driver in a 1.2 V 130 nm CMOS Technology

5.2.1 Introduction

While the first test chip proved the feasibility of high voltage design in a standard low voltage deep-submicron CMOS technology, the goals of the second test chip were set more ambitiously. With five stacked transistors a solution is provided to circumvent the low supply voltages of modern nanometer CMOS technologies. Moreover, the high voltage output buffer should fit into the SOPA architecture such that the line driver complies with the newest xDSL specifications. The prototype was implemented in a standard 1.2 V 130 nm triple-well CMOS technology. This high voltage buffer is used as the output stage of the aDSL2+ CO SOPA line driver, which is described in Chapter 6. A test structure of the output buffer was placed on the same die as the line driver such that it could be characterized separately.

Figure 5.22 depicts the block schematic of the high voltage buffer. The output stage is composed of five stacked transistors for the pull-up switch and

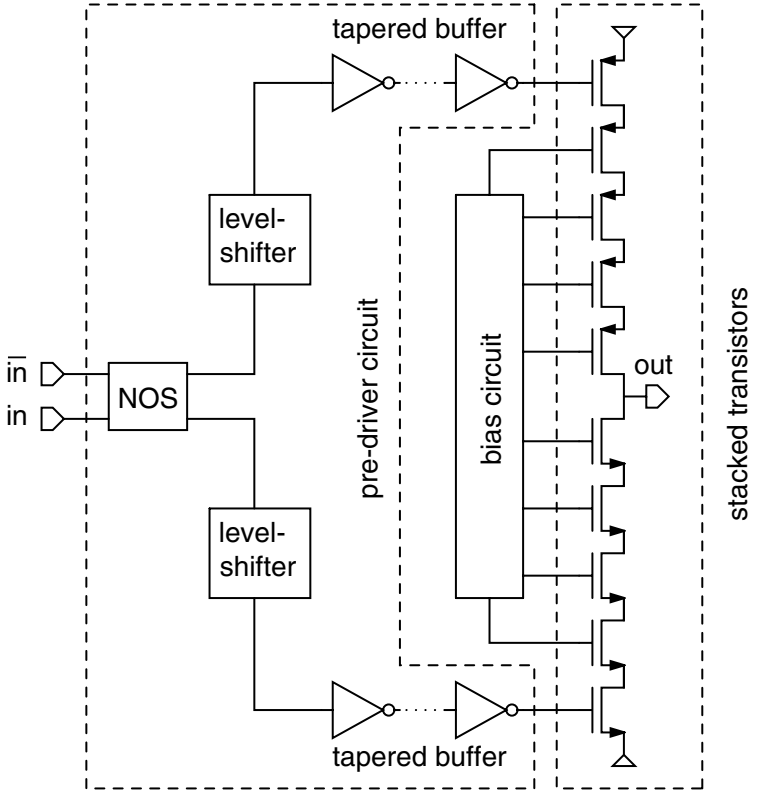


Fig. 5.22. Block schematic of the high voltage output buffer

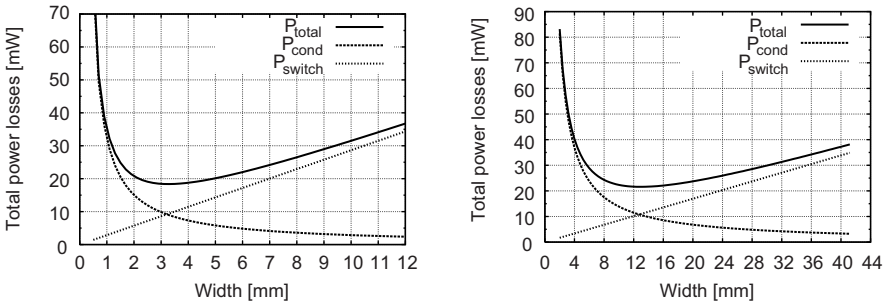
the pull-down switch respectively. The theoretical maximum supply voltage of the buffer is thus five times V_{DD}. A novel dedicated bias circuit was designed to keep the voltage across the terminals of the stacked transistors within the technology limit, the nominal supply voltage V_{DD}. The output of the buffer is controlled by the outer stacked transistors, which are driven by a tapered buffer. Distortion of the output waveform is minimized by providing matched delay paths from the input of the driver to the outer stacked transistors. This approach uses a symmetrical supply with two level-shift circuits for setting the offset voltages of the pMOS- and nMOS buffer. The level-shifters are preceded by a Non-Overlapping Switching (NOS) circuit, to minimize the power dissipation due to short circuit currents. The combination of the NOS, the tapered buffers and the level-shifters form the pre-driver circuit of the outer stacked transistors. In the next section, the design of each building block will be discussed.

5.2.2 Building Block Design

The Stacked Transistors

Since the high voltage driver is tailored to suit as the output stage of a SOPA xDSL line driver, it has to be able to transmit the full aDSL output power. As such, the equations (4.3) and (4.4) have to be used to determine the transformer ratio and the equivalent load resistance. The nominal supply voltage of the used technology equals 1.2 V and the voltage multiplication factor n was set at 5. This results in a transformer ratio rounded to 5 and a load resistance of 4 Ω.

Now the well-capacitances of the stacked transistors can be estimated, using the layout of the first test chip, the total power losses of the output buffer can be calculated for driving a 4 Ω load with a switching frequency of 40 MHz. The result is shown in Figure 5.23. Since only an estimation of the



(a) nMOS stacked transistors, n=5 (b) pMOS stacked transistors, n=5

Fig. 5.23. Estimation of the total power losses in function of the width of the stacked transistors

Table 5.10. Stacked transistor sizing

	pMOS	nMOS
W	15.156 mm	3.407 mm
L	130 nm	130 nm
C_{in}	29.1 pF	6.5 pF

dynamic power losses can be made, these results cannot be taken for granted, but they can serve as a guideline to determine the dimensions of the stacked transistors.

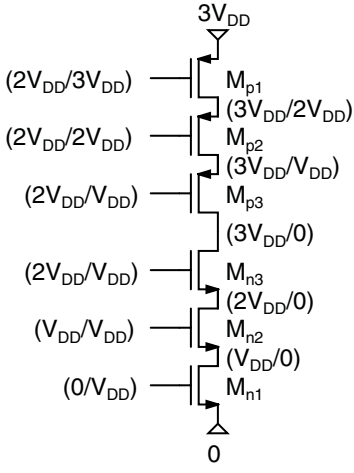
Using Figure 5.23, the total static power losses are set at 25 mW, since this roughly corresponds with the minimum of the total power losses. As a result, the static efficiency equals 80%. Using equation (4.10), this leads to a switch resistance of 1.0 Ω or an on-resistance of 0.2 Ω per transistor. Such a large on-resistance results in large transistor dimensions, which are summarized in Table 5.10 together with their input capacitances. The transistors are sized at minimal gate length in order to limit the transistor's widths and, as such, to limit the dynamic power dissipation. The widths of the stacked transistors correspond well with the minimum of the total power losses that can be read from Figure 5.23.

The Bias Circuit: Architecture Development

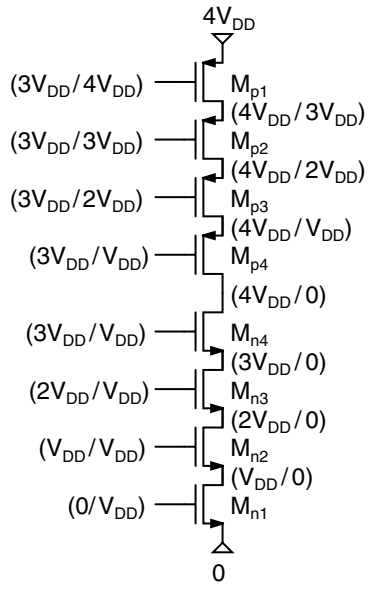
The design and analysis of the bias circuit of the first test chip was not straightforward, due to its large number of passive elements. Moreover, the architecture does not lend itself for voltage multiplication factors higher than three, since this will result in a huge increase in passive elements. Therefore, a new architecture for the bias circuit is developed. The number of passive elements should be minimized to lower the complexity and the power losses of the bias circuit. On top of that, the architecture should be easy to adapt for higher voltage multiplication factors.

For starting the development of the novel bias circuit, the node voltages of the stacked transistors are compared for different values of the voltage multiplication factor to search for some regularities. The node voltages for a $3\,V_{DD}$, $4\,V_{DD}$ and $5\,V_{DD}$ output stage in steady state operation are shown in Figure 5.24. For reasons of simplicity, the voltages are defined between 0 and nV_{DD} without taking the on-resistance and the threshold voltage of the transistors into account. The node voltages are shown between brackets. The first value gives the corresponding voltage for when the output is high. The second value gives the corresponding voltage for when the output is low. These voltages are chosen such that the voltage across the terminals of the stacked transistors does not cross the nominal supply voltage V_{DD}. The following remarks can be made:

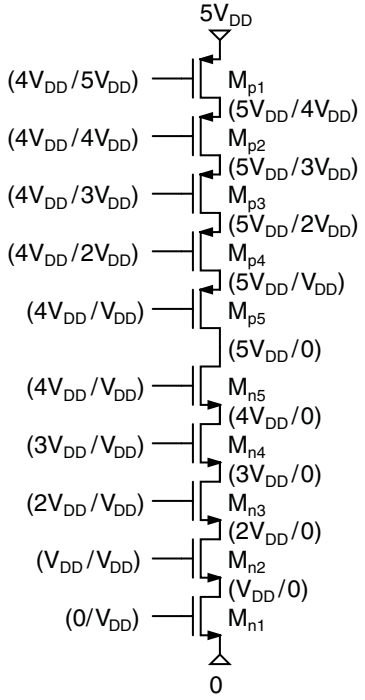
- n supply voltages are necessary for biasing n stacked transistors.
- The voltage between two consecutive gates never exceeds V_{DD}.



(a) $3V_{DD}$ output stage



(b) $4V_{DD}$ output stage



(c) $5V_{DD}$ output stage

Fig. 5.24. Node voltages of the stacked transistors for a $3\,V_{DD}$, $4\,V_{DD}$ and $5\,V_{DD}$ output stage

- The transistors M_{n2} and M_{p2} can be biased at a fixed voltage of V_{DD} and $(n-1)V_{DD}$ respectively.
- The gates of the transistors M_{nn} and M_{pn} have the same bias voltages.
- The output voltage is controlled by switching the outer stacked transistors M_{n1} and M_{p1} on and off. The bias voltages of the other stacked transistors have to follow this switching scheme in order to limit the voltage across their terminals.

With these remarks taken into account, one can construct the bias circuit for every value of the voltage multiplication factor. As an example the $5\,V_{DD}$ output stage is taken. First, the focus is set on the biasing of the nMOS stacked transistors. The gate of transistor M_{n2} is set at a fixed voltage of V_{DD}. When the output is low, the gates of the transistors M_{n3}, M_{n4} and M_{n5} have to be set at a voltage V_{DD}. Since the voltage between two consecutive gates never exceeds the nominal supply voltage V_{DD}, these bias voltages can be set by pMOS transistors in the linear region. They pass the fixed bias voltage, V_{DD}, of transistor M_{n2} to the gates of the other stacked transistors. Off course, when the output is high this path has to be broken. This leads to the circuit schematic of Figure 5.25(a), where the transistors M_{bp1}, M_{bp2} and M_{bp3} provide the V_{DD} bias voltage in the low output state. The switching sequence for these bias transistors can be found on the drain-source contacts of the stacked transistors. This results in the circuit schematic of Figure 5.25(b).

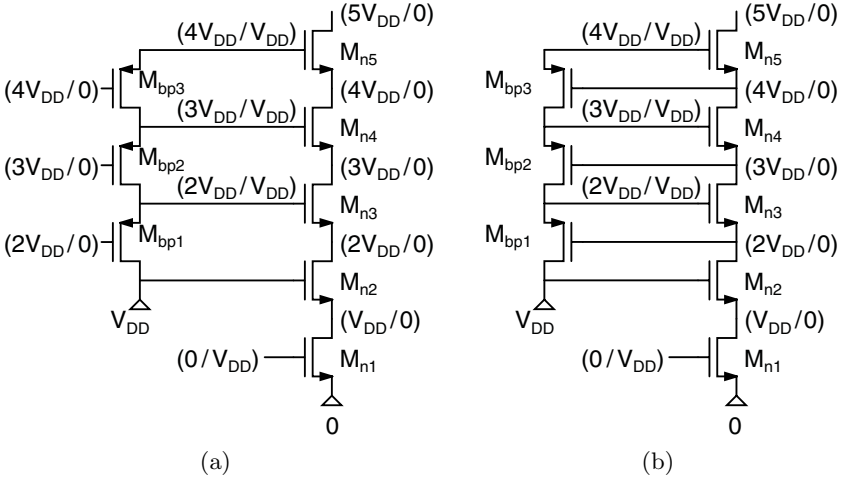


Fig. 5.25. Implementation of the bias circuit for when the output is low

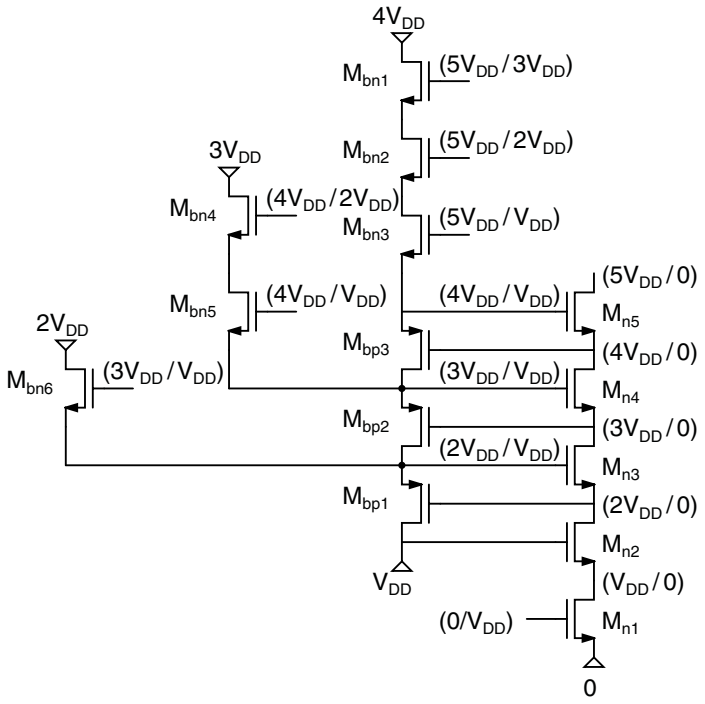


Fig. 5.26. Implementation of the bias circuit for when the output is high

When the output is high, the gate voltages of the transistors M_{n3}, M_{n4} and M_{n5} have to be set at $2\,V_{DD}$, $3\,V_{DD}$ and $4\,V_{DD}$ respectively. These bias voltages are externally applied. Via nMOS stacked transistors in the linear region, the voltages are passed to the gates of M_{n3}, M_{n4} and M_{n5}. This is shown in Figure 5.26. Since the lowest bias voltage of these gates equals V_{DD}, there are respectively 1, 2 and 3 stacked nMOS transistors necessary to reliably pass the three supply voltages. Now, when the output is low, these bias transistors should be in the off-state. Figure 5.26 also shows the switching sequence of the bias transistors M_{bn1} to M_{bn6}. One can see that the bias voltages of the transistors M_{bn5} and M_{bn6} correspond with the bias voltages of the transistors M_{n5} and M_{n4}. The bias voltages of the remaining transistors M_{bn1} to M_{bn4} can be found on the internal nodes of the pMOS stacked transistors, as can be seen in Figure 5.24(c). Therefore, in steady state operation the biasing of the nMOS stacked transistors is completely covered by switching active elements. Moreover, the signals necessary for switching these active devices can be found on the internal nodes of the stacked transistors.

For the biasing of the pMOS stacked transistors, the same strategy can be used. The gate of transistor M_{p2} can be set at a fixed voltage of $4\,V_{DD}$. The gates of the transistors M_{n5} and M_{p5} can be connected, since they have the same switching scheme. Therefore, the biasing of M_{p5} is already covered. Moreover, the bias transistors M_{bn1}, M_{bn2} and M_{bn3} which pass the $4\,V_{DD}$

voltage to the gates of M_{n5} and M_{p5} when the output is high, can also be used to pass this voltage to the gates of the transistors M_{p3} and M_{p4} for the high output state. On the other hand, when the output is low, the transistors M_{p3} and M_{p4} respectively have to be biased at $3\,V_{DD}$ and $2\,V_{DD}$. These voltages are set using pMOS stacked transistors M_{bp4} to M_{bp6} following the same principle as with the nMOS stacked transistor biasing circuit. The complete bias circuit implementation is depicted in Figure 5.27.

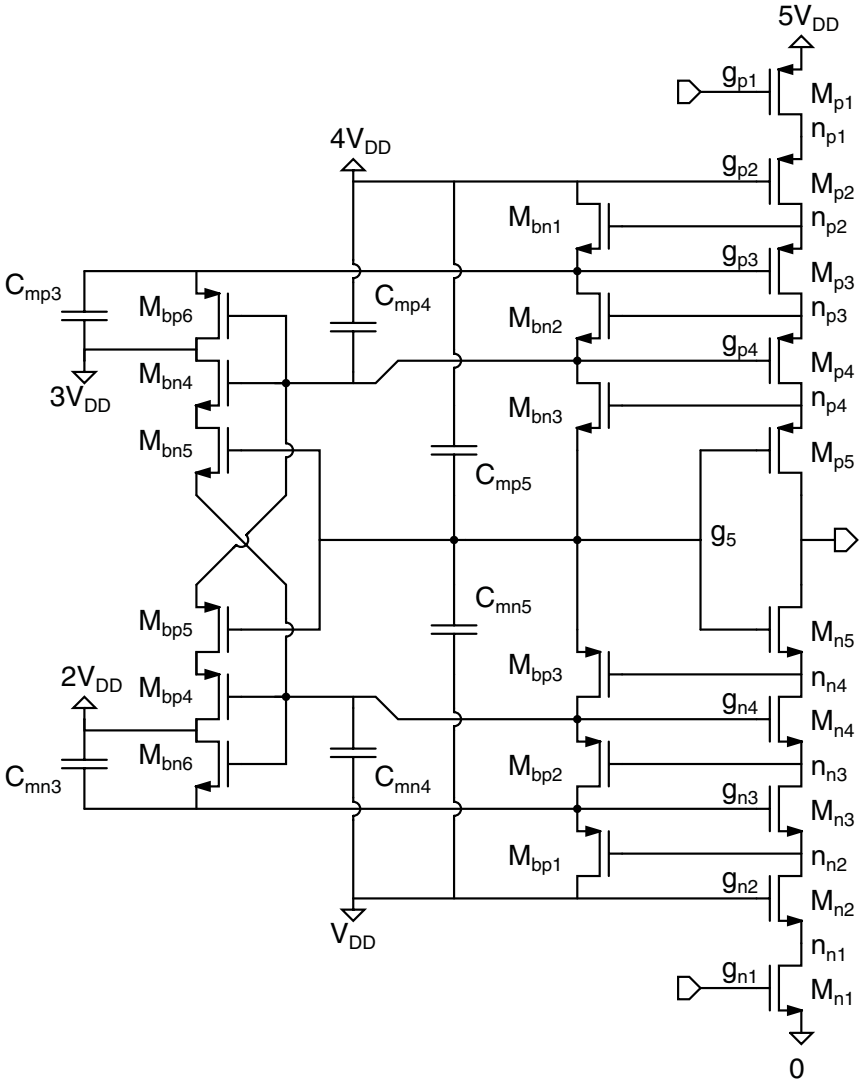


Fig. 5.27. Bias circuit implementation for the 5 V_{DD} output stage

For the transient operation, a distinction has to be made between a low-to-high and a high-to-low transition of the output. The focus is again set on the nMOS stacked transistor biasing circuit. The same reasoning applies for the complementary pMOS stacked transistors biasing circuit. For a low-to-high transition, it is known from the first test chip that the gates of the stacked transistors need to be decoupled due to the large gate-drain capacitances. These decoupling capacitors are also shown in Figure 5.27. The problem of the transient voltage peaks that occur during the high-to-low transition of the output is now solved without placing extra gate-drain capacitance, which was the case for the first test chip. The problem lies in the fact that the sources of the transistors M_{n2} to M_{n5} are faster discharged that their drains. This is now solved by the feedback provided through the transistors M_{bp1}, M_{bp2} and M_{bp3}. When, for example, the source of transistor M_{n3} gets discharged, transistor M_{bp1} switches on. As a consequence, the terminals of M_{n3} are discharged with the same speed. The same principle applies for the transistors M_{n4} and M_{n5}.

That the architecture is easy to adjust for higher voltage multiplication factors is shown in Figure 5.28. This figure depicts the bias circuit for n nMOS

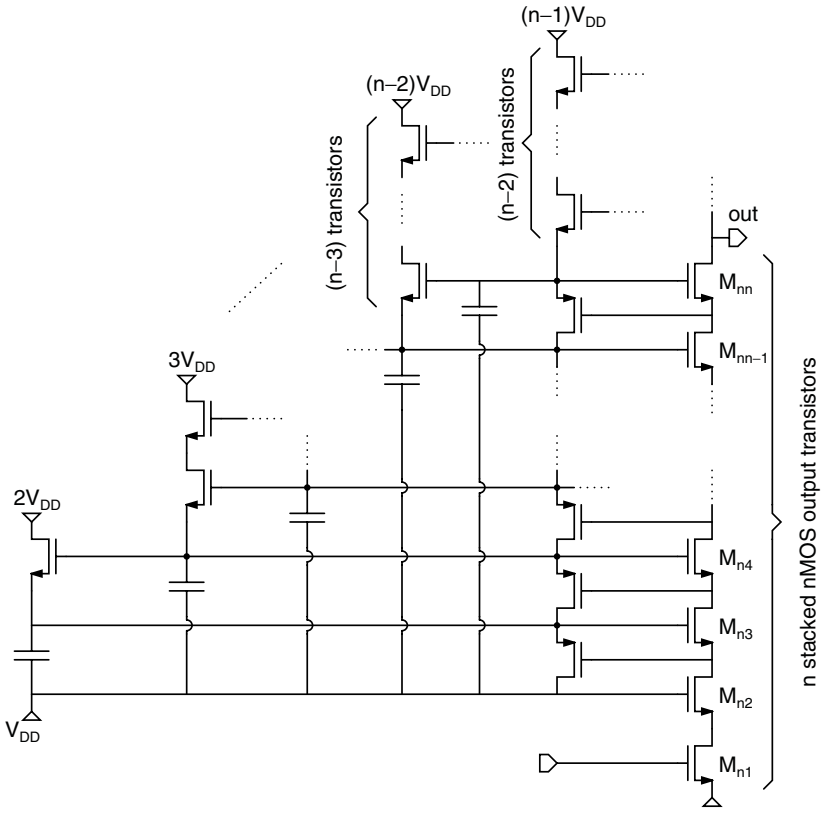


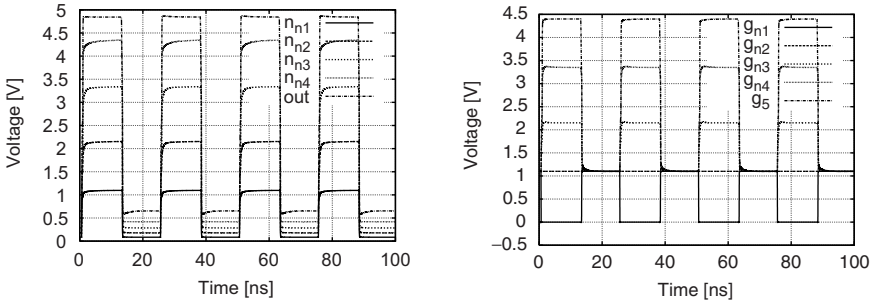
Fig. 5.28. Bias circuit implementation for the nMOS stacked transistors for an output stage with a voltage multiplication factor of n

stacked transistors. The complementary bias circuit for the pMOS stacked transistors is left out for simplicity. When the output is low, the nMOS stacked transistors are biased with a voltage V_{DD} which is passed through a chain of pMOS transistors to their gates. When the output is high, the nMOS stacked transistors are biased by external applied voltages that are passed through chains of nMOS transistors. To minimize transient voltage peaks, each gate of the nMOS stacked transistors is decoupled to the V_{DD} supply. In theory, the voltage multiplication factor n can increase infinitely until the breakdown voltage of a n-well/p-substrate junction in the used technology is reached. In a 1.2 V 130 nm CMOS technology this breakdown voltage equals 14.5 V, which thus results in a maximum voltage multiplication factor of 12.

The Bias Circuit: Analysis and Sizing

The output stage of the second test chip has a voltage multiplication factor of 5. Therefore, the naming conventions of Figure 5.27 can be taken. For the analysis of the bias circuit, only the transition of the output from high ($5\,V_{DD}$) to low (gnd) is considered. The transition from low to high can be found in an analog way. The signals arriving from the tapered buffers switch transistor M_{n1} on and transistor M_{p1} off. Node n_{n1} is discharged and transistor M_{n2} is switched on, which in turn discharges node n_{n2}. Now, transistors M_{n3} and M_{bp1} are switched on. Nodes n_{n3} and g_{n3} are thus discharged. The same reasoning accounts for the transistor pairs $M_{n4} - M_{bp2}$ and $M_{n5} - M_{bp3}$ discharging the nodes $n_{n4} - g_{n4}$ and $out - g_5$. Also, with the discharging of node g_{n4}, transistor M_{bn6} is switched off and transistor M_{bp4} is switched on. The discharging of node g_5 has three effects. First, transistor M_{bn5} is switched off. Secondly, transistor M_{p5} is switched off when node n_{p4} is discharged till V_{DD}, which in turn switch transistor M_{bn3} off. Finally, Transistor M_{bp5} is switched on. M_{bp5} discharges together with transistor M_{bp4} node g_{p4}. This switches transistors M_{bp6} on and transistor M_{bn4} off. Transistor M_{p4} is switched off when node n_{p3} is discharged till $2\,V_{DD}$. Transistor M_{bp6} discharges node g_{p3}, which switches transistor M_{p3} off when node n_{p2} is discharged till $3\,V_{DD}$. Figure 5.29 shows a transient simulation of the voltages on the terminals of the stacked transistors. The output was loaded with a resistance of $4\,\Omega$ and the input frequency was set at 40 MHz. This figure clearly shows the correct operation of the bias circuit.

Since this switching does not occur for all transistors at the exact same time, it is decided to use only 90% of the nominal supply voltage as V_{DD}. This will result in a voltage headroom for the transistors. Together with the decoupling transistors on the gates of the stacked transistors, this results in a reliable operation. Figure 5.30 shows a simulation of the drain-source to gate-source voltage transfer characteristic of the nMOS stacked transistors M_{n1} to M_{n5} of the high voltage output buffer with a $4\,\Omega$ load at a



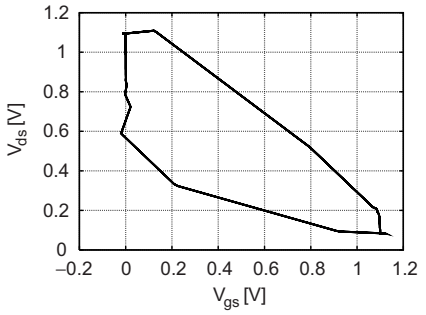
(a) Drain voltages of M_{n1} to M_{n5} (b) Gate voltages of M_{n1} to M_{n5}

Fig. 5.29. Transient simulation of the voltages on the terminals of the nMOS stacked transistors

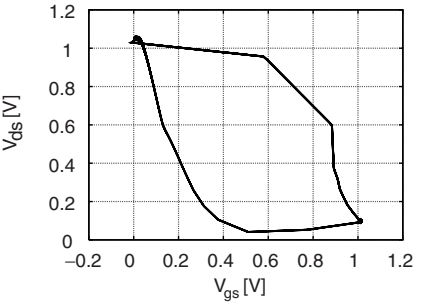
frequency of 40 MHz. The nominal supply voltage of 1.2 V is only crossed by the drain-source voltage of transistor M_{n3}. Since this peak is lower than $V_{DD} + 10\%$, the risk of hot carrier degradation and breakdown mechanisms in the stacked transistors is minimized. The same results are also obtained for the pMOS stacked transistors and the transistors of the gate bias circuit.

Due to the large number of stacked transistors, a mathematical description to determine the dimensions of the devices in the bias circuit becomes too complex and would provide no insight in the bias circuit as was the case for the first test chip in Section 5.1.2. Therefore, an intuitive description is given that explains the dimensions of the devices in the bias circuit. The transistors in this circuit only have to pass a fixed voltage to a high impedance node, the gate of a stacked transistor, in the steady state operation regime. Therefore, the on-resistance of these transistors does not need to be very low. Moreover, the dimensions of the bias transistors have to be limited, since their input capacitance add up to the already large well-capacitances on the internal nodes of the stacked transistors, $n_{np1..5}$. Furthermore, the transistor sizes are chosen such that the resistance of two paths, which pass the bias voltages to two corresponding nMOS and pMOS stacked transistors, for example M_{n4} and M_{p4}, are the same. This leads to the transistor sizes, summarized in Table 5.11.

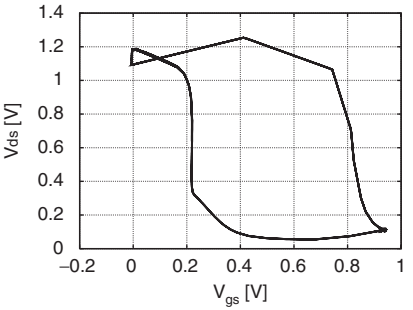
The capacitors provide a decoupling effect on the gates of the stacked transistors. After all, as stated before, during a low-to-high transition of the output, transient voltage peaks could occur on the gates of the stacked transistors due to their large gate-drain capacitance. Table 5.12 lists the capacitor's values. Actually, the decoupling exists in a capacitor in parallel with a resistor: the bias transistors in the linear region. To provide a matched decoupling effect, the RC-product must be the same within the bias circuit for the nMOS and pMOS stacked transistors. The difference in resistance of the different



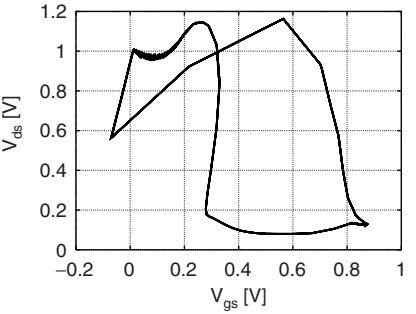
(a) Transistor M_{n1}



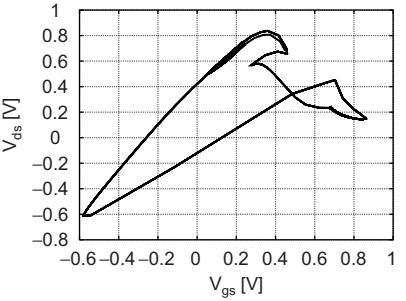
(b) Transistor M_{n2}



(c) Transistor M_{n3}



(d) Transistor M_{n4}



(e) Transistor M_{n5}

Fig. 5.30. Simulation of the drain-source to gate-source voltage transfer characteristic of the stacked nMOS transistors

paths to the gates explains then the difference in capacitance between C_{mn3}, C_{mn4} and C_{mn5} or between C_{mp3}, C_{mp4} and C_{mp5}. The difference in capacitance between two complementary capacitors, for example C_{mn4} and C_{mp4} is due to the difference in gate-drain capacitance between an nMOS and pMOS stacked transistor.

Table 5.11. Transistor sizing of the bias circuit

	M_{bp123}	M_{bp456}	M_{bn123}	M_{bn456}
W	140 µm	43 µm	35 µm	10 µm
L	130 nm	130 nm	130 nm	130 nm

Table 5.12. Capacitor values of the bias circuit

C_{mp3}	C_{mn3}	C_{mp4}	C_{mn4}	C_{mp5}	C_{mn5}
21 pF	5.4 pF	8.0 pF	2.2 pF	4.5 pF	0.3 pF

For the calculation of the power dissipation, the contribution of the well capacitors of the bias transistors can be neglected due to their small dimensions. Therefore, only the decoupling capacitors are taken into account. This results in a power dissipation of 6.4 mW at a switching frequency of 40 MHz.

The Pre-Driver Circuit

As stated before, the output level of the high voltage driver is controlled by switching the outer stacked transistors M_{n1} and M_{p1} on or off. Therefore, two control signals are necessary. The pre-driver circuit generates these two control signals. The following functions must be fulfilled by the pre-driver circuit:

- Since the input capacitance of the stacked transistors is very large, the two control signals must be buffered before driving these transistors.
- The pre-driver circuit must contain a level-shifting function. This becomes clear if one takes a look at Figure 5.31, which shows a schematic of the stacked output transistors with the necessary control signals. To switch the transistors M_{n1} and M_{p1} on or off, the following control signals are necessary: *gnd* and V_{DD} for the nMOS and $(n-1)V_{DD}$ and nV_{DD} for the pMOS if the supply voltage is defined between *gnd* and nV_{DD}. A voltage offset of $(n-1)V_{DD}$ between the two control signals is thus necessary for driving a nV_{DD} voltage circuit.
- To minimize the distortion of the output of the high voltage driver, matched delay paths are necessary from the input of the pre-driver circuit to the gates of the outer stacked transistors.
- Since the high voltage driver is used as the output stage of a SOPA line driver, its delay must be low enough for handling limit cycles up to 40 MHz. A NOS circuit should be added in the pre-driver structure if timing permits, since short circuit currents can lead to a considerable amount of power dissipation in high voltage circuits.

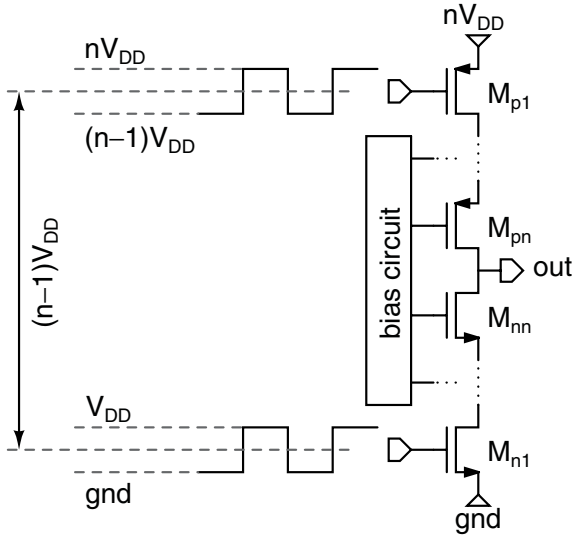


Fig. 5.31. Schematic of a high voltage buffer with its control signals

Figure 5.32 shows a schematic representation of the pre-driver circuit, which fulfills the previous stated functions. It is comprised of three main parts: a NOS circuit, two level-shift circuits and two tapered buffers. Matched delay paths are obtained by using symmetrical voltage supplies, defined between $-nV_{DD}/2$ and $nV_{DD}/2$, combined with two level-shift circuits, one with an upwards voltage offset of $2\,V_{DD}$ and one with a downwards voltage offset of $2\,V_{DD}$. The resulting total voltage offset is thus $4\,V_{DD}$, which is necessary for a $5\,V_{DD}$ voltage circuit. The pre-driver circuit converts thus two complementary square waves, defined between $-V_{DD}/2$ and $V_{DD}/2$ to two control signals, one defined between $-5\,V_{DD}/2$ and $-3\,V_{DD}/2$ for the nMOS input and one defined between $3\,V_{DD}/2$ and $5\,V_{DD}/2$ for the pMOS input. The level-shifters are placed in between the NOS and the tapered buffers. The NOS uses feedback. Therefore, two extra level-shift circuits should be necessary if the level-shifting is done before the NOS. To keep the dimensions of the level-shift circuits small, their driving capacitances should be small. Therefore, the level-shifters are placed before the tapered buffers. In the next paragraphs, each of these building blocks are discussed.

Non-Overlapping Switching Circuit

As was seen in the design of the tapered buffer of the first test chip, starting from a minimal sized inverter resulted in a large number of inverter stages and, as a consequence, a large area consumption. Moreover, since this high voltage driver will be used as the output stage of a SOPA line driver, a comparator will precede the pre-driver circuit. A start from a minimal sized inverter is

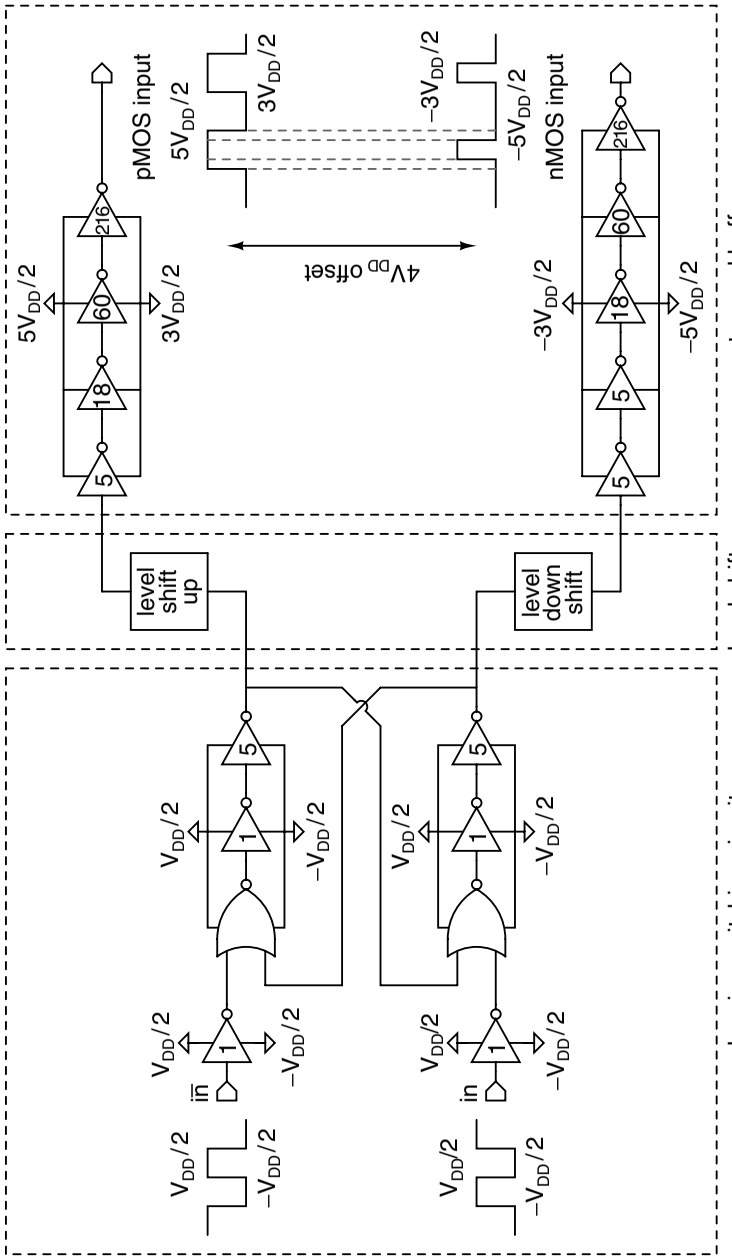


Fig. 5.32. Schematic of the pre-driver circuit

thus a start from a too small amplifier, since the sizes of the comparator will will already be larger. Therefore, the minimal inverter is resized to $W = 28.80\,\mu m$ and $L = 130\,nm$ for the pMOS and $W = 6.75\,\mu m$ and $L = 130\,nm$ for the nMOS. The input capacitance of a unit inverter for these values is $C_{io} = 68.3fF$.

The non-overlapping switching scheme is implemented by using feedback over two nor-gates. The switching signals are shifted with the delay of the inverters in the loop. The scaling factors of the inverters are shown in Figure 5.32. The total power dissipation of the NOS circuit for a 40 MHz switching frequency is less than 0.1 mW, which is negligible.

Tapered Buffer

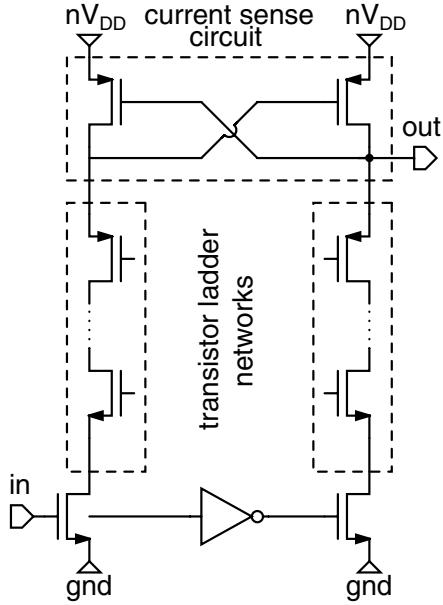
For the implementation of the tapered buffers, the same unit inverter is used as in the NOS. Again, the scaling factors chosen are larger than the scaling factors optimized for speed to reduce area and power dissipation. The scaling factors of the tapered buffers are also shown in Figure 5.32 leading to a delay of 170 ps. This buffer delay is more than low enough for a limit cycle frequency of 40 MHz, which justifies the use of a NOS. Using equation (5.6) the power dissipation of the two tapered buffers together equals 2.37 mW.

Level-Shifter

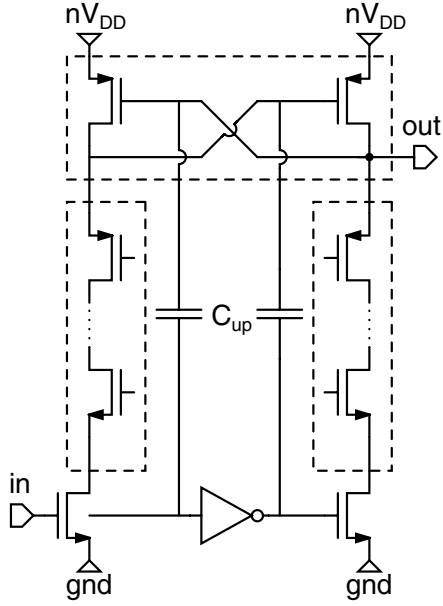
Thanks to the implementation strategy of using two level-shift circuits instead of one, the voltage offset per level-shifter is reduced to $2\,V_{DD}$, whereas an implementation with one level-shifter requires an offset of $4\,V_{DD}$ for the level-shift circuit. This reduces the complexity of the level-shift circuit dramatically.

The level-shifter implementation of the first test chip cannot be used anymore. The high-ohmic resistive division results, together with the input capacitance of the following inverter chain, in a high RC-time constant and, as a consequence, in a too large delay of the pre-driver circuit. Two examples of level-shifter implementations in a standard CMOS technology are found in [Pan03] and [Kha98]. Both implementations are comprised of two main parts: a current sense circuit and two complementary switched transistor ladder networks. A block schematic of such a conventional level-shifter is shown in Figure 5.33(a). The current sense circuit enables faster switching of the output. The transistor ladder networks have to divide the high supply voltage such that the voltages across the terminals of each transistor in the circuit is limited.

In [Pan03], this ladder network is implemented with stacked inverters biased at a fixed voltage. Therefore, this topology is easy to extend to higher offset voltages, since no extra bias circuitry is necessary to bias the transistors in the ladder network. Moreover, all internal nodes in the circuit are charged or discharged with a maximum amount of $2\,V_{DD}$ for a $(n-1)V_{DD}$ offset level-shift circuit, which improves the speed. After all, the speed of a conventional level-shift circuit is limited by the time needed to charge and



(a) Conventional circuit



(b) Improved circuit

Fig. 5.33. Block schematic of the two level-shifters

discharge the internal nodes of the transistor ladder circuit. In [Kha98] the ladder network is implemented with stacked transistors, just like the stacked transistors principle in the output stage of the high voltage driver. This implementation requires an additional bias circuit for the stacked transistors, as described in Section 5.2.2, if one wants to extend the voltage offset beyond one V_{DD}. The internal nodes of the transistor ladder network can now be charged or discharged with a maximum amount of nV_{DD} for a $(n-1)V_{DD}$ offset level-shift circuit, which negatively affects the speed of the circuit.

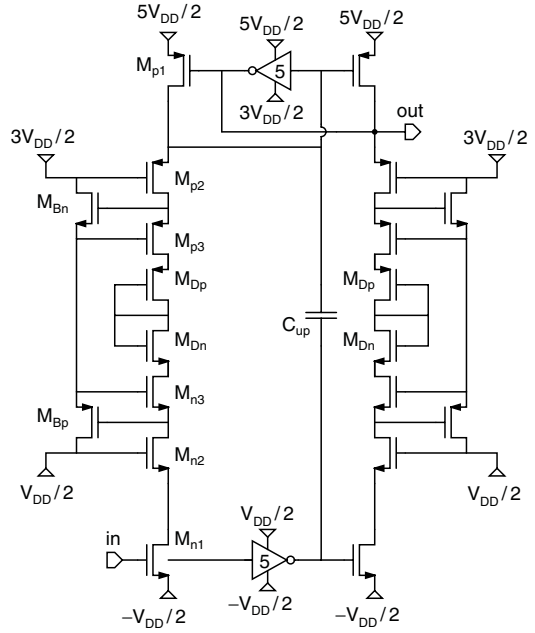
There exists two main problems in using the conventional level-shift circuit regardless the implementation of the transistor ladder network. The first one is the speed. Although the implementation with stacked inverters is faster than an implementation with stacked transistors, their speed is barely sufficient for a 10 MHz operation frequency. The second problem is the driving capability. The output can only be discharged by a pMOS transistor according to the two transistor ladder network implementations. This means that the discharging of the output is sublinear [Rab96] and that the output cannot be completely discharged due to the threshold loss of the pMOS transistor.

The speed of a level-shift circuit can be improved by increasing the switching speed of the transistors in the current sense circuit. This is done by adding coupling capacitors between the nMOS inputs and the pMOS transistors of the current sense circuit as in [Kha98]. Figure 5.33(b) shows a block schematic of the improved version of the conventional level-shift circuit. The voltage on the gates of the pMOS transistors couple up or down with ΔV:

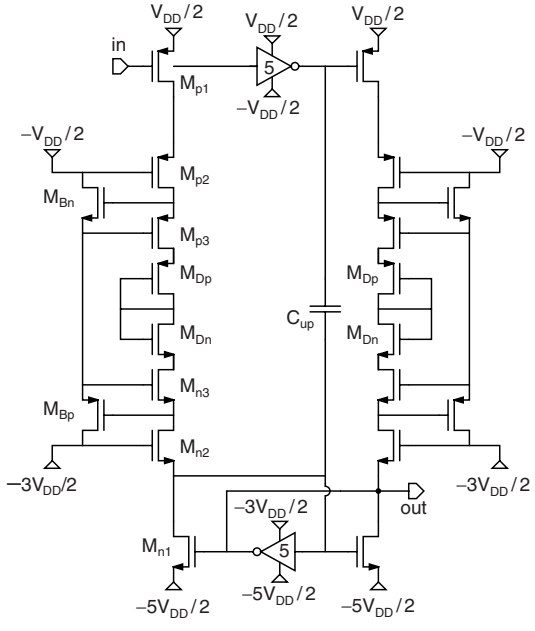
$$\Delta V = \frac{1}{1 + \frac{C_{par}}{C_{up}}} V_{DD} \tag{5.38}$$

With C_{up} the coupling capacitor and C_{par} the total parasitic capacitance on the node corresponding with C_{up}. However, the problem is now shifted to the input capacitance, which affects the rise and fall times of the level-shift circuit. Moreover, when the output load is increased, the total C_{par} on that node is increased, which results in a larger C_{up} for achieving the same ΔV and hence a larger input capacitance.

The level-shift circuit developed for the pre-driver circuit solves the problems of speed, input capacitance and driving capability of an improved level-shift implementation. The coupling capacitor at the input of the circuit is left out and its function is replaced by an inverter between the two pMOS gates of the current sense circuit, resulting in a low input capacitance. Figure 5.34(a) depicts the circuit schematic of the developed level-shifter for an upwards offset of $2\,V_{DD}$. The complementary level-shift circuit for a downwards offset of $2\,V_{DD}$ is shown in Figure 5.34(b). The supply voltages of these circuits correspond with the symmetrical supplies stated in Figure 5.32. Thanks to this extra inverter, the pMOS transistors of the current sense circuit switch nearly immediately when the input signal arrives. The speed of the level-shift circuit is thus made almost completely independent of the time needed to charge and discharge the internal nodes of the transistor ladder network. The delay of



(a) Offset $2V_{DD}$ up



(b) Offset $2V_{DD}$ down

Fig. 5.34. Circuit schematic of the level-shifter

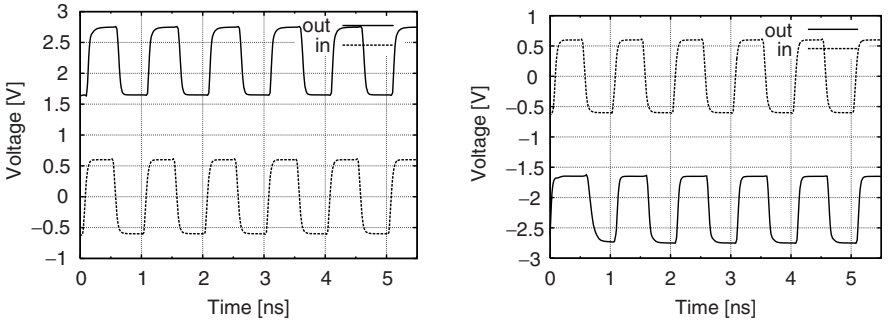
the circuit depends now on the delay through the extra inverter. Moreover, this extra inverter can now be sized for charging and discharging the output load, which solves the driving capability problem. The transistor ladder network is implemented with stacked transistors. Since the voltage offset is only $2\,V_{DD}$ and with the experience of biasing stacked transistors that was gained in Section 5.2.2, the use of stacked transistors is a logical choice. Two extra diode-configured transistors M_D are added per transistor ladder network to set off voltage transients that could occur during switching. Table 5.13 shows the transistor sizes of the level-shift circuit. The dimensions of the transistors in the ladder network are chosen small, since only a capacitive load has to be driven and hence, the on-resistance of the network is of no importance. Thanks to these small dimensions, the power dissipation due to charging and discharging of input- and well-capacitances of the transistors in the ladder networks is negligible compared to the power dissipation of the tapered buffers. The coupling capacitance C_{up} is 4 pF to provide sufficient coupling between the nMOS and pMOS gates.

Figure 5.35 shows a transient simulation of the level-shift circuit. A 1 GHz square wave, with $-V_{DD}/2$ and $V_{DD}/2$ as low and high levels, is applied at the input. The output is loaded with a capacitance of 342 fF, which corresponds to the input capacitance of the inverter following the level-shifter in the pre-driver circuit.

Table 5.14 gives the delays and the rise and fall times of the two level-shifters used in the pre-driver circuit. The time from a half V_{DD} point of the input to a $V_{DD}/2 + V_{off}$ point of the output is defined as a delay, T_{dlh}, in the charging case. In the discharging case, the delay T_{dhl} is defined in the same

Table 5.13. Transistor sizes of the level-shift circuit

	M_{n123}, M_{Dn}	M_{p123}, M_{Dp}	M_{Bn}	M_{Bp}
W	10 µm	42 µm	8.0 µm	32 µm
L	130 nm	130 nm	130 nm	130 nm



(a) Offset $2V_{DD}$ up (b) Offset $2V_{DD}$ down

Fig. 5.35. Transient simulation of the output of the level-shift circuit

Table 5.14. Delays of the level-shift circuit

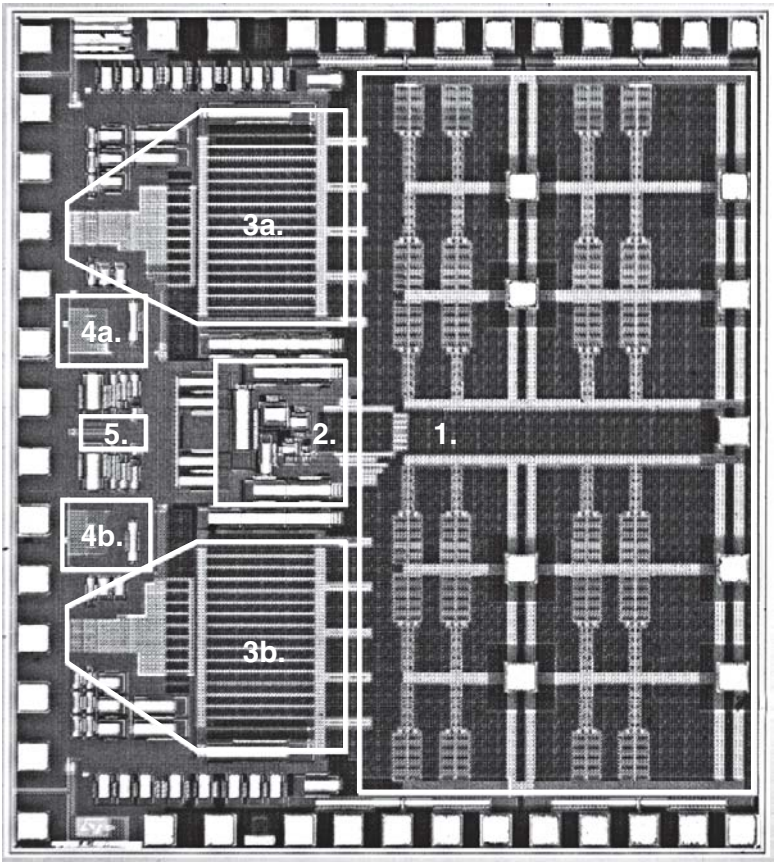
	T_{dlh} [ps]	T_{dhl} [ps]	τ_r [ps]	τ_f [ps]
Offset 2 V_{DD} up	60	47	70	60
Offset 2 V_{DD} down	47	57	57	60

way. V_{off} stands for the offset voltage of $\pm 2\,V_{DD}$ depending on level-shifting upwards or downwards. The rise and fall times, τ_r and τ_f are defined to be the time between the 10% $V_{DD} + V_{off}$ and 90% $V_{DD} + V_{off}$ points of the output. The results are quite similar for both level-shift circuits, which improves the delay-matching of the two control signals.

5.2.3 Layout Aspects

The chip photograph of the second high voltage driver is depicted in Figure 5.36. All described building blocks are clearly visible. The chip area is 1.924 x 2.146 mm^2. The technology used was a mainstream 1.2 V 130 nm triple well 1P6M CMOS technology. The layout aspects are similar to the ones of the first test chip and were described in Section 5.1.3. However, some extra remarks can be made:

- Due to the large dimensions of the stacked transistors, the output stage is now divided in 24 parallel output stages. One such output stage is laid out in a subcell in a way that all conductors have a sufficient width to cope with 1/24 of the total current. The complete output stage is then constructed by mirror and copy operations of the subcell to form an array of four by six subcells.
- The order of the stacked transistors within a subcell is kept the same as in the layout of the first test chip. This is, however, not necessary since the design is made in a triple-well technology. The bulk of the nMOS transistors is thus shielded from the substrate by an extra well, which cancels the resistive losses through the substrate. The reason for preserving this order is the complexity of the routing between the parallel connected stacked transistors. With the experience gained in the layout of the first test chip, the layout of the second test chip is speeded up when this routing strategy could be copied.
- The pre-driver circuit is laid out as symmetrical as possible to minimize the delay between the two control signals that drive the outer stacked transistors. The bias circuit is placed central, in between the two tapered buffers, such that matched delay paths are provided to the gates of the stacked transistors.
- As the gate length scales down with modern nanometer technologies, ESD protection for the circuit becomes more and more important. However, ESD protection is not straightforward in high voltage design. For the input pins, a commonly used protection circuit is used comprised of two



Legend:
1: Stacked Transistors, 2: Bias Circuit, 3ab: Tapered Buffers,
4ab: Level Shifters, 5: NOS

Fig. 5.36. Chip photograph of the high voltage driver in a 1.2 V 130 nm CMOS technology

reverse biased diodes placed between a one V_{DD} supply. An example is depicted in Figure 5.37. For the output of the high voltage driver, no ESD protection circuit is necessary, since the large drain capacitances of the stacked transistors set off possible ESD events. Between the different supply voltages power supply clamps are placed, which provide an explicit discharge path between the power rails as shown in Figure 5.37. Each power supply clamp is comprised of five series connected forward biased diodes.

After the layout step, one can extract the well-capacitances of the stacked transistors. The area of the junction between the n-well of a pMOS stacked transistors and the p-substrate measures $3.33 \cdot 10^{-8}$ m^2. Accordingly, the area

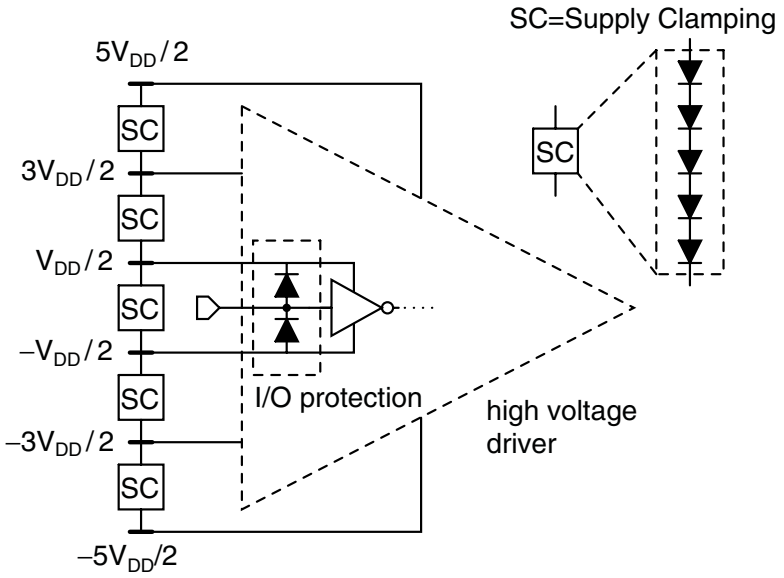


Fig. 5.37. Schematic of the high voltage driver indicating the I/O protection and the supply clamps between the different supply voltages

between the p-well of an nMOS stacked transistor and the n-doped triple well measures $1.10 \cdot 10^{-8}$ m^2. This results in a well-capacitance of 3.4 pF for the pMOS and 7.7 pF for the nMOS transistor. The high value for the nMOS transistor is due to the high doping levels of the triple well resulting in a high junction capacitance. This leads to α-factors of 16.9 and 24.8 for the pMOS and nMOS transistor respectively. By using equation (4.14) one can calculate a power loss of 19.2 mW at a switching frequency of 40 MHz.

5.2.4 Power Dissipation

Now the design and layout of the high voltage driver is completed, a comparison between the estimated power dissipation from Figure 5.23 and calculated power dissipation can be made. In Section 5.2.2, the total static power losses were set at 25 mW, leading to a total estimated dynamic power loss of roughly 20 mW. The calculated contributions to the total dynamic power dissipation were 19.2 mW for the well-capacitances, 8.2 mW for the input capacitances of the stacked transistors and 2.4 mW for the pre-driver circuit. This results in a total calculated dynamic power dissipation of 29.8 mW. The difference with the estimated value is due to an underestimation of the well-capacitances by using the α-factor of the first test chip. The total power dissipation is 60.2 mW leading to an efficiency of 63%. One has to bear in mind that this is the calculated efficiency of the high voltage driver when it is used as the output stage of a SOPA amplifier driving a 100 mW aDSL signal.

5.2.5 Measurements

Measurement Setup

The chip is wire bonded on a ceramic thick film substrate and then mounted in a copper beryllium box. The output path and supply lines were made as wide as possible to minimize the parasitic resistance. All supply lines (positive and negative) were directly decoupled to the ground as close as possible to the chip bondings. An example of the mounted chip can be seen in Figure 5.38.

Test signals were generated using a Hewlett Packard 8131A pulse generator. Time domain measurements were performed with with the Agilent 54622A Oscilloscope. To generate all supply voltages, three Delta Dual Supply sources were used.

Unmodulated Square Wave Input

Two complementary square waves, defined between -0.6 V and 0.6 V, with a frequency of 40 MHz and a duty cycle of 50% were applied to the high voltage driver. The result is shown in Figure 5.39. A peak-to-peak output swing of 4.2 V was measured over a 4 Ω load. This corresponds to an output power of 980 mW. The total power dissipation is 1.24 W, resulting in an efficiency of 79%. The efficiency corresponds well with the static efficiency of 80% that was presupposed in Section 5.2.2. After all, at such a high output power, the dynamic power dissipation can be neglected.

The low-to-high and high-to-low delay of the high voltage driver is 2.8 ns. This is right on the limit of the maximum allowable delay for integration in a SOPA system with a limit cycle frequency of 40 MHz.

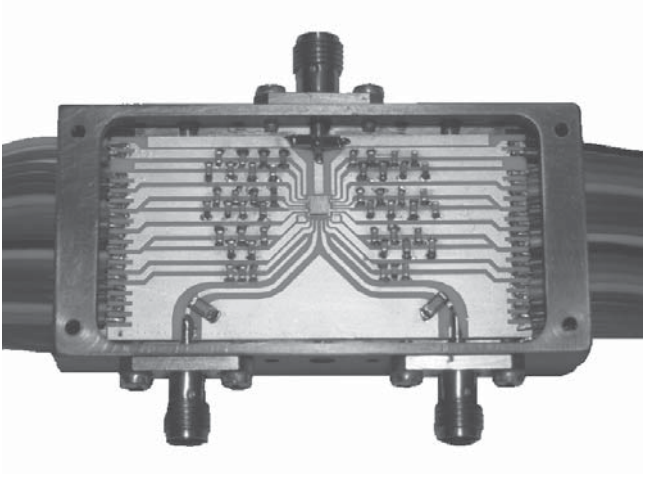


Fig. 5.38. Photograph of the chip, wire bonded on a ceramic substrate

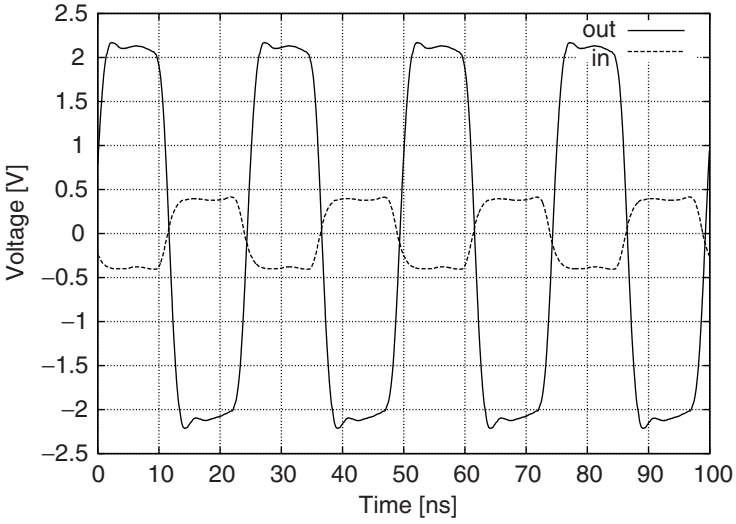


Fig. 5.39. Time domain measurement with an input square wave of 40 MHz

Table 5.15. Measured performance and process specifications

Parameter	Measured
Technology	130 nm CMOS
Nominal supply voltage	1.2 V
Supply voltage	5.5 V
Load resistance	4 Ω
Output voltage swing	4.2 V
Frequency	40 MHz
P_{diss}	1.24 W
Efficiency	79%
Delay	2.8 ns

Overview

Table 5.15 gives a summary of the measurement results. The measurement of this second test structure is restricted to a time domain measurement to prove its correct operation. As was mentioned in the beginning of this section, this high voltage driver is used as the output stage of a SOPA line driver, which is described in Chapter 6. It will be shown that the line driver meets the aDSL2+ specifications, which further validates the operation of the high voltage test structure.

5.2.6 Discussion of the Results

Comparison with the Present State of the Art

Table 5.16 summarizes the state-of-the-art published high voltage drivers in CMOS up to now. The two presented drivers have the largest voltage multiplication factor n. The second test chip even more than doubles this factor compared to the other published drivers. [Ann01] and [Sin98] operate at a higher frequency, but they only drive a low capacitive load. This explains also their small chip area. [Kil04] uses 5 V devices in a 0.35 µm CMOS technology. Moreover, the pull-down network is implemented with a gate-shifted LDDMOS, which increases the integration cost. Also, this circuit drives only a small capacitive load.

Efficiency could not be compared, since it was not mentioned for the published high voltage drivers. According to this table, the presented drivers outperform the state-of-the-art high voltage drivers.

Strong Points

The high voltage drivers excels because of the following reasons:

- The concept of stacking standard nanometer CMOS devices to design high voltage circuits works and is usable even for high-end applications like aDSL2+ (see Section 6.2).
- A novel bias circuit is developed which is easy to extend for circuits with high voltage multiplication factors. The number of passive elements is strongly reduced compared to the implementation of the first test chip, resulting in a low dynamic power dissipation. This can be seen if one compares the dynamic power dissipation of the bias circuit implementations of the two test chips at a frequency of 40 MHz. The dynamic power dissipation of the bias circuit for tree stacked transistors of the first test chip then equals 22 mW, whereas the novel bias circuit for five stacked transistors results in a dynamic power dissipation of only 6.4 mW.
- The distortion of the output waveform is minimized by providing matched delay paths from the input of the high voltage driver to the outer stacked transistors. This matching is done with circuit solutions as well as with layout solutions.
- For this second test chip, reliability is also proved, despite a $5\,V_{DD}$ supply. No performance degradation was noted after more than 24 hours, while continuously delivering full output power to the load.

Possible Improvements

Although all suggested improvements of the first test chip were applied in this second test chip, a next high voltage driver could gain by taking the following into account:

Table 5.16. Comparison with published high voltage drivers

Reference	Technology	V_{DD} high	f_s	$n = \frac{V_{DD}\text{ high}}{V_{DD}}$	Note
First test chip	2.5 V 0.25 µm CMOS	7.5 V	10 MHz	3	
Second test chip	1.2 V 130 nm CMOS	5.5 V	40 MHz	4.6	
[Ann01]	2.5 V 0.25 µm CMOS	5.5 V	50 MHz	2.2	
[Sin98]	2.1 V 0.21 µm CMOS	3.3 V	400 MHz	1.6	Complex biasing scheme Asymmetric pre-driver circuit
[Kil04]	3.3 V/5 V 0.35 µm CMOS	14 V	5 MHz	2.8	Pull-down function performed by gate shifted LDDMOS 5 V pMOS in pull-up network

- Charging and discharging the well-capacitances of the stacked transistors leads to the largest contribution of the dynamic power dissipation. Moreover, a significant part of this contribution is due to the large well-capacitance related to the nMOS stacked transistors. This high value originates from the large doping levels of the triple well. A CMOS technology with low doping levels for the triple well will thus improve the efficiency of the high voltage driver.
- The transistor ladder networks of the level-shifters were implemented with stacked transistors. In retrospect, an implementation with stacked inverters [Pan03] would be a more elegant solution for it uses less transistors and all internal nodes in the ladder network would have a maximum swing of $2\,V_{DD}$, regardless the offset voltage.
- There is no mathematical expression available to determine the dimensions of the devices in the bias circuit. Although the power dissipation of the bias circuit is very low and its correct operation is shown by simulation and measurements, the power dissipation could be further optimized by making use of Computer Aided Design (CAD) tools.

5.3 Conclusions

To prove the technique of stacking devices, for designing high voltage circuits in low voltage standard CMOS, a real implementation is mandatory. Two test chips are developed: one in a mainstream 0.25 µm technology and one in a 130 nm CMOS technology.

The first test chip, implemented in a 2.5 V 0.25 µm CMOS technology is designed to validate the concept of stacking standard CMOS devices. Although the supply voltage of the high voltage driver is set at $3\,V_{DD}$, none of the transistors in the circuit is stressed by applying too large voltages resulting in reliable operation and guaranteed minimum lifetime of operation described by the foundry. An output swing of 6.46 V at a frequency of 10 MHz is measured over a 50 Ω load. A PWM signal with a dual-tone sinusoid at 70 kHz and 250 kHz results in an IM_3 of −65 dB and an IM_2 of −67 dB.

Since the first test chip proved the feasibility of the stacking principle, the second test chip is designed to serve as the output stage of a SOPA xDSL line driver. The chip is implemented in a 1.2 V 130 nm mainstream CMOS technology. In this low voltage nanometer technology, the boundaries of the stacking principle are further explored. With five stacked transistors and a supply voltage of 5.5 V an output swing of 4.2 V at a frequency of 40 MHz is measured over a 4 Ω load with an efficiency of 79%.

The two presented prototypes have paved the way to the design of a high efficiency fully integrated high voltage SOPA xDSL line driver in a standard low voltage CMOS technology.

6

High Voltage Line Driver Realisations

THE previous chapter has proved the principle of stacking devices for designing high voltage circuits in mainstream nanometer CMOS technologies by practical implementations. Until now, only stand-alone high voltage buffers were designed, implemented and measured. To prove the usefulness of this technique, such a high voltage buffer has to be integrated in circuits for high-end applications, like xDSL. Therefore, two test chips were designed in a mainstream 130 nm CMOS technology.

The first test chip is the implementation of a high voltage zeroth-order SOPA. The test chip resulted in a materialization for the concept of integrating a high voltage output buffer, using the stacked devices principle, into the SOPA architecture in standard nanometer CMOS. It complies to the G-Lite specifications.

The second test chip aims at aDSL2+ compliance. This chip can be considered as the closing piece to prove the feasibility of stacking standard nanometer devices for designing high voltage circuits. With the high voltage output buffer, the test chip faces the two challenges of line drivers in telephone wireline communications: increasing the signal bandwidth while maintaining a high efficiency. Moreover, thanks to the implementation in a standard nanometer technology, fully integrated high voltage line drivers for xDSL applications becomes a reality.

The presented chips will prove that the stacking principle can be used for high-end applications like xDSL. Moreover, it will be shown that SOPA line drivers with a high voltage output stage can maintain their superior efficiency in nanometer CMOS technologies. The chips are compared with the present state of the art.

6.1 A Zeroth-Order SOPA in 130 nm CMOS

6.1.1 Introduction

The goal of the first test chip was to prove the feasibility of integrating a high voltage output stage using the principle of stacking devices into the SOPA

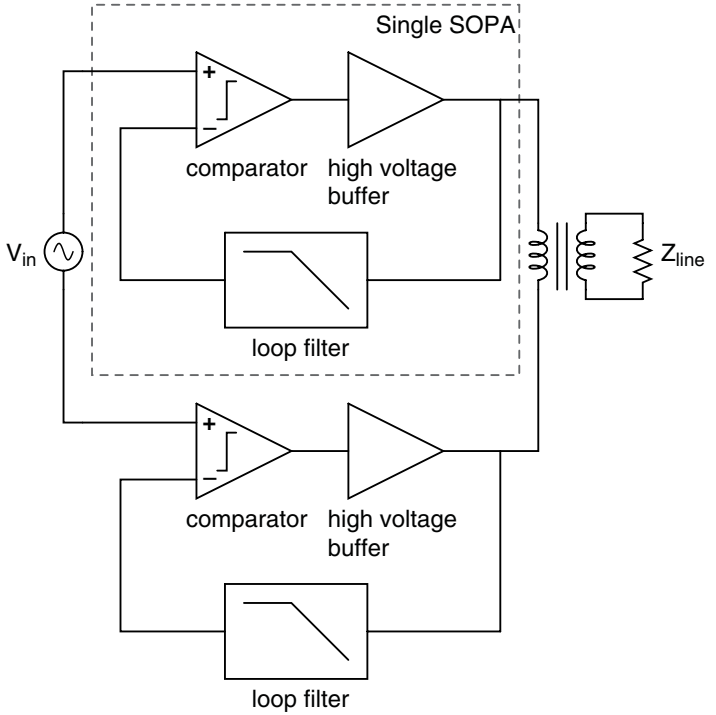


Fig. 6.1. Block schematic of the implemented zeroth-order high voltage SOPA

architecture in a standard nanometer CMOS technology. Therefore, it was not the primary goal to fully comply with one of the flavours of the xDSL family from the start on. For that, a zeroth-order SOPA architecture is chosen. The resulting prototype was implemented in a 1.2 V 130 nm 1P6M triple well CMOS technology.

The block schematic of the high voltage zeroth-order SOPA line driver is depicted in Figure 6.1. The major difference with a standard SOPA architecture is that the digital output buffer is replaced by a high voltage output buffer. The two single SOPAs are placed on the same die to provide better coupling. Every building block will be integrated except for the line transformer. The used transformer was a Midcom 50702R transformer [Mid]. The limit cycle frequency was set at 50 MHz. The OSR was set high enough to provide a linear amplifier, since it was not the goal to design at the highest possible efficiency for a certain xDSL flavour from the start on. In the next sections the building blocks of a single SOPA will be discussed.

6.1.2 Building Block Design

The High Voltage Output Buffer

The architecture and design of the high voltage output buffer was already discussed in Section 5.2. The design parameters are restated in this section. An aDSL system requires 20 dBm on a 100 Ω load. The rms voltage needed to deliver this 100 mW is 3.16 V. If the CF is set to 15 dB or a factor 5.6, the peak voltage becomes 17.7 V. Since the limit cycle amplitude should be higher than this peak voltage a factor 3 has been chosen for the maximal voltage range. The SOPA system is a bridge type line driver, so the total required voltage has to be divided by 2. The maximum voltage (V_{max}) one building block has to deal with is thus 26.55 V. Using equations (4.3) and (4.4) the transformer ratio and the equivalent load resistance can be calculated. With a nominal supply voltage of 1.2 V and a voltage multiplication factor of 5, this results in a transformer ratio rounded to 5 and a load resistance of 4 Ω.

The circuit is exactly the same as the one described in Section 5.2, the dimensions however, are different. This is due to the fact that the operation frequency of this buffer is higher for this application. The minimal total power dissipation is thus located at lower values for the widths of the stacked transistors. Moreover, due to timing constraints, the modeling and sizing of the transistors in the linear region was not optimal. This resulted in unequal sizes of the stacked transistors, since the bias circuit was not fast enough to avoid voltage transients across the nodes of the stacked transistors. A comparative assessment has been made between the dimensions of the stacked transistors and the transient voltage peaks across their terminals to determine the final widths of the stacked transistors. The dimensions of the stacked transistors are shown in Tables 6.1 and 6.2. The transistor names refer to the circuit of Figure 5.27.

Table 6.1. Dimensions of the stacked nMOS transistors

	M_{n1}	M_{n2}	M_{n3}	M_{n4}	M_{n5}
W [µm]	3,786	3,532	3,297	3,062	2,355
L [µm]	0.13	0.13	0.13	0.13	0.13

Table 6.2. Dimensions of the stacked pMOS transistors

	M_{p1}	M_{p2}	M_{p3}	M_{p4}	M_{p5}
W [µm]	16,320	15,360	14,400	13,440	12,480
L [µm]	0.13	0.13	0.13	0.13	0.13

The Comparator

As the SOPA is an asynchronous system, the comparator needs to be continuous time. Since the focus of this design is set at the integration of the high voltage buffer into the SOPA architecture, a basic comparator circuit is used. Figure 6.2 shows the circuit schematic of the comparator. The circuit consists of three stages:

1. A pre-amplifier circuit that converts an input voltage to an output current. The pre-amplifier increases the comparators sensitivity and insulates its inputs from switching noises coming from the positive feedback circuit.
2. A decision circuit incorporating positive feedback for faster comparison.
3. A nand set-reset latch which gives extra positive feedback for enabling faster comparison.

The bias current was set at 600 µA. The large bias current lowers the mismatch of the input pair M_{1ab}. This is necessary, since there are no offset cancellation techniques possible for continuous time comparators. Moreover, the large current enables faster comparison. After all, in order that the dithering effect of the limit cycle oscillation holds, the delay in the forward path of the SOPA has to be about one order of magnitude lower than τ_{lc}. As the limit cycle frequency is set at 50 MHz, the delay should be lower than 2 ns. Table 6.3 summarizes the dimensions of the pre-driver and decision circuit and Table 6.4 summarizes the dimensions of the nand set-reset latch.

The Loop Filter

Beside setting the limit cycle frequency, the loop filter has to perform another important function. The high voltage levels of the output buffer are fed back through the loop filter to the comparator operating at the nominal supply voltage. Therefore, the loop filter has to lower the signal swing at the comparator's input.

The loop filter is a simple RC-chain configuration and is of order three, which is considered as the optimal filter order as described in [Pie04]. The schematic of the loop filter is depicted in Figure 6.3. The first-order filter, comprised of R_1, R_2 and C_1, provides a voltage division with the same factor as the voltage multiplication factor, namely, 5. The second-order filter, comprised of $R_{3/4}$ and $C_{3/4}$, leads to a further lowering of the signal swing. The filter is made up by unsilicided P+ poly resistors and Metal-Insulator-Metal (MIM) capacitors. The filter's resistances and capacitances are shown in Table 6.5.

6.1.3 Layout Aspects

Figure 6.4 shows the chip photograph of the zeroth-order SOPA. Almost one half of the area is taken by the stacked output transistors to keep the on-resistance of the driver low enough. The total area is 2.6×4.3 mm^2. The

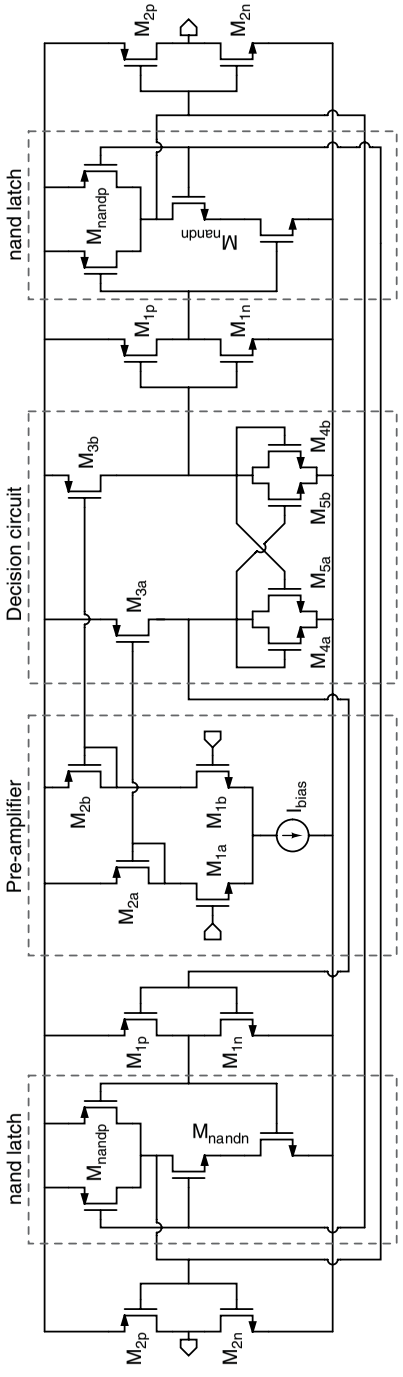


Fig. 6.2. Circuit schematic of the comparator

Table 6.3. Sizing of the pre-driver and decision circuit

	M_1	M_2	M_3	M_4	M_5
W [µm]	7.35	28.00	24.90	6.30	4.65
L [µm]	0.26	0.13	0.13	0.40	0.26

Table 6.4. Sizing of the nand set-reset latch

	M_{1n}	M_{1p}	M_{2n}	M_{2p}	M_{nandn}	M_{nandp}
W [µm]	0.30	1.00	0.63	2.80	0.90	0.52
L [µm]	0.13	0.13	0.13	0.13	0.13	0.13

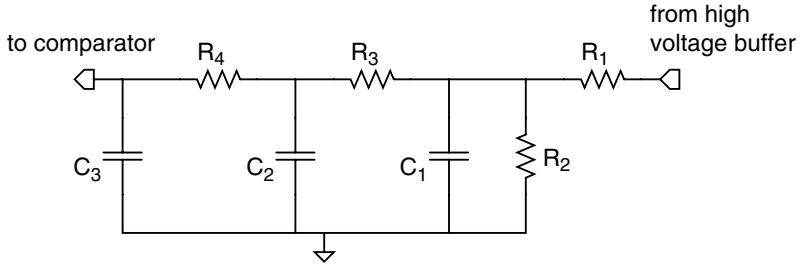


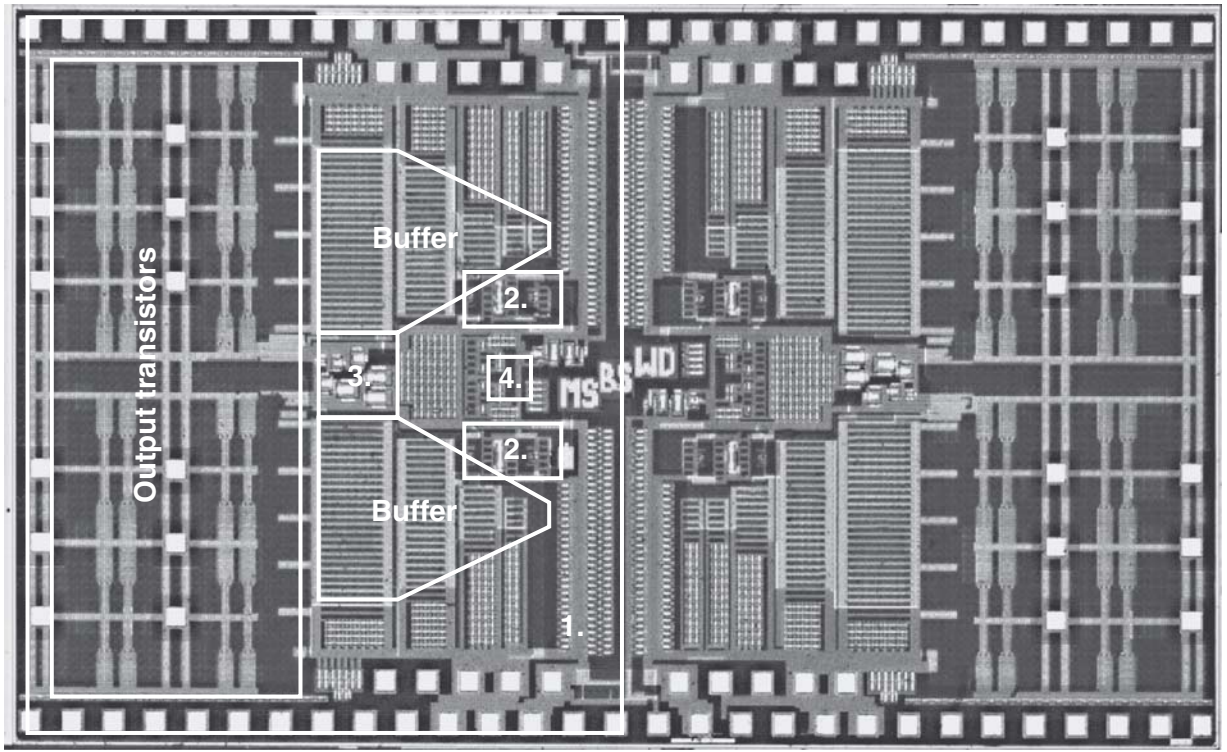
Fig. 6.3. Schematic of the loop filter

Table 6.5. Resistor and capacitor values of the loop filter

R_1	R_2	$R_{3/4}$	C_1	$C_{2/3}$
4 kΩ	1 kΩ	1 kΩ	2.5 pF	5.2 pF

majority of the layout effort is situated in the layout of the high voltage output buffer, which is already discussed in Section 5.2.3. Some additional aspects that contribute to the final SOPA layout are enumerated in the following list:

- Every building block in the SOPA architecture is separately decoupled by MIM capacitors. As the SOPA is a switching amplifier, it is important to decouple the supply voltage of the analog building blocks as much as possible.
- The chip photograph of Figure 6.4 clearly reveals that the two single SOPAs are placed directly opposed to each other. This results in separate bonding pads for the two high voltage output buffers. Since the chip was designed for classical wire bonding, the inductance of the bonding could then be reduced by placing more wires in parallel for ground and supply. Moreover, the width of the metal supply and ground conductor layers could be lowered compared to the case where the outputs are placed



1. Single SOPA 2. Level shifter
3. Bias circuit 4. Comparator

Fig. 6.4. Chip photograph of the zeroth-order SOPA

on the same side of the die. In the latter case, the supply lines must be shared between the two high voltage buffers.
- The chip is laid out as symmetrical as possible to match the delay from input to output of the two SOPA amplifiers.

6.1.4 Measurements

Measurement Setup

The same measurement setup principle as for the high voltage prototypes were used for the measurement of the line drivers. The chips were wire bonded on a ceramic thick film substrate, which was mounted in a copper beryllium box. An example is shown in Figure 6.5.

The test signals were generated using a Sony Tektronix Arbitrary Waveform Generator (AWG430). Time domain measurements were performed with the Tektronix 7845 oscilloscope. For the spectral measurements, a Hewlett Packard 3585B spectrum analyzer was used.

No Input

The response of a single-ended SOPA has been measured when no input signal was applied. The result is an output square wave with a fundamental frequency that is equal to the limit cycle frequency. Figure 6.6 shows the resulting square wave with an amplitude of 4.6 V peak-to-peak in a 7.5 Ω load resistance. The oscillation frequency of the SOPA equals 35 MHz. This value differs from

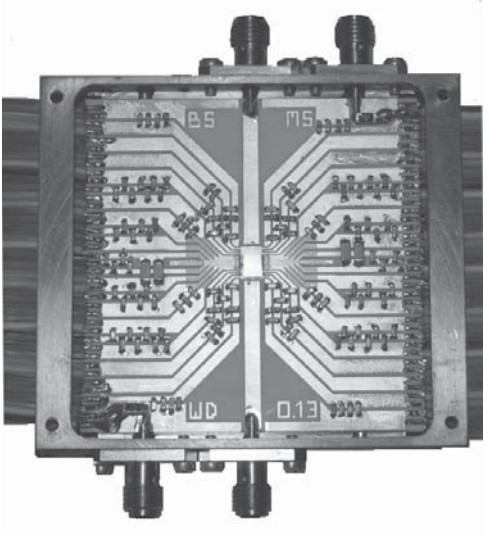


Fig. 6.5. Photograph of the chip, wire bonded on a ceramic substrate

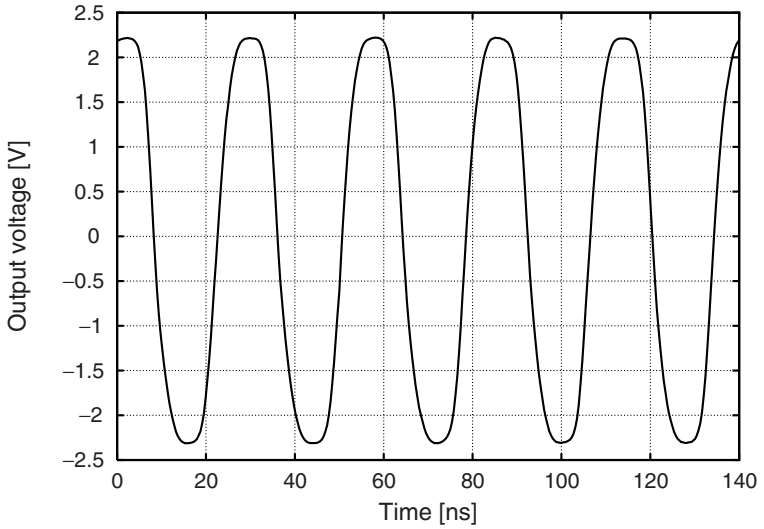


Fig. 6.6. Time domain measurement

the 50 MHz that was set by design. The difference is caused by the delay through the comparator and the high voltage buffer that turns out to be too large in practice.

Sine Wave Input

Figure 6.7 depicts the response to a sinusoidal input signal. The figure shows the output spectrum up to 10 MHz of the amplifier for a sinusoidal input signal of 1 MHz. A SFDR of 51 dB is measured without any extra filtering.

xDSL Performance

The SFDR does not characterize the capabilities for the line driver to be usable for xDSL. A better performance measure for xDSL performance is the MTPR. This figure is measured by applying a DMT modulated signal to the line driver with several tones missing. Therefore, a DMT signal consisting of 256 tones with a tone spacing of 4.3125 kHz is applied to the line driver. Tones 1–32 are left blank to form the upstream band. Tones 50, 100, 150, 200 and 226 are left out as antenna tones. Figure 6.8 shows a 20 kHz zoomed spectrum around antenna tone 226. A MTPR of 42 dB is measured for driving a DMT signal with a CF of 14 dB and an average output power of 100 mW. The total power dissipation is 249 mW, resulting in an efficiency of 40%. The equivalent load resistance is 4 Ω.

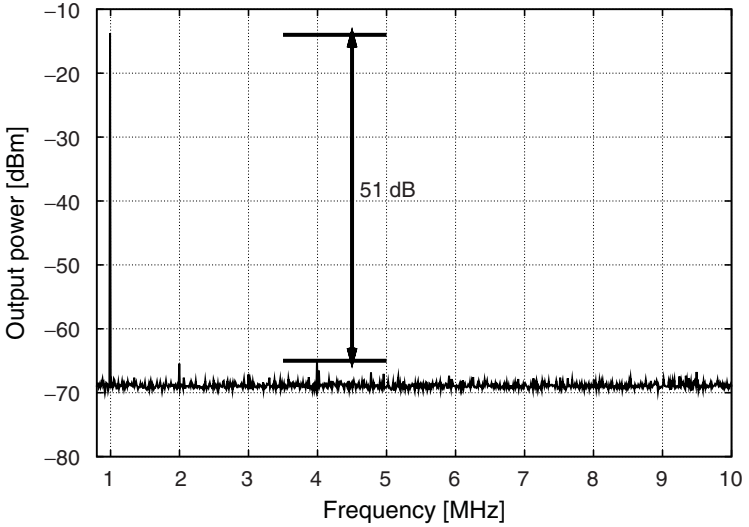


Fig. 6.7. Measured spectrum for a 1 MHz signal

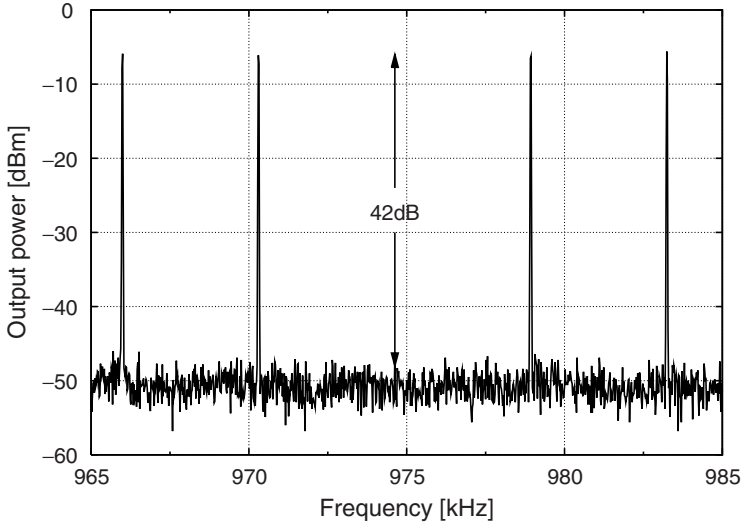


Fig. 6.8. A MTPR measurement around tone 226

Overview

Table 6.6 gives a summary of the measurement results and compares them with the aDSL G-Lite specifications. From this table, it is clear that the prototype of the zeroth-order SOPA with high voltage output buffer complies with the G-Lite standard.

Table 6.6. Measured performance and process specifications

Parameter	Measured	aDSL G-Lite
Technology	130 nm CMOS	
Nominal supply voltage	1.2 V	
Supply voltage	5.5 V	
Output voltage swing @ 7.5 Ω	4.2 V	
Bandwidth	1.1 MHz	500 kHz
Output power	20 dBm	16.3 dBm
CF	5	>5
Total power consumption	249 mW	
Efficiency	40%	
SFDR @f_{sig}=1 MHz	51 dB	
MTPR	42 dB	34 dB

6.1.5 Discussion of the Results

Strong Points

The results obtained from this test chip lead to the following conclusions:

- The feasibility of integrating a high voltage output buffer, using the stacked devices principle, into the SOPA architecture is proven. The specifications for the aDSL G-Lite standard are met.
- Due to the inclusion of the high voltage output buffer, the superior efficiency of the SOPA line driver is maintained in nanometer CMOS.
- The chips have proven to be reliable and no electro-migration effects were noted during measurements. The chips were continuously stressed for 14 days at room temperature while delivering an output power of 20 dBm. No performance degradation was seen after this time period.

Needed Improvements

After evaluation of this first prototype, several improvements can be made:

- The limit cycle frequency was about 15 MHz too low. This is probably due to the delay through the comparator and high voltage output buffer, which was too large.
- The linearity is too low to comply with the aDSL standard. This could be expected from Figure 3.11 which showed the evaluation of the upper limit of the MTPR for a zeroth-order SOPA system in a 1.2 V technology with a high voltage buffer with a voltage multiplication factor of 5. Therefore, a higher order SOPA is necessary to reach more demanding xDSL specifications.
- Due to timing constraints the sizing of the stacked output transistors was far from ideal. Better modeling of the transistors in the linear region should reduce the distortion of the output square waveform of the output buffer.

- The area of the prototype is quite large due to an over-dimensioning of the widths of the metal layers for conducting the large currents and the widths of the wells isolating the stacked transistors.

6.2 A First-Order SOPA in 130 nm CMOS

6.2.1 Introduction

As the first high voltage SOPA test chip was a hard proof for the feasibility concept of integrating a high voltage output buffer into the SOPA architecture, the goal of the second test chip was to fully comply with one of the more demanding xDSL specifications. After all, the primary goal of this research project was the design of a high voltage line driver in nanometer CMOS for aDSL/aDSL2+. For that, the linearity of the zeroth-order design has to be improved. By adding one or more integrators in the forward path of the SOPA architecture, thus introducing noise shaping, the MTPR can be improved, which was discussed in Section 3.2.5.

The order of the SOPA is a trade-off between the extra power consumption of an extra integrator and the dynamic power consumption of a higher switching frequency. Since Figure 3.11 revealed that a zeroth-order SOPA architecture in a 1.2 V CMOS technology with a high voltage output buffer barely meets the MTPR specification for aDSL, the choice is made to use only one integrator and to design for a limit cycle frequency of 40 MHz. The complete architecture is depicted in Figure 6.9.

The third-order loop filter is split-up in a first-order loop filter and a second-order filter in the forward path between the integrator and the comparator. As such, kickback noise from the switching decision-making circuitry of the comparator is filtered out by the decoupling of the integrators output and the comparators input.

Since the design target is the aDSL2+ standard, the bandwidth of the Midcom transformer is not sufficient. Therefore, the Pulse BX2639L [Pul] is chosen for this design.

6.2.2 Building Block Design

The High Voltage Output Buffer

The high voltage output buffer is exactly the same as the one described in Section 5.2. A stand-alone version of the buffer could be placed on the same die so that it could be characterized separately. A better modeling of the transistors in the linear region has led to a complete resizing of the high voltage output buffer compared to the output buffer of the first test chip. This resulted in a better matching of the on-resistance between the nMOS and pMOS transistor, leading to a lower distortion of the output waveform. The widths of

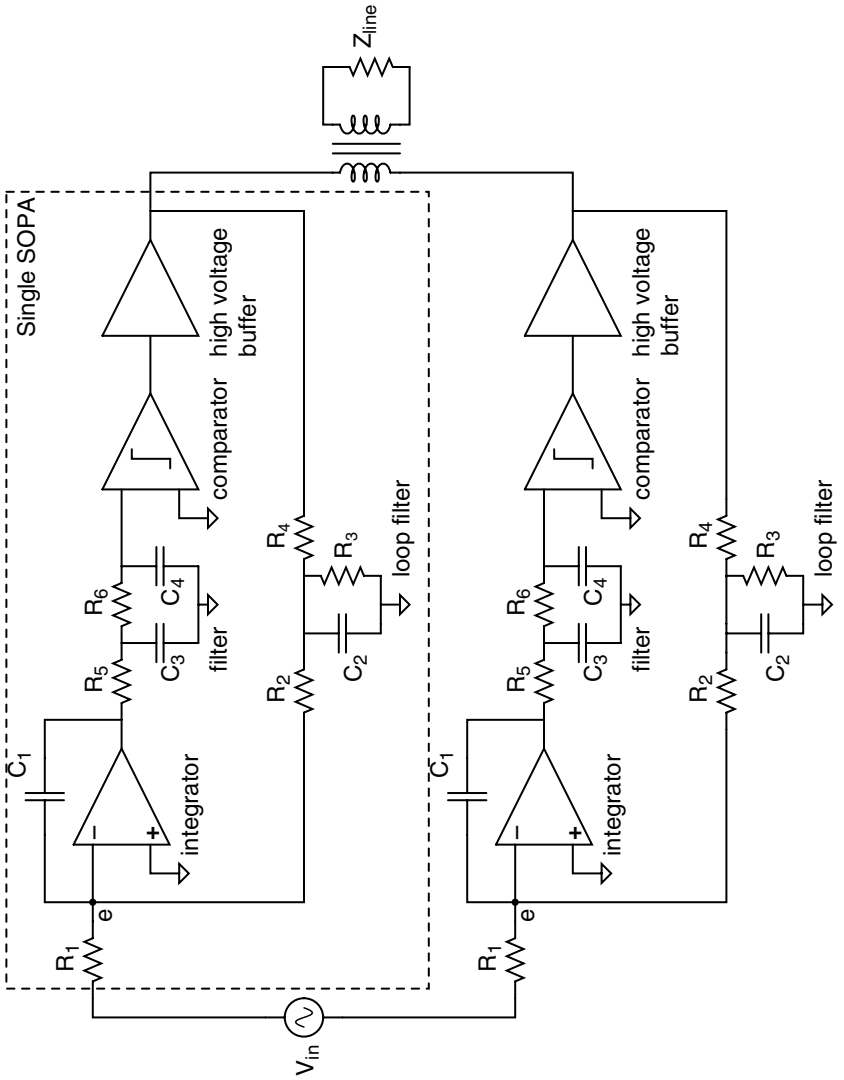


Fig. 6.9. Block schematic of the implemented first-order high voltage SOPA

the stacked transistors are also increased to lower the conduction losses of the buffer. However, this upscaling has no effect on the parasitic well-capacitances due to a more efficient splitting-up and a more compact layout of these transistors. The architecture, design and layout aspects of this buffer were discussed in Section 5.2. Important parameters of this high voltage output buffer in relation to the aDSL/aDSL2+ specifications were a supply voltage of 5.5 V leading to a transformer ratio of 5 and an equivalent load resistance of 4 Ω.

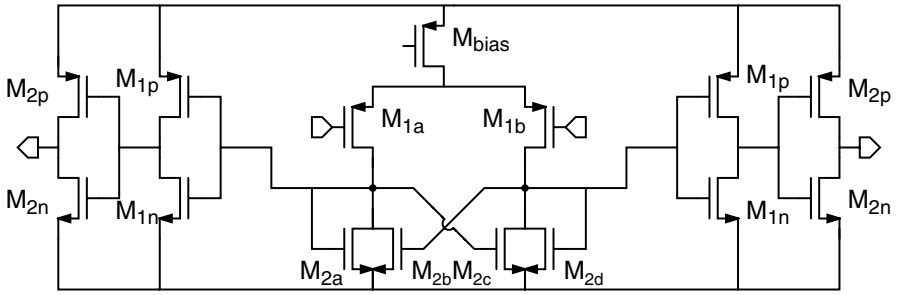


Fig. 6.10. Circuit schematic of the comparator

Table 6.7. Sizing of the comparator

	M_1	M_2	M_{bias}	M_{1p}	M_{1n}	M_{2p}	M_{2n}
W [µm]	6.24	1.17	17.05	2.32	0.60	6.96	1.80
L [µm]	0.13	0.40	0.26	0.13	0.13	0.13	0.13

The Comparator

The schematic of the comparator for the first-order architecture is shown in Figure 6.10. From the measurements of the first test chip, one can conclude that the delay of the comparator needs to be improved such that a limit cycle frequency of 40 MHz could be met. As a result, the pre-amplifier and the decision circuit are merged into each other. This is made possible by inserting the second-order loop filter in front of the comparator, which filters out possible kickback noise from the switching decision-making circuitry.

By merging the pre-amplifier and the decision-making circuitry, the bias current could be reduced to 200 µA compared to the comparator used in the zeroth-order SOPA. All dimensions are given in Table 6.7.

The nand set-reset latch is left out of the architecture as its functionality is already covered by the non-overlapping switching circuit. This circuit is located at the input of the high voltage output buffer, following the comparator and transforms its output into two differential non-overlapping square wave signals.

The Integrator

It is known from $\Delta\Sigma$ implementations that the first integrator will set the overall performance and will thus be the most demanding building block. Therefore, the choice is made to use an RC-integrator architecture over a g_m-C architecture. After all, an RC-integrator provides a high linearity for large input signals in a low voltage technology. A schematic of the integrator was shown in Figure 6.9. The current of the feedback signal, set by resistor R_2, is

subtracted from the current of the input signal, set by resistor R_1. The result of this subtraction is then integrated over capacitor C_1.

A single-ended RC-integrator is taken for that a fully differential SOPA architecture would suppress the common mode signal. As such, the self-oscillation would be damped.

The value of the resistor R_1 determines the following parameters:

- The thermal noise at the output. The noise of the integrator will be fully present at the output. Since this noise is dominated by the thermal noise (4kTR) of resistor R_1, its value can be 20 kΩ for generating 18 nv/$\sqrt{\text{Hz}}$ or −138 dBm/Hz noise at the output.
- The Gain Bandwidth (GBW). The unity gain of the integrator is given by:

$$GBW = \frac{1}{2\pi R_1 C_1} \tag{6.1}$$

  Optimal system performance has been found when the GBW is set at 2 MHz. This leads to a capacitance of 4 pF for C_1.
- The linearity of the integrator. A large value of R_1 results in a low signal swing at the input of the opamp, leading to a high linearity of the integrator.

Figure 6.11 shows a circuit schematic of the single ended opamp of the RC-integrator. The gain is increased by means of the current bleeding transistors M_{2a} and M_{2b} [Yao04]. It was found that a bias current of 400 μA together with a R_1 of 20 kΩ provides a sufficient MTPR value for the SOPA line driver. This leads to the transistor dimensions summarized in Table 6.8.

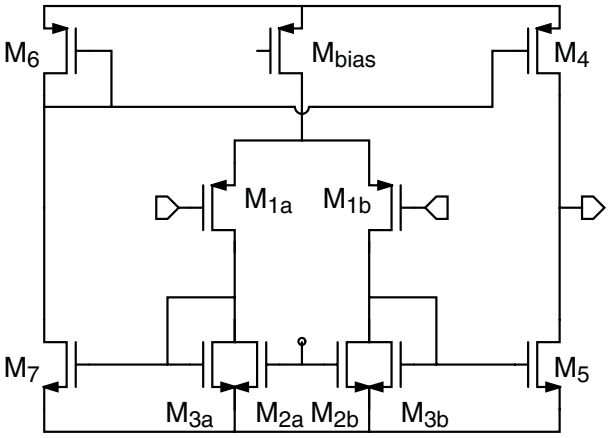


Fig. 6.11. Circuit schematic of the opamp

Table 6.8. Transistor dimensions for the integrator

	M_1	M_2	M_3	M_{bias}	M_4	M_5	M_6	M_7
W [µm]	11.46	1.42	0.49	15.98	12.05	8.03	12.47	7.81
L [µm]	0.13	0.13	0.13	0.13	0.26	0.26	0.26	0.26

The Loop Filter

A schematic of the loop filter can also be found in Figure 6.9. The filter is split-up into two parts: a second-order one in the forward path to reduce kickback noise and a first-order one in the loop to lower the signal swing at the integrator's input. The total filter order thus remains three. All filter components are made up by unsilicided P+ poly resistors and MIM capacitors.

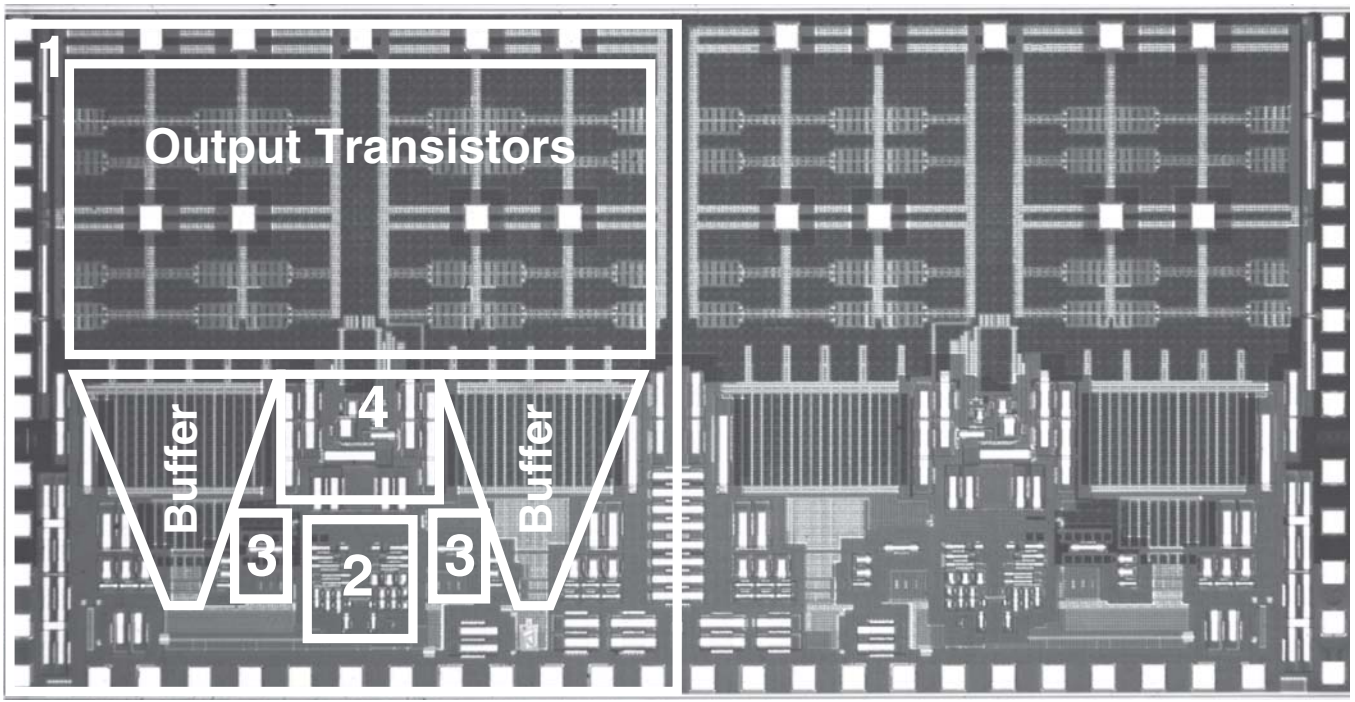
For the filter in the forward path, the structure is the same R-C stage as in the zeroth-order case. The values for R_5 and R_6 are respectively 2 kΩ and 10 kΩ. C_3 and C_4 are set at 0.4 pF.

The filter in the loop has to lower the signal swing coming from the high voltage buffer with at least the same factor as the voltage multiplication factor, namely 5. This is done in two stages. The first is a voltage division set by the resistive division R_3 and R_4. The second is a current division set by the resistors R_1 and R_2. R_2 also converts the output voltage of the loop filter to an output current, necessary for the RC-integrator. R_3 and R_4 are set at 10 kΩ and C_2 is set at 0.4 pF. Resistor R_2 equals 40 kΩ.

6.2.3 Layout Aspects

Figure 6.12 shows the chip photograph of the first-order SOPA. A first look immediately reveals that almost one half of the area is taken by the output stacked transistors, as was also the case for the zeroth-order SOPA. The total area is 2.0 x 4.1 mm^2. Again, the majority of the layout effort is situated in the layout of the high voltage output buffer, which is discussed in Section 5.2.3. However, some additional aspects need to be mentioned that contribute to the final layout:

- The outputs of the two single SOPAs are placed at the same side of the die. In this way, the supply pins are shared between the two high voltage output buffers, leading to a more compact layout. Moreover, this new orientation results in a reduction in parasitic resistance of the thick film substrate used for measurements.
- A careful study of the currents running through the circuit was performed to optimize the widths of the metal conductor layers.
- As was already the case in the layout of the zeroth-order SOPA, every building block has its own local decoupling. Every free square micrometer is filled with MIM decoupling capacitors to lower the contributions of the supply noise in the output signal.



1. Single SOPA 2. Integrator and comparator
3. Level shifter 4. Bias circuit

Fig. 6.12. Chip photograph of the first-order SOPA

6.2.4 Measurements

Measurement Setup

The measurement setup for the realized test chip is the same as the one for the previous test chips. The supply lines are extensively decoupled on the ceramic substrate as close to the chip as possible. Bias currents are set by potentiometers on a PCB. All supply lines and bias currents are sufficiently decoupled on the PCB as can be seen in Figure 6.13.

The test signals were generated using a Sony Tektronix Arbitrary Waveform Generator (AWG430). Time domain measurements were performed with the Tektronix 7845 oscilloscope. For the spectral measurements, a Hewlett Packard 3585B spectrum analyzer was used.

No Input

First the response of a single-ended SOPA is measured when no input signal is applied. The resulting output square wave is shown in Figure 6.14. The limit cycle frequency of the SOPA is 25 MHz. Again, this limit cycle frequency is about 15 MHz too low compared to the design specification of 40 MHz. A peak-to-peak voltage swing of 4.7 V is measured in a 12.5 Ω load. This load is deliberately taken higher than the load of 4 Ω, necessary for the 100 mW output power of an aDSL system. The reason is that a single-ended SOPA delivers an output power to the load equal to $\frac{V_{ptp}^2/2}{R}$, whereas two SOPAs in a bridge configuration only have to deliver the 100 mW to the load. Since the output buffer is not dimensioned for such a high output power, the choice is made to use a higher load resistance for the single-ended measurement to lower the current densities in the chip.

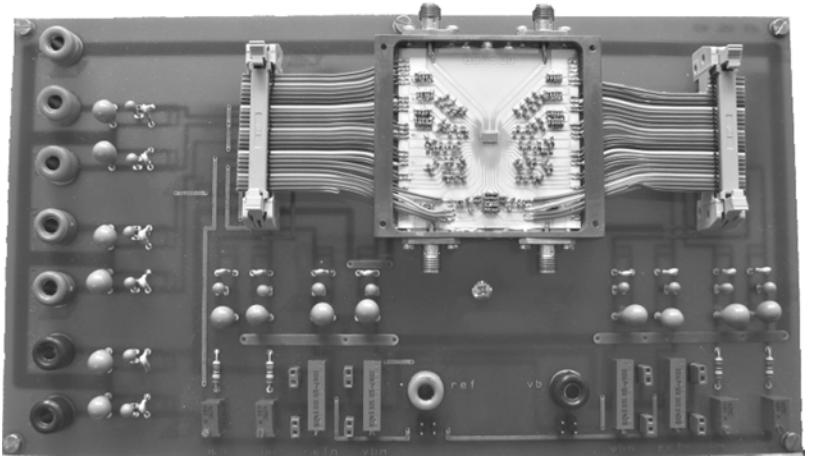


Fig. 6.13. Photograph of the PCB with the chip, wire bonded on a ceramic substrate

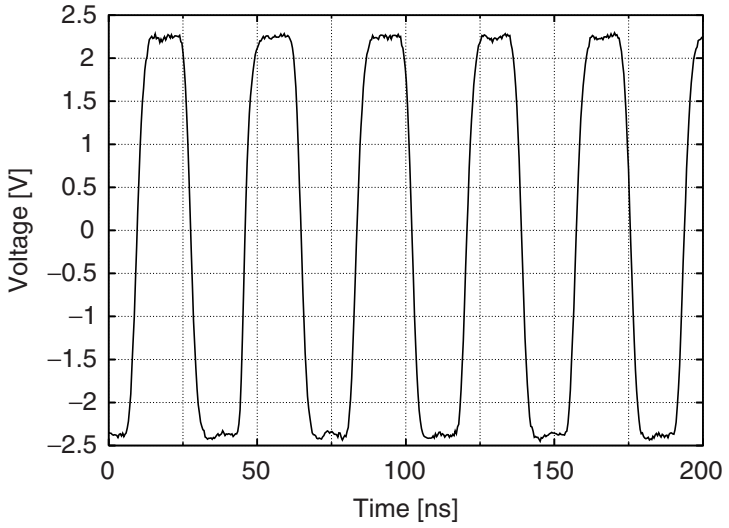


Fig. 6.14. Time domain measurement of the output square wave of the single-ended first-order SOPA

xDSL Performance

A MTPR measurement is performed to derive the aDSL2+ specifications. For these measurements, two SOPAs are connected in a bridge configuration and a DMT signal, conform the ITU-T Recommendation G.992.5 is applied to the line driver. The DMT signal consists of 512 tones with a tone spacing of 4.3125 kHz and has a CF of 15 dB. The first 64 tones are left out to form the upstream signal. An additional 5 tones, 102, 183, 286, 381 and 462 are left out as antenna tones. The output spectrum is shown in Figure 6.15.

Figure 6.16 is a zoom on the last antenna tone with the highest and most critical frequency. A MTPR of 58 dB is measured for an average output power of 100 mW. The total power consumption of the line driver is 237 mW. This gives an efficiency of 42% for driving a 100 mW aDSL2+ signal with a CF of 5.6 or 15 dB.

To compare the measured efficiency, with the calculated efficiency, Figure 4.18 has to be recalculated for a switching frequency of 25 MHz. The result is shown in Figure 6.17. The graph shows a total power loss of about 33 mW for one SOPA with a high voltage output buffer comprised of five stacked transistors. This results in a total power dissipation of 166 mW, which represents an efficiency of 60%. One has to keep in mind that this is the maximum efficiency of the line driver, delivering 100 mW to the load, with ideal building blocks, except for the stacked transistors in the high voltage output stage. The measured efficiency of the complete line driver of 42% is thus a fairly good result.

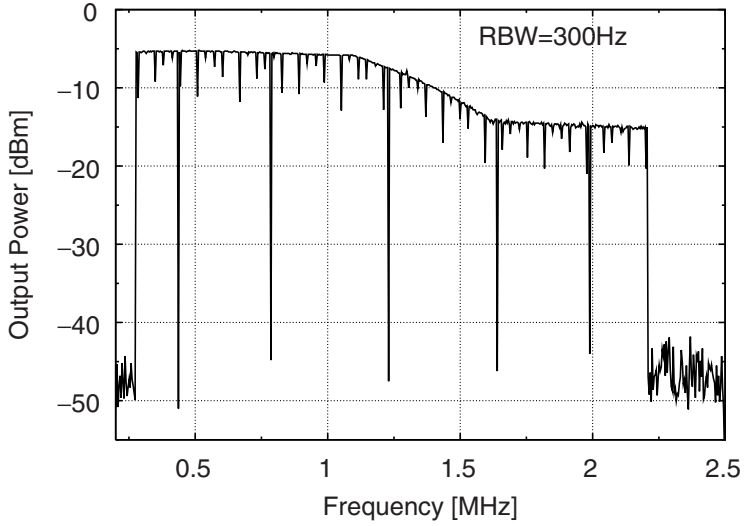


Fig. 6.15. Measured aDSL2+ output spectrum on the line conform the ITU-T Recommendation G.992.5

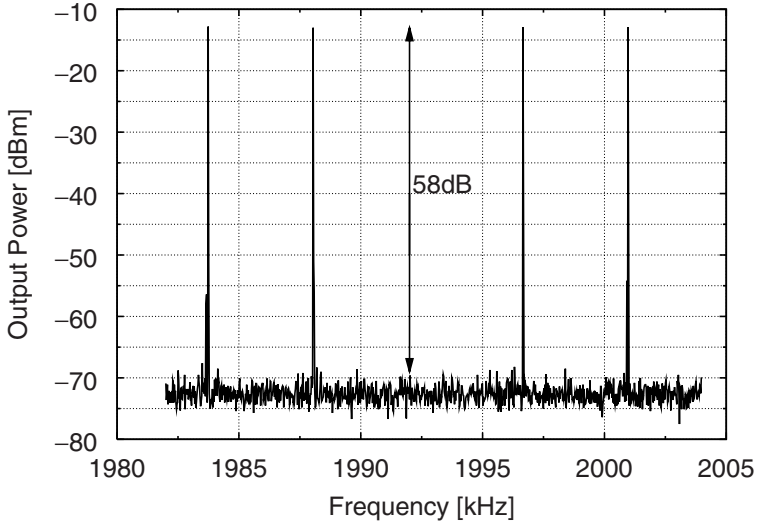


Fig. 6.16. A 58 dB MTPR line measurement around tone 462

Overview

Table 6.9 summarizes the measurement results and compares them with the aDSL2+ specifications.

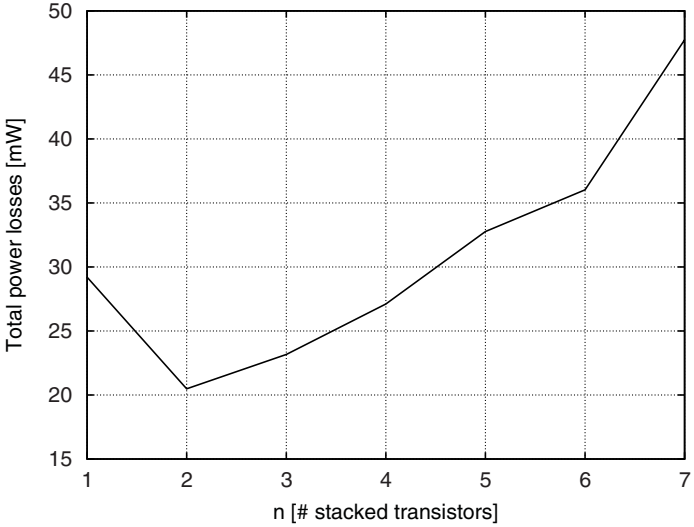


Fig. 6.17. Minimum total power loss of the SOPA output stage in function of the number of stacked transistors

Table 6.9. Performance summary

Parameter	Measured	aDSL2+
Technology	130 nm CMOS	
Nominal supply voltage	1.2 V	
Supply voltage	5.5 V	
Output voltage swing @ 12.5 Ω	4.7 V	
Bandwidth	>2.2 MHz	2.2 MHz
Output power	20 dBm	20 dBm
CF	5.6	>5
MTPR	58 dB	55 dB
Total power consumption	237 mW	
Efficiency	42%	

6.2.5 Discussion of the Results

Comparison with the Present State of the Art

Table 6.10 gives a comparison of the presented high voltage line drivers with recently published state of the art solutions. The presented line drivers advance the state of the art for the following reasons:

- The presented line driver [Ser07] is the first driver to meet the aDSL2+ standard designed in low voltage 130 nm CMOS technology. A high voltage buffer is integrated into the line driver architecture to lower the current density and to relax the transformer ratio. No extra mask-sets or process

Table 6.10. Comparison with state-of-the-art published solutions

Reference	Technology	xDSL-Spec.	BW	MTPR	P_{Total}	Eff.
This work:						
0th order [Ser05]	1.2 V 130 nm CMOS	G-Lite	1.1 MHz	42 dB	249 mW	40%
1st order [Ser07]	1.2 V 130 nm CMOS	aDSL2+	$>$2.2 MHz	58 dB	237 mW	42%
[Zoj00]	170 V BiCMOS/DMOS	G-Lite	500 kHz	63 dB	2.4 W	1.8%
[Laa01]	5 V 0.5 µm CMOS	G.SHDSL	384 kHz	THD=−82 dB	307 mW	7.2%
[Ben01]	170 V Bipolar	G-Lite			1.90 W	2.2%
		aDSL	16 MHz	64 dB	2.65 W	3.8%
[Cre01]	15 V Bipolar SOI	aDSL	1.1 MHz	68 dB	1.1 W	9%
[Pie01]	3.3 V 0.35 µm CMOS	G-Lite	800 kHz	40 dB	187 mW	23%
[Pie02a]	26 V Bipolar SOI	aDSL	1.1 MHz	71 dB	744 mW	13.4%
[Sab02]	26 V Bipolar	aDSL	1.1 MHz	75 dB	740 mW	13.5%
[Pie02b]	3.3 V 0.35 µm CMOS	aDSL		56 dB	211 mW	47%
		vDSL	8.6 MHz		141 mW	20%
[Mac03]	16 V 0.7 µm BiCMOS SOI	aDSL	1.1 MHz	69 dB	610 mW	16.4%
[Bic03]	DNW 2.5/5 V 0.25 µm CMOS	aDSL	1.1 MHz	72 dB	700 mW	14.3%
[Moy03]	2.5/5 V 0.25/0.5 µm CMOS	vDSL	12 MHz	THD=−72 dB	900 mW	3%

steps are used to create high voltage devices. This allows for a fully integrated AFE saving cost and area.
- None of the recently published line drivers meet the aDSL2+ standard.
- [Zoj00, Ben01, Cre01, Pie02a, Sab02, Mac03] use high voltage, non-CMOS technologies which increases the price of the line driver. [Bic03] is implemented in a deep N-well CMOS technology with a high voltage extension. [Moy03] uses a combined 0.25/0.5 µm CMOS technology to increase the supply voltage of the line driver. All these solutions inhibit a low cost, fully integrated xDSL AFE.
- The presented line drivers are more as twice as efficient as the published solutions up to now. Only [Pie02b] has a comparable efficiency. [Pie02b] was the first aDSL line driver based on the SOPA principle, which explains the good efficiency. However, compared to the presented aDSL2+ line driver, the bandwidth is halved and the chip was designed in an older 3.3 V 0.35 µm CMOS technology. Whereas the presented line driver has a supply voltage of 5.5 V in a 1.2 V CMOS technology, [Pie02b] had to use a larger transformer ratio, which increases the return signal attenuation.
- [Laa01] is implemented in a 5 V submicrometer CMOS technology. It only meets the G.SHDSL standard, which has an about six times lower bandwidth. The design profits also from the fact that G.SHDSL uses a CF of only 3.2 (aDSL and aDSL2+ have a CF of more than five), which explains the good distortion specifications.

Strong Points

The following enumeration summarizes an interpretation of the most remarkable measurement results:

- The concept of stacking standard CMOS devices to design a high voltage output buffer works and is usable, even for high-end applications.
- If the year of publication is regarded in Table 6.10, one can conclude that the first published SOPA line driver for aDSL, [Pie02b], was more than three years ahead of all competition. With the use of a high voltage output buffer, it is proved that this lead in efficiency is maintained in standard nanometer CMOS even for more demanding xDSL flavours.
- The presented techniques for designing a high voltage tolerant circuit can also be used for other analog designs in nanometer CMOS that require a high output voltage.
- The different orientation of the two SOPAs on the die, now with the output buffers facing the same direction, and the optimization of the metal widths lead to a more compact layout. The chip area of the second test chip is reduced with 3 mm^2 compared to the first test chip.

Possible Improvements

The following aspects could further improve the line driver design:

- A line driver design in a low voltage nanometer CMOS technology is interesting from a research point of view, to search for the limits of the technology, but it is not usable for developing a commercial product. A transformer ratio of 5 results in a too large attenuation of the receive signal. Therefore, a higher supply voltage is necessary to achieve a transformer ratio of 1 or 2. For a transformer ratio of 2, a minimum supply voltage of 12 V is necessary. With the high voltage techniques developed in this work, this can be achieved if the presented high voltage output buffer is designed in a 0.25 μm CMOS technology.
- In the two presented line driver implementations, the limit cycle frequency was determined by the delay of the comparator and the high voltage output buffer. A faster comparator should improve the bandwidth of the line driver, such that it should be possible to comply with the future vDSL2 standard with a bandwidth up to 30 MHz, leading to a fully integrated multistandard CO line driver in standard CMOS.

6.3 Conclusions

The previous chapter discussed the design and measurements of high voltage buffers in standard CMOS technologies. As stand-alone versions, the results are very promising. However, to prove the usefulness of the stacking technique, such a high voltage buffer needs to be integrated in a circuit for high-end applications. For that, the high voltage buffer, described in Section 5.2 is integrated into the SOPA architecture. The SOPA is a highly efficient line driver for xDSL applications [Pie04], but its linearity and efficiency suffers from the low supply voltages coming from nanometer technologies as described in Chapter 4. Two SOPA line drivers were implemented in a 1.2 V 130 nm standard CMOS technology with a 5.5 V output stage.

A first test chip is designed to serve as a materialization for integrating a high voltage buffer, using the stacked devices principle, into the SOPA architecture. The prototype has a bandwidth up to 1.1 MHz and a MTPR of 42 dB is measured for a DMT signal with a CF of 14 dB. An efficiency of 40% is measured for an average output power of 100 mW. The first test chip complies with the aDSL G-Lite specifications.

As the first test chip proved the concept of integrating a high voltage buffer into the SOPA architecture by compliance with the aDSL G-Lite specifications, the second test chip aimed at full aDSL/aDSL2+ compliance. The resulting line driver thus has to meet the linearity specifications of the aDSL standard, which is the most stringent in the xDSL family, at the 2.2 MHz bandwidth of the aDSL2+ standard. By inserting a continuous time RC-integrator and by optimizing the dimensions of the high voltage output

buffer, the measurements of the test chip showed aDSL/aDSL2+ compliance. A MTPR of 58 dB is reached for a DMT signal with a CF of 15 dB. The total power dissipation for an average output power of 100 mW is 237 mW. The efficiency is 42%.

The test chips thus prove that the superior efficiency of the SOPA line driver can be maintained in a low voltage nanometer mainstream CMOS technology, thanks to the principle of stacking devices to create a high voltage output buffer.

7

Conclusions

TODAY, DSL is by far the most popular "Last Mile" broadband access technology at 65.6% market share. However, with more than 700 million phone lines installed worldwide, only 5% of those lines are connected to DSL networks. Therefore, there are still large opportunities for DSL, since the majority of the world is still "unconnected". These large opportunities justify the investments for the quest to increase data-rate and reach of the DSL network.

7.1 Main Contributions and Achievements

The reuse of the billions of copper wires in the ground for last mile access is a good choice from a market point of view. Moreover, the advent of the nano-electronic era resulted in increasing integration densities of VLSI circuits and low power complex DSP-units. Smart modulation schemes, that can cope with the lossy telephone wire channel, are now easy to implement in an all-digital domain. The resulting DMT-modulation has turned the copper wires into gold by achieving bit-rates close to the Shannon limit.

However, DMT-signals are characterized by a large CF. A typical value for an aDSL system is 15 dB. This large CF poses serious problems on traditional power amplifier architectures for xDSL applications in terms of heat dissipation. The number of lines that can be driven from one line-card in the CO is, besides the number of components, also limited by the thermal dissipation. Since the line drivers take almost 80% of the total power budget, a lot of progress can be made by optimizing this building block.

In [Pie04] the Self-Oscillating Power Amplifier (SOPA) is presented as a highly efficient line driver for xDSL applications. However, in the nano-electronic era, supply voltages have dropped to nearly 1 V or below. This has the following consequences on the SOPA line driver design:

- An aDSL system requires an output power of 20 dBm to be put on a 100 Ω line. As the output power is defined as $P_{out} = V_{swing}^2/R$, the resistance has

to be lowered to achieve the same output power. Therefore, a transformer with a large transformer ratio has to be used as impedance transformation network to transform the 100 Ω line impedance to a resistor R.
- A large transformer ratio results in a huge attenuation of the received signal. Therefore, applying very stringent noise specifications on the building blocks in the receive circuit.
- A large transformer ratio also results in an up-transformation of the noise, generated in the transmit path of the modem. The linearity, or maximum achievable MTPR on the line, will thus be limited by the noise of the building blocks in the transmit circuit.
- A consequence of driving a small resistance is the high current density in the chip. Switching large currents will reduce the efficiency of the line driver. Voltage drops over small parasitic resistors, like the on-resistance of a switch, become more important as they lower the output voltage swing. Moreover, these large currents will also affect the reliability of the line driver. One has to take hot carrier and electro-migration effects into account.

These issues can be circumvented by integrating a high voltage output buffer into the SOPA architecture. One way to design a high voltage buffer is to make use of specialized high voltage technologies. However, the integration of these customized technologies comes at an extra cost. Extra mask sets and process steps are needed in a standard CMOS technology for creating high voltage devices. In a nanometer CMOS technology, the cost of the mask set increases exponentially when migrating the technology to the next node.

In this work, the choice is made for designing a high voltage output stage in a mainstream CMOS technology. It is the only solution for a fully integrated low cost xDSL modem AFE. By stacking standard CMOS transistors, higher voltages than the nominal supply voltage of the technology can be tolerated. In Chapter 4 a comparison is made between the design of a high voltage output stage in a low voltage CMOS technology and an implementation in a CMOS technology from a previous generation with a higher nominal supply voltage. It is demonstrated that a high voltage output buffer, implemented in a standard low voltage CMOS technology shows no performance degradation compared to an implementation in a technology with a higher nominal supply voltage. It is shown that an implementation with low voltage devices is even more efficient.

In Chapter 5, the theory of the stacking principle is proven with two realized high voltage output buffers. The first test chip is designed in a standard 2.5 V 0.25 μm CMOS technology. With only three stacked transistors a supply voltage of 7.5 V could be tolerated without reliability degradation. An output swing of 6.46 V at a frequency of 10 MHz is measured over a 50 Ω load. With the second test chip, designed in a 1.2 V 130 nm CMOS technolgy, the boundaries of the stacking principle are further explored. With five stacked transistors, a supply voltage of 5.5 V can be reliably tolerated. An output

Table 7.1. Performance summary of the two implemented SOPA line drivers

Parameter	0th order SOPA	1st order SOPA	xDSL specification
Technology	130 nm CMOS	130 nm CMOS	
Supply voltage	1.2 V	1.2 V	
High supply voltage	5.5 V	5.5 V	
Area	11.2 mm^2	8.2 mm^2	
Bandwidth	1.1 MHz	2.2 MHz	500 kHz (G-Lite) 1.1 MHz (aDSL) 2.2 MHz (aDSL2+)
Mean switch. freq.	35 MHz	25 MHz	
MTPR	42 dB	58 dB	34 dB (G-Lite) 55 dB (aDSL2+)
Output power	20 dBm	20 dBm	16.3 dBm(G-Lite) 20 dBm (aDSL2+)
Efficiency	40%	42%	
Crest factor	5.0	5.6	>5

swing of 4.2 V at a frequency of 40 MHz is measured over a 4 Ω load with an efficiency of 79%.

In a next step, the 5.5 V output buffer, based on the stacking principle, is integrated into the SOPA architecture. Two test chips are realized in a mainstream 1.2 V 130 nm CMOS technology. Table 7.1 summarizes the most important design parameters of the implemented line drivers, together with the related xDSL specifications. The zeroth-order SOPA complies with the aDSL G-Lite standard. The first-order implementation complies with the very demanding specifications of an aDSL2+ system. Both prototypes have power efficiencies around 40% for driving DMT-modulated aDSL-signals with a CF of 15 dB. The test chips prove that the superior efficiency of the SOPA line driver can be maintained in a low voltage mainstream nanometer CMOS technology, without any performance degradation. It is thus demonstrated that the principle of stacking devices, for designing high voltage circuits, works and is usable even for high-end applications.

The presented research can be seen as a major breakthrough in the design of xDSL line drivers in mainstream CMOS. The combination of the highly efficient SOPA line driver together with the research performed in this work towards high voltage circuits in standard CMOS leads to a high voltage, highly efficient aDSL2+ CO line driver in nanometer CMOS. The resulting prototypes proved the feasibility of fully integrated xDSL modems in low cost CMOS technologies.

References

[Alc] Alcatel, *A1000 aDSL*.

[Ang04] Costin Anghel, *High Voltage Devices for Standard MOS Technologies – Characterisation and Modelling*, Ph.D. thesis, École Polytechnique Fédérale de Lausanne, 2004.

[Ann01] Anne-Johan Annema, Govert Geelen, and Peter de Jong, "5.5 V I/O in a 2.5 V 0.25μm CMOS technology", *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528–538, 2001.

[Bal99] Hussein Ballan and Michel Declercq, *High Voltage Devices and Circuits in Standard CMOS Technologies*, Kluwer Academic Publishers, 1999.

[Ben01] Roger Benton, Russell Apfel, Bruce Webb, Jerome Wenske, Walt Schopfer, and Thiel Frank, "A high-voltage line driver (HVLDR) for combined voice and data services", in *ISSCC Digest of Technical Papers*, pp. 302–303, Feb. 2001.

[Bic03] Ara Bicakci, Chun-Sup Kim, Sang-Soo Lee, and Cormac Conroy, "A 700 mW cmos line driver for ADSL central office applications", in *ISSCC Digest of Technical Papers*, pp. 414–415, Feb. 2003.

[Bre89] K. Brenan, S. Campbell, and L. Petzold, *Numerical Solutions of Initial-Value Problems in Differential Algebraic Equations*, Elsevier Science Publishers, 1989.

[Bul90] K. Bult and G. Geelen, "A fast-settling CMOS opamp for SC circuits with 90dB DC gain", *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, Dec. 1990.

[Cas04] Herman Casier, Peter Moens, and Koen Appeltans, "Technology considerations for automotive", in *Proceedings European Solid-State Circuits Conference*, pp. 37–41. IEEE, Sept. 2004.

[Cor99] J.P. Cornil, J. Sevenhans, P. Spruyt, M. Mielants, and S. Braet, "DMT ADSL and VDSL circuits and systems", in *AACD 99 workshop on advances in analog circuit design*, pp. 1–17, Mar. 1999.

[Cre01] M. Cresi, R. Hester, K. Maclean, M. Agah, J. Quarfoot, C. Kozak, N. Gibson, and T. Hagen, "An ADSL central office analog front-end integrating actively-terminated line driver, receiver and filters", in *ISSCC Digest of Technical Papers*, pp. 304–305, Feb. 2001.

[Eat97] John W. Eaton, *GNU Octave Manual*, 1997.

[Fla96] D. Flandre, A. Viviani, J. Eggermont, B. Gentinne, and P. Jespers, "Design methodology for CMOS gain-boosted folded-cascode OTA with application to SOI technology", in *Proceedings European Solid-State Circuits Conference*, pp. 320–323. IEEE, Sept. 1996.

[Gel68] Arthur Gelb and Wallace Vander Velde, *Multiple-input Describing Functions and Nonlinear System Design*, McGraw-Hill Book Company, 1968.

[ITR05] ITRS, "International technology roadmap for semiconductors", `http://www.itrs.net/Links/2005ITRS/ExecSum2005.pdf`, 2005.

[Joh97] David A. Johns and Daniel Essig, "Integrated circuits for data transmission over twisted-pair channels", *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 398–406, Mar. 1997.

[Ker05] Ming-Dou Ker and Shih-Lun Chen, "Mixed-voltage I/O buffer with dynamic gate-bias circuit to achieve 3xVDD input tolerance by using 1xVDD devices and single VDD supply", in *ISSCC Digest of Technical Papers*, pp. 524–525. IEEE Press, Feb. 2005.

[Kha98] R. Khanna, A. Ben-Meir, L. DiGregorio, D. Draper, R. Krishna, R. Maley, A. Mehta, Oberman S., and T. Tsai, L. Williams, "A 0.25μm x86 microprocessor with a 100 MHz socket 7 interface", in *ISSCC Digest of Technical Papers*, pp. 242–243. IEEE Press, Feb. 1998.

[Kil04] dirk Killat, Oliver Salzmann, and Andreas Baumgärtner, "A 14V high speed driver in 5V only 0.35μm standard CMOS", in *Proceedings European Solid-State Circuits Conference*, pp. 151–154. IEEE, Sept. 2004.

[Laa01] P. Laaser, T. Eichler, H. Wenske, D. Herbison, and H. Eichfeld, "A 285 mW CMOS single chip analog front end for G.SHDSL", in *ISSCC Digest of Technical Papers*, pp. 298–299, Feb. 2001.

[Leb96] Yusuf Leblebici, "Design considerations for CMOS digital circuits with improved hot carrier reliability", *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 1014–1024, 1996.

[Mac03] Kenneth Maclean, Marco Corsi, Richard Hester, James Quarfoot, Peter Melsa, Robert Halbach, Carmen Kozak, and Tobin Hagan, "A 610 mW zero-overhead class G full-rate ADSL central-office line driver", in *ISSCC Digest of Technical Papers*, pp. 412–413, Feb. 2003.

[Mes93] D.J.G. Mestdagh, P.M.P. Spruyt, and B. Biran, "Effect of amplitude clipping in DMT-ADSL transceivers", *Electronics Letters*, vol. 29, no. 15, pp. 1354–1355, July 1993.

[Mid] Midcom, `http://www.midcom-inc.com/Products/Digital/pdf/50702R.pdf`, *Midcom 50702R digital transformer datasheet.*

[Moo65] Gordon E. Moore, "Cramming more components onto integrated circuits", *Electronics Magazine*, vol. 38, no. 8, 1965.

[Moo03] Elvé Moons, "looking to/for low power ADSL drivers in the DSLAM", in *Proceedings Workshop on Advances in Analog Circuit Design*, Apr. 2003.

[MOS] MOSIS, `http://www.mosis.org/Faqs/tech_cmos_rel.pdf`.

[Moy03] M. Moyal, M. Groepl, H. Werker, G. Mitteregger, and J. Schambacher, "A 700/900 mW/channel CMOS dual analog front-end IC for VDSL with integrated 11.5/14.5dBm line drivers", in *ISSCC Digest of Technical Papers*, volume 46, pp. 416–417. IEEE, Feb. 2003.

[Nau05] Bram Nauta and Anne-Johan Annema, "Analog/RF circuit design techniques for nanometerscale IC technologies", in *Proceedings European Solid-State Circuits Conference*, pp. 45–53. IEEE, Sept. 2005.

[Pan03] Dong Pan, Harry W. Li, and Bogdan M. Wilamowski, "A low voltage to high voltage level shifter circuit for mems application", in *Proceedings of the* 15*th Biennial University/Government/Industry Microelectronics Symposium*, pp. 284–287, 2003.

[Par00] Paradyne, *The DSL sourcebook*, Paradyne Corporation, 2000, `http://www.prospeed.net/DSL_Source.pdf`.

[Par03] Kaveh Parsi and Mike Wong, "24V line drivers thrive in aDSL2/aDSL2+ CO designs", *CommsDesign*, July 21, 2003, `http://www.commsdesign.com/showArticle.jhtml;jsessionid=N254I1EKJDCHMQSNDLPSKHSCJUNN2JVN?articleID=16501527`.

[Pel95] Marcel J. M. Pelgrom and E. Carel Dijkmans, "A 3/5 V compatible I/O buffer", *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823–825, 1995.

[Pet82] Corey Petersen and Allen R. Barlow, "High voltage circuits in standard CMOS processes", in *Proceedings Custom Integrated Circuits Conference*, pp. 287–291. IEEE, 1982.

[Pet03] Bruce Petipas, "Low power aDSL CO line drivers: Where do we go from here?", *CommsDesign*, July 21, 2003, `http://www.commsdesign.com/showArticle.jhtml;jsessionid=N254I1EKJDCHMQSNDLPSKHSCJUNN2JVN?articleID=16501525`.

[Pie01] Tim Piessens and Michiel Steyaert, "SOPA : A high-efficiency line driver in 0.35μm CMOS using a self-oscillating power amplifier", in *ISSCC Digest of Technical Papers*, pp. 306–307, Feb. 2001.

[Pie02a] John Pierdomenico, Scott Wurcer, and Bob Day, "A 744 mW adaptive supply full-rate ADSL CO driver", in *ISSCC Digest of Technical Papers*, pp. 320–321, Feb. 2002.

[Pie02b] Tim Piessens and Michiel Steyaert, "A central officed combined ADSL-VDSL line driver in .35 μm CMOS", in *Proceedings Custom Integrated Circuits Conference*, pp. 45–48. IEEE, May 2002.

[Pie04] Tim Piessens and Michiel Steyaert, *Design and Analysis of High Efficiency Line Drivers for xDSL*, Kluwer Academic Publishers, 2004.

[Pul] Pulse, `http://www.pulseeng.com/products/datasheets/B880.pdf`, *Pulse BX2639L digital transformer datasheet.*

[Rab96] Jan M. Rabaey, *Digital Integrated Circuits, A Design Perspective*, Prentice-Hall, Inc., 1996.

[Reu96] Peter Reussens, "DMT modulation for aDSL systems – discrete multi-tone; asymmetric digital subscriber line – digital subscriber line technologies: Exploring the promise of aDSL, SDSL and HDSL", *Mobile Phone News*, Dec 23, 1996, `http://findarticles.com/p/articles/mi_m3457/is_n50_v14/ai_19083309/pg_1`.

[Rey05] Patrick Reynaert and Michiel Steyaert, "A 1.75 GHz polar modulated CMOS RF power amplifier for GSM-EDGE", *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Aug. 2005.

[Sab02] Faramarz Sabouri and Reza Shariatdoust, "A 740 mW ADSL line driver for central office with 75 dB MTPR", in *ISSCC Digest of Technical Papers*, pp. 322–323, Feb. 2002.

[Sak86] Takayasu Sakurai, Kazutaka Nogami, Masakazu Kakumu, and Tetsuya Iizuka, "Hot carrier generation in submicrometer VLSI environment", *IEEE J. Solid-State Circuits*, vol. 21, no. 1, pp. 187–192, Feb. 1986.

[San99a] Hector Sanchez, Joshua Siegel, Carmine Nicoletta, Jose Alvarez, Jim Nissen, and Gian Gerosa, "A versatile 3.3V/2.5V/1.8V CMOS I/O driver built in a 0.2μm 3.5nm tox 1.8 V CMOS technology", in *ISSCC Digest of Technical Papers*, pp. 276–277, Feb. 1999.

[San99b] Willy Sansen, "Distortion in elementary transistor circuits", *IEEE Trans. Circuits Syst. II*, vol. 46, no. 3, pp. 315–325, Mar. 1999.

[San06] Willy M.C. Sansen, *Analog Design Essentials*, Springer, 2006.

[Ser05] Bert Serneels, Michiel Steyaert, and Wim Dehaene, "A 5.5V line driver in a standard 1.2V 0.13μm CMOS technology", in *Proceedings European Solid-State Circuits Conference*, pp. 303–306, Sept. 2005.

[Ser07] Bert Serneels, Michiel Steyaert, and Wim Dehaene, "A 237mW aDSL2+ CO line driver in a standard 1.2V 130nm CMOS technology", in *ISSCC Digest of Technical Papers*, pp. 524–525, Feb. 2007.

[Sev02] Jan Sevenhans, Wim De Wilde, Elve Moons, Peter Reusens, Laurent Bert, Lajos Kiss, Herman Casier, and George Gielen, "Driving the DSL highway: high speed, high density, low power, low cost", in *Proceedings European Solid-State Circuits Conference*, pp. 555–562, Sept. 2002.

[Sil] Siliconfareast, `http://www.siliconfareast.com/emig.htm`.

[Sin98] Gajendra Singh, "A high speed 3.3 V IO buffer with 1.9 V tolerant CMOS process", in *Proceedings European Solid-State Circuits Conference*, pp. 128–131. IEEE, Sept. 1998.

[Sin99] Gajendra P. Singh and Raoul B. Salem, "High-voltage tolerant I/O buffer with low-voltage CMOS process", *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512–1525, 1999.

[Sto06] Nino Stojković, "aDSL analog front end", *Automatica*, vol. 47, no. 1–2, pp. 59–67, 2006.

[vdZ99] Ronan A.R. van der Zee and Ed van Tuijl, "A power-efficient audio amplifier combining switching and linear techniques", *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 985–991, 1999.

[Vee84] Harry J.M. Veendrick, "Short circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits", *IEEE J. Solid-State Circuits*, vol. 19, no. 4, pp. 468–473, Aug. 1984.

[Wu03] John Z. Wu and C.R. Teeple, "Evaluation criteria for aDSL analog front end", *Analog Applications Journal*, 2003, `http://focus.ti.com/lit/an/slyt091/slyt091.pdf`.

[Yao04] Libin Yao, Michiel Steyaert, and Willy Sansen, "A 1V 140µW 88dB audio sigma-delta modulator in 90nm CMOS", *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.

[Zeg04] Van Zeghbroeck, *Principles of semiconductor devices*, University of Colorado, 2004, `http://ece-www.colorado.edu/~bart/book/book/chapter7/ch7_8.htm`.

[Zoj97] Bernhard Zojer, Rüdiger Koban, Reinhard Petchacher, and Wolfgang Sereinig, "A 150 V subscriber line interface circuit (SLIC) in a new BiCMOS/DMOS-technology", *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1475–1480, Sept. 1997.

[Zoj00] Bernhard Zojer, Rüdger Koban, and Joachim Pichler, "A broadband high-voltage SLIC for a splitter-and transformerless combined adsl-lite/pots linecard", in *ISSCC Digest of Technical Papers*, pp. 304–305, Feb. 2000.

Index