Wouter Bracke
Robert Puers
Chris van Hoof

ACSP
Analog Circuits And Signal Processing

Ultra Low Power Capacitive Sensor Interfaces

Springer

Bracke · Puers · Van Hoof
Ultra Low Power Capacitive Sensor Interfaces
ACSP

ULTRA LOW POWER CAPACITIVE SENSOR INTERFACES

ANALOG CIRCUITS AND SIGNAL PROCESSING SERIES

Consulting Editor: **Mohammed Ismail.** *Ohio State University*

Titles in Series:

ULTRA LOW POWER CAPACITIVE SENSOR INTERFACES
Bracke, Wouter, Puers, Robert, Van Hoof, Chris
ISBN: 978-1-4020-6231-5

LOW-FREQUENCY NOISE IN ADVANCED MOS DEVICES
Haartman, Martin v., Östling, Mikael
ISBN-10: 1-4020-5909-4

CMOS SINGLE CHIP FAST FREQUENCY HOPPING SYNTHESIZERS FOR WIRELESS MULTI-GIGAHERTZ APPLICATIONS
Bourdi, Taoufik, Kale, Izzet
ISBN: 978-14020-5927-8

ANALOG CIRCUIT DESIGN TECHNIQUES AT 0.5V
Chatterjee, S., Kinget, P., Tsividis, Y., Pun, K.P.
ISBN-10: 0-387-69953-8

IQ CALIBRATION TECHNIQUES FOR CMOS RADIO TRANCEIVERS
Chen, Sao-Jie, Hsieh, Yong-Hsiang
ISBN-10: 1-4020-5082-8

FULL-CHIP NANOMETER ROUTING TECHNIQUES
Ho, Tsung-Yi, Chang, Yao-Wen, Chen, Sao-Jie
ISBN: 978-1-4020-6194-3

THE GM/ID DESIGN METHODOLOGY FOR CMOS ANALOG LOW POWER INTEGRATED CIRCUITS
Jespers, Paul G.A.
ISBN-10: 0-387-47100-6

PRECISION TEMPERATURE SENSORS IN CMOS TECHNOLOGY
Pertijs, Michiel A.P., Huijsing, Johan H.
ISBN-10: 1-4020-5257-X

CMOS CURRENT-MODE CIRCUITS FOR DATA COMMUNICATIONS
Yuan, Fei
ISBN: 0-387-29758-8

RF POWER AMPLIFIERS FOR MOBILE COMMUNICATIONS
Reynaert, Patrick, Steyaert, Michiel
ISBN: 1-4020-5116-6

ADVANCED DESIGN TECHNIQUES FOR RF POWER AMPLIFIERS
Rudiakova, A.N., Krizhanovski, V.
ISBN 1-4020-4638-3

CMOS CASCADE SIGMA-DELTA MODULATORS FOR SENSORS AND TELECOM
del Río, R., Medeiro, F., Pérez-Verdú, B., de la Rosa, J.M., Rodríguez-Vázquez, A.
ISBN 1-4020-4775-4

SIGMA DELTA A/D CONVERSION FOR SIGNAL CONDITIONING
Philips, K., van Roermund, A.H.M.
Vol. 874, ISBN 1-4020-4679-0

CALIBRATION TECHNIQUES IN NYQUIST AD CONVERTERS
van der Ploeg, H., Nauta, B.
Vol. 873, ISBN 1-4020-4634-0

ADAPTIVE TECHNIQUES FOR MIXED SIGNAL SYSTEM ON CHIP
Fayed, A., Ismail, M.
Vol. 872, ISBN 0-387-32154-3

WIDE-BANDWIDTH HIGH-DYNAMIC RANGE D/A CONVERTERS
Doris, Konstantinos, van Roermund, Arthur, Leenaerts, Domine
Vol. 871 ISBN: 0-387-30415-0

Ultra Low Power Capacitive Sensor Interfaces

by

WOUTER BRACKE
Catholic University of Leuven, Belgium

ROBERT PUERS
Catholic University of Leuven, Belgium

and

CHRIS VAN HOOF
IMEC vzw, Belgium

Springer

A C.I.P. Catalogue record for this book is available from the Library of Congress.

ISBN 978-1-4020-6231-5 (HB)
ISBN 978-1-4020-6232-2 (e-book)

Published by Springer,
P.O. Box 17, 3300 AA Dordrecht, The Netherlands.

www.springer.com

Printed on acid-free paper

Contents

Foreword

The increasing performance of smart microsystems merging sensors, signal processing and wireless communication promises to have a pervasive impact during the coming decade. These autonomous microsystems find applications in sport evaluation, health care, environmental monitoring and automotive systems. They gather data from the physical world, convert them to electrical form, compensate for interfering variables or non-linearities, and either act directly on them or transfer it to other systems. Most often, these sensor systems are developed for a specific application. This approach leads to a high recurrent design cost. A generic front-end architecture, where only the sensors and the microcontroller software are customized to the selected application, would reduce the costs significantly.

This work presents a new generic architecture for autonomous sensor nodes. The modular design methodology provides a flexible way to build a complete sensor interface out of configurable blocks. The settings of these blocks can be optimized according to the varying needs of the application. Furthermore, the system can easily be expanded with new building blocks. The modular system is illustrated in a Generic Sensor Interface Chip (GSIC) for capacitive sensors. Many configuration settings adapt the interface to a broad range of applications. The GSIC is optimized for ultra low power consumption. It achieves an ON-state current consumption of 40μA. The system maintains a smart energy management by adapting the bias currents, measurement time and duty cycle according to the needs of the application (parasitic element reduction, accuracy and speed). This results in an averaged current consumption of 16μA in a physical activity monitoring system. The activity monitoring system is implemented in a miniaturized cube. It consists of a sensor layer (GSIC and accelerometer), a microcontroller layer and a wireless layer. The bidirectional wireless link (from the sensor node to the computer) makes it possible to display the data in real time and to change the interface settings remotely. So, the smart autonomous sensor node can adapt at any moment to environmental

changes. The GSIC is also successfully tested with other accelerometers and pressure sensors. Hence, the developed GSIC is a significant step towards a generic platform for low cost autonomous sensor nodes.

Wouter Bracke
KULeuven, ESAT-MICAS/INSYS
now with ICsense NV
Leuven,
January 2007

Chapter 1

INTRODUCTION

The drive towards an intelligent environment has lead to an increased need for intelligent and independent sensors. Possible forecasts predict these autonomous sensors to work as small distributed units, that can collect data over a longer period of time [War01, Asa98, Rab02]. According to this vision, they should meet the following challenging criteria:

- highly miniaturized. So, they can be worn or implanted without any discomfort for the user.
- versatile. The sensors will be able to operate without any intervention of the user.
- maintenance free. The nodes can supply their own energy. Hence, they need to combine Ultra Low Power (ULP) electronics (sensor interfaces, microcontroller and communication front-end) with an efficient energy generation and storage.
- low cost.

The emerging opportunities of these autonomous sensors will give the first impulse to several new applications such as intelligent prosthesis, sport evaluation, observation of livestock and measurement of weather patterns. The last decade, a tremendous progress has already been made in such smart microsystems. Some impressive realizations are a wireless multisensor medical microsystem [Tan02] and a very low power pacemaker system [Won04].
The multisensor medical microsystem integrates a microsensor array, the signal processing electronics, a wireless transmitter and batteries in a miniaturized capsule of 16 mm (diameter) by 55 mm (length). The sensor array contains a dissolved oxygen sensor, a pH-sensitive Ion-Selected Field Effect Transistor

(ISFET), a standard PN-junction silicon temperature sensor and a dual electrode direct contact conductivity sensor. The complete system dissipates only 6.3 mW for a minimal life cycle of 12 h.
The implantable pacemaker system monitors the heart's rate (how fast it beats) and rhythm (the pattern in which it beats), and provides electrical stimulation when the heart does not beat or beats too slowly. The pacemaker IC contains amplifiers, filters, ADCs, battery management system, voltage multipliers, high voltage pulse generators, programmable logic and timing control. The IC has 200 k transistors, occupies 49 mm^2 and consumes 8μW. This enables a lifetime of 10 years on a lithium iodine battery.

Most of these sensor systems were tailored towards the requirements of one specific application. This design approach is inflexible and requires several iteration steps for new sensor applications. It usually results in an intolerable high design cost for low and medium quantity market products. An ULP generic multisensor interface would reduce the costs significantly, since one can use the same interface chip for several applications. Hence, the recurrent design costs are eliminated and the time to market is shorter. Furthermore, the front-end can be adapted during operation. Hence, we can adjust the system to changes in the environment (e.g. enter a low power mode, when the available supply energy is getting low). Moreover, a generic interface is capable of reading out several sensors in different time intervals. So, we can combine the information from different sensors to compensate for cross-sensitivities (e.g. compensation of the temperature dependency).

Several research groups have already developed generic sensor interface architectures [Yaz00, Mas98, VDG96]. Most of these systems were designed for industrial applications, which do not need the lowest power consumption. As a consequence, their power dissipation is still too high (in the order of mW's instead of the required tens of μW) to permit autonomous functioning over a longer period of time.

This work aims to combine the flexibility of generic sensor interfacing with ultra low power consumption. The developed modular design methodology provides a flexible way to build a complete sensor interface out of configurable blocks. The settings of these blocks can be changed according to the varying needs of the application. Furthermore, the system can easily be expanded with new building blocks. The modular system is illustrated in a Generic Sensor Interface Chip (GSIC) for capacitive sensors. The GSIC is tested with several micromachined pressure sensors and accelerometers. Moreover, the GSIC is used in a miniaturized demonstrator for physical activity monitoring.

The outline of the presented work is as follows:

- In chapter 2 an overview of the most important design aspects for autonomous sensor nodes is given. The different building blocks are discussed

and the new modular architecture for the smart sensor interface chip is developed.

- Chapter 3 describes the Generic Sensor Interface Chip for capacitive sensors. Firstly, the front-end architecture and the design of the analog blocks are discussed. Secondly, the configuration settings and noise calculations are presented. Finally, experimental results are given in state-of-the-art pressure sensor and accelerometer applications. The performance of the implemented systems is compared with other generic sensor interfaces and dedicated (U)LP capacitive sensor interfaces.

- Chapter 4 studies the effect of programmability on generic (capacitive) sensor interfaces. It also provides an algorithm, which calculates the optimal configuration settings for each application. These settings enable a maximal accuracy of the sensor data for a given power consumption of the GSIC (sample frequency and measurement time).

- Chapter 5 presents a 1 cm^3 physical activity monitoring system. This physical activity monitoring system has been implemented as a 3D stacked sensor node, which contains a sensor (accelerometer and GSIC), a microcontroller and a wireless layer. The sensor node communicates with a remote station, which is implemented on the PC (USB stick). A Labview computer interface displays the data in real time and allows to change the settings remotely.

- Finally, chapter 6 presents some general conclusions.

Chapter 2

GENERIC ARCHITECTURES FOR AUTONOMOUS SENSORS

1. Introduction

During the past two decades, several smart sensor systems have been presented. In most of the cases, these systems contain one or more sensors, a sensor interface and signal conditioning circuits, a microcontroller and/or a dedicated digital signal processing unit and a display and/or a wireless core for the communication. Most often, these sensor systems were developed for a specific purpose. In the literature, one can find systems for a hugh variety of applications, such as intelligent prosthesis monitoring systems [Cla03], tire pressure monitoring systems [Kol04], intelligent weather observation systems [Hua03], etc. Dependent on the application, one uses a different type of amplifier, filter bank, analog-to-digital convertor (ADC) and digital signal processing. In spite of these differences, there is still a common system framework between most of the applications. Hence, one could benefit from a common front-end architecture, where only the sensors and the microcontroller software are customized to the selected application. Such a generic architecture would provide a low cost, flexible and easy to use environment to create autonomous microsystems.

In this chapter we present a generic architecture, which allows to create a sensor interface out of configurable blocks. The configuration settings and the combination of the blocks can be changed according to the needs of the application. Furthermore, the modular system can be easily expanded with new building blocks to provide extra features. Such a generic system can be used as the core of a smart (e.g. human body) sensor network, which connects several sensor nodes. By its generic nature, it opens opportunities for mass production, which allows to lower the price.

2. Multisensor microsystem

In the eighties, W. Sansen has developed the first conceptual view on a generic Internal Human Conditioning System (IHCS) [San82]. When we combine these insights with more recent work [Mas98, Pue99], we can define a general smart microsystem that contains a multisensor array, a sensor interface chip, a microcontroller, a wireless link and a power management (Fig. 2.1).

2.1 Sensors

Sensors are used in several commercial markets such as automotive industry, consumer electronics and medical equipment. The function of the sensor element is to convert energy from any energy domain (magnetic, chemical, optical, mechanical or thermal) into the electrical domain [Mid89]. The obtained electrical signal can be conditioned further by the interface electronics. Ideally, the output of the sensor is proportional to its input signal and remains the same over time. Unfortunately, real sensors are subject to spread in the production, non-linearities, cross-sentivities and drift.

The variations due to the manufacturing processes cause a spread in the sensor sensitivity and offset. These effects can be dealt with by calibration after fabrication. During this calibration, reference signals are applied on the system. This provides the necessary correction parameters to adjust the sensor output signal, so that its input-output relation is well defined. This correction can be implemented in the microcontroller or in the remote station. Furthemore, the calibration parameters are also used to compensate for the non-linearities and cross-sentivities, like temperature dependency, in the sensor system. For this purpose, extra temperature measurements are performed, resulting in a multisensor microsystem. In such a system, the measured temperature value is used to correct the output.

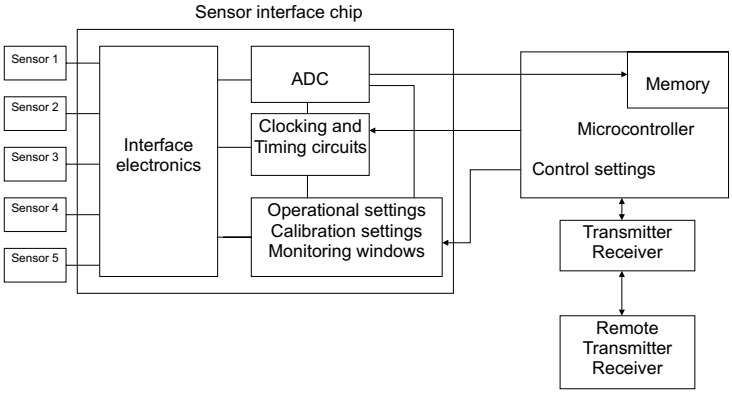

Figure 2.1. General multisensor microsystem for autonomous sensor applications.

The most difficult non-ideality to compensate is drift. Knowledge of the sensor signal in combination with appropriate signal processing algorithms, like correlation techniques, can reduce these effects significantly [Hos97].

2.2 Sensor interface chip

The sensor interface chip performs the amplification, the filtering and the analog-to-digital conversion of the sensor signals. It also contains a local configuration memory, a finite state machine, several timing and clock circuits and a microcontroller interface. This makes the sensor interface chip a versatile component, which can be programmed at any time. Hence, we can adjust the sensitivity and compensate for the offset of the sensor to ensure that the amplifiers are not saturated and the dynamic range of the sensor system is not degraded. The sensor interface chip also offers options for intelligent power management. The duty cycle operation makes the averaged power consumption adaptable to the accuracy and speed requirements of the selected sensor application. Furthermore, all the channels, which are not in use, can be switched off individually.

The low cost, Ultra Low Power (ULP) sensor interface chip will be implemented in CMOS technology. In this technology, it is important to compensate for the reduced matching (offset and drift) and 1/f noise of the transistors in the signal conditioning chain. These problems can be reduced by Correlated Double Sampling (CDS) and/or chopping [Enz96].

In the CDS technique, the offset compensation is performed in two phases. During one phase, the offset is sampled and stored and during the next phase the sampled offset is subtracted from the present one. These successive values are strongly correlated, which results in a significant offset reduction. Moreover, the CDS principle decreases the low-frequent 1/f noise.

In the chopping technique, the input signal is multiplied by a square wave signal at a frequency f_{chop}. The modulated input signal is then amplified and demodulated back to the baseband by a second chopper. The offset is, however, modulated only once and appears as frequency components around the odd harmonics of f_{chop}. These offset and 1/f noise components are removed by a low-pass filter.

In the chopping technique, the white noise of the amplifier is not aliased into the baseband, contrary to the CDS technique. This suggests that the chopper technique is more appropriate for continuous time applications, whereas the CDS technique is more suitable for sampled data applications, where aliasing is unavoidable.

The sensor interface chip should give a flexible and easy communication to different types of microcontrollers. For this purpose, a microcontroller interface is included, that is able to perform an efficient data transfer and fast

reconfiguration of the sensor front-end with a reduced complexity (limited number of IO pins, die area and power consumption).

2.3 Microcontroller

The microcontroller has several important tasks. First of all, it controls the sensor interface chip. It provides the settings of the sensor interface chip, such as the configuration of the readout electronics, the application mode and the duty cycle. Secondly, it gathers the data coming from the sensor interface chip and stores it in a memory. Furthermore, it can perform the digital linearization and cross-sensitivity compensation. For this purpose, we can use look-up tables or implement polynomial evaluation. Look-up table algorithms offer good accuracy but are very demanding on system memory. An attractive alternative is polynomial evaluation, which uses significantly less memory than look-up-table methods but is generally slower [Cra90, Yos97] . The microcontroller can also implement smart compression algorithms to extract the relevant data from the sensor signals. Hence, the amount of data, that needs to be transmitted is decreased. This reduces the power consumption significantly, since the telemetry link has a relatively large power consumption in the sensor node.

The microcontroller needs to be energy efficient to enable a large amount of signal processing with a minimum of energy. Table 2.1 lists several low power microcontrollers and their energy consumption per instruction normalized by the number of bits in the datapath (source [War03]). The table contains both general purpose microcontrollers (such as the TI MSP430 and the CoolRisc) and digital signal processing units (MIT Sensor DSP). The latter have the advantage that their architecture is more dedicated towards wireless sensor nodes. For these applications, this results in more efficient implementations.

Table 2.1. Energy consumption of various microcontrollers.

Microcontroller	*Energy (pJ/instruction/bit)*
Dallas DS80C320 High Speed 8051	1100
SICAN RISC 4b (0.25μm)	75
TI MSP430C1111 (2.2V)	45
Punch Multitask RISC core (2μm, 1.5V) [Per94]	25
CoolRisc 81 μcont. (1μm, 1.5V)	5.7
CoolRisc 81 core (0.25μm, 1.05V) [Arm00]	1.25
MIT Sensor DSP (0.6μm, 1.5V) [Ami00]	2.2

2.4 Wireless link

The wireless transceiver eliminates the need for costly wired networks. The bidirectional wireless link enhances the flexibility, since the system is adaptable during operation. This bidirectional communication sends the sensor data to a remote transceiver and provides the microsystem with new programming instructions. Hence, the accuracy, sensitivity, sample frequency, data processing, etc. can eventually be changed during operation. This is necessary to adapt the system to environment changes or to compensate for drift phenomena.

Implantable biotelemetry systems, generally use low-frequency (< 135 kHz) signals, whereas other autonomous sensor nodes often use a high-frequency (e.g. 433 MHz/916 MHz) communication front-end.

Low-frequency systems are most often based on inductive coupling [Cat04]. Such systems have a limited communication speed and a short communication range. An advantage of low-frequency radio signals is their ability to propagate through water and body tissue. This makes them very suitable for implantable devices.

High-frequency systems on the other hand offer long communication ranges and a high communication speed. Moreover, they allow for the use of smaller antennas. The main disadvantage of high-frequency radio signals is their attenuation by many (water containing) materials. High-frequent communication front-ends are implemented with narrowband [Nor, Jac03, AMI] and Ultra Wide Band (UWB) [Ryc05] solutions. Compared to narrowband implementations, sensor nodes with UWB communication have a lower power consumption for good channels, since they benefit from a simpler transmitter front-end. For average channels, narrowband solutions become better, since the transmit power dominates the front-end power consumption.

2.5 Power management

Autonomous sensor systems can be divided into active or passive powered devices.

The active devices do not require any interaction with the outside world regarding their powering. Hence, they need ULP electronics to operate autonomously over a longer period of time. These devices have a projected power budget of 100μW, which is divided into 20μW for the sensing part (sensors and readout), 40μW for the digital data processing and 40μW for the wireless transceiver. These sensor nodes can be powered by batteries or energy scavengers. Energy scavengers extract power from the environment, such as vibrations [Ste05, Des05] and body warmth [Leo05]. These power sources can vary strongly. So, specialized electronics need to convert the available power into a reliable supply voltage. Furthermore, the analog read-out electronics

should have a high power supply rejection to cope with drift in the supply voltage.

The passive devices derive their power from an external radiofrequent (RF) powering field. They only operate when this RF field is active and in the proximity. Hence, they can only be used in non-continuous monitoring applications where the external powering system is in close proximity to the monitoring device.

3. Modular design methodology

From the above derived system framework, a new generic architecture will be elaborated to create low-cost and flexible autonomous sensor nodes. Such a generic sensor system uses a plug and play approach to combine the sensors, the sensor interface, the microcontroller, the wireless communication core and the power management into a miniaturized system. In this common front-end architecture, we should only customize the sensors and the microcontroller software to the selected application.

A generic sensor interface chip is an important part of this universal platform. Such a generic sensor interface is designed as a modular system including several configurable building blocks (Fig. 2.2). These configurable blocks can be

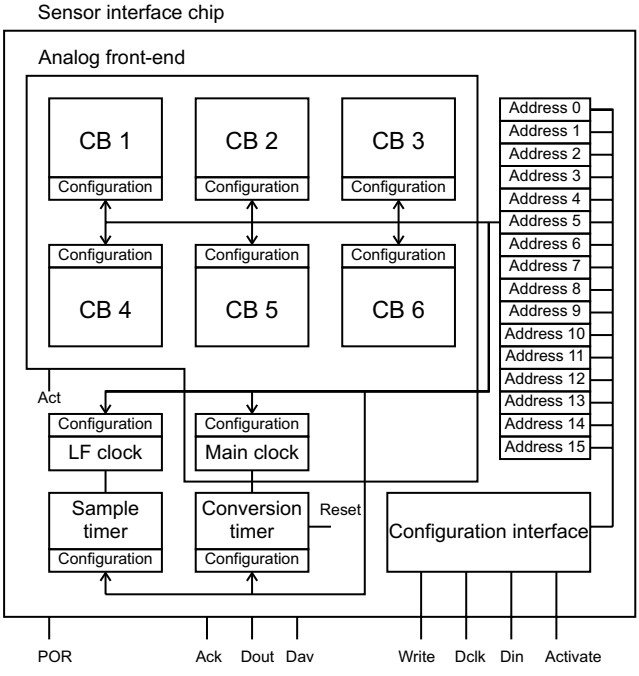

Figure 2.2. Functional description of the modular sensor interface chip.

programmable amplifiers, filters, data converters, clocks, etc. The configuration settings and the combination of these blocks can be changed according to the needs of the application. Furthermore, the modular system can be easily expanded with new building blocks to provide extra features. The settings of these blocks are stored in a configuration SRAM. The configuration interface allows the microcontroller to change the settings in a power efficient way. It contains modes for fast and complete reconfiguration. In the fast reconfiguration, only the settings of one specified address are changed. This is very useful during the calibration of one specific interface parameter. Furthermore, it is a handy manner to enter or leave a low power mode during operation. In the complete reconfiguration, all the settings of the sensor interface chip are reprogrammed. The normal operation flow stops during both configuration modes. So, the sensor interface chip is in a reset state. After completion of the programming phase, the sensor interface chip leaves the reset state and starts operating autonomously. It amplifies the sensor signals and converts them to a digital code. These digitized sensor data are transferred asynchronously to the microcontroller.

3.1 Programming flow

Four pins are used during the programming of the sensor interface: *Write*, *Activate*, *Dclk* and *Din*. When *Write* is high, the microcontroller is busy with programming and the operation flow is in a reset state. During this phase, the sensor interface loads the serial configuration data *Din* at the falling edge of *Dclk*. The *Activate* pin represents the configuration state of the sensor interface. Activate is low, when the configuration is not finished. After the configuration is complete, all the configuration flags of the SRAM memory are high, this results in a high *Activate* signal. This event is detected by the microcontroller, which lets the sensor interface enter the operation mode with the new configuration settings (*Write* becomes low).

The serial input data *Din* are generated in the following 16-bit format: ERN0 ERN1 A0 A1 A2 A3 D0 . . . D9. The first two bits (ERN0 and ERN1) encode the type of the input word. This word can be interpreted as a complete programming instruction, a fast programming instruction or a configuration word.

1 If (ERN0 ERN1) equals (1 0), the sensor interface chip needs to be fully reprogrammed. So, all the configuration flags become low. In this case, the other 14 bits in the word are don't care bits.

2 If (ERN0 ERN1) equals (0 1), only address A0 A1 A2 A3 needs to be reprogrammed. So, only the configuration flag of this address becomes low.

3 If (ERN0 ERN1) equals (0 0), the data D0 . . . D9 are loaded at the configuration address A0 A1 A2 A3. Hence, the configuration flag of this address becomes high.

Figs. 2.3 and 2.4 show the flow charts for the complete and fast configuration modes.

The proposed interface combines simplicity with low power consumption. It uses only 4 pins and saves a lot of energy, since the clock *Dclk* is only provided during the programming phase. Furthermore, the fast reconfiguration is an energy and time efficient option to change only one parameter during the operation. This is attractive in many applications. As an example, we consider

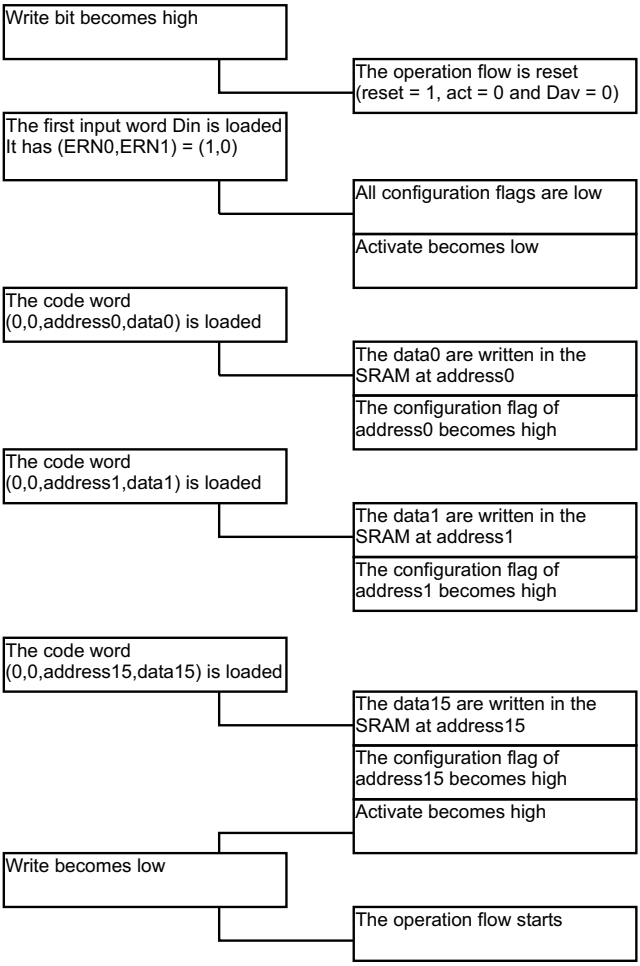

Figure 2.3. Flow chart for the complete reconfiguration mode.

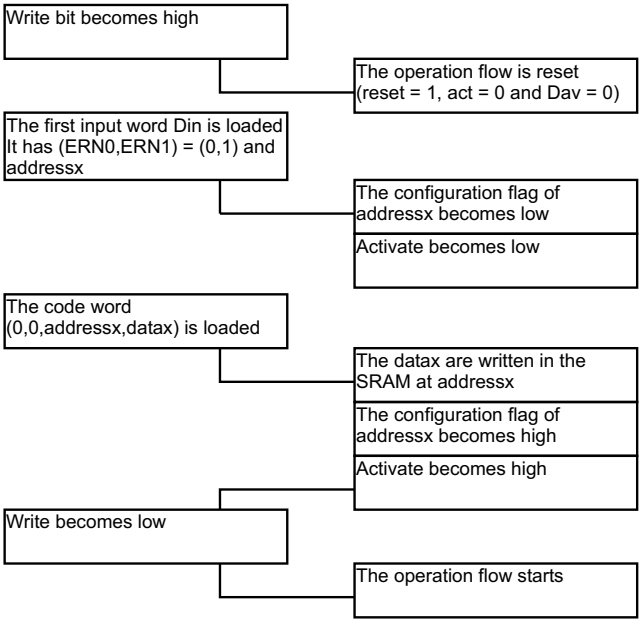

Figure 2.4. Flow chart for the fast reconfiguration mode.

the case of the smart energy management in event-triggered microsystems. In order to save the supply energy, the system is in a sleep mode. If some important event is happening, the fast reconfiguration makes the system enter the operational mode quickly and an accurate monitoring can start.

3.2 Operational flow

The programmed sensor interface chip operates autonomously. Its duty cycle operation is controlled with the sample and conversion timers. The LF clock and sample timer are running all the time, while the analog front-end and main clock are only operating in the active mode. During this active mode, the signal is converted into a digital output code. After this conversion, the sensor interface chip enters the standby mode (the analog front-end and the main clock are switched off) and puts the data available signal, *Dav*, high. This event wakes the microcontroller in order to load the digital data, *Dout*. The acknowledgement signal, *Ack*, becomes high after a successful transfer. This resets *Dav* and eventually *Ack* becomes low. When the sample timer reaches N_{sample} counts, it is reset and the process starts again (Fig. 2.5).

The microcontroller and sensor interface chip work independent in this operation flow. The communication is only set up for data transfer from the sensor interface chip to the microcontroller. The exact time and duration of

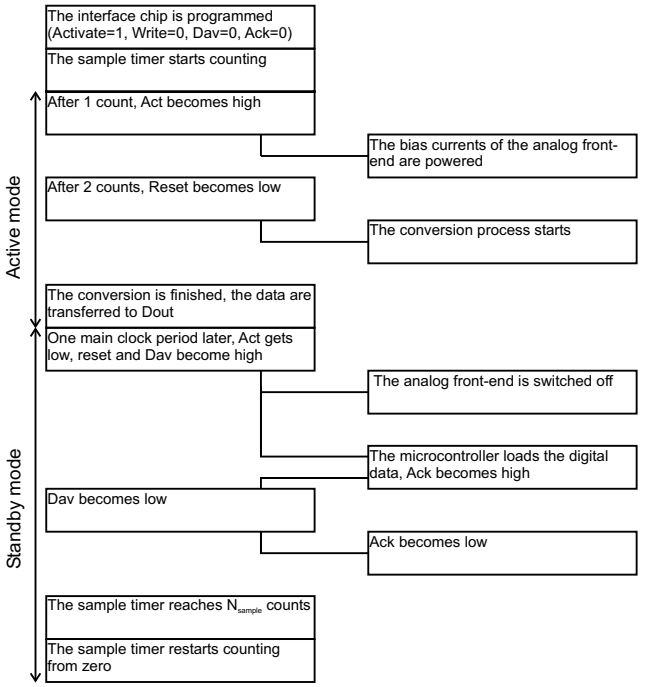

Figure 2.5. Operational flow of the modular microsystem.

this asynchronous transfer are unimportant. The system functions correctly, if the data transfer is completed during the standby mode of the sensor interface.

4. Conclusion

A generic platform for autonomous sensors would be a significant step towards low cost, flexible and easy to use sensor nodes for the smart environment. Such a general multisensor microsystem consists of a multisensor array, a sensor interface chip, a microcontroller, a wireless link and a power management. An open module architecture with plug and play approach allows to create an adequate solution for each application. Hence, most of the applications benefit from a generic sensor interface architecture, where only the sensors and the microcontroller software are customized to the selected application.

In order to create such a generic platform, we have first derived the properties and design options for the different parts of the multisensor microsystem. Secondly, a new modular architecture was presented, which allows to create a complete sensor interface chip out of configurable blocks. The combination and the settings of these blocks can be changed according to the varying needs

of the application. Furthermore, the sensor system can be expanded with additional building blocks during the development phase. The fast reconfiguration offers a power and time efficient option to change only one interface parameter during operation. The programmed sensor interface functions autonomously and performs an asynchronous data transfer to the microcontroller.

Chapter 3

GENERIC SENSOR INTERFACE CHIP

1. Introduction

A modular design approach for autonomous sensors was presented in the previous chapter. These concepts are used to create an ULP Generic Sensor Interface Chip (GSIC). The GSIC performs an interface to a broad range of capacitive sensor applications with medium accuracy (8-10 bits) and low speed requirements (bandwidth $<$100 Hz).

This chapter presents the specifications, design and results of the GSIC. In the first section, the different types of micromachined capacitive sensors are studied. This results in a classification for capacitive sensors, which eventually leads to the specifications for the GSIC. Thereafter, several front-end architectures for capacitive sensors are studied. An optimal architecture is presented, which achieves the required specifications with a minimal total power consumption. The complete sensor interface chip contains Capacitance-to-Voltage converters, a Switched Capacitor (SC) amplifier, a $\Sigma\Delta$ modulator, an LF clock, a main oscillator, timing circuits, a bandgap reference and bias circuits. The design of these blocks is described in sections 3.2 to 3.7. All these blocks are highly configurable. The many configuration settings allow to optimize the interface for a broad range of applications (section 4). The noise calculations of the interface chip are presented in section 5. Finally, the GSIC is tested in state-of-the-art pressure and accelerometer applications. The implemented pressure monitoring system achieves a power consumption of 7.3 μW for a 10 Hz sample frequency and 8-bit accuracy in the 100 to 130 kPa range. In the acceleration monitoring system, we measured a 10.3 μW power consumption for a 10 Hz sample frequency and 9-bit accuracy in the $\pm$1 g range. Furthermore, the performance of these systems is compared with other generic sensor interfaces and dedicated (U)LP pressure and accelerometer systems.

2. Capacitive sensors

Capacitive sensors can measure different types of physical signals like humidity, acceleration, pressure and position. Capacitive sensors are suitable for autonomous sensor applications since they dissipate no power and offer a high sensitivity [Pue93]. The main disadvantage is the presence of high parasitic elements. Fig. 3.1 shows a simple electrical model of a single capacitive sensor, including the effects of a shunting conductance G_p and two parasitic capacitances C_{p1} and C_{p2}.

Mechanical capacitive sensors have a higher sensitivity, lower power consumption, better temperature performance and are less sensitive to drift than piezoresistive sensors. However, piezoresistive sensors have a simpler structure, fabrication process and readout circuit, since the resistive bridge provides a low impedance output voltage. Hence, capacitive sensors are most often used in low power and high performance applications. Mechanical capacitive sensors can be developed with bulk or surface micromachining [Fre98, Yaz98]. In bulk micromachining, the wafer is etched from the backside to form the desired structures in the silicon substrate. On the contrary, surface micromachined devices are fabricated from thin films deposited on the substrate. The surface micromachining technique is compatible with CMOS technology and allows to integrate the sensor and the interface circuit on the same die. This reduces the device size and the parasitic capacitances significantly. However, the smaller dimensions result in smaller capacitance values. Moreover, the surface micromachined (accelerometers and pressure) sensors have a much lower sensitivity and a larger mechanical noise due to their smaller mass. This results in harder noise requirements for the readout circuit, which gives a higher power consumption for the input amplifiers. Hence, we will mainly focus on bulk micromachined capacitive sensors in our ULP generic capacitive sensor readout.

In order to characterize the capacitive sensors from different kinds of applications, we define the mean capacitance C_0 and the relative full-scale deviation

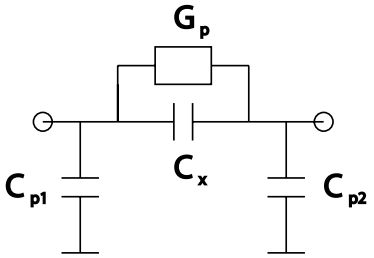

Figure 3.1. An electrical model of a single capacitive sensor with sense capacitance C_x, parasitic shunt conductance G_p and parasitic capacitances C_{p1} and C_{p2}.

α as:

$$C_0 = \frac{C_{x,min} + C_{x,max}}{2} \tag{3.1}$$

$$\alpha = \frac{\Delta C}{C_0} \tag{3.2}$$

where $C_{x,max}$ and $C_{x,min}$ are the maximal and minimal capacitance in the given sensor application. In order to develop a generic capacitive sensor interface with ULP consumption the following two difficulties need to be solved:

- The various capacitive transducer applications that have been reported show a wide range of mean capacitances and relative full scale deviations. Fig. 3.2 gives a graphical view of α and C_0 on different types of capacitor sensor applications found in literature [Mas98, Pue97, Pue00, Lap96, Yaz03, Sel97, Sei90, Tay00, Pue90, DB02, Cha02, Cha00, Egg00, Kan00, Lac03]. The α and C_0 values depend on the type of excitation (acceleration, pressure, humidity, etc.), the physical input range of the intended application, the sensor structure and the technology.

- The reduction of the effect of the parasitic elements with the lowest power consumption requires new interface architectures.

The proposed readout circuit provides an interface to single and differential capacitive sensor applications with 1 pF $< C_0 <$ 15 pF, 0.05 $< \alpha$, 200 fF $< \Delta C (= \alpha C_0) <$ 10 pF, $C_{p1} <$ 50 pF and $C_{p2} <$ 50 pF.

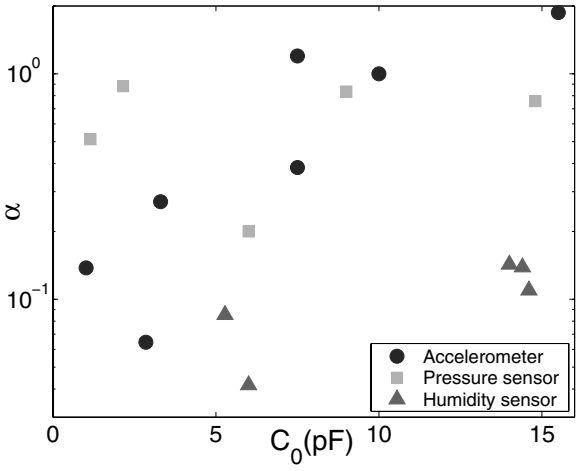

Figure 3.2. The relative full-scale deviation, α, as a function of the mean capacitance, C_0, for several capacitive microsystems.

3. Generic Sensor Interface Chip for capacitive sensors

A modular Generic Sensor Interface Chip (GSIC) for capacitive sensors will be developed. The chip is equipped with many configuration settings to offer an interface for a broad range of capacitive sensors. Furthermore, it contains a smart energy management, which adapts the averaged power consumption according to the speed and accuracy requirements of the selected application.

The GSIC contains a microcontroller interface, a configuration memory and the following configurable blocks (Fig. 3.3): LF clock, sample timer, reference and bias circuits, main oscillator and clock generation circuits, Capacitance-to-Voltage (C-V) converters, Switched Capacitor (SC) amplifier, voltage-to-current (VI) converter, modulator, decimation counter and conversion timer. The SC interface converts a capacitance variation ΔC in a proportional voltage. It consists of two C-V converters and an SC amplifier. In the C-V converters, the sense capacitance, C_x, is converted to a proportional voltage. The SC amplifier amplifies the difference between the outputs of the C-V converters and produces a quasi continuous input voltage for the $\Sigma\Delta$ modulator (VI converter and modulator). The main oscillator and clock generation circuits provide the clock signals to the capacitive sensor interface and the decimation counter. The reference and bias circuits generate the bias currents for the sensor interface and the main oscillator. The capacitive sensor interface, the main oscillator, the reference and the bias circuits are only powered in active mode (Act is high). The LF clock and sample timer are used for the timing during low power standby operation. They are the only parts of the system that are operating continuously. Therefore, they are implemented with a very low current consumption of approximately 500nA.

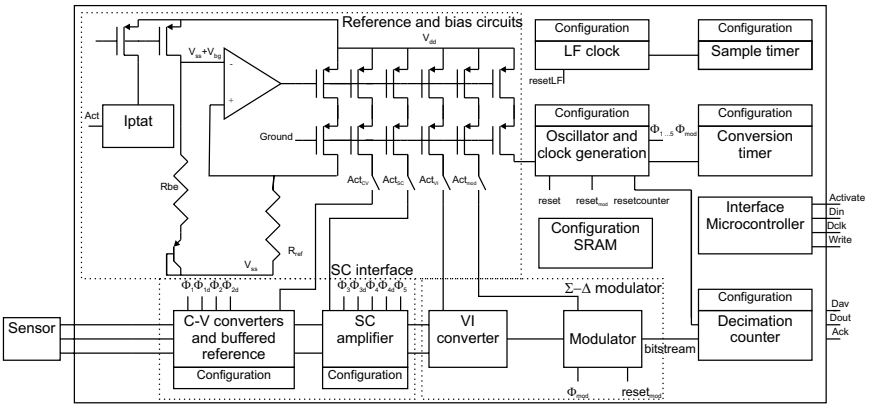

Figure 3.3. Functional description of the Generic Sensor Interface Chip for capacitive sensors.

3.1 Front-end architecture

Over the last decade, several readout circuits for capacitive sensors have been reported. These circuits can be divided into three groups [Yaz04]: square wave driven AC-bridge with voltage amplifier, harmonic driven AC-bridge with voltage amplifier and SC circuit.

A. Square wave driven AC-bridge with voltage amplifier

The square wave driven AC-bridge with voltage amplifier is shown in Fig. 3.4. The circuit consists of a half bridge, with the capacitors C_x and $C_{x'}$, driven by two opposite AC-signals V_{ref+} and V_{ref-}. The amplitude of the bridge output is proportional to the capacitance variation ΔC. This voltage is amplified and demodulated, which results in an output voltage:

$$V_{out} = A_v V_{ref} \frac{\Delta C}{2C_0 + C_p} \tag{3.3}$$

This architecture does not eliminate the effect of the parasitic capacitance, C_p. This degrades the performance significantly.

B. Harmonic driven AC-bridge with voltage amplifier

Fig. 3.5 shows the harmonic driven AC-bridge with voltage amplifier. The bridge output is held at virtual ground by an op-amp with resistive feedback, which reduces the effect of C_p. The drive signal, V_m, needs to be sinusoidal (frequency f_{drive}) to avoid errors induced by distortion. If f_{drive} is smaller than the bandwidth of the amplifier, the output voltage after demodulation equals:

$$V_{out} = 2\pi f_{drive} V_m R_f \Delta C \tag{3.4}$$

The need for a sinusoidal driving voltage complicates the design of the front-end significantly.

C. SC circuit

The SC circuit charges the sense capacitors with an opposite polarity and integrates these charges on a capacitor, C_{int} (Fig. 3.6). Hence we obtain an output

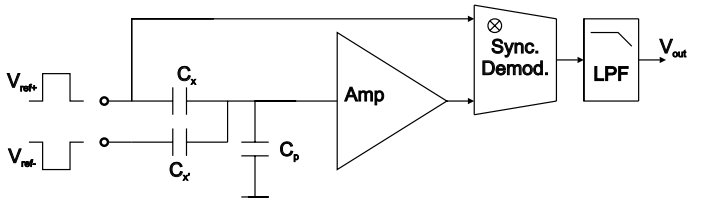

Figure 3.4. Square driven AC-bridge with voltage amplifier.

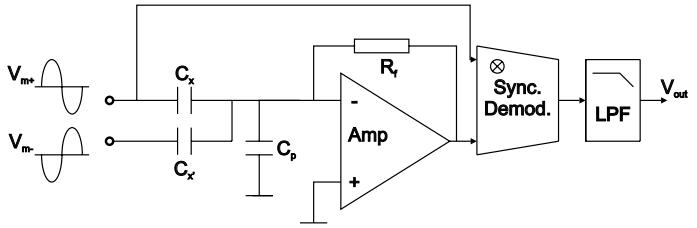

Figure 3.5. Harmonic driven AC-bridge with voltage amplifier.

voltage, which equals:

$$V_{out} = V_{ref} \frac{\Delta C}{C_{int}} \tag{3.5}$$

This circuit also eliminates the effect of the parasitic capacitances and does not need complex driving voltages.

D. Open loop ULP ΣΔ architecture

Many sensor systems reported in literature use off-the-shelf analog-to-digital converters. This approach complicates the design of the analog front-end, because a buffered analog voltage has to be transferred to the ADC chip. As shown in Fig. 3.7, the system can be considerably simplified by merging the analog part of a first order ΣΔ ADC with the front-end circuit and by implementing the digital filtering and processing in the microcontroller or DSP [Mei02, Rie93].

Many capacitive sensor interfaces use the sensor directly in a ΣΔ modulator structure [Lem99, Wan98, Kul06, Kaj02]. This leads to high power consumption, because the capacitors must be charged and discharged on the rhythm of the high oversampling clock of the modulator. Most of these sensor interfaces are designed for closed loop accelerometers. In these circuits, the electrostatic feedback force is used to keep the sensor mass in its balanced position, which results in a high linearity. Hence, the mechanical transfer characteristic acts

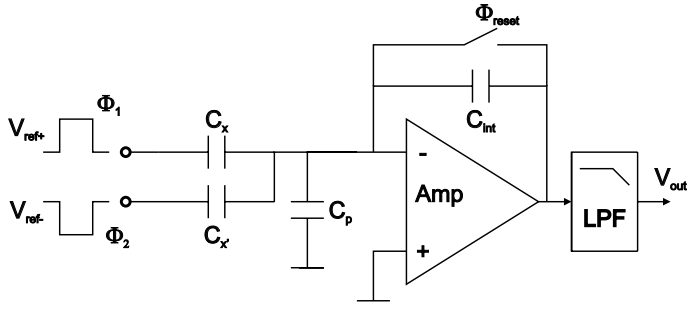

Figure 3.6. Switched Capacitor circuit.

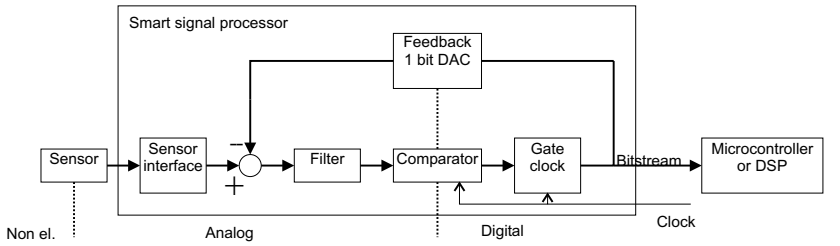

Figure 3.7. Smart sensor system architecture with first order $\Sigma\Delta$ modulator.

as a second order filter in the $\Sigma\Delta$ loop. As a consequence, the stability and the performance of the readout circuit strongly depend on the specific sensor [Pet06]. Moreover, these systems need an important start-up time to bring the sensor mass close to equilibrium [Kul03]. So, it is not possible to operate them in a power efficient duty cycle.

To combine the advantages of a $\Sigma\Delta$ modulator structure and still maintain low power consumption, we introduce a new open loop architecture, which uses a low clock frequency, 8 kHz, for the SC interface (C-V converters and a SC amplifier) and a higher clock frequency, 128 kHz, for the $\Sigma\Delta$ modulator (Fig. 3.8). Reducing the clock frequency of the SC interface increases the influence of the parasitic shunt conductance. Since the shunt conductance is highly dependent on the pollution and condensation, it can cause a serious reliability problem. So, the decrease of this effect is an important issue in the design of an ULP interface for capacitive sensors. The effect can be reduced by performing a dedicated series of eight measurements as explained in [Li00]. However, the method is not power efficient, since it requires a long measurement time.

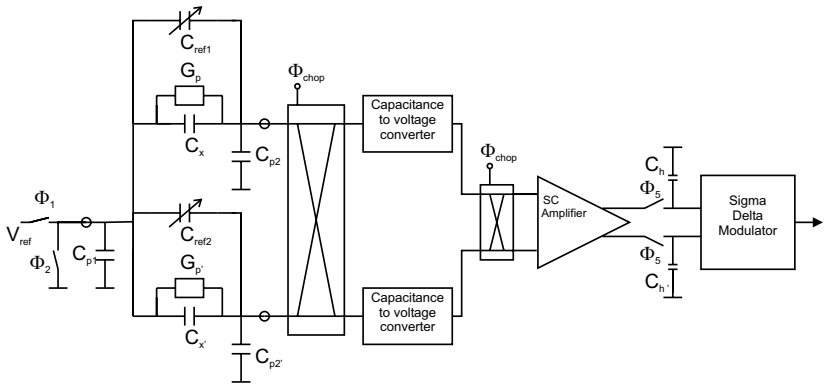

Figure 3.8. Capacitive sensor readout architecture.

This work presents a C-V converter, which uses class AB circuit techniques and Correlated Double Sampling (CDS) operation to reduce the influence of the parasitic shunting conductance while maintaining a low clock frequency and low power consumption. The C-V converter performs charge leakage suppression, which is several times higher than more conventional designs with the same power consumption. The front-end also contains an enhanced chopping scheme, which eliminates the effect of mismatches between both C-V converters. The capacitive sensor interface has two modes of operation. The first mode is for single sensor operation with on chip reference capacitor, where the reference capacitor C_{ref2} needs to be programmed to approximate C_0. The other mode is for differential sensor operation, where the on chip reference capacitor C_{ref1} (or C_{ref2}) is programmed to compensate for the offset between C_x and $C_{x'}$. In both modes the amplification factor A_{SC} of the SC amplifier and the feedback capacitor C_f need to be programmed for optimal accuracy of the interface.

3.2 Capacitance-to-Voltage convertor

Fig. 3.9 shows a conventional state-of-the-art capacitance-to-voltage converter. It is known that this circuit is very effective in reducing the effects of the parasitic capacitors C_{p1} and C_{p2}.

During the sampling phase Φ_1, the sense capacitor C_x is charged. During the signal phase Φ_2, V_p becomes a virtual ground and the charge is transferred to the feedback capacitor C_f. At the end of the signal phase, assuming an ideal charge transfer, the voltage at the output of the C-V converter equals $V_{ref}C_x/C_f$. In reality the charge transfer will be imperfect. During Φ_2 a part of the signal charge is leaking away through the parasitic shunt conductance G_p. This leakage charge has three contributions. The first contribution is due to the finite transient response of the Operational Transconductance Amplifier (OTA), which causes the potential V_p to settle in a certain time to the virtual ground potential, and during this transient time a charge will leak away. The second

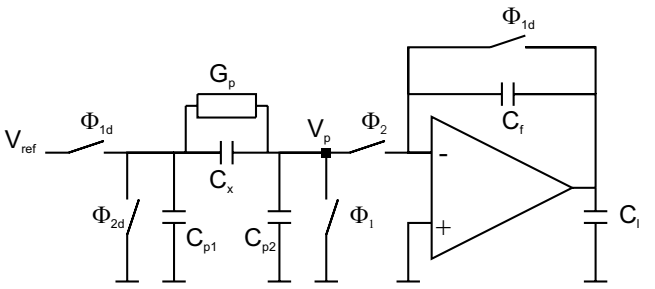

Figure 3.9. Conventional state-of-the art Capacitance-to-Voltage converter.

contribution is due to the offset voltage of the OTA, which creates a leakage charge proportional to $V_{offset}G_pT_{phase2}$. The third contribution originates from the finite DC gain A_v of the OTA, which in turn leads to a leakage charge proportional to $(V_{out}/A_v)G_pT_{phase2}$.

In [Li02], Li et al. use the conventional state-of-the-art C-V converter in combination with a chopping technique and the three-signal autocalibration method. This interface eliminates the offset leakage and compensates for the drift in the readout electronics. Unfortunately, the technique is not energy efficient, since it requires four measurement cycles and three extra voltage sources to determine C_x.

Fig. 3.10 shows the proposed ULP C-V converter. This interface needs only one voltage source V_{ref} and one measurement cycle to determine C_x. It uses Correlated Double Sampling (CDS) to eliminate the effect of the offset voltage on the sensor interface [Lam83]. During Φ_1, the capacitor C_s samples the offset voltage. During Φ_2, the sampled offset is subtracted from the instantaneous one.

The C-V converter uses a class AB OTA with cascode output stage (Fig. 3.11, 3.12). The class AB operation is a power efficient solution to reduce the transient leakage. After the transition from phase Φ_1 to phase Φ_2, the tail current of the OTA is boosted, which speeds up the charge transfer from the sense capacitor to the feedback capacitor. During settling, the voltage V_p approaches the virtual ground and the tail current falls back to a low quiescent level.

In order to understand the operation of the OTA circuit [Har99], it is important to note that the common source voltage of M_1 and M_2 is forced by the internal negative feedback to follow the larger of the two voltages V_a and V_b. When V_{in-} is smaller than V_{in+}, the output voltage V_{outop2} of the op-amp $op2$ is pulled to the positive supply and the common source voltage V_s equals V_b. So, V_s is only determined by V_{in+}, the bias current I_{bias} and the dimensions of the transistor M_b. Since the input transistors are biased in weak inversion mode,

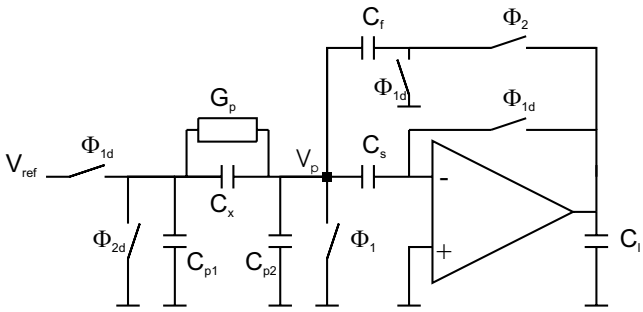

Figure 3.10. Capacitance-to-Voltage converter with correlated double sampling and class AB operation.

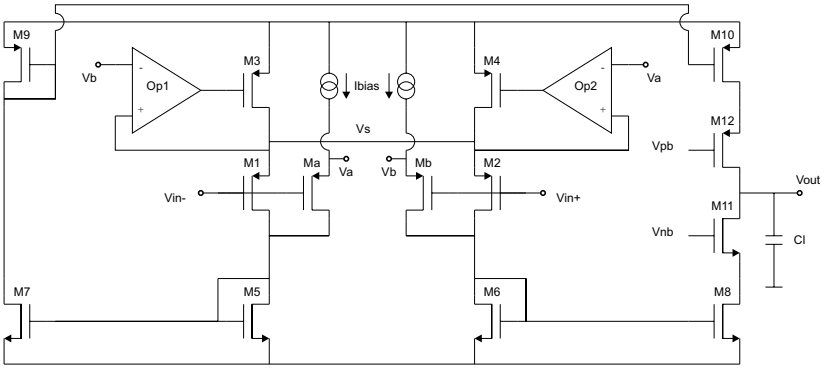

Figure 3.11. Class AB OTA.

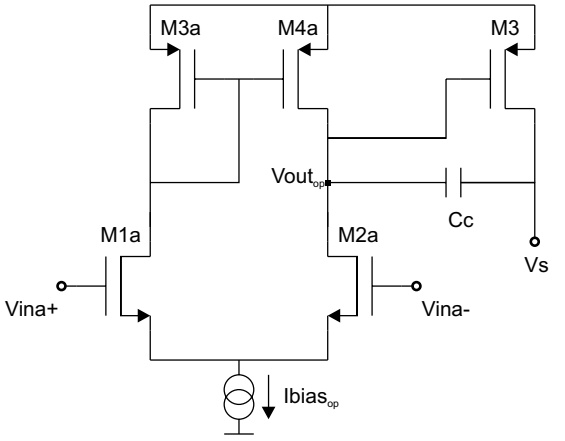

Figure 3.12. Internal feedback op-amp *op*.

current boosting for small $\Delta V_{in} = V_{in+} - V_{in-}$ is proportional to:

$$\frac{I_{M1}}{I_{M2}} = \exp\left(\frac{V_{in+} - V_{in-}}{nU_T}\right) \tag{3.6}$$

where n is the weak inversion slope factor and $U_T = (kT/q)$ is the thermal voltage. For larger ΔV_{in} the input transistors leave the weak inversion region and the current boosting is less steep than predicted by equation 3.6. Input transistors with larger W/L ratio improve the current boosting, since they operate in a deeper weak inversion mode.

The internal feedback op-amps, $op1$ and $op2$, need to be fast Miller OTA's to realize a short tracking time and a high current efficiency. The stability of this feedback mechanism is guaranteed by the compensation capacitor C_c. The op-amps, $op1$ and $op2$, are loaded by the gate source capacitances of M_1 and M_2.

Hence, larger dimensions (W/L) of M_1 and M_2 result in a larger C_c and a higher current consumption of $op1$ and $op2$ to maintain a fast tracking response. So, an optimal AB OTA needs to consider both the current boosting capabilities and the internal feedback behavior. In our designed AB OTA, the internal feedback mechanism has a phase margin of 81 deg (small signal approximation) and a tracking time smaller than 5 μs. The op-amps, $op1$ and $op2$, consume a current of 125 nA. The current boosting, I_{M1}/I_{M2}, equals 85 for an input voltage, ΔV_{in}, of 0.4 V (OTA in unity-gain feedback configuration). The class AB OTA uses a cascode output stage to achieve a high gain.

The clocks Φ_{1d} and Φ_{2d} are slightly delayed with respect to Φ_1 and Φ_2. This makes the charge injections appear as an offset on the outputs of the C-V converters [Joh97]. The SC amplifier amplifies the difference between the outputs of both C-V converters. So, the effects of charge injection in the C-V converters are eliminated.

In order to minimize power consumption, one should choose the interface clock frequency as low as possible. Our ability to reduce the clock frequency is limited by the accuracy considerations. First of all, a low clock frequency will make CDS less effective in reducing 1/f noise. Secondly, lowering the clock frequency results in undersampling the OTA noise bandwidth by a too high factor and degrades the system's noise performance. Lastly, a low clock frequency will increase the effects of electrostatic forces on accelerometers [Bao00, Pue96]. Depending on these arguments, calculations show that a clock frequency of 8 kHz is an optimal choice for our interface.

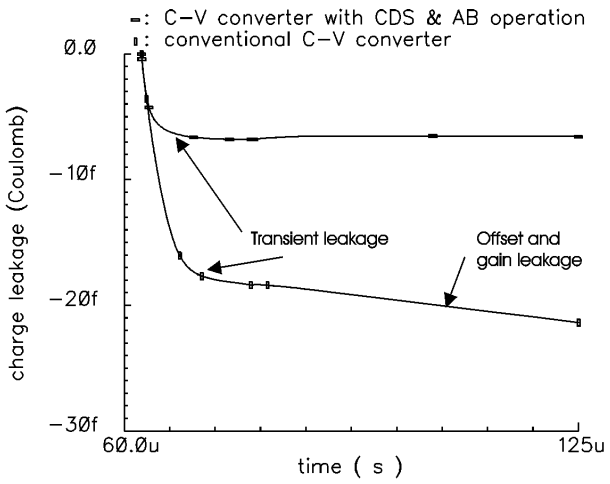

Figure 3.13. Charge leakage during signal phase Φ_2.

In order to compare a conventional C-V converter to the proposed one, both structures are biased (Fig. 3.9 vs. Fig. 3.10) with the same average current consumption (3.5 μA). Fig. 3.13 shows the charge leakage during phase Φ_2 for both C-V converters with the following properties: V_{ref} = 1 V, C_x = 10 pF, $C_{p2} = C_{p1}$ = 5 pF and G_p = 0.01 μS, feedback capacitor C_f = 27 pF, C_s = 5 pF and C_l = 10 pF. It can be seen that the new C-V converter performs a much faster charge transfer. The offset and gain leakage are almost perfectly eliminated by the high DC gain OTA and the CDS operation. Our C-V converter has a charge leakage, which is approximately three times lower than the traditional one. The simulated leakage charge equals 7 fC, which is approximately 0.07 % of the signal charge. So, the error is smaller than 10 bits for this application.

3.3 Chopping scheme

The mismatch between the switches and feedback capacitors of both C-V converters causes errors in the transfer characteristic of the sensor front-end. It also makes the interface more susceptible to interference. This can cause an extra loss in accuracy. With mismatches, we obtain the following outputs, $V_{C-V,+}$ and $V_{C-V,-}$, for the C-V converters:

$$V_{C-V,+} = \left(Q_+ + Q_{offset} + \frac{\Delta Q_{offset}}{2} + Q_{EMI} \right) \frac{1}{C_f + \frac{\Delta C_f}{2}} \tag{3.7}$$

$$V_{C-V,-} = \left(Q_- + Q_{offset} - \frac{\Delta Q_{offset}}{2} + Q_{EMI} \right) \frac{1}{C_f - \frac{\Delta C_f}{2}} \tag{3.8}$$

where Q_+ and Q_-, $Q_{offset} + \frac{\Delta Q_{offset}}{2}$ and $Q_{offset} - \frac{\Delta Q_{offset}}{2}$, Q_{EMI} and $C_f + \frac{\Delta C_f}{2}$ and $C_f - \frac{\Delta C_f}{2}$ are the sampled sense charges on C_x and $C_{x'}$, the charge injections, the common mode electromagnetic interference and the feedback capacitors.
These equations can be simplified to:

$$V_{C-V,+} - V_{C-V,-} = \frac{Q_+ - Q_-}{C_f} + \frac{Q_+ + Q_-}{C_f} \frac{\Delta C_f}{2C_f} + \frac{\Delta Q_{offset}}{C_f} + \frac{Q_{EMI}}{C_f} \frac{\Delta C_f}{C_f} \tag{3.9}$$

This corresponds to a mismatch induced error:

$$Error_{mismatch} = \frac{Q_+ + Q_-}{Q_+ - Q_-} \frac{\Delta C_f}{2C_f} + \frac{\Delta Q_{offset}}{Q_+ - Q_-} + \frac{Q_{EMI}}{Q_+ - Q_-} \frac{\Delta C_f}{C_f} \tag{3.10}$$

The proposed chopping scheme provides a solution for this problem. In this scheme, a pseudo differential structure is built, where the capacitive sensor elements (C_x and $C_{x'}$) are connected to each C-V converter for an equal number of

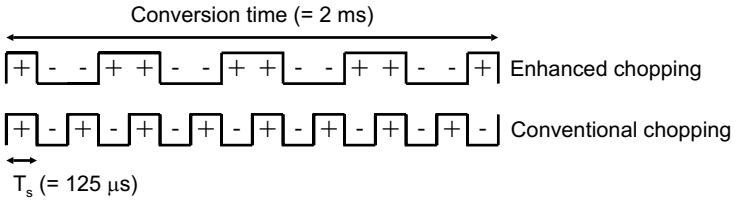

Figure 3.14. Conventional and enhanced chopping scheme during one $\Sigma\Delta$ modulator conversion period.

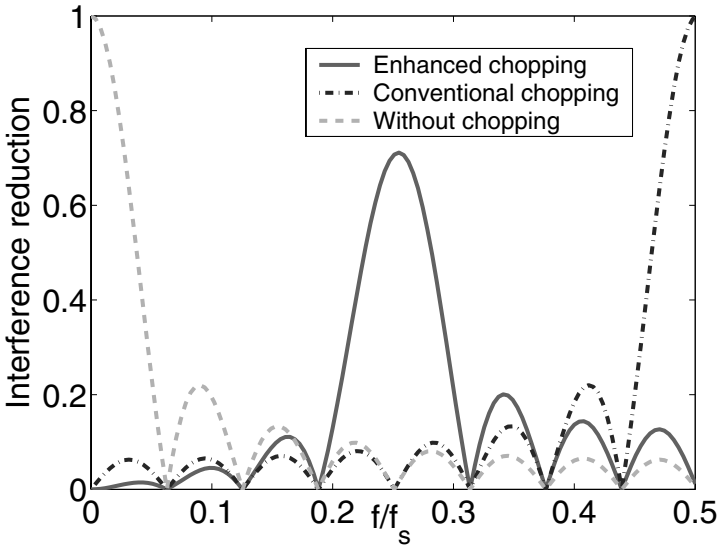

Figure 3.15. Frequency dependence of the interference reduction without chopping, with conventional chopping and with enhanced chopping.

interface periods. This modulates the effects of the mismatch with the chopping sequence. These components are filtered by the low pass operation of the $\Sigma\Delta$ modulator.

Fig. 3.14 compares the interference reduction of the enhanced chopping with a conventional chopping scheme for a $\Sigma\Delta$ conversion time of 2 ms. The enhanced chopping scheme is more efficient in eliminating low frequency interference ($f < 0.1 f_s$, where f_s is the SC interface frequency of 8 kHz) (Fig. 3.15).

3.4 SC amplifier

Fig. 3.16 shows the fully differential SC amplifier, which amplifies the difference between the outputs of the C-V converters [Mar87]. It uses a correlated

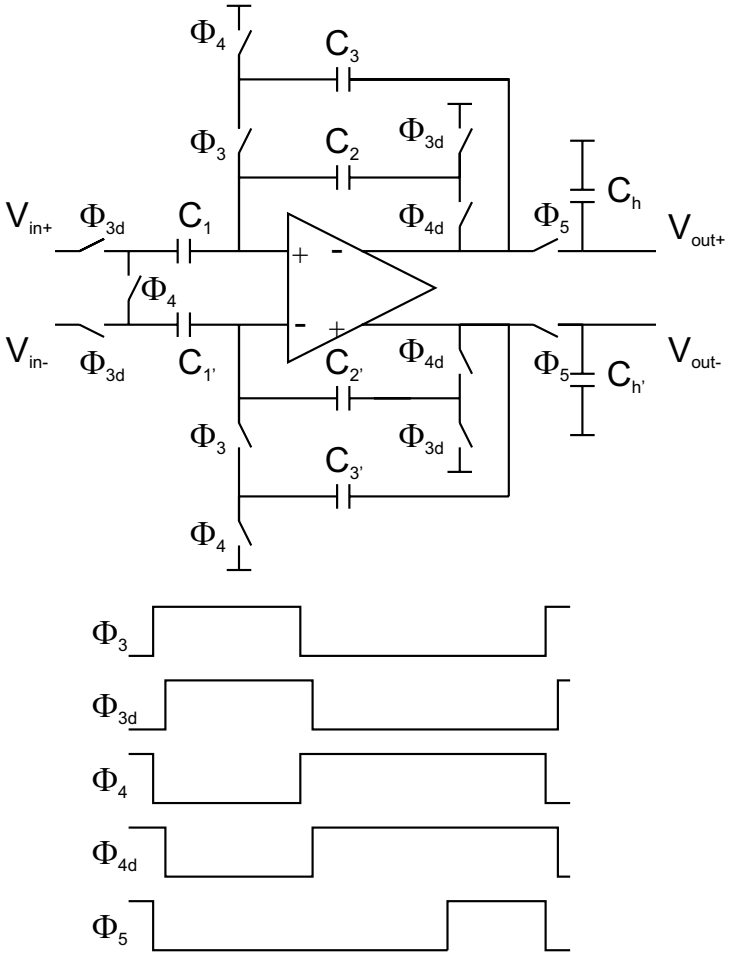

Figure 3.16. Fully differential SC amplifier with slew enhanced Correlated Double Sampling scheme.

double sampling scheme, which does not require any resetting of the output in each clock period. This topology is power efficient, since it allows more relaxed op-amp specifications for low frequency inputs. To reduce the influence of the charge injection, the clocks Φ_{3d} and Φ_{4d} are slightly delayed with respect to Φ_3 and Φ_4. The outputs of the SC amplifier are sampled on the hold capacitors C_h and $C_{h'}$ during phase Φ_5, so a quasi continuous output voltage is provided to the input of the analog-to-digital converter.

The behavior of the SC amplifier can be characterized in a state model. Fig. 3.17 shows the half circuit for the differential mode characteristics.

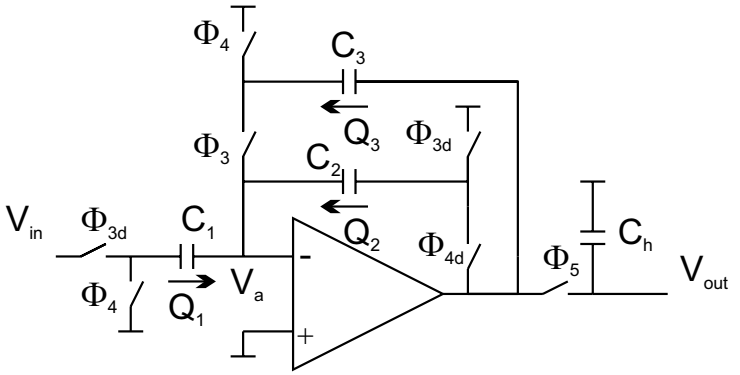

Figure 3.17. Half circuit of the SC amplifier (study of differential characteristics).

During the sampling phase Φ_3, we obtain the following set of equations:

$$q_{1,n-\frac{1}{2}} = -\left(V_{in,n-\frac{1}{2}} - V_{a,n-\frac{1}{2}}\right) C_1 \tag{3.11}$$

$$q_{2,n-\frac{1}{2}} = V_{a,n-\frac{1}{2}} C_2 \tag{3.12}$$

$$q_{3,n-\frac{1}{2}} = -\left(q_{2,n-\frac{1}{2}} - q_{2,n-1}\right) - \left(q_{1,n-\frac{1}{2}} - q_{1,n-1}\right) + q_{3,n-1} \tag{3.13}$$

$$V_{out,n-\frac{1}{2}} = V_{a,n-\frac{1}{2}} - \frac{q_{3,n-\frac{1}{2}}}{C_3} \tag{3.14}$$

$$V_{out,n-\frac{1}{2}} = -A_{diff}\left(V_{a,n-\frac{1}{2}} - V_{offset}\right) \tag{3.15}$$

where A_{diff} and V_{offset} are the differential gain and the offset of the OTA. During the signal phase Φ_4, we obtain the following set of equations:

$$q_{1,n} = V_{a,n} C_1 \tag{3.16}$$

$$q_{2,n} = -\left(q_{1,n} - q_{1,n-\frac{1}{2}}\right) + q_{2,n-\frac{1}{2}} \tag{3.17}$$

$$q_{3,n} = -V_{out,n} C_3 \tag{3.18}$$

$$V_{out,n} = V_{a,n} - \frac{q_{2,n}}{C_2} \tag{3.19}$$

$$V_{out,n} = -A_{diff}\left(V_{a,n} - V_{offset}\right) \tag{3.20}$$

With these sets of equations, we can derive a discrete state model of the form:

$$X_n = AX_{n-1} + BV_n \tag{3.21}$$

$$Y_n = CX_n \tag{3.22}$$

In this model, we take the state vector $X_n = (x_{1,n} = q_{1,n-\frac{1}{2}}, x_{2,n} = q_{2,n-\frac{1}{2}}, x_{3,n} = q_{3,n-\frac{1}{2}}, x_{4,n} = q_{1,n}, x_{5,n} = q_{2,n}, x_{6,n} = q_{3,n})$, the input vector $V_n = (v_{1,n} = V_{in,n-\frac{1}{2}}, v_{2,n} = V_{offset})$ and the output vector $Y_n = (y_{1,n} = V_{out,n-\frac{1}{2}}, y_{2,n} = V_{a,n-\frac{1}{2}}, y_{3,n} = V_{out,n}, y_{4,n} = V_{a,n})$.

The step response of the amplifier converges to a voltage

$$\lim_{n\to\infty} V_{out,n} = V_{in}\frac{C_1}{C_2}\left(1 - \frac{C_1 + C_2}{C_2 {A_{diff}}^2}\right) + \frac{C_1 + C_2}{C_2}\frac{V_{offset}}{A_{diff}} \tag{3.23}$$

Hence, the gain error is reduced with a factor $1/({A_{diff}}^2)$. This would allow the use of a low gain OTA. However, the transient response is also affected by the differential gain of the OTA. A_{diff} needs to be larger than 10000 to achieve an error smaller than 0.004 after one clock period (Fig. 3.18).

The SC amplifier uses a fully differential folded cascode OTA with SC common mode feedback to achieve a high gain (Fig. 3.19). The input transistors of the OTA are biased in weak inversion to reduce the power consumption. The phase margins of the OTA and the common mode feedback equal 78 deg and 82 deg. The phases Φ_3, Φ_4 and Φ_5 take 3/8, 5/8 and 2/8 of the clock period. The equivalent load capacitor, C_{load}, equals:

$$C_{load} = \frac{8}{3}\left(C_l + C_{c,cmfb} + C_{s,cmfb}\right) = \frac{8}{2}C_h \tag{3.24}$$

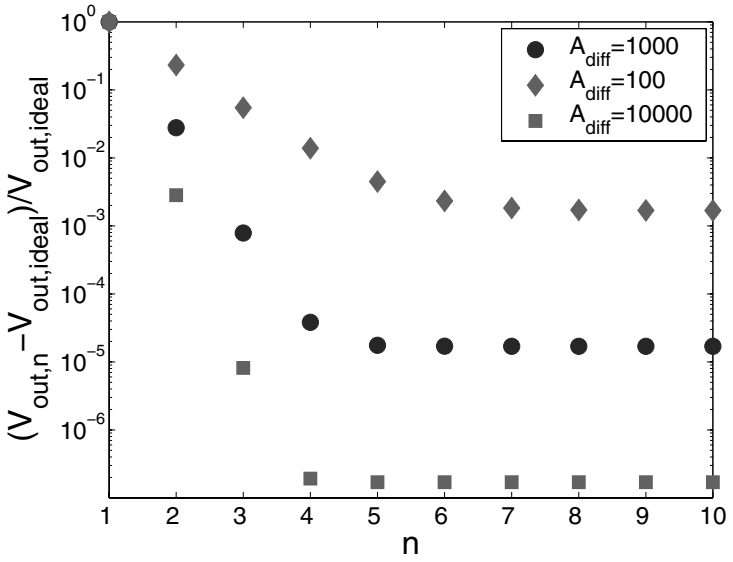

Figure 3.18. Transient error as a function of the clock cycle, n.

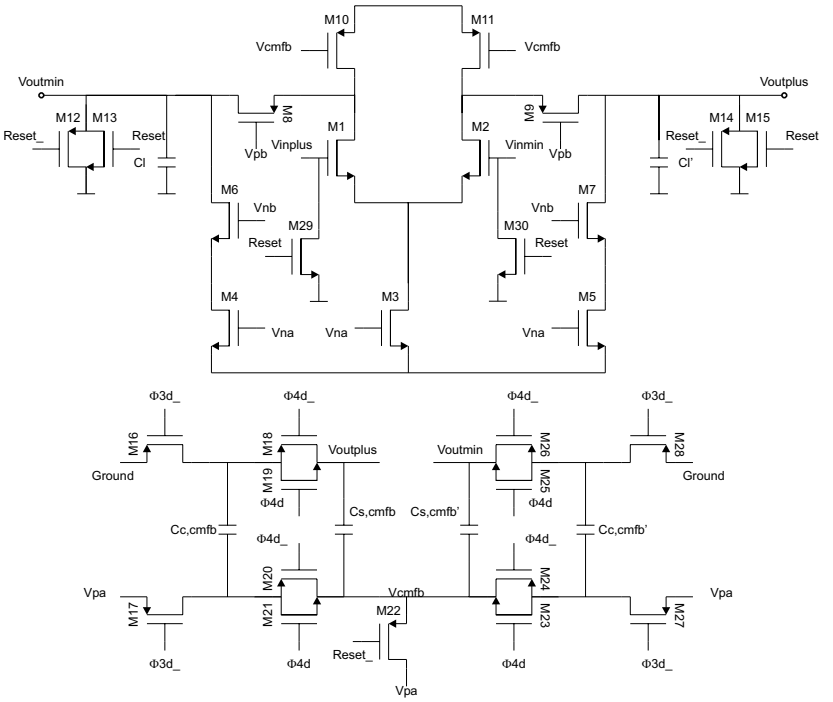

Figure 3.19. Differential folded cascode OTA with SC common mode feedback.

where the contribution of the feedback capacitor $\frac{C_2C_1}{C_1+C_2}$ in the load capacitor can be neglected, because $\frac{C_2C_1}{C_1+C_2} << C_h, C_l$.
The equivalent $GBW\left(=\frac{g_m}{2\pi C_{load}}\right)$ of the OTA equals 160 kHz, which is 20 times the clock frequency. Since the SC amplifier has a maximal programmable gain of 16, the settling error will be smaller than $\exp(-2\pi\frac{20}{16}) \approx 0.05\%$. So, the SC amplifier performs an adequate settling behavior for each gain setting.

3.5 ΣΔ modulator

The $\Sigma\Delta$ modulator structure allows one to adapt the system and its energy consumption to the selected sensor application. The accuracy of the ADC is determined by the conversion time, i.e., the number of oversampling clock periods that are used to acquire the digital bit code. Since many sensor signals have a very small bandwidth (typical order of a few tens of Hz) and a medium resolution is sufficient (8-10 bits), the system can operate in a duty cycle, where the analog readout circuitry is only for a short period of time in the ON-state. Other important advantages of the $\Sigma\Delta$ architecture are the immunity against

digital interference and locking effects and the relaxed specifications for the analog components [Bos88].

The modulator and the digital decimation filter become more complex with increasing order of the sigma delta ADC. For higher order modulators the risk for instability is higher, so only 1st and 2nd order modulators can be realized with a reduced complexity [Jes00]. The choice between a 1st and 2nd order modulator is an important dilemma. A 2nd order modulator has the advantage that it gives 6 dB per octave oversampling ratio more resolution. Hence, the measurement time can be decreased to achieve the same resolution as in a 1st order modulator. However, a 2nd order structure needs a higher order decimation filter and a more complex modulator. A 1st order modulator can use a simple digital counter as decimation filter. This counter can easily be implemented on the sensor interface chip, which reduces power consumption.

Considering the overall medium resolution and low speed requirements, we have opted for a 1st order $\Sigma\Delta$ modulator. For more accurate and faster applications a 2nd order modulator would probably be a better choice.

Traditionally, most of the $\Sigma\Delta$ modulators are SC realizations. However the first order $\Sigma\Delta$ modulator presented in this work is a Continuous Time (CT) implementation. For this type of modulator the bandwidth and slew rate requirements are less stringent, which reduces the power consumption and makes the structure less sensitive to noise and digital interference. On the $\Sigma\Delta$ feedback side, the reference voltage of a SC modulator requires buffering to attain the oversampling speed (128 kHz). The DAC of the CT integrator can be implemented with current sources, which do not load the voltage reference dynamically. The main drawback of this structure is the accuracy limitation by the non-linearity of the voltage-to-current converter. For medium resolution applications this does not pose any problem, because the total harmonic distortion of the voltage-to-current converter can easily be better than -60 dB. Most of the CT modulators presented in literature are higher order modulators, which are designed for medium and high-speed applications. However, our first order sigma delta modulator is an ULP low frequency design for autonomous sensor systems. So, a review of the dominant error sources is necessary to achieve an optimal design for our application. The most important issues, that have been addressed in the design of the CT modulator, are given below.

- The charge injections, induced by a falling and a rising transition in the feedback DAC, are not perfectly equal in magnitude. So, every falling and rising transition pair injects an extra charge in the integrator capacitor, C_{int}, which results in an accumulating error charge on C_{int}. This charge injection imbalance creates a non-linearity, which is larger in the middle of the modulator input range, since at zero input the highest number of transitions occurs. The charge injection imbalance has several causes: the difference between the rising and the falling edge delay time of the quantizer output

[Ada86] (this phenomenon is more dominant for high speed modulators), the mismatch between the DAC switches and the residual voltage between the positive and negative input of the integrator op-amp.

- The current leaking away from the integrator can also cause non-linearity problems [Fee91]. This effect can be reduced by using an integrator op-amp with a high DC gain and by using a current DAC and a voltage-to-current converter with high output impedances.
- The clock jitter creates a random variation in the timing. This introduces a random change in the amount of charge delivered to the CT loop between successive iterations [Che99].
- The non-idealities of the quantizer.
- The noise current injected in C_{int} limits the dynamic range of the modulator. The total noise contains contributions of the voltage-to-current converter and the current DAC.

The CT $\Sigma\Delta$ modulator can be a Non-Return-to-Zero (NRZ) or a Return-to-Zero (RZ) implementation. For NRZ modulators, the charge injection depends on the previous DAC symbols. In this case, the feedback DAC codes (101) and (110) have a different effect on the charge transfer to C_{int}. This creates a distortion in the conversion result. These effects are eliminated in a RZ modulator. During each clock cycle, this modulator switches according the quantizer decision for part of the time and resets to zero for the rest. In this way, independent of the quantizer decision, both a rising and a falling edge appear in the DAC pulse. Hence, the intersymbol interference is reduced. On the other hand, the clock jitter is lower in NRZ than in RZ modulators, since NRZ modulators have a smaller number of transitions. Because the charge injection imbalance dominates the clock jitter in our design, we have chosen for a RZ implementation.

A. RZ CT $\Sigma\Delta$ modulator

Fig. 3.20 shows the proposed RZ CT $\Sigma\Delta$ modulator. After the reset signal becomes low, switches 1 and 3 are closed and switches 2 and 4 are open. The output current of the VI converter is integrated on the capacitor C_{int}. The regenerative comparator executes his decision during the modulation phase Φ_{mod}. At the end of this phase, the output of the comparator is settled and saved in the following latch. After the rising edge of the feedback clock Φ_{fb}, the switches in the current DAC are stimulated. If the state changes, the break operation is executed before the make operation. The clocks Φ_{zero1} and Φ_{zero2} are created out of Φ_{mod} by a non-overlapping clock generator circuit. The delay is chosen such that the falling edge of Φ_{zero1} comes after the rising edge of Φ_{fb}.

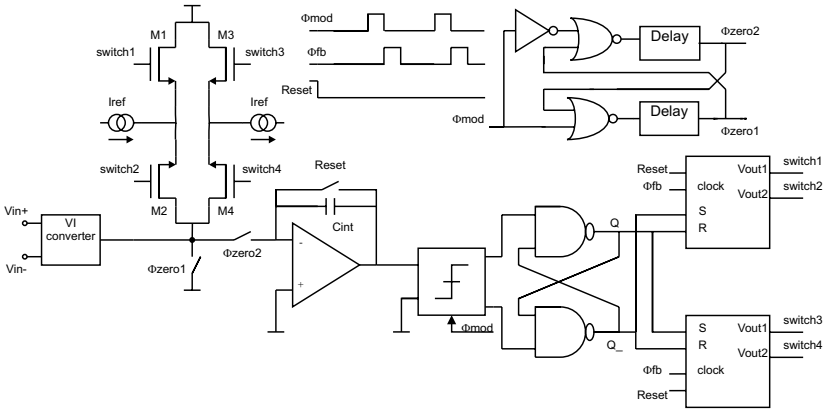

Figure 3.20. Simplified schematic of the RZ CT ΣΔ modulator with VI converter, a current DAC, an integrator, a comparator, a break-before-make feedback scheme and clocks.

Hence, the influences of charge injections due to transitions in the switches 1 to 4 are eliminated.

B. Voltage-to-current converter

Fig. 3.21 shows the VI converter, which transforms a differential voltage into a single ended current [Kwa91]. It contains a fully differential core to eliminate the even order distortion components. It uses p-type input transistors biased in subthreshold region with substrate to source connection, so the non-linearity and noise of the input transistors are limited. It has a high-impedance cascode output stage to reduce the integrator leakage. The total harmonic distortion decreases

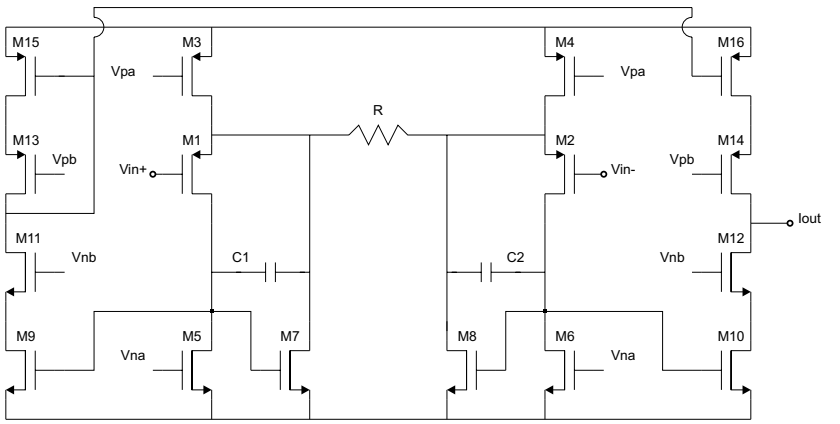

Figure 3.21. The voltage-to-current converter.

with increasing bias current. The voltage-to-current converter uses 1.8 μA. This allows a total harmonic distortion of -73 dB for a 0.5 Vpp differential sine input with frequency 100 Hz.

The VI converter has an internal feedback mechanism, which causes unstability when the compensation capacitors, C_1 and C_2, are omitted. The small signal scheme is used to study the frequency behaviour of the VI converter (Fig. 3.22).

The analysis of this network gives the following closed loop transfer function:

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{T}{N} \\ &\approx \frac{C_t C_c s^2 + C_{n1} g_{m1} s + g_{m1} g_{m7}}{C_c(C_t + C_{n1} + C_{n2})s^2 + C_c(g_{m7} + 2G)s + g_{m1} g_{m7}} \end{aligned} \tag{3.25}$$

The equivalent open loop transfer function can be calculated as:

$$\begin{aligned} \frac{T_{OL}}{N_{OL}} &= \frac{T}{N - T} \\ &\approx \frac{C_t C_c s^2 + C_{n1} g_{m1} s + g_{m1} g_{m7}}{C_c(C_{n1} + C_{n2})s^2 + C_c(2G + g_{m7})s + 2G(g_{o1} + g_{o5}) + g_{m7} g_{o1}} \end{aligned} \tag{3.26}$$

The internal loop gain of the designed VI converter ($C_1 = C_2 =$10 pF) has a GBW of 33 kHz and a phase margin of 85 deg (Fig. 3.23).
The simulated noise output current during one modulator period ($\approx 8\mu$s) equals 190 pA$_{RMS}$. This is much smaller than the required 1.25 nA, so the noise of the VI converter is negligible.

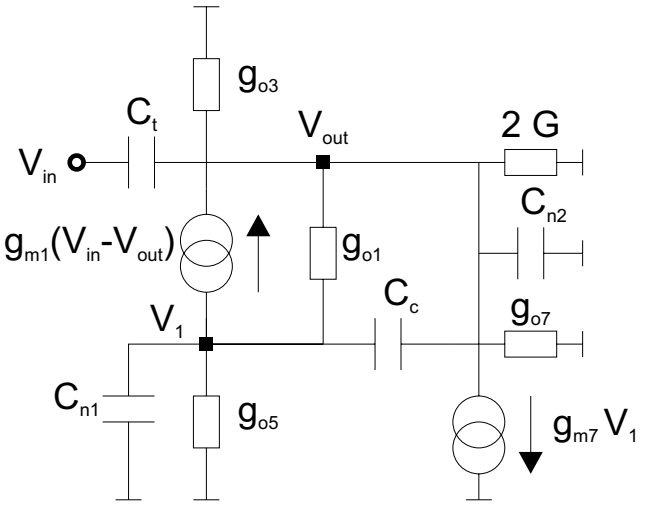

Figure 3.22. Half circuit of the input stage of the VI converter (small signal approximation).

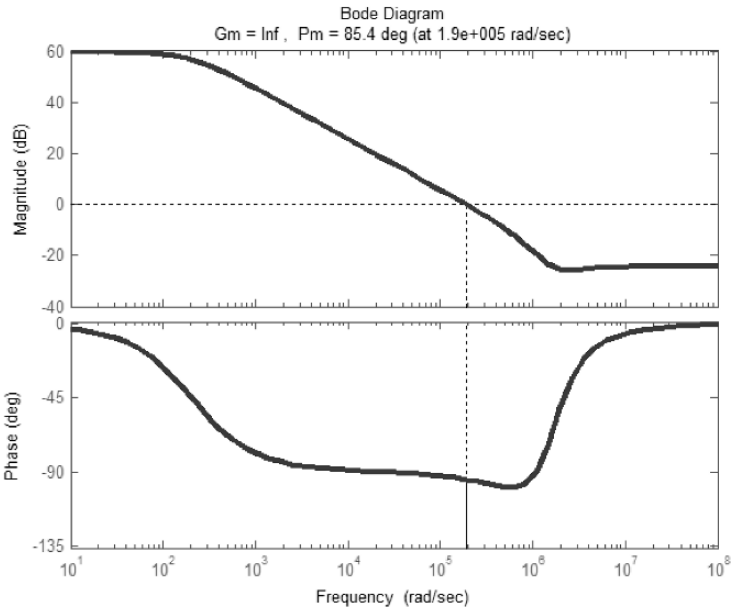

Figure 3.23. Bodeplot of the equivalent open loop transferfunction of the VI converter ($C_1 = C_2 = 10$ pF).

C. Current DAC

Fig. 3.24 shows the current DAC, which uses a cascode output stage and a break-before-make timing scheme. This break-before-make timing scheme consists

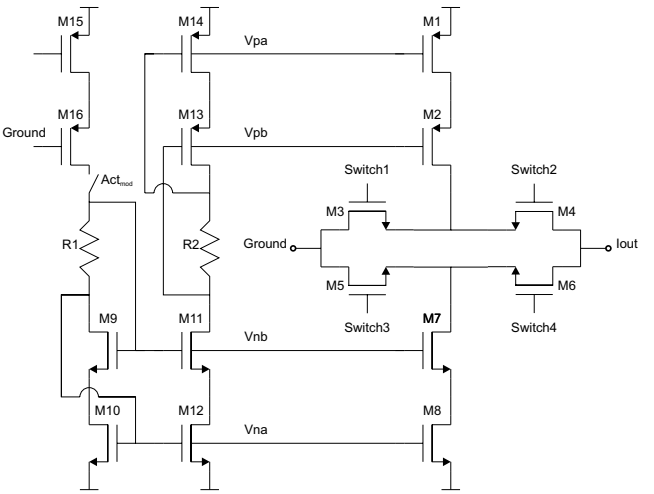

Figure 3.24. The current DAC.

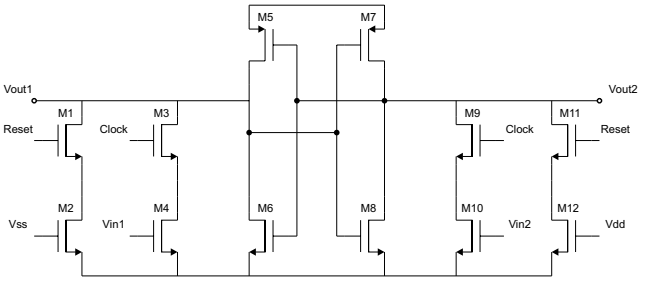

Figure 3.25. Ratioed SR latch with reset and clock switches.

of two SR latches (Fig. 3.25). When the outputs of the quantizer (Q and $Q\_$) change, the latches first open the inactive switches and thereafter they close the active switches. This ensures that at all times the switched current source has a high output impedance. The simulated noise output current during one modulator period ($\approx 8\mu$s) equals 100 pA$_{RMS}$ (=$(I_{ref+,noise} + I_{ref-,noise})$/2). This is much smaller than the required 1.25 nA, so the noise of the current DAC is negligible.

D. Integrator

The integrator uses a two-stage op-amp to achieve a high DC gain (Fig. 3.26). This limits the integrator leakage. After every transition, a residual voltage

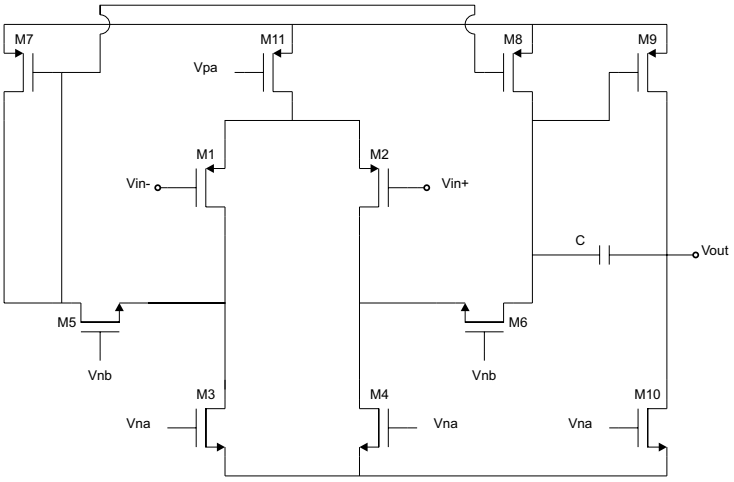

Figure 3.26. The integrator op-amp.

swing ΔV_r occurs at the inverting input of the integrator (Fig. 3.27).

$$\Delta V_r \approx \frac{2I_{ref}}{2\pi GBWC_{int}} \tag{3.27}$$

This results in a charge injection imbalance,

$$Q_{imbalance} \approx (C_{pDAC+} - C_{pDAC-}) \frac{2I_{ref}}{2\pi GBWC_{int}} \tag{3.28}$$

where C_{pDAC+} and C_{pDAC-} are the parasitic capacitors of the DAC in the positive respectively negative state. The integrator has a GBW = 250 kHz, C_{int} = 10 pF and I_{ref} = 125 nA to reduce this charge injection imbalance. The phase margin of the integrator op-amp equals 72 deg.

E. Comparator

Fig. 3.28 shows a regenerative comparator, which is used as a quantizer [Yin92]. This discrete time comparator combines a fast response with low power consumption. The comparator consists of a differential input pair (M_2/M_3), a top and bottom regeneration loop (M_{11}/M_{12} and M_4/M_5) with transfer transistors (M_6/M_7) and pre-charge transistors (M_9/M_{10}) and a switch for resetting (M_8). The comparator operates in three phases: the reset phase, the bottom and top regeneration phases. Φ_{latch} is high and Φ_{reg} is low in the reset phase. This disconnects and resets the bottom and top regeneration latches. The differential pair injects a differential current, proportional to the comparator input voltage difference, into the bottom regeneration loop and generates a voltage difference

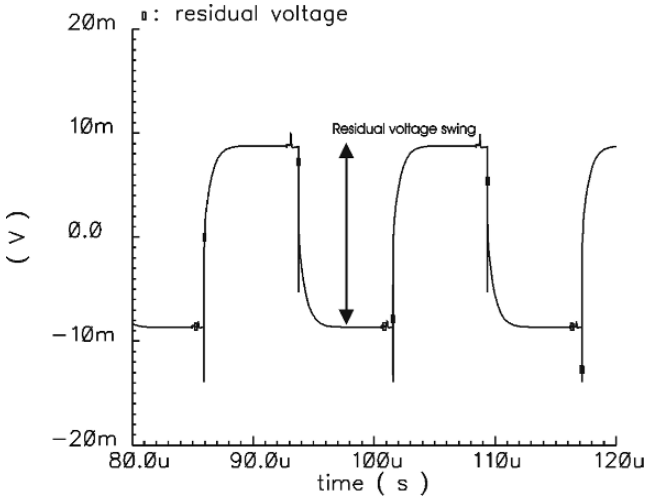

Figure 3.27. The residual voltage during a DAC transition (NRZ mode).

over M_8. This voltage will act as the initial imbalance for the regeneration. When Φ_{latch} goes down, the imbalance is regenerated by the bottom regeneration loop (bottom regeneration phase). After Φ_{reg} rises, the bottom and the top regeneration loops are connected and they both start to regenerate the imbalance (top regeneration phase).

The offset of this comparator is determined by the mismatch between the input pair and the bottom regeneration loop. The mismatches in the top regeneration loop and the transfer switches can be neglected, since the imbalance is already significantly larger at the start of the top regeneration phase. The implemented comparator has a 3 σ offset of approximately 12 mV. This effect is negligible in our $\Sigma\Delta$ modulator.

A non-overlapping clock generator creates the clocks for the comparator (Fig. 3.28). The clock generation circuit uses two different delay cells: delay cell 1 implements a large delay between 200 ns and 400 ns, dependent on the supply voltage and process tolerances, whereas delay cell 2 gives a delay of a few ns. Both delay cells are placed in the feedback path. Hence, the delays

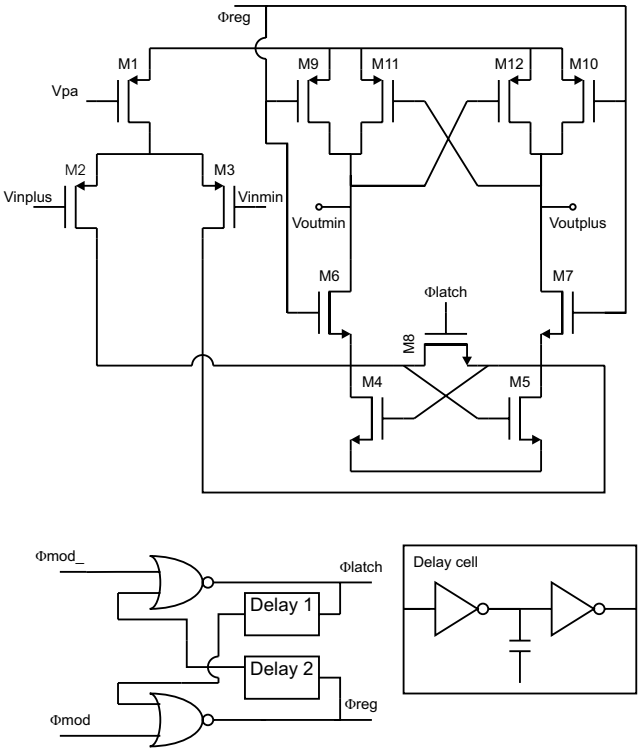

Figure 3.28. The regenerative comparator with clock generation circuit.

only effect the start of the reset and top regeneration phases (Φ_{latch} and Φ_{reg} become high), but they have no impact on the exact timing of the quantizer decision phase (Φ_{reg} goes down). Consequently, the operation of the quantizer is immune to power supply variations and process tolerances.

F. Performance

A decimation counter is used at the output of the bitstream to obtain a full digital code. The conversion time of the modulator is programmable between 256, 512 and 1024 clock cycles. So, the resolution can be varied between 8, 9 and 10 bits.

The ADC performance is measured on the final GSIC circuit (section 6). Figs. 3.29, 3.30, 3.31 and 3.32 compare the measured Integral and Differential Non-Linearity (DNL and INL) of the proposed RZ modulator with a NRZ version for a modulator clock of 128 kHz and a conversion time of 8 ms (=1024 clock cycles). Both the RZ and NRZ modulator achieve the specified resolution of 10 bits (DNL and INL are smaller than 0.5 LSB). The NRZ modulator has a larger DNL near midrange. This is caused by charge injection imbalance.

3.6 Bandgap reference, bias system and buffered reference voltage

The bias and reference system of the sensor interface consists of a bandgap reference, a reference current, bias branches for the main oscillator, modulator, VI converter, SC amplifier and C-V converters and a buffered reference voltage for the C-V converters.

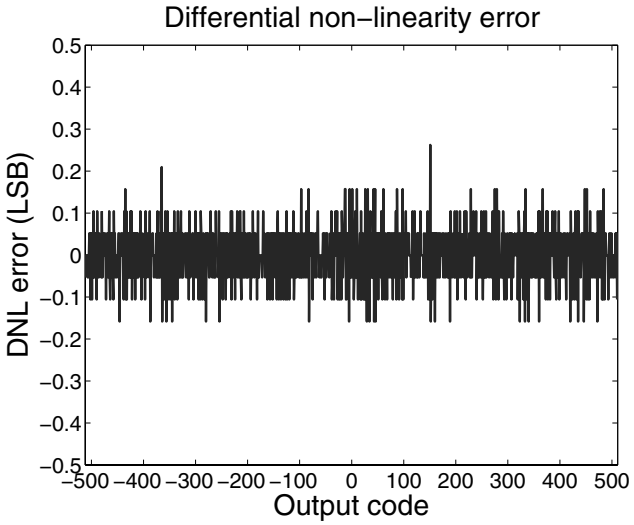

Figure 3.29. The measured differential non-linearity of the RZ modulator (10-bit mode).

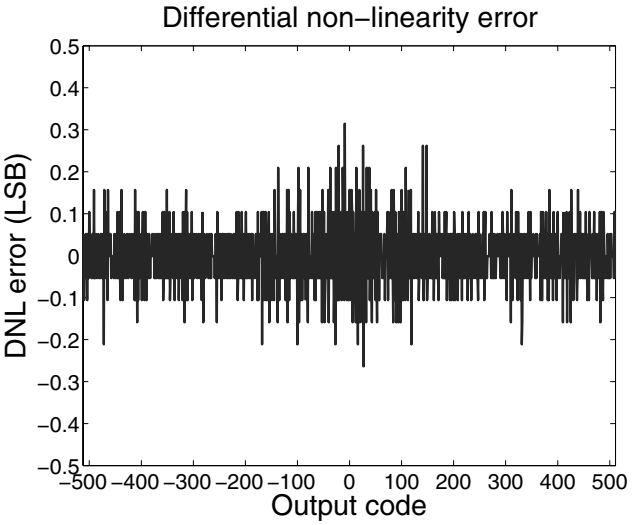

Figure 3.30. The measured differential non-linearity of the NRZ modulator (10-bit mode).

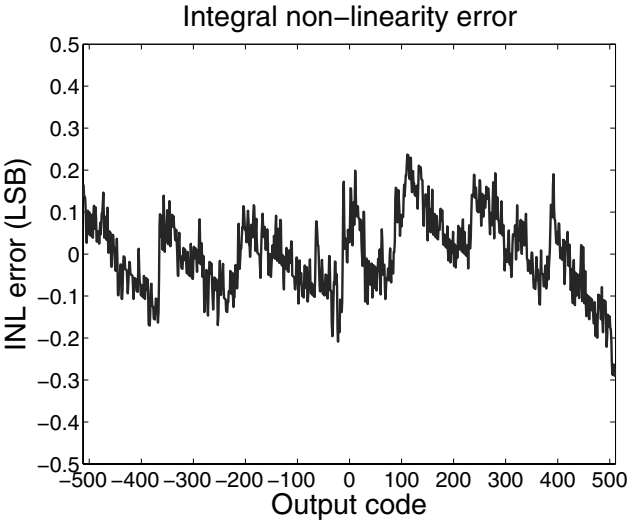

Figure 3.31. The measured integral non-linearity of the RZ modulator (10-bit mode).

A. Bandgap reference and bias system

Fig. 3.33 shows the bandgap reference and bias system. The bandgap reference circuit creates a voltage, which is independent of the power supply voltage and the temperature. The bandgap reference circuit adds a Proportional To Absolute Temperature (PTAT) voltage to the base emittor voltage, V_{be}, of the bipolar transistor Q_3. This results in a temperature stable bandgap voltage, V_{bg}.

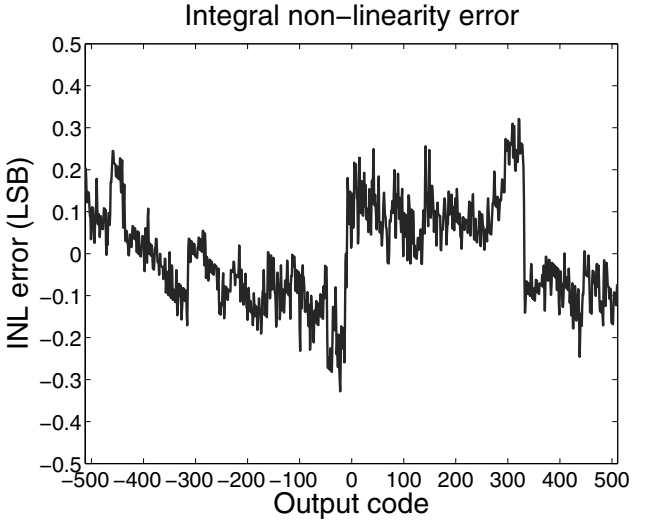

Figure 3.32. The measured integral non-linearity of the NRZ modulator (10-bit mode).

Vertical bipolar transistors, implemented in CMOS technology, have well known temperature characteristics and show almost no dependency on process parameters [Wan00]. The base emittor voltage, V_{be}, can be written as [Mei86, Bak00]:

$$V_{be} = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right) \tag{3.29}$$

where I_s is the saturation current and I_C the collector current. The saturation current I_s strongly depends on the temperature, according to the equation:

$$I_s = CT^{\eta} \exp\left(\frac{-qV_{g0}}{kT}\right) \tag{3.30}$$

where V_{g0} is the extrapolated bandgap voltage at 0 K and C and η are constants. Taking this into account, we can write equation 3.29 as

$$V_{be} = V_{g0} + \frac{kT}{q} \ln\frac{I_C}{CT^{\eta}} \tag{3.31}$$

Because $I_c/CT^{\eta} < 1$, the value of the ln function is negative, which results in a negative temperature coefficient for V_{be}. The collector current I_C is proportional to the absolute temperature (tempco K_{IC}) in the chosen bandgap circuit. So, we can write equation 3.31 as:

$$V_{be} = V_{g0} + \frac{kT}{q} \ln\frac{K_{IC}T}{CT^{\eta}} \tag{3.32}$$

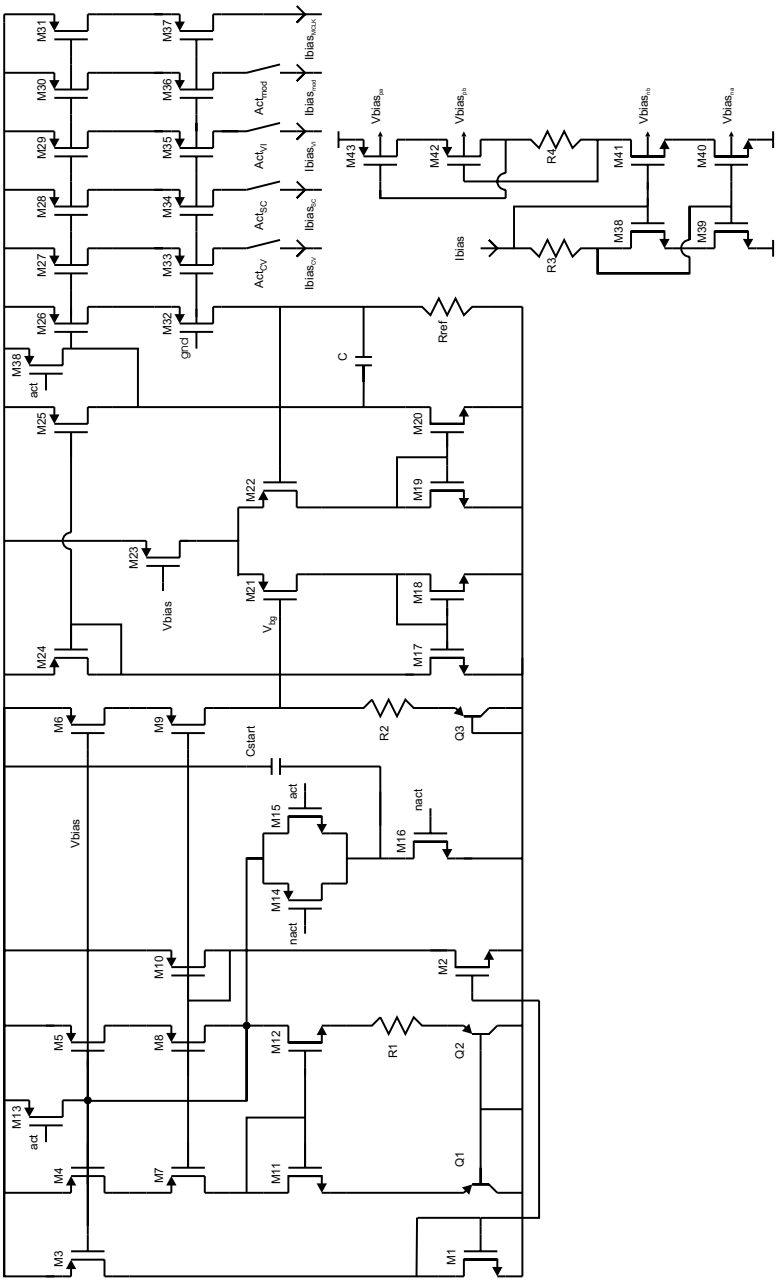

Figure 3.33. Bandgap reference and bias system.

With the base emitter voltage, $V_{be}(T_r)$, at the reference temperature T_r, we can rewrite this equation as

$$V_{be} = V_{g0}\left(1 - \frac{T}{T_r}\right) + \frac{T}{T_r}V_{be}(T_r) + \frac{kT}{q}(\eta - 1)\ln\frac{T}{T_r} \tag{3.33}$$

Equation 3.33 can be written as the sum of a constant term $(V_{g0'})$, a linear term (λT) and higher order terms $(O(T^2))$:

$$V_{be}(T) = V_{g0'} - \lambda T + O(T^2) \tag{3.34}$$

where

$$V_{g0'} = V_{g0} + (\eta - 1)\frac{kT_r}{q} \tag{3.35}$$

$$\lambda = \frac{1}{T_r}V_{g0'} - V_{be}(T_r) \tag{3.36}$$

$$O(T^2) = (\eta - 1)\frac{k}{q}\left(T - T_r + T\ln\frac{T_r}{T}\right) \tag{3.37}$$

The cascode mirrors (M_4/M_7, M_5/M_8) provide the same current through the bipolar transistors Q_1 and Q_2. Both transistors are implemented with a ratio of 1:n (Q_1= 1 element, Q_2= n elements). Hence, the voltage difference over the resistor R_1 equals

$$V_{be1} - V_{be2} = \frac{kT}{q}\ln n \tag{3.38}$$

The bias current through R_1 is proportional to the absolute temperature. This current is mirrored by the transistors M_6/M_9, which results in a PTAT voltage

$$V_{ptat} = \frac{R_2}{R_1}\frac{kT}{q}\ln n \tag{3.39}$$

This PTAT voltage compensates the negative tempco of the Q_3 base emitter voltage for $n = 10$ and $R_2/R_1 = 8$. The resistor R_1 has a nominal value of 125 kΩ. This sets the bias current in the bandgap circuit to 500 nA (300 K). Hence, the circuit performs an adequate start-up behavior (a few tens of μs) and reduces the low-level injection effects [Wan00] in the bipolar transistors. The circuit provides a bandgap voltage V_{bg} of 1.135 V, with a variation of 0.3 % in the specified temperature range from -40 °C to 85 °C.

A buffer op-amp, with load resistor R_{ref}, converts the bandgap voltage into a reference current. The buffer op-amp uses a symmetrical input core to enhance the Power Supply Rejection Ratio (PSRR) and to eliminate the systematic offset. A Miller compensation capacitor, C, is added to obtain an overdamped frequency response with GBW of 15 kHz and a phase margin of 77 deg. The resistor R_{ref} is placed in close proximity of the resistor R from the

voltage-to-current converter (common centroid layout). So, the operation of the system will be in first order independent of the temperature. The cascodes in the reference circuit make the bias currents immune to power supply variations. The bias currents are distributed from the central reference circuit to the slave bias circuits. Hence, the bias voltages for the n- and p-type (cascode) transistors are generated locally for each building block. This reduces the effects of systematic mismatches between distant regions on the chip. The C-V converters (and buffered reference voltage V_{ref}), SC amplifier, VI converter and modulator can be switched off separately, by opening a switch in their bias branches. A switch in the start-up circuit of the bandgap reference offers a power down option for the total analog part of the system (act = 0).

B. Buffered reference voltage

The buffered reference voltage needs to charge the sensor capacitances C_x, C'_x and C_{p1} on the rhythm of the SC interface clock (8 kHz). It is realized by converting the bias current with a feedback resistor R_f to a voltage V_{ref} above analog ground (Fig. 3.34). The two stage op-amp contains a symmetrical cascode input pair followed by a class AB output buffer with adaptive load [You98] (Fig. 3.35). The symmetrical input core reduces the systematic offset and enhances the power supply rejection. The class AB buffer is a power efficient solution to provide high peak currents at the output load. After Φ_1 turns on, the transistor M_{19} leaves the saturation region ($V_{ds} < V_{gs} - V_T$). Hence, node A becomes high impedant and an increased current flows from transistor M_{20} to the sensor capacitances. When the output voltage approaches its final value, transistor M_{19} returns to saturation region and the adaptive load becomes low impedant. Hence, the current consumption decreases to a low quiescent level.

The implemented class AB buffer consumes 650 nA in the input stage (bias transistor M_3), 250 nA in M_{17}/M_{13} and 75 nA in M_{19}/M_{15}. With these settings, the output (M_{20}/M_{16}) has a quiescent current of 2.5 μA. The com-

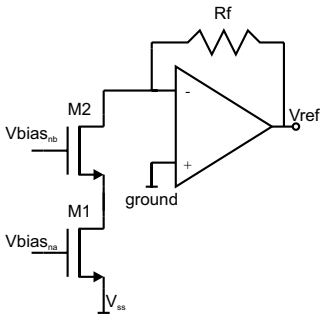

Figure 3.34. Buffered reference voltage.

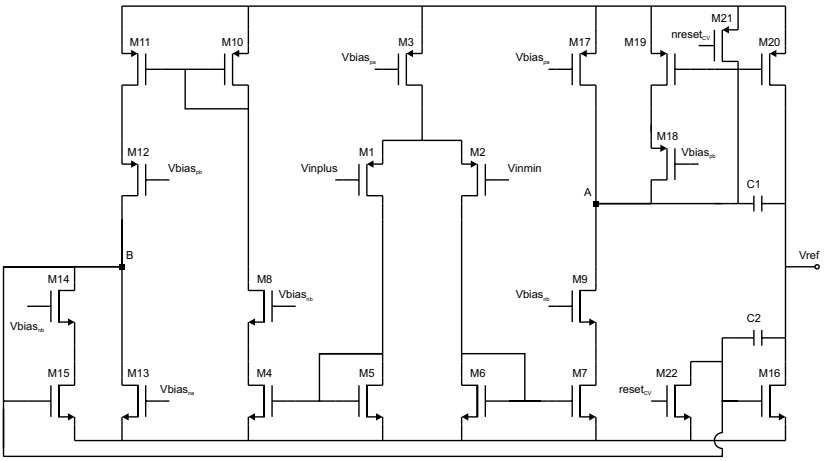

Figure 3.35. Buffer op-amp with class AB output stage.

pensation capacitors, C_1 and C_2 equal 7 pF. The buffered reference voltage has a stable transient response (Φ_2 to Φ_1) with an overshoot of 2% (without oscillation) and a 0.1 % settling time of 50 μs for the maximum load capacitor of 100 pF (worst case). This design is compared with conventional class A buffers and it is proven to be five times more efficient in power consumption.

3.7 Main clock, clock generation circuits and LF clock

The clocks for the C-V converters, SC amplifier and modulator are derived from the main oscillator. The main clock and the analog read-out electronics are switched off during OFF-state ($act = 0$). So, only the 8 kHz LF clock is running (very low power consumption). Timers are used to set the duration of the ON and OFF state. Hence, we have a system with programmable duty cycle operation and a very small OFF-state current consumption of approximately 0.5 μA. The clock frequencies are also programmable to cope with technology variations.

A. Main clock

The main clock of the GSIC is a 512 kHz square wave relaxation oscillator [Wak89]. The oscillator operates as follows (Fig. 3.36). If we assume that the SR latch is in the state $V_{out1} = 0$ and $V_{out2} = 1$, the capacitor C_1 is shorted to analog ground and the current I_{charge} is loading the capacitor C_2. When the potential at node A becomes higher than V_{turn}, the state of the SR latch is changed and the capacitor C_1 is loaded. Hence, we obtain a power supply independent oscillation frequency, which equals $I_{charge}/(2CV_{turn})$.

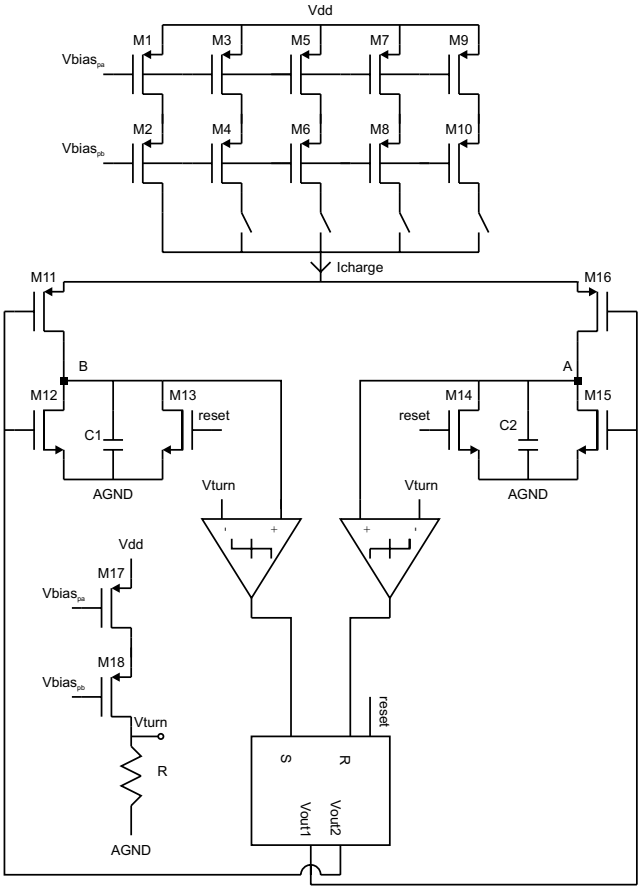

Figure 3.36. Square wave relaxation oscillator.

The capacitor C, the turning potential V_{turn} and the charge current I_{charge} are chosen to reduce the clock jitter $T_{j,\sigma}$ with respect to the modulator period ($T_{mod} \approx 8\mu$s), so that

$$\frac{4}{\sqrt{3}} \frac{T_{j,\sigma}}{T_{mod}} < \frac{1}{\sqrt{1024}} \tag{3.40}$$

Hence, we attain enough accuracy for the modulator.

The clock jitter stems from the noise current in the oscillator capacitor and the input noise voltages of the comparators. The noise current is integrated on the capacitor C during one clock period, so its effect is negligible compared to the broadband input noise of the comparator. Hence, we can approximate the

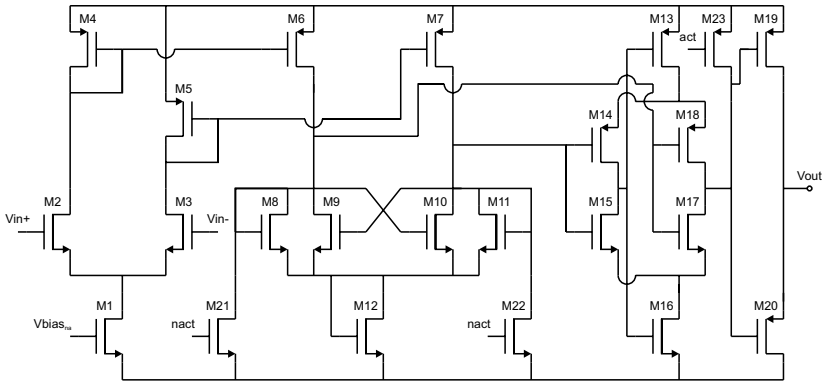

Figure 3.37. Fast continuous time comparator with low quiescent current.

clock jitter by [Abi83]

$$T_{j,\sigma} = T_{osc}\frac{\alpha\sqrt{6}}{2}\frac{V_n}{V} \tag{3.41}$$

where T_{osc} is the oscillator period ($\approx 2\mu$s), α is a constant, V_n is the equivalent rms noise input voltage of the comparator and V is the triangle wave peak-to-peak voltage. The clock jitter equals 2.9 ns in the implemented oscillator, which satisfies equation 3.40.

The oscillator uses fast continuous time comparators with low quiescent current (Fig. 3.37) [Bak98]. The first stage is a low gain, high bandwidth preamplifier that drives a latch. The preamplifier uses small size transistors that are biased in moderate inversion region. Hence, a high bandwidth is realized with a minimum power consumption. The output mirrors of the preamplifier are realized with a ratio M_4/M_6 of 1/4 to further reduce the current of the input stage. The latch performs the decision. Its transistors (M_8, M_9, M_{10} and M_{11}) have equal size to reduce the comparator hysteresis. The latch outputs are used to drive a self-biased differential amplifier. During the transition, the current in the self-biased differential amplifier is boosted to perform a fast behavior. After the decision is made, it falls back to a very low quiescent current. The output of the self-biased differential amplifier drives a push-pull output driver. The implemented comparator causes an oscillator propagation delay of 40 ns for a current consumption of 2.5 μA.

B. LF clock

The 8 kHz LF clock is used for the timing between subsequent samples. It is the only part of the system, which operates continuously. The LF clock is biased when the power supply V_{DD} is put on [Kha03]. After the GSIC is

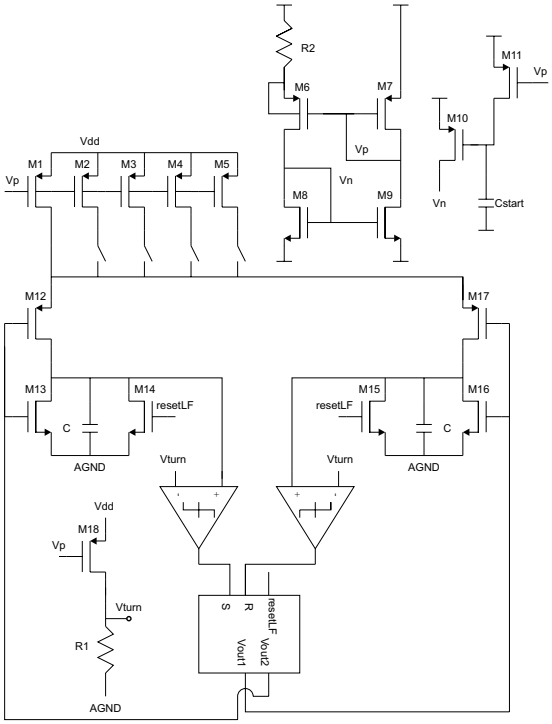

Figure 3.38. LF oscillator with bias circuit.

programmed, $resetLF$ becomes low and the LF clock and sample timer start operating (operational flow, section 3.2). The LF clock is implemented as a relaxation oscillator with a bias circuit (Fig. 3.38). The oscillator uses simple two-stage open-loop comparators.

4. Configuration settings

The GSIC is equipped with many programming settings to offer an interface to a broad range of capacitive sensor applications. The capacitive sensor interface has two modes of operation. The first mode is for single sensor operation with on chip reference capacitor, where the reference capacitor, C_{ref2}, needs to be programmed to approximate the base capacitance of the sensor, C_0. The other mode is for differential sensor operation, where the on chip reference capacitor, C_{ref1} (or C_{ref2}), is programmed to compensate for the offset between C_x and C_x'. The amplification factor, A_{SC}, of the SC amplifier and the feedback capacitor, C_f, of the C-V converters need to be programmed for optimal accuracy of the interface. The sample period is 6-bit programmable between 8 ms and 512 ms and the ADC accuracy is selectable between 8, 9

or 10 bits for a conversion time of 2, 4 or 8 ms. Hence, the averaged power consumption is strongly related to the accuracy and speed requirements of the selected application. Both the LF clock and main oscillator are programmable to cope with technology variations.

Table 3.1 shows the configuration addresses, their databits and a description of their functions. A databit with symbol X is not used and has to be interpreted as a don't care bit. A databit with symbol T is reserved for test purposes. The addresses 9 to 15 are unused. So, the modular architecture can be expanded with extra configurable blocks, such as a temperature sensor or a (bio)potential instrumentation amplifier. Hence, one can make a system that can interface with several types of sensors in different time intervals. This will result in applications such as a personal health assistant, which monitors the blood pressure, body temperature and heart rate.

Table 3.1. Description of the configuration memory of the Generic Sensor Interface Chip.

	D0	*D1*	*D2*	*D3*	*D4*	*D5*	*D6*	*D7*	*D8*	*D9*
0[a]	X	X	X	X	X	X	T	T	Mod_1	Mod_0
1[b]	X	X	X	X	X	X	LF_3	LF_2	LF_1	LF_0
2[c]	X	X	X	X	X	X	CL_3	CL_2	CL_1	CL_0
3[d]	X	X	S_5	S_4	S_3	S_2	S_1	S_0	AD_1	AD_0
4[e]	X	X	C_{r1_7}	C_{r1_6}	C_{r1_5}	C_{r1_4}	C_{r1_3}	C_{r1_2}	C_{r1_1}	C_{r1_0}
5[f]	X	X	C_{r2_7}	C_{r2_6}	C_{r2_5}	C_{r2_4}	C_{r2_3}	C_{r2_2}	C_{r2_1}	C_{r2_0}
6[g]	X	X	X	X	X	X	C_{f3}	C_{f2}	C_{f1}	C_{f0}
7[h]	X	X	X	X	A_{SC5}	A_{SC4}	A_{SC3}	A_{SC2}	A_{SC1}	A_{SC0}
8[i]	X	X	Act_{CV}	Act_{SC}	Act_{VI}	Act_{mod}	T	T	T	T
9	X	X	X	X	X	X	X	X	X	X
10	X	X	X	X	X	X	X	X	X	X
11	X	X	X	X	X	X	X	X	X	X
12	X	X	X	X	X	X	X	X	X	X
13	X	X	X	X	X	X	X	X	X	X
14	X	X	X	X	X	X	X	X	X	X
15	X	X	X	X	X	X	X	X	X	X

[a] The Mod_1 and Mod_0 bits select the interface mode (single or differential).
[b] The $LF_3 \ldots LF_0$ bits select the LF clock frequency.
[c] The $CL_3 \ldots CL_0$ bits select the main oscillator frequency.
[d] The sample period is selected by $S_5 \ldots S_0$. The LF clock, sample timer and analog front-end are off, if these bits are low ($resetLF = 1$, $Act = 0$, $Reset = 1$). AD_1 and AD_0 set the conversion resolution (8, 9 or 10 bit). The analog front-end is always off, if both bits are low ($Act = 0$, $Reset = 1$).
[e] $C_{r1\_7} \ldots C_{r1\_0}$ set the reference capacitor C_{ref1}.
[f] $C_{r2\_7} \ldots C_{r2\_0}$ set the reference capacitor C_{ref2}.
[g] $C_{f3} \ldots C_{f0}$ set the feedback capacitor C_f.
[h] $A_{SC5} \ldots A_{SC0}$ set the SC amplification factor A_{SC}.
[i] Act_{CV}, Act_{SC}, Act_{VI}, Act_{mod} offer a power down option for the C-V converters, SC amplifier, VI converter and modulator.

Furthermore, a computer algorithm is developed, which estimates the optimal C_{ref}, C_f and A_{SC} for each application. This algorithm is expressed as an optimization problem, which minimizes the total error. The objective function considers the full-scale loss, leakage error, settling error, noise and ADC accuracy. The algorithm is presented in chapter 4. The obtained values for C_{ref}, C_f and A_{SC} are the starting points of a calibration cycle. During this procedure, the settings can be adjusted in order to cope with the technology variations of the sensors and the interface chip. Furthermore, it is possible to change the configuration settings after the system is operational. Hence, we can adapt the system to changes in the environment (e.g. available supply energy) or drift phenomena.

5. Noise

The mechanical noise of the sensor, the electrical noise of the interface and the quantization noise of the ADC contribute to the total noise in the system. The electrical noise of the SC interface is studied in this section. In 5.1, a methodology is presented to estimate the noise in SC circuits in a simple and accurate manner. Subsection 5.2 presents the noise calculations in the C-V converter. The global noise performance of the SC interface is studied in 5.3.

5.1 Bennet model

The noise of the SC interface (C-V converters and SC amplifier) is calculated with the Bennet model [Ben48]. This model states that the noise can be described as an infinite sum of discrete sinusoidal components. These components have a different frequency, an equal amplitude and a random phase, which is uniformly distributed in the interval $[-\pi, \pi]$. The sum of all the Bennet components equals the total noise power, which is given by the product of the Power Spectral Density (PSD) and the bandwidth.

With the Bennet model, we can calculate the noise as follows:

- Each noise source is presented by an equivalent sinusoidal source with amplitude $\hat{u}_n$, random phase ϕ and pulsation ω. The corresponding phasor equals $\hat{u}_n \exp(j\phi)$.

- Thereafter, we compute the output phasor, U_{out}, at time t_2 (i.e. the end of the signal phase).

- The power spectrum of the noise at t_2, $S_{out,t2}(\omega)$, is given by:

$$S_{out,t2}(\omega)d\omega = \frac{1}{2\pi}\left(\int_{-\pi}^{\pi} \frac{|U_{out}|^2}{\hat{u}_n^2} d\phi\right) \frac{d\omega}{\pi} S_{un}(f) \qquad (3.42)$$

where S_{un} is the power spectrum of the noise source. With $S_{out,t2}$ as a function of the frequency, equation 3.42 can be written as:

$$S_{out,t2}(f) = 2S_{un}\frac{1}{2\pi}\int_{-\pi}^{\pi} u_{out,g}^2 d\phi \tag{3.43}$$

where $u_{out,g}$ is the normalized output amplitude at t_2

$$u_{out,g} = \frac{|U_{out}|}{\hat{u}_n} \tag{3.44}$$

- The output signal is sampled by the following SC stage. This process can be modelled by an ideal Sample and Hold operation [Fis82]. Hence, the output spectrum after sample and hold, $S_{out,h}(f)$, is given by:

$$S_{out,h}(f) = S_{out,t2}^d\left(\exp\left(\frac{j2\pi f}{f_s}\right)\right)\frac{1}{f^2}\mathrm{sinc}^2\left(\frac{f}{f_s}\right) \tag{3.45}$$

where the discrete power spectrum $S_{out,t2}^d$ is given by:

$$S_{out,t2}^d\left(\exp\left(\frac{j2\pi f}{f_s}\right)\right) = f_s^2\sum_{k=-\infty}^{\infty} S_{out,t2}(2\pi f + 2\pi k f_s) \tag{3.46}$$

This equation expresses the noise aliasing caused by the sampling operation. The noise has a finite bandwidth, BW_{noise}. If we take this in consideration, we can approximate the infinite sum by

$$\begin{aligned}\sum_{k=-\infty}^{\infty} S_{out,t2}(2\pi f + 2\pi k f_s) &\approx \sum_{k=-N}^{N} S_{out,t2}(2\pi f + 2\pi k f_s)\\ N &= 10\mathrm{round}\left(\frac{BW_{noise}}{f_s}\right)\end{aligned} \tag{3.47}$$

- The RMS-value of the sampled noise at the output, σ_{noise}, is then given by:

$$\sigma_{noise} = \sqrt{\int_{-f_s/2}^{f_s/2} S_{out,h}(f)df} = \sqrt{2\int_{0}^{f_s/2} S_{out,h}(f)df} \tag{3.48}$$

5.2 Noise calculations

The noise in the C-V converters and the SC amplifier contains contributions of the switches and the OTA's (thermal and 1/f noise). All these components

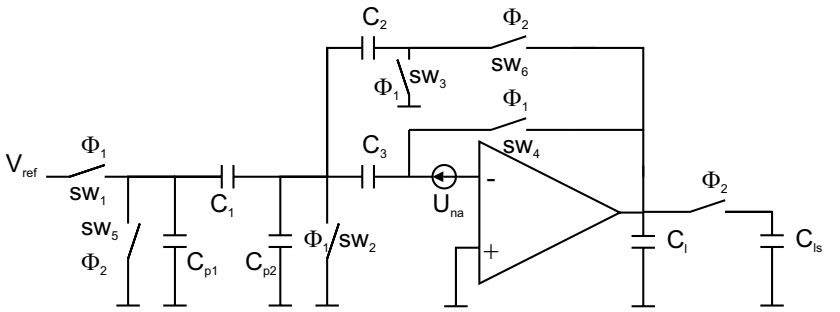

Figure 3.39. C-V converter with switches, sw_1 to sw_6, and OTA noise source, S_{una}.

are uncorrelated. So, the total noise can be found as a squared superposition of their RMS values. The effects of the individual noise sources are estimated with the Bennet model. Hereafter, only the noise calculations of the C-V converter are presented. Similar computations have been made for the SC amplifier.

The noise in the C-V converter is caused by the input referred noise, U_{na}, of the OTA and the thermal noise of the switches (Fig. 3.39). The input referred noise spectral density of the OTA, S_{una}, equals:

$$S_{una}(f) = N_{ex}\frac{8kT}{3g_m} + \frac{K_F}{f} \tag{3.49}$$

where N_{ex} is the noise excess factor [San94] and K_F is the 1/f noise factor, which depends on the technology, the type and the size of the transistors. The switches can be replaced by their ON-resistance, R_{on}, in series with a white noise source

$$S_{unsw}(f) = 4kTR_{on} \tag{3.50}$$

A. Noise of the OTA

During the sampling phase Φ_1, the noise of the OTA, U_{na}, is sampled on capacitor C_3 (Fig. 3.40). At the end of the sampling phase, t_1, this results in a

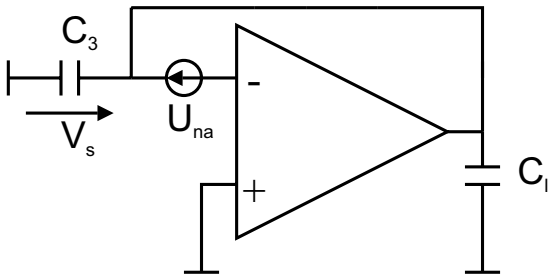

Figure 3.40. OTA noise during the sampling phase, Φ_1.

sampled voltage, V_s, given by:

$$V_s = \exp(j\omega t_1) U_{na} \left(\frac{1}{\frac{j\omega}{2\pi GBW_1} + \frac{1}{A}} \right) \left(1 + \frac{1}{\frac{j\omega}{2\pi GBW_1} + \frac{1}{A}} \right)^{-1} \tag{3.51}$$

where A is the DC gain of the OTA and GBW_1 is the gain bandwidth of the OTA during the sampling phase.

$$GBW_1 = GBW \frac{C_l}{C_l + C_3} \tag{3.52}$$

The sampled and the instantaneous noise are subtracted during the signal phase Φ_2 (Fig. 3.41). Hence, the equivalent noise source at t_2 equals

$$V_{eq} = U_{na} \exp(j\omega t_2) - V_s \tag{3.53}$$

So, the phasor V equals

$$V = \frac{C_2 V_{eq}}{(C_1 + C_2 + C_{p2}) \left(\frac{j\omega}{2\pi GBW_2} + \frac{1}{A} \right) + C_2} \tag{3.54}$$

where GBW_2 is the gain bandwidth of the OTA during the signal phase.

$$GBW_2 = GBW \frac{C_l}{C_l + C_{ls} + \frac{C_2(C_1 + C_{p2})}{C_2 + C_1 + C_{p2}}} \tag{3.55}$$

The phasor of the output voltage, U_{out}, is then given by:

$$U_{out} = V - V \frac{C_1 + C_{p2}}{C_2} \tag{3.56}$$

The obtained U_{out} is used to calculate $u_{out,g}$ (3.44). Thereafter, the output rms noise, σ_{noise}, is computed according to the procedure from subsection 5.1 (3.43-3.48).

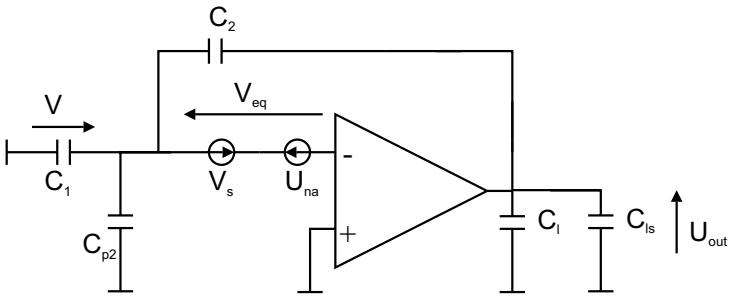

Figure 3.41. OTA noise during the signal phase, Φ_2.

The noise at the output contains contributions of the thermal and 1/f noise components of the OTA. The thermal component causes a noise voltage, σ_{noise}, which

- is independent of the transconductance g_m. The bandwidth of the C-V converter is proportional to the transconductance, g_m. So, the noise aliasing is also proportional to g_m. On the other hand, the OTA noise input spectrum decreases with g_m (3.49). Hence, the noise voltage is not effected by g_m.
- decreases with a higher load capacitor, C_l.
- is proportional to $\sqrt{C_{p2}/C_1}$.

The 1/f noise is adequately suppressed by the CDS operation.

B. Noise of switch 1

At the end of Φ_2, the thermal noise of switch 1 creates an indirect and a direct noise component at the output. The indirect component stems from the sampled noise (at the end of Φ_1) on the series parallel combination of C_1, C_{p2}, C_2 and C_3. During the signal phase, these noise charges are transferred to the feedback capacitor C_f. The direct component is caused by the thermal noise during Φ_2. This component is filtered by the low pass operation of the OTA, whereas the indirect component is only limited by the $1/(2\pi R_{ON}C)$ cut-off behavior. Since the latter frequency is much higher, we can neglect the direct component.

The sampled (indirect) noise component is evaluated in Fig. 3.42. After solving this network, we obtain the output phasor (at t_2):

$$U_{out} = \frac{Q_1(\omega) - Q_p(\omega) - Q_2(\omega)}{C_2} + \frac{Q_3(\omega)}{C_3} \tag{3.57}$$

The found U_{out} is used to calculate the rms noise value, σ_{noise}. This noise value

- is independent of R_{ON}.
- is inverse proportional to $\sqrt{C_1}$ (with a constant C_{p2}/C_1).
- decreases with increasing C_{p2}/C_1.

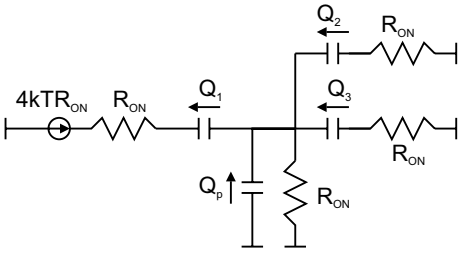

Figure 3.42. Equivalent scheme for the noise of switch 1, during Φ_1.

C. Noise of switch 2

The noise of switch 2 is also estimated by its indirect component. The solution of the network (Fig. 3.43) gives the following output phasor:

$$U_{out} = -\frac{Q_1(\omega) + Q_p(\omega) + Q_2(\omega)}{C_2} + \frac{Q_3(\omega)}{C_3} \tag{3.58}$$

The rms noise value

- is independent of R_{ON}.
- is inverse proportional to $\sqrt{C_1}$ (with a constant C_{p2}/C_1).
- increases with C_{p2}/C_1.

D. Noise of switch 3

The noise of switch 3 is estimated by its indirect component. The solution of the network (Fig. 3.44) gives the following output phasor:

$$U_{out} = \frac{Q_1(\omega) + Q_p(\omega) - Q_2(\omega)}{C_2} - \frac{Q_3(\omega)}{C_3} \tag{3.59}$$

The rms noise value

- is independent of R_{ON}.
- is inverse proportional to $\sqrt{C_1}$ (with a constant C_{p2}/C_1).
- decreases with increasing C_{p2}/C_1.

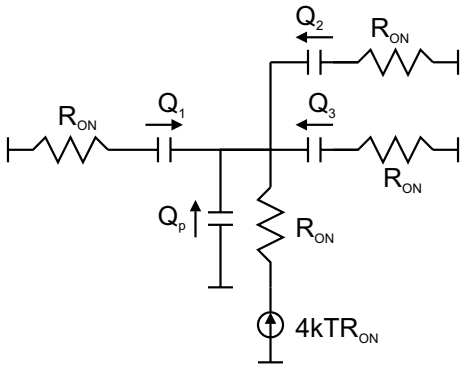

Figure 3.43. Equivalent scheme for the noise of switch 2, during Φ_1.

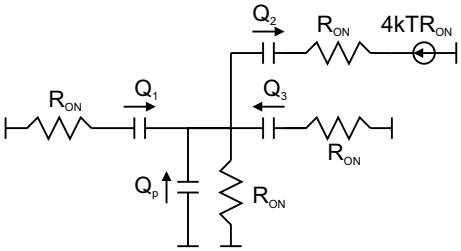

Figure 3.44. Equivalent scheme for the noise of switch 3, during Φ_1.

E. Noise of switch 4

The noise contribution of switch 4 can be approximated by the sampled $\sqrt{kT/C_3}$ noise on C_3.

F. Noise of switches 5 and 6

The noise of switches 5 and 6 has only a direct component, so it is negligible.

5.3 Effective number of bits

The noise of the sensor system depends on the application (characteristic sensor curve, parasitic capacitors, etc.) and the configuration settings of the front-end circuit. A measure for the accuracy of a sensor system has to consider both the sensor and the interface imperfections. To characterize the noise behavior of a generic system, the quantity effective number of bits is defined as follows:

Assume we have a sensor with characteristic $S(x)$, where x is a physical quantity (acceleration, pressure, humidity, ...), which varies between x_{min} and x_{max}. If one applies a sinusoidal signal between x_{min} and x_{max} at the input of the sensor, the interface will produce a fundamental harmonic $V_{out,fund,rms}$ and a disturbing component $V_{out,noise+dist,rms}$ caused by noise and distortion. The effective number of bits equals:

$$\text{Effbits} = \log_2\left(\frac{V_{out,fund,rms}}{V_{out,noise+dist,rms}}\right) - 0.2925 \tag{3.60}$$

The noise contributions of the buffered reference voltage V_{ref}, the op-amps and the switches in the C-V converters and the SC amplifier were evaluated. The sampled noise, b_{sample}, presented at the input of the ADC during one SC interface clock period (0.125 ms) is shown in Fig. 3.45. This figure gives the sampled noise as a function of α and C_0, assuming $C_{p1} = C_{p2} = 10$pF, $G_p = 0.01\mu$S and a single linear sensor characteristic:

$$C_x(x) = C_0\left(1 + \alpha\frac{x - 0.5(x_{max} + x_{min})}{x_{max} - x_{min}}\right) \tag{3.61}$$

So, only the noise contributions of the SC interface are taken into account.

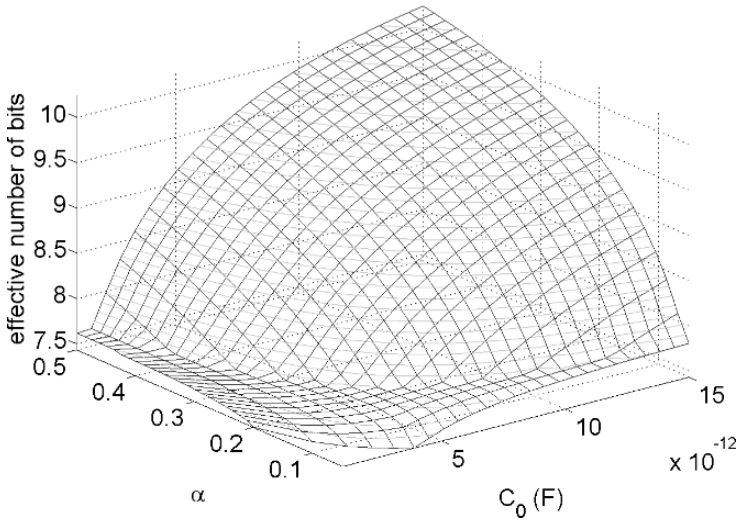

Figure 3.45. Sampled noise as a function of α and C_0.

During one measurement period, several SC interface cycles are performed. This means that the effective number of bits, b_{meas}, during one measurement equals

$$b_{meas} = b_{sample} + 0.5\log_2(N_{SC}) \tag{3.62}$$

where N_{SC} is the number of SC interface cycles during one measurement. Furthermore, the accuracy limitations by the modulator need to be considered. These quantization errors depend on the measurement time. With a conversion time between 256 and 1024 modulator periods (= 16 - 64 SC interface periods), the simulated front-end accuracy is at least 8 bits for each sensor in the specified range.

6. Experimental results

The GSIC is designed in a 0.5μm CMOS technology (AMIS) for a supply voltage between 2.7 and 3.3 V. The chip measures 3.2 mm by 2.9 mm (including the IO ring) (Fig. 3.46).

Special care has been taken to reduce the influence of the digital and higher frequency electronics on the sensitive analog read-out. For this purpose, the C-V converters are placed on the opposite side of the ADC, the main oscillator and the clock generation circuits. Furthermore, five different supplies with separate IO pads are used: a supply for the external circuits in the IO ring ($VSSE$, $VDDE$), a supply for the internal low noise transistors in the IO ring ($VSSI$, $VDDI$), a supply for the digital core cells ($VSSCO$, $VDDCO$), a supply for the guard rings ($VSSS$, $VDDS$) and an analog dual supply ($AVSS$, $AGND$,

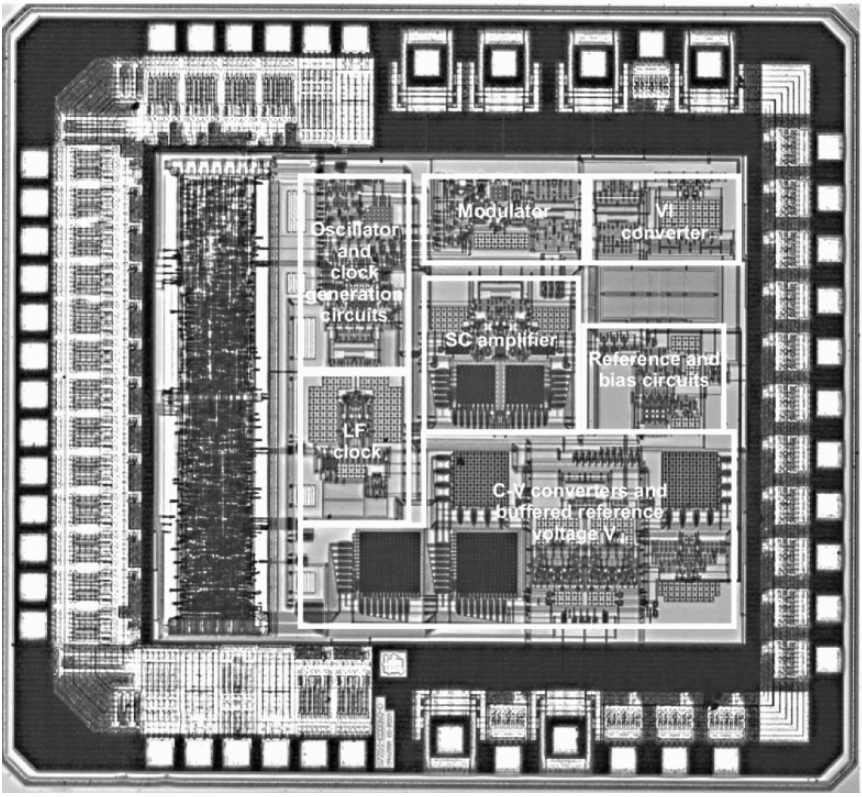

Figure 3.46. Die photograph of the Generic Sensor Interface Chip (size = 3.2 mm x 2.9 mm, including IO ring).

$AVDD$). The guard rings are placed in close proximity of the digital circuits and higher speed analog circuits. Hence, they provide a low impedance return path for the injected current pulses [Ing97]. An n-well on the ground potential $AGND$ shields the analog high ohmic poly resistors and capacitors from the substrate.

The system has a total current consumption of approximately 40μA during ON-state. Table 3.2 shows the current consumption of the analog blocks. The averaged power consumption can be tailored towards the speed and accuracy requirements of the application. Hence, the averaged current consumption is smaller than 20μA for sensor applications with small bandwidth ($<$50 Hz) and medium resolution requirements (Fig. 3.47). As an example, we consider the cases of a pressure sensor and an inclinometer application.

Table 3.2. Current consumption of the analog building blocks.

Analog building blocks	*Current (μA)*
Bandgap reference, bias system and buffered reference voltage V_{ref}	13.5
Main clock and clock generation circuits	8
C-V converters	2 x 3.5
SC amplifier	4
VI converter	1.8
Modulator	4.1
Total ON-state current	**38.4**
LF clock (runs continuously)	0.5

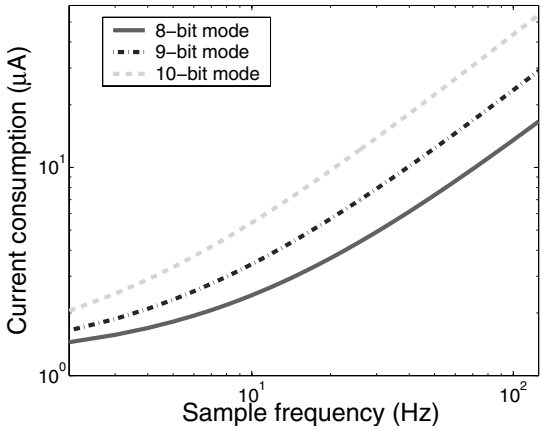

Figure 3.47. Averaged current consumption of the GSIC as a function of the sample frequency and the resolution mode.

6.1 Pressure monitoring system

In the diagnosis of urinary incontinence, one wants to observe the contraction of the bladder muscle as the bladder fills and empties. For this purpose, we use a single capacitive absolute pressure sensor (B012FB, VTI Technologies) to monitor the bladder pressure in the range of 100-130 kPa [Coo05]. This application needs a sampling frequency of 10 Hz and 8-bit accuracy. A duty cycle of 2 % can be used, which results in a measured power consumption of approximately 7.3μW (3 V supply). The test PCB contains the GSIC, the pressure sensor and a connector to a pump (Fig. 3.48). The sensor is placed in the cavity of the connector. In this way, we can apply a reliable pressure on the sensor membrane. Fig. 3.49 shows the digital output code as a function of the

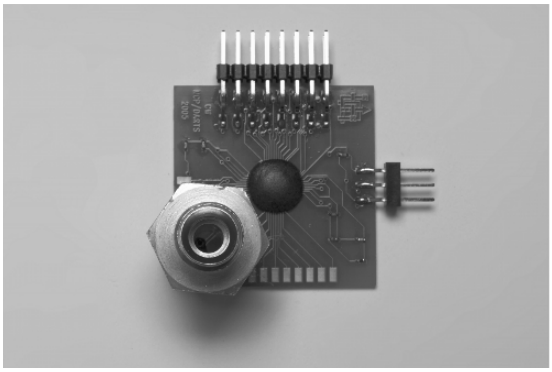

Figure 3.48. Test PCB with pressure sensor, connector and GSIC (covered with globtop coating).

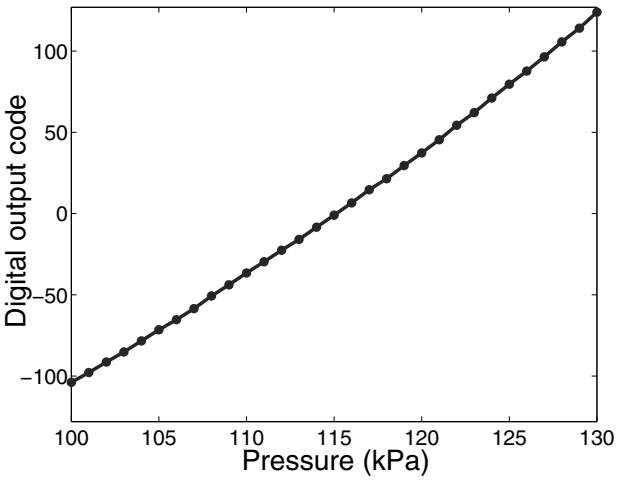

Figure 3.49. Measured digital output code as a function of the applied pressure.

applied pressure. The behavior is slightly non-linear over pressure, inherent to the performance of the sensor. The linearization is accomplished by numerical correction using a 3 points calibration on the physical sensor model (provided by the manufacturer). The remaining pressure error after this linearization is smaller than 0.1 kPa (Fig. 3.50). The repeatability of the output is, for each applied pressure, within ± 1 count. Hence, the dominant noise source is the quantization.

Furthermore the system is tested (with different settings) in the pressure range from 60 kPa to 120 kPa. For this test, we have selected a sample frequency of

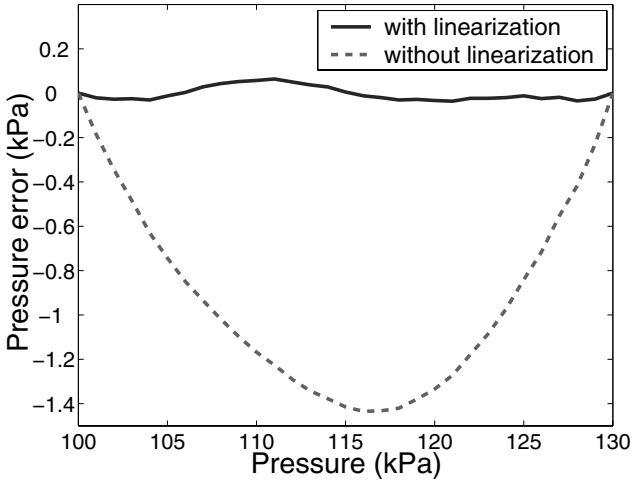

Figure 3.50. Pressure error after 3 points calibration with the sensor model.

10 Hz and 10-bit resolution. The measured power consumption equals 16.4μW (3 V supply). Fig. 3.51 shows the digital output code as a function of the applied pressure. The remaining pressure error after this linearization is smaller than 0.1 kPa (Fig. 3.52). The repeatability of the output is, for each applied pressure, within ± 1 count. Hence, the dominant noise source is the quantization.

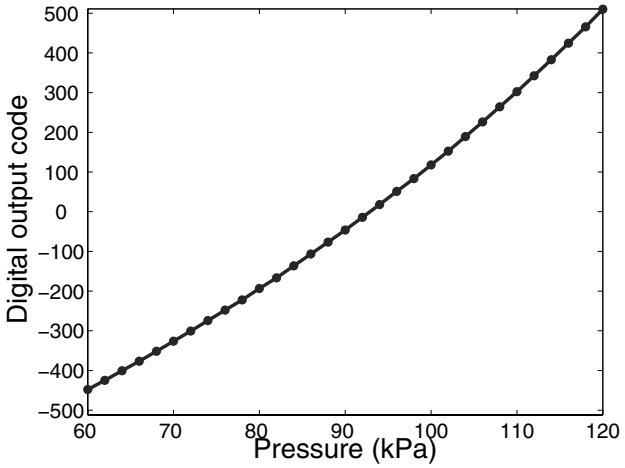

Figure 3.51. Measured digital output code as a function of the applied pressure.

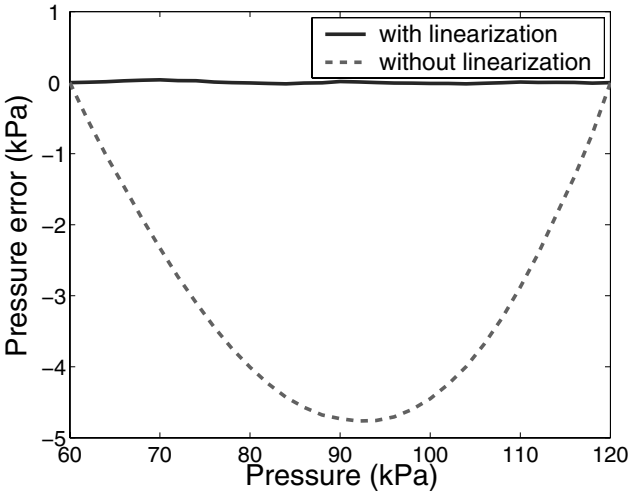

Figure 3.52. Pressure error after 3 points calibration with the sensor model.

6.2 Inclination monitoring system

The SCG10Z-G001CC low g accelerometer (VTI Technologies) is used in an inclination monitoring system. This sensor is tested with several configuration settings of the GSIC. In the first test, the functionality of the sensor system is evaluated (9-bit mode). In the second test, we have verified that the operation of the GSIC is immune to power supply variations from 2.7 V to 3.3 V. The last test shows us that the transition from 8-bit to 10-bit mode has a negligible effect on the acceleration measurement characteristic.

A. Functionality test

In this test set-up, we select a 10 Hz sample frequency and 9-bit resolution to measure the inclination from -90 to 90 degrees (equivalent with -1 g to 1 g acceleration). With these settings, the GSIC consumes 10.3μW (3 V supply). The test PCB contains the accelerometer and the GSIC. It is connected to an inclinometer calibration fixture (Model 5560, Robert A. Denton) (Fig. 3.53). In this static set-up, we can vary the orientation of the test accelerometer (gravitational field) in steps of 10 degrees.

Fig. 3.54 presents the measured digital output code as a function of the inclination. Fig. 3.55 shows the equivalent output characteristic as a function of the acceleration. In Fig. 3.56, we see that the non-linearity acceleration error is smaller than 0.03 g. The repeatability of the output is, for a constant acceleration, within ± 1 counts. Hence, the dominant noise source is the quantization.

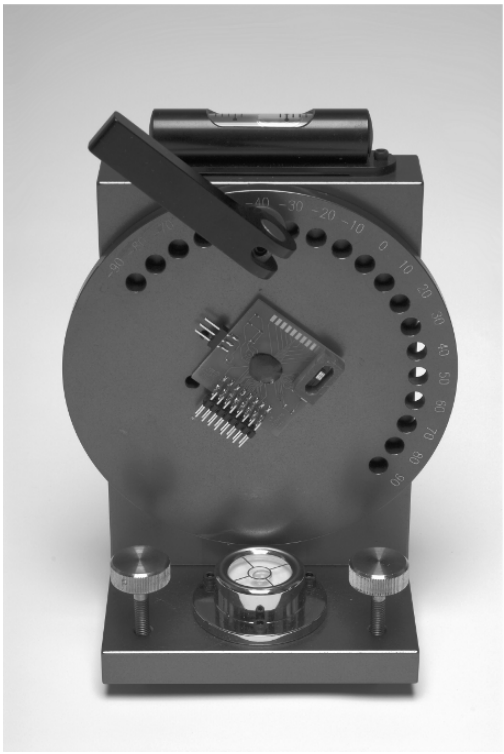

Figure 3.53. Inclination measurement set-up with test PCB (GSIC and accelerometer) connected to the calibration fixture.

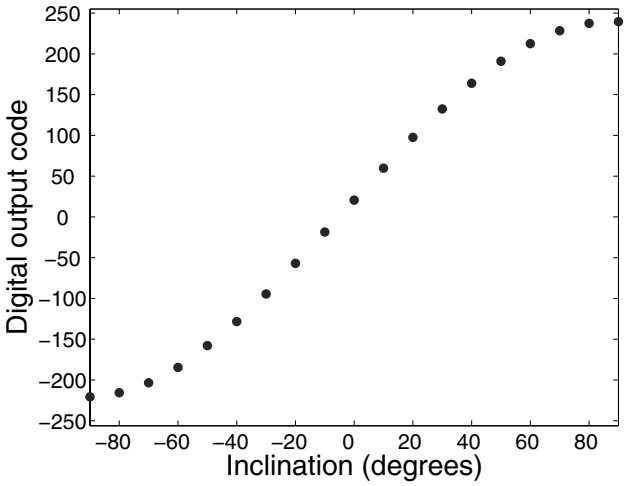

Figure 3.54. The measured digital output code as a function of the inclination.

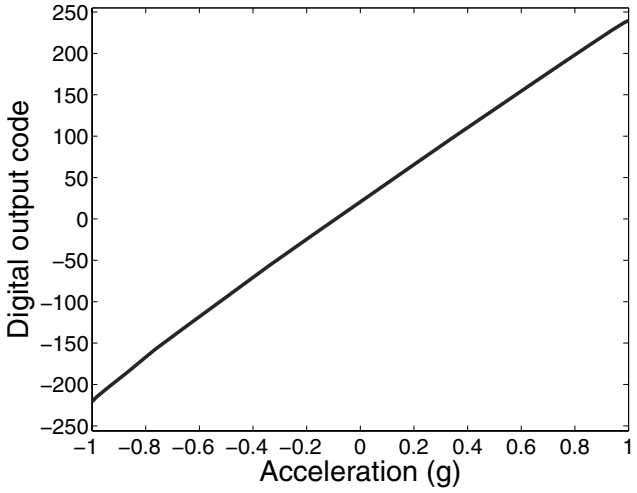

Figure 3.55. The measured digital output code as a function of the acceleration.

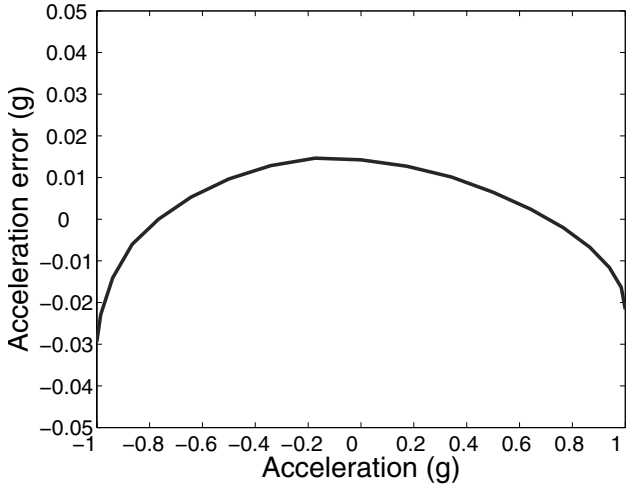

Figure 3.56. The non-linearity acceleration error as a function of the acceleration.

B. Test with different power supplies

The battery supply voltage of autonomous sensors decreases during the lifetime of the system. Furthermore, systems powered by energy scavengers (which take their energy from the environment, e.g. body warmth or vibrations) deal with a varying power source. Hence, it is important that the operation of

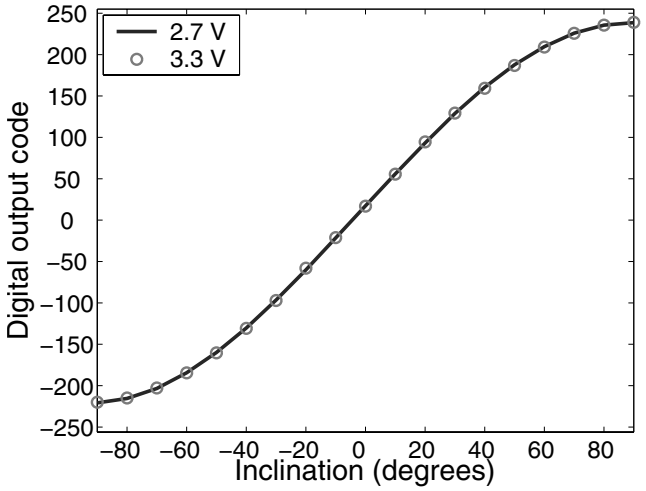

Figure 3.57. The measured digital output code as a function of the inclination for supply voltages of 2.7 and 3.3 V.

the sensor system is immune to a broad range of supply voltages. For this purpose the GSIC is tested in 9-bit mode with a 10 Hz sample frequency for a supply voltage between 2.7 V and 3.3 V. The GSIC consumed 8.2μW in the 2.7 V test and 12.4μW in the 3.3 V test. In Fig. 3.57, we see that the measured acceleration characteristic is nearly independent from the power supply.

C. Influence of the resolution mode

The configuration settings of the GSIC can be changed, while the system is operational. This allows to adapt the system to environmental changes. So, we can compensate for drift phenomena and we can decrease the average power consumption (sample frequency and resolution mode) when the available energy is getting low. A lower resolution mode corresponds with a shorter conversion time (10-bit $=>$ 8 ms, 8-bit $=>$ 2 ms). As a consequence, a change from 10-bit to 8-bit mode also creates a different electrostatic force on the mechanical sensor. In order to evaluate this phenomenon, we performed tests with the G001CC accelerometer in 10-bit and 8-bit mode for a sample frequency of 10 Hz. The GSIC consumed 16.8μW in 10-bit mode and 6.9μW in 8-bit mode with a power supply of 3 V. In Fig. 3.58, we see that the transition from 8-bit to 10-bit mode has a negligible effect on the accelerometer characteristic.

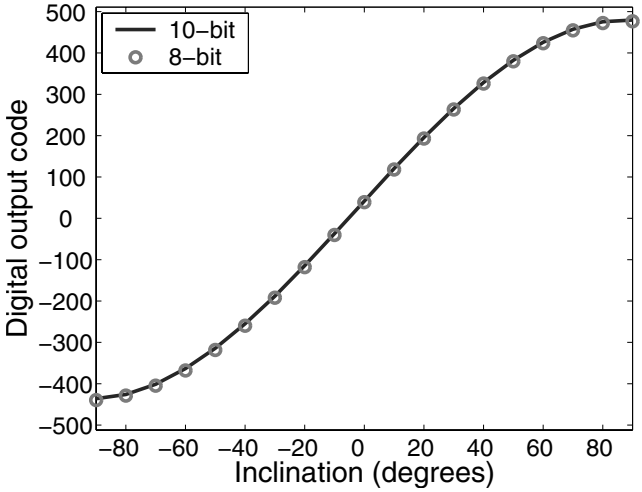

Figure 3.58. The measured digital output code as a function of the inclination for 10-bit and 8-bit resolution mode.

7. Performance comparison

The energy per accuracy level, En, gives a metric for the efficiency of the sensor interface. It is defined as follows:

$$En = \frac{P_{av}}{f_{sample} 2^b} \tag{3.63}$$

Where P_{av}, f_{sample} and b are the averaged power consumption, the sample frequency and the accuracy (in a bit number). The type of output also effects total efficiency. Sensor interfaces with digital outputs only need a serial or parallel interface to transfer the data to the microcontroller. This transfer can be extremely fast and power efficient, which allows the microcontroller to stay for a long period in sleep mode. On the other hand, sensor interfaces with analog output still need an external ADC, which consumes additional power. While sensor interfaces with quasi-digital output (frequency, period or duty cycle output) require a counting process, performed by the microcontroller, to yield the digital code. Hence, the microcontroller cannot enter the sleep mode during the conversion process. Tables 3.3 and 3.4 compare the energy per accuracy level of the GSIC with other generic interfaces and dedicated (U)LP capacitive sensor interfaces. We see that the GSIC outperforms the existing generic sensor interfaces. It even achieves an efficiency, which is better than most of the dedicated state-of-the-art ULP interfaces.

Table 3.3. Performance comparison between the GSIC, other generic sensor interfaces ($C_0 = 10.3$pF, $\Delta C = 1$ pF) and dedicated (U)LP pressure sensor systems.

ref	*output*	*range*	*accuracy*	$\mathbf{f_{sample}}$	$\mathbf{P_{av}}$	**En**
[Coo05]	quasidigital	100-130kPa	0.04kPa	10Hz	28μW	3.7nJ
[DG96]	digital	-	11 bit	2Hz	12μW	3nJ
[VTI]	digital	30-120kPa	18Pa	6.5Hz	84μW	2.6nJ
[Kol04]	digital	50-650kPa	1kPa	2Hz	1.5μW	1.3nJ
[VDG96]	quasidigital	100-130kPa	300aF	10Hz	5mW	150nJ
[Yaz00]	analog	100-130kPa	1fF	20Hz =2xBW	2.2mW	110nJ
this work	digital	100-130kPa	120Pa	10Hz	7μW	2.7nJ

Table 3.4. Performance comparison between the GSIC, other generic sensor interfaces ($C_0 = 2.5$pF, $\Delta C = 0.4$pF) and dedicated (U)LP accelerometer systems.

ref	*output*	*range*	*accuracy*	$\mathbf{f_{sample}}$	$\mathbf{P_{av}}$	**En**
[Ana]	analog	+/-2g	185mg (=6.6 x rms)	40Hz	32μW	37nJ
[ST]	digital	+/-2g	1mg	80Hz =2xBW	1.9mW	6nJ
[Col]	analog	+/-2g	1.4mg (=6.6 x rms)	42Hz =2xBW	600μW	5nJ
[Yaz00]	analog	+/-1g	1fF	20Hz =2xBW	2.2mW	275nJ
this work	digital	+/-1g	4mg	10Hz	10μW	2nJ

8. Conclusion

In this chapter, the specifications, design and results of the Generic Sensor Interface Chip for capacitive sensors have been presented. The GSIC is designed as a complete system, which is optimized for Ultra Low Power consumption. It contains the following blocks: Capacitance-to-Voltage converters, a SC amplifier, a $\Sigma\Delta$ modulator, a bandgap reference and bias circuits, a main oscillator and clock generation circuits, an LF clock, a configuration SRAM and an interface to the microcontroller.

- The SC interface (two C-V converters and a SC amplifier) converts a capacitance variation, ΔC, in a proportional voltage. It operates on a lower clock frequency, 8 kHz, than the $\Sigma\Delta$ modulator to reduce the power consumption. Reducing the clock frequency of the SC interface increases the influence of the parasitic shunt conductance. A C-V converter, which uses class AB techniques and Correlated Double Sampling operation is developed. This C-V converter is approximately three times more efficient in reducing the effects

of the shunt conductance than conventional C-V converters (with the same current consumption). The outputs of both C-V converters are chopped and filtered by the $\Sigma\Delta$ modulator to eliminate the effects of mismatches and to perform an adequate reduction of the common mode interference. The fully differential SC amplifier amplifies the difference between the outputs of both C-V converters and provides a quasi continuous input voltage for the modulator.

- The implemented CT $\Sigma\Delta$ modulator consists of a VI converter, a modulator and a decimation counter. The CT modulator has the advantage that it does not need a buffered reference voltage to attain the oversampling speed (128 kHz). This results in a significant decrease of the power consumption. The error sources in ultra low power CT $\Sigma\Delta$ modulators were examined. The dominant error source is caused by charge injections. This effect is eliminated by implementing a RZ switching scheme.

- The bandgap reference and bias circuits provide the bias currents to the sensor interface and the main oscillator. The system is immune to temperature variations in the range from -40 °C to 85 °C. Furthermore, its operation is quasi independent of the power supply in a range from 2.7 to 3.3 V. A switch in the start-up circuit of the bandgap reference offers a power down option for the total analog part of the system.

- The main oscillator and clock generation circuits provide the clock signals to the SC interface and the $\Sigma\Delta$ modulator. The main clock and the analog read-out electronics are switched off during OFF-state. A conversion timer is used to set the duration of the ON-state.

- The 8 kHz LF clock is used for the timing during low power standby operation. It is the only part of the system, which operates continuously. It has a very small current consumption of approximately 0.5μA.

- The GSIC has many configuration settings to provide an interface to a broad range of capacitive sensor applications. The capacitive sensor interface has two modes of operation. The first mode is for single sensor operation with on chip reference capacitor, where the reference capacitor, C_{ref2}, needs to be programmed to approximate C_0. The other mode is for differential sensor operation, where the on chip reference capacitor, C_{ref1} (or C_{ref2}), is programmed to compensate for the offset between C_x and C'_x. In both modes the amplification factor, A_{SC}, of the SC amplifier and the feedback capacitor, C_f, of the C-V converters need to be programmed for optimal accuracy of the interface (chapter 4).
  The sample frequency is 6-bit programmable between 2 Hz and 125 Hz and the ADC accuracy is selectable between 8, 9 or 10 bits for a conversion time

of 2, 4 or 8 ms. Hence, the averaged power consumption can be adapted to the accuracy and speed requirements of the selected application.
Both the LF clock and main oscillator are programmable to cope with technology variations.

The GSIC is designed in a 0.5μm CMOS technology and measures 3.2 mm by 2.9 mm (including the IO ring). The total system consumes merely 40μA in operational mode with a 3 V supply. The duty cycle management adapts the energy consumption according to the accuracy and speed requirements of the application. This results in a measured power consumption of 7.3μW in a pressure monitoring system (10 Hz sample frequency and 8-bit accuracy in the 100 to 130 kPa range). For the acceleration measurement system, it achieves a power consumption of 10.3μW for a sample frequency of 10 Hz and 9-bit accuracy in the ± 1 g range.

Chapter 4

ALGORITHM FOR OPTIMAL CONFIGURATION SETTINGS

1. Introduction

Generic sensor interface design reduces the costs and offers a handy solution for multisensor applications. However, previous generic readout circuits often experienced a loss of performance and an increased power consumption. The ability to program the front-end would have an important impact on the accuracy of the sensor readout. The new design methods reported in this chapter allow us to create a generic sensor interface with a minimum loss. Furthermore, an algorithm is provided, which calculates the optimal interface settings for each application. These settings enable a state-of-the-art performance from our ULP generic sensor interface.

Section 2 studies the non-ideal effects (full-scale loss, leakage error, settling error and noise) of configurable capacitive sensor interfaces. General design methods are derived, which are illustrated on the generic interface architecture. Section 3 presents an algorithm that estimates the optimal configuration of the interface for each application. This algorithm is expressed as an optimization problem, which minimizes the total error. The minimized objective function considers the full-scale loss, leakage error, settling error, noise and ADC accuracy. In section 4, we apply the algorithm in a prototype biomedical pressure monitoring system.

2. Programmability

The front-end architecture consists of a Switched Capacitor (SC) interface followed by a modulator. The SC interface works on a lower clock frequency, 8 kHz, than the modulator, 128 kHz, to reduce power consumption. In the Capacitance-to-Voltage (C-V) converter, the sense capacitance, C_x, is converted to a proportional voltage. The SC amplifier amplifies the difference between the

outputs of both C-V converters and produces a quasi continuous input voltage for the $\Sigma\Delta$ modulator. The capacitive sensor interface has two modes of operation. The first mode is for single sensor operation, where the reference capacitor C_{ref} needs to be programmed to approximate C_0. The other mode is for differential sensor operation, where the on chip reference capacitor is used to compensate for the offset between C_x and C'_x. In both modes, the amplification factor A_{SC} of the SC amplifier and the feedback capacitor C_f of the C-V converters need to be programmed for optimal accuracy of the interface.

The programmability (step size and range) of C_{ref}, C_f and A_{SC} strongly influences the use of the dynamics and the settling performance of the interface. This section introduces methods to estimate these influences mathematically. Furthermore, the appropriate step sizes and ranges of C_{ref}, C_f and A_{SC} are calculated for our generic architecture.

2.1 Full-scale loss

We consider a general sensor characteristic $C(x)$, where x varies between x_{min} and x_{max} (Fig. 4.1). If C_{ref}, C_f and A_{SC} have unlimited programmability, the input of the modulator sees a voltage characteristic between $-0.5Vfs_{pp}$ and $0.5Vfs_{pp}$. Due to the limitation of the programmability, one cannot use the full input range of the ADC (Fig. 4.2). The full-scale loss ΔVfs_{rel} is given by:

$$\Delta Vfs_{rel} = \frac{\Delta V_{max} + \Delta V_{min}}{Vfs_{pp}} \tag{4.1}$$

where ΔV_{max} and ΔV_{min} are the deviations between the ideal (unlimited programmable interface) and realistic (limited programmable interface) ADC input characteristics at x_{max} and x_{min}.

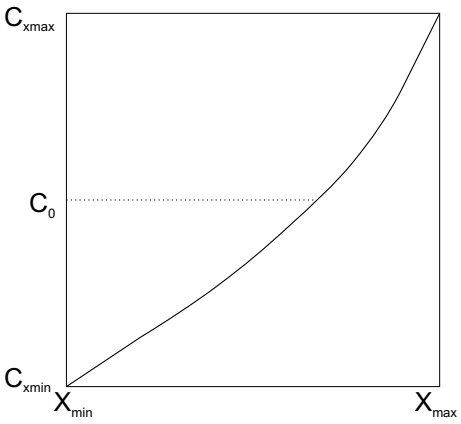

Figure 4.1. General sensor characteristic $C(x)$.

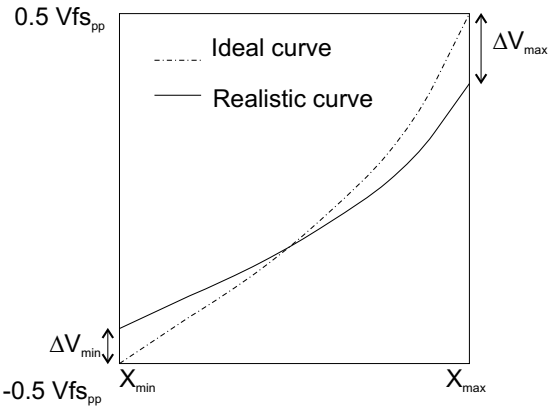

Figure 4.2. The input voltage of the modulator for an unlimited (ideal curve) and limited (realistic curve) programmable SC interface.

The full-scale loss has two causes: firstly, the components are programmable between certain boundaries, P_{min} and P_{max}; secondly, they are programmable in finite steps, P_{step}.

The optimal settings are calculated with an algorithm, which maximizes the accuracy (see section 3). This objective function considers not only the full-scale loss, but also the settling error, leakage error, noise and ADC accuracy. Due to the boundaries of the programming components, the optimal settings may result in a full-scale loss that is significant. For our capacitive sensor interface, this deterministic full-scale loss is given by:

$$\Delta Vfs_{rel} = 1 - \frac{dV_{ref}\alpha C_0 A_{SC}}{C_f Vfs_{pp}} \tag{4.2}$$

where $d = 1$ for single sensors and $d = 2$ for differential sensors.

The finite step size makes the programmed value P differ from the ideal value P_i by an amount $\Delta P = P - P_i$. This deviation ΔP can be considered as a stochastic variable with a uniform probability distribution between $-0.5P_{step}$ and $0.5P_{step}$. This results in a stochastic full-scale loss.

2.2 Programmability of C_{ref}

The deviation, ΔC_{ref}, of C_{ref} to C_0 ($d = 1$) or C_{ref} to C_{offset} ($d = 2$) results in an offset voltage, ΔV_{offset}, towards the ideal ADC input characteristic (Fig. 4.3):

$$\Delta V_{offset} = \frac{A_{SC}\Delta C_{ref} V_{ref}}{C_f} \tag{4.3}$$

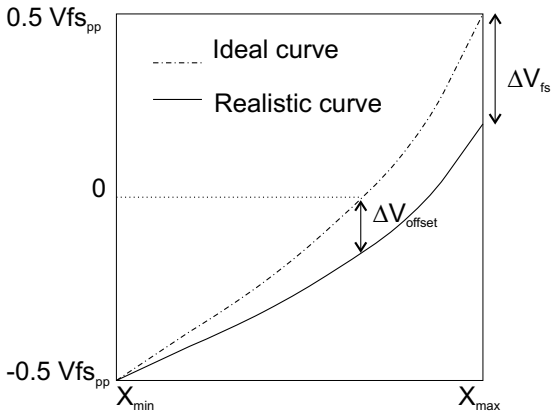

Figure 4.3. The full-scale loss ΔVfs for an offset deviation ΔV_{offset}.

If we assume that C_f and A_{SC} have unlimited programmability, we find:

$$\Delta Vfs_{rel} = \frac{2\Delta C_{ref}}{d\Delta C} \tag{4.4}$$

We consider ΔC_{ref} as a stochastic variable with a uniform probability function between $-0.5C_{ref,step}$ and $0.5C_{ref,step}$. Hence, the full-scale loss is also uniformly distributed with mean value zero and standard deviation :

$$\sigma(\Delta Vfs_{rel}) = \frac{2C_{ref,step}}{d\Delta C\sqrt{12}} \tag{4.5}$$

This standard deviation gives a measure for the loss in dynamics, which is caused by the finite step size, $C_{ref,step}$, of C_{ref}. In order to allow a good exploitation of the system dynamics, we postulate that $\sigma(\Delta Vfs_{rel})$ needs to be smaller than 25% for our interface (200fF$<\Delta C<$10pF and 1pF$<C_0<$15pF). In Fig. 4.4 we see that this condition is met for a $C_{ref,step}$ value of 75 fF.

Hence, we obtain a C_{ref} capacitance, which is 8-bit programmable between 0 and 19.125 pF ($= C_{ref,max} > C_{0,max}$) in steps of 75 fF. The matching properties of a standard analog CMOS technology do not pose any problem for the development of such an 8-bit capacitor array (INL$<<0.5$LSB).

2.3 Programmability of C_f

Fig. 4.5 shows the ULP C-V converter (section 3.2). During the sampling phase Φ_1, the sense capacitor, C_x, is charged. During the signal phase Φ_2, V_p becomes a virtual ground and the charge is transferred to the feedback capacitor, C_f. At the end of the signal phase, assuming an ideal charge transfer, the voltage at the output of the C-V converter equals $V_{ref}(C_x/C_f)$. In reality, the charge

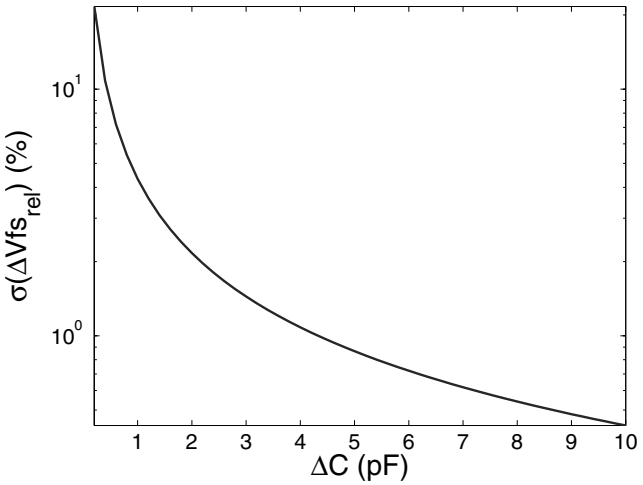

Figure 4.4. Standard deviation of the full-scale loss as a function of ΔC with $C_{ref,step}$= 75 fF ($d = 1$).

transfer will be imperfect due to the finite transient response of the OTA. This transfer error has two contributions: the leakage error and the settling error. The potential V_p will settle in a certain time to the virtual ground, during this time some charge will leak away through the parasitic shunt conductance, G_p, resulting in a leakage error. At the end of Φ_2, the potential V_p will be slightly different from the ground level, so a small charge remains on $C_{p2}+C_x$, resulting in the settling error.

The C-V converter uses a class AB OTA with cascode output stage to reduce the leakage and settling errors (Figs. 4.6 and 4.7). After the transition from phase Φ_1 to phase Φ_2, the tail current of the OTA is boosted, which speeds up the charge transfer from the sense capacitor to the feedback capacitor. During

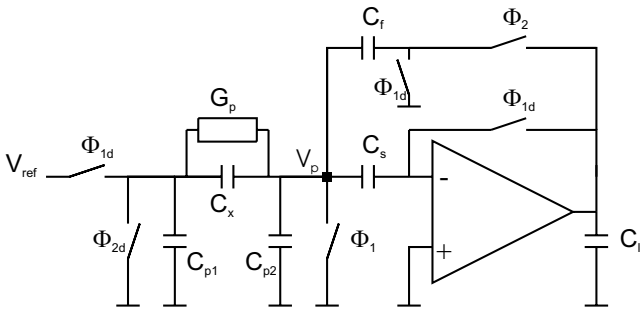

Figure 4.5. Capacitance-to-Voltage converter with correlated double sampling and class AB operation.

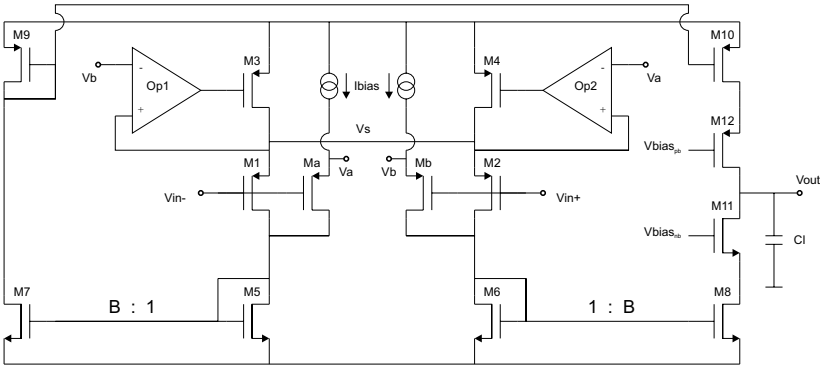

Figure 4.6. Class AB OTA.

settling, the voltage V_p approaches the virtual ground and the tail current falls back to a low quiescent level.

During Φ_2, the charge transfer passes the following three phases:

- During the first phase, the internal feedback op-amps *op* set the potential V_s to follow the larger of the two voltages V_a and V_b.

- During the second phase, the current is strongly boosted and the output current of the OTA, I_{out}, becomes:

$$\begin{aligned} I_{out} &= BI_{bias}\left(\exp\left(\frac{V_{in+}-V_{in-}}{nU_T}\right)-1\right) \\ &\approx BI_{bias}\exp\left(\frac{V_{in+}-V_{in-}}{nU_T}\right) \end{aligned} \tag{4.6}$$

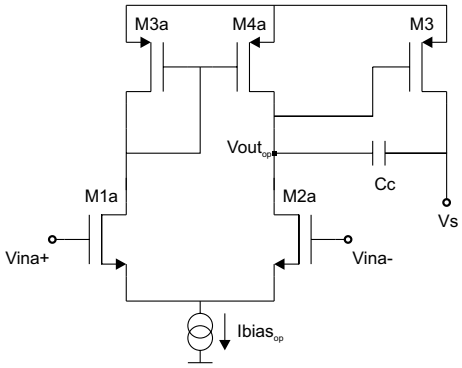

Figure 4.7. Internal feedback op-amp.

- During the third phase, the current boosting is nearly exhausted and the OTA output current shows a small signal settling behavior

$$\begin{aligned} I_{out} &= BI_{bias}\left(\exp\left(\frac{V_{in+}-V_{in-}}{nU_T}\right)-1\right) \\ &\approx BI_{bias}\left(\frac{V_{in+}-V_{in-}}{nU_T}\right) \end{aligned} \tag{4.7}$$

The total leakage error $leak_{err}$ has contributions of the three phases:

$$\begin{aligned} leak_{err} = \frac{G_p}{C_x V_{ref}}\Bigg(&\int_0^{\Delta t_1} V_{in}(0)dt + nU_T\int_0^{\Delta t_3}\exp\left(\frac{-BI_{bias}ft}{nU_T C_{out}}\right)dt \\ &-nU_T\int_0^{\Delta t_2}\ln\left(\exp\left(\frac{-V_{in}(0)}{nU_T}\right)+\frac{BI_{bias}ft}{nU_T C_{out}}\right)dt\Bigg) \end{aligned} \tag{4.8}$$

with

$$\begin{aligned} V_{in}(0) &= \frac{V_{ref}C_x}{C_x + C_{p2} + C_f C_l/(C_f + C_l)} \\ C_{out} &= C_l + \frac{C_f(C_x + C_{p2})}{C_f + C_x + C_{p2}} \\ f &= \frac{C_f}{C_f + C_x + C_{p2}} \end{aligned} \tag{4.9}$$

The time intervals Δt_1, Δt_2 and Δt_3 indicate the duration of each phase and are given by the following formulas:

$$\begin{aligned} \Delta t_1 &\approx \frac{V_{gs3}C_c}{I_{biasop}} \\ \Delta t_2 &\approx \left(\exp(-1) - exp\left(-\frac{V_{in}(0)}{nU_T}\right)\right)\frac{C_{out}nU_T}{fBI_{bias}} \\ \Delta t_3 &\approx T_{\Phi 2} \end{aligned} \tag{4.10}$$

where $T_{\Phi 2}$ is the duration of the signal phase Φ_2.

The contributions of the first two phases are negligible in the settling error, $settling_{err}$, then we obtain:

$$settling_{err} \approx \frac{(C_{p2} + C_x)nU_T \exp\left(-\frac{BI_{bias}f\Delta t_3}{C_{out}nU_T}\right)}{C_x V_{ref}} \tag{4.11}$$

The leakage and settling errors decrease with increasing C_f. Simulations show that our interface has a good settling behavior if the feedback factor f is greater

than 0.25. This implies that $C_{f,max}$ needs to be higher than $1/3(C_{x,max} + C_{p2,max})$ to provide a sufficient settling for the whole application range. On the other hand, a larger C_f needs a larger chip area and a larger amplification factor, A_{SC}, for the SC amplifier to use the full input range of the ADC. This results in a higher GBW specification and hence a higher power consumption for the SC amplifier. If we make C_f 4-bit programmable between 0 and 27 pF ($= C_{f,max}$) in steps of 1.8 pF, we can always find a suitable C_f for the specified application range.

In order to evaluate the validity of the leakage charge model, we compare the mathematical model (4.8-4.10) with Cadence simulations. Fig. 4.8 shows the leakage charge as a function of C_x and C_{p2} with $G_p = 0.01\mu$S and optimal configuration settings (algorithm section 3, with $d = 1$, $\alpha = 0.5$ and $b = 10$bits). In Fig. 4.9, we see that the model has an accuracy of 5% for most of the capacitor values. Only for small values of C_x (< 3pF) the error rises to approximately 20%.

2.4 Programmability of A_{SC}

The limited programmability of A_{SC} results in a full-scale loss (Fig. 4.10):

$$\Delta V f s_{rel} = \frac{\Delta A_{SC}}{A_{SC}} \tag{4.12}$$

The full-scale loss contains contributions of the deterministic full-scale loss (limited range $A_{SC,max}$) and the stochastic full-scale loss (limited step size $A_{SC,step}$).

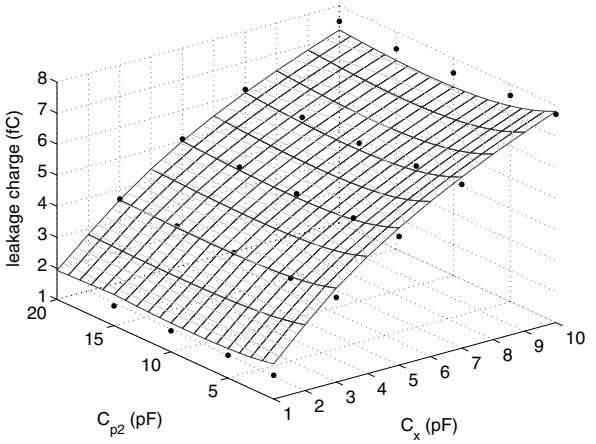

Figure 4.8. The leakage charge as a function of C_x and C_{p2} (mathematical model=meshed curve, Cadence simulation=marker points.

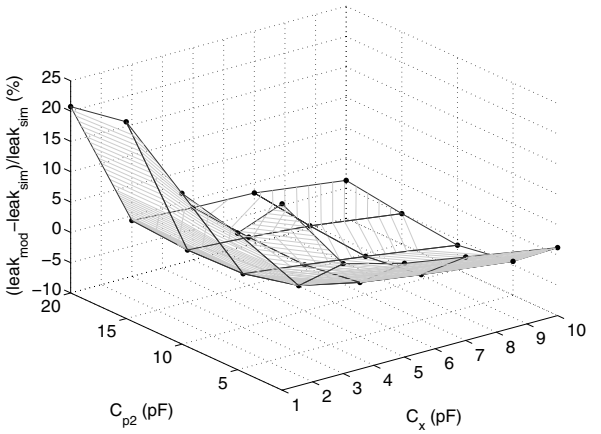

Figure 4.9. The relative deviation between the mathematical leakage charge model and the Cadence simulation points as a function of C_x and C_{p2}.

We assume that the full output range of the C-V converters is used for small α. Hence, we find that the interface can always provide an optimal usage of the ADC input range (deterministic full-scale loss $\Delta Vfs(det) = 0$) if

$$A_{SC,max} > \frac{Vfs_{pp}}{d\alpha_{min}Vfs_{C-V}} \tag{4.13}$$

where Vfs_{C-V} is the maximum allowable output voltage of the C-V converters. Consequently, the output of the C-V converter will not saturate.

In our interface ($\alpha_{min} = 0.05$, $Vfs_{C-V} = 1\text{V}$ and $Vfs_{pp} = 0.5\text{V}$ for single sensors $d = 1$) we choose $A_{SC,max} = 15.75$ accoring to condition (4.13).

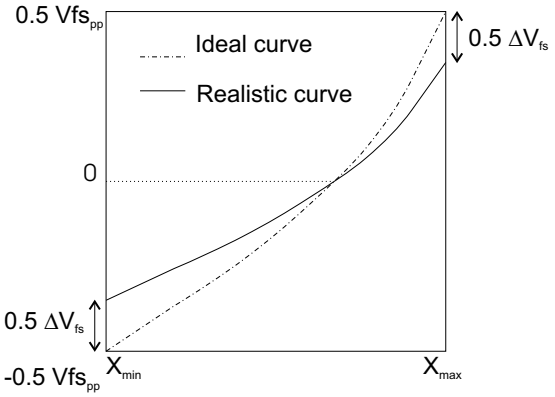

Figure 4.10. The full-scale loss ΔVfs for a slope deviation.

For the stochastic full-scale loss, we consider ΔA_{SC} as a stochastic variable with uniform probability function between $-0.5A_{SC,step}$ and $0.5A_{SC,step}$. We obtain:

$$\sigma(\Delta Vfs_{rel}) = \frac{A_{SC,step}}{\sqrt{12}A_{SC}} \tag{4.14}$$

If we assume that $C_{f,op}$ is programmed for optimal settling and the deterministic full-scale loss is zero, we find:

$$\sigma(\Delta Vfs_{rel}) = \frac{d\alpha C_0 V_{ref} A_{SC,step}}{C_{f,op} Vfs_{pp}\sqrt{12}} \tag{4.15}$$

where

if $Vfs_{pp}\frac{C_{f,max}}{\alpha C_0 V_{ref} d} < A_{SC,max}$

$$C_{f,op} = C_{f,max} \tag{4.16}$$

else

$$C_{f,op} = A_{SC,max}\frac{\alpha C_0 V_{ref} d}{Vfs_{pp}} \tag{4.17}$$

In order to offer a standard deviation of the full-scale loss smaller than 25% for capacitive sensor applications with $\alpha > 0.05$ and 200fF$< \Delta C <$ 10pF, we program A_{SC} between 0 and 15.75 in steps of 0.25 (Fig. 4.11).

2.5 Noise

The noise of the system depends on the configuration settings of the front-end circuit. The noise presented at the input of the modulator $V_{rms,noise}$ contains

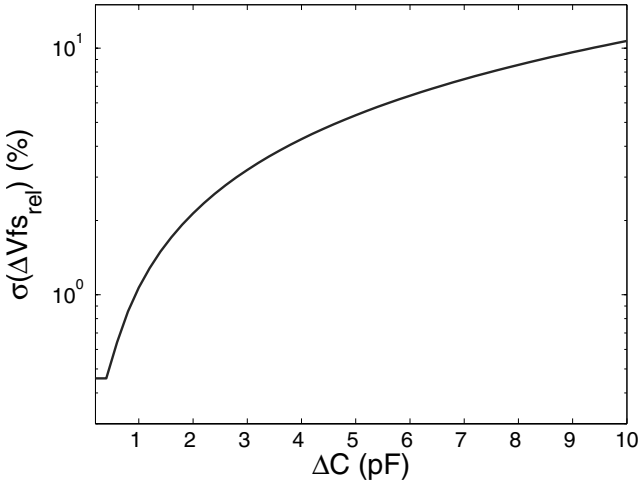

Figure 4.11. Standard deviation of the full-scale loss as a function of ΔC, with $A_{SC,step} = 0.25$ and $d = 2$ (differential sensors).

contributions of the C-V converter and the SC amplifier. This noise is calculated with the techniques from section 5.

3. Optimal settings

For every application, optimal settings for C_{ref}, C_f and A_{SC} can be obtained. They are the solution of an optimization problem, which minimizes the total error (4.18).

Given: a capacitive sensor application with the following properties: d, C_0, α, C_{p1}, C_{p2}, G_p and an ADC accuracy of b bits. For a single sensor application ($d = 1$), we set $C_{ref} \approx C_0$. In a differential sensor application ($d = 2$), we program C_{ref} to compensate for the offset between C_x and $C_{x'}$.

The algorithm minimizes the objective function:

$$\sqrt{\begin{array}{l}\left(leak_{err}(C_x = C_0)\right)^2 + \left(settling_{err}(C_x = C_0)\right)^2 \\ + \left(\frac{2^{-b}}{1-\Delta Vfs_{rel}}\right)^2 + \left(\frac{2^{-b_{noise}}}{1-\Delta Vfs_{rel}}\right)^2\end{array}} \tag{4.18}$$

where

$$\Delta Vfs_{rel} = \sqrt{\begin{array}{l}\left(\Delta Vfs_{rel}(det)\right)^2 + \left(\sigma\left(\Delta Vfs_{rel}(A_{SC})\right)\right)^2 \\ + \left(\sigma\left(\Delta Vfs_{rel}(C_{ref})\right)\right)^2\end{array}} \tag{4.19}$$

This formula has contributions of the leakage error (4.8), settling error (4.11), the noise b_{noise}, the ADC accuracy b, the deterministic full-scale loss (4.2) and the stochastic full-scale losses due to A_{SC} (4.14) and C_{ref} (4.5).

The feasible solutions of the problem are subject to the following four constraints:

- The outputs of the C-V converter are not allowed to saturate.

$$Vfs_{C-V}C_f \geqslant V_{ref}\left(1 + \frac{\alpha}{2}\right)C_0 \tag{4.20}$$

- The ADC is not allowed to saturate.

$$\frac{V_{ref}\alpha d C_0 A_{SC}}{C_f} \leqslant Vfs_{pp} \tag{4.21}$$

- The lower and upper bound of C_f.

$$0 \leqslant C_f \leqslant 27\text{pF} \tag{4.22}$$

- The lower and upper bound of A_{SC}.

$$0 \leqslant A_{SC} \leqslant 15.75 \tag{4.23}$$

4. Results

The computer algorithm is implemented in Matlab as a constraint based gradient search optimization function and performs a smooth convergence. As an example, we consider the case of bladder pressure measurements for urodynamic tests. In this application we use a single capacitive absolute pressure sensor (B012FA, VTI Technologies) to monitor the pressure in the range of 100-130 kPa. The application properties are: $\alpha = 0.1, C_0 = 10.3$pF, $G_p = 0.001\mu$S and $C_{p1} = C_{p2} = 30$pF. The ADC accuracy is set to 10 bits. Fig. 4.12 shows the error function (4.18) for the feasible A_{SC} and C_f values (4.20-4.23). The algorithm gives $C_{ref} = 10.275$pF, $C_f = 16.2$pF and $A_{SC} = 7.25$ as optimal solution. For these values, we obtain a leakage error of 0.01%, a negligible settling error, a full-scale loss of 4% and noise b_{noise} of 11.5 bits. These settings are the starting points of a calibration cycle. During this procedure, the settings can be adjusted in order to cope with the technology variations of the sensors and the interface chip. The measured full-scale loss is approximately 7%. The repeatability of the output is, for each applied pressure, within ± 1

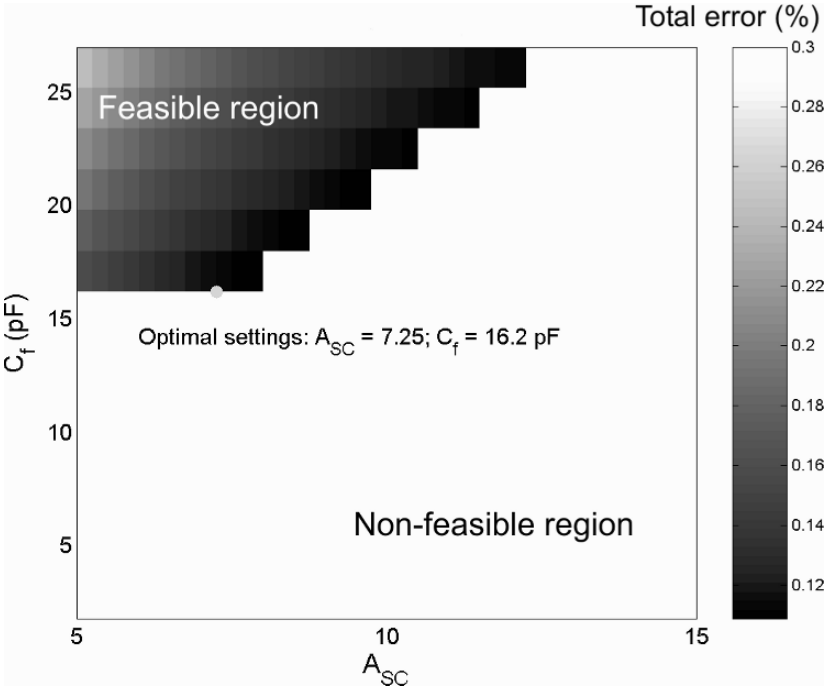

Figure 4.12. Error function (4.18) for the feasible A_{SC} and C_f values, the optimal settings $A_{SC} = 7.25$ and $C_f = 16.2$pF result in an error of 0.11%. The white region violates the constraints (non-feasible region).

count. Hence, the dominant noise source is the quantization, as was predicted by the calculated model (4.18).

5. Conclusion

The limited programmability of generic sensor interfaces results in a loss of dynamic range (full-scale loss). Hence, the influence of noise increases and the ADC accuracy is not exploited optimally. Furthermore, it is important that one maximizes the interface accuracy for each application. This can be expressed as an optimization problem. The minimized objective function considers the leakage error, settling error, noise, ADC accuracy, deterministic and stochastic full-scale losses. The obtained values for C_{ref}, C_f and A_{SC} estimate the optimal configuration. These settings are the starting points of a calibration cycle. During this procedure, the settings can be adjusted in order to cope with the technology variations of the sensors and the interface chip.

Chapter 5

PHYSICAL ACTIVITY MONITORING SYSTEM

1. Introduction

The developed Generic Sensor Interface Chip enables low cost autonomous sensor nodes for several state-of-the-art applications. This is illustrated in a demonstrator for physical activity monitoring. The system can be used to monitor the wellness of both humans and animals. The miniaturized sensor node contains an accelerometer, the GSIC, a microcontroller and a wireless transceiver. A computer interface displays the sensor data in real-time and allows to change the interface settings during operation.

Section 2 presents the background and motivation for physical activity monitoring. The implementation of the system is given in section 3.

2. Background and motivation

A physical activity monitoring system is useful for the surveillance and evaluation of patients [Ste03]. Such systems are used to motivate clinical groups to exercise, including people with diabetes, obesity and congestive heart failure. Furthermore, the motion sensor technology helps to improve the quality of rehabilitation programs and program changes.

The activity monitoring system contains an accelerometer, which monitors the low frequent body movements (bandwidth < 20Hz). The accuracy of the system is significantly increased by filtering the high frequent vibrations. For this purpose, a sensor with low pass characteristic is used. Extra filtering is performed by the read-out electronics (e.g. $\Sigma\Delta$ modulator and digital filtering techniques). In most cases, the observation of the physical activity takes several days or even weeks. Hence, Ultra Low Power sensor nodes are necessary to enable long term monitoring.

Activity monitoring systems are also used for animal welfare observations. In this application, the activity, heart rate and body temperature gives an indication for the health of livestock [Wou95]. Hence, the productivity in farms can be significantly increased.

3. Implementation

The physical activity gives a good indication for the health and wellness. For this purpose, we have developed a wireless autonomous sensor system, which monitors the acceleration in the range from -7.5 g to 7.5 g. This physical activity monitoring has been implemented as a 3D stack, which contains a sensor, a microcontroller and a wireless layer. The sensing layer is developed in this work, whereas the microcontroller and wireless layers were already presented in [Tor04]. Each layer has been made on a 14 mm x 14 mm printed circuit board. The boards are connected vertically into a miniaturized cube (Fig. 5.1).

The sensor layer performs the sensing, amplification and analog-to-digital conversion of the acceleration signal. It contains a differential capacitive accelerometer (G012BA of VTI Technologies) and the GSIC (naked die covered with globtop coating).

The microcontroller layer implements the data processing and control of the entire module. An MSP430 microcontroller (Texas Instruments) was selected for its low active power (0.6 nJ/ instruction), low standby power (2μW) and fast wakeup from standby to active mode (6μs). To meet the size requirements, a bare die component is used, which is encapsulated with globtop coating.

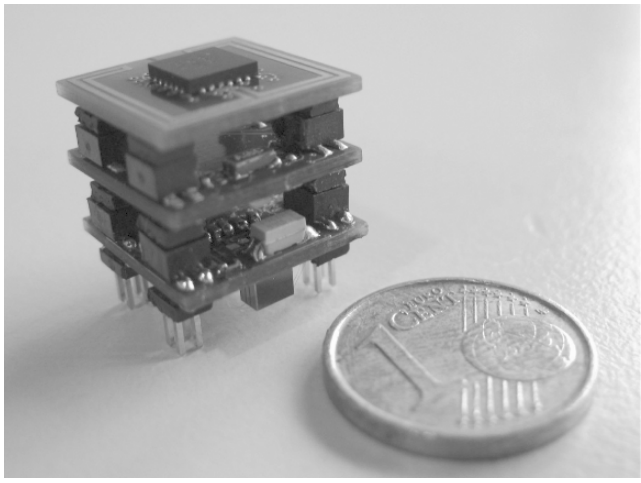

Figure 5.1. 3D stacked autonomous sensor cube, containing a sensor, a microcontroller and a wireless layer (size 14mm x 14mm x 12mm).

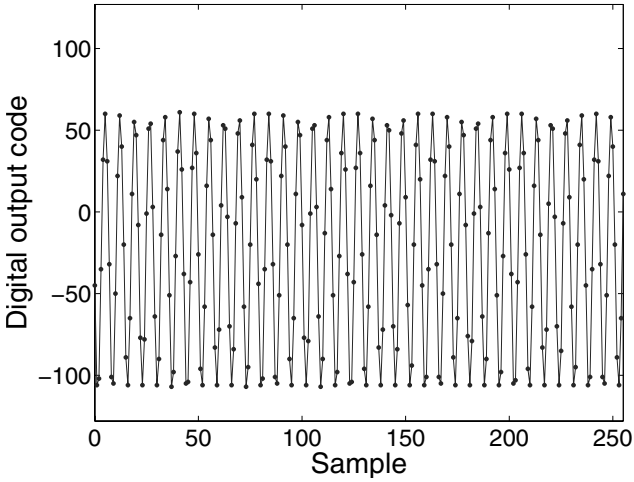

Figure 5.2. Output data for a sinusoidal acceleration (f=15Hz, peak-to-peak amplitude=10g, offset=-1g).

The wireless layer consists of a single-chip short-range 2.4 GHz transceiver (nRF2401, NORDIC, 18 nJ/bit) with a custom designed coplanar integrated folded dipole antenna.

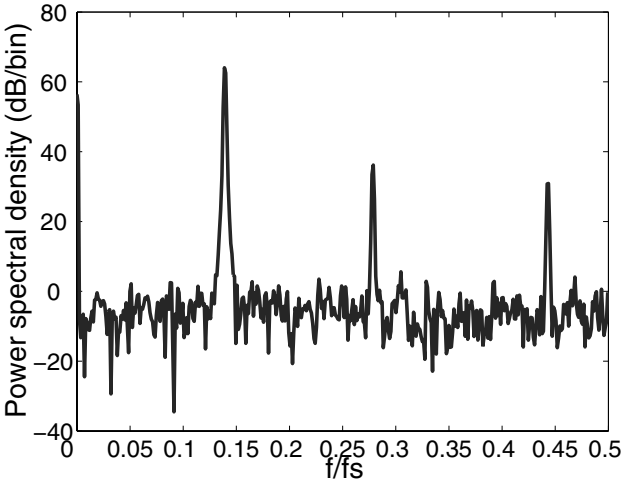

Figure 5.3. Power Spectral Density of the output data for a sinusoidal acceleration (f=15Hz, peak-to-peak amplitude=10g, offset=-1g).

The sensor node communicates with a remote basestation, which is implemented on the PC (USB stick). A Labview computer interface displays the data in real-time and allows to change the interface settings remotely.

We have selected a 120 Hz sample frequency and 8-bit accuracy for this application. Hence, the GSIC operates in a duty cycle of 24%, which results in a measured average current consumption of 16μA. The total system (GSIC, microcontroller and wireless core) consumes 700μA. The dynamic performance of the system is tested with shaker tests. In these tests, we applied a 15 Hz, 10 g (peak-to-peak) sinusoidal acceleration with 1 g (gravitational field) offset on the sensor node (Fig. 5.2). Fig. 5.3 shows the measured output spectrum. The harmonics in the spectrum correspond to a non-linearity of 4.1%. The rms noise to signal ratio equals 0.7%.

4. Conclusion

A modular autonomous sensor node for physical activity monitoring has been developed. The 3D stacked cube is approximately 1 cm^3 and contains a sensor board (accelerometer and GSIC), a microcontroller board and a wireless board. In this application, the GSIC consumes approximately 48μW for a sample frequency of 120 Hz and 8-bit accuracy. The digital sensor data are temporarily stored in the memory of the microcontroller. No data compression is performed, although application specific algorithms could be implemented in the microcontroller. The wireless transceiver sends the sensor data in packages of four words to the remote USB transceiver. The computer interface displays the data in real time and allows to change the configuration settings of the GSIC via the bidirectional wireless communication link.

Chapter 6

CONCLUSION

1. Realized developments

An increasing number of medical diagnostics, comfort, entertainment and sports applications are making use of sensor systems in and around the body. Power autonomy is still a major challenge in these applications and a significant part of the power consumption stems from the sensor interface circuitry. Most often, the sensor interface is tailored towards one specific application. This leads to a high recurrent design cost. An Ultra Low Power (ULP) generic multi-sensor interface would offer a solution to both problems. Several research groups have already developed generic sensor interface architectures. Because the power dissipation of these systems is in the mW range, the power autonomy problem is not solved. ULP sensor interface circuits have also been reported, but these are dedicated to a specific sensor and therefore do not address the generic application requirement.

This work presents a new generic architecture for autonomous sensor nodes. The modular design methodology provides a flexible way to build a complete sensor interface out of configurable blocks. The combination and the settings of these blocks can be changed according to the varying needs of the application. Furthermore, the sensor system can be expanded with additional building blocks during the development phase.

This architecture is illustrated in a Generic Sensor Interface Chip (GSIC) for capacitive sensors. The GSIC contains a microcontroller interface, a configuration memory and the following configurable blocks: LF clock, sample timer, reference and bias circuits, main oscillator and clock generation circuits, Capacitance-to-Voltage (C-V) converters, Switched Capacitor (SC) amplifier, voltage-to-current (VI) converter, modulator, decimation counter and conversion counter.

The sensor interface converts a capacitance variation, ΔC, into a proportional digital output code. It consists of a SC interface followed by a $\Sigma\Delta$ modulator. The SC interface (two C-V converters and a SC amplifier) operates on a lower clock frequency, 8 kHz, than the modulator, 128 kHz, to achieve very low power consumption. A new C-V converter with class AB and Correlated Double Sampling (CDS) operation is developed. This C-V converter is approximately three times more efficient in reducing the effects of the shunt conductance than conventional C-V converters (with the same current consumption). The mismatch between both C-V converters makes the system more susceptible to interference. This can cause an extra loss in accuracy. The proposed chopping scheme provides a solution for this problem. Hence, a pseudo differential structure is built, where the capacitive sensor elements are connected to each C-V converter for an equal number of interface periods. This modulates the effects of the mismatch with the chopping sequence. These components are filtered by the low pass operation of the $\Sigma\Delta$ modulator. The fully differential SC amplifier amplifies the difference between the outputs of the C-V converters and provides a quasi continuous input voltage for the modulator. The CT $\Sigma\Delta$ modulator consists of a VI converter, a modulator and a decimation counter. It produces an 8-bit, 9-bit or 10-bit code for a conversion time of 2, 4 or 8 ms (INL and DNL are in all modes smaller than 0.5 LSB).

The main oscillator and clock generation circuits provide the clock signals to the capacitive sensor interface and the decimation counter. The LF clock is used for the timing during low-power standby operation. The reference and bias circuits generate the bias currents for the sensor and the main oscillator.

The GSIC performs an interface to single and differential capacitive sensors with 1pF$<$ C_0 $<$15pF, 200fF$<$ ΔC $<$10pF and 0.05$<$ $\alpha(=\Delta C/C_0)$. For single sensor operation, the on chip reference capacitor, C_{ref}, needs to be programmed to approximate C_0. For differential sensor operation, the on chip reference capacitor is programmed to compensate for the offset between C_x and $C_{x'}$. In both modes the amplification factor, A_{SC}, of the SC amplifier and the feedback capacitor, C_f, of the C-V converters need to be programmed for optimal accuracy of the interface. The sample frequency is 6-bit programmable between 2 Hz and 125 Hz. Both the LF clock and main oscillator are programmable to cope with technology variations.

The GSIC is designed in a 0.5μm CMOS technology for a supply voltage between 2.7 and 3.3V. The chip has a size of 3.2mm by 2.9mm. The GSIC is tested with several pressure sensors and accelerometers. In the pressure monitoring system, we measured an averaged power consumption of 7.3μW for a 10 Hz sample frequency and 8-bit accuracy in the 100 to 130 kPa range. For the acceleration measurement system, it achieves a power consumption of 10.3μW for a sample frequency of 10 Hz and 9-bit accuracy in the $\pm$1 g range. The energy per accuracy was defined as a performance metric. It is shown that

the GSIC outperforms the existing generic sensor interfaces. It is even more efficient than most of the dedicated ULP sensor interfaces.

A physical activity monitoring system is implemented in a 1 cm^3 stack. This demonstrator consists of a sensor layer (the GSIC and an accelerometer), a microcontroller layer and a wireless layer. The bidirectional wireless link (from the sensor node to the computer) makes it possible to display the data in real time and to change the interface settings remotely. Hence, we have made a smart autonomous sensor node, which can adapt at any time to changes in the environment.

2. Suggestions for future work

Based on the developments presented in this work, some suggestions for future work in the field of autonomous sensor interfaces are summarized:

- The implemented GSIC can only interface with capacitive sensors. But the modular architecture can be expanded with extra configurable blocks, such as a temperature sensor or a (bio)potential interface. For this purpose, programmable filters, instrumentation amplifiers, etc. need to be developed. Hence, one could make a microsystem that can interface with several types of sensors in different time intervals. This will result in applications such as a personal health assistant, which monitors the blood pressure, body temperature and heart rate.

- Many biomedical applications need an extremely miniaturized sensor node. One could reduce the size of the 3D stack with special packaging techniques (e.g. 3D solder ball interconnect technology). Furthermore, the activity monitoring system could be implemented on a flexible substrate, which is very suitable for human body applications (smart bracelet). However, this packaging technique effects the mechanical response (linearity, damping, etc.) of the accelerometer system. New measurement set-ups should be developed to estimate the real life performance and reliability of such a system.

- One could integrate a microcontroller core or a digital signal processing unit with the interface electronics. Potential benefits are a reduced power consumption (less buffering, processing unit is more dedicated to smart sensor applications), a smaller size and a lower interconnection cost. The main drawback is the increased effect of the substrate noise on the interface electronics [Ast04]. For this purpose, new guarding techniques, which separate the sensitive ULP read-out electronics from the noise generating digital core, should be explored.

- The battery supply of the autonomous sensor node can be replaced by energy scavengers with conversion electronics. These electronics convert the

energy from the scavengers into a reliable supply voltage. They can be integrated with the GSIC (low cost) or implemented in a special technology (higher conversion efficiency).

- The narrowband communication front-end (NORDIC chip and folded dipole antenna) can be replaced by an Ultra Wide Band solution. This would reduce the power consumption significantly.
- The drift in autonomous sensor nodes has to be studied. New algorithms should separate the sensor signal from the long term drift. These algorithms are able to adapt the interface settings of the GSIC (optimal settings) and to digitally compensate for the sensor drift.

References

[Abi83] A. Abidi and R. G. Meyer, "Noise in relaxation oscillators", *IEEE Journal of Solid-State Circuits*, SC-18(6):794–802, 1983.

[Ada86] R. Adams, "Design and implementation of an audio 18 bit analog-to-digital converter using oversampling techniques", *Journal of Audio Engineering Society*, pages 153–166, 1986.

[AMI] AMIS, *AMIS-52100, Datasheet*, http://www.amis.com.

[Ami00] R. Amirtharaja, S. Meninger, J. O. Mur-Miranda, A. Chandrakasan, and J. Lang, "A micropower programmable dsp powered using a mems based vibration to electric energy converter", In *Proceedings IEEE International Solid-State Circuits Conference*, pages 362–363, 2000.

[Ana] AnalogDevices, *ADXL202E, Datasheet and application note: Minimizing power consumption of iMEMS accelerometer*, http://www.analog.com.

[Arm00] C. Arm, J.-M. Masgonty, and C. Piguet, "Double latch clocking scheme for low power ip cores", In *Integrated Circuit Design Power and Timing Modeling, Optimization and Simulation (PATMOS)*, pages 217–224, 2000.

[Asa98] G. Asada, M. Dong, T. S. Lin, F. Newberg, G. Pottie, and W. J. Kaiser, "Wireless integrated network sensors: low power systems on a chip", In *Proceedings of European solid-state circuit conference (ESSCIRC)*, pages 9–16, 1998.

[Ast04] A. Astaras, S. P. Beaumont, T. B. Tang, A. F. Murray, L. Wang, and D. S. R. Cumming, "Noise analysis on integrated multisensor microsystems", In *Proceedings IEEE Sensors Conference*, pages 995–998, 2004.

[Bak98] R. Baker, H. Li, and D. Boyce, *CMOS circuit design, layout and simulation*, chapter 26, pages 686–691, IEEE Press, 1998.

[Bak00] A. Bakker and J. Huijsing, *High-accuracy CMOS smart temperature sensors*, Kluwer Academic Publishers, 2000.

[Bao00] M. Bao, H. Yang, H. Yin, and S. Shen, "Effects of electrostatic forces generated by the driving signal on capacitive sensing devices", *Sensors and Actuators A*, 84:213–219, 2000.

[Ben48] W. Bennet, "Spectra of quantized signals", *Bell Syst. Tech. J.*, BSTJ-27:446–472, 1948.

[Bos88] B. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters", *IEEE Journal of Solid-State Circuits*, 23(6):1298–1308, 1988.

[Cat04] M. Catrysse, *Wireless power and data transmission for implantable and wearable monitoring systems*, PhD thesis, Katholieke Universiteit Leuven, 2004.

[Cha00] S. Chatzandroulis, D. Tsoulakas, and P. A. Neukomm, "A miniature pressure system with a capacitive sensor and a passive telemetry link for use in implantable applications", *IEEE Journal of Microelectromechanical systems*, 9(1):18–23, 2000.

[Cha02] A. V. Chavan and K. D. Wise, "A monolithic fully integrated vacuum sealed cmos pressure sensor", *IEEE Transactions on Electron Devices*, 49(1):164–169, 2002.

[Che99] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous time sigma-delta modulators", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, 46(6):661–676, 1999.

[Cla03] W. Claes, M. De Cooman, W. Sansen, and R. Puers, "A 136 μw/channel autonomous strain-gauge datalogger", *IEEE Journal of Solid-State Circuits*, 38(12):2280–2287, 2003.

[Col] Colibrys, *MS7002, Datasheet*, http://www.colibrys.com.

[Coo05] J. Coosemans and R. Puers, "An autonomous bladder pressure monitoring system", *Sensors and Actuators A*, 123–124:155–161, 2005.

[Cra90] S. B. Crary, W. G. Baer, J. C. Cowles, and K. D. Wise, "Digital compensation of high-performance silicon pressure transducers", *Sensors and Actuators A*, 21–23:70–72, 1990.

[DB02] D. De Bruyker, *Intelligent silicon pressure sensors*, PhD thesis, Katholieke Universiteit Leuven, 2002.

[Des05] G. Despesse, T. Jager, J. Chaillout, J. Léger, and S. Basrour, "Design and fabrication of a new system for vibration energy harvesting", In *Proceedings of Ph.D. research in Microelectronics and Electronics conference (PRIME)*, volume 1, pages 199–202, 2005.

[DG96] B. De Geeter, O. Nys, and J.-P. Bardyn, "A wide temperature range micropower sensor interface circuit", In *Proceedings of European solid-state circuit conference (ESSCIRC)*, pages 136–139, 1996.

[Egg00] T. Eggers, C. Marschner, B. Clasbrummel, R. Laur, J. Binder, K. Takahata, and Y. Gianchandani, "Advanced hybrid integrated low-power telemetric pressure monitoring system for biomedical applications", In *mems*, pages 329–334, 2000.

[Enz96] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization", *Proceedings of the IEEE*, 84(11):1584–1614, 1996.

[Fee91] O. Feely and L. O. Chua, "The effect of integrator leak in sigma delta modulation", *IEEE Transactions on Circuits and Systems*, 38:1293–1305, 1991.

[Fis82] J. H. Fischer, "Noise sources and calculation techniques for switched capacitor filters", *IEEE Journal of Solid-State Circuits*, SC-17(8):742–752, 1982.

[Fre98] P. J. French and P. M. Sarro, "Surface versus bulk micromachining: the contest for suitable applications", *Journal of Micromechanics and microengineering*, 8:45–53, 1998.

[Har99] R. Harjani, R. Heineke, and F. Wang, "An integrated low-voltage class ab cmos ota", *IEEE Journal of Solid-State Circuits*, 34(2):134–142, 1999.

[Hos97] B. Hosticka, *Integrated sensor systems in CMOS technology*, pages 219–241, Analog Circuit Design, W. Sansen, J. Huijsing, R. J. van de Plassche (eds.) Kluwer Academic Publishers, 1997.

[Hua03] Q. Huang, M. Qin, Z. Zhang, M. Zhou, L. Gu, H. Zhu, D. Hu, Z. Hu, G. Xu, and Z. Liu, "Weather station on a chip", In *Proceedings IEEE Sensors Conference*, pages 1106–1113, 2003.

[Ing97] M. Ingels and M. Steyaert, "Design strategies and decoupling techniques for reducing the effects of electrical interference in mixed-mode ic's", *IEEE Journal of Solid-State Circuits*, 32(7):1136–1141, 1997.

[Jac03] P. Jacobs, J. Janssens, T. Geurts, and J. Crols, "A 0.35μm cmos fractional-n transmitter for 315/433/868/915 mhz ism applications", In *Proceedings of European solid-state circuit conference (ESSCIRC)*, pages 425–428, 2003.

[Jes00] P. G. A. Jespers, *D to A and A to D architectures, analysis and simulation*, chapter 7, pages 423–427, Oxford University Press, 2000.

[Joh97] D. A. Johns and K. Martin, *Analog integrated circuit design*, pages 423–427, John Wiley & Sons, 1997.

[Kaj02] T. Kajita, U. K. Moon, and G. Temes, "A two chip interface for a mems accelerometer", *IEEE Transactions on Instrumentation and Measurement*, 51(4):853–858, 2002.

[Kan00] U. Kang and K. D. Wise, "A high-speed capacitive humidity sensor with on-chip thermal reset", *IEEE Transactions on Electron Devices*, 47(4):702–710, 2000.

[Kha03] Q. A. Khan, S. K. Wadhwa, and K. Misri, "Low power startup circuits for voltage and current reference with zero steady state current", In *ISLPED*, pages 184–188, 2003.

[Kol04] C. Kolle, W. Scherr, D. Hammerschmidt, G. Pichler, M. Motz, B. Schaffer, B. Forster, and U. Ausserlechner, "Ultra low power monolithically integrated capacitive pressure sensor for tire pressure monitoring", In *Proceedings IEEE Sensors Conference*, pages 244–247, 2004.

[Kul03] H. Kulah, *Closed-loop electromechanical sigma-delta microgravity accelerometers*, PhD thesis, University of Michigan, 2003.

[Kul06] H. Kulah, J. Chae, N. Yazdi, and K. Najafi, "Noise analysis and characterization of a sigma-delta capacitive microaccelerometer", *IEEE Journal of Solid-State Circuits*, 41(2):352–361, 2006.

[Kwa91] T. Kwan and K. Martin, "An adaptive analog continuous time cmos biquadratic filter", *IEEE Journal of Solid-State Circuits*, 26:859–867, 1991.

[Lac03] J. Laconte, V. Wilmart, J.-P. Raskin, and D. Flandre, "A high-sensitivity capacitive humidity sensor using 3-layer patterned polyimide sensing film", In *Proceedings IEEE Sensors Conference*, pages 106–107, 2003.

[Lam83] K. K. Lam and M. A. Copeland, "Noise cancelling switched-capacitor filtering technique", *IEE Electronics Letters*, 19:810–811, 1983.

[Lap96] D. Lapadatu, M. De Cooman, and R. Puers, "A double-sided capacitive miniaturized accelerometer based on photovoltaic etch-stop technique", *Sensors and Actuators A*, 53:261–266, 1996.

[Lem99] M. Lemkin and B. Boser, "A three axis micromachined accelerometer with a cmos position sense interface and digital offset trim electronics", *IEEE Journal of Solid-State Circuits*, 34(4):456–468, 1999.

[Leo05] V. Leonov, P. Fiorini, S. Sedky, T. Torfs, and C. Van Hoof, "Thermoelectric mems generators as a power supply for a body area network", In *Dig. Int. Conf. on Solid-State Sensors and Actuators (Transducers)*, pages 291–294, 2005.

[Li00] X. Li and G. C. M. Meijer, "Elimination of shunting conductance effects in a low cost capacitive sensor interface", *IEEE Transactions on Instrumentation and Measurement*, 49:531–534, 2000.

[Li02] X. Li and G. C. M. Meijer, "An accurate interface for capacitive sensors", *IEEE Transactions on Instrumentation and Measurement*, 51(5):935–939, 2002.

[Mar87] K. Martin, L. Oczolak, Y. S. Lee, and G. Temes, "A differential switched-capacitor amplifier", *IEEE Journal of Solid-State Circuits*, 22(1):104–106, 1987.

[Mas98] A. Mason, N. Yazdi, A. V. Chavan, K. Najafi, and K. D. Wise, "A generic multielement microsystem for portable wireless applications", *Proceedings of the IEEE*, 86(8):1733–1746, 1998.

[Mei86] G. C. M. Meijer, "Thermal sensors based on transistors", *Sensors and Actuators A*, 10:103–125, 1986.

[Mei02] G. C. M. Meijer and X. Li, "Smart sensor interface electronics", In *Proceedings of the 23rd international conference on microelectronics (MIEL)*, pages 106–107, 2002.

[Mid89] S. Middelhoek and S. Steigerwald-Audet, *Silicon sensors*, Academic Press, London, 1989.

[Nor] Nordic, *nRF24E1, Datasheet*, http://www.nordicsemi.com.

[Per94] J.-F. Perotto, C. Lamothe, C. Arm, C. Piguet, E. Dijkstra, S. Fink, E. Sanchez, and J.-P. Wattenhofer, "An 8-bit multitask micropower risc core", *IEEE Journal of Solid-State Circuits*, 29(29):986–991, 1994.

[Pet06] V. P. Petkov and B. Boser, "High-order electromechanical sigma delta modulation in micromachined inertial sensors", *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, 53(5):1016–1022, 2006.

[Pue90] R. Puers, E. Peeters, A. Van Den Bossche, and W. Sansen, "A capacitive pressure sensor with low impedance output and active suppression of parasitic effects", *Sensors and Actuators A*, 21–23:108–114, 1990.

[Pue93] R. Puers, "Capacitive sensors: when and how to use them", *Sensors and Actuators A*, 37–38:93–105, 1993.

[Pue96] R. Puers and D. Lapadatu, "Electrostatic forces and their effects on capacitive mechanical sensors", *Sensors and Actuators A*, 56:203–210, 1996.

[Pue97] R. Puers and P. Wouters, "Adaptable interface circuits for flexible monitoring of temperature and movement", *Journal of Analog Integrated Circuits and Signal Processing*, 14:193–206, 1997.

[Pue99] R. Puers, "Sensor, sensor interfacing and front-end data management for stand-alone microsystems", *Journal of Micromechanics and microengineering*, 9:R1–R7, 1999.

[Pue00] R. Puers, M. Catrysse, G. Vandevoorde, R. J. Collier, E. Louridas, F. Burny, M. Donkerwolcke, and F. Moulart, "A telemetry system for the detection of hip prosthesis loosening by vibration analysis", *Sensors and Actuators A*, 85:42–47, 2000.

[Rab02] J. Rabaey, J. Ammer, T. Karalar, S. Li, B. Otis, M. Sheets, and T. Tuan, "Picoradios for wireless sensor networks: the next challenge in ultra low power design", In *Proceedings IEEE International Solid-State Circuits Conference*, pages 200–361, 2002.

[Rie93] F. R. Riedijk, *Integrated smart sensors with digital bus interface*, PhD thesis, Technische Universiteit Delft, 1993.

[Ryc05] J. Ryckaert, C. Desset, A. Fort, M. Badaroglu, V. De Heyn, P. Wambacq, G. Van der Plas, S. Donnay, B. Van Poucke, and B. Gyselinckx, "Ultra-wideband transmitter for low power wireless body area networks: design and evaluation", *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, 52(12):2515–2525, 2005.

[San82] W. Sansen, "On the integration of an internal human conditioning system", *IEEE Journal of Solid-State Circuits*, 17:513–521, 1982.

[San94] W. Sansen and K. R. Laker, *Design of analog integrated circuits and systems*, McGraw-Hill, 1994.

[Sei90] H. Seidel, H. Riedel, R. Kolbeck, G. Muck, W. Kupke, and M. Koniger, "Capacitive silicon accelerometer with highly symmetrical design", *Sensors and Actuators A*, 21:312–315, 1990.

[Sel97] A. Selvakumar and K. Najafi, "A high-sensitivity z-axis capacitive silicon microaccelerometer with a torsional suspension", *IEEE Journal of Microelectromechanical systems*, 7(2):192–200, 1997.

[ST] ST, *LIS3LV02DQ, Datasheet*, http://www.st.com.

[Ste03] B. G. Steele, B. Belza, K. Cain, C. Warms, J. Coppersmith, and J. Howard, "Bodies in motion: monitoring daily activity and exercise with motion sensors in people with chronic pulmonary disease", *Journal of Rehabilitation Research & Development*, 40(5):45–58, 2003.

[Ste05] T. Sterken, P. Fiorini, and R. Puers, "Parametrical study of miniature generators for large motion applications", In *Proceedings of Eurosensors XIX*, pages MC1–MC2, 2005.

[Tan02] T. B. Tang, E. A. Johannessen, L. Wang, A. Astaras, M. Ahmadian, A. F. Murray, J. M. Cooper, S. P. Beaumont, B. W. Flynn, and D. S. R. Cumming, "Toward a miniature wireless integrated multisensor microsystem for industrial and biomedical applications", *IEEE Sensors Journal*, 2(6):628–635, 2002.

[Tay00] F. E. H. Tay, J. Xu, and V. J. Logeeswaran, "A differential low-g microaccelerometer with mg resolution", *Sensors and Actuators A*, 86:46–51, 2000.

[Tor04] T. Torfs, S. Sanders, C. Winters, S. Brebels, and C. Van Hoof, "Wireless network of autonomous environmental sensors", In *Proceedings IEEE Sensors Conference*, volume 2, pages 923–926, 2004.

[VDG96] F. M. L. Van Der Goes, *Low-cost smart sensor interfacing*, PhD thesis, Technische Universiteit Delft, 1996.

[VTI] VTI, *SCP1000-D01, Datasheet*, http://www.vti.fi.

[Wak89] M. Wakayama and A. Abidi, "A 30 mhz low-jitter high-linearity cmos voltage-controlled oscillator", *IEEE Journal of Solid-State Circuits*, 24(2):325–330, 1989.

[Wan98] B. Wang, T. Kajita, T. Sun, and G. Temes, "High accuracy circuits for on-chip capacitive ratio testing and sensor readout", *IEEE Transactions on Instrumentation and Measurement*, 47(1):16–20, 1998.

[Wan00] G. Wang and G. C. M. Meijer, "The temperature characteristics of bipolar transistors fabricated in cmos technology", *Sensors and Actuators A*, 87:81–89, 2000.

[War01] B. A. Warneke, M. Last, B. Leibowitz, and K. S. J. Pister, "Smart dust: communicating with a cubic-millimeter computer", *IEEE Computer Magazine*, pages 44–51, 2001.

[War03] B. A. Warneke, *Ultra-low energy architectures and circuits for cubic millimeter distributed wireless sensor networks*, PhD thesis, University of California at Berkeley, 2003.

[Won04] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Naas, "A very low power cmos mixed signal ic for implantable pacemaker applications", *IEEE Journal of Solid-State Circuits*, 39(12):2446–2456, 2004.

[Wou95] P. Wouters, *Intelligent and low power sensor interface systems for biotelemetry applications*, PhD thesis, Katholieke Universiteit Leuven, 1995.

[Yaz98] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors", *Proceedings of the IEEE*, 86(8):1640–1659, 1998.

[Yaz00] N. Yazdi, A. Mason, K. Najafi, and K. D. Wise, "A generic interface chip for capacitive sensors in low-power multi-parameter microsystems", *Sensors and Actuators A*, 84:351–361, 2000.

[Yaz03] N. Yazdi and K. Najafi, "A high-sensitivity silicon accelerometer with a folded-electrode structure", *IEEE Journal of Microelectromechanical systems*, 12(4): 479–486, 2003.

[Yaz04] N. Yazdi, H. Kulah, and K. Najafi, "Precision readout circuits for capacitive microaccelerometers", In *Proceedings IEEE Sensors Conference*, pages 28–31, 2004.

[Yin92] G. M. Yin, F. Op 't Eynde, and W. Sansen, "A high-speed cmos comparator with 8-b resolution", *IEEE Journal of Solid-State Circuits*, 27:208–211, 1992.

[Yos97] Y. Yoshii, A. Nakajo, H. Abe, K. Ninomiya, H. Miyashita, N. Sakuri, M. Kosuge, and S. Hao, "1 chip integrated software calibrated cmos pressure sensor with mcu, a/d convertor, d/a convertor, digital communication port, signal conditioning circuit and temperature sensor", In *Dig. Int. Conf. on Solid-State Sensors and Actuators (Transducers)*, pages 1485–1488, 1997.

[You98] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Low-voltage class ab buffers with quiescent current control", *IEEE Journal of Solid-State Circuits*, 33(6): 915–920, 1998.

Index