HYBRID SOLID-STATE/FLUIDIC COOLING FOR THERMAL MANAGEMENT OF ELECTRONIC COMPONENTS

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HYBRID SOLID-STATE/FLUIDIC COOLING FOR THERMAL MANAGEMENT OF ELECTRONIC COMPONENTS

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To

My loving parents, Rajendra and Meena

and

My siblings, Shweta and Vishal

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LIST OF SYMBOLS AND ABBREVATIONS

A — Area (m^2)

A_{base} — Microchannel heat sink base area (m^2)

A_c — Cap layer cross section area (m^2)

A_m — SLC top metal layer cross section area (m^2)

A_{ml} — Metal lead cross section area (m^2)

A_{tot} — Total surface area of the microchannel heat sink (m^2)

C^{th} — Thermal capacitance (J/K)

c_p — Specific heat (J/kg-K)

E — Electric field (V/m)

h — Convective heat transfer coefficient (W/m^2K)

h_{base} — Convective heat transfer coefficient at the base of the substrate (W/m^2K)

$h_{channel}$ — Convective heat transfer coefficient inside the microchannel heat sink (W/m^2K)

h_{eff} — Effective heat transfer coefficient between metal lead and substrate (W/m^2K)

I — SLC activation current (A)

J — Joule heating (W)

k — Thermal conductivity (W/m-K)

l — Length (m)

P — Perimeter (m)

P_{MC} — Peltier cooling at metal-cap interface (W)

P_{BS} Peltier cooling at buffer substrate interface (W)

Q_c Heat load on the SLC (W)

Q_{gnd} Heat generated at the ground electrode (W)

Q_p Parasitic heat transfer from ground electrode to superlattice cooler (W)

Q_{ml} Heat transport from metal lead to the top of superlattice layer (W)

q Heat flux (W/m^2)

q''' Volumetric heat generation (W/m^3)

R^e Electrical resistance of superlattice layer (Ω)

R'^e_{con} Specific electrical contact resistance (Ω m^2)

R^{th} Thermal resistance between heat sink and superlattice (K/W)

R^{th}_{gh} Thermal resistance between ground electrode and microchannel heat sink (K/W)

R^{th}_{gs} Thermal resistance between ground electrode and superlattice cooler (K/W)

S Seebeck coefficient (V/K)

T Temperature (K)

T_c Temperature at the cold side of the superlattice cooler (K)

T_{in} Initial temperature (K)

$T_{ml,m}$ Temperature at the metal lead and SLC top metal layer interface (K)

T_s Steady state temperature (K)

T_∞ Ambient temperature (K)

t Time (s)

U	Uncertainty
V	Voltage (V)
V_c	Volume of cap layer (m^3)
w	Width (m)
ZT	Figure of merit
Δg	Distance between the ground electrode and superlattice cooler (m)
Δs	Distance between superlattice coolers (m)
ΔT	Temperature difference between cold side of the SLC and heat sink (K)

Greek symbols

α	Thermal diffusivity (m^2/s)
χ	Amount of Joule heating transferred back to the cold side of the SLC
η	Fin efficiency
ε	Electrical permittivity (F/m)
μ	Charge mobility (m^{2}s^{-1}V^{-1})
λ	Thickness (m)
ϕ	Non-dimensional temperature
ψ	Fin thermal resistance (K/W)
Π	Peltier coefficient (V)
ρ	Density (kg/m^3)
σ	Electrical conductivity ($\Omega^{-1}m^{-1}$)
τ^{th}	Thermal time constant (s)
θ	Excess temperature (K), defined as $T - T_\infty$

Subscripts

b	Buffer layer
bs	Buffer substrate interface
c	Cap layer
cm	Charge migration
con	Contact
cond	Conduction
conv	Convection
cr	Charge relaxation
eff	Effective
gnd	Ground electrode
ins	Insulation layer
m	Metal layer
mc	Metal-cap interface
ml	Metal lead layer
sl	Superlattice layer
sp	Spreading
sub	Substrate

Superscripts

e	Electrical
th	Thermal

Abbreviations

COP Coefficient of performance

CPD Cooling power density

SLC Superlattice cooler

TEC Thermoelectric cooler

SUMMARY

A novel hybrid cooling scheme is proposed to remove non-uniform heat flux in real time from the microprocessor. It consists of a liquid cooled microchannel heat sink to remove the lower background heat flux and superlattice coolers to dissipate the high heat flux present at the hotspots. Superlattice coolers (SLC) are solid-state devices, which work on thermoelectric effect, and provide localized cooling for hotspots. SLCs offer some unique advantage over conventional cooling solutions. They are CMOS compatible and can be easily fabricated in any shape or size. They are more reliable as they don't contain any moving parts. They can remove high heat flux from localized regions and provide faster time response.

Experimental devices are fabricated to characterize the steady-state, as well as transient performance, of the hybrid cooling scheme. Performance of the hybrid cooling scheme has been examined under various operating conditions. Effects of various geometric parameters have also been thoroughly studied. Heat flux in excess of 300 W/cm^2 has been successfully dissipated from localized hotspots. The maximum cooling at the hotspot is observed to be more than 6 K.

Parasitic heat transfer to the superlattice cooler drastically affects its performance. Thermal resistance between ground electrode and heat sink, as well as thermal resistance between ground electrode and superlattice cooler, affect the parasitic heat transfer from to the superlattice cooler. Two different test devices are fabricated specifically to examine the effect of both thermal resistances.

An electro-thermal model is developed to study the thermal coupling between two superlattice coolers. Thermal coupling significantly affects the performance of an array of

superlattice coolers. Several operating parameters (activation current, location of ground electrode, choice of working fluid) affect thermal coupling between superlattice coolers, which has been computationally as well as experimentally studied. Transient response of the superlattice cooler has also been examined through experiments and computational modeling. Response time of the superlattice cooler has been reported to be less than 35 μs.

CHAPTER 1: INTRODUCTION

This chapter provides the motivation for the development of new cooling technology for thermal management of future electronic components with localized hotspots. A brief description of current state of the art cooling technologies has been provided and their pros and cons are discussed. A novel hybrid cooling scheme is proposed to overcome the limitations of the current cooling technologies. In the end, potential issues and challenges in the implementation of the hybrid cooling scheme are discussed.

1.1. Motivation

The need to increase the performance and decrease the cost of the microprocessor has led semiconductor industry to continuously decrease the feature size and pack more and more transistors on a microprocessor. This has not only increased the average heat flux dissipated by the microprocessor, but also led to localized regions of very high heat fluxes, called hotspots. Heat flux at these localized hotspots can be five to ten times higher than the average [1]. If conventional cooling approaches are used for an entire microprocessor, temperature at the hotspots can be significantly higher than the average temperature of the die. This results in temperature gradients and thermal stresses, which adversely impact reliability of the die. Even though the *International Technology Roadmap for Semiconductors* projects a capping of overall power dissipation by high performance chips, the power dissipated at hotspots is projected to increase. Moreover, the maximum allowable junction temperature for the high performance devices is projected to drop to 75 ºC by 2016 [2], which would reduce the overall thermal budget

and make thermal management even more challenging. This has made hotspot removal one of primary drivers for thermal management of today's ICs.

Moreover, the microprocessor power dissipation map varies during operation depending upon the type of the workload, distribution of the work load, etc. This problem has become more severe due to advent of the multicore and many core processors which allow transferring of the workload from one core to another. Thus, hotspot locations vary in space and time. The dynamically changing power map requires an active cooling solution with a feedback mechanism that will allow the cooling solution to evolve with the power map.

Current state of the art major cooling technologies include air cooling, liquid cooled microchannel heat sink, boiling, jet impingement, spray cooling. All of the above mentioned cooling technologies have their pros and cons. Air cooling has been widely used because of its ease of implementation, low fabrication and operating cost. However, air has poor thermophysical properties and cannot remove high heat flux dissipated by the future microprocessors. Liquid cooling has its advantages as it can provide three orders of magnitude higher heat transfer coefficient compared to the air cooling [3]. However, the penalty has to be paid in terms of increased pressure drop, increased fabrication and operating cost. Moreover, all the cooling technologies mentioned above are inherently designed for uniform heat load and thus are neither capable of providing a global cooling solution for a non-uniform power map nor suitable for addressing the dynamically changing power map.

Thermal management techniques for future electronic components require localized cooling solution at the chip scale for hotspot mitigation combined with global

cooling solution for the average power dissipated by the die. The local cooling solutions should be silicon microfabrication compatible so that it can be easily integrated within the die. Moreover, the cooling solution needs to dynamically adapt to address the microprocessor power map in real time. A new hybrid cooling scheme is proposed to provide thermal management for electronic devices and address the limitations of the current state of the art cooling technologies.

1.2. Current state of the art chip level cooling technologies

Aggressive cooling technologies, which offer higher heat flux removal capabilities, have been developed to remove the power dissipated by the high performance devices. Due to the large volume of literature, it is not possible to discuss all the potential approaches used for thermal management of electronics. Therefore, only liquid cooling technologies which provide higher heat flux removing capability are discussed in this section. Few other novel cooling methods targeted specifically for hotspot heat flux removal are also presented.

1.2.1. Review on single phase convective heat transfer in microchannel heat sink

Tuckerman and Pease [4] used liquid cooled microchannel heat sink to remove 790 W/cm^2 heat flux using water as the working fluid. The microchannel heat sink consisted of parallel channels 50 μm wide and 300 μm deep. The maximum substrate temperature was 94 °C. However, the temperature rise along the heat sink was 71 °C. Moreover, pressure drop was very high (214 kPa) with volumetric flow rate of more than 500 ml/min. Current microscale pump technologies cannot deliver the required flow rate at the pressure drop mentioned above [5].

Thereafter, several optimization studies have been carried out [6-12] to reduce the pressure drop and increase the heat transfer. Knight *et al*. [9] used resistance network analysis to minimize the thermal resistance of the microchannel heat sink for a fixed pressure drop. They found that when pressure drop is small optimal thermal resistance occurs when flow is laminar, whereas, if pressure drop is large, turbulent regime yields optimal thermal resistance. Kleiner *et al*. [10] enhanced the resistance network model by including the longitudinal conduction in the heat sink. They showed inclusion of the longitudinal heat conduction reduces the surface temperature and thus lower the heat sink thermal resistance. Recently, Li *et al*. [12] performed detailed numerical simulation to optimize the heat sink dimensions using three dimensional conjugate heat transfer model. They obtained lowest thermal resistance of 0.15 K/W for pumping power of 0.05 W.

Several variants of microchannel heat sink such as, multiple entry manifolds [13, 14], pin-fins [15-17], wavy channels [18], stacked microchannels [19-21], pulsating flow inside the channels [22, 23], have been used to improve its efficiency. Multiple manifolds have been utilized to reduce the pressure drop while maintaining the low thermal resistance. Harpole *et al*. [14] first demonstrated this concept. Besides lowering the pressure drop, use of multiple manifolds also reduces the temperature non-uniformity across the heat sink. Recently, Colgan *et al*. [13] used multiple entries manifold to keep the channel length short and reduce the pressure drop. They had offset strip fin arrangement inside the microchannel and were able to dissipate close to 275 W/cm^2 of heat flux using single phase forced convection with water as the working fluid while maintaining the junction temperature at 85 °C. However, the heat sink was very complex, difficult to fabricate and implement.

Gong *et al*. [18] used wavy microchannel instead of straight microchannel channels and showed 25% enhancement in the overall performance compared to the straight microchannel heat sink under the same operating conditions. They attributed this enhancement to the secondary flow inside the wavy channels. Xiaojin *et al*. [21] used stacked microchannels to reduce pressure drop while maintain the thermal resistance of the heat sink. They showed that stacking two layers result in more than 50 % reduction in pressure drop, as well as 25 % reduction in overall thermal resistance of the heat sink, compared to the single layer. Persoons *et al*. [22] used pulsating flow inside the microchannel to increase the heat transfer by 40% compared to steady flow. However, it required a pulsator device to allow control over pulsation amplitude and frequency.

1.2.2. Review on two-phase cooling

Two-phase cooling offers various advantages over single phase convective heat transfer. Two-phase cooling provides significant higher heat transfer coefficient compared to single phase. Two-phase heat transfer (boiling) utilizes latent heat of vaporization thus requires lower flow rate. Moreover, two-phase cooling can provide greater temperature uniformity across the die making it favorable for thermal management of electronics. Extensive work has been done to characterize the heat transfer, pressure drop, flow regimes for two-phase cooling [24-34]. Peng *et al*. [34] used the two-phase microchannel and minichannel heat sink to remove heat flux in excess of 200 W/cm^2 with flow rate of 65 ml/min, and pressure drop of less than 34.5 kPa. Corresponding wall superheat was in the range of 30 ^{o}C to 40 ^{o}C. R-113 was used as the working fluid and the CHF value was reported to be 256 W/cm^2 for the microchannel heat sink. Bowers *et al*. [35, 36] used the two-phase microchannel (hydraulic diameter =

510 μm) and mini-channel (hydraulic diameter = 2.54 mm) heat sink. R-113 was used as the working fluid and the flow rate was reported to be less than 95 ml/min for the range of inlet subcooling from 10 °C to 32 °C. The CHF value was reported to be in excess of 200 W/cm^2. Prasher *et al*. [37] studied the characteristic of two-phase heat transfer inside the microchannels in the presence of the hotspots. They compared the performance of two test devices, one with straight channels and the second with cross-linked microchannels. Channels were 700 μm wide, 300 μm deep and 24 mm long. Both devices yield relatively uniform temperature distribution with cross-linked device showing lower temperature than the straight microchannels. They were able to dissipate up to 46 W/cm^2 heat flux with flow rate of 20 ml/min with de-ionized water as the working fluid. Even though boiling offers significantly higher heat transfer coefficient compared to single phase convection there are several issues associated with boiling such as, flow instability, pre-mature dry out, flow and heat mal-distribution [38-40]. Bogojevic *et al*. [41] studied flow boiling instabilities for non-uniform heating. They concluded flow boiling instabilities due to non-uniform heating can lead to greater temperature non-uniformity compared to the single phase.

1.2.3. Review on jet impingement cooling

Beside microchannel heat sink, jet impingement and spray cooling have been used for thermal management of electronics. Jet impingement creates a thin boundary layer just outside the impingement region, thus providing very high heat flux locally. Single phase jet impingement has been investigated experimentally, as well as numerically, by several researchers [42-51]. Steven *et al*. [52] studied single phase, single jet impingement with water as working fluid. They found heat transfer coefficient to be

highest at the stagnation zone and a strong function of the jet velocity. Garimella *et al.* [53] used single phase jet impingement to obtain local heat transfer coefficient as high as 60,000 W/m^2K with FC-77 as the working fluid. Amon *et al*. [54] implemented an array of micro-nozzles for thermal management of a PC notebook. They tested the nozzles with various shapes and sizes. They reported maximum heat flux dissipation of 45 W/cm^2 with HFE-7200 and 50 W/cm^2 with water as the working fluid. Wolf *et al*. [55] used two-phase jet impingement to remove 500 W/cm^2 with wall superheat of 30-40 ºC and de-ionized water as the coolant. The jet velocity was as high as 5 m/s and the surface temperature corresponding to the onset of nucleate boiling was 105 ºC. Nonn *et al*. [56] used 50%-50% volumetric mixture of FC-72 and FC-87 to study the flow boiling over a simulated electronic chip. Using the mixture, shifts the boiling curve to 10 °C - 15 °C lower temperature resulting in reduced chip surface temperature compared to use of pure FC-72. They also concluded that the CHF increases with the jet velocities. Copeland *et al*. [57, 58] conducted experiments with FC-72 using multiple jets. They reported CHF as high as 200 W/cm^2 and concluded for a constant flow rate, CHF increases with increase in the number of nozzles.

1.2.4. Review on spray cooling

Spray cooling provides much uniform temperature distribution [59], which is independent of the heat flux fluctuations [60], compared to jet impingement. Estes *et al*. [60] compared the performance of spray cooling and free jet. Spray cooling delivered much higher CHF values than jet impingement. Yao *et al*. [61] experimentally investigated boiling spray cooling with FC-72 as the coolant. They concluded spray cooling yields more uniform surface temperature than jet impingement. They also

reported much lower boiling incipient superheat compared to the flow boiling. Chow *et al*. [62, 63] demonstrated heat flux as high as 1200 W/cm^2 can be dissipated with low superheat by maintaining an ultra thin layer of coolant on the surface with water as the working fluid. Cader *et al.* [64] conducted various benchmark tests on Intel Xeon 1U server microprocessor. They compared performance of air cooled servers and spray cooled servers. Spray cooled servers showed more than 30% performance enhancement over the air cooled servers with maximum heat flux dissipation of 150 W/cm^2 with wall temperature of 110 ^{o}C. Though both jet impingement and spray cooling can dissipate high local heat flux, the heat transfer performance degrades over larger areas, thus it is not suitable for thermal management of the entire die. Moreover, issues associated with fluid management and device packaging motivates investigation of alternative concepts.

1.2.5. Solid-state cooling

Thermoelectric coolers (TECs) have recently gained interest as the thermal management devices for hotspots. TECs are solid-state devices which work on Peltier effect. They are highly reliable and robust. However due to the low Coefficient of Performance (COP), they are not suitable for the thermal management of the entire chip. Since the total power dissipated from the hotspots is significantly smaller than the power dissipated by the entire chip, TECs have been utilized for the hotspot cooling. Chu *et al*. [65] have provided review of application of thermoelectric coolers for electronics cooling. Venkatasubramanian *et al*. [66, 67] used embedded thermoelectric cooler with footprint area of 2.5 mm x 2.5 mm. They were able to dissipate 27 W while maintaining the temperature at 85 ^{o}C. Maximum temperature drop across the thermoelectric cooler

was reported to be 70 °C. For electronics cooling application, total power dissipated by the thermoelectric cooler is more important factor than temperature drop across the thermoelectric unit [68]. Heat flux dissipation capability of the thermoelectric cooler is inversely proportional to the length of the thermoelectric elements. Shakouri *et al*. [69] have used microfabricated thin-film cooler to provide localized cooling at the hotspots. The thickness of the thermoelectric cooler is of the order of few micrometers. They have reported 600 W/cm^2 heat flux dissipation from 40 µm x 40 µm superlattice cooler. Cohan *et al*. [70] utilized mini thermoelectric cooler (3.6 mm x 3.6 mm) to dissipate 1250 W/cm^2 from 400 µm x 400 µm hotspot. They integrated the mini-TEC at the package level. Similarly, Prasher *et al*. [71] used a micro-thermoelectric cooler to provide 15 °C of cooling at 1300 W/cm^2 hotspot heat flux. TEC was not used to provide localized cooling. Instead, it was implemented at the package level between the heat spreader and the TIM layer. The size of thermoelectric cooler was four orders of magnitude greater than the size of the hotspots. Thus, if more than one hotspot is present or spatial distance between the hotspot is more than the size of the TEC (as can be the case for multicore and many core processors), the cooling performance will decrease significantly.

1.2.6. Additional hotspot thermal management cooling technologies

Narayanan *et al*. [72] used thin film evaporative cooling to demonstrate heat flux removal capability in excess of 500 W/cm^2 from the localized hotspots (250 µm x 250 µm) with surface temperature of 85 °C. The corresponding heat transfer coefficient was 0.2 MW/cm^2. Green *et al*. [73] used micro-constriction to increase the heat transfer locally at the hotspot combined with the air cooled heat sink. They were able to remove

350 W/cm^2 locally from a 100 µm x 100 µm hotspot with surface temperature of 105 °C. However background heat flux was low due to use of air cooled heat sink. The maximum background heat flux removed was 20 W/cm^2 with surface temperature of 80 °C.

1.3. Proposed hybrid cooling scheme

The proposed hybrid cooling scheme combines micro-fluidic and solid-state cooling techniques to exploit their unique advantages, and overcomes challenges associated with each method. It uses a liquid cooled microchannel heat sink to dissipate the background heat flux and solid state devices to remove high heat flux from the localized hotspots. Microchannel heat sink is designed to remove only the uniform background heat flux from the die. It cannot dissipate high heat flux present at the hotspots. To increase the heat transfer at localized hotspots superlattice coolers are used. Superlattice coolers (SLCs) [74, 75] are solid state device, which work on the Peltier effect. When a potential difference is applied across the two electrodes of the superlattice cooler, one electrode is cooled down and the other electrode is heated up. The cold electrode is placed in the proximity of the hotspots. More details on the functionality of the superlattice cooler are presented later. Superlattice coolers are strategically located over the expected locations of the hotspots and are turned on when hotspots are detected. Thus, both background heat flux, as well as hotspots, can be removed without significantly increasing the heat load on the microchannel heat sink.

Figure 1-1 shows schematic of the hybrid cooling scheme. It consists of microchannel heat sink which is modified by fabricating the superlattice coolers at the back side. SLCs are silicon micro-fabrication compatible and hence can be directly

fabricated on the back of the silicon microchannel heat sink. SLCs are fabricated at the expected location of the hotspots. An array of superlattice coolers can be used to manage multiple hotspots, or dynamically shifting hotspots. The hot electrode of SLCs is placed away from the active region of the die. This modified microchannel heat sink is bonded to the die. The working fluid enters the microchannel heat sink through the inlet port, picks up the background heat dissipated by the die, and exits the microchannel through the outlet port. If a hotspot is present, SLCs located in the proximity of the hotspot are activated. This provides localized cold spot and absorbs the heat dissipated by the hotspots. The heat generated at the hot electrode of the SLC is dissipated to the working fluid.

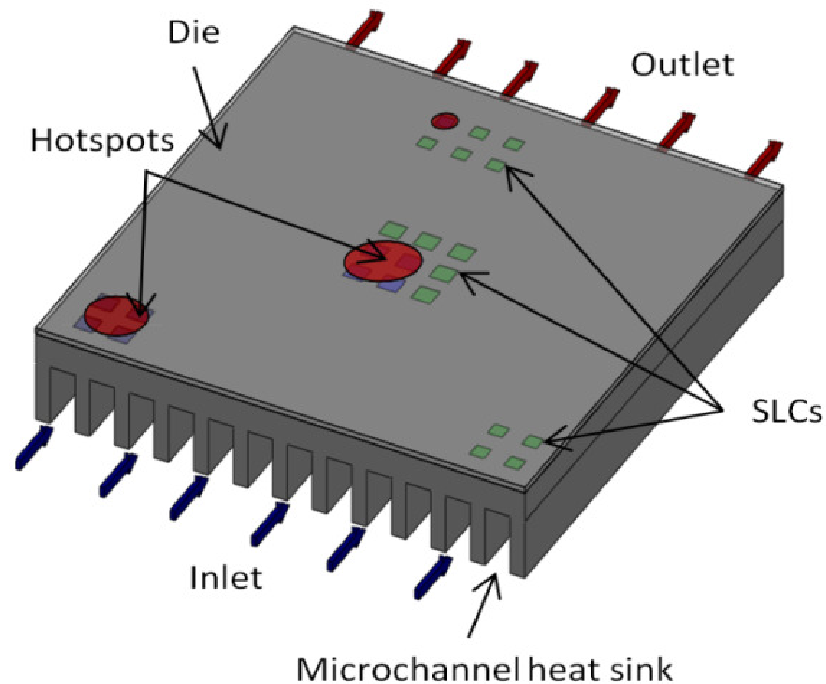


Figure 1-1: Schematic of the proposed hybrid cooling scheme. Small rectangular features show the location of superlattice coolers (green and blue features represent non-activated and activated SLC respectively).

The advantage of the hybrid cooling scheme is that it removes the non-uniform heat flux without overdesigning the heat sink. In the presence of the hotspot, the heat sink has to be designed based on the power dissipated by the hotspot. However, since the hotspot size is very small compared to the die area, the heat sink will have to be overdesigned. Figure 1-2 compares the power requirement for the single phase and the hybrid cooling scheme. Above a certain hotspot heat flux density, power required by single phase microchannel heat sink increases considerably, whereas for hybrid cooling power required increases linearly with the hotspot heat flux. More details on the analysis can be found in [76].

The key features of the hybrid cooling scheme are:

(1) It provides a global cooling solution to address non-uniform heat dissipation from the die.

(2) It can dynamically adapt to address the microprocessor power dissipation map in the real time.

(3) It optimizes utilization of the cooling resources since the microchannel heat sink does not have to be designed for the hotspot heat flux.

(4) It is compatible with silicon micro-fabrication techniques.

(5) It can be integrated into 2D as well as 3D ICs.

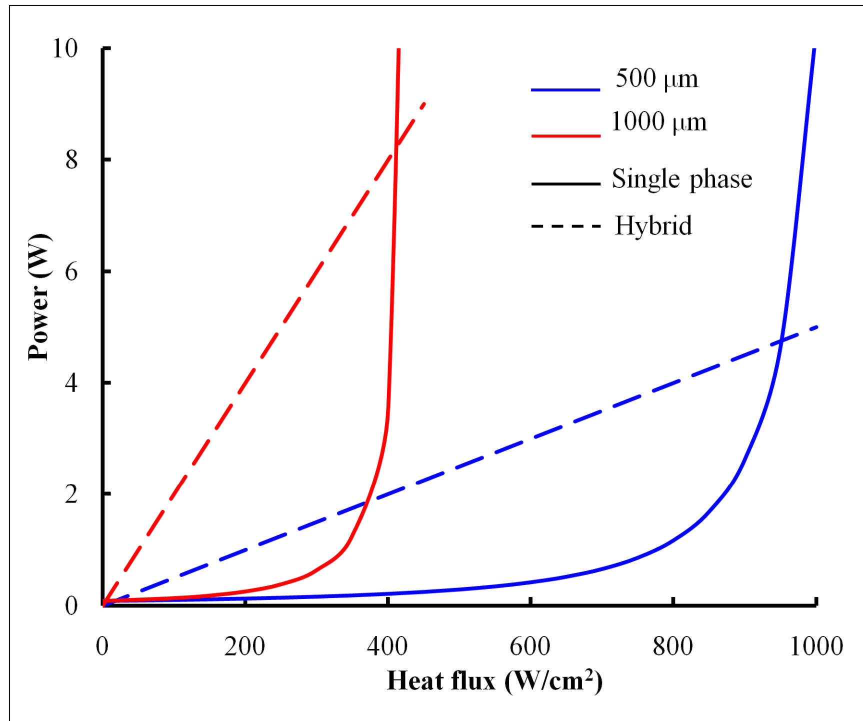
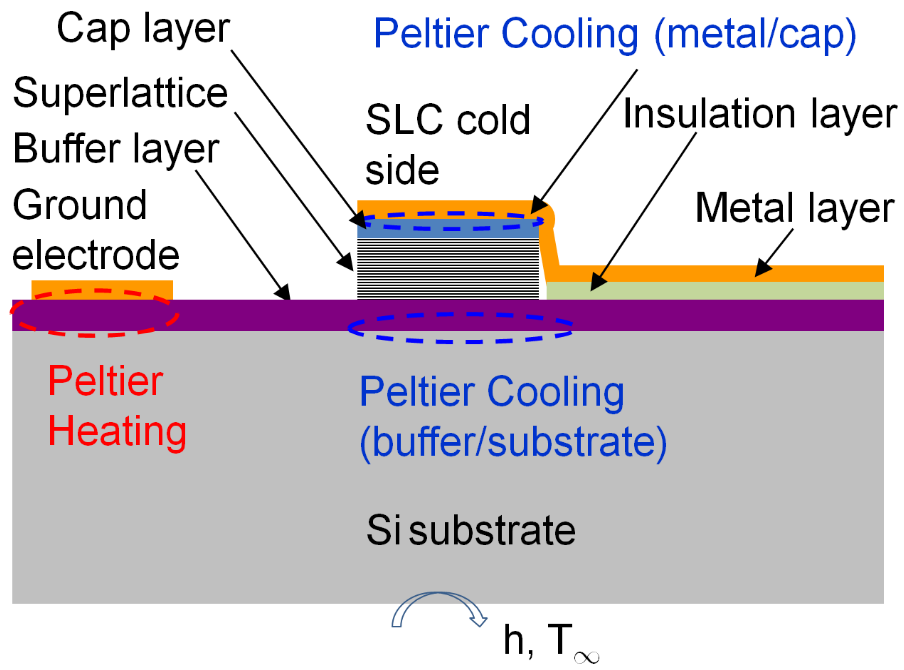


Figure 1-2: Comparison of power requirement for single-phase scheme and hybrid cooling scheme for different hot spot sizes

1.3.1. Superlattice cooler

Superlattice cooler (SLCs) [74, 75] consist of alternate layers of epitaxially grown Si and SiGe (several other materials can be utilized for superlattice fabrication). Each layer is few nanometers thick and the combined structure is few micrometers thick. Like thermoelectric coolers it works on the Peltier effect and converts electrical energy into thermal energy. However, unlike thermoelectric coolers, which work solely on the Peltier effect, SLC also utilizes thermionic emission. Figure 1-3 (a) shows the schematic of the superlattice cooler and Figure 1-3 (b) shows the SEM image of the SLC layers. Superlattice layer acts as a barrier for electrons flowing from cathode to anode. When electric current is applied to the superlattice, only hot electrons from the cathode, which have sufficient energy to cross the barrier, reach the anode. This creates deficiency of hot electrons in the cathode layer, resulting in evaporative cooling at the cathode junction.



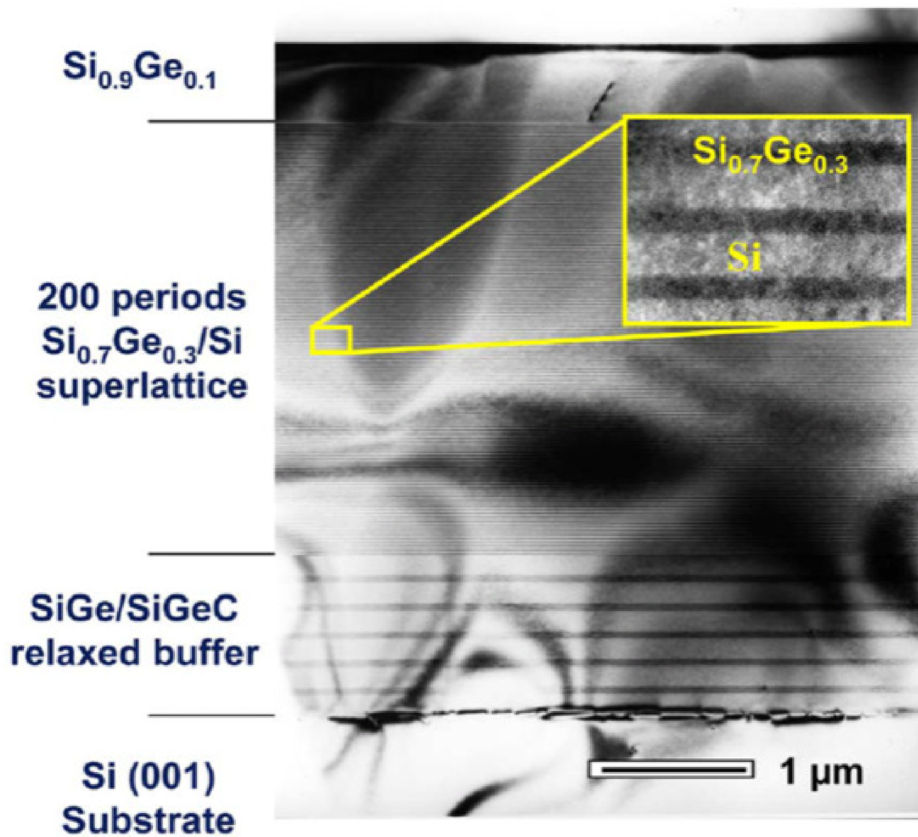


Figure 1-3: (a) Schematic of superlattice cooler showing all the layers in superlattice cooler (top), (b) The SEM image of the SLC layers (bottom* courtesy Dr. Ali Shakouri, UCSC).

At the anode junction, hot electrons reject the heat to the substrate to come into thermal equilibrium, causing heating of the anode junction. Thus, flow of electrons creates a temperature difference, with the higher temperature at the anode side of the superlattice cooler.

Cooling achieved from the SLC is given by [75]:

$$Q = SIT_C - \chi I^2 R^e - \Delta T / R^{th} \tag{1.1}$$

where, Q is the heat load on the SLC, S is the Seebeck coefficient, T_c is the cold side temperature of the SLC, χ is the amount of Joule heating transferred back to the cold side of the SLC, I is the current supplied to the superlattice cooler, R^e is the electrical resistance, $\Delta T\ (= T_{hs} - T_c)$ is the temperature difference between cold side of the SLC and heat sink, and R^{th} is the thermal resistance between the superlattice cooler and heat sink.

The first term in the above equation represents cooling due to the Peltier effect. The Seebeck coefficient is adjusted to account for both thermoelectric as well as thermionic cooling. The second term represents portion of the Joule heating transferred to the cold side of the superlattice cooler. The factor χ is a function of contact area and increases with it. The third term represents the heat transported to the superlattice cooler from the microchannel heat sink.

1.4. Potential issues and challenges in the implementation of the hybrid cooling scheme

1.4.1. Characterization of the hybrid cooling scheme

The performance of the SLC depends upon several geometric parameters (size of SLC, location of ground electrode, optimum spacing between ground electrode and SLC)

as well as operating parameters (SLC operating current, ambient temperature, working fluid). Understanding of how these parameters affect the performance of the SLC is critical for the design and implementation of the hybrid cooling scheme.

1.4.2. Effect of interface and thermal resistance

Heat dissipated at the ground electrode is eventually removed by the microchannel heat sink. However, due to the presence of dielectric and low thermal conductivity materials, significant thermal resistance can be present between the ground electrode and the microchannel heat sink. As thermal resistance increases, the microchannel heat sink will become less effective in removing heat from the ground electrode. Therefore, heat dissipated at the ground electrode will spread into the substrate and transfer to the cold side of the SLC, reducing the performance of the SLC. The effect of thermal resistance on the performance of the SLC needs to be fully characterized.

1.4.3. Thermal coupling among SLCs

The hybrid cooling scheme utilizes an array of SLCs for dynamically changing hotspots or hotspots that are significantly bigger than SLC. However, activating several SLCs in an array can considerable increase the local current density and thus Joule heating. The increase in Joule heating may adversely affect the performance of the SLCs. Therefore, it is important to characterize thermal coupling between the superlattice coolers and determine how the operating and geometric parameters affect thermal coupling.

1.4.4. Transient behavior of the hybrid cooling scheme

One of the key features of the hybrid cooling scheme is that it can dynamically adapt to address the microprocessor power map in the real time. An ideal dynamic cooling solution will evolve with the power map instantaneously, however due to finite thermal mass; any cooling scheme will have some lag. Therefore, understanding of the transient behavior is critical for dynamic thermal management of electronics.

CHAPTER 2: DEVICE DESIGN AND FABRICATION

An experimental test device is fabricated to characterize the hybrid cooling scheme and address the potential issues and challenges in its implementation. As mentioned earlier, hybrid cooling scheme has two major components; microchannel heat sink for the background heat flux removal and superlattice cooler for dissipation of the localized hotspots. Both of these components need to be optimized for optimal operation of the hybrid scheme.

2.1. Design of the microchannel heat sink

Microchannel heat sink is optimized for the minimum pumping power corresponding to fixed power dissipation from the die. Several microchannel optimization studies have been carried out [9-11] in the past for minimum pumping power as well as minimum heat sink to ambient thermal resistance. In this work, microchannel heat sink is optimized for the minimum pumping power under uniform heat load of 100 W/cm^2 using the approach described by Kleiner *et al.* [10]. The flow is assumed to be laminar inside the microchannels, which is justifiable as the Reynolds number is less than 300. Moreover, the longitudinal conduction has been ignored in the analysis. The heat sink base area is assumed to be 10 mm x 10 mm. The fluid inlet temperature is set to 300 K and the maximum chip temperature is limited to 85 °C. These constraint requirements translate to the thermal resistance of 0.58 cm^2K/W. The aspect ratio of the channel and the wall thickness is restricted to 6 and 30 µm, respectively, due to fabrication constraints. The maximum channel height is limited to 350 µm (standard wafer thickness is 500 µm), resulting in at least 150 µm thick base for structural stability.

Figure 2-1 shows required pumping power and rise in the coolant temperature as a function of the hydraulic diameter for various channel aspect ratios. Pumping power is equal to the product of pressure drop and volumetric flow rate and to minimize the pumping power product of these two factors should be minimized. At low hydraulic diameter, heat transfer coefficient is high requiring lower volumetric flow rate for heat removal. However pressure drop, being inversely proportional to fourth power of the hydraulic diameter, is large too. Thus total pumping power is high. As the hydraulic diameter increases, pressure drop decreases. However, heat transfer coefficient reduces too, requiring higher volumetric flow rate for the same heat removal and resulting in higher pumping power. Thus, an optimum hydraulic diameter exits which corresponds to the minimum pumping power. The optimum microchannel dimension is found to be 330 µm x 55 µm, and the optimized pumping power is 84 mW and the corresponding coolant temperature rise is 20 °C.

2.2. Manifold design

Heat transfer and pressure drop inside the microchannel is significantly affected by the flow mal-distribution inside the channels. Manifolds are used to distribute coolant to microchannels, however depending upon the manifold design, coolant is not distributed equally among the channels. Channels with higher volumetric flow rate have lower surface temperature, whereas channel with low volumetric flow rate have higher surface temperature, thus creating temperature gradients along the surface of the microchannel heat sink. Moreover, if the volumetric flow rate is low, boiling can occur inside the microchannel, giving rise to flow instabilities as well as increasing the pressure drop. Jung *et al*. [77] studied the effect of flow mal-distribution on the performance of

single phase heat exchanger. They found that effective NTU decreases by as much as 40% in the presence of flow mal-distribution. Peng *et al*. [78] found the friction factor to be five time lower compared to single channel and the discrepancy was attributed to the flow mal-distribution. Webb [79] has given brief review of the flow mal-distribution investigations for the rectangular microchannel. The author has also proposed effective manifold design to reduce the flow mal-distribution.

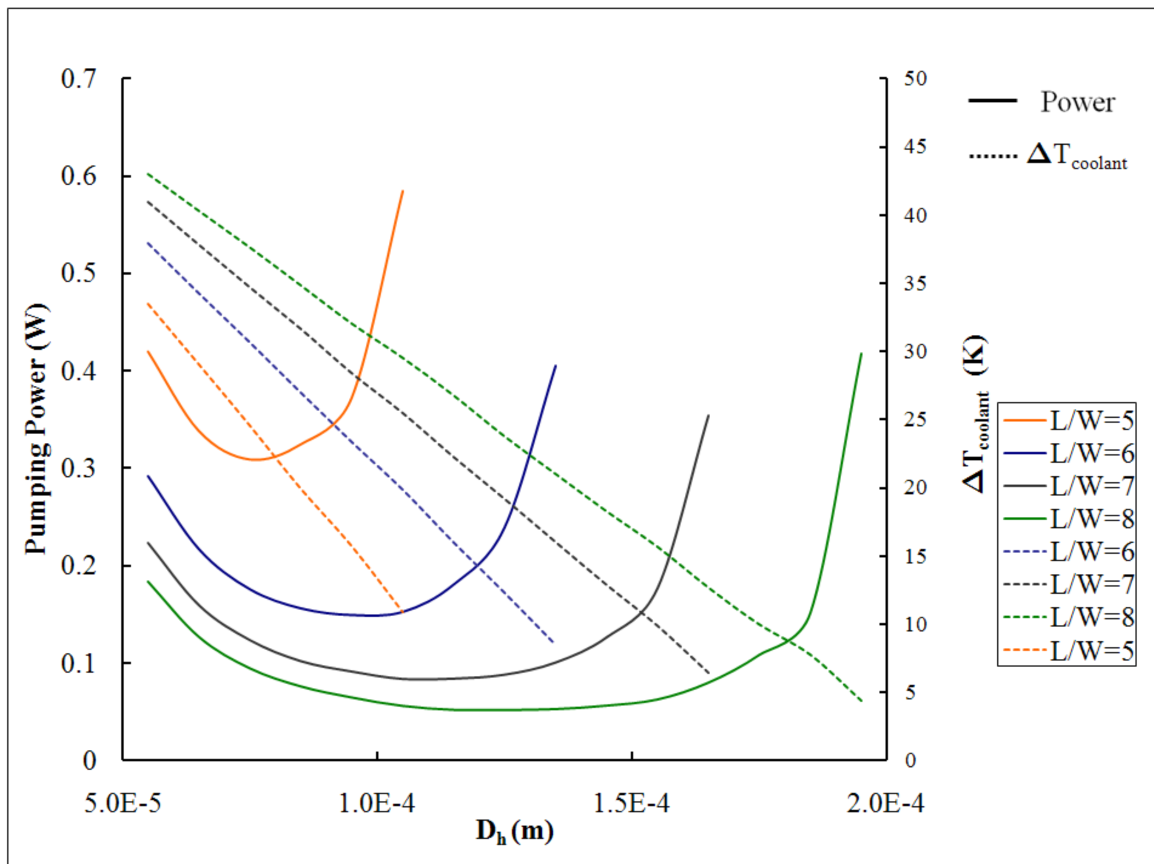


Figure 2-1: Comparison of pumping power and rise in coolant temperature for various aspect ratios as a function of hydraulic diameter.

Flow mal-distribution can be significantly reduced by proper manifold design. In this work, two types of manifold designs are considered as shown in Figure 2-2. First design uses guide vanes to distribute the flow whereas, second design uses oblique

structure. The cross sectional area of the oblique structure is designed such that the pressure at the inlet of the manifold is same throughout the microchannel heat sink. This is done by reducing the cross sectional area of the manifold so that, the velocity of coolant inside the microchannel is uniform. Figure 2-3 compares the flow distribution for two designs. Flow mal-distribution is quite significant when guide vanes are used to distribute the flow. Channels located opposite to guide vanes receive low volumetric

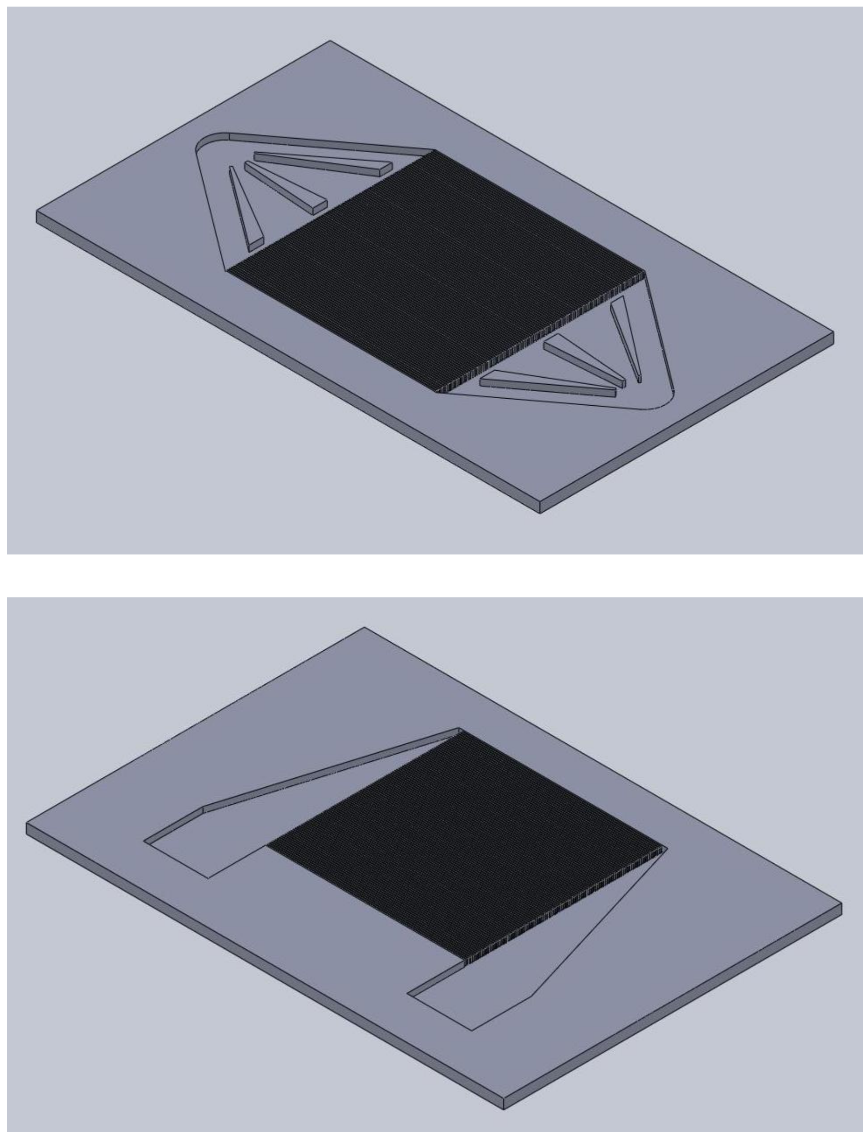


Figure 2-2: CAD model of the vane (top) and oblique (bottom) manifold.

flow, whereas channels located between guide vanes receive high flow rate, giving rise to large flow mal-distribution. Oblique geometry delivers a much uniform flow. Hence in this work, oblique manifolds are used to distribute the coolant to the microchannels.

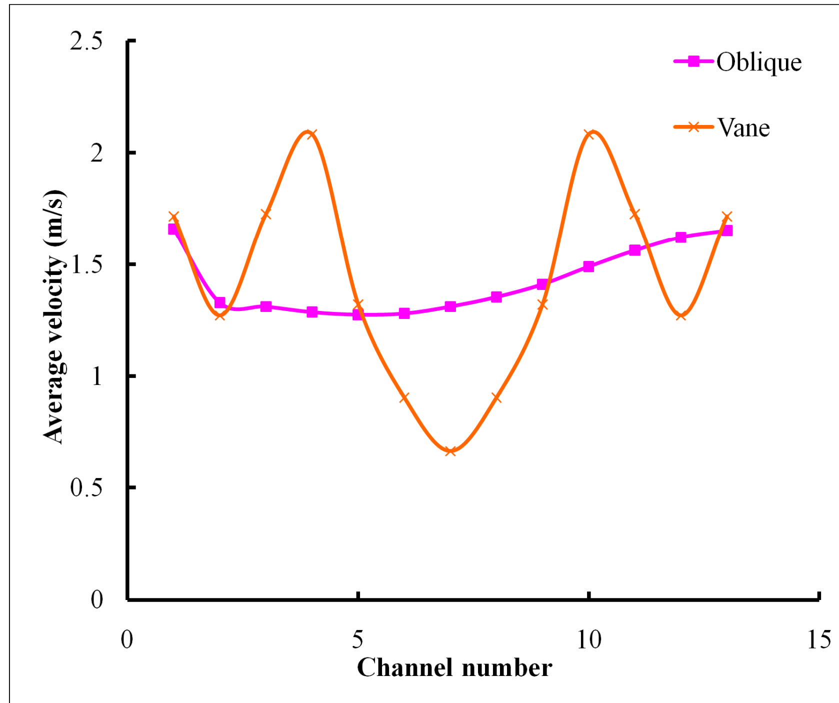
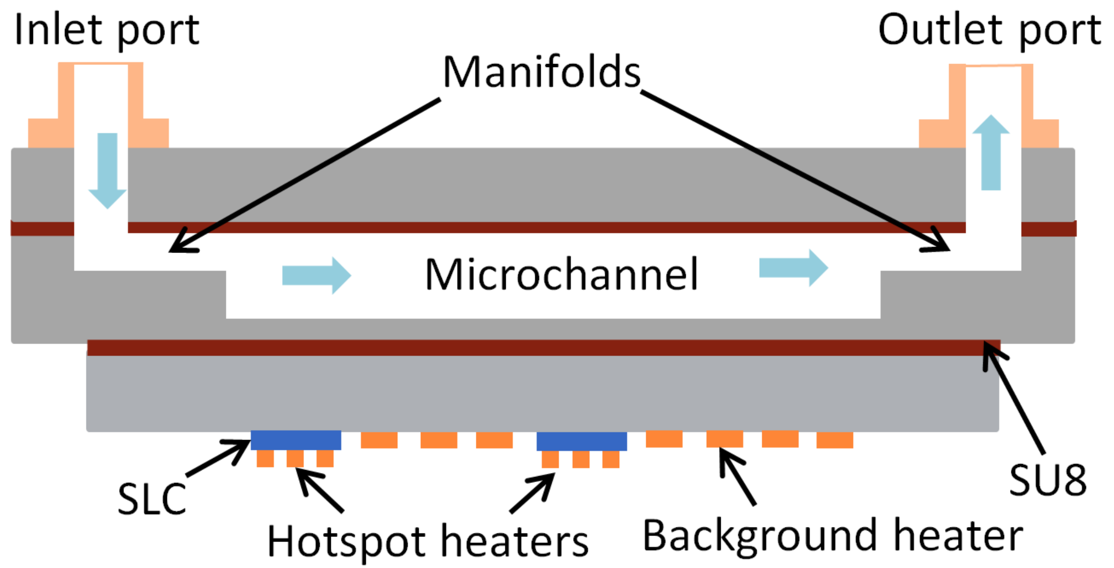


Figure 2-3: Comparison of average velocity inside the channel for two manifold configurations: guide vanes and oblique design.

2.3. Description of the test modules

Two different test modules, one with on-chip microchannels and other with off-chip microchannels, are fabricated to study the effect of interface resistance. Figure 2-4 shows the schematic of both test devices. The major difference between two test devices is in placement of the microchannel heat sink. In off-chip configuration, microchannels and SLCs are fabricated on two separate wafers and bonded together using SU8, whereas on-chip configuration microchannels are etched on the back of the SLC wafer. Fabrication of microchannels on the back of the SLC wafer reduces interface resistance between the ground electrode and microchannel heat sink by eliminating the bonding



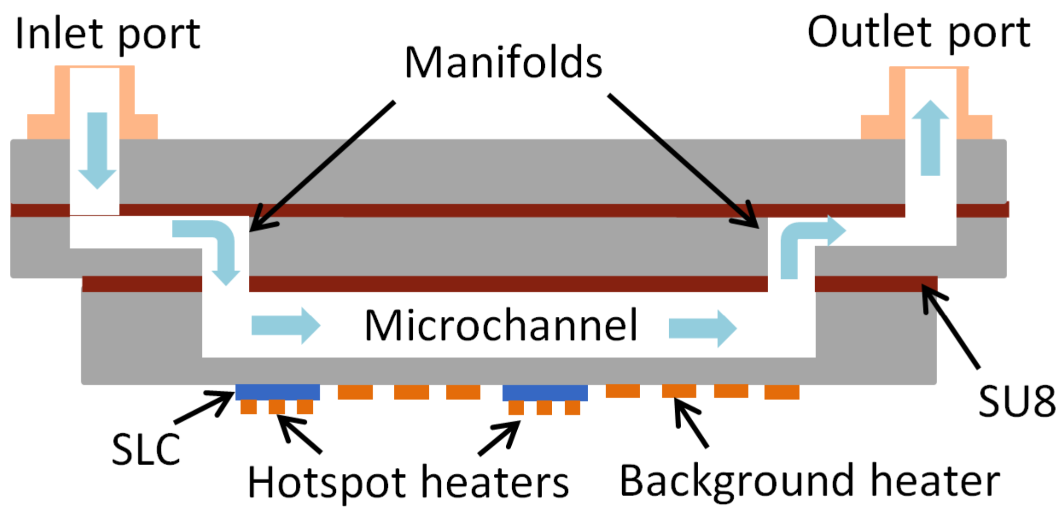


Figure 2-4: Schematic of off-chip and on-chip microchannel configurations.

layer between the two. It also eliminates contact resistance at the bonding interface. Moreover, since microchannels are fabricated by etching silicon, on-chip configuration reduces the physical distance between microchannels and SLC, decreasing the conduction resistance too.

Figure 2-5 shows the CAD model of the test device. A typical device consists of three layers of silicon which are bonded together. The bottom layer contains hotspot heaters, superlattice coolers and background heaters. Hotspot heaters are fabricated on the top of the superlattice coolers but separated by an insulation layer. For on-chip configuration, microchannels are etched at the back of bottom layer to remove the heat dissipated from the die as well as the ground electrode of superlattice cooler. Middle layer contains inlet and outlet manifolds for uniform flow distribution to the microchannels. For off-chip configuration this layer also contains microchannels. Top layer serves as a cover for manifolds as well as contains inlet and outlet ports for fluid entry and exit. Working fluid enters the test device through inlet port and is distributed to the microchannel with the help of manifolds. It removes the heat dissipated by the die and exists through the outlet port.

It should be noted that the manifold can be made on the same layer as microchannel (bottom layer). It eliminates the need to middle layer, which contains manifold, and at the same time significantly reduce the number of steps in the fabrications process. Moreover, assembly is easier too, as only two layers have to be bonded instead of three layers present in current configuration. Despite this, the reason for going with the three layer configuration is the cost of the bottom layer. Bottom layer contains superlattice coolers and is fabricated out of specialized silicon wafer which

contains superlattice layers. Superlattice layers are deposited using the Molecular Beam Epitaxy, which is very time consuming and expensive process. This makes the wafer very expensive, so the size of this layer should be kept as small as possible. Manifolds take lot of space on the die and have to be kept outside the testing area (10mm x 10 mm) so that flow is uniform across the testing area. Making the manifolds in the bottom layer would increase the area of the layer by a factor of two and for this reason they are fabricated on a separate silicon layer. The size of the bottom layer and middle layer is 14 mm x 15 mm and 19 mm x 23 mm, respectively.

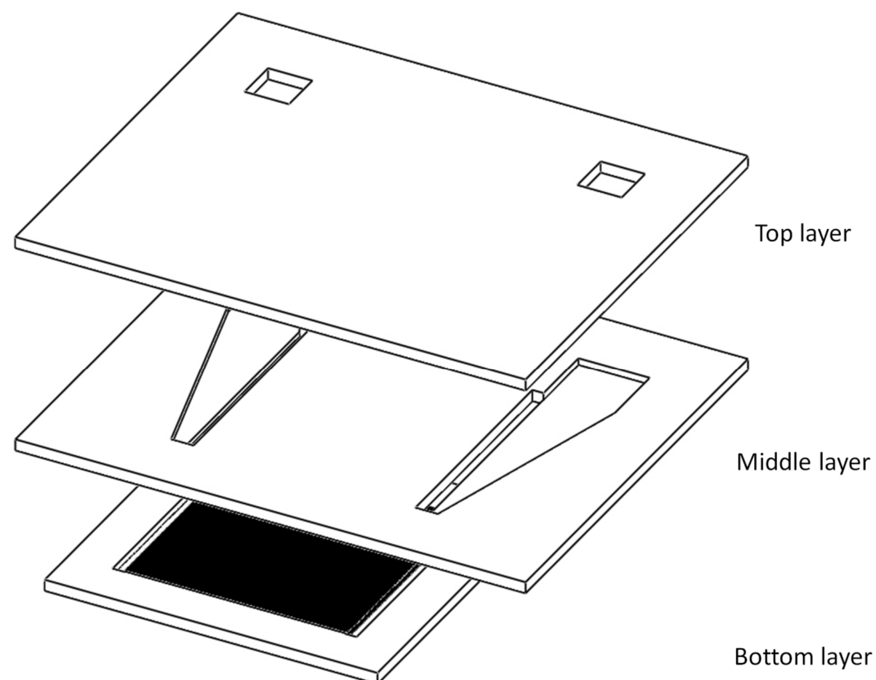


Figure 2-5: CAD model of the test device (on-chip configuration) drawn to scale.

2.4. Fabrication of the test module

The hybrid cooling scheme is implemented directly at the chip level to eliminate the interface resistance. All the steps in the fabrication processes as well as the material should be such that it can be directly integrated on the die. Therefore, device is fabricated on silicon wafers using microfabriction techniques.

2.4.1. Fabrication of the bottom die

Bottom die contains superlattice cooler, hotspot heaters, background heaters as well as microchannels (for off-chip configuration). Fabrication of superlattice coolers requires special wafers with pre-deposited superlattice layers. Fabrication of superlattice coolers as well as hotspot heaters and background heaters is done by at University of California, Santa Cruz and University of California, Santa Barbara. Figure 2-6 shows the layout of the mask. The testing area of the die is 10 mm x 10 mm. Most of the die is covered with background heaters. Hotspot heaters and superlattice coolers are located at various location of the die (center, corner, edge) to study the effect of hotspot location. Hotspot heaters are fabricated on the top of the superlattice coolers as shown in Figure 2-7. Test die contains three sizes of SLCs and hotspot heater: 70 µm x 70 µm, 100 µm x 100 µm, and 120 µm x 120 µm. At each location, all three sizes of SLCs are present. Each SLC has an individual electrode to inject the current, however SLCs share the same ground electrode. Only one ground electrode is present at each location (center, corner and edge). To save physical space on the die, adjacent hotspots share the electrode; however each of them can be individually activated. Figure 2-8 shows the optical image of one of the groups of SLCs and hotspot heaters.

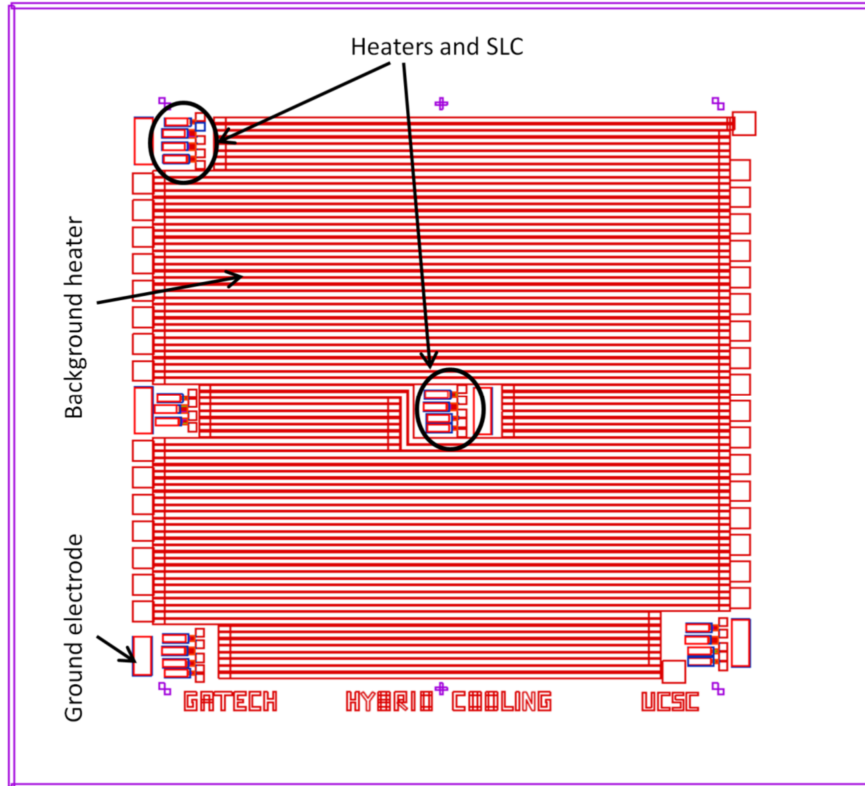


Figure 2-6: Mask layout of the superlattice coolers, hotspot heaters and background heater, showing the location of hotspots and superlattice coolers.

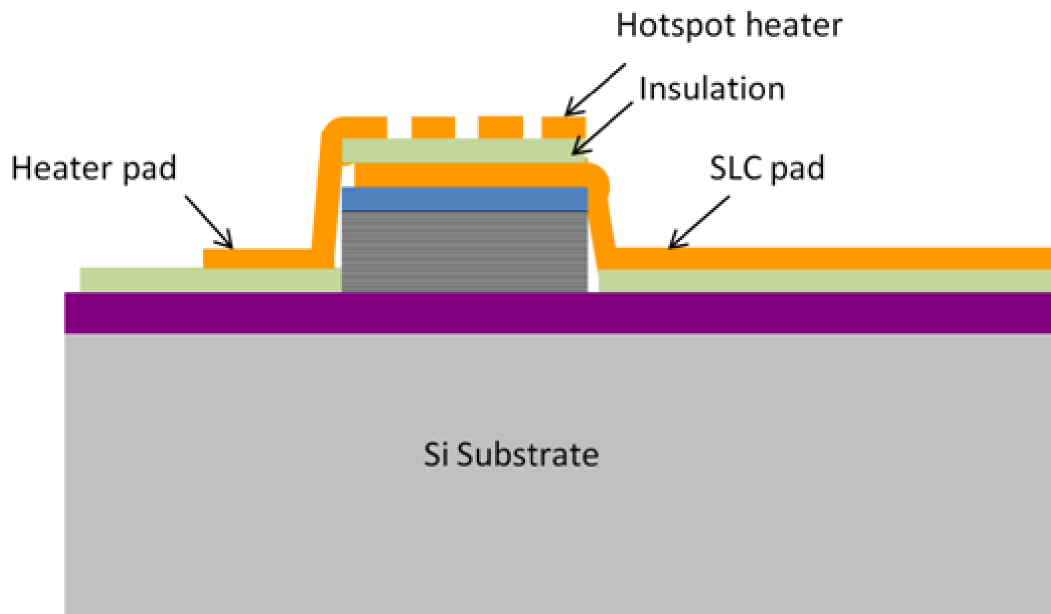


Figure 2-7: Schematic of the cross section of hotspot and superlattice coolers.

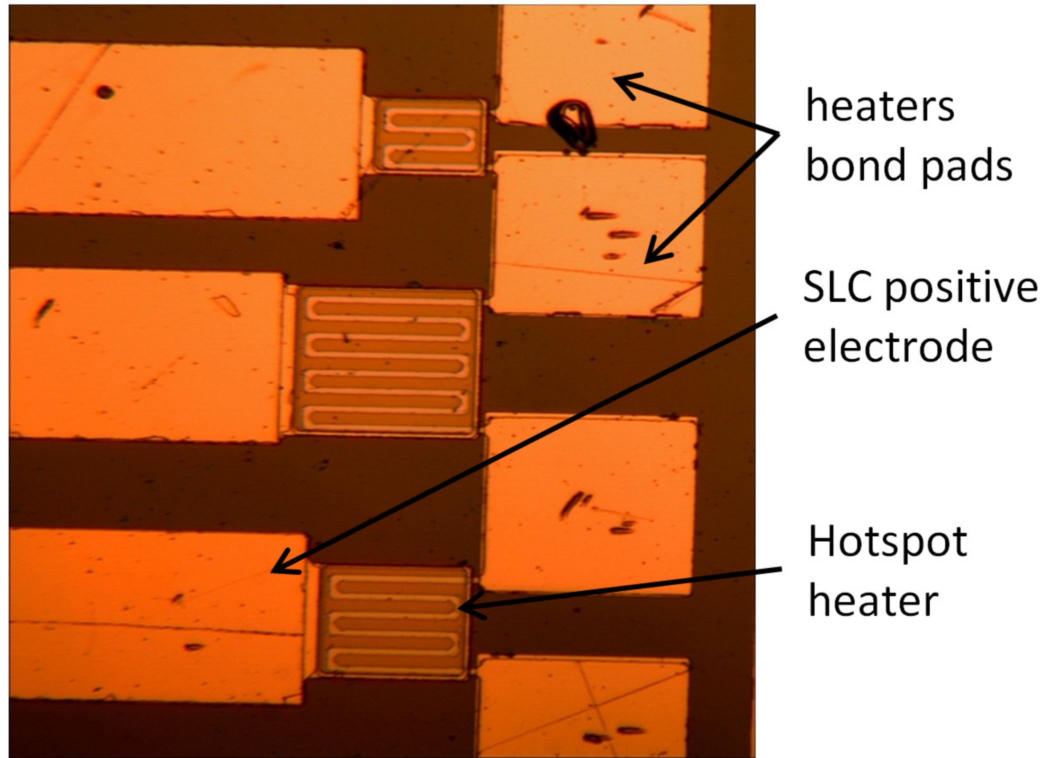


Figure 2-8: Optical image of one of the localized group of SLCs and hotspot heaters. Serpentine lines represent the hotspot heaters. Three different hotspot heaters and are shows: 70 µm x 70 µm, 100 µm x 100 µm, 120 µm x 120 µm.

2.4.2. Polishing

Once the heaters and coolers are fabricated, wafer is polished on the backside for microchannel fabrication. SLC wafer had up to 10 µm deep scratches present on the backside. The wafer is chemically and mechanically polished using Logitech PM5 polisher. The sample is bonded to a quartz substrate using either wax or crystal bond. Bonding is carried out in Logitech SS bonder. The bonded substrate is then mounted on the polisher chuck. The polishing rate depends on several operating conditions; (1) type of slurry used, (2) amount of pressure applied during polishing, (3) type of polishing pad used, and (4) RPM of the chuck. Colloidal silica is the most commonly used slurry for polishing. It contains 50 to 60 nanometer sized particles to mechanically polish the wafer.

Silica itself chemically polishes the wafer. However, polishing rate with colloidal silica is very slow, typically 0.5 μm to 1 μm per hour. Polishing rate can be increased by adding larger diameter particles in the silica. However, it comes at the price of increased surface roughness. Surface roughness during the polishing process is directly proportional to particle size and is roughly three times the particle diameter. Polishing time is reduced, while maintaining the low surface roughness, by following a two step process. First the wafer is polished with large diameter particles (0.5 μm) to remove bulk of the substrate. In the second step, smaller diameter particles (60 nm) are used to reduce the surface roughness. Cerium oxide, particle diameter of 0.5 μm, along with colloidal silica is used for the first step polishing and colloidal silica is used for the second step. Once the wafer is polished, it is removed from the substrate by heating it to 60 °C and then cleaned with acetone, methanol and isopropyl alcohol.

2.4.3. Fabrication of the microchannels

Microchannels are etched using the Bosch process. In Bosch process, an Inductive Coupled Plasma (ICP) is used to generate high energy plasma, which is used to etch the surface. Compared with Reactive Ion Etching (RIE), ICP generates higher density plasma giving higher anisotropy. The Bosch process contains three steps. The first step is isotropic etching of exposed area using SF6. In the second step, C4F8 is deposited on the side walls and bottom wall of the trench. Finally, anisotropic etching is carried out using SF6, which etches the bottom wall faster as compared to side walls. In subsequent steps, side walls are protected by the polymer so that etching occurs only in one direction. 0.5 μm of silicon is removed in one Bosch cycle. The Bosch process is repeated multiple times to get deep trenches with high aspect ratio.

Microchannel fabrication starts with silicon dioxide deposition which acts as a mask layer for silicon etching. 3 µm thick silicon dioxide is deposited using Unaxis PECVD. Thickness of the silicon dioxide layer is decided based on the height of the microchannel. Selectivity of silicon to silicon dioxide in the Bosch process is 150:1, which means for every 150 µm etching of silicon, 1 µm silicon dioxide is etched. Therefore, to etch 300 µm deep microchannels, at least 2 µm of silicon dioxide will be needed. Additional 1 µm silicon dioxide layer is deposited to account for non-uniformity in the layer as well as to make sure that it is not completely etched away during the Bosch process.

The deposited silicon dioxide layer is patterned using standard photolithography process. Positive photoresist (SC 1827) is spin on the wafer. The spinner parameters are: 1000 rpm/s ramp rate, 4000 rpm spin speed for 60 seconds. The sample is soft baked on hotplate at 115 °C for 5 minutes. Subsequently, photoresist is exposed to UV light in Karl-Suss mask aligner. The exposed wafer is developed for 2 minutes in MF319 developer and baked in an oven for 30 minutes at 120 °C. The silicon dioxide layer is then etched using the Plasma Therm-ICP. Since PT-ICP only takes 4 inch wafer and the sample is 15 mm x 14 mm in size, it is mounted on a 4 inch carrier wafer using thermally conductive grease. During the etching process, wafer is cooled from the backside using Helium to maintain the temperature of the wafer. Therefore, grease needs to be thermally conductive to minimize the thermal resistance. After patterning of silicon dioxide layer, remaining photoresist is removed by acetone and cleaned in ultra sonic bath. The sample is again mounted on a carrier wafer for silicon etching. Silicon etching is carried out in

PT-ICP using the Bosch process as described above. Figure 2-9 shows the microchannel cross section. The etched wafer is then removed from the carrier wafer and cleaned with acetone, methanol and isopropyl alcohol.

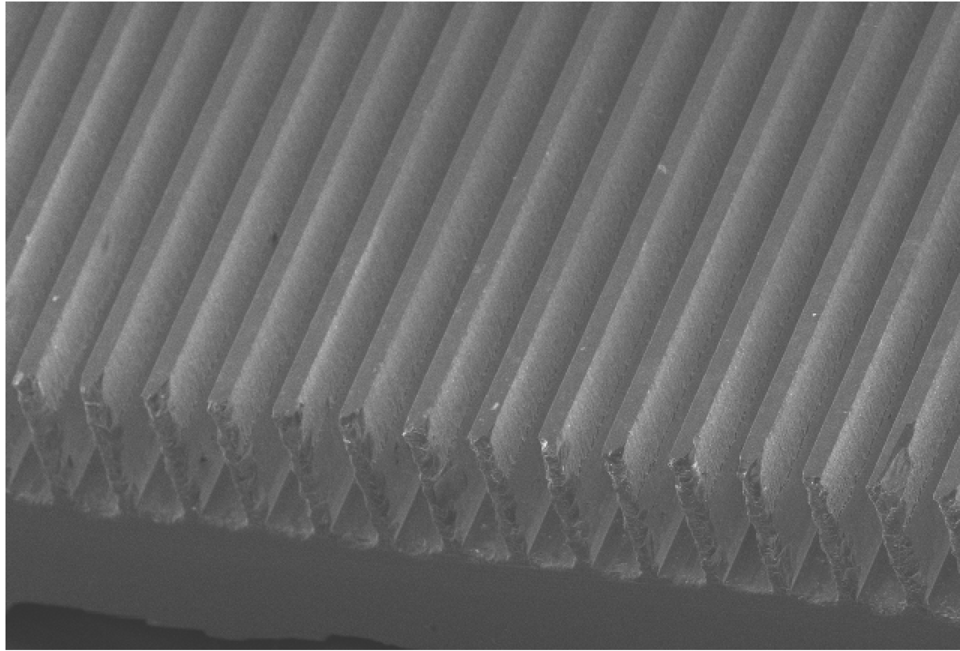


Figure 2-9: Cross section view of the microchannels.

2.4.4. Fabrication of the manifold wafer

Middle die contains manifolds for flow distribution and microchannel (for off-chip configuration). Double side polished silicon wafer was used in this step; hence no further polishing step was needed. Manifolds are etched using the Bosch process as described above. Since manifolds are blind as well as also contain through slot, etching has to be carried out in two steps. Both etching steps can either be done on the same side of the wafer or different side of the wafer. Performing both etching steps on the same side will reduce the number of fabrication steps. However after first etching step, it is very difficult to get uniform photoresist coating as the sample is already etched. Therefore, etching process is carried out on different side of the wafer. When performing etching on

different side, backside alignment is needed. Figure 2-10 shows the steps involved in the fabrication process. First 3 µm silicon dioxide layer is deposited on both sides. Then both oxide layers are patterned using the photolithography process mentioned above. It should be noted that, silicon dioxide should be patterned on both side before silicon etching is performed. Wafer is held by vacuum during the photolithography process. Performing the silicon etching on either side before oxide patterning, will not allow the wafer to be held by vacuum due to presence of deep trenches. After oxide is patterned on both sides, photoresist is removed from both sides and manifolds are etched using the Bosch process in PT-ICP. As mentioned above, the wafer is cooled by helium from the backside. When there are through features, helium will leak causing the wafer to overheat. To prevent

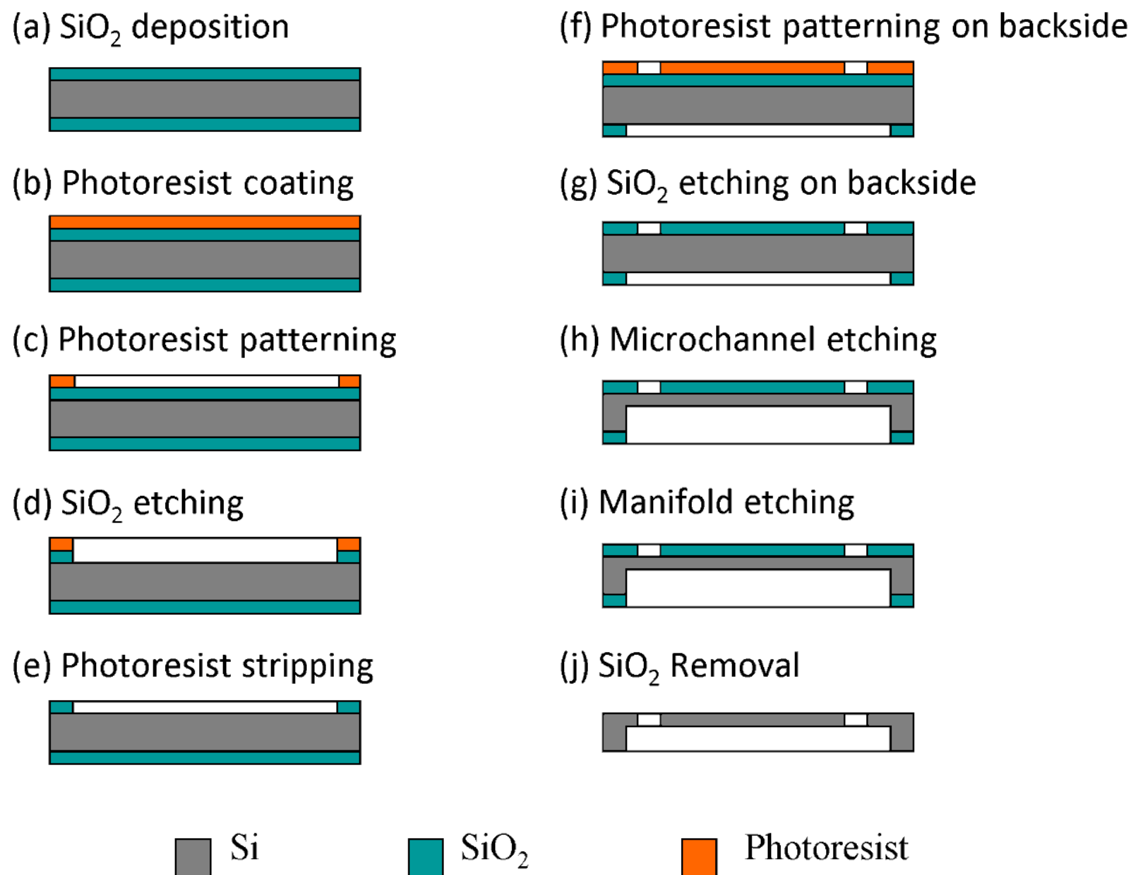


Figure 2-10: Fabrication steps involved in off-chip microchannel fabrication.

this, wafer is mounted on a 4 inch carrier wafer using thermal conductive grease. After the etching wafer is removed from the carrier wafer and cleaned. Remaining oxide layer is removed using the buffered oxide etch (BOE). Figure 2-11 shows the etched manifold.

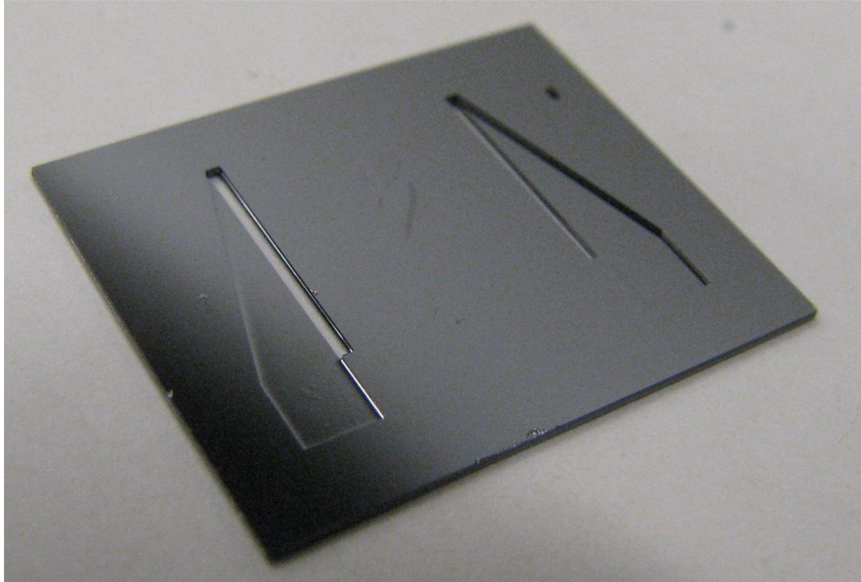


Figure 2-11: Manifolds and manifold slot fabricated on silicon wafer (off-chip configuration).

2.4.5. Fabrication of inlet/outlet port wafer

Manifolds are sealed from the top by a cover plate which also contains inlet and outlet ports. Inlet and outlet ports are also used to provide coolant to the test device. Inlet and outlet ports are etched using wet etching instead of ICP as ports need not have straight side walls. KOH is used to etch silicon as it provides anisotropic etching. Etching rate depends upon the KOH concentration and etching temperature [80, 81]. Silicon is etched in a 40% KOH solution, maintained at 70 °C, for 16 hours. KOH bath is continuously stirred to maintain uniform temperature. 1 µm silicon nitride layer is used as a mask. KOH has low silicon to silicon dioxide selectivity (200:1) at 70 °C and 40% concentration [80]. To etch 500 µm thick silicon wafer will require at least 2.5 µm thick

oxide layer. However, KOH does not etch silicon nitride [80]. Therefore, silicon nitride is used as a masking layer. Silicon nitride is deposited using the Unaxis PECVD on both sides to prevent the wafer from scratches and contamination. After ports are etched, wafer is cleaned and nitride layer is removed using BOE.

2.4.6. Device bonding

The presence of superlattice cooler does not allow device to be heated above 200 °C, hence a low temperature bonding process is needed. Several bonding techniques exists for bonding silicon wafers at low temperature such as plasma activated wafer bonding, vacuum wafer bonding, wet chemical activated bonding, adhesive bonding. The first two bonding techniques are very expensive and require special equipment. Tang *et al*. [82] have reported direct bonding at low temperature (120 °C). However, the bonding quality depends upon the surface roughness and requires roughness RMS to be less than 2 nm. Typical commercial wafer have roughness RMS of 5 nm and will require additional polishing to reduce the RMS value to 2 nm, hence this technique is not used in this work. HF bonding usually requires high temperature but some literature has reported HF bonding at less than 100 °C [83]. Even after several attempts, it was found very difficult to bond the wafer using HF at room temperature. Berthold *et al*. [84] have reported low temperature bonding using oxide as an interface layer. Even though bonding is sufficiently strong for sensor application, it is not strong enough to pass hydraulic test. Adhesive bonding has been shown to provide high bond strength at low temperature. In adhesive bonding, an adhesion layer is used to bond two surfaces. SU8 has been used as an adhesion layer and reported to provide high bond strength at temperature less than 150 °C [85, 86]. Chen *et al*. [85] bonded microchannel using SU8 and had shown that

microchannel can withstand more than 40 kPa pressure drop without any leakage. Besides high bond strength, SU8 does not require very smooth surface making it very suitable for microchannel bonding. All three dies are bonded together using SU8.

Prior to bonding, dies are dipped in 1% HF until all the hard mask layers (silicon dioxide and silicon nitride) are etched away. Afterwards dies are cleaned in Piranha at room temperature for 15 minutes. Once cleaned, the dies are dehydrated to completely remove the water by heating it on a hotplate at 150 °C for 15 minutes. First the wafer is spin coated with SU8 photoresist. Since SU8 is very thick photoresist, coating is performed in two steps. First the sample is spin at low RPM to spread the SU8 uniformly then spin at higher RPM to get the desired thickness of SU8. The spinner parameters for the first step are 100 rpm/s ramp rate, 500 rpm spin speed for 10 seconds and for the second step are 300 rpm/s ramp rate, 3000 rpm spin speed for 60 seconds. SU8 thickness was measured to be 10 µm.

Prior to bonding SU8 is softbaked at 95 °C for 2 minutes. Bonding is achieved in a vacuum chamber by heating the die and applying pressure simultaneously. Temperature and pressure are very critical for a good bond. At low temperature and pressure, bond is not strong to seal the microchannels. At high temperature and pressure, too much reflow of SU8 fills up the microchannel as shown in Figure 2-12. For this study, optimum bonding temperature and pressure is found to be 120 °C and 80 kPa respectively. Even though SU8 reflows into the microchannel, its thickness is less than 5 µm compared to microchannel height of 330 µm. The bond is strong enough to sustain more than 80 kPa pressure drop. A bonding jig is used to hold and align the dies during bonding. During bonding SU8 reflows and some amount squeezes out of the sample and sticks to the

bonding jig. To prevent the sample from sticking to the jig, the side walls and bottom walls of the jig are covered by a masking tape. The bonding process is carried out in two steps. First inlet/outlet ports are bonded to the manifold die and then this bonded structure is bonded to the superlattice die. During the first step, inlet/outlet port die is coated with SU8. The ports are covered with masking tape to prevent SU8 from reflowing to the backside. The two dies are then placed on the top of each other and heated to 120 °C while applying 80 kPa pressure for 3 hours. The bonded structure is again coated with SU8. This time manifold slots are covered with masking tape to prevent SU8 entering the manifolds. The coated structure is then bonded to the bottom die using the same process described above. Figure 2-13 shows the cross section of the microchannel after bonding.

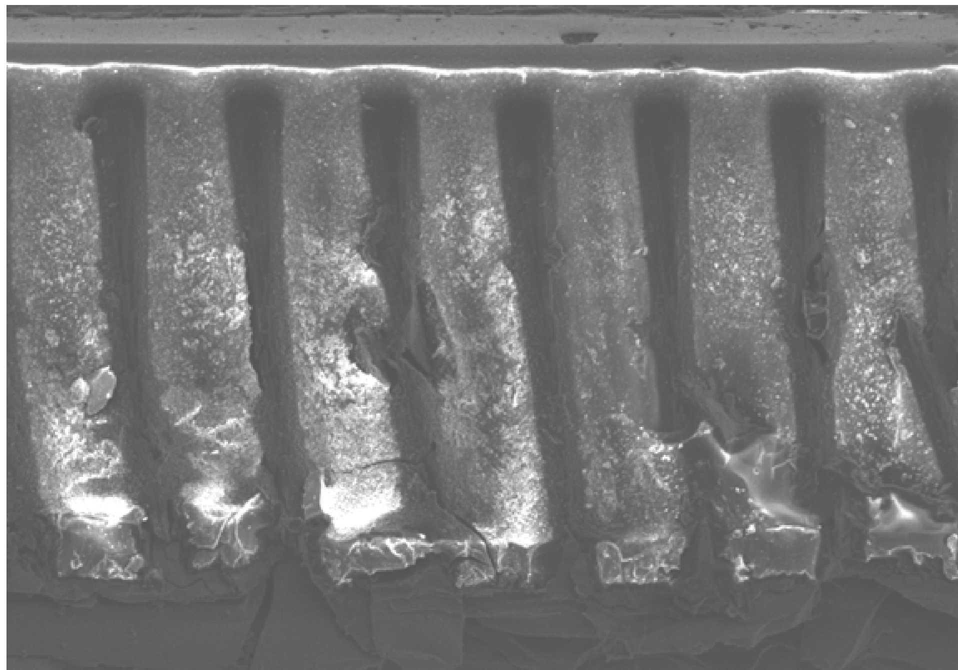


Figure 2-12: SEM image of the microchannel cross section after SU8 bonding showing the blockage of microchannels due to reflow of SU8.

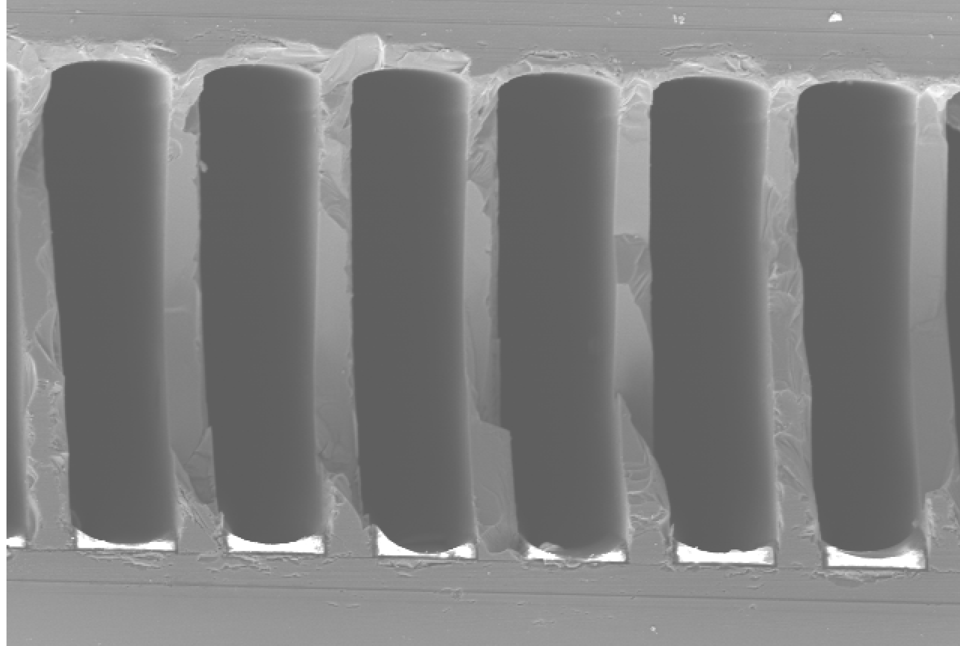


Figure 2-13: SEM image of the microchannel cross-section after SU8 bonding at 120 °C and 80 kPa. The white material inside the microchannel is SU8.

2.4.7. Device packaging

Inlet and outlet ports (obtained from Upchurch scientific) are glued to the bonded structure using an adhesive ring. The sample and ports are cleaned with the Iso-propyl alcohol to remove any contamination. Then an adhesive ring was sandwiched between the test device and port. The structure is clamped together and placed in an oven at 170 °C for 3 hours. The bond is strong enough such that trying to remove the ports results in silicon breaking.

The test device is then bonded to a specially fabricated PCB board. Figure 2-14 shows the layout of the PCB board. It contains a slot in the middle to accommodate the test device. On the periphery of the slot, copper traces are machined. Each side has 16 copper traces. On the end of each trace, 1 mm hole is made to hold PCB connectors. The test device is glued to the PCB using epoxy so that the bottom die is on the copper connector side. The heaters and superlattice coolers are wire bonded to the PCB with 1

mil Al wire. The maximum current supplied to the wire bonds is 400 mA. At higher currents, the wire melts due to Joule heating. Since superlattice share ground electrode and if more than one superlattice coolers are turned on, total current going through the ground electrode will be very high. Therefore, two wires are bonded to the ground electrode. Figure 2-15 show the front and back side of the die after packaging. The PCB connectors are then soldered to the board. Back side of the device is protected by a transparent acrylic housing to prevent damage to device as well as wire bonds. Figure 2-16 shows the assembled device.

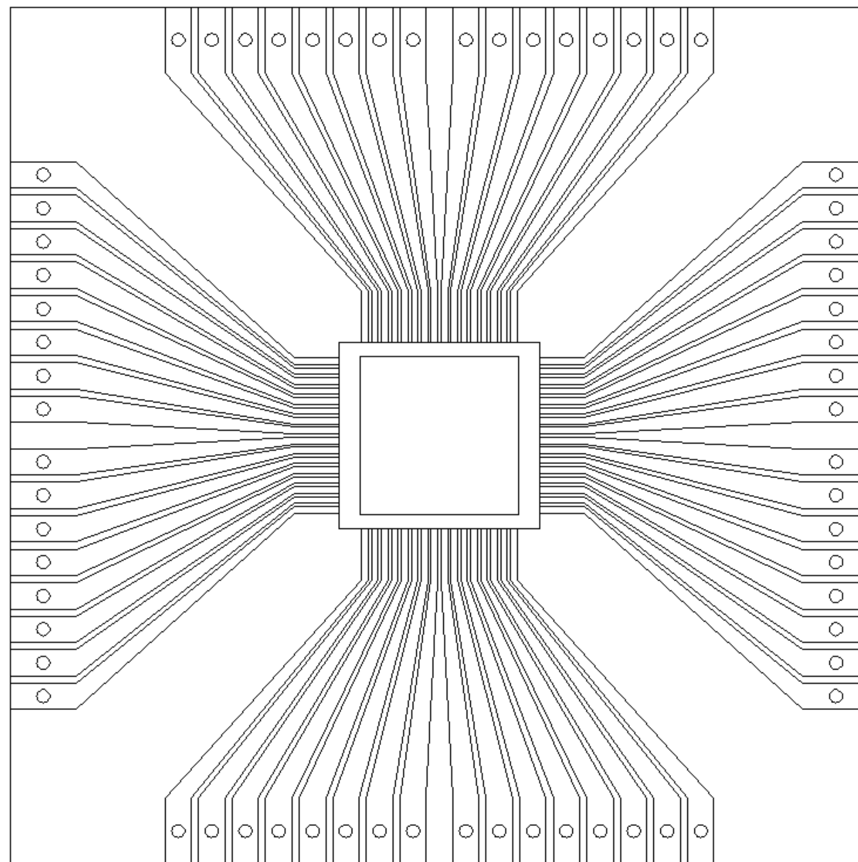
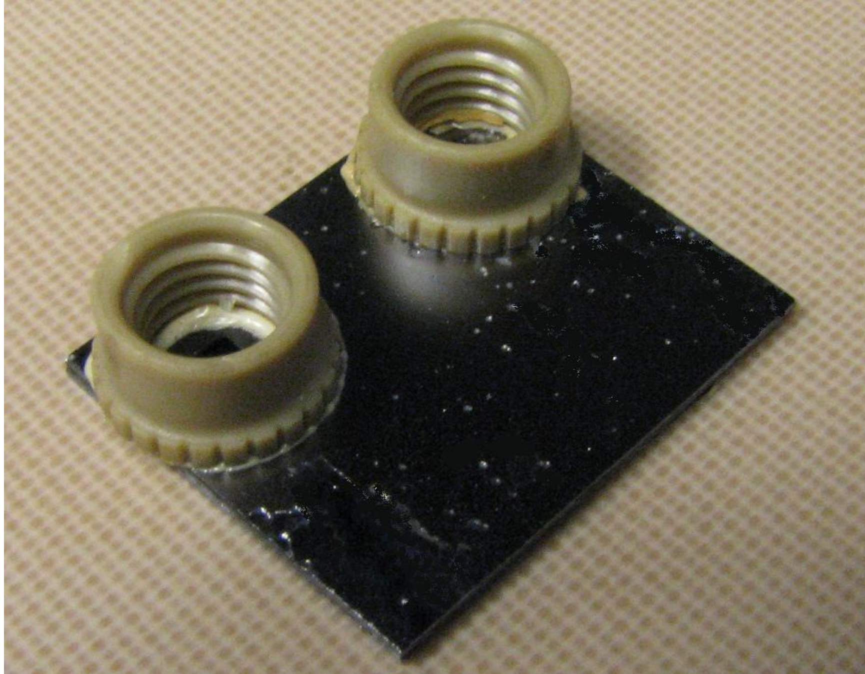


Figure 2-14: Layout of the PCB board.



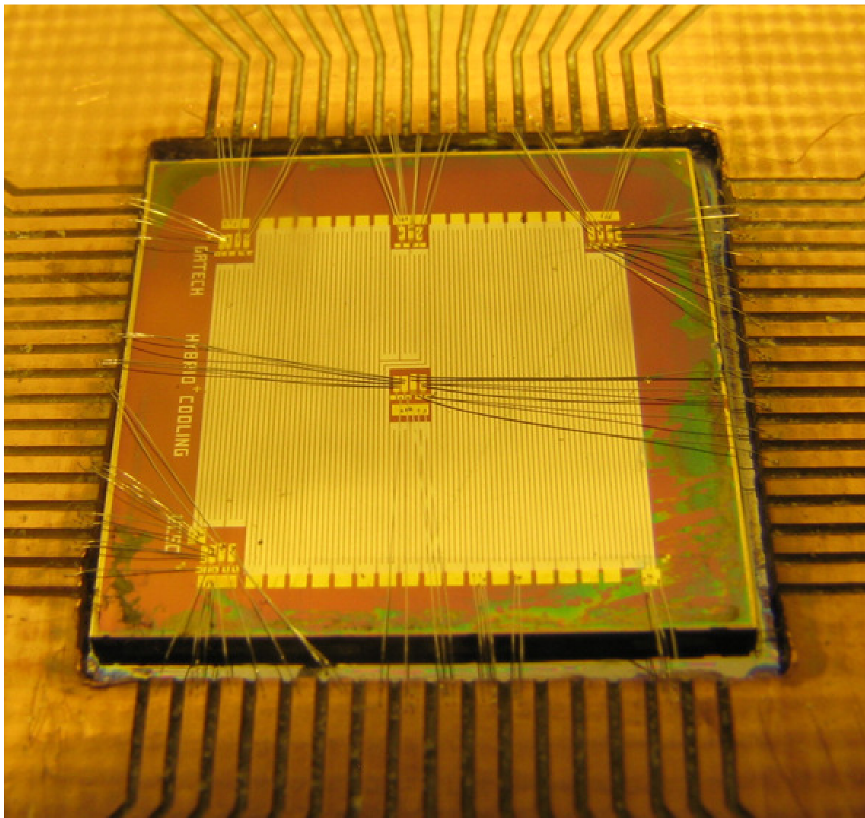
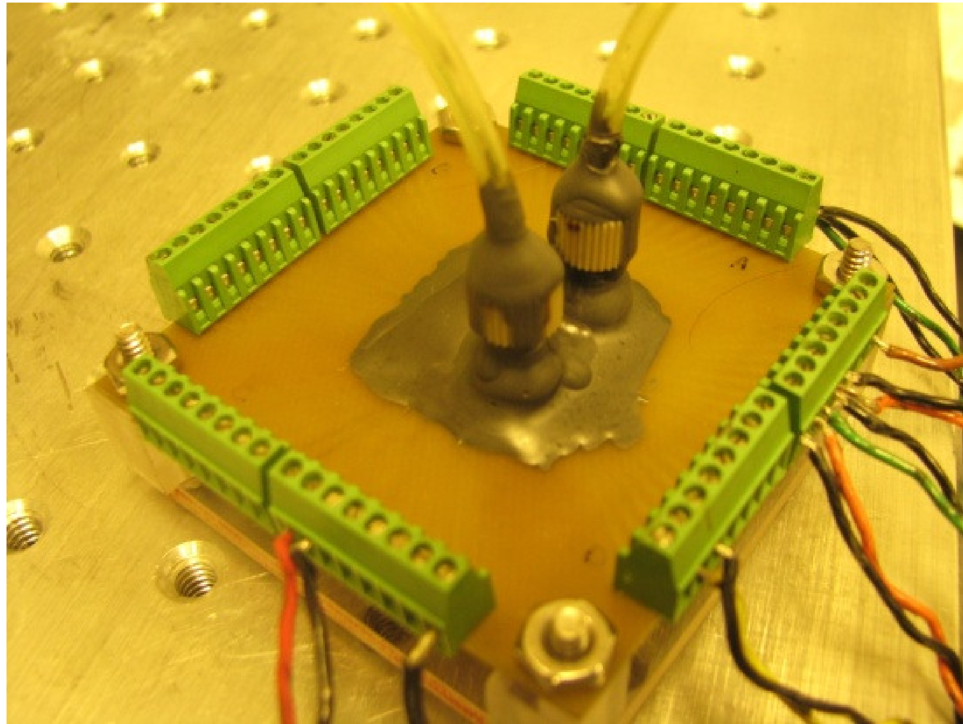


Figure 2-15: Front of the test device (top) and back of the test device (bottom) after wirebonding.



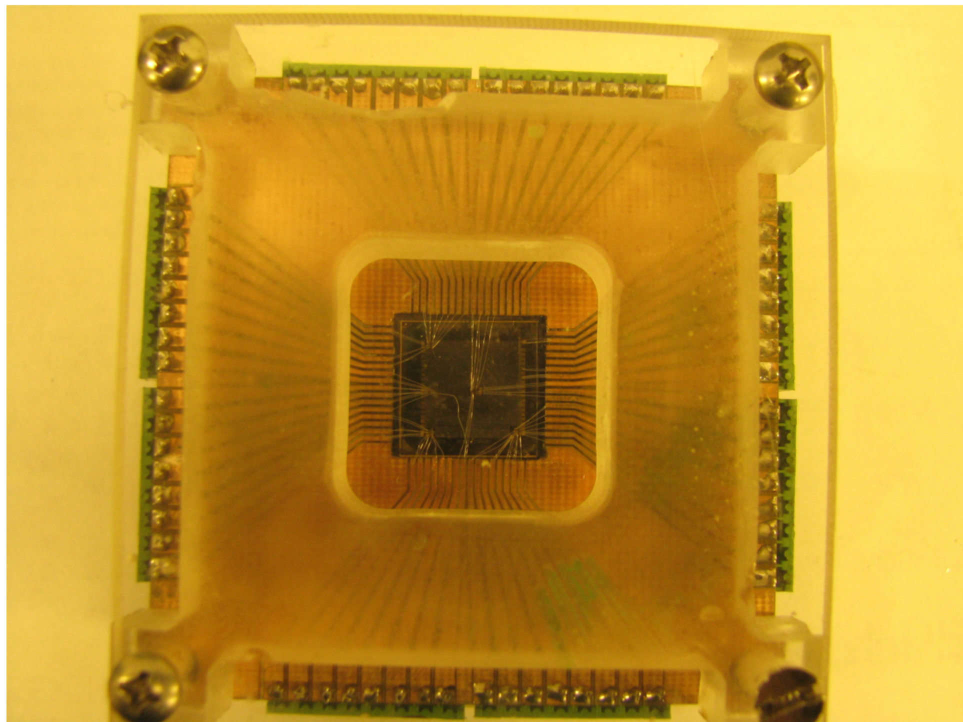


Figure 2-16: Final assembled device. The front side is covered with epoxy to avoid leakage from inlet and outlet ports (top), backside shows the housing used to protect the wirebonds and reduce heat transfer to ambient (bottom).

2.5. Summary

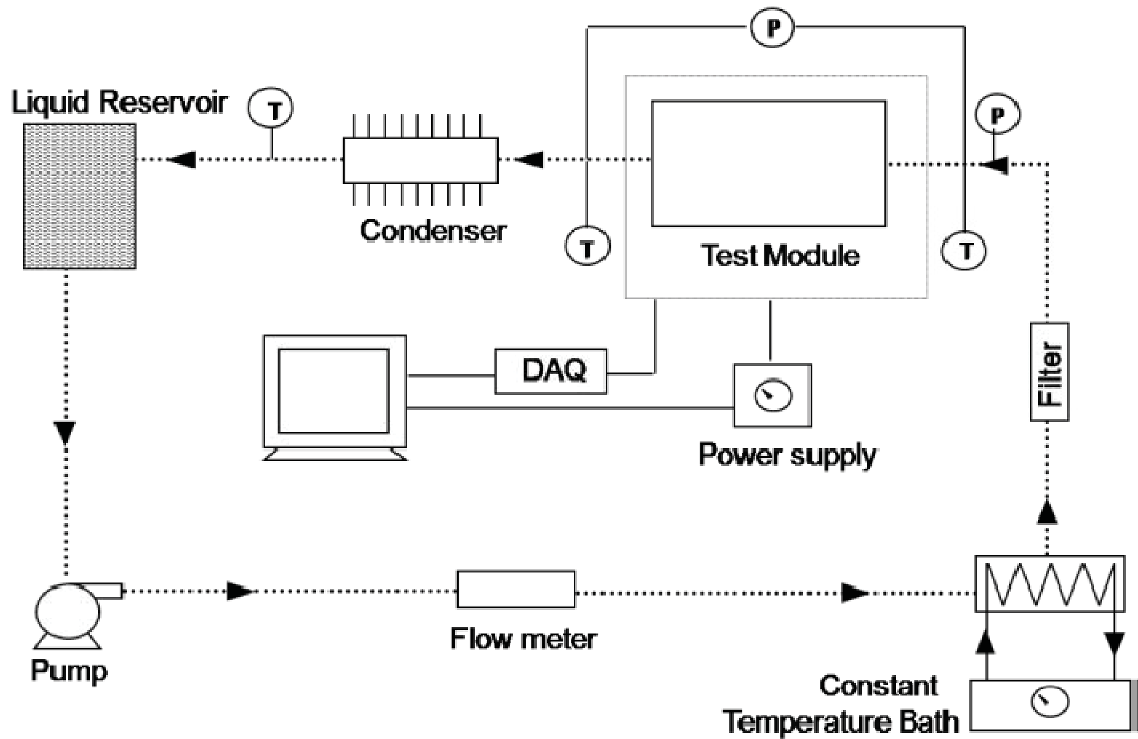
This chapter describes the design and fabrication of test device. Microchannels are optimized for minimum pumping power. Oblique manifolds are found to provide more uniform flow compared to vane guides. Test device is fabricated in the cleanroom using microfabrication techniques. Bosch process is used to etch microchannel as well as manifolds, whereas wet etching is used for ports fabrication. The device is bonded together using SU8. The bond is strong enough to prevent any leakage. The superlattice coolers and heaters are wire bonded to a PCB board for testing.

CHAPTER 3: EXPERIMENTAL SETUP AND PROCEDURE

This chapter describes the experimental facility, as well as the procedure used to test the hybrid cooling scheme. A closed flow loop with temperature and pressure sensors at appropriate locations are used to characterize the hybrid cooling scheme. Uncertainty associated in the measurement of various parameters is computed using propagation of uncertainty principle. Moreover, instrumentation procedure for infrared imaging is also presented.

3.1. Description of experimental test facility

A schematic of the experimental test facility is shown in Figure 3-1. De-ionized water and FC72 are used as the coolant. Coolant is pumped from a liquid reservoir and circulated through the flow loop by a gear pump. The gear pump has an electronic controller which allows to set the desired flow rate. The pump needs to be calibrated before performing the experiments. Calibration is done by measuring the volumetric flow rate corresponding to the pressure drop in the system. The calibration data is fed into the controller to give accurate flow rate during measurements. A valve is placed after the pump to regulate the flow. The coolant flow rate is also measured by a rotameter, which is placed downstream to the pump. A Lytron liquid to liquid heat exchanger is used to preheat the coolant. One side of the heat exchanger is connected to Lauda recirculating chiller, which circulates the water at the prescribed temperature through heat exchanger. The coolant enters from the other side and is preheated to the desired temperature. Subsequently, it is passed through a micro-filter to remove contaminations. Micro-filter is capable of removing particulates larger than 8 μm in diameter. The coolant then enters the test module where it removes the heat dissipated by the test chip. Afterwards, the



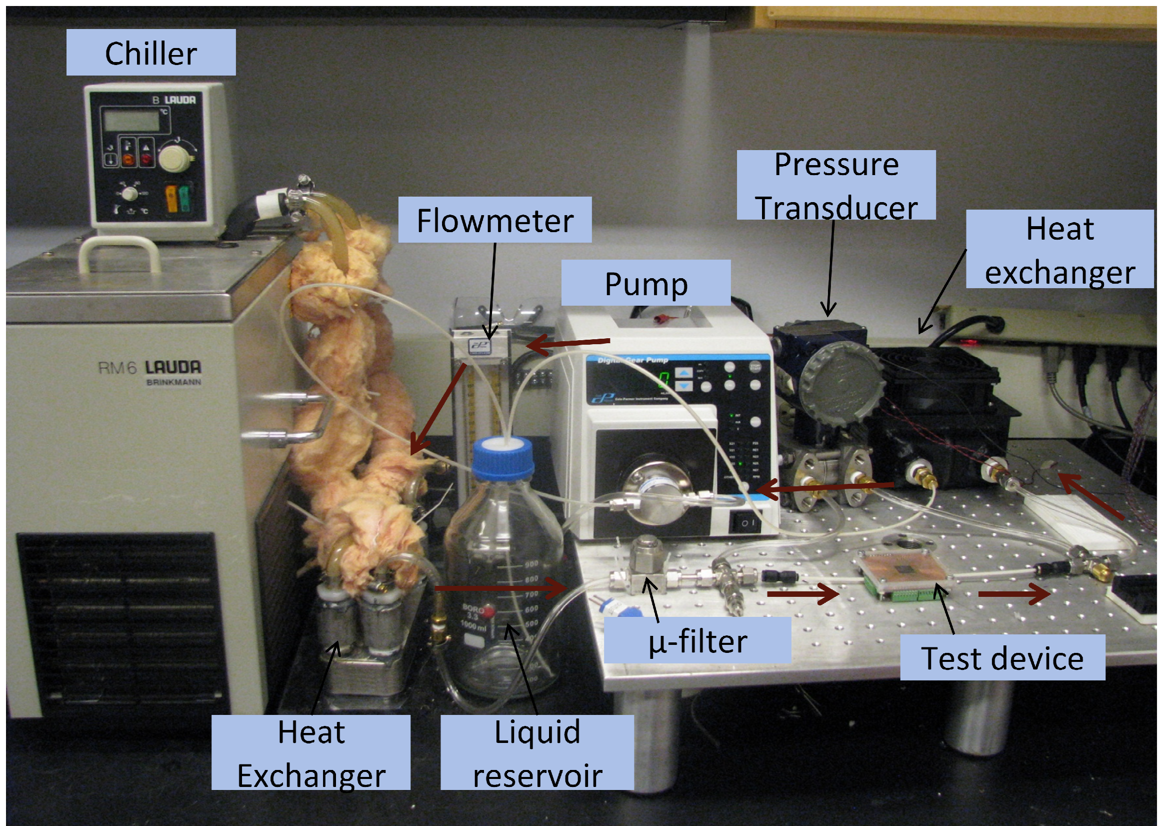


Figure 3-1: Schematic of the flow loop (top), and experimental facility (bottom). Power supplies and data acquisition unit are not shown in this image.

coolant is passed through a chiller to cool it back to the room temperature. A 126 μm diameter T type thermocouple is located at the outlet of the chiller to monitor the temperature of the coolant, which is returned to the liquid reservoir to form a closed loop.

Hotspot heaters, as well as superlattice coolers, are powered by separate DC power supplies. Hotspot heaters are powered by Agilent E3631A which is rated up to 25V/1A, while superlattice coolers are powered by Agilent E3649A which is rated up to 35V/1A. Power supplies are connected to computer through GPIB interface card and are controlled by Labview. Voltage drop across the hotspot heaters, as well as superlattice coolers, are measured using Agilent 34970 data acquisition unit with 34901A multiplexer card. Current flowing through the heaters/superlattice coolers is indirectly measured by measuring the voltage drop across the precision resistor, which is connected in series to the hotspot heater/ superlattice coolers. Since superlattice cooler draws an order of magnitude higher current than hotspot heaters, precision resistor used to measure current through superlattice coolers have higher wattage rating. 1Ω, 3 watts and 3Ω, 3 watts precision resistor is used to measure the current going through the superlattice cooler and heaters, respectively. Pressure drop across the test module is measured using Omega pressure transducer. The pressure transducer has adjustable range from 0-17 psi to 0-100 psi. The output current signal is converted to voltage signal through a precision resistor. Temperature at the inlet and outlet port is measured using a calibrated Omega quick disconnect Copper-Constantan (Type T) thermocouple. The differential pressure sensor and thermocouple data are acquired via an Agilent Data Acquisition unit. Pressure transducer and thermocouples are calibrated prior to use using Omega pressure calibrator and Omega thermocouple calibrator, respectively.

3.2. Experimental procedure

Prior to experiments whole system is degassed. The air is removed from the system by a degassing pump. Degassing is performed for an hour. All the valves are kept open during degassing. De-ionized water used for experiments is also degassed for an hour. Once the system is degassed, it is charged with de-ionized water. The pump is run for 15 minutes to avoid pump transient behavior and get steady flow in the systems. If the coolant needs to be pre-heated, system is run till the coolant temperature reaches a steady state. The temperature of the coolant is continuously monitored during this period. Once the system reaches steady state, heaters and superlattice coolers are activated. Power supplies, as well as data acquisition unit, are controlled using Labview. Manually controlling the power supply sometimes results in voltage spike. Moreover, there is a chance of accidentally feeding higher current to the heaters, damaging the heaters and wirebonds (if current is more than 400 mA, it will burn the wire bonds). Labview can set the maximum allowable current from the power supply, which prevents the device and wire bonds from erroneous current input.

Once the system has reached steady state, hotspot and superlattice cooler are activated. Due to their small size, both hotspot heater and superlattice cooler reach steady state almost instantly. The voltage drop across the hotspot heater and current supplied to it is measured to calculate the resistance of the hotspot heater. Resistance of the hotspot heater is converted into temperature using the resistance calibration curve. Each hotspot heater is calibrated in an oven to obtain resistance calibration curve prior to experiments. The measurements are averaged out for at least 25 readings to reduce random error associated with the measurements. Table 3-1 shows the various testing parameters. For

each test conditions, current supplied to superlattice coolers is increased slowly from 0 mA to 400 mA, in increment of 50 mA. At each SLC activation current, hotspot temperature is measured and averaged out for 25 readings. Moreover, for each test conditions, base temperature (temperature corresponding to 0 W/cm^2 hotspot heat flux and 0 mA activation current) is measured. Base temperature is measured both at the start of the experiment, as well as at the end of the experiments to measure change in the ambient temperature during the experiment. If the base temperature is significantly different (greater than 0.3 °C) at the start and end of the experiment, experiment is repeated for that test condition.

Table 3-1: Parameters used for testing

Testing parameters	Parameters value
Temperature	23 °C, 50 °C, 85 °C
Hotspot heat flux	0 W/cm^2, 50 W/cm^2, 100 W/cm^2, 150 W/cm^2, 200 W/cm^2, 0 250 W/cm^2, 300 W/cm^2, 350 W/cm^2
Hotspot size	70 µm x 70 µm, 100 µm x 100 µm, 120 µm x 120 µm
Working fluid	Water, FC72, Air

3.3. Measurement uncertainty

Thermocouples are calibrated using a thermocouple calibrator which has an uncertainty of ±0.2 ºC for temperature in the range 25 ºC to 100 ºC. The rotameter is graduated with minimum resolution of 1 ml/min. The uncertainty associated with differential pressure measurement is estimated to be 0.1% of the full scale. Pressure transmitter is calibrated for the full scale of 100 kPa, which means maximum error in pressure drop is ±0.1 kPa. Power supplies have the voltage uncertainty of 10 mV ± 0.05% of the supplied voltage and the current uncertainty of 4 mA ± 0.15% of the supplied current. The maximum voltage and current supplied to hotspot heaters is 2 V

and 30 mA, respectively. Thus, uncertainty in voltage and current supplied by the power supply is $\pm$ 11 mV and $\pm$ 4mA, respectively. Data acquisition system has an estimated uncertainty of $\pm$ 27 μV in voltage measurement and $\pm$ 20 μA in current measurement. Since uncertainty in voltage and current measurement is more than two orders of magnitude smaller than the uncertainty in the voltage and current supplied by power supplies, the former can be ignored. Uncertainty associated with the resistance measurement can be estimated using the principle of uncertainty propagation. Using this principle, uncertainty in resistance measurement can be written as:

$$U_{R1}^2 = \left(\frac{\partial R}{\partial V}\right)^2 U_V^2 + \left(\frac{\partial R}{\partial I}\right)^2 U_I^2 \tag{3.1}$$

where, U_{R1}, U_V, U_I is the uncertainty associated with resistance, voltage and current measurement, respectively. Solving the above expression gives uncertainty in resistance measurement to be $\pm$ 18 mΩ. Besides resistance measurement, uncertainty in resistance value comes during the heater calibration too. Uncertainty in resistance calibration is given by the expression:

$$U_{R2} = mU_T \tag{3.2}$$

where, m is the slope of the resistance calibration curve and U_T is the uncertainty associated with the temperature measurement. Thus, uncertainty in the resistance calibration is $\pm$ 43 mΩ. Total uncertainty associated in the resistance value can be expressed as:

$$U_R = \sqrt{U_{R1}^2 + U_{R2}^2} \tag{3.3}$$

Total uncertainty in resistance measurement is computed to be ± 47 mΩ. The resistance of the hotspot heaters is used to calculate the temperature, thus uncertainty in the temperature measurement can be written as:

$$U_T = \frac{U_R}{m} \tag{3.4}$$

Uncertainty in the temperature measurement is calculated to be ± 0.22 °C. Uncertainty in the power measurement can be calculated using the propagation principle and can be expressed as

$$U_P^2 = I^2 U_V^2 + V^2 U_I^2 \tag{3.5}$$

Substituting for the voltage and current values gives uncertainty in the power measurement to be ± 8 mW. Heaters are isolated from the ambient to minimize the heat loss. Heat loss to the ambient is estimated using a resistance network analysis and is found to be less than 1% of the total heat dissipated at the hotspot.

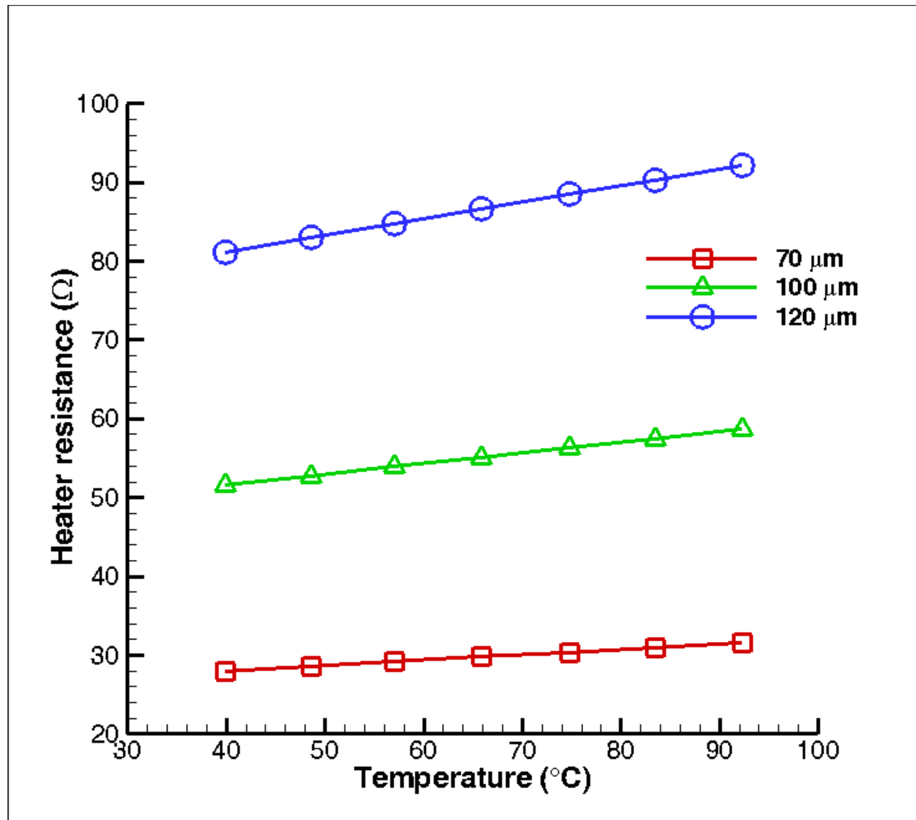
3.4. Device Characterization

Hotspot heaters serve dual purpose. Besides providing heat flux to simulate microprocessor power map, they also serve as temperature sensors. Prior to testing the devices, hotspot heaters are characterized to obtain the resistance-temperature curve. Calibration is done by uniformly heating the device in a temperature controlled environment. Resistance of the heaters is measured using the Kelvin method to eliminate the effect of lead wires. Thermocouples are placed inside oven to accurately measure the temperature near the test chip. Thermocouples are calibrated using a thermocouple calibrator prior to usage. Figure 3-2 shows the calibration curve for the on-chip

configuration as well as off-chip configuration. Resistance of all three heaters varies linearly with the temperature for the range tested. The resistance of the heaters on off-chip configuration is lower compared to the same size heaters in on-chip configuration due to two reasons. First in off-chip configuration, heaters are made of Au compared to Pt for on-chip configuration. Resistivity of Au is roughly five times lower than the Pt at room temperature. Moreover, the heater line is thicker in off-chip configuration. Thickness of heater lines in off-chip and on-chip configuration is 1.5 μm and 0.8 μm respectively.

3.5. Experimental set up for infrared imaging

Resistance thermometer gives an average temperature of the hotspot heaters. It does not reveal the temperature distribution across the heaters. Spatial temperature map is obtained to assess the temperature uniformity across the hotspot heater when superlattice cooler is activated. Infrared imaging provides a non-contact, non-obstructive method for measuring the temperature. All bodies above absolute temperature emit infrared radiation. The amount of radiation emitted by the body is dependent upon its temperature. Infrared imaging utilizes this property to measure the temperature of the surface. Infrared microscope has a quantum detector which measures the number of photons emitted by the surface. Photons emitted from the surface are focused on the detector using an optical lens. These photons excite the electrons in the detector to conduction state. The excited electrons charge the capacitor and the electrical signal is converted to voltage, which is processed to yield temperature. Figure 3-3 shows the layout of the basic operation of IR microscope.



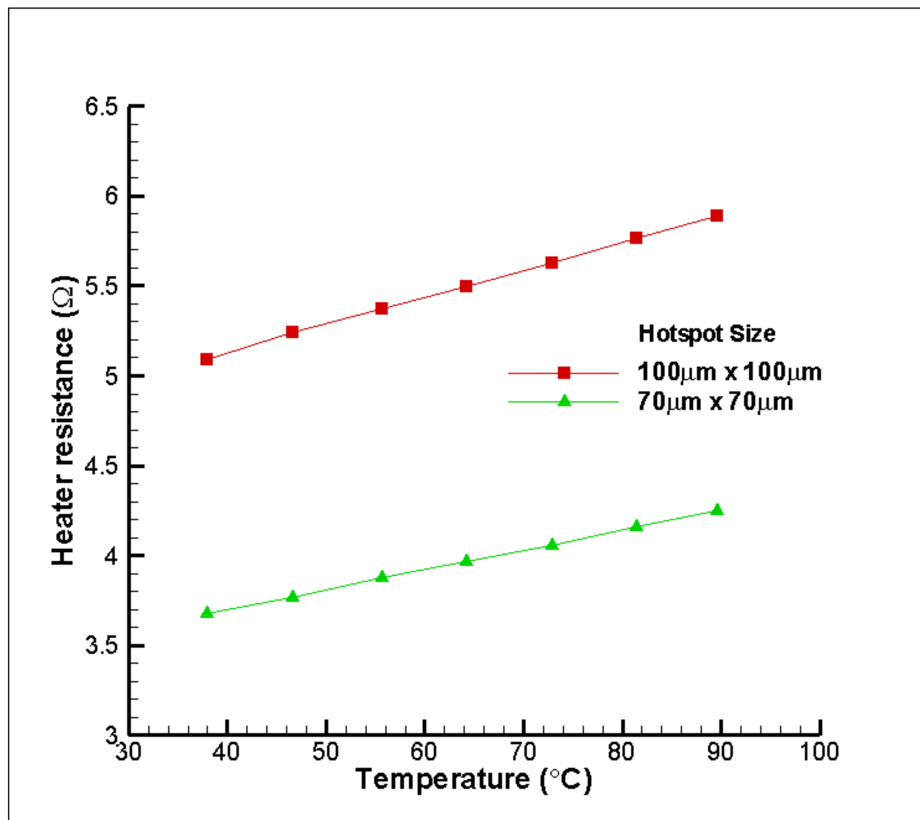


Figure 3-2: Hotspot calibration curve for on-chip (top) and off-chip configuration (bottom).

The Quantum focus Infrascope II is used for thermal imaging of the sample. The microscope has a quantum InSb detector, which is sensitive to the wavelength in the range of 1 μm to 5 μm. The microscope has maximum spatial resolution of 5 μm, which is well below the hotspot size, and temperature resolution of 0.1 °C. It has three optical lenses (1X, 5X and 15 X) and a thermal stage to heat the sample during operation. The sensitivity of the microscope is directly proportional to the number of photons hitting the detector, which is directly proportional to the temperature. Therefore for higher sensitivity, object temperature should be as high as possible. However at high temperature, convection thermal current disturb the signal and introduce noise. Recommended operating temperature for the object is in the range of 60 °C – 80 °C. In this range, sufficiently high numbers of photons are emitted by the object but convection

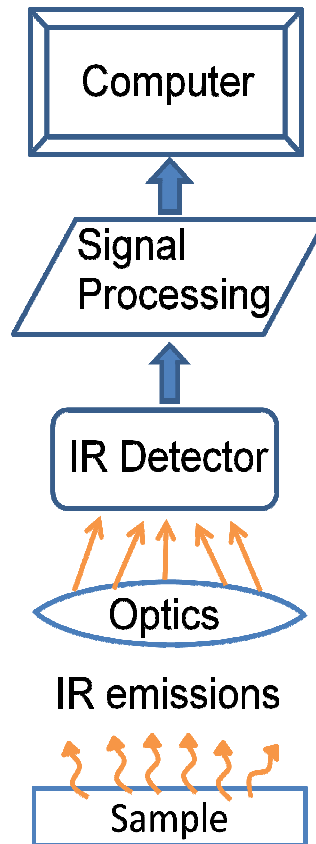


Figure 3-3: Schematic diagrams showing the basic operation of infrared microscope.

currents are not dominant enough to affect the signal. The presence of inlet and outlet ports on the back does not allow the test device to be mounted on the thermal stage. Therefore, device is heated by circulating preheated fluid through the microchannels. Recirculation chiller with a heat exchanger is used to preheat the fluid. A type T-thermocouple is inserted upstream of the inlet port to measure the temperature of the preheated fluid. Heaters and superlattice coolers are powered with the same power supply as in the resistance thermometry experiments. Voltage drop and current flowing through the heater and superlattice coolers is measured using Agilent 34970 data acquisition unit.

3.6. Experimental procedure for infrared imaging

One of the drawbacks of the infrared imaging is that the emissivity of the sample is usually not known. Even though infrared microscope is capable of calculating the emissivity during the calibration stage, it assumes emission is coming from a black body which is not the case. Emissivity of the sample might deviate significantly from the black body emissivity. Moreover, if the emissivity of the sample is low (presence of metal layer on the sample), it will not emit enough photons to excite significant number of electrons in the detector. Thus, the signal will be weak and resulting temperature map will not be very accurate. To prevent this from happening, sample is coated with high emissivity material (possibly with known emissivity). It offers two advantages. The sample has uniform emissivity and the emissivity of the sample is close to black body emissivity. Two types of coatings are used: graphite foam and carbon based black paint. Coatings can be applied by directly spraying it on the sample. However, this method does not give uniform coating. Moreover, it does not provide good control on the thickness of the coating. Airbrush offers more uniformity and control on the thickness of the coating.

Thickness of the coating is not important for steady state experiments however for transient experiments, coating adds additional thermal mass and increase the response time. Since graphite foam is found to provide thinner coating than black paint, it is used to coat samples.

The infrared detector is operated at cryogenic temperature to reduce the signal noise during measurements. The detector is cooled using liquid nitrogen. The sample is mounted on a specially built housing to accommodate the inlet and outlet ports and placed on the thermal stage of the infrared microscope. Preheated water is circulated to heat the sample to an elevated temperature (usually in the range of 50 °C – 70 °C) and the system is allowed to reach steady state. One of the hotspot heaters, located far from the hotspot heater being tested, on the test chip is powered on to measure the temperature of the test chip. Power provided to the hotspot heater is kept very low to avoid temperature rise at the hotspot due to Joule heating. Once the system has reached steady state, test chip is calibrated. Calibration is done at reference temperature between 50 °C – 70 °C. Since emissivity changes with temperature, reference temperature should be close to the actual operating temperature. During calibration, the hotspot heaters, as well as superlattice coolers, are turned off to get uniform temperature across the imaging domain. Temperature of the sample is measured by providing small power to another hotspot heater (located far from the imaging window). This value is fed into the infrared microscope software to get emissivity map of the sample. Since the sample is already coated with the high emissivity material the emissivity map shows uniform emissivity in the range of 0.9 to 1.0. Figure 3-4 shows the emissivity map of one of the superlattice coolers. Emissivity is fairly uniform across the imaging domain. This emissivity map is

used for determining the temperature during experiments. Each pixel in the emissivity map corresponds to temperature at certain location on the sample. If sample moves even a slight bit, the pixel in the emissivity map will not correspond to the temperature at the calibrated location of the sample. To avoid this from happening, sample is securely placed and all the wires taped down. Moreover, vibration during experiments is minimized. Once the sample is calibrated, hotspot heaters and superlattice coolers are activated and to obtain temperature distribution across them. Since emissivity map changes with the location and temperature of the device, new calibration should be done for each test conditions.

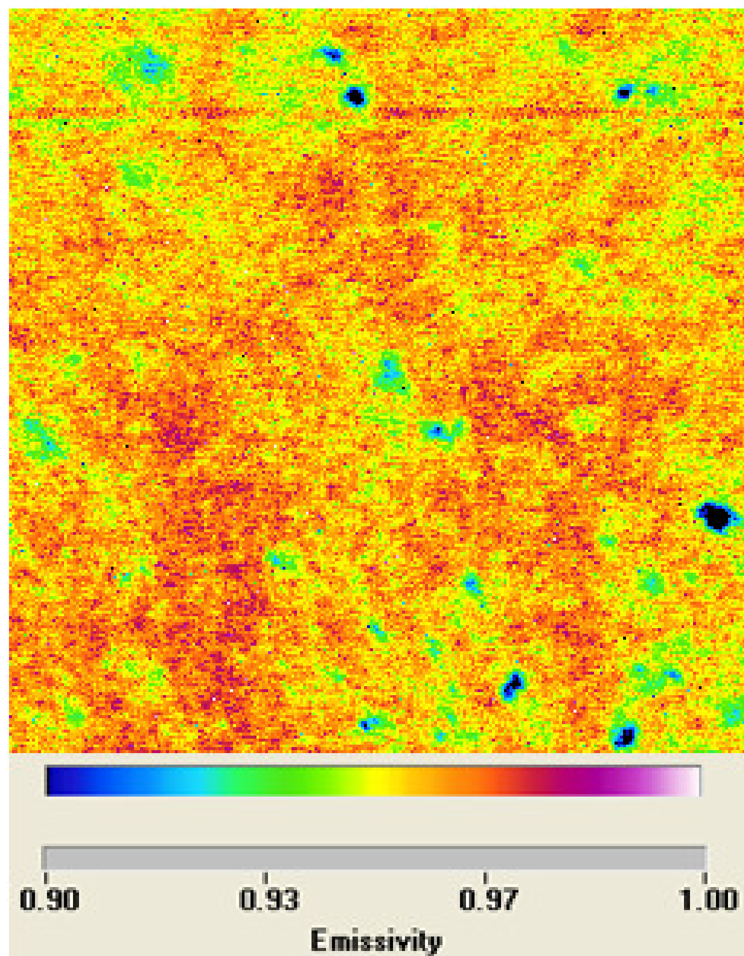


Figure 3-4: Emissivity map of one of the sample.

3.7. Experiment procedure for transient characterization

IR microscope is also used to characterize the transient behavior of the superlattice cooler. It is equipped with a single transient detector, which is connected to a trans-impedance amplifier. Since the transient detector contains a single InSb detector it gives temperature at one pixel, which is roughly the size of 30 μm x 30 μm at 15X magnification. The trans-impedance amplifier has two bandwidth ranges: normal range and extended range. Normal range has sampling frequency of 30 kHz, whereas, extended range has sampling frequency of 300 kHz. Since the expected response time of the superlattice coolers is of the orders of tens of microseconds, normal range is sufficient to capture the transient behavior of the superlattice cooler.

The procedure for the transient operation is same as that for the steady state operation mentioned above except that the microscope is externally triggered. To obtain the temperature at the superlattice as the function of time, superlattice coolers as well as IR microscope both should be triggered at the same time. Simultaneous triggering is achieved by the circuit shown in Figure 3-5. A NPN transistor is used as an electrical switch to activate and deactivate the superlattice cooler. Superlattice cooler is connected between the collector and emitter of the transistor. A square trigger pulse is applied across the base and emitter of the transistor. Superlattice activation time can be changed by changing the frequency of the pulse. A second square pulse which is synchronous and identical with the first pulse is used to trigger the microscope. Microscope starts capturing the data as soon as it receives the trigger signal. Output signal is averaged out for 200 cycles to reduce noise.

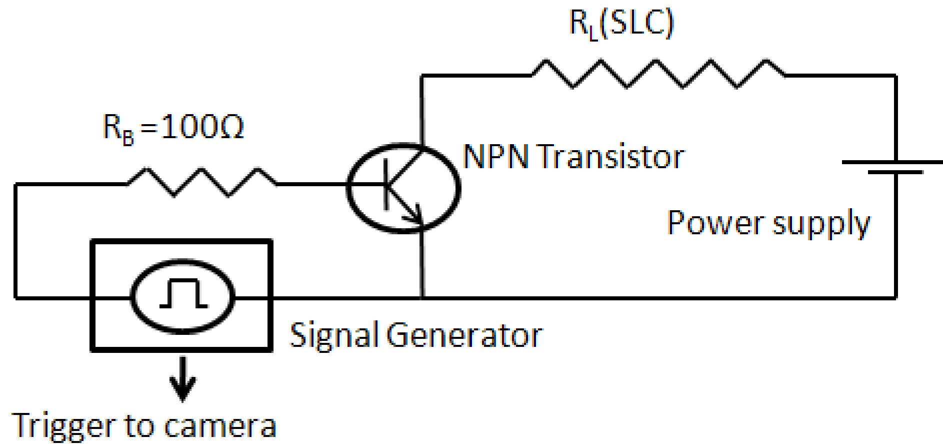


Figure 3-5: Electrical circuit used to simultaneously trigger the SLC and microscope.

In the procedure mentioned above, since the transient behavior of superlattice cooler is of interest, hotspot heater is not activated. It is assumed that the superlattice cooler is activated as soon as hotspot is detected and there is no delay in activation of superlattice cooler and hotspot. However, in a real scenario there will always be some delay between hotspot activation and superlattice cooler activation. Experiments have been performed to study the effect of time delay between the activation of superlattice cooler and hotspot heater. Figure 3-6 shows the schematic of the circuit used to introduce delay between activation of hotspot heater and superlattice cooler. Two NPN transistors and signal generator units are used; one for superlattice and other for hotspot heater. Both signal generator units are locked in so that they share the same reference and clock. By locking the signal generator unit, the output pulse from both units will be synchronous, thus both hotspot heater as well as superlattice cooler will be activated at the same time. Now to introduce delay between the activation of hotspot heater and superlattice cooler, the reference of one of the signal generator can be delayed by that amount compared to

the other unit. The delay in the reference signal is achieved by changing the phase of the reference signal.

The amount of phase change needed to introduce certain amount of delay can be obtained using the expression given below:

$$\frac{\text{phase change}}{360} = \frac{\text{time delay}}{\text{time period of pulse}} \tag{3.6}$$

A third pulse which is synchronous to the hotspot activation pulse is sent to the trigger the microscope. The output readings are averaged out for 200 cycles to reduce noise associated with the signal.

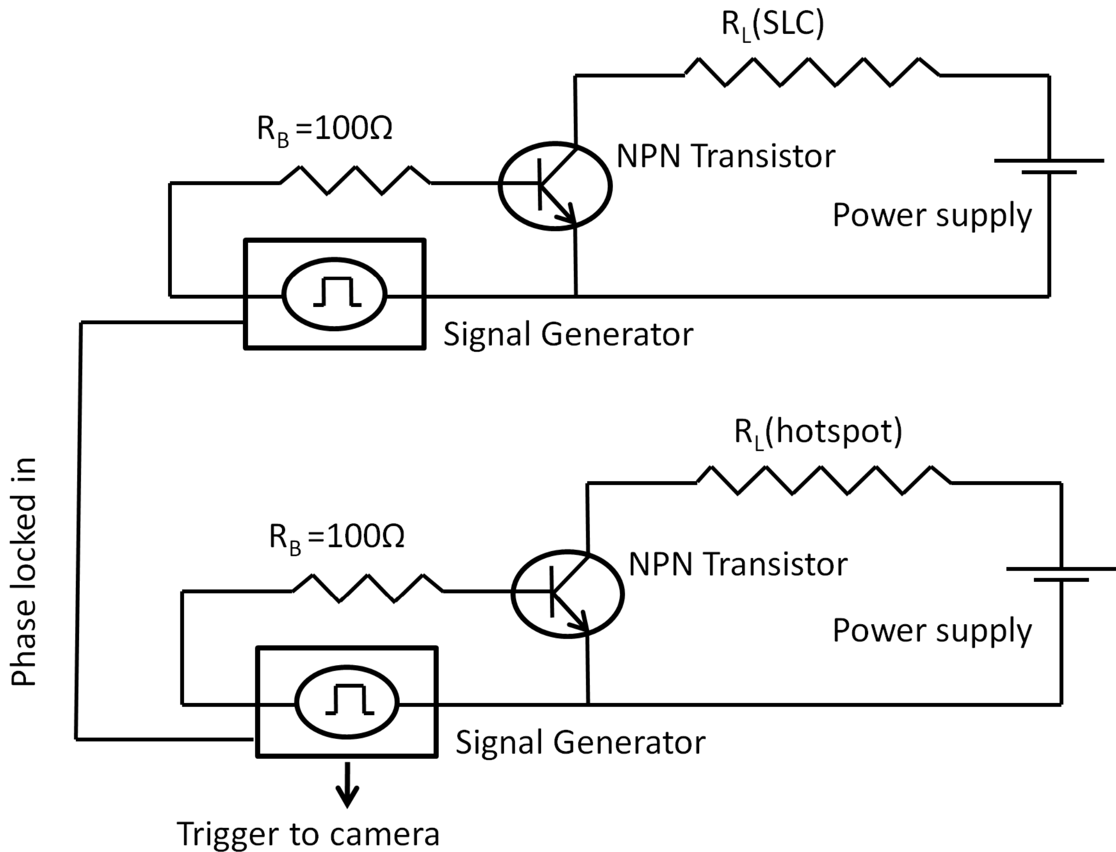


Figure 3-6: Electrical circuit used to simultaneously trigger the hotspot, SLC and microscope. The two signal generator units are locked it to share the same clock.

3.8. Summary

This chapter describes the experimental facility, procedure and testing parameters used for the resistance thermometry experiments. Uncertainty associated in the temperature measurement is calculated using the propagation of uncertainty principle. Uncertainty in the temperature measurement is calculated to be ± 0.22 °C. Resistance of the hotspot heater varies linearly with temperature for the range of temperature tested. Experimental procedure for infrared imaging, as well as transient characterization, is also described in detail.

CHAPTER 4: HYBRID COOLING SCHEME PERFORMANCE CHARACTERIZATION

Performance of hybrid cooling scheme depends upon several operating parameters, such as ambient temperature, operating current, choice of the working fluid as well as geometric parameters, for example, superlattice size, ground electrode location etc. The metric used to characterize the performance of the superlattice cooler contains following elements:

(1) Maximum temperature drop obtained at the superlattice cooler

(2) Maximum heat flux removed by the superlattice cooler, which is also defined as the cooling power density (CPD)

Experiments are conducted to understand the effect of above parameters on the performance of the superlattice cooler. Both off-chip as well as on-chip microchannel devices are characterized. Moreover, a resistance network model is developed to predict the performance of superlattice cooler, with potentially much higher ZT material, for future generation processors.

4.1. Experimental results

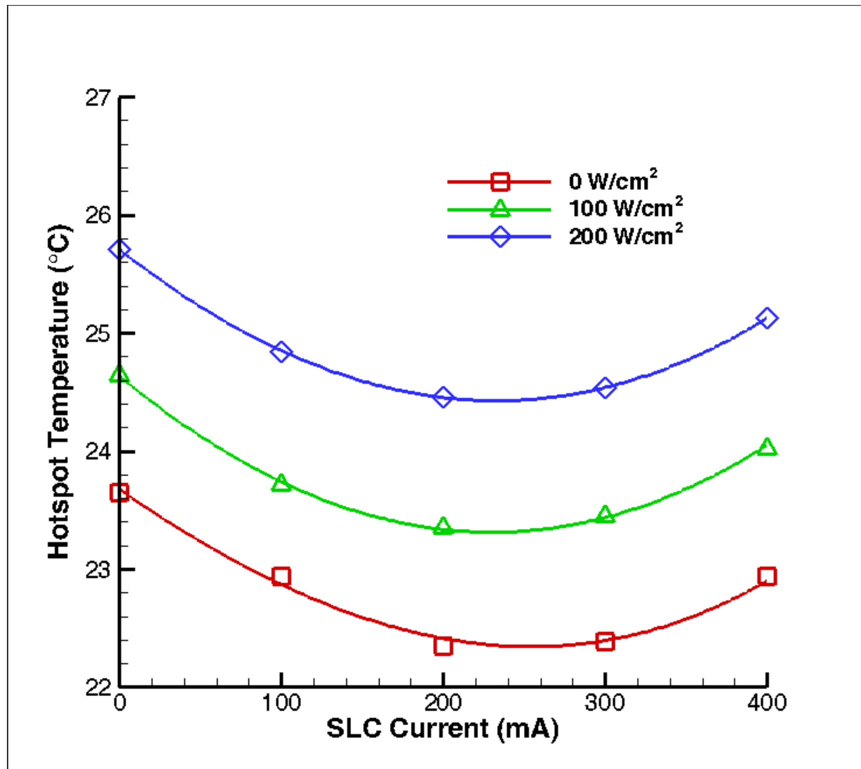
4.1.1. Superlattice cooler performance

Figure 4-1 shows the cooling curve of the off-chip as well as on-chip microchannel configuration for 100 µm x 100 µm SLC at room temperature. Cooling is defined as the temperature drop at the hotspot, when SLC is activated. As the current supplied to SLC increases, temperature at the hotspot decreases. However, an optimum current exists beyond which further increase in current, increases the temperature at the

hotspot. At low operating current, Peltier cooing is more dominant. As the current increases, Joule heating being proportional to the square of the current increases more rapidly compared to the Peltier cooling. At the optimum operating current, Peltier cooling at the superlattice is balanced by the Joule heating and parasitic heat transfer to the superlattice. Beyond the optimum current, Joule heating within the superlattice structure overshadows the Peltier cooling at the superlattice junction, thus increasing the temperature at the superlattice. The optimum current for off-chip microchannel configuration is 250 mA. For the on-chip microchannel configuration, the optimum current is more than 400 mA, which is the maximum current carrying capacity of the wire bonds used to provide power to the superlattice cooler. Maximum cooling for the off-chip and on-chip configuration is 1.5 K and 3.0 K, respectively.

The optimum operating current is not a function of the hotspot heat flux, which makes the implementation of the hybrid scheme easier, as one does not need to know the hotspot heat flux to determine the SLC activation current. As the hotspot heat flux increases the cooling curve shifts to a higher temperature, which decreases the maximum cooling obtained at the superlattice. However, optimum current remains the same. Since the hotspots are fabricated directly at the top of SLC, power dissipated at the hotspot serve as the heat load for the SLC and from Eq. 1.1, it can be shown that the optimum operating current is not a function of the heat load on the SLC. The above statement holds true only for the small temperature variation, when constant electrical and thermal properties assumption is justified.

Even though measured cooling is same for 100 mA and 400 mA operating current (for off-chip microchannel configuration), Peltier heating at the ground electrode will be



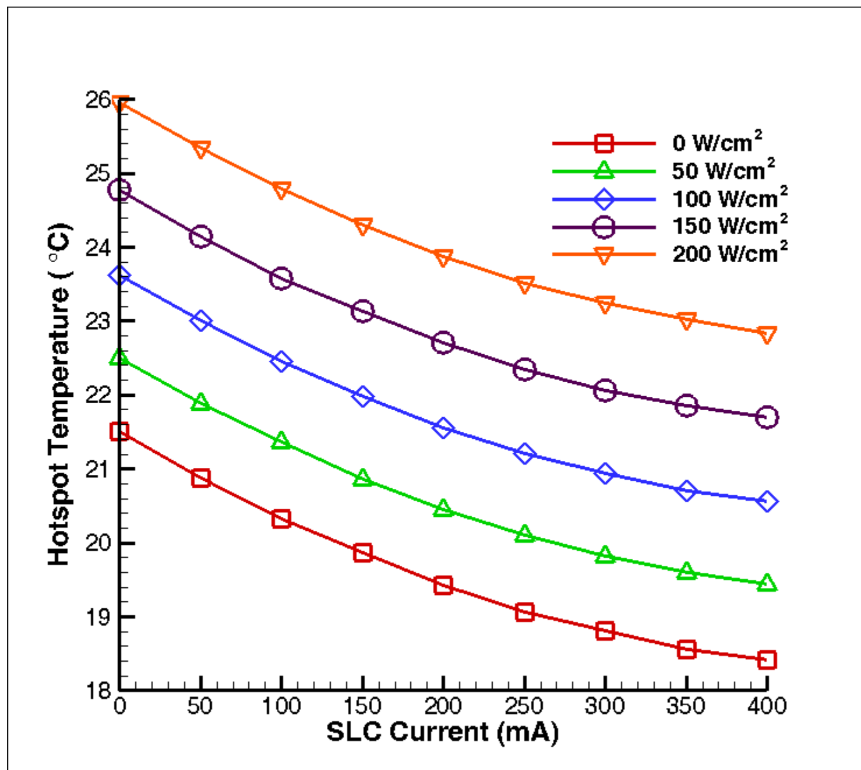


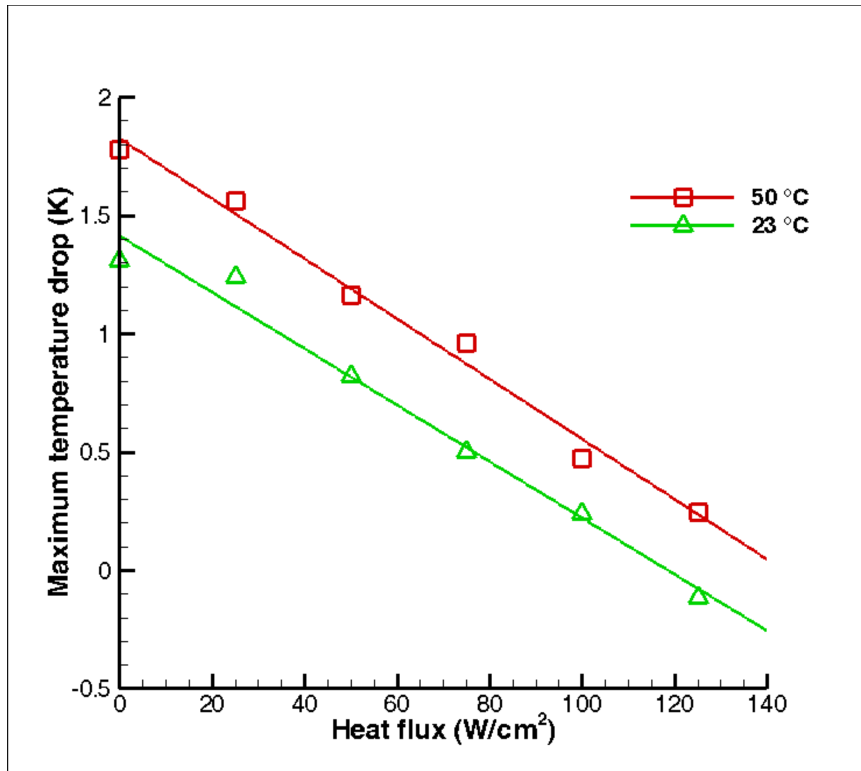
Figure 4-1: Cooling curve for off-chip configuration (top) and on-chip microchannel configuration (bottom). Symbol shows the experimental data points which are curve fitted with a second order polynomial. Ambient temperature = 23 °C, SLC size = 100 μm x 100 μm.

greater corresponding to 400 mA operating current, which puts additional load on the microchannel heat sink. Furthermore, power input to the SLC will be sixteen times higher at 400 mA compared to 100 mA activation current. Therefore, SLCs should always be operated below their optimum activation current.

4.1.2. Effect of ambient temperature

Peltier cooling is directly proportional to the temperature. As the ambient temperature increases, average energy of electron increases and more electrons can cross the energy barrier at the metal-superlattice interface, resulting in enhanced Peltier cooing. Electrical and thermal properties of the superlattice layers do not change significantly for the temperature in the range of 300 K to 358 K. The electrical conductivity of silicon reduces by 10% when temperature is increased from 300 K to 358 K [87], which increases the Joule heating in the silicon substrate. Thermal conductivity of silicon decreases by 19% for temperature increase from 300 K to 358 K [88, 89]. This increases the thermal resistance of the silicon, and thus reduces the parasitic heat transfer (due to Joule heating as well as Peltier heating at the ground electrode) to the superlattice cooler. Seebeck coefficient of superlattice layers and silicon also does not vary significantly for the temperature range of interest [90]. Hence ZT of the superlattice structure increases with the temperature. This results in increased cooling at the superlattice cooler as the ambient temperature is increased. Moreover, due to reduction in thermal resistance of the silicon substrate, parasitic heat transfer to superlattice reduces. Therefore, at higher temperature, location of the ground electrode does not play as critical role in determining the performance of the superlattice cooler. Optimum activation current also increases with the ambient temperature.

Figure 4-2 shows the effect of ambient temperature for off-chip microchannel configuration as well as on on-chip configuration. The maximum temperature drop is defined as the temperature drop corresponding to optimum current. Optimum current is obtained by curve fitting the cooling curve with a second order polynomial fit. For the on-chip microchannel configuration, the optimum current is more than 400 mA, which is the maximum current carrying capacity of the wire bonds used to provide power to the superlattice. Hence the superlattice coolers are not tested beyond 400 mA operating current. For the on-chip configuration, temperature drop corresponding to maximum achievable 400 mA current is reported as the maximum temperature drop. For both devices net cooling increases with ambient temperature. On-chip microchannel configuration shows significant improvement as ambient temperature is increased compared to off-chip microchannel configuration. At room temperature on-chip microchannel configuration, is able to dissipate 190 W/cm^2 heat flux from 70 µm x 70µm hotspot. At 85 °C, maximum heat flux dissipation increase to 340 W/cm^2, about 80% improvement compared to room temperature. The maximum temperature drop for on-chip configuration is 4 K, 5.2 K and 6.2 K, respectively, at 23 °C, 50 °C and 85 °C. For the off-chip microchannel configuration maximum temperature drop achieved at 23 °C, and 50 °C is 1.3 K and 1.8 K, respectively. The optimum activation current for the on-chip configuration at 23 °C, 50 °C and 85 °C is 370 mA, 400 mA and 440 mA, respectively. For off-chip microchannel configuration optimum current corresponding to 23 °C and 50 °C is 250 mA and 280 mA, respectively.



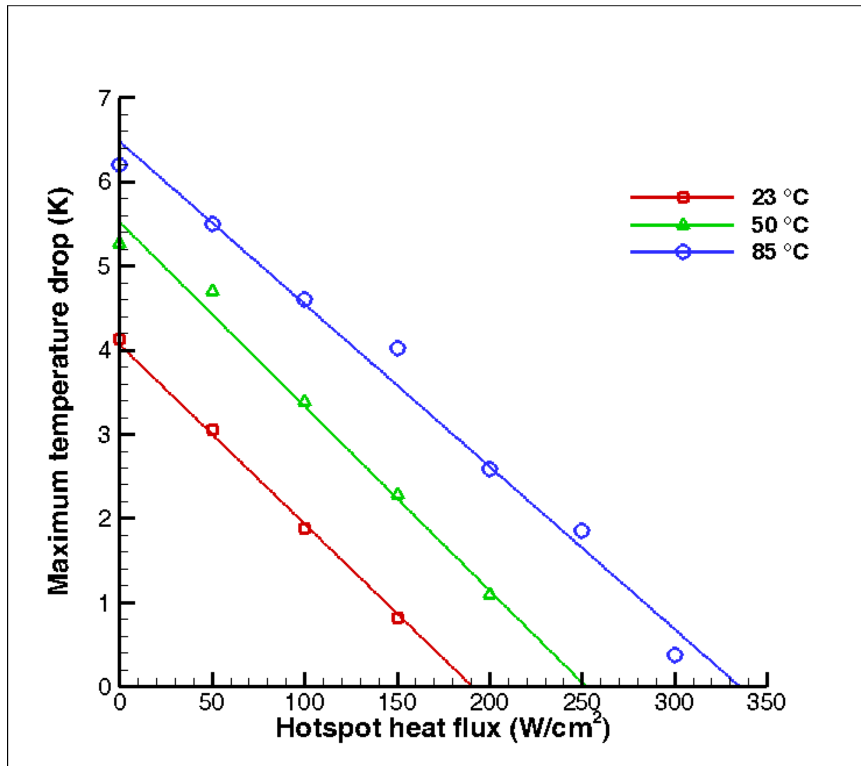
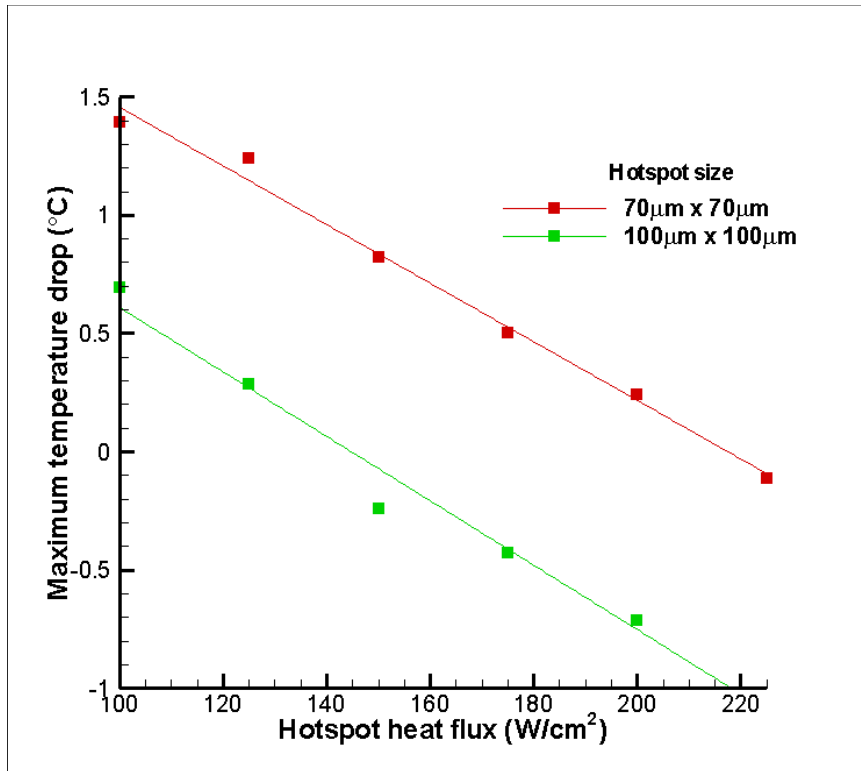


Figure 4-2: Effect of ambient temperature on the performance of 70 µm x 70 µm superlattice cooler: off-chip microchannel configuration (top) and on-chip microchannel configuration (bottom).

4.1.3. Effect of superlattice cooler size

The Peltier effect is a surface phenomenon therefore one might expect the performance of the SLC to be independent of its size. However, due to several non-ideal effects: top and side metal contact resistance, spreading resistance, cooling obtained at the SLC varies with its area. Top metal contact resistance (between the metal layer and superlattice layer) is directly proportional to area whereas side metal contact resistance (between the side metal layer and the superlattice layer) is proportional to the square root of area. Moreover, electrical spreading resistance is inversely proportional to the square root of area. Thus, Joule heating within the superlattice structure reduces with the area. However, thermal spreading resistance decreases with the square root of area, resulting in more parasitic heat transfer to the superlattice for larger devices. Furthermore, the electrical contact resistance between the metal and superlattice layers increases with the area, resulting in more Joule heating. This suggests an optimum SLC size exists, which maximizes the temperature drop. The optimum SLC size is usually around 50 μm x 50 μm to 60 μm x 60 μm [69].

Maximum heat flux removed from the SLC is defined as the cooling power density (CPD) of SLC. As the heat load on the SLC increases, the cooling decreases. The maximum heat flux removed from the SLC corresponds to zero cooling. Hotspot heaters are fabricated at the top of the SLC and the power dissipated by the hotspot heaters act as heat load on the SLC. Since the size of the hotspot heaters and SLC are same, maximum hotspot heat flux removed will be equal to the CPD of the SLC. Figure 4-3 shows the effect of SLC size for the off-chip and on-chip microchannel respectively at room temperature. Ground electrode is located 400 μm away from the SLC. 70 μm x 70μm and



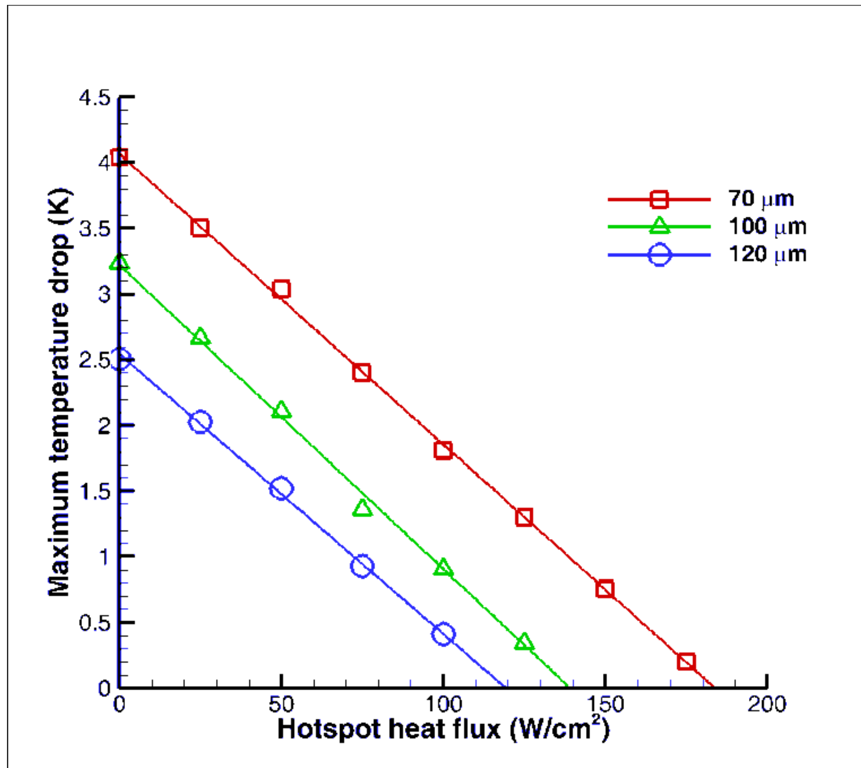


Figure 4-3: Effect of superlattice size: off-chip microchannel configuration (top) and on-chip microchannel configuration (bottom). Ambient temperature = 23 °C

100 μm x 100 μm SLCs were tested for off-chip configuration whereas additional 120 μm x 120 μm SLC is tested for on-chip configuration. As expected the maximum temperature drop and CPD decreases with increase in the SLC size. For the on-chip configuration, CPD corresponding to 70 μm x 70μm and 120 μm x 120 μm SLC is 180 W/cm^2 and 120 W/cm^2, respectively. Even though CPD is lower for larger superlattice coolers, total power dissipated by larger coolers is more compared to the smaller ones because of increase in the area.

4.1.4. Effect of working fluid

Microchannel heat sink not just removes the background heat dissipated from the die but also removes the heat generated due to Joule heating within the silicon substrate, superlattice, and buffer layer as well as Peltier heating generated at the ground electrode. A good thermal fluid will increase the efficiency of the microchannel heat sink to effectively remove heat generated due to Joule heating as well as Peltier heating, thus enhancing the performance of the superlattice cooler. Three different working fluids (water, FC72 and air) are circulated through the microchannel heat sink. Water has very good thermal properties, however it has relatively high freezing point and can short the electronic circuits. FC72 is dielectric fluid and well suited for electronics application but has poor thermal properties compared to water. Air is very widely used for electronics cooling. However it has very poor thermal properties. Convective heat transfer coefficient for water, FC72 and air is 30,000 W/m^2K, 3000 W/m^2K and 1300 W/m^2K, respectively. Figure 4-4 shows the performance of the superlattice cooler for these three working fluids. Superior the thermal fluid better the performance of superlattice cooler.

Maximum temperature drop for water, FC72 and air is $3.2\,K$, $2.8\,K$ and $1.6\,K$, respectively and CPDs are 150 W/cm^2, 130 W/cm^2 and 50 W/cm^2, respectively.

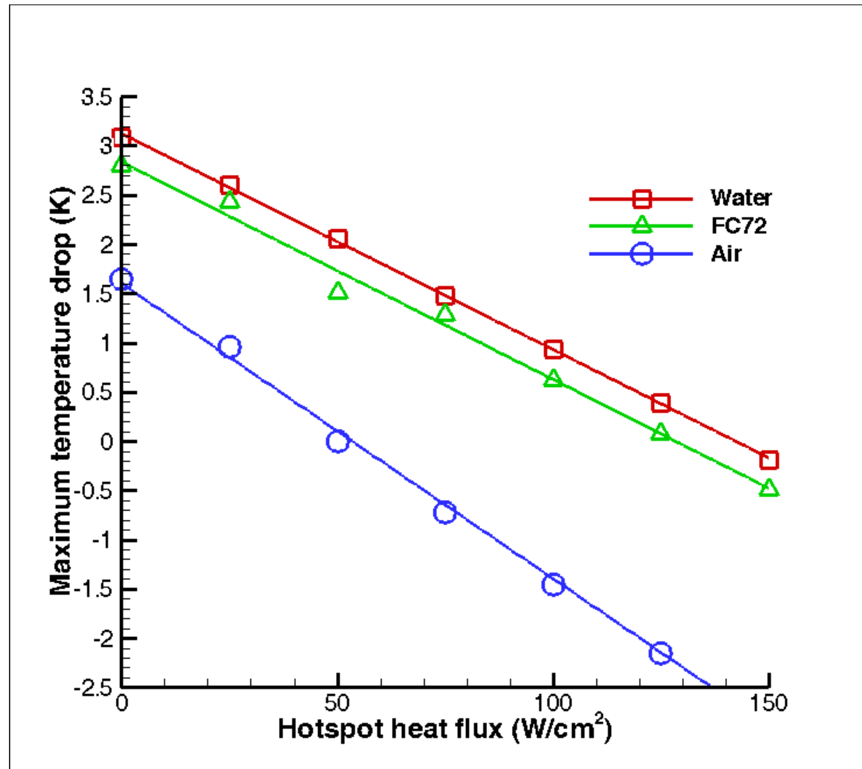


Figure 4-4: Effect of working fluid on the performance of 100 µm x 100 µm superlattice cooler for on-chip microchannel configuration. Ambient temperature = 23 °C, SLC size = 100 µm x 100 µm.

4.1.5. Spatial temperature distribution

Hotspot heater also serves as temperature sensor. Resistance of hotspot heater is converted to temperature using the resistance calibration curve. However, this technique only provides average temperature at the hotspot heater as well as superlattice cooler. It does not reveal any information regarding temperature distribution, or temperature gradients, across the superlattice cooler. Infrared imaging is used to study the spatial temperature distribution across the superlattice cooler. Infrared imaging can also measure the temperature of the substrate as well as ground electrode which is not possible to measure using the resistance thermometry.

Figure 4-5 compares the resistance thermometry with the infrared imaging. It shows the cooling obtained at 70 µm x 70 µm superlattice cooler measured using both techniques. For infrared imaging, temperature at the superlattice cooler is obtained by averaging it across the superlattice mesa. Both techniques show the same trend though IR technique measures less cooling compared to resistance thermometry. As mentioned in Chapter 3, samples are coated with a thin layer of graphite before performing infrared imaging. Presence of the graphite layer above superlattice cooler spreads the cooling obtained at the SLC and thus reduces the temperature drop. Reduction in the temperature drop at the superlattice cooler due to presence of the graphite layer can be estimated using resistance network analysis. Thickness of the graphite layer is measured to be between 5 µm to 20 µm, which result in 2.5 % to 10 % reduction in temperature drop.

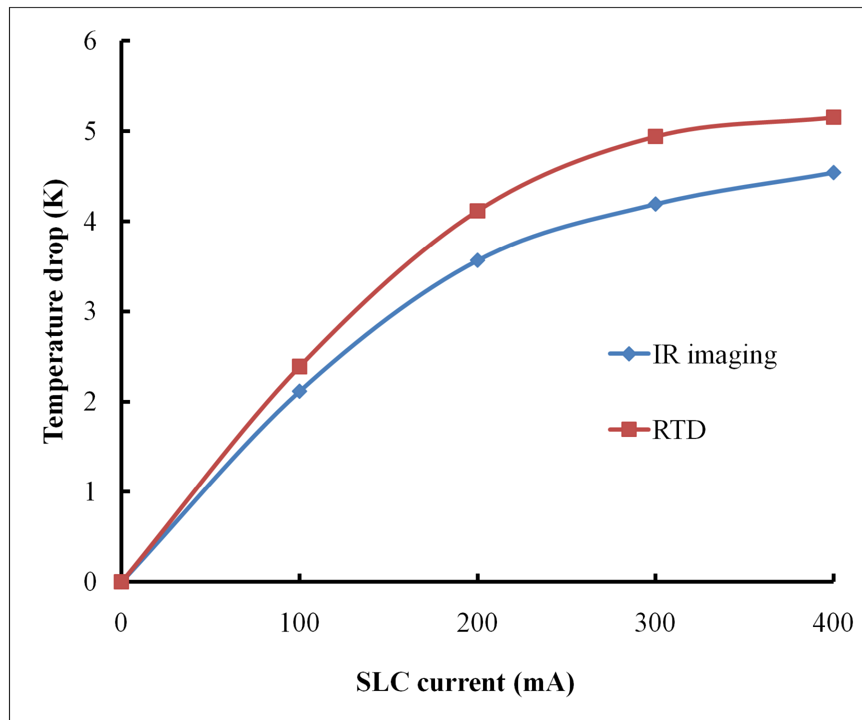


Figure 4-5: Comparison of infrared imaging with resistance thermometry. SLC size: 70 µm x 70 µm, Ambient temperature: 323 K.

Spatial temperature distribution across all three sizes of superlattice cooler is measured using infrared imaging. Figure 4-6 shows the spatial temperature distribution across 70 µm x 70 µm superlattice cooler under different activation current. Device is

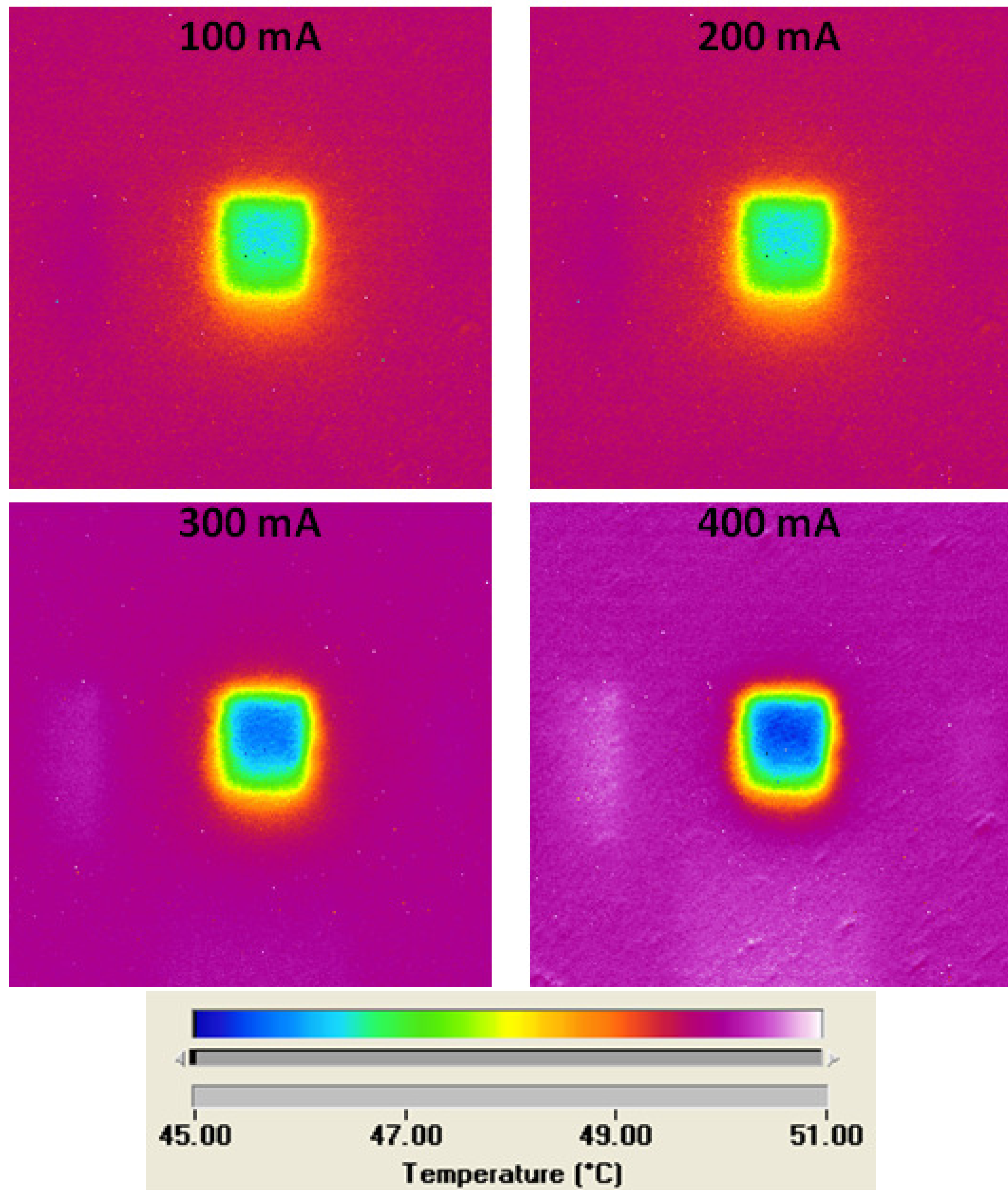


Figure 4-6: Spatial temperature distribution across 70 µm x 70 µm superlattice cooler at 50 °C ambient temperature.

heated to 50 °C by circulating preheated water through the microchannel. Temperature is uniform across the superlattice cooler under all activation current. Temperature at the superlattice drops with increase in the activation current. Moreover, temperature of the substrate also increases slightly with the activation current. As mentioned before, superlattice cooler generates more heat than the heat removed at the cold electrode. As the activation current increases, heat generated within the substrate and ground electrode increases. Thus, temperature of the substrate also increases with the activation current. Figure 4-7 shows the spatial temperature distribution across the same superlattice cooler. Temperature is fairly uniform across the superlattice cooler as well as substrate. Figure 4-8 and Figure 4-9 shows the spatial temperature distribution of 100 µm x 100 µm and 120 µm and 120 µm SLC, respectively. Furthermore, ground electrode temperature also increases with the activation current due to increased heat dissipation at the ground electrode. Figure 4-10 shows the spatial temperature distribution across the ground electrode for different superlattice cooler activation current. The temperature at the ground electrode increase by about a degree (at 400 mA activation current) due to Peltier heating.

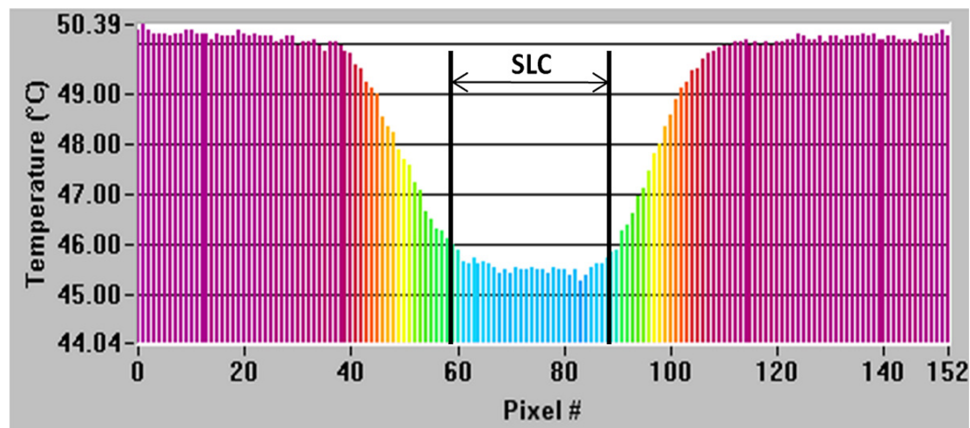


Figure 4-7: Temperature distribution across the line passing through the center of the superlattice cooler.

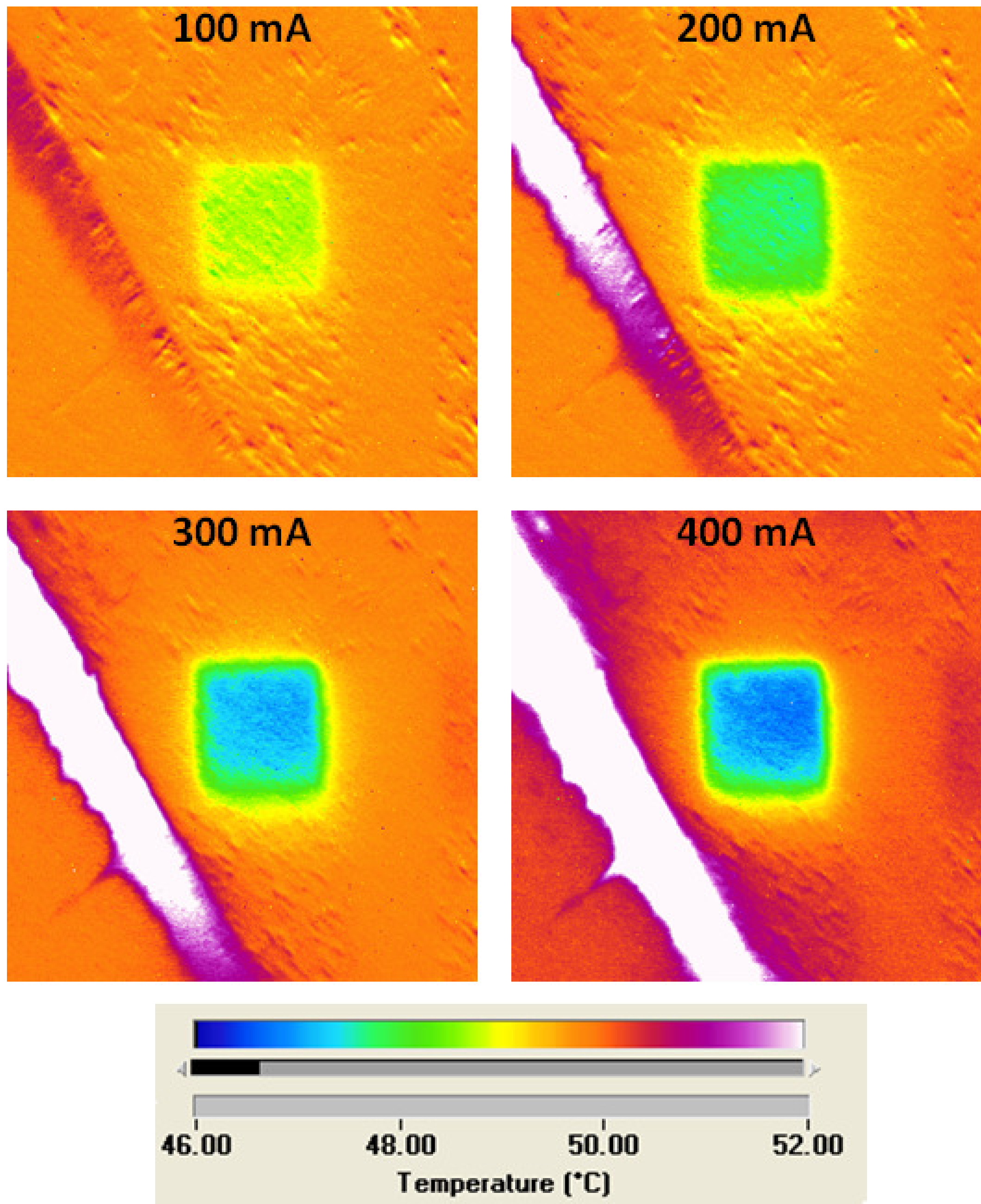


Figure 4-8: Spatial temperature distribution across 100 µm x 100 µm superlattice cooler at 50 °C ambient temperature. White band is the wire bonded to the superlattice cooler positive electrode. The wire heats up as the current going through it increases.

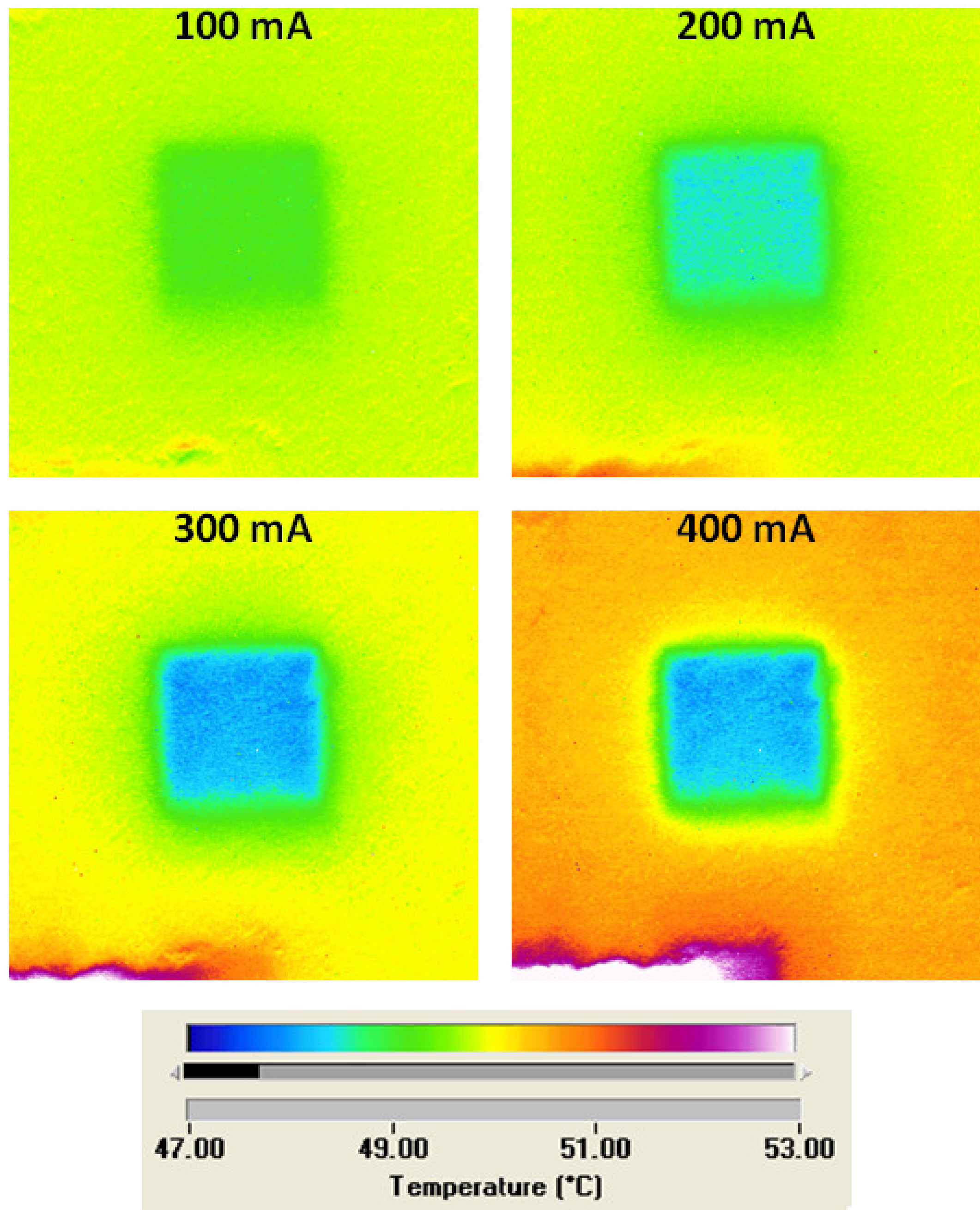


Figure 4-9: Spatial temperature distribution across 120 μm x 120 μm superlattice cooler at 50 °C ambient temperature.

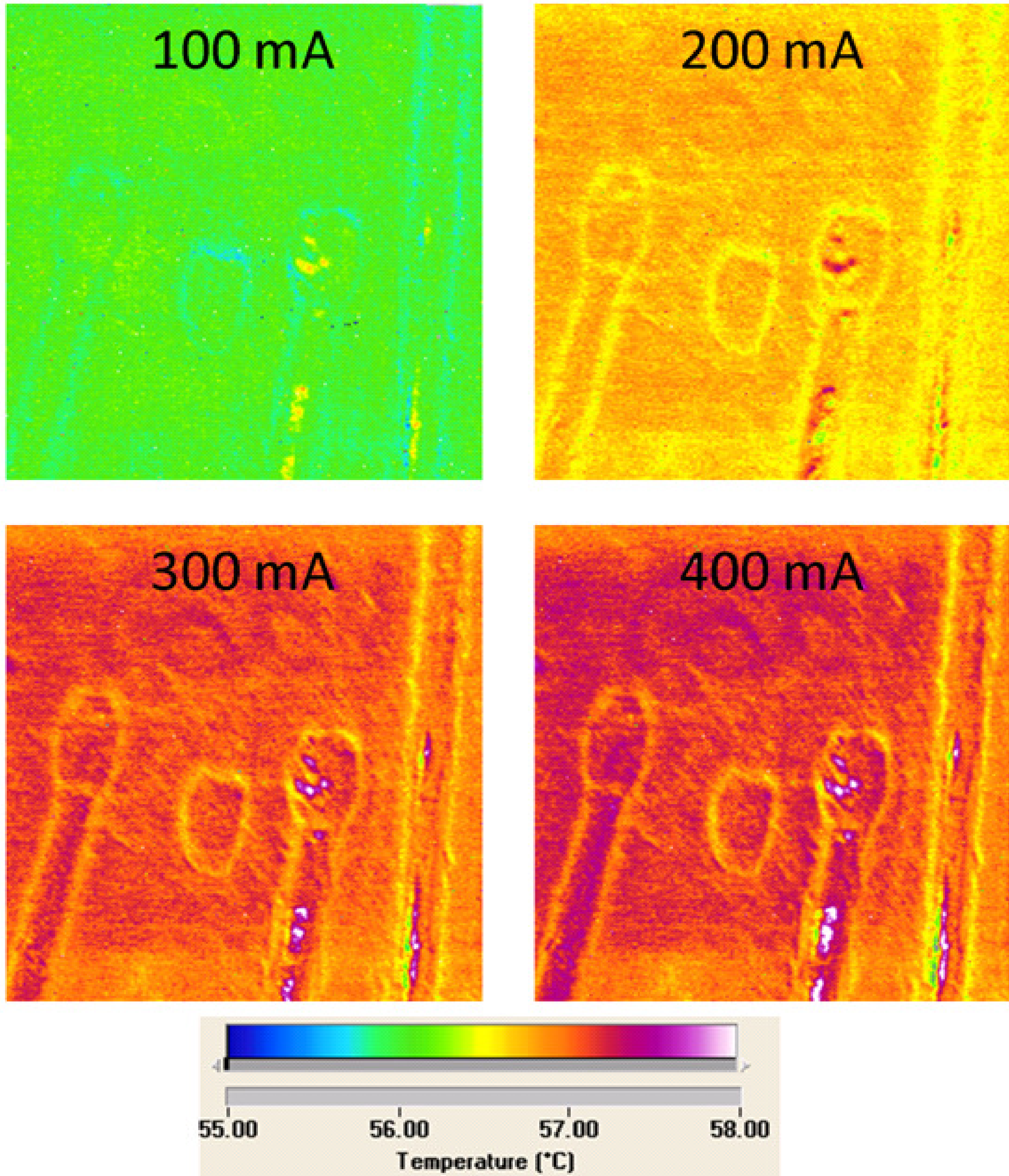


Figure 4-10: Spatial temperature distribution across ground electrode at 55 °C ambient temperature.

4.2. Resistance network model

Current state of the art materials have poor thermoelectric properties. Figure of merit of thermoelectric material is given by the term ZT which is defined as

$$ZT = \frac{S^2\sigma}{k}T \tag{4.1}$$

where, S is the Seebeck coefficient, σ is the electrical conductivity and k is the thermal conductivity and T is the temperature. Due to low ZT, thermoelectric materials are not gaining wide attention in the electronics applications. ZT for Si/SiGe superlattice at room temperature is 0.09. Several approaches have been described to increase the ZT of the thermoelectric material [91-93]. Resistance network model is developed to predict the performance of superlattice cooler for higher ZT materials.

Resistance network model for superlattice cooler has already been developed by Shakouri *et al*. [94] as well as Wang *et al* [95]. However, the authors assumed constant temperature boundary condition and did not include ground electrode in the model. The resistance network model presented in this work includes ground electrode and accounts for convective boundary condition. Inclusion of both these parameters makes the model more realistic and accurate, as well as allows us to study the effect of ground-superlattice thermal resistance and ground-heat sink thermal resistance, which is not possible with earlier models presented in the open literature.

Figure 4-11 shows the resistance network model. It accounts for Peltier cooling, Peltier heating as well as Joule heating in all the layers (except the substrate, where Joule heating is assumed to be negligible due to much larger volume of the substrate compared to superlattice). Joule heating is a volumetric term, which is not possible to directly model in resistance network analysis. Hence Joule heating for a particular layer is

included by bisecting the layer into two parts and adding a source term at the middle node. Peltier cooling and heating terms are included at the intersection of the layers where they occur.

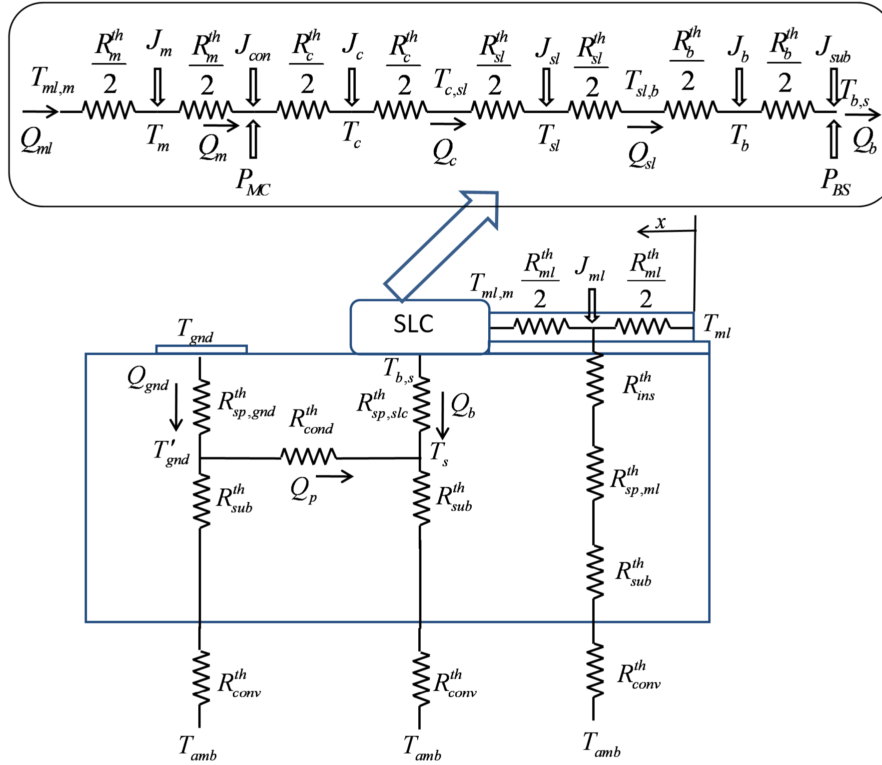


Figure 4-11: Resistance network diagram for hybrid cooling scheme.

4.2.1. Modeling of superlattice cooler

Current and heat flow in the superlattice is assumed to be perpendicular to the surface and spatially uniform. Top metal contact of the superlattice is assumed to be adiabatic, which is justified due to small size of superlattice cooler. Superlattice structure consists of four layers: metal, cap, superlattice, and buffer layer. Temperature difference across any layer is given by:

$$T_{in} - T_{out} = Q_{in} \times {R_l}/{2} + Q_{out} \times {R_l}/{2} \tag{4.2}$$

where, T_{in} and T_{out} are the temperature at either side of the layer, R_l is the thermal resistance of the layer, Q_{in} and Q_{out} are the heat going in and going out of the layer, which are related by the following expression

$$Q_{out} = Q_{in} + J_l \tag{4.3}$$

and

$$J_l = I^2 R_l^e \tag{4.4}$$

Here J_l is the Joule heating inside the layer, I is the current flowing through the layer, and R_l^e is the electrical resistance of the layer. Electrical and thermal resistances are respectively defined as:

$$R_l^{th} = \frac{\lambda}{kA} \tag{4.5}$$

$$R_l^e = \frac{\lambda}{\sigma A} \tag{4.6}$$

In Eqs (4.5) and (4.6) λ is the thickness, A is the cross section area perpendicular to heat flow, k is the thermal conductivity and σ is the electrical conductivity of the layer. Peltier cooling at the metal-cap and buffer-substrate interface is respectively defined as:

$$\begin{aligned} P_{MC} &= (S_m - S_c) I T_{MC} \\ P_{BS} &= (S_b - S_{sub}) I T_{BS} \end{aligned} \tag{4.7}$$

where, S is the Seebeck coefficient, and subscripts m, c, b and sub stand for metal, cap, buffer and substrate, respectively. T_{MC} and T_{BS} are the temperature at the metal-cap and buffer-substrate interface, respectively.

Eq (4.2) can be expressed for each layer in the superlattice structure and solved for temperature at the top of the superlattice microcooler yielding the following expression:

$$
\begin{aligned}
T_{ml,m} - T_s = & Q_{ml} \times R_m^{th} + \left(Q_{ml} + J_m + J_{con} - P_{MC}\right) \times R_c^{th} + \left(Q_{ml} + J_m + J_{con} + J_c - P_{MC}\right) \times R_{sl}^{th} \\
& + \left(Q_{ml} + J_m + J_{con} + J_c + J_{sl} - P_{MC}\right) \times R_b^{th} + \left(Q_{ml} + J_m + J_{con} + J_c + J_{sl} + J_b + J_{sub} - P_{MC} - P_{BS}\right) \times R_{sp,slc}^{th} \\
& + \frac{1}{2}\left(J_m \times R_m^{th} + J_c \times R_c^{th} + J_{sl} \times R_{sl}^{th} + J_b \times R_b^{th}\right)
\end{aligned}
\tag{4.8}
$$

Here $T_{ml,m}$ and T_s are the temperature at the top of the superlattice cooler, and substrate-cooler interface, respectively, Q_{ml} is the heat transport from the metal lead to the top of the superlattice cooler, J_i is Joule heating within layer and R_i^{th} is thermal resistance of layer (subscript $i = m, c, sl, b$ stands for metal, cap, superlattice and buffer layer respectively). J_{con} and J_{sub} are Joule heating source term due to finite electrical contact resistance at the metal-cap interface and electrical spreading resistance at buffer-substrate interface, respectively.

$$
\begin{aligned}
J_{con} &= I^2 R_{con}^e \\
J_{sub} &= I^2 R_{sp}^e
\end{aligned}
\tag{4.9}
$$

where, R_{con}^e is the electrical contact resistance. Typical value of electrical contact resistance is in the range 10^{-10} Ωm^2 to 10^{-11} Ωm^2 [96]. This analysis assumes electrical contact resistance of 5 x 10^{-11} Ωm^2. Approximating the superlattice cooler as a cylindrical disk, electrical spreading resistance can be written as:

$$
R_{sp}^e = \frac{8}{3\pi^2 \sigma_{sub}} \sqrt{\frac{\pi}{A_{SLC}}}
\tag{4.10}
$$

where, A_{SLC} is the cross sectional area of the superlattice cooler. Thermal spreading resistance from superlattice cooler to the substrate underneath it, can be calculated using the expression derived by Yovanovich *et al*. [97].

$$R^{th}_{sp,SLC} = \frac{1}{2a^2cdk}\sum_{m=1}^{\infty}\frac{\sin^2(a\alpha_m)}{\alpha_m^3}\varphi(\alpha_m) + \frac{1}{2b^2cdk}\sum_{n=1}^{\infty}\frac{\sin^2(b\beta_n)}{\beta_n^3}\varphi(\beta_n) + \frac{1}{a^2b^2cdk}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\sin^2(a\alpha_m)\sin^2(b\beta_n)}{\alpha_m^2\beta_n^2\delta_{m,n}}\varphi(\delta_{m,n}) \tag{4.11}$$

where,

$$\varphi(\zeta) = \frac{(e^{2\zeta\lambda_{sub}}+1)\zeta-(1-e^{2\zeta\lambda_{sub}})h/k}{(e^{2\zeta\lambda_{sub}}-1)\zeta+(1+e^{2\zeta\lambda_{sub}})h/k} \tag{4.12}$$

a and b are length and width of the substrate, respectively c and d are length and width of the heat source (superlattice), respectively, λ_{sub} is the thickness of the substrate, k is the thermal conductivity of substrate, and h is the heat transfer coefficient.

4.2.2. Modeling of heat transport in metal lead:

Power to superlattice cooler is delivered through metal lead. Even though, metal had two orders of magnitude higher electrical conductivity than silicon (10^7 $\Omega^{-1}m^{-1}$ as compared to 5 x 10^4 $\Omega^{-1}m^{-1}$) due to very high ratio of l/A, Joule heating in the metal lead is quite significant and cannot be ignored. A large portion of the heat generated in the lead diffuses to the top of superlattice cooler, reducing the cooling obtained at SLC. Heat transport in the metal lead can be calculated by treating it as a fin with constant volumetric heat generation term along with convective heat transfer from the side. Writing down the energy conservation for the metal lead yields following governing equation:

$$\frac{\partial^2 T}{\partial x^2} - \frac{h_{eff} P_{ml}}{k_{ml} A_{ml}} \left(T - T_{\infty} \right) + \frac{q'''}{k_{ml}} = 0 \tag{4.13}$$

where, k_{ml} is the thermal conductivity of metal lead, $A_{ml} = \lambda_{ml} w_{ml}$ is the cross sectional area of metal lead with λ_{ml} and w_{ml} being the thickness and width of metal lead respectively, h_{eff} is the effective heat transfer coefficient between metal lead and substrate underneath it, $P_{ml} = w_{ml}$ is the perimeter (through which heat transfer is taking place), q''' is the volumetric heat generation defined as:

$$q''' = \frac{I^2 R_{ml}^e}{A_{ml} l_{ml}} \tag{4.14}$$

Here $R_{ml}^e = \dfrac{l_{ml}}{\sigma_{ml} \lambda_{ml} w_{ml}}$ is the electrical resistance of metal lead, and l_{ml} is the length of metal lead. Heat transfer coefficient, h_{eff} is defined as

$$\frac{1}{h_{eff} l_{ml} w_{ml}} = R_{ins}^{th} + R_{sp,ml}^{th} + R_{sub}^{th} + R_{conv}^{th} \tag{4.15}$$

where, R_{ins}^{th}, $R_{sp,ml}^{th}$, R_{sub}^{th}, R_{conv}^{th} are the conduction resistance through insulation layer, spreading resistance, conduction resistance of substrate, and convective resistance, which are defined as:

$$\begin{aligned} R_{ins}^{th} &= \frac{\lambda_{ins}}{k_{ins} l_{ins} w_{ins}} \\ R_{sub}^{th} &= \frac{\lambda_{sub}}{k_{sub} l_{sub} w_{sub}} \\ R_{conv}^{th} &= \frac{1}{h_{base} l_{sub} w_{sub}} \end{aligned} \tag{4.16}$$

where, h_{base} is the convective heat transfer coefficient at the base of the substrate. Thermal spreading resistance from the insulation layer to the substrate underneath it can be calculated using Eq(4.11) by replacing the superlattice dimension with the metal lead. Eq (4.13) can be solved for temperature distribution in the metal lead using following boundary conditions:

$$\begin{aligned} &-k\left.\frac{\partial T}{\partial x}\right|_{x=0}=0 \\ &T_{x=l_{ml}}=T_{ml,m} \end{aligned} \tag{4.17}$$

Yielding the following expression for temperature along the metal lead.

$$\begin{aligned} &T(x)=T_{\infty}+\left(T_{ml,m}-T_{\infty}-\xi^{2}\frac{q'''}{k_{ml}}\right)\frac{\cosh(\xi x)}{\cosh(\xi l_{ml})} \\ &\xi=\sqrt{h_{eff}P_{ml}/k_{ml}A_{ml}} \end{aligned} \tag{4.18}$$

Heat transfer from the metal lead to the superlattice cooler can now be calculated using the following expression:

$$\begin{aligned} Q_{ml}&=-k_{ml}A_{ml}\left.\frac{\partial T}{\partial x}\right|_{x=l_{ml}} \\ &=-\sqrt{h_{eff}P_{ml}k_{ml}A_{ml}}\left(T-T_{\infty}-\xi^{2}\frac{q'''}{k_{ml}}\right)\tanh(\xi l_{ml}) \end{aligned} \tag{4.19}$$

4.2.3. Modeling of Joule heating in top metal layer

In order to accurately compute the volumetric heat generation due to ohmic heating, one needs an accurate estimate of the equivalent 1-D electric resistance of the top metal layer. Unfortunately, the current flow in the top metal layer is not strictly one-dimensional; it is flowing along the metal layer as well as perpendicular to its surface into the substrate. Moreover, the magnitude of current is decreasing along the length of the

layer due to transport of charge to the superlattice structure underneath it. Therefore, electrical resistance of the top metal layer cannot be calculated using Eq.(4.6), which assumes one-dimensional transport of charge. Since charge transport equation and heat transport equation are analogous, electrical resistance of the layer can be calculated if we can find thermal resistance of metal layer under identical boundary condition. Metal layer can be treated as a fin and heat transport along the layer is given by:

$$\frac{\partial^2 \theta}{\partial x^2} - \xi_{th}^2 \theta = 0 \; ; \; \xi_{th} = \sqrt{\frac{h_{eff}^{th} P_m}{k_m A_m}} \tag{4.20}$$

Here $\theta = T - T_\infty$ is temperature difference (voltage), h_{eff}^{th} is the effective heat transfer coefficient (inverse of leakage resistance), $A_m = t_m w_m$ is the cross sectional area of metal, and $P_m = w_m$ is the wetted perimeter (metal to substrate contact). Electrical boundary condition can be converted to analogous thermal boundary conditions to solve Eq. (4.20). Constant current input at the base of metal layer can be treated as constant heat input to the metal layer. Similarly, no current exist the tip of the metal layer, which can be treated as adiabatic boundary condition.

$$\begin{aligned} -kA_m \frac{\partial \theta}{\partial x}\bigg|_{x=l_{ml}} &= Q_{ml} \\ -kA_m \frac{\partial \theta}{\partial x}\bigg|_{x=l_{ml}+l_m} &= 0 \end{aligned} \tag{4.21}$$

where, Q_{ml} is the heat input (current) to the metal layer. Solution to Eq. (4.20) subject to above boundary condition is given by

$$\theta = Q_{ml} \frac{1}{\xi_{th}} \left(\frac{\sinh\{\xi_{th}(l_m + l_{ml} - x)\}}{\cosh(\xi_{th} l_m)} \right) \tag{4.22}$$

An equivalent thermal resistance of the fin is defined as:

$$\psi_m^{th} = \frac{\theta|_{x=l_{ml}}}{Q_{ml}} = \psi_{m,1D}^{th}\left(\frac{\tanh(\xi_{th} l_m)}{\xi_{th} l_m}\right) \tag{4.23}$$

where, ψ_{1D}^{th} is one-dimensional thermal resistance defined as:

$$\psi_{m,1D}^{th} = \frac{l_m}{k_m A_m} \tag{4.24}$$

Using the analogy between charge and heat transport we can define the electrical resistance as

$$R_m^e = R_{m,1D}^e\left(\frac{\tanh(\xi_e l_m)}{\xi_e l_m}\right) \tag{4.25}$$

where, $R_{m,1D}^e$ is one dimensional electrical resistance defined as

$$R_{m,1D}^e = \frac{l_m}{\sigma_m A_m} \tag{4.26}$$

with

$$\xi_e = \sqrt{\frac{h_{eff}^e P_m}{\sigma_m A_m}} \tag{4.27}$$

Here σ_m is the electrical conductivity of metal layer, and h_{eff}^e is defined in terms of electrical resistances:

$$h_{eff}^e = \frac{1}{(R_c^e + R_{sl}^e + R_b^e) l_m w_m} \tag{4.28}$$

Now, Joule heating in the top metal layer can be expressed as:

$$J_m = I^2 R_m^e \tag{4.29}$$

4.2.4. Parasitic heat transfer from ground electrode

Portion of heat dissipated at ground electrode is transferred to the superlattice, reducing the cooling at superlattice. The reduction in temperature due to parasitic heat transfer from ground electrode can be calculated by solving for the resistance network between superlattice and ground.

$$T_s - T_\infty = \left(Q_b + Q_p\right) \times \left(R_{sub}^{th} + R_{conv}^{th}\right) \tag{4.30}$$

$$T'_{gnd} - T_\infty = \left(Q_{gnd} - Q_p\right) \times \left(R_{sub}^{th} + R_{conv}^{th}\right) \tag{4.31}$$

$$T_{gnd} - T'_{gnd} = Q_{gnd} \times R_{sp,gnd}^{th} \tag{4.32}$$

$$T'_{gnd} - T_s = Q_p \times R_{cond}^{th} \tag{4.33}$$

where, Q_p is the parasitic heat transfer from the ground electrode to the superlattice, $R_{sp,gnd}^{th}$ is the spreading resistance from ground to substrate which can be calculated using eq. (4.11), Q_{gnd} is the heat dissipated at the ground electrode given by:

$$Q_{gnd} = \left(S_{sub} - S_m\right) I T_{gnd} \tag{4.34}$$

T_{gnd} is the temperature at the ground electrode. Eq. (4.8) and (4.30) - (4.33) can be used to solve for the temperature at the superlattice cooler ($T_{ml,m}$) if current supplied to superlattice is known.

4.3. Validation of resistance network model

Resistance network model is validated with experiments to verify the accuracy and consistency of the model. Table 4-1 shows the dimension and properties used in the model [98]. Figure 4-12 compares the resistance network model with the experiments. Contact resistance between the metal and cap layer is assumed to be 5 x 10^{-11} Ωm^2 [96].

The model matches well for larger superlattice (120 µm x 120 µm), however for smaller superlattice (70 µm x 70 µm), it deviates from experiments. The model assumes a constant value for electrical contact resistance, which in reality is a function of superlattice size leading to higher discrepancy for smaller superlattice. Moreover, deviation between model and experiments increases with operating current; this suggests that Joule heating within the superlattice structure is overestimated. Maximum error between model and experiment is 21 % for 70 µm x 70 µm superlattice at 400 mA operating current.

Table 4-1: Dimension and properties of the layers used in the analysis

Layer name	Length (l, µm)	Width (w, µm)	Thickness (λ, µm)	Thermal conductivity (k, W/mK)	Electrical conductivity (σ, $\Omega^{-1}m^{-1}$)	Seebeck coefficient (S, µV/K)
Top metal	100	100	0.8	150	10^7	8
Cap	100	100	0.9	6	2.884×10^5	235
Superlattice	100	100	3	6	3.65×10^4	235
Buffer	100	100	3	6	7.21×10^4	235
Metal lead	300	150	0.8	150	10^7	8
Insulation	300	150	0.3	1	10^{-9}	-
Substrate	15000	13000	500	150	5×10^4	540

4.4. Predicted performance of higher ZT material

Figure 4-13 shows the maximum temperature drop at the superlattice as a function of its size for three values of ZT: 0.1, 0.5 and 1.0. The change in ZT can be achieved by change in any of the three properties: thermal conductivity, electrical conductivity and Seebeck coefficient. However, change in the former two properties does not result in enhancement of the CPD. Since main goal of the superlattice cooler is to remove high power density hotspots, its CPD should be high. Therefore, change in the ZT is achieved by changing the Seebeck coefficient, while keeping thermal conductivity and electrical conductivity constant.

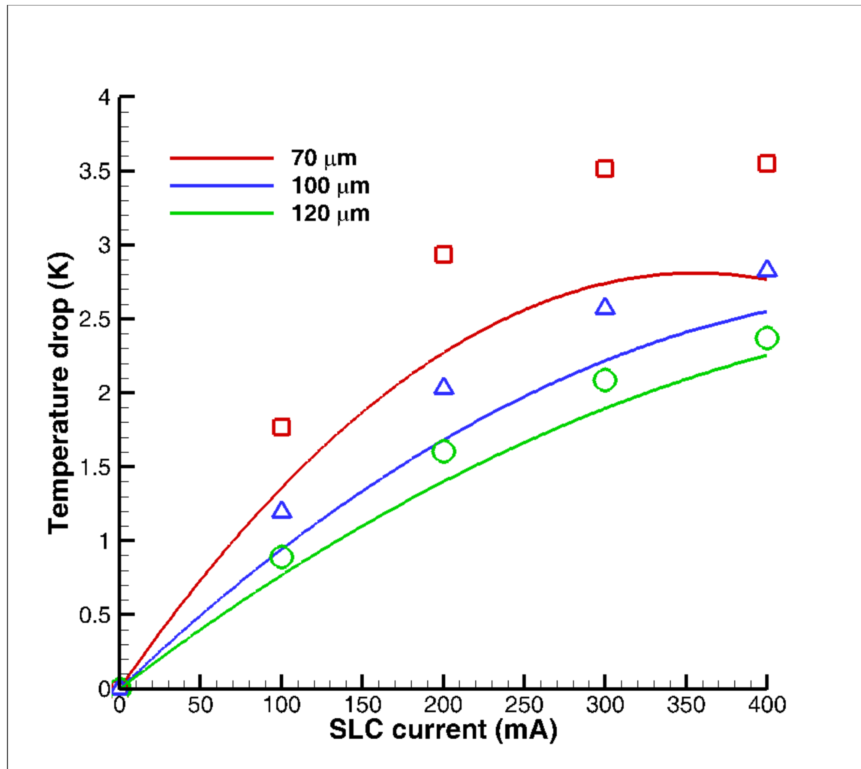


Figure 4-12: Comparison of resistance network model with experiments. Solid line represents the resistance network model. Symbols show the experimental values. Ambient temperature is 23 °C.

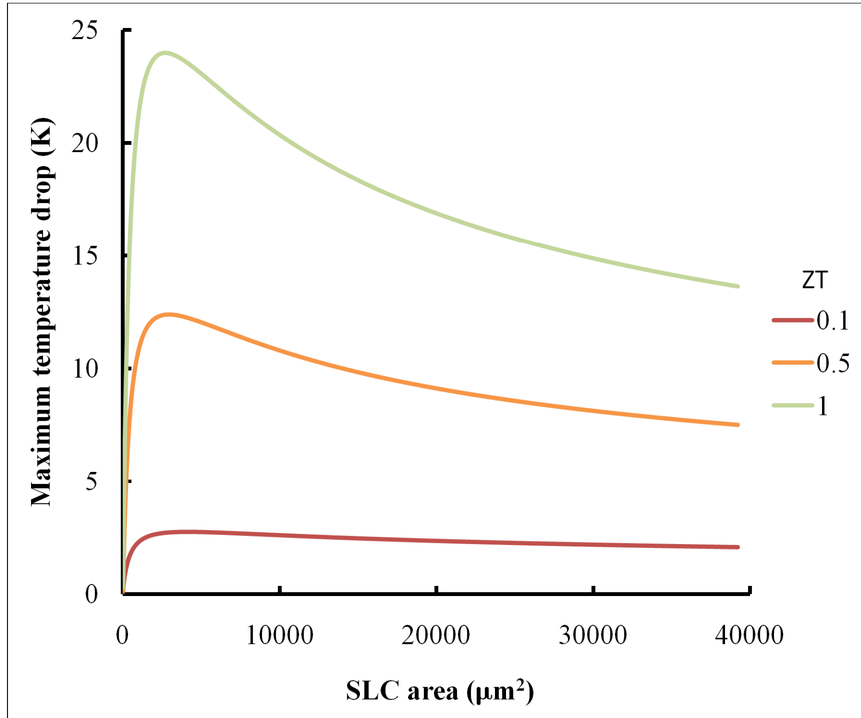


Figure 4-13: Maximum temperature drop obtained at the superlattice cooler as a function of its area for ZT of 0.1, 0.5 and 1. SLC is assumed to be square.

As mentioned earlier due to interplay between electrical and thermal spreading resistance as well as electrical contact resistance an optimum superlattice size exists. The resistance network model is able to predict the optimum superlattice size. The optimum superlattice size is 65 μm x 65 μm, 55 μm x 55 μm and 53 μm x 53 μm for ZT of 0.1, 0.5 and 1.0, respectively. As ZT increases, maximum temperature drop at the superlattice increases. For current state of the art superlattice material, ZT is close to 0.1 and maximum temperature drop obtained for these devices is $3\,K$. However, if ZT can be increased to 1.0 the maximum temperature drop will increase to $24\,K$.

Figure 4-14 shows the cooling power density of the superlattice cooler as a function of its size. CPD decreases monotonically with the superlattice size due to reduction in superlattice area. Even though CPD decreases with the area total power dissipated by the superlattice cooler increases with the area, as shown in Figure 4-15. For

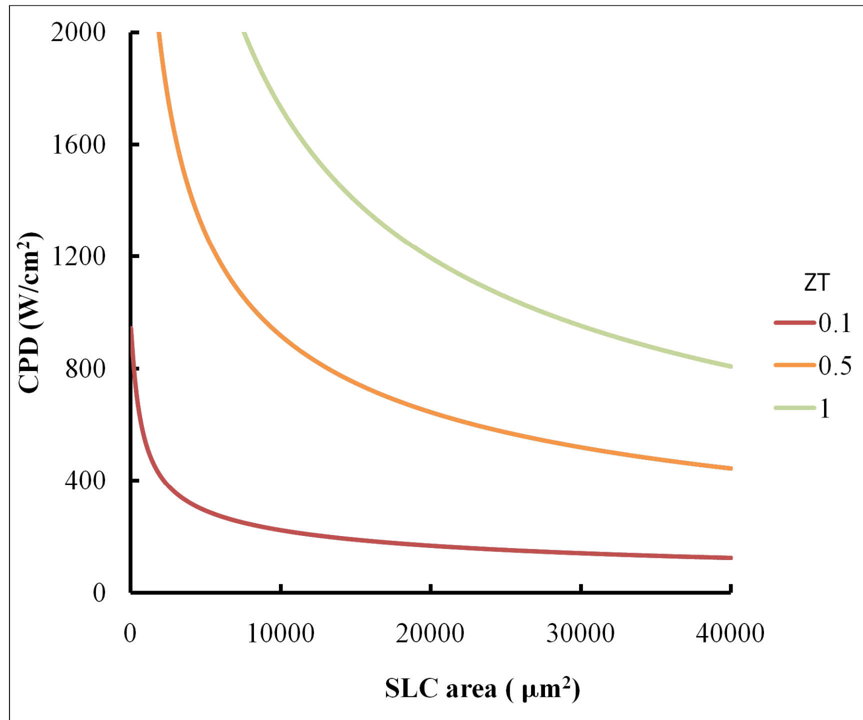


Figure 4-14: Cooling power density variation with the superlattice area shown for three ZT values. SLC is assumed to be square.

100 μm x 100 μm superlattice cooler CPD is 225 W/cm^2, 900 W/cm^2 and 1700 W/cm^2, corresponding to ZT of 0.1, 0.5 and 1.0, respectively.

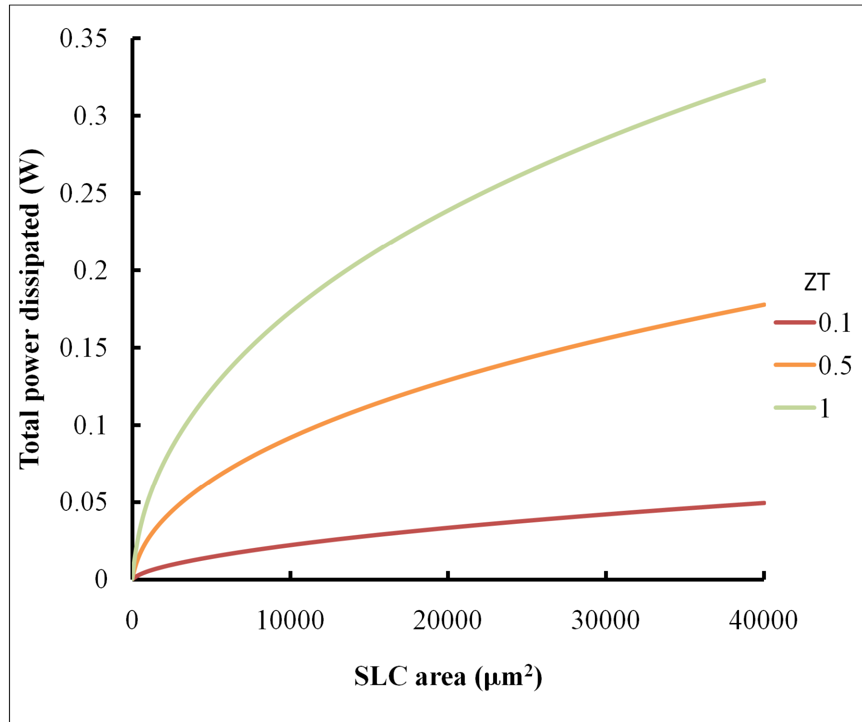


Figure 4-15: Total power dissipated by the superlattice cooler as a function of its area for ZT of 0.1, 0.5 and 1. SLC is assumed to be square.

4.5. Summary

Performance of the hybrid cooling scheme has been characterized under different operating conditions. Effect of the ambient temperature, SLC activation current, and choice of the working fluid has been studied on the cooling obtained at the superlattice cooler. Infrared imaging of the superlattice cooler has revealed uniform spatial temperature distribution across the superlattice cooler. Infrared imaging also reveals slight increase in the substrate temperature with the activation current which is not observed with the resistance thermometry. A detailed resistance network model of the superlattice cooler is developed to study the effect of enhanced ZT on the performance of

the superlattice cooler. As expected, both maximum cooling, as well as CPD, obtained by the superlattice cooler increases with ZT.

CHAPTER 5: EFFECT OF INTERFACE AND THERMAL RESISTANCE

In this chapter, the effect of interface thermal resistance, as well as thermal resistance between the ground electrode and superlattice, on the performance of hybrid scheme is investigated. Two test configurations, one with off-chip microchannels and other with on-chip microchannel are used to study the effect of interface resistance. Effect of thermal resistance is analyzed by changing the ground electrode location, as well as changing the working fluid.

5.1. Effect of interface thermal resistance

In addition to dissipating the background heat flux, microchannel heat sink also removes the heat dissipated at the ground electrode as well as heat generated due to Joule heating in the superlattice, buffer layer and within the silicon substrate. In the presence of inefficient heat sink, Joule heating in the substrate, buffer layer and superlattice will diffuse to the superlattice cooler, thus reducing its performance. Furthermore, there is also slight reduction in the SLC performance due to the parasitic heat transfer from the ground electrode to the superlattice cooler, when ground electrode is located within few characteristic diameter of the superlattice cooler. The presence of interface layer, adds additional thermal resistance between silicon substrate and microchannel heat sink, which reduces the effectiveness of heat sink in removing the heat generated due to Joule heating inside the silicon substrate, buffer layer and superlattice layer. To study the effect of interface resistance two types of devices are used. One of the devices has microchannel fabricated on the back of the superlattice cooler die. Other device has microchannel

fabricated on a separate wafer and then bonded to the die with superlattice cooler using SU8.

Figure 5-1 shows the maximum temperature drop at 100 μm x 100 μm SLC for both configurations at room temperature. As expected, on-chip configuration performs better than off-chip configuration. For the same operating current, on-chip configuration provides higher temperature reduction, suggesting more efficient removal of the heat. The maximum temperature reduction for the off-chip and on-chip configuration is 0.6 K and 3 K, respectively. The significant reduction in the superlattice cooler performance in off-chip configuration as compared to on-chip configuration is because of inefficient removal of heat generated due to Joule heating inside the superlattice, buffer layer and silicon substrate. This can be seen by studying the cooling curve of the superlattice cooler (Figure 4-1). Since the optimal current between on-chip and off-chip microchannel configurations is different, the reduction in the performance of the superlattice cooler is due to diffusion of Joule heating (term dependent on square of the current) in the superlattice, buffer and silicon substrate to the superlattice cooler.

5.2. Effect of thermal resistance between superlattice and ground electrode

Besides placement of microchannel heat sink, location of the ground electrode is also critical in designing the layout of the hybrid cooling scheme. When superlattice cooler is activated, electrical current flows from the superlattice cooler to the ground electrode. The current spreads at the superlattice-silicon substrate, as it flows from a small superlattice cooler to a much larger substrate underneath it. The electrical spreading at the superlattice-silicon interface result in Joule heating, which diffuses to the cold side

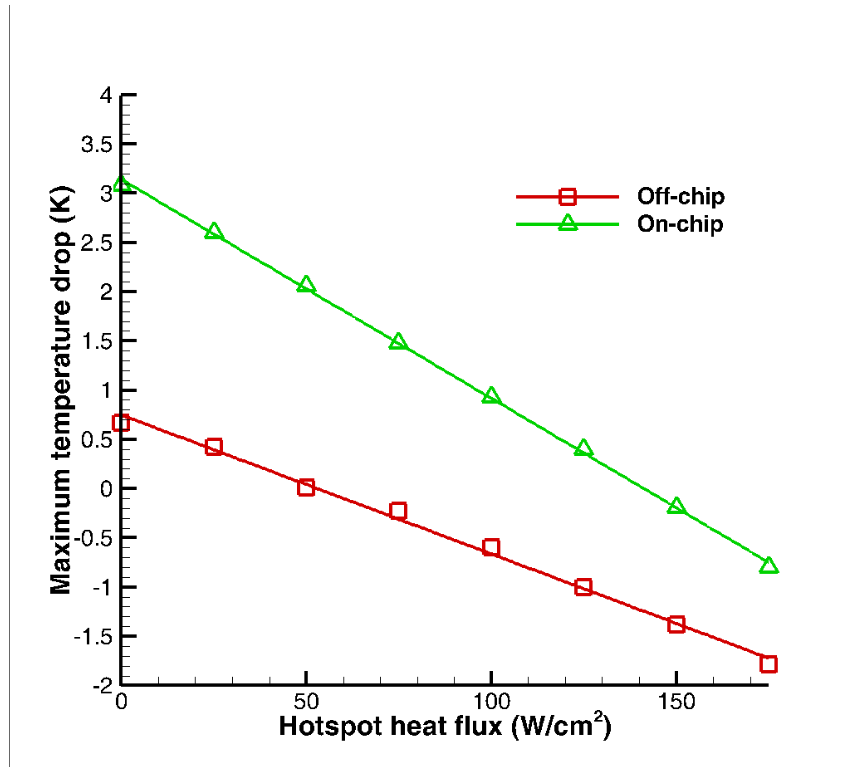
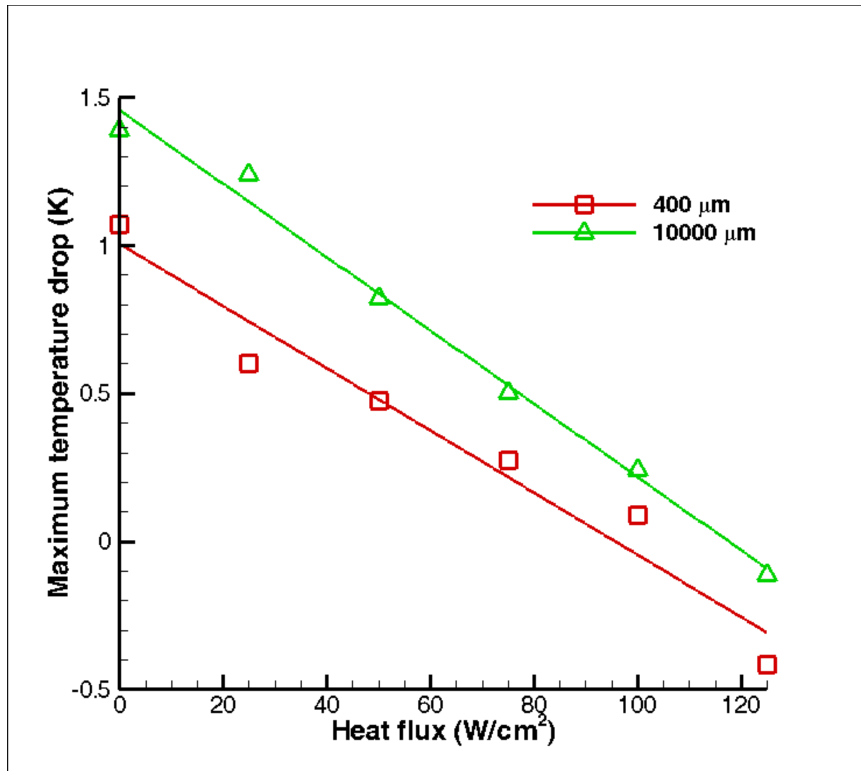


Figure 5-1: Comparison of off-chip and on-chip microchannel configuration. SLC size: 100 µm x 100 µm, ambient temperature: 23 °C, ground electrode located 400 µm from the SLC.

of the superlattice cooler, thus decreasing the cooling obtained at the cooler. Joule heating at the superlattice-silicon interface is dependent upon the distance between superlattice cooler and ground electrode. When the ground electrode is located very close to the superlattice cooler, current density near the superlattice-silicon interface is high, resulting in higher Joule heating at the interface. As the ground electrode is moved far, current density near the superlattice cooler decreases. This decreases Joule heating at the superlattice-silicon interface and enhances the performance of the superlattice cooler. If the separation distance between the ground electrode and superlattice cooler is more than few characteristic diameters of the superlattice cooler, change in the local Joule heating at the superlattice-silicon interface is not significant. Thus, performance of the SLC will not be affected by the ground electrode location beyond a certain separation distance.

Furthermore, heat dissipated at the ground electrode also slightly influences the performance of the superlattice cooler. Heat dissipated at the ground electrode spreads in the substrate and is eventually removed by the microchannel heat sink. The amount of parasitic heat transferred from the ground electrode to the superlattice cooler, depends upon the thermal resistance between the ground electrode and superlattice cooler. If superlattice cooler is placed close to the ground electrode (within few characteristic diameter of the superlattice), cooling obtained at the superlattice cooler will be slightly affected by the ground electrode location. However, as the ground electrode is moved farther away, thermal resistance between the ground electrode and superlattice cooler increases, reducing parasitic heat transfer from ground to superlattice cooler. When separation distance between the ground electrode and superlattice cooler is more than few characteristic diameters, parasitic heat transfer too becomes negligible and does not affect the performance of the SLC.

Figure 5-2 shows the maximum temperature drop obtained as a function of the hotspot heat flux for off-chip and on-chip configuration for (70 μm x 70 μm) the SLC at room temperature. Results are presented for two ground electrode locations. One ground electrode is placed about 0.4 mm apart from the SLC, and other is located about 10 mm away from the SLC. The maximum temperature drop decreases from 1.4 K to 1.1 K for the off-chip configuration. Moreover, the optimum current also increases from 250 mA to 300 mA. For the on-chip configuration maximum temperature drop is 4 K and is unaffected by the ground electrode location and corresponding maximum heat flux removed is 175 W/cm^2.



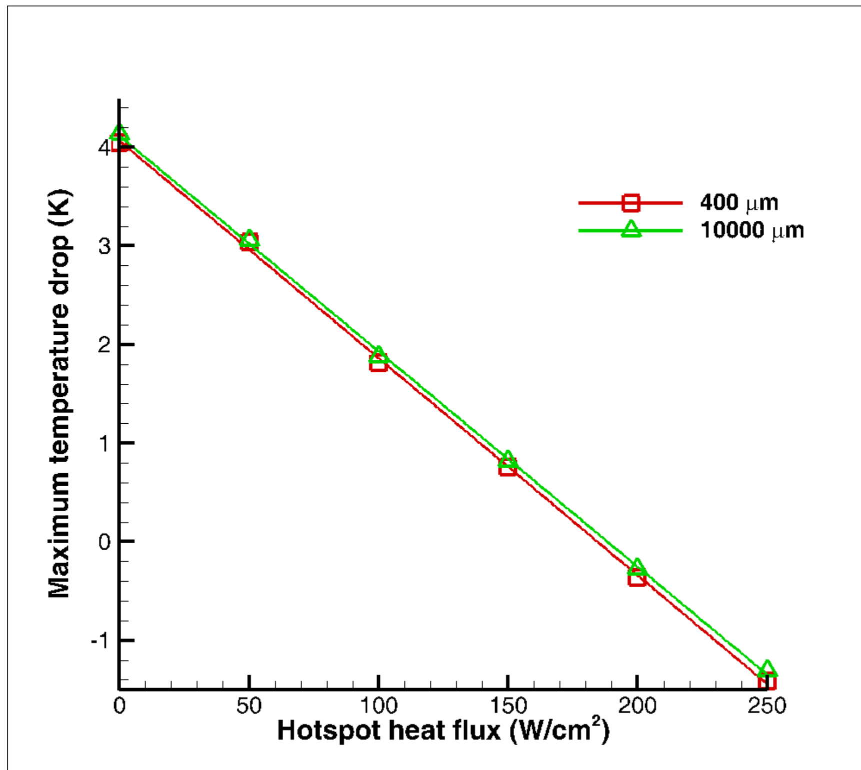


Figure 5-2: Effect of ground electrode location for (top) off-chip configuration, and (bottom) on-chip configuration. Ambient temperature = 23 °C, SLC size = 70 μm x 70 μm.

For the off-chip microchannel configuration, as the heat from ground electrode is not well heat sinked, more parasitic heat is transferred to the superlattice, reducing the cooling at SLC by 0.3-0.4 ^{o}C. However, the on-chip configuration is largely unaffected by the ground electrode location, which implies that the heat sink is effective enough to remove the heat dissipated at the ground electrode as well as heat generated due to electrical spreading. This does not mean superlattice cooler, in on-chip arrangement, is completely indifferent to the ground electrode location. When it is within characteristic diameters of the superlattice cooler, it will start affecting the performance of the superlattice cooler.

Even though net cooling obtained for on-chip configuration is not altered by the location of ground electrode, power input to the SLC is significantly higher when the ground electrode is moved further away from the SLC due to increase in the substrate electrical resistance. Total electrical resistance between the SLC and ground electrode increases from 1 Ω to 8.7 Ω when the ground electrode is moved from 0.4 mm to 10 mm away. Figure 5-3 shows the power input to the SLC as a function of activation current. Moving the electrode farther away will require almost 9 times more power input to achieve the same temperature drop at the hotspot.

The ambient temperature also affects the performance of superlattice cooler. As the ambient temperature increases, thermal conductivity of silicon decreases [88, 89] thus increasing the thermal resistance between the Joule heating sources and the heat sink. Figure 5-4 shows the maximum temperature drop obtained as a function of temperature and ground electrode location for 100 μm x 100 μm SLC for the off-chip microchannel configuration. Even though the maximum temperatures drop increases when the ground

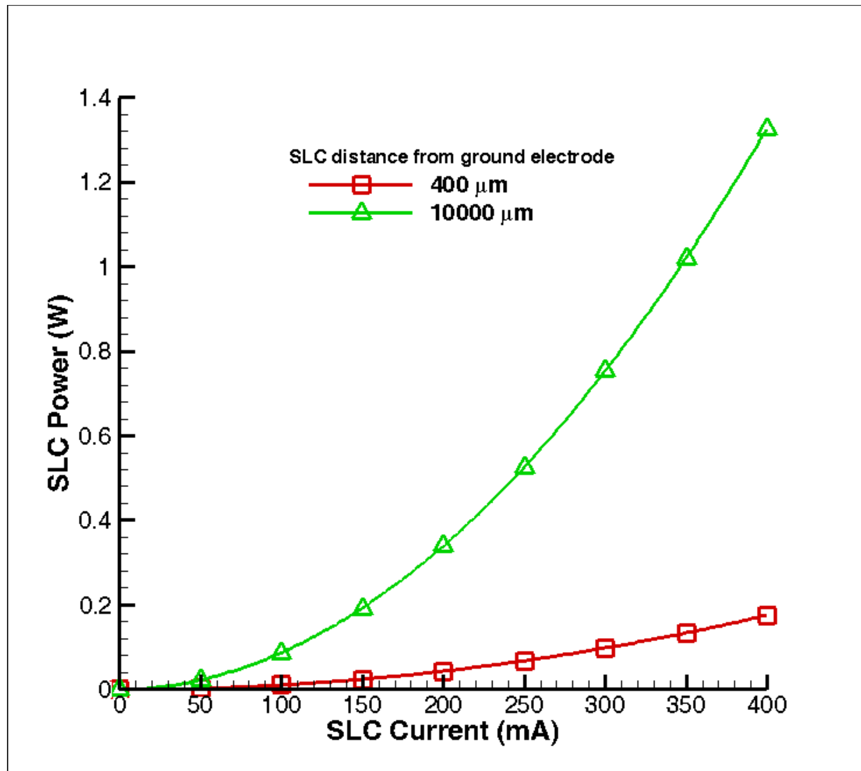


Figure 5-3: Power required by SLC for on-chip microchannel configuration for two different ground electrode locations.

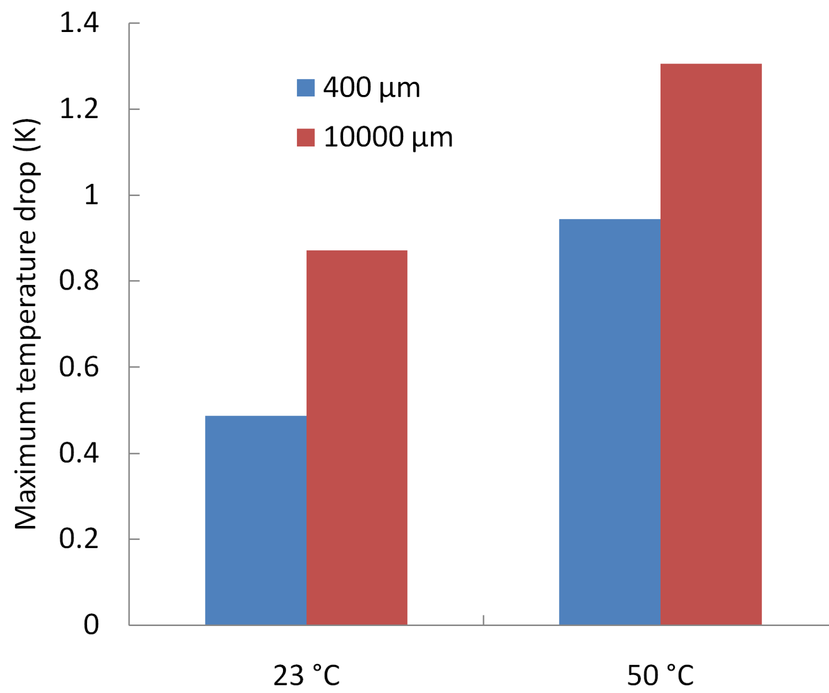


Figure 5-4: Effect of ground electrode location at different ambient temperature for 100 μm x 100 μm superlattice cooler on off-chip microchannel device.

electrode is moved farther away from SLC at both operating temperature, the enhancement is SLC performance is more at lower temperature. At 23 °C, maximum temperature drop increases by 79% when ground electrode is moved farther away, whereas at 50 °C, enhancement in maximum temperature drop is only 33% when ground electrode is moved from 400 μm to 10000 μm.

5.3. Summary

In this chapter the effects of interface and thermal resistance are investigated. On-chip microchannel configuration provides more than twice the cooling than off-chip configuration due to more efficient removal of the heat generated due to Joule heating within the superlattice layers, as well as silicon substrate. Presence of interface layer adds additional thermal resistance between the silicon substrate and microchannel heat sink, which reduces the heat removing capability of the microchannel heat sink. Placement of ground electrode is another critical parameter affecting the cooling as SLC. Local Joule heating at the superlattice-silicon interface changes with the ground electrode location, affecting the performance of superlattice cooler. Parasitic heat transfer from ground electrode to the superlattice cooler does not appreciably reduce the performance of the superlattice cooler. The effect of ground location is negligible if separation distance between the ground electrode and superlattice cooler is more than few characteristic diameters of the superlattice cooler. However, as the ground electrode is moved farther away from the superlattice cooler, power required to operate the superlattice cooler increase due to increase in the substrate thermal resistance.

CHAPTER 6: EFFECT OF THERMAL COUPLING BETWEEN SUPERLATTICE COOLERS

Hybrid cooling scheme utilizes an array of superlattice coolers to remove hotspots which do not have fixed location or have much bigger size compared to the superlattice cooler. However, an array of superlattice coolers can thermally interact with one-another, affecting the performance of individual superlattice coolers. Due to thermal coupling, performance of a single isolated superlattice cooler can be drastically different than the performance of the same superlattice cooler in an array. An electro-thermal model is developed to study the thermal coupling between superlattice coolers and the effect of geometric (location of ground electrode) and operating parameters (convective heat transfer coefficient between superlattice cooler and heat sink) on the performance of an array of superlattice coolers. We have also experimentally studied the thermal coupling between superlattice coolers under various test conditions. A sound understanding of these affects is critical for designing the hybrid scheme.

6.1. Computational modeling

The electro-thermal model solves the heat conduction equation, electrical charge continuity and constitutive relations to yield the temperature and electrical potential field in the domain. The following section describes the simulation geometry, governing equations along with boundary conditions and its implementation in COMSOL multiphysics solver.

6.1.1. Simulation geometry

Figure 6-1 shows the computational geometry. It consists of a 500 μm thick silicon substrate with superlattice coolers and ground electrode. Since fluid flow characteristics inside the microchannel heat sink are not of interest in this study, to save computational time microchannels are not included in the simulation. Instead the effect of microchannel heat sink is included through a convective boundary condition at the base of the substrate. The convective heat transfer coefficient is adjusted to account for the absence of the microchannel heat sink. Area of the superlattice cooler is kept constant in the simulations and is equal to 100 μm x 100 μm. Distance between superlattice coolers (Δs), as well as between superlattice cooler and ground electrode (Δg), are varied in the simulations. Baseline case has Δs = 100 μm and Δg = 400 μm. Metal leads and insulation layer (between the substrate and metal lead) have very high aspect ratio. Typical thickness of metal and insulation layer is few hundreds of nanometer, whereas length and width of these layers usually range from 200 μm to 300 μm. Due to very high aspect ratio (ranging from 100 to 1000) of these layers, mesh generation is challenging and require excessive number of elements as well as a significant increase in the computational time. Number of elements can be significantly reduced for these layers if one can increase the thickness of the layers (reduce aspect ratio) and adjust the properties so that electrical and thermal resistance of the layer remains unaltered. This can be done only if heat/charge transport in these layers is one dimensional. Due to high aspect ratio heat transfer can be assumed one-dimensional in these layers. Moreover, due to presence of insulation layer underneath the metal lead layer, current flow in the metal lead will be one-dimensional except close to superlattice junction. One-dimensional nature of current

and heat flow allows to artificially increase the computational thickness of these layers as long as thermal and electrical resistance of layers remain unchanged. Metal lead and insulation layer thickness is increased to 2 μm and 1 μm, respectively, and modified electrical and thermal properties of these layers are calculated as follows:

$$\left(\frac{\lambda}{kA_t}\right)_{\text{modified}} = \left(\frac{\lambda}{kA_t}\right)_{\text{actual}} \tag{6.1}$$

$$\left(\frac{l}{\sigma A_e}\right)_{\text{modified}} = \left(\frac{l}{\sigma A_e}\right)_{\text{actual}} \tag{6.2}$$

where, λ is the thickness of the layer, k is the thermal conductivity, A_t is the area perpendicular to the layer (x-z plane), l is the length of the layer (along the x direction), σ is the electrical conductivity, A_e is the cross sectional area of the layer (y-z plane). Table 6-1 shows the dimensions and properties of each layer used in simulations.

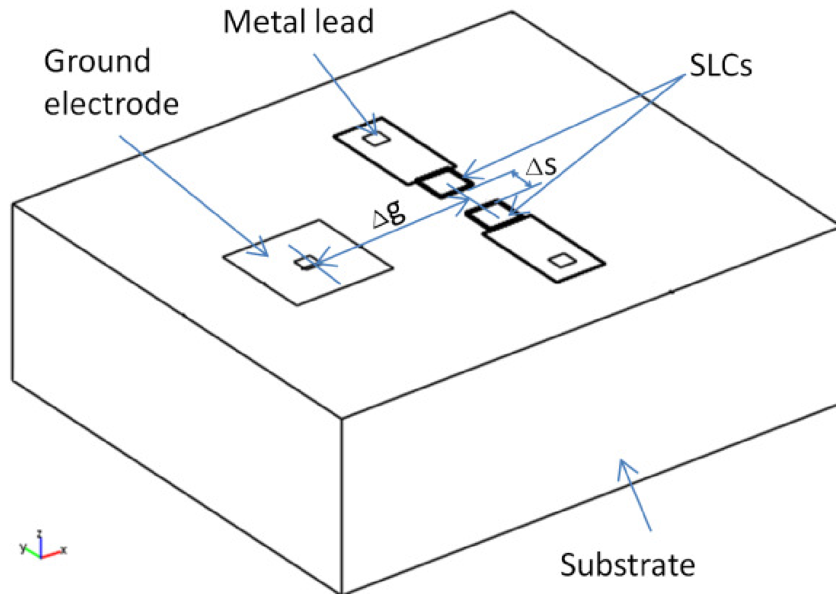


Figure 6-1: Schematic of simulations geometry. Δs is the spacing between superlattice coolers whereas Δg is the spacing between superlattice and ground electrodes.

Table 6-1: Properties used in the simulations

Layer name	Length (l, μm)	Width (w, μm)	Thickness (λ, μm)	Thermal conductivity (k, W/mK)	Electrical conductivity (σ, $\Omega^{-1}m^{-1}$)	Seebeck coefficient (S, μV/K)
Top metal	100	100	0.8	150	10^7	8
Cap	100	100	0.9	6	2.884×10^5	235
Superlattice	100	100	3	6	3.65×10^4	235
Buffer	100	100	3	6	7.21×10^4	235
Metal lead	300	150	2	150	10^7	8
Insulation	300	150	1	1	10^{-9}	-
Substrate	15000	13000	500	150	5×10^4	540

6.1.2. Governing equations

Temperature field is obtained by solving the heat conduction equation,

$$\rho c_p \frac{\partial T}{\partial t} + \nabla \bullet \mathrm{q} = q''' \tag{6.3}$$

where, ρ is the density, c_p is the specific heat, t is time, q is the heat flux vector, and q''' is the volumetric heat generation term. The heat is generated in the system due to Joule heating in the layers as well as Joule heating due to contact resistance between the metal and cap layer. The heat flux vector and volumetric heat generation terms are defined as:

$$\mathrm{q} = -k\nabla T \tag{6.4}$$

$$q''' = \mathrm{J} \bullet \mathrm{E} \tag{6.5}$$

Eq. (6.5) does not account for the Joule heating due to finite electrical contact resistance. Joule heating due to contact resistance is modeled as a constant heat generation term and included in the cap layer.

$$q_c''' = \frac{I^2}{V_c} \times \frac{R_{con}'^{e}}{A_c} \tag{6.6}$$

where, I is the current flowing through the superlattice, R'^{e}_{con} is the specific electrical contact resistance at the metal-cap interface, A_c is the surface area of the cap layer, and V_c is the volume of the cap layer. Electrical contact resistance at the metal-cap resistance is an unknown and varies from device to device. Depending upon the fabrication processes and conditions, electrical contact resistance can vary between 10^{-10} to 10^{-11} Ωm^2 [96]. In the simulations, it is assumed to be 5 x 10^{-11} Ωm^2.

Current density is obtained by solving the electrical charge continuity equation:

$$\nabla \bullet \left(\mathrm{J} + \varepsilon \frac{\partial \mathrm{E}}{\partial t} \right) = 0 \tag{6.7}$$

Here, J is the electrical current density, ε is the electrical permittivity, E is the electrical field defined as negative gradient of electrical potential.

$$\mathrm{E} = -\nabla V \tag{6.8}$$

Equation (6.3) and (6.7) require constitutive relations to solve the temperature and potential field. Following constitutive relations are used to couple the temperature and potential field:

$$\mathrm{q} = \Pi \mathrm{J} - k \nabla T \tag{6.9}$$

$$\mathrm{J} = \sigma(\mathrm{E} - S \nabla T) \tag{6.10}$$

Here, S is the Seebeck coefficient, Π is the Peltier coefficient defined as

$$\Pi = ST \tag{6.11}$$

Substituting expressions for q, q''' and J into Eq. (6.3) and (6.7), and dropping the time dependent terms yields coupled non-linear system of partial differential equations for temperature and electric potential.

$$\nabla \bullet \left\{ -\left(k + \sigma S^2 T \right) \nabla T - \sigma S T \nabla V \right\} = \sigma S \nabla T \bullet \nabla V + \sigma \left| \nabla V \right|^2 \tag{6.12}$$

$$\nabla \bullet \{\sigma S \nabla T + \sigma \nabla V\} = 0 \tag{6.13}$$

6.1.3. Boundary conditions

Convective boundary condition is applied at the substrate bottom with a constant heat transfer coefficient and ambient temperature. To simulate heat rejection in microchannel heat sink convective heat transfer coefficient at the base of the substrate (h_{base}) is calculated as:

$$h_{base} = \eta \frac{A_{tot}}{A_{base}} h_{channel} \tag{6.14}$$

where, η is the efficiency of the microchannel heat sink, A_{tot} is the total area of the microchannel heat sink, A_{base} is the area of the base of the substrate, and $h_{channel}$ is the average convective heat transfer coefficient inside the microchannel heat sink. Remaining walls are assumed adiabatic.

$$q = \begin{cases} h_{base}(T - T_{\infty}) & \text{base of the substrate} \\ 0 & \text{other walls} \end{cases} \tag{6.15}$$

where, T_{∞} is the ambient temperature. Ground electrode is kept at zero potential.

$$V = 0 \tag{6.16}$$

A constant current source is input at the metal electrode on the top of the superlattice cooler. All other walls have zero current.

$$\hat{\mathrm{n}} \bullet \mathrm{J} = \begin{cases} \text{constant} & \text{electrode contact} \\ 0 & \text{other walls} \end{cases} \tag{6.17}$$

At the interface between different layers voltage and potential are assumed to be same, as well as heat flux and current are assumed to be continuous.

$$
\begin{aligned}
-k_1 \frac{\partial T}{\partial n}\bigg|_1 &= -k_2 \frac{\partial T}{\partial n}\bigg|_2 + (\hat{\mathrm{n}}\bullet \mathrm{J})(S_1 - S_2)T_{\mathrm{int}} \\
T_1 &= T_2 \\
(\hat{\mathrm{n}}\bullet \mathrm{J})_1 &= (\hat{\mathrm{n}}\bullet \mathrm{J})_2 \\
V_1 &= V_2
\end{aligned}
\tag{6.18}
$$

Here, 1 and 2 are the two different sides of the interface, and T_{int} is the temperature of the interface.

6.2. COMSOL implementation

COMSOL PDE mode in the coefficient form is used to solve the coupled temperature and electrical potential equation (Eq. (6.12) and Eq. (6.13)). COMSOL PDE coefficient form is given as:

$$
d_a \frac{\partial u}{\partial t} + \nabla \bullet \left(-c\nabla u - au + \gamma\right) + \beta \bullet \nabla u + au = f \tag{6.19}
$$

where, the first term represents the transient term, second term represents the diffusion term, third term represents the convective term and fourth term is the absorption term. Right hand side represents the source term. u is the dependent variable, d_a is the damping coefficient, c is the diffusion coefficient, a is the absorption coefficient, α is the conservative flux convection coefficient, β is the convection coefficient and γ is the convective flux source term. Boundary conditions are given as:

$$
\hat{\mathrm{n}}\bullet\left(-c\nabla u - \alpha u + \gamma\right) + bu = g - h^t \mu \tag{6.20}
$$

$$
hu = r \tag{6.21}
$$

Equation (6.20) is the generalized Neumann boundary condition, b is the boundary absorption coefficient, g is the boundary source term, h is a scalar and μ is Lagrange multiplier. Equation (6.21) is the Dirichlet boundary condition.

Comparing equation (6.12) and (6.13) to equation (6.19), gives following value for the coefficients and dependent variables:

$$u = \begin{pmatrix} T \\ V \end{pmatrix},\ c = \begin{pmatrix} k + \sigma S^2 T & \sigma S T \\ \sigma S & \sigma \end{pmatrix}, and\ f = \begin{pmatrix} \sigma \left|\nabla V\right|^2 + S \nabla T \bullet \nabla V \\ 0 \end{pmatrix} \tag{6.22}$$

Remaining coefficients are zero. In cap layer there is an additional source term because of Joule heating due to electrical contact resistance, thus for cap layer the source term is given as:

$$f = \begin{pmatrix} q_c''' + \sigma \left|\nabla V\right|^2 + S \nabla T \bullet \nabla V \\ 0 \end{pmatrix} \tag{6.23}$$

6.2.1. Boundary condition

Coefficient b, g, h, and r are found by comparing Eq. (6.20) and Eq. (6.21) with Eq. (6.15) – Eq. (6.17). At the ground electrode:

$$b = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix},\ g = \begin{pmatrix} 0 \\ 0 \end{pmatrix},\ h = \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix},\ r = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \tag{6.24}$$

At the electrode contact area:

$$b = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix},\ g = \begin{pmatrix} 0 \\ J_o \end{pmatrix},\ h = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix},\ r = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \tag{6.25}$$

where, J_o is the electrical current density. At base of the substrate either convective or constant temperature boundary condition is used, which are respectively defined as:

$$b = \begin{pmatrix} h_{base} & 0 \\ 0 & 0 \end{pmatrix},\ g = \begin{pmatrix} h_{base} T_\infty \\ 0 \end{pmatrix},\ h = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix},\ r = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \tag{6.26}$$

$$b = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix},\ g = \begin{pmatrix} 0 \\ 0 \end{pmatrix},\ h = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix},\ r = \begin{pmatrix} T_\infty \\ 0 \end{pmatrix} \tag{6.27}$$

Remaining are assumed to be adiabatic and electrically isolated (have zero outward potential gradient).

$$b=\begin{pmatrix}0 & 0\\ 0 & 0\end{pmatrix},\ g=\begin{pmatrix}0\\ 0\end{pmatrix},\ h=\begin{pmatrix}0 & 0\\ 0 & 0\end{pmatrix},\ r=\begin{pmatrix}0\\ 0\end{pmatrix} \tag{6.28}$$

6.3. Results and discussion

6.3.1. Grid independence study

Grid independence test is carried out by progressively finer mesh. Numbers of elements in three cases were 250,000, 500,000 and 1,000,000, respectively. Minimum element quality for the coarse mesh, normal and fine mesh is 0.1, 0.2 and 0.3, respectively, and computational time for the three cases is 3 hours, 8 hours and 24 hours, respectively, on a Windows server with 3.2 GHz dual core processor and 12 GB of RAM. Figure 6-2 shows the maximum temperature as well as optimum operating current for the superlattice for all three cases. The solution is independent of the grid size. The difference in the maximum cooling predicted by coarsest and finest grid is less than 0.4 % whereas for the optimum current difference in less than 0.6%. The convergence time can be reduced further by making the grid even coarser; however, due to poor element quality solution does not converge. Number of elements used in the present study are 250,000.

6.3.2. Validation of computational model

Computational model is validated with experiments for accuracy. Details of the experimental test facility are provided in Chapter 3. Superlattice coolers have the same dimensions as present in the experimental test die. Table 6-1 show the properties and

dimensions of each layer modeled in the simulation. In test device, superlattice coolers have hotspot heaters on the top of them to imitate hotspot as well as measure temperature. Hotspot heaters were not included in the simulations to reduce computational time. The effect of the superlattice cooler is localized to vicinity of the cooler and since the size of the SLC is substantially smaller than the size of the heat sink, most of the heat sink is unaffected by the presence of the superlattice cooler. Therefore, only a portion of the heat sink is modeled in the simulation. The volume of the heat sink in the model is 1.5 mm x 1.3 mm x 0.5 mm compared to 15 mm x 14 mm x 0.5mm for the test device.

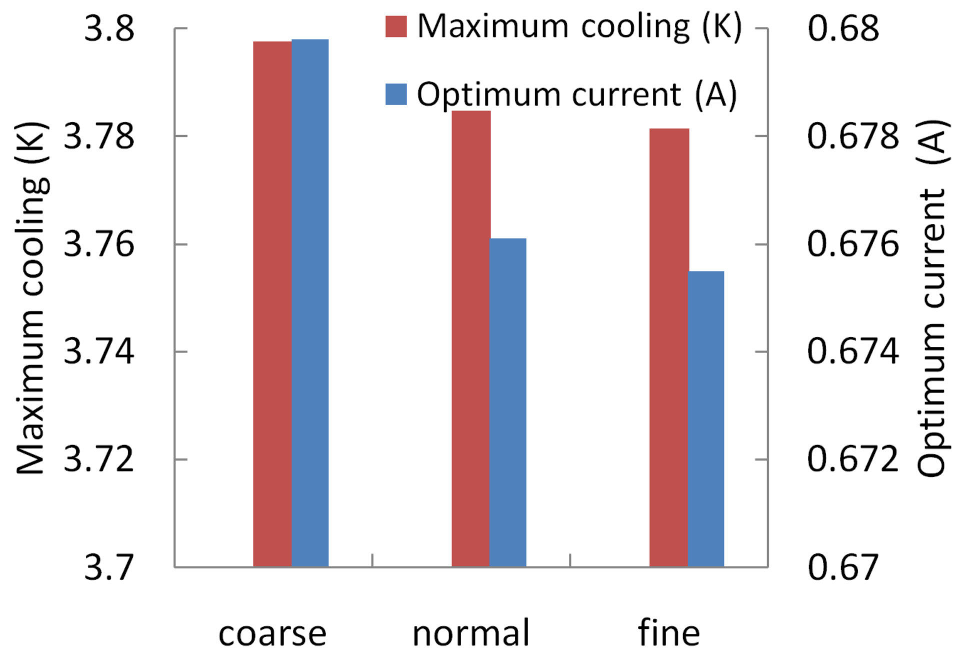


Figure 6-2: Grid independence test. Maximum temperature drop and optimum current for three mesh refinements.

Figure 6-3 compares the computational model with the experimental results for 100 μm x 100 μm SLC at ambient temperature of 300 K. The cooling at the superlattice increases with the activation current because of increase in the Peltier cooling. However,

it starts to saturate as the current increases due to rise in Joule heating resulting in an optimum current corresponding to maximum cooling. The model shows good agreement with the experiments with the maximum error in temperature drop less than 1%. The optimum current (corresponding to maximum temperature drop) predicted by model and experiments are 500 mA and 550 mA, respectively.

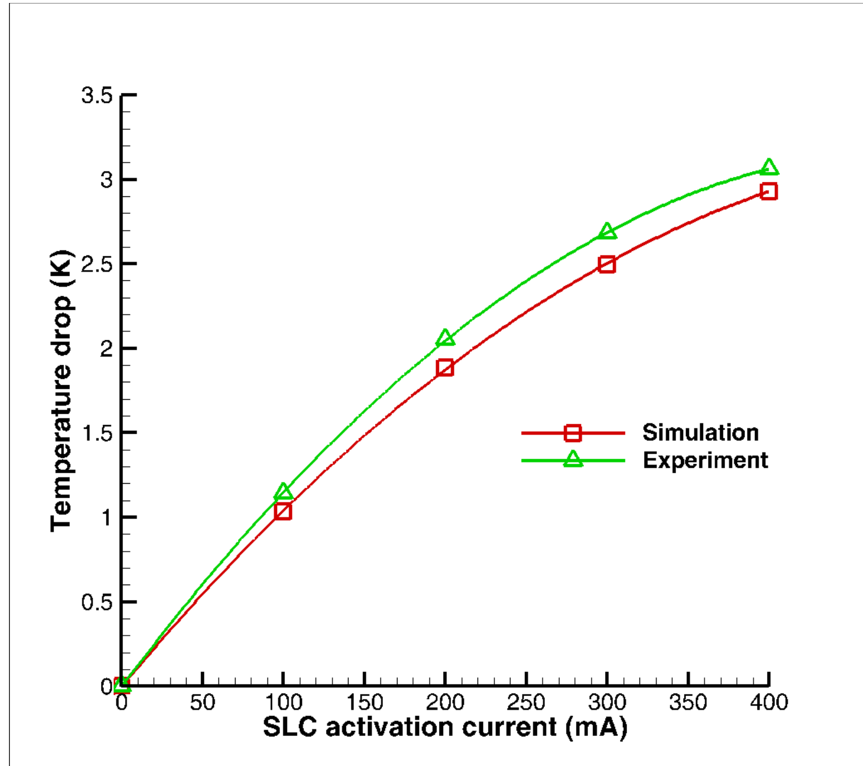
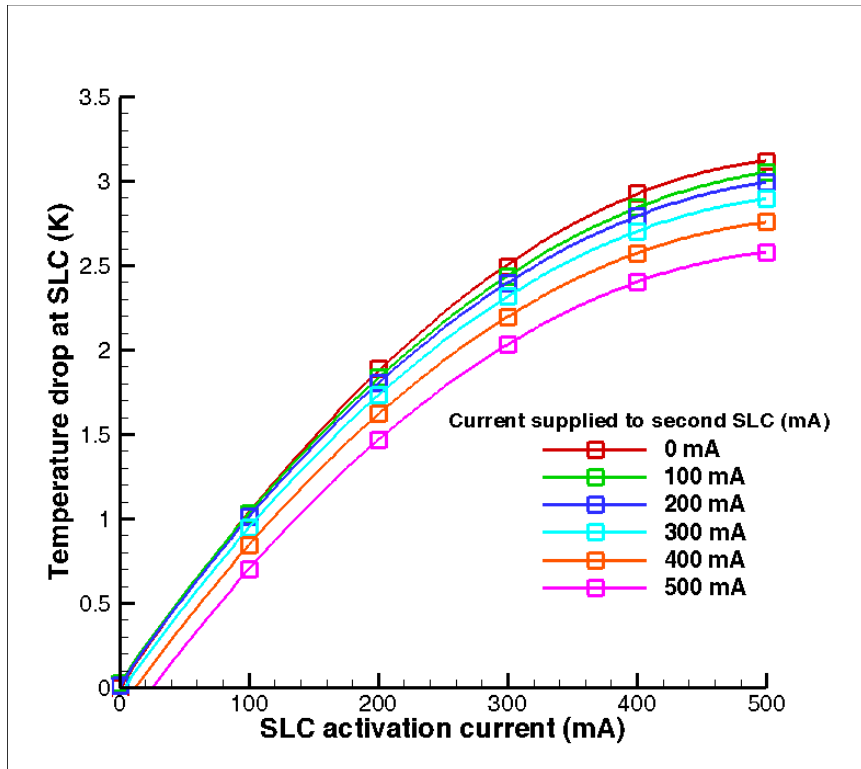


Figure 6-3: Validation of computational model with the experiments. SLC size = 100 µm x 100 µm, Δg = 400 µm, ambient temperature = 23 °C.

6.3.3. Effect of ground electrode location

As mentioned in Chapter 5, location of the ground electrode affects the performance of the superlattice cooler. The main reason for the reduction in the performance of the superlattice cooler is increased Joule heating at the superlattice-silicon interface due to electrical current spreading. Moreover, parasitic heat transfer from the ground electrode to the superlattice cooler also slightly reduces the cooling obtained at the SLC.

Figure 6-4 (a) shows the cooling obtained at one of the 100 μm x 100 μm SLC as a function of current supplied to other same size SLC, for ground electrode located 400 μm away from the SLC. Superlattice coolers are located 100 μm apart. Heat transfer coefficient at the substrate bottom is 250,000 W/m^2K. Since both superlattice coolers share the ground electrode, as current supplied to the second SLC is increased, Peltier heating at the ground electrode is increased, which increases the parasitic heat transfer from the ground electrode to the SLC. Moreover, Joule heating within the silicon substrate also increases. Since Joule heating is proportional to the square of the current whereas, Peltier heating is directly proportional to the current, activating the second superlattice cooler results in significant rise in the heat generation due to Joule heating. This increases the parasitic heat transfer to the superlattice cooler and thus reduces its performance. Figure 6-4(b) shows the effect of ground electrode location on the maximum temperature drop at the SLC as a function of the current supplied to the other SLC. The maximum temperature drop is defined as the temperature drop corresponding to the optimum operating current. Consider the operation of a single SLC in isolation (corresponding to zero current in Figure 6-4(b)). As the ground electrode is moved closer to the superlattice cooler Joule heating due to electrical current spreading at the superlattice-silicon interface increases. This results in more parasitic heat transfer to the SLC. Hence the maximum temperature drop achieved at the superlattice cooler decreases. Now, if one keeps the ground location fixed, while activating the second superlattice cooler, total heat generated within the silicon substrate as well as Peltier heating at the ground electrode increases due to increase in the current density. This further increases



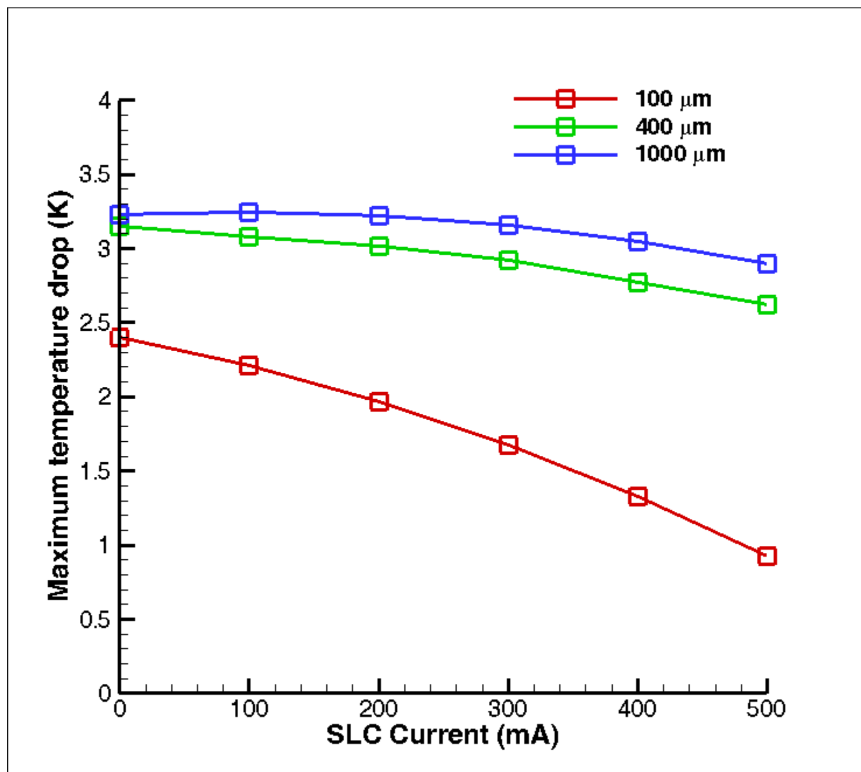


Figure 6-4: (a) Cooling obtained at one of the 100 µm x 100 µm SLC as a function of current supplied to other SLC. Ground electrode is located 400 µm far from SLCs. (b) Maximum temperature drop as a function of SLC activation current for three different ground electrodes. SLC size = 100 µm x 100 µm, Δs = 100 µm, ambient temperature = 23 °C.

the parasitic heat transfer to the superlattice cooler, resulting in additional drop in the superlattice cooler performance. The reduction in temperature drop of the superlattice cooler due to activation of another superlattice cooler is defined as the thermal coupling between the coolers. Decreasing the distance between the ground electrode and superlattice from 1000 µm to 400 µm has only moderate affect on the performance of the SLC. However, further reduction to 100 µm drastically affects the performance of the SLC. As mentioned in Chapter 5, ground electrode affects the performance of superlattice cooler when separation distance between the ground electrode and superlattice cooler is less than few characteristic diameters of the superlattice cooler (which will be equivalent to 300 µm to 400 µm in this case). If separation distance is more than 400 µm, parasitic heat transfer from ground to superlattice cooler is negligible. Moreover, Joule heating due to electrical current spreading does not change significantly if the ground electrode is located more than 400 µm from the superlattice cooler. This is the reason for such a drastic reduction in the performance of the superlattice cooler when separation distance between the ground electrode and superlattice cooler is reduced from 400 µm to 100 µm. When the ground electrode is 100 µm away from the SLC, cooling at the SLC decreases by more than 60% when second SLC is subjected to 500 mA activation current; whereas under the same operating conditions if the ground electrode is placed 1000 µm away from the SLC, cooling decreases by only 10%. Therefore, to minimize the thermal coupling between SLCs, minimum separation distance between the ground electrode and superlattice cooler should be at least a few characteristic diameters of the superlattice cooler.

6.3.4. Effect of convective thermal resistance of microchannel heat sink

Current state of the art superlattice coolers have low ZT (~0.1) and maximum COP in the range of 0.3-0.5 [99], which means for every 1 W heat removed at superlattice cooler, 2-3 W heat will be generated. Since the superlattice cooler and ground electrode temperatures are almost the same, Peltier heating at the ground electrode is almost equal to the Peltier cooling at the superlattice cooler. The main reason for low the COP is the heat generation within the silicon substrate, which is more compared to the Peltier heating at the ground electrode. The Joule heating within the silicon substrate is eventually removed by the microchannel heat sink. However, if the microchannel heat sink cannot effectively remove this heat, it will reduce the cooling obtained at the superlattice cooler.

Figure 6-5 shows the effect of convective heat transfer coefficient on the cooling obtained at the SLC. The ground electrode location is fixed at 400 μm away from superlattice. Three different heat transfer coefficient are considered: 50,000 W/m^2K, 250,000 W/m^2K, and infinity (constant wall temperature boundary condition). Convective heat transfer coefficient is adjusted to account for the presence of microchannel heat sink using Eq. (6.14). The microchannel heat sink used in the experimental prototype has dimensions of 330 μm x 65 μm with wall width of 35 μm [100]. Convective heat transfer coefficient inside the microchannel heat sink, with water as a working fluid, is around 30,000 W/m^2K. This value of heat transfer coefficient when adjusted for the absence of microchannel heat sink using Eq. (6.14) translates to a value of 250,000 W/m^2K. Heat transfer coefficient of 50,000 W/m^2K corresponds to a poor thermal fluid such as a dielectric fluid. Constant wall temperature boundary condition is

nearly impossible to achieve inside the microchannel heat sink and represents an idealized case.

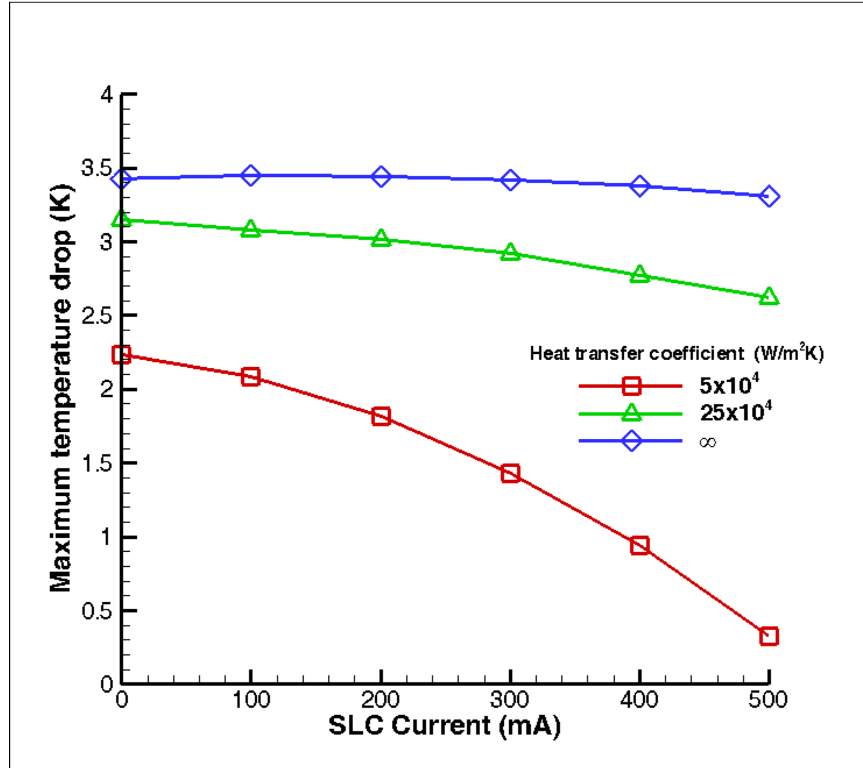


Figure 6-5: Maximum temperature drop as a function of SLC activation current for different convective heat transfer coefficients. SLC size = 100 µm x 100 µm, Δs = 100 µm, Δg = 400 µm, ambient temperature = 23 °C.

For a fixed heat transfer coefficient, as the current supplied to the other superlattice is increased the performance of SLC decreases due to increased Joule heating within the silicon substrate as well as increased heat dissipation at the ground electrode. As the heat transfer coefficient is decreased, the heat sink becomes ineffective in dissipating the heat generated within the silicon substrate, superlattice and buffer layer. This reduces the cooling at the superlattice cooler. Performance of the superlattice cooler is drastically affected by the convective thermal resistance of the microchannel heat sink, when the activation current to the second superlattice cooler is increased. Decreasing the

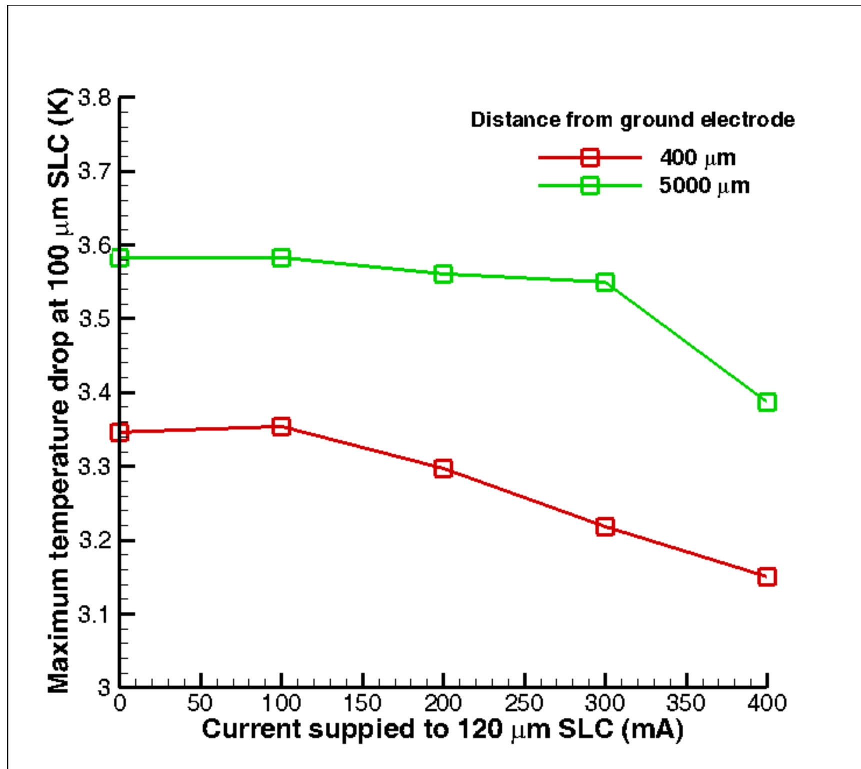
heat transfer coefficient from 250,000 W/m^2K to 50,000 W/m^2K (changing the working fluid from water to FC72), reduces the cooling by 87% corresponding to the activation current of 500 mA. However in ideal scenario, when convective thermal resistance of the microchannel heat sink is assumed to be zero, performance of the SLC decreases by only 4% due to thermal coupling. This suggests that thermal coupling is a strong function of the heat transfer coefficient.

6.4. Experimental investigation

According to computational model, thermal coupling between superlattice coolers diminishes the cooling obtained at individual coolers. Thermal coupling between superlattice coolers is a strong function of ground electrode location, as well as convective heat transfer coefficient but a weak function of spacing between coolers. Thermal coupling between superlattice coolers is experimentally investigated. Moreover, the effect of ground electrode location and convective thermal resistance of microchannel heat sink on the thermal coupling between SLCs is also examined.

6.4.1. Effect of ground electrode location

To study the effect of ground electrode location two different ground electrodes are used; one located 400 µm from the cooler and other placed about 5000 µm far. Thermal coupling is studied between two superlattice coolers (100 µm x 100 µm and 120 µm x 120 µm) located 220 µm apart as shown in Figure 2-8. De-ionized water is used as the working fluid. Figure 6-6(a) shows the maximum temperature drop obtained at 100 µm x 100 µm SLC as a function of current supplied to 120 µm x 120 µm SLC for two different ground electrode locations. Figure 6-6(b) shows the maximum temperature drop obtained at 120 µm x 120 µm SLC, as a function of the current supplied to 100 µm x 100 µm. As



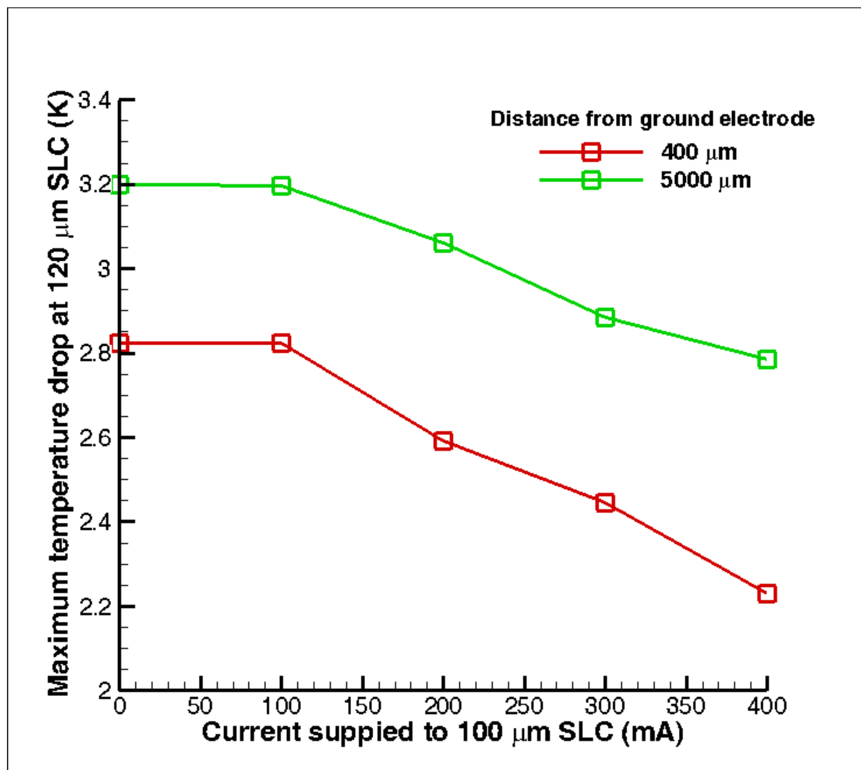


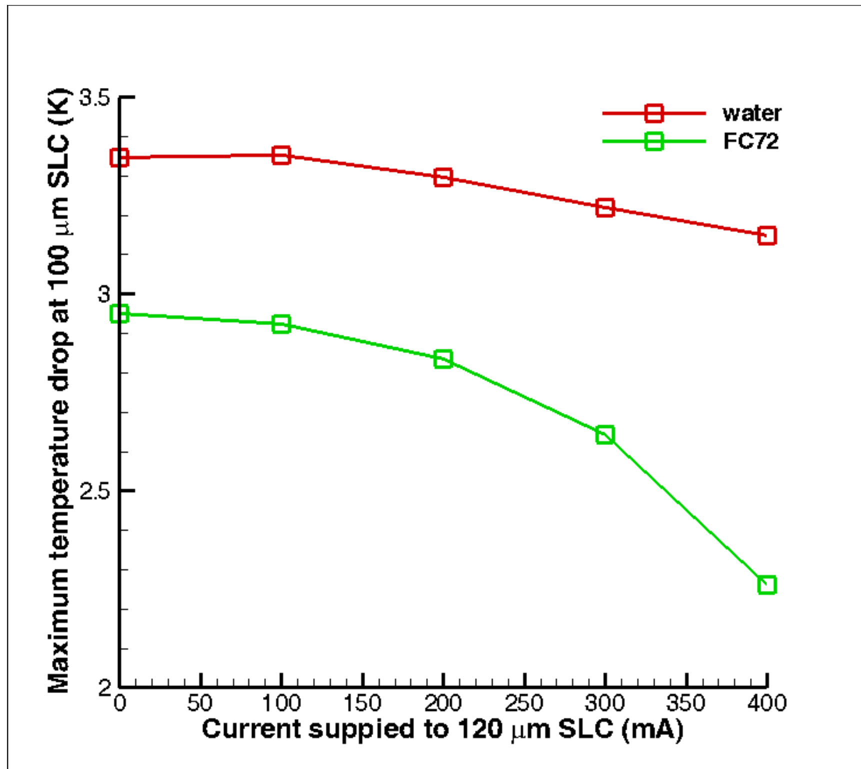
Figure 6-6: (a) Maximum temperature drop at 100 µm SLC as a function of current supplied to 120 µm SLC and (b) Maximum temperature drop at 120 µm SLC as a function of current supplied to 100 µm SLC for two ground electrode locations.

predicted by the model, cooling at either SLC decreases when other SLC is turned on and this effect is more dominant when the ground electrode is located close to the SLCs. The performance of 120 µm x 120 µm SLC is more affected by the thermal coupling with 100 µm x 100 µm SLC. This is due to lower thermal spreading resistance of the 120 µm x 120 µm SLC. Thermal spreading resistance is inversely proportional to the square root of area [101]. Therefore, 120 µm x 120 µm superlattice cooler will have lower thermal spreading resistance compared to 100 µm x 100 µm SLC, resulting in more parasitic heat transfer to the superlattice cooler as compared to 100 µm x 100 µm SLC. Hence, the performance of 120 µm x 120 µm cooler is more affected by the thermal coupling with the 100 µm x 100 µm SLC.

6.4.2. Effect of convective thermal resistance

We have also investigated the effect of convective thermal resistance of the microchannel heat sink on the thermal coupling between superlattice coolers. Two different working fluids, water and FC72, are used. Water is an excellent thermal fluid; however, microelectronics industry has been apprehensive of using water for direct cooling of die mainly because of low freezing point, and fear of electrical shortage in the case of leakage. Dielectric fluids are better suited for electronics cooling, as they are safer to use even though they have poor thermal properties compared to water.

Figure 6-7(a) and Figure 6-7(b) shows the thermal coupling between 100 µm x 100 µm and 120 µm x 120 µm SLC for both working fluids. Ground electrode is located 400 µm away from the superlattice. FC-72 has an order of magnitude lower thermal conductivity than water. Therefore, thermal resistance of microchannel heat sink is an order of magnitude higher for FC72. Average heat transfer coefficient for water and



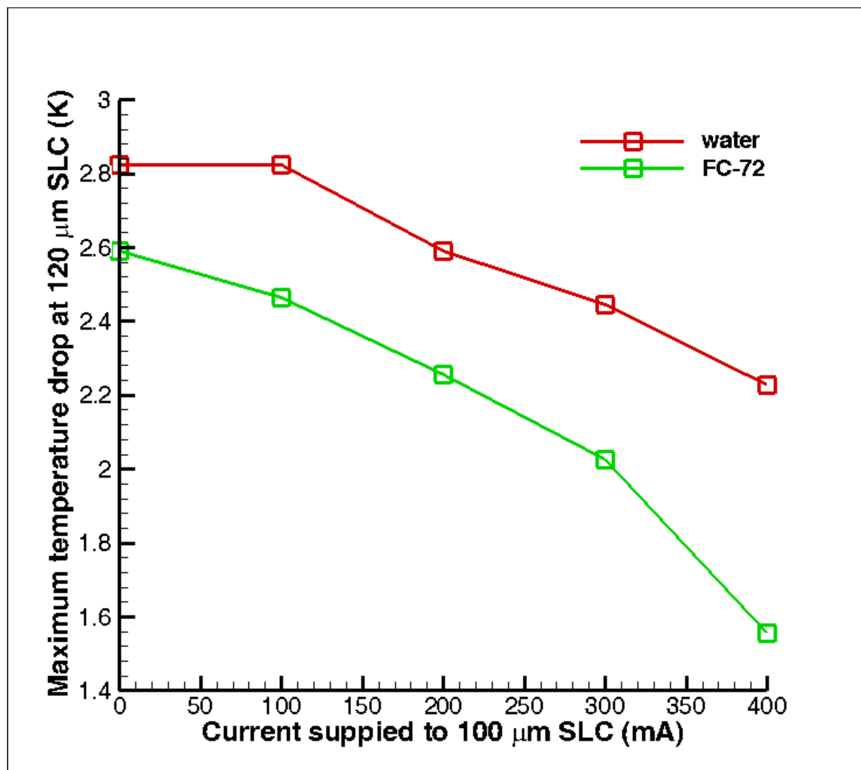


Figure 6-7: (a) Maximum temperature drop at 100 µm SLC as a function of current supplied to 120 µm SLC and (b) Maximum temperature drop at 120 µm SLC as a function of current supplied to 100 µm SLC for two working fluids.

FC72 is 30,000 W/m^{2}K and 2,800 W/m^{2}K respectively. Both superlattice coolers perform poorly when FC72 is used as the working fluid because FC72 is not able to effectively remove the heat generated due to Joule heating within the superlattice, buffer layer as well as silicon substrate. As observed in the simulations, the thermal coupling between superlattice coolers is much more pronounced for lower heat transfer coefficient (FC72) inside the microchannel heat sink. The maximum temperature drop at both SLCs reduces by approximately 30% at 500 mA activation current.

6.5. Summary

In this chapter computational and experimental investigation of the thermal coupling between superlattice coolers and its dependence on the geometric (location of ground electrode) and operating parameters (working fluid) is examined and discussed. Thermal coupling between superlattice coolers is found to be a strong function of the ground electrode location and convective thermal resistance of microchannel heat sink. Placing the ground electrode closer to the superlattice degrades the performance of the cooling due to higher parasitic heat transfer to the coolers. Using a poor thermal fluid (equivalently decreasing the convective heat transfer coefficient at the substrate bottom) also diminishes the cooling at superlattice. Thermal coupling between superlattice coolers becomes quite significant at lower heat transfer coefficient decreasing the cooling by more than 80%. Experimental results show the same trends as observed in the simulations.

CHAPTER 7: TRANSIENT CHARACTERIZATION OF HYBRID COOLING SCHEME

Microprocessor power dissipation map varies during operation depending upon the type of the workload, distribution of the work load, etc. This problem has become more severe due to advent of multi-core and many core processors which allow transferring of the workload from one core to another. Thus hotspot locations vary in space and time. The dynamically changing power map requires an active cooling solution with a feedback mechanism that would allow the cooling solution to evolve with the microprocessor power map.

Several techniques have been developed for dynamic thermal management (DTM) of microprocessor. In DTM, temperature is continuously monitored using the on chip temperature sensors and if the temperature exceeds the threshold, a cooling mechanism is executed. This local cooling mechanism is usually different from the global cooling mechanism and is only utilized in case of extreme temperatures. Almost all the DTM techniques require modification in the microprocessor which either reduces the power to the core or migrate the activity from one core to another core. Some of the most common techniques are dynamic voltage or frequency scaling [102], clock gating [103, 104], fetch gating [105], core hoping [106], thermal spare cores [107], thermal aware scheduling [108] etc. However, all these cooling techniques compromise the performance of the microprocessor in some way or other. Dynamic voltage or frequency scaling degrades the performance of the microprocessor, core hoping, thread migration and spare cores require additional cores to migrate the activity. These additional cores use real estate on the die, thus increase its size and cost.

Since hybrid cooling scheme does not require any modification in the electronics, there is no performance penalty in implementing the scheme. Localized SLCs can be placed in the region of high activity and can be triggered if local temperature exceeds the threshold. Thus, temperature can be decreased locally without compromising the performance of the electronic component. An ideal dynamic cooling solution will evolve with the power map instantaneously, however, due to finite thermal mass any cooling scheme will have some time lag. Therefore, understanding of the transient behavior is critical for dynamic thermal management of electronics.

7.1. Experimental characterization of transient behavior

Transient characterization of the hybrid scheme has been carried out using the transient detector of the infrared microscope. The transient detector is capable of acquiring the temperature signal at 300,000 readings per second. Details on the experimental set up and procedure is provided in Chapter 3.

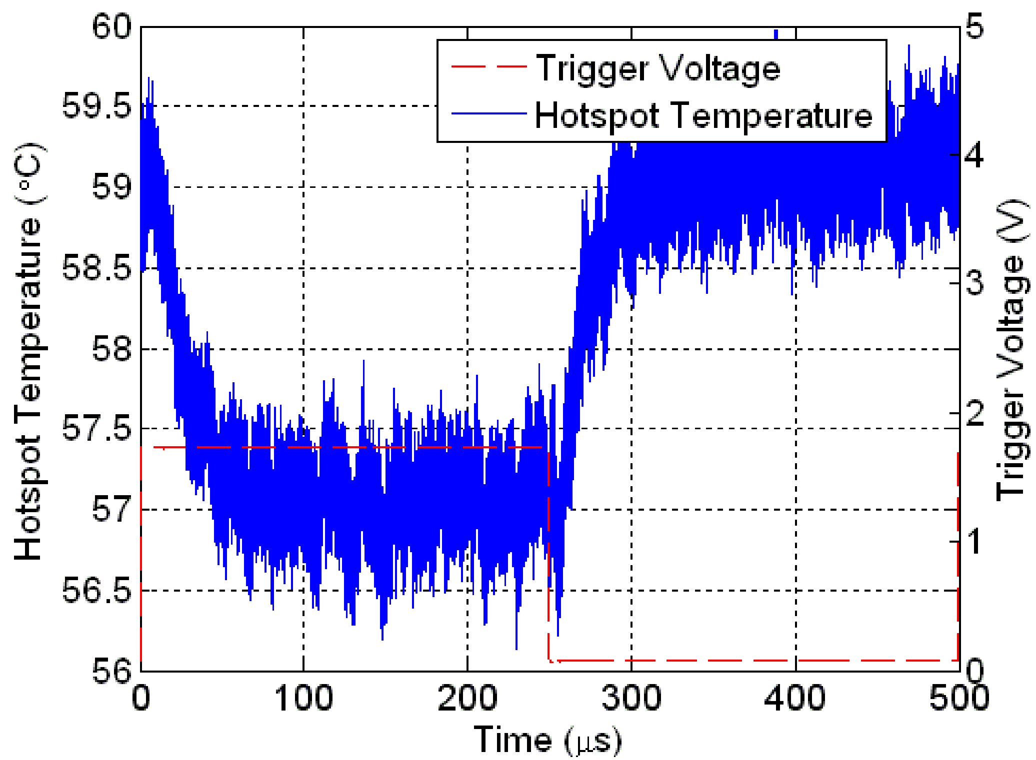
7.1.1. Transient response of the superlattice cooler

As mentioned in Chapter 3, the samples are coated with graphite to get more accurate temperature. Figure 7-1 shows the response curve of the superlattice cooler without graphite coating and with graphite coating respectively. The superlattice cooler, as well as infrared microscope is triggered with the same square pulse. The frequency of trigger pulse is 2 kHz with duty cycle of 50%. Superlattice cooler is on when trigger voltage is non-zero and off when trigger voltage is zero. This means superlattice cooler is active for 250 μs and inactive for the next 250 μs. IR microscope measures the temperature of the surface (opaque in IR wavelength). Since hotspot heater is fabricated at the top of the superlattice cooler, the microscope measures the temperature of the

heater, not the superlattice cooler. However, since the hotspot heater is less than a 1 μm thick, it will not significantly increase response time of the superlattice cooler.

Since emissivity of metals is quite low, presence of a metal layer (hotspot heater) on top of superlattice cooler reduces the number of photons received by the detector, which reduces signal to noise ratio. A thin layer of graphite coating on top of the superlattice cooler, increases the emissivity of the sample and improves signal to noise ratio. But the presence of graphite layer also increases the thermal mass and thus the time constant (defined as the time needed to decrease the temperature to 63% of the steady state value) of the superlattice cooler. Thickness of the graphite layer is estimated to be around 10 μm and the time constant of the superlattice cooler without graphite coating is measured to be around 25 μs. In the presence of graphite coating, time constant of the superlattice cooler increases to 35 μs. However, in the absence of graphite coating signal to noise ratio is low, which leads to higher fluctuations in the temperature measurement. The fluctuation in temperature when sample is not coated with graphite is $\pm 0.5\ ^{o}C$, whereas it reduces to $\pm 0.1\ ^{o}C$ when the sample is coated with graphite. Since temperature fluctuation decreases significantly when samples are coated with graphite, during experiments all samples are coated with a thin layer of graphite.

For both samples (with and without graphite coating), as soon as the superlattice cooler is activated, temperature at the hotspot starts to drop and reaches a steady state. When samples are not coated with graphite, steady state is achieved in roughly 100 μs. However, when samples are coated with graphite, it takes almost twice the time to reach steady state. Superlattice cooler is deactivated at 250 μs. As soon as the superlattice



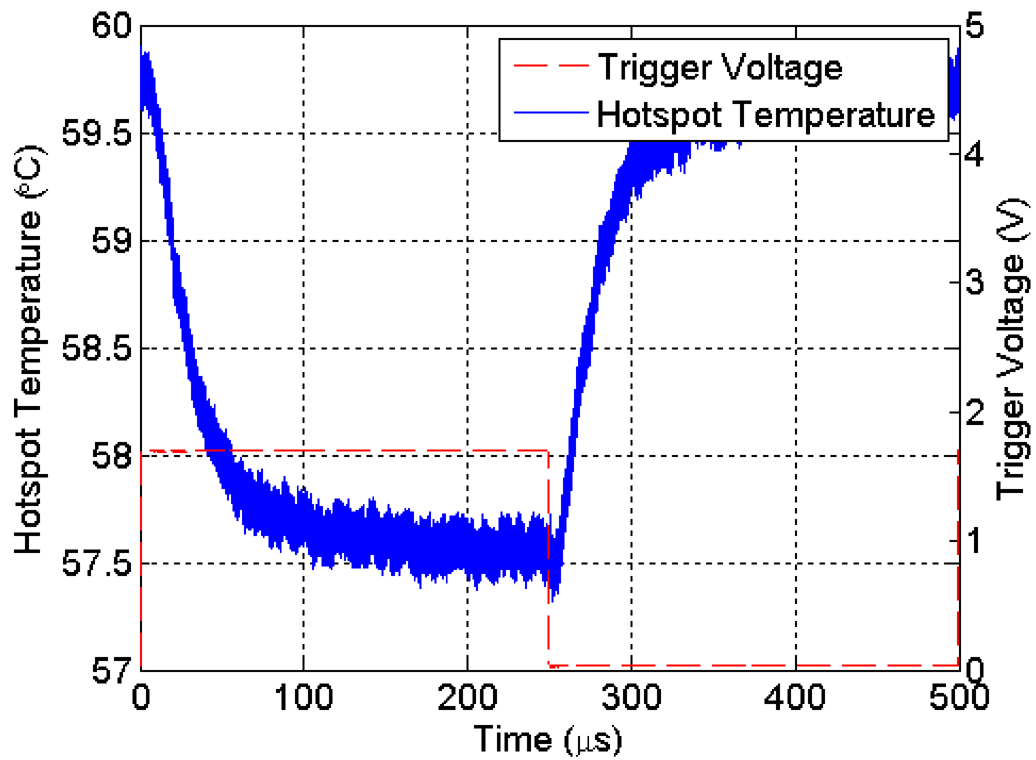


Figure 7-1: Response curve of the superlattice cooler without coating (top), with graphite coating (bottom). Red curve shows the square trigger pulse sent to superlattice cooler as well as the camera.

cooler is deactivated, the temperature increases exponentially and again achieves steady state in roughly the same time.

7.1.2. Effect of operating current on the transient behavior of superlattice cooler

Figure 7-2 shows the response of a 100 µm x 100 µm superlattice cooler under various operating current. Non-dimensional temperature is defined as

$$\phi = \frac{T - T_s}{T_{in} - T_s} \tag{7.1}$$

where, ϕ is the non-dimensional temperature, T is the instantaneous temperature, T_{in} is the initial temperature, and T_s is the steady state temperature. As expected, the time constant for all three activation current is the same. Since the charge migration and charge transport time scale is two orders of magnitude smaller than the thermal time scale (Figure 7-5), response of the superlattice cooler is decided by the thermal time scale, which is independent of the activation current. Therefore, increasing the activation current does not affect the transient response of the superlattice, even though the absolute cooling obtained at the superlattice is a function of the activation current.

7.1.3. Effect of superlattice size on the transient behavior of superlattice cooler

Figure 7-3 shows the response of three different superlattice coolers at 100 mA activation current. As evident from the graph, transient behavior of the superlattice cooler is also independent of the superlattice size. For all three superlattice size, the time constant of the cooler is 35 µs. Even though the thermal mass of the superlattice cooler increases with its size (due to larger area), thickness of all three superlattice coolers are the same. Therefore, the thermal mass per unit area is same for all three superlattice

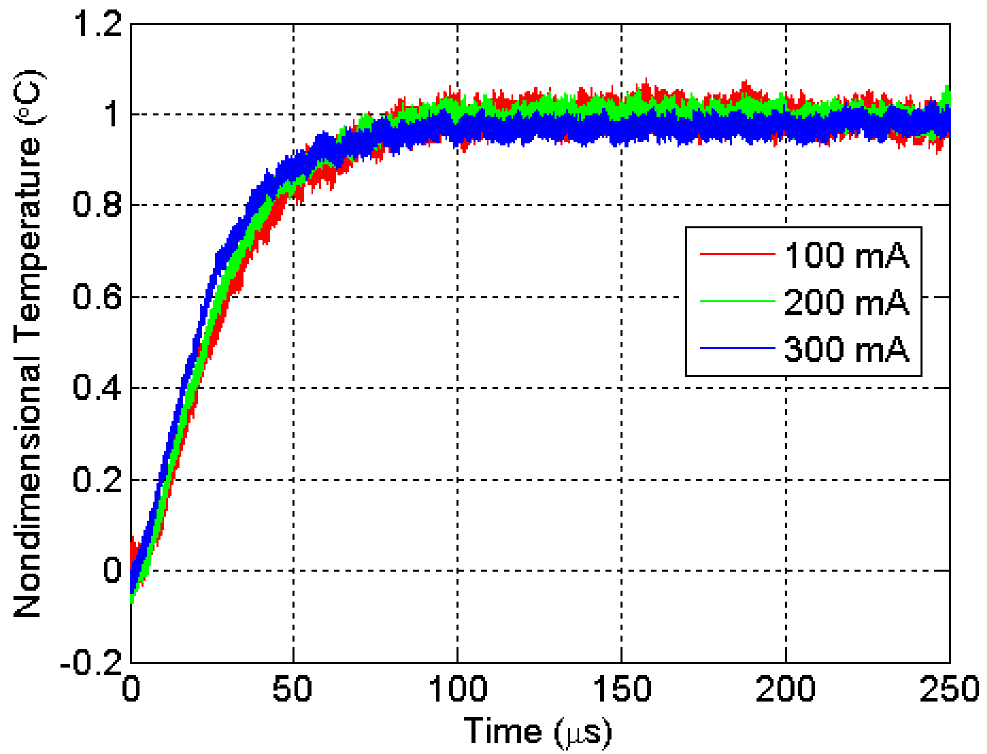


Figure 7-2: Transient response time of the SLC for different SLC activation current.

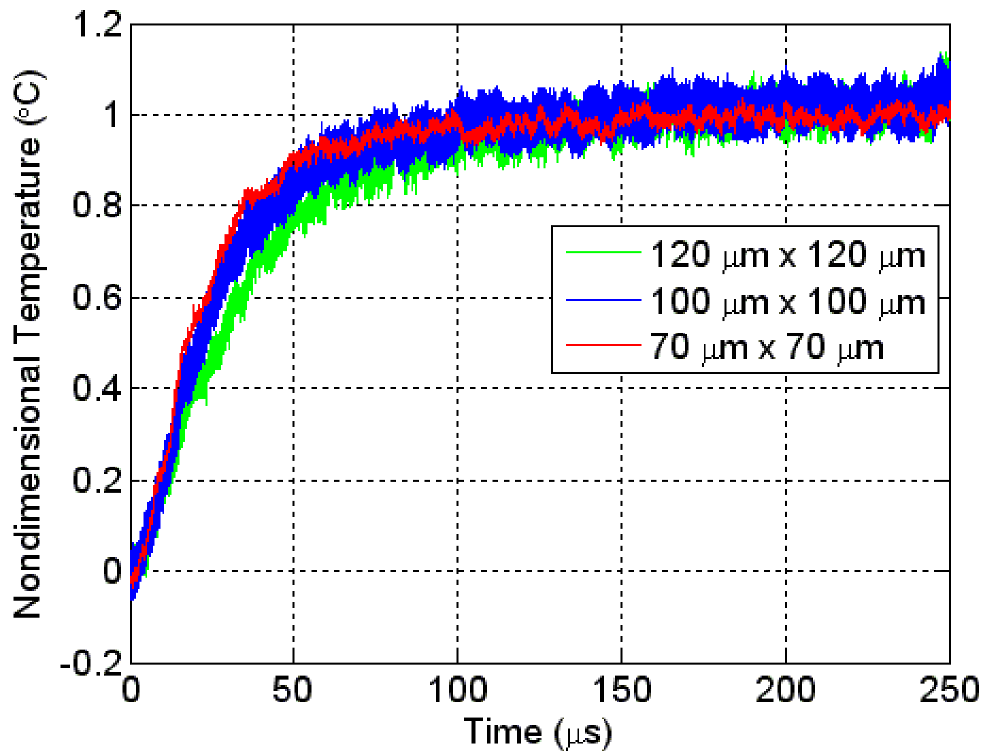


Figure 7-3: Transient response of the SLC for different SLC sizes.

coolers. Since the infrared microscope measures the area average surface temperature, transient response of the superlattice cooler is not affected by its size.

7.1.4. Effect of activation delay between hotspot and superlattice cooler

The superlattice cooler is activated once the hotspot is detected. In a real scenario, there will always be some delay associated with the superlattice activation due to inherent time lag associated with the feedback circuit used for the superlattice cooler activation. Figure 7-4 shows the effect of the delay in the SLC activation. The hotspot heater is 100 μm x 100 μm in dimension and the heat flux dissipated at the hotspot is 150 W/cm^2. Non-dimensional temperature in Figure 7-4 is defined as:

$$\phi^* = \frac{T - T_{s,h}}{T_{in} - T_{s,h}} \tag{7.2}$$

where, ϕ^* is the non-dimensional temperature, T is the instantaneous temperature, T_{in} is the initial temperature (when both hotspot and superlattice are powered off), and $T_{s,h}$ is the steady state temperature with only hotspot heater powered on.

The hotspot is activated at time t=0 μs. The superlattice cooler is activated after a certain delay. The activation current to the superlattice cooler is kept constant at 150 mA. As the delay time is increased, temperature at the hotspot initially rises and then decreases upon SLC activation. When both hotspot heater and superlattice cooler are activated simultaneously (delay time = 0 μs), temperature at the hotspot drops immediately due to cooling provided by the superlattice cooler. However, as the delay is increased temperature at the hotspot increases exponentially till the superlattice cooler is activated. As soon as the superlattice cooler is activated temperature again drops exponentially till the system reaches steady state. For the delay of 0 μs to 100 μs, the

temperature jump at the hotspot increases from 0 to 3 K. After 100 μs hotspot reaches steady state and no further temperature rise occurs. This suggests that to reduce the temperature variation at the hotspot, activation delay between the superlattice cooler and hotspot should be minimized.

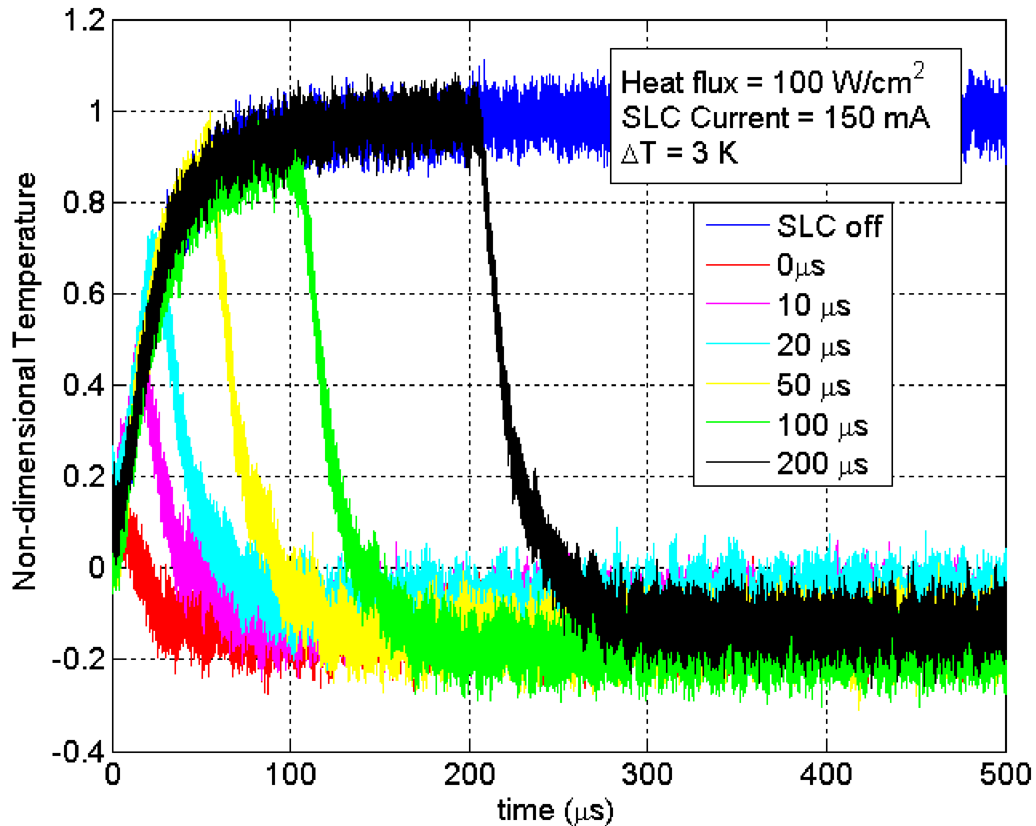


Figure 7-4: Effect of activation delay between SLC and hotspot.

7.2. Computational model

Experiments have shown superlattice coolers provide extremely fast transient response. Computational model is developed to study the transient response of the superlattice cooler, how it is affected by the operating condition (convective heat transfer coefficient inside the microchannel heat sink) and geometric parameters (ground electrode location).

An electro-thermal model is used to study the transient behavior of the hybrid cooling scheme. The steady-state model has already been described in detail for steady state in the Chapter 6. The transient term in the governing equations were originally drop; however since we are interested in transient response of the superlattice curve, time dependent terms have to be included. Eq (7.3) and (7.4) show the non-linear coupled temperature and electrical potential equation with the inclusion of time dependent terms:

$$\rho c_p \frac{\partial T}{\partial t} + \nabla \bullet \left\{ -\left(k + \sigma S^2 T\right)\nabla T - \sigma S T \nabla V \right\} = \sigma S \nabla T \bullet \nabla V + \sigma \left|\nabla V\right|^2 \quad (7.3)$$

$$\nabla \bullet \left\{ \varepsilon \frac{\partial\left(\nabla V\right)}{\partial t} + \sigma S \nabla T + \sigma \nabla V \right\} = 0 \quad (7.4)$$

The time dependent term in the electric field equation (7.4) can be neglected as the time scale associated with the charge transport is significantly smaller than the diffusive time scale. There are two time scales associated with charge transport; charge migration time scale and charge relaxation time scale, which are respectively described as:

$$t_{cm} = \frac{l_e^2}{\mu V} \quad (7.5)$$

$$t_{cr} = \frac{\varepsilon}{\sigma} \quad (7.6)$$

where, t_{cm} and t_{cr} are the time scale associated with the charge migration and charge relaxation, respectively, l_e is the characteristic length scale, and μ is charge mobility. The diffusion time scale associated with thermal transport is described as:

$$t_d = \frac{l_t^2}{\alpha} \quad (7.7)$$

where, l_t is the characteristic length scale for thermal transport and α is the thermal diffusivity. For temperature greater than 100 K, thermal conductivity is independent of doping concentration [89]. Specific heat and density can also be assumed to be independent of the doping concentration at room temperature. Thus the diffusive time scale is independent of the doping concentration. Figure 7-5 compares all three time scale for various doping concentration. Typical silicon is doped to concentration of around 10^{19} cm^{-3}, at which both charge transport time scales are more than two orders of magnitude lower than the thermal time scale. Therefore, the transient term in Equation (7.4) can be safely neglected.

$$\rho c \frac{\partial T}{\partial t} + \nabla \bullet \left\{ -\left(k + \sigma S^2 T \right) \nabla T - \sigma S T \nabla V \right\} = \sigma S \nabla T \bullet \nabla V + \sigma \left| \nabla V \right|^2 \quad (7.8)$$

$$\nabla \bullet \left\{ \sigma S \nabla T + \sigma \nabla V \right\} = 0 \quad (7.9)$$

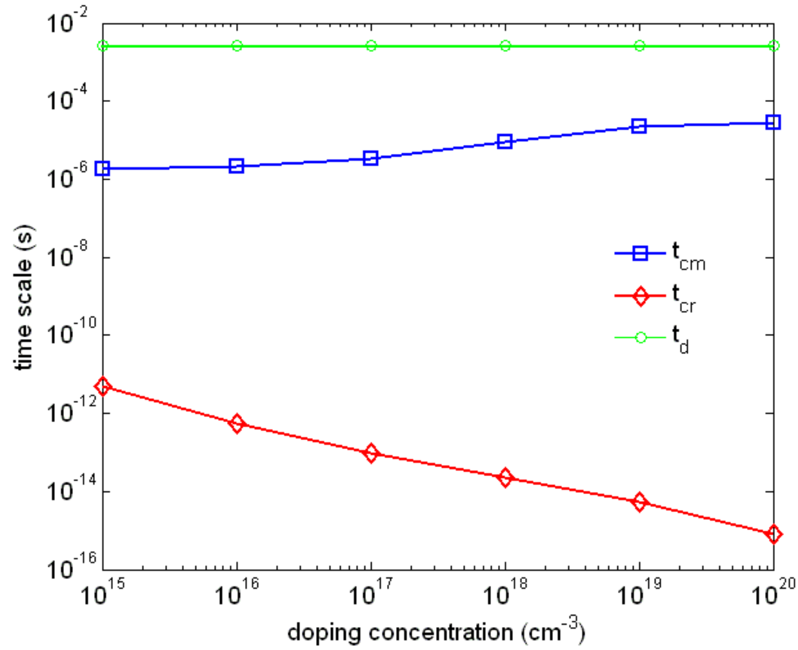


Figure 7-5: Comparison of charge migration, charge transport and diffusive time scale.

7.2.1. Boundary and initial conditions

Same boundary conditions as described in chapter 6 are used. Convective heat transfer is assumed at the base of the substrate to simulate the microchannel heat sink. Rests of the walls are adiabatic.

$$q = \begin{cases} h_b (T - T_\infty) & \text{substrate bottom} \\ 0 & \text{other walls} \end{cases} \tag{7.10}$$

Ground electrode is kept at zero potential and constant current source is input at the top metal electrode. All other walls are assumed to be electrically insulated.

$$V = 0 \tag{7.11}$$

$$\hat{\text{n}} \bullet \text{J} = \begin{cases} \text{constant} & \text{electrode contact} \\ 0 & \text{other walls} \end{cases} \tag{7.12}$$

At the interface between different layers temperature and electrical potential are assumed to be same, as well as heat flux and current are assumed to be continuous.

$$\begin{aligned} -k_1 \frac{\partial T}{\partial n}\bigg|_1 &= -k_2 \frac{\partial T}{\partial n}\bigg|_2 + (\hat{\text{n}} \bullet \text{J})(S_1 - S_2) T_{\text{int}} \\ T_1 &= T_2 \\ (\hat{\text{n}} \bullet \text{J})_1 &= (\hat{\text{n}} \bullet \text{J})_2 \\ V_1 &= V_2 \end{aligned} \tag{7.13}$$

Everywhere in the domain, initial temperature is set to 300 K and initial electrical potential is set to 0 V.

$$\begin{aligned} T_{in} &= 300 \text{ K} \\ V_{in} &= 0 \text{ V} \end{aligned} \tag{7.14}$$

7.3. COMSOL implementation

COMSOL PDE mode in the coefficient form is used to solve the coupled temperature and electrical potential equation (Eq. (7.8) and Eq. (7.9)). COMSOL PDE coefficient form is given as:

$$d_a \frac{\partial u}{\partial t} + \nabla \bullet (-c\nabla u - au + \gamma) + \beta \bullet \nabla u + au = f \tag{7.15}$$

where, the first term represents the transient term, second term represents the diffusion term, third term represents the convective term and fourth term is the absorption term. Right hand side represents the source term. u is the dependent variable, d_a is the damping coefficient, c is the diffusion coefficient, a is the absorption coefficient, α is the conservative flux convection coefficient, β is the convection coefficient and γ is the convective flux source term. Boundary condition formulation has already been described in Chapter 7.

Comparing equation Eq. (7.8) and Eq. (7.9) to equation(6.19), gives following value for the coefficients:

$$u = \begin{pmatrix} T \\ V \end{pmatrix},\ d_a = \begin{pmatrix} \rho c_p \\ 0 \end{pmatrix},\ c = \begin{pmatrix} k + \sigma S^2 T & \sigma S T \\ \sigma S & \sigma \end{pmatrix}, and\ f = \begin{pmatrix} \sigma |\nabla V|^2 + S\nabla T \bullet \nabla V \\ 0 \end{pmatrix} \tag{7.16}$$

Rests of the coefficients are zero. In cap layer there is additional source term because of Joule heating due to electrical contact resistance, thus for cap layer the source term is given as:

$$f = \begin{pmatrix} q_c''' + \sigma |\nabla V|^2 + S\nabla T \bullet \nabla V \\ 0 \end{pmatrix} \tag{7.17}$$

Boundary conditions are formulated in the same fashion as described in Chapter 6.

7.4. Results and discussion

7.4.1. Model validation

Transient computational model has been verified with the experiments to assess its accuracy. Figure 7-6 shows the simulation geometry. It contains a 100 µm x 100 µm superlattice cooler on a 500 µm thick substrate. Ground electrode is located 700 µm away from the superlattice coolers. Properties of the various layers used in the transient simulation are listed in Table 7-1. Figure 7-7 compares the transient response of 100 µm x 100 µm SLC obtained using the computational model and experiment. Experiments show slightly longer response time of the superlattice cooler (~ 30 µs) as compared to the computational model (~ 25 µs). The reason for the slight discrepancy can be attributed to the presence of the graphite layer on the top of the superlattice cooler in the experiments, which adds additional thermal mass and increases the measured response time.

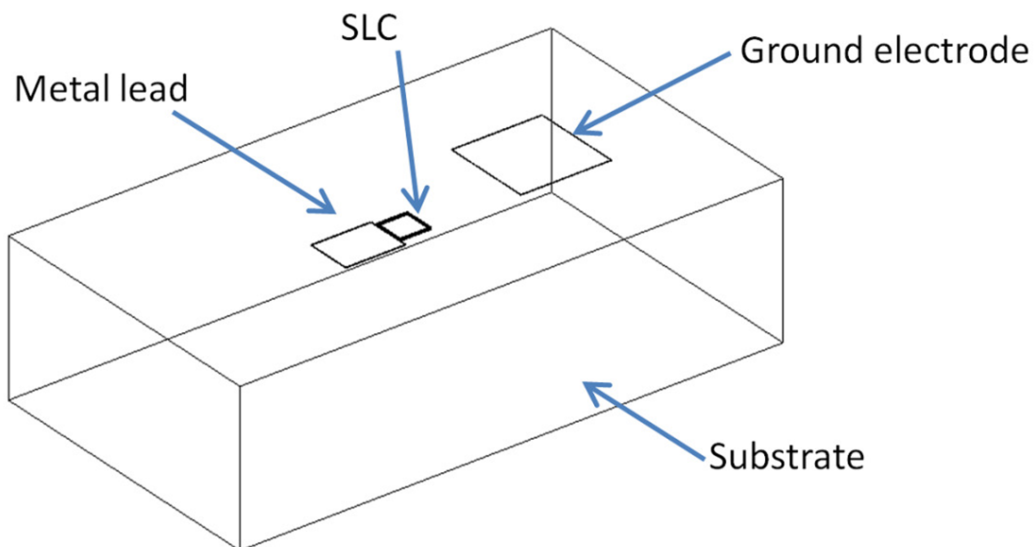


Figure 7-6: Schematic of the simulation geometry.

Table 7-1: Properties of various layers used in the computational model.

Layer name	Density (ρ, Kg/m^3)	Specific heat (C_p, J/kgK)	Thermal conductivity (k, W/mK)	Electrical conductivity (σ, Ω^{-1}m^{-1})	Seebeck coefficient (S, μV/K)
Top metal	8336	516	150	10^7	8
Cap	2673	614	6	2.884×10^5	235
Superlattice	2663	632	6	3.65×10^4	235
Buffer	2673	614	6	7.21×10^4	235
Metal lead	8336	516	150	10^7	8
Insulation	3440	170	1	10^{-9}	-
Substrate	2330	705	150	5×10^4	540

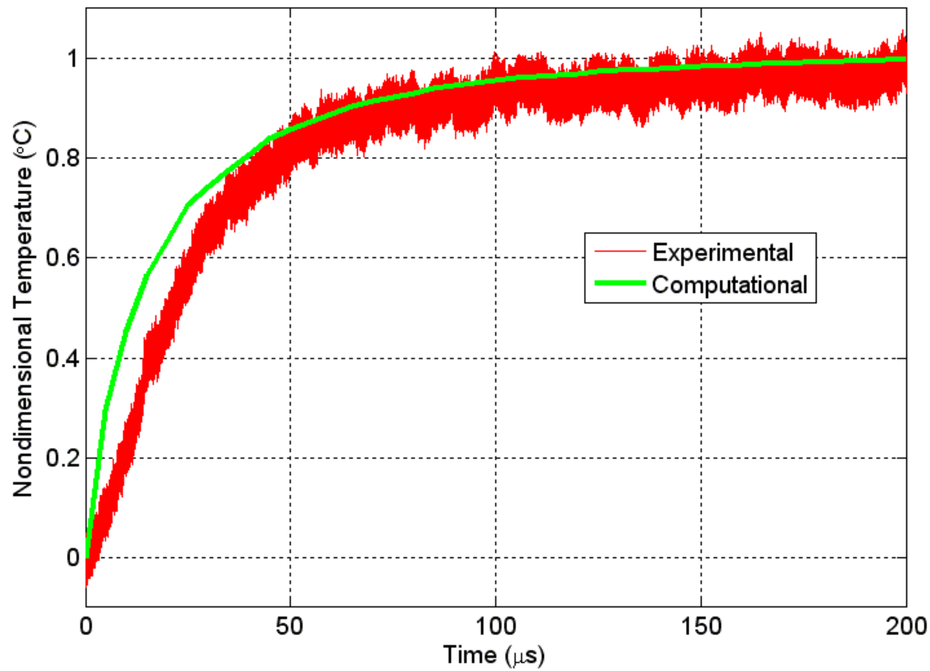


Figure 7-7: Comparisons of the computational model with the experiments.

7.4.2. Time step determination

Time step chosen for the transient characterization is a critical parameter. Reducing the time step increases the accuracy of the model at the expense of increased computational time. On the other hand, increasing the time step reduces the

computational time at the expense of the accuracy of the model. Simulations have been carried out for various time steps to determine the suitable time step. Figure 7-8 shows the transient response of 100 µm x 100 µm SLC for four time step: 1 µs, 5 µs, 10 µs and 20 µs. The selected time step size does not influence the accuracy of the model. However, time taken for the simulation increases significantly as the time step is decreased. For 1 µs time step, simulation take 36 hours to converge but at 20 µs time step, the same simulation only takes about 8 hours on a windows server with 3.2 GHz dual core processor and 12 GB of RAM. Although, the time constant of the superlattice cooler is 20 µs irrespective of the time step chosen, for simulations time step of 5 µs is chosen to properly resolve the response of the superlattice cooler.

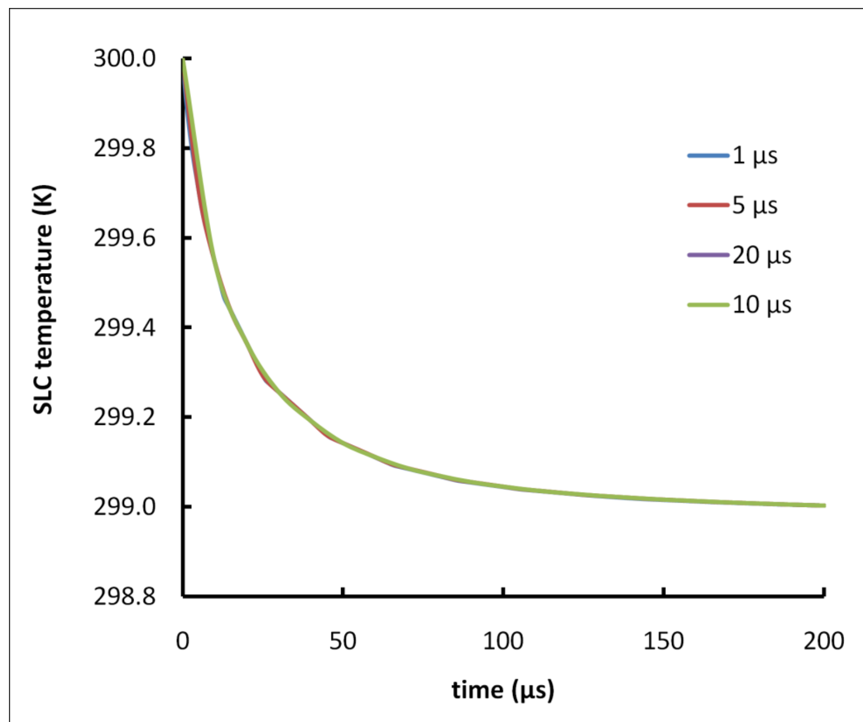


Figure 7-8: Effect of time step size on the transient response of SLC.

7.4.3. Effect of thermal resistance of the microchannel heat sink

Hybrid cooling scheme utilizes microchannel heat sink to remove low background heat flux. Heat transfer coefficient inside the microchannel depends upon the microchannel dimensions, and fluid properties. Besides removing the background heat flux, microchannel heat sink also removes the heat dissipated due to Joule heating (within the substrate) as well as Peltier heating (at the ground electrode). Therefore, the response time of the superlattice cooler not just depends upon the thermal resistance of the superlattice layer but also on thermal resistance of the microchannel heat sink. Time constant of the hybrid system can be defined as:

$$\tau^{th} = R^{th}C^{th} \tag{7.18}$$

where, τ^{th} is the thermal time constant, C^{th} is the thermal capacitance, and R^{th} is the thermal resistance defined as $R^{th} = 1/hA$. As thermal resistance increase, the time constant of the system increase. Figure 7-9 shows the transient behavior of the hybrid scheme for different convective thermal resistance of the microchannel heat sink. For all three cases, the initial response of the superlattice cooler is identical and is unaffected by the convective heat transfer coefficient inside the microchannel heat sink (insert of Figure 7-9). Furthermore, since the response of all three superlattice coolers is identical until 2 ms, this implies heat dissipated takes more than 2 ms to diffuse to the superlattice cooler. After 2 ms, temperature at the superlattice cooler starts to rise due to the parasitic heat transfer to the cooler. For the case of infinite heat transfer coefficient, temperature at the superlattice cooler does not increase even after 2 ms, which suggests no parasitic heat is transferred to the superlattice cooler (all the heat dissipated in the substrate as well as at the ground electrode is removed by the microchannel heat sink without it being

transferred to the superlattice cooler). As the heat transfer coefficient is decreased, parasitic heat transfer to the superlattice cooler increases and temperature rise at the superlattice cooler increases. Moreover, as predicted earlier, system takes longer time to reach steady state when heat transfer coefficient is low.

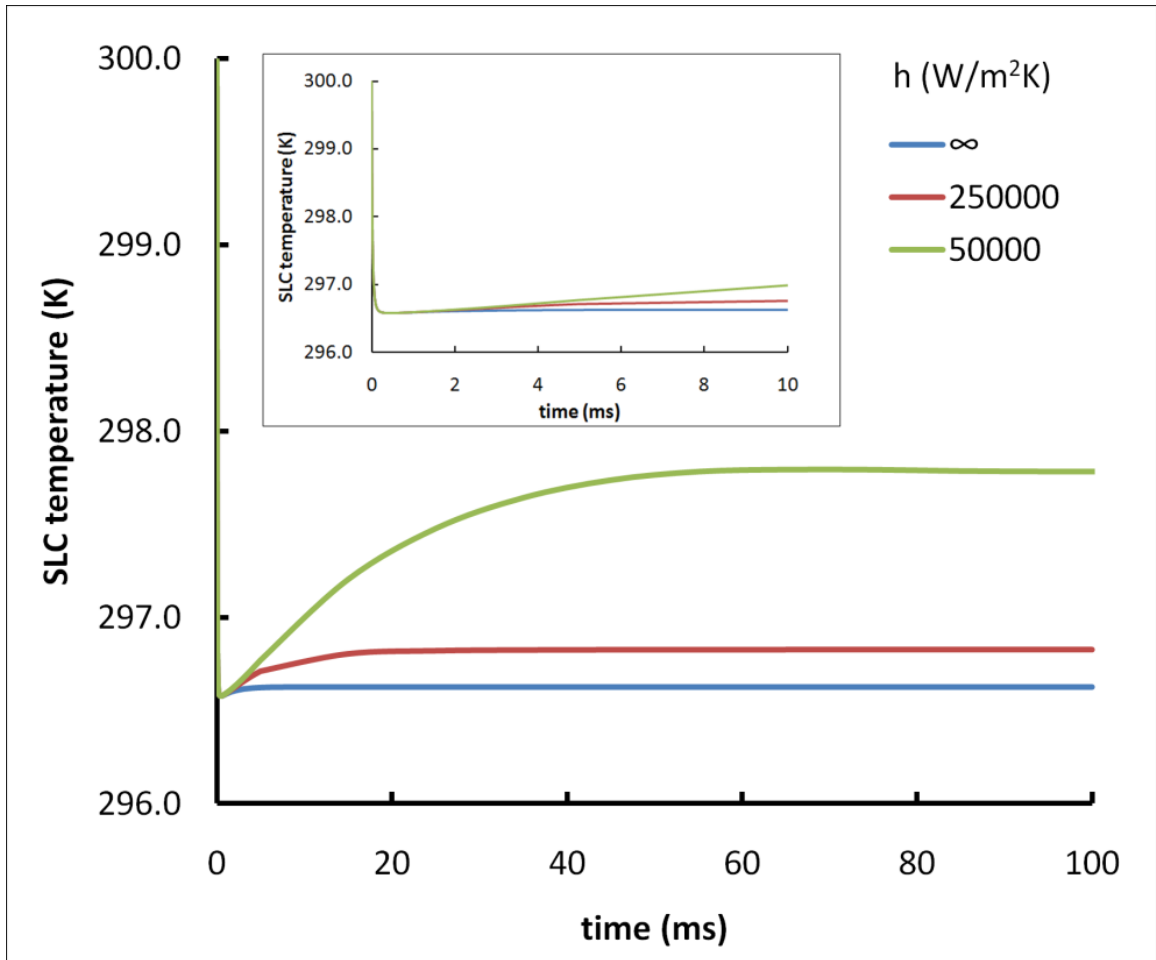


Figure 7-9: Effect of heat transfer coefficient on the transient response of the superlattice cooler.

Since the response of the system is independent of the heat transfer coefficient until 2 ms, a new mode of superlattice operation can be envisioned where superlattice is operated for short duration in pulsed fashion (less than 2 ms for this case). This operation mode can be useful when core activity is high only for the short duration. Superlattice coolers can be activated to manage the core for these short durations and then turned off.

The main advantage of operating the superlattice cooler in this mode is that it does not require efficient background cooling mechanism. Moreover, the operation time of the superlattice cooler can be tailored just by the placement of the ground electrode.

7.4.4. Transient coupling between SLCs

To remove spatially moving hotspots, an array of superlattice coolers is utilized. As shown in Chapter 6, the steady state performance of superlattice cooler in an array is affected due to the thermal coupling between the superlattice coolers. Simulations are performed to study the effect of thermal coupling on the transient behavior of superlattice coolers. Description of the simulation geometry is provided in Chapter 6. Activation current to both superlattice coolers is 500 mA. Heat transfer coefficient at the back of the substrate is assumed to be 250,000 W/m^2K. Figure 7-10 shows the transient response when single superlattice cooler is activated, as well as when both superlattice coolers are activated. In both cases, temperature drops when superlattice cooler is activated and then increases due to parasitic heat transfer to the cooler. Initial transient response (for time $<$ 100 μs) is identical for both cases. When two superlattice coolers are activated, parasitic heat transfer increases, hence, temperature rise is more in the latter case. However, for both cases steady-state is achieved at the same time. Even though cooling obtained in both cases is different, transient behavior is identical. Time scale associate with charge migration as well as chare relaxation is much shorter compared to the thermal time scale, hence transient behavior of the hybrid scheme is governed only by thermal time scale and since activating more than one superlattice cooler does not affect thermal time scale, transient behavior is identical for both the cases.

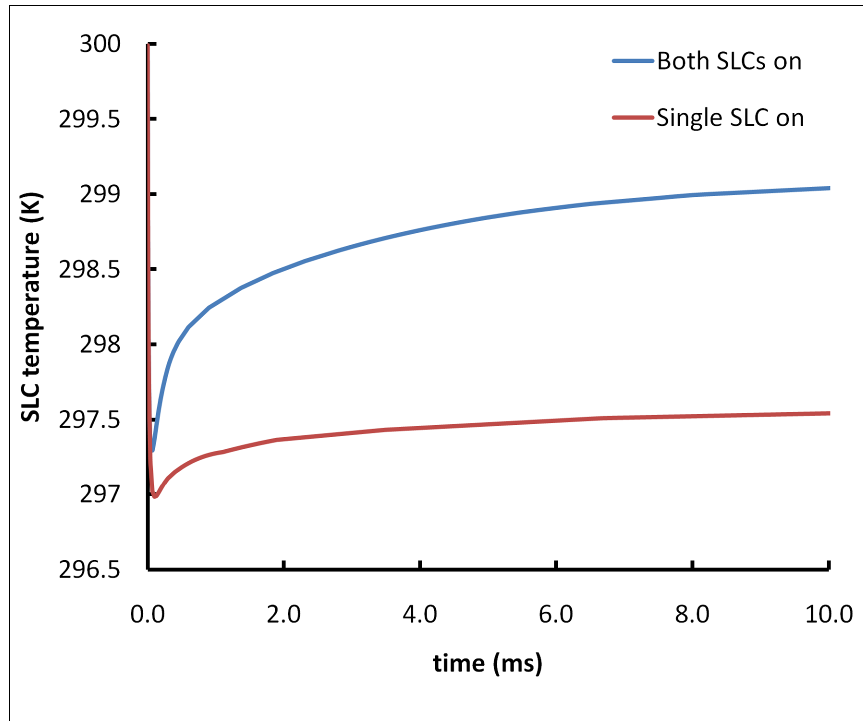


Figure 7-10: Effect of thermal coupling between superlattice coolers in transient domain.

7.5. Summary

This chapter discusses the transient behavior of hybrid cooling scheme. Superlattice cooler provides extremely fast response time with time constant in the range of 25 μs (without coating) to 35 μs (with coating). The time constant depends upon the thermal resistance of the microchannel heat sink, location of the ground electrode. Experiments as well as computational modeling have been performed to examine the effect of these parameters on the transient behavior. The time constant of the hybrid cooling scheme is inversely proportional to the convective heat transfer coefficient. The transient behavior of superlattice cooler is found to be independent of operating current, and superlattice size. Delay in activation of the superlattice cooler can lead to significant temperature jump at the hotspot, which can be minimized by reducing the delay time.

CHAPTER 8: CONCLUSION AND FUTURE WORK

This chapter summarizes the key aspects of the hybrid cooling scheme. It lists the original contribution of the dissertation. At the end, recommendations are made for the future work to extend the scope of the hybrid cooling scheme.

8.1. Summary

A novel hybrid cooling scheme has been investigated for thermal management of electronics. The hybrid cooling scheme is designed to dissipate non-uniform heat flux from the microprocessor in real time. It combines fluidic cooling and solid-state cooling to tackle background heat flux and hotspots respectively. In this dissertation, detailed characterization of the hybrid scheme is performed through use of experiments, computational and analytical models. An experimental prototype is fabricated using micro-fabrication techniques to examine the effect of operating parameters such as, activation current, ambient temperature, working fluid as well as geometric parameters, such as superlattice cooler size, ground electrode location. Thermal imaging of superlattice cooler under operation has been performed with an infrared microscope. Two types of test devices are fabricated: one with on-chip microchannel and other with off-chip microchannels to study the effect of thermal resistance between ground electrode and superlattice cooler as well as ground electrode and microchannel heat sink. Resistance network model of the hybrid scheme is developed to further investigate the effect of improved ZT. An electro-thermal model of the hybrid scheme is used to study the thermal coupling between the superlattice coolers and effect of operating and geometric parameters on the thermal coupling between two superlattice coolers. In the

end, transient characterization is carried out to examine the dynamic aspect of the hybrid cooling scheme.

8.2. Conclusions

(a) The optimum current is a function of superlattice size, ambient temperature, ground electrode location, as well as thermal and interface resistance. The optimum current increases with the superlattice size and ambient temperature. However, it decreases with interface and thermal resistance as the parasitic heat transfer from the ground electrode to the superlattice increases. Furthermore, the superlattice cooler should always be operated below its optimum current to minimize the operating power.

(b) Performance of the superlattice cooler improves with the rise in ambient temperature due to increase in Peltier cooling. In this study, increasing the ambient temperature from 23 ^{o}C to 85 ^{o}C results in 63 % enhancement in cooling and 88 % improvement in the CPD.

(c) The maximum temperature drop and the CPD of the superlattice cooler decreases with the superlattice size due to increase in parasitic heat transfer to the superlattice cooler. Several factors determine the optimum superlattice size such as: electrical contact resistance, electrical spreading resistance and thermal spreading resistance. Experiments show 33% reduction in the CPD for 300% increase in the superlattice size. Even though cooling power density decreases with area, total power dissipated by the superlattice increases with the superlattice cooler size due to increase in the area.

(d) Temperature is uniform across the superlattice cooler, except at the periphery, where it increases slightly, as observed through infrared imaging. For all three superlattice sizes temperature distribution is uniform for all the tested activation current.

(e) Presence of interface layer between the ground electrode and heat sink considerably diminishes the cooling at the superlattice cooler. Interface layer reduces the efficiency of the microchannel heat sink in removing the heat generated in the silicon and superlattice layers. Presence of the interface layer results in 400% reduction in cooling obtained at the superlattice cooler.

(f) Thermal resistance between the ground electrode and superlattice cooler is another critical factor affecting the performance of the hybrid scheme. For the off-chip microchannel configuration, which has an additional interface layer, thermal resistance between the superlattice and ground electrode plays a significant role. It reduces the maximum temperature drop achieved by the superlattice cooler by 25 %. However, for the on-chip microchannel configuration it does not affect the performance as the heat sink is effective enough to remove the heat. Even though performance of the on-chip microchannel is unaffected by the ground electrode location, the power required to operate the superlattice cooler increases considerably as the ground electrode is moved farther away from the superlattice cooler due to increase in the substrate electrical resistance.

(g) Thermal coupling between superlattice coolers reduces the performance of an array of superlattice cooler compared to an isolated superlattice cooler. The electro-thermal model reveals that thermal coupling between superlattice coolers

can reduce the performance of an isolated superlattice cooler by up to 87%. Thermal coupling is affected by the geometric and operating parameters.

i. Closer the ground electrode, higher the thermal coupling between superlattice coolers. As separation between ground electrode and superlattice cooler is reduced form 1000 μm to 100 μm, thermal coupling increases from 10% to 60%.

ii. Reduction in convective heat transfer coefficient augments the thermal coupling between superlattice coolers since the heat sink becomes less effective in removing the heat generated due to Joule heating in various layers as well as Peltier heating at the ground electrode. Reducing the convective heat transfer coefficient from 250,000 W/m^2K to 50,000 W/m^2K increases the thermal coupling by 87%. Even in the ideal case, (corresponding to infinite heat transfer coefficient) thermal coupling reduces the performance of superlattice cooler by 4 % compared to an isolated superlattice cooler.

(h) Experiments also show significant thermal coupling between the superlattice coolers. Trend observed with experiments agree with the computational model. Reducing the separation between the ground electrode and superlattice cooler and decreasing the convective thermal resistance both increase thermal coupling between superlattice coolers. Thermal coupling increases by 30% when water is replaced by FC72 as the working fluid.

(i) Response time of the superlattice cooler is independent of the operating current as well as superlattice size. However, the time constant of the superlattice cooler

increases the thermal resistance of the microchannel heat sink as observed through computational model. In the present study time constant of the superlattice cooler is measured to be 35 µs.

(j) To reduce the temperature fluctuation at the hotspot, superlattice cooler should be activated as soon as hotspot is detected. Since the temperature at the hotspot increases exponentially, even a few microseconds delay in the activation of the superlattice cooler will result in significant temperature fluctuations at the hotspot.

(k) Current state of the art thermoelectric materials used for the superlattice fabrication have low ZT thus limiting their application space. Increasing the ZT of the superlattice cooler drastically improves its performance. For 100 µm x 100 µm superlattice cooler, cooling power density as high as 1700 W/cm^2 and temperature drop of 20 K can achieved if the ZT is increased to 1.0.

8.3. Original contributions

(a) A novel hybrid cooling scheme for thermal management of microprocessors with high background heat flux in the presence of ultra high localized hotspots is proposed and investigated. The hybrid scheme provides a unique cooling solution for non-uniform heat flux dissipation in real time.

(b) An experimental prototype of the hybrid cooling scheme is fabricated using the micro-fabrication technique. Optimum bonding parameters for low temperature SU8 bonding has been obtained.

(c) Thermal resistance between the ground electrode and the microchannel heat sink is identified as performance limiting parameter. This resistance is reduced by

making on-chip microchannel, resulting in more than 100 % performance enhancement as compared to the off-chip microchannel heat sink.

(d) A detailed resistance network model for the hybrid cooling scheme is developed and validated with the experiments The resistance network model presented in this dissertation takes into account following parameters which were not included in the other resistance network models presented in literature:

   a. Joule heating in the top metal layer.

   b. Parasitic heat transfer from the ground electrode to the superlattice cooler.

   c. Finite convective thermal resistance between the heat sink and the ground electrode.

   Including above parameters makes the model more realistic and accurate.

(e) An electro-thermal model to study the thermal coupling between superlattice coolers is developed and validated with the experiments. The electro-thermal model solves heat conduction as well as charge continuity equations along with constitutive relations to yield temperature distribution and electric potential field. The model suggests thermal coupling between superlattice coolers increases as the ground electrode is placed closer to the superlattice cooler, or convective heat transfer coefficient inside the heat sink is reduced. Thermal coupling is a very strong function of the convective heat transfer coefficient inside the heat sink.

(f) Transient characterization of the superlattice cooler is carried out using the transient capability of the infrared microscope. A trigger circuits is designed to activate the hotspot and superlattice cooler simultaneously as well as trigger the infrared microscope at the same time. The trigger circuit also introduces a

specified time delay between the hotspot and superlattice activation to examine the effect of activation delay.

8.4. Recommendations for future work

(a) Future microprocessor will have 3D ICs to enhance the performance. In this work, hybrid scheme has been implemented for a 2D architecture. Since the superlattice coolers are monolithically integrated, the hybrid cooling scheme can be extended to 3D ICs. However, interface resistance will need to be minimized to get full advantage from the hybrid scheme for implementation in 3D ICs.

(b) In this work, superlattice coolers were fabricated directly underneath the hotspot heaters. In an actual die, this implementation is not feasible as superlattice coolers cannot be fabricated directly on the active side of the die. To make the hybrid scheme more realistic, both hotspot heaters and superlattice coolers can be fabricated on separate die and then bonded together or they both can be fabricated on the same die but on the opposite sides. Implementation of either of these methods presents significant fabrication issues and challenges which will need to be addressed.

(c) In Chapter 7, pulsed mode operation of superlattice cooler is suggested to enable cooling of cores which are active for short duration. The main benefit of pulsed mode operation is that the performance of the superlattice cooler becomes independent of the background cooling scheme. Experiments can be done to investigate the pulse mode operation of superlattice cooler and study effect of pulse duration on SLC performance.

(d) Current test devices have superlattice coolers arranged in a group of 3 to 4 in a linear fashion with separation of about 200 µm between them. This limits the examination of thermal coupling between the superlattice coolers. New layout with more arrays of superlattice cooler, which will have different spacing, as well as different shape and size can be perform a detailed characterization of thermal coupling.

(e) Current layout of the die does not have sufficient ground electrodes to proper characterize the effect of ground electrode location experimentally. Moreover, it only contains three sizes of superlattice cooler: 70 µm x 70 µm, 100 µm x 100 µm and 120 µm x 120 µm. New layout with more ground electrodes located at various distances as well as more variety in superlattice cooler size can be used to do more detailed experimental characterization.

(f) Superlattice coolers cannot be exposed to temperature more than 250 °C hence a low temperature SU8 bonding technique is used. However, SU8 is a polymer and adds significant thermal resistance between the heat sink and ground electrode. Other bonding techniques such as, low temperature HF bonding, hydrophilic bonding, etc. have been reported to be performed below 200 °C and they do not add any interface layer. In this work, low temperature HF bonding was carried out but the bond strength was not sufficient to seal the microchannels. More careful optimization of the bonding parameters might provide a good seal. Use of low temperature bonding will reduce the interface resistance and thus will improve the performance of the hybrid scheme (especially for off-chip microchannel

configuration, which is significantly affected by the presence of interface resistance).

(g) The ZT of the superlattice cooler used in this work is around 0.09. As mentioned earlier, the performance of the superlattice increases drastically as ZT is increased. This suggests need to develop higher ZT material or utilize Bismuth telluride (which has reported to have ZT close to 1) for superlattice fabrication.

(h) Superlattice structure is grown using Molecular Beam Epitaxy, which is very slow and expensive process. The cost of the cooling scheme might be an inhibiting factor in its utilization for electronics cooling. Other techniques such as MOCVD can be utilized to reduce the cost of the superlattice fabrication as well as hybrid cooling scheme.

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