EMBEDDED THERMOELECTRIC DEVICES FOR ON-CHIP COOLING AND POWER GENERATION

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EMBEDDED THERMOELECTRIC DEVICES FOR ON-CHIP COOLING AND POWER GENERATION

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To my father,

Robert Tew Sullivan (1954-2008),

the smartest and most adventurous Dad that a son could ask for.

Without his support and nurturing of my scientific mind,

I would never have made it this far.

Love you Dad!

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CHAPTER I

INTRODUCTION

Seebeck, Peltier, and Thomson discovered the phenomenon of thermoelectricity in the early 1800's [1, 7]. Over the last century, thermoelectric devices have been used in many power generation or cooling applications, such as energy recovery in space and cooling of sensors located in heat-sinking missiles [1]. Until recently, however, thermoelectric applications have often been highly specialized and have not conformed to the constraints of more traditional technologies due to low efficiencies of thermoelectric materials (TEMs). Thermoelectric devices operate at approximately 10% of Carnot efficiency, whereas a typical kitchen refrigerator can operate at approximately 30% and a large building's HVAC system can operate at approximately 60% [1, 7]. TEMs have been used mainly in cases where small size, low weight, and high reliability are more important issues than efficiency [7]. Recent advances in thermoelectric materials, though, have motivated further research into a broader spectrum of applications where conventional technologies have been used in the past.

In the case of power generation, thermoelectric materials produce an emf, known as the Seebeck voltage, when a temperature difference is applied across the two ends of the materials. Thermoelectric generators (TEGs) have been used on spacecraft to provide an energy source millions of miles away from the Earth's surface [1]. This is an extreme case, but TEGs have also been used on Earth to generate power for remote data communication system for oil and gas pipelines and polar weather stations [7]. Recently, some work has delved into the possible use of TEGs in automobile exhaust pipes to reduce the load on a vehicle's alternator [31], and there are many other possible applications as new thermoelectric materials are discovered and engineered

to be more efficient.

Thermoelectric devices can also be used as heat pumps or thermoelectric coolers (TECs) using the Peltier effect, which results from a current applied through a thermoelectric device. The Peltier effect is the reverse of the Seebeck effect, which leads to electric potential across a device when subjected to a temperature difference. There are many current applications of thermoelectric coolers, including cooling of laser diodes to keep them at constant temperature, climate-controlled seats in cars to provide passenger comfort, and portable ice-free beverage coolers [1].

Recent work in thermoelectric devices has improved their efficiency, resulting in figure of merit, ZT, values of approximately 2, but the figure of merit must increase to approximately 9.2 in order to compete with two-phase refrigeration systems [1]. The figure of merit does not need to be 9.2 to be of interest in the field of microelectronics, however. Chowdhury et al. have fabricated and tested superlattice-based thin-film thermoelectrics that display improved cooling capabilities, an approximate ZT of 2.1, and a very small form factor [5]. Superlattice thin-film thermoelectrics are therefore a possible cooling solution for a microchip package, as they can be incorporated within the package and provide a discreet form of embedded cooling for microchips in comparison to other technologies such as microfluid channels.

In follow-up to the preliminary experimental work by Chowdhury et al. in *Nature Nanotechnology* [5], this work explores the possibility of embedding thermoelectric devices within electronic packaging for both hot spot cooling and power generation, using the commercial CFD solver FLUENT and the analog electronic circuit simulator SPICE, to investigate operation of single and arrayed thermoelectric devices integrated inside a micro-electronic package. The effect of electrical and thermal contact resistances and the location of thermoelectric device in package and energy efficiency of thermoelectric device operation are explored for both steady-state and transient mode operation.

In Chapter 2, an in-depth background of thermoelectric devices is presented with emphasis on the progression of thermoelectric materials over the years and research related to thermoelectric devices integrated with microelectronics.

In Chapter 3, the computational methodology for this work is outlined. It outlines the governing heat transfer equations of the package and thermoelectric devices and describes the models constructed in the commercial CFD solver FLUENT and the analog electronic circuit simulator SPICE.

Chapter 4 outlines the modeling and simulation results, using FLUENT, of an array of nine TECs embedded inside a microchip package. The study begins with steady-state analysis with specific emphasis on the thermal coupling among adjacent TECs within the package. It then progresses to transient analysis, showing the additional cooling possible with transient current pulses through TECs. A study of pulse shapes exhibits the cooling behaviors using transient pulses, and further analysis is completed to find the best current shape given several optimization parameters. Finally, transient cooling with TECs is investigated on a package with three random hot spots to simulate a more realistic scenario and illustrate the long term effects of transient cooling.

Chapter 5 builds a compact model in SPICE, the electronic circuit simulator, which is capable of simulating operation of TEC(s) in a microchip package faster and with high accuracy compared to the FLUENT model. The SPICE model is validated against steady-state and transient FLUENT results. Several parameters were investigated to analyze their effect on cooling; these included the proximity of the TEC to the chip, the thermal contact resistance within the TEC, and the cooling solution used to cool the package.

Chapter 6 presents an investigation of superlattice thermoelectric generators embedded inside a microchip. The model is a modified version of the FLUENT model used in Chapter 4. Various parameters were considered to investigate their effect on a

single thermoelectric generator, including load resistance, background heat flux, and proximity of a TEG to chip. An array of thermoelectric generators is also studied to determine the effect of adding multiple TEGs on-chip to boost the total useful power generated. A simple transient simulation is completed as well, showing how the thermoelectric generators react when the background heat flux is changed.

Chapter 7 presents the conclusion and includes discussion of possible future work.

CHAPTER II

BACKGROUND

2.1 Thermoelectric Devices

Thermoelectric (TE) devices can function as heat pumps or heat engines, depending on the desired application. Heat pump TE devices use electricity to provide cooling or heating, and heat engine TE devices harvest electricity from temperature gradients, usually caused by the expulsion of waste energy. Thermoelectric devices are environment friendly and can help reduce CO_2 and greenhouse gas emissions [1]. TE devices are simpler in operation than systems that compress and expand a two-phase fluid as they have no moving parts or bulk fluids and are lightweight, small, and inexpensive [1, 7]. TE devices are also useful for rapid on-off cycling at low temperatures since they are highly reliable and have fast response times [7]. On-off cycling refers to the cyclic operation of any heat source. This often applies to transistors on an electronic chip because the full processing power of a chip is generally not needed all of the time and, thus, many transistors are inactive at any instant [10]. The main drawback of TE devices is their low efficiency relative to traditional methods of heating/cooling and power generation. The efficiency of TE devices is approximately 12% of the carnot efficiency compared to 30-60% for the traditional systems [1, 7].

Jean Peltier, a French scientist, discovered the Peltier effect in 1834 [1, 7]. Peltier observed heating at the junction of dissimilar electrically conductive materials when a current was applied and observed cooling at the junction when the current direction was reversed [1]. The dissimilar materials are n-type and p-type semiconductors. A voltage across a p-n junction creates electron/hole pairs. Electrons flow away from the junction in n-type materials, and holes flow away from the junction in p-type

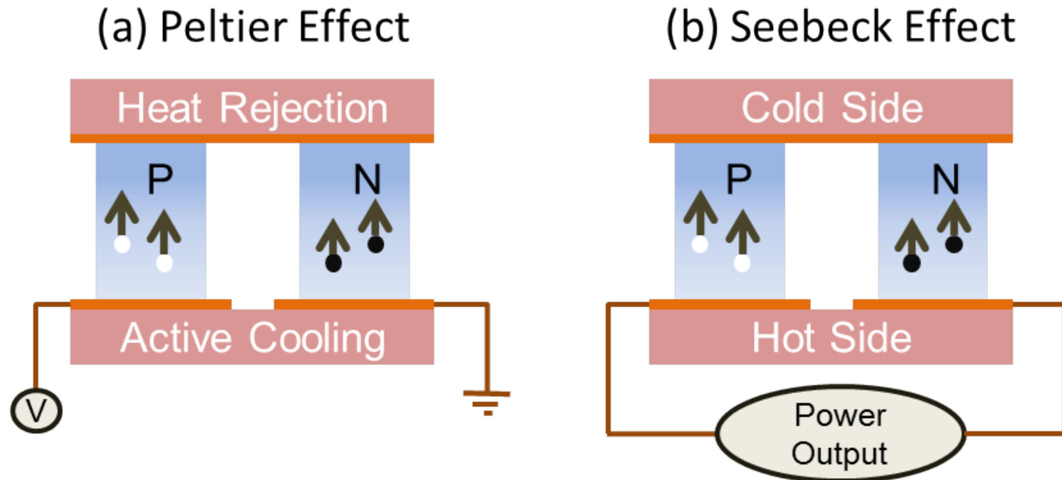


Figure 1: (a) Peltier effect across a p-n couple due to an applied voltage (b) Seebeck effect across a p-n couple due to an applied temperature gradient

materials. This movement of electrons and holes requires energy and thus removes energy from the junction, effectively cooling the junction [1]. At the opposite end, electrons and holes recombine, which releases energy and heats the junction [1]. This heating and cooling effect can be seen in Figure 1(a).

Thomas Seebeck discovered the Seebeck effect in 1821 [1, 7]. Seebeck noticed a needle deflects in the presence of dissimilar metals when exposed to a temperature gradient and connected in series electrically and parallel thermally [1]. The temperature gradient causes electrons and holes to flow from the hot junction to the cold junction and recombine, similar to the Peltier effect [1]. The flow of electrons causes a build-up of electrons at the cold junction and creates an electric potential between the two ends called the Seebeck Voltage, which deflected the needle [1]. The Seebeck effect is the basis of temperature-measurement using thermocouples as it creates an electrical signal in response to temperature. The Seebeck effect is illustrated in Figure 1(b).

The Peltier and Seebeck effects both rely on materials that are good electrical conductors and poor thermal conductors. High electrical conductivity is important because it reduces electron scattering; low thermal conductivity is important because

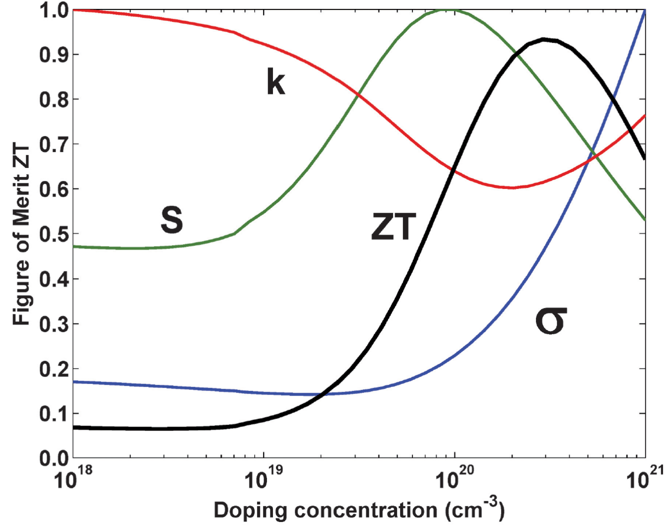


Figure 2: Interdependence of Seebeck coefficient, S, electrical conductivity, σ, and thermal conductivity, k, as related to the doping concentration of n-type $Si_{80}Ge_{20}$ at 300 K. Adapted from [21].

it reduces the backflow of heat and maintains the temperature difference between the junctions [1]. In addition to electrical and thermal conductivity, the Seebeck coefficient must also be optimized in order to ensure an efficient TE device operation [1]. These three material parameters must be optimized simultaneously, as they are all highly correlated [1]. The thermal conductivity is related to the electrical conductivity through the Wiedemann-Franz relationship:

$$\kappa_e = L_o \sigma T \tag{1}$$

where κ_e is the charge carrier contribution of thermal conductivity, L_o is a constant called the Lorenz number (2.44x10^{-8}[WΩK^{-2}]), σ is the electrical conductivity, and T is the temperature [33]. Figure 2 illustrates this by plotting the dependence of the Seebeck coefficient (S), electrical conductivity (σ), and thermal conductivity (κ) against the doping concentration of n-type $Si_{80}Ge_{20}$ at 300 K [21]. As can be seen in the figure, improvements in one parameter often correspond to degradation of another key parameter. It is desirable to have a base material that can be n- and p-type doped, as this allows the same material to be used at both sides of the junction with different

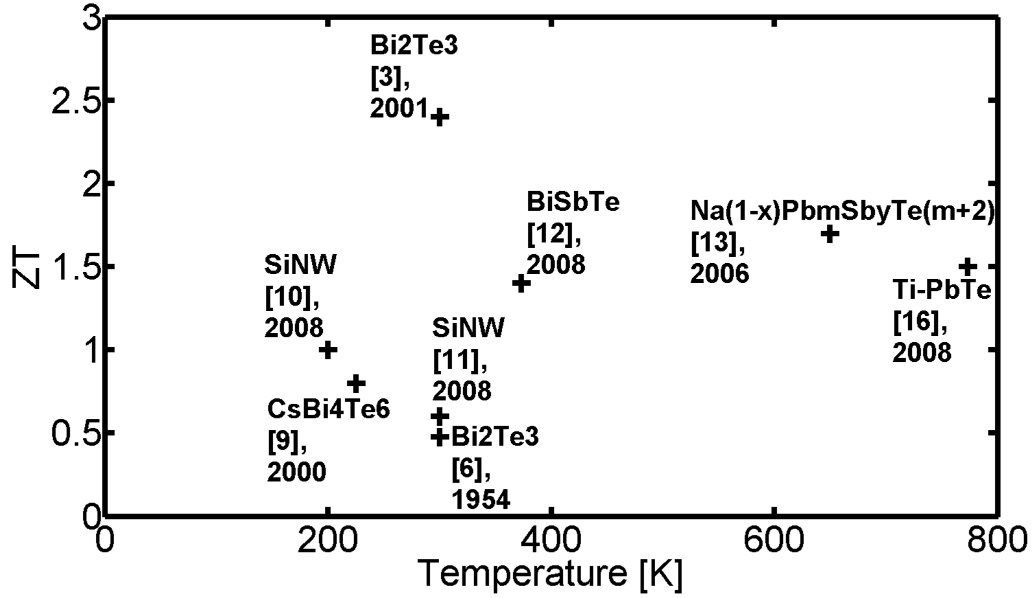


Figure 3: Figure of merit values versus temperature for various materials with year of measurement. All materials with $ZT > 1$ have been achieved using nanostructuring. Adapted from [35]

doping concentrations [1].

Thermoelectric materials are categorized based on the figure of merit, ZT, given by:

$$ZT = \frac{S^2 \sigma T}{k} \tag{2}$$

where S is the Seebeck voltage per unit of temperature, σ is the electrical conductivity, k is the thermal conductivity, and T is the absolute temperature. The efficiency of the thermoelectric material improves with increasing ZT. Increase in electrical conductivity and decrease in thermal conductivity are both sought after, but due to the high correlation between electrical and thermal conductivity, accomplishing both is a difficult objective. A ZT of 1 is approximately 10% of the carnot efficiency and a ZT of 4 is approximately 30% of the carnot efficiency. Nanostructured materials are being researched and have reached average ZT values of a little over 1 with an outlier reaching higher than 2 in Figure 3 [33, 35]. The outliers illustrate one of the major difficulties with nanostructured thermoelectric materials, which is the ability

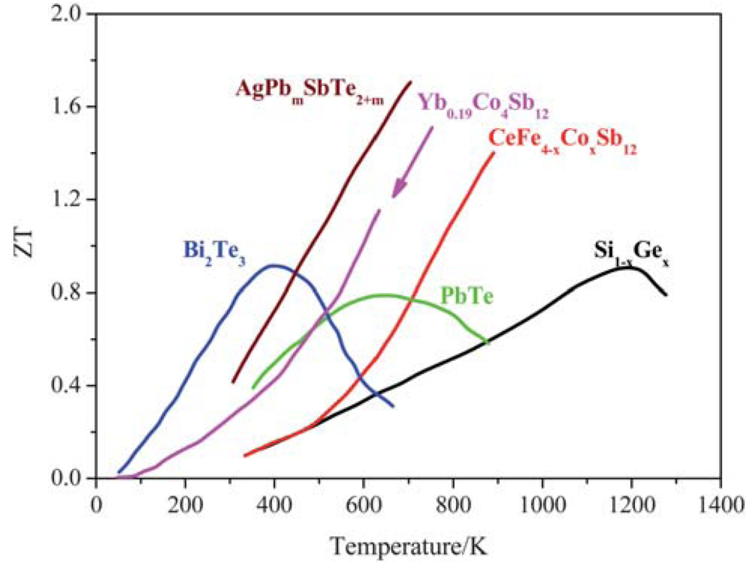


Figure 4: Figure of merit versus temperature for various materials. Adapted from [33]

to obtain reproducible and reliable measurements of κ, σ, and S, as many of the outlier results have not been reproduced [33].

Theoretically, the best thermoelectric material is "phonon glass, electron crystal," as it will have low thermal conductivity but still conduct electricity well [21]. The most efficient bulk thermoelectric materials were alloyed semiconductors for many years. Alloyed semiconductors have a high carrier concentration, which increases electrical conductivity, disrupts the transport of phonons, and decreases thermal conductivity. Some examples of well-known bulk alloyed thermoelectric materials include $Bi_xSb_{2-x}Te_3$ and PbTe-PbSe [21]. Alloy thermoelectric materials had a theoretical limit on their efficiency called the "alloy limit," and thermoelectric materials were stuck at this limit for several decades [35]. Due to increased research in nanoscale structuring of materials, substantial improvements in thermoelectric materials have been achieved in the past decade. The nanostructured materials are categorized into three subcategories: two-dimensional (2-D), one-dimensional (1-D), and zero-dimensional (0-D).

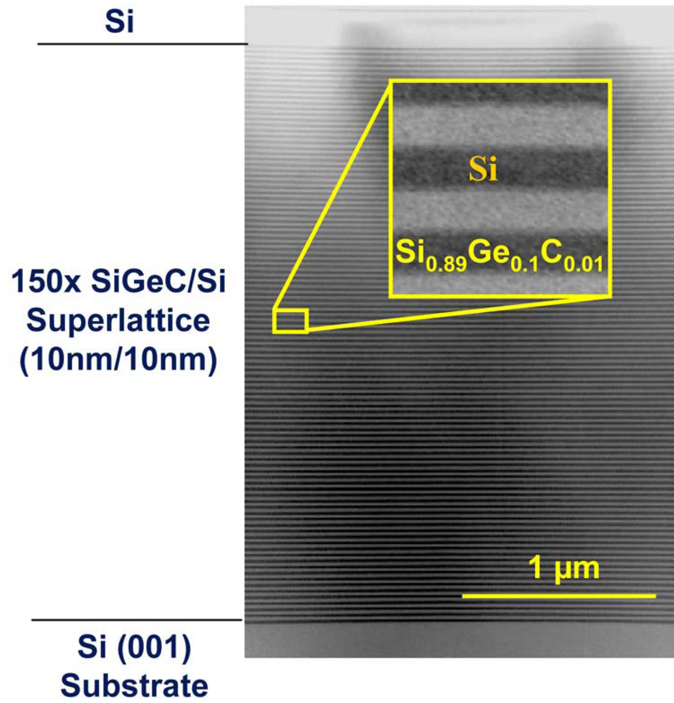


Figure 5: Transmission electron micrograph of $Si_{0.89}Ge_{0.1}C_{0.01}$ superlattice structure. Adapted from [24].

The two-dimensional nanostructured materials use quantum wells and superlattices in order to achieve higher figures of merit. The superlattice structure confines higher energy (hotter) carriers between planes while still allowing lower energy (colder) carriers to flow freely. Confinement of hot carriers reduces thermal and electrical conductivity, but the superlattice is designed to affect thermal conductivity, k, more than electrical conductivity, σ, therefore it results in an overall increase in the figure of merit. Hicks and Dresselhaus predicted that quantum confinement could lead to a ten-fold increase in the figure of merit [35]. In order to achieve significant increase in ZT, it has been hypothesized that the superlattice period must be smaller than 3 nm [35]. The physical reasons for the impact of the superlattice structure on thermal conductivity are attributed to modifications of the phonon spectrum, resulting from zone folding, bandgap formation, and phonon localization [35]. It has been suggested that the interfacial area per unit volume may be the most important

factor in decreasing the thermal conductivity in a lattice [33]. The selection of the materials used in the superlattices is also important, and often the pairs of materials are selected to have small or no band offsets and large relative static permittivities [35]. The thermoelectric device modeled in this work is based on a thin-film superlattice thermoelectric cooler fabricated and tested by Chowdhury et al. [5]. A thin-film superlattice TEC is used because it has an increased figure of merit compared to other TECs on the market and it is thin enough to fit inside an electronic package for on-chip cooling [5]. A transmission electron micrograph of a $Si_{0.89}Ge_{0.1}C_{0.01}$ superlattice is shown in Figure 5 [24]. One can see the separate planes of silicon and germanium alternating layers throughout the superlattice structure. The superlattice in Reference [5] is of similar structure, but it is made of Bismuth and Telluride.

Two alternative methods of 2-D nanostructuring include carrier energy filtering and thermal diodes [35]. Both methods require cross-plane carrier transport, in contrast to in-plane carrier transport. Cross-plane direction is usually the direction of lowest thermal conductivity which translates to a boost in the Seebeck coefficient [35]. Carrier energy filtering filters out the lower-energy carriers, which increases the Seebeck coefficient [35]. Thermal diodes place the n-type and p-type materials in a diode structure and increase the power factor, $S^2\sigma$, but the physics behind thermal diodes is not well understood yet and it cannot be determined whether the diode structure is the sole reason for the enhancement [35].

One-dimensional nanostructuring is showing great promise with the recent fabrication of nanowires. Nanowires are quantum wires with diameters $\geq$ 5 nm [35]. Currently, however, most of the work with nanowires have been theoretical studies showing the benefits of thermoelectric materials with nano length scales. Experimental work with nanowires is limited, but a few studies have been completed with rough silicon nanowires. The figure of merit for the silicon nanowire was measured to be approximately 0.6 at room temperature, in comparison to $\sim$0.01 for bulk silicon [35].

The thermal conductivity of silicon nanowires scales proportional to $(D/\Delta)^2$, where D is the diameter of the nanowire and Δ is the surface roughness of the nanowire [33]. Therefore, the figure of merit can theoretically be improved by decreasing the diameter of the nanowires or increasing the surface roughness. Phonon drag effects have been suggested as the primary cause for the increase in ZT for nanowires, but this is still a new area of research so results are inconclusive [35].

Zero-dimensional nanostructuring consists of the inclusion of quantum dots within thermoelectric materials. As with thermal diodes, the inclusion of quantum dots has not explicitly been shown to improve the performance of thermoelectric materials, but initial measurements show enhanced properties. Quantum dots are hypothesized to scatter mid- and long-wavelength phonons, which further reduces the thermal conductivity below the alloy limit, since alloying only scatters short-wavelength phonons [35].

A major problem with nanostructured materials is that they are inherently unstable, so high operating temperatures are a problem. As the temperature increases, desired 'defects' diffuse, and this leads to degradation in the thermoelectric material properties back to the bulk values [33]. Nanostructured materials are most frequently fabricated using atomic layer deposition (ALD), which is an expensive manufacturing process and is not suitable for mass production. Bulk manufacturing of nanostructured thermoelectric materials is an important area of research as it will significantly decrease the cost of nanostructured thermoelectric materials and allow thermoelectrics to infiltrate more market segments in the future.

2.2 Thermoelectric Coolers

Thermoelectric coolers (TECs) use the Peltier effect to pump heat, using electricity as their working fluid. TECs are used in a variety of specialized applications, but as the figure of merit for the thermoelectric materials has increased so have the

number of applications. Power dissipation in microelectronic processors is highly non-uniform on both local and temporal scales, which results in the generation of several hot spots on the chip [37]. Rapid removal of high heat fluxes from these hot spots can provide lower temperatures and greater thermal uniformity on the chip, which can significantly improve chip performance and reliability [5, 18, 20, 37]. Chowdhury et al. demonstrated a thin-film superlattice thermoelectric cooler thin enough to fit inside an electronic package and efficient enough to cool hot spots on-chip and achieve a more uniform temperature distribution [5]. Although conventional cooling technologies involving conduction and convection mechanisms are capable of removing high heat fluxes, they are not able to provide site-specific on-demand cooling of the chip [5, 41]. Design of system level cooling solutions is primarily driven by peak temperatures on the chip. This design approach results in bulky and inefficient cooling systems that are incapable of handling exclusively localized high heat fluxes [20]. Thermoelectric coolers have been proposed as an effective solution for providing site-specific on-demand cooling which may boost the performance of semiconductor devices, improve the reliability of electronic systems, and increase the operation life of electronic circuits [12, 25, 32, 34].

The size of the thermoelectric pellets in a thermoelectric module (TEM) affects the overall size of the device and therefore influences the feasibility of integrating TECs within an electronic package. Pellet geometry also has significant effects on the TEC performance and crucial operating parameters such as cooling rate, coefficient of performance (COP), temperature difference across the TEM, and operating current and voltage [13, 14]. A limiting factor of TECs with small thermoelectric pellets is the interfacial resistances, since they become a bottleneck in performance as size of the pellets decrease [13]. Interfacial resistances have a large impact on design and implementation of thermoelectric coolers. The thermal contact resistance and electrical contact resistance at the TEC's interfaces are affected by the fabrication

process and are considered two of the most critical parameters affecting the device performance [6]. High electrical and thermal contact resistances significantly degrade the performances of these devices [17, 19].

TECs can be utilized both for steady as well as transient operations. Their steady state behavior is well studied and utilized in various commercial applications [23]. Pulsed transient operation of TECs can provide additional cooling over steady state for a short period of time [15, 27, 40, 42]. The Peltier effect appears at the junction of thermoelectric elements, while Joule heating occurs throughout the volume of the thermoelectric elements. This difference, between surface effects and volume effects, explains the additional cooling during transient pulsed operation, i.e., Peltier cooling occurs before the effect of Joule heating is realized at the cold junction. This transient behavior has been studied in detail theoretically and experimentally by Snyder et al. in Reference [27]. In this study, Snyder et al. explored various parameters such as current pulse amplitude, thermal diffusivity, super-cooled temperature, and time to reach minimum temperature. The study was focused on thick TEC modules. An example of the positive and negative aspects of pulsed cooling can be seen in Figure 6 [27]. The TEC is operating at the best steady-state current of 0.675 amperes and then pulsed with a current 2.5 times larger than the steady-state current. An additional cooling is realized immediately, but after the pulse is turned off there are many negative temperature effects such as high temperature overshoot and long settling time.

Chip-scale integration requires ultrathin TEC modules, which means electrical and thermal contact resistances at the superlattice-metal interface and the TEC module-spreader interface can significantly affect the TEC performance [5]. Some efforts have been made to study the effect of these parasitic resistances, and it has been suggested that the impact of electrical contact resistance can be much more pronounced for thermoelectric coolers of length of the order of 100 μm or smaller [17, 19, 22, 36, 39].

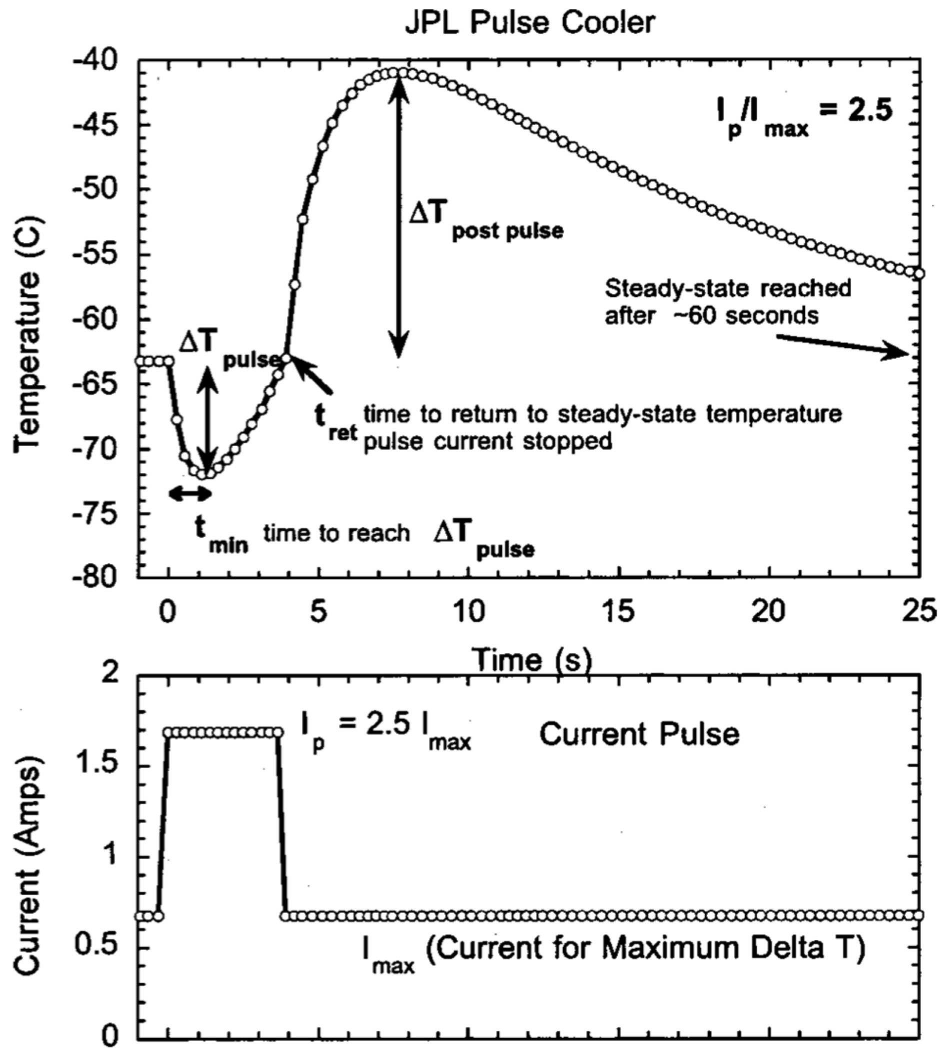


Figure 6: Example of pulsed cooling with thermoelectric cooler. Top: Temperature of the cold junction. Bottom: Current pulse passed through TEC. I_{max} is the best steady-state current, 0.675 amperes, and I_p is the pulse current, 2.5*I_{max} or 1.69 amperes. Adapted from [27]

Wang et al. have studied the effects of various crucial contact parameters, such as electrical contact resistance on the performance of silicon based thermoelectric microcoolers. Their study employed an analytical model to explore the effect of electrical contact resistance and the width of the wire lead used to send current into the microcooler. Wang et al. report that electrical contact resistance could potentially degrade TEC performance by up to 43% [36]. Pulse cooling performance is severely degraded by Joule heating due to these parasitic contact resistances [17].

Recently, TEC modules made of ultrathin (100 micron) Bi_2Te_3 based superlattices have been successfully integrated onto the heat spreader of an electronic package with total cooling up to 15°C at the hot spot [5]. This suggests the possibility of cooling dynamic hot spots by integrating multiple thermoelectric coolers that can be switched on and off on demand at the locations of dynamic hot spots. An on-chip array of multiple thermoelectric coolers has been fabricated by Goncalves et al.[9]. The authors predicted cooling of 15°C from numerical models but experimentally observed a maximum temperature difference of 5°C between hot and cold sides of a TEC [9]. The cooling effects of their TECs were degraded approximately 66% by high electrical resistance and low thermal conductance at the interface of the thermoelectric material [9].

2.3 Thermoelectric Generators

Thermoelectric generators (TEGs) use the same physics as the thermoelectric coolers except that they work in a passive manner. TEGs generate a voltage from a temperature difference between the hot and cold junctions of the thermoelectric material. Electron/hole pairs will form at the hot end and recombine at the cold end, essentially forming an electric potential or voltage between the two junctions. This voltage is known as the Seebeck voltage and can then be harnessed to power electrical

circuits. TEGs have been most frequently used for power generation in remote areas where maintenance is difficult to perform and reliability is very important; some examples include data communication systems for oil and gas pipelines and polar weather station power generators [7].

The equation for the Seebeck voltage generation can be given by

$$V = (\alpha_p - \alpha_n)(T_h - T_c) = S\Delta T \tag{3}$$

where α_p and α_n are the Seebeck coefficients of the p and n poles, respectively, T_h and T_c are the temperatures of the hot and cold junctions, respectively, and S and ΔT are the shorthand abbreviations for these terms [8]. Given this equation for voltage, all other useful terms can be written as simple electrical equations, such as current, I=V/R and power, $P=I^2R$. The total power created by the thermoelectric generator can be found by multiplying current and voltage together, but the total power has two distinct parts– useful power and dissipated power. Dissipated power results from Joule heating whereas useful power can be used external to the generator to accomplish other electrical tasks. The useful power can be estimated using this equation:

$$W = \left[\frac{S\Delta T}{R_L + R}\right]^2 R_L \tag{4}$$

where R_L and R are the load resistance and device resistance, respectively [8].

Mathematical models of thermoelectric generators are outlined in [4] and [38]. They consist of a thermoelectric generator connected in series with a load resistance between two heat reservoirs at temperatures, T_H and T_L, high and low, respectively. The schematic can be seen in Figure 7. This setup is common for studies on modeling of thermoelectric generators, and it achieves satisfactory results with small error for the systems where the two sides of the TEG are kept at approximately the same temperatures. An example of this system in practice would be a TEG placed between two fluid flows of different temperatures, as might happen for TEGs placed on the

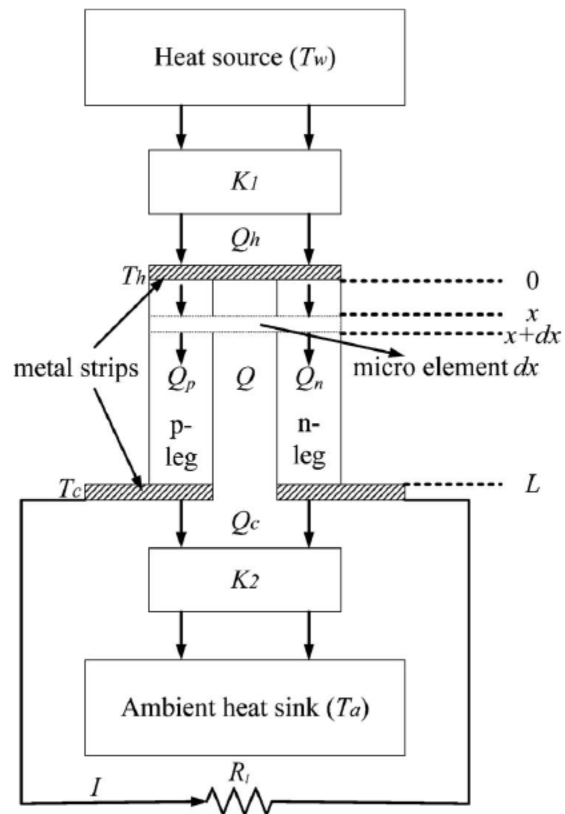


Figure 7: Schematic of thermoelectric generator model with the two junctions of the TEG kept at constant temperatures. Adapted from [4].

exhaust systems of cars. The car exhaust would be at a higher temperature than the surrounding ambient air, and since both air flows are moving with high velocity, the two sides of the TEG will remain at almost constant temperature. Chen et. al. created a CFD model of this setup in FLUENT with hot and cold fluid sources on either side of the TEG, and results were compared with other simulations and experimental data from TEGs [3]. They found agreement between experimental measurements and numerical simulations [3]. 3D modeling of the system helps in further understanding bottlenecks within the system since one can observe the temperature gradients throughout the entire system which can lead to better design and efficiency [3].

Solbrekken et al. attached 1 mm thick TEGs to a portable device's CPU and used the generated power to drive a cooling fan [28]. The fan was able to keep the CPU temperature below 85°C in a 35°C ambient environment [28]. This solution harvests energy from the waste heat and powers the thermal cooling solution (∼fan) for the package, turning an active form of cooling into a passive form since it no longer requires battery power [28]. One mm thick TEGs are too thick to be embedded inside electronic packages, but Chowdhury et al. have fabricated a thin-film superlattice thermoelectric cooler (TEC), which are thin enough ($\sim 100\ \mu m$) to be embedded within a package [5]. The ultrathin superlattice based TECs showed increased performance compared to the other TECs due to the high figure of merit of the thermoelectric material [5].

There are many studies on power generation using TEGs [2, 3, 4, 26, 28, 38], but the investigation of power generation using ultrathin TEGs embedded within an electronic packaging has not been performed. Most models of the TEGs consider constant temperatures at the hot and cold junctions [4, 38, 3]. Constant temperatures at the two junctions of the thermoelectric generators is applicable in only a few situations, such as fluid flow on both sides of a TEG with different temperatures as presented in [3]. The maximum useful power generation corresponds to the case

when the load resistance is equal to the device resistance while temperature across the device is kept constant. Solbrekken et al. reported that maximum power generation occurs when the load resistance is not equal to the device resistance. This can occur if the temperatures of the junctions are not constant. Given that this situation is more realistic and applicable for a larger set of scenarios, it is important to analyze the optimum load resistance for power generation using ultrathin TEGs embedded inside a package.

The next chapter outlines the computational methodology of this work including the governing equations and the methods used for models developed using FLUENT and SPICE.

CHAPTER III

COMPUTATIONAL METHODOLOGY

The developed computational models and governing equations are presented in this chapter. The models are developed using two software packages: FLUENT and SPICE. FLUENT is a computational fluid dynamics package, and SPICE (Simulation Program with Integrated Circuit Emphasis) is an analog electronic circuit simulator. The finite volume method based model is first developed using FLUENT, then a compact model is developed in SPICE in order to reduce computation time and enable the integration of the compact model with models of electronic circuits for further simulations.

3.1 Finite Volume Method Based Model

A finite volume method based computational model is developed in FLUENT to analyze the effect of a TEC device on temperature reduction at a hot spot on-chip. The developed model solves Fourier's conduction equation in the electronic package and TEC module to obtain temperature distribution. The package and thermoelectric device geometry considered in the present work is similar to the geometry used in Reference [11]. In Reference [11], the packaged TEC model is validated against Chowdhury et al.'s experimental and numerical work with superlattice thermoelectrics [5].

Reference [5] gives a detailed description of a numerical model validated against their experimental results for a superlattice Bi_2Te_3 TEC module embedded between a test chip and heat spreader. Effective bulk material properties for the TEC module are given in Ref. [5]; the bulk superlattice material properties are Seebeck coefficient, S, of 301 $\mu V/K$, electrical resistivity, ρ, of 1.08*10^{-5} Ω-m, and thermal conductivity,

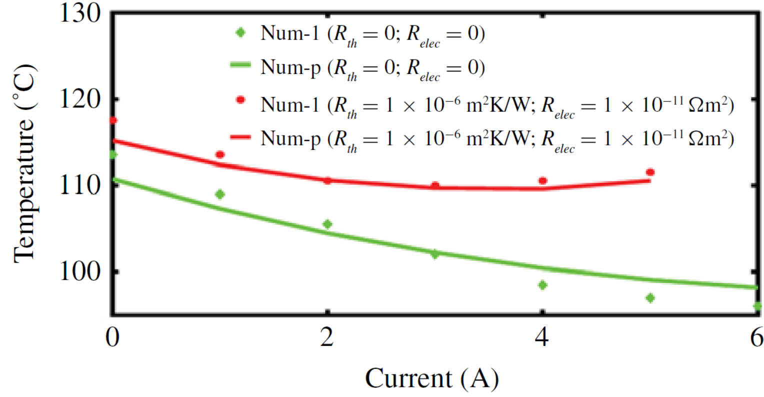


Figure 8: Validation of FLUENT model in Reference [11] against the numerical results from Reference [5]. 'Num-1' corresponds to the numerical results in Reference [5] and 'Num-p' corresponds to the simulation results in Reference [11].

k, of 1.2 W/m-K. These bulk properties are used instead of modeling the individual layers of the thermoelectric superlattice. Using these detailed specifications for the package and TEC, a FLUENT model is presented and validated in [11]. The chip size is 11 mm x 13 mm with a localized hot spot of 400μm x 400μm; a single TEC of area 3.5 mm x 3.5 mm is located 25 μm above the chip. A plot of the validation from Reference [11] is shown in Figure 8, with and without given electrical and thermal contact resistances taken into account. Results matched within 2-3°C and maximum cooling is achieved at current amplitude of 3A [11]. The validated model of the TEC module is then used for all modeling and simulations in this work.

A schematic of the electronic package including the TEC modules and heat sink, is shown in Figure 9(a). The results presented in Chapter 4 are based on this geometry of packaged TECs. The model consists of nine TEC modules, each 100 μm thick and comprised of 7x7 p-n couples. These modules are attached at the back side of the heat spreader. The area of each TEC device is 3mm x 3mm. The thickness of the superlattice material in a TEC device is 8 μm [5] and is sandwiched between two copper layers. The reference values of electrical/thermal contact resistance at the

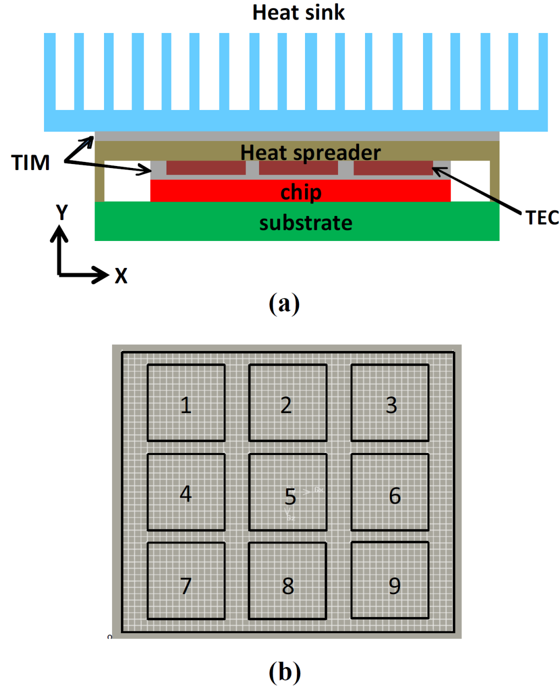


Figure 9: (a) Schematic of the electronic package. Heat Spreader, thermal interface material (TIM), chip, substrate and thermoelectric coolers (TECs) are shown. (b) Layout of the nine TECs and associated mesh in a 2D cross-section.

interface of superlattice-metal layer ($10^{-11}\Omega\text{m}^2$; $1*10^{-6}\text{m}^2\text{K/W}$) and of thermal contact resistance at the interface of TEC module-heat spreader layer ($8*10^{-6}\text{m}^2\text{K/W}$) are taken from Reference [5]. These values of contact resistances are considered in all simulations unless stated otherwise. Dimensions and thermal conductivity of different components of the electronic package and TEC module are listed in Table 1.

The computational domain of the FLUENT model presented in Chapter 4 includes heat spreader, thermal interface material (TIM), chip, and nine thermoelectric coolers (TECs). The layout of the nine TECs and associated mesh is shown in Figure 9(b). To reduce the computational time of the simulation, the heat sink is represented by a convective heat transfer boundary condition (h=2,050 W/m^2-K) at the top of the spreader surface. Nine high heat flux (1,000 W/cm^2) sources are located at the bottom surface of the chip (each with area 500 x 500 μm^2) to generate hot-spots at the corresponding locations. Each of the nine high heat flux sources lies at the center

Table 1: Thermal conductivity, k_{th}, and dimensions of different components of the electronic package.

Component	k_{th} **(W/m-K)**	**Dimensions**
Spreader	400	30mm x 1mm x 30mm
TIM	1.75	11mm x 0.125mm x 13mm
TEC-superlattice	1.2	3.0mm x 0.008mm x 3.0mm
Chip	140	11mm x 0.5mm x 13mm

of a TEC. The rest of the bottom surface of chip is considered as a heat source of uniform heat flux of 42.7 W/cm^2.

The operation of TECs is based on the interplay of Peltier cooling and Joule heating. Heat is absorbed at one side of the TEC module (cold-junction) and rejected at the other side of the module (hot-junction) when a TEC module is turned on. The Peltier cooling effect is incorporated by adding heat ($\sim$SIT$_h$) at the hot side and subtracting heat ($\sim$SIT$_c$) from the cold side of the superlattice structures. Here, T$_h$ and T$_c$ are the temperatures of the hot and cold junctions, respectively. The value of S is taken as 300μV/K based on the experimental measurement in Reference [5]. The volumetric heat generation inside the TE layer and at the interface of the superlattice/metal layer is considered by adding joule heating ($\sim$I^{2}R) terms at the corresponding layers and volumes. The thermal contact resistances at these interfaces are incorporated by adding an appropriate thermal resistance at the corresponding interfaces.

The simulations are performed using the finite volume method based commercial solver FLUENT. 250K cells are considered for the simulations; grid independence tests verify that these cells are sufficient for the further simulations. Temperature contours on the chip bottom surface of the electronic package with and without TECs are shown in Figure 10.

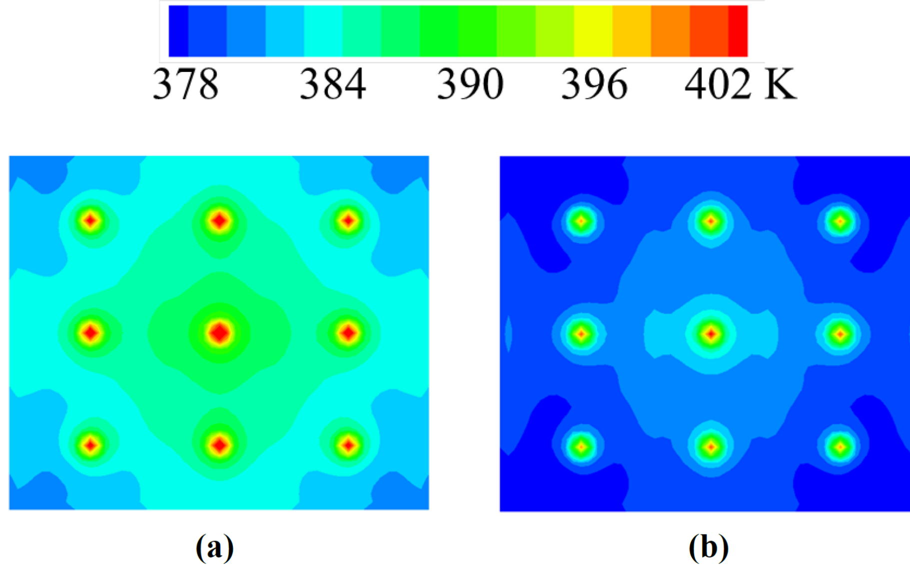


Figure 10: **(a)** Temperature contours on the bottom surface of the chip with no TECs turned on. High heat flux (1,000 W/cm^2) sources are located at nine symmetrical points of area 500 x 500μm^2 which generate hot-spots. The rest of the surface has a uniform heat flux of 42.7 W/cm^2. **(b)** Temperature contours on the bottom surface of the chip with TECs turned on at 1.5 amperes.

3.1.1 Governing Equations for Thermoelectric Coolers

The governing differential equation for heat distribution inside the electronic package is represented as,

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \dot{Q} = \frac{\partial T}{\alpha \partial t} \tag{5}$$

where

$$\dot{Q} = \begin{Bmatrix} \frac{I^2}{A^2 \sigma k} & \text{inside TEC} \\ 0 & \text{elsewhere} \end{Bmatrix} \tag{6}$$

Here, T is temperature, α is thermal diffusivity, I is current, A is the area of an element, σ is electrical conductivity, and k is thermal conductivity.

3.1.2 Boundary Conditions

A heat flux boundary condition is applied at the bottom of the chip, which can be expressed as:

$$-k\frac{\partial T}{\partial y} = q'' \text{ where } q'' = \begin{Bmatrix} 1,000W/cm^2 & \text{at the hot spot} \\ 42.7W/cm^2 & \text{elsewhere} \end{Bmatrix} \tag{7}$$

In addition, at the cold end of the TEC,

$$-kA\frac{\delta T}{\delta y}\Big|_{y=y_c^+} = \left[-kA\tfrac{\delta T}{\delta y} - SIT\right]_{y=y_c^-} + I^2R_{elec} \tag{8}$$

Here, the y coordinate is directed from TEC to the heat spreader, and y_c^+ and y_c^- are locations just above and below the cold junction, respectively. S is the Seebeck coefficient and R_{elec} is the contact electrical resistance. Also, at the hot end of the TEC,

$$-kA\frac{\delta T}{\delta y}\Big|_{y=y_h^+} = \left[-kA\tfrac{\delta T}{\delta y} - SIT\right]_{y=y_h^-} + I^2R_{elec} \tag{9}$$

where y_h^+ and y_h^- are locations just above and below the hot junction, respectively.

Finally, at the top surface of the heat spreader,

$$-k\frac{\delta T}{\delta y} = h(T - T_\infty) \tag{10}$$

where h is the convective heat transfer coefficient and T_∞ is the ambient air temperature, which is taken to be 300 K for all simulations.

3.1.3 Governing Equations for Thermoelectric Generators

All of the previous governing equations, boundary conditions, and geometric details of the packaged thermoelectric module are the same for the thermoelectric generators, except for the hot spot which is removed. Therefore the heat flux boundary condition on the bottom surface of the chip is given by:

$$-k\frac{\partial T}{\partial y} = q'' \text{ where } q'' = \begin{Bmatrix} 42.7W/cm^2 & \text{entire chip} \end{Bmatrix} \tag{11}$$

For thermoelectric coolers, the current is controlled by an external source. The details of the external source, its resistance, and corresponding joule heating are not considered in the TEC computational model. In thermoelectric generators, the current is determined by a combination of several factors: Seebeck coefficient, temperature difference across the poles, and the resistances of the TEG and load. The expression for the Seebeck voltage in thermoelectric generators is given by:

$$V = S(T_h - T_c) \tag{12}$$

where S is the Seebeck coefficient, T_h is the temperature of the hot junction, and T_c is the temperature of the cold junction. From the Seebeck voltage, it is simple to determine the current, as current is voltage divided by resistance:

$$I = \frac{V}{R} = \frac{S(T_h - T_c)}{R_L + R_{TEG}} \tag{13}$$

Here, R_L is the electrical load resistance, and R_{TEG} is the electrical resistance of the TEG device. The amount of useful work is the power dissipated through the load resistance, which can be estimated by the following expression:

$$W = I^2 R_L = \left[\frac{S(T_h - T_c)}{R_L + R_{TEG}}\right]^2 R_L \tag{14}$$

3.2 Compact Model Using SPICE

The multi-dimensional compact model of a TEC is developed using SPICE, which is validated and calibrated by the FLUENT model described in the previous section. A compact 1-D resistor model is first developed in SPICE for an isolated TEC subjected to heat flux on one side and convective cooling on the other side. A finite volume based model using FLUENT is also created for comparing to results of the 1-D resistor network model in SPICE. The 'one-dimensional' FLUENT model consists of the same layers and contact resistances inside the TEC module as the previous full TEC-package FLUENT model; however, the lateral area is reduced to the size of a single

TEC, 3mm x 3mm. It is essentially a 1-D model, where the vertical surfaces of the TEC module are insulated and there is no lateral thermal spreading, which is confirmed by observing the constant temperature distributions of several horizontal slices. This FLUENT model is used to validate the internal operation of the TEC module within the compact model.

The 1-D compact model of the TEC is built following the geometry of the 'one-dimensional' FLUENT model in order to ensure significant agreement between the two models. The compact model is constructed in SPICE and consists of a thermal resistor network that can be solved using circuit analysis techniques. The one-dimensional steady-state compact model can be seen in Figure 11 and consists of resistors, current sources, voltage sources, and voltage controlled current sources. The resistors simulate each material, convection, and any thermal contact resistances that exist inside the TEC FLUENT model. No spreading resistance is included at the TEC-spreader interface because the model is being validated against a FLUENT model whose heat spreader is of the same area as the chip and TEC below. The current sources simulate the chip heat flux at the bottom surface (iHeatFlux) as well as electrical heat generation that occurs in the TEC due to a current being passed through the device(ihgCu1, ihgTEC, ihgCu2, and ihgCu2Spr). The voltage controlled current sources or G-elements simulate the cooling effects of the TEC by removing heat at the cold surface (gTECcold) and adding heat at the hot surface (gTEChot), depending on the temperature difference between the two sides. The last element is the voltage source at the top of Figure 11, ($V=T_{amb}=300K$), which sets the ambient temperature at 300K. Both ends of the model are connected to ground as this allows exact control of the boundary conditions. All elements of the compact model shown in Figure 11 are outlined in Table 2 with descriptions of their function within the model.

The thermal resistance values for each conduction and convection element are

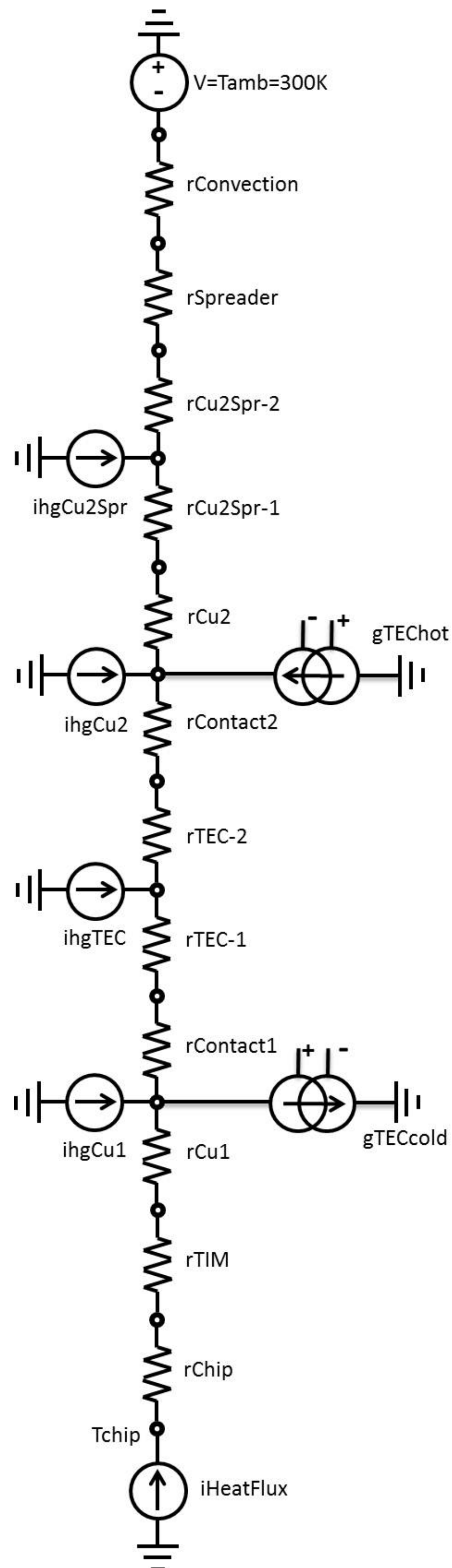


Figure 11: One-dimensional steady-state compact model of the thermoelectric cooler integrated inside package.

Table 2: Summary of elements in 1-D compact model.

Element Name	Function
V=Tamb=300K	voltage source representing ambient temperature
rConvection	thermal convection resistance at top of heat spreader
rSpreader	thermal resistance of spreader material
rCu2Spr-2	contact resistance layer of TEC-spreader interface
ihgCu2Spr	heat dissipation within copper-spreader interface
rCu2Spr-1	contact resistance layer of TEC-spreader interface
rCu2	top copper layer of TEC device
ihgCu2	current source representing electrical contact resistance between copper and Bi_2Te_3 superlattice
gTEChot	adds heat to top of superlattice layer α SIT_hot
rContact2	top thermal contact resistance between copper and Bi_2Te_3 superlattice
rTEC-2	superlattice layer of TEC device
ihgTEC	heat dissipation within TEC device
rTEC-1	superlattice layer of TEC device
rContact1	bottom thermal contact resistance between copper and Bi_2Te_3 superlattice
ihgCu1	current source representing electrical contact resistance between copper and Bi_2Te_3 superlattice
gTECcold	removes heat from bottom of superlattice layer α SIT_cold
rCu1	bottom copper layer of TEC device
rTIM	thermal resistance of thermal interface material between chip and TEC device
rChip	thermal resistance of silicon chip material
Tchip	temperature of bottom of silicon chip
iHeatFlux	power source at bottom of chip

calculated using Equation 15:

$$R_{conduction} = \frac{L}{kA}; \text{ and } R_{convection} = \frac{1}{hA} \tag{15}$$

where L is the thickness of the material, k is the thermal conductivity of the material, A is the cross-sectional area of the element, and h is the convective heat transfer coefficient. When the model is converted to a transient model, thermal capacitance is included for each material layer, which consists of a capacitor with a capacitance, C, calculated by Equation 16:

$$C = \rho c_p \tag{16}$$

where ρ is the density of the material and c_p is the specific heat of the material. The units of resistance and capacitance are [K/W] and [J/m^3-K], respectively.

The 1-D compact model of the TEC device is integrated into a full chip electronic package model for further simulations. The electronic package in SPICE has parameters similar to the FLUENT model. The package has a 9mm x 9mm chip with one 3mm x 3mm TEC device placed at the center. A heat flux boundary condition (~427,000 W/m^2) is applied at the bottom surface of the chip; the total chip power is approximately 35 W. The thickness of the heat spreader, thermal interface material (TIM), and chip, are considered as 1mm, 0.125mm, and 0.5mm, respectively. Each material layer has resistors in all three-dimensions connected in a 3-D mesh to form a multi-dimensional resistor network. The multi-dimensional network is capable of simulating the effects of spreading in the heat spreader, so no additional spreading resistance is required at the TEC-spreader interface. The resistor-capacitor configuration of a single cell in the chip package is shown in Figure 12. The chip package is built using thousands of these cells in a mesh resistor network, each belonging to one of the three package materials: silicon for the chip, thermal interface material for the chip-spreader interface, or copper for the heat spreader. The TEC compact model is inserted within the chip package model as a sub-circuit consisting of the resistor

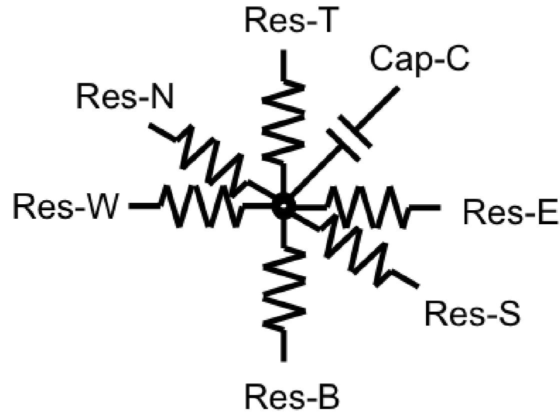


Figure 12: Resistor-capacitor network for a single cell of chip or electronic package (∼chip, TIM, or heat spreader). Abbreviations stand for North (N), South (S), East (E), West(W), Top (T), Bottom (B), and Center (C).

network from rCu1 to rCu2 in Figure 11, and each instance of the TEC only needs two nodes to connect to the package model. The model is adaptable to changes in grid size, and a grid-independence test was completed. It was observed that 0.5mm x 0.5mm lateral gridding was sufficient for further simulations.

The package model consists of many vertical 1-D resistor networks connected in a 2-D array in order to create a 3-D package. Hence, the package geometry is a prism with horizontal area of 9 x 9 mm^2 and the heat spreader is the same area as the chip itself, so the model lacks the effect of a larger heat spreader. Initially, the top of the model was given a heat transfer convection coefficient of 13,000 W/m^2-K and was compared to the same TEC-package model built in FLUENT for finite-volume method based simulations. The results were similar and led to the next step of adding a larger heat spreader.

After validation of the prism geometry, equivalent resistors were added to the sides of the heat spreader to simulate convection and spreading that would occur if a larger heat spreader were present. The simulated heat spreader size is 23mm x 23mm, which is sized according to the geometry specified in Reference [11]. Each side of the spreader is assumed to have a straight rectangular fin extending out, and the

equivalent resistance, R_{fin}, is found using equations 17-19 [16].

$$R_{fin} = \frac{1}{hA_f\eta_f} \tag{17}$$

$$\eta_f = \frac{tanh(mL_c)}{mL_c} \tag{18}$$

$$m = \sqrt{\frac{hP}{kA_c}} \tag{19}$$

The equivalent resistance of the fin, R_{fin} (equation 17) is a function of h, A_f, and η_f, where h is the convection heat transfer coefficient, A_f is the surface area of the fin, and η_f is the fin efficiency defined by equation 18. The fin efficiency, η_f, is a function of L_c and m, where L_c is the characteristic length and m is defined by equation 19. m is a function of h, P, k, and A_c, where P is the perimeter of the fin, k is the conductivity of the fin material, and A_c is the cross-sectional area of the fin. The equivalent resistance values of the fins need to be calibrated against the results from the FLUENT model, i.e., a multiplier is needed to correct R_{fin} since the FLUENT model considers convection on only one side of the fins, whereas the equivalent resistance model considers both sides of the fins. In addition, the equivalent resistances added to the compact model only consider fins projecting straight from the four sides of the spreader and do not model the corner areas of the heat spreader. The compact model is in good agreement with the FLUENT results for both steady-state and transient simulations if the resistance of the fin is multiplied by a derived constant (∼multiplier), which varies with the equivalent size of the heat spreader. These multipliers varied from 1 to 0.4; the limits correspond to a heat spreader of the same size as the chip and to a very large heat spreader respectively. The multiplier appears to saturate to 0.4 at large heat spreader size as further increase in heat spreader size does not lead to any additional effective cooling of the system. For the

heat spreader of size 23 mm x 23 mm, a multiplier of 0.615 gave very close results to the FLUENT model.

CHAPTER IV

ARRAY OF THERMOELECTRIC COOLERS

4.1 Effect of Conductive Coupling Among Multiple TECs

Hot spot locations may be known to the chip's designers for some electronic packages or hot spots may appear randomly across a large area of a chip. In either case, an array of thermoelectric coolers may be needed to manage the temperature profile on-chip. In this section the simultaneous operation of multiple TECs are analyzed in steady-state, and the effect of conductive coupling among active TECs in cooling multiple hot spots on the chip is investigated. Multiple TECs could potentially provide improved cooling and better thermal management on-chip. Steady-state analysis is followed by the transient analysis of cooling multiple hot spots using pulsed currents in TECs. Transient pulses through thermoelectric coolers can provide additional cooling over that provided by optimum steady-state current.

4.1.1 Steady-state Analysis

The primary purpose of developing a model with nine hotspots and TECs is to investigate the conductive coupling between TECs and examine the advantages or disadvantages of having multiple TECs inside a package. Simulations were performed for four different cases to investigate the effects of nine TECs (Figure 9) on steady-state cooling of hot spots. Hot spots with high heat flux sources (1,000 W/cm^2) are turned on at specific locations on-chip while a uniform low heat flux (42.7 W/cm^2) is applied to the rest of the chip. In case 1, only one hot spot at the center and corresponding TEC (at location 5 in Fig. 9b) are turned on. In case 2, two adjacent hot spots and corresponding TECs (locations 5 and 6) are turned on. In case 3, five hot spots and corresponding TECs (locations 2, 4, 5, 6, and 8) are turned on. In case 4, all nine hot

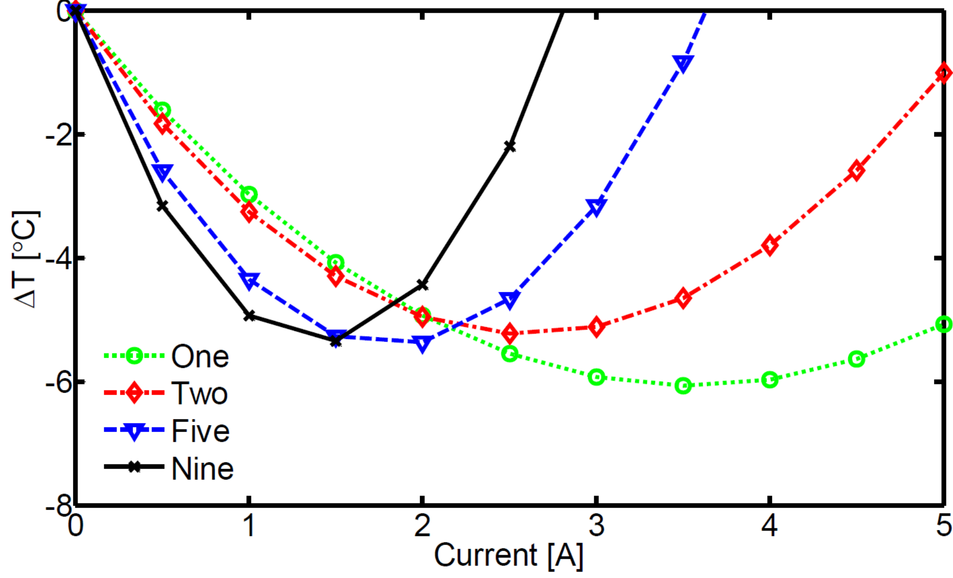


Figure 13: Temperature change at the center hot spot (ΔT) for various configurations of active hot spots and TECs: (1) Only center hot spot active, (2) Hot spots 5 and 6 active, (3) Hot spots 2, 4, 5, 6, and 8 active, (4) All nine hot spots active.

spots and TECs are turned on. Case 1 tests the cooling of a single hot spot on the chip whereas cases 2, 3, and 4, test the conductive coupling of active TECs located next to each other in different arrangements. The temperature change at the center hot spot (ΔT) for these various cases is shown in Figure 13. Two important features of the conductive coupling between TECs can be observed: (i) the maximum cooling (ΔT_{max}) occurs at higher amplitude currents when fewer hot spots and TECs are turned on or active, and (ii) ΔT_{max} is better for a single TEC and hotspot than the other cases which have multiple hot spots and TECs. The maximum cooling for case 1 is 6°C at a current of 3.5 amperes ($\sim$ optimum current). Case 2, corresponding to the adjacent positioning of a second active TEC, has relatively similar cooling behavior with the maximum cooling of 5°C occurring at 2.5 amperes current. When five hot spots and TECs are turned on, the maximum cooling of 5.4°C occurs at 2 amperes. For case 4, where all nine hot spots and all nine TECs are turned on, the maximum cooling occurred at 1.5 amperes with 5.3°C of cooling. As the number of hot spots increases from one to nine, ΔT_{max} decreases; however, the decrease in ΔT_{max} is very

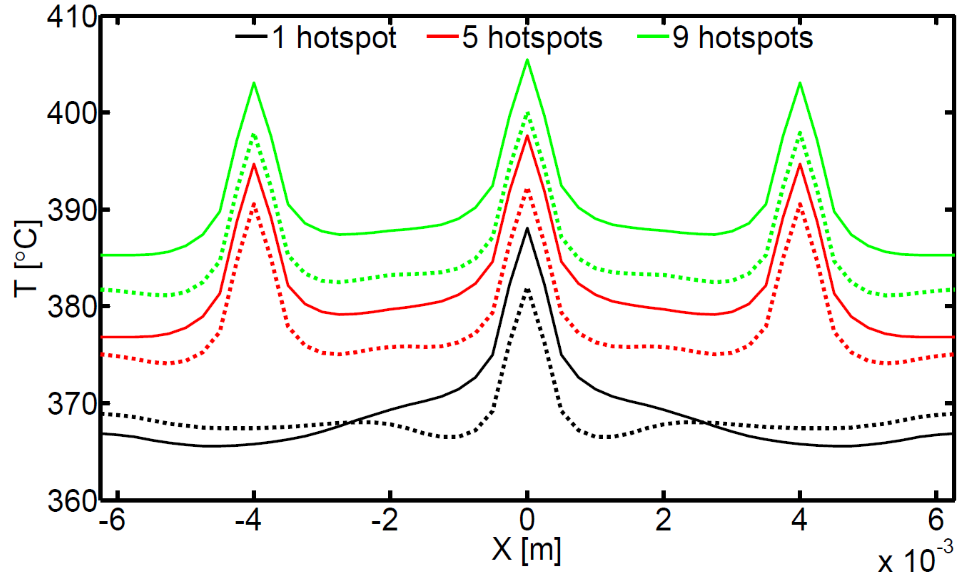


Figure 14: Centerline temperatures for 1, 5, and 9 hotspots turned on; solid line is with no TECs turned on and dashed line is with associated TECs turned on with best steady-state current.

small as it varies by only 1°C.

It is important to understand the behavior in Figure 13 due to the conducting coupling of active TECs. The temperature along the centerline of the bottom of the chip for one active TEC (Case-1), five active TECs (Case-3), and nine active TECs (Case-4) are shown in Figure 14, with and without associated TECs turned on at each configuration's best current. As seen in Figure 14, more hotspots result in higher temperatures across the chip, but the TECs are capable of lowering temperatures uniformly across the chip. The temperature gradients across the chip are very high, however, even with active TECs. This suggests that smaller size TECs may be better to cool localized hot spots and simultaneously mitigate the temperature gradient across the chip. The total heat passing through the cold side of the center TEC (Q_{in} [watts]) and the maximum cooling (°C) at center hot spot location for 1, 5, and 9 active hotspots and active TECs are shown in Figure 15. Turning on an additional hot spot leads to a 2.5 W increase in the chip total power dissipation. The Q_{in} through the center TEC decreases from 9.6 W to 7.4 W from the case of one active

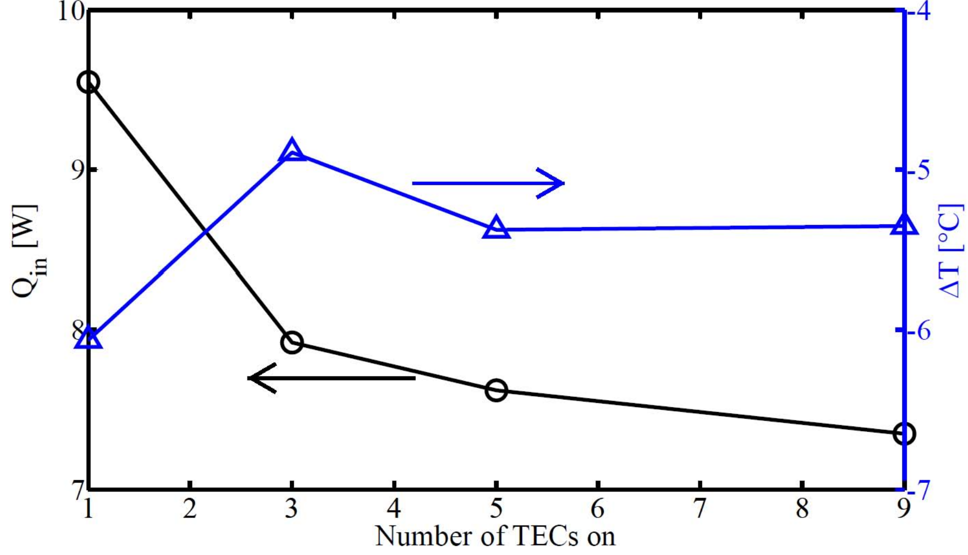


Figure 15: Heat passing through the cold side of the center TEC (Q_{in} in watts) and maximum cooling (°C) at the center hot spot when 1, 3, 5, or 9 hotspots with corresponding TECs turned on with best steady-state current (see Fig. 13 for best currents).

hot spot to nine active hot spots, and ΔT_{max} also decreases from 6°C to 5.3°C. This 23% decrease in Q_{in} suggests that once adjacent TECs are active, they pump out heat from the chip and decrease the cooling load ($\sim Q_{in}$) placed on the center TEC.

Figure 16 shows the temperature distributions, 10μm below the chip-TIM interface, when only the center hotspots and center TEC are turned on at 2 amperes (Fig. 16(a)) and when center hotspots, center TEC, and two adjacent TECs are turned on at 2 amperes (Fig. 16(b)). The temperature contours clearly show that active TECs adjacent to the center TEC create a large temperature gradient (~10°C) and pull heat from the center, as shown by the arrows in Figure 16. Simulations with active hot spots adjacent to the center hot spot but adjacent TECs in off state are performed. It has been observed that in this case ΔT_{max} increases with an increasing number of hot spots or increasing power on the chip, but when adjacent TECs are also active, ΔT_{max} decreases. The decline in cooling at the center hot spot could be due to the additional Joule heating when TECs adjacent to the center TEC become active. The Joule heating from adjacent TECs also leads to a decrease in the best

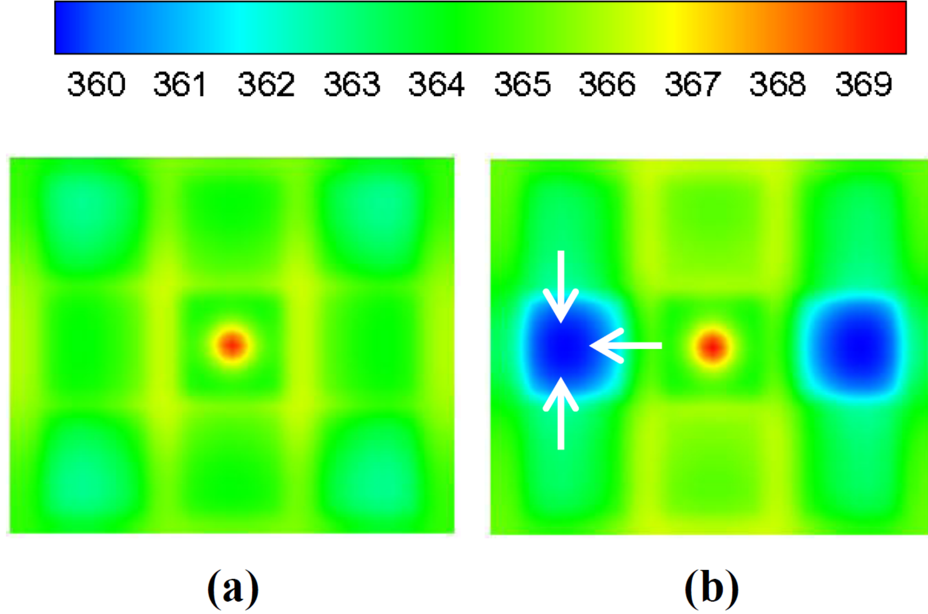


Figure 16: Temperature contours in a horizontal cross-section of chip at 10 μm below the chip-TIM interface when only center hotspot is active. **(a)** center TEC turned on at 2 amperes, and **(b)** center and two adjacent TECs turned on at 2 amperes; arrow shows heat flow direction due to the active TEC at left side.

current for the center TEC (Fig. 13). However, the overall effect is optimistic since even at lower selected currents, the decrease in ΔT_{max} is minimal, suggesting that multiple TECs can be employed for localized cooling. The conductive coupling between TECs can be very strong, especially when Joule heating in one TEC device can significantly affect the operation of adjacent TECs. Careful design and control is required for energy efficient operation of such multiple TECs.

4.1.2 Transient Analysis

Transient current pulses through the TECs can lead to additional cooling above Peltier cooling achieved in steady-state operation [27, 40, 42]. The additional cooling can be helpful in mitigating rapid hot spots and can allow the chip to run at full speed longer before slowing down. Selection of these current pulses can lead to efficient on-demand cooling of hot spots in microelectronic chips. It is important to analyze the effects of conductive coupling of TECs on transient operation since

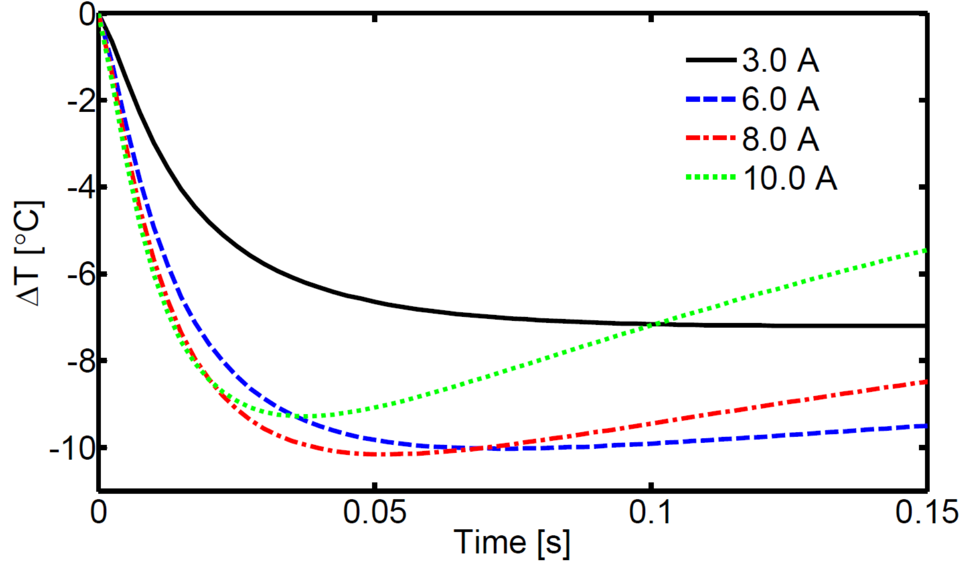


Figure 17: Transient analysis of center hot spot; center TEC turned on with 3.0 A, 6.0 A, 8.0 A, and 10.0 A current.

these effects may be significantly different from the steady-state results due to the large variation in thermal capacitances of the different materials inside an electronic package. Figure 17 shows the results of a transient analysis with the center hotspot turned on until steady-state is reached and then the corresponding TEC is turned on with a step current pulse of amplitude in the range of 3.0-10.0 amperes. The results corresponding to 3.0 amperes show that the temperature is monotonically decreasing and ΔT is approaching the steady-state values after 0.1 seconds. Higher amplitude pulse current through the TEC results in higher ΔT, but for higher amplitude current pulses the cooling disappears with time as the effect of Joule heating in each TEC is realized at the center hotspot. As seen for the case of 10.0 amperes applied current, the cooling is approximately 9.0°C at 0.03 seconds, but the cooling decreases to 7°C by 0.1 seconds, which is worse than the corresponding cooling 3.0 amperes applied current. The best transient cooling occurred for a current of 8.0 amperes and duration of 0.05 seconds. These results were used as the guidelines for the study of the effect of current pulse shapes in the next section.

The 8.0 A current is selected for the analysis of the effect of varying the number

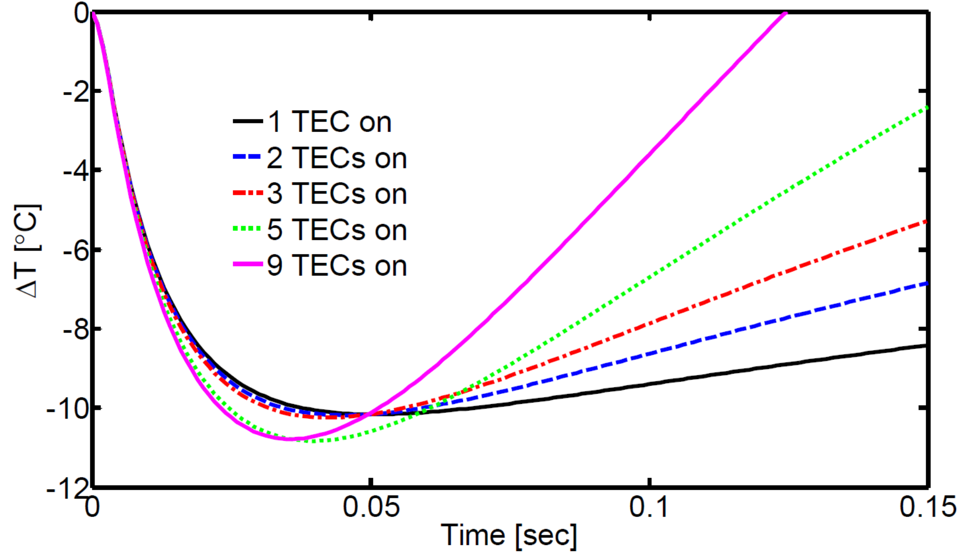


Figure 18: Transient analysis of center hotspot with 8.0 A current for various number of hotspots and active TECs. Hotspots are turned on for active TECs.

of active hotspots and TECs from one to nine. The transient temperature change (ΔT) of the center hotspot is presented in Figure 18. The maximum ΔT (ΔT_{max}) and time to reach maximum ΔT_{max} is similar for the cases of one, two, or three hot spots and active TECs at the corresponding locations. The ΔT_{max} increases by approximately 1°C at the center hot spot as the number of TECs and hotspots increase to nine and the time to reach ΔT_{max} decreases from approximately 0.05 seconds to 0.03 seconds. This analysis shows that the transient coupling between TECs is much weaker than the steady-state coupling. However, it should be noticed that the trajectory of temperature rise at hot spot location is very different for these different cases of active TECs after reaching ΔT_{max}. This means that adjacent TEC activity should be taken into consideration for control schemes, since coupling effects can be strong between active and inactive TECs. Some of these effects can be observed in subsection 4.2.2 for random hot spot temperature control.

4.1.3 Pulse Shape and Duration

Shape of the current pulse can significantly affect the maximum cooling, energy consumption, and post-pulse behavior at the hot spot location. In this section, various pulse shapes were investigated to analyze and compare them for hot spot temperature management. The best pulse obtained from the analysis will be used to study temperature control in the next section. The pulses under investigation are a step pulse (t^0) of constant amplitude of 8 amperes and pulses whose magnitude increases from 0 amperes to 8 amperes along linear (t), square root ($t^{1/2}$), and parabolic paths (t^2) [27]. Figure 19 shows the pulse shapes used in the transient simulations. In a real application of TECs, formation of these pulse shapes would be difficult to achieve through the associated circuits, but the perfect shapes are used for the sake of simplicity in the modeling. For the study of transient pulse simulations, only the center hot spot is turned on and different pulses are applied to the corresponding center TEC only (location 5 in Figure 9(b)). The system is first allowed to reach steady-state with the hot spot turned on and no current passing through the TEC. After reaching steady-state, current pulses of different shapes were applied to the TEC. The transient change in hot spot temperature corresponding to different pulses is presented in Figure 20. The best cooling at the hot spot is obtained by using a square root pulse ($\sim \Delta T_{max}$=10.4°C). A similar degree of cooling (ΔT_{max}=10.2°) is also obtained by using step pulse or constant amplitude pulse, but the temperature overshoot after turning off the step pulse is higher compared to the other pulses; this pulse consumes maximum energy (see next section) even though it leads to fastest cooling over the period of the pulse (Fig. 20). Linear and parabolic pulses cool the hot spot by 9.6°C and 8.1°C, respectively.

A subsequent study is performed to investigate the effect of the pulse period. The best pulse shape is selected from the previous analysis, i.e. square root shaped pulse with maximum amplitude of 8 amperes. The time length or period of the pulse is

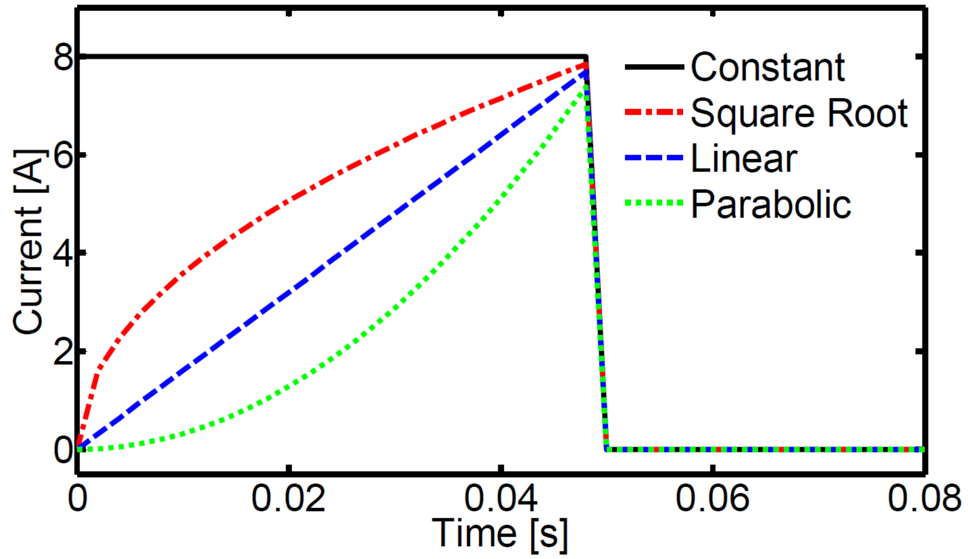


Figure 19: Pulse shapes used in transient analysis include constant, linear, square root, and parabolic.

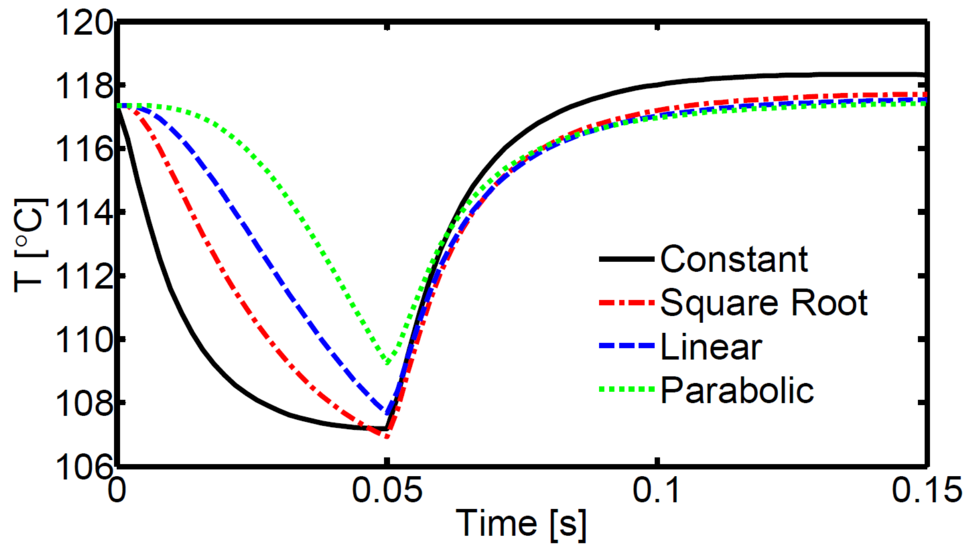


Figure 20: Hot spot 5 turned on with a high heat flux of 1,000 W/cm^2 and allowed to reach steady-state. Center TEC turns on with various pulses: constant, linear, root, and parabolic.

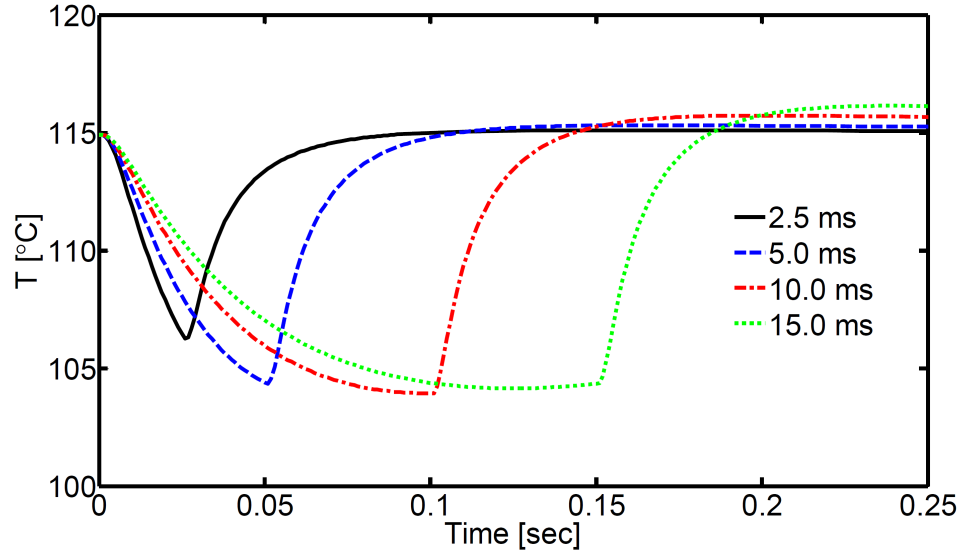


Figure 21: Hot spot 5 turned on with a high heat flux of 1,000 W/cm^2 and allowed to reach steady-state. Center TEC turns on with square root pulse of various periods: 2.5 ms, 5.0 ms, 10.0 ms, 15.0 ms.

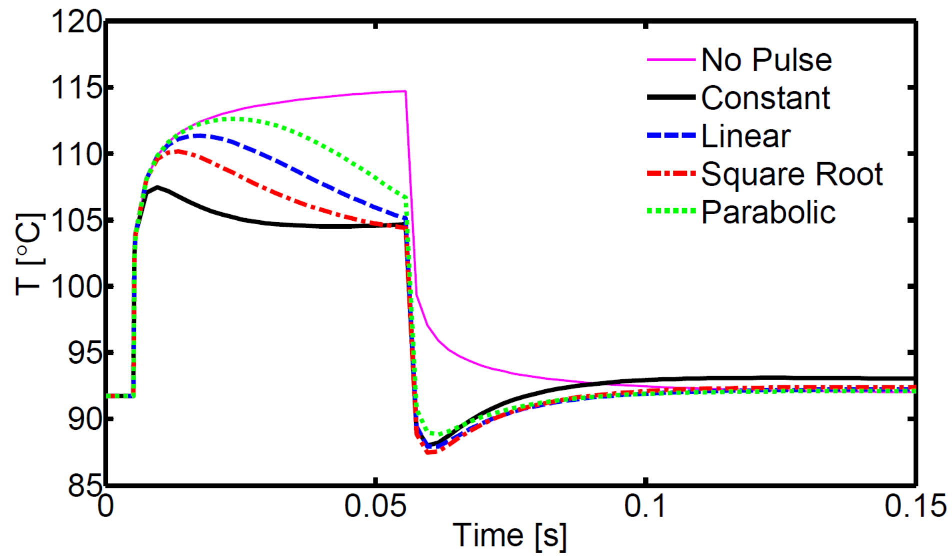
varied in the range of 2.5 ms to 15 ms. Similar to the previous analysis, the chip is allowed to first reach steady-state with the center hot spot turned on, and the TEC is then turned on with the square root pulses of various time lengths. The maximum hot spot cooling by the center TEC increases up to the 10 ms pulse and then begins to decrease for longer pulses (Fig. 21) . This suggests that there is an optimal pulse length corresponding to maximum cooling for any shape of pulse of given maximum amplitude. This analysis provides a very important suggestion about the hot spot cooling, i.e., if transient cooling for a longer time is required, then longer duration pulses of same maximum amplitude can help, but with a compromise in maximum degree of cooling at the hot spot. The longer duration pulse can provide extended cooling, but the temperature increases rapidly once the pulse is turned off, leading to larger temperature overshoot with increasing pulse period.

4.2 Temperature Control and Energy Analysis

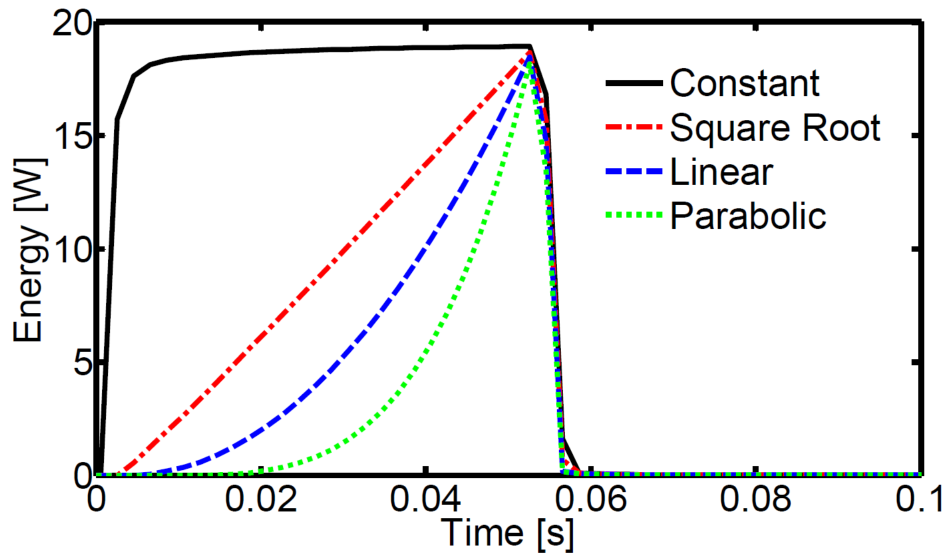
In a microelectronic package, the TEC can be activated based on a threshold temperature sensed on the chip. Temperature control with TECs can provide active cooling when and where needed, greatly increasing the cooling efficiency of hot spots. Traditional cooling methods cool the entire chip. Cooling of hot spots therefore require cooling the entire chip with traditional methods, which is much less efficient than localized cooling technologies, such as TECs. In this section, a single hot spot control and random hot spot control by TECs are analyzed once hot spot temperatures cross a specified temperature threshold. Pulse shapes analyzed in the previous sections are further used for hot spot temperature control and investigation of energy consumption during the TEC operation.

4.2.1 Temperature Control of Single Hot Spot

Each pulse shape has different cooling behavior and thus a metric is required for comparing different pulse shapes used for removing a transient heat flux. Energy consumption coupled with the degree of cooling at a hot spot for different pulses can provide an elementary set of guidelines to judge the application of an appropriate pulse to a TEC. In addition, some important factors need to be considered to select an appropriate pulse, such as the maximum temperature overshoot after the pulse is turned off and the time the system takes to reach steady-state again. The next set of simulations evaluate the pulse shapes from the previous section using the important parameters discussed above. The system is first allowed to reach steady-state with no hot spots turned on and no TECs turned on. The center hot spot is then turned on and once the temperature of the hot spot reaches a pre-selected threshold of 102°C, the corresponding TEC is turned on using the pulses shown in Figure 19. The pulse duration is considered the same as the lifetime of the transient heat flux, i.e., 0.05 seconds. Among the four current pulses, the constant pulse provides the fastest



(a)



(b)

Figure 22: Hot spot 5 turns on with a high heat flux of 1,000 W/cm^2 and center TEC turns on at 102° with various pulse shapes: constant, linear, root, and parabolic. **(a)**Real temperatures of simulation, **(b)** Energy consumed over time.

Table 3: Total energy expended for cooling of hot spot using four pulse shapes: (1) constant, (2) linear, (3) square root, and (4) parabolic.

Pulse Shape	Total Energy Expended (Joules)
Constant	204.9 (100%)
Linear	70.8 (34.6%)
Square Root	103.2 (50.4%)
Parabolic	45.1 (22.0%)

cooling of 10°C, shown in Figure 22(a). In this figure, degree of cooling is estimated at the end of the pulsed operation with a reference to the peak temperature (∼115°C) in the absence of any pulsed current through the TEC (shown in Figure 22(a) as 'No Pulse'). The square root pulse responds more slowly than the constant pulse but gives the best cooling of 10.5°C. The linear and parabolic pulses provide slower cooling than the constant and square root pulses with cooling of 9.9°C and 8.6°C, respectively.

Analysis of total energy consumed during the pulsed TEC operation can be used to determine which pulse is most energy efficient. Figure 22(b) shows the energy consumed over time, which is then integrated to find the total energy consumed for each pulse as shown in Table 3. The constant pulse consumes 204.9 joules, approximately twice the energy required by the square root pulse, which uses 103.2 joules. The linear and parabolic pulses use 70.8 joules and 45.1 joules, respectively. Even though the parabolic shaped pulse is best from the energy perspective, it is slowest in response and less effective in controlling the temperature of the hot spot. The square root pulse is the winner here as it has the same degree of cooling but at half the energy expense of the constant pulse.

Other factors which need to be considered include highest temperature, maximum temperature overshoot after the pulse is turned off, and the time the system takes to reach steady-state. These statistics are compared for each pulse in Figure 23. The pulses are displayed as follows: (1) Constant, (2) Square Root, (3) Linear, and (4)

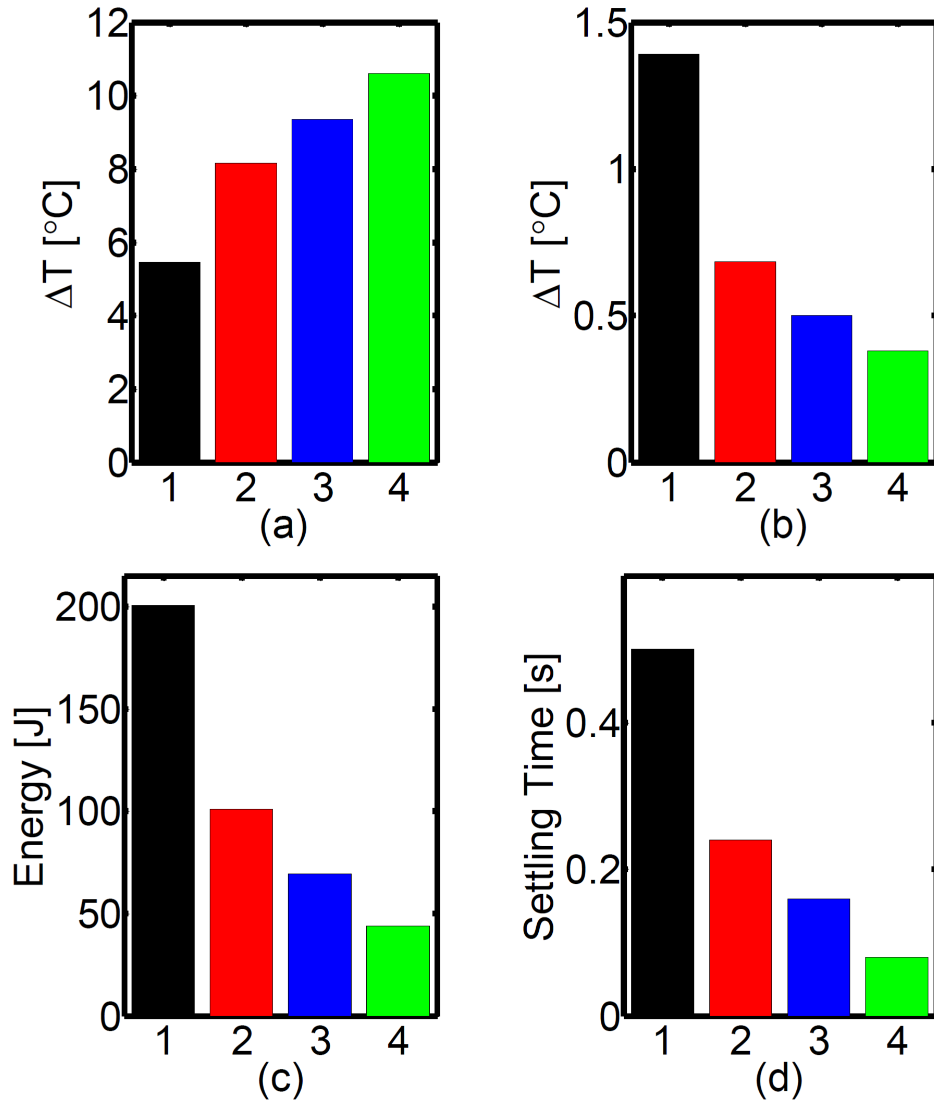
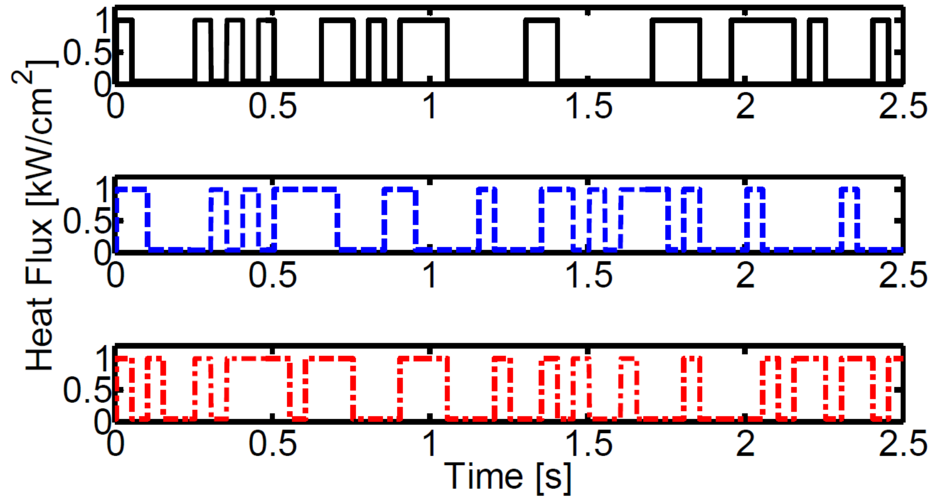


Figure 23: Comparison of the four pulses: (1) Constant, (2) Square Root, (3) Linear, and (4) Parabolic, using four parameters important to select a pulse. **(a)** Difference between maximum temperature and threshold temperature (102°), **(b)** Temperature overshoot after pulse is turned off, **(c)** Total energy expended during pulsed operation, and **(d)** Settling time for temperature within 0.5° of steady-state.

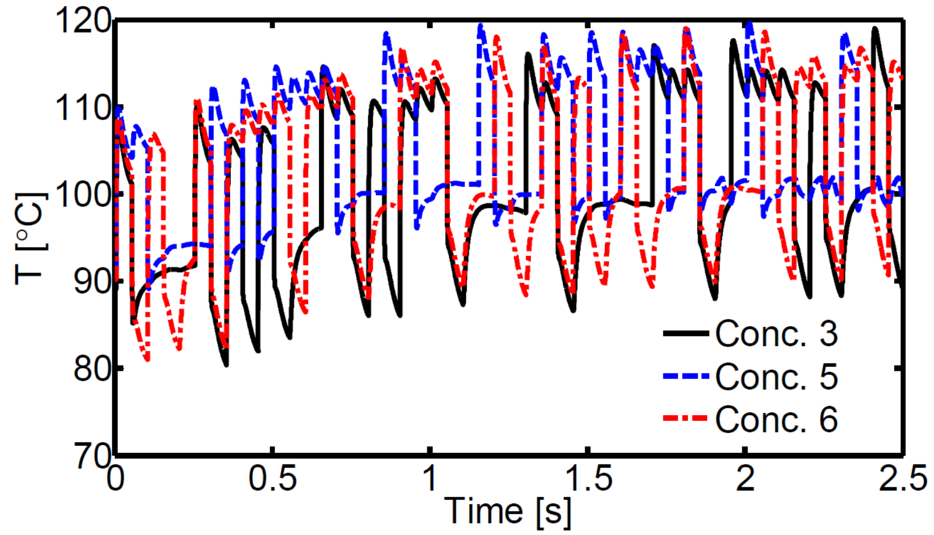
Parabolic. Figure 23(a) shows the difference (ΔT) between the maximum temperature and the threshold temperature (∼102°C) that triggers the pulse, where smaller ΔT values are better. The constant pulse has the best ΔT of 5.7 °C followed by the square root pulse with ΔT of 8.1°C. The linear and parabolic pulses have ΔT's of 9.3°C and 10.6°C, respectively. Figure 23(b) shows the temperature overshoot (ΔT_{sh}), which is defined as the difference between the maximum temperature after the pulse and hot spot are turned off and the steady-state temperature. The parabolic pulse has the best overshoot with 0.4°C, followed by the linear pulse at 0.5°C. The square root pulse and constant pulse have a ΔT_{sh} of 0.7°C and 1.4°C, respectively. Figure 23(c) compares the total energy consumed during pulsed operation, shown in Table 3. Figure 23(d) shows the settling time for each pulse, which is defined as the time it takes for the hot spot temperature to fall within 0.5 degrees of the steady-state temperature after the pulse and hot spot are turned off. Settling time provides a metric to quantify the duration of adverse Joule heating effects after a current pulse is switched off. The constant pulse takes the longest settling time of 0.5 seconds. The square root pulse is second longest at 0.25 seconds, but it takes considerably less time than the constant pulse. The linear pulse and parabolic pulse are the best with times of 0.16 and 0.08 seconds, respectively. Comparing pulses based on the combination of these four factors suggests that the square root pulse is the best pulse of all pulse shapes tested; it is used for further testing the system with random hot spots.

4.2.2 Temperature Control of Random Hot Spots

Location of hot spots on-chip can vary with time. Multiple TECs integrated inside an electronic package should be able to manage high heat fluxes originating from these hot spots according to their spatiotemporal variation by providing localized active cooling. The following study implements a simple maximum temperature control, which turns on the corresponding TECs as soon as the hot spot's temperature reaches



(a)



(b)

Figure 24: **(a)** Random cycling of hot spots 3, 5, and 6, respectively **(b)** Transient temperature at hot spots when TECs turn on with square root pulse at hot spot temperature > 102 °C during random cycling of hot spots.

a pre-set threshold temperature, as in the previous section. To test the control of random hot spot temperatures by TECs, a simulation is performed with three hot spots: hot spots at locations 3, 5, and 6 in Figure 9(b), which turn on randomly in 0.05 second periods. Once the hot spot reaches 102°C, the TEC corresponding to the hot spots is turned on with a square root pulse of amplitude 8 amperes and duration of 0.05 seconds. After 0.05 seconds TECs are switched to inactive mode ($\sim$ no current through TECs).

Figure 24(a) shows the random cycling of the hot spots, and Figure 24(b) shows the temperatures of the hot spots. The square root pulse is capable of cooling the chip below the control temperature with no active TEC for the first 0.75 seconds, but transient cooling with the TEC is no longer effective after this point. The Joule heating in the TECs continues to heat the entire chip, and thus over long periods of time, the temperature continues to rise. By the end of the 2.5 second simulation, temperature on the chip appears to have approached a steady periodic temperature but is approximately 3-4°C higher than the temperature with no TEC cooling. Therefore, transient cooling with high amplitude current pulses is effective for infrequent, short period hot spots, but for frequent hot spots, current values closer to steady-state ($\sim$3A instead of 8A) should be utilized to provide cooling without the degradation over time seen in Figure 24(b). The present analysis of temperature control of random hot spots is a sample case study to observe the behavior of an electronic package with random hot spots under pulsed TEC operation. In addition to the thermal behavior of the surroundings, the intensity of heat flux and transient temperature rise at hot spot locations need to be appropriately considered for energy efficient control of hot spots by TECs. Further investigation needs to be performed to determine better dynamic control techniques for managing multiple hot spots.

4.3 Summary of Results

The array of nine TECs provided important results related to thermal coupling of adjacent TECs and transient pulse operation of TECs. Coupling among TECs during transient operation is weak, but the coupling is more significant during steady-state operation. From the analysis of pulse shapes, the square root pulse is observed to provide the best cooling considering all the important parameters: maximum cooling, temperature overshoot after current pulse is turned off, total energy expended, and settling time. Preliminary control results for random hot spots, using the square root pulse, show that frequent hot spots should be cooled with steady-state currents whereas infrequent hot spots may be able to better utilize transient pulses.

CHAPTER V

COMPACT MODEL OF THERMOELECTRIC COOLERS

A compact model can facilitate faster modeling of a system with only a small increase in the error compared to the detailed simulation. A compact model therefore allows analysis of parameters in a large range and makes multi-parameter optimization of a system possible, since the time for each simulation is drastically shorter than the time for each simulation using detailed model such as FLUENT model described and utilized in the previous chapter. The compact model of the thermoelectric cooler is built in SPICE, an analog electronic circuit simulator, which also allows for the possibility of integration of the thermal model with an electrical circuit model of TEC controllers.

5.1 Validation of Compact Model

The 1-D compact model of the thermoelectric cooler is validated against the 1-D FLUENT model for both steady-state and transient behavior. All elements in the compact model have an area of 3mm x 3mm area, which is the same as the TEC area used in the FLUENT model. The steady-state validation of the compact model against the finite-volume model can be seen in Figure 25. Temperatures at the bottom of chip, bottom of TEC superlattice, and top of TEC superlattice are compared. The results are very comparable and follow similar trends. Figure 26 shows the relative error in percentage. The error grows as the current is increased, but the error fell below 2% for the range of the current amplitudes that will be considered within this work and for the typical TEC operation. This means that the compact model is capable of providing results very similar to the finite-volume method.

The 1-D model is then validated for the transient behavior. The comparison of

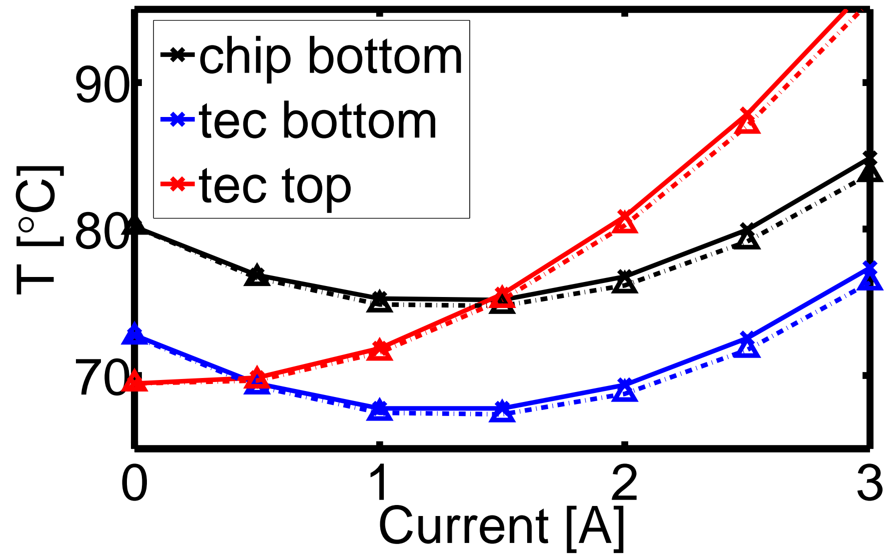


Figure 25: Steady-state validation of the 1-D compact model (dashed lines) against the 1-D finite volume model (solid lines) with varying current. Temperatures at bottom of chip, bottom of TEC superlattice, and top of TEC superlattice are compared.

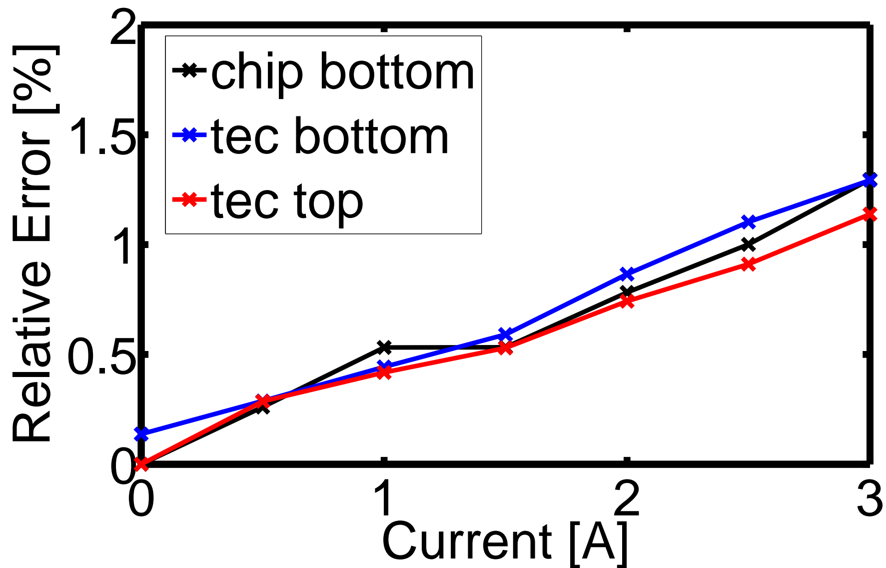


Figure 26: Relative steady-state error between the 1-D finite-volume model and 1-D compact model for various currents.

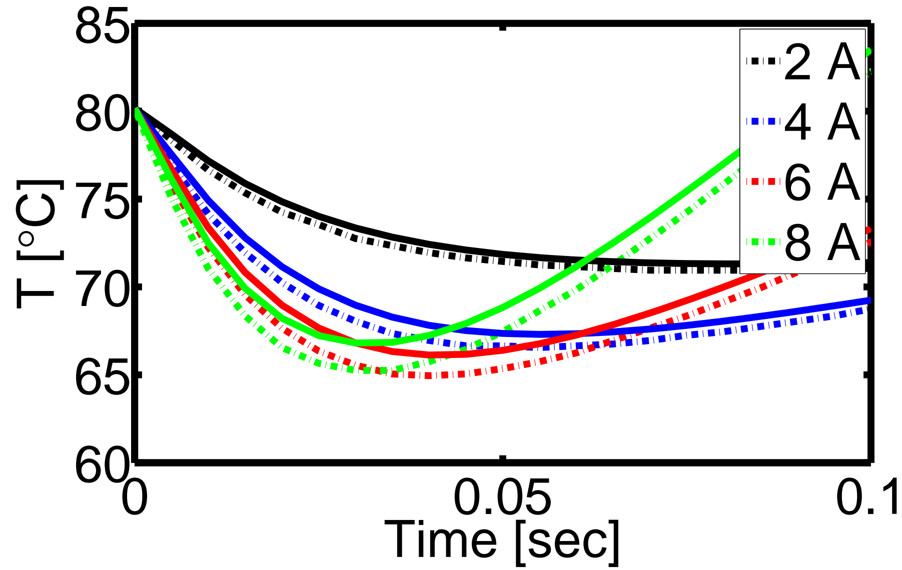


Figure 27: Validation of the transient temperature behavior obtained from 1-D compact model (dashed lines) against the 1-D finite-volume model (solid lines) with varying currents. Temperature is measured at the bottom of the chip.

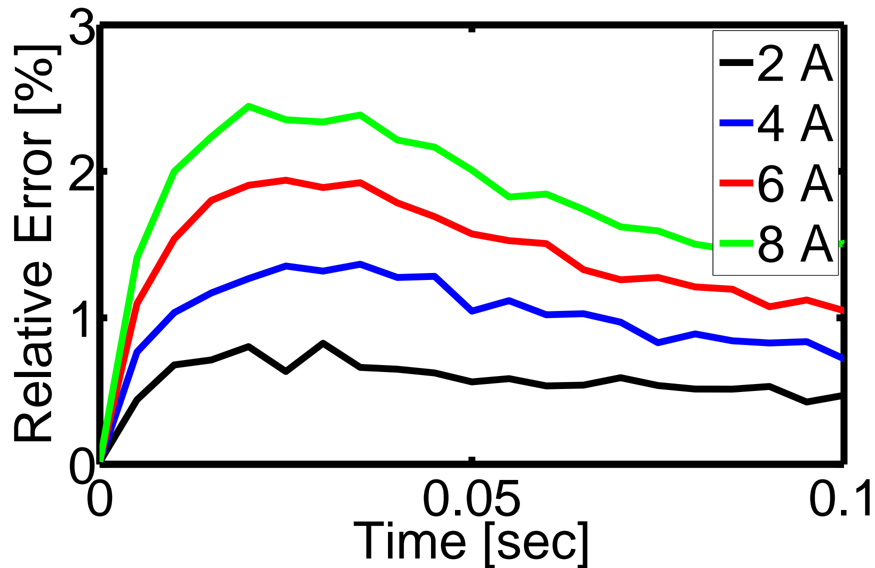


Figure 28: Relative error for transient temperature at hot spot computed from the 1-D finite volume method and 1-D compact models at various currents.

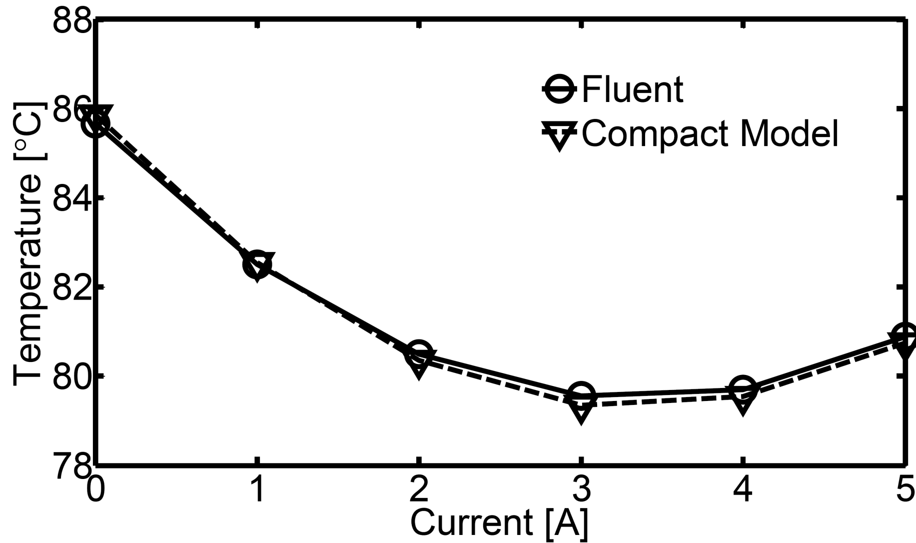


Figure 29: Steady-state validation of compact model of TEC integrated inside an electronic package against finite-volume model at various currents. The comparison is done for cooling (ΔT) at the center of the chip, directly below the location of TEC.

finite-volume method to compact model is shown in Figure 27. Once again the finite volume model and compact model follow similar trends. The relative error of the compact model compared to the finite volume method is shown in Figure 28. The error grows with increasing current similar to the steady-state models, but even with 8 amperes of current the maximum error is below 2.5% and further decreases with time. The transient results for hot spot temperature in the compact model were in good agreement with the finite-volume based model results. This close agreement of the compact model with the finite-volume method based model in both steady-state and transient operation suggests that the compact model can be used as an alternate model for all further simulations.

The 1-D model is then integrated into a full electronic package model by placing 1-D model of TEC in a 3-D array of resistances and capacitances representing the electronic package. The steady-state and transient comparisons for compact model and detailed FLUENT model are shown in Figures 29 and 30, respectively. The compact model's steady-state and transient behavior are very similar to the finite-volume

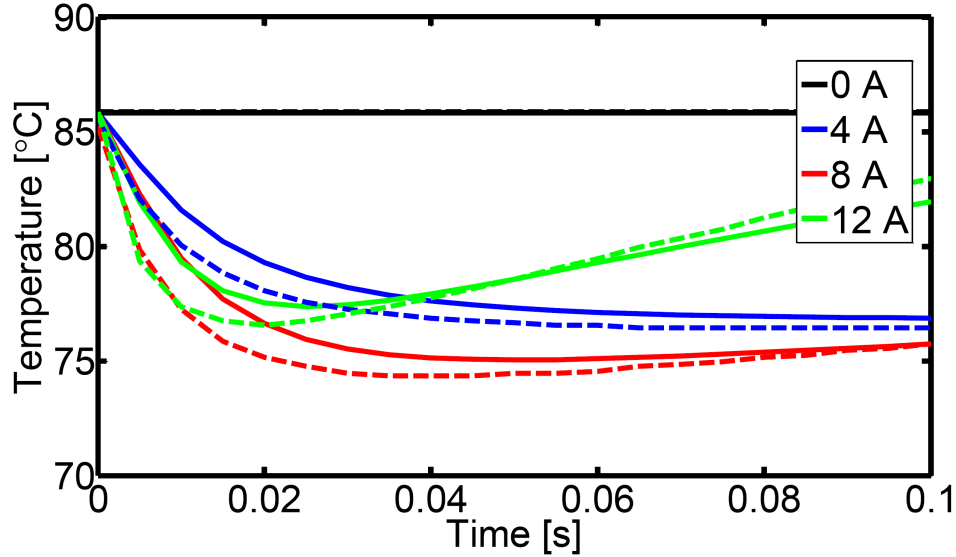


Figure 30: Transient validation of the compact model of TEC integrated inside an electronic package (dashed lines) against the finite-volume model (solid lines) for currents varying in the range of 0A-12A. The comparison is done for cooling (ΔT) at the center of the chip, directly below the location of TEC.

model. The addition of the spreader equivalent resistors and use of the multiplier have reduced the steady-state error dramatically (maximum relative error of ∼0.019%). The error present during the transient operation (maximum relative error of ∼2.9% for 8 ampere current) is also within acceptable ranges and validates the applicability of the compact model. The transient behavior of the package with the integrated TEC device at various currents is shown in Figure 30. The temperatures in this figure correspond to the center of the bottom surface of the chip, directly below the center of the TEC device.

The best current for transient behavior is observed to be at 8 amperes for the package geometry considered in the simulations and results in approximately 12 degrees of cooling in the package. Increasing the amplitude of transient current pulse results in an increase in cooling with a shorter response time, but the cooling lasts for a shorter period as the current amplitude is increased. This is due to the Peltier cooling at the surface, which has a faster response than the volumetric Joule heating within the

TEC device. For current pulses with higher amplitudes, the Joule heating increases rapidly (α I^2) and overcomes the Peltier cooling provided by the TEC device. A four ampere current pulse takes approximately 0.1 seconds to reach maximum cooling, but twelve amperes current takes only 0.02 seconds to reach maximum cooling. TEC controllers need to be able to detect the temperature rise at a hotspot and turn on a TEC for appropriate periods of time and current amplitudes in order to properly react to the thermal needs of the package. The computational time for the results shown in Figure 30 with 12 ampere current were estimated. The FLUENT model took 674.3 seconds whereas the SPICE model took 156.34 seconds; a 430% reduction in the computation time.

5.2 *Effect of TEC Location*

In this section, the effect of TEC location inside the package on TEC performance is investigated using the compact model developed in SPICE. The focus of this investigation is to evaluate how the location of the device affects the device performance and degree of cooling at hot spots. It is recognized that manufacturing constraints exist that inhibit attaching a TEC device directly to the chip. In the model used for the results in Figure 30, a 24μm thick TIM layer exists between the top of the chip and the bottom of the TEC device. Figure 31 shows the effect of decreasing this thickness from 24μm to 0μm, which is effectively decreasing the thermal resistance and capacitance between the chip and TEC device to zero. The degree of cooling achieved by the TEC device is higher and the maximum cooling occurs faster as the thickness of the TIM is decreased, effectively decreasing the response time of the TEC device for cooling the chip. Since the thermal resistance of any material is proportional to L/k, it can be expected that the results of Figure 31 would occur with proportional increase in the conductivity of the TIM as well. Therefore, either a decrease in TIM thickness between the top of the chip and bottom of the TEC device or an increase

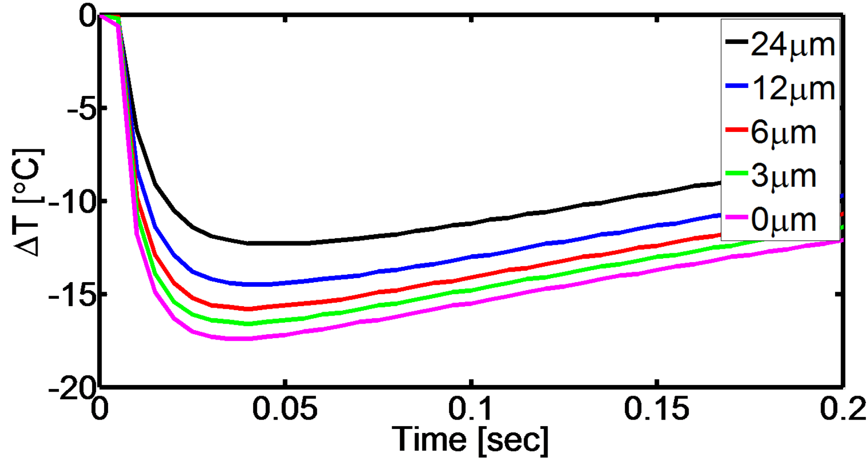


Figure 31: Effect of TIM thickness between chip and bottom of TEC device on the transient behavior of the TEC device with a current of 12 amperes. Five thicknesses are tested: 24μm, 12μm, 6μm, 3μm, and 0μm.

in the TIM conductivity by use of a different material can result in faster and better control of temperatures on-chip while using the TEC device.

5.3 Effect of Thermal Contact Resistance

As seen in Reference [30], thermal contact resistances within the TEC can have detrimental effects on the behavior of the TEC device. Figure 32 shows the performance of the compact model when increasing the thermal contact resistance between the copper and superlattice layers from 1x10^{-6} to 7.5x10^{-6} m^2K/W. It is expected that the cooling provided by the TEC device will degrade as the thermal contact resistance within the TEC increases. The compact model provides the expected results, i.e., cooling decreases as the thermal contact resistance increases. When contact resistance is increased from 1x10^{-6} to 7.5x10^{-6} m^2K/W, the cooling at hot spot degrades from 12°C to 5°C which is an over 50% reduction in the cooling performance of the TEC device. This result emphasizes the importance of the quality of the interfaces inside TEC device. Dependent on the fabrication method of the TEC modules and materials used in TEC device, the quality of interfaces can significantly change and an

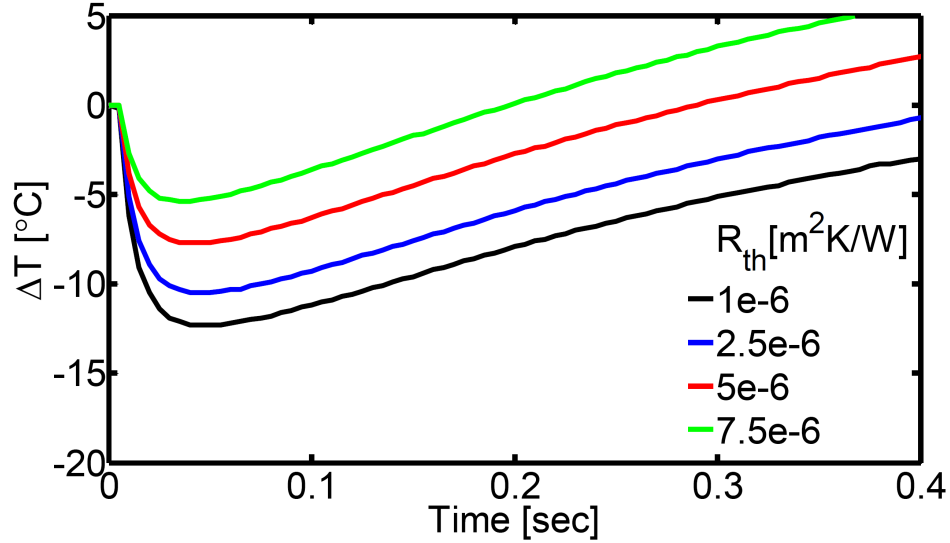


Figure 32: Effect of thermal contact resistance between copper and superlattice layers within TEC on transient performance of the TEC device for constant TEC current of 12 amperes. Thermal contact resistances are in the range from 1x10^{-6} to 7.5x10^{-6} m^2K/W.

interface with high thermal contact resistance can severely hamper the TEC's ability to perform.

5.4 Effect of Cooling Solution

The heat transfer coefficient (HTC) is typically utilized at the top of the heat spreader to represent cooling by an attached heat sink and the fluid flow through the heat sink. The material, design, and size of the heat sinks and the mass flow rate of the fluid through a heat sink affect the total amount of heat which can be removed using such cooling solution. The effective HTC applied at the top side of the heat spreader can significantly affect the TEC's performance. Figure 33 shows the effect of varying HTC on the maximum steady-state cooling of the TEC and the current amplitude at which this maximum cooling occurs. The heat transfer coefficient is varied from 1,000 W/m^2-K to 20,000 W/m^2-K, which represents a wide range of cooling solutions that can be employed for heat removal from microelectronic packages [16]. The maximum Peltier cooling obtained by using TECs at steady-state increases significantly for HTC

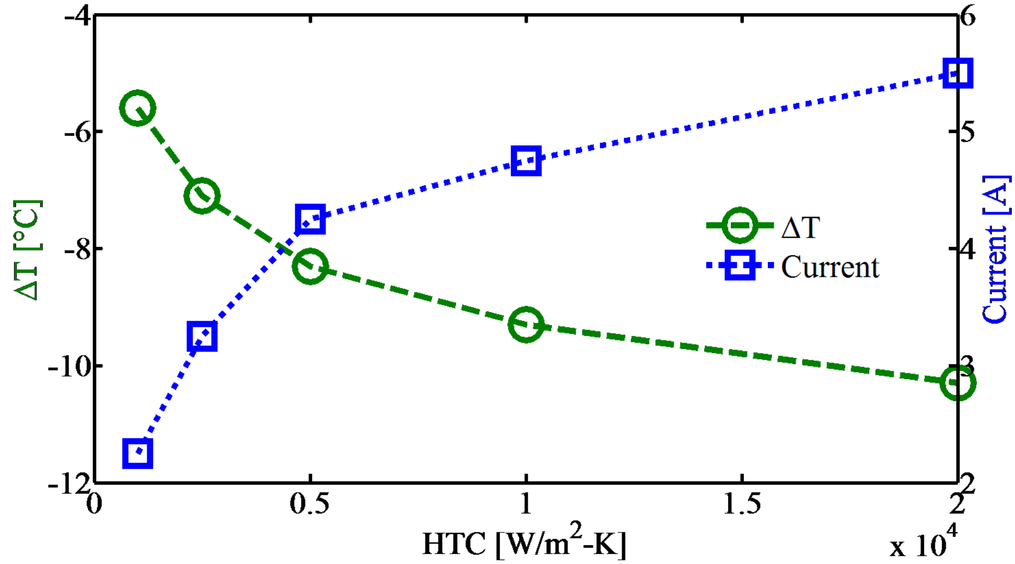


Figure 33: Maximum steady-state cooling and associated currents for various heat transfer coefficients (HTC) at top surface of heat spreader. HTC is varied from 1,000 W/m^2-K to 20,000 W/m^2-K.

in the range of 1,000 to 5,000 W/m^2-K. The Peltier cooling on the chip approaches to saturation with further increase in HTC or convective cooling. The point of saturation is due to the convective resistance approaching zero relative to other resistances in the system, such as the conductance resistance of materials or contact resistances at interfaces. The results in Figure 33 correspond to the materials and size of the electronic package under consideration, but similar trends are expected for other chip packages. The current associated with maximum cooling is also specified for each HTC considered and appears to follow a similar trend, i.e., the current amplitude for maximum cooling increases and approaches to saturation after 5,000 W/m^2-K. The analysis emphasizes that better cooling solutions used for the microelectronic package will also lead to the enhanced capability of TECs in cooling hot spots on the chip.

The following analysis investigates the effect of HTC on the transient operation of packaged TECs. Figure 34 shows the steady-state temperature (SST) at hot spot for various heat transfer coefficients when no current is applied through TECs and

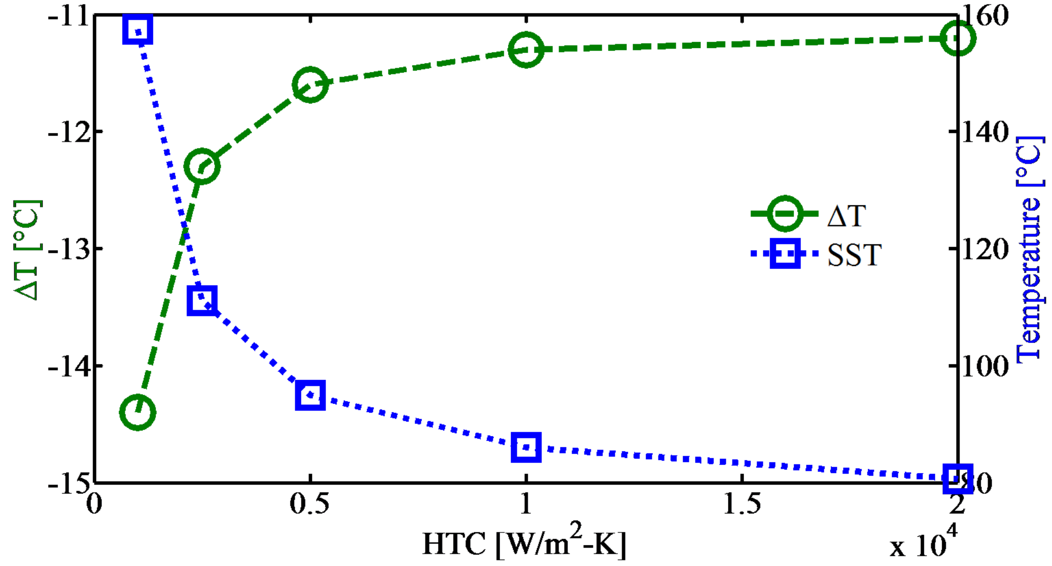


Figure 34: Maximum transient cooling (ΔT) and steady-state temperature (SST) with zero TEC current for various heat transfer coefficients at top surface of heat spreader, varying from 1,000 W/m^2-K to 20,000 W/m^2-K. Maximum cooling occurred at 7.5 amperes and 0.045 seconds for all cases.

the maximum Peltier cooling at hot spot (ΔT) during transient operation of TECs using optimal current pulse of 7.5 amperes. The maximum cooling occurred at 7.5 amperes and 0.045 seconds for the entire range of HTCs considered; so the heat transfer coefficient has no effect on the optimal current or response time for the transient cooling. The maximum transient cooling decreases from 14.4°C to 11.2°C as the HTC increases from 1,000 W/m^2-K to 20,000 W/m^2-K, which is in stark contrast with the steady-state cooling results. This can be explained by steady-state temperatures (SSTs) plotted in Figure 34 for different HTCs. As the HTC is increased, the steady-state temperature decreases rapidly and then saturates to near constant values as the convective resistance essentially approaches zero in comparison to the rest of the system. Increasing HTC at the spreader surface leads to different temperature distributions in the electronic package and reduces the hot spot temperature at steady state. The high HTC coefficient does not improve heat removal from TEC hot side during transient operation, which is reflected in the same optimal current for

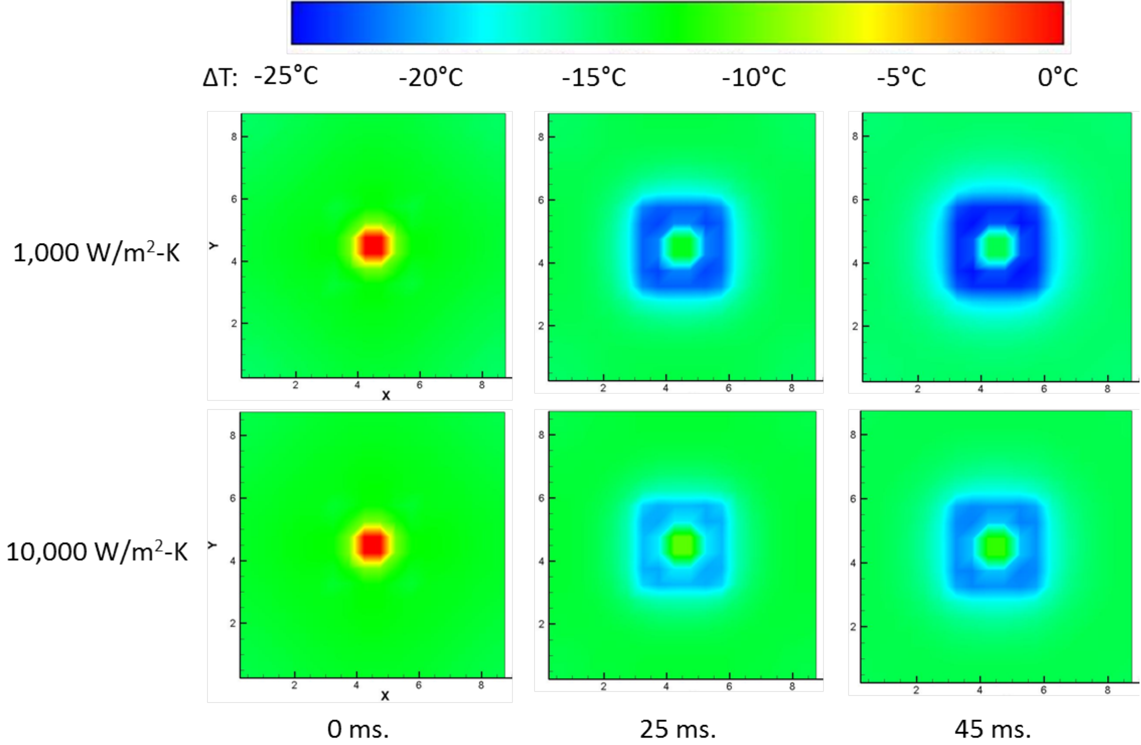


Figure 35: Contour plots for ΔT_p at the bottom surface of chip for convective heat transfer coefficients 1,000 W/m^2-K and 10,000 W/m^2-K at three different time steps: 0 ms, 25 ms, and 45 ms. For each convection coefficient, ΔT_p is estimated as temperature difference with respect to the peak temperature on-chip at t=0ms.

maximum cooling and the same time to achieve this maximum cooling for the entire range of HTCs considered. However, the lower steady state temperature at hot spots for high HTC leads to less cooling by TECs (ΔT in Figure 34) during transient operation. This behavior is further supported in the observed similar trend of saturation with HTC for both SST and ΔT in Figure 34.

Contour plots of T for the transient simulations are shown in Figure 35 for HTC 1,000 W/m^2-K and 10,000 W/m^2-K and for three different time steps: 0 ms, 25 ms, and 45 ms. Here, ΔT_P represents the difference in temperature as compared to the peak temperature on-chip at t=0ms for a given HTC. The peak temperature on-chip varies with HTC as shown in Figure 34, but such representation of ΔT_P provides a good way of comparing the contour plots for different HTCs. As shown, the lower

HTC corresponds to higher Peltier cooling under the TEC at different time instances, which could be due to the elevated steady-state temperature of the hot spot on-chip with a lower HTC as discussed above.

5.5 Summary of Results

A compact model was developed in SPICE for a TEC embedded in a microelectronic package. The model was validated for steady-state and transient behavior against the detailed finite-volume model. The integrated compact model can simulate the response of packaged TEC in significantly reduced time with reasonable accuracy when compared to the finite volume based model; in one scenario the computation time was reduced by 430%. Investigation of the packaged TEC suggested that the TEC provided optimal cooling with a current of 8 amperes during transient operation. The degree of cooling and response time improved as the TEC was moved closer to the top of the chip. Increasing thermal contact resistance at the metal-TE material interface detrimentally hurt the device's performance. Increasing the heat transfer coefficient at the top surface of the heat spreader results in an increase in maximum steady-state cooling but decreases the maximum transient cooling.

CHAPTER VI

THERMOELECTRIC GENERATORS

This chapter investigates the energy harvesting by thermoelectric generators (TEGs) embedded inside an electronic package. The geometry and thermoelectric properties of these TEGs are same as the TEC modules investigated in Chapter 4. The nine TEGs are arranged on-chip as shown in Figure 9. Unlike the previous work with the array of nine TECs, the TEGs were removed whenever the configuration is changed from a set of nine TEGs to a configuration with different number of TEGs. This chapter develops a CFD model in FLUENT for analysis of energy harvesting by TEGs.

6.1 Power Generation using Single TEG

This section studies the behavior of a single 3mm x 3mm TEG located at position 5 in Figure 9. There is a uniform background heat flux of 100 W/cm^2 and no hot spots for all simulations unless stated otherwise.

6.1.1 Load Resistance

TEGs produce a Seebeck voltage under an applied thermal gradient which can be used to power an electrical device or circuit. The electronic circuits can be very complex, but for the simplicity of analysis only a single load resistance connected in series with the TEG is considered. Figure 36(a) shows the current flow and voltage across TEG as a function of the load resistance (∼0-1 ohms). Figure 36(b) shows the temperature difference between the hot and cold junctions as a function of the load resistance. The electrical resistance of the TEG is 0.114 ohms including both material resistance and electrical contact resistance. As the load resistance increases,

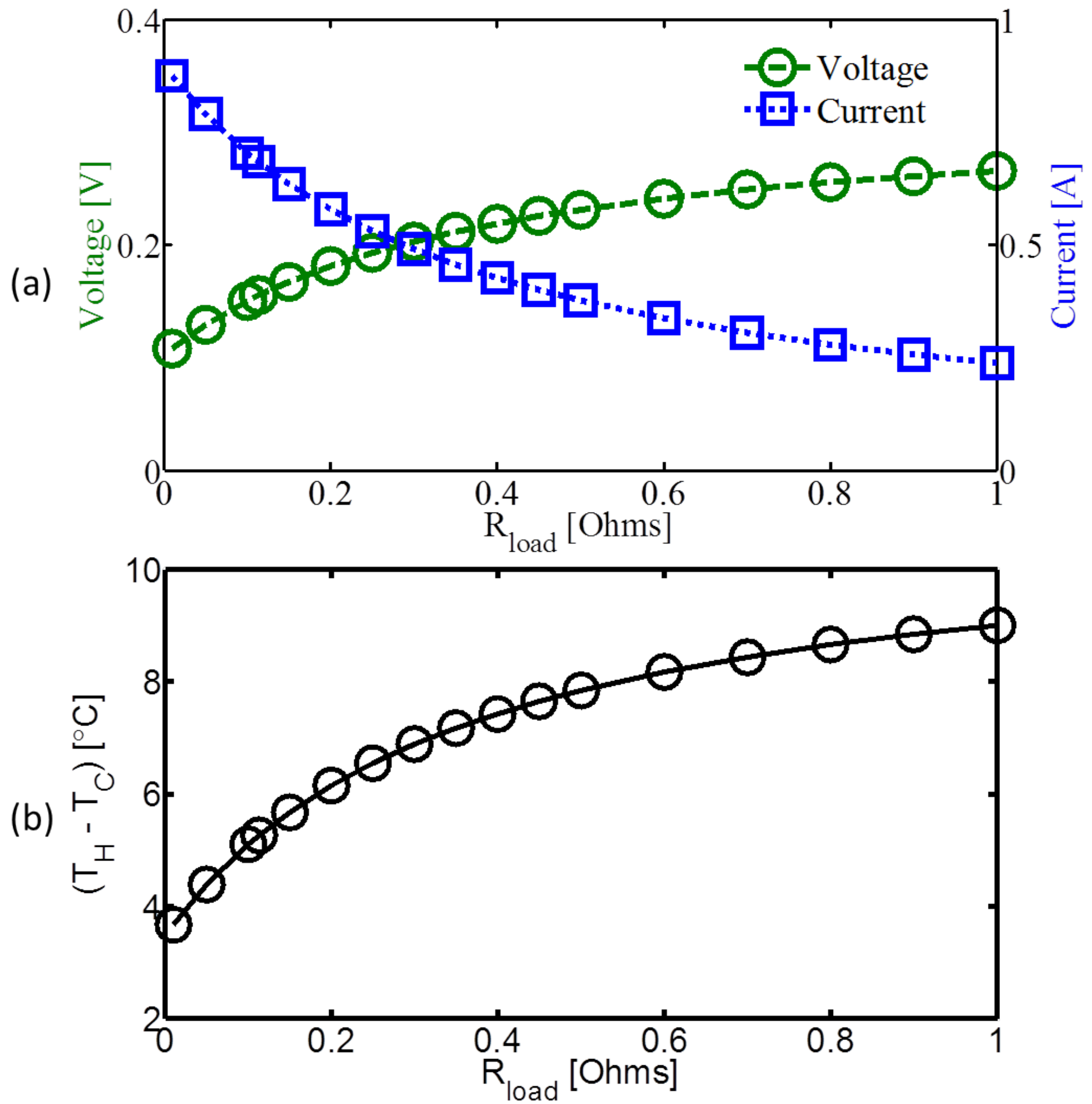


Figure 36: (a) Voltage and current, and (b) Temperature difference between hot and cold junction, of single TEG at position 5 as functions of load resistance.

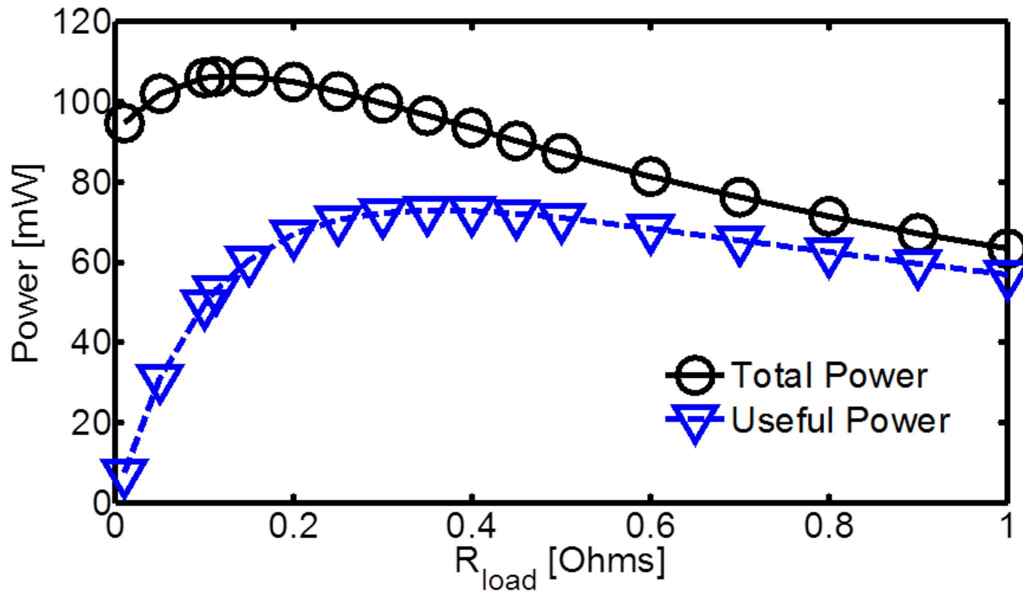


Figure 37: Total power and useful power, in milliwatts, of single TEG at position 5 as a function of load resistance.

the Seeback voltage and the temperature difference across TEG increases, but the current decreases. The increasing load resistance leads to decreasing current flow as expected from the relation in Equation 2. Lower currents provide less Peltier cooling at hot side of TEG, which increases the temperature difference and the Seebeck voltage as observed in Figure 36.

The CRC Handbook of Thermoelectrics states that maximum power transfer is obtained when the load resistance is equal to device resistance [8]. In the present study, the maximum power transfer did not occur when the load resistance is equal to the TEG device resistance.

The total power and useful power as functions of load resistance are shown in Figure 37. The total power is the addition of the power dissipated across the device and the load as opposed to the useful power, which is defined as the power dissipated across the load. The total power reaches its maximum value of 105 mW when the load resistance is equal to the device resistance (∼0.114 ohms), but the useful power doesn't reach its maximum until 0.35 ohms. The maximum useful power is 72.91

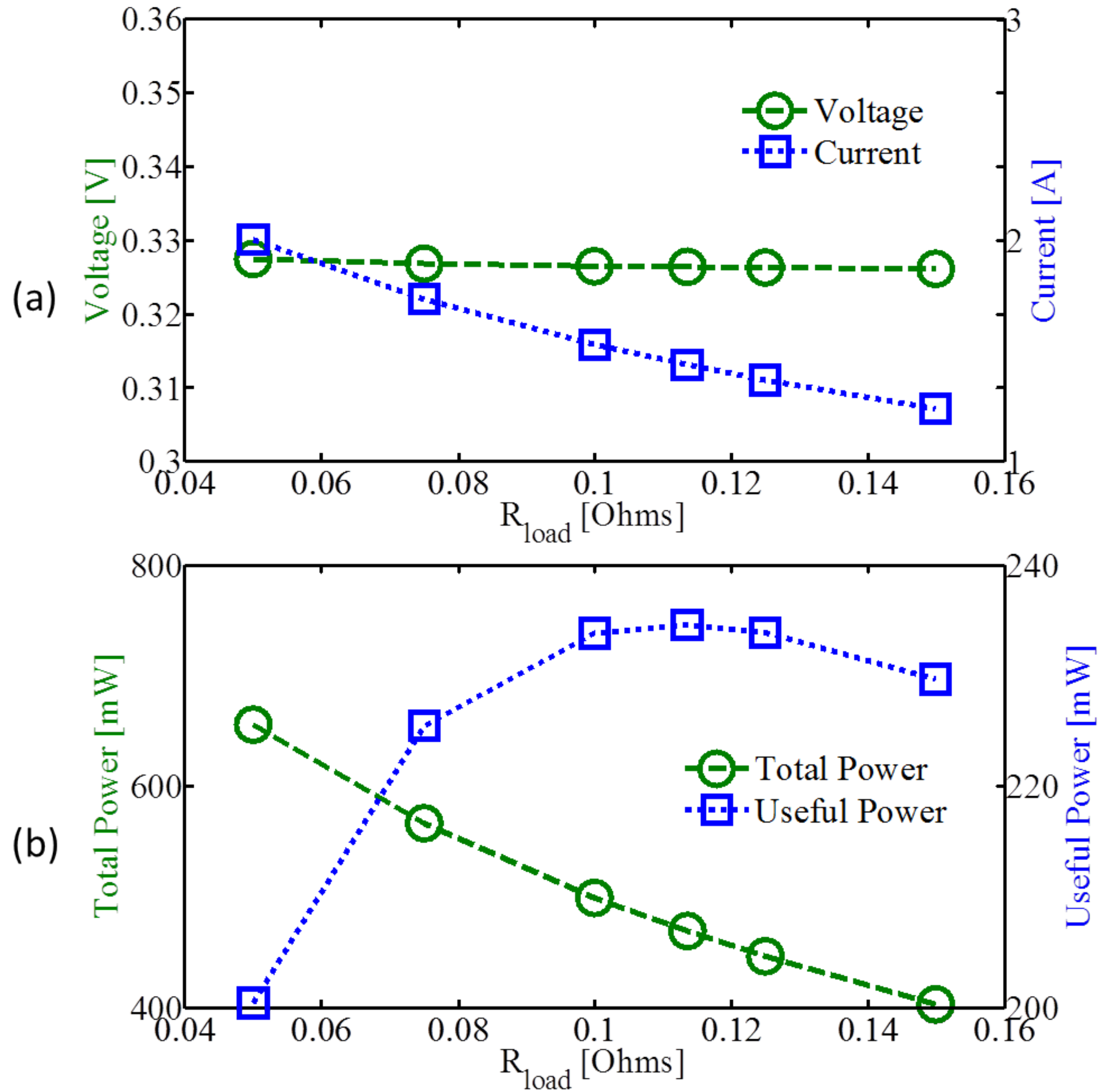


Figure 38: (a) Voltage and Current, and (b) Total power and useful power, in milliwatts, of single TEG with no Peltier effects at position 5 as a function of load resistance.

mW at this resistance. The reason the maximum useful power occurs at a different resistance is the dependence of Seeback voltage on temperature gradient across TEG, which is in turn dependent on Joule heating and Peltier cooling. Maximum useful power transfer will occur when the load resistance equals the device resistance only for the systems that have fixed temperatures across TEG. In the present analysis, the final temperature drop across TEG is itself dependent on the current flow due to the Peltier cooling effect, and a self-consistent solution is necessary to estimate the current flow, voltage, and temperature across TEG. This is reflected in the deviation of maximum useful power from the point when load resistance is equal to TEG resistance. Experimental validation is needed to confirm the magnitude of these results. Deviations from the expected load resistance for maximum power transfer were also reported by Solbrekken et al. in their work but TEGs were attached outside of an electronic package [28].

In order to further understand the deviation of maximum useful power discussed above, simulations where Peltier effect is not considered were performed. Figures 38(a) and 38(b) shows estimated current, voltage, and power with no Peltier effects, which is effectively keeping the voltage constant as the load resistance is changed. The maximum useful power is 234.56 mW when the load resistance is equal to the device resistance of 0.114 ohms. This is consistent with the expected resistance for maximum power transfer. The only change from Figure 38 to Figures 36 and 37 is the inclusion of Peltier effects, which affect the temperature difference across the two junctions and hence change the Seeback voltage. Therefore, the reason the results in Figure 37 differ from those expected for maximum power transfer is that the Peltier effects change the temperature gradient and voltage when load resistance is varied.

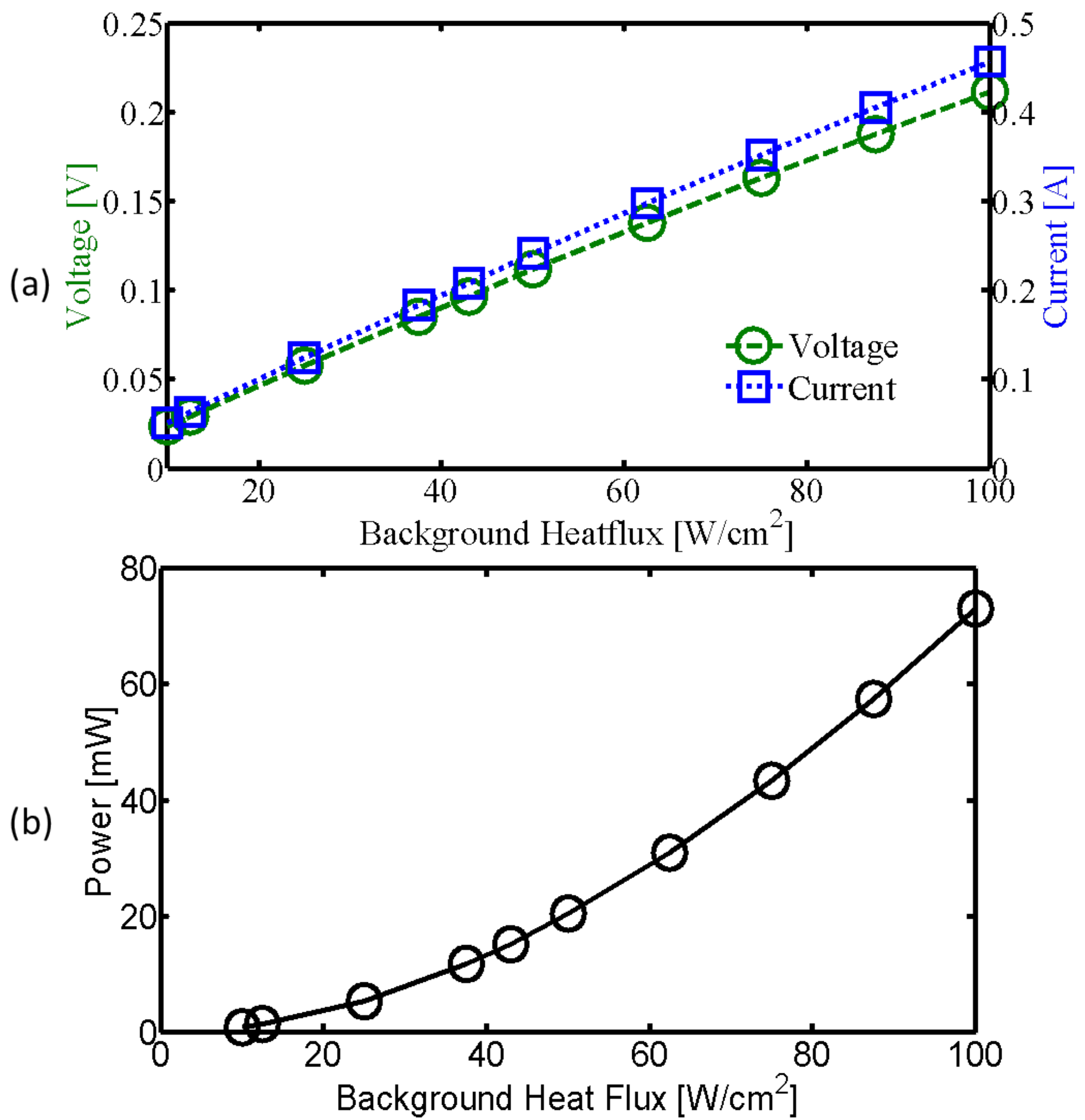


Figure 39: (a) Voltage and current, and (b) Useful power in milliwatts, of single TEG at position 5 as a function of background heat flux.

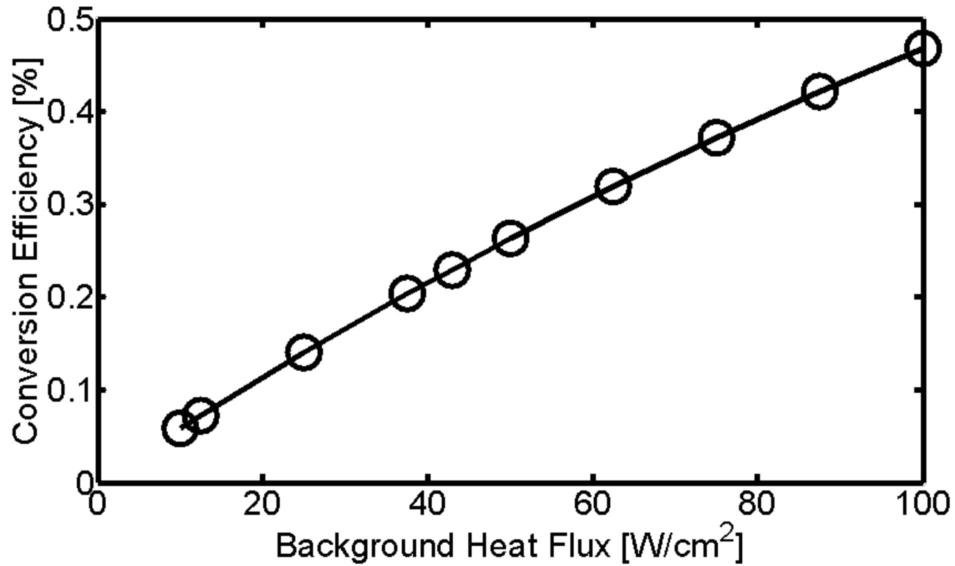


Figure 40: Conversion efficiency of single TEG at position 5 as a function of background heat flux.

6.1.2 Background Heat Flux

Thermoelectric generators can be used in conjunction with electronic packages for energy harvesting from waste heat. Heat dissipation varies in a wide range for electronic chips and significantly affects many design choices from the chip level up to the package level design and even further to server and building designs. This section investigates the effect of varying the chip's background heat flux on TEG performance.

The steady-state operation of the single TEG is investigated with background heat fluxes ranging from 10 W/cm^2 to 100 W/cm^2. The load resistance is set at 0.35 ohms as this resistance is shown to provide the best power transfer in the previous section. The Seebeck voltage and current as a function of background heat flux is plotted in Figure 39(a). The voltage and current increases almost linearly with increasing background heat flux. The load resistance is kept constant in these simulations, so voltage and current are proportional to each another. The useful power generated at various background heat fluxes is shown in Figure 39(b). As can be seen in this figure, the useful power increases in a parabolic form, which is expected since the

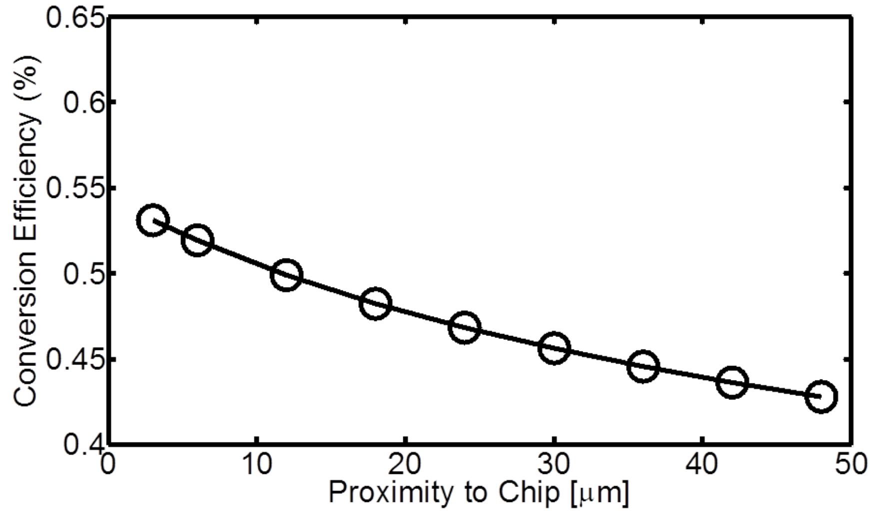


Figure 41: Conversion efficiency of single TEG at position 5 as a function of TEG's proximity to chip.

current increases almost linearly and power is proportional to current-squared. At 100 W/cm^2, the TEG generates 72.91 mW of useful power compared to 0.90 mW at 10 W/cm^2. This parabolic increase in useful power with background heat flux shows the increased utility of TEGs as power densities on-chip increase from one generation to another generation.

Conversion efficiency is the indicator of the power generation efficiency of TEGs. The conversion efficiency of TEGs gives the percentage of waste heat harvested into useable power and is defined as the amount of useful power divided by the heat flow through the hot junction. Figure 40 shows the conversion efficiency of the TEG as background heat flux increases. The conversion efficiency is observed to be almost linearly increasing with heat flux, e.g., conversion efficiency is 0.06% for 10 W/cm^2 and increases to 0.47% for 100 W/cm^2.

6.1.3 Proximity of TEG to chip

The degree of cooling by a thermoelectric cooler can be enhanced by moving the device closer to the heat source [29]. However, the modification in the performance of embedded TEG device as a function of proximity to chip is not studied yet. In

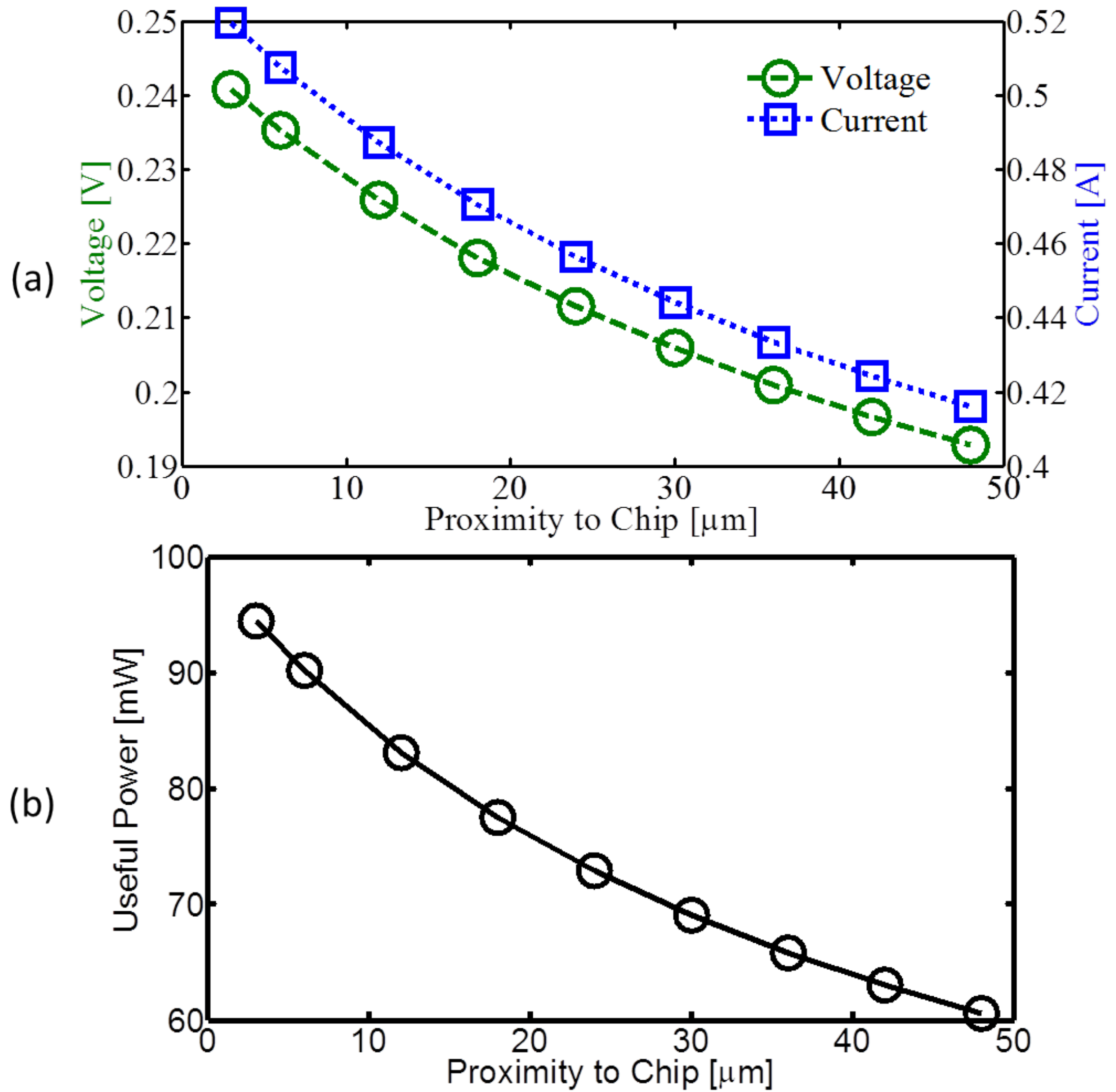


Figure 42: (a) Voltage and current, and (b) Useful power in milliwatts, of single TEG at position 5 as a function of TEG's proximity to chip.

this section, the TEG's proximity to the chip is varied to observe if there are similar increases in the TEG performance. The TEG is moved from 48 μm to 3 μm in order to test the chip proximity's effect on TEG performance. Figure 42(a) shows the voltage and current as a function of proximity to chip. Figure 42(b) shows the resulting useful power obtained at a load resistance of 0.35 ohms. The voltage, current, and useful power all degrade as the device is moved away from the heat source or chip. This is due to a decrease in temperature difference between the hot and cold junctions as the device is moved away from the chip. Figure 41 shows the conversion efficiency as a function of proximity to chip. The conversion efficiency behaves similarly to the useful power which is expected as the device is still the lowest path of resistance from chip to spreader and the heat flux through the device will not change drastically as it is moved further away from the chip. The next section investigates the use of multiple TEGs inside package to harvest energy from chip waste heat.

6.2 Array of TEGs on-chip

The discussion in the previous sections is based on the simulation of single packaged TEGs. This section will investigate the coupling effects of multiple TEGs on-chip and how this coupling affects the total useful power. It is expected that adding more TEGs will provide additional power as they are capable of harvesting more waste heat from the chip. Five different cases are investigated: (1) TEG-5 only, (2) TEGs 3, 5, and 7, (3) TEGs 1, 3, 5, 7, and 9, (4) All TEGs except 2 and 8, and (5) All TEGs 1-9. Here the location of TEGs corresponds to the setup depicted in Figure 9. Figure 43 shows the total useful power generated by all TEGs present on the chip and the average useful power per TEG. The total useful power continues to increase as additional TEGs are added, but it is interesting to note that it is not a linear increase. Total useful power increases in an approximately linear trend from one TEG to five TEGs on the chip, but this trend changes drastically for seven and nine

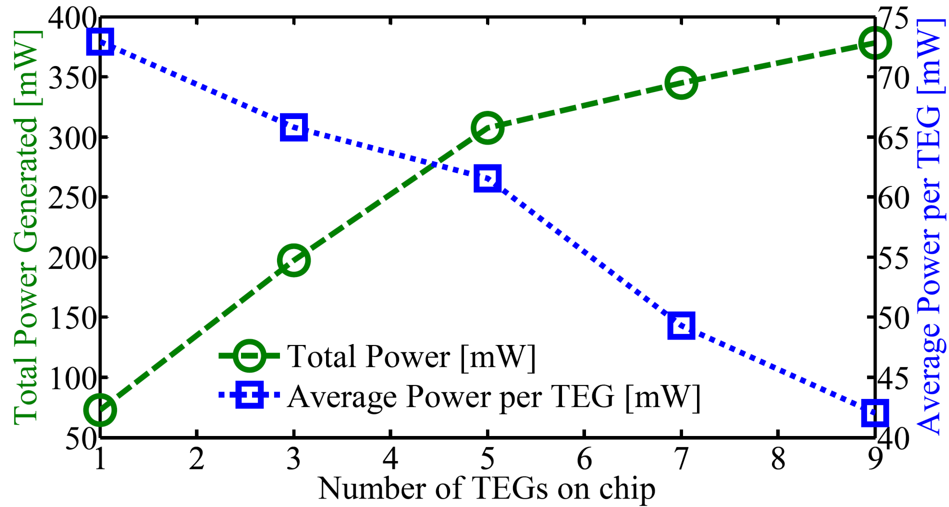


Figure 43: Total useful power and average useful power per TEG in milliwatts for five setups with varying number of TEGs on-chip: (1) TEG 5 only, (2) TEGs 3, 5, and 7, (3) TEGs 1, 3, 5, 7, and 9, (4) All TEGs except 2 and 8, and (5) All TEGs 1-9. Numbering of TEGs corresponds to setup shown in Figure 9.

TEGs. One TEG has a total useful power of 72.9 mW, five TEGs has 307.7 mW, and nine TEGs has 378.4 mW. Addition of four TEGs from Case 1 to Case 3 yields additional useful power of 234.8 mW, but another four TEGs from Case 3 to Case 5 only yields additional useful power of 70.7 mW. This decrease in the additional power that each additional TEG provides is due to the crowding of the TEGs on-chip. In cases 1-3 TEGs are well spread out at the center and corners of the chip. Cases 4 and 5, however, add TEGs on the sides in between the existing TEGs and end up degrading the performance of the TEGs already present on-chip. Overall the total useful power still increases, but the gains from additional TEGs begin to diminish. The average useful power provided per TEG degrades from 72.9 mW per TEG for Case 1 to 42.0 mW per TEG for Case 5.

The conversion efficiency of the center TEG and the average conversion efficiency of all TEGs present on-chip are shown in Figure 44 for Cases 1-5. The efficiency for Case 1 with only the center TEG is approximately 0.47%. This is the highest efficiency per TEG out of all cases considered. The conversion efficiency of the center TEG at

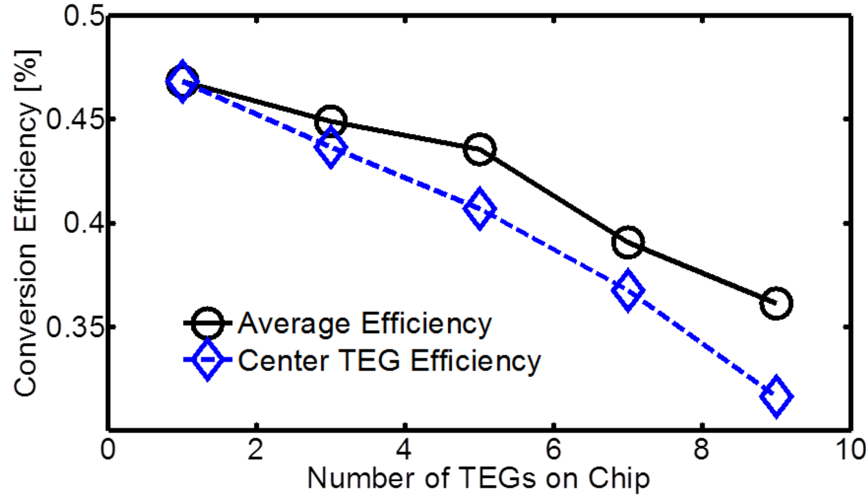


Figure 44: Average conversion efficiency of all TEGs and of center TEG only for the five setups outlined in Figure 43.

location 5 degrades drastically as more TEGs are added on the chip. The efficiency of center TEG decreases from 0.47% to 0.32% from case-1 of single TEG to case-5 of nine TEGs on the chip. Additional TEGs on-chip reduces the heat flux through the center TEG as it is no longer the sole low resistance path. This decreases the temperature difference between the hot and cold junctions significantly. The average conversion efficiency of all TEGs present on the chip is consistently higher than the efficiency of just the center TEG alone. This is due to the higher efficiency values for the TEGs located at the corners, which help in raising the average efficiency of TEGs. The average conversion efficiency reduces from 0.47% to 0.36% from Case 1 to Case 5.

The results from this section show that additional TEGs on-chip will always provide additional power generation, but TEG conversion efficiency degrades as more TEGs are added on-chip. Therefore, important design decisions need to be taken while designing a chip with embedded TEGs as there is an optimal number of TEGs for a desired total power.

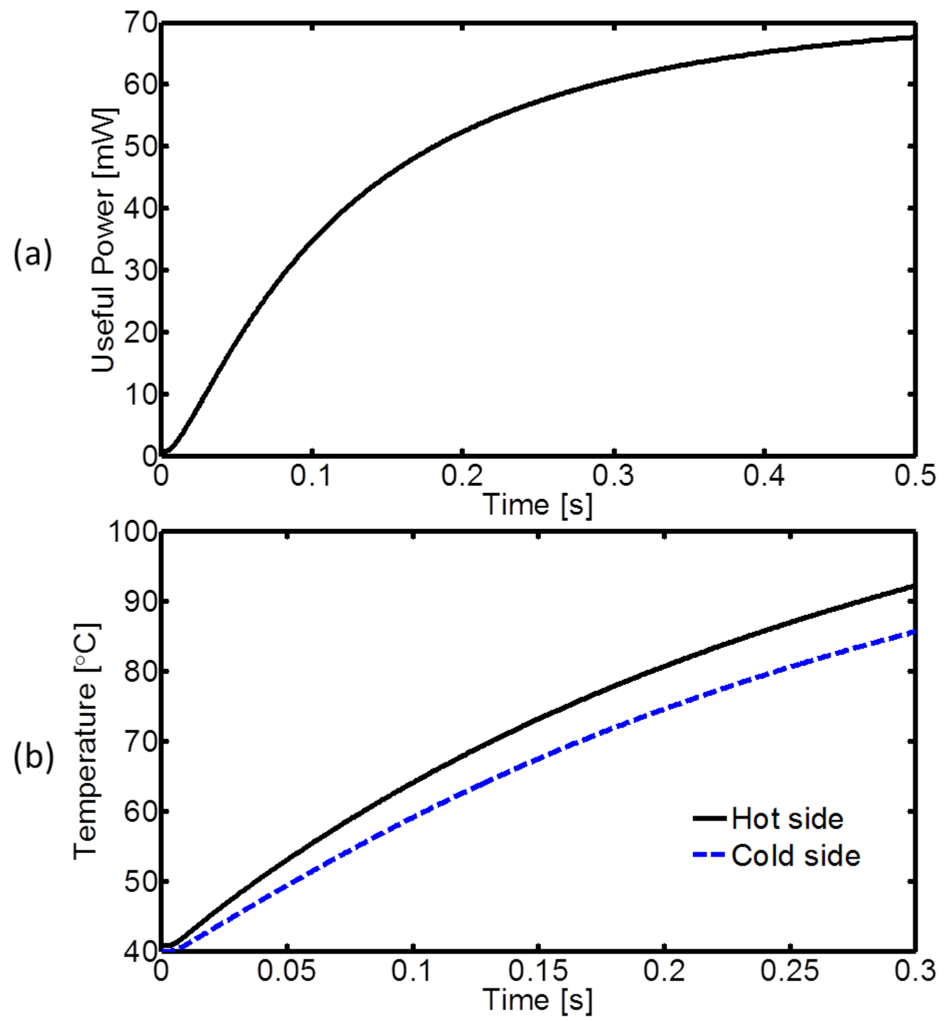


Figure 45: Transient (a) useful power response and (b) hot and cold junction temperatures of thermoelectric generator when background heatflux changes from 10 W/cm^2 to 100 W/cm^2.

6.3 Transient Response

In this section, the transient response of TEGs subjected to change in the background heat flux is investigated. Figure 45(a) shows the useful power of a TEG as the background heat flux is changed from 10 W/cm^2 to 100 W/cm^2. A small lag is observed between the heat flux change and the initial response of the TEG due to the time needed in any significant change in temperature across the TEG. As soon as the temperature difference across the TEG starts increasing, the useful power also begins to increase and finally approaches the steady-state useful power generation ($\sim$72.9 mW) for 100 W/cm^2. The temperatures of the hot and cold junctions of the TEG can be seen in Figure 45(b). The difference in temperatures follow the same trend as the useful power, i.e., it increases with time and approaches towards the steady-state solution for 100 W/cm^2. A TEG is a passive device, so there are no extra benefits in power generation in transient operation due to the dynamic change in chip heat flux. The most useful aspect of the present transient simulations would be to make sure that the current or voltage across load components does not exceed their given thresholds. The slow response time of the TEG to changes in the background heat flux appears to prevent any sudden spikes in current or voltage, and it seems that there is no danger to external loads.

6.4 Summary of Results

The FLUENT model of TEGs embedded in a chip provided insightful results. Maximum power transfer occurs when the load resistance is higher than the device resistance. This is due to the interdependence of the generated electric current and the temperature difference between the hot and cold junctions. Increasing the background heat flux can increase useful power in a parabolic fashion. Reducing TIM thickness between the hot junction of the TEG and the surface of the chip improves power generation from the TEGs, so proximity to chip is important. TEGs were then

arranged in an array and it was found that additional TEGs inside package always increases the total useful power generated, but TEG efficiency degrades as more TEGs are added.

CHAPTER VII

CONCLUSION & FUTURE WORK

7.1 Conclusion

This work explored the possibility of embedding thermoelectric devices within electronic packaging for both hot spot cooling and power generation. It used the commercial CFD solver FLUENT and the analog electronic circuit simulator SPICE to investigate operation of single and arrayed thermoelectric devices integrated inside a micro-electronic package. The important conclusions of this investigation are listed below:

- The FLUENT model of the array of nine TECs discussed in Chapter 4 provided many important results related to thermal coupling of adjacent TECs and transient pulse operation of TECs with different pulse shapes. The coupling among adjacent TECs during transient operation is weak, but the coupling is much more significant during the steady-state operation. The use of many smaller TECs can lead to better temperature control at hot spot locations. This would also minimize Joule heating from the TEC devices. From the analysis of pulse shapes, it can be concluded that the square root pulse provided the best cooling considering all of the important parameters: maximum cooling, temperature overshoot after current pulse is turned off, total energy expended, and settling time. Preliminary control results for random hot spots, using the square root pulse, show that frequent hot spots should be cooled with steady-state currents whereas infrequent hot spots may be able to better utilize transient pulses.

- A compact model of a TEC embedded in a microelectronic package was developed in SPICE and validated for steady-state and transient behavior against the

detailed finite-volume model. The compact model can simulate the response of packaged TECs in significantly reduced time and with reasonable accuracy when compared to the finite volume based model; in one scenario, the computation time was reduced by 430%. Investigation of the packaged TEC suggested that the TEC provided optimal cooling with a current of 8 amperes during transient operation. The degree of cooling and response time improved as the thermoelectric cooler was moved closer to the top of the chip. Increasing thermal contact resistance at metal-TE material interface within the TEC device detrimentally hurt its performance. Increasing the heat transfer coefficient at the top surface of the heat spreader results in an increase in maximum steady-state cooling but decreases the maximum transient cooling.

- Analysis using FLUENT model of TEGs embedded in a chip yielded important and insightful results. The maximum power transfer occurred at a load resistance higher than the device resistance, which conflicts with the traditional solution in which maximum power transfer occurs when the load resistance and device resistance are equal. This is mainly due to the dependence of the generated electric current on the temperature difference between the hot and cold junctions. This temperature difference is itself dependent on generated current and is inversely proportional to the load resistance. It was observed that increasing the background heat flux can increase useful power in a parabolic fashion. Reducing the TIM thickness between the hot junction of the TEG and the surface of the chip yielded improved power generation from the TEGs, so close proximity is very important. Finally, a study of an array of TEGS was completed and it was found that additional TEGs inside package always increases the total useful power generated; however, TEG efficiency degrades as more TEGs are added.

7.2 Future Work

Development of efficient control algorithms for the transient operation of TECs on-chip is an area that still needs detailed investigation. The random hot spot analysis in Chapter 4 provided some insights into some of the issues that can arise during TEC operation, but in-depth analysis must be completed to better understand transient TEC operation and efficiently control TECs. Further exploration of different electronic packages using the compact model should be performed. Using the compact model, it should be possible to integrate the thermal model described in this paper with a realistic circuit model of a controller or entire chip, which would allow realistic control and analysis of TEC. Finally, the work on TEGs only brushes the surface of possible work with TEGs. Experimental work on TEGs is needed to validate the TEG model. The TEC compact model can be changed to model TEGs and could be integrated with a realistic load device that may contain a mix of impedances, resistances, and capacitances to accurately model real devices. TEGs could be very beneficial for mobile devices as these devices run on a limited power source. Further research into use of TEGs in mobile devices could lead to important and insightful results.

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