PACKAGING DESIGNS FOR ULTRAVIOLET LIGHT EMITTING DIODES

A Thesis
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Master of Science in the
G.W. Woodruff School of Mechanical Engineering

Georgia Institute of Technology
December 2012

PACKAGING DESIGNS FOR ULTRAVIOLET LIGHT EMITTING DIODES

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To the Negassi & Habtemichael Family

ACKNOWLEDGEMENTS

I acknowledge God for His many blessings in bringing me to this point of achievement in my life.

I wish to thank Dr. Samuel Graham, my advisor in this long journey, for giving me the opportunity to study under him and for his technical guidance as well as his remarkable patience with me. Dr. Anusha Venkatachalam was also instrumental in my initial understanding of the subject-matter and for that I am deeply thankful to her. I also would like to thank my amazing partner-in-crime, Shweta Natarajan. Her hard work was a motivation, her constant support was paramount, and her insight into our project led to productive discussions and a better understanding of our problem.

I would like to thank the members of the EMRL group for their support and friendship. Here are some names off the top of my head: MinSeok Ha, Hossein Sojoudi, Sukwon Choi, Anne Mallow, Dr. Anuradha Bulusu, Samuel Kim, Nazli Donmezer, HyungChul Kim, Yongjin Kim, and Parisa Pour Shahid Saeed Abadi. I also want to mention some people outside of our group that have made the journey more enjoyable and less painful; Steven Isaacs, Vikneshan Sundaralingam, Paanii Ansah-Kofi, Sabri Gokmen, Victor Nwaneri, the Endirias family, Dr. Timothy Hsu, Akibi Archer, Benedict Vani, Jose Baltazar, and MANY more. People met through the GT-BGSA and the Gift-of-God Eritrean Church were also a big part of my journey.

Lastly, I must thank the sponsors of my work, the Defense Advanced Research Projects Agency (DARPA), Nitek, and Crystal IS, for without their support, this work would not have been possible.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Aluminum Gallium Nitride (AlGaN) / Gallium Nitride (GaN) based deep ultraviolet (DUV) light emitting didoes (LEDs) with emission wavelengths between 200-280 nm enable key emerging technologies such as water/air purification and sterilization, covert communications and portable bio-agent detection/identification systems for homeland security, and surface and medical device sterilization. These devices produce a large amount of undesired heat due to low quantum efficiencies in converting electrical input to optical output. These low efficiencies are attributed to difficulties in the growth & doping of $Al_xGa_{1-x}N$ materials and UV absorbing substrates leading to excessive joule heating, which leads to device degradation and a spectral shift in the emission wavelength. With this regard, effective thermal management in these devices depends on the removal of this heat and reduction of the junction temperature. This is achieved by decreasing the package thermal resistance from junction-to-air with cost-effective solutions. The use of heat sinks, thermal interface materials, and high conductivity heat spreaders is instrumental in the reduction of the overall junction-to-air thermal resistance.

This thesis work focuses on thermal modeling of flip-chip packaged deep UV LEDs to gain a better understanding of the heat propagation through these devices as well as the package parameters that have the biggest contributions to reducing the overall thermal resistance. A parametric study focusing on components of a lead frame package is presented to ascertain the thermal impacts of various package layers including contact metallizations, thermal spreading sub-mounts, and thermal interface materials. In addition the use of alternative thermal interface materials such as phase change materials and liquid metals is investigated experimentally.

CHAPTER 1

INTRODUCTION

1.1 Background

Light Emitting Diodes (LEDs) are a form of solid state lighting that use semiconductor materials to convert electricity into light. They have been in use in the electronics industry for more than 30 years as circuit board mounted indicator lights. The LED is considered as the next generation general lighting source and is becoming increasingly attractive in commercial arenas for its potential low cost, energy savings, longer life, significantly smaller size, higher intensity, variety of light colors, crack resistance, low temperature operation, etc. when compared with the incandescent light. The development of gallium nitride (GaN) has led to the main breakthroughs in LED technology due to its wide electronic band-gap, making it suitable for high-power, high frequency, and high temperature applications [1-3]. Continual improvement in the fabrication of high-quality bulk III-nitride crystals and their epitaxial layers has led to the recent advancements of GaN based light emitting diodes (LEDs) [4]. While much of the focus has been placed on visible light emitting diode technology for display and solid state lighting, scientific focus has turned towards the shorter-wavelength ultraviolet (UV) devices due to their technological importance.

Group III-nitride materials have band-gap energies tunable from 6.2 eV for AlN to 3.4 eV for GaN to 0.7 eV for InN [3]. Band-gap energy is the minimum energy required to excite an electron from the valence band to the conduction band. It also determines the photon energy emitted when a conduction electron recombines with a hole in the valence band [5]. Band-gap energy is inversely proportional to wavelength; this

relationship is denoted in Eq. 1-1. Therefore, the emission wavelength of an LED is dictated by the band-gap of the material used in its active region [4]. Figure 1.1 demonstrates the relationship between the direct transition band-gap energy, wavelength, and the lattice constant of the wurtzite In-Al-Ga-N material system. It is clear from this graph that a wide range of emission wavelengths can be obtained through the selection of various compositions of ternary compounds. Systems with higher mole fractions of Al (e.g., $Al_xGa_{(1-x)}N$) have higher band-gaps and emit at shorter wavelengths while high mole fractions of In (e.g., $In_xGa_{(1-x)}N$) emit at longer wavelengths due to the smaller band gap. However, it should be noted that the lattice constant of the ternary system also shifts, thus making growth of these systems on lattice matched substrates even more difficult. Table 1.1 shows the various combinations of semiconductor compounds that can be engineered based on desired emission wavelengths.

$$E_g(eV) = \frac{1.24}{\lambda(\mu m)} \tag{1-1}$$

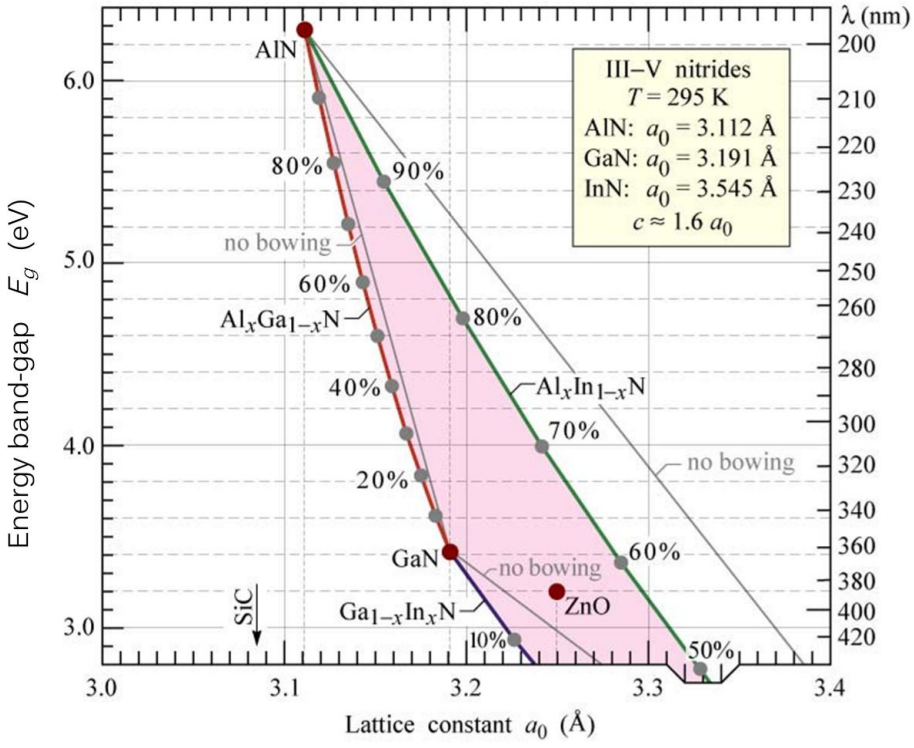


Figure 1.1 Relationship between band-gap energy, emission wavelength, and lattice constant of III-V nitride semiconductors at room temperature [6].

Table 1.1 Band-gap energy and emission wavelength ranges that can be achieved with the compound semiconductors; $0 \leq x \leq 1$.

Compounds	E_g (eV) Range	λ (nm) Range
$In_xAl_{1-x}N$	0.7 – 6.2	200 – 1771
$In_xGa_{1-x}N$	0.7 – 3.47	357 – 1771
$Al_xGa_{1-x}N$	3.47 – 6.2	200 – 357

1.1.1 Applications of Ultraviolet Radiation

The electromagnetic spectrum is divided into regions based on the wavelength of radiation. Current UV LEDs emit in the UV range of the electromagnetic spectrum ranging from 210 nm to 400 nm [4]. The UV spectrum is divided into four distinct regions: UV-A or long-wave UV (320-400 nm), UV-B or mid-wave UV (290-320 nm), UV-C or short-wave UV (200-290 nm), and vacuum UV (10-200 nm). Figure 1.2 displays an approximation of the UV spectrum as well as the visible band.

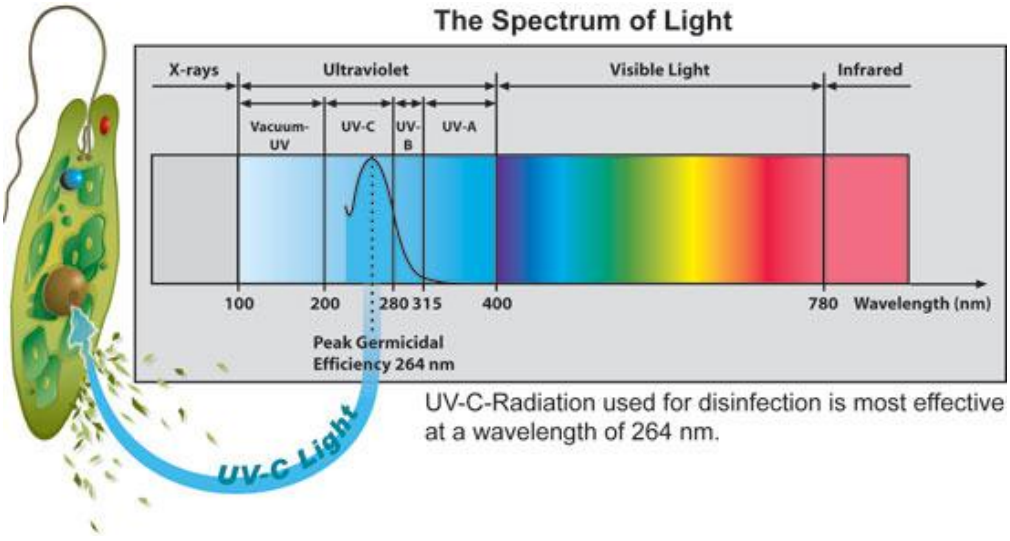


Figure 1.2 A schematic showing the ultraviolet region of the electromagnetic spectrum sub-divided into four regions [7].

Ultraviolet light in the 250-350 nm range has numerous useful and attractive functions. Some potential applications including air and water purification, UV photolithography, in situ activation of drugs through optical stimulus, solid state lighting, polymer curing and laser surgery exist for III-nitride based UV light sources [3]. The combined markets are fairly large, and the water purification market alone is estimated to be worth over $5 billion [8].

Water Purification

Efficient UV light sources can be used for the purification of river water, industrial waste water or atmospheric gases. The "germicidal range" of UV light is in the UV-C range (200-300 nm) with a peak germicidal effectiveness at 265 nm [9]. Exposure to ultraviolet light in the range of UV-C band disrupts the DNA of micro-organisms, preventing them from reproducing, thereby effectively killing them. It has been pointed out that an efficient 320-340 nm UV light source is required for the photo-catalytic decomposition of refractory pollutants (dioxin, PCB or NO_x gas, etc.) with titanium oxide (TiO_2) [3]. It was also found that UV LEDs emitting at 269 nm and 282 nm were able to effectively inactivate *Bacillus subtilis* spores during static and flow-through testing of varying water qualities [10]. Figure 1.3 shows an example of the germicidal effects of UV-C light disinfection. Another important application of UV LEDs is detection of biochemical agents. Certain agents glow when illuminated by UV light, thus being detectable due to the fluorescent light given off by these particular agents [3, 4].

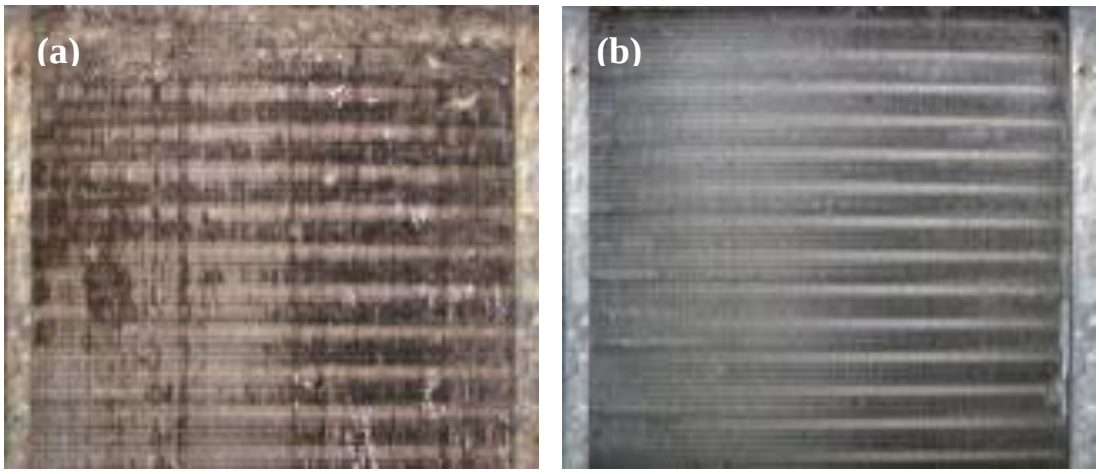


Figure 1.3 UV-C light penetrates the cell walls of micro-organisms causing cellular damage, and preventing cell reproduction. This can be seen in the difference between cooling coils (a) with mold growth and coils (b) cleaned by UV-C light exposure [11].

Covert Communications

There is a need for secure means of sending messages in a battlefield using low-power communication systems, a requirement that cannot be met with conventional RF radios. Covert or Non-line-of-sight (NLOS) communication with very low background, over distances up to 250 meters, is made possible by UV sources that take advantage of the "solar blind" region located at 280 nm and below. Also the high scattering and high absorption rate of the UV signal makes it difficult to detect from a distance, thus making compact, energy-efficient UV emitters an essential factor in the realization and advancement of portable UV-frequency-communicator technology [3, 12, 13]. Figure 1.4 shows the applications of UV transmitters and receivers in NLOS communication.

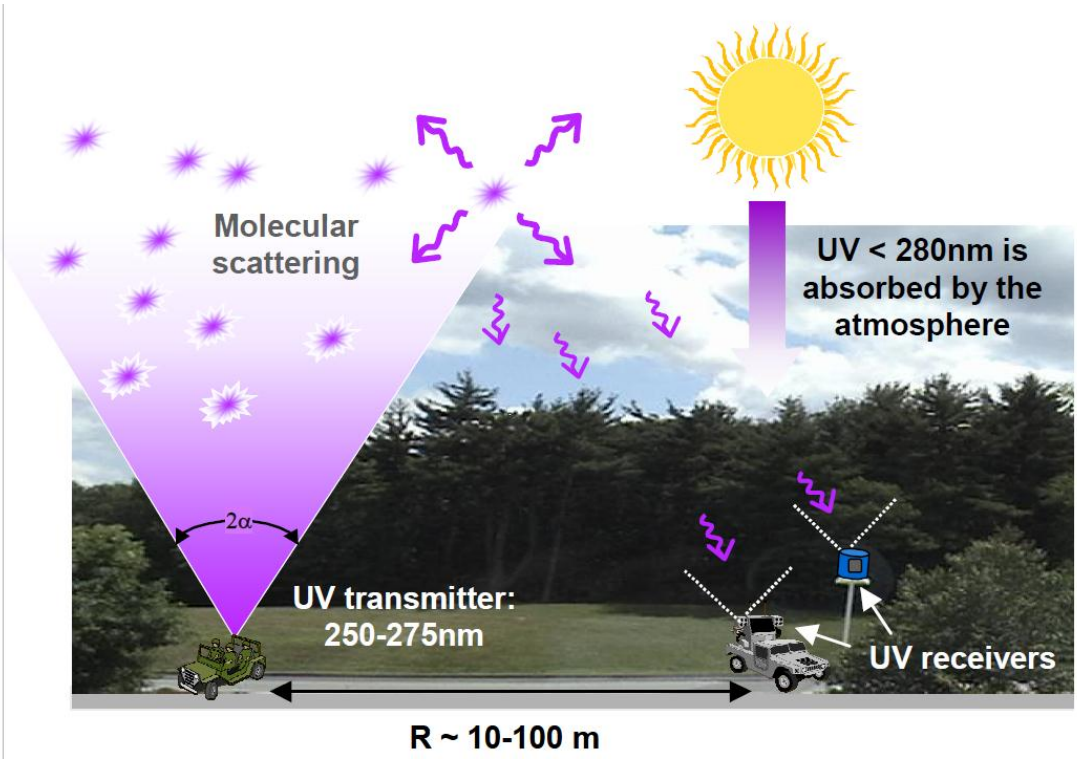


Figure 1.4 A diagram depicting NLOS UV communication between a vehicle and two sensors. The transmitter directs a broad UV beam upwards, and isotropic scattering from air molecules provides a diffuse return signal covering a large area. Receivers with broad acceptance angles detect the flux from within this scattering volume and demodulate the message. Atmospheric attenuation significantly reduces the solar background flux at wavelengths less than 280nm, which, in addition to presenting a benign background, prevents third-party detection and interception at ranges beyond a few kilometers [13].

White Light Generation

UV LEDs have the potential to make a big impact in the white-light LED market in the near future. By using UV LED pumped RGB (red, green, & blue) phosphors, white light with excellent color rendering and color reproducibility can be generated [3, 4, 14, 15]. This method would supersede the two existing methods of generating white light; one which combines RGB colors to produce white color and the other which combines blue color with yellow phosphorus (see Figure 1.5). The white light produced by the UV technique only depends on phosphors whereas the other methods involve several functions which result in problems that impede the color rendering, such as color mixing

and unwanted yellow-green gap with the RGB technique and poor phosphorus conversion efficiency and self-absorption in the blue-light-yellow-phosphorus technique [3, 14, 15].

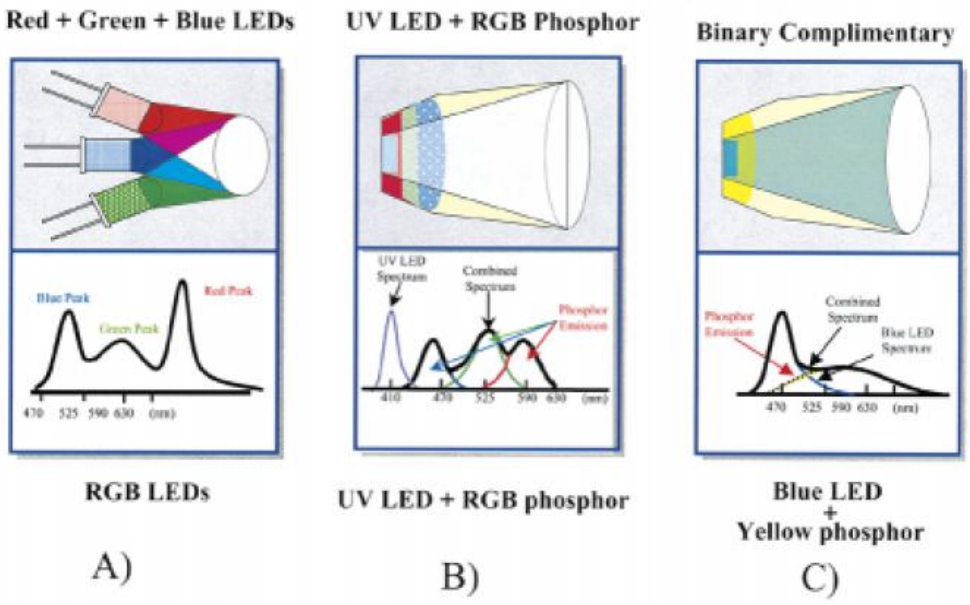


Figure 1.5 Three methods of generating white light from LEDs: (a) red + green + blue LEDs, (b) UV-LED + RGB phosphors, and (c) blue-LED + yellow phosphor [14, 15].

Today, the main source of deep ultraviolet (DUV) light for purification of microbiological contaminants is the mercury lamp. Many drawbacks exist with these lamps as they are bulky, require high operating voltages, cannot be driven in pulsed mode, and emit at fixed wavelengths. Moreover, contamination issues arise when considering medical or bio-medical applications. One attractive alternative to this lamp is the Al-In-Ga-N-based deep-ultraviolet (DUV) LED, which can be formed on sapphire or AlN substrates that are transparent at short wavelengths [8].

1.2 AlGaN/GaN based Deep UV-LEDs

1.2.1 Challenge 1: Heteroexpitaxy of Deep UV-LEDs

As previously stated, UV-LEDs are based on group III-V compounds, mainly combinations of Aluminum (Al), Indium (In), Gallium (Ga) and Nitrogen (N). These semiconductor devices require greater aluminum content, usually 50-80% (see Figure 1.1), than visible LEDs to emit at shorter wavelengths. Deep UV LEDs use AlN/GaN/InN quantum well (QW) structures grown on sapphire (see Figure 1.6). Due to the large difference between the lattice parameters of AlInGaN alloys and sapphire, 16% lattice mismatch with GaN [4, 16] and 12% with AlN [16], it is very difficult to grow high-quality epilayers (heteroepitaxially grown layers) directly on sapphire, which is the current substrate-of-choice because bulk lattice-matched substrates are not readily available. A low-temperature, thin buffer layer of GaN or AlN is usually grown on sapphire to initiate nucleation, relax the strain due to lattice mismatch, and aid in the growth of subsequent high quality layers [3, 17]. This creates a dislocated interface between the buffer layer and the sapphire which is necessary to produce more efficient LEDs, but also results in high thermal impedance due to the phonon scattering that occurs in the dislocated regions [3].

Growth of DUV LEDs on sapphire becomes more challenging in the UV-C range due to *high threading dislocation densities (TDD)* in the growing of AlN/AlGaN films on sapphire with the increasing lattice mismatch at high Al mole fractions, *doping challenges of* $Al_xGa_{1-x}N$ *layers* at high Al mole fractions [3], and biaxial tensile strain in AlGaN films, causing cracking [18]; just to name a few. The use of AlGaN/AlN superlattice (SL) buffer layers has been shown to alleviate the cracking of thick AlGaN films over sapphire substrates and to enable the growth of highly doped n-AlGaN layers with thickness exceeding 2 μm [19].

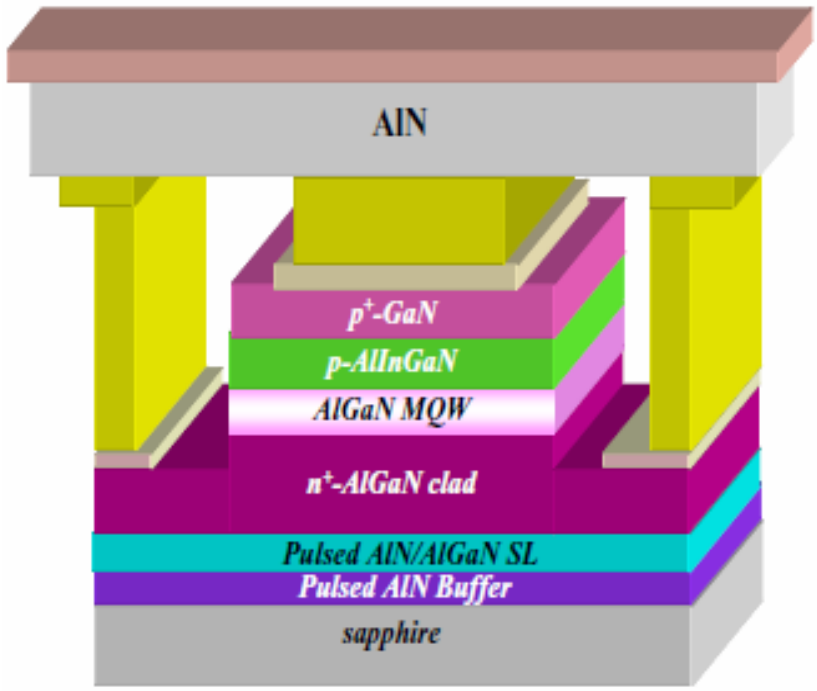


Figure 1.6 Typical structure of a flip-chip packaged DUV LED grown on Sapphire [4].

For $Al_xGa_{1-x}N$ on GaN, the in-plane stress is tensile because the lattice constant of $Al_xGa_{1-x}N$ is less than that of GaN. In most of the semiconductor material systems, this tensile stress can be relieved through generation of misfit dislocations, if the thickness of the layer under tensile stress exceeds a "critical thickness" [3], as described by the Matthews and Blakeslee model [20]. However, below this critical thickness, the top layer will grow "pseudomorphically", meaning its in-plane lattice constant will assume that of GaN [3]. Figure 1.7 shows the structure of an epilayer illustrating these two instances. Pseudomorphic growth of $Al_xGa_{1-x}N$ (x = 0.6) on a low-defect-density bulk AlN substrate has been achieved with a thickness far exceeding the "critical thickness" discussed above by more than an order of magnitude [21]. Pseudomorphic growth allows a high quality structure to be grown. However, it is clear from the steps needed to grow high quality layers for UV-LEDs, numerous interfaces as shown in Figure 1.6 are required and that dislocations are unavoidable. Also, due to the lattice mismatch issue, growth on either sapphire or AlN, which have suitable optical transparency in the DUV range, is required.

These factors impact the thermal response of the LEDs due to the limited thermal conductivity of the growth substrate, the dislocations in the material, and the number of interfaces that have been shown to reduce thermal conduction in other supper lattice structures such as thermoelectric devices. Thus, limited methods exist to effectively dissipate the heat generated by UV LEDs without damaging the functionality of the device.

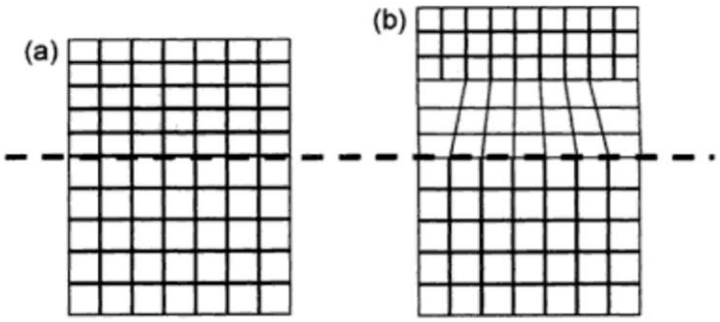


Figure 1.7 Structure of an epilayer under biaxial tensile strain: (a) pseudomorphic and (b) relaxed with misfit dislocations [3].

1.2.2 Challenge 2: Doping of AlGaN UV-LEDs and External Quantum Efficiency

In addition to growing high quality AlN/AlGaN, n-type and p-type doping of AlGaN films becomes very challenging due to low ionization efficiencies exhibited by silicon (n-type dopant) and magnesium (p-type dopant), as aluminum content is increased [4]; AlGaN with more than 50% Al content is required for fabrication of DUV LEDs. In other words, the "activation energy" of these dopants increases with higher aluminum-concentration AlGaN, thus leading to less hole and electron contributions from Mg and Si respectively, at room temperature. This leads to an increase in sheet resistance in the n-contact AlGaN layer, resulting in severe current crowding, which is further discussed in Chapter 2. It also leads to high forward voltages and makes it difficult to achieve

conduction in p-type AlGaN with an aluminum composition greater than about 15-20% [4].

Considering the relatively high ionization energy of magnesium dopants, 250 meV [4] in p-GaN and 510 meV in p-AlN [3, 22, 23], p-doping of high-Al-content AlGaN is even more challenging. Furthermore, it is also difficult to make an ohmic contact to p-AlGaN films, which is why a p-GaN layer is deposited on top of the p-AlGaN to serve as a contact layer (refer to Figure 1.6). This p-GaN layer has the potential to act as a barrier to holes passing from the p-metal onward to the p-AlGaN and the QWs. These trapped holes can recombine non-radiatively with electrons in the p-GaN layer, resulting in heat generation; a major factor in low quantum efficiency. The p-GaN layer also absorbs some of the UV emission, reducing light extraction and leading to low external quantum efficiencies (EQEs). *In order to deal with the problems associated with poor doping of the p-GaN layers in UV-LEDs, specific structures of the LEDs are required to reduce current crowding and improve the contacts. This involves the use of interdigitated and micro-pixel LED geometries that will be discussed in more detail in Chapter 2. However, these requirements further restrict what can be done in terms of efficiently dissipating the heat from these devices.*

For III-nitride materials, piezoelectric fields in the quantum-wells (QWs) also get stronger as the aluminum content of the alloy composition increases in order to achieve even shorter-wavelength emission. These spontaneous fields lead to the reduction of the radiative recombination efficiency of these devices owing to the quantum-confined Stark effect [4, 24]. This effect bends the valence and conduction bands of the material causing a detachment of the electron-hole pairs [4]. This poor electron-hole overlap greatly reduces the opportunities for radiaitive recombination, which leads to low EQEs. Additional factors that contribute to low EQEs include *low carrier confinement*, *UV absorbing templates and substrates*, and *lateral current crowding* [4].

The performance of an LED is characterized by its external quantum efficiency (EQE) also known as its wall-plug efficiency (WPE), which is the ratio of optical power output to electrical power input. It is a function of the internal quantum efficiency (the number of photons generated in the active region per electrons injected) and the extraction efficiency (the number of photons emitted from the LED per photon generated in the active region) [4]; see Eq. 1-2. Figure 1.8 summarizes the extremely low EQEs of these devices in the UV emission range (200-400 nm). It also shows the near-future targeted efficiency ranges.

$$\eta_{EQE} = \eta_{IQE} \cdot \eta_{EXT} \tag{1-2}$$

Currently, maximum EQEs for UV-LEDs (280-350 nm) range from 2 to 6%, while LEDs in the UV-C wavelength range have even lower EQEs with maximums around 1% [25]. The shortest wavelength UV-C LED, reported to emit 210 nm [4, 25, 26], was an AlN-based diode with an EQE of 10^{-6} % [26]. It is noteworthy to mention that these low efficiencies are also partly due to the novelty of these devices with the first AlGaN/GaN multiple-QW (MQW) LED, emitting at 353 nm being developed in 1998 [4, 27] and the first UV-C LED emitting at 285 nm being developed in 2002 [4, 28].

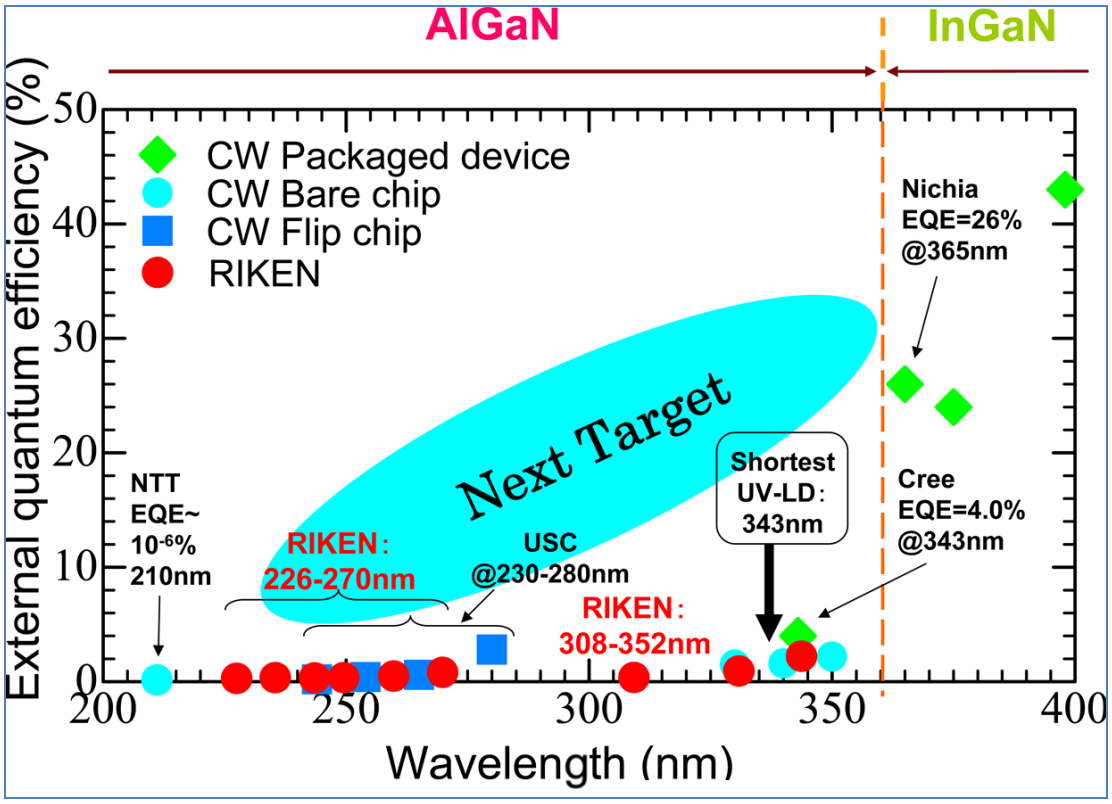


Figure 1.8 A display of the current state of external quantum efficiencies in UV-LEDs [29].

Hirayama et al. attributed the abrupt drop of efficiency of UV LEDs at wavelengths shorter than 360 nm, as seen in Figure 1.8, to the following three reasons [29]. First, the weak light emission of AlGaN because of high density of threading dislocations. Second, the difficulty of *p*-doping AlGaN and third, the unavailability of AlN/AlGaN buffer layers with low threading dislocation densities. In short, they suggested that all the problems of UV-LEDs arose from the use of AlGaN materials [29].

The key to producing the first successful devices was the combination of pulsed atomic layer epitaxy (PALE) and SL buffer layers. Taking this approach enabled the fabrication of 280 nm LEDs that delivered 1 mW of power at a DC pump current of 20 mA, and showed a reduction in power output after 1000 hours of operation of only 50 percent [8, 30]. However, to date there has been little progress in terms of higher powers

and longer lifetimes. Recently the Riken research group has succeeded in fabricating 250 nm devices that produce 1 mW of power at a 20 mA pump current [8, 29].

Nitek, a start-up company from the University of South Carolina, reported the use of pulsed lateral overgrowth (PLOG) in the fabrication of low-defect AlGaN templates with thicknesses well above 10 microns. These templates were not just beneficial to the emission efficiency but also displayed significant improvements in thermal management, leading to an increase in device lifetime by approximately 50% [8].

1.3 Reliability Issues

In LEDs, reliability issues come in two main forms; thermal and mechanical degradation. High power applications result in large heat generation due to the poor output efficiencies of these devices. Thus continuous wave operation often leads to high heat loads on the devices which eventually lead to a decrease in performance. Figure 1.9 shows this depreciation in performance with increased continuous operation time.

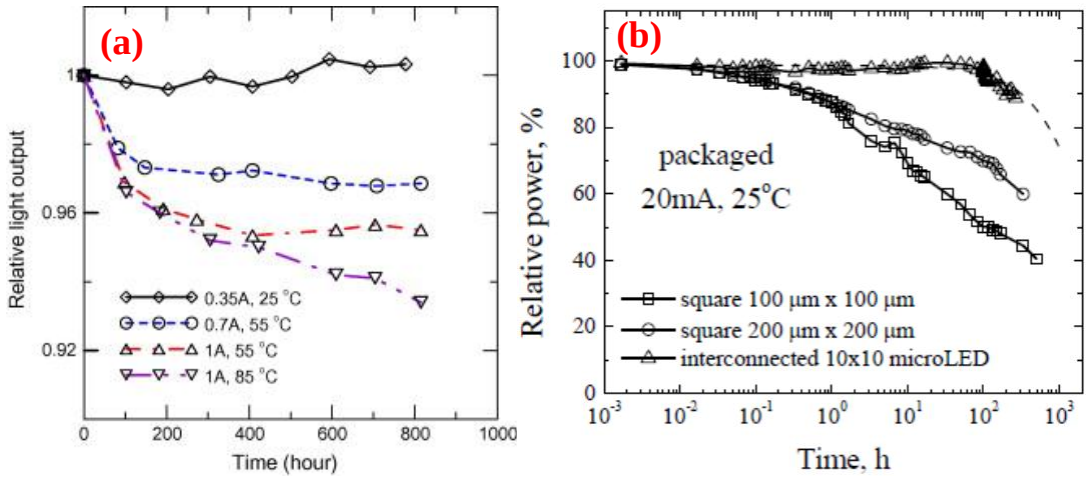


Figure 1.9 (a) Transient degradation of the relative luminous flux of LED samples under various aging stresses [31]. (b) Power degradation of packaged deep UV LED at 20 mA dc and 25 °C heat sink temperature [30].

Figure 1.9a presents the normalized luminous flux degrades at a greater rate for LEDs operating in higher ambient temperatures and higher driving current. At 1 A/85 °C, 1 A/55 °C and 0.7 A/55 °C, during more than 800 h of aging, the light output of the LED samples decreased by 6.6%, 4.5% and 3%, respectively [31]. Furthermore, the optical output diminishes with increased junction/ambient temperature and increased electrical bias; the lower the input power, the higher the optical integrity. Figure 1.9b shows the increase in junction area of the interconnected micro-pixel array (IMPA) LED leads to improved reliability performance with the projected operation lifetime for 50% power reduction to be over 1000 hours while the square devices reach a 50% power reduction in around 100 hours [30]. Shatalov et al. attributed this one order-of-magnitude improvement to lower current densities due to larger device areas and lower operating voltages due to lower series resistances, both leading to lower operating junction temperatures. The IMPA LED used for the aging test was made up of a 10x10 array of 22-μm-diameter pixels resulting in an active area close to 200 μm x 200 μm.

1.3.1 Thermal Degradation

Joule heating, also known as resistive heating, is the process by which the passage of an electric current through a conductor releases heat. Excessive joule heating or self-heating in sapphire-based UV LEDs, caused by high operating voltages, low emission efficiencies and poor thermal conductivity of sapphire (35 W/m·K), leads to a reduction in device lifetime and a spectral shift in emission [4]. Device self-heating can be alleviated by using highly conductive materials and mitigating the current crowding issue, which is further discussed in Chapter 2.

Thermally stressed AlGaN-based DUV LEDs were shown to have a distinct degradation trend than those that were electrically biased [32]. Figure 1.10 shows the two DUV LEDs, one thermally stressed and the other electrically biased, and their differing

degradation rates. The thermally stressed LED was placed in an oven at 184 °C, corresponding to the junction temperature when operated at 75 mA, and was taken out periodically for electroluminescence measurements while the second LED was stressed with a continuous drive current of 75 mA and underwent the same electroluminescence measurements.

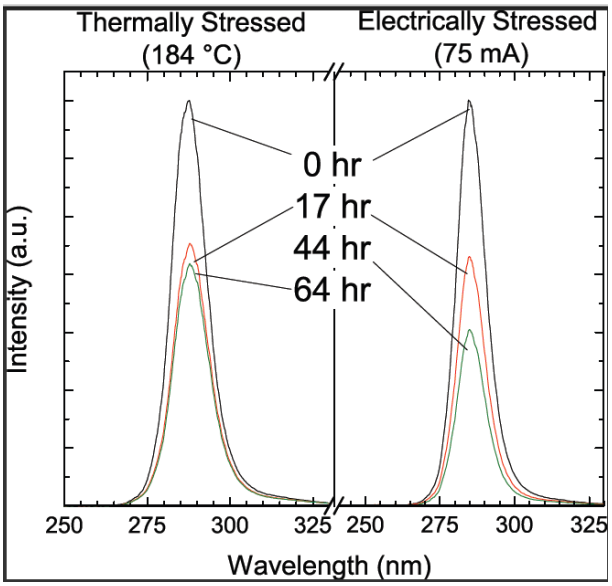


Figure 1.10 Electroluminescence spectra of LEDs thermally (left) and electrically (right) stressed over time. The device under electrical bias continued to degrade beyond that of the device held at the equivalent operating temperature [32].

The existence of another degradation mechanism besides joule heating is apparent in the differing degradation rates seen in Figure 1.10. Moe et al. ascribed this additional degradation to an increased nitrogen vacancy formation caused by the kinetic energy of electrons at the junction under high current densities [32] rather than to changes in the active region. Shatalov et al. also observed power degradation with two characteristic time constants indicating two degradation mechanisms; the faster time constant being bias dependent and temperature independent, while the slower time constant varied exponentially with junction temperature [30].

1.4 Thesis Outline

Packaging of deep UV LEDs is crucial for both light extraction and thermal management. The lack of transparent growth substrates with perfect lattice matching coupled with device self-heating makes it hard to realize high quantum efficiencies. This thesis seeks to study packaging schemes to address the thermal management aspect of AlGaN-GaN-based DUV LEDs through thermal simulation. Conventional LED packaging technologies, although mature, are not applicable in this case because UV emission can be greatly limited due to absorption by device layers as well as the growth substrate.

Chapter 2 provides an in depth description of UV LED device packaging. The structure of UV-LED chips, the development of UV LED arrays, and their advantages and disadvantages are discussed. Methodical material selection and packaging schemes are necessary to ensure semi-transparent to fully transparent layers in these packages while still being able to keep the junction-to-ambient thermal resistances low and reject the excess heat effectively. Chapter 3 will focus on the finite element analysis of single-chip and interdigitated micro-pixelated array (IMPA) UV LED packages. The factors at the chip-level package that impact the thermal resistance of the thermal circuit model as well as the effect of key layers on the junction temperature is studied. The 3D finite element analysis, performed in COMSOL Multiphysics, studies substrates, flip-chip bond pads and materials, as well as geometrical factors. The model is used to elucidate parameters which should be used to reduce the packaging thermal resistance. Chapter 4 will present data from alternative cooling experiments performed using innovative die-attach materials that were explored in this work such as immersion cooling in a dielectric fluid, liquid metal die-attach, and phase change materials. Chapter 5 states the final conclusions and proposes future work to further the development of the thermal management of UV-LEDs.

CHAPTER 2

LIGHT-EMITTING-DIODE PACKAGING REVIEW

2.1 Introduction

Heat dissipation in LEDs is governed by conductive heat transfer near the chip and thus the packaging architecture and materials used are critical in determining their thermal performance. With specific limitations in the optical requirements for UV LEDs, the packaging solutions are more restrictive than visible light LEDs. The purpose of this chapter is to review the packaging solutions of visible light LEDs, and the specific issues that must be addressed for UV-LED devices in greater detail.

2.2 Diode Packaging

All LEDs are mounted to a package that provides two electrical leads, a transparent optical window for the light to escape, and in power packages, a thermal path for heat dissipation. The evolution of diode packaging from the typical two finger leaded frames used as indicators to the modern high-power packages on printed circuit boards such as the “Barracuda” from Lumileds are presented in Figure 2.1. Early LED packages such as those used for the indicator LED have a chip that is soldered to the reflector cup which is attached to the cathode lead. The anode is electrically connected to the chip via wire-bond; these packages have a high thermal resistance of about 250 K/W. In low power applications, heat is usually extracted through the cathode/anode leads but for high power applications where thermal management demands are more critical, thermally-

enhanced structures are required. In such a structure, a heat slug made of Al or Cu is inserted between the sub-mount and printed-circuit-board/heat sink to create a direct, thermally conductive path from the LED chip, through the package, to the heat sink. These packages spread the heat and reduce the thermal resistance down to 6-12 K/W [6]. Adhesive layers are required to attach the sub-mount to the heat slug and the heat slug to the board, which unfortunately contribute significantly to the package thermal resistance [33]. This thermal bottleneck will be further discussed in the Chapter 3.

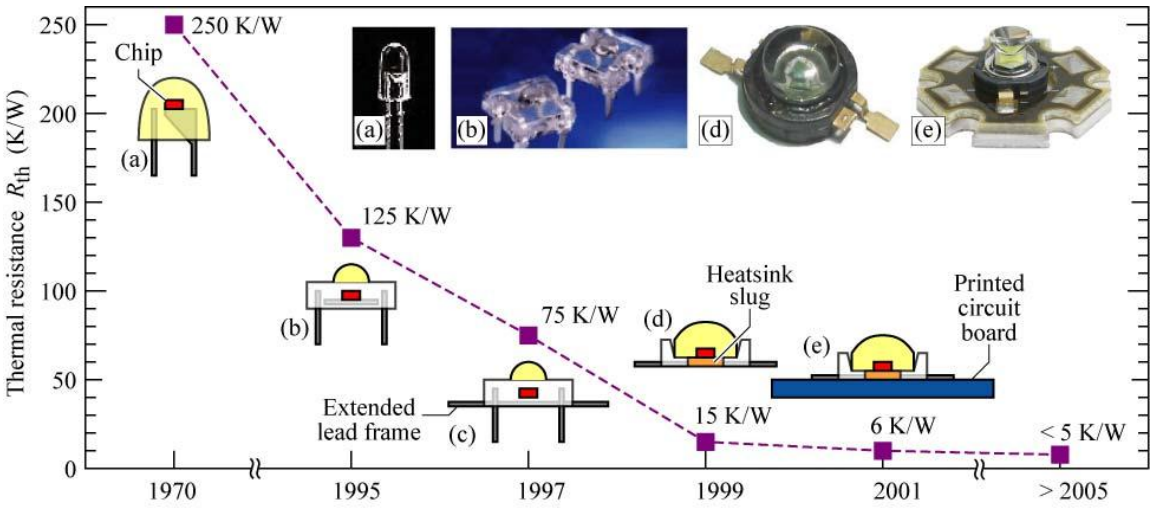


Figure 2.1 Thermal resistance of LED packages: (a) 5mm (b) low-profile (c) low-profile with extended lead frame (d) heatsink slug (e) heatsink slug mounted on printed circuit board (PCB). Trade names for these packages are "Piranha" (b and c, Hewlett Packard Corp.), "Barracuda" (d and e, Lumileds Corp.), and "Dragon" (d and e, Osram Opto Semiconductors Corp.) [6, 34].

2.2.1 TO Headers

Transistor Outline (TO) packages have been used for several decades in microelectronic packaging. A TO package consists of a TO header, which provides power to the encapsulated components and a TO cap, which ensures smooth optical transmissions. Generally, there are three different types of TO headers, distinguished by the production technology used to manufacture them and they are shelled TO headers, stamped TO headers with raised heads, and stamped TO headers with flat heads [35].

Sensor Electronic Technology Inc. (SETi) develops, manufactures, and sells DUV LEDs under the UVTOP® trademark. These UVTOP® LEDS are hermetically sealed in metal-glass TO packages with a variety of UV-transparent optical windows with varying beam profiles [36]. These packages are the TO39 header, offered with a Flat window, a Ball Lens, a Hemispherical Lens, or a Tall Flat Window, and the TO18 header offered similarly with either a Flat Window, or a Ball Lens. Figure 2.2 shows the three different lens types along with their typical emission patterns.

Nitek Inc. offers UV LEDs and UV Lamps in TO-39 and TO-3 packages respectively, under the UVRayZ™ trademark. Figure 2.3 shows the packaged Nitek devices. Researchers from Nitek have also used a TO-66 header to package a DUV LED lamp [30, 37].

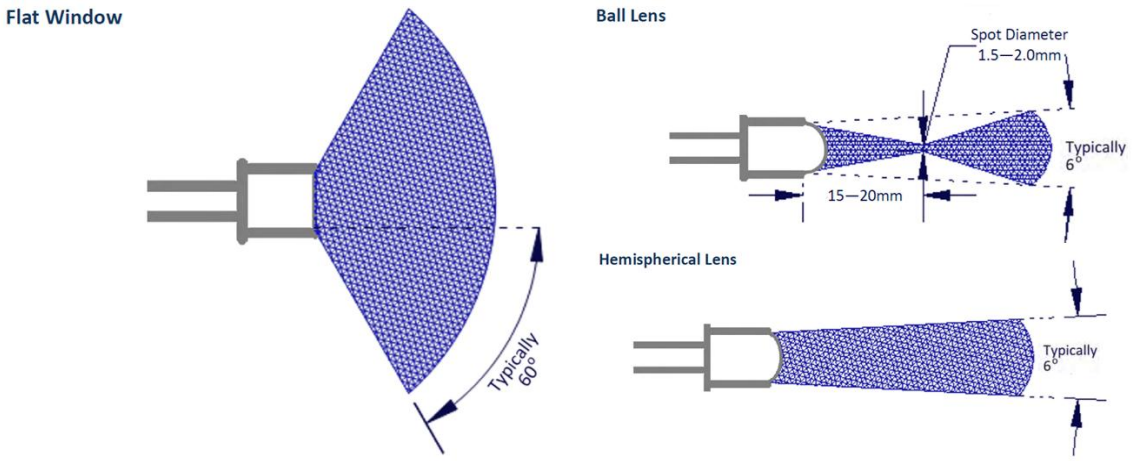


Figure 2.2 Typical emission patterns of UV LEDs packaged in TO39 and TO18 headers with various lens types [36].

Figure 2.3 TO39 packaged UV LEDs and TO3 packaged UV Lamps offered by Nitek Inc [38].

2.3 Chip Packaging & Design

Chip packaging design for III-nitride LEDs depends on the growth substrate and in the case of sapphire, the common approaches are conventional chip (CC) packaging, flip-chip (FC) packaging, vertical-injection thin film (VTF) packaging, and thin-film flip-chip (TFFC) packaging (see Figure 2.4). CC and VTF packaging both suffer from increased thermal resistance due to the low-conductivity sapphire substrate being in the heat extraction path as well as from the need for topside electrodes and wire-bonds hindering light emission. The approach that is most suitable for DUV LEDs is FC packaging, given that the additional manufacturing processes present with TFFC, in removing the growth substrate and roughening the exposed GaN surface to improve light extraction, are not necessary as sapphire is transparent to UV emission.

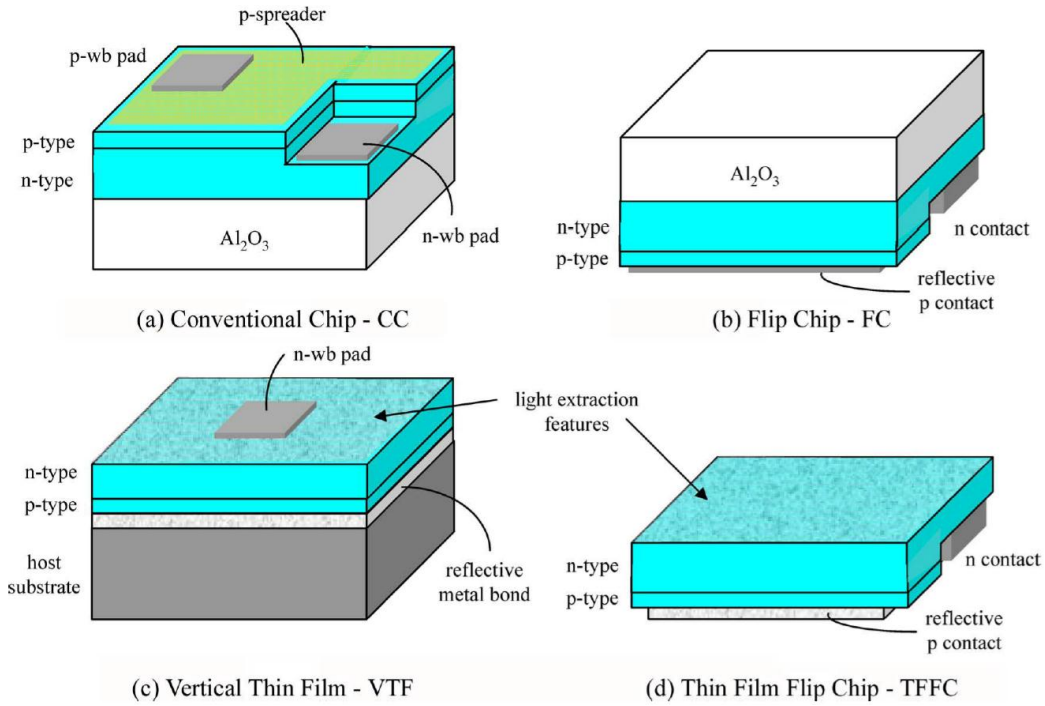


Figure 2.4 Typical chip designs for sapphire-based GaN LEDs; (a) Conventional "epi-up" design with semi-transparent top-p-contact. (b) Flip-chip design with reflective p-contact. (c) Vertical-injection thin-film design with reflective metal on host substrate. (d) Thin-film flip-chip design without sapphire growth substrate. Light extraction efficiency increases from (a)-(d) [1, 39].

Although flip-chip packaging is a more expensive [6] packaging process compared with conventional packaging where the LED top contact pads are contacted by wire bonding, it offers two main advantages making it attractive for UV LEDs. These include the elimination of hindering metal contacts in the UV light radiation path, and the enhancement of thermal management by attaching the chip to a high-thermal-conductivity sub-mount, see Figure 2.5.

The LED chip and growth substrate are diced, flipped and gold bonded on to a highly conductive sub-mount, which maybe AlN [4, 40], SiC [40], or a metal composite [40] in UV LED structures. This allows for the light to radiate from the top through the growth substrate while the heat can travel in the opposite direction.

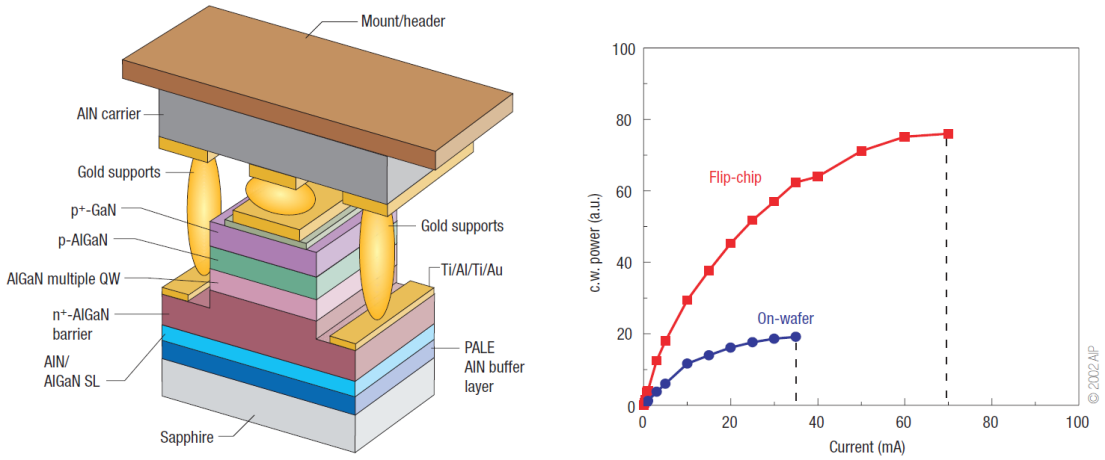


Figure 2.5 Flip-chip UV LED. (Left) Schematic of a flip-chip packaged deep UV LED. (Right) Continuous-wave output power of standard and flip-chip mounted UV LEDS. [4, 41]. Note that the left image is upside-down; meaning that when assembled normally, the flip-chip package will have the sapphire growth substrate on top and the AlN sub-mount/header on the bottom.

As presented in Figure 2.5, flip-chip packaging increases the saturation current by approximately two-fold. This allows for higher input currents and higher power devices, all owing to the lowering of device self-heating. The slope of the curve was also improved indicating better light extraction in the flip-chip configuration. Most importantly, flip-chip packaging negates the the p-GaN layer from absorbing the UV light by removing it from the path of the emission and it also places the p-GaN, which is a heat generating region, closest to the conductive sub-mount.

2.3.1 Lateral Current Crowding

Lateral current crowding, which is the non-uniform current distribution at the contacts leading to a non-uniform current injection through the active region, is one of the causes of joule heating and low injection efficiencies. Chitnis et al. observed higher temperatures in the periphery of flip-chipped devices, which was an indication of current crowding [41]. The finite resistance of the *n-type* GaN buffer layer causes the *pn* junction current to "crowd" near the edge of the contact; refer to Figure 2.6.

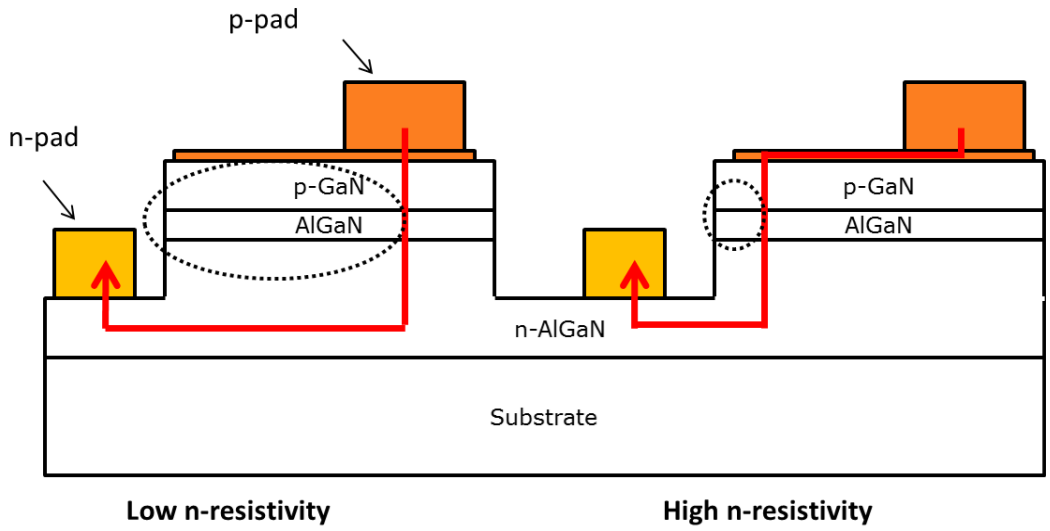


Figure 2.6 Schematic of two GaN/InGaN LED structures with one showing good current spreading and uniform distribution (left) and the second showing lateral current crowding (right). The current flow, from p to n, is depicted by the red line.

Guo and Shubert also showed that LEDs with high *p-type* contact resistance and *p-type* confinement layer resistivity have a relatively uniform current distribution. Also improvements in the *p-type* GaN conductivity and *p-type* ohmic contact conductivity will lead to significant current crowding near the contact edge [42]. Therefore, novel contact geometry designs such as the interdigitated multifinger geometry and the interconnected micro-pixelated array (IMPA) geometry were proposed solutions to mitigating lateral current crowding and improving device efficiencies [4, 42-44].

2.3.2 Interdigitated and Micro-pixelated Configurations

These electrode geometries mitigate the current crowding issue for large area high power LEDs by reducing the lateral distance between adjacent n-contact metallizations (see Figure 2.7). Chakraborty et al. showed a reduction in series resistance which made it possible to drive more than 3.5-A dc current through an IMPA DUV LED. Through calculations, they also showed that IMPA designs with pixel widths ≤ 40 μm would result

in significant improvement in current spreading [44]. The details of the IMPA DUV LED growth and device characteristics can be found [45].

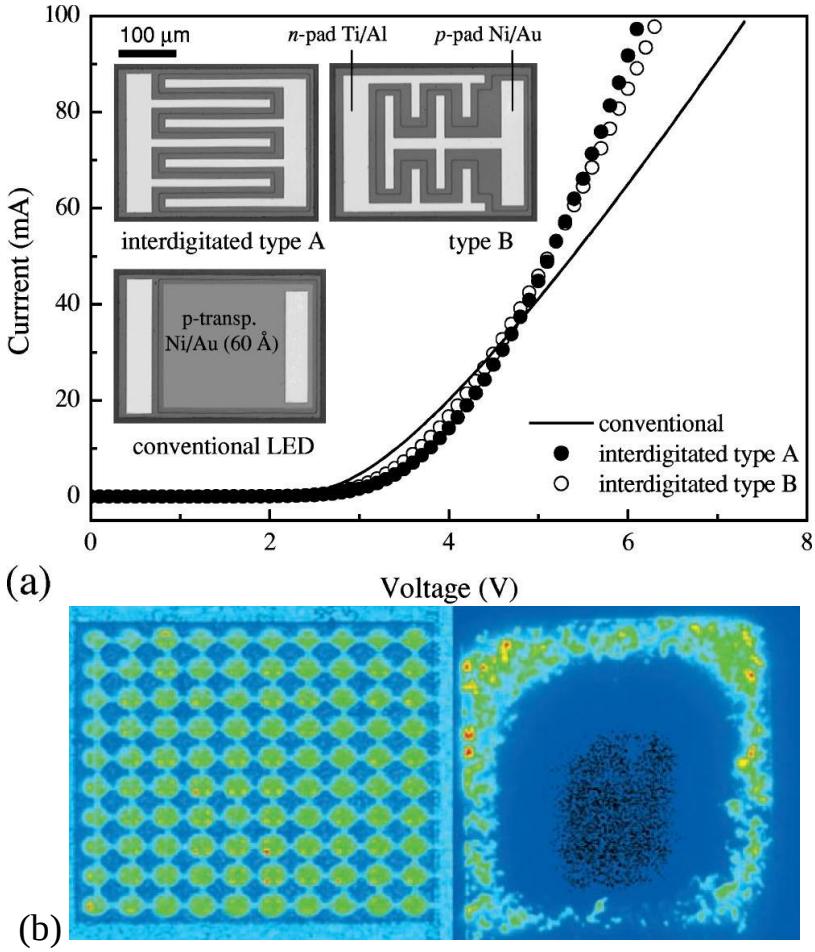


Figure 2.7 (a) The I-V curves of a conventional and interdigitated geometries [43]. (b) Micropixel UV-LED (left) and conventional square-geometry LED (right). Both devices have nearly equal total active areas and are shown under c.w. bias conditions [4].

Figure 2.7(a) shows the *I-V* characteristics of the conventional and the interdigitated type LEDs with same overall dimensions. The electrical characteristics are clearly superior for the interdigitated devices as appose to the conventional LED. Figure 2.7(b) shows images obtained from a CCD camera of a micropixel UV LED and a conventional UV LED of comparable size. The changes in color indicate non-uniform emission due to spatial variations in current injection; the lateral crowding, and thereby

joule heating, is reduced for lateral geometry LEDs by implementing the micropixel design [4].

The finite element modeling, reported in Chapter 3, was mainly performed on geometries similar to 'intergdigitated type B' from Figure 2.7. The only difference was that the structure used for modeling had *p* fingers on the outside with the *n* fingers stemming out from the middle; exact opposite from 'type B' in Figure 2.7(a).

2.4 Thermal Characterization of UV-LEDs

Effective handling of heat generation is a key consideration in the design of DUV LEDs. Thermal design requires understanding of spatial and temporal distribution of temperature fields within the system resulting from multiple-input operating parameters [46]. There are various numerical and experimental methods for thermal characterization of LEDs. Combined heat transfer mode modeling using the finite-element method (FEM) and the finite-volume method (FVM) are necessary in most practical interests in electronics cooling. Despite all of its advantages, computational methods cannot replace experiments. Numerical results must be validated with experimental thermal characterization methods; usually noncontact electrical or optical ways involving measurement of a temperature-dependent parameter. Electrical techniques such as the forward-voltage method and optical methods such as electroluminescence, Raman scattering, and infrared radiation are used for estimating temperatures at the junction of LEDs. There are also physical contact methods for measuring the temperature of an operating semiconductor device. Detailed explanation of the physical measuring methods can be found in the review by Blackburn [47].

2.4.1 Finite Element Thermal Modeling

Shatalov et al. have shown thermal analysis of flip-chip packaged 280 nm LEDs mounted on TO-66 headers and attached to heat sinks. Numerical simulations showed that 82% of heat energy flows along the flip-chip bond, through the AlN submount, into the header and heat sink while only 18% passes through the sapphire growth substrate [48]. Han et al. studied the effect of the top-adhesive (between sub-mount and heat slug) thickness and conductivity on the junction temperature and maximum strain using thermo-mechanical modeling. It was found that increasing the conductivity and reducing the thickness of the adhesive lowers the junction temperature but increases adhesive strains [33]. On the other hand, significant improvements in junction temperature and negation of CTE mismatch effects on strain can be achieved by using solder materials instead of adhesives [33, 39]. Senawiratne et al. investigated junction temperature effects of GaInN/GaN quantum well LEDs grown on sapphire and bulk GaN substrate. Finite element simulation results suggested better cooling efficiencies and lower junction temperatures in dies grown on GaN versus sapphire substrates. Dies grown on GaN substrates demonstrated thermal resistances of 75 K/W whereas dies on sapphire substrates had values as high as 425 K/W [49]. Arik et al. conducted several studies to deduce the effect of chip packages on junction-to-board thermal resistance of high-brightness (HB) LEDs using finite element analysis. At first, they changed the growth substrate from sapphire to silicon carbide (SiC); the SiC chip system exhibited a junction-to-board thermal resistance of 4.4 K/W, outperforming the 9.2 K/W result for the sapphire setup. Next, they used the sapphire chip system to compare the effects of adding thermally conductive adhesive filler, also known as underfill, around solder bumps at the chip-submount interface. The system with underfill displayed a 4 K/W resistance reduction from the “no underfill” package. Finally, they introduced phosphor particles and phosphor coated chips to study the localized heating effects for various phosphor

applications. They found that small phosphor particles can result in local hot spots and excessive temperatures in HB LEDs. Further details of this work can be found in ref [50].

More recently, Ha studied the impact of different layers on the junction temperature of a high power LED using finite element analysis (FEA) [1]. In this work, it was shown that the thermal resistance across the die-attach was sensitive to thermal conductivity and thickness of the layer whereas the thermal interface layer (TIM) was not critically impacted by conductivity and thickness [1]. Although this analysis was not of a flip-chip UV LED, it still provides interesting points. Thermal conductivity and thickness played a major role at the chip-to-substrate connection or die-attach rather than the TIM layer at the substrate-heat-sink interface. This was because the high heat flux near the chip was greatly reduced when it reached the TIM layer, down to 2~6% of the flux at the chip level, due to the heat spreading that occurred in the power electronic substrate, either direct-bonded copper (DBC) substrate or insulated metal substrate (IMS) depending on packaging scheme [1].

2.5 Thermal Management of UV LEDs

Thermal management for UV LEDs is a key design parameter for both package and system level. The efficiency of these devices depends on the junction temperature and the ability of the package to maintain that temperature at a reasonable level. Therefore the main focus of thermal management in UV LEDs is the reduction of the overall package thermal resistance present in the heat path between the *pn* junction and the ambient atmosphere.

There are two paths for heat dissipation; one is up through the sapphire growth substrate and stagnant air, while the more dominant way is conduction through the chip-attached materials and package. Considering the hyper heat flux density at the chip-level,

these materials should not only transfer the heat vertically, but also spread the heat to peripheries rapidly by effective configurations [40].

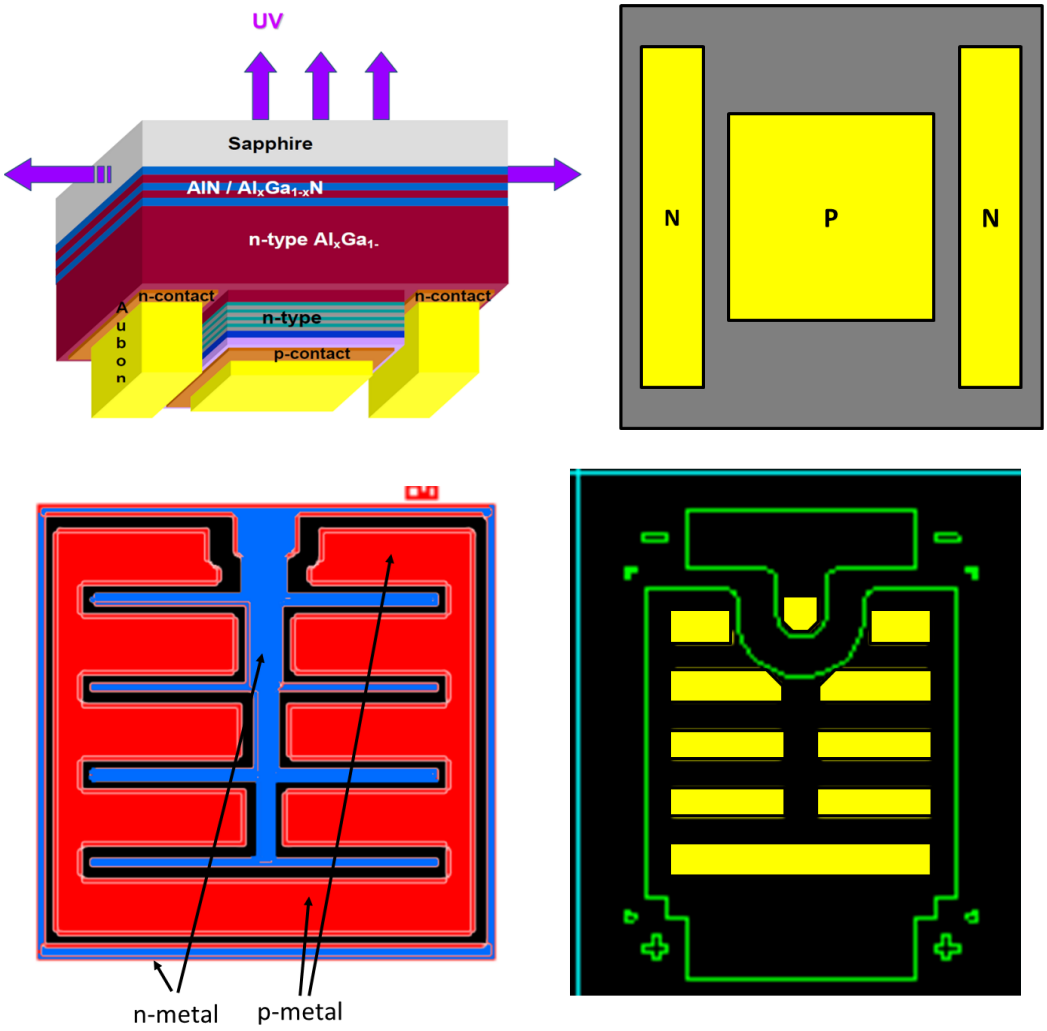


Figure 2.8 Two flip-chip-packaged DUV LED chips, with differing device architectures, on the left along with their respective sub-mounts on the right. The yellow demarcations on the sub-mounts are solder pads and represent the physical footprints of their respective chips.

The extremely high heat-flux present near the chip is one of the main thermal-management challenges in DUV LEDs. Typical lateral area of these chips is 1 mm^2 [1]. Therefore, with an input power of just 1 W, the conductive heat flux in the active region becomes 100 W/cm^2, equivalent to heat from an oxy-acetylene torch at flame tip [51]. This high flux is then transported down through even smaller contact pads, reducing the effective area for heat conduction and creating a thermal bottleneck before the underlying

package can spread the heat, see Figure 2.8. Therefore, effective thermal impedance of a packaged LED can be reduced by increasing the contact cross-section area between the device and sub-mount. However, precautions in device geometry optimization should be taken to avoid lateral current crowding, as it may well result in an increase of the device resistance and hence a reduction of quantum efficiency [48, 52, 53].

Lead Frame Packaging

A prevalent high-power-LED packaging technique, first developed by Lumileds in 1998 and dubbed LUXEON, embeds a metal slug with large volume for heat removal. The lead frame-based plastic (LFP) package has since been adopted by other companies such as Osram and Seoul Semiconductor. Figure 2.9 provides a schematic of the LUXEON LED.

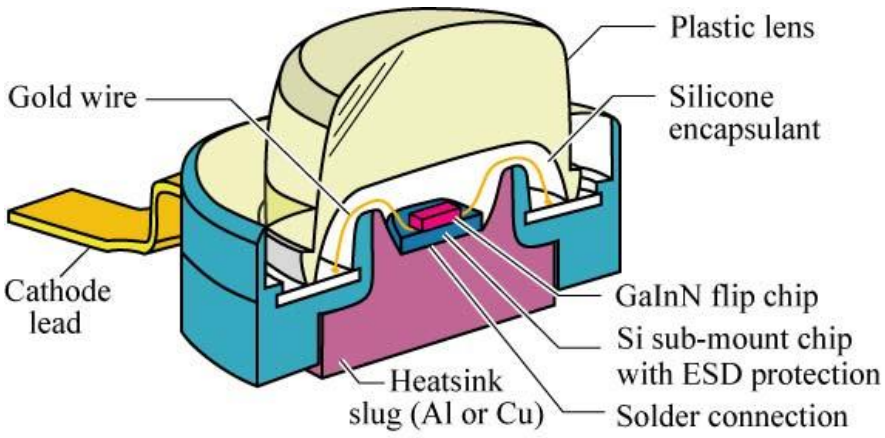


Figure 2.9 Cross section through a high-power package; this package is called Barracuda package, introduced by Lumileds [6].

It is reported that the LFP packaging configuration reduces thermal resistance to 4-10 K/W and can dissipate up to 5W of chip power [40, 54]. Recent improvements in high power packaging for LEDs are highlighted in the LUXEON K2 package released in 2006. The improvements in base material and attach technologies provide a package that

can allow operating junction temperatures of 150 °C for white LEDs and higher (185 °C) for non-white LEDs with forward currents up to 1.5 A, which is 50% higher than its predecessor, the LUXEON LFP package [39, 40].

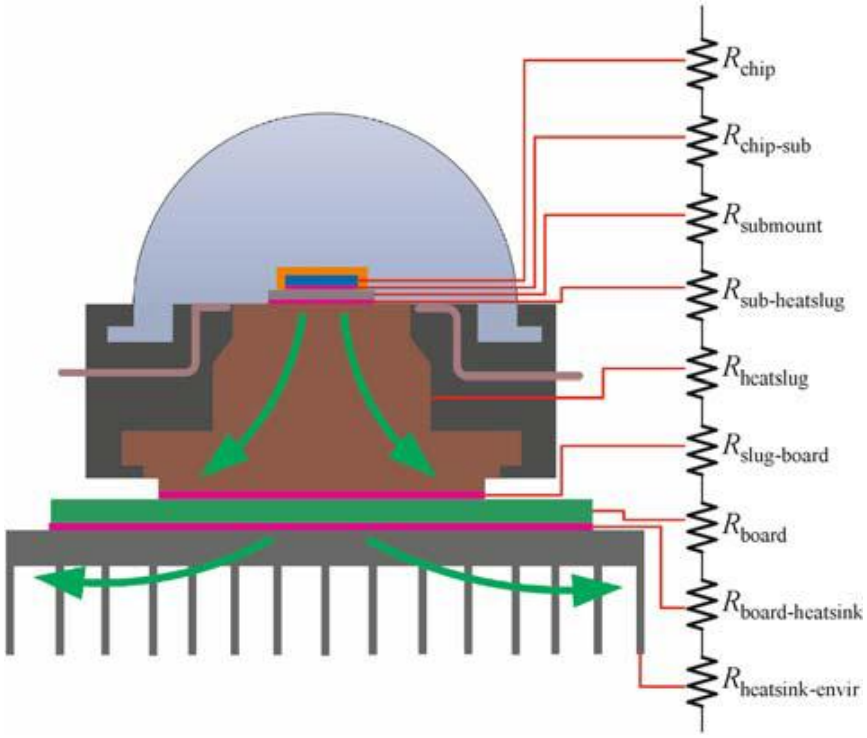


Figure 2.10 Thermal resistance network for the LUXEON LED; the heat slug is soldered to a printed circuit board for efficient heat removal [40].

Thermal resistance networks are generally used to characterize the performance of heat dissipation in these devices; see Figure 2.10 for the thermal resistance network of the LUXEON LED. The overall thermal resistance together with the maximum temperature-of-operation (junction temperature) determines the maximum thermal power that can be dissipated in a package. The total system resistance is the sum of all the resistances shown in Figure 2.10. Note that there are four interface resistances, which remain the main bottlenecks for efficient heat conduction. High system thermal resistance implies that heat cannot be rapidly conducted to the environment and thereby causes a high thermal gradient between the junction and environment.

Chip-On-Board Packaging

A different solution to packaging that does not require a heat slug or a LFP package for high power LEDs is the chip-on-board (CoB) approach. In this method, the chip is directly mounted on a printed circuit board (see Figure 2.11) and can be directly packaged on a heat sink. This leads to a more compact package and allows for a higher packaging density of chips on the same board [1, 40, 55].

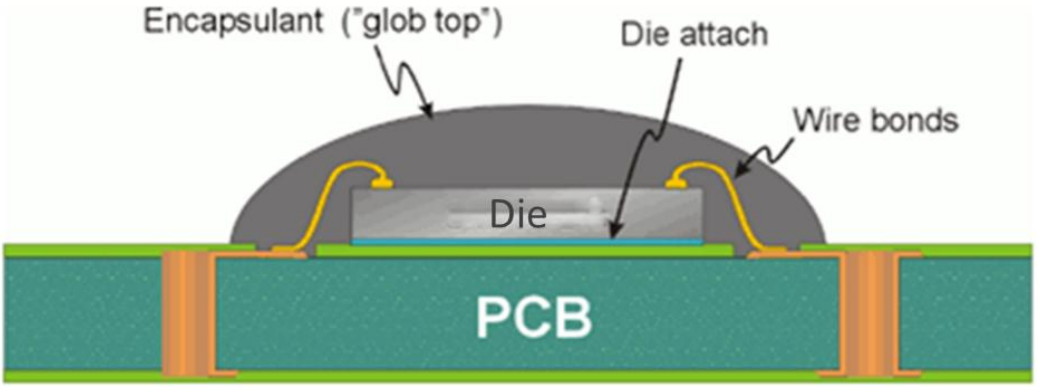


Figure 2.11 Cross-sectional diagram of Chip-on-Board (CoB) packaging [56].

CoB packages have several advantages when compared to LFP packages for high power LEDs. By eliminating the heat slug, a large resistance is removed from the network and thus enables efficient heat conduction to heat sink. The reduction in assembly parts and overall manufacturing processes as well as increased lumen output in a unit packaging area also makes CoB packages more cost effective than LFP packages [1, 40]. Although the CoB scheme removes one bulky material (heat slug) and one interfacial resistance, reducing overall thermal resistance, light intensity control of a large surface light source and thermal dissipation of high density heat flux are still main concerns. Figure 2.12 provides the thermal resistance network for CoB packaging.

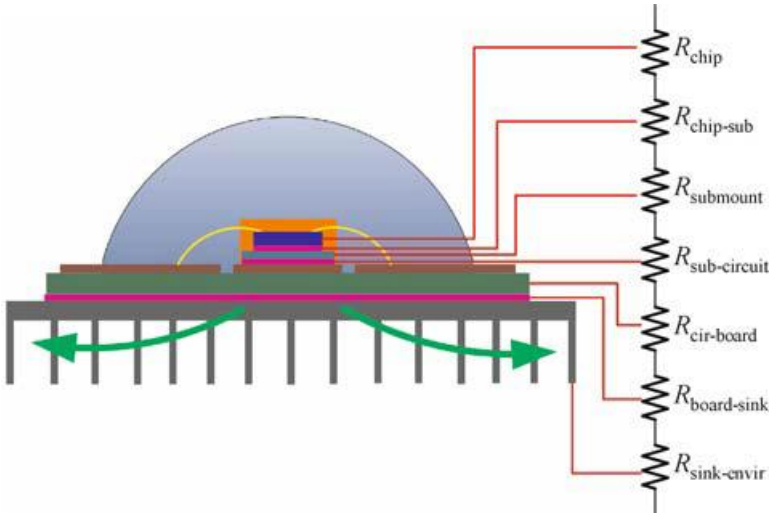


Figure 2.12 Thermal resistance network of CoB packaging technology. The total thickness of CoB is significantly thinner than that of LUXEON; therefore, the system resistance of CoB is believed to be lower than that of LUXEON [40].

In summary, there are three major factors that impact the junction temperature of a high power LED; input power, thermal path, and ambient temperature. High power demands lead to high heat generation in the active region of LEDs. Generated heat must be effectively, both thermally and cost effectively, syphoned away from the LED because high junction temperatures diminish light output, device life, and color integrity. The rate of heat transfer to the outside world is dominated by the temperature difference between the device and the ambient conditions as well as the thermal path from junction to ambient. Therefore the optimum and desired conditions for LED operation are with a low resistance thermal package design operating in low ambient temperatures, thus utilizing the high thermal gradients to increase heat transfer and dissipate high input powers successfully.

CHAPTER 3

FINITE ELEMENT MODELING OF UV-LEDS

3.1 Introduction

The purpose of this chapter is to model the heat dissipation from a flip chipped UV LED and provide an understanding of the most critical factors within the packaging architecture that impact the junction-to-air thermal resistance. The software package COMSOL Multiphysics was used to study the effects of the package architecture on junction temperature and overall thermal resistance in addition to thermal stress in a UV LED package. The main bottlenecks for heat dissipation are identified and alternate solutions are presented. Although the main package analysis was done with an interdigitated chip configuration, the micro-pixel configuration was also analyzed with a focus on the impact of pixel density on the thermal response of the packaged device.

3.2 Rational for Thermal Analysis of UV LED Packaging

As discussed in Chapter 2, the flip chip bonding architecture required for deep UV LEDs provides severe limitations to the heat conduction path for dissipating thermal energy; this is primarily through the *p* & *n* contacts into the substrate materials below. However, the size of the *p* & *n* contacts cannot be chosen arbitrarily as the issues of poor p-GaN doping and current crowding must also be addressed by judiciously spacing the *p* & *n* regions. This is achieved through the creation of interdigitated fingers or micro-pixel geometries. With these limitations in mind, there is a need to explore the impact of the

remaining variable attributes of the packaging architecture to determine which have the greatest impact on packaging thermal resistance and device performance. This includes contact metallization, thermal spreading sub-mounts, the use of lead frame packages, and power substrates.

3.3 Thermal Package Design & Modeling

Heat transfer modeling was used to investigate the effect of power input, power distribution, and device dimensions on maximum device temperature and temperature distribution in the package. The heat diffusion equation, derived from the conservation of energy and Fourier's law of heat transport, first documented in Fourier's *Théorie analytique de la chaleur* in 1822 [2, 57, 58], was solved in COMSOL; refer to Eq. 3-3.

3.3.1 Device Structure

The UV LED structure analyzed in this work was a flip-chipped device that was mounted to a lead frame package, as described in Chapter 2. For modeling simplicity and to save simulation time and memory, only the thermal package below the p-contacts, without the chip & growth substrate, was modeled. The LED chip itself is approximately 1 μm in thickness and heat flows away from the growth substrate, therefore the model was simplified. Justification for eliminating the growth substrate from the model is provided in Section 3.3.3. Figure 3.1 presents the simplified device structure.

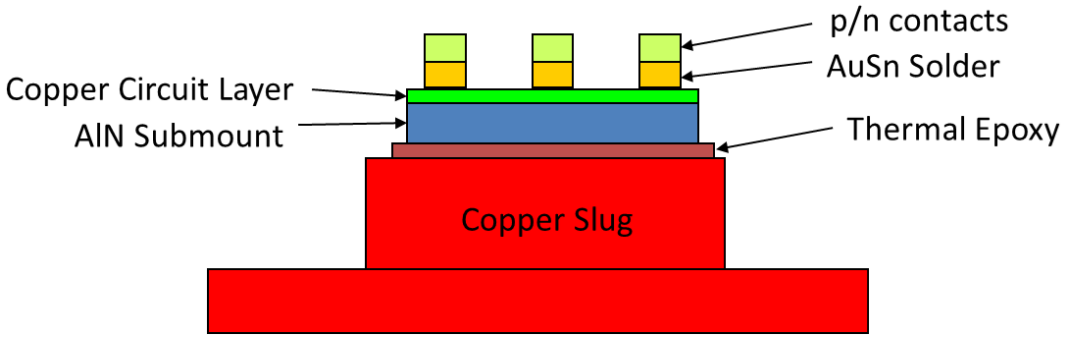


Figure 3.1 Schematic of the simplified flip-chipped UV LED model placed atop a copper heat slug. The p & n contacts have an interdigitated multifinger configuration.

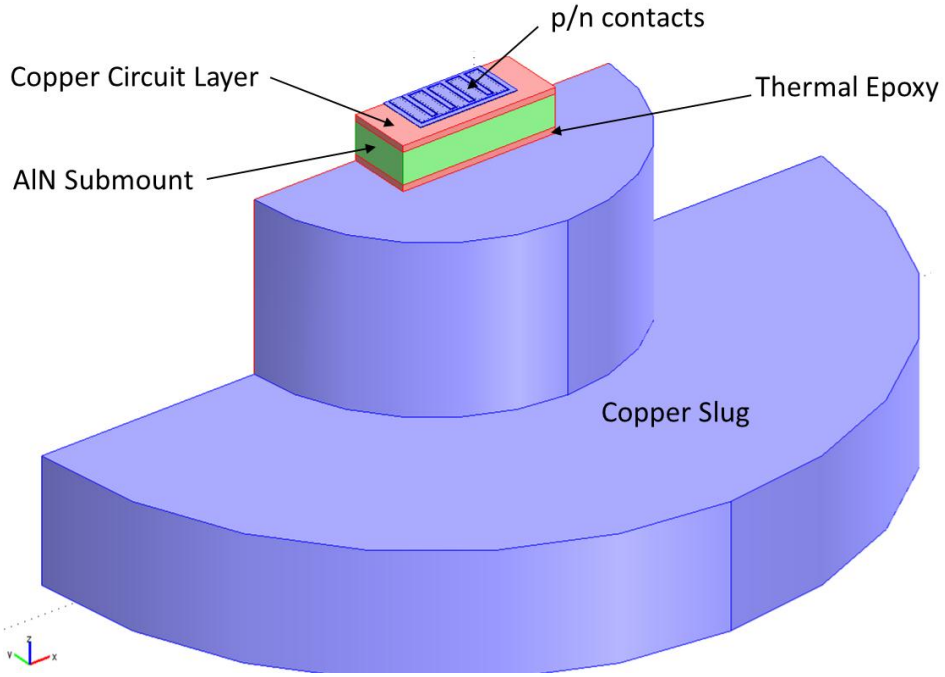


Figure 3.2 Model geometry created in COMSOL. Note the AuSn solder pads are not labeled because it is not visible; there are rectangular solder pads under the p-contacts.

Figure 3.2 shows the model configuration built for the finite element analysis. Half symmetry was employed to save processing memory and reduce simulation time. A noteworthy simplification of the model was the copper circuit layer; it was modeled as a continuous layer whereas in reality it would have etched traces separating the *p* and *n* currents and preventing an electrical short when the device is powered. This generalization, although a bit unrealistic, serves to model the best case scenario for heat

removal, where the copper layer is continuous in the package. This simplification is justified later in this chapter. Note the interdigitated geometry of the metallizations and device used in the model, as discussed in Chapter 2.

3.3.2 Thermal Simulation Methodology and Setup

The primary modes of heat transfer are conduction, q_{cond}, through the layers and natural convection, q_{conv}, at the boundaries, which are governed by

$$q_{cond} = -kA\frac{\partial T}{\partial \xi} \tag{3-1}$$

$$q_{conv} = hA_s(T_s - T_\infty) \tag{3-2}$$

where k is thermal conductivity, A is the cross-sectional area normal to the direction of heat conduction, $\delta T/\delta \xi$ is the temperature gradient, ξ is the directional vector of heat flow, h is the convective heat transfer coefficient, A_s is the convective surface area, T_s is the surface temperature, and T_∞ is the ambient temperature.

As previously stated, the heat diffusion equation was solved in COMSOL to determine the temperature distribution throughout the UV LED package. The governing equation is given by

$$Q_{vol} = \rho C_P\frac{\partial T}{\partial t} + \nabla \cdot (-k\nabla T) \tag{3-3}$$

where ρ is density (kg/m^3), C_P is specific heat capacity (J/(kg·K)), T is temperature (K), k is thermal conductivity (W/(m·K)), t is time (s), and Q_{vol} is the volumetric heat generation (W/m^3).

For studying the thermal resistance of the package, a simple modeling approach was considered; a heat source at the p-contacts, conduction through the package layers and a specified base temperature with all remaining external surfaces modeled as

adiabatic (see Figure 3.3). Thermal resistance analysis is further discussed in Section 3.3.4.

Modeling Setup

The main device dimensions used for the model are described here, with changes described throughout when necessary. Device dimensions used are of a commercial AlGaN/GaN based DUV LED provided by industry partners. The vertical temperature distribution through the device provides good insight into the thermal resistance and performance of the package, therefore the layer thickness, in the z-direction, is the dimension of interest. Similarly since a majority of the heat generated is removed through conduction, thermal conductivity of the different layers was also important. Table 3.1 contains the z-axis thicknesses as well as the thermal conductivities used in the FEM.

Table 3.1 - Thermal conductivity and thickness data of materials used in the general model

Material	Thermal Conductivity	Thickness
Au (Gold Contacts)	317 W/m-K	4 µm
AuSn (Gold-Tin Solder)	57 W/m-K	4 µm
Copper (Circuit Layer)	401 W/m-K	50 µm
AlN (Aluminum Nitride)	285 W/m-K	254 µm
Thermal Epoxy (TIM)	3 W/m-K	50 µm
Copper (Heat Slug)	401 W/m-K	2.392 mm

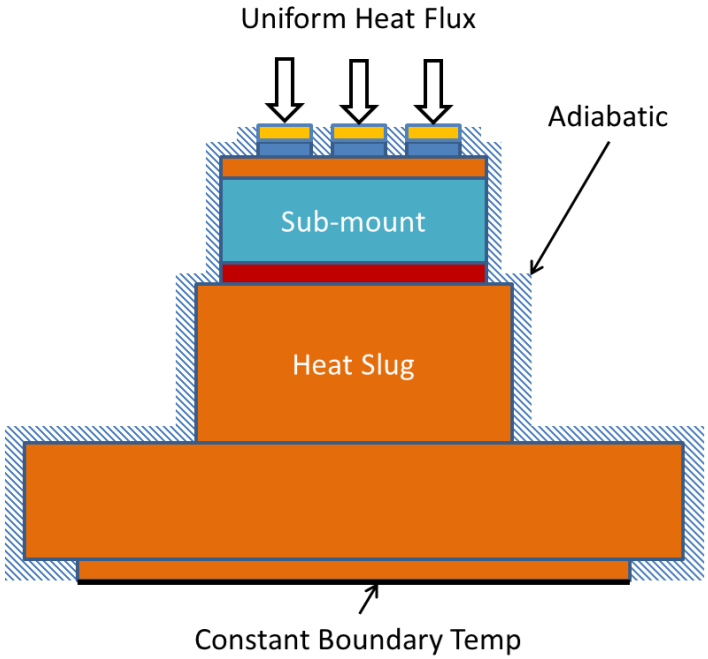


Figure 3.3 Boundary conditions used in main study; uniform heat flux on top of the p-contacts, constant boundary temperature on the bottom of the copper slug, and adiabatic on all other surfaces. Continuity was assumed at all the interfaces.

The base of the copper slug was set to a constant temperature of 298.15 K (25 °C) or room temperature. All other outer boundaries were modeled as adiabatic. The heat source was modeled as a downward flux on the p-contacts; a flux of 230 W/cm^2 was used, corresponding to a power of 800 mW at an input current of 100 mA, which was consistent to experimental levels that showed significant joule heating.

3.3.3 Neglecting Growth Substrate and Die in Model

Since the UV LED chip along with the metallization layer only totals to approximately 4 microns in thickness, such aspect ratios become very difficult to mesh. In order to neglect the chip and growth substrate and only focus on the lower part of the package, a study was conducted on the impacts of those layers on the junction temperature.

Three models were developed; the first includes an AlN growth substrate and the GaN chip, the second only includes the GaN chip, and the third model excludes both. For

the first two simulations where the heat generating region is embedded in the geometry, the GaN chip was assigned as the heat generating region whereas the third model employed a downward heat flux, equal to the heat generated in the first two models, into the package because the top layers were removed and heat could be applied directly to the p-contacts. The simulation results for all three configurations can be found in Figure 3.4. It shows that the junction temperature goes from 313.01 K to 312.1 K, a 0.91 K difference, for the model without the chip versus the one with the GaN layer. Also, the junction temperature goes from 312.1 K to 310.99, a 1.11 K difference, when the AlN growth substrate and the chip are included in the model versus when it's just the GaN chip in the model.

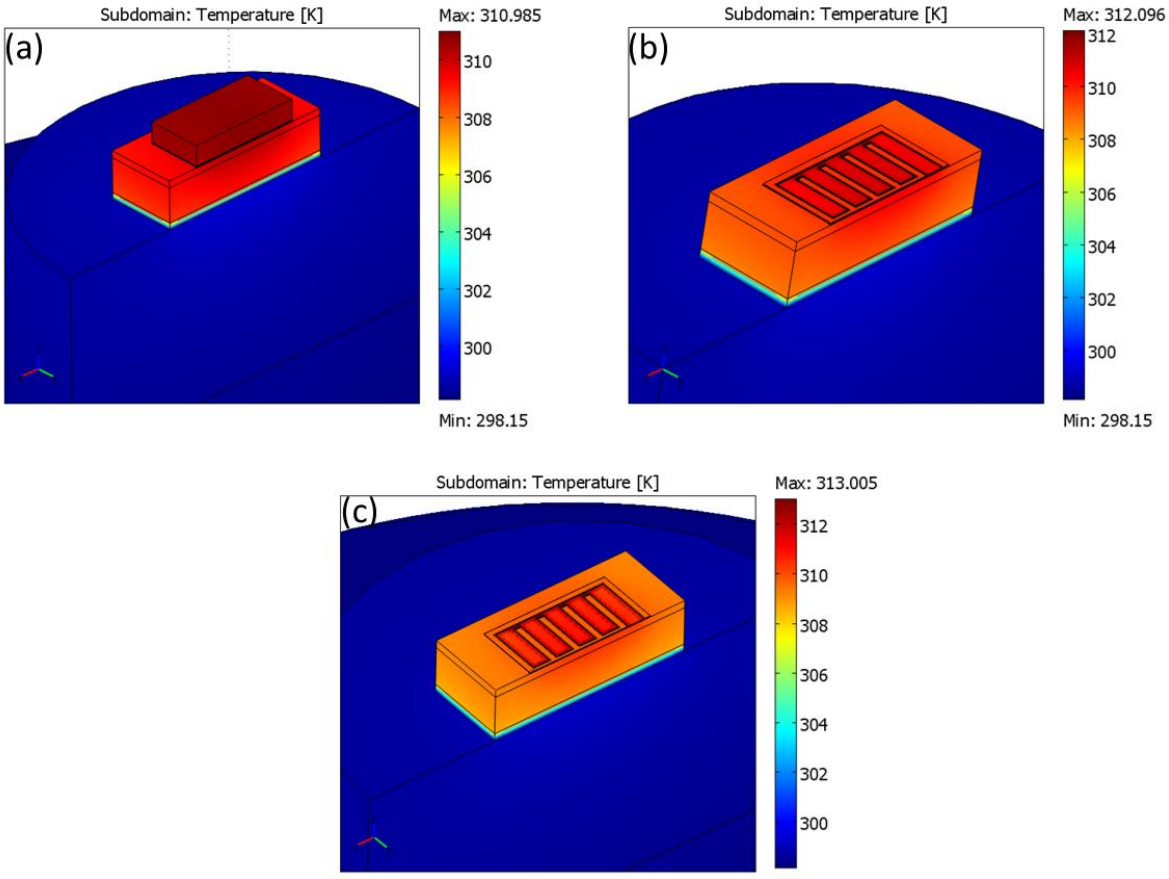


Figure 3.4 (a) Temperature distribution of model with growth substrate and die. (b) Results of model with just the GaN chip and (c) results from model without GaN chip or AlN submount.

The results suggested that the growth substrate and the chip itself have a minor impact, around 1 K, on the junction temperature. This is because the majority of the heat travels through the thermally conductive package below the junction rather than above it. Therefore, the growth substrate and GaN chip were neglected for the remaining studies, and only *p*/*n*-contacts-and-below were modeled, same as shown in Figures 3.1 and 3.2.

3.3.4 Thermal Resistance Analysis

A common way of gauging the thermal implications of various packages is through comparisons of the operating junction temperatures offered with differing packages. This method simply shows which package achieves a lower peak temperature but it is unable to show why; meaning one cannot necessarily determine the reason for better performance based on simply maximum temperature. In order to evaluate why one package is better than another, a deeper study of the thermal performance of the subcomponents must take place. This determines the major factors and layers that play a big role in heat dissipation. As such, thermal performance of UV LED packages is assessed using the concept of thermal resistance networks and thermal resistance analysis. The thermal resistance is quantified by Eq. 3-4.

$$R_{th} = \frac{\Delta T}{Q_{in}} \tag{3-4}$$

where R_{th} is thermal resistance across a layer, ΔT represents the temperature difference between two opposite surfaces of a layer, and Q_{in} represents the total heat load entering the layer. Thermal resistance based on maximum surface temperatures gives simpler and clearer understanding of the heat spreading effect in these packages rather than using the average temperature of interfaces [1]. Therefore the thermal resistance analysis for the

UV LED package presented in this chapter will use the maximum temperatures of interfaces to calculate thermal resistances of different layers.

Also as mentioned in [2] and [1], the effect of using temperature independent thermal conductivities under predicts the junction temperature of devices because at high input powers and high operating temperatures, the thermal conductivity of most materials decreases as temperature increases. However since the simulations in this case are low power, less than 1 W, the use of constant temperature thermal conductivities can be used with minimal error [2]; the effect on overall thermal resistance is not significant.

3.3.5 Results: Impact of Submount Size and Conductivity

A very important and significant function in heat removal of these devices is the heat spreading influence of the AlN submount. As the majority of the heat generated flows through the submount at high heat densities, it is important to spread the heat in this layer and reduce the heat flux into the remainder of the package.

AlN, a covalently bonded ceramic, exhibits high thermal conductive properties while remaining a strong dielectric; this is an unusual and attractive combination. In dielectric materials, heat is transferred in the form of lattice vibrations (phonons) also known as phonon conduction. Anything that impinges on the phonon propagation through the solid has negative influence on thermal conductivity of the solid. Temperature, impurities, pore size and distribution, grain size, compositional homogeneity and orientation affect the mean free path for phonon conduction [59, 60]. Thus while theoretical thermal conductivity of AlN is about 285 W/m-K at 300 K, typical values for polycrystalline AlN are significantly lower and vary from 140 – 180 W/m-K, depending upon the processing conditions and purity. The simulations in this work assumed high purity AlN and used the intrinsic value of 285 W/m-K, whenever the conductivity of the submount was fixed.

A parametric study was conducted examining submount design parameters to determine the influence of lateral size, thickness, and material property on the overall thermal resistance of the UV LED package. Again, the symmetry associated with the structure allows for simulation of half the domain. Figure 3.5 shows the structure of the device and package used in the parametric study. As previously mentioned, the model consists of interdigitated *p* & *n* contact pads to which gold-tin solder is applied allowing the device to be attached to the copper circuit layer on top of the submount. The submount is then attached to the copper slug with the use of thermal epoxy as the thermal interface material (TIM). The corresponding thickness value of each layer is also indicated in Figure 3.5a. Three parameters of the submount were considered for the simulations, namely, lateral area dimensions, vertical thickness, and thermal conductivity were varied to study their effects on thermal resistance.

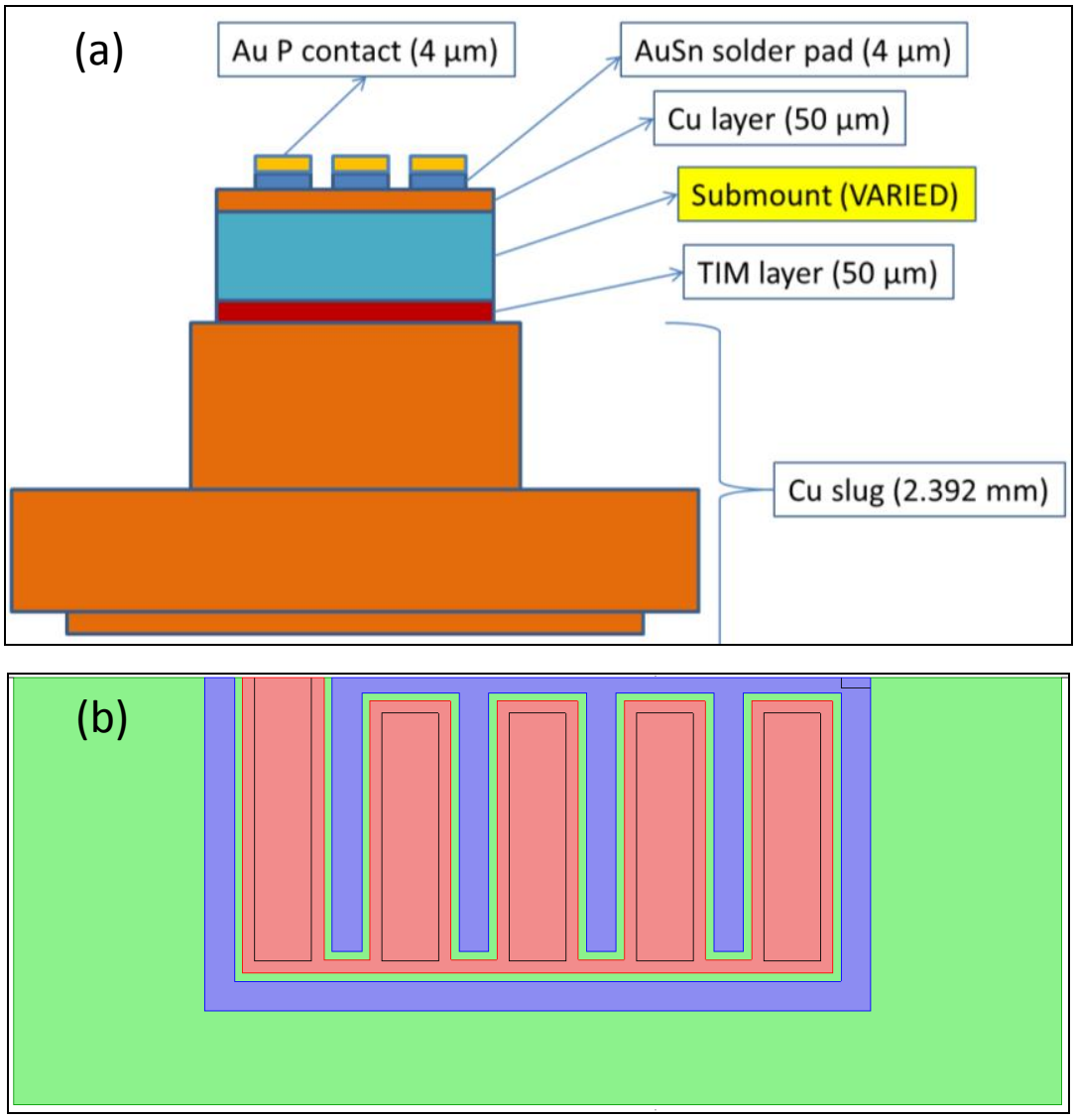


Figure 3.5 (a) Cross-sectional view of model used for submount optimization including the thicknesses of layers and (b) top view of the structure showing the interdigitated configuration.

Figure 3.5b shows the top view of the half symmetry model. The red region represents the *p*-contact pads and the blue represents the *n*-contact pads. The rectangular pads with the black outlines represent the AuSn solder pads under the *p* & *n* contacts. The green region is the copper circuit layer that sits on top of the submount.

As depicted in Figure 3.3, the boundary conditions for this simulation were as follows: 1) Constant temperature was assumed at the base of the copper slug. 2) All other outer boundaries were insulated and modeled as adiabatic since the losses from the sides

were assumed to be negligible and only the conduction through the package was relevant in this study. 3) A heat source of 229.75 W/cm^2 corresponding to 400 mW of power through *half* of the device was concentrated on top of the *p* contacts; 400 mW through half of the device is consistent with the 800 mW power level discussed earlier. The thermal conductivities of the materials used in this model are listed in Table 3.2.

Table 3.2 - Thermal conductivity of materials used in the finite element model.

Material	Thermal Conductivity
Au	317 W/m-K
AuSn	57 W/m-K
Cu	401 W/m-K
Epoxy	3 W/m-K

As a first step to evaluating the impact of the submount on the overall thermal resistance, an area ratio (AR) was defined as displayed in Eq. 3-5,

$$AR = \frac{Area\ of\ the\ submount}{Area\ of\ LED\ die} \tag{3-5}$$

Next, the relationship between material property of the submount and its thickness was considered. Evaluation of the system thermal resistance variation as a function of the submount thickness with varying submount thermal conductivities is shown in Figure 3.6, for an AR of 1. Thermal conductivity was varied from 100 W/m-K to 1000 W/m-K by 100-W/m-K increments and the thickness was varied from 50 µm to 500 µm by 50-micron increments. Note that in all the simulations, the lateral areas of the top copper circuit layer, the submount, and the bottom TIM layer were kept equal to each other; meaning all three layers were altered together.

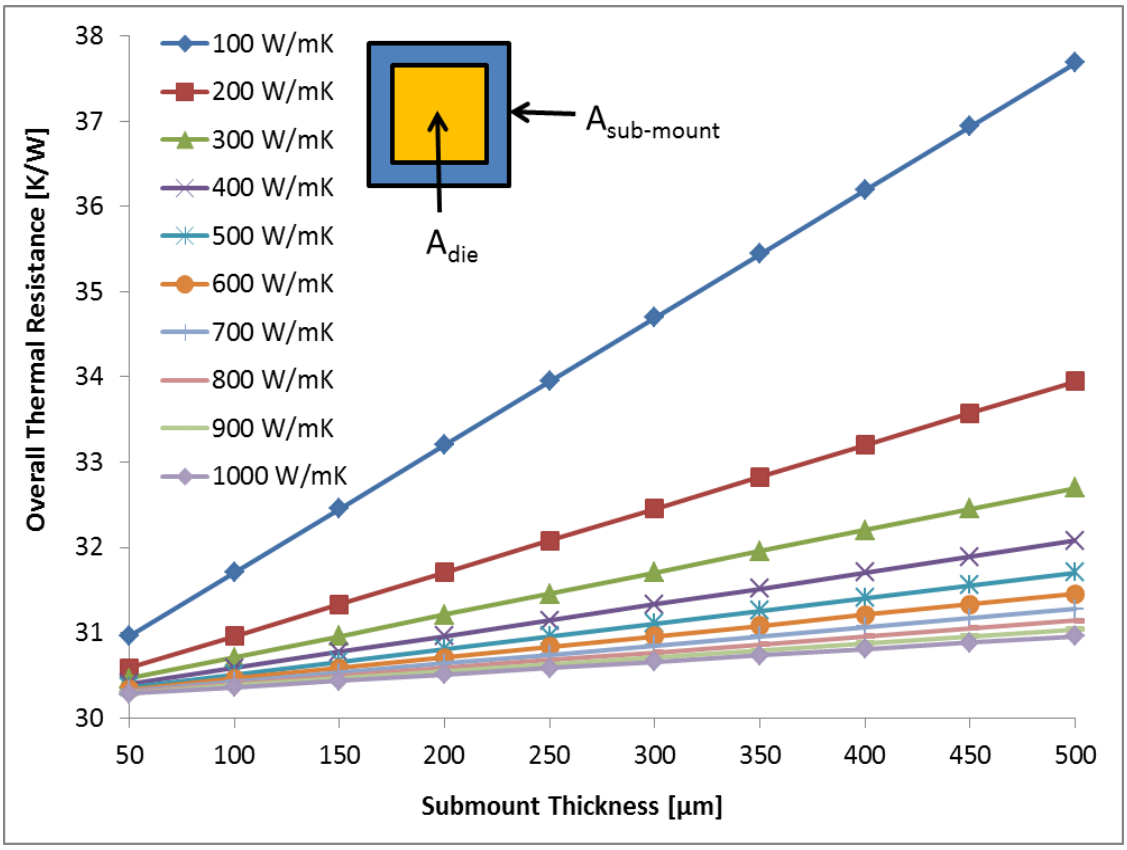


Figure 3.6 Thermal resistance of package as a function of submount thickness for various submount thermal conductivities. Note, submount and die have the same lateral area size; AR=1.

For a 900-W/m-K enhancement in the thermal conductivity of the submount, the thermal resistance varied most drastically for thicker submounts. For example, at a thickness of 50 microns, the thermal-resistance drop from using a 100-W/m-K submount versus a 1000-W/m-K submount was 0.671 K/W as opposed to a 6.731 K/W reduction at a thickness of 500 microns. Moreover, for a given thickness, the largest reduction of thermal resistance occurred when conductivity was increased from 100 W/m-K to 200 W/m-K. Again this trend was greatest for thicker submounts; for a 500-micron thick submount, the increase of conductivity from 100 W/m-K to 200 W/m-K offered a reduction of 3.742 K/W as opposed to 2.989 K/W reduction when conductivity was increased from 200 W/m-K to 1000 W/m-K. This indicated that the submount material and thickness have an impact on the thermal resistance of the package, which also meant

an impact on the junction temperature of the UV LED. From the plots shown in Figure 3.6, it was concluded that a thinner submount was more important on reducing the overall thermal resistance of the package than a high conductivity material. Based on the modeled geometry, thermal conductivity did not show a significant impact after about 300-400 W/m-K; this meant that AlN (180 W/m-K [61]) or SiC (370 W/m-K [1]) will suffice in this configuration.

Figure 3.7 shows the impact of submount thickness for varying AR values, at a fixed thermal conductivity of 400 W/m-K. For this investigation, AR was varied from 1 to 5; 5 meaning the submount was 5X larger in lateral area than the die, with the die always in the center. Thickness was varied from 100 µm to 500 µm in 100-micron increments.

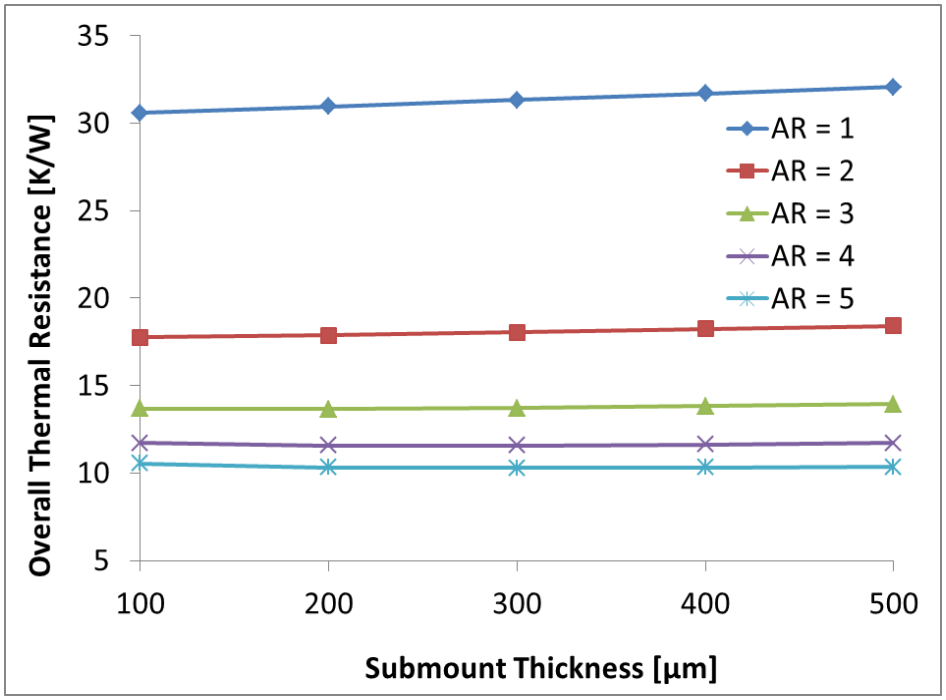


Figure 3.7 Effect of varying AR and thickness of a specific material (k = 400 W/m·K).

It was shown that increasing submount-to-die AR significantly decreases the system thermal resistance. For low ARs, the thermal resistance was a positively

increasing linear function of the submount thickness. However, this relationship is lost when the area factor is increased. Additionally, with higher ARs, thinner submounts present higher thermal resistances. This effect can better be seen in Figure 3.8, where the thermal resistance was plotted as a function of AR for the thinnest and thickest submount, with an arbitrarily selected thermal conductivity of 400 W/m-K. The thin (100 µm) submount offers smaller thermal resistances for ARs ≤ 3, and larger thermal resistances for ARs 4 and 5, when compared with the thick (500 µm) submount.

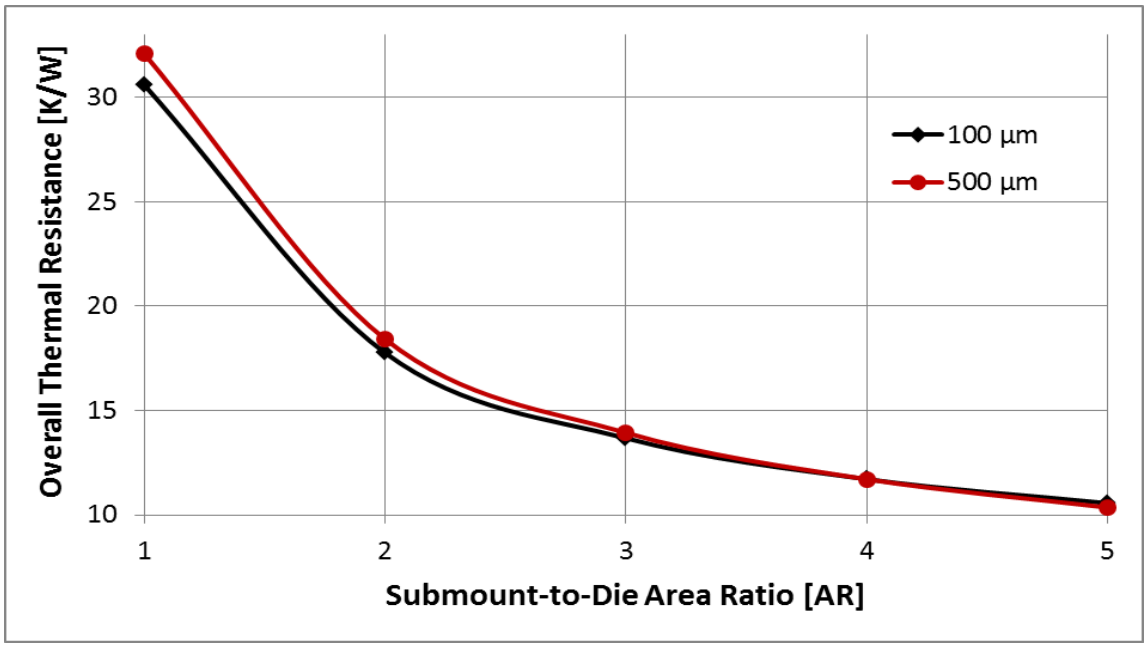


Figure 3.8 Thermal resistance as a function of area ratio for 100 µm and 500 µm sub-mounts. Both sub-mounts have a thermal conductivity of 400 W/m-K.

The highest change in the thermal resistance occurred when the area of the submount was increased to twice the die area; for example, when the 100-micron submount AR was increased from 1 to 2, the thermal resistance decreased by 12.83 K/W. However the overall thermal resistance only decreased by 7.2 K/W when the AR was increased from 2 to 5. The implication of this is that when the submount AR was increased from 1 to 2, the lateral heat-spreading potential was the largest and beyond

some critical AR, the overall thermal resistance becomes independent of the lateral area of the submount. As such, larger ARs have a "redundant area" [1], which plays a negligible role in spreading the heat and reducing flux due to the fact that heat spreading occurs over a limited area [1].

Figure 3.9 also shows the overall thermal resistance plotted as a function of increasing submount-to-die AR. The plot compares two submounts with differing material properties, one with a conductivity of 200 W/m-K and the other with a conductivity of 1000 W/m-K; both are 200 µm in thickness. Again, the lateral dimensions of the submount were varied for a fixed submount thickness.

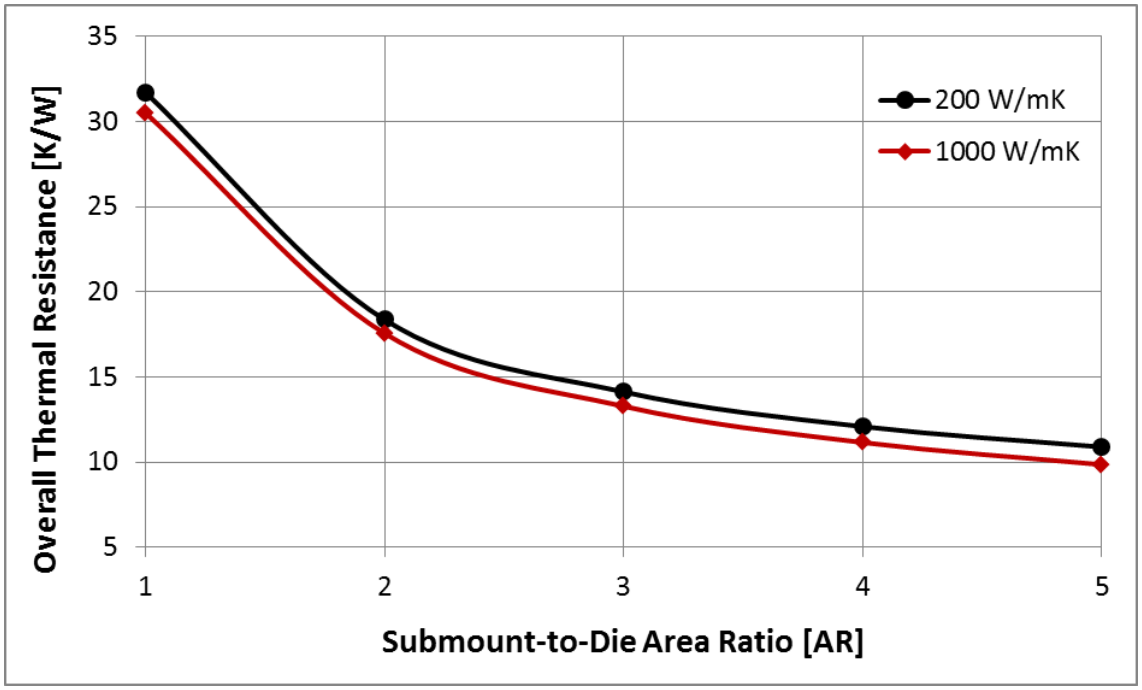


Figure 3.9 The variation of the system thermal resistance with increasing submount-to-die area ratio for two submounts of equal thickness but opposing thermal properties.

The largest reduction in thermal resistance again occurred when the area ratio was increase from 1 to 2. Figure 3.9 suggests that material property had a small impact on overall thermal resistance. The biggest factor to reducing resistance seems to be the ability to spread the high heat density from the chip and reduce the high flux into the

package. *The parameter that had the biggest impact on this ability was the aforementioned submount-to-die area ratio.*

To briefly summarize, the submount-to-die area ratio appeared to have a greater effect on overall package thermal resistance than the submount thickness or the submount thermal conductivity. Based on the structure studied in this section, it is best to choose a thinner submount that is at least twice the lateral area of the die but not greater than three times the die area. If those two parameters are fulfilled, then there is much freedom in the material chosen for heat removal. In the same token, an AR between 2 and 3 with a submount thermal conductivity above 200 W/m-K affords much flexibility on the thickness of the submount. Other aspects of the package will be discussed in the following sections to ascertain their effect on the overall thermal resistance of the package.

3.3.6 Results: Impact of Additional Packaging Components

Multiple geometrical and material-selection based variations were analyzed to determine their respective influences on the thermal performance of the UV LED device. Explanation and interpretation of each analysis accompanies each subsection. Several recommendations are also presented based upon the analysis. The impact of these additional components was evaluated using device peak temperatures rather than package thermal resistance.

The overall device configuration and boundary conditions remained as presented in Figure 3.5, in Section 3.3.5. The notable difference in this section was that the submount had a specified material and geometry; the submount-to-die AR was approximately 2, thickness was set to 254 µm, and conductivity was 285 W/m-K (AlN).

A device power level of 800 mW was used. All external boundaries except the bottom face were modeled as adiabatic boundaries. The bottom face was fixed at approximately room temperature, 25 °C or 298.15 K. The dimensions and material

properties for each component are the same as given in Figure 3.5 and Table 3.2 of Section 3.3.5. Since half-symmetry was again utilized in this series of studies, 400 mW of power through half of the device, represented by a 230 W/cm^2 downward heat flux, was placed on the *p*-contact pad; see Figure 3.10. To further reduce computational effort, meshing optimization was investigated. Figure 3.11 presents the meshing strategy used in this model. Multiple mesh refinements were analyzed to ensure the fewest elements without appreciable variation in numerical solutions.

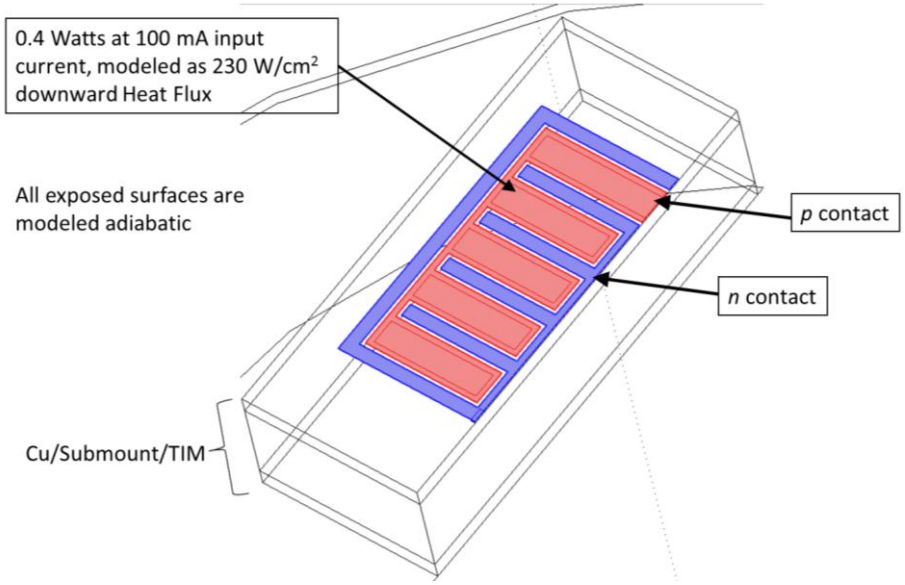


Figure 3.10 Interdigitated configuration with major components labeled.

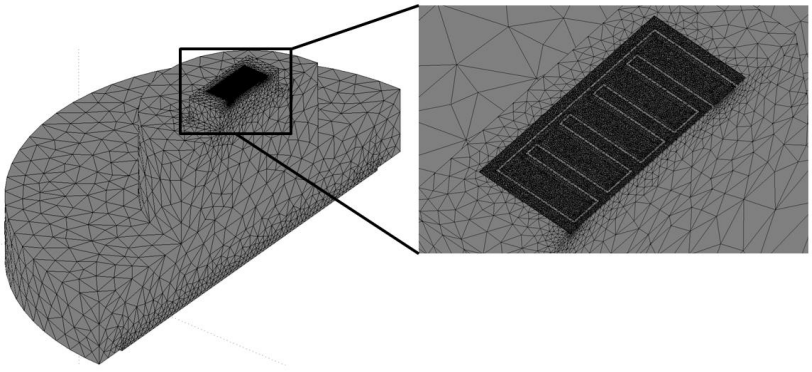


Figure 3.11 Meshed finite element model. Note the increased mesh density in the region of interest.

A schematic of the initial results representing the thermal resistances for each layer is presented in Figure 3.12. The most resistive layer was determined to be the thermal epoxy used as the interface material between the AlN sub-mount and the copper slug. The epoxy layer had a thermal resistance of 12.45 K/W. These layers present opportunities for significant potential improvement through alternate material selections and geometrical optimization. Similar conclusions can be drawn for the less thermally resistive copper layers.

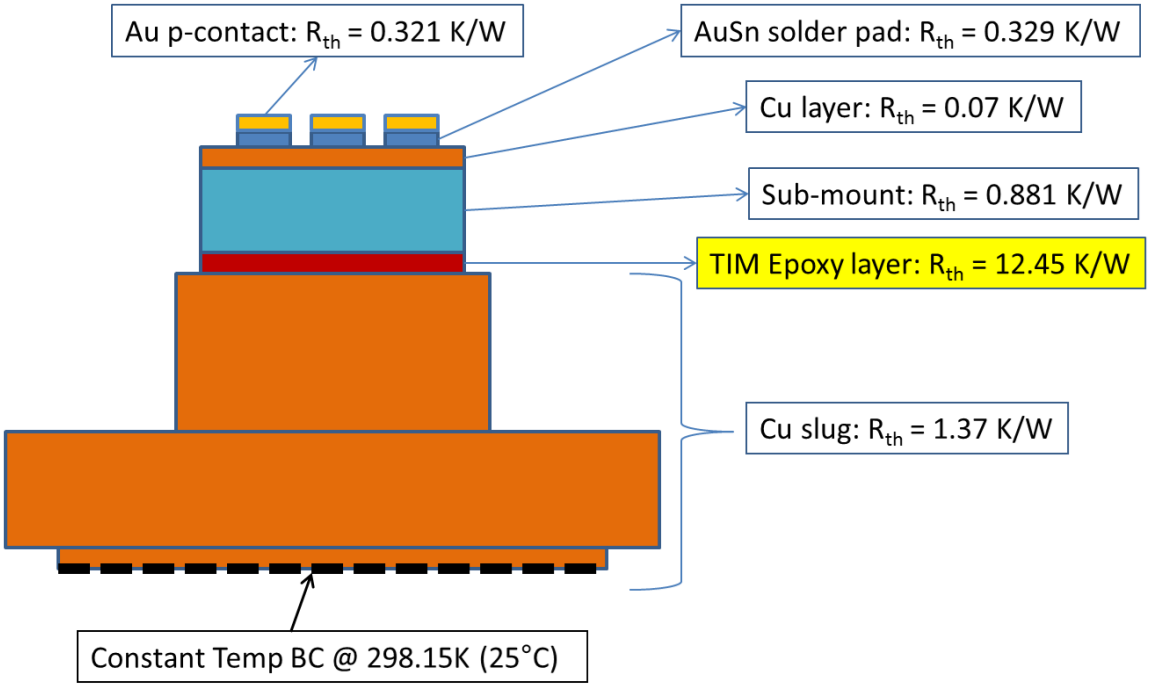


Figure 3.12 Thermal resistance contributions of package components.

3.3.6.1 *P* and *N* Metallization and Solder Pad Materials

The first set of studies consisted of the *p* & *n* metallizations and solder pads. The use of Au (Gold) and AuSn (Gold-Tin) as the material for the contact metallization was investigated. Figure 3.13 provides the results from the two material combinations. The less conductive and thus more resistive AuSn contact material yielded a higher maximum temperature; a 9.13 K difference. Moreover, higher temperature gradients in critical

connections on the periphery of the p-contacts were observed. Thermal distributions throughout the p-contacts were more uniform through the use of Au as the contact material and overall package thermal resistance was reduced by 11.4 K/W.

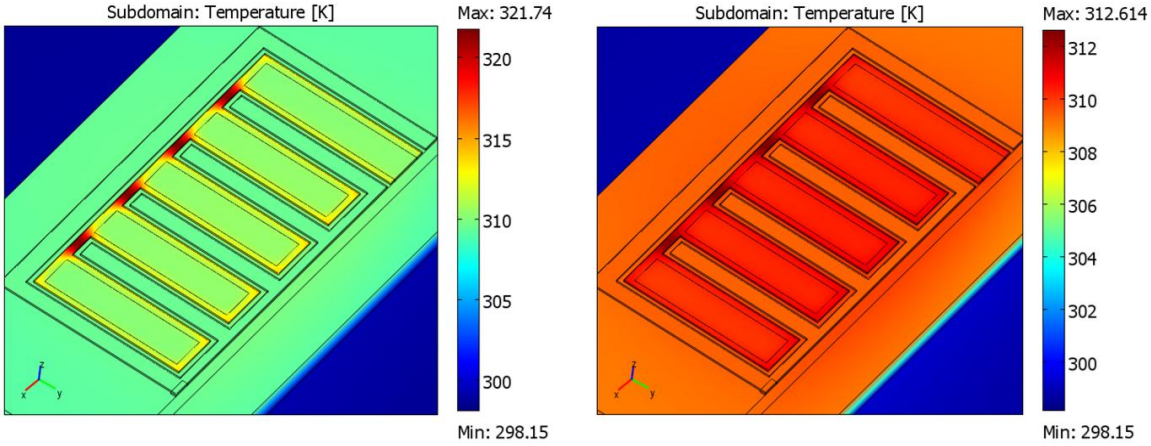


Figure 3.13 AuSn (left) vs. Au (right) electrodes, both with AuSn solder pads.

The reduced maximum temperature can be attributed to the increased thermal conductivity of Au as compared with that of AuSn; 317 W/m-K versus 57 W/m-K. The gold contacts quickly spread the heat whereas there's much resistance in the structure with AuSn contacts, resulting in high thermal gradient across the *p* contact surface. These thermal gradients in the p-contact connections can potentially have profound implications on the lifetime expectations, as these reduced cross-sections are repeatedly heated to elevated temperatures well above the temperatures achieved through the use of Au contacts.

The influence of using a solder material with a higher thermal conductivity than the AuSn solder is illustrated in Figure 3.14. Au-Au bonding which uses gold solder and has a thermal conductivity of 317 W/m-K versus 80Au-20Sn solder, which has a conductivity of 57 W/m-K [1, 62-66]. The thermal behavior was nearly identical in both packages, except for the slightly higher maximum temperature, only by 0.52 K, with the AuSn solder pads, translating to a 0.65 K/W reduction in overall thermal resistance.

These results indicated that the use of AuSn solder pads will suffice instead of using a higher conductivity solder like gold-gold bonding.

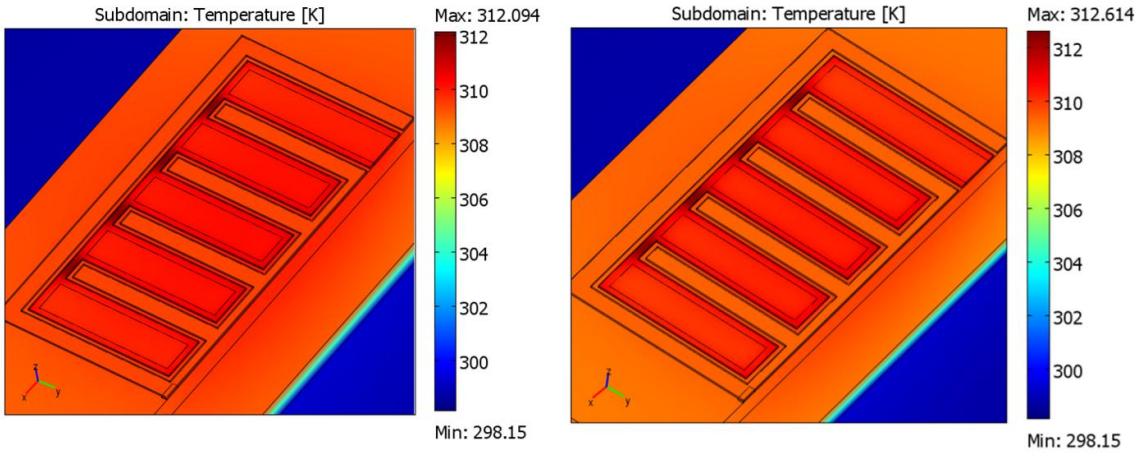


Figure 3.14 Au (left) vs. AuSn (right) solder pads, both with Au as their p & n metallizations.

3.3.6.2 Examination of Top Copper Circuit Layer

Next, the simplification made earlier in the copper circuit layer was investigated. The purpose of this analysis was to determine the precise contribution to thermal management from the copper layer and justify the use of a non-etched copper layer. Therefore, the top layer material was reduced and an interdigitated copper layer was constructed and shown in Figure 3.15; exactly matching the pattern of the *p* and *n* metallizations. The maximum temperature in the package with an interdigitated copper layer increased by less than 0.1% or 0.29 K, when compared to a package that had a top layer with contiguous copper. This was a 0.36 K/W reduction in thermal resistance which demonstrated that the additional copper material was essentially insignificant from a thermal management perspective, and the excess copper could be removed from the wire-bonding pads without appreciable increases in temperature rise.

One more consideration was taken concerning the top copper layer, to understand its impact on the maximum temperature. The approach of copper reduction was extended to the total removal of the copper layer. The copper layer was removed from the

COMSOL model and the temperature distribution was analyzed. The solder pads were directly connected to the AlN sub-mount. From Figure 3.16, it can be determined that the structure with no copper layer had a maximum temperature 0.26 K (< 0.1%) lower than the case for a structure with a non-etched, contiguous copper. This suggests that the top copper layer is not a significant contributor to the high junction temperatures of UV LEDs.

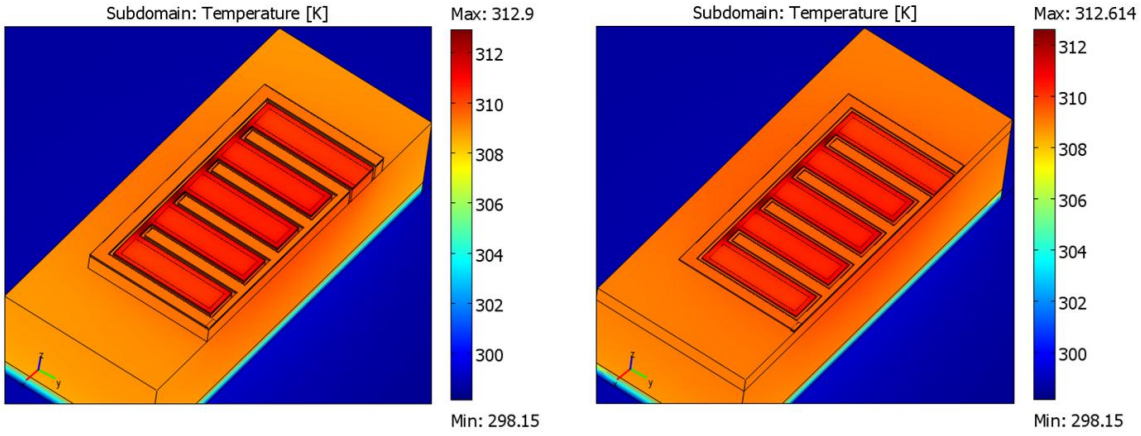


Figure 3.15 Interdigitated top copper layer (left) versus contiguous copper (right).

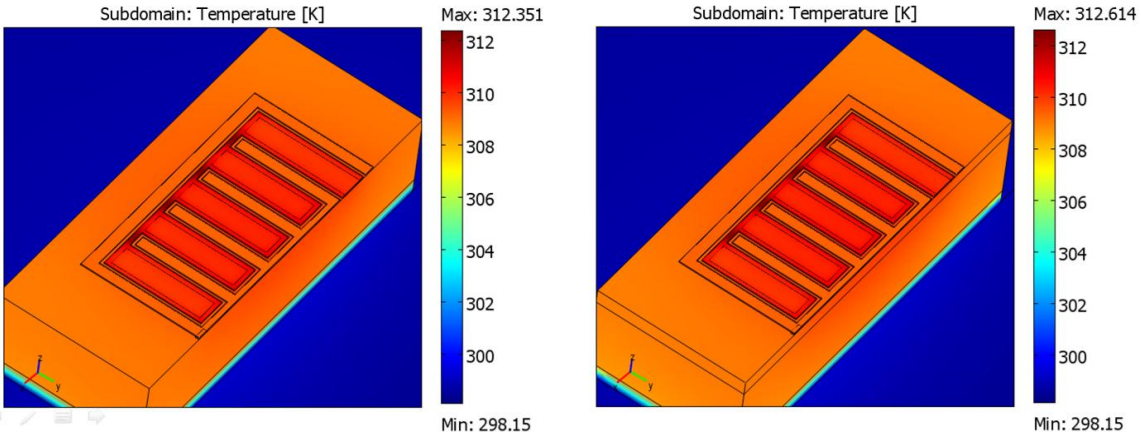


Figure 3.16 Removal of top copper circuit layer (left) versus contiguous copper layer (right).

3.3.6.3 Varying of the Thermal Interface Material (TIM)

In this portion of the study, the TIM material was varied to determine the material selection influences. Thermal epoxy and AuSn were modeled as thermal interface

materials on the 254-μm AlN sub-mount. As mentioned previously, the TIM layer was a heat transfer bottleneck in the package and a point of interest for improvement in thermal performance of the device. Figure 3.17 presents the results from the simulation showing a 9.34 K (3.0%) reduction in maximum temperature and a 11.7 K/W reduction in thermal resistance with the use of AuSn. This was attributed to the superior thermal properties of solder versus epoxy. AuSn is nearly 20 times more conductive than epoxy; therefore, the thermal resistance of that interfacial layer is greatly reduced. The p-contacts were operating at nearly 10 K lower that the configuration utilizing epoxy; this is significant.

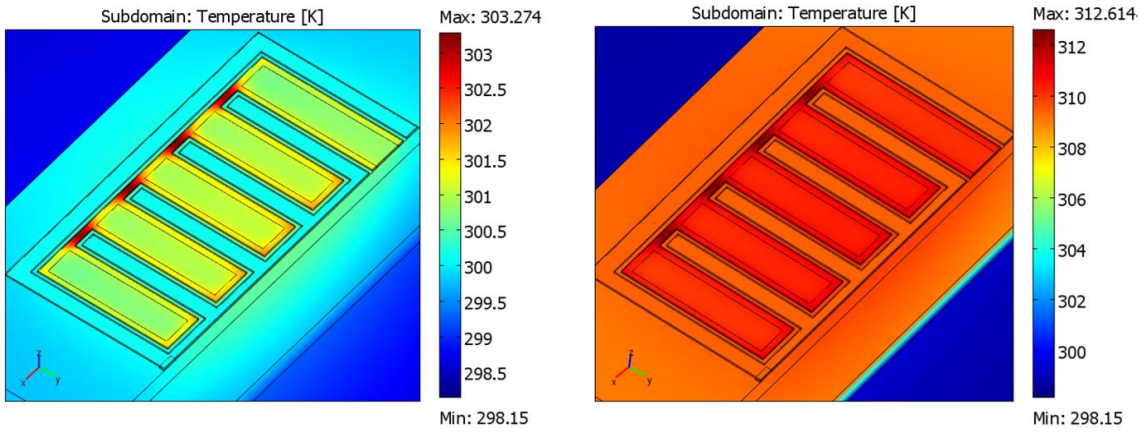


Figure 3.17 Comparison of AuSn (left) and thermal epoxy (right) as thermal interface material.

In addition, there is a significant reduction in AlN-TIM interfacial temperature gradient when AuSn is used. These reduced thermal interfacial loadings, in conjunction with material thermal properties (e.g. CTE match), could yield more robust electrical and mechanical interfacial connections, resulting in an increase in reliability and efficiency. The thermal management advances of the more conductive TIM allows for further optimization of the copper slug heat sink.

3.3.6.4 Investigation of Thermal vias in Sub-mount and TIM Thickness

The purpose of this study is to investigate a possible packaging solution in reducing the high junction temperatures of UV LEDs. Thermal vias are high thermal

conducting pathways from the chip to the heat sink [46, 67]. In most cases, thermal vias are cylinders of copper created by plating a thin insulation layer on the inside surface of a hole drilled through a dielectric material and filling it with a conducting material. For this study, the vias were modeled as rectangular pillars, as presented in Figure 3.18, to simulate an ideal situation where large area vias are used to see the best improvement on the maximum package temperature. They're meant to create an enhanced thermal path for heat through the ceramic AlN submount. Both copper and screen-printed silver were simulated as the via material.

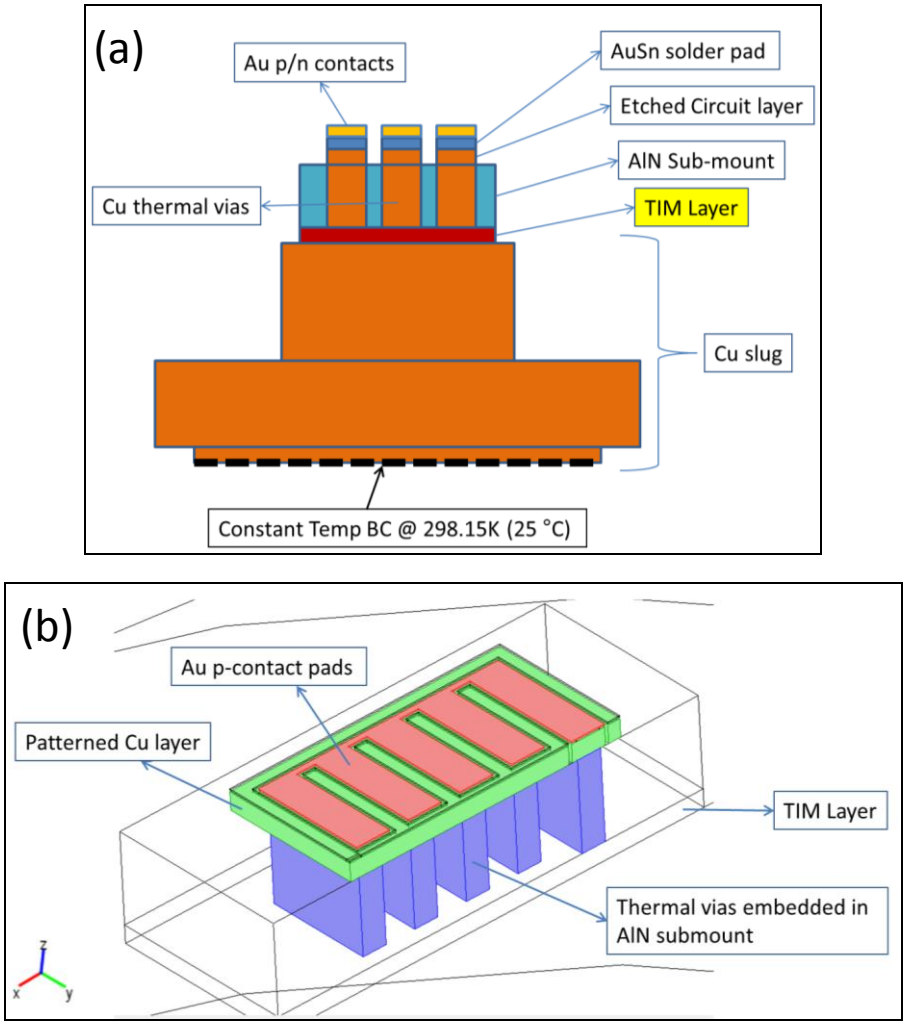


Figure 3.18 (a) Cross-sectional view of submount with thermal vias; all the layers have the same thicknesses as before. (b) COMSOL model view of the structure showing the thermal vias with the etched top copper circuit layer. The vias only contact the "p portion" of the copper circuit layer; this is done to ensure electrical isolation.

The study also looked at the impact of varying the TIM thickness for both epoxy and AuSn solder, at the sub-mount-slug interface. As in the previous studies, a heat flux of 230 W/cm^2 was used with all outside surfaces modeled as insulated and the bottom surface at a constant temperature of 25 °C or 298.15 K. The TIM layer thickness was varied from 13 µm to 50 µm.

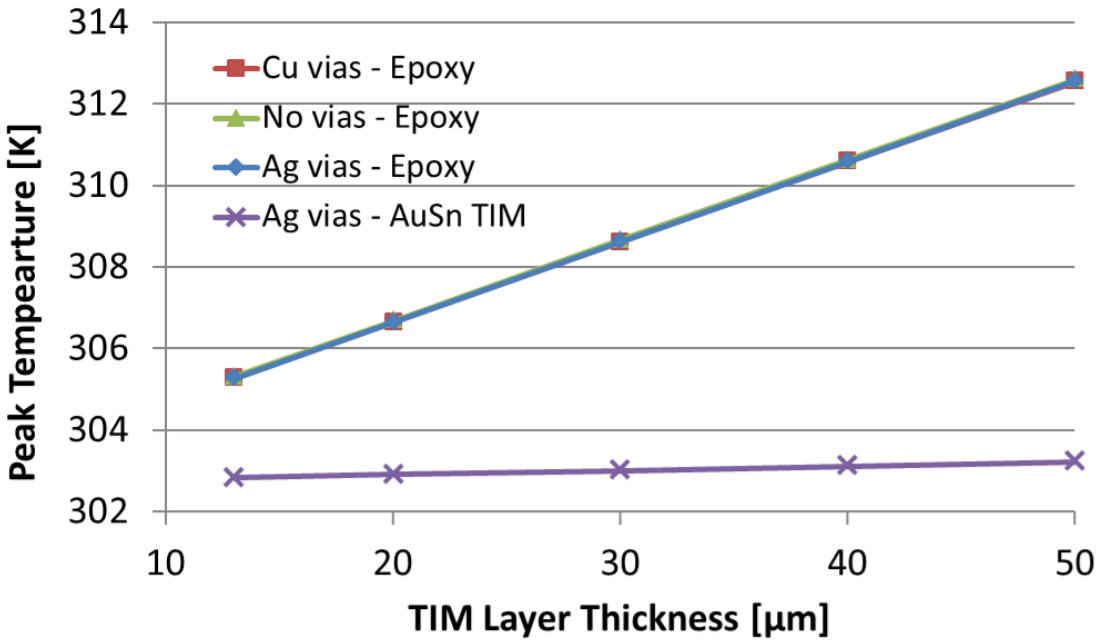


Figure 3.19 Maximum temperatures versus TIM layer thickness comparing both AuSn and epoxy TIMs and also comparing copper & silver vias to a no-via package.

It is clear from Figure 3.19 that the difference between using epoxy and AuSn solder is substantial even though that difference is lessened with a reduction in the TIM thickness; 9.34 K reduction for a 50-micron TIM versus a 2.44 K reduction for a 13-micron TIM. With the use of epoxy, there is a linear relationship between maximum temperature and TIM thickness. There is no spreading in this layer; therefore, the 1D vertical resistance is directly proportional to the layer thickness and inversely proportional to the layer thermal conductivity. Hence, the replacement of 3-W/m-K

epoxy with 57-W/m-K AuSn solder has a staggering impact on the thermal resistance of the TIM layer; a 94% reduction in thermal resistance for a 50-micron thick TIM layer.

Figure 3.20 shows the impact of the thermal vias while varying the thickness of a TIM layer made of AuSn solder. It was deduced from Figures 3.19 & 3.20 that the thermal vias didn't make a significant impact on the maximum temperature of the package; only a 0.042 K reduction from no vias to using silver vias and an extra 0.01 K reduction from using copper instead of silver.

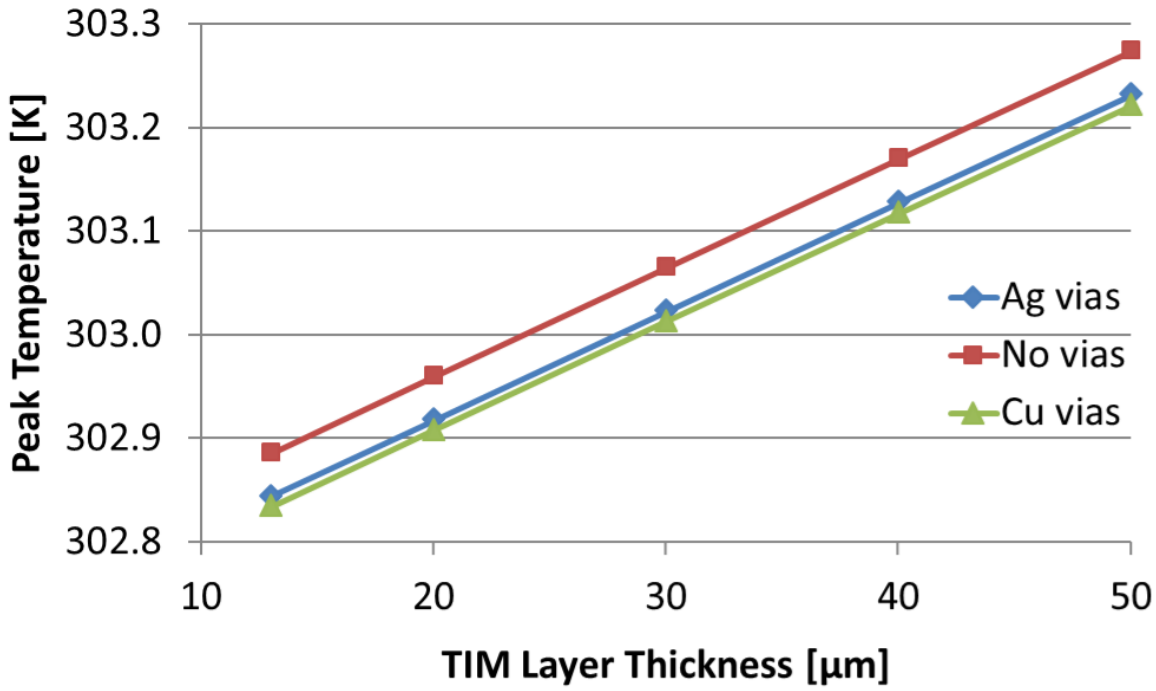


Figure 3.20 Maximum temperatures versus TIM thickness, using only AuSn as the TIM and comparing copper & silver vias to a no-via structure.

3.4 Thermal Stress Modeling

This section briefly describes the thermo-mechanical issues in these devices and the importance of thermal stress modeling in better understanding failure mechanisms and improving the reliability of UV LEDs. High junction temperatures and continuous

thermal cycling introduce thermally induced stresses, which eventually lead to early failures and shortened lifetimes. Operational heating stress was modeled excluding other stresses such as residual stress from solder reflow process and cooling stress.

The model previously neglected (see Section 3.3.3) was used to analyze the thermal stresses caused by the thermal expansions and temperature gradients within the package. The structure analyzed along with the materials used is included in Figure 3.21. The material properties of the different layers are provided in Table 3.3.

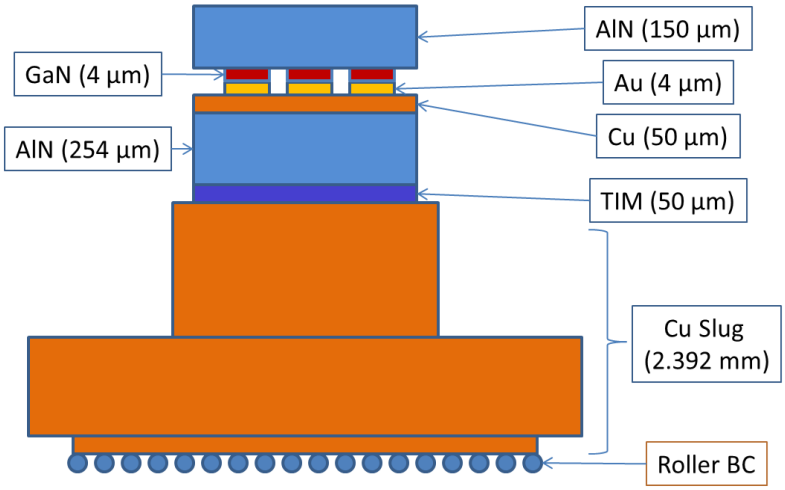


Figure 3.21 Cross-sectional view of structure used for thermal stress modeling; heat transfer boundary conditions have not changed from the previous section. Structurally, the geometry is constrained with rollers on the bottom and is also fixed at several specific points to avoid rigid body motion and rigid body rotation. All other surfaces are free to expand.

Table 3.3 – Materials properties used in the stress simulations [33, 59-61, 68-70]

Material	Thermal Conductivity (W/m-K)	CTE (1/K)	Young's Modulus (GPa)	Poisson's Ratio
GaN	250	5.59 e-6	394	0.352
Au	317	14.2 e-6	70	0.44
AlN	285	4.5 e-6	330	0.24
AuSn	57	16 e-6	68	0.405
Epoxy	3	150 e-6	0.005	0.4
Cu	401	16.5 e-6	120	0.34

COMSOL solves the coupled linear elastic thermal-mechanical constitutive equation for the displacements given boundary conditions and temperatures with in the device [2]. The physical dimensions for the geometry are the same as originally introduced in the previous section. The heat transfer inputs and boundary conditions have not changed as well. A uniform volumetric heat generation value, equivalent to 0.4 W of input power through the half symmetry model, was used as the heat source in the GaN layer. Normal stresses in the three directions as well as displacements are solved for by using the temperature distribution obtained from the heat transfer solution coupled with the structural information provided in Table 3.3. Several key changes to note for this study are as follows. First, gold-gold bonding was used as the interfacial material between the GaN chip and the submount. Second, a GaN layer, representative of the UV LED chip, was included to determine the effects of its thermal expansion. Lastly, both epoxy and AuSn were considered and compared as the thermal interface material between the submount and the copper heat slug.

The next series of figures will compare the structure described in Figure 3.21 with the AuSn solder versus the thermal epoxy as the interfacial material. Figure 3.22 begins by showing the temperature distributions in the two structures.

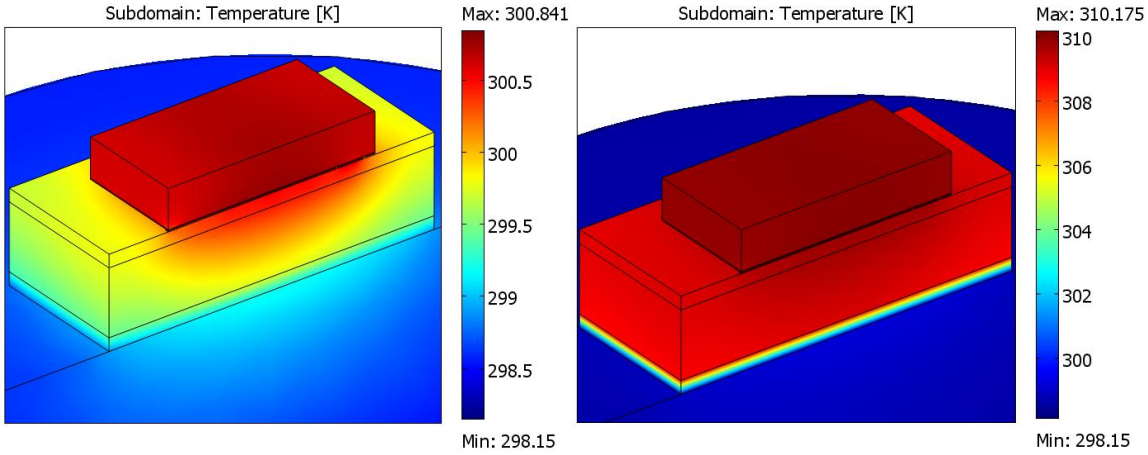


Figure 3.22 Temperature distributions in the UV LED package, assessing AuSn solder (left) and thermal epoxy (right) as interfacial materials.

As expected, the higher conductivity AuSn is able to conduct heat away at a faster pace and therefore offers a lower temperature gradient across the package than the epoxy. The results of the thermal analysis shown in Figure 3.22 were then taken and used as the loading conditions for the structural model along with the mechanical boundary conditions described earlier in this section. The normal stress distributions in the x, y, and z directions are shown in Figures 3.23, 3.24, & 3.25, respectively.

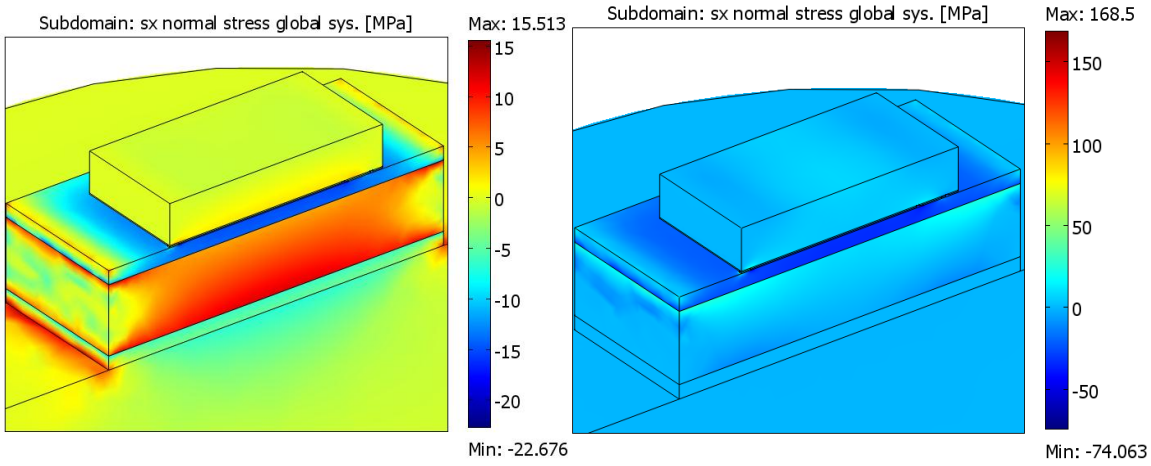


Figure 3.23 Normal stresses in the x-direction for AuSn (left) versus epoxy (right) models.

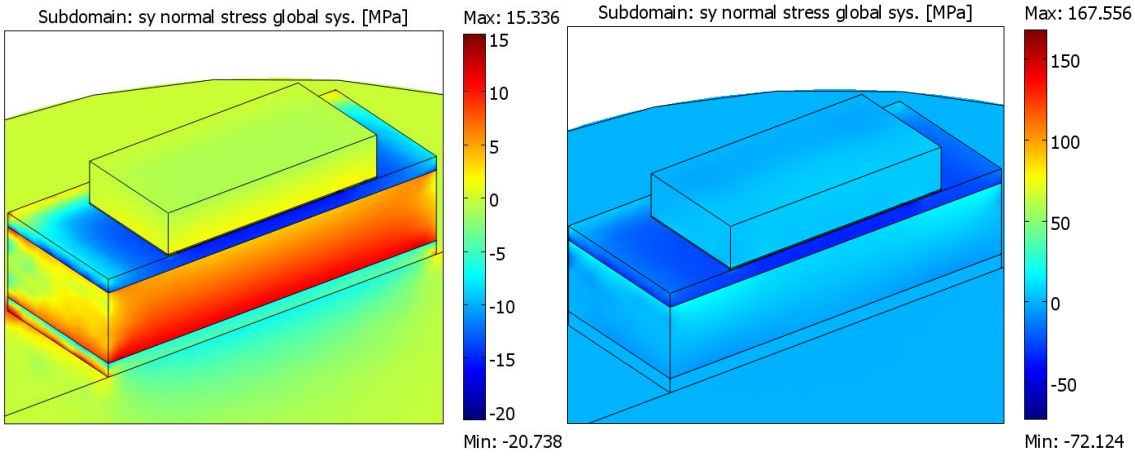


Figure 3.24 Normal stresses in the y-direction for AuSn (left) versus epoxy (right).

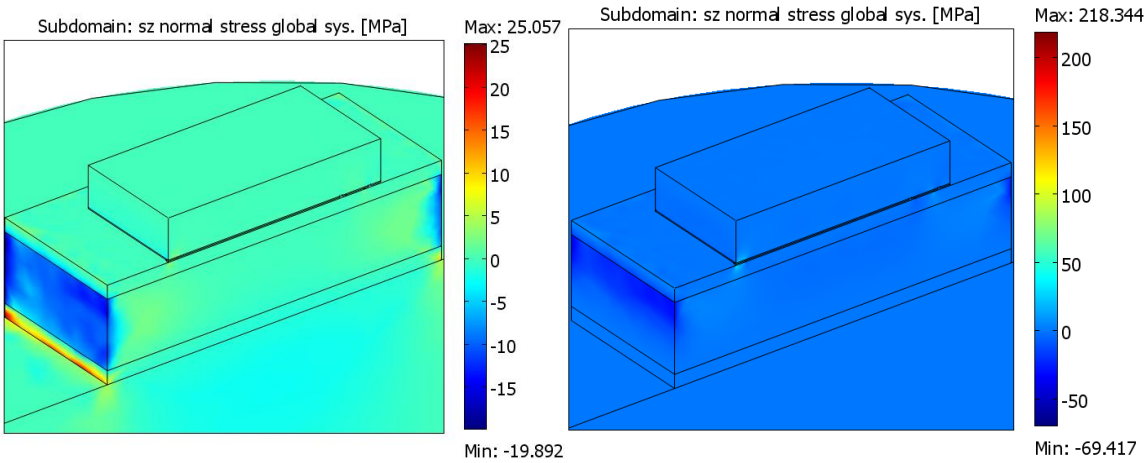


Figure 3.25 Normal stresses in the z-direction for both models; AuSn (left) and epoxy (right).

The first clear contrast in the thermal stresses of the two configurations is the magnitude disparity. The model using the epoxy as the TIM has over 8 times the stress levels in the z direction and over 10 times the stress levels of the AuSn structure in both the x & y directions. This disproportionality can be explained by the inability of the epoxy to dissipate the heat effectively as seen in Figure 3.22. This congestion of heat near the active layer also causes the stress concentrations to be near the junction; this can be seen in Figures 3.23, 3.24, and 3.25. In the structure with AuSn, the peak stresses are clustered near the submount-slug interface whereas the structure with epoxy has its peak stresses massed around the gold-gold bonding sites, very close to the junction.

Figure 3.26 shows the displacements in the package due to thermal stresses and Figure 3.27 shows a visualization of the deformations and deflections in the package. It can be seen that the structure with epoxy has higher deformations and displacements than the AuSn-attached model. Again, the noteworthy aspect is the location of these deformations. In the AuSn configuration, peak displacements occur on the periphery of the heat slug whereas the epoxy model shows peak displacements around the junction, the growth substrate and the AlN submount, which is a negative issue in these devices.

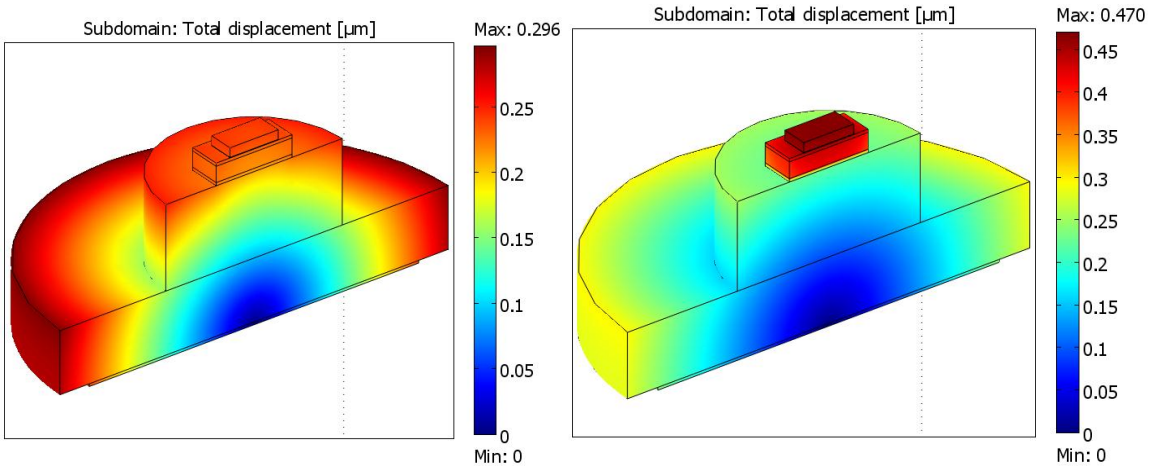


Figure 3.26 The total displacements, in microns, due to thermal expansion for both configurations. AuSn TIM on the left and epoxy TIM on the right.

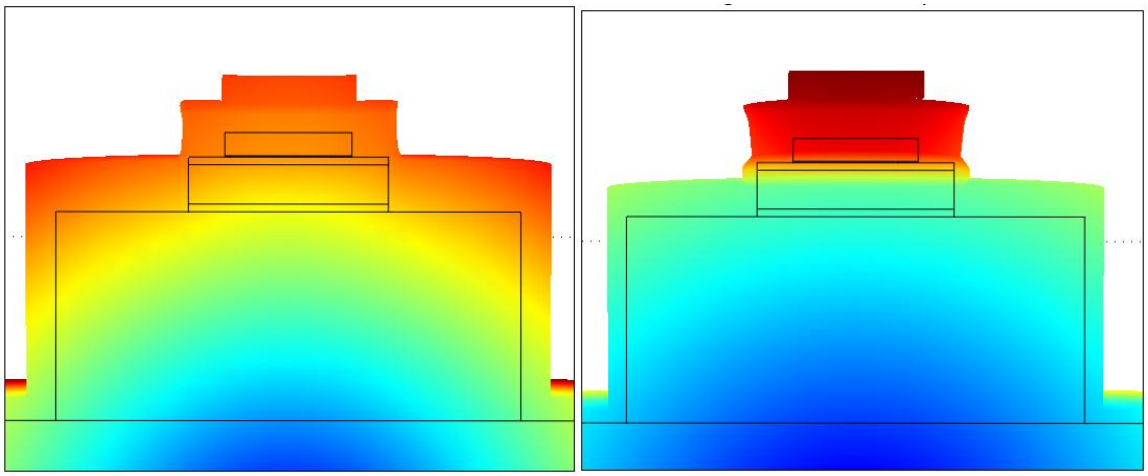


Figure 3.27 Deformation visuals of displacements presented in Figure 3.26.

High junction temperatures and high thermal gradients result in high thermally induced stresses, which lead to deformations, delamination, and shortened device lifetimes. Therefore the reduction of these thermal stresses go hand-in-hand with the decline of high temperatures in these devices. As discussed several times in this chapter, the thermal interface material is the biggest culprit in slowing down heat conduction through the package. The use of alternative materials such as metallic solders at these interfaces significantly improves heat dissipation and greatly reduces thermal induced stresses.

To take it a step further, the reduction of interfacial joints can potentially lead to reduced opportunity for interfacial defects. These defects can lead to resistive electrical contacts, which can result in increased temperatures, reduced thermal and electrical efficiencies, and accelerated degradation of device optimal properties. Poor mechanical and structural integrity can result from similar defects at interfacial regions.

3.5 Transient Modeling

Thermal transient simulation is a useful method to represent the temporal behavior of packaged UV LEDs and high power electronics in general. Understanding of these thermal transient characteristics and responses can provide guidance in designing components and providing adequate heat-sinking. Models can also be used to validate experimentally-obtained transient response curves of devices.

A transient thermal response curve plots junction temperature as a function of time, incorporating the thermal effects of the device structure in the process. Studying a device's transient response at short time scales can provide ways to obtain thermal resistance and capacitance contributions of specific layers of the device and package, along the heat pathway from junction to air, using a method called TRAIT or Thermal Resistance Analysis for Induced Transient [71]. A detailed litany of the TRAIT method and its use in determining discrete and spatially-specific contributions to system thermal resistance in optoelectronic devices can be found here [71-74].

A quick transient simulation was carried out in COMSOL to provide an example of the transient thermal response of a UV LED package. Two different packages were modeled, comparing the two sub-mount-attach materials discussed in the previous sections; gold-tin solder and thermal epoxy. Figure 3.28 presents the model used for this simulation, which is the same model from Section 3.3 with the same heat transfer inputs

of 0.4 W through half of the device and a constant temperature boundary condition on the bottom surface at 298.15 K. It also shows the peak temperature region, on the p-contact, that is analyzed for the thermal transient study. In addition, the transient responses for the two attach materials are plotted and presented in Figure 3.29.

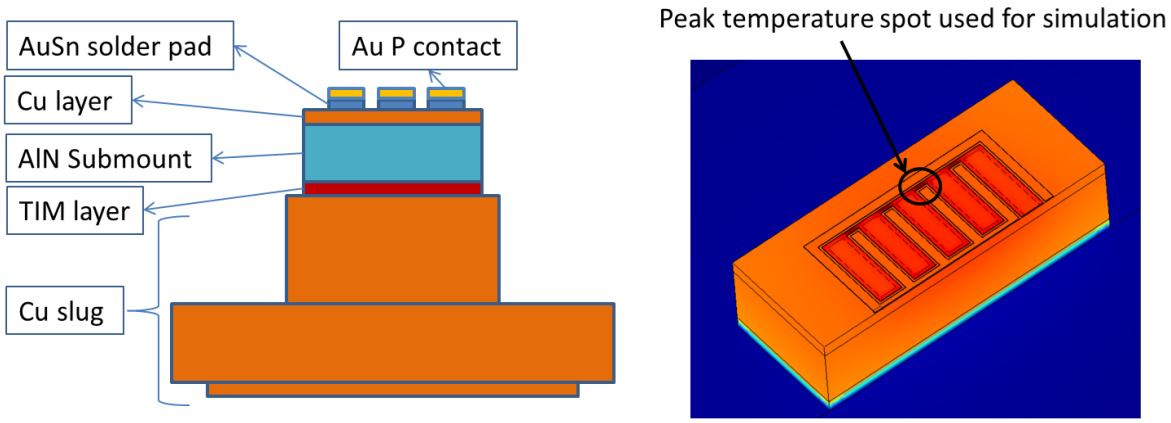


Figure 3.28 Transient model set up; same geometric and boundary conditions as Section 3.3 apply. Note the maximum temperature region used for transient analysis.

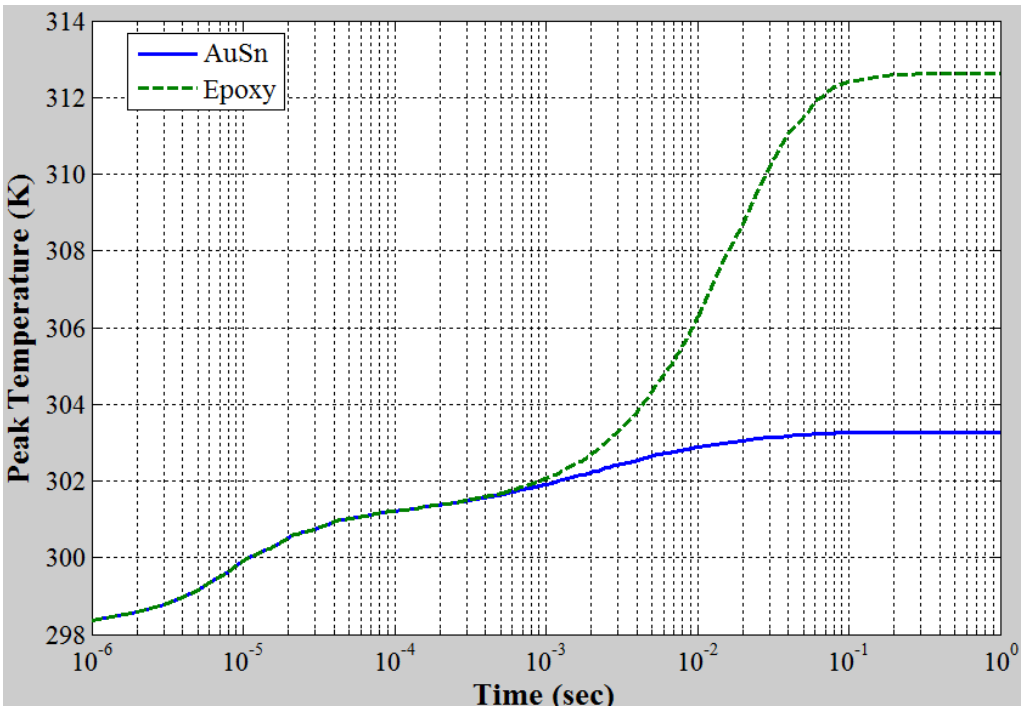


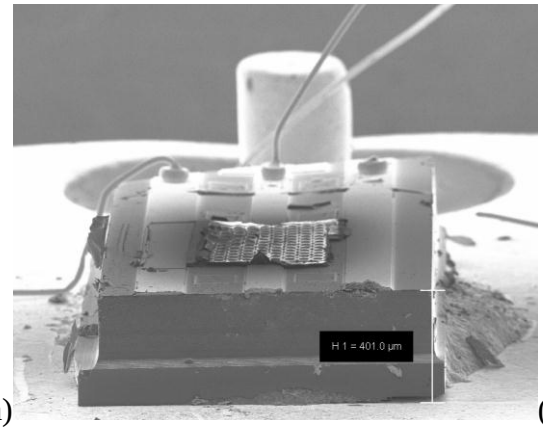
Figure 3.29 Transient response of the UV LED package with two different thermal interface materials; gold-tin solder and thermal epoxy.

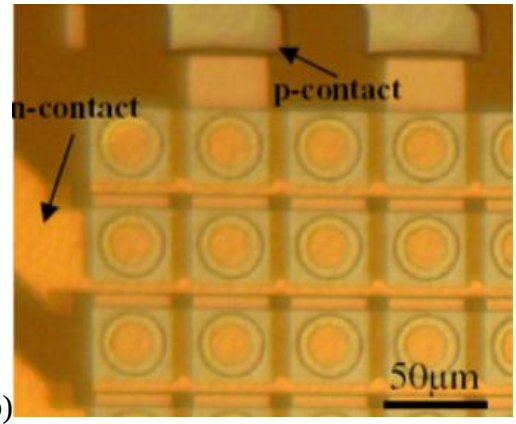
Initial parts of the two curves in Figure 3.29 are identical and separate around 10^{-3} s. This indicates the heat flow through the package prior to the TIM layer, which is the only difference in the two models. The high thermal resistance of the epoxy causes the temperature to rise significantly before it reaches steady state around 0.4 seconds. The plotted transient results reiterate the point that was discussed in the previous sections, which is that the gold-tin solder performs better than the epoxy and keeps the peak temperature of the package much lower than the epoxy.

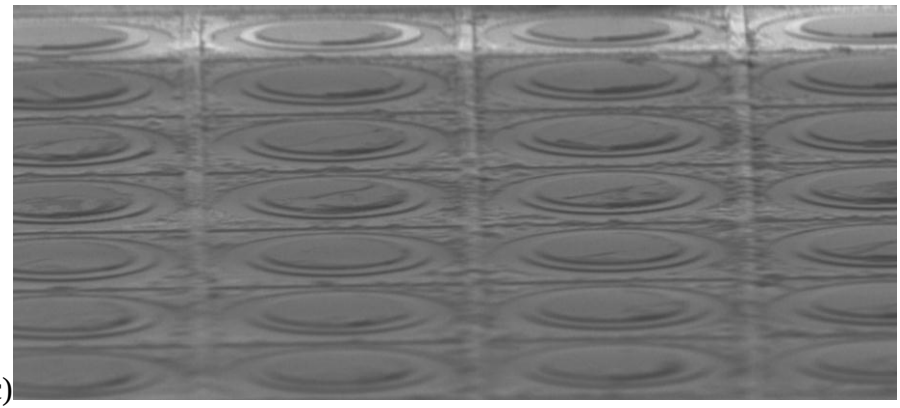
3.6 Interdigitated Micro Pixelated Array Design

The following section presents the thermal analysis of an interdigitated micro pixelated array (IMPA) LED structure. Figure 3.30 shows SEM (Scanning Electron Microscope) and optical images of an IMPA LED configuration, after which the finite element model was constructed; the finite element geometry along with the materials used and thicknesses of different layers is presented in Figure 3.31.

The modeling strategy for this study was as follows: quarter symmetry was utilized in the model to conserve computational memory, the device heating was represented by a 1 W/mm^2 heat flux placed on top of the p-contact pillars, the bottom surface was fixed at a constant 300 K, approximately room temperature, and all other external boundaries were modeled as adiabatic boundaries because the heat loss from the sides is negligible.

(a) 

(b) 

(c) 

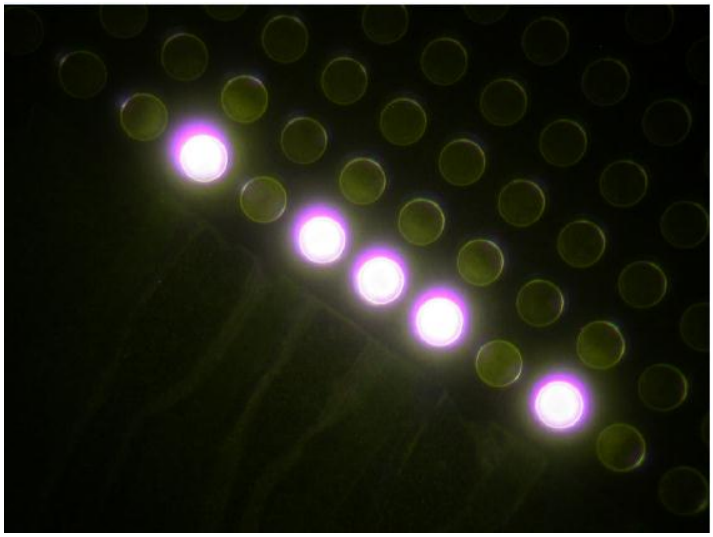
(d) 

Figure 3.30 (a) SEM image of IMPA LED on sub-mount showing wire bonds and micro pixels, (b) Top view of an optical image of the micro pixel array, (c) isometric view of micro pixels showing the vertical depth of the pixels and the borders that separate the p-side from the n-side, and (d) microscope image of a micro-pixel array with several pixels turned on and emitting in the UV range.

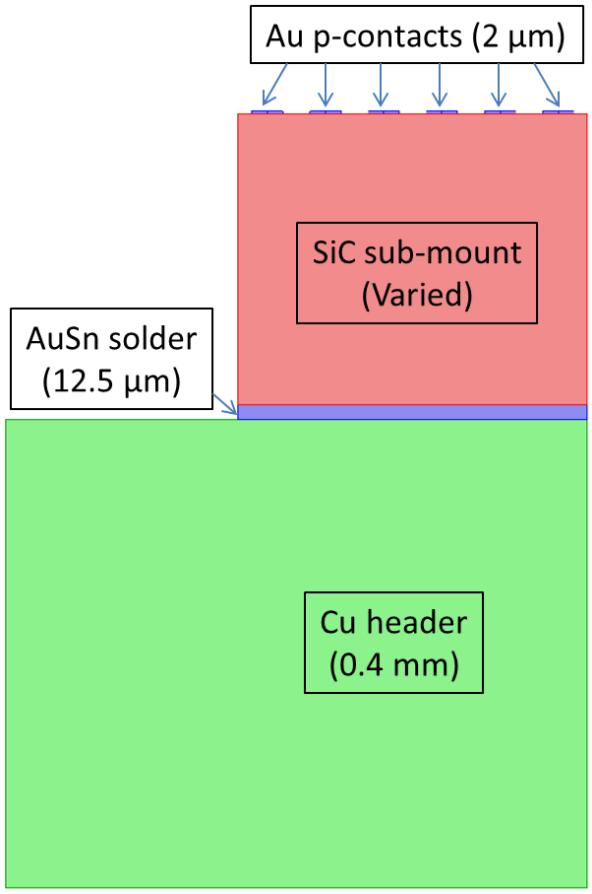


Figure 3.31 Cross-sectional view of finite element model constructed to investigate the thermal performance of the IMPA LED configuration.

The purpose of this study was to investigate the impact of pixel density and sub-mount thickness on the overall package thermal resistance. The thicknesses investigated were 250 µm, 150 µm, 100 µm, 75 µm, and 50 µm. Two different pixel densities were considered; one model was made up of 60 pixels and the other 24 pixels. These pixel quantities were for the quarter model; therefore the two models represented a 240-pixel device (20X12 array) and a 96-pixel device (12X8 array), respectively. As mentioned above, both models experienced exact same boundary conditions and material properties. The thermal conductivities of the materials shown in Figure 3.31 have all been discussed in previous sections except for Silicon Carbide (SiC), which has a thermal conductivity of 370 W/m-K. The next two figures display the results from the finite element analysis.

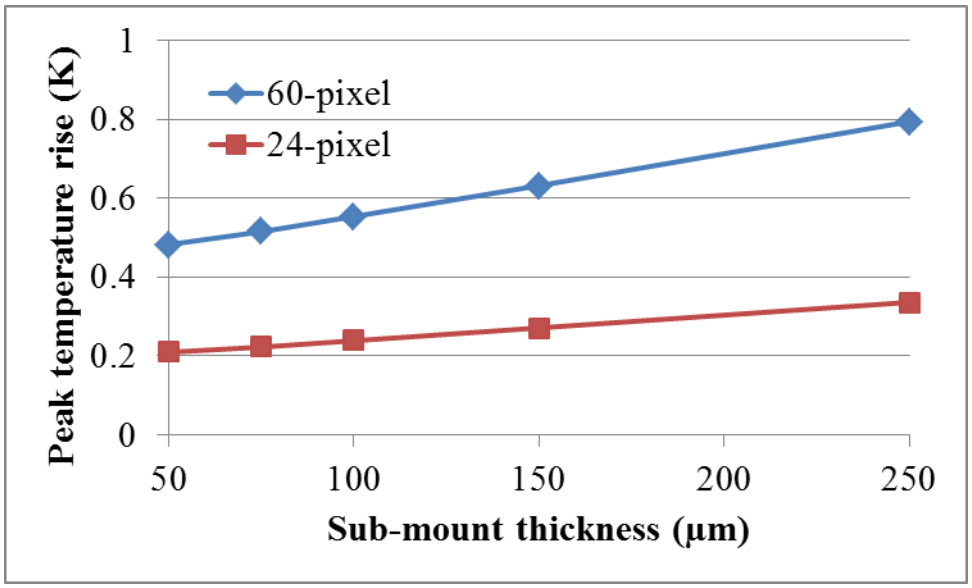


Figure 3.32 A display of peak temperature rise of the IMPA LED as a function of the SiC sub-mount thickness.

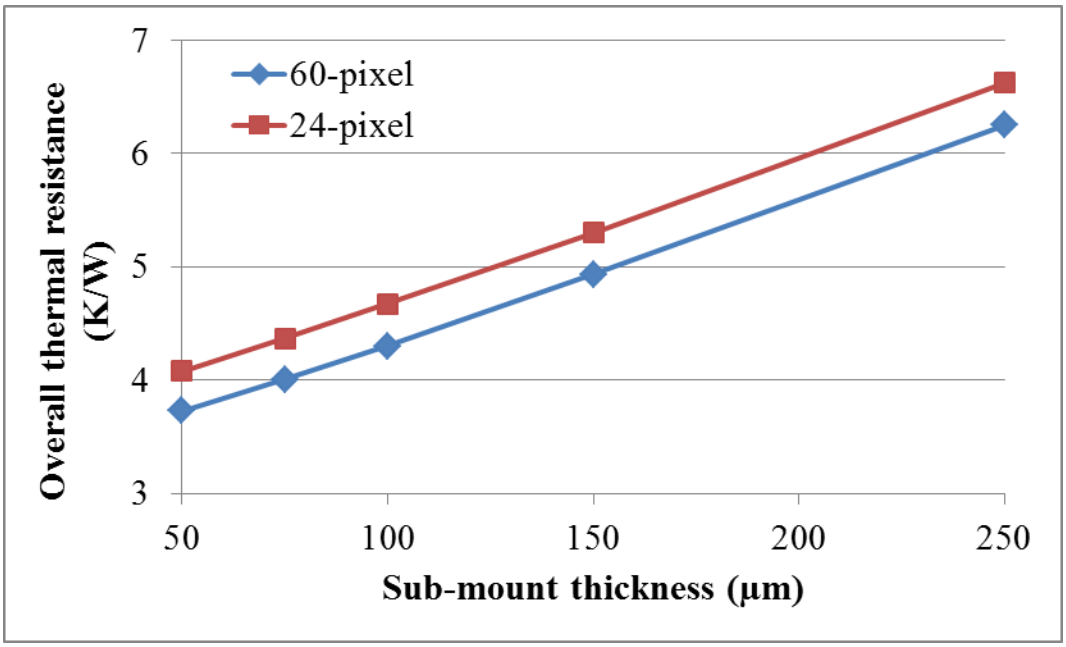


Figure 3.33 A plot of overall package thermal resistance variation as a function of SiC sub-mount thickness.

Figure 3.32 shows the peak temperature rise for the two configurations when altering the thickness of the silicon carbide sub-mount. It is clear from the plot that the device with the smaller pixel density experiences lower peak temperatures. Both models

observed temperature rises of less than 1 K for the inputted power. The submount thickness had a bigger impact on the 240-pixel device over the 96-pixel device because higher pixel density equates to a higher total heat load even though each pixel faced equivalent heat fluxes in both models.

Figure 3.33 shows the total thermal resistance of the system, as it fluctuates with the variation of the sub-mount thickness. Although smaller pixel density was the superior configuration when comparing peak temperatures, as seen in Figure 3.32, Figure 3.33 suggests that the model with the higher pixel density has the smaller overall thermal resistance. This is explained by the fact that the heat load was more than doubled with more pixels but the temperature rise was not directly proportional. For example, the 250-micron-thick sub-mount experienced the highest temperature rise with more pixels; temperature rise increased by a factor of 2.37 while the heat load increased by a factor of 2.51, from 52.76 mW to 132.24 mW. Since the thermal resistance was calculated using the ratio of temperature rise to heat input, the higher density configuration was able to achieve a lower thermal resistance. Therefore, the 240-pixel device was able to dissipate more heat-per-degree-rise than the 96-pixel device.

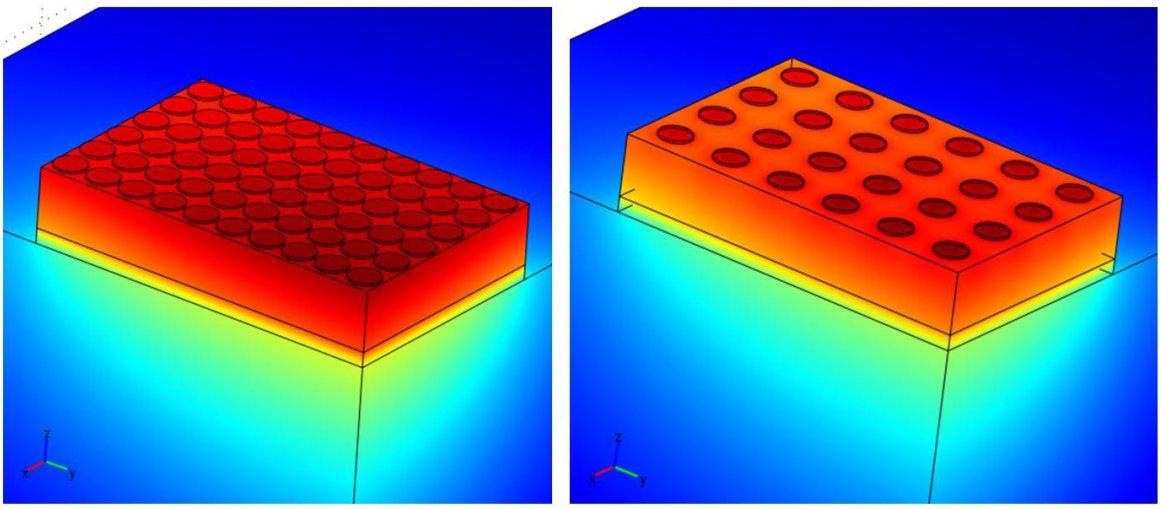


Figure 3.34 Finite element results showing temperature distributions in the 60-pixel (left) and the 24-pixel (right) quarter models. Both sub-mounts have a thickness of 50 μm.

Figure 3.34 shows the temperature distribution contour plots for both models. For effective thermal management, the heat spreading effect of the sub-mount must not be hindered. The micro-pixel pitch must not be so small that the pixels are impeding on each other's effective heat spreading areas. The 24-pixel model had a uniform pitch of 50 μm between its pixels while the 60-pixel model had a pitch of 30 μm in the x direction and 33.33 μm in the y direction. Hence, the higher peak temperatures of the 60-pixel model can be attributed to smaller pitch which resulted in heat congestion around the p-contacts, as seen in Figure 3.34. Since the input power in this model was low, less than 1 W, the impact on junction-temperature rise and overall thermal resistance was low; although pitch should increase with higher operating powers [1]. Micro pixel pitch is also important optically because intensity overlap becomes an issue for small-pitch arrays. Kelm et al. performed 1D calculations of intensity versus micro-LED pitch between two adjacent pixels of a 32X32 micro-UV-LED array and found that the intensity crosstalk is below 10% for a pitch greater than 80 μm [75].

Inspection of results presented in Figure 3.33 indicates appreciable thermal diffusion through thinner SiC sub-mounts. The thickness of the sub-mount has a significant effect on the reduction of the overall package thermal resistance while the pixel density has the controlling impact on the maximum temperature of the device. Therefore, the use of thinner sub-mounts with small pixel densities will offer the optimum thermal performance. Note that less pixel density does not equate to less pixels. A device may have as many pixels as desired but the important factor is the pitch between pixels. Adequate spacing between pixels is necessary in order to allow for heat spreading and operate the device at lower junction temperatures.

3.7 Summary

Thermal resistance analysis of a UV LED lead frame package was carried out using finite element modeling in COMOSL. Major components were modeled and their effects on the junction temperature and the overall package thermal resistance were analyzed. Various studies were performed not necessarily to find optimum parameters but to provide tradeoff assessments.

P and *N* metal contacts were shown to have a bigger impact on the junction temperature than the solder pads used to connect the chip to the sub-mount. Using the same solder pad material, gold contacts resulted in a lower junction temperature than gold-tin contacts because of gold's superior thermal conductivity. In addition, using the same metal contact material, the use of gold-tin solder bonding pads versus gold-gold bonding pads proved to have a small effect on the maximum device temperature. This means that it is important for the metals contacts to have a high thermal conductivity and not as important for the solder pads to have high thermal conductivity.

The sub-mount was shown to have a significant impact on the overall package thermal resistance. Three parameters were studied in depth; lateral area, thickness, and thermal conductivity were varied and package resistance was analyzed. It was determined that the lateral area ratio between the sub-mount and the UV LED is important as it facilitates in heat spreading and reduces the incoming heat-flux. The data showed an exponential decrease in resistance with increasing AR, meaning that the largest reduction in overall thermal resistance was seen in a change from AR=1 to AR=2. For a material with k > 100 W/mK, the AR was found to be the dominating parameter in reducing overall thermal resistance. With an optimum sub-mount-to-die area ratio, there's flexibility on the thickness and thermal conductivity of the sub-mount, in regards to thermal resistance.

A large bottleneck of heat flow was found at the thermal interface material layer, between the submount and slug. The thermal epoxy had the largest thermal resistance because of its poor thermal conductivity, only 3 W/m-K. Eutectic gold-tin solder was shown to have significant improvement on the thermal performance in place of the thermal epoxy. The improvement in thermal resistance and peak temperatures allows the device to be operated at higher powers with manageable thermal drawbacks.

Several minor studies of less-critical components were conducted. The growth substrate was excluded from all of the models because it was shown to have a small impact on thermal performance due to fact that the heat pathway was in the opposite direction. The etched copper circuit layer was shown to have a low impact on thermal performance of the modeled UV LED device. Thermal vias embedded in the AlN sub-mount did not show significant enhancement in thermal performance. Thermal stress modeling showed that the highest stress regions, caused by CTE mismatches, were found to be in the interfacial and attach layers, reinforcing the need to reduce thermal gradients in these layers. The usefulness of thermal transient curves was briefly discussed.

Interdigitated Micro Pixelated Array (IMPA) UV LED modeling showed the effects of pixel density on thermal performance. It was shown that the higher-pixel-density model results in a smaller thermal resistance than the lower-density model, at low input powers, less than 1W. Conversely, it was the high-pixel-density model that resulted in higher peak temperatures and this was considered to be due to increased heat load from the additional pixels.

CHAPTER 4

EXPERIMENTAL EVALUATION OF ALTERNATIVE COOLING TECHNIQUES

4.1 Introduction

This chapter explores two alternative materials as potential cooling technologies for UV LEDs as well as other electronic devices. As stated in the previous chapters, the flip-chipped DUV LED chip sits on a heat-spreading sub-mount, is then attached to a variety of high-conductivity substrates or metal slugs, and then attached to a heat sink to dissipate thermal energy efficiently. Therefore, the interfaces that occur in the heat-flow pathway in these architectures require thermal interface materials (TIMs) to be used, which lead to the potential of increased thermal resistance. One opportunity to address these interfaces is through the use of phase change materials (PCM) that operate at a fixed temperature during the phase transition process. For devices that undergo intermittent operations, where the device goes through short on/off cycles, a PCM such as paraffin wax may be able to limit the peak temperature of the LED. Another alternative to the typical thermal grease or epoxy interface material is to use a high-thermal-conductivity compound such as Galinstan. The eutectic alloy, comprised of gallium, indium, and tin, is a non-toxic, high wetting, highly conductive compound that is liquid at room temperature with a boiling point that exceeds 1300°C [76]. Both paraffin wax and GaInSn are compared with thermal grease in their ability to dissipate heat effectively. To analyze these options for improving thermal management, a commercial yellow light LED was attached to an insulated metal substrate (IMS) using one of the aforementioned interface materials; paraffin wax, GaInSn, or zinc-oxide-filled silicone grease. The

performance of the LED was assessed using the forward voltage method. The temperature rises of the three different configurations were compared to evaluate the functionality of these thermal interface materials in LED packaging.

Furthermore, the concept of immersion cooling in LEDs is briefly discussed in this chapter. Liquid cooling commonly maintains higher heat transfer coefficients and thus higher heat transfer rates than air cooling. In this particular investigation, a commercial white light LED in operation was immersed in a dielectric heat transfer liquid and the thermal performance was assessed. The immersed LED performance was then compared to the operation of the same package attached to an air-cooled heat sink.

4.2 LED Performance with Alternative Thermal Interface Materials

A commercial yellow LED was chosen for this study. The packaged LED consisted of a lead frame package with a metal slug. The dimensions of a typical LED package and the material properties are listed in Table 4.1. A commercially available, high-power LED package like the Luxeon III LED has a thermal resistance of 13 K/W [77, 78]. Typically the packaged LED is attached to a board (e.g. printed circuit board) using a thermally conductive adhesive [33, 78]. It is then placed on a heat sink for additional thermal management because heat dissipation from the package surfaces is not always sufficient [33]. The slug-to-board attachment was varied in this study to demonstrate the effectiveness of alternative materials, see Figure 4.1.

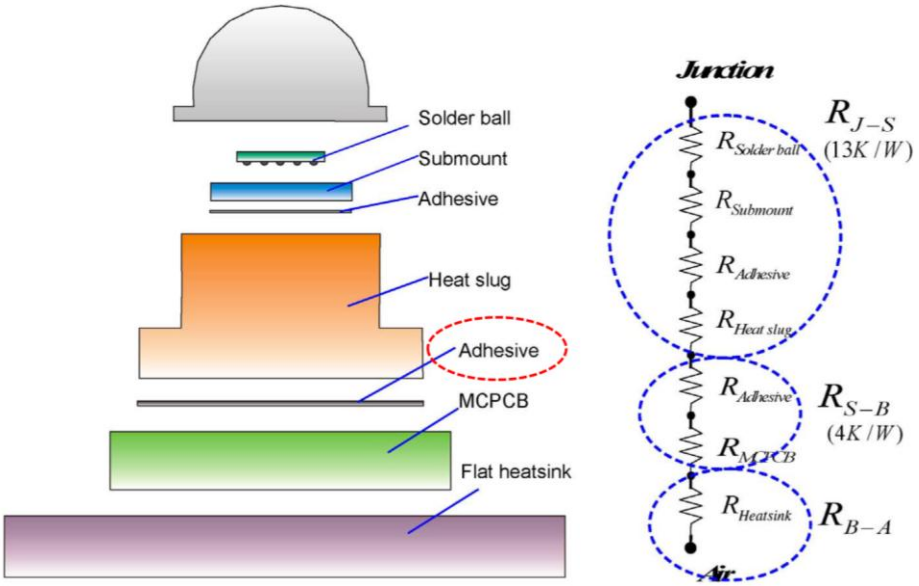


Figure 4.1 Thermal network model for a typical high-power LED package [78, 79]. The studied interface is between the heat slug and MCPCB; marked by the red oval.

Table 4.1 Material properties and thermal resistance of a typical high-power LED package [78, 79].

	Thermal Conductivity (W/m·k)	Thickness (mm)	Thermal Resistance (K/W)
Solder	50	0.1	2
Submount (Si)	150	0.5	1.48
Adhesive (Submount-Heat Slug)	1	0.035	8.5
Heatslug (Cu)	360	2.87	0.97
Adhesive (Heat Slug-MCPCB)	1	0.07	–
MCPCB Dielectric Layer Metal Layer (Al)	1.8 237	0.1 1.5	–
Tape	0.067	0.130	–
Heat Sink (Al)	237	1.6	–
Total Thermal Resistance			12.95

4.2.1 Alternative Materials

As discussed in this thesis, the push for higher power LEDs means higher power densities, which leads to elevated junction temperatures necessitating the application of more aggressive thermal management techniques [78]. Desai et al. have demonstrated

novel cooling techniques based on the use of PCMs near the junction of GaN high electron mobility transistor (HEMTs) grown on silicon wafers. The PCM-enabled devices showed a 10% improvement in device performance due to the thermal management enhancement [80]. Kandasamy et al. demonstrated thermal enhancements with the use of PCM-based heat-sinks in transient electronic devices. Finned-heat-sink cavities filled with paraffin wax were shown to increase the cooling performance of the package, with high input powers (> 2 W) [81]. This study focused on the use of paraffin wax as a thermal interface material in high-power LED packages; refer to Figure 4.1.

Paraffin wax is a hydrocarbon with the general formula C_nH_{2n+2}, and has a typical melting point between about 46°C and 68°C (115 and 154°F), based on the length of its carbon chain [82]. Pure paraffin is an excellent electrical insulator, with an electrical resistivity of between 10^{13} and 10^{17} Ω·m [83]; better than many materials except some plastics like Teflon. Paraffin has favorable features like congruent melting meaning repeated melting without degradation of latent heat of fusion and self-nucleation meaning it crystallizes with little super-cooling and non-corrosiveness [84]. However, for the purpose of this study, paraffin wax was selected due to its suitable phase-transition temperature and high latent heat of transition. The chemical structure of the paraffin used in these experiments was $C_{26}H_{54}$ with a melting point of 56.3°C (133.34°F) and latent heat of fusion of 256 kJ/kg [84].

In the second approach, a high thermal conductivity metal was used as the interface material to reduce interfacial thermal resistance. Galinstan was chosen for this purpose due to its low melting temperature and its ability to wet the interface between the packaged LED and the IMS heat spreader shown in Figure 4.2. Galinstan (GaInSn) is a eutectic alloy, mainly consisting of gallium, indium, and stannum (tin), typically found as 68.5% Ga, 21.5% In, and 10% Sn by weight. GaInSn is liquid at room temperature with a freezing point of -19°C (-2°F) [85]. This liquid metal is commonly used as a replacement for liquid mercury because of its low toxicity and reactivity. Galinstan has high

wettability and adhesion to many materials, including glass, which is a major limitation when compared to mercury but is excellent for applications such as making mirrors; it has favorable reflective properties. It's commercially used as a mercury replacement in thermometers but the inner tube must first be coated with gallium oxide to prevent the alloy from wetting the glass surface. Another major obstacle is its chemical compatibility with other materials; it corrodes many other metals, especially aluminum, by dissolving them. Although it has a high thermal conductivity of 16.5 W/m-K, it is also electrically conductive and corrosive to metals, therefore careful considerations must be taken when using Galinstan as interfacial material in electronics packaging.

The thermal grease used for this experiment is zinc-oxide-filled silicone grease obtained from Rawn·America™ with high dielectric strength, 250-350 volts/mil. It is a viscous fluid substance that is white in color. The enhanced thermal properties of the liquid silicone grease come from the zinc oxide ceramic powder that is suspended in the grease. The grease is stable over a large temperature range, between -40°F and 500°F. It is non-flammable, non-corrosive, and moreover it does not separate, soften, run, dry out or harden. These aforementioned qualities make it a suitable candidate as an interfacial material in electronics, to reduce contact resistance and aid with thermal dissipation via a heat sink. Note that thermal grease is intended to fill air gaps at interfaces and not to create a layer between device and heat sink, as that would increase thermal resistance because of the low thermal conductivities of thermal grease, usually ranging from 0.8 to 4.5 W/m-K [1].

4.2.2 Sample Preparation

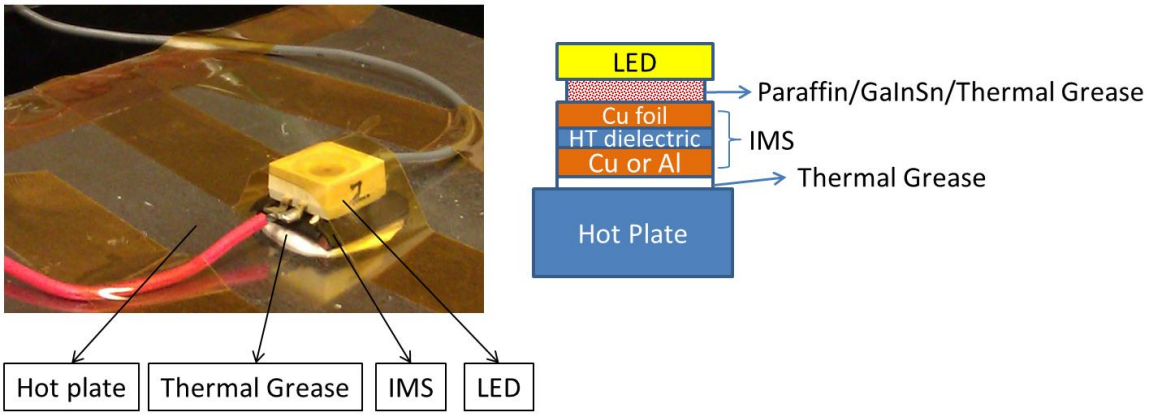


Figure 4.2 Experimental setup of a yellow LED attached to a substrate with various attach-materials at the LED-IMS interface. Paraffin wax, GaInSn, and thermal grease were varied during the experiments.

As seen in the experimental setup displayed in Figure 4.2, the yellow LED was placed on a T-Clad® insulated metal substrate (IMS), obtained from The Bergquist Company, which was then placed on a HCP324 hot plate regulated by the INSTEC STC200 temperature-controller. The IMS was a three-layer board consisting of a 0.06" (1.52 mm) thick copper base and a 20 oz. (70 µm) thick top copper circuit foil with a 3 mil (0.003" or 76 µm) thick high-temperature (HT) dielectric layer sandwiched in between the copper layers. The lateral sizes of the IMS and the LED (heat slug area) were approximately 4.76 mm^2 (0.1875 in^2) and 1.88 mm^2 (0.074 in^2) respectively; substrate-to-LED area ratio was around 2.5, yielding good heat spreading.

The three different materials of interest (Paraffin, Galinstan, & Grease) were placed at the LED-IMS interface. A square reservoir using polyisobutylene edge sealant (HelioSeal™ PVS 101) was constructed atop the IMS to contain the paraffin wax and Galinstan and ensure no spills would occur due to any phase change. This also ensured equal volumes for all three materials; the lateral dimensions were the same as the heat slug (1.88 mm^2) while the thicknesses were controlled by the sealant thickness, which was approximately 400 µm. A thin layer of thermal grease was used in all experiments, at the IMS-Hot-plate interface, to affix the setup to the hot-plate.

For the transient study, the LED was powered to approximately 750 mW at an input current of 260 mA and forward voltage readings were taken. All experiments were conducted with a base (hot plate) temperature of 48°C and the LED was only powered after allowing for entire setup to reach thermal equilibrium. High sampling rates at short time scales were employed to capture the fast transients of the LED. Signal noise was reduced by shielding wires and grounding the Keithley chassis. The transient forward-voltage response was then converted to junction temperature transient data via Eq. 4-1 and the resulting plots are presented in Figure 4.3. Note temperature rise was calculated by taking the temperature transient data and subtracting the known stage temperature of 48°C.

4.2.3 Temperature Measurements

The transient junction temperature response of the yellow LED was extracted from forward voltage data experimentally measured under continuous DC bias. The diode forward voltage (V_f) can be used to assess the junction temperature of an LED [86]. The calibration was conducted in which the LED was biased in pulse mode with a known current, and the V_f was measured over a range of known junction temperatures. The pulse duration was set to 900 µs at a period of 1 s. The duty cycle was kept small (< 0.1%) to ensure that the junction temperature was equal to the stage-controlled temperature. All electrical measurements were taken using 4-wire sensing eliminating resistance contributions from the wiring. The high-power Keithley 2651A source measure unit (SMU) was used as the power source. A linear relationship between forward voltage and temperature was obtained at specific input current levels; see Equation 4-1.

$$V_f = A \cdot T_j + B \tag{4-1}$$

where T_j is the junction temperature, A is the slope of the calibration curve, and B is the y-intercept.

4.2.4 Discussion of Results

As presented in Figure 4.3, paraffin wax exhibited the poorest thermal performance in a five minute transient study. The paraffin configuration showed a junction temperature rise of 25°C above 48°C whereas the thermal grease and Galinstan setups yielded temperature rises around 10°C. Galinstan showed a slight advantage, due to its higher thermal conductivity, by maintaining the LED ~2°C cooler. Initially, the paraffin was able to perform as well as the others during its melting phase; however once the phase change was complete, the liquid wax became a high-thermal-resistance layer and exacerbated the device heating.

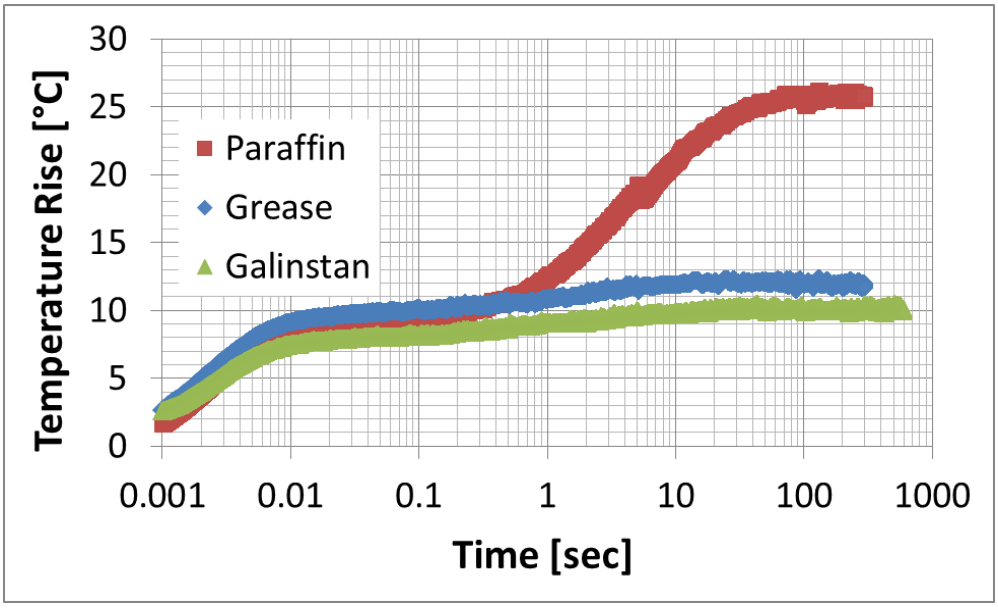


Figure 4.3 Thermal transient response of a yellow LED using three different attach materials. The plot shows the junction temperature rise in degree Celsius with respect to time in seconds.

The junction-to-IMS-board thermal resistance ($R_{J\text{-}B}$) was calculated using the steady state temperature rise (ΔT) and dividing it by the known input power (Q_{in}).

Furthermore, the thermal resistance of each TIM layer-of-interest (R_{TIM}) was extracted by subtracting the IMS board resistance (R_B) and the junction-to-slug resistance ($R_{J\text{-}S}$); refer to Equations 4-2 & 4-3. The reported junction-to-slug thermal resistance of a typical high-power LED of 13 °C/W was used (see Figure 4.1). The thermal resistance across the IMS was found to be 0.0796 °C/W through finite element analysis. Therefore, the thermal resistances of the paraffin wax, Galinstan, and thermal grease were 21.59 °C/W, 0.25 °C/W, and 2.92 °C/W respectively.

$$R_{TIM} = R_{J-B} - (R_{J-S} + R_B) \tag{4-2}$$

$$R_{J-B} = \frac{\Delta T}{Q_{in}} \tag{4-3}$$

The heat flux near the chip and the heat flux at the base of the heat slug (before the TIM) were calculated by dividing the input power by lateral area of heat transfer. The chip was assumed to have the typical area of 1 mm^2 while the heat-slug lateral area was stated previously as 1.88 mm^2. Hence, the high heat flux was reduced by 47% at the slug-IMS interface due to the heat spreading effects of the heat slug and prior package layers. Perhaps this was one reason that a bigger impact was not seen by Galinstan over the thermal grease. In addition, both materials were applied in thin layers, reducing their thermal resistances; therefore the advantage of Galinstan over thermal grease would be more prevalent in thicker layers or under operation with larger heat loads.

4.3 Immersion Cooling

The ever-increasing power-dissipation demands by electronic devices are likely to transition future cooling technologies from being air-based to being liquid-based. With chip heat fluxes approaching or exceeding 10 W/cm^2, attention must be turned to liquid cooling techniques [87]. Forced convection, micro-channels, spray and impinging jets, capillary pumped loops, and immersion cooling [88-93] are being considered.

It has been over two decades now that researchers have been exploring immersion cooling in dielectric fluids [94, 95]. The high dielectric strength and low dielectric constant of these liquids, as well as their chemical inertness, make it possible to immerse most electronic components directly in these fluoro-chemical liquids [87]. Immersion cooling aims to take advantage of the one order-of-magnitude higher heat-flux removal than air-cooling present through pool (nucleate) boiling [87]. Nucleate boiling is a complex convective heat transfer process depending upon liquid-to-vapor phase change by the formation of vapor bubbles at a heated surface. Boiling typically commences when the surface temperature exceeds the liquid saturation (boiling) temperature by 3 – 10°C, and vapor bubbles are then found to grow and issue from minute cavities in the surface [96].

Jou performed thermal and optical characterizations of high-power (3W) LEDs fully submerged in air, silicone oil, and FC-40 [97]. The dielectric fluid (FC-40) showed significant thermal enhancement over air and silicone oil; 36% improvement over air and 3% improvement over silicone oil. Arik et al. studied the thermal performance enhancements of bare LED chips via immersion cooling in optical fluids [87]. A three-chip LED light engine enclosed in a fluid-filled dome was shown to increase heat transfer by 60% when compared to an air-filled dome. This study explored the use of immersion cooling of commercial LEDs in a dielectric fluid, which was compared to passive cooling through free convection in air. A brief experimental study was conducted to obtain the

thermal performance of a white light LED in two setups; one fully immersed in dielectric fluid and the other mounted on a large air-cooled heat sink.

4.3.1 Experimental Methodology and Setup

In this study, the junction temperature rise above ambient was studied for a white light LED; refer to Figure 4.4 for an image of the tested device. The transient forward voltage response to known input currents was measured and combined with calibration data for the LED to extract the junction temperature transient response; see Section 4.2 for a detailed explanation. Junction temperature rise was calculated by subtracting the ambient room temperature from the junction temperature calculated.

The white light LED used in the experiment was a Cree XLamp XR-E LED mounted on a Starboard insulated metal substrate. The LED features a maximum drive current up to 1000 mA and maximum junction temperature of 150°C. The XLamp XR-E also offers a junction to solder point thermal resistance of 8 °C/W [98]. The star substrate is an insulated metal substrate (IMS) consisting of an Al base and a top copper layer with a dielectric layer sandwiched in between the metals.

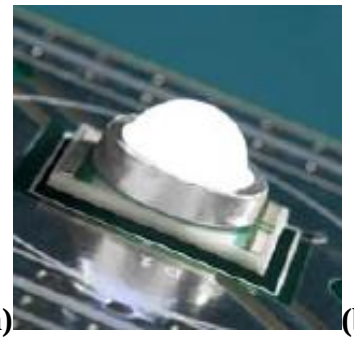
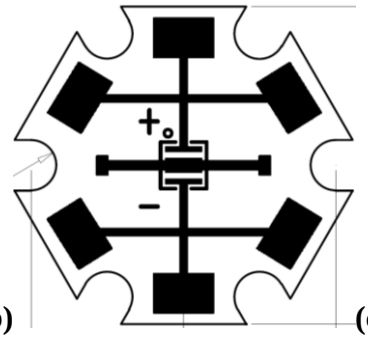
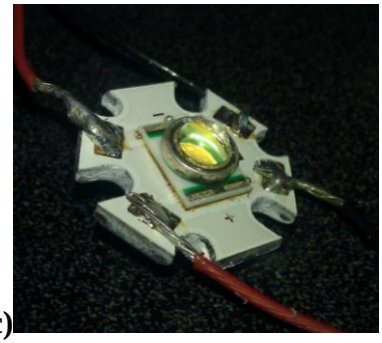
(a)  **(b)**  **(c)** 

Figure 4.4 (a) Cree XLamp XR-E LED, (b) StarBoard substrate, and (c) White XR-E LED mounted on star substrate and used in immersion testing.

Two cases were studied; one with the LED package open to air placed on a large heat-sink in room temperature and the other with the LED immersed in a dielectric fluid. The LED was placed on the heat sink using a thin layer of zinc-oxide-filled silicone thermal grease. The dielectric fluid selected for this study was the Novec™649, manufactured by 3M™. It is an advanced fluoroketone fluid with the lowest Global Warming Potential (GWP) of its kind. Its saturation temperature is 49°C, which was suitable for this study because it minimizes junction temperature rises and thermal stress. Figure 4.5 shows the experimental setup with the LED placed on a large heat-sink in room temperature and Figure 4.6 shows the setup used for the pool boiling study. Room temperature was 22 ± 1°C, as measured by a Type K thermocouple near the device.

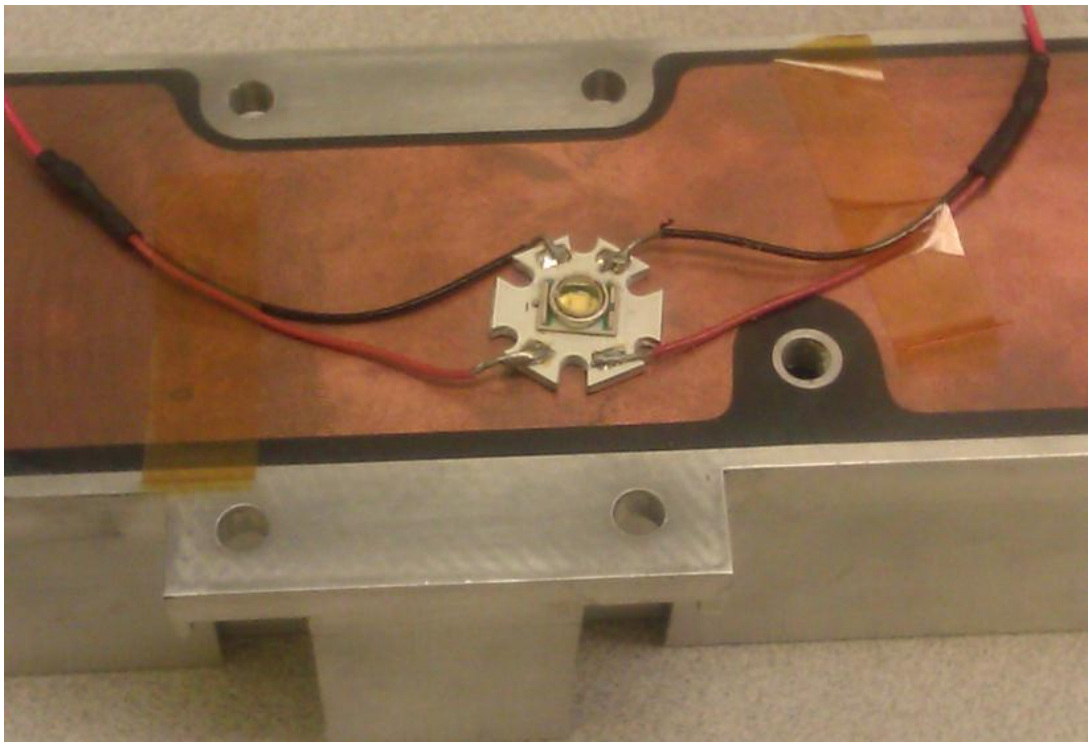


Figure 4.5 Test setup of a white light LED placed on a large, air-cooled copper heat sink.

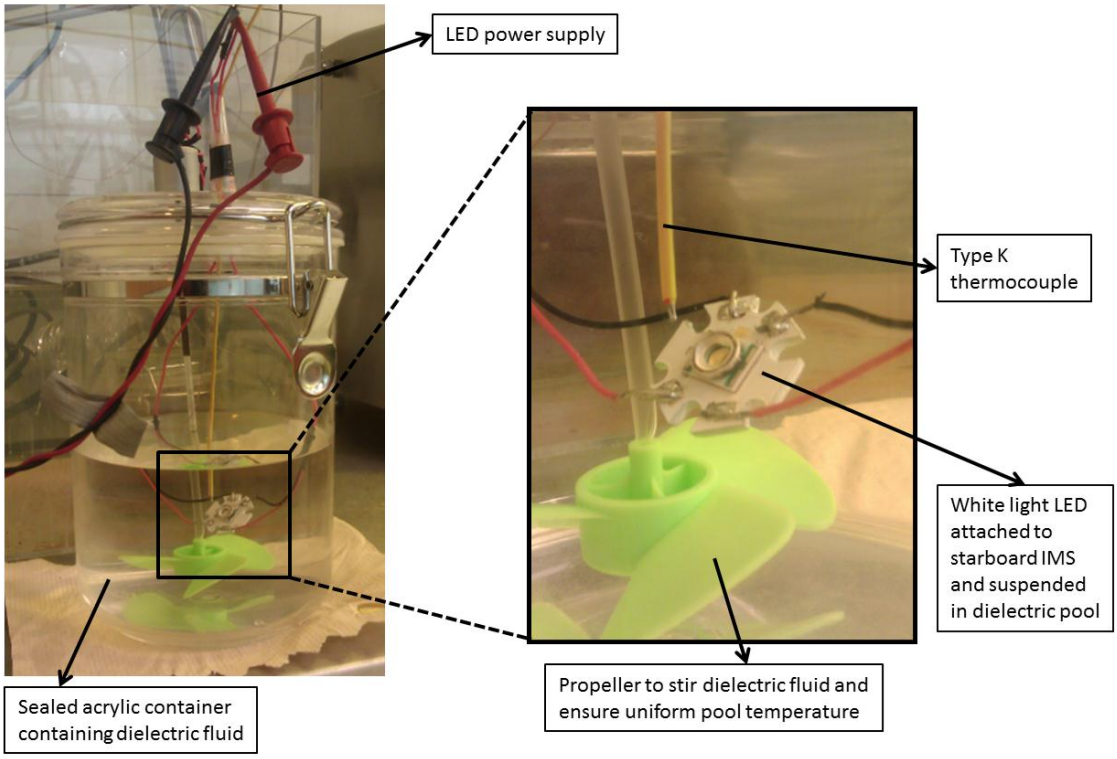


Figure 4.6 Experimental setup of immersion cooling of a commercial white light LED.

The immersion cooling system consisted of the white light LED being immersed in a sealed acrylic container containing the heat transfer fluid and a propeller to stir the fluid and ensure uniform temperature. A Type K thermocouple was also placed in the dielectric pool to measure the bulk fluid temperature throughout the experiment. The entire setup was allowed to reach thermal equilibrium at room temperature before the LED was operated and forward voltage data recorded. The LED was driven at three distinct power levels corresponding to input currents of 100 mA, 300 mA, and 500 mA; the resulting power conditions were approximately 299 mW, 984 mW, and 1.74 W respectively. The temperature measurement technique described in Section 4.2.3 was followed in this study.

4.3.2 Experimental Results

The average steady state junction temperature was extracted from the collected transient data. Hence the average junction-temperature rise as a function of input current is compared for the two experimental setups; see Figure 4.7.

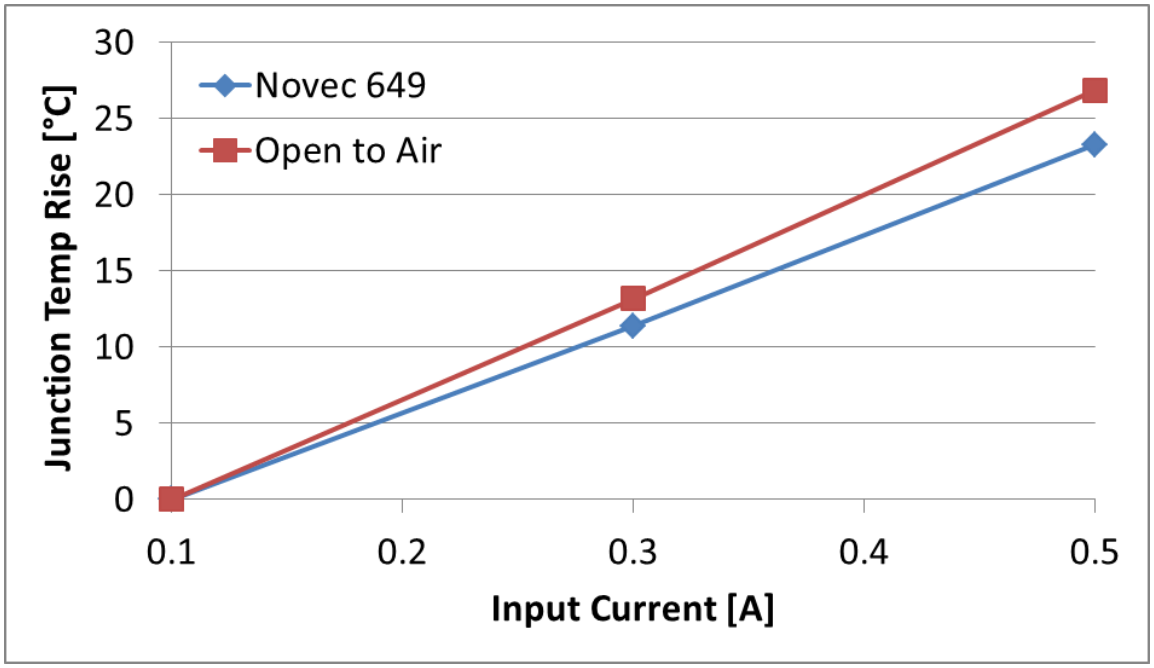


Figure 4.7 Plot shows the average junction-temperature rises above ambient for the white LED versus the input current. 'Novec™649' represents the dielectric fluid and the immersion cooling results while the 'open to air' results are for the LED attached to the large heat sink at room temperature.

The plot in Figure 4.7 shows the effectiveness of the dielectric fluid as opposed to air. At an input current of 500 mA, the immersed LED showed a 13% reduction in junction-temperature rise from air cooling. This significant improvement via immersion cooling was further supported by the results of Arik et al. A 60% performance enhancement with the use of a heat transfer fluid was reported [87]. Those results were exacerbated by the fact that the maximum power in their study was 2.3 W while the maximum power in this study was 1.7 W. Also the experimental configurations and methodology, as well as test fluid and devices were different. In that study, three bare LED chips were attached to a PCB board and covered with a glass dome and the PCB

was insulated on the backside to create an adiabatic boundary condition and force the heat to travel up through the dome. The dome was filled with different optical fluids and binders as well as air and the LEDs' thermal performance was studied. Nonetheless, the benefits of immersion cooling for passive thermal management of LEDs were demonstrated; as opposed to passive or air cooling.

4.4 Summary & Conclusions

In the first investigation, two novel attach materials were studied to discern their influences in heat dissipation for a yellow light LED. The performance of both materials was compared with common thermal grease. Paraffin wax, a phase change material, was first studied. Its heat storage capability displayed better performance than the grease initially but proved to be a poor thermal conductor once in the liquid phase more than doubling the junction temperature rise. Next, Galinstan, a liquid metal at room temperature, was studied. The eutectic alloy demonstrated a thermal advantage, keeping the junction temperature 2°C cooler than the commercial grease. Both materials have advantages but only in specific situations; the paraffin wax needs to be operated in pulsed or intermittent applications and the Galinstan needs to be electrically isolated as to not short the device.

In the second investigation, an experimental study was performed to obtain the thermal behaviors of a white light high brightness LED using two different heat transfer mediums. First free convection in air, with the LED on a finned heat-sink, was studied. This setup is common in the LED industry for heat dissipation. Next, immersion cooling with the dielectric fluid Novec™649 was studied. Superior thermal results were observed in the fluid over air. In fact, the heat transfer was improved by over 13%. The maximum powers tested did not surpass the dielectric fluid's saturation temperature and therefore

the increased heat transfer from nucleate boiling was not realized. Therefore it is believed that with increased input powers, the heat transfer enhancement of immersion cooling will even be greater.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

The development of UV LEDs has a major technological role to play in providing solid state light sources that emit in the UV-C range. These light sources have poor efficiencies and thus major work is needed to address this issue and expand the range of applications for these devices. Currently, they are being sought for use in water purification, bio-agent detection, solar blind communications, and manufacturing. Due to the wavelength of the emitted photons, there are numerous constraints on the materials that can be used as well as the packaging architecture for the thermal management of UV LEDs. The work presented in this thesis has investigated both the thermal and stress response of AlGaN/GaN based UV LED packages. FEA and experimental analysis was presented which provided insight into the salient aspects that impact this response.

The main focus of this work was the parametric study of UV LED packaging components by the way of finite element modeling. The study utilized thermal resistance analysis as well as peak temperatures, peak stresses and displacements to elucidate the contribution of each component on the overall performance of the modeled device. It is believed that these devices experience early degradation and low efficiencies owing to the coupled effects of fabrication challenges, optical, electrical, thermal, and mechanical issues. This complex problem is studied in some detail in this work, with a major focus on overall package thermal resistance as a function of varying geometric parameters and material properties, thermal stresses as a function of CTE mismatch, and alternative cooling techniques. Key findings that were discussed in the previous chapters are reiterated below.

- The largest bottleneck for improved thermal performance is the thermal interface material layer. A large temperature gradient exists in the thermal grease layer

leading to a large contribution to the overall package thermal resistance. Alternative material choices for the interfacial material between the sub-mount and the heat slug should strongly be considered. Eutectic gold-tin solder was shown to have significant improvement on the thermal performance in place of the thermal epoxy. It has excellent wettability allowing very thin layers (10 µm or less), excellent resistance to corrosion, high thermal conductivity, high joint strength, and fluxless process. In addition it has good CTE matching with various packaging materials such as ceramics, and copper [1]. The improvement in thermal resistance and peak temperatures allows the device to be operated at higher powers with manageable thermal drawbacks.

- The sub-mount was shown to have a significant impact on the overall package thermal resistance. This was shown through a parametric study where lateral area, thickness, and thermal conductivity were varied and the thermal performance was examined. It was determined that the lateral area ratio between the sub-mount and the UV LED is important as it facilitates in heat spreading and heat-flux reduction. Therefore a sub-mount with a larger lateral area than the diode is necessary for good heat spreading but a large ratio between these areas proves to be ineffective as it does not have a significant effect on heat spreading after a certain optimum area or "effective heat spreading area". The data showed an exponential decrease in resistance with increasing AR, meaning that the largest reduction in overall thermal resistance was seen in a change from AR=1 to AR=2. It was also determined that the thickness had the lesser impact when compared to AR for a given material but had a meaningful impact when comparing thickness and thermal conductivity for a set sub-mount-to-die area ratio. This means that the AR is the dominating parameter in reducing overall thermal resistance. With an optimum sub-mount-to-die area ratio, there's flexibility on the thickness and thermal conductivity of the sub-mount, as far as thermal resistance is concerned.

- *P* and *N* metal contacts were shown to have a bigger impact on the junction temperature than the solder pads used to connect the chip to the sub-mount. Using the same solder pad material, gold contacts resulted in a lower junction temperature than gold-tin contacts. In addition, using the same metal contact material, the use of gold-tin solder pads versus gold solder pads proved to have a small effect on the maximum device temperature. This means that it is important for the metals contacts to have a high thermal conductivity and not as important for the solder pads to have high thermal conductivities.
- The etched copper circuit layer was shown to have a low impact on thermal performance of the modeled flip-chipped UV LED device.
- Thermal vias embedded in the AlN sub-mount provided little improvement in the UV LED modeled.
- Thermal stress modeling showed that the highest stress regions, caused by CTE mismatches, were found to be in the interfacial and attach layers, reinforcing the need to reduce thermal resistance in these layers.
- Interdigitated Micro Pixelated Array (IMPA) LED modeling showed the effects of pixel density on thermal performance. It was shown that a 60-pixel array caused a significant increase in junction-temperature rise over a 24-pixel array; by two orders of magnitude.
- Alternative attach materials were investigated experimentally to discover new and innovative cooling techniques. Galinstan, a liquid metal and Paraffin wax, a phase change material were explored as potential second level thermal interface materials. Both test materials performed better than regular thermal grease initially but the paraffin wax performed the worst because of its low thermal conductivity once in the liquid phase. In summary, it was shown that Galinstan is

a potential interfacial material because of its high thermal conductivity and Paraffin wax also displayed good potential because of its excellent heat storing abilities, but should only be considered in cyclic applications to avoid the very low thermal conductivity of liquid Paraffin.

- The thermal performance of a commercially-available white light LED was studied under different boundary conditions. Two forms of convection, free or natural convection and nucleate boiling, were compared. The purpose of the investigation was to ascertain if pool boiling would cool the LED better than air, by studying junction-temperature rises above the ambient for the two setups. The data showed a 13% decrease in junction-temperature rise for the pool boiling case, at a maximum power of 1.7 W.

Future Work

Continued research in UV LED modeling and characterization is vital in investigating innovative solutions to the thermal problem. The research in this thesis was mainly focused on studying heat dissipation of the interdigitated multifinger chip design. As such the micro-pixelated array design was not covered in depth and needs to be further studied to find optimum array configurations for increased thermal dissipation. A parametric study should be conducted studying things such as pixel radius, pixel pitch, as well as other packaging aspects that influence thermal performance. Furthermore, electro-thermal-mechanical models should be used to understand the coupled electrical-thermal-mechanical relationship present in UV LEDs in general. There is very little understanding of how the coupled response leads to the heat distribution within the active portion of the LED. This will give device growth engineers and designers more insight into the impact that doping and the formation of *p* and *n* contacts has on the performance of the device. It is not clear at this time how much additional thermal control can be gained by coupling

thermal design into the chip architecture as opposed to simply managing the heat loads via the packaging materials. Finally, additional work needs to be done to couple the thermal packaging design along with the optical design for UV LED systems. As of now, these are treated as separate challenges, but they are truly coupled in the design of LED luminaires. This will illuminate the bigger picture of device-operation behavior and lead to realistic conclusions on how to apply them in a wide range of applications.

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