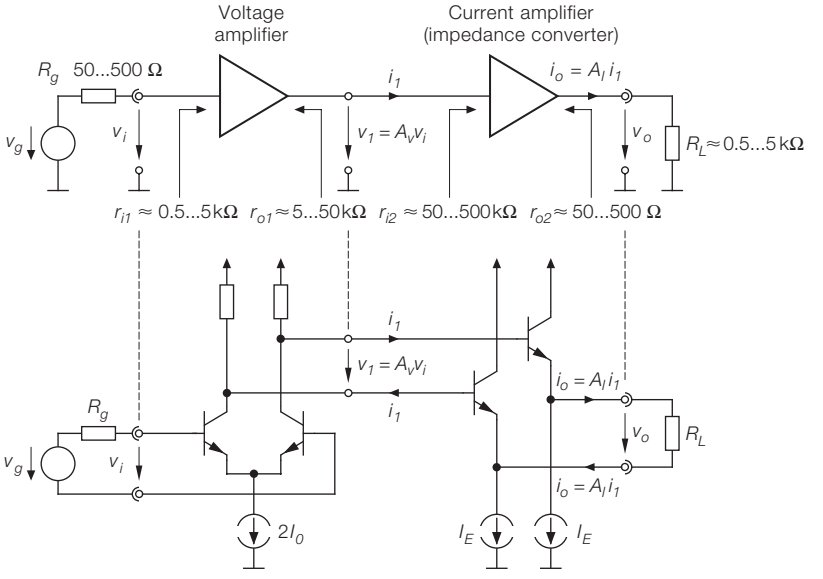
Chapter 27: High-Frequency Amplifiers

Today, in the high- and intermediate-frequency assemblies of telecommunication systems, amplifiers composed of discrete transistors are still used in addition to modern integrated amplifiers. This is particularly the case in high-frequency power amplifiers employed in transmitters. In low-frequency assemblies, on the other hand, only integrated amplifiers are used. The use of discrete transistors is due to the status quo of semiconductor technology. The development of new semiconductor processes with higher transit frequencies is soon followed by the production of discrete transistors, but the production of integrated circuits on the basis of a new process does not usually occur until some years later. Furthermore, the production of discrete transistors with particularly high transit frequencies often makes use of materials or processes which are not (or not yet) suitable for the production of integrated circuits in the scope of production engineering or for economic reasons. The high growth rate in radio communication systems has, however, boosted the development of semiconductor processes for high-frequency applications. Integrated circuits on the basis of compound semiconductors such as gallium-arsenide (GaAs) or silicon-germanium (SiGe) can be used up to the GHz range. For applications up to approximately 3 GHz bipolar transistors are mainly used, which, in the case of GaAs or SiGe designs, are known as *hetero-junction* bipolar transistors (HBT). Above 3 GHz, gallium-arsenide junction FETs or *metal-semiconductor field effect transistors* (MESFETs) are used.[1] The transit frequencies range between 50 . . . 100 GHz.

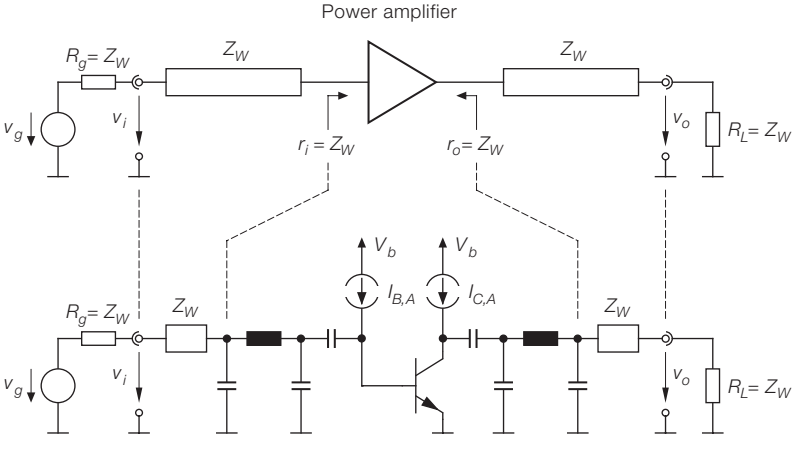
27.1 Integrated High-Frequency Amplifiers

In principle, integrated high-frequency amplifiers use the same circuitry as low-frequency or operational amplifiers. A typical amplifier consists of a differential amplifier used as a voltage amplifier and common-collector circuits used as current amplifiers or impedance converters (see Fig. 27.1a). The differential amplifier is often designed as a cascode differential amplifier to reduce its reverse transmission and its input capacitance (no Miller effect). Such circuits are described in Chap. 4, Sect. 4.1. Since the transit frequency of high-frequency transistors ($f_T \approx 50 \ldots 100\,\text{GHz}$) is approximately 100 times higher than that of low-frequency transistors ($f_T \approx 500\,\text{MHz} \ldots 1\,\text{GHz}$), the bandwidth of the amplifier increases by approximately the same factor. This, however, presumes that the parasitics of the bond wires and the connections within the integrated circuit can be reduced enough so that the bandwidth is primarily determined by the transit frequency of the transistors and is not limited by the connections. This is a key problem in both the design and use of high-frequency semiconductor processes.

[1] The construction of an HBT corresponds to that of a conventional bipolar transistor. Here, however, different material compositions are used for the base and emitter regions in order to enhance the current gain at high frequencies. The construction of a MESFET is shown in Fig. 3.26b on page 198.



a Principle and design of an integrated amplifier



b Principle and design of a matched amplifier with one discrete transistor

Fig. 27.1. Principle construction of high-frequency amplifiers

27.1.1 Impedance Matching

Generally, the connecting leads within integrated circuits are so short that they can be considered as ideal connections even in the GHz range;[2] therefore, it is not necessary to carry out matching to the characteristic impedance within the circuit. In contrast, the external

[2] These are *electrically short lines* (see Sect. 26.2). In this context the term *ideal* does not refer to the losses; these are relatively high in integrated circuits due to the comparably thin metal coating and the losses in the substrate.

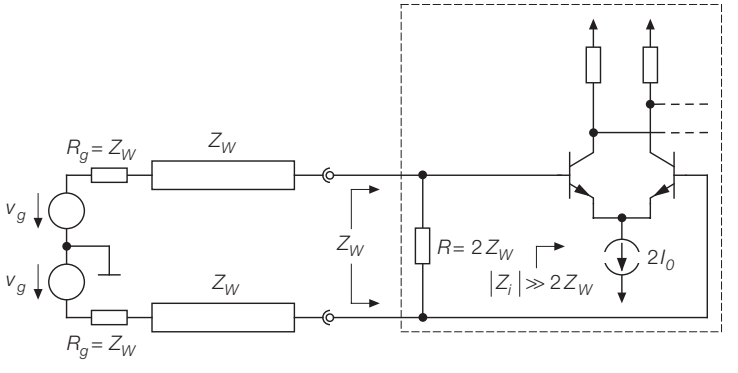
signal-carrying terminals must be matched to the characteristic impedance of the external lines to prevent any reflections. In the ideal case, the circuit is dimensioned such that input and output impedances, including the parasitic effects of bond wires, connecting limbs and the case, correspond to the characteristic impedance. Otherwise, external components or strip lines must be used for impedance matching (see Sect. 26.3).

Figure 27.1a shows typical values of low-frequency input and output resistances of the voltage and the current amplifier in an integrated high-frequency amplifier where it is assumed that equivalent amplifiers are employed as signal source and load.

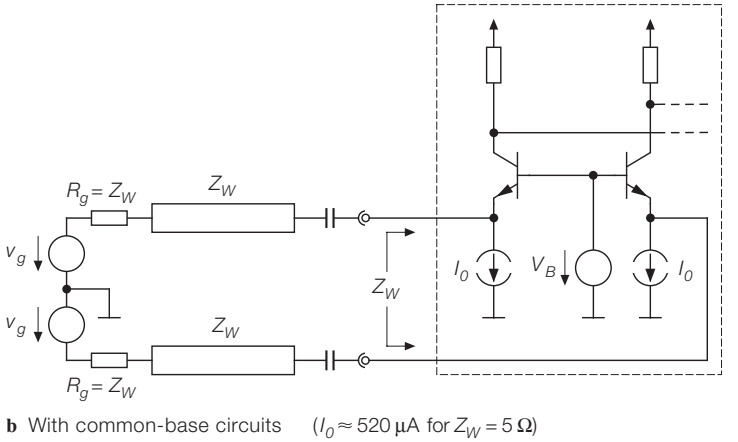
Impedance Matching at the Input

For high frequencies, the input impedance of a differential amplifier is ohmic-capacitive due to the capacitances of the transistor. Generally, up to around 100 MHz, its value is clearly higher than the usual characteristic impedance $Z_W = 50\,\Omega$.

A rigorous impedance matching method involves inserting a terminating resistance $R = 2Z_W = 100\,\Omega$ between the two inputs of the differential amplifier (see Fig. 27.2a);



a With terminating resistance



b With common-base circuits ($I_0 \approx 520\,\mu A$ for $Z_W = 5\,\Omega$)

Fig. 27.2. Impedance matching at the input side of an integrated amplifier

this matches both inputs to $Z_W = 50\,\Omega$. This method is simple, easy to accomplish with a resistor in the integrated circuit and acts across a wide band. A disadvantage is the poor power coupling owing to the dissipation of the resistor and the large increase in the noise figure (see Sect. 27.1.2). Instead of placing a resistance $R = 2Z_W$ between the two inputs, each of the two inputs can be connected to ground via a resistance $R = Z_W$. However, this means that a galvanic coupling to signal sources with a DC voltage is no longer possible as the inputs are connected to ground with low resistance. The version with a resistance $R = 2Z_W$ is thus preferred.

As an alternative, common-base circuits can be used for the input stages (see Fig. 27.2b); then, the input impedance corresponds approximately to the transconductance resistance $1/g_m = V_T/I_0$ of the transistors. With a bias current $I_0 \approx 520\,\mu\text{A}$, this resistance is $1/g_m \approx Z_W = 50\,\Omega$. In this case, the power coupling is optimal. A disadvantage is the comparably high noise figure (see Sect. 27.1.2).

Both methods are suitable for frequencies in the MHz range only. In the GHz range, the influence of the bond wires, the connecting limbs and the casing have a noticeable effect. The situation can be improved by using loss-free matching networks made up of reactive components or strip lines that must be fitted externally. This will provide an optimum power coupling with a very low noise figure. In practice, impedance matching focuses less on optimum power transmission than it does on optimum noise figure, or a compromise between both optima. This is described in more detail in Sect. 27.1.2.

Impedance Matching at the Output

Wideband matching of the output impedance of a common-collector circuit to the usual characteristic impedance $Z_W = 50\,\Omega$ can be achieved by influencing the output impedance of the voltage amplifier while taking into consideration the impedance transformation in a common-collector circuit. For the qualitative aspects refer to Fig. 2.105a on page 149 and to the case shown in the left portion of Fig. 2.106 where the output impedance of a common-collector circuit has a wideband ohmic characteristic if the preceding amplifier stage has an ohmic-capacitive output impedance with a cut-off frequency that corresponds to the cut-off frequency $\omega_\beta = 2\pi f_\beta$ of the transistor. Due to secondary effects this type of matching can be achieved *quantitatively* only with the aid of circuit simulation. Again, in the GHz range, the influence of the bond wires, the connecting limb and the casing show a disturbing effect. In principle, impedance matching remains possible, but not with the wideband effect.

If impedance matching is not possible by influencing the output impedance of the common-collector circuit, external matching networks with reactive components or strip lines are used.

27.1.2 Noise Figure

In Sect. 2.3.4 we showed that the noise figure of a bipolar transistor with a given collector current $I_{C,A}$ is minimum if the effective source resistance between the base and the emitter terminal reaches its optimum value:

$$R_{g\,opt} = \sqrt{R_B^2 + \frac{\beta\, V_T}{I_{C,A}}\left(\frac{V_T}{I_{C,A}} + 2R_B\right)} \overset{R_B \to 0}{\approx} \frac{V_T\sqrt{\beta}}{I_{C,A}} \tag{27.1}$$

Here, R_B is the base spreading resistance and β the current gain of the transistor. For the collector currents $I_{C,A} \approx 0.1 \ldots 1\,\text{mA}$, which are typical of integrated high-frequency circuits, the source resistance for $\beta \approx 100$ is in the region $R_{g\,opt} \approx 260 \ldots 2600\,\Omega$. With larger collector currents, $R_{g\,opt}$ can be further reduced, e.g. to $50\,\Omega$ at $I_{C,A} = 23\,\text{mA}$ and $R_B = 10\,\Omega$, but the noise figure reaches only a local minimum as shown in Fig. 2.52 on page 92. This is caused by the base spreading resistance. Very large transistors with very small base spreading resistances are used in low-frequency applications which enables the global minimum of the noise figure to be nearly reached even with small source resistances. However, in this case the transit frequency of the transistors drops rapidly; thus, in high-frequency applications, this method can be used in exceptional cases only.

In impedance matching at the input side by means of a terminating resistance as shown in Fig. 27.2a, the effective source resistance has the value $R_{g,eff} = R_g || R/2 = Z_W/2 = 25\,\Omega$ for each of the two transistors in the differential amplifier due to the parallel connection of the external resistances $R_g = Z_W$ and the internal terminating resistance $R = 2Z_W$. It is thus clearly lower than the optimum source resistance $R_{g\,opt} \approx 260 \ldots 2600\,\Omega$. Furthermore, the noise of the terminating resistance causes the noise figure to become relatively high. With impedance matching at the input side by means of a common-base circuit as shown in Fig. 27.2b, the effective source resistance has the value $R_{g,eff} = R_g = Z_W = 50\,\Omega$; here, too, the noise figure is comparably high.

For impedance matching with reactive components or strip lines, the internal resistance R_g of the signal source can be matched to the input resistance r_i of the transistor by means of a loss-free and noise-free matching network. If we disregard the base spreading resistance R_B, then $r_i = r_{BE}$. For the effective source resistance $R_{g,eff}$ between the base and emitter terminals this means that $R_{g,eff} = r_{BE}$. For $r_{BE} = \beta V_T / I_{C,A}$ and $R_{g\,opt}$ the following relationship is obtained from (27.1) with $R_B = 0$:

$$R_{g,eff} = r_{BE} = R_{g\,opt}\sqrt{\beta} \tag{27.2}$$

Thus, with impedance matching, the effective source resistance is higher than the optimum source resistance by a factor of $\sqrt{\beta} \approx 10$. This might make the noise figure lower than that in the configurations with a terminating resistance or a common-base circuit, but it is still clearly higher than the optimum noise figure.

The optimum noise figure is only obtained when noise matching is performed instead of power matching. This means that the internal resistance $R_g = Z_W$ of the signal source is not matched to $r_i = r_{BE}$ but to $R_{g\,opt} = r_{BE}/\sqrt{\beta}$. Conversely, the input resistance of the (noise) matched amplifier is no longer Z_W but $Z_W\sqrt{\beta}$. This leads to the input reflection factor

$$r \overset{(24.34)}{=} \frac{Z_W\sqrt{\beta} - Z_W}{Z_W\sqrt{\beta} + Z_W} = \frac{\sqrt{\beta} - 1}{\sqrt{\beta} + 1} \overset{\beta \approx 100}{\approx} 0.82$$

and a standing wave ratio *(SWR)*:

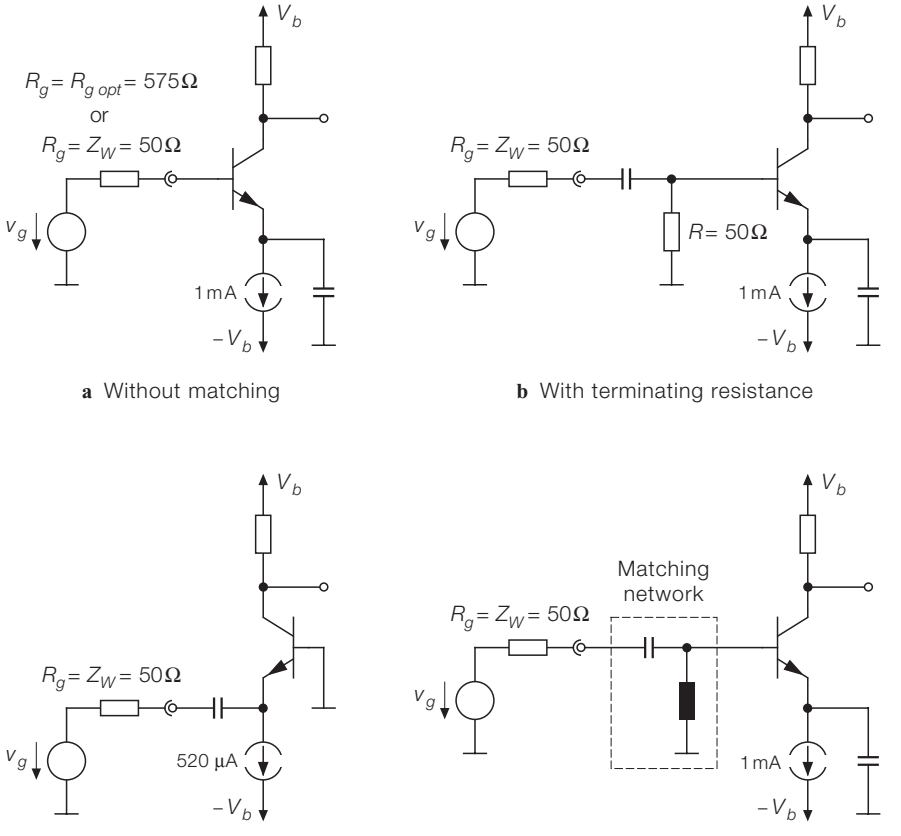
$$s \overset{(24.42)}{=} \frac{1 + |r|}{1 - |r|} = \sqrt{\beta} \overset{\beta \approx 100}{\approx} 10$$

In most applications this is not acceptable. Therefore, a compromise between power and noise matching is used in most practical cases where a low noise figure is of importance. Power matching is generally used if the noise figure is of no importance.

Above $f = f_T/\sqrt{\beta} \approx f_T/10$ the optimum source resistance decreases, as can be seen from the equation for $R_{g\,opt,RF}$ in Sect. 2.3.4. This does not mean that the matching

methods in Fig. 27.2 can achieve a lower noise figure in this range. Factor $R_{g,eff}/R_{g\,opt}$ does go down but the minimum noise figure increases as the equation for $F_{opt,RF}$ in Sect. 2.3.4 shows. We will not examine this range more closely as the noise model for bipolar transistors with a transit frequency above 10 GHz as used in Sect. 2.3.4 will only allow qualitative statements in this case. The range $f > f_T/10$ is then entirely in the GHz range and some secondary effects, such as the correlation between the noise sources of the transistor, which were disregarded in Sect. 2.3.4, become significant, and the optimum source impedance is no longer real.

Example: With the help of circuit simulation we have determined the noise figure of the different circuit versions for an integrated amplifier with the transistor parameters in Fig. 4.5 on page 278. Owing to the symmetry, we can restrict the calculations to one of the two input transistors; Fig. 27.3 shows the corresponding circuits. We use a transistor of size 10 and a bias current of $I_{C,A} = 1$ mA. In the common-base circuit according to Fig. 27.3c, we reduce the bias current to 520 µA in order to achieve impedance matching to $Z_W = 50\,\Omega$.



a Without matching

b With terminating resistance

c With common-base circuit

d With matching network
(power matching or noise matching)

Fig. 27.3. Circuits for a noise figure comparison

The base spreading resistance is $R_B = 50\,\Omega$ and the frequency $f = 10\,\text{MHz}$. From (27.1) it follows that $R_{g\,opt} = 575\,\Omega$ for $I_{C,A} = 1\,\text{mA}$ and $R_{g\,opt} = 867\,\Omega$ for $I_{C,A} = 520\,\mu\text{A}$.

The circuit without matching in Fig. 27.3a achieves an optimum noise figure $F_{opt} = 1.12$ (0.5 dB) for $R_g = R_{g\,opt} = 575\,\Omega$ and $F = 1.52$ (1.8 dB) for $R_g = 50\,\Omega$. The circuit with terminating resistance in Fig. 27.3b results in the noise figure $F = 2.66$ (4.2 dB); the noise figure thus clearly increases. A more favourable value is achieved with the common-base circuit in Fig. 27.3c where $F = 1.6$ (2 dB). With power matching to $R_g = Z_W = 50\,\Omega$, according to Fig. 27.3d, the value obtained is $F = 1.25$ (0.97 dB), which is only a factor of 1.1 (0.5 dB) above the optimum value. The optimum noise figure is achieved with noise matching.

If power matching is essential in order to prevent reflections, the circuit with matching network and power matching according to Fig. 27.3d leads to the lowest noise figure, followed by the common-base circuit in Fig. 27.3c and then the circuit with terminating resistance in Fig. 27.3b. Without power matching, the circuit with matching network and noise matching according to Fig. 27.3d is clearly superior to the circuit without matching in Fig. 27.3a for $R_g = 50\,\Omega$ with regard to both the noise figure and the reflection factor.

27.2 High-Frequency Amplifiers with Discrete Transistors

Figure 27.1b shows the principle design of high-frequency amplifiers made up of discrete transistors. It is clear that the circuit design differs fundamentally from that of the integrated amplifier shown in Fig. 27.1a. The actual amplifier consists of a bipolar transistor in common-emitter configuration and circuitry for setting the operating point, which is presented in Fig. 27.1b, by the two current sources $I_{B,A}$ and $I_{C,A}$. The practical functionality will be further described below. Instead of a bipolar transistor, a field effect transistor can also be used. Coupling capacitances are used in front of and behind the transistor to prevent the operating point from being influenced by the additional circuitry. The networks for impedance matching to the characteristic impedance of the signal lines include π elements (Collins filters) with a series inductance and two shunt capacitances as shown in Fig. 27.1b.

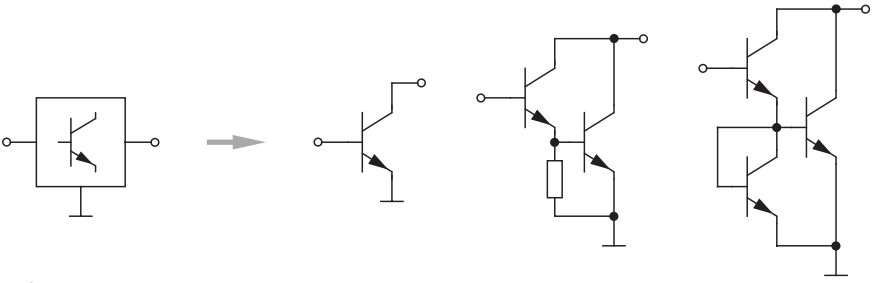
27.2.1 Generalised Discrete Transistor

The term *discrete transistor* should not be misunderstood in a limited sense because the components used in practice often contain several transistors and additional resistances and capacitances in order to simplify the process of setting the operating point. We call these components *generalised discrete transistors*.[3]

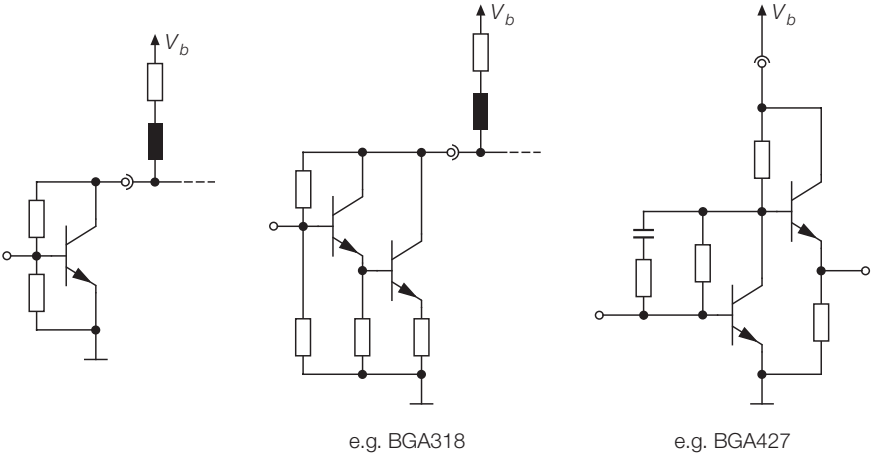
Figure 27.4a shows the graphic symbol and the most important versions of a generalised discrete transistors without additional components for setting the operating point. A Darlington circuit is often used to enhance the current gain at high frequencies.

Figure 27.4b presents some typical designs with additions for setting the operating point. The version at the left can be used equally well for the Darlington circuits in Fig. 27.4a. The resistances provide a voltage feedback which, at sufficiently high-resistive

[3] This can be related to the CC operational amplifier which may also be regarded as a generalised discrete transistor (see Sect. 5.5 and Figs. 5.82 to 5.87).



a Symbol and circuit configurations



b Circuit configurations with additional elements for setting the operating point

Fig. 27.4. Generalised discrete transistor

dimensions, becomes virtually inefficient at high frequencies if the impedance of the collector-base capacitance falls below the value of the feedback resistor. The external element is an inductance which represents an open circuit at the operating frequency and consequently causes a separation of the signal path and the DC path. The version shown in the centre of Fig. 27.4b has an additional emitter resistance for current feedback; therefore, it is particularly suitable for wideband amplifiers or amplifiers with a high demand in terms of linearity.

The version shown at the right of Fig. 27.4b consists of a common-emitter circuit with voltage feedback followed by a common-collector circuit. Strictly speaking, this does not belong to the group of discrete transistors since, like the integrated amplifier in Fig. 27.1b, it comprises a voltage amplifier (common-emitter circuit) and a current amplifier (common-collector circuit). Nevertheless, we have included it since it usually comes in a casing that is typical of discrete transistors. The voltage feedback is often operated with two resistances and one capacitance. Only the resistance, which is directly connected between the base and the collector, influences the operating point and is used for setting the collector voltage at the operating point. The capacitance is given dimensions such that it functions as a short circuit at the operating frequency, thus allowing the parallel arrangement of the two resistances to become effective.

The versions shown in Fig. 27.4 are regarded as low-integrated circuits and are termed *monolithic microwave integrated circuits (MMIC)*. They are made of silicon (Si-MMIC), silicon-germanium (SiGe-MMIC) or gallium-arsenide (GaAs-MMIC) and are suitable for frequencies of up to 20 GHz.

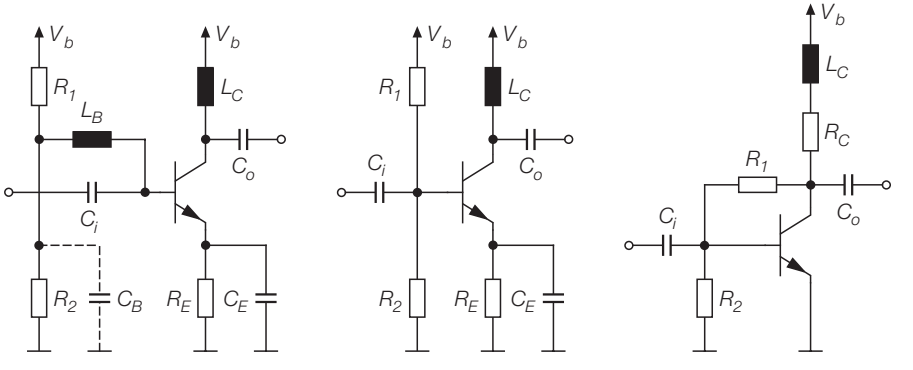
27.2.2 Setting the Operating Point (Biasing)

Generally, the operating point is set in the same way as for low-frequency transistors. However, with high-frequency transistors, one attempts to make the resistances required in order to set the operating point ineffective at the operating frequency otherwise they will have an adverse effect on the gain and noise figure. For this reason, the resistances are combined with one or more inductances which can be considered short-circuited with regard to setting the operating point, and nearly open-circuited at the operating frequency.

A description of how the operating point is set in a bipolar transistor is given below. The circuits described may equally well be used for field effect transistors.

DC Current Feedback

If we apply the above-mentioned principle to the operating point adjustment with DC current feedback as shown in Fig. 2.75a on page 119, we obtain the circuit design shown in Fig. 27.5a in which high-frequency decoupling is achieved for the base and the collector of the transistor by means of inductances L_B and L_C respectively. The collector resistance can be omitted in this case. Thus, there is no DC voltage drop in the collector circuit so that this method is particularly suitable for low supply voltages. In extreme situations, one may remove R_1 and R_2 and connect the free contact of L_B directly to the supply voltage; the transistor then operates with $V_{BE,A} = V_{CE,A}$. Due to the decoupled base, the noise of resistors R_1 and R_2 have only very little influence on the noise figure of the amplifier at the operating frequency which is a particularly low-noise method for setting the operating point. This is especially the case if an additional capacitance C_B is introduced which, at



a With current feedback and decoupling of the base (low noise)

b With current feedback and no decoupling of the base

c With voltage feedback

Fig. 27.5. Setting the operating point in high-frequency transistors

the operating frequency, acts almost as a short circuit. Where a slight increase in the noise figure is not critical, it may not be necessary to decouple the base and thus the circuit shown in Fig. 27.5b may be used.

With an increase in frequency decoupling becomes more and more difficult since the characteristics of the inductors used to achieve the required inductance become less favourable. In order to make the magnitude of the impedance as high as possible, an inductor with a resonant frequency that is as close as possible to the operating frequency is used. As a result, the resonant impedance is approximately reached which, however, decreases with an increasing resonant frequency as shown in Fig. 28.4 on page 1406. For this reason, in the GHz range, the inductances are replaced by strip lines of the length $\lambda/4$. These lines are short-circuited for small signals at the end opposite the transistor by capacitance C_B or by connecting them to the supply voltage. The end closest to the transistor then acts as an open circuit.

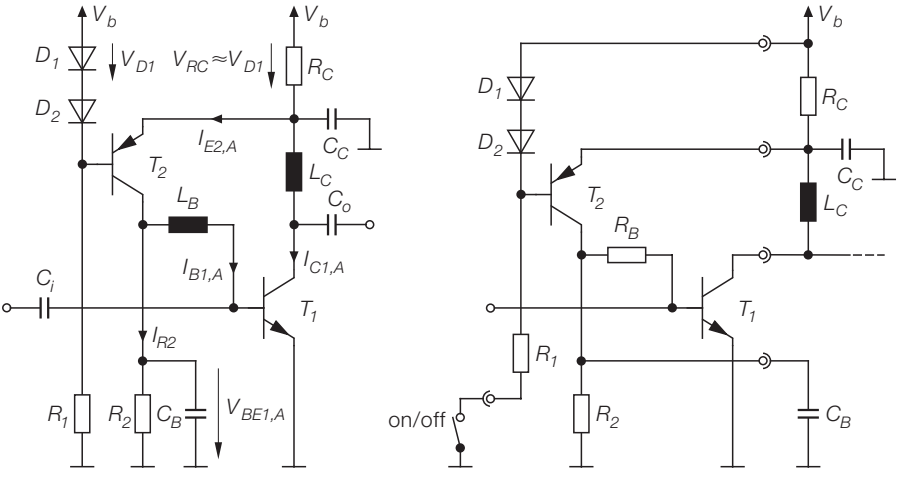
Particularly problematic is the capacitance C_E which, at the operating frequency, must perform as a short circuit. Here, too, a capacitance with a resonant frequency as close as possible to the operating frequency is used, whereby doing so results in impedances with a magnitude close to that for the series resistance of the capacitance (typically $0.2\,\Omega$). However, with increasing resonant frequency, the resonance quality of the capacitances increases (see Fig. 28.5 on page 1406), thus making the adjustment more and more difficult. As an alternative, an open-circuited strip line of length $\lambda/4$ could be used that acts as a short circuit at the transistor end but, owing to the unavoidable radiation at the open-ended side (antenna effect), this method is not practical. A short-circuited strip line must also be rejected as it provides a short circuit for the DC current and thus short-circuits the resistance R_E. Owing to these problems, the DC current feedback is used only in the MHz range while in the GHz range the emitter terminal of the transistor must be connected directly to ground.

DC Voltage Feedback

Figure 27.5c shows the method of setting the operating point by means of DC voltage feedback. This is used in many monolithic microwave integrated circuits (see Fig. 27.4b). A collector resistance R_C is essential in order to render the feedback effective and to ensure a stable operating point. The collector is decoupled by the inductance L_C so that, at the operating frequency, the output is not loaded by the collector resistance. The base can be decoupled by adding series inductances to the resistances R_1 and R_2; however, this method is not used in practice. A disadvantage is an increase in the noise figure due to the noise contributions from R_1 and R_2, but these can be kept low using high-resistive dimensioning.

Automatic Operating Point Control

Amplifiers, whether consisting of integrated circuits or discrete components, are often provided with automatic control of the operating point as shown in Fig. 27.6. Here, the collector current of the high-frequency transistor T_1 is measured from the voltage drop V_{RC} across the collector resistance R_C and compared with a setpoint value V_{D1}. Transistor T_2 controls the voltage at the base of transistor T_1 so that $V_{RC} \approx V_{D1} \approx 0.7\,\mathrm{V}$.



a Discrete components **b** Integrated circuit (e.g. BGC405)

Fig. 27.6. Automatic operating point control

Let us first look at the circuit in Fig. 27.6a. It follows that:

$$V_{RC} = \left(I_{C1,A} + I_{E2,A}\right) R_C \ , \ V_{BE1,A} = I_{R2} R_2 \ , \ I_{E2,A} \overset{I_{B2,A} \approx 0}{\approx} I_{B1,A} + I_{R2}$$

Consequently:

$$V_{RC} \ = \ \left(I_{C1,A} + I_{B1,A} + \frac{V_{BE1,A}}{R_2} \right) R_C \overset{I_{C1,A} \gg I_{B1,A}}{\approx} \left(I_{C1,A} + \frac{V_{BE1,A}}{R_2} \right) R_C$$

If the emitter-base voltage of transistor T_2 corresponds approximately to the voltage of diode D_2, then:

$$V_{RC} \ \approx \ V_{D1} \quad \Rightarrow \quad I_{C1,A} \ \approx \ \frac{V_{D1}}{R_C} - \frac{V_{BE1,A}}{R_2} \ \approx \ 0,7\,\mathrm{V} \left(\frac{1}{R_C} - \frac{1}{R_2} \right)$$

$R_2 \gg R_C$ is typically the case in practice; thus $I_{C1,A} \ \approx \ 0.7\,\mathrm{V}/R_C$.

The control circuit must have a pronounced low-pass characteristic of the first order to ensure stability; capacitance C_B serves this purpose. It is selected such that the cut-off frequency

$$f_g \ = \ \frac{1}{2\pi C_B \left(R_2 \,||\, r_{BE1}\right)}$$

is below the operating frequency by a factor of at least 10^4.

Figure 27.6b shows the control of the operating point for an integrated circuit where the elements L_C and C_B must be provided externally. The inductance L_B is usually replaced by a resistance which slightly shifts the operating point. Resistance R_C is usually an external component so that the bias current can be adjusted. This adjustment is necessary as the bias current, which is optimum in terms of gain and noise figure, depends on the operating frequency. Furthermore, the ground connection of resistance R_1 is usually accessible from the outside so that the amplifier can be turned on and off by a switch.

27.2.3 Impedance Matching for a Single-Stage Amplifier

Calculation of the matching networks for an amplifier with a generalised single transistor is complex because the impedances at the input and output port depend on the circuitry connected to the other port, respectively; this is due to the internal reactive feedback which also leads to a non-zero reverse transmission. The calculation is usually based on the S parameters of the transistor *including* the circuitry for setting the operating point.

Conditions for Impedance Matching

Figure 27.7 shows a transistor with matching networks and the corresponding reflection factors at various positions. Since these points are fully matched, the reflection factors at the signal source and the load are zero. The matching network at the input side transforms the reflection factor of the signal source from zero to r_g at the transistor input where it meets the input reflection factor r_1 of the transistor. Similarly, the matching network at the transistor output transforms the reflection factor of the load from zero to r_L, which meets the output reflection factor r_2 of the transistor. For two-sided impedance matching, the respective reflection factors must be conjugate complex to one another:

$$r_g = r_1^* \quad , \quad r_L = r_2^* \tag{27.3}$$

The related impedances are also conjugate complex to one another:

$$Z_g = Z_W \frac{1+r_g}{1-r_g} \overset{r_g=r_1^*}{=} Z_W \frac{1+r_1^*}{1-r_1^*} = Z_1^*$$

$$Z_L = Z_W \frac{1+r_L}{1-r_L} \overset{r_L=r_2^*}{=} Z_W \frac{1+r_2^*}{1-r_2^*} = Z_2^*$$

The conditions for power matching are thus met.

Reflection Factors of the Transistor

The reflection factors r_1 and r_2 of the transistor depend on r_L and r_g due to the reverse transmission (see Fig. 27.8). For the transistor, including the circuitry for setting the operating point, the following is true:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

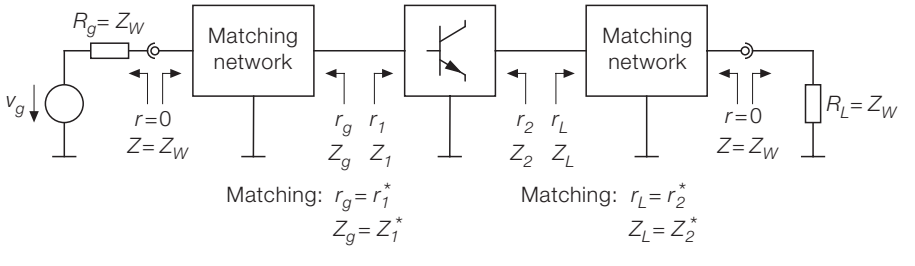
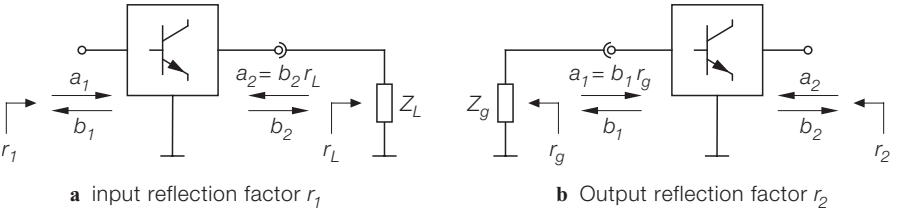


Fig. 27.7. Conditions for impedance matching on both sides



a input reflection factor r_1 **b** Output reflection factor r_2

Fig. 27.8. Calculating the reflection factors of a connected transistor

With a load with reflection factor r_L connected to the output, the input reflection factor r_1 is determined by inserting the condition $a_2 = b_2 r_L$ from Fig. 27.8a and solving the equation for $r_1 = b_1/a_1$. Similarly, the output reflection factor r_2 with a source with reflection factor r_g connected to the input is calculated by inserting the condition $a_1 = b_1 r_g$ from Fig. 27.8b and solving the equation for $r_2 = b_2/a_2$. This leads to:

$$r_1 = S_{11} + \frac{S_{12}S_{21}r_L}{1 - S_{22}r_L} \tag{27.4}$$

$$r_2 = S_{22} + \frac{S_{12}S_{21}r_g}{1 - S_{11}r_g} \tag{27.5}$$

Without reverse transmission ($S_{12} = 0$), there is no interdependence and the reflection factors are $r_1 = S_{11}$ und $r_2 = S_{22}$.

Calculating Impedance Matching

If we insert the conditions (27.3) into (27.4) and (27.5), the reflection factors r_g and r_L of the matched condition are obtained through elaborate calculations [27.1]:

$$r_{g,m} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{27.6}$$

$$r_{L,m} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{27.7}$$

The parameters are:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta_S|^2$$

$$B_2 = 1 - |S_{11}|^2 + |S_{22}|^2 - |\Delta_S|^2$$

$$C_1 = S_{11} - \Delta_S S_{22}^*$$

$$C_2 = S_{22} - \Delta_S S_{11}^*$$

$$\Delta_S = S_{11}S_{22} - S_{12}S_{21}$$

In (27.6) and (27.7) the negative sign applies to $B_1 > 0$ or $B_2 > 0$ and the positive sign to $B_1 < 0$ or $B_2 < 0$.

Stability at the Operating Frequency

To ensure that the amplifier is stable, the following must apply:

$$|r_{g,m}| < 1 \quad , \quad |r_{L,m}| < 1$$

The real parts of the impedances are thus positive:

$$\mathrm{Re}\left\{Z_g\right\} = \mathrm{Re}\{Z_1\} > 0 \quad , \quad \mathrm{Re}\{Z_L\} = \mathrm{Re}\{Z_2\} > 0$$

It can be demonstrated that this is the case when the *stability factor (k factor)* is

$$k = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}S_{21}|} > 1 \tag{27.8}$$

and the secondary conditions

$$|S_{12}S_{21}| < 1 - |S_{11}|^2 \quad , \quad |S_{12}S_{21}| < 1 - |S_{22}|^2 \tag{27.9}$$

are met [27.1].

Without reverse transmission ($S_{12} = 0$), the k factor is $k \to \infty$. In this case the secondary conditions require that $|S_{11}| < 1$ and $|S_{22}| < 1$, i.e. the real parts of the input and output impedances of the transistor, including the circuitry for setting the operating point, must be greater than zero. Therefore, a transistor without reverse transmission can be matched at both sides if the real parts of the impedances are greater than zero. If reverse transmission exists ($S_{12} \neq 0$), the secondary conditions are more stringent and thus positive real parts of the input and output impedance are no longer sufficient. In this case, however, the condition $k > 1$ is more crucial than the secondary conditions, i.e. the secondary conditions are usually met but the condition $k > 1$ is not.

Calculating Matching Networks

If the conditions (27.8) and (27.9) are met, the matching networks can be determined from (27.6) and (27.7) with the help of the reflection factors $r_{g,m}$ and $r_{L,m}$. First, the input and output impedances of the transistor, whose operating point is set for the matched condition, are calculated:

$$Z_{1,m} = Z_W \frac{1 + r_{1,m}}{1 - r_{1,m}} \overset{r_{1,m}=r_{g,m}^*}{=} Z_W \frac{1 + r_{g,m}^*}{1 - r_{g,m}^*} \tag{27.10}$$

$$Z_{2,m} = Z_W \frac{1 + r_{2,m}}{1 - r_{2,m}} \overset{r_{2,m}=r_{L,m}^*}{=} Z_W \frac{1 + r_{L,m}^*}{1 - r_{L,m}^*} \tag{27.11}$$

Using the procedure described in Sect. 26.3, it is now possible to calculate the matching networks for these impedances.

If conditions (27.8) and (27.9) are not met, a straight-forward procedure is not available. In this case a mismatch at the input or output must be accepted. A problem arises in finding suitable reflection factors r_g and r_L for which the mismatch is as small as possible while the operation of the system is sufficiently stable. [27.1] describes a procedure on the basis of stability circles which is not discussed in more detail here. A relatively easy procedure is to connect additional load resistances to the input or output of the transistor so that the S parameters meet the conditions of (27.8) and (27.9). However, it depends on the given application whether this yields a better overall result than a possible slight mismatch.

Stability Across the Entire Frequency Range

The stability conditions (27.8) and (27.9) ensure stability only at the operating frequency for which the matching networks are determined. However, in no way does this guarantee that the amplifier will be stable at all frequencies. This can be investigated by means of a test setup or by simulating the small-signal frequency response across the entire frequency range from zero up to and beyond the transit frequency of the transistor. When measuring the small-signal frequency response with a network analyser it should be noted that, in this case, the amplifier is connected to wide-band circuitry with $R_g = Z_W$ and $R_L = Z_W$. In the actual application, the amplifier may only have narrow-band matching that can cause instability at frequencies other than the operating frequency, i.e. the stability at the network analyser does not necessarily indicate stable operating conditions in the actual application.

Power Gain

For impedance matching on both sides with reactive, i.e. loss-free, matching networks, the *maximum available power gain (MAG)* [27.1]

$$MAG = \left|\frac{S_{21}}{S_{12}}\right| \left(k - \sqrt{k^2 - 1}\right) \tag{27.12}$$

can be determined from (27.8) with the stability factor $k > 1$. This and other power gains are described in Sect. 27.4 in more detail.

Example: The task is to design a high-frequency amplifier with transistor type BFR93 matched at both sides for an operating frequency (centre frequency) $f_C = 1.88\,\text{GHz}$. The supply voltage is to be 3.3 V. We use automatic control of the operating point according to Fig. 27.6a with a bias current of $I_C = 5\,\text{mA}$. For this bias current we obtain a minimum noise figure as stated in the data sheet.[4]

Figure 27.9 shows the dimensioned components of a circuit for setting the operating point. The following aspects were taken into consideration:

- Since the input impedance of the transistor is very low ($\text{Re}\{S_{11}\} < 0 \rightarrow \text{Re}\{Z_i\} < 50\,\Omega$), the inductive decoupling of the base is omitted; therefore, the inductance L_B of Fig. 27.6a is replaced by a resistor $R_B = 1\,\text{k}\Omega$.
- An inductor with $L_C = 33\,\text{nH}$ and a parallel resonant frequency of approximately 1.9 GHz ($C \approx 0,2\,\text{pF}$) is used for the inductive decoupling of the collector.
- A resistor $R_{LC} = 100\,\Omega$ is placed in series with L_C so that at frequencies below the operating frequency it causes losses which increase the k factor in the frequency range 100 MHz ... 1.8 GHz (see Fig. 27.10). This reduces the tendency to oscillate in this frequency range.
- For capacitive blocking at the operating frequency, the capacitors C_{B1} and C_{C1}, whose series resonant frequency is approximately 1.9 GHz, are used ($C = 4.7\,\text{pF}$, size 0604: $L \approx 1.5\,\text{nH}$).

[4] The data sheet also specifies that the maximum transit frequency is reached with $I_C = 20\,\text{mA}$ so that $I_C = 5\,\text{mA}$ is not optimum. However, one should be careful, since the transit frequency is measured with the output short-circuited, allowing only limited conclusions to be drawn as regards to the power gain that can be achieved with impedance matching on both sides. In another design, conducted in parallel to this one, for $I_C = 20\,\text{mA}$ a power gain was achieved that was a mere 0.2 dB greater, a value which does not warrant the bias quiescent current, especially since the noise figure increases significantly.

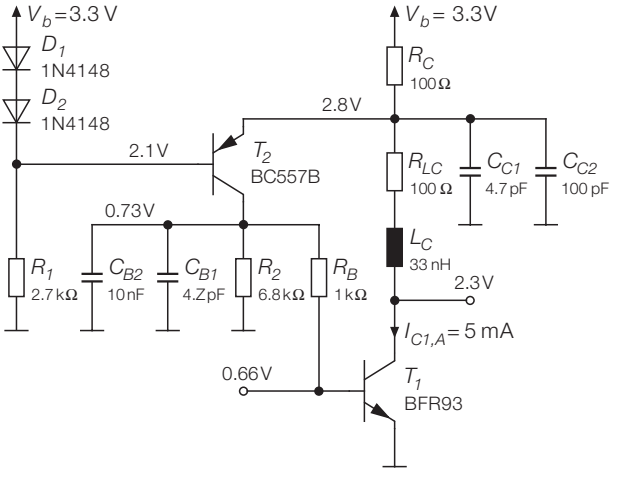


Fig. 27.9. Circuit for setting the operating point of transistor BFR93

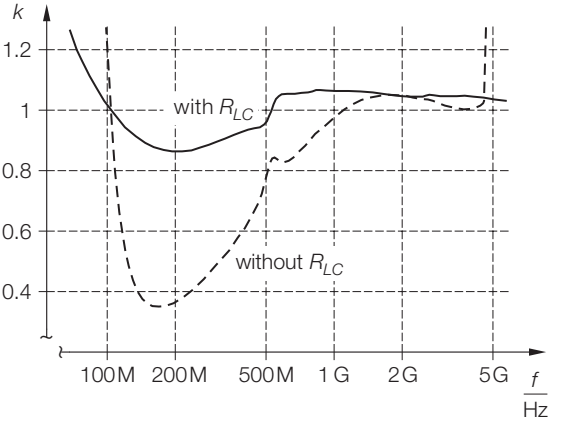


Fig. 27.10. k factor for the circuit shown in Fig. 27.9

– An additional capacitor C_{C2} with a higher capacitance is placed in parallel to C_{C1} in order to improve the capacitive blocking effect at low frequencies.
– Capacitor C_{B2} determines the cut-off frequency of the operating point control and therefore has a relatively high capacitance.

The S parameters of the transistor with operating point setting are determined by circuit simulation:[5]

$$S_{11} = -0.3223 + j\,0.2527 \quad , \quad S_{12} = 0.1428 + j\,0.1833$$
$$S_{21} = 1.178 + j\,1.3254 \quad , \quad S_{22} = 0.09015 - j\,0.249$$

[5] In this simulation, the high-frequency equivalent circuits of resistors and capacitors were taken into consideration. Nevertheless, the results of the simulation cannot be used for a real circuit design since the simulation model for transistor BFR93 provided by the manufacturer is not accurate enough for this frequency range. In practice, the S parameters of the transistor, including the network for setting the operating point, must be measured with a network analyser. In this example we use the S parameters from the simulation so that it can repeated with *PSpice*.

With (27.8) it follows that $k = 1.05 > 1$, i.e. impedance matching on both sides is possible. The power gain to be expected is obtained with (27.12): $MAG = 5.57 \approx 7.5\,\text{dB}$. Equations (27.6) and (27.7) lead to:

$$r_{g,m} = -0.6475 - j\,0.402 \quad , \quad r_{L,m} = 0.3791 + j\,0.6$$

Then, using (27.10) and (27.11) we can calculate the input and output impedances of the transistor with operating point setting in the matched condition:

$$Z_{1,m} = (7.3 + j\,14)\ \Omega \quad , \quad Z_{2,m} = (33 - j\,80)\ \Omega$$

For both impedances, the real part is smaller than $Z_W = 50\,\Omega$ so that matching requires a step-up transformation according to Fig. 26.21a on page 1342.

For matching at the input side we obtain from (26.25) with $R = 7.3\,\Omega$ and $X = 14\,\Omega$:

$$X_1 = \pm 20.7\,\Omega \quad , \quad X_2 = \mp 17.7\,\Omega - 14\,\Omega$$

We select the high-pass filter characteristic ($X_1 > 0$, $X_2 < 0$) according to Fig. 26.22b on page 1343, because then the series capacitance C_2 can simultaneously serve as a coupling capacitor. From

$$X_1 = 20.7\,\Omega \quad , \quad X_2 = -31.7\,\Omega$$

it follows with (26.26) that:

$$L_{1,i} = 1.75\,\text{nH} \quad , \quad C_{2,i} = 2.65\,\text{pF}$$

The additional index i refers to the *input side* matching.

For matching at the output side we obtain from (26.25) with $R = 33\,\Omega$ and $X = -80\,\Omega$:

$$X_1 = \pm 70\,\Omega \quad , \quad X_2 = \mp 24\,\Omega + 80\,\Omega$$

We now select the low-pass filter characteristic ($X_1 < 0$, $X_2 > 0$) according to Fig. 26.22a on page 1343 so that the overall characteristic is that of a band-pass filter. From

$$X_1 = -70\,\Omega \quad , \quad X_2 = 104\,\Omega$$

it follows with (26.26) that:

$$C_{1,o} = 1.2\,\text{pF} \quad , \quad L_{2,o} = 8.8\,\text{nH}$$

The additional index o refers to matching at the *output* side. An additional coupling capacitor is required at the output. We use a 4.7 pF capacitor with a series resonant frequency of 1.9 GHz which, at the operating frequency $f_C = 1.88\,\text{GHz}$, it acts as a short-circuit and thus has no influence on the matching effect.

Figure 27.11 shows the amplifier with the two matching networks. The elements of the matching networks are ideal; at this stage the design is not ready for practical use. It is necessary to check at which points inductors and capacitors can be connected and where strip lines may be advantageous or are mandatory for functionality of the elements. This is not discussed any further; please refer to the notes on impedance matching in multi-stage amplifiers in the next section.

Finally we present the results achieved. The upper part of Fig. 27.12 shows the magnitudes of the S parameters in the matched amplifier at the operating frequency $f_C = 1.88\,\text{GHz}$. One can see that matching covers a relatively narrow frequency band. If the requirements $|S_{11}| < 0.1$ and $|S_{22}| < 0.1$ hold for the reflection factors, then the bandwidth is approximately 53 MHz. Matching at the input covers a narrower band than

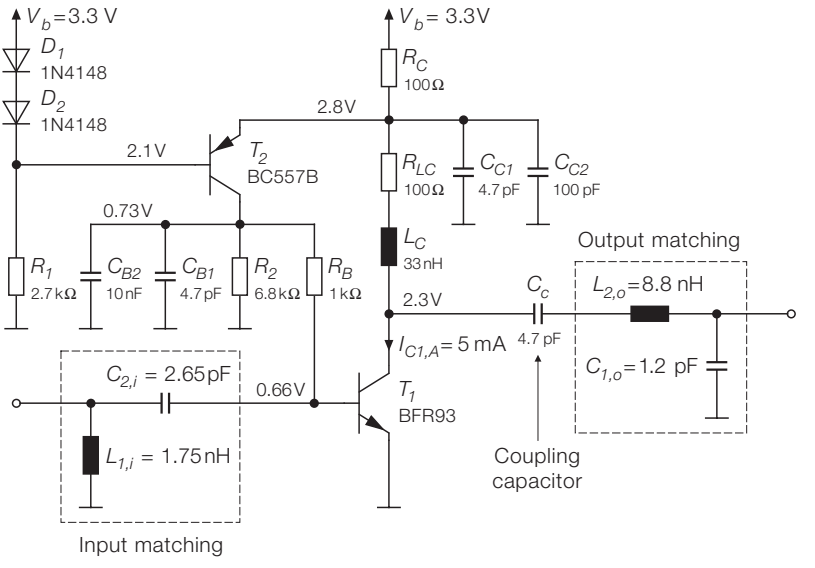


Fig. 27.11. Amplifier with matching networks

at the output since the transformation factor for the real part of the impedance is higher: 7.3 Ω → 50 Ω at the input compared to 33 Ω → 50 Ω at the output. In the centre of Fig. 27.12 the magnitudes of the S parameters are plotted over a wider range. This shows that the output is also nearly matched ($|S_{22}| \approx 0.1$) in the range around 600 MHz. The position of this range depends on the capacitance of the coupling capacitor at the output, which can be used for adjustment. This can be useful when the amplifier is followed by a mixer for conversion to a low intermediate frequency. A suitable choice of the coupling capacitor can also provide a sufficient matching for the intermediate frequency. This indicates that high-frequency circuit engineering often takes advantage of secondary effects. The bottom diagram of Fig. 27.12 shows the gain in decibel. At the operating frequency it reaches its maximum, which we have calculated with (27.12): $MAG \approx 7.5$ dB. The gain is comparatively low as the transistor type BFR93 has a transit frequency of only 5 GHz and is operated in our example at its performance limit. Modern circuits for the frequency range around 2 GHz use transistors with transit frequencies of about 25 GHz, resulting in gains of 20 . . . 25 dB.

27.2.4 Impedance Matching in Multi-stage Amplifiers

Matching in multi-stage amplifiers is done in the same way as in single-stage amplifiers. Each stage is matched at both sides and then arranged in series, where the matching networks between the stages can often be simplified by combining the elements. In most cases, however, this is not the optimum procedure. In practice, it is used only if, for construction purposes, the stages are so far apart that the connections between the stages can no longer be considered as electrically short lines as is especially the case in the GHz range.

In all other cases the output of each stage is matched directly to the input of the next stage. The calculation of this type of impedance matching is complicated since an

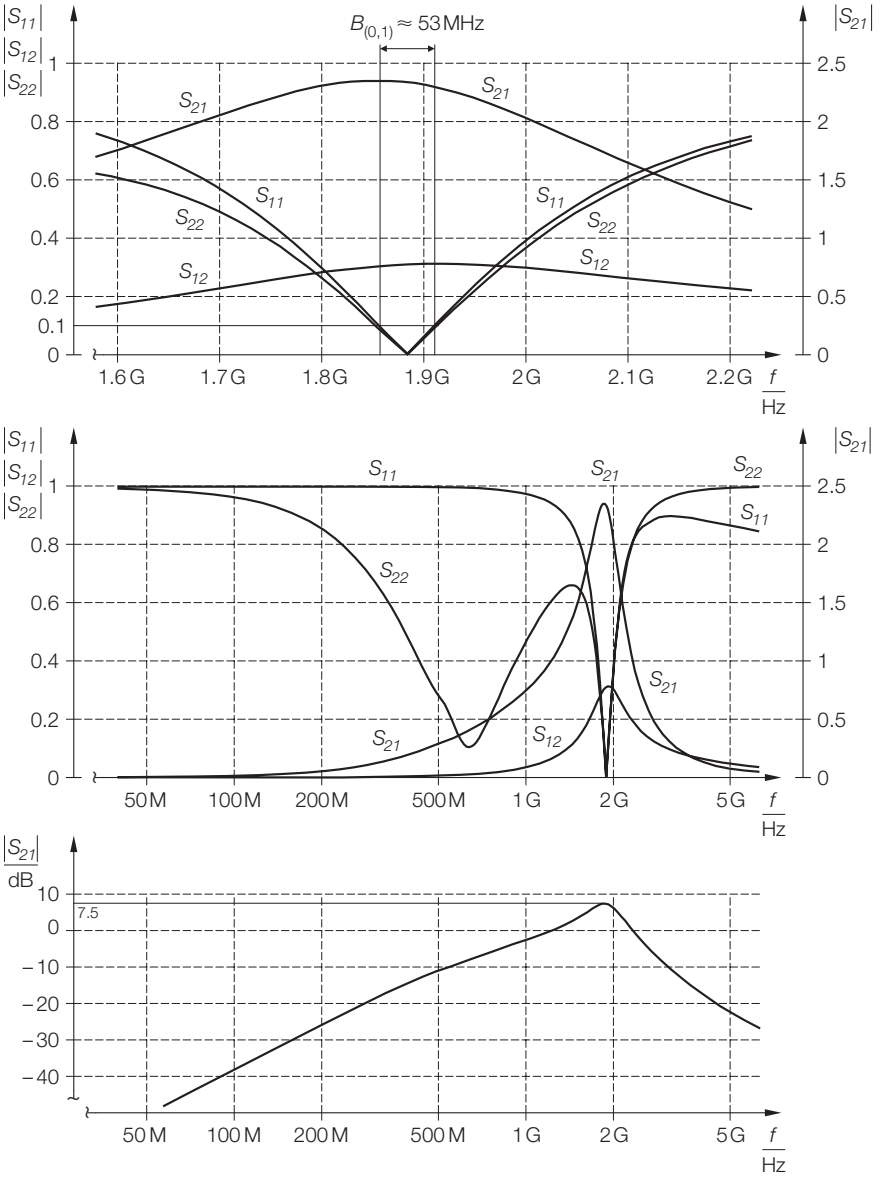


Fig. 27.12. S parameters of the amplifier in Fig. 27.11

amplifier with n stages, including $n + 1$ matching networks (input side, output side and $n - 1$ networks between the stages), are interdependent owing to the reverse transmission of the transistors. The procedure is divided into two steps:

– In the first step, structures must be selected that, in principle, allow impedance matching on the basis of the S parameters of the individual transistors. This must include all wiring that is required for construction, i.e. the PC board layout of the amplifier must be roughly outlined.

– In the second step, the values of the elements in the individual structures must be determined by means of a simulation program. For this purpose, iterative optimisation methods (*optimisers*) are used to find the ideal dimensions with regard to the criteria specified by the user. Often these criteria include maximising $|S_{21}|$ observing the secondary conditions $|S_{11}| < 0.1$ and $|S_{22}| < 0.1$ in the specified frequency range.

If the reverse transmission of the transistors is not very high, the first run may already provide a satisfactory result. Otherwise the structures must be varied before further runs are carried out. These may become necessary solely because the established element values cannot be achieved or arranged on the predetermined layout of the PC board.

In practice, this procedure is also used for single-stage amplifiers. The ideal matching networks can, of course, be calculated directly by following the procedure described in the previous section, but practical operation on the basis of the properties of the real components and the PC board layout require additional computer-aided optimisation.

Impedance Matching with Series Inductance

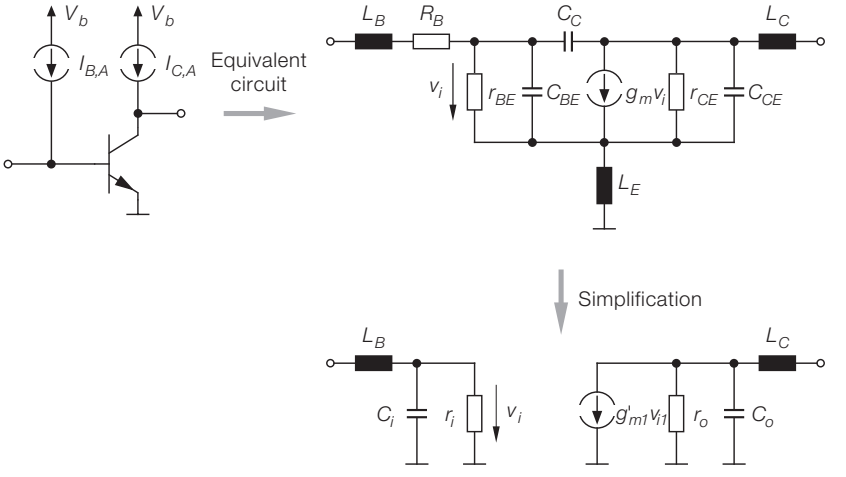
For high-frequency bipolar transistors with a transit frequency above 10 GHz, the capacitances of the actual transistor are so low that the input and output capacitances are formed by the parasitic capacitance of the case. The equivalent circuit for these transistors with case capacitances C_{BE} and C_{CE} and case inductances L_B, L_C and L_E is shown in Fig. 27.13a where the relationships are $C_{BE} > C_{CE} > C_C$ and $L_B \approx L_C > L_E$. The equivalent circuit can be simplified owing to the component dimensions. When using the simplified equivalent circuit for a multi-stage amplifier as shown in Fig. 27.13b, the circuitry between each of the stages represents a Collins filter. The capacitances of the filter are formed by the capacitances of the transistor and the inductances of the filter by the series connection of the case inductances and an external inductance. Therefore, if the dimensions are favourable, matching between the stages can be achieved with a series inductance. Similarly, the parasitic elements of the transistors at the input and output of the amplifier can be integrated into a Collins filter.

27.2.5 Neutralisation

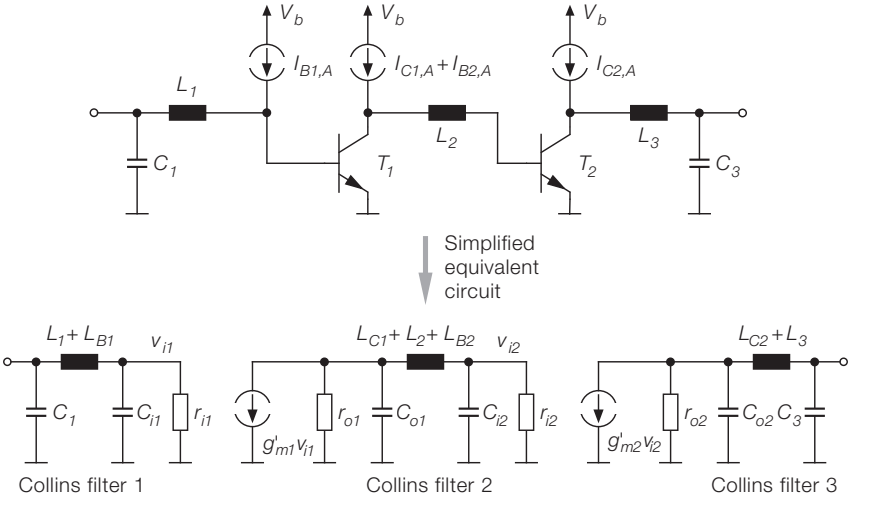
The main obstacle in impedance matching is the reverse transmission of the transistors which reduces the stability factor k and prevents matching on both sides if $k < 1$. For a transistor without reverse transmission $S_{12} = 0$ and $k \to \infty$ holds, so both sides can be matched provided the real parts of the input and output impedances are positive, i.e. $|S_{11}| < 1$ and $|S_{22}| < 1$. A transistor without reverse transmission operates *unilaterally* which means that signal transmission takes place only in the forward direction.

Circuits for Neutralisation

The reverse transmission is caused by the collector-base capacitance C_C in bipolar transistors and by the gate-drain capacitance C_{GD} in FETs. It can be eliminated by connecting a *neutralisation capacitance* C_n of the same value between the base and a point in the circuit that carries the inverted small-signal voltage of the collector. Such a point is created by using an inductor with centre tap for decoupling the collector and connecting this tap



a Simplified equivalent circuit of a bipolar transistor in common-emitter configuration



b Simplified equivalent circuit of a two-stage amplifier with matching circuitry

Fig. 27.13. Impedance matching of a two-stage amplifier with Collins filters utilising the parasitic elements of the transistors

to the supply voltage (see Fig. 27.14). The point opposite the collector then carries the inverted small-signal voltage. Neutralisation is almost ideal up to approximately 300 MHz, but above this frequency the disturbing influence caused by the parasitic effects of the transistor (base spreading resistance and base inductance), the inductor and the capacitor becomes apparent. Amplifiers for higher output power often use two transistors in push-pull arrangement which can then be neutralised by cross-coupling with two capacitances C_{n1} and C_{n2} (see Fig. 27.15). Neutralisation of a differential amplifier according to Fig. 27.16 is based on the same principle.

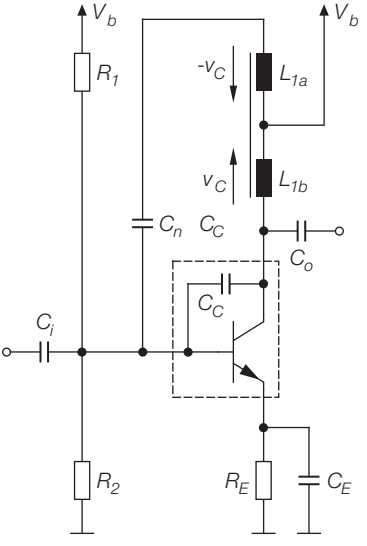


Fig. 27.14. Neutralisation of a transistor

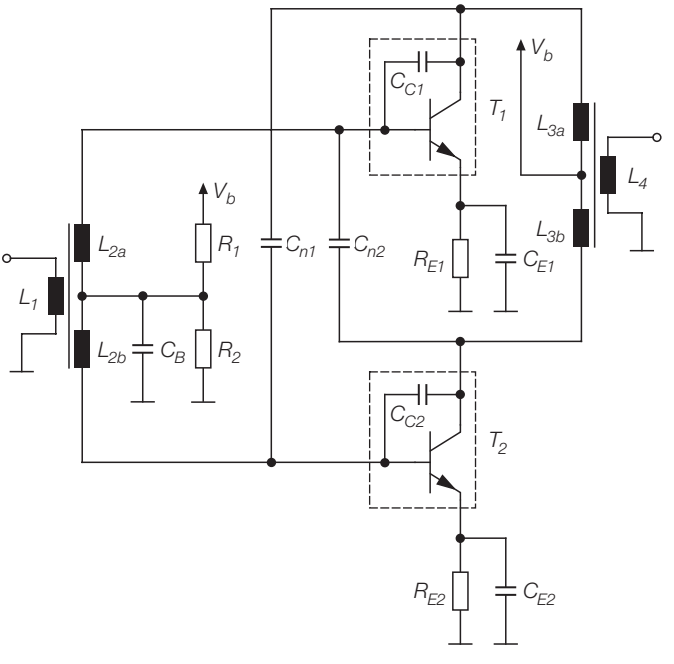


Fig. 27.15. Neutralisation of a push-pull circuit

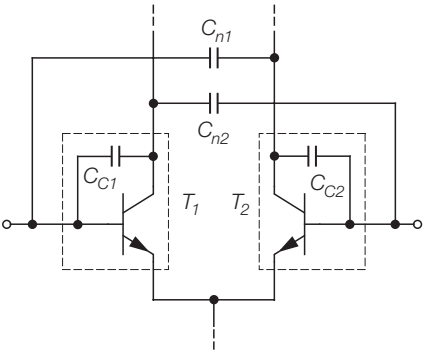


Fig. 27.16. Neutralisation of a differential amplifier

Power Gain in the Case of Neutralisation

Neutralisation and two-sided impedance matching produce the highest possible power gain, known as *unilateral power gain* [27.1]:

$$U = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left\{\frac{S_{21}}{S_{12}}\right\}} \tag{27.13}$$

Here, the S parameters of the transistor *without* neutralisation and the stability factor k from (27.8) on page 1374 are to be inserted. However, the S parameters of the neutralised transistor can also be used, making $S_{12,n} = 0$ and leading to:[6]

$$U = \frac{|S_{21,n}|^2}{\left(1 - |S_{11,n}|^2\right)\left(1 - |S_{22,n}|^2\right)}$$

27.2.6 Special Circuits for Improved Impedance Matching

If the methods described so far fail to provide acceptable matching, circulators or 90° hybrids can be used to improve matching. This is the case, for example, if noise matching is carried out at the input of an amplifier in order to minimise the noise figure and at the same time the lowest possible reflection factor is required.

Impedance Matching with Circulators

A *circulator* is a transmission-asymmetric multi-port element. In practice, 3-port circulators are used exclusively, which are suitable for frequencies in the GHz range and achieve their transmission asymmetry by means of premagnetised ferrites [27.1].

[6] This relationship is obtained by calculating the transducer gain G_T according to (27.30) on page 1398 with matching on both sides and without reverse transmission, thus giving us $S_{12} = 0$, $r_g = S_{11}^*$ and $r_L = S_{22}^*$.

An ideal 3-port circulator is characterised by

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = e^{j\varphi} \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \tag{27.14}$$

where a_1, a_2, a_3 are the incoming and b_1, b_2, b_3 the reflected waves at the three ports. The circulator is fully matched, thus $S_{11,C} = S_{22,C} = S_{33,C} = 0$. The incident waves are transmitted to the next port in the order $1 \rightarrow 2 \rightarrow 3 \rightarrow 1$ and simultaneously undergo a rotation with the angle φ. Transmission asymmetry is seen in the asymmetry of the S matrix where $S_{12,C} \neq S_{21,C}$, $S_{13,C} \neq S_{31,C}$ and $S_{23,C} \neq S_{32,C}$.

Figure 27.17 shows a non-matched amplifier ($S_{11,A} \neq 0$, $S_{22,A} \neq 0$) provided with a circulator at the input and the output. The directional orientation of the circulators is indicated by arrows in the diagrams. Let us first look at the circulator at the input and assume the non-limiting condition $\varphi = 0$ which ensures that the wave a1 coming from the signal source is passed on to the amplifier unaltered:

$$b_2 = S_{21,C}\, a_1 \overset{\varphi=0}{=} a_1$$

Wave $a_2 = S_{11,A}\, b_2$, which is reflected at the amplifier input, is then transferred to the terminating resistance Z_W at port 3:

$$b_3 = S_{32,C}\, a_2 = S_{32,C}\, S_{11,A}\, S_{21,C}\, a_1 \overset{\varphi=0}{=} S_{11,A}\, a_1$$

Here, the wave is absorbed without reflection. This means that no incident wave occurs at port 3 and thus no reflected wave at port 1:

$$a_3 = 0 \quad \Rightarrow \quad b_1 = S_{13,C}\, a_3 = 0$$

This causes the reflection factor at the input to be zero:

$$S_{11} = \frac{b_1}{a_1} \overset{b_1=0}{=} 0$$

The functional principle of this matching method is based on the fact that a wave reflected at the input of the amplifier does not reach the signal source but is absorbed in the terminating resistance. In practice, this requires a circulator with very favourable characteristics and equally good termination at port 3. The circulator at the output of the amplifier operates in the same fashion.

In practice, only one circulator is normally used to improve the reflection factor of the amplifier. In low-noise amplifiers, the circulator is used at the input side to correct any existing input mismatch in the case of noise matching. The next section will describe noise

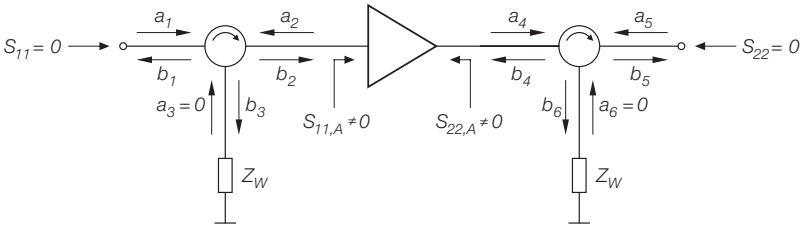


Fig. 27.17. Impedance matching with circulators

matching in more detail. Power amplifiers sometimes use a circulator at the output; the circulator then performs two tasks:

– It reduces the reflection factor S_{22} at the amplifier output to zero.
– It prevents the wave reflected by the load from reaching the output of the amplifier; instead, the wave is absorbed in the terminating resistance Z_W.

The second task is of particular importance as the power amplifier can be destructed by the reflected wave.

Matching with 90° Hybrids

Matching with 90° hybrids requires two hybrids and two amplifiers with identical characteristics as shown by the circuit arrangement in Fig. 27.18. The S parameters of the 90° hybrids is determined with Eq. (28.48) on page 1459.

Let us first look at the relationships at the input. An incident wave a_1 is distributed in terms of its power to the two amplifiers. Wave b_4 at amplifier 2 leads in phase by 90°:

$$b_3 = S_{31,H}\, a_1 = -\frac{a_1}{\sqrt{2}} \quad , \quad b_4 = S_{41,H}\, a_1 = -j\,\frac{a_1}{\sqrt{2}}$$

At the inputs of the amplifiers, the waves are reflected with the input reflection factor $S_{11,A}$:

$$a_3 = S_{11,A}\, b_3 = -S_{11,A}\,\frac{a_1}{\sqrt{2}} \quad , \quad a_4 = S_{11,A}\, b_4 = -j\, S_{11,A}\,\frac{a_1}{\sqrt{2}}$$

This allows the calculation of the waves that occur at ports 1 and 2:

$$b_1 = S_{13,H}\, a_3 + S_{14,H}\, a_4 = -\frac{a_3}{\sqrt{2}} - j\,\frac{a_4}{\sqrt{2}} = 0$$

$$b_2 = S_{23,H}\, a_3 + S_{24,H}\, a_4 = -j\,\frac{a_3}{\sqrt{2}} - \frac{a_4}{\sqrt{2}} = j\, S_{11,A}\, a_1$$

One can see that the waves reflected by the amplifiers are transmitted to the terminating resistance Z_W at port 2 and that the reflection factor at port 1 becomes zero:

$$S_{11} = \frac{b_1}{a_1} \overset{b_1=0}{=} 0$$

Similarly, the value at the output is $S_{22} = 0$.

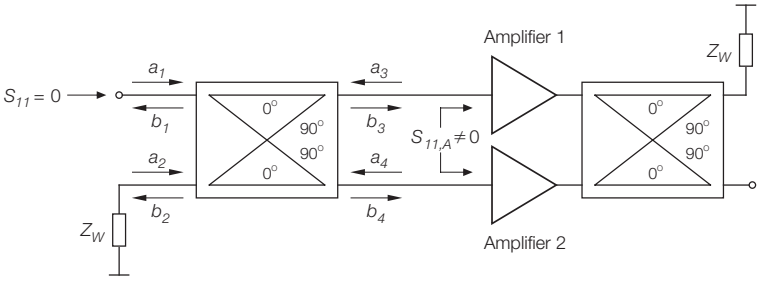


Fig. 27.18. Matching with 90° hybrids

The hybrid at the output acts as a *power combiner* and adds the output powers of the two amplifiers. Therefore, this version of matching is often used in power amplifiers despite its comparatively elaborate circuit construction.

27.2.7 Noise

In relation to the noise figure of integrated high-frequency amplifiers, we explained in Sect. 27.1 that bipolar transistors with (power) matching do not achieve the minimum noise figure since the matching network transforms the source resistance R_g to the input resistance r_{BE} of the transistor, while the optimum source resistance is $r_{BE}/\sqrt{\beta}$. In order to minimise the noise figure, power matching can be replaced by noise matching although this causes unacceptably high input reflection factors in most cases. The same applies to field effect transistors where here, too, power and noise matching differ substantially.

Noise Parameters and Noise Figure

At frequencies in the GHz range, the characteristic noise behaviour of bipolar and field effect transistors can no longer be accurately described by the noise models discussed in Sects. 2.3.4 and 3.3.4. Instead, it is necessary to use the noise parameters specified in the data sheets including the minimum noise figure F_{opt}, the optimum reflection factor $r_{g,opt}$ of the signal source and the normalised noise resistance r_n. Often the noise resistance $R_n = r_n Z_W$ is quoted instead of the normalised noise resistance. The noise parameters allow the noise figure to be calculated for any given reflection factor r_g [27.2]:

$$F = F_{opt} + 4\,r_n \frac{\left|r_g - r_{g,opt}\right|^2}{\left(1 - |r_g|^2\right)\left|1 + r_{g,opt}\right|^2} \tag{27.15}$$

For $r_g = r_{g,opt}$ the following is true: $F = F_{opt}$.

Design of a Low-Noise Amplifier

When designing an amplifier, the noise figure is calculated for all reflection factors with $|r_g| < 1$ and presented in the r plane, thus resulting in circles of constant noise figures. The diagram also represents the related power gain where, for the reflection factor $r_{g,m}$ with power matching, the maximum available power gain (*MAG*) is achieved if matching on both sides is possible. The power gain for other values of r_g corresponds to the transducer gain G_T and is calculated as follows:

$$r_g \overset{(27.5)}{\Longrightarrow} r_2 = S_{22} + \frac{S_{12}S_{21}r_g}{1 - S_{11}r_g} \overset{\text{Matching}}{\Longrightarrow} r_L = r_2^*$$

$$\overset{(27.30)}{\Longrightarrow} G_T = \frac{|S_{21}|^2\left(1 - |r_g|^2\right)\left(1 - |r_L|^2\right)}{\left|\left(1 - S_{11}r_g\right)\left(1 - S_{22}r_L\right) - S_{12}S_{21}r_g r_L\right|^2}$$

This results in circles with constant power gain. Normally the calculation is performed with the aid of suitable simulation or mathematical programs.

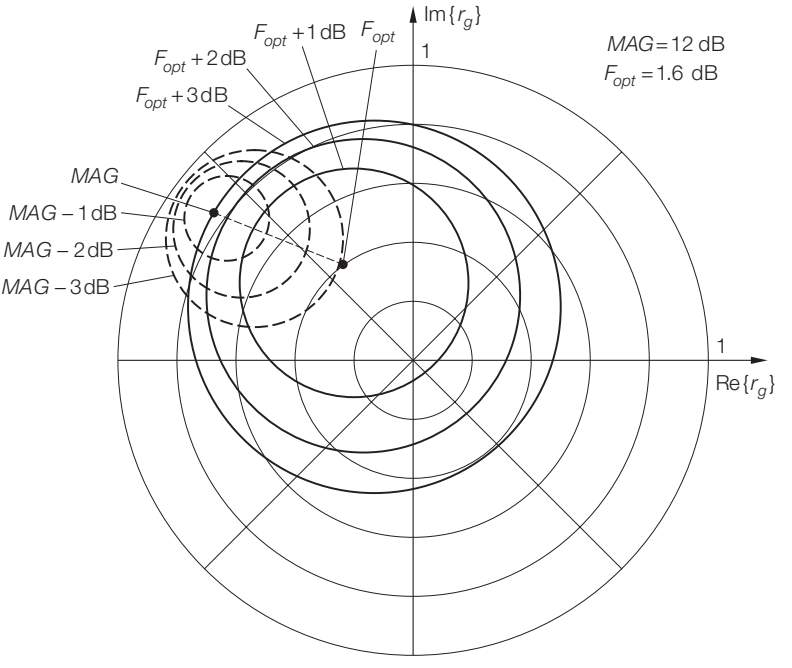


Fig. 27.19. Noise figure and power gain of a GaAs MESFET CFY10 at $f = 9\,\text{GHz}$ ($I_{D,A} = 15\,\text{mA}$, $V_{DS,A} = 4\,\text{V}$)

Figure 27.19 shows the noise figure and the power gain of a GaAs MESFET CFY10 at $f = 9\,\text{GHz}$. Power matching is achieved for $r_g = r_{g,m} = -0.68 + j\,0.5$ and noise matching is achieved for $r_g = r_{g,opt} = -0.24 + j\,0.33$. The circles of constant noise figures show that with power matching the noise figure is 3 dB higher than with noise matching. Likewise one can see from the circles of constant power gain that with noise matching the power gain is 3.1 dB lower than *MAG*. Now it is possible to draw a connecting line between $r_{g,m}$ and $r_{g,opt}$ and to select a reflection factor r_g for which the user-specific requirements are met.

Where matching at both sides is not possible, one can often carry out noise matching at the input and power matching at the output. For this purpose, the circles of constant noise figures are first drawn in the r plane. Then the power gain is calculated for all r_g values for which stable operation is possible. The procedure is as follows:

– Starting with a given reflection factor r_g, the reflection factor at the output is calculated:

$$r_2 \overset{(27.5)}{=} S_{22} + \frac{S_{12}S_{21}r_g}{1 - S_{11}r_g}$$

If $|r_2| \geq 1$, stable operation with power matching at the output is not possible.
– If $|r_2| < 1$, power matching at the output is assumed: $r_L = r_2^*$.
– The corresponding reflection factor at the input is calculated:

$$r_1 \overset{(27.4)}{=} S_{11} + \frac{S_{12}S_{21}r_L}{1 - S_{22}r_L} = S_{11} + \frac{S_{12}S_{21}r_2^*}{1 - S_{22}r_2^*}$$

If $|r_1| \geq 1$, stable operation with power matching at the output is not possible.

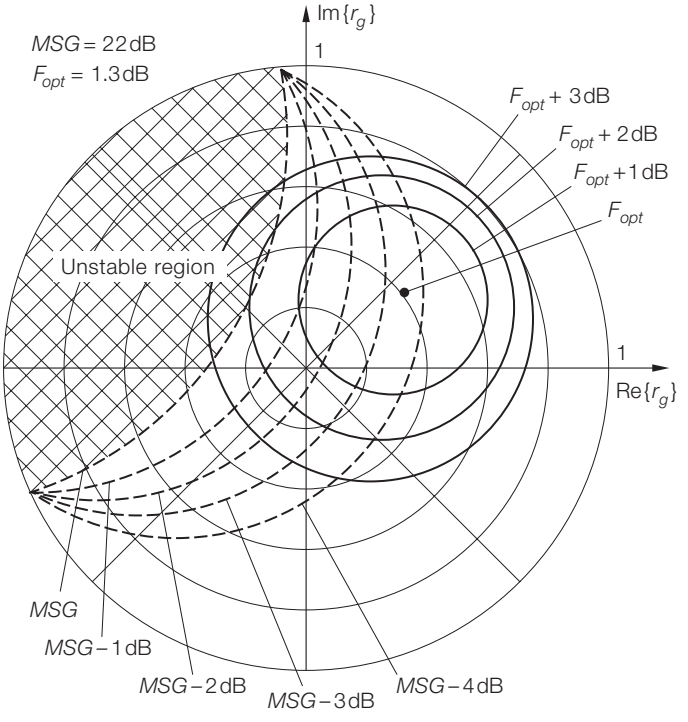


Fig. 27.20. Noise figure and power gain of a bipolar transistor BFP405 at $f = 2,4\,\text{GHz}$ ($I_{C,A} = 5\,\text{mA}$, $V_{CE,A} = 4\,\text{V}$)

– If $|r_1| < 1$, the related transducer gain G_T is calculated:

$$G_T = \frac{|S_{21}|^2 \left(1 - |r_g|^2\right)\left(1 - |r_L|^2\right)}{\left|\left(1 - S_{11} r_g\right)\left(1 - S_{22} r_L\right) - S_{12} S_{21} r_g r_L\right|^2}$$

This results in circles of constant power gain that are limited by a stability border which is also circular. The stability border is the point at which the *maximum stable power gain MSG* is obtained; this will be described in more detail in Sect. 27.4.

Figure 27.20 shows the noise figure and the power gain of a bipolar transistor BFP405 at $f = 2.4\,\text{GHz}$. The stability factor is below one so that power matching at both sides is not possible. Noise matching is obtained for $r_g = r_{g,opt} = 0.32 + j\,0.25$. The circles of constant power gain are limited by a stability border at which the maximum stable power gain *MSG* is reached. The circles of constant power gain show that, with noise matching, the power gain is 3.5 dB below *MSG*. Likewise the circles of constant noise figure indicate that for operation with the power gain *MSG*, the noise figure is 1.8 dB above the minimum noise figure. A suitable reflection factor r_g can now be selected.

If the optimum reflection factor $r_{g,opt}$ with power matching at the output side is located inside the instable region, one must do without power matching and shift the stability border by a suitable choice of $r_L \neq r_2^*$ until $r_{g,opt}$ is within the stable region.

In practice, optimising the parameters r_g and r_L in terms of noise, power gain and other criteria is done by means of simulation or mathematical programs with which non-linear optimisation processes can be carried out.

27.3 Broadband Amplifiers

Amplifiers with a constant gain over an extended frequency range are known as *broadband amplifiers*. High-frequency amplifiers are called broadband amplifiers if their bandwidth B is wider than the centre frequency f_C thus producing a lower cut-off frequency $f_L = f_C - B/2 < f_C/2$ and an upper cut-off frequency $f_U = f_C + B/2 > 3f_C/2$ as well as a ratio $f_U/f_L > 3$. Sometimes $f_U/f_L > 2$ is used as a criterion. The term *broadband* is given to these amplifiers only because their bandwidth is clearly higher than the bandwidth of reactively matched amplifiers that are typical of high-frequency applications and in most cases have a ratio of $f_U/f_L < 1.1$. Furthermore, the wideband characteristic of high-frequency amplifiers is also related to impedance matching. Therefore, it is not the -3dB bandwidth that is used as the bandwidth, but the bandwidth within which the magnitude of the input and output reflection factors remain below a given limit. While reactively matched amplifiers usually require reflection factors of $|r| < 0.1$, broadband amplifiers accept reflection factors of $|r| < 0.2$. The less stringent demand reflects the fact that wideband matching in the MHz or GHz range is much more complicated than the narrow-band reactive matching.

27.3.1 Principle of a Broadband Amplifier

The functional principle of a broadband amplifier is based on the fact that a voltage-controlled current source with resistive feedback can be matched at both sides to the characteristic impedance Z_W. To implement the voltage-controlled current source, one of the generalised discrete transistors from Fig. 27.4 on page 1368 is used.[7] Figure 27.21 shows the principle of a broadband amplifier.

Let us first calculate the gain using the small-signal equivalent circuit shown in Fig. 27.22a. The nodal equation at the output is:

$$\frac{v_i - v_o}{R} = g_m v_i + \frac{v_o}{R_L}$$

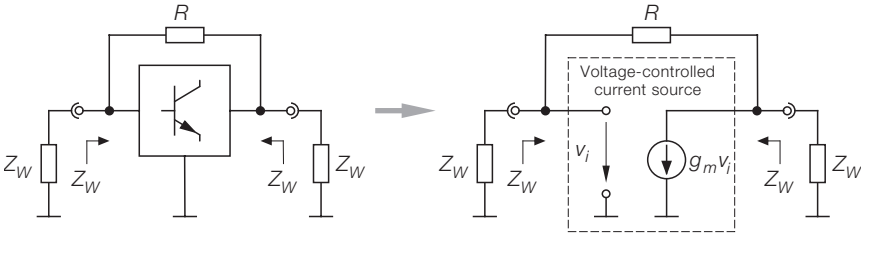
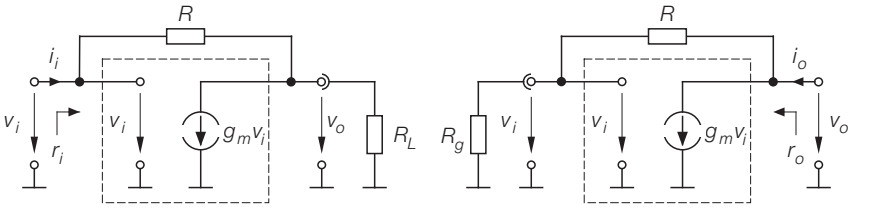


Fig. 27.21. Principle of a broadband amplifier

[7] The version in the right portion of Fig. 27.4b cannot be used as it has no high-resistance output.



a Gain and input resistance **b** Output resistance

Fig. 27.22. Equivalent circuits for calculating the gain as well as the input and output resistances of a broadband amplifier

This leads to the gain:

$$A = \frac{v_o}{v_i} = \frac{R_L\,(1 - g_m R)}{R + R_L} \tag{27.16}$$

The input current is

$$i_i = \frac{v_i - v_o}{R} = \frac{v_i(1 - A)}{R}$$

which leads to the input resistance:

$$r_i = \frac{v_i}{i_i} = \frac{R + R_L}{1 + g_m R_L} \tag{27.17}$$

According to Fig. 27.22b, the output current is:

$$i_o = \frac{v_o}{R + R_g} + g_m v_i = \frac{v_o}{R + R_g} + g_m \frac{R_g v_o}{R + R_g}$$

This leads to the output resistance:

$$r_o = \frac{v_o}{i_o} = \frac{R + R_g}{1 + g_m R_g} \tag{27.18}$$

We set $R_L = R_g = Z_W$ and calculate the reflection factors at the input and output:

$$S_{11} = \left.\frac{r_i - Z_W}{r_i - Z_W}\right|_{R_L = Z_W} = \frac{R - g_m Z_W^2}{R + 2Z_W + g_m Z_W^2} \tag{27.19}$$

$$S_{22} = \left.\frac{r_o - Z_W}{r_o - Z_W}\right|_{R_g = Z_W} = \frac{R - g_m Z_W^2}{R + 2Z_W + g_m Z_W^2} = S_{11} \tag{27.20}$$

The reflection factors S_{11} and S_{22} are identical and become zero for:

$$\boxed{R = g_m Z_W^2} \tag{27.21}$$

This means that both sides are matched. The forward transmission factor is:

$$S_{21} = \left. A \right|_{R_L = Z_W\,,\; R = g_m Z_W^2} = -\frac{R}{Z_W} + 1 = -g_m Z_W + 1 \tag{27.22}$$

This is identical to the gain in a circuit which is matched at both ends. It can be influenced only by means of the transconductance g_m as the feedback resistance is linked to the transconductance. A high transconductance results in a high gain.

27.3.2 Design of a Broadband Amplifier

Figure 27.23 shows the practical design of a broadband amplifier on the basis of an integrated Darlington transistor with resistances for the operating point adjustment. Resistances R_3 und R_4 have values in the kΩ range and are therefore negligible. This is especially the case for the internal feedback resistance R_3 which is higher by at least a factor of 10 than the resistance R required for impedance matching. The effective feedback resistance is thus:

$$R_{eff} = R \,||\, R_3 \overset{R \ll R_3}{\approx} R$$

Resistance R_C serves to adjust the bias current. In terms of the small-signal parameters, it is parallel to the amplifier output and acts like an additional load resistance. This means that the amplifier no longer exactly fulfils the symmetry condition $S_{11} = S_{22}$ of an ideal broadband amplifier, in other words, the matching condition $S_{11} = S_{22} = 0$ can only be approximately satisfied. R_C must therefore be made as high as possible. In the region of the upper cut-off frequency, the gain and matching can be improved by the inductances L_R and L_C. The inductance L_R also contains the parasitic inductances of the resistance R and the coupling capacitance C_c. Therefore, C_c can be a capacitor with a relatively high capacitance and inductance, i.e. with a low resonant frequency, without producing any negative effect. Capacitances C_i and C_o serve as coupling capacitances at the input and the output. These are critical as most capacitors only achieve an impedance of $|X| \ll Z_W = 50\,\Omega$ in a relatively narrow range around the resonant frequency (see Fig. 28.5 on page 1406). Thus, the matching bandwidth is usually limited by the coupling capacitors.

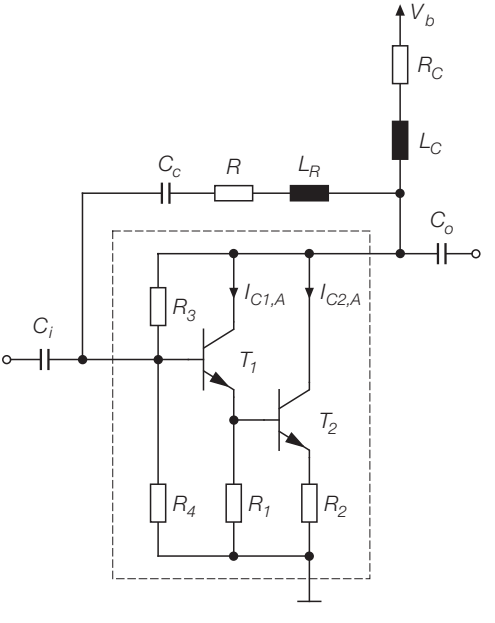


Fig. 27.23. Practical design of a broadband amplifier

With the help of (27.22) we can use the desired gain to derive the necessary transconductance g_m of the voltage-controlled current source which corresponds approximately to the transconductance of transistor T_2 when taking the current feedback via R_2 into account:

$$g_m \approx \frac{g_{m2}}{1 + g_{m2} R_2} \qquad \text{with } g_{m2} = \frac{I_{C2,A}}{V_T}$$

The selection of the bias current $I_{C2,A}$ determines the maximum output power of the amplifier. In practice, a control signal with an effective value (rms) of up to $I_{eff} \approx I_{C2,A}/2$ is useful; the distortion factor then remains below 10%. Consequently, the output power and the quiescent current are:

$$P_{o,max} = I_{eff}^2 Z_W \approx \frac{I_{C2,A}^2 Z_W}{4} \quad \Rightarrow \quad I_{C2,A} > \sqrt{\frac{4\, P_{o,max}}{Z_W}} \tag{27.23}$$

However, the bias current must be high enough to achieve the necessary transconductance: $I_{C2,A} \geq g_m V_T$. In this case, the resistance of the current feedback is:

$$R_2 \overset{I_{C,A} > g_m V_T}{=} \frac{1}{g_m} - \frac{V_T}{I_{C2,A}} \tag{27.24}$$

The parasitic inductance of resistor R_2 must be as low as possible in order to avoid undesirable reactive feedback and is of particular importance with values below 20 Ω. If the expected bandwidth is not achieved in a broadband amplifier with current feedback, the reason is often because the parasitic inductance in the emitter circuit of T_2 is too high.

The current feedback via R_2 also influences the bandwidth by causing it to increase with increasing feedback. This is the reason why amplifiers with a particularly wide bandwidth make use of current feedback even if this is not required on the basis of the output power; typical examples are broadband amplifiers for instrumentation.

Example: In the following, a broadband amplifier is designed according to Fig. 27.23 for a 50 Ω system by using two transistors of the type BFR93 in Darlington configuration (see Fig. 27.24). A gain of $A = 16\,\text{dB}$ and a maximum output power of $P_{o,max} = 0.3\,\text{mW} = -5\,\text{dBm}$ are required. For the supply voltage we assume $V_b = 5\,\text{V}$. The gain is:

$$|A| = |S_{21}| = 10^{\frac{A\,[\text{dB}]}{20\,\text{dB}}} = 10^{\frac{16\,\text{dB}}{20\,\text{dB}}} = 6.3$$

With (27.22) we obtain the necessary transconductance:

$$S_{21} = -g_m Z_W + 1 \overset{!}{=} 6.3 \overset{Z_W = 50\,\Omega}{\Longrightarrow} g_m = \frac{7.3}{50\,\Omega} = 146\,\text{mS}$$

For the quiescent current of T_2 it follows that $I_{C2,A} > g_m V_T = 3.8\,\text{mA}$. With (27.23) we obtain from the maximum output power $I_{C2,A} > 4.9\,\text{mA}$. We select $I_{C2,A} = 5\,\text{mA}$. The resistor R_2 is calculated with (27.24) to be $R_2 = 1.6\,\Omega$. The resulting small current feedback is not implemented for the moment as we must expect a loss in gain owing to secondary effects.

For the bias current of transistor T_1 we select $I_{C1,A} = 2\,\text{mA}$ since, with smaller currents, the transit frequency drops rapidly. As the base-emitter voltage of T_2 is approximately 0.66 V and the base current $I_{B2,A} \approx 50\,\mu\text{A}$ (current gain approximately 100) is negligible compared to $I_{C1,A} = 2\,\text{mA}$, the value for the resistor R_1 is obtained:

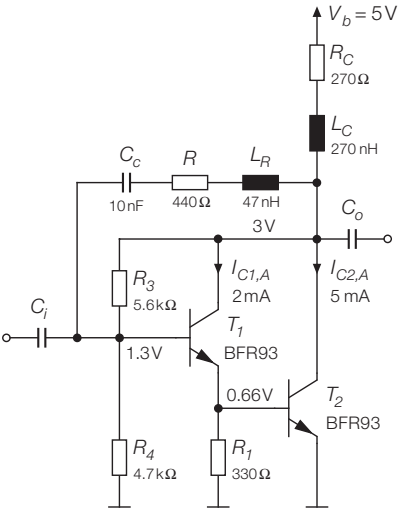


Fig. 27.24. Example of a broadband amplifier

$R_1 \approx 0,66\,V/2\,mA = 330\,\Omega$. Concerning the voltage divider for operating point adjustment we select $R_3 = 5.6\,k\Omega$ and $R_4 = 4.7\,k\Omega$ resulting in a voltage of 3 V at the collectors of the transistors (see Fig. 27.24). To ensure that the desired bias current for T_2 is achieved ($I_{C2,A} = 5\,mA$), a collector resistor $R_C = 270\,\Omega$ must be used for the supply voltage $V_b = 5\,V$.

After all resistors for operating point setting have been dimensioned, we can calculate the transconductance g_m. For this purpose we use the equation for the transconductance of a Darlington transistor with resistance R from Sect. 2.4.4 and insert $R = R_1$:

$$g_m \approx g_{m1} \frac{1 + g_{m2}\,(r_{BE2} \,||\, R_1)}{1 + g_{m1}\,(r_{BE2} \,||\, R_1)}$$

For $g_{m1} = I_{C1,A}/V_T = 77\,mS$, $g_{m2} = I_{C2,A}/V_T = 192\,mS$ and $R_1 = 330\,\Omega$, the transconductance is $g_m \approx 185\,mS$. From (27.21) the feedback resistance is thus $R = g_m Z_W^2 = 463\,\Omega$.

Further dimensioning is done with the aid of circuit simulation. We have used the high-frequency equivalent circuits for all resistances and inductances as well as the capacitor C_c, only for the coupling capacitances C_i and C_o have we assumed ideal capacitances. First, the reflection factors S_{11} and S_{22} are optimised at low frequencies by finely tuning the resistance R; the result is $R \approx 440\,\Omega$. Then, the gain and the impedance matching at high frequencies is optimised by adding inductors L_R and L_C. For $L_R = 47\,nH$ and $L_C = 270\,nH$, the plots of the magnitude of the S parameters are obtained as shown in Fig. 27.25. The typical demand on broadband amplifiers of $|S_{22}| < 0.2$ is complied with up to about 1 GHz. In this range $|S_{11}| < 0.1$, i.e. the input matching is extremely good for a broadband amplifier. The desired gain $|S_{21}| = 6.3 = 16\,dB$ is reached up to approximately 300 MHz. The $-3dB$ cut-off frequency is at 700 MHz.

The current feedback calculated for transistor T_2 with $R_2 \approx 1.6\,\Omega$ can be neglected because the amplifier achieves the desired gain. Deviations from the calculated values have two sources. First, the transconductance $g_m = 185\,mS$ of the Darlington transistor is lower than the transconductance $g_{m2} = 192\,mS$ of transistor T_2, and second, the transistor BFR93 has a parasitic emitter resistance of approximately $1\,\Omega$.

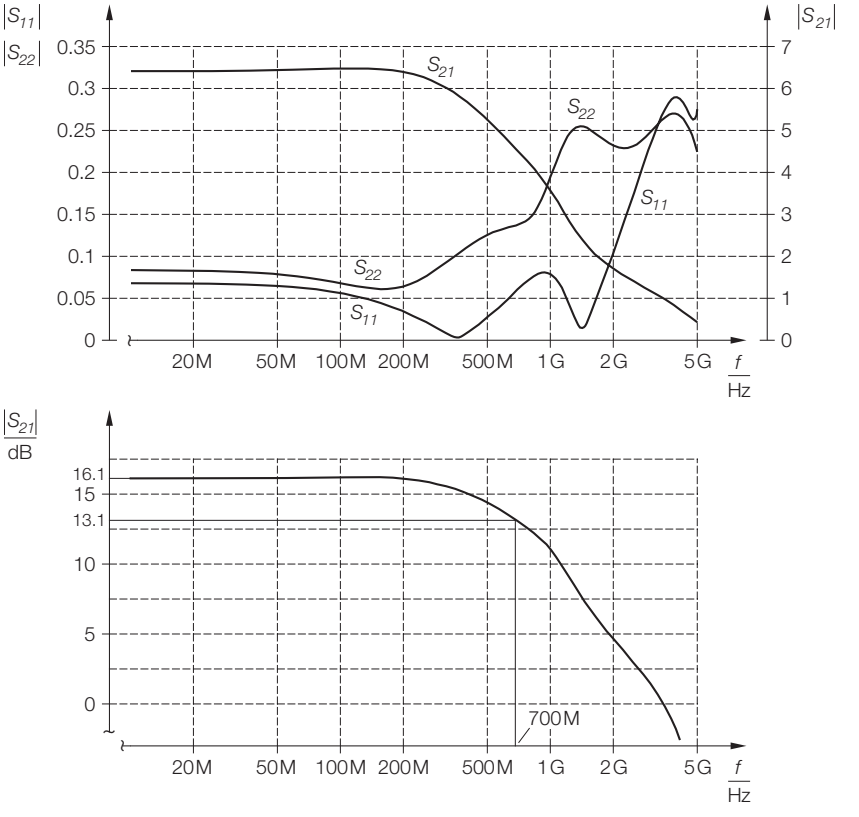


Fig. 27.25. S parameters of the broadband amplifier from Fig. 27.24

In practice, the very good overall performance of this amplifier can only be used in a comparatively small frequency band as the coupling capacitances C_i and C_o cannot be given a wide-band low-resistance characteristic. If necessary, several capacitors with staggered resonant frequencies must be used.

27.4 Power Gain

Usually the *power gain* is specified for high-frequency amplifiers. There are different definitions of *gain* which relate to different parameters. Some of the related equations on the basis of S or Y parameters are very complicated. We shall begin by explaining the definitions of gain for an ideal amplifier and then extend these to cover a more general situation. The complex equations on the basis of S and Y parameters are intended for computer-aided evaluations only as *manual* calculation is very involved.

Figure 27.26 shows the ideal amplifier with the open-circuit gain factor A, the input resistance r_i and the output resistance r_o; there is no reverse transmission. The amplifier is operated with a signal source of the internal resistance Rg and a load R_L. For further calculations we require the *overall gain*

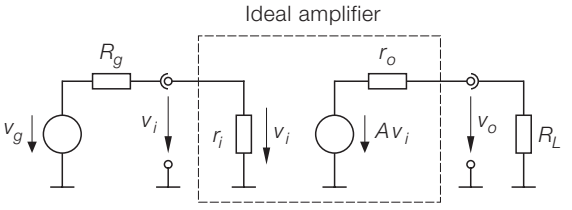


Fig. 27.26. Ideal amplifier with signal source and load

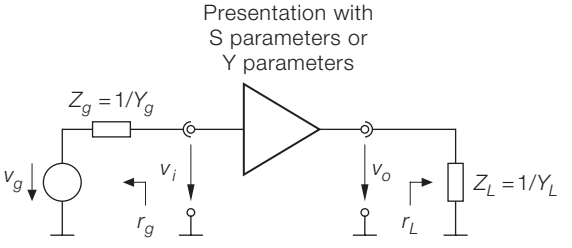


Fig. 27.27. General amplifier with signal source and load

$$A_B = \frac{v_o}{v_g} = \frac{r_i}{R_g + r_i} A \frac{R_L}{r_o + R_L}$$

and the *gain under load*:

$$A_L = \frac{v_o}{v_i} = A \frac{R_L}{r_o + R_L}$$

For the general situation, we look at an amplifier that is characterised by S and Y parameters. It is operated with a source of the impedance $Z_g = 1/Y_g$ and a load $Z_L = 1/Y_L$ (see Fig. 27.27). For presentation with the help of the S parameters we also need the reflection factors of the source and the load

$$r_g = \frac{Z_g - Z_W}{Z_g + Z_W} \quad , \quad r_L = \frac{Z_L - Z_W}{Z_L + Z_W}$$

and the determinant of the S matrix:

$$\Delta_S = S_{11} S_{22} - S_{12} S_{21}$$

It should be noted that the parameters r_g and r_L are reflection factors while r_i and r_o are the resistances of the ideal amplifier from Fig. 27.26.

27.4.1 Direct Power Gain

Direct power gain refers to the power gain in the conventional sense:

$$G = \frac{P_L}{P_i} = \frac{\text{Effective power absorbed by the load}}{\text{Effective power absorbed at the amplifier input}}$$

For the ideal amplifier from Fig. 27.26 it follows that [8]:

$$P_L = \frac{v_o^2}{R_L} \quad , \quad P_i = \frac{v_i^2}{r_i}$$

[8] We use effective values so that $P = u^2/R$.

This leads to:

$$G = \left(\frac{v_o}{v_i}\right)^2 \frac{r_i}{R_L} = A_L^2 \frac{r_i}{R_L} = \frac{A^2 r_i R_L}{(r_o + R_L)^2} \tag{27.25}$$

The corresponding calculation for the amplifier in Fig. 27.27 leads to:

$$\begin{aligned} G &= \frac{|S_{21}|^2 \left(1 - |r_L|^2\right)}{1 - |S_{11}|^2 + |r_L|^2 \left(|S_{22}|^2 - |\Delta_S|^2\right) - 2\,\mathrm{Re}\left\{r_L \left(S_{22} - \Delta_S S_{11}^*\right)\right\}} \\ &= \frac{|Y_{21}|^2\,\mathrm{Re}\{Y_L\}}{\mathrm{Re}\left\{Y_{11} - \dfrac{Y_{12}Y_{21}}{Y_{22}Y_L}\right\} |Y_{22} + Y_L|^2} \end{aligned} \tag{27.26}$$

The direct power gain is independent of the signal source impedance and therefore contains no indication regarding the impedance matching on the input side. Comparison of, say, two amplifiers that use the same signal source, the same load, and output the same effective power to the load reveals that the amplifier with the lower effective input power has a higher direct power gain. In relation to high-frequency amplifiers, this property is not useful; therefore, the direct power gain is rarely used in high-frequency engineering.

27.4.2 Insertion Gain

Insertion gain is the ratio of the effective powers absorbed by the load with or without amplification:

$$G_I = \frac{P_L}{P_{L,wa}} = \frac{\text{Effective power absorbed by the load with amplifier}}{\text{Effective power absorbed by the load without amplifier}}$$

Consequently, $P_{L,wa}$ is the effective power which the signal source can deliver directly to the load. For the ideal amplifier from Fig. 27.26, the following is true:

$$P_L = \frac{v_o^2}{R_L} \quad , \quad P_{L,wa} = \frac{v_g^2 R_L}{\left(R_g + R_L\right)^2}$$

Consequently:

$$G_I = \left(\frac{v_o}{v_g}\right)^2 \left(\frac{R_g + R_L}{R_L}\right)^2 = A_B^2 \left(\frac{R_g + R_L}{R_L}\right)^2$$
$$= \left(\frac{r_i}{R_g + r_i}\right)^2 A^2 \left(\frac{R_g + R_L}{r_o + R_L}\right)^2 \tag{27.27}$$

The corresponding calculation for the amplifier in Fig. 27.27 leads to:

$$G_I = \frac{|S_{21}|^2 \left|1 - r_g r_L\right|^2}{\left|\left(1 - S_{11} r_g\right)\left(1 - S_{22} r_L\right) - S_{12} S_{21} r_g r_L\right|^2}$$
$$= \frac{|Y_{21}|^2 \operatorname{Re}\left\{Y_g\right\} \operatorname{Re}\left\{Y_L\right\} \left|Y_g + Y_L\right|^2}{\left|\left(Y_{11} + Y_g\right)\left(Y_{22} + Y_L\right) - Y_{12} Y_{21}\right|^2 \left|Y_g Y_L\right|} \tag{27.28}$$

The insertion gain depends on the impedance of the signal source and the load and therefore takes the input and output impedance matching into account. However, the maximum gain is generally not reached with matching at both sides. This can be exemplified with the ideal amplifier. With two-sided matching, $R_g = r_i$ and $R_L = r_o$ where insertion into (27.27) leads to:

$$G_{I,match} = \left(\frac{1}{2}\right)^2 A^2 \left(\frac{R_g + R_L}{2R_L}\right)^2$$

This shows that, despite impedance matching at both sides, the insertion gain depends on the ratio R_g/R_L. A constant insertion gain is achieved only in the special case of equal resistances at the input and output, i.e. $R_g = r_i = r_o = R_L$. Owing to this characteristic, the insertion gain is hardly used.

27.4.3 Transducer Gain

Transducer gain specifies the ratio of the effective power absorbed by the load to the available (effective) power at the signal source:[9]

$$G_T = \frac{P_L}{P_{A,g}} = \frac{\text{Effective power absorbed by the load}}{\text{Available power at the signal source}}$$

For the ideal amplifier from Fig. 27.26 the following is true:

$$P_L = \frac{v_o^2}{R_L} \quad , \quad P_{A,g} = \frac{v_g^2}{4R_g}$$

This leads to:

$$G_T = \left(\frac{v_o}{v_g}\right)^2 \frac{4R_g}{R_L} = A_B^2 \frac{4R_g}{R_L} = \left(\frac{r_i}{R_g + r_i}\right)^2 A^2 \frac{4R_g R_L}{(r_o + R_L)^2} \tag{27.29}$$

[9] The available power is an effective power by definition and thus does not have to be explicitly specified as being effective.

The corresponding calculation for the amplifier in Fig. 27.27 leads to:

$$G_T = \frac{|S_{21}|^2 \left(1-|r_g|^2\right)\left(1-|r_L|^2\right)}{\left|\left(1-S_{11}r_g\right)\left(1-S_{22}r_L\right)-S_{12}S_{21}r_g r_L\right|^2}$$

$$= \frac{4\,|Y_{21}|^2\,\mathrm{Re}\left\{Y_g\right\}\,\mathrm{Re}\left\{Y_L\right\}}{\left|\left(Y_{11}+Y_g\right)\left(Y_{22}+Y_L\right)-Y_{12}Y_{21}\right|^2} \tag{27.30}$$

The transducer gain depends on the impedance of the signal source and the load and becomes maximum with impedance matching at both sides. This can be demonstrated with (27.29):

$$\frac{\partial G_T}{\partial R_g} = 0 \quad , \quad \frac{\partial G_T}{\partial R_L} = 0 \qquad \Longrightarrow \qquad R_g = r_i \quad , \quad R_L = r_o$$

Thus, the transducer gain meets the reasonable demands expected of a gain definition.

27.4.4 Available Power Gain

Available power gain specifies the ratio of the available powers of the amplifier to the signal source:

$$G_A = \frac{P_{A,A}}{P_{A,g}} = \frac{\text{Available power of the amplifier}}{\text{Available power of the signal source}}$$

For the ideal amplifier from Fig. 27.26 the following is true:

$$P_{A,A} = \frac{(Av_i)^2}{4r_o} \quad , \quad P_{A,g} = \frac{v_g^2}{4R_g}$$

This leads to:

$$G_A = \left(\frac{Av_i}{v_g}\right)^2 \frac{R_g}{r_o} = \left(\frac{r_i}{R_g+r_i}\right)^2 A^2\,\frac{R_g}{r_o} \tag{27.31}$$

The corresponding calculation for the amplifier in Fig. 27.27 leads to:

$$G_A = \frac{|S_{21}|^2\left(1-|r_g|^2\right)}{1-|S_{22}|^2+|r_g|^2\left(|S_{11}|^2-|\Delta_S|^2\right)-2\mathrm{Re}\left\{r_g\left(S_{11}-\Delta_S S_{22}^*\right)\right\}}$$

$$= \frac{|Y_{21}|^2\,\mathrm{Re}\left\{Y_g\right\}}{\mathrm{Re}\left\{\left(\left(Y_{11}+Y_g\right)Y_{22}-Y_{12}Y_{21}\right)\left(Y_{11}+Y_g\right)\right\}} \tag{27.32}$$

The available power gain is independent of the load and includes no indication with regard to impedance matching at the output side. It is required for noise calculations since these are based on the available power. The available power gain has already been described in Sect. 4.2.4 in connection with the calculation of the noise figure of amplifiers connected in series (see Eqs. (4.200) and (4.201) on page 460).

27.4.5 Comparison of Gain Definitions

Specific properties of the various gain definitions have already been described in the relevant sections; for this reason, we shall restrict ourselves to a brief comparison here.

Direct power gain G is of no relevance in high-frequency amplifiers since the optimum use of the available power of the signal source is required and because impedance matching at the input side necessary for this purpose has no bearing on the direct power gain. In fact, it reaches its maximum if the amplifier absorbs as little power from the signal source as possible, i.e. with the poorest possible impedance matching. The direct power gain is relevant for low-frequency amplifiers since, in these cases, the aim is to achieve the highest possible voltage gain, which means a minimum load on the signal source. In high-frequency amplifiers such mismatches are undesirable because of the resulting reflections.

The insertion gain G_I is of no real significance for matched amplifiers. This will be explained for the ideal amplifier in Fig. 27.26. With matching at both sides and different resistances at input and output a mismatch occurs in the direct connection of signal source and load that, in practice, would be corrected by a matching network. For this reason, the two operating modes which are compared in the definition of the insertion gain are not *practical* but *theoretical* alternatives only. With impedance matching at both sides and equal resistances at the input and output, the matched condition ($R_g = R_L$) exists even with a direct connection between signal source and load, but in this case the available power of the signal source is delivered to the load and the insertion gain G_I corresponds to the transducer gain G_T.

Due to its properties, the transducer gain G_T is the preferred definition of gain in high-frequency engineering and is simply referred to as gain. However, it is not to be confused with *voltage gain* or *power gain*. Only in the case of impedance matching at both sides and the same resistances at the input and output are the voltage gain, current gain and transducer gain identical in their *decibel* values.

The available power gain G_A is required for noise calculations, as mentioned above, but beyond this it is of no importance.

27.4.6 Gain with Impedance Matching at Both Sides

With identical resistances at the input and output, matching at both sides means that, for the ideal amplifier in Fig. 27.26, $R_g = r_i = r_o = R_L = Z_W$. In this case, all gain definitions are identical:

$$G = G_I = G_T = G_A = \frac{A^2}{4} = 4\,A_B^2 \tag{27.33}$$

This is also true for a general amplifier which can be demonstrated by comparing the equations on the basis of the S and Y parameters, taking into account the given matching conditions. Due to the length of the required calculations, proof thereof is not given here.

Using the S parameters for an amplifier matched at both sides with $R_g = R_L = Z_W$ leads to:

$$S_{11} = S_{22} = r_g = r_L = 0 \quad \Rightarrow \quad G = G_I = G_T = G_A = |S_{21}|^2$$

This is a simple relationship because the measuring condition $R_L = Z_W$ for determining S_{21} is equal to the operating condition.

When using the Y parameters, the two-sided match to $1/Y_g = 1/Y_L = Z_W$ is reached when certain conditions are met:[10]

$$Y_{11} = Y_{22} \quad , \quad (Y_{11}Y_{22} - Y_{12}Y_{21})\, Z_W^2 = 1 \tag{27.34}$$

Then:

$$G = G_I = G_T = G_A = \frac{|Y_{21}|^2 Z_W^2}{|1 + Y_{11}Z_W|^2} \tag{27.35}$$

For an amplifier without reverse transmission $Y_{12} = 0$; from the above conditions it follows that $Y_{11} = Y_{22} = 1/Z_W$, i.e. the input resistance $r_i = 1/Y_{11}$and the output resistance $r_o = 1/Y_{22}$ must be equal to the characteristic resistance Z_W. This case corresponds to the ideal amplifier in Fig. 27.26 from which the matching conditions $r_i = Z_W$ and $r_o = Z_W$ can be directly derived if $R_g = R_L = Z_W$.

27.4.7 Maximum Power Gain with Transistors

Sect. 27.2 showed that a generalised discrete transistor can be matched at both sides if the stability factor is

$$k = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}S_{21}|} > 1 \tag{27.36}$$

and the secondary conditions

$$|S_{12}S_{21}| < 1 - |S_{11}|^2 \quad , \quad |S_{12}S_{21}| < 1 - |S_{22}|^2 \tag{27.37}$$

are met; here $S_{11}, \ldots, S_{22}$ are the S parameters of the transistor. The conditions for the Y parameters are

$$k = \frac{2\,\mathrm{Re}\,\{Y_{11}\}\,\mathrm{Re}\,\{Y_{22}\} - \mathrm{Re}\,\{Y_{12}Y_{21}\}}{|Y_{12}Y_{21}|} > 1 \tag{27.38}$$

and:

$$\mathrm{Re}\,\{Y_{11}\} \geq 0 \quad , \quad \mathrm{Re}\,\{Y_{22}\} \geq 0 \tag{27.39}$$

Maximum Available Power Gain

If matched on both sides, the transistor, *including* the matching networks, fulfils the condition $S_{11,match} = S_{22,match} = 0$ (see Fig. 27.28). The corresponding power gain is known as the *maximum available power gain* (*MAG*) and is given by [27.1]:

$$MAG = |S_{21,match}|^2 = \left|\frac{S_{21}}{S_{12}}\right| \left(k - \sqrt{k^2 - 1}\right) = \left|\frac{Y_{21}}{Y_{12}}\right| \left(k - \sqrt{k^2 - 1}\right) \tag{27.40}$$

At high frequencies, *MAG* is inversely proportional to the square of the frequency: $MAG \sim 1/f^2$, which corresponds to a declining rate of 20 dB/decade. This is caused by the frequency dependence of the S and Y parameters.

[10] These conditions are determined by calculating the Y parameters according to Fig. 24.40 on page 1227 from the S parameters while taking into account the condition $S_{11} = S_{22} = 0$.

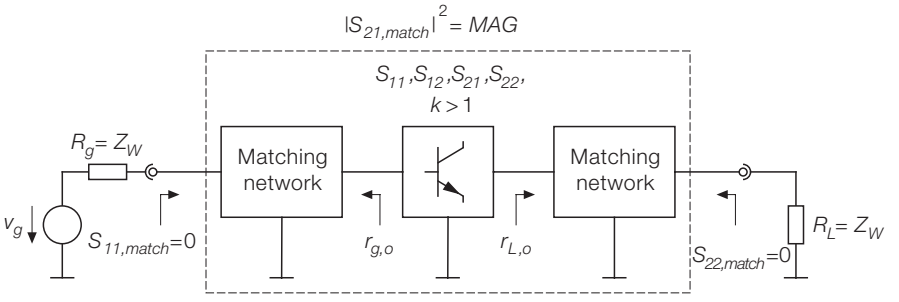


Fig. 27.28. *Maximum available power gain* (MAG) of an amplifier matched at both sides

Maximum Stable Power Gain

At frequencies above approximately a quarter of the transit frequency, the conditions for impedance matching at both sides are usually met. Below this frequency range $k < 1$, i.e. matching at both sides is no longer possible; in this case the maximum available power gain is not defined. Only the *maximum stable power gain* (*MSG*) can be achieved [27.1]:

$$MSG = \left|\frac{S_{21}}{S_{12}}\right| = \left|\frac{Y_{21}}{Y_{12}}\right| \tag{27.41}$$

At low frequencies it is approximately inversely proportional to the frequency: $MSG \sim 1/f$, which corresponds to a rate of decline of 10 dB/decade. When approaching the frequency for $k = 1$, the decline rate increases to 20 dB/decade resulting in a smooth transition between *MSG* and *MAG*.

Unilateral Power Gain

The highest achievable power gain is the *unilateral power gain* (U):

$$U = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left\{\frac{S_{21}}{S_{12}}\right\}} = \frac{|Y_{21} - Y_{12}|^2}{4\left(\mathrm{Re}\{Y_{11}\}\,\mathrm{Re}\{Y_{22}\} - \mathrm{Re}\{Y_{12}Y_{21}\}\right)} \tag{27.42}$$

This assumes that the transistor is *neutralised* by suitable circuitry, i.e. it has no reverse transmission; it then operates *unilaterally*. Circuits for neutralisation are described in Sect. 27.2. At high frequencies, the unilateral power gain is approximately inversely proportional to the square of the frequency: $U \sim 1/f^2$, which corresponds to a decline rate of 20 dB/decade.

Limit Frequencies

The maximum available power gain (*MAG*) assumes the value 1 or 0 dB at the transit frequency f_T of the transistor. The unilateral power gain (U) is higher than one even above the transit frequency since the reverse transmission is eliminated. The frequency at which U assumes the value 1 or 0 dB is called the *maximum oscillation frequency* f_{max}. This represents the maximum frequency at which the transistor can be operated as an oscillator.

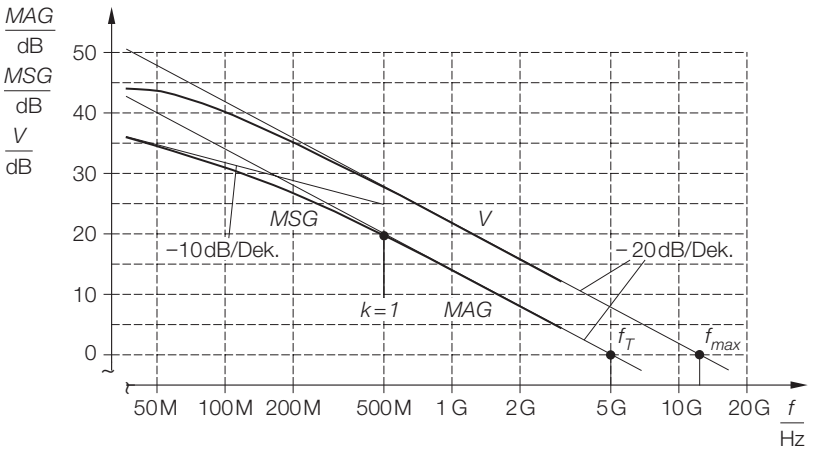


Fig. 27.29. Maximum power gains for transistor BFR93 at $V_{CE,A} = 5\,\mathrm{V}$ and $I_{C,A} = 30\,\mathrm{mA}$

Example: Figure 27.29 shows the maximum power gains for transistor BFR93 at $V_{CE,A} = 5\,\mathrm{V}$ and $I_{C,A} = 30\,\mathrm{mA}$. The maximum available power gain (*MAG*) is only defined for $f > 500\,\mathrm{MHz}$ as only here does the stability factor k rise above one. It declines at a rate of 20 dB/decade and assumes the value 1 or 0 dB at the transit frequency $f_T = 5\,\mathrm{GHz}$. For $f < 500\,\mathrm{MHz}$ the maximum stable power gain (*MSG*) is obtained which, at lower frequencies, declines at a rate of 10 dB/decade. At high frequencies the unilateral power gain U is higher than *MAG* by approximately 7.5 dB and assumes the value 1 or 0 dB at $f_{max} = 12\,\mathrm{GHz}$.

In transistors with transit frequencies above 20 GHz, the collector-base capacitance C_C or the gate-drain capacitance C_{GD} are usually reduced to such an extent that the transistor can be regarded as having no reverse transmission even without neutralisation. In this case, the maximum oscillation frequency f_{max} is only slightly higher than the transit frequency f_T.

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Electronic Circuits
Handbook for Design and Application
Tietze, U.; Schenk, C.
2007, Approx. 1700 p., 1600 illus., Hardcover
ISBN: 978-3-540-00429-5