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High Performance Distributed On-Chip Voltage Regulation for Modern Integrated Systems

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High Performance Distributed On-Chip Voltage Regulation for Modern Integrated Systems

by

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DEDICATION

To those who seeded or nourished my life.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Distributed on-chip voltage regulation where multiple voltage regulators are distributed among different locations of the chip demonstrates advantages as compared to on-chip voltage regulation utilizing a single voltage regulator. Better on-chip voltage noise performance and faster transient response can be realized due to localized voltage regulation. Despite the advantages of distributed on-chip voltage regulation, unbalanced current sharing issue can occur among each voltage regulator, which has been demonstrated to deteriorate power conversion efficiency, stability, and reliability of the power delivery network. An effective balanced current sharing scheme that can be applied to most voltage regulator types is proposed to balance the current sharing. Furthermore, a relatively high on-chip temperature induced by increased power density leads to prominent voltage regulator performance degradations due to aging. The emerging type of digital low-dropout regulator is investigated regarding aging induced transient and steady state performance degradations. Reliability enhancement techniques for digital low-dropout regulators are developed and verified. Such techniques introduce negligible power and area overhead and do not affect the normal operations of digital low-dropout regulators. Reliability enhancement techniques also reduce the area overhead needed to mitigate aging induced performance degradations. Area overhead saving further translates into more space for increased number of distributed on-chip voltage regulators, enabling scalable on-chip voltage regulation.

CHAPTER 1:

INTRODUCTION

1.1 Power Delivery Networks

Power delivery networks are essential parts of modern integrated systems such as processors, internet of things (IoT) devices, and energy harvesting platforms to supply the required power and voltage levels to each functional block within these systems. Representative power delivery network components [1–3] for modern integrated systems are shown in Fig. 1.1, which include power supply/off-chip voltage regulators, printed circuit board (PCB) with parasitics, package and bumps, global power grid, on-chip voltage regulators, and local power grid. The power and voltage levels generated by the power supply or off-chip voltage regulators feed to the integrated system through PCB. PCB and global power grid are connected through package and bumps. Global and local power grids are, respectively, connected to the inputs and outputs of on-chip voltage regulators. On-chip voltage regulators provide the required power and voltage levels to the load circuits through local power grid.

Performance of the whole power delivery network such as power conversion efficiency, stability, and reliability largely replies on the characteristics of each individual component and the interactions among them [4–29]. Conventionally, a single on-chip voltage regulator per functional block is utilized to supply the load circuits. Such an on-chip power delivery scheme may not be able to satisfy the stringent on-chip voltage noise performance requirement especially when each functional block occupies a relatively large chip area and the load current changes can be considerable and abrupt [30, 31]. The emerging distributed on-chip voltage regulation [4, 7, 18, 19, 25] is a viable solution to achieve better on-chip voltage noise performance. Within such a power delivery scheme, multiple tiny on-chip voltage regulators are distributed within each functional block to
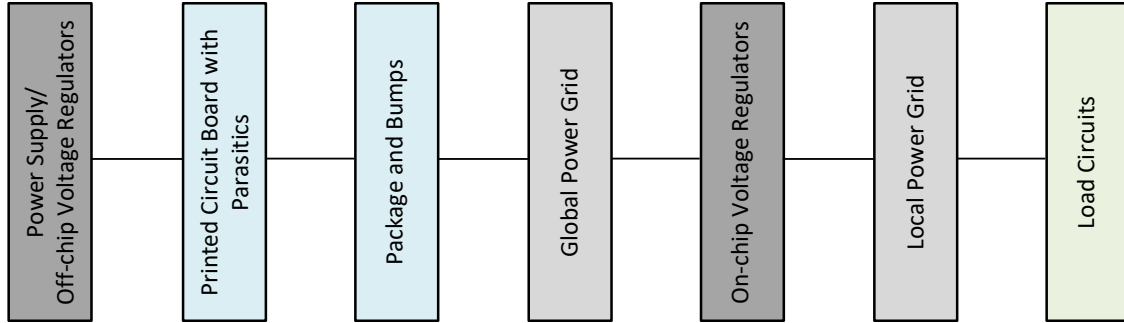
Figure 1.1: Representative power delivery network components for modern integrated systems.

regulate the voltage and supply the load current. Localized on-chip voltage regulation enabled by each individual voltage regulator can rapidly mitigate the voltage overshoot and undershoot due to load current changes to realize better on-chip voltage noise profile.

By adaptively turning on or off some of the distributed on-chip voltage regulators, the regulator-gating methodology [15] can be adopted to achieve optimal power efficiency. Moreover, once the optimal number of active on-chip voltage regulators is determined, the locations of these active on-chip voltage regulators can be decided in a thermally-aware fashion to optimize the on-chip thermal profile [31]. The locations of the distributed on-chip voltage regulators together with decoupling capacitors at the design stage have also been investigated to achieve better voltage noise performance [5]. Due to the large number of distributed on-chip voltage regulators and the sophisticated interactions among different voltage regulators and the on-chip power grids, conventional stability checking criteria for individual voltage regulator cannot be directly applied. Efficient localized stability checking schemes [32, 33] have been proposed to address this issue.

More recently, power delivery network has been leveraged to enhance the security of modern integrated systems [34–61]. The output voltage ripple of a multiphase switched capacitor converter has been shown to be related to the activation/deactivation pattern of different phases in [61]. Through randomly changing the activation/deactivation pattern of a multiphase switched capacitor converter, the security level against side channel power analysis attacks is enhanced. Converter-reshuffling technique is proposed in [59] to further improve the security feature against side-channel attacks by randomly changing the active converter stages even when there is no load current change. Time-delayed converter-reshuffling [48], charge-withheld converter reshuffling [46], and false key-

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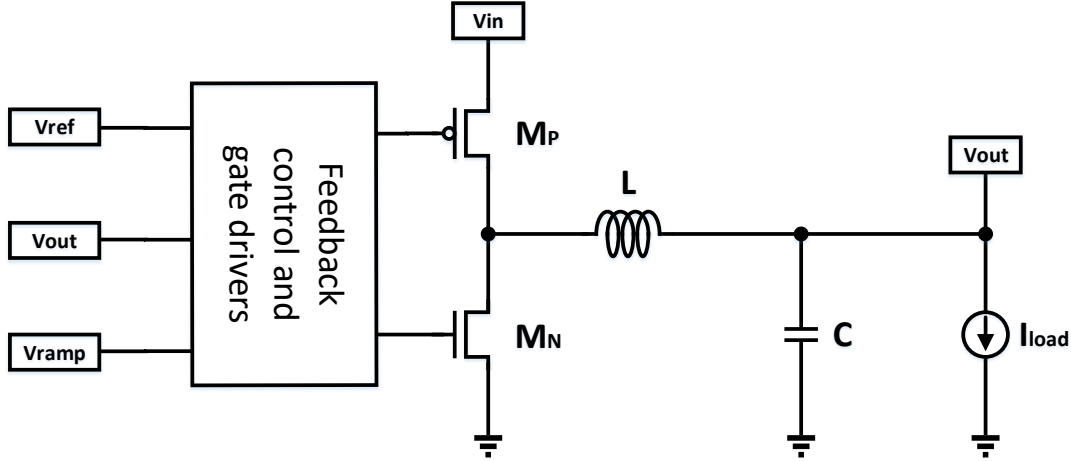
Figure 1.2: Schematic of a buck converter.

controlled aggressive voltage scaling [42] are more advanced countermeasures against power analysis attacks through leveraging different characteristics of power delivery network. Multiphase on-chip voltage regulators have been exploited as strong physical unclonable function (PUF) primitives to secure IoT devices [35]. Distributed on-chip power delivery also demonstrates advantages against electromagnetic (EM) side-channel attacks [51].

Individual voltage regulator is an essential part of distributed on-chip voltage regulation systems. Different types of on-chip voltage regulators demonstrate their respective advantages that can be utilized for different application scenarios. Typical on-chip voltage regulator types include buck converters, low-dropout regulators (LDOs), and switched capacitor converters which are briefly illustrated below.

1.1.1 Buck Converters

Buck converters consist of power switches M_P and M_N, an LC filter, feedback control circuits, and gate drivers as shown in Fig. 1.2. Feedback control circuits sense the output voltage V_{out} change and compare the instant V_{out} with a reference voltage V_{ref} to determine if the duty cycle of the power transistor gate signals needs to be increased or decreased. A ramp signal V_{ramp} is utilized for pulse width modulation (PWM) signal generation. The intermediate voltage generated in the middle of the power transistors M_P and M_N is filtered to supply the load. Buck converters
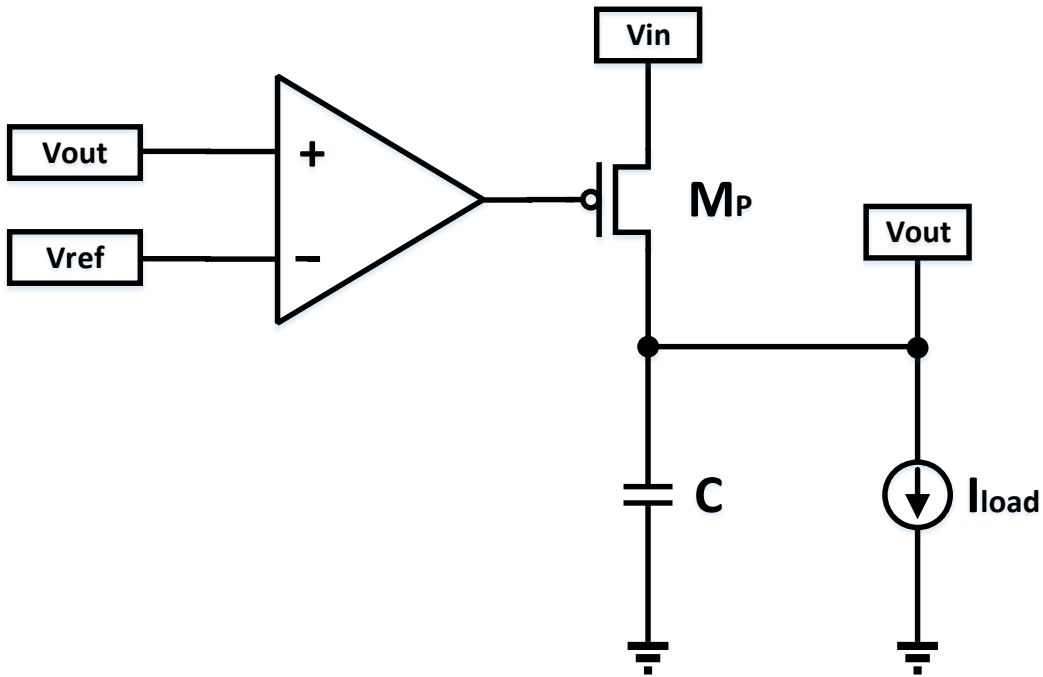
Figure 1.3: Schematic of a low-dropout regulator.

can achieve high power conversion efficiency over a wide load current range and are implemented in recent Intel Core^{TM} SoCs [62].

1.1.2 Low-Dropout Regulators

LDOs have the benefits of easy implementation and fast transient response speed. The schematic of a conventional analog LDO is shown in Fig. 1.3. It consists of a power transistor M_P, an error amplifier, and an output capacitor. The error amplifier senses the output voltage V_{out} changes and compares the instant V_{out} with the reference voltage V_{ref} to generate the gate signal of M_P for output voltage regulation. When M_P is divided into a power transistor array and controlled by a digital logic, digital LDOs [63] are formed which can operate under low supply voltages for IoT applications. LDOs are widely used in recent IBM [64] and Intel products [65, 66].

4
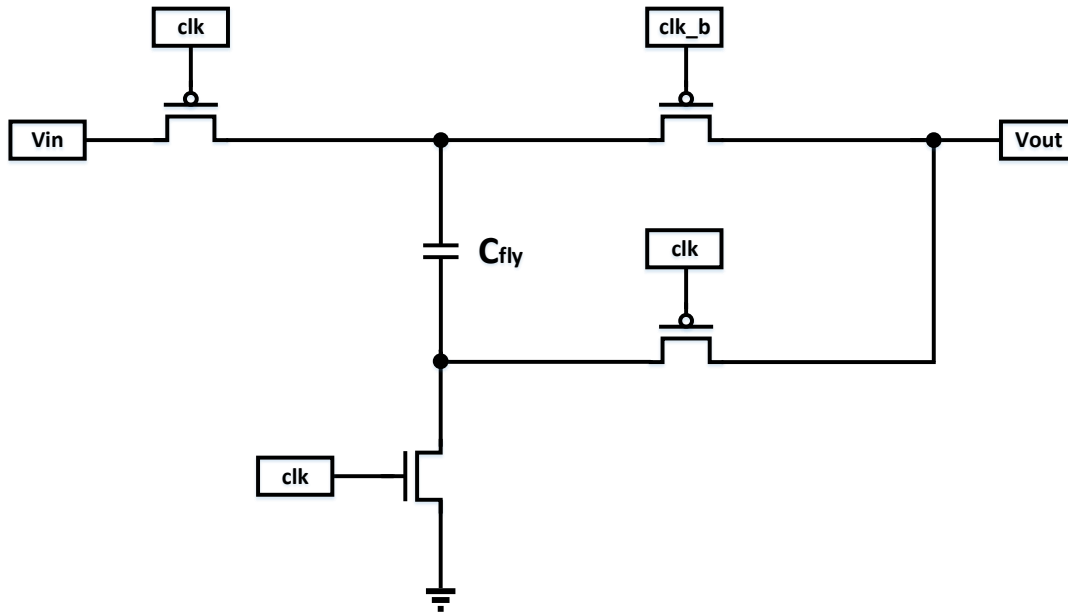
Figure 1.4: Schematic of a switched capacitor converter with 2:1 conversion ratio.

1.1.3 Switched Capacitor Converters

Switched capacitor (SC) converters consist of only capacitors and switches. The schematic of a SC converter with 2:1 conversion ratio is shown in Fig. 1.4. It includes four switches and one flying capacitor C_{fly}. The switches are controlled by complementary clock signals *clk* and *clk_b*. C_{fly} is charged when connected to input voltage V_{in} and discharged when only connected to V_{out} and ground. As no inductor is needed, SC converters have the benefits of easy integration. Through varying the topologies of capacitors and switches, different conversion ratios as well as reconfigurable conversion ratios can be achieved [67]. A high power density of 3.2 W/mm^2 can also be realized utilizing a switched capacitor converter [68]. Distributed version of a multiphase SC converter has also been implemented in the form of a DC-DC converter ring to achieve fast dynamic voltage scaling [69].

1.2 Our Contribution

Efficiency, stability, and reliability implications of unbalanced current sharing phenomenon among distributed on-chip voltage regulators are investigated. An effective balanced current sharing

5

scheme that is general enough for most voltage regulator types within the framework of distributed on-chip voltage regulation is proposed. The effectiveness and benefits of the proposed scheme are verified through extensive simulations under practical simulation settings. Furthermore, aging effects on the emerging digital LDOs, which are essential parts of distributed on-chip voltage regulation systems, are demonstrated to degrade transient and steady state performance. Aging mitigation techniques that induce negligible power and area overhead are proposed and verified.

1.3   Organization

The content of this work is organized as follows. In Chapter 2, unbalanced current sharing issue is discussed and the corresponding balanced current sharing scheme is proposed and verified. Aging effects on the transient and steady state performance degradation of on-chip voltage regulators are, respectively, investigated in Chapters 3 and 4. Conclusions and future work are, respectively, offered in Chapters 5 and 6.

CHAPTER 2:

UNBALANCED CURRENT SHARING AMONG DISTRIBUTED

ON-CHIP VOLTAGE REGULATORS

2.1 Introduction

Efficient, stable, and reliable operation of power delivery networks (PDNs) are crucial to sustain high performance and low power design targets of modern large scale integrated circuits (ICs).[1] Thermal design power (TDP) of microprocessors has increased over generations and can go beyond 100W [2]. The peak power of a microprocessor can, however, be 1.5 times the TDP rating [70]. Even small power conversion efficiency degradations within such power-hungry ICs lead to tremendous power loss, resulting in higher heat dissipation. Meanwhile, the complexity and large component count incur serious stability and reliability concerns.

Voltage regulators (VRs) as an essential part of PDNs, including commonly used buck, switched capacitor, and low-dropout regulators, have been moved from off-chip placements to on-chip implementations to save board area and to enable efficient, fast, and secure localized voltage regulation [61, 71, 72]. Distributed on-chip voltage regulation has recently become an emerging research field where multiple on-chip VRs are connected in parallel and distributed across the power grid to supply current across the whole die [32, 33, 73–78]. Previous work mainly focuses on the efficiency improvement of stand-alone VRs [71] and that of the PDNs as a whole [79]. The implications of the complex interactions among on-chip VRs and the power grid have, however, been typically overlooked. Although there are appealing benefits of the distributed on-chip voltage regulation, complex interactions among regulators and the power grid may lead to significant efficiency,

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[1]This chapter was published in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 11, pp. 3019-3032, November 2017 "Efficiency, Stability, and Reliability Implications of Unbalanced Current Sharing among Distributed On-Chip Voltage Regulators". Permission is included in Appendix A.

stability, and reliability issues. Among the various implications of distributed on-chip voltage regulation, unbalanced current sharing, if not carefully controlled, can stultify the previously proposed efficiency enhancement benefits or even shorten the lifetime of the chip.

Unbalanced current sharing problem has been widely studied in conventional power electronics field for multiphase interleaving buck regulators [80, 81]. Little attention has, however, been paid to this problem within microelectronics field for distributed on-chip voltage regulation and, to the best of the authors' knowledge, the efficiency, stability, and reliability implications of unbalanced current sharing within distributed on-chip PDNs have not yet been investigated.

Voltage regulators within distributed on-chip PDNs, are connected to a passive mesh network [2], which supplies the required current to the load circuits. Several factors may lead to unbalanced current sharing within distributed on-chip power delivery systems that consist of multiple parallel VRs. These factors include mismatches in the component values and control loop mismatches, which are common factors leading to the unbalanced current within conventional centralized multiphase regulators [80, 81]. Specific to distributed on-chip PDNs, the power grid parasitic impedance among the VRs and load circuits, although quite small, may have significant variations based on the placement of the VRs and the load circuits. Therefore, even with perfectly matched components and control loops among different distributed on-chip VRs, the variations of the power grid resistance among individual VRs and load circuits may lead to non-negligible mismatch and severe current sharing problems.

The contribution of this chapter is threefold. First, the unbalanced current sharing problem is presented with extensive simulations in both Cadence Virtuoso and VoltSpot [82]. Power efficiency, stability, and reliability implications of the unbalanced current sharing within distributed on-chip PDNs are investigated. Theoretical derivations and simulation results lead to the observation that unbalanced current sharing can adversely affect the important design concerns, which necessitates an efficient current balancing scheme. Second, an adaptive reference voltage control mechanism is proposed as the current balancing scheme for distributed on-chip VRs to dynamically modulate the reference voltage of each individual VR. Circuit implementations are analyzed for the proposed control algorithm and preliminary simulations are performed to verify the effec-
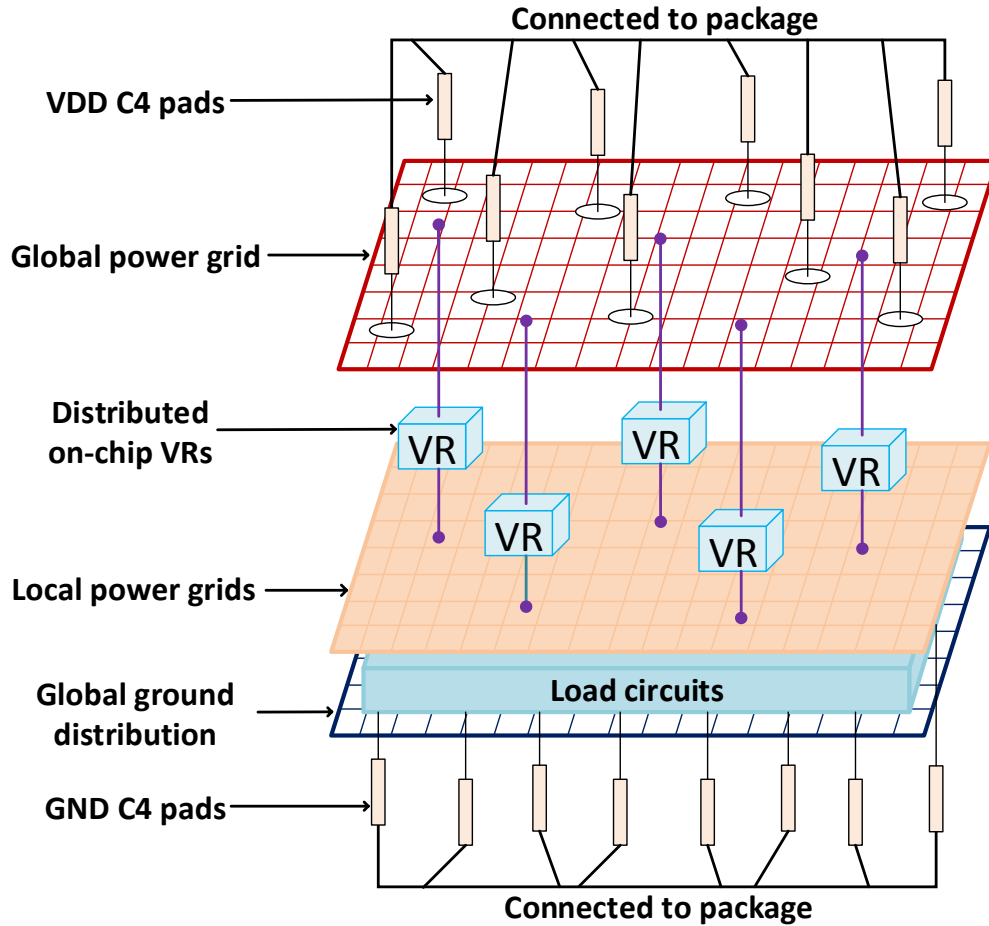
Figure 2.1: On-chip power delivery network with distributed voltage regulators.

tiveness. Finally, an IBM POWER8-like [64] microprocessor simulation platform is constructed in VoltSpot [82] to study the implications of the unbalanced current sharing problem in practical applications. Extensive simulations based on several benchmarks are performed and simulation results confirm the benefits of balanced current sharing. Although the analyses are conducted assuming a homogeneous PDN with buck regulators, without loss of generality, the proposed technique can be easily applied to heterogeneous PDNs that house different regulator types.

2.2   The Unbalanced Current Sharing Problem

An on-chip PDN model with distributed VRs is shown in Fig. 2.1. The inputs of the distributed VRs are connected to a global power grid that is connected to the package through
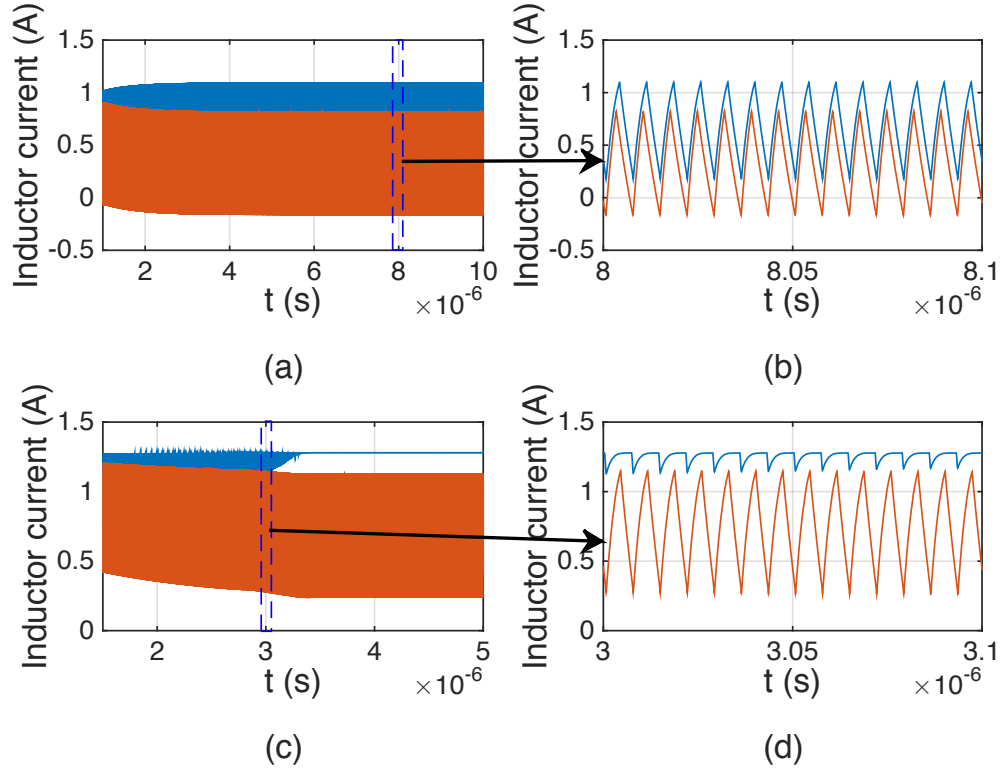
Figure 2.2: Unbalanced current sharing between two identical distributed on-chip buck regulators. (a) Inductor currents of two identical regulators supplying total load current of 1A. (b) A zoomed view of the inductor current profiles at steady state. (c) Inductor currents of two identical regulators supplying total load current of 2A, one inductor current goes saturated due to the maximum 1.27A load current one regulator can supply. (d) A zoomed view of the inductor current profiles showing the saturation of one inductor current.

the dedicated C4 pads. The outputs of the distributed on-chip VRs provide the required current at the target voltage level to the local power grid that feeds the load circuits. The global ground distribution provides the ground plane for the load circuits and is connected to the package through the dedicated GND C4 pads. The global and local power grid, and the global ground distribution are composed of orthogonal metal lines connected with vias [2]. With a first order approximation, these power grids can be modeled as a resistive mesh where the effective resistance between any two nodes on the power grid depends on the distance between the two nodes [30, 83]. The effective resistance mismatch between the distributed VRs with only local voltage regulation loops may cause unbalanced current sharing among the VRs and may even cause VR malfunctions.
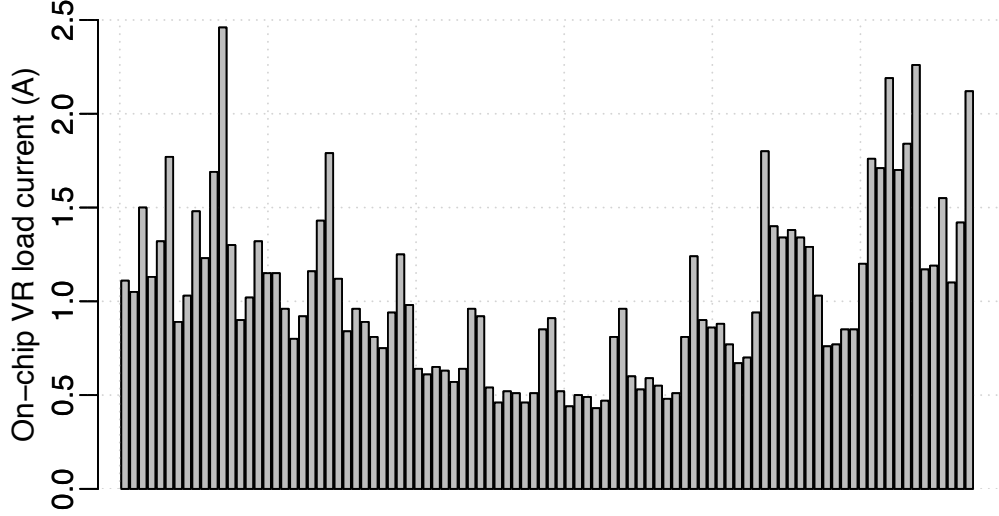
Figure 2.3: Unbalanced current sharing among 96 identical distributed on-chip VRs within IBM POWER8 like microprocessor.

To demonstrate the unbalanced current sharing problem, two sets of simulations are performed. First, two identical buck regulators providing localized voltage regulation are designed and simulated in Cadence Virtuoso using IBM 130nm CMOS process. The input voltage of the buck regulator is 3.3V and the output voltage is 1V. The switching frequency is 140MHz with a $5n$H inductor. The peak to peak current ripple on the inductor is about 1A and the load regulation is 0.02%/A. Each regulator has a maximum load current supply capability of 1.27A. The on-chip power grid is designed as a resistive mesh using the design parameters of respective metal layers in [84]. Second, a buck regulator model is extracted and included in VoltSpot [82] for PDN simulations with large number of on-chip VRs. An IBM POWER8 like processor with 96 identical distributed regulators is used in the simulations. Detailed VoltSpot simulation setup is explained in Section 2.7. Simulation results demonstrating the unbalanced current sharing problem in both Cadence Virtuoso and VoltSpot are summarized in this section.

2.2.1 Large Current Variations

The load current supplied by a buck regulator is the average value of the respective inductor current. The inductor current of the two regulators when the total load current is 1A is shown in

11

Fig. 2.2 (a) and (b). Due to the difference in the effective resistance for the two regulators, these regulators have different average inductor current values of 328.7mA and 671.3mA, respectively. With unbalanced current sharing, one regulator supplies more than twice the output current than the other. With a larger effective resistance mismatch, the difference can be even larger.

The output current values of the 96 identical distributed on-chip VRs within an IBM POWER8 like microprocessor chip for application lu_ncb is shown in Fig. 2.3. The detailed simulation setup is explained in Section 2.7. In this simulation, 96 on-chip VRs are evenly distributed across the chip. As can be seen from Fig. 2.3, large current variations occur among these on-chip VRs. The highest current supplied by one VR goes up to nearly 2.5A and the lowest current supplied by one VR is around 0.5A. There is 5x difference between the highest and lowest on-chip VR current.

2.2.2 Voltage Regulator Malfunctions

For the same two buck regulator design at the same physical locations on the power grid as used in Section 2.2.1, with a higher total load current of 2A, the inductor current distribution between the two regulators is shown in Fig. 2.2 (c) and (d). As can be seen from these figures, the difference between the two regulator inductor currents gradually becomes larger and at steady state one inductor becomes saturated and provides a constant current. For the saturated regulator, the pull-up pMOS transistor is always on, leading to 100% duty cycle operation and the malfunction of the VR. When the total load current is equally shared between the two, the malfunction of the VRs could be avoided as the current supplied by each VR is less than the maximum VR current capability.

Note that, in Fig. 2.3, on-chip VR model is included in VoltSpot for current distribution simulations and no limit is set for the maximum current that an individual VR can provide. If the output current capability of a VR is designed to be 1.5A, there would be more than ten on-chip VRs that enter this saturation point in this simulation, leading to chip-wide VR malfunctions. As over-current protection schemes are implemented for most VRs, VR malfunctions can be avoided. However, overloaded current can lead to output voltage drop [85], which is still not acceptable.
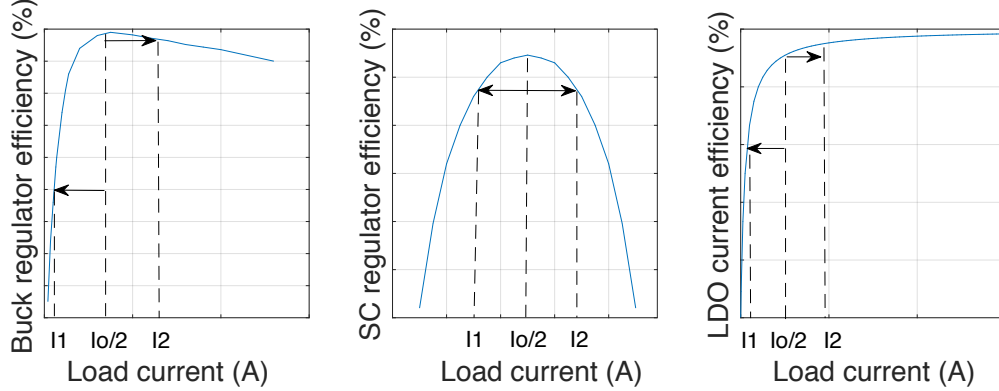
Figure 2.4: Conventional buck regulator, SC regulator, and LDO efficiency curves.

Furthermore, as one VR supplies 5x current than the other, huge current density can lead to local hotspots of the VR and even destroy the VR and the nearby functional blocks.

With unbalanced current sharing, each on-chip VR needs to be designed for the worst case scenario to be able to supply the highest possible current with high efficiency. The size of power MOSFETs needs to be increased as compared to the design targeting at the total load current divided by N for N distributed VRs, which may introduce extra power and area overhead as power MOSFETs can occupy a large percentage of the total VR area.

2.3 Efficiency Implications of Unbalanced Current Sharing

Power conversion efficiency curves for the conventional buck, SC, and LDO regulators are shown in Fig. 2.4. Consider two identical distributed on-chip buck or SC regulators with each design optimized at $I_o/2$ for a total load current of I_o. With balanced current sharing, each buck or SC regulator operates at the optimum design point, providing maximum efficiency. With unbalanced current sharing, one regulator provides lower current I_1 while the other one provides higher current I_2. As can be seen from Fig. 2.4, any variation in the load current from the optimum load current point leads to an unavoidable power efficiency loss. For LDOs, the efficiency is determined by

$$\eta_{LDO} = \frac{I_o V_o}{(I_o + I_q)V_i},$$ (2.1)

13

where I_o is the output current of the LDO and I_q is the quiescent current. With balanced current sharing, each LDO provides $I_o/2$ current and the total efficiency is $(I_oV_o/2)/(I_o/2 + I_q)V_i = I_oV_o/(I_o + 2I_q)V_i$. With unbalanced current sharing, one of the LDOs provides I_1 current and the other one provides I_2 current with $I_1 + I_2 = I_o$. Since MOS transistors have a nearly constant quiescent current with respect to the load current [86], the total efficiency can be expressed as $(I_1 + I_2)V_o/(I_1 + I_2 + 2I_q)V_i$, which is the same as the balanced current sharing case. Theoretically, there is no significant efficiency degradation due to unbalanced current sharing for LDOs, however, larger currents induced by the unbalanced current sharing do adversely affect the reliability as will be discussed in Section 2.5.

Buck regulators will be the focus throughout the chapter, however, the proposed techniques can also be tailored for SC and LDO regulators. The regulator loss model and optimum efficiency discussions are provided in Section 2.3.1 . The extra power loss and efficiency degradation induced by unbalanced current sharing for the general case of N identical distributed on-chip regulators are theoretically explored in Section 2.3.2.

2.3.1 Regulator Loss Model and Efficiency

The simplified schematic of a synchronous buck regulator is shown in Fig. 2.5. It is composed of high-side (Q1) and low-side (Q2) power MOSFETs for synchronous rectification, LC filter with parasitic resistances R_{DCR} and R_{ESR}, and a feedback control path.

The simplified power loss model in [87] is enhanced by including the conduction loss of the capacitor ESR (P_{ESR}) for the power loss analysis in synchronous buck regulators

$$P_{loss} = R_{eq} \cdot i_{rms}^2 + P_{ESR} + A \cdot f \tag{2.2}$$

where R_{eq} is the regulator equivalent resistance, i_{rms} is the inductor RMS current, A is the switching power loss factor, and f is the regulator switching frequency. Detailed power loss analysis and expressions for R_{eq}, P_{ESR}, and A can be referred to [87, 88].

14
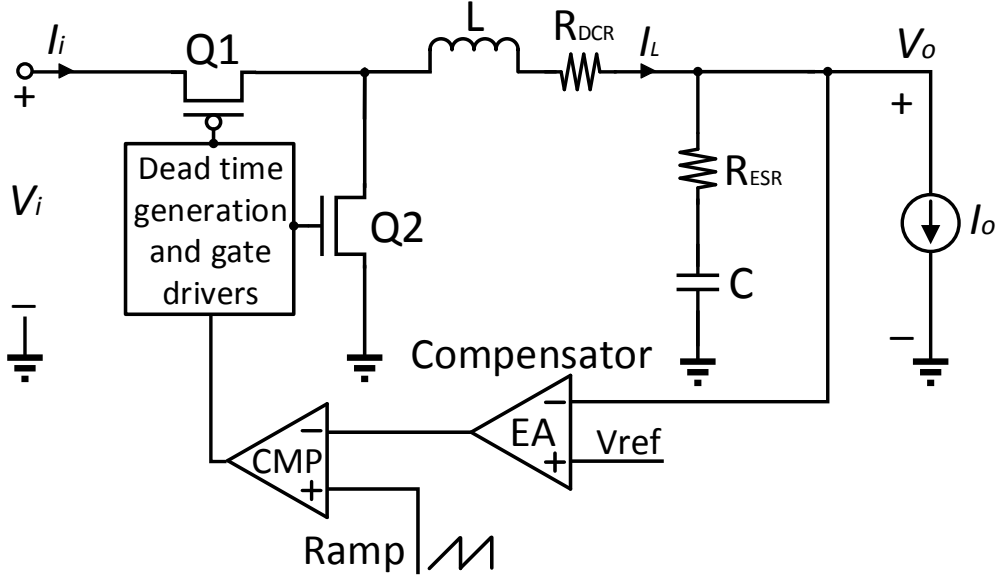
Figure 2.5: Simplified schematic of a synchronous buck regulator.

Power conversion efficiency can be written as

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}. \tag{2.3}$$

Since P_{ESR} is independent of the regulator output current I_o, by setting $\partial\eta/\partial I_o = 0$, the maximum efficiency for the continuous conduction mode (CCM) operation is obtained as [87]

$$\eta_{max} = \frac{1}{1 + 2\frac{R_{eq}}{V_o} \cdot I_{o\_opt}} \tag{2.4}$$

at the optimum load current of

$$I_{o\_opt} = \sqrt{\frac{A \cdot f + P_{ESR}}{R_{eq}} + \frac{1}{12}I_{p-p}^2} \tag{2.5}$$

where V_o and I_{p-p} are, respectively, the regulator output voltage and inductor peak to peak current.

2.3.2 Efficiency Degradation of Distributed Regulators with Unbalanced Current Sharing

Consider two identical buck regulators and assume the total load current supplied by these two regulators is I_o and each regulator design is optimized at $I_o/2$. With unbalanced current sharing, the load current supplied by the two regulators are, respectively, I_1 and I_2 for regulators 1 and 2. Current sharing ratio (CSR) for the two regulators are

$$CSR_1 = \frac{I_1}{I_o}, CSR_2 = \frac{I_2}{I_o}. \tag{2.6}$$

According to (2), for CCM operations, the extra power loss induced by the unbalanced current sharing for two regulators as compared to the balanced case is

$$P_{loss\_2}^{ex} = R_{eq} \cdot I_o^2 \cdot (CSR_1^2 + CSR_2^2 - \frac{1}{2}) \tag{2.7}$$

and $P_{loss\_2}^{ex} = 0$ if and only if when $CSR_1 = CSR_2 = 1/2$, otherwise $P_{loss\_2}^{ex} > 0$, which means that unbalanced current sharing leads to extra power loss.

Efficiency degradation due to unbalanced current sharing can be written as

$$\eta_{deg\_2} = \eta_{max}|_{I_{o\_opt}=\frac{I_o}{2}} - \frac{V_o}{\frac{V_o}{\eta_{max}|_{I_{o\_opt}=\frac{I_o}{2}}} + R_{eq} \cdot I_o \cdot (CSR_1^2 + CSR_2^2 - \frac{1}{2})}, \tag{2.8}$$

where $\eta_{max}|_{I_{o\_opt}=\frac{I_o}{2}}$ is the maximum efficiency at the optimum load current of $I_o/2$. Note that $\eta_{deg} = 0$ for balanced current sharing.

Equations (2.7) (2.8) can be generalized for N identical distributed on-chip VRs with each design optimized at I_o/N for a total load current of I_o as explained below.

The extra power loss induced by unbalanced current sharing with CSR_i for the ith regulator is

$$P_{loss\_N}^{ex} = R_{eq} \cdot I_o^2 \cdot (\sum_{i=1}^{N} CSR_i^2 - \frac{1}{N}). \tag{2.9}$$
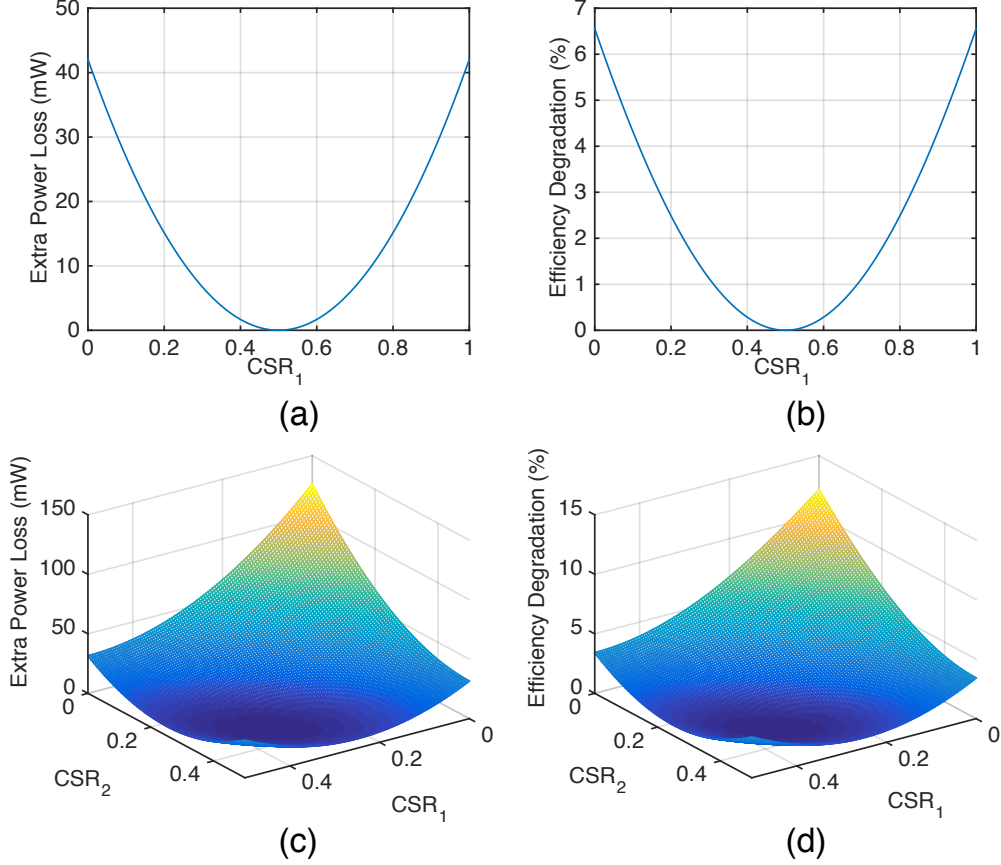
Figure 2.6: Unbalanced current sharing induced extra power loss and efficiency degradation as a function of CSR_i for N identical distributed on-chip VRs. (a) Extra power loss, N=2. (b) Efficiency degradation, N=2. (c) Extra power loss, N=3. (d) Efficiency degradation, N=3.

The total efficiency degradation induced by unbalanced current sharing is

$$\eta_{deg\_N} = \eta_{max}|_{I_{o\_opt}=\frac{I_o}{N}} - \frac{V_o}{\frac{V_o}{\eta_{max}|_{I_{o\_opt}=\frac{I_o}{N}}} + R_{eq} \cdot I_o \cdot (\sum_{i=1}^{N} CSR_i^2 - \frac{1}{N})}. \quad (2.10)$$

Note that (2.9) (2.10) can be applied to a wide range of load current. As phase shedding technique [62, 89] for conventional multiphase converters and converter gating technique [61] for distributed on-chip VRs are well developed to enhance the light load efficiency and achieve a high efficiency over a wide load range, the number of active VRs N_{active} can be dynamically changed to make sure that each regulator can operate at the optimal efficiency point under various load

conditions with balanced current sharing. Thus, (2.9) (2.10) hold for extra power loss and efficiency degradation calculations under a wide load range.

As an example, using design parameters in [71] for the fully integrated buck regulator, the extra power loss and efficiency degradation are evaluated for two and three distributed buck regulator cases with different CSR values. Each regulator is optimized at 225mA and the total load currents are, respectively, 450mA and 675mA for two and three regulator cases. As can be seen from Fig. 2.6, as CSR varies from the balanced current sharing point ($CSR_1 = 0.5$ for two regulator case, $CSR_1 = CSR_2 = 1/3$ for three regulator case), the additional power loss and efficiency degradation increase rapidly. Moreover, the highest extra power loss and efficiency degradation points for the three regulator case are worse than the two regulator case. It is difficult to visually demonstrate the extra power loss and efficiency degradation change when the number of regulators increase over three. With more number of regulators and larger output current, however, the highest extra power loss and efficiency degradation further increase. This indicates that significant attention should be paid to guarantee the proper current sharing among distributed on-chip VRs that are widely used in high performance microprocessors.

2.4   Stability Implications of Unbalanced Current Sharing

Stable operation of the stand-alone on-chip VR as well as the whole PDN is the basis for every other performance metric. Oscillations can occur due to an unstable internal feedback loop of a single VR or interactions among different VRs. The stability issue, if not properly addressed, can adversely affect important design aspects including line and load regulations, making other performance enhancing techniques useless.

Stability implications of unbalanced current sharing are explored for both individual on-chip VRs and the PDN as a whole in this section. To evaluate the effects of unbalanced current sharing on individual on-chip VRs, the state-space averaging method [90] is applied to obtain the various important transfer functions of closed loop synchronous buck regulators while considering parasitic impedances. For the stability of the whole PDN, the implications of unbalanced current sharing

can be examined by analyzing the Y-parameter model of the individual on-chip VRs based on the recently proposed hybrid stability framework for PDNs [32].

2.4.1 Stability of Individual On-Chip Voltage Regulators

The state-space expression for a conventional voltage mode controlled buck regulator with diode rectification and g-parameters has been explored in [91]. For the synchronous buck regulator operating in CCM, as shown in Fig. 2.5, the open-loop g-parameter set can be written as

$$
\begin{bmatrix} Y_{i\_o} & T_{oi\_o} \\ G_{io\_o} & -Z_{o\_o} \end{bmatrix} = \frac{\begin{bmatrix} \frac{D^2 s}{L} & \frac{D(1+sR_{ESR}C)}{LC} \\ \frac{D(1+sR_{ESR}C)}{LC} & -\frac{(R_E+sL)(1+sR_{ESR}C)}{LC} \end{bmatrix}}{s^2 + s\frac{R_E+R_{ESR}}{L} + \frac{1}{LC}}
\tag{2.11}
$$

$$
\begin{bmatrix} G_{ci} \\ G_{co} \end{bmatrix} = \frac{\begin{bmatrix} \frac{sDU_E}{L} \\ \frac{U_E(1+sR_{ESR}C)}{LC} \end{bmatrix}}{s^2 + s\frac{R_E+R_{ESR}}{L} + \frac{1}{LC}} + \begin{bmatrix} I_o \\ 0 \end{bmatrix}
\tag{2.12}
$$

where

$$
R_E = R_{DCR} + R_{on\_hs}D + R_{on\_ls}(1-D)
\tag{2.13}
$$

$$
U_E = V_i + (R_{on\_ls} - R_{on\_hs})I_o.
\tag{2.14}
$$

$Y_{i\_o}, T_{oi\_o}, G_{io\_o}, Z_{o\_o}, G_{ci}, G_{co}, D$ are, respectively, the open loop input admittance, the output to input current transfer function, the input to output voltage transfer function, the output impedance, the control to input current transfer function, the control to output voltage transfer function, and the duty cycle of the buck regulator.

The line and load regulation capabilities of a buck regulator can be examined by analyzing the closed-loop input to output voltage transfer function G_{io_c} and the output impedance Z_{o_c}, respectively. To achieve a stable line and load regulation, all poles of the corresponding transfer function need to lie within the left-half of the s-plane. The closed-loop g-parameters can be obtained
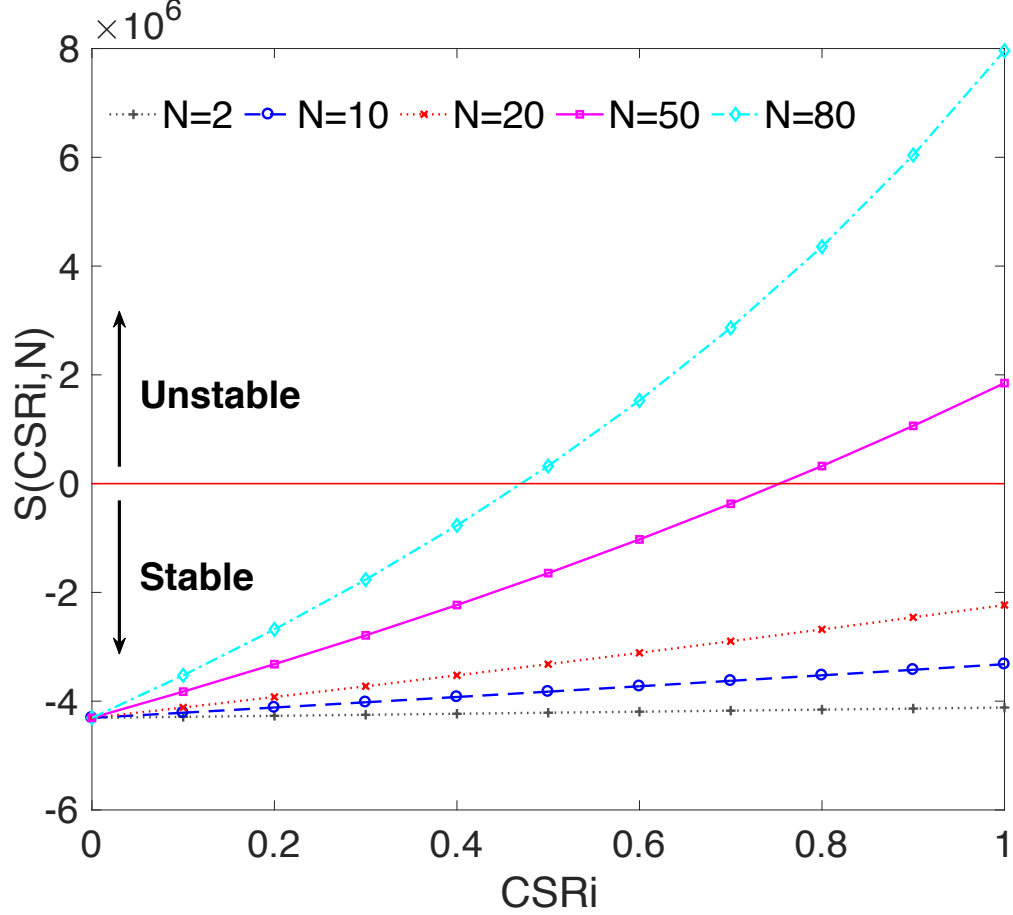
Figure 2.7: Stability of individual on-chip VR as a function of CSR_i and N.

based on the open-loop g-parameters and the relationship demonstrated in [91]. Assuming Type III compensation [92], the characteristic equation of G_{io_c} and Z_{o_c} is

$$CLs^2 + (CG_aG_{cc}G_{se}U_ER_{ESR} + CR_{ESR} + CR_E)s + G_aG_{cc}G_{se}U_E + 1 = 0 \qquad (2.15)$$

where G_{se}, G_{cc}, G_a are, respectively, the sensing gain of the output voltage, the transfer function of the error amplifier (EA) and compensator, and the PWM generator gain. Typically, G_{se} and G_a are constant. As some of the coefficients are a function of I_o, solutions of (2.15) change as I_o changes. For N identical distributed on-chip VRs with unbalanced current sharing, some of the parallel on-chip VRs will supply more current while others will supply less, leading to the movement of system poles. As the stability is affected by the right-half plane (RHP) poles, we define a CSR-

and N-dependent function $S(CSR, N)$ as

$$S(CSR, N) = \begin{cases} \max_{i=1,...,n} \{Re(p_i)\}, & \max_{i=1,...,n} \{Re(p_i)\} < 0 \\ \min_{i=1,...,j} \{Re(p_i^+)\}, & otherwise \end{cases} \tag{2.16}$$

where n, j, p_i $(i = 1, ..., n)$, p_i^+ $(i = 1, ..., j)$ are, respectively, the total number of system poles, the total number of RHP (or 0) poles, the ith system pole, and the ith RHP (or 0) pole. $|S(CSR, N)|$ either indicates how close the system is to be unstable (for $\max_{i=1,...,n} \{Re(p_i)\} < 0$) or how far the system has gone beyond the marginally stable point (for $otherwise$). The system is stable if $S(CSR, N) < 0$ and unstable otherwise.

Using similar design parameters in [71], $S(CSR_i, N)$ for the ith VR within N identical distributed on-chip VRs is plotted as a function of CSR_i and N in Fig. 2.7. It can be seen from Fig. 2.7 that, for a fixed number N, $S(CSR_i, N)$ increases as CSR_i increases. Note that although all CSR_i values are plotted even for large number of N in Fig. 2.7 for completeness, due to the maximum current supply capability of a single VR, inductor current of individual VR can become saturated and the CCM model is no longer valid. The output voltage can drop [85] for large number of N and CSR_i values, for example $N = 80$ and $CSR_i = 0.5$. Also, as N becomes large, $S(CSR_i, N)$ approaches the unstable region from the stable one as CSR_i increases, indicating the negative effects of unbalanced current sharing on the stability and proper operation of individual VR.

2.4.2 Stability of the Power Delivery Network

A sufficient condition for stability checking of the PDN network is proposed in [32] based on the hybrid stability framework. This condition consists of a complementary way of using either passivity evaluation or system gain evaluation for LTI systems. By satisfying either one of these two conditions, the stability of the PDN can be guaranteed. For stability checking using the system gain condition, a Z-parameter model of the passive subnetwork is needed for evaluation. The passive subnetwork model can vary for different applications or design requirements, which makes it difficult
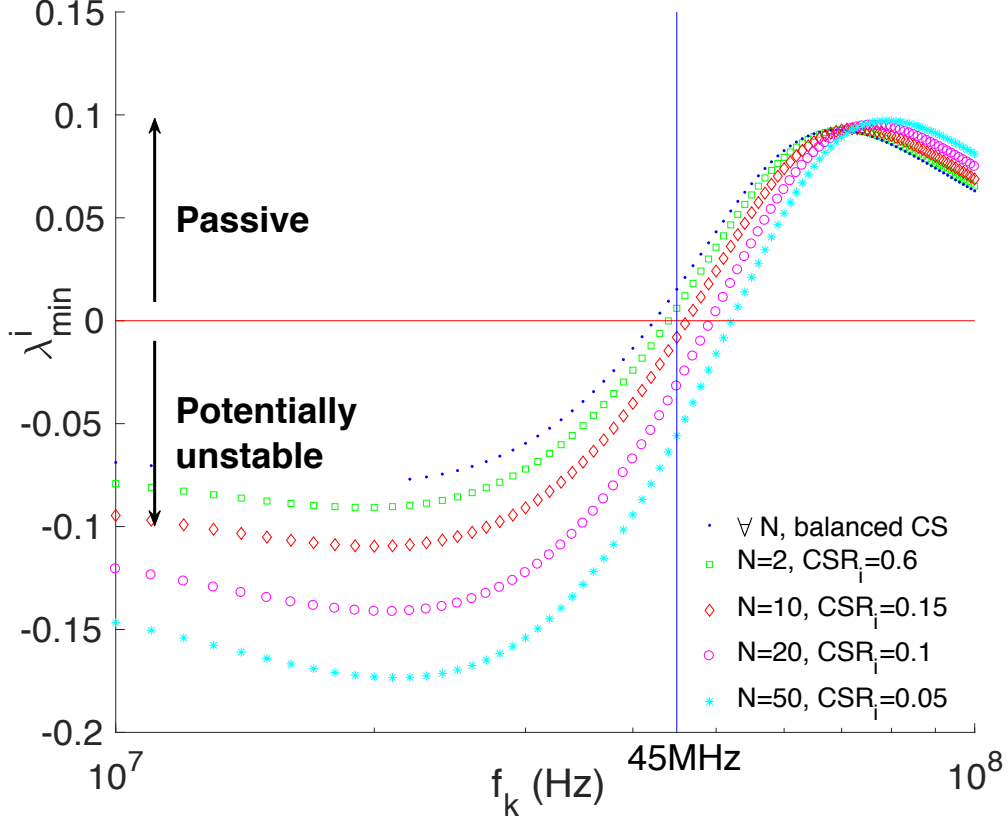
Figure 2.8: $\lambda_{min}^i(j\omega_k)$ as a function of f_k under different values of CSR_i and N. $\lambda_{min}^i(j\omega_k)$ shifts rightwards as $N \cdot CSR_i$ increases, demonstrating the adverse effects of unbalanced current sharing on VR passivity.

to evaluate the general effects of unbalanced current sharing on the stability of PDN. However, the passivity evaluation does shed light on this point.

The synchronous buck regulator system is approximated as a linear continuous-time time-invariant system through state-space averaging method [93]. Thus, the passivity criterion [32] can be applied, which is given by

$$\lambda_{min}(j\omega_k) = \min_{i=1,...,N;j=1,2}\{\lambda_j(\boldsymbol{Y}_i(j\omega_k) + \boldsymbol{Y}_i^H(j\omega_k))\} \tag{2.17}$$

where $\lambda_{min}(j\omega_k)$ is the minimum eigenvalue among any i^{th} VR at ω_k and H denotes the complex conjugate transpose. Passivity condition is met for the VRs if $\lambda_{min}(j\omega_k) \geq 0$.

The Y-parameter model for the ith VR can be obtained through the closed-loop g-parameters. Note that the Y-parameter model is a function of individual VR output current I_o and thus with unbalanced current sharing, it will be affected and so does $\lambda_{min}(j\omega_k)$. Using the same design parameters in Section 2.4.1, $\lambda_{min}^i(j\omega_k)$ is examined for the ith VR under different CSR_i and N values in Fig. 2.8, where

$$\lambda_{min}^i(j\omega_k) = \min_{j=1,2}\{\lambda_j(\boldsymbol{Y}_i(j\omega_k) + \boldsymbol{Y}_i^H(j\omega_k))\}. \tag{2.18}$$

$\lambda_{min}^i(j\omega_k)$ remains negative for $f_k < 10$MHz and positive for $f_k > 100$MHz. As I_o supplied by the ith VR, (i.e., $N \cdot CSR_i$), increases, $\lambda_{min}^i(j\omega_k)$ shifts rightwards, rendering the following

$$\lambda_{min}(j\omega_k)|_{\omega_k \leq \omega_{k0}} = \min_{i=1,...,N}\{\lambda_{min}^i(j\omega_k)\} = \lambda_{min}^i(j\omega_k)|_{CSR_i=CSR_{max}} \tag{2.19}$$

where

$$\lambda_{min}(j\omega_{k0}) = 0, \ CSR_{max} = \max_{i=1,...,N} CSR_i. \tag{2.20}$$

For example, at $f_k = 45$MHz, with balanced current sharing (CS), (i.e., $\forall N$, balanced CS), $\lambda_{min}(j\omega_k)|_{\omega_k=9\pi \cdot 10^7} > 0$, the passivity condition is satisfied. However, with unbalanced current sharing case, (e.g., $N = 20$, $CSR_i = 0.1$), $\lambda_{min}(j\omega_k)|_{\omega_k=9\pi \cdot 10^7} < 0$, which pushes the originally passive point to the potentially unstable region, indicating the adverse effects of unbalanced current sharing on the stability of the whole PDN.

2.5 Reliability Implications of Unbalanced Current Sharing

Electromigration (EM) induced wear-out dictates the lifetime of each component of the PDN. EM results in gradual mass transport in metal conductors along the direction of an applied electric field, which in turn may cause open or short circuits. The metal wires in the PDN are particularly vulnerable to EM as they experience uni-directional currents [94], and such constant stress reveals EM failures faster. EM grows with current density J.

Black's equation [95] captures the mean time to failure (MTTF) due to EM:

$$MTTF = AJ^{-n}exp(Ea/kT) \tag{2.21}$$
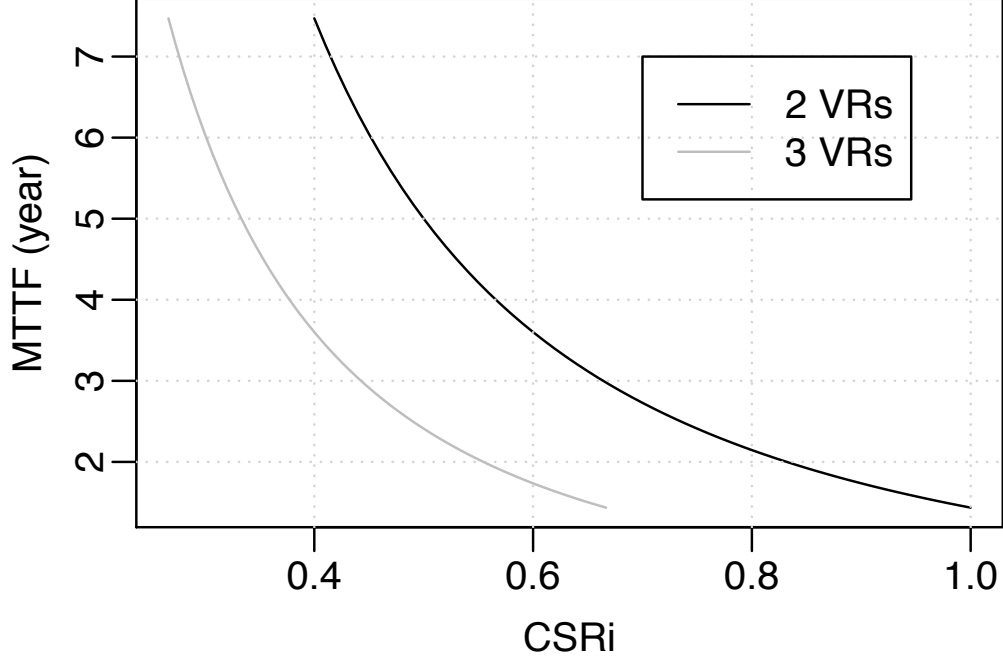
Figure 2.9: MTTF as a function of CSR_i.

where A is a constant that depends on the geometry, Ea is the EM activation energy, k is Boltzmann constant, n is a material-specific constant, and T is the temperature. Following [82], Black's equation can be adjusted to consider current crowding and Joule heating as

$$MTTF = A(cJ)^{-n}exp[Q/k(T+\Delta T)] \qquad (2.22)$$

where both Q and c are material-specific constants.

Consider N identical distributed on-chip VRs, each of which optimized for a load current of I_o/N, where I_o represents the total load current. Since J is directly related to CSR_i at a specific I_o, MTTF of the metal wire at the output of the ith regulator can be expressed in terms of CSR_i as

$$MTTF_i = A^{'}(cCSR_i)^{-n}exp[Q/k(T+\Delta T)] \qquad (2.23)$$

where $A^{'}$ is a constant that depends on the geometry and I_o.
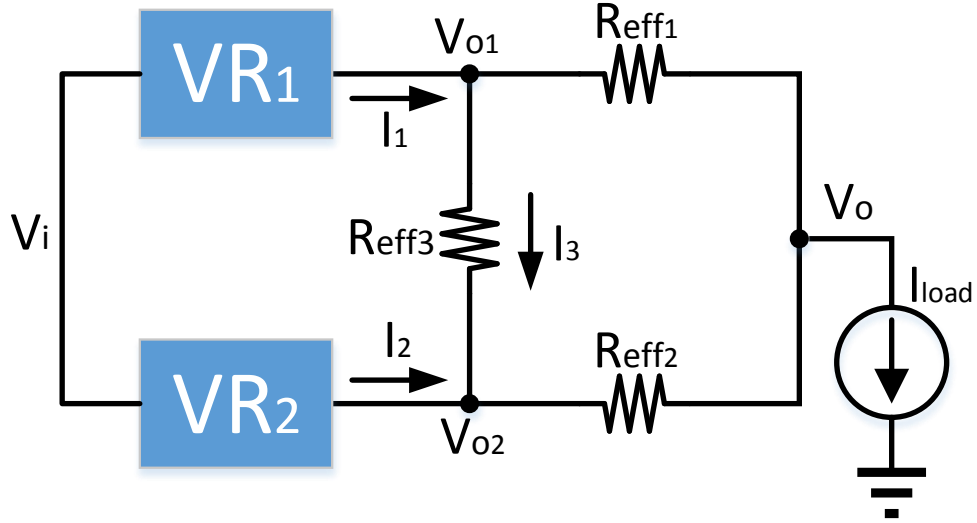
Figure 2.10: Simplified model of two identical distributed on-chip VRs with power grid effective resistances.

For the same example in [71], for two and three regulator cases with a total load current of 450mA and 675mA, respectively, Fig. 2.9 shows how $MTTF_i$ for the ith regulator changes due to unbalanced current sharing. Fig. 2.9 captures the impact of unbalanced current sharing on MTTF under EM per (2.23). We report how the MTTF varies as a function of CSR where $n = 1.8$, Q = 0.8eV, $c = 10$, and $\Delta T = 40°$C [96]. We observe that differences in CSR can result in notable differences in MTTF. The MTTF at $CSR = 0.5$ (0.33), which corresponds to perfect load balance, is 5 years at 65°C for the two (three) regulator case. For the two regulator case, both regulators would have this same MTTF=5 years at $CSR = 0.5$. If CSR assumes a higher value than 0.5 for one of the regulators, the MTTF value quickly decreases below 5 years. The other regulator's CSR in this case remains lower than 0.5, and hence induces an MTTF of more than 5 years. In this case, one of the regulators would fail much earlier than the other. Better load balance (*i.e.*, $CSR = 0.5$ for the two regulator case) mitigates this adverse effect on reliability. Fig. 2.9 reveals a similar trend for three VR case.
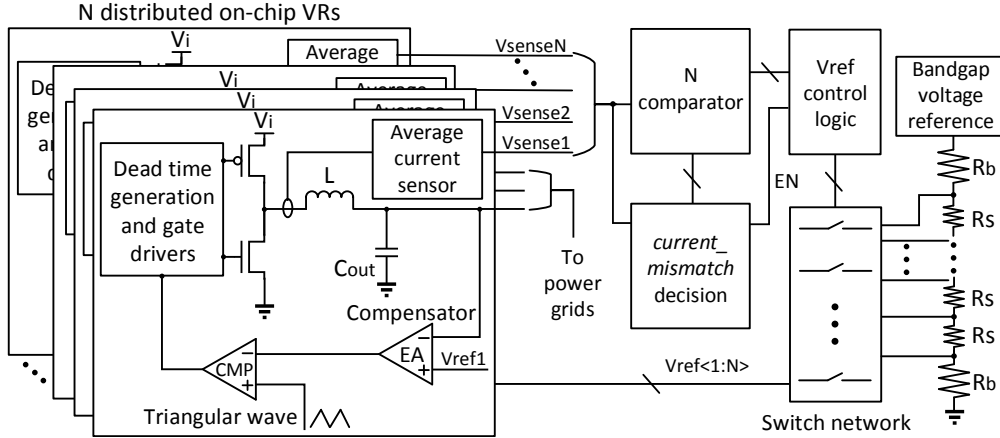
Figure 2.11: System level block diagram of the proposed V_{ref} control method and multi-level V_{ref} generator for N identical distributed on-chip VRs.

2.6 Adaptive Reference Voltage Control

The implications of unbalanced current sharing on power efficiency, stability, reliability and overall functionality of the chip are demonstrated above. Balanced current sharing is beneficial to maintain the overall PDN performance. An adaptive reference voltage control method designed specifically for distributed on-chip VRs is proposed to balance the current sharing. The proposed technique is scalable for different number of distributed on-chip VRs and can be used for different types of VRs. The control algorithm is explained and circuit implementation and simulations are presented to verify the effectiveness of the proposed techniques. Practical concerns are also addressed in this section.

2.6.1 Adaptive Reference Voltage Control Mechanism

Consider two identical distributed VRs connected to the same power grid. The simplified model is shown in Fig. 2.10 with the power grid effective resistance included between any two connection nodes within the grid. With a large number of VDD C4 pads, the input voltage of the VRs V_i can be considered ideal and constant. To perform a steady state analysis with multiple VRs, suppose $V_{o1} = V_{o2}$, then $I_3 = 0$, and R_{eff3} can be removed as open circuit. When $V_{o1} = V_{o2}$, to make $I_1 = I_2$ for balanced current sharing, R_{eff1} and R_{eff2} have to be equal. However, in practice, due to the location variations of the VRs with respect to the load, R_{eff1} and R_{eff2} can hardly be
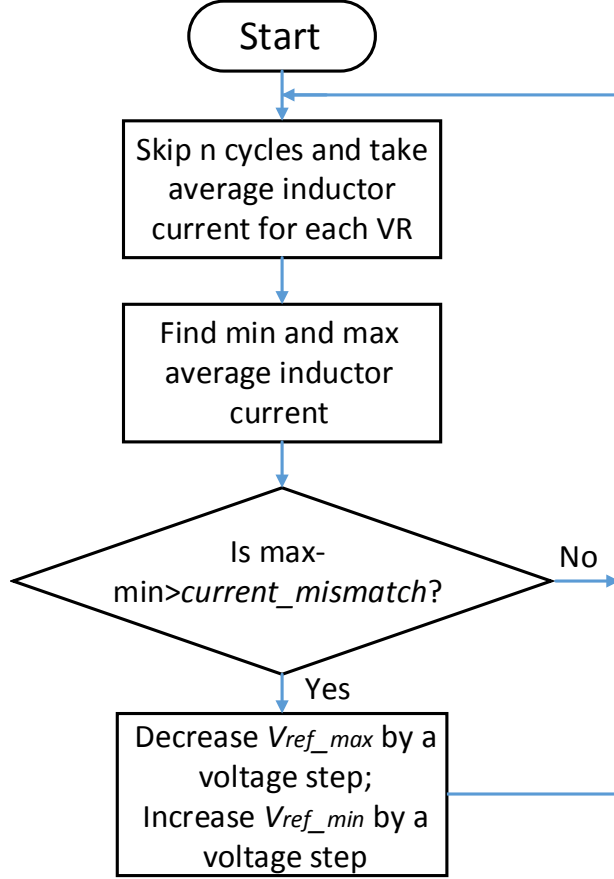
Figure 2.12: Flowchart of the proposed adaptive V_{ref} control algorithm.

equal, which means variations between V_{o1} and V_{o2} are unavoidable to make $I_1 = I_2$ for balanced current sharing. In fact, the effective resistances R_{eff1}, R_{eff2}, and R_{eff3} are very small, making the balanced current sharing possible with quite small variations of V_{o1} and V_{o2} with negligible effects on the regulated output voltage V_o.

Based on the above analyses, an adaptive reference voltage V_{ref} control mechanism that is tailored specifically for distributed on-chip VRs is proposed. A system level block diagram of the proposed adaptive V_{ref} control method is illustrated in Fig. 2.11 and the V_{ref} control algorithm is presented in Fig. 2.12 for N identical distributed on-chip VRs. The proposed adaptive V_{ref} control block consists of an average current sensor within each VR, two comparators with N inputs for each (N comparator) [97] to determine the maximum and minimum currents, a $current\_mismatch$ decision block, and a V_{ref} control logic. For each iteration, the average current value of each VR for that

cycle is obtained through the average current sensor and represented by respective output voltage V_{sense_i} ($i = 1, ..., N$). The maximum and minimum value of V_{sense_i} ($i = 1, ..., N$) are decided by the N comparator [97]. The difference between the maximum and minimum current is compared to a *current_mismatch* value by the *current_mismatch* decision block. The processed outputs of the N comparator and *current_mismatch* decision block serve as the control signals for the V_{ref} control logic for multi-level V_{ref} generation through the switch network and resistor string. Mismatch between the maximum and minimum average inductor current indicates unbalanced current sharing. If the mismatch is larger than a certain threshold *current_mismatch*, the proposed V_{ref} control algorithm is triggered and the corresponding reference voltages are adjusted. *current_mismatch* value is added as an option to adjust the desired accuracy for the current matching among the VRs and to eliminate constant toggling during steady state where all the VR output currents are close to each other. If the optimal load current (I_{o_opt} in (2.5)) a single VR can supply is in the range of several hundred mA, a few mA of the threshold value can be considered as balanced current. A threshold value of 30 mA is used in the simulations. A too small threshold value can lead to toggling reference voltages at steady state.

By increasing (decreasing) V_{ref} of an individual on-chip VR, the output current supplied by that VR will increase (decrease). V_{ref_max} and V_{ref_min} in Fig. 2.12 denote the reference voltages for the on-chip VRs with the maximum and minimum average inductor current, respectively. Once the difference between the maximum and minimum average inductor current values is greater than *current_mismatch*, V_{ref_max} is decreased by a voltage step to decrease the output current supplied by the VR which provides the maximum output current. V_{ref_min} is increased by a voltage step to increase the output current supplied by the VR which provides the minimum output current. The reference voltages of other VRs remain unchanged.

Note that the V_{ref} control loop waits n clock cycles before changing the V_{ref} again. This is done in order to allow the VR's voltage regulation feedback loop to respond before any changes made to the V_{ref} in the next step. Making the reference control loop slower than the VR's voltage regulation feedback loop improves the stability of the overall system.
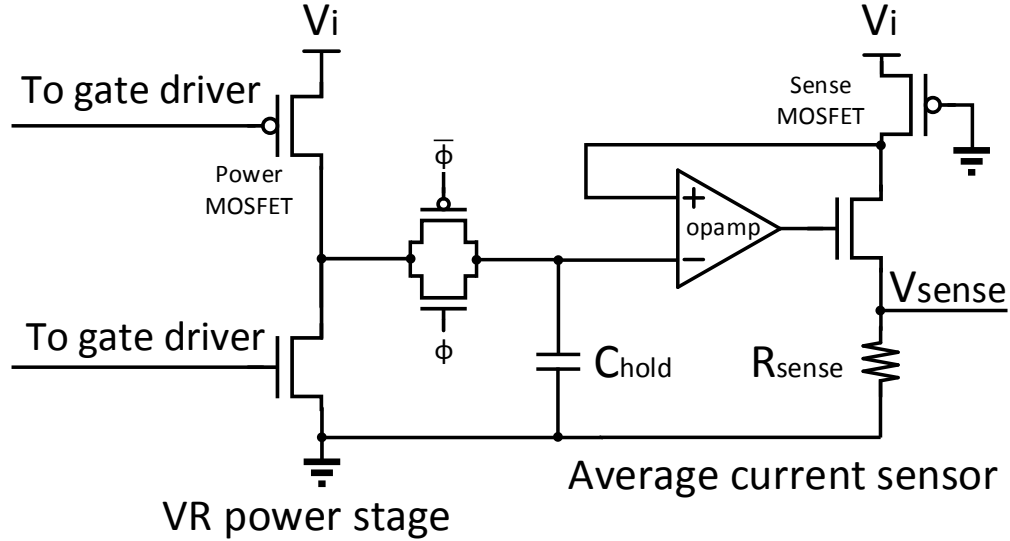
Figure 2.13: Schematic of the average current sensor.

As compared with [73], the proposed method does not rely on equalizing duty cycles to balance the current sharing, and thus can be applied to most regulator types that need a reference voltage to operate. Furthermore, as the reference voltage of each VR is adjusted individually with respect to an initial reference voltage, the power noise on the local power grids is less affected by localized load fluctuations.

2.6.2 Adaptive Reference Voltage Control Implementation

Circuit level implementation of the proposed adaptive V_{ref} control method is analyzed in this section. Although buck regulator is adopted for demonstration, the proposed V_{ref} control method can be applied to other regulator types by adopting an appropriate current sensor for that regulator type, as the proposed method is a general way of modulating V_{ref} to balance the current.

2.6.2.1 Average Current Sensor

The schematic of the average current sensor [98] is shown in Fig. 2.13. When the sampling clock ϕ becomes high, the drain voltages of the power MOSFET and the sense MOSFET are equalized by the operational amplifier. The inductor current from the power MOSFET is mirrored
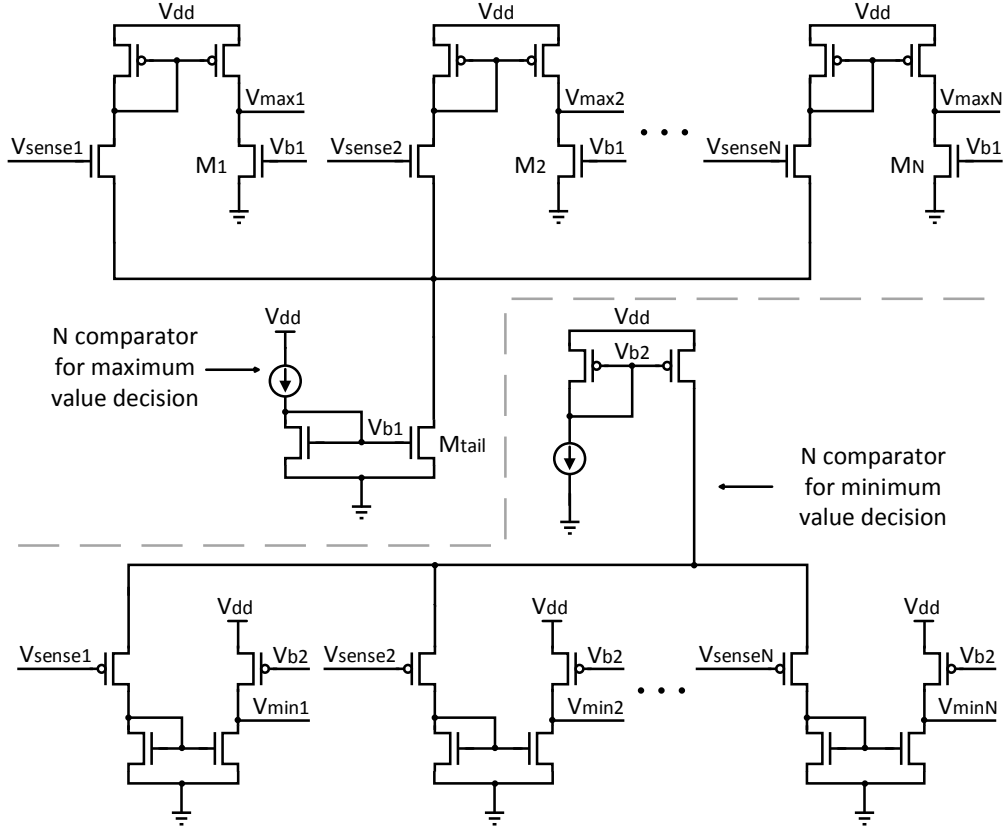
Figure 2.14: Schematic of the analog N comparator for maximum and minimum current decision.

to the sense MOSFET and a corresponding voltage V_{sense} that is proportional to the inductor current is generated as output. V_{sense} is maintained when ϕ becomes low. By replacing the ramp signal in Fig. 2.5 with a symmetrical triangular waveform shown in Fig. 2.11, a clock signal ϕ' can be generated to sample the instant inductor current value in the middle of the inductor energizing or de-energizing phase, which corresponds to the average inductor current value [98]. As n clock cycles need to be skipped before taking the next sample for average inductor current, the frequency f_ϕ of the actual sampling clock signal ϕ needs to be $f_{\phi'}/(n+1)$.

2.6.2.2 N Comparator

The schematic of the N comparator [97] for maximum and minimum current decision is shown in Fig. 2.14. V_{sense_i} $(i = 1, ..., N)$ from the output of the average current sensor serves as the input of the N comparator. For the N comparator for maximum current decision, the tail current

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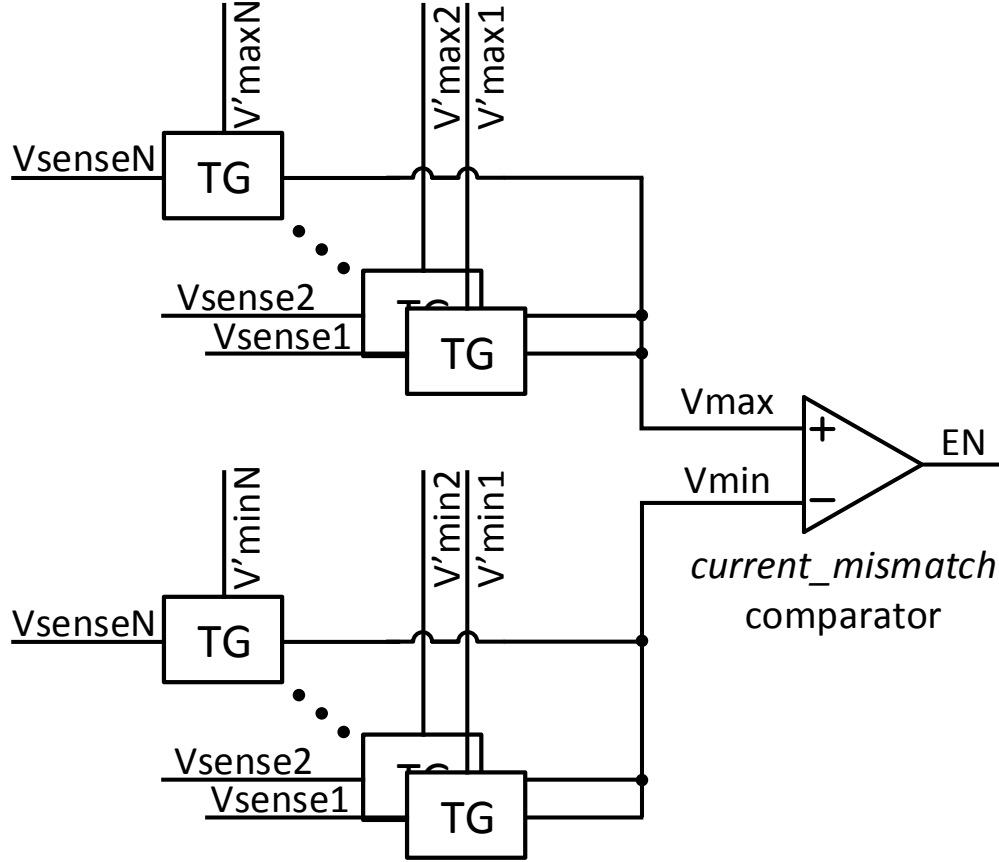
Figure 2.15: Schematic of the *current_mismatch* decision block.

provided by transistor M_{tail} is divided into each branch equally when the same voltage is given to all inputs. M_i $(i = 1, ..., N)$ devices are biased and sized appropriately $((\frac{W}{L})_{M_{tail}} = N(\frac{W}{L})_{M_i})$ to reflect this distribution. The voltage input V_{sense_i} determines the portion of the tail current that passes through each branch. Since the sum of the currents from all the branches must be equal to the tail current provided by the M_{tail} device, the branch with the highest input voltage gets the largest portion of the tail current. The branch currents are then mirrored and a high resistance output node is formed using the M_i $(i = 1, ..., N)$ devices. Since M_i $(i = 1, ..., N)$ devices are biased for $1/N$ of the tail current, the output voltage becomes logic high when a branch gets more than $1/N$ of the tail current, which is true for the branch with the highest voltage, and logic low if a branch gets less than $1/N$ of the tail current. The high resistance node provides high gain at the output but further cascading may be needed to provide rail to rail outputs. Less than 1mV input

Figure 2.16: Simulation results with and without the proposed adaptive V_{ref} control scheme for two identical distributed on-chip VRs. (a) Inductor currents before and after the proposed V_{ref} control is applied. (b) A zoomed view of balanced current sharing showing the effectiveness of the proposed V_{ref} control method. (c) A zoomed view of unbalanced current sharing without the proposed V_{ref} control. (d) V_{refs} signal change showing the operation of the proposed V_{ref} control method.

voltage difference can be distinguished by cascading three stages in the simulations. In the case where the input voltages are very close to each other, this comparator may give incorrect outputs where more than one current is minimum or maximum. Considering this case, the outputs of the N comparator V_{max_i} and V_{min_i} $(i = 1, ..., N)$ are processed by a digital logic to generate V'_{max_i} and V'_{min_i} $(i = 1, ..., N)$ to control the *current_mismatch* decision block and V_{ref} control logic shown in Fig. 2.11. If there are more than one maximum or minimum current, the digital logic simply selects the VR with smaller i as the one that supplies the maximum or minimum current. The N comparator for minimum current decision can be implemented as a complement of the N comparator for maximum current decision shown in Fig. 2.14.
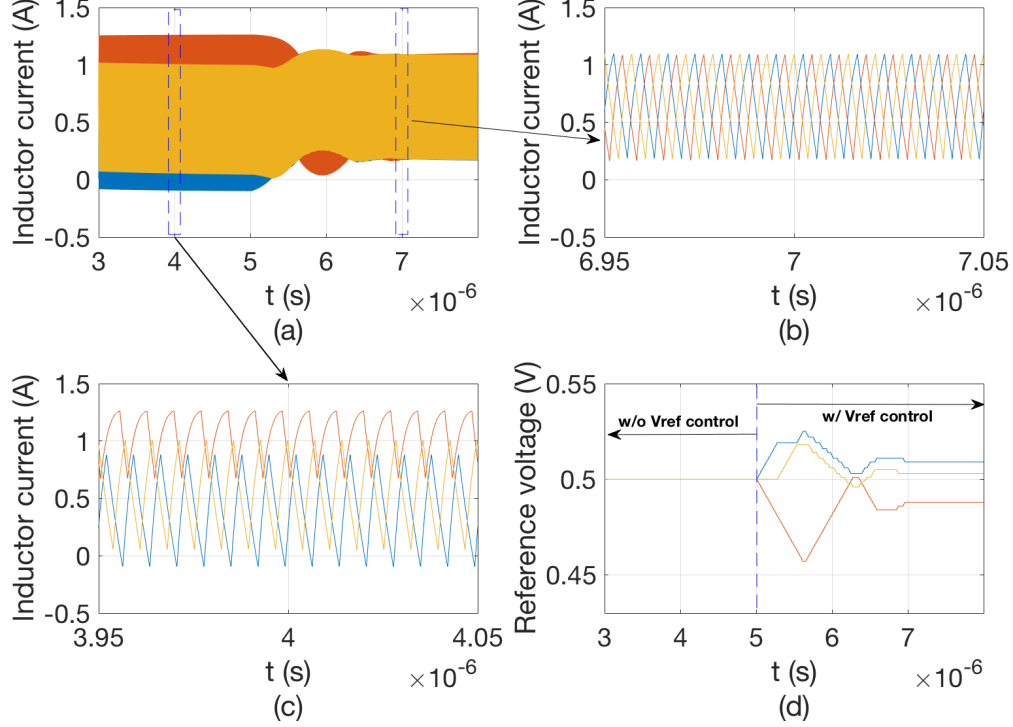
Figure 2.17: Simulation results with and without the proposed adaptive V_{ref} control scheme for three identical distributed on-chip VRs. (a) Inductor currents before and after the proposed V_{ref} control is applied. (b) A zoomed view of balanced current sharing showing the effectiveness of the proposed V_{ref} control method. (c) A zoomed view of unbalanced current sharing without the proposed V_{ref} control. (d) V_{refs} signal change showing the operation of the proposed V_{ref} control method.

2.6.2.3 Current Mismatch Decision

The schematic of the $current\_mismatch$ decision block is shown in Fig. 2.15. The processed outputs of the N comparator V'_{max_i} and V'_{min_i} $(i = 1, ..., N)$ are fed to $2N$ transmission gates (TG) as selection signals for the maximum and minimum value of V_{sense_i} $(i = 1, ..., N)$. The maximum and minimum value of V_{sense_i} serve as the inputs of the $current\_mismatch$ comparator as, respectively, V_{max} and V_{min} to generate the enable signal EN for subsequent V_{ref} control logic. An intentional input transistor size mismatch is introduced for the $current\_mismatch$ comparator with larger transistor size connected to V_{min} as compared to that connected to V_{max} to achieve the offset voltage V_{offset} that corresponds to the $current\_mismatch$ value. Only when $V_{max} - V_{min} > V_{offset}$ will the EN signal be active. As $current\_mismatch$ does not need to be accurate as long as it is

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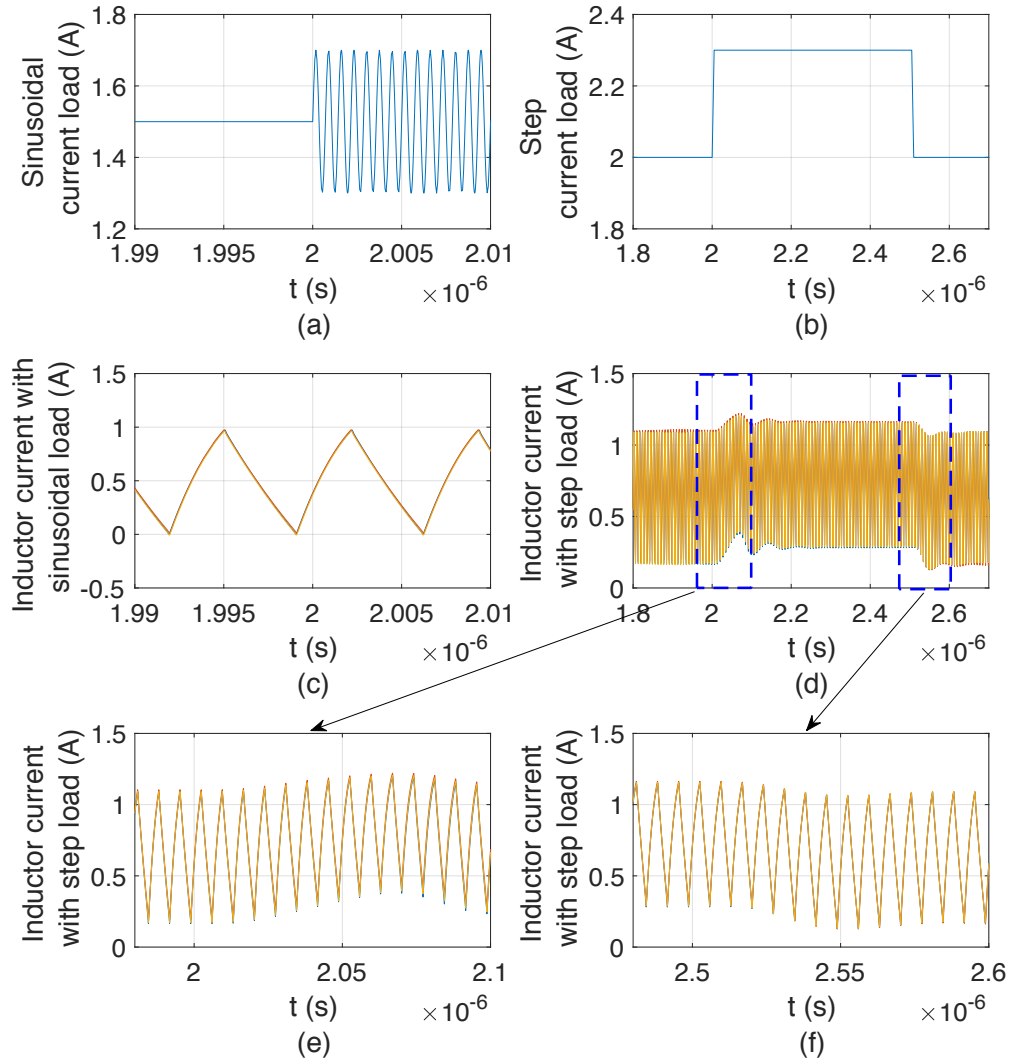
Figure 2.18: Simulation results with sinusoidal and step load current for three identical distributed on-chip VRs. (a) Sinusoidal load current applied at $2\mu s$. (b) Step load current waveform applied. (c) Balanced inductor currents under sinusoidal current load. (d) Balanced inductor currents under step current load. (e) A zoomed view of balanced inductor currents near the rising edge of the step current load. (f) A zoomed view of balanced inductor currents near the falling edge of the step current load.

larger than $\Delta(\Delta I)$, as will be discussed next, practical circuit implementations considering process variations have negligible impacts on the circuit function.
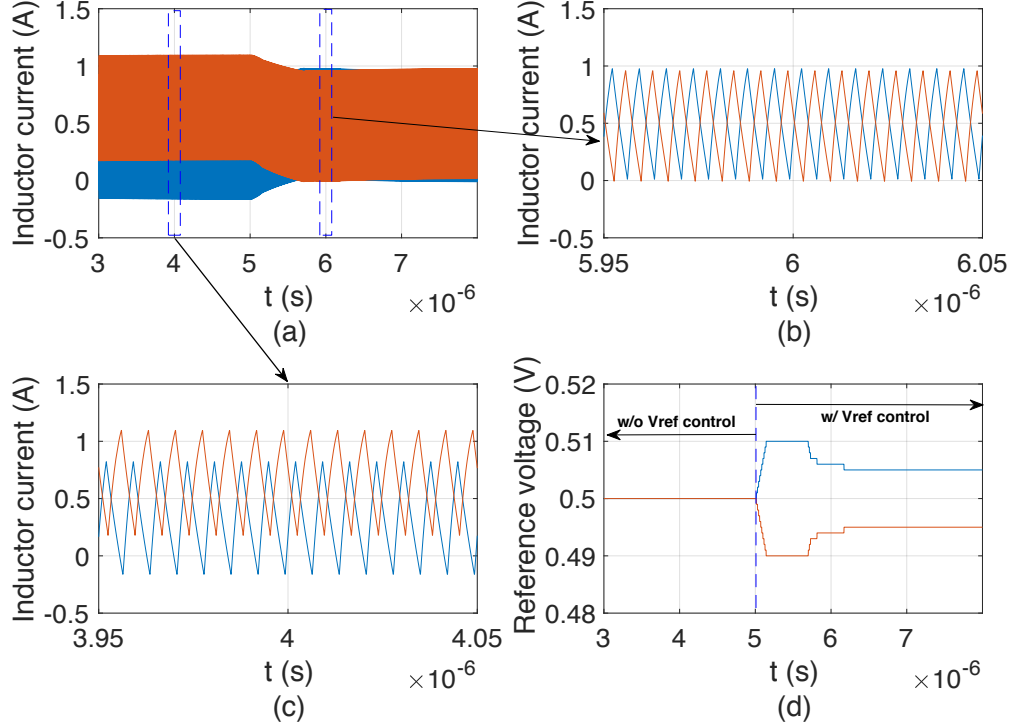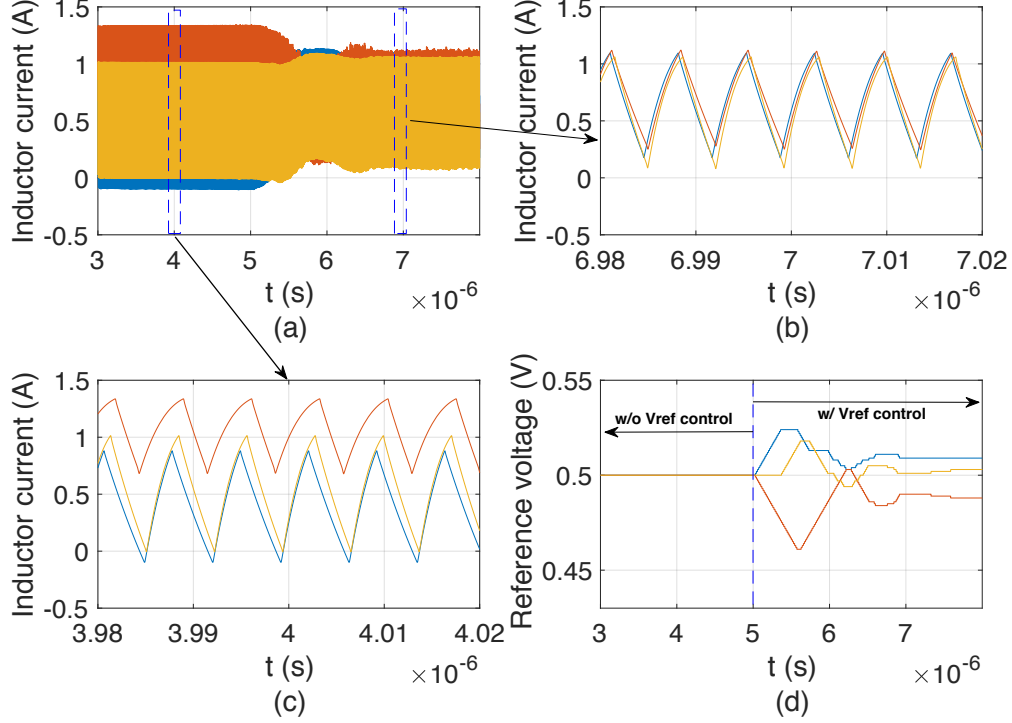
Figure 2.19: Simulation results with and without the proposed adaptive V_{ref} control scheme for three distributed on-chip VRs under distribution wire and VR mismatches. (a) Inductor currents before and after the proposed V_{ref} control is applied. (b) A zoomed view of balanced current sharing showing the effectiveness of the proposed V_{ref} control method under distribution wire and VR mismatches. (c) A zoomed view of unbalanced current sharing without the proposed V_{ref} control. (d) V_{refs} signal change showing the operation of the proposed V_{ref} control method.

2.6.2.4 Multi-Level Reference Voltage Generation

The proposed multi-level V_{ref} generator is composed of a V_{ref} control logic, a bandgap voltage reference, and a simple resistor string DAC as shown in Fig. 2.11. There are two resistors with large resistance R_b at the top and bottom of the string and a few resistors with smaller resistance R_s connected in the middle to generate the desired V_{refs}. V'_{max_i}, V'_{min_i} $(i = 1, ..., N)$, EN and a clock signal, which is a delayed version of ϕ are given to the V_{ref} control logic. This logic determines how the reference voltages for each VR should behave according to the algorithm in Fig. 2.12. The logic can be implemented completely in verilog and synthesized.

The reference voltage generation requires analog implementation, and this implementation can be a resistor string DAC. The voltage step level that can achieve the desired *current_mismatch*

value is the LSB of the DAC. The goal of the adaptive V_{ref} control method is to achieve $\Delta I = I_{max} - I_{min} < current\_mismatch$. If without V_{ref} control, $\Delta I = \Delta I_0$ and one voltage step change can introduce $\Delta(\Delta I)$ of ΔI change, the number of bits for the DAC (N_{DAC}) that is fine enough for balanced current sharing can be estimated as $N_{DAC} > \log_2(\Delta I_0/\Delta(\Delta I))$. A 7-bit DAC is used to achieve a 30mA $current\_mismatch$ value with a voltage step of 1mV in the simulations. In the case where large number of VRs and high resolution DAC are needed, a charge pump can be utilized for each phase after the V_{ref} control logic for DAC implementation to avoid possible routing problem induced by the resistor string.

2.6.3   Simulation Verifications

To demonstrate the effectiveness of the proposed control method, two and three identical distributed on-chip VR cases are simulated. The power grid parameters are provided in Section 2.7. Simulation results with constant DC load current are shown in Fig. 2.16 and Fig. 2.17, respectively, for the two and three VR cases. In the simulations, ideal $V_{ref} = 0.5V$ is used to realize 1V output voltage. A V_{ref} step of 1mV is used in the simulations. The proposed adaptive V_{ref} control method begins to operate at $5\mu s$. As can be seen from Fig. 2.16 (a)(c) and Fig. 2.17 (a)(c), for stand-alone VRs operating without proper V_{ref} control, large inductor current variations occur among those VRs. After the proposed V_{ref} control mechanism is applied, seen from Fig. 2.16 (a), (b) and Fig. 2.17 (a), (b), the unbalanced current converges quickly to the balanced one for both two and three VR cases. Also, as can be seen from Fig. 2.16 (d) and Fig. 2.17 (d), only small variations of reference voltage lead to quite good inductor current match and meanwhile the proper operation of the VRs is guaranteed. Simulation results with a fast changing sinusoidal and a step current load are shown in Fig. 2.18. In the simulations, the frequency of the sinusoidal wave is ten times of the VR switching frequency. As can be seen from Fig. 2.18, the proposed V_{ref} control method works well under changing load currents.

Table 2.1: Technology and Architecture Parameters

Technology Parameters
Technology node: 22nm, Frequency: 4.0GHz TDP: 150W, Area: $441mm^2$, Vdd: 1.03V
Architecture Parameters
cores: 8 issue width: 8 64 architectured FRF, 32 architectured IRF
L1-I cache: 32KB, 8-way, 64B, LRU, 1-cycle hit L1-D cache: 64KB, 8-way, 64B, LRU, 1-cycle hit L2 cache: 512KB, 8-way, 128B, LRU, 11-cycle hit L3 cache: 64MB, 8-way, 128B, LRU, 30-cycle hit

2.6.4 Practical Concerns

Considering the practical implementations of the V_{ref} control method, there are parasitic impedances between the generated reference voltage and the corresponding error amplifier introduced by the distribution wires. The impedance of the distribution wires among different VRs can be different. Also, there can be VR components and control loop mismatches. Considering these effects, simulations are performed by introducing wire resistances and capacitances as well as VR components and loop delay mismatches to justify the effectiveness of the proposed method. 1mm distribution wire is assumed in the simulations. Based on IBM 130nm process, the parasitic resistance and capacitance are, respectively, around 70Ω and 230fF. A 10% mismatch is introduced among each VR regarding distribution wire impedance, L, C, R_{DCR}, R_{ESR}, $Q1$, $Q2$ size. $5ns$ control loop delay difference is introduced among each phase. The simulation results for three phases are shown in Fig. 2.19. As can be seen from the simulation results, the proposed method is immune to these mismatches.

(a) core   (b) chip
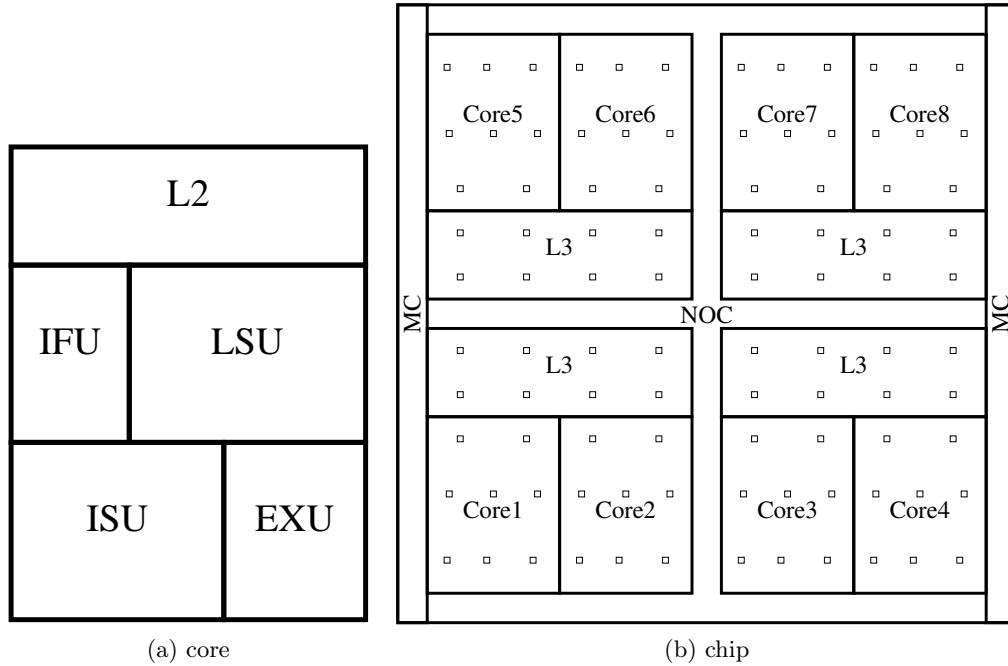
Figure 2.20: Chiplet simplified floorplan.

2.7 Case Study: IBM POWER8 Like Microprocessor

2.7.1 Benchmarks

All the benchmarks used in the simulations are from SPLASH2x [99]. The benchmarks experimented represent typical application domains and features. Eight threads are involved in the simulations and analysis is limited to the region-of-interest of the benchmarks.

2.7.2 Architecture

An IBM POWER8-like [64] processor is modeled to quantitatively characterize unbalanced current sharing effects. The technology and architecture parameters of the processor are summarized in Table 2.1. The schematic of a core is shown in Fig. 2.20a, which contains a private L2, an instruction scheduling unit (ISU), an execution unit (EXU), a load store unit (LSU), and an instruction fetch unit (IFU). L1 data cache is a part of LSU, while L1 instruction cache resides
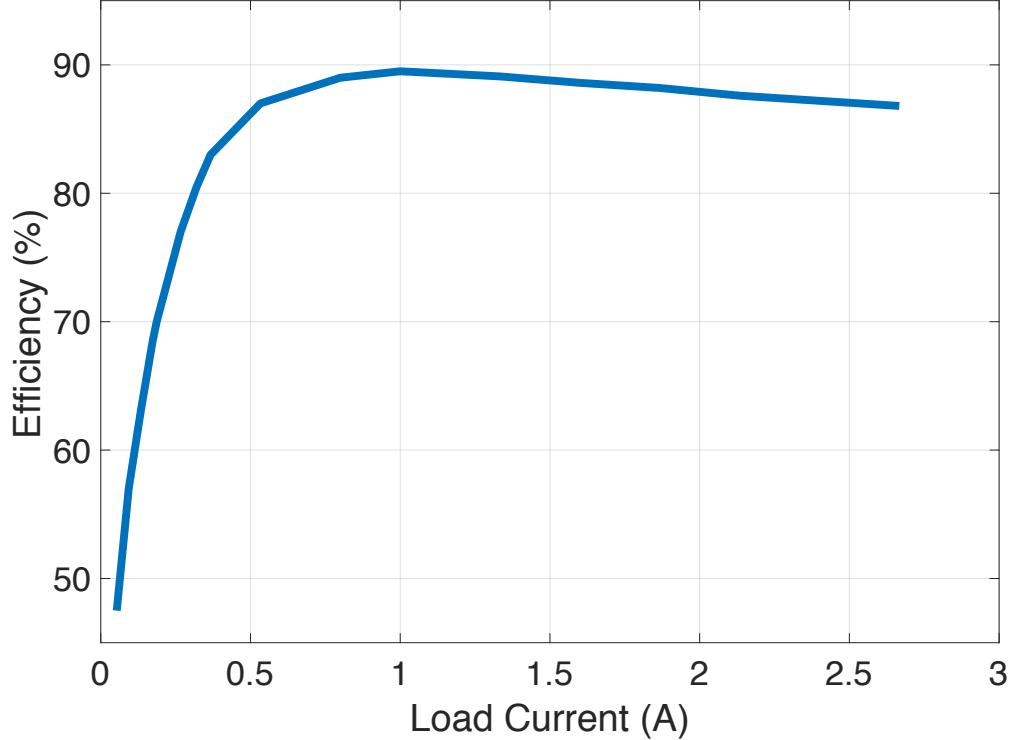
Figure 2.21: Calibrated efficiency curve for the on-chip voltage regulator.

inside IFU. Fig. 2.20b illustrates the whole chip floor plan, which contains 8 cores, 96 identical on-chip regulators, shown as little squares, network-on-chip (NOC), and memory controller (MC).

2.7.3   Simulation Framework

Dynamic power traces are collected by integrating MR2 [100] version of McPAT [101] into SNIPER6.0 [102] micro-architectural simulator. Then, we calculate the static power of each unit based on its temperature and area. We use the equation from [103] to capture temperature-dependence of static power. The static power of the whole chip is calibrated in a way that it takes less than 30% of the total chip power at 80°C. Hotspot6.0 [104] is used to find the transient temperature across the chip. Transient temperature (output of Hotspot) is used to calculate the static power (input to Hotspot). So, we iteratively run Hotspot and update the static power numbers until they converge. Default parameters of Hotspot are used. VoltSpot is deployed to capture the current distribution among VRs at different locations and the method from [82] is followed to generate cycle-accurate power traces. One sample contains 2K cycles and 200 samples are obtained
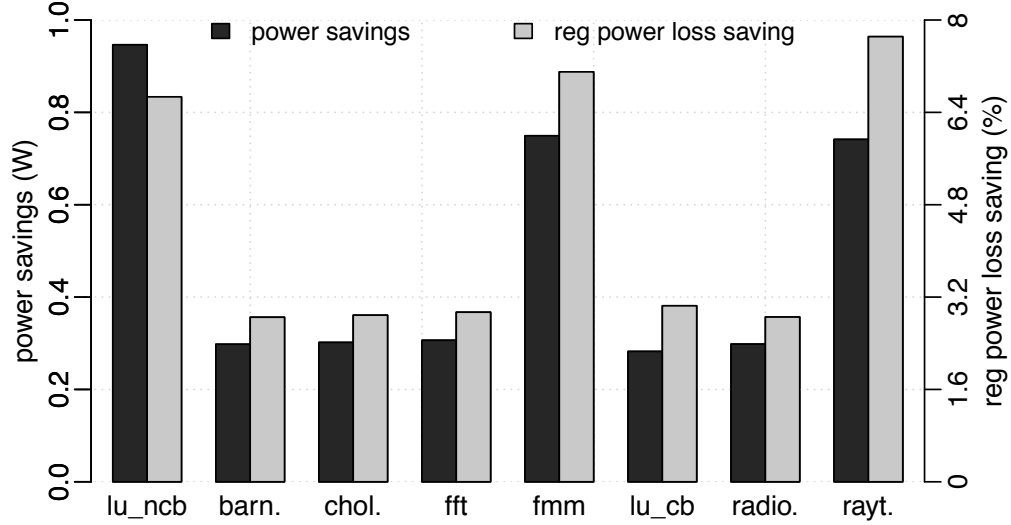
Figure 2.22: Power saving and regulator power loss saving with balanced current sharing for different applications.

with equal distance for each application. The first 1K cycles are used for warm-up and the rest for analysis. 4 clock cycles are used as the power trace sampling interval.

2.7.4 Power Grid and Voltage Regulator Properties

In VoltSpot configurations, the on-chip power grid is designed as a resistive mesh using similar metal width, pitch, and thickness parameters in [84] for the global, intermediate, and local PDN layers. The unit power grid resistance is around $8m\Omega$ and the total power grid size is 345 by 345. The effective resistance between any two nodes can be estimated using the equations in [30, 83].

LDOs used in IBM POWER8 microprocessor and FIVRs used in Intel Haswell microprocessor are two state-of-the-art on-chip power delivery solutions. It is demonstrated in [78] that FIVR-based power delivery scheme is more advantageous with large number of cores due to high efficiency over a wide conversion ratio. The gaining impetus and benefits of distributed on-chip voltage regulation together with the advantages of FIVR motivate us to investigate distributed buck regulators in the simulation setups.

96 identical on-chip VRs, with the area of each as $0.04mm^2$, are used in the simulations to distribute across the chip as shown in Fig. 2.20b. The optimal placement of LDOs is first investigated

in [105] to meet the IR-drop constraint. To avoid any adversely biased analysis in our simulations, we mimic the algorithm proposed in [106] where a voltage-noise-minimizing technique is proposed to determine the locations of the C4 pads across several benchmarks. We use this algorithm to determine the optimal locations of the on-chip VRs that would minimize the voltage-noise. Since the resulting maximum voltage noise only decreases by less than 0.4% with the optimal placement as compared to the uniform distribution, we adopt the uniform placement of the VRs to simplify the analysis. These on-chip regulators are calibrated to match the conversion efficiency of FIVR design in Intel's Haswell processor [62] as it is one of the most efficient regulators in industry. Efficiency curves in [62] are picked for calibration and each VR provides around 1A load current with the optimum efficiency of about 90%. The calibrated efficiency curve is shown in Fig. 2.21. The on-chip VR is modeled as an ideal supply voltage in series with a RLC network in VoltSpot [82] simulations. Simpler RL and RC based models have previously been used, respectively, in [2, 107] and in [108] to model VRs. The proposed adaptive V_{ref} control method can be applied to balance the current sharing.

Simulation results showing the power saving and regulator power loss saving with balanced current sharing for different applications are shown in Fig. 2.22. Power saving up to 1W and VR power loss saving up to 8% are observed. Note that balancing the current may lead to extra power losses on the power-grid resistors. The total gained power saving is due to the fact that the power saving induced by balanced current sharing can be much larger than the extra power loss consumed on the power grid resistors. For a general case of N distributed VRs, a total load current NI_{o_opt} with any CSR_i $(i = 1, ..., N)$ for the ith VR, when CSR_i varies further from the balanced current sharing point, balanced current sharing may introduce more loss on the power-grid parasitic resistors, however, balanced current sharing induced power saving also increases as can be seen from Fig. 2.6 and (2.9). With large number of VRs deployed, distributed load currents are supplied by adjacent VRs, which effectively reduces the distance VR output currents travel to balance others. Furthermore, effective resistance between two nodes on the power grid does not increase linearly with distance [30, 83]. Even with quite large distance, effective resistance can be only a few times of the unit power-grid resistance. All these factors contribute to the power savings

seen from Fig. 2.22. More importantly, with balanced current sharing, VR malfunctions can be avoided and stability and reliability are enhanced.

2.8 Conclusion

Efficiency, stability, and reliability implications of unbalanced current sharing among distributed on-chip voltage regulators are investigated in this chapter both theoretically and through extensive simulations. A current balancing scheme that can be applied to most regulator types is proposed in this work. A simple relationship between the individual voltage regulator output current and its corresponding V_{ref} is identified for balanced current sharing. And an adaptive V_{ref} control method based on the relationship is proposed. The proposed method generates and modulates the V_{ref} for each regulator to balance the output current. The implementation of the method is analyzed and simulations are presented to verify the effectiveness. Regulator power loss saving up to 8%, enhanced system stability, and several years of MTTF improvement are verified through practical case studies.

CHAPTER 3:

AGING EFFECTS ON THE TRANSIENT PERFORMANCE DEGRADATION OF

ON-CHIP VOLTAGE REGULATORS

3.1 Introduction

With ubiquitous applications of on-chip voltage regulation [2] within modern microprocessors, Internet of Things (IoT), wireless energy harvesting, and applications such as aerospace engineering, the reliable operation and lifetime of on-chip voltage regulators have become one of the most significant and challenging design considerations.[1] Within those applications, large variations in the load current, voltage, and temperature can occur. These variations may speed up the aging process of the devices under stress and further deteriorate the performance and lifetime of on-chip voltage regulators. As those regulators are already deployed in the field, replacement of them can be costly or even impossible. The conflicting need of harsh environment applications and highly reliable designs necessitates reliability evaluations at design stage as well as reliability enhancement techniques.

The major transistor aging mechanisms include bias temperature instability (BTI), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and electromigration (EM), among which BTI is the dominant reliability concern for nanometer integrated circuits design [2-4]. BTI can induce threshold voltage increase and consequent circuit level performance degradation. Positive BTI (PBTI) induces aging of nMOS transistors while negative BTI (NBTI) causes aging of

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[1]This chapter was published in IEEE Design, Automation and Test in Europe Conference and Exhibition, Dresden, Germany, 2018, pp. 803-808 "Mitigation of NBTI Induced Performance Degradation in On-Chip Digital LDOs" and in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Early Access, DOI (identifier) 10.1109/TVLSI.2018.2871381 "Exploiting Algorithmic Noise Tolerance for Scalable On-Chip Voltage Regulation". Permissions are included in Appendix A.

pMOS transistors [109]. The impact of BTI aging mechanism is a strong function of temperature, electrical stress, and time.

On the other hand, as an essential part of large scale integrated circuits, on-chip voltage regulators need to be active most of the time to provide the required power to the load circuit. The load current and temperature can vary a lot especially for microprocessor applications [31]. All of these variations partially contribute to different aging mechanisms of on-chip voltage regulators, which should be considered to avoid overdesign for a targeted lifetime.

Several studies have been performed regarding the reliability issues in nanometer CMOS designs [6-8]. There is, however, quite limited amount of work on the reliability of on-chip voltage regulators. Device aging on the immunity level of electro-magnetic interference (EMI) for low-dropout regulators (LDO) is characterized in [110]. A method of distributing the aging stress by rotating the phase to shed at light load is proposed in [111] to enhance the light load efficiency for multiphase buck converters. The reliability of metal wires connected to on-chip voltage regulators is investigated in [6]. Nonetheless, quantitative analysis of aging effects on on-chip voltage regulators considering load current characteristics and temperature variations as well as efficient reliability enhancement techniques under arbitrary load conditions have not yet been investigated.

As compared to other voltage regulator types, the emerging digital LDO (DLDO) has gained impetus due to the design simplicity, easiness for integration, high power density, and fast response [63, 112]. DLDOs have demonstrated major advantages in modern processors including the recent IBM POWER8 processor [64]. More importantly, as compared to the analog LDOs, DLDO can provide certain advantages for low-power and low-voltage IoT applications due to its capability for low supply voltage operations [113]. However, as pMOS is used as the power transistor for DLDOs, NBTI induced degradations largely affect important performance metrics such as the maximum output current capability I_{max}, load response time T_R, and magnitude of the droop ΔV as defined in [73]. It is therefore imperative to investigate aging mitigation techniques for DLDOs to achieve reliable operation of critical systems.

The main contributions of this chapter are threefold. First, NBTI induced threshold voltage V_{th} degradations are theoretically demonstrated that deteriorate DLDO performance metrics

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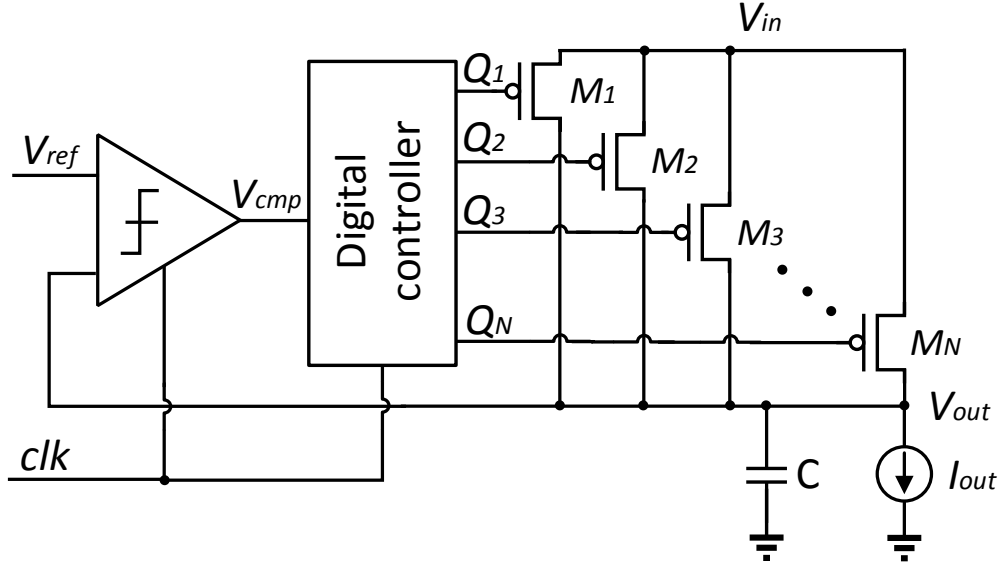
Figure 3.1: Schematic of conventional DLDO.

including I_{max}, T_R, and ΔV, making NBTI-aware DLDO designs necessary. Second, a novel uni-directional shift register (uDSR) is proposed to mitigate the NBTI induced DLDO performance degradation under arbitrary load conditions without degrading the performance. Third, possible mitigation strategies of DLDO performance degradation using the proposed technique are evaluated and reliability-aware design considerations are explored within practical applications.

The rest of this chapter is organized as follows. Background information regarding conventional DLDO regulator and NBTI is introduced in Section 3.2. NBTI induced DLDO performance degradation including I_{max}, T_R, and ΔV is demonstrated theoretically in Section 3.3. The proposed uDSR based NBTI-aware DLDO is described in Section 3.4. Evaluation of the benefits of the proposed NBTI-aware DLDO through simulation of an IBM POWER8 like processor is provided in Section 3.5. Concluding remarks are offered in Section 3.6.

3.2   Background

3.2.1   Conventional DLDO Regulator

The schematic of a conventional DLDO [63] is shown in Fig. 3.1. DLDO is composed of N parallel pMOS transistors M_i $(i = 1, ..., N)$ connected between the input voltage V_{in} and

(a)

Q₁	Q₂	Q₃	Q₄	Q₅	Q₆	• • •	• • •	Q_{N-1}	Q_N
(1) Initialize: all M_i turned off									
1	1	1	1	1	1	• • •	• • •	1	1
(2) Step k									
0	0	0	0	1	1	• • •	• • •	1	1
(3-a) Step k+1 if V_cmp=H: Shift right ➡									
0	0	0	0	0	1	• • •	• • •	1	1
(3-b) Step k+1 if V_cmp=L: Shift left ⬅									
0	0	0	1	1	1	• • •	• • •	1	1
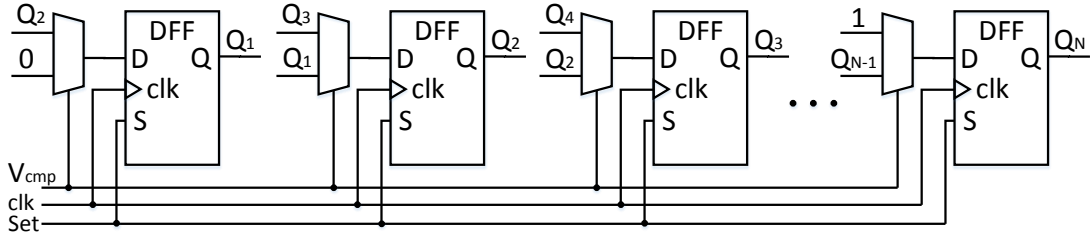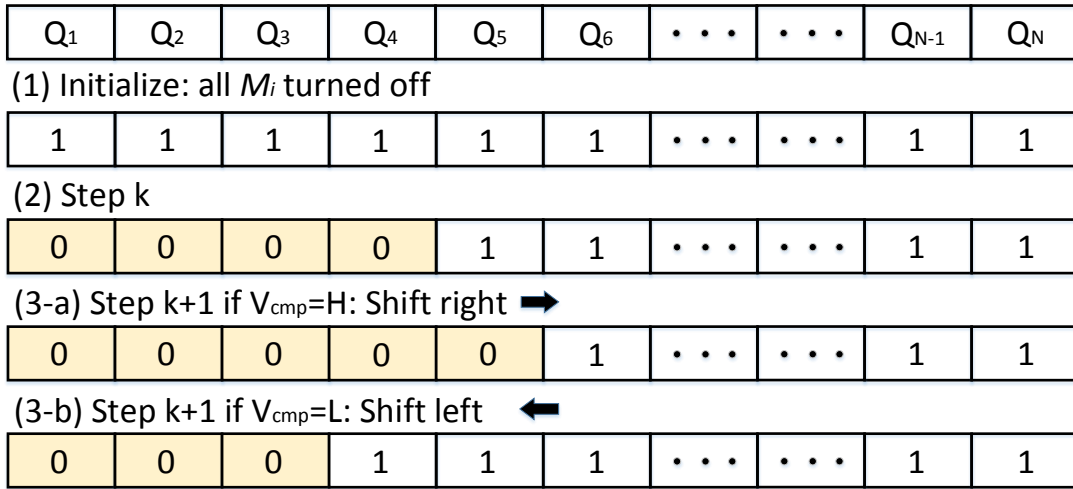
(b)

Figure 3.2: Digital controller for conventional DLDO. (a) Bi-directional shift register. (b) Operation of bi-directional shift register.

output voltage V_{out}, and feedback control loop implemented with a clocked comparator and digital controller. The value of V_{out} and reference voltage V_{ref} are compared through the comparator at the rising edge of the clock signal clk. More (less) number of M_i is turned on through the digital controller output signals Q_i $(i = 1, ..., N)$ if $V_{out} < V_{ref}$, $V_{cmp} = H$ ($V_{out} > V_{ref}$, $V_{cmp} = L$). A bi-directional shift register (bDSR), as shown in Fig. 3.2a, is conventionally implemented for the digital controller to turn on (off) power transistors M_1 to M_m (M_{m+1} to M_N) with the value of m decided by the load current I_{out}. At a certain step $k+1$, M_{m+1} (M_m) is turned on (off) if $V_{cmp} = H$ ($V_{cmp} = L$) and bDSR shifts right (left) as demonstrated in Fig. 3.2b.

DLDO needs to able to supply the maximum possible load current I_{max}. It is, however, demonstrated that, within most practical applications, including but not limited to smart phone [111] and chip multiprocessors [114], less than the average power is consumed most of the time. The application environment of DLDO together with the conventional activation scheme of M_i leads to the heavy use of M_1 to M_m and less or even no use of M_{m+1} to M_N. This scheme can therefore introduce serious degradation to M_1 to M_m due to NBTI. The subsequent DLDO performance deteriorations are discussed in Sections 3.2.2 and 3.3.

3.2.2 Negative Bias Temperature Instability

NBTI can introduce significant V_{th} degradations to pMOS transistors due to negatively applied gate to source voltage V_{gs}. The increase in $|V_{th}|$ due to NBTI is considered to be related to the generation of interface traps at the Si/SiO_2 interface when there is a gate voltage [115]. $|V_{th}|$ increases when electrical stress is applied and partially recovers when stress is removed. This process is commonly explained using a reaction-diffusion (R-D) model [115]. The V_{th} degradation can be estimated during each stress and recovery phase using a cycle-to-cycle model and can also be evaluated using a long-term reliability model [109, 116, 117]. As the long-term reliability evaluation is the focus of this work, the analytical model for long-term worst case threshold voltage degradation ΔV_{th} estimation in [109] is adopted in this work as

$$\Delta V_{th} = K_{lt}\sqrt{C_{ox}(|V_{gs}| - |V_{th}|)}e^{\frac{-E_a}{kT}}(\alpha t)^{\frac{1}{6}} \qquad (3.1)$$

where C_{ox}, k, T, α, and t are, respectively, the oxide capacitance, Boltzmann constant, temperature, the fraction of time (activity factor) when the device is under stress, and operation time. K_{lt} and E_a are the fitting parameters to match the model with the experimental data [109]. Note that NBTI recovery phase is already included in the model.
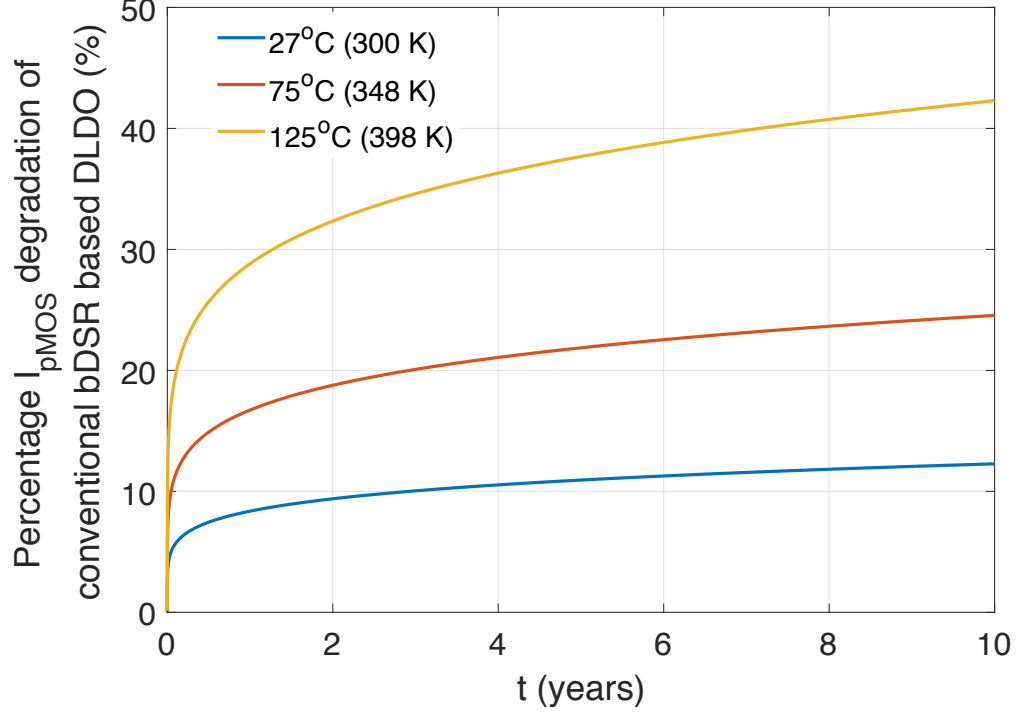
Figure 3.3: Percentage I_{pMOS} degradation of conventional bDSR based DLDO.

3.3 NBTI Induced Performance Degradation

I_{max}, T_R, and ΔV are among the most important design parameters for DLDOs. The effect of NBTI induced degradations on these important performance metrics is examined in this section.

3.3.1 Maximum Current Supply Capability

Without NBTI induced degradations, $I_{max}=NI_{pMOS}$, where I_{pMOS} is the maximum output current of a single pMOS stage. For DLDO, $|V_{gs}|$ in (3.1) is equal to V_{in} when M_i is active. The pMOS transistor M_i operates in linear region when turned on and the on-resistance R_{on} of a single pMOS stage can be approximated as [109]

$$R_{on} \approx [(W/L)\mu_p C_{ox}(V_{in} - |V_{th}|)]^{-1} \tag{3.2}$$

where W, L, μ_p, and C_{ox} are, respectively, the width, length, mobility, and oxide capacitance of M_i. I_{pMOS} can thus be expressed as

$$I_{pMOS} = \frac{V_{sd}}{R_{on}} = (V_{in} - V_{out})(W/L)\mu_p C_{ox}(V_{in} - |V_{th}|) \tag{3.3}$$

where V_{sd} is the source drain voltage of M_i. NBTI induced degradation factor DF_i for M_i can be defined as

$$DF_i = \frac{I_{pMOS_i}^{deg}}{I_{pMOS}} = \frac{V_{in} - |V_{th}| - \Delta V_{th_i}}{V_{in} - |V_{th}|} \tag{3.4}$$

where ΔV_{th_i} and $I_{pMOS_i}^{deg}$ are, respectively, NBTI induced V_{th} degradation and the degraded I_{pMOS} for M_i. Degraded I_{max} can be expressed as

$$I_{max}^{deg} = I_{pMOS} \sum_{i=1}^{N} DF_i. \tag{3.5}$$

As an example, the percentage I_{pMOS} degradation $1 - DF_i$ for smaller value of i, considering M_i is active most of the time, is shown in Fig. 3.3 as a function of time under different temperatures. A 32 nm metal gate, high-k strained-Si CMOS technology from PTM model library [117] is utilized. A nominal supply voltage $V_{in} = 0.9$ V is used. PTM is adopted for simulation as it is widely used for BTI study due to the availability of fitting parameter values in the ΔV_{th} degradation model [109, 118], [6-8]. As shown in Fig. 3.3, NBTI can induce significant I_{pMOS} degradations, especially at high temperatures. Degraded I_{pMOS} can further lead to reduced I_{max} and lower output voltage regulation capability under high load current. Moreover, as discussed in Sections 3.3.2 and 3.3.3, degraded I_{pMOS} also exacerbates T_R and ΔV, necessitating reliability enhancement techniques.

3.3.2 Load Response Time

Load response time T_R measures how fast the feedback loop responds to a step load. T_R can be estimated as [119]

$$T_R = RCln(1 + \frac{\Delta i_{load}}{I_{pMOS}f_{clk}RC}) \tag{3.6}$$

where R, C, f_{clk}, and Δi_{load} are, respectively, the average DLDO output resistance before and after Δi_{load}, load capacitance, clock frequency, and amplitude of the load change. Considering NBTI effect, degraded T_R can be expressed as

$$T_R^{deg} = RCln(1 + \frac{\Delta i_{load}}{DFI_{pMOS}f_{clk}RC}).$$

(3.7)

As $0 < DF < 1$ and $T_R < T_R^{deg}$, NBTI induced degradation slows down DLDO response.

3.3.3 Magnitude of the Droop

Magnitude of the droop ΔV reflects the V_{out} noise profile under transient response and can be estimated as [119]

$$\Delta V = R\Delta i_{load} - I_{pMOS}f_{clk}R^2Cln(1 + \frac{\Delta i_{load}}{I_{pMOS}f_{clk}RC}).$$

(3.8)

Considering NBTI effect, degraded ΔV can be expressed as

$$\Delta V_{deg} = R\Delta i_{load} - DFI_{pMOS}f_{clk}R^2Cln(1 + \frac{\Delta i_{load}}{DFI_{pMOS}f_{clk}RC}).$$

(3.9)

Let $\Delta i_{load}/I_{pMOS}f_{clk}RC = A$, $A > 0$. Under $0 < DF < 1$, the following holds

$$1 + A > (1 + \frac{A}{DF})^{DF}$$

(3.10)

thus

$$I_{pMOS}f_{clk}R^2Cln(1 + \frac{\Delta i_{load}}{I_{pMOS}f_{clk}RC}) > DFI_{pMOS}f_{clk}R^2Cln(1 + \frac{\Delta i_{load}}{DFI_{pMOS}f_{clk}RC})$$

(3.11)

and $\Delta V < \Delta V_{deg}$, which means NBTI can degrade the transient voltage noise profile.

Furthermore, it is worth noting that, as seen from (3.5), (3.6), and (3.8), NBTI induced DLDO performance degradations are mainly due to the degradation of the power transistors M_i
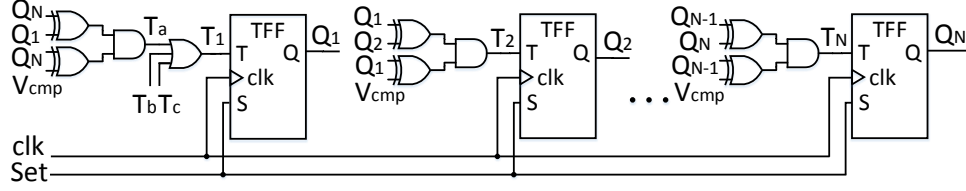
Figure 3.4: Proposed uni-directional shift register for NBTI-aware DLDO.

$(i = 1, ..., N)$ rather than the control loop. Thus, mitigation of power transistor degradations should be taken as a priority.

Power transistor M_is with smaller values of i are more heavily used than those with larger values of i for conventional bDSR based DLDO. As studied in [114] that load current variation per processor clock cycle can be small most of the time. It is thus reasonable to assume that the newly activated/deactivated power stages have similar level of I_{pMOS} degradations. As below average power is mostly consumed, conventional bDSR based DLDOs experience worst case T_R and ΔV degradations since the worst degraded M_is are utilized most of the time.

3.4 NBTI-Aware DLDO Voltage Regulator

To mitigate NBTI induced DLDO performance degradations, distributing the electrical stress among all available power transistors as evenly as possible under arbitrary load current conditions is essential. Reliability is not considered in conventional bDSR based DLDO designs, and therefore too much stress is exerted on a small portion of M_is. A novel uDSR is thus proposed in this work to evenly distribute the electrical stress among all of the M_is to realize a NBTI-aware DLDO voltage regulator and enhance reliability.

The schematic and operation of the proposed uDSR are shown, respectively, in Figs. 3.4 and 3.5. The elementary D flip-flop (DFF) and multiplexer within bDSR, as shown in Fig. 3.2a, are replaced with T flip-flop (TFF) and simple logic gates within the proposed uDSR, respectively. The rest of the DLDO including parallel power transistors and clocked comparator remains unchanged. The idea is to balance the utilization of each available M_i under all load current conditions. To achieve this objective, control signals Q_{i-1} and Q_i for two adjacent power transistors M_{i-1} and M_i,

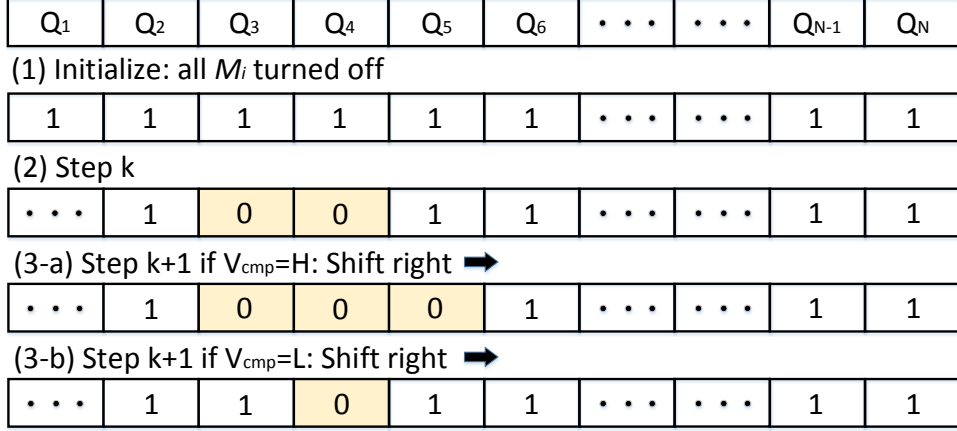| Q₁	Q₂	Q₃	Q₄	Q₅	Q₆	· · ·	· · ·	Q_{N-1}	Q_N
Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	· · ·	· · ·	Q_{N-1}	Q_N
(1) Initialize: all M_i turned off									
1	1	1	1	1	1	· · ·	· · ·	1	1
(2) Step k									
· · ·	1	0	0	1	1	· · ·	· · ·	1	1
(3-a) Step k+1 if V_cmp=H: Shift right ➡									
· · ·	1	0	0	0	1	· · ·	· · ·	1	1
(3-b) Step k+1 if V_cmp=L: Shift right ➡									
· · ·	1	1	0	1	1	· · ·	· · ·	1	1

Figure 3.5: Operation of the proposed uni-directional shift register.

respectively, are XORed to determine if M_{i-1} and M_i are at the boundary of active and inactive power transistor portions. Normally, there are two such boundaries if at least one power transistor is active, as shown in Fig. 3.5. Q_{i-1} and output of the comparator V_{cmp} are thus XORed to decide which power transistor at the boundaries need to be turned on/off at the rising edge of the clock signal. Inactive (active) power transistor at the right (left) boundary is turned on (off) if V_{cmp} is logic high (low). A uni-directional shift register is realized through this activation/deactivation scheme, as demonstrated in Fig. 3.5. Q_{i-1} for the first stage is Q_N from the last stage and thus a loop is formed. Considering the initialization step when all M_is are off and the full load current condition when all M_is are on, additional control signals are inserted as T_b and T_c in the first stage, to avoid inaction under these two situations, where $T_b = Q_1 \cdot Q_2 \cdots Q_N \cdot V_{cmp}$ and $T_c = \overline{Q_1 + Q_2 + \cdots + Q_N + V_{cmp}}$. The logic functions for T_b and T_c can be implemented with n-input AND/NOR gates [120]. Considering the similar area of DFF and TFF, the proposed uDSR only induces $\sim 3.8\%$ area overhead per control stage compared to bDSR. The total area overhead is thus $\sim 2.6\%$ of a single DLDO area designed with μA current supply capability [63]. As little extra transistors are added per control stage and the bDSR only consumes a few μW power [63], the uDSR induced power overhead is also negligible. With larger I_{pMOS} for higher load current rating, both the area and power overhead can be significantly less.

Table 3.1: Load Characteristics of Different Functional Blocks within One Core of an IBM POWER8 Like Microprocessor Chip under All Experimented Benchmarks

	IFU	LSU	ISU	EXU	L2
Min I_{load} (A)	0.091	0.172	0.125	0.251	0.178
Max I_{load} (A)	3.245	12.092	1.356	5.056	2.195
Avg I_{load} (A)	1.138	0.908	0.201	1.294	1.719

Under transient load current conditions, if $V_{out} < V_{ref}$ ($V_{out} > V_{ref}$) due to increased (decreased) load current, inactive (active) power transistors at the right (left) boundary are gradually turned on (off) to supply the required output current and regulate V_{out}. Under steady state conditions, the number of active power transistors changes dynamically due to limit cycle oscillations as shown in [63] in order to supply the required current. Newly activated (deactivated) power transistors always occur at the right (left) boundary, leading to the right shift of the active power transistors all the time. Thus, regardless of the load current conditions, electrical stress can always be evenly distributed among all of the available power transistors. Furthermore, as compared to conventional bDSR based DLDO, the number of activated/deactivated power transistors per clock cycle remains the same and thus the DLDO performance is not negatively affected.

Unlike the rotating phase-shedding scheme for multiphase buck converters implemented in [111], which only mitigates aging effects at light load conditions with only one active phase, the proposed uDSR is effective under all load current conditions. Moreover, as the proposed uDSR is a generalized method to determine which parallel power stage needs to be turned on/off, it can also be tailored for reliability enhancement within multiphase buck or switched capacitor voltage regulators with phase-shedding functionality.

3.5 Evaluation

To evaluate the benefits of the proposed uDSR based DLDO architecture in terms of reliability enhancement and to provide design insights for a targeted lifetime, an IBM POWER8 like microprocessor [64] simulation platform is constructed.
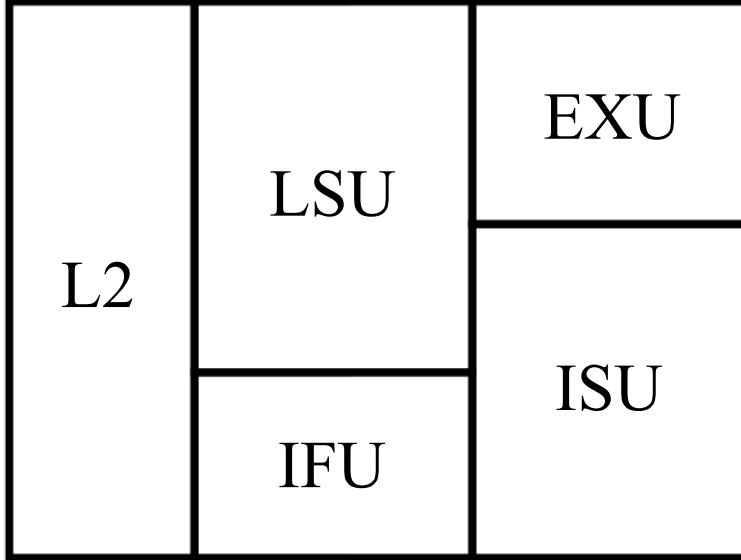
Figure 3.6: A schematic diagram demonstrating the floor plan of one core within IBM POWER8 like microprocessor chip.

3.5.1 Simulation Framework

3.5.1.1 IBM POWER8 Like Microprocessor

IBM POWER8 microprocessor [64] is among one of the state-of-the-art server-class processors and thus representative for evaluation of the proposed NBTI-aware DLDO scheme. The same corresponding technology and architecture parameters listed in Table 2.1 are considered. The IBM POWER8 like microprocessor as shown in Fig. 3.6, includes a load store unit (LSU), an execution unit (EXU), an instruction fetch unit (IFU), an instruction scheduling unit (ISU), an L1 data cache inside LSU, an L1 instruction cache inside IFU, and a private L2. All benchmarks are from SPALSH2x [121] and cover a wide range of representative application domains. Analysis is restricted to the region-of-interest of the benchmarks and eight threads are involved in the simulations. The load characteristics of different functional blocks, as shown in Fig. 3.6, under all experimented benchmarks are summarized in Table 3.1.

Table 3.2: Conventional DLDO Performance Degradation for Different Functional Blocks under All Experimented Benchmarks for a Five-Year Time Frame

	IFU	LSU	ISU	EXU	L2
% I_{pMOS} degradation	16.2	21.4	15.3	16.6	15.1
% T_R degradation	9.4	12.9	8.9	9.7	8.7
% ΔV degradation	6.4	8.7	6.1	6.6	6

3.5.1.2 DLDO Design Specifications

Distributed micro-regulators are implemented in IBM POWER8 microprocessor [122]. In this simulation example, a switch array of 256 pMOS transistors, which is typical in DLDO designs [63], is implemented in each micro-regulator. Two different DLDO designs with bDSR and uDSR controls are implemented using 32 nm PTM CMOS technology where $V_{in} = 1.1$ V and $V_{out} = 1$ V as in [122]. $I_{pMOS} = 2$ mA and $I_{max} = 512$ mA are used in the simulations, leading to 7, 24, 3, 10, and 5 micro-regulators (DLDOs) in, respectively, IFU, LSU, ISU, EXU, and L2 blocks to be able to supply the maximum load current across all benchmarks in each block. Load current of each block is assumed to be supplied by micro-regulators within that block, which is reasonable due to the principle of spatial locality [30] regarding current distribution. Each micro-regulator within a certain block is assumed to provide equal current due to the availability of current balancing scheme implemented within IBM POWER8 microprocessor [73]. $f_{clk} = 10$ MHz and $C = 15$ nF are used for each DLDO to achieve smaller than 10% Vdd transient voltage noise [31] most of the time. The total output capacitance of 735 nF is comparable to 750 nF used in [122].

3.5.1.3 Evaluation of NBTI Induced Performance Degradation

Equations (3.1), (3.3), (3.6), and (3.8) are leveraged for evaluation of NBTI induced performance degradation. A typical temperature profile [31, 123] of 90°C, 69°C, 67°C, 63°C, and 62°C for, respectively, LSU, EXU, IFU, ISU, and L2 is adopted for evaluations. The activity factors for both DLDO designs under different benchmarks and functional blocks are estimated through simulations in Cadence Virtuoso. The worst case I_{pMOS} degradations are used for evaluations of both designs, which is reasonable due to load characteristics of typical applications [114] and the consequent heavy use of a portion of M_is in conventional DLDOs.
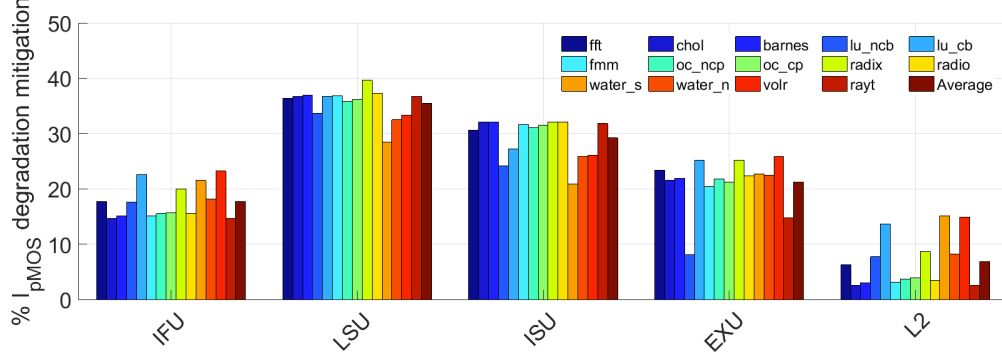
Figure 3.7: Percentage I_{pMOS} degradation mitigation of the proposed NBTI-aware DLDO as compared to the conventional DLDO design for different functional blocks under all experimented benchmarks.

3.5.2   Simulation Results

3.5.2.1   Performance Degradation within Conventional DLDO

Conventional DLDO performance degradation for different functional blocks for a five-year time frame is summarized in Table 3.2. These degradations apply to all the experimented benchmarks as the worst case I_{pMOS} degradation is considered. As shown in Table 3.2, NBTI can induce serious I_{pMOS}, T_R, and ΔV degradations for all functional blocks. I_{pMOS} degradation can lead to the deterioration of DLDO V_{out} regulation capability and possible V_{out} drop under large load current conditions. Larger than 10% V_{out} drop can lead to voltage emergencies and potential execution errors for microprocessors. Similarly, T_R and ΔV degradations can, respectively, increase the duration and frequency of voltage emergencies, which can slow down microprocessor executions as further actions may need to be taken to remedy the errors. Moreover, for a longer targeted lifetime of more than five years, the degradations are expected to be more disastrous as I_{pMOS} degradations are even worse, as seen from Fig. 3.3, which may not be tolerable for critical applications where replacement of the devices can be costly or even impossible.

3.5.2.2   Mitigation with Proposed NBTI-Aware DLDO

Simulation results for all benchmarks are summarized in Figs. 3.7, 3.8, and 3.9 regarding, respectively, I_{pMOS}, T_R, and ΔV degradation mitigation of the proposed NBTI-aware DLDO as
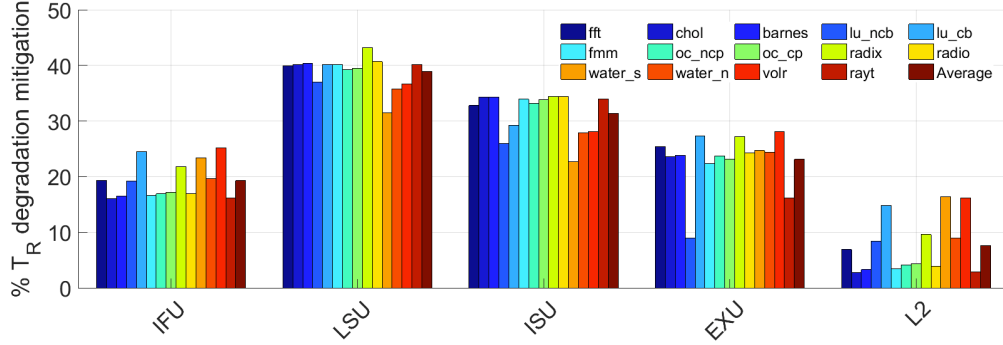
Figure 3.8: Percentage T_R degradation mitigation of the proposed NBTI-aware DLDO as compared to the conventional DLDO design for different functional blocks under all experimented benchmarks.
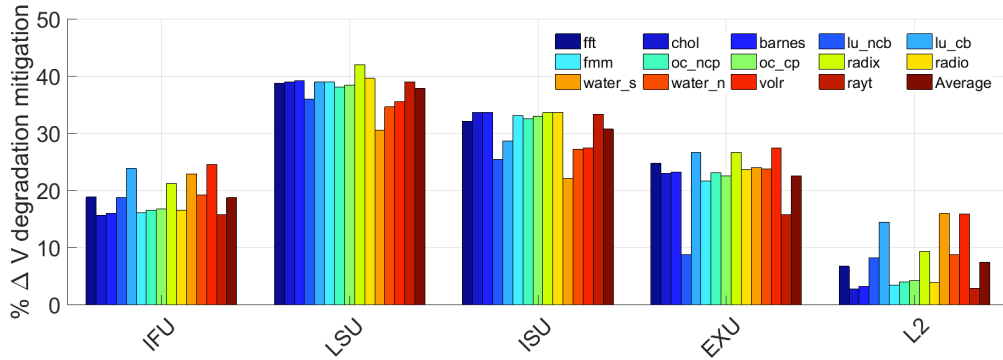

Figure 3.9: Percentage ΔV degradation mitigation of the proposed NBTI-aware DLDO as compared to the conventional DLDO design for different functional blocks under all experimented benchmarks.

compared to the conventional DLDO design for a five-year time frame. Up to 39.6%, 43.2%, and 42% performance improvement is achieved for, respectively, I_{pMOS}, T_R, and ΔV. The highest performance improvement is obtained for LSU with the highest operation temperature. Even at the lowest operation temperature within L2, degradation mitigations of up to 15.1%, 16.4%, and 15.9% are achieved for, respectively, I_{pMOS}, T_R, and ΔV.

3.5.2.3 Discussions

For high temperature applications and applications with high maximum to average current ratio, such as the LSU block, NBTI can induce greater performance degradations as summarized in Tables 3.1 and 3.2. The benefits of the proposed NBTI-aware DLDO scheme are also more advantageous for certain applications as shown in Figs. 3.7, 3.8, and 3.9 for the LSU portions. For

applications where the average current is close to the maximum current, such as the L2 block, the performance degradation mitigations using the proposed NBTI-aware DLDO are less significant but still beneficial as compared to the conventional design considering negligible extra power and area overhead induced by the proposed design.

DLDO performance degradations can vary under different load characteristics and temperature. It is thus essential to examine these degradations in early design stage with the applied reliability enhancement techniques. Extra design margins, such as increased number of M_i and/or output capacitance, should be adopted adaptively according to the aging speed of different functional blocks and benchmark applications instead of utilizing a uniform margin to avoid potential overdesign.

3.6   Conclusion

The DLDO regulators can experience serious NBTI induced performance degradations including I_{pMOS}, T_R, and ΔV. These degradations are typically overlooked in the design of DLDOs and can deteriorate the regulation capability, response speed, and transient voltage noise profile. A novel uni-directional shift register is proposed in this chapter to evenly distribute the electrical stress among different power transistors to mitigate NBTI induced performance degradation with nearly no extra power and area overhead under arbitrary load conditions. Through practical simulations of an IBM POWER8 like microprocessor and benchmark evaluations, it is demonstrated that up to 39.6%, 43.2%, and 42% degradation mitigation can be achieved for, respectively, I_{pMOS}, T_R, and ΔV with the proposed technique. Simulation results also highlight the necessity of adaptive design margins to avoid overdesign.

CHAPTER 4:

AGING EFFECTS ON THE STEADY STATE PERFORMANCE

DEGRADATION OF ON-CHIP VOLTAGE REGULATORS

4.1 Introduction

Distributed on-chip voltage regulation [2, 124] in fine temporal and spatial granularity enables fast and timely control of the operating point.[1] Thereby the operating voltage and frequency can better match the needs of the workload to maximize energy efficiency. As a function of the workload, throughout the execution time, different components of a processor chip exhibit different microarchitectural activities, which translates into different demands for current to be pulled from the respective regulators. Different components of the processor chip also show different degrees of tolerance to errors, which may result from deviation of design parameters from their target values due to device wear-out, voltage noise, temperature, or process variations. For example, it has been observed that the emerging recognition, mining, and synthesis (RMS) [125] applications can tolerate errors in the data flow, but not in control [126].

Heterogeneous distributed on-chip voltage regulation has been explored to best capture spatio-temporal variations in current demand of different processor components, where the regulator operating regimes are tailored to the activity range of the respective load (processor component). Such tailoring can be achieved by (i) keeping the regulator design constant across chip, but making each regulator reconfigurable; or (ii) by designing each regulator from the ground-up to match different load conditions. A promising direction which has not been explored is how such heterogeneity can help in trading the program output quality for area overhead, by *e.g.*, assigning error-prone

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[1]This chapter includes portions of the published paper in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Early Access, DOI (identifier) 10.1109/TVLSI.2018.2871381 "Exploiting Algorithmic Noise Tolerance for Scalable On-Chip Voltage Regulation". Permission is included in Appendix A.

(*i.e.*, slower and/or less accurate) regulators to feed processor components in charge of data flow which can tolerate errors. Control-heavy components, on the other hand, should not be permitted to leave the error-free zone to avoid catastrophic program termination or excessive loss in program output quality even if the program does not crash.

To this end, we must understand the type and impact of errors that voltage regulators can introduce to the system, such that we can assess to what extent such regulator-induced errors can be masked by their respective loads (*i.e.*, data flow heavy processor components) and how regulator-induced errors interact with load-induced potential errors in determining the final computation accuracy. In this chapter, we will try to shed light into this question by quantifying the impact of one of the most prevalent reliability concerns, aging, on regulator robustness, without loss of generality.

The major transistor aging mechanisms include bias temperature instability (BTI), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and electromigration (EM), among which BTI is the dominant reliability concern for nanometer integrated circuits design [109, 118, 127]. BTI can induce threshold voltage increase and consequent circuit level performance degradation. Positive BTI (PBTI) induces aging of nMOS transistors while negative BTI (NBTI) causes aging of pMOS transistors [109]. The impact of BTI aging mechanism is a strong function of temperature, electrical stress, and time.

As an essential part of a processor chip, on-chip voltage regulators need to be active most of the time to provide the required power to different components of the processor chip. The load current and temperature can vary significantly among these components for different processor applications [31]. All of these variations partially contribute to different aging mechanisms of on-chip voltage regulators, which should be considered to avoid over-design for a targeted lifetime. Additionally, in certain processor components that can show higher degrees of tolerance to errors, the regulators can be intentionally under-designed to save valuable chip area and potentially power-conversion efficiency. In other words, a heterogeneous distributed power delivery network can be designed consisting of different voltage regulators with accurate voltage regulators that house additional circuitry to mitigate the aging induced supply voltage variations and approximate voltage

regulators that are intentionally under-designed to mitigate just-enough aging-induced variations. The quality of the supply voltage directly affects data path delay and signal quality, and fluctuations in the supply voltage result in delay uncertainty and clock jitter. Accordingly, the supply noise tolerance of certain processor components is investigated as an area-quality control knob where the quality of the supply voltage can be compromised to save valuable chip area.

Several studies have been performed regarding the reliability issues in nanometer CMOS designs [116, 128, 129]. There is, however, quite limited amount of work on the reliability of on-chip voltage regulators. Device aging on the immunity level of electro-magnetic interference (EMI) for low-dropout regulators (LDO) is characterized in [110]. A method of distributing the aging stress by rotating the phase to shed at light load is proposed in [111] to enhance the light load efficiency for multiphase buck converters. An algorithm to uniformly distribute the current provided by the power transistor array of a digital LDO (DLDO) is proposed in [65] to reduce hot spots and ensure reliable silicon operation. The reliability of metal wires connected to on-chip voltage regulators is investigated in [6]. Nonetheless, quantitative analysis of aging effects on on-chip voltage regulators considering load current characteristics and temperature variations as well as efficient reliability enhancement techniques under arbitrary load conditions have not yet been investigated.

As compared to other voltage regulator types, the emerging digital LDO has gained impetus due to the design simplicity, easiness for integration, high power density, and fast response [63, 112, 130]. DLDOs have demonstrated major advantages in modern processors including the recent IBM POWER8 processor [64]. More importantly, as compared to the analog LDOs, DLDO can provide certain advantages for low-power and low-voltage IoT applications due to its capability for low supply voltage operations [113]. However, as pMOS is used as the power transistor for DLDOs, NBTI induced degradations largely affect important performance metrics such as the maximum output current capability I_{max}, load response time T_R, and magnitude of the droop ΔV as defined in [73]. Meanwhile, the combined NBTI and PBTI induced control loop degradations can potentially increase the mode of inherent limit cycle oscillations (LCOs) within DLDOs and adversely affect the steady state output voltage ripple performance. It is therefore imperative to investigate aging mitigation techniques for DLDOs to achieve reliable operation of critical components. As aging
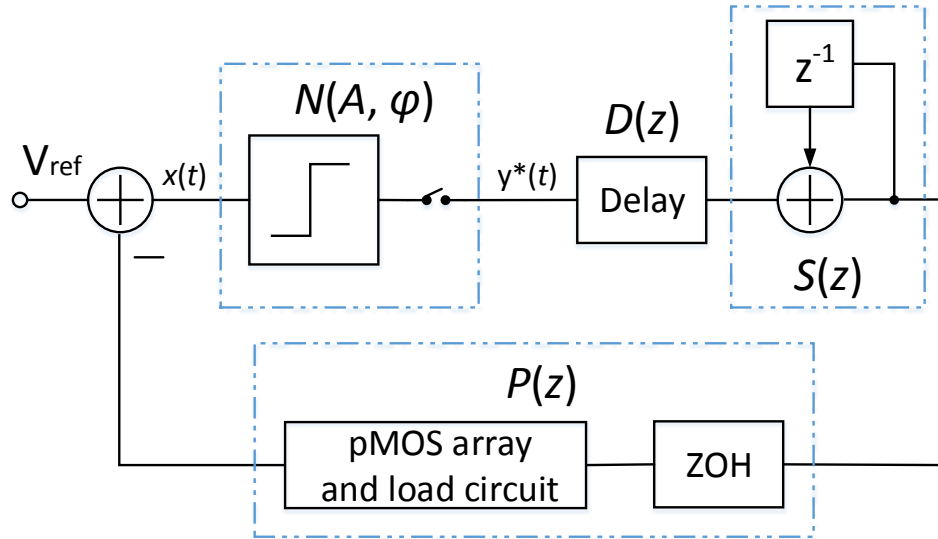
61

Figure 4.1: Nonlinear sampled feedback model of a conventional DLDO.

effects on the transient performance degradation of DLDOs have been investigated in Chapter 3, aging effects on the steady state performance degradation of DLDOs will be the focus of this chapter. Furthermore, when a circuit component can tolerate higher degrees of errors, the DLDOs can be designed with minimal area overhead, achieving heterogeneous power delivery. A voltage regulator is proposed in this chapter that can be designed at the design time based on the supply noise resiliency requirement of the circuitry it powers. Since the number of voltage regulators can be as high as several hundreds in modern processors [64], the area and number of voltage regulators can be easily scaled thereby to satisfy the diverse needs of systems that house components with varying degrees of noise tolerance.

The rest of this chapter is organized as follows. The potential side effects of limit cycle oscillation on the steady state performance of DLDO is studied in Section 4.2. Aging-aware limit cycle oscillation mitigation technique is investigated in Section 4.3. Effectiveness of the proposed technique is verified in Section 4.4. Trade-off between area overhead and program output quality is illustrated in Section 4.5. Concluding remarks are offered in Section 4.6.

4.2 Limit Cycle Oscillation

In conventional DLDOs, when the shift register turns on/off the pass transistor, the output voltage of the DLDO cannot change instantaneously due to the output pole of the DLDO. The delay between the operation of the shift register and fluctuation of the output voltage, together with the quantization effects of the comparator and the delay between the sampling instant and the time of pMOS array actuation lead to the occurance of LCO. Such behavior can be examined by a nonlinear sampled feedback model developed in [131] to determine the possible modes and amplitudes of LCOs.

The model consists of $N(A, \varphi)$, $P(z)$, $S(z)$, and $D(z)$ as shown in Fig. 4.1, which represent, respectively, the describing function of the clocked comparator, transfer function of the zero-order hold (ZOH) together with the pMOS array and load circuit, transfer function of the shift register, and delay element between the comparator and shift register. A and φ stand for the LCO amplitude and the phase shift of $x(t)$, respectively.

$N(A, \varphi)$, $P(z)$, $S(z)$, and $D(z)$ can be expressed, respectively, as [132, 133]

$$N(A, \varphi) = \frac{2D}{MTA} \sum_{m=0}^{M-1} sin(\frac{\pi}{2M} + \frac{m\pi}{M}) \angle (\frac{\pi}{2M} - \varphi) \tag{4.1}$$

$$P(z) = K_{OUT} \frac{1 - e^{-F_l T}}{F_l(z - e^{-F_l T})} \tag{4.2}$$

$$S(z) = \frac{z}{z - 1} \tag{4.3}$$

$$D(z) = z^{-1} \tag{4.4}$$

where $K_{OUT} = K_{DC} I_{pMOS}$, $T = 1/f_{clk}$, $F_l = 1/(R_L || R_{pMOS})C$, and $\varphi \in (0, \pi/M)$. D, F_l, K_{OUT}, K_{DC}, R_L, and R_{pMOS} are, respectively, the amplitude of comparator output, load pole, gain of $P(z)$, DC proportional constant, load resistance, resistance of power transistor array.

The mode and amplitude of LCO can be determined by the following Nyquist criterion,

$$N(A, \varphi)P(e^{j\omega T})S(e^{j\omega T})D(e^{j\omega T}) = 1\angle(-\pi) \tag{4.5}$$
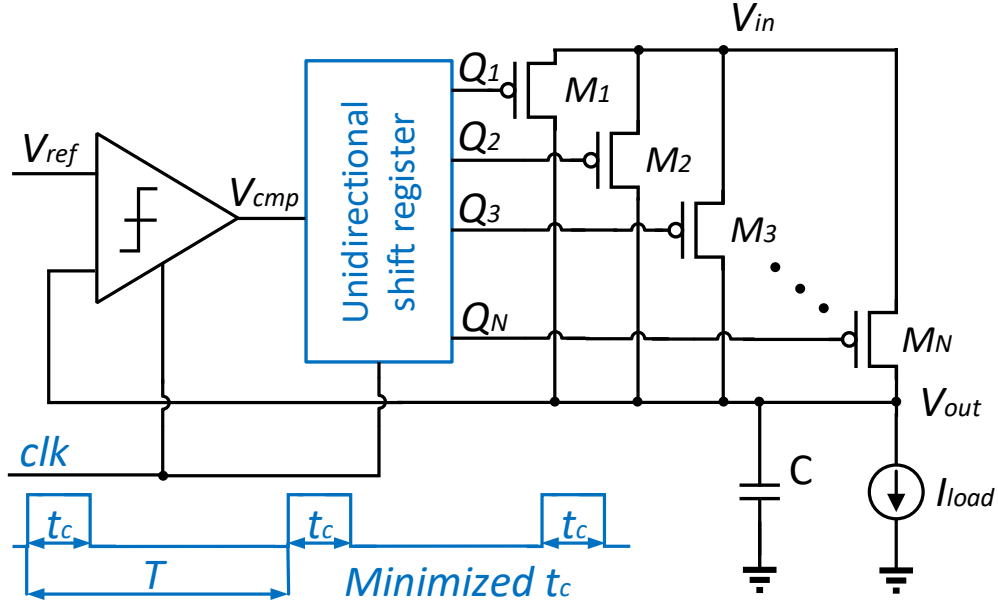
Figure 4.2: Schematic of the proposed aging-aware DLDO.

where $\omega = \pi/TM$ is the angular LCO frequency. The phase shift φ_{LCO} for a steady LCO can thus be expressed as [132]

$$\varphi_{LCO} = \frac{\pi}{2} - \frac{\pi}{2M} - tan^{-1}(\frac{\pi}{MTF_l}). \tag{4.6}$$

φ_{LCO} needs to be within $(0, \pi/M)$ for mode M to exist.

Transistor aging can lead to increased path delay [134]. Considering BTI induced propagation delay degradation of the clocked comparator and shift register, the delay element in Fig. 4.1 becomes

$$D'(z) = z^{-1}z^{-\frac{t_c^d}{T}}z^{-\frac{(t_s^d - t_c^d)}{T}} = z^{-1-\frac{t_s^d}{T}} \tag{4.7}$$

where t_c^d and t_s^d are, respectively, the degraded propagation delay of the clocked comparator and shift register. Note that t_c^d is canceled out in $D'(z)$ and thus the propagation delay of clocked comparator has negligible effects on the mode of LCO. φ_{LCO} then becomes

$$\varphi'_{LCO} = \frac{\pi}{2} - \frac{\pi}{2M} - tan^{-1}(\frac{\pi}{MTF_l}) - \frac{\pi t_s^d}{MT}. \tag{4.8}$$

64

The negative effect of the propagation delay of the shift register on LCO can be explained as follows. If an LCO mode M_a exists and the propagation delay of the shift register is not considered, the phase shift φ_{LCO} is within $(0, \pi/M_a)$. That is $0 < \pi/2 - \pi/2M_a - tan^{-1}(\pi/M_a TF_l) < \pi/M_a$. For a larger LCO mode $M_a + 1$ to exist, the following condition needs to be satisfied

$$0 < \frac{\pi}{2} - \frac{\pi}{2(M_a+1)} - tan^{-1}(\frac{\pi}{(M_a+1)TF_l}) < \pi/(M_a+1). \tag{4.9}$$

Typically

$$\frac{\pi}{2} - \frac{\pi}{2(M_a+1)} - tan^{-1}(\frac{\pi}{(M_a+1)TF_l}) > \frac{\pi}{2} - \frac{\pi}{2M_a} - tan^{-1}(\frac{\pi}{M_a TF_l}) \tag{4.10}$$

and if $\pi/2 - \pi/2M_a - tan^{-1}(\pi/M_a TF_l)$ is very close to π/M_a, it is likely that

$$\varphi_{LCO}|_{M=M_a+1} = \frac{\pi}{2} - \frac{\pi}{2(M_a+1)} - tan^{-1}(\frac{\pi}{(M_a+1)TF_l}) > \pi/M_a > \pi/(M_a+1) \tag{4.11}$$

such that LCO mode $M_a + 1$ can not exist as (4.9) is violated.

However, if the propagation delay of the shift register is included, for LCO mode $M_a + 1$, φ_{LCO} becomes

$$\varphi'_{LCO}|_{M=M_a+1} = \frac{\pi}{2} - \frac{\pi}{2(M_a+1)} - tan^{-1}(\frac{\pi}{(M_a+1)TF_l}) - \frac{\pi t_s^d}{(M_a+1)T}. \tag{4.12}$$

The contribution of $\pi t_s^d/(M_a+1)T$ term may push $\varphi'_{LCO}|_{M=M_a+1}$ to be within the range of $(0, \pi/(M_a+1))$, making a larger LCO mode $M_a + 1$ possible. This demonstrates the potential negative effect of the propagation delay of the shift register on LCO.

4.3 Reduced Clock Pulse Width

Dual clock edge triggering has been employed in [133, 135] to reduce the control signal delay, where the clocked comparator and shift register are triggered at the rising and falling edge of the clock signal, respectively. Considering the potential side effect of the control loop delay element $D'(z)$ on LCO, a reduced clock pulse width t_c, as shown in Fig. 4.2, is proposed to minimize the delay element. With dual clock edge triggering implementation of the control loop, the following

Table 4.1: TFF Setup Time, Logic Delay, and Comparator Delay Before and After a Five-Year Aging Period

	TFF setup time	Logic delay	Comparator delay
Fresh (ps)	170	209.6	171.5
Aged 5 yrs (ps)	180	227.4	225
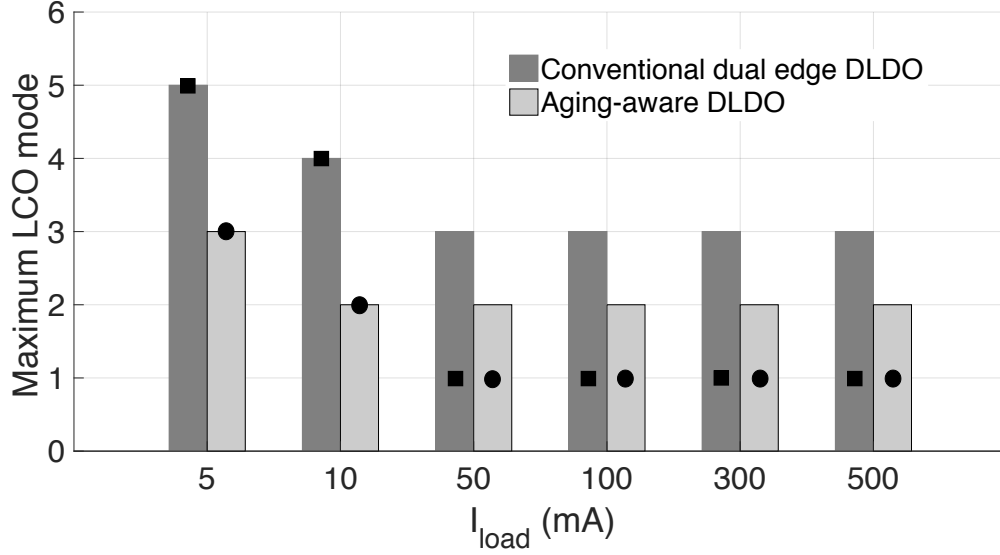
Figure 4.3: Maximum LCO mode with simulation results superimposed for conventional and aging-aware DLDO under different load current conditions after a five-year aging period.

condition needs to be satisfied regarding t_c for proper operation of the uDSR based DLDO

$$t_c > t_c^d + t_l^d + t_t^{st} \tag{4.13}$$

where t_l^d and t_t^{st} are, respectively, the total propagation delay of the logic gates connected to the first stage TFF within the uDSR and the setup time of the TFF. Aging induced degradation of t_c^d, t_l^d, and t_t^{st} needs to be considered with the targeted lifetime to decide the value of t_c. The one-shot pulse generator in [98] can be leveraged for reduced pulse width clock generation.

Within the proposed aging-aware DLDO, φ_{LCO} becomes

$$\varphi_{LCO}'' = \frac{\pi}{2} + \frac{\pi}{2M} - tan^{-1}(\frac{\pi}{MTF_l}) - \frac{\pi(t_s^d + t_c)}{MT}. \tag{4.14}$$

Table 4.2: Maximum LCO Mode under Different Sampling Clock Frequency and Load Current Condition for Conventional Dual Edge (CDE) and Aging-Aware (AA) DLDO

CDE/AA LCO mode	Sampling clock frequency f_{clk} (MHz)				
I_{load} (mA)	10	50	100	300	500
10	4/2	8/6	11/9	20/18	27/27
100	3/2	3/2	4/3	6/6	8/8
500	3/2	3/2	3/2	3/3	4/4

4.4 LCO Mitigation with Proposed Aging-Aware DLDO

To verify the benefits of the proposed reduced clock pulse width DLDO regarding LCO mitigation, the theoretical maximum LCO mode for dual edge triggered and reduced clock pulse width DLDO with uDSR implementation are respectively examined by considering BTI induced threshold voltage degradation of the control loop. An average IBM POWER8 microprocessor temperature profile of 70^oC is utilized for V_{th} degradation evaluation. NBTI and PBTI are considered as the major V_{th} degradation factor for pMOS and nMOS transistors in the control loop, respectively. Under different load current conditions, the activity factor of each transistor within the control loop is obtained through Cadence Virtuoso simulations. Equation (3.1) is then leveraged to calculate the V_{th} degradation for each transistor within a five-year time frame. The calculated V_{th} degradation is embedded in each transistor by adopting the subcircuit model for BTI effect in [136] within Cadence Virtuoso simulations. The fresh and aged TFF setup time t_t^{st}, logic delay t_l^d, and comparator delay t_c^d are summarized in Table 4.1. The aged t_t^{st}, t_l^d, and t_c^d are approximately load current independent. $t_c = 1ns$ is adopted to satisfy timing constraint in (4.13). The maximum LCO mode for dual edge triggered and reduced clock pulse width DLDO under different load current conditions after a five-year aging period is illustrated in Fig. 4.3.

Seen from Fig. 4.3, with reduced clock pulse width considering aging imposed limitations, maximum LCO mode can be greatly reduced especially at light load conditions. The simulated steady state output voltages for both conventional dual edge triggered DLDO and the proposed aging-aware DLDO under 10 mA load current are demonstrated in Fig. 4.4. LCO mode reduction from 4 to 2 and 3 times output voltage ripple amplitude reduction are achieved. As the minimum and average I_{load} can be way smaller than the maximum I_{load} shown in Table 3.1 especially for LSU,

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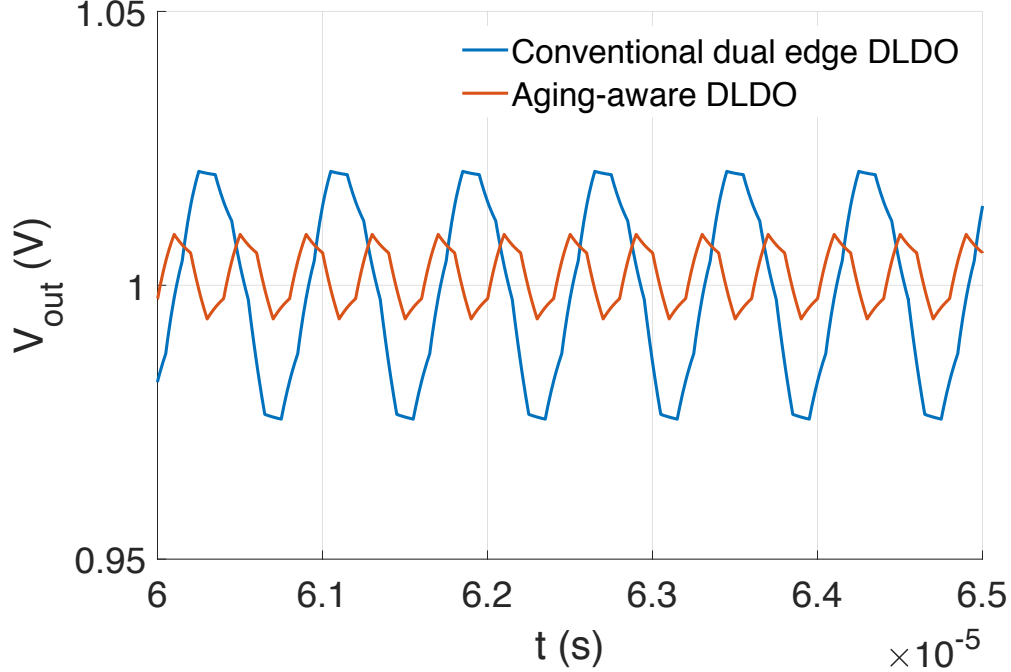
Figure 4.4: Simulated output voltage ripple and LCO mode reduction with the proposed aging-aware DLDO under 10 mA load current.

light and medium load conditions are experienced most of the time such that outstanding benefits can be achieved with the proposed aging-aware DLDO considering the negligible power and area overhead induced.

Furthermore, in many applications the clock frequency can be much higher than 10 MHz such as 1 GHz in [137]. However, the 1 GHz sampling clock sacrifices the quiescent current. Recent work such as [135] and [138] utilizes a high clock frequency for fast transient and a much lower frequency for steady state operation. For a better verification of LCO improvement utilizing the proposed reduced clock pulse width scheme, maximum LCO mode under different sampling clock frequency and load current condition for both conventional dual edge and aging-aware DLDO is shown in Table 4.2. Seen from the table, the proposed reduced clock pulse width scheme demonstrates maximum LCO mode reduction under a wide f_{clk} range especially under light load current condition. For a clock frequency of 1 GHz, there would be no room to further reduce the pulse width due to the timing constraint. However, as discussed before, clock frequency utilized at steady state operation is typically much lower.
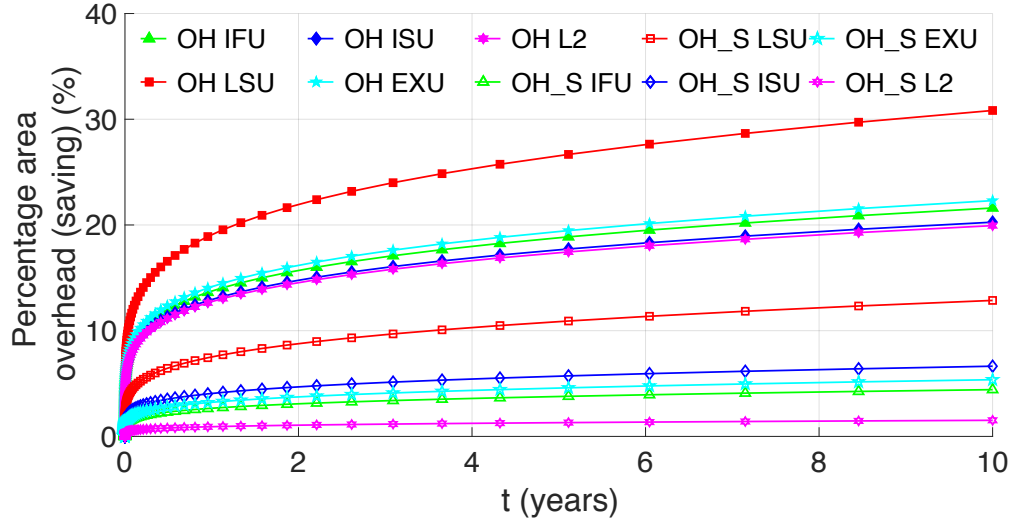
Figure 4.5: Percentage area overhead (OH) utilizing conventional DLDO and percentage area overhead saving (OH_S) utilizing aging-aware DLDO for ΔV degradation mitigation within each functional unit.
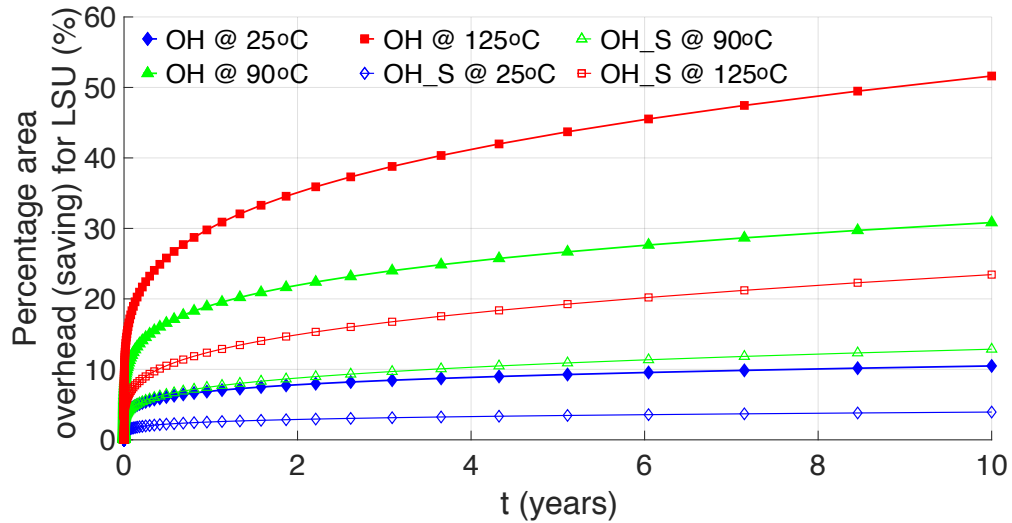
Figure 4.6: Percentage area overhead utilizing conventional DLDO and percentage area overhead saving utilizing aging-aware DLDO for ΔV degradation mitigation within LSU under different temperature profile.

4.5 Trade-Off between Area Overhead and Program Output Quality

Considering aging effects, regulators are typically designed and optimized for the expected service life of the processor. Deploying regulators optimized for a shorter service life cannot guarantee error-free operation, however, if such regulators are confined to feed error-tolerant loads, the
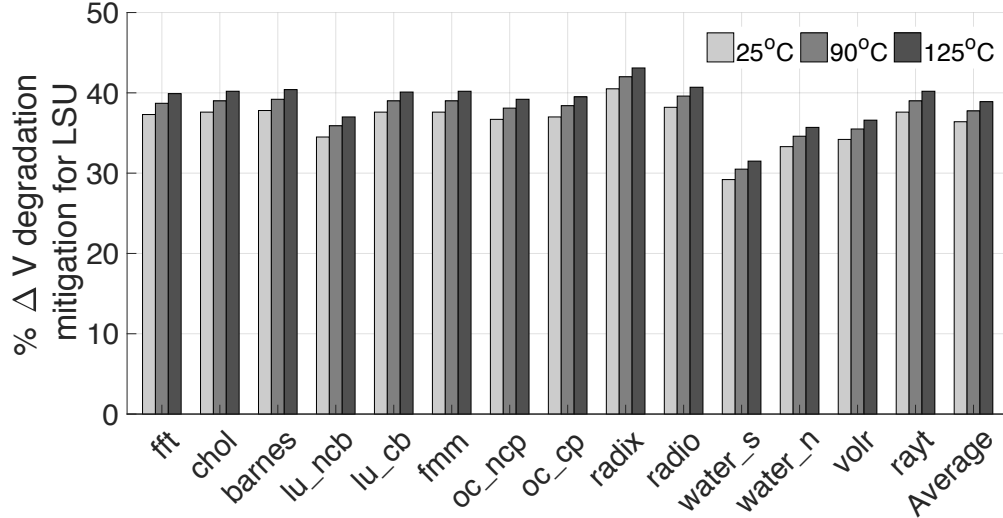
Figure 4.7: Percentage ΔV degradation mitigation of the proposed aging-aware DLDO as compared to the conventional DLDO design for LSU under all experimented benchmarks and different temperature profile.

service life can be traded for lower hardware complexity, which almost always directly translates into area savings. Please note that area represents a scarce on-chip resource for distributed voltage regulators as many of these regulators are squeezed between various circuit blocks. Such area savings can enable a higher number of on-chip voltage regulators, hence enhance the scalability of on-chip voltage regulation. To illustrate this point, the percentage area overhead within each functional unit to achieve the same fresh ΔV performance utilizing conventional DLDO is examined in Fig. 4.5. The relative area between pMOS array & shift register and output capacitance is based on the data in [138] for estimation. Adding extra output capacitance to mitigate ΔV degradation is considered in the estimation. The percentage area overhead is relative to the original DLDO area including output capacitance designed in an aging-unaware fashion. The percentage area overhead saving within each functional unit for ΔV degradation mitigation utilizing the proposed aging-aware DLDO is also demonstrated in Fig. 4.5. As shown in Fig. 4.5, a large area overhead can be introduced to mitigate aging induced transient voltage noise degradation for conventional DLDOs. Similar to the trend demonstrated in Fig. 3.3, the area penalty required to compensate for the aging-related deterioration of ΔV is significant especially in the first two years. The percentage area overhead also plateaus to within 10% after two years. These trends need to be considered to realize optimal
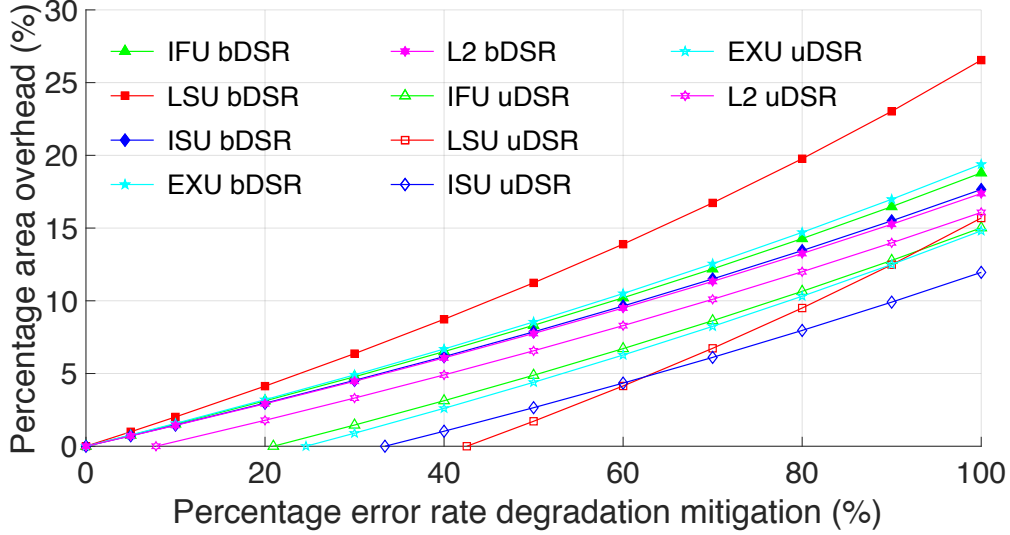
Figure 4.8: Percentage area overhead within each functional unit for percentage error rate degradation mitigation utilizing bDSR and uDSR based DLDO.

design based on different application environment and lifetime target. Furthermore, leveraging the proposed aging-aware DLDO, due to mitigation of aging induced ΔV degradation, significant area overhead savings compared to the conventional DLDO case can be achieved as shown in Fig. 4.5. Our proof-of-concept analysis reveals approximately 1% total DLDO area, which corresponds to $\sim$ 36% active DLDO area, savings for per year service life reduction.

The temperature variation effects on percentage area overhead (saving) within LSU is demonstrated in Fig. 4.6. Seen from the figure, as temperature increases, the percentage area overhead needed for conventional DLDO to mitigate ΔV degradation increases significantly. The percentage area overhead saving achieved by the aging-aware DLDO also greatly increases. Although the relative benefits of aging-aware DLDO do not improve significantly as temperature increases shown in Fig. 4.7, the area overhead saving is considerable due to the relatively large ratio between the area of output capacitance and that of active DLDO.

For a proof of concept analysis, considering a five-year aging period, the percentage area overhead within each functional unit for percentage error rate degradation mitigation utilizing bDSR and uDSR based DLDO is demonstrated in Fig. 4.8 based on the relationship between error rate and supply voltage demonstrated in [139, 140]. The percentage error rate degradation mitigation is with

respect to the degraded error rate utilizing bDSR based DLDO and a 100% error rate degradation mitigation means the same error rate within each functional unit is achieved as the fresh one after a five-year aging period. Seen from Fig. 4.8, contrary to the bDSR curves, the uDSR curves do not start from origin, which means with negligible area overhead, uDSR based DLDO achieves certain amount of error rate degradation mitigation compared to bDSR based DLDO. Also, for the same amount of error rate degradation mitigation, the area overhead needed for uDSR based DLDO is lower than that of bDSR based DLDO.

4.6   Conclusion

As an emerging and essential part of modern processor power delivery network, DLDO regulators experience serious aging induced performance degradations including I_{pMOS}, T_R, and ΔV. In particular, DLDO degradation can increase noise in the supply voltage and further deteriorate program output quality. Area overhead needed to fully compensate these degradations can be significant especially when a conventional DLDO design is utilized. Algorithmic noise tolerance of different processor components is leveraged as an area-quality control knob to alleviate the area overhead requirement through scalable on-chip voltage regulation at design time. Furthermore, DLDO designed in an aging-aware fashion is proposed to mitigate aging induced performance degradations with negligible power and area overhead. With reduced DLDO performance degradation, a significantly better area and quality trade-off can be achived due to aging-aware DLDO induced area overhead savings. Therefore, more efficient scalable on-chip voltage regulation can be realized with the proposed aging-aware DLDO. Up to 3X steady state DLDO performance improvement as well as more than 10% area overhead saving can be achieved utilizing the proposed aging-aware paradigm.

72

CHAPTER 5:

CONCLUSIONS

Unbalanced current sharing among distributed on-chip voltage regulators negatively affect the power conversion efficiency, stability, and reliability of the power delivery network. An effective balanced current sharing technique is proposed to enhance the power efficiency, stability, and reliability. The proposed technique slightly increases the reference voltages of on-chip voltage regulators that provide less current and decreases the reference voltages of those providing more current to balance the overall current sharing. Due to the small effective resistance variations connecting voltage regulators at different locations, the reference voltage changes needed to balance the current are also negligible. Simulation results demonstrate up to 8% regulator power loss saving, several years of MTTF improvement, and enhanced system stability.

NBTI leads to the amplitude increase of the threshold voltage and has been demonstrated to degrade the current supply capability, transient response time, and voltage droop performance of digital LDOs. Conventional digital LDOs utilizing bidirectional shift register for power transistor array control impose too much stress on a certain portion of power transistors. The proposed unidirectional shift register based NBTI-aware digital LDO can more evenly distribute the electrical stress among all of the power transistors to mitigate NBTI induced performance degradations. Under practical simulation settings, NBTI-aware digital LDO can achieve up to 42% voltage droop and 43.2% transient response time degradation mitigation.

BTI also leads to control loop degradation of digital LDOs, specifically propagation delay degradation of the control loop, which is not desirable for steady state performance. It is demonstrated through simulations that the propagation delay degradation can be small as compared to half clock cycle of typical digital LDO clock signal such that reduced clock pulse width triggering can be implemented to further reduce the mode and amplitude of steady state limit cycle oscilla-

tions especially at light load conditions. Up to three times steady state digital LDO performance improvement is achieved.

Error rate of a certain functional block is largely affected by the supply voltage level. Aging can lead to the degradation of on-chip voltage noise profile and further the degradation of error rate. Algorithmic noise tolerance of different functional blocks can vary. Meanwhile, additional area overhead is needed to mitigate aging induced on-chip voltage regulator performance degradations. Higher algorithmic noise tolerance of a certain functional block can be leveraged to reduce area overhead and allow more on-chip voltage noise degradations. The desired error rate can also be maintained. Area overhead reduction may further enable increased number of distributed voltage regulators for functional blocks that may have lower level of algorithmic noise tolerance.

CHAPTER 6:

FUTURE WORK

6.1 Co-Optimizing Different Design Aspects to Avoid Overdesign

High performance on-chip power delivery network involves different design aspects such as power conversion efficiency, thermal issue, and reliability. Different application scenarios and environments may impose different design targets and specifications. Power conversion efficiency, thermal issue, and reliability can be mutually affected and should be considered as a whole to realize optimal design and avoid overdesign. For example, power conversion efficiency can be a function of temperature. Reliability can be largely affected by temperature. Implementation of thermal mitigation techniques may need to sacrifice power conversion efficiency. Reliability enhancement techniques can also introduce additional power and area overhead. Depending on the targeted lifetime, power efficiency requirement, and on-chip temperature profile, appropriate efficiency boost technique, thermal emergency mitigation technique, and aging mitigation technique need to be adopted. Furthermore, algorithmic noise tolerance capability of different functional blocks needs to be considered. A generic design flow considering different design aspects and trade-offs among them will be considered in our future work.

6.2 NBTI-Aware Digital LDO with Adaptive Gain Scaling Control

Unidirectional shift register that can activate or deactivate a single power transistor per clock cycle is proposed in our recent work [4, 130] to mitigate NBTI induced digital LDO performance degradations. Digital LDO with improved transient performance [141] has been proposed to achieve faster response time by turning on or off more number of power transistors per clock cycle during the load transient. However, bidirectional shift register is utilized in [141] that can lead to the heavy

use of a portion of power transistors. The unidirectional shift register proposed in [4, 130] cannot be directly applied to digital LDOs with adaptive gain scaling control capability. Novel NBTI-aware digital LDO with adaptive gain scaling control capability will be proposed in our future work to mitigate NBTI induced performance degradations.

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APPENDICES

Appendix A: Copyright Notices

The following notice is for the material in Chapter 2.

Appendix A (Continued)

The following notices are for the material in Chapters 3 and 4.

Appendix A (Continued)

92

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