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Improving Doping and Minority Carrier Lifetime of CdTe/CdS Solar Cells by in-situ Control of CdTe Stoichiometry

by

Vamsi Krishna Evani

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
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Keywords: Photovoltaics, Intrinsic Doping, Open Circuit Voltage, Elemental Vapor Transport

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Dedication

I dedicate this dissertation to my grandparents Mr. C.B. Rao, Mrs. C. Vardhani
and my Mom, Hima Bindu

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I am forever grateful and indebted to my maternal grandparents, Mr. C.B. Rao and Mrs C. Vardhani for everything they have done to make me what I am today. I thank my Mom, my best friend and guide, for always being there for me. I also thank my sister, Sriya, for all her love. I could not have done any of this without their backing.

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Table of Contents

List of Tables iv

List of Figures v

Abstract viii

Chapter 1: Introduction 1
- 1.1 PV Technologies 1
  - 1.1.1 Wafer Based PV 1
    - 1.1.1.1 Crystalline Silicon 1
    - 1.1.1.2 GaAs Solar Cells 2
    - 1.1.1.3 III-V Multi-junction Cells 3
  - 1.1.2 Commercial Thin Films 3
    - 1.1.2.1 Amorphous Si 4
    - 1.1.2.2 CdTe 4
    - 1.1.2.3 Copper Indium Gallium Diselinide 4
  - 1.1.3 Emerging Thin Film PV's 5
    - 1.1.3.1 Dye-Sensitized Solar Cells (DSSC) 5
    - 1.1.3.2 Perovskites 5
- 1.2 Why CdTe? 5

Chapter 2: Semiconductors and Solar Cells 8
- 2.1 Semiconductors 8
- 2.2 P.N Junction 8
  - 2.2.1 Homojunction under Equilibrium 8
  - 2.2.2 Homojunction under Forward and Reverse Bias 9
- 2.3 Heterojunction 10
- 2.4 Solar Cells 11
  - 2.4.1 Solar Spectrum and Air Mass 11
  - 2.4.2 Solar Cell Operation 12
  - 2.4.3 Solar Cell Parameters 13

Chapter 3: CdTe Technology 16
- 3.1 Current Status 16
- 3.2 Future Potential 16
- 3.3 Strategies to Improve Open Circuit Voltage (V_{OC}) 18
  - 3.3.1 Improvement of Back Contact 18
  - 3.3.2 Improving Acceptor Concentration and Lifetime 19
  - 3.3.3 Key Points 20

Chapter 4: p-type Doping and Lifetime Limitations in CdTe 21
- 4.1 Defects in Semiconductors 21
  - 4.1.1 Native Intrinsic Defects 21
  - 4.1.2 Impurity Defects 22
- 4.2 Defects in CdTe 22
  - 4.2.1 Intrinsic Defects 22
  - 4.2.2 Impurity Related Defects 23
  - 4.2.3 Role of Native Point Defects in CdTe 23

4.3 Theoretical Study of Defects in CdTe 24
4.3.1 Transition Energies of Intrinsic Defects 27
4.3.2 Compensation by Intrinsic Defects 27
4.3.3 Lifetime Limiting Defects 28
4.3.4 P- Doping: Group I Dopants 29
4.3.5 P- Doping: Group V Dopants 30
4.3.6 Cu and Cl Related Defects 31
4.4 Summary of Theoretical Studies 32
4.5 Experimental Study of Native Defects in CdTe 33
4.6 Doping CdTe through Stoichiometry Control: Previous Experimental Work 33
4.6.1 Control of Stoichiometry by Varying Substrate Temperature 33
4.6.2 Stoichiometry Change by Stacked Elemental Layer Method 34
4.6.3 Vapor Growth of CdTe from Elemental Cd and Te 34
4.6.4 Te-rich Films by CSS Method 35
4.6.5 Cd Self-Sputtering of CdTe 35
4.7 Motivation and Objectives 35

Chapter 5: Experimental Methods 36
5.1 Cell Fabrication 36
5.1.1 Glass 36
5.1.2 Front Contact (Transparent Conducting Oxide) 37
5.1.3 Window Layer 38
5.1.4 CdTe Layer 39
5.1.4.1 Elemental Vapor Transport 40
5.1.5 $CdCl_2$ Heat Treatment 41
5.1.6 Back Contact 42
5.1.6.1 Etching the CdTe Surface 42
5.1.6.2 Back Contacts 43
5.2 Device Characterization 44
5.2.1 I-V Measurements 44
5.2.2 Spectral Response 44
5.2.3 Temperature-Resistivity Measurements 44
5.2.4 Capacitance-Voltage Measurements 45
5.2.5 Time Resolved Photoluminescence (TRPL) 46
5.2.6 Deep Level Transient Spectroscopy (DLTS) 46
5.2.7 Morphology and Structure Analysis 47

Chapter 6: Results 49
6.1 Introduction 49
6.2 Ratio Calculations 50
6.3 Initial Results on Alumina Substrate 51
6.3.1 Elimination of Powdery Deposits 51
6.3.2 Film Morphology 52
6.3.3 Effect of Stoichiometry on Film Conductivity 52
6.3.4 Summary of Key Findings from Results on Alumina Substrate 55
6.4 Initial Results on ‘CdS/TCO/Glass’ Substrates 55
6.4.1 Introduction 55
6.4.2 Mass Transport 55
6.4.2.1 Effect of Elemental Zone Temperature 56
6.4.2.2 Effect of Elemental Flowrate 56
6.4.2.3 Effect of Mixing Zone Flowrate 56
6.4.2.4 Effect of Cd/Te Ratio 57
6.4.2.5 Thickness Profile 58
6.4.3 Structural Analysis 58
6.4.3.1 XRD Analysis 58
6.4.3.2 SEM Analysis 59

6.4.3.3 TEM and EDX Analysis 60
6.4.4 Summary of Key Findings from Structural Analysis 61
6.5 Solar Cell Fabrication 61
6.5.1 Cell Performance: As-Deposited Films (Without $CdCl_2$ HT) 61
6.5.2 Cell Performance: With $CdCl_2$ HT 62
6.5.3 Cell Performance: Flow Rate as the Control Variable 65
6.5.4 Summary of Key Findings from Cell Performance with Variable Flow Rates 66
6.6 Adhesion Issue 67
6.6.1 Introduction 67
6.6.2 Reduced Ratio Window 68
6.6.3 2 Layered Depositions 70
6.6.4 Summary of Key Findings from Adhesion Issues 71
6.7 Cu Effects 72
6.7.1 Introduction 72
6.7.2 Experimental Details and Results 73
6.7.3 Summary of Key Findings from Cu Dose vs. Cd/Te Ratio Experiments 75
6.8 Minority Carrier Lifetime Measurements 75
6.8.1 Measurement Technique 75
6.8.2 Observations and Results 76
6.8.3 Carrier Lifetimes: Discussion 76
6.8.4 Summary of Key Findings on the Effect of Cd/Te Ratio and Cu on Lifetimes 78
6.9 Alternate Strategies to Improve V_{OC} 79
6.9.1 Saturation Limit for Te-rich Growth Conditions 79
6.9.2 Annealing CdTe in Cd and Te Ambient 79
6.9.3 Absorber Grading 81
6.9.4 Summary of Key Findings from Alternate Strategies to Improve V_{OC} 84
6.10 Effects of Substrate Temperature 84
6.10.1 Introduction 84
6.10.2 Observations and Results 84
6.10.3 Summary of Key Findings from Increased Substrate Temperature 87
6.11 Deep Level Transient Spectroscopy 87
6.11.1 Introduction 87
6.11.2 Observations and Results 88
6.11.2.1 DLTS on CSS CdTe Films 88
6.11.2.2 DLTS on EVT-CdTe Films 91
6.11.3 Summary of Key Findings from DLTS Experiments 94

Chapter 7: Conclusions and Future Work 95
7.1 Conclusions 95
7.2 Ongoing and Future Work 97

References 99

Appendix A: Copyright Permissions 111
A.1 Permission for Figure 10 111
A.2 Permission for Figure 14 112
A.3 Permission for Figure 15 114
A.4 Permission for Figure 17 116
A.5 Permission for Figure 18 118
A.6 Permission for Figure 20 120

List of Tables

Table 1: Efficiencies of CdTe champion cells over the past two decades 16

Table 2: List of native point defects that can form in CdTe 22

Table 3: Examples of substitutional defects in CdTe 23

Table 4: Summary of theoretical defect calculation studies reported by various groups 25

Table 5: Ease of formation of various defects at Cd-rich and Te-rich conditions 32

Table 6: Experimentally determined defect transition energies of CdTe intrinsic defects by various groups 33

Table 7: Properties of popular TCO and buffer layers used in CdTe/CdS solar cells 37

Table 8: Temperatures and flowrates for the Cd and Te zones used in this study 51

Table 9: V_{OC}, FF and J_{SC} for cell with Cd/Te ratio 0.5 and different $CdCl_2$ HT 64

Table 10: V_{OC} of different deposition ratio CdTe cells with their measured carrier concentration and minority carrier lifetime 77

Table 11: CSS CdTe device parameters with different $CdCl_2$ HT and Cu 90

Table 12: EVT-CdTe device performance with different Cu 91

Table 13: EVT-CdTe device parameters with different Cd/Te ratio and different Cu 94

List of Figures

Figure 1:	Efficiency chart of various PV technologies	6
Figure 2:	p and n-type semiconductors before contact (left & center), p-n junction at equilibrium (right)	9
Figure 3:	p-n junction under forward bias (left) and reverse bias (right)	10
Figure 4:	Heterojunction before and after contact (left and right)	11
Figure 5:	Solar spectrum under AM 0 and 1.5 conditions	12
Figure 6:	Band structure of n-CdS and p- CdTe solar cell	13
Figure 7:	I-V characteristics of a p-n junction in dark and light	14
Figure 8:	Equivalent circuit of a solar cell	15
Figure 9:	J_{SC}, FF and V_{OC} improvement for champion cells.	17
Figure 10:	Q.E curves for champion cells	18
Figure 11:	wxAMPS simulation of V_{OC} dependence on doping concentration and lifetime	19
Figure 12:	Unit cell of CdTe	22
Figure 13:	Defect transition energies of native CdTe defects calculated by various groups.	26
Figure 14:	Formation energies of native point defects in CdTe	27
Figure 15:	Mid-gap states in CdTe which limit carrier lifetimes	28
Figure 16:	Formation energies of Group I dopants in CdTe	29
Figure 17:	Formation energy of Group V dopants in CdTe (left); AX center formation (right)	30
Figure 18:	Formation energy of Cl and Cu related defects in CdTe (left and right respectively)	31
Figure 19:	Superstrate CdTe solar cell configuration	36
Figure 20:	Phase diagram of CdTe	40
Figure 21:	Schematic of the Elemental Vapor Transport	41
Figure 22:	Capacitance transient on a reverse biased p-n junction due to carrier injection	47
Figure 23:	XRD plot for EVT-CdTe films with different CdTe ratios	52

Figure 24: SEM images of EVT-CdTe on Alumina with Cd/Te ratios 53

Figure 25: Resistivity vs. 1000/T for EVT-CdTe films deposited at different Cd/Te ratios and doped with Cu 53

Figure 26: Room temperature resistivity Vs Cd/Te ratio 54

Figure 27: Growth rate as a function of Cd zone temperature, elemental flowrate and mixing zone flowrate 57

Figure 28: Growth rate as a function of Cd/Te ratio (left); thickness (in microns) profile on the substrate (right) 58

Figure 29: XRD plots for EVT-CdTe ratios 0.3, 0.5, 1.0 and 2.0 59

Figure 30: SEM images for Cd/Te ratios 0.3, 0.5, 1.0 and 2.0 (clockwise from left) 60

Figure 31: TEM images for as-deposited excess Te film (left) and excess Cd film (right) 60

Figure 32: SR for EVT-CdTe without $CdCl_2$ 62

Figure 33: JV and SR for EVT CdTe ratios 0.5, 1.0 and 2.0 $CdCl_2$ HT at 390° C 63

Figure 34: V_{OC}'s Vs Cd/Te ratios for various $CdCl_2$ annealing temperatures 64

Figure 35: EDX map for Cd (left) and O (right) and Cl segregation at grain boundaries and S diffusion for as-deposited EVT film deposited in excess Te conditions 65

Figure 36: JV and Q.E. curves for Cd/Te ratios 0.8, 1.0 and 1.6 where the ratio was changed using flowrates 66

Figure 37: Variation in V_{OC} for cells on the same substrate for ratios 0.5 and 2.0 67

Figure 38: SEM cross sections for Cd/Te ratios 0.5, 2.0 68

Figure 39: SEM cross section for ratio 0.7 film 68

Figure 40: JV and SR for Cd/Te ratios 0.7, 1.0 and 1.4 69

Figure 41: Doping concentrations Vs Cd/Te ratios (left) for different $CdCl_2$ annealing temperatures 69

Figure 42: SEM cross section images for Cd/Te ratios 0.7, 0.5 and 0.3 with a starting layer of ratio 1.0 70

Figure 43: JV curve for Cd/Te ratio 0.7 with starting layer of ratio 1.0 and 2.0 71

Figure 44: Variation in V_{OC} for cells on the same substrates for Cd/Te ratio 0.5, 0.7 and 0.7 with a starting ratio of 1.0 72

Figure 45: JV (left) and SR (right) for Cd/Te ratio 0.7 and 5 Å Cu 73

Figure 46: Change of V_{OC} with different Cu concentrations (left) SR for Cd/Te ratio 0.7 with varying Cu (right) 74

Figure 47: Carrier concentrations (left) and doping profile (right) for Cd/Te ratios 0.7, 1.0 and 1.4 with different Cu concentrations (left) 74

Figure 48: Lifetimes for Cd/Te ratios 0.7, 1.0 and 1.4 with various Cu concentrations (left); TRPL data for Cd/Te ratio 0.7 (right) 76

Figure 49: JV curves (left) and V_{OC}, FF for extreme Te-rich conditions 79

Figure 50: JV and SR for CSS-CdTe films annealed in Te over pressure 80

Figure 51: JV and SR for CSS-CdTe films annealed in Cd over pressure 81

Figure 52: Simulated JV curve for graded CdTe devices 82

Figure 53: JV and SR for EVT-CdTe films with absorber grading 83

Figure 54: Doping profile for EVT-CdTe with graded absorbers 83

Figure 55: Q.E. curve for Te-rich CdTe films deposited at high temperatures showing CdS thinning 85

Figure 56: JV curves and doping profiles for EVT-CdTe films deposited at high temperatures 86

Figure 57: Carrier lifetimes for EVT-CdTe films deposited at high temperatures with and without Cu 87

Figure 58: Current-voltage measurements (left) and doping profile (right) for CdTe devices with different $CdCl_2$ treatment and Cu doping 88

Figure 59: DLTS spectra of a CdS/CdTe without $CdCl_2$ (left) and with $CdCl_2$ (right) 89

Figure 60: DLTS spectra for CdS/CdTe with $CdCl_2$ HT and 2Å Cu (left) and with $CdCl_2$ HT and 10 Å Cu (right) 90

Figure 61: DLTS for EVT-CdTe with different ratios $CdCl_2$ HT and no Cu 92

Figure 62: DLTS for EVT-CdTe with different ratios with $CdCl_2$ HT and 2Å Cu. 93

Figure 63: Simulated and measured values for the highest carrier concentrations and lifetimes measured in this study 96

Abstract

Cadmium Telluride (CdTe) is a leading thin film photovoltaic (PV) material due to its near ideal bandgap of 1.45 eV and its high optical absorption coefficient. Advancements in efficiencies of CdTe/CdS solar cells over the past few decades have come from improving the short circuit current (J_{SC}) and Fill Factor (FF) but the Open Circuit Voltage (V_{OC}) has been stagnant. Further improvements in efficiencies should come from increased V_{OC}'s. V_{OC}'s can be improved by increasing the acceptor concentration and minority carrier lifetime. Both these parameters can be controlled by manipulating the native defect concentration in CdTe which can be achieved by varying CdTe stoichiometry.

In this study, a deposition system called Elemental Vapor Transport was used to vary the CdTe stoichiometry with an intent to change the native defect concentration and therefore pave way to increase acceptor concentration and lifetimes. Elemental cadmium and tellurium were heated in dedicated zones and their vapors were transported to the substrate using a carrier gas. By varying the temperatures and flowrates of the carrier gas through the zones, the gas phase Cd/Te ratio was varied to deposit Cd-rich, Te-rich and stoichiometric films.

Structural properties were investigated using Scanning Electron Microscopy (SEM), X-Ray Diffraction (XRD), and Transmission Electron Microscopy (EDS). Electrical characterization of completed devices was carried out by Current-Voltage (J-V), Capacitance-Voltage (C-V), and Spectral Response (SR) and Deep Level Transient Spectroscopy (DLTS) measurements.

Cd-rich films showed smaller grain sizes and lesser degree of preferential orientation. Te-rich films showed increased acceptor concentration and carrier lifetimes and solar cells fabricated using these films showed higher V_{OC}'s compared to Cd-rich and stoichiometric films .Higher degree of CdTe-CdS mixing was observed at the interface for films deposited at increased substrate temperatures.

Chapter 1: Introduction

Renewable energy from wind, sunlight, geothermal heat, biomass and water provide extensive benefits to our climate, health and economy. Global warming emissions trap heat and are steadily increasing the planet's temperature creating detrimental impacts on human life. Electricity production accounts for more than one-third of the U.S. global warming emissions with the majority generated by coal-fired power plants. On the other hand, renewable energy sources produce little or no global warming emissions. Harvesting energy from sunlight is a simple and elegant way to produce electricity. It is one of the cleanest forms of energy which produces no air pollution or hazardous waste, as it does not require fuels to be transported or combusted. It is free and abundant because the source is the Sun [1]. Solar energy is quite evenly distributed across the globe and varies by only a factor of three across densely populated areas [2]. Solar cells (also called Photovoltaic cells) convert light to electricity making use of the photovoltaic effect The PV market is growing rapidly at a rate of over 25% annually [3]

1.1 PV Technologies

The PV technologies can be classified into two main categories as wafer and thin film based.

1.1.1 Wafer Based PV

Three wafer based PV technologies exist today and are discussed below.

1.1.1.1 Crystalline Silicon

The first PV cell capable of generating 'sufficient' power to run electronic equipment from sunlight was demonstrated by Daryl Chain and Calvin Fuller using Silicon in 1954 [4]. The efficiency of the first reported Si solar cell was 6%. Since then, substantial advancements have been made and current efficiencies have reached 26.3% [5]. Today, Si solar cells constitute about 90% of the current global production capacity and are considered the most mature of all the PV technologies [15]. Si solar cells can be classified as single crystalline and multi crystalline. The market shares in 2014 were 35% for single and 55% for multi crystalline solar cells.

1. Mono (single) Crystalline

As the name indicates, these cells are made from single crystals of Silicon (Si). Cylindrical single crystals are grown by the Czochralski or the float zone methods [6,7]. The cells are then sliced from large crystals grown under controlled conditions. The production costs for this type of Si are quiet high making it the most expensive PV technology. Current record efficiencies are at 26.3% for small area cells and 22.4% for large area modules [5].

2. Multi-Crystalline Si

These cells are made of multi-crystalline Si wafers. The processing cost is lower than their single crystal counterparts. They are typically produced by cooling graphite mold filled with molten silicon [8].The cells have randomly oriented grains sizes of around 1 cm^2 area. The random orientation of grains gives rise to grain boundaries which produce defects which are detrimental for charge collection. This causes the cells to have lower efficiencies than single crystal Si cells. Current record efficiencies are at 20.8% for small area cells and 18.5% for large area modules [5].

Si has an indirect bandgap and therefore a low absorption coefficient. Both these qualities are not ideal for efficient conversion of light to electricity. In order to compensate these limitations, a very thick layer of the Si wafer is needed to absorb most of the incident light. Typical wafer thicknesses are about 100 – 300 μm which adds to the high processing cost of Si, increasing the overall price of the module. In crystalline Si solar cells, the cost of Si constitutes 40% of the final module price [9]. In addition to increasing the thickness of the Si layer, the surface is textured into a pyramid like structures, which reflect light off the edges increasing the path length of the light resulting in increased absorption. This process is called light trapping and is utilized by most commercial modules available today [10]. Key innovations such as backside contacting [11] and laser grooving [12] are also commonly used to improve efficiencies of Si solar cells.

1.1.1.2 GaAs Solar Cells

GaAs is an III-V semiconductor whose material properties make it an attractive candidate for PV applications. Its direct bandgap, which is well matched to the solar spectrum, coupled with strong absorption has led to efficiencies of 28.8% for small area cells and 24.1% for modules [13, 5]. However, the high manufacturing costs for these cells have limited their usage to space applications and concentrated solar power cells (discussed below). The most expensive component of these solar cells is the GaAs parent

wafer, which is grown by epitaxy. Recent advancements have reduced the costs by using a technique called epitaxial liftoff which creates very thin layers of GaAs from the parent wafer allowing the wafer to be used multiple times [14]. Nevertheless, the cost of this technology is high even when compared to single crystal Si solar cells [15]. Presently these cells are predominantly used in space applications.

1.1.1.3 III-V Multi-junction Cells

The use of multiple junctions can improve the efficiencies of the cells dramatically. Multiple junctions (also called sub cells) are stacked on the top of each other and each sub cell absorbs light from specific region of the solar spectrum. The sub cells are arranged in such a way that the light is incident on the material with the largest bandgap. The bandgaps of the materials decrease as light travels away from the point of incidence. The conversion efficiency increases with the number of sub cells. The maximum theoretical efficiency that can be obtained by a single junction cell is close to 33%. For a cell with 2 junctions, this limit increases to 54%, and for a theoretical infinite number of junctions, the limit reaches 86%. III-V semiconductors made of (Al,Ga,In) and N,P,As, Sb can form high quality crystalline films with variable bandgaps leading to efficiencies up to 46% for a 4 junction cell [16].

The solar cell parameters namely Open Circuit Voltage (V_{OC}), Short Circuit Current (J_{SC}) and Fill factor (FF) (to be discussed later) increase with increasing the light intensity resulting in a rise in efficiency. The light intensity can be increased by using solar concentrators. These systems make use of mirrors and lenses to concentrate solar power over a larger area to a smaller surface. The increased intensity of light reduces the cell area required and therefore the overall cost. Currently, GaAs solar cells and multiple junction solar cells are dominantly used in concentrated systems and space applications with some pilot lines in terrestrial applications due to high cost

In summary, the leading PV technology is Si with a 90% market share. The other wafer based PV technologies are currently limited to space applications sue to the cost involved in the manufacture.

1.1.2 Commercial Thin Films

The remaining 10% of the PV market is constituted mainly by thin film solar cells. These are made of very thin absorber layers compared to that of Si solar cells. Typically the absorber thicknesses for Si solar cells are in the range of 300 to 400 microns while thin film solar cells have absorbers in the range of few microns due to high absorption coefficients. The reduced thickness decreases the overall capital cost

of production making this technology a low cost alternative to Si PV technology. Unlike the wafer-based cells, these cells are deposited on glass, plastic or metal substrates. Thin films can be subdivided into commercial thin film and emerging thin films. They are the low cost alternative to crystalline Si solar cells. Key Thin film technologies include the following.

1.1.2.1 Amorphous Si

Amorphous Si offers a better absorption than crystalline Si. However, its larger bandgap (1.7-1.8 eV) does not match the solar spectrum well [17,18]. As a result, these cells exhibit lower efficiencies. They are typically deposited by plasma enhanced chemical vapor deposition (CVD) at low substrate temperatures [17]. These cells are well suited for low power applications such as calculators as they are prone to light-induced degradation. Their efficiencies are limited to 13.4% for a triple junction cell [13] which is not encouraging for commercial scale manufacturing. Moreover, these solar cells are known to degrade upon exposure to light causing serious stability issues making it undesirable for commercial applications [19]. This technology is on a decline due to lowering costs of other commercial PV technologies.

1.1.2.2 CdTe

CdTe is the leading thin film PV technology on the market today. It has a market share of 5% in the global PV market and a 56% share in the thin film market as of 2013 [20]. With an ideal bandgap of 1.45 eV and a very strong absorption coefficient CdTe is an ideal candidate for PV applications. It offers the lowest module costs compared to any other PV technology on the market today. Toxicity of Cadmium (Cd) and scarcity of tellurium (Te) are concerns with respect to this technology. Current record efficiency is at 21.5% and has surpassed the efficiency of multi-crystalline Si solar cells [5].

1.1.2.3 Copper Indium Gallium Diselinide

Copper indium gallium diselinede ($CuIn_xGa_{1-x}Se_2$ or CIGS) is a compound semiconductor with a direct bandgap of 1.1-1.2 eV [16]. It has a market share of 2% and a thin film market share of 22%. While laboratory results have been promising, large scale production was found to be extremely difficult due to the complex stoichiometry. The advantage however this technology has over CdTe is that it uses lower amounts of Cd or none at all.

1.1.3 Emerging Thin Film PV's

Emerging PV technologies employ nano-structured materials that can be engineered to achieve the desired optical and electronic properties [16]. These technologies offer low cost fabrication that attract commercial scale production.

1.1.3.1 Dye-Sensitized Solar Cells (DSSC)

DSSC are considered to be the pioneer in the emerging thin film market and are currently regarded as the most mature of nanomaterial-based PV technology. These were invented by Michael Graetzel and are commonly referred as the Graetzel cells [21]. They employ an organic dye, which can produce electricity when exposed to light. Charge separation is achieved using a transparent inorganic paste, typically TiO_2. Charge conduction is achieved through an electrolyte. DSSC's have achieved efficiencies up to 11.9% and 8.8% at the cell and module level respectively [5]. However, the use of liquid electrolyte causes problems such as instability, risk of evaporation and a limited operating temperature [22] and have paved way for the innovation of pervoskites.

1.1.3.2 Perovskites

Perovskites cells have evolved from DSSC's and are the fastest growing PV technology achieving an efficiency up to 20.1% in less than 3 years of their development [23].A perovskite solar cell includes a perovskite structured compound, most commonly a hybrid organic-inorganic lead or tin halide-based material, as the light absorber. The term "perovskite" refers to the ABX_3 crystal structure, and the most widely investigated perovskite for solar cells is the hybrid organic–inorganic lead halide CH_3NH_3-$Pb(I,Cl,Br)_3$ [16]. Key advantages of this class of material include low materials and manufacturing cost. In addition, the bandgap of these materials can be easily tuned to match the solar spectrum. Key challenges include high sensitivity to moisture, phase separation and the use of toxic lead [24]. This technology is in its early stages of commercialization and there further research is needed to ascertain stability. Figure 1 shows the efficiencies of various PV technologies commercially available in the market today. [25]

1.2 Why CdTe?

The choice of materials for PV applications is based on the following requirements [26]:

1. A direct bandgap material in the range of 1-1.5 eV for maximum photovoltaic conversion
2. A high optical absorption coefficient (10^4-10^5 cm^{-1}) in the wavelength region of 300-1000nm

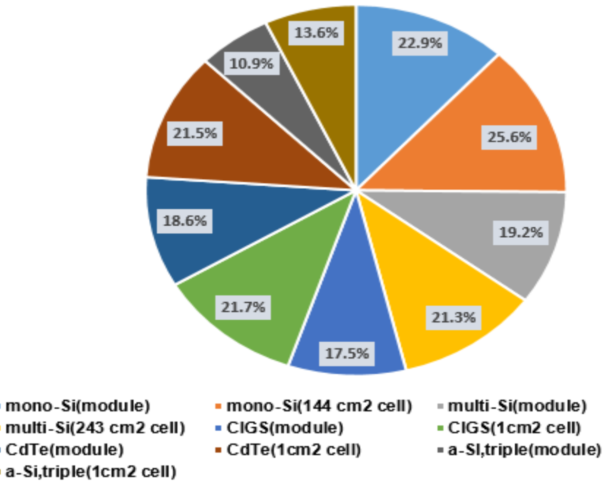

Figure 1: Efficiency chart of various PV technologies [25]

3. The ability to form both p and n-type materials

Si has a low absorption coefficient because of its indirect bandgap, therefore a very thick absorber layer is necessary to absorb all of the incident light [27]. However, Si solar cells have emerged to being the natural first choice for PV applications due to the vast advancements in the manufacturing process. Research on low cost alternatives to Si revealed that many III-V and II-VI compound semiconductors meet the above mentioned criteria. However, only CdTe cells have shown great potential for replacing silicon solar cells for commercial terrestrial applications with compound semiconductors like GaAs, CdSe, InP having very high manufacturing costs [28]. Today the efficiency of CdTe solar cells has surpassed that of multi-crystalline Si. CdTe is a widely renowned photovoltaic absorber whose attractive properties have made it one of the leading PV technologies in the world today. An ideal bandgap of 1.45 eV and its high optical absorption coefficient of 10^4 cm^{-1} make it one of the best choices for absorbers in PV technology. Using the relationship E= hc/λ, (where E is the energy, h is the plank's constant, c is the velocity of light and λ is the wavelength) a bandgap of 1.45 eV translates to an absorption edge of 850 nm. This implies that CdTe can absorb light with wavelengths below 850 nm. Therefore, CdTe has the capability to absorb light throughout the visible spectrum (400 to 900 nm). Using Beer-Ambert's law, an absorption coefficient of 10^4 cm^{-1} implies that a 2 μm CdTe film has the capability to absorb 90% of the photons in the visible

spectrum range. However, homojunction CdTe devices are practically not viable due to very high surface recombination velocity. Therefore, CdTe is typically used in conjunction with CdS, which acts as an n-type window layer completing the heterojunction.

Chapter 2: Semiconductors and Solar Cells

2.1 Semiconductors

Semiconductors are materials whose conductivity lies in between those of metals and insulators. In their purest form they are called intrinsic semiconductors and have low electrical conductivity. Their conductivity can be increased by controlled incorporation of impurities and such semiconductors are called extrinsic semiconductors. This process is called doping and the impurities are called dopants. Extrinsic semiconductors can be classified as p-type or n-type depending on the type of impurity added. Si belongs to Group IV of the periodic table and has 4 valence electrons. When doped with a Group V element like Phosphorus (P), an extra electron is added making it n-type. Similarly, a Group III element like Boron (B) adds a hole making Si p-type. N-type dopants increase electron concentrations in the semiconductor and are called donors while P-type dopants increase hole concentrations and are called acceptors. Semiconductors comprised of two or more elements are called compound semiconductors. Examples are III-V semiconductors such as GaAs, GaN and II-VI semiconductors such as CdTe, CdS etc.

2.2 P.N Junction

2.2.1 Homojunction under Equilibrium

A homojunction is formed when a p-type and n-type semiconductors of the same material are contacted. The Figure 2 (left) shows the band diagram of p and n-type semiconductors at equilibrium. The n-type region has a high concentration of electrons and the p-type region has a high concentration of holes. The Fermi energy level is the maximum energy of an electron at 0K which is closer to the valence band (VB) in the p-type semiconductor and to the conduction band (CB) in the n-type semiconductor. When a contact is established between the p and n regions, the majority carriers from the n-region (electrons) diffuse to the p-region. Similarly, the majority carriers from the p-region (holes) diffuse towards the n-region. This diffusion of charge carriers constitutes the diffusion current and leaves behind uncompensated charge of acceptor ions (negative) and donor ions (positive) respectively. The uncompensated charge creates an

electric field, which is called the built-in electric field. This electric field is spread across a region called the depletion region (also called the space charge region) and creates a drift current which is equal and opposite of the diffusion current. The potential caused due to the accumulation of uncompensated charges on either side of the junction is called built-in potential, V_{bi}. Under thermal equilibrium, the Fermi energy is spatially continuous across the p-n junction. As a result, the conduction and valence bands bend by an amount equal to qV_{bi}. This is called the potential barrier and it represents the energy an electron on the n-side has to overcome to go over to the conduction band on the p-side. The band diagram of a p-n junction under equilibrium is shown in Figure 2 (right).

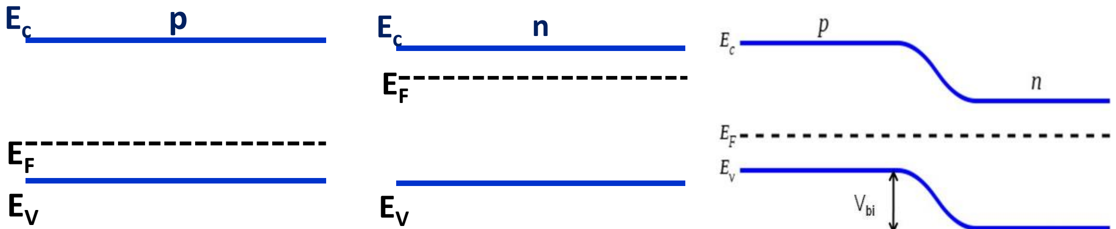

Figure 2: p and n-type semiconductors before contact (left & center), p-n junction at equilibrium (right)

The built-in potential is given by:

$$V_{bi} = \frac{kT}{q} \times ln\left(\frac{N_A N_D}{{n_i}^2}\right) \quad (1)$$

where N_A and N_D are acceptor and donor concentrations in the p and n-type regions, n_i is the intrinsic carrier concentration. K is the Boltzmann constant, and T is the absolute temperature.

2.2.2 Homojunction under Forward and Reverse Bias

When a p-n homojunction is forward biased, the majority of the applied voltage (V_A) drops across the depletion region. Therefore, the potential barrier decreases by an amount equal to the applied voltage. The electrons on the n-side can now readily overcome the barrier to reach the p-side. The band diagram of a p-n junction under forward bias is shown in Figure 3 (left)Under reverse bias, the applied voltage adds to the built-in potential and the electrons on the n-type region have a higher barrier to crossover to the conduction band of the p-type region. The barrier is now given by the following equation:

$$V = (q * [V_{bi} + V_a]) \quad (2)$$

A p-n junction under reverse bias is shown in Figure 3 (right). The current – voltage relationship of a p-n junction in equilibrium is given by equation 3 Where I_0 is the reverse saturation current, A is the diode quality factor, which lies between 1 and 2 which describes the dominant recombination in the junction.

$$I = I_o \times \left(e^{\frac{qV}{AkT}} - 1\right) \quad (3)$$

2.3 Heterojunction

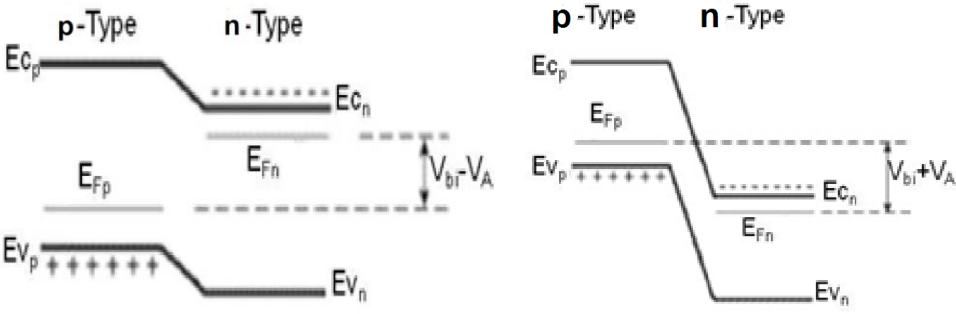

Figure 3: p-n junction under forward bias (left) and reverse bias (right)

Heterojunctions are formed between two different semiconductor materials. They are named Type I, II and III depending on their band alignment.. Figure 4 (left) shows the band diagram of a type I n- p heterojunction before a contact is established. E_{gn} and E_{gp} are the bandgaps, Φ_n and Φ_p are the Fermi levels, and χ_n and χ_p are the electron affinities of the n and p-type semiconductors respectively. When a junction is formed, as in the case of homojunctions, the Fermi energy is constant throughout the material under equilibrium conditions. When the Fermi energies align, discontinuities in the conduction band (ΔE_C) and valence band (ΔE_V) accommodate the difference between the semiconductor bandgaps (ΔE_G). The discontinuities in the conduction and valence bands are given by:

$$\Delta E_C = \chi_P - \chi_n \quad (4)$$

$$\Delta E_V = E_{gP} - E_{gn} - \Delta E_c \quad (5)$$

The total built-in potential V_{bi} is equal by the sum of the partial built-in voltages ($V_{bn} + V_{bp}$), where V_{bn} and V_{bp} are the electrostatic potentials at equilibrium of the n and p semiconductors respectively. The major difference between a homojunction and a heterojunction is the barrier height seen by the carriers (electrons and holes). In the case of a homojunction under equilibrium, the barrier height seen by the

electrons and holes was equal to the built-in potential V_{bi}. Therefore the magnitude of hole and electron currents is determined by the doping levels. In the case of a heterojunction, the barrier is not the same as seen by the electrons and holes due to a difference in the built-in potentials on the n and p sides. The barrier height for electrons in Figure 4 (right) is larger than for holes.

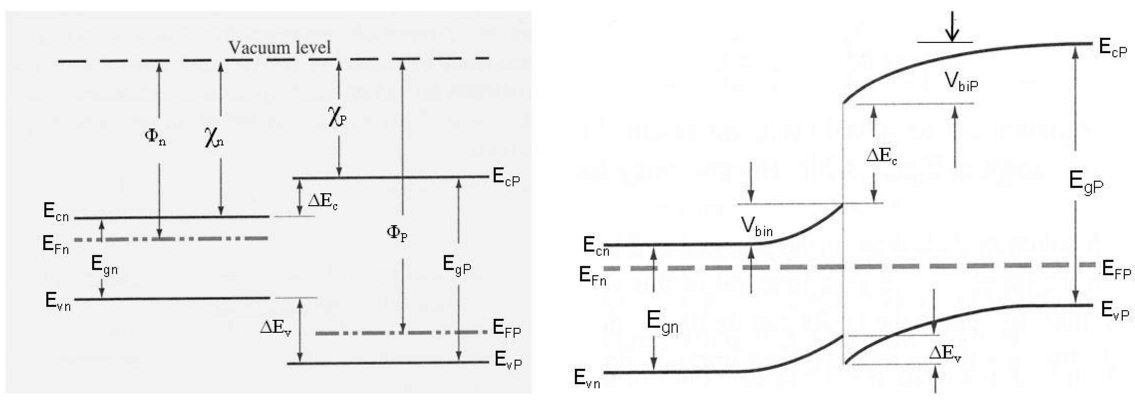

Figure 4: Heterojunction before and after contact (left and right)

2.4 Solar Cells

2.4.1 Solar Spectrum and Air Mass

The power density of the solar radiation incident on the earth is constant outside the atmosphere and expressed in W/m^2. Before the solar radiation reaches the earth's surface, light gets absorbed or scattered due to various constituents of the atmosphere like water vapor, CO_2 etc. In addition to local atmosphere, factors such as the latitude, season and pollution, affect the solar power reaching the earth's surface. This causes a variation in the solar power density, which changes with location. A quantity called Air Mass (AM) is used to quantify the attenuation of solar power density as light passes through the earth's atmosphere. AM is defined as the path length of the sun's radiation normalized to the shortest path. It is given by the formula: AM = 1/cosΘ, where Θ is the angle between the path length at the point of interest and the normal at which sun is at the zenith. AM0 corresponds to the power density in outer space and AM 1.0 refers to the irradiation when the sun is at the zenith. The measured power density at AM0 condition is 1.353kW/m^2 and 1040 W/m^2 at AM1.0. AM 1.5 was chosen to be the global standard to compare solar cell efficiencies measured across the world and has a power density of 844 W/m^2. For convenience, the spectrum was normalized to 1000 W/m^2. Figure 5 shows AM 0 and AM 1.5 spectrum [29].

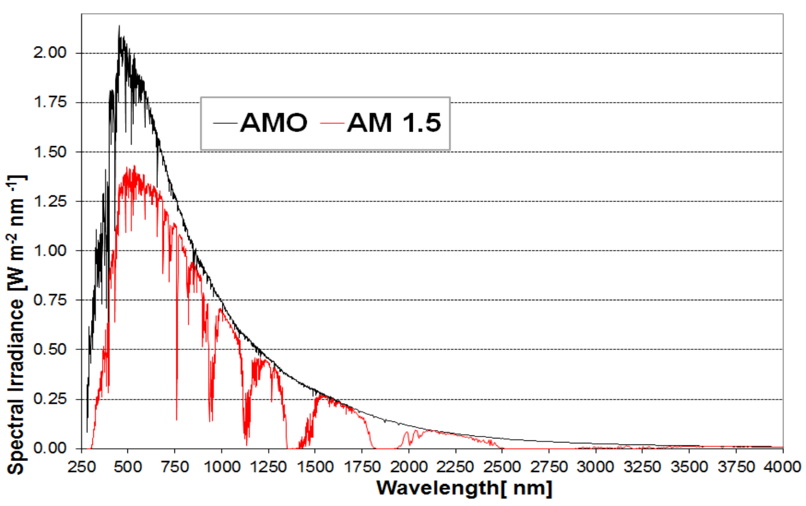

Figure 5: Solar spectrum under AM 0 and 1.5 conditions [29]

2.4.2 Solar Cell Operation

A solar cell is a device that converts light energy to electric energy based on the Photovoltaic effect (PV). The PV effect can be described in 3 steps:

1. Absorption of light
2. Separation of photo-generated charge carriers
3. Collection of photo-generated charge carriers

A solar cell essentially consists of a p-n junction. When photons with energy greater than the bandgap of the semiconductor material are incident, they excite carriers and generate electron-hole pairs. These carriers are called photo-generated carriers and the process is called light absorption. The carriers generated close to the depletion region come under the influence of the built-in electric field and are separated by the field. Finally, the separated carriers are collected by metal contacts at the two ends of the junction.

The heterojunction consisting of a wide-bandgap n-semiconductor, (CdS) and a narrow bandgap p-semiconductor (CdTe) is shown in Figure 6 [30].The wide bandgap semiconductor (represented with subscript 1) is called the window layer and the narrow bandgap semiconductor (represented with subscript 2) is called the absorber. Photons with incident energy less than E_{g1} ($E_{h1} > h\nu$) will pass through the n-CdS layer and only those photons with energy greater than the bandgap (of CdS) will be absorbed. Photons with

energy hv ≥ E_{g2} and less than E_{g1} will get absorbed in the p-type semiconductor (CdTe). Carriers generated within a diffusion length of the junction are collected. Heterojunction solar cells have better efficiencies over their homojunction counterparts due to greater collection in the short wavelength (λ) region. The wider bandgap of the window layer allows more photons (from the short λ region) to enter the absorber layer resulting in more photo-generated carriers.

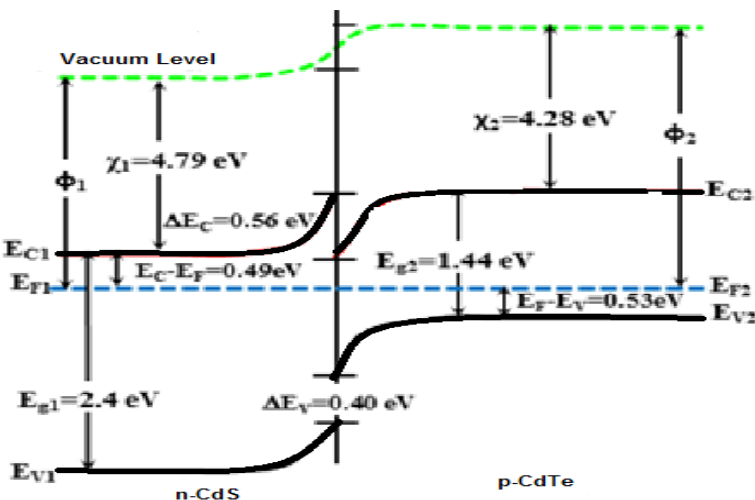

Figure 6: Band structure of n-CdS and p- CdTe solar cell

2.4.3 Solar Cell Parameters

The major performance parameters for Solar Cells are: Open-Circuit Voltage (V_{OC}), Short-Circuit Current (J_{SC}), Fill factor (FF) and Efficiency (η). Figure 7 shows the IV characteristics of a solar cell in the dark and under illumination [31].

The current is given by:

$$I = I_s \times \left(e^{\frac{qV}{AkT}} - 1\right) - I_{Ph} \tag{6}$$

I_S is the reverse saturation current, I_{Ph} is the photo-generated current.

V_{oc} is the voltage output when the attached load is infinite and from equation 5, setting I=0 the equation for V_{oc} is given by

$$V_{oc} = \frac{AkT}{q} \times \ln\left(\frac{I_{ph}}{I_s} + 1\right) \tag{7}$$

The maximum possible area P_{max}= $I_{max} * V_{max}$ for a given current voltage curve determined the FF, which is defined by

$$FF = \frac{V_{max} * I_{max}}{V_{OC} * I_{SC}} \tag{8}$$

The efficiency of the solar cell (η) is calculated by using the three parameters V_{oc}, I_{sc} and FF by the following expression:

$$\eta = \frac{P_{max}}{Pin} = \frac{V_{OC}\, FF\, I_{SC}}{P_{in}} \tag{9}$$

where P_{in}, is the incident light power.

The efficiency of a solar cell is influenced by series (R_s), and shunt (R_{sh}) resistances. For an ideal solar cell the series resistance is zero and the shunt resistance is infinite. All practical devices have finite

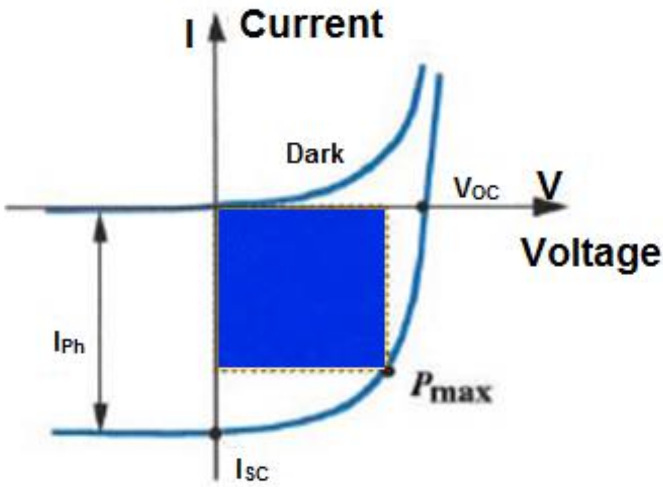

Figure 7: I-V characteristics of a p-n junction in dark and light

series and shunt resistances. By taking the series and shunt resistances into account, the new equation for current is:

$$I = I_s \times \left(e^{\frac{q(V-IR_S)}{AkT}} - 1\right) - I_{ph} + \frac{(V-IR_S)}{R_{Sh}} \tag{10}$$

The series resistance is due to the resistance of the contacts and the bulk of the device material. Defects like pinholes, grain boundaries and dislocations in the solar cell are responsible for low shunt resistance. A low shunt resistance produces high leakage currents which decrease the values of V_{oc} and

FF. Series resistance also reduces the FF. Figure 8 shows the equivalent circuit of a solar cell with series and shunt resistances.

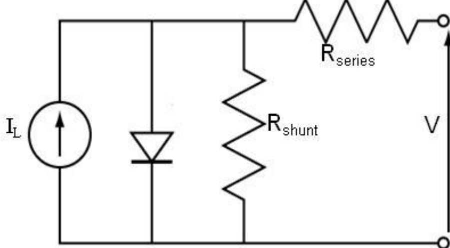

Figure 8: Equivalent circuit of a solar cell

Chapter 3: CdTe Technology

3.1 Current Status

Efforts to improve the conversion efficiency of CdTe solar cells has been active for the past several years. Table 1 shows the champion cell efficiencies achieved by various research groups over this time frame. After a period of stagnation for 10 years (between 2001 and 2011), the CdTe technology has experienced a rapid growth over the past few years. The current record laboratory efficiency is at 21.5% and module efficiency is at 18.5% [32] both held by First Solar, the leading manufacturer of CdTe based PV modules. The highest efficiency at the University level is 18.3% and was achieved by CSU [33].

Table 1: Efficiencies of CdTe champion cells over the past two decades

Year	Team	Efficiency (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Ref.
1993	USF	15.8	843	25.1	74.5	[34]
1997	Matsushita	16.0	840	26.1	73.1	[35]
2001	NREL	16.4	848	25.9	74.5	[36]
2001	NREL	16.7	845	26.1	75.5	[37]
2011	FSLR	17.3	845	27.0	75.8	[38]
2012	GE	18.3	857	27.0	79.0	[39]
2012	FSLR	18.7	852	28.6	76.7	[40]
2013	FSLR	19.0	872	28.0	78.0	[40]
2014	FSLR	21.5	876	30.25	79.4	[5]
2016	CSU	18.3	863	26.8	79.2	[33]

3.2 Future Potential

Considering the theoretical limit for photovoltaic conversion (Shockley- Queisser limit) of 33% there is an opportunity for increasing the efficiency of CdTe devices [41]. The limiting values for the open-circuit voltage (V_{OC}), short-circuit current (J_{SC}) and fill factor (FF) for CdTe Solar Cells were calculated to be

1.156V, 30.5 mA/cm² and 88.7% respectively [42]. The corresponding values for the current champion cell are 887 mV (V_{OC}), 30.3 mA/cm² (J_{SC}) and 78.0% (FF). While the J_{SC} seems to have approached its practical limit, V_{OC} and FF have room for improvement. Fill factors can be improved further by improving the V_{OC} [43]. Therefore, further improvements in efficiency is possible if V_{OC} is increased.

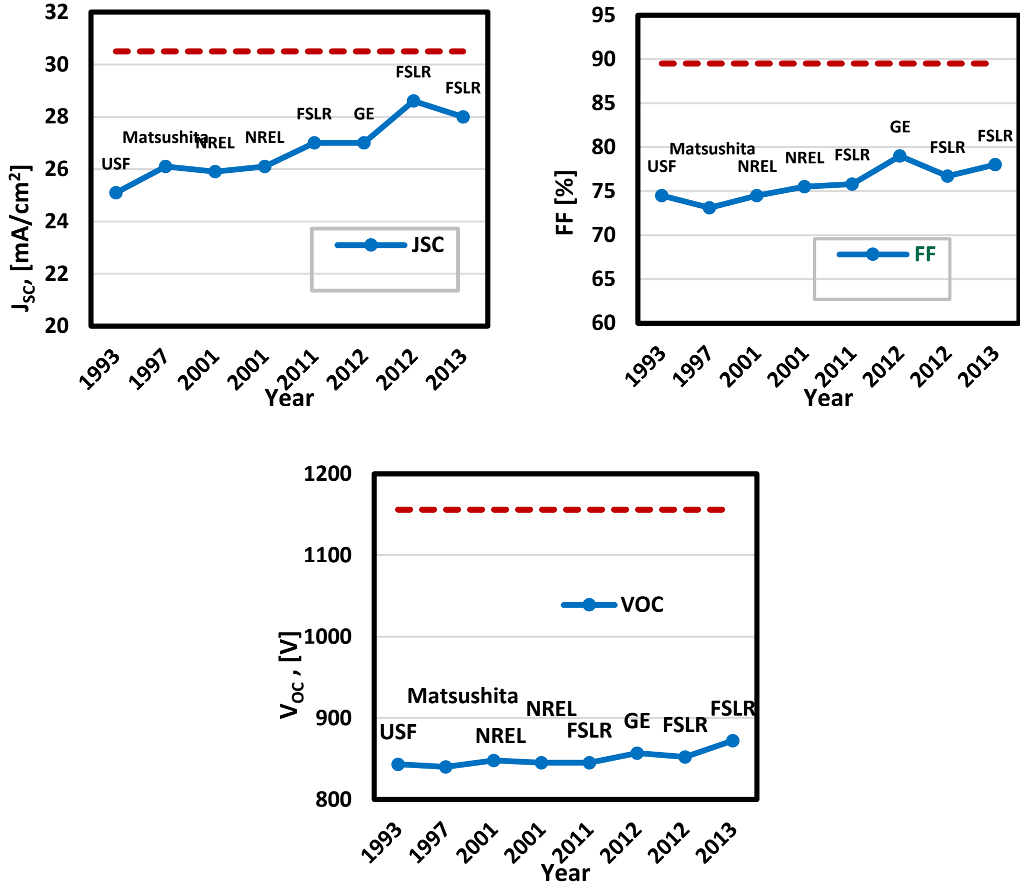

Figure 9: J_{SC}, FF and V_{OC} improvement for champion cells. The red dotted line represents the limiting value

Figure 9 shows the improvement in V_{oc}, FF, J_{sc} for the champion cells. While J_{SC} and FF show constant growth, the V_{OC} seems to have stagnated for the past 20 years. Though V_{OC}'s above 1 volt have been reported recently by employing n-type CdTe [44] and single crystal CdTe [45] as the absorber layer, most high efficiency polycrystalline devices continue to be in the 870-900 mV range. The improvement in J_{SC} can be understood by studying the Q.E. curves for the respective solar cells (Figure 10) [42]. The collection in the shorter wavelength region (λ< 510 nm) has shown a gradual increase over the years. This

is indicative of reduced absorption in the window layer (CdS), which can be achieved by reducing its thickness or by using a replacement to CdS. In addition to reducing window layer absorption, the latest champion device fabricated by First Solar also modified the bandgap of CdTe by incorporating Selenium (Se) to increase absorption above 850 nm [33]. Unlike the case with J_{SC}, factors limiting V_{OC} cannot be understood by analyzing the JV or Q.E. curves. Due to the limited understanding of the complex physics involved with polycrystalline devices, there are no direct measurements available to estimate the limiting factors to V_{OC}. However, a set of parameters called "third level; metrics" have been defined earlier [46] to gain insight into the V_{OC} limiting factors. These metrics break down J_{SC}, V_{OC} and FF to their constituents like carrier lifetimes, acceptor concentrations etc., which can be directly measured and therefore pave the way towards V_{OC} improvement. Based on these metrics, and several other studies the prominent reasons for poor V_{OC}'s in CdTe/CdS solar cells are:

1. Low acceptor (hole) concentrations and minority carrier lifetimes in CdTe layer
2. Non-ohmic back contact
3. Poor interface quality at the CdTe/CdS junction

3.3 Strategies to Improve Open Circuit Voltage (V_{OC})

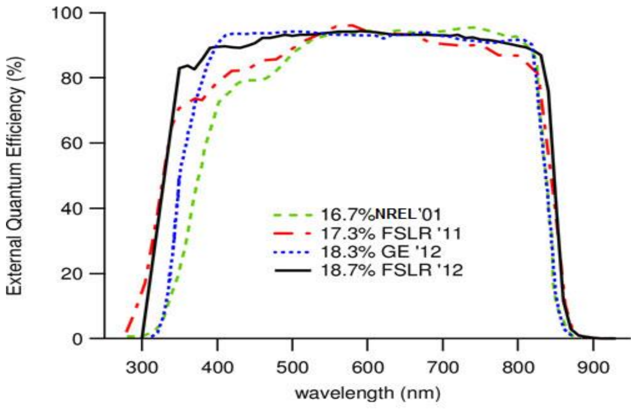

Figure 10: Q.E curves for champion cells [42]

3.3.1 Improvement of Back Contact

Due to the high electron affinity of CdTe, most metals form non-ohmic back contacts to CdTe. The resulting Schottky barrier causes the valence and conduction bands to bend at the back contact. This band bending inhibits hole collection and also increases voltage-limiting recombination and therefore reduces

V_{OC}. A strategy to include an electron reflector layer at the back contact has been suggested to reflect electrons from the back surface and improve V_{OC}'s [47]. This strategy is currently being investigated by various groups using materials like CdMgTe and ZnTe [48,49].

3.3.2 Improving Acceptor Concentration and Lifetime

Major limitations to V_{OC} improvement are the poor acceptor (hole) concentrations and lifetimes in CdTe. As-deposited CdTe films have carrier lifetimes and hole densities on the order of 10^{13} cm^{-3} and pico seconds respectively. During cell fabrication, both these parameters are improved by employing post-deposition treatments (to be discussed later). Nevertheless, the carrier concentrations for the best CdTe/CdS devices are currently in the range of $10^{15}cm^{-3}$ and lifetimes are in the order of a few nanoseconds [46]. These values cannot yield V_{OC}'s beyond the current threshold.

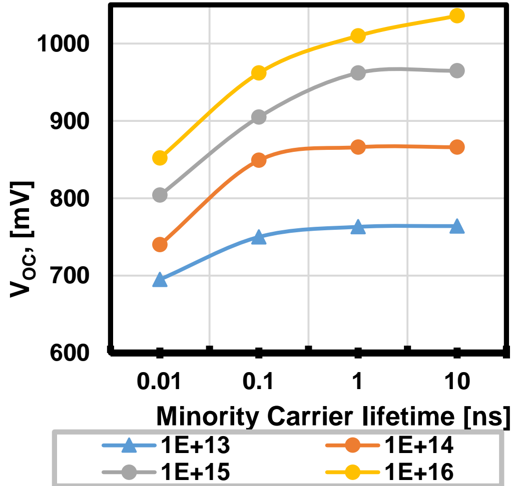

Figure 11: wxAMPS simulation of V_{OC} dependence on doping concentration and lifetime

Figure 11 shows wxAMPS simulation [50] of the V_{OC} dependence on minority carrier lifetime and acceptor concentration in CdTe. The simulations have been performed for a CdTe/CdS solar cell with SnO_2 as the front contact. The mid-gap defect concentration was varied to achieve the desired carrier lifetimes. Improving V_{OC} is noticeably caused by improving the acceptor concentration. As the carrier concentration increases, the role of minority carrier lifetimes becomes increasingly dominant. For carrier concentrations above 10^{15} cm^{-3}, V_{OC} is significantly affected by the minority carrier lifetime. For instance, for a concentration of 10^{13} cm^{-3}, an increase in minority carrier lifetime from 1ns to 10 ns causes the V_{OC} to improve by less

than 3 mV. Whereas, for a concentration of 10^{16} cm^{-3} improving the carrier lifetime from 1ns to 10 ns causes the V_{OC} to improve by about 40 mV. Acceptor concentration levels up to 10^{16} cm^{-3} along with lifetimes above 5 ns are necessary to improve V_{OC} beyond 900 mV.

Though higher acceptor densities yield better V_{OC}'s, improving acceptor concentrations without improving lifetimes may result in the reduction of FF faster than the V_{OC} increase thereby reducing the overall performance [51,52]. Increasing acceptor concentration results in a reduction of the depletion width (space charge region). This causes more light to be absorbed outside the space charge region where the effect of built-in electric field is nonexistent. With little or no electric field to separate the photo-generated carriers, they tend to recombine. However, the carriers can diffuse to a length equal to the diffusion length (L_D) before they recombine. Therefore, the collection in the quasi-neutral region (where there is no effect of the built-in electric field) is limited by diffusion length (L_D) of the carriers. L_D depends on mobility (μ) and minority carrier lifetime (τ), and is given by the equation: $L_D = [kT\mu\tau/q]^{1/2}$. Therefore, improving both the carrier concentration and the minority carrier lifetimes are essential to achieve higher V_{OC}'s and therefore higher efficiencies.

In this study, V_{OC} enhancement through improving carrier concentration and lifetime is investigated. The details regarding implementing this approach will be discussed in the subsequent sections.

3.3.3 Key Points

- Further improvements in efficiencies of CdTe solar cells is possible only by increasing V_{OC}'s
- To improve V_{OC} the acceptor concentration and carrier lifetime need to be improved simultaneously
- Acceptor concentrations of 10^{16} cm^{-3} along with lifetimes > 5 ns are necessary to improve V_{OC}'s beyond the current state of the art devices. Current values are below 10^{15} cm^{-3} (acceptor concentration) and less than 5 ns.

Chapter 4: p-type Doping and Lifetime Limitations in CdTe

As is the case with any semiconductor, carrier concentration can be increased by doping. A major bottleneck in improving the V_{OC} of CdTe solar cells is the difficulty in achieving high p-type doping in CdTe. The main factors that limit p-doping in CdTe are [53]:

1. Low dopant solubility
2. High dopant ionization energies
3. Formation of oppositely charged defect states which compensate p-doping

In CdTe, ‘native defects’ play a major role in influencing the acceptor concentration and lifetimes and hence the V_{OC}. Knowledge of the defect properties is necessary to identify the dominating factors limiting the doping and carrier lifetimes in CdTe.

4.1 Defects in Semiconductors

The crystal lattice consists of periodic arrangement of atoms. Deviation from the perfect single crystal causes ‘defects’ to be formed in the lattice. The presence of defects causes electronic states to be formed within the bandgap. These states can cause major changes in the electrical and optical properties of semiconductors. Therefore, a thorough understanding of defects is necessary to achieve higher V_{OC}’s. Defects can be broadly classified into two categories: a) Native or Intrinsic defects and b) Impurity related defects.

4.1.1 Native Intrinsic Defects

Native defects arise due to disorder of host atoms in the crystal lattice. These defects can be broadly classified as point, line, plane and volume defects. Common native point defects are vacancies, interstitials and antisite defects. Vacancy defects arise when one of the host atoms is missing from its lattice site. An interstitial defect arises when an extra atom tries to occupy a lattice site of the host atom and remains within the lattice due to unavailability of a lattice site. Antisite defects arise when one of the host atoms occupies a lattice site that belongs to another host atom.

4.1.2 Impurity Defects

Defect states can also arise due to impurity incorporation. Impurities may be added intentionally to improve the conductivity by the process of doping. These states can either improve electronic properties such as carrier concentration etc. or form trap states which can be detrimental for carrier transport.

4.2 Defects in CdTe

4.2.1 Intrinsic Defects

CdTe exists in the zinc blende structure with a face centered cubic and hexagonal lattice configuration. The resulting tetrahedron arrangement causes each Cd atom to be surrounded by 4 Te atoms and vice-versa as shown in Figure 12 [54]. Disarrangement of the atoms in the lattice causes many defects to form. A description of all native point defects in CdTe is given in the Table 2 below.

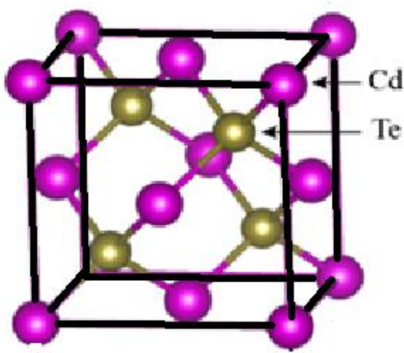

Figure 12: Unit cell of CdTe [54]

Table 2: List of native point defects that can form in CdTe

Notation	Defect Name	Description
V_{Cd}	Cadmium vacancy	Missing Cd atom
Te_i	Tellurium interstitial	Extra Te atom in the lattice
Te_{Cd}	Te at cadmium antisite	Te occupying a Cd lattice site
Cd_{Te}	Cd at Tellurium antisite	Cd occupying a Te lattice site
V_{Te}	Tellurium vacancy	Missing Te atom
Cd_i	Cadmium interstitial	Extra Cd atom in the lattice

4.2.2 Impurity Related Defects

Defects can also be formed due to impurity atoms in the crystal lattice. Substitutional defects, as the name suggests, are formed when the impurity atom occupies a lattice site belonging to a host atom (in this case, Cd or Te). Group I elements such as Copper (Cu) and Group V elements such as Antimony (Sb), by occupying a cadmium vacancy (V_{Cd}) or a Tellurium vacancy (V_{Te}) can form substitutional defects such as Cu_{Cd}, Sb_{Te} respectively. Similarly, Group III elements like Indium (In) can occupy a V_{Cd} to form substitutional defect, In_{Cd}. Impurity atoms can also form interstitial defects like Cu_i and Cl_i etc. In CdTe, substitutional defects can also combine with native defects to form complex defects. An example of a complex defect is an A-center, which is formed when the Cl substitutional defect, Cl_{Te} combines with a V_{Cd} (V_{Cd}-Cl_{Te}).

4.2.3 Role of Native Point Defects in CdTe

CdTe is an amphoteric semiconductor, which can be doped both p and n-type [55]. Doping in CdTe is possible both intrinsically and extrinsically using native point defects. A Cadmium Vacancy defect (V_{Cd}), when doubly ionized forms V_{Cd}^{2+} and contributes two holes to the lattice thereby increasing the acceptor (hole) concentration i.e. p-type conductivity. Similarly, a Cadmium interstitial defect (Cd_i) when ionized forms Cd_i^{-1} and contributes an electron thereby increasing the donor (electron) concentration i.e. n-type conductivity. Therefore, intrinsic doping can be achieved through the creation of native defects such as V_{Cd}'s and V_{Te}'s (p and n-type respectively) or Cd_i and Te_i (n and p respectively). Alternatively p or n-type doping can be achieved with the addition of extrinsic impurities. When the host atom (Cd or Te) is substituted by an element which has one less valence electron (than the host), an acceptor defect is created.

Table 3: Examples of substitutional defects in CdTe

Element	Group	Defect	Type of defect
Cu	I	Cu_{Cd}	Acceptor
Sb	V	Sb_{Te}	Acceptor
Al	III	Al_{Cd}	Donor
Cl	VII	Cl_{Te}	Donor

Similarly, an element with an extra valence electron creates a donor defect by substituting the host atom. For example, Group V elements like Sb can substitute a missing Te atom i.e. V_{Te} (group VI) to form Sb_{Te} which is an acceptor and therefore increase p-type conductivity. Similarly, a Group I element like Cu, can occupy a V_{Cd} (Group I) to form acceptor defect Cu_{Cd}. On the other hand, a group III element occupying a V_{Cd} and a group VI element occupying a V_{Te} would increase the electron concentration and hence n-type conductivity. In order to effectively dope CdTe the conditions must be favorable to incorporate the chosen dopant. To dope CdTe p-type using Group V elements, (which will replace Te or occupy a V_{Te}), it is necessary to create V_{Te}'s in order to create the respective substitutional defects.

It should be noted that defects can create acceptor states and improve conduction, or create trap states and act as recombination centers which limit carrier lifetimes. Examples of substitutional defects in CdTe are listed in Table 3.

4.3 Theoretical Study of Defects in CdTe

The main properties which define a defect are the formation energy and the transition energy (also called ionization energy). The formation energy defines the ease of formation of a defect. The higher the formation energy of a defect, the less likely it is to occur. The transition energy refers to the position of the defect in the bandgap. Defects with smaller ionization (transition) energies are more likely to contribute towards conduction at room temperature.

Many research groups have attempted to quantify the defect properties by using numerical methods. To calculate the defect properties Schrodinger's equation for many electrons is reduced to an effective single electron problem using the Density Functional Theory (DFT). However, the solution to the DFT model is iterative and involves the use of various approximations to converge at the solution. Some of the popularly used approximations under DFT are:

1. Local Density Approximation (LDA)
2. Generalized Gradient Approximation (GGA)
3. Heyd-Scuseria-Ernzerhof: (HSE)

DFT and GGA provide exact information about the ground state defect properties [56] and many initial studies relied on these two approaches to calculate the defect properties. However, these approaches have several shortcomings, the most important of which is the inaccurate estimation of the bandgap. Recently,

the LDA and GGA approximations have been replaced by the computationally intensive and more accurate hybrid functional [57]. Since 2012, the latest version of the hybrid functional, Heyd-Scuseria-Ernzerhof (HSE) functional, HSE 06, is being used by various groups to calculate the defect properties. The defect properties are modeled by placing the defect at the center of a periodic supercell (multiple unit cells joined to make one large cell). The complexity of the problem increases with the size of the supercell. Various research groups used supercells with different sizes (number of atoms) depending on their computational capabilities. However, it was recently shown that any supercell with less than 128 atoms in size would lead to stronger defect-defect interaction and the reliability of the calculations is reduced [58]. In addition to choosing the approximation (LDA, GGA, HSE) and supercell size researchers are often forced to employ many approximations due to the complexity of the calculations. The calculations are extremely sensitive to minor changes in the ground state energies of the calculated systems and therefore can be affected by any approximations/assumptions made [59]

Table 4: Summary of theoretical defect calculation studies reported by various groups

Group	Year	Approx.	Super Cell Size	Assumptions	Ref
Berding et al.	1999	LDA	32	• To account for the bandgap error of the Local Density Approximation (LDA) approach, the donor levels were shifted upward by 0.85 eV. • A gradient corrected energy of 0.55 per Cadmium atom and 0.59 eV per Tellurium atoms was added to each supercell	[60]
Su Hei Wei et al.	2002	LDA	32/64	• To reduce the LDA bandgap error, the calculations were performed nonrelativistically. • The error was estimated to be 0.2 eV for formation energies and 0.1 eV for transition energies.	[53]
Du et al.	2008	LDA	64		[61]
Du et al.	2012	PBE/HSE	64/216		[62]
Su Hei Wei et al.	2013	HSE 06	216		[67]
Krasikov et al.	2016	HSE 06	64	• For charged defect super cells, a potential alignment correction scheme was employed.	[63]

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Berding '99
CBM
Cd_i 0.2 (0/2+)
Te_{Cd} 0.4 (0/2+)
V_{Te} 0.4 (0/+)
V_{Te} 0.5 (0/2+)
V_{Cd} 0.80 (0/2-)
V_{Cd} 0.20 (0/-)
VBM
32 atom
LDA

Wei '02
Cd_{Te} 0.10 (2+/0)
Te_{Cd} 0.34 (+1/0)
Cd_i 0.45 (2+/0)
Te_{Cd} 0.59 (2+/+1)
V_{Te} 0.71 (2+/0)
Te_i 0.57 (0/-2)
V_{Cd} 0.21 (-1/2-)
V_{Cd} 0.13 (0/-)
32 atom
LDA

Du '08
Cd_i 0.71 (+2/0)
V_{Te} 0.78 (+2/0)
Te_{Cd} 0.35 (+2/0)
V_{Cd} 0.26 (-1/2-)
V_{Cd} 0.18 (0/-1)
Te_i 0.02 (+2/+1)
64 atom
LDA

Du '12
V_{Te} 0.30 (+2/0)
Te_{Cd} 0.58 (+1/0)
V_{Cd} 0.50 (-1/2-)
Te_{Cd} 0.38 (+2/+1)
Te_i 0.35 (+2/0)
V_{Cd} 0.20 (0/-1)
64 atom
PBE

Wei '13
V_{Te} 0.07 (2+/0)
Cd_{Te} 0.10 (2+/0)
Te_{Cd} 0.34 (+1/0)
Cd_i 0.45 (2+/0)
Te_{Cd} 0.70 (2+/+)
Te_i 0.75 (0/-2)
V_{Cd} 0.4 (-1/2-)
64 atom
HSE

Krasikov '16
CBM
V_{Te} 0.11 (+2/+0)
Te_{Cd} 0.51 (+1/+0)
Te_{Cd} 0.41 (+2/+1)
V_{Cd} 0.35 (0/-2)
Te_i 0.26 (+2/+0)
V_{Cd} 0.19 (0/-1)
VBM
64 atom
HSE

Figure 13: Defect transition energies of native CdTe defects calculated by various groups. The same defects are marked in the same color

4.3.1 Transition Energies of Intrinsic Defects

The summary of the calculations performed by various groups are shown in the Table 4 below in chronological order: The variations in the defect transition levels reveal the complex nature of the calculations. The calculations performed using the latest HSE06 functional are highlighted in. Figure 13. V_{Cd} was found to be a shallow acceptor defect and V_{Te} was found to be a shallow donor defect according to HSE06 calculations. This implies that V_{Cd} has lower ionization energies and can readily contribute holes than other acceptor defects like Te_i.

4.3.2 Compensation by Intrinsic Defects

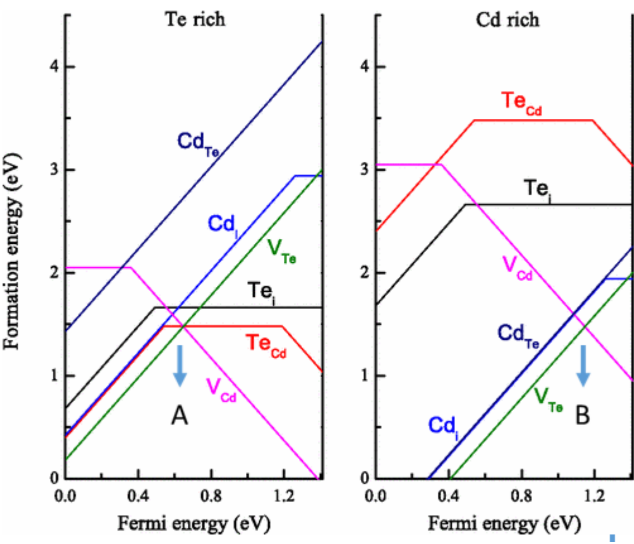

Figure 14: Formation energies of native point defects in CdTe [64]

Figure 14* shows formation energies of some of intrinsic point defects as a function of Fermi energy (E_F) calculated using the HSE06 functional [64]. The energy where the slope of the formation energy changes is the transition energy of the defect, i.e. a non-zero slope of a defect indicates that the defect is ionized/activated. V_{Cd} was found to be an acceptor (negative slope) while Cd_i, V_{Te} and Te_i were found to be donors (positive slope). The calculations showed that formation energies depend on the growth conditions. The formation energy for the V_{Cd} defect was found to be lower under Te-rich conditions compared to Cd-

* Reprinted with permission from Ma, Jie, et al. "Dependence of the minority-carrier lifetime on the stoichiometry of CdTe using time-resolved photoluminescence and first-principles calculations." *Physical review letters* 111.6 (2013): by the American Physical Society

rich conditions. Under Cd and Te rich conditions, as the Fermi level moves towards the valence band maximum (VBM) (making CdTe more p-type), the formation energy of the donor defects (Cd_i, V_{Te}) decreases (Figure). For p-type doping under Te-rich conditions, the Fermi level was found to be pinned at 0.7 eV from the VBM (point A). This is because, if E_F is below point A, the formation of acceptor defects V_{Cd}^{2-} is compensated by the formation of donor defects V_{Te}^{2+}. Similarly, under the Cd-rich conditions the Fermi level was found to be pinned at 1.2 eV because below point B, the formation of donor defect V_{Te}^{2+} is spontaneous compensating the acceptor defect, V_{Cd}^{2+}. This phenomenon, called compensation, is one of the main factors limiting doping in CdTe.

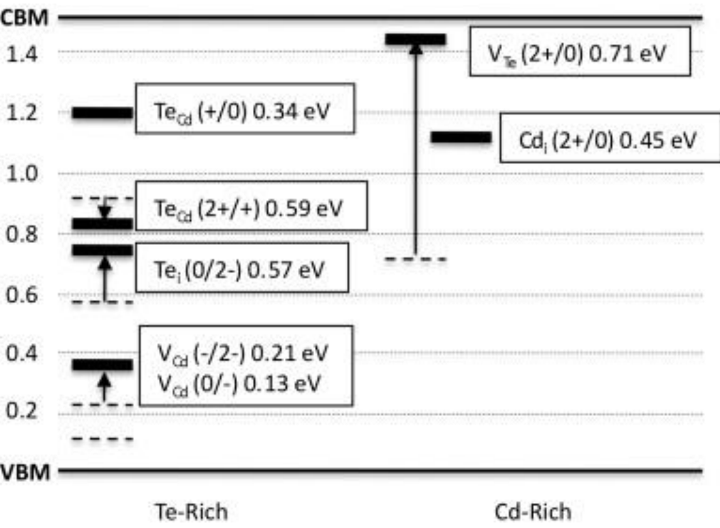

Figure 15: Mid-gap states in CdTe which limit carrier lifetimes [67]

4.3.3 Lifetime Limiting Defects

The main process that limits carrier lifetimes in CdTe is the 'defect-mediated' recombination. According to the Shockley-Read Hall (SRH) model, the most efficient recombination centers are deep level defects in the middle of the bandgap [65,66]. SRH recombination is believed to be the primary mechanism limiting minority carrier lifetime in CdTe. According to the calculation performed using HSE Te_{Cd} and Te_i were found to be the main mid-gap states in CdTe [67]. A study by Krasikov et al. [63] also used the HSE approach and found that the capture rate of Te_{Cd} defect is the highest among all mid-gap defects making it

the main defect responsible for limiting lifetimes. The formation energy diagram shows that Te_{Cd} has lower formation energy under Te-rich conditions. Figure 15* shows the main mid-gap defects in CdTe.

4.3.4 P- Doping: Group I Dopants

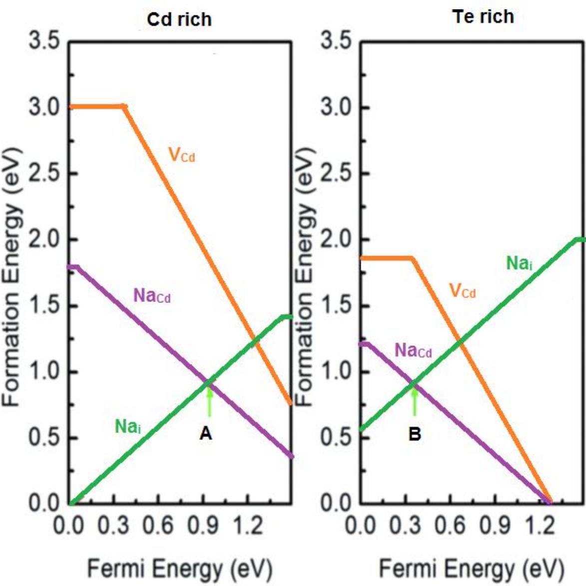

Figure 16: Formation energies of Group I dopants in CdTe

Group I elements like Na and Cu can form acceptor states Na_{Cd} and Cu_{Cd} respectively by occupying a V_{Cd}. In addition to acceptor states, Group I dopants also form interstitial defects like Na_i, and Cu_i which are donors. The acceptor defect Na_{Cd} was found to be a very shallow defect with its transition level at 0.05 eV above the VBM and Na_i was found to be donor with transitional level of 0.04 eV below the CBM [68]. The donor states can act as compensating defects limiting p-type doping. Figure 16 shows the defect formation energies for Na_{Cd} and Na_i as a function of E_F under Cd-rich and Te-rich growth conditions. Similar to the intrinsic defects, Na_{Cd} and Na_i compensate when E_F is below point B (0.36 eV above VBM) under Te-rich growth conditions. P-doping under Cd-rich conditions is not effective with Na, as the E_F is pinned at about 1 eV above the VBM (point A). Cu also a group I impurity continues to play a key role in CdTe and is therefore discussed in more detail below.

*Reprinted from Gessert, T. A., et al. "Research strategies toward improving thin-film CdTe photovoltaic devices beyond 20% conversion efficiency." *Solar Energy Materials and Solar Cells* 119 (2013) with permission from Elsevier.

4.3.5 P- Doping: Group V Dopants

Figure 17† shows the formation energy for P and As as a function of E_F under Cd-rich and Te-rich conditions. P and As (Group V elements) are expected to replace Te (Group VI) to form acceptor states. According to the calculations performed using the HSE06 approximation, P and As form very shallow acceptor states (0.07 and 0.1 eV from VBM respectively) [69]. Unlike the Group I dopants, interstitials were not found to be the main compensating defects for Group V elements. When a P atom occupies a Te site, it forms the substitutional defect P_{Te} where it is surrounded by four Cd atoms. In some occasions the P atom (in the Te site) moves towards a neighboring Te atom to form a P-Te bond breaking two bonds with

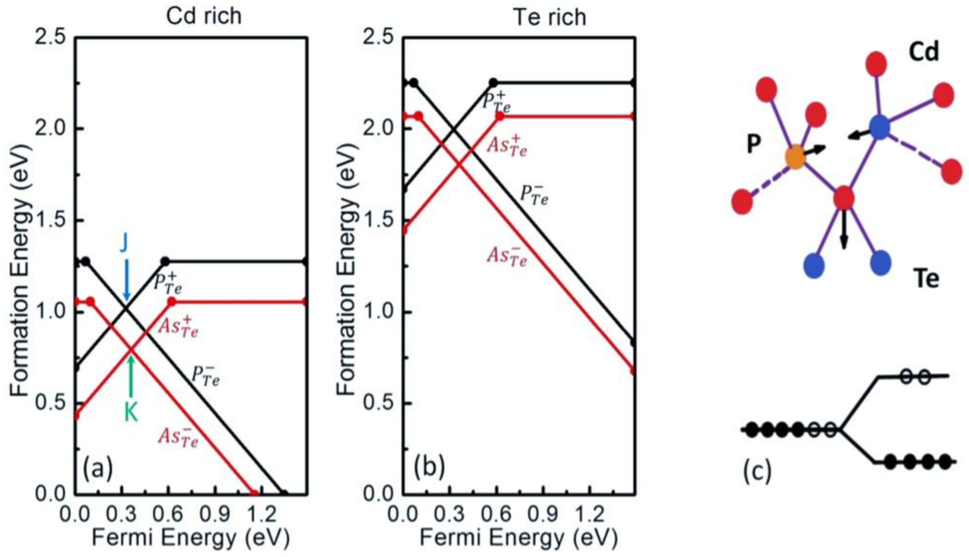

Figure 17: Formation energy of Group V dopants in CdTe (left); AX center formation (right) [69]

Cd (Figure 17, right). This results in the formation of a new defect state called the AX center which is a donor. It was found that the AX center donor defects have lower formation energies than P_i or As_i making them the main compensating defects. Under equilibrium growth conditions, the Fermi level was found to be pinned at 0.32 eV and 0.36 eV for p-doping using P and As respectively. This corresponds to a net acceptor density of approximately $10^{14}/cm^3$.

†Reprinted from Yang, Ji-Hui, et al. "Enhanced p-type dopability of P and As in CdTe using non-equilibrium thermal processing." *Journal of Applied Physics* 118.2 (2015) with permission of AIP publishing.

4.3.6 Cu and Cl Related Defects

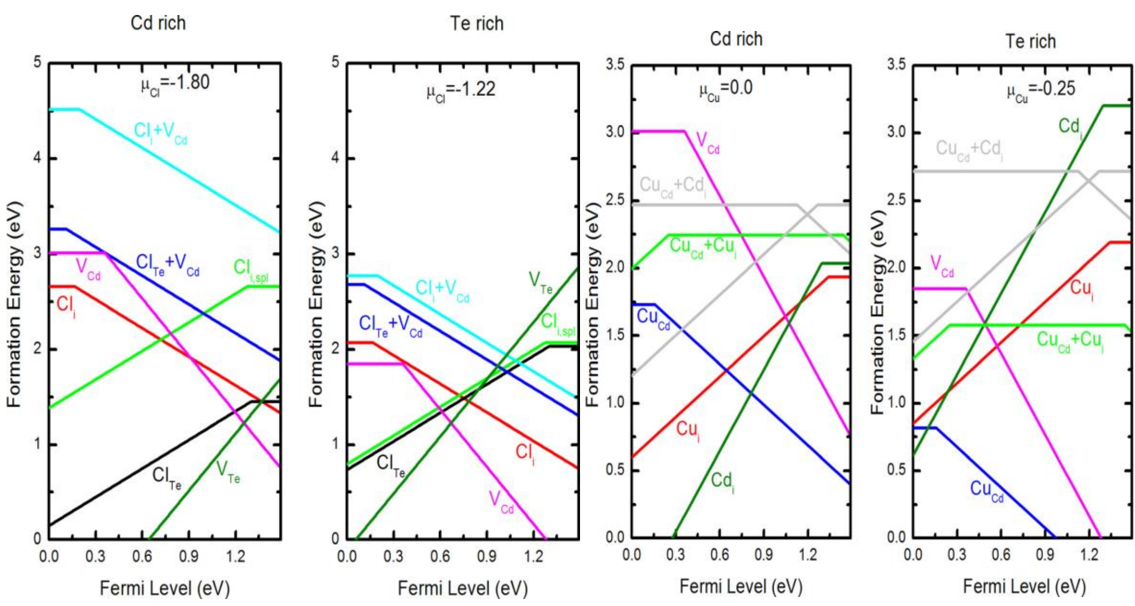

Figure 18: Formation energy of Cl and Cu related defects in CdTe (left and right respectively) [71]

Cu and Cl treatments have widely been accepted to be crucial for achieving high efficiency CdTe/CdS solar cells. In addition to aiding the formation of an Ohmic back contact to CdTe, Cu has been experimentally proven to increase the p-type conductivity in CdTe [70]. Irrespective of the method used for CdTe deposition, the Cl treatment is known to improve the structural and electronic properties of the CdTe layer and improve the efficiency of CdTe/CdS solar cells. Numerous mechanisms have been proposed to explain the role of Cu and Cl in improving device performance. The theoretical predictions of various defects introduced by Cu and Cl are discussed in this section. The role of Cu and Cl in cell fabrication will be discussed in detail in subsequent chapters.

Cu is a Group I dopant and like Na can occupy a V_{Cd} to form the substitutional acceptor defect, Cu_{Cd}. The formation energies of Cu related defects in CdTe under Cd and Te rich conditions are shown in Figure 18* (right) [71]. Cu forms a shallow defect with an acceptor level at 0.16 eV above the VBM. The formation energy of the acceptor defect Cu_{Cd} is always lower than the compensating defect Cu_i. This makes Cu the best cation (Cd) substitutional defect in CdTe.

*Reprinted from Yang, Ji-Hui, et al. "First-principles study of roles of Cu and Cl in polycrystalline CdTe." *Journal of Applied Physics* 119.4 (2016): 045104. with permission of AIP publishing

Figure 18 (left) shows the defects formed due to Cl in CdTe [64]. Cl being a Group VI element, is expected to form a donor defect (Cl_{Te}) by occupying a V_{Te}. In addition to Cl_{Te}, it also forms other interstitial defects like Cl_i^+ which is also a donor. One of the advantages of Cl treatment was improved p-doping in the CdTe layer. Cl_{Te} can form complex defects by combining with V_{Cd} called A-centers (V_{Cd} + Cl_{Te}). A centers were found to be very shallow acceptor states at 0.11 eV above the VBM which explains the increase in p-doping often observed in experiments. However, the concentration of the A-centers is dependent on the availability of V_{Cd}'s. Once all the V_{Cd}'s are consumed, Cl can no longer form A-centers but starts to form Cl_{Te} and Cl_i^+ which are both donor defects. Therefore, the amount of Cl incorporation has to be controlled.

4.4 Summary of Theoretical Studies

Table 5 shows the ease of formation of various native defects which influence the doping mechanism and carrier lifetime in CdTe. Te-rich conditions which favor the formation of V_{Cd} (the main intrinsic acceptor defect responsible for p-type doping) also favor the formation of mid-gap states, Te_{Cd} and Te_i, which are detrimental for carrier lifetimes. Cd-rich conditions on the other hand do not favor the formation of V_{Cd}, Te_{Cd} or Te_i. This would result in poor carrier concentration due to a lower V_{Cd} concentration and good carrier lifetimes due to lower concentration of mid-gap states i.e. Te_{Cd} or Te_i. This implies that Te-rich conditions favor better acceptor concentrations and also poor lifetimes, which will not yield high efficiency devices. In addition to native defects the following observations can be made regarding dopants:

- Cu is the best Group I dopant and since it forms very shallow acceptor states Cu_{Cd} however, it also forms interstitial states Cu_i, which are donors.
- Cl forms substitutional defects Cl_{Te} which can combine with V_{Cd} defects to form shallow acceptors called A-centers
- Compensating defects due to dopants limit p-doping in CdTe

Table 5: Ease of formation of various defects at Cd-rich and Te-rich conditions

Defects	**Ease of Formation**	**Effect**
V_{Cd}	Difficult	Low carrier conc.
V_{Te}	Easy	Shallow donor: Self-compensation for V_{Cd}
Cd_i	Easy	Shallow donor: Self-compensation for V_{Cd}
Te_{Cd}	Difficult	Improved lifetime

Table 5 (Continued)

Te_i	Difficult	Improved lifetime
V_{Cd}	Easy	High carrier conc.
V_{Te}	Difficult	Shallow donors
Cd_i	Difficult	Shallow donors
Te_{Cd}	Easy	Poor lifetime
Te_i	Easy	Poor lifetime

4.5 Experimental Study of Native Defects in CdTe

Table 6 below shows the defect transition levels of native point defects measured by various groups using: Deep level Transient Spectroscopy (DLTS), photo deep level transient spectroscopy (PDLTS), photo-induced current transient spectroscopy (PICTS), admittance spectroscopy (AS), photoluminescence (PL), electron paramagnetic resonance (EPR) and modulated photocurrent (MPC). V_{Cd} and V_{Te} defects were found to be a shallow acceptor defect by various groups which is in agreement with theoretical studies.

Table 6: Experimentally determined defect transition energies of CdTe intrinsic defects by various groups

Defect	Transition	Transition Energy	Measurement
V_{Cd}	(0/-1)	0.145	AS [72]
		0.14	PL [73]
		0.14	DLTS [74]
		0.18	PICTS [75]
	(0/-2)	0.38	DLTS [73]
		0.4	DLTS [74]
Te_{Cd}	(+2/+1)	0.32	PDLTS, PICTS [74]
	(+1/0)	0.2	EPR 71[76]
V_{Te}	(+2/0)	0.04	PL [73]
	(+2/+1)	0.06	PL [73]
Te_i	(+2/0)	0.46	AS [72]

4.6 Doping CdTe through Stoichiometry Control: Previous Experimental Work

Doping CdTe through stoichiometry control was investigated by various groups. A brief review of such studies is discussed in this section.

4.6.1 Control of Stoichiometry by Varying Substrate Temperature

According to the CdTe phase diagram, films deposited at higher temperatures tend to be more Te-rich while samples grown at low temperatures are Cd-rich [77]. This approach was used to study the effect of CdTe stoichiometry on minority carrier lifetime [67]. CdTe films were grown at temperatures of 484° C and 625° C. Qualitative verification of changes in stoichiometry was performed using Inductively Coupled

Mass Spectroscopy (ICP MS). The Cd: Te ratios measured were 1.00 ± 0.001 for 484° C sample and 0.98 ± 0.01 for sample grown at 625° C. Time Resolved Photoluminescence (TRPL) measurements estimated carrier lifetimes for the Cd-rich sample to be nearly 10 ns and for the Te-rich sample to be 1-2 ns. Higher V_{OC} were reported for Cd-rich samples (0.83V for 484° C) samples and (0.78V for 625° C). Similar studies on very large grain polycrystalline samples with grain sizes of approximately 1mm were reported to follow similar trends with Cd-rich films exhibiting carrier lifetimes up to 20 ns and Te-rich samples exhibiting lifetimes of about 3 ns. Large grain structure could improve the performance of the solar cell by reducing grain boundary related defects and hence enhancing carrier lifetimes. However, for the samples heat treated with Cl and Cu incorporation, other effects like CdS thinning could also play a role. At high substrate temperatures such as 600° C CdS could intermix with CdTe and lead to CdS thinning causing lower V_{OC}'s. Similar procedures followed earlier by the same group yielded contradicting results with V_{OC} increasing with increase in substrate temperature [78].

4.6.2 Stoichiometry Change by Stacked Elemental Layer Method

Stacked Elemental Layer was used by [79] to achieve variation in stoichiometry. The physical properties were investigated using XRD, AFM and Transmittance and reflectance measurements. Bi layers of Te/Cd were deposited on glass substrates by evaporation with pressures at 10^{-6} to 10^{-5} Torr range. The desired stoichiometry was achieved by varying the thickness of the individual Te and Cd layers. The deposited bi-layers were subsequently annealed at temperatures ranging from 170 to 250°C for different time periods. It was found that CdTe formation starts at 170° C with the presence of Te and Cd free phases, but useful optical properties (characteristic absorption edge at 830 nm) were found only when the temperatures above 300° C.

4.6.3 Vapor Growth of CdTe from Elemental Cd and Te

Vapor growth of CdTe was used to control stoichiometry of CdTe for laser window application was investigated by [80] using elemental Cd and Te sources. The deposition was carried out at near atmosphere by independently controlling the vapor pressures of Cd and Te sources above their respective melting points. The electrical conductivity was found to increase with increase in Te gas phase during growth. Voids were observed at the grain boundaries when the films were grown near stoichiometric conditions or at high

super saturations. Depositions at substrate temperatures as high as 950° C exhibited better microstructures.

4.6.4 Te-rich Films by CSS Method

CdTe films were deposited by CSS and then made Te-rich by evaporating Te onto the same substrate by [81]. The stoichiometry was varied by evaporating 0.5,1,2,3,4 mg of Te onto CdTe substrates. The structure of the film was analyzed by XRD and SEM. EMPA measurements were conducted to study the composition. Hall measurements were conducted to study mobility and carrier concentration. An increase in grain size was observed with increase in Te content. XRD measurements indicated an increase in crystal quality with increase in Te content. Hall measurements indicated an increase in carrier concentration with increase in Te content.

4.6.5 Cd Self-Sputtering of CdTe

CdTe-Cd target was used as the sputtering source by [82] to deposit Cd rich films. N-type CdTe films were successfully made and the conductivity change from p to n-type was observed. The presence of interstitial Cd was said to be the reason for the change of conductivity.

4.7 Motivation and Objectives

The review of theoretical and experimental studies discussed in the previous section ascertains that control over stoichiometry is necessary to achieve high doping levels and carrier lifetimes in CdTe. With this understanding, choosing a Cd or Te-rich condition growth regime over the other is not a direct or an easy choice. Though several groups have attempted stoichiometry control in CdTe, consolidated efforts to improve carrier concentration and lifetimes have not been adequate. In this study, CdTe is deposited using the Elemental Vapor Transport (EVT) method. In this method, elemental Cd and Te are used to deposit CdTe in excess Cd or excess Te conditions which enables for the control of native defect concentration and therefore pave the way to improve acceptor concentrations and carrier lifetimes. The deposition system enables precise control over stoichiometry. The objectives of this study are to:

1. Undertake a systematic approach in order to create favorable conditions for improved p-doping and carrier lifetimes in p-CdTe through stoichiometry control.
2. Study the effect Cu and Cl treatments on Cd-rich and Te-rich films.

Chapter 5: Experimental Methods

The solar cell fabrication and characterization methods used in this work are discussed in this section. CdTe solar cells can be fabricated either in a substrate or a superstrate configuration. The basic superstrate structure which is predominantly used, is glass//TCO/CdS/CdTe/Back contact as shown in Figure 19. The substrate configuration is essentially the inverse of the superstrate configuration i.e. back contact/CdTe/CdS/TCO deposited on an opaque substrate. All high efficiency devices till date have the superstrate structure. The substrate configuration, is less successful due to problems such as poor ohmic contact to CdTe and poor CdS/CdTe/junction quality [83].

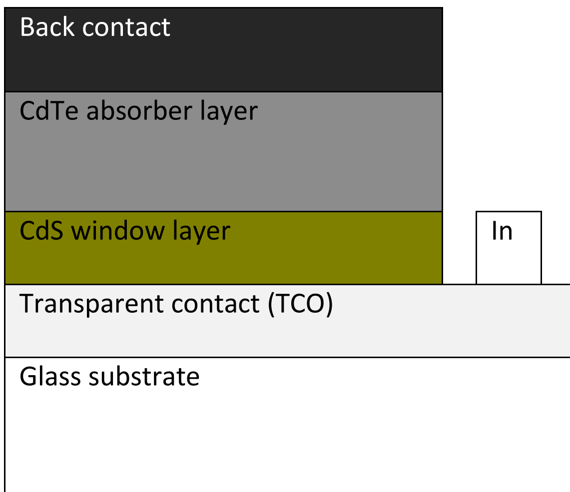

Figure 19: Superstrate CdTe solar cell configuration

5.1 Cell Fabrication

5.1.1 Glass

The choice of the glass is generally dependent on the operating temperatures of the subsequent processing steps. Borosilicate glass is used for higher operating temperatures (~600° C) and soda-lime glass is used for lower temperatures (< 500° C) [84]. Typically, higher deposition temperatures (>550° C) result in the highest efficiencies of CdTe solar cells. In this study, Eagle XT was used as the glass substrate.

It is an alkali free borosilicate glass with a transmittance of >90% in the wavelength range of 380-2200 nm. Prior to deposition of the front contact, the substrates were cleaned with D.I water and etched for a very short period using 10 % HF solution.

5.1.2 Front Contact (Transparent Conducting Oxide)

Transparent conductors are materials which possess high optical transmission. The main characteristics that are required for a material to qualify as a Transparent Conducting Oxide are [85]:

1. High transparency in 400 nm -900 nm wavelength range
2. Low resistivity (Typically in the order of ~ 10^{-4} Ω cm or a sheet resistance of about 10 Ω/□
3. Good thermal and chemical stability to support further high temperature processing steps.

For CdTe solar cells, the TCO should have an electron affinity of less than 4.5 eV in order to form an ohmic contact to the n-type CdS layer. Some of the popular TCOs used in CdTe solar cells are Florine doped Tin Oxide (SnO_2:F), Tin doped Indium oxide (In_2O_3:Sn) and Cadmium Stannate (Cd_2SnO_4). Table 7 shows the properties these TCO and buffer layers [85].Typically the TCO for high efficiency CdTe solar cells utilize a bi-layer structure for the TCO. This consists of a high conducting layer which enables current collection and a thin high resistive buffer layer which prevents the formation of pinholes and shunt paths. The buffer layer also serves as an extension to the window layer which allows for employing a thinner window layer. Reducing the thickness eliminates parasitic current losses in the window layer increasing the efficiency.

Table 7: Properties of popular TCO and buffer layers used in CdTe/CdS solar cells [85]

Material	Resistivity (Ω cm)	Transparency (%)
SnO_2	8.0 x 10^{-4}	80
SnO_2:F	4.0x 10^{-4}	84
In_2O_3:Sn	2 0x 10^{-4}	85
Cd_2SnO_4	2.0x 10^{-4}	92
In_2O_3: F	2.5 x 10^{-4}	85
Zn_2SnO_4	1.0 x 10^{-2}	90
ZnO: In	8.0 x 10^{-4}	85

In this study Indium oxide doped with Sn, popularly known as Indium Tin Oxide (ITO) was used as the front contact and SnO_2 was used as the buffer layer. Both the layers were deposited using RF sputtering

on the pre-cleaned glass substrates. The thickness of the ITO layer was between 2500 and 3000 Å while that for SnO_2 was between 1000 and 1500 Å. The deposition was carried out at 250° C in ultra-high purity argon (Ar) ambient. The substrate holder was rotated during deposition to maintain uniform thickness. The front contact (ITO) was deposited from a (In_2O_3/SnO_2, 90/10 wt%) 99.9995% without a vacuum break between depositions.

5.1.3 Window Layer

The primary function of the window layer is to form a junction with the absorber and allow maximum light to reach the absorber. The bandgap of the window layer should be as high as possible and the thickness has to be as low as possible to allow maximum amount of light to reach the absorber. CdS layer has been the best heterojunction partner for CdTe in spite of the 10% lattice mismatch between the two layers. This is due to the fact that they are both miscible. The reaction between CdTe and CdS at high temperatures (which is typically reached during CdTe deposition or subsequent $CdCl_2$ treatment) leads to formation of an interfacial layer $CdS_{(1-x)}Te_x$. The formation of this layer is believed to reduce the lattice mismatch between CdTe and CdS and improve the junction properties [86]. CdS has a bandgap of 2.4 eV which corresponds to a wavelength of 510 nm. A considerable amount of the solar spectrum falls below 510 nm. Due to the poor properties of the CdS layer, the light absorbed in this layer does not contribute to photocurrent. The theoretical maximum for CdTe based on its bandgap is 30.5 mA/cm^2, out of which up to 7 mA/cm^2 could be potentially lost due to a thick (> 500 Å) CdS layer[87]. Therefore, the CdS layer is kept as thin as possible. Typical CdS thickness is less than 100 nm. However, thinning the CdS could have an adverse effect on the solar cell performance. Thin CdS is known to reduce the V_{OC} and FF [87]. Another disadvantage of using thin CdS layer is the formation of pinholes. Pinholes lead to micro junctions to form between CdTe and the front TCO layer reducing solar cell performance. Therefore, the thickness has to be optimized to get the maximum possible current while eliminating any shunt paths.

CdS films can be deposited using various techniques like vacuum evaporation, spray deposition, electrodeposition, screen printing, chemical vapor deposition, RF sputtering and Chemical Bath Deposition (CBD) [88]. Of these techniques, films grown by CBD are known to have excellent optical and electrical properties. Moreover, the process is simple, readily scalable with low fabrication cost [88]. In this study, CdS was deposited using CBD. Deposition of CdS using CBD is based on slow release of Cd^{2+} and S^{2-}

ions in an aqueous alkaline solution [89]. Cadmium acetate is used as cadmium source. Thiourea is used as sulfur source, ammonium acetate (NH_4Ac) and ammonium hydroxide (NH_4OH) are used as buffers to maintain alkalinity and control the reaction speed. The ITO/SnO_2 coated glass substrates were immersed in DI water pre heated to 80° C. The Cd and S precursors (viz. cadmium acetate and Thiourea) along with the buffer agents are added in regular intervals to the D.I. water. The temperature was maintained at 80-85 ˚C using a constant temperature bath. The solution was continuously stirred with a magnetic stirrer. The thickness of CdS can be changed by varying the deposition time. The reaction steps were proposed by J. Herrero et al. [90] and are provided here:

$Cd(CH_3COO)_2 \leftrightarrow Cd^{2+} + 2CH_3COO^-$

$NH_3 + HOH \leftrightarrow NH_4^+ + OH^-$

$Cd(NH_3)_4^{2+} + 2OH^- \leftrightarrow [Cd(OH)_2(NH_3)_2] + 2NH_3$

$[Cd(OH)_2(NH_3)_2] + SC(NH_2)_2 \rightarrow [Cd(OH)_2(NH_3)_2SC(NH_2)_2$

$[Cd(OH)_2(NH_3)_2SC(NH_2)_2] \rightarrow CdS_{(S)} + CN_3H_5 + NH_3 + 2HOH$

After the deposition, the samples were rinsed with warm water in an ultra-sonic bath to eliminate any large particles that may have adhered to the substrate surface during the reaction. Heterogeneous growth is preferred to homogenous growth in the solution which results in the formation of large particles.

5.1.4 CdTe Layer

One major advantage of CdTe is the resilience it shows towards changes in deposition techniques [83]. Such tolerance to the deposition techniques resulted in the development of many deposition techniques. The electronic properties of CdTe manufactured by various processes described above are generally dependent on post deposition treatment [91]. The most common deposition methods are sputtering [92], electrodeposition [93], [94], screen printing [95], metal-organic chemical vapor deposition [96] and close-spaced sublimation (CSS) [97], [98]. Each of these present their own advantages with CSS and vapor transport yielding the best results to date [99,100]. Figure 20 shows the Phase diagram of CdTe [101]. In the high temperature regime, CdTe is p-type due to more pronounced deviation around stoichiometry in the Te-side, giving rise to Te-over pressure during growth which results in p-type conductivity of as-deposited CdTe [102].

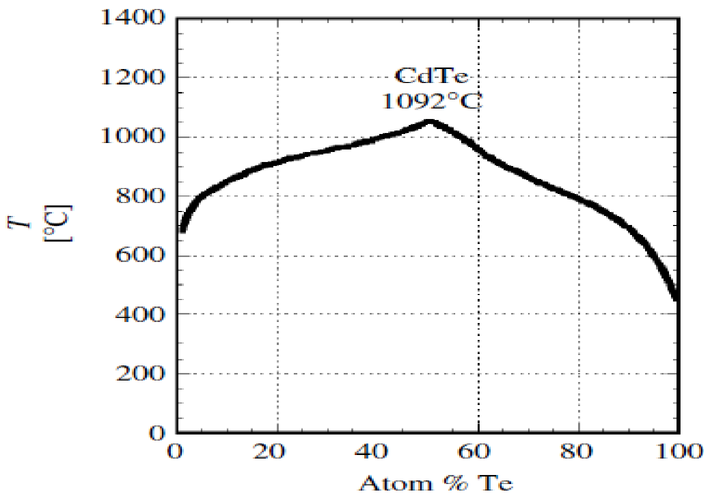

Figure 20: Phase diagram of CdTe [83]

5.1.4.1 Elemental Vapor Transport

The basis for vapor deposition of CdTe is the equilibrium between Cd and Te vapors and the CdTe solid [4]. The relatively low vapor pressure of CdTe compared to elemental Cd and Te facilitates the deposition of single phase solid films over a wide range of substrate temperatures [103]. In this study, CdTe is deposited using a technique called Elemental Vapor Transport (EVT). The major advantage of this process is *in situ* control of stoichiometry which, as discussed in the previous sections can pave the way for CdTe devices with higher carrier densities and lifetimes. The schematic diagram for the EVT process is shown in Figure 21. Vapors of elemental Cd and Te were used to deposit polycrystalline CdTe using the EVT process (Figure 21). Cd and Te metals of 99.999% purity were loaded into dedicated zones made of high purity graphite. Each zone was independently heated using 6KW tungsten halogen lamp heaters. A mixing zone where the substrate is located was placed after the last elemental zone. Each elemental zone was supplied with UHP Helium (He) carrier gas (through quartz tubes) with dedicated mass flow controllers to control the flow rate. Condensation of elemental vapors is desirable only on the substrate and has to be avoided elsewhere. Therefore, the zones were placed such that the temperature increases from the inlet to the outlet of the reactor, with the mixing zone held at the highest temperature. The sample holder was positioned in the mixing zone such that the temperature was between 580 and 600° C. The gas phase

Cd/Te ratio was varied by controlling the vapor transport of Cd and Te in order to influence the stoichiometry of the CdTe films. Mass transfer depends on the vapor pressures of Cd and Te and therefore is a function of the temperatures of the individual zones and flow rates of the carrier gases. The vapor pressures for Cd and Te were obtained from previous studies [104], [105]. The pressure of the chamber was maintained at 700 Torr using a mechanical pump and a pressure control valve. The flowrates of the mixing zone was maintained at 2L/min and the flowrates of the elemental zones were varied between 250cc/min to 400 cc/min. The temperatures of the Cd and Te zones were varied in the range of 435 – 460 and 535 - 560° C respectively to achieve the desired Cd/Te ratios. The temperatures of the mixing zone was maintained between 700 - 720° C. Prior to each deposition, the chamber was purged with UHP He several times to eliminate O_2 in the reactor.

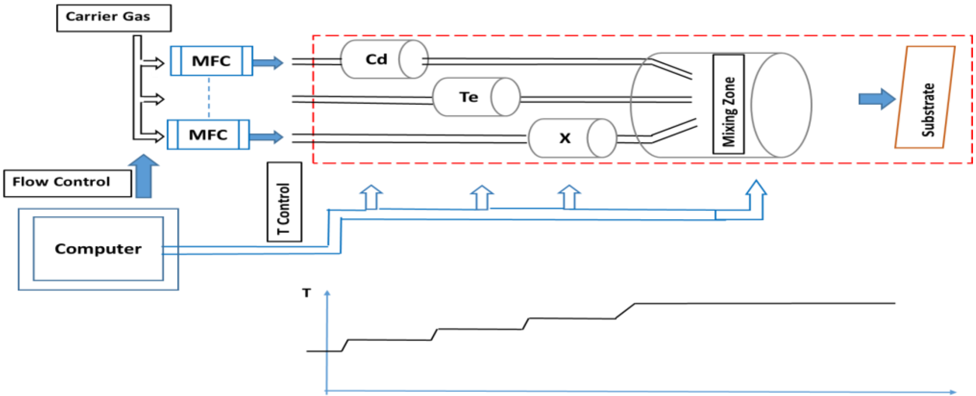

Figure 21: Schematic of the Elemental Vapor Transport

5.1.5 $CdCl_2$ Heat Treatment

$CdCl_2$ heat treatment is widely accepted as a necessary step to fabricate high efficiency CdTe/CdS solar cells. The properties of the CdTe layer are vastly influenced by the $CdCl_2$ treatment. This process is known to have three major effects on the CdTe solar cell: (a) CdTe grain enhancement; (b) enhanced inter diffusion between CdTe and CdS; (c) grain boundary passivation/lifetime improvement via the formation of Cl-related complexes in CdTe [106]. $CdCl_2$ HT was observed to cause recrystallization in CBD grown CdS process enhancing grain growth. This treatment was also found to reduce interface state densities by causing CdS diffusion into CdTe [107]. Inter-diffusion of S near the CdTe/CdS junction is known to improve the electronic properties of CdS/CdTe junction by reducing the lattice mismatch between CdS and CdTe

[108].In addition to improving the structural properties, the morphology of the films, Cl treatment was found to increase the shallow-acceptors concentration giving rise to additional p-type CdTe doping [109].

$CdCl_2$ HT can be performed by dipping the CdTe layer in a $CdCl_2$: CH_3OH or $CdCl_2$: H_2O solution followed by drying and heat treating at high temperatures up to 450° C in air. Though this method is simple for laboratory size devices and is also scalable for larger substrates. However, this approach leaves $CdCl_2$ residue on the surface which must be cleaned and therefore increases the number of processing steps [110]. Alternatively, the CdTe layer can be exposed to $CdCl_2$ vapor followed by a thermal anneal in the presence of O_2 at high temperatures.

In this study, the $CdCl_2$ process was carried out by depositing $CdCl_2$ onto the CdTe surface by evaporation and subsequently heat treating at high temperatures in the range of 375° - 410° C in O_2 and He ambient.

5.1.6 Back Contact

The formation of stable, low resistance and non-rectifying contact to p-CdTe is a challenge in the fabrication of high efficiency CdTe/CdS solar cells. P-type CdTe has a high electron affinity (χ=4.5 eV) and a bandgap of 1.45 eV and has a work function close to 5.8 eV. To form an ohmic contact, the contact metal should have a work function greater than that of p-type CdTe. There exists very few metals with such a high work function (Pt, Au etc.). Use of lower work function metals results in the formation of Schottky barriers giving rise to an undesirable back barrier. The presence of back contact barrier can reduce the performance of the solar cell by limiting hole transport. The back barrier changes the I-V characteristics of the solar cell by causing what is referred to as “roll-over”.

The presence of the back barrier is hard to eliminate, alternatively, a stable back contact with reduced barrier height is formed by one of the following methods:

1. Heavily doping the back surface to reduce the barrier followed by metal deposition to facilitate tunneling.
2. Using an interlayer or a buffer layer with a very high function such as HgTe or ZnTe [111]

5.1.6.1 Etching the CdTe Surface

The surface of the CdTe layer can be heavily doped by etching which changes the defect chemistry of CdTe surface. Etching serves two purposes: a) It provides a p^+ Te-rich layer and b) removes any residual

oxides from the CdTe surface that might have been formed during the $CdCl_2$ treatment. The most common etchants used are Br_2/methanol solutions, aqueous nitric acid/phosphoric acid mixtures (NP) and chromate etches ($K_2Cr_2O_7$:H_2SO_4). Etching converts the surface of the CdTe film to a Te-rich p^+ type conductive layer. This layer facilitates easier hole transfer from the CdTe layer to the Te-rich layer and to the back contact metal electrode by reducing the valence band offset.

5.1.6.2 Back Contacts

Cu is one of the most popular metal used in the back contact preparation in CdTe solar cells. It serves a dual role in improving the performance of CdTe solar cells. As mentioned in the earlier sections, Cu forms acceptor states by occupying V_{Cd}'s to form Cu_{Cd} improving p-type doping. When used as the back contact, Cu forms Cu_2Te with the Te-rich layer (formed as a result of the etching). The Cu_2Te layer is known to cause band bending at the CdTe/Te interface lowering the back barrier. Cu is generally used in combination with other metals to form the back contact. Commonly used Cu containing back contacts are Cu/Au [112], Cu_2Te [113], ZnTe doped with Cu [114], graphite paste doped with Cu [115], Cu/Mo.

Though Cu offers the above mentioned advantages, several studies have proved that Cu degrades the performance of the solar cell in the long run. 'Excess' Cu can also decrease p-doping by forming compensating defects Cu_i. Cu is known to be a fast migrator towards to CdTe/CdS junction under thermal stress. At the junction, Cu forms mid-gap states which act as recombination centers which lower the carrier lifetimes [116]. Therefore, controlled amounts of Cu has to be used when used as a back contact. Owing to the stability issues in Cu based back contacts, Cu free contacts have been widely been investigated. Examples of Cu free back contacts are: Ni: P [117], Sb_2Te_3 [118] and HgTe [119].

In this study, MoN/Mo was used as the back contact. MoN was deposited by RF sputtering under Ar and N_2 followed by the deposition of Mo layer in Ar ambient. The thicknesses of the MoN and Mo layers was around 500 and 5000 Å respectively. Cu was added on select films after the MoN/Mo layer in order to limit the Cu migration towards the junction. Plain graphite ink was also used for select films where the influence of Cu needed to be avoided.

5.2 Device Characterization

5.2.1 I-V Measurements

The current-voltage (I-V) curve under light gives many important parameters of the solar cell such as the V_{OC} and FF. Current voltage characteristics were measured using a solar simulator calibrated to AM 1.5 condition. The light intensity was adjusted to replicate AM 1.5 illumination with the help of a Si reference. A four point Kelvin probe measurement was used to eliminate the effect of parasitic contact resistances. A keithely 2410 Source meter was used to sweep the voltage and measure the current. A LabVIEW program was used to collect the I-V data and calculate the FF, J_{SC} and V_{OC}.

5.2.2 Spectral Response

Spectral response (SR) is defined as the ratio of the current generated by the solar cell to the power incident on it. Quantum efficiency (QE) is defined as the ratio of the number if collected electrons to the number of incident photons. If all the photons at a particular wavelength are absorbed and all the photo-generated carriers are collected, the resulting Q.E is unity. The QE is measured over the range of the spectrum between 400 and 900 nm which can be used to calculate the SR. The absorption coefficient is a function of the wavelength and therefore, the current generated by the solar cell changes as a function of wavelength. Quantum efficiency is a useful technique which estimates the current generated at different wavelengths. It is also useful to determine the losses due to reflection, transmission and recombination. An Oriel monochromater (model 74100) was used to measure the spectral response. A GE400W/120V Quartz line lamp was used as the light source and its intensity was calibrated using a silicon reference photodiode. LabVIEW program was used to collect and plot the data. The current response of the reference was first measured ($I_{Reference}$) followed by the current response of the solar cell (I_{Device}). The QE was then calculated according to the formula:

$$\mathrm{QE_{Device}} = \mathrm{QE_{Reference}} * \frac{\mathrm{I_{Device}}}{\mathrm{I_{Reference}}} \tag{11}$$

The current density is then calculated by integrating the $Q.E_{Device}$ multiplied by the AM 1.5 equivalent current.

5.2.3 Temperature-Resistivity Measurements

Temperature-resistivity measurement is a simple yet useful tool to analyze the electrical properties of a semiconductor. The resistivity of a semiconductor is inversely proportional to the carrier concentration

and mobility. Depending on the transition energy level, different defects and dopants are activated at different temperatures which affect the carrier concentration. The resistivity of doped semiconductors can be described by an Arrhenius temperature dependence given by the following equation:

$$\rho = \rho_o * \exp[\frac{E_a}{kT}] \quad (12)$$

where ρ is the resistivity at a particular temperature in Ω-cm, ρ_o is the pre-exponential resistivity in Ω-cm, E_a is the activation energy in eV, k is the Boltzmann's constant and T is the temperature in K. By measuring the resistivity as a function of temperature, it is possible to estimate the activation energy of the defects.

Resistivity of the deposited films were measured by Keithley electrometers with the 4-point measurement method. Co-linear Au contacts were deposited using DC sputtering in Ar ambient. The measurements were performed inside a Faraday cage. The temperature was varied from -40˚C to 120˚C using liquid N_2 and heater.

5.2.4 Capacitance-Voltage Measurements

The Capacitance-Voltage technique is commonly used to characterize the carrier density of semiconductors. The measurement relies on the fact that the width of a reverse biased space-charge region of a semiconductor junction depends on the applied voltage. The measurement assumes the device to be an n^+- p or a p^+- n junction. When an alternating voltage is applied to an n^+- p junction, the width of the space charge changes mainly on the p region. Due to heavy doping on the n-side, the change in depletion width is negligible. The change in depletion width causes a change in the junction capacitance. By measuring the change in junction capacitance with respect to the change in voltage, it is possible to estimate the carrier density in the p-region. The depletion region of a p-n junction can be approximated as a parallel plate capacitor with a junction capacitance given by:

$$C = \epsilon \frac{A}{W} \quad (13)$$

where ϵ is permittivity, A is the area of the device and W is the distance between the plates (in this case, the edges of the depletion region).

The width of the space charge (depletion) region in a p-n is given by:

$$W = \sqrt{\frac{2\varepsilon}{qN_A}(V_{bi} - V)} \quad (14)$$

where N_A is the carrier density of the p-type semiconductor, V_{bi} is the built-in voltage, and V is the applied voltage.

By substituting for 'W' in 'C', the C can be re-written as:

$$C = \varepsilon \frac{A}{\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi} - V)}} \tag{15}$$

By rearranging the above equation we obtain:

$$\frac{A^2}{C^2} = \frac{2}{q\varepsilon N_A}(V_{bi} - V) \tag{16}$$

A plot of $1/C^2$ vs V yields the carrier density and the intercept gives the built-in potential.

5.2.5 Time Resolved Photoluminescence (TRPL)

Minority carrier lifetimes can be measured by the TRPL technique. The film or device under study is excited with a laser pulse of known energy. As a result, carriers are excited from their ground state to an excited state. After a short delay, the carriers return to their ground state emitting a photon in the process. By measuring the time delay between the sample excitation and photon emission by the detector, the carrier lifetime can be estimated. In this study, TRPL measurements were performed at the National Renewable Energy Laboratory (NREL) with single photon excitation (1PE) and two photon excitation (2PE) time resolved photoluminescence (TRPL) measurements [120]. The films/carriers were excited from the glass side through the window layer (CdS) with 700 nm (1PE) and 1200 nm (2PE) wavelength laser beam and the photon emission was detected at a wavelength of 840nm.

5.2.6 Deep Level Transient Spectroscopy (DLTS)

Deep level Transient Spectroscopy (DLTS) is a technique which can be used to quantify mid-gap states. For this work, an instrument was purchased from Sula Technologies (shown in Figure) to perform DLTS measurements. The measurement system comprises of a cryo-based cooling stage with a heater, temperature controller, and turbo pump to maintain vacuum. The instrument is capable of measuring CV, IV, CT and IV along with capacitance transient measurements like DLTS, CCDLTS and CDTLS. Temperature ranges from 77K to 500K could be used. Simultaneous generation up to 6 spectra with different rate windows could be used to identify deep traps and their respective activation energies.

During the DLTS measurement the capacitance transient of a reverse biased p^+ - n or n^+ - p junction due to charge carrier injection is measured. The capacitance transient is given by the following equation,

$$C(t) = C_0\left[1 - \frac{N_T}{2N_D}\exp\left(-\frac{t}{\tau}\right)\right] \tag{17}$$

where, C(t) is the instantaneous capacitance, C_0 is the reverse bias background capacitance, N_T is the trap concentration, N_D is the doping concentration and τ is the carrier lifetime.

Depending on the type (majority or minority) of the trap levels activating at a certain temperature in the semiconductor the change in the transient can be negative or positive (Figure 22). The capacitance decay rate changes due to the change in the thermal emission rate and is therefore a function of temperature. A plot of change in capacitance (ΔC) observed through a temporal rate window (Δt) vs. temperature (T) results in the DLTS spectrum. A majority carrier trap yields a negative peak, while a

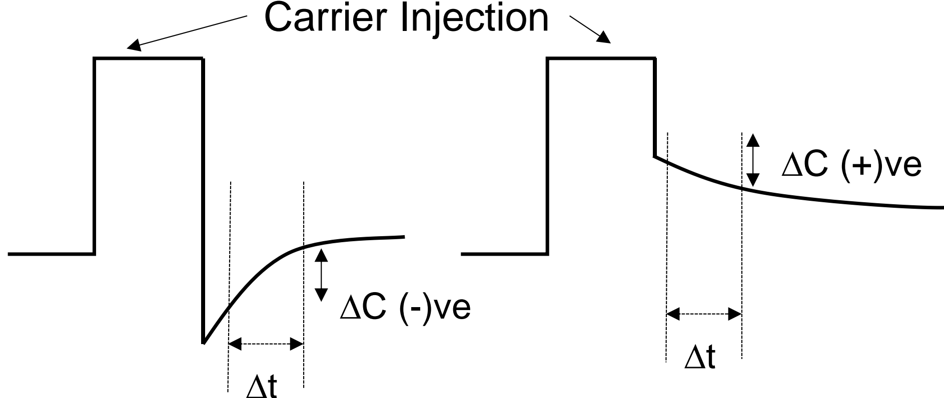

Figure 22: Capacitance transient on a reverse biased p-n junction due to carrier injection. A negative capacitance change, ΔC (left) indicates a majority carrier trap, while a positive ΔC (right) indicates a minority carrier trap. Δt signifies the rate window.

minority carrier trap produces a positive peak in the DLTS spectra. The trap concentration is calculated from the peak intensity. The activation energy and capture cross section of the trap can be calculated from analyzing the Arrhenius plot of the peak positions at different rate windows [121].

5.2.7 Morphology and Structure Analysis

Film Thickness was measured using Dektak 3030ST profilometer. XRD measurements were made to study the crystallographic properties using Panalytical X'pert Pro with a Copper (Cu) kα source. The grain morphology was studied using Scanning Electron Microscopy (SEM) on Hitachi S800 with an accelerating voltage of 25 KV. Electron Dispersive Spectroscopy (EDX) was used to estimate the film composition on select samples. Samples for EDX were prepared by focused Ion Beam milling using a dual

beam FEI Nova 600 Nanolab. EDX analysis has been carried out using a Tecnai F20 operating at 200 kV equipped with an Oxford instruments X-max N80 TLE SDD detector

Chapter 6: Results

6.1 Introduction

The main objective of this work is to undertake a systematic study of a process capable of creating favorable conditions for efficient doping and improved carrier lifetimes in CdTe thin films by following the theoretical guidelines discussed in the previous chapter. Native defects control the carrier concentrations and lifetimes in CdTe. By varying the CdTe stoichiometry, the concentration of native intrinsic defects can be controlled.

In this study, CdTe was deposited from elemental sources namely Cd and Te, using the Elemental Vapor Transport process (EVT). Cd and Te were heated to temperatures above their respective melting points (321 and 435° C for Cd and Te respectively). The vapors were then transported to a mixing zone where the substrate holder was located, using Helium as the carrier gas. Since the vapor pressure of CdTe is lower when than that of Cd and Te, the vapors condense readily on the substrate to form solid CdTe. To achieve stoichiometry control, the ***vapor phase Cd/Te ratio*** was varied to deposit Cd-rich (Cd/Te ratio >1), Te-rich (Cd/Te ratio < 1.0) and stoichiometric (Cd/Te ratio 1.0) films. The change in vapor ratio was attained by controlling the elemental zone temperatures and flowrates. The theoretically achievable change in atomic stoichiometry in CdTe as per the phase diagram is extremely limited. The single-phase, homogeneity region for CdTe is capable of supporting a maximum excess of only 4×10^{-3} at. % Cd or 13×10^{-3} at. % Te [77]. Therefore the actual change in stoichiometry of the CdTe film is expected to be infinitesimally small when compared to the change in gas phase Cd/Te ratio. Such minor variation in the elemental composition is below or close to the resolution limit of most composition analysis techniques, making it difficult to accurately estimate the changes in film stoichiometry. However, the stoichiometry change can be ascertained by studying its effect on the electrical properties of the films, based on the theoretical studies discussed earlier. Unless otherwise stated the term *Cd/Te ratio will be used throughout this document to define the gas phase Cd/Te ratio.*

6.2 Ratio Calculations

In order to achieve the desired Cd/Te ratio, the amount of Cd and Te vapors reaching the substrate have to be controlled. The mass transport and therefore the Cd/Te ratio depends on the vapor pressure of Cd and Te and the flowrates through the Cd and Te zones. The Cd/Te ratio was determined using the Ideal Gas Law. The vapor pressure of Cd and Te is a function of the temperature.

The vapor pressure for Cd is given by [104]

$$P_{Cd}(\text{torr}) = 10^{7.66023-\frac{4757.62}{T_{Cd}+228.438}} \tag{18}$$

where T_{Cd} is the temperature of the Cd zone in Celsius. The number of moles of Cd was then calculated using the ideal gas relationship:

$$n_{Cd} = \frac{(P_{Cd}*133.32)*V}{R(T_{Cd}+273)} \tag{19}$$

where P_{Cd} is the vapor pressure from eq. [17]. R is the ideal gas constant (8.31 J/K/mole), V is the total volume calculated using the following equation:

$$V_{Cd}\left(\frac{\text{moles}}{\text{min}}\right) = \text{FR}\left(\frac{\text{cc}}{\text{min}}\right) * 10^{-6} * \text{time (mins)} \tag{20}$$

FR is the flow rate of the carrier gas (Helium) through Cd zone in cc/min controlled by a dedicated mass flow controller.

The vapor pressure for Te is given by [105]:

$$P_{Te}(\text{torr}) = 10^{6.6385-\frac{4084.38}{T_{Te}+98.94}} \tag{21}$$

The flow rates for Te zone was calculated using the following equation:

$$\text{F.R (Te)} = \frac{(n_{Te}*R)*(T_{Te}+273)}{(P_{Te}*133.32)*\frac{10^{-6}}{\text{time (mins)}}} \tag{22}$$

In the above equation, T is the temperature of the Te zone, P_{Te} is the vapor pressure of the Te zone calculated from equation 20. n_{Te} is the number of moles of Te determined by the following equation:

$$n_{Te} = n_{Cd}/\ (\text{Cd/Te ratio}) \tag{23}$$

For a Cd/Te ratio of 1.0, the number of moles of Te is equal to the number of moles of Cd i.e. $n_{Te} = n_{Cd}$. Therefore, by plugging in the value of n_{Cd} (calculated from equation 18) for n_{Te} in equation 5, the flow rate of the Te zone can be determined. The temperatures of the zones were maintained at least 100 ° C above the respective meting points of Cd and Te (321 and 435° C respectively).

6.3 Initial Results on Alumina Substrate

6.3.1 Elimination of Powdery Deposits

Alumina was chosen as the substrate for the initial set of experiments. The gas phase Cd/Te ratio was varied from 0.3 (extreme Te-rich) to 3.0 (extreme Cd-rich). Gas phase nucleation is possible during the deposition process which may result in powdery deposits and therefore must be avoided. Various process variables such as flowrates, temperatures of the elemental zones and the substrate temperature (temperature of the substrate holder when the deposition was initiated) were optimized to eliminate gas phase nucleation. Elemental flowrates greater than 600 cc/min and temperatures above 460° C for Cd and 560° C for Te resulted in powdery deposits. It is possible that high mass transport increases the collisions in the gas phase and causes nucleation in that phase. The flowrates were varied between 250 cc/min to 400 cc /min for all the experiments conducted in this study. Powdery deposits were observed for substrate temperatures less than 550° C. Therefore, a minimum temperature of 550° C was used as a standard for all subsequent depositions. The substrate temperature increased from 550° C at the beginning of the deposition to around 580° C at the end of the deposition.

Table 8: Temperatures and flowrates for the Cd and Te zones used in this study

Cd/Te ratio	Condition	T(Cd) °C	T(Te) °C	F.R(Cd) cc/min	F.R.(Te) cc/min
1.0	Stoichiometric	435	535	400	400
0.7	Te-rich	435	568	400	400
0.7	Te-rich	435	535	350	500
1.4	Cd-rich	466	535	400	400
1.6	Cd-Rich	435	535	550	350

The gas phase Cd/Te ratio and therefore the CdTe stoichiometry can be controlled by changing either the temperature or the flowrates of the elemental zones. However, flowrate offers limited control over gas phase stoichiometry when compared to temperature since the vapor pressure varies exponentially with temperature. Therefore large Cd and Te overpressures can be achieved with relatively small changes in temperatures. For example, to change the Cd/Te ratio from 1.0 to 2.0, with the temperatures and flowrates of Te zone constant, the flowrate of the Cd zone has to be increased by 100%. The same change in ratio can be achieved by increasing the temperature of cadmium zone by 7%. The temperatures and flowrates for various Cd/Te ratios used in this study are shown in Table 8.

6.3.2 Film Morphology

After optimizing the process variables to eliminate powdery deposits, the samples were analyzed for structure using X-Ray Diffraction (XRD) and Scanning Electron Microscopy (SEM). Normalized XRD patterns are shown in Figure 23 for Cd/Te ratios 1.2, 1.1, 0.8, 0.9 and 0.8. All the films exhibited strong (111) preferential orientation. Elemental Cd or Te peaks were not observed.

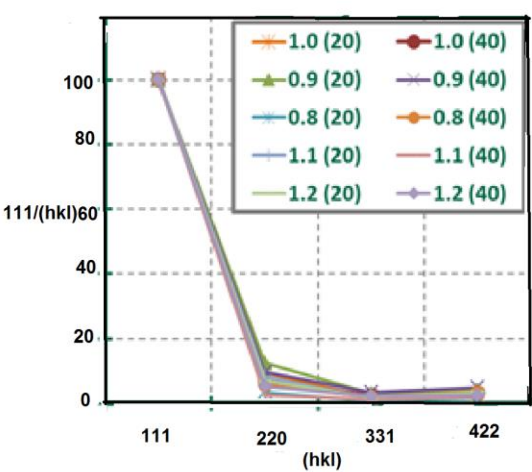

Figure 23: XRD plot for EVT-CdTe films with different CdTe ratios

SEM images of the EVT-CdTe films with different Cd/Te ratios are shown in Figure 24.The grain size increased as the Cd/Te ratio decreased from 2.0 to 0.5. The largest grains were observed for films with Cd/Te ratios 0.6 and 0.5. However, further decrease in Cd/Te ratio below 0.4 resulted in grain clustering (Figure). Although the film did not exhibit any powdery deposits, the clustering is believed to be due to gas phased nucleation.

6.3.3 Effect of Stoichiometry on Film Conductivity

To study the influence of stoichiometry variation on CdTe conductivity, temperature-resistivity measurements were conducted on films with different Cd/Te ratios. Four co-linear gold contacts sputtered (using DC sputtering) on EVT-CdTe films deposited on Alumina. 5Å Cu was then added on select films by RF sputtering. The films were annealed at 275°C for 20 mins to diffuse the Cu into the CdTe film. The resistivity of as-deposited films was too high to be measured at room temperature (RT) (300K) and below.

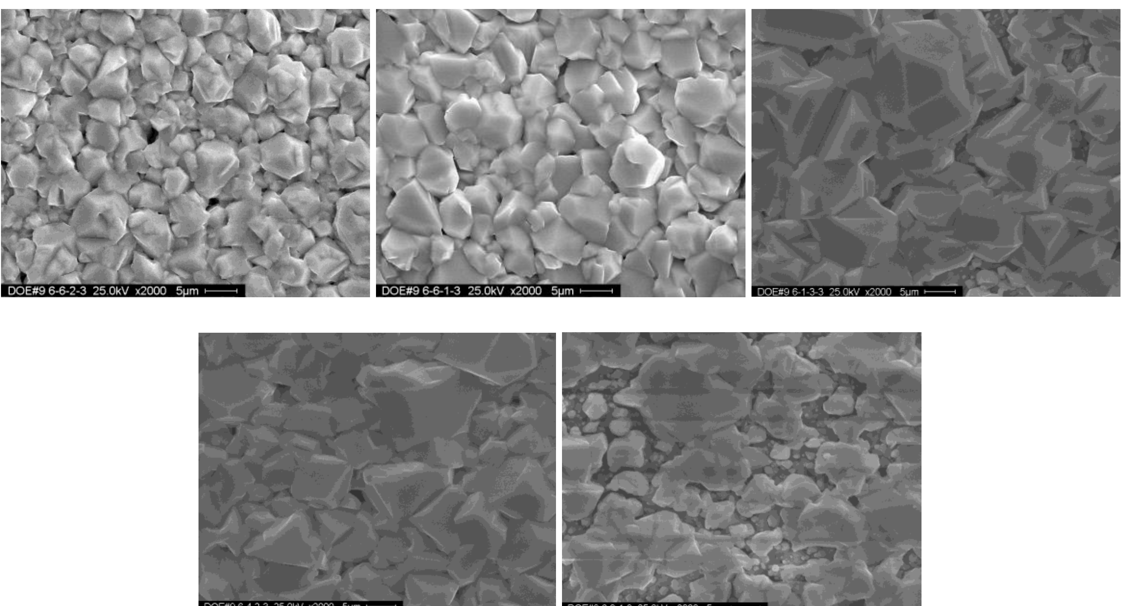

Figure 24: SEM images of EVT-CdTe on Alumina with Cd/Te ratios. Clockwise from top left: 2.0, 1.25, 0.6, 0.5 and 0.4

Cu decreased the resistivity of the films to 'measurable' values. The results presented in this section, are for EVT-CdTe films with 5Å Cu. Figure 25 shows the resistivity (σ) Vs 1000/T plot for Cd/Te ratios ~0.4 – 2.0. The film with Cd/Te ratio of 0.6 had the lowest resistivity at all temperatures (3 x 10^4 ohm-cm @ 300K), while Cd/Te ratio < 0.4 showed the highest resistivity (5x 10^5 ohm-cm @ 300 K).

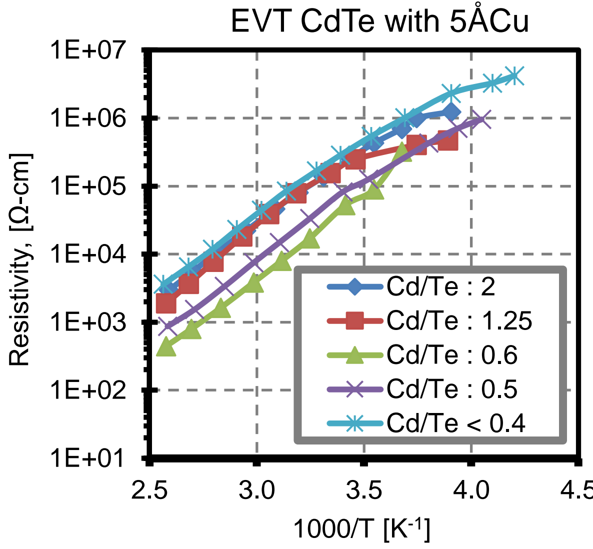

Figure 25: Resistivity vs. 1000/T for EVT-CdTe films deposited at different Cd/Te ratios and doped with Cu

The room temperature resistivity is plotted against Cd/Te ratio in Figure 26. As the Cd/Te ratio decreased from 2.0 to 0.6 resistivity decreased. Further decrease in Cd/Te ratio from 0.6 to 0.4, increased the resistivity. As the Cd/Te ratio decreased, (making the films more Te-rich), the concentration of V_{Cd}'s is expected to increase since the formation energy of V_{Cd}'s is lower under Te-rich growth conditions. Cu is known to occupy V_{Cd}'s to form acceptor defects Cu_{Cd}, therefore the concentration of Cu_{Cd} should also increase with decrease in Cd/Te ratio. Cu_{Cd} was calculated to be 0.22 eV above the VBM in CdTe which is shallower defect than V_{Cd} at 0.34 eV [64]. Therefore, the conductivity is expected to increase with Cu due to increased p-type doping. This explains the decrease in resistivity of the as-deposited films with Cu incorporation. The decrease in resistivity with Cd/Te ratio from 2.0 to 0.6 can be attributed to increase p-doping due to an increase in Cu_{Cd} concentration. However, the increase in Cu_{Cd} concentration should result in the Cd/Te ratio 0.4 film having the lowest resistivity which was not observed. SEM images in Figure 25 show poor grain quality for Cd/Te ratio 0.4 which could be detrimental for carrier mobility and hence lead to higher resistivity at the lower ratios. Therefore, the morphology of the film influences the resistivity.

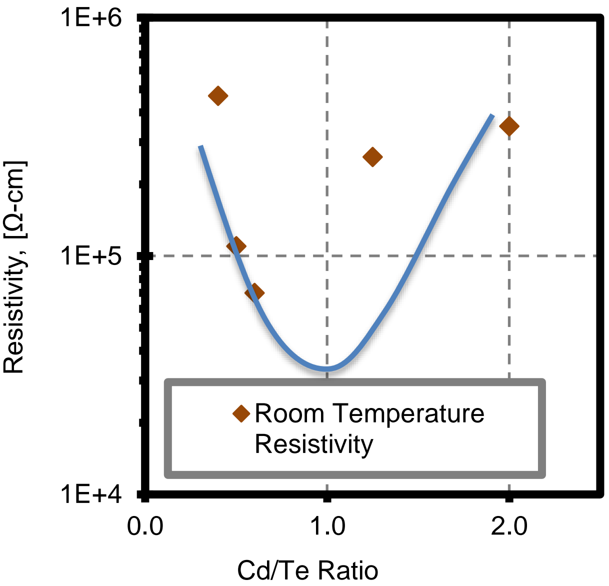

Figure 26: Room temperature resistivity Vs Cd/Te ratio

6.3.4 Summary of Key Findings from Results on Alumina Substrate

- Higher partial pressures of Cd and Te resulted in gas phase nucleation and powdery deposits. The optimum substrate temperature was found to be 550° C. Temperatures below 550° C resulted in powdery deposits.
- The grain size decreased with increase in Cd/Te ratio i.e. films deposited under Cd-rich growth conditions exhibited smaller grain sizes compared to the films deposited under Te-rich conditions. Films with Cd/Te ratio below 0.4 resulted in grain clustering.
- The resistivity change was affected by the Cd/Te ratio. The room temperature resistivity for the films with Cu decreased with decrease in Cd/Te ratio. The resistivity for the Te-rich films was lower than Cd-rich films. This could be due to the increase in the number of acceptor defects Cu_{Cd}'s.

6.4 Initial Results on 'CdS/TCO/Glass' Substrates

6.4.1 Introduction

After the initial experiments on Alumina, EVT films were deposited on 'CdS/TCO/glass' substrates with an intent to fabricate solar cells using the superstrate structure. The fabrication details were discussed in chapter 5. Nearly all samples were $CdCl_2$ heat treated (HT). Cu was added for select films to study its influence on CdTe stoichiometry. The structural properties as a function of CdTe stoichiometry were studied using X-Ray Diffraction (XRD) and Scanning Electron Microscopy (SEM) techniques. Solar cells were characterized using Current Voltage (JV) and Spectral response (SR) measurements. Capacitance Voltage measurements (CV) were conducted to estimate the carrier concentrations. Time Resolved Photoluminescence (TRPL) measurements were performed at the National Renewable Energy Laboratory (NREL) to study minority carrier lifetimes. Deep Level Transient Spectroscopy (DLTS) studies were conducted to study deep levels in EVT films. The results of above mentioned measurements will be presented in the subsequent chapters. In this chapter, the structural properties and mass transport effects of EVT- CdTe films are discussed.

6.4.2 Mass Transport

As mentioned earlier, the Cd/Te ratio can be changed by adjusting the elemental zone temperatures or flowrates. Experiments were conducted to investigate the individual impact of temperature

and flowrates on the growth rate of CdTe. The optimized depositions conditions established on the alumina substrates were used to set an upper limit for temperatures and flowrates of the elemental zones in order to avoid powdery deposits.

6.4.2.1 Effect of Elemental Zone Temperature

CdTe films with Cd/Te ratio 1.0 were deposited using different Cd and Te elemental temperatures and the thickness of the films was measured. Figure 27 shows the growth rate as a function of the Cd elemental zone temperature. The growth rate increased with increase in Cd and Te elemental zone temperatures. The vapor pressure increases exponentially with increase in temperature. Since the vapor pressure of Cd and Te determines the amount of material evaporated, the mass transfer and therefore the growth rate increases with increase in temperature.

6.4.2.2 Effect of Elemental Flowrate

To study the influence of elemental flowrate on growth rate, CdTe films with Cd/Te ratio 1.0 were deposited using different elemental flowrates of Cd and Te. The flowrates through both the zones were maintained to be the equal for all depositions. There was no significant change in growth rate with increase in elemental flowrate (Figure 27). The growth rate saturated for elemental flowrates above 100cc/min. This indicates that flowrate as low as 100cc/min through the elemental zones is sufficient to transport the evaporated material to the substrate. Increasing the flow rate would increase the velocity of the carrier gas and not cause additional evaporation of extra Cd and Te molecules. However, flowrates below 250 cc/min resulted in pinholes. This could be due to increased dilution of Cd and Te vapors. It should be noted that an increase in the elemental flowrates would result in an increase in the total flowrate of vapors in the mixing zone. For example, a flowrate of 400 cc/min through Cd and Te zones, the total flowrate in the mixing zone would be 2.8L/ min. (800 cc /min (Cd and Te) + 2L/min (mixing zone)). Increasing the elemental flow rate to 500 cc/min would increase the total flow rate to 3L/min.

6.4.2.3 Effect of Mixing Zone Flowrate

Figure 27 shows the effect of mixing zone flowrate on the deposition rate. The rate increased with increase in mixing zone flow. Multiple data points at the mixing zone flow of 2L/min correspond to different elemental flowrates. The observed trend suggests that a minimum flowrate is necessary to transport the

Cd and Te vapors from the mixing zone to the substrate. Mixing zone flowrates above 3L/min resulted in powdery deposits. A mixing zone flowrate of 2L/min was used as a standard.

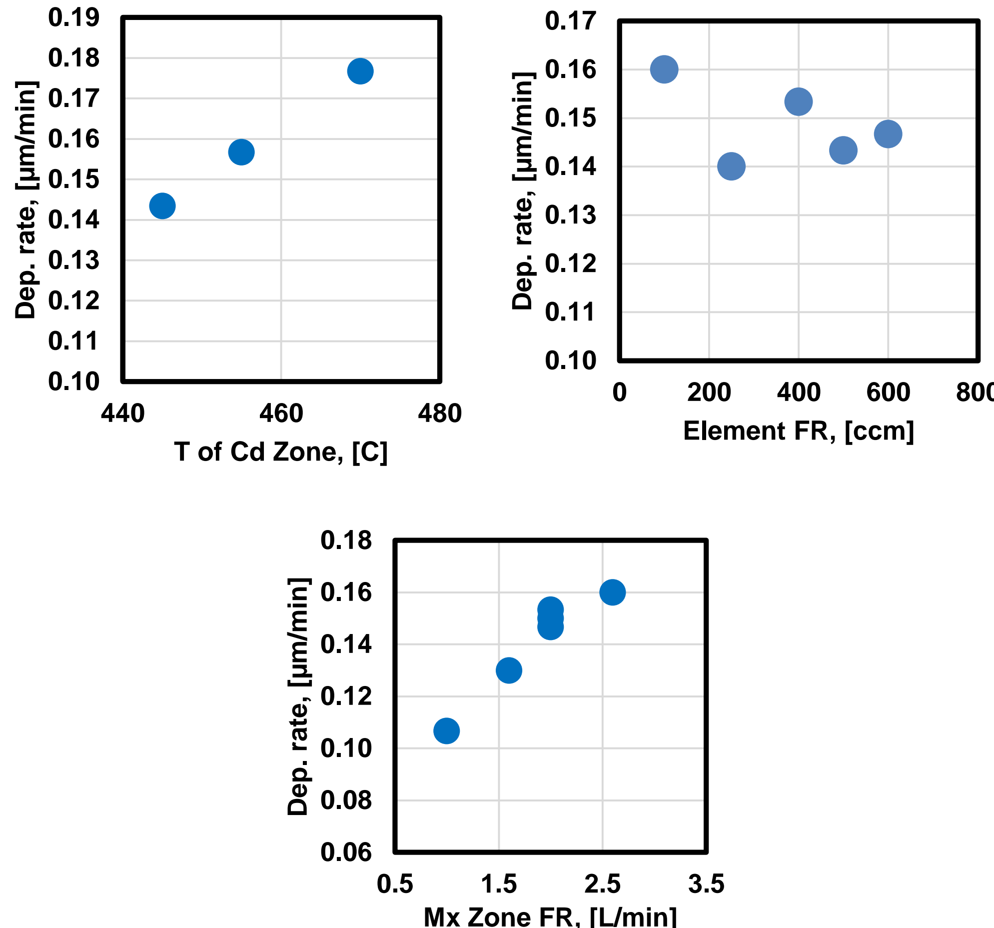

Figure 27: Growth rate as a function of Cd zone temperature, elemental flowrate and mixing zone flowrate. (Clockwise from left)

6.4.2.4 Effect of Cd/Te Ratio

The deposition rate showed a strong correlation to the gas phase Cd/Te ratio. The effect of Cd/Te ratio on the growth rate is shown in Figure 28 (left). Films deposited with Cd/Te ratio 2.0 were about 40% thinner than films grown with Cd/Te ratio 0.5 for the same deposition time, implying a slower growth rate for films deposited above stoichiometry (Cd/Te >1). The reason for the faster growth rate under Te-rich conditions is not fully understood at this point. However, a few speculations based on earlier studies could be made. One possibility is that the Cd gas phase molecules form a 'stagnant layer' at the substrate

preventing Te molecules to diffuse through the Cd layer to reach the substrate, consequently lowering the deposition rate for films grown above stoichiometry. Such hydrodynamics for MOCVD has been discussed earlier in [122]. Another possibility is the Eiley-Rideal mechanism described earlier [123] as a possible growth mechanism for CdTe. In this process, gas phase Te (Cd) molecules get adsorbed on the substrate. This is followed by the Cd (Te) molecules reacting with the adsorbed Te (Cd) molecules to form CdTe before the Te (Cd) molecules re-evaporate. If the re-evaporation rate of Cd is higher than Te, the formation of solid CdTe molecule could be slower.

6.4.2.5 Thickness Profile

The thickness of the CdTe layer showed a gradient across the area of the substrate. The top half was thicker than the bottom half and was used in cell fabrication. The thickness profile is shown in Figure 28 (right). Since the growth rate showed dependence on the Cd/Te ratio, the deposition times were adjusted to achieve a thickness of approximately 5 μm at the center of the substrate.

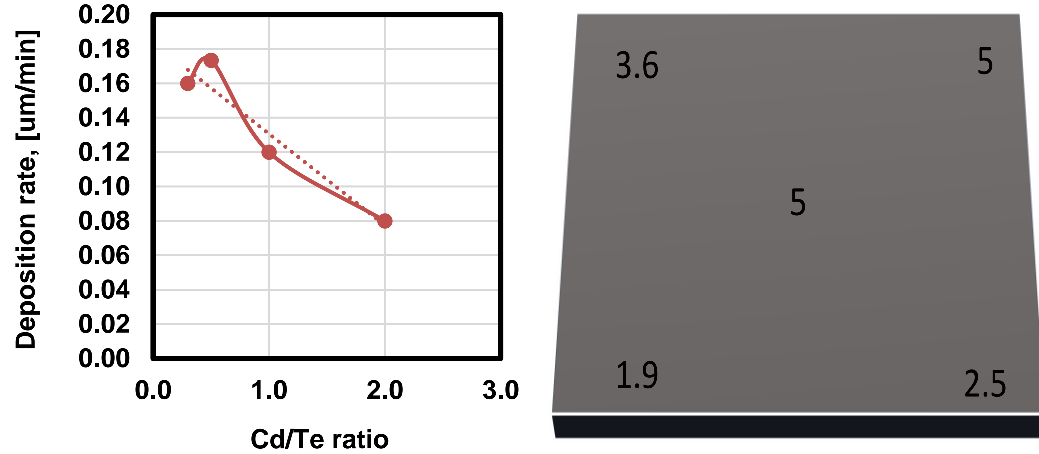

Figure 28: Growth rate as a function of Cd/Te ratio (left); thickness (in microns) profile on the substrate (right)

6.4.3 Structural Analysis

6.4.3.1 XRD Analysis

XRD studies were conducted to study the crystallographic orientation of the films. Figure 29 shows XRD data for Cd/Te ratios 0.3, 0.5, 1.0 and 2.0. The temperatures and flow rates used are described on the plot.

The sharp diffraction peaks at 2ϴ = 23.750°, 39.286°, 46.433°56.82°, and 76.56°correspond to the (111), (220), (311), (422) and (511) planes of the cubic CdTe structure [ICCCD Ref 015-0770]. All the films exhibit a strong (111) peak indicating preferential orientation along the (111) direction. The film with Cd/Te ratio 0.3 exhibited the higher degree of preferential orientation with peaks other than (111) almost non-existent. Increased crystal quality for Te-rich samples have been reported earlier [124]. The relative intensity of (220) and (311) peaks for the film with Cd/Te ratio 2.0 increased indicating a lower degree of preferential orientation. Similar result were reported previously for Cd-rich films [125]. For the temperatures and flow rates used here, ratio 0.3 appeared to have the better crystallinity compared to Cd/Te ratios 0.5, 1.0 and 2.0. The mass transfer rate was reduced by lowering the temperatures of the elemental zones. The XRD plot for Cd/Te ratios 0.5, 1.0 and 2.0 for lower mass transfer rates. The trend was similar to that of the films with higher mass transfer suggesting that the orientation is not effected by the deposition rate.

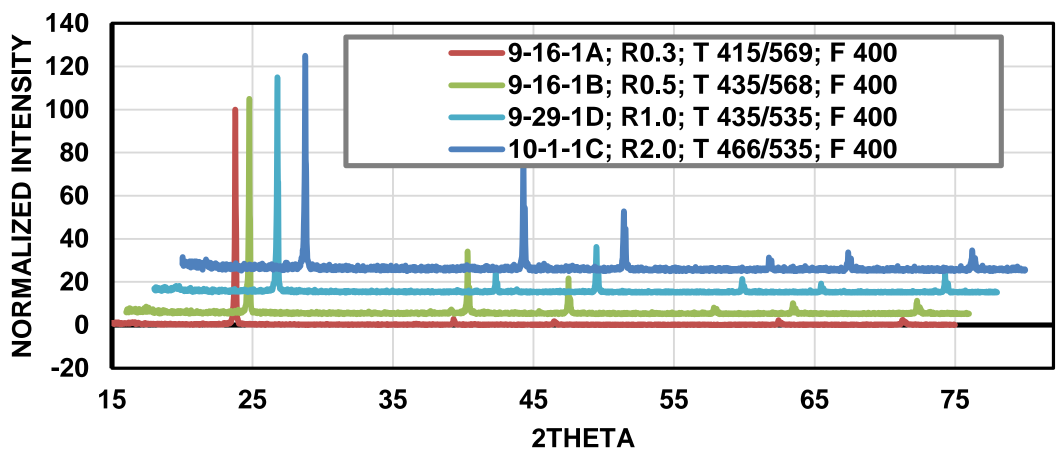

Figure 29: XRD plots for EVT-CdTe ratios 0.3, 0.5, 1.0 and 2.0

6.4.3.2 SEM Analysis

Figure 30 shows SEM images for Cd/Te ratios 0.3, 0.5, 1.0 and 2.0. The grains were densely packed and uniform throughout the sample. The grain size increased with decrease in Cd/Te ratio (i.e. increase in Te content). The largest grain sizes were observed for Cd/Te ratios 0.3. Increased grain growth is often linked to increase in deposition temperature [126]. However, the substrate temperature was not altered for any of the depositions. It was reported in an earlier study [124] that film growth in excess Te conditions could lead to improved grain growth by causing smaller grains to merge to form larger grains.

This claim is supported by the XRD results which show better orientation order for the Cd/Te ratio 0.3. Larger grain size can lead to better performance in the solar cell by reducing grain boundary defects.

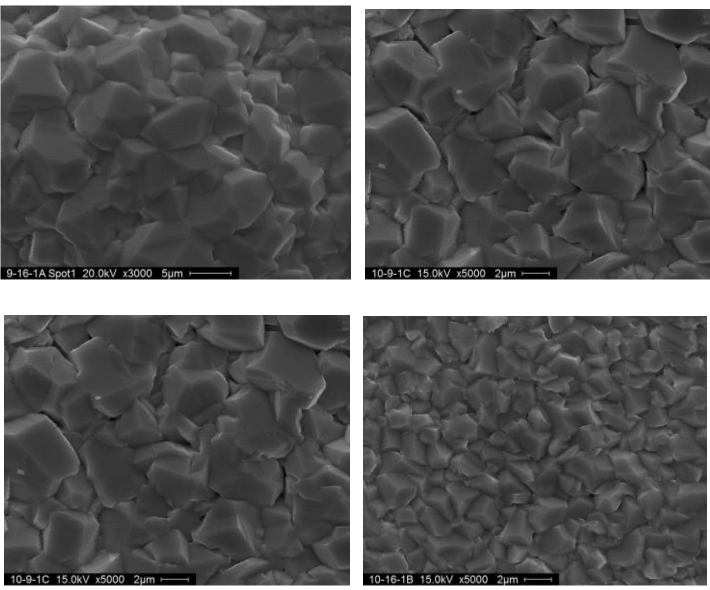

Figure 30: SEM images for Cd/Te ratios 0.3, 0.5, 1.0 and 2.0 (clockwise from left)

6.4.3.3 TEM and EDX Analysis

Figure 31 shows TEM images for an as-deposited (without $CdCl_2$ HT) CdTe films deposited at excess Te (left) and excess Cd (right) conditions. Both films showed grains extending through the thickness of the film of about 2 microns in diameter. Twin boundaries were observed in both films. No observable change was noticed in the TEM images with respect to change in Cd/Te ratio

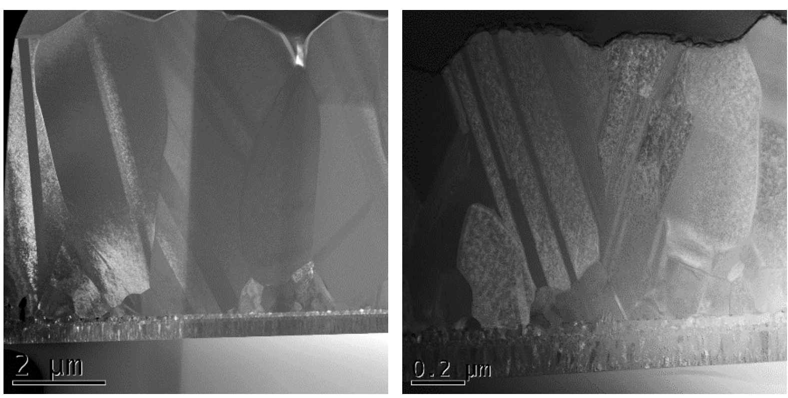

Figure 31: TEM images for as-deposited excess Te film (left) and excess Cd film (right)

6.4.4 Summary of Key Findings from Structural Analysis

- The growth rate showed a strong correlation to Cd/Te ratio. Films deposited under Te-rich conditions showed higher growth rates.
- XRD studies showed that films deposited under Te-rich conditions exhibited the highest degree of preferential orientation.
- The grain sizes varied with Cd/Te ratios. Films deposited under Te-rich growth conditions showed larger grains than the Cd-rich films

6.5 Solar Cell Fabrication

6.5.1 Cell Performance: As-Deposited Films (Without $CdCl_2$ HT)

After the preliminary morphology and growth studies, the next step was to fabricate solar cells with EVT-CdTe films and study the effect of CdTe stoichiometry on cell performance. For this purpose EVT CdTe films with Cd/Te ratios 0.5 (Te-rich), 1.0 (Stoichiometric), 1.4 and 2.0 (Cd-rich) were deposited. The superstrate structure used was Glass/TCO/CBD-CdS/EVT-CdTe/MoN. The experimental details of the solar cells fabrication were discussed in the previous chapters. In order to obtain high efficiency devices, $CdCl_2$ HT and Cu incorporation are necessary [83]. However, for these experiments these treatments were intentionally avoided to study the effect of CdTe stoichiometry on solar cell performance.

Solar cells showed poor performance (V_{OC} < 500 mV) for cells with all Cd/Te ratios. The Quantum efficiency (Q.E) is shown in Figure 32. The cells with Te-rich CdTe, (Cd/Te ratio < 1.0) showed better collection at all wavelengths. The cells with Cd-rich films on the other hand (Cd/Te ratio > 1.0), exhibited poor collection. These cells also showed increased collection at the longer wavelengths. The noteworthy detail is the shape of the Q.E curves. Typical high efficiency solar cells have Q.E. curves that resemble those of the cells with Te-rich (Cd/Te < 1.0) CdTe. In order to form an Ohmic contact to CdTe, the work function of the back contact metal has to be at least 5 eV. The work function of Mo is 4.37 eV and therefore, Mo forms a non-ohmic back contact to CdTe. The resulting Schottky barrier at the CdTe/Mo interface inhibits the collection of holes at the back contact causing roll-over in the JV characteristics. With a Schottky barrier at the back contact, the device now has two internal fields: The first one at the CdTe/CdS interface where majority of the collection is expected to occur; the second at the back junction due to the Schottky barrier formed at the Mo/CdTe interface. A weak electric field at the CdTe/CdS junction cannot separate

the carriers generated in its vicinity. This results in poor collection and hence poor QE. Cells with a Cd/Te ratio > 1.0 (Cd-rich) showed increased collection towards the longer wavelengths suggesting that the collection of photo-generated carriers is more towards the back of the device (away from the CdTe/CdS junction). Long wavelength photons have smaller absorption coefficients and travel longer distances before they can be absorbed. The increased collection towards the back shows that the carriers generated by the long wavelength photons are collected. This behavior is indicative of a stronger electric field at the CdTe/Mo junction than the one at CdTe/CdS interface. Growth under Cd-rich conditions promotes the formation of the donor defect, Cd_i which compensate the native acceptor defect V_{Cd}. It is possible that Cd-rich depositions make the CdTe intrinsic or possibly n-type due to the formation of Cd_i's. This would result in reduced band bending at the CdTe/CdS interface, lowering the strength of the electric field. Eventually the majority of the collection takes place at the back junction i.e. CdTe/Mo interface. The possible band diagram for both cases is also shown in Figure 32. The results suggest that the Cd/Te ratio can impact the conductivity of CdTe layer.

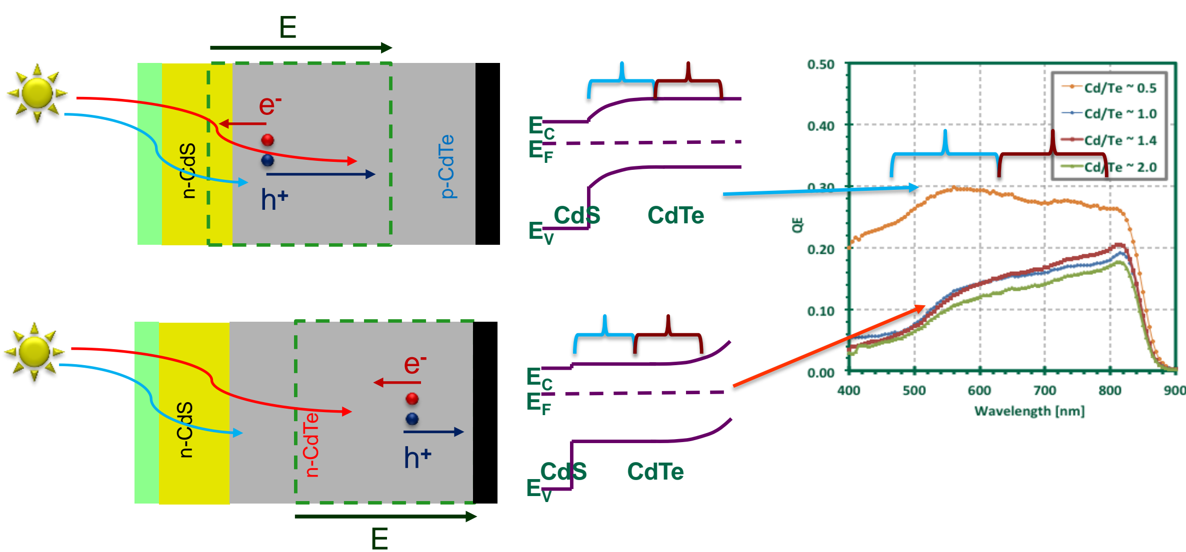

Figure 32: SR for EVT-CdTe without $CdCl_2$. The corresponding band diagram is also shown.

6.5.2 Cell Performance: With $CdCl_2$ HT

The effects of $CdCl_2$ heat treatment (HT) on CdTe solar cells has already been described earlier. In addition to improving the structural and the junction properties of CdTe (by promoting intermixing of CdS

and CdTe), Cl treatment is also known to improve the p-type conductivity of CdTe by forming the complex acceptor defects called the A-centers and also enhance grin boundary collection [53]. The $CdCl_2$ HT for 'standard' CSS based CdTe solar cells is performed in He and O_2 ambient In order to find the best annealing temperature for EVT-CdTe cells, the $CdCl_2$ HT was carried out at three temperatures: 375°C, 390°C and 410°C in He and O_2 ambient. EVT-CdTe films with Cd/Te ratios 0.5, 1.0 and 2.0 were used for these experiments. MoN/Mo was used as the back contact. Figure 33 shows the JV and Q.E. characteristics for cells heat treated at 390°C. The most evident observation is the vast improvement in Q.E for all Cd/Te ratios following the $CdCl_2$ HT. Ratio 1.0 showed better current collection compared to ratio 0.5 and 2.0. The better collection of ratio 1.0 could be an anomaly as it was not observed for other $CdCl_2$ annealing conditions. All films showed roll over which is due to the non-ohmic back contact. Figure 34 shows the V_{OC} for all ratios and $CdCl_2$ annealing conditions. The solar cell with Cd/Te ratio 0.5 showed higher V_{OC}'s for all $CdCl_2$ annealing temperatures. Higher annealing temperatures (410° C) reduced the V_{OC} for all Cd/Te ratios. Table 9 shows the V_{OC}, FF and J_{SC} values for 0.5 ratio film for varying $CdCl_2$ HT. For all the subsequent experiments 390° C annealing was used as the standard annealing condition.

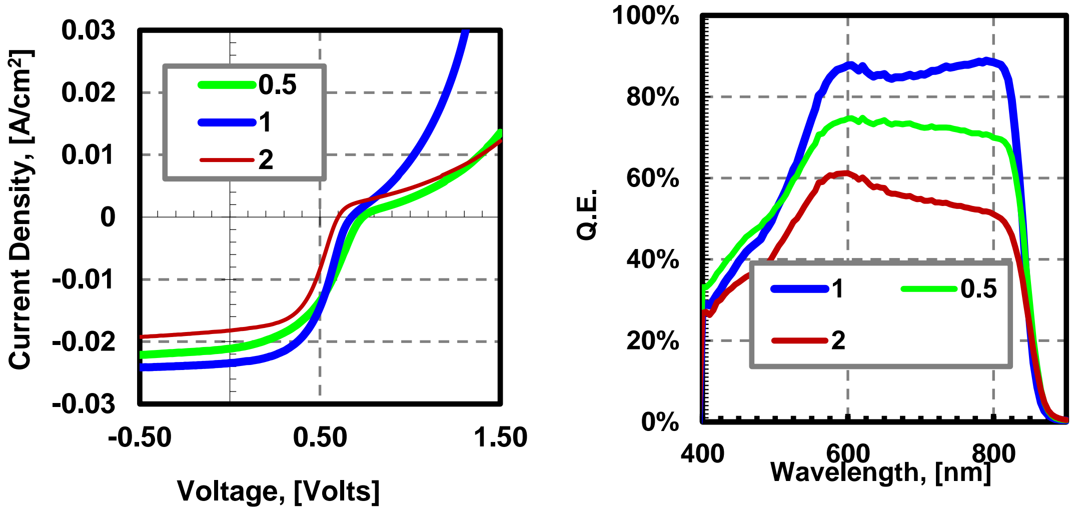

Figure 33: JV and SR for EVT CdTe ratios 0.5, 1.0 and 2.0 $CdCl_2$ HT at 390° C

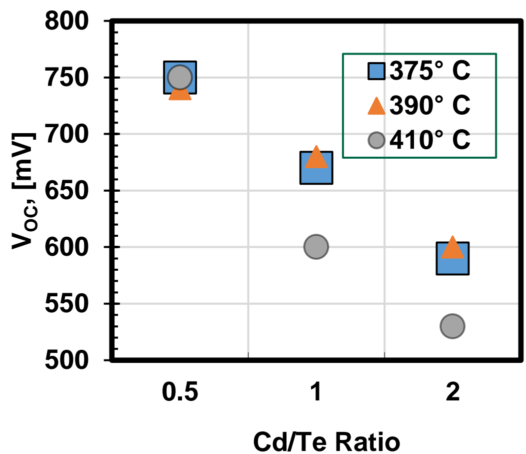

Figure 34: V_{OC}'s Vs Cd/Te ratios for various $CdCl_2$ annealing temperatures

Table 9: V_{OC}, FF and J_{SC} for cell with Cd/Te ratio 0.5 and different $CdCl_2$ HT

$CdCl_2$	Voc	FF	Jsc
410	750	39.10%	18.23
390	740	44.00%	18.75
375	750	52.40%	21.89

EDX mapping (shown in Figure 35) on *excess* Te film showed regions rich with Cd and O_2 within CdTe just above the CdS layer. $CdCl_2$ HT caused remarkable changes in the morphology. The twin boundaries became more prominent and O was introduced in the grain boundaries near the surface. Cl segregation along the grain boundaries and S diffusion into the CdTe layer was also observed (Figure). Cl segregation along GB in $CdCl_2$ HT films was demonstrated earlier in numerous other studies [127,128,129]. It is well known that one of the benefits of $CdCl_2$ HT is enhanced S diffusion into the bulk of CdTe which improves the overall performance [130]. This could be the reason for the overall improvement in performance for all Cd/Te ratios following the $CdCl_2$ HT.

The better performance of the cells with Te-rich CdTe (Cd/Te ratio 0.5) could be a result of increased p-doping following the $CdCl_2$. The formation energy for V_{Cd}'s is lower under Te-rich growth conditions. During the $CdCl_2$ HT, Cl forms donor defects Cl_{Te} which combine with V_{Cd}'s to form shallow acceptor complex defects viz. A-center [53]. The better performance of the cell with Cd/Te ratio 0.5 could be due to an increase in A-center concentration. However, the formation of A-centers is limited by the

presence of V_{Cd}'s. In the case of Cd-rich films, the availability of V_{Cd}'s is limited and therefore, Cl forms compensating donor defects Cl_{Te}. At higher annealing temperatures, the Cl concentration could exceed the V_{Cd} concentration and therefore the concentration of Cl_{Te} increases resulting in lower doping and hence V_{OC}'s.

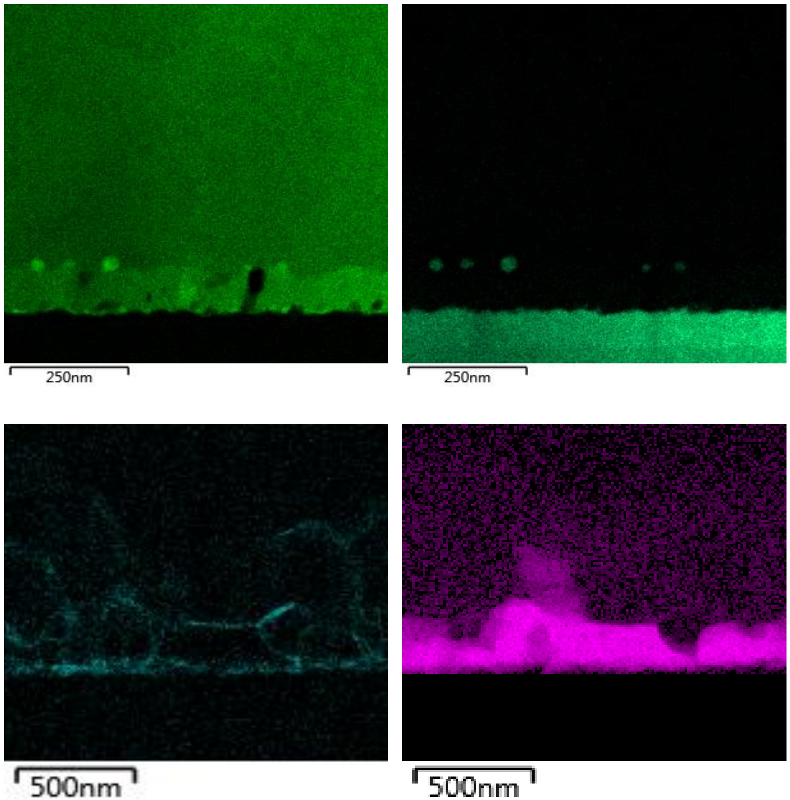

Figure 35: EDX map for Cd (left) and O (right) and Cl segregation at grain boundaries and S diffusion for as-deposited EVT film deposited in excess Te conditions

6.5.3 Cell Performance: Flow Rate as the Control Variable

As mentioned earlier, the Cd/Te ratio can be changed using either temperature or the flowrates of the elemental zones. In the above experiment, the Cd/Te ratio was altered by controlling the elemental zone temperature. It was mentioned earlier that the change in Cd/Te that can be achieved by using flowrate as the control variable is limited. To compare solar cell performance by changing Cd/Te ratios with flowrates and temperatures, solar cells were fabricated using CdTe films with Cd/Te ratios 0.8 (Te-rich), 1.0 and 1.6 (Cd-rich) by controlling the flowrate of Cd and Te zones. Cu-free Graphite was used as the back contact. All films were heat treated with $CdCl_2$ at 390° C in He and O_2 ambient. Figure 36 shows the JV and Q.E.

curves for the above mentioned films. The V_{OC}'s did not change with Cd/Te ratios in this case which is consistent with the change in growth rate vs. Cd/Te ratios with variable flowrates. The Cd-rich cell shows reduced collection and FF. It was demonstrated earlier that a flowrates above 100 cc/min do not increase the mass transport of Cd and Te vapors to the mixing zone. Therefore, changing the elemental flowrates would have little or no effect on the gas phase Cd/Te ratio and therefore the cell performance. Flowrates below 100 cc/min should be used to realize the effect of Cd/Te ratio on cell performance. However, such low flowrates resulted in the formation of pinholes. Though the cell with Cd-rich CdTe (ratio 1.6) showed a variation in JV and SR from, the difference in V_{OC} was not significant. Therefore, temperature is a better control variable to observe the effect of Cd/Te ratio on cell performance.

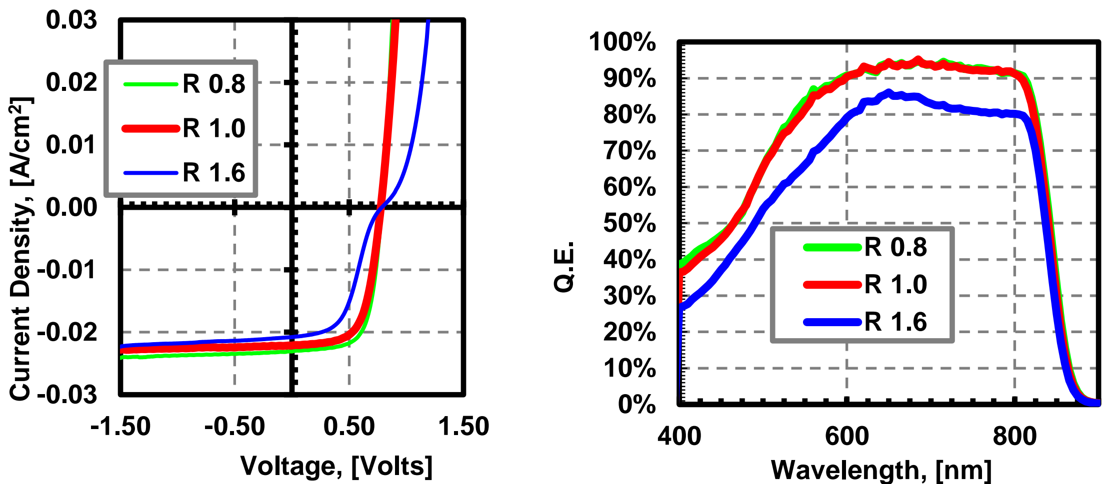

Figure 36: JV and Q.E. curves for Cd/Te ratios 0.8, 1.0 and 1.6 where the ratio was changed using flowrates

6.5.4 Summary of Key Findings from Cell Performance with Variable Flow Rates

- CdTe films with Cd/Te ratios > 1.0 (Cd-rich) could become n-type causing poor collection at the CdTe/CdS junction suggesting that conductivity of EVT-CdTe can be adjusted using appropriate Cd/Te ratios.
- $CdCl_2$ HT is necessary to obtain good solar cell performance for all Cd/Te ratios. 390° C was found to be the optimum annealing temperature and was used for all subsequent experiments.

- The main ramification of this set of experiments was the higher V_{OC}'s for the cells with Te-rich CdTe. Cd/Te ratios 0.5 showed better V_{OC}'s than 1.0 and 2.0 with $CdCl_2$ HT
- Ratio change with FR did not show any change in cell performance and therefore, the Cd/Te ratio was changed by using the elemental zone temperature as the control variable for subsequent experiments.

6.6 Adhesion Issue

6.6.1 Introduction

Though the cells with Cd/Te ratio 0.5 ratio exhibited higher V_{OC}'s the cells frequently flaked during subsequent processing steps; especially during the $CdCl_2$ rinse and back contact etch (performed using Br-Methanol solution). As a result, the performance was not consistent from cell to cell on the same substrate. The variation in V_{OC} for the cells on the same substrate with Cd/Te ratio 0.5 and 2.0 is shown in Figure 37.

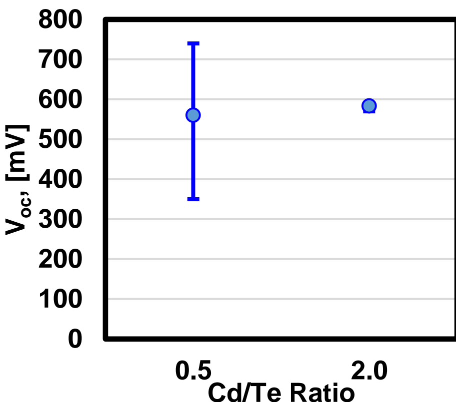

Figure 37: Variation in V_{OC} for cells on the same substrate for ratios 0.5 and 2.0

The huge error bar on the 0.5 ratio cell is not seen on the cell with ratio 2.0. SEM cross section images revealed the presence of voids at the CdTe/CdS interface (shown in Figure 38). No voids were observed for the Cd/Te ratio 2.0 sample. It has been reported in an earlier study that faster growth rate causes voids and discontinuities in grains due to rapid growth of adjacent faces [131]. In this study, films which exhibited voids were deposited at higher growth rate. Therefore, it is possible that the higher growth rate for Te-rich films is the reason for the presence of voids. The variation in V_{OC} could be a result of pinholes

formed during processing steps as a result of poor adhesion/void presence. In order to improve adhesion and reduce inconsistencies, two approaches were used:

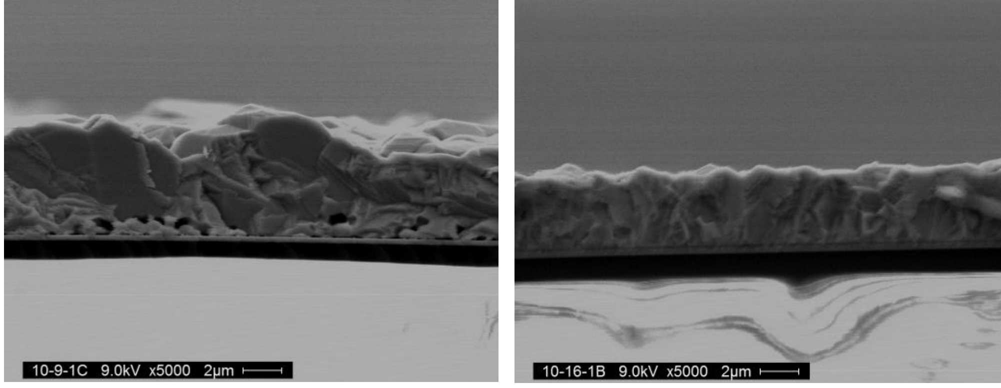

Figure 38: SEM cross sections for Cd/Te ratios 0.5, 2.0. Voids are present for the 0.5 ratio film.

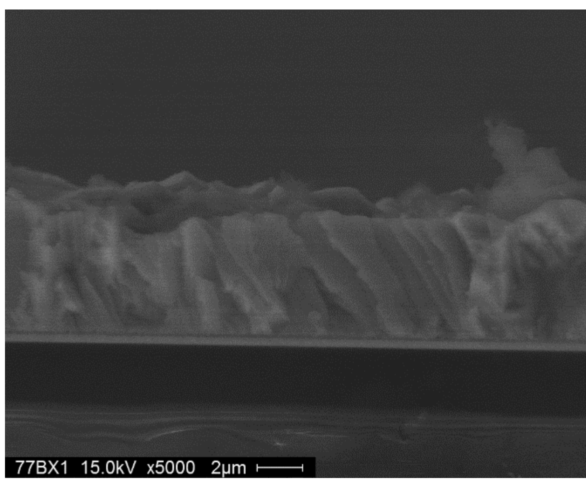

Figure 39: SEM cross section for ratio 0.7 film

1. Reduced Ratio window
2. 2-layer deposition

6.6.2 Reduced Ratio Window

Since films deposited at Cd/Te ratios below 0.5 flaked, solar cells were fabricated using CdTe films with Cd/Te ratios 0.7, 1. aand 1.4. The SEM images showed larger grain sizes for films with Cd/Te ratio 0.7. The cross sections did not reveal any voids and no flaking was observed for the 0.7 ratio films (Figure 39). The JV and Q.E for these cells are shown in Figure 40. Solar cells made with Cd/Te ratio 0.7 (Te-rich)

exhibited the highest V_{OC} of 800 mV. The roll-over was present due to a non-ohmic back contact present in all cells.

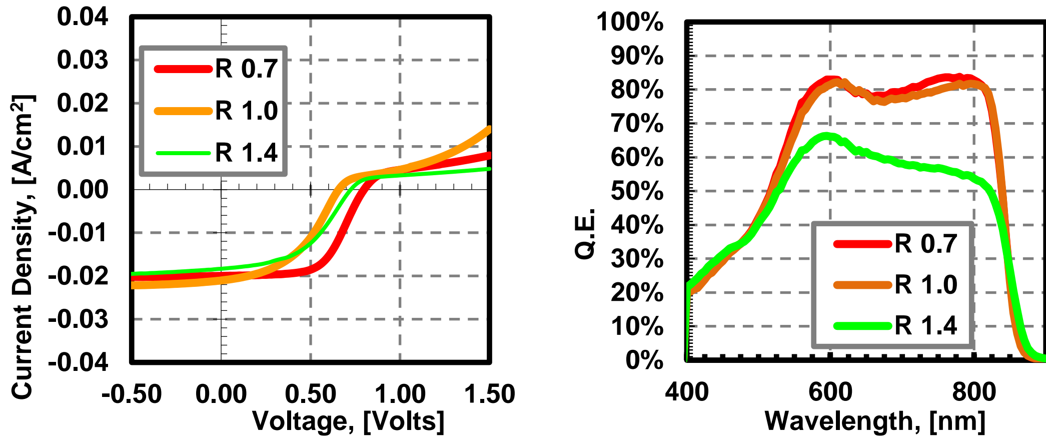

Figure 40: JV and SR for Cd/Te ratios 0.7, 1.0 and 1.4

Figure 41 (left) shows the measured carrier concentrations from Capacitance – Voltage measurements for $CdCl_2$ annealing temperatures 375 and 390° C as a function of Cd/Te ratio. The doping for Cd/Te ratio 0.7 was higher than ratio 1.0 and 1.4. Also, the doping for 390° C $CdCl_2$ HT was higher. The error bars indicate the highest and lower carrier concentrations obtained from the doping vs depletion width profile shown in Figure 41 (right). An order of magnitude higher doping was observed for Te-rich samples

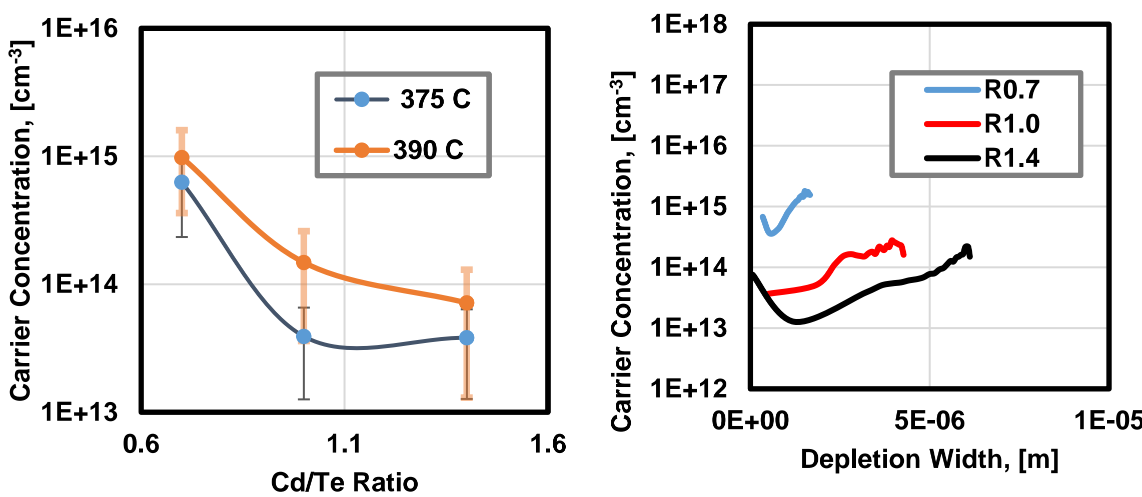

Figure 41: Doping concentrations Vs Cd/Te ratios (left) for different $CdCl_2$ annealing temperatures

(3×10^{14} cm^{-3}), compared to Cd-rich (1×10^{13} cm^{-3}) deposited films. $CdCl_2$ HT improves the carrier concentration by forming complex defects called A-centers. However the formation of A-centers is limited by the availability of V_{Cd}'s. In case of Cd-rich conditions, the availability of V_{Cd}'s is limited and therefore Cl forms compensating donor defects Cl_{Te}. The V_{oc}'s showed good correlation to the carrier concentrations.

6.6.3 2 Layered Depositions

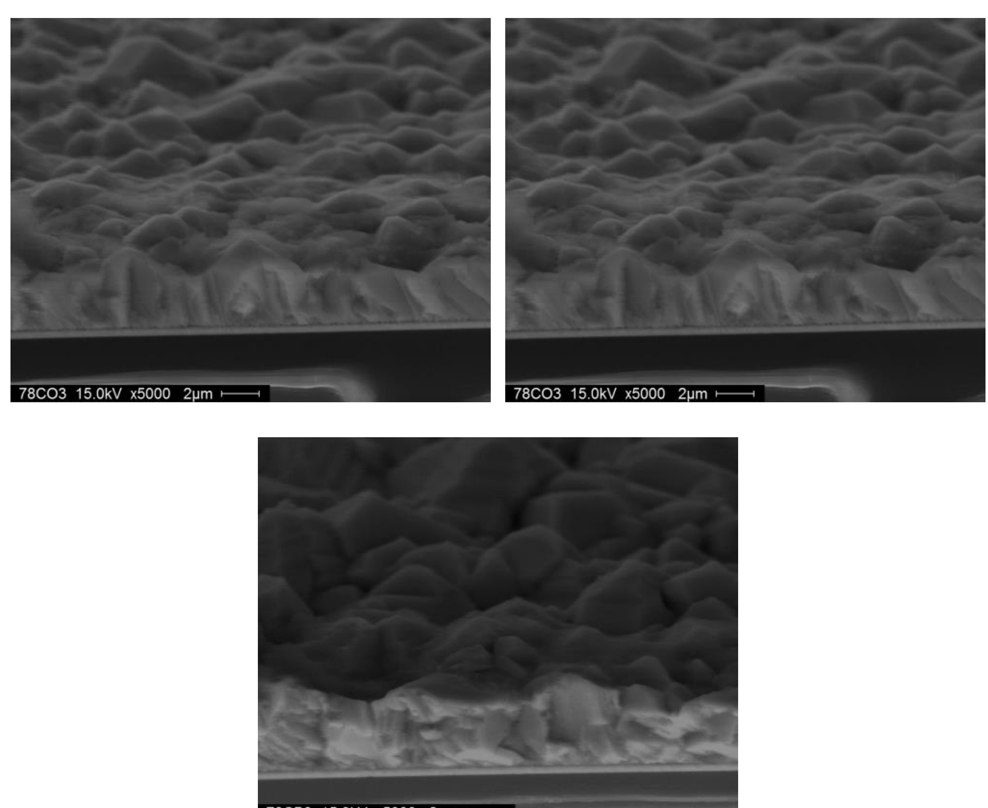

Figure 42: SEM cross section images for Cd/Te ratios 0.7, 0.5 and 0.3 with a starting layer of ratio 1.0

Alternatively, films were deposited in two layers. The initial layer was Cd/Te ratio ≥1 (which showed better adhesion to CdS layer) followed by a second layer of Cd/Te ratio <1. The initial layer was timed to achieve an estimated thickness of 0.5 μm while the overall film thickness was aimed to be 5 μm. Since the thickness of the initial layer was only 10% of the total thickness, the second layer was also expected to influence the performance of the solar cell on par or slightly more than the initial layer. Two sets of samples were deposited using this approach: First set had Cd/Te ratios 0.3, 0.5 and 0.7 with initial layer of Cd/Te ratio 1.0 and second set with an initial layer of ratio 2.0. The flaking observed in single layer depositions

was not observed in two-layered depositions. Figure 42 shows SEM cross section images for films deposited with Cd/Te ratios 0.3, 0.5 and 0.7, with an initial layer of Cd/Te ratio1.0. All films showed grains extending along the cross-section with no signs of voids. Similar growth was observed for the films with initial layer of Cd/Te ratio 2.0. Solar cells showed consistency and repeatability in performance for Cd/Te ratios as low as 0.3. Figure 43 shows the JV characteristics for solar cell with Cd/Te ratio 0.7 with 1.0 and 2.0 as the initial layers. The cells with initial Cd/Te ratio 1.0, performed better with a V_{OC} of 790 mV compared to 740 mV for the cell with initial layer of ratio 2.0. Though the variations in V_{OC} on different cells on the same substrate was eliminated, the cell performance did not show variation as a function of Cd/Te

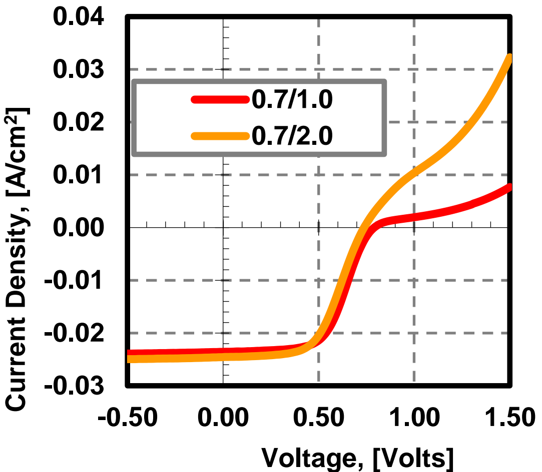

Figure 43: JV curve for Cd/Te ratio 0.7 with starting layer of ratio 1.0 and 2.0

ratio. This shows that the initial layer has a larger impact on the performance than anticipated, shadowing the effect of Cd/Te ratio. Figure 44 shows the variations in V_{OC} for ratio 0.5, 0.7 and 0.7 with initial layer of 1.0.

6.6.4 Summary of Key Findings from Adhesion Issues

- Cells fabricated with Cd/Te ratios < 0.5 flaked, possibly due to fast growth rate; two approaches were used to improve CdTe adhesion to CdS: a) Reduced ratio window b) 2-layered method

- Both the approaches helped in eliminating the flaking observed for CdTe films grown under Te-rich conditions. The variations in V_{OC}'s on the same substrate were eliminated with both the approaches.

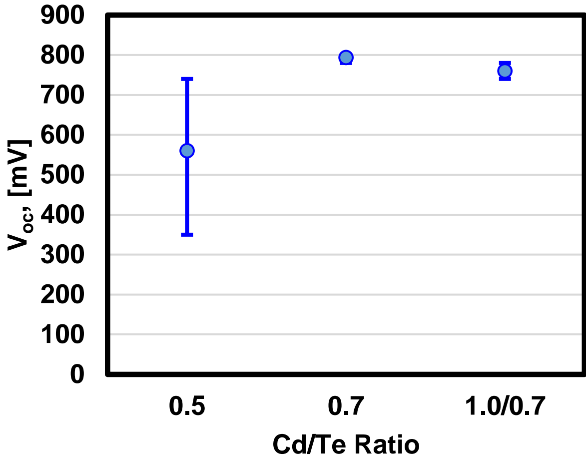

Figure 44: Variation in V_{OC} for cells on the same substrates for Cd/Te ratio 0.5, 0.7 and 0.7 with a starting ratio of 1.0

- The cells made with Cd/Te ratio of 0.7 showed the best V_{OC} of 800 mV. Te-rich growth conditions appear to yield higher V_{OC}'s.
- The carrier concentrations for Te-rich samples was higher than Cd-rich samples and correlates with observed V_{OC} trends

6.7 Cu Effects

6.7.1 Introduction

Cu is known to play an important role in improving the performance of CdTe solar cells. It is believed to serve two purposes. Firstly, Cu forms substitutional acceptor defects (Cu_{Cd}) by occupying V_{Cd}'s. Cu_{Cd} was found to be 0.22 eV above VBM and therefore, being shallower than V_{Cd}'s Cu improves the p-type conductivity of the CdTe. Secondly, it is used in the back contact formation to form an ohmic contact to CdTe. Cu is predominantly used in combination with materials like Au, Mo and graphite to create a heavily doped CdTe layer thereby forming a tunnel junction for the holes [112]. However, Cu is also known to have adverse effects on device performance. Excess Cu can form Cu_i which is a shallow donor level, and leads to compensation of p-type Cu_{Cd} [132]. It is also known to diffuse rapidly in CdTe and deteriorate the

performance of the solar cell by forming recombination centers and shunt paths at the CdTe/CdS junction reducing the minority carrier lifetime. Therefore, the amount of Cu must be optimized in order to achive long term stability and maximum device performance.

6.7.2 Experimental Details and Results

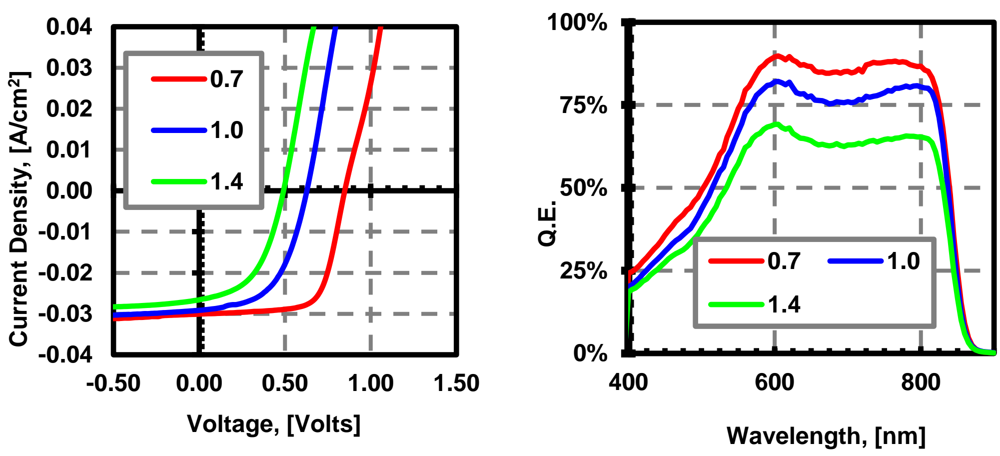

Figure 45: JV (left) and SR (right) for Cd/Te ratio 0.7 and 5 Å Cu

In this study, Cu has been deposited on select samples to investigate its effect vs CdTe stoichiometry. Cu has been added after the MoN/Mo back contact and the films were annealed at 275° C for 20 minutes. Figure 45 shows JV and Q.E characteristics for solar cells with Cd/Te ratios 0.7 (Te-rich), 1.0(stoichiometric) and 1.4(Cd-rich). While the cell with Cd/Te ratio of 0.7 showed a V_{OC} of 800 mV and 60.1 % FF, adding 5 Å Cu increased the V_{OC} to 850 mV and FF to 70%. In addition, Cu also reduced the roll-over significantly for all the Cd/Te ratios which indicates a reduced Schottky barrier at the back contact. The hypothesis is that Cu occupies the V_{Cd}'s which are present in excess in the CdTe film with Cd/Te ratio 0.7 ratio forming a high concentration of Cu_{Cd} thereby increasing the p-type doping [132]. For the 1.4 ratio cells, the concentration of V_{Cd}'s is expected to be significantly lower and therefore Cu forms donor defects i.e. Cu_i resulting acceptor in compensation and therefore lower V_{OC}'s.

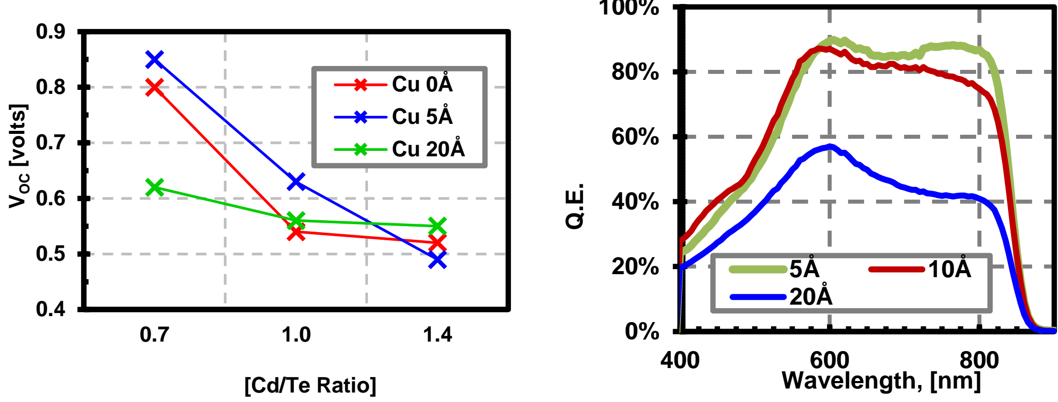

Figure 46: Change of V_{OC} with different Cu concentrations (left) SR for Cd/Te ratio 0.7 with varying Cu (right)

The performance of all cells deteriorated with increasing Cu concentration. The V_{OC} for the three ratios and spectral response for Cd/Te ratio 0.7 with varying amounts of Cu is shown in Figure 46. The current collection decreased in the long wavelength regions for the cell that received 10 Å Cu. 'Excessive' amounts of Cu, (20 Å) drastically reduced the performance yielding the lowest collection through the entire wavelength range. Similar trends were observed for Cd/Te ratios of 1.0 and 1.4. Such poor collection throughout the spectrum indicates a poor carrier lifetimes. Excess Cu is known to diffuse to the CdTe/CdS interface and form recombination centers which are harmful for carrier lifetimes. The measured carrier

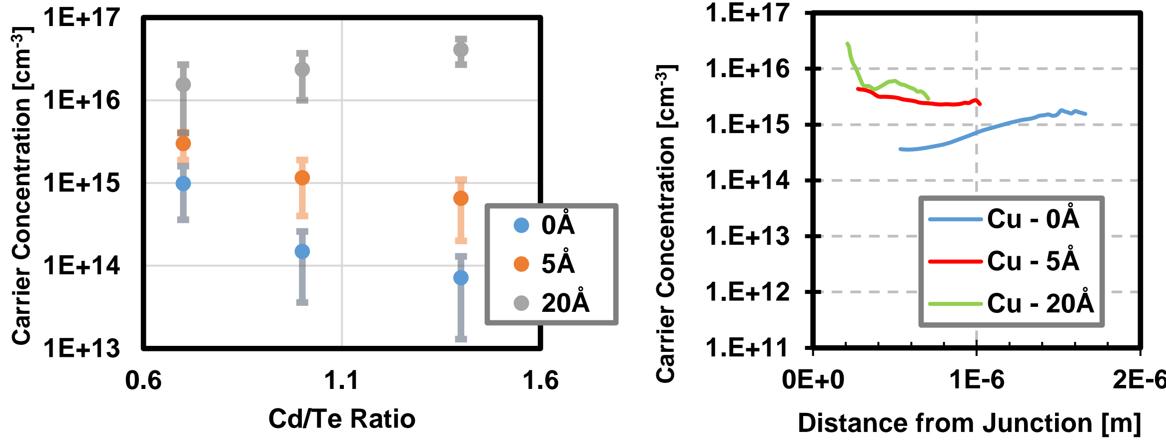

Figure 47: Carrier concentrations (left) and doping profile (right) for Cd/Te ratios 0.7, 1.0 and 1.4 with different Cu concentrations (left)

concentrations of the EVT CdTe devices with varying Cd/Te vapor ratios and Cu amounts are shown in Figure 47. The carrier concentration for the cells with no Cu was the same as the ones shown in the previous section in Figure 41. A 5Å Cu dose increased the doping for all ratios with same ratio dependence as the case with no Cu (higher doping for Te-rich films). The ratio dependence is reversed for 20Å Cu dose with the films deposited under Cd-rich conditions showing higher doping (in the order of 10^{16} cm^{-3}) compared to the films grown under Te-rich conditions.

For the cells with No Cu and 5Å Cu, the trend in doping corresponds to the trend in V_{OC}. However, the apparent higher doping concentration from CV measurements did not translate into higher V_{OC} for the cells that received 20Å Cu. The hole concentration profile (Figure 47) indicates shorter depletion width for higher Cu concentrations. As the net doping increases the depletion region decreases, causing a reduction in photo-generated carrier collection due to increased recombination. Hence, excess Cu decreases V_{OC} and FF [116].

6.7.3 Summary of Key Findings from Cu Dose vs. Cd/Te Ratio Experiments

- Cu improved the V_{OC}'s for cells with Cd/Te ratio 0.7 (Te-rich) more than the higher Cd/Te ratio cells.
- Optimum amounts of Cu improves performance while excess Cu is detrimental to the device efficiency

6.8 Minority Carrier Lifetime Measurements

6.8.1 Measurement Technique

Minority carrier lifetime measurements were performed at the National Renewable Energy Laboratory (NREL) with single photon excitation (1PE) and two photon excitation (2PE) time resolved photoluminescence (TRPL) measurements [133]. The carriers were excited from the glass side through the window layer (CdS) with 700 nm (1PE) and 1200 nm (2PE) wavelength laser beam and the TRPL signal was detected at 840nm wavelength. The measurements were performed on completed CdTe solar cells the results of which were presented in the earlier sections. The thickness for all the samples was about 5 µm. The cells had the following structure: Glass/TCO/CdS/EVT-CdTe/MoN/Mo. The cells were excited from the glass side. Cu was added on select samples to study the change in lifetimes as a function of Cu concentration and CdTe stoichiometry.

6.8.2 Observations and Results

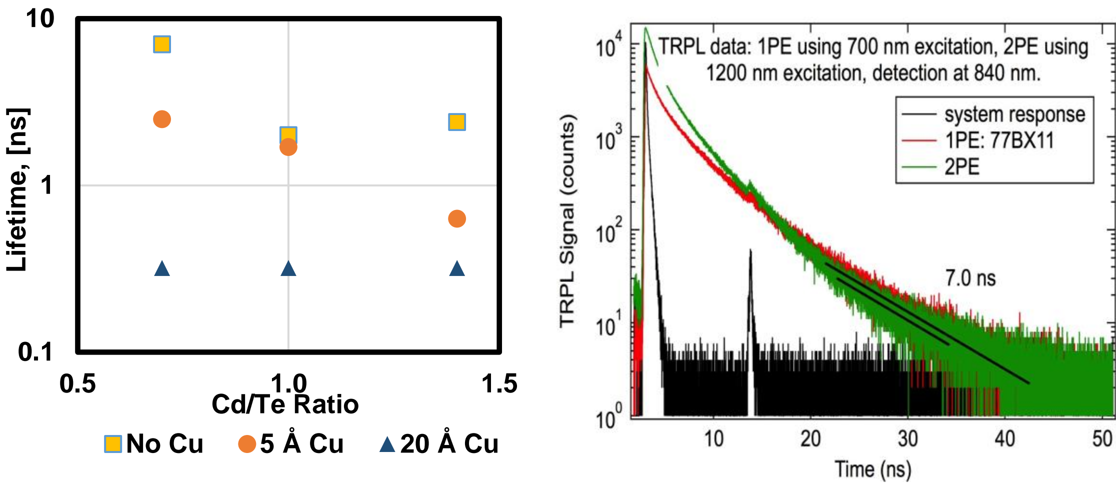

Figure 48: Lifetimes for Cd/Te ratios 0.7, 1.0 and 1.4 with various CU concentrations (left); TRPL data for Cd/Te ratio 0.7 (right)

The TRPL measurements indicated a strong correlation between minority carrier lifetime and Cd/Te ratio. TRPL measurements on as-deposited films yielded very low minority carrier lifetimes, close to system response. The $CdCl_2$ HT, improved the lifetimes significantly. The carrier lifetimes for different ratios and Cu concentrations are shown in Figure (left). The values are also tabulated in Figure 26.

The highest carrier lifetime of 7 ns was for a cell with Cd/Te ratio 0.7 and the lowest lifetime of 2 ns was observed for a cell with Cd/Te ratio of 1.4. The TRPL data for the 0.7 ratio cell is shown in Figure. (right). Cu incorporation reduced lifetimes for all Cd/Te ratios. The lowest lifetimes were measured for 20Å Cu where the lifetimes were close to system response.

6.8.3 Carrier Lifetimes: Discussion

Te-rich growth conditions favor the formation of various mid gap states like Te_{Cd}, Te_i etc. which act as SRH recombination centers lowering minority carrier lifetime. Therefore as-deposited CdTe is expected to have higher lifetimes under Cd-rich when compared to Te-rich growth conditions. However, the lifetimes for all as-deposited samples were too low to be measured. The performance of these films was poor and the results were shown in earlier sections. The $CdCl_2$ HT improved the lifetime for Cd-rich, stoichiometric and Te-rich deposition conditions. The cells with Te-rich CdTe exhibited higher lifetimes. This suggests that $CdCl_2$ heat treatment improved the lifetimes to a greater extent for the cells with Te-rich CdTe.

In addition to point defects, polycrystalline CdTe has a high density of different types of planar defects and grain boundary (GB) defects. As is the case with native point defects, planar and GB defects also create electronic states within the bandgap. If these states are deep, they can act as SRH recombination centers and reduce carrier lifetimes. Lamellar twins and Stacking faults are common planar defects in CdTe. Both these defects do not create deep levels as they do not contain dangling bonds [134]. On the other hand, GB defects introduce deep defects in CdTe. According to the double positioning twin boundary model, polycrystalline CdTe has two main types of GBs, referred as Cd-core and Te-core [135]. Cd-core GBs are identified by Cd-terminated grain interface, and Te-core by Te termination. ToF-SIMS study by D. Mao et al. has identified that more than 90% of the Cl in $CdCl_2$ treated CdTe is concentrated along the grain boundary [136]. The reason for this is the low formation energy of Cl related defects (Cl_{Te}, Cl_i) in the GB than the bulk of CdTe. In a Te-core GB, both substitutional (Cl_{Te}) and interstitial chlorine (Cl_i) has lower formation energy than that in Cd-core [137]. More Cd-core GBs are expected in a Cd-rich deposition condition, and Te-core GBs in Te-rich films. As a result, Cl incorporation is likely to passivate the grain boundary related deep states in Te-rich samples more effectively than Cd-rich samples, resulting in a better minority carrier lifetime. Cl segregation at the GB was found in EVT-CdTe films too. (The line scan for EDX analysis was shown earlier).

Table 10: V_{OC} of different deposition ratio CdTe cells with their measured carrier concentration and minority carrier lifetime

Cd/Te Deposition Ratio	Cu Dose(Å)	Doping Conc. (cm^{-3})	1PE Lifetime (ns)	2PE Lifetime (ns)	V_{OC} (volts)
0.7	0	3.6×10^{14}	7	7	0.8
1.0		3.6×10^{13}	2.0	-	0.54
1.4		1.3×10^{13}	2.4	1.8	0.52
0.7	5	1.9×10^{15}	2.5	0.1	0.85
1.0		4×10^{14}	1.7	0.1	0.63
1.4		2×10^{14}	0.63	0.1	0.49
0.7	20	4×10^{15}	0.1	0.1	0.62
1.0		1×10^{16}	0.1	0.1	0.56
1.4		2.7×10^{16}	0.1	0.1	0.55

Another striking observation is the difference between 1PE and 2 PE measurements. The difference in the lifetimes observed for 1PE and 2PE could have arisen due to the difference in the wavelength of light used for the two methods. Single photon excitation TRPL (1PE) uses 700 nm light as the excitation source from the glass side. The absorption coefficient for CdTe at 700 nm wavelength light is 3.5×10^{4} cm^{-1}. Using the Beer-Lambert Law, 90% of the excitation photon are absorbed in the first 0.65 µm depth into the CdTe. Considering the doping concentration of CdTe, this falls within the width of the depletion region. Therefore, the TRPL signal is obtained from areas in proximity to the CdTe/CdS junction. The 2PE measurement on the other hand uses light source with a wavelength of 1200 nm. This method employs the usage of microscopes and optics to focus the light at the interior of the films and away from the influence of the CdTe/CdS junction and the back contact. The difference between 1PE and 2 PE is significant for Cu doped cells. Cu is known to reduce carrier lifetimes by forming recombination states and in this study, Cu is deposited near the back junction. It is possible that the 2PE TRPL measure the local carrier lifetimes near the back junction where the Cu concentration could be higher. In order to get reliable information from 2PE measurements, the thickness of CdTe has to be greater so that the excitation source can be focused away from the CdTe/CdS junction and the back contact.

A third observation that could be made is the decrease in carrier lifetime with Cu incorporation. Though incorporation of Cu improved doping concentration and back contact properties, the minority carrier lifetime decreased for all Cu concentrations. It has been recently reported that Cu_{Cd}, the main substitutional defect formed by Cu incorporation acts as recombination center reducing minority carrier lifetime [138]. This also implies that for the 5Å Cu dose, though the doping increased, the increase in V_{OC} could have been more if not for the reduction in lifetimes.

6.8.4 Summary of Key Findings on the Effect of Cd/Te Ratio and Cu on Lifetimes

- Carrier lifetimes for as-deposited films (without $CdCl_2$ HT) was very low and could not be measured
- Films with Cd/Te ratio 0.7 (Te-rich) showed the highest carrier lifetimes up to 7 ns and the lifetimes decreased at higher Cd/Te ratio 1.4 (1.7 ns).
- Cu improved carrier concentrations but decreased carrier lifetimes for all cd/Te ratios.

6.9 Alternate Strategies to Improve V_{OC}

6.9.1 Saturation Limit for Te-rich Growth Conditions

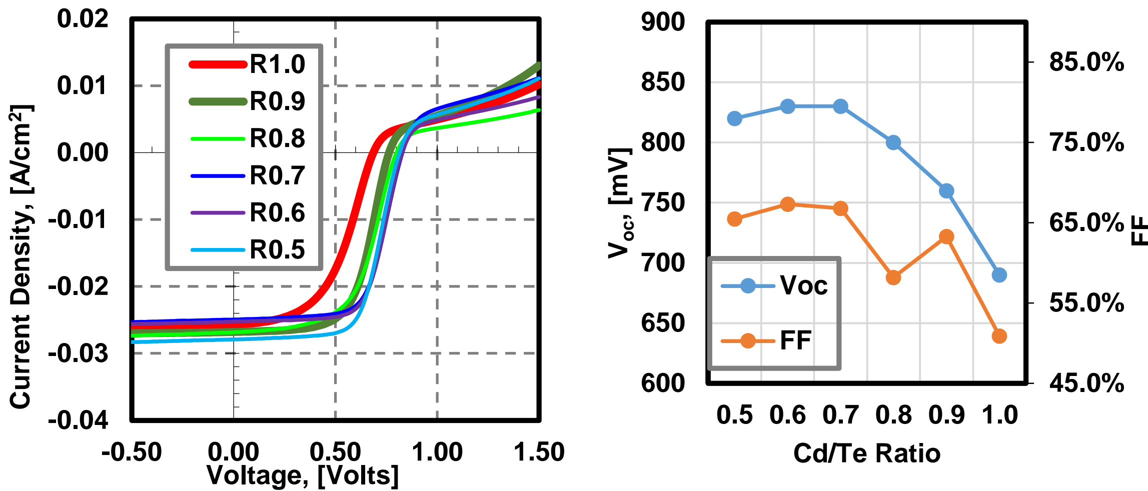

Figure 49: JV curves (left) and V_{OC}, FF for extreme Te-rich conditions

The formation energies calculated using the HSE approach predicted that films deposited under Te-rich conditions, after Cl treatment are prone to Fermi-level pinning at around mid-gap. In this study, solar cells with Te-rich CdTe showed better doping levels, carrier lifetimes and V_{OC}'s. The best V_{OC} was obtained for a Cd/Te ratio 0.7. To establish a saturation limit for V_{OC} under Te-rich conditions solar cells were fabricated with Cd/Te ratios below 0.7. The intent was to deposit CdTe using the lowest Cd/Te ratio possible. MoN/Mo was used as the back contact. At Cd/Te ratios 0.3, the CdTe films were less adherent to CdS and resulted in flaking. Cd/Te ratios below 0.3 often resulted in pinholes and therefore no cells were processed. Figure 49 shows the JV characteristics (left) and the V_{OC}, FF for Cd/Te ratios 1.0-0.3. The V_{OC} saturated at 830 mV for Cd/Te ratios less than 0.7. The roll-over is due to MoN/Mo non-ohmic back contact. The carrier concentration for the Te-rich samples (Cd/Te ratio <1) was higher than the stoichiometric film (Cd/Te ratio 1.0). As predicted by the theoretical calculations, the V_{OC} saturated (at 830 mV) indicating the saturation limit for Cl doped CdTe films deposited in Te-rich conditions.

6.9.2 Annealing CdTe in Cd and Te Ambient

The solubility of cadmium and tellurium vacancies can be increased with temperature [139]. Annealing CdTe films in Cd and Te over pressures can increase the concentration of V_{Cd} and V_{Te} defects,

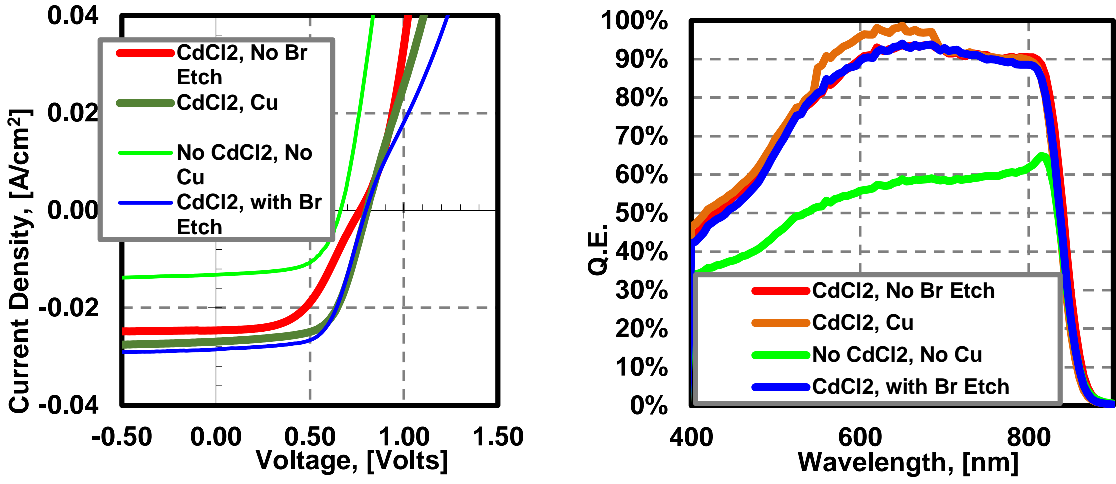

Figure 50: JV and SR for CSS-CdTe films annealed in Te over pressure

paving the way for extrinsic doping with Group I and Group V elements [140]. Typically, as-deposited CdTe is p-type due to a Te-rich defect stoichiometry [77]. Annealing in a Cd overpressure can make as-deposited CdTe n-type by causing a change in the defect chemistry [141]. To study the effect of annealing in Cd and Te ambient, CdTe films deposited by the CSS method were annealed in Cd and Te overpressures. CdTe films were deposited on 'CdS/TCO/Glass' substrates using the Closed-spaced Sublimation (CSS) process. The films were then annealed at 550° C in Te or Cd over pressures for 20 minutes in the EVT chamber. Cu free graphite paste was used as the back contact. For annealing in Cd, the Cd elemental flow was kept on and the flow through Te was shut off and vice versa.

Figure 50 shows the JV and Q.E characteristics for a cell annealed in Te over pressure. The sample was cut into four quarters and solar cells were fabricated without $CdCl_2$ HT, with $CdCl_2$ and no Br etch, with $CdCl_2$ HT and Br etch and $CdCl_2$ HT with Br etch and Cu. Br etch is used prior to back contact formation and helps to create a Te rich layer aiding in the formation of an Ohmic contact. The Q.E. for the sample with no $CdCl_2$ showed reduced collection indicating a weak CdTe/CdS junction which is typical for as-deposited cells. Such behavior was observed earlier for EVT-CdTe films deposited under Cd-rich conditions. $CdCl_2$ HT improved the performance in all aspects, i.e. V_{OC}, J_{SC}, FF and η. Br etch improved the V_{OC} slightly. The addition of Cu did not improve the performance significantly, barring the marginal improvement in FF. The increased collection for the Cu sample between 500 and 700 nm may be a result

of an erroneous measurement and therefore the resultant increase in J_{SC} should be neglected. The highest V_{OC} was 800mV and the FF was 63% for the Cu doped sample.

Figure 51 shows the results for the film annealed in Cd over pressure. The film with no $CdCl_2$ HT shows almost zero collection. The slight bump in collection at around 850 nm corresponds to the absorption

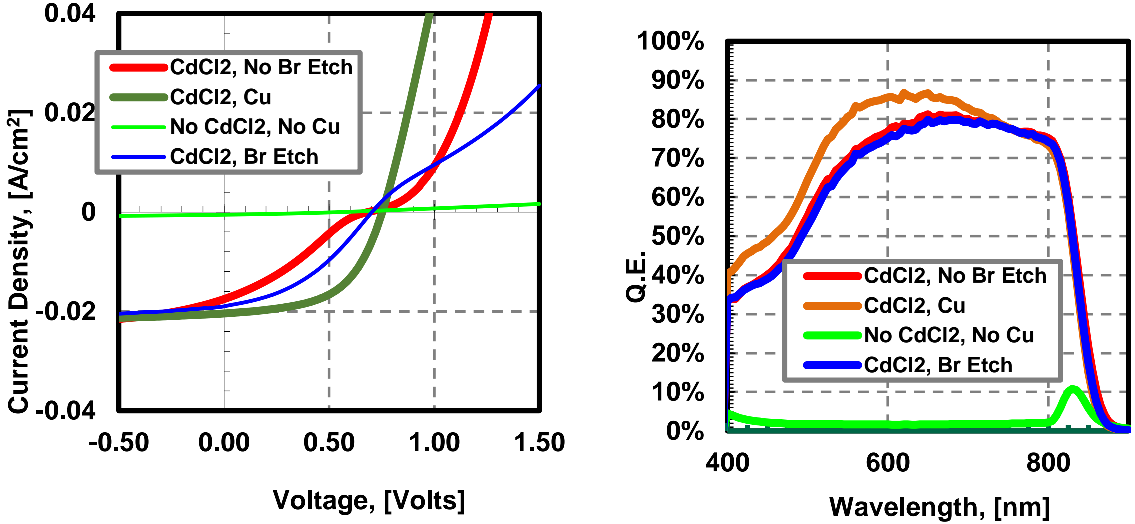

Figure 51: JV and SR for CSS-CdTe films annealed in Cd over pressure

edge of CdTe. The $CdCl_2$ HT however, increased the performance tremendously. Bromine etch improved the V_{OC} and FF like in the case of the film annealed in Te overpressure. Cu improved V_{OC} and FF. The improvement in current however, again may not be real and could be a measurement artifact. As-deposited CSS-CdTe is p-type; the Q.E. curve for the Cd-annealed sample reveals that the CdTe film may be intrinsic or n-type and resembles a Cd-rich film without $CdCl_2$. This study revealed that annealing in Cd and Te overpressures can change the defect chemistry of CdTe. Further research is needed to quantify the change in defect chemistry.

6.9.3 Absorber Grading

To bypass the problem of poor carrier lifetimes and improve V_{OC}, Jim Sites and Jun Pan [46] proposed a strategy to fully deplete the CdTe layer so that the internal field would assist the collection of photo generated carriers. A fully depleted device can be achieved by employing a n(CdS)-i(CdTe)-p(back contact) structure. However, such a device also needs an electron reflector barrier to prevent electrons reaching the back electrode.

Figure 52 shows JV curves from SCAPS simulation for three CdTe/CdS devices. The first device is a typical CdTe/CdS structure where the carrier concentration of CdTe is 10^{14} cm^{-3}. The second device

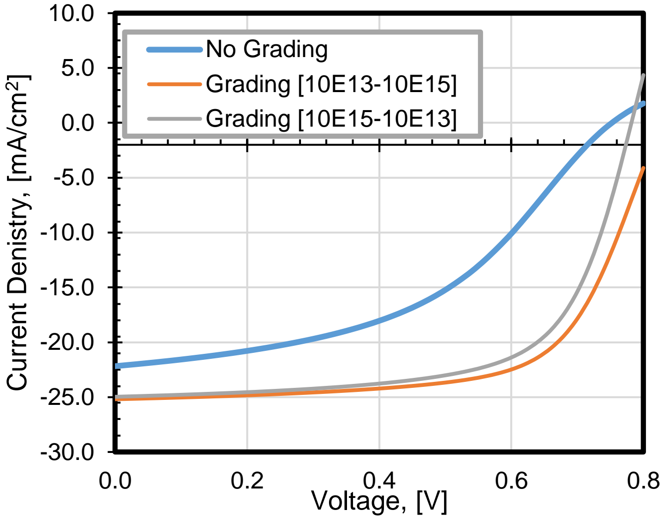

Figure 52: Simulated JV curve for graded CdTe devices

has a graded absorber where the carrier density decreases uniformly from 10^{15} cm^{-3} near the CdTe-CdS junction to 10^{13} cm^{-3} near the back contact. The third and final device also has a graded CdTe layer except the carrier density is 10^{13} cm^{-3} at the junction and 10^{15} cm^{-3} near the back contact. This device is somewhat similar to the n-i-p structure proposed by Jim Sites et al. The V_{OC} for the third device is higher than the first and second. The low carrier density at the interface widens the depletion region and therefore circumvents most of the recombination taking place in the bulk.

To achieve absorber grading, CdTe was deposited with different Cd/Te ratios on the same substrate. Two such films were deposited where the sequence of the Cd/Te ratio was changed: a) 0.7-1.0-1.4, b) 1.4-1.0-0.7. The first device (a) was expected to have higher doping near the junction (as it is Te-rich) and the second (b) was expected to have higher doping near the junction (as it is Cd-rich). Since the growth rate depends on Cd/Te ratio, the deposition for each layer (Cd/Te ratio) was timed such that the thickness was 2µm. 2Å Cu was sputtered on select films before graphite back contact. Figure 53 shows the JV and SR for CdTe films with graded absorbers. The cell with Cd/Te ratio 1.4 near the junction performed better in all aspects. The carrier concentration vs. absorber depth is shown in Figure 54. The film with Cd/Te ratio 1.4 near the junction showed increased doping. However, no significant change in depletion width was

observed. The doping clearly increased with Cu and the depletion width decreased which corroborates the increased doping levels.

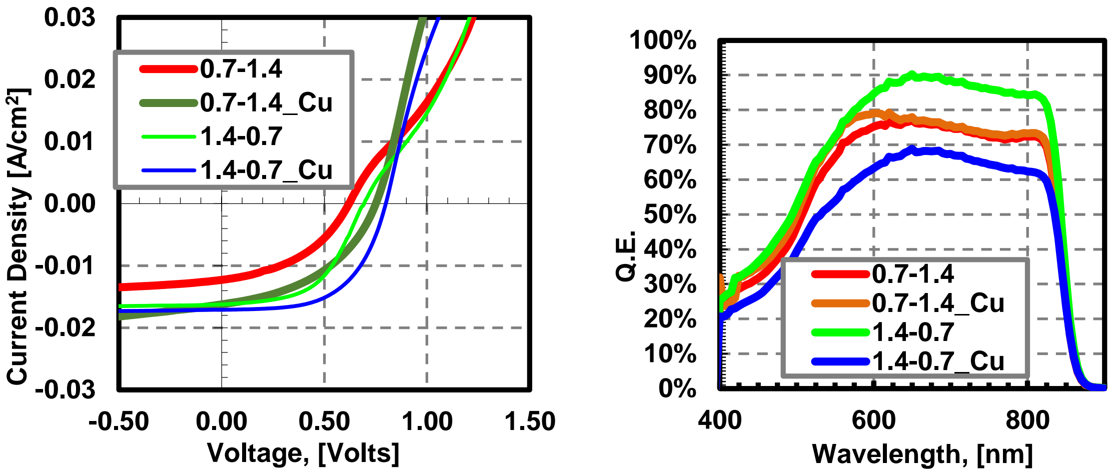

Figure 53: JV and SR for EVT-CdTe films with absorber grading

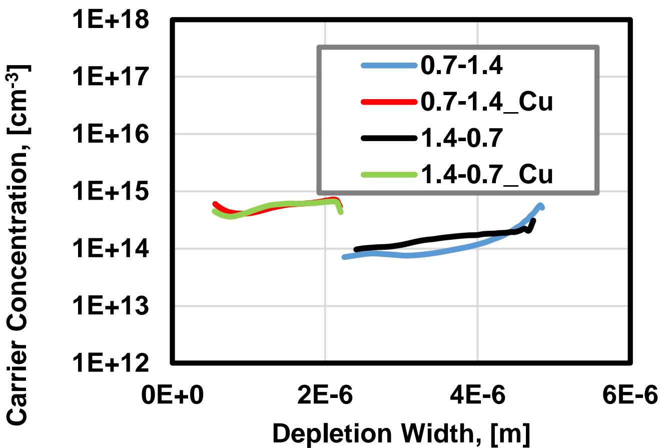

Figure 54: Doping profile for EVT-CdTe with graded absorbers

The expected outcome of the experiment was that the cell with Cd/Te ratio 1.4-1.0-0.7 would perform better due to increased depletion width and therefore reduced recombination. Though the results were in agreement with the hypothesis, the C-V measurements did not show any evidence of increased depletion width. The improved performance could be due to the properties of the Te-rich layer (Cd/Te ratio 0.7) rather

than the graded absorber. Further investigation is needed to fully understand the absorber grading in EVT films.

6.9.4 Summary of Key Findings from Alternate Strategies to Improve V_{OC}

- The V_{OC} saturates for Cd/Te ratios below 0.7 at 830 mV.
- Annealing in Cd and Te over pressures can influence the defect chemistry of CdTe Cd annealing caused poor performance possibly due to formation of compensating defects (Cd_i).
- Simulation studies show that lower doping near the CdTe/CdS junction helps to improve V_{OC}. Absorber grading showed expected results but CV measurements do not show the expected trend in doping.

6.10 Effects of Substrate Temperature

6.10.1 Introduction

According to the CdTe phase diagram, CdTe deposited at high temperature tends to be Te-rich [77]. To study the influence of growth temperature on stoichiometry, the substrate temperature was increased to 630° C (About 50° C higher than the standard deposition temperature of 580° C) to deposit CdTe films with different Cd/Te ratios. Films deposited at higher temperature showed pinholes, therefore the deposition was carried out in two steps. For the first 3 minutes, the temperature was at 580° C, which was followed by the high temperature deposition at 630° C.

6.10.2 Observations and Results

Figure 55 shows the Q.E curves for cells with Cd/Te ratios 0.3, 0.4, 0.5, 0.6, 0.7, 0.8 and 1.0. Copper free graphite paste was used as the back contact. A sight increase in carrier collection with decrease in Cd/Te ratio was observed in the blue region (between 400 and 500 nm). Increased collection in the blue region was also accompanied by a shift in absorption edge of CdTe (above 830 nm). Since the absorption in the blue region is mainly due to CdS layer, an increase in collection implies thinning of CdS layer [142]. However, all the films received the same amount of CdS. This suggests that the thickness of CdS decreases with increase in Te vapor (or at low Cd/Te ratios). Films deposited with Cd/Te ratios < 0.5 were found to be visibly different from the glass side when compared to films deposited at ratios 1.0 and above.

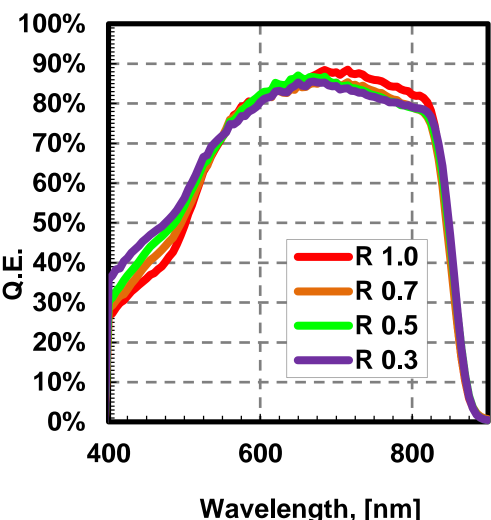

Figure 55: Q.E. curve for Te-rich CdTe films deposited at high temperatures showing CdS thinning

It is known that $CdCl_2$ HT promotes S diffusion from CdS to CdTe and results in the formation of $CdTe_{(1-x)}S_x$ alloy leading to thinning of CdS [143]. Due to increased Te content in Te-rich films, it is possible that the thickness of $CdTe_{(1-x)}S_x$ increases causing CdS thinning. Formation of $CdTe_{(1-x)}S_x$ alloy leads to a reduction in the bandgap of CdTe which results in shifting the absorption edge of CdTe [143]. Higher T_{Sub} causes increased CdTe/CdS intermixing [144]. An earlier study reported that cells with Te-rich CdTe perform better as a result of reduced interface recombination. The improvement in the junction properties was attributed to increased CdTe/CdS intermixing for films grown in Te- rich conditions [145]. A recent study on the electronic properties of defects in $CdTe_{(1-x)}S_x$ showed that that the transition levels of V_{Cd} and Te_{Cd} become close to the valence band when these defects have more S in their local environment [146]. Te_{Cd} is considered as the main lifetime limiting defect and V_{Cd} is considered to be the main intrinsic acceptor defect responsible for p-doping in CdTe. When V_{Cd} becomes closer to the valence band, it improves the p-doping. Te_{Cd} cannot be an effective recombination center if it moves away from mid-gap and therefore improves lifetimes. Though the effect of intermixing was evident only for films deposited at higher substrate temperatures, it is possible that Te-rich films have relatively higher intermixing than films deposited under stoichiometric and Cd-rich conditions at lower substrate temperatures too. Therefore the improvement in V_{OC}'s for Te-rich films could also be due increase in intermixing of CdTe and CdS. Further investigation is needed to confirm this hypothesis.

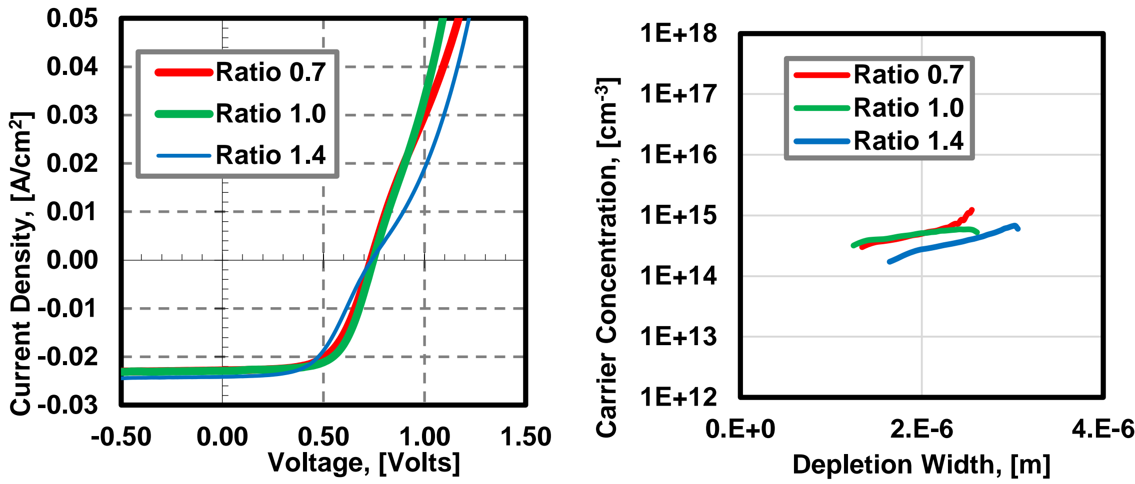

Figure 56: JV curves and doping profiles for EVT-CdTe films deposited at high temperatures

Figure 56 (left) shows the JV characteristics for cells with Cd/Te ratios 0.7, 1.0 and 1.4 deposited at high substrate temperatures. The cell with Cd/Te ratio 1.4 showed lower V_{OC}'s. The carrier concentration vs depletion width profile is shown in Figure 56 (right). As was the case with V_{OC}'s the 1.4 ratio sample showed slightly lower doping. However, the difference in the V_{OC} and carrier concentrations for different Cd/Te ratios is not as prominent, compared to the films deposited at a substrate temperature of 580° C. Since growth in high temperatures makes CdTe films Te-rich, the films deposited at ratio 1.0 and 1.4 could be shifted towards the Te-rich side of stoichiometry causing them to have carrier concentrations and V_{OC}'s similar to Te-rich samples.

The recombination rates for these cells were measured at NREL by the 1PE TRPL. The measured carrier lifetimes are shown in the Figure 57. The Te-rich samples showed higher lifetimes than the Cd-rich samples but lower than the Cd/Te ratio 0.7 ratio deposited at standard temperature (580° C). The reason for the decrease in carrier lifetimes for the high substrate temperature samples is not understood at this point. An interesting observation is the increase in carrier lifetime with Cu which was not observed for the cells discussed earlier. The amount of Cu used in this experiment was only 2Å (lower than any of the Cu cells discussed earlier). Cu occupies V_{Cd}'s to form shallower defects Cu_{Cd}'s. The decrease in concentration of deeper defects which could potentially act as recombination centers could be the reason for increase in carrier lifetimes. Therefore optimum amount of Cu could improve doping and carrier lifetimes too. It is anticipated that further increase in Cu concentration would result in decrease in carrier lifetimes as Cu_{Cd}'s

can also act as recombination centers. However, Cu_{Cd}'s being shallower defects than V_{Cd}'s, their influence on the carrier lifetimes could be minor.

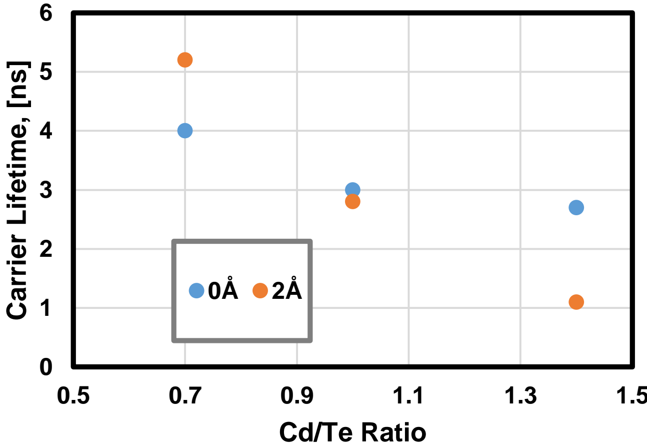

Figure 57: Carrier lifetimes for EVT-CdTe films deposited at high temperatures with and without Cu

6.10.3 Summary of Key Findings from Increased Substrate Temperature

- Increased substrate temperature caused CdS and CdTe intermixing. The amount of intermixing was more for the Te-rich samples.
- An optimum amount of Cu can improve carrier lifetimes and doping.

6.11 Deep Level Transient Spectroscopy

6.11.1 Introduction

Deep Level Transient Spectroscopy (DLTS) is a powerful tool for the identification of deep levels in Schottky barriers and p-n junctions. Carrier emissions from a pulse can cause several capacitance transients to occur. By analyzing those capacitance transients as a function of temperature, the energy levels of deep states within the bandgap along with their concentration and capture cross-section can be estimated. However, the CdTe/CdS hetero-structure is not ideal for DLTS measurements. One of the necessary conditions for a reliable DLTS measurement is the presence of an ohmic contact which is a challenge in CdTe devices.

Plain graphite was used as the back contact for all devices used for DLTS measurements. The DLTS is extremely sensitive to any capacitance changes and a non-ohmic back contact can lead to erroneous results. Discharge processes that take place from parasitic capacitances such as the back

contact capacitance in addition to the transient process corresponding to the thermal emission from trap states can lead to signal distortion and erroneous results [147]. Such parasitic capacitances can arise from a non-ohmic back contact. DLTS measurements above 300K have shown to be detrimental and lead to loss of DLTS signal for subsequent measurements. Therefore the analysis was conducted in the temperature range of 80K- 300K.

6.11.2 Observations and Results

6.11.2.1 DLTS on CSS CdTe Films

In order to establish a baseline DLTS for CSS samples of various conditions was carried out first. Figure 58 shows current-voltage (JV) characteristics and carrier concentration profiles for CSS) CdTe devices fabricated with different amounts of Cu in the back contact. An untreated device (no $CdCl_2$) is also included as a reference, and as expected it exhibits poor diode behavior. The $CdCl_2$ HT improves the open-circuit voltage (V_{OC}), fill factor (FF) and short-circuit current (J_{SC}). Capacitance-Voltage (CV) measurements indicate that the $CdCl_2$ treatment doesn't affect the doping concentration (it improves the lifetime of the absorber [4]). 2Å of Cu further improves the cell performance and results in an increase in doping concentration from 1×10^{13} to 1×10^{14} cm^{-3}. Further increase in Cu to 10 Å degraded the V_{OC} and FF, despite

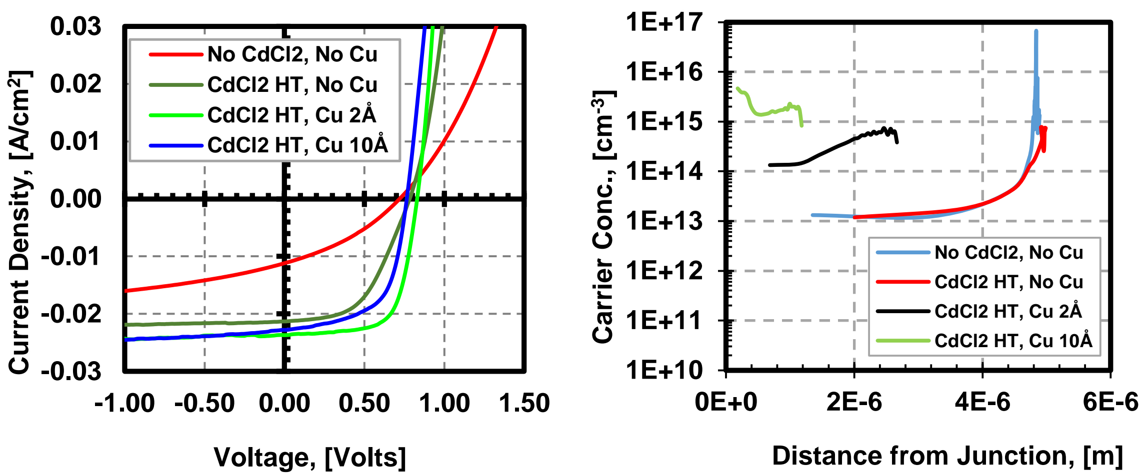

Figure 58: Current-voltage measurements (left) and doping profile from (right) for CdTe devices with different $CdCl_2$ treatment and Cu doping.

an increase in doping concentration to 10^{15} cm^{-3}. As the net doping increases the depletion region decreases, causing a reduction in photo-generated carrier collection due to recombination. TRPL

measurements shown in previous chapters established that Cu is detrimental to carrier lifetime. Therefore, unless the carrier lifetime is simultaneously improved along with doping, excess Cu reduces V_{OC} and FF [2].

Figure 59 (left) shows the DLTS analysis of the sample without $CdCl_2$ HT. A minority carrier peak of low intensity is observed in the temperature range of 170- 220 K. Since the C is positive, it represents an electron trap. The activation energy of this minority peak was calculated to be 0.38 eV below the CBM with a concentration of 10^8cm^{-3}. Above 280K, the onset of a deep majority peak was also observed. Such

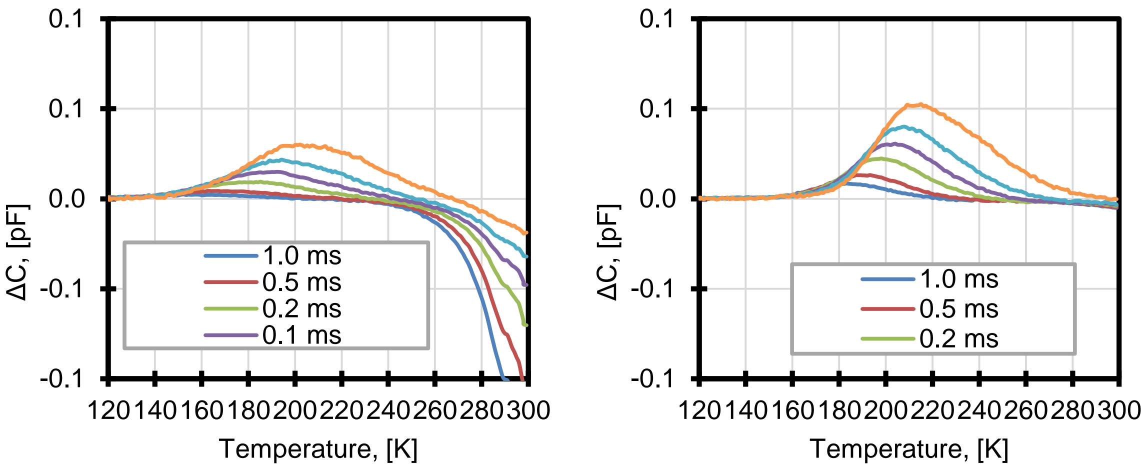

Figure 59: DLTS spectra of a CdS/CdTe without $CdCl_2$ (left) and with $CdCl_2$ (right)

deep majority peaks could be the mid-gap defects like Te_{Cd} or Te_i which limit carrier lifetimes in CdTe. Figure 59 (right) shows DLTS spectra of the sample with $CdCl_2$HT. The deep majority peak observed for the sample with no $CdCl_2$ was not observed suggesting the reduction in the concentration of mid-gap defect levels. The intensity of the shallow minority peak increased with an activation of energy of 0.48 eV below CBM along with a trap concentration of 10^{12}cm^{-3}.

Figure 60 (left) shows the DLTS spectra for the sample with $CdCl_2$ HT and 2Å Cu. The intensity of the minority carrier peak further improved by almost an order of magnitude. The activation energy was 0.26 eV below CBM with a concentration of 10^{14} cm^{-3} (shown in the inset). This defect being shallower than the minority defect observed in the previous two cases could be related to Cu. At temperatures above 200 K, the C becomes negative suggesting the presence of a deep majority trap. This also implies that the carrier lifetime for the samples with Cu could be low. The DLTS spectra for excess Cu concentration of 10Å is

shown in Figure 60 (right). The spectrum is different from what was observed in the previous cases. Multiple majority and minority peaks very close to each other or overlapping were observed. The activation energies for over lapping peaks do not yield reliable results and hence were not calculated. The negative peak at

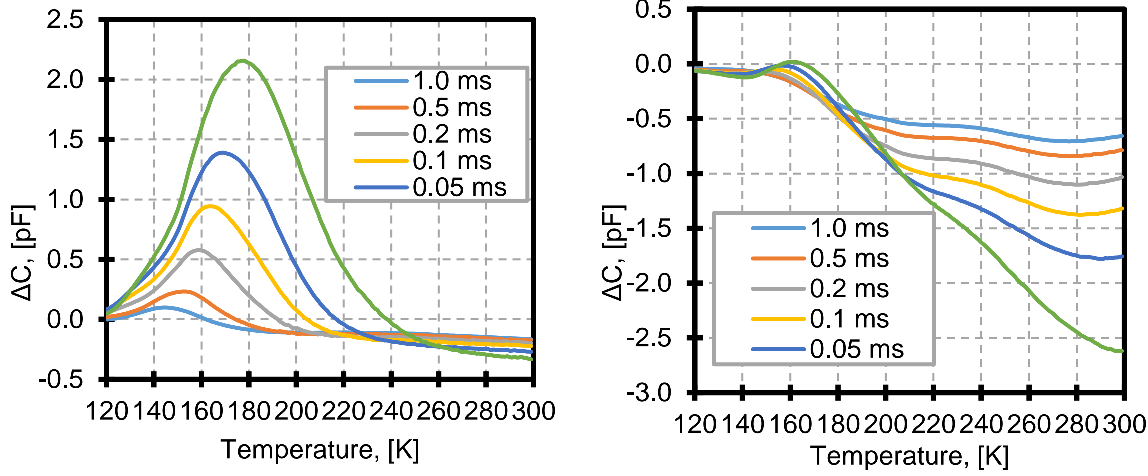

Figure 60: DLTS spectra for CdS/CdTe with $CdCl_2$ HT and 2Å Cu (left) and with $CdCl_2$ HT and 10 Å Cu (right)

140K represents a shallow majority trap with a low concentration and activation energy. This could be the substitutional defect Cu_{Cd}, responsible for p-doping in CdTe. The broad negative peak which begins at 260 K had a shoulder at 200K implying two majority traps. These deep defects are believed to be related to Cu which are detrimental for carrier lifetimes. The summary of the activation energies and trap concentrations is shown in Table 11.

Table 11: CSS CdTe device parameters with different $CdCl_2$ HT and Cu

Cell Structure	V_{OC} [mV]	FF [%]	Carrier Conc. [cm^{-3}]	Minority carrier trap	
				Activation energy (eV)	Conc. [cm^{-3}]
No $CdCl_2$, No Cu	720	35	1×10^{13}	0.38	4×10^{8}
$CdCl_2$ HT, No Cu	780	51	1×10^{13}	0.48	4×10^{12}
$CdCl_2$ HT, Cu 2Å	830	67	1×10^{14}	0.26	1×10^{14}
$CdCl_2$ HT, Cu 10Å	780	62	1×10^{15}	-	8×10^{12}

6.11.2.2 DLTS on EVT-CdTe Films

DLTS measurements were conducted on EVT-CdTe films with Cd/Te ratios: 1.6, 1.0, 0.9, and 0.8. The cell results are shown in Table 12. Cd/Te ratio was changed by using flowrate as the control variables because of which the change in performance with ratio is not significant. Within the range of the Cd/Te ratios experimented, better cell performance is observed for lower ratios with improvements in the FF for samples without Cu. V_{Cd} is considered to be the main acceptor defect in CdTe, which has lower formation energy under Te-rich deposition conditions. Cu doping improves cell performance, except for Cd-rich vapor deposition conditions. Cu can form substitutional acceptor defects Cu_{Cd}, and is favorable under Te-rich deposition conditions and has a lower ionization energy compared to V_{Cd}. However under Cd-rich conditions lower concentration of V_{Cd} and higher concentration of Cd_i is expected. This makes the formation energy of Cu_{Cd} higher, causing the Cu to move to interstitial sites as Cu_i. These compensating defects such as Cd_i and Cu_i are assumed to be responsible for the poor performance on Cd-rich deposited films with Cu.

Table 12: EVT-CdTe device performance with different Cu

Cd/Te Ratio	No Cu			Cu 2Å		
	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)
1.6	790	47.3	20.1	600	50.5	20.59
1.0	780	63.0	23.12	810	62.4	22.00
0.9	790	56.0	22.34	810	60.7	21.93
0.8	790	66.4	23.34	810	57.4	22.25

Figure 61 shows the DLTS spectra obtained from EVT CdTe samples with $CdCl_2$ HT (No Cu). Drawing a parallel to the CSS deposited samples with similar post deposition treatment, it is possible that EVT-CdTe films have better electrical properties compared to CSS-CdTe samples; for CSS-cells with 'no Cu' very weak DLTS signal was observed. On all EVT samples, minority carrier peaks are observed around 200-250 K. The Cd-rich deposited film shows a different characteristic, the minority peak appears to be composed of 2 peaks - the dominant one at 250 K with a shoulder at 210 K. A shallow majority carrier peak is observed for all samples except the stoichiometric deposition. In CSS-CdTe films, a shallow majority

peak has been observed on Cu doped samples only (DLTS spectra is shown in Figure 60). This indicates that the shallow peak could be the acceptor defect responsible for better device performance. However, the absence of this shallow peak for stoichiometric film cannot be explained and further investigation is needed to ascertain the cause.

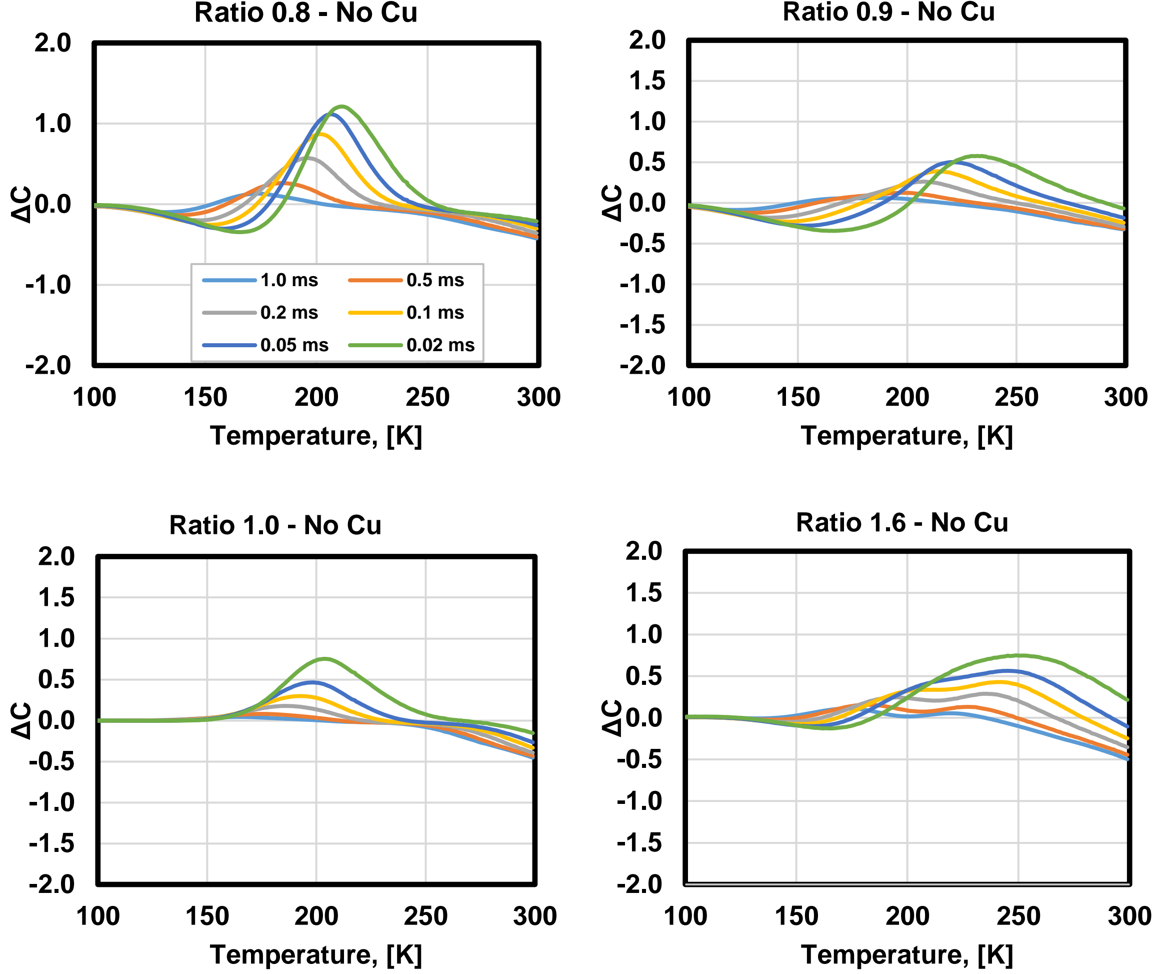

Figure 61: DLTS for EVT-CdTe with different ratios $CdCl_2$ HT and no Cu

Also noticeable is that in all samples ΔC continues to increase in the negative direction at higher temperatures. This suggests the presence of deep majority carrier defects. Figure 62 shows the DLTS spectra obtained from EVT CdTe samples with $CdCl_2$ HT and 2Å Cu. The spectra is qualitatively similar to 'no Cu' samples, with respect to the presence of shallow majority and deeper minority carrier defects. The Cd-rich deposited device could not be measured in this case, possibly due to poor diode quality. Ratio 1.0 with 2Å Cu also stands out due to its high intensity negative ΔC near room temperature. This could be

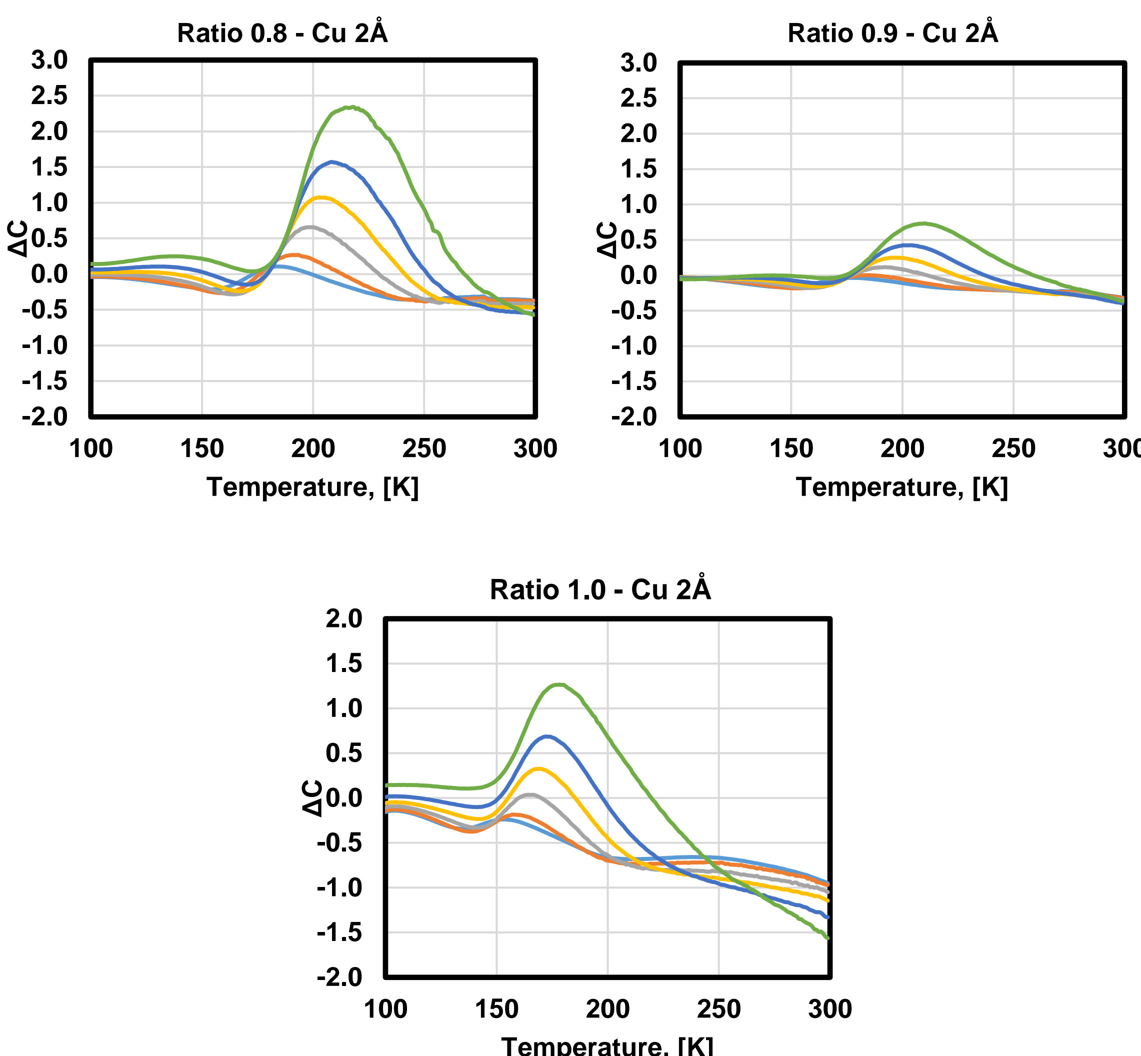

Figure 62: DLTS for EVT-CdTe with different ratios with $CdCl_2$ HT and 2Å Cu.

indicating Cu related deep defects. Due to the complex nature of these peaks, the activation energy and trap concentration cannot be calculated in some cases.

Table 13 shows the calculated defect parameters for these samples. An important observation is that the electron trap is correlated to dopant concentration calculated from CV measurements. This suggests that although this is a minority carrier trap, its formation could be indirectly linked to the formation of majority carrier acceptor defects.

6.11.3 Summary of Key Findings from DLTS Experiments

Though there are minor changes in the DLTS spectra, there was no significant changes in the activation energies of the defects levels for different Cd/Te ratios. A shallow acceptor defect observed for Cd/Te ratios 0.8 and 0.9. The defect kevels identified can be related to Te_{Cd} or Cd_i. Though noticeable trends were observed in the DLTS spectra with respect to change in Cd/Te ratio, it is difficult to draw a correlation to device performance at this point. The summary of the defect transition energies is shown in Table 13. Further investigation is needed to fully understand the defect activation energies at higher temperatures.

Table 13: EVT-CdTe device parameters with different Cd/Te ratio and different Cu

Cd/Te Ratio	**Cu**	**Doping Conc. (cm^{-3})**	**Hole Trap**		**Electron Trap**	
			E_A (eV)	**N_T (cm^{-3})**	**E (eV)**	**N_T(cm^{-3})**
1.6	X	2.0E14			0.43	1E13
1.0		5.8E14			0.41	3.2E13
0.9		2.2e14	0.13	1.0E13	0.35	1.7E13
0.8		1.4E14	0.21	4.2E12	0.48	1.5E13
1.6		5.5E14			n/a	n/a
1.0	Å	6.4E14			0.42	5.8E13
0.9		5.7E14			0.40	2.4E13
0.8		6.4E14			0.43	7.4E13

Chapter 7: Conclusions and Future Work

7.1 Conclusions

A systematic study of a process capable of creating favorable conditions for achieving higher doping and carrier lifetimes in CdTe thin films was conducted. Both doping and lifetimes can be influenced by the CdTe stoichiometry which was altered by changing the vapor phase Cd/Te ratio. CdTe films were deposited under Cd-rich (Cd/Te > 1.0), Te-rich (Cd/Te < 1.0) and stoichiometric (Cd/Te =1.0) growth conditions. The structural and electrical properties of CdTe and the performance of CdTe/CdS solar cells as a function of Cd/Te ratio was studied. The role of Cl and Cu treatments on cells made with different Cd/Te ratios was also investigated. The conclusions are summarized below.

XRD studies revealed that CdTe films deposited under Te-rich growth conditions showed the highest degree of preferential orientation. SEM images revealed that the grain sizes depend on Cd/Te ratio. The grain sizes decreased with increase in Te content in the CdTe film. The growth rate showed a strong correlation to gas phase Cd/Te ratio. Films deposited under Te-rich growth conditions showed higher deposition rates. The Te-rich films also showed lesser adhesion to CdS layer with increase in Te content. Films deposited with Cd/Te ratios below 0.5 exhibited flaking and pinholes. The adhesion was improved by following a 2-layered deposition approach and by reducing the ratio window.

Solar Cells fabricated with as deposited EVT-CdTe films without the traditional $CdCl_2$ HT required for high efficiency devices indicated very poor performance for the films deposited under Cd-rich conditions. The shape of the Q.E. curve indicated a very weak CdTe/CdS junction. This is indicative of the Cd-rich CdTe film being intrinsic or possibly n-type. $CdCl_2$ HT improved performance for cells with all Cd/Te ratios, and to a better extent for the cells made with CdTe films deposited under Te-rich conditions.

Capacitance Voltage measurements revealed higher carrier concentrations for the cells with Te-rich CdTe (Cd/Te < 1.0). Cl treatment is known to introduce donor defects Cl_{Te} which combine with V_{Cd}'s to

form shallow acceptor defects called the A-centers. Since the Te-rich films are expected to have a higher concentration of V_{Cd}'s the increase in doping can be attributed to the increase in A-center concentration.

TRPL measurements were conducted to measure carrier lifetimes. Solar cells fabricated using CdTe with Cd/Te ratio 0.7 and $CdCl_2$ HT showed the highest carrier lifetimes of 7 ns. Cl is treatment is known to passivate grain boundary related defects. A previous study indicated that Cl passivates Te-core boundary defects better than Cd-core defects. Therefore, the improved carrier lifetimes for the Te-rich samples could be due to the preferential passivation of GB by the Cl treatment.

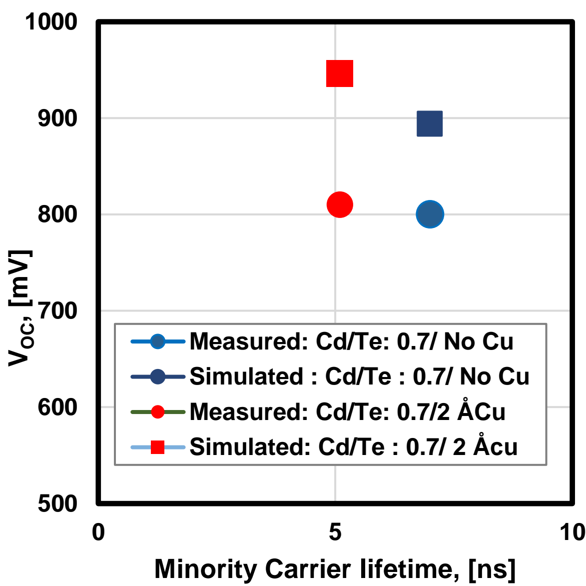

Figure 63: Simulated and measured values for the highest carrier concentrations and lifetimes measured in this study

The highest V_{OC} observed was 830 mV for a cell with Cd/Te ratio 0.7. Since the 0.7 ratio films showed better carrier concentrations and lifetimes, the increased V_{OC} can be attributed to better doping and carrier lifetimes of the films grown under Te-rich conditions. However, the V_{OC}'s exhibited a saturation limit. In this study, the V_{OC} did not increase for cells made with Cd/Te ratios below 0.7. This observation agrees with the theoretical studies that Cl treatment under Te-rich conditions pins the Fermi level to around mid-gap.

A 5Å dose Cu improved doping for all Cd/Te ratios. Cu occupies V_{Cd}'s to form Cu_{Cd}'s and the concentration of V_{Cd}'s is expected to be higher in films deposited under Te-rich conditions. However, the same amount of Cu decreased carrier lifetimes for all ratios. For the 0.7 ratio sample the lifetime decreased from 7ns to 2.5 ns with 5Å Cu. However, the V_{OC} increased owing to the increase in doping. 'Excess' Cu (20 Å) deteriorated overall cell performance for all ratios by reducing the lifetimes drastically. This observation agrees well with most theoretical and experimental studies conducted so far. However, Cu improved doping and the carrier lifetimes when the Cu concentration was 'optimum' (2Å). Since V_{Cd}'s are deeper than Cu_{Cd}'s, an optimum amount of Cu can improve lifetimes by reducing the concentration of V_{Cd}'s.

Figure 63 shows the simulated and measured values of the highest V_{OC}'s and corresponding lifetimes. The calculations have been performed using the carrier concentrations of the respective cells. The values correspond to the CdTe film with Cd/Te ratio 0.7 without Cu and a film with Cd/Te ratio 0.7 and 2Å Cu. In comparison to the simulation data, the measured V_{OC}'s are significantly lower. CdTe/CdS interface recombination velocity is an important parameter in defining the V_{OC} [42], which is not incorporated in the simulation model being used. The effect of Cd/Te ratio and Cu concentration on the interface recombination velocity is not well understood at this moment, and may have played a role in reducing the V_{OC} as compared to the simulated values.

7.2 Ongoing and Future Work

One of the benefits of $CdCl_2$ HT is intermixing of CdTe and CdS leading to reduced interface recombination. At high temperatures, the Q.E suggests that Te-rich samples undergo more intermixing than CdTe. The hypothesis is that the degree of intermixing is more for Te-rich films compared to Cd-rich films. This factor can also contribute towards the improved performance for the films deposited under Te-rich conditions. Therefore, future studies should investigate the intermixing of CdS and CdTe at lower Cd/Te ratios.

V_{OC}'s above the current threshold can be achieved with doping concentrations above 10^{16} cm^{-3} and lifetimes above 2ns. Though lifetimes above 2 ns were achieved in this study, the highest doping concentration achieved was in the order of 10^{15}. Depositing CdTe under Te rich conditions enabled to create favorable conditions to achieve such doping levels through Cl and Cu treatments. However, a saturation limit was observed beyond which these treatments fail to improve doping concentrations. Therefore, to

further increase doping above 10^{16} cm^{-3} range, extrinsic doping using Group V elements needs to be investigated. Research is ongoing to dope CdTe using Group V elements like P and As under Cd-rich conditions

References

[1] M.A. Green," Third generation photovoltaics: solar cells for 2020 and beyond, "Physics E: Low-dimensional Systems and Nanostructures, vol. 14, pp. 65-70, 2002

[2] http://energy.mit.edu/news/solar-photovoltaic-technologies

[3] Pvps, I. "Snapshot of global photovoltaic markets 2015." Report IEA-PVPS TI-29 (2016).

[4] http://www.nrel.gov/education/pdfs/educational_resources/high_school/solar_cell_history.pdf

[5] Green, Martin A., et al. "Solar cell efficiency tables (Version 45)." *Progress in photovoltaics: research and applications* 23.1 (2015): 1-9.

[6] Czochralski, Jan. "A new method for the measurement of the crystallization rate of metals." *Zeitschrift für physikalische Chemie* 92 (1918): 219-221.

[7] Teal, Gordon K., and J. B. Little. "Growth of germanium single crystals." *Physical review*. Vol. 78. No. 5. ONE PHYSICS ELLIPSE, COLLEGE PK, MD 20740-3844 USA: AMERICAN PHYSICAL SOC, 1950.

[8] Shruti Sharma, Kamlesh Kumari Jain, Ashutosh Sharma,"Solar cells: In Research and Applications", Material Sciences and Applications 2015,6,1145-1155

[9] Spinelli, Pierpaolo, et al. "Plasmonic light trapping in thin-film Si solar cells." Journal of Optics 14.2 (2012): 024002.

[10] Yablonovitch, Eli, and George D. Cody. "Intensity enhancement in textured optical sheets for solar cells." IEEE Transactions on Electron Devices 29.2 (1982): 300-305.

[11] Dicker, J., et al. "Analysis of one-sun monocrystalline rear-contacted silicon solar cells with efficiencies of 22.1%." *Journal of Applied Physics* 91.7 (2002): 4335-4343.

[12] Green, Martin A. "High efficiency silicon solar cells." *Seventh EC Photovoltaic Solar Energy Conference*. Springer Netherlands, 1987.

[13] Best Research-Cell Efficiencies (rev. 12-18-2014), National Renewable Energy Laboratory, 2014

[14] Yablonovitch, Eli, et al. "Extreme selectivity in the lift-off of epitaxial GaAs films." Applied Physics Letters 51.26 (1987): 2222-2224.

[15] Bett, A. W., et al. "III-V compounds for solar cell applications." Applied Physics A 69.2 (1999): 119-129.

[16] Jean, Joel, et al. "Pathways for solar photovoltaics." Energy & Environmental Science 8.4 (2015): 1200-1219.

[17] Handbook of Photovoltaic Science and Engineering, ed. A. Luque and S. Hegedus, 2nd edn, 2011

[18] A. V. Shah, H. Schade, M. Vanecek, J. Meier, E. Vallat- Sauvain, N. Wyrsch, U. Kroll, C. Droz and J. Bailat, Prog. Photovoltaics, 2004, 12, 113–142

[19] Wang, Nanlin. "Improving the stability of amorphous silicon solar cells by chemical annealing." (2006).

[20] Photovoltaics Report, Fraunhofer ISE, 2014.

[21] Grätzel, Michael. "Dye-sensitized solar cells." Journal of Photochemistry and Photobiology C: Photochemistry Reviews 4.2 (2003): 145-153.

[22] Shah, Arvind, et al. "Photovoltaic technology: the case for thin-film solar cells." *science* 285.5428 (1999): 692-698.

[23] M. A. Green, A. Ho-Baillie and H. J. Snaith, Nat. Photonics, 2014, 8, 506–514.

[24] H. J. Snaith, J. Phys. Chem. Lett., 2013, 4, 3623–3630

[25] Kaur, Manjot, and Harjit Singh. "A REVIEW: COMPARISON OF SILICON SOLAR CELLS AND THIN FILM SOLAR CELLS." International Journal Of Core Engineering & Management (IJCEM) Volume 3, Issue 2, May 2016

[26] Thin film Solar cells: Fabrication, Characterization and Applications edited by Jef Poortmans and Vladmiar Arhipov

[27] Chopra,K.L., Paulson, P.D. and Dutt, V. (2004) Thin-Film Solar Cells: An Overview. Progress in Photovoltaics, 12, 69-92

[28] Bonnet, Dieter, and Peter Meyers. "Cadmium-telluride—Material for thin film solar cells." Journal of Materials Research 13.10 (1998): 2740-2753.

[29] http://rredc.nrel.gov/solar/spectra/am1.5/

[30] Abdullah, Rasha A., Mohammed A. Razooqi, and Adwan NH Al-Ajili. "Characterization of the Energy Band Diagram of Fabricated SnO2/CdS/CdTe Solar Cells." *World Academy of Science, Engineering and Technology* 79 (2013): 118-122.

[31] J. Merten, J. M. Asensi, C. Voz, A. V. Shah, R. Platz, and J. Andreu, "Improved equivalent circuit and analytical model for amorphous silicon solar cells and modules," Institute of Electrical and Electronics Engineers Professional Technical Group on Electron Devices, vol. 45, pp. 423-429, 1998

[32] Best Research Cell efficiencies Chart maintained at NREL http://www.nrel.gov/ncpv/images/efficiency_chart.jpg NREL PV chart

[33] Jim Sites et al. "Progress and challenges with CdTe efficiency" PVSC IEEE conference

[34] J. Britt and C. Ferekides, "Thin-film CdS/CdTe solar cell with 15.8% efficiency," Appl. Phys. Lett., vol. 62, no. 22, pp. 2851–2852, 1993

[35] H.Ohyama,T.Aramoto,S.Kumazawa,H.Higuchi,T.Arita,S.Shibutani, T. Nishio, J. Nakajima, M. Tsuji, A. Hanafusa, T. Hibino, K. Omura, and M. Murozono, "16.0% efficient thin-film CdS/CdTe solar cells," in Proc. Conf. Rec. 26th IEEE Photovoltaic Spec. Conf., Anaheim, CA, USA, 1997

[36] M. A. Green, K. Emery, D. L. King, S. Igari, and W. Warta, "Solar cell efficiency tables (version 18)," Progr. Photovoltaics: Res. Appl., vol. 9, pp. 287–293, 2001

[37] X. Wu, J. C. Keane, R. G. Dhere, C. DeHart, D. S. Albin, A. Duda, T. A. Gessert, S. Asher, D. H. Levi, and P. Sheldon, "16.5%-efficient CdS/CdTe polycrystalline thin-film solar cell," in Proc. 17th Eur. Photovoltaic Sol. Energy Conf., 2001, pp. 995–1000

[38] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, "Solar cell efficiency tables (version 40)," Progr. Photovoltaics: Res. Appl., vol. 20, pp. 606–614, 2012.

[39] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, "Solar cell efficiency tables (version41),"Progr.Photovoltaic:Res.Appl., vol. 21, pp. 1–11, 2013.

[40] Gloeckler, M.; Sankin, I.; Zhao, Z., "CdTe Solar Cells at the Threshold to 20% Efficiency," Photovoltaics, IEEE Journal of , vol.3, no.4, pp.1389,1393, Oct. 2013

[41] W. Shockley and H. J. Queisser, "Detailed balance limit of efficiency in P-N junction solar cells," J. Appl. Phys., vol. 32, no. 3, pp. 510–510, 1961.

[42] R. M. Geisthardt, M. Topič and J. R. Sites, "Status and Potential of CdTe Solar-Cell Efficiency," in IEEE Journal of Photovoltaics, vol. 5, no. 4, pp. 1217-1221, July 2015

[43] R. Geisthardt, “Device characterization of cadmium telluride photovoltaics,” Ph.D. dissertation, Dept. Phys., Colorado State Univ., Fort
Collins, CO, USA, 2014.

[44] Zhao, Yuan, et al. "Monocrystalline CdTe solar cells with open-circuit voltage over 1 V and efficiency of 17%." Nature Energy 1 (2016): 16067.

[45] Burst, James M., et al. "CdTe solar cells with open-circuit voltage breaking the 1 V barrier." Nature Energy 1 (2016): 16015.

[46] James Sites, Jun Pan, Strategies to increase CdTe solar-cell voltage, Thin Solid Films, Volume 515, Issue 15, 31 May 2007, Pages 6099-6102

[47] Hsiao, Kuo-Jui, and James R. Sites. "Electron reflector strategy for CdTe solar cells." Photovoltaic Specialists Conference (PVSC), 2009 34th IEEE. IEEE, 2009.

[48] P. S. Kobyakov, D. E. Swanson, J. Drayton, J. M. Raguse, K. L. Barth, and W. S. Sampath, Progress towards a CdS/CdTe solar cell implementing an electron reflector,” in Proc. 39th IEEE Photovoltaic Spec. Conf., 2013, pp. 0386–0391.

[49] T. A. Gessert, J. N. Duenow, S. Ward, J. F. Geisz, and B. To, “Analysis of ZnTe:Cu/Ti contacts for crystalline CdTe,” in Proc. 40th IEEE Photovoltaic Spec. Conf., 2014, pp. 2329–2333

[50] Yiming Liu, Yun Sun, Angus Rockett, A new simulation software of solar cells—wxAMPS, Solar Energy Materials and Solar Cells, Volume 98, March 2012, Pages 124-128, ISSN 0927-0248

[51] T.A. Gessert, S. Asher, S. Johnston, A. Duda, M.R. Young, T. Moriarty, “Formation of ZnTe:Cu/Ti contacts at high temperature for CdS/CdTe devices,” in Proc. 4th World Conf. PV Energy Conv., 2006, pp. 432-435

[52] A. Kanevce and T. A. Gessert, "Optimizing CdTe Solar Cell Performance: Impact of Variations in Minority-Carrier Lifetime and Carrier Density Profile," in *IEEE Journal of Photovoltaics*, vol. 1, no. 1, pp. 99-103, July 2011.

[53] Wei, Su-Huai, and S. B. Zhang. "Chemical trends of defect formation and doping limit in II-VI semiconductors: The case of CdTe." Physical Review B66.15 (2002): 155211.

[54] Shepidchenko, Anna, et al. "Tailoring of defect levels by deformations: Te-antisite in CdTe." *Journal of Physics: Condensed Matter* 25.41 (2013): 415801.

[55] V. Lyahovitskaya, L. Chernyak, J. Greenberg, L. Kaplan, and D. Cahen, J. Cryst. Growth 214Õ215, 1155 ~2000

[56] Mauricio A. Flores, Walter Orellana, Eduardo Menéndez-Proupin, First-principles DFT + GW study of the Te antisite in CdTe, Computational Materials Science, Volume 125, December 2016, Pages 176-182

[57] A.V. Krukau, O.A. Vydrov, A.F. Izmaylov, and G.E. Scuseria, “Influence of exchange screening parameter on the performance of screened hybrid functionals,” J. Chem. Phys., vol. 125, pp. 224106, 2006.

[58] Lindstorm, Anna “Defects and impurities in CdTe: An ab Initio Study”, Ph.D. Dissertation

[59] Lindström, A., et al. "High resistivity in undoped CdTe: carrier compensation of Te antisites and Cd vacancies." Journal of Physics D: Applied Physics49.3 (2015): 035101.

[60] Berding, M. A. "Native defects in CdTe." *Physical Review B* 60.12 (1999): 8943.

[61] Du, Mao-Hua, Hiroyuki Takenaka, and David J. Singh. "Carrier compensation in semi-insulating CdTe: First-principles calculations." *Physical Review B*77.9 (2008): 094122.

[62] Biswas, Koushik, and Mao-Hua Du. "What causes high resistivity in CdTe." *New Journal of Physics* 14.6 (2012): 063020.

[63] Krasikov, D. N., et al. "Theoretical analysis of non-radiative multiphonon recombination activity of intrinsic defects in CdTe." *Journal of Applied Physics* 119.8 (2016): 085706.

[64] Ma, Jie, et al. "Dependence of the minority-carrier lifetime on the stoichiometry of CdTe using time-resolved photoluminescence and first-principles calculations." *Physical review letters* 111.6 (2013): 067402..

[65] W. Shockley and W.T. Read, Phys. Rev. 87, 835 (1952).

[66] R.N. Hall, Phys. Rev. 87, 387 (1952).

[67] Gessert, T. A., et al. "Research strategies toward improving thin-film CdTe photovoltaic devices beyond 20% conversion efficiency." *Solar Energy Materials and Solar Cells* 119 (2013): 149-155.

[68] Yang, Ji-Hui, et al. "Review on first-principles study of defect properties of CdTe as a solar cell absorber." *Semiconductor Science and Technology* 31.8 (2016): 083002.

[69] Yang, Ji-Hui, et al. "Enhanced p-type dopability of P and As in CdTe using non-equilibrium thermal processing." *Journal of Applied Physics* 118.2 (2015): 025102.

[70] Kranz, Lukas, et al. "Doping of polycrystalline CdTe for high-efficiency solar cells on flexible metal foil." Nature communications 4 (2013).

[71] Yang, Ji-Hui, et al. "First-principles study of roles of Cu and Cl in polycrystalline CdTe." *Journal of Applied Physics* 119.4 (2016): 045104.

[72] Seymour, Fred H., et al. "Cu and CdCl2 influence on defects detected in CdTe solar cells with admittance spectroscopy." Applied Physics Letters87.15 (2005): 153507.

[73] F. A. Abulfotuh, Al. Balcioglu, and T. Wangensteen et al., in Proceedings of the 26th IEEE Photovoltaic Specialists Conference, September 29,1997, Anaheim, CA, USA, pp. 451–454.

[74] Castaldini, A., et al. "Deep energy levels in CdTe and CdZnTe." Journal of applied physics 83.4 (1998): 2121-2126.

[75] Ou, S. S., et al. "Hole traps in p-type electrochemically deposited CdTe thin films." Journal of applied physics 55.4 (1984): 1020-1022.

[76] Verstraeten, David, et al. "A combined EPR and modulated photocurrent study of native defects in Bridgman grown vanadium doped cadmium telluride: the case of the tellurium antisite." Semiconductor science and technology 18.11 (2003): 919.

[77] J.H. Greenberg, J. Cryst. Growth 161, 1 (1996)

[78] D.H. Rose, F.S. Hasoon, R.G. Dhere, D.S. Albin, R.M. Ribelin, X.S. Li, Y. Mahathongdy, T.A. Gessert, and P. Sheldon, Prog. Photovoltaics 7, 331 (1999).

[79] L.R Cruz, R.R de Avillez, The formation of CdTe thin films by the stacked elemental layer method, Thin Solid Films, Volume 373, Issues 1–2, 3 September 2000, Pages 15-18

[80] L.Tuller, K.Uematsu and H.K. Bowen, Journal of Crystal Growth 42(1977),150-156

[81] N. Abbas Shah, A. Ali, Z. Ali, A. Maqsood, A.K.S. Aqili, Properties of Te-rich cadmium telluride thin films fabricated by closed space sublimation technique, Journal of Crystal Growth, Volume 284, Issues 3–4, 1 November 2005, Pages 477-485

[82] A. Picos-Vega et al. “ Cd self doping of CdTe polycrystalline films by co-sputtering of CdTe- Cd targets”,J. Appl. Phys. 83, 760 (1998)

[83] McCandless, Brian E., and James R. Sites. "Cadmium telluride solar cells." *Handbook of Photovoltaic Science and Engineering* 2 (2003).

[84] Chopra, K. L., P. D. Paulson, and V. Dutta. "Thin-film solar cells: an overview." Progress in Photovoltaics: Research and Applications 12.2-3 (2004): 69-92.

[85] Arturo Morales-Acevedo, Thin film CdS/CdTe solar cells: Research perspectives, Solar Energy, Volume 80, Issue 6, June 2006, Pages 675-681

[86] Ferekides, C.S., Marinskiy, D., Viswanathan, V., Tetali, B., Palekis, V., Salvaraj, P., Morel, D.L., 2000. High effi- ciency CSS CdTe solar cells. Thin Solid Films 361–362, 520– 526

[87] C.S. Ferekides, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D.L. Morel, CdTe thin film solar cells: device and technology issues, Solar Energy, Volume 77, Issue 6, December 2004, Pages 823-830

[88] Choi, Jun Young, et al. "Properties of cadmium sulfide thin films deposited by chemical bath deposition with ultrasonication." Solar energy 64.1 (1998): 41-47.

[89] Khallaf, Hani, et al. "Characterization of CdS thin films grown by chemical bath deposition using four different cadmium sources." Thin Solid Films516.21 (2008): 7306-7312.

[90] J. Herrero, M.T. Gutierrez, C. Guillen, J.M. Dona, M.A. Martinez, A.M. Chaparro, Rayon, Photovoltaic windows by chemical bath deposition” Thin Solid Films 361-362, (2000), 28-33

[91] K. Durose, P.R. Edwards, D.P. Halliday, Materials aspects of CdTe/CdS solar cells, Journal of Crystal Growth, Volume 197, Issue 3, 15 February 1999, Pages 733-742

[92] A. D. Compaan, A. Gupta, S. Lee, S. Wang, J. Drayton, “High efficiency, magnetron sputtered CdS/CdTe solar cells”, Solar Energy Vol.77 (2004), pp.815–822

[93] N.W. Duffy, L.M. Peter, R.L. Wang, D.W. Lane, K.D. Rogers,“Electrodeposition and characterization of CdTe films for solar cel applications”, Electrochemical Acta 45, (2000), 3355–3365.

[94] G. C. Morris, S. K. Das, “Some Fabrication Procedures for Electrodeposited CdTe Solar Cells”, Inter. Journal of Solar Energy, 12, (1992), 95-108.

[95] S. Ikegami, “CdS/CdTe solar cells by the screen-printing-sintering technique: Fabrication. Photovoltaic properties and applications”, Solar Cells, 23, (1998), 89-105

[96] A. Rohatgi, H. C. Chou, N. M. Jokerst, E. W. Thomas, “Effects of CdTe Growth Conditions and Techniques on the Efficiency Limiting Defects and Mechanisms in CdTe Solar Cells”, AIP. 353, (1996), 368-735

[97] T. L. Chu, S. S. Chu, “High Efficiency thin film CdS/CdTe solar cells”, Inter Journal of Solar Energy, 12, (1992), 121-132.

[98] T. L. Chu, S. S. Chu, C. Ferekides, C. Q. Wu, J. Britt, C. Wang, “High efficiency thin film CdS/CdTe heterojunction solar cells”, Journal of Crystal Growth, Vol. 117, (1992), 1073.

[99] McCandless, B. E. and Sites, J. R. (2010) Cadmium Telluride Solar Cells, in Handbook of Photovoltaic Science and Engineering, Second Edition (eds A. Luque and S. Hegedus), John Wiley & Sons, Ltd, Chichester, UK

[100] Powell R et al., U.S. Patent 5,945,163 (1999).

[101] Massalski, Thaddeus B., et al., eds. *Binary alloy phase diagrams*. Vol. 1. No. 2. Metals Park, OH: American Society for Metals, 1986.

[102] M. Aven, J.S. Prener, Physics and Chemistry of II-VI Compounds, North-Holland Publishing Company, Amsterdam, 1967

[103] Data from Knacke O, Kubaschewski O, Hesselmann K, Thermochemical Properties of Inorganic Substances, 2nd Edition, Springer-Verlag, New York (1991)

[104] A. T. Aldred , J. N. Pratt, J. Chem. Eng. Data, 1963, 8 (3), pp 429–431

[105] Doolan, J. J.,Partington, J. R.,Trans. Faraday Soc.,1924

[106] Levi, D.H., Moutinho, H.R., Hasoon, F.A., Keyes, B.M., Ahrenkiel, R.K., Al-Jassim, M., Kazmerski, L.L., 1994. Micro through nanostructure investigations of polycrystalline CdTe: correlations with processing and electronic structures, Proc. 1st WCPEC, 127–131

[107] P.D. Paulson, V. Dutta, Study of in situ CdCl2 treatment on CSS deposited CdTe films and CdS/CdTe solar cells, Thin Solid Films, Volume 370, Issues 1–2, 17 July 2000, Pages 299-306

[108] R. Dhere, B. Fluegel, A. Mascarenhas, J. Duenow, T. Gessert, “Investigation of effects of processing and impurities on the properties of CdTe using microscopic two-dimensional photoluminescence image technique”, Proc. Of the 34th IEEE PVSC, (2009), pp. 1443-1447.

[109] P. Nollet, M. Burgelman, S. Degrave, J. Beier, “ Importance of air ambient during CdCl2 treatment of thin film CdTe solar cells studied through temperature dependent admittance spectroscopy”, Proc. Of the 29th IEEE PVSC, (2002), pp. 704-707.

[110] Zhao, Hehong, et al. "Vapor chloride treatment studies of CdTe/CdS solar cells." Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE. IEEE, 2002.

[111] T. L. Chu, S. S. Chu, Solid-State Elect., 38, (1995), pp.533-549

[112] H. C. Chou, A. Rohatgi, E. W. Thomas, S. Kamra, A. K. Bhat, Electrochem. Soc., Vol. 142, (1995), pp. 254-259

[113] C. S. Ferekides, V. Viswanathan, D. L. Morel, Proc. 26th IEEE PVSC, (1997), pp. 423-426

[114] J. Tang, D. Mao, L. Feng, W. Song, J. U. Trefny, Proc. 25th IEEE PVSC, (1996), pp. 925-928

[115] Y. L. Soo, S. Huang, S. Kim, G. Kioseglou, Y. H. Kao, Appl. Phys. Lett. 76 (2000), pp. 3729-3731

[116] Demtsu, Samuel, David Albin, and James Sites. "Role of copper in the performance of CdS/CdTe solar cells." 2006 IEEE 4th World Conference on Photovoltaic Energy Conference. Vol. 1. IEEE, 2006.

[117] B.Ghosh, S. Purakayastha, P.K. Datta, R.W. Miles, M.J. Carter, R. Hill, Semicond. Sci. Tech., 10 (1995), 71-76

[118] N. Romeo, A. Bosio, R. Tedeschi, V. Canevari, Thin Solid Films, 361, (2000), 327.

[119] T. L. Chu, S. S. Chu, K. D. Han, M. Mantravadi, Proc. 20th IEEE PVSC, (1988), pp. 1422-1425

[120] S. Johnston, K. Zaunbrecher, R. Ahrenkiel, D. Kuciauskas, D. Albin, and W. Metzger, "Simultaneous Measurement of Minority-Carrier Lifetime in Single-Crystal CdTe Using Three Transient Decay Techniques," Photovoltaics, IEEE Journal of , vol.4, no.5, pp.1295,1300, Sept. 2014

[121] D. V. Lang, "Deep Level Transient Spectroscopy: A New Method to Characterize Traps in Semiconductors." Journal of applied physics 45.7 (1974): 3023-3032.

[122] Coleman, J.J., "Metalorganic chemical vapor deposition for optoelectronic devices," Proceedings of the IEEE , vol.85, no.11, pp.1715,1729, Nov 1997

[123] P.V.Myers, et al., " Atmospheric Pressure Chemical Vapor Deposition of CdTe for High Efficiency Thin Film PV Devices", NREL annual report, 1999.

[124] N. Abbas Shah, A. Ali, Z. Ali, A. Maqsood, A.K.S. Aqili, Properties of Te-rich cadmium telluride thin films fabricated by closed space sublimation technique, Journal of Crystal Growth, Volume 284, Issues 3–4, 1 November 2005, Pages 477-485

[125] Razykov, T.M.; Acher, R.; Crisalle, O.D.; Craciun, V.; Anderson, T.J.; Kouchkarov, K.; Li, S.S.; Goswami, D.Y.; Vijayaraghavan, S., "Characteristics of CdTe films of different compositions fabricated by CMBD," Photovoltaic Specialists Conference, 2005. Conference Record of the Thirty-first IEEE , vol., no., pp.484,486, 3-7 Jan. 2005

[126] Jae-Hyeong Lee, Dong-Gun Lim, Jun-Sin Yi, Electrical and optical properties of CdTe films prepared by vacuum evaporation with close spacing between source and substrate, Solar Energy Materials and Solar Cells, Volume 75, Issues 1–2, January 2003, Pages 235-242

[127] A. Abbas et al., "The Effect of Cadmium Chloride Treatment on Close-Spaced Sublimated Cadmium Telluride Thin-Film Solar Cells," in IEEE Journal of Photovoltaics, vol. 3, no. 4, pp. 1361-1366, Oct. 2013

[128] M. Terheggen, H. Heinrich, G. Kostorz, A. Romeo, D. Baetzner, A.N. Tiwari, A. Bosio, N. Romeo, Structural and chemical interface characterization of CdTe solar cells by transmission electron microscopy, Thin Solid Films, Volumes 431–432, 1 May 2003, Pages 262-266

[129] Poplawsky, J. D., Paudel, N. R., Li, C., Parish, C. M., Leonard, D., Yan, Y., Pennycook, S. J. (2014). Direct Imaging of Cl- and Cu-Induced Short-Circuit Efficiency Changes in CdTe Solar Cells. Adv. Energy Mater., 4: 1400454

[130] R. W. Birkmire , B. E. McCandless & S. S. Hegedus(1992) Effects of Processing on CdTe/CdS Materials and Devices, International Journal of Solar Energy, 12:1-4, 145-154

[131] H.L.Tuller, K.Uematsu and H.K. Bowen, Journal of Crystal Growth 42(1977),150-156

[132] K. K. Chin, T.A. Gessert, Su-Huai Wei, "The roles of Cu impurity states in CdTe thin film solar cells," Photovoltaic Specialists Conference (PVSC), 35th IEEE, pp.001915,001918 (2010)

[133] S. Johnston, K. Zaunbrecher, R. Ahrenkiel, D. Kuciauskas, D. Albin, and W. Metzger, "Simultaneous Measurement of Minority-Carrier Lifetime in Single-Crystal CdTe Using Three Transient Decay Techniques," Photovoltaics, IEEE Journal of , vol.4, no.5, pp.1295,1300, Sept. 2014

[134] Y.Yan, M.M. Al-Jassim, “Transmission electron microscopy of chalcogenide thin-film photovoltaic materials”, Current Opinion in Solid State and Materials Science, Volume 16, Issue 1, February 2012, Pages 39-44.

[135] Y. Yan, M.M. Al-Jassim, and K.M. Jones, “Structure and effects of double-positioning twin boundaries in CdTe” Journal of Applied Physics, 94, 2976-2979 (2003).

[136] D. Mao; C.E. Wickersham, M. Gloeckler, "Measurement of Chlorine Concentrations at CdTe Grain Boundaries," IEEE Journal of Photovoltaics, vol.4, no.6, pp.1655-1658, Nov. 2014.

[137] L. Zhang et al. “Effect of Co-passivation of Cl and Cu on CdTe Grain Boundaries,” Phys. Rev. Lett, Vol. 101, Issue. 15-10, October 2008.

[138] Darius Kuciauskas, Pat Dippo, Zhibo Zhao, Long Cheng, Wyatt Metzger, Recombination Analysis In Cadmium Telluride Photovoltaic Solar Cells with Photoluminescence Spectroscopy, Presented at the 42nd PVSC IEEE conference, 2015.

[139] J. H. Greenberg, J. Cryst. Growth 197(3), 397 (1999)

[140] J. L. Pautrat, J. M. Francou, N. Magnea, E. Molva, and K. Saminadayar, J. Cryst. Growth 72, 194 (1985)

[141] Burst, James M., et al. "Carrier density and lifetime for different dopants in single-crystal and polycrystalline CdTe”."APL Materials” 4.11 (2016): 116102.

[142] W.K. Metzger, D. Albin, M.J. Romero, P. Dippo, and M. Young, J. Appl. Phys. 99, in press (2006)

[143] S.-H. Wei, S.B. Zhang, and A. Zunger, J. Appl. Phys. 87, 1304 (2000).

[144] Bin Lv, Bo Yan, Yun Li, Chenghua Sui, Ellipsometric investigation of S–Te inter-diffusion and its effect on quantum efficiency of CdS/CdTe thin films solar cell, Solar Energy, Volume 118, August 2015, Pages 350-358

[145] H.C. Chou, A. Rohatgi, N.M. Jokerst, S. Kamra, S.R. Stock, S.L. Lowrie, R.K. Ahrenkiel, D.H. Levi, Approach toward high efficiency CdTe/CdS heterojunction solar cells, Materials Chemistry and Physics, Volume 43, Issue 2, 1996, Pages 178-182, ISSN 0254-0584

[146] Park, Ji-Sang, et al. "Effect of intermixing at CdS/CdTe interface on defect properties."Applied Physics Letters” 109.4 (2016): 042105.

[147] Komin, V., et al. "Identification of defect levels in CdTe/CdS solar cells using deep level transient spectroscopy." Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE. IEEE, 2002.

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