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In Situ Extrinsic Doping of CdTe Thin Films for Photovoltaic Applications

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by

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DEDICATION

To my respected parents and beloved siblings.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

The Cadmium Telluride thin film solar cell is one of the leading photovoltaic technologies. Efficiency improvements in the past decade made it a very attractive and practical source of renewable energy. Considering the theoretical limit, there is still room for improvement, especially the cell's open circuit voltage (V_{OC}). To improve V_{OC}, the p-type carrier concentration and minority carrier lifetime of the CdTe absorber needs to be improved. Both these parameters are directly related to the point defect distribution of the semiconductor, which is a function of deposition stoichiometry, dopant incorporation and post-deposition treatments.

CdTe films were deposited by the Elemental Vapor Transport (EVT) deposition method, which allowed in situ control of the vapor phase stoichiometry (Cd/Te ratio). Extrinsic doping of polycrystalline CdTe by in situ incorporation of antimony (Sb) and phosphorus (P) was investigated. The structural and electrical properties of CdTe thin films and solar cells were studied. Sb and P incorporation were found to increase the net p-doping concentration. Cl and Sb improved the minority carrier lifetime of polycrystalline CdTe, while lower lifetime with Cu and P doped films were indicated. Deep Level Transient Spectroscopy (DLTS) was performed on devices fabricated with different deposition stoichiometry, post-deposition treatments, and phosphorus dopant dose. Several majority and minority carrier traps were identified, and assigned to different point defects based on first principle studies in the literature and experimental conditions used for the deposition and processing of the thin films.

CHAPTER 1: INTRODUCTION TO SOLAR

1.1 Solar Energy

In the modern world energy has become one of the basic needs of life. With increasing world population and technological advancements, the worldwide energy consumption is increasing on average by 1.8% a year [1]. Due to the depleting reserves and increasing costs, fossil fuels are hardly expected to cope with this. Our current reserve of oil and natural gas could run out by 2050s [2]. In 2015, 29% of the U.S. greenhouse gas emissions came from electricity production with the majority generated by coal-fired power plants. Nuclear power has the capability of providing large scale power generation, but safety and waste management concerns make it unfitting as a long-term solution. Sooner rather than later, we need to turn to renewable energy sources, and solar energy is one of the most pragmatic candidates.

Among the various renewable energy sources (e.g. solar, wind, water and geothermal heat) in our planet, solar energy is projected to play a dynamic role as a future energy source. Solar energy is expected to be the world's largest source of electricity by 2050, with solar photovoltaics 16% and concentrated solar power 11% of the global overall consumption [3]. The earth's surface receives about 3×10^{24} joules of energy from sunlight per year. This number is nearly 10^4 times more than the whole world's energy consumption [4]. While the source of practically infinite source of energy is there, we need practical methods for conversion, distribution and storage of this energy.

1.2 Photovoltaics

Photovoltaics is the technology of generating direct current electrical power from semiconductors when they are illuminated by the photons in sunlight. Photovoltaic (PV) devices are the primary solar energy conversion systems to produce solar energy. These photovoltaic

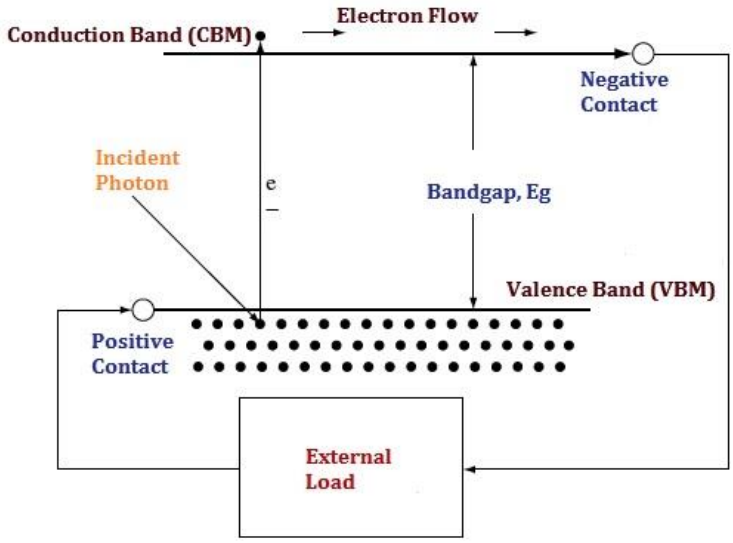

Figure 1.1 Basic operation of a solar cell

devices (also known as solar cells) convert the energy of the incident photons into electrical energy through the generation and subsequent collection of electron-hole pairs. The schematic in Figure 1.1 shows the basic operation of a solar cell. Sunlight consists of photons with a range of energies, dependent on the wavelength of the light (Figure 1.6). Photons with higher energy than the band gap energy (the energy required to free an electron to move around in the lattice) of the semiconductor excites electrons from the valence to the conduction band. These high energy electrons can exit the device in the form of electrical current and perform electrical work at the external load.

1.3 Photovoltaic Technologies

Several solar technologies were and are being explored to achieve reliability, cost-effectiveness and high efficiency with great success. These technologies can be roughly categorized in three generations based on the fabrication processes involved, their performance and cost.

1.3.1 First Generation Solar Cells

The first generation of solar cells are proven technologies with relatively higher photo-conversion efficiency with somewhat expensive production costs. They are the classical example

of homojunction (see section 1.4.1) solar cells. Photo-generated electron-hole pairs are separated and collected through the p-n junction of a doped semiconductor, mainly silicon. The devices are fabricated on single or multi crystalline wafers.

The commercial market is dominated by silicon based solar cells of this generation. Silicon (Si), one of the most abundant materials on the Earth, is the semiconductor used in crystalline form (c-Si) for 90% of the photovoltaic (PV) applications today. The silicon band gap of 1.1 eV, is close to the optimum value for a solar converter (Figure 1.7). Si solar cells can be classified as single crystalline and multi crystalline. These are the most commercially available PV technologies with of 35% for single and 55% for multi crystalline Si of all the newly installed solar cell capacities in 2014 [5].

Single crystal silicon solar cells are made from crystalline Silicon (Si) wafers, which is also the main component of most electronic microprocessors. Cylindrical single crystals are grown (Czochralski or float zone method), sliced into thin wafers and then devices are fabricated on them under a controlled environment. The high production costs are mitigated by wide adoption and large-scale production. The current record for cell efficiencies are at 26.7% and 24.4% for small area cells and large area modules respectively [6].

The Si solar cell technology had a big boost when it was demonstrated that high efficiency solar cells can be fabricated from large-grain (1–10 mm) multi-crystal wafers, called multicrystalline Si. Although the efficiency is a few percent lower compared to crystalline Si, the lower cost and faster fabrication process makes the price per watt the same on a module basis. The current efficiency records are at 22.3% and 19.9% for small area cells and large area modules respectively [6]. The simplicity of the process and the fabrication equipment is showing a clear tendency towards the use of the multicrystalline option.

Although Si has many advantages for PV application, due to its indirect bandgap and consequently low absorption coefficient, it is not the ideal material for light to electricity conversion. The required wafer thicknesses are on the order of hundreds of micrometers leading

to the high processing costs. Single junction Si solar cells are near their theoretical efficiency limit of 33%. The current technology of Si PV devices is likely near its peak and any significant improvement in efficiency or cost may not be possible.

GaAs, a III-V semiconductor, is another attractive first-generation PV technology. It has a larger absorption coefficient and its direct bandgap of 1.42 eV is better matched to the solar spectrum compared to Si (Figure 1.7). Efficiencies up to 28.8% for small area cells and 25.1% for modules have been achieved so far [6]. Nevertheless, due to the high manufacturing costs for GaAs devices, applications are limited to concentrated solar power systems and space applications [5]. GaAs and its “cousins” (other III-V compound semiconductors) have applications in multiple junction or tandem solar cells. Material layers with gradually decreasing bandgaps are stacked to efficiently absorb different regions of the solar spectrum. For 5 junction cells of III-V materials, efficiencies up to 38.8% has been achieved under the terrestrial AM1.5 spectrum. Using direct beam concentrators, the efficiency value can be as high as 46% [6].

1.3.2 Second Generation Solar Cells

Thin film solar cells (TFSC) are the second generation. They are named “thin film SC” because of their absorption material requirement of only a few micrometers in thickness. Their absorption coefficient is much higher than that of Si. The combined economy of less material utilization, lower manufacturing costs and simpler processes make solar panels made from this type of technologies less expensive compared to the first-generation ones. Amorphous Si (α-Si), CIGS and CdTe are the three most widely commercialized TFSCs. Common among the three materials is their direct band gap (1.75 eV, 1.0~1.7 eV and 1.45 eV respectively) and high absorption coefficient, which enables the use of very thin material.

Amorphous Si is typically deposited from hydride gases such as SiH_4 using plasma-enhanced chemical vapor deposition (PECVD). Large area uniform coatings are possible by this method with exceptional control. Nevertheless, much of the source material is wasted as the gas utilization is only 10 to 30%. This material has the lowest fabrication temperature of any of the

TFSC materials (~150 to 300 ºC) allowing the use of lower-cost and low-temperature flexible substrates. Efficiencies up to 10.2% for small area cells and 12.3% for tandem modules have been achieved so far [6]. α-Si devices have niche market in low cost and low power electronics such as toys and calculators. It is not feasible for commercial scale manufacturing due to light-induced degradation and lower efficiency, and is being rapidly displaced by the other technologies.

The compound semiconductor Copper indium gallium diselenide ($CuIn_xGa_{1-x}Se_2$, popularly known as CIGS) with a direct bandgap of 1.0-1.7 eV is a more promising PV material compared to α-Si [7]. It has a market share of 1.3% globally and ~26.5% among the thin film PV market, as of 2016 [8]. Efficiencies up to 22.6% for small area cells and 19.2% for modules have been achieved [9]. Despite having impressive laboratory results, large scale production has been difficult due to the complexity in stoichiometry control.

CdTe is currently the leading TFSC technology with a market share of 3.1% globally and ~63% among the thin film PV market [8]. CdTe is a particularly well-suited semiconductor for PV applications with a direct bandgap of 1.45~1.5 eV and a very strong absorption coefficient. It offers the lowest module costs compared to any other PV technology on the market today. First Solar Inc. is pioneering the CdTe technology development research. Current laboratory record efficiency is at 22.1% and is on par with the efficiency of multi-crystalline Si solar cells [10]. Record module efficiency has reached 18.6% [11]. CdTe is the main focus of this study and is discussed in greater detail in Chapter 2.

1.3.3 Third Generation (Emerging PV Technologies)

Third generation solar cells use novel materials such as complex nanostructures or polymers. Among the emerging technologies, most promising are the Dye Sensitized Solar Cells (DSC) and the Perovskites.

DSC, invented by Michael Graetzel and commonly referred as the Graetzel cells [4], are considered to be the pioneer in the emerging thin film market. An organic dye produces collectible

electron when illuminated. The molecules are adsorbed on a high bandgap and porous inorganic paste, generally TiO_2. An electrolyte acts as the hole transport layer to complete the circuit. Efficiencies up to 11.9% for small area cells and 8.8% for modules have been achieved [6]. Efficiency is not at par with the 1st and 2nd generation PV, but DSCs have other advantages. DSC efficiency is nearly temperature-independent over the typical operating temperature range of 25–65 ºC. For the same range, the efficiency of Si solar cells declines by 20% [12]. In diffused sunlight or cloudy conditions, DSCs exhibit even better efficiency than polycrystalline Si solar cells. Also, the aesthetic aspect of DSCs (can be fabricated in different colors) makes them suitable for certain applications.

Perovskite solar cells have evolved from DSCs and are currently one of the most researched and most promising PV technology. In only 5 years of their development, their efficiency has reached up to 20.9% [6]. The main absorber is a perovskite structured compound which refers to the ABX_3 crystal structure. Most investigated among them is the inorganic–organic lead halide $CH_3NH_3Pb(I,Cl,Br)_3$. They require very low-cost materials, are fabricated using simple manufacturing processes and their bandgap can be tailored to match the solar spectrum. Achieving long term stability and possible lead toxicity are two of the main concerns for this technology, and extensive research is underway [13].

Although the performance and stability of third generation solar cells is still limited compared to first and second generation solar cells, they have a great potential and are already in the commercialization phase.

1.4 Semiconductors and P-N Junctions

First and second generation solar cells are based on a semiconducting material as the light absorber. The conductivity of a Semiconductor can be made p-type (majority carrier hole) or n-type (majority carrier electron) by controlled intrinsic or extrinsic (impurity) doping. Group IV semiconductors, such as Si, can be doped p-type by adding group III elements (e.g. boron) as

they have one less valence electron compared to Si with valency 4. Similarly, phosphorus, a group V element can make Si n-type.

The energy band diagram of a semiconductor is identified by the presence of a bandgap separating the conduction band minima (E_C) and valence band maxima (E_V). Valence band signifies the ground state for the electrons. Electrons reaching the conduction band either by absorbing a photon or having thermal energy can move around freely in the semiconductor lattice. The Fermi level (E_F) relates to the probability of finding an electron across the energy band, and for an intrinsic semiconductor with equal number of electrons and holes, is located at the center of the bandgap (E_i).

1.4.1 Homojunction Solar Cells

At the heart of most 1st and 2nd generation solar cell is the pn junction, formed when a p-type semiconductor and an n-type semiconductor are placed in contact to form an electrical junction. Figure 1.2 shows a simplistic diagram of a p-n junction under thermal equilibrium. Without the presence of any applied bias, an electric field is formed at the p-n junction (depletion region) due to the inter-diffusion of majority charges from each side. Photon absorption from sunlight at the depletion region generates electron-hole pairs as electrons escape the valence band to reach the conduction band. Electrons in conduction band (CB) and holes in valence band (VB) are mobile entities, and can get separated by the built-in electric field. The conduction band

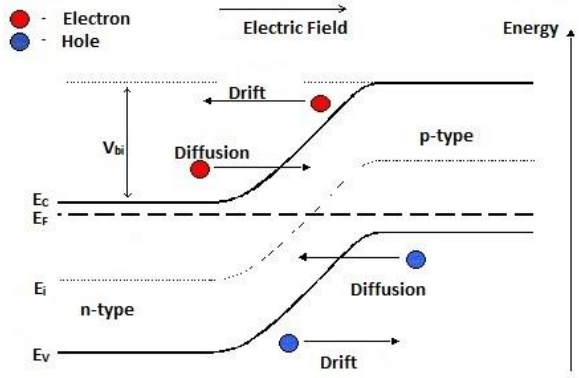

Figure 1.2 Charge separation in a P-N homo-junction

electrons driven to the external circuit by the E-field, lose their energy by doing work in the external circuit. (Figure 1.1).

First generation solar cells are homojunction devices which means both the p-type and n-type part of the p-n junction consists of same semiconductor material doped with different type of impurities to achieve both conductivity types (Figure 1.2).

1.4.2 Heterojunction Solar Cells

In a p-n heterojunction, the p-type and n-type materials are of two different semiconductors. This leads to the formation of valance and conduction band offsets. Figure 1.3 shows a type II heterojunction formed between a p-type CdTe absorber and n-type CdS absorber. Contrary to homojunction devices, conduction and valence band discontinuities can lead to barriers for electron and/or holes. In the CdS/CdTe solar cell, the CdS layer is made very thin and the electron-hole generation is mostly in the p-CdTe absorber. The electric field is dominantly in the CdTe due to orders of magnitude lower doping concentration compared to CdS. Due to the E-field driving the photogenerated holes across the CdTe layer, the VB offset doesn't affect device performance. Electrons are driven across the CdS/TCO layer, and the small 'cliff' (negative ΔE_C) due to CB offset may cause loss of voltage. [14]

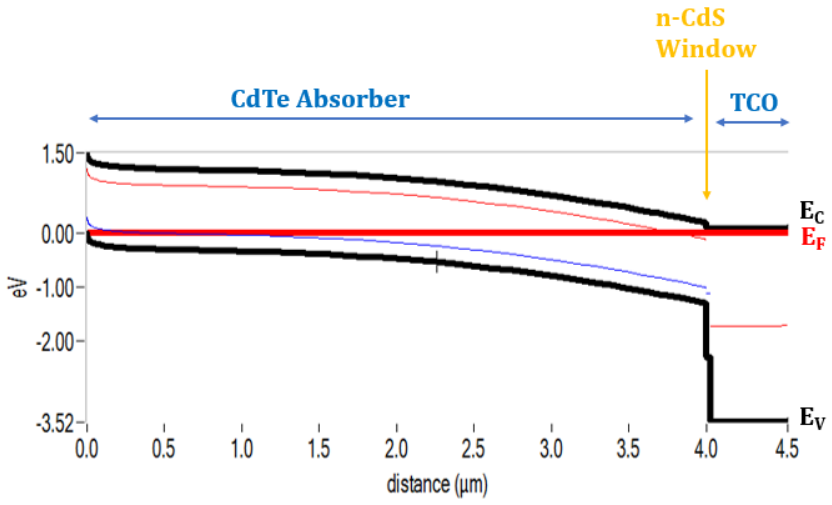

Figure 1.3 Type II heterojunction for CdS/CdTe solar cell

1.5 Solar Cell Terminologies

A current source in parallel with a forward biased diode can serve as the equivalent circuit of an ideal solar cell (Figure 1.4). Series (R_S) and parallel (R_{SH}) resistances are added to account for various loss mechanisms.

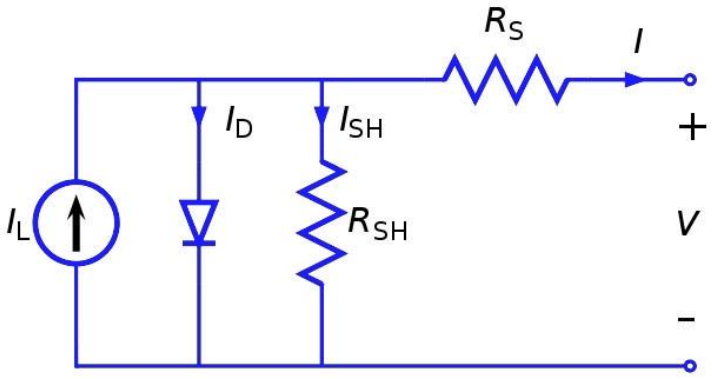

Figure 1.4 Equivalent circuit diagram of a solar cell

1.5.1 Photo Conversion Efficiency

The efficiency (η) of a solar cell is the ratio of maximum electrical power output to the power input from the sun. Thus, the mathematical definition of efficiency:

$$\eta = \left(\frac{V_{OC} \times I_{SC} \times FF}{P_{in}}\right) \qquad (1.1)$$

where, P_{in} is the power input from the sunlight. V_{OC}, I_{SC} and FF refer to open circuit voltage, short circuit current and fill factor.

Fill Factor (FF) is a measure of the maximum power output from a solar cell irrespective of the biasing. It represents the squareness of the I-V curve (Figure 1.5) and is defined as the ratio of the maximum power to the product of V_{OC} and I_{SC} for the solar cell:

$$FF = \frac{V_m \times I_m}{V_{OC} \times I_{SC}} \qquad (1.2)$$

where, V_m and I_m are the voltage and current at maximum power point. The fill factor is a function of the series and shunt resistance of the solar cell. It reflects the extent of various electrical losses during cell operation.

The short circuit current is the current obtained from a solar cell when the output is short circuited (when the load resistance is zero). The solar cell short-circuit current is generally represented as current density, J_{sc}:

$$J_{SC} = \frac{I_{SC}}{A} \qquad (mA/cm^2) \tag{1.3}$$

where A is the effective area of the solar cell. It is a function of the solar illumination, optical properties and charge transfer probability of the cell.

The open circuit voltage (V_{OC}) is the maximum output voltage available from a solar cell and is obtained when the cell is operating without a load (i.e. open-circuited). It is a function of the semiconductor bandgap, doping concentration and charge recombination (minority carrier lifetime) in the cell. For a pn-junction solar cell, the V_{OC} is given by:

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right) \qquad (volts) \tag{1.4}$$

where kT/q is the thermal voltage, N_A is the doping concentration, Δn is the excess minority carrier concentration in the absorber and n_i is the intrinsic carrier concentration.

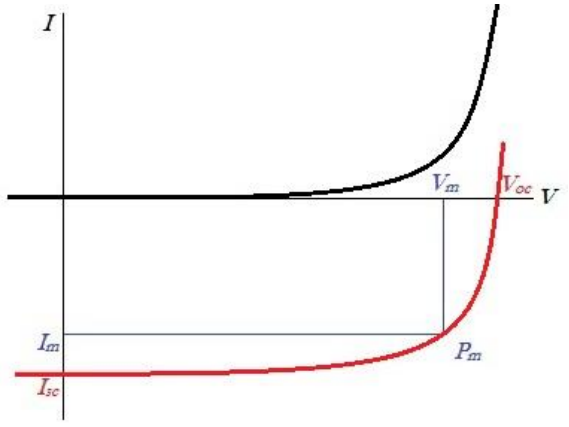

Figure 1.5 Typical current-voltage relationship of a solar cell. Light (red line) and dark (black line).

1.5.2 Solar Spectrum and Quantum Efficiency

Cell efficiency also depends on the incident light spectrum and intensity as well as operating temperature. The internationally recognized standard condition for efficiency measurements for terrestrial applications is known as 'AM1.5 Global' solar irradiation at a temperature of 25°C (Figure 1.6); the figure is drawn based on the standardized data provided in [15]. Air Mass (AM) coefficient is defined as the ratio of the path length for sunlight through the atmosphere to the path length vertically upward (zenith). Since, AM = $[\cos\theta]^{-1}$ where θ is the zenith angle, AM1.5 refers to a zenith angle of 48.2º.

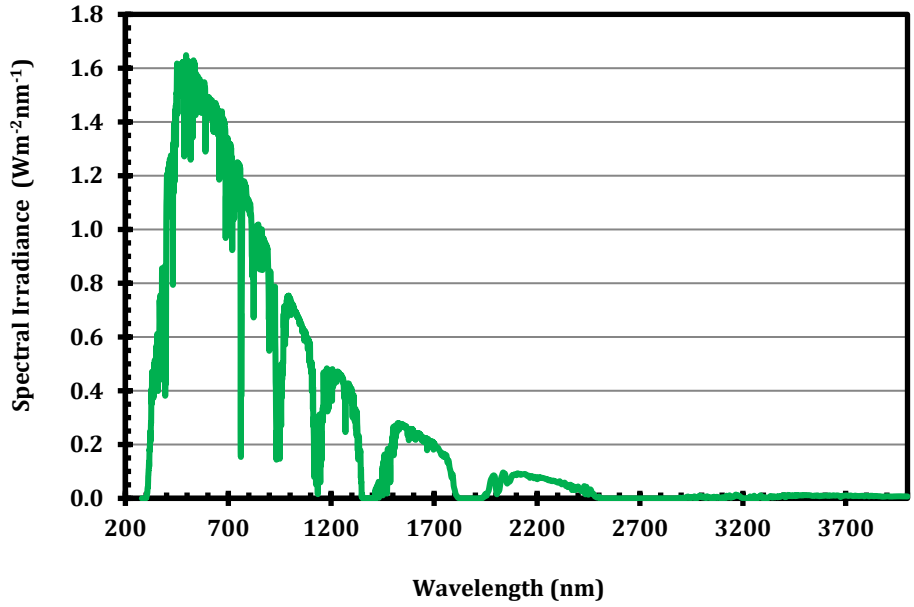

Figure 1.6 'AM1.5 Global' spectra for solar cell measurement

Quantum efficiency (QE) or 'External Quantum Efficiency (EQE)', sometimes also referred to as Incident Photon to Charge Carrier Efficiency (IPCE) is a measure of how efficient a solar cell is in producing photo-generated charge at a given wavelength of light. It is the ratio of the number of incident photons to the number of charge carriers generated and is a function of the excitation wavelength:

$$QE(\lambda) = 1240 \times \frac{I_{SC}}{\lambda \times \phi} \qquad (1.5)$$

where, I_{SC} is the short circuit current (mA/cm^2), λ is the wavelength (nm) and Φ is the incident radiative light flux (W/m^2).

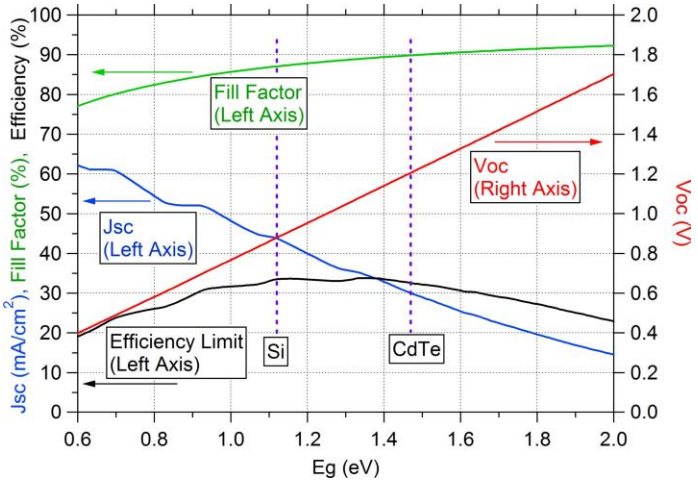

Figure 1.7 Theoretical maximums of the solar cell performance parameters

Figure 1.7* shows the theoretical maximum of these solar cell parameters as a function of the absorber material bandgap [16].

1.6 Summary of Chapter 1

The current status of different PV technologies along with their advantages and disadvantages are discussed. A simple operating principle for a solar cell is presented and the parameters to quantify solar cell performance are introduced. This chapter sets up the introductory information for the remaining part of this dissertation.

* Reprinted with permission from [16]. Permission is included in Appendix B.

CHAPTER 2: CADMIUM TELLURIDE SOLAR CELLS: THEORY AND LITERATURE

2.1 Why CdTe

The CdTe solar cell is one of the most promising thin film PV technologies. CdTe has nearly ideal band gap of ~1.45 eV (Figure 1.7) to convert sunlight into electricity and is a direct band gap material. The absorption coefficient in the visible range is greater than 5×10^5 cm^{-1} [17]. This means a CdTe film only a few micrometers thick can absorb more than 99% of photons with up to 855 nm wavelength. The material cost for CdTe solar cells is relatively low compared to Si solar cells, which require significantly thicker absorbers (100s of micrometers). CdTe thin films can be deposited by various low-cost methods, such as close spaced sublimation (CSS), electro deposition, spray deposition, screen-printing, and physical vapor deposition (PVD). All these deposition methods can lead to high efficiency devices. Recently the efficiency of CdTe solar cells has surpassed that of multi-crystalline Si [6]. Although CdTe cell efficiency has improved significantly over the last decade, the performance needs to be further boosted to continue to be a viable alternative to fossil fuel options.

2.1.1 Environmental Concerns for CdTe

There is a general sensitivity among the public regarding CdTe PV, due to the health and environmental issues regarding elemental Cd. The subject has been studied extensively since CdTe has been gaining ground in the PV industry. Studies have shown that CdTe PV has the lowest life cycle carbon footprint and is one of the most environment friendly photovoltaic technologies [18].

CdTe as a compound is more stable and less soluble compared to elemental Cd, hence much less toxic. Nevertheless, the PV industry treats CdTe with same precautions as those applied to Cd [19]. Cd is a byproduct of zinc production, leading to production of few tens of

thousands of tons of Cd annually. If not processed industrially, this byproduct Cd must be treated as hazardous waste. Rechargeable batteries use more than half of this amount, and the rest goes to other minor applications. It requires only 1% of the Cd production, for a GW/year scale CdTe PV manufacturing [19]. Leading CdTe solar cell manufacturer First Solar conducted medical monitoring on the persons working at their facilities, and the Cd level in their systems were found to be well below the threshold limit [20]. It is economically and technically possible to operate a CdTe PV manufacturing plant with zero Cd emission [21]. Additional concerns are the broken modules and fire hazards during the active lifetime of a solar panel. Due to the low vapor pressure of CdTe at temperatures of typical residential fires (800-1000 ºC), no Cd is released. Besides, the compounds are encapsulated in molten glass [22]. The leaching of hazardous material from broken panels were also found to be well below the tolerance limit [23].

2.2 CdTe Photovoltaics Development Timeline

Crystalline CdTe was first produced by Frerichs in 1947, using a reaction of Cd and Te vapors in a hydrogen atmosphere [24]. Jenny and Bube in 1954 reported for the first time that *p*-type and *n*-type conductivity could be attained in CdTe by doping with extrinsic impurities [25]. Later, the work of Kruger and de Nobel revealed that the conductivity type of CdTe could also be changed by varying the Cd-Te stoichiometry [26]. Excess Cd yielded *n*-type and excess Te yielded *p*-type conductivity.

Single-crystal homo-junction CdTe cells were demonstrated by Rappaport at RCA Laboratories in 1959 [27]. The conversion efficiency of the device was ~2% and was fabricated by diffusing indium into *p*-type CdTe crystals to form the p-n junction. In 1963, the first CdTe thin film solar cells were demonstrated by Cusano [28]. The device structure was CdTe/$Cu_{2-x}Te$, where $Cu_{2-x}Te$ was used as the p-layer and CdTe was the n-layer. CdTe/CdS solar cells, which is currently the most typical CdTe photovoltaic device structure, were first proposed in 1968 by Andirovich [29]. Only ~1 % efficiency devices could be achieved at that time. Kodak demonstrated 10% efficient devices in 1981 and in 1990 AMETEK achieved 12% devices. After 1990, the

research was led by USF, Photon Energy and BP alternatively. C. Ferekides and J. Britt improved the efficiency up to 15.8% devices in 1992 [30]. In the late 1990s, NREL was leading the CdTe photovoltaic research pushing efficiency numbers above 16%. Since the beginning of 2000s, the record for thin film CdTe solar cell has been held by First Solar (FSLR). The current record for laboratory efficiency is at 22.1% [10]. CdTe based solar cells are also leading the thin film photovoltaics industry with a module efficiency of 18.6% [11].

Table 2.1 Recent progress in CdTe photovoltaics

Year	Affiliation	Efficiency (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Ref.
1993	USF	15.8	843	25.1	74.5	[30]
1997	Matsushita	16.0	840	26.1	73.1	[31]
2001	NREL	16.7	845	26.1	75.5	[32]
2011	FSLR	17.3	845	27.0	75.8	[33]
2012	GE	18.3	857	27.0	79.0	[34]
2012	FSLR	18.7	852	28.6	76.7	[35]
2014	FSLR	21.4	876	30.25	79.4	[36]
2016	FSLR	22.1	-	-	-	[10]

2.3 CdTe: A Defect Semiconductor

CdTe is a group II-VI defect semiconductor. It is evident from Cd-Te system phase diagram (Figure 2.1) that CdTe as a semiconductor can only be grown near stoichiometry [37] (simplified image, redrawn based on the reference). The single-phase, homogeneity region for CdTe allows growing the semiconductor only with a maximum excess of only $4x10^{-3}$ at. % (160 ppm or 2.5×10^{18} cm^{-3} defects) of Cd and $13x10^{-3}$ at. % (520 ppm or 8.1×10^{18} cm^{-3} defects) of Te [38]. Within this homogeneity limit, different point defects can form in CdTe during crystal growth. For example, growth in Cd-rich condition can create tellurium vacancies (V_{Te}). Te-rich growth conditions can create cadmium vacancies (V_{Cd}) (Figure 2.2). These defects can be donors, acceptors or charge neutral. The activation/ionization energy and concentration of these defects determine the net doping concentration and minority carrier lifetime of the material. Both p- and n-type conductivity in CdTe can be achieved based on the deposition stoichiometry. Cd-rich

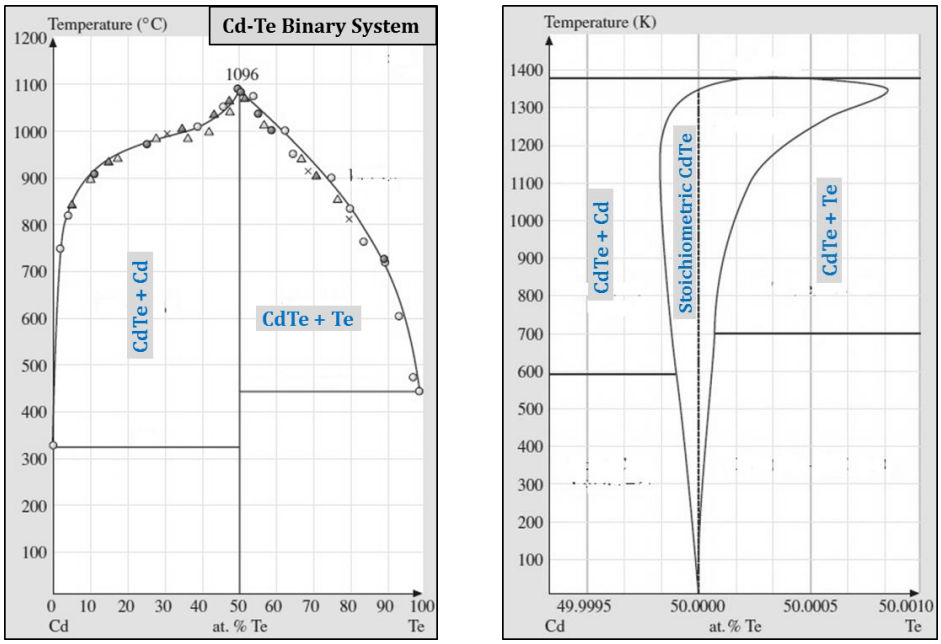

Figure 2.1 Phase diagram of the Cd-Te system

grown films are n-type due to the presence of interstitial Cd (Cd_i) and V_{Te} donors, while Te-rich films are p-type because of V_{Cd} acceptor defects. Table 2.2 lists some of the commonly occuring native point defects in CdTe [39].

Table 2.2 Commonly occurring native point defects in CdTe

Symbol	Defect Name	Description	Favorable Growth Condition
V_{Cd}	Cadmium vacancy	Missing Cd atom	Te-rich
V_{Te}	Tellurium vacancy	Missing Te atom	Cd-rich
Cd_i	Cadmium interstitial	Extra Cd atom in the lattice	Cd-rich
Te_i	Tellurium interstitial	Extra Te atom in the lattice	Te-rich
Cd_{Te}	Cd antisite	Cd at a Te lattice site	Cd-rich
Te_{Cd}	Te antisite	Te at a Cd lattice site	Te-rich

From a material properties perspective, the efficiency of a solar cell is directly related to the net doping concentration and minority carrier lifetime of the absorber semiconductor. Various shallow and deep defects can form in CdTe, depending on the deposition technique, deposition parameters and post deposition treatments which ultimately determine the carrier concentration and lifetime of the material, and consequently the solar cell performance.

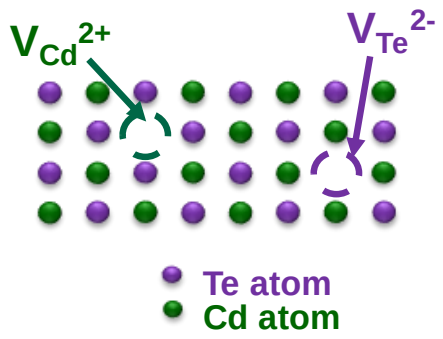

Figure 2.2 Simplified 2D depiction of Cd and Te vacancy point defects

2.3.1 Theoretical Analysis of Defects

First principles calculations and modeling were performed by different research groups across the globe to identify the various defect levels in CdTe, and their electrical properties in determining solar cell performance. The defect formation energy and their transition energies were calculated by modelling the CdTe lattice structure based on Density Functional Theory (DFT). These models are computationally extensive and require specific approximations to reach convergence. For this reason, we come across different set of theories from different studies on how various defects might affect material properties. Due to the availability of more computational resources and updated experimental information we often encounter that the models are being continuously updated by the same research group. Figure 2.3 shows various intrinsic and extrinsic defect levels in CdTe and their activation energies based on first principle calculations by different research groups. One of the most extensive early first principle defect modelling for CdTe was done by Wei *et al.* in 2002 [39]. The model was updated in 2013 [40] and 2016 [41]. Another recent model is from Krasikov *et al.* [42]. Both groups used first-principles DFT calculations with Heyd–Scuseria–Ernzerhof (HSE) approximation.

Although there are significant differences among these models, there are also some common findings. Most researchers agree that the principal acceptor defect in p-type CdTe is the cadmium vacancy. However, there is major debate on the transition energy of V_{Cd}, which ranges from 0.1 to 0.8 eV above the VBM [41, 42, 43, 44]. The other important native defect is the

tellurium vacancy (V_{Te}), which is a shallow donor based on recent models [41, 42]. The compensating mechanism between these two defects limits the p-type dopability in intrinsic CdTe. Other donor defects, such as Te_{Cd} and Cd_i, also play a role. The formation energy of these defect levels is a function of deposition stoichiometry and the Fermi energy (Figure 2.4*). Te-rich deposition is a favorable condition for p-type CdTe, but intrinsic p-dopability is limited by compensating defects; the maximum achievable hole density is 1.77×10^{14} cm^{-3} with the Fermi level of 0.35 eV above the VBM [41].

The next important intrinsic defect is Te_{Cd}. Both Wei *et al.* and Krasikov *et al.* proposed that Te_{Cd} is the main lifetime limiting defect in CdTe, although a different tapping mechanism was anticipated; Te_i is another midgap defect. Both of these defects are favorable in Te-rich deposition conditions. Thus, lower lifetime is expected in intrinsic Te-rich deposited film despite having higher

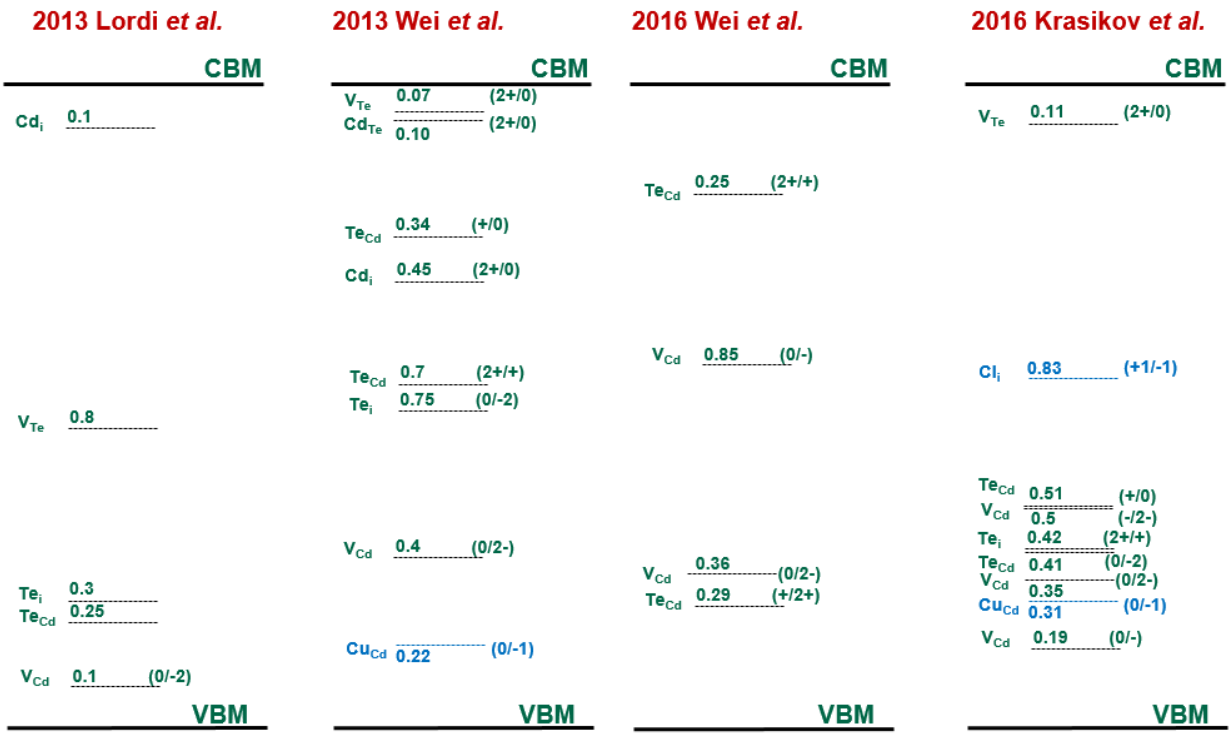

Figure 2.3 Intrinsic and extrinsic point defects in CdTe and their ionization energies

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p-doping. This theory was supported by Time Resolved Photoluminescence (TRPL) measurements performed on very large grain (effectively crystalline) pX CdTe [45].

Depositions under excess Cd conditions have the potential to attain high carrier lifetime by inhibiting formation of Te_{Cd} and Te_i. Since Cd-rich conditions also favor donor defects such as V_{Te} and Cd_i, p-type conductivity can be achieved by using group V materials as dopants (discussed in section 2.4). This method has the possibility of attaining better minority carrier lifetime by limiting midgap defects, while also achieving p-type conductivity.

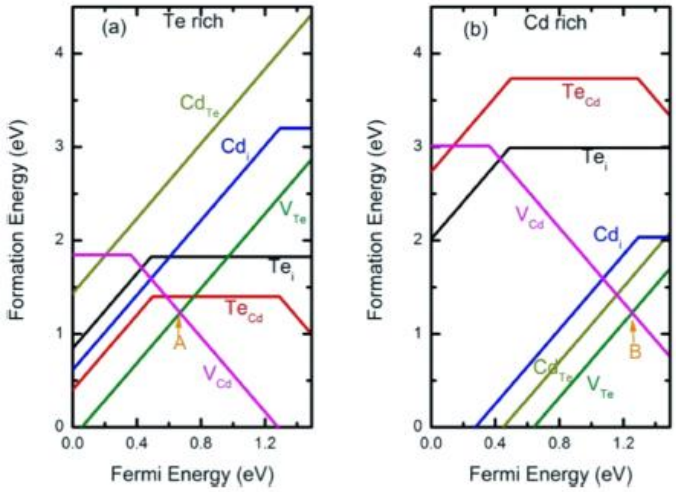

Figure 2.4 Formation energy of intrinsic and extrinsic point defects in CdTe

2.3.2 Experimental Characterization of CdTe Defects

The incongruity among scientific community about the defect distribution in CdTe was outlined in the previous section. The evolution of these defect models was triggered often by their inability to properly explain experimental results. Attempts to experimentally identify various defects in CdTe were done by many different studies. The characterization methods include Deep Level Transient Spectroscopy (DLTS) [46, 47, 48], Photoluminescence (PL) [49, 50], Admittance Spectroscopy (AD) [51, 52], Photo-induced Current Transient Spectroscopy (PICTS) [53] and Thermo-Electric Effect Spectroscopy (TEES) [54]. The findings of these methods vary significantly due to the employment of different methods of deposition and post-deposition treatments. In this

study, DLTS was employed to identify and analyze the defect distribution in CdTe as a function of different deposition stoichiometry and dopant incorporation.

2.3.3 Deep Level Transient Spectroscopy (DLTS)

The minority carrier lifetime of a material is directly related to its deep defect distribution, which can be measured by the DLTS method. During the DLTS measurement the change in capacitance on a reverse biased one-sided p^+n or n^+p junction due to charge carrier injection is measured. The capacitance transient when the injected carriers are removed, is given by the following equation,

$$C(t) = C_0\left[1 - \frac{N_T}{2N_D} exp\left(-\frac{t}{\tau}\right)\right] \qquad (2.1)$$

Here, C(t) is the instantaneous capacitance as a function of time (t), C_0 is the background capacitance at reverse bias, N_D is the doping concentration, N_T is the trap concentration and τ is the carrier lifetime. The change in the transient can be negative or positive, depending on the type (majority or minority) of the trap levels being active in the semiconductor at a certain temperature (Figure 2.5).

The capacitance decay rate is determined by the thermal emission rate of the traps and is a function of temperature. The DLTS spectrum is a plot of change in capacitance (ΔC) captured

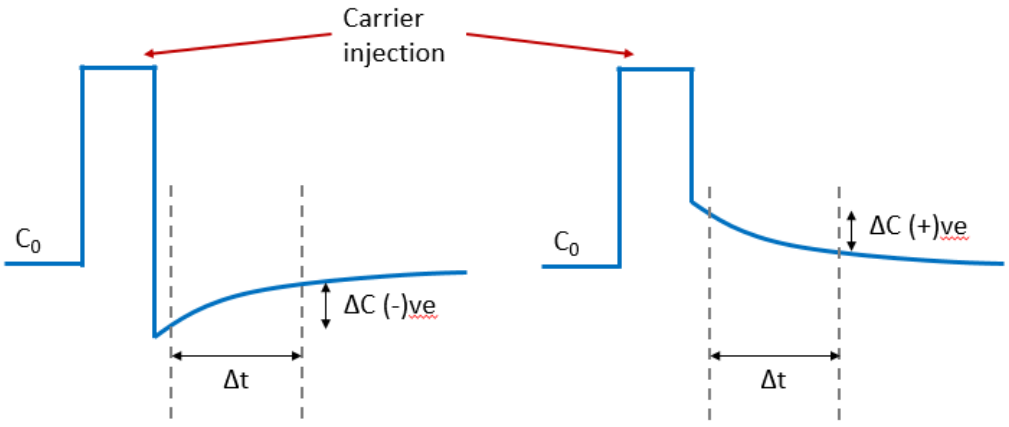

Figure 2.5 Capacitance transient during DLTS measurement

through a time rate window (Δt) vs. temperature (T). A DLTS peak is observed only if the emission time constant of one trap level falls into the rate window given by the selection of t_1 and t_2 values.

A negative peak is observed if the trap is of a majority carrier, while a minority carrier trap introduces a positive peak in the DLTS spectra (ΔC vs. T). The trap concentration is proportional to the peak intensity given by the following equation,

$$N_T = \frac{2\Delta C V_r}{C_0 \Delta V}(N_{D-}N_A) \qquad (2.2)$$

and can be calculated form the background capacitance and doping concentration data. The activation energy and capture cross section of the trap is calculated by evaluating the Arrhenius plot of the peak positions at different rate windows [55].

2.3.4 DLTS on CdTe in Literature

CdS is considered to make an effective n^+p–junction suitable for DLTS measurement at the CdS/CdTe interface heterojunction [56, 57]. Table 2.3 lists the result of DLTS studies on CdTe devices grown by different methods found in the literature.

2.4 Extrinsic Dopants in CdTe

Extrinsic p-type doping of CdTe can be achieved using two different approaches. Firstly, by using group I elements such as, Cu or Na to substitute Cd, which is favorable under Te-rich deposition conditions. Secondly, using group V (P, As, Sb) elements to substitute Te and this is favorable under Cd-rich deposition conditions. Nevertheless, for both the intrinsic and extrinsic cases, the formation of compensating defects limits the upper boundary of dopability. Recent theoretical studies suggest that intrinsically p-type CdTe (Te-rich deposited) could suffer from low minority carrier lifetime because of the formation of various midgap defects (Te_{Cd} and Te_i). Hence, even if a high carrier concentration is achieved for intrinsically-doped p-type CdTe poor carrier lifetime would limit the V_{OC} [40]. Cd-rich films are theorized to exhibit better lifetime at the cost of having the wrong type of doping for heterojunction CdS/CdTe solar cells. CdTe deposited under Cd-rich condition can be grown p-type using extrinsic dopants. This work intends to explore the

use of Group V elements (Sb and P) as dopants for CdTe and characterizes the electronic properties of the resulting films.

Table 2.3 Defects identified in CdTe by DLTS method from literature

CdTe Growth Method	Defects Identified	Defect Assignment	Reference
Travelling Heater	E_V+0.12	V_{Cd}-Cl_{Te}	[46]
	E_V+0.32	Cu_{Cd}	
	E_V+0.40	V_{Cd}	
	E_V+0.76	Deep donor	
CSS	E_V+0.13	V_{Cd}-Cl_{Te}	[58]
	E_C-0.18	Cu_i	
CSS	E_V+0.11	V_{Cd}-Cl_{Te}	[59]
	E_V+0.19	--	
	E_V+0.70	--	
Bridgman, Travelling Heater	E_V+0.20	--	[60]
	E_V+0.45	--	
	E_V+0.65	--	
CSS	E_V+0.34	Cu_{Cd}	[47]
	E_V+0.45		
	E_C-0.28	Cu_i^{++}	
CSS	E_V+0.12	V_{Cd}-Cl_{Te}	[61]
	E_V+0.30	Cu_{Cd}	
	E_V+0.43	V_{Cd}	
CSS	E_V+0.48	--	[62]
	E_C-0.26	--	
	E_C-0.95	--	
	E_C-1.00	--	
MBE	E_V+0.64	--	[63]
	E_V+0.17	V_{Cd}-Cl_{Te}	

2.4.1 $CdCl_2$ Treatment

A chlorine (Cl)-based post-deposition heat-treatment is crucial for CdTe solar cells to obtain high conversion efficiency. The exact role that Cl plays in polycrystalline CdTe is still under debate. Among the various effects that have been observed are: promoting interdiffusion between CdTe and CdS to improve the CdS/CdTe interface [64], recrystallization and grain growth [65], enhanced carrier collection [66], and passivation of deep defects to improve lifetime [67]. Recent experimental studies indicated that Cl in CdTe film was mostly segregated at grain boundaries,

with only a small percentage (on the order of 10^{16} -10^{17} cm^{-3}) penetrating the grain interior [68]. Chlorine can form several point defects in CdTe, such as Cl_i interstitial defects and Cl_{Te} substitutional defects by removal of Te atoms from their lattice sites. The later process can also form Te_i native defects [69]. It has been proposed by many groups that Cl_{Te} can form complex acceptor defects by combining with V_{Cd}, called A-centers (V_{Cd}-Cl_{Te}), to improve net p-doping [70]. A-centers are expected to be shallow acceptors with an activation energy 0.11 to 0.17 eV, reported in the literature (section 2.3.4). Formation of this complex defect is dependent on the availability of cadmium vacancies; thus, “excessive” Cl treatment can reduce net p-doping by compensation due to Cl_i and Cl_{Te}. Cl_{Te} is a shallow donor with ionization energy 0.19 eV, while Cl_i can act as both shallow donor (E_C - 0.17 eV) and shallow acceptor (E_V + 0.22 eV) [41].

2.4.2 Copper Doping

All high efficiency CdTe solar cells to date use Cu doping. Cu in CdTe can either form a substitutional defect or an interstitial defect, Cu_{Cd} and Cu_i respectively. Cu_i is a shallow donor (0.01eV) while Cu_{Cd} is a deeper acceptor level (0.15 - 0.34 eV) [41]. The mobility of interstitial Cu is very high. Copper plays two important roles in CdTe solar cells. It can occupy Cd sites to form the acceptor defect Cu_{Cd}. Thus, Cu takes up the V_{Cd} sites in intrinsically doped CdTe and due to its lower activation energy compared to V_{Cd}, improves the carrier concentration [71]. It also dopes the CdTe back contact surface layer p+ to assist the formation of an ohmic back contact by tunneling. Inclusion of controlled amounts of Cu also led to the record breaking efficiency in substrate configuration CdTe solar cells [72].

The diffusion of Cu in CdTe is also believed to be responsible for instability observed in CdTe/CdS solar cells. Interstitial Cu diffuses fast and accumulates at the interface of CdTe/CdS and is believed to be the main reason of degradation. Asher *et al*. reported a significant amount of Cu diffused through the CdTe/CdS layer to compensate the shallow donor levels with deep acceptors in CdS [73]. But an earlier study at USF, where Cu was introduced directly on CdS

surface, showed that a suitable amount of Cu in the interface also improves the device performance [74].

Excess Cu adversely affects the minority carrier lifetime in CdTe [75], and acceptor defect Cu_{Cd} is reported to be acting as SRH recombination center [76]. However, based on first principle studies, Krasikov *et al.* theorized that in Cl and Cu doped CdTe, stable $(Cl_i–Cu_{Cd})^{2+}$ defect complexes can form that become the dominant compensating defects limiting the p-type doping. Formation energies of various Cl and Cu related defects in Cd- and Te-rich deposition conditions are shown in Figure 2.6*.

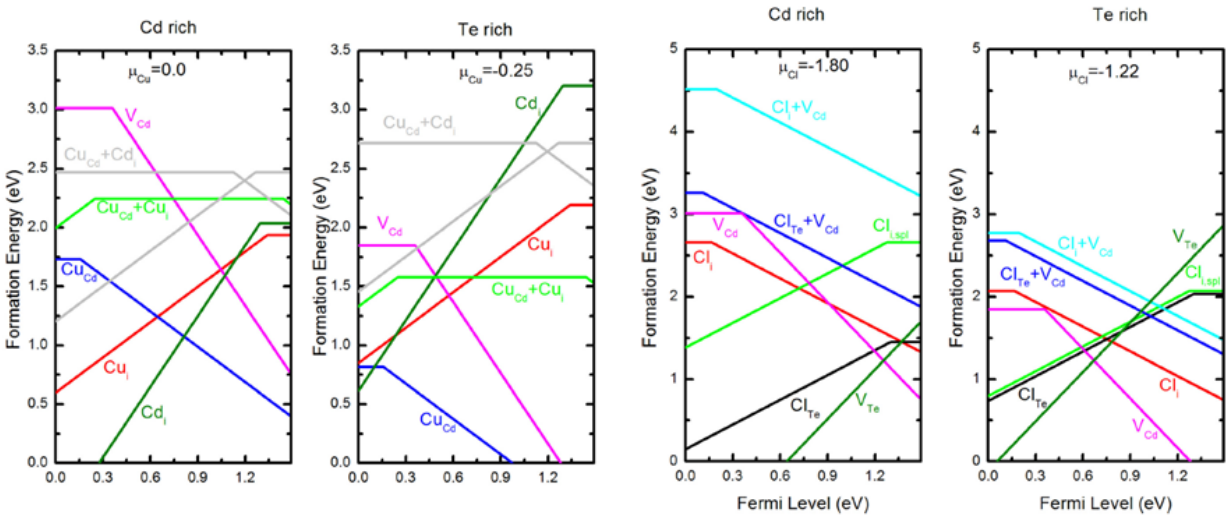

Figure 2.6 Formation energies of Cl and Cu related defects in CdTe

2.4.3 Antimony Doping

Antimony (Sb) (group V) can act as a p-type dopant in CdTe. Occupation of Sb at Te site forms stable substitutional acceptor defects Sb_{Te} and has a relatively low ionization energy of 0.28 eV [77]. The formation energy of V_{Te} is lower under Cd-rich deposition conditions, leading to the formation of Sb_{Te}.

$$Sb + V_{Te} = Sb_{Te} \qquad (2.3)$$

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This is beneficial to the electrical characteristics of CdTe films in two ways. First, conversion of the Cd-rich n-type CdTe to p-type by quenching V_{Te} (a shallow donor) with Sb_{Te} acceptors. Second, Cd-rich deposited films inhibit the formation of lifetime "killing" defects such as Te_{Cd} and Te_i. Based on first principle calculations, both high carrier concentration and high lifetime can be expected at the same time for Sb doped CdTe films. Sb has a low diffusion constant and can easily be incorporated into CdTe.

Colegrove *et al.* studied the antimony diffusion mechanism in single and polycrystalline CdTe [78]. SIMS measurements identified fast grain boundary (GB) diffusion along with a slow bulk diffusion component, suggesting that Sb doping via diffusion might leave the Sb localized around GBs. It was suggested based on first principle analysis that $(Sb_{Te})^-$ acceptor defect has an ionization energy of E_V + 0.23 eV. This $(Sb_{Te})^-$ defect can transition to another form, called the AX center $(Sb_{Te})^+$, a donor defect that could compensate p-type doping (Figure 2.7*).

Picos-Vcga *et al*. studied physical properties of CdTe-Sb thin films by RF sputtering [79]. They found that increase in Sb in the film decreased the Cd and Te content. For high concentration of Sb (around 10^{19} cm^{-3}) in CdTe, the CdTe became a semi-insulating material. At

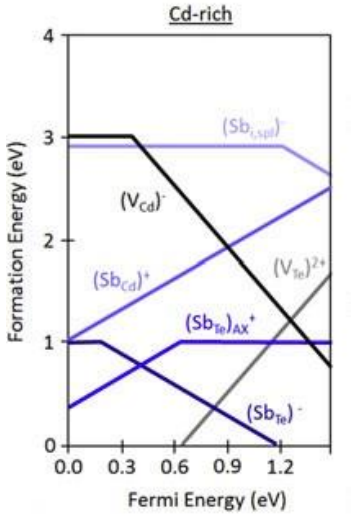

Figure 2.7 Formation energies of Sb related defects in Cd-rich deposition condition

* Reprinted with permission from [78]. Permission is included in Appendix B.

low concentration, the Sb preferred substituting Te as an acceptor. However, with the increase of Sb concentration, more Sb atoms substituted Cd and compensated the Sb_{Te} acceptors. Highly conductive Sb doped p-type CdTe film using photo assisted MBE process was reported by R. N. Bicknell *et al*. [80]. The hole concentration was $5x10^{16}$ cm^{-3} with a mobility of 40~45 cm^2/Vs. An argon laser was used to assist the chemical reaction. They hypothesized that the argon laser could provide the energy needed to overcome potential barriers at the growing film surface to increase dopant activation. J. D. Benson *et al.* observed enhanced Te-desorption using laser-illumination and produced more sites for Sb incorporation [81]. Complementary Auger studies indicated a 20% increase in Sb adsorption due to Sb filling both photons desorbed Te-sites and some equilibrium Te-site vacancies.

J. Santos-Cruz *et al*. studied the influence of the growth parameters of Sb doped CdTe with RF sputtering [82]. They found that, with low concentrations the structure is a mixture of zinc blend (ZB) and hexagonal wurtzite (W) phases. Sb atoms in the CdTe lattice favored the stable ZB Phase, and W is considered the metastable crystalline phase. The resistivity was $9x10^5$ Ω-cm with 10% of Sb at 100ºC, but less than 1% Sb was measured with SIMS. The resistivity decreased with increasing Sb concentration. Y. Hatanaka *et al*. attempted excimer laser assisted Sb doping by diffusion in crystalline CdTe [83]. The best doping characteristics reported are resistivity of 0.027 Ω-cm with a hole concentration $5X10^{18}$ cm^{-3}.

J. P. Nair *et al*. reported in situ Sb doping of polycrystalline CdTe with electrodeposition. PIXE data confirmed the presence of Sb in the film, however no doping data was presented [84]. Okamoto *et al*. investigated Sb doping of polycrystalline CdTe deposited by CSS [85]. Sb doped CdTe powder was used as the source, and improvement of solar cell performance was reported. SIMS data exhibited Sb incorporation up to 10^{16} cm^{-3}, and XRD measurement showed decrease in (111) preferential orientation. No doping data was presented. Zhao *et al.* also reported Sb doping on CSS deposited CdTe films; the incorporation process was diffusion and significant improvement in net doping concentration (up to 10^{16} cm^{-3}) was observed [77].

Sb incorporation under Te-rich conditions can lead to the formation of Sb_2Te_3, which can facilitate the formation of the back contact for CdTe solar cells, but does not contribute to p-type doping [86].

2.4.4 Phosphorus Doping

Phosphorous (P) is one of the most attractive dopant elements as it is theorized to create very shallow acceptor levels in CdTe. If P incorporation in CdTe can be enhanced through nonequilibrium processes, the doping concentration could be significantly improved. Occupation of P at Te site in CdTe forms stable substitutional acceptor defect P_{Te} and has a low ionization energy. The formation energy of V_{Te} is lower under Cd-rich deposition conditions, leading to the formation of P_{Te}.

$$P + V_{Te} = P_{Te} \qquad (2.4)$$

Su-Huai Wei *et al.* calculated (DFT calculations with HSE approximation) p-type dopant formation energies in CdTe [87] (Figure 2.8*). For both P and As dopants, p-type doping is self-compensated by the formation of AX centers. When P in the P_{Te} substitutional defect breaks its two bonds with Cd and moves towards the neighboring Te atom to form a P-Te bond, the resulting

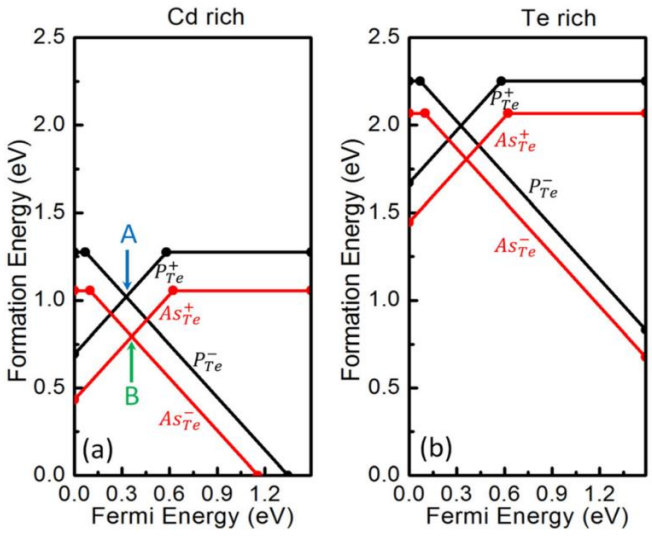

Figure 2.8 Formation energies of P_{Te} and As_{Te} as functions of Fermi levels

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defect is called an AX center which is a donor defect. Due to this, the fermi level would be pinned at point A or B in the figure. Based on first principle calculations, the authors suggested rapid cooling to avoid formation of these self-compensating defects. By cooling CdTe from a high growth temperature to room temperature under Te-poor conditions and choosing an optimal dopant concentration of about 10^{18} cm^{-3}, P and As doping could reach a hole density above 10^{17} cm^{-3} at room temperature and lower the Fermi level to within 0.1 eV above the VBM [87].

M. A. Flores *et al.*, provided a different explanation for the compensation mechanism in P doped CdTe [88]. Based on their DFT calculations with PBE (Perdew, Burke and Ernzerhof) approximation, AX centers are not stable enough to be the main compensating defect. Their model estimates that under Te-rich growth conditions the phosphorus interstitials (P_i^+) and under Cd-rich deposition condition complex defect $(P_{Te}\text{-}V_{Te})^+$ are the compensating defects limiting the p-type doping.

One of the earliest and comprehensive experimental study on P doping of CdTe was performed by Selim and Kröger, where P-doped CdTe crystals were used [89]. A phosphorus acceptor level of E_V + 0.035 eV was measured, and it was theorized to be P_i and/or P_{Te}. The authors suggested that at high phosphorus concentrations Cd_i would be the compensating defect.

The highest hole concentration to date is $5x10^{19}$ cm^{-3} and has been reported by H. L. Hwang *et al.* who used P+ implantation on single crystal CdTe with pulsed electron beam annealing for dopant activation [90]. Phosphorus atoms are often associated with native defects and form complexes and precipitates, such as Cd_3P_2, P_2Te_3. It might exist as P_i, P_{Te}, and P_{Cd} in CdTe. It is an acceptor when it occupies the interstitial site and surrounded by Cd atoms, or if it occupies Te site (P_{Te}). When P_i is surrounded by tellurium atoms, or occupies Cd site (P_{Cd}) it acts as a donor. The shallow acceptors P_{Te} are compensated by Cd_i at high cadmium pressure annealing, while at low cadmium pressure annealing, the shallow acceptors V_{Cd} are compensated by P_{Cd}. At high doping concentration, the neutral or charged complexes become dominant leading to a large degree of self-compensation.

A. D. Compaan *et al*. studied phosphorus doped CdTe films by reactive sputtering from $CdTe/Cd_3P_2$ [91]. They observed the effect of CdTe doping in improving solar cell device performance. A stability study showed that the uniformly doped CdTe:P device has the poorest stability due to the degradation in both J_{SC} and FF.

Recent studies of P doped single crystal CdTe have revealed attractive results in terms of V_{OC}, dopant concentration and carrier lifetime. Researchers at NREL and Washington State University have published several reports of successful P doping in single crystal CdTe [92, 93, 94]. Crystals were grown by a modified vertical Bridgman technique, with variable levels of P and excess Cd introduced into the source material. This approach has achieved for the first time 1V V_{OC} CdTe device [95]. Doping concentration of $1x10^{17}$ cm^{-3} with a minority carrier lifetime up to 400 ns has been achieved. Colegrove *et al.* studied P diffusion in single and poly- crystalline CdTe [96]. TOF-SIMS measurements identified fast grain boundary diffusion along with a slow bulk diffusion and a fast bulk diffusion component. The slow bulk diffusion process is theorized to be due to substitutional P through Te sites, whereas the fast bulk diffusion component was via interstitial sites.

Recently, B. McCandless et al. investigated P doping in vapor transport deposited polycrystalline CdTe and reported doping concentration up to 10^{15} cm^{-3} [97]. Dopant incorporation levels of 10^{17}-10^{18} cm^{-3} (doping activation efficiency 1.5%) with minority carrier lifetime of 1.5 ns was reported.

2.5 Objective of This Study

Although the efficiency of CdTe thin film devices has seen a tremendous boost in the last 16 years, more can be achieved considering its theoretical maximum (Shockley-Queisser limit for single junction device) of 33% for CdTe [98]. Progress over the last decade made it apparent that both short-circuit current (J_{SC}) and fill factor (FF) of the record cells are approaching their practical limits of 30 mA/cm^2 and 80% respectively [99]. The short circuit current (J_{SC}) of the present polycrystalline champion cell has exceeded the theoretical maximum for CdTe due to bandgap

grading [100]. However, the maximum attainable V_{OC} of the bandgap graded device is lower than that of CdTe, as the V_{OC} is determined by the layer with the smallest bandgap.

Considering the fact that the highest reported V_{OC} for CdS/CdTe solar cell is 1017 mV, which is about 100 mV higher than the maximum efficiency cell, further advances in cell efficiency will be achieved through improvement of the open-circuit voltage (V_{OC}) [99].

The V_{OC} of a solar cell is directly related to the carrier concentration and inversely related to the reverse saturation current of the device. The reverse saturation current is dependent upon the minority carrier lifetime. Hence, to improve V_{OC} both the doping concentration and carrier lifetime need to be simultaneously improved. Nevertheless, if the dopant can act as a recombination site, doping concentration and carrier lifetime can be inversely proportional at high doping situations. It is imperative to understand the defect chemistry in CdTe as a function of deposition stoichiometry, various post deposition treatments and dopant incorporation to further enhance the device performance.

CHAPTER 3: EXPERIMENTAL DETAILS

3.1 Elemental Vapor Transport Deposition System

The deposition of polycrystalline CdTe films by the Elemental Vapor Transport (EVT) process is one of the key features of this investigation. This process allows in situ control of vapor phase stoichiometry of elemental Cd and Te during CdTe growth, capable of manipulating native defect density and incorporation of extrinsic impurities. Figure 3.1 shows a schematic diagram of the system, along with a photo of the implemented system.

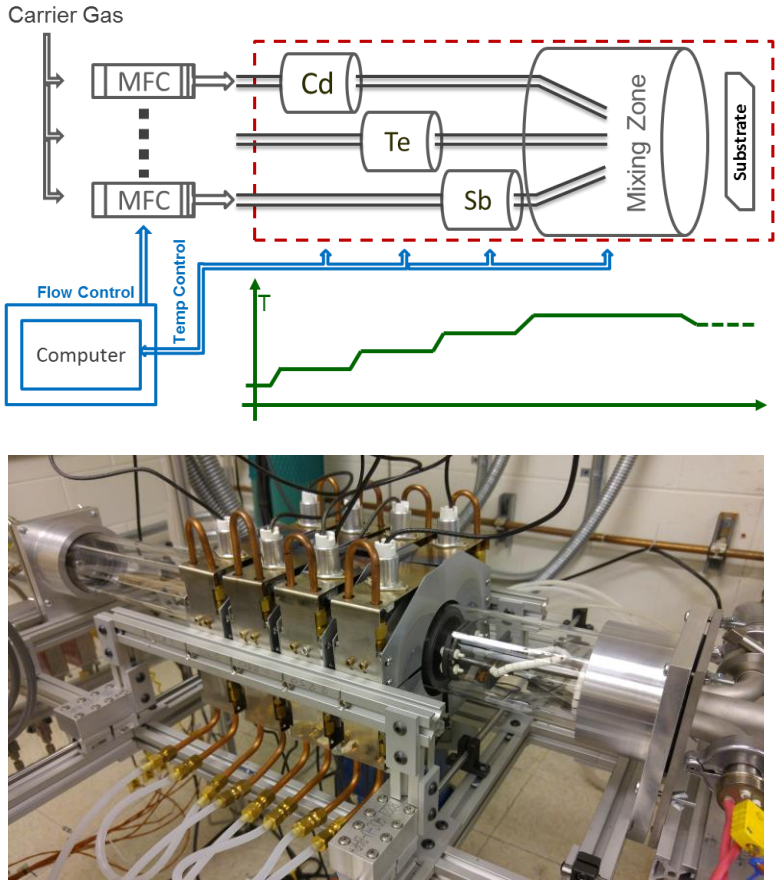

Figure 3.1 (Top) Schematic diagram and (bottom) implementation of the EVT Deposition Apparatus

The elemental sources were kept in separate heating zones made of high purity graphite. Each zone was equipped with 6kW halogen lamp heaters and a temperature controller. Separate mass flow controllers controlled the carrier gas (UHP He) flow rate individually through each elemental zone. The reactor setup allowed for specific control of the gas phase Cd/Te stoichiometry and dopant concentration by the adjustment of zone temperature and flow rate. Each elemental zone was loaded with 99.9999% purity Cd and Te metal sources. The generated vapors were carried forward through separate quartz tubes. After the last elemental zone, a cylindrical graphite tube served as a mixing zone, where the substrate was placed. To avoid vapor condensation before the substrate, the zones were placed in sequence of increasing temperature from the source to the deposition/mixing zone. For example, typical zone temperature for a stoichiometric vapor ratio deposition were – Cd zone 435 ºC, Te zone 535 ºC and mixing zone 720 ºC. The substrate holder was positioned at the edge of the mixing zone to attain a deposition temperature of 580-610 ºC. The substrate holder was also equipped with a borosilicate heater, used to preheat the substrate. The depositions were performed in a pressure range of 25-700 Torr. The pressure was controlled by a pressure regulated valve and a mechanical pump. The system parameters such as temperature, flowrate and pressure were controlled and monitored from a computer equipped with a LabVIEW program.

3.2 Cell Fabrication

CdTe solar cells were fabricated in the superstrate configuration. The baseline structure is glass/TCO/CdS/CdTe/Back contact (Figure 3.2). The various components of the cell fabrication steps are discussed in the following sections.

3.2.1 Glass Substrate

Corning Eagle XG, an alkaline earth boro-aluminosilicate glass (alkali-free), was used as the substrate due to its high optical transmittance (up to 90% in the wavelength range 350-2200 nm), mechanical strength and high temperature tolerance. The dimension of the substrates was

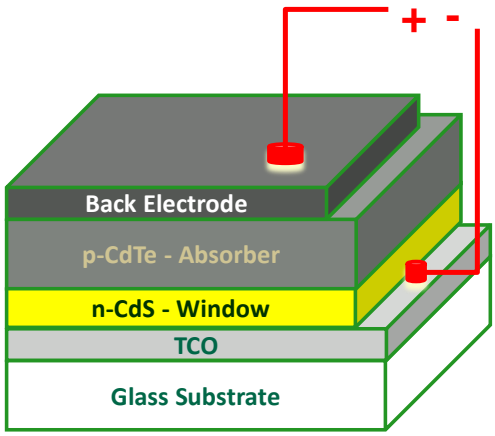

Figure 3.2 CdTe solar cell in superstrate configuration

1.45" x 1.32" with a thickness of 0.7 mm. The substrates were thoroughly cleaned under running de-ionized (DI) water following a very short etch in 10% HF solution.

3.2.2 Transparent Conductive Oxide (TCO)

A bilayer of indium tin oxide (ITO) and tin oxide (SnO_2) was used as the front contact of the CdTe photovoltaic devices. Both the layers were deposited by RF sputtering in a single system without breaking vacuum in ultra-high purity (UHP) Ar environment. The ITO was the conductive layer with a thickness of 3000 Å, deposited at 250 °C. The SnO_2 was used as the buffer layer having a thickness of 1000 Å. The resulting bilayer had a sheet resistance of approx. 8-10 Ω/□.

3.2.3 Cadmium Sulfide Window Layer

Cadmium Sulfide (CdS) as the window layer was used as the n-type layer to form the p-n heterojunction with p-type CdTe absorber. Due to the poor electrical properties of CdS, light absorbed in CdS layer does not convert to photocurrent. The CdS layer needs to be as thin as possible, while still thick enough to prevent the formation of pinholes. CdS, in this study, was deposited by the Chemical Bath Deposition (CBD) process on glass/TCO substrates. The process involves the formation of CdS from aqueous alkaline solution of Cd^{2+} and S^{2-} ions; the sources of the ions were cadmium acetate and thiourea respectively. Ammonium hydroxide (NH_4OH) and ammonium acetate (NH_4Ac) were the agents used to maintain solution pH balance and control the speed of reaction. The reaction was maintained at ~ 80 °C controlled using a temperature

bath, while the solution was stirred with a magnetic stirrer to ensure uniform deposition. The reaction steps are the following [101].

$NH_3 + HOH \leftrightarrow NH_4^+ + OH^-$

$Cd(CH_3COO)_2 \leftrightarrow Cd^{2+} + 2CH_3COO^-$

$Cd(NH_3)_4^{2+} + 2OH^- \leftrightarrow [Cd(OH)_2(NH_3)_2] + 2NH_3$

$[Cd(OH)_2(NH_3)_2SC(NH_2)_2] \rightarrow CdS_{(S)} + CN_3H_5 + NH_3 + 2HOH$

$[Cd(OH)_2(NH_3)_2] + SC(NH_2)_2 \rightarrow [Cd(OH)_2(NH_3)_2SC(NH_2)_2$

The reaction was carried out for a duration of 90 min to get an approximate thickness of 90 nm.

3.2.4 Cadmium Telluride Absorber Layer

CdTe in the absorber layer were deposited on glass/TCO/CdS substrates by the EVT outlined in section 3.1. The film thickness was in the range of 4-7 μm.

3.2.5 Cadmium Chloride Heat Treatment

$CdCl_2$ heat treatment (HT), a necessary step for fabricating high efficiency CdTe solar cells, was performed on most devices. In some devices the step was intentionally avoided to isolate its effect from the dopant incorporation. $CdCl_2$ was deposited by thermal evaporation on CdTe surface. The film stack was subsequently annealed under He and O_2. The annealing was performed at a temperature varied from 350 °C to 390 °C for 25 mins. After the annealing, the samples were ultra-sonicated in methanol to remove residual $CdCl_2$.

3.2.6 Back Contact

Prior to the back-contact formation, the CdTe films were lightly etched in a Br-methanol solution for 5 seconds. The films were sonicated afterwards in methanol to remove any residue. This chemical etch removes oxides that may have formed on the CdTe surface during $CdCl_2$ treatment annealing, and it provides a Te-rich p^+ layer on the surface. This layer facilitates back contact hole transfer from the CdTe layer due to tunneling.

Two different back contacts were employed in this study. Undoped (i.e. no intentional Cu added) graphite paste was used for Sb and P doped devices to isolate the effect of the dopants.

For intrinsically deposited devices both undoped and doped graphite paste were used for back contacts. The doped graphite contained Cu doped HgTe. After the back contact application, the devices were annealed in an inert ambient at 275 °C for 20 mins. Strips of indium were used around the devices to facilitate the front contact.

3.3 Characterization

3.3.1 Current-Voltage (JV) Measurement

The open circuit voltage (V_{OC}) and fill factor (FF) of the photovoltaic devices were extracted from Current-Voltage measurements. The measurements were performed inside a solar simulator with intensity calibrated to replicate AM 1.5 condition using a Si reference solar cell. A four-point probe setup to mitigate contact resistance was used with a Keithely 2410 Source meter and the current output was measured as the voltage bias was swept. The data was collected using a LabVIEW program, and the V_{OC} and FF of the devices were calculated.

3.3.2 Spectral Response (SR) Measurement

Spectral response measurements of the devices were performed using an Oriel monochromator (model 74100) to quantify the quantum efficiency (QE) and short circuit current density (J_{SC}) of the cells. The light source for the monochromator was a GE400W/120V Quartz line lamp, and its spectral output was calibrated using a Si reference cell. The current response of the reference and device were measured from 400 nm to 900 nm wavelength. The photon count at each wavelength was calculated from the reference cell response to quantify the QE (see section 1.5.2). The J_{SC} was calculated by integrating the current response using the AM 1.5 spectrum.

3.3.3 Capacitance-Voltage (CV) Measurement

The net doping of the devices was estimated from capacitance-voltage measurements. The measurements were carried out using a HP 4194A Impedance Analyzer at 10 kHz or 50 kHz frequency with -2 to +0.5 V bias sweep operated from a LabVIEW program. Prior to the CV measurements, the capacitance vs. frequency response of the devices was measured for each

cell to ensure that there were no significant frequency dispersions present due to deep states and interface states. At high frequencies, CV measurements are affected by external circuit inductance [102]. The measurement frequency was chosen to mitigate both these effects. Net doping vs. distance from junction plot was obtained from the CV data, and the net doping value corresponding to the 0 V bias voltage was used for comparison among devices.

3.3.4 Minority Carrier Lifetime Measurement (TRPL)

Minority carrier lifetimes were measured at National Renewable Energy Laboratory (NREL) facilities with single photon excitation (1PE) Time-Resolved Photoluminescence (TRPL) technique. The carriers were excited from the substrate side through the CdS window layer using a 650 nm excitation laser beam and the resultant photon emission was captured at 840 nm detection wavelength.

3.3.5 Deep Level Transient Spectroscopy (DLTS)

A Sula Technologies Deep Level Spectrometer (Model DDS-12) was employed to analyze the defect distribution of the devices. The sample temperature was varied from 80K to 320K using liquid N_2 and heater inside a Janis VPF-100 cryostat. For DLTS measurements, small size CdS/CdTe devices with ~1.5 mm X ~1.5 mm area were fabricated due to the capacitance limit of the DLTS instrument and to reduce contact effects. The devices were screened based on dark JV and CV measurements; the reverse bias leakage current in the dark needed to be less than 100 µA. Temperature sweep above room temperature was avoided in most cases, as it caused permanent change to the defect structure. A bias pulse of -1V to 0V with a pulse width of 1ms was used for the measurements. The capacitance transients due to carrier injection were analyzed with 6 different rate windows from 0.02 to 1 ms. The resultant spectra were analyzed to attain information on trap concentration, activation energy and capture cross section.

3.3.6 Morphology Analysis

The focus of this study was mainly electrical properties of the CdTe thin films. However, structural properties of select films were analyzed employing Scanning Electron Microscopy (SEM) and X-Ray Diffraction (XRD) to obtain additional information. SEM was performed using a Hitachi S800 system with an accelerating voltage of 25 KV. The crystallographic properties of the films were analyzed using a Panalytical X'pert Pro with a Copper kα source. Film thicknesses were measured on a Dektak 3030ST α-step profilometer.

CHAPTER 4: BASELINE CDTE DEVICES*

4.1 Introduction

The objective of this study is to investigate the effect of CdTe deposition stoichiometry in determining the point defect distribution, and thus create favorable conditions for effective extrinsic dopant incorporation. This chapter is divided into two sections. The first section deals with modeling the typical thin film CdTe solar cell structure and understanding the effect of carrier concentration and minority carrier lifetime in determining the photovoltaic performance of CdTe solar cells. The second section describes the baseline EVT CdTe thin film properties, device performance and defect distribution as a function of deposition stoichiometry and post deposition treatments.

4.2 CdTe Device Modeling

The effect of doping concentration and minority carrier lifetime on CdTe solar cells were simulated using the wxAMPS solar simulation tool [103], an updated implementation of the solar cell simulation software AMPS [104]. The baseline device structure was obtained from the material properties outlined in the literature [105]. In order to simulate a practical device, a CdS_xT_{1-x} intermixed layer with thickness of 0.1 μm and a bandgap of 1.41 eV was introduced between the n- type CdS and p- type CdTe layer. A midgap defect with concentrations 10^{13}-13^{15} cm^{-3} was introduced as a means to vary the minority carrier lifetime. Figure 4.1 shows the simulation results. Legends in the graphs are p-type net doping concentrations in cm^{-3}. With increasing doping concentration and carrier lifetime, the V_{OC} increases. Typical doping levels in polycrystalline CdTe solar cells at present are on the order of 10^{14} cm^{-3}. Therefore, significant

* A portion of this chapter was previously published in [75]. Permission is included in Appendix B.

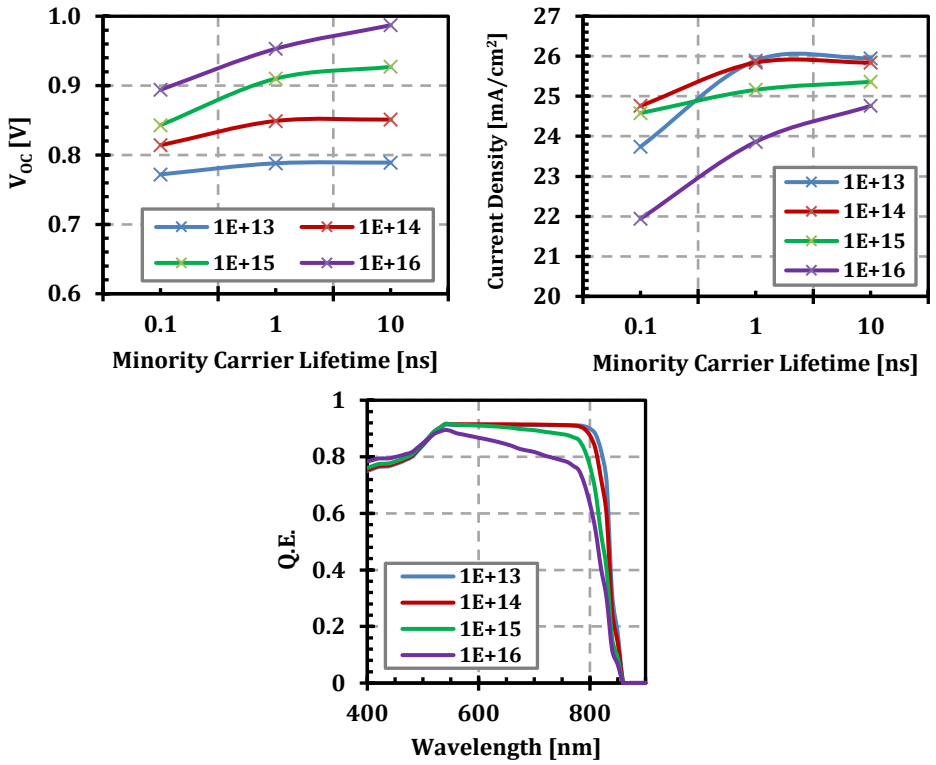

Figure 4.1 wxAMPS simulation showing the effect of doping conc. and minority carrier lifetime in the CdTe device performance

increases in V_{OC} can be achieved by the increasing the doping concentration, however, with the tradeoff of reduced J_{SC}. At increased doping concentrations the lifetime becomes considerably more important, as V_{OC} becomes more minority carrier lifetime dependent. With the increase in doping concentration, the carrier collection at longer wavelengths decreases resulting in lower total current output from the cell (J_{SC}). The low doping concentrations in typical CdTe cells, results in an extended space charge region in the CdTe region [106]. The width of the space charge region decreases with increased p-doping CdTe. Long wavelength photons are absorbed deeper in the CdTe, and the collection for the photo-generated charge carrier becomes diffusion dominated. This results in reduced quantum efficiency at long wavelengths. These simulations corroborate the importance of improving the minority carrier lifetime of the CdTe layer along with the doping concentration to improve the efficiency of CdTe solar cells.

4.3 EVT CdTe Depositions

The Elemental Vapor Transport (EVT) process was used to deposit CdTe with different vapor phase stoichiometry from elemental sources of Cd and Te. Cd and Te vapors were generated by heating the elements above their melting point temperatures, 321.11 ºC and 449.57 ºC respectively [107]. The lower vapor pressure of CdTe compared to that of Cd and Te, enables the vapors to condense at the substrate to deposit solid polycrystalline CdTe. Cd-rich, Te-rich and stoichiometric CdTe films were deposited using vapor phase Cd/Te ratios >1.0, <1.0 and 1.0 respectively. The vapor ratio was varied by adjusting the elemental zone temperature while holding the carrier gas flow rate constant. The actual stoichiometry change in the CdTe films is expected to be very small in comparison to the gas phase Cd/Te ratio, due to the single-phase homogeneity limit for CdTe growth (details in section 2.3). Such small variation in the elemental composition is below the resolution limit of most composition analysis tools, making it difficult to quantify the film stoichiometry. However, the effect of the change in deposition stoichiometry on the electrical properties of the films can be an indirect measure of stoichiometry. Unless otherwise mentioned, the term Cd/Te ratio will be used throughout this document to indicate the vapor phase Cd/Te ratio during the deposition.

4.4 Vapor Phase Ratio / Stoichiometry

The vapor phase Cd/Te ratio or the deposition stoichiometry depends on the vapor pressure of Cd and Te and the flowrates through the Cd and Te zones. The vapor pressures of Cd and Te as a function of temperature are given by the following equations [107].

$$\mathrm{P_{Cd}(torr)} = 10^{7.66023 - \frac{4757.62}{\mathrm{T_{Cd}} + 228.438}} \quad (4.1)$$

$$\mathrm{P_{Te}(torr)} = 10^{6.6385 - \frac{4084.38}{\mathrm{T_{Te}} + 98.94}} \quad (4.2)$$

The mass transport was calculated by the ideal gas law where the effective volume is proportional to the carrier gas flow rate. The calculated vapor ratios were verified by performing calibration experiments. The deposition was run at typical experiment conditions for certain vapor ratios for

60 minutes and the weight loss on the elemental sources were measured by weighing the source material before and after depositions. Table 4.1 shows the typical experimental conditions used for EVT CdTe deposition at different Cd/Te ratios and the ratio calculated from the calibration runs. The ratio of evaporated mass was found to be within ±0.12 of the calculated ratio, and thus in good agreement with the calculations. The carrier gas flow rate for the elemental zone was kept equal, to have the vapor ratio to be only dependent on zone temperature.

Table 4.1 Calibration runs for vapor phase ratio verification

Cd/Te vapor ratio (Calculated)	Cd Zone Temperature (ºC)	Te Zone Temperature (ºC)	Cd & Te Zone Flow rate (cc/min)	Cd/Te ratio (Measured)
0.5	435	568	400	0.45
0.7	435	551	400	0.69
1.0	435	535	400	1.06
2.0	470	535	400	2.12

4.5 Deposition Pressure Dependence

At the early stages of the project the depositions were performed at near atmospheric pressure (AP) of 700 Torr. In order to increase the deposition rate, the depositions were carried out at lower pressures during the latter stages of the project. A near 600% increase in the deposition rate was observed for the deposition pressure of 25 Torr. The deposition time was

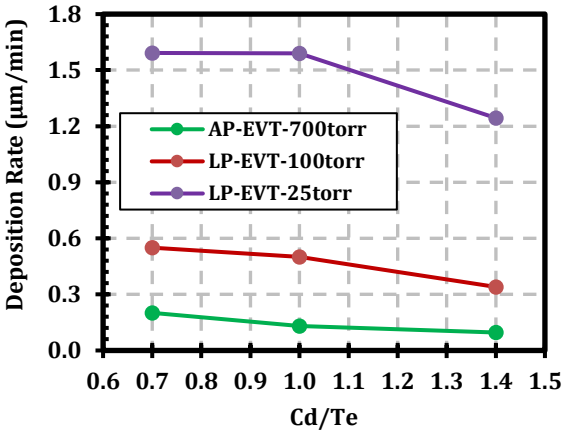

Figure 4.2 Effect of base pressure on the deposition rate at different ratio

reduced to 5 mins compared to 40-60 mins depositions at near atmospheric pressure conditions. Increased deposition rate at Te-rich deposition conditions for all pressure conditions indicate that Te species may have better adsorption on the substrate surface facilitating the nucleation for faster growth of the films.

Table 4.2 Stoichiometric vapor deposition parameters at various pressures

System Pressure	Cd Zone Temperature (ºC)	Te Zone Temperature (ºC)	Mixing Zone Flow Rate (liter/min)	Cd & Te Zone Flow rate (cc/min)	Deposition time (minute)	Stoichiometric deposition rate (µm/min)
700	435	535	2.0	400	40	0.13
100	421	520	0.8	100	12	0.50
25	421	520	0.8	100	5	1.59

Low pressure depositions also improved the film thickness uniformity across the sample. Figure 4.3 shows the thickness profile comparison for EVT deposited CdTe sample with ratio 1.0 for base pressure of 700 Torr and 25 Torr. If the thickness numbers are normalized by the average thickness, for AP deposition a standard deviation of 0.35 is observed. For LP depositions the film is more uniform with a 0.24 standard deviation.

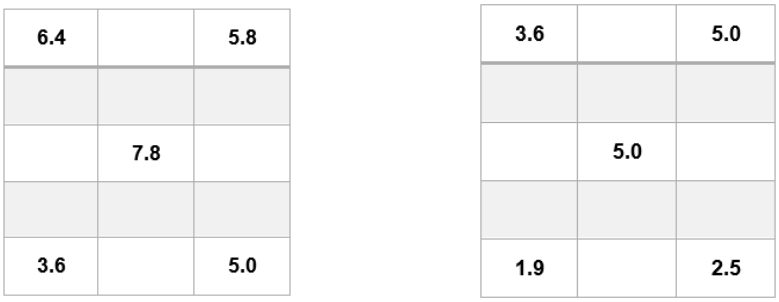

Figure 4.3 Thickness profile for EVT deposited CdTe film on a 1.3” x 1.45” substrate. (Left) Deposition at 700 Torr, Ratio 1.0, 40 min. (Right) Deposition at 25 Torr, Ratio 1.0, 5 min.

4.6 Baseline CdTe Device Performance

To investigate the effect of deposition stoichiometry on device performance, CdTe films were deposited under excess Te (Cd/Te vapor ratio 0.7), stoichiometric (ratio 1.0) and excess Cd (ratio 1.4) vapor conditions on TCO/CdS substrates. All samples were $CdCl_2$ heat-treated under the baseline conditions outlined in the experimental section. Graphite ink (no intentional Cu) was

used as the back-contact electrode for the samples without Cu doping. For Cu doped devices the back contact was Cu doped graphite ink.

Photovoltaic device performance of the CdS/CdTe cells is shown in Fig. 4.4. Devices with CdTe deposited under excess Te vapor conditions (Cd/Te ratio 0.7) exhibited superior performance with 10~20 mV higher V_{OC}. Net carrier concentrations obtained from capacitance-voltage measurements (Figure 4.4 right) indicate that the improved performance is partly due to higher doping [77]. It is speculated that the higher doping is due to increased cadmium vacancy (V_{Cd}) concentration as a result of the Te-rich deposition conditions [108]. A doping concentration on the order of 10^{15} cm^{-3} is observed for Te-rich deposited samples. Inclusion of Cu in the back contact improved the doping concentration (see Table 4.3), along with device performance (Figure 4.7). Copper forms substitutional acceptor Cu_{Cd}, which is favorable under Te-rich deposition conditions and have a lower ionization energy compared to V_{Cd}. Since Cu_{Cd} is a shallower acceptor compared to V_{Cd}, Cu doping improves carrier concentration in CdTe.

Besides device performance and doping concentration, deposition stoichiometry also affects the minority carrier lifetime. The minority carrier lifetime of as-deposited films (without any post deposition treatment) at all different Cd/Te ratio were very poor and below the detection limit of the TRPL instrument. When $CdCl_2$ treated, the Te-rich deposited devices exhibited better

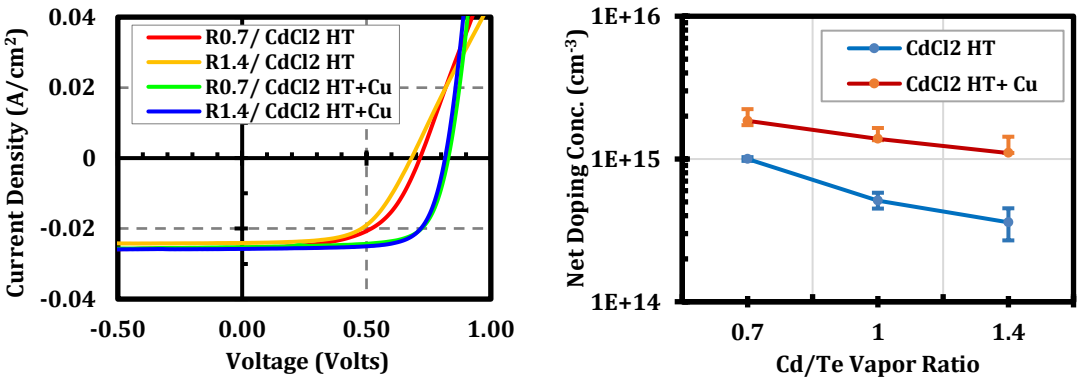

Figure 4.4 (Left) JV data and (right) net doping conc. different Cd/Te vapor ratios and post deposition treatments. Doping data is extracted from Capacitance-Voltage measurements.

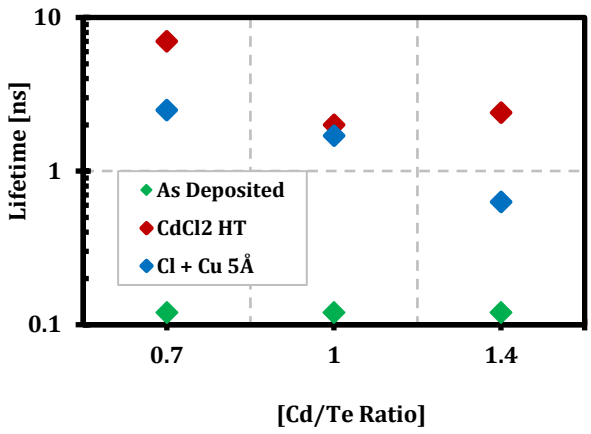

Figure 4.5 Minority carrier lifetime for CdTe with different Cd/Te ratios

carrier lifetimes (Figure 4.5). This signifies the lifetime improvement properties of the $CdCl_2$ HT in pX CdTe. The trend remained the same after a Cu dose of 5Å was used for the formation of the back contact; however, the lifetime values at all ratios decreased significantly [75]. This observation of lifetime variation is discussed in the next section along with DLTS data.

4.7 Defects in Baseline CdTe Devices

The effect of deposition stoichiometry and post-deposition treatment in manipulating the defect chemistry in polycrystalline CdTe was investigated using Deep Level Transient Spectroscopy (DLTS). Figure 4.6 shows DLTS spectra for $CdCl_2$ HT CdTe devices with different vapor phase deposition stoichiometry. For the excess Te deposited (Cd/Te ratio 0.7) device two distinct peaks were observed - a positive peak E1 at 150-250K indicating a minority carrier trap

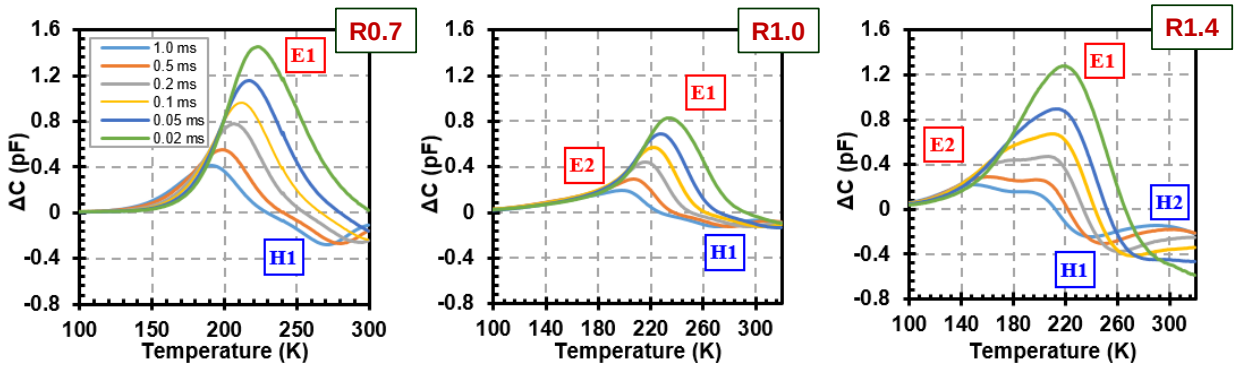

Figure 4.6 DLTS spectra from CdS/CdTe heterojunction with $CdCl_2$ HT. Cd/Te deposition ratio 0.7 (left), 1.0 (center) and 1.4 (right)

and a negative peak H1 at 250K to room temperature (RT) indicating a majority carrier trap. Both peaks E1 and H1 were also observed in stoichiometric and Cd-rich deposited films. A second positive peak (E2) at 100~180K indicated a shallower minority carrier trap, which became more prominent with increasing Cd/Te vapor ratio. For the ratio 1.4 device, ΔC continued to become increasingly more negative at higher temperatures suggesting the presence of a deep majority carrier trap (H2).

The DLTS spectra for the devices with Cu doped back contact exhibited significant differences (Figure 4.7). Peak E1 was no longer present and a shallower electron trap was observed for all devices regardless of stoichiometry. Based on its shape and temperature range, it was speculated to be the same minority trap E2 that appeared in Cd-rich deposited device without Cu (Figure 4.6 right). A small negative peak at 120~140K indicated the presence of a shallow hole trap with low concentration for Cd-rich deposited film with Cu (H3). Defect properties of H3 could not be resolved due to the low intensity of this peak. For all Cu doped devices ΔC continued to larger negative values at high temperatures (>300K) suggesting the presence of a deeper majority carrier trap (labeled as H2 in the figures).

The activation energy of H1 was calculated to be ~0.4 eV and was tentatively assigned to V_{Cd} [41]. This assignment was further corroborated by the observation that the peak disappeared in Cu doped samples, since Cu could occupy a cadmium vacancy in CdTe to form the acceptor defect Cu_{Cd} and therefore reduce or eliminate the concentration of V_{Cd} [109]. The electron trap E1 was previously observed on CSS deposited CdTe devices with and without Cl treatment [71], and it is speculated to be a native CdTe defect. The calculated activation energy of 0.4~0.5 eV suggests that it is either Cd_i or Te_{Cd} [40].

The activation energy of E2 in devices deposited under stoichiometric and excess Cd conditions could not be calculated due to its proximity to E1. However, in Cu doped devices, the activation energy of the same was calculated to be 0.22~0.3 eV. Activation energy value calculated in Cu-doped Cd-rich deposited device was likely to be affected by the proximity of H3,

hence 0.22~0.24 eV is a more accurate transition energy approximation for E2. Considering all the samples in this study are $CdCl_2$ heat treated, this defect is possibly related to Cl. Theoretical analysis anticipates Cl to occupy a Te site in CdTe, and its formation is favorable under Cd-rich deposition conditions. Cl_{Te} is a shallow donor defect with an activation energy of 0.19 eV. Interstitial Cl (Cl_i) also can be a donor with activation energy 0.22 eV. Cl_{Te} can form a complex shallow acceptor (E_V + 0.11 eV) defect (A-centers, V_{Cd}-Cl_{Te}) in conjunction with a cadmium vacancy [110]. The formation of A-centers is dependent upon the availability of V_{Cd}'s. The formation energy of Cu and Cl related defects in CdTe, based on first-principle calculations by Wei *et al.*, are the following [39].

$$Cu_i + V_{Cd} \rightarrow Cu_{Cd} \qquad \Delta H = -3.55eV \qquad (4.3)$$

$$Cl_{Te} + V_{Cd} \rightarrow V_{Cd}\text{-}Cl_{Te} \qquad \Delta H = -2.02eV \qquad (4.4)$$

$$Cu_i + V_{Cd}\text{-}Cl_{Te} \rightarrow Cu_{Cd} + Cl_{Te} \qquad \Delta H = -1.56eV \qquad (4.5)$$

Negative energy of reaction indicates energetically favorable and exothermic reaction. A lower concentration of V_{Cd} is expected in Cd-rich deposited films. Cl_{Te} donor defects might not encounter an adequate amount of V_{Cd} to form A-centers, and remained as Cl_{Te}. If the V_{Cd}'s are all consumed, A-centers have higher formation energy than Cl_{Te}. When Cu is introduced in Cl treated films, it can occupy a cadmium vacancy site, or take the V_{Cd} site in an A-center. The former scenario is more favorable. However, when all the V_{Cd} sites are filled, Cu can occupy the A-

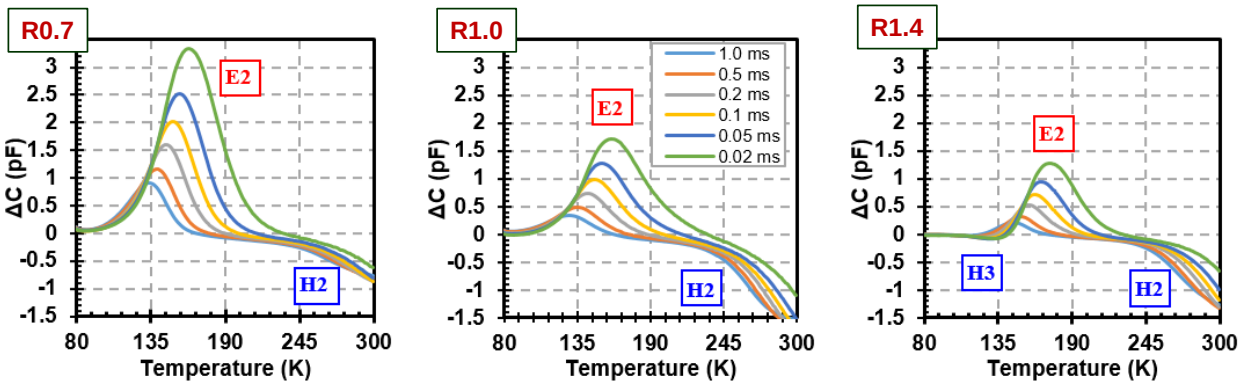

Figure 4.7 DLTS spectra from CdS/CdTe heterojunction with $CdCl_2$ HT and Cu. Cd/Te deposition ratio 0.7 (left), 1.0 (center) and 1.4 (right).

centers. In such case, Cl_{Te} part of A-centers can emerge as Cl_{Te} donors. The following two observations support this hypothesis - E2 appeared in all Cu doped devices, and in Cu-free devices, it became more prominent as the films were grown in more Cd-rich conditions. This relatively shallow minority carrier defect with concentrations in the order of up to 10^{14} cm^{-3} possibly had a compensating effect in limiting the doping efficiency of Cu doped polycrystalline CdTe. Thus, based on the above observations, E2 is likely a Cl related defect, possibly Cl_{Te} or Cl_i.

Negative ΔC for all Cu doped devices at high temperatures (>300K) indicates the presence of a majority carrier tap H2 and is possibly a Cu related deep defect. Similar characteristics were also observed for CSS deposited Cu doped devices [71]. The presence of a deep defect in Cd-rich Cu free devices, also denoted as H2, may or may not be the same defect that was observed in Cu doped samples. The presence of deep defects in Cd-rich deposited film was consistent with the minority carrier lifetime measurement on Cl treated Cd-rich samples (Figure 4.5). For samples with $CdCl_2$ HT, Te-rich deposited films demonstrated higher lifetime (7 ns) compared to Cd-rich deposited films (2 ns), consistent with the presence of H2 in Cu-free Cd-rich deposited device. For polycrystalline CdTe films, the grain boundaries (GB) play a significant role in determining the carrier lifetime. Cl incorporation is expected to passivate the GB related deep states in CdTe. First principle studies suggest that Cl passivation is more effective for Te-core GB compared to Cd-core [111]. Hence, H2 in Cd-rich deposited Cu free device could be related to un-passivated Cd-core grain boundary states (possible SRH recombination center). The presence of H2 in both Cu-doped and Cu-free devices are found to be correlated to the minority carrier lifetime of the devices.

Table 4.3 lists the different traps that were identified in different samples along with their trap concentration and activation energy. The terms ‘N/Q’ used for some cases indicate the presence of the peak, that could not be quantified due to either low intensity or proximity to other peaks.

Table 4.3 Trap conc. and activation energy from DLTS measurements

Cd/Te Vapor Ratio	Post-deposition Treatment	Doping Concentration (cm^{-3})	E1		E2		H1	
			Activation Energy (eV)	Trap Conc. (cm^{-3})	Activation Energy (eV)	Trap Conc. (cm^{-3})	Activation Energy (eV)	Trap Conc. (cm^{-3})
0.7	$CdCl_2$	1.0E15	0.47	8E13			0.42	1E13
1.0		5.1E14	0.5	2E13			0.41	4E12
1.4		3.6E14	N/Q	N/Q	N/Q	N/Q	0.38	1E13
0.7	$CdCl_2$ + Cu	1.9E15			0.24	1E14		
1.0		1.4E15			0.22	5E13		
1.4		1.1E15			0.31	3E13		

4.8 Summary of Chapter 4

The effect of Cd/Te deposition ratio on the electrical properties of polycrystalline CdTe was studied. Direct correlation to doping concentration and minority carrier lifetime was observed with vapor phase stoichiometry. Te-rich deposition conditions were found to be favorable in both aspects. Carrier lifetime up to 7 ns was observed for Te-rich deposition conditions with $CdCl_2$ heat treatment. However, incorporation of Cu was found to reduce the minority carrier lifetime.

The defect structure of EVT deposited polycrystalline CdTe with $CdCl_2$ treatment and Cu doping was investigated with Deep Level Transient Spectroscopy. Majority and minority carrier traps with different activation energies were identified. These traps were assigned to various native and extrinsic CdTe defects based on their activation energy and presence in specific devices. Cl related shallow minority trap in Cl and Cu treated devices indicated a possible dopant compensation mechanism. Lower minority carrier lifetime for Cd-rich deposited device with $CdCl_2$ HT was found to be due to deep majority carrier defects. This study provides a useful insight to the defect distribution of CdTe devices at different deposition stoichiometry, and how they are influenced by post deposition treatments such as $CdCl_2$ HT and Cu doping.

CHAPTER 5: ANTIMONY DOPING OF CDTE*

5.1 In Situ Sb Doping

Antimony (Sb), a group V element, can be a p-type dopant in CdTe. When it occupies Te sites, it forms Sb_{Te} an acceptor defect (Section 2.4.3). Sb as an extrinsic dopant was investigated by in-situ incorporation in CdTe [112].

5.2 Vapor Phase Sb Dose

The source of antimony vapor was elemental Sb with 99.9999% purity. Vapor phase Sb concentration was calculated using the ideal gas law; the Sb vapor pressure as a function of temperature was obtained from literature [113]. Vapor phase Sb concentration in parts per million (ppm) was calculated as the ratio of Sb vapor concentration, and either Cd or Te vapor concentration for a stoichiometric Cd/Te vapor ratio deposition. The samples are described in terms of the vapor phase Cd/Te ratio and Sb concentration – i.e. a sample/device identification of '3.0/125k' signifies a gas phase Cd/Te vapor ratio of 3.0 with a gas phase Sb concentration of 125k ppm.

Various gas phase deposition conditions with different Sb concentrations were used to deposit CdTe films on glass substrates and glass/TCO/CdS substrates. The depositions were performed under near-atmospheric pressure of 700 Torr with 1.5 to 2 liter/min flow of UHP He as the main carrier gas. The gas phase stoichiometry was varied by controlling the Cd and Te zone temperatures. The vapor phase Sb concentration was varied by a combined manipulation of dopant zone temperature and gas flow rate. The experimental parameters that were used to achieve different vapor phase Sb concentration during deposition are listed in Table 5.1.

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* A portion of this chapter was previously published in [112]. Permission is included in Appendix B.

Table 5.1 Experimental conditions for different Sb vapor concentrations

Vapor Phase Sb Conc. (ppm)	Dopant Zone Temperature (ºC)	Dopant Zone Carrier Flow rate (cc/min)
8	455	10
60	500	10
160	523	10
280	520	20
600	560	10
3000	588	20
16k	650	20
32k	700	20
125k	660	250
250k	660	500

5.3 Structural Analysis

X-Ray Diffraction analysis of the Sb doped CdTe films with up to 125k ppm Sb exhibited only cubic CdTe peaks with a (111) preferential orientation (Figure 5.1). Peaks at 23.75°, 39.29°, 46.43°, 56.82° and 76.56° correspond to (111), (220), (311), (422) and (511) planes respectively of the zinc blend structure cubic CdTe (ICCD Ref. 015-0770). With increasing Cd/Te ratio the intensity of (220) and (311) peaks increased. This lower degree of preferential orientation for higher Cd/Te ratio films was observed for intrinsically deposited CdTe also [114].

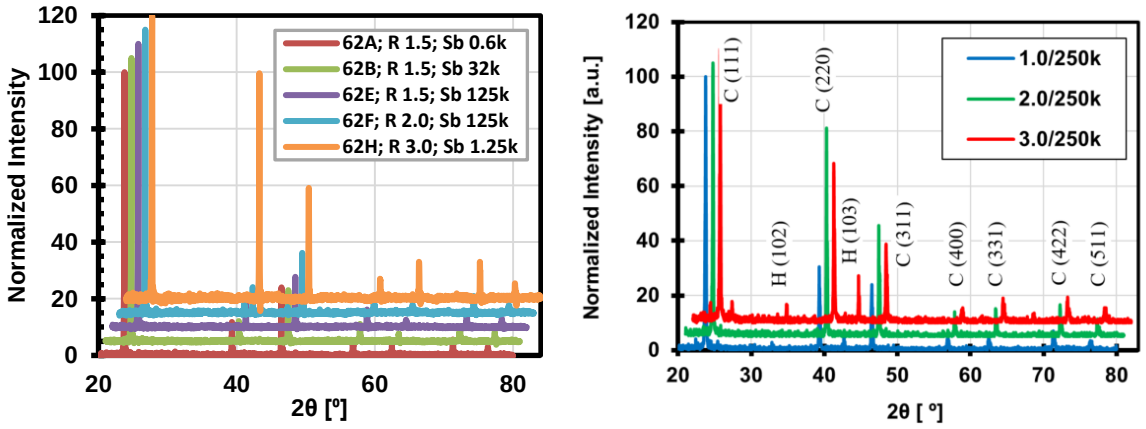

Figure 5.1 XRD spectra of EVT CdTe with different gas phase stoichiometry and Sb concentration. Hexagonal CdTe is observed. C and H indicate cubic and hexagonal structure respectively.

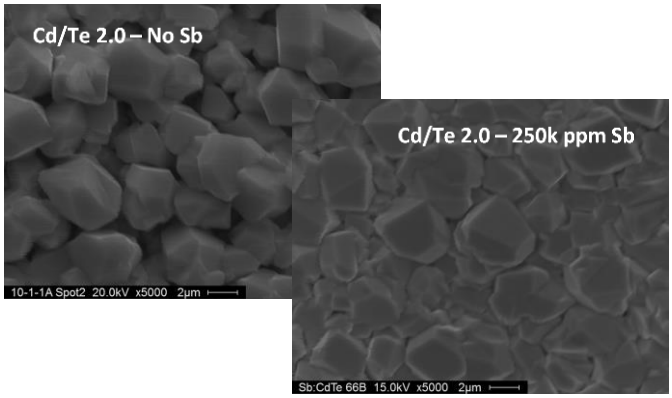

Figure 5.2 SEM images of high Cd/Te vapor ratio EVT CdTe. Improved grain structure is observed due to Sb incorporation.

However, for films with 250k ppm Sb additional peaks at 25.3º, 32.7º and 42.7º were observed. These peaks were consistent with wurtzite (hexagonal) CdTe (ICCD Ref. 019-0193) [115], and became more prominent at high Cd/Te ratios. These peaks were not observed in films with low concentration of Sb at any ratio. It should be noted that no secondary phase formation due to antimony compounds (e.g. metallic Sb or Sb_2Te_3) were observed. The hexagonal CdTe peaks were not present for intrinsic EVT CdTe without Sb and were a function of Cd/Te ratio for Sb doped samples. These observations suggested that hexagonal CdTe formation was a combined effect of both the high Sb vapor concentration and the higher Cd/Te ratio. Sb incorporation also appeared to improve the grain structure of the films. Intrinsic high Cd/Te vapor ratio depositions resulted in loosely connected smaller grains, shown in the SEM image (Figure 5.2), whereas Sb deposited films were more uniform with improved grain structure. Results on intrinsically deposited films suggested that Te sites facilitated the nucleation sites formation during vapor transport deposition [114]. Cd-rich deposition conditions are expected to enable Sb incorporation in the films. Adsorption of Sb species on the deposition surface possibly provided additional nucleation sites leading to the wurtzite crystal structure of CdTe.

5.4 Dopant Incorporation

Incorporation of Sb in the films is the first challenge for doping. In order for Group V elements (such as Sb) to contribute to p-type doping by occupying Te sites, it is necessary to

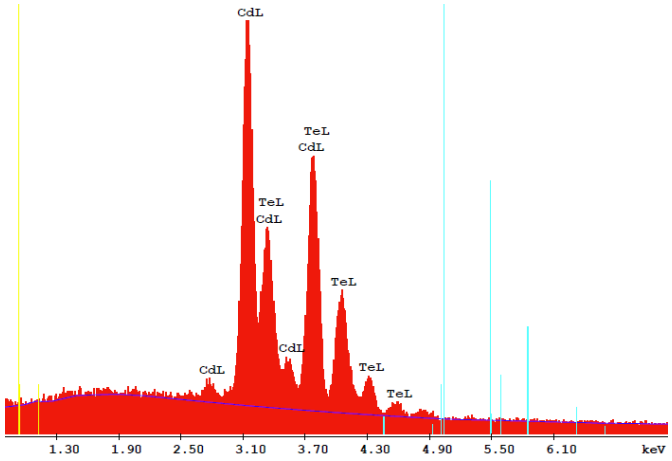

Figure 5.3 EDS measurement on CdTe film deposited with vapor phase Cd/Te ratio 2.0 and 250k ppm Sb

create Te-vacancies; hence Cd-rich deposition conditions are required. No Sb was detected with Energy Dispersive X-ray Spectroscopy (EDS) measurements within the detection limit (~1%) of the EDS device. No amount of Sb was detected, even for the highest vapor phase Sb film (Figure 5.3); 250k ppm Sb concentration corresponds to nearly 25% of the Cd or Te vapor phase atoms.

The presence of Sb in the films was confirmed by SIMS measurements, suggesting Sb incorporation only at the impurity concentration level. Figure 5.4 illustrates the maximum and minimum of measured Sb concentration in the films at various deposition conditions. The data verifies that Sb was indeed incorporated in the films with a high concentration, however with no significant correlation to the Cd/Te ratio. For 8 ppm and 160 ppm films Sb concentration was on the order of 10^{17} cm^{-3}. For higher Sb vapor content (125k and 250k ppm), the concentration was increased by nearly an order of magnitude to above 10^{18} atoms cm^{-3}. SIMS measurements were performed in collaboration with the National Renewable Energy Laboratory (NREL). The calculated vapor phase concentrations of Sb for most of the experiments described in this work was in the range of 10^{20}~10^{22} cm^{-3}. This implies poor incorporation efficiency of antimony in CdTe. Sb concentration in the film is 2 to 4 orders of magnitude lower in comparison to gas phase quantity. Sb exists mostly as Sb_4 molecules in the vapor phase [116], which is possibly the reason for low incorporation.

5.5 Net Doping Concentration

Capacitance-Voltage (CV) measurements on CdS/CdTe (Sb doped) devices are shown in Figure 5.5. The data indicates that for the same Sb vapor content, the carrier concentration exhibited an increasing trend with higher Cd/Te ratio. The trend was observed for both low and high Sb vapor concentrations. This is consistent with the fact that, the formation energy of V_{Te} decreases for higher Cd/Te ratio [39] and Sb incorporation contributes to the net hole concentration by occupying a Te site, forming Sb_{Te}.

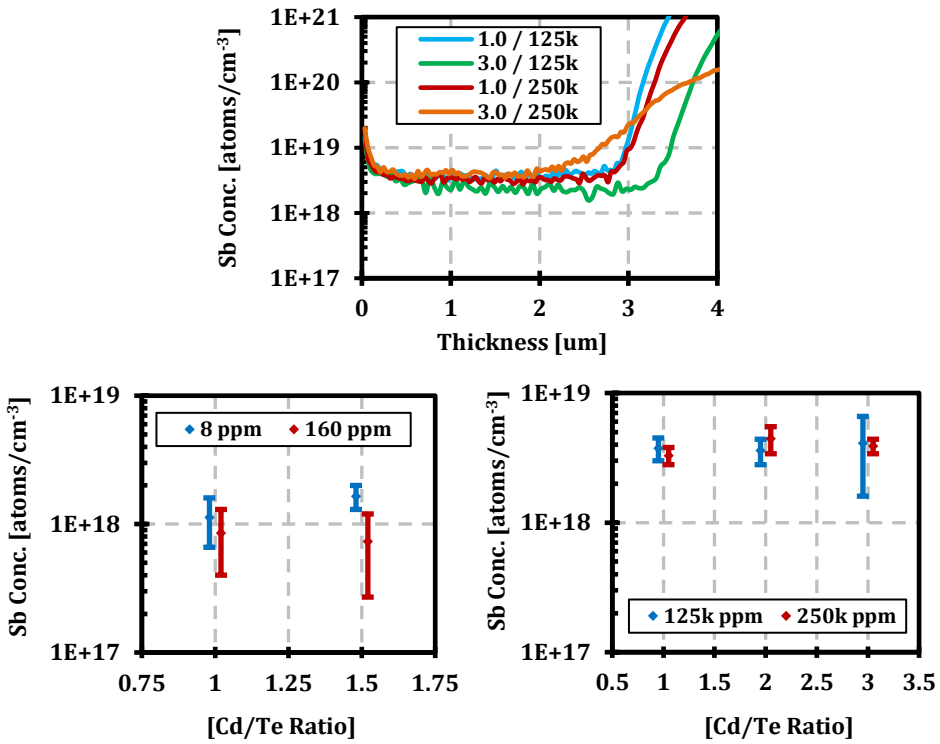

Figure 5.4 SIMS measurement on Sb doped CdTe films

Net p-type doping also increased with increasing vapor phase Sb concentration. For an Sb vapor concentration of 250k ppm, nearly two orders of magnitude increase in the doping concentration was observed compared to as deposited or low Sb concentration films.

Nevertheless, compared to the dopant incorporation level indicated in the SIMS measurements, the doping efficiency was low. Only 0.01 ~ 0.1% of the Sb atoms in the film

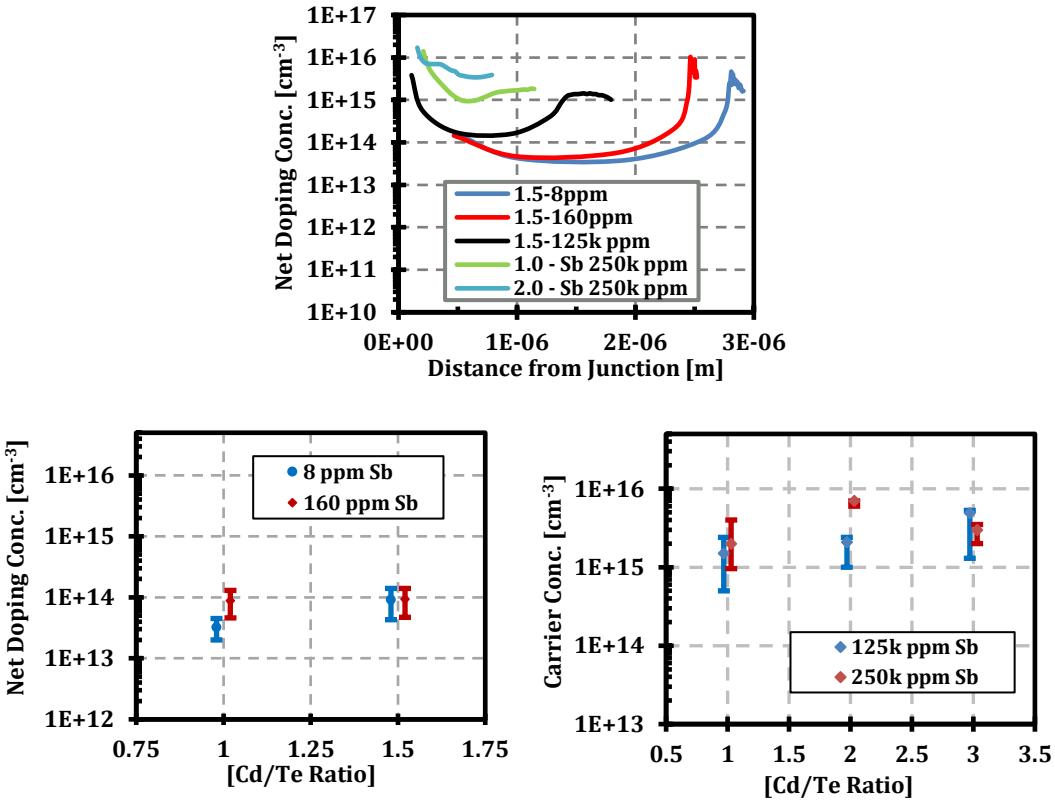

Figure 5.5 Capacitance-Voltage measurement on Sb doped CdTe devices. (Top) The doping profile as a function of distance from junction for select devices. (Bottom) Net doping concentration for EVT-CdTe with different gas phase Cd/Te ratio and Sb concentration.

contributed to the net hole concentration. The ionization energy of 0.23 eV for Sb_{Te} acceptor defect is one possible reason for low doping efficiency. Secondly, these films were deposited in Cd-rich deposition conditions favoring the formation of V_{Te} and Cd_i, intrinsic shallow donor defects in CdTe. At such high concentration, the scenario of Sb occupying Cd sites or the formation of interstitial Sb cannot be neglected, creating additional donor defects. Compensation by these donor defects is likely to adversely affect the doping efficiency. Doping concentration values as a function of Cd/Te ratio and gas phase Sb concentration is tabulated in Table 5.1. The net doping values presented on the table represent the 0 V bias doping value obtained from the CV measurements. A carrier concentration up to $3x10^{15}$ cm^{-3} was observed for vapor phase Cd/Te ratio 2.0 with 250k ppm Sb.

The CV measurements also indicated a very short junction length (Figure 5.5 Top), with a decreasing trend at higher doping value devices. This is consistent with the fact that the depletion width is inversely proportional to the doping concentration in CdTe. For high doping concentrations a depletion width less than 1 μm is expected. Assuming a CdS doping level of 1×10^{17} cm^{-3} and a CdTe doping level on the order of 10^{15} cm^{-3}, a depletion width of approx. 0.7 μm forms in the CdTe layer.

Table 5.2 Net doping conc. with different vapor phase Sb conc. and Cd/Te ratio

Cd/Te Vapor Ratio	Sb Vapor Conc. (ppm)	Doping Conc. (cm^{-3})
1.0	8	$2x10^{13}$
1.0	60	$3x10^{13}$
1.0	160	$5x10^{13}$
1.0	125k	$1x10^{14}$
1.5		$2x10^{14}$
2.0		$4x10^{14}$
1.0	250k	$2x10^{15}$
2.0		$7x10^{15}$
3.0		$3x10^{15}$

5.6 Cell Performance

Standard optimization steps for CdTe solar cells, such as $CdCl_2$ heat treatment and Cu doping, were not performed on these devices with the intention of isolating the effect of Sb on CdTe. Undoped (i.e. no intentional Cu added) graphite paste was used as the back contact, in order to avoid Cu effects. Hence, the cell performances were not comparable to high efficiency state-of-the-art devices. An increasing trend in V_{OC} was observed as a function of increasing Sb vapor concentration and also increasing Cd/Te ratio. For vapor phase Sb concentrations up to 10^5 ppm, device V_{OC}'s were below 600 mV (Table 5.3), despite increasing net doping concentrations. V_{OC}'s increased above 700 mV for 250k ppm Sb. In Figure 5.6 (top) each data point shows the range of V_{OC}'s for 3 cells made on the same substrate. The highest V_{OC} of 760 mV with a FF of 52% was observed for Cd/Te vapor ratio of 2.0 with the gas phase Sb concentration of 250k ppm. Further increase in Cd/Te ratio resulted in drastic reduction in cell

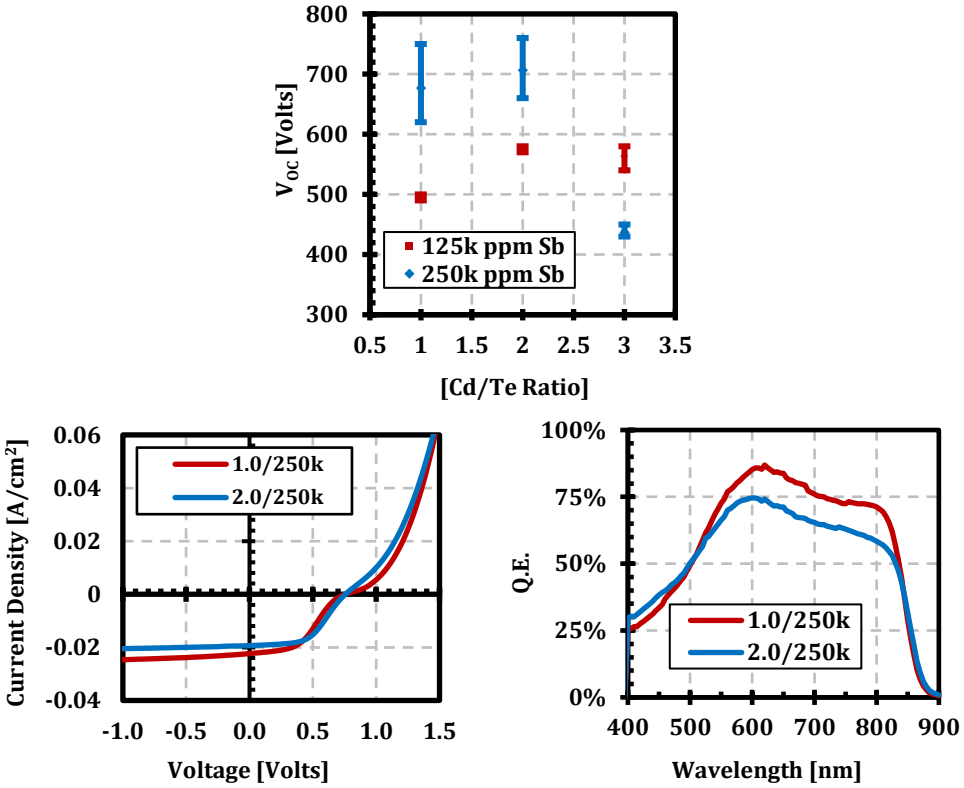

Figure 5.6 Cell performance for Sb doped CdTe devices. (Top) V_{OC} of devices with different gas phase stoichiometry and Sb concentration. (Bottom) JV and SR for two of the better performing cells.

performance. This decrease in performance at high Cd/Te ratio could be due to changes in the morphology of the films (discussed in section 5.3).

Table 5.3 Cell performance with Sb conc. and Cd/Te ratio

Cd/Te Vapor Ratio	Sb Vapor Conc. (ppm)	V_{OC} (volts)	Fill Factor (%)	J_{SC} (mA/cm^2)
1.0	70	570	39.4	16.1
1.25	70	570	40.2	16.2
1.0	22k	570	36.0	16.3
1.25	22k	570	35.0	15.1
1.0	125k	505	38.4	16.1
1.5		580	38.9	16.9
2.0		580	45.8	16.8
1.0	250k	750	42.6	19.4
2.0		760	52.2	17.5
3.0		450	44.2	16.3

One possible reason for the overall low FF for the cells is the non-optimized back contact (no intentional Cu), causing added series resistance. The effect of short junction length is observed on the SR measurements, resulting in reduced J_{SC}. Longer wavelength light gets absorbed deeper in the bulk CdTe, away from the junction. In this case, due to narrower depletion widths charge collection becomes diffusion dominant, resulting in a reduced quantum efficiency at longer wavelengths.

The QE data is also indicative of low minority carrier lifetime, as diffusion dominant carrier collection require higher carrier lifetime to prevent carrier loss due to SRH recombination (discussed in the next section). Formation of rectifying back contact can also be responsible for the reduced charge collection efficiency at long wavelengths.

5.7 Minority Carrier Lifetime

Minority carrier lifetimes were measured using time-resolved photoluminescence (TRPL) for a subset of the samples. The results are shown in Figure 6 along with the corresponding carrier concentrations from CV measurements. Although theoretical calculation suggests better lifetime for Cd-rich CdTe, previous work indicated poor carrier lifetime (below the detection limit of the TRPL device, possibly in the order of 0.1 ns) for as-deposited undoped polycrystalline CdTe [75]. The $CdCl_2$ HT is an essential post deposition treatment for improving minority carrier lifetime in polycrystalline CdTe. Table 5.4 lists the minority carrier lifetime for various CdTe films. With $CdCl_2$

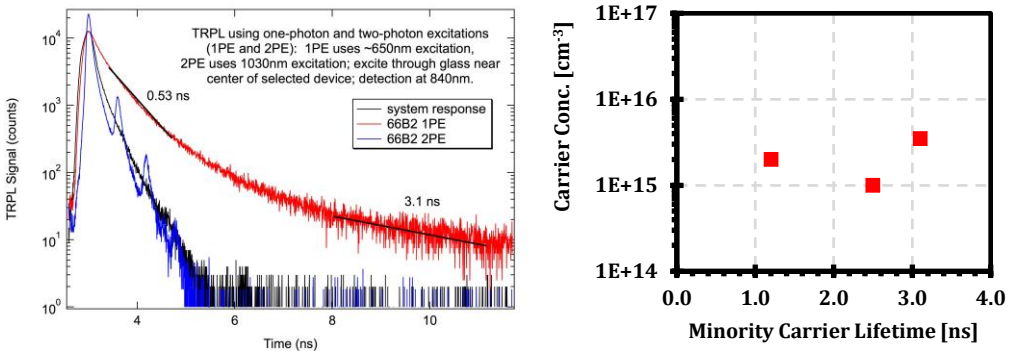

Figure 5.7 Carrier lifetime data for Sb doped CdTe. (Left) TRPL for EVT CdTe films deposited with Cd/Te vapor phase ratio 2.0 and 250k ppm Sb. (Right) Minority carrier lifetime in relationship to their net doping concentrations.

HT Te-rich deposited films exhibited higher lifetime. For in situ Sb doped films, higher lifetimes were observed for Cd-rich deposited devices.

Table 5.4 TRPL lifetime data for different Cd/Te ratio and post-deposition treatments

Cd/Te	Attribute	Lifetime, τ (ns)
0.7	As Deposited	0.1*
1		0.1*
1.4		0.1*
0.7	$CdCl_2$ HT	7.0
1		2.0
1.4		2.4
1.0	In situ Sb	2.5
2.0		3.1
3.0		1.2

Incorporation of Sb during the deposition process improved the lifetime up to 3.1 ns, for Cd/Te ratio 2.0 with 250k ppm Sb (Figure 5.7). A possible explanation for lifetime improvement is that the incorporation of Sb in highly non-stoichiometric Cd-rich vapor deposition can reduce grain boundary (GB) related deep states to improve the carrier lifetime. According to the double positioning twin boundary model, two main types of deep level introducing GBs, referred as Cd-core and Te-core, are present in polycrystalline CdTe [117]. Cd-core GBs are identified by Cd-terminated surfaces, and are expected in a higher concentration in Cd-rich deposition condition. It is possible that Sb incorporation can passivate the deep defects associated with Cd terminated surfaces to improve the minority carrier lifetime. Sb was not as effective in lifetime improvement as Cl, but the significance of Sb incorporation was that it improved the lifetime in Cd-rich deposited CdTe.

5.8 Sb Incorporation and $CdCl_2$ HT

Figure 5.8 (top) shows the JV and SR data for the Sb doped CdTe solar cell devices without any post deposition treatment. V_{OC} remained in 600 mV range for Sb concentrations up to 125k ppm. The SR of the devices with Cd/Te ratio 1.5 and low concentrations of Sb were significantly different. These Cd-rich deposited devices exhibited a weak short wavelength response that increased at longer wavelengths. These results suggested that the junction was

located deep into the sample (i.e. near or at the back contact). This could occur if the CdTe was intrinsic / n-type forming a Schottky junction with the graphite back contact. The SR for the 125k and 250k ppm devices, was more typical of what one would expect from a p-CdTe/n-CdS heterojunction. These observations suggested that high concentrations of Sb could convert the Cd-rich deposited CdTe conductivity type from n- to p-type.

Figure 5.8 (bottom) shows the JV and SR data for the Sb doped CdTe solar cell devices with $CdCl_2$ heat treatment. No improvement in V_{OC} was observed even at the highest concentrations of Sb. High QE for the devices with low concentrations of Sb, indicated that $CdCl_2$ HT could also convert the intrinsic / n-type CdTe films to p-type. The high Sb devices in this case exhibited reduced carrier collection specially in longer wavelength. This is an indication of lower minority carrier lifetime (discussed in section 4.2). Comparison of the QE data for low and high conc. of Sb with Cl, suggested that high Sb concentration negated the lifetime improvements in

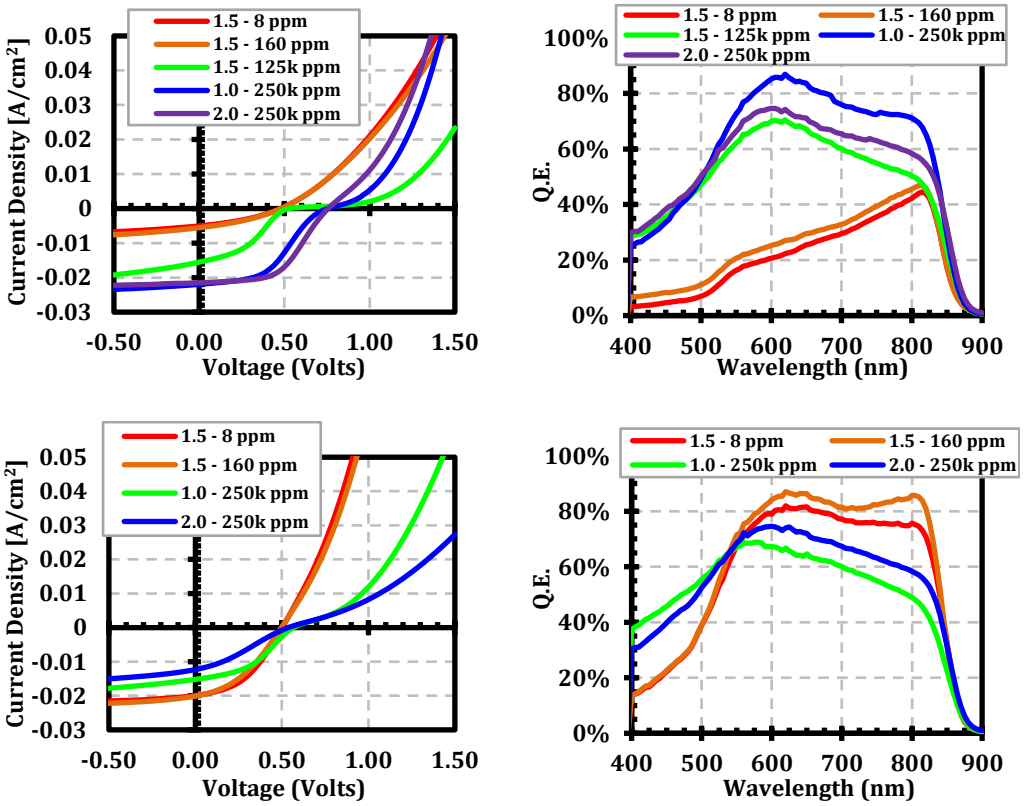

Figure 5.8 JV and SR data for Sb doped CdTe devices. (Top) without $CdCl_2$ HT and (bottom) with $CdCl_2$ HT.

Cl treatment. Both Cl and Sb could compete for the same Te site in CdTe. This could work in two ways, Cl_{Te} could compensate the effect of Sb_{Te} acceptor defects, and Sb could nullify the lifetime improvement due to $CdCl_2$ HT.

5.9 Summary of Chapter 5

In-situ Sb doping in pX CdTe was demonstrated. The structural and electrical characteristics of the resultant films/devices were studied. SIMS measurements confirmed the presence of Sb in the films. The net p-type carrier concentrations were influenced by the gas phase Cd/Te ratio and Sb vapor concentration. The higher carrier concentrations were correlated to higher V_{OC}'s. The observed behavior was explained in terms of defect formation and ionization energy. Sb incorporation also resulted in improvement in minority carrier lifetime. This led to a V_{OC} of 760 mV without Cu or $CdCl_2$ heat treatment, with corresponding minority carrier lifetime of 3.1 ns and carrier concentration of 10^{16} cm^{-3}. No improvement in device performance was observed due to $CdCl_2$ HT for Sb doped CdTe devices, indicating a possible competing mechanism for Sb and Cl to occupy the same Te sites in CdTe.

CHAPTER 6: PHOSPHORUS DOPING OF CDTE

6.1 In Situ P Doping

Phosphorus (P), a group V element, can be a p-type dopant in CdTe. When P occupies Te sites, it forms P_{Te} a shallow acceptor defect (Section 2.4.4). P as an extrinsic dopant was investigated by in situ P during CdTe growth.

6.2 Vapor Phase Phosphorus Dose

Glass/TCO/CdS was used as the substrate for all P doped CdTe depositions with an intent to fabricate solar cells. Cadmium Phosphide (Cd_3P_2) with purity 99.999% was used as the phosphorus dopant source. The gas phase concentration of P was estimated using vapor pressure data of Cd_3P_2, given by the following equation [118].

$$\mathrm{P}_{Cd_3P_2}(\mathrm{atm}) = 10^{-\frac{7725.2}{\mathrm{T}}+8.4933} \qquad (6.1)$$

Then, the vapor pressure contribution of the phosphorus species is found as, $P(P_4)$ = 0.143 x $P(Cd_3P_2)$. Phosphorus molecules in the vapor phase stay as quadratomic P_4, due to the following decomposition reaction.

$$Cd_3P_2\ (c) \leftrightarrow 3Cd\ (g) + ½\ P_4\ (g) \qquad (6.2)$$

Vapor phase P concentration in parts per million (ppm) was calculated as the ratio of P vapor concentration, and either Cd or Te vapor concentration for a stoichiometric Cd/Te vapor ratio deposition. The samples are described in terms of vapor phase Cd/Te ratio and P concentration in parts per million (ppm).

The vapor phase P concentration was varied by a combined manipulation of dopant zone temperature and gas flow rate. The experimental parameters used to achieve different vapor phase P concentration during deposition are listed in Table 6.1.

CdTe depositions for in situ P doping were performed both in near atmospheric pressure (700 Torr) and low pressure (25 Torr). For the following sections of the manuscript these will be referred to as AP-EVT and LP-EVT, and the results are discussed in sections 6.3 and 6.4 respectively.

Table 6.1 Experimental conditions for different phosphorus vapor concentrations

Vapor Phase P Conc. (ppm)	Dopant Zone Carrier Flow rate (cc/min)	Dopant Zone Temperature (ºC)
1	10	236
10	10	274
100	20	302
1000	20	351
4000	20	383
16000	20	420
20000	20	427

For characterization, the films/devices were contacted with graphite ink (no intentional Cu). Each deposited film was divided in half and processed with and without $CdCl_2$ heat treatment (HT), to understand the interaction of P and Cl.

6.3 P Doping: Atmospheric Pressure CdTe Deposition

The AP-EVT depositions were performed under near-atmospheric pressure of 700 Torr with 2 liter/min flow of UHP He as the main carrier gas. The Cd and Te zone flow rates were 400 cc/min. The deposition times were 40-80 mins. Phosphorus can form P_{Te} shallow acceptor defects by occupying Te sites; the availability of V_{Te} can facilitate P incorporation which is favorable in Cd-rich deposition conditions. Therefore, stoichiometric (Cd/Te ratio 1.0) and different Cd-rich (Cd/Te ratio 1.4, 2.0, 3.0) depositions conditions were chosen for P-doping. The vapor phase P conc. was varied from 1 ppm to 16k ppm. No P was detected with Energy Dispersive X-ray Spectroscopy (EDS) measurements within the detection limit (~1%) of the EDS instrument, even for the highest vapor phase P film (Figure 6.1), which indicated that no detectable alloying was present.

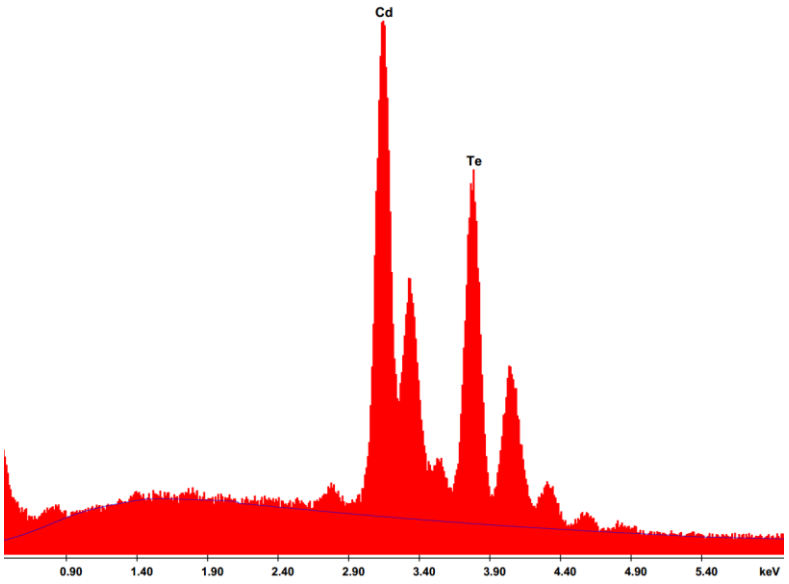

Figure 6.1 EDS Spectra for device deposited with 16k ppm P. No phosphorus detected.

6.3.1 Device Performance

Figure 6.2 shows the photovoltaic device performance for Cd/Te ratio 1.0 devices with various P vapor concentrations. As deposited devices exhibited low open circuit voltage, ~600 mV. V_{OC} increased for the 4k ppm P vapor concentration. With $CdCl_2$ HT the trend reversed, V_{OC}'s decreased for P concentrations of 4k and 16k ppm.

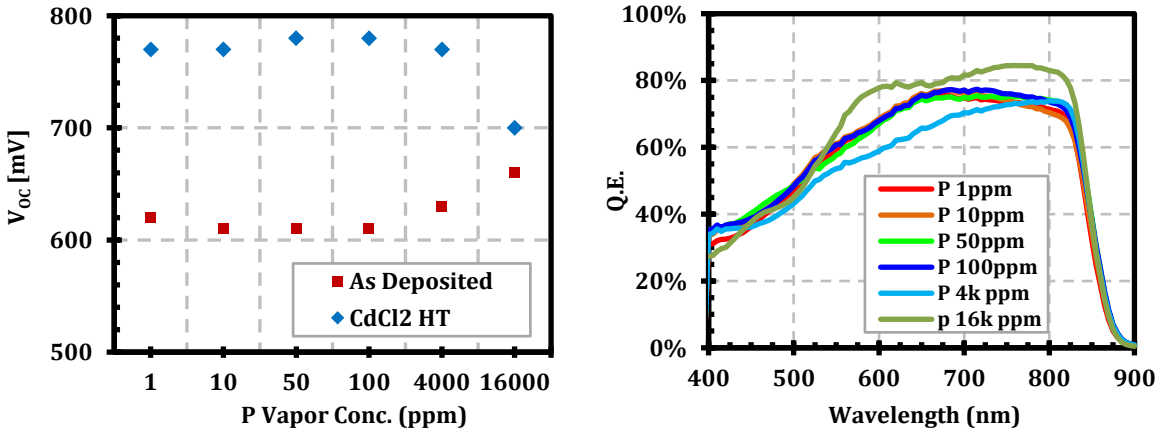

Figure 6.2 Cell performance for P doped CdTe devices with Cd/Te ratio 1.0. (Left) V_{OC} for devices with different P, with and without $CdCl_2$ HT. (Right) SR data for as deposited devices.

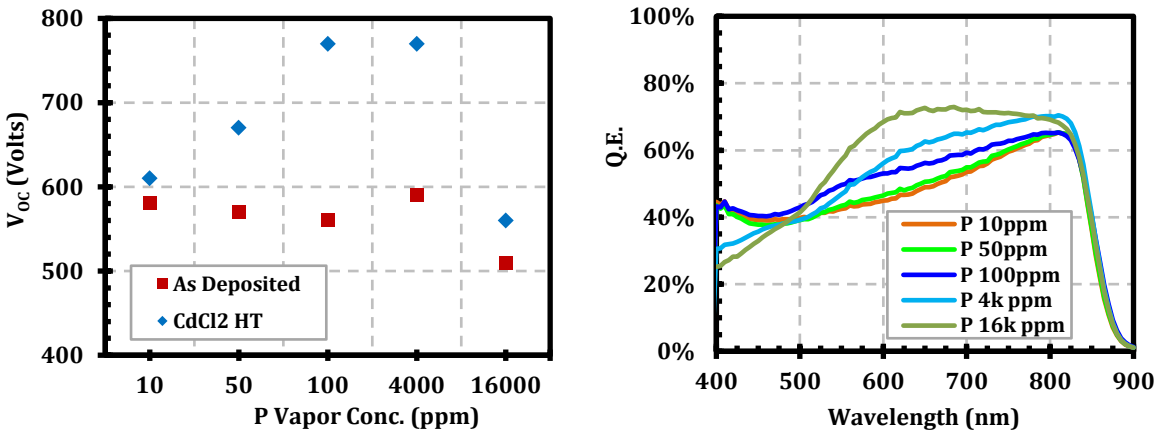

Figure 6.3 Cell performance for P doped CdTe devices with Cd/Te ratio 2.0. (Left) V_{OC} for devices with different P, with and without $CdCl_2$ HT. (Right) SR data for as deposited devices.

In Figure 6.3 the solar cell performance for Cd/Te ratio 2.0 devices with different P concentrations are shown. Device performance is overall lower compared to stoichiometric depositions. Cd/Te ratio 2.0 devices could be intrinsic or n-type [119], due to the shallow donors present in Cd-rich deposition conditions. Comparison with the ratio 1.0 deposited devices revealed that ratio 2.0 devices required a higher concentration of P to reach the same V_{OC} level. The reduction in performance for 16k ppm phosphorus is even more drastic in this case.

Both in Figure 6.2 (right) and 6.3 (right), the spectral response data for as deposited devices qualitatively indicated that the deposited films exhibited a transition from intrinsic/n-type to p-type. Longer wavelength light gets absorbed deeper in the junction. Reduced QE at low wavelength suggested that the junction could be at the back contact instead of the n-CdS/CdTe interface. This is possible when the CdTe absorber is either intrinsic and/or n-type [119]. At high P concentration, the QE appeared to be similar to typical CdTe solar cells, indicating that vapor phase P can convert the films to become p-type, indicating the formation of P_{Te} acceptor states by elimination of V_{Te} donors. When the Cd/Te ratio further increased (R3.0), the device shows 'intrinsic/n-type' like behavior even with 16k ppm P (Figure 6.4 left). After $CdCl_2$ HT all films become p-type, irrespective of deposition ratio and P concentration, evident from the SR data for

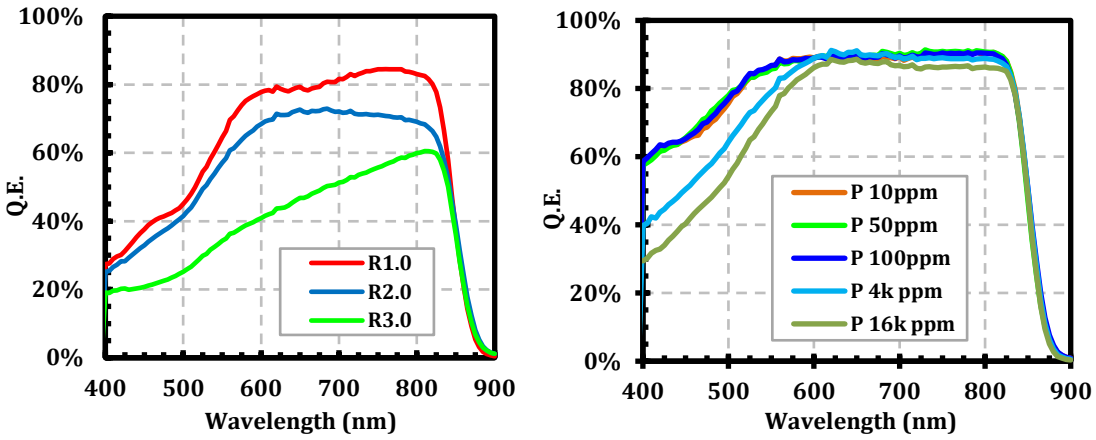

Figure 6.4 SR data for P doped CdTe devices with different Cd/Te ratio. (Left) As deposited (without $CdCl_2$ HT) CdTe devices with different ratio and 16k ppm P. (Right) $CdCl_2$ HT devices with Cd/Te ratio 2.0 and different P conc.

$CdCl_2$ treated ratio 2.0 devices with different P (Figure 6.4 right). The difference in QE at short wavelength in this case is due to a difference in CdS window layer thicknesses. The device performance data for some of these devices are listed in Table 6.2.

Although higher Cd/Te ratio is expected to facilitate P incorporation, we observe that stoichiometric deposited CdTe:P devices performed relatively better. P doping was attempted on Te-rich deposited devices, and they exhibited the highest V_{OC} for various conditions of stoichiometry (Figure 6.5). Overall efficiency was higher for ratio 1.0 with 50 ppm phosphorus,

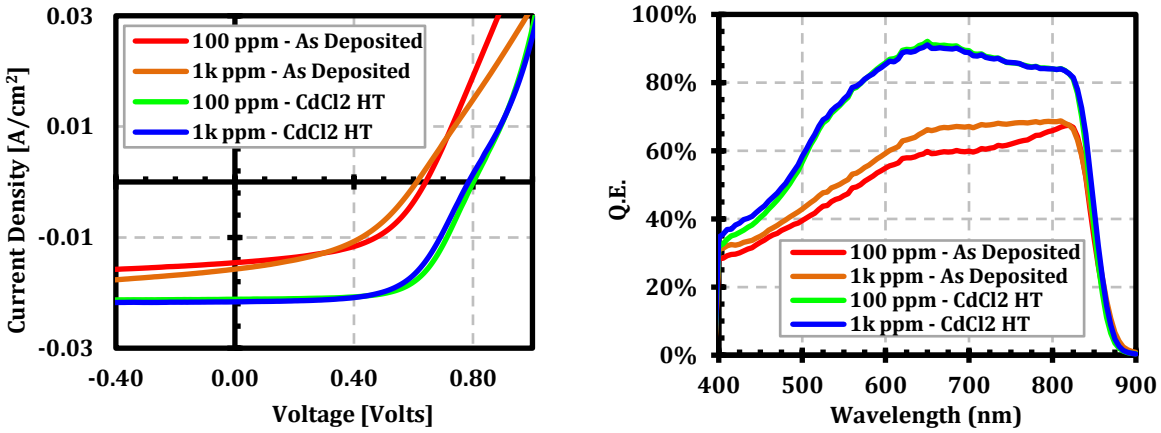

Figure 6.5 SR data for P doped CdTe devices with Cd/Te ratio 0.7 and P. (Left) JV data and (Right) SR data for devices with and without $CdCl_2$ HT.

due to higher fill factor. Device performance can be explained in terms of measured doping concentration.

Table 6.2 Cell performances for in situ phosphorus doping with AP-EVT

Cd/Te Vapor Ratio	Vapor Phase P Conc. (ppm)	$CdCl_2$ HT	V_{OC} (mV)	Fill Factor (%)	J_{SC} (mA/cm^2)	Efficiency (%)
1.0	1	N	620	43.7	18.2	4.9
1.0	1	Y	770	65.4	22.3	11.2
1.0	50	N	610	44.4	18.6	5.0
1.0	50	Y	780	67.9	22.9	12.1
1.0	4k	N	630	48.5	17.3	5.3
1.0	4k	Y	770	58	22.3	10.0
1.0	16k	N	660	53.7	20.0	7.1
1.0	16k	Y	700	44.2	22.1	6.8
2.0	50	N	570	41.8	14.7	3.5
2.0	50	Y	670	48.4	24.5	7.9
2.0	4k	N	590	44.3	16.3	4.3
2.0	4k	Y	770	56.1	23.22	10.0
2.0	16k	N	510	42.4	17.7	3.8
2.0	16k	Y	560	30.3	21.9	3.7
3.0	16k	N	530	44.4	12.5	2.9
3.0	16k	Y	550	30.6	22.0	3.7
0.7	100	N	640	51.4	15.4	5.1
0.7	100	Y	800	64.2	21.9	11.2
0.7	1k	N	610	45.4	16.7	4.6
0.7	1k	Y	790	62.9	22.1	11.0

6.3.2 Doping Concentration

Net doping concentrations for the devices were estimated form capacitance-voltage (CV) measurements. Doping data could not be obtained from as deposited devices, as the CV measurements indicated completely depleted absorbers. The doping data was obtained from $CdCl_2$ HT devices, and the net doping concentration corresponding to 0 V bias is shown in figure 6.6 right.

The doping concentrations showed an overall increasing trend with increasing phosphorus concentration. The highest doping values were observed at high P concentrations, reaching near $1x10^{15}$ cm^{-3} value. These relatively higher values didn't translate to better performing devices, as

the films looked blackish and powdery. Poor performance in this case was possibly due to structural defects. To improve the structural characteristic of the films at those high dopant films, low pressure EVT depositions were attempted which are discussed in section 6.4.

It can be anticipated that shallow acceptor levels V_{Te} and Cd_i, prevalent in Cd-rich deposition conditions, are the limiting factors for the net dopant concentration saturation. Te-rich deposited films, on the other hand, are intrinsically p-type, but P doping could be limited due to unavailability of Te vacancy sites. $CdCl_2$ HT also could have played a role in limiting the net doping, as Cl and P compete for the same Te sites in CdTe.

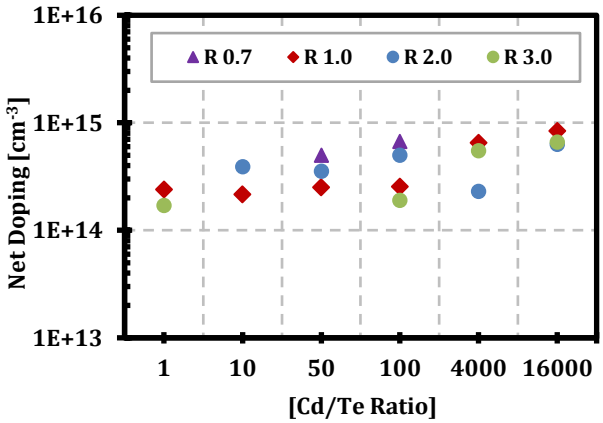

Figure 6.6 CV measurement for P doped CdTe devices. Net doping conc. corresponding to 0 V bias from CV data for devices with $CdCl_2$ HT.

6.4 P Doping: Low Pressure CdTe Deposition

Low pressure EVT CdTe depositions not only exhibited increased deposition rate, but also eliminated powdery deposits observed at high Cd/Te ratio and high P dose conditions. The LP-EVT depositions were performed under 25 Torr with 0.8 liter/min flow of UHP He as the carrier gas. The Cd and Te zone flow rates were 100 cc/min. The deposition times were 4-7 mins. The vapor phase P concentration was varied from 0 to 20k ppm. The depositions were performed at Te-rich (R0.7), stoichiometric (R1.0) and Cd-rich (R1.4) deposition conditions.

6.4.1 Device Performance

In situ P doped CdTe devices without $CdCl_2$ HT exhibited low photovoltaic performance. V_{OC} is in the 600 to 650 mV range with no significant relation to deposition stoichiometry and phosphorus concentration. Figure 6.7 (left side) shows the JV data for the vapor phase Te-rich (top) and Cd-rich (bottom) deposited devices. Stoichiometric (Cd/Te=1.0) deposited devices exhibited the same characteristics (not shown here). High P concentration devices also exhibited back barrier behavior. No doping data could be extracted from CV measurements due to completely depleted absorbers, suggesting very low doping. Higher P concentration devices also exhibited lower J_{SC} (Figure 6.7 right column). Lower long wavelength carrier collection along with the overall reduction suggests reduced minority carrier lifetime and poor interface. Considering SR data to be an indication of the carrier lifetime, Cd-rich deposited films could have lower lifetimes compared to Te-rich deposited films.

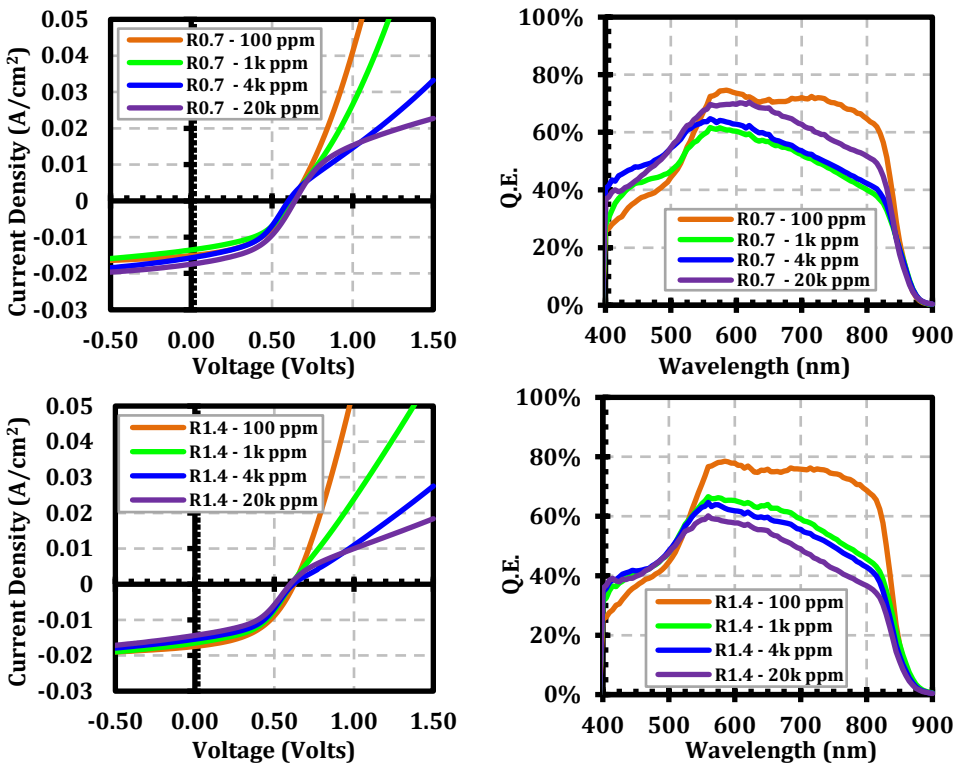

Figure 6.7 Device performance for as-deposited CdTe devices with different P. Current-Voltage measurement (left) and Spectral Response (right) for cells from Te-rich (top) and Cd-rich (bottom) deposited CdTe devices. No $CdCl_2$ HT or no intentional Cu doping.

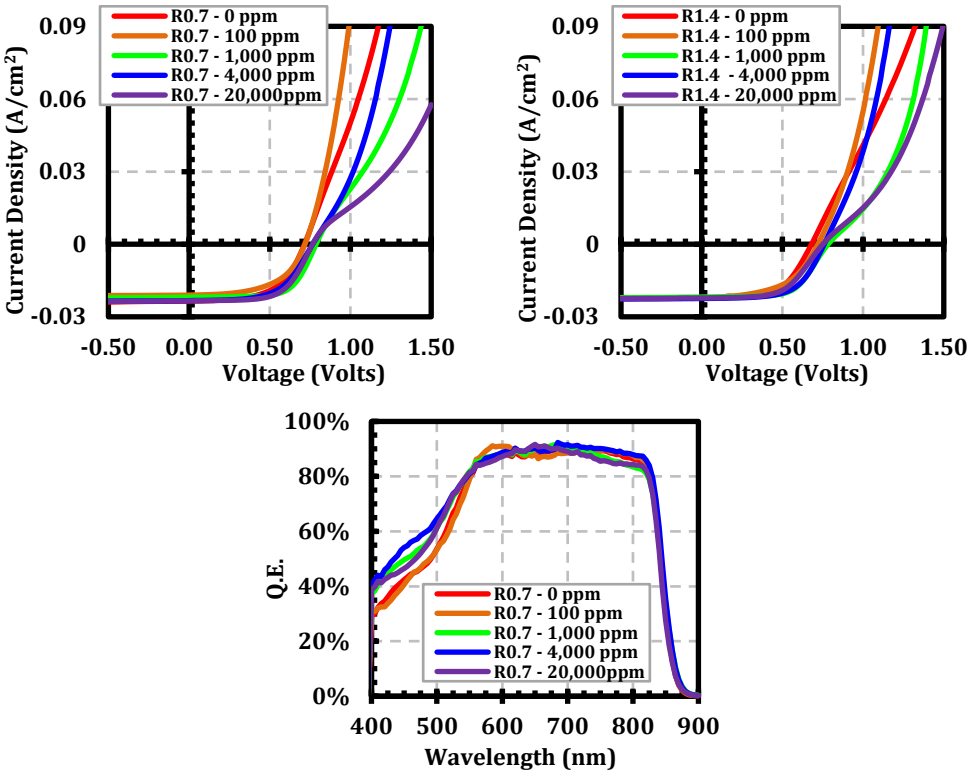

Figure 6.8 Device performance for CdTe devices with $CdCl_2$ HT and different P dose

The baseline $CdCl_2$ HT at 390 ºC for 25 min improved device performances (Figure 6.8). Without the P dopant, Te-rich deposited devices demonstrated higher V_{OC} and net doping, possibly due to the presence of V_{Cd} acceptors. V_{OC} increased with vapor phase P up to 1000 ppm. Further increase in P dose decreased V_{OC}. The indication of a back barrier in the devices with high P concentration persisted after the $CdCl_2$ HT of the devices. The solar cell performance numbers for some of the key P doped CdTe devices are shown in Table 6.3.

6.4.2 Doping Concentration

Figure 6.9 (left) shows the net doping concentrations calculated from CV measurements for devices with different deposition stoichiometry and P concentrations. The corresponding V_{OC} of the devices are shown on the right side of the figure.

Table 6.3 Cell performances for in situ phosphorus doping with LP-EVT

Cd/Te Vapor Ratio	Vapor Phase P Conc. (ppm)	$CdCl_2$ HT	V_{OC} (mV)	Fill Factor (%)	J_{SC} (mA/cm^2)	Efficiency (%)
0.7	0	Y	720	56.7	22.0	8.98
1.0	0	Y	710	58.2	22.9	9.46
1.4	0	Y	680	58.2	22.1	8.75
0.7	100	N	630	46.1	17.7	5.14
1.0	100	N	630	47.5	18.7	5.60
1.4	100	N	630	46.1	18.4	5.34
0.7	100	Y	720	55.0	21.9	8.67
1.0	100	Y	720	54.3	22.0	8.60
1.4	100	Y	720	52.3	21.8	8.21
0.7	1000	Y	790	66.4	22.6	11.86
1.0	1000	Y	790	64.2	22.4	11.36
1.4	1000	Y	780	62.5	22.4	10.92
0.7	20k	Y	770	61.9	22.2	10.58
1.0	20k	Y	760	62.9	22.3	10.66
1.4	20k	Y	750	57.2	22.2	9.52

The V_{OC} error bar is generated from three devices on the same substrate, while the dotted line connects the average values. The doping graph shows the range of net doping values from CV measurements, and the dotted line in this case connects the net doping value corresponding to 0 V (zero volt) bias. The inclusion of P during the deposition increased net doping, however the net doping decreased at high P concentrations, possibly due to compensation. The net doping values were weakly correlated to the V_{OC}. Phosphorus occupying Te site in CdTe forms P_{Te}

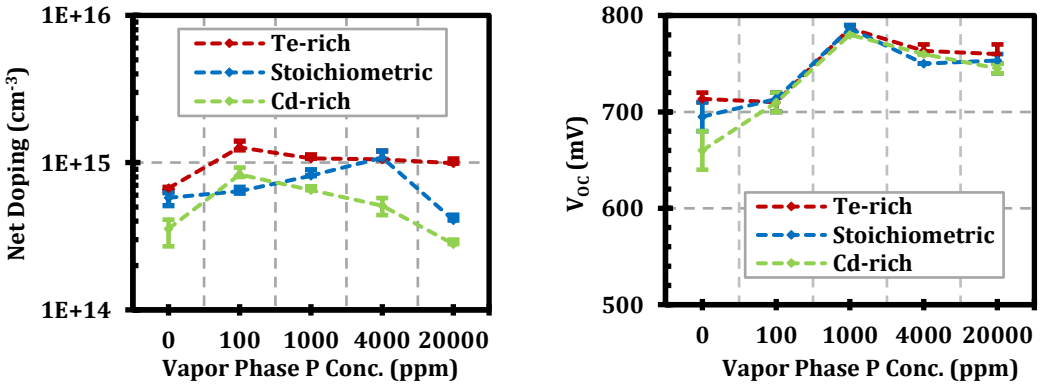

Figure 6.9 Device summary for CdTe devices with $CdCl_2$ HT and different P dose

shallow acceptors, favorable under Cd-rich deposition condition. Overall lower net doping in Cd-rich vapor deposited devices could be the result of compensation due to native Cd_i or V_{Te} shallow defects. Reduction in net doping at high P concentration devices is possibly because of the formation of compensating Ax-centers. Moreover, Cl also occupies Te sites in CdTe, that can also play a compensating role in reducing net doping. Discussion of possible Cl effect in phosphorus doping is continued in the following section.

6.4.3 Defect Analysis: P Doped CdTe

The phosphorus vapor conc. of 1,000 ppm resulted in the best performing devices and 20k ppm indicated excessive amount of P. These two concentrations were chosen for further analysis. Both vapor phase Cd-rich and Te-rich devices with in situ 1k ppm and 20k P concentration were treated with $CdCl_2$ at temperatures of 350, 370 & 390 ºC for 25 mins. V_{OC} & J_{SC} improved with increased $CdCl_2$ HT temperature; the best performance was obtained at the baseline temperature of 390 ºC. The increase in J_{SC} was due to the well-known lifetime improvement effect of $CdCl_2$ HT, evident from the increase in long wavelength carrier collection (Figure 6.10 right). The overall higher net doping for Te-rich deposited devices is reproduced. However, the highest doping is observed at $CdCl_2$ HT temperature of 370 ºC. $CdCl_2$ HT can contribute to p-type doping by forming A-center complex defect. In $CdCl_2$ treated P-doped sample,

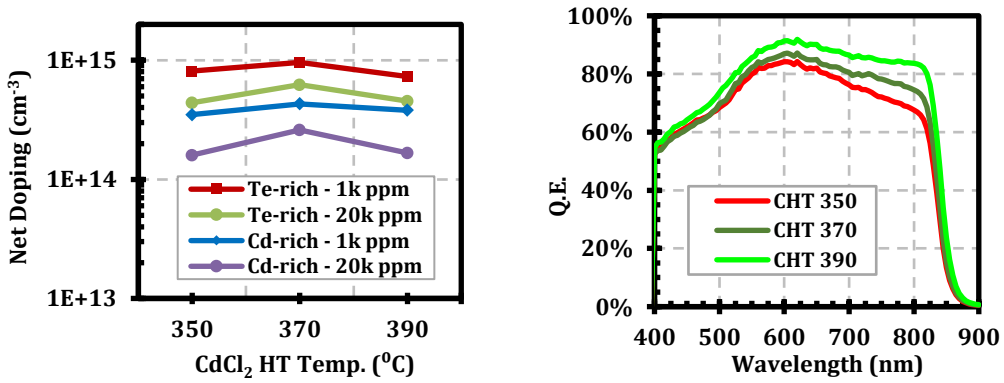

Figure 6.10 Device data for P doped CdTe with different $CdCl_2$ HT temperature. (Left) Net doping from CV measurements. (Left) Spectral response for Cd-rich deposited devices with 1000 ppm P.

both Cl and P can compete for the available Te-sites and Cl_{Te} donors can compensate for P_{Te} acceptors.

Deep Level Transient Spectroscopy (DLTS) measurement on these devices revealed a number of different electron and hole traps. Figure 6.11 shows the DLTS spectra for the devices with 1000 ppm vapor phase phosphorus. DLTS measurement on $CdCl_2$ treated intrinsically deposited EVT-CdTe with different stoichiometry has been discussed in Section 4.7. Minority carrier electron trap E1 was speculated to be a native CdTe defect, related to Cd_i and/or Te_{Cd}, due to its presence in all CdTe devices. E2 is a shallower electron trap, and it becomes more distinct with increasing $CdCl_2$ HT temperature. It is assigned to Cl related defects, possibly Cl_{Te} or Cl_i.

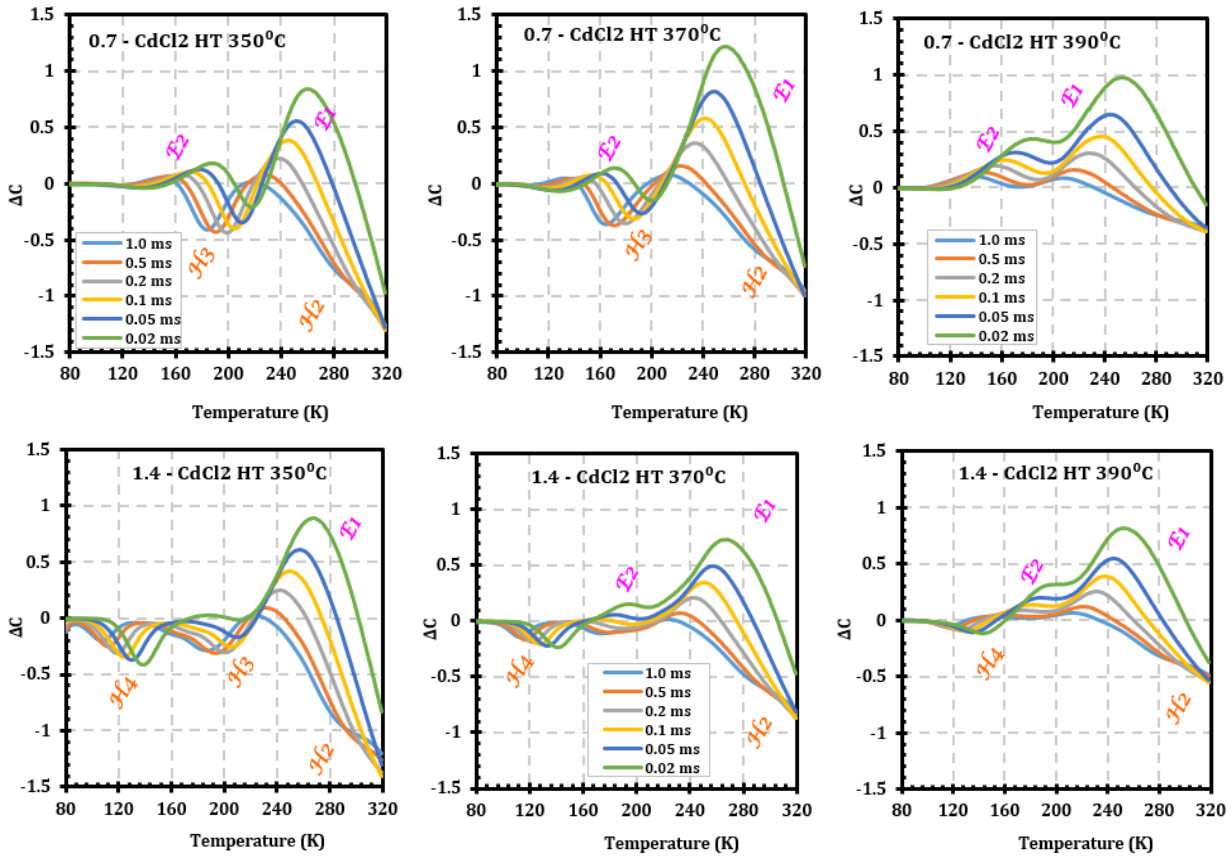

Figure 6.11 DLTS spectra for CdTe devices with in situ phosphorus dose of 1000 ppm. Different Cd/Te vapor ratio and $CdCl_2$ HT temperature; Top row – Te rich and bottom row – Cd rich deposited devices. Columns, from left to right, represent $CdCl_2$ HT temperatures of 350, 370 and 390 ºC respectively.

H2 is a hole trap representing a shallow acceptor defect. Based on its activation energy, it could be the A-center theorized in the literature. The DLTS spectra continues toward larger negative values at room temperature and above. This signifies the presence of deep hole traps, denoted H2. The intensity decreased with increasing $CdCl_2$ HT temperature. This deep defect could be related to the minority carrier lifetime and its intensity correlates to the SR data shown in Figure 6.10 (right). In baseline CdTe devices, H2 was mostly eliminated/passivated by the baseline $CdCl_2$ HT. This suggested that P doped CdTe devices might have lower minority carrier lifetime compared to intrinsically deposited CdTe.

The most prominent observation among these DLTS data was the shallow hole trap H4. This trap indicated a shallow acceptor defect, and was not observed in any other CdTe devices

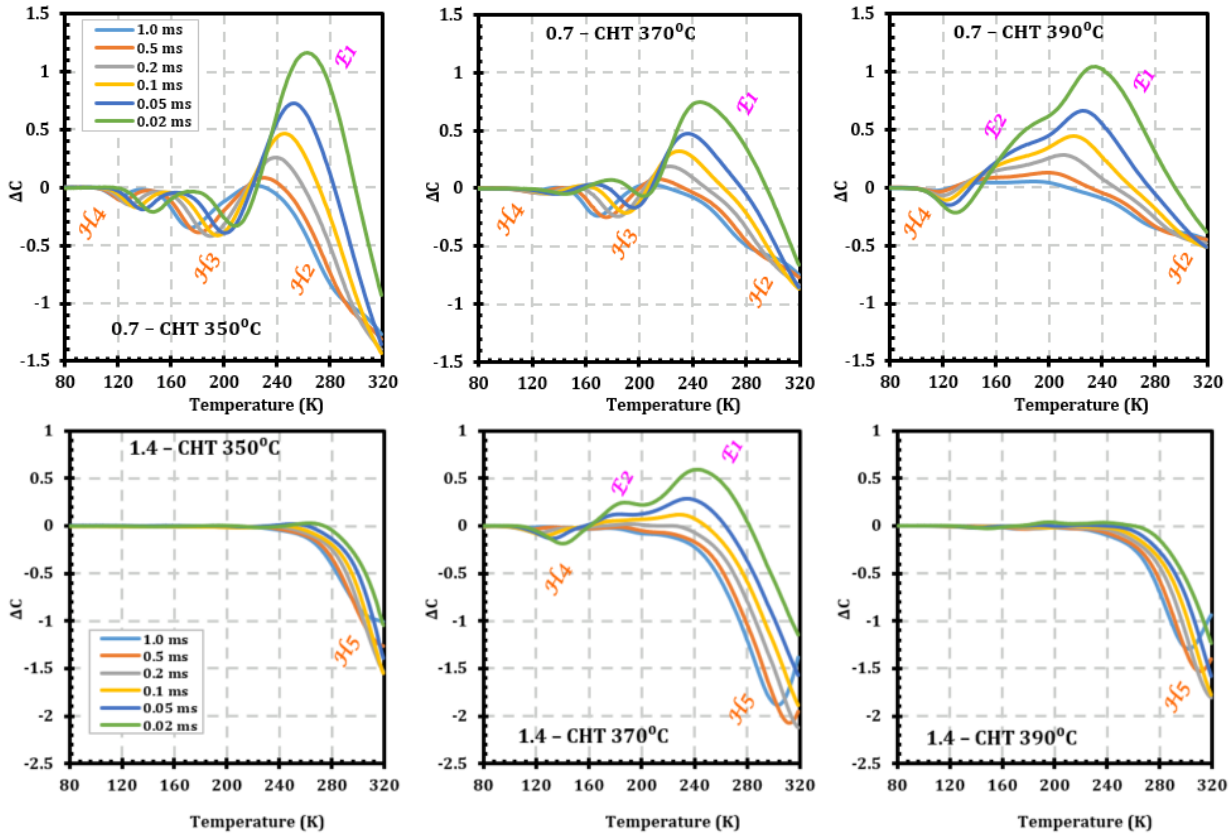

Figure 6.12 DLTS spectra for CdTe devices with in situ phosphorus dose of 20k ppm. Different Cd/Te vapor ratio and $CdCl_2$ HT temperature; Top row – Te-rich and bottom row – Cd-rich deposited devices. Columns, from left to right, represent $CdCl_2$ HT temperatures of 350, 370 and 390 ºC respectively.

without P. Its presence in Cd-rich deposited devices only, along with its reduced intensity with $CdCl_2$ HT temperature, suggested that it could be a P related acceptor defect P_{Te}. However, this defect was not as shallow as it had been suggested in the literature. A decrease of its intensity with higher $CdCl_2$ HT temperature indicated that Cl and P could be competing for the Te sites, and may remove the P from the P_{Te} acceptor states to interstitial sites.

Figure 6.12 shows the DLTS spectra for the devices with 20k ppm P vapor phase concentration. A distinct difference compared to the 1k ppm devices is that H4 was observed even for Te-rich deposited devices, and didn't get eliminated at the highest $CdCl_2$ HT temperature. For the Cd-rich deposited devices with 20k ppm P, a deep majority carrier peak H5 was the most prominent. One of the criteria for DLTS measurement is that trap concentration N_T << net doping concentration, N_D. High concentration of this deep majority defect may have made it difficult to quantify the shallower defects. An attempt at high temperature DLTS to measure this deep defect caused permanent damage to the device. Figure 6.13 shows the result for one such measurement; the higher temperature measurement could only be performed once per device. The activation energy of the trap was calculated to be E_V + 0.75 eV, and as a midgap defect, could reduce the minority carrier lifetime of the films. A possible source of this deep defect is Te_i [40], as excess P may substitute Te forcing it to move to interstitial sites.

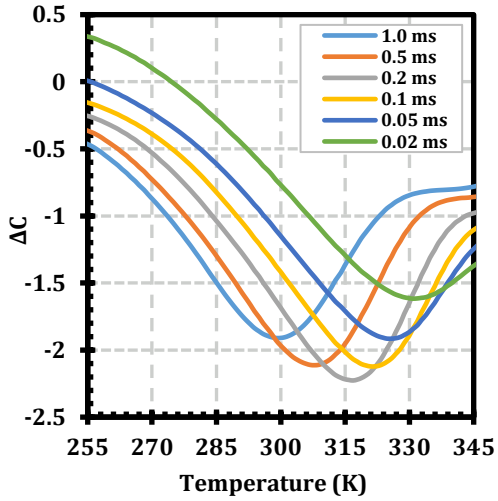

Figure 6.13 DLTS spectra for the deep defect in Cd-rich CdTe device with 20k ppm P

A summary of different defects identified in devices deposited with various deposition conditions and post-deposition treatments are listed in Table 6.4. In some cases, not all defect parameters could be resolved with certainty due to the proximity to other peaks and low intensity. In such situations, the presence of the traps were only qualitatively confirmed. The range of values given are from measurements of the same defect in different samples. The tentative defect assignments are based on their behavior vs. deposition stoichiometry, doping concentration, and post-deposition treatment conditions.

Table 6.4 Different defects identified form DLTS measurement

Defect	**Observations**	**Tentative Assignment**	**Activation Energy (eV)**	**Capture Cross Section (cm^{-2})**
E1	• Present in all samples without Cu • Disappears after Cu	Cd_i or Te_{Cd}	E_C- 0.46~0.52 eV	10^{-12} - 10^{-14}
E2	• Increases in intensity with Cd-rich deposition Present in all samples with Cu • Increases in intensity with $CdCl_2$ HT temperature	Cl_{Te} or Cl_i	E_C- 0.22~0.26 eV	10^{-15} - 10^{-16}
H1	• Observed in intrinsic deposited devices with $CdCl_2$ HT • Disappear after Cu doping	V_{Cd}	E_V+ 0.38~0.42 eV	10^{-17}
H2	• In Cd-rich deposited devices with Cl HT • Passivated by increasing Cl HT temp. • Observed in Cu doped devices • Parameters could not be determined due to higher temperature requirement • Responsible for carrier lifetime, may be related to GB defects in pX CdTe	GB	--	--
H3	• Disappears with increasing $CdCl_2$ HT	V_{Cd} - Cl_{Te}	E_V+ 0.14~0.18 eV	10^{-16} - 10^{-17}
H4	• Observed in P doped devices only • More prominent in Cd-rich deposited devices • Eliminated with increased $CdCl_2$ HT temperature	P_{Te}	E_V+ 0.15~0.20 eV	10^{-17} - 10^{-19}
H5	• Observed in high P dose devices	Te_i	E_V + 0.68~0.75 eV	10^{-12} - 10^{-13}

6.5 Summary of Chapter 6

In situ P doping of Polycrystalline CdTe by elemental vapor transport was investigated. The carrier concentration in the films was influenced by the gas phase Cd/Te ratio and P vapor concentration. The higher carrier concentrations were correlated to higher V_{OC}'s in the solar cells. Excessive amount of P reduced both net doping concentration and device performance. The observed behavior was explained in terms of defect formation and ionization energy. DLTS measurements on the devices identified various shallow and deep defects. The presence of the deep defect may be limiting the device performance for high P concentration samples. DLTS data suggested that P incorporation might also negatively impact the minority carrier lifetime; and in $CdCl_2$ treated devices, they are compensated by the Cl_{Te} defects. In high P concentration samples, the doping could be compensated by interstitial phosphorus or AX center, and carrier lifetime could be limited by formation of midgap defect Te_i. Shallow acceptor defect was identified in P doped CdTe devices.

CHAPTER 7: CONCLUSIONS AND FUTURE OPPORTUNITIES

7.1 Conclusions

The effect of deposition stoichiometry (Cd/Te vapor ratio) in determining the electrical properties of polycrystalline (pX) CdTe thin films and solar cells was investigated. Vapor phase stoichiometry was directly correlated to doping concentration and minority carrier lifetime, and consequently device performance. DLTS measurements were performed in devices with various post deposition treatments. $CdCl_2$ heat treatment was more effective in Te-rich deposited devices in eliminating deep defects and improving lifetime. Cd-rich deposited devices with $CdCl_2$ HT exhibited lower minority carrier lifetime due to the presence of deep majority carrier defects. Incorporation of Cu further reduced the minority carrier lifetime, as deep defects were re-introduced in devices with both Cl and Cu. These traps were assigned to different native and extrinsic CdTe defects based on their presence in specific devices and transition energy. Shallow minority trap in Cl and Cu treated devices, possibly Cl related, suggested a dopant compensation mechanism.

Polycrystalline CdTe with in situ Sb doping was deposited by elemental vapor transport. The presence of Sb in the films was confirmed by SIMS measurements. This work demonstrated that the carrier concentration on the films are influenced by the gas phase Cd/Te ratio and Sb vapor concentration. The higher carrier concentrations were correlated to higher V_{OC}'s in the solar cells. The observed behavior was explained in terms of defect formation and ionization energy. Sb incorporation also resulted in improved minority carrier lifetime. Poor doping efficiency is possibly due to non-optimal ionization energy of Sb_{Te} and donor compensation in Cd-rich deposition condition. V_{OC} of 760 mV without Cu or $CdCl_2$ heat treatment was achieved, with

corresponding minority carrier lifetime of 3.1 ns and net carrier concentration of 10^{16} cm^{-3}. $CdCl_2$ HT reduced the device performance in Sb doped CdTe.

Phosphorus doping in pX CdTe was performed using Cd_3P_2 as vapor source of P. Improved doping concentration due to increasing P vapor concentration was observed for $CdCl_2$ treated devices. The performance for as deposited devices was poor and no significant dopant incorporation effect was detected. Vapor phase P dose of 20k ppm was found to be excessive, and reduced device performance and doping. P doping was more effective on Te-rich deposition conditions, possibly due to compensation from Cd_i and V_{Te} donors. DLTS measurements on P doped devices revealed shallow acceptor trap that could be related to P_{Te} substitutional defect. Devices treated with various $CdCl_2$ HT temperatures suggested that P doping may be limited by Cl related donor defects.

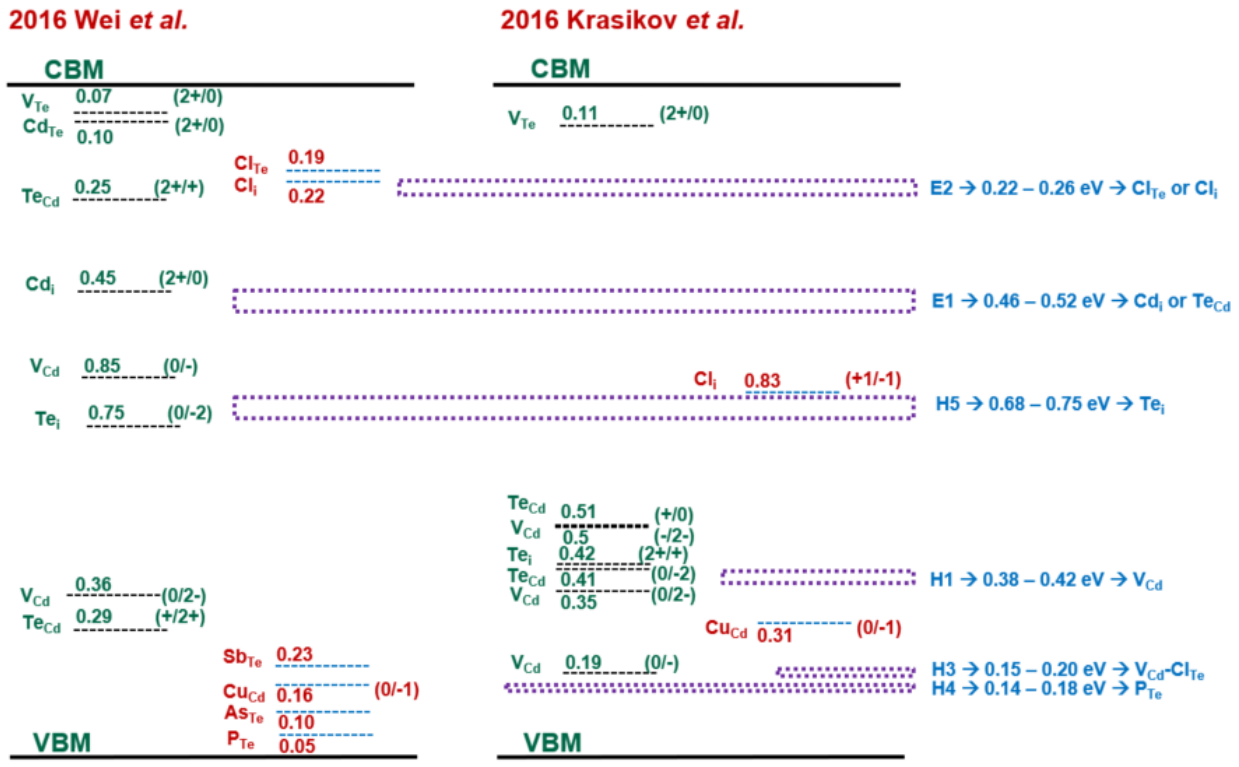

Figure 7.1 Defects identified in DLTS measurement in relation to the first principle calculations

Figure 7.1 shows the various CdTe defect levels identified in this investigation. Most recent first principle calculation results from two major research groups are shown for comparison (details in section 2.3.1). The findings of this study were mostly correlated with the calculations from Wei *et al*. It should be noted that, these theoretical calculations are continuously evolving and the underlying approximations are adjusted; often enabled due to the findings of the experimental results. Further investigations may be required to substantiate these defect assignments.

7.2 Future Opportunities

There were several distinctions between the findings for Sb and P as extrinsic dopants in CdTe. Very high dose of Sb (up to 250k ppm) was required compared to the P dose (up to 20k ppm) to observe the effect in device performance; suggesting that P could have a relatively better activation efficiency in CdTe. On the other hand, Sb incorporation improved carrier lifetime but DLTS measurements suggested poor lifetime (presence of deep defects) for P doped devices. TRPL lifetime measurement on the P doped films are needed to support the effect of phosphorus on the carrier lifetime in pX CdTe. $CdCl_2$ HT was required in P doped devices, whereas performance reduced in Sb doped devices with $CdCl_2$ HT. Sb at Te sites could be more favorable than P. Sb_{Te} has lower formation energy compared to P_{Te}. This is possibly due to the fact that the size of the Sb atom is close to Te atoms, making it more stable. Despite this, the relatively higher ionization energy of Sb_{Te} makes it undesirable. The issue with P in CdTe is the requirement of Cl treatment, which leads to dopant compensation with Cl, and possible lower lifetimes. However, P as dopant showed impressive results in sX CdTe. So, there may be other pathways for achieving better P activation. Theoretical analysis suggested rapid thermal cooling for group V doped CdTe films to limit the formation of compensating Ax centers, which could not be attempted in this investigation due to limitation in the deposition system.

The grain boundaries play a major role in defining the material properties of pX CdTe. Within the scope of this investigation, it could not be quantified how much of these dopant species

was segregated in the GB or affecting the CdS/CdTe interface. Studying the films using TEM, EDX and TRPL mapping could be a significant future extension to understand and troubleshoot the dopant compensation mechanism.

An alternative dopant is As, which stands between P and Sb in group V in the periodic table. Arsenic can be a p-type dopant in CdTe, creating shallow As_{Te} with a calculated ionization energy of 0.1 eV. Recent publications suggested that for As doping the high doping is retained after $CdCl_2$ HT. Fabricated in First Solar vapor transport deposition process, hole carrier-density $> 10^{16}$ cm^{-3} was reported [120].

The other attractive direction of exploring extrinsic dopant incorporation in the $CdTe_{1-x}Se_x$ alloy. Leading CdTe solar cell manufacturer First Solar is using graded $CdTe_{1-x}Se_x$ alloy as their core absorber layer due to improvement in output current. Considering that the first solar devices are way ahead in efficiency numbers than others researchers, investigating the alloy with extrinsic dopants such as P and As could lead to further improvement in efficiency. Research is ongoing at USF Thin Film Photovoltaic lab on these aspects.

REFERENCES

[1] "BP Statistical Review of World Energy June 2017", Retrieved October 11, 2017 from https://www.bp.com/content/dam/bp/en/corporate/pdf/energy-economics/statistical-review-2017/bp-statistical-review-of-world-energy-2017-full-report.pdf

[2] "BP Statistical Review of World Energy June 2016", Retrieved October 11, 2017 from https://www.bp.com/content/dam/bp/pdf/energy-economics/statistical-review-2016/bp-statistical-review-of-world-energy-2016-full-report.pdf

[3] "*Technology Roadmap: Solar Photovoltaic Energy",* International Energy Agency (2014), Retrieved October 11, 2017 from https://www.iea.org/publications/freepublications/publication/TechnologyRoadmapSolarPhotovoltaicEnergy_2014edition.pdf

[4] M. Grätzel, Solar Energy Conversion by Dye-Sensitized Photovoltaic Cells, Inorg. Chem., 2005, 44(20), 6841–6851

[5] Bett, A. W., et al. "III-V compounds for solar cell applications." Applied Physics A 69.2 (1999): 119-129

[6] Green, Martin A., et al. "Solar cell efficiency tables (version 51)." *Progress in Photovoltaics: Research and Applications* 26.1 (2018): 3-12

[7] Jean, Joel, et al. "Pathways for solar photovoltaics." Energy & Environmental Science 8.4 (2015): 1200-1219

[8] Photovoltaics Report, Fraunhofer ISE, 2017. Retrieved October 11, 2017 from https://www.ise.fraunhofer.de/content/dam/ise/de/documents/publications/studies/Photovoltaics-Report.pdf

[9] Jackson, Philip, et al. "Effects of heavy alkali elements in Cu (In, Ga) Se2 solar cells with efficiencies up to 22.6%." *physica status solidi (RRL)-Rapid Research Letters* 10.8 (2016): 583-586

[10] First solar Press Release February 23, 2016. Retrieved October 11, 2017 from http://investor.firstsolar.com/index.php/news-releases/news-release-details/first-solar-achieves-yet-another-cell-conversion-efficiency

[11] First solar Press Release June 15, 2015. Retrieved October 11, 2017 from http://investor.firstsolar.com/index.php/news-releases/news-release-details/first-solar-achieves-world-record-186-thin-film-module

[12] M. Grätzel, *The Advent of Mesoscopic Injection Solar Cells*, Progress in Photovoltaics: Research and Applications, 2006, 14(5), 429-442

[13] H. J. Snaith, J. Phys. Chem. Lett., 2013, 4, 3623–3630

[14] Song, Tao, A. Kanevce, and J. R. Sites. "Emitter/absorber interface of CdTe solar cells." *Journal of Applied Physics* 119.23 (2016): 233104.

[15] National Renewable Energy Laboratory (2017), Reference Solar Spectral Irradiance: Air Mass 1.5, Retrieved October 11, 2017 from http://rredc.nrel.gov/solar/spectra/am1.5/

[16] Geisthardt, R. M., M. Topič, and J. R. Sites. "Status and potential of CdTe solar-cell efficiency." *IEEE Journal of photovoltaics* 5.4 (2015): 1217-1221

[17] McCandless, B. E., and J. R. Sites. "Cadmium telluride solar cells." *Handbook of Photovoltaic Science and Engineering* 2 (2003)

[18] V. M. Fthenakis, H. C. Kim, and E. Alsema. "Emissions from photovoltaic life cycles," *Environmental Science & Technology,* vol. 42(6), pp. 2168-2174, 2008

[19] K. Zweibel and V. Fthenakis, Cadmium facts and handy comparisons, revision 26-12-2002, Report of NREL (National Renewable Energy Laboratory) and BNL (Brookhaven National Laboratory), Retrieved October 11, 2017 from https://www.bnl.gov/pv/files/pdf/art_165.pdf

[20] Bohland, John R., and K. Smigielski. "First Solar's CdTe module manufacturing experience; environmental, health and safety results." *Photovoltaic Specialists conference, 2000. Conference Record of the Twenty-Eighth IEEE*. IEEE, 2000

[21] Bonnet, D., Cadmium telluride solar cells, in *Clean Electricity from Photovoltaics*, M. Archer and R. Hill (Eds.), Imperial College Press, London (2001)

[22] P. Moskowitz and V. Fthenakis, Toxic materials released from photovoltaic modules during fires; health risks, *Solar Cells*, **29**, 63–71 (1990)

[23] H. Steinberger, Health, safety and environmental risks from the operation of CdTe and CIS thin-film modules, *Prog. Photovolt. Res. Appl.*, **6**, 99–103 (1998)

[24] Frerichs R, *Phys. Rev.* **72**, 594–601 (1947)

[25] Jenny D, Bube R, *Phys. Rev.* **96**, 1190–1191 (1954)

[26] Kr¨uger F, de Nobel D, *J. Electron.* **1**, 190–202 (1955)

[27] Rappaport, Paul. "The photovoltaic effect and its utilization." *Solar Energy* 3.4 (1959): 8-18

[28] D. A. Cusano, 1963, Solid-State Electronics, vol. 6, pp. 217-232

[29] E. I. Andirovich, Y. M. Yuabov, and G. R. Yagudaev, 1969, Sov. Phys. Semicond., 3, pp. 61

[30] J. Britt and C. Ferekides, “Thin-film CdS/CdTe solar cell with 15.8% efficiency,” Appl. Phys. Lett., vol. 62, no. 22, pp. 2851–2852, 1993

[31] H. Ohyama, et al., “16.0% efficient thin-film CdS/CdTe solar cells,” in Proc. Conf. Rec. 26th IEEE Photovoltaic Spec. Conf., Anaheim, CA, USA, 1997

[32] X. Wu, et al., “16.5%-efficient CdS/CdTe polycrystalline thin-film solar cell,” in Proc. 17th Eur. Photovoltaic Sol. Energy Conf., 2001, pp. 995–1000

[33] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, “Solar cell efficiency tables (version 40),” Progr. Photovoltaics: Res. Appl., vol. 20, pp. 606–614, 2012

[34] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, “Solar cell efficiency tables (version 41),” Progr. Photovoltaic: Res. Appl., vol. 21, pp. 1–11, 2013

[35] Gloeckler, M.; Sankin, I.; Zhao, Z., "CdTe Solar Cells at the Threshold to 20% Efficiency," Photovoltaics, IEEE Journal of, vol.3, no.4, pp.1389,1393, Oct. 2013

[36] Green, Martin A., et al. "Solar cell efficiency tables (version 50)", *Progress in Photovoltaics: Research and Applications* 25.7 (2017): 668-676

[37] Wang, Jifeng, and Minoru Isshiki. "Wide-bandgap II–VI semiconductors: growth and properties." *Springer handbook of electronic and photonic materials*. Springer US, 2006. 325-342

[38] J. H. Greenberg, J. Cryst. Growth 161, 1 (1996)

[39] Wei, Su-Huai, and S. B. Zhang. "Chemical trends of defect formation and doping limit in II-VI semiconductors: The case of CdTe." *Physical Review B* 66.15 (2002): 155211

[40] Gessert, T. A., et al. "Research strategies toward improving thin-film CdTe photovoltaic devices beyond 20% conversion efficiency." *Solar Energy Materials and Solar Cells* 119 (2013): 149-155

[41] Yang, Ji-Hui, et al. "Review on first-principles study of defect properties of CdTe as a solar cell absorber", *Semiconductor Science and Technology* 31.8 (2016): 083002

[42] Krasikov, D. N., et al. "Theoretical analysis of non-radiative multiphonon recombination activity of intrinsic defects in CdTe", *Journal of Applied Physics* 119.8 (2016): 085706

[43] Berding M A 1999 Phys. Rev. B 60 8943

[44] Lordi, Vincenzo. "Point defects in Cd(Zn)Te and TlBr: Theory", *Journal of Crystal Growth* 379 (2013): 84-92

[45] J. Ma et al. “Dependence of the Minority-Carrier Lifetime on the Stoichiometry of CdTe Using Time-Resolved Photoluminescence and First-Principles Calculations,” Phys. Rev. Lett. Vol. 111, Issue. 6-9, August 2013

[46] Castaldini, A., et al. "Deep energy levels in CdTe and CdZnTe." *Journal of applied physics* 83.4 (1998): 2121-2126

[47] Balcioglu, A., R. K. Ahrenkiel, and F. Hasoon. "Deep-level impurities in CdTe/CdS thin-film solar cells." *Journal of Applied Physics* 88.12 (2000): 7175-7178

[48] Kremer, R. E., and W. B. Leigh. "Deep levels in CdTe." *Journal of Crystal Growth* 86.1-4 (1988): 490-496

[49] Collins, Shamara, et al. "Radiative recombination mechanisms in CdTe thin films deposited by elemental vapor transport." *Thin Solid Films* 582 (2015): 139-145

[50] Halliday, D. P., J. M. Eggleston, and K. Durose. "A photoluminescence study of polycrystalline thin-film CdTe/CdS solar cells." *Journal of crystal growth* 186.4 (1998): 543-549

[51] F. H. Seymour, V. Kaydanov, T. R. Ohno, and D. Albin, Appl. Phys. Lett. **87**, 153507 (2005)

[52] Isett, L. C. "Characterization of CdS/CdTe thin-film solar cells by admittance spectroscopy and deep-level transient spectroscopy." *Journal of applied physics* 56.12 (1984): 3508-3517

[53] Eiche, C., et al. "Investigation of compensation defects in CdTe: Cl samples grown by different techniques." *Journal of applied physics* 74.11 (1993): 6667-6670

[54] Ablekim, Tursun, et al. "Defects in Undoped p-type CdTe Single Crystals." *IEEE Journal of Photovoltaics* 6.6 (2016): 1663-1667

[55] D. V. Lang, "Deep Level Transient Spectroscopy: A New Method to Characterize Traps in Semiconductors." Journal of applied physics 45.7 (1974): 3023-3032

[56] L. C. Isett, "Characterization of CdS/CdTe Thin Film Solar Cells by Admittance Spectroscopy and Deep Level Transient Spectroscopy" Journal of applied physics 56.12 (1984): 3508-3517

[57] R. Dhere et al., "Influence of CdS/CdTe interface properties on the device properties," Photovoltaic Specialists Conference, 1997, Conference Record of the 26th IEEE, Anaheim, CA, 1997, pp. 435-438

[58] Zhao, Wang, et al. "Deep level transient spectroscopy investigation of deep levels in CdS/CdTe thin film solar cells with Te: Cu back contact." *Chinese Physics B* 19.2 (2010): 027303

[59] Versluys, Jorg, et al. "DLTS and admittance measurements on CdS/CdTe solar cells." *Thin Solid Films* 431 (2003): 148-152

[60] Collins, R. T., and T. C. McGill. "Electronic properties of deep levels in p-type CdTe." *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* 1.3 (1983): 1633-1636

[61] Komin, V., et al. "The effect of the CdCl 2 treatment on CdTe/CdS thin film solar cells studied using deep level transient spectroscopy." *Thin Solid Films* 431 (2003): 143-147

[62] Lourenco, M. A., et al. "Deep level transient spectroscopy of CdS/CdTe thin film solar cells." *Journal of applied physics* 82.3 (1997): 1423-1426

[63] Rohatgi, A. "A study of efficiency limiting defects in polycrystalline CdTe/CdS solar cells." *International journal of solar energy* 12.1-4 (1992): 37-49

[64] Metzger, W. K., et al. "Cd Cl 2 treatment, S diffusion, and recombination in polycrystalline CdTe." *Journal of applied physics*99.10 (2006): 103703

[65] Moutinho, H. R., et al. "Effects of $CdCl_2$ treatment on the recrystallization and electro-optical properties of CdTe thin films." *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* 16.3 (1998): 1251-1257

[66] Ringel, S. A., et al. "The effects of $CdCl_2$ on the electronic properties of molecular-beam epitaxially grown CdTe/CdS heterojunction solar cells." *Journal of applied physics* 70.2 (1991): 881-889

[67] Zhang, Lixin, et al. "Effect of co-passivation of Cl and Cu on CdTe grain boundaries." *Physical review letters* 101.15 (2008): 155501

[68] Harvey, Steven P., et al. "Direct evidence of enhanced chlorine segregation at grain boundaries in polycrystalline CdTe thin films via three-dimensional TOF-SIMS imaging." *Progress in Photovoltaics: Research and Applications* 23.7 (2015): 838-846

[69] Krasikov, Dmitry, and Igor Sankin. "Defect interactions and the role of complexes in the CdTe solar cell absorber." *Journal of Materials Chemistry A* 5.7 (2017): 3503-3513

[70] Krasikov, Dmitry, et al. "Search for the Major Chlorine-Related Defects in CdTe: Cl." *MRS Online Proceedings Library Archive*1638 (2014)

[71] Khan, M., et al. "Study of defects in polycrystalline CdTe using DLTS." *Photovoltaic Specialists Conference (PVSC), 2016 IEEE 43rd*. IEEE, 2016

[72] Kranz, Lukas, et al. *Nature communications* 4 (2013)

[73] S.E. Asher, F.S. Hasoon, T.A. Gessert, M.R. Young, P. Sheldon, J. HiltneP and J. Sites, 2000, IEEE Photovoltaic Specialists Conference, pp. 479-482

[74] K. Barri, M. Jayabal, H. Zhao, D. L. Morel, S. Asher, J. W. Pankow, M. R. Yong, C. S. Ferekides, 2005, IEEE 29th PVSC

[75] Khan, Imran S., et al. "Effect of Stoichiometry on the Lifetime and Doping Concentration of Polycrystalline CdTe." *IEEE Journal of Photovoltaics* 7.5 (2017): 1450-1455

[76] Kuciauskas, Darius, et al. "The impact of Cu on recombination in high voltage CdTe solar cells." *Applied Physics Letters* 107.24 (2015): 243906

[77] H. Zhao, A. Farah, D. Morel and C. Ferekides, “The effect of impurities on the doping and V_{OC} of CdTe/CdS thin film solar cells,” Thin Solid Films, Volume 517, Issue 7, 2 February 2009, pp.2365-2369

[78] Colegrove, Eric, et al. "Antimony Diffusion in CdTe." *IEEE Journal of Photovoltaics* 7.3 (2017): 870-873

[79] A. Picos-Vcga *et al*. “Physical properties of CdTe-Sb thin films” 1996, Thin Solid Films 290-291, pp. 395-400

[80] R. N. Bicknell, N. C. Giles, J. F. Schetzina, 1986, Appl. Phys. Lett. 49(25), pp. 1735-1737

[81] J. D. Benson *et al*, 2002, J. Cryst. Growth, Volume 95, Issues 1-4, pp. 543-546

[82] Santos-Cruz, J., et al. "Influence of the growth parameters of p-CdTe thin films on the performance of Au–Cu/p-CdTe/n-CdO type solar cells." *Solar energy* 80.2 (2006): 142-147

[83] Y. Hatanaka *et al*. 2001, Applied Surface Science 175-176, pp. 462-467

[84] Nair, Jaya P., et al. "In situ Sb-doped CdTe films." *Semiconductor science and technology* 13.3 (1998): 340

[85] Okamoto, Tamotsu, et al. "Effects of Antimony Doping in Polycrystalline CdTe Thin-Film Solar Cells." *Japanese Journal of Applied Physics* 51.10S (2012): 10NC12

[86] A.E. Abken, “Chemical stability of sputtered Mo/Sb_2Te_3 and Ni/Sb_2Te_3 layers in view of stable back contacts for CdTe/CdS thin film solar cells,” Sol. Energy Mater. Sol. Cells 73 (2002) 391

[87] Yang, Ji-Hui, et al. "Enhanced p-type dopability of P and As in CdTe using non-equilibrium thermal processing." *Journal of Applied Physics* 118.2 (2015): 025102

[88] Flores, Mauricio A., Walter Orellana, and Eduardo Menéndez-Proupin. "Self-compensation in phosphorus-doped CdTe." *arXiv preprint arXiv:1708.01847* (2017)

[89] Selim, F. A., and F. A. Kröger. "The Defect Structure of Phosphorus-Doped CdTe." *Journal of The Electrochemical Society* 124.3 (1977): 401-408

[90] H. L. Hwang, Klaus Y. J. Hsu, H. Y. Ueng, 1996, J. of Cryst. Growth 161, pp. 73-81

[91] Compaan, A. D., and V. Karpov. "The fabrication and physics of high-efficiency CdTe thin-film solar cells." *Annual Technical Report* (2002)

[92] Burst, J. M., et al. "Advances in control of doping and lifetime in single-crystal and polycrystalline CdTe." *Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th*. IEEE, 2014

[93] Colegrove, Eric, et al. "Phosphorus doping of polycrystalline CdTe by diffusion." *Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd*. IEEE, 2015

[94] Ablekim, Tursun, et al. "Fabrication of single-crystal solar cells from phosphorous-doped CdTe wafer." *Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd*. IEEE, 2015

[95] Burst, James M., et al. "CdTe solar cells with open-circuit voltage breaking the 1 V barrier." Nature Energy 1 (2016): 16015

[96] Colegrove, Eric, et al. "Phosphorus Diffusion Mechanisms and Deep Incorporation in Polycrystalline and Single-Crystalline CdTe." *Physical Review Applied* 5.5 (2016): 054014

[97] McCandless, Brian, et al. "Enhancing p-type Doping in Polycrystalline CdTe Films." *Photovoltaic Specialist Conference (PVSC), 2017 IEEE 44th*. IEEE, 2017

[98] W. Shockley, and H. J. Queisser, "Detailed balance limit of efficiency of p-n junction solar cells," *Journal of applied physics*, vol. 32, no. 3, pp. 510-519, 1961

[99] M. Gloeckler, I. Sankin, and Z. Zhao. "CdTe solar cells at the threshold to 20% efficiency", IEEE Journal of Photovoltaics 3.4, 2013, pp.1389-1393

[100] A. R. Duggal, J. J. Shiang, W. H. Huber, and A. F. Halverson, “Photovoltaic devices,” U.S. patent US20140373908 A1, Dec. 25, 2014

[101] J. Herrero, M.T. Gutierrez, C. Guillen, J.M. Dona, M.A. Martinez, A.M. Chaparro, Rayon, Photovoltaic windows by chemical bath deposition” Thin Solid Films 361-362, (2000), 28-33

[102] Handbook of Photovoltaic Science and Engineering; John Wiley & Sons, 2003; ch. 14; pp. 649-650

[103] Y. Liu, Y. Sun, and A. Rockett, “A new simulation software of solar cells—wxAMPS”, Solar Energy Materials and Solar Cells, Volume 98, March 2012, Pages 124-128, ISSN 0927-0248

[104] Solar Cell Device Physics, Second Edition. Stephen Fonash

[105] Gloeckler, M.; Fahrenbruch, A.L.; Sites, J.R., "Numerical modeling of CIGS and CdTe solar cells: setting the baseline," Photovoltaic Energy Conversion, 2003. Proceedings of 3rd World Conference on, vol.1, no., pp.491-494 Vol.1, 18-18 May 2003

[106] L. C. Isett, "Characterization of CdS/CdTe Thin Film Solar Cells by Admittance Spectroscopy and Deep Level Transient Spectroscopy" *Journal of applied physics*, vol. 56, no. 12, pp. 3508-3517, 1984

[107] Sharma, R. C., and Y. A. Chang. "The Cd-Te (cadmium-tellurium) system." *Journal of Phase Equilibria* 10.4 (1989): 334-339

[108] V. Evani, et al. "Effect of Cu and Cl on EVT-CdTe solar cells." *42nd IEEE Photovoltaic Specialist Conference (PVSC)*, 2015

[109] K. K. Chin, T. A. Gessert, and Su-Huai Wei, "The roles of Cu impurity states in CdTe thin film solar cells," *35th IEEE Photovoltaic Specialist Conference (PVSC)*, 2010

[110] Ji-Hui Yang, et al. "First-principles study of roles of Cu and Cl in polycrystalline CdTe." *Journal of Applied Physics*, vol. 119(4), pp. 045104, 2016

[111] L. Zhang et al. “Effect of Co-passivation of Cl and Cu on CdTe Grain Boundaries,” *Physical Review Letters*, vol. 101(15), pp. 122201, 2008

[112] Khan, M., et al. "In-situ antimony doping of CdTe." *Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd*. IEEE, 2015

[113] Aldred, A. T., and J. N. Pratt. "Vapor Pressures or Zinc, Cadmium, Antimony, and Thallium." *Journal of Chemical and Engineering Data* 8.3 (1963): 429-431

[114] Evani, V. K. "Improving Doping and Minority Carrier Lifetime of CdTe/CdS Solar Cells by in-situ Control of CdTe Stoichiometry." (2017)

[115] S. Kumar and T. Nann, "Hexagonal CdTe nanoparticles of various morphologies", Chem. Commun., 2003, 2478-2479

[116] Rosenblatt, Gerd M., and C. Ernest Birchenall. "Vapor Pressure of Antimony by the Torsion-Effusion Method." *The Journal of Chemical Physics* 35.3 (1961): 788-794.

[117] Y. Yan, M.M. Al-Jassim, and K.M. Jones, “Structure and effects of double-positioning twin boundaries in CdTe” Journal of Applied Physics, 94, 2976-2979 (2003)

[118] Schoonmaker, R. C., and K. Rubinson. "Vaporization of cadmium phosphide." *The Journal of Physical Chemistry* 71.10 (1967): 3354-3357

[119] Kendre, V., et al. "CdTe films by elemental vapor transport." *Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th*. IEEE, 2013

[120] Grover, S., et al. " Characterization of Arsenic Doped CdTe Layers and Solar Cells." *Photovoltaic Specialists Conference (PVSC), 2017 IEEE 44th* IEEE, 2017

APPENDIX A: LIST OF ACRONYMS

A.1 List of Acronyms

CB – Conduction Band

CdTe – Cadmium Telluride

CSS – Close Spaced Sublimation

CV – Capacitance - Voltage

DFT – Density Functional Theory

DLTS – Deep Level Transient Spectroscopy

FF – Fill Factor

GB – Grain Boundary

HSE – Heyd–Scuseria–Ernzerhof

JV – Current Density - Voltage

J_{SC} – Short circuit current

PBE – Perdew-Burke-Ernzerhof

PV – Photovoltaic

pX – Polycrystalline

QE – Quantum Efficiency

SIMS – Secondary Ion Mass Spectroscopy

SR – Spectral Response

sX – Single Crystalline

TFSC – Thin film solar cell

TRPL – Time Resolved Photoluminescence

UHP – Ultra High Purity

USF – University of South Florida

VB – Valence Band

V_{OC} – Open circuit voltage

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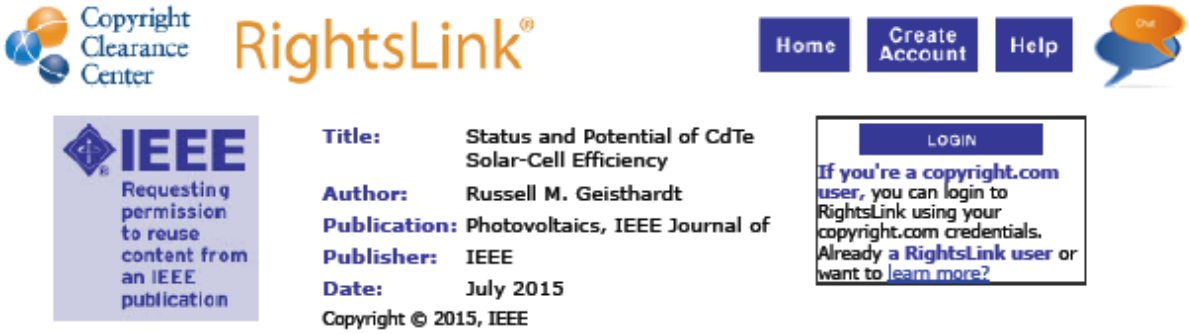

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