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Microwave Characterization of Printable Dielectric Inks Using Additive Manufacturing Methods

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by

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ABSTRACT

Two methods of dielectric characterization are presented that offer quick and cost-effective solutions for screening complex dielectric material properties. Through Direct-Print Additive Manufacturing (DPAM) methods, a dielectric material of choice is dispensed into a capacitor structure and characterized through 1-port s-parameter measurements. The presented methods use fixtures that are modeled and validated through simulation then implemented in practice. Advanced simulations are performed to gain insights which are used to optimize the dielectric characterization performance of the fixtures. Additional investigations are performed which investigate the durability of the fixture and material within by exposing the combination to rough environmental conditions for an extended duration. The presented capacitor structures are investigated to characterize dielectric materials within the bandwidth of 0.1-15 GHz, saving the time and effort required in using multiple dielectric characterization methods that cover the same bandwidth. Both methods are compared based on the results for each method achieved in practice while considering the process required perform each method. The pros and cons of the presented characterization methods are weighed which highlights the key aspects for successfully characterizing dielectric materials with each method as well as revealing the potential limitations associated with each.

CHAPTER 1: INTRODUCTION

1.1 Motivation

Additive manufacturing is changing the world as we know it; transforming traditional processes into new digital processes and providing great cost benefits as well as advantageous design freedoms. [1] Many aspects of industry are incorporating additive manufacturing methods in attempt to find new ways to benefit in their particular sector. One major area of interest for incorporation of additive manufacturing techniques is in the area of RF and microwave circuit design. The inherent benefits of incorporating these techniques to RF and microwave circuit design are the added flexibility and design freedoms. Exploitation of these freedoms can yield better electrical and mechanical performance not previously obtainable with traditional methods and opens the door for complex but efficient designs. [2]

The rapid growth of the additive manufacturing industry for RF and microwave circuits has resulted in a large number of commercially available printable materials that cover a variety of applications. One of the main categories of printable materials is dielectric inks. Dielectric inks come in many colors and viscosities all with particular applications ranging from in-mould electronics to flexible and wearable technologies. Many of these new printable dielectrics are desired to be used for RF and Microwave applications, and thus, must be characterized in the frequency band of interest. Some dielectric information may typically be provided on the respective manufacturer's datasheet, but will likely be limited, if at all available.

Traditional dielectric characterization methods require samples to be prepared that are of a specific set of dimensions to be used with a cavity specific fixture. For wide-band dielectric material characterization, multiple cavities may be required, making the overall process potentially slow and inefficient. This work proposes some quick screening solutions for the characterization of dielectric inks through utilization of Direct-Print Additive Manufacturing (DPAM) techniques. The presented solutions are intended to cut the time out of using multiple cavities or methods and could potentially be used in-line with a manufacturing process.

1.2 Overview

The first method of dielectric characterization presented features a circular fixture etched from PCB substrate. This method has been the subject of a few papers published from research conducted at the University of Massachusetts Lowell where the fixture was used to characterize a few different materials for the dielectric permittivity and loss tangent over an appreciable bandwidth. Through an admittance analysis method, the capacitor can be used to effectively extract the permittivity and loss tangent profile of the dielectric ink that is placed within the gap of the fixture.

In this investigation, an analysis is conducted on the effectiveness of the PCB fixture for dielectric properties extraction of dielectric inks. An improved equivalent circuit model of the PCB capacitor fixture is presented which is used to derive new extraction equations for permittivity and loss tangent based on the input admittance of the fixture. A simulation-based circuit model of the PCB fixture is built and simulated to test the effectiveness of the methodology and newly proposed extraction equations. This simulation-based model is built through optimization fitting the proposed circuit model to 3D simulation data of the fixture generated with ANSYS EDT. Through advanced 3D modeling, additional analyses are presented

which have not been previously conducted, providing key insights on practical utilization of the PCB fixture for dielectric characterization.

In addition to the PCB capacitor characterization method, a second method of dielectric characterization is proposed in which the simplicity of the parallel plate capacitor is exploited. With the presented method, a DPAM parallel plate capacitor is printed exclusively by micro-dispensing conductive and dielectric inks. Through an admittance analysis the capacitor is analyzed to extract the permittivity and loss tangent of the dielectric material between the plates. The printing of the capacitor is a three-step process by which the capacitor built by stacking layer upon layer. The simplicity of the proposed parallel plate extraction method makes for a fair comparison to the PCB capacitor fixture extraction method.

Both dielectric characterization methods presented utilize structures that are 1-port, therefore, they are both measured with a single probe in practice. The s-parameter data from the 1-port measurement is converted into admittance data which is used to construct models of the proposed structures. In both cases, circuit models are developed to identify and model the parasitics of each structure. Once the parasitics are identified, they are de-embedded from the fixture data. The admittance resulting from the de-embedding process is analyzed assuming a simplified capacitor model to extract the dielectric properties of interest.

After the presentation of the extraction methods, the two methods are compared analytically from a theoretical as well as practical perspective. An analysis of the pros and cons of each method is conducted where the challenges that were overcome with each method are considered. The performance of each extraction method is evaluated with the data obtained through the various investigations conducted.

The material printer utilized to conduct the experiments on the methods presented is a Tabletop-3Dn Series nScrypt like that shown in figure 1.1. The printer utilizes a pressurized valve system to dispense the ink that is actuated through programming. The desired valve actuation is proportional to the particle size of the material being used and determines the printed line width. The printer has a resolution of 0.5 um in every dimension with 100 mm of vertical range.

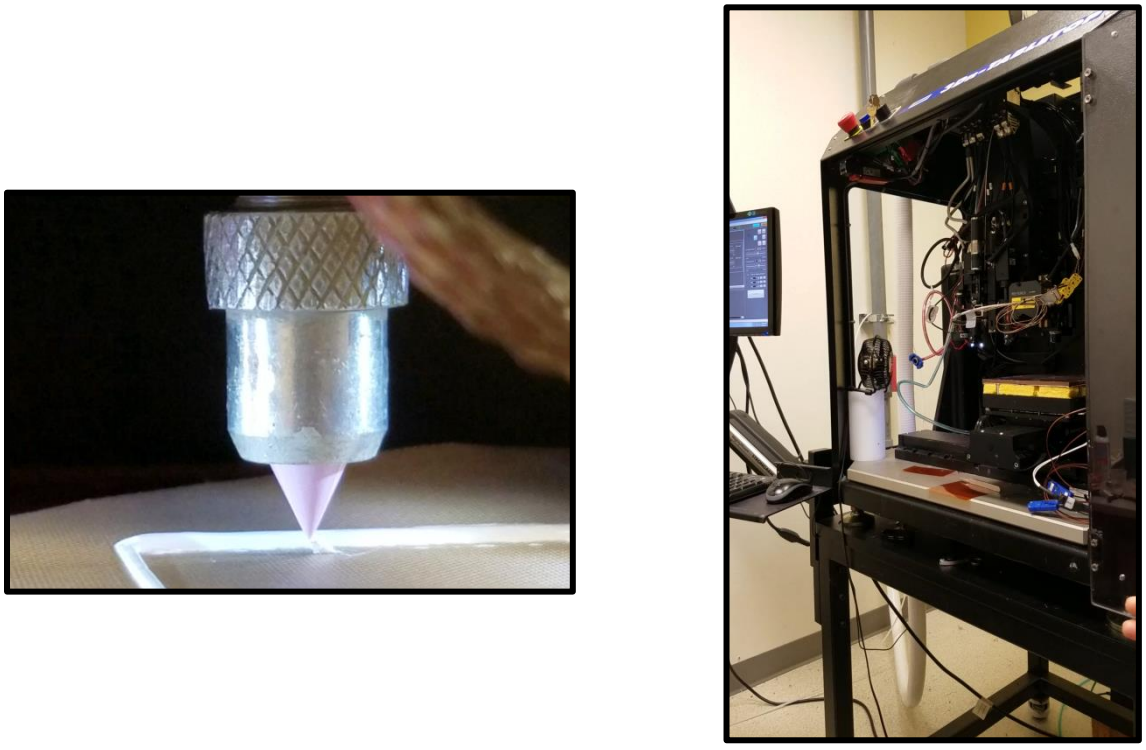


Figure 1.1 - *Tabletop Series nScrypt Material printer used to conduct the experiments presented.*

CHAPTER 2: CIRCULAR PCB CAPACITOR CHARACTERIZATION METHOD

2.1 Introduction and Background

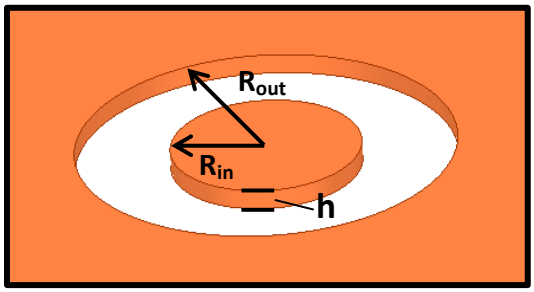
The first method of dielectric characterization presented utilizes a circular fixture etched from PCB substrate which can be seen in figure 2.1. This fixture was utilized previously to characterize a Barium Strontium Titanate polymer and a dielectric ink where it was reported that the fixture could yield wide-band dielectric characterization from 1-20 GHz [4,5]. The methodology used to characterize those materials with this fixture is explored further and improved upon by introducing a new set of equations for the dielectric properties extraction. Some additional experiments and analysis are performed to optimize the extraction performance of the fixture.

The effective capacitance of this circular PCB fixture can be modeled by considering a coaxial transmission line as the foundation. With that assumption, the capacitance equation is derived from the per-unit-length capacitance of a coaxial transmission line. From the Pozar text, the per-unit-length capacitance of a coaxial transmission line is calculated as [6]:

$$C' = \frac{2\pi\varepsilon}{\ln\left(\frac{b}{a}\right)} \tag{2.1}$$

In equation (2.1), variables *a* and *b* are the inner and outer radii of the gap, respectively, and are replaced as shown in figure 2.1. Since equation (2.1) represents the per-unit-length capacitance, the equation must be multiplied by the length of the assumed coaxial transmission line to get the whole fixture capacitance. In this situation the length of transmission line is equal

to the thickness of the copper cladding, *h*, so the per-unit-length capacitance gets multiplied by the cladding height to arrive equation (2.2).



$$C_{gap} = \frac{2\pi\varepsilon h}{\ln\left(\frac{R_{out}}{R_{in}}\right)} \tag{2.2}$$

Figure 2.1 - *Depiction of the circular PCB fixture with labeled dimensions and corresponding capacitance equation.*

The simplicity of the circular design allows for flexibility when it comes to probing the structure as measurements can be performed from any angle with an appropriately sized Ground-Signal-Ground (GSG) probe. The signal pin would land on the center conductor and the ground pins are free to land anywhere on the outer conductor across the gap. Two important design parameters of interest with this fixture are the gap width, which controls the ratio of R_{out} to R_{in}, and the cladding thickness, which determines *h*.

2.2 Fixture Modeling

The equivalent model of the circular capacitor fixture is presented in figure 2.2 [4,5]. The gap between the conductors represents a capacitance (C_{mat}) which can be calculated using equation (2.2). To complement this capacitance, there is an associated frequency dependent loss mechanism (G_{mat}) in parallel which is calculated using (2.3). When the fixture is empty (air-filled), G_{mat} is zero because air is assumed to be lossless.

$$G_{mat} = \omega C_{mat} \tan \partial_{\text{mat}} \tag{2.3}$$

Embedded in the circuit elements C_{mat} and $G_{mat,}$ are the dielectric properties of the material in the gap where the permittivity is embedded in C_{mat} and the loss tangent is embedded

in G_{mat}. There is also an associated parasitic capacitance (C_{par}) resulting from the ground plane of the PCB which needs to be included in the model along with its associated loss (G_{par}) defined by the same equation as G_{mat}. Additionally, an equivalent series resistance (R_s) is included to account for the conductor losses.

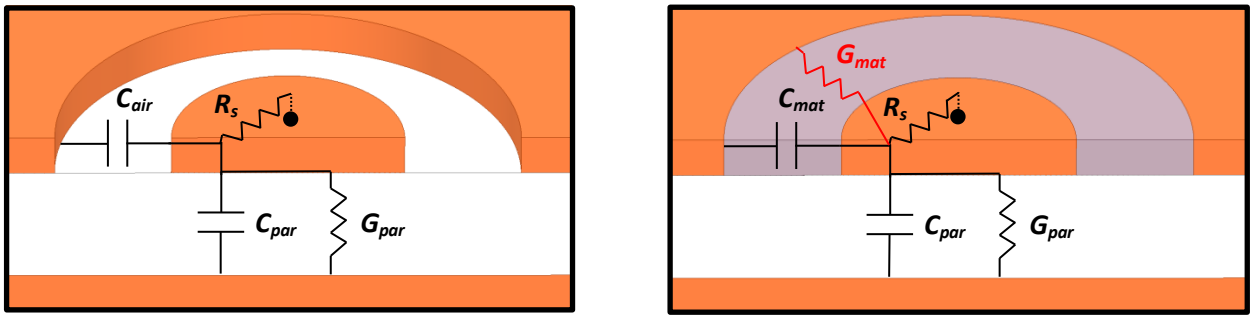


Figure 2.2 - *Equivalent circuit model diagrams of the empty fixture (left) and the filled fixture (right). With material in the gap, there is an additional loss mechanism, G_{mat}.*

The addition of the parasitic capacitance in the model makes it difficult to de-embed the desired parameters of interest. However, if the assumption is made that the parasitic capacitance does not change under any circumstance, then some exploitations can be applied to effectively subtract out the parasitic capacitance. This assumption was applied previously to arrive at the extraction equations that are shown in [4] and [7], derived from the impedance of the structure. This same assumption for the parasitic capacitance will be applied to generate a new set of extraction equations, derived from the admittance of the structure rather than the impedance.

2.3 Modeling Analysis

When a material is present in the gap, there is an additional loss mechanism, G_{mat}, which arises from the loss tangent of that material. The main difference between the empty fixture admittance and the material-filled fixture admittance is between C_{mat} and G_{mat}, where C_{par} and R_s are assumed to be equivalent in both the empty and filled cases. This assumption is made since neither the conductor nor the substrate should be affected by the presence of a material in the gap

of the fixture. If the series conductor loss R_s is assumed to be negligible, then the resulting admittance equations for the empty and filled fixture scenarios are the following:

$$Y_{empty} = G_{par} + j\omega\left(C_{air} + C_{par}\right) \tag{2.4}$$

$$Y_{filled} = G_{mat} + G_{par} + j\omega\left(C_{mat} + C_{par}\right) \tag{2.5}$$

From observation of the provided admittance equations, a note can be made about their similarity, only differing by the material capacitance and conductance terms. Assuming that the parasitic capacitance is the same for both the empty and filled cases, then by subtracting the admittance of the empty fixture from the admittance of the filled fixture, the parasitic capacitance term drops out and the result can be analyzed to derive the equations to extract the dielectric properties of the material in the gap.

$$Y_{filled} - Y_{empty} = G_{mat} + j\omega(C_{mat} - C_{air}) \tag{2.6}$$

Embedded in the imaginary part of this result is the material capacitance, containing the permittivity of material, and embedded in the real part of this result is the material conductance, containing the loss tangent of the material. By taking the imaginary part of this result, the material capacitance can be solved for through some algebraic manipulation. A similar result can be reached for the loss tangent by taking the real part of equation (2.6).

$$Imag\{Y_{filled} - Y_{empty}\} = \omega(C_{mat} - C_{air})$$

$$C_{mat} = \frac{Imag\{Y_{filled} - Y_{empty}\}}{\omega} + C_{air} \tag{2.7}$$

With the material capacitance, equation (2.2) can be rearranged to solve for the permittivity:

$$\varepsilon_r = \frac{\ln(\frac{R_{out}}{R_{in}})}{2\pi\varepsilon_0 h} C_{mat} \tag{2.8}$$

By taking the real part of equation (2.6), only the material conductance term remains:

$$Real\{Y_{filled} - Y_{empty}\} = G_{mat}$$

From here, equation (2.3) can be substituted and the result can be re-arranged to solve for the loss tangent of the material:

$$tan\partial_{mat} = \frac{Real\{Y_{filled} - Y_{empty}\}}{\omega C_{mat}} \tag{2.9}$$

The real part of the fixture admittance contains the loss mechanisms of the structure, and consequently, includes the loss tangent of the material deposited in the gap. This loss tangent is embedded in the additional loss mechanism, G_{mat}, which represents the frequency dependent loss resulting from the presence of a material in the gap. However, this loss term also depends on the capacitance of the material in the gap which can now be calculated with equation (2.7).

By observing the resulting characterization equations (2.8) and (2.9), it can be observed that this method of dielectric parameter extraction is straightforward to perform in practice so long as the admittances of an empty fixture and its corresponding filled counterpart are known. The admittance can be calculated through a 1-port s-parameter measurement and the well-known formulation:

$$Y_{fixture} = \frac{1}{Z_0}\left(\frac{1 - \Gamma e^{-j2\beta l}}{1 + \Gamma e^{-j2\beta l}}\right)$$

In this situation, we are dealing with a one-port structure so the term $\Gamma e^{-j2\beta l}$ is replaced by S(1,1):

$$Y_{fixture} = \frac{1}{Z_0}\left(\frac{1 - S(1,1)}{1 + S(1,1)}\right) \tag{2.10}$$

To summarize, characterization of a printable dielectric material with this fixture requires admittance data for the empty and filled situations. Then, equation (2.7) is used to calculate the capacitance of the material in the gap. From there, the capacitance data is used in equation (2.8) to extract the corresponding permittivity. Finally, using the real part of the admittance data,

along with the calculated material capacitance, the loss tangent of the material in the gap is calculated using (2.9).

2.4 Simulations

In this section, the circular PCB capacitor is modeled using ANSYS EDT 3D modeling and analysis software. The PCB fixture was modeled on a 60mil Rogers RT/Duroid 5870® substrate with 1 oz. copper cladding (35 um thickness). The capacitor has an inner radius of 400 um and an outer radius of 600 um. The goal is to test the proposed extraction method by obtaining two 1-port s-parameter data files from the simulation and employ the formulations found the in the previous section to arrive at a characterization result.

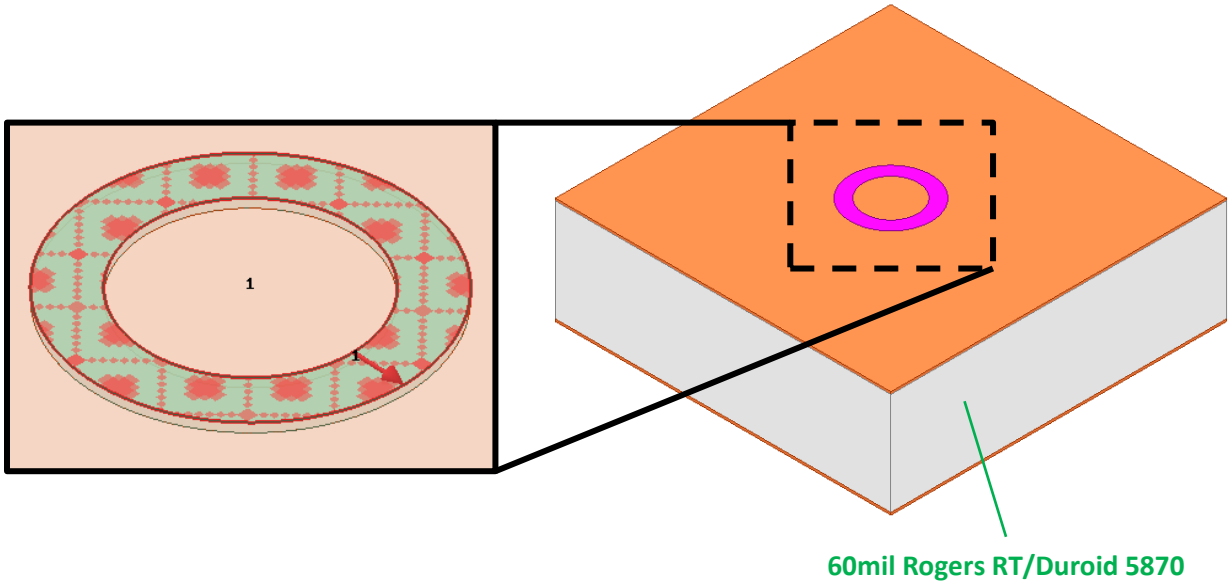


Figure 2.3 - *Model setup in ANSYS EDT with the port definition and integration line shown*

The initial model setup can be seen in figure 2.3 along with the port definition. Since the capacitance of gap was derived from the coaxial transmission line assumption, the port definition resembles the dielectric portion of a coaxial transmission line whose cross-section is parallel to

the surface. The integration line of the port is defined from the edge of the center conductor to the edge of the outer conductor.

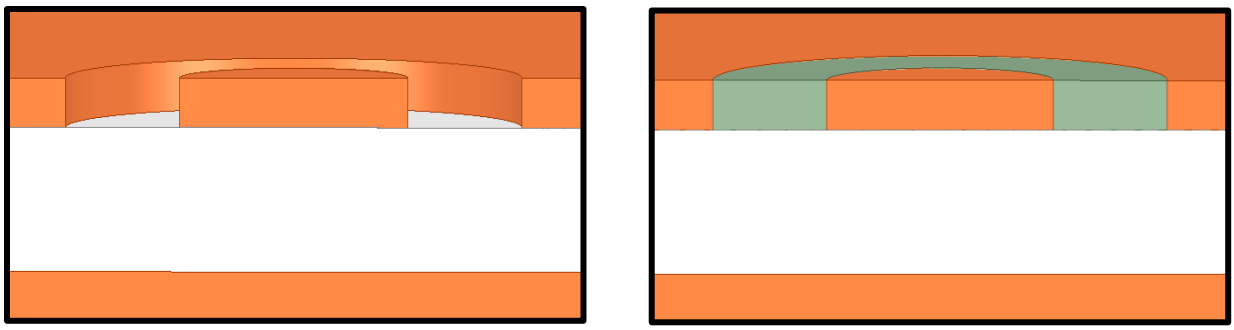


Figure 2.4 - *Cross-sectional view of the empty capacitor used to generate Y_{empty} (left), cross-sectional view of the filled capacitor used to generate Y_{filled} (right). The scaling of the dimensions were altered slightly to aid the visualization.*

Initially, the empty fixture is simulated to generate the s-parameter file that will be used to extract Y_{empty}. Then, a material is modeled into the gap like that shown in figure 2.4 and another 1-port s-parameter file is generated to extract Y_{filled}. The material used in this simulation experiment is ABS, a commonly used 3D printing material. The relatively permittivity and loss tangent were entered into the software as a single scalar value vs. frequency with the goal of being extrapolated with equations (2.7) through (2.9) and the methodology presented in the previous section. The simulations were run from 10 MHz to 15 GHz after which the data was processed through a Matlab script which was used to generate the results shown in figure 2.5. The permittivity value used in the simulation was 2.6 and the loss tangent value used was 0.006. The script used to perform this simulation data processing can be found in Appendix B.

From the resulting dielectric properties data it can be observed that the permittivity profile was relatively close to the expected value that was specified in the simulation, differing by about 7% across the entire simulated band. The loss tangent shows some deviation in the lower frequencies, dipping down to as low as 30% difference around 3 GHz. Overall, the

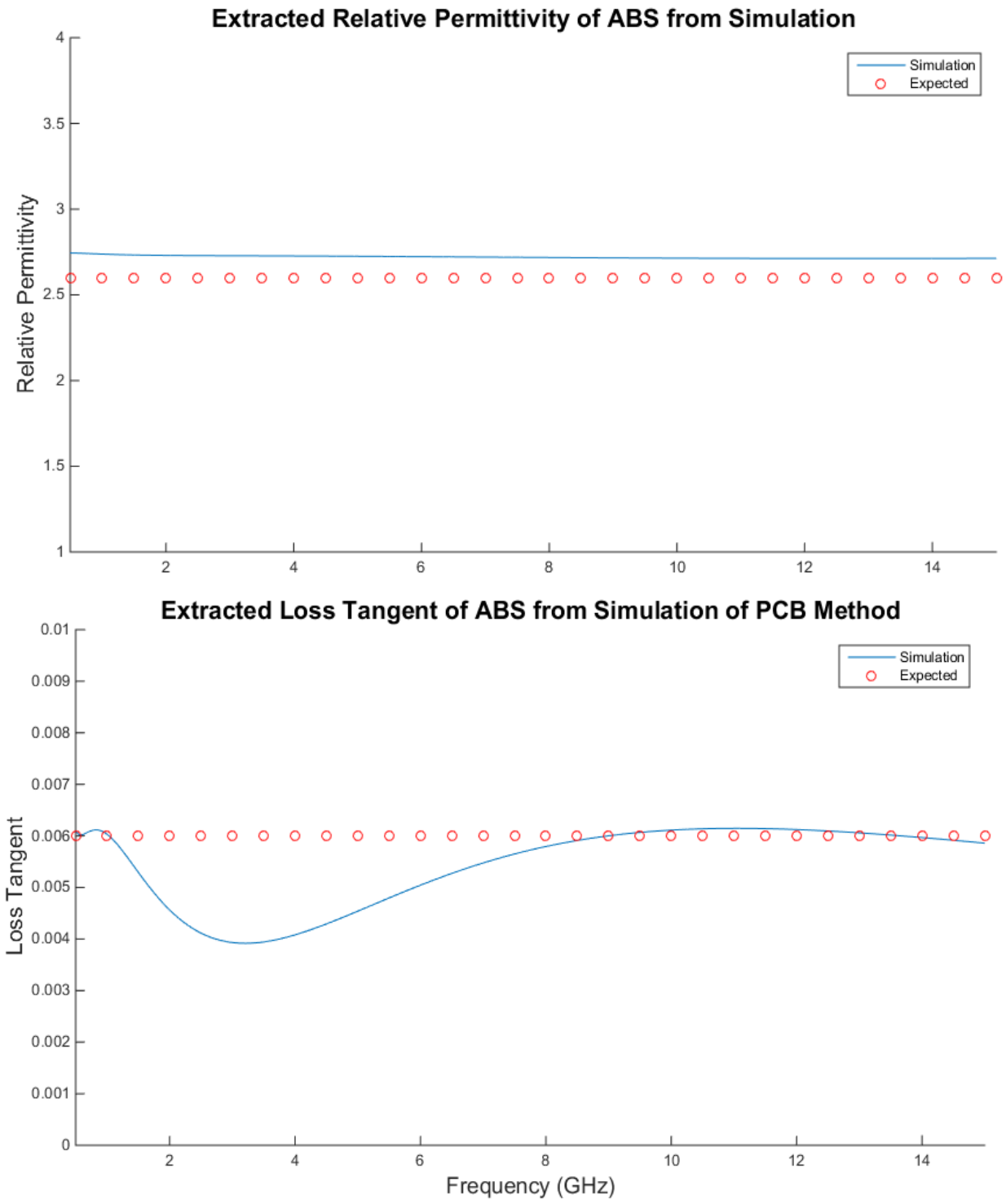


Figure 2.5 - *Results of the PCB extraction method performed on simulation data from ANSYS EDT. The Solid blue line is the extracted dielectric property profile from simulation data processed with a code in Matlab that performs the functions described in section 2.3. The simulation data extraction is compared against the dielectric property profile entered in simulation.*

simulation based extraction results show some promise for the presented method which was able to effectively extract a flat permittivity profile and a loss tangent profile with some accuracy at high frequency.

It should be noted that the situation presented in these simulations thus far is idealistic in the sense that the height of the material in the gap is flush with the height of the copper surface. In reality, the surface of the dried dielectric within the gap will have some roughness to it. Furthermore, the surface of the material in the gap will likely be above or below the surface of the copper by some amount. The capacitance equation for the material in the gap is assuming a squared-off donut shape, perfectly fitting the fixture. Any deviation from this shape will affect the extraction results and such is the case in reality.

2.5 Practical Considerations and Additional Modeling

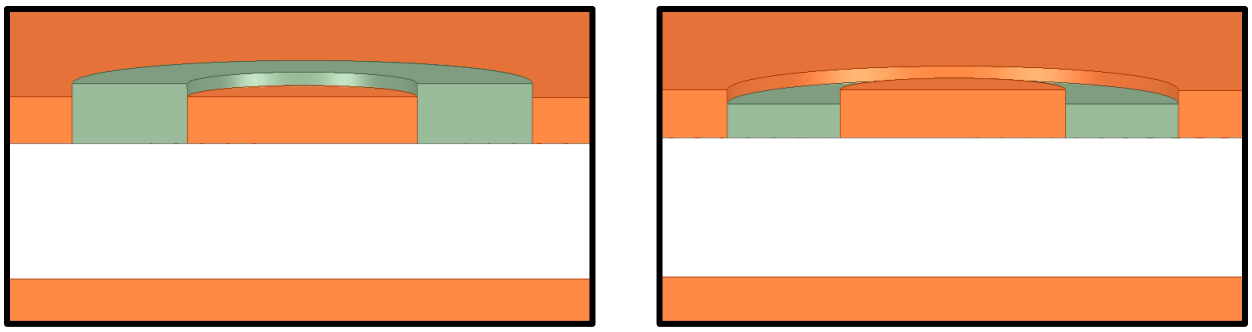


Figure 2.6 - *Depiction of material height and cladding height difference (a) material overflow (b) material underflow.*

In the previous section, the PCB capacitor was modeled assuming that the material in the gap and the conductor cladding have the same height. This assumption allowed the port in the 3D simulation to resemble that of a coaxial line which resulted in relatively simple extraction process for the parameters of interest. In reality, it would be difficult to print material at the exact

height of the conductor cladding, especially in a uniform fashion across the entire gap of the fixture. This section will investigate how the parameter extraction presented is affected as a result of minor differences between material and cladding heights.

The basics of the investigation that is being performed can be seen in figure 2.6 where the material in the gap has a different height level than the cladding. Of course, if the height of the material is lower than the copper cladding, then the same simulation method used previously would suffice, but not if material is higher than the cladding. Practically, a material height above the cladding is a reasonable case to consider, however, the model must be altered to do so.

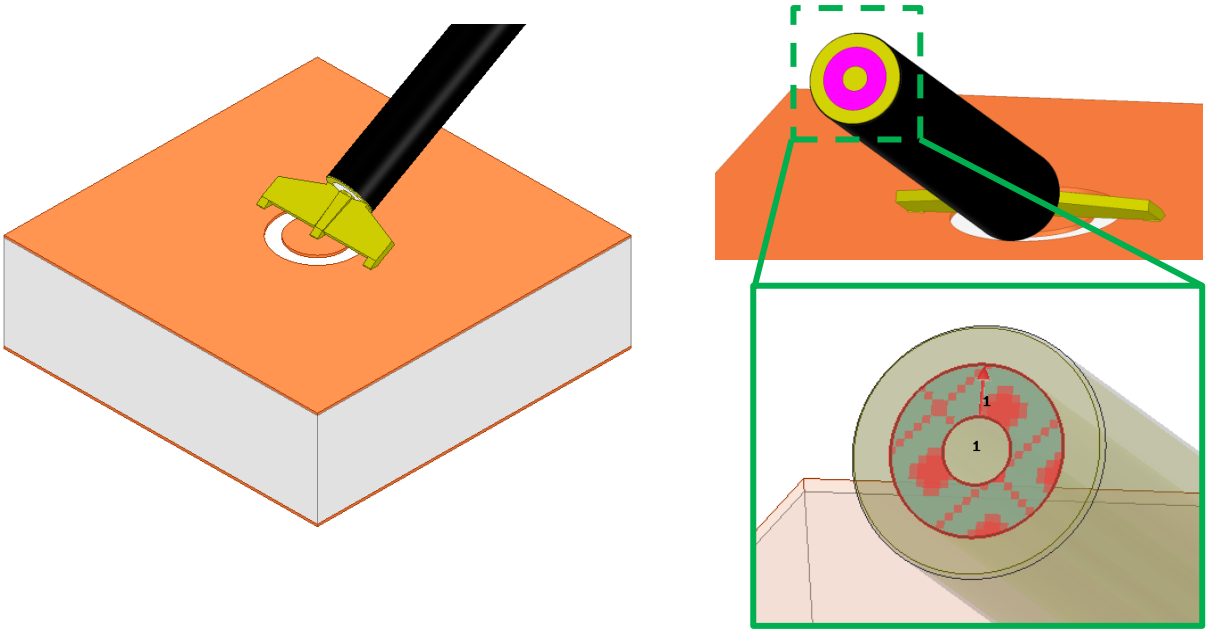


Figure 2.7 - *PCB capacitor modeling setup with a probe included. The port for the simulation was defined as a typical coaxial port on a cross section of the coaxial transmission line of the probe.*

The new setup used to investigate the height differences can be seen in figure 2.7 where there is now a GSG probe included in the model. Here, the port is defined identically to the first case, except now it is located on the coaxial line of the probe. The model presents a challenge in the sense that now there is a probe in the way of extracting the parameters of interest. This is not

a major issue, though, since the probe can be modeled and de-embedded. The first part of the probe is a coaxial transmission line and the second part is a series-shunt LC circuit representing the probe fingers. The 3D model and equivalent circuit model of the probe are both shown in figure 2.8. The probe was modeled after an 850-pitch GGB Picoprobe which was determined as the best sized fit for the given dimensions of the simulated PCB capacitor (details in section 2.4).

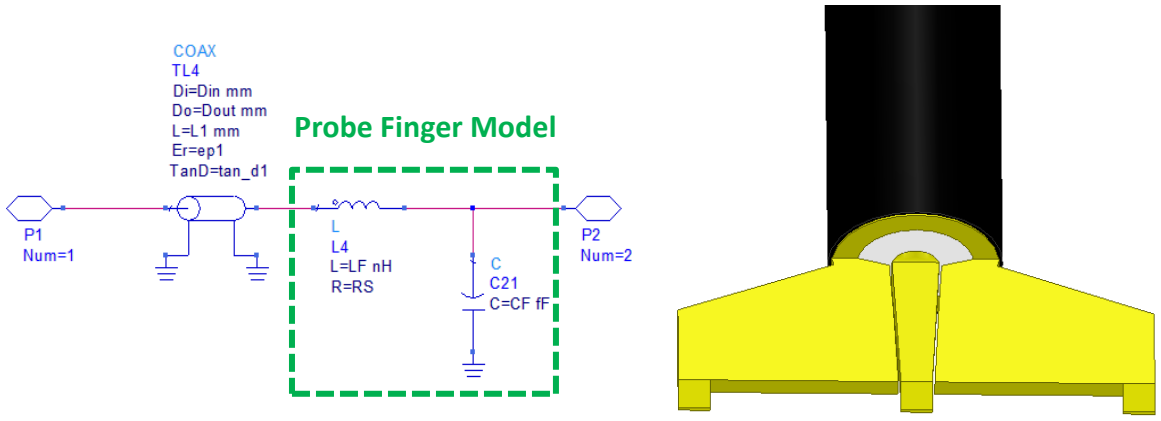


Figure 2.8 - *Equivalent circuit model of the 850-pitch probe used in the simulations. The coaxial portion of the probe is modeled as a coaxial transmission line and the fingers were modeled as a series-shunt LC network.*

To model the coaxial portion of the probe, a 2-port simulation in ANSYS EDT was performed on an equivalent coaxial transmission line 3D model to obtain a 2-port s-parameter file. That data file was then ported to Keysight ADS to create a coaxial transmission line model from the drop-in coaxial element available in the software. The parameters of the coax model were declared as variables that were optimized through simulation. The optimization goals minimized the vector magnitude difference between S(1,1) and S(2,1) of each circuit as shown in figure 2.9. The resulting model parameters are shown in table 2-1.

To create a model for the fixture itself, the circuit model presented previously in section 2.2 is used as the foundation. However, this fixture model now includes a series inductor which

accounts for the inductance resulting from the copper cladding of the fixture. Using the simulation setup utilized previously in section 2.4 where the port was flush with the cladding, simulation data was generated that was then used to construct the model of the fixture. Similarly to the probe model, the fixture simulation data generated in ANSYS is ported to ADS where the optimizer minimizes the vector magnitude difference of the S-parameters between the simulation and the model. Through this method, a model for the empty air-filled fixture and ABS-filled fixture were constructed.

Table 2-1 - *Final values of the parameters for the coaxial transmission line model*

Parameter	**D_i**	**D_o**	**L**	**ε_r**	**$tan\partial$**
Value	**176 um**	**451 um**	**4 mm**	**1.324**	**0.0009**

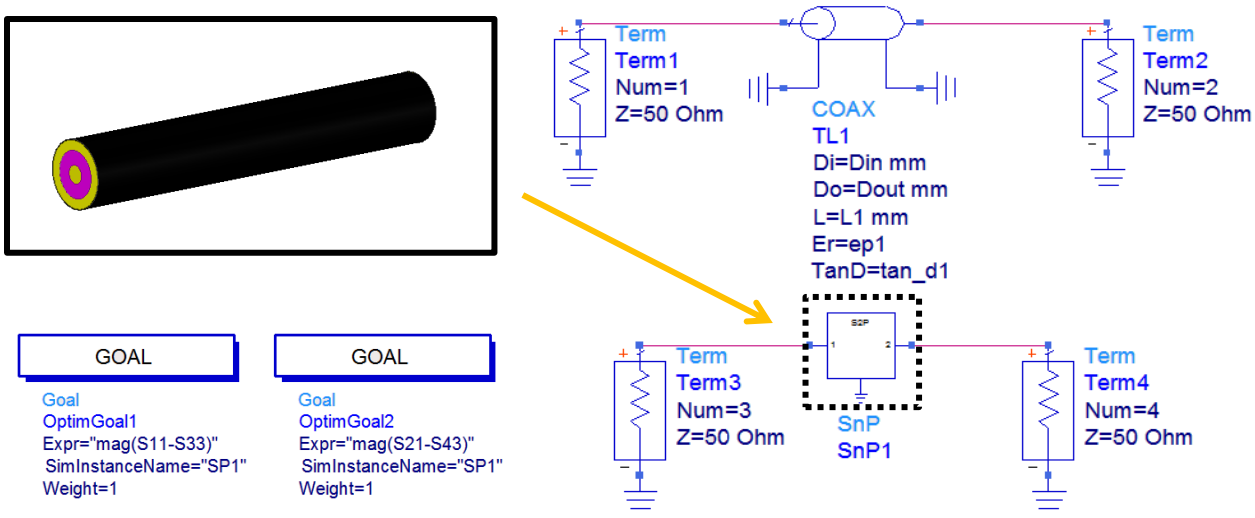


Figure 2.9 - *Modeling approach for the coaxial portion of the probe. The ANSYS EDT simulation data was ported to ADS where the optimizer was used to minimize the vector magnitude difference between S(1,1) and S(2,1) of the circuits.*

The complete model of the probe and fixture can be seen in figure 2.10 where the probe model is being represented by the box labeled "Probe_Model" at the front of the circuit. Since

the probe and the fixture both have an equivalent series resistance, the two were lumped together as the variable R_s on the inductance of the probe fingers as shown in figure 2.8.

The main parameters of interest when building the fixture model are the parasitic inductance (L_{par}) and the parasitic capacitance (C_{par}). The resistance values are defined by equation (2.3) where G_{par} is a function of the parasitic capacitance and loss tangent of the substrate and G_{mat} is a function of the loss tangent of the material in the gap and its associated capacitance. The material capacitance is calculated using equation (2.2) and the loss tangent of the substrate and material are entered as known information.

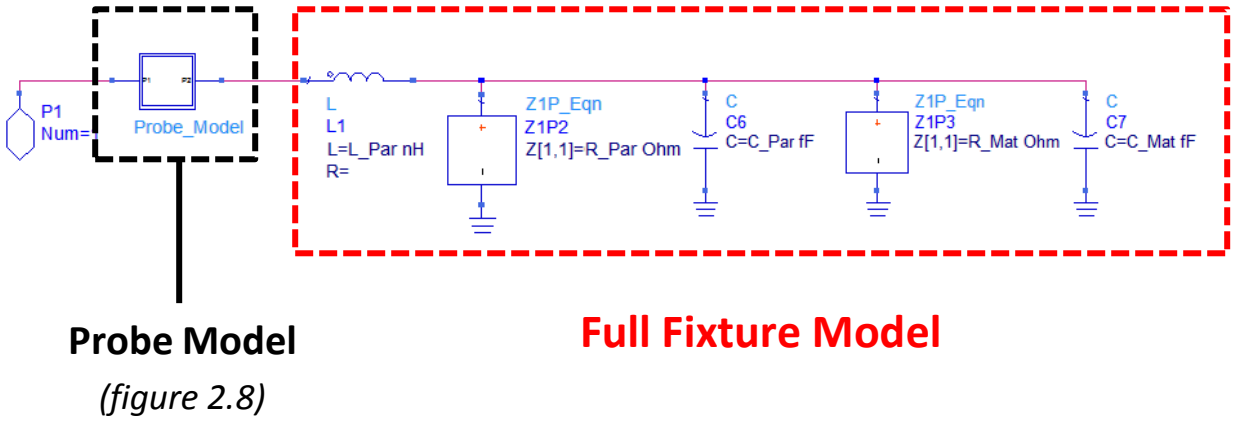


Figure 2.10 - *The full model of the PCB capacitor with probe simulation setup.*

Through the same vector magnitude difference optimization method utilized previously, two full fixture models were developed for the air-filled and ABS-filled situations where the final values of the optimized parameters can be seen in table 2-2. From the final results shown in the table, it can be seen that the assumption about the parasitic capacitance being the same between empty and filled scenarios holds true as the values ended up almost identical in both cases. The parasitic inductance resulting from the copper cladding was also found to be identical in both scenarios, as would be expected.

Table 2-2 - *Values used in the model as well as final optimization values for optimized parameters L_{par} and C_{par}.*

Material	ε_r	$\tan\partial_{mat}$	C_{mat}	C_{par}	L_{par}
Air	***1***	***0***	***2.33 fF***	***215 fF***	***12.7 pH***
ABS	***2.6***	***0.006***	***6.06 fF***	***217 fF***	***12.7 pH***

With the equivalent model shown in figure 2.10, data from the improved simulation setup (shown in figure 2.7) can be utilized to generate an effective model of the complete setup. The inductance and capacitance values for the probe fingers are still unknown at this point; however, the model for the fixture is known and a coaxial model has been built for the probe. Using the air-filled and ABS-filled fixture models built previously in conjunction with the coax model, the simulation data generated by the setup shown in figure 2.7 is ported to ADS and optimizations are run to match the two models to the two simulation data files. Since the only variables left are the probe inductance and capacitance, these variables are optimized exclusively and a complete model is established. The results of this optimization for the final values of the probe finger circuit elements are shown in table 2-3.

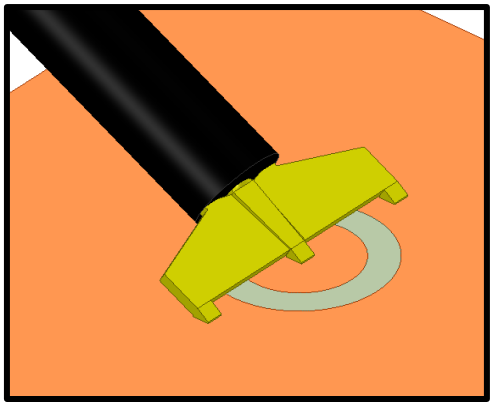
Table 2-3 - *Final values of the circuit elements representing the probe fingers for the probe model.*

Parameter	C_f	L_f
Value	**6.22 fF**	**58.9 pH**

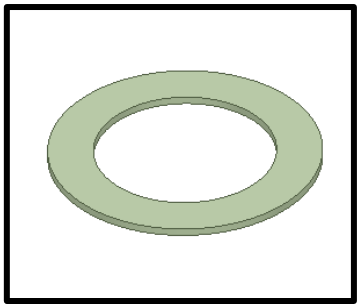
2.6 Model Testing

By identifying the values of the circuit elements representing the probe fingers, the model of the simulation setup in figure 2.7 has been completed. To test this model, the material properties of air and ABS are extracted through de-embedding the fixture parasitics and probe

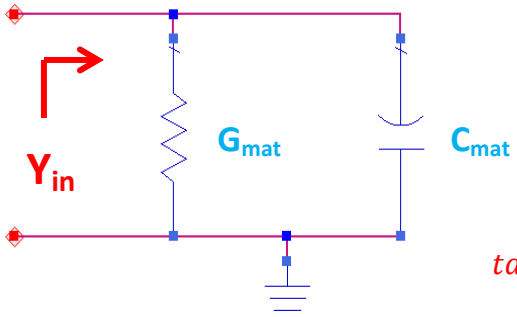
model. After de-embedding the probe and fixture parasitics, the only part that remains is the donut shaped volume of the gap which contains the material properties as shown in figure 2.11. An analysis of the input admittance of this de-embedded result will provide the dielectric parameters of interest.



Probe and fixture parasitics de-embedding



Model of resulting donut shape



$$Y_{in} = G_{mat} + j\omega C_{mat}$$

$$C_{mat} = \frac{Imag\{Y_{in}\}}{\omega}$$

$$G_{mat} = Real\{Y_{in}\}$$

$$tan\partial_{mat} = \frac{Real\{Y_{in}\}}{\omega C_{mat}}$$

From equation (2.3)

$$\varepsilon_r = \frac{\ln(\frac{R_{out}}{R_{in}})}{2\pi\varepsilon_0 h} C_{mat}$$

From equation (2.2)

Figure 2.11 - *Visual representation of the effect of de-embedding the probe and fixture models from the simulation data. After the de-embedding process, all that remains is the squared-off donut-shaped gap that contains the material circuit elements: C_{mat} and G_{mat}.*

The assumption is that the resulting donut shape is a two-element circuit where the input admittance (Y_{in}) is a function of G_{mat} and C_{mat}, the parameters bearing the dielectric properties of interest. With this assumption the material capacitance can be solved for by taking the imaginary

part of the input admittance and performing some algebra. With this capacitance, the resulting permittivity can be calculated with (2.2). The loss tangent is embedded in the real part of the admittance. However, the assumption here is that the real part of the input admittance is equal to G_{mat}; therefore, equation (2.3) can be substituted accordingly and the result can be rearranged to solve for the loss tangent.

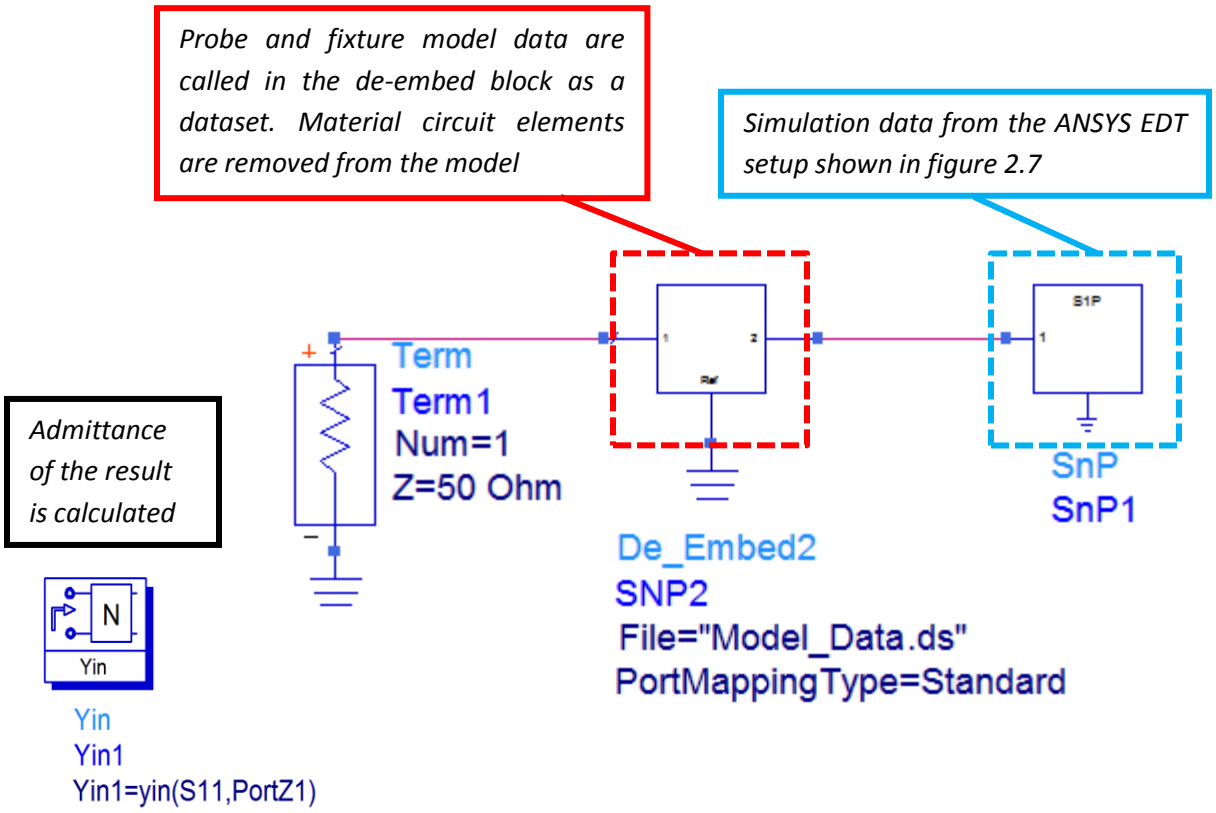


Figure 2.12 - *De-embedding process to extract dielectric properties from the PCB fixture and probe simulation setup. The resulting input admittance is calculated and the dielectric parameters are extrapolated.*

The schematic used for the de-embedding process is shown in figure 2.12 along with some description on how the process is laid out. The simulation data from the complete setup in figure 2.7 is fed into the block on the right hand side of the schematic. The de-embedding box to the left of the simulation data contains the model parameters (minus the circuit elements

representing the material). The resulting S-parameters of this circuit are converted to admittance values which are analyzed to extract the dielectric properties of the material in the gap through the analysis method shown in figure 2.11.

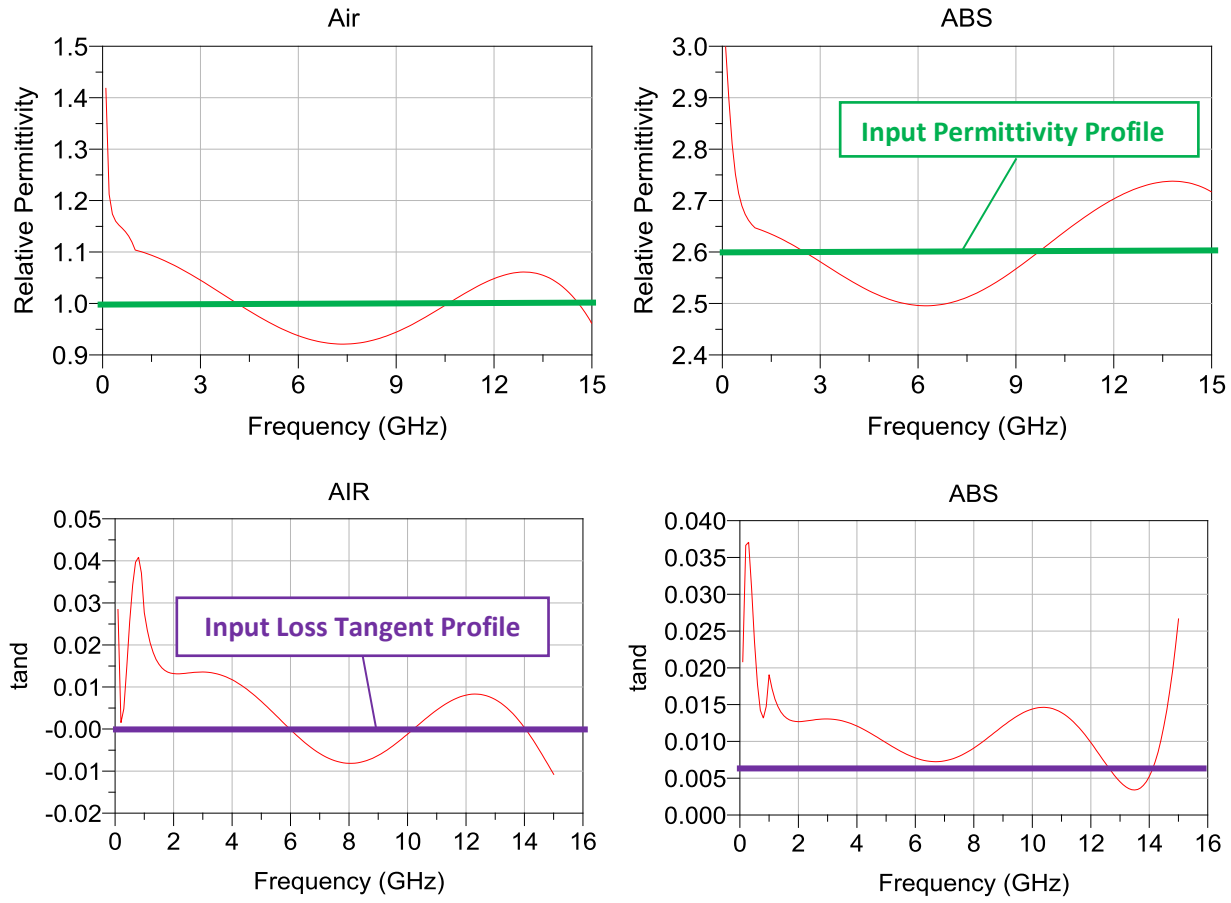


Figure 2.13 - *Results of the extracted permittivity and loss tangent through de-embedding the probe and fixture parasitics then analyzing the resulting admittance.*

The results of the admittance analysis of the de-embedded simulation data can be seen in figure 2.13 where the permittivity and loss tangent profiles are plotted vs. frequency. From the data, it can be observed that the loss tangent extraction of ABS has improved from the last attempt, particularly from 0.1-12 GHz. The permittivity extraction results are now within ±4% of the expected value, an improvement from the 7% difference seen with the previous attempt.

However, in both cases there are some parasitics that were not effectively modeled and are revealing themselves as oscillations around the expected result.

2.7 Material Height vs. Cladding Height Analysis

With a model of the PCB fixture developed, an additional advanced analysis can be performed. In this section, an investigation is conducted where the height of the material within the gap is varied to observe the effects on the extraction of the dielectric properties. Different material height levels were chosen with respect to the cladding height, some above and some below. The relative height values chosen for this analysis were: 3 um, 1 um, 0 um, -1 um, and -3 um where 0 um represents the material height being equal to the copper cladding height and the negative values represent a material height below the cladding height. A visual representation of what is being described can be seen in figure 2.6.

By running the simulation setup with the material in the gap at the relative heights mentioned, a series of s-parameter files are generated. Then, each s-parameter file is put through the de-embedding process described in the previous section. The results of the extracted permittivity and loss tangent for these different situations are shown in figure 2.14 where the red line represents the condition where material height is equal to the cladding height (results from the previous section).

From inspection of the results, it can be observed that the height of the material within the gap should be carefully controlled. Any deviation from the perfect donut shape results in a respectable difference in extracted dielectric properties. This is an important consideration in practice, primarily because the material and the cladding are typically not going to be at the exact same height, and especially not in a uniform fashion throughout the gap. Surely, there will be some roughness in the dielectric, resulting in slight deviations from the perfect donut shape.

However, this is also assuming that the material was printed at the exact height of the cladding which is difficult in practice; especially considering 1oz cladding which is only 35 um thick. Rather, it would be simpler to print an overflow situation, and then sand down the excess solidified dielectric to make the cladding flush with the material surface.

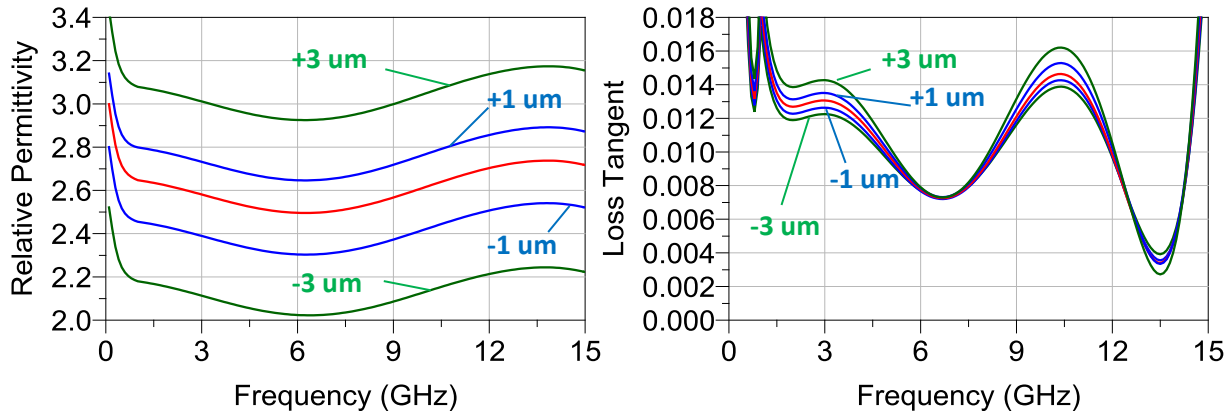


Figure 2.14 - *Permittivity and loss tangent extraction results for different material heights with respect to the cladding height. Relative values were selected above and below the surface where the ideal case, 0 um, is shown in red.*

The simulations performed in this analysis revealed that any deviation from the ideal situation where the material perfectly fits the cavity has its consequences. Just one micron difference between the two heights results in roughly 8% difference in extracted permittivity and 30% difference in extracted loss tangent at 3 GHz. Such a deviation would be very easy to achieve in practice, highlighting an important consideration when using this characterization method. Additional measures should be taken to ensure that the material height and the cladding height are equal to ensure the least possible extraction difference.

2.8 Measurements

In this section, the proposed circular PCB capacitor method of dielectric characterization is tested through measurement of fixtures loaded with dielectric ink. The capacitors were prepared by a copper etching process on Rogers 5870 substrate with 1oz. copper cladding (35

um). The resulting copper etched fixture is shown in figure 2.15 along with a fixture that has been filled with a dielectric. To begin the characterization of dielectric inks with this method, first the fixtures that will be used in the characterization should be selected and measured for their inner and outer radii. For this analysis, a sample set of five fixtures were chosen whose dimensions are listed in table 2-4. The dimensions of the fixtures were obtained through microscope measurements with a calibration slide. From the table, some spread in the dimension values can be observed as a consequence of the etching process.

Table 2-4 - *Values of the inner and outer radii of the fixtures used in the characterization study.*

Parameter	Fixture 1	Fixture 2	Fixture 3	Fixture 4	Fixture 5
R_{in}	*356.4 um*	*357.7 um*	*359.1 um*	*344.3 um*	*345.6 um*
R_{out}	*557.4 um*	*571.7 um*	*564.0 um*	*569.4 um*	*566.7 um*

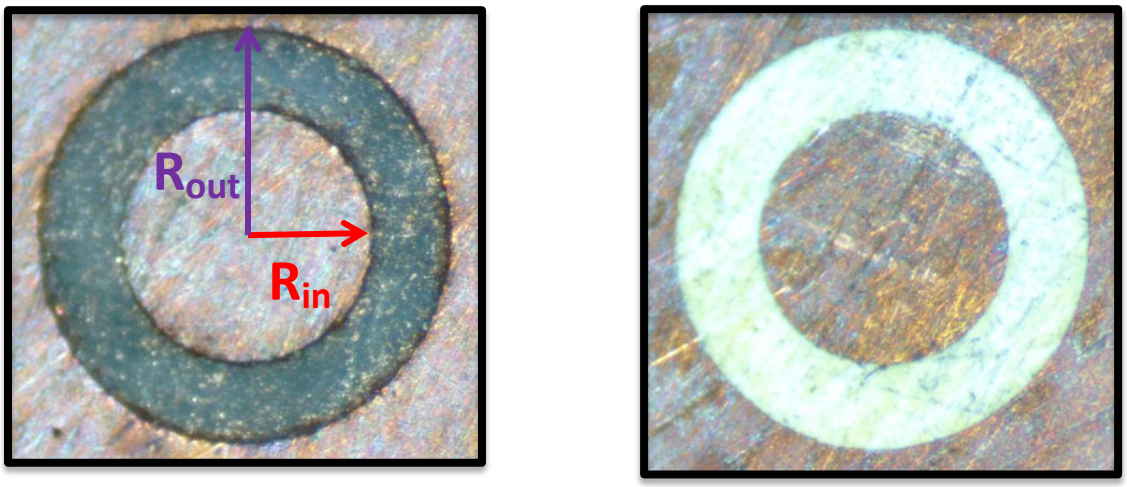


Figure 2.15 - *Empty air-filled fixture (left) and its corresponding dielectric-filled counterpart (right).*

With the fixtures selected and dimensions measured, the next step is acquisition of the s-parameter data of the empty fixtures. First, a good one-port probe-tip calibration must be achieved on the vector network analyzer that is desired to be used for the measurement. With an

acceptable calibration on the VNA, the air-filled fixtures are measured for their one-port S-parameters which will later be used to calculate Y_{empty}. Then, the fixtures are taken to the nScrypt printer where the dielectric ink that is desired to be characterized is printed within the gap. Since the dielectric ink requires curing, the samples are placed in an oven where the residual solvent within the ink evaporates out as the dielectric bulk solidifies. The resulting samples are then taken back to the VNA with the previous calibration that was used for the air measurements, and a new set of measurements are taken of the material filled fixtures.

Based on the result of the advanced simulation modeling in the previous section, the material in the gap of the samples should be sanded down to the level of the copper cladding prior to the second set of measurements to reduce the amount of deviation in the extraction that results from mismatching height levels. In practice, it is easy to print above the level of copper cladding due to physical limitations of the minimum thickness of dielectric material that can be printed.

The measurements of the PCB capacitor samples were made on a Keysight ENA Series Network Analyzer which was calibrated from 10 MHz to 18 GHz. There are 401 points in the measurement and an averaging factor of 16 was used. The samples were measured with an 850-pitch GGB Picoprobe that was calibrated out to the probes tips using a CS-10 calibration substrate.

After sanding down the samples and measuring them for S-parameters, the data was processed using the same MATLAB script utilized previously (found in appendix B). The results of this measurement-based extraction performed the dielectric ink can be found in figure 2.16 where the data is being compared to characterization results from two Damaskos cavity

resonators that cover a similar bandwidth. The details of the dielectric characterization process of the ink with the Damaskos cavities can be found in appendix A.

The resulting permittivity and loss tangent from the five PCB capacitor samples is consistent with the exception of the sample 5 permittivity profile which differed from the other samples by about 25%. Upon further investigation, it was found that the dielectric appeared to have a slightly over-sanded surface with respect to the other samples. Additionally, the surface of the dielectric had a characteristic air bubble. As a result of these surface impurities, the measured dielectric bulk is now a combination of the dielectric and air, resulting in a lower-than-average dielectric constant and loss tangent extraction.

The results of the measured extraction show that the presented method can be a quick and useful way to screen a dielectric ink for its characteristic properties. With the exception of sample 5, the permittivity results were accurate up to about 10 GHz. The other four samples had extracted permittivity values that were within ±8% difference of the expected value from 2-10 GHz. The loss tangent results of the first four samples from 2-8 GHz differed from the Damaskos results by about 50% from 2-8 GHz. In the same frequency ranges, sample 5's permittivity extraction differed from the Damaskos results by roughly 20% and the loss tangent extraction differed by about 70% as a result of its characteristic surface impurities. At around 9 GHz, the loss tangent extraction begins to deviate, indicating a potential limitation with this method. The permittivity extraction appears to be valid over a slightly wider bandwidth, but unfortunately starts to deviate around 12 GHz. Certainly, the samples did not achieve the 1-20 GHz characterization that was set out to be achieved.

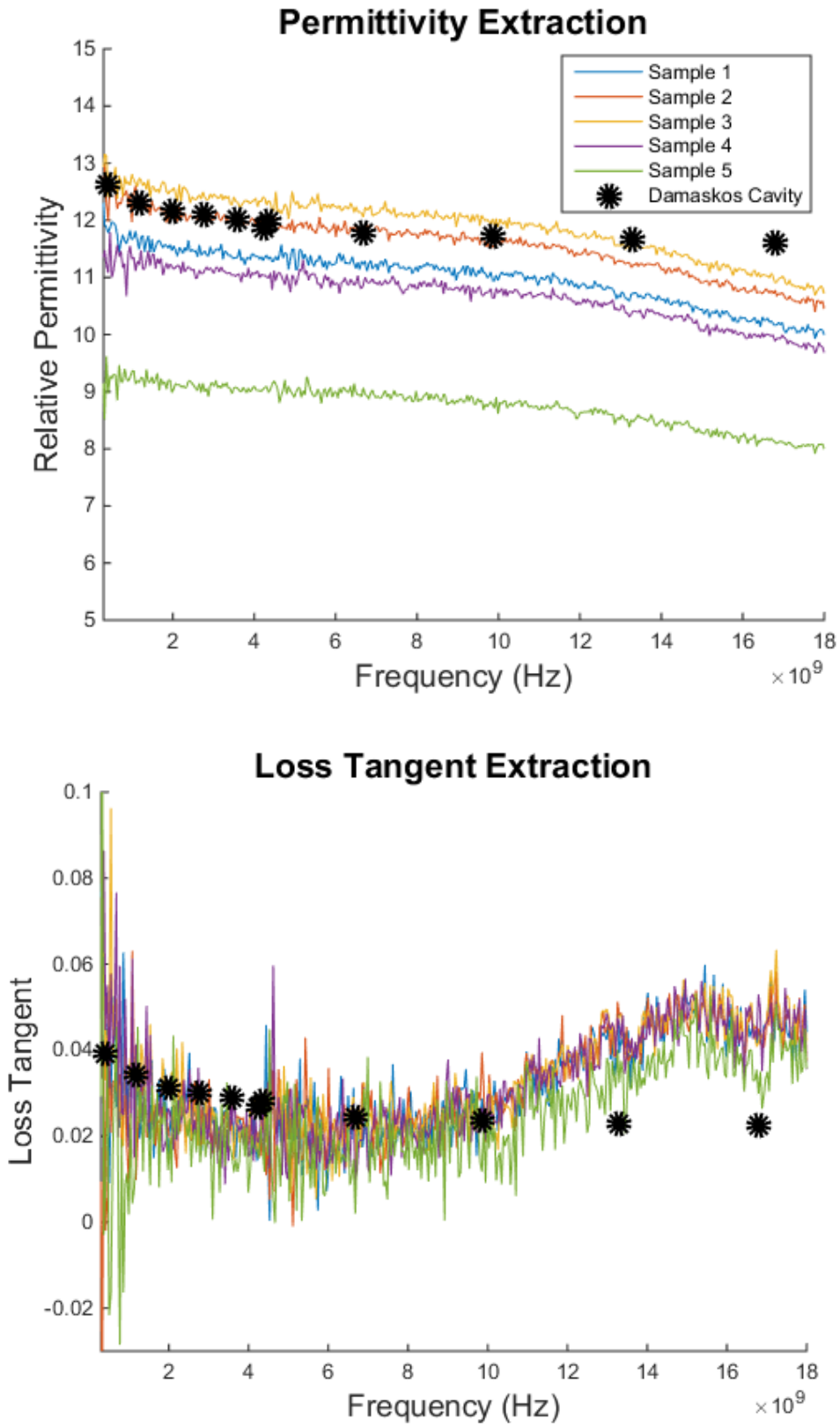


Figure 2.16 - *Results of the measured PCB capacitor extraction of dielectric properties compared to Damaskos results. Five samples were prepared with dielectric ink 1in the gap.*

2.9 Temperature and Humidity Testing

In the previous section, PCB capacitor samples were measured for s-parameter data which was used to extract the dielectric properties of the material in the gap. As an added analysis, those samples are put through a long-term temperature and humidity test to observe the effect on the dielectric material and PCB characterization process. The environment inside the chamber is held at a constant 85ºC and 85% relative humidity. At certain checkpoints, the samples are removed and measured for s-parameter data which is used to perform the extraction process for dielectric permittivity and loss tangent demonstrated in the previous section. The test is performed in a CSV Micro Climate Temperature and Humidity Chamber for a duration of 1000 hours. After 150 hours, the samples were removed and measured for S-parameters then placed back in the chamber to complete the 1000 hour cycle. The samples are measured again at the end of the 1000 hours.

After one week inside the temperature and humidity chamber, the samples were removed and measured for S-parameters. This s-parameter data is converted to admittance data and analyzed with equations (2.7)-(2.9) to extract the dielectric properties of the material in the gap. The resulting permittivity and loss tangent profiles are shown in figure 2.17 along with the Damaskos cavity data from Appendix A.

After 150 hours inside the testing chamber under the conditions described, the samples were removed and measured for S-parameters. This s-parameter data was used to extract the dielectric properties profile as previously demonstrated. As a result of this 150 hour testing process, the extracted permittivity profile of the samples decreased collectively as all of the samples now have permittivity profiles that fall below the Damaskos results 2-18 GHz.

Additionally, the extracted permittivity profiles of the samples do not have as much spread between them as they did before the 150 hour test.

When the samples were recovered from the chamber, there were small pools of standing water around the samples and the surrounding copper cladding was entirely oxidized. Some sanding was performed to eliminate the oxidation layer before proceeding with the s-parameter measurements of the samples. This sanding process could have resulted in unintentional sanding of the dielectric surface causing the level of the material surface to descend relative to the level of the copper cladding surface. Recalling the results of the material vs. cladding height analysis in section 2.7, the unintentional sanding of the dielectric material surface would lower the extracted permittivity.

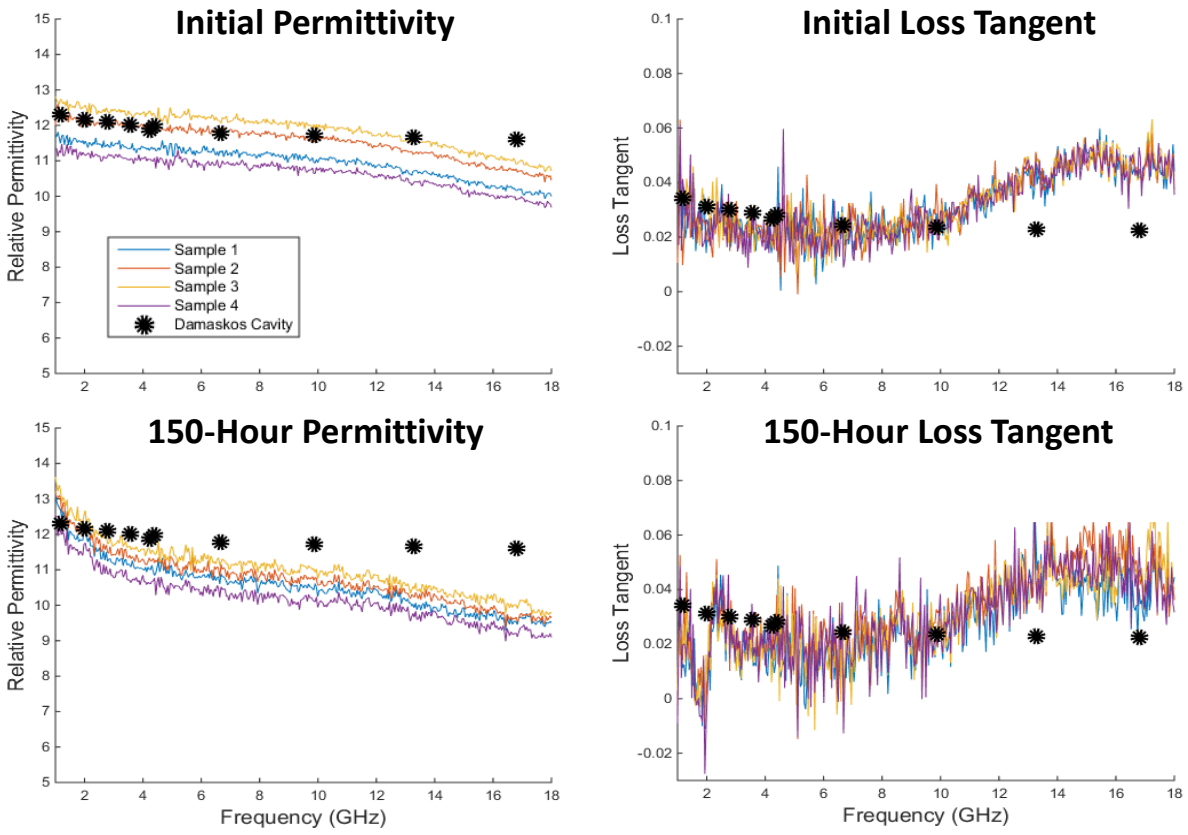


Figure 2.17 - *Results of the 150 hour temperature and humidity test at 85ºC and 85% relative humidity. Initial PCB capacitor extraction results are included for reference.*

After 1000 hours inside the chamber, the samples were removed and lightly sanded to eliminate the oxidation while trying to preserve the dielectric material height level. Upon examination of the samples, the dielectric in the gap appeared deformed. Under a microscope, there was a noticeable difference between the material and copper cladding height levels. To investigate, some profile measurements were taken of the samples which revealed that there was an additional micron or two of height difference between the dielectric material surface and cladding surface on average across all of the samples that was not present before the chamber testing. It is possible that the dielectric material suffered from some shrinkage as a result of the chamber environment. The extracted permittivity and loss tangent profiles of these samples after the 1000-hour test are shown in figure 2.18 along with the 150-hour test data for reference.

The extracted permittivity profiles of the samples further decreased collectively with respect to the results of the 150-hour test. This was expected, considering the observations made of the samples dielectric surface profile. The amount of deviation in permittivity is consistent with the results of the cladding vs material height analysis. Sample 1 had a dielectric surface which was roughly a micron below the cladding and resulted in about 9% permittivity deviation. Additionally, the loss tangent results are trending lower than before, especially at the high frequencies. Now the samples extracted loss tangent is closer to that measured by the Damaskos cavities from 10-16 GHz.

It cannot be overlooked that the samples had to be sanded down each time they were measured due to the presence of oxidation on the cladding after each test. Each sanding attempt could have chipped away at the dielectric material surface, contributing to the difference between material and cladding height levels and lowering the extracted permittivity. This could also be the reason why the spread between the samples decreased after each trial. The repeated sanding

could have resulted in samples with dielectric heights at similar levels. After the 1000-hour test, it can be concluded that the samples suffered some sort of damage or deformation either from the environment or as a result of the sanding process, or both.

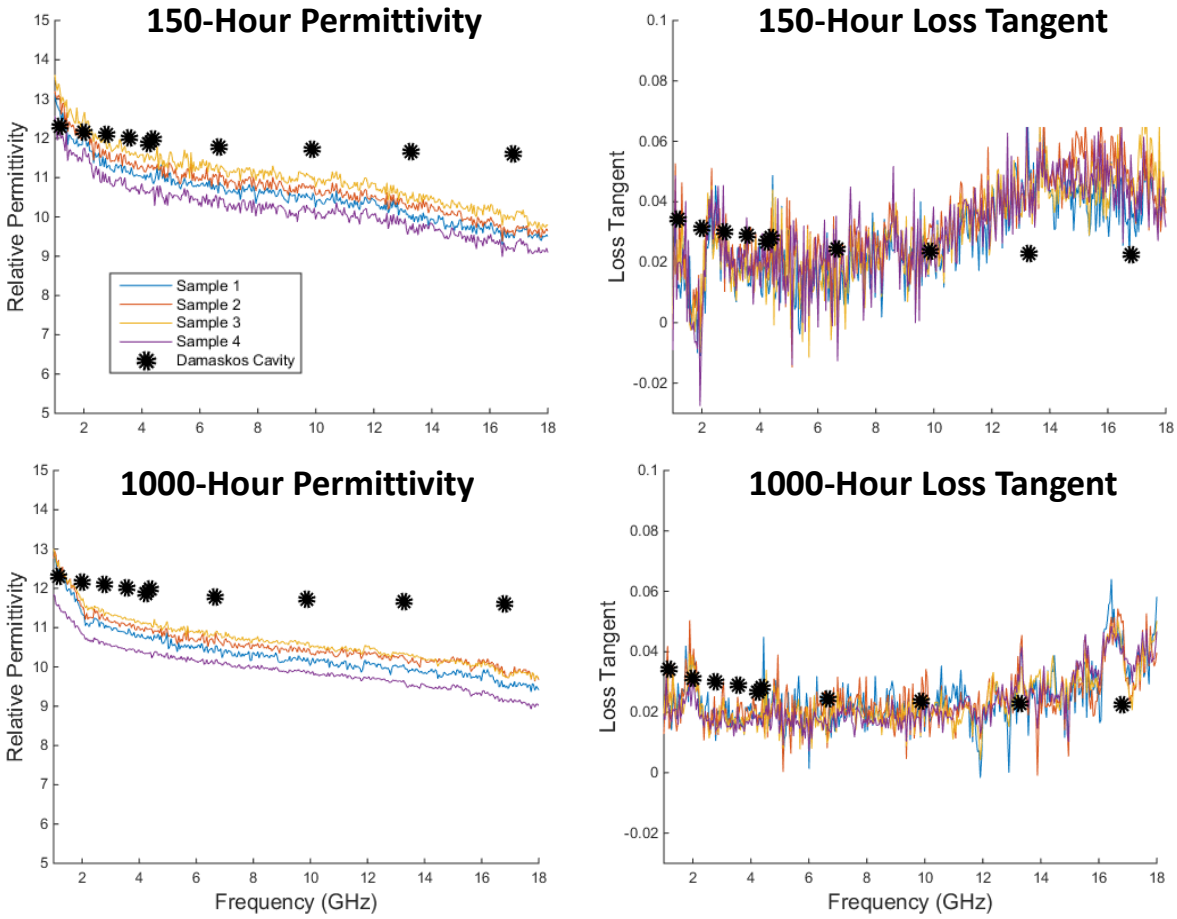


Figure 2.18 - *Results of the 1000-hour temperature and humidity test at 85ºC and 85% relative humidity. One-week extraction results are included for reference.*

2.10 PCB Capacitor Gap Length Analysis

Up to this point, only a particular set of PCB capacitors have been studied which have similar inner and outer radii dimensions. In this section, a set of PCB capacitors with larger gap sizes are utilized to perform the presented extraction method conducted in section 2.8. The goal is to observe how the increased gap size affects the results of the extraction of dielectric

properties. The samples that were chosen as for larger gap size analysis are shown in table 2-5. From the table, it can be noted that the samples have a very similar inner radii to the previously characterized smaller gap samples. However, these new samples have gap sizes that are 320 um on average. This is 52% larger than the previous samples which had an average gap size of 210 um.

Table 2-5 - *Values of the inner and outer radii of the fixtures used in the larger gap analysis.*

Parameter	Fixture 1	Fixture 2	Fixture 3	Fixture 4
R_{in}	*322.5 um*	*337.1 um*	*334.0 um*	*328.6 um*
R_{out}	*639.3 um*	*664.3 um*	*658.5 um*	*644.4 um*

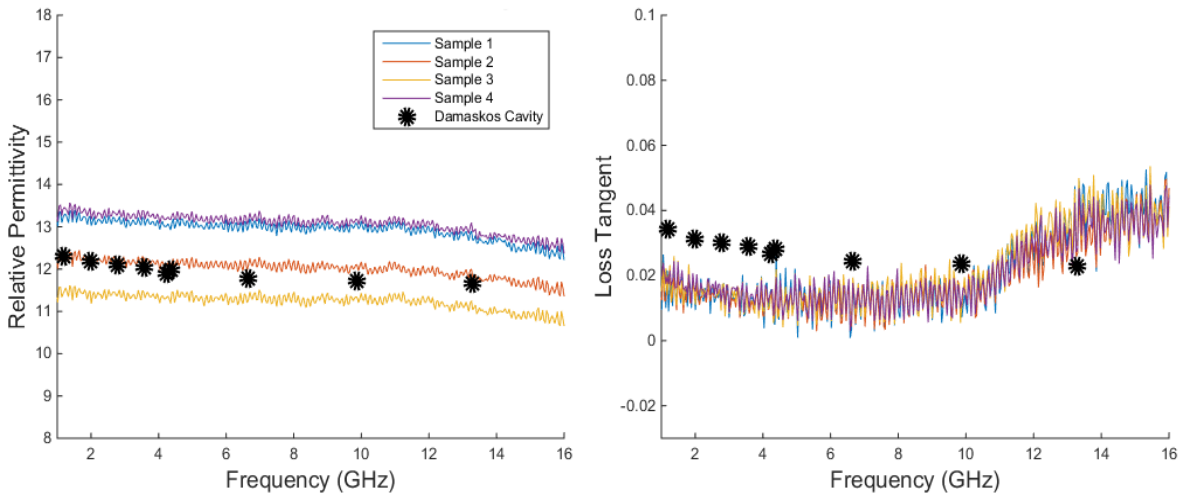


Figure 2.19 - *Resulting permittivity and loss tangent profiles extracted using the PCB method on samples with a larger gap size.*

The preparation of the samples and s-parameter measurement process performed to characterize these samples is identical to that which is detailed in section 2.8. The dielectric material dispensed in the gap of the samples is the same as used previously and was cured under

the same conditions. The resulting extracted of permittivity and loss tangent from the s-parameter data of the measured larger gap samples are shown in figure 2.19.

The PCB extraction method with the larger gap samples shows more spread in the permittivity results than the previously conducted extraction attempt with the smaller gap samples. Additionally, the larger gap PCB samples have extracted permittivity profiles that are larger on average than the smaller gap samples. The average of the extracted loss tangent of the larger gap samples at the lower frequencies is between 0.015-0.017. This is over 30% lower than the previously extracted average of 0.025 achieved with the smaller gap samples. The plots of the calculated average permittivity and loss tangent profiles for both sets of samples are shown in figure 2.20 compared against the Damaskos results.

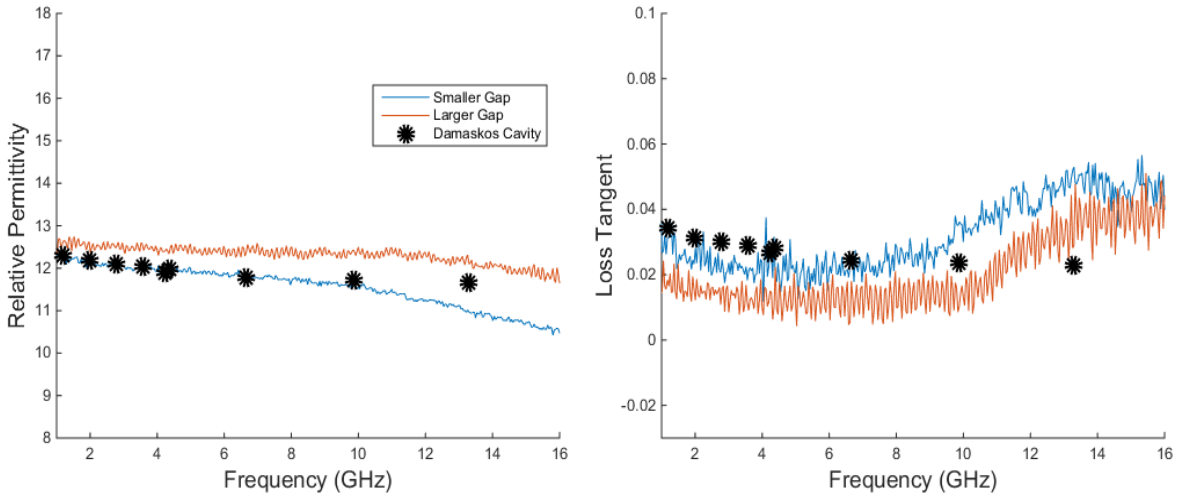


Figure 2.20 - *Average extracted permittivity and loss tangent profiles through the PCB method with fixtures of different gap sizes. Results of the extraction are compared to results of characterization of the material with Damaskos cavity resonators.*

By increasing the gap size, the capacitance of the PCB capacitor structure is decreased which increases the input impedance seen in a measurement scenario. One possible reason for the increase in the spread between the extracted permittivity profiles with the larger gap samples

comes from the fact that the samples have a larger impedance seen in measurement. According to Agilent's Impedance Measurement Handbook, s-parameter measurements should be made on fixtures with a magnitude of impedance that is within 1-200 Ω to guarantee results within 10% measurement accuracy [8]. Figure 2.21 shows the typical impedance magnitudes seen by PCB samples loaded with dielectric ink. From the figure, it can be observed that the increased gap size results in an increased measured impedance magnitude, drifting away from the desired range of impedance magnitude desired for s-parameter measurements. Thus, increasing the gap size of the fixture introduces the potential for larger measurement error.

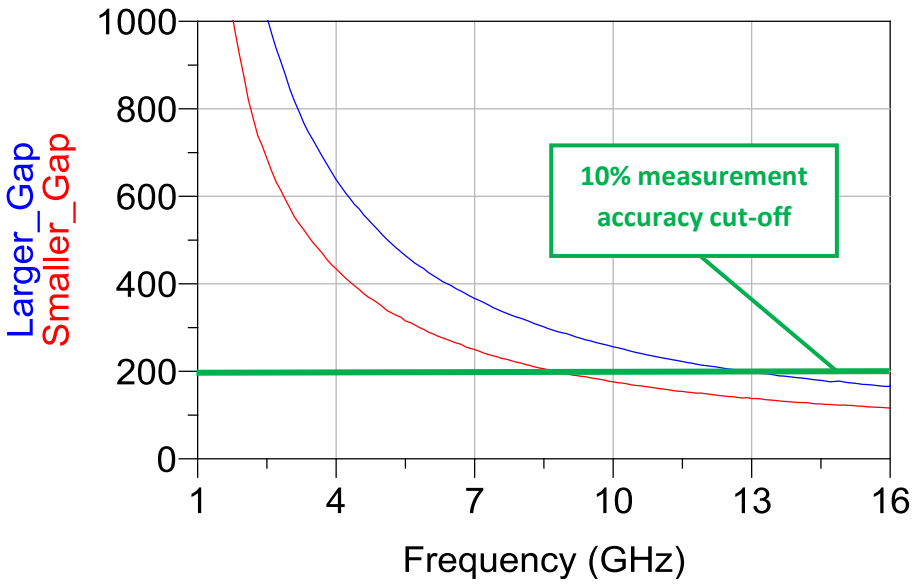


Figure 2.21 - *Typical impedance magnitude seen from a material-filled PCB fixture in practice: red – smaller gap, blue – larger gap. The measured impedance magnitude should be within the 1-200 Ω range for an effective s-parameter measurement.*

Overall, the PCB extraction method is straightforward to perform, requiring a two sets of admittance data and a couple equations to reach a result. However, the fixtures must be prepared through an etching process resulting in fixtures of variable gap sizes, and thus, variable and uncontrollable impedances. Additionally, the capacitance of the structure was found to be as

small as a few femtofarads which yields high magnitude input impedances seen by the measurement out to several gigahertz. This was found to be problematic for s-parameter measurements which require the measured impedance to fall within a particular range for reliable accuracy.

Increasing the gap size of the fixture resulted in a wider spread of extracted permittivity results and lower than average loss tangent extraction. The smaller gap fixtures were found to be more effective for characterizing the dielectric material, showing ±8% difference in the permittivity results from the expected Damaskos results from 2-10 GHz, but still about 50% difference in loss tangent at low frequency. The lost tangent extraction was found to be effective out to about 10 GHz before deviating away from the Damaskos results.

CHAPTER 3: DPAM PARALLEL PLATE CHARACTERIZATION METHOD

3.1 Introduction and Background

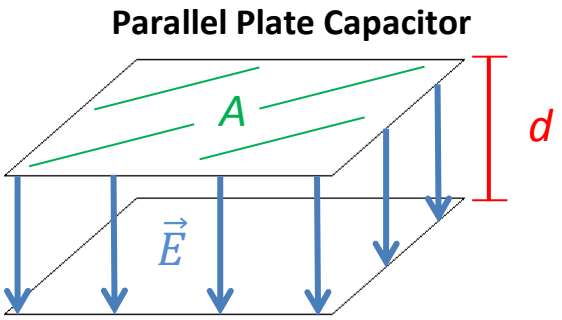
In the previous chapter, a method of dielectric characterization is introduced that is simple to perform, but has some drawbacks. One drawback is the fixture is prepared through a copper etching process which results in fixtures with variable gap sizes. Additionally, the impedance of the structure was found to be quite large which is problematic since reflection measurements have a limited impedance magnitude that can be measured effectively. The PCB method was able to extract a wide-band permittivity and loss tangent result, but the loss tangent result showed as much as 50% deviation from the expected value at low frequency.

To work around some of the drawbacks experienced with the circular PCB fixture characterization method, a new method of dielectric characterization is presented by which the simplicity of parallel plate capacitor theory is exploited. With the proposed method, a parallel plate capacitor is fully printed in a three-dimensional fashion using DPAM methods where the dielectric to be characterized is sandwiched between two conductive layers. The proposed structure is printed through a three-step process which is exclusively built through micro-dispensing material ink.

The parallel plate capacitor is a structure that is understood well fundamentally; its simplicity is the key to the presented characterization method. A parallel plate capacitor consists of two conductor plates that are parallel to each other and at different voltage levels, resulting in

an electric field between the plates. Insertion of a dielectric material between the plates perturbs the electric field and the capacitance of the structure increases.

3.2 Model Development



Capacitance Equation

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{3.1}$$

Figure 3.1 - *Depiction of a parallel plate capacitor and corresponding capacitance equation.*

The main parameters of interest in the design of a parallel plate capacitor are the area of the conductor plates (*A)* and the distance between them (*d*). A visual representation of an air-filled parallel plate capacitor is shown in figure 3.1 along with the classical formula used to calculate the capacitance of the structure [3]. The perturbation of the electric field by an arbitrary dielectric is accounted for by the inclusion of the relative permittivity term (ε_r) in equation (3.1).

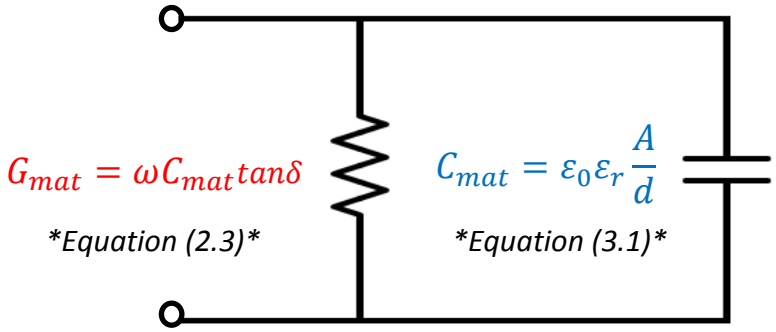


Figure 3.2 - *Schematic representation of the ideal parallel plate capacitor circuit model.*

If such a structure could be printed, then theoretically the dielectric properties of the material between the plates could be characterized with a similar circuit analysis method used in the previous chapter. The model of a parallel plate capacitor is a capacitance (C_{mat}) and its corresponding loss (G_{mat}) expressed as a conductance like that show in figure 3.2. Embedded within the capacitance is the relative permittivity of the material between the plates, embedded within the conductance is the material's loss tangent.

3.3 DPAM Parallel Plate Capacitor Design

With the presented circuit model, the dielectric characterization process through utilization of a parallel plate capacitor appears straightforward. To maintain this simplicity, the proposed parallel plate capacitor design should introduce as little parasitics as possible to ensure that the dielectric properties are effectively extracted. Additionally, the capacitor design should be measureable using only a single probe to be comparable to the PCB capacitor method of dielectric characterization.

The proposed DPAM parallel plate capacitor that will be investigated and utilized to characterize dielectric inks is shown in figure 3.4. This parallel plate design features a top and bottom conductor plate that meet at a single probing area, providing the benefits of a 1-port measurement. The probing area is a set of coplanar waveguide pads where the signal pad is connected to the top plate via a printed bridge and the ground pads are connected to the bottom plate underneath the dielectric layer.

The main parameters of interest when designing the DPAM parallel plate capacitor start with the parameters that control the parallel plate capacitance, the conductor plate area (A) and the distance between the plates (d). The other two parameters of interest are the pad width (W) and the gap length (G). These parameters control the dimensions of the probing area and are

important to consider because they determine the probe pitch required to effectively measure the capacitor in practice.

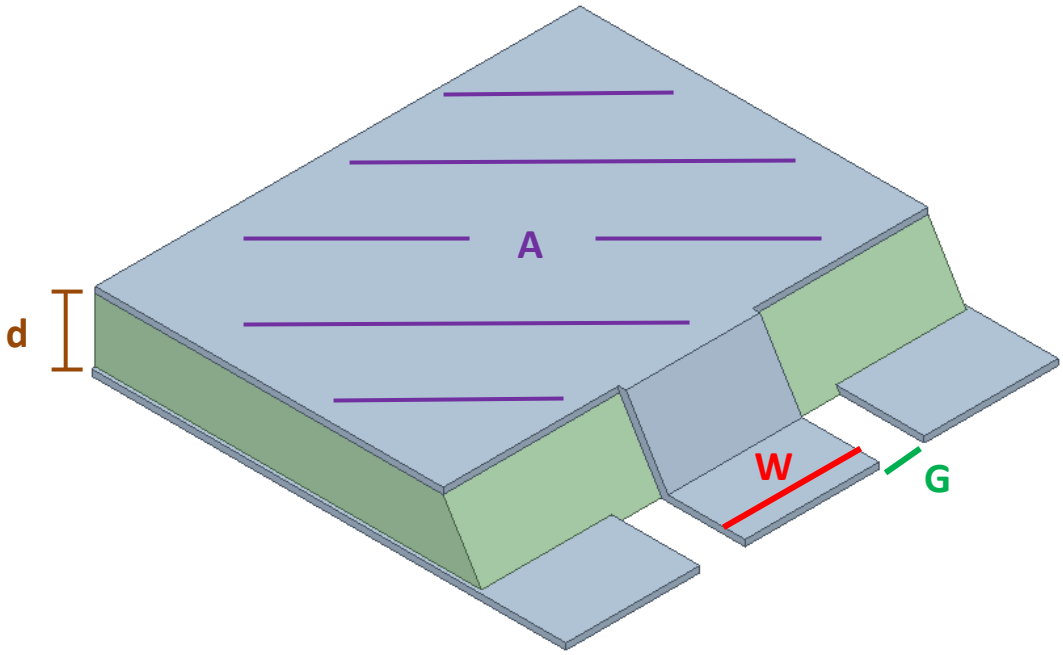


Figure 3.3 – *The proposed DPAM parallel plate capacitor design with labeled parameters of interest.*

Printing the proposed parallel plate capacitor would be done as a three step process which is detail in figure 3.4. First, the ground plate would be printed along with the entire set of probe pads. Here the signal pad is an isolated conductor surrounded by the ground plane at a distance *G*. Then, the dielectric layer is printed down on top of the ground plate. Part of this dielectric layer extends out over the edge of the pads to create a ramp area in preparation for the future bridge connection. The final step involves dispensing the top conductor plate as well as a bridge down to the signal pad below via the ramp area created by the sloping dielectric. An important note is that the printing process requires each layer to be individually cured after printing in order to create a solid surface for the next layer to be printed upon.

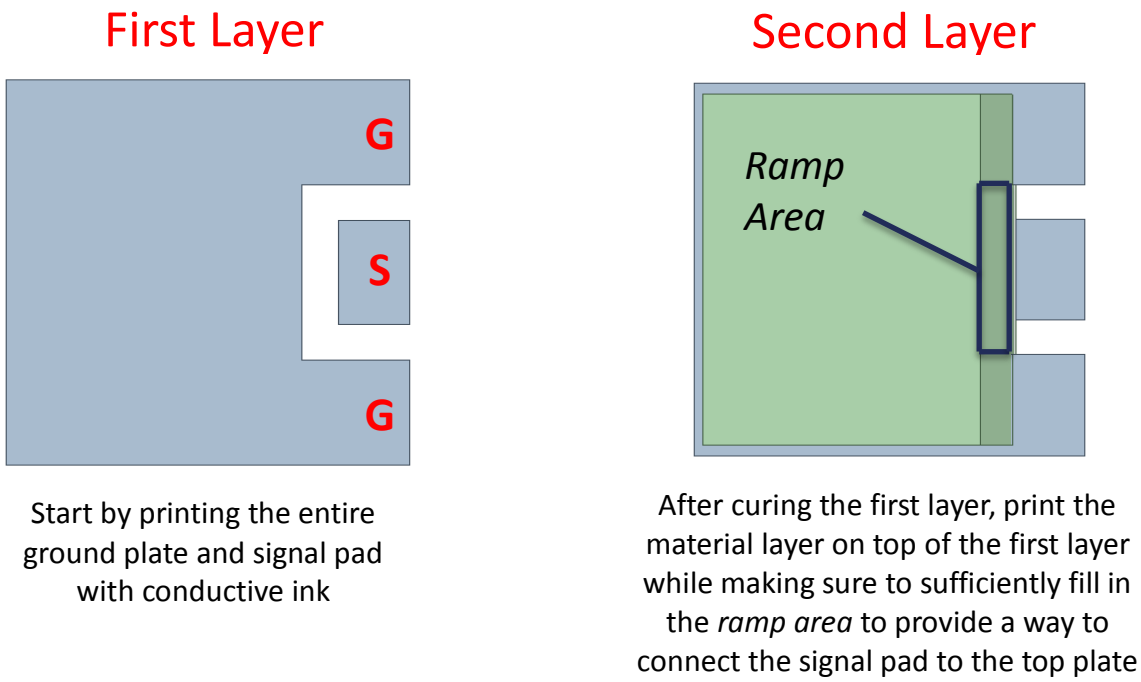


Figure 3.4 - *Details of the three-step printing process of the DPAM parallel plate capacitor.*

3.4 DPAM Parallel Plate Capacitor 3D Modeling and Analysis

Following the three-step capacitor building methodology, a 3D simulation setup was built in ANSYS EDT which is shown in figure 3.5. This parallel plate model setup is utilized to generate 1-port S-parameters data files that are analyzed to extract the permittivity and loss tangent from the dielectric material in the middle layer. The initial assumption is that the circuit

model equivalent of the parallel plate structure is that of the ideal parallel plate model shown in figure 3.2.

3.4.1 Model Construction

When constructing the 3D model setup of the parallel plate capacitor, measures were taken to ensure the practicality of the simulation so that it can be comparable to measured data of an identically printed parallel plate capacitor in the future. The proposed parallel plate capacitor is modeled on top of 60mil Rogers RT/duroid 6010 substrate and was designed with a conductor cladding thickness of 25 um and a dielectric material thickness of 100 um. These values

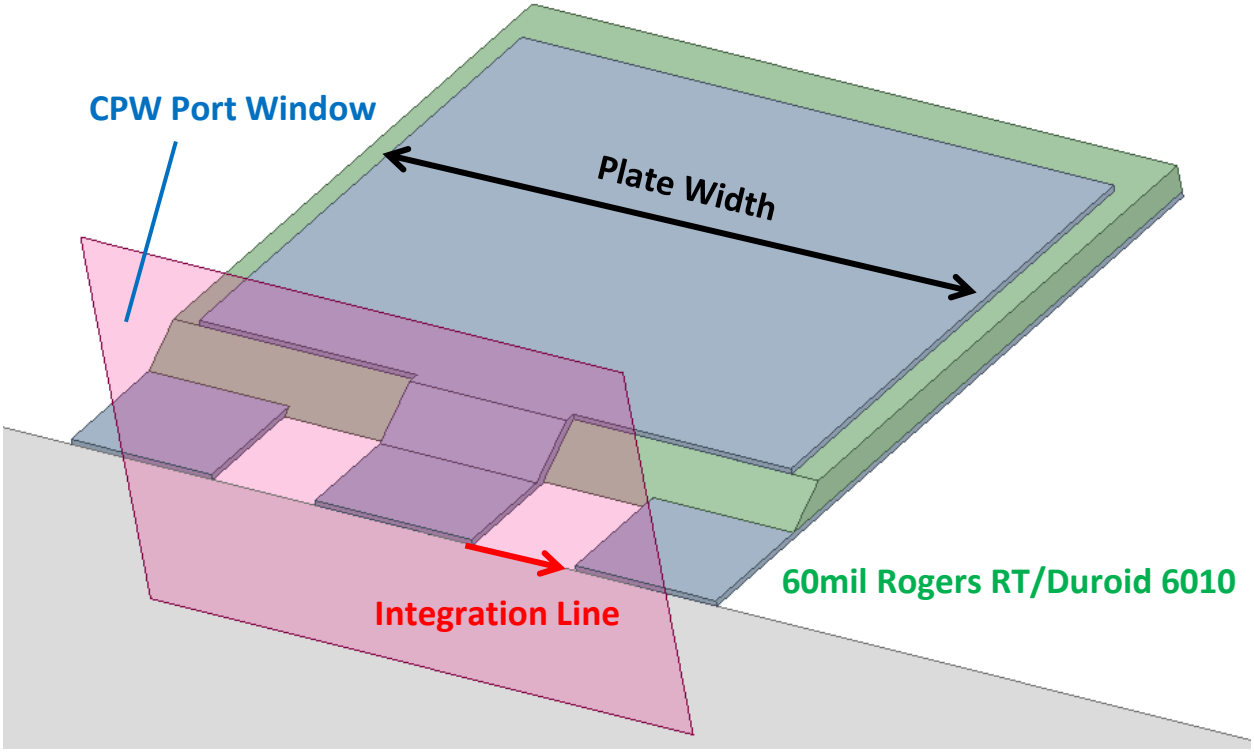


Figure 3.5 - *Simulation setup in ANSYS EDT of the DPAM parallel plate capacitor. The capacitor was modeled on top of 60mil Rogers RT/duroid 6010 substrate. The defined port is a wave port with the integration line shown.*

were selected by considering practical values for the thicknesses of the conductive and dielectric inks to be used in the practical implementation of the design. The pads were designed with a 600 um width (*W*) and a 400 um gap length (*G*) between them to accommodate measurements with a 1200-pitch GSG probe.

The area of the top plate was chosen to be slightly smaller than the area of the bottom plate to help prevent shorting between the top and bottom layers when printing the structure in practice. The final design value for the width of top plate is 2.4 mm and the final value of top plate length is 1.8 mm. These values for the plate dimensions were selected to bring the magnitude of the impedance of the proposed parallel plate design within the 1-200 Ω impedance range that is desired for accurate reflection measurements. This direct control over the impedance of the structure highlights one of the benefits of the proposed extraction method. The defined port for the simulation is a wave port with an integration line from the center conductor to the outer conductor, parallel to the surface of the substrate.

3.4.2 Ideal Model Assumption

With the constructed model of the parallel plate capacitor, a simulation is run from 0.1-10 GHz to generate a set of 1-port s-parameter files to be converted to admittances and analyzed. With the assumption that the parallel plate structure presented possesses a model like that shown in figure 3.2, the dielectric parameters of interest can be extracted with an admittance analysis. By the equations shown in the figure, the material capacitance, C_{mat}, can be extracted from the imaginary part of the admittance, resulting in the extraction of the permittivity. The loss tangent can be extracted from the real part of the admittance:

$$Real\{Y_{in}\} = \omega C_{mat} tan\partial_{mat}$$

$$Imag\{Y_{in}\} = \omega C_{mat}$$

$$C_{mat} = \frac{Imag\{Y_{in}\}}{\omega} \tag{3.2}$$

With the material capacitance, C_{mat}, the permittivity and loss tangent can be calculated as:

$$\varepsilon_r = \frac{dC_{mat}}{\varepsilon_0 A} \tag{3.3}$$

$$tan\partial_{mat} = \frac{Real\{Y_{in}\}}{\omega C_{mat}} \tag{3.4}$$

where equation (3.3) is the rearranged form of equation (3.1) for ideal parallel plate capacitors. Equation (3.4) is the rearranged form of the equation that defines G_{mat}.

To begin the simulation extraction process, the generated 1-port s-parameter data from the 3D model in figure 3.5 is ported to Keysight ADS. Using the tools available in the software, the S-parameters are converted to admittances and equations (3.2)-(3.4) are utilized to extract the dielectric properties of the material simulated between the plates. In this simulation, the dielectric material between the plates is a custom created material whose permittivity was specified in simulation to be 11.9 and the loss tangent was specified to be 0.025. These values were chosen based on the average values of the Damaskos characterization results of the dielectric ink in Appendix A. The results of the dielectric properties extraction are shown in figure 3.6.

From the results of the extraction, it is clear that there are some lingering parasitics in the structure which are causing the extraction results to tend to infinity with increasing frequency. As a result, the extraction of permittivity has its lowest percent difference of roughly 15% between 0.1-1 GHz and from there increases exponentially with frequency. The loss tangent extraction hits the desired value of 0.025 at 100 MHz, but quickly rises to 0.028 at 200 MHz and continues to deviate with increasing frequency.

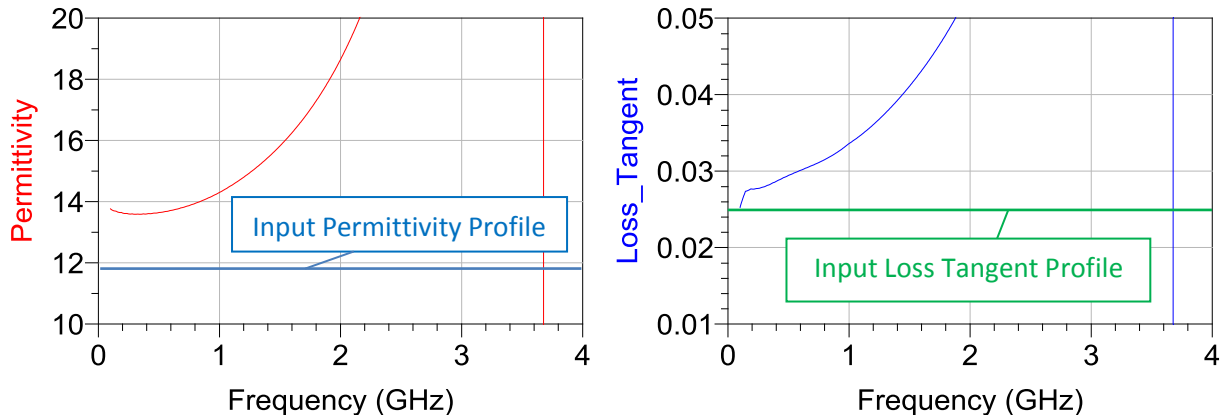


Figure 3.6 - *Results of the permittivity and loss tangent extraction assuming the ideal parallel plate capacitor model. The dielectric material used in the simulation is s custom created material whose permittivity was specified as 11.9 and loss tangent specified as 0.025.*

One important consideration is that the assumed model in this extraction method is the ideal model of a parallel plate capacitor. In reality, the conductor plates introduce some inductance which would certainly affect the extraction results since both the permittivity and loss tangent depend on the material capacitance, C_{mat}, which is derived from the imaginary part of the input admittance. Any stray reactance such as the proposed parasitic inductance must be properly accounted for to ensure the best possible extraction results of the dielectric property extraction with this method.

3.4.3 Improved Modeling Approach

To account for the parasitic behavior affecting the extraction results, a series inductor is added to the ideal parallel plate model to arrive at a revised model which is shown in figure 3.7. With this theoretical model as a foundation, a circuit model of the parallel plate capacitor can be constructed with the newly added parasitic inductance (L_{par}) included. From there, the parasitic inductance can be de-embedded from the admittance data to improve the bandwidth of the extraction result for permittivity and loss tangent with the proposed method.

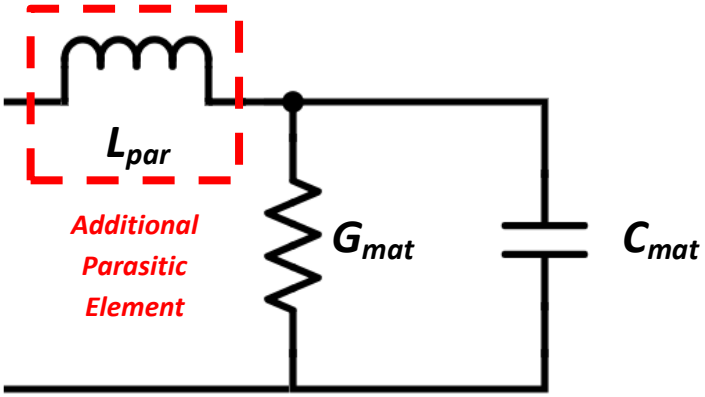


Figure 3.7 - *Revised model of the proposed DPAM parallel plate capacitor.*

To generate the circuit model of the parallel plate capacitor, a schematic in ADS is constructed with the revised model in figure 3.7 which is fit to the data from the 3D simulation like that shown in figure 3.8. From here, a vector magnitude difference optimization is run to solve for the parameter of interest, L_{par}. The permittivity and loss tangent of the dielectric material are entered as known information which means a ballpark figure for C_{mat} and G_{mat} can be calculated with the corresponding equations referenced in figure 3.2. The expected value for C_{mat} is about 4.8pF and the assumed loss tangent value for G_{mat} is 0.025. The variables C_{mat} and G_{mat} are given a ±5% degree of freedom in the optimization to help provide a better fit to the data presented.

After performing the optimization process described, a value for the parasitic inductance is obtained. With the parasitic inductance value, a schematic is created which generates a 2-port dataset file of that inductance. The resulting dataset file is placed within a de-embedding block which is placed in front of a dataset block containing the simulation data from the 3D model simulation. As a result, the parasitic inductance is de-embedded from the 3D simulation data, leaving only C_{mat} and G_{mat}. The S-parameters of the de-embedded simulation data are converted

to admittance data which is analyzed with equations (3.2)-(3.4) to extract the permittivity and loss tangent profiles. The results of the dielectric properties extraction are shown in figure 3.9 along with the schematic used to perform the de-embedding process.

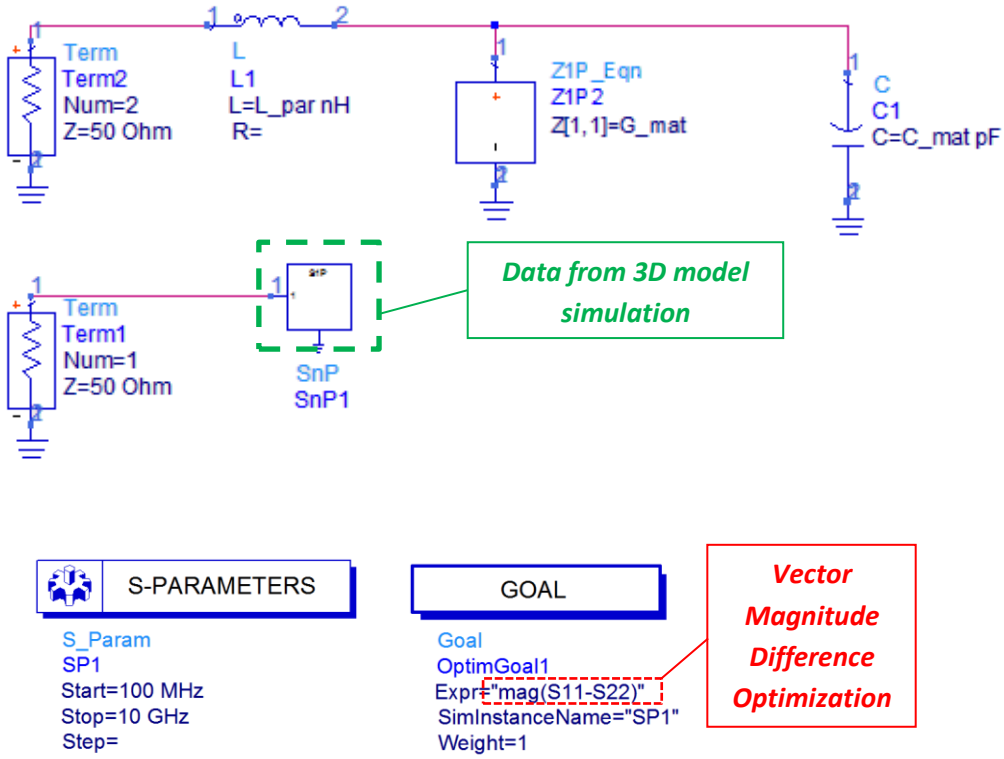


Figure 3.8 – *Schematic in Keysight ADS that was used to build the circuit model of the DPAM parallel plate capacitor. A vector magnitude difference optimization was run to minimize the S-parameters between ports 1 and 2. The main variable in the optimization is the parasitic inductance,* L_{par}.

When the parasitic inductance is de-embedded from the simulation data, the resulting extraction of permittivity through the admittance analysis is effective over a wide bandwidth with an extracted permittivity profile that is within 5% of the expected value at from 2-8 GHz. The extracted permittivity does not show signs of an exponential deviation until about 7 GHz.

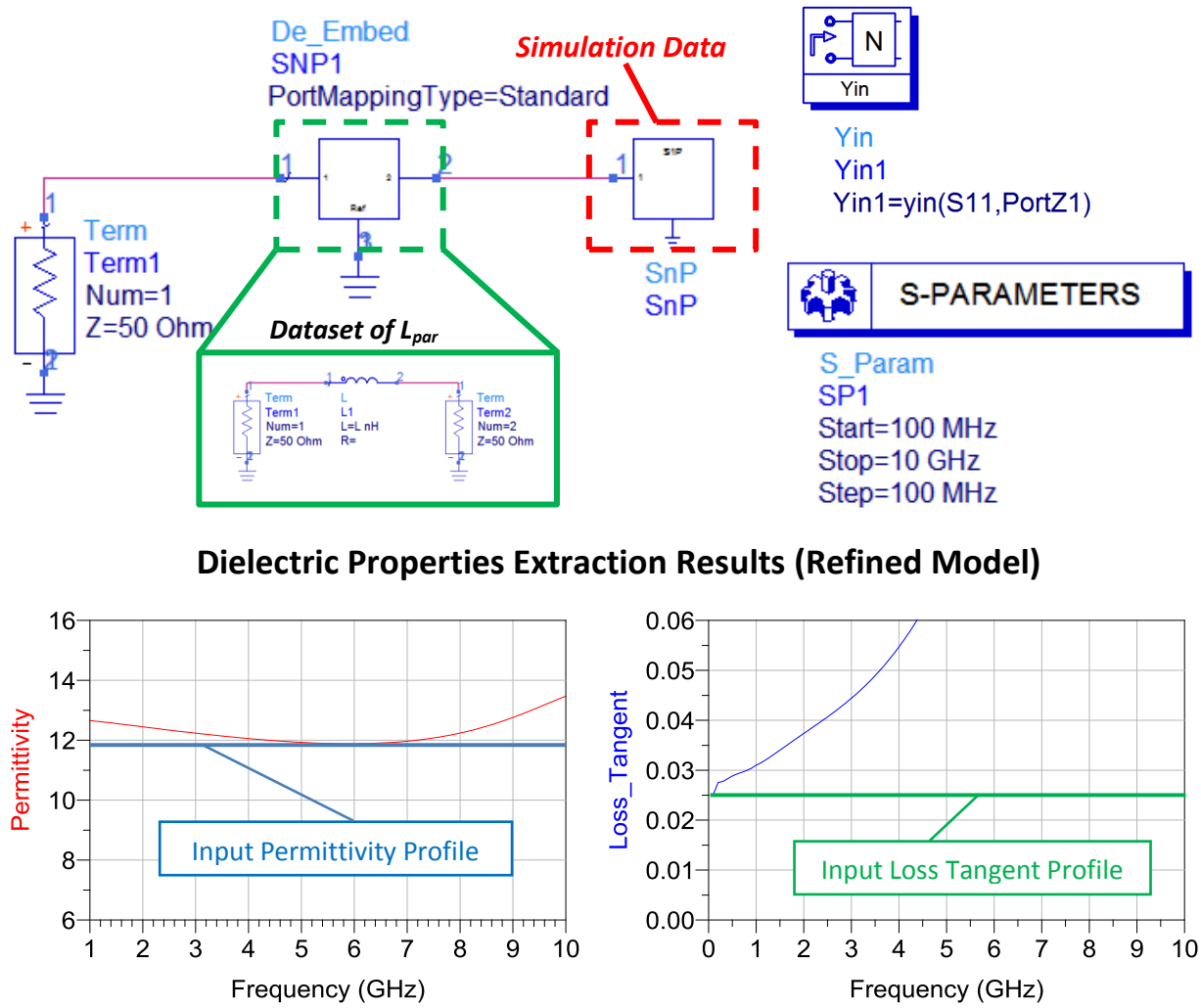


Figure 3.9 - *Schematic setup used to de-embed the dielectric parameters (top) results of the dielectric properties extraction (bottom).*

The loss tangent still appears to have an exponential deviation starting at low frequency, but the de-embedding of the inductance did have a slight effect on the extraction results. Previously, the loss tangent reached a value of 0.05 at about 1.8 GHz. Now, that same value of 0.05 is reached at 3.7 GHz signifying some improvement.

The results of this extraction attempt signify that the parasitic inductance that arises from the conductors is definitely a crucial element to consider when performing the extraction process. However, there still appears to be lingering parasitics causing a situation with the loss tangent

extraction. The extraction results are still band-limited and exponentially deviate from the expected result with frequency. One thing that has not been considered yet, however, is the series loss introduced by the conductor plates.

3.4.4 Full Circuit Model Development and Analysis

To further develop the circuit model shown in figure 3.7, a frequency dependent series loss is added to effectively model the conductor losses in the parallel plate structure. By appropriately modeling the conductor losses, they can be de-embedded from the simulation data to improve the loss tangent extraction results. The series loss is specified was fit to a model like that shown below:

$$R_s = a + b\sqrt{f} \tag{3.5}$$

where a and b are major optimization parameters and f represents frequency (in GHz). By running a vector magnitude difference optimization, the values of a and b that represent the loss profile are solved for in a similar fashion to the parasitic inductance. The final values of the parasitic inductance along with the series loss parameters obtained through optimizations are shown in table 3-1.

Table 3-1 - *Final optimized values of the parasitics associated with the conductors of the capacitor.*

Parameter	L_{par}	a	b
Value	**387 pH**	**0.1353**	**0.0011**

With element values for the parasitic circuit elements L_{par} and R_s, the de-embedding process outlined in figure 3.9 can now be performed again. This time, the dataset file within the de-embedding block contains circuit data for the newly added series loss, R_s, which is desired to

be removed from the admittance analysis. The results of the admittance based extraction of dielectric properties after de-embedding both conductor parasitics is shown in figure 3.10.

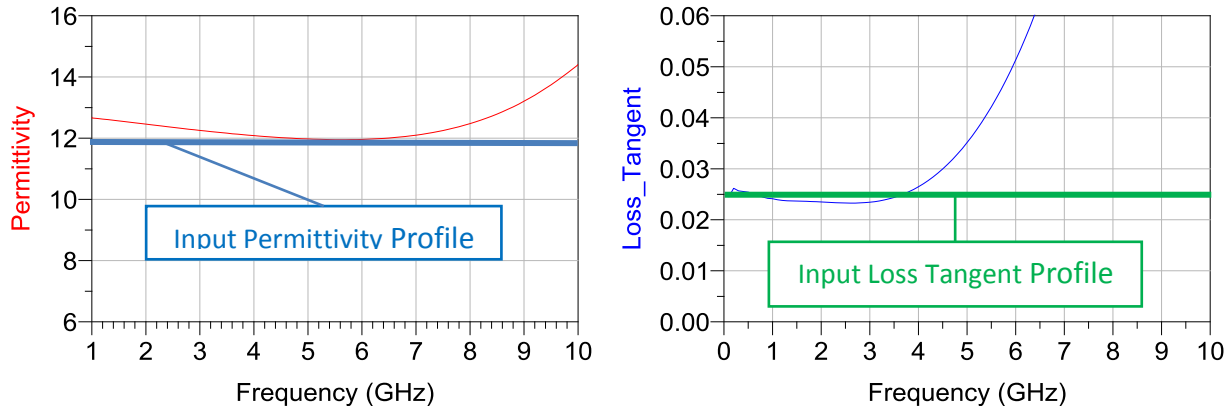


Figure 3.10 - *Results of dielectric properties extraction from the improved model that accounts for conductor losses.*

From the results in the figure, the extracted permittivity is seemingly unaffected from the previous extraction results. This is expected since the permittivity extraction only depends on the imaginary part of the admittance, adding a series loss to the model should have no effect. The resulting extracted loss tangent profile bounces between 0.023-0.027 within the band of 0.1-4 GHz. This result calculates out to ±8% difference from the expected value of 0.025. This result is an appreciable improvement from the last result where only the parasitic inductance was considered in the model. After 3.5 GHz, however, the extracted loss tangent beings to deviate exponentially from the expected value resulting in a far more band-limited result than the permittivity extraction. It is clear from the results that the loss of the proposed parallel plate structure is not effectively modeled after 4 GHz.

An additional possible loss mechanism not yet considered, however, is radiation loss. Given the size of the plates, there is a possibility that the structure begins to radiate and exponentially affect the loss tangent extraction results with increasing frequency. By modifying

the previously utilized 3D model of the parallel plate capacitor, the radiation loss, if present, can be revealed. By specifying the conductor plates to be a perfect electrical conductor and dielectric between the plates to be lossless, the only remaining loss of the simulated structure would be that of radiation.

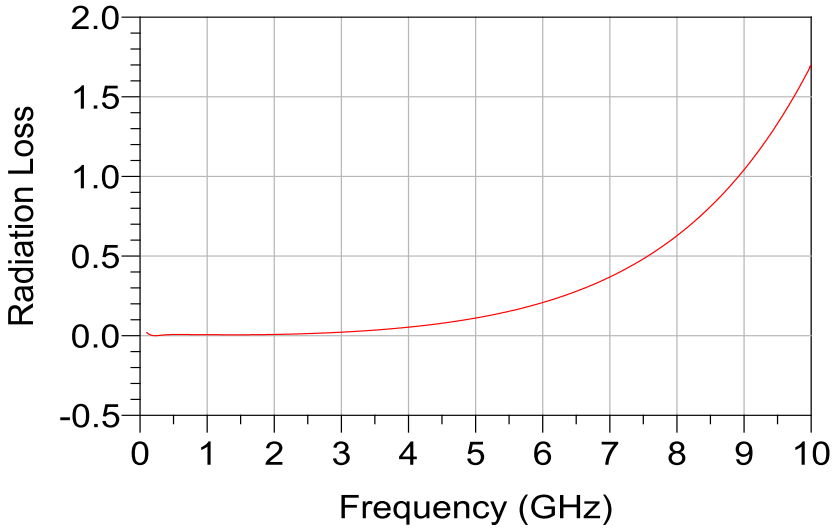


Figure 3.11 - *Radiation loss of the parallel plate structure. Results were obtained through a simulation of the parallel plate in ANSYS EDT with PEC conductor plates and a lossless dielectric.*

Through this modified model investigation, it was found that the parallel plate capacitor structure does indeed radiate and has an associated radiation resistance that grows exponentially with frequency like that shown in figure 3.11. From the plot, it can be observed that the behavior follows a similar trend to that seen in the loss tangent extraction. This data obtained from the simulation is taken to ADS where an optimizer fits the loss profile to a frequency dependent loss like that shown by equation (3.6). Here, c is the optimized parameter and f represents frequency (in GHz). The value obtained for c through optimization was 0.0075.

$$R_{rad} = cf^2 = 0.075f^2 \tag{3.6}$$

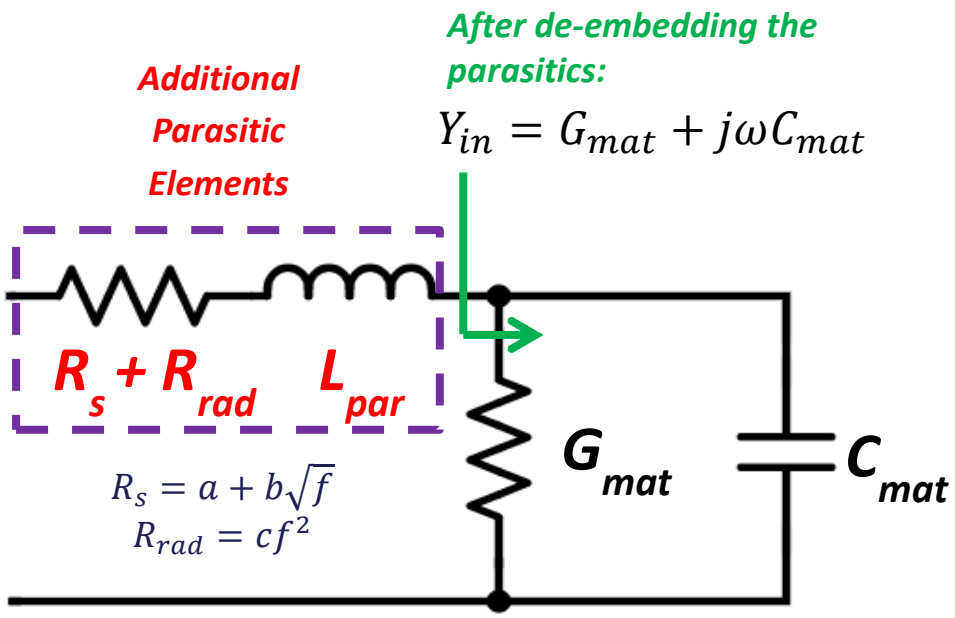


Figure 3.12 - *Full parasitic model of the DPAM parallel plate capacitor.*

By considering all of the mentioned parasitics of the parallel plate structure, the circuit equivalent model has evolved to the form shown in figure 3.12. With the three parasitic elements L_{par}, R_s, and R_{rad} effectively modeled, they are collectively de-embedded from the original simulation data of the parallel plate structure like demonstrated in figure 3.9. The resulting data is analyzed using equations (3.3) and (3.4) to extract the permittivity and loss tangent profiles. The results of this fully de-embedded simulation extraction are shown in figure 3.13.The final optimization values for the parasitic elements are listed in table 3-2.

Table 3-2 - *Final optimized values of all of the parasitics of the DPAM parallel plate capacitor.*

Parameter	L_{par}	***a***	***b***	***c***
Value	**387 pH**	**0.1353**	**0.0011**	**0.0075**

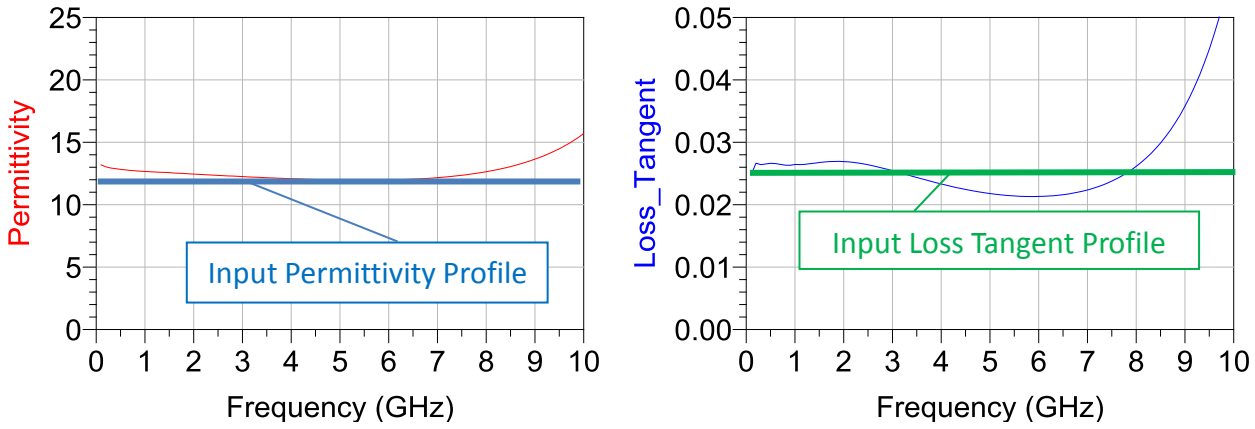


Figure 3.13 - *Extracted permittivity and loss tangent profiles of the fully de-embedded simulation data. The parasitic inductance, series conductor loss and radiation loss were de-embedded and the resulting admittance was analyzed.*

By incorporating a series loss to account for the radiation of the parallel plate capacitor, the loss tangent extraction dramatically improved, effectively doubling the extraction bandwidth from 4 GHz to 8 GHz. The largest deviation in the loss tangent extraction was roughly 16% occurring around 6 GHz where the extracted profile appears to begin to deviate exponentially. The extracted loss tangent profile is indicative of some radiation loss that still exists. A further investigation and improvement to the radiation loss model could extend the bandwidth of the loss tangent extraction out to even higher frequencies. The extracted permittivity profile in this case remains unchanged from the previous extraction attempt since the permittivity extraction depends only on the imaginary part of the admittance.

3.5 Printing

In previous sections, the proposed parallel plate capacitor was introduced and designed considering some hurdles in practical implementation. Then, a 3D model of the structure was generated and analyzed using available CAD software in an attempt to characterize the dielectric material between the plates. Next, the proposed parallel plate capacitor design is printed using

DPAM methods with the goal of achieving a structure with similar dimensions to the design already proposed.

The capacitor will be printed on top of 60mil Rogers RT/duroid 6010 substrate, identical to the simulation model previously presented. The first main goal in the printing process is to obtain the proper thicknesses for each respective layer. To match the simulated design, the conductor thickness should be 25 um and dielectric thickness should be 100 um. Another goal is to ensure nice flat surfaces for each layer with as little roughness possible to be consistent with the simulation.

The parallel plate capacitor design is built in a three-step process like that shown in figure 3.14. To start, the bottom ground layer is printed with conductive ink at a height of 40 um above the surface of the substrate. This print height was chosen to ensure that enough material is dispensed to obtain the desired thickness after curing the material. The chosen printed line width for this layer was around 300 um. The script to print the capacitor, however, was written with a line spacing of 200 um. The extra 100 um overlap can be helpful when trying to print smooth surfaces as the lines merge together and flatten. This is especially true when dealing with high viscosity materials.

After the first layer is dispensed and cured, dielectric layer is ready to be dispensed over the top of it. This dielectric layer is printed at a height of 150 um to ensure enough material is dispensed to achieve the desired plate spacing (*d*) post-cure. When the second layer is dispensed, some overlap is intentionally laid down over the side edges of the ground plate to prevent the possibility of creating a short circuit with the incoming top layer. Similarly to the 3D model, the dielectric layer partially extends over the signal pad in preparation for the bridge connection from the top plate.

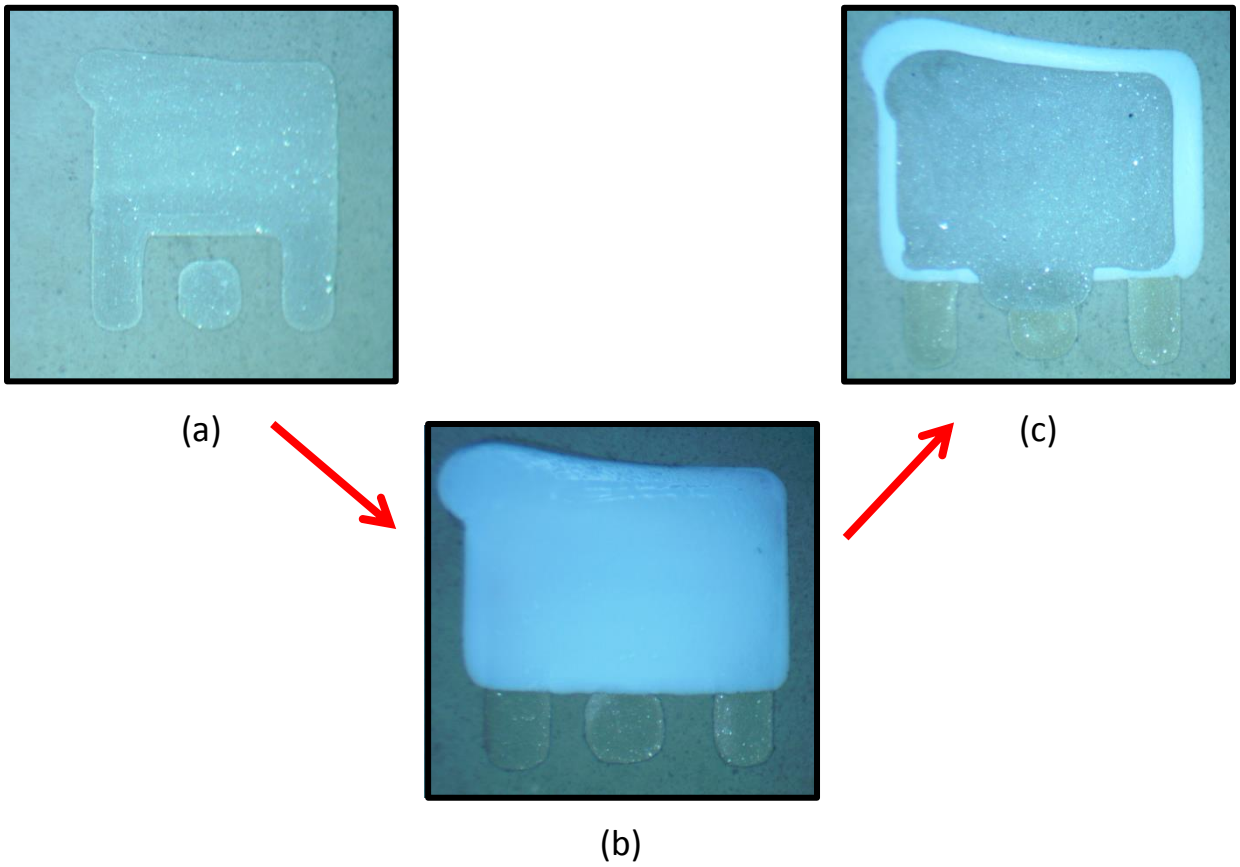


Figure 3.14 - *Printed stages of the DPAM parallel plate capacitor: (a) ground layer, (b) ground layer with a dielectric layer dispensed on top, (c) full DPAM parallel plate capacitor.*

The last layer to be printed in the structure contains the top conductor plate and the bridge down to the signal pad. This final conductor layer is printed at the same height level as the first layer (40 um above the surface). The reference point for the printing height of this level is taken from the middle of the dielectric layer. Since the dielectric layer was printed in excess over the sides, the top plate can be aligned well with the bottom plate. To execute the bridge connection, an extra line of code was added to the script to sweep out the last line of the plate printing process towards the signal pad below. The quick sweep out to the side was found to create nice looking bridges like that seen in figure 3.14 (c).

After each layer was printed and appropriately cured, the result was taken to a Dektak 3030ST Profiler to observe the surface characteristics of the resulting layer. From this analysis, it was found that the conductor levels had an average thickness of about 20 um, but also had some undesired roughness where the level would dip as low as 12 um in some cases. As for the dielectric, some mixed results were obtained with the thickness. Some of the prepared samples were found to have a thickness as low as 80 um and others were found to have a thickness as high as 120 um.

With some samples prepared, dimension measurements of samples are taken which are used in the extraction process. The average value for the top plate width of the samples was roughly 2.5 mm which is 0.1 mm larger than the simulated value. As for the plate length, the average value was about 1.8 mm which is the value simulated. With the dimensions of the conductor plates measured and the distance between plates known, the extraction process can be performed on the samples.

3.6 Measurements

In this section, the prepared capacitor samples are measured for s-parameter data which is converted to admittance data and analyzed using the method presented in section 3.4.4. The VNA used to perform the measurements is a Keysight ENA Series Network Analyzer which was calibrated from 0.1-16 GHz. There are 401 points in the measurement and an averaging factor of 16 was used. The probe used to measure the parallel plate capacitors is a 1200-pitch GGB Picoprobe which was calibrated out to the probe tips using a CS-10 substrate.

With the measurement setup described, the parallel plate samples are measured for 1-port s-parameter data. The resulting s-parameter files are imported to an ADS schematic where they are fit to a model like that shown in figure 3.12. Initially, the model developed for the 3D

simulation data was used on the measured data in attempt to de-embed the dielectric properties. Although the developed loss model was sufficient for the measured data, the parasitic inductance model was not. The optimizer in ADS was utilized to run another vector magnitude difference optimization to generate a new value for the measured parallel plate parasitic inductance.

The resulting parasitic inductance that provided the best fit for the measured data was 274 pH which differs from the value found previously for the simulation data modeling. This difference in inductance values can be attributed to the difference between the probing position in the measurement and to the port definition in the simulation. To obtain a good measurement result, the capacitor had to be probed further down the pads where the conductor surfaces were more suitable for a probe landing.

After a parasitic inductance value was obtained from the measured data of the parallel plate, a dataset file was created for the parasitic inductance and loss model which is de-embedded from the measured data. After the parasitics are de-embedded from the measured data, the resulting admittance is analyzed to extract the dielectric properties of the material between the plates. The results of the dielectric properties extraction after this de-embedding process are shown in figure 3.15.

Figure 3.15 shows a simulated vs. measured comparison of the measured s-parameter data along with the resulting dielectric properties extraction from that data compared against Damaskos results. The extracted permittivity profile of the de-embedded measured data from 0.1-5 GHz shows a flat 16% difference from the Damaskos cavity results. After 5 GHz, the extracted permittivity from the de-embedded measured data deviates and tends to infinity. As for the loss tangent, the result was found to band-limited to about 6 GHz after which the extracted

profile beings to deviate exponentially. This is about 2 GHz less bandwidth than the simulated extraction attempt which accomplished a loss tangent extraction out to 8 GHz.

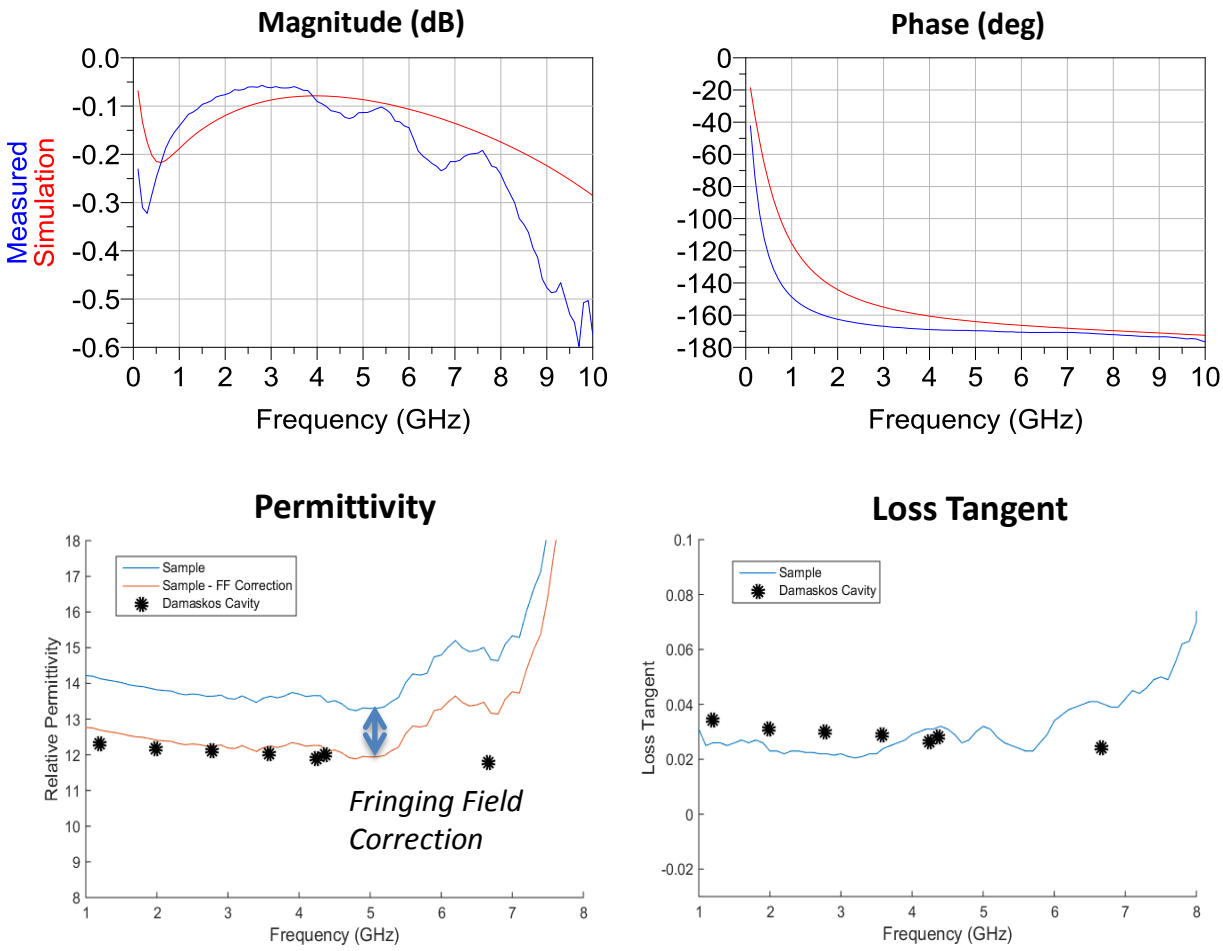


Figure 3.15 - *Measured vs. simulated comparison for the DPAM parallel plate capacitor. Measured vs. simulated S-parameters (top) De-embedded simulation data extraction vs de-embedded measured data extraction of dielectric properties (bottom).*

To improve the permittivity extraction, Palmer's rectangular parallel plate capacitance formula can be utilized which accounts for the fringing fields of the structure [9]:

$$C_{FF} = \frac{\varepsilon_0}{G} WL\left(1 + \frac{G}{\pi W} + \frac{G}{\pi W}\ln\left(\frac{2\pi W}{G}\right)\right)\left(1 + \frac{G}{\pi L} + \frac{G}{\pi L}\ln\left(\frac{2\pi W}{G}\right)\right) \tag{3.7}$$

where the original capacitance equation is multiplied by correction terms for the length and width dimensions. The dimension corrections are with respect to the gap length and result in

enlarging the dimensions of the plate which lowers the extracted permittivity (see equation 3.3). The result of applying Palmer's formula to the measured data is shown as the red trace in figure 3.15 which is a downward shifted version of the original measured data. By applying the fringing field correction, the extracted permittivity profile traces the Damaskos data from 1.5-5.5 GHz where only 2-3% is observed, a dramatic improvement from 16%. Shortly after 5.5 GHz, the extracted permittivity begins to deviate exponentially towards infinity.

Although the dielectric properties were effectively extracted, the results were band-limited and have a tendency to deviate exponentially after 5-6 GHz. The loss tangent extraction was improved appreciably by effectively modeling the radiation resistance and the permittivity was improved through implementation of Palmer's formula to account for the fringing effects of the parallel plate. There is still an apparent exponential deviation of the extracted dielectric properties profiles which could likely be attributed to the 1200-pitch probes used to make the measurement which are not suitable for high frequencies.

There were numerous challenges to overcome in development of the parallel plate method. Many hours were devoted to learning about the conductive and dielectric inks that were used to print the structure as well as developing the printing scripts which are included in Appendix C. However, once the process was laid out and the printing process was understood, the dielectric characterization process with the parallel plate became much quicker to perform with highly accurate results up to 5 GHz. The PCB method was found to be material limited, any material than cannot be sanded down cannot be characterized. If you can print the material, you can characterize it with the parallel plate method. The parallel plate method takes a bit longer to establish, but it can be trusted to produce accurate results.

CHAPTER 4: CONCLUSIONS

Two methods of dielectric characterization have been proposed, both of which utilize direct-print additive manufacturing as part of the extraction process. Both methods presented have simple fixtures used to perform their respective extraction process. An analysis was conducted for each fixture starting with basic modeling and simulation based extractions, then moving on to measurements and practical extractions.

The first method shown was a circular capacitor etched in PCB substrate where the dielectric to be characterized is dispensed in the gap left behind by the etching process. This extraction method relies on a two-measurement based extraction where the combination of data files can be used to effectively subtract out the parasitics of the structure, leaving an RC circuit with the dielectric properties of interest. With an admittance analysis of the de-embedded result, the desired dielectric properties can be extracted.

When this method was conducted in practice, the results of the extraction for permittivity were within ±8% of the expected value from 1-12 GHz. The best loss tangent extraction results were between 2-8 GHz where there was about 50% difference from the expected value. The results obtained with the fixture suggest that the proposed method would be valuable as a quick screening method of dielectric properties.

Some advanced modeling of the PCB capacitor fixture was conducted to draw some additional conclusions about the effectiveness of the extraction method. A study was conducted on the effects of having a dielectric surface level that differs from the conductor cladding height.

From this analysis, it was concluded that the extraction method is very sensitive to deviations from the ideal scenario where the dielectric surface is perfectly flush with the conductor cladding height. As a result, the material should be sanded down to the height of the cladding before the measurements of the material filled fixtures is performed in practice. This highlights a key material limitation argument surrounding this method, as this sanding process must be performed to generate effective extraction results. A slight difference of 1 um between the dielectric surface level and conductor cladding height results in about 8% difference in extracted permittivity and as much as 15% difference in extracted loss tangent at some frequencies.

Then, a second method of dielectric characterization is proposed by which a parallel plate capacitor is printed exclusively through micro-dispensing conductive and dielectric inks. The capacitor is built in a step-by-step process where three layers are stacked on top of each other. An analysis was conducted on the proposed parallel plate structure in which a circuit model was constructed from 3D model simulation data. Through this analysis, the parasitics of the structure were identified and modeled accordingly. With the fully developed model, an extraction of dielectric properties from simulated data was conducted which was shown to be effective from 1-8 GHz for permittivity and loss tangent.

Then, the parallel plate capacitor method was demonstrated in practice as samples were printed by executing the same three-step building process laid out for the simulation. The samples were measured for s-parameter data that was ported to ADS where a measured data model of the parallel plate capacitor was constructed. By performing a similar de-embedded admittance analysis method as the PCB capacitor, the dielectric properties were extracted from the measured data. Some additional modeling was performed as a follow up to the initial extraction attempt with the goal of improving the results of the extraction. By appropriately

modeling the parasitic inductance and loss parasitics, the permittivity extraction and loss tangent were effective out to 5 or 6 GHz.

The results of the parallel plate extraction of dielectric properties proved to be more band-limited than the results obtained with the PCB capacitor method. However, the parallel plate method generated results with much higher accuracy within its effective bandwidth than the PCB method. One downside of the parallel plate method is that it required a printing process foundation to be established which was time consuming to develop. However, after this process was put in place, the characterization process became much quicker and more effective.

The PCB capacitor method was straightforward to perform in practice, but required fixtures to be etched in substrate. Additionally, the fixtures were found to have large impedance magnitudes, an undesirable characteristic for s-parameter measurements. Additionally, the PCB method is limited to materials that can be sanded down post-cure. Any material overflow or underflow in the fixture would result in undesired dielectric properties extraction error. The parallel plate method can be used to characterize any material that can be printed and the impedance of the structure can be controlled.

4.1 Future Work

The two dielectric characterization methods presented were performed on a single dielectric ink. Additional investigations could be made to explore the extraction performance of the proposed methods with a variety dielectric inks that cover an array of material profiles. In regards to the PCB fixture, care should be taken to select dielectric materials that are capable of being characterized with both methods. An ideal material would be printable and able to be sanded after the material has properly cured.

Some additional investigations can be conducted on the parallel plate capacitor such as improving the parasitic model. From the results of the parallel plate extraction, it is apparent that some parasitics still exist which are causing the extracted permittivity and loss tangent to tend to infinity. The radiation loss model could potentially be improved to extend the loss tangent extraction further. Some investigations into printing different sized parallel plates can be conducted to observe if a better extraction result can be achieved.

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APPENDIX A: DIELECTRIC CHARACTERIZATION WITH DAMASKOS CAVITIES

The dielectric ink used in the experiments throughout this work did not have its dielectric properties specified on its datasheet from the manufacturer. In order to confirm the results of the methods presented in this paper, some reliable dielectric property information is required to compare the results against. To get the reliable data that would be used as the "golden standard" for the experiments conducted in this work, two Damaskos cavities were used that cover two different bandwidths that overlap conveniently around 4 GHz. The cavities use software to calculate the resonance frequencies at which the material will be characterized. Each cavity has at least 5 resonances that are calculated within its bandwidth.

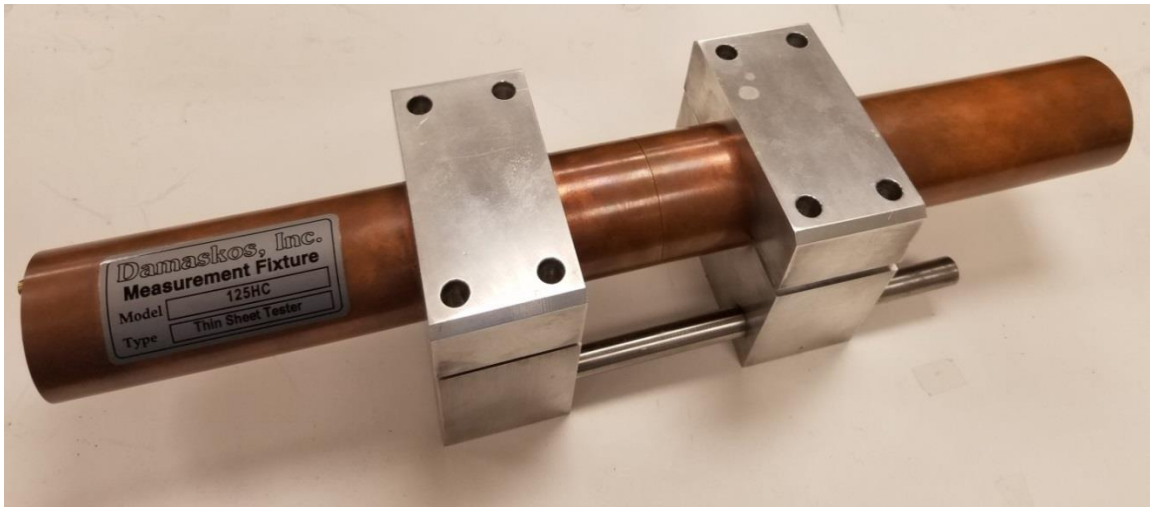

Figure A.1 – *The Damaskos 125HC Measurement Fixture used to characterize dielectric inks from 0.4-4.3 GHz at six resonance frequencies*

Table A-1 - *Results from the dielectric properties measurement of the ink with the Damaskos 125HC Measurement Fixture.*

Frequency (GHz)	Q	Permittivity		Loss Tangent
		Real	Imaginary	
0.40	1200	12.64	0.49	0.0391
1.19	1572	12.31	0.42	0.0344
1.98	1776	12.17	0.38	0.0311
2.78	1886	12.10	0.36	0.0301
3.57	1867	12.03	0.35	0.0290
4.37	1474	11.99	0.34	0.0283

The first cavity is the Model 125HC and can be seen in figure A.1. This cavity was used to cover the frequency band: 0.4–4.3 GHz. This Damaskos cavity measures the dielectric properties of the material at six different resonance frequencies. The results of the dielectric properties measurement of ink 1 with the 125HC cavity are shown in table A-1.

The second cavity used to characterize dielectric inks is the Damaskos 015 Measurement Fixture which is shown in figure A.2. This cavity measures the dielectric properties at five

Figure A.2 - *The Damaskos Model 015 Measurement Fixture used to characterize dielectric inks from 4.2-16.8 GHz at five resonance frequencies*

Table A-2 - *Results from the dielectric properties measurement of the ink with the Damaskos Model 015 Measurement Fixture*

Frequency (GHz)	Q	Permittivity		Loss Tangent
		Real	Imaginary	
4.25	575	11.88	0.315	0.0265
6.67	627	11.77	0.285	0.0242
9.86	678	11.72	0.276	0.0236
13.28	754	11.66	0.265	0.0227
16.80	804	11.60	0.262	0.0226

resonance frequencies, one less than the 125HC. For this application, the five resonance frequencies covered the band: 4.2-16.8 GHz. The results of the dielectric properties characterization in this frequency band for ink 1 are shown in table A-2.

The two Damaskos cavities conveniently overlap around 4.3 GHz. The lower frequency cavity (125HC) has its highest resonance at 4.37 GHz while the higher frequency cavity (Model 015) has its lowest resonance at 4.25 GHz. This overlap was exploited to get a wide-band characterization that can be used as a standard for future measurements.

APPENDIX B: MATLAB SCRIPTS

Throughout the experiments performed in this work, Matlab was relied on to perform calculations with the scripts shown in this section. The first script shown in figure B.1 extracts the permittivity and loss tangent profile from a set of s-parameter measurements or simulations of the circular PCB capacitor using the method described in section 2.3.

```
r_in = 400;
r_out = r_in + 200;
h = 35e-6;


perm = 8.85418782e-12;
c_air = (2*pi*perm)*(h/(log(r_out/r_in)));



data_air = read(rfdata.data, empty.s1p');
freq = data_air.Freq;
s_air = extract(data_air, 'S_PARAMETERS', 50);

data_mut = read(rfdata.data, 'filled.s1p');
freq2 = data_mut.Freq;
s_mut = extract(data_mut, 'S_PARAMETERS', 50);


a = size(freq);
b = a - [0 1];
limit1 = norm(b);

a2 = size(freq2);
b2 = a2 - [0 1];
limit2 = norm(b2);


for i = 1 : limit2;

   w(i,1) = (2*pi)*(freq(i,1));
```

```
    z_air(i,1) = 50*((1 + s_air(1,1,i))/(1 - s_air(1,1,i)));
    z_mut(i,1) = 50*((1 + s_mut(1,1,i))/(1 - s_mut(1,1,i)));
    w_imag_air(i,1) = (1/(w(i,1)*imag(z_air(i,1))));
    w_imag_mut(i,1) = (1/(w(i,1)*imag(z_mut(i,1))));

    c_d(i,1) = w_imag_air(i,1) - w_imag_mut(i,1) + c_air;

    epsilon(i,1) = c_d(i,1)/((2*pi*perm)*(h/(log(r_out/r_in))));
    tan_d(i,1) = (c_d(i,1)*w(i,1))*(real(z_mut(i,1)) - real(z_air(i,1)));


end

plot(freq2,epsilon), title('\fontsize{18}Permittivity Extraction'),
xlabel('\fontsize{14}Frequency (GHz)'),
ylabel('\fontsize{14}Epsilon');
axis([0.1e9 18e9 5 20]);
grid on;

figure
plot(freq2,tan_d), title('\fontsize{18}Loss Tangent Extraction'),
xlabel('\fontsize{14}Frequency (GHz)'),
ylabel('\fontsize{14}Epsilon');
axis([0.1e9 18e9 -0.1 0.1]);
grid on;

csvwrite('LOSS_SIM',tan_d);
csvwrite('PERM_SIM',epsilon);

csvwrite('freq',freq);
```

APPENDIX C: PRINTER SCRIPTS

In this section, the scripts used to perform the printing tasks on the nScrypt printer are included for reference. All of the scripts in this section were written by hand by a combination of Matlab and Excel. To create the script that prints inside the PCB capacitor, first a circle was parameterized in Matlab. From there, a differential vector was created between the successive points to generate a format suitable for a printer. Then, excel was used to generate the repetitive "MOVE" commands and structure the code. The script generated that prints a circle suitable for

```
speed 1

move 0.45 0 0

trigvalverel 0.15 8
trigwait 0.01

move -0.004 0.056 0
move -0.011 0.056 0
move -0.017 0.054 0
move -0.024 0.051 0
move -0.030 0.048 0
move -0.036 0.044 0
move -0.041 0.039 0
move -0.046 0.033 0
move -0.050 0.027 0
move -0.053 0.021 0
move -0.055 0.014 0
move -0.056 0.007 0
move -0.057 0.000 0
move -0.056 -0.007 0
move -0.055 -0.014 0
move -0.053 -0.021 0
move -0.050 -0.027 0
move -0.046 -0.033 0
move -0.041 -0.039 0
move -0.036 -0.044 0
move -0.030 -0.048 0
move -0.024 -0.051 0
move -0.017 -0.054 0
move -0.011 -0.056 0
move -0.004 -0.056 0
move 0.004 -0.056 0
move 0.011 -0.056 0
move 0.017 -0.054 0
move 0.024 -0.051 0
move 0.030 -0.048 0
move 0.036 -0.044 0
move 0.041 -0.039 0
move 0.046 -0.033 0
move 0.050 -0.027 0
move 0.053 -0.021 0
move 0.055 -0.014 0
move 0.056 -0.007 0
move 0.057 0.000 0
move 0.056 0.007 0
move 0.055 0.014 0
move 0.053 0.021 0
move 0.050 0.027 0
move 0.046 0.033 0
move 0.041 0.039 0
move 0.036 0.044 0
move 0.030 0.048 0
move 0.024 0.051 0
move 0.017 0.054 0
move 0.011 0.056 0
move 0.004 0.056 0

valverel 0 5
speed 50

move 0 0 5
```

Figure C.1 – *Script that prints the circle required for the PCB characterization method.*

the characterization method described in chapter 2 is shown in figure C.1. This script was designed to print a circle that has a radius around 450 um since this was determined to be a good average value for the fixtures prepared.

The combination of scripts used to print the DPAM parallel plate capacitor are shown in the next series of figures C.2-C.4. Each script represents a layer of the capacitor starting from the first layer. The scripts were written with the intention of matching the 3D simulation model in chapter 3 where the line thickness was chosen to be 200 um.

```
speed 3

trigvalverel 0.10 0.1

trigwait 0.01
move 0 1.5 0
move 2.5 0 0
move 0 -1.5 0
move -2.40 0 0
move 0 1.45 0
move 0.2 0 0
move 0 -1.4 0
move 0.2 0 0
move 0 1.4 0
move 0.2 0 0
move 0 -1.4 0
move 0.2 0 0
move 0 1.4 0
move 0.2 0 0
move 0 -1.4 0
move 0.2 0 0
move 0 1.4 0
move 0.2 0 0
move 0 -1.4 0
move 0.2 0 0
move 0 1.4 0
move 0.2 0 0
move 0 -1.4 0
move 0.2 0 0
move 0 1.4 0
move 0.2 0 0
move 0 -1.4 0
move 0.2 0 0
move 0 1.4 0
move 0.2 0 0
move 0 -1.4 0
move 0.2 0 0
move 0 1.4 0

valverel 0 5
speed 5

move 0 0 5
move -2.45 -1.45 0
move 0 0 -5
wait 0.001

speed 0.5

trigvalverel 0.09 0.5

trigwait 0.01
move 0 -1 0
move 0.5 0 0
move 0 0.95 0
move -0.45 0 0
move 0 -0.9 0
move 0.2 0 0
move 0 0.9 0
move 0.2 0 0
move 0 -0.9 0
valverel 0 5
speed 5

move 0 0 5
move -1.45 0 0
move 0 0 -5
wait 0.001

speed 0.5

trigvalverel 0.09 0.5

trigwait 0.01
move 0 0.5 0
move 0.5 0 0
move 0 -0.5 0
move -0.5 0 0
move 0.25 0.25 0
valverel 0 5
speed 5
```

Figure C.2 - *Script that prints the first layer of the DPAM parallel plate capacitor.*

```
speed 3
trigvalverel 0.34 1
trigwait 0.01
move 0 1.5 0
move 2.5 0 0
move 0 -1.6 0
move -2.40 0 0
move 0 1.55 0
move 0.2 0 0
move 0 -1.5 0
move 0.2 0 0
move 0 1.5 0
move 0.2 0 0
move 0 -1.5 0
move 0.2 0 0
move 0 1.5 0
move 0.2 0 0
move 0 -1.5 0
move 0.2 0 0
move 0 1.5 0
move 0.2 0 0
move 0 -1.5 0
move 0.2 0 0
move 0 1.5 0
move 0.2 0 0
move 0 -1.5 0
move 0.2 0 0
move 0 1.5 0
valverel 0 5
speed 5
```

Figure C.3 - *Script that prints the dielectric layer of the DPAM parallel plate capacitor.*

```
speed 3
trigvalverel 0.1 0.3
trigwait 0.01
move0 1.4 0
move2.4 0 0
move0 -1.4 0
move-2.30 0 0
move0 1.4 0
move0.2 0 0
move0 -1.4 0
move0.2 0 0
move0 1.4 0
move0.2 0 0
move0 -1.4 0
move0.2 0 0
move0 1.4 0
move0.2 0 0
move0 -1.4 0
move0.2 0 0
move0 1.4 0
move0.2 0 0
move0 -1.4 0
move0.2 0 0
move0 1.4 0
move0.2 0 0
move0 -1.4 0
move0.2 0 0
move0 1.4 0
valverel 0 5
speed 5
```

Figure C.4 - *Script that prints the third layer of the DPAM parallel plate capacitor.*