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Nonlinear Properties of Nanoscale Barium Strontium Titanate Microwave Varactors

by

Tony Price

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
Department of Electrical Engineering
College of Engineering
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Keywords: ferroelectrics, grain size, two-tone measurements, intermodulation distortion,
third order intercept

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Dedication

This work is dedicated to all underprivileged youth, especially those in Flint, MI. The completion of this work shows that the solicitation of drugs and involvement in violent behavior are not necessary to acquire an improved style of living. It also serves as proof that you can come from anywhere and do anything, as long as you really, really, really want to do it!

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Abstract

Barium strontium titanate thin film varactors have been widely investigated for the purpose of creating tunable front-ends for RF and microwave systems. There is an abundance of literature observing the capacitance-voltage behavior and methods on improving tunability. However, there is a lack of thorough investigations on the nonlinear behavior, specifically the third order intermodulation distortion, and the parameters that impact it. There is also a research void that needs to be filled for nanoscale barium strontium titanate varactors as nanotechnology becomes increasingly prevalent in the design of RF and microwave components.

This work aims to advance the understanding of nonlinear properties of barium strontium titanate varactors. Temperature and voltage impacts on the third order intermodulation distortion products of BST varactors are observed by two-tone measurements. The material properties of the films are correlated with the nonlinear behavior of the varactors. Additionally, size reduction capabilities are shown by fabricating planar barium strontium titanate interdigital varactors with nanoscale size gaps between the electrodes. Modeling techniques are also investigated.

Chapter 1 Introduction

1.1 Motivation

Consumers are constantly looking for faster, more portable, and affordable devices with greater functionality. Electronic device and circuit miniaturization governed by Moore's Law has played a key role in the pursuit of this goal. Over the past 40 years, advances in semiconductor processing have helped to reduce transistor dimensions from 10μm down to 30nm [1].

In an effort to keep up with Moore's Law, there has been an explosion of research in nanotechnology, particularly involving the application of carbon nanotubes (CNTs) and nanoscale complementary metal oxide semiconductor (CMOS) devices. Such applications include logic, energy storage using nanotube capacitors, and nanotube transistors for RF purposes [1-5]. As more frequency allocation becomes necessary, RF engineers are now looking towards the THz range for many applications including amplifiers and antennas for RFID tags. Nanoscale devices such as nanotube radios and antennas are capable of operating at that frequency range [6]. However, other arenas need to be investigated to allow more tunability and frequency agility at the nanoscale.

1.2 Problem Definition

There is an increased demand for low cost, frequency agile wireless communication systems which translates to an increased need for reconfigurable RF components for tunable front ends. Due to their field dependent permittivity, ferroelectric thin films, such

as barium strontium titanate (BST), have been widely researched and recognized as a leading solution for this issue. However, there is still a lack of knowledge regarding the nonlinear properties of BST devices and accurate models to predict the nonlinear behavior. Additionally, there is a gap that needs to be bridged between the material properties of the BST thin films and the microwave performance of BST based microwave devices.

As carbon nanotubes and other nanoscale technologies become more prevalent for RF and microwave devices, it is necessary to move in the direction of integrating nanoscale BST devices with existing nanoscale RF and microwave technology. Doing so could produce more compact frequency agile systems capable of operating in the THz range and advancing the overall capabilities of RF systems. Currently, there is little information on nanoscale barium strontium titanate devices; thus, a challenge is presented.

1.3 Research Objectives

The primary objective of this work is to examine the nonlinear behavior of BST varactors for RF and microwave applications. A more detailed understanding of the nonlinear properties can assist in integrating BST varactors into RF and microwave components such as phase shifters, tunable filters and nonlinear transmission lines for modulation purposes. Before a BST varactor is integrated into an RF component, it would be beneficial for its nonlinear performance to be well analyzed and properly modeled. Therefore, a thorough investigation of existing BST varactor models is needed to see how accurately they predict the nonlinear behavior.

BST IDCs with microscale gaps have been widely investigated. By fabricating planar BST varactors with nanoscale size critical features, a much higher capacitance density will be provided along with higher field strength in the BST film for given DC voltages and RF signal power levels. Currently, there is limited literature discussing how the nonlinear behavior of BST varactors is impacted by reducing the critical dimensions down to the nanoscale, and this needs to be addressed.

1.4 Contributions

The major contributions of this work revolve around advancing the understanding of the nonlinear behavior of planar BST varactors. Various parameters are considered while investigating the nonlinear behavior. These parameters include material properties such as substrate of choice and BST film quality. Other parameters examined, beyond the material influences, include externally applied DC bias voltage, temperature, and RF power. Details on reducing the size of planar BST varactors by using nanoscale gaps instead of microscale gaps are also discussed.

Single crystalline substrates have generally been the substrate of choice for growing high quality BST films. However, in this work, a comparison of the nonlinear behavior is presented for BST varactors fabricated on single crystalline and polycrystalline substrate materials showing that higher tunability and more nonlinearity can be obtained from the cheaper polycrystalline substrates for a given film deposition technique.

By completing two-tone measurements of BST varactors, third-order intermodulation distortion (IMD) products are analyzed with respect to input RF power. A relative minimum or dip is observed in the third-order IMD. This dip can potentially cause inaccuracies when trying to predict the power levels of the third-order IMD. Additionally, it has been observed that the input RF power in which the dip is located along with its

depth are both dependent on the applied DC voltage and the temperature of the environment that the measured BST varactor is subjected to.

Another aspect of this work involves the correlation of the nonlinear RF behavior of BST varactors to the material properties of the BST films used to fabricate them. S-parameter and two-tone measurements are taken on BST varactors that contain films of various surface roughness and grain size to observe how these two particular material properties impact the tunability and the power level of the third-order IMD products, respectively. A correlation as such could be quite useful when designing BST varactors as precursor values for roughness and grain size of the film can be established for designing varactors and microwave components to yield specified nonlinear traits.

Lastly, planar BST varactors with nanoscale gap sizes are presented. It is shown that planar nanoscale varactors can be designed to give higher capacitance and tunability than planar varactors with microscale gap sizes. Additionally, the area of the planar BST varactor can be reduced by over 80% when using a device with nanoscale gaps versus using one with microscale gaps. This can be very useful for the purpose of size reduction for RF components and systems.

1.5 Dissertation Structure

Chapter 2 contains background information on ferroelectric materials. Properties such as electric-field and temperature dependent permittivity are discussed. A comparison of ferroelectrics and its competing technologies (semiconductor and MEMS) is presented. Details are given on current RF applications of ferroelectric thin films along with current models and their shortcomings.

The most significant element of a tunable ferroelectric RF device is the ferroelectric thin film. Chapter 3 discusses techniques used in this work for depositing the barium

strontium titanate thin films for tunable capacitors in addition to post deposition treatment. An important component of this research involves correlating the material properties of the BST thin film to the RF properties of the tunable capacitors that are fabricated with these films. The thin film material properties examined include crystallinity, grain size and surface roughness. Metrology tools including X-ray diffraction (XRD), transmission electron microscopy (TEM) and atomic force microscopy (AFM) and procedures used for obtaining these parameters are discussed.

Design and fabrication methods for the microscale and nanoscale capacitors are given in Chapters 4 and 5, respectively. Simulation details are outlined for designing the planar capacitors. Conventional lithography procedures are used for patterning the BST and constructing the electrodes for the microscale capacitors. The conventional lithography tools used for this work yield devices with a limited critical dimension of 5μm which presents a challenge when trying to reduce the planar capacitor gap size down to the nanoscale. Electron beam lithography is used to obtain the desired nanoscale dimensions for this work, and the procedures for this technique are discussed.

Chapter 6 marks the transition from the materials and fabrication related work to the RF and microwave analysis. The small-signal measurement techniques are outlined along with the methods used for extracting capacitance and calculating tunability from measured S-parameter data. Details are given on the various types of measurement conditions used for analyzing the capacitance and tunability when devices are subjected to various temperatures.

In Chapter 7, a review of previous nonlinear characterization methods of BST varactors is presented in addition to nonlinear RF measurement results from this work followed by a summary of device modeling presented in Chapter 8.

Concluding remarks are found in Chapter 9 summarizing the major contributions of this work and the potential areas to be examined for future work.

Chapter 2 Background of Ferroelectric Devices

2.1 Introduction

Over the past few decades, the use of wireless communication systems and their capabilities have grown at an exponential rate. Once utilized primarily for defense and emergency broadcast purposes, wireless systems are now commercially available to the public for enumerable applications from cellular phones and Bluetooth headsets to video game consoles with wireless control units. Below is a list of examples of common uses of wireless systems:

- PDAs and internet access on mobile phones
- GPS
- Garage door openers
- TV remotes
- Headphones

The use of wireless technology in common household products has become more and more feasible because of the miniaturization of the circuit components through semiconductor technology. With the advancements in integrated circuit (IC) technology, large components that were once on breadboards and printed circuit boards were able to be reduced down to smaller chips. Techniques, such as ion implantation, provided breakthroughs in easing the production of p-n junctions for semiconductor diodes and transistors (which can be used as capacitors in filter design and amplifiers respectively) and helped to overcome the challenges of size and bulkiness of vacuum tube

computing/systems. RF circuit components were miniaturized down to the micro-scale allowing RF transceiver designs to be implemented on relatively smaller chips. The reduction in required real estate paved the way for more complex frequency agile communication systems that include components such as tunable filters, matching networks, and phase shifters.

2.2 Technology Comparison for Tunable Devices

Semiconductor devices are typically fabricated with crystalline materials such as silicon, gallium arsenide, germanium [7]. These materials are well characterized and the processing methods are mature. The tunability in semiconductor varactor diodes is caused by the variation in the width of the depletion region. The width of the depletion region is adjusted by applying a reverse biased external electric filed across the junction. Changing the width of the region is similar to changing the thickness of the insulating material in a parallel plate capacitor. When the width changes, so does the capacitance. The junction is lightly doped to achieve high tunability. These lightly doped layers, however, can be resistive, causing the varactor diode to be lossy at RF and microwave frequencies [8]. The tuning speed of semiconductor varactor diodes varies from type to type, but they are generally fast devices. The switching is dependent on the transfer of electrons across the depletion or intrinsic regions and this happens on the order of ns to μs depending on the type of diode [9]. The disadvantages of semiconductor devices are poor power handling capability along with increased losses at high frequencies.

RF MEMS switches have the benefits of being able to handle moderately high power along with exhibiting low loss at RF frequencies [10]. Since they are physical switches that are either open or closed (not in contact or in contact), they have high isolation. The fact that they are physical switches, however, comes with its downfalls as well. Metal-to-

metal contact RF MEMS switches have been known to fail by remaining in the closed positioned when they are supposed to be open due to the metal pads sticking to each other. Although there has been significant progress in addressing this issue for metal-to metal contact switches, there is still a similar problem with capacitive RF MEMS switches in which the flexible cantilever beam sticks to the dielectric material due to charging. They also have slower switching speeds compared to semiconductor devices (>1 μs), and they can be expensive to manufacture due to the requirement of vacuum packaging [9]. Research with MEMS varactors has not accelerated like that of MEMS switches because of the abundance of low loss silicon and GaAs varactors [7]. Additionally, they suffer from low tunability and bias-noise effects [7, 11].

Over the past few decades, ferroelectric materials have become popular candidates for tunable RF and microwave components [12-15]. Ferroelectrics have a relative permittivity that changes with an externally applied electric field. When used as the dielectric/insulating material in capacitors, the device will take on the behavior of a varactor due to the capacitance value changing with an applied voltage. Although the reported tunability may not be as high for ferroelectric varactors when compared to semiconductor varactors, they have fast switching speeds (ps – ns) and low losses at RF frequencies [16, 17]. Additionally, they are less prone to fail compared to MEMS switches since the tuning is caused by an electrical characteristic of the material instead of a mechanical switch. They also have a symmetric capacitive-voltage relationship which can ease the design of biasing networks used with these types of devices. The main concern with ferroelectric devices is that they have to be operated above a certain temperature to avoid hysteretic behavior. This is further explained in the next section. Table 2-1 summarizes the advantages and disadvantages of each of the previously mentioned technologies.

Table 2-1: Comparison of Technologies for Tunable RF Devices

Technologies	Advantages	Disadvantages
Semiconductor	▪Fast tuning speeds ▪High Tunability ▪ Relatively small size (microns)	▪Suffer from junction noise ▪Poor power handling capability (<1mW) ▪Q degradation at higher frequencies
MEMS	▪Can handle high power levels ▪Low loss at RF frequencies	▪Low tunability ▪Slow switching speed ▪Expensive packaging
Ferroelectrics (BST)	▪Fast tuning speed (ns, ps) ▪Low losses at RF frequencies ▪Symmetric C-V curve (no requirement for reverse biasing)	▪ Must operate above Curie temperature to avoid hysteresis

2.3 Ferroelectrics

2.3.1 Theory of Ferroelectrics

Some dielectric materials can exhibit spontaneous polarization in which the positive charges and the negatively charged electron cloud are not concentric when there is no external electric field being applied. When this spontaneous polarization can be reversed by an electric field, then the material is defined as a ferroelectric [18].

Ferroelectric materials can exist in two phases: ferroelectric (polar) phase and paraelectric phase. While in the ferroelectric phase, the material is still subject to spontaneous polarization. Therefore, it may not follow the same polarization-field relationship at all times while in the ferroelectric phase as shown in Figure 2-1 (a). From a mathematical perspective, the polarization-field relationship is not functional for the ferroelectric phase since there could be multiple values of polarization for the one particular value of electric field. Because of the hysteretic behavior of the polarization-

field relationship while in the ferroelectric phase, the permittivity-field curve will not be symmetric. These effects for the ferroelectric phase are shown in Figure 2-1 (a-b).

Above some critical temperature, known as the Curie temperature, the spontaneous polarization in ferroelectrics disappears [19]. When this occurs, the ferroelectric material is said to be in a paraelectric phase. Notice in Figure 2-1 (c), there are no longer any hysteretic effects observed in the polarization-field relationship. The permittivity-field relationship is also symmetric about the y-axis as shown in Figure 2-1 (d). Hence, the capacitance-voltage (C-V) curve will also be symmetric for a ferroelectric varactor while in the paraelectric phase. Operating in the paraelectric phase is preferred when using ferroelectric thin films for microwave devices because it is easier to predict their behavior compared to the ferroelectric phase. Additionally, the dielectric loss is greater in the ferroelectric phase due to increased friction in the domain walls caused by the spontaneous polarization [20].

2.3.2 Barium Strontium Titanate (BST)

Several ferroelectric materials have been considered for tunable microwave devices such as PbTiO3 and LiNbO3 [21, 22] . As of now, BST is one of the most attractive ferroelectric materials due to its high permittivity, high tunability and low loss at RF frequencies [17, 23]. BST has a perovskite crystal structure (ABO_3) which is cubic in nature (shown in Figure 2-2) and has a chemical formula of $Ba_xSr_{1-x}TiO_3$. Just like any other ferroelectric, it can be either in ferroelectric phase (exhibiting spontaneous polarization) or the paraelectric phase (no spontaneous polarization). However, the Curie temperature for BST can be adjusted by varying the barium and strontium concentrations. Previous research has shown that if the barium concentration is kept at

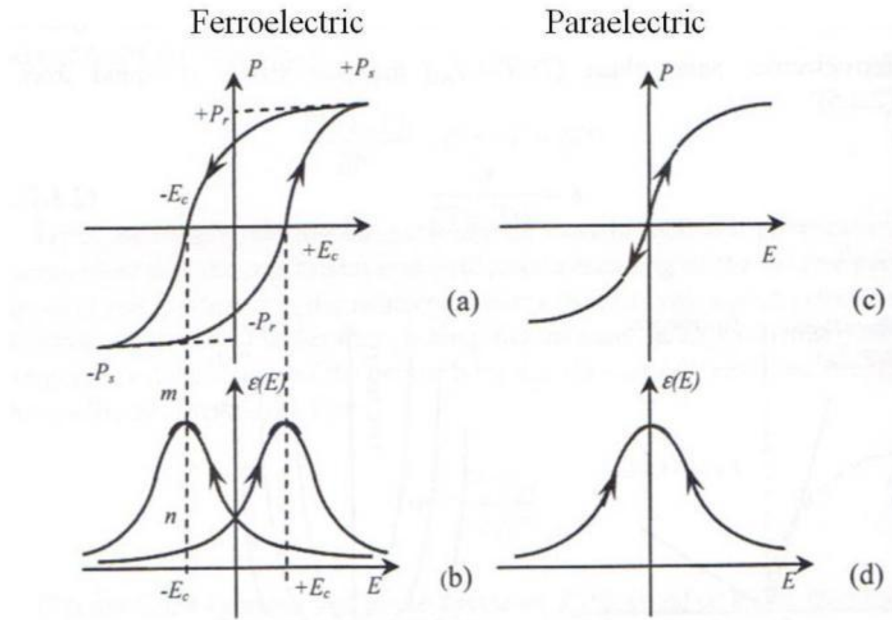


Figure 2-1: Field Dependent Polarization and Permittivity for Ferroelectrics
(a) & (b): Ferroelectric Phase, (c) & (d): Paraelectric Phase

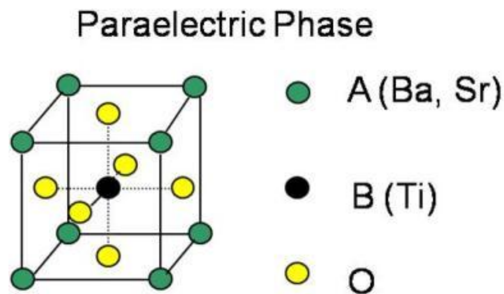


Figure 2-2: BST Cubic Structure

0.6 and below ($x \leq 0.6$), then the Curie temperature of the BST material will be well below room temperature [24]. This is a very advantageous characteristic because microwave devices can be designed with BST films that have been engineered to operate in the

paraelectric phase at and above room temperature. Therefore, the electrical behavior of a BST device in the paraelectric phase would be more stable with respect to temperature as shown in Figure 2-3 [9].

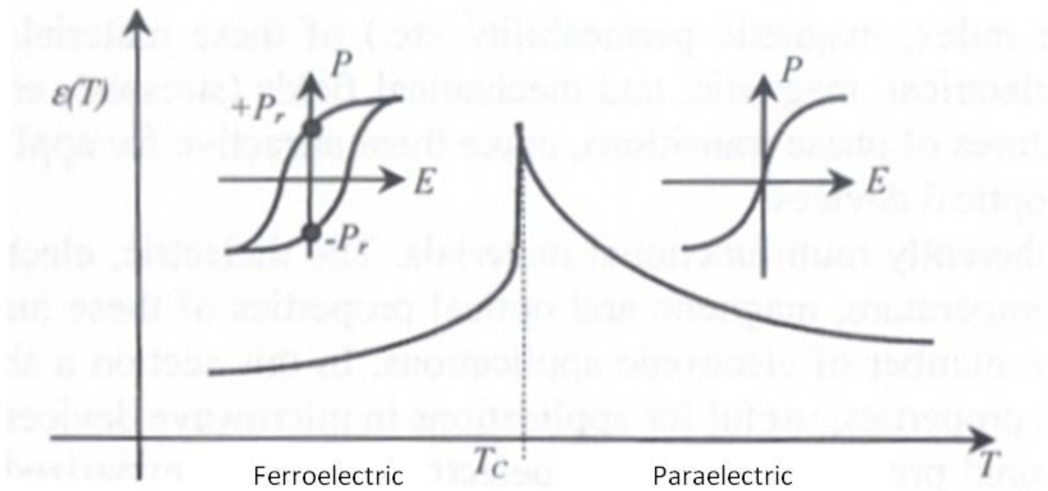


Figure 2-3: Permittivity vs. Temperature for Ferroelectric Materials

For the purpose of this work, the BST will be in the paraelectric phase. In the paraelectric phase, the crystal has no spontaneous polarization and the cubic structure is symmetric. When an E-field is applied, there is an ionic polarization that takes place within the BST molecule. For simplicity, a 1 dimensional model with springs can be used to illustrate how the titanium ion moves about its equilibrium point [9]. When there is no applied E-field, the titanium ion rests at its equilibrium point at the center of the cubic structure as shown in Figure 2-4(a). However, the titanium ion will shift in the direction of an externally applied field as shown in Figure 2-4(b), and the distance of the shift will depend on the strength of the electric field. As the titanium ion shifts from its equilibrium point, its free energy increases and is characterized by a parabolic dependence [9]. This increase in free energy causes the titanium ion to begin to lose its capability to take on

more energy. In other words, the dielectric material will begin to lose its ability to take on more charge from the externally applied field. The dielectric constant of a material indicates its charge (energy) storage capability: the larger its value, the greater its ability to store charge (energy) [19]. Figure 2-5 shows that the free energy of the titanium ion is inversely related to the permittivity of the film, theoretically. Therefore, the shifting of the titanium ion is the physical mechanism that allows the permittivity of the BST to change with an applied field, which in turn makes it a candidate for tunable microwave devices.

2.4 BST Devices

The previously described tunable characteristic of BST has made it a popular material to integrate into capacitors; hence making them varactors (tunable capacitors). BST varactors have a C-V relationship that is directly related to the permittivity-field relationship. Figure 2-6 shows a plot of capacitance vs. voltage for a BST varactor simulated using Agilent's Advanced Design System (ADS). Notice the similarities that it has with the permittivity-field curve illustrated in Figure 2-5. Compared to the previously mentioned technologies, ferroelectric devices are appealing for microwave applications due to their simple fabrication process, fast analog-switching speed, compatibility with non-hermetic packaging, working frequencies above 5 GHz, compact size, and low DC control voltage [17].

BST varactors have gained significant attention because they can be used to make reconfigurable components for the front ends of wireless communication systems. For instance, Kim et al have reported phase shifts of up to 135° using phase shifters that were designed with planar BST interdigitated capacitors (IDCs) [25]. Other examples of BST based phase shifters can be found in [26, 27]. In addition to phase shifters, BST

varactors have also been used for the design of phased array antennas, such as the steerable reflect-array mentioned in [28].

Having the capability to adjust the frequency of operation in communication systems is an advantageous quality. Most tunable filters in defense and satellite communication systems rely on mechanically tunable filters or switched capacitor filter banks which

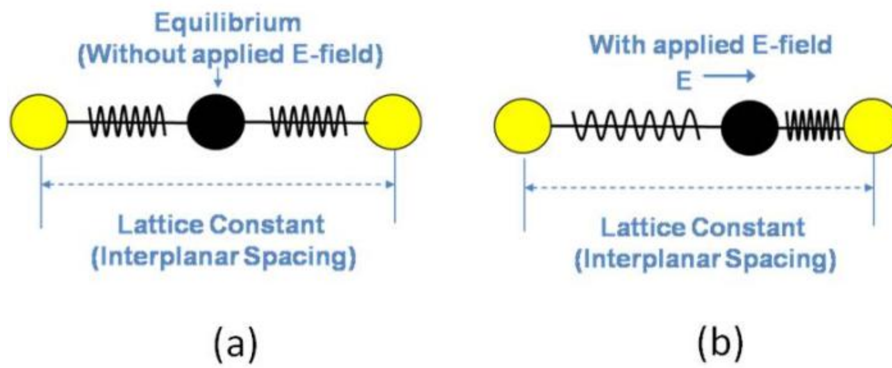


Figure 2-4: Ionic Polarization of BST
(a) No Applied E-Field (b) With Applied E-Field

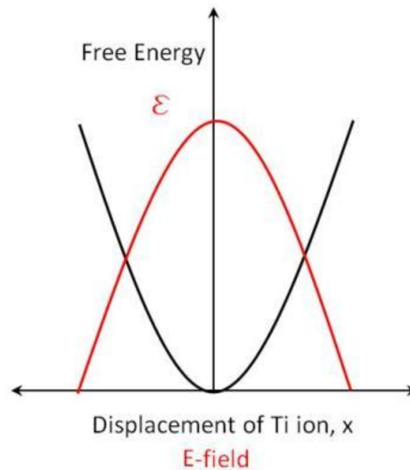


Figure 2-5: Free Energy & Permittivity vs. Ti Ion Displacement & E-field, Respectively

suffer from low tuning speeds and the lack of a continuous tuning range, respectively [29]. For this reason, tunable filters using BST varactors are being investigated. Nath et al used BST interdigital capacitors (IDCs) to fabricate a bandpass filter in which the center frequency shifted from 2.44 GHz to 2.88 GHz using a bias voltage of up to 200V while maintaining a 1dB bandwidth of 400 MHz [13]. Other examples of tunable filters with integrated BST varactors are discussed in [30] and [31].

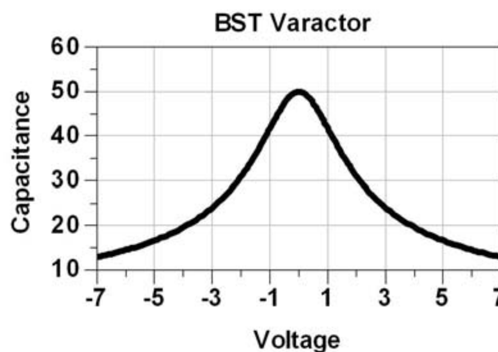


Figure 2-6: Capacitance (pF) vs. DC Voltage (V) for Simulated BST Varactor

Impedance matching networks are essential in wireless communication systems. They are particularly used between the antenna and the front end of the system. The antennas, primarily in handsets, are subject to the surrounding environment which may also change their input impedance [32]. For this reason, BST varactors have been integrated into impedance matching networks to make them tunable. Vicki Chen et al, reported a tunable impedance transformation ratio of 2:1 to 4:1 using BST varactors [33]. In [33], a tunable matching network is also designed to shift the operating frequency of the system to ensure that the antenna of the system was performing at high efficiency. Tunable impedance matching networks have also been reported in [34] and [35].

As reported, there are several RF and microwave applications for tunable BST varactors. However, more work needs to be done to fully understand the nonlinearity of BST devices in addition to developing proper models that will predict the nonlinear behavior.

Chapter 3 BST Film Deposition and Analysis

3.1 Introduction

Highly tunable and low loss barium strontium titanate films are necessary to produce tunable microwave devices. There are several deposition techniques available to obtain BST thin films of high quality. Popular methods include sol-gel deposition, pulsed-laser deposition (PLD), metal organic chemical vapor deposition (MOCVD) and RF sputtering [27, 36-41]. Table 3-1 shows the advantages and disadvantages of each method [42]. Both sol-gel and MOCVD require the use of precursors which can be expensive [43]. Another downfall of the sol-gel technique is that it's difficult to control the composition of the film. PLD generally produces films with good composition control; however, particulates from the laser ablation on the target are usually formed and deposited with the film. Additionally, the deposition area is relatively small for PLD [44]. RF sputtering is a popular deposition technique for both research and industrial purposes. This method produces smooth, stoichiometric films that adhere well to the substrate and are uniform in thickness over large areas [42]. For this work, RF sputtering is the method of choice for depositing BST thin films.

Previous studies have shown that the BST film composition has an impact on the tunability [45-48]. As the barium content of the film increases, the tunability also increases. The tradeoff of increasing the barium content is that the Curie temperature of the film rises with it.

Table 3-1: BST Deposition Techniques

Method	Advantages	Disadvantages
Sol-Gel	Inexpensive, low capital investment Rapid sampling of materials Quickly produce new materials	Phase control Composition Control Morphology Scalability
Sputtering	Uniformity Scalability Low growth Temperature Standard IC Processing	Residual Stresses Point defect Concentration
Pulsed Laser Deposition	Non-equilibrium deposition Highly stoichiometric films Quickly produce new materials	Particulate formation Uniformity Morphology
MOCVD	Uniformity Morphology Composition Control	Expensive Precursor availability Precursor stability

As mentioned in the previous chapter, the BST films for this work will be kept in the paraelectric phase at room temperature to avoid hysteretic behavior in the devices; therefore, the film composition of the RF sputtering target must be chosen accordingly. For this work, $Ba_{0.5}Sr_{0.5}TiO_3$ or BST (50/50) is chosen to ensure that the films will be in paraelectric phase at room temperature.

Another important consideration for fabricating planar BST varactors is the substrate. In the case of planar structures, the BST film is grown directly on the substrate which will have a significant impact on the overall quality of the film. Therefore, the substrate must be chosen carefully.

Popular substrates for planar BST devices include magnesium oxide (MgO), lanthanum aluminum oxide (LAO), sapphire, and polycrystalline alumina [14, 49-55]. The primary advantage of MgO, LAO, and sapphire substrates is that they are single crystalline materials. When BST thin films are grown on single crystalline substrates, it is more likely that the films will be epitaxial leading to higher permittivity and increased

tunability. The caveat presented with using these types of substrates is the high cost. For this reason, polycrystalline alumina has been investigated for making tunable RF devices. In addition to being a cheaper alternative when compared to the previously mentioned materials, research has shown that highly tunable BST devices can be obtained when BST films deposited on alumina go through post-deposition treatment [56, 57]. Although there are some comparative results of BST varactors fabricated on alumina versus MgO presented in this work, polycrystalline alumina is the primary substrate of choice for the bulk of the investigations. Materials characterization is performed for BST films on alumina substrates only.

3.2 RF Sputtering

BST (50/50) films are sputtered onto polycrystalline alumina substrates using an AJA ATC 1800 Sputtering system courtesy of Dr. Gong's group at the University of Central Florida. Within the sputtering chamber, a high-energy plasma is created using an RF power level of 200 Watts along with argon and oxygen gases flowed into the chamber at a ratio of 20:2.5 respectively. If the RF power is ramped up too quickly, the temperature of the ceramic target will also rise expeditiously causing the target to crack. For this reason, the RF power supplied to the BST target is ramped up to 200 Watts at a rate of 10 Watts/minute. As the plasma bombards the BST sputtering target, BST atoms are released from the target and deposited onto the alumina substrates. Other deposition parameters include a base pressure of 1.5×10^{-7} T, a deposition pressure of 5mT and a temperature of 400°C.

Figure 3-1: AJA RF Sputtering System

3.3 Annealing

To achieve tunable BST RF devices, it is important that the BST films are crystalline. This implies that the atoms of the thin film must be organized in a periodic, repetitive fashion. These clumps of crystallite structures are referred to as grains. If the films are amorphous (atoms randomly oriented), then they will most likely not be tunable. Previous studies show that post deposition annealing is a method that can be used to enhance the crystallinity of BST thin films [58-60]. When BST thin films are annealed, the grains increase in size which also increases the permittivity of the film.

One of the objectives of this work is to analyze the RF properties of BST varactors with varied film qualities. Therefore, samples of BST films on alumina are annealed for various times to obtain several experimental control points of BST film quality. Annealing times include 0, 3, 12, 18, and 24 hours. Samples are annealed in a Fisher Scientific oven in an oxygen ambient environment at a temperature of 900°C. Oxygen is circulated into the oven during the annealing process to prevent oxygen vacancies from forming in the BST film, in turn reducing the RF losses [61]. The temperature is ramped

up to 900°C at a rate of 10°C/min. After the annealing is completed, the samples are allowed to cool down to room temperature while oxygen is still flowing into the oven. Once the oven reaches room temperature, the oxygen is turned off and the samples are then removed.

3.4 X-Ray Diffractometer Measurements (XRD)

X-ray diffraction measurements can be used to analyze the crystallinity, grain size, and lattice constant (also known as interplanar spacing) of a material [62-64]. In XRD measurements, X-rays are transmitted at a range of incident angles. When X-rays are incident upon an atom within a material, they scatter in all directions. However, if the atoms are arranged periodically, then there will be a certain angle in which the scattered X-rays will interfere constructively with one another and be diffracted, as shown in Figure 3-2. At this angle (θ) Bragg's Law shown in Equation 3-1 will be satisfied, and the intensity of the scattered x-rays will be higher than at any other scanned incident angle [65]. The XRD data is generally plotted as diffracted x-ray intensity vs. scan angle, and a peak can be seen at the angle that satisfies Bragg's Law. The full width half max of this peak (B) along with the wavelength of the x-ray (λ) and θ can be used to determine the average grain size (t) using Scherrer's Equation 3-2 the grain size (t) and the interplanar spacing can be obtained from x-rays that are diffracted from the sample for a range of incident angles. K is a shape factor that is usually defined as 0.9.

$$n\lambda = 2d\sin(\theta) \qquad \text{Equation 3-1}$$

$$t = \frac{K\lambda}{B\cos(\theta)} \qquad \text{Equation 3-2}$$

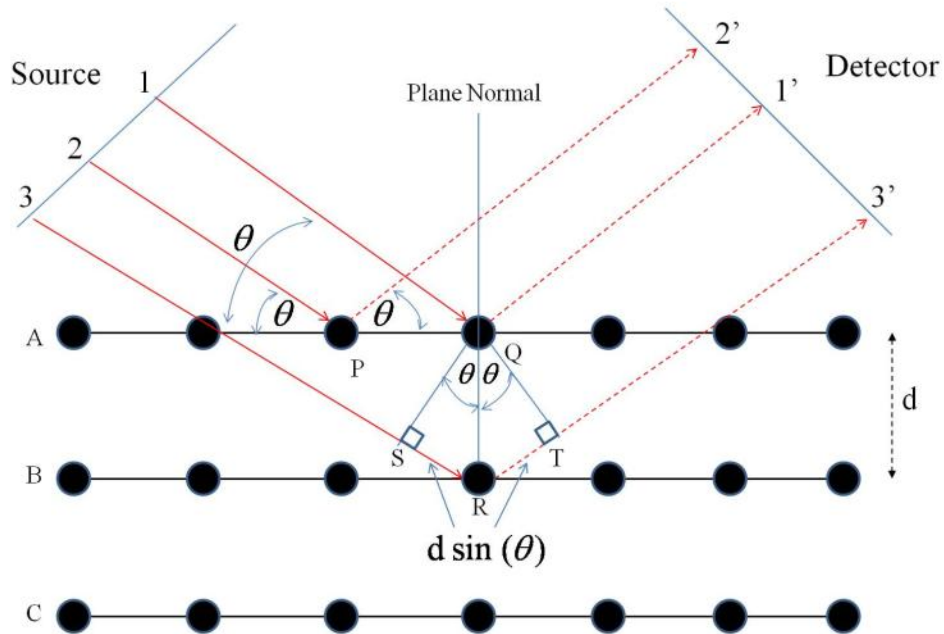


Figure 3-2: XRD Illustration

XRD measurements are taken on samples from each of the annealing times using the Philips XRD system shown in Figure 3-3. The optics settings used for these measurements is listed in Appendix B. The measured data is observed and analyzed using Xpert HighScore software. Initially, data is collected using a typical powder diffraction scanning technique. Figure 3-4 shows XRD data of both a blank polycrystalline alumina sample without BST and a polycrystalline alumina sample with a 300nm thick blanket layer of BST (50/50) film that is annealed in oxygen for 12 hours. All of the peaks that are displayed in the top graph correspond to the various crystal orientations of polycrystalline alumina sample. This is also true for the data set at the bottom of the Figure 3-4 except for the small peak located at 32°. This peak corresponds to the BST thin film on top of the alumina substrate.

Figure 3-3: Philips XRD System

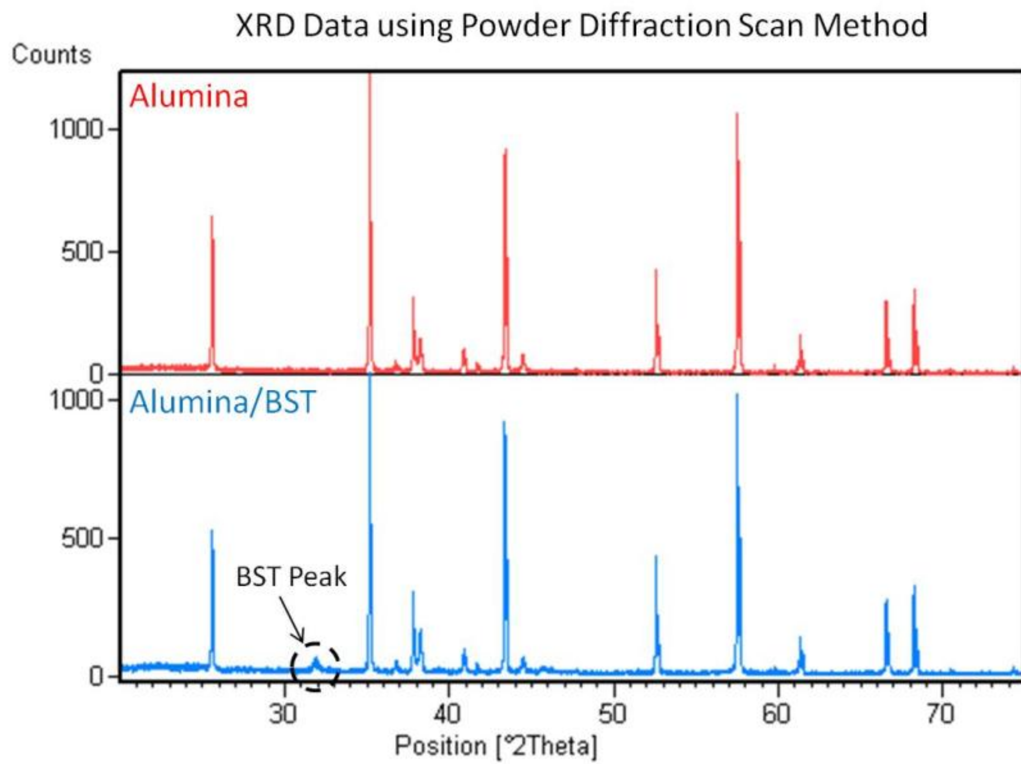


Figure 3-4: XRD Data of Bare Alumina Sample (top) and Alumina/BST Sample (bottom)

Since the BST peak is close to the noise floor when compared to the alumina peaks, it is difficult to perform a trustworthy analysis of the crystallinity of the BST film using the powder diffraction scan data. Therefore, the grazing incidence method for XRD measurements is investigated.

3.4.1 Grazing Incidence Technique

In order to properly measure the BST films, grazing incidence XRD (GI-XRD) measurements are taken. With this technique, the incident angle of the X-rays to the substrate is fixed at a low value typically below 1°. The low angle of incidence allows the X-rays to be concentrated in the BST thin film and prevents them from penetrating the substrate. Since the majority of the incident X-rays are contained within the thin film, most of the diffracted X-rays are going to be generated within the thin film instead of the substrate. This will cause the intensity of the detected BST peaks to increase above the noise floor of the measured data while lowering the intensity of the substrate peaks. Figure 3-5 shows measured data collected by GI-XRD for a 12 hour annealed alumina/BST sample. The incident angle is fixed at 0.6° which raises the intensity of the BST peak that was barely detected before using the powder diffraction technique. This low angle of incidence also helps to detect more BST peaks. The dominant peak at 32° corresponds to a <110> orientation. However, Figure 3-6 shows that when the GI-XRD method is used to measure non-annealed BST films on alumina, no peaks are detected for the BST film. This confirms that the non-annealed BST films are amorphous and post deposition annealing is needed to make them polycrystalline.

GI-XRD measurements are used to collect data for each of the annealing conditions used. To extract the grain size for each annealing condition, the FWHM value of the dominant peak is used from the XRD data. However, a close observation of the peaks

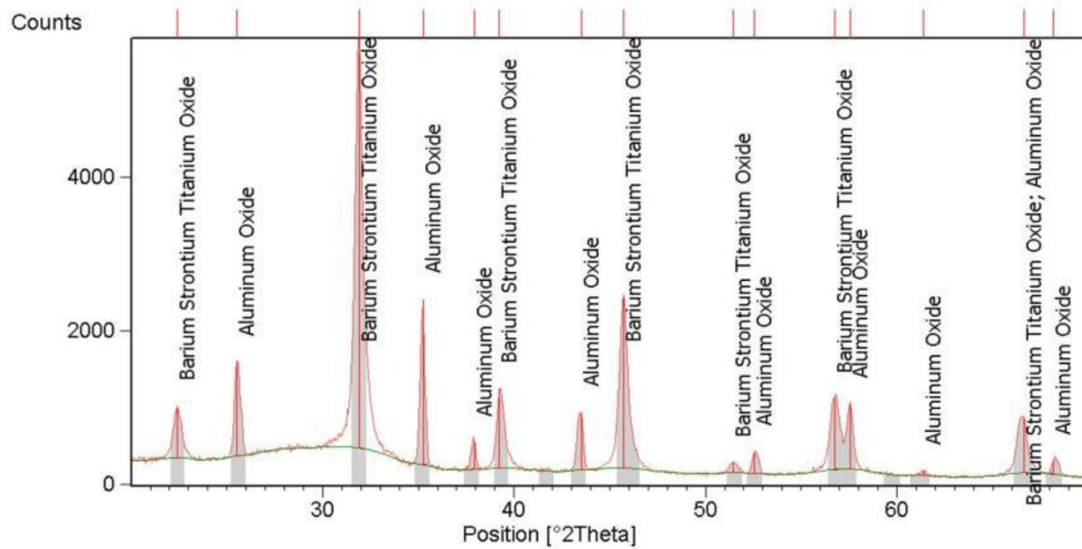


Figure 3-5: GI-XRD Data of 12 Hour Annealed BST on Alumina

shows that other than the non-annealed films, the FWHM does not vary with respect to annealing time. Therefore, the extracted grain size calculated from Scherrer's Formula does not vary either. This problem stems from either the grain size of the film not changing significantly for the various anneal times or from limitations of the available diffracted beam optic configurations of the Philips XRD system. To resolve this issue, a lanthanum boron (LaB_6) powder standard from the National Institute of Standards and Technology (NIST) is measured using the same GI-XRD method that is used to measure the alumina/BST samples. The NIST standard theoretically has no peak broadening affiliated with it; therefore, it is used to determine the instrumental peak broadening that is caused by the Philips XRD system. The FWHM of the peak observed from the NIST standard is measured to be the same as that of the dominant peaks from the alumina BST/samples. This implies that the instrumental peak broadening caused by the XRD system is so large that the peak width of the measured data cannot be determined accurately using GI-XRD with the available beam optics. Although using the GI-XRD

method with the available system proves to be useful for observing the crystallinity of the BST thin films, it cannot be used to observe the variation in grain size as initially planned. Therefore, alternative methods are needed to determine the grain size of the BST films.

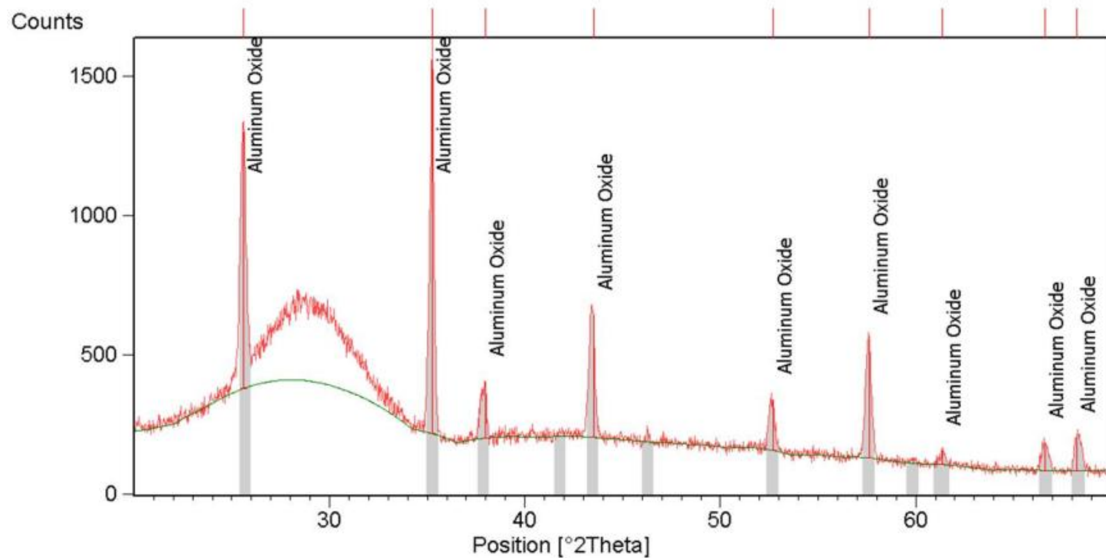


Figure 3-6: GI-XRD Data of Non-Annealed BST on Alumina

3.5 Transmission Electron Microscope Analysis

Transmission electron microscopy (TEM) is investigated to measure the size of the grains within the BST thin films. TEM is powerful enough to achieve atomic-scale resolution [66, 67]. Using TEM, electrons are focused into a very narrow beam using electromagnetic lenses. The electron beam passes through and interacts with the sample causing some of the electrons to scatter. The unscattered electrons travel through the specimen and collected onto a fluorescent screen creating a shadow image of the specimen. Since the electrons are passing through the sample, the image produced gives a view of the sample interior. In order for the electrons to pass through

the sample, it has to be very thin. Therefore, careful procedures must be followed to prepare the alumina/BST samples for TEM measurements.

3.5.1 TEM Sample Preparation

To measure the grain dimension of the BST thin films by TEM, a very thin cross-sectional fragment must be extracted from the alumina/BST samples. This is done using focused ion beam (FIB) milling. Since the alumina substrates are insulative, a thin blanket layer of gold-palladium is sputtered onto the alumina/BST samples to avoid charging effects during the FIB milling process. Once the sample is loaded into the FIB chamber, a platinum bar (10μm long x 1μm wide x 1μm thick) is deposited on the area to be extracted for TEM measurements. The platinum protects the region to be extracted during the trench milling process. A beam of gallium ions is used to mill a trench surrounding the area to be extracted from the alumina/BST sample. Once extracted, the fragment is mounted onto a special holder for TEM measurements as shown in Figure 3-7. Figure 3-8 shows that the thickness of the sample is about 100nm, which is thin enough for TEM measurements.

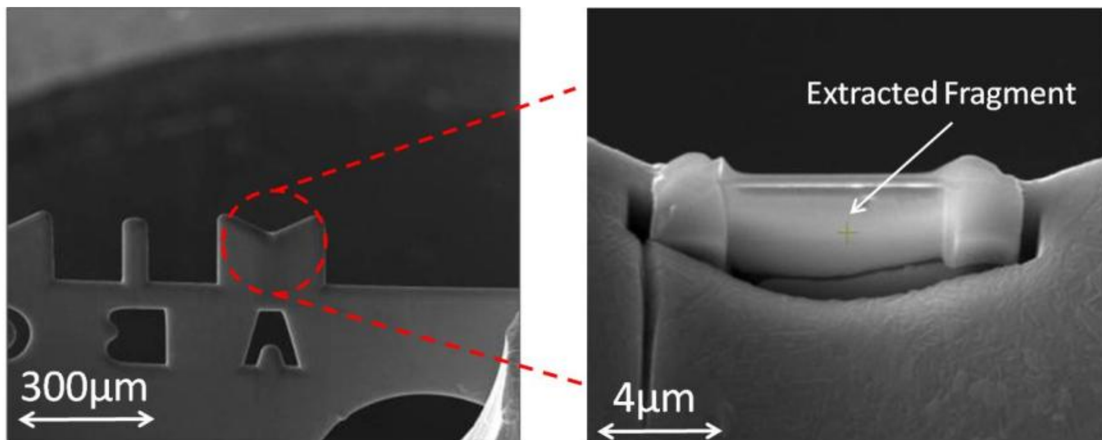


Figure 3-7: SEM Image of Sample Prepared for TEM

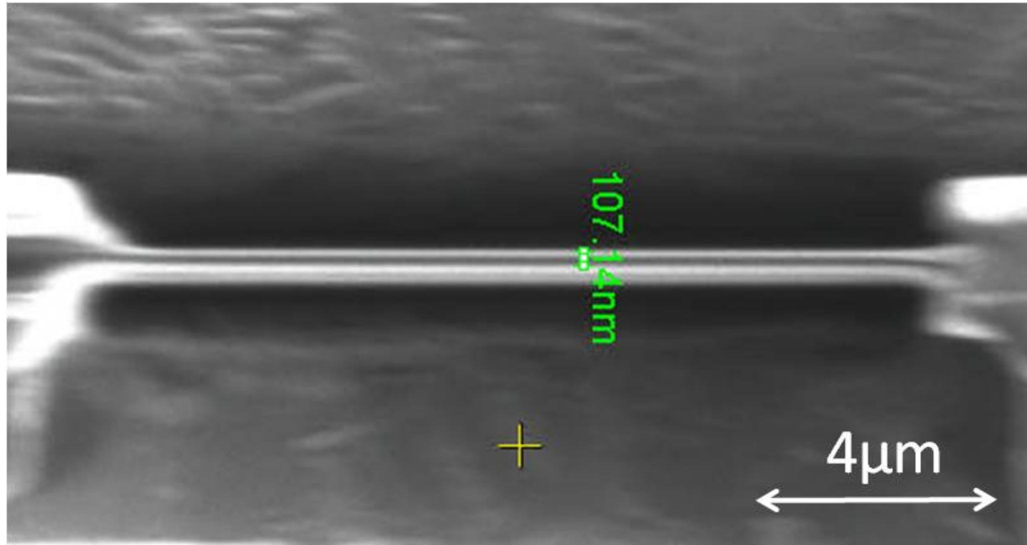


Figure 3-8: SEM Image of Sample Prepared for TEM Displaying Thickness

3.5.2 TEM Measurements

TEM measurements are performed using the Tecnai T20 system shown in Figure 3-9. Initially, a low magnification is used to identify the BST layer within the cross-sectional sample. Figure 3-10 shows a low magnification TEM image of a sample with a BST thin film that is annealed for 12 hours. Small particles/grains are visible throughout the BST film layer at a low magnification. To accurately measure the size of the grains, the magnification is increased to 400,000X to see the atomic planes within the grains. Figure 3-11 shows an image with increased magnification of a grain within the BST film annealed for 12 hours. Within a grain, the atomic planes are all aligned in the same direction. A grain boundary is reached when the alignment changes. This particular grain is measured to be 26nm based on the arrangement of the atomic planes.

TEM is used to obtain an average grain size for each annealing condition used. The TEM software used lacks the statistical analysis capability for calculating the average

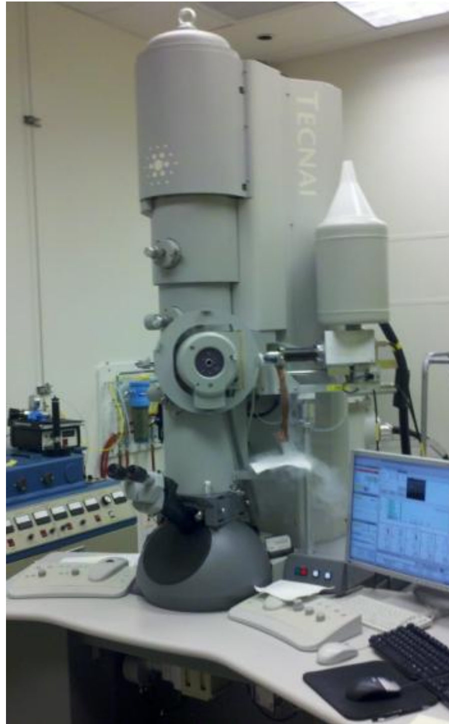


Figure 3-9: Tecnai T20 TEM System

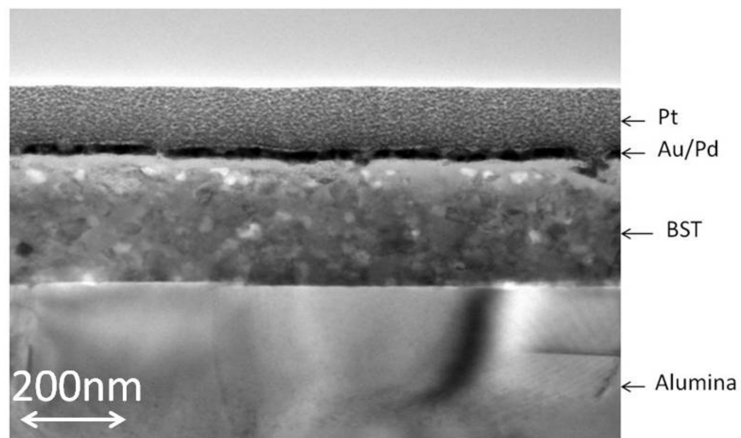


Figure 3-10: TEM of Prepared Sample with 12 Hour Annealed BST

grain size for a given observed area. Therefore, individual grains are randomly selected from each sample and measured. From there, an average grain size is calculated for each annealing condition. Grains are easily observed and measured for each of the

annealing times except for the non-annealed samples. As shown in Figure 3-12, the atoms are randomly positioned throughout the film; therefore, there are no atomic planes in place (no grains) to measure. The average grain size for each annealing condition is shown in Figure 3-13. There is a significant increase in grain size from non-annealed films to those annealed for 3 hours. However, there is very little difference in grain size of films annealed for 3 hours and 12 hours. Another increase in grain size is observed for the 18 hour and 24 hour annealed films when compared to the 12 hour annealed films.

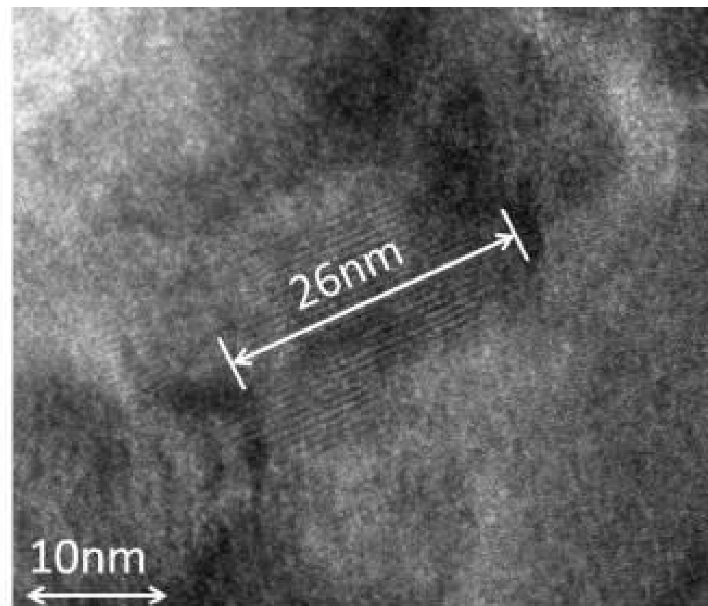


Figure 3-11: TEM of 12 Hour Annealed BST

3.6 BST Film Roughness

In addition to crystallinity, the surface roughness of the BST film was also monitored with respect to annealing time. The film roughness was measured using the Digital Instruments atomic force microscope (AFM) shown in Figure 3-14 . Using this technique, a flexible cantilever with a sharpened tip is brought into close proximity of the

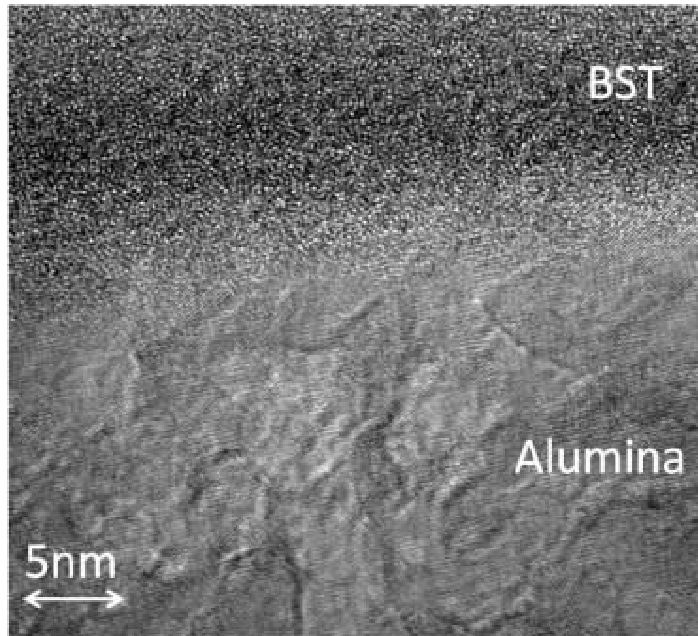


Figure 3-12: TEM of Non-annealed BST on Alumina

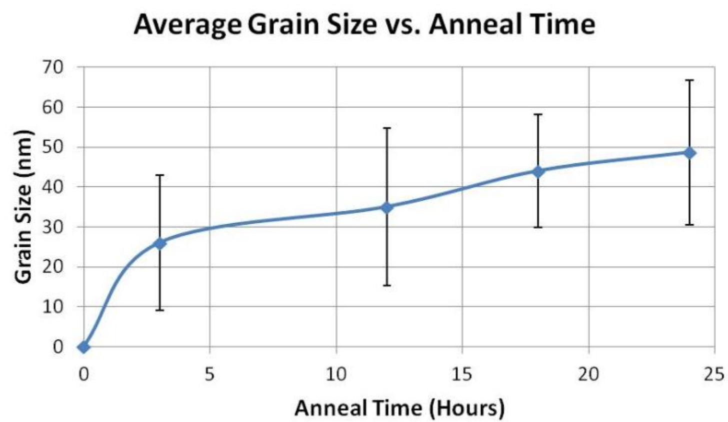
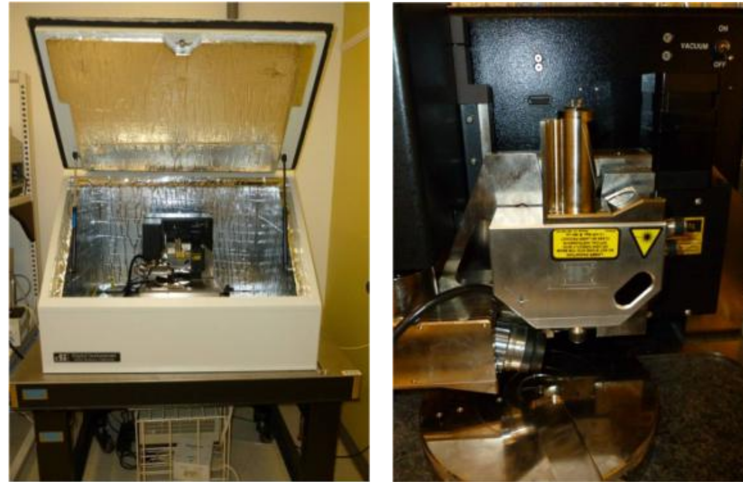


Figure 3-13: Average Grain Size vs. Annealing Time

sample surface, but it never makes physical contact with the sample. Van der Waals interactions between the atoms of the BST film surface and the cantilever tip cause the cantilever to bend as it scans across the sample [68-70]. A laser and detector within the piezohead unit of the AFM tool are used to determine how far the cantilever is deflected

from its natural position due to the atomic interactions between the tip and the film surface. This information is then used to plot the surface topography of the sample.

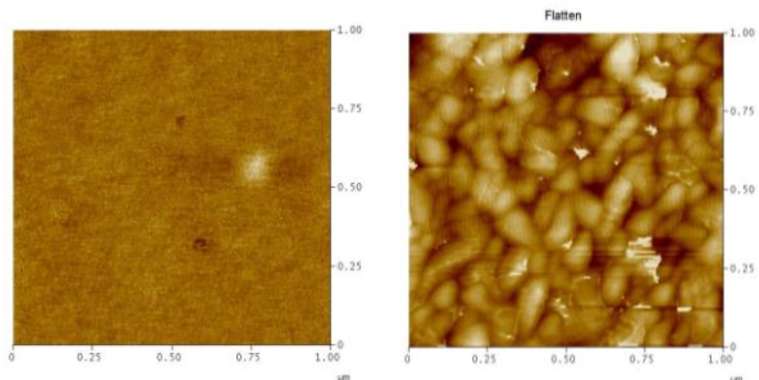


(a) (b)

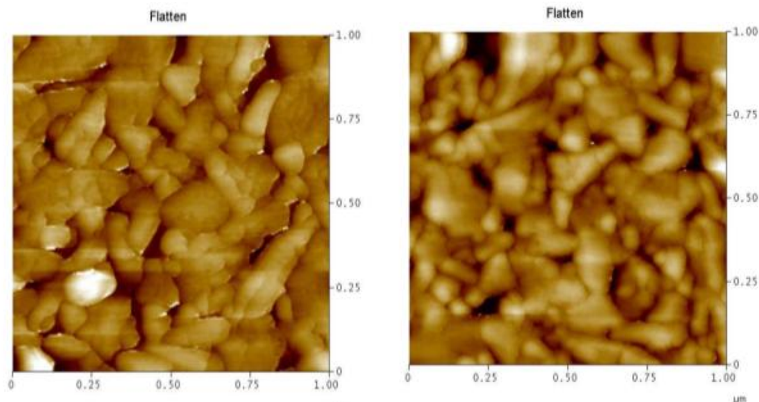
Figure 3-14: Atomic Force Microscopy System
(a) AFM System (b) AFM Piezohead

Three samples from each annealing condition are measured with the AFM tool using a 1μm x 1μm scan area. Each sample is scanned in three different areas. Two-dimensional plots of the surface topography of the BST film from each annealing condition are displayed in Figure 3-15. No grains are observed on the surface of the non-annealed BST films. However, as the BST films are annealed, grains begin to form and appear to coagulate with annealing time. This also confirms where the difference in the XRD data of the annealed and non-annealed BST films stems from. When considering the AFM measurements of the amorphous non-annealed BST film, there are no grains/particles observed; therefore, no peak in the XRD data for this sample is detected either.

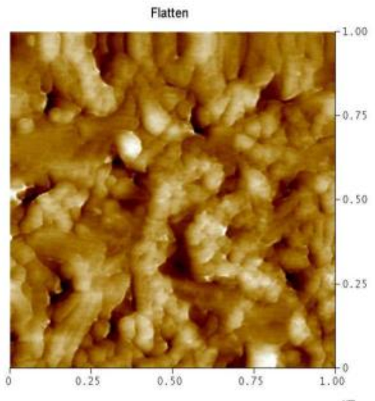
The surface roughness of the film is also impacted by annealing. Figure 3-16 shows the relationship of the surface roughness versus the annealing time for the range of 0 hours – 24 hours. The average surface roughness increases by three fold when comparing non-annealed films to those that were annealed for just three hours. The subsequent increments of annealing time following three hours did not cause as much of a change in the observed film roughness; however, there is a monotonic increase in roughness versus annealing time.



(a) (b)



(c) (d)



(e)

Figure 3-15: AFM Measurements of BST Annealed for Various Times
(a) 0hrs (b) 3hrs (c) 12hrs (d) 18hrs (e) 24hrs

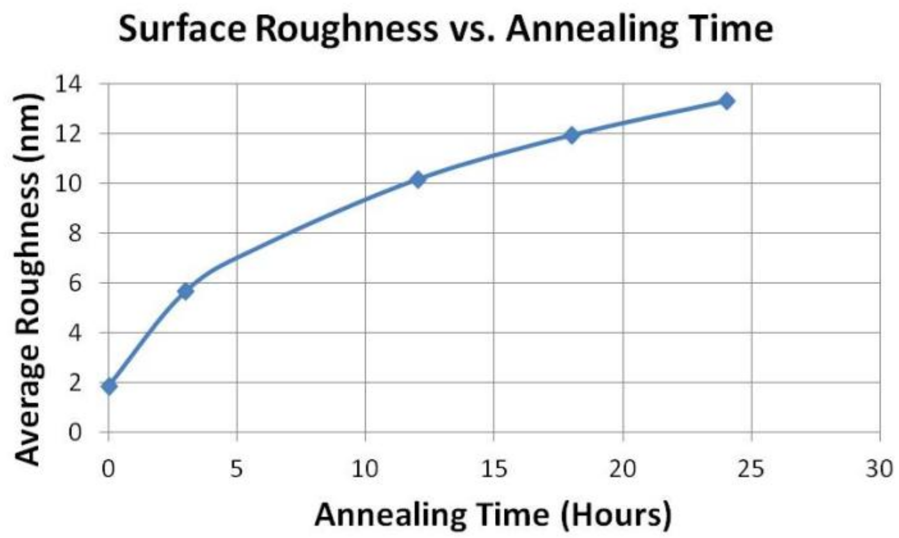


Figure 3-16: BST Film Roughness vs. Annealing Time

Chapter 4 Design and Fabrication of Microscale Planar BST Varactors

4.1 Introduction

Both parallel plate and planar device configurations have been used to make BST varactors for tunable RF components [30, 71-78]. The parallel plate structures come with the advantage of higher tunability due to the overall structure of the device. Planar structures; however, have the advantage of being easier to fabricate. This chapter discusses further details on the tradeoffs of both types of devices. Additionally, design specifications along with fabrication procedures are explained.

4.2 Parallel Plate vs. Planar Structures

Parallel plate or metal-insulator-metal (MIM) devices are popular because of their high tunability compared to planar structures. With the BST film being sandwiched between the two metal electrodes, the electric field of the external bias is mostly confined within the film resulting in higher capacitance and tunability than those obtained from planar structures [38]. The field confinement for a parallel plate and planar structure BST varactor is illustrated in Figure 4-1. The disadvantage of MIM structures is the fabrication complexity presented by the bottom electrode. As discussed in the previous chapter, the BST films typically have to be subjected to a post deposition anneal for enhancing crystallinity. The metal that is chosen for the bottom electrode must be able to withstand the high temperature of the annealing process for extended periods of time. For this reason, platinum is usually the metal of choice for the bottom electrode. However it is very expensive. In addition to that, hillocks can form between the platinum and the BST layers forming a dead layer of non-tunable BST [79, 80].

Planar structures are easier to fabricate than MIM structures [26, 81]. In this case, the BST is deposited directly onto the substrate. Since there is no bottom electrode, there is no concern about forming hillocks when the BST is annealed. Once the BST is annealed, the top electrodes are fabricated on top of the BST film. The tradeoff with this type of structure is that the electric field confinement is sacrificed. The electric field from the external bias is no longer completely confined within the film. As shown in Figure 4-1, only a portion of the electric field between the two electrodes fringes into the BST film, reducing the capacitance and tunability of the device. In an effort to focus more on modeling instead of fabrication, it was decided to use planar BST varactors for this work.

The capacitance and the tunability of planar BST varactors can be varied by adjusting the length of the gap between the electrodes and the gap width. As the gap width is reduced, the capacitance increases. Additionally more of the E-field is confined within the film, increasing the tunability. The length of the gap can also be adjusted to modify the capacitance. By meandering the gap, a given surface area can yield a higher capacitance value. This is what makes the interdigital structure attractive for planar BST varactors.

4.3 IDC Design and Simulations

When designing the interdigital BST capacitors used for this work, the frequency range of the nonlinear measurement test-bench must be considered. For a given capacitance value, a capacitor can potentially appear as an RF open or an RF short depending on the frequency of the RF signal that is incident to the capacitor. The goal is to make sure the capacitor's behavior falls somewhere between the two extremes when performing the nonlinear characterization.

S-parameter simulations of several static capacitors are completed using Agilent's Advance Design System (ADS). The simulation schematic shown in Figure 4-2 is used to observe the reactance at 1GHz for a range of capacitance values (1 – 30pF). As shown in Figure 4-3, there is a significant change in the reactance at low frequencies when comparing the 1pF, 5pF, and 10pF capacitors. However, the reactance does not change much for the simulated capacitance values above 10pF. Additionally, the reactance is small for the larger values of simulated capacitance. This implies that the capacitors larger than 10pF will resemble an RF short at 1GHz which is not suitable for the nonlinear characterization of the BST varactors (more details in Chapter 7). Therefore, it was decided to aim for capacitance values in the range of 1 – 10pF.

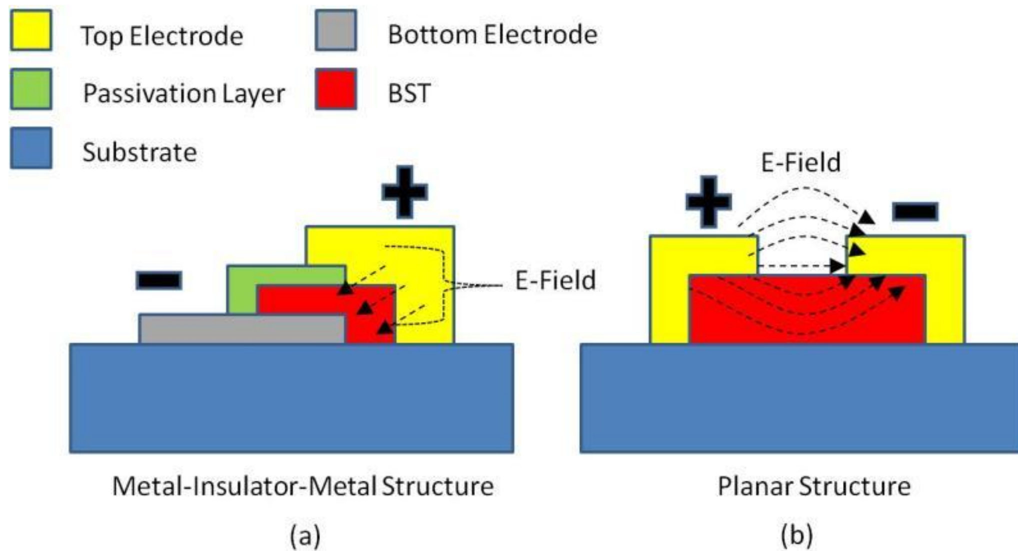


Figure 4-1: BST Varactor Structures
(a) MIM Structure (b) Planar Structure

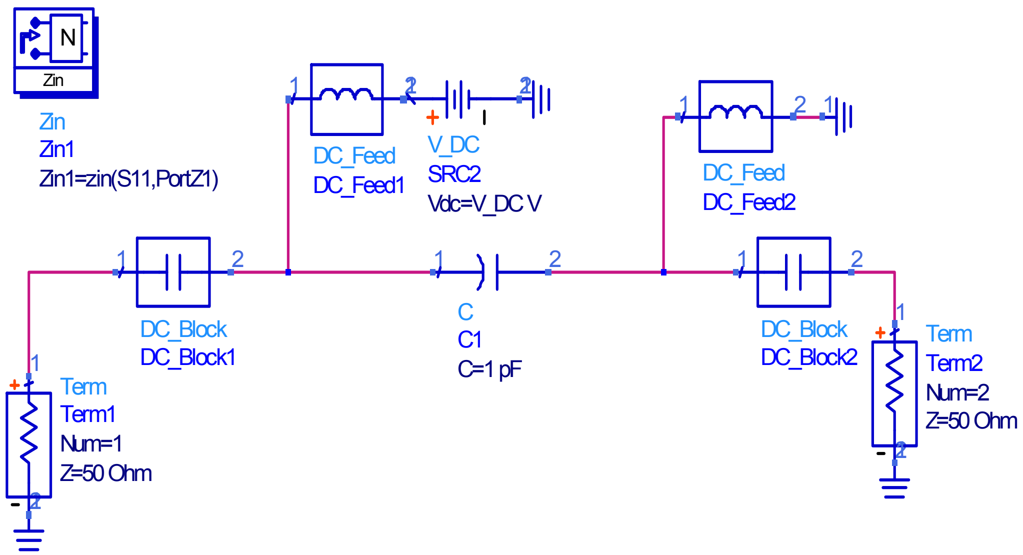


Figure 4-2: ADS Schematic for Static Capacitor Simulation

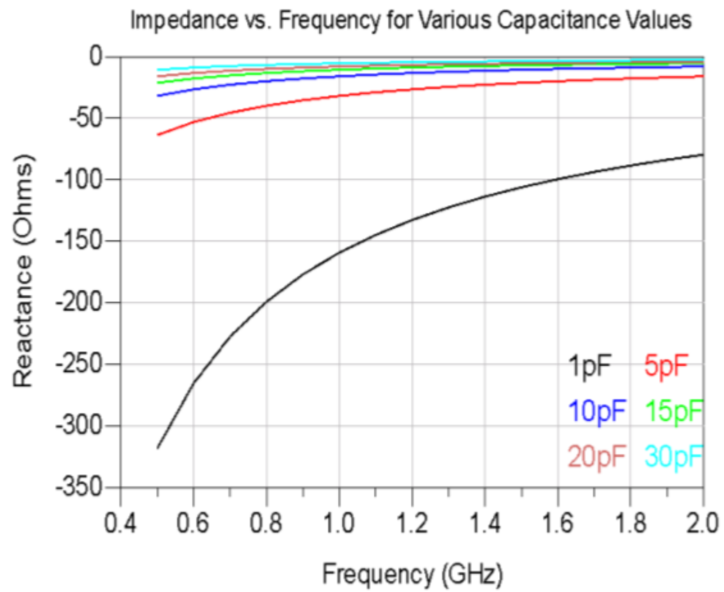


Figure 4-3: Impedance vs. Frequency for Various Capacitance Values

To design the photolithography mask for the conventional IDCs, simulations of various IDC geometries are performed using Ansoft's High Frequency Simulation Software (HFSS). Since the permittivity and loss tangent of the BST films used were unknown at the time, values for both are pulled from literature to run the simulations [82, 83]. Using a permittivity of 500 and loss tangent of 0.02 for the BST film, IDC geometries using 5µm gaps are simulated. This gap size is chosen because it is the smallest gap that can be obtained consistently using the tools available for conventional lithography. An IDC with 300nm of patterned BST beneath the fingers is simulated with 5 finger pairs using finger dimensions of 400µm long by 50µm wide. A schematic of this IDC is shown in Figure 4-4. The simulated capacitance of this device is 4.016pF, which is approximately in the middle of the capacitance range that was aimed for. To allow for deviations in the actual permittivity and the simulated permittivity and keep the measured capacitance within the desired range of 1pF – 10 pF, IDC designs with 3 finger pairs and 7 finger pairs are also included in the mask layout.

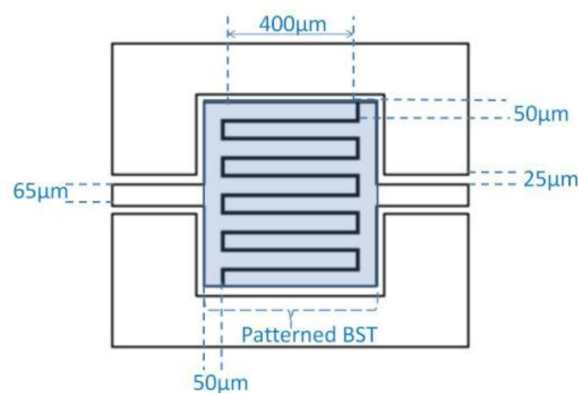


Figure 4-4: 5 Finger Pair BST IDC Design

4.4 Fabrication

4.4.1 Patterning BST

The first step in fabricating the interdigital capacitors is to pattern the BST film that was deposited on the alumina substrates. Initially, Shipley 1813 positive photoresist is used as a mask layer to prevent sections of the BST layer from being etched. The samples are submerged in 6:1 buffered oxide etchant (BOE) to pattern the BST. Although this method is adequate for etching non-annealed BST films, the BOE solution is not strong enough to etch the annealed BST films. Several variations of diluted hydrofluoric acid solutions (HF and water) along with diluted hydrochloric acid solutions are used in an attempt to etch the annealed BST films. These diluted solutions are strong enough to etch the annealed films; however, the solutions are so strong that they undercut the masking photoresist and etch the films laterally. This leaves BST patterns with damaged edges and pinholes after wet etching. The effects of diluted HF and diluted HCl are shown Figure 4-5.

Another option to obtain cleaner, non-damaged annealed BST patterns, is to use deep reactive ion etching (DRIE). DRIE provides an anisotropic etching method for patterning the BST; therefore, there is no need to worry about undercutting the mask layer while etching. The recipe used is more of a physical bombardment on the etched surface than a chemical reaction; so, the mask layer has to be thick enough to withstand the etching recipe until the BST film is completely etched down to the alumina substrate. Because of this, Shipley 1827 is used in place of 1813 when using DRIE to etch the annealed BST films. Once the films are etched, the remaining resist of the mask layer is stripped from the samples using oxygen plasma. More details of the recipe are given in Appendix B.

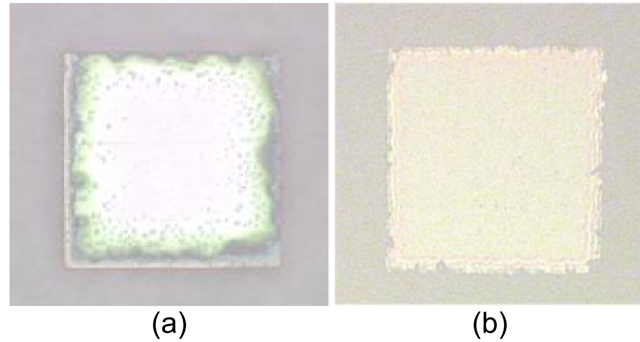


Figure 4-5: Damaged BST Films from Wet Etch
(a) Diluted HF (b) Diluted HCl

4.4.2 Electrodes for IDCs

The electrodes for the IDCs are fabricated on top of the BST patterns by using Futurexx 3000PY negative photoresist. After the resist is patterned, the metal is deposited by thermal evaporation, A metal thickness of 800nm is used. Initially, a metal stack consisting of Cr/Ag/Cr/Au (15nm/700nm/15nm/100nm) is considered because it is a cheaper alternative than using Cr/Au (15nm/800nm) only. The Denton DV-502A thermal evaporator used to deposit the metal is capable of housing two metal sources at a time. To put down the Cr/Ag/Cr/Au metal stack, the chamber has to be pumped down to a pressure of 2×10^{-6} Torr and Cr/Ag has to be deposited first. The chamber has to be vented to atmospheric pressure to open it and exchange the Ag source for the Au source. After pumping the thermal evaporator chamber back down, the Cr/Au layer is then deposited on top of the Cr/Ag layer. A lift-off is performed using Futurexx RR41 resist remover heated to 100°C, leaving the metal electrodes on top of the patterned BST.

After fabricating the first round of IDCs, they are tested for tunability by applying an external DC voltage. Upon applying a voltage in the range of 25V – 30V, burning is

noticed within the gaps of the IDCs as shown in Figure 4-6. At the time, it was unknown whether the burning was due to the BST film breaking down or due to faulty electrodes.

In an effort to isolate the cause of the burning effect with DC bias, IDCs are fabricated on bare alumina samples without BST using two different metal stacks. The initial metal stack of Cr/Ag/Cr/Au (15nm/700nm/15nm/100nm) is one of them. The second metal stack consists of Cr/Au (15nm/800nm). Both sets of metal are deposited by thermal evaporation. Unlike the deposition process for the Cr/Ag/Cr/Au metal stack, vacuum is never broken when depositing the Cr/Au metal stack. Current-voltage measurements are taken on both sets of electrodes by sweeping DC voltage from 0V – 100V across the gaps of the IDCs using DC probes. The IDCs consisting of the Cr/Ag/Cr/Au metal stack started to draw current once the DC voltage reached the range of 50-75 Volts. Figure 4-7 shows a typical I-V plot for the IDC electrodes with the Cr/Ag/Cr/Au metal. At low voltage levels, no measureable current is being pulled from the device; however, 10mA of current is drawn once the swept voltage reaches 60V. The electrodes using this metal stack also appear to burn with increasing DC voltage as displayed in Figure 4-8. Since the same burning phenomena is observed with and without the BST film while using the Cr/Ag/Cr/Au this metal stack, it is obvious that the burning effect is not being caused by any defects of the BST film.

The IDC electrodes that are fabricated using Cr/Au pull no measureable current throughout the entire range of swept voltage. The current versus voltage data is shown in Figure 4-9. There are no spikes or outliers observed in the data which implies that the amount of current being pulled or lack thereof is consistent throughout the duration of the DC testing. As shown in Figure 4-10, the Cr/Au electrodes sustain no visible damage with applied voltage up to 100V.

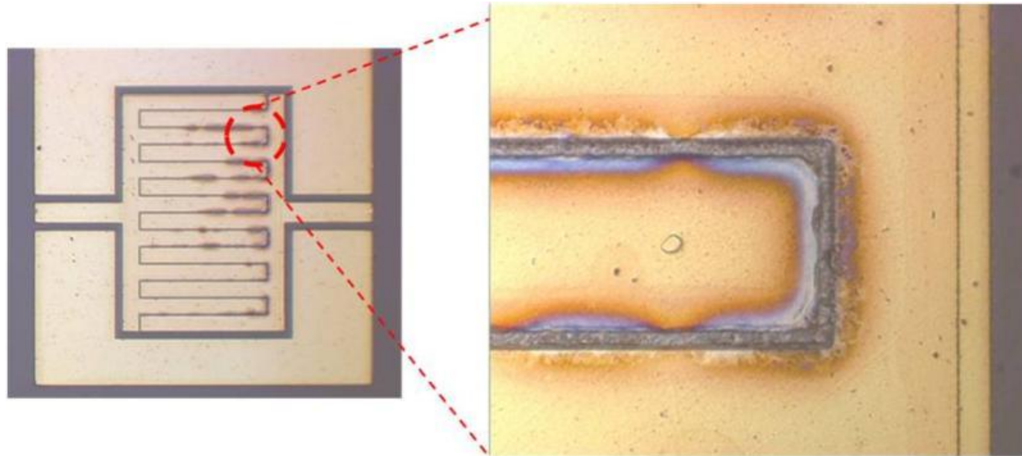


Figure 4-6: Burned BST IDCs with Cr/Ag/Cr/Au Metal Stack after Application of 25V

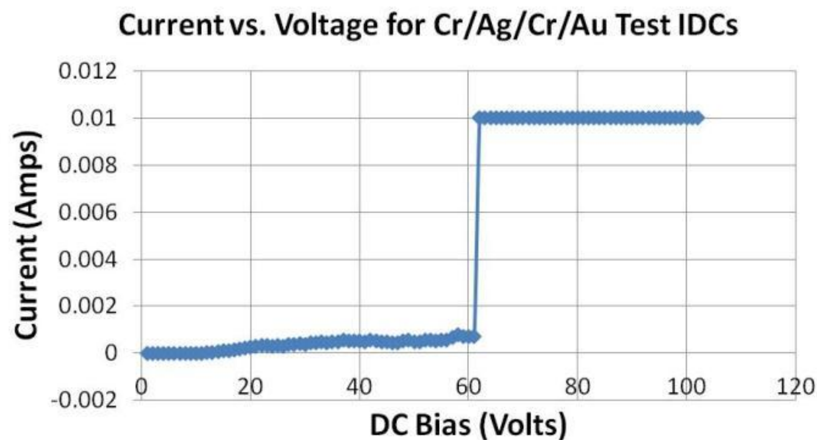


Figure 4-7: Current vs. Voltage for Cr/Ag/Cr/Au Electrodes

At this point, the Cr/Au metal stack becomes the material of choice for the IDC electrodes. It allows the for the BST film to be biased with a high externally applied electric field without suffering from physical defects which could cause discrepancies in the capacitance and tunability extraction. It remains unknown whether the burning of the Cr/Ag/Cr/Au electrodes is due to some faulty characteristic of the silver that is exploited with applied bias or if there is an issue with the overall quality of the metal stack because

vacuum has to be broken in the process of the deposition. The entire process flow for the fabrication of the IDCs using the Cr/Au metal stack for the electrodes is shown in Figure 4-11 with more details of the recipes listed in the Appendix B. Examples of the 3, 5, and 7 finger pair BST IDCs are shown Figure 4-12.

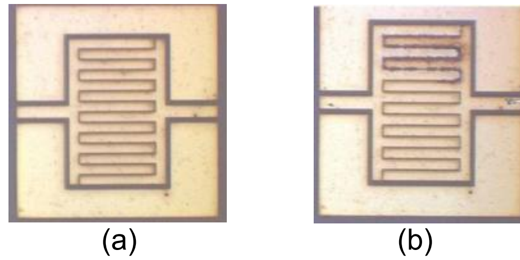


Figure 4-8: Cr/Ag/Ac/Au Electrodes
(a) Before Biasing (b) After Biasing

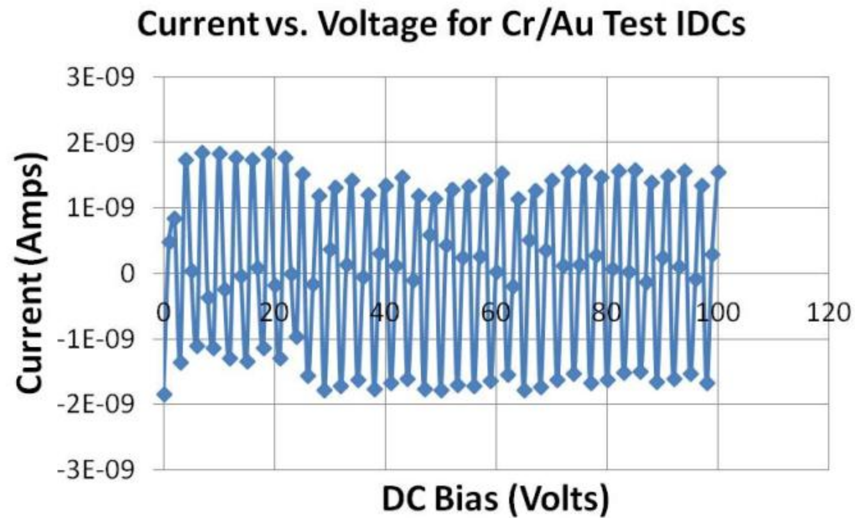


Figure 4-9: Current vs. Voltage for Cr/Au Electrodes

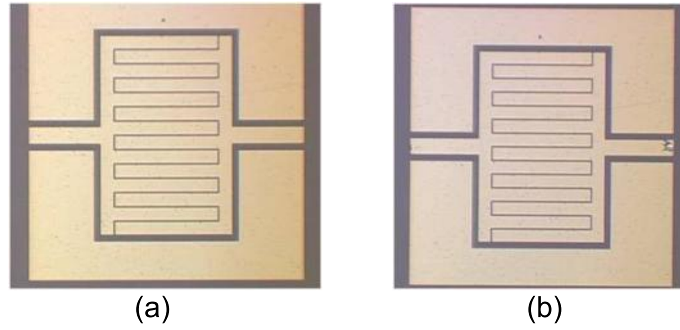


Figure 4-10: Cr/Au Electrodes
(a) Before Biasing (b) After Biasing

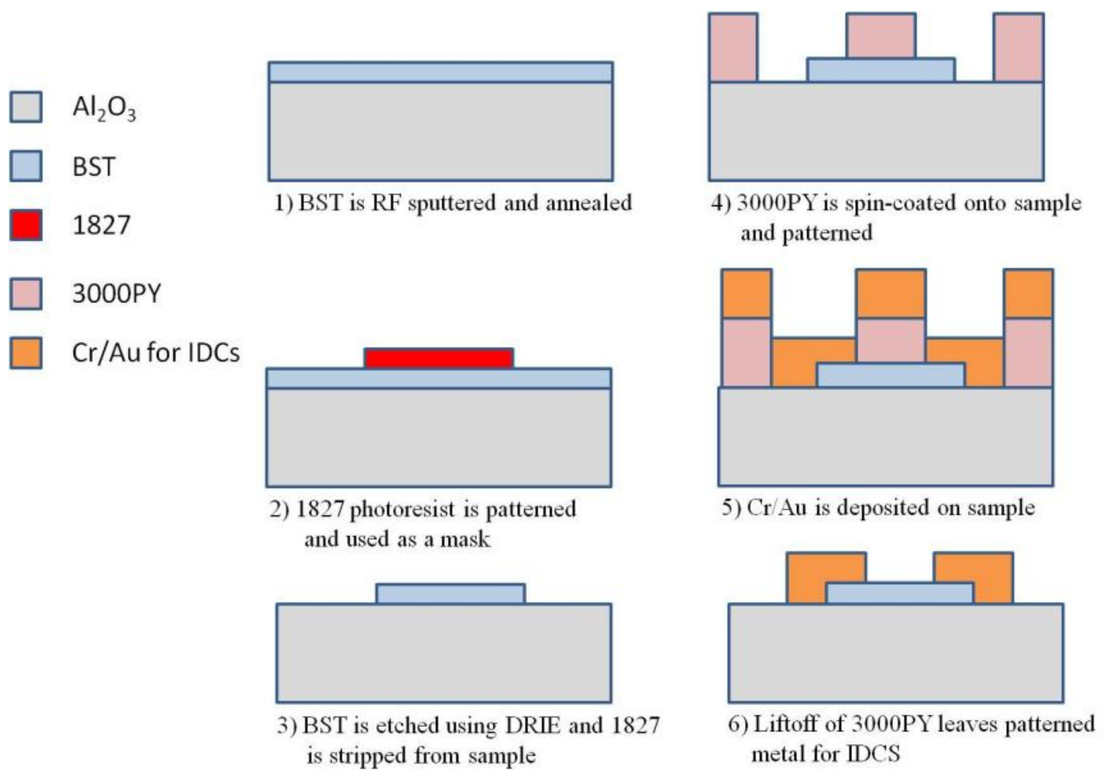


Figure 4-11: Microscale IDC Fabrication Process Flow Chart

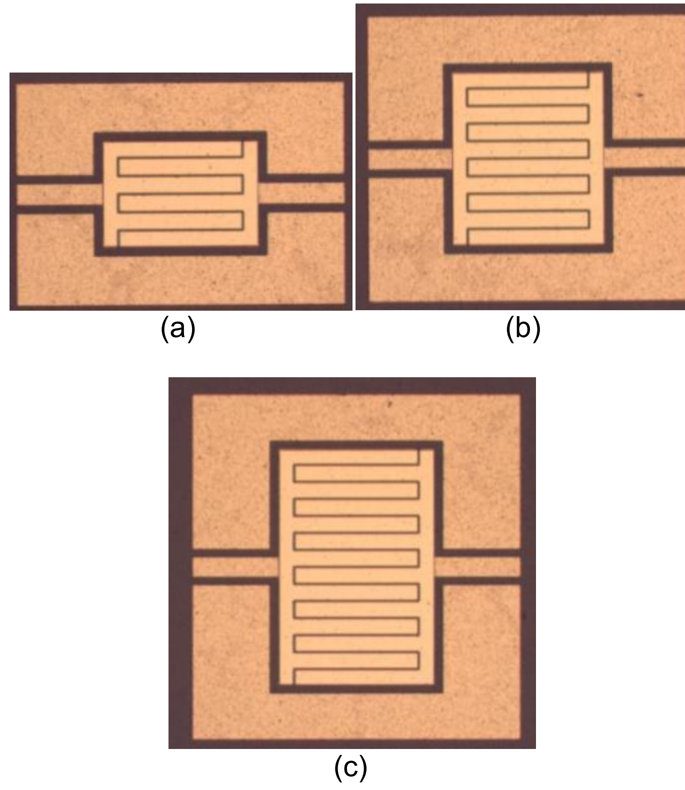


Figure 4-12: BST IDCs with 5µm Gaps
(a) 3 Finger Pairs (b) 5 Finger Pairs (c) 7 Finger Pairs

Chapter 5 Nanoscale IDCs by Electron Beam Lithography

5.1 Introduction

To further enhance tunability, the gap size of the planar structure varactors needs to be reduced to enhance the E-field confinement within the BST film. Additionally, making tunable nanoscale BST varactors will help to ease integration of tunable BST varactors into full nanoscale tunable receivers. Conventional photolithography using contact mask aligners similar to the one used for the work in the previous chapter limits the varactor gap sizes to the micrometer range. Electron beam lithography (EBL) is used to reduce the gap size down to the nanoscale. This chapter explains the procedures used to fabricate the nanoscale varactors used for this work.

5.2 Fabrication Process Flow

The overall concept of the nanoscale BST varactors is very similar to that of the microscale designs discussed in the previous chapter. The process flow chart is shown in Figure 5-1. The BST layer is patterned by DRIE etching using 1827 resist as a mask. ZEP, a positive EBL resist, is used for nanoscale lithography. A layer consisting of Cr/Au patterns for EBL alignment marks is fabricated using 3000PY litho and liftoff. The significance of this layer will be further discussed later in this chapter. To avoid charging effects that are encountered from the electron beam hitting the insulative alumina substrates, a conductive spin on polymer is spincoated on top of the ZEP resist. A comparison of writing patterns with and without E-spacer on alumina displayed in Figure 5-2 shows why the E-spacer is necessary for insulative substrates. After the patterns have been written with the electron beam, the E-spacer is removed by ultrasonication in

water. The ZEP resist is then developed using Xylenes. A thin metal layer of Cr/Au (15nm/125nm) is deposited followed by a liftoff in anisole, leaving electrodes with nanoscale gaps.

The areas of the resist that are exposed to the electron beam will be developed and rinsed away. Metal will be deposited in these exposed areas and a lift-off will be performed to leave the metal patterns. After the exposure and develop, there will be very thin traces of resist that will be used to create the nanoscale gaps in the varactors when the lift-off is performed. Therefore, it is important to make sure the resist is not being over-exposed by the electron beam when the nano-patterns are written. In an effort to reduce the possibility of devices being shorted, the electron beam current is reduced to write regions of the patterns that are close to the gaps. Instead of using 40nA, a 1nA beam current is used to write the outer 500nm areas of the electrode patterns. This is shown in

Figure 5-3 using an illustration of a line gap device.

5.3 Exposure Dose Tests

Dose tests are performed on bare silicon and alumina substrates as a part of the process development to derive the optimum exposure conditions for nanoscale features. It also allows one to determine the smallest achievable gap size for each structure type. An array of different patterns featuring various gap sizes is written repeatedly at various doses to see which dose yields the best results consistently. The dose test matrix consists of tapered series gap, line gap, and interdigitated structures as shown in Figure 5-4. The design gap dimension for each structure is shown in Table 5-1.

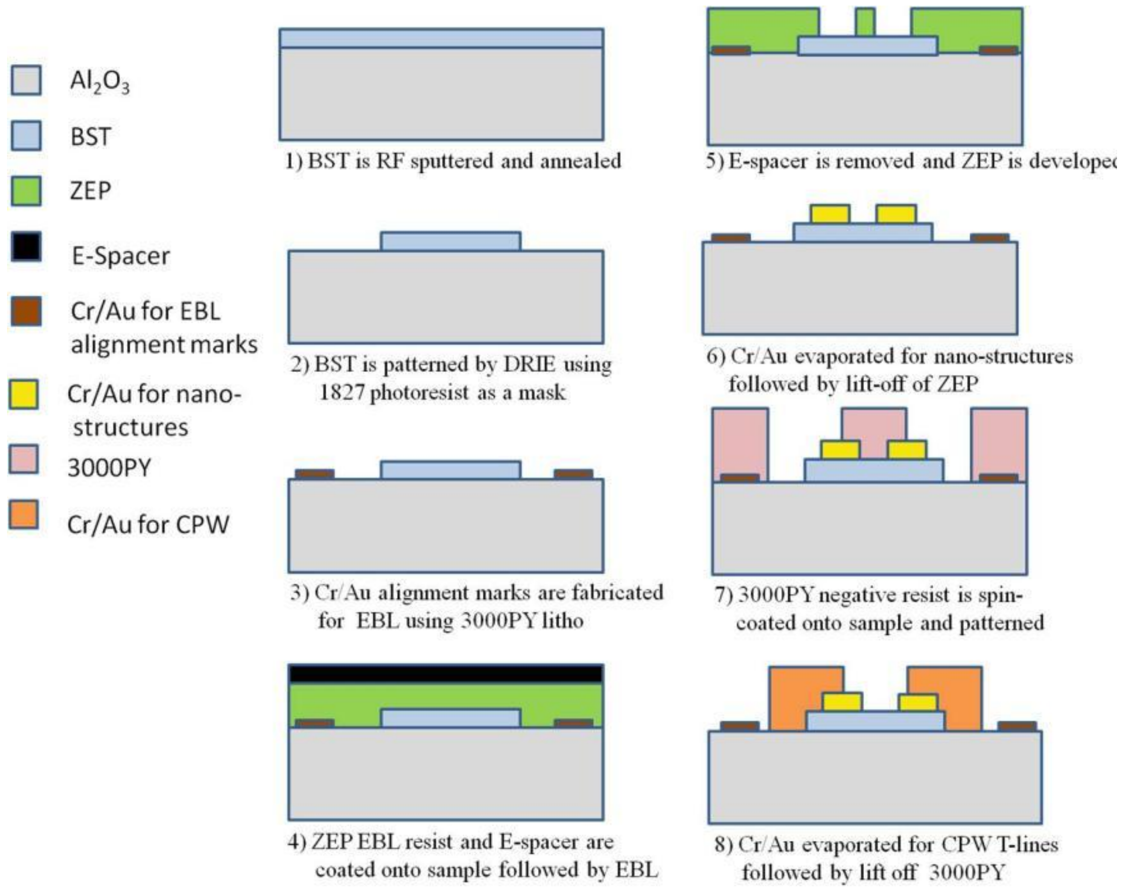


Figure 5-1: EBL Process Flow

After writing several arrays using doses in the range of 100 – 180 mJ/cm^2, 160 mJ/cm^2 proves to be the optimum dose value to use. Most of the features written using doses of 170 and 180 mJ/cm^2 are shorted after performing the liftoff. Also, it is observed that structures with the 25nm tapered gap design along with the 100nm line gap design are consistently shorted no matter what dose value is used. Therefore, the minimum design gaps used are 50nm, 150nm, and 200nm for the tapered gap, line gap, and IDC structures respectively.

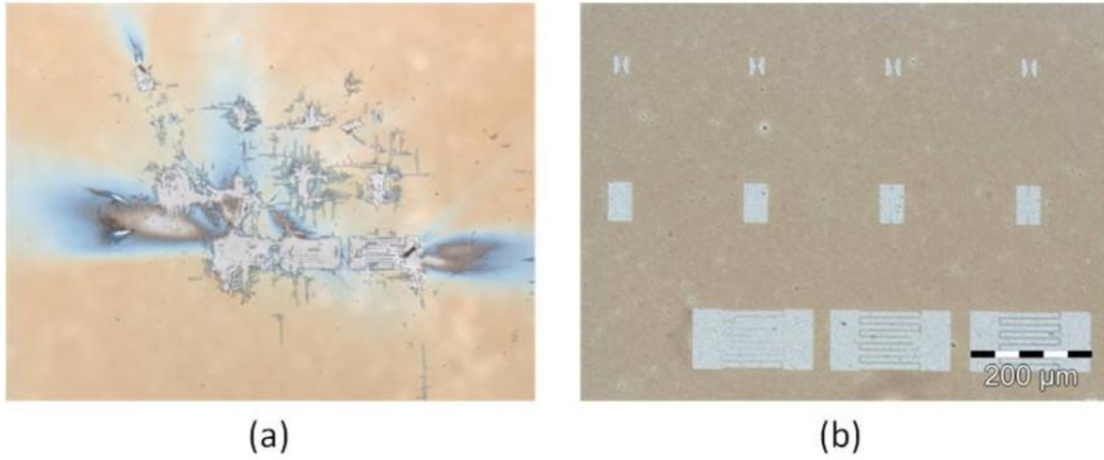


Figure 5-2: Impact of E-spacer
(a) Without E-spacer (b) With E-spacer

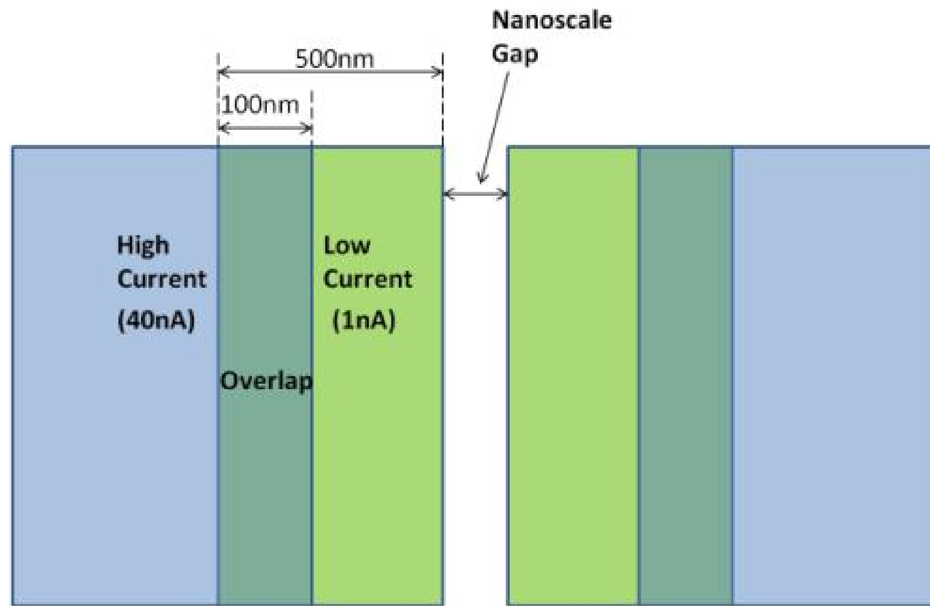


Figure 5-3: Overlap of High and Low Current Patterns

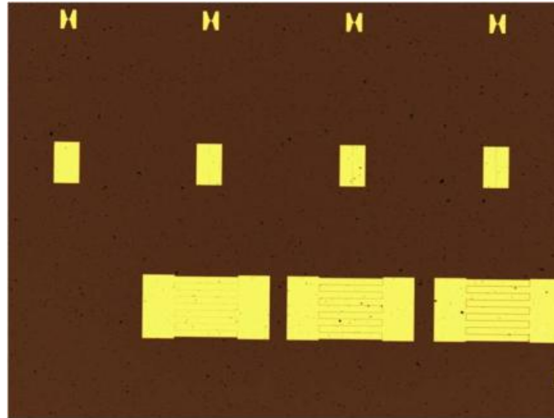


Figure 5-4: Dose Test Layout

Table 5-1: Dose Test Array Dimensions

Tapered Gap	25nm	50nm	100nm	200nm
Line Gap	100nm	150nm	200nm	250nm
IDC		200nm	300nm	400nm

5.4 EBL Alignment

The EBL portion of this work is done at the Center for Nanoscale Materials (CNM) within Argonne National Laboratory using the JEOL JBX-9300FS EBL system, shown in Figure 5-5. The system is equipped with a semi-automatic alignment tool that can be used to write the nanoscale features so that they are properly aligned to previous fabrication layer in the design; the BST layer in this case. In order to use this feature, alignment marks are included in the design of the BST mask layer so that the EBL system could use them as a point of reference when determining where to write the nano-patterns.

A total of at least four alignment marks are necessary to use the alignment feature of the JEOL EBL system. The local CAD design coordinates for the center of each

selected alignment mark to be used must be known. Additionally, the corresponding global coordinates of the stage position within the main chamber of the EBL system must be known for each alignment mark used. If the samples are loaded into the EBL system without the user's knowledge of the global coordinates of the alignment marks, the user would have to turn on the SEM and blindly drive the stage around to find the marks. The problem with this is that the SEM will expose all of the ZEP resist within the viewing window as the user tries to locate the marks, which would potentially yield a lot of shorted devices by the time the entire process flow is completed.

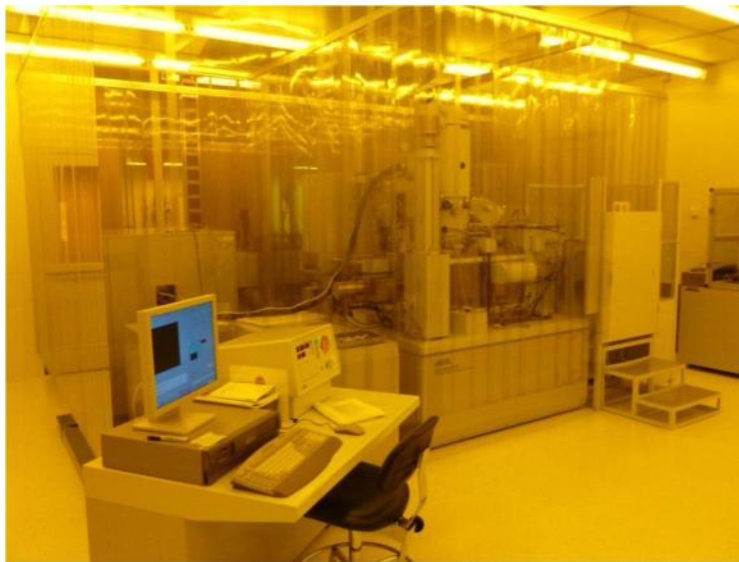
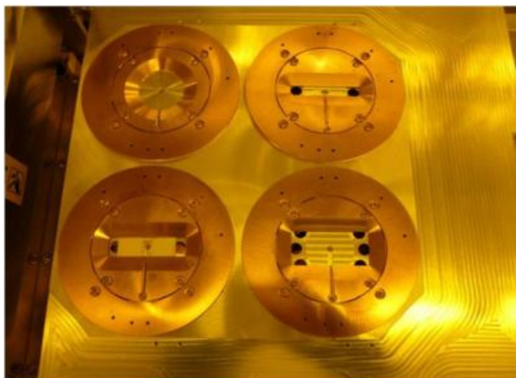


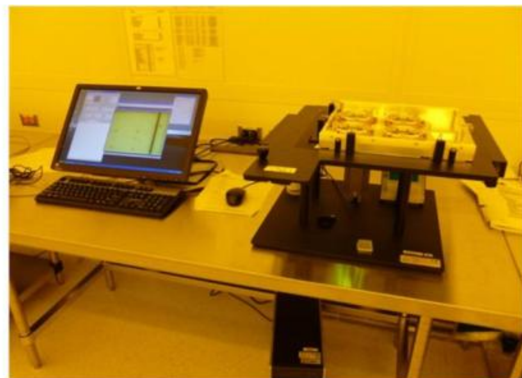
Figure 5-5: JEOL JBX-9300FS EBL System

To avoid the aforementioned issues, the Pre-Alignment Microscope System (PAMS) Metrology Tool is used to get a rough estimation of the global stage coordinates for the alignment marks. Once the samples are prepared with ZEP and E-spacer, they are mounted on the JEOL cassette. The JEOL cassette is loaded onto the PAMS tool which

consists of an inverted microscope and a mock stage of the JEOL EBL system. Both the cassette and the PAMS tool are shown below in Figure 5-6. The mock stage is connected to a PC with PAMS software that displays the global coordinates of the mock stage. Using the microscope, the user can position the mock stage so that the targeted alignment marks appear in a cross hair on the monitor and the global stage coordinates can be observed. Once the global stage coordinates are obtained from the mock stage, the cassette is loaded into the JEOL EBL system. The known global coordinates can be entered into the JEOL EBL system so that the stage is driven to the exact coordinates of the targeted alignment marks. The SEM is then turned on to verify that the alignment marks are in the near vicinity of the coordinates that are entered.



(a)



(b)

Figure 5-6: JEOL Accessories
(a) Cassette (b) PAMS Metrology Tool

The previously mentioned alignment procedures are initially attempted using alignment marks that were patterned in the BST layer from the DRIE process. However, when trying to use the semi-automatic alignment tool of the JEOL EBL system, the BST alignment marks do not provide enough back scattered electrons for the alignment tool to detect the marks. Therefore another mask layer has to be introduced to the process

to put down a layer of Cr/Au for the EBL alignment marks on top of the existing BST alignment marks. The metal provides enough back scattered electrons so that the alignment marks can be detected by the semi-automatic alignment tool of the JEOL.

Caution must be exercised when choosing the target alignment marks for the semi-automatic alignment tool. If the chosen alignment marks suffer from a bad lift-off and have flags or adhesion issues with the surface, there is a possibility that the alignment tool within the JEOL will not recognize the alignment marks properly or not recognize them at all. Figure 5-7 shows examples of good and bad alignment marks. If bad alignment marks are used for the semi-automatic alignment tool of the EBL system, the nanoscale EBL patterns can be misaligned, stretched, and/or compressed with respect to the BST layer resulting in devices like the one shown in Figure 5-8. If the IDC electrodes are not fabricated on top of the patterned BST, the measured capacitance of the device along with its tunability will be reduced. If the alignment marks do not have any major flaws then the devices will come out as they are designed with the entire meandered gap of the IDC being on top of the patterned BST such as the one displayed in Figure 5-9.

A variety of designs are used for the nanoscale IDCs so that a wide range of 0V bias capacitance values could be obtained for RF experimental purposes. The device shown in Figure 5-9 has 3 finger pairs, and the IDC fingers are 65μm long and 10μm wide. The gap spacing in this case is designed for 500nm, but it is measured to be approximately 365nm after the lift-off was performed. A second IDC design is used consisting of 10 finger pairs with dimensions of 200μm x 10μm with similar gap dimensions.

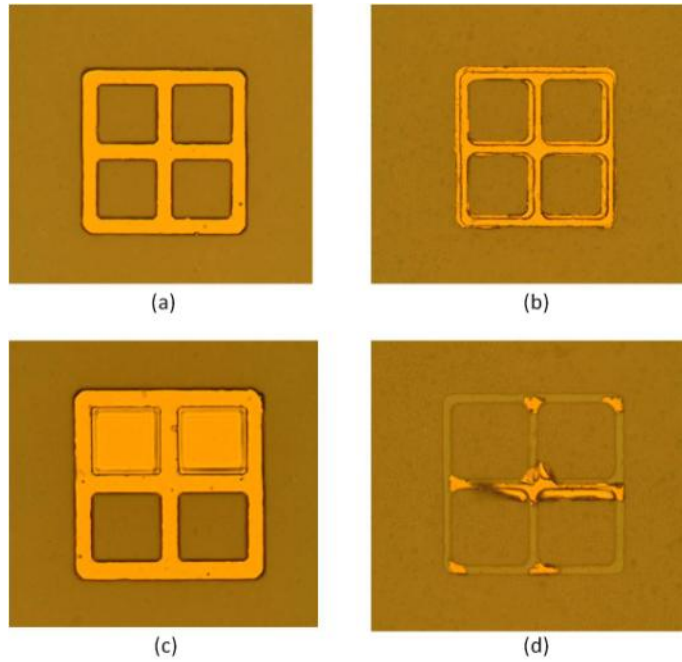


Figure 5-7: Alignment Marks
(a) Good Mark on Alumina (b) Good Mark on Patterned BST (c) Bad Mark from Incomplete Liftoff (d) Bad Mark on Patterned BST due to Metal Adhesion Issues

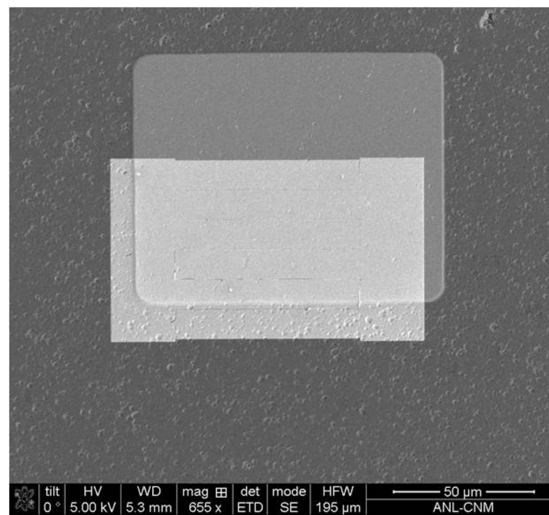


Figure 5-8: Misaligned IDC from Flawed Alignment Marks

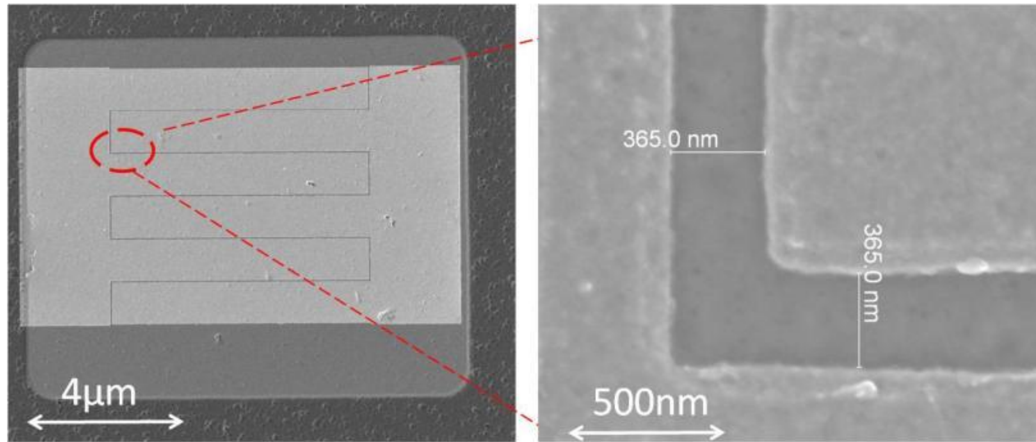


Figure 5-9: IDC with Nanoscale Gap Size

5.5 CPW Transmission Lines

In order to perform RF measurements on the nanoscale varactors, coplanar waveguide transmission lines have to be fabricated such that they overlap and make contact with the nanoscale features for probing. This is done by patterning Futurex 3000PY negative photoresist on top of the nanoscale electrodes followed by a Cr/Au deposition of 15nm and 800nm respectively using thermal evaporation. A lift-off is then performed using Futurex RR41 resist remover. An example of a completed structure is shown in Figure 5-10 in which the signal line of the CPW transmission line overlaps the nano-structures that were fabricated by EBL.

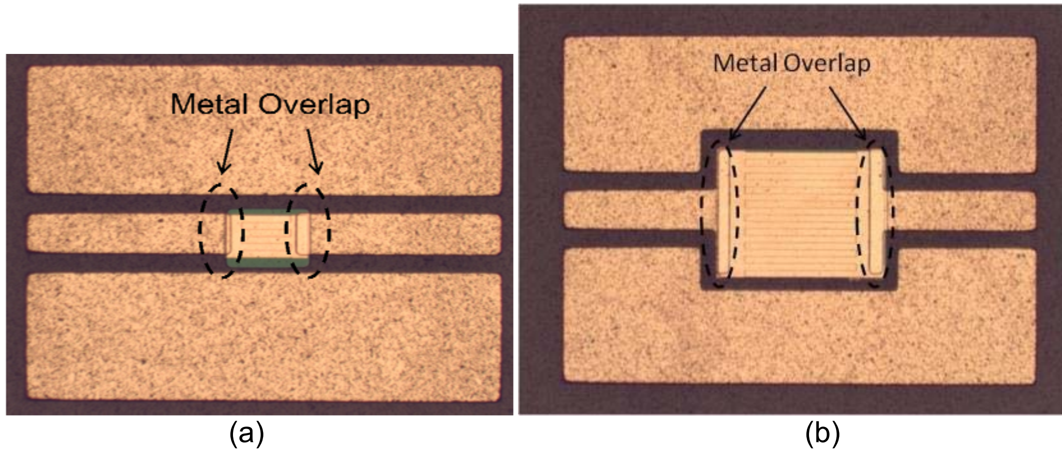


Figure 5-10: CPW Transmission Lines Overlapping Nanoscale IDCs
(a) 65μm long fingers (b) 200μm long fingers

Chapter 6 Small Signal RF Measurements & Analysis

6.1 Introduction

Small RF signal characterization is performed on the fabricated BST varactors using Scattering (S) parameter measurements. The S-parameter data is used to observe the overall behavior of the devices with respect to frequency. Additionally, the data is used to extract the capacitance and tunability of the varactors. This chapter explains the procedures of how the S-parameter data is collected and analyzed for the microscale and nanoscale devices used in this work. Temperature and substrate dependent tunability is also discussed.

6.2 S-Parameter Measurements

S-parameters are used to characterize the frequency dependent behavior of RF networks [84-87]. A voltage wave is inserted into one port of the device under test (DUT). It scatters through the DUT and the output voltage wave is measured at all ports of the DUT including the insertion port. This process is repeated using each port of the DUT as an insertion port while measuring the output at the remaining ports. The measured S-parameter data is presented as ratios of the input and output voltage waves at the various ports. For example, parameter S_{ij} corresponds to the ratio of the voltage signal coming out of port i to the incident voltage signal at port j [88]. Investigating these parameters can result in useful information on the RF behavior of the DUT. For this work in particular, the measured S-parameter data will be used to model the BST varactors and extract the capacitance along with tunability. Therefore, it is imperative that the S-parameter data is obtained as accurately as possible.

When obtaining S-parameter data, the losses of all of the components within the measurement test bench (cables, probes, adapters, etc.) must be taken into account to avoid collecting false data for the DUT. A custom set of on wafer CPW standards are designed using ADS LineCalc to perform a thru-reflect-line (TRL) calibration. The TRL calibration method is primarily used for non-coaxial test settings such as waveguides, using test fixtures, or on-wafer measurements [89]. It is a popular technique because it allows the reference planes for the S-parameter measurements to be extended beyond the tips of the probes and interconnects used to contact the DUT [90, 91]. The TRL calibration standards consist of a thru, two opens, and three delay lines which theoretically span a frequency range of 0.7 – 147GHz (shown in Table 6-1). The standards are designed for a characteristic impedance of 50 Ohms using a signal line width of 65μm and a gap of 25μm between the signal line and the ground lines. When the TRL calibration is properly completed, the reference planes of the S-parameter measurements will be at the center of the thru [92]. The thru for this set of standards is designed to be 500μm long. Therefore, the CPW interconnects leading to the interdigitated fingers of the BST varactors are designed to be 250μm or half the length of the thru calibration standard. The shifted reference planes are illustrated in Figure 6-1.

Table 6-1: TRL Delay Lines

Lines	20 deg	90 deg	160 deg
Delay 1 (11.5mm)	0.7 GHz	3.25 GHz	5.75 GHz
Delay 2 (3mm)	3.25 GHz	19 GHz	25.3 GHz
Delay 3 (0.93mm)	19 GHz	82.5 GHz	147 GHz

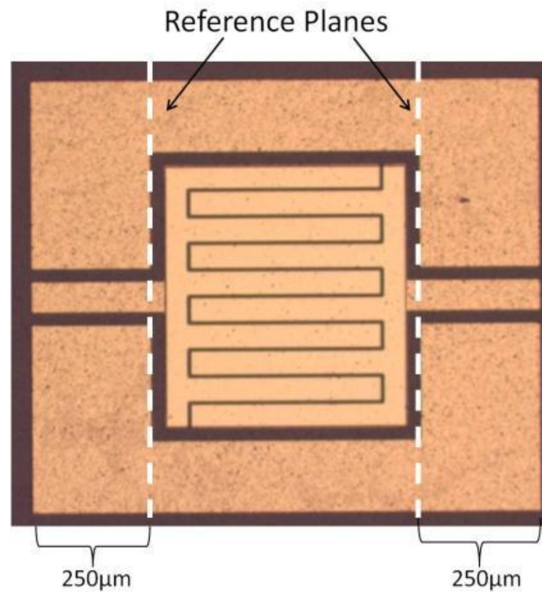


Figure 6-1: Reference Planes After TRL Calibration

MultiCal software by the National Institute of Standards and Technology (NIST) is used to collect the raw S-parameter data from the TRL standards and complete the calibration. The quality of the calibration is verified by measuring the thru and open calibration standards. For a good calibration, the log magnitude of S21 of the thru should be 0dB +/- 0.05dB and S11 of the opens should be 0dB +/- 0.05dB for the entire frequency range of interest. Once the calibration is confirmed to be good, the BST varactors are measured.

Using an Anritsu 37397C vector network analyzer and a Cascade Micro-Chamber probe station with a temperature controlled chuck shown in Figure 6-2, S-parameter data of the on-wafer IDCs is collected at varied bias voltages. This set of measurements is done at room temperature. GGB ground-signal-ground (GSG) probes with a 150µm pitch are used to contact the devices. Picosecond Pulse Lab bias tees are used to apply a DC voltage across the gaps of the planar varactors through the signal line tips of the

GSG probes. The data was acquired using Maury Microwave Automated Tuner System (ATS) 400 Software to control the set-point of the DC power supply and to collect data from the VNA.

Figure 6-2: Alumina Sample on Temperature Controlled Chuck

6.3 Microscale IDCs (MgO vs. Alumina)

Before fabricating and testing nanoscale devices, IDCs with microscale gap sizes are tested first. Although alumina is the primary substrate of choice for this work, IDCs are fabricated on both MgO and alumina substrates for the first round of devices. For the case of comparing tunability on the two different substrates only BST films that have been annealed for 12 hours are used. Figure 6-4, Figure 6-5, and Figure 6-6 show the S21 response for the 3 finger pair, 5 finger pair, and 7 finger pair IDCs, respectively. Data is shown for various applied DC voltages ranging from 0 – 90 Volts. Although data is collected for frequencies up to 65 GHz, a reduced frequency range is used for each plot to illustrate tunability. The log magnitude of S21 decreases as the applied voltage increases for the illustrated frequency range. This behavior is caused by an increase in the impedance of the devices with DC voltage which corresponds to the permittivity of the BST films decreasing with applied electric field.

Agilent's Advanced Design System (ADS) is used to convert the measured S-parameter data into Y-parameters. The Pi-network model displayed in Figure 6-3 is then used to extract the series capacitance of the IDCs. The series component labeled as $-Y_{12}$ represents the series admittance of the device corresponding to the 5 um gaps between the fingers. The shunt components of the model represent the admittance that occurs between the outermost fingers of the IDC and the surrounding ground planes of the CPW transmission lines. Equation 6-1 is used to extract the capacitance from the Y-parameters.

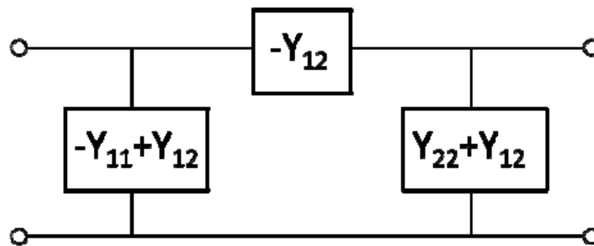
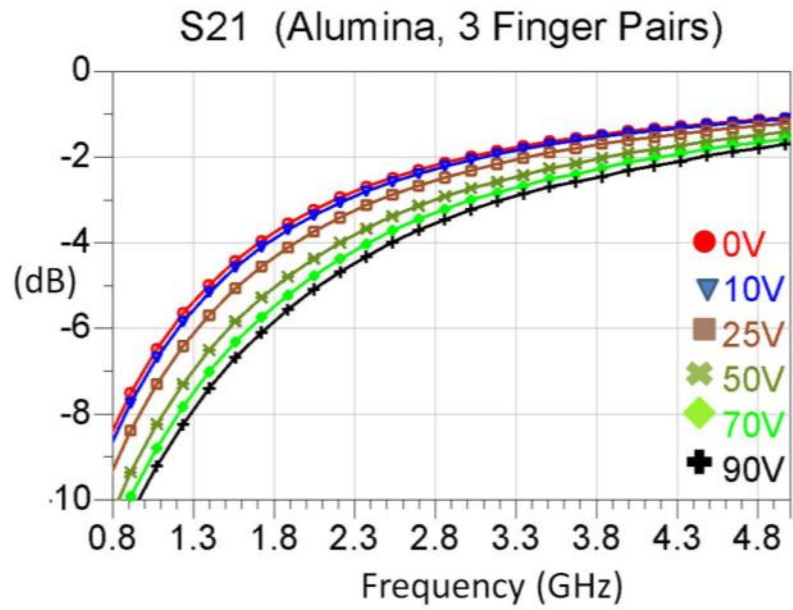


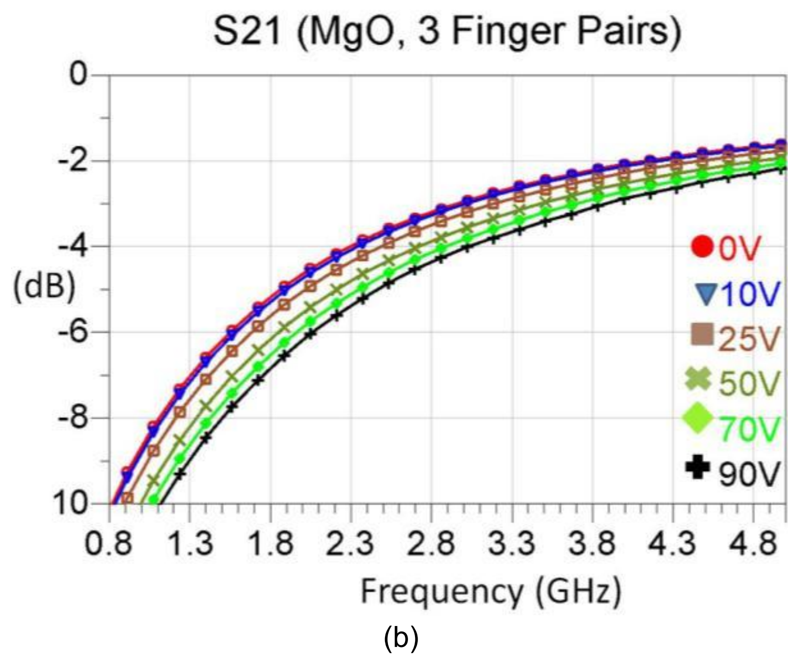
Figure 6-3: Pi Network Model for Capacitance Extraction

$$C = \frac{-imag(Y_{1,2})}{2\pi f} \quad \text{Equation 6-1}$$

Figure 6-7 shows the extracted series capacitance as a function of frequency for each of the three IDC geometries with an applied DC voltage of 0 Volts. There is an increase in capacitance with increasing frequency due to the behavior of the devices approaching a point of resonance. The more finger pairs a device has, the larger its series capacitance will be. If the devices are viewed as microwave resonators, the

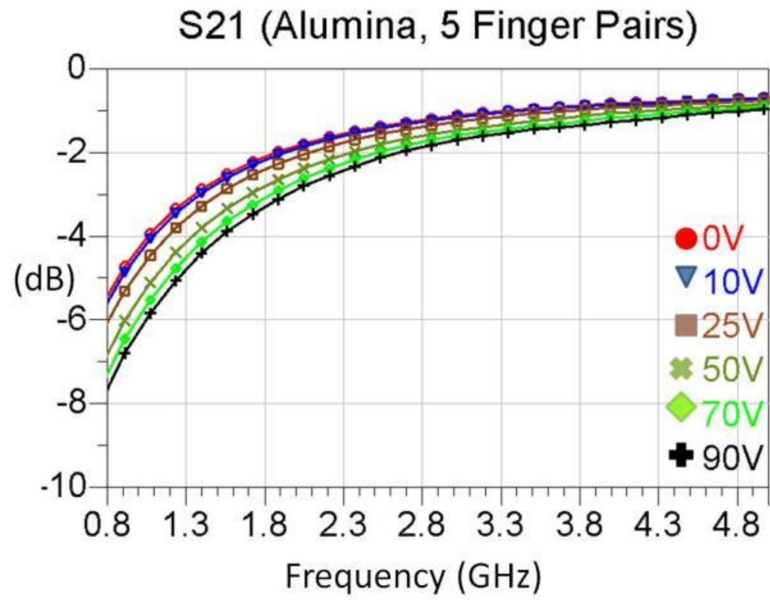


(a)

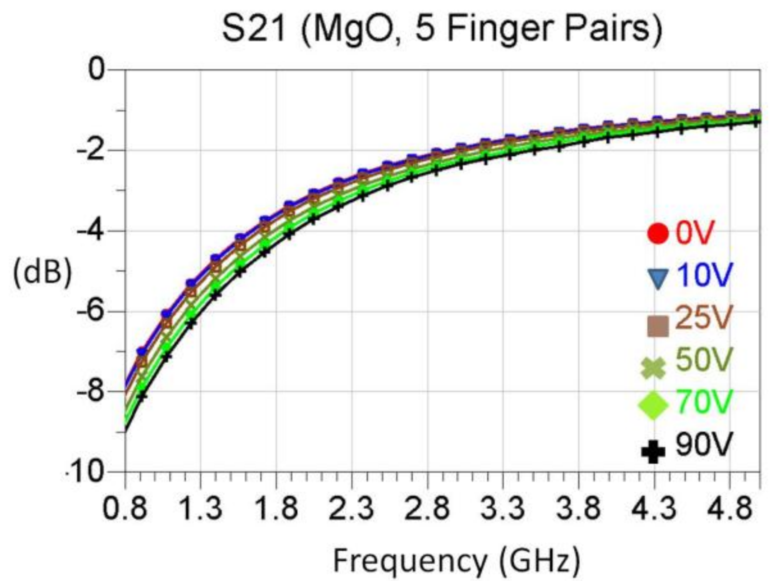


(b)

Figure 6-4: S21 Response of 3 Finger Pair IDCs
(a) Alumina (b) MgO

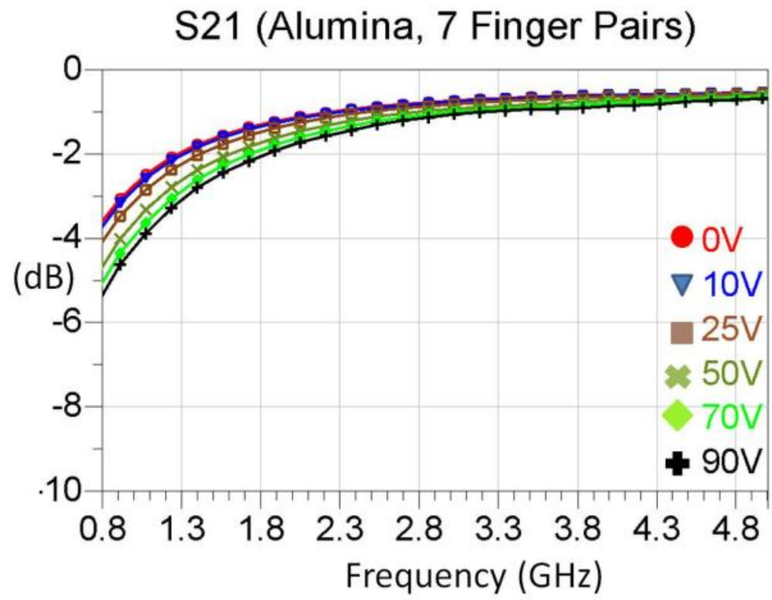


(a)

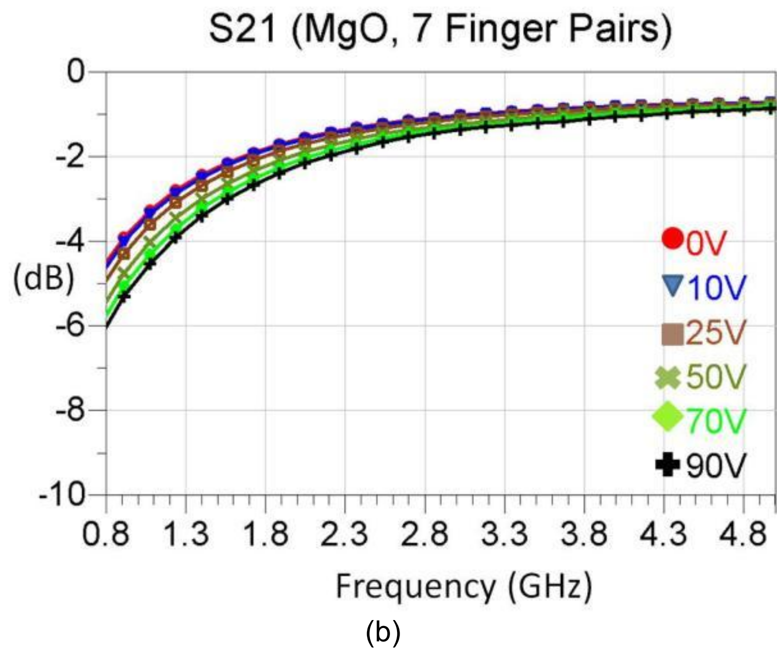


(b)

Figure 6-5: S21 Response of 5 Finger Pair IDCs
(a) Alumina (b) MgO



(a)



(b)

Figure 6-6: S21 Response of 7 Finger Pair IDCs
(a) Alumina (b) MgO

increased capacitance will lead to a decrease in resonant frequency according to Equation 6-2.

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Equation 6-2

Capacitance versus voltage (C-V) for each device type is shown in using a frequency of 1 GHz. This relatively low frequency is used so that the C-V curves and calculated tunability would not be skewed by the device resonance points. It is also close to the fundamental tone frequency that is used for nonlinear characterization which is discussed in Section IV. The C-V curves confirm that the IDCs fabricated on alumina have higher capacitance and tunability than those on MgO substrates. The tunability (τ) for each device is calculated at voltage (x) by using the expression

$$\tau(x) = \frac{C(V_{DC}=0) - C(V_{DC}=x)}{C(V_{DC}=0)} \times 100\%$$

Equation 6-3

where V_{DC} represents the DC voltage being applied.

Table 6-2 shows the 0 Volts bias capacitance for each type of device along with the calculated tunability at 50 Volts (100 kV/cm across the gaps) and 90 Volts (180 kV/cm). The capacitance and tunability for the 5 finger device on MgO both appear to be outliers. The data for this device is displayed for consistency as it was the only one of its type that did not burn with an applied voltage of 90 Volts. The highest tunability observed at 90 Volts (equating to 180 kV/cm using a 5μm gap) for an IDC on alumina was 33.8% and 25.8% on MgO. Previous studies have shown tunability of 33% on alumina at lower DC voltages (116 kV/cm) and up to 65% on MgO [57, 93]. Although the tunability reported

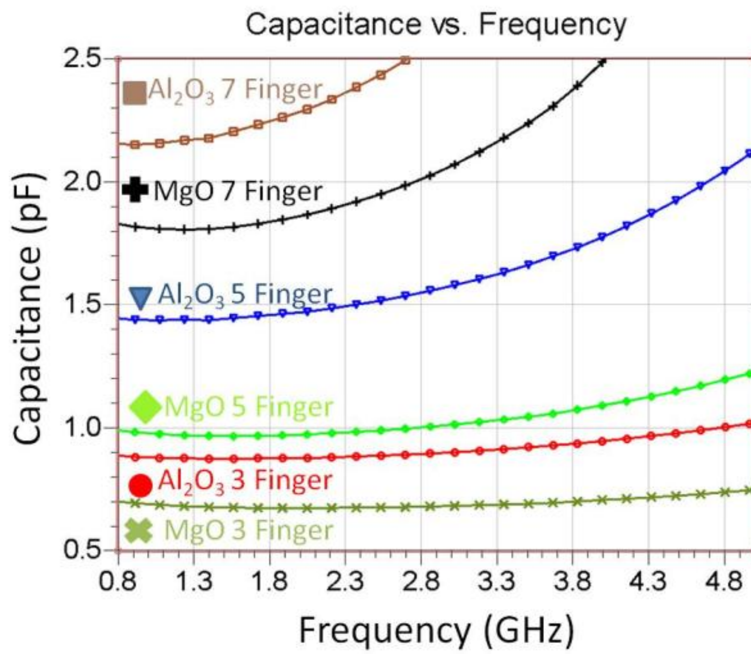


Figure 6-7: Capacitance vs. Frequency for all Microscale IDCs at 0 Volts Bias

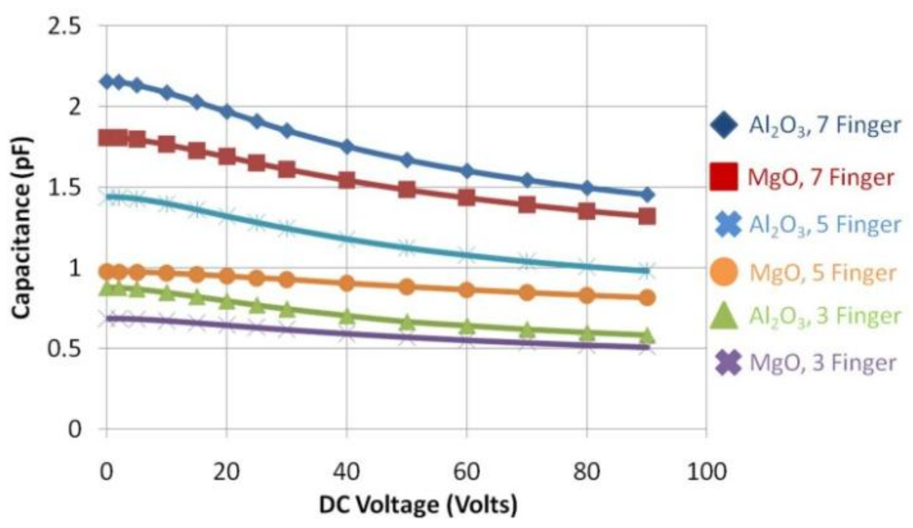


Figure 6-8: Capacitance vs. Voltage for all Microscale IDCs at 1 GHz

here is less than that reported previously, it is still enough for nonlinear characterization. After determining that the tunability obtained using polycrystalline alumina substrates was higher than that obtained from single crystalline MgO, it was decided to use the alumina for further device fabrication and RF characterization since it was the cheaper option.

Table 6-2: Tunability on Alumina vs. MgO

Finger Pairs	Capacitance at 0 V		Tunability at 50V (100 kV/cm)		Tunability at 90V (180 kV/cm)	
	Al_2O_3	*MgO*	*Al_2O_3*	*MgO*	*Al_2O_3*	*MgO*
3	0.878	0.686	24.3%	16.7%	33.8%	25.8%
5	1.438	0.9745	22%	9.5%	31.9%	16.5%
7	2.157	1.808	22.6%	17.9%	32.5%	27%

6.4 S-par Measurements on Alumina (varied Temperature)

An understanding of how temperature affects the tunability of BST varactors is beneficial when designing BST based RF circuits. This information is particularly useful for applications in which the devices are used in various types of climates. More S-parameter measurements are taken on the planar BST varactors fabricated on alumina to further investigate the impact of temperature on the device tunability. For this set of measurements, only the 5-finger pair IDCs are used.

S-parameter data of the on-wafer IDCs is collected at various bias voltages; however, the temperature of the chuck was varied from 25° C to 125° C in 25° increments for these measurements. A thru-reflect-line (TRL) calibration is again performed using standards that were fabricated on an alumina substrate. For this set of measurements, both forward and reverse bias DC voltages ranging from -90 to 90V are applied to the varactors.

Once the S-parameter data is collected, the effective series capacitance is again extracted at 1 GHz for each experimental voltage and temperature using similar methods discussed earlier in the previous section. Figure 6-9 shows the capacitance vs. voltage (C-V) behavior of the measured IDCs. The overall capacitance of the devices decreases as the chuck temperature is raised. Theoretically, as long as the BST film is operating in the paraelectric phase, the permittivity is expected to decrease with increasing temperature [9, 94]. The symmetry of the C-V curves in Figure 6-9 confirms that the BST film is operating in the paraelectric phase at room temperature (25°C) and above. The decrease in permittivity with increasing temperature is verified for the measured data using HFSS simulations to extract the film permittivity for each experimental temperature. The results are displayed in Table 6-3. From observing the compression of the C-V curves with increased temperature, it appears that temperature has its greatest impact on the permittivity when there is no DC bias applied to the devices.

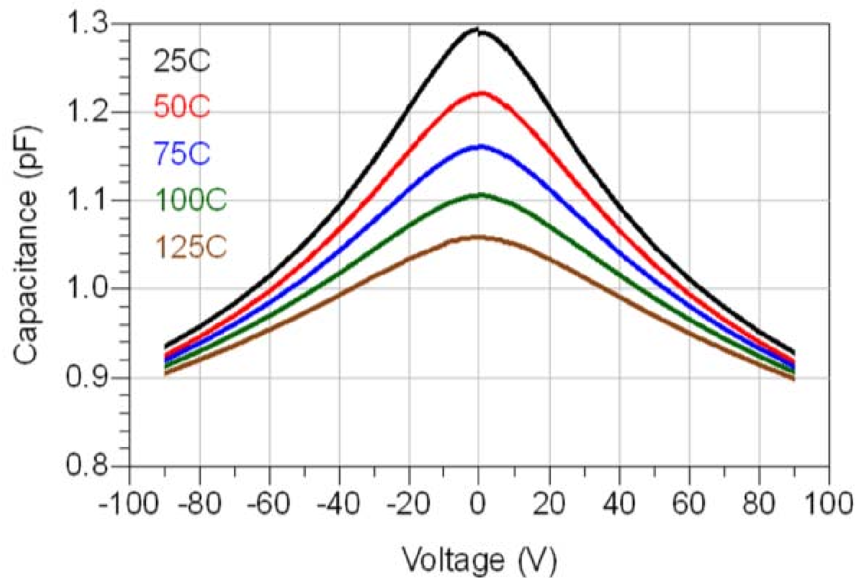


Figure 6-9: Capacitance vs. Voltage at Various Temperatures

Table 6-3: Extracted Permittivity vs. Temperature

Temperature (°C)	Relative Permittivity
25	300
50	275
75	260
100	245
125	225

6.5 Tunability vs. Annealing Time

S-parameter measurements are taken on IDCs fabricated with BST films that are annealed for different times. This is done to observe the impact that the material properties of the film have on the tunability of the IDCs. Only the 5-finger pair IDC design is used for this work. The capacitance and tunability are extracted using similar methods discussed earlier.

Figure 6-10 shows capacitance vs. voltage plots for IDCs fabricated with BST films annealed for 0, 3, 12, 18, and 24 hours. The CV trace representing the IDCs with non-annealed BST films is relatively flat which implies that there is little or no tunability. The zero-bias capacitance is just above 0.5pF. According to the TEM data previously presented, the non-annealed BST films contain no grains or signs of atomic alignment which is important for obtaining tunable films. As the films are annealed, the IDCs display a higher zero-bias capacitance along with increased tunability due to the formation of grains within the film. The three hour annealed films produce IDCs with an average zero-bias capacitance of about 0.9pF. For anneal times of 18 and 24 hours, there is very little difference in the zero-bias capacitance which is just above 1pF for each of the annealing conditions. The largest change in the zero-bias capacitance is

observed between the IDCs with the non-annealed films and those with films annealed for 3 hours. This corresponds to the largest change in the film roughness and grain size occurring between the non-annealed films and those annealed for 3 hours.

The tunability is extracted at 90V and shown with respect to the annealing time in Figure 6-11. The largest change in tunability is observed between the non-annealed films and those annealed for 3 hours which corresponds to the largest change in grain size occurring for the same anneal time increments. An increase in tunability is observed between the 12 hour and 18 hour annealing times, but there is not much difference in tunability for the 18 hour and 24 hour annealed samples. Overall, the tunability increases with anneal time which translates to the tunability being directly related to the grain size. This is validated by Figure 6-11 resembling the same trend as Figure 3-13 which shows grain size with respect to anneal time.

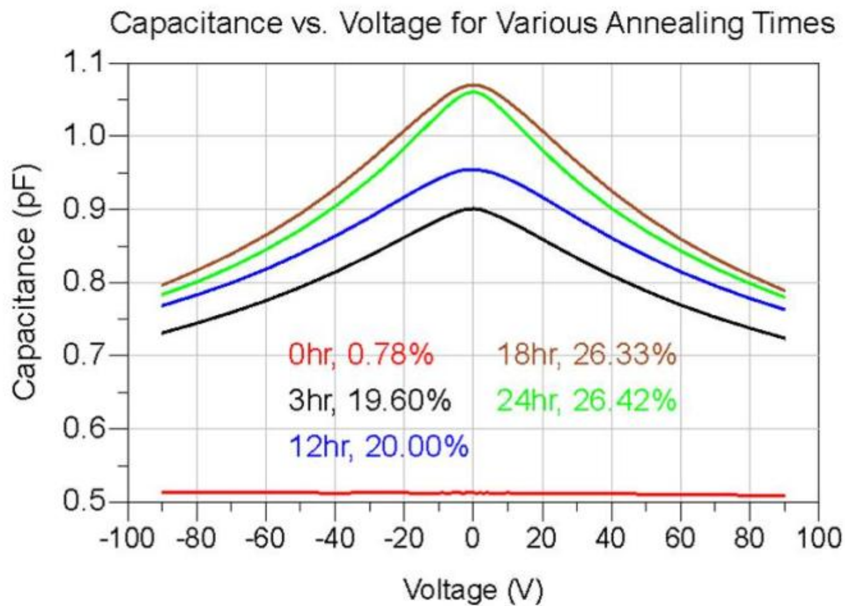


Figure 6-10: Capacitance vs. Voltage for Various Annealing Times

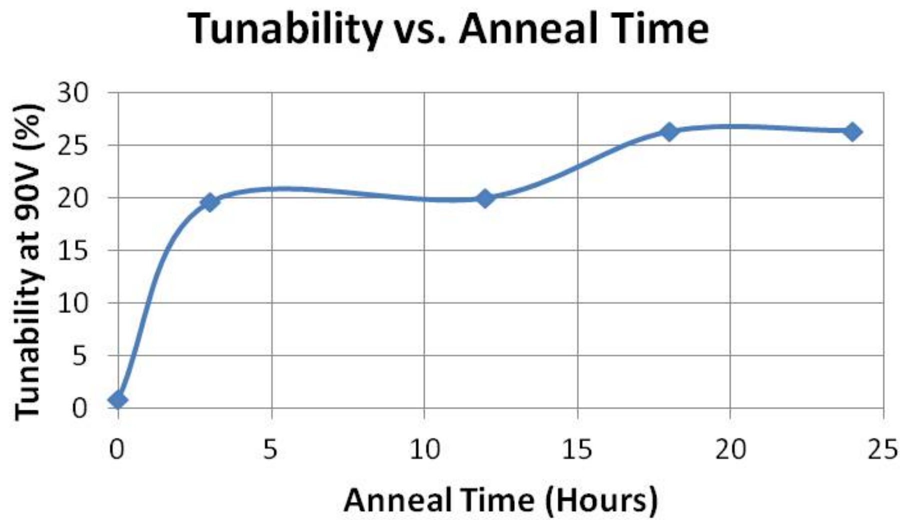


Figure 6-11: Tunability vs. Anneal Time

6.6 S-Parameter Measurements on Nanoscale IDCs

S-parameter data is collected for the IDCs with nanoscale gap sizes which are fabricated on 12 hour annealed BST films. For the case of the nanoscale IDCs, DC bias voltages up to 25V are applied. Beyond this voltage, the devices fail and behave as short. They are not able to withstand higher voltages due to the reduced gap size between the fingers compared to the microscale devices. The reduced metal thickness used for the electrodes of the nanoscale IDCs could also be a contributing factor in device failure at higher voltages. The capacitance and tunability are calculated by the same methods used for the microscale IDCs.

The CV curves for both geometries are displayed in Figure 6-12 and Figure 6-13. The average zero-biased capacitance of the IDCs with 65μm and 200μm long fingers is 0.23pF and 2.25pF, respectively. The tunability for both nanoscale IDC geometries is roughly the same at 23% and 22%. These tunability values are much higher than that of the 5-finger pair IDC with 5 μm gaps which has only a tunability of 5.35% with a 25V DC

bias. This is illustrated in Figure 6-14 which displays normalized C-V curves for the microscale and nanoscale devices. The nanoscale IDCs with 200μm long fingers have a zero-biased capacitance that is more than twice the capacitance of the IDCs with microscale gaps. Additionally, by comparing the size of the microscale and nanoscale geometries shown in Table 6-4, the nanoscale IDC electrode geometry has an area that is about 20% of that of the microscale-gap IDC. If an IDC geometry with nanoscale gaps is designed to give the same 1pF capacitance as the microscale-gap IDC used in this study, it would result in using an even smaller area than the geometry presented here with the 200μm long fingers. By substituting an IDC with nanoscale gaps for an IDC design with microscale gaps, the physical size can be reduced by over 80%. This is advantageous for several microwave circuit applications in which there is limited real-estate.

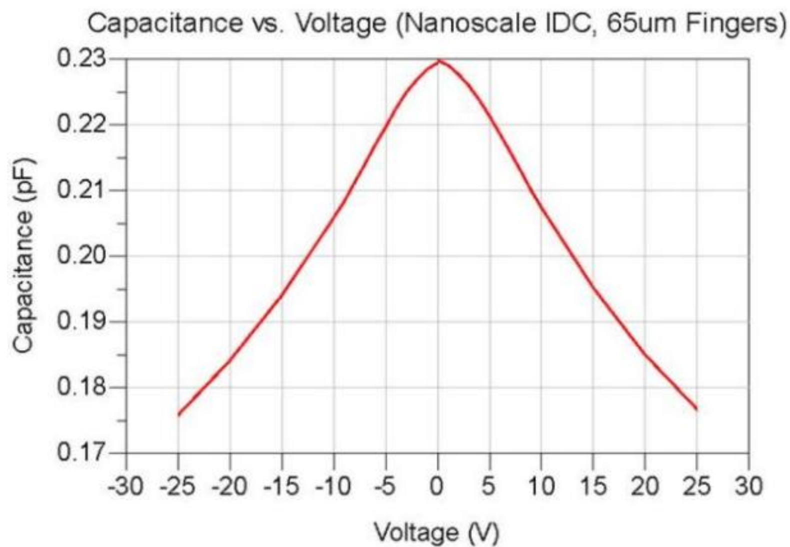


Figure 6-12: Capacitance vs. Voltage for Nanoscale IDC (65μm Fingers)

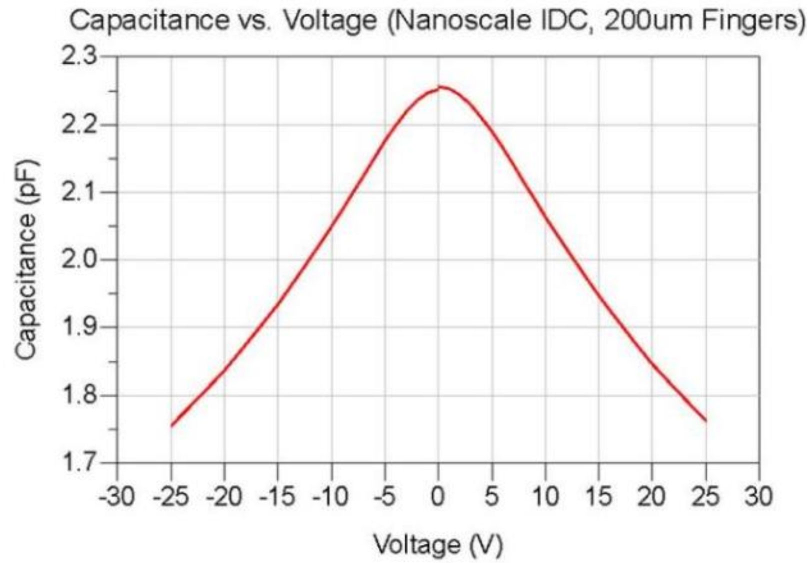


Figure 6-13: Capacitance vs. Voltage for Nanoscale IDC (200μm Fingers)

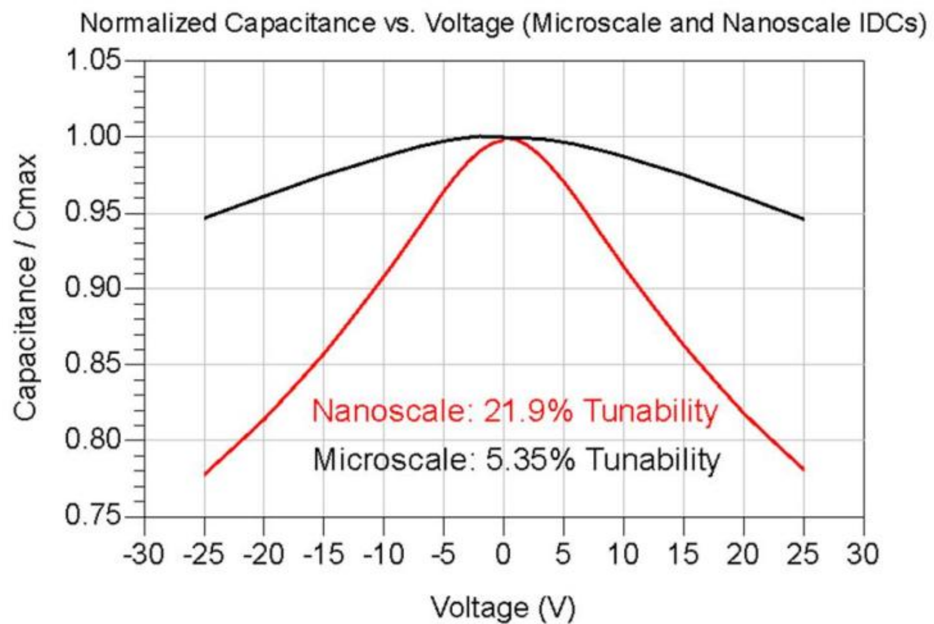


Figure 6-14: Normalized Capacitance vs. Voltage of Microscale and Nanoscale IDCs

Table 6-4: Varactor Comparison

Varactor Dimensions	Area (µm^2)	Cap at 0V (pF)	Cap at 25V (pF)	Tunability at 25V
Gap Size: 365nm Fingers: 65µm x 10µm	5525	0.23	0.177	23.04%
Gap Size: 365nm Fingers: 200µm x 10µm	60000	2.256	1.762	21.90%
Gap Size: 5µm Fingers: 400µm x 50µm	275225	0.954	0.903	5.35%

6.6.1 E-Field Confinement

When comparing the normalized capacitance of the 5µm gap devices to that of the 365nm gap devices, the device with the microscale gap actually appears to be more tunable as shown in Figure 6-15. However, for a given DC bias voltage, the E-field across the 365nm gap is going to be approximately 13 times greater than the E-field across the 5µm gap due to the scaling of the gap size. An approximation of the E-field can be calculated by dividing the bias voltage by the gap size. With a 25V DC bias, for example, the E-field across the 5µm gap is calculated to be roughly 5V/µm. However, the application of 25V across the 365nm gap yields an E-field of roughly 68.5 V/µm.

To confirm this, electrostatic simulations are performed using Ansys' Maxwell Software to observe E-field for the two gap sizes. Figure 6-16 shows the cross section of metal electrodes with a 5µm gap on top of alumina/BST along with the simulated E-field when a 25V bias is applied across the electrodes. Figure 6-17 shows the same but for a 365nm gap. When comparing the two simulated geometries, the E-field of the nanoscale gap is just over an order of magnitude larger than that of the microscale gap, and the E-field values displayed by the center of the color topography scale are similar to the E-field approximations previously calculated. Additionally, the simulation results show that more of the field is confined within the film for the nanoscale gap. The

tunability is greatly enhanced for the nanoscale gap device due to the increased E-Field Therefore, less voltage is needed to tune the nanoscale varactor down to a given capacitance compared to that needed for a microscale varactor which can lead to less power consumption for tunable BST RF components.

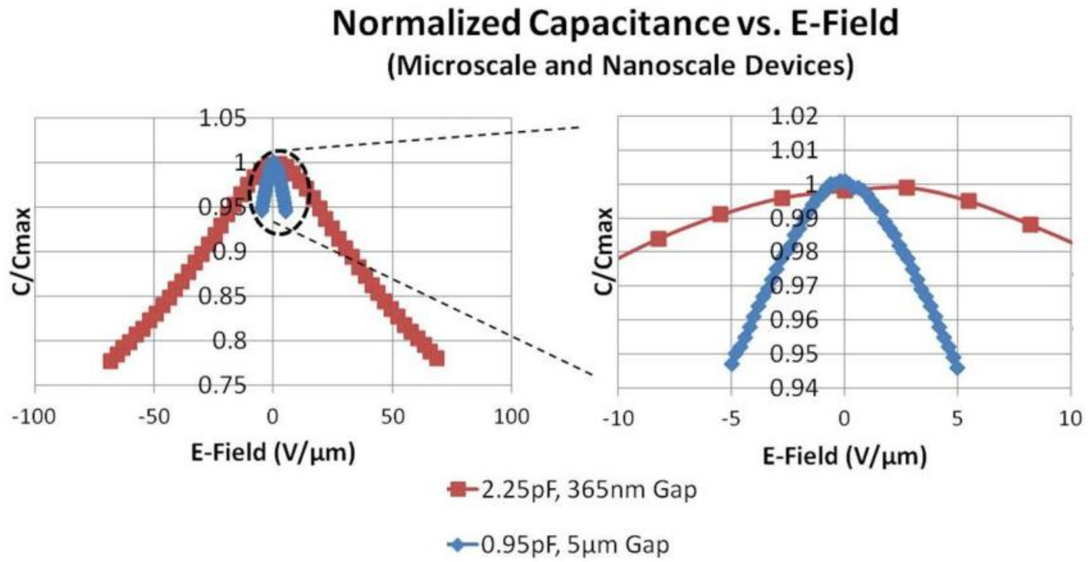


Figure 6-15: Normalized Capacitance vs. E-Field of Microscale and Nanoscale IDCs

0.95pF, 5µm Gap

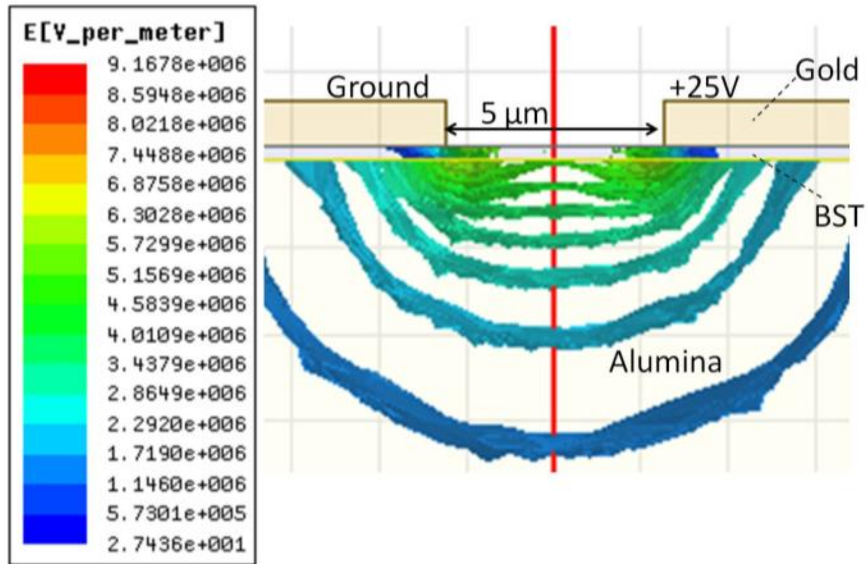


Figure 6-16: E-Field Confinement of 5µm Gap

2.25pF, 365nm Gap

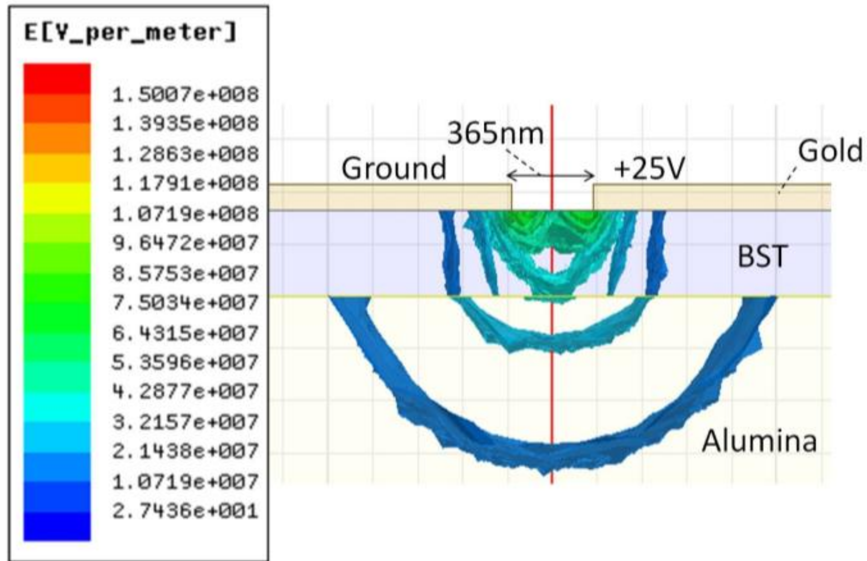


Figure 6-17: E-Field Confinement of 365nm Gap

Chapter 7 Nonlinear RF Measurements & Analysis

7.1 Introduction

The tunable nature of BST is derived from its electric field-dependent permittivity. With this behavior comes an innate nonlinear characteristic. The nonlinearity of BST devices must be accounted for in the design stages of RF components because of the possible generation of unwanted harmonics or intermodulation distortion products (IMD). This chapter discusses the nonlinear behavior of planar barium strontium titanate varactors. The methodology of two-tone measurements for observing device nonlinearity is presented. Details are given on previous investigations of the nonlinearity of BST varactors followed by the nonlinear characterization performed in this work.

7.2 Intermodulation Distortion

Nonlinear devices do not follow the concept of superposition, which means that they are capable of modifying the frequency spectra of its input signal. When two RF (sinusoidal) signals of frequencies ω_1 and ω_2 are placed into a nonlinear device (Equation 7-1), the output consists of a large number of mixing terms as shown in Equation 7-2 where $\omega_r = m\omega_1 + n\omega_2$, and m, n ∈ Z [95].

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \quad \text{Equation 7-1}$$

$$y(t) = \sum_{r=1}^{\infty} A_r \cos(\omega_r t + \theta_r) \quad \text{Equation 7-2}$$

All of the mixing frequencies (ω_r) generated by the combination of the two original tones are referred to as intermodulation distortion (IMD) products.

An illustration of how this concept works is shown in Figure 7-1. If two signals of different frequencies are inserted into a linear device, theoretically, the output would consist of two signals at the same frequencies as the input signals but scaled in amplitude. However, if this same test was done on a nonlinear device, the output would again have the same two signals at the same frequencies scaled in amplitude in addition to harmonics and IMD products that are generated by adding multiples of the two original tones together.

IMD products can present a serious problem in communication receivers because they can interfere with the desired signals. This is particularly the case for third order IMD products because these mixing terms are the closest in frequency to the fundamental/desired tones, and they are the strongest of the generated IMD products [96]. With the third order products being so close to the desired signals, they cannot be filtered out without disturbing the desired tone.

One method of analyzing the nonlinearity of a device is to observe the generated IMD products when two signals of different frequencies are inserted into the device. This measurement concept is formally known as a two-tone measurement [95]. The power levels of the harmonics and IMD products can be measured to characterize the overall nonlinear behavior of the device. Although higher order IMD products such as 5th and 7th can be observed, generally the 3rd order IMD products are of primary interest for reasons previously mentioned.

7.3 Previous Studies of BST Device Nonlinear Characterization

Previous research shows that the capacitance-voltage curve for BST varactors compresses as temperature is increased [75, 97]. Lourandakis et al shows this behavior for a parallel plate BST varactor used for a tunable power divider. However, no

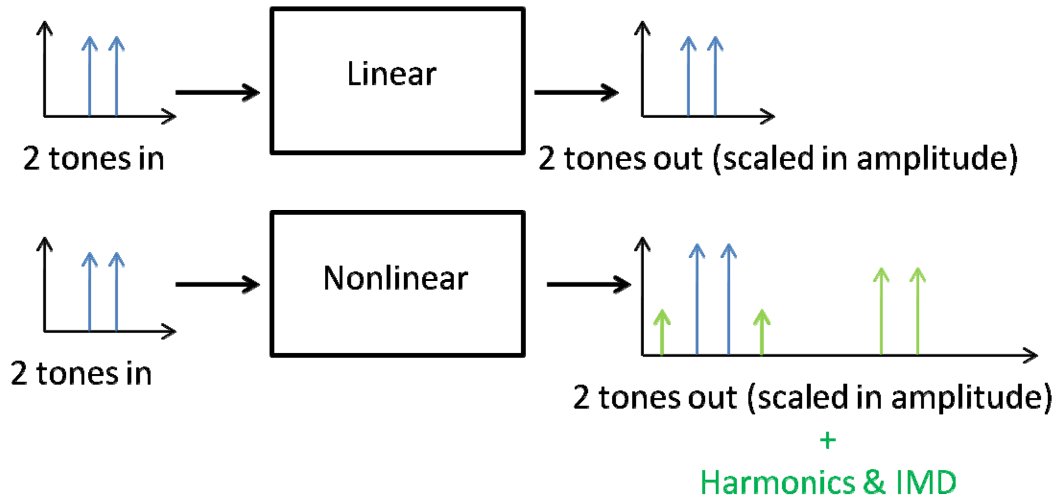


Figure 7-1: Linear vs. Nonlinear Device Behavior

intermodulation distortion data is presented to correlate with the C-V behavior. On the other hand, Deleniv et al shows temperature dependent C-V behavior along with temperature dependent IMD data in the form of third order intercept calculations for parallel plate devices. It is unclear, however, what input RF power levels are used to calculate the third order intercept. It also appears that the third order intercept is calculated using the 3rd harmonic and fundamental tone in this work. Traditionally, the third order intercept is calculated using the third-order IMD product making the validity of this calculation questionable.

There is limited literature regarding the voltage impacts on the intermodulation distortion products of BST varactors. Chakraborty et al, show the effects of voltage on the third order intercept for a BST varactor based bandpass filter [98]. The third-order intercept remains constant throughout the tested voltage range, up to 300V. For this particular case, however, the filter is fabricated on a bulk BST substrate that is roughly 2 mm thick. The third-order intercept remains constant because very high voltages are necessary to tune the varactors using the bulk BST substrate. Such high voltages are

not needed when using BST thin films for making tunable devices; therefore, the nonlinearity will be impacted by the application of lower DC voltages. The voltage dependent nonlinearity of BST thin film varactors needs to be investigatedPrevious studies show that annealing BST films can alter the internal structure, primarily the interplanar spacing and grain size [18]. It has been shown that as the grain size becomes larger, the dielectric constant and film tunability increases [99]. Although the material properties have been linked to the RF properties of dielectric constant and tunability, correlating the internal structure of the film to the intermodulation distortion of BST varactors has not yet been explored.

Although previous studies have been carried out on the nonlinear behavior of BST RF and microwave devices, there are still other areas that need to be investigated for planar BST thin film varactors. Correlating the material properties to the nonlinear behavior of varactors is important in the design stages of BST based RF components. The voltage and temperature effects on the nonlinear behavior of planar varactors needs to be further investigated for RF devices that may be subjected to different environments/climates. These key items need to be addressed along with observing the nonlinear behavior of nanoscale BST varactors, which is a primary objective of this work.

7.4 Nonlinear Behavior of Microscale IDCs (MgO vs. Alumina)

The two-tone test bench displayed in Figure 7-2 was used to collect the first round IMD data to compare the nonlinearity of devices fabricated on alumina and MgO substrates. Each RF signal is produced by an HP signal generator. Two 10 Watt amplifiers are used to increase the power level of the RF signals. Isolators and low pass filters are used to lower the power levels of any harmonics that may be generated by the

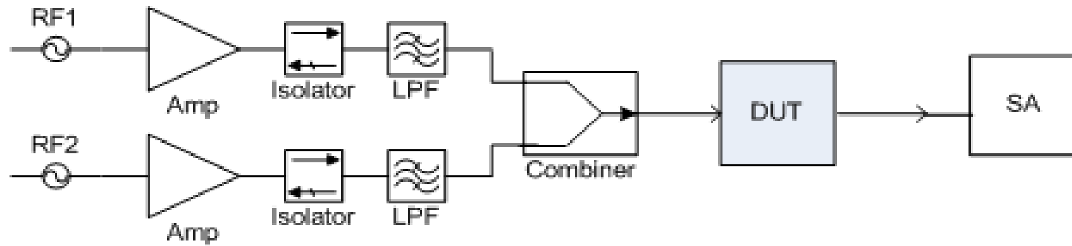


Figure 7-2: Two-Tone Test Bench

amplifiers. Once both tones are filtered they are combined and inserted into the device under test (DUT). The output of the DUT is then measured using a spectrum analyzer.

Previous research has shown that the IMD performance of the BST devices can be impacted by the tone spacing used during two-tone measurements [16, 100]. The observed change in the IMD power levels with respect to tone spacing can be correlated to the response time of the BST film. To ensure that the film is responding to the RF signals and due to equipment limitations, a 1MHz tone separation is chosen for this work. Fundamental tones of 950 MHz and 951 MHz are used for this series of measurements.

The nonlinear behavior of the IDCs is observed at 0 Volts DC bias for the first round of measurements. Theoretically, this is the applied DC voltage where the devices are most nonlinear [57]. Maury Microwave's Automated Tuning System along with one of the thru lines from the TRL calibration is used to calibrate the two-tone test bench before measuring the IDCs. Third order intermodulation distortion (IMD) products of the thru are measured to analyze the linearity of the test bench. This is done to ensure that the IMD products that are observed with the spectrum analyzer when measuring the devices under test are being generated by the IDCs and not the test bench itself. As long as the observed IMD of the IDCs is higher than that observed when measuring the thru, then

the measured IDC data is assumed to be valid. Figure 7-3 shows the measured third order IMD for the thru and the measured IDCS.

The 3rd order IMD generated by the IDCs overcomes that of the thru lines when hit with an input RF power at or above ~25 dBm. Although measurements are taken with an input RF power ranging from 1 – 34 dBm, the displayed data in Figure 7-3 has been truncated to illustrate valid data only. It is observed that the 3rd order IMD produced by the alumina devices is higher than that of the MgO devices at RF power levels above ~29 dBm.

Also, the nonlinearity of the measured IDCs appears to be dependent on the number of fingers. As the number of finger pairs increases for the alumina devices, the power level of the 3rd order IMD decreased. Increasing the number of fingers would decrease the capacitive reactance, lowering the RF voltage that is being placed across the device. By reducing the RF voltage swing along the static C-V curve of the device, it behaves in a more linear fashion [101, 102] which reduces the power level of the 3rd order IMD as shown in Figure 7-3.

A similar trend is noticeable with devices fabricated on MgO substrates when comparing the 3 finger pair IDCs to both the 5 and 7 finger pair IDCs. It is believed that the 5 finger pair IDCs on MgO would have been more nonlinear than the 7 finger pair IDCs if the measured 5 finger device had not produced outlying data.

The overall trend of the data for the alumina devices shows that the IDCs are being driven into compression at the displayed input RF power levels. This compression, along with the observed dips in the curves are possibly due to higher order IMD products that are being produced and cancelling out the 3rd order IMD products [57].

The 3rd order IMD data displayed for the measured thru shows that the noise floor of the system is at about -45 dBm for this case. Therefore, unless the IMD power level of the DUTs is above this value, it is not feasible to obtain accurate data for the DUT. In order to obtain accurate IMD data at lower input RF power levels, the two-tone test bench has to be modified.

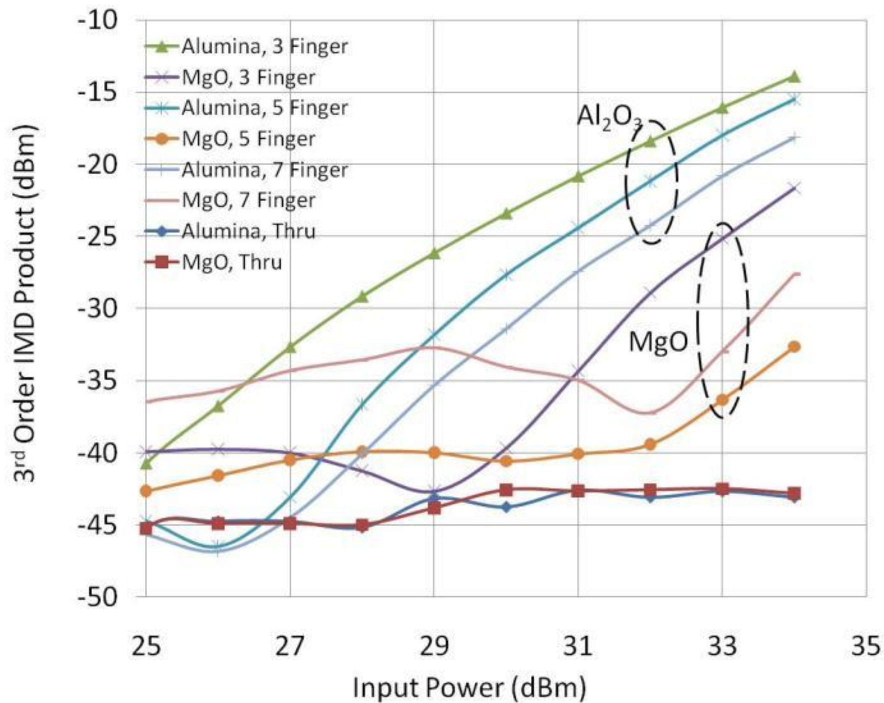


Figure 7-3: 3rd Order IMD of All Device Types and Thru Lines on MgO and Alumina

7.5 Two-Tone Testbench Modifications

When using a high RF power level to measure intermodulation distortion products, it is important to keep the test bench itself as linear as possible to ensure that all nonlinearities are coming from the DUT. Undesired nonlinearities can typically be generated by the internal mixer of the spectrum analyzer when performing two-tone measurements especially when attempting to use moderately high RF power levels for

the two tones. To accurately measure the nonlinearity of the DUT, it needs to be driven with a high RF power level while not overdriving the spectrum analyzer at the output of the DUT. Adding a filter at the back-end of the test bench to reduce the fundamental tone power level will not help to achieve this goal because the 3rd order IMD products are typically close in frequency to the fundamentals and will be filtered out as well.

A tone cancellation scheme is implemented to reduce the power level of the fundamental tones before reaching the spectrum analyzer without impacting the 3rd order IMD data [16]. Additional components consisting of 2-way splitters, continuously variable attenuator (CVA), phase shifters, and a 3-way combiner have to be added to the original test bench to accomplish this. As shown Figure 7-4, each fundamental tone is divided in half using 3 dB power splitters. Half of each tone travels down the main branch of the test bench leading to the DUT. The other half of each tone goes through a tone cancellation branch containing a phase shifter and a CVA. The phase shifters are used to ensure that the half of each tone going through the cancellation branch was 180° out of phase with its other half that travels down the main branch before recombining the 2 halves at the 3-way combiner. The CVA is used to make sure the two halves are equal in amplitude. Once the two halves meet at the 3-way combiner, they destructively intefere with one another which significantly reduces the power level of the fundamental tone before it reaches the spectrum analyzer. This method allows the DUT to be subjected to a high RF power level without pushing the spectrum analyzer to a nonlinear, and perhaps damaging, point.

The spectrum analyzer has a built in automatic input attenuator that is used to protect itself when it is subject to high RF power levels. When the input RF power level reaches a certain threshold, the input attenuation level increases to avoid damaging the internal mixer. The major caveat this presents is that when the input attenuation level

increases, the noise floor the spectrum analyzer rises with it. As the noise floor rises, it becomes more difficult to observe 3rd order IMD of relatively low amplitudes. Since the tone cancellation scheme lowers the RF power level of the fundamental tones before reaching the spectrum analyzer, it prevents the input attenuation level from rising thus keeping a low noise floor of the spectrum analyzer. The tone cancellation scheme not only helps to ensure that the observed IMD is coming from the DUT. It also allows for a low noise floor of the test bench, enhancing the ability to accurately measure low power IMD products.

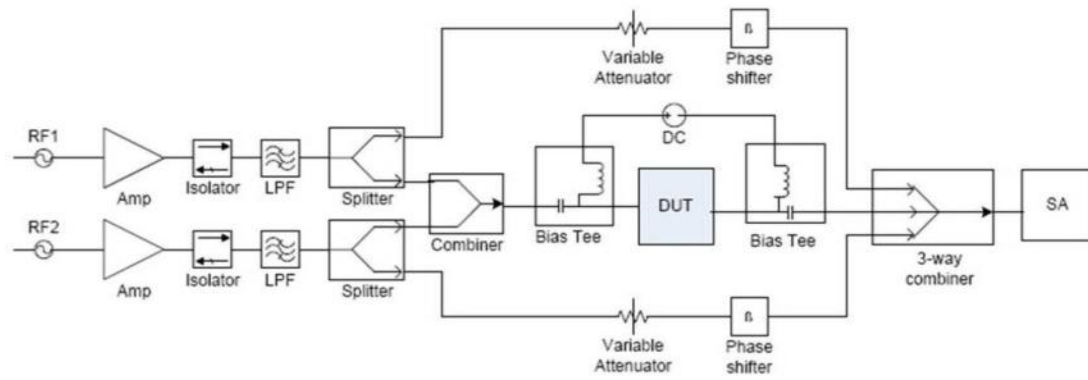


Figure 7-4: Modified Two-Tone Test Bench

7.6 Temperature and Voltage Dependent Nonlinearity

The modified two-tone test bench was used to observe the temperature and voltage impact of BST varactors. Due to bandwidth limitations of components that were added to modify bench, the frequencies of the tones had to be altered to 1 GHz and 1.001 GHz. Bias tees were used in the modified test bench to study the DC voltage impact on the DUT nonlinearity. Since it was previously determined that the devices on alumina substrates are more tunable and nonlinear than those on MgO, only the IDCs on

alumina were used for this analysis. Only the 5 finger pair microscale IDCs are measured for this case.

In the following plots displaying the 3rd-order IMD, the term I3_lo corresponds to 2f1-f2 (0.99 GHz) and I3_up corresponds to 2f2-f1 (1.002 GHz). The combined power level of the RF tones was swept from -20 dBm to 34 dBm. Figure 7-5 shows I3_lo vs. the combined input RF power level (consisting of both tones) at 25ºC for various applied DC voltage levels. The noise floor of the test bench was established at approximately -80 dBm. This shows that the tone cancellation scheme that was implemented in the two-tone test bench decreased the noise floor of the system by approximately 35 dB. Although the lower limit of the input RF power was -20 dBm during the measurements, no significant data is observed until the input RF power reaches about 10 dBm. Therefore, the plotting range has been truncated accordingly for the subsequent plots.

Figure 7-6 shows the same data as Figure 7-5 with the focus being on the observed relative minimum/dip in the plotted I3_lo. When viewing the 3rd-order IMD vs. input RF power, there is a notch in the data that is very similar to the nonlinear behavior of power amplifiers [103]. It has been documented that these minimum points, also known as sweet spots, are caused by higher-order IMD products (such as 5th and 7th) interacting with the 3rd order IMD products when the DUT is subject to large incident RF signals [95, 103, 104].

At input RF power levels below that of the location of the notch, the power levels of I3_lo decrease with applied DC voltage. This occurs due to the behavior of the static C-V curve. When the RF voltage is superimposed along the C-V curve at a particular DC voltage setting (V_{DC}), the instantaneous change in the capacitance caused by the RF

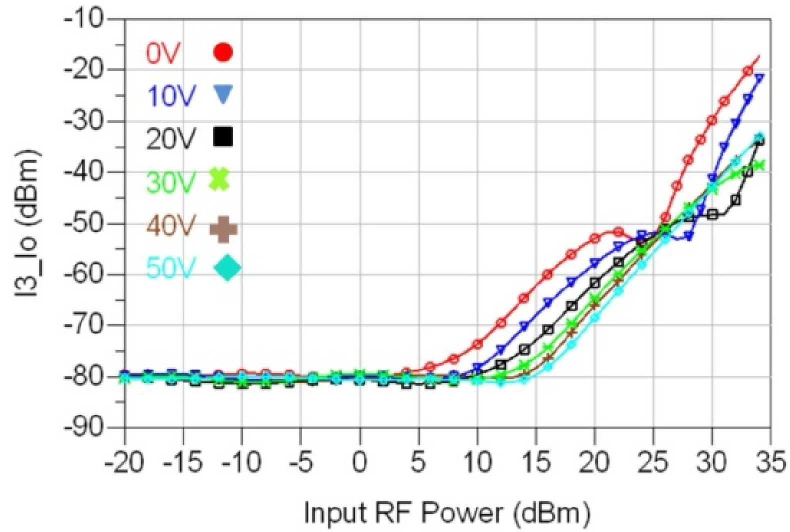


Figure 7-5: I3_lo vs. Input RF Power at Different DC Bias Voltages, Displaying Noise Floor

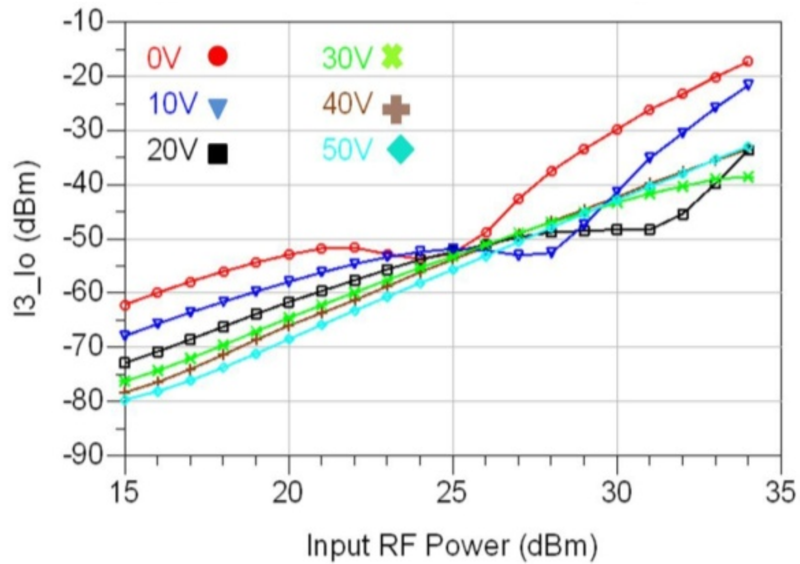


Figure 7-6: I3_lo vs. Input RF Power with Varied DC Bias Voltage at 25°C

voltage swing decreases as $|V_{DC}|$ increases [105]. Therefore, the BST varactor will behave in a more linear fashion at higher DC voltages.

Also as shown in Figure 7-6, the location of the I3_lo dip shifts to higher input RF power levels as V_{DC} increases. The same behavior is observed for I3_up which is

shown in Figure 7-7. The dip location can shift upward with respect to RF power by about 4–5dBm for every 10 volt increment of DC bias applied to the device. Figure 7-7 also shows that the dip can cause I3_up to be 10 dB below its expected value with a 20 volt DC bias. Behavior such as this is important to consider when predicting the nonlinear behavior of BST varactors.

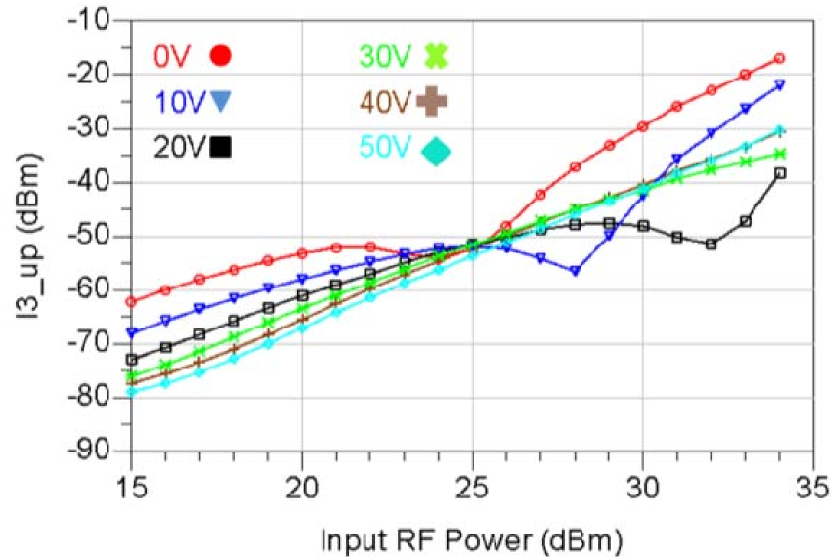


Figure 7-7: I3_up vs. Input RF Power with Varied DC Bias Voltage at 25°C

The nonlinear behavior is also observed while varying the temperature without the application of DC voltage. Figure 7-8 and Figure 7-9 show I3_lo and I3_up vs. input RF power, respectively. The temperature is incremented from 25 to 125°C. As the temperature increases, the power level of the 3rd-order IMD products decreases. This correlates with the overall compression of the C-V curve with increased temperature shown in Figure 6-9.

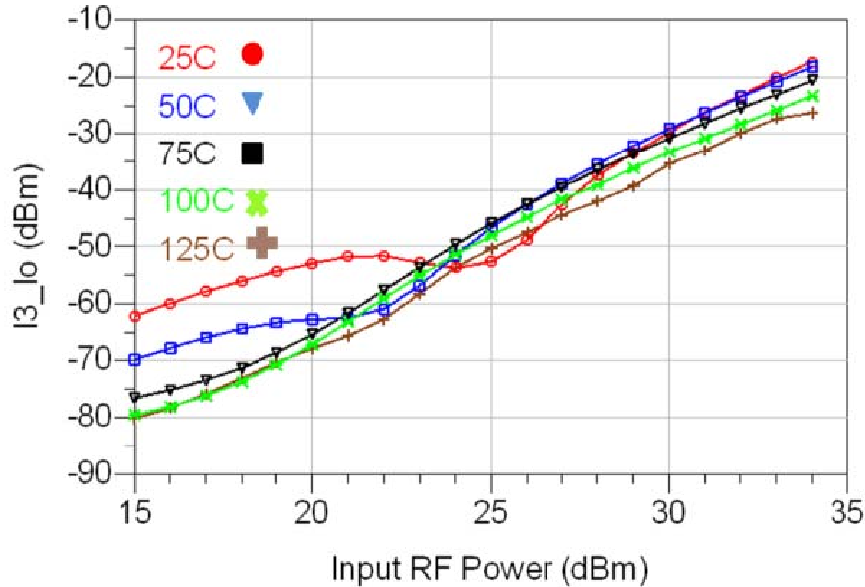


Figure 7-8: I3_lo vs. Input RF Power at 0 Volts with Varied Temperature

7.7 Annealing Dependent Nonlinearity of Microscale Devices

In an effort to correlate the BST thin film material properties to the nonlinear behavior of the BST varactors, two-tone measurements are taken on IDCs fabricated with BST films annealed for various times. The lower-band (I3_lo) and upper-band (I3_up) third order IMD products are displayed in Figure 7-10 and Figure 7-11, respectively. Each trace represents an average obtained from measuring three different 5-finger pair devices. Similar to previous two-tone measurement results, I3_lo and I3_up are approximately identical.

For the case of the IDCs with non-annealed BST films, the power levels of the measured third order IMD products remain below the noise floor until an RF power of about 28 dBm is inserted into the device. For all of the other annealing conditions, the third-order IMD power level rises above the noise floor at an input RF power of approximately 10 dBm. This means that IDCs with annealed BST films will behave in a more nonlinear fashion compared to those with non-annealed films. The low third-order

IMD power level of the non-annealed samples stems from the flat nature of its C-V curve displayed in Figure 6-10. The capacitance of IDCs using non-annealed BST is nearly independent of the applied DC bias voltage; hence, making them more linear.

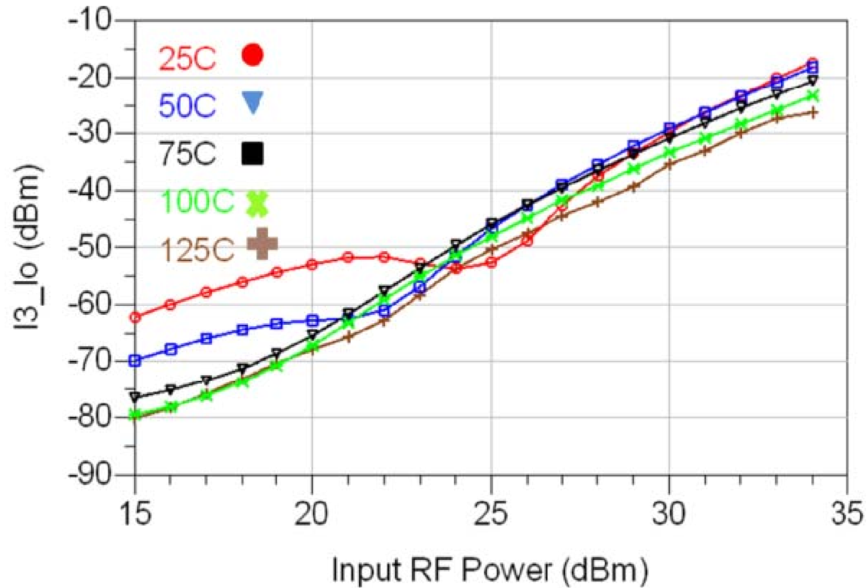


Figure 7-9: I3_up vs. Input RF Power at 0 Volts with Varied Temperature

Unexpectedly, the I3_lo for the 12 hour annealed films starts to slope toward a relative minimum point/sweet-spot before that of the films annealed for 18 hours and 24 hours when observed with respect to the input power. The dip for the 12 hour I3_lo data is seen at an RF power level of 25 dBm while the dip in the I3_lo data for 18 hours and 24 hours does not occur until reaching an input RF power of about 30 dBm.

At low input RF power levels (before the sweet-spot occurs), the third order IMD power levels of the IDCs with variously annealed BST films follow somewhat of an expected trend. For instance, at an input RF power of 15 dBm, the I3_lo power levels increase with anneal time as shown in Figure 7-12. The trace displayed here resembles that of Figure 6-11 which shows tunability vs. anneal time. This confirms that the

behavior of the third order IMD of BST varactors corresponds directly to the tunability of the device. Furthermore, a relationship of the third-order IMD power level and the grain size is established and shown in Figure 7-13. The third-order IMD power levels increase as a function of grain size.

7.8 Nonlinear Behavior of Nanoscale Varactors

Two-tone measurements are taken at room temperature on the IDC varactors fabricated with nanoscale gaps to observe their nonlinearity. The maximum RF input power was reduced to 30 dBm in an effort to avoid damaging the measured devices. As shown in Figure 7-14, the upper band and lower band third order IMD products match fairly well. The lower band third order IMD products for both nanoscale geometries and the 5-finger microscale gap IDC (all with 12 hour annealed films) are displayed in Figure 7-15. The dips in I3_lo occur at lower input RF powers for the nanoscale IDCs compared to that of the microscale IDCs. This means that the higher order IMD products that contribute to the dip come into play at lower RF power levels for the nanoscale IDCs. To get more of a quantifiable comparison of the nonlinear behavior of the nanoscale and microscale IDC, the output third order intercept (OIP3) is calculated for each device using the expression

$$OIP3(dBm) = P_{F1_OUT}(dBm) + \frac{P_{3_IMD}(dBc)}{2} \qquad \text{Equation 7-3}$$

where PF1_out is the power of one of the fundamental tones at the device output in units of dBm and P3_IMD is the power level of the third order IMD in (dBC). The OIP3 is calculated for each device type for a range of input RF power and is displayed in Figure 7-16. The nanoscale device with 65μm long fingers (~0.23pF capacitance) has the lowest OIP3, meaning that it exhibits more nonlinearity than the other two IDC

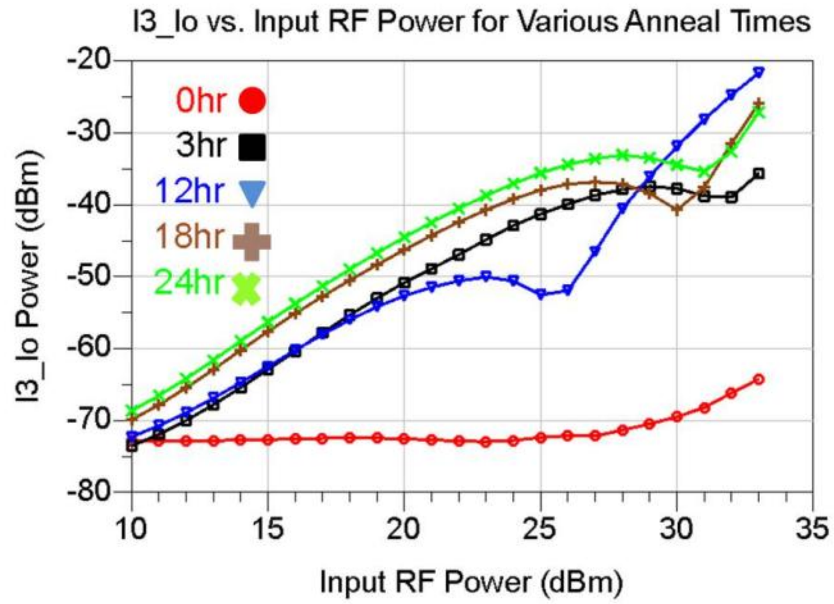


Figure 7-10: I3_lo vs. Input RF Power for Various Anneal Times

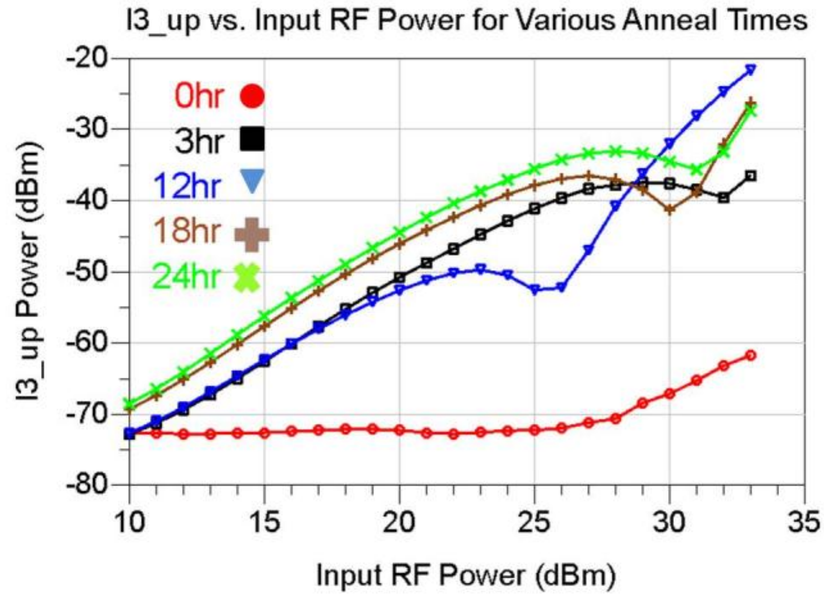


Figure 7-11: I3_up vs. Input RF Power for Various Anneal Times

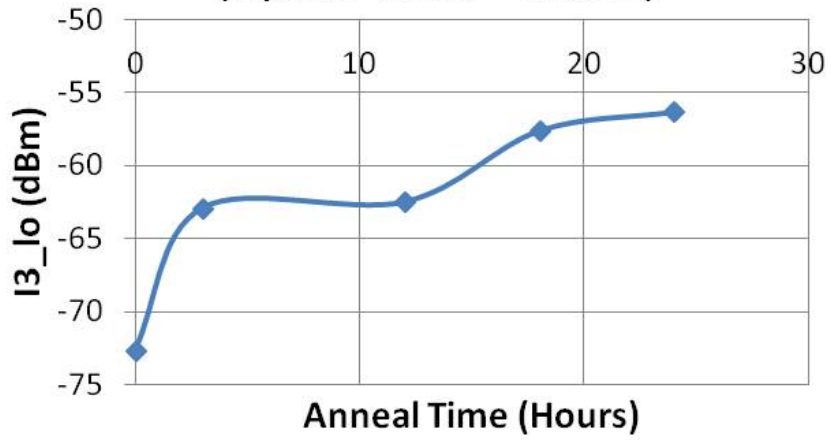


Figure 7-12: I3_lo vs. Anneal Time

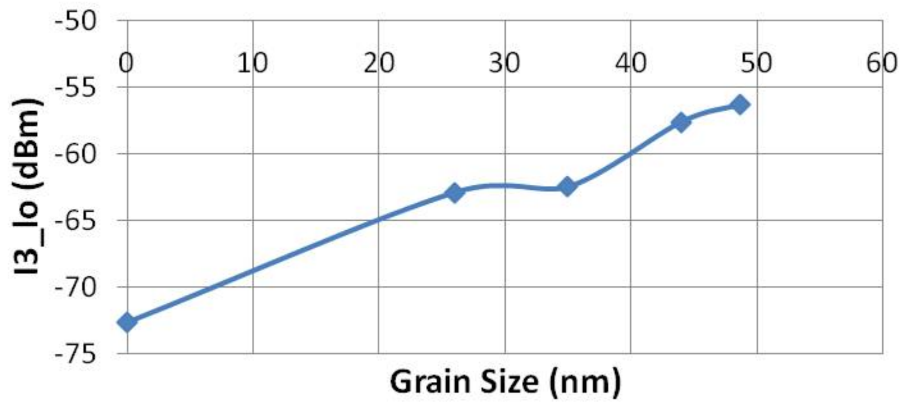


Figure 7-13: I3_lo vs. Grain Size

geometries. The nanoscale IDC with 200μm long fingers (~2.25pF capacitance) has an OIP3 that is higher than that of the microscale IDC (~0.95pF capacitance). Even though the nanoscale IDC with 200μm long fingers has a higher tunability than the microscale IDC, it behaves in more of a linear fashion than the microscale IDC. This shows that the nonlinearity of BST varactors is not just dependent on the tunability, but on the zero-bias capacitance as well for reasons explained in section 7.2.

Potentially, a microscale BST varactor with a given zero-bias capacitance can be replaced by a much physically smaller nanoscale BST varactor designed for the same capacitance, yielding higher tunability (as shown in Chapter 6) and possibly IMD behavioral traits that are very similar. This could be advantageous for RF and microwave applications in which maintaining a linear system is a priority.

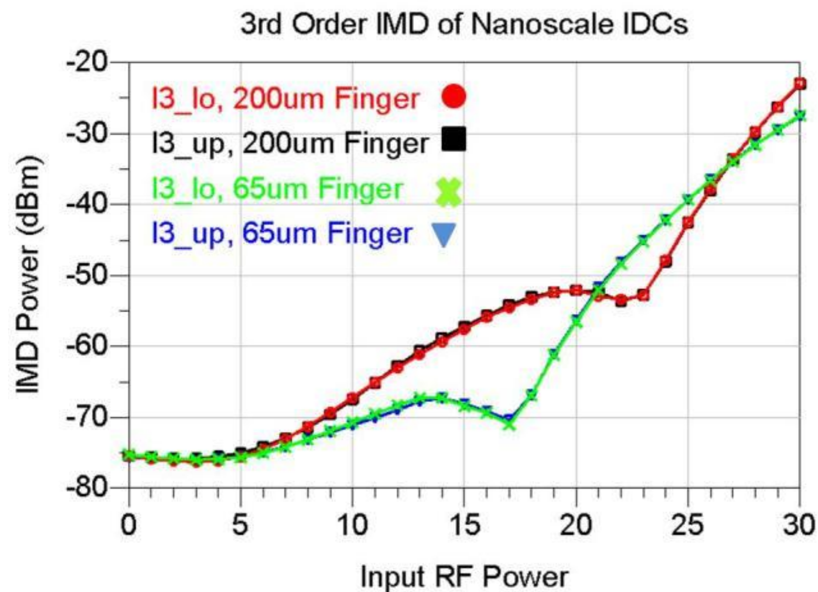


Figure 7-14: Third-Order IMD vs. RF Input Power of Nanoscale IDCs

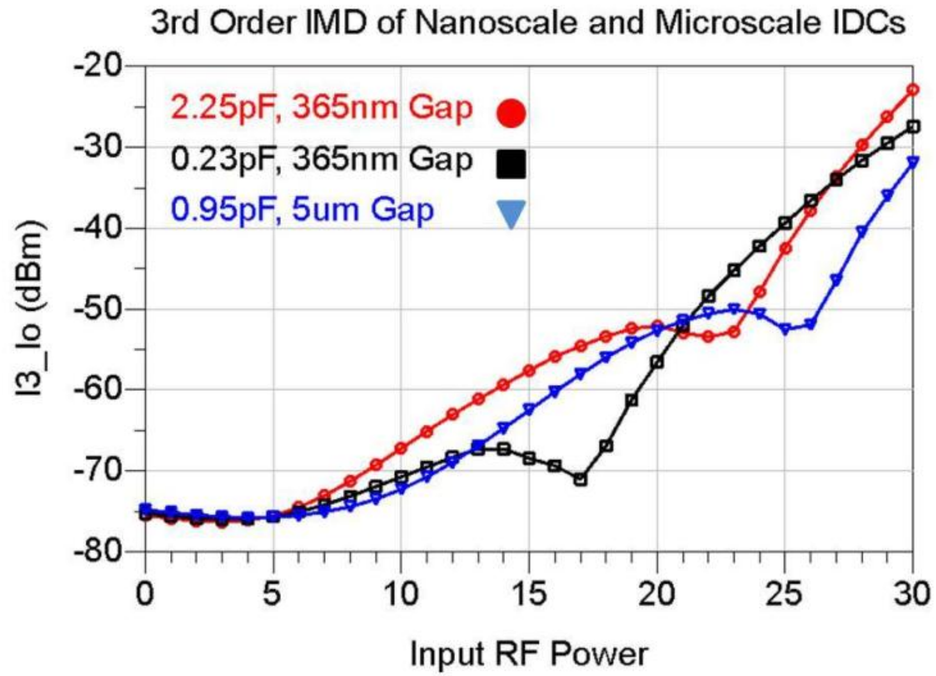


Figure 7-15: Third-Order IMD Comparison of Nanoscale and Microscale IDCs

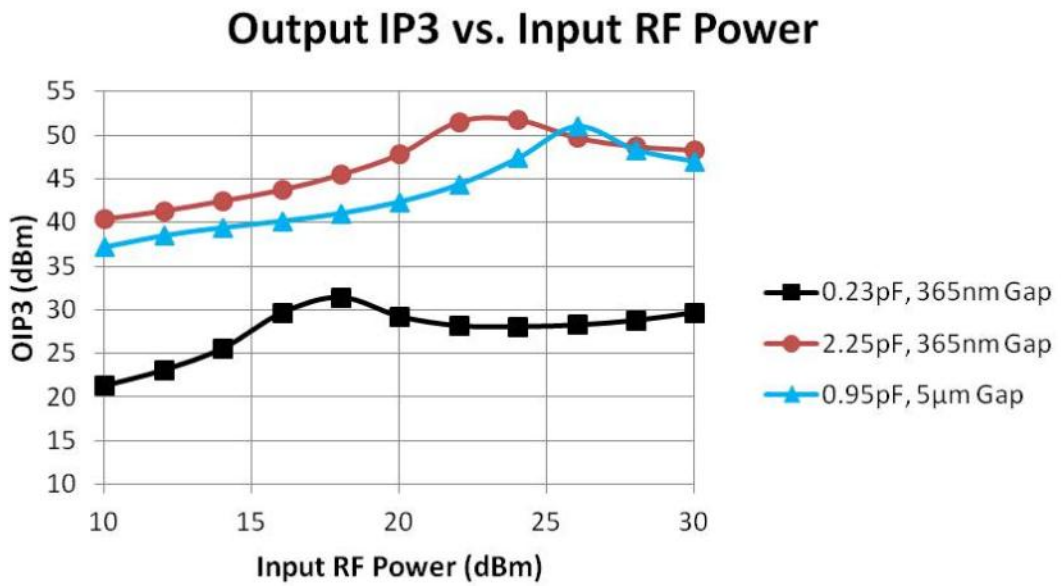


Figure 7-16: Output Third-Order Intercept Comparison of Nanoscale and Microscale IDCs

Chapter 8 Modeling

8.1 Introduction

When integrating RF and microwave components into full systems, it is important to know how the components are going to behave under certain conditions based on the potential environments that the final system will be subjected to. Hence, it is imperative to have accurate models to predict the microwave behavior of components, BST varactors in this case. This chapter discusses the modeling aspects of this work. A summary of previously derived models for BST varactors along with their shortcomings is presented. Details are then given on the equivalent circuit and mathematical modeling techniques used in this work to simulate the behavior the BST varactors. First, the C-V curve is addressed followed by the IMD behavior. Future modeling considerations for BST varactors are also discussed.

8.2 Previous Studies of BST Varactor Models

With increased RF applications of BST varactors comes the necessity for accurate models that are needed in the design stages. Chase et al. have developed the following expression for the DC voltage dependent capacitance of parallel plate BST devices:

$$C(V) = \frac{C_{\max} - C_f}{2\cosh\left[\frac{2}{3}\sinh^{-1}\left(\frac{2V}{V_2}\right)\right] - 1} + C_f \qquad \text{Equation 8-1}$$

where C_{max} is the maximum capacitance at zero DC volts, C_f is the fringing capacitance, and V_2 represents the voltage at which $C(V) = {}^{C_{max}}/_{2}$ [74]. This model is based on a power series expansion of the field-polarization relation described in the Landau-Devonshire-Ginzburg model. Equation 2-1 is further developed to be dependent on the thickness of the BST thin film to account for the non-tunable interfacial capacitance. A temperature dependence at 0 Volts DC bias is also presented.

Chase's model is referenced and further expanded by Schmidt et al. to consider nonlinear conductance [106]. The expression for the differential conductance was assumed to be:

$$G(V) = \gamma_0 + \frac{\gamma_1 / \gamma_2}{1 + \left(\frac{V}{\gamma_2}\right)^2} \qquad \text{Equation 8-2}$$

where $\gamma_0, \gamma_1, \text{and } \gamma_2$ are fitting parameters. The model was verified up to an RF power level of 10 dBm by comparing two-tone measurement results of an SP2T switch with ADS simulations utilizing symbolically defined devices (SDDs). Above 10 dBm, the model no longer fits the data. Although this model accounts for the device geometry of parallel plate devices, film thickness, and fringing capacitance, a correlation between the RF signal level and the capacitance was not established. Also, in [106], it is not stated if the two-tone measurements were taken with an applied DC bias voltage to verify the model. Other shortcomings of this model are discussed later in Chapter 8.

In [107], planar STO varactors are used to fabricate microstrip resonators. The effect of the RF signal level on nonlinear response is examined at 1.7 – 1.9 GHz by

measuring the level of the third order intermodulation distortion signal relative to the input signal level. The fundamental tones were 1 MHz apart and the power for each tone was 22 dBm. When a DC bias voltage was applied, the level of the third order IMD product was depressed relative to the output power at the fundamental frequency. The DC bias also caused the resonator transmission coefficient to increase, which was attributed to a lower loss tangent with increasing DC bias. As in [106], the capacitor impedance is modeled as parallel connected capacitance and conductance which are both dependent on microwave voltage and presented as a power series. It was also stated that the losses increase with microwave voltage, but decrease with increasing DC voltages.

A third order IMD transfer function was derived depending on the incident power, the varactor reactance, and the resonator quality factor in [107].

$$P_{3out} = 36 X_c^2 Q_e^2 \xi^2 S_{21}^6 \frac{1+\left(\frac{U_0}{U_g}\right)^4 (X_c g_0)^2}{U_0^4 [1+(X_c g_0)^2]} P_{1inc}^3 \qquad \text{Equation 8-3}$$

In Equation 2-3, ξ is the inclusion coefficient (defined as the ratio of capacitive RF energy stored in the capacitor to the total energy stored in the resonator microstrip line and capacitor), X_c is the varactor reactance, and Q_e is the external quality factor of the resonator. The transfer function shows a relationship between the P_{3out} and the capacitor reactance, but it does not appear that this expression accounts directly for the DC bias voltage. This function may have been derived for 0V DC bias, and it does not seem to account for the polarization of the STO film. It seems that this expression could have been derived no matter what type of capacitor was placed into the resonator. The argument that this expression is dependent on STO film properties is questionable.

Rundqvist et al developed a large signal model for parallel plate ferroelectric varactors based on measurements using RF signals ranging from -10 dBm to 17 dBm at 0 Volts DC bias [77]. In this study, all the RF characterization is completed using either a vector network analyzer or LCR meter. Therefore, all higher order harmonics are measured as losses. No measurements were actually carried out using a spectrum analyzer, but it is stated that the harmonic generation of the model was verified using ADS. Measured data of harmonics and intermodulation distortion products would have provided stronger validation.

8.3 C-V Modeling

In an attempt to model the C-V behavior of the BST varactors, the expression in Equation 2-1 derived in [74] is used in a symbolically defined device (SDD) component in ADS. The results are labeled as “Chase Model” in Figure 8-1. A second model discussed in [106], which accounts for nonlinear conductance, (labeled as “Schmidt Model” in Figure 8-1) is also investigated. Although both models are popular for predicting the C-V behavior of BST varactors, neither can be used to accurately emulate the measured C-V behavior of the devices used in this work. It is likely that this deficiency stems from the fact that these models were developed for parallel plate structures. Only the 5-finger pair IDCs with microscale gaps are considered for modeling purposes in this work since this is the only geometry that is subject to all aforementioned measurement techniques.

A cubic spline interpolation fit was performed using MATLAB to model the measured C-V behavior. A list of measured data points consisting of n ordered pairs consisting of a voltage value and its corresponding capacitance is used by the MATLAB program to generate n-1 third order polynomials to fit the measured C-V curve. There is a separate

polynomial to fit (interpolate) the data between all the measured data points. The complete C-V expression derived by the spline interpolation is expressed as a piecewise function of the following in the form:

$$C(V) = \begin{cases} c_1(v) & if\ v_1 \le v \le v_2 \\ c_2(v) & if\ v_2 \le v \le v_3 \\ \vdots & \\ c_{n-1}(v) & if\ v_{n-1} \le v \le v_n \end{cases}$$ Equation 8-4

where c_i is a third order polynomial in the form:

$$c_i(v) = a_i(x - x_i)^3 + b_i(x - x_i)^2 + c_i(x - x_i) + d_i$$ Equation 8-5

for *i* = 1, 2, . . . *n-1*. The MATLAB code is shown in Appendix E. Once the polynomial is created, it is then inserted into an SDD component in ADS and simulated. The results, labeled as “Spline Model”, are shown in Figure 8-1. Even though the spline model lacks physical significance, it provides a better fit for the measured C-V data than the two previously discussed models. Although modeled C-V results are shown for a temperature of 25°C only, a spline fit is derived for each investigated temperature: 25°C, 50°C, 75°C, 100°C, 125°C.

Once the C-V behavior is modeled, other components are added to the C-V SDD component to create a more accurate equivalent circuit model. A static series inductance and frequency dependent resistance is added to model the behavior of the electrodes of the IDC. Shunt capacitors are added to account for the capacitance between the IDC fingers along the outer perimeter of the device and the ground planes

of the CPW lines. Optimizations are completed in ADS to determine the values of these added components by matching the measured S-parameters to the simulated S-parameters of the equivalent circuit model which is shown in Figure 8-2. Optimization goals are set to minimize the differences of the measured and modeled S_{21} responses and that of the measured and modeled S_{11} responses for the frequency range of 0.5 – 10 GHz. Measured and modeled S-parameter responses resulting from the optimization are shown in Figure 8-3.

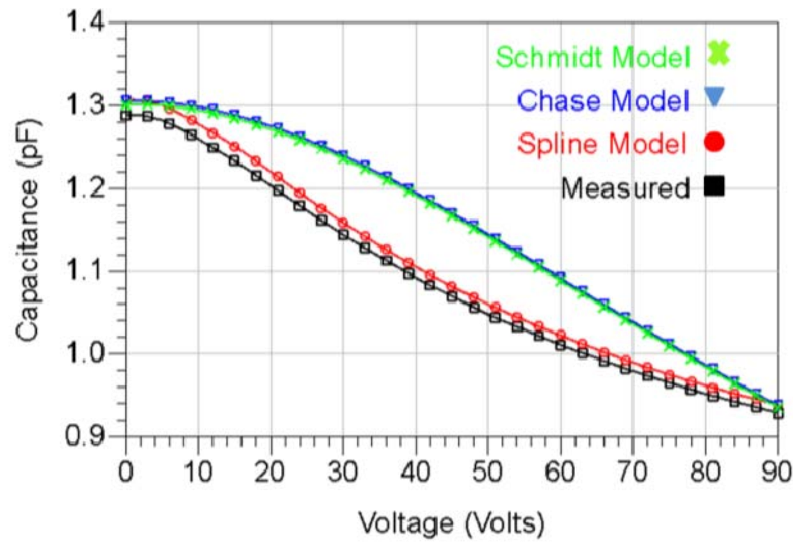


Figure 8-1: Capacitance vs. Voltage (Measured and Modeled)

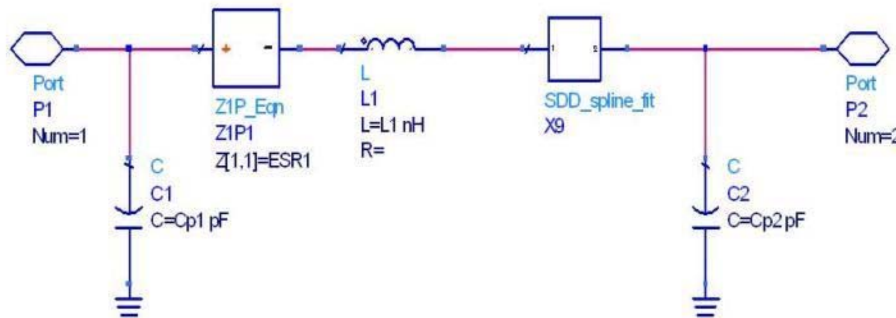
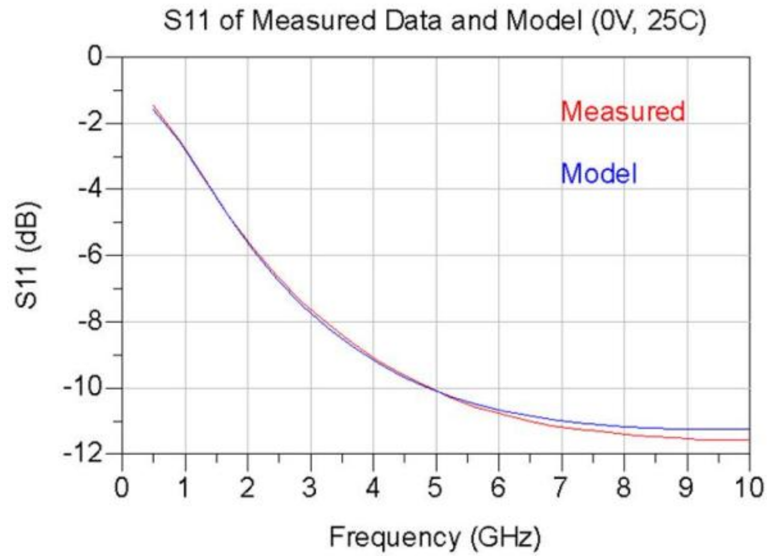
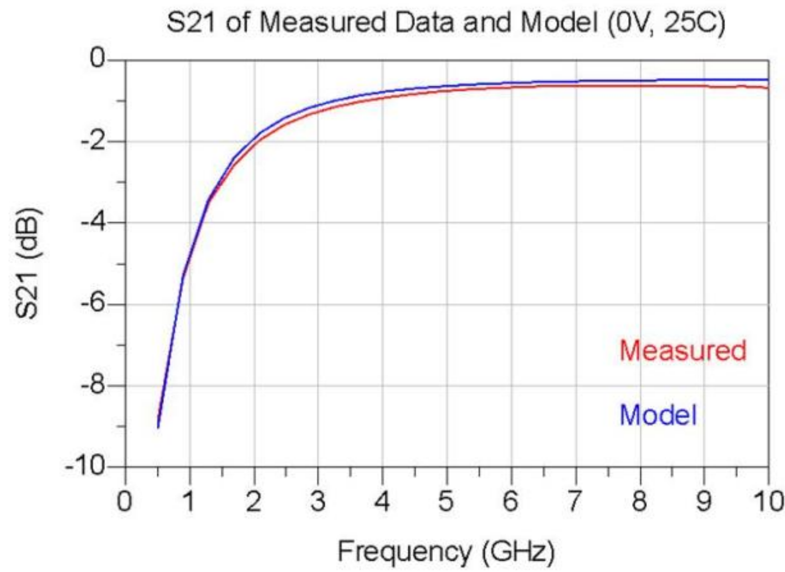


Figure 8-2: Equivalent Circuit Model of BST Varactor



(a)



(b)

Figure 8-3: Measured and Modeled S-Parameters
(a): S11 (b) S21

8.4 IMD Prediction

Harmonic balance simulations are completed in ADS to emulate two-tone measurements of the equivalent circuit model. Simulated RF tones of 1 GHz and 1.001 GHz are inserted into the model with various amplitudes similar to those used in the

actual two-tone test bench. Although the spline model yields a good fit for the C-V behavior of the BST varactors, the simulated third order IMD does not match the measured third order IMD as shown in Figure 8-4. When observing the lower input RF power range, the location of the simulated sweet-spot does not match that of the measured data. The fit improves beyond the dip at higher RF power levels over 30 dBm.

It has been documented that models should not only fit the initial parameters of interest to accurately predict the IMD behavior, but the derivatives of those parameters as well [103, 108, 109]. In light of this, the C-V spline model is revisited for further investigation. To ensure that the spline model is a good fit for the measured C-V data, the first derivatives of the measured C-V data and the spline fit are calculated and compared using MATLAB. Figure 8-5 displays the calculated derivatives and further validates that the spline interpolation is a good model for the C-V data. Therefore, studies that go beyond obtaining a good fit for the C-V data are necessary in order to accurately predict the IMD behavior of a BST varactor. In [106], it is shown that the voltage dependent conductance component of the derived model can impact the simulated IMD behavior, specifically causing a dip in the third order IMD product. Hence, the nonlinear conductance of the BST varactor is investigated.

8.4.1 Nonlinear Conductance for IMD Prediction

To account for the nonlinear conductance of the BST varactor, another SDD component is added to the equivalent circuit model. This component is placed in parallel with the spline fit SDD component and is defined by the expression:

$$G(V) = \gamma_0 + \frac{\gamma_1 / \gamma_2}{1 + \left(\frac{V}{\gamma_2}\right)^N} \qquad \text{Equation 8-6}$$

where γ_0, γ_1, γ_2, and N are fitting parameters. This expression is very similar to Equation 2-2, except that the exponent of 2 has been made adjustable in this case to allow for more flexibility when fitting the measured data. More optimizations are run in ADS to determine the fitting parameters within the G(V) expression for each temperature. By doing so, a model for the BST varactor is derived for each specific temperature that is investigated. Each model consists of a unique spline fit to model the CV behavior and a unique G(V) expression to model conductivity at each temperature. The revised equivalent circuit model for 25°C is shown in Figure 8-6. The optimized G(V) fitting parameters are displayed in Table 8-1. The shunt resistance values obtained by taking the inverse of the calculated G(V) values are plotted and displayed in Figure 8-7.

Overall, the models fit the measured data better at higher RF input power (beyond the power level in which the dip in the measured data occurs). The results of the measured and new modeled third order IMD data at 25°C are shown in Figure 8-8. The dip location in the modeled data begins to approach that of the measured data, but still does not match it exactly. This is the case for each of the models derived for the considered temperatures. This affirms that adding the nonlinear conductance component to the model is a step in the right direction.

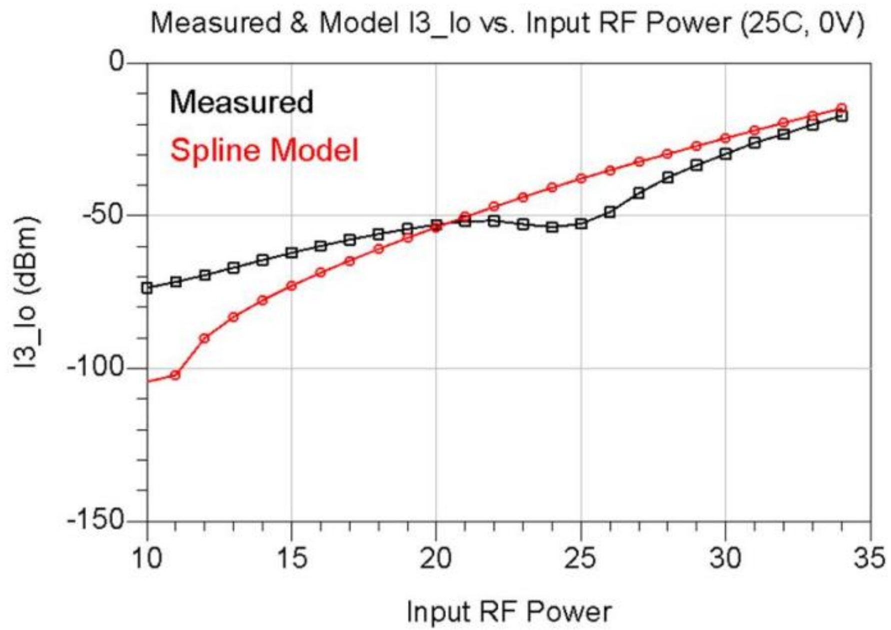


Figure 8-4: Third Order IMD (Measured and Modeled)

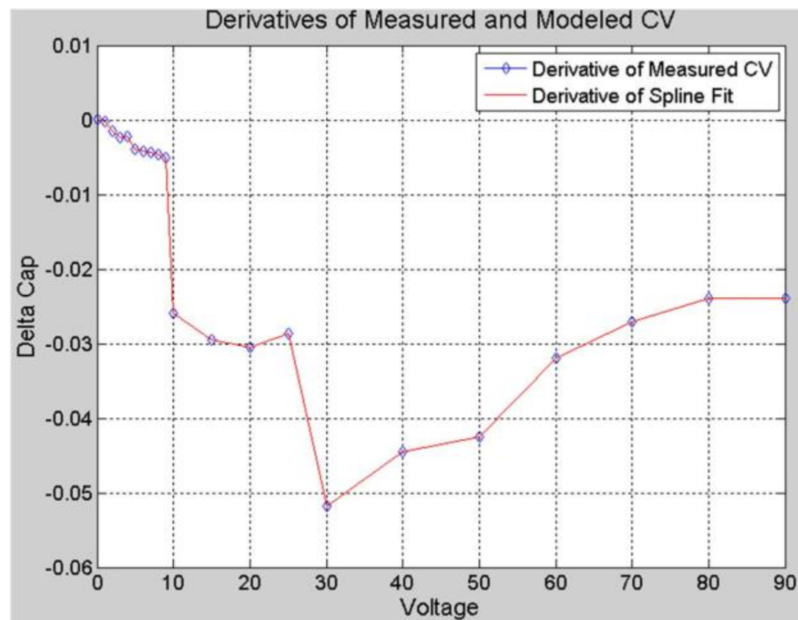


Figure 8-5: Derivatives of Measured and Modeled C-V

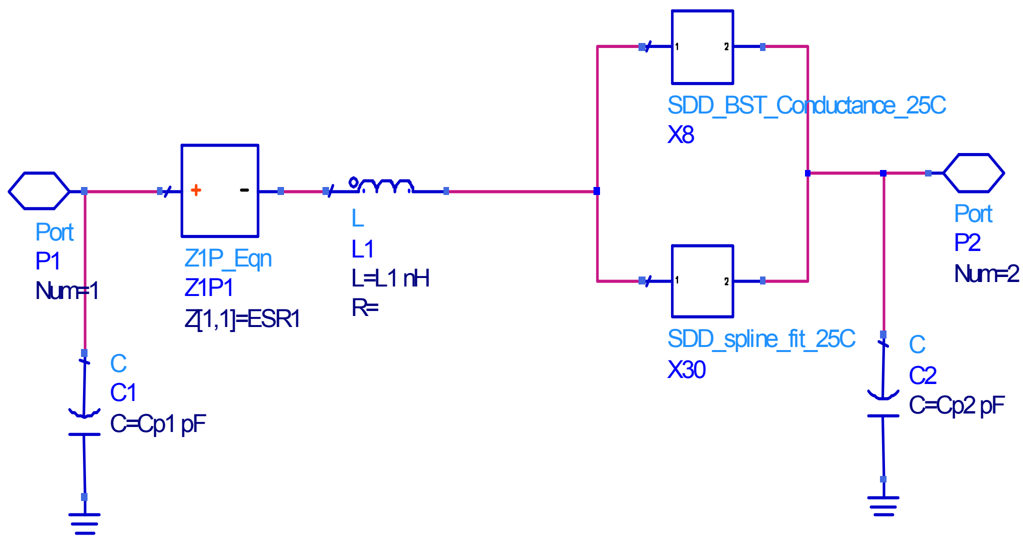


Figure 8-6: Circuit Model with Nonlinear Conductance Component

Table 8-1: Optimized G(V) Fitting Parameters

	25C	50C	75C	100C	125C
gamma_0	0.000982046	0.000929424	0.000928808	0.00131808	0.00115483
gamma_1	8.33E-05	6.91E-05	6.50E-05	2.13E-05	1.29E-12
gamma_2	0.278519	0.230305	0.234956	0.228377	0.245785
exponent	1.89686	2.31911	1.9954	2.12052	2.07743

In an effort to better understand the voltage and temperature impact on the shunt conductance, the G(V) SDD components in the revised equivalent circuit models are replaced with static resistors. Using the spline fit to model the CV behavior, optimizations are performed to fit the shunt resistances for various voltages (0V – 50V) while leaving the temperature fixed at 25°C, initially. This is done to see how the shunt resistance changes as a function of voltage for various temperatures. After fitting the resistors at 25C, more optimizations are performed to fit the resistance values over

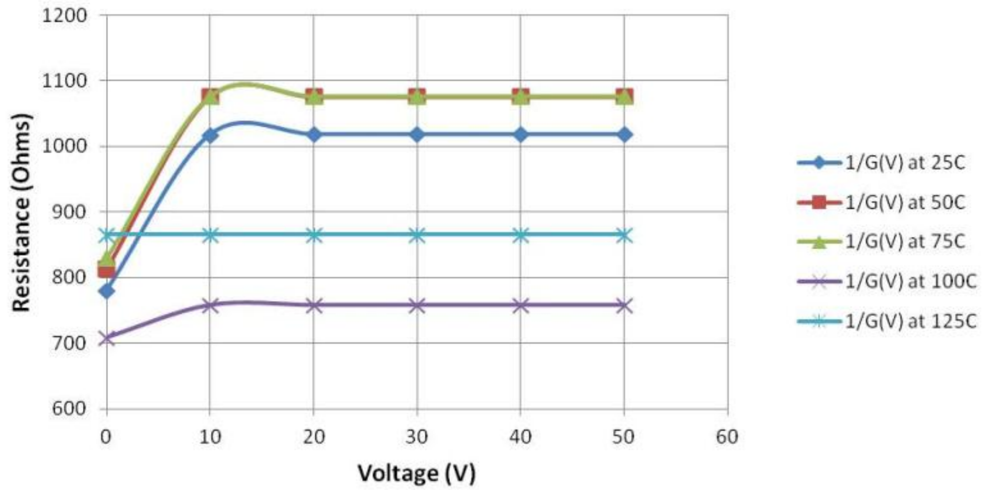


Figure 8-7: Third Order IMD (Measured and Modeled) with G(V)

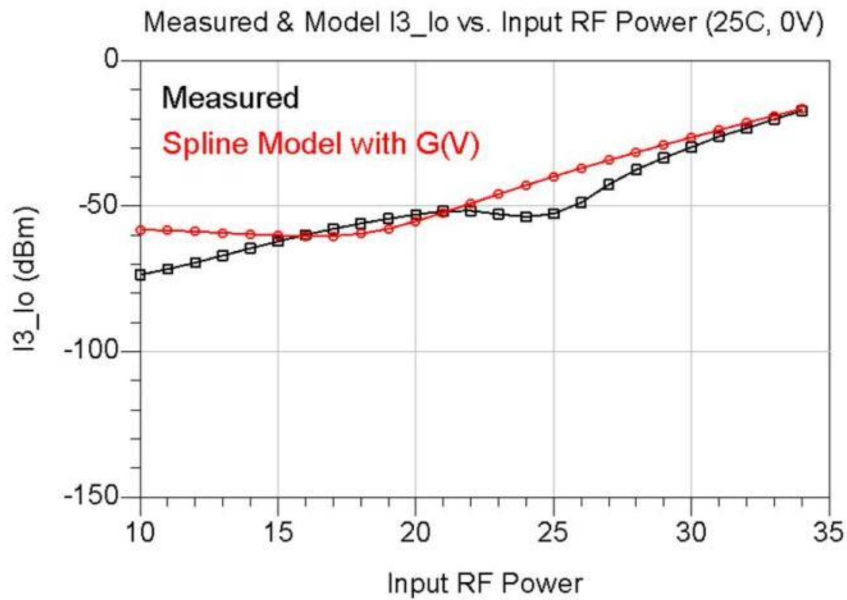


Figure 8-8: Third Order IMD (Measured and Modeled) with G(V)

voltage at fixed temperature points of 50°C, 75°C, 100°C, and 125°C. Figure 8-9 shows the optimized values for the shunt resistors for each of the voltage and temperature settings. The only temperatures that display a monotonic change in the shunt resistance with respect to the voltage are 25C, 50C, and 75C. At the other investigated temperatures (100C, and 125C), the shunt resistance value doesn't change monotonically.

The resistance values obtained from the two methods (static resistor fit and G(V) fit) do not match exactly; however they do show an overall similar trend of the resistance increasing with respect to voltage. For the temperatures in which the optimized static resistance values do not increase monotonically with respect to voltage, the G(V) expression in its current form will not be able to replicate this behavior. There appears to be another component/parameter that is not being accounted for in the G(V) expression. More work is necessary to accurately model the nonlinear conductivity with respect to temperature for BST varactors.

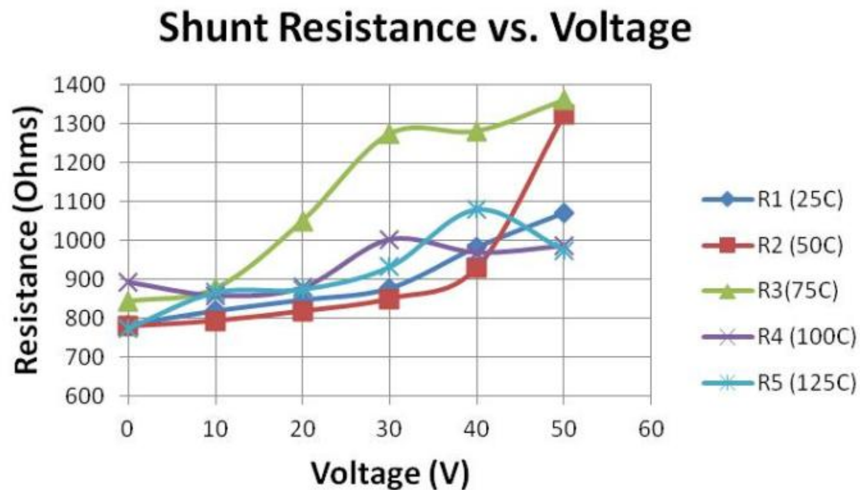


Figure 8-9: Optimized Values for Static Resistors

8.4.2 Conductance vs. Anneal Time

Using similar methods previously discussed, the effects of anneal time on the shunt conductance component of the BST varactors is investigated. Figure 8-10 shows the shunt resistance value vs. anneal time for various DC bias voltages which is extracted by ADS optimizations. Overall, the shunt resistance decreases with respect to the anneal time. This shows that the anneal time/grain size impacts the nonlinear conductivity translating to an influence of the sweet spot location in the IMD products. Therefore, in addition to temperature and voltage, the grain size could potentially be a parameter to be included in future models for describing the nonlinear conductance and accurately predicting the IMD products of BST varactors.

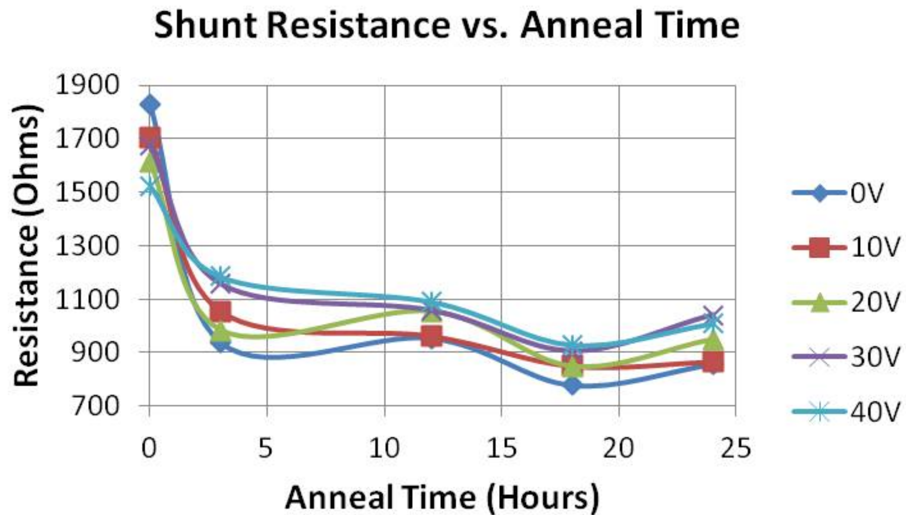


Figure 8-10: Optimized Resistance Values vs. Anneal Time

Chapter 9 Conclusion

9.1 Summary of Accomplishments

The nonlinear properties of microscale and nanoscale planar BST varactors have been investigated. The material properties of the BST thin films have been correlated to the nonlinear behavior and the post-deposition annealing treatment is proven to contribute greatly to the overall quality of the film and the tunability of the BST varactors. Post deposition annealing is also shown to contribute greatly to the intermodulation distortion generated by the BST varactors. In addition to the film properties, temperature and DC voltage have an impact on the intermodulation distortion and trends have been identified. It is also shown that a significant reduction in size can be achieved when using IDCs with nanoscale gap sizes instead of microscale gap sizes. Modeling techniques for predicting the C-V behavior have been examined; however, more work needs to be done to accurately predict the IMD products, particularly at the sweet-spot.

9.2 Future Work

From a procedural perspective, the experiments could have been performed differently to yield more precise and consistent results. For this work, materials characterization and RF measurements were done in parallel. For a particular batch of samples with films annealed for a certain time, half of those samples were used for materials characterization: XRD, TEM, AFM. The other samples from the batch were used to fabricate the BST varactors for RF measurements. Instead of carrying out experiments in parallel on different samples, perhaps the work could be repeated by using a set of samples for the materials analysis and then using the exact same set of

samples for fabricating devices for RF measurements once the materials analysis is completed.

Additionally, the grain size values extracted could have more of a statistical validation if the XRD approach could have been used. Using a parallel plate collimator of a finer mesh than that available at the time to collect the diffracted X-rays coming from the measured samples would have possibly resolved the issue of the FWHM values not changing with respect to the anneal time. Statistically this would allow for a better extraction of grain size by calculating the size of the grains within the entire section of the film that is being exposed to the X-rays rather than using TEM to zoom and measuring randomly selected grains individually.

As discussed in Chapter 8, there is still much work to be done in deriving models that accurately predict the 3rd order intermodulation distortion products for BST varactors. The nonlinear conductance component has been identified as a source for the dip observed in the third order IMD when viewed with respect to input RF power. If an expression can be derived for the conductance that is not only dependent on the DC voltage, but on the RF voltage amplitude, temperature, and grain size, it is believed that this will lead to better prediction capability of the third order IMD products. Once a more accurate model is derived, it can be used for designing RF components that contain planar BST varactors such as filters, phase shifters, tunable matching networks, and tunable antennas for frequency selective surface applications.

This work examines BST films that have been annealed for 0, 3, 12, 18, and 24 hours. It is shown that the largest change in material properties of the BST film along with the tunability and nonlinear behavior of the BST varactors occurs between the non-annealed samples and those annealed for 3 hours.

More work needs to be done to see how the film quality and RF behavior of the varactors change when the films are annealed for smaller increments: perhaps 15 – 30 minutes at a time.

The BST films observed in this work are 50/50 in composition and are also non-doped. It may be worthwhile to examine the nonlinear behavior of BST varactors produced with films of various concentrations such as 60/40 and 70/30, as these other compositions are also popular for developing tunable RF components. Additionally, nonlinear properties of varactors created with doped BST films should also be investigated as doped films have been examined in the past to increase tunability and lower losses [53]. This could possibly lead to advanced models for predicting the nonlinear behavior of BST varactors using various stoichiometries of BST that could possibly account for hysteretic behavior.

Previous research has aimed to examine the switching speed of BST films using two-tone measurement techniques with varied tone spacing [16]. The power level of the third order IMD products is observed with respect to tone spacing in an effort to see how the film is responding to RF signals at various frequencies. It would be advantageous to perform the same type of studies on BST films that have various material properties. This would allow for the examination of BST film switching speed based on roughness, grain size, and perhaps interplanar spacing.

The nanoscale BST IDCs fabricated for this research have gap sizes just below 400nm and this significantly reduces the size of the BST varactor when compared to one with microscale gaps. If the gap size of the nanoscale devices can be further reduced, this could lead to additional device miniaturization which will be advantageous for

producing tunable nanoscale front ends for carbon nanotube and nanoscale CMOS based RF applications.

Overall, the work presented here shows that there is still room and purpose for advancing the understanding of the nonlinear behavior of BST film based varactors.

List of References

1. Russer, P. and N. Fichtner, *Nanoelectronics in Radio-Frequency Technology.* Microwave Magazine, IEEE. **11**(3): p. 119-135.

2. Cha, S.N., et al., *Perspectives on Nanotechnology for RF and Terahertz Electronics.* Microwave Theory and Techniques, IEEE Transactions on. **PP**(99): p. 1-1.

3. Wong, H.S.P., et al., *Nanoscale CMOS.* Proceedings of the IEEE, 1999. **87**(4): p. 537-570.

4. Jing, H., M. Momenzadeh, and F. Lombardi, *An Overview of Nanoscale Devices and Circuits.* Design & Test of Computers, IEEE, 2007. **24**(4): p. 304-311.

5. Rutherglen, C. and P. Burke, *Carbon Nanotube Radio.* Nano Letters, 2007. **7**(11): p. 3296-3299.

6. Rouhi, N., D. Jain, and P.J. Burke, *Nanoscale Devices for Large-Scale Applications.* Microwave Magazine, IEEE. **11**(7): p. 72-80.

7. Rebeiz, G.M., *RF MEMS: Theory, Design, and Technology*. 2003, Hoboken, NJ: John Wiley & Sons. 483.

8. Ghosh, D., *Tunable Microwave Devices Using BST (Barium Strontium Titanate) and Base Metal Electodes*, in *Materials Science and Engineering*. 2005, North Carolina State University: Raleigh.

9. Gevorgian, S., *Ferroelectrics in Microwave Devices, Circuits, and Systems (Physics, Modeling, Fabrication, and Measurements)*. Engineering Materials and Processes, ed. B. Derby. 2009, London: Springer. 394.

10. Goldsmith, C.L., et al., *Performance of low-loss RF MEMS capacitive switches.* Microwave and Guided Wave Letters, IEEE, 1998. **8**(8): p. 269-271.

11. Kenle, C., et al., *Antibiased Electrostatic RF MEMS Varactors and Tunable Filters.* Microwave Theory and Techniques, IEEE Transactions on. **58**(12): p. 3971-3981.

12. Al Ahmad, M., et al. *Tuning of Barium Strontium Titanate (BST) Thin Film Materials Employing High Resistive Thin Indium Tin Oxide (ITO) Layer*. in *Microwave Conference, 2008. EuMC 2008. 38th European*. 2008.

13. Nath, J., et al., *An electronically tunable microstrip bandpass filter using thin-film Barium-Strontium-Titanate (BST) varactors.* Microwave Theory and Techniques, IEEE Transactions on, 2005. **53**(9): p. 2707-2712.

14. Victor, A., et al. *Voltage Controlled GaN-on-Si HFET Power Oscillator Using Thin-Film Ferroelectric Varactor Tuning*. in *Microwave Conference, 2006. 36th European*. 2006.

15. Sazegar, M., et al. *Compact artificial line phase shifter on ferroelectric thick-film ceramics*. in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*.

16. Mateu, J., J.C. Booth, and S.A. Schima, *Frequency Tuning and Spurious Signal Generation at Microwave Frequencies in Ferroelectric $SrTiO_3$ Thin-Film Transmission Lines.* Microwave Theory and Techniques, IEEE Transactions on, 2007. **55**(2): p. 391-396.

17. Kwang, C., et al. *X-band and Ka-band tunable devices using low-loss BST ferroelectric capacitors*. in *Applications of Ferroelectrics, 2009. ISAF 2009. 18th IEEE International Symposium on the*. 2009.

18. Uchino, K., *Ferroelectric Devices*. 2000, New York, NY: Marcel Dekker. 308.

19. Balanis, C., *Advanced Engineering Electromagnetics*. 1989, Hoboken, NJ: John Wiley & Sons, Inc. 981.

20. Du, H., *Processing, Microstructure, and Microwave Dielectric Properties of Tunable (BA, Sr)TiO_3 Thin Films*, in *Materials Science and Engineering*. 2009, Carnegie Mellon University: Pittsburgh, PA.

21. Meng, Q., Y. Kui, and Y.C. Liang. *Development of low-cost ferroelectric PLZT devices for photovoltaic power generation*. in *Sustainable Energy Technologies (ICSET), 2010 IEEE International Conference on*.

22. Wang, G.S., et al. *$PbZr_{0.5}Ti_{0.5}O_3$ thin films prepared on $La_{0.5}Sr_{0.5}CoO_3$/$LaNiO_3$ heterostructures for integrated ferroelectric devices*. in *Solid-State and Integrated-Circuit Technology, 2001. Proceedings. 6th International Conference on*. 2001.

23. Tagantsev, A.K. and V.O. Sherman. *Composite tunable materials with low loss-factor at microwaves*. in *Microwave Conference, 2005 European*. 2005.

24. Ban, Z.G. and S.P. Alpay, *Phase diagrams and dielectric response of epitaxial barium strontium titanate films: A theoretical analysis*. Vol. 91. 2002: AIP. 9288-9296.

25. Kim, D. and J.S. Kenny, *Experimental Investigations of Intermodulation Distortion in Tunable Ferroelectric Phase Shifters.* IEICE Transactions on Electronics, 2005. **E88-C**(12): p. 2310-2315.

26. Zhao, Z., et al., *Ferroelectric Phase Shifters at 20 and 30 GHz.* Microwave Theory and Techniques, IEEE Transactions on, 2007. **55**(2): p. 430-437.

27. Majumder, S.B., et al., *Sol-gel derived grain oriented barium strontium titanate thin films for phase shifter applications.* Journal of Applied Physics, 2001. **90**(2): p. 896-903.

28. Sazegar, M., et al. *Reconfigurable unit cell for reflectarray antenna based on barium-strontium-titanate thick-film ceramic*. in *Microwave Conference, 2009. EuMC 2009. European*. 2009.

29. Tombak, A., et al. *Tunable RF filters using thin film barium strontium titanate based capacitors*. in *Microwave Symposium Digest, 2001 IEEE MTT-S International*. 2001.

30. Courreges, S., et al. *Ferroelectric Tunable Bandpass Filters for Ka-Band Applications*. in *Microwave Conference, 2008. EuMC 2008. 38th European*. 2008.

31. Feng, Z., et al. *Narrowband Barium Strontium Titanate (BST) tunable bandpass filters at X-band*. in *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International*. 2009.

32. Yuliang, Z., et al. *Constraints on Efficient Control of Tunable Impedance Matching Network Based on Barium-Strontium-Titanate Thick-Film Varactors*. in *Microwave Conference, 2008. EuMC 2008. 38th European*. 2008.

33. Vicki Chen, L.Y., et al. *Analog tunable matching network using integrated thin-film BST capacitors*. in *Microwave Symposium Digest, 2004 IEEE MTT-S International*. 2004.

34. Jia-Shiang, F., et al. *A ferroelectric-based impedance tuner for adaptive matching applications*. in *Microwave Symposium Digest, 2008 IEEE MTT-S International*. 2008.

35. Scheele, P., et al. *Continuously tunable impedance matching network using ferroelectric varactors*. in *Microwave Symposium Digest, 2005 IEEE MTT-S International*. 2005.

36. Tahan, D.M., A. Safari, and L.C. Klein, *Preparation and Characterization of Ba_xSr_{1-x}, TiO_3 Thin Films by a Sol-Gel Technique.* Journal of the American Ceramic Society, 1996. **79**(6): p. 1593-1598.

37. Lu, S.G., et al., *Compositionally graded epitaxial barium strontium titanate thin films derived from pulsed laser deposition.* Materials Chemistry and Physics, 2003. **79**(23): p. 164-168.

38. York, R., et al. *Microwave integrated circuits using thin-film BST*. in *Applications of Ferroelectrics, 2000. ISAF 2000. Proceedings of the 2000 12th IEEE International Symposium on*. 2000.

39. Kumar, A., et al., *Dielectric and structural properties of pulsed laser deposited and sputtered barium strontium titanate thin films.* Materials Science and Engineering: B, 2007. **139**(23): p. 177-185.

40. Bang-Hung, T., S. Heidger, and J.A. Weimer. *Sputtered barium titanate and barium strontium titanate films for capacitor applications*. in *Applications of Ferroelectrics, 2000. ISAF 2000. Proceedings of the 2000 12th IEEE International Symposium on*. 2000.

41. Tombak, A., et al., *Tunable barium strontium titanate thin film capacitors for RF and microwave applications.* Microwave and Wireless Components Letters, IEEE, 2002. **12**(1): p. 3-5.

42. Manavlan, S.G., *Structural and Electrical Properties of Barium Strontium Titanate Thin Films for Tunable Microwave Applications*, in *Electrical Engineering*. 2005, University of South Florida.

43. Kumar, V., *Solution-Precipitation of Fine Powders of Barium Titanate and Strontium Titanate.* Journal of the American Ceramic Society, 1999. **82**(10): p. 2580-2584.

44. Eppler, A.S., et al., *Model Catalysts Fabricated Using Electron Beam Lithography and Pulsed Laser Deposition.* The Journal of Physical Chemistry B, 1997. **101**(48): p. 9973-9977.

45. Su, B. and T.W. Button, *The processing and properties of barium strontium titanate thick films for use in frequency agile microwave circuit applications.* Journal of the European Ceramic Society, 2001. **21**(15): p. 2641-2645.

46. Ries, A., et al., *Barium strontium titanate powder obtained by polymeric precursor method.* Materials Characterization, 2003. **50**(23): p. 217-221.

47. Ezhilvalavan, S. and T.-Y. Tseng, *Progress in the developments of (Ba,Sr)TiO3 (BST) thin films for Gigabit era DRAMs.* Materials Chemistry and Physics, 2000. **65**(3): p. 227-248.

48. Acikel, B., et al., *A new high performance phase shifter using* $Ba_xSr_{1-x}TiO_3$ *thin films.* Microwave and Wireless Components Letters, IEEE, 2002. **12**(7): p. 237-239.

49. Miranda, F.A., et al., *Design and development of ferroelectric tunable microwave components for Ku and K-band satellite communication systems.* Microwave Theory and Techniques, IEEE Transactions on, 2000. **48**(7): p. 1181-1189.

50. Fardin, E.A., K. Ghorbani, and A.S. Holland. *Low Cost Interdigital BST Varactors for Tunable Microwave Applications*. in *TENCON 2005 2005 IEEE Region 10*. 2005.

51. Al Ahmad, M., et al. *Tunable Low-Field Interdigitated Barium Strontium Titanate Capacitors*. in *Microwave Conference, 2007. APMC 2007. Asia-Pacific*. 2007.

52. El-Shaarawy, H.B., et al. *Characterization of ferroelectric $Ba_{0.6}Sr_{0.4}TiO_3$> thin films on different substrates for reconfigurable microwave application*. in *Microwave Conference (EuMC), 2010 European*.

53. Cole, M.W. and C. Joshi. *Fabrication and characterization of doped barium strontium titanate thin films for tunable device applications*. in *Antennas and Propagation Society International Symposium, 2000. IEEE*. 2000.

54. Kohno, T., et al. *Sputtering Deposition of $Ba_xSr_{1-x}TiO_3$ Thin Films for Microwave Waveguide Devices*. in *Applications of Ferroelectrics, 2007. ISAF 2007. Sixteenth IEEE International Symposium on*. 2007.

55. Wooldridge, I., et al., *Electrical tuning of passive HTS microwave devices using single crystal strontium titanate.* Applied Superconductivity, IEEE Transactions on, 1999. **9**(2): p. 3220-3223.

56. Price, T., et al. *Comparison of barium strontium titanate varactors on magnesium oxide and alumina substrates*. in *Wireless and Microwave Technology Conference (WAMICON), 2011 IEEE 12th Annual*.

57. Nath, J., et al. *Discrete Barium Strontium Titanate (BST) Thin-Film Interdigital Varactors on Alumina: Design, Fabrication, Characterization, and Applications*. in *Microwave Symposium Digest, 2006. IEEE MTT-S International*. 2006.

58. Ha, J.-Y., et al., *Effects of Annealing Process on Dielectric Properties of $(Ba,Sr)TiO_3$ Thin Films Grown by RF Magnetron Sputtering.* Jpn J Appl Phys, 2005. **44**(38): p. L1196-L1198.

59. Knauss, L.A., et al., *The effect of annealing on the structure and dielectric properties of $Ba_xSr_{1-x}TiO_3$ ferroelectric thin films.* Applied Physics Letters, 1996. **69**(1): p. 25-27.

60. Samantaray, C.B., et al., *Effect of post-deposition annealing on microstructural and optical properties of barium strontium titanate thin films deposited by r.f. magnetron sputtering.* Journal of Materials Science: Materials in Electronics, 2001. **12**(7): p. 365-370.

61. Laughlin, B., J. Ihlefeld, and J.-P. Maria, *Preparation of Sputtered $(Ba_x,Sr_{1-x})TiO_3$ Thin Films Directly on Copper.* Journal of the American Ceramic Society, 2005. **88**(9): p. 2652-2654.

62. Zachariasen, W.H. and E.L. Hill, *The Theory of X-ray Diffraction in Crystals.* The Journal of Physical Chemistry, 1946. **50**(3): p. 289-290.

63. Ryland, A.L., *X-ray diffraction.* Journal of Chemical Education, 1958. **35**(2): p. 80.

64. Dorset, D.L., *X-ray Diffraction: A Practical Approach.* Microscopy and Microanalysis, 1998. **4**(05): p. 513-515.

65. Cullity, B.D., *Elements of x-ray diffraction*. 1978: Addison-Wesley Pub. Co.

66. Wang, Z.L., *Transmission Electron Microscopy of Shape-Controlled Nanocrystals and Their Assemblies.* The Journal of Physical Chemistry B, 2000. **104**(6): p. 1153-1175.

67. Stoner, B.R., et al., *Characterization of bias-enhanced nucleation of diamond on silicon by invacuo surface analysis and transmission electron microscopy.* Physical Review B, 1992. **45**(19): p. 11067-11084.

68. Meyer, E., *Atomic force microscopy.* Progress in Surface Science, 1992. **41**(1): p. 3-49.

69. Binnig, G., C.F. Quate, and C. Gerber, *Atomic Force Microscope.* Physical Review Letters, 1986. **56**(9): p. 930-933.

70. Hutter, J.L. and J. Bechhoefer, *Calibration of atomic force microscope tips.* Review of Scientific Instruments, 1993. **64**(7): p. 1868-1873.

71. De Flaviis, F., N.G. Alexopoulos, and O.M. Stafsudd, *Planar microwave integrated phase-shifter design with high purity ferroelectric material.* Microwave Theory and Techniques, IEEE Transactions on, 1997. **45**(6): p. 963-969.

72. Giere, A., et al. *Coating of planar Barium-Strontium-Titanate thick-film varactors to increase tunability*. in *Microwave Conference, 2007. European*. 2007.

73. Sherman, V., et al., *Digital reflection-type phase shifter based on a ferroelectric planar capacitor.* Microwave and Wireless Components Letters, IEEE, 2001. **11**(10): p. 407-409.

74. Chase, D.R., C. Lee-Yin, and R.A. York, *Modeling the capacitive nonlinearity in thin-film BST varactors.* Microwave Theory and Techniques, IEEE Transactions on, 2005. **53**(10): p. 3215-3220.

75. Deleniv, A., et al. *Experimental Characterization of the 3rd Order Nonlinearities in Thin Film Parallel-Plate Ferroelectric Varactors*. in *Microwave Symposium, 2007. IEEE/MTT-S International*. 2007.

76. Erker, E.G., et al., *Monolithic Ka-band phase shifter using voltage tunable* $BaSrTiO_3$ *parallel plate capacitors.* Microwave and Guided Wave Letters, IEEE, 2000. **10**(1): p. 10-12.

77. Rundqvist, P., et al., *Large signal circuit model of parallel-plate ferroelectric varactors.* Journal of Applied Physics, 2006. **100**(7): p. 074101-074101-9.

78. Vorobiev, A., et al., *Silicon substrate integrated high Q-factor parallel-plate ferroelectric varactors for microwave/millimeterwave applications.* Applied Physics Letters, 2003. **83**(15): p. 3144-3146.

79. Jin, H.Z., et al., *An interfacial defect layer observed at* $(Ba,Sr)TiO_3/Pt$ *interface.* Thin Solid Films, 2003. **429**(12): p. 282-285.

80. Schmitz, S. and H. Schroeder, *Leakage Current Measurements of STO and BST Thin Films Interpreted by the "Dead" Layer Model.* Integrated Ferroelectrics, 2002. **46**(1): p. 233-242.

81. Papapolymerou, J., et al. *A Miniature Low-Loss Slow-Wave Tunable Ferroelectric BandPass Filter From 11-14 GHz*. in *Microwave Symposium Digest, 2006. IEEE MTT-S International*. 2006.

82. Pervez, N.K., P.J. Hansen, and R.A. York. *Optimization of high tunability barium strontium titanate thin films grown by RF magnetron sputtering*. in *Applications of Ferroelectrics, 2004. ISAF-04. 2004 14th IEEE International Symposium on*. 2004.

83. Delprat, S., et al., *Voltage and frequency dependent dielectric properties of BST-0.5 thin films on alumina substrates.* Microwave and Wireless Components Letters, IEEE, 2003. **13**(6): p. 211-213.

84. Cooke, B.J., J.L. Prince, and A.C. Cangellaris, *S-parameter analysis of multiconductor, integrated circuit interconnect systems.* Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, 1992. **11**(3): p. 353-360.

85. Majid, I., A.E. Nadeem, and F. e Azam. *Small signal S-parameter estimation of BJTs using artificial neural networks*. in *Multitopic Conference, 2004. Proceedings of INMIC 2004. 8th International*. 2004.

86. Shuo, W., F.C. Lee, and W.G. Odendaal, *Characterization and parasitic extraction of EMI filters using scattering parameters.* Power Electronics, IEEE Transactions on, 2005. **20**(2): p. 502-510.

87. Schutt-Aine, J.E. and R. Mittra, *Scattering parameter transient analysis of transmission lines loaded with nonlinear terminations.* Microwave Theory and Techniques, IEEE Transactions on, 1988. **36**(3): p. 529-536.

88. Pozar, D.M., *Microwave engineering*. 1997: Wiley.

89. Company, H.P., *Applying Error Correction to Network Analyzer Measurements, Application Note 1287-3*. 1999.

90. Engen, G.F. and C.A. Hoer, *Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer.* Microwave Theory and Techniques, IEEE Transactions on, 1979. **27**(12): p. 987-993.

91. DuFault, M.D. and A.K. Sharma. *A novel calibration verification procedure for millimeter-wave measurements*. in *Microwave Symposium Digest, 1996., IEEE MTT-S International*. 1996.

92. Technologies, A., *Agilent Network Analysis Applying the 8510 TRK Calibration for Non-Coaxial Measurements*. 2000.

93. Bellotti, J., et al., *Tunable Dielectric Properties of BST Thin Films for RF/MW Passive Components.* International Symposium on Integrated Ferroelectrics, 2002.

94. Tiggelman, M.P.J., et al., *Electrical characterization of thin film ferroelectric capacitors*, in *Proceedings of the 9th annual workshop on Semiconductor Advances for Future Electronics and Sensors 2006*. 2006, Technology Foundation STW: Veldhoven, The Netherlands.

95. Pedro, J.C. and N.B. Carvalho, *Intermodulation Distortion in Microwave and Wireless Circuits*. 2003, Norwood, MA: Artech House, Inc. 450.

96. Maas, S.A., *Nonlinear Microwave and Rf Circuits*. 2003: Artech House.

97. Lourandakis, E., et al. *Tunable lumped element filters with bst thin-film varactors*. in *Wireless Technology, 2008. EuWiT 2008. European Conference on*. 2008.

98. Chakraborty, T., et al. *Intermodulation distortion in wide-band dual-mode bulk ferroelectric bandpass filters*. in *Microwave Symposium Digest, 2005 IEEE MTT-S International*. 2005.

99. Chen, H., et al., *The size effect of Ba0.6Sr0.4TiO3 thin films on the ferroelectric properties.* Applied Surface Science, 2006. **252**(12): p. 4171-4177.

100. Mateu, J., et al. *Measurements and Analysis of Microwave Nonlinearities in Ferroelectric Thin Film Transmission Lines*. in *Microwave Symposium Digest, 2006. IEEE MTT-S International*. 2006.

101. Jia-Shiang, F., et al. *A Linearity Improvement Technique for Thin-film Barium Strontium Titanate Capacitors*. in *Microwave Symposium Digest, 2006. IEEE MTT-S International*. 2006.

102. Fu, J.S., et al., *Improving Linearity of Ferroelectric-Based Microwave Tunable Circuits.* Microwave Theory and Techniques, IEEE Transactions on, 2007. **55**(2): p. 354-360.

103. Fager, C., et al., *Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model.* Microwave Theory and Techniques, IEEE Transactions on, 2002. **50**(12): p. 2834-2842.

104. Seung-Yup, L., et al. *The IMD sweet spots varied with gate bias voltages and input powers in RF LDMOS power amplifiers*. in *Microwave Conference, 2003. 33rd European*. 2003.

105. Mueller, C.H., R.R. Romanofsky, and F.A. Miranda, *Ferroelectric thin film and broadband satellite systems.* Potentials, IEEE, 2001. **20**(2): p. 36-39.

106. Schmidt, M., et al. *A Thin-Film BST Varactor Model for Linear and Nonlinear Circuit Simulations for Mobile Communication Systems*. in *Applications of ferroelectrics, 2006. isaf '06. 15th ieee international symposium on the*. 2006.

107. Kozyrev, A.B., et al., *Nonlinear behavior of thin film $SrTiO_3$ capacitors at microwave frequencies.* Journal of Applied Physics, 1998. **84**(6): p. 3326-3332.

108. Pedro, J.C. and J. Perez, *Accurate simulation of GaAs MESFET's intermodulation distortion using a new drain-source current model.* Microwave Theory and Techniques, IEEE Transactions on, 1994. **42**(1): p. 25-33.

109. Maas, S.A. and D. Neilson, *Modeling MESFETs for intermodulation analysis of mixers and amplifiers.* Microwave Theory and Techniques, IEEE Transactions on, 1990. **38**(12): p. 1964-1971.

Appendices

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Ferroelectrics in Microwave Devices, Circuits and Systems Physics, Modeling, Fabrication and Measurements

Appendix A (Continued)

Series: Engineering Materials and Processes Gevorgian, Spartak 1st Edition., 2009, XX, 394 p. 236 illus.
Hardcover version
ISBN 978-1-84882-506-2

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Appendix A (Continued)

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Step Two

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Step Three

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Appendix A (Continued)

:

Hello,

I would like to reproduce some of the text and figures from my papers that were published in the WAMICON 2011 & 2012 Conference Proceedings for my dissertation. The papers are entitled, "Comparison of Barium Strontium Titanate Varactors on Magnesium Oxide and Alumina Substrates" and "Temperature and Voltage Impact on Intermodulation Distortion of Planar Barium Strontium Titanate Varactors". I am the first author of both papers. Please let me know of your approval within 2 weeks as I am planning to submit and defend my dissertation this summer.

Thanks,
Tony

Tony Price
RF Microsystems Research Group

University of South Florida
4202 E. Fowler Avenue, ENB-118,
Tampa, FL, 33620
Office: ENB 412
Phone: (404) 291-3506

Notes/Comments

7 attachments

pic16512.jpg
23K

Appendix B: XRD Optics and Settings

B.1 Incident Beam Optics (Powder Diffraction Method)

The following options are selected for the incident beam optics on the XRD system when using the powder diffraction method:

- PreFIX Module: X-ray mirror Cu
- Divergence slit: slit fixed 1/2 °
- Anti scatter slit: none
- Mask: Inc. Mask fixed 10mm
- Mirror: None
- Monochromator: None
- Beam attenuator: None
- Filter: None
- Soller Slit: 0.04 rad

B.2 Diffracted Beam Optics (Powder Diffraction Method)

The following options are selected for the diffracted beam optics on the XRD system when using the powder diffraction method:

- PreFIX Module: Programmable Receiving Slit (PRS)
- Anti scatter slit: slit fixed 1/2 °
- Receiving slit: 0.25mm
- Filter: Nickel
- Mask: None
- soller slit: 0.04 rad
- Monochromator: None
- Collimator: None

Appendix B (Continued)

- Detector: Mini Prop. Large Window
- Beam attenuator: None

B.3 Scanning Specifications (Powder Diffraction Method)

The following scanning specifications are used for the powder diffraction method:

- Scan range: 20° – 70°
- Time per step: 5 seconds
- Scan speed: 0.012°/sec.
- Total Scan Time: 1:09:30

B.4 Incident Beam Optics (Grazing Incidence Method)

The following options are selected for the diffracted beam optics on the XRD system when using the grazing incidence method:

- PreFIX Module: X-ray mirror Cu
- Divergence slit: slit fixed 1/8 degree
- anti scatter slit: none
- Mask: Inc. Mask fixed 10mm
- Mirror: default Inc X-ray mirror Cu (MRD)
- Monochromator: none
- Beam attenuator: Ni 0.125mm automatic, usage: at pre-set intensity
- filter: none
- soller slit: none

Appendix B (Continued)

B.5 Diffracted Beam Optics (Grazing Incidence Method)

The following options are selected for the diffracted beam optics on the XRD system when using the grazing incidence method:

- PreFIX Module: Parallel plate collimator 0.27°
- anti scatter slit: none
- Receiving slit: none
- Mask: none
- soller slit: 0.04 rad
- Monochromator: None
- Collimator: Default 0.27°(thin film)
- Detector: Mini Prop. Large Window
- Beam attenuator: None

B.6 Scanning Specifications (Grazing Incidence Method)

The following scanning specifications are used for the grazing incidence method:

- Omega = 0.6° (This is fixed throughout the entire scan when using the grazing incidence method.)
- Scan range: 20° – 70°
- Time per step: 5 seconds
- Scan speed: 0.012°/sec.
- Total Scan Time: 1:09:30

Appendix C: Detailed Fabrication Recipes for Microscale BST IDCs

C.1 Cleaning Samples

- Label (scribe) the back of all samples with series and sample number before using
- Clean with acetone and methanol, then N2 dry
- Dehydration bake on hotplate at 115°C for 5 minutes. Let it cool for a couple of minutes before spin-coating with resist.

C.2 Depositing BST

- BST Deposition at UCF (AJA ATC 1800 Sputtering System)
- Deposition Pressure: 5mT
- Base Pressure: ~1.5e-7T
- Argon/oxygen ratio: 20:2.5
- RF Power: 200 Watts (ramped up at 5W every 30 seconds)
- Temperature: 400°C
- Annealing: Ramp up to 900°C at 10°/minute
- Anneal at 900°C in oxygen.using a Fisher Scientific . Various annealing times are used for this work.
- Let the oven cool down on its own (no ramp rate set for cool down). It takes about 3 hours to cool down.
- An extra silicon sample is included with each run when depositing BST. This sample is not annealed and used to estimate the thickness of the BST film.

C.3 Patterning 1827 Positive Resist

- Be sure to put down black colored dicing saw tape on Quintel chuck if using transparent substrates to avoid reflective scattering while exposing the resist.
- Spin HMDS at 3000rpm for 30 seconds.
- Spin 1827 at 3000rpm for 30 seconds.
- Bake on hotplate at 90oC for 90 seconds.
- Expose for 10 seconds on Quintel mask aligner (lamp intensity was at 18.5 mW/cm2 when recipe was derived)
- Develop for 30 - 40 second (or longer if necessary) in MF319 or AZ-726.
- Descum for 2 minutes in O2, using brown box asher at 50-75W (It's difficult to tune right at 50W). This will remove 1827 resist at 82nm/min. Or the plasma therm can be used: O2, flow rate of 99 sccm, pressure of 300 mT, power of 75 Watts.
- No Hardbake, resist etches at ~304 nm/min in DRIE.
- Initially 1813 resist was being used when doing wet etch, but it was not thick enough to protect the films during the DRIE process. Therefore 1827photoresist was used for patterning BST with DRIE.

C.4 Determining BST Thickness

- Pattern 1827resist on the Si/BST sample (the one that was not annealed).
- Submerge the sample in 10:1 BOE to etch the BST film.
- Observe the sample while it is in the BOE. When it appears that the BST has been etched (you should be able to clearly see the silicon substrate in the areas in which there is no photoresist), take the sample out of the BOE. It could take anywhere from 5 – 10 minutes to etch through the non-annealed BST using 10:1 BOE, depending on the thickness.
- Place it in DI water for 1min and then N2 dry.
- Observe the sample using a microscope to ensure that the BST film has been removed from the field.
- Rinse the sample with acetone and methanol to remove the 1827 resist. If that doesn't work, then use 1165 resist remover at 80oC for ~20 minutes.
- Determine thickness of the non-annealed BST using a profilometer. (Measurement A)
- Etch the BST using NREC's Alcatel DRIE system with recipe listed below

C.5 Pyrex Recipe

- RF 2800W (13.5MHz)
- Bias: 550W
- C4F8: 17sccm
- CH4: 13 sccm
- Argon: 100sccm
- Temp: -20C

- Substrate distance from source: 140mm
- Once the samples have patterned 1827 on them, measure the thickness of the patterned resist using a profilometer. (Measurement B)
- Run the pyrex DRIE recipe for 1-2 min and then take more profilometer measurements. The step that is being measured in this case consists of resist and patterned BST. (Measurement C)
- Strip the resist from the sample by putting it in the brown box asher (up to 30 min) or by using the plasma therm.
- Take more profilometer measurements. This time, only the step height of the BST is being measured since the resist has been removed. (Measurement D)
- Use etch rate = Measurement D / experimental etch time to calculate the etch rate of the BST film. Calculate the time required to etch through the total film by using total etch time = Measurement A/etch rate. (Based on film thickness determined from silicon sample)
- Calculate the thickness of the resist that was left on the sample after the DRIE etch by using Measurement C – Measurement D.
- Calculate the etch rate of the resist by using (Measurement B – (Measurement C-MeasurementD)) / experimental etch time.
- Once the total etch time required is known, use this time to etch the BST films on the remainder of the samples.
- Strip the remaining resist using oxygen plasma 150 Watts for 10minutes.

- Side notes: Films grown on different substrate materials will have different characteristics and will etch at different rates. Also, if the annealing conditions are different, the etch rates will vary. Therefore, the above procedure needs to be carried out for each substrate material used along with each annealing condition used.
- Etches BST on Alumina (annealed for 12 hours) at 75nm/min (calculated from Series A)
- Etches 1827 resist at 304nm/min
- Etches alumina substrate at 145nm/min
- Series A average BST film thickness was ~550nm. I used an etch time of 7.5 min, but I think that the samples were slightly over-etched.
- Since the resist has been exposed to plasma during the DRIE process, it will be very difficult to remove with acetone and methanol. This is why it is best to put it in the asher to get rid of any resist residue.

C.6 Patterning 3000PY (NR-1) Resist

- Spin coat 3000PY at 6krpm for 50 seocnds (resist thickess: ~2.5um)
- Pre-exposure bake at 155C for 90 seconds
- Expose for 11 seconds (lamp intensity on Quintel was down to 18.8 mW/cm2 at the time),
- Bake at 110C for 60 seconds
- Develop in RD6 for 7-10 seconds
- Descum for 2 minutes in O2 at 75W in for 2 min

Appendix C (Continued)

C.7 Metal Deposition (Using Thermal Evaporator)

Metal	Rate	Current	Displayed Thickness	Actual Thickness
Cr	0.3 – 0.4 A/s	~50Amps	0.15kA or 15nm	
Au	0.4 – 0.5 A/s (0-100A) 3 A/s (100 – 1000A) 6.5 A/s (1000 – max)	190 Amps 210 Amps 220 Amps	5.3kA or 530nm 10.06 kA or 1um 12kA or 1.2um	4.7kA or 400nm 7.8kA or 780nm 9.1 kA or 912nm

C.8 Lift Off

- Lift-off 3000PY and excess metal using RR41 resist remover at temperature of 100 C for at least 20 minutes.
- USB clean as needed (up to 10 – 15 minutes) while samples are submerged in RR41.

Appendix D: Fabrication Recipe for Nanoscale BST Varactors

D.1 Sample Preparation

- Spin-coated undiluted ZEP at 4krpm for 45 seconds
- Bake on a hotplate at 180°C for 3 minutes
- Let the sample cool briefly
- Spin-coat with diluted Espacer (2:1) at 900rpm for 45 seconds
- Changed spin recipe to 2krpm for 5 seconds to get rid of edge beads and excess resist in the corners of the sample
- Write the pattern using JEOL 9300 FS

D.2 Develop

- Dipped in Xylenes to break E-spacer
- Rinsed with IPA
- USB clean in H2O for 30 seconds to remove E-spacer residue
- Tilt the beaker slightly and insert the sample, face up into the beaker. Use the tweezers to hold on to it while developing. Develop the sample in Xylenes for 1.5 – 2 minutes in 30 second increments to ensure ZEP resist is not over-developed.
- Immediately after developing, rinse the sample with IPA.
- Dry with N2.
- Descum at 165 mT using 25W, and 25sccm of O2 for 20 seconds

D.3 Metal Deposition

- 15nm of Cr is deposited by E-beam evaporation
- 125nm of Au is deposited by E-beam evaporation

D.4 ZEP Lift-Off

- Heat anisol in a glass beaker on a hotplate up to 70 deg C. Once it is at temperature, submerge the sample for 15min and observe. If there is still residue, put it back in the beaker for a few minutes at a time.
- When it looks good, put it in the ultrasonic bath for up to 10min.
- Rinse the sample with IPA.
- Never spray this with water. This could damage the nanoscale features in the EBL resist.

Appendix E: MATLAB Code for Spline Fit Coefficients

```
%%% Tony Price
%%% Capacitance-Voltage Curve Fit Using Cubic Spline
Interpolation
%%% USF/UCF BST films Series C


%%%positive voltage only
clc; close all; clear all;
format short e;

%%%%%Sample C3 Device R4C3 5F2P at Temperature: 25C
voltage = [0 2 5 10 15 20 25 30 40 50 60 70 80 90];
Cap_pF=[1.288 1.288 1.282 1.260 1.234 1.204 1.173 1.144 1.092
1.048 1.011 0.979 0.952 0.928];

% Data at Temperature 50C
% Cap_pF=[1.221 1.220 1.214 1.198 1.178 1.155 1.132 1.109 1.065
1.027 0.994 %0.965 0.940 0.918];

% Data at Temperature 75C
%Cap_pF=[1.161 1.160 1.156 1.144 1.130 1.112 1.094 1.076 1.041
1.009 0.981 %0.955 0.933 0.913];

% Data at Temperature 100C
%Cap_pF=[1.106 1.106 1.102 1.094 1.084 1.070 1.057 1.043 1.016
0.989 0.966 %0.944 0.924 0.906];

% Data at Temperature 125C
%Cap_pF=[1.059 1.058 1.056 1.051 1.043 1.033 1.024 1.013 0.991
0.969 0.950 %0.932 0.915 0.899];


figure(1);
plot(voltage, Cap_pF);

xlabel('Volts');
ylabel('Capacitance (pF)');
title('CV Measured and Fitted Data');
legend('Measured Data', 'Fitted Data', 'Gaussian_CV', 'York CV');
grid on;

%%% Calcultating 1st derivative of measured data and padding with
extra %element in array%%%
```

Appendix E (Continued)

```
dev_meas=diff(Cap_pF);
last_ind = find(dev_meas, 1, 'last');
last_element = dev_meas(last_ind);
new_dev_meas = [dev_meas, last_element];


%%%%Plotting derivatives
figure(2)
plot(voltage, new_dev_meas);
xlabel('Volts');
ylabel('1st derivative of Capacitance');
title('Derivatives of Measured Data');
grid on;


%%%Spline fit
%%%define smaller increments for voltage
spline_val = spline(voltage,Cap_pF);
[breaks,coefs,l,k,d] = unmkpp(spline_val);
spline_CV_fit=ppval(spline_val,voltage);

figure(3)
plot(voltage,Cap_pF,'o',voltage,spline_CV_fit);
legend('Measured CV', 'Spline Fit');
grid on

%%%Coefficients to ADS%%%%
%%% This section of code assigns variable names to the calculated
%%% coefficients from the MATLAB spline fit and places them into
a text
%%% file which is later used to insert the coefficients into an
ADS
%%% schematic for modeling

siz = size(coefs);   %size of coefs matrix, row x column

row = siz(1); % number of rows
column = siz(2); % number of columns

for x = 1:column  % assigns variables A, B, C, or D to columns
1,2,3,and 4
    if x==1
        var = 'A';
    elseif x==2
        var = 'B';
```

Appendix E (Continued)

```
elseif x==3
        var = 'C';
    elseif x==4
        var = 'D';
    end


for y = 1:row  %assigns row numbers to variable name
        varnam = strcat(var,int2str(y)); % concatenates letter
and number assignments (i.e. A1)
        varcnam = strcat(varnam,'=',num2str(coefs(y,x))); %
assigns variables to coefs in the form, i.e. A1=2

foldername= 'Coeffs'; % name of text file
dest_dir='C:\Documents and Settings\tsprice\My Documents\MATLAB';
% directory text file is saved in
  dest_filename = char(strcat(dest_dir,'\',foldername, '.txt'));
% concatenates destination and file name for complete directory

dlmwrite(dest_filename, varcnam,'delimiter', '', 'newline', 'pc',
'-append', 'roffset', 0); % saves variable to text file


    end


end

%%% Calcultating 1st derivative of Spline Fit and padding with
extra element in array%%%
spline_dev=diff(spline_CV_fit);
last_ind_spline_dev = find(spline_dev, 1, 'last');
last_element_spline_Dev = spline_dev(last_ind_spline_dev);
new_spline_dev = [spline_dev, last_element_spline_Dev];

figure(4)
plot(voltage, new_dev_meas,'bd-', voltage, new_spline_dev,'r');
grid on
legend('Derivative of Measured CV', 'Derivative of Spline Fit');
xlabel('Voltage');
ylabel('Delta Cap');
title('Derivatives of Measured and Modeled C-V')
```

About the Author

Tony Price, a native of Flint, MI, earned his B.S. in Electrical Engineering from Clark Atlanta University in 2004. He began working with the Wireless and Microwave Research group in 2006 after receiving his M.S. from USF. As a Ph.D. candidate in the Electrical Engineering Department at USF, he worked in conjunction with the Center of Nano-scale Materials User Facility at Argonne National Laboratory. His research involves the application of ferroelectric thin films to fabricate and model tunable RF devices. Tony is a recipient of the National Science Foundation Bridge to the Doctorate Fellowship, the NSF Graduate Research Fellowship, the NACME Alfred P. Sloan Fellowship, and the McKnight Doctoral Fellowship.