A low-power minaturised intracranial pressure monitoring microsystem

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Abstract

Area and available energy are two opposing factors in the design of implantable biosensors, e.g. neural stimulators and bio-fluidic pressure sensing systems. On the one hand, the device should be small enough to be seamlessly assimilated to the body environment. On the other hand, the available power sourced by an on-board battery drops proportionally with the size of the implant. Moreover, implantable devices are preferred to operate on a battery-free mode for leaking toxic chemicals of the battery may result in life threatening health conditions. Also, the life-time of the implant will be determined by that of the battery whose extension demands battery replacement by means of costly surgical procedures. Thus, other energy sources such as RF power scavengers or fuel cells are considered an optimal solution as power sources. In such cases, however, the inverse relationship between the available power and the size of the implant is more pronounced making design of chronic non-battery-operated implantable systems one of the most stringent of engineering problems.

The ultimate goal of this work is realisation of a fully implantable chronic intracranial pressure (ICP) monitoring system. Due to the required mm-scale form factor of the implantable device, the available power is scarce. This calls for investigation of new circuit and sensor integration techniques to decrease the total power consumption of the system down to a few hundreds of nano watts. So the main focus of this work is design of an ultra-low power integrated circuit (IC) for measuring ICP. Power consumption minimization of the sensing system proposed in this work paves the way for integration of an RF-power scavenger or biological fuel cells. The proposed sensing system also takes full advantage of Invensense MEMS-CMOS process to heterogeneously integrate the sensor and interface. This integration type requires no post-processing and results in sub-pF sensor-interface parasitic interconnection capacitance C_p which is an order of magnitude smaller than previously reported C_p's.

Since energy-efficiency is of main concern, the minimum energy consumption for maintaining a certain signal to noise ratio (SNR) is analytically calculated and compared for two energy-efficient sensor front ends, namely the switched-capacitor (SC) capacitance-to-voltage converter (CVC) and the successive approximation register (SAR) capacitance to digital converter (CDC). The comparison reveals for small values of C_p and for low-to-moderate SNRs, the SAR CDC outperforms the SC CVC in terms of power consumption. Heterogeneous integration of sensor and CMOS electronics results in only 720fF of C_p which enables direct SAR capacitance to digital conversion. Correlated double sampling (CDS) is also integrated into the proposed SAR switching scheme to combat $1/f$ noise and the input referred offset voltage of the comparator.

The proposed system was fabricated in Global Foundaries 0.18μm CMOS process and the entire pressure sensing system measures $2.2 \times 2.6 \times 0.4\text{mm}^3$ in size, consumes 130nW at 650Hz sampling rate and performs 12-bit digitization with >0.2% sensor-electronics combined non-linearity over 520mmHg pressure range.

Declaration

This is to certify that

1. the thesis comprises only my original work towards the M.Phil.,
2. due acknowledgement has been made in the text to all other material used,
3. the thesis is fewer than 100,000 words in length, exclusive of tables, maps, bibliographies and appendices.

Mohammad Meraj Ghanbari

Date

"Recite in the name of your Lord who created; created man from a clinging substance. Recite, and your Lord is the most Generous; Who taught by the pen; taught man that which he knew not."

96:1–5

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CHAPTER 1

Introduction

1.1 Intracranial pressure

CEREBRAL blood flow (CBF) must be maintained at a constant level (∼50 mL of blood per 100 g of brain tissue per minute [Cipolla 2009]) to ensure a sustained delivery rate of Oxygen and other nutrients to brain cells. Low levels of CBF results in irreversible brain ischaemia, and in turn permanent disability or death. A well-developed autoregulation mechanism exists to regulate CBF in the brain for a wide range of cerebral perfusion pressure (∼60–160 mmHg). Analogous to Ohm's law, CBF is defined by

$$CBF = \frac{CPP}{CVR}, \tag{1.1}$$

where CPP is cerebral perfusion pressure, and CVR is cerebrovascular (flow) resistance. Cerebral autoregulation counteracts CPP variations by modulating CVR accordingly which is done through dilation and constriction of cerebral vessels in response to respectively decreased and increased CPP. As a result, CVR tracks CPP, and CBF remains relatively constant. CPP, however, may depart the autoregulatory range of the brain for various reasons such as traumatic brain injury. In the case of traumatic brain injury, due to swelling of the brain, intracranial pressure (ICP), the pressure of cerebrospinal fluid (CSF), increases significantly which results in a proportional decrease to CPP because for high levels of ICP

$$CPP = MAP - ICP, \tag{1.2}$$

where MAP is the mean arterial blood pressure. So, elevated levels of ICP (>20 mmHg) indirectly slows down CBF and results in life-threatening brain ischaemia. Thus, *continuous* ICP monitoring followed by external drainage of CSF in case of raised ICP is recommended after all medium to severe head injuries.

Precision continuous ICP monitoring may help physicians in early diagnosis and treatment of normal pressure hydrocephalus (NPH). Due to common symptoms, NPH in its early stages is often misdiagnosed with Alzheimer's disease and

dementia. However, unlike Alzheimer's disease, NPH-caused mental disorders are reversible. NPH is due to brain losing its ability to control excess accumulation of cerebrospinal fluid. As a result, ICP elevates steadily. Since, the elevation rate of ICP is small in this case, lateral ventricles adapt and expand themselves to decrease intracranial pressure and hold it in a semi-normal range (<20 mmHg). Enlargement of lateral ventricles translates to proportional reduction in the grey matter and thus mental disorders. At this stage, abnormal enlargement of ventricles detected by brain medical imaging can hint at NPH. Continuous monitoring of ICP wave forms, however, can detect minuscule variations of ICP and predicts links between the observed symptoms and NPH at the onset. Manual drainage of ICP can then be practiced to avoid enlargement of ventricles and loss of neurons. In addition to traumatic brain injury and NPH, continuous monitoring of ICP can also help early diagnosis of tumour development since in this case added mass of the tumour leads to detectable intracranial hypertension.

1.2 ICP monitoring methods

As discussed above, similar to blood pressure, ICP is a critical indicator of a person's health. For a supine adult, ICP is normally measured 7-15mmHg and elevated levels of ICP above 20mmHg are considered abnormal which potentially lead to life-threatening brain ischaemia if not detected and treated appropriately.

According to the Association for the Advancement of Medical Instrumentation (AAMI) [Bratton 2006], an ICP monitoring device should have a pressure range of 0–100 mmHg (relative to atmospheric pressure), $\pm$2 mmHg accuracy in the range of 0–20 mmHg, and a maximum error of 10% in the range of 20–100 mmHg. Furthermore, ICP waveforms can have frequency components as high as 15 Hz [Czosnyka 2004]. This mandates sampling rates of greater than 30 Hz. For better synthesis, higher sampling rates are common [Eide 2010]. No minimum detectable pressure is prescribed by AAMI, however, to meet the accuracy requirement, pressure resolution should be better than 4 mmHg. These requirements along with targeted specifications are listed in Table 1.1.

The least invasive ICP measurement technique is known as Lumbar puncture. The measurement can be done at bed side where the patient lies in a fetal position. A needle is inserted in the spinal cord to allow CSF to flow into a simple manometer. Lumbar puncture is the least accurate ICP monitoring method and has an inherent limitation on the number of measurements taken per day making it inadequate for continuous monitoring [Bratton 2006].

Intraventricular catheter is the most invasive method with high risk of infec-

Table 1.1: Standard and targeted requirements of ICP monitoring devices

	Range [mmHg]	Accuracy [mmHg]	Resolution [mmHg]	BW [Hz]	Power [uW]
Standard	0–20 20–100	±2 10%	<4	>30	N/A
Target	0–(100,200)	±2	1–4	50	<1

tion, but it is known as the golden reference in term of accuracy [Bratton 2006]. This method requires guiding a sub-cm scale catheter into the ventricles to allow cerebrospinal fluid to flow into a manometer. Consequently, it allows drainage of ICP on the fly for relief of ICP. Its application, however, is limited for the case of traumatic brain injury when placement of catheter in ventricles is challenging. Also, because of high risk of infection it is rarely used for chronic measurements.

In-situ methods of continuous ICP monitoring include fiber-optic catheter tip transducer (e.g. Integra® Camino® [Integra® Camino 2016]) and microchip transducer (e.g. ICP Express® Codman [ICP Express® Codman 2016]). For these methods similar to insertion of intraventricular catheter, skull is drilled and a catheter is guided inside the cranium. The difference is the catheter used in these methods measures a few mm in diameter. The catheter is connected to an external readout device during measurement and ICP therapy. Because the cranium is exposed, infection rate escalates (>∼%5–15) hindering prolonged (in the order of months) continuous ICP measurement. Furthermore, because of the sensitivity of catheters to movement and elevation, the mobility of patients is strictly limited for available methods.

Moreover, the difficulty of ICP measurement has limited its applications only to emergency conditions, e.g. traumatic brain injury. In fact, the correlation between ICP waveforms and common non-emergency symptoms, e.g. headache, is not well studied due to lack of a simple technique capable of prolonged continuous ICP measurement in a normal medium other than intensive care units.

The ultimate goal of this work is design of an implantable pressure sensing system to enable continuous intracranial pressure monitoring while addressing the issues described above. The final design will include an RF power scavenging circuitry for power/data transmission. Nonetheless, as the first step this work focuses only on the sensing system, that is the sensor transducer and interfacing circuitry. Target sensor specifications are listed in Table 1.1. Note that maximum power consumption of the interface is bound to 100 nW to allow operation of the

device under low energy efficiency of inductive/RF power transfer. It deserves mention that piezoelectric ultrasound wireless power transfer is a more attractive solution for this application implantable medical devices (IMDs) because in tissue the attenuation of ultrasound waves compared to RF waves is considerably smaller; thanks to slower speed of sound to electromagnetic waves in tissue. Lastly, the device should measure <1 mm in thickness to enable implantation in the subarachnoid space [Libicher 1992].

1.3 List of publications

Journal article

M. M. Ghanbari, J. M. Tsai, A. Nirmalathas, R. Muller and S. Gambini, "An Energy-Efficient Miniaturized Intracranial Pressure Monitoring System," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 720-734, March 2017.

International conference

M. M. Ghanbari, J. M. Tsai and S. Gambini, "An energy-efficient heterogeneously-integrated capacitive pressure sensing system," *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Atlanta, GA, 2015, pp. 1-4.

1.4 The organisation of the thesis

As discussed earlier, the small form-factor of the device imposes tight restrictions on the power consumption of the system. Thus, the sensing system needs to be as energy efficient as possible to maximize the lifetime of the implant. Therefore, special attention is paid to energy efficiency of the system. For ultra-low power pressure sensing applications, capacitive sensors are attractive mainly because of their dynamic-only power consumption, as opposed to their resistive counterparts for which a constant flow of charge must be present during sensor readout.

Chapter 2 presents the proposed concept of holistic noise power optimisation for sensor interfaces. The application of the proposed optimisation technique enables quantitative benchmarking of available sensor interface architectures with respect to their energy efficiency. Furthermore it reveals that minimizing power consumption of sensor interfaces inevitably requires minimizing sensor-interface parasitic interconnection capacitance C_p.

The entire pressure sensing system can be divided into two main domains, namely mechanical and electrical. Traditionally, these two domains are realised

independently and then interconnected to form the final system. We, however, find that heterogeneous integration of the two domains results in minimal C_p. It also minimizes integration and packaging efforts to zero by taking full advantage of standard MEMS-CMOS process. On-chip sensor fabrication is not necessarily flawless, though. Unlike high quality sensors available in the market, on-chip sensors need to be carefully designed from geometrical aspects to obtain the highest sensitivity (and if possible linearity). Performance of such on-chip sensors is severely prone to process variations; a drawback which requires certain considerations in designing the sensor interface. Chapter 3 deals with the design and simulation of the sensor in the proposed heterogeneously integrated chip.

The design of the capacitive sensor requires an extensive study of deflection theory of plates and membranes. As there is no closed-form solution to the deflection of rectangular membranes, numerical methods, e.g. finite element methods, using MATLAB or other software applications should be used to solve the deflection equations with a reasonable accuracy.

In chapter 4, implementation considerations of the electronics is presented. Sensor nonlinearity and power consumption simulation results are presented. To bypass saturation of the interface due to process variations, programmable full-scale range is incorporated. Moreover, novel low-leakage t-switches and layout techniques used to enhance interface nonlineairty are also presented in this chapter.

Measurement results of the fabricated chip are presented in Chapter 5 followed by conclusions drawn in Chapter 6.

CHAPTER 2

Noise power optimisation

Miniaturised pressure monitoring systems have been under active research for biomedical applications [Chen 2014, Sosa 2015, Deng 2015]. Yet, choosing the right sensor interface architecture for ultra low power applications is not evident by surveying the state-of-the-art since a significant number of capacitive sensor interfaces reported in literature are designed for energy-relaxed industrial applications [Chun 1985, Watanabe 1986, Matsumoto 1987, Kondo 1989, Cichocki 1990, Toth 1992, Yamada 1992, Goes 1996, Toth 1996, Yamada 1997, Wang 1998, Li 2000, Li 2002, George 2006, George 2007, Chiang 2008], and there are few which focus on low-power designs [Tan 2012, Tan 2013, Nizza 2013, Omran 2014, Scotti 2014, Oh 2014, Oh 2015, Trung 2015, Wang 2015, Jung 2015, Wang 2016]. Furthermore, none of the reported interfaces is a *sensor-specific* design. In fact, they are all general purpose sensor front ends. But, in this work, there is a great deal of flexibility in co-designing the sensor and the interface. Co-designing sensor and interface, as discussed in Chapter 3, relaxes some design requirements of the interface. Thus, the energy-efficiency evaluation of available sensor interfaces is possible only through analysis of available architectures.

In this chapter, after reviewing basic concepts of sensor interfaces, a design framework denoted as holistic noise-power optimisation is presented in section 2.2. Then, the proposed design framework is shown to minimize the power consumption of a given sensor interface architecture. The presented optimisation technique is then applied to four sensor interfaces to compare their energy efficiency. Finally, the comparison result is critically analysed focusing on the two most energy efficient architectures, namely switched-capacitor (SC) capacitance to voltage converter (CVC) and successive approximation register (SAR) capacitance to digital converter (CDC).

2.1 Background

A transducer converts a physical quantity of interest (the actual physical signal), pressure in this case, to an intermediate quantity in electronic domain, basically resistance or capacitance. A sensor interface is responsible to extract the actual

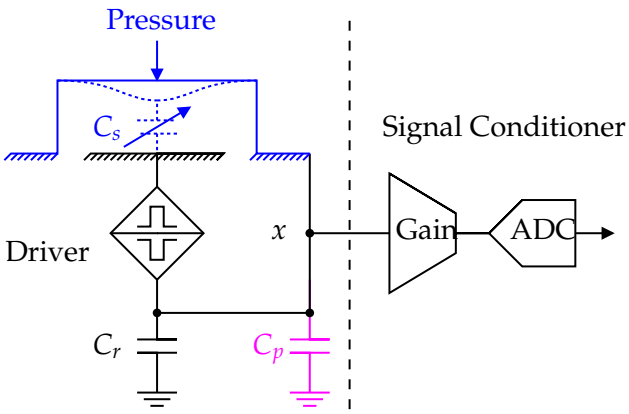


Figure 2.1: Generic capacitive pressure sensing system

signal off and prepare it for further signal processing in the electronic domain. Due to manufacturing challenges, differential pressure transducers are scarce [Mastrangelo 1996, Wang 2000], and a reference capacitor C_r (resistor R_r) is commonly used within the driver to offset the base capacitance C_{s0} (resistance R_{s0}) of the sense capacitor $C_s = C_{s0} + \Delta C$ (resistor $R_s = R_{s0} + \Delta R$). The signal, e.g. pressure, is also assumed to be linearly proportional to ΔC (ΔR). Moreover, the sensing element is usually external and wire-bonded to the sensor interface. This results in a problematic parasitic capacitance at the interconnection node (see section 2.2).

A sensor interface is comprised of a driver and a signal conditioner. Unlike data converters, a sensor interface needs to both *generate* its signal and condition (amplify and/or digitize) it. Conditioning is required since sensors often have relatively low sensitivity which means the signal generated by the driver needs to undergo some sort of amplification in presence of noise to maintain the required signal to noise ratio (SNR) set by the application. Shown in Figure 2.1 is a generic pressure sensor interface.

A capacitive-type pressure transducer (instead of resistive-type) is adopted in Figure 2.1 because of power consumption considerations. Consider Figure 2.2 which illustrates a resistive and a capacitive half-bridge driver, the simplest interface driver. Both the resistive and capacitive branches are driven by a square wave voltage source. Output voltages V_r and V_c can be respectively expressed by

$$V_r = V_{dd}\frac{R_r + \Delta R}{2R_r + \Delta R} \approx \frac{V_{dd}}{2}(1 + \frac{\Delta R}{R_r}) \tag{2.1}$$

$$V_c = V_{dd}\frac{C_r + \Delta C}{2C_r + \Delta C}(1 - e^{-t/R_{in}C_{eq}}) \approx \frac{V_{dd}}{2}(1 + \frac{\Delta C}{C_r}) \tag{2.2}$$

where R_{in} is the internal resistance of the supply voltage and C_{eq} is the series

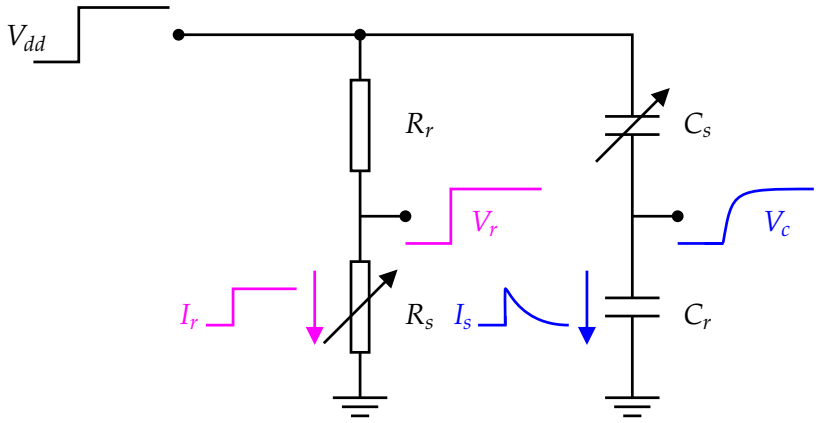


Figure 2.2: A simple resistive-capacitive half-bridge driver

equivalent capacitance of C_s and C_r, $C_{eq} = C_s C_r/(C_s + C_r)$. So for $\Delta C/C_r = \Delta R/R_r$ if $t \to \infty$, (2.1) and (2.2) are equal. However, the amount of current supplied by the source for the two branches are

$$I_r = \frac{V_{dd}}{R_s + R_r} \tag{2.3}$$

$$I_c = \frac{V_{dd}}{R_{in}} e^{-t/R_{in}C_{eq}}. \tag{2.4}$$

For $t \to \infty$, the current supplied to the capacitive branch (2.4) drops to zero. However, that of the resistive driver remains constant. Thus, the capacitive divider is more suited for low power applications because for maintaining the voltage, capacitors need not be constantly supplied by current. This is in stark contrast to the case of the resistive driver. Thus, capacitors are said to consume dynamic switching energy compared to static energy consumption of resistors. To reduce static power consumption of the resistive divider down to a few nano watts, resistors must be in a GΩ range. Creating such large resistors on integrated chips is extremely area-inefficient. Apart from that, most ADCs benefit a sample-and-hold block at the front end meaning the signal needs to be valid merely at certain points in time. Thus, continuously generating a signal at the output of the driver is power-inefficient, too. Due to these inefficiencies and implementation difficulties, capacitive transducers are preferred elements in ultra-low power applications, and hereafter the focus is only on capacitive sensor interfaces. The holistic noise power optimisation technique introduced in the next section, however, can be applied to any sensor interface regardless of the type of the transducer.

2.2 Holistic noise-power optimisation

2.2.1 Introduction

Quantitative benchmarking of state-of-the-art designs is often proposed and practised in literature. The noise [Steyaert 1987] and power [Muller 2012] efficiency factors (NEF/PEF) of neural amplifiers and Walden's FOM [Walden 1999] of analog-to-digital converters are prime examples. Interestingly, most of these performance measures are tailored towards energy efficiency, that is the minimum energy required to have a certain task done by the electronics. Since these performance measures apply to any design regardless of its architecture and implementation, they help *qualitatively* understand the relative energy efficiency of different architectures. For instance, by comparing the FOM of reported state-of-the-art analog-to-digital converters [Murmann 2016], it can be safely said that the SAR ADC and the $\Sigma\Delta$ ADC are respectively the most and least energy-efficient architectures, and that the pipeline architecture resides somewhere in the middle of the spectrum. Such a high-level description can be used as a guideline for designers in choosing the right architecture for a given application.

Unfortunately unlike the grown-up areas of data converters or RF transceivers, the number of reported designs is scant to reach a consensus about the energy efficiency ranking of different available architectures for emerging circuit families, e.g. sensor interfaces. Alternatively for such circuit families, golden theoretical reference designs can be established. These reference designs are highly optimised with respect to the parameter of interest, e.g. energy, for available topologies and thus can be compared *quantitatively* to conclude which architecture is potentially the most energy-efficient one. Furthermore thanks to the quantitative nature of the work, it is possible to learn how far current best-performing implemented designs are against their golden reference, and understand how much room is left for improvement. This latter technique, investigation of the most energy-efficient architecture by the help of golden designs, is the focus of this section.

The comparison framework proposed here bypasses the difficulty of comparing systems which work in different domains, e.g. voltage, current or time, and which are composed of inherently different building blocks, e.g. operational transconductance amplifiers vs. comparators. To make the comparison as fair as possible, all the design parameters that are common amongst the interfaces are kept the same while quantitatively evaluating final results. To keep the analysis manageable, it is assumed the interfaces are thermal noise limited and only Johnson (thermal) noise is considered. This simplifying assumption for architectures employing correlated

double sampling (CDS) is valid since flicker noise is cancelled by CDS. Moreover, it will be shown in chapter 4 that for medium-high resolution interfaces thermal-noise-limited assumption is valid since the quantisation noise level is smaller than that of the thermal noise. Finally, the proposed optimisation technique finds a lower bound on the power consumption of each interface which illustrates how well reported sensor interfaces in literature perform compared to the best achievable design.

2.2.2 Basic idea

The driving side of the interface is responsible for generating the signal by extracting ΔC from the sense capacitor. This requires deposition of charge in the sense and reference capacitors. Only a fraction, depending on the topology and the sensor sensitivity $\Delta C/C_{s0}$, of the energy consumed for charging C_s and C_r contributes to the power of the generated signal P_{signal} at the input of the conditioning circuit. So, P_{signal} can be related to the power consumption of the driver P_{driver} by

$$P_{signal,x} = \eta \times P_{driver}, \tag{2.5}$$

where $\eta \leq 1$ is the power efficiency factor. To illustrate (2.5), as an example consider the half-bridge capacitive sensor driver shown in Figure 2.3. The signals ϕ_1 and ϕ_2 are two non-overlapping clocks with frequency f. If the output signal is defined as the total amount of charge flowing into node x during ϕ_2, its power will be

$$P_{signal} = (\Delta C \times V_{ref})^2, \tag{2.6}$$

and the average power required to charge both C_s and C_r during ϕ_2 will be

$$P_{driver} = f(C_s + C_r){V_{ref}}^2. \tag{2.7}$$

So for a fixed sensor sensitivity, increasing the signal power commands increasing V_{ref} which proportionally increases the power consumption at the driver's side. The linear relationship between P_{signal} and P_{driver} is also evident from (2.6) and (2.7).

In Figure 2.1, noise at node x, $P_{noise,x}$ is dominated by the input-referred noise of the signal conditioner. But, the input-referred noise and the power consumption $P_{conditioner}$ of the signal conditioning block are inversely proportional,

$$P_{noise,x} \propto (P_{conditioner})^{-1}. \tag{2.8}$$

This last proportionality is evident from the fundamental trade-off between noise

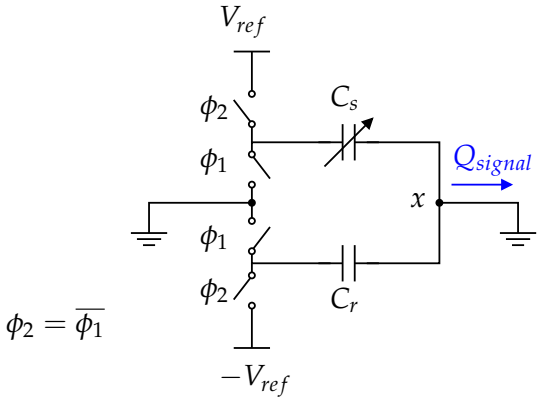


Figure 2.3: Half-bridge capacitive sensor driver

and power consumption in electronic circuits (see [Murmann 2012, Razavi 2000]). For instance, the input-referred noise power spectral density (PSD) of any front-end consisting of CMOS transistors is simply $4KT\alpha\gamma/g_m$. To decrease the input-referred noise PSD, one should increase g_m which ultimately results in increased power consumption. Dividing (2.5) by (2.8), the signal to noise ratio at node x is found,

$$SNR_x = \frac{P_{signal,x}}{P_{noise,x}} \propto (P_{driver} \times P_{conditioner}). \tag{2.9}$$

So as long as the product of P_{driver} and $P_{conditioner}$ is constant a certain SNR can be achieved. A family of solutions then exists for power allocation, only one solution is optimal though. The optimal solution for a given SNR minimizes the total power consumption of the interface,

$$P_{total} = P_{driver} + P_{conditioner}. \tag{2.10}$$

Two worst solutions also exist when the total power consumption is maximized: 1) Maximum P_{driver}, minimum $P_{conditioner}$, and 2) Maximum $P_{conditioner}$, minimum P_{driver}. In fact, by converting the proportionality of (2.9) to equality by a constant factor K, that is $SNR = K \times P_{driver} \times P_{conditioner}$, the optimal solution will be

$$P_{driver} = P_{conditioner} = \sqrt{\frac{SNR}{K}}, \tag{2.11}$$

however, in general, the proportionality expressed in (2.9) takes the form of

$$SNR \propto \sum_{m=0}^{M} \eta_m {P_{driver}}^m \times \sum_{n=0}^{N} \eta_n {P_{conditioner}}^n, \tag{2.12}$$

where $M, N \geq 1$ and $0 < \eta_{m,n} < 1$ are topology-dependent constants. For topologies of interest, the relationships between (P_{driver}, P_{signal}) and $(P_{conditioner}, P_{noise})$ can be analytically derived, and the optimal power allocation to the driver and signal conditioner can be found using (2.10) and (2.12). State-of-the-art sensor interfaces are designed such that the driver charges the sense and reference capacitors to the maximum available voltage to maximize P_{signal}, and then the input referred noise of the conditioning circuit is set accordingly. This design practice, however, neglects P_{driver} which due to the discussion above may not lead to an optimal solution from power management perspectives. Please note in the foregoing analysis, the switches clock feed-through and charge injection are neglected. From practical standing points, the clock feed-through is negligible because sense and reference capacitors C_s and C_r are much larger than the overlap capacitance of the MOS switches. The charge injection of ϕ_2 switches is irrelevant, since the signal is available before ϕ_2 switches become non-transparent. Also, because of differential sampling at ϕ_1, and that their injected charge is input-independent (similar to bottom-plate sampling), their contribution appears only as an offset that is dealt with differential circuits. The conditioned explained earlier hold true for the discrete-time systems of interest and thus the effect of charge-injection and clock-feed-through is neglected throughout this chapter. In the next section, the introduced optimization technique is applied to the ubiquitous switched-capacitor capacitance-to-voltage converter, SAR capacitance-to-digital converter, Transimpedance amplifier and time-based capacitive sensor interfaces to enable a comparison between all these architectures with regard to their energy efficiency. The switched-capacitor interface is treated first.

2.2.3 CDS Switched-Capacitor CVC

A generic switched-capacitor capacitance-to-voltage converter is shown in Figure 2.4. Pre-charged correlated double sampling switching scheme [Ha 2014] is used as a reference architecture since it requires only a single supply rail (in contrast to bipolar $\pm V_{ref}$ supply rails [Chun 1985]) and enables digital correction of low-frequency noise and the input-referred offset of the amplifier. The signals ϕ_1 and ϕ_2 are two non-overlapping conversion clock signals, while ϕ_p defines the pre-charging phase. As denoted in Figure 2.4, a complete CVC cycle requires two pre-charging phases each followed by a voltage conversion phase. The operation of the SC CVC is summarized in Figure 2.5. At the end of the first and second conversion phases,

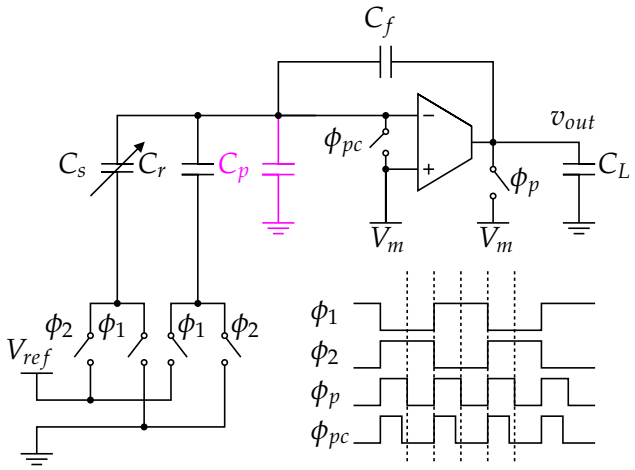


Figure 2.4: A generic switched-capacitor capacitance-to-voltage convert; the timing diagram of the switches is also shown in the panel.

the output voltage of the amplifier is respectively,

$$v_{o1} = \frac{C_s - C_r}{C_f} V_{ref} + \frac{C_s + C_r + C_p}{C_f} V_{OS}, \tag{2.13}$$

and

$$v_{o2} = \frac{C_r - C_s}{C_f} V_{ref} + \frac{C_s + C_r + C_p}{C_f} V_{OS}, \tag{2.14}$$

where V_{OS} is the input-referred offset voltage of the amplifier. It is assumed that at the end of each phase $v_{o1,2}$ is sampled and digitized by a quantizer. So, subtracting (2.13) from (2.14) in digital domain yields

$$v_{signal} = v_{o1} - v_{o2} = \frac{2\Delta C}{C_f} V_{ref}. \tag{2.15}$$

The power consumption of the half-bridge driver for a full conversion cycle (precharge1, conversion1, precharge2, conversion2) can be expressed as

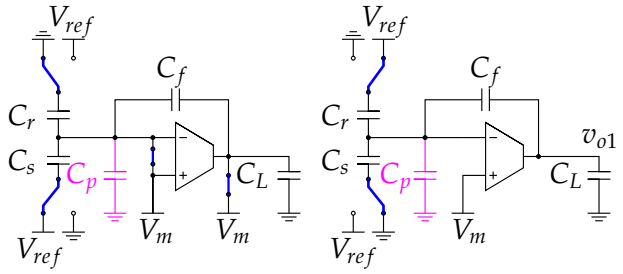
$$P_{driver} = f_s (C_s + C_r) {V_{ref}}^2, \tag{2.16}$$

where f_s is the conversion frequency.

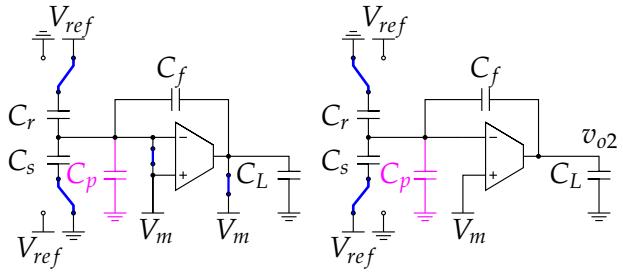
Two noise sources contribute to the total output referred noise $\overline{v_n{}^2}$ of the SC CVC,

$$\overline{v_n{}^2} = \overline{v_{n,sw}{}^2} + \overline{v_{n,gm}{}^2}. \tag{2.17}$$

$\overline{v_{n,sw}{}^2}$ is due to the noise of the switches during the pre-charging phase, and $\overline{v_{n,gm}{}^2}$ is regarding the noise of the amplifier during the conversion phase. Just before ϕ_{pc}



(a) First precharge, sub-conversion



(b) Second precharge, sub-conversion

Figure 2.5: SC CVC conversion phases

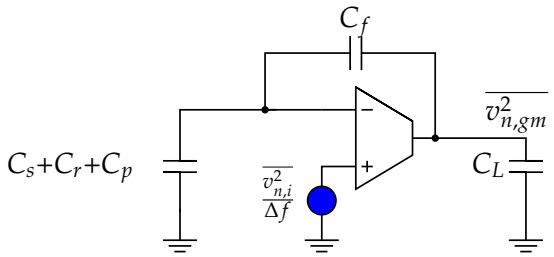


Figure 2.6: An equivalent circuit diagram of SC CVC interface in the sub-conversion phase. The input-referred noise source of the g_m-cell is explicitly shown at the non-inverting input of the g_m-cell.

transitions to low, C_s, C_r, C_p and C_f appear in parallel and form a single degree of freedom from energy storage point of view. The equipartition theorem then can be deployed [Murmann 2012] to find out the total noise charge $\overline{q_n{}^2}$ sampled by this degree of freedom as

$$\overline{q_n{}^2} = KT(C_s + C_r + C_p + C_f). \tag{2.18}$$

This noise charge then redistributes across C_f in the conversion phase and generates

$$\overline{v_{n,sw}{}^2} = \frac{KT(C_s + C_r + C_p + C_f)}{C_f{}^2}. \tag{2.19}$$

Figure 2.6 displays the CVC in the conversion period. The amplifier is modelled

by a g_m-cell with unit-gain bandwidth of g_m/C_L. During this phase, only the noise from the amplifier is considered because if the switches are designed with $R_{on} \ll 1/g_m$, their noise contribution to $\overline{v_n{}^2}$ is minimal and can be ignored [Murmann 2012]. The noise transfer function $V_{n,out}/V_{n,gm}$ and the output noise power $\overline{v_{n,gm}{}^2}$ during the conversion phase are respectively

$$NTF(s) = \frac{1}{\beta(1 + s\frac{C_L+(1-\beta)C_f}{\beta g_m})}, \tag{2.20}$$

$$\omega_{noise} = \frac{\beta g_m}{C_L + (1-\beta)C_f} \tag{2.21}$$

$$\overline{v_{n,gm}{}^2} = \frac{4KT\alpha\gamma}{g_m}\frac{1}{\beta^2}\frac{\omega_{noise}}{4} = \frac{KT\gamma\alpha/\beta}{C_L + (1-\beta)C_f} = \frac{KT\gamma\alpha/\beta}{C_{eq}}. \tag{2.22}$$

In (2.20) and (2.22), β is the capacitive feedback factor

$$\beta = \frac{C_f}{C_s + C_r + C_p + C_f}, \tag{2.23}$$

γ is the noise coefficient of MOS transistors, and α is the topology-dependent excess noise factor of the amplifier. The total output noise power is then

$$\overline{v_n{}^2} = \frac{KT(C_s + C_r + C_p + C_f)}{C_f{}^2} + \frac{KT\gamma\alpha/\beta}{C_L + (1-\beta)C_f}. \tag{2.24}$$

Assuming the duration of the pre-charging phase is negligible to that of the conversion phase and that double sampling is employed, if $f_s = 1/T_s$ is the sampling frequency, the output of the amplifier has $T_s/2$ seconds to settle to within half-LSB error, that is

$$v_o e^{-T_s/2\tau} \leq \frac{v_o}{2^{N+1}}. \tag{2.25}$$

In (2.25), $\tau = 1/\omega_{-3dB}$ is the time-constant of the system in the conversion phase, and N is the quantization resolution. Solving (2.25) for τ finds the minimum bound of the system bandwidth

$$\omega_{-3dB} \geq f_s(N+1)\ln(2). \tag{2.26}$$

Based on (2.24), increasing C_L is the only way to decrease the output referred noise of the SC CVC because other terms are either constants (K, T, γ, α) or given by the sensor specifications and the sensor-interface interconnection quality (C_s, C_r, C_p and C_f due to (2.15)). Increasing C_L, however, trades off with ω_{-3dB} and ultimately

Table 2.1: Typical design parameters used for noise-power optimization of SC CVC and SAR CDC

C_{s0} [pF]	ΔC [pF]	C_p [pF]	α	γ	ζ	V_{dd} [V]	f_s [kHz]
6	2	6	4	0.5	1.5	1	1

g_m (since ω_{-3dB} must maintain a minimum value according to (2.26)) through

$$\omega_{-3dB} = \frac{\beta g_m}{C_L + (1-\beta)C_f}. \tag{2.27}$$

Combining (2.15), (2.24), (2.26) and (2.27), the relationship between the SNR, V_{ref} and g_m can be expressed as

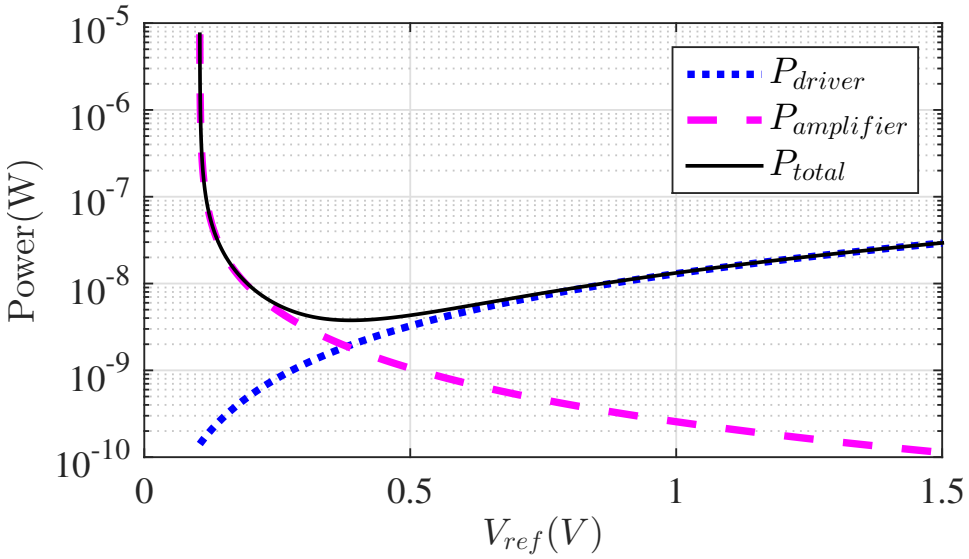
$$g_m = \frac{\alpha\gamma f_s (N+1)\ln(2)}{\frac{2}{KTSNR}\left(\frac{\Delta C V_{ref}}{C_s+C_r+C_p+C_f}\right)^2 - \frac{1}{C_s+C_r+C_p+C_f}}. \tag{2.28}$$

Depending on the topology and biasing regime of the amplifier g_m can be related to its power consumption. For instance, for a sub-threshold folded-cascode amplifier

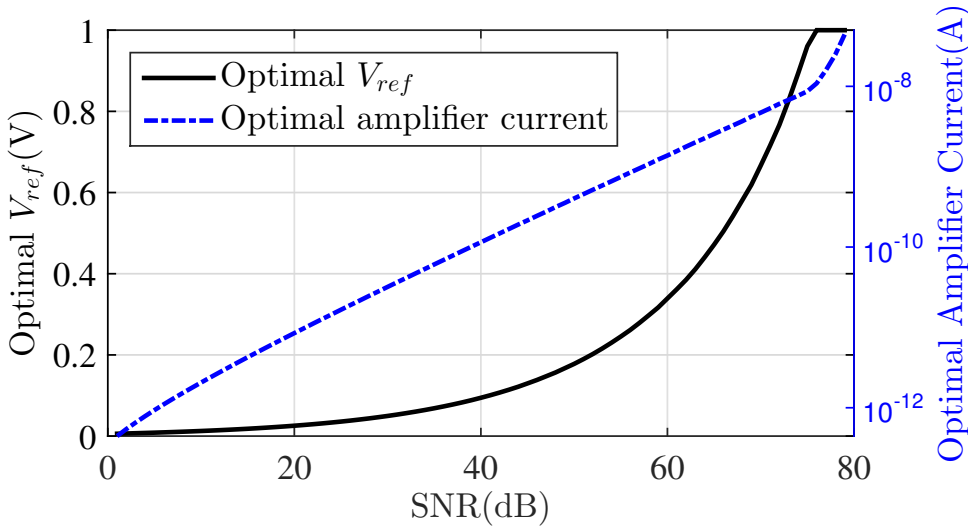
$$P_{amplifier} \geq 2\zeta V_t g_m V_{dd}, \tag{2.29}$$

where ζ is the subthreshold slope coefficient, V_t is the thermal voltage and V_{dd} is the supply voltage of the amplifier. For a list of design parameters (C_s, ΔC, C_p, f_s, V_{dd}, α, γ and SNR), (2.28) can be used to solve for a family of solution for V_{ref} and g_m. Each solution duo (V_{ref}, g_m) can then be mapped to the power consumption domain (P_{driver}, $P_{amplifier}$, P_{total}) according to (2.10), (2.16) and (2.29).

Table 2.1 lists typical design parameters used for illustration of noise-power optimization of SC CVC. To achieve 60dB of SNR, Figure 2.7a demonstrates a family of solutions for power allocation to the driver and the amplifier. The total power consumption of the interface is also plotted in the same panel suggesting that for 60dB of SNR P_{total} is minimized only if $V_{ref} = 0.33V$; note also how P_{total} is dominated by $P_{amplifier}$ and P_{driver} for $V_{ref} < 0.33V$ and $V_{ref} > 0.33V$, respectively. For a given SNR, there exists a unique V_{ref} (and so $I_{amplifier}$) that leads to a minimal P_{total}. These values are displayed in Figure 2.7b where it is assumed that the maximum available voltage is $1V$ (the same as V_{dd}). For SNRs>75dB, V_{ref} is capped to $1V$, and therefore P_{driver} is fixed. So to maintain the required SNR, the amplifier noise must be more aggressively reduced which needs a significant increase in its supply current and ultimately in a non-optimal P_{total}. Following the results shown



(a) Power management of sub blocks of the SC CVC for the case of 60dB SNR



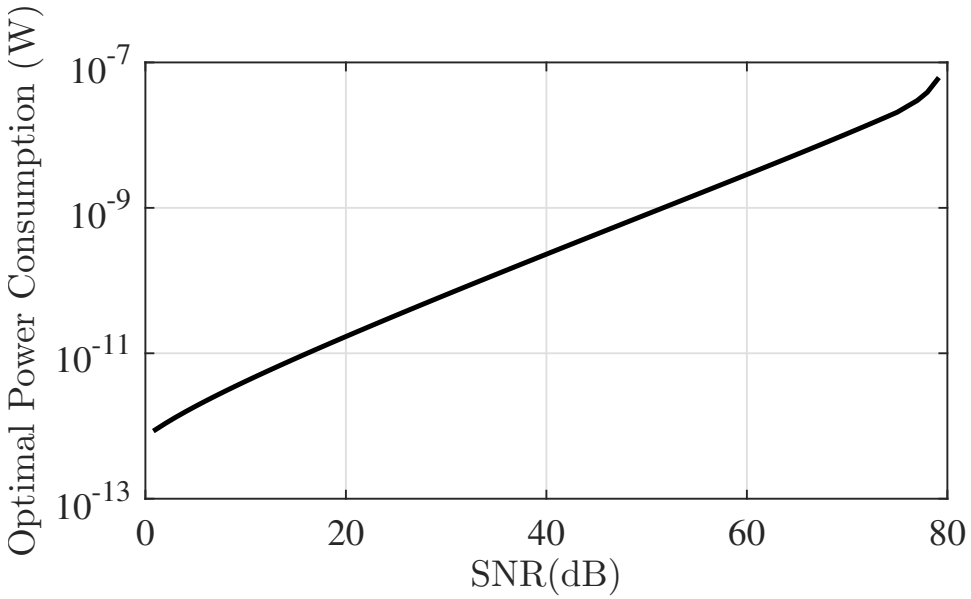
(b) Optimal V_{ref} and amplifier current

Figure 2.7: Demonstration of presence of optimal power management

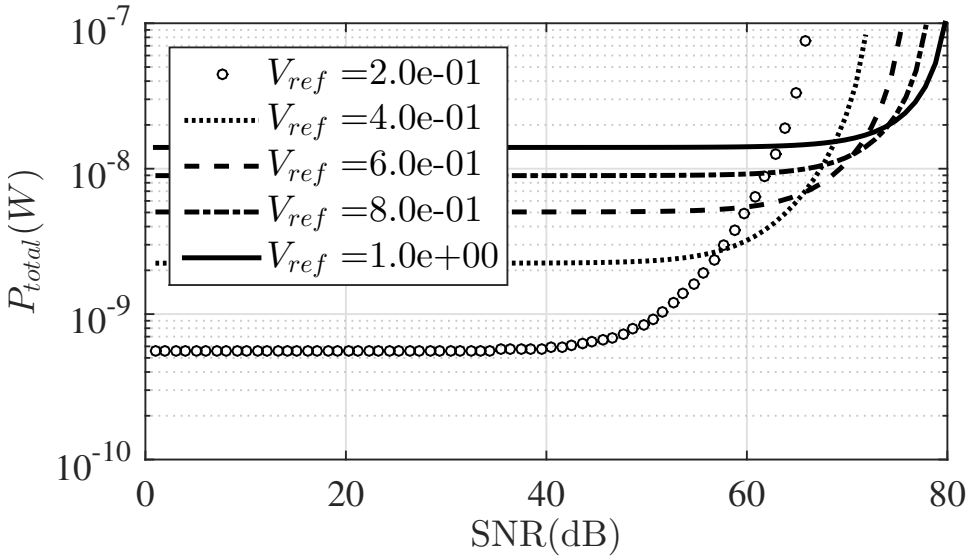
in Figure 2.7b, the lower bound on P_{total} as a function of SNR can be derived as depicted in Figure 2.8a.

In practice, generating V_{ref} other than the maximum available voltage V_{dd} is often costly, and it is preferred to have $V_{ref} = V_{dd}$. To illustrate the excess power consumption in such cases consider Figure 2.8b. Choosing $V_{ref} = V_{dd} = 1V$, instead of the optimal value of $0.33V$, when 60dB of SNR is required gives rise to a P_{total} which is 5 times as large as the optimal value.

Next, the optimization technique discussed earlier is applied to the SAR CDC.



(a) Lower bound on P_{total}



(b) Total power consumption of the interface for different driving voltages

Figure 2.8: Noise-power optimization characteristic graphs of CDS SC CVC

As a result, similar figures to Figure 2.7 and Figure 2.8 will be obtained for the SAR CDC architecture to allow performance comparison of the two interfaces.

2.2.4 CDS Successive Approximation Register CDC

The SAR CDC architecture is shown in Figure 2.9. The main difference between the SAR CDC and the SC CVC is in the former the output is available in the

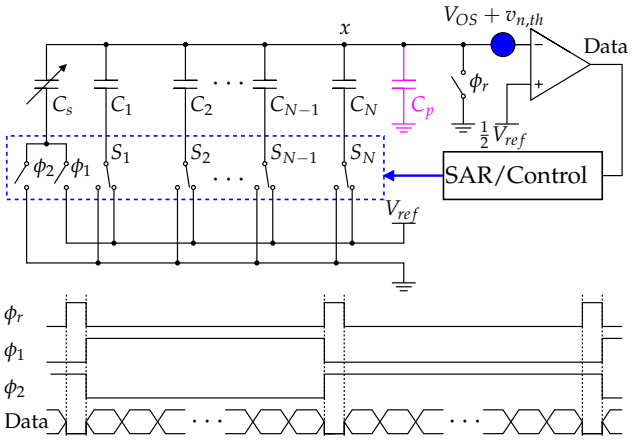


Figure 2.9: SAR CDC architecture

digital form, but a stand alone SC CVC must be followed by a quantizer in case a digital output is required. To make the power consumption comparison of the two interfaces as fair as possible, the SAR CDC analysed here also incorporates correlated double sampling. Also, the same design parameters listed in table 2.1 are used for quantitative data representation. Furthermore, it is assumes the comparator is comprised of a latch and a pre-amplifier, and the noise and offset of the pre-amplifier dominate. The interface operates in two phases ϕ_1 and ϕ_2, and each phase is preceded by a reset phase ϕ_r during which all the capacitors are discharged. In ϕ_1, the top plate of the sense capacitor C_s is switched to V_{ref} and the bottom plates of the capacitors in the capacitive array switched to V_{ref} in a SAR fashion such that at the end of ϕ_1, the input terminals of the comparator are at the same potential, neglecting the quantization error, that is

$$V_{ref}\frac{C_s+C_{\phi_1}}{C_s+C_p+C_T}+(V_{OS}+v_{n,th})=\frac{1}{2}V_{ref}, \tag{2.30}$$

where C_T is the total capacitance of the array, C_p is the parasitic interconnection capacitance, $C_{\phi 1}$ is the total capacitance of the array that remains connected to V_{ref} at the end of ϕ_1, V_{OS} and $v_{n,th}$ are respectively the offset and the input referred thermal noise of the comparator. Rearranging (2.30), $C_{\phi 1}$, which is available in digital domain, is given by

$$C_{\phi 1}=\frac{C_T-C_s+C_P}{2}-\frac{V_{OS}+v_{n,th1}}{V_{ref}}(C_T+C_s+C_p). \tag{2.31}$$

In the second conversion phase, the top plate of the sense capacitor is connected to ground, and the SAR bit-cycling process results in

$$C_{\phi 2} = \frac{C_T + C_s + C_P}{2} - \frac{V_{OS} + v_{n,th2}}{V_{ref}}(C_T + C_s + C_p). \tag{2.32}$$

The final digital code, in terms of capacitance, is found by subtracting (2.31) from (2.32),

$$C_{out} = C_s + \frac{v_{n,th1} - v_{n,th2}}{V_{ref}}(C_T + C_s + C_p). \tag{2.33}$$

C_{out} has a signal component,

$$C_{out,s} = C_s = C_{s0} + \Delta C, \tag{2.34}$$

and a noise component,

$$C_{out,n} = \frac{v_{n,th1} - v_{n,th2}}{V_{ref}}(C_T + C_s + C_p), \tag{2.35}$$

where it is assumed that the input referred noise of the comparator during the phases ϕ_1 and ϕ_2 is uncorrelated. The main drawback of the SAR CDC compared to the SC CVC is apparent from (2.34), that is the total sense capacitor has to be quantized, while C_{s0} carries no information and only ΔC is of interest. So with

$$SNR = \frac{\Delta C^2}{\overline{C_{out,n}{}^2}}, \tag{2.36}$$

the SAR CDC must be implemented for an extended SNR range SNR^* defined as

$$SNR^* = C_{out,s}^2 / \overline{C_{out,n}{}^2} = (\frac{C_{s0} + \Delta C}{\Delta C})^2 \times SNR, \tag{2.37}$$

meaning the resolution of the CDC must be increased by $\log_2(1 + C_{s0}/\Delta C)$ which leads to a proportional increase in the power consumption of the driver (capacitive array).

By modelling the pre-amplifier by a g_m-cell with a dominant pole at ω_0, its total input referred noise can be expressed as

$$\overline{v_{n,pre}{}^2} = \frac{KT\gamma\alpha\omega_0}{g_m}. \tag{2.38}$$

The speed requirement on the pre-amplifier is stricter than that of the SC CVC, since for the SAR CDC the output of the pre-amplifier has T_s/N seconds, compared to T_s

seconds of the SC CVC, to settle to within half-LSB error. So,

$$\omega_0 \geq f_s N(N+1)\ln(2). \tag{2.39}$$

In addition to (2.38), the switch noise sampled by the capacitive array at the time the reset switch opens, $KT/(C_T+C_s+C_p)$, also appears at the input of the comparator. The two noise components according to (2.35) generate the total noise power

$$\overline{C_{out,n}{}^2} = 2\left(\frac{KT}{C_T+C_s+C_p} + \frac{KT\gamma\alpha\omega_0}{g_m}\right)\left(\frac{C_T+C_s+C_p}{V_{ref}}\right)^2. \tag{2.40}$$

Using (2.36), (2.39) and (2.40), the relationship between SNR, g_m and V_{ref} can be derived

$$g_m = \frac{\alpha\gamma f_s N(N+1)\ln(2)}{\frac{2}{KTSNR}\left(\frac{\Delta C V_{ref}}{C_s+C_r+C_p+C_f}\right)^2 - \frac{1}{C_s+C_r+C_p+C_f}}. \tag{2.41}$$

The g_m expressed by (2.41) is N times as large as that of the SC CVC (2.28), and so in general signal conditioning in the SAR CDC requires more power than the SC CVC. This is a direct consequence of excess bandwidth requirement for digitization (2.39). Moreover, because the base capacitance C_{s0} also needs to be quantized in the SAR CDC, for the same ΔC, N of the SAR CDC is $\log_2(1+C_{s0}/\Delta C)$ larger than N in the case of the SC CVC.

The power consumption of the driver (capacitive array) in the SAR CDC is a C_s-and-C_p-dependent complex function; the effect of V_{OS} is ignored here because the switching energy consumption is only a weak function of V_{OS}.

To calculate the total switching energy consumption of the N-bit SAR CDC shown in Figure 2.9, the sum of packets of charge drawn form the supply voltage V_{ref} must be determined during the SAR bit-cycling process for both the phases ϕ_1 and ϕ_2. During the reset phase, all the capacitors are discharged to ground. In ϕ_1, the sense capacitor C_s and the MSB capacitor of the array C_1 are switched to V_{ref}. This results in the voltage of the floating node v_x to jump to

$$v_{x,\phi 1}[1] = \frac{C_s+C_1}{C_T+C_s+C_p}V_{ref}, \tag{2.42}$$

So, the voltage across both C_s and C_1 has changed from 0 to $V_{ref}-v_{x,\phi 1}[1]$, and the charges required for this voltage change across C_s and C_1 are respectively

$$Q_{s,\phi 1}[1] = C_s(V_{ref}-v_{x,\phi 1}[1]), \tag{2.43}$$

$$Q_{a,\phi 1}[1] = C_1(V_{ref}-v_{x,\phi 1}[1]). \tag{2.44}$$

At the end of ϕ_1 according to (2.31), the digital representation $\mathbf{D_{\text{Œ1}}}$ of $C_{\phi 1}$ is available. $\mathbf{D_{\text{Œ1}}}$ is an array of binary values $\mathbf{D_{\text{Œ1}}} = [D_{\phi 1}(1), D_{\phi 1}(2), \cdots D_{\phi 1}(N)]$, where $D_{\phi 1}(i)$ is the output of the comparator after the i$^{\text{th}}$ comparison/step. For known C_s and C_p, $\mathbf{D_{\text{Œ1}}}$ can be calculated by the help of which the floating node voltage after the i$^{\text{th}}$ switching step can be derived as

$$v_{x,\phi 1}[i] = \frac{C_s + C_i + \sum_{k=1}^{i-1} D_{\phi 1}(k) C_k}{C_T + C_s + C_p} V_{ref}. \tag{2.45}$$

Consequently, (2.43) and (2.44) for the i$^{\text{th}}$ ($2 \leq i \leq N$) step are given by

$$Q_{s,\phi 1}[i] = C_s(v_{x,\phi 1}[i-1] - v_{x,\phi 1}[i]), \tag{2.46}$$

$$Q_{a,\phi 1}[i] = (C_i + \sum_{k=1}^{i-1} C_k D_{\phi 1}(k))(v_{x,\phi 1}[i-1] - v_{x,\phi 1}[i]) + C_i V_{ref}. \tag{2.47}$$

Using (2.43)–(2.47), the total charge drawn from V_{ref} during ϕ_1 can be calculated

$$Q_{\phi_1} = \sum_{i=1}^{N} (Q_{s,\phi 1}[i] + Q_{a,\phi 1}[i]) \tag{2.48}$$

A similar analysis can be applied to calculate $Q_{\phi 2}$. Since C_s is grounded in this phase $Q_{s,\phi 2} = 0$, and only $Q_{a,\phi 2}$ needs to be considered. The voltage of the floating node v_x after the MSB capacitor of the array C_1 is switched to V_{ref} is given by

$$v_{x,\phi 2}[1] = \frac{C_1}{C_T + C_s + C_p} V_{ref}, \tag{2.49}$$

which translates to a transfer of charge equal to

$$Q_{a,\phi 2}[1] = C_1(V_{ref} - v_{x,\phi 1}[1]) \tag{2.50}$$

from V_{ref} to C_1. For $2 \leq i \leq N$, (2.49) takes the form of

$$v_{x,\phi 2}[i] = \frac{C_s + C_i + \sum_{k=1}^{i-1} D_{\phi 2}(k) C_k}{C_T + C_s + C_p} V_{ref}, \tag{2.51}$$

where $D_{\phi 2}(i)$ is the i$^{\text{th}}$ MSB-bit of the output code. By using (2.51), the charge drawn from V_{ref} at the i$^{\text{th}}$ ($2 \leq i \leq N$) SAR step can be expressed by

$$Q_{a,\phi 2}[i] = (C_i + \sum_{k=1}^{i-1} C_k D_{\phi 2}(k))(v_{x,\phi 2}[i-1] - v_{x,\phi 2}[i]) + C_i V_{ref}, \tag{2.52}$$

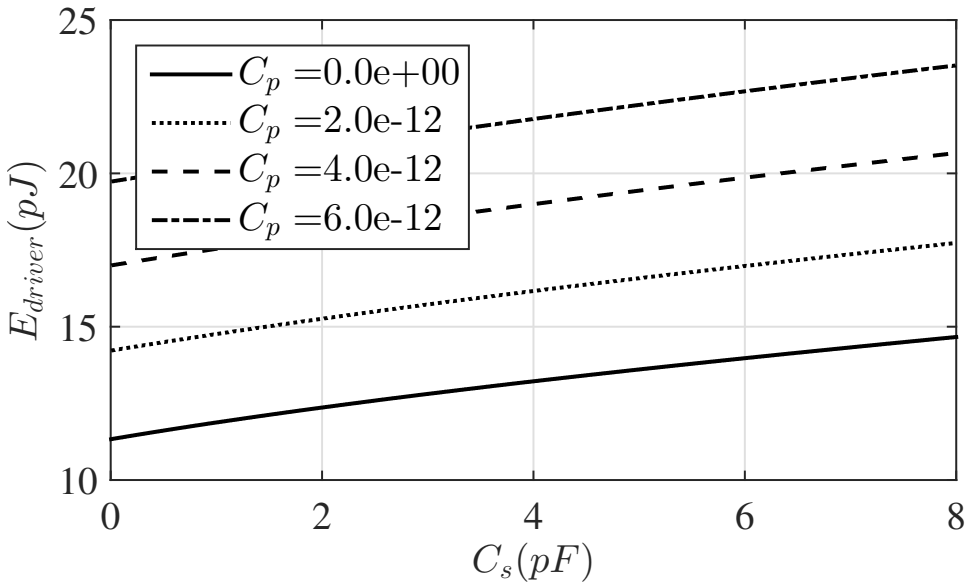


Figure 2.10: Total switching energy consumption of capacitive array

and the total charge transfer during ϕ_2 will be given by

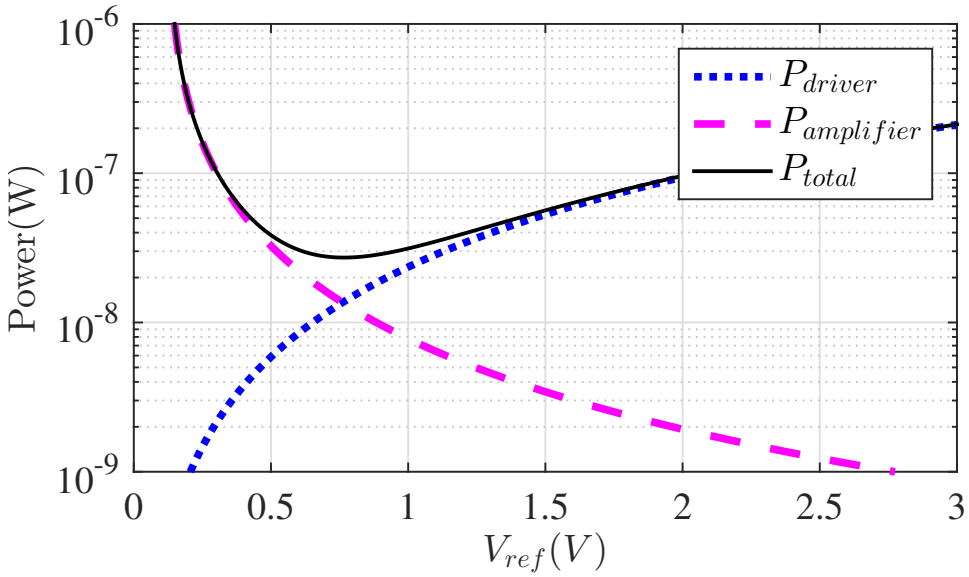
$$Q_{\phi_2} = \sum_{i=1}^{N} Q_{a,\phi 2}[i]. \tag{2.53}$$

Finally, the total switching energy consumption associated with the capacitive array of the correlated-double sampling SAR CDC is given by

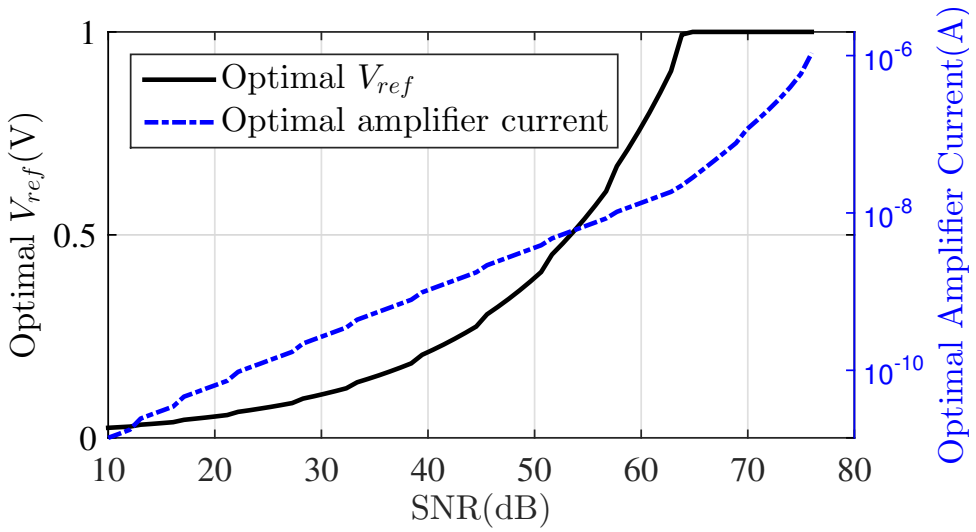
$$E_{driver} = (Q_{\phi_1} + Q_{\phi_2})V_{ref}. \tag{2.54}$$

The switching energy (including correlated double sampling) of the capacitive array E_{driver} as discussed above is a function of $C_s = C_{s0} + \Delta C$, C_p and V_{ref}. To illustrate this, E_{driver} is plotted in Figure (2.10) as a function of $C_s = C_{s0} + \Delta C$ and C_p for a fixed reference voltage $V_{ref} = 1$ [V]. The linear relationship between E_{driver} and C_p is evident in Figure (2.10). Furthermore, the switching energy of this capacitive array for small values of $C_p \approx 0$ is equal to that of the SC CVC half-bridge driver. It can also be noticed that E_{driver} is an increasing function of C_s. So, for the worst case scenario, the maximum value of $C_s = C_{s0} + \Delta C$ is used to estimate the power consumption of the capacitive array.

Using (2.29), (2.41) and (2.54) a set of noise-power optimization figures, similar to Figure 2.7 and Figure 2.7, can also be generated, as shown in Figure 2.11 and Figure 2.12, for the CDS SAR CDC.



(a) Power management of sub blocks of the CDS SAR CDC for the case of 60dB SNR



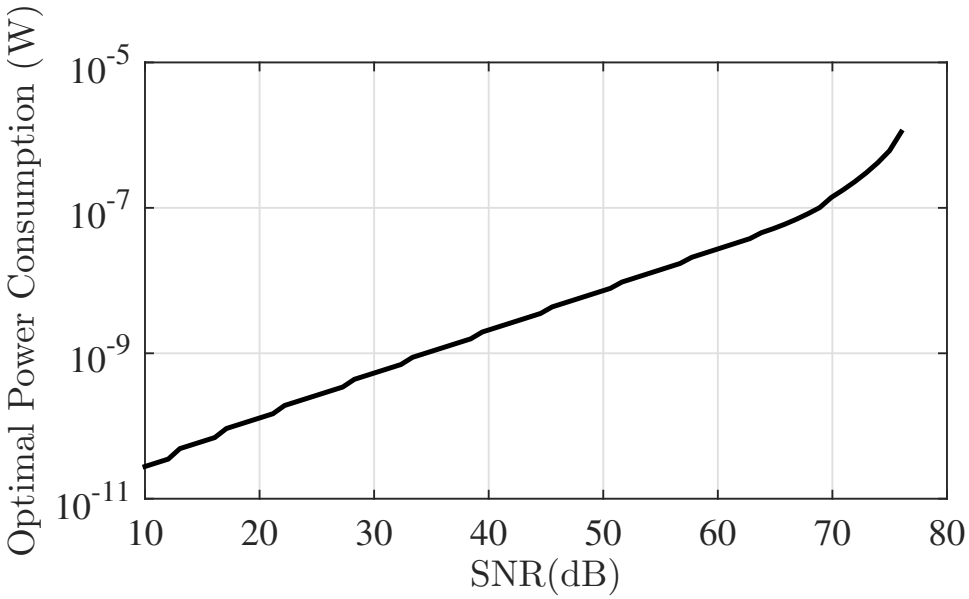
(b) Optimal V_{ref} and amplifier current

Figure 2.11: Demonstration of presence of optimal power management

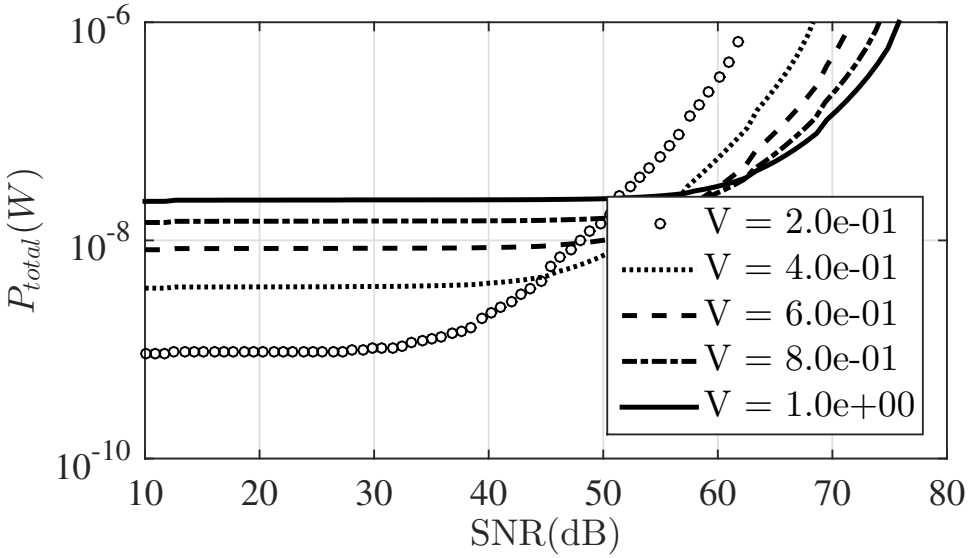
2.2.5 Critical analysis I

Since the optimal power consumption of the foregoing CDS SC CVC and CDS SAR CDC are found marginally in the same range (see Figures 2.8 and 2.12), before delving into noise-power optimisation of the other architectures, it is worthwhile critically analyse the obtained results to summarise under what circumstances each of these architectures is more energy-efficient.

Shown in Figure 2.13 is the *ideal* lower bound on the power consumption of



(a) Lower bound on P_{total}



(b) Total power consumption of the interface for different driving voltages

Figure 2.12: Noise-power optimization of CDS SAR CDC

the two architectures when it is assumed the cost of generating an arbitrary V_{ref} other than V_{dd} is negligible, and so the driver side of the interface can leverage the optimal V_{ref} value, based on Figure 2.7b and Figure 2.11b, to achieve a certain SNR. In this ideal case, the SC CVC outperforms the SAR CDC by a factor of 7 for the entire SNR range.

In a realistic case, however, since loss-less generation of an arbitrary voltage on

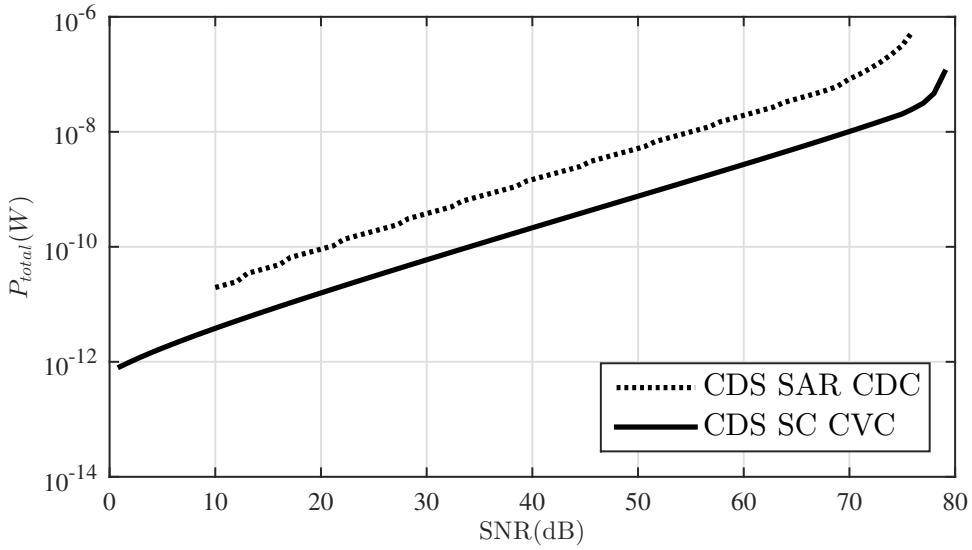
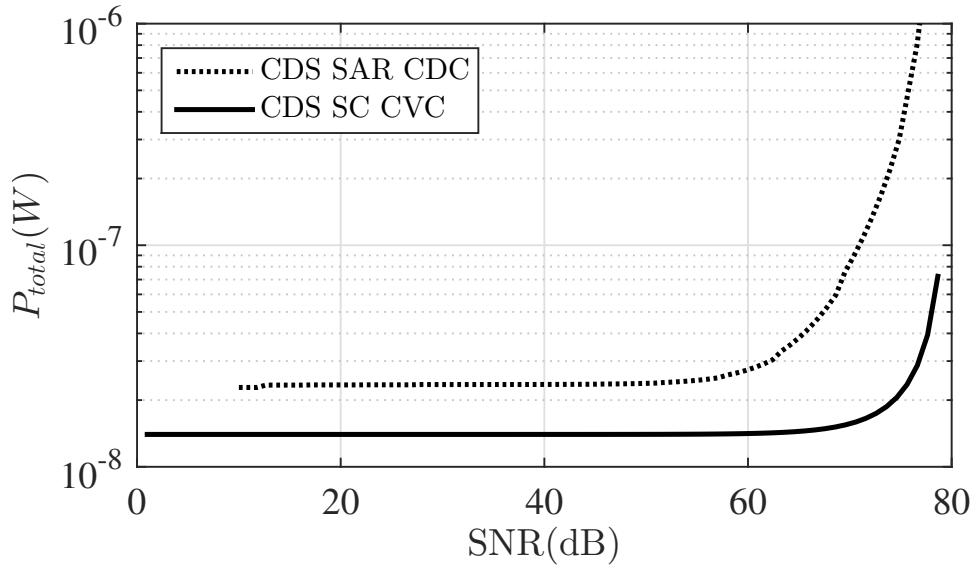


Figure 2.13: Minimum power consumption with *flexible* optimal V_{ref}, $C_p = 6$pF

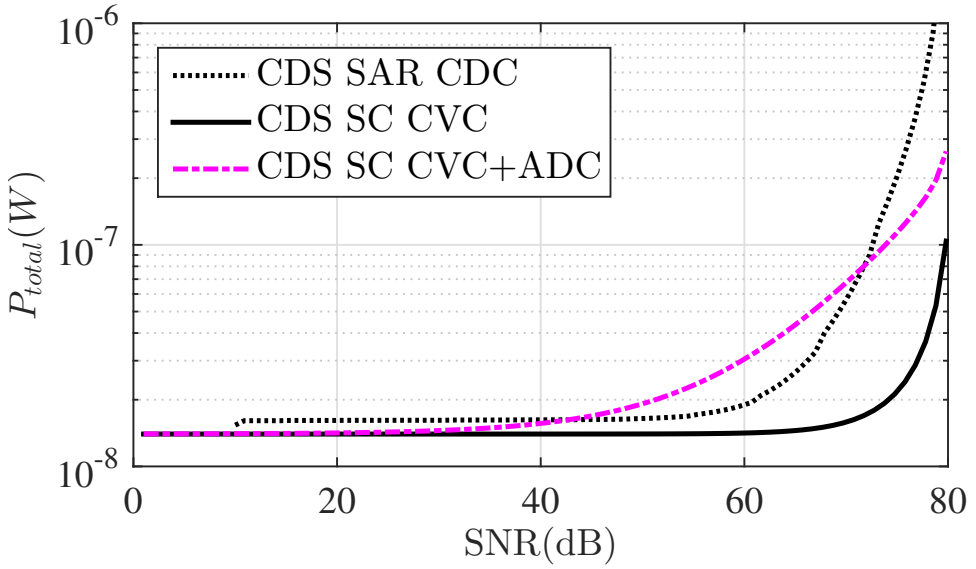
the driver's side V_{ref} is impractical, the discussion is limited to the case where $V_{ref} = V_{dd}$. For design parameters listed in Table 2.1, the minimum power consumption of the SC CVC and SAR CDC with respect to SNR is plotted in Figure 2.14a where it is assumed $V_{ref} = V_{dd} = 1V$. For the entire SNR range, the SC CVC is found to be twice as more power efficient as the SAR CDC. But, Figure 2.14a does not account for required power consumption for digitization in the case of SC CVC.

The output of the SAR CDC is digital, whereas that of the SC CVC is analog and for digitization it needs to be followed by an ADC. Therefore, for the most fair comparison, the power consumption of the ADC, P_{ADC}, should also be included. Also, it will be shown in the next section that with heterogeneous sensor-interface integration proposed in this work, C_p can be as small as 1pF. Figure 2.14b reflects the effect of P_{ADC} and $C_p = 1$pF. The ADC is assumed to have a state-of-the-art ([Harpe 2015, Liu 2015, Tai 2014, Liou 2013, Harpe 2013]) Figure of Merit of 10fJ/Conversion-step. First of all, it can be observed that for $C_p = 1$pF (compared to the case where $C_p = 6$pF) the power consumption of the SAR CDC and SC CVC tend towards each other for SNR<$\sim$60dB. This is mainly because in this case the SAR CDC requires a smaller full-scale range. Moreover, for 40dB <SNR<72dB, the SAR CDC outperforms the cascade of SC CVC and an ADC. In an actual design, for 40dB <SNR<72dB, the gap between the power consumption of SAR CDC and SC CSV+ADC shown in Figure 2.14b further increases for a non-optimal ADC with energy efficiency of <10fJ/Conversion-step.

So, in summary, direct SAR capacitance to digital conversion for SNR up to $\sim$72dB is found to be the optimal choice, if the parasitic interconnection capacitance



(a) Minimum power consumption vs. SNR for $C_p = 6$pF



(b) Minimum power consumption vs. SNR for $C_p = 1pF$. The included ADC is assumed to have FOM=10fJ/Conversion-step.

Figure 2.14: Minimum power consumption comparison with $V_{ref} = V_{dd} = 1V$, and the design parameters listed in Table 2.1 but with $C_p = 1$pF

can be kept small. However, for high-resolution digitization in presence of large parasitic interconnection capacitance, the cascade of SC CVC and an energy efficient ADC is the optimal choice. Summarized in Table 2.2 is the qualitative comparison of the two interfaces for different conditions. In the next section, heterogeneous integration of the sense capacitor and the CMOS interface is introduced as a means

Table 2.2: Qualitative comparison of the SC CVC and the SAR CDC

Architecture	Output	SNR	C_p
SC CVC	Analog	–	–
SC CVC + ADC	Digital	Low-High	High
SAR CDC	Digital	Low-Medium	Low

of minimizing C_p and enabling energy-efficient CDS SAR capacitance to digital conversion explained in this section.

2.2.6 Transimpedance interface

The continuous-time version of the switched-capacitor interface is the well-known transimpedance architecture whose simplified circuit diagram is shown in Figure 2.15. The sensor and reference capacitors are driven by a half-bridge driver at some optimal driving frequency (see below). The voltage-current feedback around the OTA is the key factor behind the operation of the interface. To the first order, it offers input impedance as low as $1/g_m$ while maintaining node 'x' at virtual ground. Providing that the capacitors are driven differentially, a current proportional to $\Delta C = C_s - C_r$ is injected to the virtual ground node and thus flows through the feedback resistor which eventually outputs a voltage proportional to ΔC, R_f, driving signal amplitude and frequency. As the whole interface has a band-pass characteristic, the output is preferred to be a sinusoidal signal which is in stark contrast to the switched-capacitor interface. Thus, a mixer must be used to down convert the output signal to DC so as to prepare it for digitisation. Note for the sake of simplicity, power consumption of the synchronous mixer and the the low-pass filter is assumed negligible and thus neglected for the analysis that follows. Nonetheless, their effects can be accounted for in the same fashion the effect of ADC was included to the total power consumption of the CDS SC CVC in the previous section if needed.

The transimpedance interface can be designed in a number of ways. In order for the text to be self-contained, a design procedure is first described which makes the optimisation analysis more straightforward. Similar to the switched-capacitor interface, the OTA is modelled by a gm-cell with infinite output resistance and a unity gain bandwidth of g_m/C_L. The OTA is assumed to have a folded-cascode architecture operating in the subthreshold region, and thus its power consumption is given by (2.29).

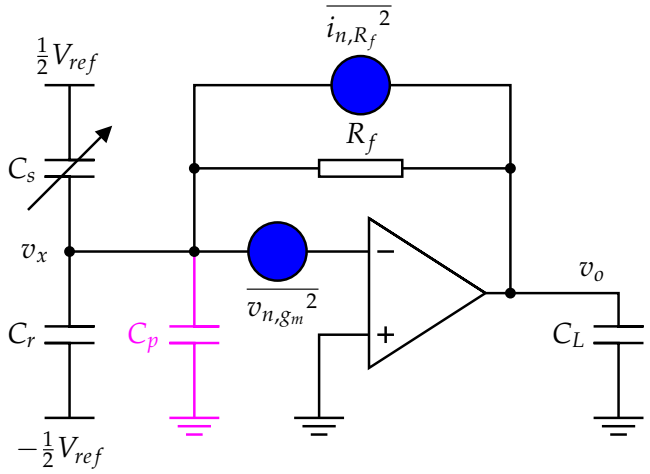


Figure 2.15: Simplified transimpedance interface circuit diagram

A nodal analysis of the circuit shown in Figure 2.15 results in

$$(\frac{1}{R_f}+s(C_s+C_r+C_p))v_x-\frac{1}{R_f}v_o=v_{n,g_m}-(\frac{1}{R_f}+s(C_s+C_r+C_p))i_{n,R_f}+\frac{V_{ref}}{2}s(C_s-C_r) \tag{2.55}$$

$$(g_m-\frac{1}{R_f})v_x+(\frac{1}{R_f}+sC_L)v_o=-i_{n,R_f}+\frac{1}{R_f}v_{n,g_m} \tag{2.56}$$

where v_{n,g_m} and i_{n,R_f} are respectively the input referred noise voltage of the amplifier and the shunt current noise source of the feedback resistor. The power spectral density of noise sources v_{n,g_m} and i_{n,R_f} is given by

$$S_{n,g_m}=\overline{v_{n,g_m}{}^2}/\Delta f=4KT\alpha\gamma/g_m, \tag{2.57}$$

$$S_{n,R_f}=\overline{i_{n,R_f}{}^2}/\Delta f=4KTR_f \tag{2.58}$$

where K is the Boltzmann's constant and T is the absolute temperature. Signal voltage at the output of the amplifier v_o is then found by solving (2.55) when $v_{n,g_m}=i_{n,R_f}=0$

$$v_o(s)=\frac{s(1/g_m-R_f)(C_s-C_r)V_{ref}/2}{1+s(C_s+C_r+C_p+C_L)/g_m+s^2R_fC_L(C_s+C_R+C_P)/g_m}. \tag{2.59}$$

According to (2.59), the signal transfer function has a zero at the origin and two

complex conjugate poles

$$\omega_0 = \sqrt{\frac{g_m}{R_f C_L (C_s + C_R + C_P)}} \tag{2.60}$$

at which the signal power is maximum which is given by

$$P_{signal} = |v_{signal}(j\omega_0)|^2 \approx (g_m R_f \frac{V_{ref}}{2\sqrt{2}} \frac{C_s - C_r}{C_s + C_r + C_p + C_L})^2. \tag{2.61}$$

Noise transfer functions (NTF) of v_{n,g_m} and i_{n,R_f} can also be found by solving (2.55) as

$$NTF_{v,n}(s) = \frac{1 + sR_f(C_s + C_r + C_p)}{1 + s(C_s + C_r + C_p + C_L)/g_m + s^2 R_f C_L (C_s + C_R + C_P)/g_m}, \tag{2.62}$$

$$NTF_{i,n}(s) = \frac{-R_f(1 + s(C_s + C_r + C_p)/g_m)}{1 + s(C_s + C_r + C_p + C_L)/g_m + s^2 R_f C_L (C_s + C_R + C_P)/g_m}. \tag{2.63}$$

Note $NTF_{i,n}(s)$ is of transimpedance nature such that it transfers the resistance current noise to the *output* noise voltage.

Theorem If a signal with power spectral density $S_{in}(s)$ is applied to a linear time-invariant system with transfer function $H(s)$, then the output power spectral density is given by [Razavi 2000]

$$S_{out}(f) = S_{in}(f)|H(f)|^2. \tag{2.64}$$

Providing that total power of a signal with the spectral density $S(f)$ is given by

$$P = \int_0^\infty |S(f)| \mathrm{d}f, \tag{2.65}$$

by using (2.57)–(2.58), (2.62)–(2.63) and (2.64)–(2.65), the total power of the noise sources v_{n,g_m} and i_{n,R_f} can be derived as

$$\overline{{v_{n,g_m}}^2} = KT\alpha\gamma \frac{1 + g_m R_f (C_s + C_r + C_p)/C_L}{C_s + C_r + C_p + C_L}, \tag{2.66}$$

$$\overline{{v_{n,R_f}}^2} = KT \frac{g_m R_f + (C_s + C_r + C_p)/C_L}{C_s + C_r + C_p + C_L}, \tag{2.67}$$

where the following integral formulae [Dastgheib 2008] are used to obtain a closed-form solution to (2.65) when deriving (2.66)–(2.67),

$$\int_0^\infty \left| \frac{1}{1+\frac{s}{\omega_0}} \right|^2 \mathrm{d}f = \frac{\omega_0}{4}, \tag{2.68}$$

$$\int_0^\infty \left| \frac{1}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}} \right|^2 \mathrm{d}f = \int_0^\infty \left| \frac{\frac{s}{\omega_0}}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}} \right|^2 \mathrm{d}f = \frac{\omega_0 Q}{4}, \tag{2.69}$$

$$\int_0^\infty \left| \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}} \right|^2 \mathrm{d}f = \frac{\omega_0 Q}{4}\left(\frac{\omega_o^2}{\omega_z^2}+1\right). \tag{2.70}$$

Since the two available noise sources are uncorrelated the total noise power at the output of the amplifier is readily

$$\overline{v_{n,T}{}^2} = \overline{v_{n,g_m}{}^2} + \overline{v_{n,R_f}{}^2}. \tag{2.71}$$

The last consideration is that the output of the OTA must always remain within its available output voltage swing, otherwise it saturates and causes excessive non-linearity. Thus,

$$v_{signal} = g_m R_f \frac{V_{ref}}{2} \frac{C_s - C_r}{C_s + C_r + C_p + C_L} \leq \frac{V_{swing,pp}}{2} \tag{2.72}$$

where $V_{swing,pp}$ is the available peak-to-peak voltage swing at the output of the amplifier.

Finally by using (2.61) and (2.71), SNR can be expressed by

$$SNR = \frac{V_{swing,pp}^2 (C_T + \frac{g_m}{\omega_0^2 R_f C_T})}{8KT(\alpha\gamma + g_m R_f + \frac{\omega_0^2 R_f C_T^2}{g_m} + \alpha\gamma\omega_0^2 C_T^2 R_f^2)}, \tag{2.73}$$

where $C_T = C_s + C_r + C_p$ is the total capacitance seen into the virtual ground node. In (2.72), g_m can be factored out

$$g_m = \frac{C_T}{\frac{V_{ref}}{V_{swing,pp}} R_f \Delta C - \frac{1}{R_f C_T \omega_0^2}} \tag{2.74}$$

and replaced in (2.73) to generate a bi-quadratic equation of variable R_f

$$aR_f^4 + bR_f^2 + c = 0, \tag{2.75}$$

where a, b and c are

$$a = (C_T\omega_0)^4 \left(\frac{V_{ref}}{V_{swing,pp}}\frac{\Delta C}{C_T}\right)\left(\frac{V_{ref}}{V_{swing,pp}}\frac{\Delta C}{C_T} + \gamma\right), \tag{2.76}$$

$$b = (C_T\omega_0)^2 \left(1 - \gamma + \frac{V_{ref}}{V_{swing,pp}}\frac{\Delta C}{C_T}\left(\gamma - 2 - \frac{V_{swing,pp}^2 C_T}{8KTSNR}\right)\right), \tag{2.77}$$

$$c = 1 - \gamma. \tag{2.78}$$

For a given SNR and V_{ref}, (2.75) can be numerically solved for R_f. Consequently, substitution of the obtained R_f in (2.74) and (2.60) gives the corresponding values of g_m and C_L respectively and the design is complete.

To arrive at a minimum interface power consumption, for a given SNR, V_{ref} is swept and corresponding values of R_f, g_m and C_L are calculated as explained above. The power consumption of an amplifier working in the subthreshold regime is given by (2.29). The power supplied by the sinusoidal source in the half-bridge driver can be expressed by

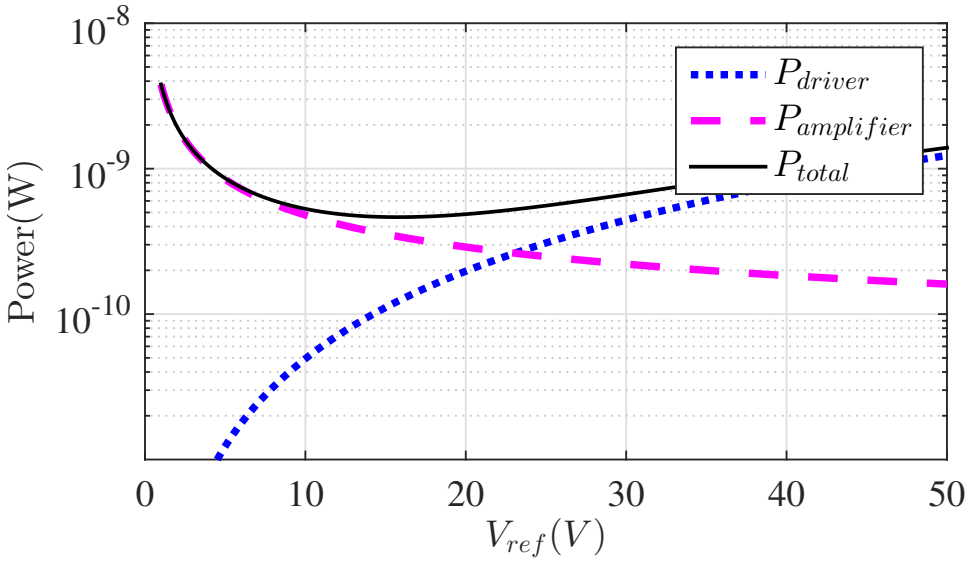
$$P_{driver} = \frac{V_{ref}^2}{8R_s}\left(\frac{(\omega R_s C_s)^2}{1 + (\omega R_s C_s)^2} + \frac{(\omega R_s C_r)^2}{1 + (\omega R_s C_r)^2}\right), \tag{2.79}$$

where R_s is the internal resistance of the voltage source and ω is the driving frequency. Obviously, as discussed above there exists an optimal driving frequency ω_0 expressed in (2.60) at which the SNR is maximised. Therefore in (2.79), $\omega = \omega_0$. Also evident from (2.79), the power consumption of the driving subsystem in this case is a function of R_s. Finding the optimal solution for a range of R_s values shows that the optimal power consumption of the interface is indeed a weak function of R_s (see Figure 2.17a). Therefore, to make the analysis consistent with other architectures the minimum R_s is chosen for comparison purposes.

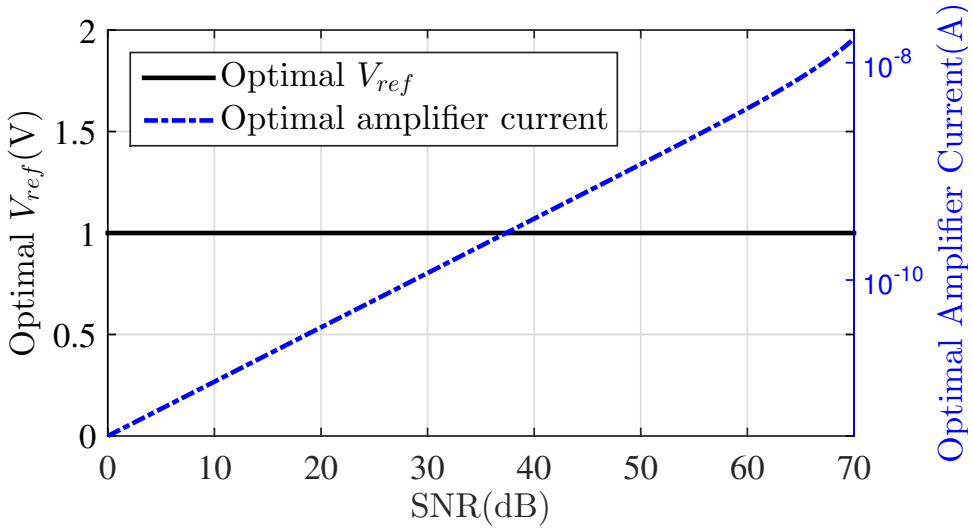
Using (2.73)–(2.79), similar plots to those of the switched-capacitor CVC and the SAR CDC, can be obtained for the transimpedance capacitance to voltage converter (TI CVC) as shown in Figures 2.16 and 2.17. These figures will be used as performance metrics of the TI CVC to compare it with other interfaces.

2.2.7 Slope interface: continuous-time variant

Comparator-based slope capacitive sensor interfaces should also be considered among low-power sensor interfaces. On the one hand, the slope interface relies on comparator and not power-hungry OTAs. Moreover, the architecture complexity is relaxed as it is comprised of only few elements. Avoiding complexity by designing



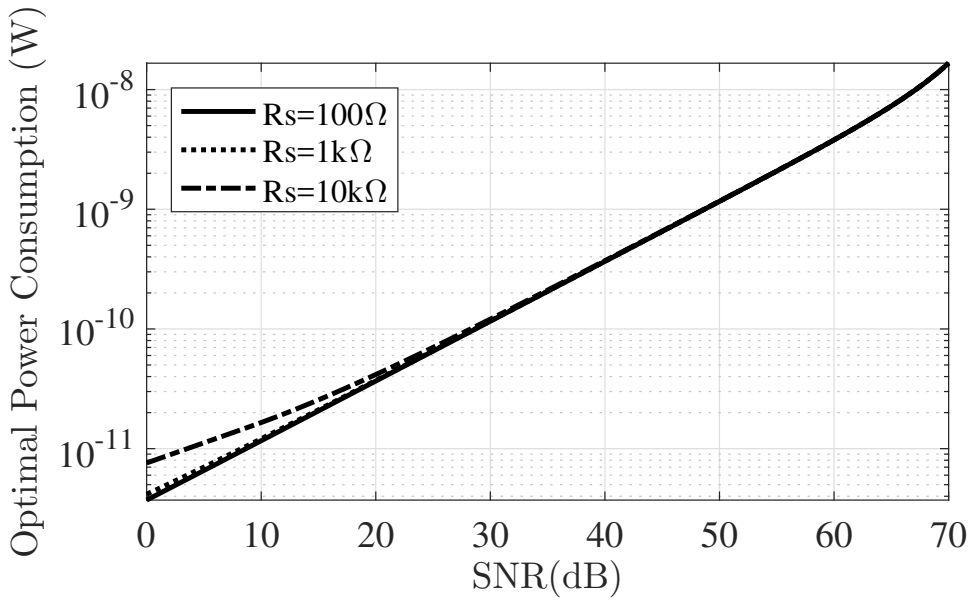
(a) Power management of sub blocks of the TI CVC for the case of 60dB SNR



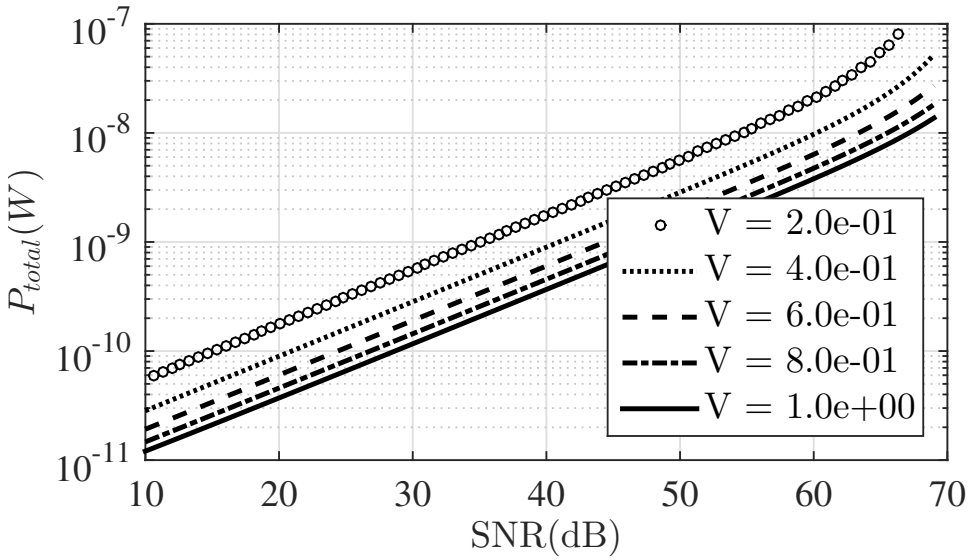
(b) Optimal V_{ref} and amplifier current

Figure 2.16: Demonstration of presence of optimal power management

systems with as few elements and operational phases as possible is an excellent low-power-design practice. On the other hand, this interface offers a quasi-digital, e.g. Pulse Width Modulation (PWM) or Pulse Period Modulation (PPM), representation of the sense capacitance. This is particularly important for bio-sensing applications when the power consumption of wireless data transmission should also be considered in the design phase. Efficient data transmission protocols lend themselves more easily to quasi-digital data. That is this type of output can result in minimum number of bits for data transmission. For instance in the case of PPM,



(a) Lower bound on P_{total}



(b) Total power consumption of the TI CVC for different driving voltages

Figure 2.17: Noise-power optimization of TI CVC

since information is modulated in time with respect to a reference time, wireless transmitter needs to transmit only one pulse for each word, rather than sending N bits of data. In such cases, at the receiver data can be simply digitised by the use of a counter whose frequency determines the number of digitisation steps. Lastly, although quasi-digital data minimises the required bandwidth of the transceiver,

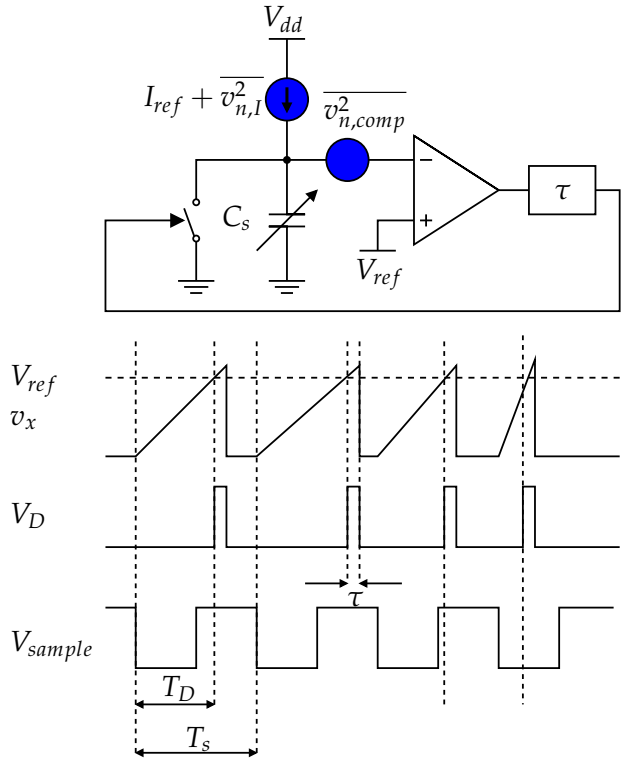


Figure 2.18: Simplified diagram of the time-based capacitive sensor interface

since the data is not yet digitised prior to transmission, it is prone to both transceiver and channel noise. Nonetheless, for low data-rate sensor applications and medium bit-error rate the slope-interface sensor front-end can potentially be the architecture of interest.

A simplified circuit diagram of the slope interface is shown in Figure 2.18. In contrast to the previously discussed interfaces, the reference capacitor of this topology is implicit to the design by means of a reference current source, reference voltage and the sampling period. The sense capacitor is initially discharged by the reset switch. At the falling edge of the sampling clock, the switch opens and the capacitor is linearly charged by a reference current source I_{ref}. The time it takes the capacitor to charge up to the reference voltage V_{ref},

$$T_D = \frac{C_s V_{ref}}{I_{ref}}, \tag{2.80}$$

is captured by the comparator. That is, for the known reference voltage and current, the sensor capacitance is transferred to the time domain and can be digitised by a decimation filter, e.g. counter. The larger the sensor capacitance, the longer it takes it to charge to the reference voltage. As the conversion time is bound to the

sampling period T_s, for the maximum sense capacitance (2.80) can be rewritten as

$$T_s = \frac{C_{s,max} V_{ref}}{I_{ref}}. \tag{2.81}$$

As soon as the sense capacitor voltage exceeds V_{ref}, the output of the comparator toggles to logic High. The output of the comparator controls the state of the reset switch through a delay cell, meaning that after τ seconds the switch is closed, and the sense capacitor is discharged. The switch remains connected until the next rising edge of the sampling clock. Thus, the decimation period is controlled by the falling edge of the sampling clock and the rising edge of the output of the comparator. The delay is necessary to ensure the decimation filter is given enough time to reliably detect the rising edge of V_D and consequently the end of the decimation period.

The interface shown in Figure 2.18 is an excellent circuit level example of the generic interface previously shown in Figure 2.1 by which the trade-off between the power consumption of the signal conditioning block (comparator in this case) and the input-referred noise $\overline{v_n^2}$ can be well explained. In other words, it will be shown that how increasing the power budget of the comparator decreases the input noise and hence increases the SNR. As the input noise is dominated by the input referred noise of the comparator which itself is a strong function of the topology of the comparator, the discussion can be divided into two main streams, continuous and discrete. In the former, a continuous-time comparator detects the end of decimation period. In this stream, the comparator consumes static power. On the other hand, in the discrete-time slope interface, discussed in the next sub-section, a latch (dynamic) comparator is clocked just before the rising edge of the counter (decimator) clock, to detect whether the capacitance voltage has reached the threshold or not. Intuitively, this latter choice should be more energy efficient as the comparator makes the comparison (and hence consumes dynamic power) at only certain times.

To understand the noise-power trade-off, the simplest continuous-time comparator, a differential amplifier shown in Figure 2.19, is analysed first. Further modifications to this comparator and related analyses come next. The noise power spectral density of the input pair devices $8KT\gamma/g_m$ directly appears at the input which then adds up to that of the resistors referred to the input $8KT/g_m^2 R$. Providing that the bandwidth of this single-pole system is $1/RC$, the total input referred noise power is given by

$$\overline{v_n^2} = \frac{2KT}{g_m RC}\left(\gamma + \frac{1}{g_m R}\right). \tag{2.82}$$

Clearly, the input referred noise power is a function of C, R and g_m. Increasing

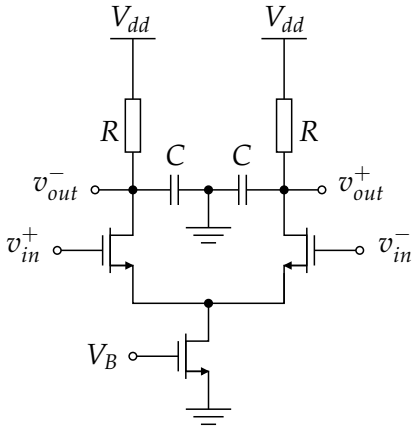


Figure 2.19: Circuit diagram of a simple differential amplifier operating as a continuous time comparator

any of these design parameters decreases the input referred noise power. As an example, if the capacitor value increases, in order to maintain the bandwidth, the resistor value must decrease proportionally. On the other hand, reducing the resistor value decreases the DC gain, and thus the transconductance must increase proportionally for compensation of the gain loss. Therefore, eventually, to decrease the input referred noise more heat (current) must dissipate [Razavi 2000]. The same conclusion holds if the other parameters are initially chosen to reduce the input referred noise. So, this simple example illustrates how noise and power consumption of the signal conditioning block trade with each other and that how the SNR of the interface can be increased solely by allocating more power to the conditioning block.

The comparator of the interface must meet certain gain-bandwidth specifications for flawless capacitive digitisation. It must be able to compare voltages as small as the LSB ($V_{ref}/2^N$) of the interface within a required time ($T_s/2^N$). Thus the gain A_v and bandwidth ω_{-3dB} of the comparator must respectively be

$$A_v = 2^N \frac{V_{dd}}{V_{ref}}, \tag{2.83}$$

$$\omega_{-3dB} = 2^N \frac{5}{T_s}. \tag{2.84}$$

For medium to high resolution applications, (2.83) and (2.84) can hardly be met even by a well-designed OTA. One solution is a k-stage cascade of low-gain high-speed differential amplifiers as shown in Figure 2.20. The gain and bandwidth of

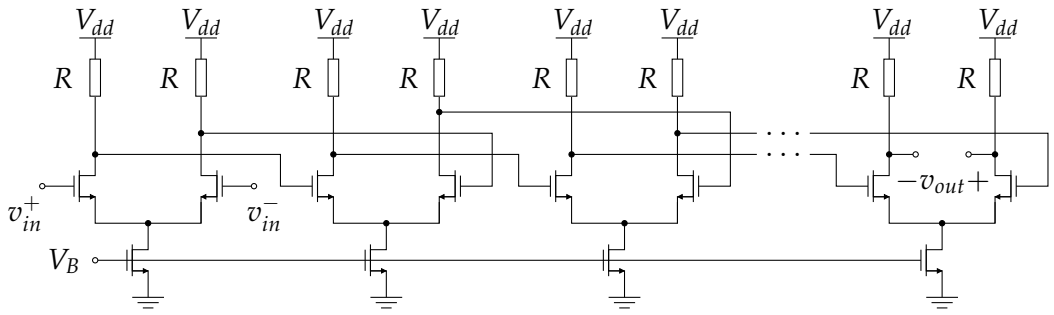


Figure 2.20: A continuous time comparator realised by cascades of k differential amplifiers to meet the gain-bandwidth requirements

this comparator can be easily obtained as

$$A_v = A_0^k = (g_m R)^k, \tag{2.85}$$

$$\omega_{-3dB} = \omega_{-3dB,0}\sqrt{2^{1/k}-1} = \frac{\sqrt{2^{1/k}-1}}{RC}, \tag{2.86}$$

where A_0 and $\omega_{-3dB,0}$ are respectively the gain and bandwidth of one of the stages.

The total input referred noise of the k-stage comparator shown in Figure 2.20 is the sum of the input referred noise of each stage when referred to the input, that is

$$\overline{v_{n,comp}^2} = \overline{v_n^2}\left(1 + \frac{1}{A_0^2} + \frac{1}{A_0^4} + \cdots + \frac{1}{A_0^{2k-2}}\right) = \overline{v_n^2}\frac{1 - Av^{-2}}{1 - A_v^{-2/k}} \tag{2.87}$$

where $\overline{v_n^2}$ is the input-referred noise power of each stage given by

$$\overline{v_n^2} = \frac{2KT}{g_m/\omega_{-3dB,0}}\left(\gamma + \frac{1}{A_0}\right) = \frac{2KT\omega_{-3dB}}{g_m\sqrt{2^{1/k}-1}}\left(\gamma + \frac{1}{A_v^{1/k}}\right). \tag{2.88}$$

Equations (2.87) and (2.88) describe the input referred noise of the comparator based on the required gain and bandwidth defined by the resolution and speed of the interface, (2.83) and (2.84), however there are two more noise contributors in the slope interface. One is the switch noise voltage that the sensing capacitor samples and stores at the time the discharging switch opens, known as KT/C noise. The other noise is sourced by the noisy current source that charges the sense capacitor, known as Random Walk noise. This noise power of the latter contributor is a linear function of time and can be expressed by

$$\overline{v_{n,I}^2} = \frac{t}{2C_s^2}S_i(f) \tag{2.89}$$

where it is assumed the current source is a single transistor biased in the subthreshold region whose noise power spectral density is

$$S_i(f) = 4KT\gamma g_m = \frac{4q\gamma I_{ref}}{\zeta}. \tag{2.90}$$

Evident from (2.89) is that $\overline{v_{n,I}^2}$ linearly increases with time. So, it must be evaluated just before the comparison is being made, that is, from (2.81) $t = T_s$, so (2.89) takes the form of

$$\overline{v_{n,I}^2} = \frac{2q\gamma V_{ref}}{\zeta C_s}. \tag{2.91}$$

Finally, the total noise power at the input of the comparator is the sum of all available noise powers

$$\overline{v_{n,total}^2} = \overline{v_{n,comp}^2} + \overline{v_{n,I}^2} + \frac{KT}{C_s}. \tag{2.92}$$

Therefore, the SNR can be derived by dividing the signal power at the time the comparison is being made by the comparator, V_{ref}^2, by (2.92). In other terms,

$$\overline{v_{n,comp}^2} = \frac{V_{ref}^2}{SNR} - \overline{v_{n,I}^2} - \frac{KT}{C_s}. \tag{2.93}$$

Thus, the required transconductance of the comparator as a function of SNR, V_{ref}, can be expressed by

$$g_m = \frac{\frac{2KT\omega_{-3dB}}{\sqrt{2^{1/k}-1}}\left(\gamma + \frac{1}{A_v^{1/k}}\right)\frac{1-A_v^{-2}}{1-A_v^{-2/k}}}{\frac{V_{ref}^2}{SNR} - \frac{2q\gamma V_{ref}}{\zeta C_s} - \frac{KT}{C_s}} \tag{2.94}$$

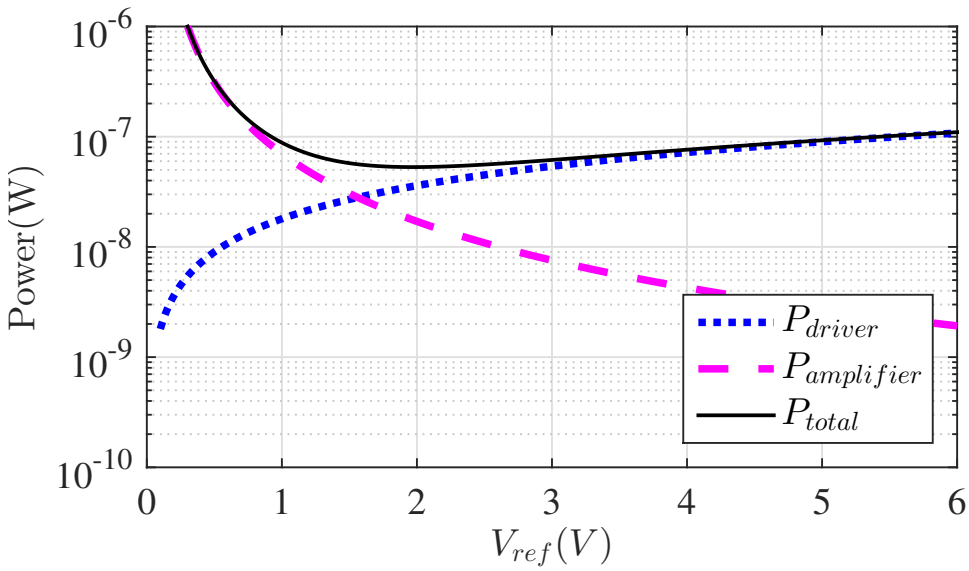
The power consumption of each stage of the comparator can be related to its g_m through (2.29), and the total power consumption of the k-stage comparator is

$$P_{comparator} = 2k\zeta V_T V_{dd} g_m. \tag{2.95}$$

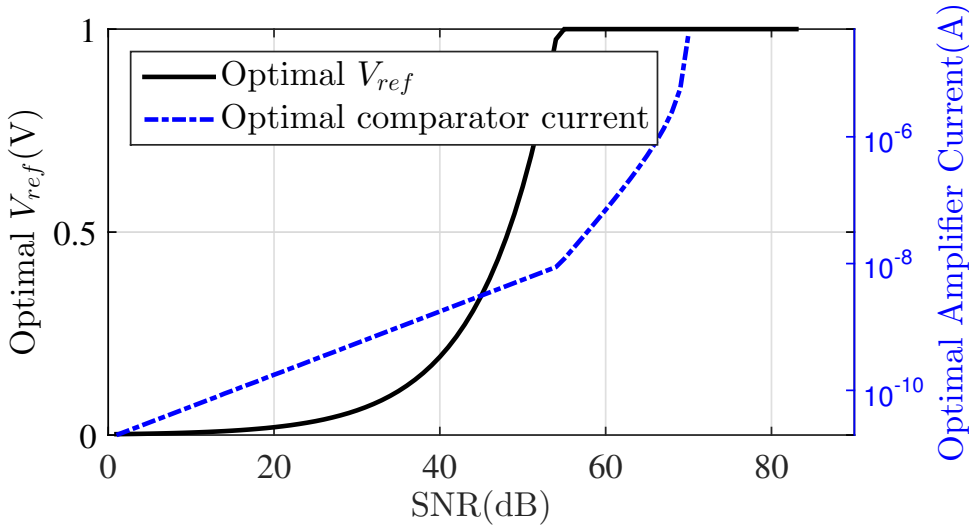
On the driving side, the analysis is more straightforward. The driver consists of only the reference current source whose power consumption is simply given by

$$P_{driver} = I_{ref} V_{dd} = \frac{C_{s,max} V_{ref} V_{dd}}{T_s}. \tag{2.96}$$

And finally, the total power consumption of the interface as a function of SNR and



(a) Power management of sub blocks of contiuous-time slope interface for the case of 60dB SNR



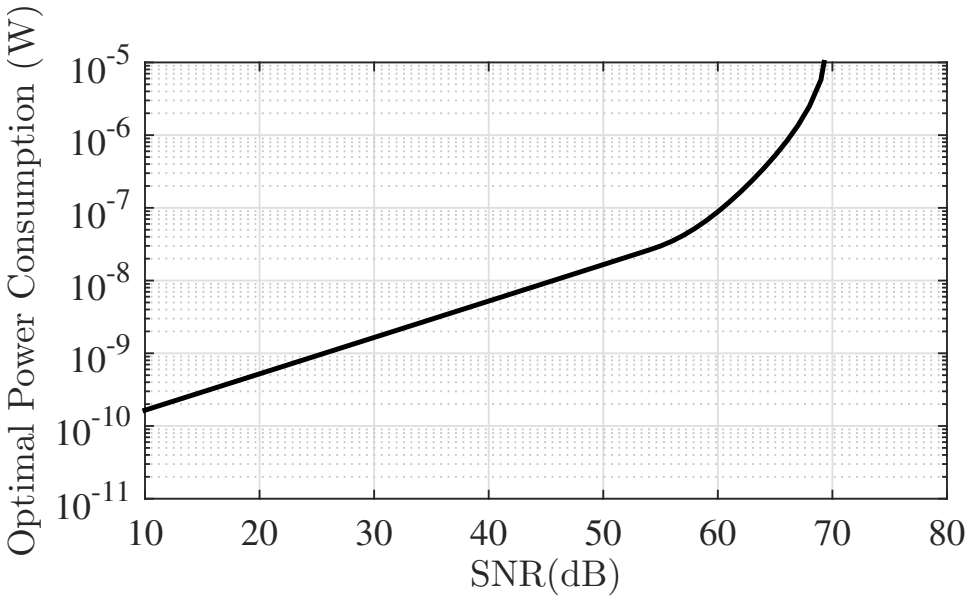
(b) Optimal V_{ref} and amplifier current

Figure 2.21: Demonstration of presence of optimal power management

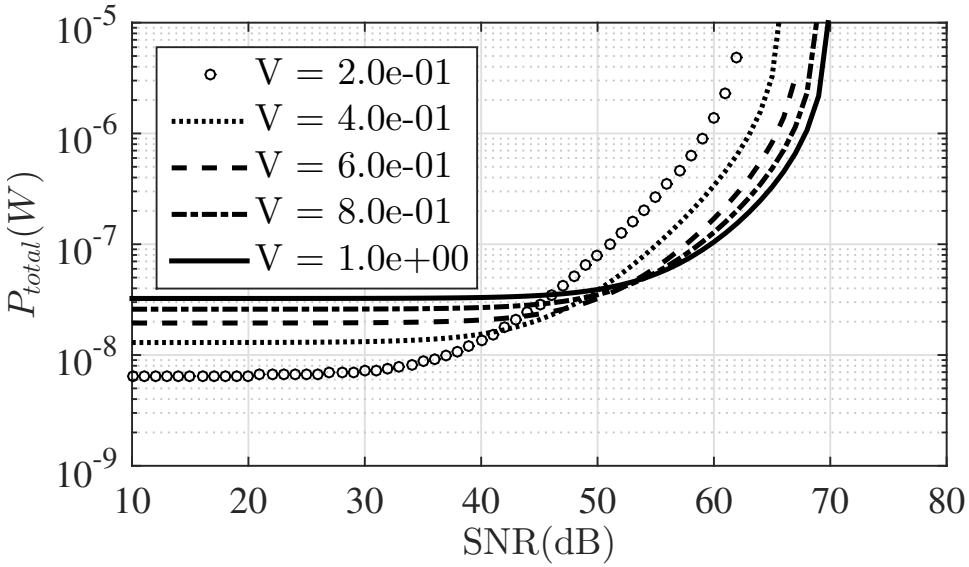
V_{ref} is

$$P_{total} = P_{driver} + P_{comparator}. \tag{2.97}$$

For a given SNR and sampling frequency, e.g. 60dB at 1000Hz, the reference voltage can be swept and the power consumption associated with the driver and the comparator can be calculated and plotted using (2.95) and (2.96), Figure 2.21a. This plot demonstrates, for this specific SNR, the total power consumption of the



(a) Lower bound on P_{total}



(b) Total power consumption of the continuous-time slope interface different driving voltages

Figure 2.22: Noise-power optimization of continuous-time slope interface

interface is minimised by $V_{ref} = 1.96$ [V]. Such optimal bias points as functions of SNR values are plotted in Figure 2.21b. From another perspective, the total power consumption can be plotted when SNR is swept for certain values of V_{ref}, Figure 2.22b. As already discussed for previous interfaces, this plot clearly reveals that for instance for SNR values smaller than 40dB, driving the sensor with all the available voltage headroom is energy inefficient, and for maximum energy efficiency the

sensor should be driven at $V_{ref} = 0.192$ [V]. Similar to other interfaces discussed earlier, this last figure can be plotted for a finer resolution of reference voltages as shown in Figure 2.22a.

2.2.8 Slope interface: discrete-time variant

This section is an extension to the discussion of the slope capacitive interface which aims at investigating whether the discrete-time slope capacitive interface is more energy-efficient than its continuous-time counterpart or not. The working principles of the discrete-time capacitive interface is exactly the same as that discussed in the previous section except for the fact that the comparator is of a different type; dynamic (latch) comparator. The idea behind this modification is the comparison of the sensing capacitor voltage and the reference voltage needs to be made just before the counter ticks, and thus continuous comparison is wasteful energy-wise. In other words, as the capacitance voltage is always increasing, it is sufficient to just compare its voltage with the reference voltage just before the rising edge of the counter clock. In this scenario, the dynamic comparator consumes only 2^N packets of charge for every comparison, where N is the required resolution. This is in contrast to the static power consumption of continuous time comparators.

The derivation of the input referred noise power of dynamic comparators due to their time-varying nature is not straightforward. Therefore, to greatly simplify the noise analysis of this section a reference dynamic comparator, known as StrongArm, shown in Figure 2.23 is chosen whose input referred noise power is reported in [Nuzzo 2008]. The operating principles of this comparator can also be found in [Nuzzo 2008].

According to [Nuzzo 2008], For a well-designed latch comparator, the input referred noise power of the comparator shown in Figure 2.23 can be accurately estimated by

$$\overline{v_{n,comp}^2} = \frac{2KT\gamma V_{OD,1}}{C_x V_{Th,B}} \tag{2.98}$$

where $V_{OD,1}$ and $V_{Th,B}$ are respectively the overdrive voltage of the input pair devices and the threshold voltage of the tail current source, and C_x is the total capacitance at the drains of the input pair devices and output nodes. In the previous section, the total noise power at the input of the comparator was derived as (2.92). Substituting (2.98) in (2.92) and factoring out C_x yields

$$C_x = \frac{2KT\gamma V_{OD,1}/V_{Th,B}}{\frac{V_{ref}^2}{SNR} - \frac{4q\gamma V_{ref}}{\zeta C_s} - \frac{KT}{C_s}}. \tag{2.99}$$

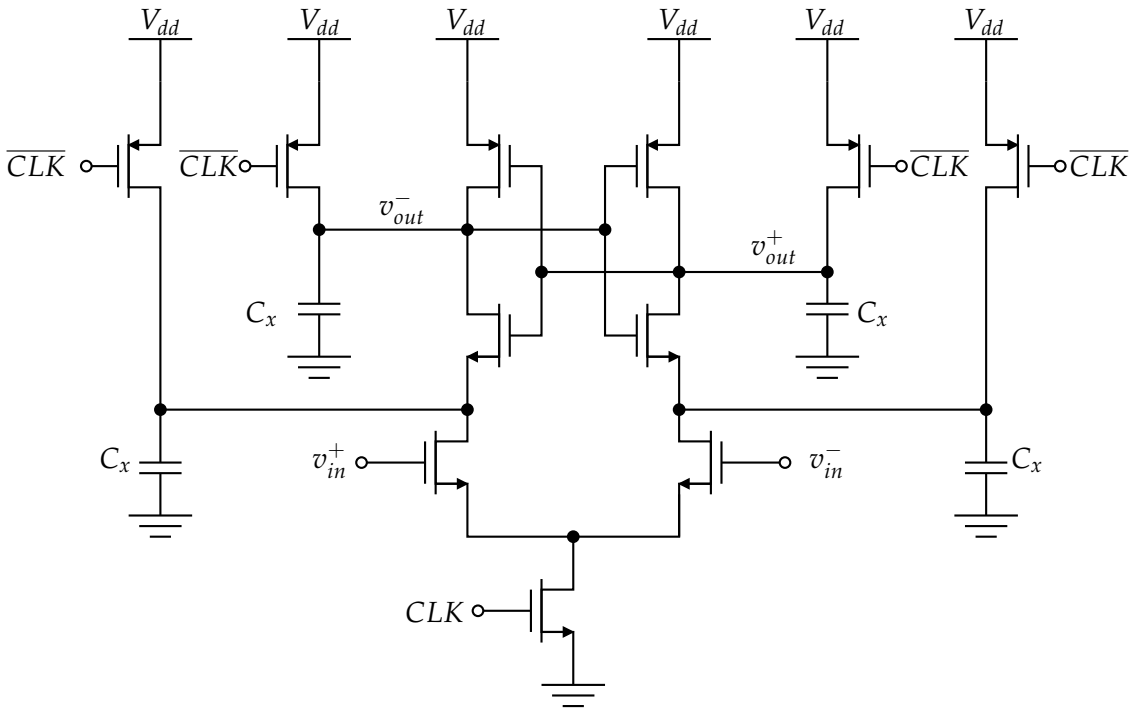


Figure 2.23: Dynamic latch comparator

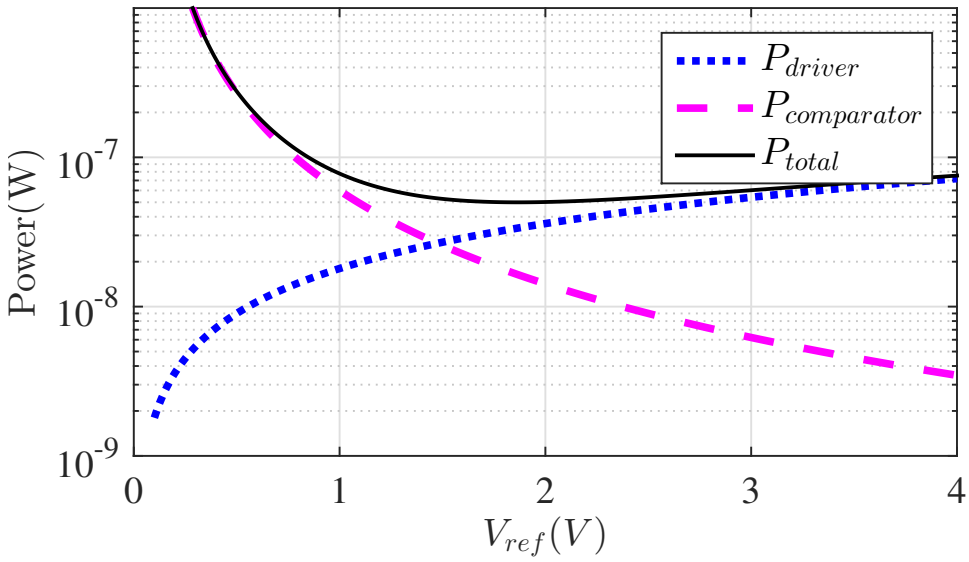
For every comparison, all the four capacitors C_x in the reference dynamic comparator are pre-charged to V_{dd}. Although, one of the output capacitors is first almost half-discharged and then charged up to V_{dd} during the comparison, as the worst case all the capacitors are considered fully discharged and hence the total energy associated with each comparison is

$$E = 4C_x V_{dd}^2. \tag{2.100}$$

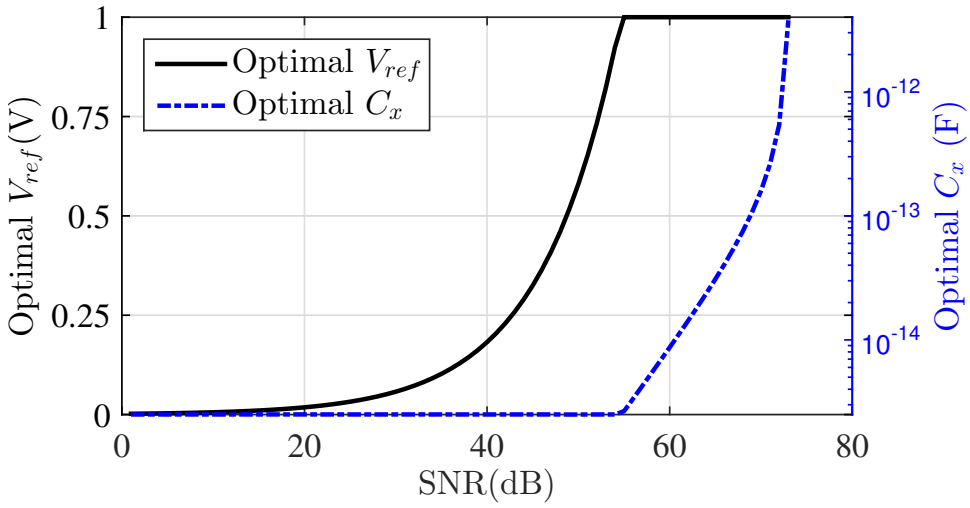
An N-bit interface requires 2^N comparisons to be made by the comparator in T_s seconds. Thus, the power consumption of the comparator for each conversion period can be derived as

$$P_{comparator} = 2^{N+2} V_{dd}^2 f_s \frac{2KT\gamma V_{OD,1}/V_{Th,B}}{\frac{V_{ref}^2}{SNR} - \frac{4q\gamma V_{ref}}{\zeta C_s} - \frac{KT}{C_s}}. \tag{2.101}$$

The power consumption of the driver is the same as that of the continuous time interface which is given by (2.96). The total power consumption of the interface



(a) Power management of sub blocks of the discrete-time slope interface for the case of 60dB SNR



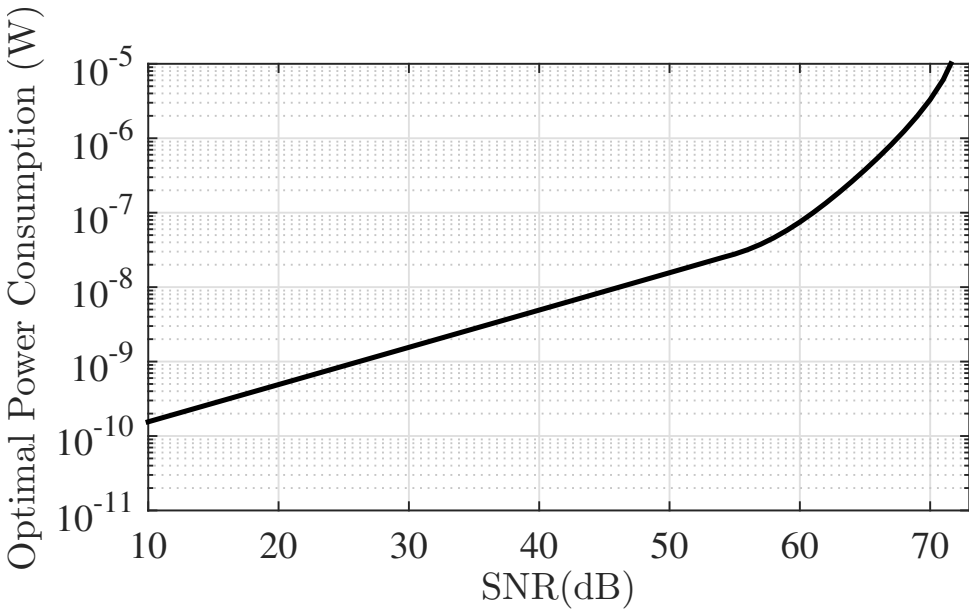
(b) Optimal V_{ref} and comparator capacitance

Figure 2.24: Demonstration of presence of optimal power management

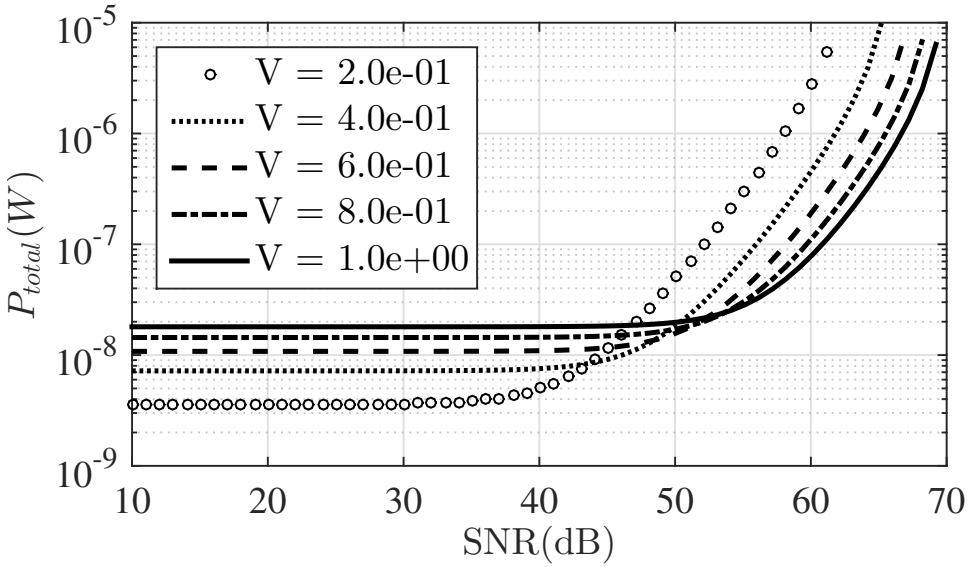
will then be the sum of (2.96) and (2.101) as

$$P_{Total} = 2^{N+2} V_{dd}^2 f_s \frac{2KT\gamma V_{OD,1}/V_{Th,B}}{\frac{V_{ref}^2}{SNR} - \frac{4q\gamma V_{ref}}{\zeta C_s} - \frac{KT}{C_s}} + \frac{C_{s,max} V_{ref} V_{dd}}{T_s} \tag{2.102}$$

This final equation can be used to generate a similar set of figures similar to previously analysed architectures as shown in Figures 2.24 and 2.25. These figures along with Figures 2.7, 2.8, 2.11, 2.12, 2.21 and 2.22 are optimal noise-power



(a) Lower bound on P_{total}



(b) Total power consumption of the discrete-time slope interface different driving voltages

Figure 2.25: Noise-power optimization of discrete-time slope interface

characteristics of the discussed sensor interface architectures which will be critically analysed in the next section.

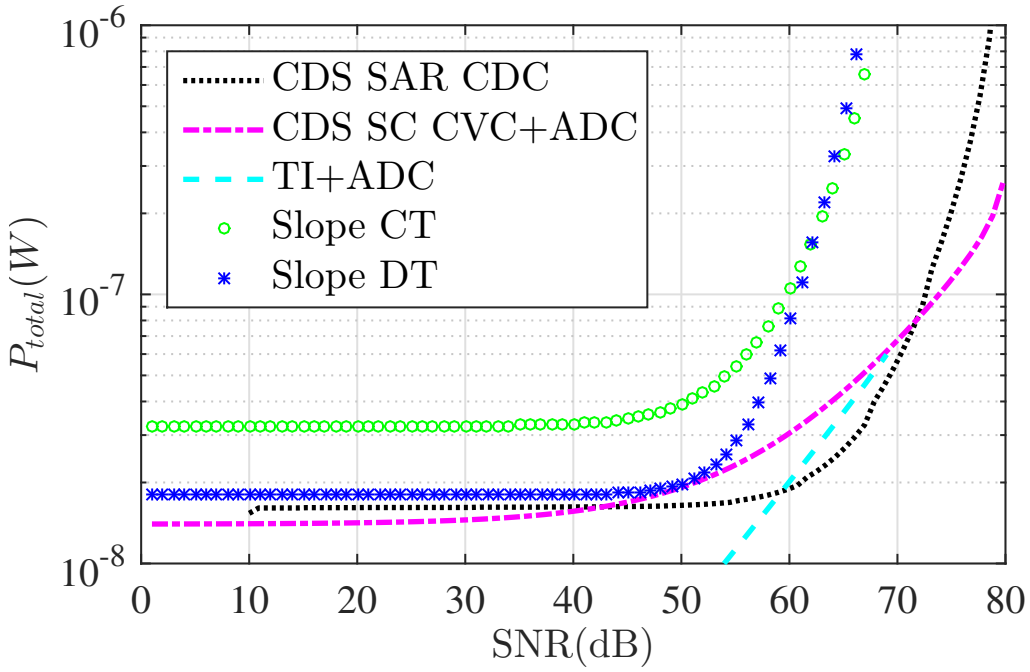


Figure 2.26: Power consumption comparison of the analysed sensor interface architectures. The ADC used in this comparison is assumed to have a FOM of 10fJ/conversion-step.

2.2.9 Critical analysis II

In this section, five sensor interface architectures, namely switched-capacitor capacitance to voltage converter (SC CVC), successive approximation register capacitance to digital converter (SAR CDC), transimpedance amplifier (TI), continuous-time and discrete-time slope-based capacitance to digital converters, were analysed with respect to their optimal power consumption. In subsection 2.2.5, the power consumption of correlated double sampling (CDS) SC CVC and SAR CDC were compared. It was concluded that for small C_p and moderate SNR (<72dB) the SAR CDC is more energy-efficient than the SC CVC. Here the comparison is extended to include the other three architectures.

The slope converters output thermometer-coded digital codes, whereas the output of the transimpedance amplifier must be down-converted by a mixer, low-pass filtered and then digitised. Therefore, when considering the power consumption of the TI interface for comparison, the power consumption of the mixer, LPF and the ADC must also be included. Shown in Figure 2.26 is the minimum achievable power consumption of the analysed interfaces when $V_d = 1$ and $C_p = 1pF$.

The power consumption of the discrete-time slope interface is slightly lower than that of the continuous-time slope interface. This is well in-line with intuition,

that is the latch-comparator in the DT slope interface draws packets of charge from V_{dd} for each conversion and is idle between comparison times, whereas the continuous-time comparator of the CT slope interface consumes static flows of charge. Moreover, evident from Figure 2.26 is the CDS SC CVC and SAR CDC are unconditionally more energy-efficient than the slope converters.

For effective benchmarking, it suffices to only include the power consumption of the ADC to that of the transimpedance amplifier, even though the mixer and active LPF consume substantial amount of energy. The ADC considered for the TI interface has the same level of energy-efficiency used for the SC CVC, that is 10fJ/conversion-step. The TI interface for low SNR consumes the least amount of energy among all the other architectures. However, for moderate SNR (60<SNR<75) and high SNR (<75) the SAR CDC and the SC CVC respectively outperform the TI interface, and should be opted accordingly.

2.3 Conclusion

In this chapter, a holistic noise-power optimisation technique was introduced which theoretically calculates the minimum power consumption of a given sensor interface when associated power consumption of generating an arbitrary voltage is negligible. In a more realistic case, where the sensors are driven by the supply voltage, the proposed technique finds the minimum achievable power consumption for a given SNR. This optimisation technique was applied to five sensor interfaces to enable a comparison between their energy efficiencies. For moderate SNR and small sensor-interface interconnection parasitic capacitance it was concluded that the CDS SAR CDC is the optimal choice. An integration technique is proposed in the next chapter that minimizes the interconnection parasitic capacitance. Also, moderate SNR($\sim 60dB$) is required for ICP monitoring. Therefore, based on the conclusion made in this chapter, a CDS SAR CDC is chosen for sensor interfacing electronics. Design considerations of this CDS SAR CDC are detailed in chapter 3.

CHAPTER 3

Sensor Design

Summary

A capacitive pressure sensor can be considered as two conductive parallel plates. One of the plates is fixed, while the other is clamped along the edges and is exposed to ambient pressure. As a result of deflection of the exposed plate towards the fix plate the capacitance increases. Since the capacitance is a function of the deflection of the bending plate, characterising the sensor requires some basic knowledge of theory of plates and membranes. The realization of the capacitive transducer in Invensense MEMS process and the motivation behind this heterogeneous integration are discussed in the next section. Moreover, a brief summary of the governing equations of plate displacements is introduced in section 3.2. Timoshenko's solution for the deflection of thin plates with built-in edges is presented to gain insight to the mechanical behaviour of the membrane. Even though the accuracy of this model is inferior to those treating the plate in a full 3D model, e.g. Mindlin-Reissner, it provides a priceless insight into how (and to what extent) different parameters of the plate affect the deflection profile. A short discussion on full 3D modelling of plates and the principle of virtual work which forms the basis of any FEM solver are also presented in section 3.2. And lastly, design considerations of the membrane for this specific application are discussed and simulation results are presented in section 3.3.

3.1 Motivation

Wire bonding external pressure transducers to the sensor interface IC is the traditional way of realizing a pressure sensing system [Ha 2014, Tanaka 2007]. This inevitably enforces a large parasitic interconnection capacitance C_p which needs to be either bypassed by an SC CVC or tolerated by increasing the dynamic range of the interface, e.g. SAR CDC, to avoid interface saturation. As discussed in the previous chapter, either of these solutions, however, trades off with the power consumption. Therefore realizing an energy-efficient pressure sensing system commands minimizing C_p.

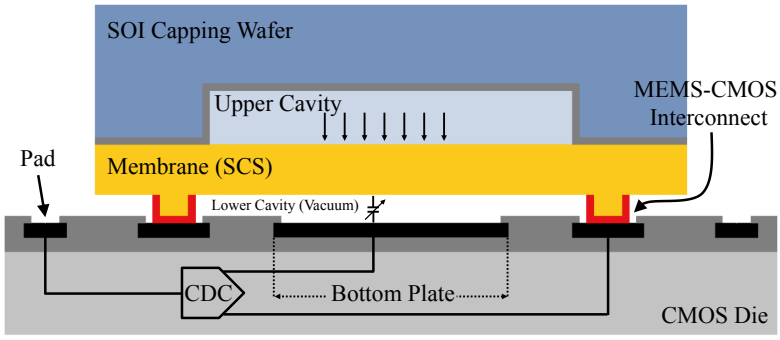


Figure 3.1: sensor-CMOS heterogeneous integration realized in Invensense process

Sensor-CMOS heterogeneous integration, first presented in [Ghanbari 2015, Ghanbari 2017], is the key solution to restrain C_p. A cross section of this integration type realized in Invensense MEMS-CMOS process [Seeger 2010] is shown in Figure 3.1. This process offers eutectic bonding of a device wafer (including the sense membrane and the capping wafer) and a CMOS wafer. The top metal layer in the CMOS wafer is designated to serve as the bottom plate of the sense capacitor. Thanks to the wafer-level bonding of the device and the CMOS wafers, the parasitic interconnection capacitance is limited to only the parasitic capacitance between the bottom plate of the sense capacitor (top metal layer of the CMOS) and the ground Silicon substrate. This capacitance can be easily estimated by knowing the dielectric constants and heights of the passivation layers sandwiched between the top-metal layer and the Silicon substrate. Designed for maximum sensor sensitivity (see below) the dimensions of the bottom plate of the sense capacitor are $460 \times 460 \mu m^2$, and the dielectric constants and heights of the sandwiched passivation layers are well documented in the process description. In total, there is a stack of 11 passivation layers resulting in a series interconnection of 11 capacitors whose values are 39.3pF ($\times 5$), 5.86pF ($\times 5$) and 8.81pF ($\times 1$). Thus, C_p is estimated

$$C_p = \frac{1 \times 10^{-12}}{\frac{5}{39.3} + \frac{5}{5.86} + \frac{1}{8.81}} = 0.91 \times 10^{-12}(F) \tag{3.1}$$

which is 55 times smaller than the parasitic capacitance reported in [Tanaka 2007]. This C_p is small enough to leverage the energy-efficient CDS SAR CDC as the interface whose implementation is presented after a short discussion on the membrane design.

3.2 Background

3.2.1 Kirchhoff-Love Model

This model is accurate for the deflection of plates whose thickness t to side length L ratio is smaller than 5% ($t/L < 5\%$) [Bucalem 2011]. Thus, the model simply assumes the plate deflection is negligible to the thickness of the plate. It also assumes that straight material lines which are initially orthogonal to the mid-surface of the plate will remain straight and orthogonal to the deformed mid-surface [Bucalem 2011]. Under these assumptions, the partial differential equation explaining the deflection profile of the plate at the point (x, y), $w(x, y)$ under a uniformly distributed applied pressure P is given by Lagrange equation

$$\frac{\partial^4 w}{\partial x^4} + 2\frac{\partial^4 w}{\partial x^2 \partial y^2} + \frac{\partial^4 w}{\partial y^4} = \frac{P}{D}, \tag{3.2}$$

Where D is the flexural rigidity of the plate defined by

$$D = \frac{Et^3}{12(1-\nu^2)}, \tag{3.3}$$

where E and ν are Young's modulus and Poisson's ratio of the material of the plate, respectively. For a given plate under pressure P, the integration above must be solved for given boundary conditions. As the plate of interest in a capacitive sensor is clamped at all the edges, the boundary conditions are the followings

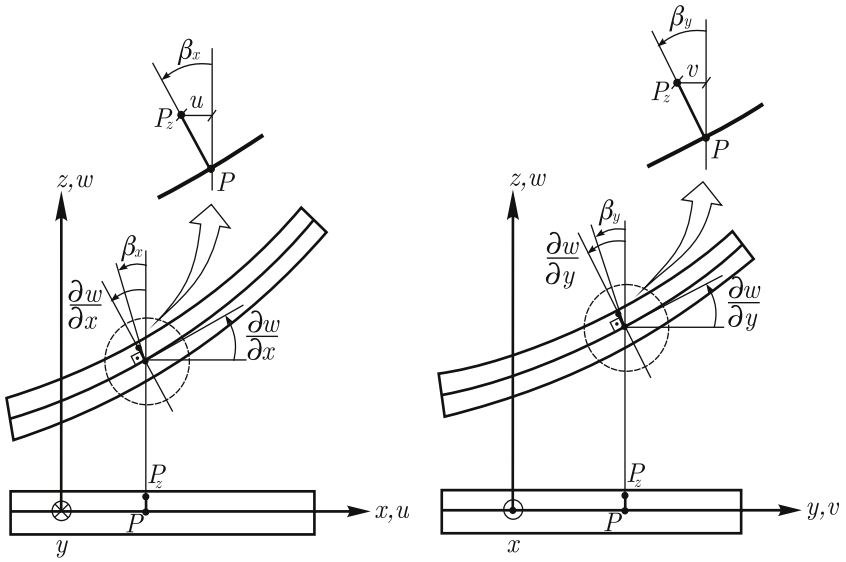
$$w\left(x = \pm\frac{L}{2}\right) = w\left(y = \pm\frac{L}{2}\right) = 0 \tag{3.4}$$

$$\frac{\partial w}{\partial x}\left(x = \pm\frac{L}{2}\right) = \frac{\partial w}{\partial x}\left(y = \pm\frac{L}{2}\right) = 0 \tag{3.5}$$

where the center of of the plate is assumed to be aligned with the origin at point $(0, 0)$. In section 3.3, a simple formula for the maximum deflection of the plate occurring at $(0, 0)$, based on Timoshenko's solution to the above PDEs, is presented.

3.2.2 Mindlin-Reissner Model

In section 3.3, Finite Element Analyses, using COMSOL Multiphysics, is used and presented as a design tool for the sensor. In this numerical simulation, the plates are modelled as full 3D objects. So it is noteworthy to distinguish the simple thin model discussed in the previous section with the more realistic case dealt with in simulation. This subsection serves as an introductory to an advanced plate



(a) (b)

Figure 3.2: Mindlin Reissner Model visualisation of assumptions and contradictions to Kirchhoff-Love model in the (a) xz and (b) yz planes, Image is from [Bucalem 2011]

bending model. Here, different assumptions from those of Kirchhoff-Love model are schematically shown.

Mindlin-Reissner model is a result of making more realistic assumptions. Unlike Kirchhoff-Love model, it assumes that straight material lines which are initially orthogonal to the mid-surface of the plate remain straight after deflection but *not* necessarily orthogonal. In other words it assumes

$$u = -z\beta_x(x, y), \tag{3.6}$$

$$v = -z\beta_y(x, y), \tag{3.7}$$

where u and v are displacement vectors in x and y directions, respectively. $\beta_x(x, y)$ and $\beta_y(x, y)$ characterize the rotation of material lines that are initially orthogonal to the midsurface of the plate. This assumption is illustrated in Figure 3.2 and contrasted to the assumptions made for Kirchhoff-Love theory where

$$u = -z\frac{\partial w(x, y)}{\partial x}, \tag{3.8}$$

$$u = -z\frac{\partial w(x, y)}{\partial y}. \tag{3.9}$$

The consequence of such an assumption is the addition of two shear stresses (and hence strains) in xz and yz planes which makes the displacement calculation challenging. The complete PDE formulation of the plate and its solution are out of the scope of this work and discussed elsewhere [Bucalem 2011].

3.2.3 Virtual Work

The principle of virtual work is a powerful tool which is basis for numerical solutions to plate bending and other complex physical problems. It can also be used to gain insight into the effect of different parameters as a variational method [Senturia 2007]. Here, the mathematical formulation of the virtual work as well as its application on the variational method is presented.

The concept of virtual work is simply associated with the conservation of energy. It states for a solid in equilibrium, the internal work done by internal stresses must be equal to the external work done by body and surface forces on the bulk and surface of the solid, and can be expressed as

$$\int_v \overline{\epsilon}^T \tau \mathrm{d}V = \int_v \overline{u}^T f^B \mathrm{d}V + \int_v \overline{u}^T f^s \mathrm{d}S \tag{3.10}$$

where

$$\overline{u} = \begin{bmatrix} \overline{u}(x,y,z) \\ \overline{v}(x,y,z) \\ \overline{z}(x,y,z) \end{bmatrix}, \tag{3.11}$$

is the virtual displacement field, ϵ is the associated strain matrix, f^B and f^S are respectively the external body and surface force fields, and τ is the internal stress matrix which is calculated based on Hooke's law [Bucalem 2011]. The integral at the left side of the equation in (3.10) equals the internal work W_i or the stored energy, and that in the right hand side equals the external work W_{ex} done on the solid. So, the principle of virtual work can be rewritten as [Senturia 2007]

$$U = W_i - W_{ex}, \tag{3.12}$$

where in equilibrium, U must be zero such that the total energy is conserved. This representation of virtual work is specifically useful for approximating the displacement in solids, a method known as variational method. The procedure is to first guess a virtual (imaginary) displacement function $\overline{u}$ with n degrees of fredom $c_1, c_2, \cdots, c_n$. Then, for a given body and surface forces $c_1, c_2, \cdots, c_n$ can be fined

such that U is stationary with respect to any virtual displacement, that is

$$\frac{\partial U}{\partial c_i} = 0. \tag{3.13}$$

This leads to a set on n linear equations which can be solved for c_i. The assumed imaginary displacement function is then uniquely characterised. This displacement function, however, is an approximation and can be improved by starting with a more complex function. More information about variational methods can be found in [Senturia 2007].

3.3 Design Considerations

No closed-form solution is yet found associated with the deflection profile of an elastic plate when under uniformly distributed pressure, and (3.2)-(3.5) should be solved numerically by finite element techniques. Numerical methods, however, offer limited intuition as to how plate dimensions affect its deflection profile, unless computationally-heavy parametric simulations are run. The variational method discussed in the previous subsection can be utilized to only *approximate* the displacement field of the plate. Hence the variational method is over-simplistic whose accuracy is limited by the initial assumption on the displacement function. In [Timoshenko 1959], Timoshenko suggests an extension to Levy's solution for simply-supported plates to solve (3.2)-(3.5) with given boundary conditions. Although Timoshenko's solution is neither in closed form, it finds the *maximum* displacement of the clamped membrane as follows

$$w_{max} = w(0,0) = 151 \times 10^{-3} \frac{1-\nu^2}{E} \frac{L^4}{t^3} P. \tag{3.14}$$

w_{max} occurs at the center of symmetry of the plate as shown in Figure 3.3. A strong relationship between the plate side length and thickness to the deflection of membrane is evident from (3.14), that is to gain maximum deflection (sensitivity) the side length must be maximized and the thickness must be minimized. Since Invensense process is designed for inertial sensors, it utilizes a thick μm-scale membrane. This limits the maximum vertical displacement of the plate and consequently $(\Delta C/P)$. The only design parameter of the plate is then its side length. The membrane is made of single-crystalline Silicon which is rigid enough ($\sigma_{Yield} \sim 7GPa$ [Petersen 1982]) for the pressure range of interest (absolute 760-960mmHg), meaning that for the maximum applied pressure the membrane remains in its elastic region. So, the side-length of the membrane can be calculated from (3.14) such that

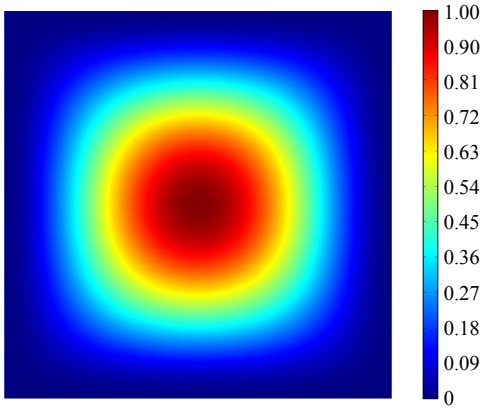


Figure 3.3: Displacement profile of a clamped membrane under uniformly applied pressure. Displacement at each point is normalized to the maximum displacement

W_{max} is smaller than the gap height to avoid collision of the membrane and the top metal layer of the CMOS die. The side-length calculated from (3.14) is then accurately fine tuned by simulating the plate in a finite element solver, COMSOL Multiphysics, to account for other non-ideal effects such as thickness, the attachment of the capping wafer and the stand-offs. Finally, the side length of 1.4mm turned out to be the optimal choice.

As discussed in the previous chapter, to decrease the switching energy consumption it is favourable to minimize the base capacitance C_{s0} of the sensor especially with the SAR CDC sensor interface. To accomplish this, sensor sensitivity $\Delta C/C_{s0}$ must be maximized. Note according to Figure 3.3, the areas around the edges of the membrane experience little to no deflection and so contribute little to ΔC and most to C_{s0} if the bottom plate is center-aligned with the membrane and is a replica of it in size. Thus, the best practice is to scale down the bottom plate of the sense capacitor to concentrate the electric field in the center of the membrane (where maximum deflections happen) and to avoid contribution of the near-edge areas to C_{s0}. An example is shown in Figure 3.4, where the bottom plate of the sense capacitor is swept from 50μm to 1250μm for a fixed membrane side length of 1.4mm. The reduction of both C_{s0} and ΔC is clear for smaller bottom plate side lengths. But, as shown in Figure 3.5, the rate of decreasing C_{s0} is faster than that of ΔC, and the combined effects result in a better sensitivity. For the case of 400μm side length, the sensitivity improves by almost 2.5 times. Further scaling down the bottom plate side length results in an extremely small ΔC, in the order of tens of fF, which severely limits the SNR and avoids medium-resolution quantization. So, we stop bottom plate down-scaling at 460μm.

Membrane thickness and gap height both experience $\pm$10% of variation due

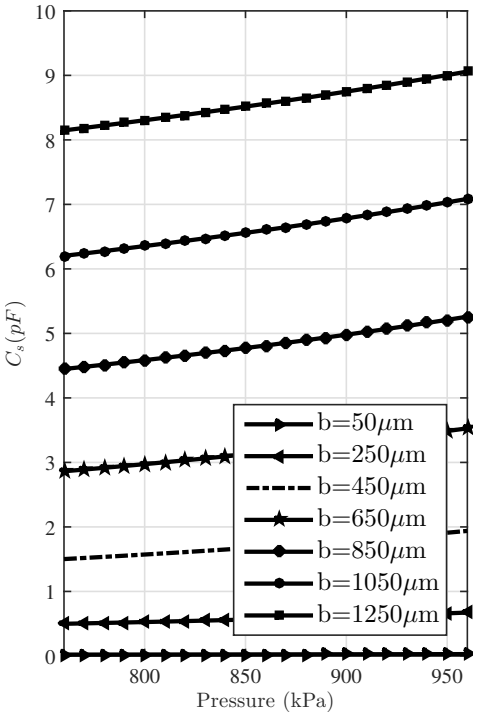


Figure 3.4: The effect of bottom plate scaling on C_s, a=1.4mm

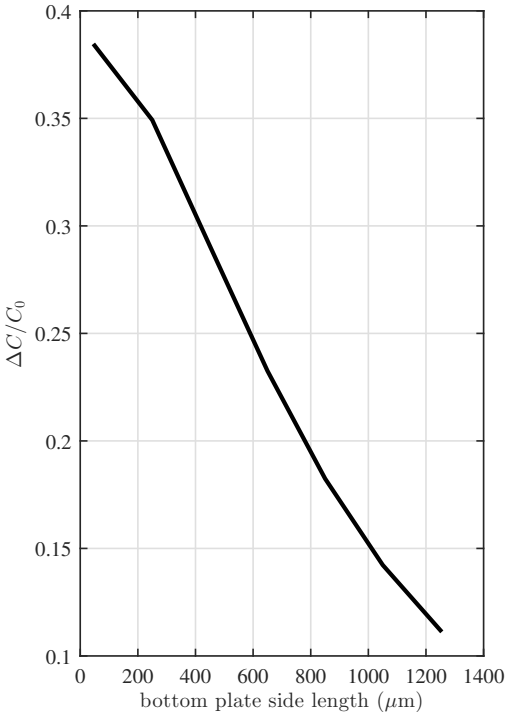


Figure 3.5: Sensor sensitivity vs. bottom plate side length, a=1.4mm

to Invensense MEMS process uncertainties. Plotted in Figure 3.6 are the deflection profiles of the cross-section of the membrane on its axis of symmetry for the minimum and maximum pressures of interest. The displacement is normalized to the minimum gap height. The minimum and maximum sense capacitance using the simulated profiles, shown in Figure 3.7, are then obtained as 1.1pF and 9.84pF for respectively the worst membrane at 760mmHg and best membrane at 960mmHg. The typical sense capacitance is also estimated to vary from 1.56pF to 2pF under respectively 760mmHg and 960mmHg applied pressures. Thus, the SAR CDC full-scale range needs to exceed 9.84pF to avoid saturation for 0–200mmHg pressure range (and with $C_p = 0$). Smaller full-scale ranges, however, are also acceptable for ICP monitoring since the standard required range is 0–100mmHg translating to maximally 4.6pF full-scale range. Nonetheless, we choose 9.5pF as the full-scale range of the CDC to account for non-zero (<4.6pF) parasitic capacitance and a pressure range of 0–100mmHg. In fact, since the total parasitic capacitance is $\sim$1.4pF, the pressure range in the worst case would be extended to 0–150mmHg.

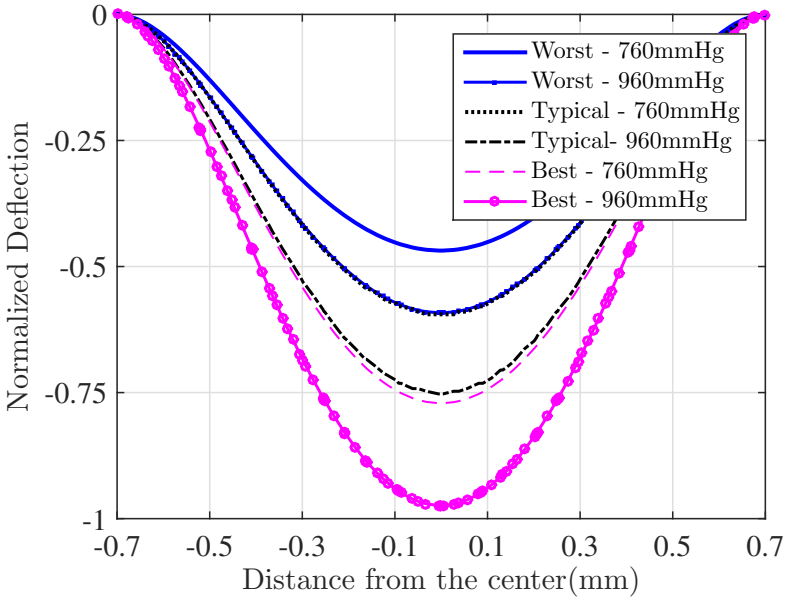


Figure 3.6: Normalized (to the gap height) deflection profile of the membrane for different process corners

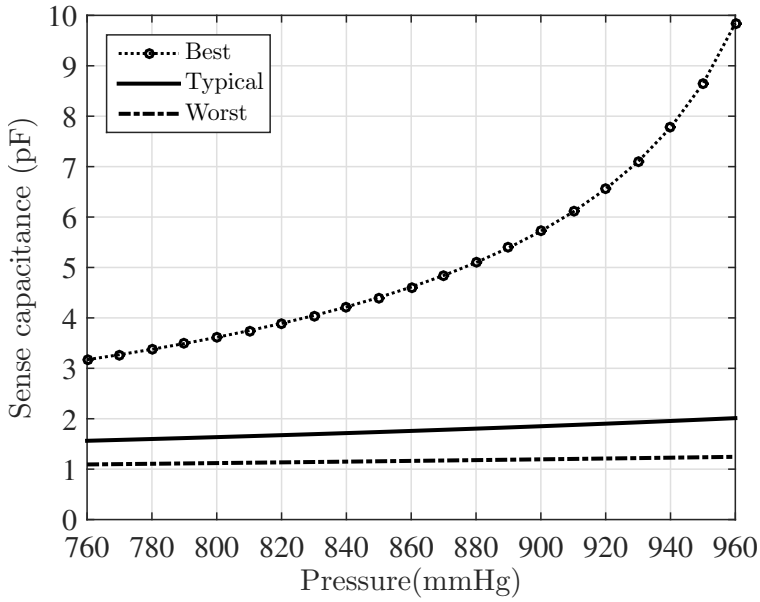


Figure 3.7: Process corner simulation on the sense capacitance

3.3.1 Conclusion

In this chapter, the mechanical structure of the sensor was outlined. The parasitic interconnection capacitance was estimated, and the design considerations of the

membrane were discussed both analytically and through simulations. The small parasitic capacitance of the designed sensor was the key observation that led to the choice of the interface. Thanks to a small parasitic capacitance, direct capacitance (without any intermediate signal) quantisation of pressure sounds the optimal choice according to the analyses performed in Chapter 2. In the next chapter, the implementation considerations of the SAR sensor front-end are discussed in detail.

CHAPTER 4

Interface implementation

Summary

The working principles of the proposed correlated double sampling SAR capacitance to digital converter used for this work was discussed in chapter 2. Here, its implementation considerations and added features are discussed in considerable detail.

4.1 Programmable Dynamic Range

The minimum detectable pressure by the ICP monitoring system is 1mmHg. For the least sensitive membrane at 760mmHg, see Figure 3.7, 1mmHg translates to 0.75fF (or 13.6 bits of resolution with 9.5pF full-scale range). Whereas, the smallest available metal-insulator-metal (MIM) capacitor in Global Foundries CMOS process is 18.5fF. Thus, to achieve the desired resolution split-capacitive array [Baker 2008] is deployed. An N-bit binary-weighted split-capacitive array with the attenuating capacitor C_A is shown in Figure 4.1 where

$$C_i = \begin{cases} 2^{i-1}C_0 & 1 \leq i \leq L, \\ 2^{i-L-1}C_0 & L+1 \leq i \leq L+M, \\ \frac{2^L}{2^L-1}C_0 & i = A, \end{cases} \tag{4.1}$$

and L is the number of branches in the LSB side of the array, $M = N - L$ is the number of MSB-side branches and C_0 is the unit capacitor of the array. Assuming C_0 is chosen the minimum available MIM capacitor $C_{MIM,min} = 18.5\text{fF}$, to achieve a resolution better than $C_\Delta = 0.75\text{fF}$, the number of LSB-side branches needs to be

$$L = \left\lceil \log_2 \frac{C_{MIM,min}}{C_\Delta} \right\rceil = 5. \tag{4.2}$$

So with 14 bits of resolution, the split-capacitive array of Figure 4.1 with 5 LSB-side branches and C_0 of 18.5fF is equivalent to a 14-bit normal binary-weighted capacitive array with $C_0 = C_\Delta$ of 0.57fF.

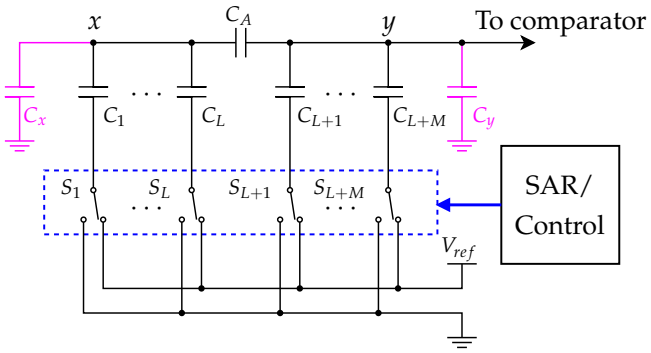


Figure 4.1: Schematic of the split-capacitive array. C_x and C_y are the parasitic capacitors at each side of the array

Table 4.1: SAR CDC Modes of operation

Mode	Active Capacitors	C_0	C_Δ	C_{FS}
1	C_1–C_{12}	18.57fF	0.58fF	2.37pF
2	C_2–C_{13}	37.1fF	1.16fF	4.75pF
3	C_3–C_{14}	74.3fF	2.32fF	9.5pF

Note in Figure 3.7 both the sensitivity and the base capacitance of C_s increase from the worst to the best membrane. This means the worst membrane needs a smaller full-scale range C_{FS} and a finer C_Δ, but the best membrane needs a larger C_{FS} and C_Δ. As an example consider a typical sense capacitance which ranges from 1.5pF to 2pF. Having a maximum full-scale range of 9.5pF for resolving the typical sense capacitor is costly in terms of capacitive array switching power. Because in this case in every conversion, the two MSB capacitors are charged wastefully. So, to further adapt the CDC to the sense capacitor, programmability is incorporated to its full-scale range and resolution C_Δ. The SAR CDC has three modes of operation. For all the three modes the number of bits is kept constant, but the full-scale range and the LSB capacitance C_Δ are doubled. In all the three modes, only 12 capacitors (out of 14) take part in the SAR process and the other two capacitors float using Tri-state switches. The full-scale range and resolution for each mode is summarized in Table 4.1. Thus according to the sense capacitor regardless of whether it has the best or worst membrane, the best full-scale range can be selected.

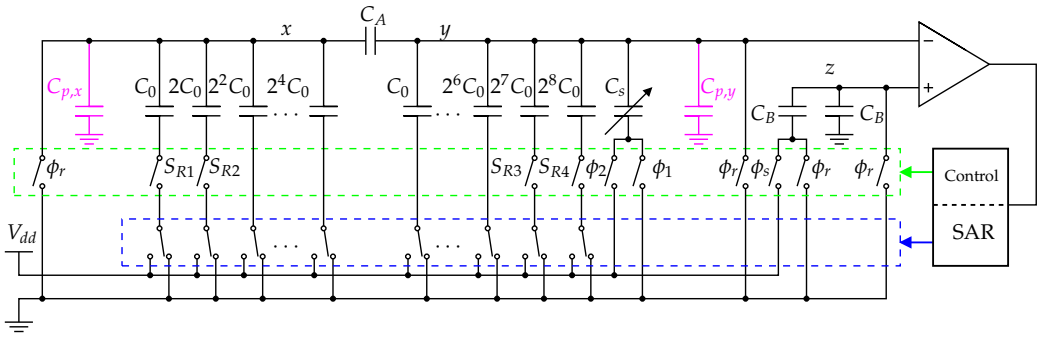


Figure 4.2: SAR CDC circuit diagram. Four tri-state switches are used for full-scale range selection, and T-switches are used for minimizing leakage from the floating nodes x, y and z

4.2 T-switches

Figure 4.2 depicts the circuit diagram of the programmable SAR CDC. The positive terminal of the comparator is pulled to $V_{dd}/2$ at the beginning of each conversion period by the help of two identical capacitors C_B. To minimize capacitance asymmetry at the input terminals of the comparator, these bias capacitors should be half of the total capacitance of the array, $C_B = C_T/2$. To avoid charge accumulation at the positive terminal of the comparator V_z, at the end of each conversion period C_Bs are discharged by a reset switch. The charge leakage through this reset switch during conversion periods, however, causes the reference voltage to drop and drift away from $V_{dd}/2$. For example, if a normal NFET is used as the reset switch, V_z decreases at a rate of 0.88V/s, limiting the sampling rate to 7.2 KHz for 12-bits of resolution. To mitigate this issue, this reset switch is realized by a 3-transistor T-type switch shown in Figure 4.3. When the reset signal is high, M_P is off, and the two NFETs normally discharge the bias capacitors to ground. When the reset signal toggles to low, the NFETs turn off and M_P pulls the drain of M_{N2} high. As a result, the source and drain of M_{N1} swap roles and it experiences a negative, $-V_{dd}/2$, gate-source voltage during the conversion period. This negative V_{gs} significantly enhances the OFF-resistance of the switch. Simulation results show that using this T-switch decreases the voltage V_z drift rate to 0.29mV/s allowing sampling rates down to 3 Hz. Although, the same T-switches are used to implement the reset switches of the array at nodes x and y, the leakage charge through tri-state switches serves as the bottleneck for the sampling rate constricting it to 650 Hz.

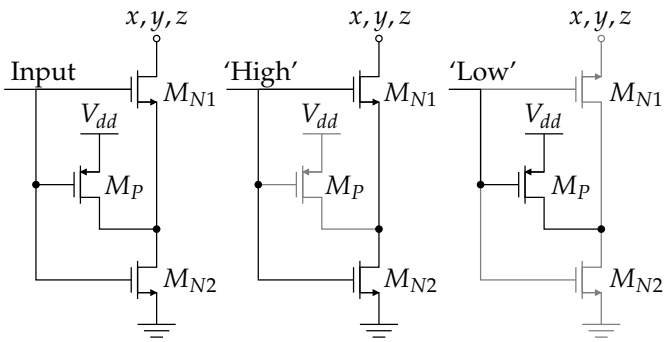


Figure 4.3: T-type reset switch

4.3 Capacitive Array Nonlinearity

Random Nonlinearity

The non-linearity of the binary-weighted split array should also be considered in the design. The derivation of the integral/differential nonliearity $\sigma_{INL}/\sigma_{DNL}$ is the focus of this section.

The nonlinearity of a capacitive DAC with attenuating capacitor C_A is discussed for a special case of equal number of LSB and MSB branches in [Saberi 2011]. However, the capacitive array is asymmetric around C_A. Thus, a general analysis of the statistical nonlinearity for the capacitive DAC with attenuating capacitor is required.

For the following analysis, let's assume each capacitor in Figure 4.1 is a sum of a nominal capacitance as expressed in (4.1) and an error term δ_i which has a zero mean and a variance of [Ginsburg 2007]

$$E\left[\delta_i^2\right] = \sigma_i^2 = \begin{cases} 2^{i-1}\sigma_0^2 & 1 \le i \le L, \\ 2^{i-L-1}\sigma_0^2 & L+1 \le i \le L+M, \end{cases} \tag{4.3}$$

where σ_0^2 is the variance of the error of the unit capacitor.

Also assume the binary representation of the input code is $\mathbf{D} = [D_N, D_{N-1}, \cdots, D_1]$. Two other useful definitions are the total capacitance of the LSB $C_{LSB,T}$ and MSB $C_{MSB,T}$ sides of the array derived as

$$C_{LSB,T} = 2^L C_0 + \sum_{i=0}^{L} \delta_i \tag{4.4}$$

$$C_{MSB,T} = (2^M - 1)C_0 + \sum_{i=L+1}^{L+M} \delta_i \tag{4.5}$$

In order to calculate the INL, trip points of the DAC should be first expressed in presence of the error terms. Then, the gain and offset error have to be cancelled. And finally, $INL[\mathbf{D}]$ is computed as the distance between each ideal value and the associated calculated trip point. The voltage of ideal trip points at the output of the DAC for a given input code $\mathbf{D}$ is given by

$$V_{T,ideal}[\mathbf{D}] = \frac{\sum_{i=1}^{L} C_i D_i + 2^L \sum_{i=L+1}^{L+M} C_i D_i}{2^{L+M} C_0} V_{ref}. \tag{4.6}$$

In presence of error terms δ_i, the voltage of trip points will be given by

$$V_T[\mathbf{D}] = \left(\frac{\sum_{i=1}^{L} (C_i + \delta_i) D_i}{(C_{MSB,T} \| C_A) + C_{LSB,T}} \times \frac{C_A}{C_A + C_{MSB,T}} + \frac{\sum_{i=L+1}^{L+M} (C_i + \delta_i) D_i}{(C_{LSB,T} \| C_A) + C_{MSB,T}} \right) V_{ref}, \tag{4.7}$$

where sign $\|$ is used to show the equivalent capacitance of two series-connected capacitors. After some algebra, (4.7) can be expressed by

$$V_T[\mathbf{D}] = \left(\frac{\sum_{i=1}^{L} C_i D_i + 2^L \sum_{i=L+1}^{L+M} C_i D_i}{2^{L+M} C_0} + E[\mathbf{D}] \right) V_{ref}, \tag{4.8}$$

where $E[\mathbf{D}]$ is given by

$$\begin{aligned} E[\mathbf{D}] = & \frac{1}{2^{L+M} C_0} \left[\sum_{i=1}^{L} \delta_i D_i - \left(\sum_{i=1}^{L} C_i D_i \right) \left(\frac{1}{2^L C_0} \sum_{i=0}^{L} \delta_i + \frac{1}{2^M C_0} \sum_{i=L+1}^{L+M} \delta_i \right) \right] \\ & + \frac{1}{2^M C_0} \left[\sum_{i=1}^{L} \delta_i D_i - \left(\sum_{i=L+1}^{L+M} C_i D_i \right) \left(\frac{1}{2^M C_0} \sum_{i=L+1}^{L+M} \delta_i + \frac{1}{2^{M+L} C_0} \sum_{i=0}^{L} \delta_i \right) \right] \end{aligned} \tag{4.9}$$

By neglecting $\delta_m \delta_n$ terms, the above equation can be further simplified to

$$V_T[\mathbf{D}] \approx \left(\frac{\sum_{i=1}^{L} C_i D_i + 2^L \sum_{i=L+1}^{L+M} C_i D_i}{2^{L+M} C_0} + \frac{\sum_{i=1}^{L} \delta_i D_i + 2^L \sum_{i=L+1}^{L+M} \delta_i D_i}{2^{L+M} C_0} \right). \tag{4.10}$$

The voltage of the trip points with gain and offset errors canceled $V_T^*[\mathbf{D}]$ is given by

$$V_T^*[\mathbf{D}] = \frac{(2^N - 2) V_{LSB}}{V_T[2^N - 1] - V_T[1]} \left(V_T[D] - V_T[1] \right) + V_{LSB}, \tag{4.11}$$

where $V_{LSB} = V_{ref} / 2^{M+L}$ and

$$V_T[1] = \frac{C_1 + \delta_1}{C_0} V_{LSB} \tag{4.12}$$

$$V_T[2^N - 1] = \frac{(2^N - 1) C_0 + 2^L \sum_{i=L+1}^{L+M} \delta_i + \sum_{i=1}^{L} \delta_i}{C_0} V_{LSB}. \tag{4.13}$$

Thus, the gain error G in (4.11) is

$$G = \frac{(2^N-2)V_{LSB}}{V_T[2^N-1]-V_T[1]} =\approx 1 - \frac{1}{(2^N-2)C_0}\left(2^L\sum_{i=L+1}^{L+M}\delta_i + \sum_{i=1}^{L}\delta_i - \delta_1\right) \quad (4.14)$$

By substituting (4.12)–(4.14) in (4.11) and neglecting $\delta_m\delta_n$ terms $V_T^*[\mathbf{D}]$ is obtained as

$$\begin{aligned} V_T^*[\mathbf{D}] = {} & \frac{V_{LSB}}{C_0}\left(2^L\sum_{i=L+1}^{L+M}C_iD_i + \sum_{i=1}^{L}C_iD_i\right) + \frac{V_{LSB}}{C_0}\left(2^L\sum_{i=L+1}^{L+M}\delta_i + \sum_{i=1}^{L}\delta_i - C_1 - \delta_1\right) \\ & - \frac{V_{LSB}}{(2^N-2)C_0}\left(2^L\sum_{i=L+1}^{L+M}C_iD_i + \sum_{i=1}^{L}C_iD_i - C_1\right)\left(2^L\sum_{i=L+1}^{L+M}\delta_i + \sum_{i=1}^{L}\delta_i - \delta_1\right) \end{aligned} \quad (4.15)$$

Interestingly, the terms enclosed with the first pair of parentheses in the right hand side of (4.15) define the ideal values of the trip points. Thus, $INL[\mathbf{D}]$ is simply given by (4.15) excluding the terms in the first pair of parentheses, that is

$$INL[\mathbf{D}] = \frac{1}{C_0}\left(2^L\sum_{i=L+1}^{L+M}\delta_i(D_i - B[\mathbf{D}]) + \sum_{i=2}^{L}\delta_i(D_i - B[\mathbf{D}]) + \delta_1(D_1-1)\right), \quad (4.16)$$

where

$$B[\mathbf{D}] = \frac{2^L\sum_{i=L+1}^{L+M}C_iD_i + \sum_{i=2}^{L}C_iD_i - C_1}{(2^N-2)C_0} = \frac{\mathbf{D}-1}{2^N-2}. \quad (4.17)$$

Taking variance from both sides of (4.16) yields the variance of the integral nonlinearity of the array as

$$\begin{aligned} {\sigma_{INL}}^2[\mathrm{D}] = {} & (\frac{\sigma_0}{C_0})^2 \times (2^{2L}\sum_{i=L+1}^{L+M}(2^{i-L-1}(D_i - B[D])^2) \\ & + \sum_{i=2}^{L}2^{i-1}\,(D_i - B[\mathrm{D}])^2) + (D_1-1)^2). \end{aligned} \quad (4.18)$$

In Global Foundries 0.18μm CMOS process,

$$\frac{\sigma_0}{C_0} = \frac{\alpha}{\sqrt{C_0}} \approx \frac{6\times 10^{-10}}{\sqrt{C_0}}. \quad (4.19)$$

Using (4.18) and (4.19), the INL and DNL of the array for the three modes of operation of the CDC are plotted in Figure 4.4. Numerical calculations show that the CDC in the worst case (with the smallest C_0) should maintain better than 0.6LSB of INL.

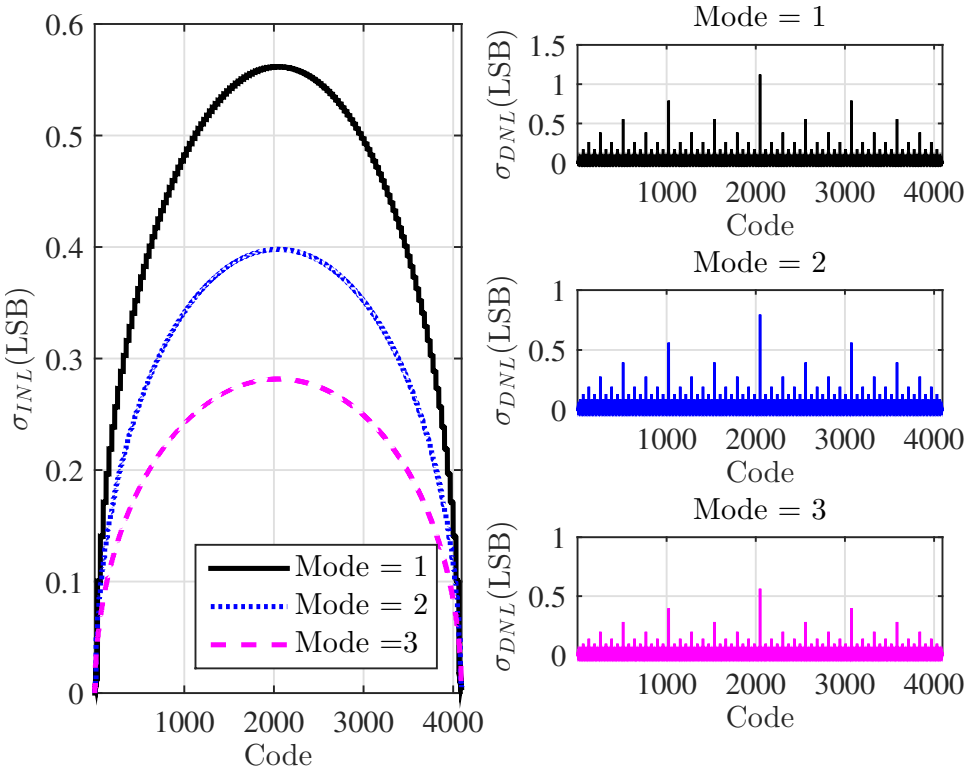


Figure 4.4: Calculated σ_{INL} and σ_{DNL} of the capacitive array for different settings of Table 4.1

Systematic Nonlinearity

The capacitive array in presence of parasitic capacitance suffers systematic nonlinearity. This is because parasitic capacitance (due to routing) appearing across capacitors of the array may not be binary weighted. Also, since the number of LSB branches of the capacitive array is 5, $C_A = 32/31C_0$ can be approximated to $C_A \approx C_0$ for layout simplicity at the cost of further systematic nonlinearity. To show this effect, post layout parasitic extraction was run. Table 4.2 summarizes the parasitic capacitance across various capacitors of the array. Including the parasitic capacitors, the array exhibits a large systematic INL as plotted in Figure 4.5 (solid black lines). To remedy this, a layout technique is introduced in the next section that minimizes the effect of parasitic capacitors on the array nonlinearity.

4.4 Layout Considerations

The last point that deserves mention is regarding the layout of the capacitive array. In the previous section, it was pointed out that the capacitor mismatch in the SAR

capacitive array degrades the linearity of the interface. So, special care must be taken over the layout of the capacitive DAC.

Common layout techniques to increase the matching between the capacitors are listed below and each is followed by a short explanation.

Large capacitors It can be noticed from (4.18) that the variance of the INL is linearly proportional to $(\sigma_0/C_0)^2$ which itself is inversely proportional to C_0, meaning that the larger the value of the unit capacitor, the smaller the nonlinearity, at the cost of power consumption. Unfortunately for this work, this technique cannot be utilised as the maximum value for the unit capacitor is dictated by the sensor maximum capacitance and the resolution, or more accurately by the slope of the capacitance-pressure curve at 760mmHg.

Common-centroid layout Common centroid layout is an effective way to reduce the effect of temperature, pressure and oxide thickness gradients. Note that this technique minimises only the systematic mismatch [Hastings 2006], and it is deployed in almost all IC layouts. It is also suggested that capacitors should be square.

Dummy capacitor Adding one or two rings of dummy capacitors around the main capacitor array help reduce the effect of etching on active capacitors locating along the side of the array.

Dispersion The unit capacitors of a single capacitor should be distributed over the whole array [Hastings 2006].

Merged arrays For a better matching between the two MSB and LSB side arrays it is helpful to merge them into one array.

Shielding To desensitize the layout of the capacitive array to parasitic capacitors of routing traces, the routing of the top and bottom plates of the array should be decoupled. So, here the bottom plates of the array capacitors were routed on M1/M2 and their top plates were routed on M3/M5. Then a ground plane was placed on M4 to shield the top and bottom plate routing traces. The ground plane makes the parasitic capacitance across the array capacitors more binary weighted (see Table 4.2). This layout technique also decreased the parasitic capacitance across C_A by 3 times. The parasitic capacitances of $C_{p,x}$ and $C_{p,y}$, however, increase by almost 5 times responsible for which is the parasitic capacitance between the ground plane and the routing traces of the unit capacitor top plates of the entire array. Because the top plate routing traces are on M3 and M5, a ground plane on M4 substantially increases $C_{p,x}$

Table 4.2: Parasitic capacitance in fF across the capacitors of the array with and without the ground plane

	WOG	WG		WOG	WG
$\mathbf{C_1}$	1.9	1.2	$\mathbf{C_2}$	2.4	2.1
$\mathbf{C_3}$	4.7	4.1	$\mathbf{C_4}$	9.2	8.2
$\mathbf{C_5}$	17.6	16.5	$\mathbf{C_6}$	1.7	1
$\mathbf{C_7}$	3.2	2.1	$\mathbf{C_8}$	5.9	4.84
$\mathbf{C_9}$	9.4	8.8	$\mathbf{C_{10}}$	19.5	18.2
$\mathbf{C_{11}}$	39	36.3	$\mathbf{C_{12}}$	78.9	73.7
$\mathbf{C_{13}}$	157.5	147.8	$\mathbf{C_{14}}$	313.9	295.1
$\mathbf{C_{p,x}}$	11.7	55.5	$\mathbf{C_{p,y}}$	131.3	728.2
$\mathbf{C_A}$	5.6	1.7	—	—	—

and $C_{p,y}$ at the cost of power consumption. In fact, since the added parasitic capacitance is still much smaller than the total capacitance of the array, its associated power consumption is negligible. The overall effect of the ground plane on the systematic INL is also plotted in Figure 4.5 which shows more than 2x improvement.

Considering the above points, the floor plan of the capacitive array can be realised as Figure 4.6. Each square represents a unit capacitor. Unit capacitors with the same color belong to the same capacitor that are routed in parallel. The number inside each capacitor shows the number of unit capacitors (of the same color) that have to be placed in parallel. For example, number 256 in every square with darkest green color means that there are 256 capacitors with such a color. All these capacitors in parallel count up to $256C_0$, making the MSB capacitor of the array. Common-centroid layout, dispersion, shielding, merging and dummy capacitors are all considered for this layout. Please note, dummy capacitors are not shown in the floor plan. The size of each unit capacitor is $4\mu m \times 4\mu m$, and the array consists of 26×26 capacitors (including dummies). The bottom and top plate routing of the capacitors (the first 5 LSBs) are also shown in Figure 4.7 and Figure 4.8.

The final layout of the chip is shown in Figure 4.9. The Silicon real estate measures $2.2 \times 2.6\text{mm}^2$. The chip includes two CDS SAR capacitance to digital converter. One of the CDCs is connected to the on-board transducer, whereas the other CDC is used for experimental characterisation of an external variable capacitor. The gray square top-metal layer aligned with the center of the chip is the bottom plate of the sense capacitor, and the pink thick square ring enclosing the

two SAR CDCs is the stand-off connection of the top plate of the sense capacitor. Total active area of the chip is estimated to be less than 20%, since the dimensions of the chip are dictated by those of the capacitive transducer and not the electronics.

In the chapter, design considerations of the electronics were detailed. Dynamic full-scale range were introduced to adopt the power consumption of the CDC to process-dependent transducer. Furthermore, the non-linearity of the capacitive array were derived and shown to be smaller than 0.6LSB INL/DNL. Moreover, layout techniques used to improve the nonlinearity were outlined, and post-layout parasitic extraction showed the effectiveness of the techniques in reducing the non-linearity of the array by more than two fold.

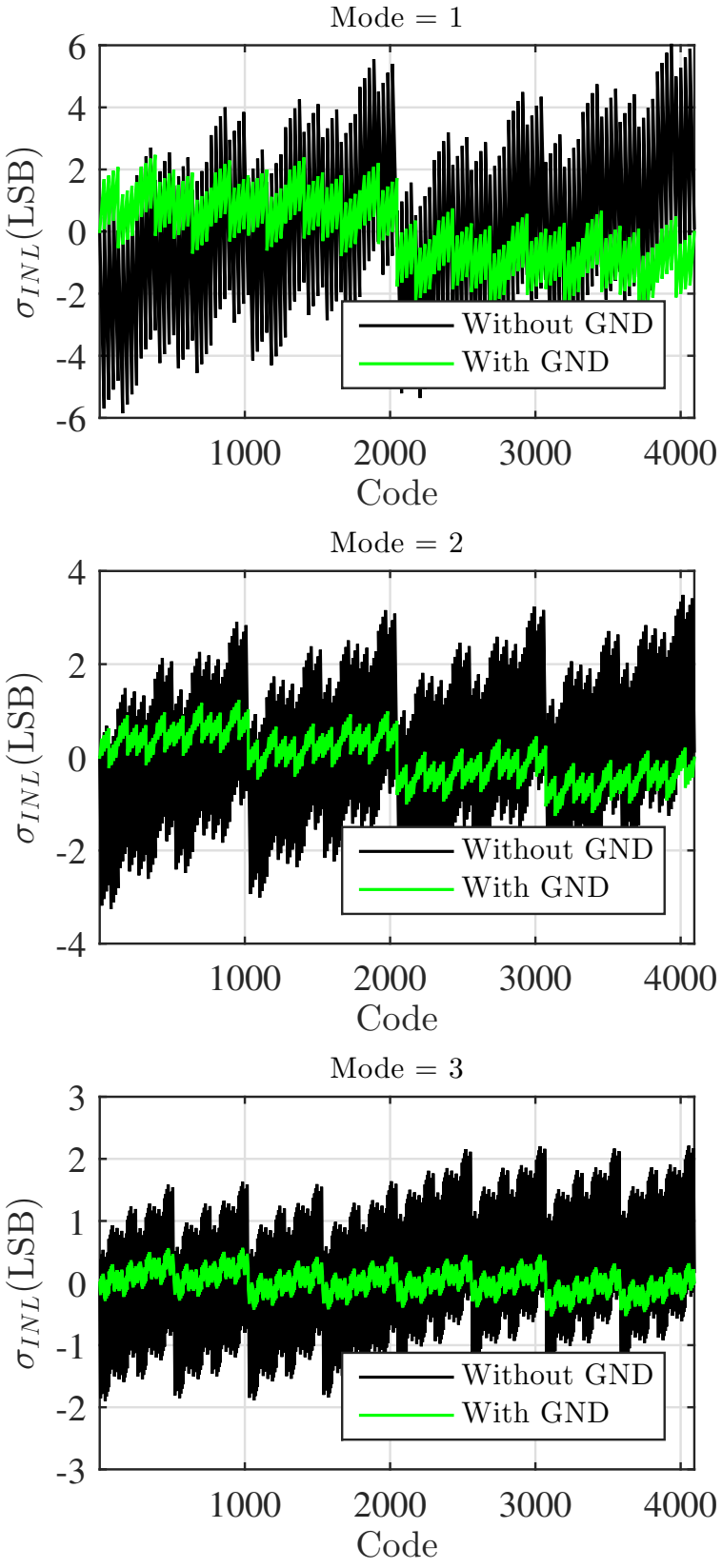


Figure 4.5: σ_{INL} after parasitic extraction with and without the ground plane

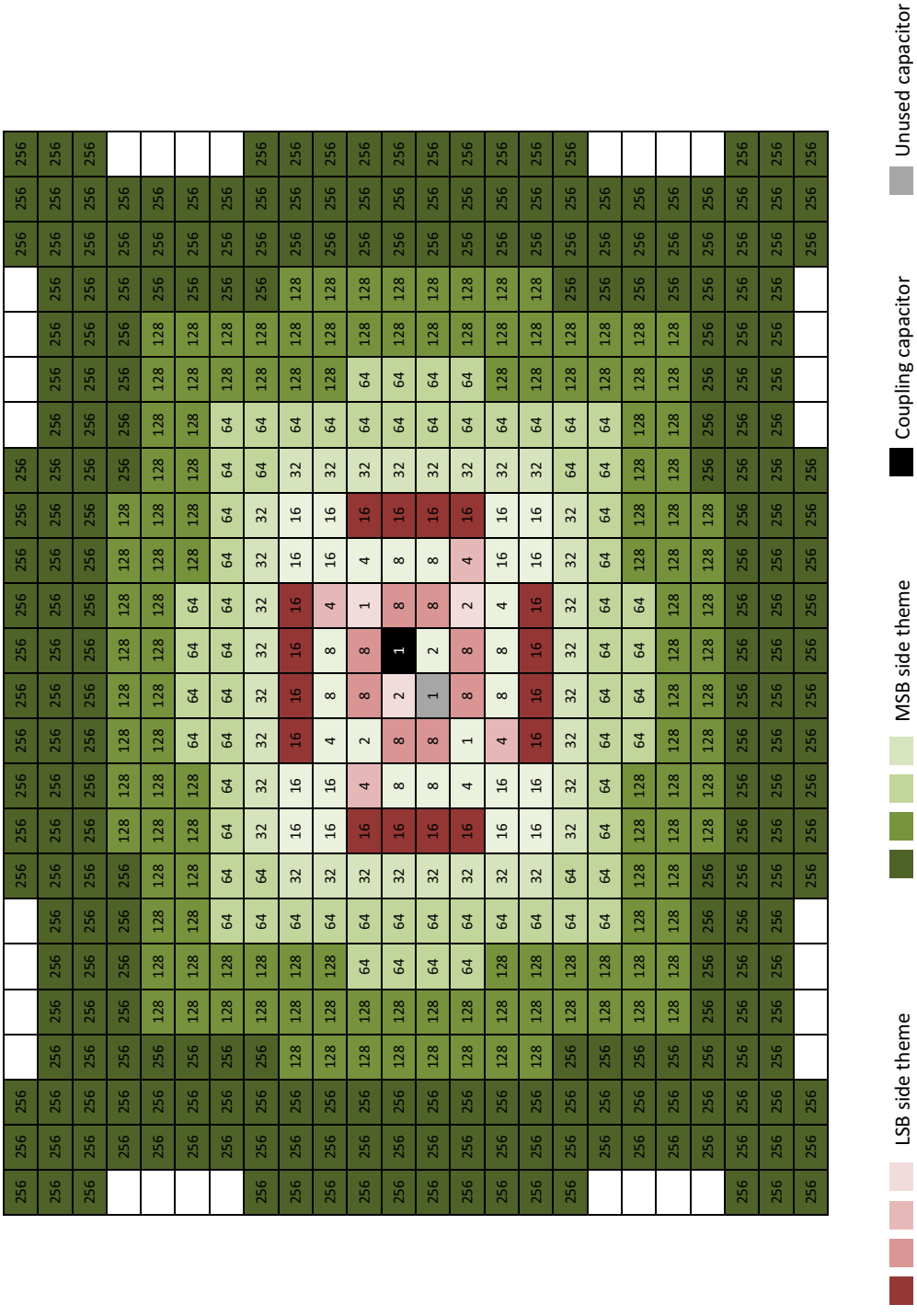


Figure 4.6: Layout floor plan of the capacitive array. Each square shows a unit capacitor. Unit capacitors with the same color are routed in parallel.

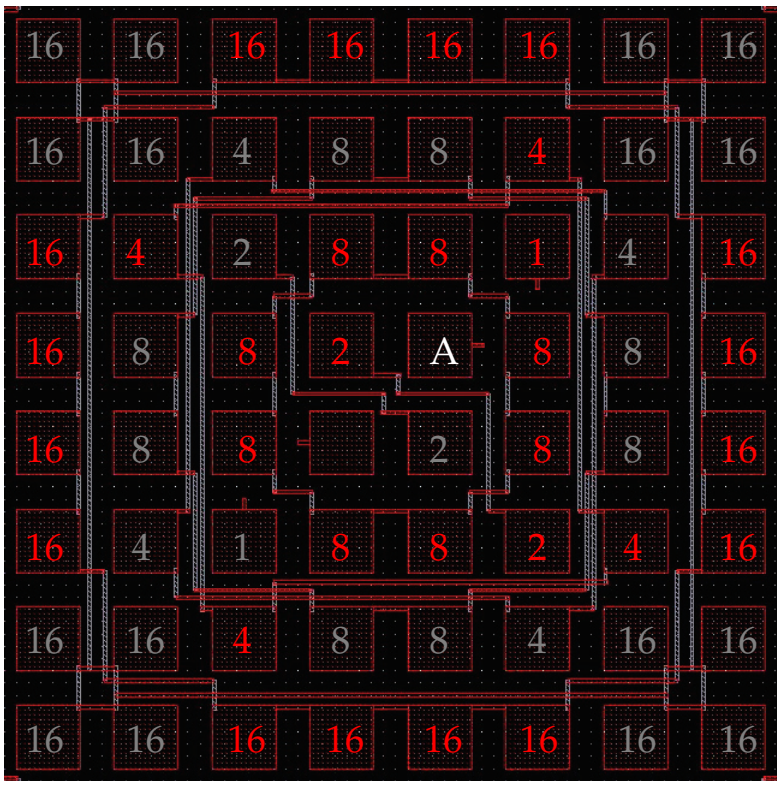


Figure 4.7: Bottom plate routing of the capacitive array on (gray) M1 and (red) M2 layers. Only the routing of the central 8×8 capacitors is shown

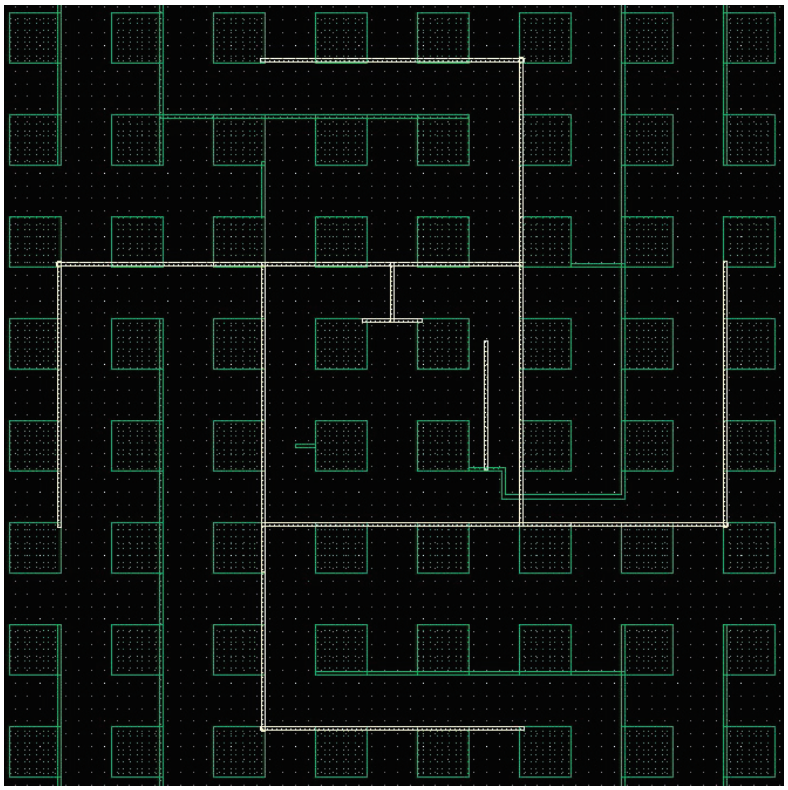


Figure 4.8: Top plate routing of the capacitive array on (white) M5. The top plates of the MIM capacitors are on (green) M3. Only the routing of the central 8×8 capacitors is shown

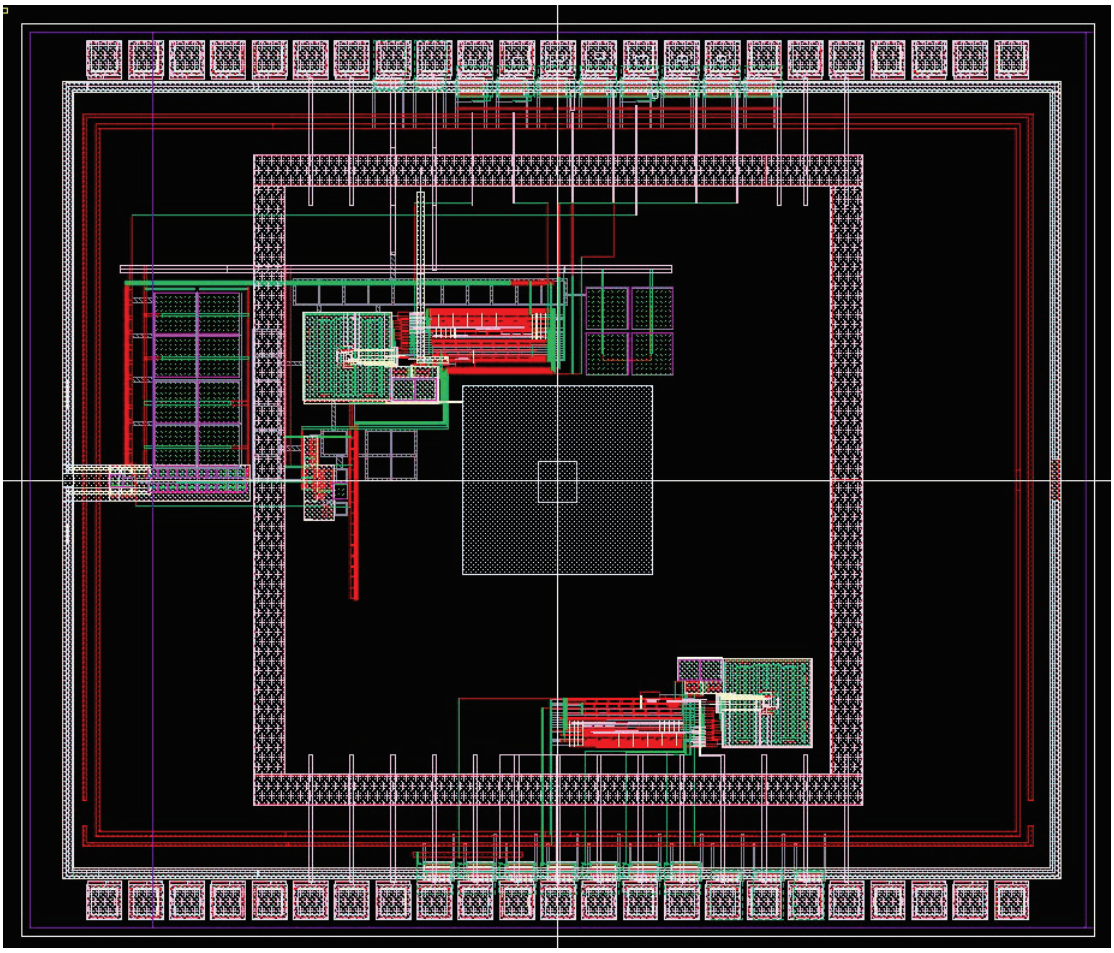


Figure 4.9: Final layout of the chip

CHAPTER 5

Measurement Results

Summary

In this chapter, the characterisation of the fabricated pressure sensing system is presented. The measurement environment and the results alongside comparison of the performance of the fabricated chip with those of the state-of-the-art concludes the work.

5.1 Measurement Environment

The pressure sensing system was fabricated in 0.18μm Invensense MEMS process. In addition to the pressure-sensing core, the chip contains bias generation, power on rest circuitry and a 32 KHz sawtooth oscillator for clock generation. To prevent any fabrication post-processing, the upper cavity (see Figure 3.1) was extended to the MEMS device dicing edge such that a 200μm-wide inlet was automatically formed when the device wafer was diced as shown in Figure 5.1.

A custom-designed pressure chamber was used to characterize the sensor. Design of a pressure chamber for the purpose of this work is extremely challenging. Providing that the chamber must be sealed at all time, there needs to be a wire connectivity between the chip placed inside the chamber and other test setups, e.g. FPGA and PC which are normally outside of the chamber. Specifically, the main difficulty arises from lack of a perfect sealing method around the drilled hole/wires at high pressures of 960mmHg. To have the entire test setup on a PCB board is an option, but development of such a board is time-consuming. Furthermore, such a PCB would measure tens of centimeters in length/width which mandates a large pressure chamber increasing the cost associated with the measurement setup. Here, a simple pressure chamber allowing wire connectivity with low pressure leakage is implemented. The cost associated with the parts of the proposed chamber totals below $1000. The schematic of the proposed chamber is shown in Figure 5.2. One side of the interfacing PCB is extended such that it can fit inside a hose. The front-end of the hose can be perfectly sealed using Teflon tape and hose clamps. Wire connectivity of the chip is done on copper layers of the PCB. The back-end of the

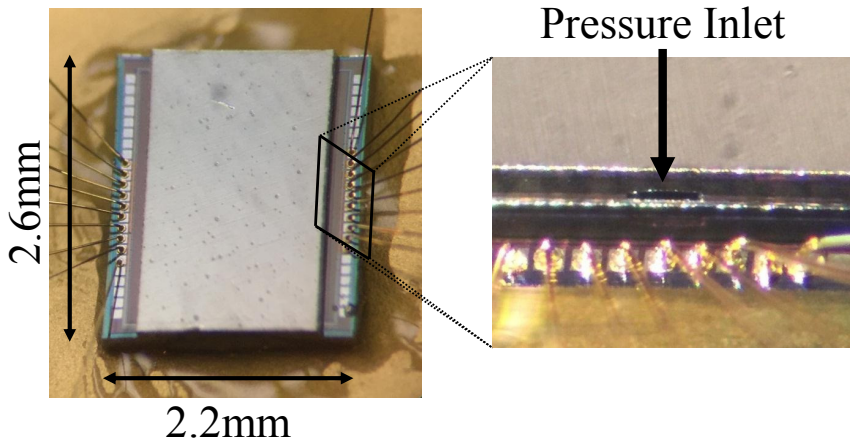


Figure 5.1: Chip photograph and the pressure channel to the upper cavity

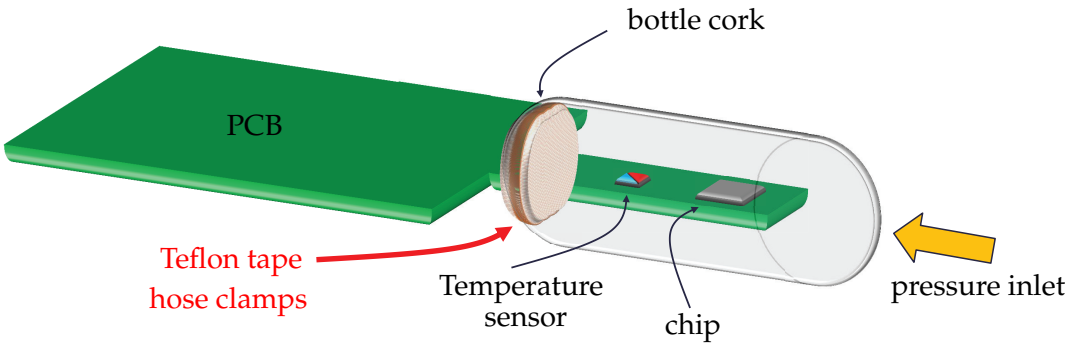


Figure 5.2: The proposed measurement setup. A perfectly sealed pressure chamber is realised by means of a tube around the PCB.

hose is connected to a pneumatic pressure calibration pump (Additel 901) which is also connected to a precision pressure test gauge (Fluke 700GA4). The chip and the precision pressure gauge are then enclosed in the chamber. The pneumatic pressure pump allows adjusting the pressure of the chamber. The precision pressure gauge is used as a reference and the chip is the device under test. The read-out data from the gauge and the chip are compared against each other for the applied pressure range. A temperature sensor is also placed in the vicinity of the chip to allow temperature recordings. The interfacing PCB is control by a National Instrument logic analyser. The interfacing PCB and the measurement environment is depicted in Figures 5.3–5.6.

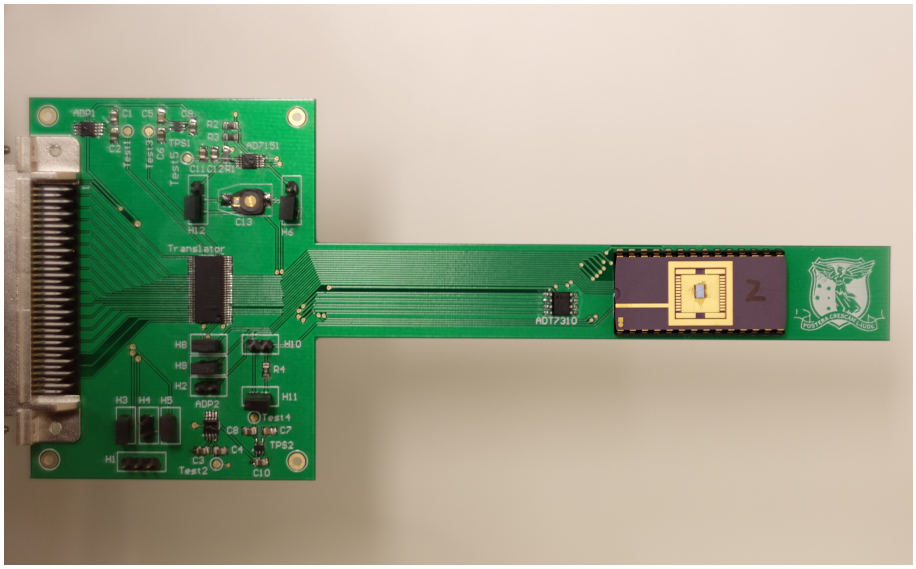


Figure 5.3: The interfacing PCB

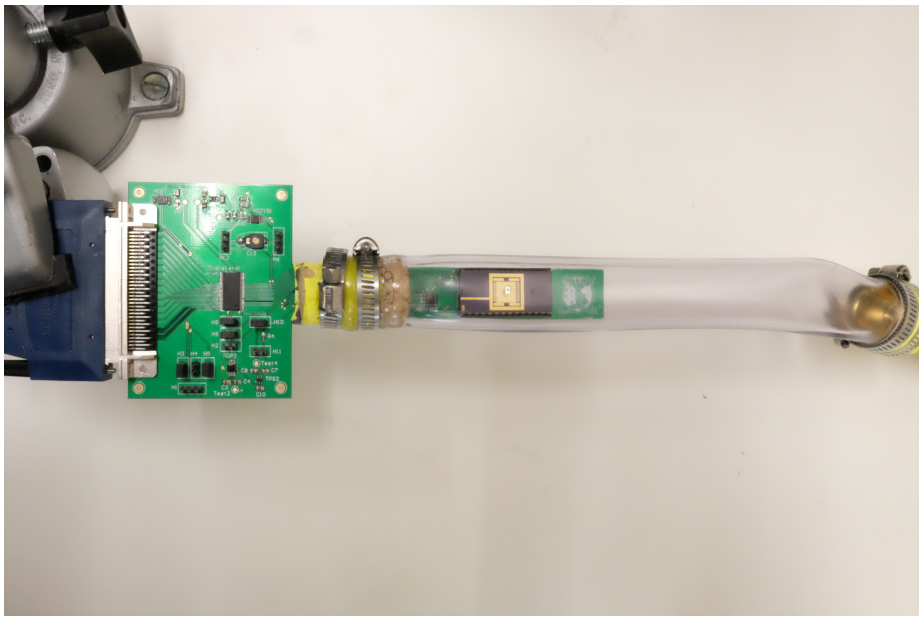


Figure 5.4: The interfacing PCB sealed inside the hose

Figure 5.5: Measurement set-up

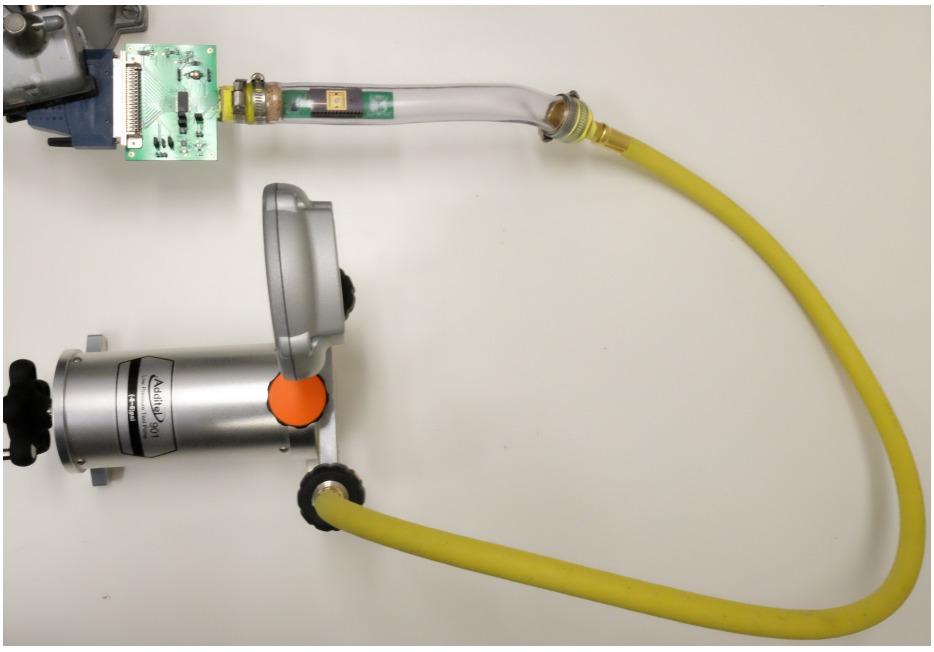


Figure 5.6: Measurement set-up, top view

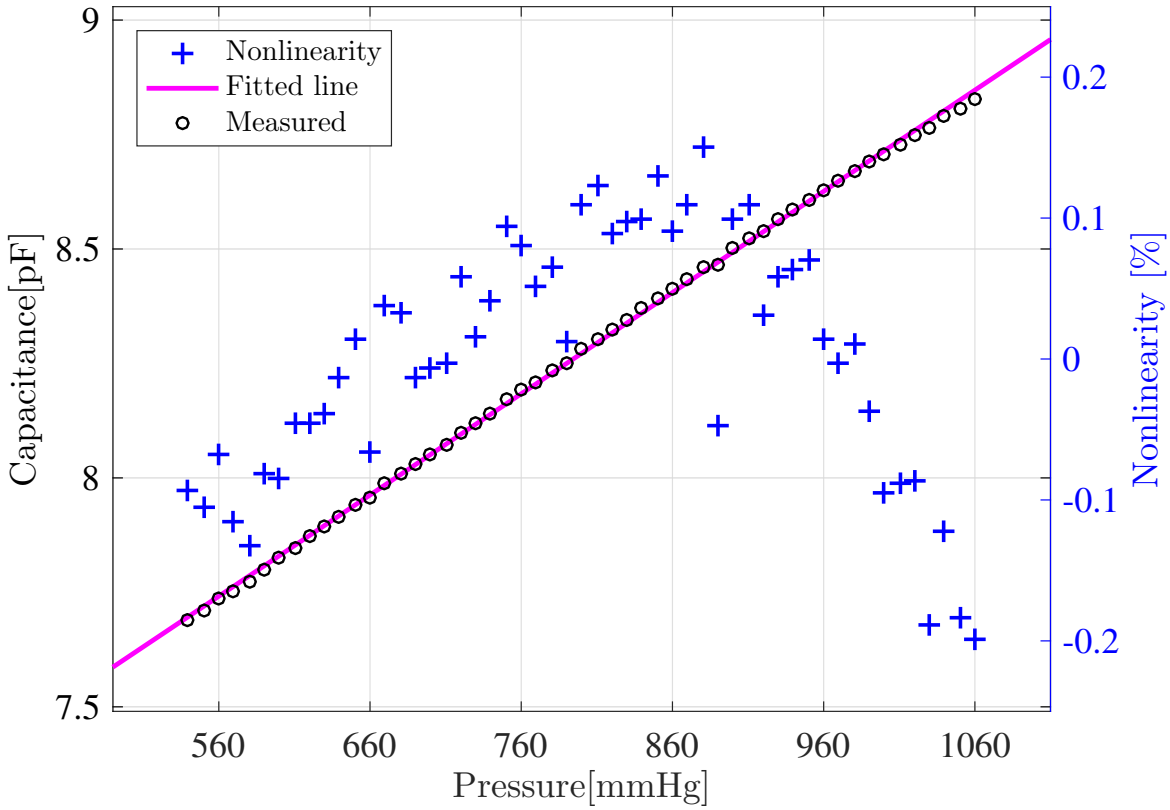


Figure 5.7: Capacitance vs. pressure curve

5.2 Results

During measurement, pressure was swept from 540mmHg to 1060mmHg at 10mmHg/step. Shown in Figure 5.7 is the obtained capacitance-pressure curve of the sensor.

There exists a mismatch between the measured capacitance and the finite element simulation presented earlier. More specifically, the measured base capacitance C_{s0} is larger than expected. High linearity of the sensor (0.2% of nonlinearity) at this large base capacitance hints at the possibility that the sensor operates in a touch-mode rather than the normal mode of operation. Careful investigation of the system revealed a layout error is responsible for the observed mismatch. No pad opening window was placed over the top metal layer (the bottom plate of the sense capacitor), and consequently two (SiO_2 and Si_3N_4) passivation layers were left between the two plates of the sense capacitor decreasing its gap height by 40%. Finite element simulations confirm with the reduced gap size the sense capacitor indeed operates in the touch-mode. The mismatch between the simulated and measured C_s would be eliminated, if the top metal layer had been properly

exposed. Nonetheless, the current touch-mode sensor covers the entire pressure range required for ICP monitoring.

To confirm the proposed heterogeneous sensor-CMOS integration results in minimal C_p, parasitic capacitance is estimated by the help of the measured sensor characteristic shown in Figure 5.7. Note for any applied pressure P, the interface outputs $C_{\phi 1}$ and $C_{\phi 2}$. Denoting $C_A = C_{\phi 1} + C_{\phi 2}$, (2.31) and (2.32) result in

$$C_A(p) = C_T + C_P + 2\frac{V_{OS}}{V_{ref}}(C_T + C_P + C_s(P)). \tag{5.1}$$

In (5.1), the only unknown variables are V_{OS} and C_p. So, for two applied pressures, e.g. 540 mmHg and 640 mmHg, (5.1) can be solved for the unknown variables. C_p and V_{OS} are calculated 1.45pF and 21mV, respectively. According to the post-layout parasitic extraction, Table 4.2, 728fF of this C_p is due to the parasitic capacitance of the routing traces, and thus the current integration method gives rise to only 722fF of C_p, the smallest among reported designs.

The sensor sensitivity is measured 2.2fF/mmHg with 0.2% sensor and CDC *combined* nonlinearity. The total power consumption of the converter core is just below 50nW at 650S/s. Temperature drift of the system is shown in Figure 5.9 where the readout pressure error is negligible for temperatures below 37°C. It, however, increases for temperatures above 37°C by a rate of 1.8mmHg/°C. This degree of temperature stability is sufficient for implantable devices, where self-heating is negligible and ambient temperature excursions are limited to ±1°C. Responsible for increased pressure readout error for temperatures above 40°C is the decreased (sampling) frequency of the oscillator which in turn results in higher leakage current through tri-state switches. Allan deviation of the sensor is also reported in Figure 5.10, suggesting that a noise floor of 2.16mmHg (4.75fF) is achieved when sampling at 60Hz. Providing that the input range of the SAR CDC is 9.5pF, its SNR and FOM based on the definitions given in [Oh 2015] ($\text{SNR} = 20\log\left(\frac{\text{Cap.inputrange}/2\sqrt{2}}{\text{Cap.resolution}}\right)$, $\text{FOM} = \frac{\text{Power}}{\text{f}_\text{s}\times 2^{(\text{SNR}-1.76)/6.02}}$) are respectively 57dB and 3.9pJ/Conv-step.

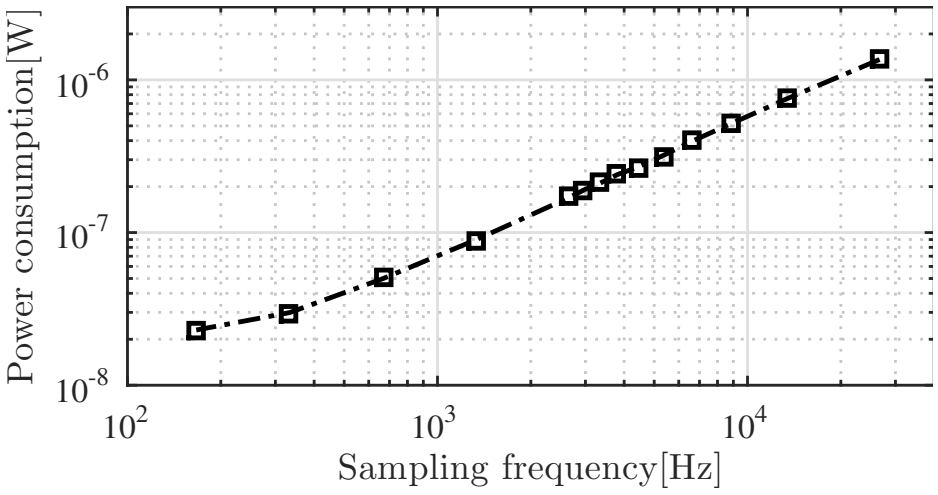


Figure 5.8: Power consumption vs. sampling frequency

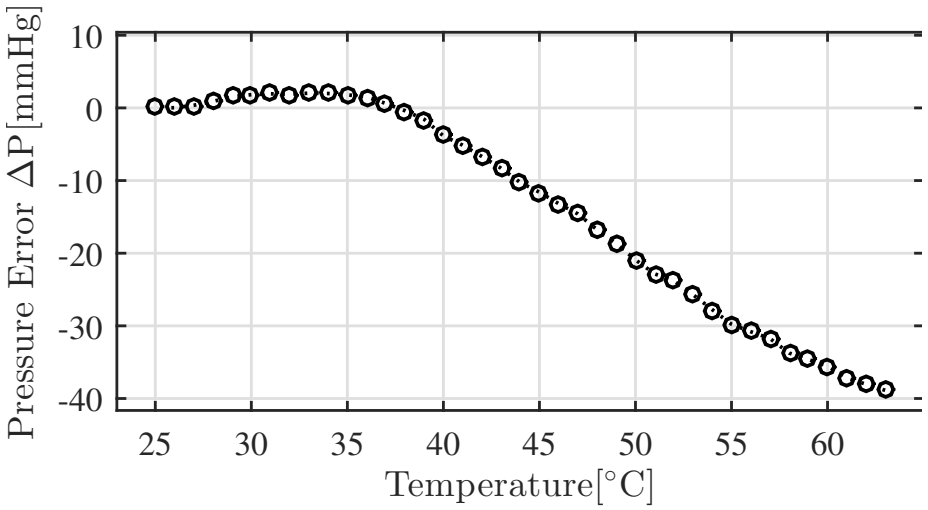


Figure 5.9: Pressure drift from its nominal value (atmospheric pressure at room temperature) vs. temperature change

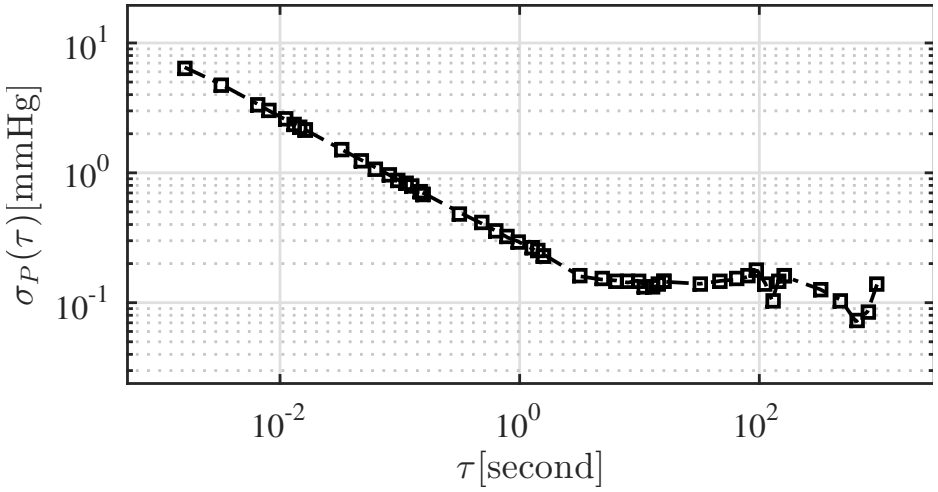


Figure 5.10: Allan deviation

Table 5.1: Performance summary and comparison of recently published capacitive sensing systems

	[Oh 2014]	[Tan 2013]	[Jung 2015]	[Oh 2015]	[Hierold 1999]	[Ha 2014]	**This work**
Sensor type	–	–	–	External	Integrated	External	**Integrated**
CDC Architecture	ΣΔ	ΣΔ	IDCD	Slope	ΣΔ	SAR	**SAR**
Technology	0.18μm	0.16μm	0.04μm	0.18μm	0.8μm	0.18μm	**0.18μm**
Fabrication post-processing	–	–	–	Yes	Yes	Yes	**No**
Input Range(pF)	0–24	0.54–1.06	0.7–10000	5.3–30.7	2.53	2.5–75.3	**9.5**
Power	33.7μW	10.3μW	1.84μW	110nW	1.4mW	160nW	**130nW**
Sensitivity(fF/mmHg)	–	–	–	17.5	1.35	27	**2.2**
Sampling freq.	4.29kHz	1.25kHz	52.6kHz	156Hz	100kHz	250Hz	**60Hz**
Resolution	0.15fF	70aF	12.3fF	8.7fF	0.17fF	6fF	**4.75fF**
SNR(dB)	94.7	68.4	49.7	44.2	74	55.4	**57**
FOM(pJ/Conv.-step)	0.18	3.8	0.14	5.3	899	1.3	**3.9**
Supply	1.4V	1.2V	0.45–1V	1.2-4V	3.5V	0.9–1.2V	**1V**
System Volume	–	–	–	6.27mm^3	1.52mm^3	–	**2.29mm^3**

5.3 Comparison

The performance metrics of the pressure sensing system are comparable to those of recent state-of-the-art systems. The comparison is summarised in Table 5.1. In contrast to other systems, the proposed heterogeneous pressure sensing system requires no fabrication post-processing, and it outperforms highly custom-designed capacitive sensors [Hierold 1999, Sundararajan 2015] in terms of sensitivity. The power consumption of the system and the obtained pressure resolution (2.16mmHg) make it a perfect fit for an intracranial pressure monitoring system.

CHAPTER 6

Conclusion

A pressure sensing microsystem suitable for implantable intracranial pressure monitoring was designed and implemented in Invenses MEMS 0.18μm-CMOS process. The entire system measures $2.2 \times 2.6\text{mm}^2$ in surface area and is only 0.4mm in thickness. The dimensions of the system allow prospect integration of an on-chip RF antenna for efficient power and/or data transmission. Nonetheless, the focus of this work was the design of the core elements, transducer and sensor interface, with maximum energy-efficiency to enable battery-less operation of the implant.

The system incorporates two modules namely interfacing circuitry and sensor transducer. The two modules were co-designed with emphasis on energy-efficiency. Firstly, the concept of holistic noise-power optimisation was introduced. The proposed optimisation technique promises calculation of optimal power consumption of a given architecture for given SNR. Therefore, it provides a powerful metric to enable fair performance evaluation of sensor interfaces. Detailed optimisation analyses were applied to known low-power interface topologies. it was concluded that

- energy efficiency of sensor interfaces enhances with high-quality sensor-interface interconnections, characterised by interconnection parasitic capacitance C_p, and

- for moderate SNR, required for ICP monitoring, and small C_p the successive approximation register capacitance to digital converter SAR CDC is the most energy-efficient sensor interface.

The contributed circuit design techniques in the design of the SAR CDC are as follows.

- Correlated double sampling was incorporated in the switching scheme of the interface to combat low-frequency 1/f noise and input referred offset voltage of the comparator.

- The proposed 3-transistor purging T-switch used in the capacitive array decreased leakage current by more than three orders of magnitude allowing sampling speed down to 3Hz.
- Detailed analyses and simulations were performed to ensure in-bound systematic and random non-linearity. Furthermore, placement of a shielding GND plane was found effective in reducing parasitic capacitance related non-linearity by twofold.

In the transducer department, the focus of the design was obtaining minimal C_p. So, a unique heterogeneous sensor-interface integration was proposed. As a result of this integration, unlike previously reported designs no fabrication post-processing was required and the chips were measured immediately after fabrication. Moreover, the quality of the sensor-interface interconnection was to be better by an order of magnitude compared to traditional integration methods.

6.1 Future Work

- The noise immunity of the SAR CDC sensor interface designed for this work can be further improved by implementing a fully-differential capacitive array. Although it doubles the power consumption of the array, it nulls substrate coupled noise and kick-back noise to the input terminals of the comparator and overall enhances the figure of merit of the interface.
- In Chapter 2, only a single slope sensor interface was considered. However, there are other variants, e.g. double and multiple slope converters, that can be included to the analyses for the sake of completeness.
- In this work to reduce the leakage current, a T-switch was proposed. Investigation of other possibilities to/improvement upon this T-switch to further decrease the leakage current such as back-gate modulation is a sound future track.
- As mentioned earlier, an on-chip RF antenna can be integrated to the system for energy-scavenging and data transmission purposes. Thanks to nW power consumption of the system, alternatively, integration of low-efficient energy-scavenging methods such as biological fuel cells [Rapoport 2012] can also be investigated.
- Recently, Invensense has upgraded its MEMS process to include piezoelectric materials. Therefore, another possibility for power transmission is ultrasound

which in fact because of lower speed of sound (compared to RF waves) in tissue is more efficient than RF power transmission. In this case, ultrasound wave back-scattering can be exploited for data transmission.

- The system at its current state cannot be implanted in a biological medium for lack of a biologically-friendly packaging/coating. Thus, packaging, in-vivo and in-vitro measurements should also be performed to evaluate the performance of the system in a biological medium.

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