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CdTe/CdS Thin Film Solar Cells Fabricated on Flexible Substrates

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CdTe/CdS Thin Film Solar Cells Fabricated on Flexible Substrates

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
Department of Electrical Engineering
College of Engineering
University of South Florida

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Stainless Steel Foils

DEDICATION

I dedicate this dissertation to my wife and my family for all their support throughout the years.

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I must first thank God for giving me strength and courage to achieve my goal of obtaining this degree. I would like also to thank my major professor, Dr. Christos Ferekides for his continuous support and guidance during this project. I would like to thank my committee members, Dr. Don Morel, Dr. Elias Stefanakos, Dr. Yogi Goswami and Dr. Sarath Witanachchi for their help and advice during my research.

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ABSTRACT

Cadmium Telluride (CdTe) is a leading thin film photovoltaic (PV) material due to its near ideal bandgap of 1.45 eV and its high optical absorption coefficient. The typical CdTe thin film solar cell is of the superstrate configuration where a window layer (CdS), the absorber (CdTe) and a back contact are deposited onto glass coated with a transparent electrode.

Substrate CdTe solar cells where the above listed films are deposited in reverse are not common. In this study substrate CdTe solar cells are fabricated on flexible foils.

The properties of the Molybdenum back contact, Zinc Telluride (ZnTe) interlayer and CdTe absorber on the flexible foils were studied and characterized using X-Ray Diffraction (XRD), and Scanning Electron Microscopy (SEM).

Substrate curvature and film flaking was observed during the fabrication as a result of differences in thermal expansion coefficients between the substrate and the deposited films, and also due to impurity diffusion from the foil into the film stack. In order to overcome this problem diffusion barriers where used to eliminate contamination. Silicon dioxide (SiO_2), silicon nitride (Si_3N_4) and molybdenum nitride (Mo_xN_y) were used as such barriers.

Electrical characterization of completed devices was carried out by Current-Voltage (J-V), Capacitance-Voltage (C-V) and Spectral Response (SR) measurements.

Roll-over was observed in the first quadrant of J-V curves indicating the existence of a back barrier due to a Schottky back contact. The formation of non-rectifying contact to p-CdTe thin-film is one of the major and critical challenges associated with the fabrication of efficient and stable solar cells.

Several materials (ZnTe, Cu, Cu_2Te, and Te) were studied as potential candidates for the formation of an effective back contact.

CHAPTER 1

INTRODUCTION

Global power consumption rate currently stands at approximately 15 TW (1 TW=10^{12} W). The majority of the energy is produced from fossil fuels (coal, oil and natural gas). The burning of fossil fuels produces carbon dioxide (CO_2) which contributes to global warming causing the surface temperature of the earth to rise.

Solar energy is the cleanest energy we can use and could last billions of years. Using the photovoltaic effect, a solar cell converts solar energy directly into electricity. Photovoltaics (PV) is an important energy technology that has a small impact on the environment as it generates electricity from light and produces no air pollution or hazardous waste. It doesn't require fuels to be transported or combusted, and because its energy source - sunlight - is free and abundant, PV systems can guarantee access to electric power.

The photovoltaics' (PV) market is dominated by crystalline silicon solar modules which require thicknesses of approximately 200 µm and high cost manufacturing processes. High production costs of Si based PV's, lead to the development of thin film PV technologies.

Thin film solar cells use a group of materials with high absorption coefficients. This property reduces the thickness of the films from a few hundred microns to only a few microns. Therefore the amount of raw materials needed for the fabrication of solar cells is significantly lower than that used for the crystalline Si technology and they can be used in polycrystalline form not requiring expensive processing and deposition techniques. Today's leading thin film solar cells are copper indium gallium diselinide (CIGS) and cadmium telluride (CdTe).

Crystalline silicon accounts for 85% of the PV market. The biggest change this past decade has been the emergence of CdTe thin-film technology. First Solar has brought CdTe to mass production and in 2009 it became the world's first PV manufacturer to exceed 1 GW/year production rate capturing 13% of the global market. Figure 1 shows the global market share of the different PV technologies for the years 2008 and 2009.
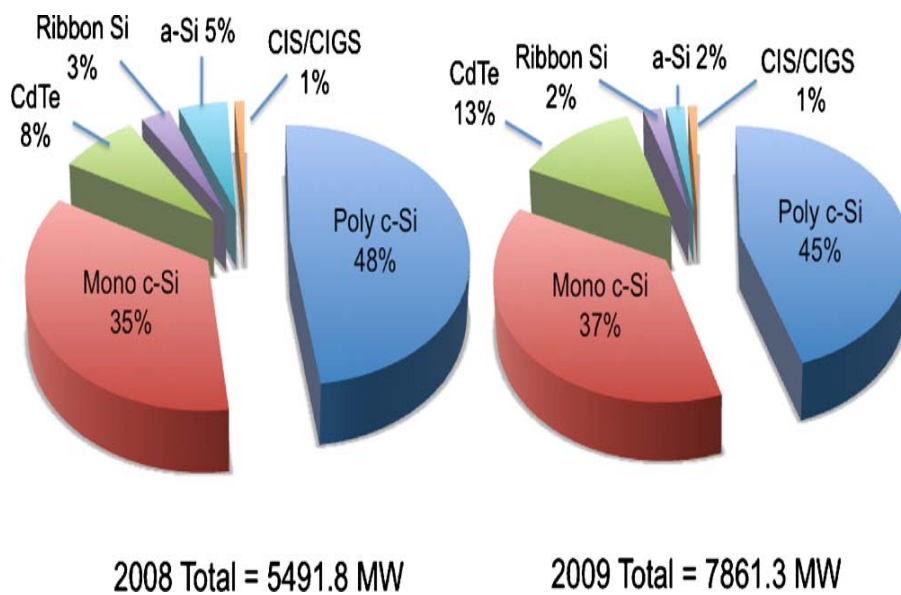
Figure 1. Market share for PV technologies

CdTe and CIGS small area laboratory cells demonstrated efficiencies of 16.5% [1] and 20.3% [2] respectively, while on the manufacturing side the module efficiencies stand at ~11% for CdTe and ~13% for CIGS.

The objective of this study will be to transform the design of CdTe solar cells from the standard superstrate configuration to a flexible substrate configuration with the capability for a roll-to-roll manufacturing, which has the potential to further reduce costs for the lowest cost PV technology.

CHAPTER 2

SEMICONDUCTORS AND SOLAR CELLS

2.1 Semiconductors

Semiconductors are materials whose conductivity lies between those of insulators and metals. Silicon (Si) is the most common elemental semiconductor. Compound semiconductors are formed from combinations of group II and group VI elements and combinations of group III and group V. Gallium arsenide (GaAs) and gallium phosphide (GaP) are Group III-V semiconductors while cadmium telluride (CdTe) and cadmium sulfide CdS) are group II-VI.

Semiconductors are the foundation of modern electronics because of the ability to change their conductivity by introducing impurities in their crystal lattice. The process of adding controlled amounts of specific types of impurity atoms that change the electrical characteristics of a semiconductor is called doping.

Depending on the type of dominant charge carrier the semiconductor can be n or p-type. Adding phosphorus, a group V element, into Si produces a free electron, increasing the concentration of free electrons. This process is called n-type doping and phosphorus is called a donor. P-type doping is obtained when an element of group III, like boron is added to Si. Boron atoms, or in general

p-type doping atoms, that cause an increase in the hole concentration are called acceptors.

2.2 PN Junctions

Most semiconductor devices contain at least one pn junction. The pn junction provides the characteristics needed for rectifiers, amplifiers and many other electronic circuit functions. A pn junction is formed when p-type material (majority carriers are holes) comes in contact with n-type material (majority carriers are electrons). The interface separating the n- and p- regions is called the metallurgical interface. Initially at this interface there is a large concentration of electron and holes. Majority carrier holes from the p-region will begin diffusing into the n-region and majority carrier electrons from the n-region will begin diffusing into the p-region. This movement of carriers constitutes the diffusion current. Electrons leaving the n-region and holes leaving the p-region leave behind uncompensated charge of donor and acceptors ions respectively. This uncompensated charge creates an electric field called the built-in field. This field appears in a region in the junction called the depletion region and creates a drift component of current in the opposite direction to the diffusion current. The electric field continues to build up until equilibrium is reached and the net current is zero.

In thermal equilibrium the Fermi energy level is constant throughout the system. The Fermi energy level is defined as the maximum energy occupied by an electron at 0K. Figure 2 shows the energy band diagram for the pn junction at

equilibrium. The bands bend in the depletion region by an energy qV_{bi}, and this is called the built-in-potential.
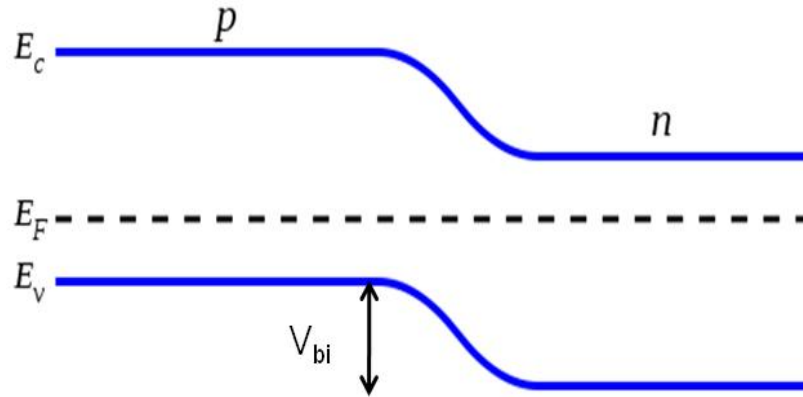
Figure 2. PN junction energy band diagram at equilibrium

The built-in-voltage in thermal equilibrium can be expressed by the following equation:

$$V_{bi} = \frac{kT}{q} \times ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{1}$$

where N_A and N_D are the doping concentrations in the p and n type semiconductors, n_i is the intrinsic carrier concentration, k is Boltzmann's constant, and T is the absolute temperature.

Figure 3 shows the pn junction under forward bias. The forward bias voltage V_A appears across the depletion region splitting the Fermi levels in the opposite direction reducing the potential barrier from V_{bi} to $(V_{bi}-V_A)$.Majority carrier electrons from the n-region are injected to the p-region and majority

carrier holes from the p-region are injected to the n-region and are subjected to the diffusion and recombination process.
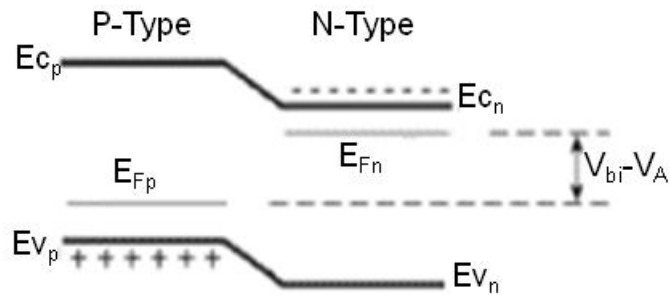
Figure 3. PN junction under forward bias

If the pn junction is reversed biased, the potential barrier is increased by the amount of the applied voltage. The increase of the potential barrier decreases the number of majority carriers able to diffuse reducing therefore the diffusion current. Figure 4 shows the pn junction under reverse bias.
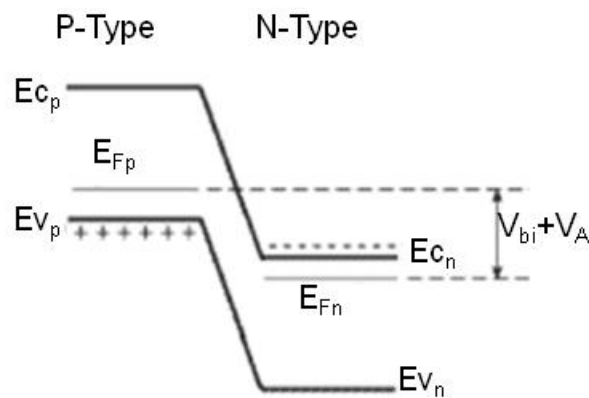
Figure 4. PN junction under reverse bias

The current flowing through a pn junction under forward or reverse bias is given by the following relationship:

$$I = Is \times \left(e^{\frac{qV}{AkT}} - 1\right) \hspace{4cm} (2)$$

where I_s is the reverse saturation current and A is the diode quality factor. Typical values for the diode quality factor are between 1 and 2. For A=1 the current transport is dominated by diffusion while for A=2 by recombination.

2.3 Metal-Semiconductor Contacts

Semiconductor devices must make contact with the outside world. This contact is made by depositing a metal over the semiconductor. There are two different types of metal-semiconductor contacts:

- Rectifying contacts known also as Schottky barriers and
- Ohmic contacts.

2.3.1 Schottky Barriers

Figure 5 shows the energy band diagrams of a metal and an n-type semiconductor before they come into contact. E_0 is the vacuum energy level and represents the energy of a completely free electron. Φ_M is the metal work function and Φ_S is the semiconductor work function. The work function of a material is the energy difference from the vacuum energy to the Fermi energy level (E_F). For a semiconductor the work function is not a material constant but depends on the doping. However the doping does not influence the position of the bands with

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respect to the vacuum level. The parameter χ is the electron affinity energy and is the position of the bottom of the conduction band with respect to the vacuum level.
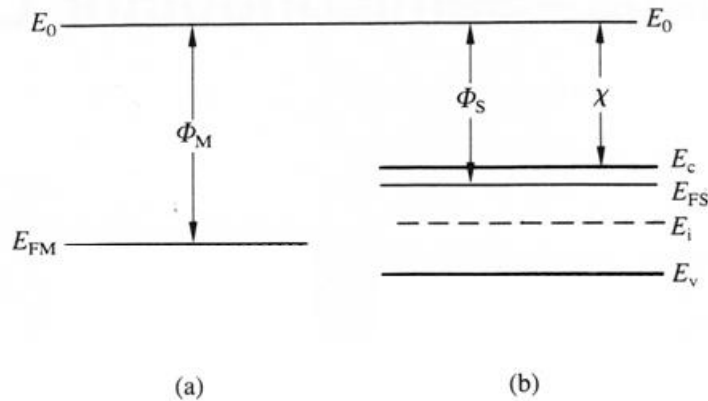
Figure 5. Energy band diagrams of (a) metal and (b) n-type semiconductor

From Figure 5, the Fermi level of the n-type semiconductor is higher than the Fermi level of the metal and therefore the energy of electrons in the semiconductor is greater than the energy of those in the metal. When the two materials come into contact electrons flow from the semiconductor to the metal until the Fermi energy levels of the two materials align and the system reaches equilibrium. Figure 6 shows the energy band diagram of the system in equilibrium.

The transfer of electrons from the semiconductor to the metal creates a depletion layer at the semiconductor surface. The energy bands are bent in the depletion layer. This bending is the difference between the Fermi levels of the metal and the semiconductor and is given by

$$V_{bi} = \Phi_M - \Phi_S \qquad (3)$$

This is the energy barrier for electrons moving from the semiconductor to the metal. Electrons moving from the metal to the semiconductor see a different barrier, Φ_B, given by the difference between the metal Fermi level and the semiconductor electron affinity

$$\Phi_B = \Phi_M - \chi \qquad (4)$$
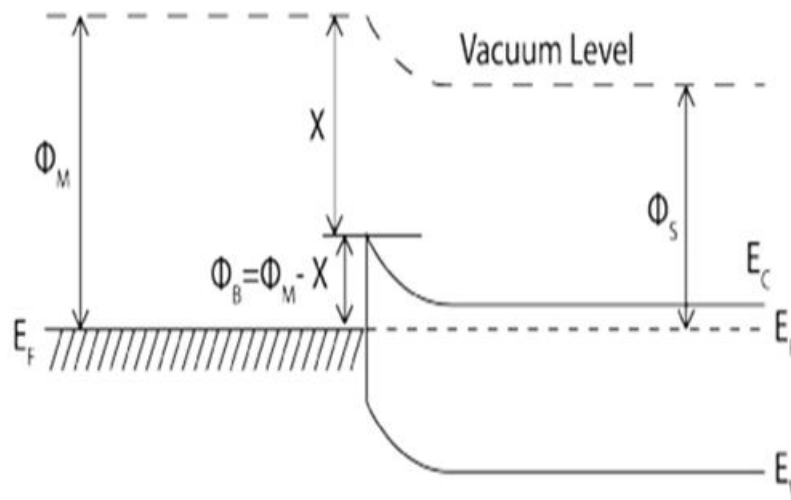
Figure 6. Metal-semiconductor Schottky barrier band diagram at equilibrium

The current in the metal-semiconductor is determined by the flow of electrons from the metal to the semiconductor and vice versa. A voltage is applied from the metal to the n-type semiconductor, V_A, in the same way as the p-n junction. Figure 7 shows the metal-semiconductor contact under forward and reverse bias. When $V_A > 0$, the contact is forward biased and the energy barrier in the depletion layer reduces to $q(V_{bi}-V_A)$ This enables electrons to overcome

the barrier and flow from the semiconductor to the metal. Current flows from metal to semiconductor and increases exponentially with the forward bias voltage. Electrons in the metal however see the same barrier, Φ_B, as in the equilibrium case.
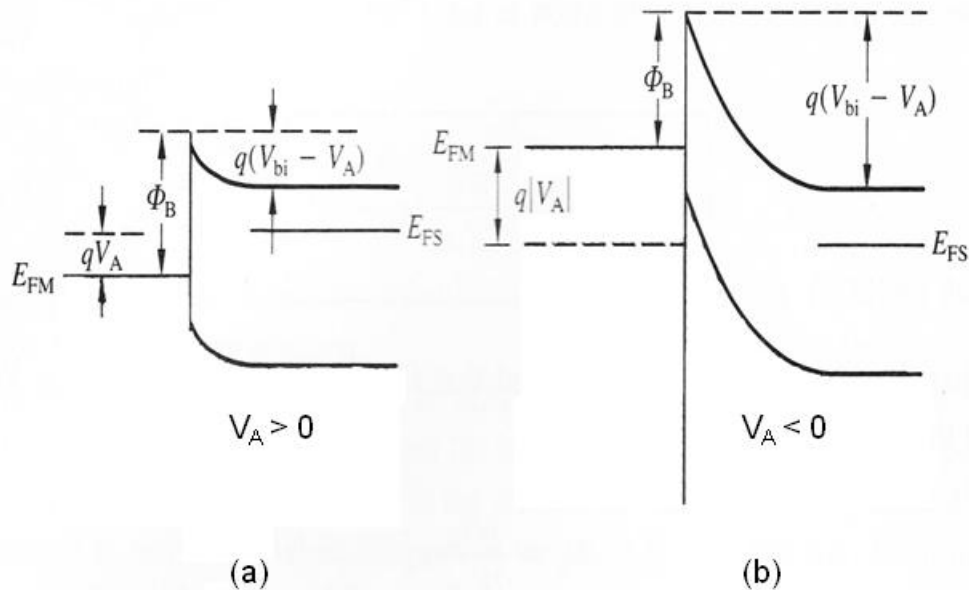
Figure 7. Schottky barrier under (a) forward bias and (b) reverse bias

Under reverse bias, $V_A < 0$, the energy barrier height for the electrons in the semiconductor increases to $q(V_{bi}+V_A)$. This barrier reduces the amount of electrons that can get into the metal. The electrons flowing from the metal to the semiconductor remains the same as in the forward bias case because the Φ_B barrier remains unchanged. The reverse current flows from semiconductor to metal.

2.3.2 Ohmic Metal-Semiconductor Contacts

The band diagram for a metal and an n-type semiconductor where the work function of the semiconductor is higher than that of the metal, $\Phi_S > \Phi_M$, is shown in Figure 8.
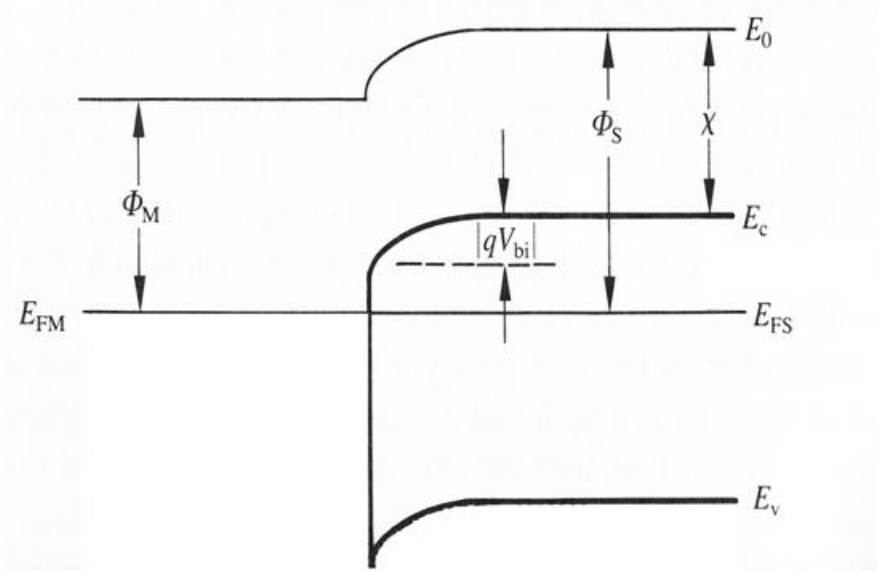
Figure 8. Band–diagram of an ohmic metal-semiconductor contact

When the two materials are brought into contact electrons flow from. the metal to the n-type semiconductor. Electrons have accumulated at the semiconductor surface, making the electron concentration higher than in the bulk. The surface charge in the semiconductor consists of free electrons which was not the case for the Schottky contact where the surface consisted of positive donor ions that caused the formation of a depletion region. In the ohmic contact due to the absence of the depletion region the voltage drop across the junction at any bias is negligible. From Figure 8, the electrons in the conduction band of the

semiconductor see no potential barrier towards the metal. An ohmic contact can be also formed between a p-type semiconductor and a metal when the work function of the metal is higher than that of the p-type semiconductor, $\Phi_M > \Phi_S$.

In reality is difficult to find the right work function combinations to obtain an ohmic contact and therefore a different technique is used. The p or n-type semiconductor is heavily doped making the depletion width very narrow. As a consequence the electrons from the metal can tunnel through the barrier when negative voltage is applied to the metal as shown in Figure 9(a). Figure 9(b) shows the case where negative voltage is applied to the semiconductor. Electrons from the semiconductor not only go over the reduced barrier but also tunnel through the potential barrier.
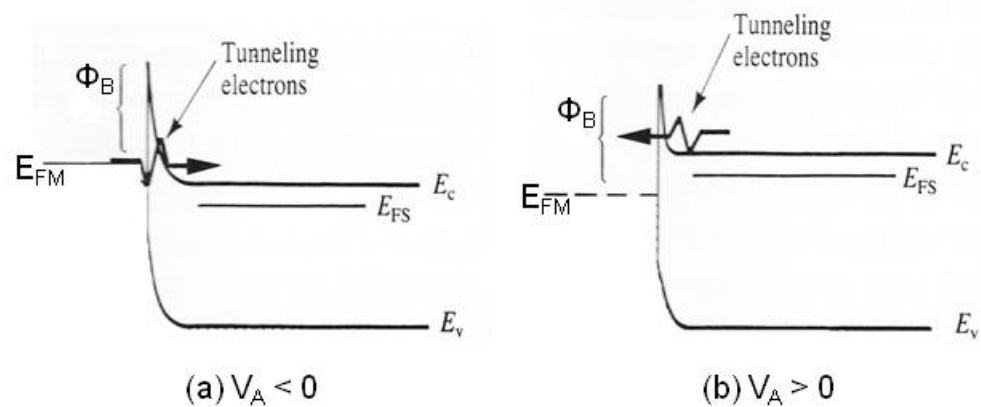
Figure 9. Ohmic metal-semiconductor contact with (a) negative and (b) positive voltage at the metal

2.4 Semiconductor Heterojunctions

In the discussion of pn junctions in the previous sections, the semiconductor material was the same throughout the entire device. This type of junction is called a homojunction. When two different semiconductor materials are used to form a junction, the junction is called a heterojunction. There are two basic types of heterojunctions. Those in which the conductivity of the materials is the same and the junction is called an isotype and those in which the conductivity of the materials is different and the junction is called an anisotype.

Figure 10 shows the energy-band diagrams of an n and p type semiconductors before contact.
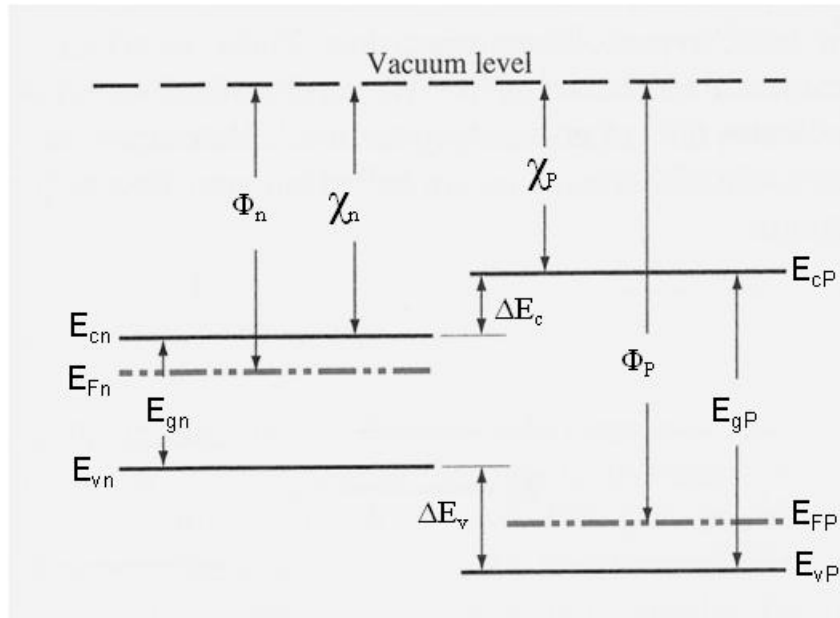
Figure 10. Energy band diagrams of an n-p heterojunction before contact

E_{gn} and E_{gP} are the bandgaps, Φ_n and Φ_P are the Fermi levels, and χ_n and χ_P are the electron affinities of the n and p-type semiconductors respectively. The difference between the two valence band energies is given by ΔE_V, and the difference between the two conduction bands is given by ΔE_C. From figure 9

$$\Delta Ec = \chi_P - \chi_n \tag{5}$$

and

$$\Delta Ev = E_{gP} - E_{gn} - \Delta Ec \tag{6}$$

Figure 11 shows the band diagram of an n-p heterojunction in equilibrium.
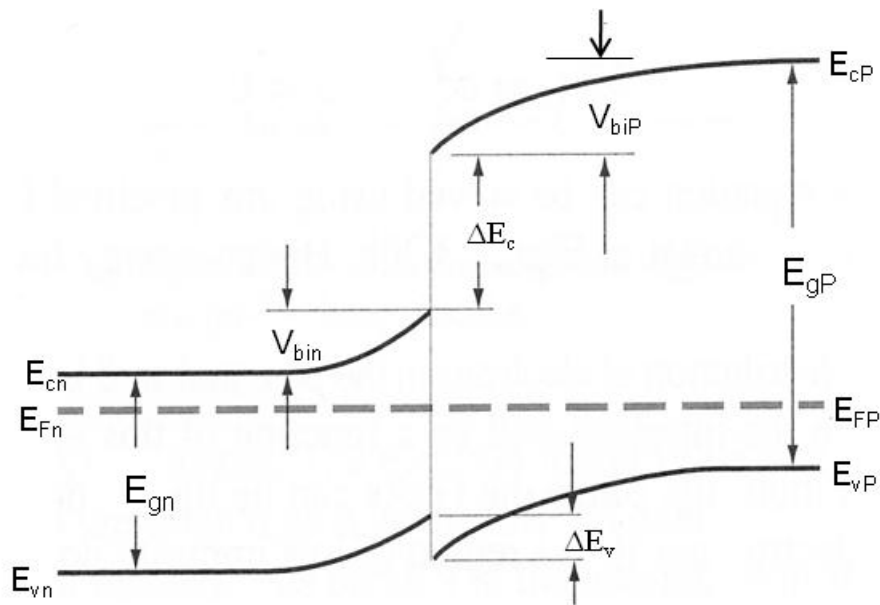
Figure 11. Energy band diagram of an n-p heterojunction in thermal equilibrium

In order for the Fermi levels in the two materials to become aligned, electrons from the n region and holes from the p region must flow across the junction creating a depletion region as in the case of a homojunction. Potential

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differences exist across the depletion regions in both the n and p regions which correspond to the built in potential barriers on either side of the junction. The total built in potential barrier is given by

$$V_{bi} = V_{bin} + V_{biP} \qquad\qquad (7)$$

The valence and conduction discontinuities, ΔE_c and ΔE_v, in Figure 11 given by equations, 5 and 6 respectively are based on an ideal abrupt heterojunction. Experimentally determined values of ΔE_c and ΔE_v usually differ from the ideal ones due to the presence of interface states at the junction.

Under forward or reverse bias the change in the band diagram of a heterojunction at the interface region is very similar to that of a homojunction. If a reverse bias voltage, V_A, is applied across the heterojunction V_{bi} is replaced with $V_{bi} + V_A$. Similarly, if forward bias is applied V_{bi} is replaced with $V_{bi} - V_A$. One difference between a homojunction and a heterojunction is the barrier heights seen by the holes and electrons. The potential barrier for electrons and holes in a homojunction is the same and therefore the magnitude of hole and electron currents is determines by the doping levels. In a heterojunction the barrier heights seen by electrons and holes are not the same. The barrier height for electrons in Figure 11 is larger than for holes. Therefore, the hole injection over the barrier is much more efficient that the electron injection.

2.5 Solar Cells

A solar cell is a device that converts the energy of sunlight directly into electricity by the photovoltaic effect. The first pn junction silicon solar cell was developed by Chapin, Fuller, and Pearson in 1954. Solar cells are made using different device configurations and employing single-crystal, polycrystal and amorphous structures.

2.5.1 Solar Spectrum

The intensity of solar radiation in free space at the average distance of the earth from the sun is defined as the solar constant. This is known as the solar constant of air mass zero (AM0), which represents the solar spectrum outside the earth's atmosphere and is the standard used for satellite and space-vehicle applications. Measurements taken at high altitudes have yielded the currently accepted average value of 1.353 kW/m^2. On earth at sea level with the sun at zenith the power level is reduced to 0.925 kW/m^2. This is the AM1 spectrum. AM1.5 is the adopted terrestrial standard that allows a meaningful comparison of different solar cells. It has a value of 0.844 kW/m^2, even though the value of 1000 W/m^2 was incorporated to become a standard. This value is close to the maximum received at the earth's surface.

The energy of the light incident on a semiconductor in terms of wavelength in the light spectrum can be obtained from the relationship

$$\lambda = \frac{c}{v} = \frac{1.24}{hv} \mu m \tag{8}$$

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where v is the frequency in Hertz, c is the velocity of light in m/s and h v is the photon energy in eV. Figure 12 shows a typical p-n heterojunction band diagram in thermal equilibrium.
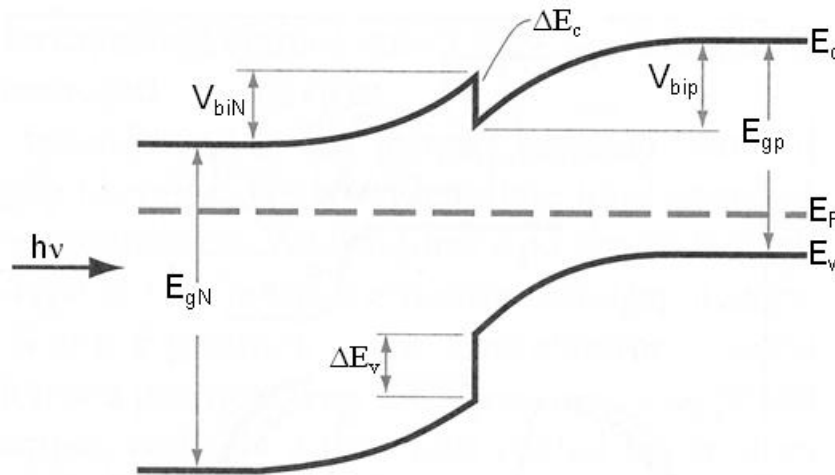
Figure 12. Energy-band diagram of a p-n heterojunction in thermal equilibrium

Photons with energy, hv, less than E_{gN} will pass though the wide-bandgap material and photons with energies greater than E_{gp} will be absorbed in the narrow-bandgap material. Carriers created in the depletion region and close to the junction will be collected and will contribute to the photocurrent. Photons with energy greater than E_{gN} will be absorbed in the n region and carriers collected near the junction will be collected. This type of heterojunction solar cell should have better characteristics than a homojunction, since more photons will penetrate the p-region without being absorbed in the n region resulting in more photogenerated carriers.

2.5.2 Solar Cell Parameters

The parameters of interest in evaluating a solar cell are the values of the short circuit current (I_{sc}), open circuit voltage (V_{oc}), fill factor (FF) and the energy conversion efficiency (η). Figure 13 shows the I-V characteristics of a solar cell in the dark and under illumination.
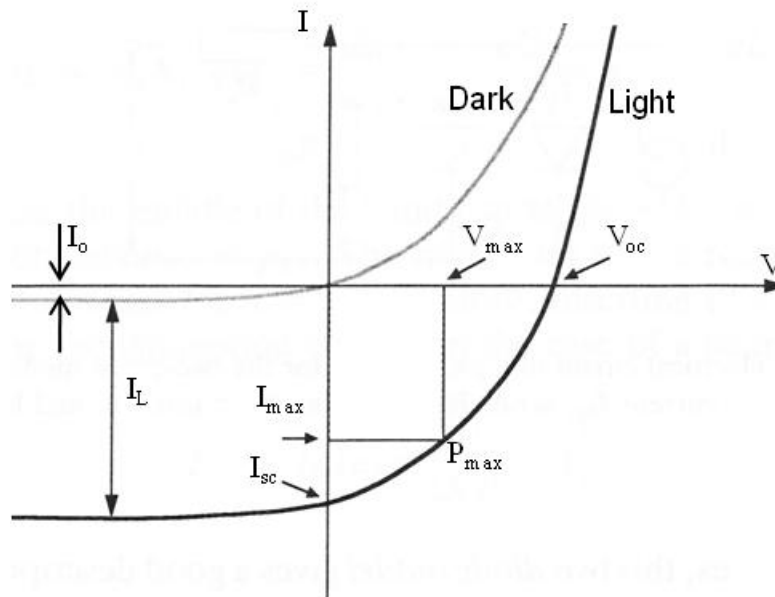
Figure 13. I-V curve of the solar cell in the Dark and under Illumination

The total current is given by

$$I = I_s \times \left(e^{\frac{qV}{AkT}} - 1 \right) - I_L \qquad (9)$$

Where I_s, is the reverse saturation current and I_L is the light generated current. In the fourth quadrant the I-V product is negative, indicating that the solar cell can

deliver power to a load. I_{sc} is defined as the current flowing in the circuit when the applied voltage is zero. Setting V=0, equation 9, gives $I_{sc}=I_L$.

V_{oc} is the voltage output when the attached load is infinite and from equation 9, setting I=0 the equation for V_{oc} is given by

$$V_{oc} = \frac{AkT}{q} \times \ln\left(\frac{I_L}{I_S} + 1\right) \tag{10}$$

From Figure 13, I_{max} and V_{max} are the current and voltage corresponding to the maximum power that can be generated by the device. The maximum possible area $P_{max} = I_{max} V_{max}$ for a given current voltage curve determined the FF, which is defined by

$$FF = \frac{Vmax\ Imax}{Voc\ Isc} \tag{11}$$

The three parameters V_{oc}, I_{sc} and FF are sufficient to calculate the conversion efficiency η of the solar cell, given by the following expression

$$\eta = \frac{Pmax}{Pin} = \frac{Voc\ FF\ Isc}{Pin} \tag{12}$$

where P_{in}, is the incident light power.

The efficiency of a solar cell is influence by series (R_s), and shunt (R_{sh}) resistance. For an ideal solar cell the series resistance is zero and the shunt resistance is infinite. All real solar cells are characterized by a finite shunt and series resistance.

Taking into consideration the series and shunt resistance equation 9 becomes

$$I = I_S \times \left(e^{\frac{q(V-IRs)}{AkT}} - 1\right) - I_L + \frac{I_L+(V-IRsh)}{Rsh} \tag{13}$$

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The series resistance is caused by the resistance due to the contacts and the bulk of the device material. Defects like pinholes, grain boundaries and dislocations in the solar cell are responsible for low shunt resistance. A low shunt resistance produces high leakage currents which decrease the values of V_{oc} and FF. Series resistance also reduces the FF.

Figure 14 shows the equivalent circuit of a solar cell with series and shunt resistances.
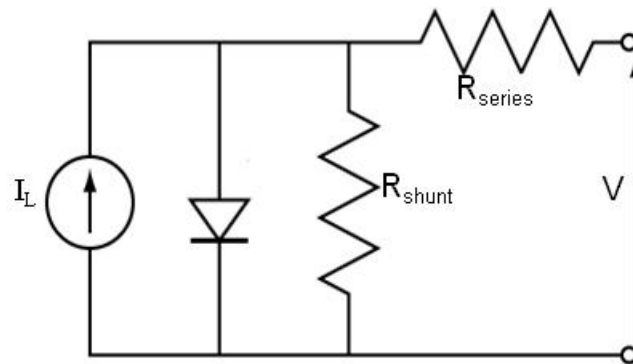
Figure 14. Equivalent circuit of a solar cell with series and shunt resistance

CHAPTER 3

THE CdTe/CdS THIN FILM SOLAR CELL

3.1 Superstrate Configuration

Figure 15 shows the typical superstrate configuration. A Transparent Contact (TC) is deposited on glass substrate followed by the deposition of CdS, CdTe, and the back contact.
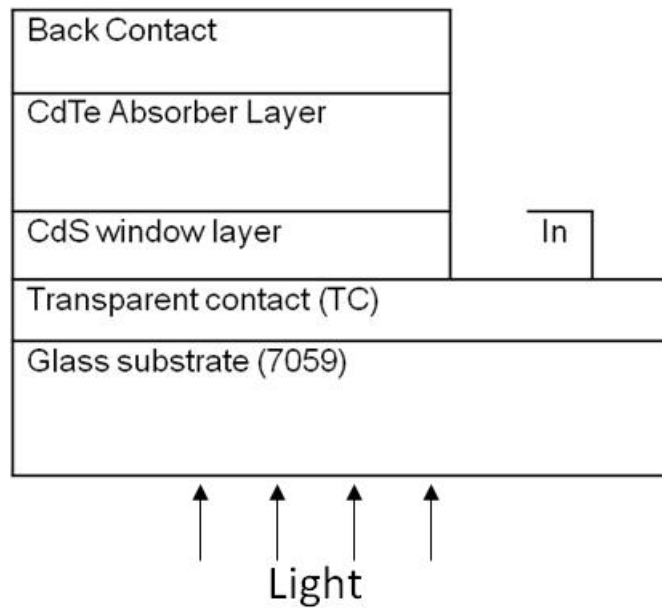
Figure 15. CdTe superstrate solar cell

3.2 Glass Substrate

The highest efficiencies in CdTe solar cells have been obtained under high substrate temperatures (~550 °C). Alkali free glass is used as it can withstand these high temperatures, and has a high optical transmission. However, industry uses soda lime glass due to its low cost.

3.3 Transparent Contacting Oxides (TCOs)

Transparent conducting oxides have optical and electrical properties well suited to act as transparent contacts for thin-film solar cells. A highly transparent and conducting oxide with proper properties is required to form an ohmic contact with the CdS layer, mainly, the electron affinity has to be less than 4.5eV. If the electron affinity of the TCO is higher than that of the CdS a Schottky contact is formed.

The characteristics required for a TCO to be used as a front contact are:

- Low resistivity $<10^{-4}$ Ω cm

- High transparency in the 400-850 nm range

- Good stability at the processing temperatures of the other layers of the solar cell

Transparent oxides in a pure intrinsic, stoichiometric and undoped state are usually insulators due to their wide bandgaps. Since good electrical conductivity is desired different methods are employed to increase the conductivity of the TCO's. The most common way is doping. This is achieved by the substitution of valence cations by donor impurities in the oxide which

increases the n-type conductivity by increasing the electron concentration. The most common TCO's for CdTe solar cells are fluorine doped tin-oxide SnO_2: F (FTO), tin doped indium oxide In_2O_3: Sn (ITO) and cadmium stannate Cd_2SnO_4 (CTO). These metallic oxides exhibit very good optical transparency ~90% and very high n-type conductivity. Studies have shown that the solar cell performance improved with the use of bi-layer transparent contacts (TC), one that consists of a low resistive layer (low-ρ) followed by a high resistive layer (high-ρ) [3]. The use of a high-ρ layer, referred also as buffer layer, has been found to maintain high FF's and Voc's while using thinner CdS layers. It has been suggested that the use of high-ρ layer next to CdS serves as a high bandgap extension of the thin CdS [4]. It is also believed that the high-ρ layer acts as an insulator preventing possible shunts through the thin CdS. Table 1 shows the properties of some of the most common TCO's and buffer layers.

Table 1. Properties of transparent conducting oxides and buffer layers [3]

Material	Resistivity (Ω cm)	Transparency (%)
SnO_2	8×10^{-4}	80
SnO_2:F	4×10^{-4}	84
In_2O_3:Sn	2×10^{-4}	85
Cd_2SnO_4	2×10^{-4}	92

3.3.1 Fluorine Doped Tin Oxide (FTO)

SnO_2 (TO) is one of the most widely used transparent oxides. TO films are deposited by Chemical Vapor Deposition [5, 6] and by R.F sputtering.

In CVD a film is deposited onto a substrate from gas or liquid reactants supplied and pre-mixed close to the deposition zone. Inorganic and metal-organic precursors are used for the deposition of TO films such as tin tetrachloride ($SnCl_4$), dimethyltindichloride (($CH_3)_2SnCl_2$), tetramethylin ($Sn(CH_3)_4$), and oxygen (O_2). In TO films the n-type conductivity is primarily due to Oxygen-vacancies, but the resistivity of the films is not low enough to be used as front TCO's for the solar cells. To increase the conductivity of the TO films pre-cursors containing HF (hydrogen-fluoride) acid is used. This way fluorine is used to dope the TO producing films with high conductivity.

CVD is a complicated process that utilizes ~10% of the reagent species. For this reason sputtering is the most utilized technique for the deposition of TCO's in general. A. Bosio et al. studied typical sputtering parameters for the deposition of low resistivity TCO films [7]. TO films prepared by sputtering in Ar atmosphere from a SnO_2 target yielded a resistivity of 10^{-1} Ω cm and an optical transparency of 90% in the visible region.

Films were deposited by introducing CHF_3 in the range 1-10% with respect to the total Ar + CHF_3 pressure during sputtering. The minimum resistivity achieved was about 8 x 10^{-4} Ω cm.

3.3.2 Tin Doped Indium Oxide (ITO)

Indium tin oxide (ITO) is another widely used front contact material for solar cells. D.C and R.F sputtering, spray pyrolysis, chemical vapor deposition and vacuum evaporation are the most common techniques for the deposition of ITO films. Tin acts as a cationic dopant in the In_2O_3 lattice and substitutes the indium providing an electron in the conduction band resulting in n-type doping. The best ITO films are deposited using R.F sputtering [8]. R.B.H. Tahr et al. reported resistivities of 1.8×10^{-4} Ω cm.

N. Romeo et al. prepared ITO films by R.F sputtering from different targets with different stoichiometries [9]. In_2O_3 containing 1, 2, 4 and 10% weight of SnO_2 were used. Depositions were carried under different ambient conditions. ITO films were deposited in a gas mixture containing Ar + O_2 and Ar + H_2. Oxygen and hydrogen partial pressures were varied between 2-20% and 1-10% respectively. All films exhibited very low resistivities of 2×10^{-4} Ω cm. The stoichiometry of the targets and the ambient used during the depositions did not affect the resistivity of the films, meaning that tin is an effective dopant and the doping level does not depend on oxygen vacancies.

3.3.3 Cadmium Stannate Oxide (CTO)

The highest efficiency CdS/CdTe ever made used cadmium stannate as the front transparent contact [1]. CTO films are prepared by RF sputtering.

R. Mamazza et al. prepared Cd_2SnO_4 films by RF co-sputtering from cadmium oxide (CdO) and tin oxide (SnO_2) targets in an argon ambient and room

temperature [10]. The as deposited films were amorphous and were subjected to high annealing temperatures to improve their structural properties. It was determined that the films began to crystallize at approximately 550 °C. Films with excess Cd produced the lowest resistivities. Such films exhibited charge carrier densities of 7.40×10^{20} cm^{-3}. Cd_2SnO_4 thin films with resistivities as low as 2.01×10^{-4} Ω cm, and average optical transmission (between 400 and 900 nm) in excess of 90% were produced.

X. Wu et al. deposited Cd_2SnO_4 films in pure oxygen ambient and at room temperature from a CTO target [11]. The CTO films were annealed at 600-660 °C in argon. Electrical resistivities as low as 1.5×10^{-4} Ω cm were achieved. The low resistivities of CTO films are due to its high carrier concentration and high mobility. CTO films have better optical properties than tin oxide and indium tin oxide films due to their high conductivity which allows for thinner films to be used. The main disadvantage of the CTO films are the high processing temperatures, >550 °C, required to produce high quality TCO layers.

3.4 The Cadmium Sulfide (CdS) Layer

The CdS film in the CdTe/CdS solar cell is the so-called window layer. Since it is n-type it enables the formation of a p-n junction with p-type CdTe. With an energy gap of 2.42eV, CdS is mostly transparent in the visible part of the solar spectrum, allowing the solar light to penetrate into the CdTe layer thus giving rise to the photovoltaic effect.

The maximum theoretical value of the short circuit current (J_{sc}) in CdS/CdTe solar cells is ~30 mA/cm^2. Based on AM1.5 data the CdS layer absorbs the equivalent of about 7 mA/cm^2 [12]. Due to the poor properties of the CdS layer, low hole lifetime and high recombination, most of the photo-generated carriers in this layer contribute negligible photocurrent and therefore constitutes a current loss for the wavelength range below 510 nm. To minimize these losses it is necessary to minimize the thickness of the CdS layer (~100nm). The junction quality in the device depends on maintaining a uniform and continuous interface to avoid the formation of pinholes which will create parallel junctions between CdTe and the transparent contacting oxide. Chemical bath deposition (CBD) and chemical surface deposition (CSD) [13], are the most promising deposition methods for thin (<100nm) uniform CdS layers.

The lattice mismatch between CdS and CdTe is ~9%. This reduces the amount of strain and therefore the amount of defects at the interface. A key reason for the high quality and efficient CdTe/CdS junctions is the formation of an interfacial layer of $CdS_{1-x}Te_x$ during the cell fabrication [14]. The formation of this layer is believed to be responsible for lowering the interfacial defect density resulting in high efficiency devices [15]. There are several techniques for the deposition of CdS like Chemical Bath Deposition (CBD) [16], Close Spaced Sublimation (CSS) [17], spray pyrolysis [18] and R.F sputtering [19].

Although the highest energy conversion efficiencies were obtained by using a CdS layer prepared by CBD, it is preferred to use the sputtering or CSS deposition method since CBD is not suitable for large-scale production.

3.4.1 CdS by Chemical Bath Deposition (CBD)

The highest efficiency CdS/CdTe solar cell used the CBD technique for the deposition of the CdS layer. CBD is a low-cost simple technique to achieve good quality CdS films needed to obtain high efficiency CdS/CdTe solar cells. CBD CdS films can be deposited using an "acetate-based" process. Cadmium acetate is used as cadmium source, thiourea is used as sulfur source, ammonium acetate (NH_4AC) and ammonium hydroxide (NH_4OH) are used as buffers to control the PH value. A solution is prepared by mixing specific amounts of CdAc, NH_4AC and NH_4OH and by adding thiourea at specific intervals during the deposition. The thickness of CdS can be changed by varying the deposition time. J. Herrero et al. [20] proposed the possible reactions as follows:

$$Cd(CH_3COO)_2 \leftrightarrow Cd^{2+} + 2CH_3COO^-$$

$$NH_3 + HOH \leftrightarrow NH_4^+ + OH^-$$

$$Cd(NH_3)_4^{2+} + 2OH^- \leftrightarrow [Cd(OH)_2(NH_3)_2] + 2NH_3$$

$$[Cd(OH)_2(NH_3)_2] + SC(NH_2)_2 \rightarrow [Cd(OH)_2(NH_3)_2SC(NH_2)_2$$

$$[Cd(OH)_2(NH_3)_2SC(NH_2)_2] \rightarrow CdS_{(S)} + CN_3H_5 + NH_3 + 2HOH$$
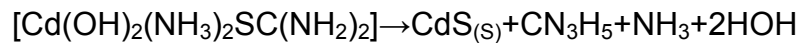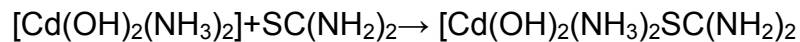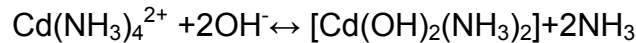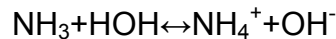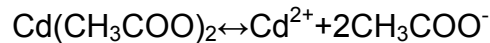
As deposited films might contain the two crystalline structures of CdS, the cubic and the hexagonal. Annealing of the CBD films at temperatures around 400°C increases the percentage of the hexagonal grain orientation which is more stable than the cubic orientation and also provides films with an energy gap of 2.42eV [7].

3.4.2 CdS by Close-Spaced Sublimation (CSS)

The deposition of CdS films by CSS is based on the reversible dissociation of CdS at high temperature. The CdS dissociates into its elements which recombine on the substrate to form the CdS film. D. Marinskiy et al. [21] studied the effects of the CSS CdS on the performance of the CdS/CdTe solar cells. High efficiency devices ~15% were achieved using CdS by the CSS method. Samples where the CdS layer was deposited in He and He+O_2 ambient were fabricated. Samples fabricated in oxygen ambient showed a reduction in sulfur vacancies as a result of O_2 incorporation in the CdS. The performance of the cells increased when the CdS (CSS) films were subjected to a heat treatment.

3.5 The Cadmium Telluride (CdTe) Layer

Cadmium telluride is a II-IV semiconductor with properties that make it an ideal absorber layer for solar cells. Figure 16 shows the theoretical efficiency-bandgap relationship. It is maximum close to 1.5eV. CdTe has a bandgap of 1.45eV. CdTe is a direct bandgap material with high absorption coefficient of 10^4 cm^{-1}. This means that only a few micrometers (~2μm) of material are enough to absorb nearly 100% of the incident radiation.
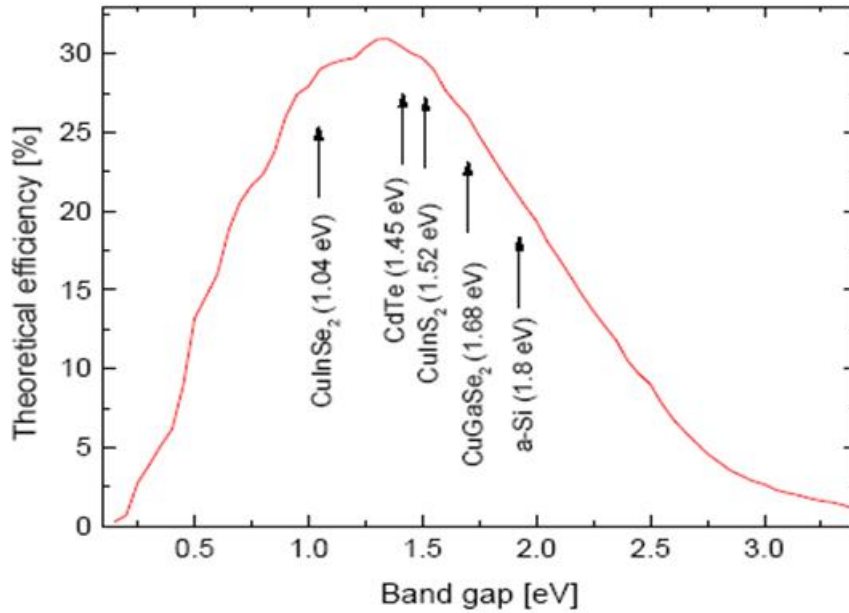
Figure 16. Theoretical efficiency for a given bandgap (AM 1.5 illumination)

Depending on the method and the conditions used during deposition, the CdTe film can be grown self-doped by both cadmium and tellurium vacancies. Cadmium vacancies cause the film to exhibit p-type conductivity while tellurium vacancies cause the film to exhibit n-type conductivity. Several methods have been used to deposit polycrystalline CdTe films. The most common deposition methods are sputtering [22], electrodeposition [23], [24], screen printing [25], metal-organic chemical vapor deposition [26] and close-spaced sublimation (CSS) [27], [28].

3.5.1 CdTe by Close-Spaced Sublimation (CSS)

The most efficient CdTe solar cells have been fabricated using the CSS method for the deposition of the CdTe layer. The deposition of the CdTe films by

the CSS method is based on the reversible dissociation of CdTe at high temperature. The CdTe dissociates into its elements

$$2CdTe(s) \leftrightarrow 2\ Cd(g) + Te_2(g)$$
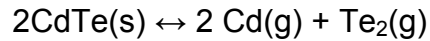
which recombine on the substrate surface to form the CdTe film.

As mentioned previously the formation of the CdS_xTe_{1-x} layer is beneficial to the solar cell by improving the quality of the CdS/CdTe junction and the high temperature associated with the CSS leads to the formation of this layer. The CSS technique is known to produce high quality films because of the large crystalline grain size which means a low defect density compared with other processes like sputtering and physical vapor deposition that produce small grains.

Many research groups found that CdTe films deposited by CSS in oxygen containing ambient exhibited better crystalline and electro-optical properties. The use of oxygen increases the p-type characteristics of CdTe and reduces the grain size making the film more compact with decreased pinhole density [29].

3.6 CdCl$_2$ Heat Treatment (HT)

An essential processing step for fabricating high efficiency CdTe/CdS solar cells is the heat treatment in the presence of CdCl$_2$. The CdCl$_2$ treatment improves the overall performance of the cells due to morphological and electronic changes that occur during the process.

This treatment is generally carried out by depositing a CdCl$_2$ film on top of the CdTe by dipping the film in a CdCl$_2$-methanol solution or by evaporation [30,

31]. The film is then annealed in air or in ambient containing oxygen. $CdCl_2$ vapor treatment is another method used which is also applicable for large-scale manufacturing because it eliminates the need to rinse excess amounts of $CdCl_2$ residue on the film surface associated with the two previous methods [32, 33].

Structural changes have been observed for CdS/CdTe films that were $CdCl_2$ treated. CBD CdS films recrystallize causing the film to have lower density of defects better crystallinity and larger grain size [34]. CSS CdS films grown at higher temperatures have much better crystallinity than CBD CdS films and even though the $CdCl_2$ HT does not affect much the grain size or crystallinity of the film, it decreases the amount of intragrain strain [34].

In low-temperature grown CdTe films the grain size is <1 μm and the $CdCl_2$ HT results in grain growth and recrystallization. During recrystallization structural defects become mobile and form new grain boundaries that relieve internal stress in the CdTe film [35]. Grain growth is influenced by the reaction temperature and the oxygen amount. Higher temperatures and increasing oxygen concentration promote grain growth. Sulfur diffusion into the CdTe film is also enhanced with higher oxygen concentration which leads to the CdS thinning [33].

CdTe films deposited by high temperature processes like CSS exhibit large grain structure, usually >2 μm. The $CdCl_2$ treatment does not increase the grain size, but it rather eliminates smaller grains [36]. Unlike the low-temperature grown CdTe films, the oxygen concentration during $CdCl_2$ HT does not influence the consumption of the CdS film [37].

It was also found also that this HT facilitates interdiffusion of S and Te near the CdTe/CdS junction which improves the electronic properties of the CdS/CdTe junction by reducing interface recombination [38, 39]. Sulphur diffuses into the CdTe layer creating a $CdTe_{1-x}S_x$ layer. The incorporation of S into CdTe reduces the bandgap of CdTe and enhances carrier collection in the long wavelengths of the spectrum.

The presence of oxygen during the $CdCl_2$ treatment enhances the performance of the CdS/CdTe solar cell. An increase of the shallow-acceptors concentration was observed giving rise to additional p-type CdTe doping [40]. In particular, the grain boundary regions become more p-doped, owing to grain boundary diffusion of chlorine and oxygen, and increased photo-carrier collection efficiency is measured [41].

3.7 Back Contact

The formation of stable, low resistance and non-rectifying contact to p-CdTe is the biggest challenge in the fabrication of high efficient solar cells. P-type CdTe is a semiconductor with a high electron affinity (χ=4.5 eV) and a bandgap of 1.45 eV that makes the work function close to 5.8eV. To form an ohmic contact, the metal used for the contact should have a work function greater than that of p-type CdTe. This aligns the metal Fermi level with the upper valence band edge. Unfortunately there are no metals available with the appropriate high work function to form the ohmic contact on CdTe. Use of lower work function metals result in the formation of Schottky barriers at the back contact. The

presence of back contact barriers can affect the current-voltage characteristics of the solar cell usually by impeding hole transport.

As an alternative approach, pseudo-ohmic contacts can be made by heavily doping the semiconductor adjacent to the contact generating a very thin barrier that can be crossed by charge carriers through tunneling.

The electrical properties of II-VI semiconductors are usually determined by a departure from a 1:1 stoichiometry, which leads to the presence of intrinsic defects. These native defects are the result of the preparation conditions as well as by post heat treatments. For CdTe such defects are Cd vacancies (V_{CD}), Cd interstitials (Cd_i), Te vacancies (V_{TE}) and Te interstitials (Te_i). V_{TE} and Cd_i act as donors while V_{CD} and Te_i act as acceptors. These native defects are the main reason for the doping limit due to self-compensation. Furthermore, acceptors cannot be introduced by diffusion-doping from the surface, as dopants diffuse preferentially along the grain boundaries.

Due to the difficulty in doping polycrystalline CdTe two different approaches are implemented for fabricating pseudo-ohmic contacts. The first approach involves a surface treatment to produce a p^+-surface which is a Te-rich layer, followed by the deposition of a metallic contacting material. In the second approach an interlayer or buffer layer of another semiconductor which has a suitable valence band with CdTe is used. In some cases these buffer layers can be highly doped p-type at the interface with the metal contact.

3.7.1 Etching of CdTe

Prior to contacting the CdTe surface must be modified as mentioned above. Etching of the CdTe surface accomplishes two things. It provides a Te-rich layer and removes any residual oxides from the CdTe surface that might have been formed during the $CdCl_2$ treatment. Etching can be classified as wet or dry depending on the medium used. Based on the mechanism, dry etching can be divided into physical sputtering, reactive ion etching and plasma etching. The most widely used approach for CdTe etching has been the wet chemical etching.

The most common etchants used for wet etching are Br_2/methanol solutions (BM) [42], aqueous nitric acid/phosphoric acid mixtures (NP) [43] and chromate etches ($K_2Cr_2O_7$:H_2SO_4) [42].

While CdTe etching prior to contact deposition is used for the formation of low-resistance contacts, improvements in cell performance have been shown with post-contact etching due to the removal of oxides in the contact or even CdTe oxides from beneath the contact.

Currently, different kinds of back contacts have been achieved; they can be classified into two categories: copper containing back contacts and copper-free contacts.

3.7.2 Copper Containing Back Contacts

A dual role has been proposed for the effect of Cu in CdTe/CdS solar cells when used for the fabrication of back contacts. It is generally accepted that Cu

increases the p-doping of CdTe near or at the back contact interface which causes the formation of better ohmic contacts. At the same time, however, because of its ability to diffuse through the polycrystalline CdTe film to the cell junction is considered to be the main component responsible for the degradation of the solar cell.

The most commonly used copper containing contacts are Cu/Au, Cu_2Te, ZnTe doped with Cu and graphite pastes doped with Cu.

3.7.2.1 Gold/Copper (Au/Cu) Contacts

Chou et.al [44], studied the effects of Cu on CdTe solar cells with Au/Cu contacts. Cu and Au were sequentially evaporated to form the back contact. Cu thickness was varied from 0 to 300 Å. After the metallization the cell was annealed at 150 °C in Ar ambient followed by Br_2-methanol etching. Secondary Ion Mass Spectroscopy (SIMS) analysis showed that Cu had penetrated into the CdTe reaching all the way to the CdTe/CdS interface. Annealing of the cell had no significant change in the Cu profile. This leads to the conclusion that Cu diffuses into CdTe during metallization, along the grain boundaries.

C-V measurements were performed to investigate changes in the doping concentration. Cells with Au/Cu back contact showed the acceptor concentration to decrease from the CdTe surface toward the CdTe/CdS interface. Acceptor concentration was lower with a flat profile for cells with only Au contact. The enhanced acceptor concentration with addition of Cu supports the evidence of Cu diffusion into CdTe.

I-V measurements showed that both series and shunt resistances decrease with the increase in Cu thickness. This is probably because the increase in Cu thickness results in better back contact which reduces series resistance but the excess Cu causes shunt paths that reduce the shunt resistance.

The conclusion derived, was that the copper helps the formation of better ohmic contacts and increases the doping concentration due to interstitials occupying Cd sites. Excess Cu diffuses to the junction where it forms recombination centers and shunt paths that degrade the cell performance.

3.7.2.2 Copper Telluride (Cu_2Te) Contacts

Several techniques are employed for the formation of Cu_2Te back contacts. These include R.F sputtering of a Cu_2Te target, evaporation of Cu_2Te powder and evaporation of Cu on previously etched CdTe surface.

Cu_2Te back contacts by R.F sputtering were studied at USF [45]. Cu_2Te was deposited on etched CdTe followed by the deposition of Molybdenum (Mo) as the final metal layer. Cu_2Te films were sputtered under different substrate temperatures and composition was determined using Energy dispersive X-ray analysis (EDS). Nearly stoichiometric films of Cu_2Te were obtained at 250 °C. Thickness and annealing temperatures affected the performance of the solar cells. Cu_2Te thickness of less than 50 Å gave low field factors (FF's) due to high series resistance, whereas thicknesses in excess of 100 Å gave low shunt resistances due to the formation of shunting paths. A Cu_2Te thickness of ~50 Å

gave the best results. The substrate temperature was varied during the deposition. Degradation in device performance was observed for high deposition temperatures > 300 °C, associated with low shunt resistances. Excessive Cu diffusion along the grain boundaries is believed to be the reason for the poor cell performance. Best results were obtained for Cu_2Te films deposited at 250 °C.

J. H. Yun et.al [46], utilized the Cu_2Te layer as a Cu source for doping CdTe and as an electrode material. Cu_2Te layer was deposited on the CdTe film at room temperature by evaporating Cu_2Te powder. The samples were annealed at various temperatures and then an Au layer was deposited and annealed as a secondary electrode.

An amorphous layer was found at the $CdTe/Cu_2Te$ interface by depositing Cu_2Te at room temperature and disappeared by annealing at 200 °C. Minimum contact resistance of CdTe cell and highest efficiency was obtained for samples annealed at 180 °C. Degradation was observed for samples annealed at over 200 °C due to an increase in series resistance that resulted from a Schottky back contact.

J. Chou et al. [47], studied the formation of different phases of Cu_xTe. Cu layers of different thicknesses were evaporated on etched CdTe followed by annealing at different temperatures. Several Cu_xTe phases were observed after post-annealing at 250 °C. CuTe, $Cu_{1.4}Te$ and Cu_2Te were the main phases detected. Best device performance was achieved when the CuTe and $Cu_{1.4}Te$ phases were present. Cells with a Cu_2Te layer had poor performance with low Voc's and FF's caused by shunting. The large amount of Cu used to create the

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Cu$_2$Te layer provided more Cu to diffuse into the front region along grain boundaries, which should be the reason for the increased shunting.

3.7.2.3 Copper Doped Zinc Telluride (ZnTe : Cu) Contacts

As mentioned before an interlayer or buffer layer of another semiconductor which has a suitable valence band with CdTe and that can be highly doped p-type at the interface with the metal contact, can be used to form ohmic contact.

Vacuum-evaporated Cu-doped zinc-telluride (ZnTe) films have been used as the intermediate layer between CdTe and metal contacts achieving an efficiency of 12.9% [48]. Copper concentration of 4.3 – 7.5% gave similar results, while a further increase in the Cu reduced the FF. ZnTe post-deposition annealing was necessary to improve the performance of the cells, 200 °C being the optimum temperature. Au and Ni were used as the final metal on the cells. Ni contacted cells gave lower FF's and Voc's and degraded faster compared to the cells made with an Au as the back metal. It was found that interdiffusion takes place in Au contacted cells, whereas no changes were observed for Ni contacted cells [49]. The amount of Cu diffusing into CdTe is limited by the consumption of Cu by the Au layer. This might explain the difference in degradation between Au- and Ni- contacted cells.

T. A. Gassert et al. [50], used the sputtering technique to deposit ZnTe:Cu/Ti contacts for CdTe/CdS devices. Deposition temperature was critical to the performance of the solar cells [51]. SIMs analysis showed that increasing

the temperature resulted in increase of the Cu concentration in the CdTe and CdS layers. C-V analysis revealed that the depletion width decreased with increased contacting temperature which is consistent with the SIMS findings. At high temperatures >360 °C, excessive Cu diffusion, resulted a loss in the collection of carriers generated deep in the CdTe because of the depletion width being too narrow. Best results were obtained for contacts deposited at 320 °C.

3.7.2.4 Doped Graphite Paste

The highest efficiencies for CdS/CdTe solar cells have been achieved using doped graphite paste as the back contact [1, 52]. The procedure consisted of etching the CdTe surface to produce a Te rich surface, application of graphite paste doped with a mixture of HgTe:Cu followed by low temperature annealing (250-275 °C). It is believed that highly p-doped layers of Cu_2Te and $Hg_{1-x}Cd_xTe$ are formed that provide tunneling across the contact [53].

3.7.2.5 Cu Related Issues

Addition of Cu is commonly used to obtain better back contacts and therefore improving the performance of CdS/CdTe solar cells. Copper can form a $Cu_{2-x}Te$ layer and increase the effective doping in the CdTe at the back contact that lowers the back-contact barrier. The presence of Cu also leads to poor stability of cells under stress. Cu is known to be a fast diffuser in CdTe [54]. Most likely Cu diffuses along grain boundaries reaching the cell junction and the CdS layer. At the cell junction it was proposed that Cu forms recombination centers

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and shunt pathways that cause the degradation and instability of the cell. Cu depletion from the back contact may result in the formation of a back-contact barrier expressed as a roll-over in the J-V characteristics of the solar cell [55].

3.7.3 Copper Free Back Contacts

To overcome the stability issues associated with Cu-containing back contacts, effort has been made to fabricate back contacts containing no Cu, such as mercury-telluride (HgTe), nickel phosphide (Ni-P), antimony telluride (Sb_2Te_3) and zinc-telluride (ZnTe).

3.7.3.1 HgTe Back Contacts

Mercury Telluride is a semimetal with a reported high work function of ~5.9 eV and a nearly matched lattice parameter to CdTe than can be used as an ohmic back contact. HgTe contacts based on graded heterostructures were grown on single crystalline CdTe using MOCVD [56]. Results indicated that MOCVD HgTe contacts can exhibit ohmic behavior but needed careful control of growth conditions such as susceptor temperature, deposition time and partial pressures of Hg vapors. Furthermore HgTe could be doped n-type because of surface charges in CdTe. For the reasons mentioned above this process was really hard to control and reproduce. Chu et al. [57] used the close-space sublimation and chemical vapor deposition to deposit HgTe on polycrystalline CdTe solar cells. Due to the difference in partial pressures of Hg and Te the depositions had to be carried out at low temperatures ~300 °C. The deposition

rates were extremely slow that frequently led to shunting of the devices due to the long deposition times. Although efficiencies of 10.6% were achieved the lack of repeatability was detrimental to the use of HgTe as a back contact for CdTe cells.

3.7.3.2 Ni-P Back Contacts

At USF nickel phosphide in powder form was mixed with graphite paste and applied to CdTe for the formation of the back contact [58]. Ni_2P concentration, annealing temperatures and times were varied to study the effect on the cell performance. Conversion efficiencies of 12% were attained when concentration of 25%wt Ni_2P, annealing temperature and time of 250 °C and 90 minutes respectively were used. Lower annealing temperatures gave low Voc's and FF's due to inefficient carrier collection. At higher temperatures the contact became rectifying reducing the FF. Based on C-V measurements it was concluded that no phosphorus (P) diffuses into the device. Stress studies have been performed and the contact appeared to be stable with a slight decrease in Voc and FF.

3.7.3.3 Sb_2Te_3 Back Contacts

Antimony Telluride is a stable compound with a low band gap ~0.3eV, is p-type and has a very low resistivity of 10^{-4} Ω cm. The Sb_2Te_3 as back contact does not require a Te-rich surface therefore the etching of CdTe prior to contact formation is eliminated. N. Romeo et al. deposited Sb_2Te_3 by sputtering on CdTe

followed by sputtering of Mo as the final metal [59]. Substrate temperature during sputtering was optimized at 300 °C. At this temperature the Sb_2Te_3 layer exhibited the lowest resistivity (2×10^{-4} Ω cm) and solar cells with efficiencies of 15% were fabricated. Accelerated tests on solar cells with Sb_2Te_3/Mo as back contacts showed high stability with a slight increase in Voc (~20mV) and a slight decrease in FF (< 1%) [60]. The Mo/Sb_2Te_3 combination remains chemically stable while annealing due to high activation energy of the alloy formation [61].

CHAPTER 4

SUBSTRATE CONFIGURATION

4.1 Substrate Configuration
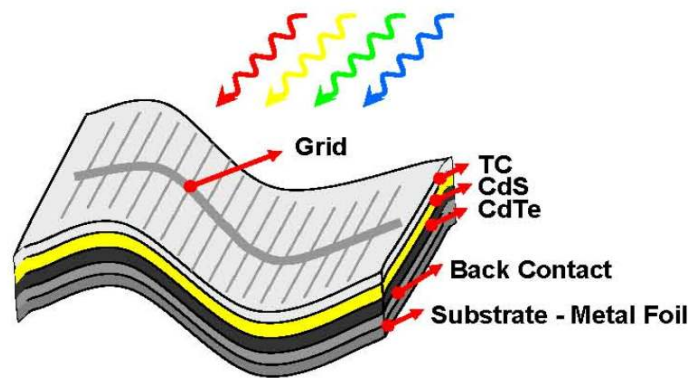
Figure 17. Substrate configuration

Figure 17 shows the substrate configuration of a CdTe solar cell. This configuration uses flexible metallic foils as the substrate. The main difference between the superstrate and the substrate configuration is the reversing of the deposition sequence. In the substrate configuration the back contact is deposited first, followed by the CdTe, CdS and front contact layers. Another difference is that the substrate material in this configuration doesn't have to be transparent.

4.2 Solar Cells on Flexible Substrates

CdTe has long been recognized as an ideal material for thin film photovoltaics because of its near-ideal bandgap and high absorption coefficient. It has been shown that CdTe has the highest stability under proton and electron irradiation [62] compared to other photovoltaic devices, which makes CdTe solar cells very promising for space applications.

In conventional solar cells, the CdTe is developed on the CdS window layer deposited on glass substrates. Most CdTe deposition techniques involve high processing temperatures, especially the Closed-Space Sublimation (CSS), in which CdTe is deposited at temperatures in excess of 500 °C. Devices on glass offer no weight advantage or shape adaptability for curved surfaces and due to high processing temperatures are prone to damages.

On the other hand fabricating solar cells on flexible substrates can overcome the above problems associated with glass substrates. Flexible solar cells are also lightweight making it easy to deploy in space. Furthermore being lightweight and flexible gives these solar cells much more possibilities for integration in buildings and maybe in such applications as solar cars, consumer electronics and portable source of power for emergencies.

Recent development of CdTe solar cells on flexible metallic substrates reported efficiencies from 3.5 to 7.8% [63, 64, 65].

4.2.1 CdTe/CdS by R.F. Sputtering on Mo Foils

The group at the University of Toledo developed Mo/CdTe/CdS/ITO, thin-film solar cells grown by rf magnetron sputtering [65]. Molybdenum was chosen as the substrate because its thermal expansion coefficient and work function are close to those of CdTe.

CdTe is naturally p-type and CdS is n-type when grown by sputtering therefore no intentional doping was used during the fabrication. The substrate temperature during deposition was kept at 250 °C. Following the CdTe/CdS deposition the cells received a vapor $CdCl_2$ treatment at 390 °C for 30 minutes. The last step involved the sputtering of ITO as the front electrode. Typical spectral quantum efficiency of a Mo substrate cell with a glass superstrate cell is shown in Figure 18.
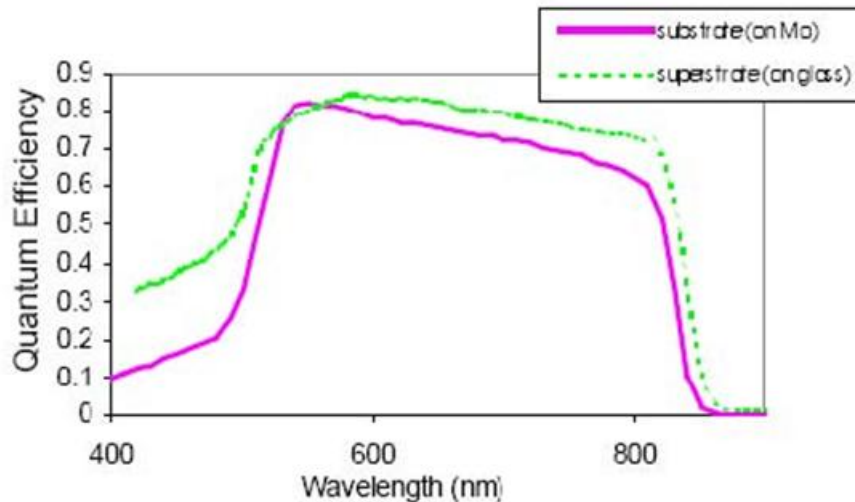
Figure 18. Comparison of the QE curves of the substrate and superstrate cells [65]

The substrate cell has a sharp turn-on of the QE near 530nm, an indication of little alloying between CdTe and CdS.

An efficiency of 7.8% was achieved when a nitrogen-doped ZnTe layer was deposited between the Mo and the CdTe. Figure 19 shows the complete substrate cell structure.
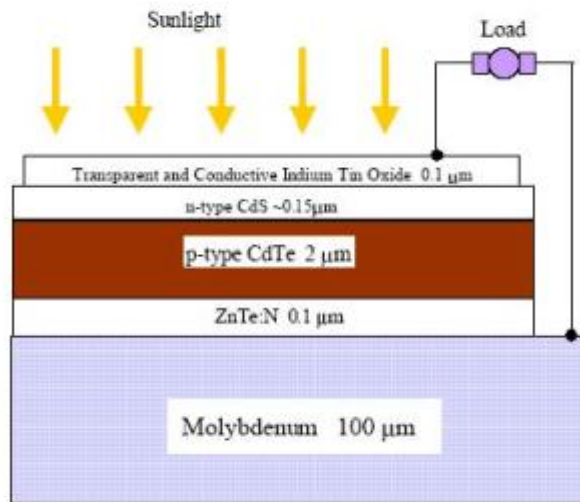
Figure 19. The structure of the substrate solar cell
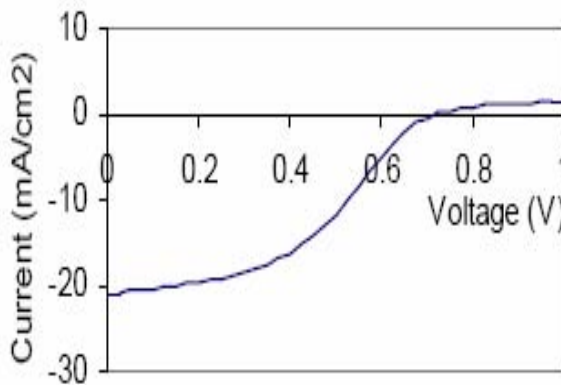
Figure 20. I-V curve of a typical substrate cell [65]

A typical current-voltage curve of the substrate cell is shown in Figure 20. The severe roll-over in the first quadrant indicates the presence of a blocking diode, most likely due to the interface between CdTe and Mo.

4.2.2 CdTe/CdS by Thermal Evaporation on Mo Foils

Cell efficiency of 5.3% was achieved by the groups at the universities of Kentucky and Texas at El Paso [66]. A schematic of the CdTe–CdS solar cell is shown in Figure 21.

| TCO (ITO, ZnO:Al) 500-600 nm |
| CdS 800 nm |
| CdTe 5μm |
| Cu $_{2-x}$ Te interlayer |
| Mo Substrate |
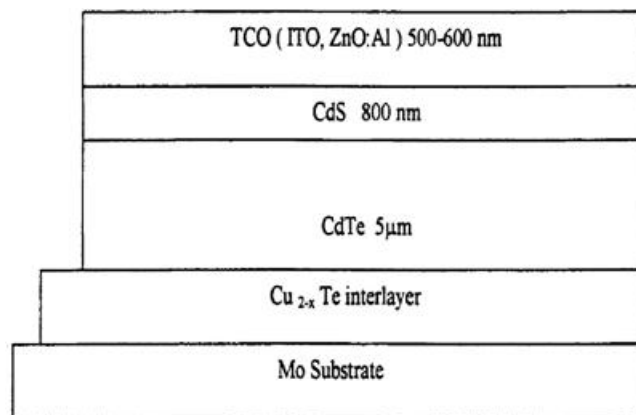
Figure 21. CdTe-CdS solar cell device configuration

Molybdenum metal foil of thickness 0.1 mm was used as the substrate. Contact resistance between CdTe and Mo was reduced when Cu and Te layers (~50 nm thick), were evaporated on the Mo foil creating a region of high carrier concentration allowing the carriers to tunnel through. CdTe was then deposited by thermal evaporation at a temperature of 220 °C and a typical thickness of

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5 µm. After CdTe deposition the films were dipped in CdCl$_2$ solution and annealed at temperatures between 300 °C and 500 °C for 1–4 hours.

CdS was deposited by chemical bath deposition, sputtering and thermal evaporation. Highest open circuit voltage was obtained when the CdS layer was deposited by thermal evaporation.

ITO, aluminum doped Zinc oxide (ZnO : Al) and a combination of ITO/ZnO : Al were sputtered on CdS as the front transparent contacts. With ITO as the front contact efficiencies greater than 5% have been achieved. Figure 22 shows the I-V curve of the highest efficient solar cell.
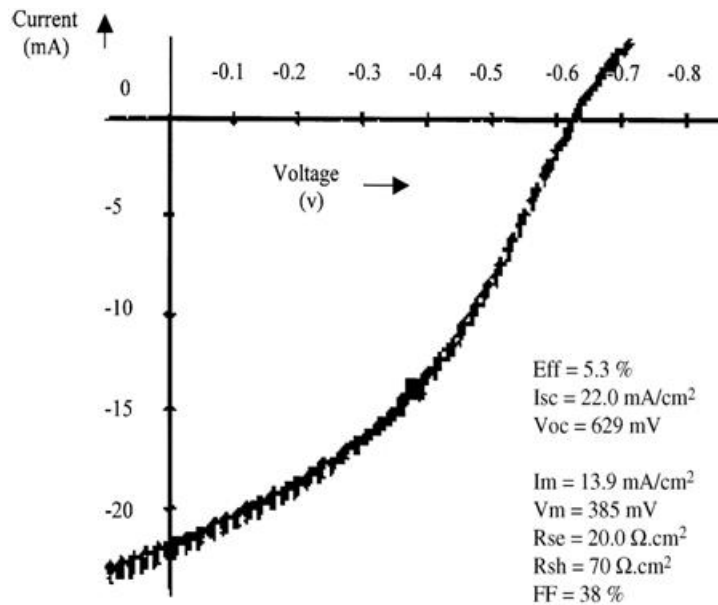
Figure 22. I-V curve of CdTe/CdS substrate cell on Mo foil [66]

The above I-V curve shows that limiting factors in the performance of the cell are the high series and the low shunt resistances. To improve the CdTe/CdS

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junction a series of annealing and $CdCl_2$ treatments were performed. The effects of the various treatments are shown in Table 2. For all devices, the first CdS layer is deposited at room temperature and then heat treated at 350 °C for 1 hour in air, before deposition of the second CdS layer. The thickness of the first CdS layer is 200 nm and of the second layer is 800 nm. When only one CdS layer is used, it is 1000 nm thick.

Table 2. V_{oc}'s of devices under different treatments

Device #	Device description	Voc (mV)
MB52-2	No CdTe–$CdCl_2$ treatment, CdTe annealed in N_2, no CdS–$CdCl_2$ treatment, single CdS layer	430
MB57-2	No CdTe–$CdCl_2$ treatment, CdTe annealed in air, no CdS–$CdCl_2$ treatment, single CdS layer	530
MB57-2	No CdTe–$CdCl_2$ treatment, CdTe anealed in air, no CdS–$CdCl_2$ treatment, two CdS layers	570
MB53-2	CdTe–$CdCl_2$ treatment, CdTe anealed in air, no CdS–$CdCl_2$ treatment, two CdS layers	640
NIB65-11	CdTe–$CdCl_2$ treatment, CdTe anealed in air, CdS–$CdCl_2$ treatment, two CdS layers	768

From Table 2, the device annealed in $CdCl_2$ and with two layers of CdS exhibited the highest V_{oc}.

4.2.3 CSS CdTe and CBD CdS Solar Cells on Mo Foils

The group at the University of Mexico used the close-spaced sublimation (CSS) and electro deposition (ED) methods to deposit CdTe on flexible substrates [67]. Scanning Electron Microscopy (SEM) analysis showed the CSS films to be superior to the ED films. CSS films had larger grain size and were closely packed compared to the ED films.

Figure 23 shows the schematic of the CdTe/CdS device in the substrate configuration. For the fabrication of solar cells Mo foil was used as the substrate and CdTe was deposited by the CSS technique. To obtain an ohmic contact a thin layer of Au/Pd (Gold/Palladium) alloy was used as an interlayer between Mo and CdTe. The thickness of the Au/Pd was 500 Å and was deposited by sputtering. CdTe films were prepared at a substrate and source temperatures of 570 and 670 °C respectively. The structures were then treated with a saturated solution of $CdCl_2$ and annealed at 400 °C in dry air followed by Br–methanol rinsing to clean the CdTe surface.
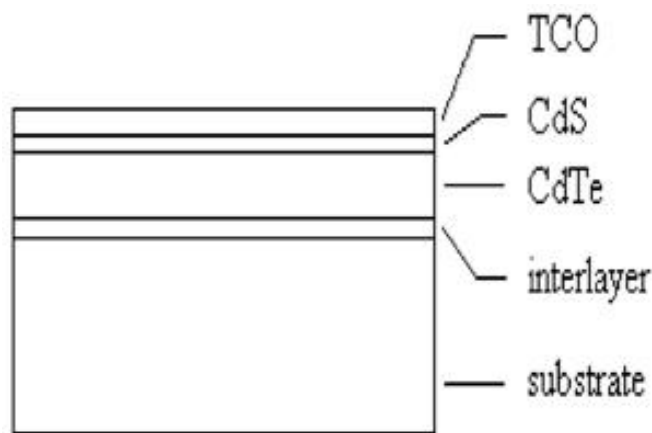
Figure 23. Schematic of the CdTe/CdS device in the substrate configuration

CdS 0.1 µm thick was deposited by CBD and the devices were air annealed at different temperatures. Maximum values for Voc and Jsc were obtained when devices were annealed at 400 °C for 30 minutes. Devices were completed by sputter depositing ITO as the top contacting material.

Figure 24 shows the I-V curve of the best solar cell with an efficiency of 3.5%.
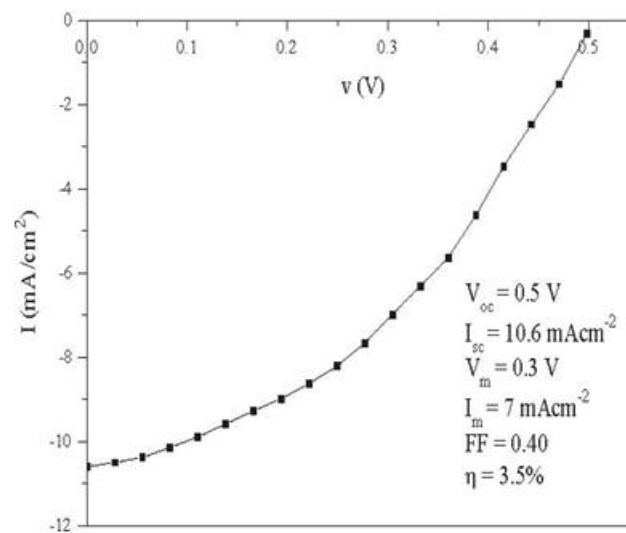
Figure 24. I-V-curve of a CdTe/CdS solar cell on Mo substrate [67]

CHAPTER 5

EXPERIMENTAL AND CHARACTERIZATION METHODS

5.1 Substrate Preparation

The substrate used was stainless steel foil of thickness 25 μm. Prior to processing the substrate was cleaned using a four-step process in an ultrasonic bath, starting with detergent, acetone, methanol and deionised water. Immediately after cleaning the substrate was dried using nitrogen and loaded into the sputtering chamber for the back contact deposition.

5.2 Device Fabrication

5.2.1 Sputtering

The back and front contacts were deposited by sputtering. The Mo back contact was deposited by radio frequency (RF) sputtering from a Mo (99.999% assay) target at room temperature. The sputter ambient was high purity argon gas with the pressure varying from 3 to 18mTorr. Typical Mo thickness was 0.5-1 μm.

The front contacts were SnO_2 and ITO deposited sequentially in a deposition system with two magnetron sputtering guns. The substrate holder was rotated during deposition to ensure film thickness uniformity. SnO_2 was sputtered

from 99.999% pure SnO_2 target in an argon environment at temperatures up to 250 °C. The thickness was varied from 100 to 2000 Å. Following the SnO_2 deposition, ITO was sputtered from (In_2O_3/SnO_2, 90/10 wt%) 99.995% pure target. The thickness was varied from 1000-3000 Å and the temperature was varied from room to 350 °C.

5.2.2 Close-Spaced Sublimation (CSS)

ZnTe, CdTe and CdS were deposited using the close-spaced sublimation method. This method offers several advantages compared to other methods, such as: a) high deposition rates making it attractive for manufacturing purposes; b) processing temperatures that result in CdTe/CdS interdiffusion which improves the quality of the junction; c) films with large grain size resulting in less grain boundaries with less recombination and d) process is under low vacuum conditions which eliminates the need for expensive high vacuum systems.

Two different system configurations were used for the CSS deposition. Figure 25 shows the setup for the first system. Halogen lamps were used to heat the graphite block containing the source and the graphite plate supporting the substrate. Thermocouples inserted in the graphite blocks were used to measure the temperatures which were controlled by Omega temperature controllers. The source temperature was varied from 600-650°C, while the substrate temperature was varied from 400-550°C. Spacing between the source and the substrate were kept constant throughout the experiments. Inert gas was used during the depositions and the pressure was varied from 1-30 torr.
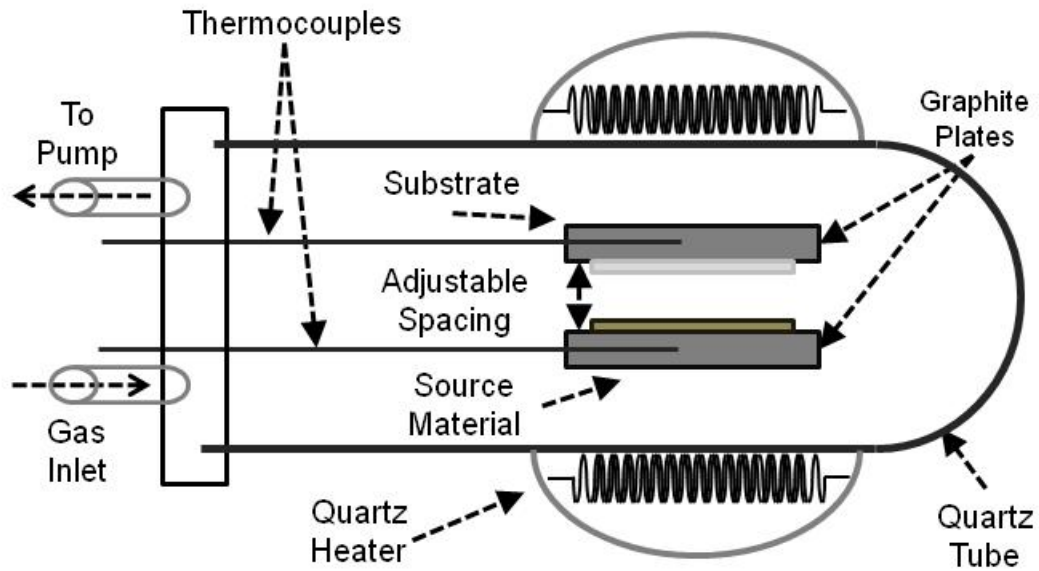
Figure 25. Schematic diagram of first CSS deposition chamber

A second system was also used that provided an in-situ sequential deposition of up to three different materials (ZnTe, CdTe and CdS), shown in Figure 26.
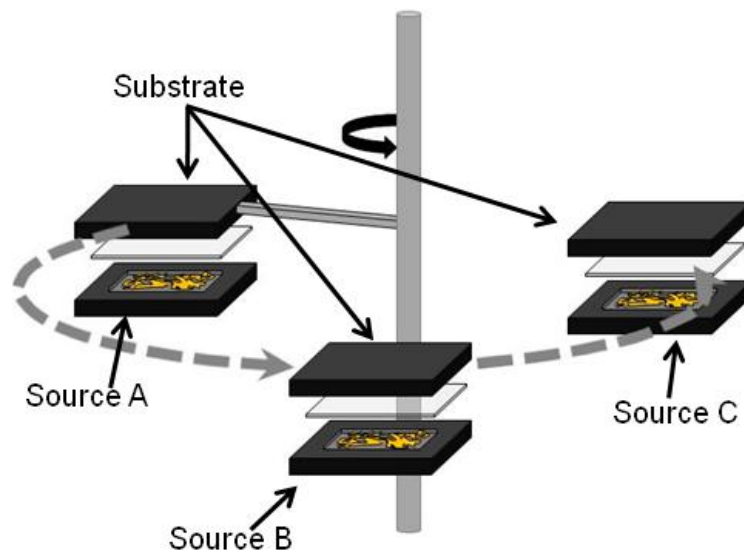
Figure 26. Second CSS system for an in-situ sequential deposition

Limitations of the second system, were, the fixed spacing between source and substrate and the substrate temperature being constant throughout the whole process.

5.2.3 Chemical Bath Deposition (CBD)

As mentioned in chapter 3, the highest efficiency CdTe solar cells were achieved when CdS was deposited using the CBD deposition method. Solar cells were fabricated in this way as an alternative to CdS being deposited by CSS. Figure 27 shows the setup for the CBD method.
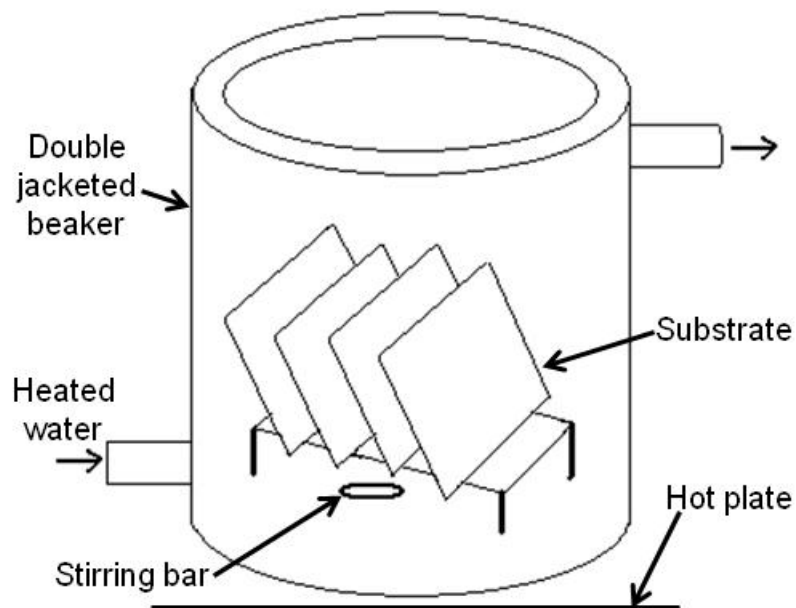
Figure 27. CBD schematic diagram

The substrates were immersed in hot de-ionized water whose temperature is maintained constant at 85°C during the deposition. A solution is prepared by

mixing specific amounts of CdAc, NH_4AC and NH_4OH and by adding thiourea at specific intervals during the deposition. The CdS thickness was varied between 200 and 1000Å depending on the time of the deposition.

5.3 Device Characterization

5.3.1 Material Characterization

To investigate the crystallographic and structural properties of films deposited on flexible substrates samples were measured with X-Ray diffraction(XRD) and scanning electron microscopy(SEM).

Grain sizes and uniformity of films were obtained from SEM micrographs of the films taken using Hitachi 800 SEM. Film thicknesses and growth rates were calculated from SEM cross-section images.

The crystallographic structures of the films were analyzed from XRD data collected using a Philips X-ray diffractometer.

5.3.2 Current-Voltage Measurement

Measurement of the I-V curve is the most common technique to characterize a solar cell. Current voltage characteristics were measured at room temperature in the dark and under A.M.1.5 illumination. The solar simulator was calibrated using a standard silicon solar cell. A four-point Kelvin-probe contact was used to minimize the effects of contact resistances. The power supply used was a Keithley 2410 Source Meter. I-V data was collected using a LabVIEW program that calculated FF and efficiency. Color I-V measurements were also

done using LED's. Spectral response measurements were carried out to determine the specific wavelength of the LED's. The intensity of the LED's was adjusted based on a standard silicon solar cell with a known QE response for a AM1.5 light intensity.

5.3.3 Spectral Response

Quantum efficiency (QE) is defined as the ratio of the number of collected electrons to the number of incident photons. QE is measured over a range of wavelengths that gives the spectral response of the solar cell. QE measurements are useful in determining the output current of the solar cell when exposed to the solar spectrum, as well as determining individual losses responsible for reducing the current.

An Oriel monochromator (model 74100) was used for the spectral response measurements. The light source was a GE400W/120V Quartz Line lamp. The light intensity was adjusted using a silicon reference solar cell calibrated at the U.S National Renewable Energy Laboratory (NREL). Data was collected using a LabVIEW program. The current response of the reference device is measured ($I_{Reference}$) and then the current response of the device is measured (I_{Device}). The QE of the device is obtained from:

$$QE_{Device} = QE_{Reference} \frac{I_{Device}}{I_{Reference}} \qquad (14)$$

The device current density was obtained by integrating the QE multiplied by the Am1.5 spectrum equivalent current.

5.3.4 Capacitance-Voltage Measurement

The capacitance-voltage (C-V) measurement is a useful technique to determine the doping concentration, doping profile and depletion width of the lightly doped side of a pn junction. Using the pn$^+$ approximation the C-V measurements give information about the CdTe layer. The capacitance measurement relies on the fact that the depletion width (W) of a reverse-biased p-n junction changes with applied voltage.

The depletion region of the pn junction can be approximated as a parallel plate capacitor, and the capacitance is given by

$$C = \varepsilon \, \frac{A}{D} \tag{15}$$

where ε is the permittivity, A is the area and D is the distance between the plates. In a p-n$^+$ junction the depletion width W is given by

$$W = \sqrt{\frac{2\varepsilon}{qN_A}(V_{bi} - V)} \tag{16}$$

where N_A is the carrier concentration on the p-side, Vbi is the built-in voltage and V is the applied voltage. Substituting equation 15 for D in equation 14 gives

$$C = \varepsilon \, \frac{A}{\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi}-V)}} \tag{17}$$

Rearranging equation 16 gives

$$\frac{A^2}{C^2} = \frac{2}{q\varepsilon N_A}(V_{bi} - V) \tag{18}$$

Plotting 1/C^2 Vs V should yield a straight line and the hole density p can be calculated.

C-V measurements were performed on selected samples using an HP4194 Gain Phase Analyzer. An ac voltage of 20 mV was applied and the dc bias was varied from -2 V to 0.5 V. Prior to a C-V measurement, capacitance Vs frequency measurement (C-F) was performed so a frequency can be chosen so that the capacitance is insensitive to frequency throughout the dc bias. The selected frequency was usually in the order of 100 KHz . Data were collected with a LabVIEW program.

CHAPTER 6

RESULTS AND DISCUSSION

The main objective of this study was to transform the process of fabricating CdTe solar cells from the glass-superstrate configuration to a flexible foil substrate configuration with the potential for high throughput roll-to-roll manufacturing.

6.1 Flexible Substrate

The substitution of the well established soda-lime-glass substrate by a flexible alternative without drawbacks and without the generation of new obstacles is not as straight-forward.

Therefore some requirements for the selection of the substrate will have to be established. A list of these requirements is:

- film adhesion; meaning a coefficient of thermal expansion must be close to that of the deposited layers

- thermal stability; to allow the use of high temperatures

- reasonable cost; similar or lower than glass

- suitable for roll-to-roll manufacturing

There is a wide selection of metal foils. Molybdenum, titanium, tungsten, stainless steel and unalloyed steel foils. Unalloyed steel foil is the cheapest one but was found to be detrimental to solar cells due to excessive diffusion of iron (Fe) in the layers of the cell [68]. Titanium and molybdenum foils have also been used, but these foils are expensive [63, 64, 65, 69]. Table 3 lists the prices for some of the foils.

Table 3. Pricing for different foils

Foils	Price ($/square inch)
Molybdenum	1.47
Titanium	1.38
Tungsten	4.27
SS 430	0.10
SS 316	0.45

Stainless steel 316 (SS) foil was chosen as the substrate material based on its low cost, availability, mechanical and thermal properties. The cost of this material is almost the same to that of a glass substrate, it is readily available in large quantities in roll form, and it can withstand high processing temperatures associated with the solar cell fabrication. Due to stressed devices after the deposition of the CdTe layer, SS 316 was replaced with SS 430 (see Section 6.2) that has a better matched thermal expansion coefficient to the deposited layers (see Table 4).

6.2 Back Metallic Contact

Sputtered Molybdenum (Mo) was chosen as the metallic back electrode. It has been shown that Mo resulted in the formation of effective back contacts on CdTe and provides a good thermal match to CdTe [45]. Table 4 lists the thermal expansion coefficients (CTE) of the different foil substrates and deposited layers.

Table 4. CTE's for foil substrates and deposited layers

Material	SS 316	SS 430	Mo	ZnTe	CdTe	CdS
CTE $(K^{-1} \times 10^{-6})$	16.0	10.5	4.8	10.0	5.9	4.5(7.0)

To minimize the back contact contribution to the series resistance a low resistive film is desired. Another important parameter is the ability of the back contact to adhere well to the substrate. The adhesion of Mo films to glass substrates and the sheet resistivity are dependent on the sputter deposition conditions [70, 71, 72].

In order to investigate the adhesion and stress of Mo films on SS, a series of films have been prepared under low and high pressure and low and high deposition rates. All Mo films were deposited at room temperature and had the same thickness. Table 5 shows the characteristics of films prepared under different conditions.

It was observed that films deposited at high power of 350W and low argon pressure of 4.5 mTorr developed compressive stresses. The thin foil deposited

under these parameters showed convex bending. On the other hand, films deposited at low power of 100W and high argon pressure of 8 mTorr resulted in tensile stresses showing concave bending.

Table 5. Study of Mo films deposited at different conditions

Sample #	11-28-1	11-29-2	11-30-1
Press. (mTorr)	4.5	7.9	10
Dep.Rate (Å/s)	10.2	10.8	10.8
ρ (Ω-cm)	1.74×10^{-4}	1.70×10^{-3}	1.50×10^{-3}
Sample #	12-5-1	12-5-2	12-4-1
Press. (mTorr)	4.5	7.9	10
Dep.Rate (Å/s)	6.2	6.2	6.4
ρ (Ω-cm)	7.80×10^{-4}	7.36×10^{-3}	9.06×10^{-3}
Sample #	11-21-1	11-29-1	12-1-1
Press. (mTorr)	4.5	7.9	10
Dep.Rate (Å/s)	2.8	2.6	2.2
ρ (Ω-cm)	1.14×10^{-3}	1.35×10^{-2}	2.28×10^{-2}

It can be seen from Table 5 that the resistivity decreases as the deposition rate increases and the pressure decreases which agrees with the work of others [71, 72].

Depositions were carried out using a combination of high power/low pressure and low power/high pressure to obtain a stress free (flat) foil. This is a well known approach used for CIGS solar cells.
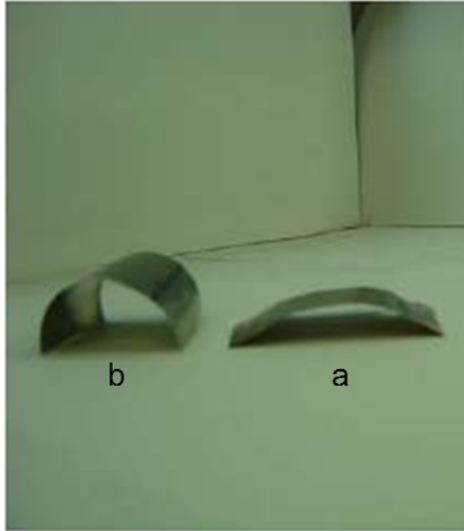
Figure 28. 316 SS coated with Mo/ZnTe/CdTe/CdS at different substrate deposition temperature; a) 450°C and b) 520°C.

Figure 28 shows a photograph of two SS substrates coated with Mo/ZnTe/CdTe/CdS. The substrate temperature during the deposition of the semiconductor layers was kept at 450°C for foil a, and 520°C for foil b. The figure shows the varying degree of stress in the substrates suggesting a correlation between the substrate temperature and the degree of curvature.

The effect of temperature on the stress of the films can be attributed to the difference in the thermal expansion coefficient of the various films and the substrate foil. Mismatch minimization of the substrate's CTE reduces thermal stress and promotes adhesion. This lead to the decision to look for an alternative SS substrate as the CTE of the 316 SS was $16 \times 10^{-6}K^{-1}$, which is considerably higher than the CTE of the other films (see Table 4).

SS 430 was chosen as the new SS substrate as its CTE is $10 \times 10^{-6}K^{-1}$ which is closer to the CTE's of the other layers to be used.

6.3 Growth Study of CdTe Layers

The growth of CdTe films deposited on Mo coated flexible substrates has been investigated in order to study their structural properties for solar cell applications.

Several CdTe films were deposited by CSS at different source and substrate temperatures. The pressure and the spacing between source and substrate were kept the same for all the depositions. Table 6 shows a summary of the conditions used during the deposition of CdTe on the SS/Mo substrates. Cross-sections from SEM images were used to measure thicknesses and calculate the growth rate of all films.

Table 6. Conditions used for the CdTe deposition on SS/Mo

Sample #	Tsource C°	Tsubstrate C°	Growth Rate µm/min
11-3-2A	600	450	2.2
11-4-1B	630	460	7.5
11-17-1A	650	460	18
11-3-2B	600	500	1.54
11-3-1A	630	500	6.35
11-17-1B	650	500	16.24
11-4-1A	600	550	0.93
11-3-1B	630	550	5
11-18-1A	650	550	13.5

The growth rate was found to increase rapidly as the source temperature is increased while keeping the substrate temperature constant due to an increased sublimation rate as also reported by S.N Alamri [73]. The growth rates were in the 1 to 18μm/min range. These high deposition rates are important for a high throughput process.

For a constant source temperature as the substrate temperature increased the growth rate decreased which can be attributed to re-evaporation of CdTe, which agrees with the work of others [74].

In order to study changes in texture all samples were measured using X-Ray Diffraction. Normalized patterns for a source temperature of 600°C are shown in Figure 29.
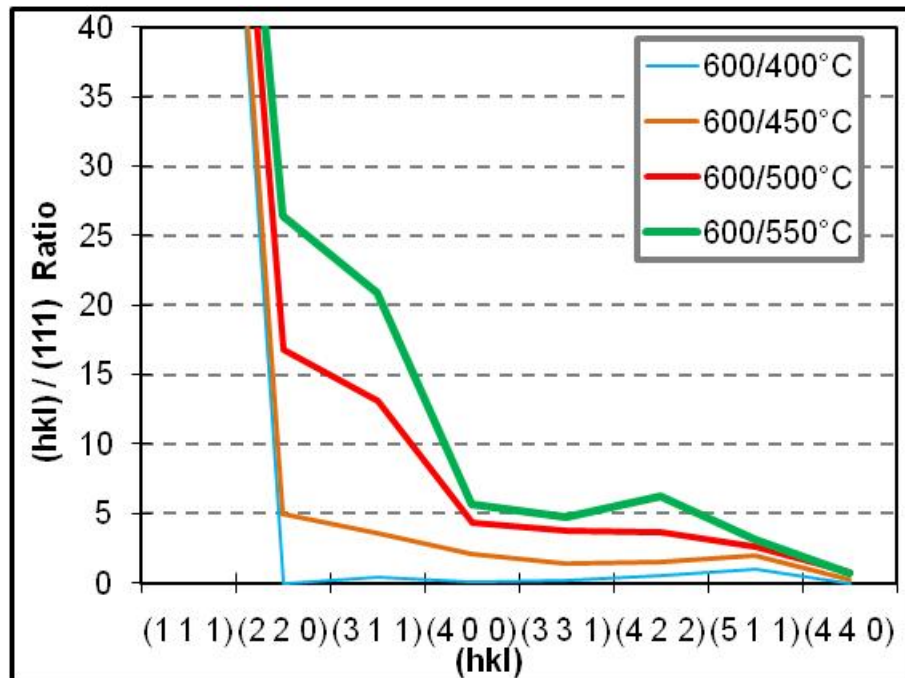
Figure 29. Normalized XRD-patterns of CdTe films deposited at the same source temperature at different substrate temperatures

The XRD patterns show the characteristic peaks of the cubic structure. It is clear from figure 29 that the substrate temperature influences the grain growth and preferred orientation. For low substrate temperatures a strong texture along the (1 1 1) direction is observed. As the substrate temperature increases there is a shift from the (1 1 1) orientation to a mix of (1 1 1), (2 2 0) and (3 1 1) orientations, which agree with the findings of G.P.Hernandez [75]. Preferential orientation of CdTe films results in columnar structures that improve the performance of the solar cells [76].

SEM micrographs in Figure 30 show that films deposited at a substrate temperature of 450 °C and different growth rates appear to be uniform with an average grain size of ~3μm.
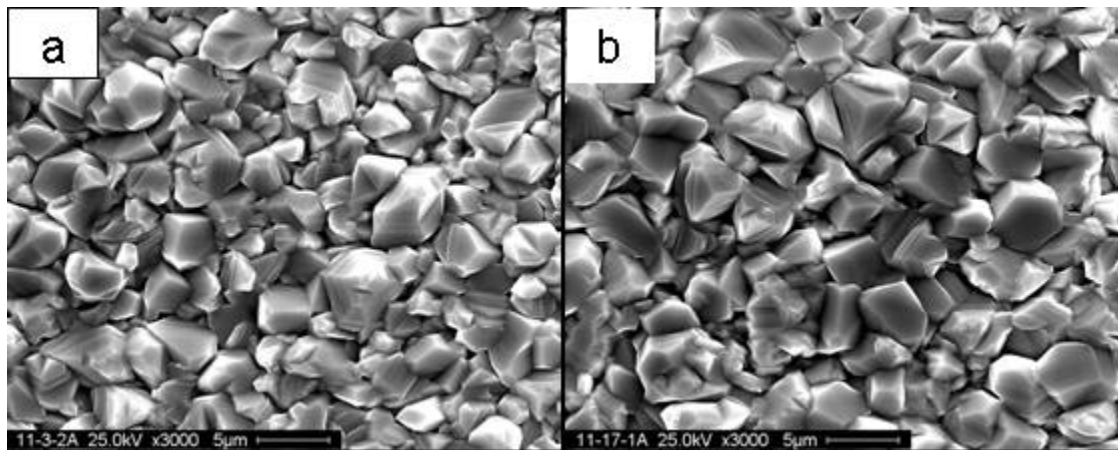
Figure 30. SEM pictures of CdTe films deposited at a substrate temperature of 450°C and different source temperatures. Growth rates; a) 2.2 μm/min, b)18 μm/min

Films deposited at higher substrate temperatures (Figure 31) were inhomogeneous with grain size between 2-6 μm. Despite the non-uniformities all

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samples appear densely packed and pinhole-free a requirement for thin film solar cells.
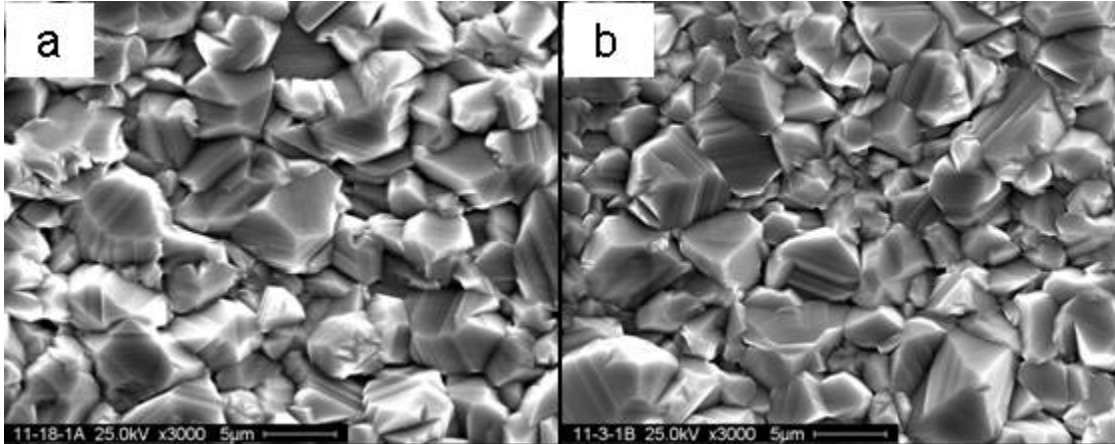
Figure 31. SEM pictures of CdTe films deposited at a substrate temperature of 550°C and different source temperatures. Growth rates; a) 13.5 μm/min, b) 5 μm/min

Grain boundaries in CdTe films act as recombination centers and may also act as barriers to carrier transport [77]. Maximizing the grain size reduces the impact of grain boundaries therefore enhancing the device performance. It is clear from the above described results that CSS-CdTe films can be tailored to meet these requirements.

6.4 Back Contacts/Interlayers

6.4.1 Zinc Telluride (ZnTe)

Zinc Telluride (ZnTe), a p-type semiconductor with a direct bandgap of 2.24eV has been chosen as an interlayer. The formation of ohmic contacts to ZnTe is easier due to its lower work function and the ability to dope it highly p-

type. Another quality of ZnTe is the low valence band discontinuity of -0.14eV with CdTe [78], so it does not impede the flow of holes from CdTe to ZnTe towards the metallic contact. Figure 32 shows the schematic of the CdTe/ZnTe band diagram.
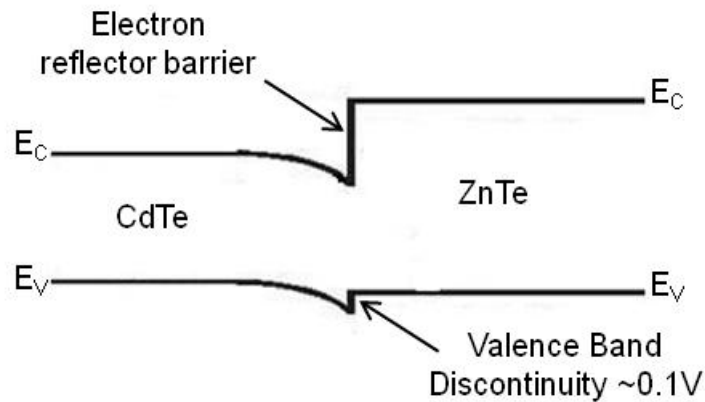
Figure 32. Band diagram of CdTe/ZnTe interface

The conduction-band offset between CdTe and ZnTe can serve as what is called an "electron reflector" barrier. It has been suggested that this electron barrier can be used as a strategy to improve the Voc of the CdTe solar cells by reducing the number of electrons recombining at the back surface [79].

The bulk lattice constant of ZnTe is 6.05 Å, which gives a 6.6 % lattice mismatch to CdTe which has a lattice constant of 6.48 Å. ZnTe films with thickness less than 20 Å, grown on CdTe were found to be highly stressed. ZnTe films with thickness higher than 300 Å, were shown to be completely relaxed [80].

ZnTe is a stable material at high temperatures and it has been shown to be effective as an interlayer to form low resistance back contact in the superstrate configuration [81]. It can be deposited by CSS-the same process used for the deposition of CdTe and CdS.

Based on the above information ZnTe was the first choice to be used as an interlayer between CdTe and the metal contact in the substrate solar cells.

6.4.1.1 Growth Study of ZnTe Films

Close-spaced sublimation (CSS) is a relatively inexpensive technique for deposition of polycrystalline thin films due to low vacuum operating pressures (1-30 Torr) and high deposition rates are easily obtained making it very attractive for manufacturing purposes.

The performance of CdTe solar cells depends on the structure and morphology of the polycrystalline film. Pinholes that cause shunting and grain boundaries that can be recombination pathways affect the performance of solar cells.

Therefore in order to study the structural and adhesion properties of ZnTe, a series of ZnTe films deposited by CSS on molybdenum coated SS foils were fabricated. The effect of the substrate-source temperature and the growth rate on the structure and surface morphology of the films were analyzed.

Figure 33 show the SEM images of four different ZnTe films deposited on SS/Mo. The source temperature was kept constant, and the films a, b, c, d were deposited at substrate temperatures of 450/500/520 and 550°C respectively.

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Films deposited at lower temperatures appear to be more uniform, have small grain size and are more densely packed. As the substrate temperature increases the grain size becomes larger and less uniform. The sample deposited at 550° exhibits incomplete coverage. At high substrate temperatures the surface mobility of the depositing material increases leading to less nucleation sites, larger grains resulting in incomplete coverage for films with small thickness.
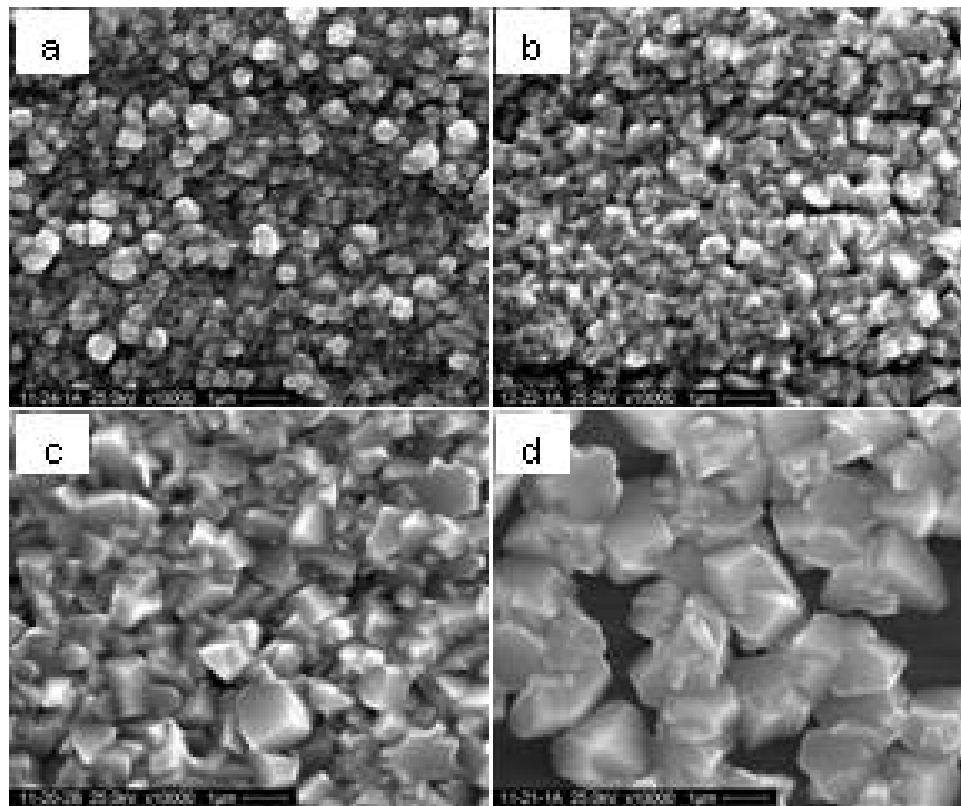
Figure 33. SEM images of ZnTe films prepared at different substrate temperatures of (a) 450°C, (b) 500°C, (c) 520°C and (d) 550°C. The source temperature was constant at 630°C

The grain size of ZnTe films at different source and substrate temperatures are shown in Table 7.

Table 7. Grain size of ZnTe films

Substrate Temp. (°C)	Source Temp. (°C)		
	610	630	Grain Size (µm)
450	0.5	0.6-0.8	
500	0.6-0.8	0.7-1.0	
550	1.0-1.3	1.8-2.0	

XRD analysis of ZnTe samples deposited at substrate temperatures between 400 and 500°C and a source temperature of 600°C are shown in Figure 34. The film deposited at the lowest temperature has a stronger preferred orientation along the (1 1 1) direction. As the substrate temperature increases there is shift from the (1 1 1) orientation to a mix (1 1 1), (2 2 0), and (3 1 1) orientations. This effect of substrate temperature was also observed in films deposited at different source temperatures. Table 8 lists the various diffraction peaks identified in the XRD spectra of Figure 34. All the peaks belong to the cubic ZnTe structure.

Table 8. 2θ values and (h k l) directions for the ZnTe films of Figure 34

Reference ZnTe file		ZnTe films deposited at different substrate temperatures		
2θ	(h k l)	400°C	450°C	500°C
25.259	1 1 1	25.267	25.287	25.267
29.248	2 0 0	29.233	29.234	29.251
41.806	2 2 0	41.809	41.839	41.807
49.498	3 1 1	---	49.432	49.435
51.847	2 2 2	49.430	---	---
60.634	4 0 0	60.602	60.616	60.608
66.747	3 3 1	66.738	66.722	66.743
68.739	4 2 0	---	---	68.644
76.401	4 2 2	76.269	76.282	76.353
81.969	5 1 1	---	---	---
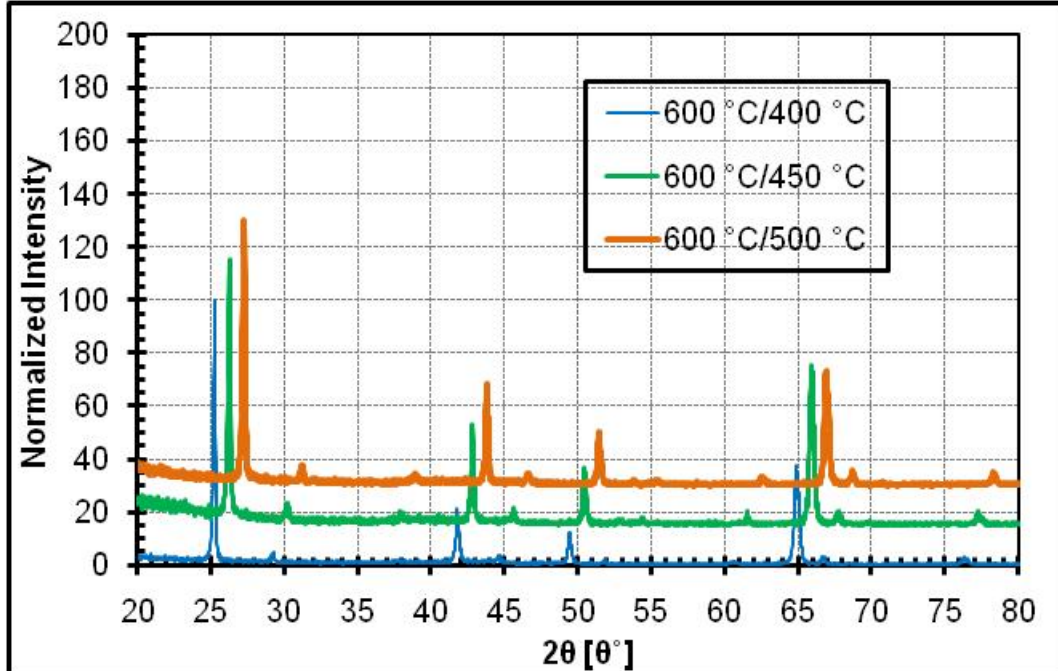
Figure 34. Normalized XRD-patterns of ZnTe films deposited at the same source temperature but with different substrate temperatures

Figure 35 shows the cross-section of a ZnTe film deposited on stainless steel coated with Mo. From the SEM image it appears that the film is uniform and the grains extend through the entire film thickness.
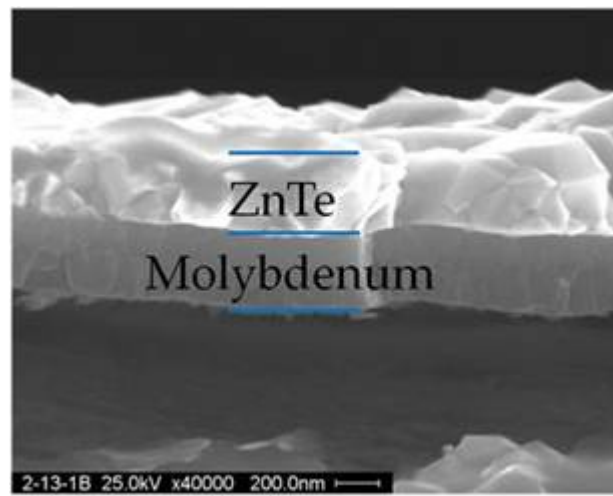
Figure 35. Cross-section SEM image of SS/Mo/ZnTe film deposited at a source and substrate temperature of 600 and 500°C respectively

6.4.1.2 Solar Cells with ZnTe as an Interlayer/Back Contact

Based on the growth study of the ZnTe layer conditions were chosen that provided films with complete coverage and the most uniformity (see Figure 35).

Figure 36 gives the variation of V_{oc}, J_{sc} and FF as a function of the ZnTe thickness. It is evident that the device with no interlayer has the lowest V_{oc}. The V_{oc} increases as the ZnTe thickness increases and decreases slightly at the highest ZnTe thickness. The highest V_{oc} and J_{sc} are obtained for a ZnTe thickness of 1000 Å. J_{sc} is lowest for the largest ZnTe thickness.
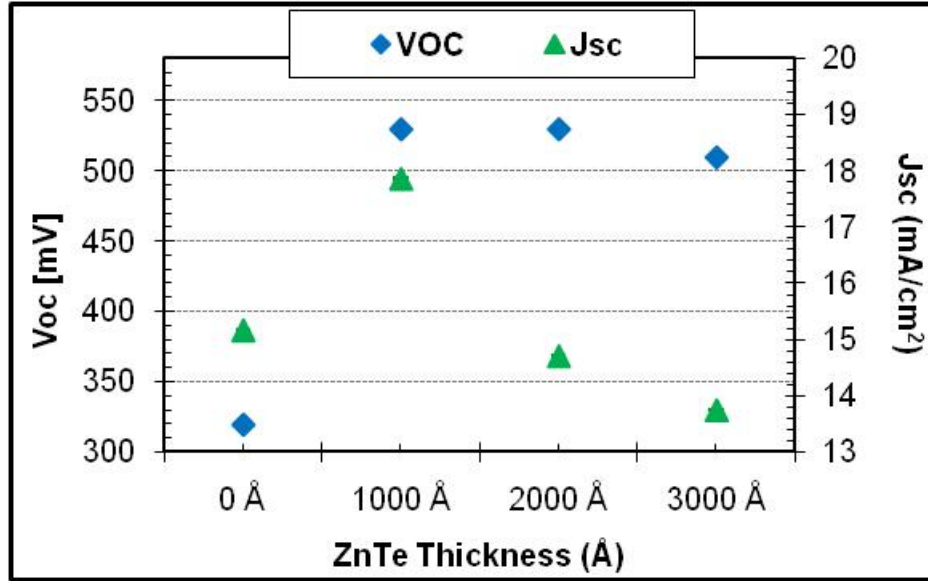
Figure 36. Effect of ZnTe thickness on cell performance

The decrease in the J_{sc} is due to the increase in resistance as a result of the increase in ZnTe thickness. In order to measure the resistivity of the ZnTe layers, films with the same thickness as the ones in Figure 36 were deposited on glass. The four-point probe technique was used but the sheet resistance was too high to measure. This was expected because the ZnTe films used were undoped. J-V characteristics for the above cells shown in Figure 37 demonstrate the increase in series resistance.

Another important observation from the J-V data is the severe roll-over in the first quadrant. This behavior has been seen in thin-film polycrystalline solar cells and is an indication of a back barrier [82]. When a metal contact is applied on a semiconductor, this often results in the formation of a Schottky barrier.
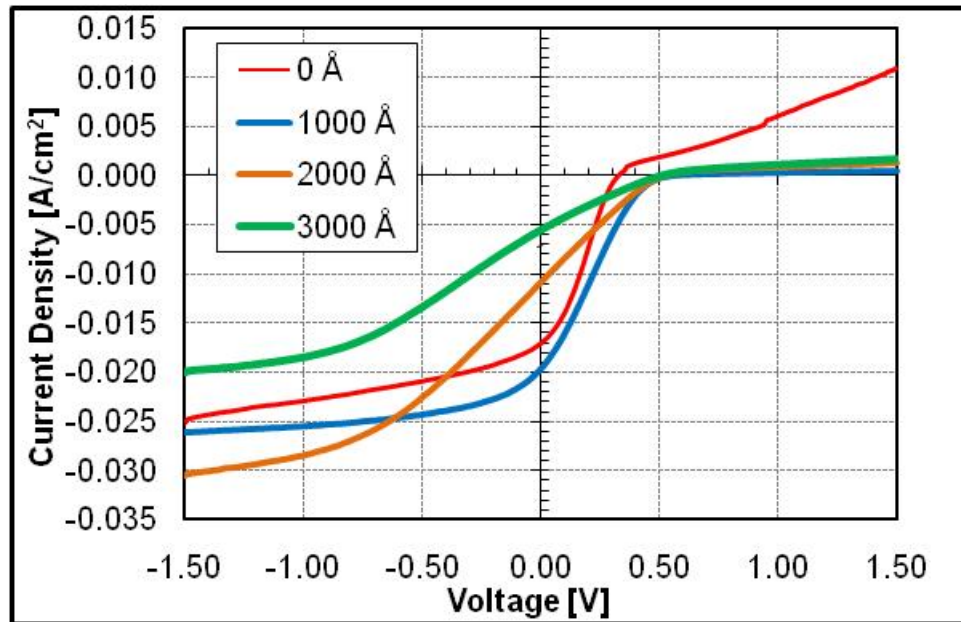
Figure 37. Effect of ZnTe thickness on J-V characteristics

The barrier can be modeled by a series connection of two diodes with opposite polarities. The CdS/CdTe main junction and the CdTe/metal-contact back diode. Figure 38 shows the schematic of the two-diode model. When a forward bias is applied the voltage is divided between the main and the back contact junction. Under illumination the voltage across the main junction saturates at V_{oc}. Further increase in the applied voltage will appear at the back diode which is reverse biased limiting the current.

The presence of a back contact barrier in a solar cell can significantly affect the current-voltage characteristics primarily by impeding hole transport. Analytic simulations with back barrier heights exceeding 0.5 eV resulted in significant FF and V_{oc} reduction [83, 84]. Figure 39 show the effect of back barrier on V_{oc}. For barrier heights less than 0.35 eV there is no significant change

in V_{oc}. When the barrier height is heigher than 0.35eV V_{oc} starts decreasing with a significant drop when the barrier height exceeds 0.50eV.
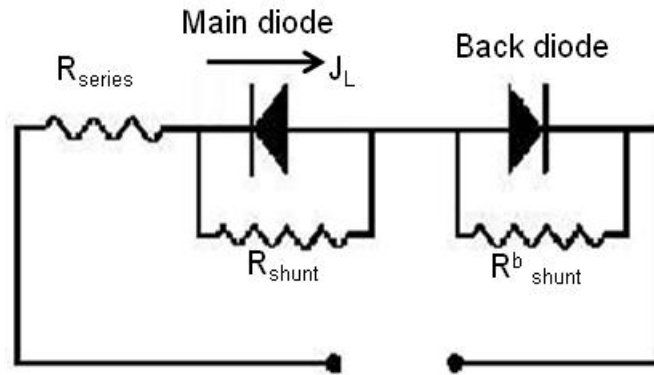
Figure 38. A two-diode equivalent circuit model
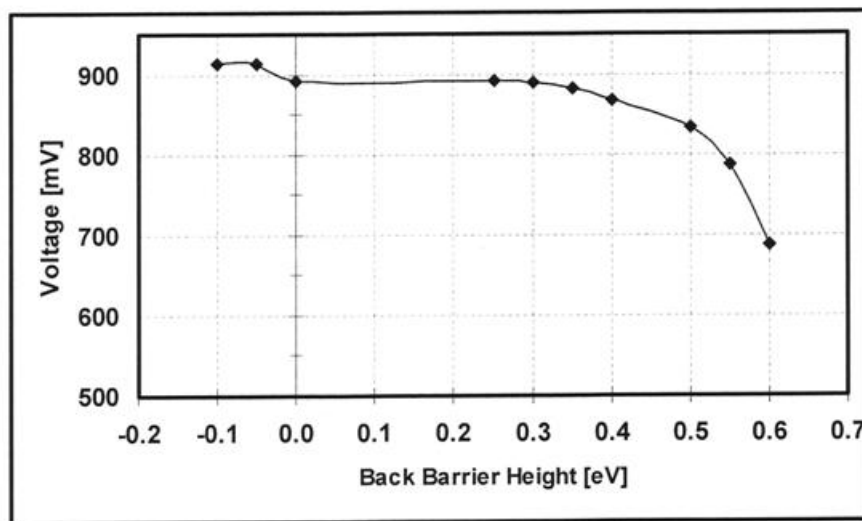
Figure 39. The effect of back barrier on Voc

The formation of ohmic contact to ZnTe should be easier compared to CdTe due to its lower work function. Table 9 lists electronic properties of CdTe,

ZnTe and Mo. From Table 9 the difference in the work function between ZnTe and Mo is smaller than that of CdTe and Mo and therefore an improvement in the back contact is expected.

Table 9. Electronic properties of CdTe, ZnTe and Mo

	CdTe	ZnTe	Mo
Band gap (eV)	1.45	2.24	
Electron Affinity (eV)	4.50	3.53	
Work Function (eV)	~5.70	~5.10	4.60

Based on the results (see Figure37) the addition of ZnTe between the Mo and the CdTe resulted in an increase of 200 mV for the V_{oc}. There was no significant improvement in the back contact with the use of the ZnTe layer. The back barrier due to the ZnTe/Mo interface might still be high enough causing the low values for Voc and FF. Another explanation might be the formation of dipole layers due to charge exchange at the ZnTe/CdTe interface. This will create an increase in the valence band discontinuity between the two materials creating a barrier. The formation of this barrier might be the one causing the roll-over seen in the J-V data and not a back barrier in the back contact.

The ZnTe used in this study was undoped resulting in films with high resistivity and solar cells exhibiting a large back contact barrier thus limiting the

performance of the devices. A typical approach to overcome this obstacle is to heavily dope the material –in this case ZnTe- as it was explained in section 3.7.

It was shown that ZnTe can be highly doped p-type with nitrogen [85], antimony [86] or Cu [87], that could improve the back contact formation and therefore enhance the performance of the solar cell.

6.4.2 Copper (Cu) as a Back Contact

In the superstrate configuration copper is commonly used in the back contact to improve the device performance of the solar cell. A small amount of Cu is added to effectively p^+-dope the CdTe surface to allow the formation of better ohmic contact.

From the results obtained in the previous section it was decided to add Cu prior to the ZnTe deposition as a way of doping ZnTe to improve the back contact formation. In this study Cu was deposited by sputtering and the thickness was varied from 40 to 100 Å based on previous studies that found a Cu thickness of around 100 Å to be optimum for high performance CdS/CdTe solar cells [87].

Figure 40 shows the light J-V and SR characteristics for the CdTe solar cells with different Cu thicknesses. The addition of Cu improved the back contact as the roll-over in the first quadrant of the J-V data was reduced. From the third quadrant shunting is observed for all the devices and the largest thickness of Cu resulted in significant reduction in V_{oc} and J_{sc}. These results underscore the impact of Cu on CdTe solar cells (clearly demonstrated in superstrate cells) and suggest that it may be possible to optimize Cu-based contacts in substrate cells,

although it appears that presently the substrate cells degrade substantially (see SR data below) with the addition of Cu.

From the SR data in Figure 40 all devices suffer significant collection losses throughout the whole spectrum. Similar behavior was observed previously for excessive amounts of Cu in the CdS layer [88].
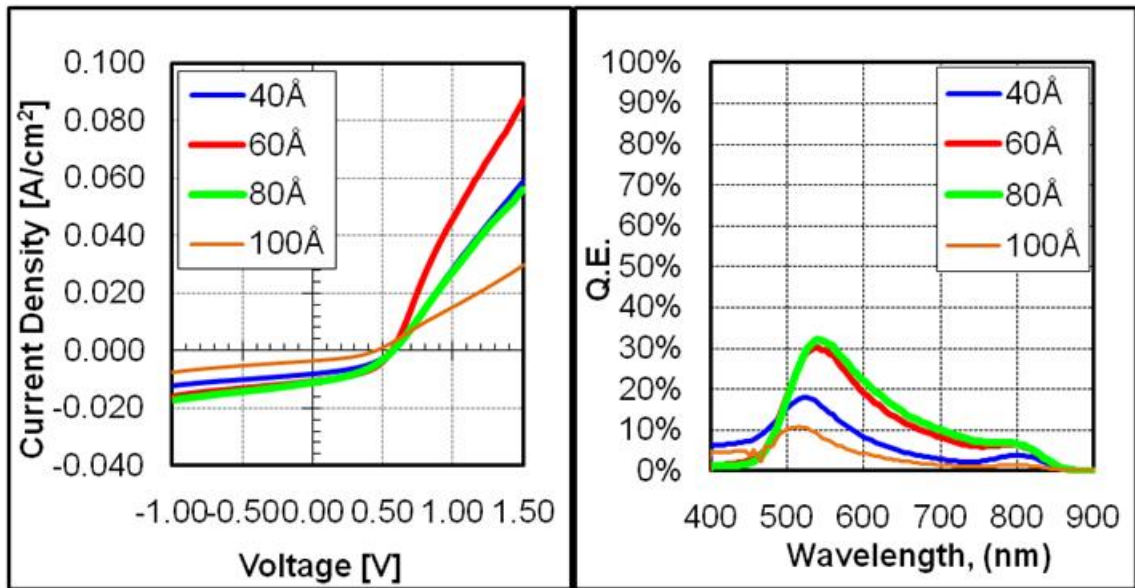
Figure 40. J-V and SR curves for different Cu thicknesses

Cu diffusion in the device from the back contact during high processing temperatures proved to be detrimental in the performance of the solar cells. In order to better control and limit the amount of free Cu diffusing into the solar cell, copper telluride was exploited as a back contact candidate.

6.4.3 Copper Telluride (Cu$_2$Te) as a Back Contact

Copper telluride has been effectively used as a back contact in the superstrate configuration. For Cu$_2$Te contacted CdTe solar cells the thickness of Cu$_2$Te is a critical parameter because it determines the amount of free Cu diffusing into the solar cell [45,46]. The thickness was varied from 5 to 100 Å, and the films were deposited by sputtering at 250 °C. From previous studies at the University of South Florida, nearly stoichiometric films were deposited at this temperature. Figure 41 shows the J-V characteristics for the Cu$_2$Te back contacted solar cells.
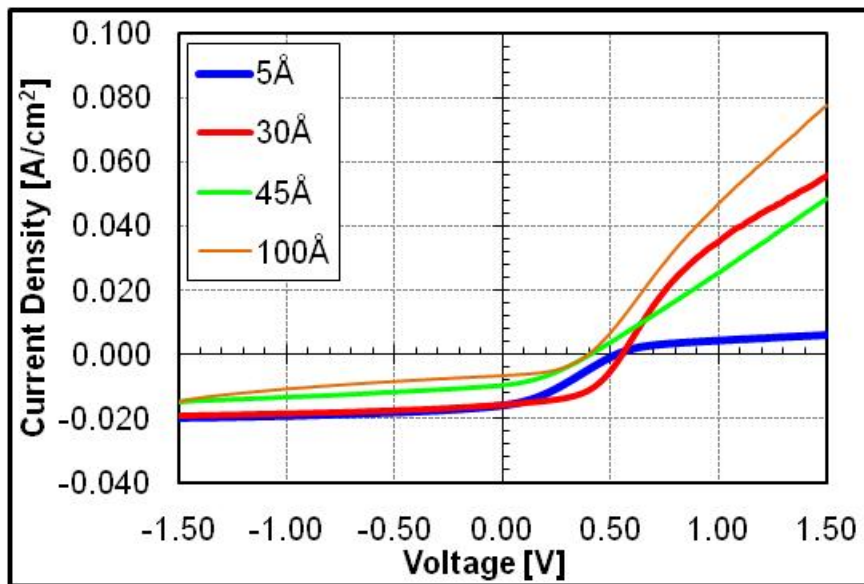
Figure 41. Effect of Cu$_2$Te thickness on J-V characteristics

From the J-V data as the Cu$_2$Te thickness increases there is less roll-over suggesting an improvement in the back contact but Jsc decreases. The device with the smallest thickness of Cu$_2$Te suffers from a strong roll-over. In the third

quadrant under reverse bias the cells with the larger Cu_2Te thickness exhibit lower shunt resistance that can be the result of shunting paths due to excess free Cu in the solar cell.

The corresponding spectral response data for the above cells are shown in Figure 42. Strongly reduced carrier lifetimes and depletion widths with increasing Cu_2Te can have a significant effect on carrier collection. Cu can form both deep donors and acceptors [89]. Cu that forms deep donors can act as recombination centers that lower lifetimes causing decrease in carrier collection. The cell with the smallest amount of Cu_2Te results in the highest SR.
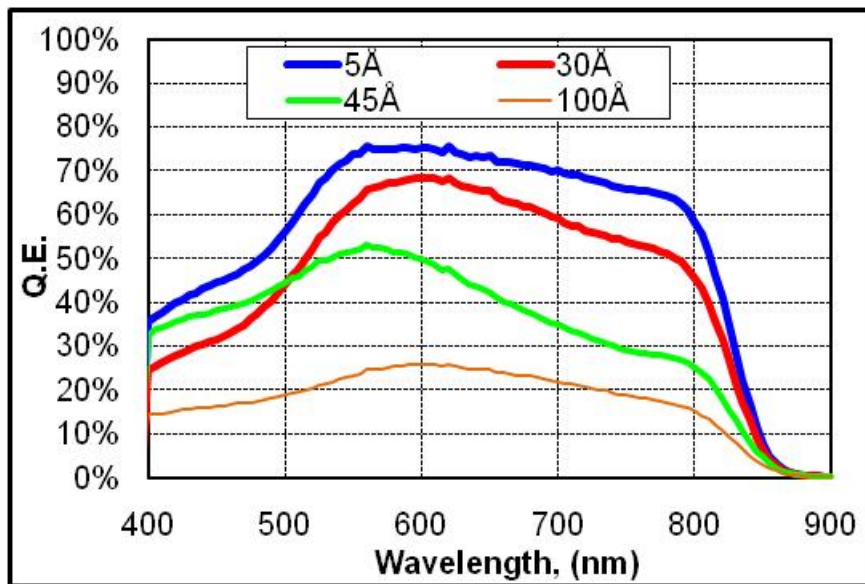
Figure 42. Spectral response of solar cells with Cu_2Te as the back contact

Device characteristics are shown in Table 10. It is clear that the amount of Cu_2Te influences the V_{oc} and the J_{sc} of the solar cells. The sample with 30 Å of Cu_2Te has the best performance. The samples with the two largest thicknesses

show a significant drop in V_{oc} and J_{sc}. Although to a certain extent some roll-over is present in all cells it is more severe for the cell with the smallest Cu_2Te thickness. The FF shows some improvement as the thickness of Cu_2Te is increased.

Table 10. Effect of Cu_2Te thickness on cell performance

Cu_2Te Thickness (Å)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
5	520	17.77	32
30	550	14.81	39
45	400	10.89	36
100	390	5.71	39

As mentioned earlier a high back contact barrier can cause reduction on V_{oc}. From the J-V data (see Figure 41) one would expect an increase in the V_{oc} with the apparent decrease in the roll-over. It is clear from Table 10 that V_{oc} still remained at low values. Recombination in the CdS/CdTe junction can also limit the V_{oc} of the device.

Figure 43 shows the dark J-V characteristics for the devices with different Cu_2Te thicknesses. The reverse saturation current decreases with decrease in Cu_2Te thickness indicating better junction quality that explains the increase in V_{oc} from Table 10. The lowest saturation current is observed for the device with 30 Å of Cu_2Te which is the device with the highest V_{oc}.
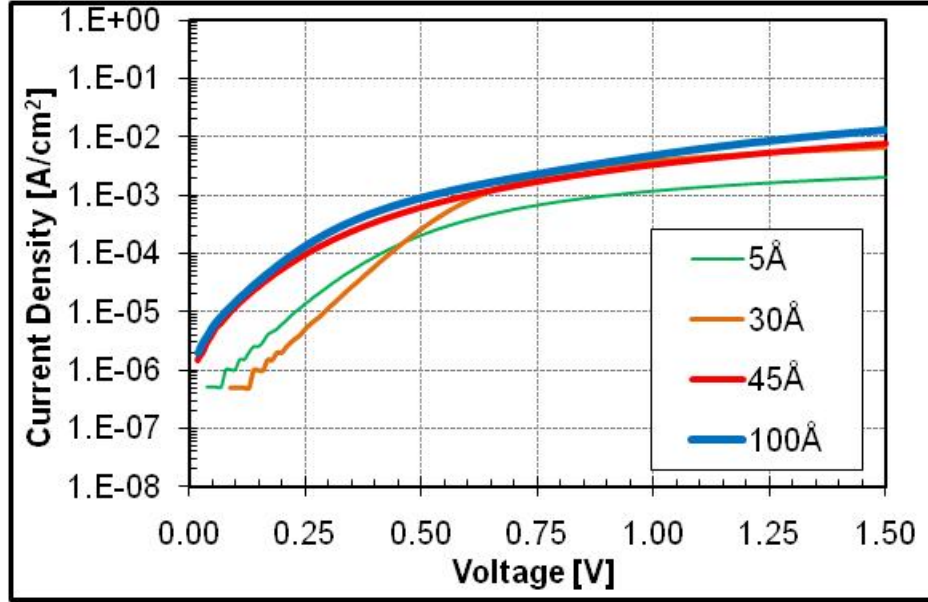
Figure 43. Dark J-V characteristics for different Cu_2Te thicknesses

Equation 19 gives the current equation for a typical diode.

$$J = J_s \times \left(e^{\frac{qV}{AkT}} - 1 \right)$$ (19)

where A is the diode quality factor and J_s is the reverse saturation current.

Using the data from Figure 43 the intercept of the y-axis gives J_s and the slope gives A. Using equation 10 (see Section 2.5.2) the value for V_{oc} can be calculated. A typical superstrate solar cell has A~1.4, J_s ~10^{-9} A/cm^2 and J_{sc}~25 mA/cm^2. This results in V_{oc} of 0.868 V which is very close to a typical value of 850 mV. From Figure 43, A was calculated to be 1.73, J_s was 10^{-7} A/cm^2 and from Table 10 J_{sc} was 14.81 mA/cm^2. Calculating V_{oc} using equation 19 resulted in a value of 540 mV. This value is really close to the V_{oc} (550 mV) obtained from the J-V measurement (see Table 10). This is an interesting finding as the quality of the junction is responsible for the low V_{oc} values. The back contact barrier,

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even though it is present for the low Cu_2Te thickness might not be high enough to affect the V_{oc} but just the FF of the device.

The J-V data from Figure 41 suggested an improvement in the back contact, although V_{oc} values seen in Table 10 did not improve. The high reverse saturation current and the high value of A indicate high recombination in the junction which is another factor limiting the value of V_{oc}.

These results suggest that in all instances (including the 5 Å case) a large amount of Cu reaches the junction, while the corresponding J-V suggest that the optimum back contact is achieved with one of the intermediate thicknesses (30 Å). The back contact/CdTe interface is subjected to the CSS high temperatures used for the deposition of CdTe and CdS and therefore is hard to control the amount of Cu able to diffuse even at the lowest thickness for Cu_2Te. Therefore the challenge for the substrate device is to develop a process to be able to limit/control the amounts of Cu at the back contact and the junction.

6.4.4 Evaporated Tellurium (Te) as a Back Contact

In typical superstrate configuration the CdTe surface is etched to provide a Te-rich layer which effectively results in a p^+-doped CdTe which is necessary to obtain better contact formation [90, 91]. This is usually accomplished by etching the CdTe surface in bromine-methanol solution or a mixture of nitric and phosphoric acids in water. In the substrate configuration the CdTe etching step cannot be done because the back contact is deposited before CdTe. In this study different thicknesses of Te layers are evaporated on the back contact prior to

CdTe deposition to investigate if an ohmic contact can be established by creating a Te-rich region in CdTe adjacent to the metal electrode. Te thickness was varied from 50 to 300 Å. Increase in Te thickness resulted in flaking of the CdTe. All CdTe films had pinholes seen with the naked eye. Te has a melting point of 449.5 °C. Te melting during the heating of the sample for CdTe deposition might caused adhesion problems leading to pinholes and flaking. J-V data are shown in Figure 44. The performance of the devices was limited due to shunting and low collection as seen from the fourth quadrant, resulting in low V_{oc} and FF's.
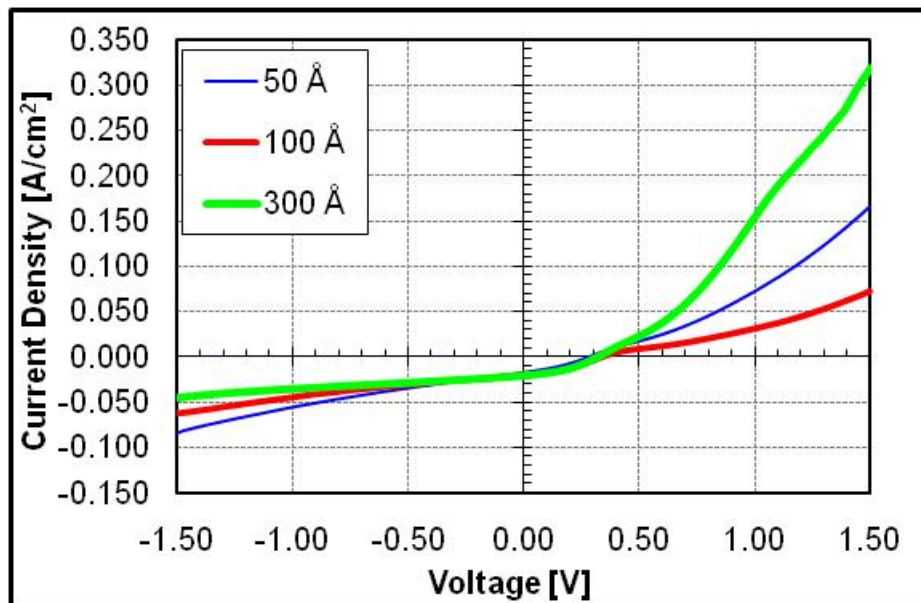
Figure 44. J-V data for solar cells with evaporated Te as a back contact

6.5 Diffusion Barriers

As previously mentioned the $CdCl_2$ heat treatment is a critical step for high efficiency CdTe/CdS solar cells. Flaking and discoloration was often observed on

the surface of the cells after the CdCl$_2$ treatment. Figure 45 shows an image of a film after the treatment. EDS analysis performed on the white spot (top left image) revealed a large concentration in iron, chromium and chlorine. This lead to the conclusion that at some point during the fabrication process impurities diffuse from the SS substrate to the film, that caused flaking and most probably had a negative effect on the performance of the cells.
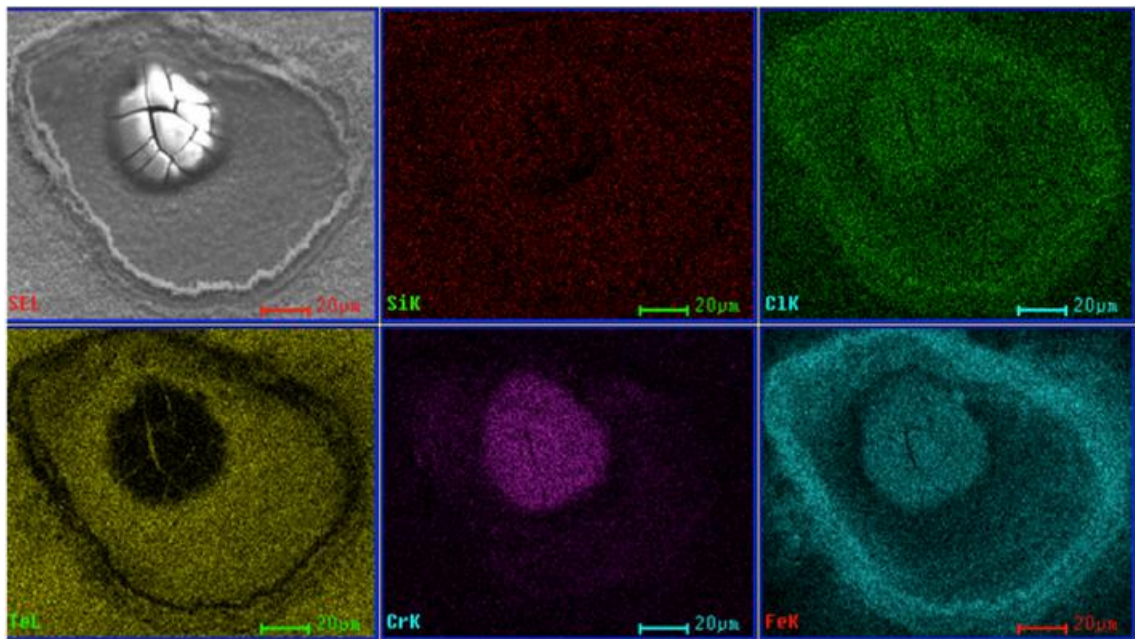
Figure 45. Elemental mapping around a CdTe surface feature; the maps show Cl (top right), Te (bottom left), Cr (bottom middle) and Fe (bottom right)

Secondary Ion Mass Spectroscopy (SIMS) analysis was conducted at the National Renewable Energy Laboratory (NREL). The results showed high concentration of Fe and Cr in the CdTe layer [92].

Impurity diffusion was also observed from groups developing CIGS solar cells on flexible metallic substrates [93]. In order to overcome this problem diffusion barriers can be applied to eliminate contamination. Such barriers are silicon oxide (SiO_x), aluminum oxide (Al_2O_3) and silicon nitride (Si_3N_4). $Al_2O_3$ oxide was found to reduce the amount of diffused Fe but Al from the barrier itself was diffusing in the solar cell.

6.5.1 Silicon Nitride (Si_3N_4) as a Diffusion Barrier

Silicon nitride films have been widely used in the semiconductor device industry because they are mechanically strong, have good dielectric properties and provide an excellent barrier against moisture corrosion and mobile ions. Si_3N_4 was deposited by Plasma Enhance Chemical Vapor Deposition (PECVD), followed by the deposition of Mo/ZnTe/CdTe/CdS/TC. To study the effect of the barrier, the thickness of Si_3N_4 was varied from 0.2 to 2µm. Figure 46 shows the V_{oc} and FF as a function of the barrier thickness. V_{oc} increases from 390 to 500 mV and FF from 20 to 32 % as the thickness of the barrier increases from 0.2 to 1 µm.

J-V characteristics are shown in Figure 47. The solar cell with the thinnest barrier had the poorest performance. High series resistance resulted in J_{sc} losses. As the barrier thickness increases the J-V data improved due to the lowering of the series resistance. All the samples still suffer from the severe roll-over in the first quadrant.

The device with the thickest Si_3N_4 had the best performance with V_{oc} of 500mV, J_{sc} of 18mA/cm^2 and 32% FF.
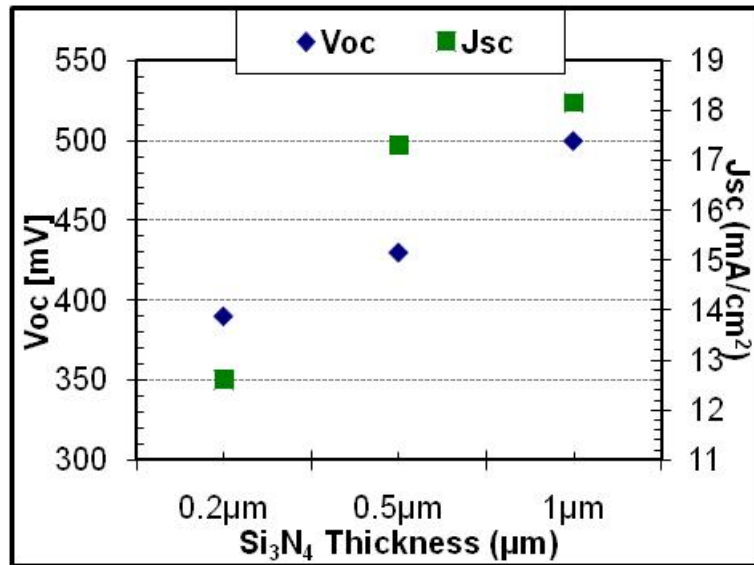
Figure 46. V_{oc}/J_{sc} data for cells with Si_3N_4 of different thicknesses
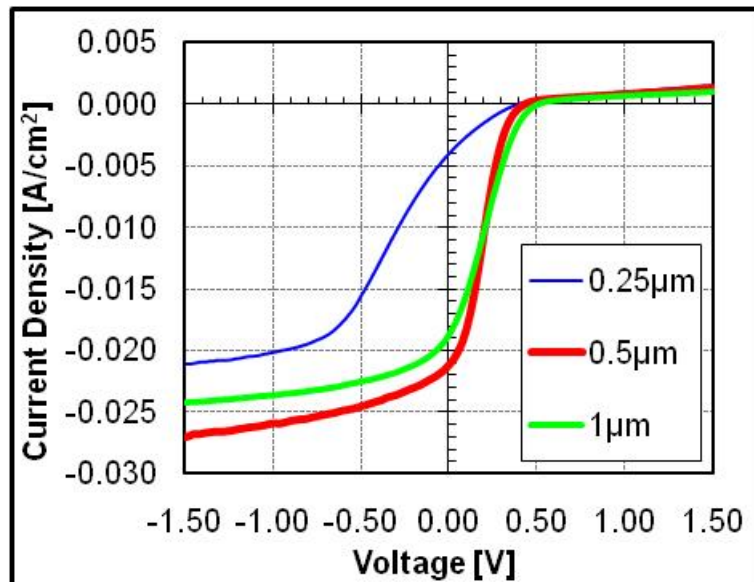
Figure 47. J-V data for cells shown in Figure 46

The improvements in performance due to the increase of the diffusion barrier are evident from the SR data shown in Figure 48. In the blue region all the cells have the same QE. Starting around 500nm there is a significant drop in the QE of the device with the smallest barrier. This can be explained by increased recombination due to impurity diffusion from the substrate. The red response improved as the barrier increases indicating improvement in collection.

Figure 48. SR data for cells with different Si_3N_4 thicknesses

Further increase of the barrier layer beyond 1µm was not successful. Adhesion problems causing flaking did not allow the fabrication of complete solar cells. Stress due to the increased thickness and the difference in the thermal expansion coefficients between Si_3N_4 and the different layers might be the explanation for this behavior.

6.5.2 Silicon Dioxide (SiO$_2$) as a Diffusion Barrier

Silicon dioxide is another material used as a diffusion barrier against impurities from the metallic substrates. Based on the results obtained from the Si$_3$N$_4$ study the thickness of the SiO$_2$ film was varied from 1 to 2µm. Reactive sputtering of silicon in argon and oxygen atmosphere was used for the deposition. One disadvantage of this process was the low deposition rates that required several hours to deposit 1-2 µm of SiO$_2$. Titanium improves adhesion to SiO$_2$ so a thin layer was applied before the Mo deposition [94].

The summary of the devices' performance is shown in Table 11. Similar data were obtained for all three SiO$_2$ thicknesses. These results suggest that SiO$_2$ performs better as a diffusion barrier compared to Si$_3$N$_4$.

Table 11. Summary data for different SiO$_2$ thicknesses

SiO$_2$ Thickness (µm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
1	530	19.15	38
1.5	560	18.83	37
2	540	19.48	39

The SR of all the cells is shown in Figure 49. The differences in the blue region are due to thickness variation in the CdS layer. The cell with the thinnest

barrier had a slightly lower carrier collection at longer wavelengths that might be due to impurities diffusing through silicon dioxide and into the bulk CdTe.
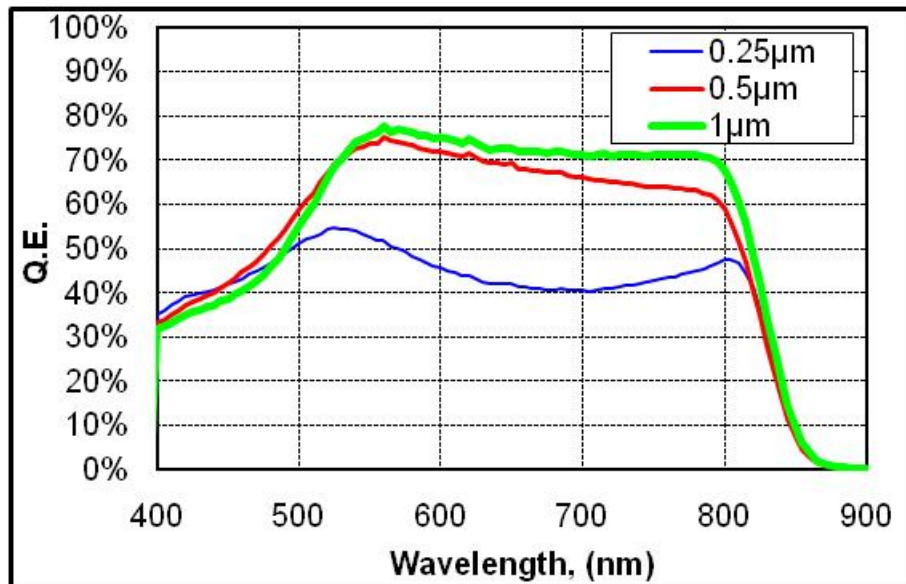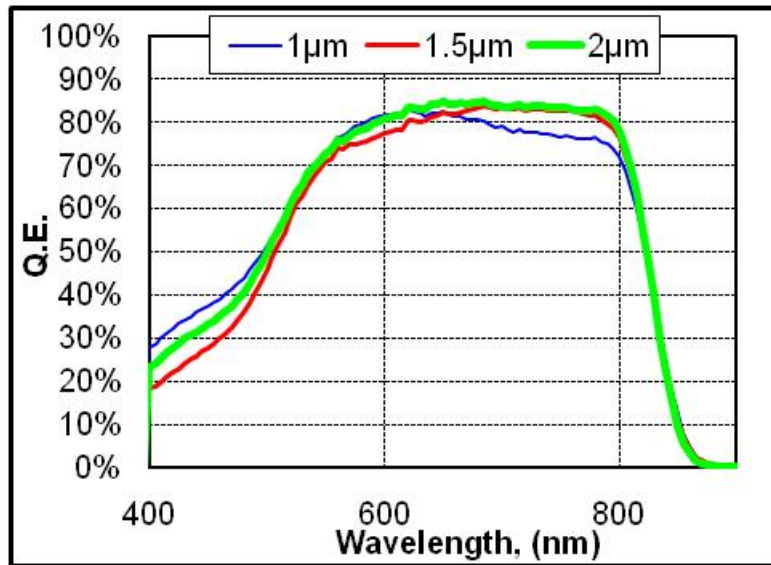

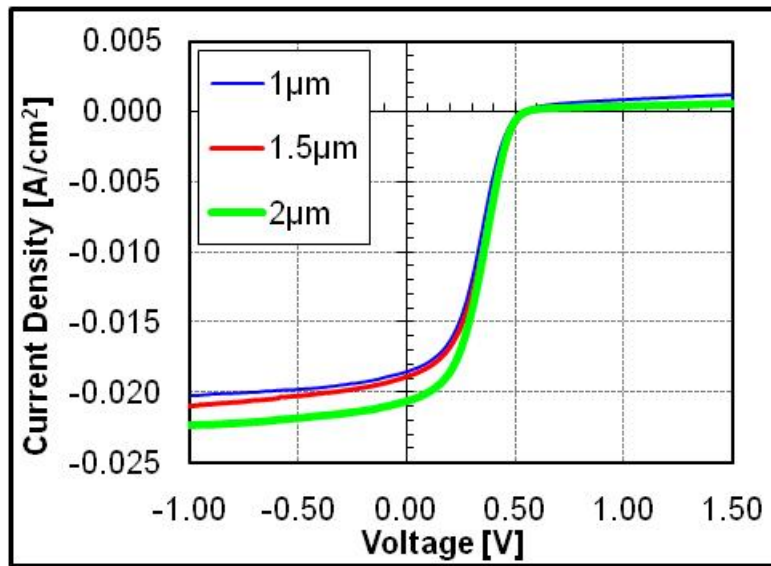Figure 49. SR data for cells with different SiO$_2$ thicknesses

Figure 50. J-V data for the cells shown in Figure 49

Figure 50 shows the J-V characteristics of the devices. All the curves exhibit the same behavior with the strong roll-over in the first quadrant that limits the FF and V_{oc}.

In this study the results suggest that SiO_2 is a better barrier than Si_3N_4, giving higher V_{oc}'s, J_{sc}'s and FF's. J-V and SR curves are almost identical for all three barrier thicknesses which suggest that a layer between 1-2 μm is adequate enough to be used as a diffusion barrier.

6.5.3 Molybdenum Nitride (Mo_xN_y) as a Diffusion Barrier

Thin films of molybdenum nitride have been extensively used in various technological areas, especially as diffusion barriers in microelectronics, hard wear–resistant materials in engineering and interconnections in semiconductor devices. All these applications are due to its properties such as good chemical stability, high melting point and high hardness [95]. Mo_xN_y films were deposited by reactive r.f. sputtering of a Mo target in an argon-nitrogen ambient, on molybdenum coated substrates. The thickness of the Mo_xN_y layer was kept constant at 0.5 kÅ for all the depositions. For the first part of this study the Ar-N_2 gas mixture during sputtering was varied to see the effect on completed solar cells. N_2 flow was increased from 1 to 3, 6 and 9 mT while adjusting the Ar flow to a total pressure of 12mT. XRD analysis showed the formation of different Mo_xN_y configurations for the different Argon to Nitrogen mixtures. Figure 51 shows the XRD spectra of the different Ar:N_2 ratios.

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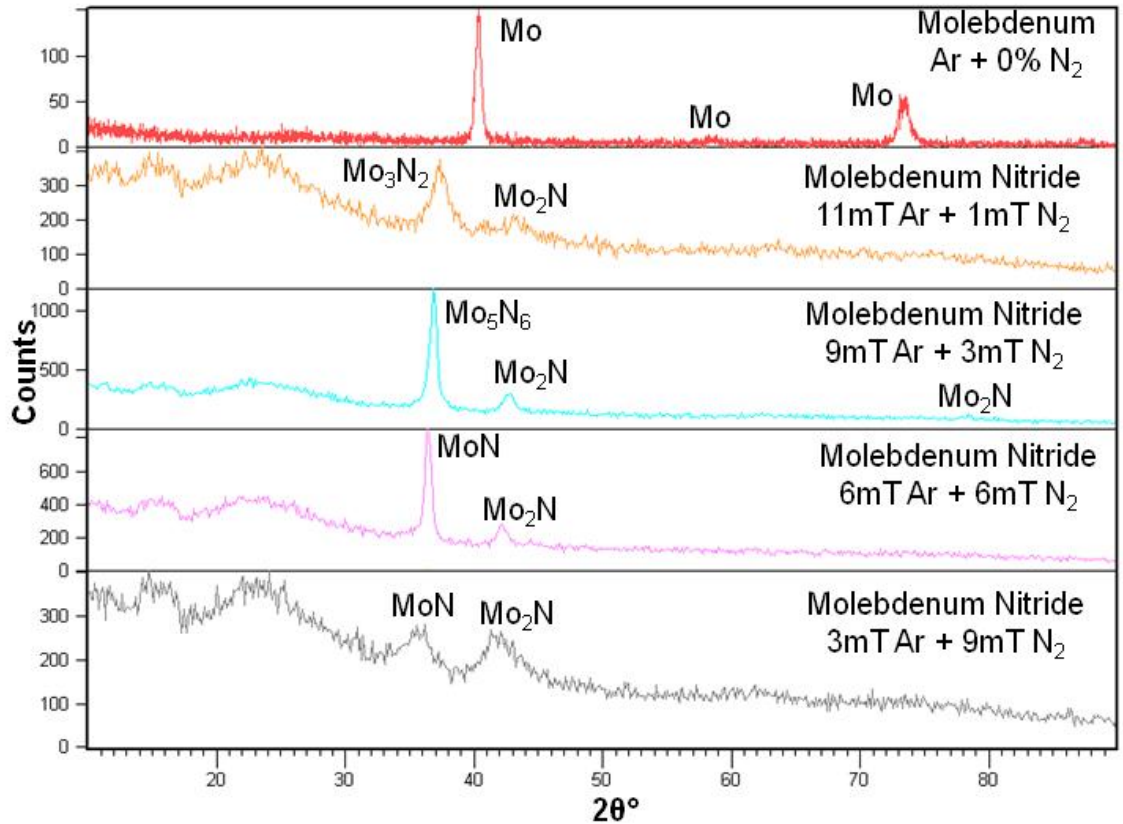
Figure 51. XRD spectra of Mo and Mo_xN_y films deposited at different Ar to N_2 ratios

Figure 52 shows the results for the different gas ratios. As the nitrogen pressure increases the V_{oc} and FF increase reaching a maximum at a ratio of 50:50. At a higher nitrogen pressure the FF reduces dramatically. It is not clear at this time what causes this variation in the results. One explanation might be that at the 50:50 ratio the nitrogen concentration in the Mo_xN_y layer makes it a better diffusion barrier as well as a good conducting interlayer between CdTe and Mo. Further studies are being done to try and determine the difference in the Mo_xN_y layers.
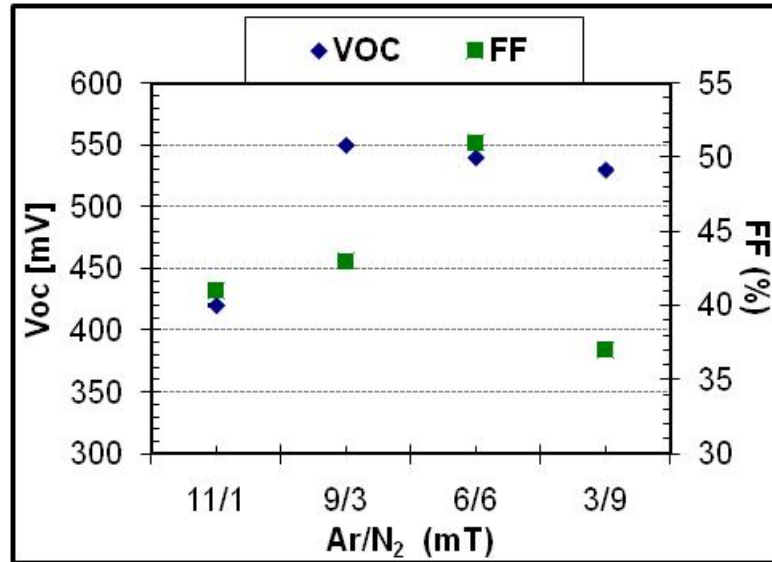
Figure 52. V_{oc}/FF data for devices with different Argon/Nitrogen mixture

The use of the molybdenum nitride layer, which was deposited after the Mo back contact, gave the best overall results compared to the other diffusion barriers. In the second part of this experiment the position of the Mo_xN_y layer in the solar cell was varied to see if that had any effects on the performance of the cells. Solar cells with the following configurations were fabricated:

- SS/Mo/MoN/CdTe/CdS/TC

- SS/MoN/Mo/CdTe/CdS/TC

- SS/Mo/MoN/Mo/CdTe/CdS/TC

- SS/MoN/Mo/MoN/CdTe/CdS/TC

Table 12 shows the summary for the different Mo/MoN configurations. All the characteristics of the cells have been improved and the addition of the Mo_xN_y.layer resulted in solar cells with good reproducibility. V_{oc}'s around 600mV, J_{sc}'s around 20mA/cm^2 and FF's close to 50% were achieved.

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Table 12. Summary data for different Mo/MoN configurations

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
Mo/MoN	540-600	19.07-20.03	43-51	5.25
MoN/Mo	500-590	19.19-20.40	41-43	5.17
Mo/MoN/Mo	540-570	19.77-20.50	42-45	5.25
MoN/Mo/MoN	540-560	19.77-20.37	41-45	5.13

Typical J-V and SR data for the above samples are shown in Figures 53 and 54 respectively.
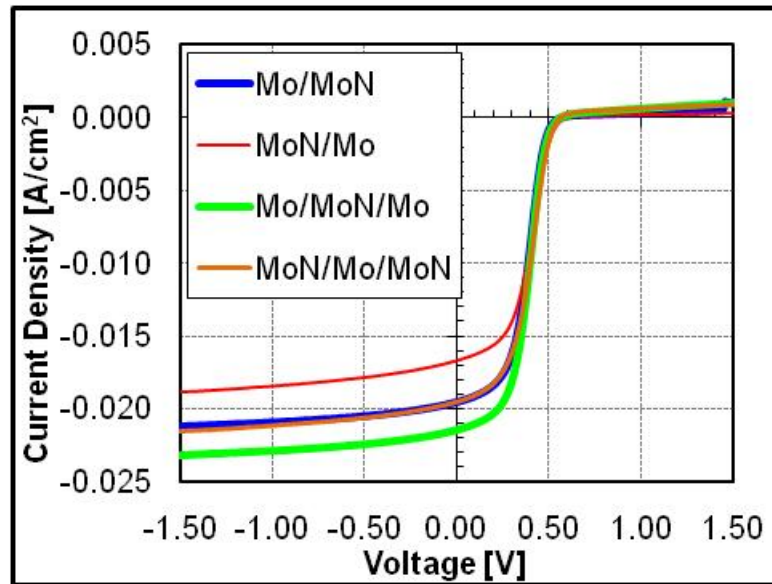
Figure 53. J-V data for devices fabricated with different Mo/MoN configurations
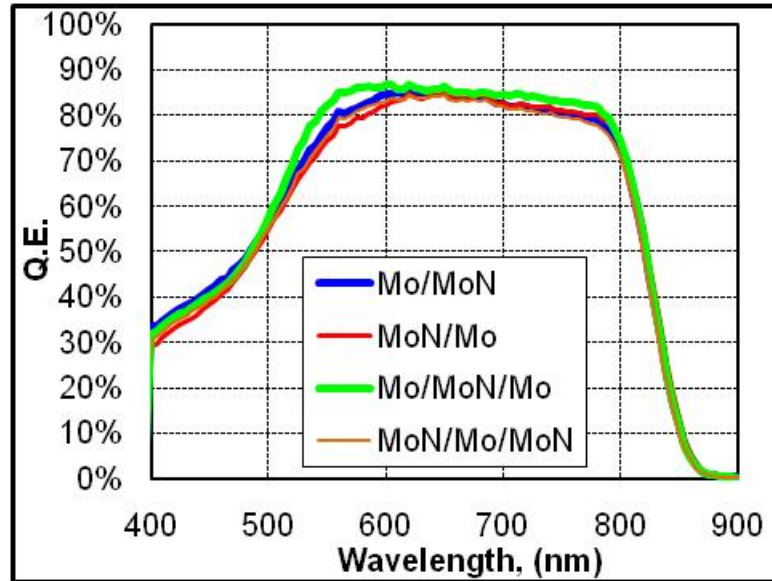
Figure 54. SR data for the devices shown in Figure 53

From the J-V and SR data it can be seen that the performance of the films with all configurations has been improved and all of them exhibit similar characteristics. From the SR characteristics, collection has been improved and the data look almost the same with the SR of films in the superstrate configuration. The presence of the back barrier is still obvious from the roll-over in the first quadrant of the J-V curves.

In order to further analyze the performance of the cells a series of measurements were performed. These included color I-V in the blue and red regions and C-V measurements. Figure 55 show the color I-V data of MoN/Mo/MoN and Mo/MoN/Mo configurations. Similar results were observed for the Mo/MoN and MoN/Mo configurations. The devices showed reduced collection at the long wavelengths that can be due to short carrier lifetimes because of recombination. Recombination centers might be the result of impurity diffusion

from the foil substrate or from the interface between the CdTe layer and the different Mo-MoN configurations.
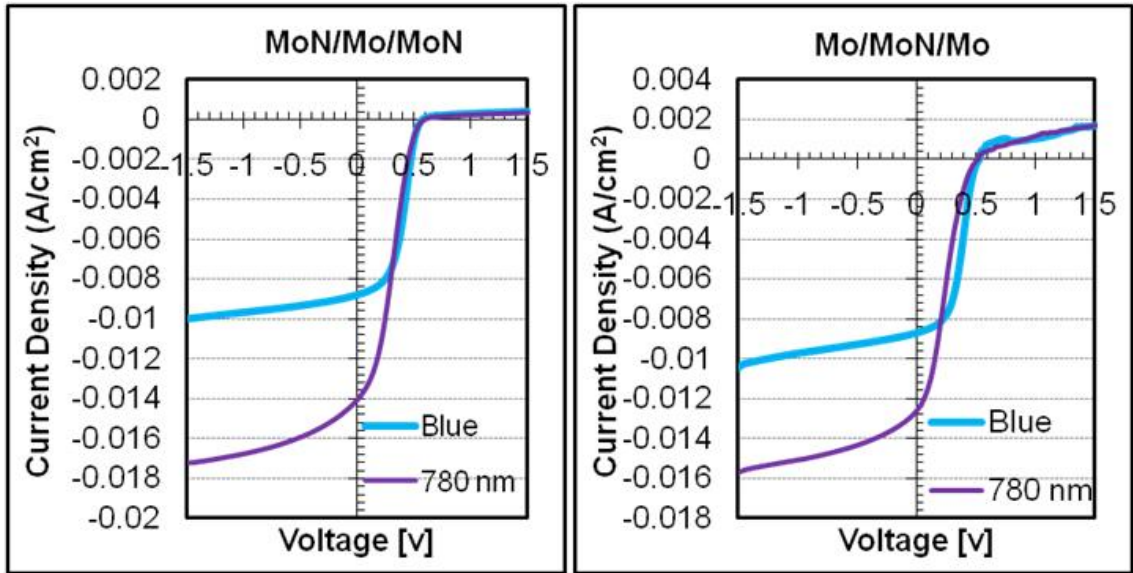
Figure 55. Color J-V's for MoN/Mo/MoN and Mo/MoN/Mo configurations
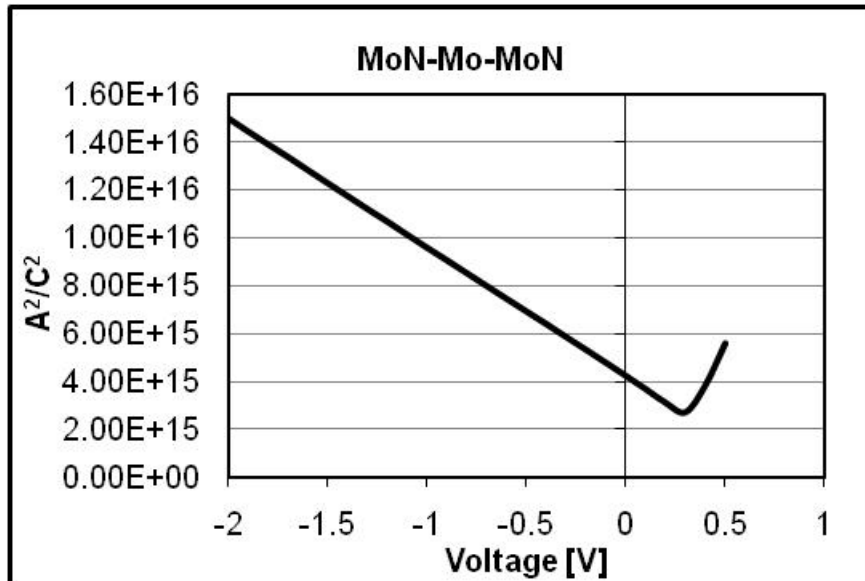
Figure 56. C-V measurement for the MoN/Mo/MoN configuration

Figure 55 shows the C-V measurement for the MoN/Mo/MoN configuration. Similar behavior was seen for the other devices in Figure 53. From the C-V measurement a decrease in the capacitance occurs around 0.3V in forward bias. The existence of a back contact diode that becomes reverse bias at this voltage causes the capacitance to decrease, confirming that there is a secondary diode in the opposite direction of the main junction diode. Similar behavior was also observed by others [96].

From this study it was concluded that the addition of a Mo_xN_y layer before CdTe improves V_{oc}, J_{sc} and FF of the cells. This can be due to a better diffusion barrier formation and good conductivity of the layer. Based on the presence of the roll-over seen in Figure 53 there is no improvement in the formation of the back contact. Therefore it seems that the Mo_xN_y layer acts as a diffusion barrier against the foil impurities.

Completed solar cells with different configurations have been sent for SIMS analysis in order to confirm the above conclusion.

6.5.4 Copper in the Mo-MoN Configuration

Molybdenum nitride can be used not only as an impurity barrier for the substrate but it has also been used as a Cu diffusion barrier in the microelectronic industry.

Small amounts of Cu were sputtered deposited in order to obtain a better back contact and to see weather MoN can block the amount of Cu delivered to the device. Cu thickness was varied from 10-30Å, and similar results were

obtained for all thicknesses. The configuration of the devices was SS/MoN/Mo/Cu/MoN/CdTe/CdS/ITO.

Figure 57 shows the SR of the device. The decrease of the SR above 600nm strongly suggests higher recombination of photogenerated carriers in the CdTe layer because of Cu related defects.
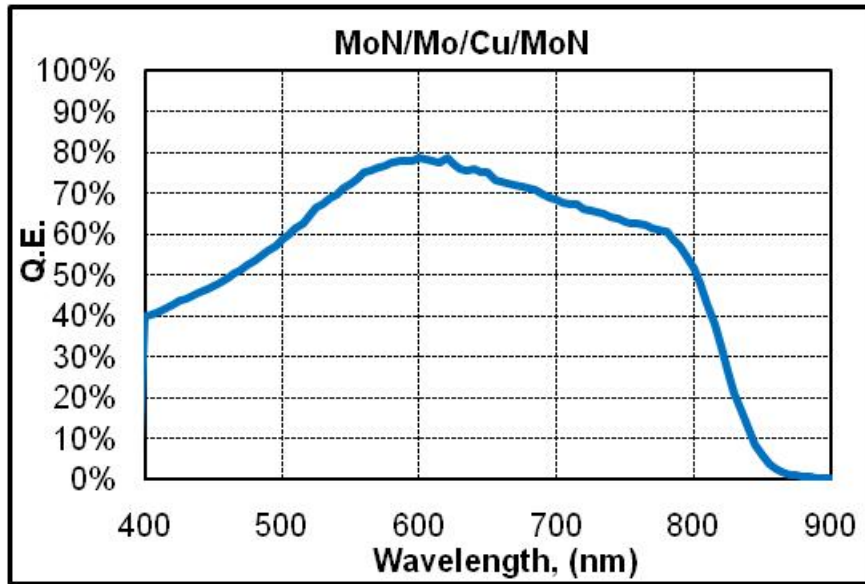
Figure 57. SR of a device with MoN/Mo/Cu/MoN as a back contact

Dark and light J-V curves of the device are shown in Figure 58. Table 13 shows the measured V_{oc}, J_{sc} and FF of the above device.

Table 13. Measured data for the MoN/Mo/Cu/MoN configuration

V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
590	17.68	49

Roll-over in the first quadrant is greatly reduced suggesting that the addition of Cu improved the back contact. The other observation is the cross-over between the light and dark J-V's. A possible explanation has to do with the photoconductivity of CdS. Cu diffusing in to CdS can act as acceptor states to free electrons resulting in low electron concentration and therefore increasing the resistivity of CdS in the dark. Under illumination electron concentration in CdS increases resulting in an increase of the CdS conductivity.
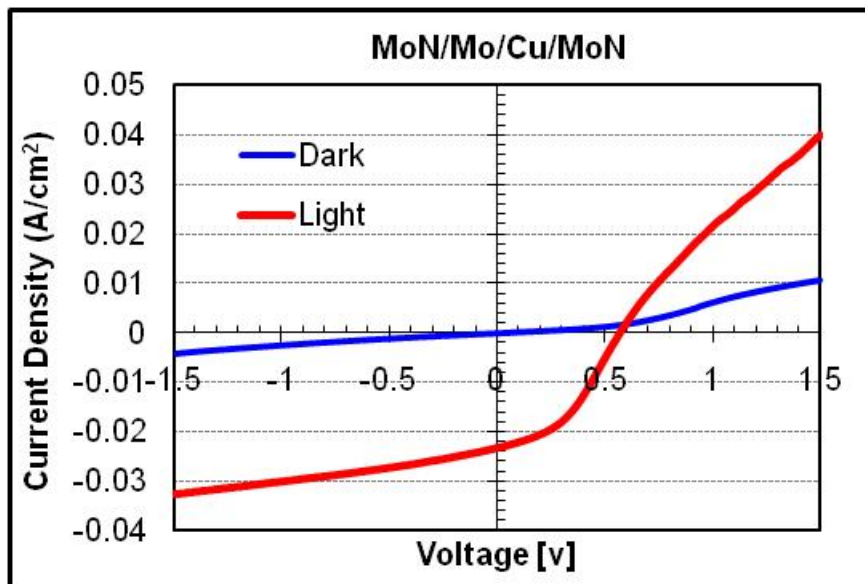
Figure 58. Light and dark J-V's for the device with the MoN/Mo/Cu/MoN configuration

Even though the addition of small amounts of Cu eliminated some of the roll-over, there is evidence of Cu diffusing in the bulk CdTe and possibly into CdS. Other ways will have to be implemented to incorporate Cu into the back contact without significant diffusion into the device.

CHAPTER 7

CONCLUSIONS

The primary objective of this work was to invert the superstrate CdTe solar cell into a substrate device, and develop a process for high efficiency CdTe solar cells on flexible substrates.

Adhesion, stress and flaking of the films were influenced by the properties of the foil used. The use of SS 430 minimized the difference between the CTE's of the foil and the deposited films that resulted in improved adhesion and performance.

The growth of Mo, ZnTe and CdTe on flexible substrates was studied. Adhesion of Mo films and resistivity are dependent on the deposition conditions. The use of Mo bi-layers eliminated the stress in the films promoting adhesion and resulted in films with low resistivity. ZnTe and CdTe films exhibited strong preferential orientation as the substrate temperature decreased. Lower substrate temperatures resulted in more densely packed and more uniform films.

Impurity diffusion from the SS foil into the device during fabrication caused flaking of the films. Impurity barrier layers were introduced in the solar cell as a solution to the problem. Si_3N_4, SiO_2 and Mo_xN_y were the barriers used.

The performance of the solar cells improved as the Si_3N_4 thickness increased. Increase of the film beyond 1μm in thickness resulted in flaking of the device, most probably related to stress. SiO_2 films between 1 and 2 μm were used. Device performance improved and was similar for all thicknesses.

The use of Mo_xN_y resulted in devices with the highest performance out of all the impurity barriers used. All the characteristics of the cells improved and the addition of the Mo_xN_y.layer resulted in solar cells with good reproducibility. V_{oc}'s around 600mV, J_{sc}'s around 20mA/cm^2 and FF's close to 50% were achieved.

Despite the improvement in adhesion and performance with the use of the diffusion barriers all devices exhibited signs of a back barrier contact that was the limiting factor in the performance of the devices.

Different interlayer/back contacts were used to improve the formation of the back contact. ZnTe was the first material used. Voc improved but the high resistivity of ZnTe limited the collection of carriers. The roll-over seen in the J-V data indicated no improvement in the back barrier.

Cu was used before the deposition of ZnTe as a way of doping the film. The addition of Cu improved the back contact as the roll-over in the first quadrant of the J-V data was reduced. The performance of the devices was limited due to shunting and very poor collection because of excess Cu diffusion into the solar cell.

To limit the amount of free Cu from diffusing into the device Cu_2Te was used. The performance was best at a thickness of 30 Å. Roll-over was improved but reduced carrier lifetimes had a significant effect on carrier collection. Dark J-V

measurements resulted in high diode quality factor and reverse saturation current indicating that the junction might be responsible for the low V_{oc}'s and not the presence of the back contact barrier.

Substrate CdTe solar cells fabricated on SS foil have to-date reached efficiencies of 6.8 %.

The biggest challenge has been the formation of the back contact. Future work should focus on ways to dope ZnTe with Cu, Sb or N_2. Further studies should concentrate on the formation of the front junction. Recombination centers in the CdS/CdTe junction can also limit the V_{oc} of the devices. Improving the formation of the junction will improve the performance of the cells.

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