SCHOLAR COMMONS
USF UNIVERSITY OF SOUTH FLORIDA

University of South Florida
Scholar Commons

Graduate Theses and Dissertations

Graduate School

2009

Non-contact characterization of dielectric conduction on 4H-SiC

Helen N. Benjamin
University of South Florida

Follow this and additional works at: http://scholarcommons.usf.edu/etd

Part of the American Studies Commons

Scholar Commons Citation
Benjamin, Helen N., "Non-contact characterization of dielectric conduction on 4H-SiC" (2009). *Graduate Theses and Dissertations.* http://scholarcommons.usf.edu/etd/1852

This Dissertation is brought to you for free and open access by the Graduate School at Scholar Commons. It has been accepted for inclusion in Graduate Theses and Dissertations by an authorized administrator of Scholar Commons. For more information, please contact scholarcommons@usf.edu.

Non-Contact Characterization of Dielectric Conduction on 4H-SiC

by

Helen N. Benjamin

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
Department of Electrical Engineering
College of Engineering
University of South Florida

Major Professor: Andrew M. Hoff, Ph.D.
Stephen E. Saddow, Ph.D.
Scott W. Campbell, Ph.D.
Richard A. Gilbert, Ph.D.
Sarath Witanachchi, Ph.D.

Date of Approval:
April 30, 2009

Keywords: Corona-Kelvin Metrology, Field Emission, Voltage Decay, Non-Contact SILC, Trapped Charge

© Copyright 2009, Helen N. Benjamin

Dedication

I would like to dedicate this manuscript to Mom, Dad, Marcia, Hilma, Alicia, Maurice, and family. Through their constant prayers and positive words of encouragement, I was able to overcome the challenges that I encountered throughout my pursuit of this degree. Also, to my fiancé, Leonard, thank you for believing in me and providing a listening ear throughout this endeavor.

Acknowledgments

I am grateful to Andrew Hoff, Ph.D., for giving me the opportunity to work in this field of non-contact metrology. I am also indebted to Elena Oborina, Ph.D., for not only providing me with scientific criticism of my work but also helping me with data acquisition. To Sasha Savtchouk, Ph.D., and John D'Amico, Ph.D., at Semiconductor Diagnostics, Inc. (SDI), thanks for providing technical support for the FAaST-230 tool. I would also like to thank Eric Persson for teaching me how to analyze statistical data. To my committee members, Stephen Saddow, Ph.D., Richard Gilbert, Ph.D., Sarah Witanachchi, Ph.D., and Scott Campbell, Ph.D., I greatly appreciate your time, suggestions, and support of this manuscript. To Robert Tufts and Richard Everly at Nanomaterials and Nanomanufacturing Research Center (NNRC), thanks for the metrology training. Finally, I would like to thank all my friends and colleagues, Gene Short, Aura Polo, Norelli Schettini, Alexandra Oliveros, Chris Frewin, and Chris Locke for being my social outlet.

Table of Contents

List of Tables ... iv

List of Figures ... vi

Abstract ... xi

Chapter 1. Introduction ... 1
1.1. Research Objectives and Motivation ... 1

Chapter 2. Overview of Electrical Stress Testing Methodology of Dielectrics ... 4
2.1. Standard Measure of Oxide Quality ... 4
2.2. Overview of 4H-SiC Substrates ... 5
2.2.1. Silicon Carbide (SiC) Oxidation Theory ... 8
2.3. Current Ramp Test and Voltage Ramp Test ... 10
2.4. Conduction Mechanisms of Dielectric-Semiconductor System ... 11
2.4.1. Poole-Frenkel Conduction ... 12
2.4.2. Fowler-Nordheim Conduction ... 14
2.5. Constant Current Stress Technique ... 20
2.6. Time Dependent Dielectric Breakdown (TDDB) ... 21
2.7. Contact Stress Induced Leakage Current (SILC) Technique ... 27
2.8. Non-Contact Stress Induced Leakage Current (SILC) Technique ... 30
2.8.1. Corona-Kelvin Metrology ... 30
2.8.2. Capacitance-Voltage Measurements ... 33
2.8.3. Equivalent Oxide Thickness (EOT) Measurement ... 38
2.8.4. Current-Voltage Measurements ... 40
2.8.5. Stress-Induced Leakage Current Method ... 42
2.9. Statistical Issues in Device-Based Measurements ... 45
2.10. Chapter Summary ... 46

Chapter 3. Experimental Procedures 48
3.1. Non-Contact Instrumentation 48
3.1.1. Film Analysis and Substrate Testing (FAaST) 230 and Components 48
3.1.2. Ion-Drift Spectrometer 51
3.2. Pre-Oxidation Cleaning Procedure 52
3.3. Oxidation Sequence/Interval Experiments 53
3.3.1. Brief Description of Afterglow (AG) Furnace 54
3.3.2. Afterglow (AG) Oxidation Parameter Variations 55
3.3.3. Thermal Oxidation 60

Chapter 4. Experimental Results and Discussion 61
4.1. Measurement Test Conditions 61
4.2. Non-Contact Corona Current Stress 61
4.3. Potential Factors Affecting the Accuracy of the Contact Potential Difference 68
4.4. Fowler-Nordheim Conduction in Afterglow Oxide and Thermal Oxide on 4H-SiC 69
4.4.1. Self Adjusting Steady State (SASS) Voltage on Oxides 82
4.4.2. Significant Parameters: Effective Mass in the Oxide and Barrier Height 83
4.4.3. Comparison with Fowler-Nordheim Literature Data on Oxide-n-type 4H-SiC Devices 87
4.4.4. Influence of Trapped Charge in the Oxide 90
4.4.5. Fowler-Nordheim Equation Modification for Oxide-4H-SiC 94
4.5. Distribution of Trapped Charge in Oxide on 4H-SiC 97
4.5.1. Diluted Hydrofluoric Acid Etch Rate on Oxide-4H-SiC 97
4.5.2. Influence of Dehydration Procedure on Oxide-4H-SiC 100
4.5.3. Effective Trapped Charge Distribution 102
4.6. Non-Contact Stress Induced Leakage Current (SILC) Analysis 106
4.6.1. Oxidation Process Influence on Leakage Current 107
4.6.2. Oxide Consistency: Statistical Distribution 109

Chapter 5. Conclusion 118
5.1. Summary of Research Contributions 118
5.2. Future Work 121

References 123

Appendices 131
Appendix A: Afterglow Oxide Recipes 132

About the Author .... End Page

List of Tables

Table 2.1: Properties of 4H-SiC and Si at room temperature (300K) [14-16]. 7

Table 2.2: Chemical reactions during dry thermal oxidation of SiC [20]. 9

Table 2.3: Commonly used effective oxide mass for Fowler-Nordheim calculations. 18

Table 3.1: Annealed afterglow (AG) recipes. 56

Table 3.2: Non-annealed afterglow (AG) recipes. 57

Table 4.1: Stress current measurement parameters and conditions. 63

Table 4.2: Stress measurement protocol. 65

Table 4.3: Oxidation process chemistry variation. 73

Table 4.4: Calculated effective barrier for annealed 4H-n-type experimental samples. 76

Table 4.5: Calculated effective barrier for non-annealed 4H-n-type experimental samples. 76

Table 4.6: Reported effective barrier height for 4H-SiC MOS devices at room temperature. 89

Table 4.7: Etch rate comparison between 4H-SiC and Si wafers at 24^0C. 98

Table 4.8: Effective trapped charge calculation parameters. 105

Table 4.9: Stress measurement protocol for SILC measurements. 110

Table A.1: AG I_A Recipe 132

Table A.2: AG I_B Recipe 132

Table A.3: AG II Recipe 133

Table A.4: AG III Recipe 134

Table A.5: AG IV Recipe 135

Table A.6: AG V Recipe 136

Table A.7: AG VI Recipe 137

Table A.8: AG VII Recipe 138

Table A.9: AGW I Recipe 139

Table A.10: AGW II Recipe 140

Table A.11: AGW III Recipe 140

Table A.12: AGW IV Recipe 141

Table A.13: AGW V Recipe 141

Table A.14: AGW VI Recipe 142

List of Figures

Figure 2.1: A simple MOS capacitor. 4

Figure 2.2: Four carbon atoms covalently bonded with a silicon atom [12]. 6

Figure 2.3: A 4H-SiC three-dimensional lattice structure [13]... 6

Figure 2.4: Location of oxide charges after a thermal oxidation of Si [24]...................... 10

Figure 2.5: Example of Poole-Frenkel plot for SiO_2 on Si. 13

Figure 2.6: Energy band diagrams depicting a MOS device without stress (a) and under Fowler-Nordheim tunneling (b). 15

Figure 2.7: An example of a Fowler-Nordheim plot. 17

Figure 2.8: An example of a gate voltage-time characteristic of a MOS device obtained by CCS testing [33]. 20

Figure 2.9: Weibull cumulative distribution for a population fraction failing by time [47]. 23

Figure 2.10: An example of a Weibull plot [48]. 24

Figure 2.11: A normal cumulative distribution function for a population failing by y [47]. 27

Figure 2.12: A sketch illustrating an nMOS (a) without stress and (b) after SILC. 28

Figure 2.13: An example of SILC modes [3]. ... 29

Figure 2.14: A sketch of Kelvin probe measurement. ... 31

Figure 2.15: Energy band diagram after the deposition of corona charges. ... 35

Figure 2.16: Non-contact C-V characteristics of (a) a 150 Å thermal oxide on a p-type Si and (b) a 400 Å afterglow oxide on an n-type 4H-SiC. ... 37

Figure 2.17: Non-contact C-V characteristic of a 499 Å afterglow oxide on an n-type 4H-SiC measured in the dark (circles) and in the light (asterisks). ... 39

Figure 2.18: Oxide voltage decay after corona charging [76]. ... 41

Figure 2.19: Energy-band diagram during non-contact SILC. ... 43

Figure 2.20: Example of determining thickness with the Fowler-Nordheim current density [64]. ... 44

Figure 3.1: Schematic of the measurement apparatus based on ref. [64]. ... 49

Figure 3.2: Sketch of the (a) wire enclosure, (b) discharge distance to the wafer, and (c) aperture diameter. ... 51

Figure 3.3: RCA cleaning procedure. ... 53

Figure 3.4: Sketch of afterglow furnace system [77]. ... 54

Figure 3.5: Measurement sequence to calculate J_{F-N}. ... 57

Figure 3.6: Etch pattern and quadrant designation on the substrate. ... 58

Figure 3.7: Measurement sequence to calculate trapped charge. ... 59

Figure 3.8: Measurement sequence to obtain SILC data acquisition............................... 60

Figure 4.1: Current density versus V_{cpd} for various corona currents. 62

Figure 4.2: Theoretical ideal D_{it}=0 (before stress) and $D_{it} \neq 0$ (after stress) [33]. 64

Figure 4.3: Capacitance-voltage characteristics versus corona stress. 66

Figure 4.4: Poole-Frenkel plot comparing theoretical and experimental oxides. 70

Figure 4.5: Fowler-Nordheim plot for various thermal oxide thicknesses on Si. 72

Figure 4.6: Oxidation process chemistry influence on the effective barrier height for SiO_2/4H-SiC systems (see Table 4.3 for oxidation process representation).. 74

Figure 4.7: Fowler-Nordheim plot of AG annealed oxides. 77

Figure 4.8: Fowler-Nordheim plot of thermal annealed oxides...................................... 78

Figure 4.9: Fowler-Nordheim plot of non-annealed AG oxides...................................... 80

Figure 4.10: Comparison of experimental data and predicted Fowler-Nordheim lines. 81

Figure 4.11: Steady-state voltage experimental oxide comparison. 83

Figure 4.12: Variation of M_{ox} on the predicted Fowler-Nordheim characteristics.. 84

Figure 4.13: Theoretical Fowler-Nordheim plot varying the effective barrier height with M_{ox} of 0.36. 86

Figure 4.14: Example of current-voltage characteristics of a 4H-SiC MOS capacitor with a 500 Å gate oxide measured at room temperature [52]. 87

Figure 4.15: Fowler-Nordheim conduction comparison of contact versus non-contact measurements.. 90

Figure 4.16: Charge trapped within tunneling regime in SiO_2/Si system: (a) negative charge trapping, (b) positive charge trapping [92].. 92

Figure 4.17: Example of trapped charge outside or inside the Fowler-Nordheim tunneling regime in a 500 Å oxide................................. 93

Figure 4.18: Capacitance-voltage characteristics of AG IV and Thermal TA oxides before and after stress.. 95

Figure 4.19: Non-triangular Fowler-Nordheim plot fitted to experimental oxides. 96

Figure 4.20: Oxide thickness after diluted HF etching for oxide AG IV_EA. 99

Figure 4.21: Oxide thickness after diluted HF etching for oxide AG IV_EB. 100

Figure 4.22: The influence of a dehydration method on the Fowler-Nordheim plot (a) AG IV_EA and (b) AG IV_EB....................... 101

Figure 4.23: Fowler-Nordheim plot of thinner oxides (unfilled geometric shapes) compared to thick oxides (filled geometric shapes). 103

Figure 4.24: Absolute trapped charge versus oxide thickness...................................... 104

Figure 4.25: Measurement site positions. 107

Figure 4.26: Effect of stress fluence on a 150 Å thermal oxide grown on a p-type Si substrate.. 108

Figure 4.27: Current density versus oxide field at point (10, 10) for AG I_A oxide. 110

Figure 4.28: Probability plot for AG III oxide at each cumulative time......................... 111

Figure 4.29: Probability plot of AGW I oxidation process run repeatability. 112

Figure 4.30: Probability plot of AG I_A oxidation process run repeatability. 113

Figure 4.31: Probability plot of AG II oxidation process run repeatability.................... 115

Figure 4.32: Probability plot of AG III oxidation process run repeatability. 116

Figure 4.33: Leakage current sites greater than $1 \times 10^{-7} A/cm^2$.. 117

Non-Contact Characterization of Dielectric Conduction on 4H-SiC

Helen N. Benjamin

ABSTRACT

Consistent charge or defect control in oxide grown on silicon carbide (SiC) continues to be difficult to achieve and directly impacts the electrical performance of SiC-based metal oxide semiconductor (MOS) devices. This research applied non-contact Corona-Kelvin metrology to investigate the charge transport in oxides grown on n-type 4H-SiC epitaxial substrates. The cost and engineering science impact of this metrology are significant as device fabrication is avoided leading to quick determination of electrical characteristics from as-grown oxide films. Non-contact current-voltage (I-V) measurements of oxide on SiC were first demonstrated within this work and revealed that Fowler-Nordheim (F-N) current emission was the dominant conduction mechanism at high electric fields.

Oxides on SiC were grown at atmospheric pressure (thermal oxides) or at a reduced pressure (afterglow oxides) ambient and examined using non-contact charge-voltage (Q-V), capacitance-voltage (C-V), equivalent oxide thickness (EOT), and I-V methods. The F-N conduction model was modified to address charge trapping and effective barrier effects obtained from experimental oxide films. Trap densities determined with this metrology were used to show that the F-N model including their

density and position was adequate for thermal oxides on SiC but not for afterglow films. Data from the latter films required further modification of the theory to include a chemical effect of the oxide growth process on the effective conduction band offset or barrier. This work showed that afterglow chemistry was able to vary the effective conduction band offset from 2.9 eV, typical of thermal oxidation of SiC, up to 3.2 eV.

Stress induced leakage current (SILC), an excess above the F-N base current resulting from prolonged current through the dielectric films, was also investigated. Multiple point SILC testing was used to identify statistical effects of process variations and defects in as-grown oxide films on SiC. These results open the possibility to improve oxide manufacture on SiC using methods common in the silicon IC industry. This work demonstrated the first non-contact F-N current determination in oxides on SiC and showed both charge trapping and chemical dependencies of as-grown films. Future studies may extend the findings of this work to further improve this important dielectric-semiconductor system.

Chapter 1. Introduction

1.1. Research Objectives and Motivation

Silicon carbide (SiC), a wide band gap semiconductor, is an ideal candidate for the development of the next generation high power, frequency, and temperature device applications. The quality of an oxide can directly influence the electrical performance of metal oxide semiconductor (MOS) devices. Process induced charges in the oxide, which can either be neutral, positive, or negatively charged, impact the reliability and integrity of gate oxides in MOS devices. The commercialization of silicon-based MOS devices is due to over four decades of research based on the control of charges at the silicon dioxide/silicon (SiO_2/Si) interface or in the bulk of the oxide. For example, one popular treatment to reduce charges in the oxide is the addition of a post annealing process after oxidation and metallization of the gate. The realization of commercialized SiC-based power devices, controlled by MOSFETs (field effect transistors), is contingent on the control of charges in the oxide. Currently, an optimized oxidation process, for this binary semiconductor, to reduce charges in the oxide remains under investigation. Extensive analysis to obtain significant consistent statistical data for SiO_2/SiC characterization is costly and time consuming using standard measurement techniques accepted for SiO_2/Si characterization.

The aim of this research was to investigate the application of non-contact stress induced leakage current (SILC) testing for oxides grown on 4H-SiC epitaxial substrates. Non-contact SILC testing has been successfully established for oxide characterization on Si substrates to detect the vulnerability of an oxide film to breakdown or become conductive. Oxide breakdown induced by SILC testing on SiO_2/Si systems has been generally characterized by trap-assisted tunneling. In the advent of integrated-circuit (IC) chip miniaturization, one popular characterization technique done on thin oxides grown on Si is SILC testing [1-5]. This testing has also been used to characterize thick oxides on Si [6, 7]. Currently, oxides grown on SiC substrates for MOSFETs used in power devices are nominally 500 Å thick. The gate oxide is predominately characterized by current-voltage measurements to determine such parameters as its Fowler-Nordheim tunneling characteristics and its time-to-breakdown characteristics. Prior to this research, SILC testing on SiO_2/SiC systems has not been extensively reported in literature. Since this testing technique does not exist for the characterization of oxides on 4H-SiC substrates, it is intended to have the same characterization success established for SiO_2/Si systems.

Specifically, this work investigated the details and variations in the conduction mechanism of an oxide grown on n-type 4H-SiC substrates using a modified non-contact characterization tool. Stress induced leakage current is the excess current in addition to the Fowler-Nordheim current for oxide thicknesses greater than 50 Å. It was essential to establish the Fowler-Nordheim current as the dominate conduction mechanism for each experimental oxide. The testing methods developed identified the Fowler-Nordheim current on each oxide.

It was observed that the value for the effective barrier height and the effective mass in the oxide were influenced by oxidation process conditions. These two parameters are important because they define the Fowler-Nordheim curve characteristic. The effective barrier height in this case is related to the conduction band offset of the oxide-semiconductor interface. Trapped charges in the oxide also strongly influenced the Fowler-Nordheim characteristics and as a result, a variation of the Fowler-Nordheim equation was addressed. The location of the trapped charge and its centroid was further analyzed to fit the experimental data to a modified Fowler Nordheim tunneling equation.

After establishing this current, seventeen sites on various oxides were subjected to non-contact SILC testing and analyzed. The goal was to use the effective SILC value as an indicator to identify weak spots around the oxide surface. It was shown that this unique characterization method for oxides on n-type 4H-SiC has the potential to be used as a measure of oxide reliability. In addition, it enabled a fast assessment of an oxidation process in the absence of fabricated capacitors or transistors.

Chapter 2. Overview of Electrical Stress Testing Methodology of Dielectrics

2.1. Standard Measure of Oxide Quality

The reliability of an oxide grown on SiC substrates dictates its success in IC chips. Gate oxide of Si-based devices, such as capacitors or field effect transistors, have been extensively researched over four decades and summarized by D.J. Dumin, D.J. Dimaria, J.H. Sathis and others [3, 8-11]. A simple MOS capacitor test device is composed of a semiconductor, a gate oxide, and a gate (see Figure 2.1). The gate is either a metal plate or doped poly-silicon, where a voltage or current can be applied.

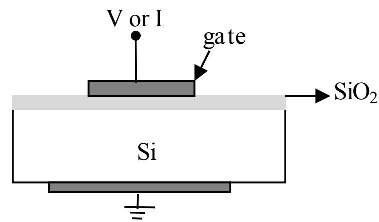


Figure 2.1: A simple MOS capacitor.

Oxide breakdown is the wear out mechanism in the oxide after losing its insulating or resistive properties in the presence of high or low electric fields due to the breakage of SiO_2 bonds in its lattice structure. There are two types of oxide breakdown: destructive (hard breakdown (HBD)-irreversible) and non-destructive breakdown (soft breakdown (SBD)-reversible). These breakdowns can be due to intrinsic failures, such as the quality of the oxide, extrinsic failures, such as electrical stress, or both. The quality of the oxide

corresponds to its processing condition (e.g. free from metal contamination), its uniformity, its surface roughness, and any other form of micro-defects. The ability to monitor an oxide behavior over a range of electric fields in the oxide can be performed using either a current or voltage ramp test.

2.2. Overview of 4H-SiC Substrates

Silicon carbide (SiC) crystal growth is not manufactured by the highly engineered Czochralski (CZ) crystal growth method, but from the seeded sublimation growth method [12]. By comparison with the CZ method for silicon substrates, SiC substrates are defective and require a high quality epitaxial layer due to underlying crystal defects such as, open-core screw dislocations (micro-pipes) per cm^2 and low angle boundaries. As a result, these substrates are 100 times more expensive than silicon substrates. Silicon carbide substrates are orientated between 3 to 8 degrees off-axis and have two terminated surfaces, silicon and carbon. In the Miller notation, which describes crystallographic directions in a unit cell, the silicon face is on the (0001) plane while the carbon face is on the $(000\bar{1})$ plane. The numbers in the parentheses represent the coordinates x, y, z, and c axes in the unit cell. The c-axis corresponds to the stacking direction. The fabrication of devices mostly occurs on the silicon face.

The basis of every SiC crystal comprises of a silicon atom surrounded by four carbon atoms forming a tetrahedral structure (see Figure 2.2). Likewise, each carbon atom bonds to four nearest-neighbor silicon atoms. The distance between a neighboring silicon or carbon atom is approximately 3.08 Å.

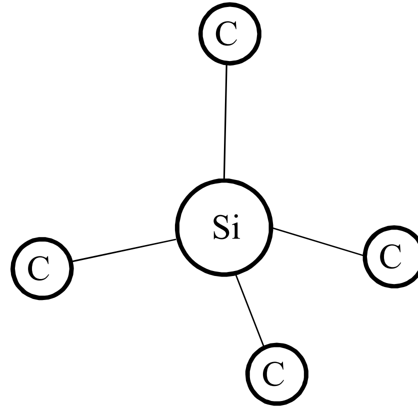


Figure 2.2: Four carbon atoms covalently bonded with a silicon atom [12].

Out of 200 SiC crystal systems, one of the commonly used SiC crystal geometries or polytypes for MOS-based power devices is 4H-SiC. This crystal geometry is depicted as 4H-SiC because it has a hexagonal crystal structure, whose repetitive stacking sequence of four layers of silicon-carbon atoms, is arranged as ABCBABCB to complete one unit cell. The position of A, B, and C each represent a layer of atoms. Figure 2.3 illustrates a 4H-SiC three-dimensional lattice structure [13].

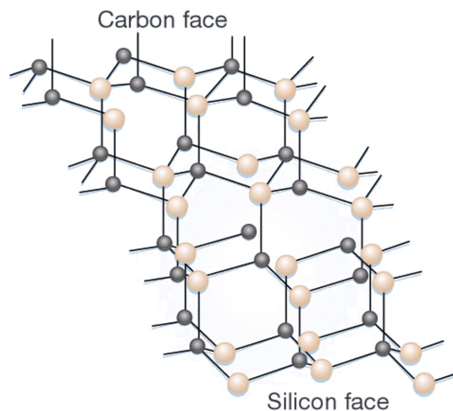


Figure 2.3: A 4H-SiC three-dimensional lattice structure [13].

The 4H-SiC substrates used for this study were 8^0 off-axis and were doped with nitrogen. Nitrogen impurities in the crystal lattice depicted that its conduction type was n-type because of the addition of negative charge carriers. Table 2.1 lists the properties of 4H-SiC and Si. These properties make 4H-SiC substrates attractive candidates for power switching devices.

Table 2.1: Properties of 4H-SiC and Si at room temperature (300K) [14-16].

Crystal Structure	4H-SiC	Si
Band gap Energy (eV)	3.25	1.12
Instrinsic Carrier Concentration (cm^{-3})	$2x10^{-8}$	$1x10^{10}$
Breakdown Field (V/cm)	$1.5\text{-}4x10^6$	$3\text{-}4x10^5$
Bulk Electron Mobility (cm^2/Vs) ($\perp$ to c-axis) (‖ toc-axis)	 ~1050 ~800	~1350
Thermal Conductivity	3.3	1.5
Saturation Velocity (cm/s)	$2.2x10^{-7}$	$1x10^{-7}$
Lattice Constant (Å)	a=3.073 c=10.05	a=5.43

As seen in Table 2.1, the critical breakdown field of 4H-SiC is an order of magnitude higher than silicon, making it conducive for high power blocking or switching in power devices. These properties continue to make this binary semiconductor a promising candidate for power devices due to its capability to block high voltages, switch at high frequencies, and operate at high temperatures.

2.2.1. Silicon Carbide (SiC) Oxidation Theory

The two types of oxidation growth method used in this study were atmospheric thermal oxidation and afterglow oxidation. An overview of the oxide growth kinetics on SiC is presented. Silicon carbide is the only binary compound semiconductor whose native oxide is silicon dioxide (SiO_2). Similar to oxidation of Si, thermal oxidation of SiC can be either in dry O_2, pyrogenic H_2O, or both. The growth kinetics of SiO_2 on SiC is not the same as on Si due to the presence of carbon atoms. The oxidation growth rate on SiC is an order of magnitude slower than Si under the same conditions [17-22]. One reason attributed to this phenomenon is the oxidation of carbon. Based on the model for the oxidation of Si, the model for the oxidation of SiC is expressed as [17]

$$X^2 + AX = B(t+\tau) \tag{2.1}$$

$$A = \frac{1 + \frac{1.5K_f}{h_{O_2}} + \frac{K_r}{h_{CO}}}{\frac{1.5K_f}{D_{O_2}} + \frac{K_r}{D_{CO}}} \tag{2.2}$$

$$B = \frac{K_f C^*_{O_2} - K_r C^*_{CO}}{N_0\left(\frac{1.5K_f}{D_{O_2}} + \frac{K_r}{D_{CO}}\right)} \tag{2.3}$$

where X is the oxide thickness, t is the oxidation time, τ is the initial thickness, B is a parabolic rate constant, B/A is a linear rate constant, K_f is the rate constant of the forward reaction, K_r is the rate constant of the reverse reaction, O_2 is oxygen, CO is carbon monoxide, h is the gas-phase transport coefficient, D is the diffusion coefficient, C^* is the equilibrium concentration, and N_0 is the number of oxidant molecules incorporated into a

unit volume of the oxide layer. Table 2.2 lists the chemical reactions at the SiC interface during the growth of a dry thermal oxide.

Table 2.2: Chemical reactions during dry thermal oxidation of SiC [20].

Sequence	Chemical Reaction
Primary	$\left\{ \begin{matrix} SiC + \frac{3}{2}O_2 \leftrightarrow SiO_2 + CO \\ SiC + O_2 \leftrightarrow SiO_2 + C \end{matrix} \right\}$
Secondary	$\left\{ \begin{matrix} SiC + 2CO \leftrightarrow 3C + SiO_2 \\ 2C + O_2 \leftrightarrow 2CO \end{matrix} \right\}$

From the chemical reactions, the oxidized carbon is out-diffused in the form of a gas. The amount of carbon remaining in the oxide, as a result of incomplete carbon oxidation, leads to the accumulation of carbon or carbon clusters at the SiO_2/SiC interface. These clusters form a density of interface states or traps near the interface [23]. Other reported sources of traps near the interface are due to carbon or silicon interstitials and stable carbon pairs [21].

The four most cited types of charges associated with SiO_2/Si systems and more so in SiO_2/SiC systems are fixed oxide charge (Q_f), mobile oxide charge (Q_m), oxide trapped charge (Q_{ot}), and interface trapped charge (Q_{it}). Figure 2.4 illustrates the location of these charges after a thermal oxidation of Si [24].

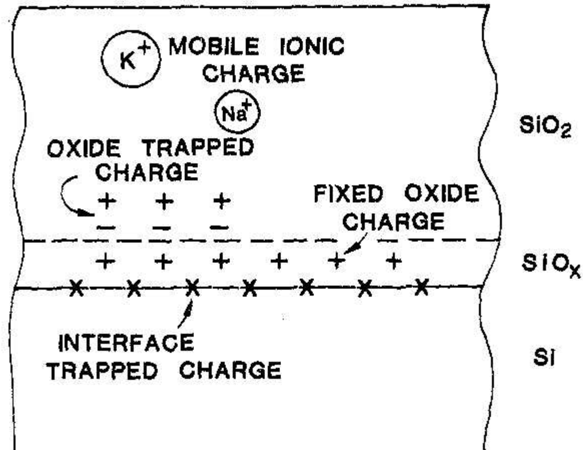


Figure 2.4: Location of oxide charges after a thermal oxidation of Si [24].

The reduction and control of these charges are done typically by a post-oxidation anneal. A hydrogen anneal at 450^0C, on an oxide grown on Si, reduced the density of interface states (D_{it}) from above $10^{11}/cm^2$ eV to $10^{10}/cm^2$ eV [14]. Contrary to SiO_2/Si systems, this anneal does not reduce D_{it} at the SiO_2/SiC interface. Proposed anneals to decrease oxide charges in SiO_2/SiC systems are Argon (Ar) anneal, Nitric oxide (NO) anneal, Nitrous oxide (N_2O) anneal, Ammonia (NH_3) anneal, or Re-oxidation (Re-ox) anneal. The reduction of D_{it} at the SiO_2/SiC interface remains an ongoing challenge.

2.3. Current Ramp Test and Voltage Ramp Test

Current and voltage ramp test techniques enable a quick assessment of the integrity of a gate oxide [25-27]. These tests are used to analyze an oxide under a range of electric fields to reveal intrinsic or extrinsic failures. When a critical charge density is reached, observed as a spike in the current, the oxide is no longer able to sustain its insulating properties. The electric field in the oxide cannot be directly measured. It can

be calculated from the voltage drop across the oxide (V_{ox}) divided by the oxide thickness (t_{ox}) (see equation 2.4).

$$E_{ox} = \frac{V_{ox}}{t_{ox}} \tag{2.4}$$

Both of these techniques reveal how the current conduction in an oxide over a range of electric fields can provide information about the charge-to-breakdown (Q_{bd}), the breakdown voltage (V_{bd}), and the time-to-breakdown (T_{bd}).

The main disadvantage using such techniques is the inability to establish the potential defect mechanism leading to the breakdown of the oxide. In the following sections, other techniques, such as constant current stress (CCS), constant voltage stress (CVS), time dependent dielectric breakdown (TDDB), and stress induced leakage current (SILC), are standard measurements used to examine the defect mechanisms leading to oxide breakdown. These device-based measurement methods are described with the intention of applying similar technique principles for the investigation of oxides on 4H-SiC wafers using non-contact Corona-Kelvin metrology.

2.4. Conduction Mechanisms of Dielectric-Semiconductor System

In this research study, oxides greater than 80 Å were stressed using a constant corona current to induce an electric field, greater than 5 MV/cm, in the oxide. In this field range, the current may conduct as Fowler-Nordheim emission or Poole-Frenkel emission.

2.4.1. Poole-Frenkel Conduction

In 1938, Poole-Frenkel conduction, named after Horace H. Poole and Yakov Frenkel, is a process due to the field-enhanced thermal ionization of electrons from charged or neutral traps. Therefore, the current flow is due to the contribution of traps in the bulk of the dielectric [28]. The Poole-Frenkel plot is defined as $\ln(J_{pf}/E)$ versus $\sqrt{E}$, where the current density (J_{pf}), based on the Boltzmann approximation, is given by [29]

$$J_{pf} = CE\exp\left(\frac{-q\left(\Phi - \sqrt{qE/\pi\varepsilon_0\varepsilon_r}\right)}{\xi kT}\right) \tag{2.5}$$

where Φ is the ionization potential in eV of the Coulombic traps in the oxide, C is the proportionality constant related to the density of the trap centers, k is Boltzmann's constant, T is the temperature, ξ is the factor, which varies between one and two depending on the relative concentration of acceptor traps (1) or donor traps (2) within the oxide, ε_0 is the permittivity of vacuum, ε_r is the dielectric constant, q is the electronic charge, and E is the electric field in the dielectric. The ionization potential is the energy required for a trap charge to overcome the influence of the trapping center in the absence of an electric field. The Poole-Frenkel plot yields a straight line and is expressed as [29]

$$\ln\left(\frac{J_{pf}}{E}\right) = \left(\frac{\sqrt{q^3/\pi\varepsilon_0\varepsilon_r}}{\xi kT}\right)\sqrt{E} + \left(\ln C - \frac{q\Phi}{\xi kT}\right) \tag{2.6}$$

The slope of this line is used to assess whether or not the dielectric conduction was due to Poole-Frenkel.

For a SiO_2/Si system, the Poole-Frenkel current density was calculated based on an ionization potential of 1 eV, ξ of 1, and a proportionality constant of $1x10^{-13}$. These parameters were reported values in literature for silicon dioxide [29].

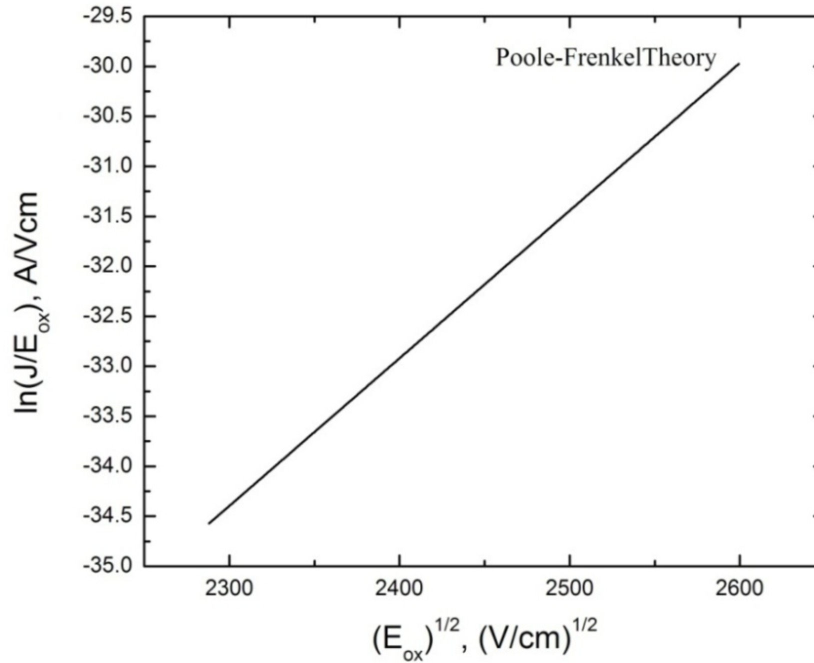


Figure 2.5: Example of Poole-Frenkel plot for SiO_2 on Si.

Based on these parameters, the slope of this line is 0.015 (see Figure 2.5). According to Equation 2.6, this slope decreases if there are less acceptor traps within the oxide (ξ=2) to 0.0074. In this study, the slope was the only parameter used to check the occurrence of Poole-Frenkel conduction in an experimental oxide.

2.4.2. Fowler-Nordheim Conduction

In 1928, Sir Ralph Fowler and Lothar W. Nordheim introduced a theory to explain field emission from a metal into vacuum. The Fowler-Nordheim current density characteristic, based on the free-electron gas model and tunneling probability by the Wentzel-Kramers-Brillouin (WKB) approximation method, was related to the electric field at the surface of an emitter. This current density was expressed as [30]

$$J_{fn} = \left(AF^2\right)\left(\frac{1}{t^2(y)}\right)\left(\frac{\pi ckT}{\sin(\pi ckT)}\right)\exp\left(\frac{-B(v(y))}{F}\right) \tag{2.7}$$

$$A = \frac{q^3}{8\pi h\Phi} \tag{2.8}$$

$$B = \frac{8\pi\sqrt{2m(\Phi^3)}}{3hq} \tag{2.9}$$

$$c = \frac{4\pi(t(y))\sqrt{2m\Phi}}{hqF} \tag{2.10}$$

where h is Planck's constant, q is the electronic charge, F is the electric field, Φ is the barrier height, m is the free-electron mass, t(y) and v(y) are correction factors, k is Boltzmann's constant, and T is the temperature. The correction factors, t(y) and v(y), rendered the image potential rounding effect on the top of the barrier [30, 31]. Forty years later, the Fowler-Nordheim equation was modified for emission from a metal into silicon oxide. Fowler-Nordheim conduction occurs when electrons tunnel from the semiconductor conduction band into the oxide conduction band, through the deformation of the potential barrier at the oxide-semiconductor interface. As the applied voltage

across the oxide exceeds the semiconductor electron affinity, the potential barrier changes from an impenetrable rectangular barrier to a penetrable triangular barrier [32]. Figure 2.6 illustrates this phenomenon with an energy band diagram of a MOS device.

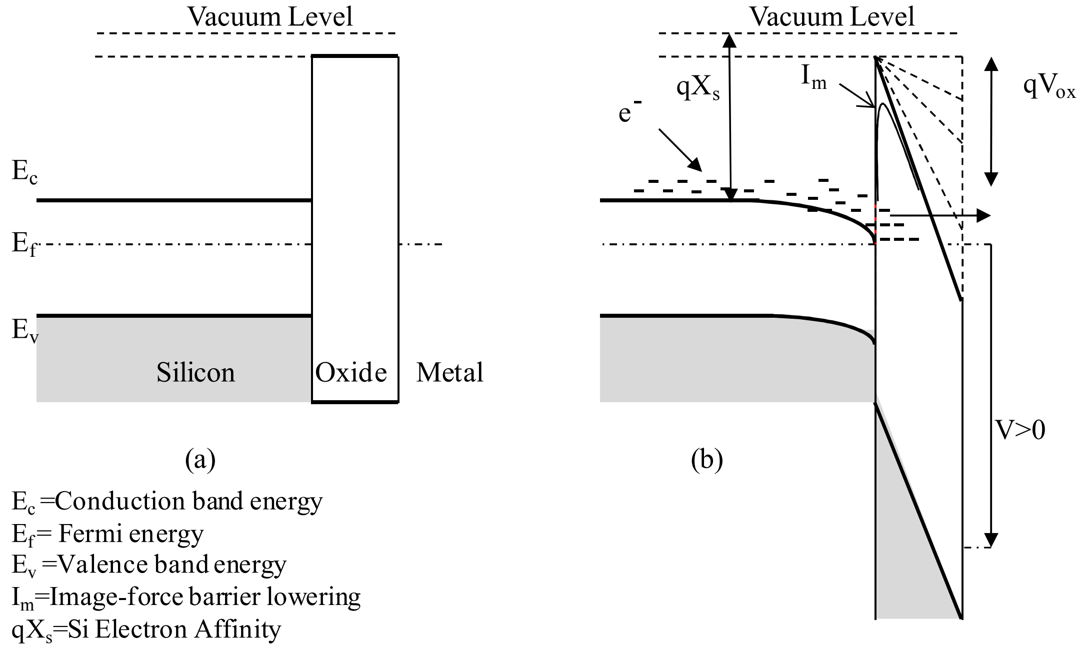


Figure 2.6: Energy band diagrams depicting a MOS device without stress (a) and under Fowler-Nordheim tunneling (b).

The semiconductor electron affinity potential (eV) is defined as the potential difference between the vacuum level and the bottom of the conduction band [33]. Based on photoemission measurements, the electron affinity for Si is given as 4.05 eV [16] and 4H-SiC is given as 3.62 eV [15].

In the modified Fowler-Nordheim equation, the free electron mass (m) was replaced by the effective mass of an electron in the oxide band gap (m_{ox}). Coefficients A, B, and c were modified from Equation 2.8 to 2.10 as [34]

$$A = \frac{q^3 m}{8\pi h \phi_b m_{ox}} \quad (2.11)$$

$$B = \frac{8\pi\sqrt{2m_{ox}(\phi_b^3)}}{3qh} \quad (2.12)$$

$$c = \frac{4\pi(t(y))\sqrt{2m_{ox}\phi_b}}{qhE_{ox}} \quad (2.13)$$

where E_{ox} is the electric field in the oxide (defined by Equation 2.4) and ϕ_b is the effective barrier height. This effective barrier height "takes into account barrier height lowering and quantization of electrons at the semiconductor surface" [33]. Internal electron photoemission is a standard measurement method used to determine the band offset of a semiconductor-dielectric interface. Using photoemission measurements, it was reported that the effective barrier height represented the conduction band offset in an oxide-semiconductor system [34]. Unless otherwise noted, the electric field in the oxide for the Fowler-Nordheim plot is represented as E throughout the document. The Fowler-Nordheim plot is defined as $\ln(J/E^2)$ versus $(1/E)$, which yields a straight line expressed as

$$\ln\left(\frac{J}{E^2}\right) = -B\left(\frac{1}{E}\right) + \ln(A) \quad (2.14)$$

The slope of this line corresponds to negative B and the intercept of the line is equal to the natural log of A. From the Fowler-Nordheim plot, the effective mass in the oxide and the effective barrier height are obtained by simultaneously solving Equation 2.11 and 2.12. An example of a Fowler-Nordheim plot is shown by Figure 2.7.

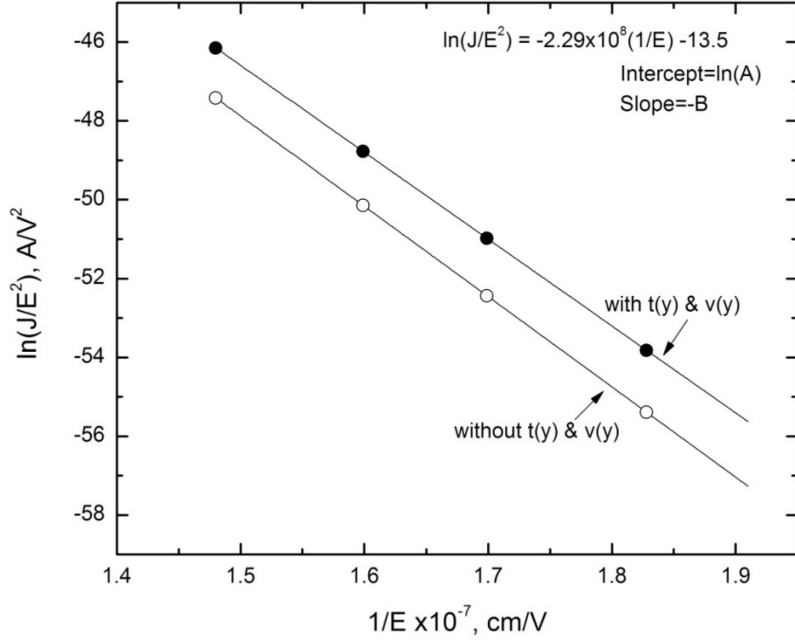


Figure 2.7: An example of a Fowler-Nordheim plot.

In Figure 2.7, the image force barrier lowering effects on the current density led to a parallel shift of the line resulting in slightly higher values of J/E^2.

The modified Fowler-Nordheim equation was simplified further, when the low temperature approximation was used and the image-force barrier lowering was ignored (because of its negligible effect on the tunneling distance (see Figure 2.7)) to [33, 35]

$$J_{FN} = \left(1.54x10^{-6}\left(\frac{m}{m_{ox}\phi_b}\right)E_{ox}^2\right)\exp\left(\frac{-6.83x10^{-7}\sqrt{\left(m_{ox}/m\right)\phi_b^3}}{E_{ox}}\right) \tag{2.15}$$

For an ideal case, Equation 2.15 assumed that charges trapped in the oxide were negligible. It was also derived under the following conditions: "the electrons in the emitting electrode can be described by a free Fermi gas; electrons in the oxide have a single effective mass (m_{ox}); and the tunneling probability is derived by taking into account the component of the electron momentum normal to the interface only" [33, 35]. The ratio of m_{ox}/m is represented as M_{ox} throughout the remainder of the document. Table 2.3 shows a few commonly used effective mass in the oxide, (M_{ox}), reported for Si-based MOS devices using either a Franz or parabolic dispersion relation.

Table 2.3: Commonly used effective oxide mass for Fowler-Nordheim calculations.

Reference	Effective Mass in the Oxide (M_{ox})	Effective Barrier Height
[36]	0.36	3.15 eV
[34]	0.42	3.25 eV
[35]	0.50	2.9 eV

These values may change based on a particular oxidation process. In this instance, the effective barrier height and M_{ox} calculated from the experimental Fowler-Nordheim plot, for a lightly nitride oxide on Si, was 3.05 eV and 0.38, respectively [37].

Non-contact Corona-Kelvin metrology, used to obtain Fowler-Nordheim characteristics for an un-metallized gate oxide on Si, was first pioneered by R. Williams and M. Woods in 1973 [38]. The fundamental principles of this metrology will be described in Section 2.8. The measured current density (J_{exp}) was expressed as [39, 40]

$$J_{\exp} = -(\varepsilon_0 \varepsilon_r) \frac{dE_{ox}(t)}{dt} \tag{2.16}$$

$$E_{ox}(t) = \frac{V(t) - V_o}{t_{ox}} \tag{2.17}$$

where ε_0 is the permittivity of vacuum and ε_r is the dielectric constant, V(t) is the surface voltage decay data following the cessation of corona charge, and V_0 is the potential difference between the Kelvin-probe and the oxide, prior to corona charge deposition. Equation 2.15 and Equation 2.16 were combined and the solution was given as [39, 40]

$$\frac{1}{E_{ox}} = \frac{1}{B} \ln \frac{AB}{\varepsilon_{ox}} (t + t_o) \tag{2.18}$$

$$t_o = \frac{1}{AB} \exp\left(\frac{B}{E_0} \right) \tag{2.19}$$

where E_0 is the initial field for the time after the cessation of corona charges. The Fowler-Nordheim plot was defined as $\log(t+t_o)$ versus $1/E_{ox}$, which was analogous to $\ln(J/E^2)$ versus $(1/E)$. The electric field in the oxide was calculated based on Equation 2.4. Any presence of oxide charges in the oxide was observed by a shift between the C-V curves taken before and after Fowler-Nordheim current stress. Fowler-Nordheim characteristic for un-metallized oxide thicknesses ranging from 500 Å to 2600 Å on Si was reported to have a barrier height of 2.9 eV and M_{ox} of 0.48 [39]. These values are comparable to Si-based MOS devices (see Table 2.3).

2.5. Constant Current Stress Technique

Constant current stress (CCS) test is also known as a current limited or compliance-limited stress test method [10]. It is a measurement technique where a predetermined density of coulombs per second is applied to the oxide until the gate voltage, measured as a function of time, drops abruptly. This abrupt voltage drop is indicative of oxide breakdown (see Figure 2.8). In CCS testing, the current flowing through the oxide is by Fowler-Nordheim conduction. During CCS, the electric field is adjusted to achieve the desired current stress factor. The power supply raises or lowers the voltage drop across the device to maintain the desired current. As the flux of charges increases, the electric field in the oxide increases and these charges may or may not become trapped within the oxide. The generation rate of trapped charges is assumed to be constant as this is related to the supplied current. Subsequently, the continuous formation of trapped charges forms a conductive path leading to oxide breakdown.

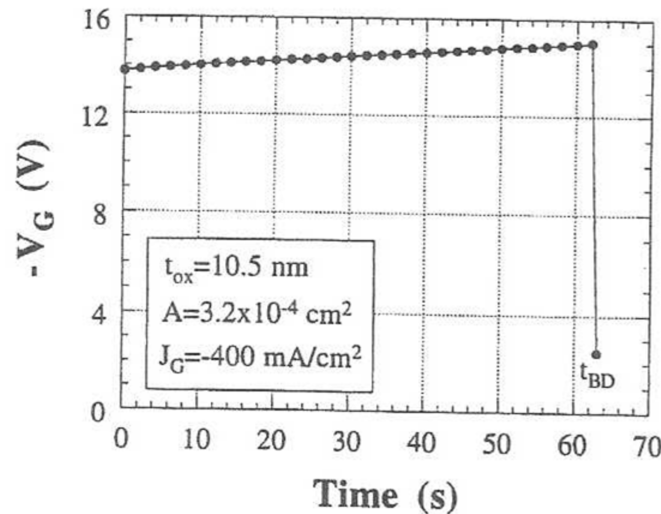


Figure 2.8: An example of a gate voltage-time characteristic of a MOS device obtained by CCS testing [33].

In Figure 2.8, the device sustained an oxide field greater than 13 MV/cm for one minute until reaching an oxide breakdown at 15 MV/cm. The oxide breakdown mechanism during CCS testing is related to an impact ionization process and trap creation process [41, 42].

Impact ionization is a process where point defects in the oxide are caused by trapped holes recombining with free electrons injected either from the substrate or the gate. Unlike impact ionization, trap creation is a process where electrons with energies greater than 2 eV liberate hydrogenous species, such as atomic hydrogen radicals, from the substrate. These species may cause interface traps or oxide traps at or near the SiO_2/Si interface [43]. Non-contact CCS testing was also performed on oxidized Si substrates with the intention to achieve oxide breakdown. This result will be discussed in Chapter 4. Another electrical stress test used to predict the lifetime of an oxide is known as time dependent dielectric breakdown (TDDB).

2.6. Time Dependent Dielectric Breakdown (TDDB)

Time dependent dielectric breakdown (TDDB) technique applies either a constant current or voltage stress to a gate oxide at a given temperature and monitors the time it takes for the oxide to breakdown. Elevated temperatures are used to accelerate testing as a means to quickly induce device failure. A gate oxide failure is defined when it surpasses a predefined leakage current limit or drops below a predefined voltage [33]. Using the TDDB technique, percolation and other physical models were developed to postulate the defect mechanisms leading to oxide breakdown.

Fundamentally, all models are based on the concept that a critical defect density leads to oxide breakdown [8, 9, 43-45]. Other models relating the electric field in the oxide to the time-to-breakdown with temperature were also developed [3, 46].

Constant voltage stress (CVS) test is a measurement technique where a constant potential is applied to a MOS device and the gate current is measured as a function of time. The power supply adjusts the current to maintain a constant electric field in the oxide. The breakdown mechanism is similar to a CCS test. In a typical CVS test, a series of capacitors are tested simultaneously using contact probes on a grounded measurement chuck. As each gate oxide is stressed, defects are created at localized areas within the oxide. The time it takes for each capacitor to electrically short or fail is monitored and either the first detectable or final breakdown is recorded. The reliability of the gate oxide is then evaluated by plotting the cumulative probability versus time-to-failure or time-to-breakdown for each group of capacitors. The Weibull distribution, which predicts the reliability of a product and models the failure rate, is commonly used for TDDB statistical data acquisition. The cumulative failure probability in the Weibull distribution for oxide breakdown is described as [45]

$$F(x) = 1 - e^{(-x/\alpha)^{\beta}} \tag{2.20}$$

$$W \equiv \ln(-\ln(1-F)) \tag{2.21}$$

where F is the cumulative failure probability, x is charge or time, α is the charge or time where 63.2% of the samples failed, β is the slope parameter, and W is the Weibit or

Weibull parameter. The Weibull cumulative distribution F(x) for various slope values is plotted in Figure 2.9 [47].

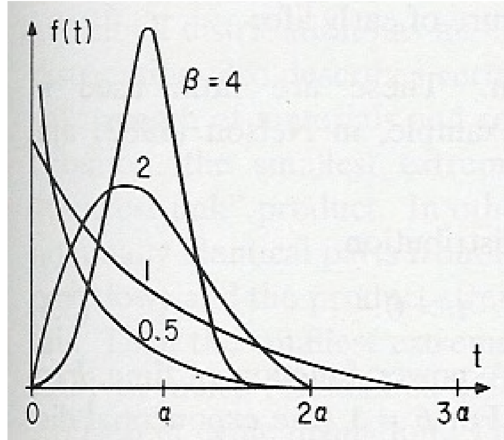


Figure 2.9: Weibull cumulative distribution for a population fraction failing by time [47].

This slope parameter is obtained by plotting the Weibit versus ln(x). Plotting the log of the time-to-breakdown versus the applied electric field in the oxide also yields the constant, β, which is referred to as the "electric-field acceleration factor", since this factor is proportional to $1/E_{ox}^2$ [46].

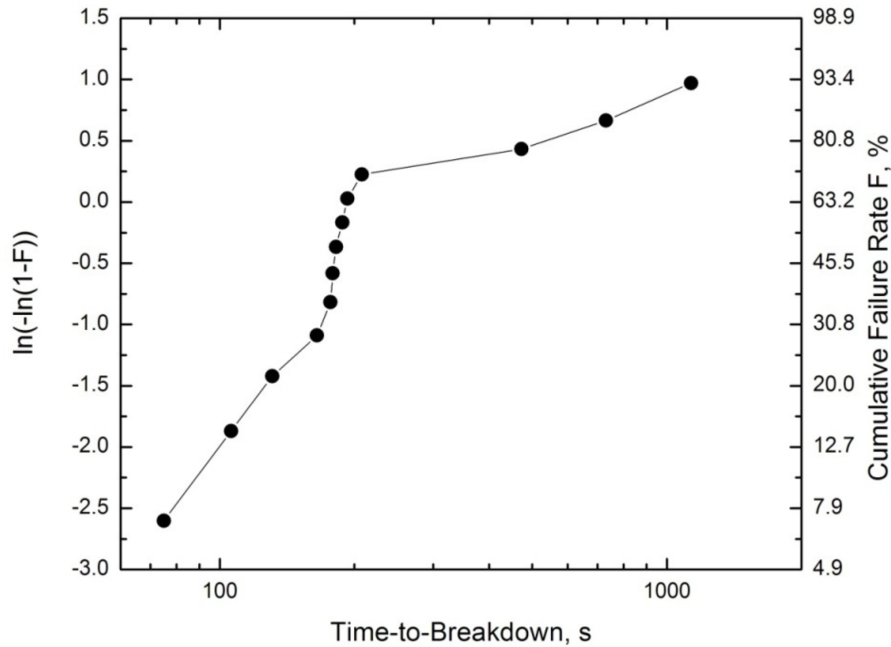


Figure 2.10: An example of a Weibull plot [48].

Figure 2.10 illustrates a TDDB distribution for thirteen 100 μm diameter MOS capacitors tested at a constant voltage stress of 37 volts at 250^0C [48]. A straight line represents that the devices had a similar breakdown mechanism. The "kink" and "bend" on the curve is usually interpreted as the occurrence of a different breakdown mechanism. In Figure 2.10, there are two bends in the curve, one at 31% and the other at 72%. Early failures in the first group, below 20%, were probably due to extrinsic failures. In the second group, from 25% to 70%, another type of failure mode occurred. The last group lasted for a longer time and failed with a different type of failure mechanism. Reliability engineers isolate the type of failure modes and rectify the first two types of failures. The goal is to have the capacitors sustain longer time durations to shift the distribution to the right.

To characterize the defect density for all oxide thicknesses, stress times, and electric fields, an equation fitted on the Eyring formulation was defined by [3]

$$N_T = 1.5x10^{21} \exp\left(\frac{-0.32 + 0.012E}{kTf\left(t/_{t_o} \right)} \right) \quad (2.22)$$

where kT is the thermal energy in eV, and $f(t/t_o)$ is the normalized time dependence of the trap generation. The reported gate oxide breakdown mechanism in SiC-based n-type MOS or nMOS devices after TDDB testing is as follows:

1. After testing 48 nMOS capacitors at room temperature, the slope of the Weibull distribution plot of the charge-to-breakdown indicated that the oxide breakdown was due to either wafer properties, such as the epitaxial surface roughness and metal impurities, or intrinsic failures. [49]
2. Two breakdown modes, edge breakdown and dislocation-related breakdown, were reported after testing 120 4H-SiC-based nMOS capacitors at room temperature. Oxide degradation was found to be caused by the dislocation defect density. [50]
3. After testing 40 6H-SiC based nMOS capacitors at 145^0C-305^0C, the TDDB results revealed a high field acceleration factor at fields greater than 7 MV/cm. The oxide was reliable if the electric field in the oxide was kept below 5 MV/cm at 150^0C. The temperature was found to be inversely proportional to the oxide reliability. The oxide breakdown mechanism was due to intrinsic failures. [51]
4. After testing 4H-SiC nMOS capacitors and double implanted MOSFETs at 200^0C, TDDB results showed that the failure mechanism varied at oxide fields

above 6 MV/cm due to current tunneling or impact ionization. After TDDB testing, it was also confirmed, through the use of electron-beam-induced current (EBIC) measurement, that the oxide breakdown mechanism was not due to the epitaxial SiC film defects under the oxide as reported in 1 and 2. Further analysis is ongoing to identify the defects responsible for oxide breakdown. [52]

In this research study, seventeen sites were measured on various oxide surfaces by SILC testing to obtain similar statistical analysis. The normal or Gaussian distribution function was used to assess the data distribution because of the short time durations used for this analysis. The function depicting the population fraction failing by a given parameter, such as time or voltage, is given as [47]

$$F(y) = \int_{-\infty}^{y} (2\pi\sigma^{2})^{-0.5} \exp\left(\frac{-1}{2}\right)\left(\frac{y-\mu}{\sigma}\right)^{2} dy \tag{2.23}$$

where μ is the population mean, σ is the population standard deviation, and y is the parameter causing failure, i.e. voltage. A normal cumulative distribution function plot is illustrated in Figure 2.11 [47].

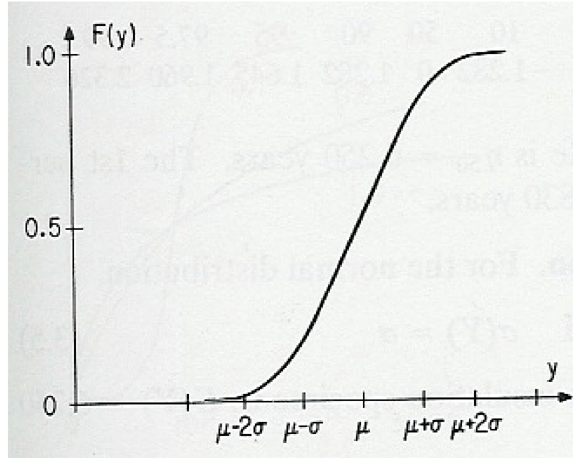


Figure 2.11: A normal cumulative distribution function for a population failing by y [47].

The experimental data set was sorted in ascending order before the probability graph was plotted. The formula used to generate the plotting position is expressed as

$$P_i = 100 \times \left(\frac{i}{n+1} \right) \tag{2.24}$$

where P_i is the percent cumulative probability, i is the number of measured sites (1,2,3,…etc.), and n is the test sample size. The distribution results will be shown in Section 4.6.

2.7. Contact Stress Induced Leakage Current (SILC) Technique

Contact stress induced leakage current (SILC) is referenced in this study as the technique tested with MOS devices. Stress induced leakage current is defined as the increase of oxide leakage current after high field stress compared with the current prior to stress. It encompasses time dependent components, such as transient and steady-state components [53, 54] and is usually observed at electric fields between 4 to 8 MV/cm [33]. The conduction in oxide thicknesses greater than or equal to 50 Å at these fields is

commonly due to Fowler-Nordheim current characteristics. As previously mentioned, Fowler-Nordheim tunneling occurs when electrons tunnel from the semiconductor conduction band into the oxide conduction band through a triangular barrier at the oxide-semiconductor interface. Stressing the oxide, beyond the Fowler-Nordheim tunneling regime, generates defects in the oxide. As a result, the current flows through the oxide by trap-assisted tunneling [3, 6, 54-58]. It is widely known that as an oxide degrades, under electrical stress, local defects or traps generated within the oxide structure create an increase in the current density, which lead to “thermal runaway” [3].

Figure 2.12 illustrates an energy band diagram of an nMOS device during SILC. In this tunneling regime, generated trapped charge sites, containing neutral electron traps, act as “stepping stones” for tunneling carriers, thereby assisting more current leakage to flow through the oxide [53].

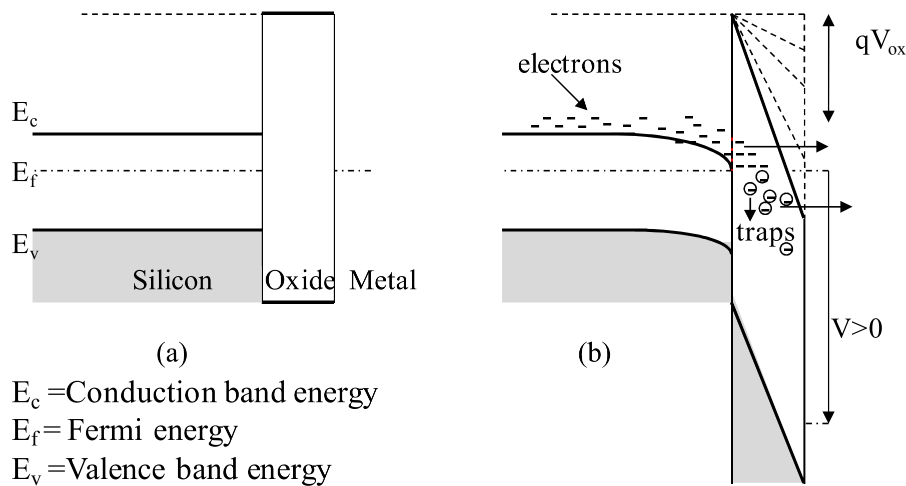


Figure 2.12: A sketch illustrating an nMOS (a) without stress and (b) after SILC.

These defects represent electron traps, interface traps, positively charge donor like states, or neutral electron traps [11, 45]. Neutral traps may be positively or negatively charged by acquiring a hole or an electron, respectively. This type of SILC has been classified as type-A SILC, trap-to-trap tunneling or trap-assisted tunneling (TAT) [3]. There are three modes of SILC: type-A, type-B, and type-C. The conduction mechanism for B-mode SILC occurs after partial breakdown, while the conduction mechanism for C-mode SILC occurs after final breakdown. An example of these three SILC modes is illustrated in Figure 2.13 [3].

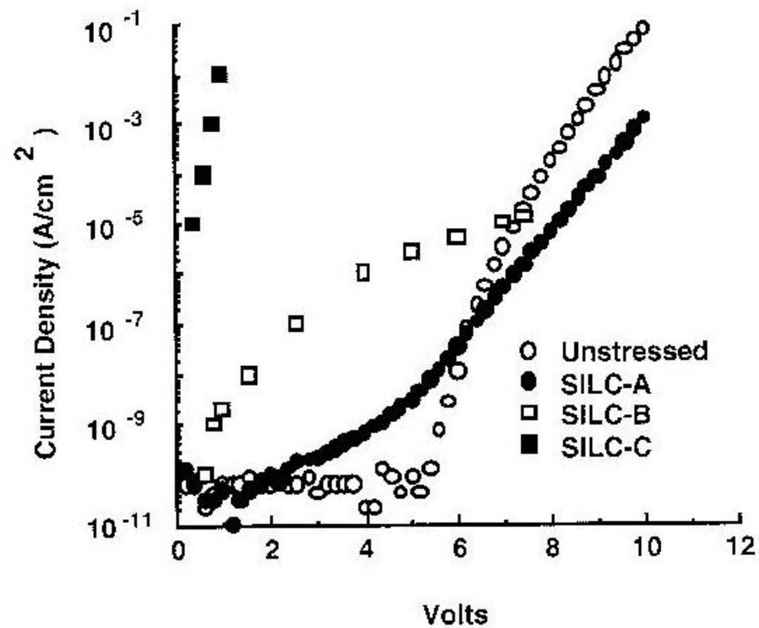


Figure 2.13: An example of SILC modes [3].

Based on various annealing kinetics after SILC measurements and charge-to-breakdown measurements performed on MOSFETs, the type of trap generation from SILC was reported to differ from the traps created by charge-to-breakdown [59]. Out of the three

SILC modes, A-mode SILC will be investigated in this research using non-contact SILC testing. This is because the current injected in the oxide did not lead to hard breakdown.

2.8. Non-Contact Stress Induced Leakage Current (SILC) Technique

Non-contact stress induced leakage current testing characterizes an oxide in the absence of fabricated devices. The definition of SILC remains the same as in contact SILC. The fundamental principle for this metrology will be discussed in the following sections.

2.8.1. Corona-Kelvin Metrology

Early in the 1970s, non-contact Corona-Kelvin metrology was introduced to investigate thermal oxides grown on silicon substrates in the absence of a metal or doped poly-silicon gate [60]. Fowler-Nordheim tunneling characteristics on oxide thicknesses greater than 500 Å were examined using corona ions. These ionic charges were deposited on the surface of the oxide for a given amount of time. After the cessation of charge, the contact potential difference (V_{cpd}) at the surface of the oxide was monitored and recorded based on the Kelvin method.

Corona ions, generated from air, are formed by applying a high DC voltage (kV) to a discharge electrode. The composition of these ions is dependent on the environmental air condition, such as the relative humidity. A positive voltage creates positive corona charges which may either be composed of $H^+(H_2O)_n$ ions [61] or $[H_3O]^+(H_2O)_n$ ions[62]. A negative voltage creates negative corona ions composed of $CO_3^-(H_2O)_n$, $O_2^-(H_2O)_n$,or O^- [61, 63].

Depending on the voltage polarity, these ionic charges generate an electric field in the oxide when they are deposited on the oxide surface. They are removed from the oxide surface by rinsing the substrate with de-ionized (D.I.) water or neutralized by depositing the opposite ionic polarity [60].

The technique of the Corona-Kelvin method utilizes a Kelvin probe to determine the contact potential difference (V_{cpd}) at the surface of the oxide after the deposition of corona ions. The probe consists of a 2-4 mm diameter metal plate referred to as the reference electrode. It is connected to a lock-in amplifier and other relevant electronics for noise to signal enhancement (see Figure 2.14). The distance between the probe and the surface of the oxide is nominally less than a fraction of a millimeter.

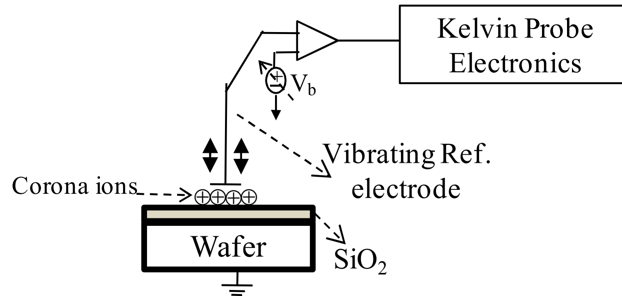


Figure 2.14: A sketch of Kelvin probe measurement.

The probe vibrates vertically at a low frequency to induce an alternating current (J_{ac}) through the circuitry. This current is defined as

$$J_{ac} = (V_b + V_{cpd})C_o \sin(\omega t) \tag{2.25}$$

where V_b is a DC bias voltage and C_o is the capacitance between the substrate and the reference electrode. To extract V_{cpd} from Equation 2.25, the DC bias voltage is varied to

null the electric field, created between the electrode and the substrate. The contact potential difference (V_{cpd}) is then determined when the DC bias voltage renders the displacement current to zero. At this instance, the bias voltage value is equal to V_{cpd}. The contact potential difference is expressed as

$$V_{cpd} = -V_b = \phi_{ms} + V_{ox} + V_{sb} \tag{2.26}$$

where ϕ_{ms} is the semiconductor-reference electrode work function difference, V_{ox} is the voltage drop across the oxide, and V_{sb} is the voltage drop across the surface barrier or space charge region.

The use of ions generated by corona discharge followed by measuring the contact potential difference at the oxide surface was classified as Corona Oxide Characterization of Semiconductor (COCOS) metrology in the late 1990s [5, 64-67]. The integrity of thin oxides on Si has been investigated using this measurement approach [68, 69]. Commercial tools using this metrology for whole wafer characterization are manufactured by Semiconductor Diagnostics, Inc. (SDI), Tampa, Florida [70]. Characterization parameters include acquiring the flat band voltage, interface trap density, total dielectric charge, SILC value, and the capacitance of an as-grown oxide film [69, 71]. Biasing the surface of the oxide with corona charges is the fundamental criterion to perform non-contact capacitance-voltage (C-V) measurements and current-voltage (I-V) measurements.

2.8.2. Capacitance-Voltage Measurements

Capacitance-voltage (C-V) measurements detect the influence of interface trap charges and other charge defects within the oxide. In addition, C-V measurements are used to determine other characteristics of the oxide such as the oxide thickness, the oxide breakdown field, the work function difference between the semiconductor and the gate electrode, and the oxide conductivity [72]. Capacitance-voltage plots characterize the total capacitance of an oxide-semiconductor system within four ideal regions of operation: accumulation, flat band, depletion, and inversion regions. For a low frequency (<1kHz) measurement, these regions are defined as follows [73]

1. Accumulation: the concentration of majority carriers near the oxide-semiconductor interface is larger than in the bulk of the semiconductor. The oxide capacitance (C_{ox}) is

$$C_{ox} = \frac{(\varepsilon_0 \varepsilon_r) A_g}{t_{ox}} \tag{2.27}$$

   where t_{ox} is the oxide thickness and A_g is the area of the gate.

2. Flat band: equilibrium state in the bulk of the semiconductor (no band bending). The flat band capacitance (C_{fb}) is

$$C_{fb} = \frac{C_{ox} C_s}{C_{ox} + C_s} \tag{2.28}$$

   where C_s is the semiconductor capacitance.

3. Depletion: the concentration of majority carriers near the oxide-semiconductor interface is smaller than in the bulk of the semiconductor. The capacitance (C) is

$$C = \frac{C_{ox} C_d}{C_{ox} + C_d} \tag{2.29}$$

where C_d is the depletion layer capacitance.

4. Inversion: the concentration of minority carriers exceeds the majority carriers near the oxide-semiconductor interface. The capacitance is equal to the oxide capacitance, C_{ox}.

If no oxide charges are present within the oxide, the flat band voltage is equal to the semiconductor-metal work function. In the presence of oxide charges, the flat band voltage is defined as [33]

$$V_{fb} = \phi_{ms} - \sum \frac{Q_{oxt}}{C_{ox}} \tag{2.30}$$

where Q_{oxt} includes the interface trapped charge, the fixed oxide charge, the oxide trapped charge, and the mobile oxide charge. Unlike Si-based MOS systems, SiC-based MOS systems at room temperature cannot form an inversion region due to the low thermal generation rate of minority carriers. One way this region can be formed is through the introduction of these carriers into the substrate by an ion implantation of a doped source region.

In the non-contact low frequency or quasi-static C-V method, a pulse of corona charge $Q_{c(n)}$ is deposited on the surface of the oxide. The semiconductor is placed into a region where the concentration of electrons near the oxide-semiconductor interface is larger than in the bulk of the semiconductor. This region is referred to as the accumulation region for an n-type semiconductor or the inversion region for a p-type

semiconductor. The deposited corona charges are imaged in the semiconductor's space charge region or surface barrier and in any traps in the oxide, which can exchange charge with the semiconductor [66]. The energy band diagram illustrating these charges, with respect to the reference electrode, is seen in Figure 2.15.

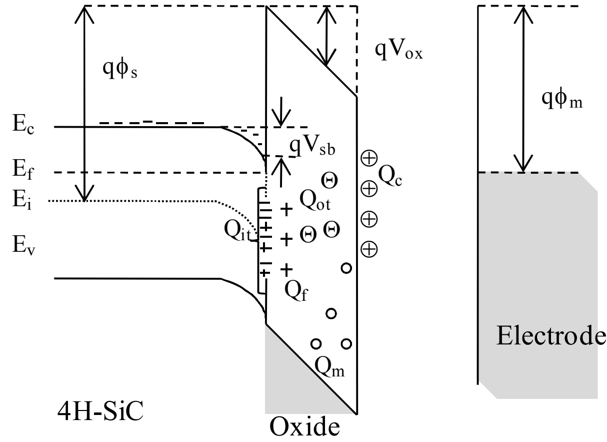


Figure 2.15: Energy band diagram after the deposition of corona charges.

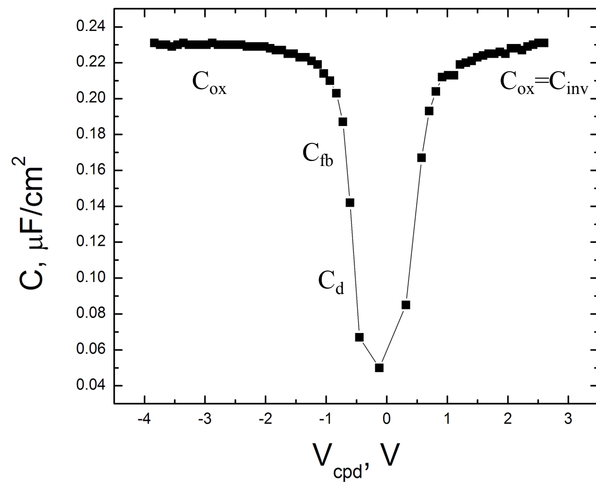
Immediately, after the deposition of corona charges on the surface of the oxide, a time varying contact potential difference $V_{cpd(n)}(t)$ is then measured (see Equation 2.26). This voltage is measured with a precision of 0.1 mV. Afterwards, series of corona charge quantities, $Q_{c(n+1)}$, are deposited on the surface of the oxide to slowly transition the semiconductor from accumulation to depletion to inversion. Each increment of charge is followed by the measurement of the contact potential difference as a function of time, $V_{cpd(n+1)}(t)$. The total capacitance, C_{tot}, is derived from

$$C_{tot} = \frac{dQ_c}{dV_{cpd}} = \frac{Q_{c(n)} - Q_{c(n-1)}}{V_{cpd(n)} - V_{cpd(n-1)}} \tag{2.31}$$

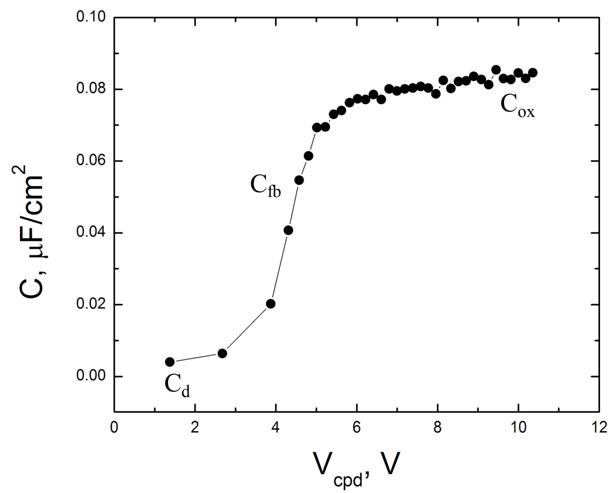
where n and n-1 represent the immediate and immediate past increments of charge application. In Equation 2.31, the change of the contact potential difference (ΔV_{cpd}) eliminates the contribution of ϕ_{ms} and is expressed as

$$\Delta V_{cpd} = \Delta V_{ox} + \Delta V_{SB} \tag{2.32}$$

Figure 2.16 shows an example of a non-contact C-V characteristic of a 150 Å thermal oxide on a p-type Si substrate and a 400 Å afterglow oxide on an n-type 4H-SiC substrate. These C-V characteristics were measured in the dark.



(a)



(b)

Figure 2.16: Non-contact C-V characteristics of (a) a 150 Å thermal oxide on a p-type Si and (b) a 400 Å afterglow oxide on an n-type 4H-SiC.

The most commonly used calibrated corona charge, deposited during C-V measurements, was 0.016 $\mu C/cm^2$. In Si, this density of charge does not damage the oxide [74].

2.8.3. Equivalent Oxide Thickness (EOT) Measurement

Capacitance-voltage characteristics of an oxide measured in either the dark or light was used to calculate its equivalent oxide thickness. The equivalent oxide thickness was determined in the region where the semiconductor was placed into accumulation. The C-V characteristic of the oxide, measured in light, is obtained with the same quantity of charge and step increments used in the dark. When the oxide is measured under illumination, the light generates excess electron-hole pairs in the semiconductor depletion layer or space charge region. As a result, the voltage drop across the surface barrier is minimized to a negligible value. When the oxide is measured in the dark, the voltage drop across the surface barrier is minimized to a negligible value in accumulation. In both cases, the oxide capacitance is accurately determined since the measured voltage is only taken across the oxide (see Equation 2.33).

$$C_{ox} = \left(\left(\frac{dQ_c}{dV_{cpd}} \right)_{dark} \right)_{acc} = \left(\left(\frac{dQ_c}{dV_{cpd}} \right)_{ill} \right)_{acc} \tag{2.33}$$

where C_{ox} is the oxide capacitance measured in the dark or light. The equivalent oxide thickness is then calculated, in reference to SiO_2, as

$$EOT = \frac{\varepsilon_r \varepsilon_o}{C_{ox}} \tag{2.34}$$

where ε_r is the dielectric constant and ε_0 is the permittivity of vacuum. The EOT can also be extracted from the slope of the deposited corona charge and the measured voltage drop across the oxide within the accumulation region.

Equation 2.34 is also referred to as the capacitance equivalent thickness (CET). It has been reported that EOT obtained for oxides grown on 4H-SiC substrates is comparable to Ellipsometer measurements [75]. Figure 2.17 illustrates a non-contact C-V measurement characteristic of a 499 Å afterglow oxide on an n-type 4H-SiC substrate measured in the dark and in the light, respectively.

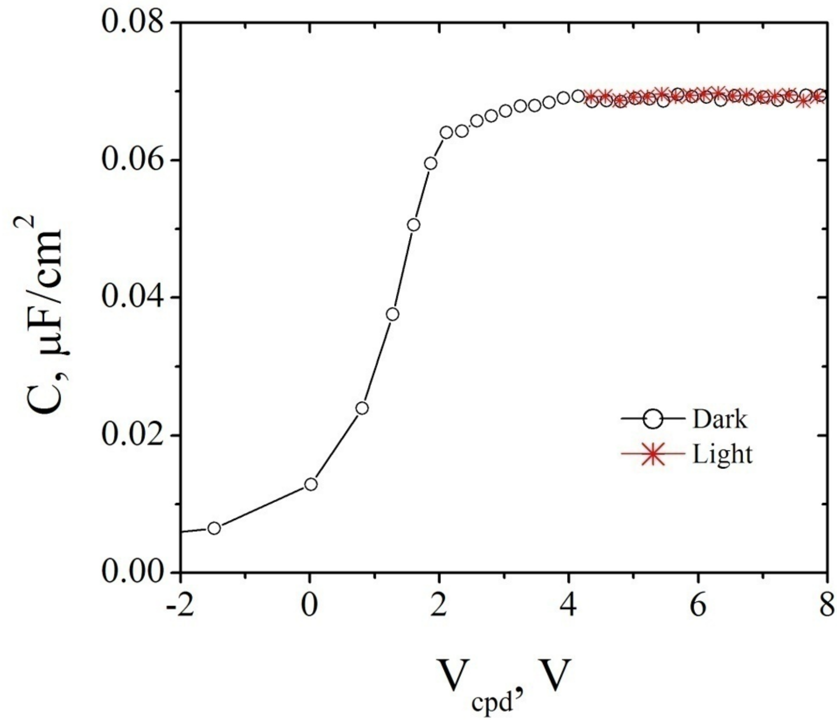


Figure 2.17: Non-contact C-V characteristic of a 499 Å afterglow oxide on an n-type 4H-SiC measured in the dark (circles) and in the light (asterisks).

In Figure 2.17, the C-V curve taken in the light does not deplete because of the excess minority carriers generated by the light.

2.8.4. Current-Voltage Measurements

Prior to non-contact current-voltage (I-V) measurement, a blanket of positive corona charge ($\sim 10^{-7}$ C/cm^2) is deposited over the entire surface of the oxide to minimize lateral charge spreading at a measurement site. Current-voltage measurements are performed under illumination to measure only the voltage drop across the oxide.

A quantity of corona ions is deposited on the surface of the oxide to generate an electric field in the oxide. As ionic charges buildup on the surface of the oxide, the oxide voltage increases linearly with time. The voltage drop across the oxide remains linear until the injection of electrons from the substrate occurs by Fowler-Nordheim tunneling. The onset of the Fowler-Nordheim voltage is equal to the conduction band offset voltage. As the flux of corona ions induces tunneling of electrons from the semiconductor into the oxide conduction band, the buildup of ionic charges on the surface of the oxide stops when the electron current density reaches the corona ionic current density, which is controlled by the power supply [64, 67].

After the cessation of charge, the corona charge decay is expressed as

$$\frac{dQ_c}{dt} = C\frac{dV_{cpd}}{dt} \qquad (2.35)$$

This condition is referred to as a Self-Adjusting Steady State (SASS) condition [65, 76]. The current density, J_{exp}, is calculated from the measured dielectric voltage decay given by

$$J_{\exp} = \left(\frac{\varepsilon_o \varepsilon_r}{t_{ox}}\right)\left(\frac{dV_{cpd}}{dt}\right)_{ill}. \quad (2.36)$$

Based on the classical non-contact Fowler-Nordheim analytical equation (see Equation 2.18), the oxide voltage decay was fitted to a logarithmic time dependence curve as shown in Equation 2.37.

$$\frac{dV_{ox}}{dt} = \left(\frac{dV_{cpd}}{dt}\right)_{ill} = \frac{-b_1}{(a_1 + b_1 \ln(t))^2 (t)} \quad (2.37)$$

where a_1 and b_1 are constants from the logarithmic curve fitting and are related to the Fowler-Nordheim coefficients, A and B. [39, 76]. An example of various oxide voltage decays with respect to a positive corona current density, in $\mu A/cm^2$, on Si is illustrated in Figure 2.18.

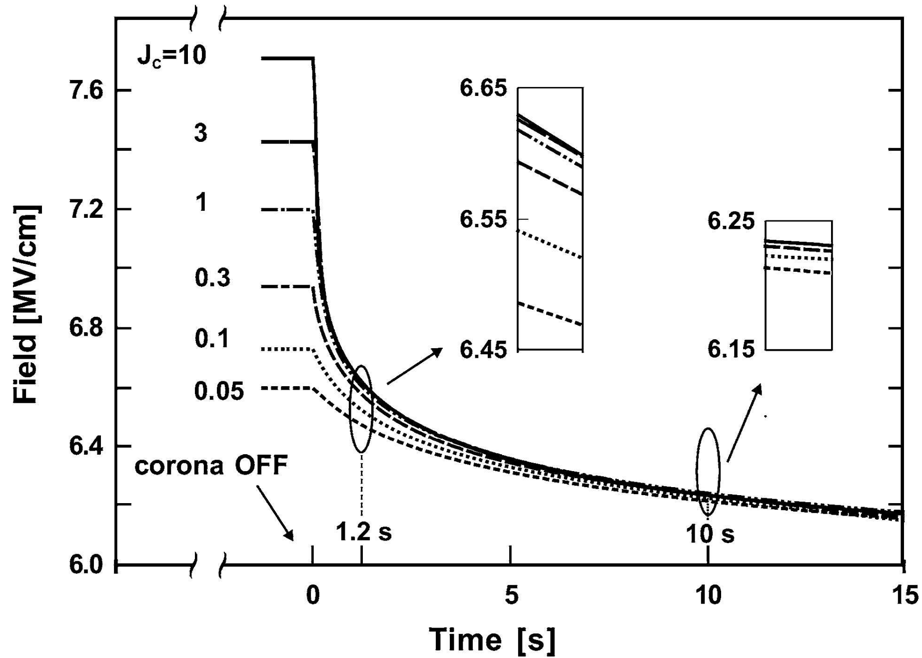


Figure 2.18: Oxide voltage decay after corona charging [76].

In Figure 2.18, the electric field in the oxide is proportional to the corona current density. For longer time durations, the precision of the SASS voltage increases. The electric field in the oxide can be calculated with further accuracy by including ϕ_{ms}

$$E_{ox} = \frac{\left(V_{cpd}\right)_{ill} - \phi_{ms}}{t_{ox}}. \tag{2.38}$$

In SiO_2/Si systems, holes injected from the Si valence band is negligible due to a higher potential barrier of 4.73 eV at the oxide-semiconductor valence band. Non-contact SILC testing is based on non-contact I-V measurement principles. Its methodology will be discussed in the next section.

2.8.5. Stress-Induced Leakage Current Method

A controlled ionic current is used to perform non-contact SILC testing. Before stressing the oxide to calculate SILC values, a sufficient quantity of corona charges is deposited for a few seconds to produce substrate injection of electrons. This quantity of charges induces an electric field in the oxide greater than 5 MV/cm. The contact potential difference is measured in a 20-second interval following a 5-second charge deposition. The calculated current density is fitted to a predicted Fowler-Nordheim current. It is assumed that this small charge fluence does not give rise to defects above the Fowler-Nordheim current. Fluence is defined as the product of the calibrated ionic current and the deposition time. It has units of coulombs per cm^2 (C/cm^2). After confirming that the experimental current was by Fowler-Nordheim conduction, the corona deposition time was increased. The oxide is stressed beyond the Fowler-

Nordheim tunneling regime and electron traps or defects are created within the oxide, as shown in Figure 2.19.

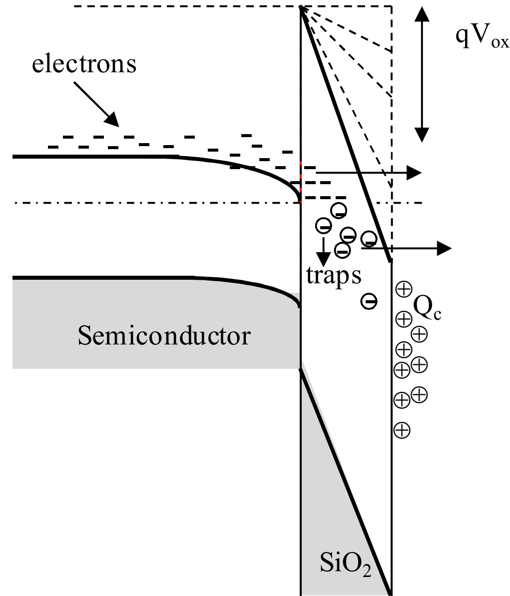


Figure 2.19: Energy-band diagram during non-contact SILC.

The voltage decay is monitored and the total experimental current density is calculated based on Equation 2.36. The total experimental current density (J_t) is expressed as

$$J_t = J_{SILC} - J_{F-N}. \tag{2.39}$$

In Equation 2.39, the component of the calculated current due to SILC is subtracted from the Fowler-Nordheim current. The SILC density is typically one or more orders of magnitude above the Fowler-Nordheim current. Therefore, the total calculated current is essentially equal to the SILC value. However, the thickness is not calculated from EOT but from the measured Fowler-Nordheim current after the 5-second charge deposition. Since the Fowler-Nordheim current density is dependent on the electric field in the oxide,

the current density versus the oxide electric field is plotted to determine the oxide thickness. The oxide thickness is adjusted to fit the theoretical Fowler-Nordheim current curve for a given oxide-semiconductor system. This thickness adjustment is accurate if the effective mass in the oxide and effective barrier height values are precisely known. The theoretical Fowler-Nordheim current curve is based on M_{ox} of 0.36 and an effective barrier height of 3.15 eV. These values are the default values for atmospheric thermal SiO_2/Si systems defined in the FAaST 230 tool's software. Figure 2.20 illustrates an example of this method for a thermal SiO_2/Si system.

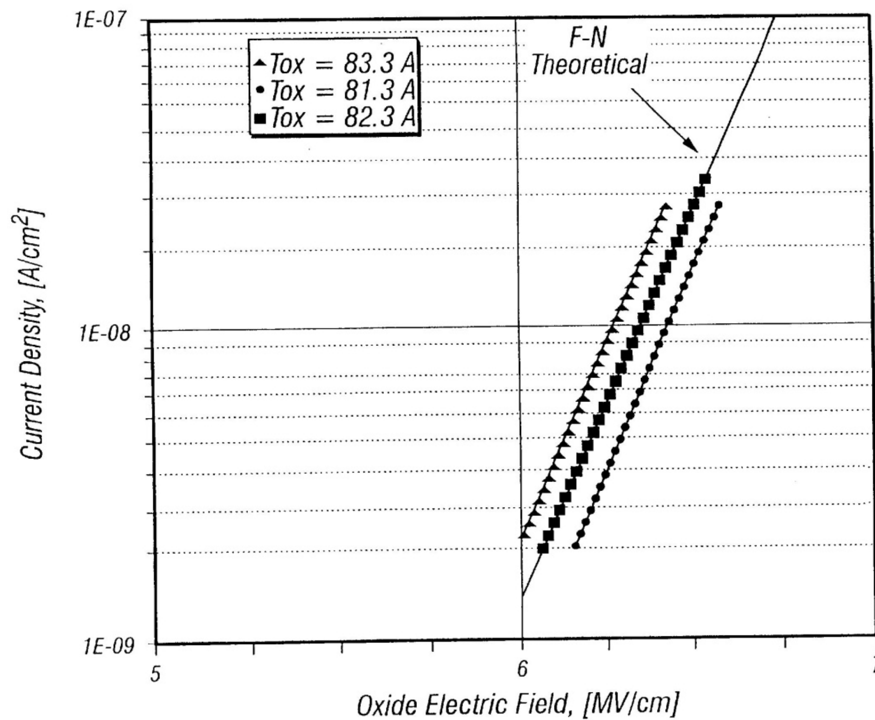


Figure 2.20: Example of determining thickness with the Fowler-Nordheim current density [64].

This determined thickness also matched the independently measured EOT value for this thermal oxide grown on a p-type Si wafer. Once the thickness is determined, SILC values are calculated. A constant oxide field value is then chosen to compare the SILC densities at their respective stress fluence. An increase in the density of the leakage current indicates a localized weak spot in the oxide structure, which may be susceptible to more defect formation. A weak spot maybe due to process contamination. Preliminary, non-contact SILC testing was first used to characterize two oxide growth methods, pyrogenic steam oxide and afterglow oxide, on n-type 4H-SiC substrates [77]. The results revealed that the afterglow oxide showed less susceptibility to defect formation at a field of 6 MV/cm and a charge fluence of 1.55 mC/cm^2.

2.9. Statistical Issues in Device-Based Measurements

Even though a new technique using dual voltage and time integration was developed to characterize long-term TDDB measurements [44], there exist two major disadvantages in obtaining TDDB distributions. First, it is time consuming when testing various voltages, currents, and temperatures. This data acquisition may take months or even years to report. Second, TDDB testing requires a large group of MOS devices to be tested consecutively to obtain statistical distributions. These distributions predict the lifetime of the oxide and the intrinsic or extrinsic mechanism responsible for breakdown. Statistical data acquisition of an oxidation process requires the correct mathematical expression for the time-to-breakdown (t_{bd}) or time-to failure (TF), which is dependent on the electric field induced in the oxide. Based on either the Anode Hole Injection model ((1/E)-model) or the Thermochemical model (E-model), the time-to-failure can be expressed as [3]

$$\text{E-model: } \ln(TF) \propto \frac{Q_1}{kT} - \gamma(E_{ox}) \tag{2.40}$$

$$\text{(1/E)-model: } \ln(TF) \propto \frac{Q_2}{kT} + G\left(\frac{1}{E_{ox}}\right) \tag{2.41}$$

where γ and G represent the field acceleration parameters in the two respective models, Q_1 is the thermal activation energy required for bond breakage, and Q_2 is the thermal activation energy associated with the current-induced hole injection into the oxide. Since the electric field cannot be directly measured using the current state-of-art metrology techniques, the accuracy of the voltage and thickness measurements are critical. Any errors in the thickness can lead to an erroneous field calculation (see Equation 2.4) resulting in an over or under estimation of the lifetime of the oxide. Probable causes of an oxide thickness error from a C-V measurement are: an incorrect value of the gate area and an incorrect dielectric constant value. The cost to predict the lifetime of an oxide grown on SiC can be expensive, as these substrates are more costly than Si substrates.

2.10. Chapter Summary

The reliability of an oxide can be assessed using electrical stress testing methods. The reported failure mechanisms of oxides for Si-based and SiC-based MOS devices, under high electric fields, were presented using TDDB measurements. An exact defect mechanism leading to the breakdown of an oxide for SiC-based MOS devices has not been reported. The conduction mechanisms, Fowler-Nordheim and Poole-Frenkel emission, were explained to analyze the conduction obtained in the experimental oxides

using non-contact SILC testing. The principle technique of non-contact C-V measurements and non-contact SILC testing were also introduced.

Chapter 3. Experimental Procedures

3.1. Non-Contact Instrumentation

The Ion-Drift (ID) Spectrometer tool and the Film Analysis and Substrate Testing (FAaST) 230 tool were the non-contact metrology tools utilized to investigate the oxide/4H-SiC interface. In the following section, a brief description of each tool will be presented.

3.1.1. Film Analysis and Substrate Testing (FAaST) 230 and Components

The commercial Film Analysis and Substrate Testing (FAaST) 230 tool was modified to investigate oxides grown on 4H-SiC substrates. One unique modification implemented to the tool was the use of a UV light (λ=375 nm) diode instead of a green light diode. The light generates free minority carriers to eliminate the surface barrier voltage drop across the 4H-SiC substrate's space charge layer. The components within the tool, which was utilized to perform non-contact C-V measurements and non-contact SILC measurements, are illustrated below.

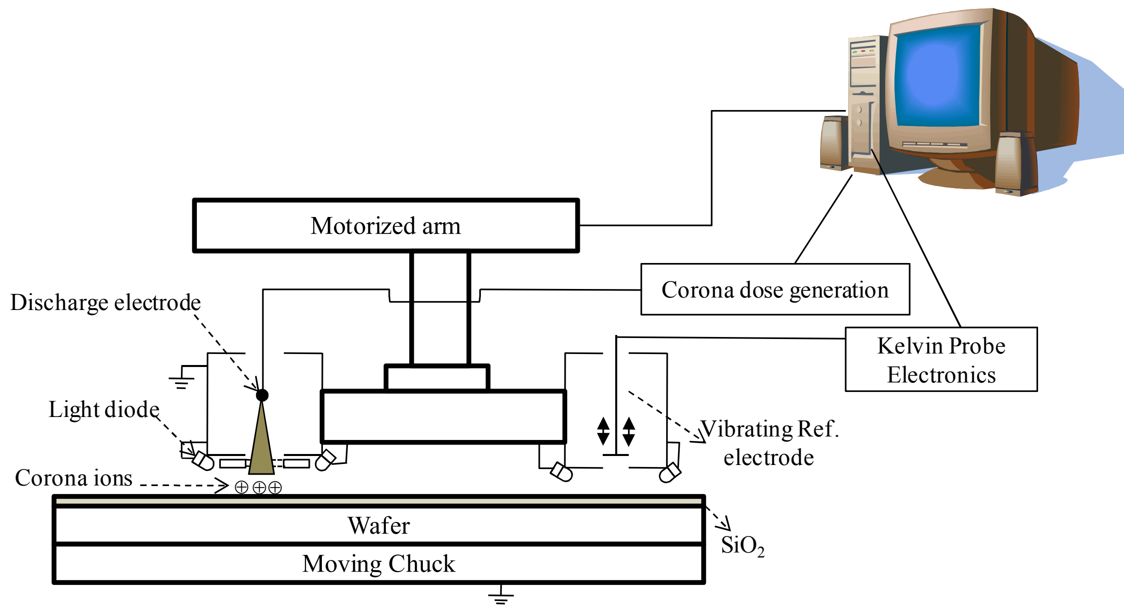


Figure 3.1: Schematic of the measurement apparatus based on ref. [64].

In Figure 3.1, the charging station located on the left comprised of a needle type corona discharge electrode and light diodes, and the measurement station located on the right included a Kelvin probe and light diodes. The probe consisted of a platinum reference electrode plate and the vibrating frequency was set to 1600 Hz. Within the corona dose generation modulation, a high DC voltage between $\pm$ 5 KV to $\pm$10 KV supplied the corona discharge electrode to create corona ions. The probe and the corona source were positioned about 500 μm above the oxide surface. The distance of the corona discharge electrode above the wafer was automatically controlled by the computer within a calibrated range to achieve the desired corona dose. The corona charge deposition on the dielectric surface was measured either by the instrument directly or calibrated. The density of the charge deposition was influenced by the level of the voltage, the charging time, the distance between the corona source and the oxide surface, and the charge interaction with any surface charges on the oxide [78]. The ion production could be set

from 10^{-7} to 10^{-4} A/cm^2. After the cessation of charge deposition, in less than a couple of seconds, the Kelvin probe determined the contact potential difference (V_{cpd}) at the deposition site with a precision of 0.1 mV (refer to section 2.8.1). The probe transfer to this site was achieved by a mechanical actuator. The voltage decay measurement acquisition was terminated after a predefined time.

The diodes were used to illuminate the oxide surface. As previously mentioned, when the dielectric is measured under illumination, the light generates excess electron-hole pairs in the semiconductor depletion or space charge layer, which minimized the voltage drop across the surface barrier to a negligible value. The change of the contact potential difference was equal to the change in the voltage drop across the oxide. Subsequently, the change in the voltage drop across the surface barrier was obtained by [66]

$$\Delta V_{sb} = \left(\Delta V_{cpd}\right)_{dark} - \left(\Delta V_{cpd}\right)_{ill} \tag{3.1}$$

$$\left(\Delta V_{cpd}\right)_{dark} = \Delta V_{sb} + \Delta V_{ox} \tag{3.2}$$

$$\left(\Delta V_{cpd}\right)_{ill} = \Delta V_{ox}. \tag{3.3}$$

For non-contact C-V measurements, the user input the desired charge value in units of q/cm^2 for a particular number of incremental steps. The software then calculated the necessary corona current and time needed to generate this charge density. On the contrary, for non-contact SILC measurements, the user input a value from ± 0.2 to ± 0.8 in the corona current parameter.

This parameter was proportional to the power supply and it directly produced a calibrated ionic corona current in the μA/cm^2 range. The corona deposition time was also entered by the user. The measurement cycle depended on the number of stress fluence (corona current multiplied by the deposition time) level(s) requested.

3.1.2. Ion-Drift Spectrometer

The Ion-Drift Spectrometer was an experimental tool based on the FAaST 230 tool's contact potential difference measurement principles. One of the major differences between this tool and the FAaST 230 tool was the corona discharge electrode. The corona source encompassed a wire discharge electrode and its enclosure (see Figure 3.2).

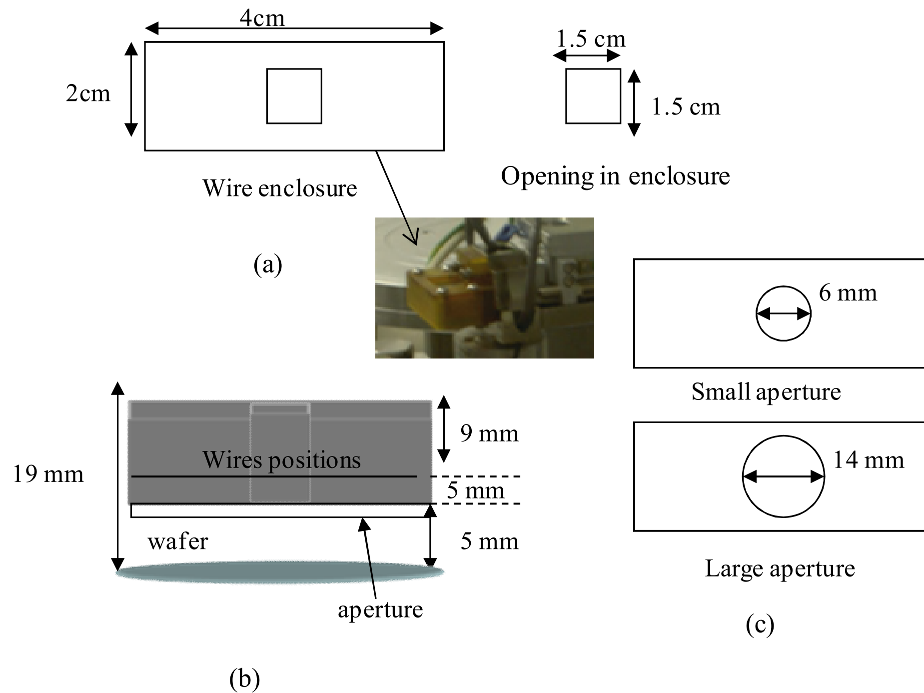


Figure 3.2: Sketch of the (a) wire enclosure, (b) discharge distance to the wafer, and (c) aperture diameter.

The opening at the top of the wire enclosure allowed air to flow into the enclosure so corona ions may be created. The diameter of the aperture's opening, which was placed at the bottom of the enclosure, controlled the amount of corona charges deposited on the oxide surface. The user interface was similar to the one used in the FAaST 230 tool for non-contact SILC measurements. The user input a value from $\pm$0.2 to $\pm$0.8 in the corona current parameter and the corona deposition time in seconds. This tool was used as a training tool for three purposes: 1. to understand the non-contact Corona-Kelvin measurement method; 2. to verify the current limitation from the corona source; and finally, 3. to indicate the influence of constant corona current stress on C-V measurements.

3.2. Pre-Oxidation Cleaning Procedure

Prior to oxidation, if the wafers were previously oxidized, the wafers were submerged in a (10:1) H_2O:HF solution for 5 minutes to remove the oxide. This was followed by de-ionized (D.I.) water rinse cycles and a (2:1) H_2SO_4:H_2O_2 or piranha clean for 10 minutes. The wafers were then rinsed and dipped in a (1:1) H_2O:HCL solution for 10 minutes and rinsed. Afterward, the wafers followed a standard cleaning procedure for bare silicon. Standard clean 1 (SC1) and standard clean 2 (SC2), developed by the Radio Corporation of America [79], removed organic and metallic surface contamination from the wafer. Figure 3.3 illustrates the RCA cleaning procedure used in this study.

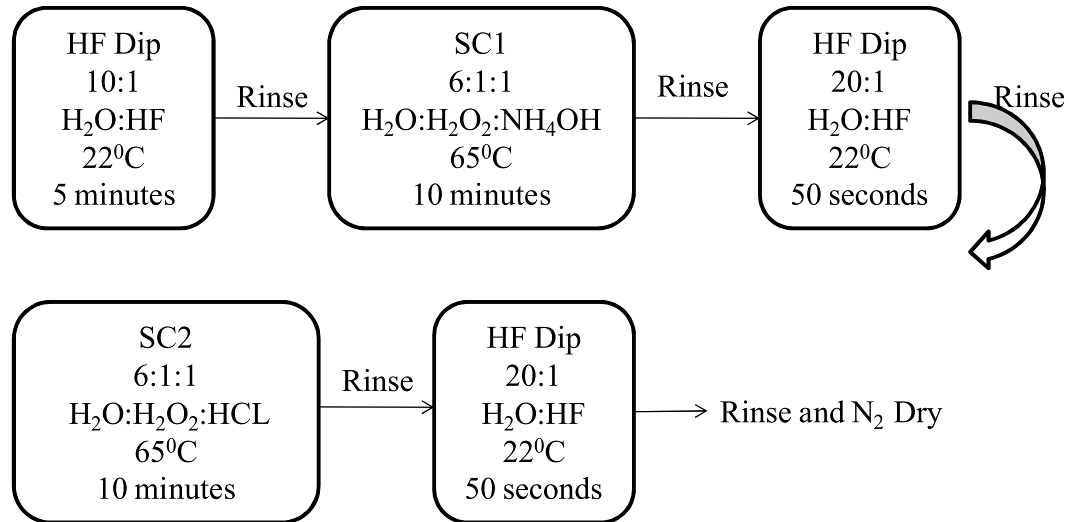


Figure 3.3: RCA cleaning procedure.

The D.I. water used for cleaning and rising had a resistivity of 18 Mohm-cm. The HF dip after SC1 and SC2 removed any thin layer of chemical oxide formed during the standard cleans. Subsequently, the wafers were oxidized using either an afterglow (AG) furnace system or an atmospheric furnace system.

3.3. Oxidation Sequence/Interval Experiments

The substrates used in this work were commercially available 8^0off-axis n-type 4H-SiC epitaxial wafers. These 3-inch wafers had an n-type epitaxial layer, grown on the (0001) Si face, with a nitrogen doping concentration of approximately $5x10^{15}/cm^3$. This concentration was determined by a non-contact doping profiling method [80]. These wafers were reused or recycled allowing substrate cost-savings to the project and the characterization of a variety of oxidation processes.

3.3.1. Brief Description of Afterglow (AG) Furnace

The afterglow (AG) or remote plasma vacuum furnace system has been shown to oxidize 4H-SiC at a lower oxidizing temperature, time, and pressure [75, 77] than possible for this material when compared to an atmospheric furnace system. The afterglow system is illustrated in Figure 3.4. Only the primary gas inlet was used. The gases available were Argon (Ar), Oxygen (O_2), Nitrous Oxide (N_2O), Nitrogen (N_2), and Forming gas (H_2:N_2). Forming gas (FG) was a mixture of 4-5% H_2: 96-95% N_2. A microwave plasma source generated neutral atomic and excited molecular species of O_2, N_2O, and FG. The furnace idle temperature and pressure in a N_2 ambient was 400^0C at 0.3 Torr. To load the wafers, the system was brought up to atmospheric conditions, where the wafers were centered in the growth zone of the furnace and placed under vacuum in a N_2 ambient.

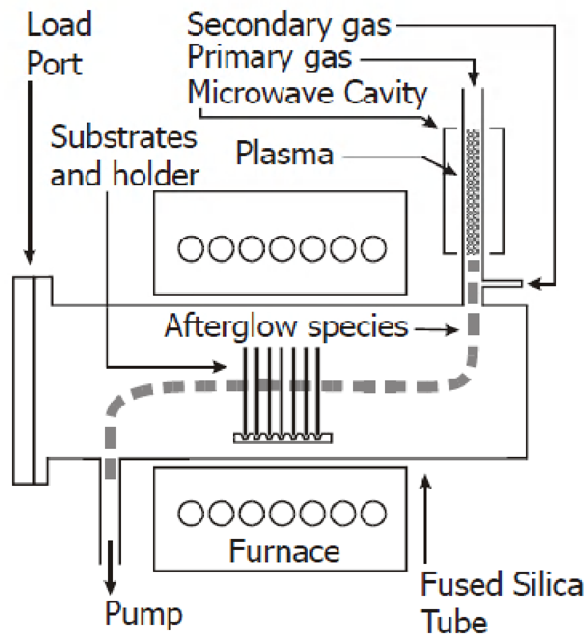


Figure 3.4: Sketch of afterglow furnace system [77].

In a non-excited media, the temperature was stabilized to the oxidation temperature. The standard oxidation was performed at 850^0C for 90 minutes at one Torr in the remote plasma excited mixture of O_2: N_2O: FG with a gas flow rate of (3: 0.2: 0.5) liters/minute. Following oxidation, the wafers were either annealed at a specific temperature and time in a non-excited media or unloaded. Argon was the standard gas used to stabilize the temperature either between anneals or prior to unloading. The wafers were then unloaded in a N_2 ambient at a specific temperature.

3.3.2. Afterglow (AG) Oxidation Parameter Variations

Thirteen afterglow oxide recipes were reported in this work. Three major measurement sequences will be presented along with their purpose. A detailed listing of each afterglow oxide recipe can be found in Appendix A. The oxidation parameter variations included surface pre-conditioning, oxidation time variation, and post-oxidation annealing.

The objective of the first stage in this study was to establish and verify the conduction mechanism of annealed and non-annealed oxides, under a high oxide field (greater than 5 MV/cm), as Fowler-Nordheim conduction. The annealed AG recipes were varied by the gas media mixture and temperature used for post-oxidation annealing (see Table 3.1). The post-oxidation anneals used for comparison were Argon (Ar) anneal, Re-oxidation (Re-ox) anneal, Oxygen-nitrous anneal, or Oxygen-FG anneal.

Table 3.1: Annealed afterglow (AG) recipes.

AG Anneal Recipe	Anneal Description	Duration Time (min)
I_A	Re-ox anneal	60
I_B	Re-ox anneal	25
II	Ar anneal	60
III	Re-ox and Ar anneal	120
IV	Oxygen-FG anneal	120
V	Re-ox anneal	360
VI	Oxygen-nitrous anneal	120

The AG oxides referred to as AG I_B, AG IV, AG V, and AG VI were modified in the following manner: in AG I_B, the oxidation time was reduced from 90 minutes to 40 minutes; and in AG IV, AG V, and AG VI, instead of Ar, the same anneal gas ambient was used to stabilize the temperature to the anneal temperature. These minor variations were included to observe the influence of growth thickness and anneal variation on the Fowler-Nordheim characteristics. The variation in the post-oxidation anneal was to verify the influence of charges in the oxide on the Fowler-Nordheim plot, since it was reported that the density of interface states is decreased by post-oxidation anneals [14]. Table 3.2 lists the modification within the non-annealed recipes.

Table 3.2: Non-annealed afterglow (AG) recipes.

Non-Annealed AG recipes	Modified Process	Unload Temperature
AGW I	N/A	600^0C
AGW II	No FG pre-treatment	600^0C
AGW III	10 minutes of oxidation	850^0C
AGW IV	No FG pretreatment and 10 minutes of oxidation	850^0C
AGW V	Oxidation mixture media	600^0C
AGW VI	Oxidation mixture media	600^0C

The influence of the surface pre-conditioning, the oxidation growth time, the variation of the oxidation mixture media, and the unloading temperature on the Fowler-Nordheim characteristics were observed for the non-annealed AG oxides. The measurement sequence is illustrated in Figure 3.5.

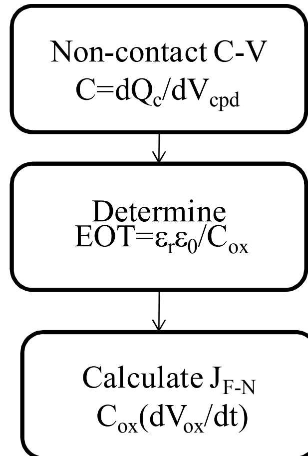


Figure 3.5: Measurement sequence to calculate J_{F-N}.

The results of the first stage prompted the objective for the second stage of measurements. In this stage, the trapped charge distribution within AG oxides was examined. The trapped charge distribution may exist in the bulk of the oxide or at the oxide interface. Afterglow IV oxide was the primary afterglow oxide process recipe used for this experiment. To perform this task, the oxidized substrates were etched in a diluted HF solution bath of 100:1 (H_2O:HF) at 24^0C. Figure 3.6 shows the etch pattern and quadrant created on a substrate.

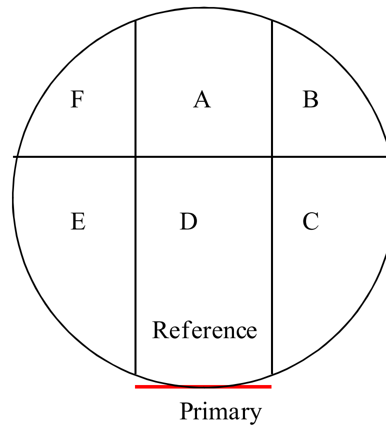


Figure 3.6: Etch pattern and quadrant designation on the substrate.

The wafers were then dehydrated using three methods: a hotplate at 200^0C for 5 to 60 minutes, a rapid thermal processing (RTP) anneal in Ar at 800^0C for 2 minutes, and an afterglow non-excited Ar anneal at 600^0C for 20 minutes. The measurement sequence is illustrated in Figure 3.7.

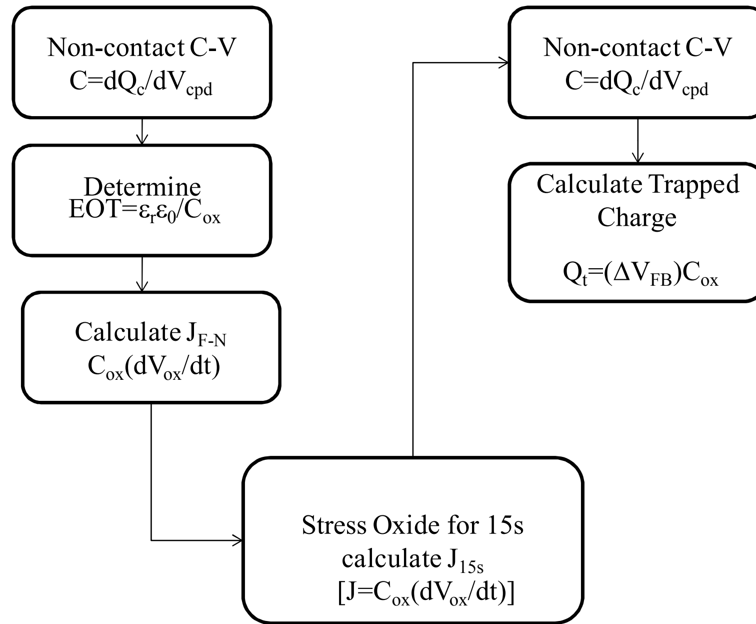


Figure 3.7: Measurement sequence to calculate trapped charge.

Finally, the objective for stage three was to analyze the potential breakdown mechanism and assess the growth oxide consistency using SILC testing at seventeen sites on the wafer. Afterglow recipes AGW I, AG I_A, AG II, and AG III were repeated at least three times on the same substrate. The influence of the environmental/processing conditions, which included unintentional contamination from the cleaning procedure or the furnace, was observed by the leakage current measurements. The measurement sequence is illustrated in Figure 3.8.

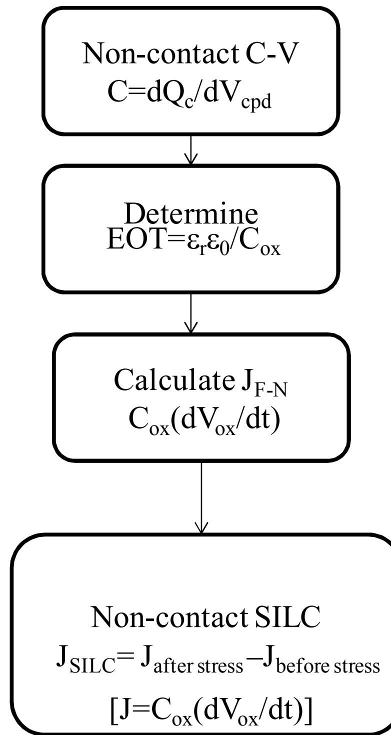


Figure 3.8: Measurement sequence to obtain SILC data acquisition.

3.3.3. Thermal Oxidation

To compare the AG oxides to atmospheric oxides, n-type 4H-SiC oxidized samples, Thermal TA and Thermal TB were obtained from two separate industrial laboratories. The oxide on these 3-inch diameter wafers were grown using an atmospheric furnace. Oxidation occurred at a temperature greater than 1100^0C followed by a nitric oxide (NO) anneal at a temperature not exceeding 1150^0C.

Chapter 4. Experimental Results and Discussion

4.1. Measurement Test Conditions

To ensure proper wafer backside contact with the measurement chuck, the oxide was stripped from the carbon face of each wafer using hydrofluoric (HF) vapor. Following the 5-minute HF vapor etch, the wafers were subjected to D.I. water rinse cycles and dried with a nitrogen air gun. Since the relative humidity (R.H.) affected the amount of corona discharge ions generated in air, all measurements performed on the FAaST 230 tool were taken at an R.H. level between 45% and 50%. The room temperature ranged from 19 to 20^0C. On the contrary, the Ion Drift Spectrometer was not in a controlled environment and as a result, the relative humidity and temperature was recorded for each measurement. Unless otherwise noted, the oxide field range, chosen to calculate the predicted Fowler-Nordheim characteristics, was based on the field range of the experimental data.

4.2. Non-Contact Corona Current Stress

Two sets of experiments were performed on the Ion-Drift Spectrometer: constant corona current stress and corona deposition time versus C-V characteristics. To have a known reference, thermal oxides on p-type (100) Si wafers were used for these sets of experiments. The objective of the first experiment was to determine the current limitation of the measurement tool.

Each oxide was stressed with negative corona charges until the current density (following such stress) reached between 10^{-6} A/cm^2 and 10^{-5} A/cm^2. Negative charges were used to place the semiconductor into accumulation to induce substrate injection of electrons. Two oxides, 320 Å and 365 Å thick, were stressed. The large aperture was chosen since more corona charges were deposited on the oxide surface. As shown in Figure 4.1, the current density range of 10^{-6} to 10^{-5} A/cm^2 was not achieved even though the electric field in the oxide was greater than 13 MV/cm. The electric field breakdown for silicon dioxide ranges from 10 to 14 MV/cm. Table 4.1 shows the measurement conditions and parameters.

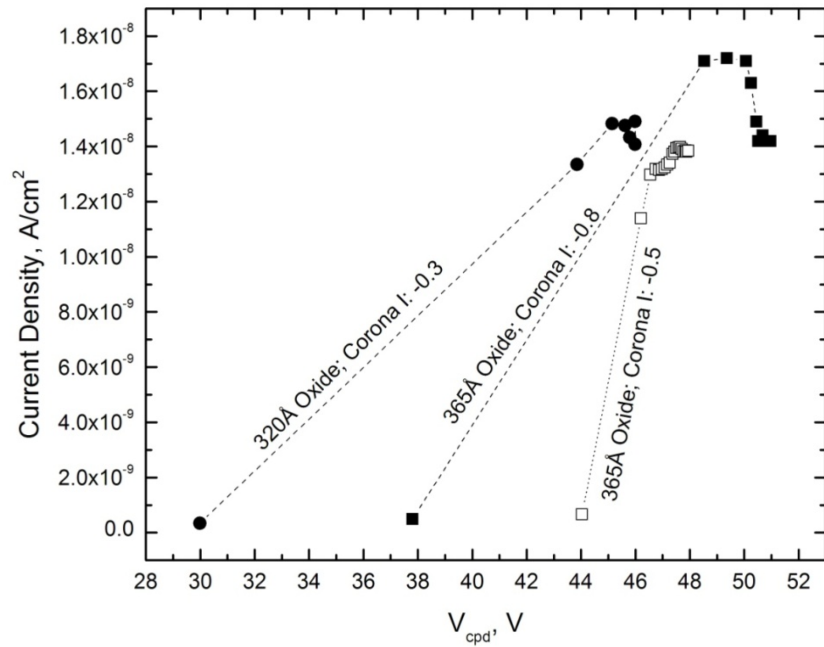


Figure 4.1: Current density versus V_{cpd} for various corona currents.

Table 4.1: Stress current measurement parameters and conditions.

Oxide Thickness (Å)	Room Temp (^{0}C); R.H. (%)	Corona Current Parameter	Corona Deposition Time (s)	Pulse Duration (s)	Oxide Electric Field (MV/cm)
320	23; 68	-0.3	15	105	14
365	25; 70	-0.8	3	57	13
365	24; 66	-0.5	10	110	14

Various corona currents and times were tested to obtain the desired breakdown field. As seen in Figure 4.1, the highest current density achieved was approximately 0.018 μA/cm^2. Even though more charges were deposited at the maximum current parameter, the voltage potential, along with the current density, leveled at a particular value. It was concluded that the corona source was current limited.

The objective of the second experiment was to observe the influence of the corona deposition time versus C-V characteristics. Using standard device based contact measurements, capacitance-voltage plots can be used to illustrate the influence of the interface trap density (see Figure 4.2).

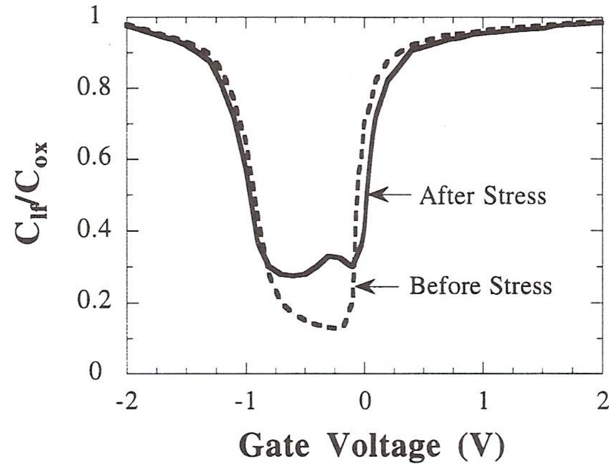


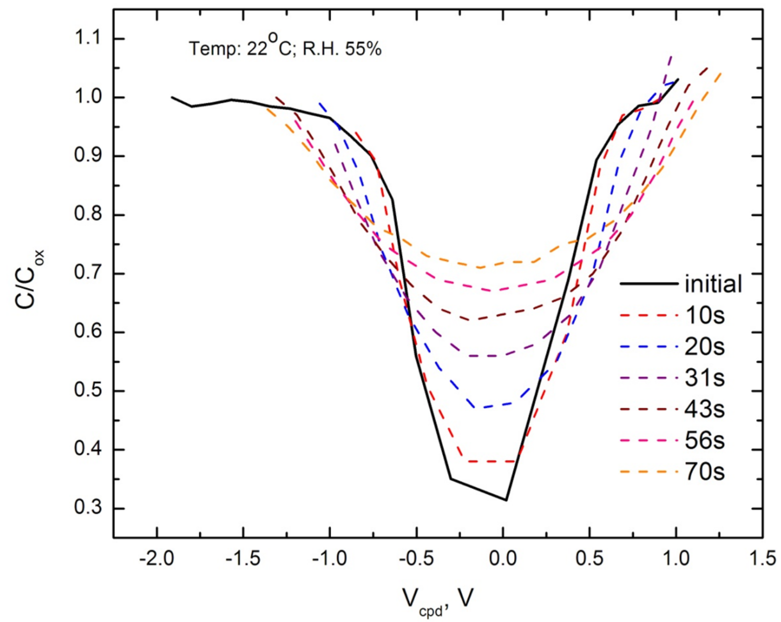
Figure 4.2: Theoretical ideal D_{it}=0 (before stress) and $D_{it} \neq 0$ (after stress) [33].

In Figure 4.2, the minimum capacitance increased as a result of the formation of interface trap defects. The same concept was predicted to occur once the oxide was stressed with corona ions. The measurement protocol included: 1. obtain the initial C-V, 2. stress the oxide using negative corona charges for 10s, and 3. re-measure the C-V. Step two was repeated for 10s, 11s, 12s, 13s, and 14s. The total cumulative time was 70s. Table 4.2 reiterates the measurement procedure.

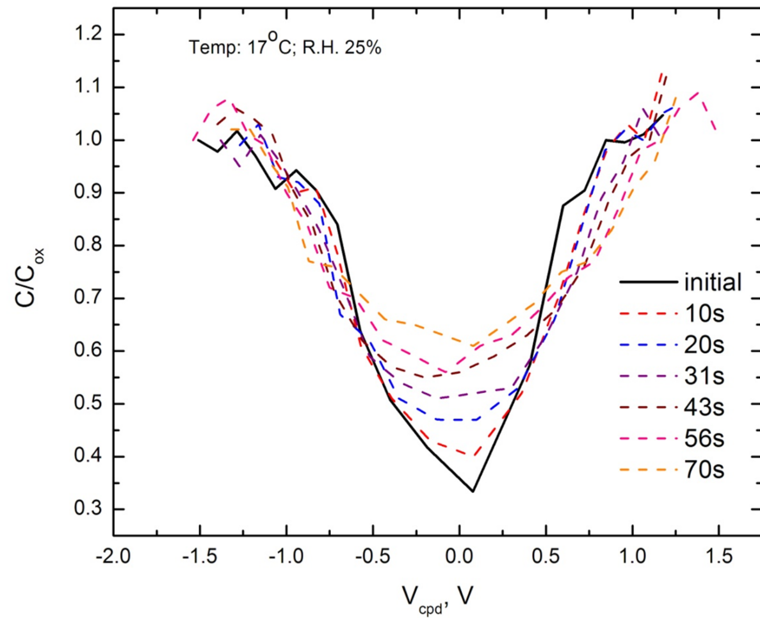
Table 4.2: Stress measurement protocol.

Measure	Time (s)	Cumulative Time (s)
C-V		
1st Stress	10	10
C-V		
2nd Stress	10	10+ 10= 20
C-V		
3rd Stress	11	20 + 11= 31
C-V		
4th Stress	12	31+ 12= 43
C-V		
5th Stress	13	43+ 13=56
C-V		
6th Stress	14	56+ 14= 70

The corona current parameter was set at -0.8. Each C-V measurement was done at an incremental charge of ~0.03 μC/cm^2. Below illustrates the results for two different sites on a 150 Å thick oxide.



(a)



(b)

Figure 4.3: Capacitance-voltage characteristics versus corona stress.

In Figure 4.3, as the time of stress increased up to the cumulative time of 70s, the minimum capacitance and depletion width increased. The minimum capacitance is the value at which the curve depletes before weak inversion occurs. This phenomenon may be due to the creation of traps or a high charge density on the oxide surface. At the depletion region, the total capacitance without interface trap charges is equal to the series connection of the oxide capacitance and the depletion layer capacitance (see equation 4.1).

$$C_t = \frac{C_{ox}\left(C_d + C_{it}\right)}{C_{ox} + C_d + C_{it}} \tag{4.1}$$

where C_{ox} is the oxide capacitance, C_d is the depletion capacitance, and C_{it} is the interface trap capacitance. As C_{it} increased, the total capacitance in the depletion region also increased. Since the charge deposited on the oxide surface cannot be directly measured, it was calculated using a calibrated capacitor. The results from this capacitor revealed that the deposited charge was in the range of micro-coulombs. As a result of the experiments, the Ion-Drift Spectrometer tool could be used for non-contact C-V measurements but the location of the tool was not ideal for non-contact SILC measurements on 4H-SiC oxidized wafers. The relative humidity and room temperature varied on a daily basis which created inconsistencies on the quantity of ionic charges. Hence, the deposited charges could not be efficiently calibrated for a sequence of repeatable measurements. In summary, it was shown that the corona source is current limited and high corona charge fluences induced trapped charges in the oxide.

4.3. Potential Factors Affecting the Accuracy of the Contact Potential Difference

The contact potential difference (V_{cpd}) was determined by the Kelvin method as stated in Section 2.8.1. A Kelvin probe is connected to a lock-in amplifier and other relevant electronics. As the reference electrode vibrated periodically at a defined frequency, the lock-in amplifier detected a displacement current defined by Equation 2.25. The DC bias voltage varied until this current approached zero. The precision of the determined V_{cpd} was within 0.1 mV. According to Equation 2.25, the height of the probe and the frequency of the sinusoidal signal affect the determined V_{cpd}. Internal calibrations were performed on known SiO_2/Si systems to verify the accuracy of the measurement. The height of the probe from the surface of the substrate was calibrated between 200 μm and 500 μm.

After corona deposition on the surface of the oxide, V_{cpd} was measured. There were essentially three unknown components of V_{cpd} , the semiconductor-reference electrode work function difference, the voltage drop across the oxide and the voltage drop across the semiconductor surface barrier (see Equation 2.26). The work function varied based on the semiconductor doping levels and condition of the probe's surface. It primarily caused a shift in the calculated electric field. This work function offset effect was not observed when determining the capacitance and current density because the change in the contact potential difference was calculated (see Equation 2.32). The voltage drop across the oxide and the voltage drop across the semiconductor surface barrier were determined by following the procedure described in Section 3.1.1.

The contact potential difference was measured as a function of time. A logarithmic regression analysis of the inverse of the measured V_{cpd} versus time was performed to determine the characteristic of the curve, which was related to the predicted Fowler-Nordheim current density equation coefficients. The corresponding R-squared value determined if the data fitted to this function. The R-square value ranged from 0.997 to 1 for all measured data. The current density was then calculated at each increment of time from the fitted voltage decay and the oxide capacitance (see Equation 2.36).

4.4. Fowler-Nordheim Conduction in Afterglow Oxide and Thermal Oxide on 4H-SiC

After the pre-charging treatment, all measured oxides were given a high dose of positive corona charge for a 5-second duration under illumination. The substrate was placed into deep accumulation. The corona current parameter was set to 0.8. This low charge fluence, 40 $\mu C/cm^2$, created a high oxide field for the occurrence of Fowler Nordheim tunneling and established the maximum voltage drop across the oxide. This maximum voltage was known as $V_{SASS.}$ The oxide voltage (V_{ox}) decay was monitored for 20 seconds after the cessation of corona charging. The average EOT value for each oxidized wafer was obtained from their accumulation capacitance. This thickness was used in the calculation of the experimental Fowler-Nordheim current density. The valence band offset in reference to SiO_2 for 4H-SiC is 3.05 eV as oppose to 4.73 eV for Si [14]. Substrate injection of holes, from this binary semiconductor, was energetically not feasible. The injection of holes would require enough energy to go against the direction of the electric field in the oxide created by a quantum of positive corona charge.

In this regards, only substrate injection of electrons was considered to occur, when a quantum of positive corona charge was deposited on the surface of the oxide.

Before this current was analyzed, each oxide was compared to the Poole-Frenkel slope for SiO_2 to verify that the conduction was indeed by Fowler-Nordheim conduction. In Figure 4.4, the slope of the experimental oxides, AG IV (0.023) and Thermal TA (0.029), did not match the Poole-Frenkel theoretical slope of 0.015 accepted for silicon dioxide.

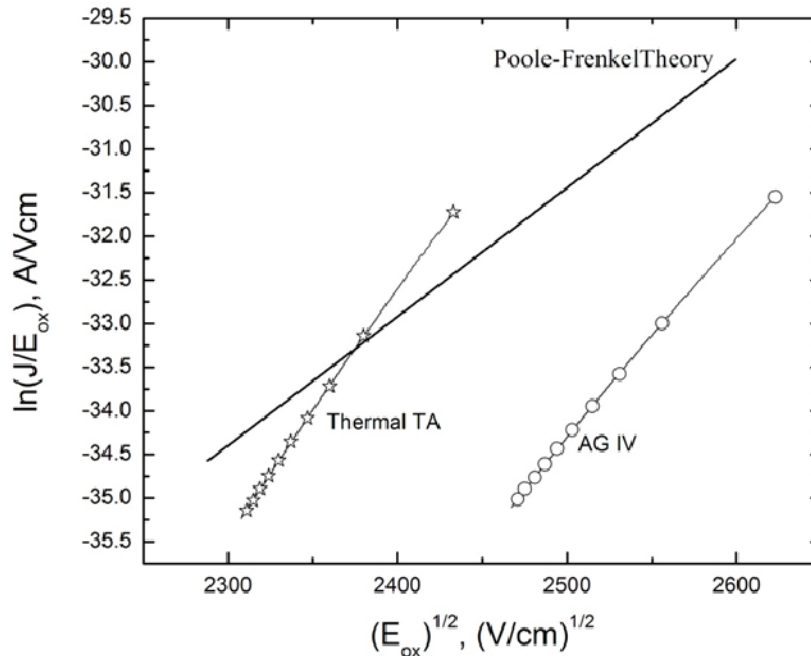


Figure 4.4: Poole-Frenkel plot comparing theoretical and experimental oxides.

The theoretical Poole-Frenkel current density was calculated based on an ionization potential of 1 eV and a proportionality constant of $1x10^{-13}$. Both of these parameters were reported in literature for silicon dioxide [29]. The theoretical slope assumed that a

significant number of acceptor traps were present within the oxide at room temperature and as a result ξ was set to one. According to Equation 2.6, the slope decreases, if there were less acceptor traps within the oxide (ξ=2), to 0.0074. This slope was not remotely close to the experimental slopes. The proportionality constant calculated from the intercept of the Poole-Frenkel plot for the experimental oxides indicated that the density of trap centers was in the range of 10^{-28} to 10^{-24}. Due to the mismatch between the slope of the theoretical line and the experimental lines, it was concluded that the conduction through the experimental oxides was not due to Poole-Frenkel. Although, the line for Thermal TA intersected the theoretical Poole-Frenkel line, the parameters which affected the slope, the dielectric constant and the value of ξ, could not rectify the angle between the lines.

The Fowler-Nordheim characteristics were analyzed for each AG oxide and thermal oxide of 4H-SiC substrates. The experimental Fowler-Nordheim characteristics of oxidized Si samples, with oxide thicknesses greater than 50 Å, had an overall good match to the predicted Fowler-Nordheim current characteristic (see Figure 4.5). As seen in Figure 4.5, the Fowler-Nordheim characteristic is independent of oxide thickness.

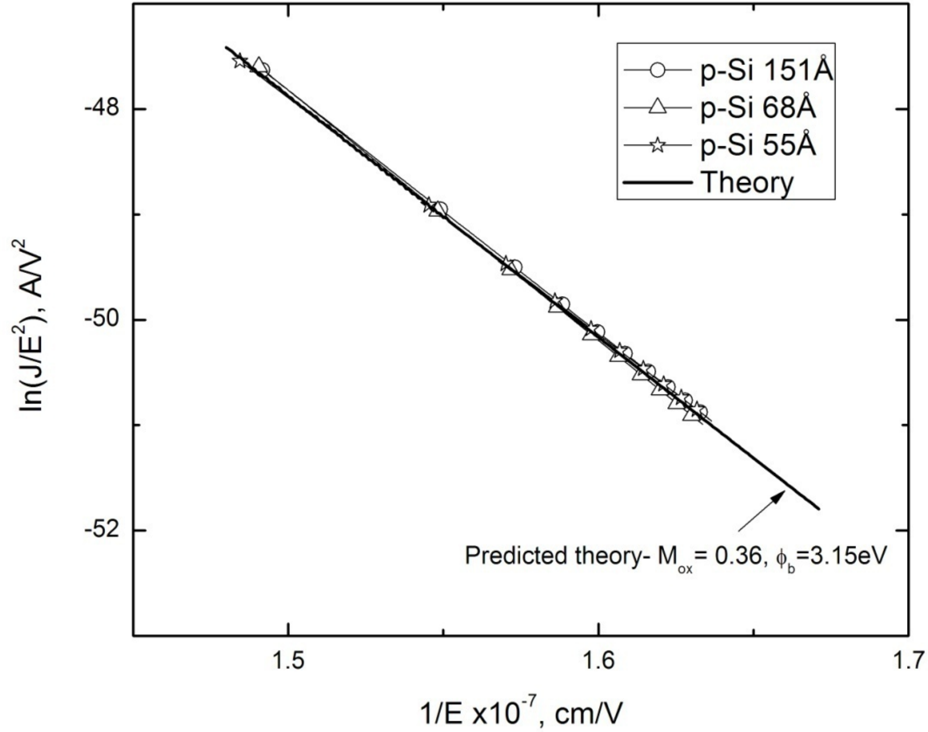


Figure 4.5: Fowler-Nordheim plot for various thermal oxide thicknesses on Si.

In this study, the effective barrier height was established by two methods. The first method utilized the measured current (J_{exp}) from I-V measurements. It was then fitted to the predicted theoretical Fowler-Nordheim current characteristics defined in the software and the thickness was determined. The default theoretical Fowler-Nordheim current characteristic for SiO_2/Si systems was based on M_{ox} of 0.36 and an effective barrier height of 3.15 eV. The change implemented in the software for SiO_2/4H-SiC systems, with regards to the default values, was the effective barrier height. It was changed from 3.15 eV, the conduction band offset for SiO_2/Si [36] to 2.7 eV, the conduction band offset for SiO_2/4H-SiC [81]. The effective mass in the oxide was not changed since it was previously shown that AG oxide or thermal oxide grown on 4H-SiC substrates had a

relative dielectric constant of 3.9 [75]. However, the thickness value from the I-V measurement did not match the independently measured average EOT value from C-V measurements. This indicated that trapped charges and the oxidation process chemistry influenced the measured voltage. To optimize the measured Fowler-Nordheim curve to the theoretical Fowler-Nordheim curve, the effective barrier height was varied until the thickness fitted to $\pm$ 5% of the independently measured average EOT value. Table 4.3 along with Figure 4.6 shows the effect of oxidation process chemistry on the effective barrier height for SiO_2/4H-SiC systems. The x-axis on the graph represents the oxidation process for a thermal oxide and AG oxides (annealed and non-annealed).

Table 4.3: Oxidation process chemistry variation.

Afterglow oxidation at 850^{0}C, 90 min. in excited media: (O_2:N_2O:FG) with variation of FG flow						
Process	FG Flow	Parameters of Post Oxidation Anneal				
	(l/min)	Temp (^{0}C)	Time (min)	FG (l/min)	N_2O (l/min)	O_2(l/min)
TH TB	Thermal atmospheric oxide, outside vendor					
AG I_A	0.5	850	60	0.5	0.2	3
AG IV	0.5	950	120	1	-	3
AG V	0.5	900	360	0.5	0.2	3
AG VI	0.5	950	120	-	0.3	4
AG VIII	0.5	AG IV after RCA clean and anneal (2h, 1100^{0}C, Ar)				
AGW V	1	-	-	-	-	-
AGW VI	1.3	-	-	-	-	-

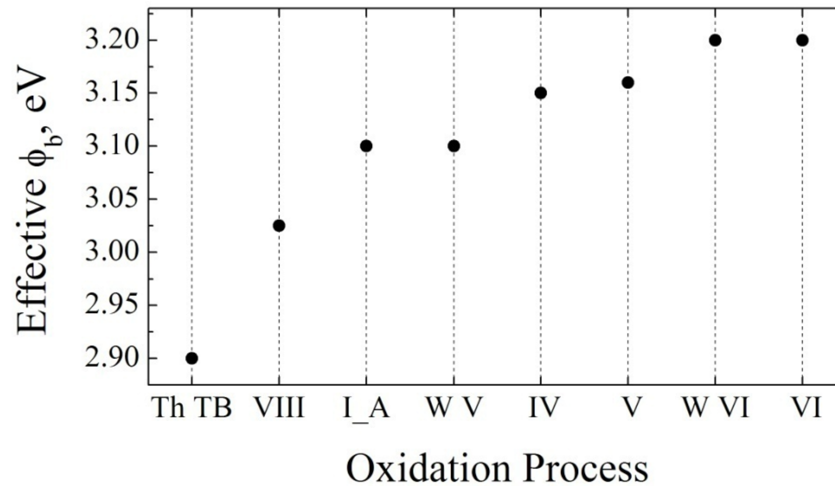


Figure 4.6: Oxidation process chemistry influence on the effective barrier height for SiO_2/4H-SiC systems (see Table 4.3 for oxidation process representation).

In Figure 4.6, the estimated effective barrier height value slightly varied depending on the oxidation process conditions. It is shown that a post-oxidation anneal in (O_2: FG) slightly decreased the estimated effective barrier height, when compared to a post-oxidation anneal in (O_2: N_2O). Comparing AGW V and AGW VI, the estimated effective barrier height slightly increased to 3.2 eV for a variant of the oxidation growth mixture, when compared to 3.1 eV for a slight FG increase in the oxidation growth mixture. The oxidation of 4H-SiC at a temperature greater than 1100^0C following a NO post-oxidation anneal at a similar temperature (Thermal TB) revealed a reduced estimated effective barrier height of 2.9 eV, when compared to AG oxidation of 4H-SiC at a temperature of 850^0C. The AG VIII oxide is the same as AG IV oxide, except for the addition of a 2-hour 1100^0C Ar anneal after SC1 and SC2 cleans without HF dip. This oxide had a lower estimated barrier height value of 3.03 eV compared to AG IV oxide.

Similar evidence of the oxidation process influence on the effective barrier height has been reported in literature on SiO_2/Si systems. The effective barrier height increased up to 0.2 eV due to microscopic atomic structural changes in an oxide grown on silicon within a controlled chemical environment [82]. This method was used to calculate the effective SILC values for a given oxidation process.

In the second method, Fowler-Nordheim current was calculated using Equation 2.36. From the Fowler-Nordheim plot, the experimental slope value for each oxide was extracted and the effective barrier height was calculated using Equation 2.12. The Fowler-Nordheim analysis reported in literature for SiO_2/SiC systems assumes M_{ox}= 0.42 and calculates the effective barrier height using Equation 2.12. As a result, two effective mass in the oxide values were compared: M_{ox}= 0.36, used for Fowler-Nordheim characteristics in the FAaST 230 tool; and M_{ox}= 0.42, used commonly for SiO_2/SiC systems [83-87]. Table 4.4 and Table 4.5 show the effective barrier height calculated based on an assumed effective mass in the oxide.

Table 4.4: Calculated effective barrier for annealed 4H-n-type experimental samples.

Oxidation Process	EOT (Å)	Oxide Electric Field (MV/cm)	Experimental Slope (V/cm)	ϕ_b based on 0.36 (eV)	ϕ_b based on 0.42 (eV)
AG I_A	515	6.1 to 6.9	-1.81E+08	2.70	2.56
AG I_B	320	6.2 to 7.0	-1.91E+08	2.79	2.65
AG II	500	6.0 to 6.8	-1.87E+08	2.75	2.61
AG III	554	6.1 to 6.9	-1.82E+08	2.70	2.57
AG IV	520	6.1 to 6.9	-1.81E+08	2.70	2.56
AG V	489	6.1 to 6.9	-1.76E+08	2.65	2.51
AG VI	480	6.3 to 7.0	-1.97E+08	2.84	2.70
Thermal TA	517	5.3 to 5.9	-1.81E+08	2.69	2.55
Thermal TB	439	5.5 to 6.1	-1.87E+08	2.75	2.61
Thermal TC	318	6.1 to 6.9	-1.87E+08	2.75	2.62

Table 4.5: Calculated effective barrier for non-annealed 4H-n-type experimental samples.

Oxidation Process	EOT (Å)	Oxide Electric Field (MV/cm)	Experimental Slope (V/cm)	ϕ_b based on 0.36 (eV)	ϕ_b based on 0.42 (eV)
AGW I	511	6.1 to 6.9	-1.83E+08	2.71	2.57
AGW II	433	6.2 to 6.9	-1.89E+08	2.77	2.63
AGW III	160	5.6 to 6.2	-1.70E+08	2.58	2.45
AGW IV	135	5.7 to 6.3	-1.71E+08	2.59	2.46
AGW V	412	6.0 to 6.7	-1.88E+08	2.76	2.62
AGW VI	310	6.2 to 7.0	-1.84E+08	2.72	2.59

In Figure 4.7, the Fowler-Nordheim plot is influenced by post-oxidation annealing, since there was a slight variation in the slopes of the oxides.

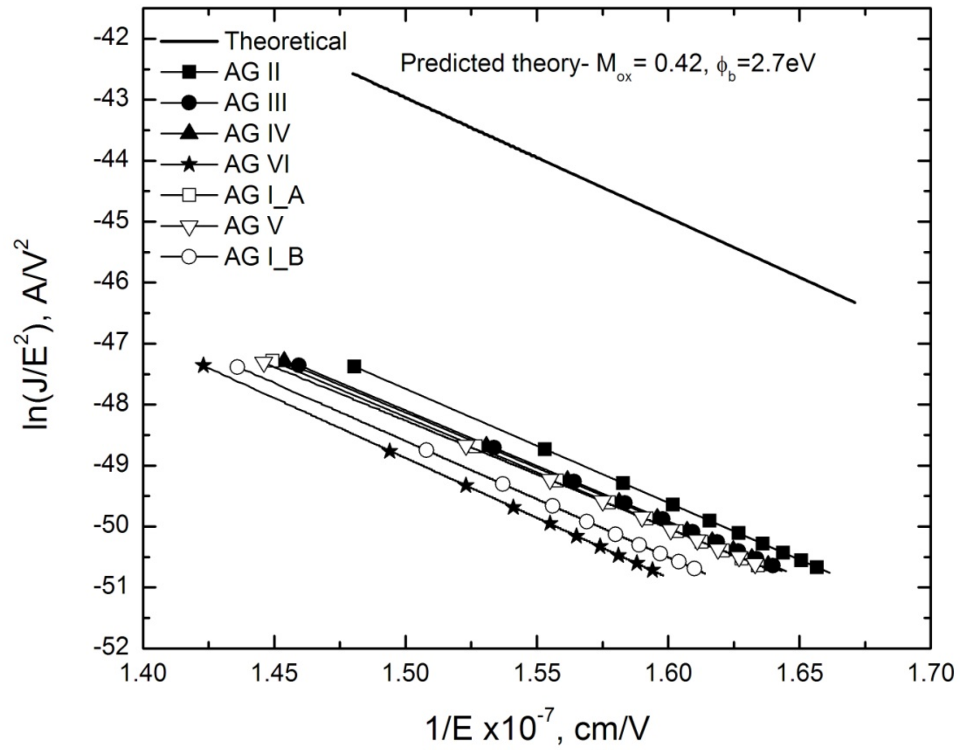


Figure 4.7: Fowler-Nordheim plot of AG annealed oxides.

Although the oxidation process conditions varied, the AG oxides' Fowler-Nordheim slope was comparatively independent of oxide thickness. The slight parallel shift, between the various annealed experimental AG oxides, indicated that the density of the oxide and trapped charges in the oxide affected the intercept and slope of the Fowler-Nordheim plot. The offset between the experimental lines and the theoretical line could be due to a variant of the effective mass in the AG oxides.

From the experimental data, the effective mass in the AG oxide could not be accurately extracted from the slope and intercept of experimental Fowler-Nordheim plots. As seen in Equation 2.15, the effective mass in the oxide is included in the pre-exponential and exponential factor of the Fowler-Nordheim current density equation. Any slight error in the intercept of the line results in a significant change of M_{ox}. This was not a concern for the measurements on SiO_2/Si systems. Therefore, it was possible that the intercept for an AG oxide on 4H-SiC was affected by the quantization of the energy level of the electrons tunneling through the oxide. To confirm this hypothesis, Fowler-Nordheim plot of thermal oxides measured under the same conditions was compared to the theoretical Fowler-Nordheim line (see Figure 4.8).

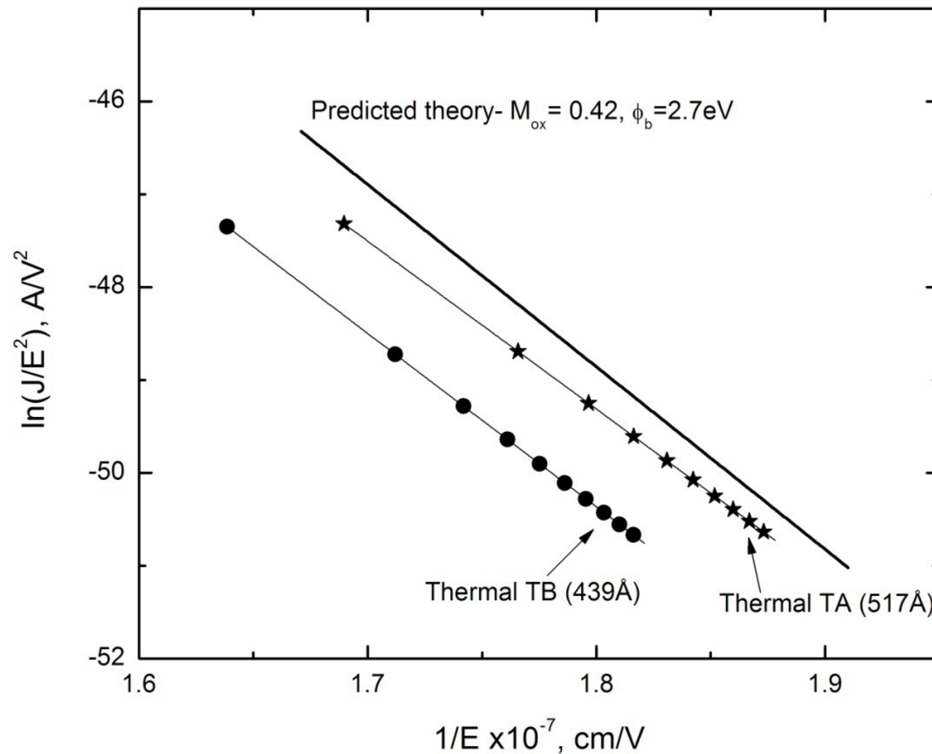


Figure 4.8: Fowler-Nordheim plot of thermal annealed oxides.

All of the experimental thermal oxides were parallel to the theoretical line, with Thermal TA being in close proximity to this line. The offset between the experimental thermal oxides and the theoretical line, however, was still present. There are three possible explanations. The first possibility was based on the assumption that traps created during Fowler-Nordheim stress on oxidized n-type 4H-SiC were not negligible as compared to oxidized Si samples. The second possibility was based on the assumption that the dielectric constant of oxide grown on 4H-SiC was not 3.9 as accepted for thermal silicon dioxides [16]. However, the second possibility was discredited. A simulation of this parameter revealed that the dielectric constant needed to be increased more than 100% of its current value to match the theoretical intercept value. Finally, the third possibility was based on the fact that the value of the effective mass in the AG oxide could be higher than 0.42m. In addition to the AG annealed oxides, the non-annealed 90-minute oxides also exhibited a similar oxide field range compared to the annealed oxides (see Figure 4.9).

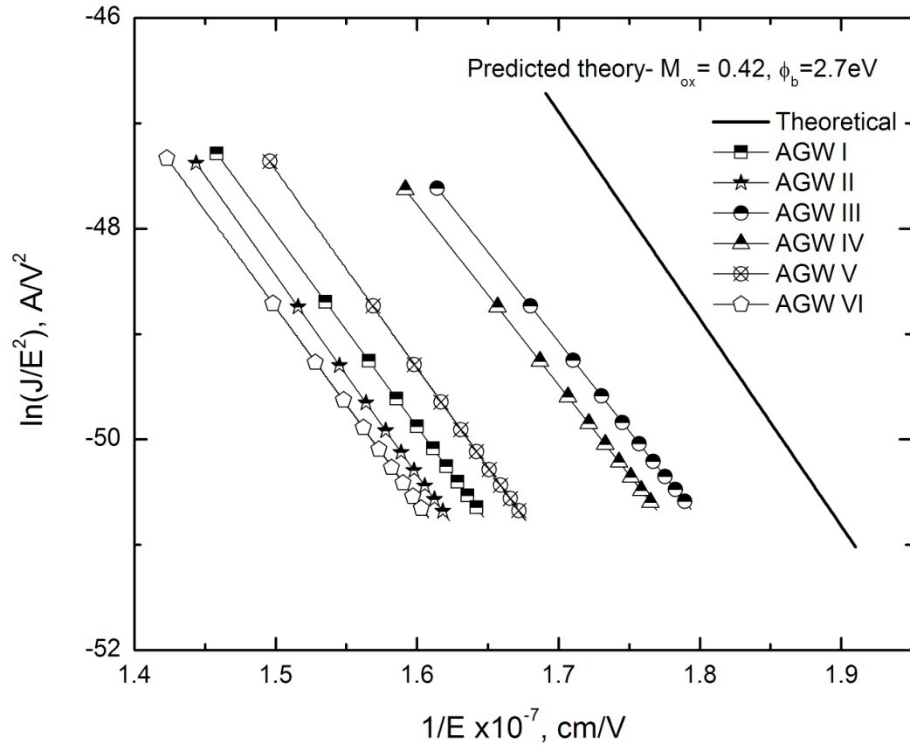


Figure 4.9: Fowler-Nordheim plot of non-annealed AG oxides.

In Figure 4.9, the ten minute non-annealed oxides, AGW III and AGW IV shifted toward the theoretical line. This variance further indicated that the Fowler-Nordheim characteristics had a dependence on the oxidation of n-type 4H-SiC substrates. The effect of the FG pre-treatment was not significant on the Fowler-Nordheim plot except by thickness comparability. The FG pre-treatment led to a higher growth rate and better oxide thickness uniformity throughout the wafer. This evidence was seen through C-V measurements of five measurement sites on the wafer taken in the dark and light, respectively. These regions were located on the wafer's top, right, center, left, and bottom point sites. The offset was still evident with non-annealed oxides, which confirmed the first and third possibilities conjectured earlier.

As seen in Table 4.4 and Table 4.5, using an assumed M_{ox} of 0.36 instead of 0.42, the experimental effective barrier height value is in proximity to 2.7 eV. However, in Figure 4.10, the theoretical line with M_{ox} of 0.36 has a greater offset when compared to the experimental oxides.

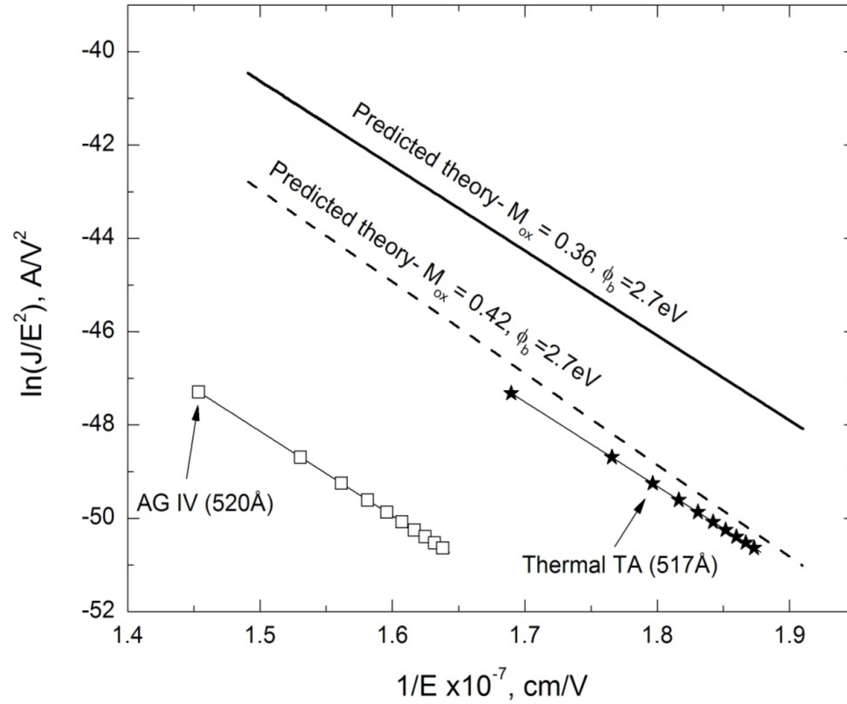


Figure 4.10: Comparison of experimental data and predicted Fowler-Nordheim lines.

The predicted Fowler-Nordheim lines implied that AG oxides had an effective barrier height value greater than 2.7 eV, contrary to the value found using internal electron photoemission study [81]. To further investigate this offset, the influence on the self-adjusting steady state voltage (V_{SASS}), the effective mass in the oxide, effective barrier height, and trapped charges in the oxide will be analyzed in the proceeding sections.

4.4.1. Self Adjusting Steady State (SASS) Voltage on Oxides

The self-adjusting steady state voltage, V_{SASS}, was determined for each oxide after the Fowler-Nordheim conduction. The corona current density was set to 8 $\mu A/cm^2$. Each oxide was further stressed with the same high dose of positive corona charge in 100s increments. It was reported that the SASS voltage correlated to the band offset in a dielectric-Si system [76]. The SASS voltage reported for SiO_2/Si systems was taken at 1.2 seconds. In this study, the SASS voltage for SiO_2/4H-SiC systems was taken at 1.7 seconds due to the later stabilization of the voltage measurement acquisition. The total stress cumulative times were 5s, 105s, 205s, 305s, and 405s on AG oxides and up to 505s for thermal oxides. Figure 4.11 illustrates the V_{SASS} trend for all experimental annealed oxides.

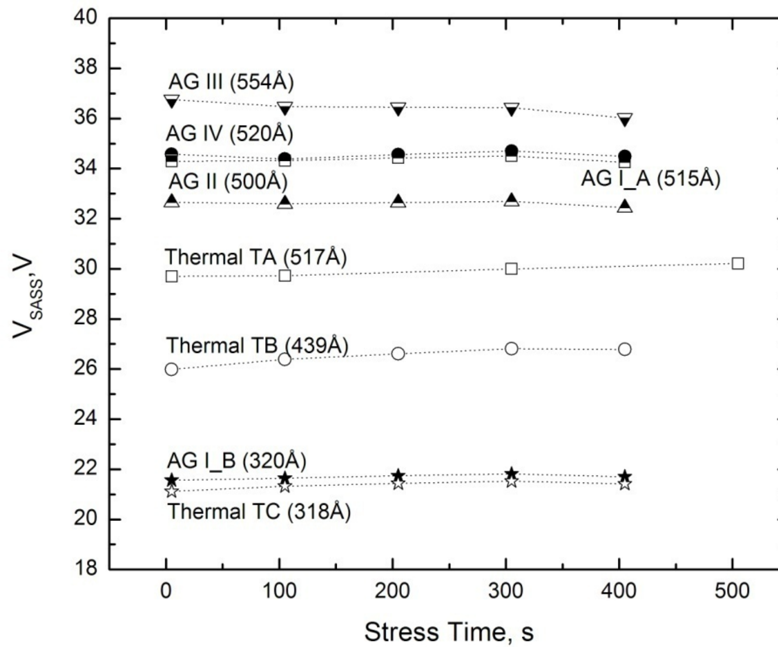


Figure 4.11: Steady-state voltage experimental oxide comparison.

In Figure 4.11, comparing comparable thicknesses, the AG oxides had a higher steady state voltage than the thermal oxides. This indicated that the AG oxides had a higher tunneling barrier height. At the highest stress time, the AG oxides tend to slightly decrease in voltage when compared to the thermal oxides, which was attributed to the post-oxidation anneal treatment.

4.4.2. Significant Parameters: Effective Mass in the Oxide and Barrier Height

To examine the shift in the Fowler-Nordheim plot between the experimental oxides and the predicted Fowler-Nordheim characteristics, only AG IV and Thermal TA oxides will be used since their thickness was comparable. The possibility, which

assumed that the traps induced in the Fowler-Nordheim regime were negligible, is discussed in the following paragraph.

The effective mass in the oxide and effective barrier height from the theoretical curve were varied to fit the experimental oxides. First, the effective mass in the oxide was increased and the effective barrier was kept constant at 2.7 eV (see Figure 4.12).

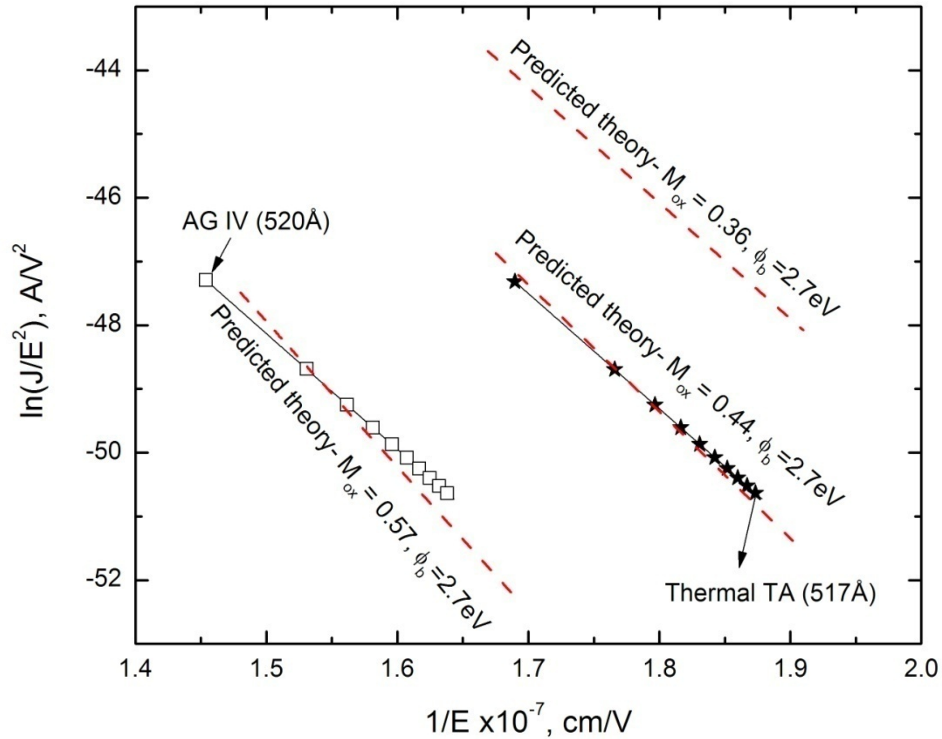


Figure 4.12: Variation of M_{ox} on the predicted Fowler-Nordheim characteristics.

For the AG oxides, M_{ox} was approximately 0.57 and for the commercial thermal oxides, it was about 0.44. Further increase in M_{ox} did not lead to an exact match for the AG oxides. There are three probable causes: the trapped charge influence on the oxide field, the oxide structure's incorrect effective barrier height, or both. The effective mass in the

oxide increases as a result of the electron's dispersion during tunneling. Theoretically, the effective mass in the oxide is based either on a Franz dispersion relation or parabolic dispersion relation [34, 36, 88]. These dispersion relations are attributed to the tunneling electron energy momentum in the oxide band gap. This momentum includes the electron wave vector of the tunneling electron and the total tunneling electron energy from the semiconductor conduction band edge. In Table 2.3, the standard accepted value for M_{ox} on SiO_2/Si system ranged from 0.36 to 0.5. A M_{ox} of 0.42 is the typical value chosen for SiO_2/SiC systems since it is assumed that electrons tunneling in the oxide band gap have similar dispersion relationship. Determining the dispersion relation for SiO_2/SiC was beyond the scope of this study. To demonstrate the influence of varying the effective barrier height on the Fowler-Nordheim plot, the theoretical line was evaluated over the same oxide field using a constant M_{ox} of 0.36 with an effective barrier height of 2.7 eV, 2.9 eV, 3.15 eV, and 3.25 eV, respectively (see Figure 4.13).

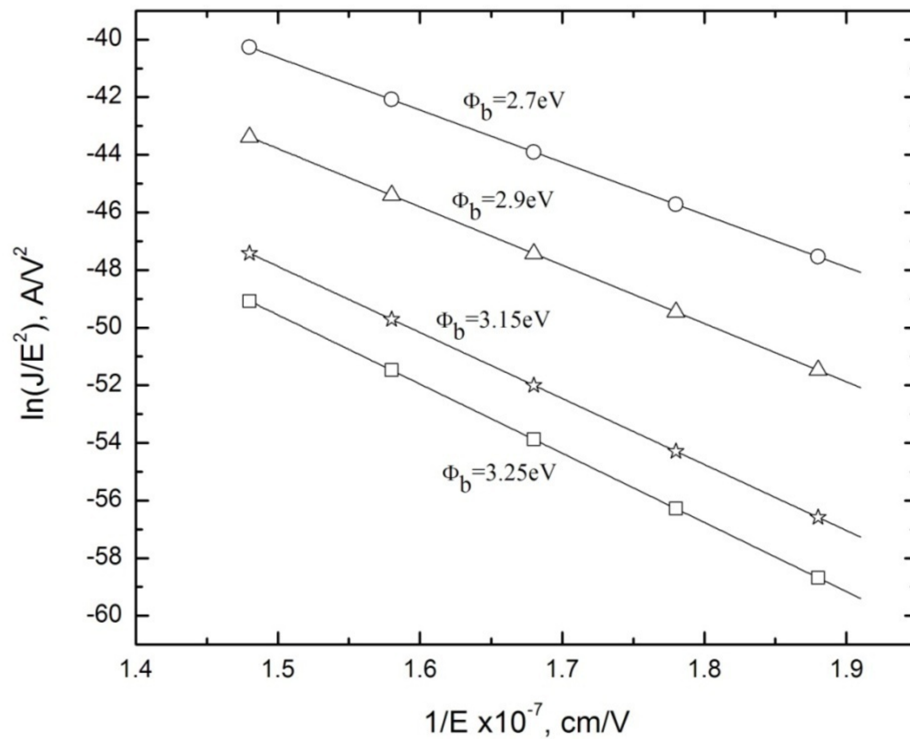


Figure 4.13: Theoretical Fowler-Nordheim plot varying the effective barrier height with M_{ox} of 0.36.

In Figure 4.13, as the effective barrier height increased, the intercept and the offset between the lines decreased. The slopes of the lines were nominally in the same range $\sim 10^8$ V/cm. The apparent reduction or increase in the calculated effective barrier height for the experimental oxides compared to 2.7 eV (the theoretical effective barrier height for SiO_2/4H-SiC) was attributed to the influence of trapped charge in the oxide. Trapped charges were confirmed by an observed shift of the flat band voltage on re-measured C-V measurements.

4.4.3. Comparison with Fowler-Nordheim Literature Data on Oxide-n-type 4H-SiC Devices

Figure 4.14 illustrates an example of a typical measurement performed on 4H-SiC-MOS devices to analyze the Fowler-Nordheim conduction. The voltage is swept at a defined rate (dV/dt) and the current is measured. A spike in the current indicated the breakdown of the oxide.

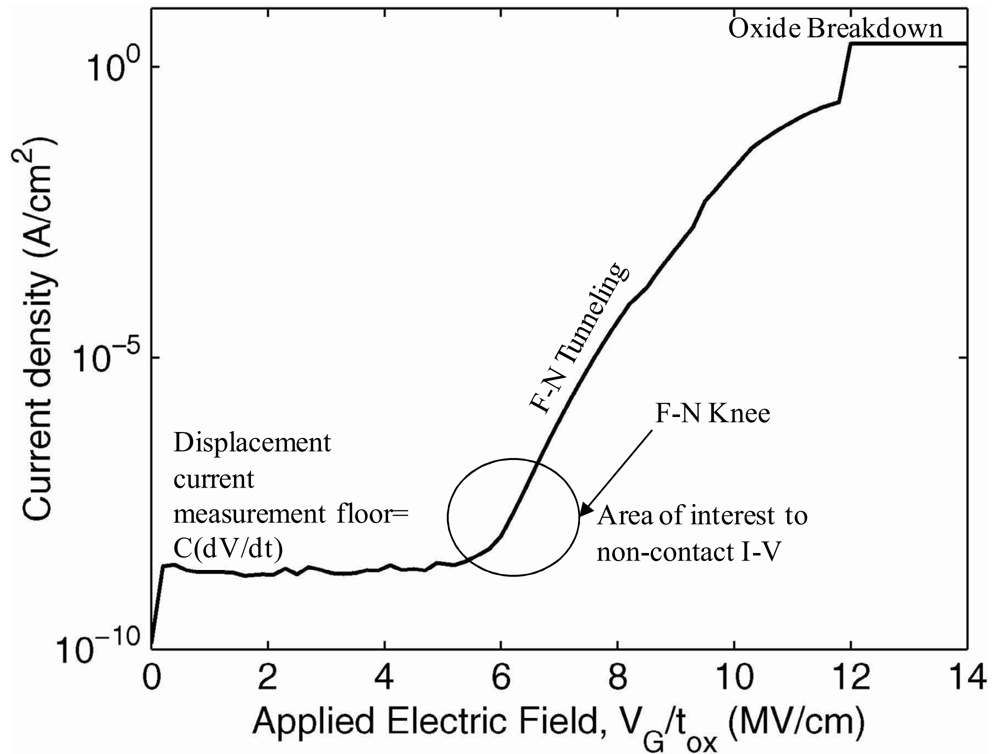


Figure 4.14: Example of current-voltage characteristics of a 4H-SiC MOS capacitor with a 500 Å gate oxide measured at room temperature [52].

The displacement current, below the Fowler-Nordheim voltage knee, changed to a conduction current from the conduction band, above this voltage knee. The area of interest for non-contact I-V measurements was within the Fowler-Nordheim voltage

knee. The maximum electric field attained during non-contact I-V measurements was approximately 7 MV/cm.

Equation 2.15 is the standard Fowler-Nordheim equation used historically to analyze SiO_2/SiC devices. Only a few research groups have explored the occurrence of Fowler-Nordheim tunneling regime on SiC-based MOS devices with respect to temperature [85-87]. It was concluded that higher temperatures decreased the effective barrier height. At room temperature, the conduction band offset at the SiO_2/4H-SiC interface was determined to be 2.7 eV using internal electron photoemission (IPE) [81]. As a result, the theoretical Fowler-Nordheim plot for SiO_2/4H-SiC systems is based on the effective barrier height of 2.7 eV and on an assumed effective mass in the oxide. This M_{ox} is commonly chosen as 0.42 and is taken from measurements done on SiO_2/Si systems [34]. Table 4.6 includes the effective barrier height values reported for 4H-SiC MOS devices after Fowler-Nordheim injection of electrons from 4H-SiC into the oxide conduction band. These values were calculated from the Fowler-Nordheim plot slope using Equation 2.12 with an assumed M_{ox} of 0.42.

Table 4.6: Reported effective barrier height for 4H-SiC MOS devices at room temperature.

Reference	Gate oxide T_{ox} (Å)	Experimental Slope (V/cm)	Effective Barrier Height (eV)	Oxide Electric Field (MV/cm)
[83]	400	-2.06E+08	2.78	6.9 to 8.3
[85]	230	-1.90E+08	2.64	7.7 to 10
[86]	93	-1.73E+08	2.48	6.3 to 7.1
[84]	670	-1.96E+08	2.70	7.1 to 10
[87]	225	-1.68E+08	2.43	6.3 to 10

In Table 4.6, although the oxidation process conditions in each report varied, the Fowler-Nordheim slope was comparatively independent of oxide thickness. Figure 4.15 illustrates the comparison between device-based contact measurements and non-contact measurements. The Fowler-Nordheim characteristic of the un-metallized thermal oxide is comparable to metallized oxides.

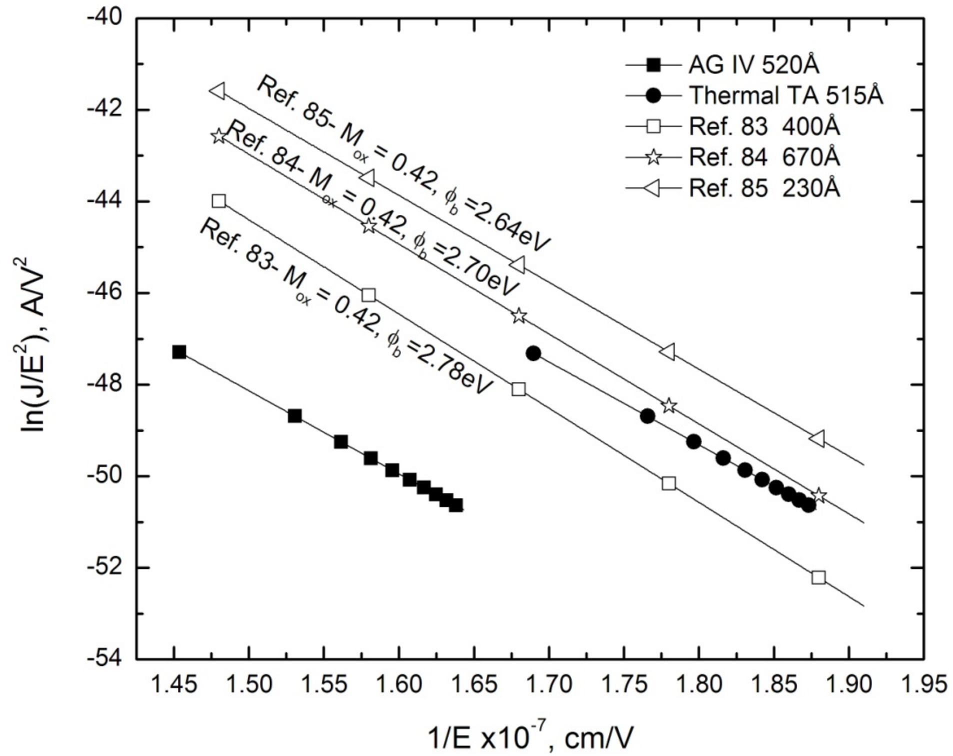


Figure 4.15: Fowler-Nordheim conduction comparison of contact versus non-contact measurements.

The current density for the experimental oxides is lower than the metallized oxides due to the current limitation of the non-contact measurement system. The inconsistency observed by these studies in the effective barrier height value indicates the sensitivity of the fabrication process. It was postulated to be due to the effect of the post-oxidation annealing condition used, which influenced the quantity of charges in the oxide.

4.4.4. Influence of Trapped Charge in the Oxide

To reiterate, Fowler-Nordheim conduction occurs when electrons flow into the oxide conduction band through a triangular potential barrier. If oxide charges are located within the Fowler-Nordheim tunneling regime, the centroid of these trapped charges

influences the voltage drop across the oxide and changes the shape of the potential barrier from triangular to a non-triangular barrier. In the presence of these charges within the Fowler-Nordheim tunneling regime, the oxide field (F) is given as [89-91]

$$F = \frac{V_{ox}}{t_{ox}} - \frac{Q_t}{\varepsilon_0 \varepsilon_r}\left(1 - \frac{\bar{x}}{t_{ox}}\right) \tag{4.2}$$

where Q_t is the trapped charge in the oxide, $\bar{x}$ is the centroid of the charge distribution measured with respect to the semiconductor/SiO_2 interface, t_{ox} is the oxide thickness, V_{ox} is the voltage drop across the oxide, ε_r is the dielectric constant, and ε_0 is the permittivity of vacuum. Figure 4.16 illustrates the influence of charge trapped within the Fowler-Nordheim tunneling regime in SiO_2/Si system [92].

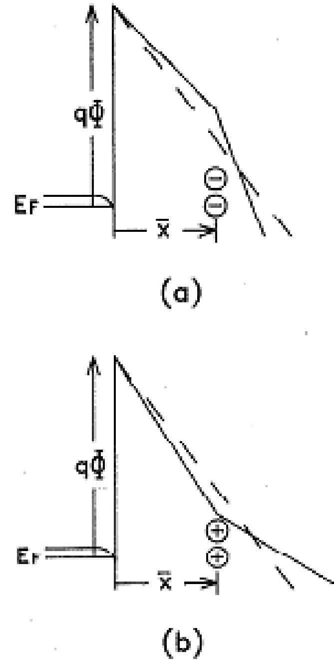


Figure 4.16: Charge trapped within tunneling regime in SiO_2/Si system: (a) negative charge trapping, (b) positive charge trapping [92].

In Figure 4.16, the gradient of the potential in the oxide changed depending on the polarity of the trapped charge. The modified oxide field is lowered as predicted by Equation 4.2 due to trapped charge. To account for this effect, the Fowler-Nordheim current equation was modified and denoted as J_{non} [91]

$$J_{non} = \frac{mq^2 E_{ox}^2}{8\pi h m_{ox} C_{non}} \exp\left(\frac{-\left(8\pi\sqrt{2qm_{ox}}\right) D_{non}}{3hE_{ox}} \right) \tag{4.3}$$

$$C_{non} = \left(\sqrt{\phi_b} + \left[\left(\frac{Q_t}{\varepsilon_{ox} E_{ox} - Q_t} \right) \sqrt{\phi_b - E_{ox}\bar{x}} \right] \right)^2 \tag{4.4}$$

$$D_{non} = \left(\sqrt{\phi_b^3} + \left(\frac{Q_t}{\varepsilon_{ox} E_{ox} - Q_t} \right) \left[\left(\phi_b - E_{ox} \bar{x} \right)^{3/2} \right] \right). \tag{4.5}$$

Equation 4.3 assumes that the trapped sheet charge is uniformly distributed within the oxide. To illustrate the effect of this modification, an example of a theoretical Fowler-Nordheim plot with trapped charges within or outside the Fowler-Nordheim tunneling regime is shown in Figure 4.17.

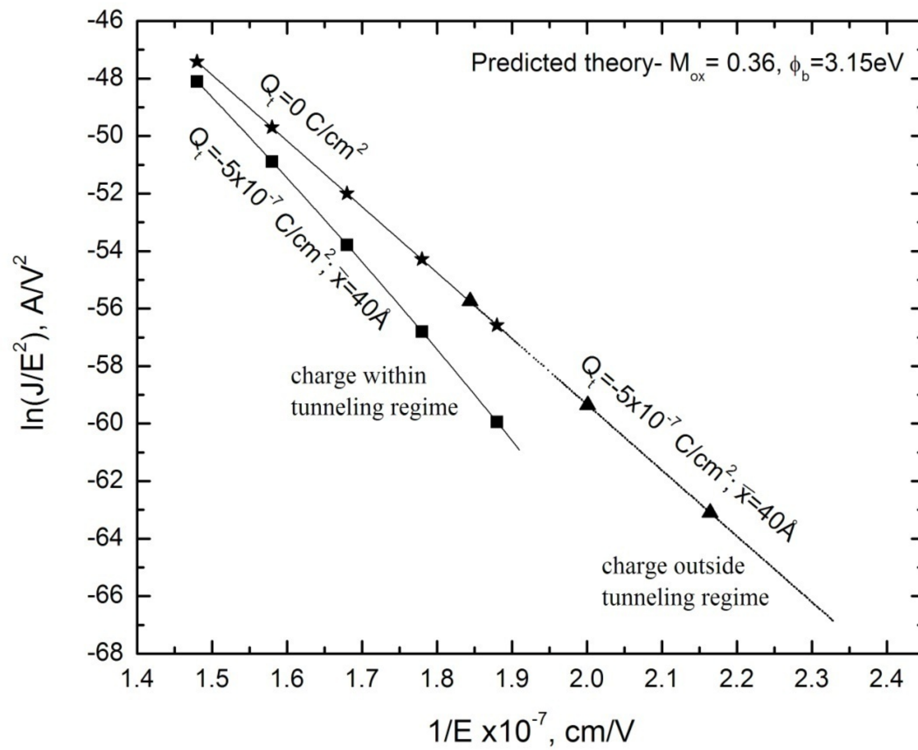


Figure 4.17: Example of trapped charge outside or inside the Fowler-Nordheim tunneling regime in a 500 Å oxide.

As seen in Figure 4.17, charges within the Fowler-Nordheim tunneling regime increased the slope of the line. The angle between the theoretical line without trapped charges and the theoretical line with trapped charges, within the Fowler-Nordheim tunneling distance,

also increased as the oxide field decreased. This angle is controlled by the location of this trapped charge centroid.

4.4.5. Fowler-Nordheim Equation Modification for Oxide-4H-SiC

The influence of the trapped charge in an experimental oxide was verified by re-measuring its C-V characteristics after stress. A flat band voltage shift marked the presence of trapped charges in the oxide. The offset between the Fowler-Nordheim theoretical line and the experimental lines could only be resolved with the assumption that trapped charges were within the Fowler-Nordheim tunneling regime. Equation 4.3 was fitted to the experimental oxides in the attempt to minimize or eliminate this offset. The quantity of the trap charge was estimated by

$$Q_t = \left(V_{fb}^{initial} - V_{fb}^{final}\right)C_{ox} \tag{4.6}$$

where $V_{fb}^{initial}$ and V_{fb}^{final} are the flat band voltage taken before Fowler Nordheim conduction and after a moderate stress, respectively, and C_{ox} is the oxide capacitance. Figure 4.18 illustrates the C-V characteristics of the experimental oxides before and after stress.

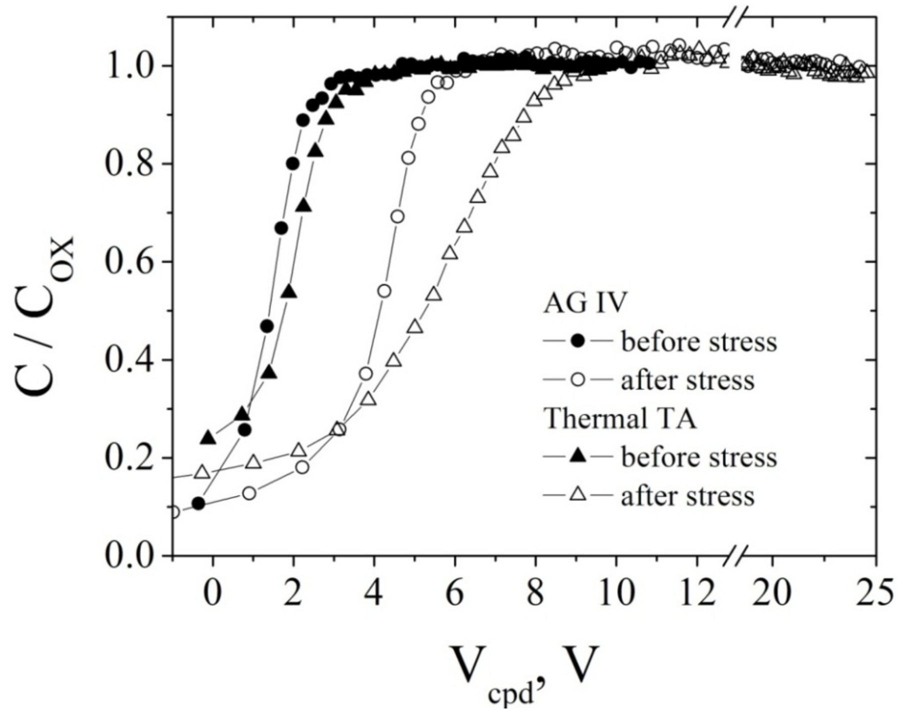


Figure 4.18: Capacitance-voltage characteristics of AG IV and Thermal TA oxides before and after stress.

The trapped charge density for Thermal TA oxide and AG IV oxide was evaluated to be -4.07x10^{-7} C/cm^2 and -7.06x10^{-8} C/cm^2, respectively. A M_{ox} of 0.42 did not provide a reasonable overlay to the experimental oxides. Since the calculated effective barrier height value was in proximity to 2.7 eV (the conduction band offset for SiO_2/4H-SiC systems), M_{ox} was chosen to be 0.36 for the non-triangular theoretical Fowler-Nordheim current characteristic (see Table 4.4 and Table 4.5).

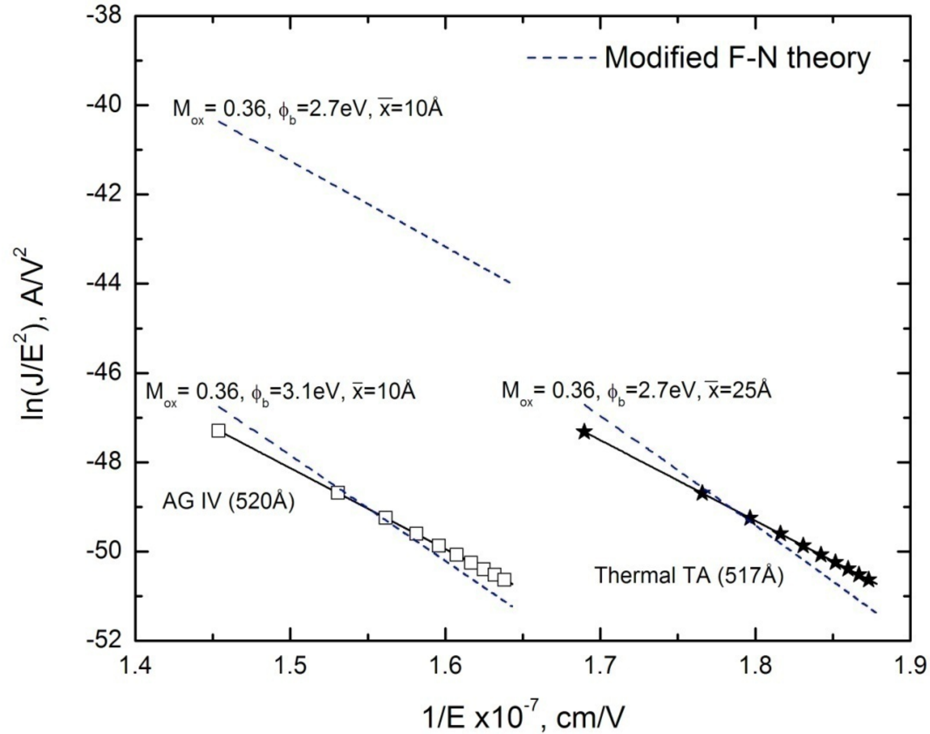


Figure 4.19: Non-triangular Fowler-Nordheim plot fitted to experimental oxides.

As seen in Figure 4.19, to obtain a nominal overlay to the non-triangular Fowler-Nordheim theoretical line, the location of the charge centroid was adjusted to 25 Å for Thermal TA oxide. However, the afterglow oxide did not provide an overlay at the minimum distance of 10 Å. Contrary to Thermal TA oxide, the non-triangular Fowler-Nordheim model parameters could not intersect the AG IV oxide without a change in the barrier height from 2.7 eV to 3.1 eV. This further indicated that the AG oxide structure has fundamental differences from the thermal oxide structure. This increase in the effective barrier height for the AG oxide was also an indication that the AG oxidation growth method modified the surface of the interface. It has been reported that oxidation of 4H-SiC with atomic nitrogen and hydrogen at a temperature of 750^0C revealed a

disordered Si-rich surface [22]. An investigation of the Fowler-Nordheim derivative also suggested that in the presence of negative trapped charge, the exponential oxide field dependence and the effective barrier height value increased [89]. The non-triangular Fowler-Nordheim theoretical line only intersected the experimental lines, which revealed that the exact location of the trapped charge centroid is a critical fitting parameter. The perfect match will depend on the exact charge value and location of the charge centroid within the oxide. To potentially obtain the location of the trapped charge centroid and the charge distribution within an AG oxide, an AG oxide thickness was etched back and analyzed.

4.5. Distribution of Trapped Charge in Oxide on 4H-SiC

The oxide recipe used for this experiment was AG IV oxide. This oxide was etched back to obtain various thicknesses. Prior to testing, the wafers were subjected to two dehydration treatment: a hotplate anneal and a high temperature Ar anneal. After the average EOT was obtained by non-contact C-V measurements in light, the Fowler-Nordheim analysis was examined for each quadrant (see Figure 3.6). Subsequently, the C-V characteristic for each quadrant was re-measured to estimate the trapped charge within each thickness.

4.5.1. Diluted Hydrofluoric Acid Etch Rate on Oxide-4H-SiC

In Figure 3.6, the corresponding time for etch quadrant is as follows: region A was etched for 2 minutes; region B was etched for 5 minutes; region C was etched for 3 minutes; region D was not etched; region E was etched for 8 minutes; and region F was etched for 10 minutes. Afterglow IV oxide was repeated twice for this experiment. This

oxide was also grown on n-type Si wafers. Before each wafer was etched, the uniformity of the oxide was checked by measuring 5 sites on the wafer (top, bottom, right, left, and center). For the 4H-SiC wafers, non-contact C-V measurements determined the average EOT on each site. For the Si wafers, the average oxide thickness was determined by Ellipsometer measurements. This is because afterglow oxidation process was too harsh for the silicon surface, as evident through noisy non-contact C-V characteristics. The difference between the two oxidation process runs, AG IV _EA and AG IV_EB, was the excitation plasma power level. The first plasma run was set to approximately 900 W and the second plasma run was set about 1100 W.

A linear regression analysis was then performed to determine the etch rate. In Table 4.7, the etch rate, along with the corresponded R-squared value, is reported for each oxidation process run.

Table 4.7: Etch rate comparison between 4H-SiC and Si wafers at 24^0C.

Oxidation Run	Etch Rate (Å/min) for Si	Etch Rate (Å/min) for 4H-SiC
AG IV_EA	41 (R^2=0.937)	46 (R^2=0.939)
AG IV_EB	32 (R^2=0.996)	36 (R^2=0.992)

The oxide on 4H-SiC etched at a slightly faster rate than the oxide on Si. The etch rate variation between Si and 4H-SiC differed only by a few angstroms. In the first oxidation process run, AG IV_EA, the R-squared correlation did not give a relatively good fit to the data but gave a better fit for the second oxidation run. This was attributed to the as-

grown oxide uniformity and density structure. Figure 4.20 and Figure 4.21 illustrates the linear regression fit for each oxidation process run.

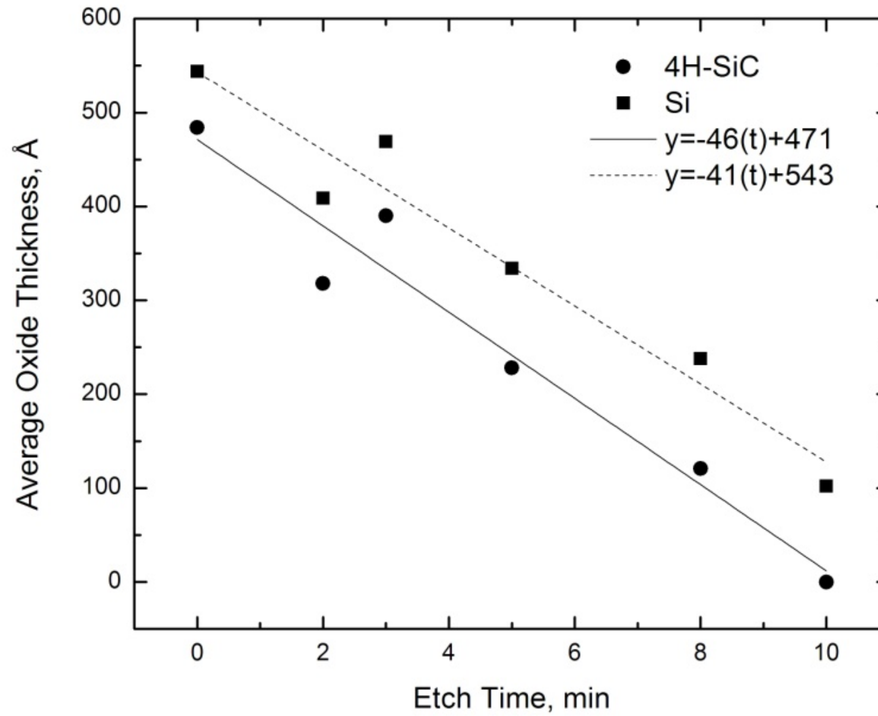


Figure 4.20: Oxide thickness after diluted HF etching for oxide AG IV_EA.

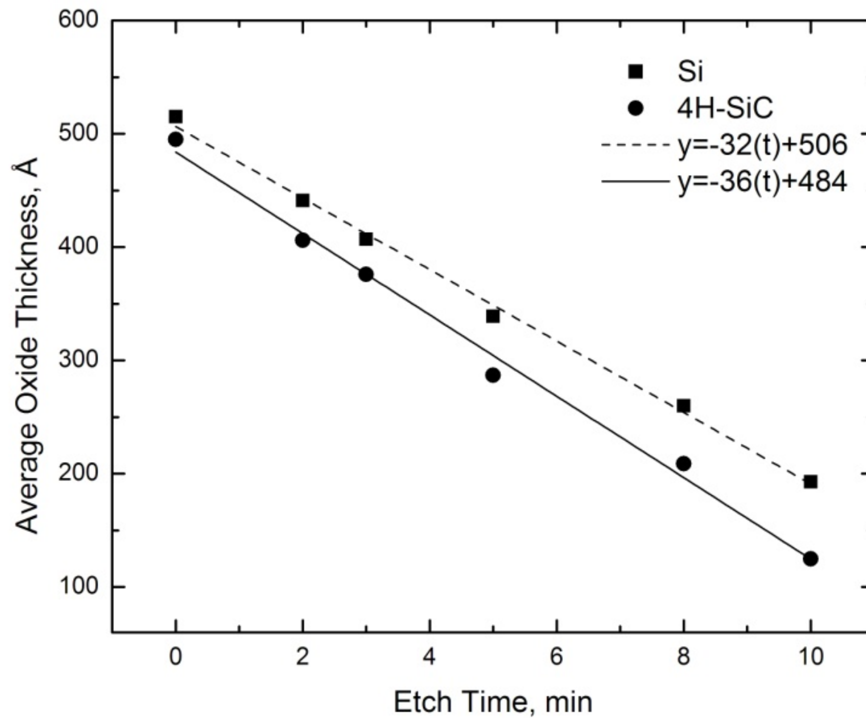
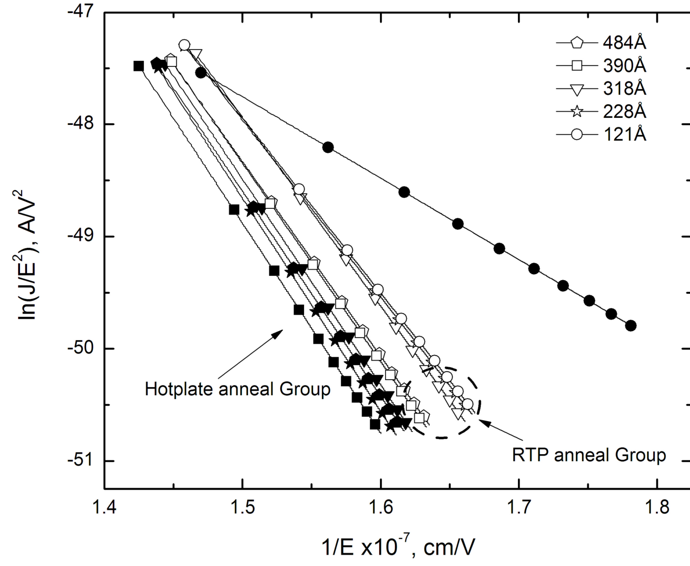


Figure 4.21: Oxide thickness after diluted HF etching for oxide AG IV_EB.

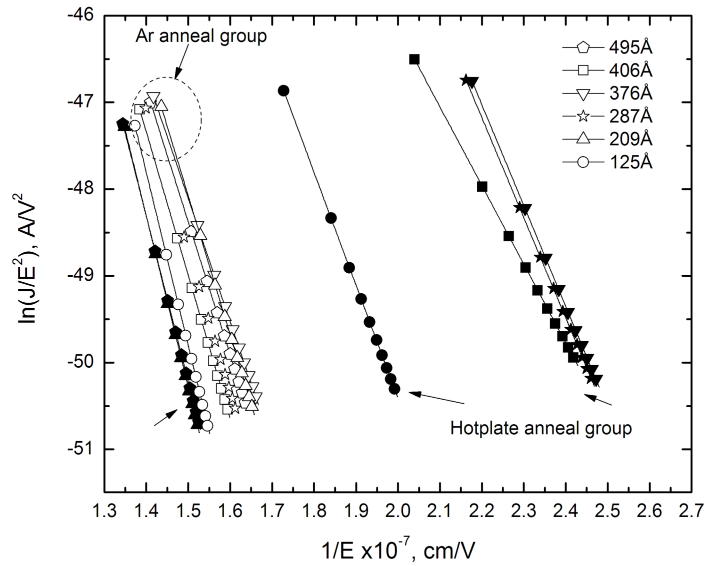
4.5.2. Influence of Dehydration Procedure on Oxide-4H-SiC

The AG IV_EA oxide on 4H-SiC was dehydrated using two methods: on a hotplate at 200^0C for 5 minutes and a rapid thermal processing (RTP) anneal in Ar at 800^0C for 2 minutes. Afterglow IV_EB oxide on 4H-SiC was also dehydrated using a hotplate at 200^0C for one hour and an afterglow Ar anneal at 600^0C for 20 minutes. Following each dehydration method, the experimental Fowler-Nordheim tunneling current was analyzed. The influence of moisture on the electric field in the oxide is demonstrated in Figure 4.22. The random behavior of the voltage, influencing the electric field in the oxide, was attributed to the presence of water molecules absorbed on the surface of the oxide (see Figure 4.22 (b)). The effect of the absorbed moisture was

more prominent on the Fowler-Nordheim slope of the thinnest oxide. This behavior was corrected by the high temperature Ar anneal treatment, which eliminated the error in the measured voltage drop across the oxide for both oxidation processes.



(a)



(b)

Figure 4.22: The influence of a dehydration method on the Fowler-Nordheim plot (a) AG IV_EA and (b) AG IV_EB.

4.5.3. Effective Trapped Charge Distribution

Afterglow IV_EB oxide was used to investigate the trapped charge distribution and determine its centroid within the oxide. After obtaining the Fowler-Nordheim regime, the oxide was given a small charge fluence of 0.12 mC/cm^2 before re-measuring the C-V in each quadrant. The effective trapped charge in the oxide was calculated using Equation 4.6. To further study the influence of trapped charge on the electrical signature of the Fowler-Nordheim plot, the thickness in four quadrants were etch down from: 376 Å to 265 Å; 287 Å to 178 Å; 209 Å to 164 Å; and 125 Å to 79 Å. These oxide thicknesses were subjected to a 5-minute 1:1 (H_2O:HNO_3) diluted nitric clean followed by another 5-minute 1:1 (H_2O:HCL) diluted hydrochloric clean. Between each solution clean, the wafer was rinsed with D.I. water. Afterwards, the wafer was annealed in Ar in the afterglow system for 20 minutes at 600^0C. The same measurement procedure was repeated. In Figure 4.23, the variation of the slopes of the thinner oxides indicated that the distribution of the trapped charge did not appear to be uniformly distributed in the oxide. In addition, etching and cleaning conditions also influenced the Fowler Nordheim characteristic.

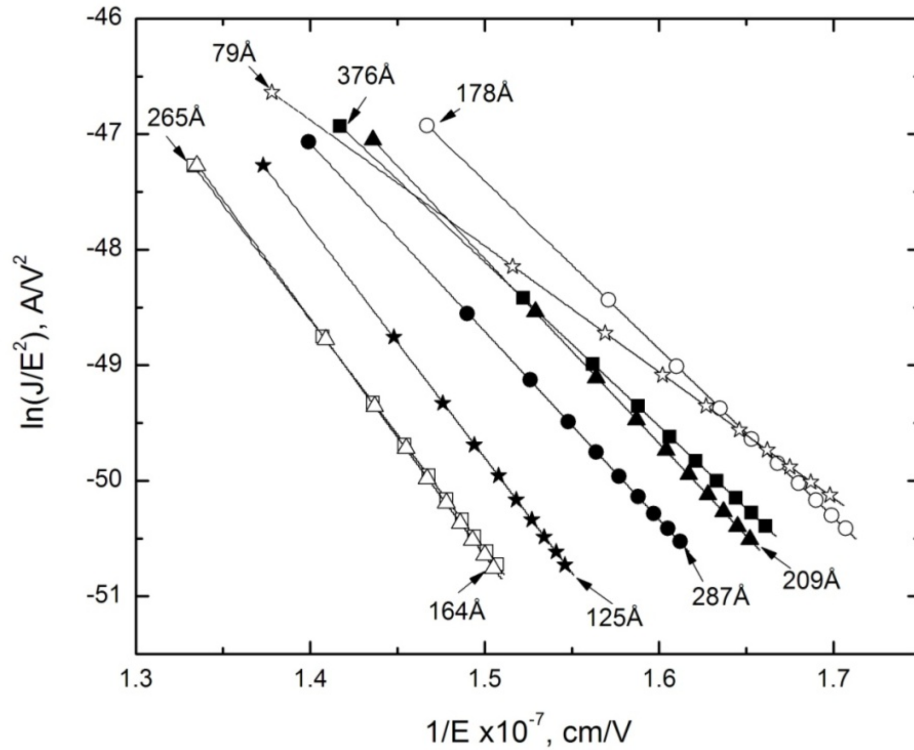


Figure 4.23: Fowler-Nordheim plot of thinner oxides (unfilled geometric shapes) compared to thick oxides (filled geometric shapes).

The thinnest oxide, 79 Å, exhibited a straight line but had a different slope as compared to the thicker oxides. The parallel shifts of the second etched regions indicated the influence of further hydrogenation on the oxide surface. This effect was seen in the distribution of the calculated effective trapped charge. Figure 4.24 illustrates the behavior of the effective trapped charge in the etched AG oxide and un-etched AG oxide.

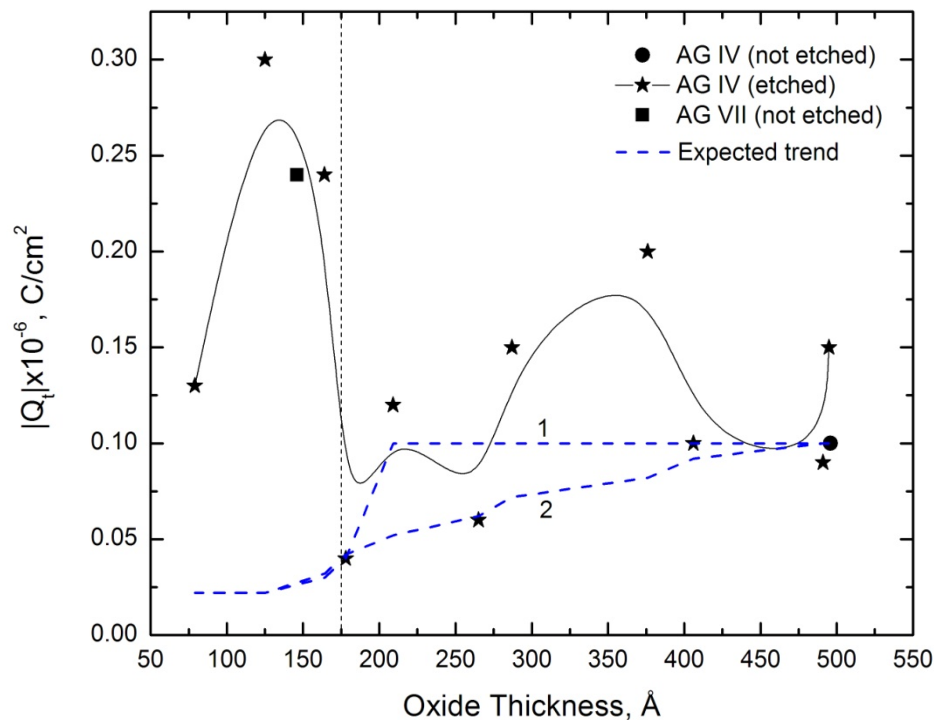


Figure 4.24: Absolute trapped charge versus oxide thickness.

In Figure 4.24, the un-etched 500 Å oxide showed a similar quantity of trapped charges in the oxide. Two possible trends were predicted as thickness decreased. As the thickness was etched back, the density of the trapped charges tends to decrease as the thickness decreased to 175 Å. Below this thickness value, the density of the trapped charge did not follow either of the predicted trends. A higher trapped charge value was also noted for an un-etched 146 Å AG oxide (AG VII). Further investigation to explain this phenomenon for oxide thicknesses less than 175 Å is ongoing. Table 4.8 summarizes the measurement parameters for AG IV_EB such as the flat band voltage, current at the SASS voltage, and the effective trapped charge, in an attempt to explain the trapped charge distribution.

Table 4.8: Effective trapped charge calculation parameters.

Oxide Thickness (Å)	Initial V_{fb} (V)	Final V_{fb}(V)	Q_t ($\mu C/cm^2$)	Initial E_{ox} at V_{SASS} (MV/cm)	Final E_{ox} at V_{SASS} (MV/cm)	F-N current at V_{SASS} ($\mu A/cm^2$)	Final current at V_{SASS} ($\mu A/cm^2$)
495	0.6	2.82	-0.150	6.75	6.73	0.060	0.054
406	0.43	1.57	-0.097	6.90	6.89	0.058	0.057
376	0.53	2.72	-0.200	6.70	6.78	0.064	0.059
287	0.4	1.62	-0.150	6.83	6.91	0.058	0.056
265	0.7	1.18	-0.063	7.21	7.14	0.053	0.051
209	0.38	1.09	-0.120	6.66	6.91	0.056	0.052
178	0.85	1.06	-0.041	6.49	6.98	0.058	0.059
164	0.62	1.75	-0.240	7.20	7.13	0.051	0.056
125	0.38	1.46	-0.300	7.02	6.94	0.050	0.123
79	0.49	0.78	-0.130	6.75	5.95	0.085	0.118

In Table 4.8, although these oxides were subjected to the same charge doses, the initial flat band voltage varied independent of thickness. However, this behavior was not evident before the etching process. The flat band voltage before the etching process was about 0.9 volts on 5 sites of the wafer (center, bottom, top, left, and right). The possible reason for this variation in the flat band voltage is the influence of a hydrogenated oxide surface. The high temperature, Ar anneal, may have left the oxide with shallow trap centers. However, the electric field in the oxide remained at a constant value of ~7 MV/cm before and after stress except for the thinnest oxide region. The increase in the current density after stress, for thicknesses below 175 Å, was attributed to an increase in

the trapped charge density. As a result of this experiment, the trapped charge centroid could not be determined due the influence of unintentional trap creation within the oxide. The influence of these charges was evident through C-V characteristics. Charge trapping and de-trapping effect impacted the accuracy of the contact potential measurement.

4.6. Non-Contact Stress Induced Leakage Current (SILC) Analysis

A controlled ionic current of 8 $\mu A/cm^2$ was used for all measurements. Non-contact stress induced leakage current (SILC) testing was performed to characterize four oxidation process recipes, AGW I, AG I_A, AG II, and AG III. The difference between these recipes was the post-oxidation anneal: AGW I was not annealed; AG I_A included a re-oxidation anneal; AG II included an Ar anneal; and AG III included both a re-oxidation anneal and an Ar anneal. The impact of the process conditions, which included unintentional contamination from the cleaning procedure or from the furnace environmental conditions, was investigated. To obtain statistical data acquisition on an oxide, seventeen test sites were evaluated on the 3-inch diameter substrates (see Figure 4.25).

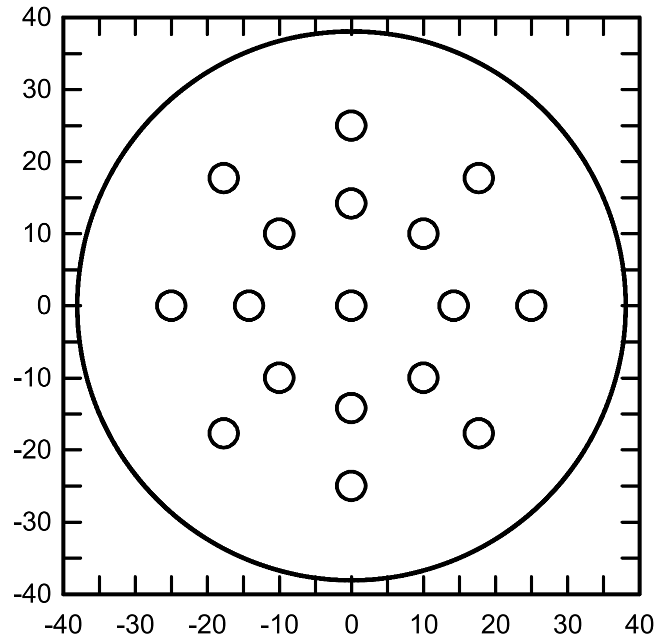


Figure 4.25: Measurement site positions.

4.6.1. Oxidation Process Influence on Leakage Current

The leakage current calculation depended on the oxide thickness, the dielectric constant, and the differentiation of the measured oxide voltage with respect to time (see Equation 2.36). An example of non-contact SILC density versus stress time is shown in Figure 4.26 on a 150 Å thermal oxide grown on Si.

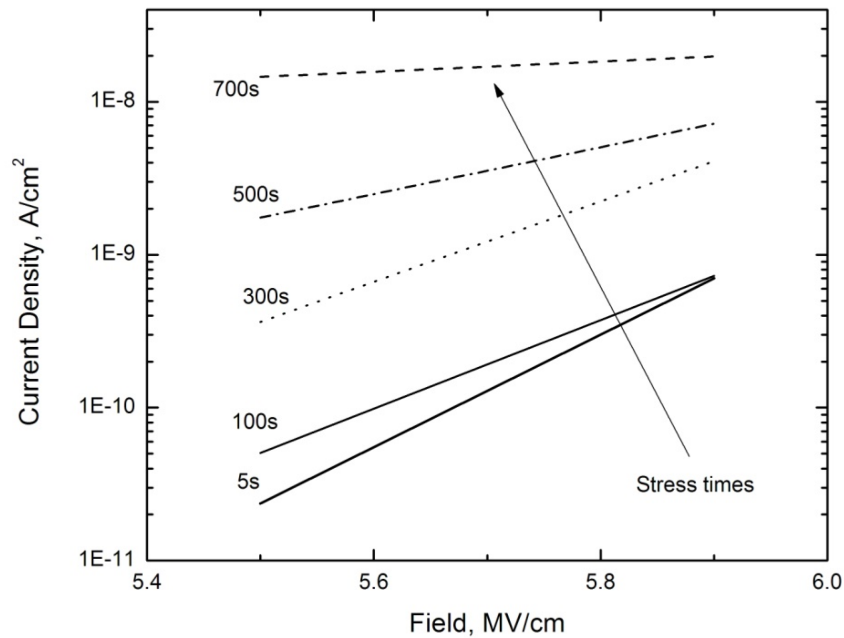


Figure 4.26: Effect of stress fluence on a 150 Å thermal oxide grown on a p-type Si substrate.

In this example, a 150 Å thermal oxide grown on a p-type Si substrate was stressed for 100s and then in three 200s increments. The charge fluence ranged from 0.8 mC/cm^2 to 5.6 mC/cm^2. In Figure 4.26, it was observed that the SILC density increased by two orders of magnitude from the lowest fluence to the highest fluence. The slope of the line is almost horizontal at 700s. This demonstrated the limitation of the corona current source. At this current level, the trap density was at its maximum. However, at a field of 5.9 MV/cm, the difference between the 5s and 100s stress was minimal, indicating that the density of traps was comparable. As the stress fluence increased, the current flowing across the oxide also increased. Therefore, the density of trapped charge was

proportional to the current density. This behavior was expected to occur on AG oxides grown on n-type 4H-SiC substrates.

For non-contact SILC, the leakage current is calculated from the excess current above the Fowler-Nordheim current characteristics. To fit the theoretical Fowler-Nordheim curve with the assumption of M_{ox}= 0.36, the barrier height value was adjusted until the thickness determined from the I-V measurement was fitted to $\pm$5% of the independently measured average EOT value of each oxide. For the AGW I, AG I_A, AG II and AG III oxides, the estimated barrier height value was determined to be 3.1 eV. As a result, the SILC values obtained through this optimization was known as effective SILC values.

4.6.2. Oxide Consistency: Statistical Distribution

Each measurement site was stressed in 100s increments (see Figure 4.27) to observe any trends in the effective SILC characteristics. The normal distribution was used to investigate the effective SILC values. The fluence ranged from 0.8 mC/cm^2 to 3.2 mC/cm^2 assuming a steady calibrated ionic current of 8 μA/cm^2 from the corona source. Figure 4.27 illustrates the typical plot a user sees when selecting each site after the measurement has been performed.

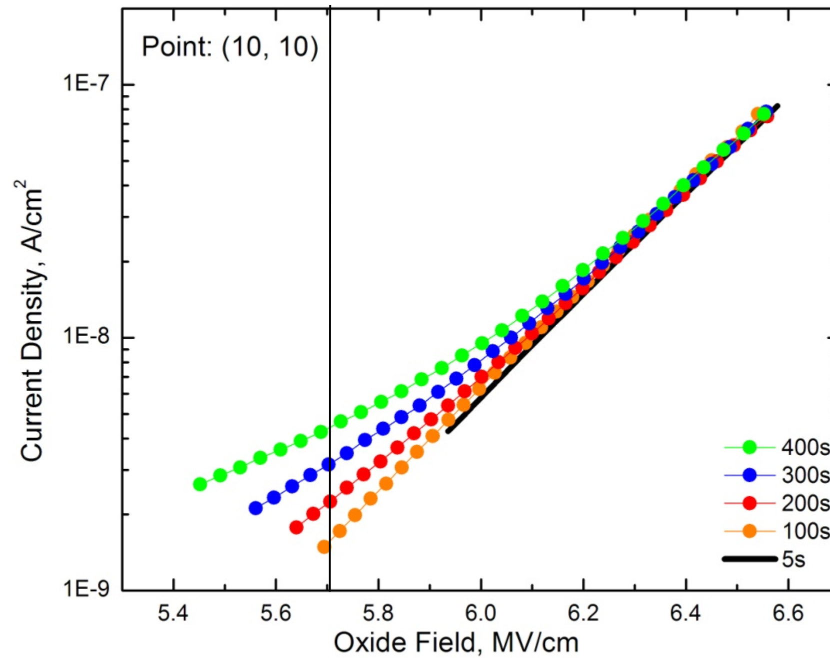


Figure 4.27: Current density versus oxide field at point (10, 10) for AG I_A oxide.

The measurement sequence at each site was as follows: step 1: 5s charge deposition and monitor the contact potential difference for 20 seconds; and step 2: 100s charge deposition and monitor the contact potential difference for 60 seconds. Step two was repeated three more times. Table 4.9 summarized the stress measurement protocol.

Table 4.9: Stress measurement protocol for SILC measurements.

Charge Deposition Time	Cumulative Stress Time
5s	5s (establish F-N conduction)
100s	100s
100s	100s +100s= 200s
100s	200s+ 100s= 300s
100s	300s + 100s= 400s

Once the measurement sequence was completed, the wafer was automatically positioned to another measurement site. For each new site, the measurement sequence was repeated. Figure 4.28 illustrates a typical probability plot with respect to the stress time on AG III oxide taken at 5.7 MV/cm.

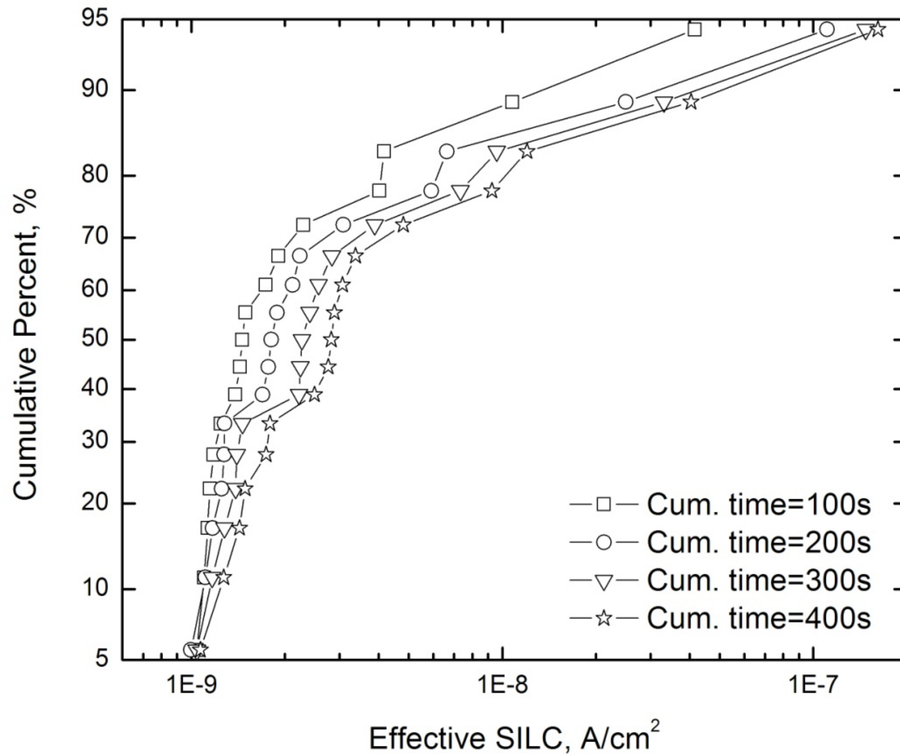


Figure 4.28: Probability plot for AG III oxide at each cumulative time.

In the above figure, there are three straight lines: one below 30%, the second between 30 to 70%, and the third above 80%, which indicated weak areas on the wafer. The leakage current increased two orders of magnitude from the sites within the 30 percentile range to sites within the 80 percentile range. This was attributed to an increase of defects in the as-grown oxide film. Since the differences between the curves were minimal, the data analyzed for each oxide was taken at 400s for each repeatable run.

The electric field chosen to perform data analysis was at 5.7 MV/cm as it encompassed the stressed curves. Each oxidation process run was repeated and analyzed to determine if the effective SILC values were consistent on the same oxidation recipe. These oxidation recipes were repeated at least three times. The same cleaning procedure and oxidation plasma excitation power was kept relatively constant for each run. The first three oxides, AGW I, AG I_A, and AG II, was repeated three times except for AG III which was repeated twice. This was because the microwave power supply was replaced. One of the specifications of the new power supply which differed from the old power supply was the magnetron head. Figure 4.29 shows the probability plot of AGW I oxidation process run repeatability.

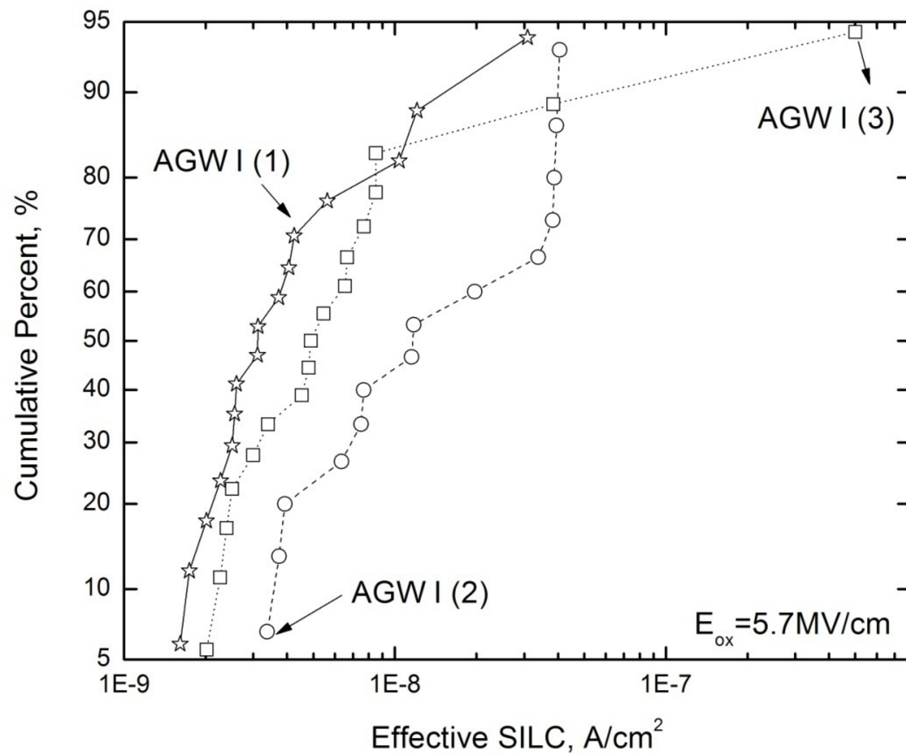


Figure 4.29: Probability plot of AGW I oxidation process run repeatability.

In Figure 4.29, AGW I oxide did not include a post-oxidation anneal. In the first process run, 70% of the wafer sustained a leakage current below $5x10^{-9}$A/cm^2. The second process run had five straight lines in the curve, which indicated that the cleaning procedure was not optimal and unintentional contamination occurred. The third process run was similar to the first process run except for two site areas, which showed a leakage current greater than $1x10^{-8}$ A/cm^2. In summary, the optimum acceptable current for each region was defined at $1x10^{-8}$ A/cm^2. Under this condition, 80% of the wafer sites passed in the first and third process run, and 40% of the wafer sites passed for the second run. Figure 4.30 shows the probability plot for AG I_A oxidation process run repeatability.

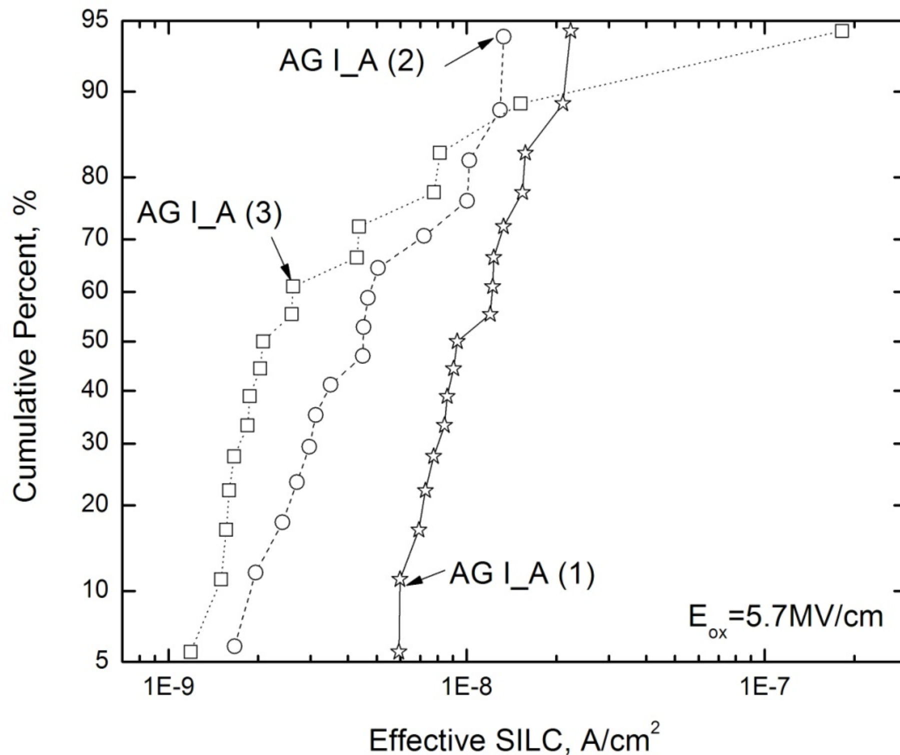


Figure 4.30: Probability plot of AG I_A oxidation process run repeatability.

Figure 4.30 shows the trend for an oxidation process run which included a 60-minute re-oxidation anneal at the same oxidation temperature of 850^0C. Compared to the second and third process runs, the first process run had a higher current density and the leakage current varied slightly throughout the wafer. Subsequent process runs indicated that the cleaning process of the wafer improved. At a current leakage of $1x10^{-8}$ A/cm^2, approximately 80% of the wafer sites passed in process runs two and three, and 50% of the wafer sites passed in the first process run. Although the third process run showed a lower leakage current at 80%, the curve had three "kinks" above 50%. These were attributed to weak spots in the as-grown oxide film. In summary, the re-oxidation anneal did not significantly lower the current leakage throughout the wafer. Figure 4.31 illustrates the probability plot of AG II oxidation process run repeatability.

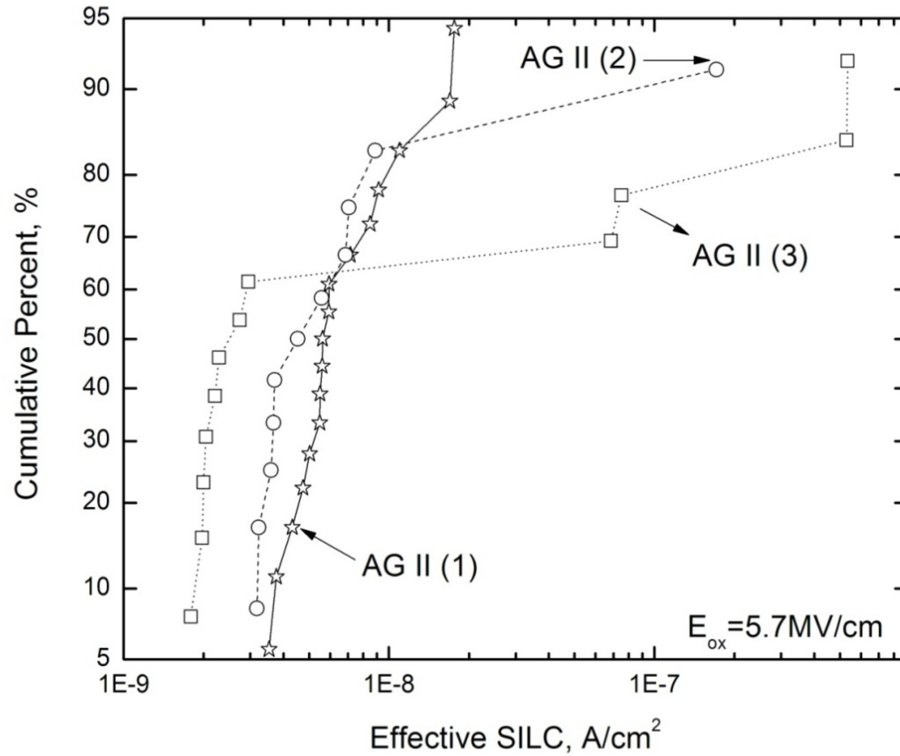


Figure 4.31: Probability plot of AG II oxidation process run repeatability.

In Figure 4.31, this oxidation process included an Ar anneal for one hour at 950^{0}C. All three process runs showed a comparable leakage current below 60% of the measurement sites. Above 60%, the first process run showed approximately a linear increase in the current compared to the others. Leaky sites were attributed to the possibility of unintentional process contamination. In conclusion, similar to the re-oxidation anneal, the high temperature Ar post oxidation anneal showed an improvement in each subsequent processing run within 60% of the wafer area. Finally, Figure 4.32 shows the repeatability of the oxidation process run, which combined both the Ar and re-oxidation post anneal.

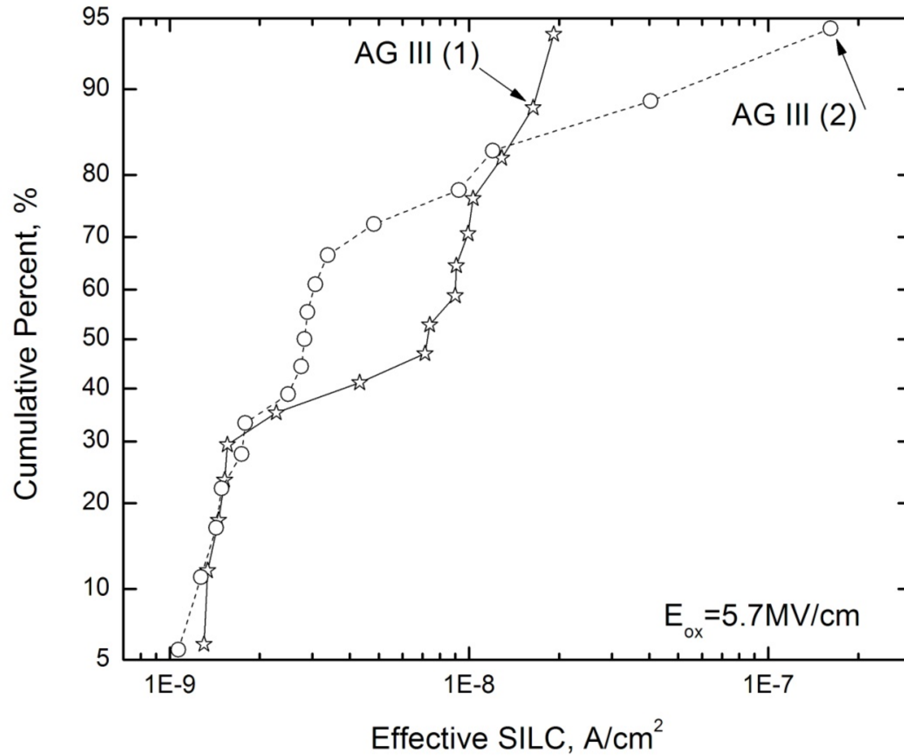


Figure 4.32: Probability plot of AG III oxidation process run repeatability.

In Figure 4.32, 40% of the measurement sites on both process runs sustained a leakage current of $3x10^{-9}$ A/cm^2, which is an improvement compared to the other oxidation processes. However, between 40% and 80%, both process runs showed an opposite density of trap formation, as apparent by the slope of their line. Above 80%, the leakage current increased linearly for both process runs. In summary, this post-oxidation process did not improve the oxide tendency to form defects throughout the wafer.

The repetition of the oxidation process runs showed how non-contact SILC testing can be used to assess the oxidation process conditions and cleaning protocols. Figure 4.33 shows the corresponding sites on the wafers which had leakage currents greater than $1x10^{-7}$ A/cm^2 in these experiments.

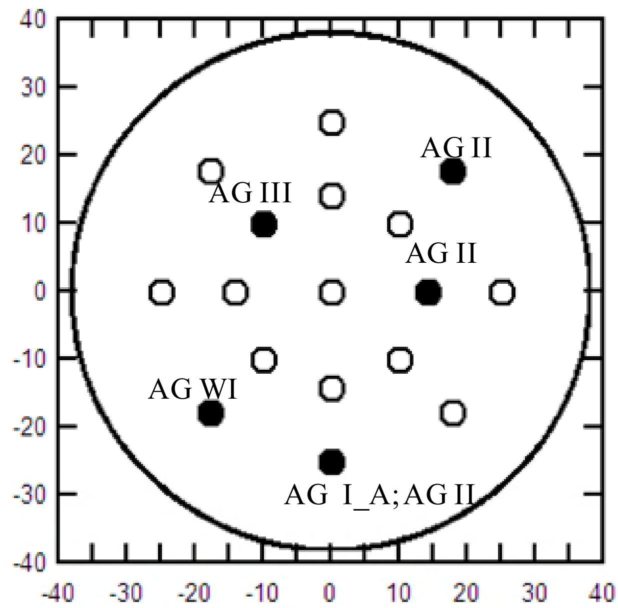


Figure 4.33: Leakage current sites greater than $1x10^{-7}A/cm^2$.

Stricter cleaning protocols were implemented for subsequent oxidation process runs and a standard excited plasma mixture was used to clean the furnace tube prior to loading the wafers for oxidation process runs. Non-contact SILC has the potential to assess the reliability of oxides grown on 4H-SiC substrates.

Chapter 5. Conclusion

5.1. Summary of Research Contributions

Non-contact Corona-Kelvin metrology was used to investigate the charge transport in various oxides grown on n-type 4H-SiC substrates. The measurements used were voltage-charge (V-Q) measurements, capacitance-voltage (C-V) measurements, equivalent oxide thickness (EOT) measurements, charge trapping (Q_t) evaluation measurements, and current-voltage (I-V) measurements.

Variations of afterglow oxides and thermal oxides were compared. After the deposition of a charge fluence of 0.04 mC/cm^2 on the oxide surface, Fowler-Nordheim conduction was identified for the first time. The electric field in the oxide at this regime was greater than 5 MV/cm for thick oxides. The experimental Fowler-Nordheim characteristics compared to the classical Fowler-Nordheim characteristics revealed an offset between the plots.

This offset was greater for thick AG oxides as compared to thermal oxides. The AG oxidation variation parameters influenced the Fowler-Nordheim characteristics. The three dominant variation parameters were the pre-conditioning treatment of the substrate surface prior to oxidation, the oxidation growth time, and the post-oxidation anneal. The offset between AG oxide thicknesses less than 160 Å and the theoretical line in the Fowler-Nordheim plot was marginally reduced. The effective barrier height and the

effective mass in the oxide are the two defining parameters in the current density equation describing the Fowler-Nordheim conduction. The theoretical classical Fowler-Nordheim plot used an effective barrier height of 2.7 eV and an effective mass in the oxide of 0.42m. This effective barrier height value, which represented the conduction band offset at the SiO_2/4H-SiC interface, was independently found using standard photoemission experimentation. The effective mass in the oxide was the common value used in 4H-SiC MOS devices for Fowler-Nordheim analysis.

To fit the experimental data to the effective barrier height of 2.7 eV, the effective mass in the oxide was assumed to be 0.36m. Using this value, the calculated effective barrier height for both thermal and AG oxides was comparable to the calculated effective barrier height value found in literature using 4H-SiC MOS devices. However, this effective mass in the oxide did not correct the offset between the classical Fowler-Nordheim curve and the experimental Fowler-Nordheim curves. As a result, a modified Fowler-Nordheim equation, which accounted for trapped charges and their centroid location within the Fowler-Nordheim tunneling regime, provided a proximate overlay for the thermal oxides but not for the AG oxides. An additional adjustment of the barrier height value of 3.1 eV for the AG oxides was necessary to provide this overlay with a reasonable location of the trapped charge. This result was an indication that the AG oxidation growth method modified the surface of the substrate and the oxide grown could be silicon enriched. Recently, it was found that a 146 Å AG oxide on new 4H-SiC substrate revealed an effective barrier height of 2.75 eV using the EOT optimization parameter.

To further investigate the distribution of the trapped charge and their location in AG oxides, various AG oxide thicknesses, ranging from 490 Å to 79 Å, determined that trapped charges are not uniformly distributed in the oxide. The density of trapped charges increased for oxide thicknesses less than 175 Å indicating that shallow traps are not neutral. These traps influenced the measured voltage drop across the oxide. The electric field in the oxide decreased as a result of these traps. It was determined that hydrogenation of the oxide surface increased the trapped charge density. The source of the hydrogenation of the oxide was from the diluted HF solution. The high temperature Ar anneal possibly led to unintentional surface roughness changes. This post-etching anneal was performed since the hotplate did not completely dehydrate the surface of the oxide. Moisture in the oxide influenced the value of the measured voltage. Determining the exact location of the trapped charge could not be achieved using the etch-back experimental procedure.

Currently, only Fowler-Nordheim data on SiC-based MOS devices have been published in the literature but not SILC data. Non-contact SILC testing only caused area defects in various sites for a particular oxide growth recipe in the absence of fabricated devices. Caution should be taken when defining the Fowler-Nordheim current. As a result, the effective SILC values were reported for a particular oxidation process. Various oxidation process parameters could not be compared with SILC testing because changing the effective barrier height, to fit the thickness determined from I-V measurements to EOT, impacts the electric field in the oxide. Subsequently, the Fowler-Nordheim current characteristic is changed.

Taking this condition into consideration, non-contact SILC revealed the effectiveness of an anneal treatment. Normal probability plots of the effective SILC value variation gave a quick assessment of the oxide reliability. Stress times were proportional to the quantity of the defect formation. Constant corona current testing revealed that this test does not cause destructive breakdown of the oxide. Non-contact C-V, EOT, and SILC show promise to be used for in-line monitoring of as-grown oxide films. Two benefits of applying in-line monitoring techniques to SiC technology are the absence of device fabrication and the quick assessment of an oxide to identify process variations to defect. These techniques may enable the optimization of an oxidation growth process to effectively control oxide reliability, in an attempt to commercialize 4H-SiC-MOS devices.

5.2. Future Work

The location of the trapped charge and it is distribution within the oxide need to be addressed on un-etched thin AG oxides. With this information, the Fowler-Nordheim equation, which includes the effects of trapped charge within the Fowler-Nordheim tunneling regime, should be re-examined. If this set of experiments does not adjust the Fowler-Nordheim experimental curves characteristics to the theoretical curve characteristic, then the Fowler-Nordheim equation should be modified further. The theory to determine the effective mass in the oxide and the image force effect also require further examination. The image force of an electron tunneling through trap centers may decrease the intercept value.

To confirm the structural changes during the AG oxidation of n-type 4H-SiC substrates, X-ray photoelectron spectroscopy (XPS), which measures the elemental composition of a surface, should be performed on AG oxide films. If AG oxidation of 4H-SiC is lightly nitrated, then it would further support the increase of the effective barrier height value. It has been reported that SiO_2 containing nitrogen grown on silicon varied the effective barrier height and the effective mass in the oxide [93]. Also, sequential oxidation process runs should be performed with variation of oxidation parameters to improve AG oxide reliability, such as surface pre-conditioning, oxidation chemistry, and post-oxidation anneal. Longer and higher temperature post-oxidation anneals may result in the reduction of shallow trap charges in the oxide. This post-oxidation anneal treatment may provide an effective barrier height close to 2.7 eV.

Statistical acquisition of dielectrics grown on 4H-SiC using non-contact SILC assessment can be used to acquire fundamental information about the oxide-substrate interface. Reliability curves can be developed from various dielectrics to compare different oxidation process parameters.

References

[1] M. A. Alam, "SILC as a measure of trap generation and predictor of T_{BD} in ultrathin oxides," *IEEE Trans. Electron Devices,* vol. 49, pp. 226-231, 2002.

[2] D. J. Dumin and J. R. Maddux, "Correlation of stress-induced leakage current in thin oxides with trap generation inside the oxides," *IEEE Trans. Electron Devices,* vol. 40, pp. 986-993, 1993.

[3] D. J. Dumin, *Oxide Reliability : A Summary of Silicon Oxide Wearout, Breakdown, and Reliability.* New Jersey: World Scientific, 2002.

[4] R. Moazzami and C. Hu, "Stress-induced current in thin silicon dioxide films," in *International Technical Digest on Electron Devices Meeting,* 1992, pp. 139-142.

[5] M. Wilson, J. Lagowski, A. Savtchouk, D. Marinskiy and L. Jastrzebski, "Study of stress-induced leakage current in thin oxides stressed by corona charging in air: relationship to GOI defects," *Mater. Res. Soc. Symp. Proc.,* vol. 592, pp. 345-350, 2000.

[6] E. Rosenbaum and L. F. Register, "Mechanism of stress-induced leakage current in MOS capacitors," *IEEE Trans. Electron Devices,* vol. 44, pp. 317-323, 1997.

[7] E. F. Runnion, S. M. Gladstone, R. S. Scott Jr., D. J. Dumin, L. Lie and J. C. Mitros, "Thickness dependence of stress-induced leakage currents in silicon oxide," *IEEE Trans. Electron Devices,* vol. 44, pp. 993-1001, 1997.

[8] D. J. Dimaria, "Defect production, degradation, and breakdown of silicon dioxide films," *Solid-State Electron.,* vol. 41, pp. 957-965, 1997.

[9] S. Holland, I. C. Chen, T. P. Ma and C. Hu, "On physical models for gate oxide breakdown," *IEEE Electron Device Lett.,* vol. 5, pp. 302-305, 1984.

[10] S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo and C. H. Tung, "Dielectric breakdown mechanisms in gate oxides," *J. Appl. Phys.,* vol. 98, pp. 121301-1-121301-36, 2005.

[11] J. H. Stathis, "Reliability limits for the gate insulator in CMOS technology," *IBM J. Res. Develop.,* vol. 46, pp. 265-286, 2002.

[12] O. Kordina and S. E. Saddow, "Silicon carbide overview," in *Advances in Silicon Carbide Processing and Applications* S. E. Saddow and A. Agarwal, Eds. Boston: Artech House, 2004, pp. 1-27.

[13] R. Madar, "Silicon carbide in contention," *Nature,* vol. 430, pp. 974-975, 2004.

[14] J. A. Cooper Jr., "Silicon carbide MOSFETs," in *Wide Energy Bandgap Electronic Devices* F. Ren and J. C. Zolper, Eds. Singapore: World Scientific Publishing Co., 2003, pp. 339-394.

[15] H. O. Olafsson, "Detection and removal of traps at the SiO_2/SiC interface," *Ph. D. Dissertation, Chalmers University of Technology,* 2004.

[16] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: John Wiley & Sons, Inc., 1981.

[17] Y. Song, S. Dhar, L. C. Feldman, G. Chung and J. R. Williams, "Modified Deal Grove model for the thermal oxidation of silicon carbide," *J. Appl. Phys.,* vol. 95, pp. 4953-4957, 2004.

[18] I. Vickridge, J. Ganem, Y. Hoshino and I. Trimaille, "Growth of SiO_2 on SiC by dry thermal oxidation: mechanism," *J. Phys. D: Appl. Phys.,* vol. 40, pp. 6254-6263, 2007.

[19] C. Raynaud, "Silica films on silicon carbide: a review of electrical properties and device applications," *J. Non-Cryst. Solids,* vol. 280, pp. 1-31, 2001.

[20] C. I. Harris and V. V. Afanas'ev, "SiO_2 as an insulator for SiC devices," *Microelectron. Eng.,* vol. 36, pp. 167-174, 1997.

[21] J. M. Knaup, P. Deak, T. Frauenheim, A. Gali, Z. Hajnal and W. J. Choyke, "Theoretical study of the mechanism of dry oxidation of 4H-SiC," *Phys. Rev. B,* vol. 71, pp. 235321-1-235321-9, 2005.

[22] M. Losurdo, M. M. Giangregorio, P. Capezzuto, G. Bruno, A. S. Brown, T. Kim and C. Yi, "Modification of 4H-SiC and 6H-SiC $(0001)_{Si}$ Surfaces through the interaction with atomic hydrogen and nitrogen," *J. Electron. Mater.,* vol. 34, pp. 457-465, 2005.

[23] M. Bassler, G. Pensl and V. V. Afanas'ev, ""Carbon cluster model" for electronic states at SiC/SiO_2 interfaces," *Diamond Relat. Mater.,* vol. 6, pp. 1472-1475, 1997.

[24] B. E. Deal, "Standardized terminology for oxide charges associated with thermally oxidized silicon," *IEEE Trans. Electron Devices,* vol. 27, pp. 606-608, 1980.

[25] D. Brisbin and Q. Wang. (2002, Evaluating oxide reliability with V-ramp and J-ramp testing. [http://archive.evaluationengineering.com/archive/articles/0802wafer.htm].

[26] J. T. Yue, "Reliability," in *ULSI Technology* C. Y. chang and S. M. Sze, Eds. New York, NY: McGraw-Hill, 1996, pp. 656-704.

[27] F. Jensen, *Electronic Component Reliability : Fundamentals, Modelling, Evaluation, and Assurance.* Chichester, England;: John Wiley & Sons Ltd., 1995.

[28] S. Chakraborty, M. K. Bera, S. Bhattacharya and C. K. Maiti, "Current conduction mechanism in TiO_2 gate dielectrics," *Microelectron. Eng.,* vol. 81, pp. 188-193, 2005.

[29] W. R. Harrell and J. Frey, "Observation of Poole–Frenkel effect saturation in SiO_2 and other insulating films," *Thin Solid Films,* vol. 352, pp. 195-204, 1999.

[30] R. H. J. Good and E. W. Muller, "Field emission," in *Encyclopedia of Physics: Electron-Emission Gas Discharge I* , vol. 21, S. Flugge, Ed. Berlin: Springer-Verlag, 1956, pp. 176-231.

[31] J. M. Houston, "The slope of logarithmic plots of the Fowler Nordheim equation," *Phys. Rev.,* vol. 88, pp. 349, 1952.

[32] R. A. Ashton, "Gate oxide thickness measurement using Fowler-Nordheim tunneling," *Proc. IEEE Int. Conf. Microelectron. Test Struct.,* vol. 4, pp. 57-60, 1991.

[33] D. K. Schroder, "Oxide and interface trapped charges, oxide integrity," in *Semiconductor Material and Device Characterization* ,2nd ed.Anonymous New York: John Wiley & Sons, Inc., 1998, pp. 337-419.

[34] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2," *J. Appl. Phys.,* vol. 40, pp. 278-283, 1969.

[35] Z. A. Weinberg, "On tunneling in metal-oxide-silicon structures," *J. Appl. Phys.,* vol. 53, pp. 5052-5056, 1982.

[36] M. Depas, B. Vermeire, P. W. Mertens, R. L. Van Meirhaeghe and M. M. Heyns, "Determination of tunneling parameters in ultra-thin oxide layer poly-Si/SiO2/Si structures," *Solid-State Electron.,* vol. 38, pp. 1465-1471, 1995.

[37] C. Y. Ng, T. P. Chen, Y. Liu and C. Q. Sun, "Influence of nitrogen on tunneling barrier heights and effective masses of electrons and holes at lightly-nitrided SiO_2/Si interface," *Journal of Applied Physics,* vol. 96, pp. 5912-5914, 2004.

[38] R. Williams and M. H. Woods, "High electric fields in silicon dioxide produced by corona charging," *J. Appl. Phys.,* vol. 44, pp. 1026-1028, 1973.

[39] Z. A. Weinberg, W. C. Johnson and M. A. Lampert, "High-field transport in SiO_2 on silicon induced by corona charging of the unmetallized surface," *J. Appl. Phys.,* vol. 47, pp. 248-255, 1976.

[40] Z. A. Weinberg, "Tunneling of electrons from Si into thermally grown SiO_2," *Solid-State Electron.,* vol. 20, pp. 11-18, 1977.

[41] J. H. Chen, C. T. Wei, S. M. Hung, S. C. Wong and Y. H. Wang, "Breakdown and stress-induced oxide degradation mechanisms in MOSFETs," *Solid-State Electron.,* vol. 46, pp. 1965-1974, 2002.

[42] T. Tomita, H. Utsunomiya, T. Sakura, Y. Kamakura and K. Taniguchi, "A new soft breakdown model for thin thermal SiO_2 films under constant current stress," *IEEE Trans. Electron Devices,* vol. 46, pp. 159-164, 1999.

[43] D. J. DiMaria, E. Cartier and D. Arnold, "Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon," *J. Appl. Phys.,* vol. 73, pp. 3367-3384, 1993.

[44] Y. Chen, J. S. Suehle, C. Shen, J. B. Bernstein, C. Messick and P. Chaparala, "A new technique for determining long-term TDDB acceleration parameters of thin gate oxides," *IEEE Electron Device Lett.,* vol. 19, pp. 219-221, 1998.

[45] J. H. Stathis, "Percolation models for gate oxide breakdown," *J. Appl. Phys.,* vol. 86, pp. 5757-5766, 1999.

[46] I. C. Chen and C. Hu, "Accelerated testing of time-dependent breakdown of SiO_2," *IEEE Electron Device Lett.,* vol. 8, pp. 140-142, 1987.

[47] W. Nelson, *Accelerated Testing: Statistical Models, Test Plans, and Data Analyses.* New York: Wiley-Interscience Publication, 1990.

[48] E. Persson, "Analysis of reliability test failure data: data processing and presentation," (private communication), 2006.

[49] J. Senzaki, K. Kojima and K. Fukuda, "Effects of n-type 4H-SiC epitaxial wafer quality on reliability of thermal oxides," *Appl. Phys. Lett.,* vol. 85, pp. 6182-6184, 2004.

[50] J. Senzaki, K. Kojima, T. Kato, A. Shimozato and K. Fukuda, "Correlation between reliability of thermal oxides and dislocations in n-type 4H-SiC epitaxial wafers," *Appl. Phys. Lett.,* vol. 89, pp. 022909-1-022909-3, 2006.

[51] M. M. Maranowski and J. A. Cooper Jr., "Time-dependent-dielectric-breakdown measurements of thermal oxides," *IEEE Trans. Electron Devices,* vol. 46, pp. 520-524, 1999.

[52] K. Matocha, G. Dunne, S. Soloviev and R. Beaupre, "Time-dependent dielectric breakdown of 4H-SiC MOS capacitors and DMOSFETs," *IEEE Trans. Electron Devices,* vol. 55, pp. 1830-1834, 2008.

[53] D. J. DiMaria and E. Cartier, "Mechanism for stress-induced leakage currents in thin silicon dioxide films," *J. Appl. Phys.,* vol. 78, pp. 3883-3894, 1995.

[54] J. De Blauwe, J. Van Heudt, D. Wellekens, G. Groeseneken and H. E. Maes, "SILC-related effects in flash E^2PROM's-Part I: a quantitative model for steady-state SILC," *IEEE Trans. Electron Devices,* vol. 45, pp. 1745-1750, 1998.

[55] B. De Salvo, G. Ghibaudo, G. Panabnakakis, B. Guillaumo and G. Reimbold, "Study of stress induced leakage current by using high resolution measurements," *Microelectron. Reliab.,* vol. 39, pp. 797-802, 1999.

[56] M. P. Houng, Y. H. Wang and W. J. Chang, "Current transport mechanism in trapped oxides: a generalized trap-assisted tunneling model," *J. Appl. Phys.,* vol. 86, pp. 1488-1491, 1999.

[57] D. Ielmini, A. S. Spinelli, A. L. Lacaita, A. Martinelli and G. Ghidini, "A recombination- and trap-assisted tunneling model for stress-induced leakage current," *Solid-State Electron.,* vol. 45, pp. 1361-1369, 2001.

[58] K. Sakakibara, N. Ajika, M. Hatanaka, H. Miyoshi and A. Yasuoka, "Identification of stress-induced leakage current components and the corresponding trap models in SiO_2 films," *IEEE Trans. Electron Devices,* vol. 44, pp. 2267-2273, 1997.

[59] L. Pantisano and K. P. Cheung, "Stress-induced leakage current (SILC) and oxide breakdown: are they from the same oxide traps?" *IEEE Trans. Device Mater. Reliab.,* vol. 1, pp. 109-112, 2001.

[60] M. H. Woods and R. Williams, "Injection and removal of ionic charge at room temperature through the interface of air with SiO_2," *J. Appl. Phys.,* vol. 44, pp. 5506-5510, 1973.

[61] S. Sakata, M. Inoue, T. Kushima and T. Okada, "Formation of clusters from clean room air by corona discharge," in *The 39Th Annual Technical Meeting of Institute of Environmental Sciences,* 1993, pp. 79-86.

[62] M. Pavlik and J. D. Skalny, "Generation of $[H_3O]^+(H_2O)_n$ clusters by positive corona discharge in air," *Rapid Commun. Mass Spectrom.,* vol. 11, pp. 1757-1766, 1997.

[63] J. D. Skalny, T. Mikoviny, S. Matejcik and N. J. Mason, "An analysis of mass spectrometric study of negative ions extracted from negative corona discharge in air," *Int. J. Mass Spectrom.,* vol. 233, pp. 317-324, 2004.

[64] J. Lagowski, M. Wilson and A. Savtchouk, "Method for measuring stress induced leakage current and gate dielectric integrity using corona discharge," US Patent 6538462B1, Mar. 25, 2003.

[65] A. Savtchouk, J. Lagowski, J. D'Amico, M. Wilson and L. Jastrzebski, "Steady state method for measuring the thickness and the capacitance of ultrathin dielectric in the presence of substantial leakage current," US Patent 668062 B2, Jan. 20, 2004.

[66] M. Wilson, J. Lagowski, L. Jastrzebski, A. Savtchouk and V. Faifer, "COCOS (corona oxide characterization of semiconductor) non-contact metrology for gate dielectrics," in *Characterization and Metrology for ULSI Technology,* 2001, pp. 220-225.

[67] M. Wilson, J. Lagowski, A. Savtchouk, D. Marinskiy, L. Jastrzebski and J. D'Amico, "COCOS (corona oxide characterization of semiconductor) metrology: physical principles and applications," in *Gate Dielectric Integrity: Material, Process, and Tool Qualification* D. C. Gupta and G. A. Brown, Eds. ASTM STP1382 West Conshohocken, Pa., 1999, pp. 74-90.

[68] J. D'Amico, "Thin Silicon Dioxide Integrity: Advanced Techniques," *Ph. D. Dissertation, University of South Florida,* 2000.

[69] P. Edelman, J. Lagowski, A. Savtchouk, M. Wilson, A. Aleynikov, D. Marinskiy and J. Navarro, "Full wafer non-contact mapping of electrical properties of ultra-thin advanced dielectrics on Si," *Mater. Sci. Eng. , B,* vol. 91-92, pp. 211-215, 2002.

[70] Semiconductor Diagnostics Inc. [http://www.sditampa.com].

[71] P. Edelman, D. Marinskiy, C. Almeida, J. N. Kochey, A. Byelyayev, M. Wilson, A. Savtchouk, J. D'Amico, A. Findlay, L. Jastrzebski and J. Lagowski, "Non-contact charge-voltage method for dielectric characterization on small test areas of IC product wafers," *Mater. Sci. Semicond. Process.,* vol. 9, pp. 252-256, 2006.

[72] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology.* New York: Wiley-Interscience Publication, 1982.

[73] B. V. Zeghbroeck. (2004, *Principles of Semiconductor Devices.* [http://ece-www.colorado.edu/~bart/book/].

[74] M. S. Dautrich, P. M. Lenahan, A. Y. Kang and J. Conley J.F., "Noninvasive nature of corona charging on thermal Si/SiO_2 structures," *Appl. Phys. Lett.,* vol. 85, pp. 1844-1845, 2004.

[75] A. M. Hoff, E. Oborina, S. E. Saddow and A. Savtchouk, "Thermal oxidation of 4H-silicon carbide using the afterglow method," *Mater. Sci. Forum,* vol. 457-460, pp. 1349-1352, 2004.

[76] P. Edelman, M. Wilson, J. D'Amico, A. Savtchouk and J. Lagowski, "Band offset diagnostic of advanced dielectrics," *J. Mater Sci: Mater Electron,* vol. 19, pp. 73-78, 2008.

[77] A. M. Hoff, "Growth and metrology of silicon oxides on silicon carbide," *Mater. Res. Soc. Symp. Proc.,* vol. 815, pp. 189-198, 2004.

[78] J. D'Amico, "Theory and application of non-contact methods for in-line reliability determination," in Integrated Reliability Workshop Final Report, 2003 IEEE International, pp.157-168.

[79] W. Kern and D. A. Puotinen, "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology," *RCA Rev.,* vol. 31, pp. 187, 1970.

[80] A. Savtchouk, E. Oborina, A. M. Hoff and J. Lagowski, "Non-contact doping profiling in epitaxial SiC," *Mater. Sci. Forum,* vol. 457/460, pp. 755-758, 2004.

[81] V. V. Afanas'ev, M. Bassler, G. Pensl, M. J. Schulz and E. S. von Kamienski, "Band offsets and electronic structure of SiC/SiO_2 interfaces," *J. Appl. Phys.,* vol. 79, pp. 3108-3114, 1996.

[82] H. Yamada, "Additional fluorine passivation to pyrolytic-N_2O passivated ultrathin silicon oxide/Si(100) films," *J. Appl. Phys.,* vol. 100, pp. 034507-1-034507-7, 2006.

[83] R. K. Chanana, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, J. R. Williams and R. A. Weller, "Fowler-Nordheim hole tunneling in p-SiC/SiO_2 structures," *Appl. Phys. Lett.,* vol. 77, pp. 2560-2562, 2000.

[84] P. Friedrichs, E. P. Burte and R. Schomer, "Dielectric strength of thermal oxides on 6H-SiC and 4H-SiC," *Appl. Phys. Lett.,* vol. 65, pp. 1665-1667, 1994.

[85] H. Li, S. Dimitrijev, D. Sweatman and H. B. Harrison, "Analysis of Fowler–Nordheim injection in NO nitrided gate oxide grown on n-type 4H–SiC," *Microelectron. Reliab.,* vol. 40, pp. 283-286, 2000.

[86] R. Waters and B. V. Zeghbroeck, "Temperature-dependent tunneling through thermally grown SiO_2 on n-type 4H- and 6H-SiC," *Appl. Phys. Lett.,* vol. 76, pp. 1039-1041, 2000.

[87] A. K. Agarwal, S. Seshadri and L. B. Rowland, "Temperature dependence of Fowler-Nordheim current in 6H- and 4H-SiC MOS capacitors," *IEEE Electron Device Lett.,* vol. 18, pp. 592-594, 1997.

[88] B. Brar, G. D. Wilk and A. C. Seabaugh, "Direct extraction of the electron tunneling effective mass in ultrathin SiO_2," *Appl. Phys. Lett.,* vol. 69, pp. 2728-2730, 1996.

[89] R. Kies, T. Egilsson, G. Ghibaudo and G. Pananakakis, "A method for the assessment of oxide charge density and centroid in metal-oxide-semiconductor structures after uniform gate stress," *Appl. Phys. Lett.,* vol. 68, pp. 3790-3792, 1996.

[90] C. Papadas, P. Morfouli, G. Ghibaudo and G. Pananakakis, "Analysis of the trapping characteristics of silicon dioxide after Fowler-Nordheim degradation," *Solid-State Electron.,* vol. 34, pp. 1375-1379, 1991.

[91] S. J. Oh and Y. T. Yeow, "Voltage shifts of Fowler-Nordheim tunneling J-V plots in thin gate oxide MOS structures due to trapped charges," *Solid-State Electron.,* vol. 32, pp. 507-511, 1989.

[92] J.A. Lopez-Villanueva, J.A. Jimenez-Tejada, P. Cartujo, J. Bausells, and J.E. Carceller, "Analysis of the effects of constant-current Fowler-Nordheim-tunneling injection with charge trapping inside the potential barrier," *J. Appl. Phys.*, vol. 70, pp. 3712-3720, 1991.

[93] L. F. Mao, Z. O. Wang, J. Y. Wang and G. Y. Yang, "The effective mass issues in light nitride silicon oxide," *Semicond. Sci. Technol.,* vol. 20, pp. 1078-1082, 2005.

Appendices

Appendix A: Afterglow Oxide Recipes

Table A.1: AG I_A Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
6	ReOx Anneal	850	O_2 : N_2O : FG (3:0.2:0.5)	60	
7	Ramp Down	850 to 600	Ar (0.23)	75	
8	Unload	600	N_2 (10)	5	

Table A.2: AG I_B Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	40	Yes
6	ReOx Anneal	850	O_2 : N_2O : FG (3:0.2:0.5)	25	
7	Ramp Down	850 to 740	Ar (0.23)	5	
8	Unload	740	N_2 (10)	5	

Appendix A (Continued)

Table A.3: AG II Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
6	Ramp Up	850 to 950	Ar (0.23)	24	
7	Ar Anneal	950	Ar (0.23)	60	
8	Ramp Dow	950 to 600	Ar (0.23)	90	
9	Unload	600	N_2 (10)	5	

Table A.4: AG III Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
6	ReOx Anneal	850	O_2 : N_2O : FG (3:0.2:0.5)	60	
7	Ramp Up	850 to 950	Ar (0.23)	24	
8	Ar Anneal	950	Ar (0.23)	60	
9	Ramp Down	950 to 600	Ar (0.23)	90	
10	Unload	600	N_2 (10)	5	

Appendix A (Continued)

Table A.5: AG IV Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
6	Ramp Up	850 to 950	O_2 : FG (3:1)	20	
7	ReOx Anneal	950	O_2 : FG (3:1)	120	
8	Ramp Down	950 to 600	Ar (0.23)	90	
9	Unload	600	N_2 (10)	5	

Table A.6: AG V Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
6	Ramp Up	850 to 900	O_2 : N_2O : FG (3:0.2:0.5)	10	
7	ReOx Anneal	900	O_2 : N_2O : FG (3:0.2:0.5)	360	
8	Ramp Down	900 to 600	Ar (0.23)	90	
9	Unload	600	N_2 (10)	5	

Table A.7: AG VI Recipe.

Interval	Description	Temp (^{0}C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
6	Ramp Up	850 to 950	O_2 : N_2O (4:0.3)	20	
7	ReOx Anneal	950	O_2 : N_2O (4:0.3)	120	
8	Ramp Down	950 to 600	Ar (0.23)	90	
9	Unload	600	N_2 (10)	5	

Appendix A (Continued)

Table A.8: AG VII Recipe.

Interval	Description	Temp (^{0}C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	7	Yes
6	Ar Anneal	850	Ar (0.23)	60	
7	Ramp Down	850 to 600	Ar (0.23)	75	
8	Unload	600	N_2 (10)	5	
	HF Vapor Etch				
9	Load	600	N_2 (10)	5	
10	Ar Anneal	600	Ar (0.23)	20	
11	Unload	600	N_2 (10)	5	

Table A.9: AGW I Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
6	Ramp Down	850 to 600	Ar (0.23)	75	
7	Unload	600	N_2 (10)	5	

Table A.10: AGW II Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 850	Ar (0.23)	38	
3	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	90	Yes
4	Ramp Down	850 to 600	Ar (0.23)	75	
5	Unload	600	N_2 (10)	5	

Table A.11: AGW III Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	10	Yes
6	Unload	850	N_2 (10)	5	

Appendix A (Continued)

Table A.12: AGW IV Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	Ramp Up	600 to 850	Ar (0.23)	38	
4	Oxidation	850	O_2 : N_2O : FG (3:0.2:0.5)	10	Yes
5	Unload	850	N_2 (10)	5	

Table A.13: AGW V Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (3:0.2:1)	90	Yes
6	Ramp Down	850 to 600	Ar (0.23)	75	
7	Unload	600	N_2 (10)	5	

Appendix A (Continued)

Table A.14: AGW VI Recipe.

Interval	Description	Temp (^0C)	Gas Flow (l/min)	Time (min)	Excited Media
1	Load	400	N_2 (10)	5	
2	Ramp Up	400 to 600	O_2 : N_2 (0.5:3.5)	28	
3	FG Pre-treatment	600	FG (4)	20	Yes
4	Ramp Up	600 to 850	Ar (0.23)	38	
5	Oxidation	850	O_2 : N_2O : FG (2.5:0.15:1.3)	90	Yes
6	Ramp Down	850 to 600	Ar (0.23)	75	
7	Unload	600	N_2 (10)	5	

About the Author

Helen Benjamin was born on the Caribbean island of Martinique. She attended Sts. Peter and Paul High School in St. Thomas, U.S. Virgin Islands, where she graduated as the Valedictorian of her class. She began her college education at the University of the Virgin Islands in Mathematics. After one year, she transferred to the University of South Florida, Tampa, FL, where she received her Bachelor of Science and Masters of Science in Electrical Engineering. During the pursuit of her Doctoral degree, she received three prestigious awards: the Alfred P. Sloan Foundation Scholarship Award, the Integrative Graduate Education and Research Traineeship (IGERT) Award, and the National Science Foundation (NSF) Graduate Research Fellowship Award. She gained teaching experience by being a laboratory instructor for the Integrated-Circuit (IC) Processing Lab for a year. She authored one publication in *Sensors and Actuators B* and co-authored publications related to this dissertation and her Master's thesis.