

**A highly flexible stimulator for a high  
acuity retinal prosthesis implemented in  
65 nm CMOS process**

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## Abstract

This thesis presents a design of a flexible stimulator in 65 nm Complementary Metal Oxide Semiconductor (CMOS) as part of a 1024-electrode epiretinal prosthesis to restore partial vision in patients suffering from eye diseases such as retinitis pigmentosa (RP) and age-related macular degradation (AMD).

The stimulator design is to support as many different stimulation strategies as possible. In particular, a wide variety of current amplitudes and stimulation frequencies is called for. Bipolar as well as monopolar stimulation strategies are also catered for. The selection of electrodes is fully flexible where any electrodes and any number of them can be selected as active or return at any time slice. The separation of image data update rate and stimulation refresh rate helps reduce data bandwidth by a half, which is very beneficial because the bandwidth for the data receiver of the stimulator chip is limited to 300 kHz in Medical Implant Communication Service (MICS) band.

A distributed design where data is mainly processed at the local controller of every electrode driver simplifies signal routing, which is critical when the number of electrodes goes up to 1024. Global controlling circuits which help realizing some of the flexibility were designed, fabricated and tested with good performance.

A novel electrode driver topology was proposed. Each electrode is controlled by its own driver, which helps selecting electrodes independently. The proposed electrode driver allows its electrode to act as active or return. The novel electrode driver operates in an alternately push-pull manner where only one current sink or source works at a time when doing stimulation. This results in a reduction of headroom voltage by a half, or equivalently more voltage can be used for stimulation, which is extremely advantageous as the maximum supply voltage of the implemented 65 nm CMOS process is limited to 3.3V.

In order to verify the feasibility of the flexibility in terms of the ability of circuit implementation and power consumption, a prototype stimulator with 64 outputs was designed, fabricated, and tested. This prototype stimulator supports all the targeted stimulation flexibility. The verification of this prototype stimulator is a very useful and

important preparation stage in designing a fully integrated high acuity epiretinal stimulator. The prototype stimulator was extensively tested and expected performance has been achieved. The power consumption of the prototype stimulator is 400  $\mu\text{W}$  excluding the stimulus power, which makes the power consumption of the ultimate 1024-electrode stimulator just a few mW.



## Declaration

This is to certify that:

1. The thesis comprises only my original work towards the PhD.
2. Due acknowledgement has been made in the text to all other materials used.
3. The thesis is less than 100,000 words in length, exclusive of tables, maps, bibliographies and appendices.

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## Abbreviations

<b>Abbreviation</b>	<b>Full text</b>
AMD	Age-related Macular Degeneration
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CPGA	Ceramic Pin Grid Array
CRC	Cyclic Redundant Check
DAC	Digital to Analog Converter
DAQ	Data Acquisition device
DFP	D-type Flip Flop
DNL	Differential Non-linearity
ESD	Electrostatic Discharge
GND	Ground
IBM	International Business Machines
IC	Integrated Circuit
INL	Integral Non-linearity
LabVIEW	Laboratory Virtual Instrumentation Engineering Workbench
LSB	Least Significant Bit
MICS	Medical Implant Communication Service
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
NI	National Instruments
PCB	Printed Circuit Board
RP	Retinitis Pigmentosa
USB	Universal Serial Bus
VDD	Voltage Drain Drain
VSS	Voltage Source Source



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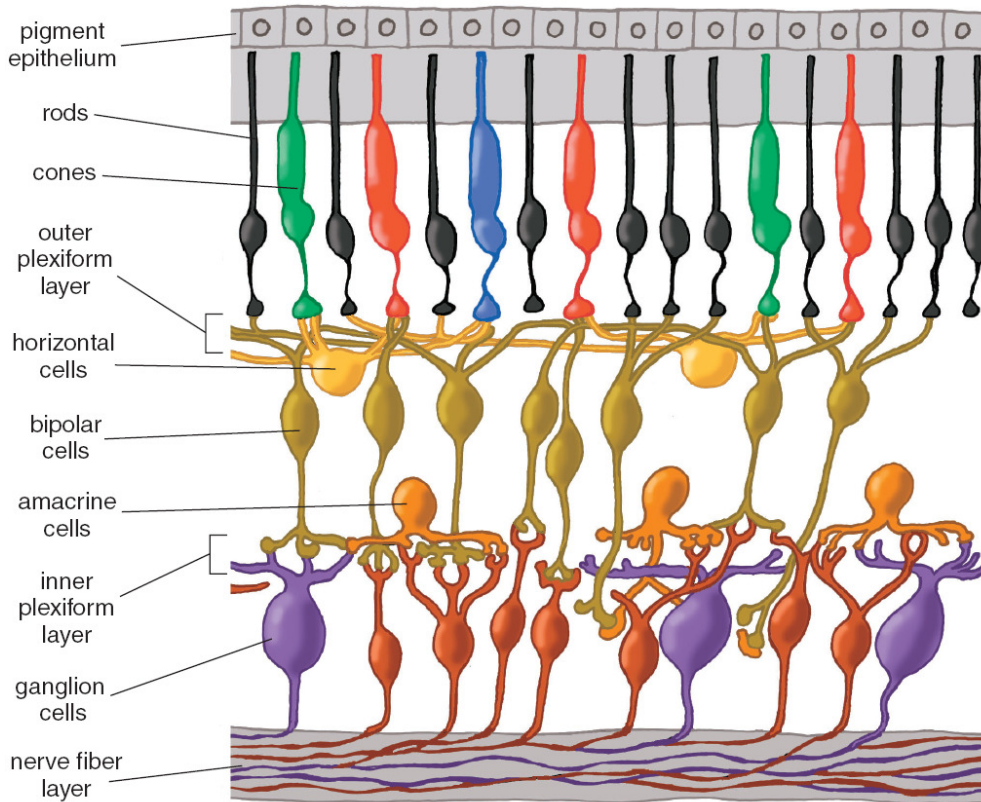
# Chapter 1 Introduction

This chapter gives an overview of retinal prostheses and surveys of previous work on retinal prostheses. Motivation, objectives, and challenges addressed in this thesis follow.

## 1.1 Literature review

Retinitis pigmentosa (RP) and age-related macular degeneration (AMD) are the two most common retinal diseases causing vision loss due to the degeneration of photoreceptors. In the retina, photoreceptors convert photons into a neural signal and other cells in the retina process this signal, and send it to the visual cortex via the optic nerve [1]. Figure 1 shows a piece of the retina in which rods and cones could be the defective photoreceptors in those diseases while other layers such as ganglion cells and bipolar cells are still healthy. Electrically stimulating the surviving parts along the visual path such as the ganglion cells in the retina, or the visual cortex, or the optic nerve has been proved to be able to generate a perception of light [2-22].

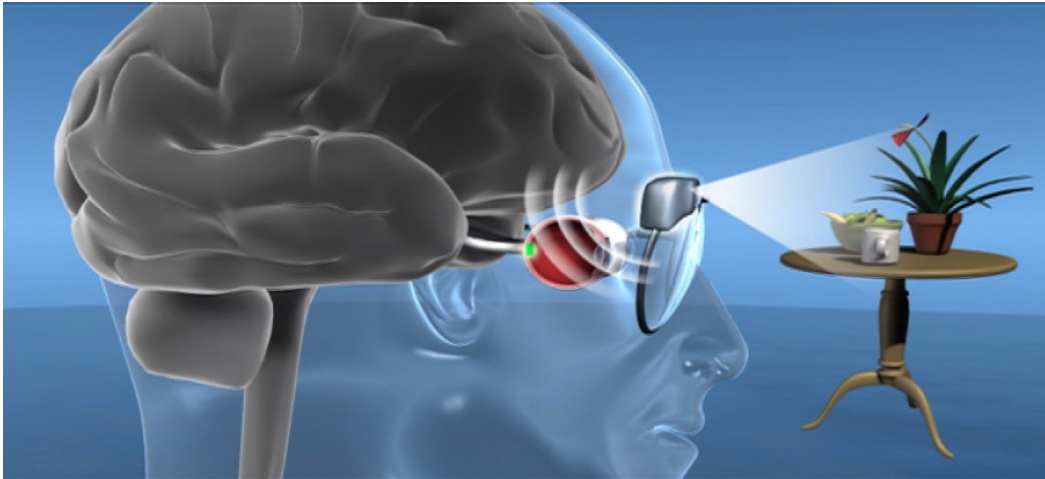
Retinal prostheses including epiretinal implants and subretinal implants have attracted more research including human trials worldwide [2-7, 10, 11, 21], than other visual cortex stimulation [8, 18-20, 22] or optic nerve stimulation [9, 13-17]. This is probably explained by the fact that retinal prostheses have distinct advantages over visual cortex prostheses and optic nerve prostheses in the area of ease of surgical implantation and access to target tissue cells [23].



**Figure 1 Different cell layers in the retina**

Figure 2 shows a concept of a retinal prosthesis system. The retinal prosthesis consists of an external device and an implant device. The external device includes a camera to capture the scene in front of the wearer and a processor to process the image and send it to the implant device wirelessly. The implant device, which is powered wirelessly via an inductive link, receives the image data and converts it into electrical currents to stimulate the retina via an array of electrodes.

In epiretinal prostheses, the electrode-neuron interface is on the epiretinal surface [3, 24-28]. In subretinal prostheses, the electrode-neuron interface is in the subretinal space which is inside the retina [29-31]. Both epiretinal and subretinal approaches have their own advantages and disadvantages. Nevertheless, epiretinal approach is dominant over subretinal approach in aspect of sufficient space to place electronic components, as it has been suggested that a minimum number of 600-1000 electrodes will be needed for the blind to read large-sized text, navigate a room unaided, and recognize faces [32-35]. The remainder of this section surveys the details of some reported epiretinal prostheses, in particular those for which the electronics were well described.



**Figure 2 Conceptual illustration of a retinal prosthesis system**

Human trials with a 16-electrode epiretinal prosthesis show that subjects were able to detect motion and locate objects [4, 6, 10]. However, as details on the electronics behind this device are sketchy, commentary will be brief. Monopolar stimulation was used and simultaneous stimulation was supported. Stimulus pulse width was set at 1 ms. As disc-shaped platinum electrodes were used, the distance between electrodes and target ganglion cells was large, which resulted in a high perception threshold of  $0.35 \text{ mC/cm}^2$ .

The next generation of the above device consisted of 60 electrodes [3, 36]. The system also employed monopolar stimulation with up to 60 simultaneously active electrodes. Stimulus parameters such as current amplitude, pulse widths, and interphase delay were programmable via a wireless link from an external device. The maximum pulse width was 1 ms. The implant chip was fabricated using  $1.2 \mu\text{m}$  CMOS process with an area of  $5.5 \times 5.25 \text{ mm}^2$ . The supply voltages were  $\pm 7 \text{ V}$ . The current drivers could provide full-scaled stimulus currents of 200, 400, or  $600 \mu\text{A}$ , each of which had a resolution of 16 levels.

The latest retinal stimulator of this group consists of 256 electrode drivers [26]. The system also used monopolar stimulation with all 256 electrodes being able to act as active in parallel. Biphasic pulse widths and amplitudes at each electrode were independently controlled. The output current drivers could provide full scaled stimulus currents of 50, 100, 150, 250, 300, 350, 400, and  $500 \mu\text{A}$ , each of which has a resolution of 16 levels. The chip is fabricated in  $0.18 \mu\text{m}$  32V CMOS process with an area of  $5.3 \times$

5.1 mm<sup>2</sup>. The supply voltages are +/-12V and +/-1.8V. No human trials using this stimulator have been reported.

Another research group has performed human trials with their 25-electrode epiretinal prosthesis [5]. One of the most important findings was that the perception threshold varied from 7.8 to 73.2  $\mu\text{C}/\text{cm}^2$ , which is really small compared to the threshold of 0.35  $\text{mC}/\text{cm}^2$  above. This could be explained by the fact that using 3-dimensional electrodes ensured close contact to the ganglion cells, as less charge is wasted along the stimulation path less stimulus current is needed. This low threshold makes it possible to use low voltage for stimulation, which is essential as small-scale CMOS process is proposed to implement the high density epiretinal prosthesis in this research.

A 232-electrode epiretinal prosthesis with maximum 116 simultaneously active electrodes was built but no human trials using this device have been reported yet [28]. The device, which is implemented using 0.35  $\mu\text{m}$  high voltage CMOS process, supports monopolar stimulation. Its electrode driver provides 4 full-scaled stimulus currents with a resolution of 32 levels to represent phosphene brightness and duration. The reason this device has not been tested in human probably lies in the power consumption. With this large number of electrodes and stimulation voltage of up to 25V, the chip can not be supplied with enough power via a wireless link.

A 98-electrode epiretinal prosthesis with a special way of choosing return electrodes was developed [37, 38]. Ninety eight electrodes are arranged in a hexagonal mosaic and divided into 14 groups of 7 electrodes in which each centre electrode acts as the active electrode while the 6 surrounding electrodes act as the return electrodes. This hexagonal mosaic of return electrodes reduces current cross talk between active electrodes in simultaneous stimulation. One limitation of this device is that it supports only 14 simultaneously active electrodes. This epiretinal prosthesis applies bipolar stimulation with stimulation voltage of up to 20V.

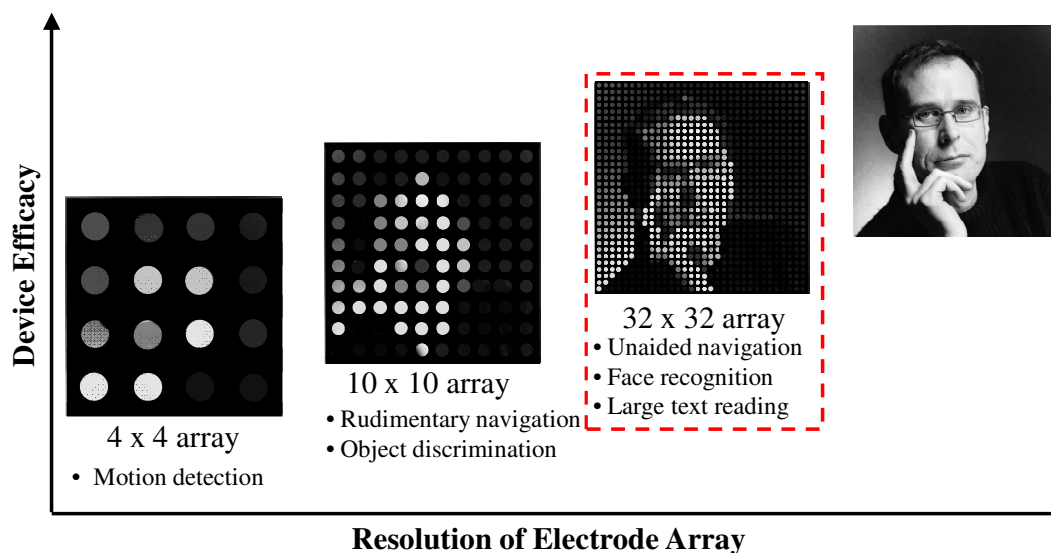
Table 1 summarizes some specifications of the reported prostheses comparing these with the device as planned in the present research.

**Table 1 Comparison of different epi-retinal prostheses with the planned epi-retinal prosthesis**

Number of Electrodes	Stimulation techniques	Stimulus parameters	Maximum current pulse width	Resolution	Stimulation voltage	CMOS process	Chip size	Human trial?	Maximum stimulation current	Charge density threshold	Electrode type
16 electrodes [4]	Monopolar, simultaneous support	N/A	1 ms each	N/A	N/A	N/A	N/A	Yes	~ mA	<0.35 mC/cm <sup>2</sup>	Platinum Disc-shaped
60 electrodes [36]	Monopolar, up to 60 simultaneous	Amplitude, width, interphase delay	1 ms each	16 levels	+/- 7 V	1.2 μm CMOS	5.5 x 5.25 mm <sup>2</sup>	Yes	200, 400, 600 μA	N/A	N/A
256 electrodes [26]	Monopolar, up to 256 simultaneous	Amplitude, width, interphase delay	N/A	16 levels	+/- 12V	0.18 μm HV CMOS	5.3 x 5.1 mm <sup>2</sup>	No	50,100,150, 250,300, 350, 400, 500 μA	N/A	N/A
232 electrodes [28]	Monopolar, up to 116 simultaneous	Amplitude, width, interphase delay	3.2 ms each	32 levels	25 V	0.35 μm HV CMOS	22 mm <sup>2</sup>	No	124, 248, 496, 992 μA	N/A	880 μm <sup>2</sup> platinum
25 electrodes [5]	Monopolar	Amplitude, width, interphase delay, frequency	1526 μs	N/A	10 V	1.2 μm CMOS	8 mm <sup>2</sup>	Yes	100 μA	7.8 – 73.2 μC/cm <sup>2</sup>	3-D
98 electrodes [37]	Bipolar, up to 14 simultaneous	Amplitude, width	1 ms each	32 levels	20 V	0.35 μm HV CMOS	2.8 x 4.6 mm <sup>2</sup>	No	620 μA, 1.24 mA	N/A	N/A
<b>This work – 1024 electrodes</b>	Bipolar or monopolar, up to 1024 simultaneous	Amplitude, stimulation rate, width, interphase delay, frequency	Several ms each	64 levels for amplitude coding, 5 levels for rate coding	3.3V	65 nm CMOS	5 x 5 mm <sup>2</sup>	No	100 μA	N/A	Penetrating boron-doped diamond

## 1.2 Motivations

The fact that human trials have shown that visual perception can be achieved via retinal stimulation makes it promising to conduct more research in retinal prostheses. The state-of-the-art implantable retinal prosthesis does not provide sufficient vision to patients due to its limited number of pixels [3], which leads to a demand for higher resolution retinal prostheses. Figure 3 gives a graphical illustration of device efficacy versus the resolution of electrode array. In this illustration, to achieve some basic forms of vision such as recognizing face, navigating unaided, and reading large text, a 32x32 electrode array is needed.



**Figure 3 Device efficacy vs. resolution of electrode array**

As the number of electrodes increases to 1000, the controlling circuit becomes complicated and needs to be carefully designed so that it can drive the electrode array effectively with as low power consumption as possible. Up to date, the stimulation voltages are usually very high as shown in Table 1. This is probably one of the biggest limitations in realizing high resolution retinal prostheses because with high resolution retinal prostheses, simultaneous stimulation is probably unavoidable. Stimulating multiple electrodes simultaneously at high voltages requires a lot of instantaneous power, which makes it extremely difficult to realize a wireless power harvester in a small chip to provide this amount of power.



In addition to power consumption constraint, the implantable device's size is another constraint when designing high resolution retinal prostheses due to the limited area of the retina and the difficulty in surgery. The chip surface is usually flat while the retina surface is curved, which makes chip area not to be so large to conform to the retina surface. The surgery inserting a chip into the eyeball through the eye wall is a challenging task, which needs the chip to be as small as possible.

Recent work [5, 39] revealed low thresholds of light perception with the use of three-dimensional electrodes ensuring close contact with the ganglion cells, which makes it possible to use lower stimulus voltage than previously for flat electrodes [36, 38]. Therefore, a small-scale CMOS process is ideal for implementing this high acuity retinal stimulator chip to realize high level of circuit integration as well as low power consumption in a compact area.

### **1.3 Research objectives**

The ultimate goal of the electronics team in the Bionic Vision Australia (BVA) bionic eye project is to build a 1024-electrode retinal prosthesis chip using 65 nm CMOS process for low power consumption and high integration. The chip consists of four main parts, which are power recovery circuit, wireless transceiver, diagnostic circuitry, and stimulator. As a part of the project, the research in this thesis aims to build a 1024-electrode stimulator which must be very flexible to be able to realize as many stimulation strategies as possible. However, building the whole 1024-electrode retinal stimulator at the first chip fabrication is not practical. Instead, this research proposes and implements a lot of stimulation flexibility that the ultimate 1024-electrode stimulator could have. To test the feasibility of the 65 nm CMOS process retinal stimulator, new stimulation architectures are developed and a prototype 64-electrode stimulator is implemented using IBM 65 nm CMOS process. This prototype 64-electrode stimulator has all the flexibility the final 1024-electrode stimulator could have. All of the flexibility is verified and performance of every single building block is evaluated. The final objective of this research is to produce a system including the fully functioned prototype 64-electrode stimulator together with supporting hardware and controlling software to be used for preclinical tests to evaluate some stimulation strategies.

## 1.4 Contributions and publications

The research contributes to providing the system design of a highly flexible 1024-electrode retinal stimulator using 65 nm CMOS process. This is the smallest-scale CMOS process ever used for implementing retinal prostheses. The use of this small-scale CMOS process allows high integration, high flexibility, and low power consumption for the targeted high acuity retinal prosthesis.

A lot of stimulation flexibility was proposed and circuits implementing the flexibility have been designed, fabricated, and tested. Measurement results verified correct function and good performance of all the circuits. The stimulation flexibility will help realize many stimulation strategies.

This research resulted in a fully functional prototype 64-electrode stimulator with all the proposed flexibility. Most of the circuits in this prototype stimulator can be reused in the ultimate 1024-electrode stimulator, which reduces significantly future time and effort. This stimulator together with the supporting hardware and controlling software is going to be used in preclinical tests to help verifying many stimulation strategies. This is a very important stage to understand what stimulation strategies are necessary and which are not, before building a complete 1024-electrode stimulator.

The outcomes of this research have been presented in major conferences in the field of biomedical IC design. The work on the prototype 64-electrode stimulator won the 2<sup>nd</sup> place for Best Student Paper Competition at the 33<sup>rd</sup> Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC '11) held in Boston, USA from 30<sup>th</sup> Aug to 3<sup>rd</sup> Sep 2011. The list of publications arising from this research is given below.

### **Journals:**

1. Ng D., Bai S., Yang J., **Tran N.**, Skafidas E., "Wireless Technologies for closed loop retinal prosthesis," *Journal of Neural Engineering*. Vol. 6, No. 6, pp. 1-10, Oct. 2009.
2. J. Yang, **N. Tran**, S. Bai, D.C. Ng, M. Halpern, E. Skafidas, "A Super Low Power CMOS Receiver for High Resolution Epi-retinal Prosthesis", *Journal of Energy and*

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*Power Engineering*, David Publishing Company, USA, Vol. 4, No.8, Serial No.33, pp. 32-39, Aug. 2010.

### **Conferences:**

1. **Nhan Tran**, Stan E. Skafidas, Jiawei Yang, Shun Bai, Meng Fu, David Ng, Mark Halpern, Iven Mareels, "A fully flexible stimulator using 65 nm CMOS process for 1024-electrode epi-retinal prosthesis," *the 33rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2011)*, Boston, USA, pp. 6729-6732, Sep. 2011, won the 2<sup>nd</sup> place for Best Student Paper Competition.
2. **Tran, N.**; Yang, J.; Bai, S.; Skafidas, E.; Mareels, I.; Ng, D.; Halpern, M., "A Flexible Electrode Driver using 65 nm CMOS Process for 1024-electrode Epi-retinal Prosthesis", *the International Workshop on Design, Analysis and Tools for Integrated Circuits and Systems, in the 5<sup>th</sup> International Conference on Future Information Technology (DATICS-FUTURETECH 2010)*, Busan, Korea, pp. 1-5, 20-24 May 2010.
3. **Nhan Tran**, Jiawei Yang, Shun Bai, David Ng, Mark Halpern, David B. Grayden, Stan E. Skafidas, Iven Mareels, "A fully flexible stimulator using 65 nm CMOS process for 1024-electrode epi-retinal prosthesis," *the 31st Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2009)*, Minneapolis, USA, pp. 1643-1646, Sep. 2009.
4. **Nhan Tran**, Jiawei Yang, David Ng, Mark Halpern, Stan E. Skafidas, Iven Mareels, "An alternately pull-push electrode driver using small-scale CMOS process for high resolution epi-retinal prosthesis," *Medical Bionics 2008*, Lorne, VIC, Australia, pp. 51, 17 Nov. 2008.
5. J. Yang, **N. Tran**, S. Bai, M. Fu, E. Skafidas, I. Mareels, M. Halpern, D. Ng, "A Subthreshold Down Converter Optimized for Super-Low-Power Applications in Mics Band", *IEEE Biomedical Circuits and Systems Conference 2011 (IEEE BioCAS 2011)*, San Diego, California, USA, pp. 189-192, 10-12 Nov. 2011.
6. J. Yang, **N. Tran**, S. Bai, M. Fu, E. Skafidas, I. Mareels, M. Halpern, "A Ultra Low Power, Wide Input Range MICS Band Channel Selection Filter on 65 nm CMOS",

- IEEE Biomedical Circuits and Systems Conference 2010 (IEEE BioCAS 2010), Paphos, Cyprus, pp. 218-221, 3-5 Nov. 2010.
7. J. Yang, M. Fu, E. Skafidas, **N. Tran**, S. Bai, I. Mareels, D.C. Ng, M. Halpern, "A Super Low Power MICS Band Receiver Front-end Down Converter on 65 nm CMOS", *the 3rd International Conference on BioMedical Engineering and Informatics* (IEEE BMEI 2010), Yantai, China, Vol. 4, pp. 1412-1415, 16-18 Oct. 2010.
  8. Yang, Jiawei; **Tran, Nhan**; Bai, Shun; Ng, David C.; Halpern, Mark; Skafidas, Efstratios; Mareels, Iven; "A super low power MICS band receiver in 65 nm CMOS for high resolution epi-retinal prosthesis", *the 8<sup>th</sup> IEEE International Conference on ASIC* (ASICON 2009), pp. 435 – 438, 20-23 Oct. 2009.
  9. Jiawei Yang, **Nhan Tran**, David Ng, Mark Halpern, Stan E. Skafidas, Iven Mareels, "A super-low-power and high data rate CMOS wireless transceiver for high resolution epi-retinal prosthesis using 65nm technology," *Medical Bionics 2008*, Lorne, VIC, Australia, pp. 51, 17 Nov. 2008.
  10. S. Bai, D. Ng, J. Yang, **N. Tran**, M. Halpern, I. Mareels and E. Skafidas, "Wireless Power Supply Module for High Resolution Epi-retinal Prosthesis using 65nm CMOS Process", *2009 International Symposium on Bioelectronics and Bioinformatics* (ISBB 2009), Melbourne, Australia, pp. 1-4, 9-11 Dec., 2009.
  11. M. Fu, J. Yang, **N. Tran**, S. Bai, D. C. Ng, M. Halpern, E. Skafidas, I. Mareels, "A GFSK Demodulator for Ultra-Low Power MICS Band Receiver", *the 5<sup>th</sup> International Conference on Broadband and Biomedical Communications* (IB2Com 2010), Malaga, Spain, pp.1-4, 15-17 Dec. 2010.
  12. David C. Ng, Shun Bai, Clive Boyd, **Nhan Tran**, Jiawei Yang, Mark Halpern, Efstratios Skafidas, " High Efficiency Double-paired Inductive Coils for Wireless Powering of a Retinal Prosthesis," *the 7<sup>th</sup> IASTED International Conference on Biomedical Engineering (BioMED 2010)*, Innsbruck, Austria, pp. 106-110, 17-19 Feb. 2010.

13. Ng, D. C., Bai, S., Yang, J., **Tran, N.**, Skafidas, E., "Closed-loop Inductive Link for Wireless Powering of a Retinal Prosthesis," *Progress in Electromagnetics Research Symposium* (PERS 2009), Moscow 18-21 Aug. 2009.

## 1.5 Thesis organization

This thesis contains seven chapters including this introduction. The remainder of this thesis is organized as follows.

Chapter 2 presents the flexibility that the stimulator provides. It begins with an introduction on electrical stimulation, and then discusses two methods used to represent phosphene brightness. A novel electrode driver topology comes next. It is followed by the flexibility the stimulator provides.

Chapter 3 discusses system design considerations and describes the design of the global controlling circuits. The stimulator's system architecture is introduced. A distributed design approach is employed. Some circuits providing global parameters such as the bias current and system timing information are described in detail.

Chapter 4 focuses on the design of the new electrode driver which is the key component determining the flexibility of the whole stimulator. In this stimulator, each electrode is controlled by its own independent driver. This ensures fully free control of each electrode, independent from any other.

Chapter 5 presents the design of the prototype 64-electrode stimulator. Details on the baseband controller including bit synchronizer, frame synchronizer, CRC checker, and data type decoder are described. Measurement results verifying the functionality follow. Global configuration data are also described in detail.

Chapter 6 presents the measurement results of the prototype stimulator. It starts with an overview of the measurement setup and then shows the performance of an individual electrode driver. The verification of the proposed flexibility of the stimulator is explained.

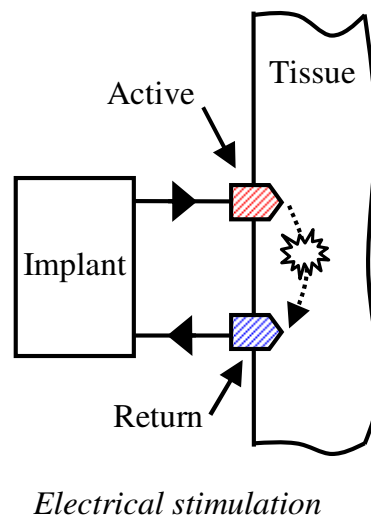
Chapter 7 concludes the work and identifies some future work to implement the fully integrated 1024-electrode retinal stimulator.

## Chapter 2 Stimulation Flexibility

Stimulation strategies for retinal prostheses are still under research [40-46]. Therefore, the stimulator must be flexible enough to be able to implement different stimulation strategies. This chapter presents all the flexibility the ultimate high acuity stimulator is designed for.

### 2.1 Functional electrical stimulation

Functional electrical stimulation is to inject a certain amount of charge into the targeted tissue cells within certain time duration via electrodes to mimic the functions of the stimulated tissue cells. Figure 4 illustrates an example of electrical stimulation, in which one electrode acts as an active electrode, the other acts as a return electrode. When the two electrodes are far away from each other, the stimulation configuration is called monopolar. When the two electrodes are close to each other, the stimulation configuration is referred to as bipolar [47]. The charge amount is a very important factor when performing electrical stimulation because it determines the depolarization of the stimulated cells. In addition, with the same amount of charge, different ways of injecting may result in different stimulation effects. Therefore, the stimulator in this work is designed so that it is able to control the charge injection as much as possible.

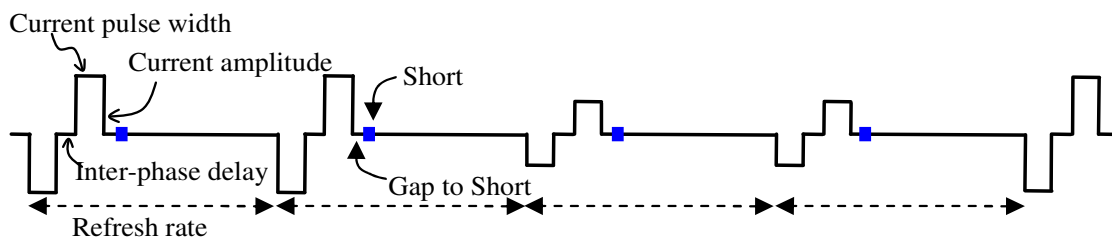


**Figure 4 Electrical stimulation**

## 2.2 Two approaches representing phosphene brightness

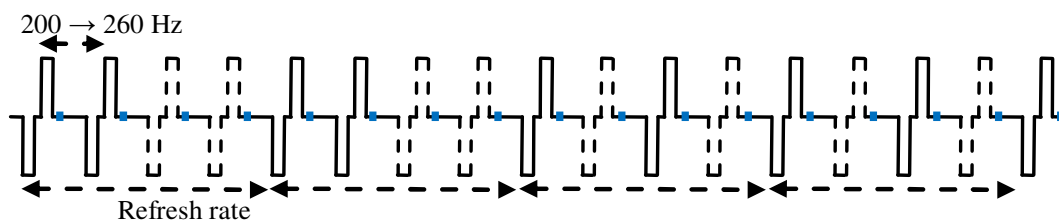
A biphasic current pulse has been widely used as a means of stimulating retina tissues whilst ensuring charge balance at the electrodes [5, 36, 38, 48]. The aim of the retinal stimulator in this work is to translate a grey-scaled image to stimulation currents. A grey-scaled image is made of different brightness levels. Brightness may be represented by stimulus current amplitude [49] or possibly by rate of stimulation [50]. The stimulator described in this thesis can support both of these two stimulation approaches. Figure 5 shows the waveform for the stimulus current amplitude approach. In this approach, the stimulus current amplitude is varied to represent the brightness, while other parameters such as current pulse widths, interphase delay and stimulation rate (refresh rate) are fixed. To achieve flicker-free vision, the refresh rate is chosen to be 60 Hz [49]. In the figure, there is an electrode shorting time after each stimulus pulse. This is to short all electrodes to chip ground to discharge any residual charge on any electrode, which may cause electrode corrosion if allowed to accumulate over time.





**Figure 5 Stimulus current amplitude representing phosphene brightness**

Meanwhile, in the stimulation rate approach shown in Figure 6, all parameters of the stimulus current are fixed but for a high stimulation rate (200-260 Hz), and the brightness is determined by the number of stimulus pulses and the locations of them in one stimulation refresh period. In the figure, in the first two refresh periods the stimulation is done by two consecutive pulses at the beginning of each period, while in the last two refresh periods, two pulses are also used for stimulation but they are separated by an empty pulse. The designed stimulator provides this stimulation ability with the hope that it may lead to different stimulation effects.



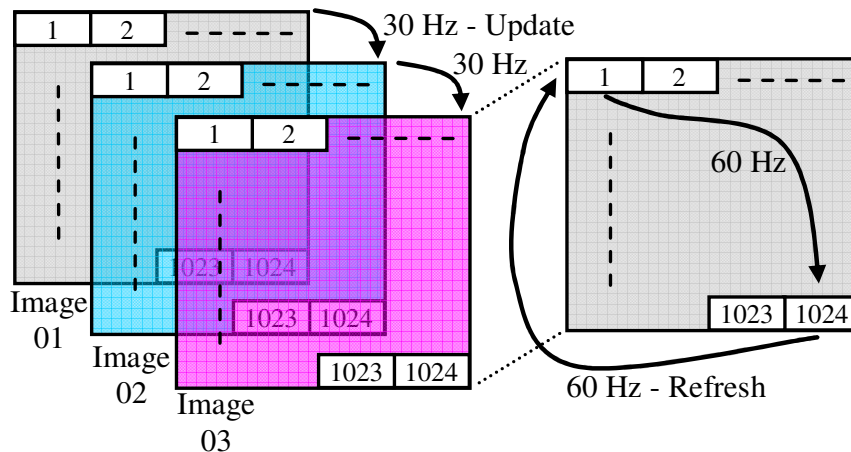
**Figure 6 Rate of stimulation representing phosphene brightness**

In short, the designed stimulator supports two stimulation approaches to represent brightness: current amplitude and stimulation rate. The main purpose of this stimulation ability is to implement different stimulation strategies in terms of charge injection.

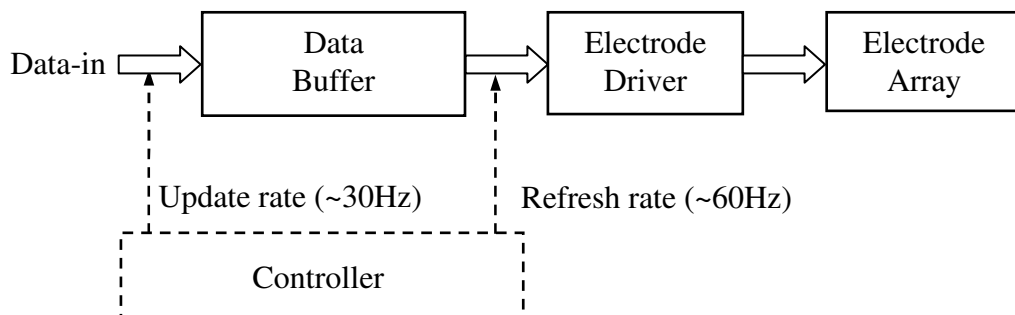
### 2.3 Separation of data update rate and stimulation refresh rate

Figure 7 shows an illustration of updating consecutive image frames and refreshing one image frame. The update rate of video images is about 30 frames per second to provide continuous motion. Meanwhile, to achieve flicker-free vision, the refresh rate

needs to be around 60 Hz as mentioned in the previous section. Therefore, it is not necessary to transmit data according to the image refresh rate as in [10]. Instead, the image data is transmitted based on the update rate, and valid data is stored in a data buffer before being refreshed. Every image frame stored in the buffer is refreshed twice (at 60 Hz) before replaced by new frame (at 30 Hz) as illustrated in Figure 8. The separation of image update and refresh rate with the help of the data buffer reduces the required data bandwidth by a half, which is very useful when the data transmission of the targeted retinal prosthesis chip uses the MICS frequency band (402 MHz to 405 MHz) where channel bandwidth is limited to 300 kHz [51, 52]. For example, with an image consisting of 1024 pixels each of which has 6 bits, when updated at 60 Hz, the required data rate is  $1024 \times 6 \times 60 \approx 360$  kHz. But when updated at 30 Hz, the required data rate is reduced by a half to approximately 180 kHz, which fits perfectly well within the bandwidth of the MICS band.



**Figure 7 Image update and refresh**

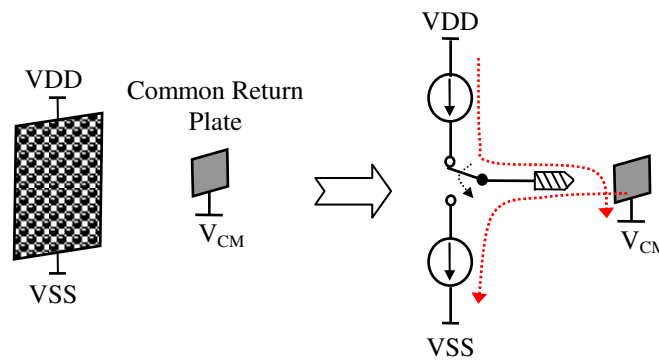


**Figure 8 Illustration of update and refresh separation**

## 2.4 Novel electrode driver topology

Choosing electrode driver configuration is a very important step in the whole design process since it will determine what supply voltages are to be used, which is very important as developing negative supply voltage is a challenge for standard CMOS design. The following sections analyze all the reported stimulation configurations.

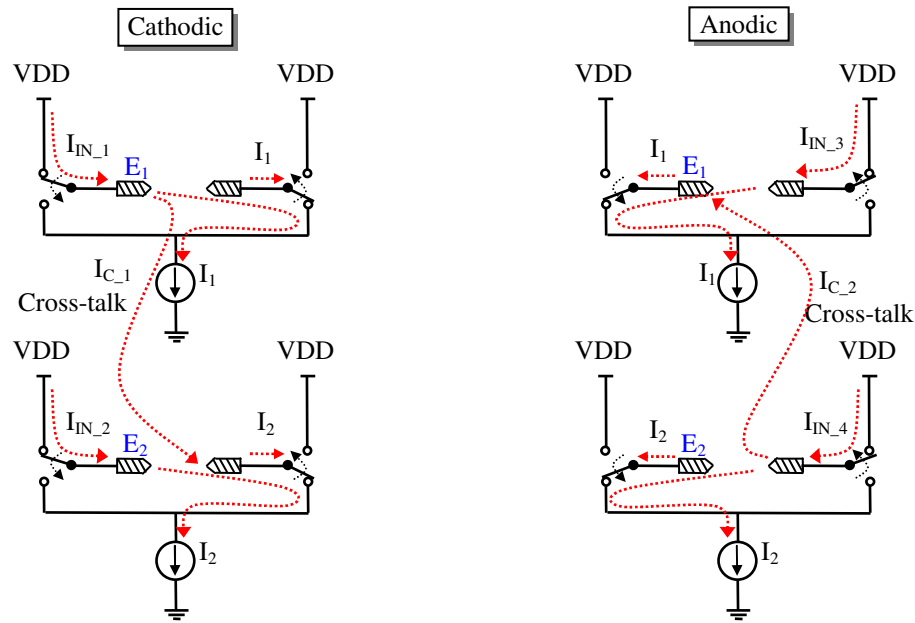
The first configuration is monopolar where one remote common electrode acts as return electrode. This configuration was used in [26, 28, 36, 53, 54]. In this configuration, one big plate plays the role of return electrode. This plate is far away from the stimulation electrode array as shown in Figure 9. In the figure, VDD is the highest voltage and VSS is the lowest voltage while  $V_{CM}$  is at the middle of them.



**Figure 9 Common return electrode configuration**

This structure is the best in terms of achieving charge balance at any single electrode as the current flowing in and out of that electrode is totally controlled by the current source and sink as long as these two currents are equal. However, this structure has two drawbacks. Firstly, the maximum voltage across stimulation electrodes is  $(VDD - V_{CM})$  or  $(V_{CM} - VSS)$ , which is just half of the maximum usable voltage  $(VDD - VSS)$ . This reduces stimulation capability when  $(VDD - VSS)$  is not high enough. Especially, with small scale CMOS process for high integration, this voltage is small, which can make the stimulating current smaller than expected. Secondly, the common return plate is potentially difficult from a surgery point of view.

The second configuration is bipolar where electrodes are stimulated in pairs with only one current sink for a pair [24]. This configuration uses one current sink for both phases of stimulus pulse as shown in Figure 10.



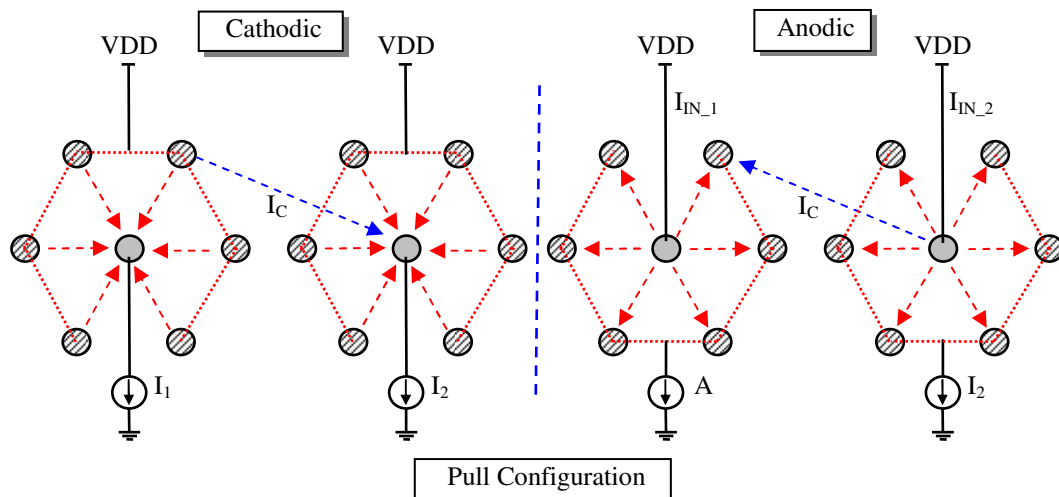
**Figure 10 Paired couple stimulation with only one current sink**

This configuration can utilize the maximum voltage in the circuit for stimulation but the charge balance becomes a critical issue since the current flowing into an electrode is highly unequal to the current flowing out of it due to cross-talk with other electrodes when stimulated simultaneously as illustrated in the figure. For example, in the cathodic phase, the current  $I_{IN_1}$  flowing into electrode  $E_1$  may include the controllable current  $I_1$  and the unpredictable crosstalk current  $I_{C_1}$ , while in the anodic phase, the current flowing out of it is just the controllable current  $I_1$ , which means that charge balance at electrode  $E_1$  will not be achieved.

The third configuration is also bipolar but with multiple return electrodes arranged in hexagonal mosaic instead of one [37, 38]. Three different ways of sending stimulus currents were investigated as follows:

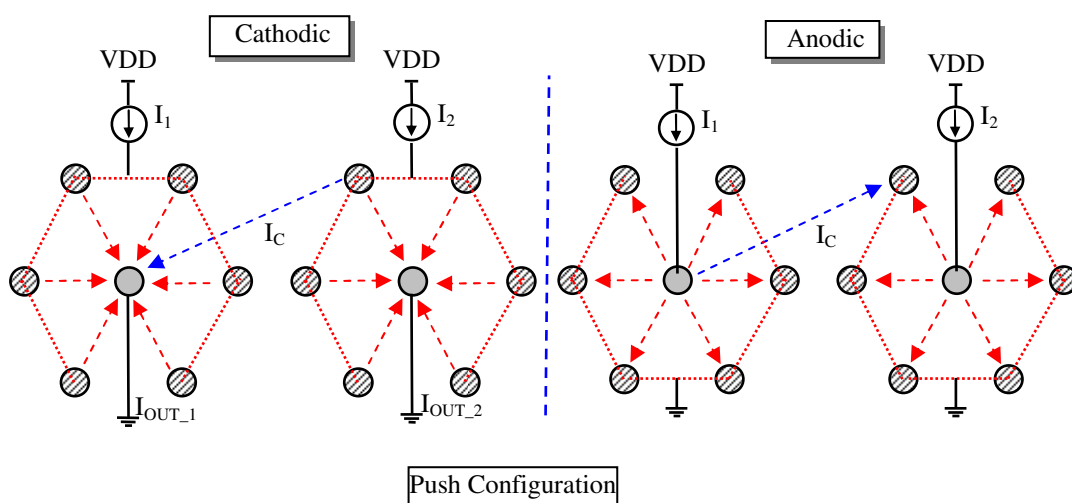
**Pull configuration:** The cathodic phase of stimulus current is pulled out from the active electrode by a current sink while the anodic phase is injected into this electrode directly from VDD with the same current sink pulling out current from returning

electrodes. Therefore, the anodic phase of the current is uncontrollable due to the possible occurrence of current crosstalk during simultaneous stimulation as shown in Figure 11.



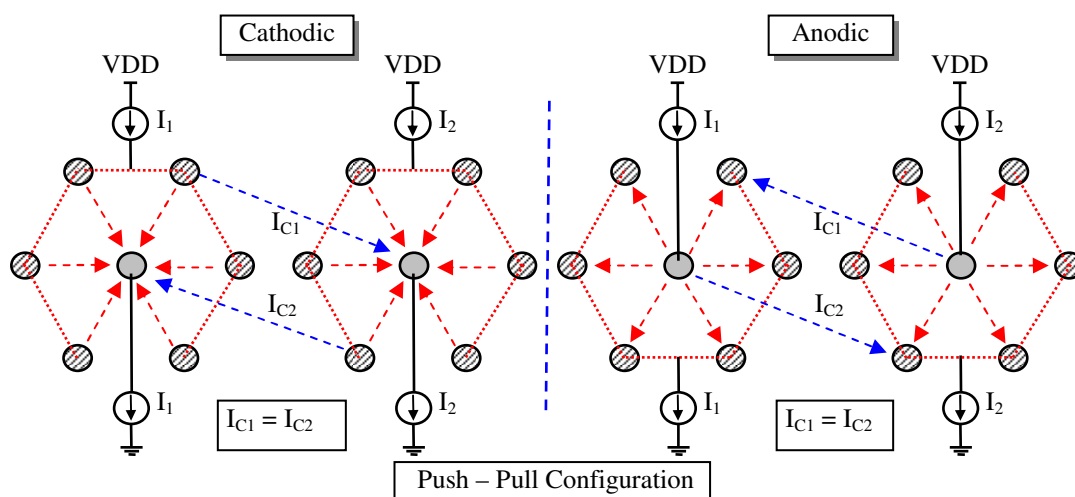
**Figure 11 Hexagonal mosaic – pull configuration**

**Push configuration:** The cathodic phase of stimulus current is pulled out from the active electrode with a current source pushing current into returning electrodes while the anodic phase current is pushed into this electrode by the same current source. Therefore, the cathodic phase of the current is also uncontrollable due to the cross-talk current during simultaneous stimulation as shown in Figure 12.



**Figure 12 Hexagonal mosaic – push configuration**

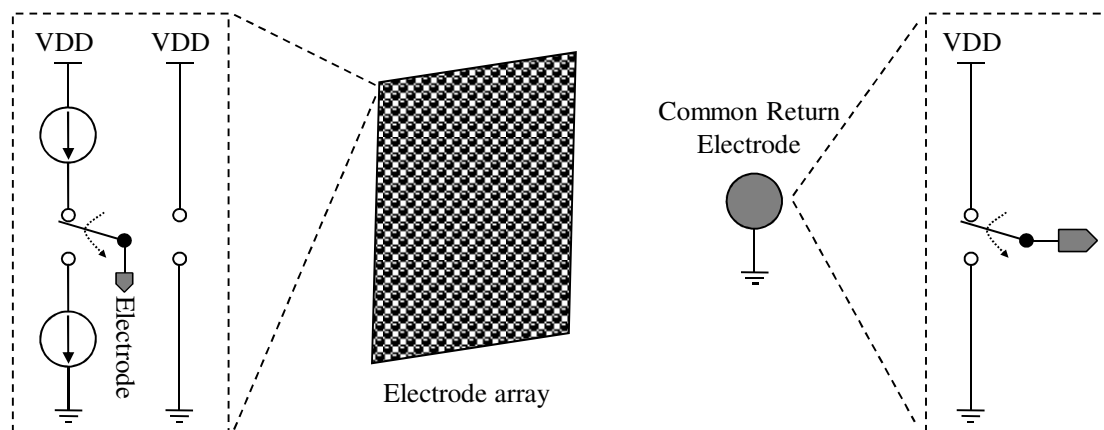
**Push-pull configuration:** This configuration can achieve the best concentration of stimulating current and the best charge balance at the stimulating electrode. However, charge balance at each return electrode is not guaranteed. As shown in Figure 13, crosstalk probably happens between electrode groups, but thanks to the current sink and the current source, total crosstalk from one group to another might cancel each other. But what happens if crosstalk just happens from one direction? Assuming that during the cathodic phase, crosstalk current  $I_{C2}$  does not exist while crosstalk current  $I_{C1}$  tends to flow a lot, then the active electrode in the left group might not collect enough current as most of the current flows to the right group. Another limitation of this configuration is that there are one current source and one current sink operating at the same time when stimulating, this results in a smaller available stimulating voltage across electrodes compared to single pull or push configuration. This becomes critical when small-scale CMOS is used to implement the electrode drivers.



**Figure 13 Hexagonal mosaic – Push-pull configuration**

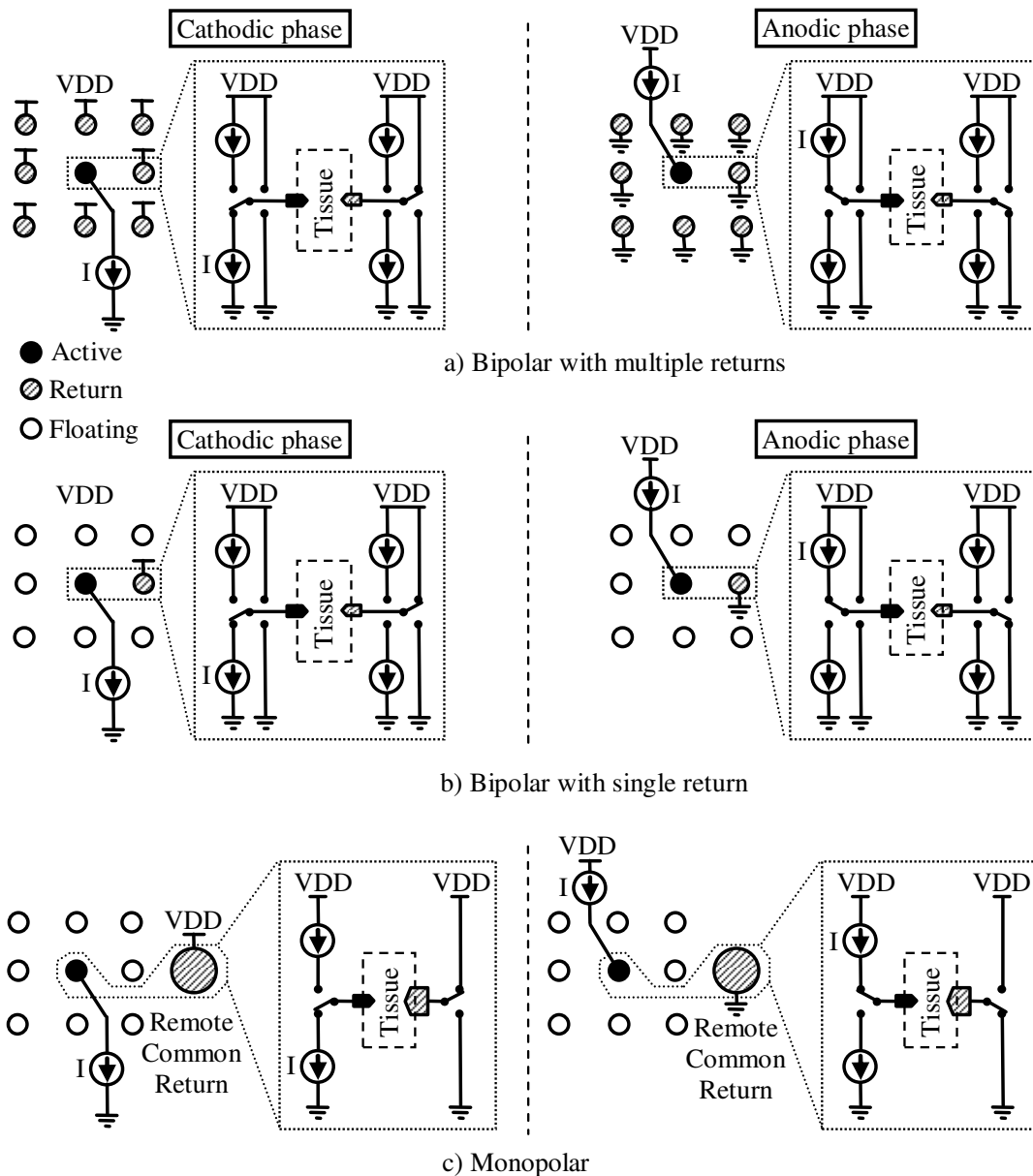
From the analysis of different stimulation configurations above, a charge-balanced, low headroom voltage, and localized stimulation configuration is necessary for the proposed high density epiretinal stimulator. Figure 14 shows such a stimulation configuration, in which each electrode in the array is driven by one driver, which can connect the electrode to either a current sink or a current source or VDD or GND. As each electrode has its own driver, any electrode can be stimulated at any time, independently of any other. This feature makes this configuration different from the one

in [55] where a demultiplexer follows an electrode driver to drive multiple electrodes, which not only reduces stimulation flexibility but also consumes more headroom voltage. In the figure, for the common return electrode, the driver consists of two switches which connect the common return electrode to either VDD or GND. The common return electrode can be placed at the back of the eye ball or can be just a large pad on the chip which is exposed to the vitreous humor.



**Figure 14 Proposed electrode driver topology**

A stimulation operation takes place as follows: an active electrode is first connected to a current sink, and then a current source to generate biphasic stimulus current (with cathodic phase leading), while the return electrode is connected to VDD, and then GND, respectively. This alternately push-pull manner makes the stimulus current at the active electrode controllable and also consumes less headroom voltage as only one current sink or source is used at a time. In addition, the ability to switch return electrodes between VDD and GND makes it possible to utilize all of the maximum available voltage in the device for stimulation ( $VDD - GND$ ), and the use of only single rail supply is preferable in CMOS circuit design.



**Figure 15 Charge-balanced guaranteeing, low headroom voltage, and localized stimulation configurations**

The proposed electrode driver topology allows any electrode in the array to act as either active or return, which results in the ability of implementing three different stimulation configurations. The first configuration is bipolar with multiple returns as shown in Figure 15a, in which all inactive electrodes surrounding an active electrode act as return electrodes, which makes stimulus current localized closely to the active electrode. The second configuration is also bipolar but with only one single return as shown in Figure 15b where return electrode is a single electrode close to active

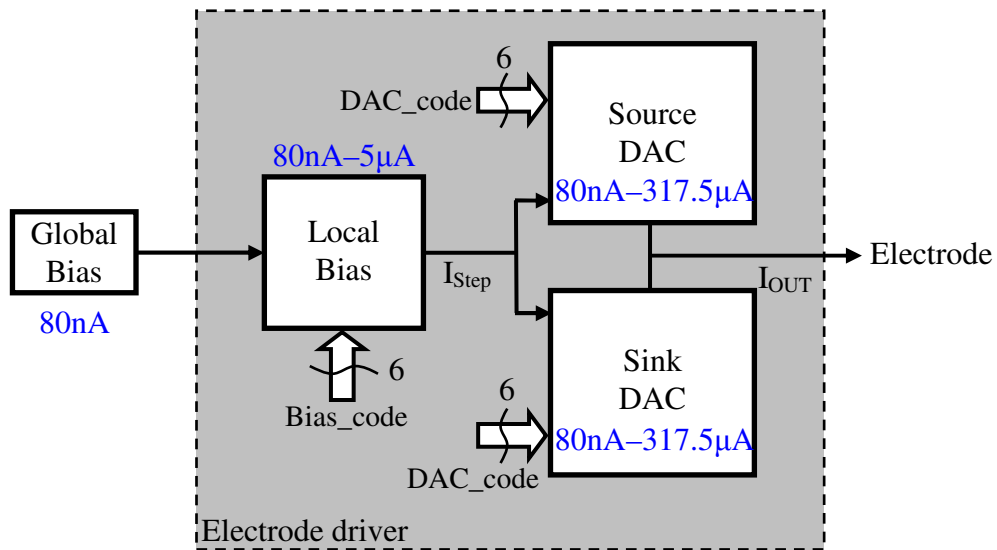


electrode. The last configuration is monopolar as shown in Figure 15c where all electrodes in the array act as active only, and the remote electrode acts as return.

In brief, the proposed electrode driver topology results in lots of flexibility. Each electrode in the array is controlled by its own driver, which makes both the controlling and the selecting of any electrode independent from all other electrodes. The alternately push-pull manner with only one current sink or source working at a time helps reduce headroom voltage by a half, which is very meaningful when considering the pretty low supply voltage of the small-scale CMOS process. The novel electrode driver topology supports three different stimulation configurations which are bipolar with multiple returns, bipolar with single return, and monopolar.

## **2.5 Wide-range current amplitude**

Electrode-tissue impedance varies depending on electrode's position in the eye, electrode's material and size [6, 56]. With a fixed stimulation voltage, the maximum current which can be delivered to tissue is dependent on the electrode-tissue impedance, which also varies over time [4] and can probably range from tens of  $k\Omega$  to hundreds of  $k\Omega$ . Therefore, to deal with the wide range of impedance, the current source must be able to provide wide range current amplitude in order to provide appropriate current values. Figure 16 shows a new current bias topology which can provide stimulus current from 80 nA to 317.52  $\mu\text{A}$ .



**Figure 16 Stimulus current's bias topology**

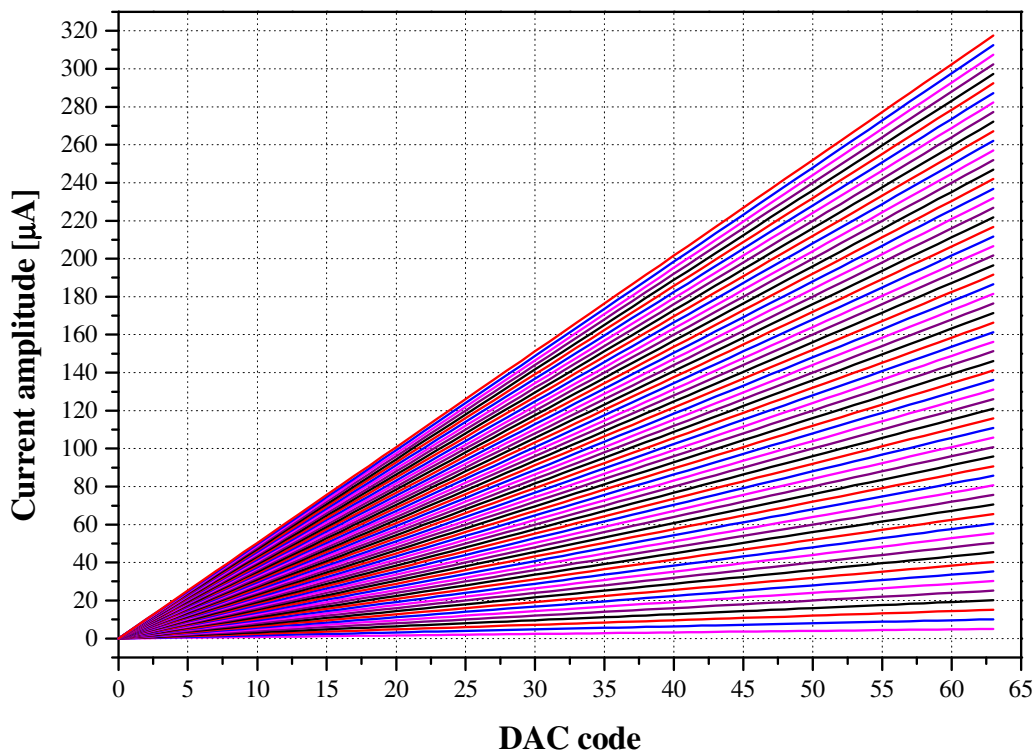
In this topology, a global bias generator delivers 80 nA of bias current which is used as a reference current for every electrode driver. At each electrode driver, there is a local bias generator which is a 6-bit Digital to Analog Converter (DAC). This DAC generates 63 different step currents ( $I_{Step}$ ) starting from the global bias of 80 nA to maximum 5.04  $\mu$ A. Each step current is then used as a reference current for output current source and sink DAC's, which also use 6 bits to multiply up each step current to 63 different levels. Equation (1) gives the calculation of output current.

$$I_{OUT} = DAC\_code \times I_{Step} = 80 \times Bias\_code \times DAC\_code \quad [nA] \quad (1)$$

Table 2 lists all the current values corresponding to 63 different step currents. Figure 17 illustrates the current amplitude as a function of the digital input of the current source/sink DAC for different step currents.

**Table 2 Current amplitude at different step currents**

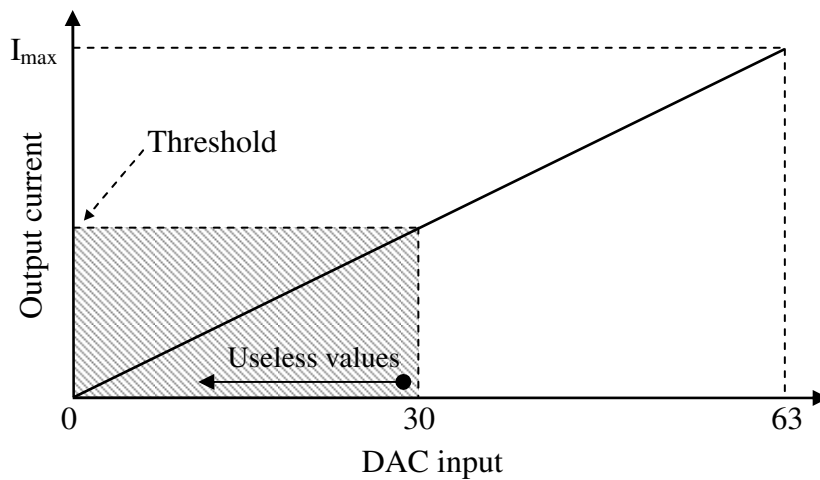
Step\DAC_code	1	2	3	...	61	62	63
80 nA	80 nA	160nA	240 nA	...	4.88 $\mu$ A	4.96 $\mu$ A	5.04 $\mu$ A
160 nA	160 nA	320 nA	480 nA	...	9.76 $\mu$ A	9.92 $\mu$ A	10.08 $\mu$ A
240 nA	240 nA	480 nA	720 nA	...	14.64 $\mu$ A	14.88 $\mu$ A	15.12 $\mu$ A
...							
4.88 $\mu$ A	4.88 $\mu$ A	9.76 $\mu$ A	14.64 $\mu$ A	...	297.68 $\mu$ A	302.56 $\mu$ A	307.44 $\mu$ A
4.96 $\mu$ A	4.96 $\mu$ A	9.92 $\mu$ A	14.88 $\mu$ A	...	302.56 $\mu$ A	307.52 $\mu$ A	312.48 $\mu$ A
5.04 $\mu$ A	5.04 $\mu$ A	10.08 $\mu$ A	15.12 $\mu$ A	...	307.44 $\mu$ A	312.48 $\mu$ A	317.52 $\mu$ A

**Figure 17 Current source output vs. DAC input code at different step currents**

## 2.6 Fully utilizing the number of current levels

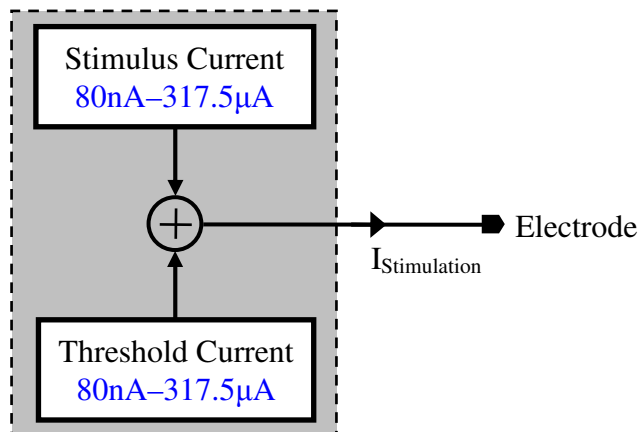
Different patients and different regions in the retina have different depolarization threshold from which phosphene starts to be perceived [4]. Therefore, each electrode driver should have the ability to provide its own threshold current to cope with these

variations. In addition, for a certain number of output current levels, the threshold lies within the current range. Only currents higher than the threshold are effective, the ones below the threshold are useless. Figure 18 shows an illustration of this circumstance, in which the output current source has 63 different levels, the depolarization threshold is at the current value where the DAC input value is 30. It can easily be seen that for the DAC input values of less than 30, the output currents are below the threshold, hence useless. This is the case for all of the reported retinal stimulator [4, 5, 26, 28, 36, 37].

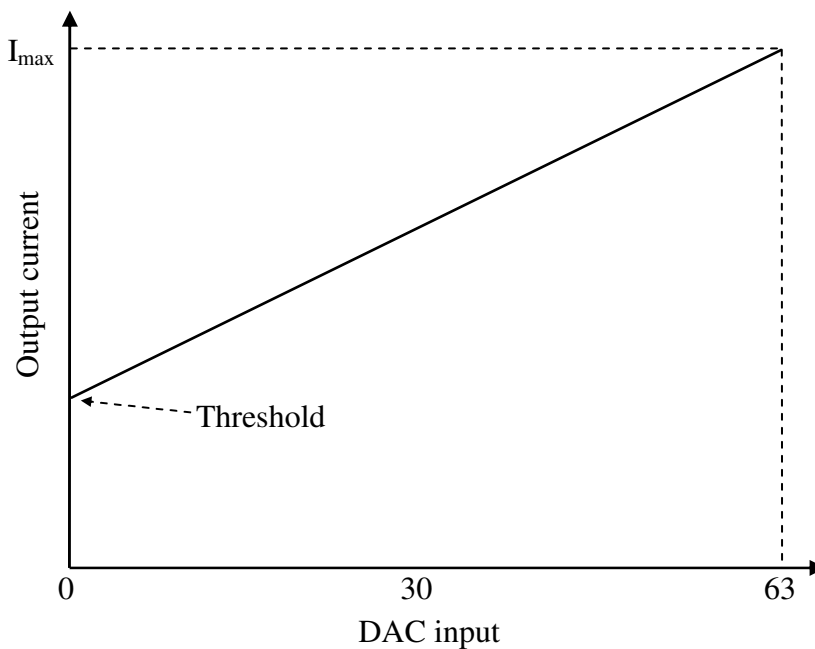


**Figure 18 Illustration of the effect of depolarization threshold to the effectiveness of the output current source**

Therefore, in order to utilize all of the output current levels, a new output current scheme was proposed. In this scheme shown in Figure 19, the output current is sum of stimulus current and threshold current. With this combination, each output current used for stimulation consists of a fixed threshold added with one of 63 values of the stimulus current as shown in Figure 20. By doing this way, all 63 different levels above the threshold can be used to represent brightness, hence no level is useless. The threshold current generator is a replica of the stimulus current generator shown in Figure 16, hence it also has a very wide range of values starting from 80 nA to 317.52  $\mu$ A. As a result, the total stimulation current varies in a double-sized range from 80 nA to 635.04  $\mu$ A.



**Figure 19** Threshold and stimulus current combination

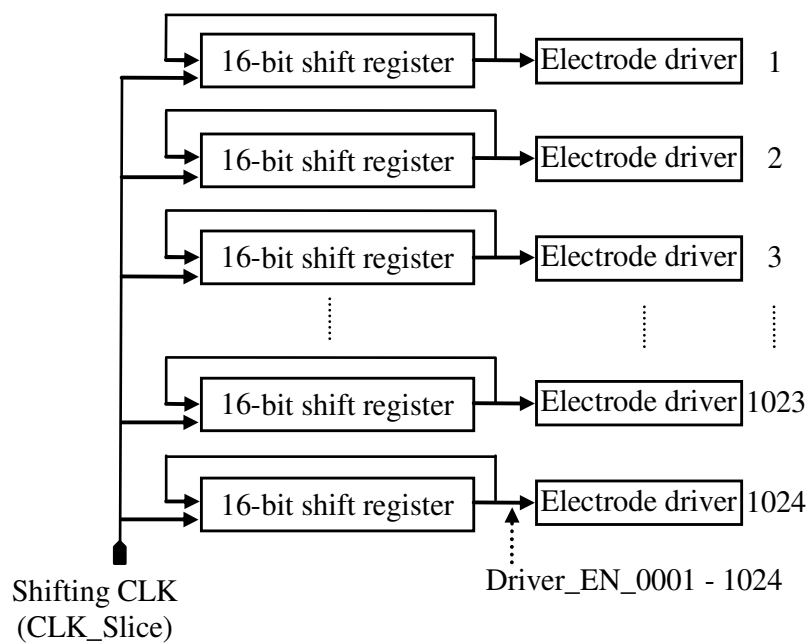


**Figure 20** Output current vs. DAC input with the addition of threshold current

In short, the combination of stimulus current and threshold current not only helps utilizing all the available current levels but also enhances the range of the stimulation current amplitude.

## 2.7 Fully flexible electrode selection

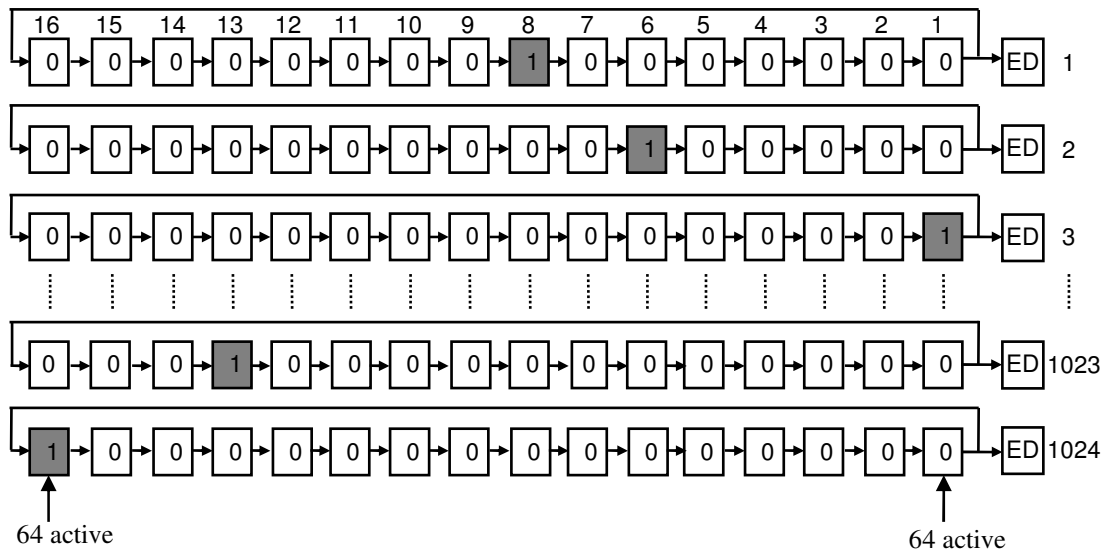
The number of simultaneously active electrodes is determined by the total number of electrodes in the stimulator, the total stimulus pulse duration, and the refresh rate. Indeed, to stimulate  $N_E$  electrodes with a  $T_P$ -ms stimulus pulse for each electrode, a refresh rate of  $f_S$  Hz (refreshing interval –  $T_S = 1/f_S$  ms) needs to be divided into  $N_{TS} = T_S / T_P$  time slices, in each of which  $N_E / N_{TS}$  electrodes are stimulated simultaneously so that after  $N_{TS}$  time slices, all  $N_E$  electrodes in the array are stimulated. For example, to stimulate 1024 electrodes at a refresh rate of 60 Hz (16.67 ms) with a total stimulus pulse duration of 1 ms ( $16.67\text{ms}/1\text{ms} = 16$  time slices),  $1024/16 = 64$  electrodes must be simultaneously activated.



**Figure 21** Array of sequencers

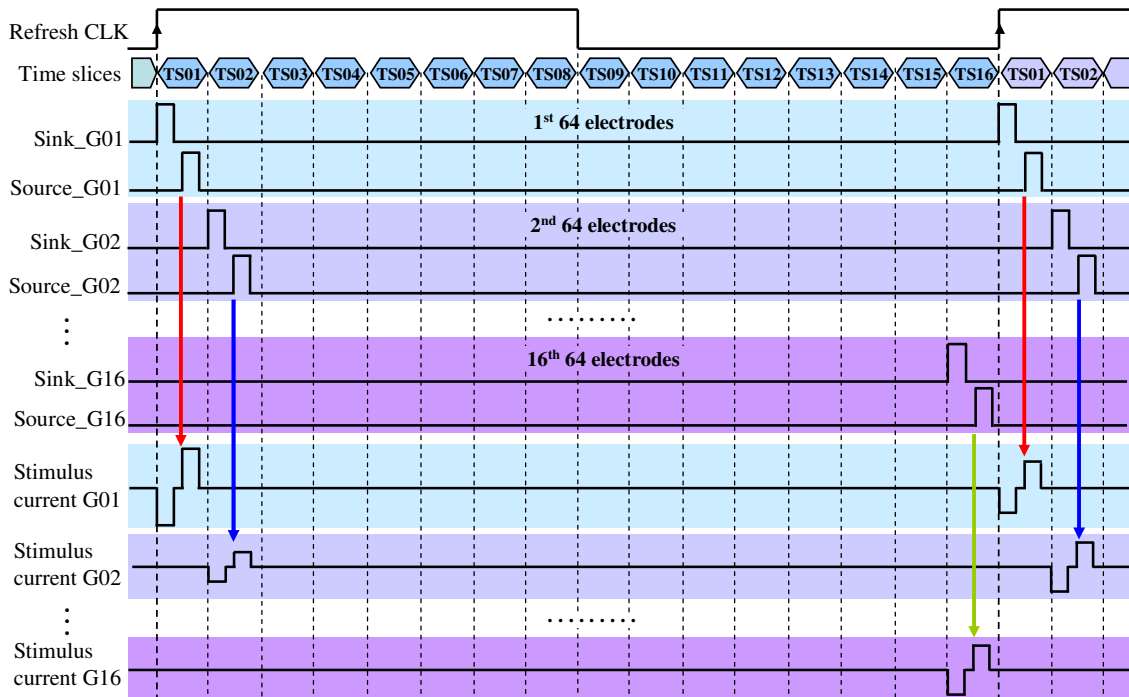
It is necessary that the selection of those 64 electrodes must be as flexible as possible to investigate all possible electrode patterns. An array of sequencers including 1024 16-bit shift registers as shown in Figure 21 can select any number of electrode drivers at any time slice. Each electrode driver is driven by one sequencer. When a binary bit of 1 is present at output of a sequencer, the corresponding electrode driver is selected. Once data representing sequence of stimulation has been written, the 16-bit shift registers keep circulating to periodically select the electrode drivers. Therefore, any electrode can

be selected at any time slice as long as at that time slice, 1 is present at its sequencer output. Figure 22 shows an illustration of the sequencer operation where 64 electrodes are selected at one time slice. In this figure, at time slice 1, electrode driver 3 and 63 others are selected, while at time slice 8, electrode 1 and 63 others are chosen, and so on. Eventually, after 16 time slices all 1024 electrodes are stimulated, and this process repeats during the stimulation stage of the stimulator's operation.



**Figure 22 Stimulation with 64 active electrodes at one time slice**

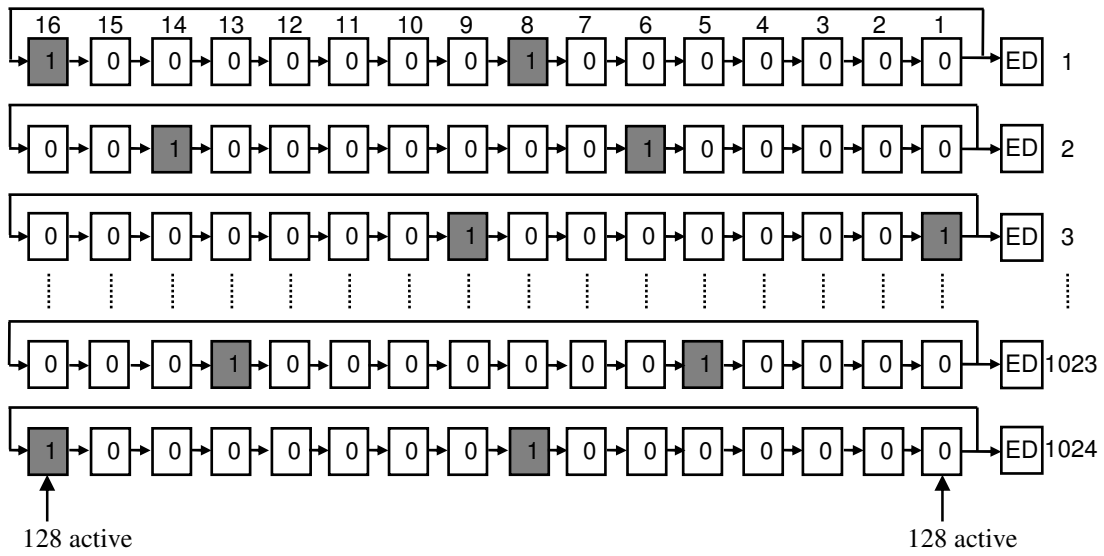
Figure 23 shows an illustration of the stimulus current waveforms with groups of 64 simultaneously active electrodes. In one refresh cycle, there are 16 time slices, at each of which 64 electrodes are activated. As a result, 64 cathodic-first biphasic current waveforms are generated in each group of 64 electrodes at each time slice.



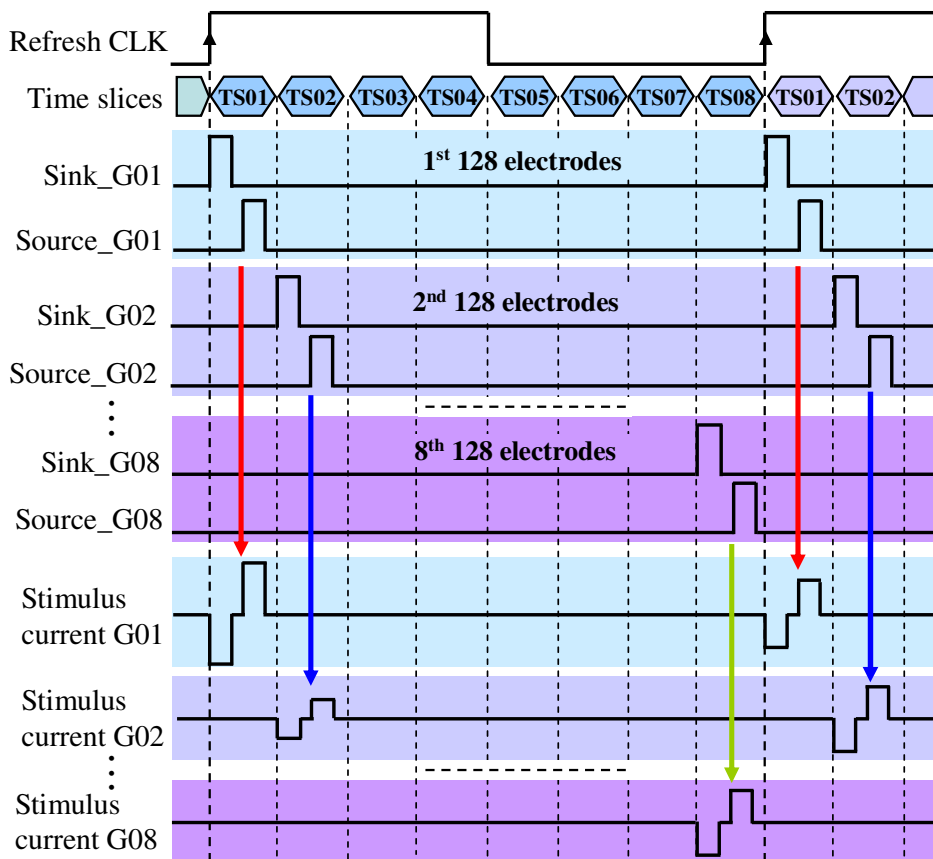
**Figure 23** Waveform illustration of the stimulation approach using stimulus current amplitude with groups of 64 simultaneously active electrodes

Another example of the freedom in selecting any number of electrodes is illustrated in Figure 24. In this stimulation case, the refresh rate is kept at 60 Hz but the total stimulus current pulse duration is now increased to 2 ms to allow more charge to be injected into tissues, which results in only 8 time slices and, therefore, 128 electrode drivers need to be activated at each time slice. This is easily done by writing 128 1's at each time slice and repeating after 8 time slices. An illustration of this stimulation case is given in Figure 25, where 1024 electrodes are divided into 8 groups of 128 electrodes.





**Figure 24 Stimulation with 128 active electrodes at one time slice**



**Figure 25 Waveform illustration of the stimulation approach using stimulus current amplitude with groups of 128 simultaneously active electrodes**

From the stimulation cases above, it can be seen that the number of available time slices is reversely proportional to the number of simultaneously active electrodes. The number of simultaneously active electrodes is expected to be as small as possible as the stimulator may not have enough instantaneous power to stimulate a huge number of electrodes at the same time. Because the total stimulus pulse normally is 1 ms or 2 ms, it is likely that the number of simultaneously active electrodes is normally 64 or 128, respectively.

The selection of active electrodes can be pre-defined or on-the-fly. On-the-fly selection of electrodes requires more data transmission bandwidth and can probably not be necessary due to the periodical manner of the stimulation operation. In fact, as long as any electrode in the whole array can be stimulated in every 60 Hz for flicker-free vision, the electrode location does not matter. Therefore, in this stimulator, it is determined that the selection of active electrodes is pre-defined during configuration stage of the stimulator's operation to reduce data transmission bandwidth.

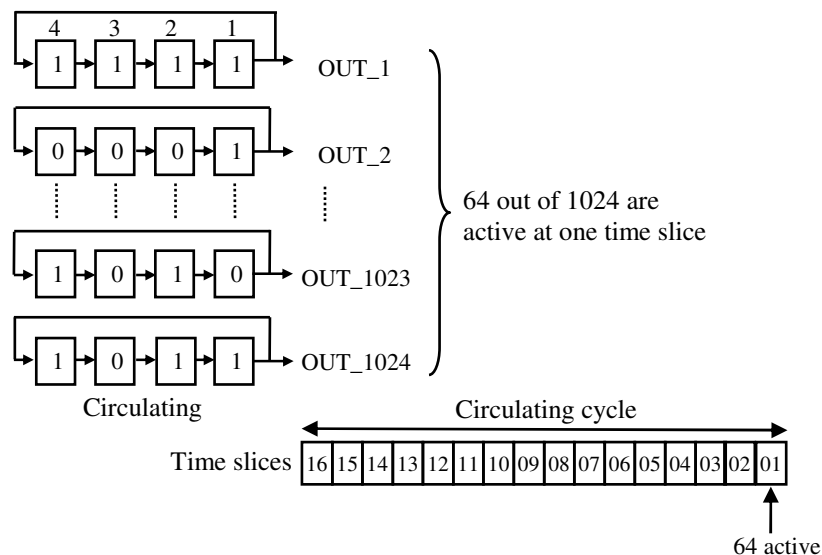
In bipolar stimulation configuration where return electrodes are on the same array as active electrodes, an identical array of sequencers is also used to select return electrodes. As a result, each electrode is controlled by two sequencers, and they have to be controlled in such a way that one does not conflict with the other because an electrode can not be both active and return at the same time slice.

In summary, by using two sequencers at each electrode driver, any electrode and any number of them can be selected at any time slice, which allows any patterns of electrodes to be stimulated at any time. The time interleaving behavior of electrode selection also helps reduce the instantaneous stimulation power, which needs to be as small as possible as the power is wirelessly transferred.

## **2.8 Represent brightness using stimulation rate with the help of sequencers**

In order to implement the stimulation approach which uses rate of stimulation to represent phosphene brightness, the idea of using sequencer is also applied. In this stimulator, stimulation rate data is represented by 4 bits and is stored at each electrode driver by a shift register which operates similarly to the sequencers as shown in Figure

26. Stimulation rate data is updated at a rate equal to image update rate. After updated, stimulation rate data is stimulated (refreshed) twice. In one stimulation refresh cycle, all of these 4 bits are circulated at a rate of 4 times faster than the refresh rate. Within one circulating cycle, there are 16 time slices at each of which 64 electrodes are active. Depending on the binary value at the output of each shift register, the corresponding electrode driver delivers a stimulus pulse to its electrode or not. As a result, after 4 circulating cycles (equal to 1 refresh cycle) every electrode in the array is selected 4 times, at each of which there exists a stimulus pulse or not depending on the binary value at the corresponding output of the driving shift register. Therefore, the contents of the shift registers define the number of stimulation pulses and the locations of them.

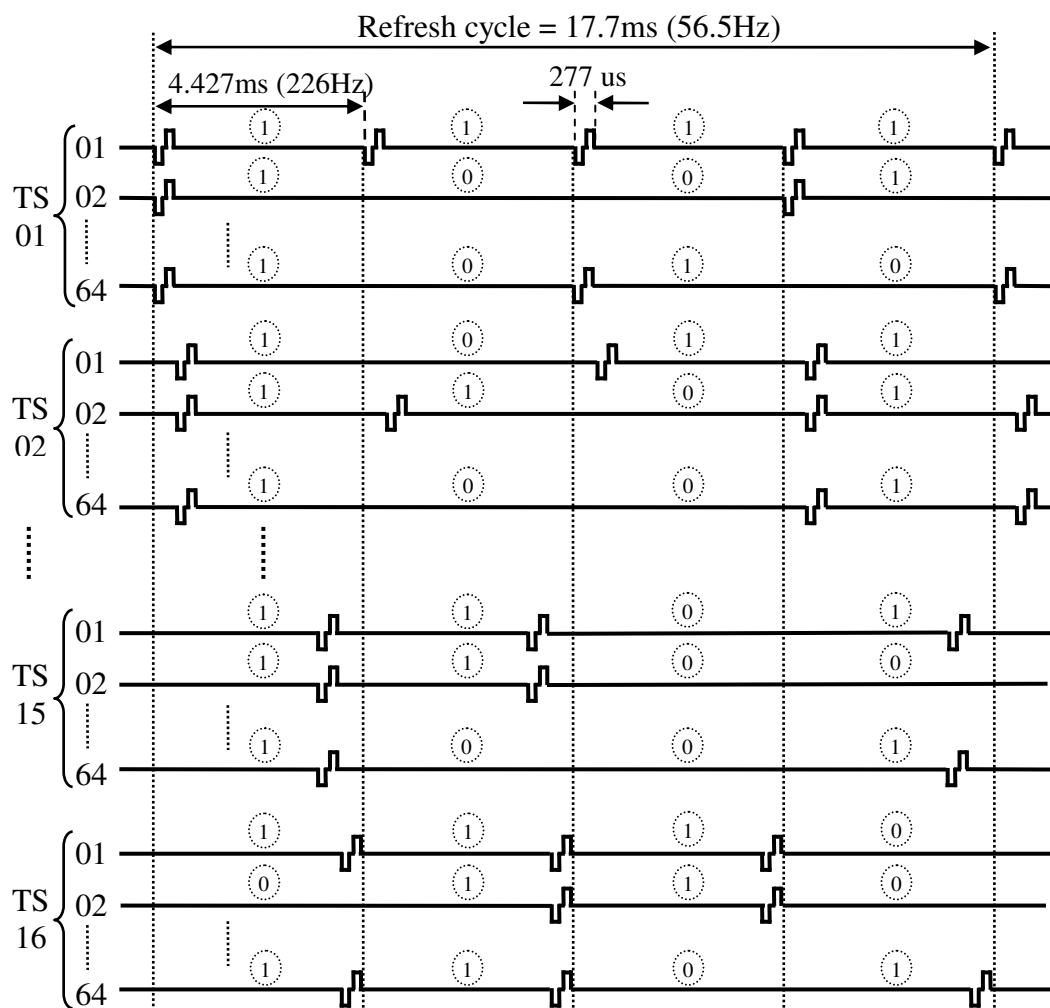


**Figure 26 Implementation of rate stimulation using sequencers**

Figure 27 shows waveform illustration of an example where rate of stimulation is used. In this example, 1024 electrodes are divided into 16 groups of 64 electrodes, each of which is activated at a time slice (from TS 01 to TS 16). In a stimulation refresh period of 17.7 ms (56.5 Hz), a faster stimulation rate of 226 Hz (4.427 ms) is used with total stimulus pulse duration of 0.277 ms (4.427ms/16), and different number of stimulus pulses is encoded to represent different brightness levels.

The stimulation refresh rate in this example is 56.5 Hz instead of 60 Hz because it is used by the prototype stimulator to be presented in Chapter 5. **From this point on, the**

stimulation refresh rate will be 56.5 Hz and the image data update rate will be a half of that (28.2 Hz) to conform to the fabricated prototype 64-electrode stimulator. As illustrated, in one stimulation refresh period, although there are only 5 possible numbers of pulses, from 0 to 4, to represent brightness levels, the locations of them may have certain effects. Therefore, different combinations of the number of pulses and pulse locations can represent different brightness levels.

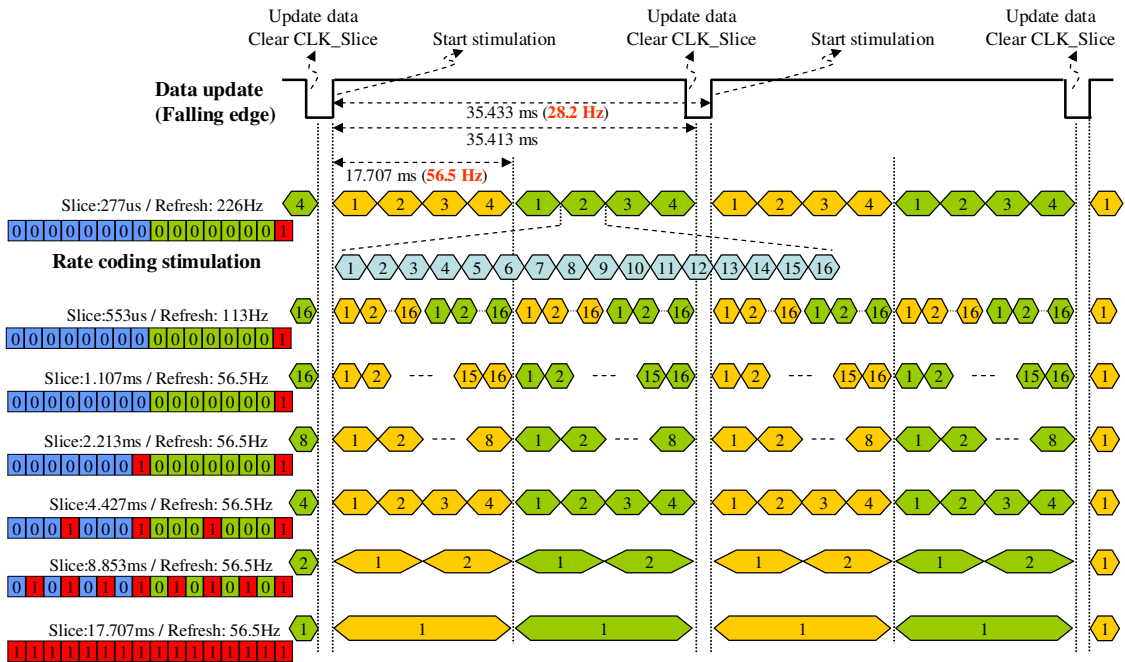


**Figure 27** Waveform illustration of the stimulation approach using rate of stimulation with 16 groups of 64 simultaneously active electrodes

In short, using shift registers as sequencers helps not only realizing full freedom in electrode selection but also implementing stimulation using rate.

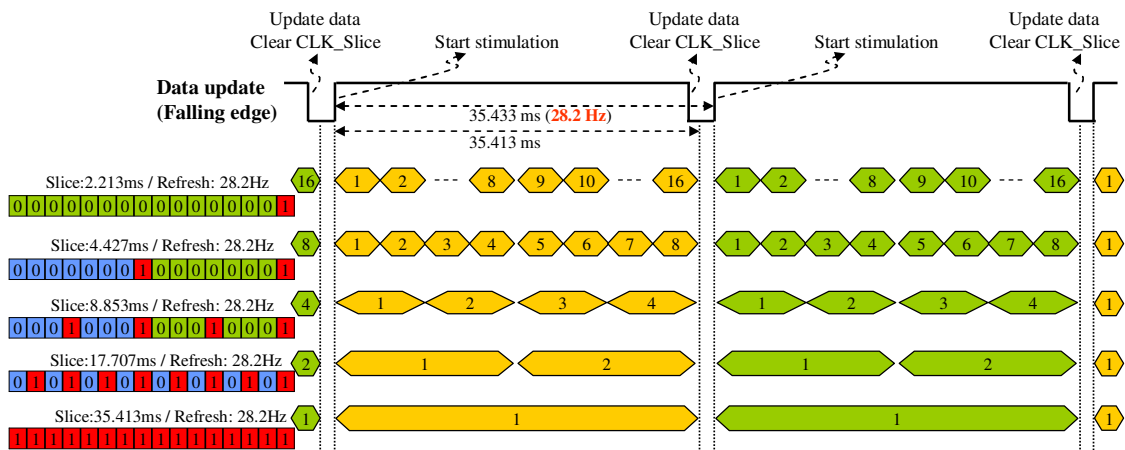
## 2.9 Various stimulation refresh rates and pulse durations

In retinal prostheses, the stimulation rate is usually chosen between 50 and 60 Hz to achieve flicker-free vision, and total stimulus pulse duration including both phases is usually between 1 ms and 2 ms [4, 36, 49]. Nevertheless, other stimulation rates and stimulus pulse durations should also be tried to investigate the effect of the timing differences. The stimulator in this thesis has the ability of generating various stimulation refresh rates and stimulus pulse durations. The combination of the sequencers and different time slice durations gives a lot of different stimulation refresh rates and stimulus pulse durations. Figure 28 gives an illustration of generating three different refresh rates of 226 Hz, 113 Hz, and 56.5 Hz. The refresh rate of 226 Hz is used in stimulation using rate of pulses (rate coding stimulation). With the refresh rate of 56.5 Hz, several time slice durations can be used. Longer time slice durations allow longer pulse durations to be used. However, longer time slice durations result in less number of time slices, which then requires more number of simultaneously active electrodes. Again, in the prototype 64-electrode stimulator to be presented in Chapter 5, the normal stimulation refresh rate is 56.5 Hz and the data update rate is 28.2 Hz, which are slightly different from the theoretical 60 Hz and 30 Hz, respectively. This slight difference is due to the way the prototype stimulator uses its system clock of 300 kHz to generate the timing information, and it is believed that this difference makes no effect to the stimulating operation.



**Figure 28** Waveform illustration of generating different time slice durations

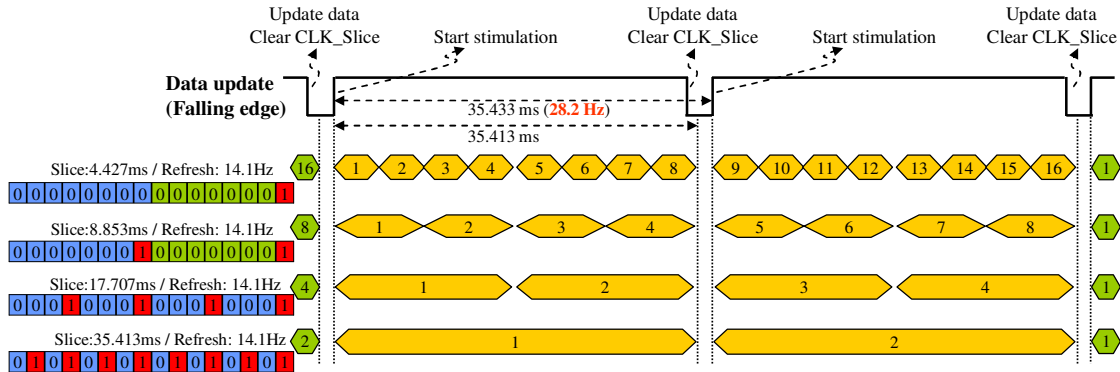
Figure 29 gives an illustration of using a refresh rate of 28.2 Hz with 5 different possible time slice durations ranging from 2.213 ms to 35.413 ms.



**Figure 29** Waveform illustration of generating different time slice durations at refresh rate of 28.2 Hz

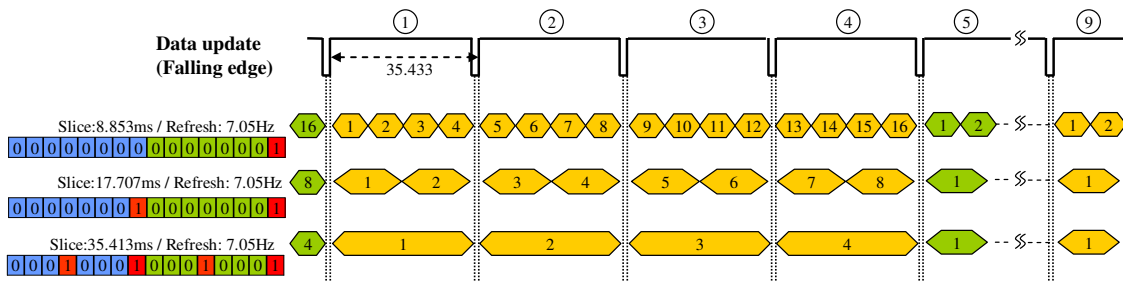
An illustration of stimulation using a refresh rate of 14.1 Hz is shown in Figure 30. With this refresh rate, there are 4 different possible time slice durations from 4.427 ms to 35.413 ms. Because the refresh rate is now a half of data update rate, the same image

date is updated twice. Date update rate is fixed to 28.2 Hz in order not to affect the baseband data processing.



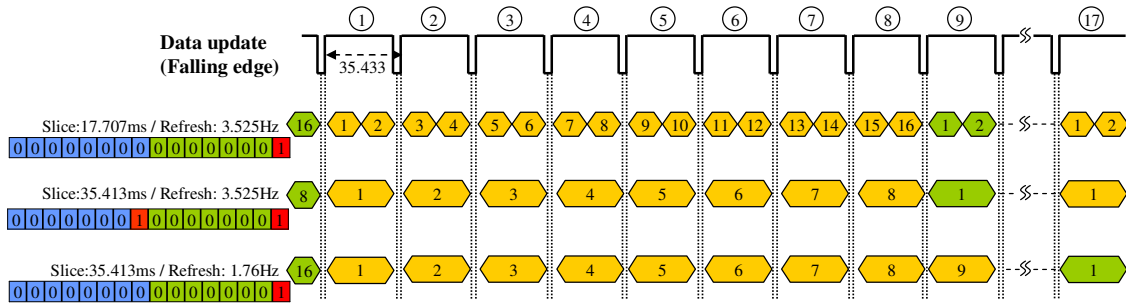
**Figure 30 Waveform illustration of generating different time slice duration at refresh rate of 14.1 Hz**

Figure 31 illustrates a stimulation strategy with a refresh rate of 7.05 Hz with 3 different possible time slice durations of 8.853 ms, 17.707 ms, and 35.413 ms. The same image data is updated 4 times within one refresh cycle as the data update rate is now 4 times higher than the stimulation refresh rate.



**Figure 31 Waveform illustration of generating different time slice duration at refresh rate of 7.05 Hz**

Figure 32 shows an illustration of stimulation using very low rates of 3.525 Hz and 1.76 Hz. Time slice durations for these two refresh rates are also very long, 17.707 ms or 35.413 ms. The same image data is updated 16 times or 32 times within one refresh cycle.



**Figure 32** Waveform illustration of low stimulation frequencies with long time slice durations

In summary, to realize stimulation strategies with different timing information, the proposed stimulator can support various stimulation refresh rates and wide-range stimulus pulse durations.

## 2.10 Summary of stimulation flexibility

The advance of implementing the high resolution retinal stimulator using small-scale CMOS process is the ability of providing a lot of flexibility which helps realizing as many stimulation strategies as possible. The flexibility of the proposed stimulator is summarized as the followings.

The stimulator supports both varying stimulus current amplitude and varying stimulation rate to represent different brightness levels.

The stimulator supports both bipolar stimulation where return electrodes are from the electrode array and monopolar stimulation where a remote common electrode acts as return electrode.

In the stimulator, data update rate and stimulation refresh rate are separated to help reducing data transmission bandwidth, which is critical when the MICS band's bandwidth is just 300 kHz.

A novel electrode driver topology allows any electrode in the array to act as active or return. The driver operates in an alternately push-pull manner, in which only one current source or sink works at a time. This reduces by a half the headroom voltage, which is



extremely advantageous because the supply voltage is limited. This also helps controlling charge balance at active electrodes.

One electrode is driven by its own individual driver which consists of two sequencers, which allows full freedom in electrode selection, any electrodes and any number of them can be selected as active or return at any time slice.

Each current source/sink can generate 64 different amplitude levels at each of 64 different step sizes, which makes the stimulus current amplitude range from 80 nA to 317.5  $\mu$ A. The combination of stimulus current and threshold current helps fully utilizing 64 different levels above the depolarization threshold at each electrode, which then makes the total current delivered to each electrode range from 80 nA to 635.04  $\mu$ A.

The stimulator supports various stimulation refresh rates ranging from 1.76 Hz to 226 Hz with various pulse durations ranging from 227  $\mu$ s to 35.413 ms.

To sum up, the high density stimulator supports a wide variety of stimulation flexibility to implement several different stimulation strategies. All of the proposed flexibility is going to be verified with a prototype 64-electrode stimulator which will be presented in Chapter 5.

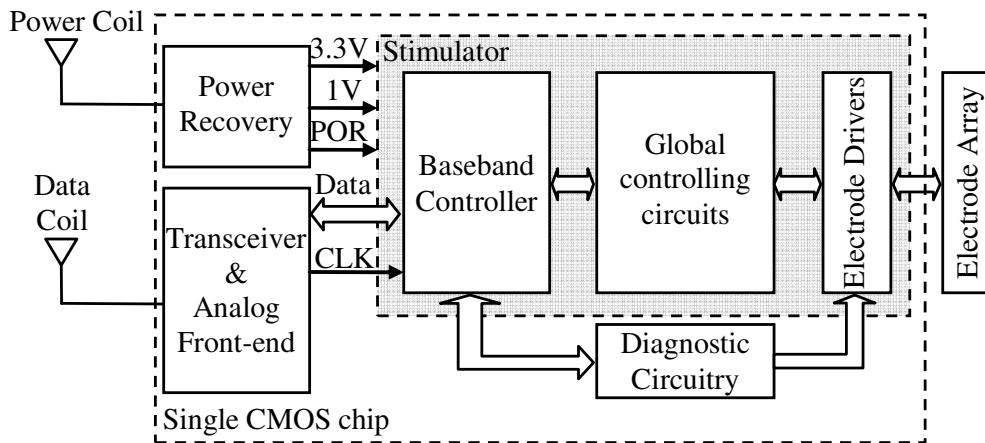


# **Chapter 3 System design considerations and global controlling circuits**

Designing a flexible stimulator with 1024 electrode drivers faces many challenges, among which are the required data rate to provide sufficient real-time image data and the signal routing which supplies data to every electrode driver. This chapter presents the high acuity retinal chip's architecture and discusses the distributed design approach which simplifies the signal routing and enhances the flexibility of the stimulator. Global control circuits defining timing information and global bias current are also presented in detail.

## **3.1 System architecture**

The implantable device placed on the retina surface receives the image information from the external device and converts it into corresponding stimulus currents to stimulate the ganglion cells via an array of electrodes. Power for the implantable device is transferred from the external device via an inductive link. Figure 33 shows the architecture of the implantable device. The implantable device consists of a power recovery circuit with its coil for power reception, a transceiver with its coil and an analog front-end for data communication, a stimulator for processing image data and stimulating the electrode array, diagnostic circuitry for monitoring the implantable device's conditions (such as temperature and electrode-tissue contact), and an electrode array for interfacing the stimulator to the targeted tissue cells. The whole implantable device, except for the electrode array and the coils, is integrated in one single silicon chip (implantable chip).



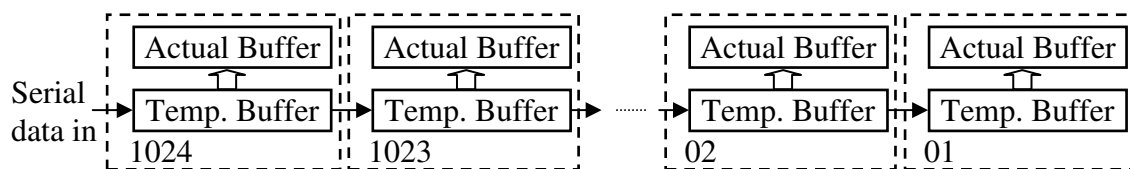
**Figure 33 System architecture of the implantable chip**

This thesis focuses on the stimulator which consists of a baseband controller, global controlling circuits, and electrode drivers. The baseband controller processes digital data from the transceiver. The baseband controller will be presented in detail with the prototype stimulator in Chapter 5. Electrode drivers are used to deliver stimulus currents to tissues via the electrode array and will be described in-depth in Chapter 4. Global control circuits are implemented to generate timing information and global bias current. These are presented in detail in the following sections.

### 3.2 Distributed design approach

In the proposed stimulator, each electrode is controlled by its own individual electrode driver. Therefore, there are 1024 electrode drivers controlling 1024 electrodes. Each electrode driver needs a certain amount of stimulation data defining stimulus current pulse to drive its electrode. Before doing any stimulation, these data must be stored in a buffer to verify their validity. The location of this buffer has great effect on the data routing of the stimulator. Indeed, data received from the receiver is serially shifted into the data buffer, if the buffer is located centrally, the routing from the buffer to the driver array will be extremely complicated as each electrode driver need several data bits. On the other hand, if the buffer is broken into 1024 smaller buffers and distributed to 1024 electrode drivers, the routing becomes significantly simplified. These two data buffering topologies have been discussed in [36]. The limitation of the serial topology according to this report is that it loses flexibility since the order of data

shifting is fixed and while a data packet is shifted in, no stimulation can be performed. However, in this research, the separation of data update rate and stimulation refresh rate can help overcome this limitation. Indeed, in every electrode driver, there are two kinds of buffers, one of which is a temporary data buffer (shift register) to store data before verified and the other is actual data buffer to store valid data for stimulation as shown in Figure 34. Data is serially shifted into the temporary buffers to be validated. If data is valid, it will be loaded into the actual buffers in parallel. The stimulation uses data in the actual buffers and the order of stimulation is defined by the sequencers, independently of the order of data shifting. Therefore, the data shifting activity does not affect the stimulation activity, and the order of data shifting does not matter.



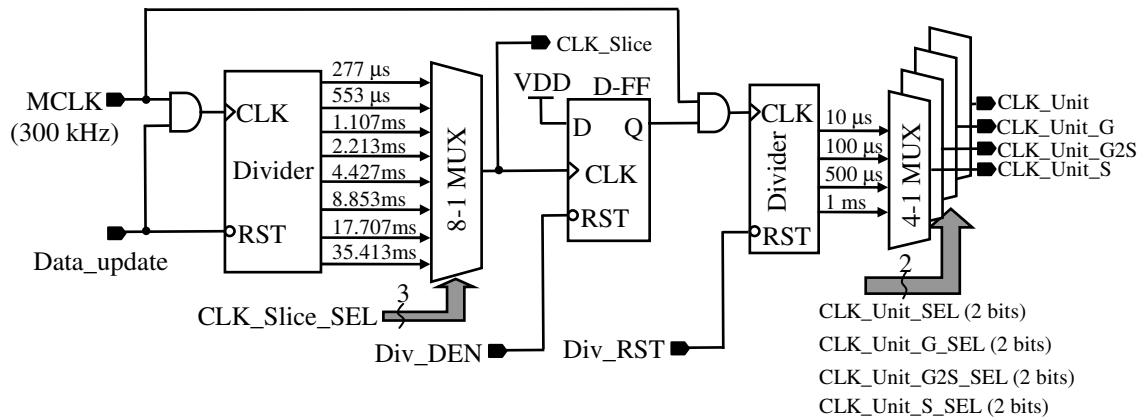
**Figure 34 Serial data shifting**

In short, distributing the global data buffer into local data buffers helps simplifying the signal routing while keeping flexibility. The following 4 sections will describe 4 global controlling circuits which are used to set up the global parameters of the stimulator such as time slice duration, unit clocks, pulse duration, and global bias current. Common return circuitry used to control the remote common return electrode is also presented.

### 3.3 Clock profile

Global timing information defining time slice duration and stimulus pulse duration is generated by a clock profile circuit shown in Figure 35. A master clock of 300 kHz is fed into a divider – slice divider - after every data updating time. One out of 8 time slice clocks is selected by 3 bits (CLK\_Slice\_SEL) via an 8-to-1 multiplexer. Within one time slice, a stimulus pulse including 5 different timing components is generated. Those components are stimulation phase, interphase gap, return phase, gap to short, and short as shown in Figure 5. The time units for each of these timing components can be 10  $\mu$ s,

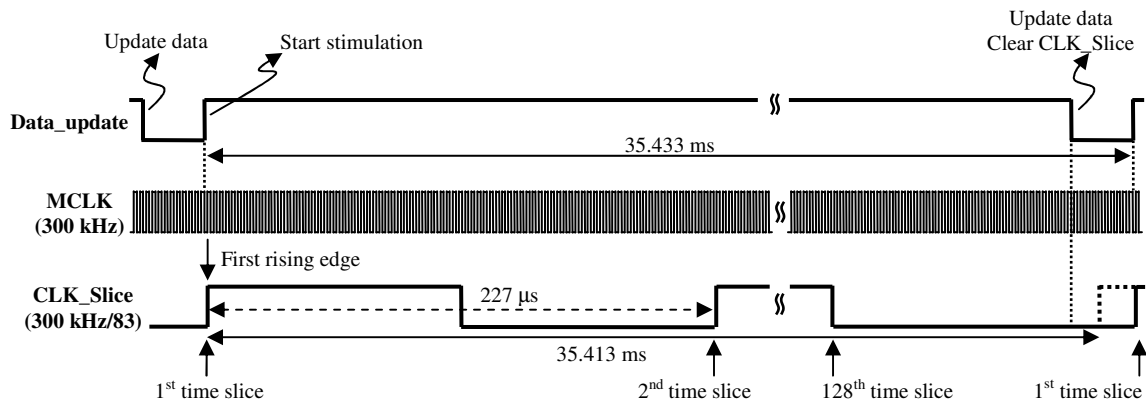
100  $\mu$ s, 500  $\mu$ s, and 1 ms. These unit clocks are also generated from the master clock by another divider – called unit divider. Four 4-to-1 multiplexers are used to select unit clocks for these components. The two main components – stimulation phase and return phase – use the same unit clock selected by CLK\_Unit\_SEL, while three others – interphase gap, gap to short, and short – use their own independent unit clocks selected by CLK\_Unit\_G\_SEL, CLK\_Unit\_G2S\_SEL, and CLK\_Unit\_S\_SEL, respectively. Therefore, the duration of each of these timing components can be selected in a wide range with 4 possible time units. The two signals Div\_DEN and Div\_RST are used to disable and reset the unit divider, respectively. The unit divider is reset when the generation of each timing component is finished, and it is disabled when the generation of the last timing component is done.



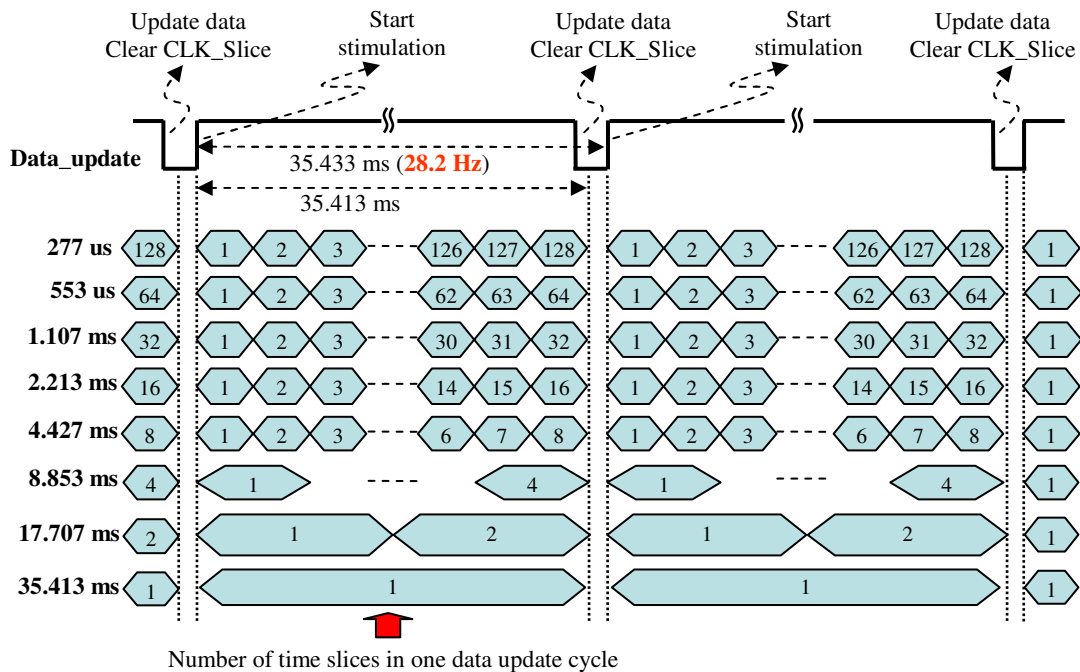
**Figure 35 Schematic of the clock profile**

Figure 36 shows an illustration of generating the time slice clock of 227  $\mu$ s from the master clock of 300 kHz. Right after data is updated, the first time slice is generated. The Data\_update signal resets the slice divider when it goes low before initiating another stimulating cycle.

The generation of 8 different time slice clocks is illustrated in Figure 37. It can be seen that the number of time slices within one data updating cycle is inversely proportional to the time slice duration.



**Figure 36** Waveform illustration of the time slice clock's generation



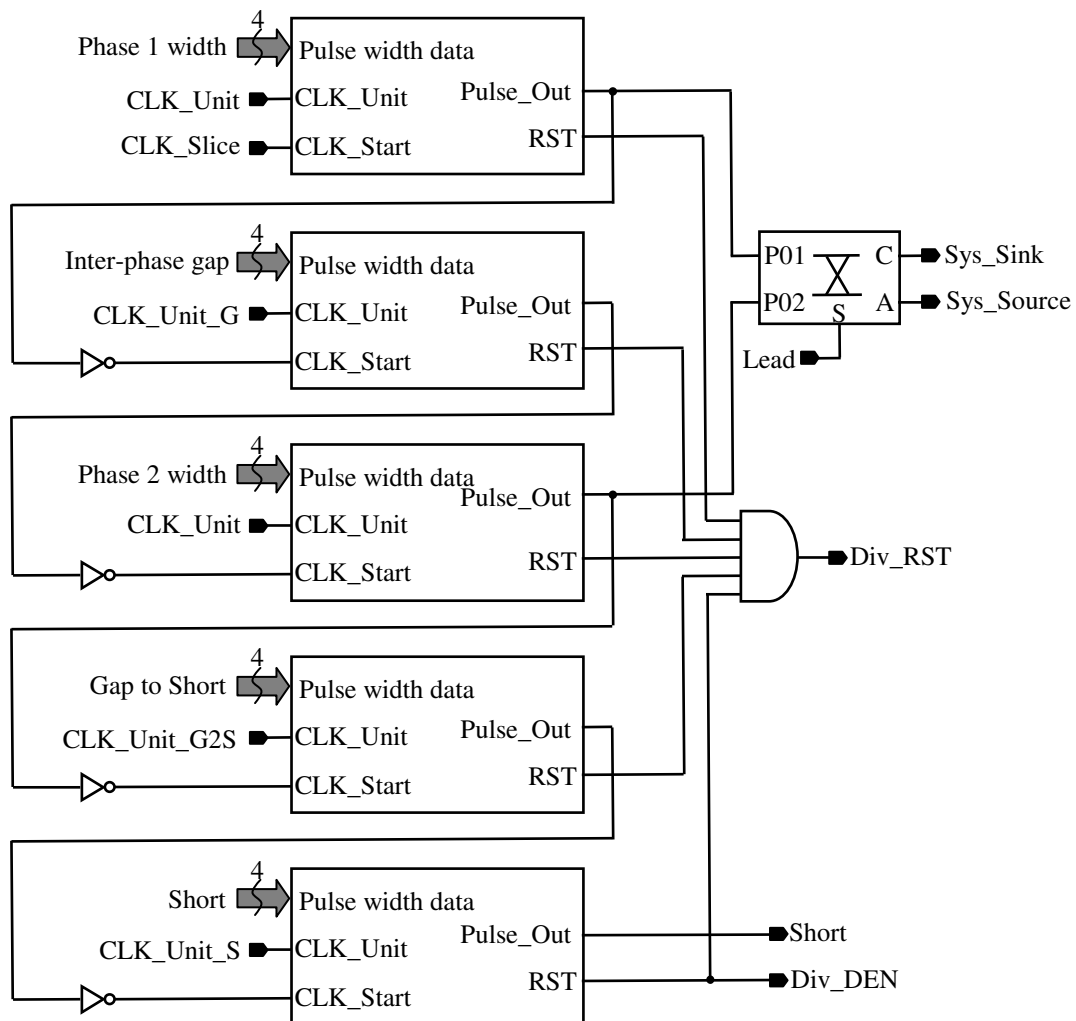
**Figure 37** Waveform illustration for generating different time slice clocks

In summary, there are 8 different time slice clocks of 277  $\mu$ s, 553  $\mu$ s, 1.107 ms, 2.213 ms, 4.427 ms, 8.853 ms, 17.707 ms, and 35.413 ms with 4 different unit clocks of 10  $\mu$ s, 100  $\mu$ s, 500  $\mu$ s, and 1 ms. These varieties make a wide-range of global timing parameters.

### 3.4 Stimulus pulse generator

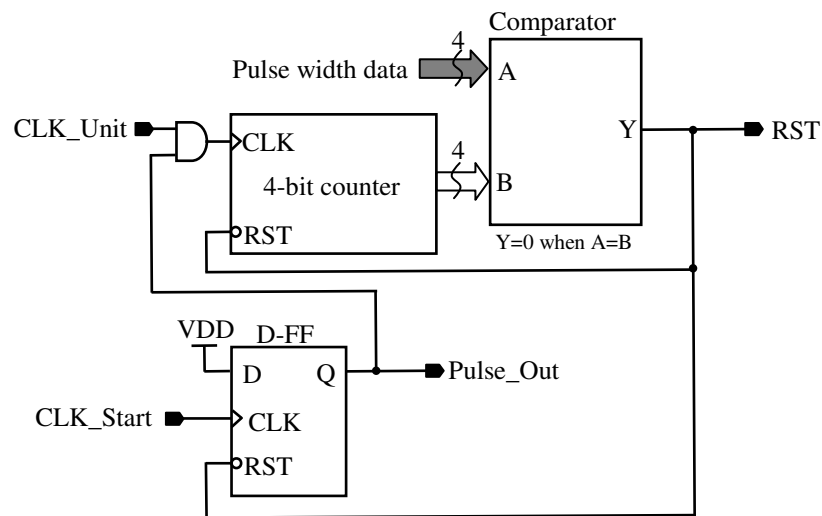
The stimulus pulse generator shown in Figure 38 defines the timing information for the stimulus pulse which includes 5 different timing components as mentioned in the previous section. The stimulus pulse generator consists of 5 single pulse generators corresponding to 5 different timing components as shown in Figure 39. A single pulse generator consists of a DFF, a 4-bit counter, and a comparator. The pulse is triggered by the rising edge of `CLK_Start`, the pulse duration is determined by the 4-bit pulse width data. When the pulse is started, the 4-bit counter is enabled and starts to count with the time base `CLK_Unit`. The comparator output goes low when the counted value equals the pulse width data. This active-low output of the counter pulls down the `Pulse_Out` signal (by clearing the DFF) and clears the counter output. The generation of the pulse is finished.





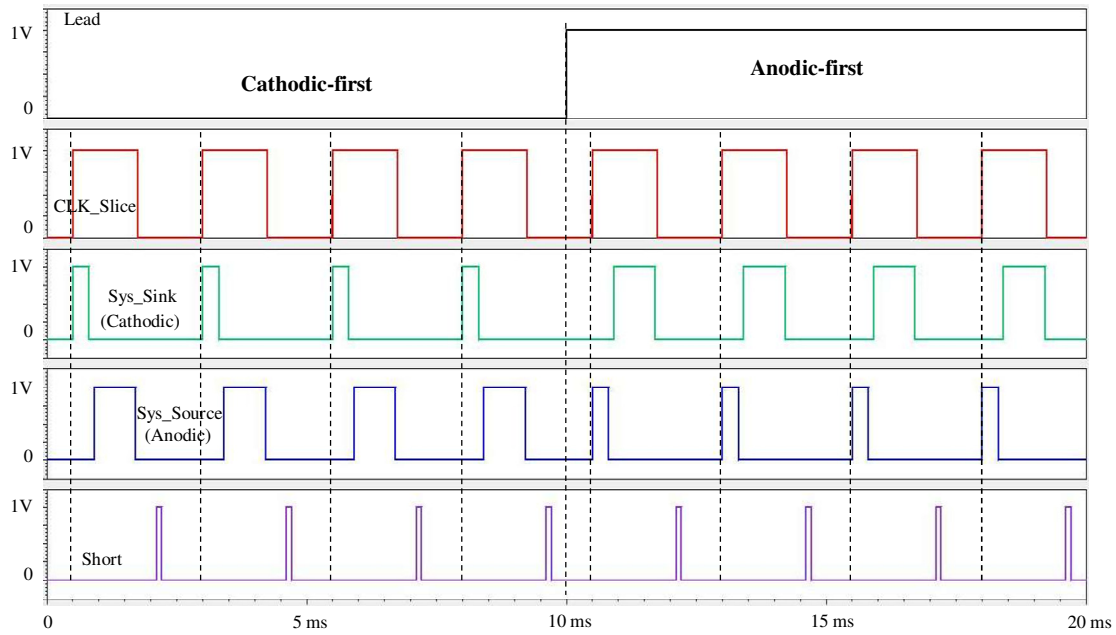
**Figure 38 Schematic of the stimulus pulse generator**

The stimulus pulse generator starts generating the first timing component of the stimulus pulse – stimulation phase - at the rising edge of the time slice clock (CLK\_Slice). On the finishing of the first component, the generation of the second component begins. The whole pulse generating process continues in this manner until the last component is generated. A selection bit (Lead) controls the leading pulse (cathodic first or anodic first) with a simple switch matrix.



**Figure 39 Schematic of the single pulse generator**

Figure 40 shows simulation results of the stimulus pulse generator. Two cases of leading pulse – cathodic first and anodic first – are shown. Within one time slice, the whole stimulus pulse including 5 components of different durations is generated. In the cathodic-first case, the pulse begins with the system sink signal Sys\_Sink which controls the cathodic phase of the stimulus pulse. While in the case of anodic-first, the pulse starts with the system source signal Sys\_Source which controls the anodic phase of the stimulus pulse.



**Figure 40 Simulation result of the stimulus pulse generator**

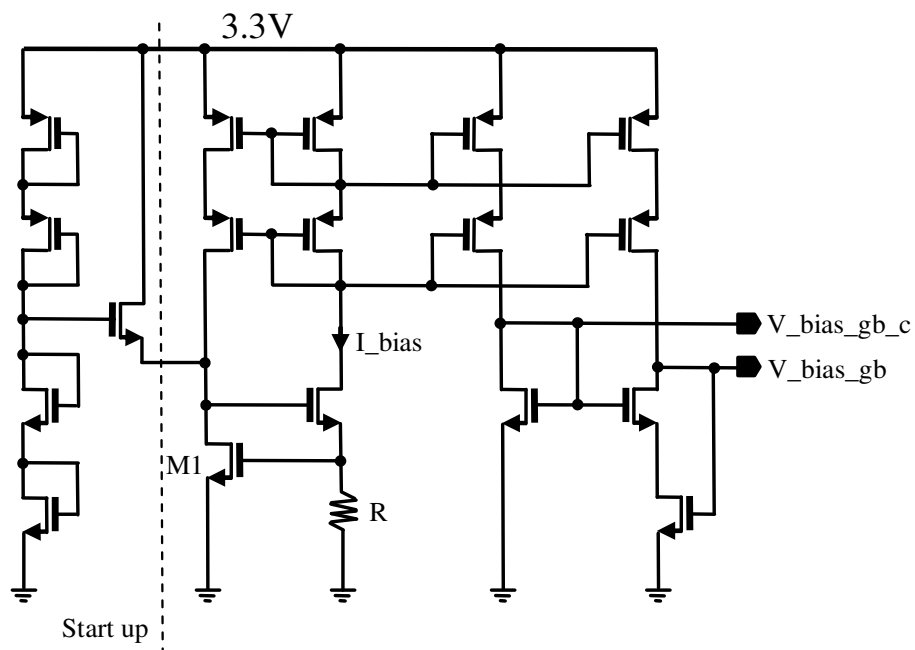
In summary, each of 5 components of a stimulus pulse is independently controlled with a variety of time durations based on 4 different time units of 10  $\mu$ s, 100  $\mu$ s, 500  $\mu$ s, and 1 ms. Table 3 lists all the possible time durations for each of 5 components of a stimulus pulse.

**Table 3 Time duration corresponding to different digital input data**

Digi\Unit	10us	100us	500us	1ms
0000	0	0	0	0
0001	0	0	0	0
0010	10us	100us	500us	1ms
0011	20us	200us	1ms	2ms
0100	30us	300us	1.5ms	3ms
0101	40us	400us	2ms	4ms
0110	50us	500us	2.5ms	5ms
0111	60us	600us	3ms	6ms
1000	70us	700us	3.5ms	7ms
1001	80us	800us	4ms	8ms
1010	90us	900us	4.5ms	9ms
1011	100us	1ms	5ms	10ms
1100	110us	1.1ms	5.5ms	11ms
1101	120us	1.2ms	6ms	12ms
1110	130us	1.3ms	6.5ms	13ms
1111	140us	1.4ms	7ms	14ms

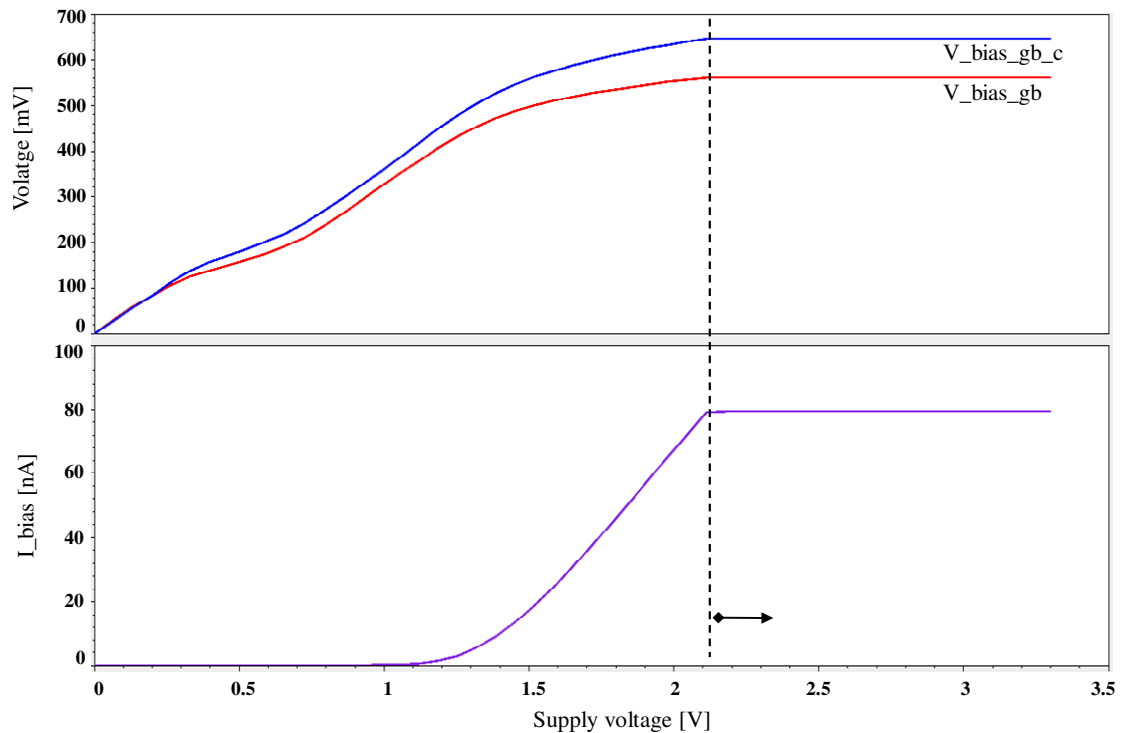
### 3.5 Global bias generator

The global bias generator delivers a primary bias current of 80 nA from which each electrode driver's output step currents are biased. This value of 80 nA of the bias current is biased up to 63 different levels by the local bias circuit at every electrode driver, and then each of these levels is then stepped up to 63 different levels at the output stage as mentioned in Section 2.5. This flexibility of the current bias topology relaxes the accuracy of the bias current, hence the design of the global bias generator. The bias generator used in this research is a threshold referenced self-biasing circuit [57, 58] as shown in Figure 41 due to its simplicity and supply independence. The bias current is given by  $V_{GS1}/R$  which depends on the threshold voltage of M1 and the resistance R. Because the stimulator will be used inside the human body where the temperature is pretty constant, the bias generator is not necessary to be temperature insensitive.



**Figure 41 Schematic of the global bias generator**

Figure 42 shows simulation result of the global bias generator. When supply voltage is more than 2.1V, a bias current of 80 nA is generated. This current is mirrored to the local bias circuit at each electrode driver via the two bias voltages  $V_{bias\_gb}$  and  $V_{bias\_gb\_c}$ .

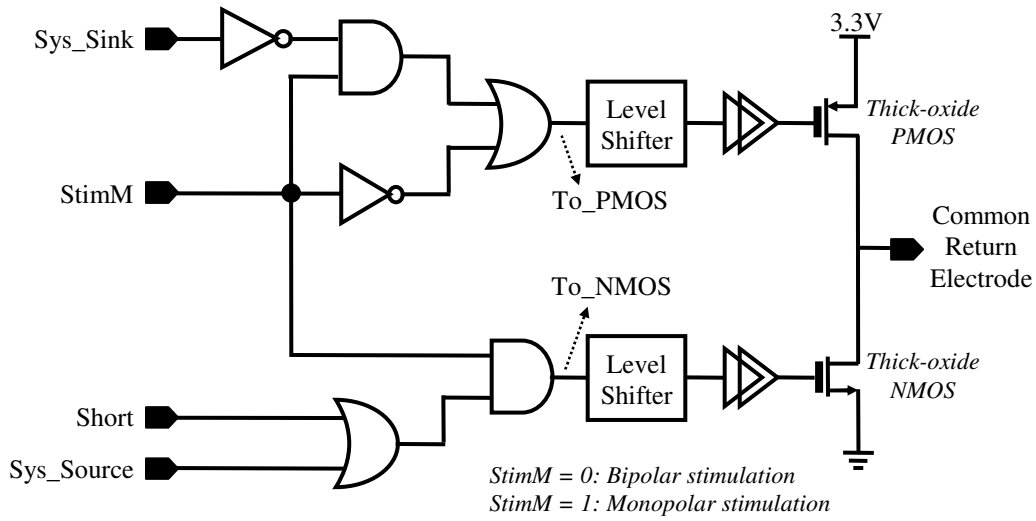


**Figure 42 Simulation result of the bias generator**

In short, a simple bias circuit is used to generate globally across all electrodes a primary bias current of 80 nA, which is used as the reference at each electrode driver.

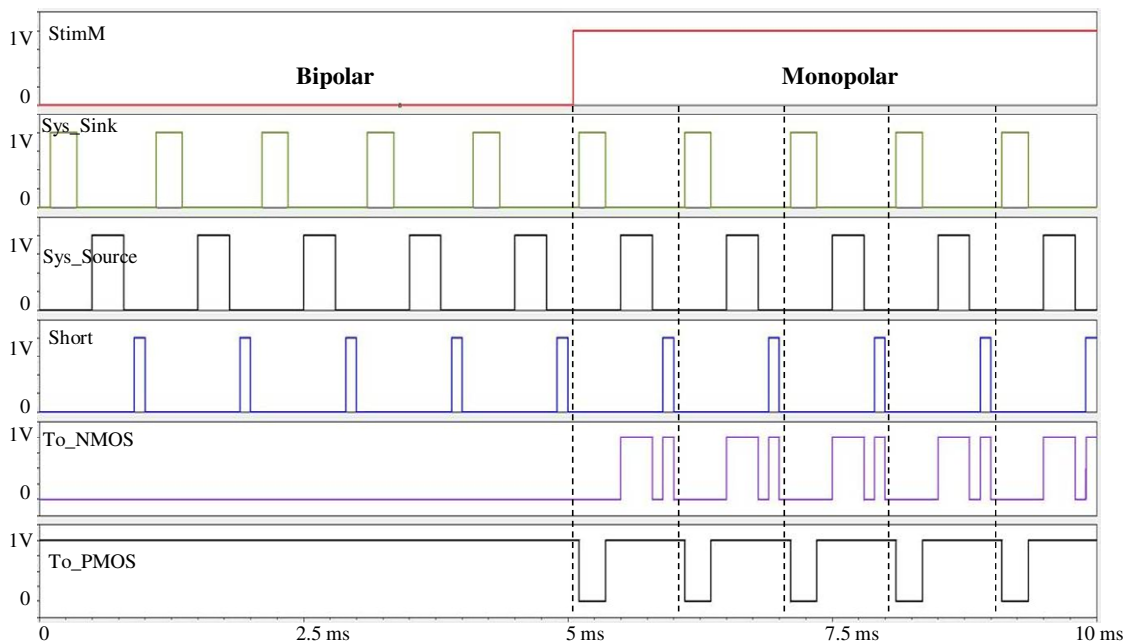
### 3.6 Common return circuitry

In monopolar stimulation, a remote big electrode is used as a return electrode. In this stimulator, a common return circuit is implemented to control this common return electrode. Its function is basically to connect the return electrode to VDD or GND depending on the phases of stimulation. Figure 44 shows the schematic of this circuit. A bit (StimM) defines stimulation mode – bipolar or monopolar. The phases of stimulation are defined by the Sys\_Sink and Sys\_Source signals. The output stages are implemented by two big thick-oxide transistors functioning as switches. Two level shifters are used to shift the voltage level of 1V at the control logic to 3.3V to drive the two thick-oxide transistors at the output.



**Figure 43 Schematic of the common return circuitry**

Simulation result of this common return circuit is given in Figure 45. When StimM is low, bipolar stimulation is selected, and the output stage is left floating. When StimM is high for monopolar stimulation, the common return electrode is connected to GND when Sys\_Source and Short are high, and is connected to VDD when Sys\_Sink is high.



**Figure 44 Simulation result of the common return circuitry**

### **3.7 Summary**

The stimulator's system architecture was described. A distributed design approach was proposed to simplify signal routing. Global controlling circuits were implemented to define global timing and bias information. A common return circuitry used to control the common return electrode in monopolar stimulation was also implemented.



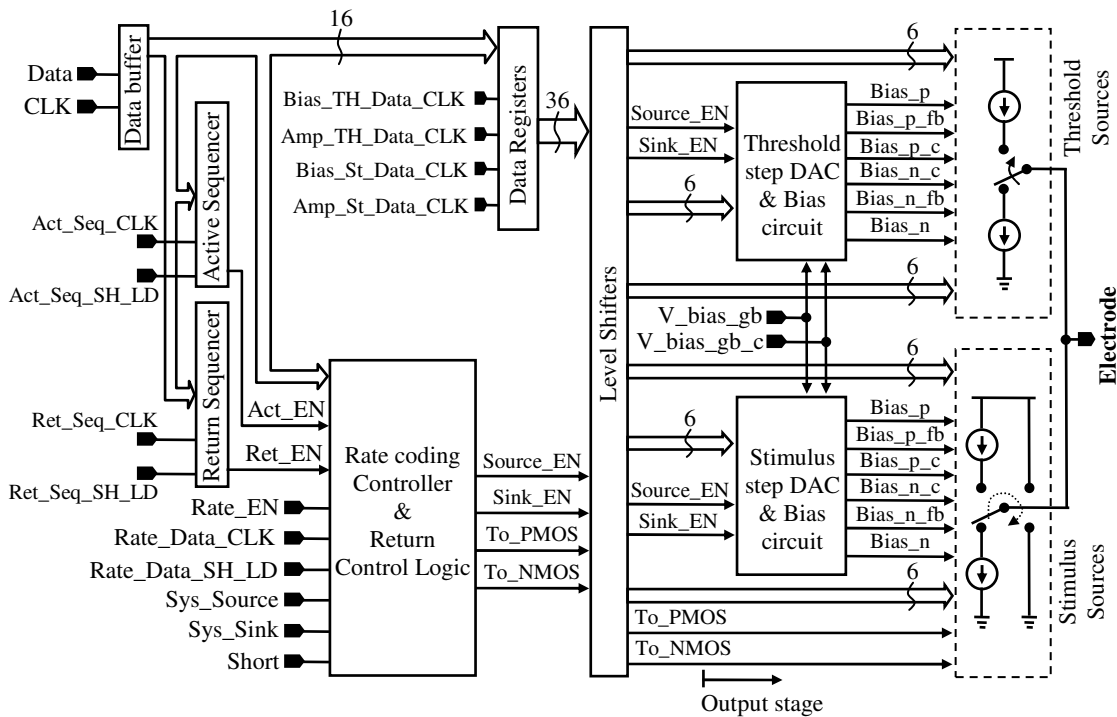


# Chapter 4 Electrode Driver

The design of the electrode driver is a key factor in achieving the proposed flexibility because in the distributed design approach, all the complexity is distributed to every electrode driver. This chapter describes the electrode driver for the stimulator. Detailed designs of all building blocks are presented.

## 4.1 Electrode driver architecture

The electrode driver topology described in Section 2.4 provides a lot of flexibility for the stimulator. Figure 45 shows a corresponding circuit implementation. The electrode driver consists of a digital part at the input and an analog part at the output with level shifters in between. The digital part is composed of a 16-bit data buffer storing temporary data, registers storing stimulation data, an active sequencer defining order when acting as active, a return sequencer defining order when acting as return, and a rate coding controller and return control logic. The output analog part consists of threshold current source and sink with their bias circuit, and stimulus current source and sink with their bias circuit as well. The output current delivered to electrode is the sum of the threshold current and the stimulus current as mentioned in Section 2.6. The digital part provides four controlling signals to connect the driver's output to current sources or current sinks or VDD or GND, and 36 digital data bits for the DAC's at the analog bias and output stage. The digital part works at a supply of 1V to minimize power consumption while the analog output part made of thick-oxide transistors is supplied by 3.3V to maximize stimulation voltage. Therefore, levels shifters are used between them to shift signals from 1V to 3.3V.

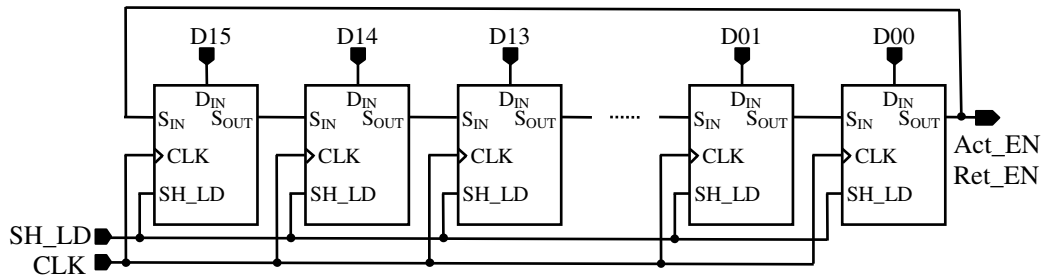


**Figure 45 Architecture of electrode driver**

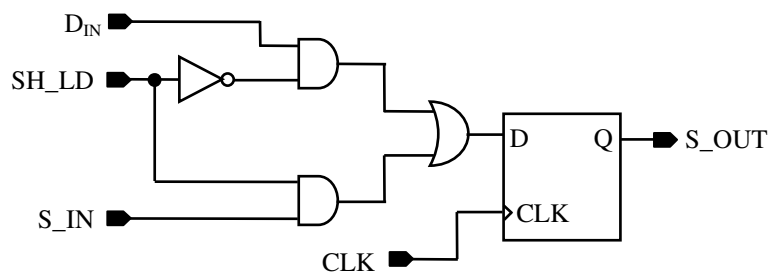
The following sections will describe in details all of these building blocks.

## 4.2 Active and return sequencers

The active and return sequencers allow full freedom in electrode selection. Schematic of the sequencer is shown in Figure 46. The sequencer is basically a 16-bit shift register comprising 16 synchronous input loading D-flip flops whose schematic is shown in Figure 47. The DFF output  $S_{OUT}$  is equal to the parallel input  $D_{IN}$  or the serial input  $S_{IN}$  at every rising edge of the clock  $CLK$  depending on the state of the  $SH\_LD$  signal. When  $SH\_LD$  is low,  $S_{OUT}$  is equal to  $D_{IN}$ , and when  $SH\_LD$  is high,  $S_{OUT}$  is equal to  $S_{IN}$ . Once the sequence data has been simultaneously loaded in, the sequencer keeps circulating to generate the sequence of stimulation for its driven electrode. The circulating rate of the sequencer is the time slice rate.



**Figure 46 Sequencer**



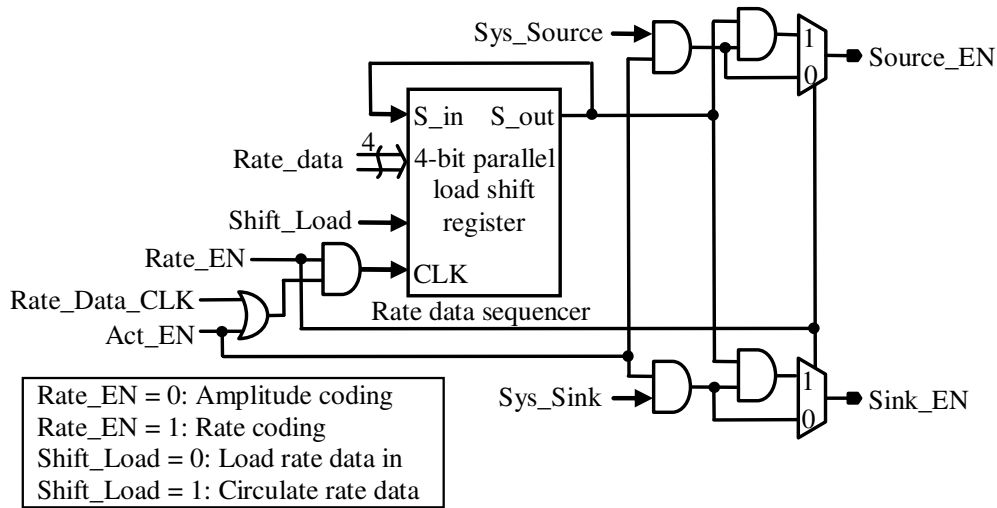
**Figure 47 Synchronous input loading D-flip flop**

### 4.3 Electrode driver control logic

The control logic of the electrode driver consists of a rate coding controller and control logic for the return path. The rate coding controller controls the driver's operation in two brightness coding modes – current amplitude coding and stimulation rate coding. The return path control logic controls the return path of each electrode driver when the electrode works as return.

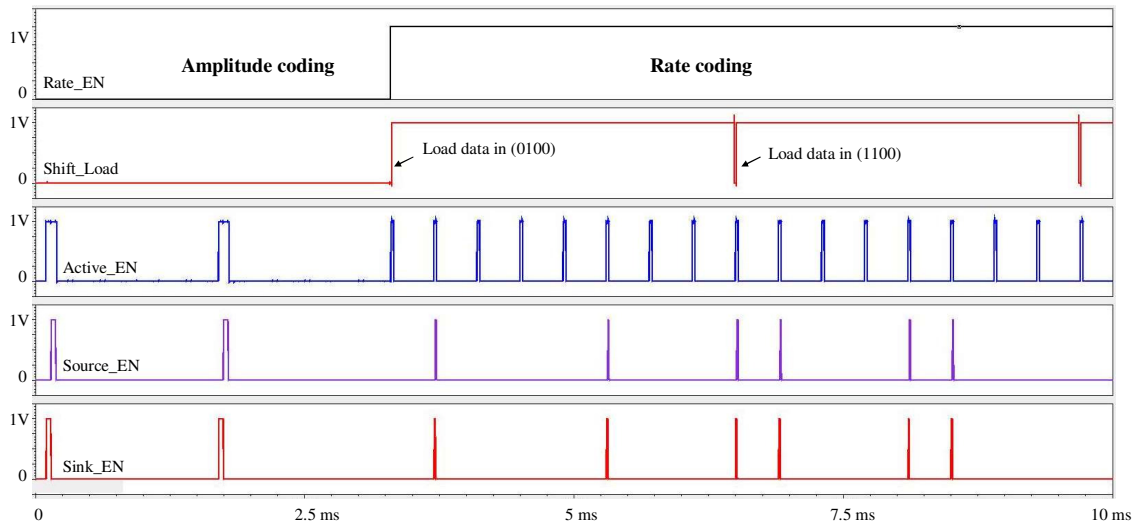
The rate coding controller shown in Figure 48 provides “enable” signals to the current sinks and sources at the output stage of current generators (Source\_EN and Sink\_EN). Depending on the brightness coding mode of the stimulator (amplitude coding when Rate\_EN is low, or rate coding when Rate\_EN is high), these signals are adjusted correspondingly. In the amplitude coding mode, the system sink (Sys\_Sink) and system source (Sys\_Source) signals are bypassed to the two “enable” signals (Sink\_EN and Source\_EN) with the control of the active “enable” signal (Act\_EN). In the rate coding mode, the 4-bit parallel load shift register (rate date sequencer) loads

data representing brightness in (at rising edge of Rate\_Data\_CLK) and then circulates until new data is loaded (circulate using Act\_EN).



**Figure 48 Schematic of the rate coding controller**

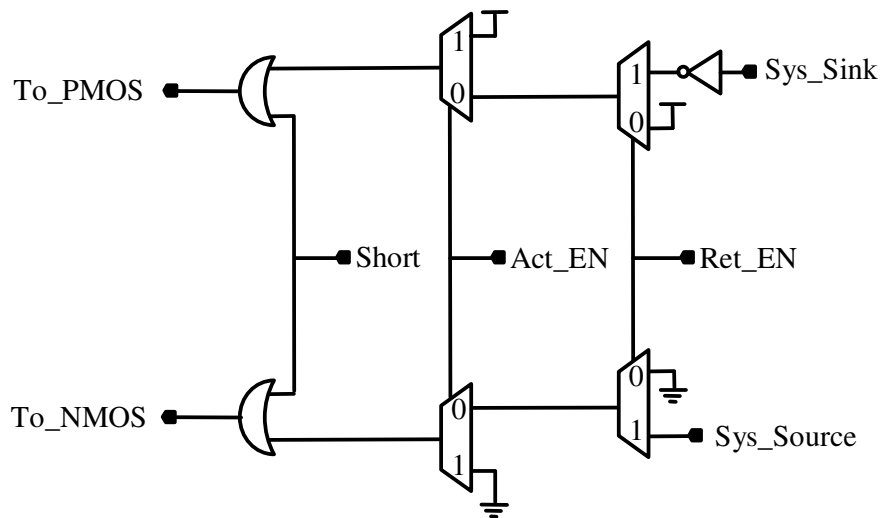
Figure 49 shows the simulation result of the rate coding controller. In the amplitude coding mode, the “enable” signals are wider and at lower frequency compared to the case of the rate coding mode. In rate coding mode, once a rate data pattern is loaded, it is refreshed twice before new rate data comes. This performs the approach where stimulation refresh rate is twice higher than the data update rate to reduce data transmission bandwidth. It can be seen that with the first rate data of ‘0100’, there is only one stimulus pulse (made of Source\_EN and Sink\_EN) appearing at the second stimulation time within one stimulation refresh cycle including four stimulation times. While with the rate data of ‘1100’, two stimulus pulses appear at the first two stimulation times. With rate data made of four bits, there are 5 possible stimulus pulses, which are 0, 1, 2, 3, or 4. However, the relative locations of them may have certain effect in tissue stimulation. For example, with 2 pulses out of 4 within one stimulation cycle, there are 6 possible different combinations of them, which are ‘1100’, ‘0011’, ‘1010’, ‘0101’, ‘1001’, and ‘0110’. These combinations deliver the same amount of charge but at different rates, hence may result in different effects.



**Figure 49 Simulation result of the rate coding controller**

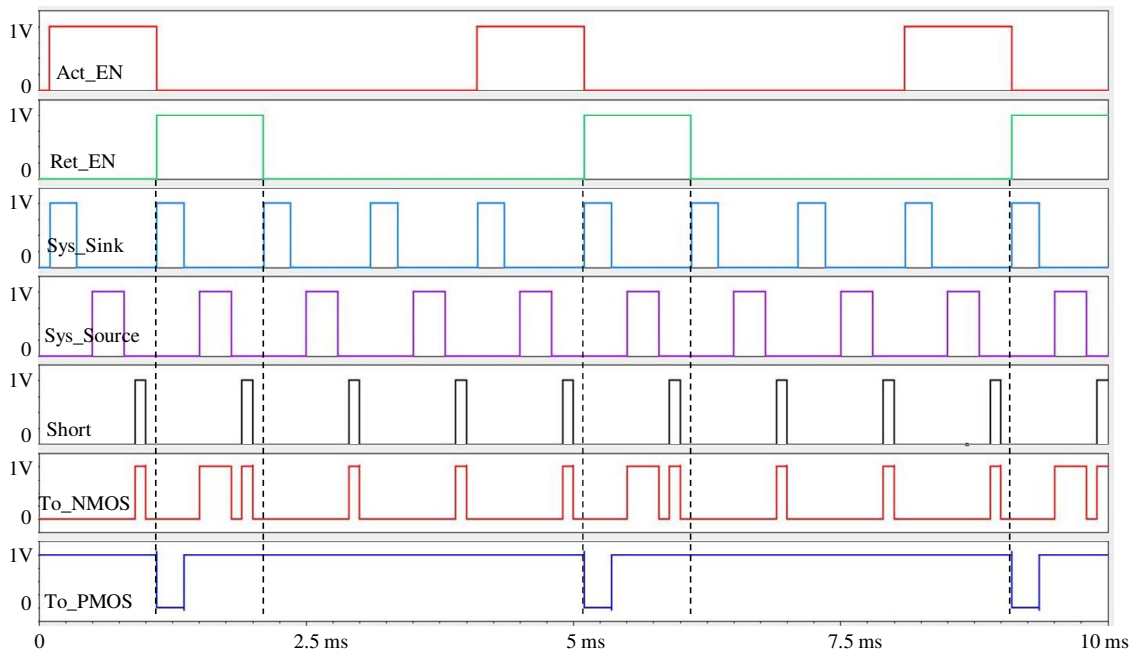
The control logic for the return path is shown in Figure 50 with the truth table included. The main purpose of the control logic is to connect its electrode to GND or VDD when the electrode is selected as return (Ret\_EN is high and Act\_EN is low). Electrode shorting after every stimulus pulse is also implemented by the control logic by shorting the electrode to GND when Short is high. When the electrode is selected as active (Act\_EN is high, regardless Ret\_EN), the control logic disables the two switches, the return path is kept disconnected from the electrode except when Short is high.

Figure 51 shows simulation result of the return path control logic. The control logic operates under its main purpose only when Ret\_EN is high. In all other cases, it connects the electrode to GND every time Short is high.



Short	Act_EN	Ret_EN	To_NMOS	To_PMOS
0	0	0	0	1
0	0	1	Sys_Source	/Sys_Sink
0	1	X	0	1
1	X	X	1	1

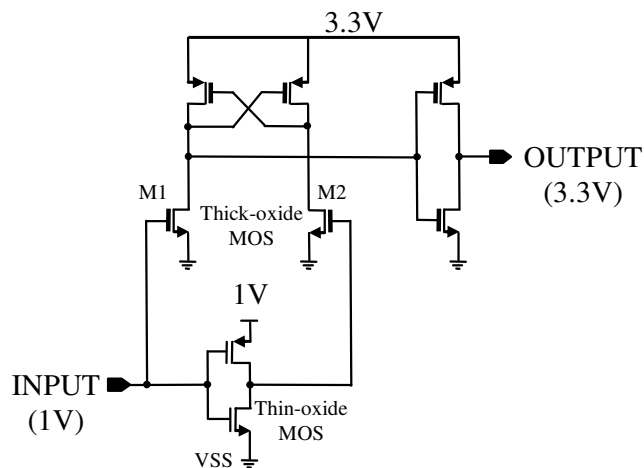
**Figure 50 Control logic for the return path at each electrode driver**



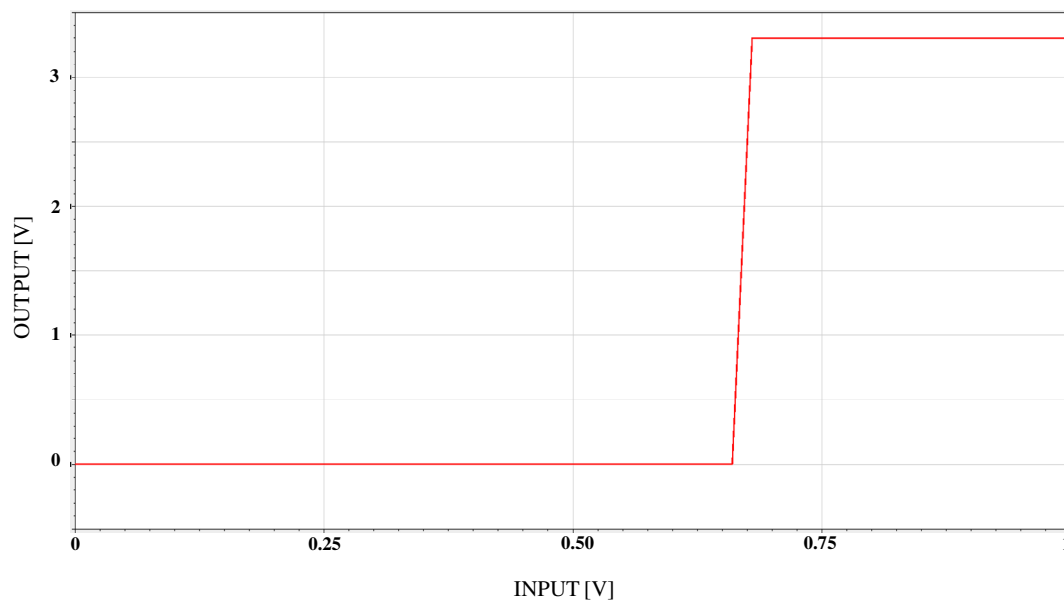
**Figure 51 Simulation result of the return path**

#### 4.4 Level shifter

A level shifter is needed to shift the signal from 1V at the digital part to 3.3V at the output stage of the electrode driver. Figure 52 shows the schematic of a conventional level shifter used in this design. When INPUT is at 1V, M2 turns off and M1 turns on, the OUTPUT is at 3.3V thanks to the output inverter. Similarly, when INPUT is at VSS, M2 turns on and M1 turn off, the OUTPUT is at VSS. Simulation result with DC input sweep is shown in Figure 53. The switching point of the level shifter is determined by the width/length ratio of the two thick oxide transistors M1 and M2, the bigger the ratio the smaller the switching point. However, bigger width/length ratio consumes more power. Therefore, a tradeoff has been made and the switching point of the designed level shifter is around 0.65V as shown in the simulation result.



**Figure 52 Schematic of the conventional level shifter used in this design**

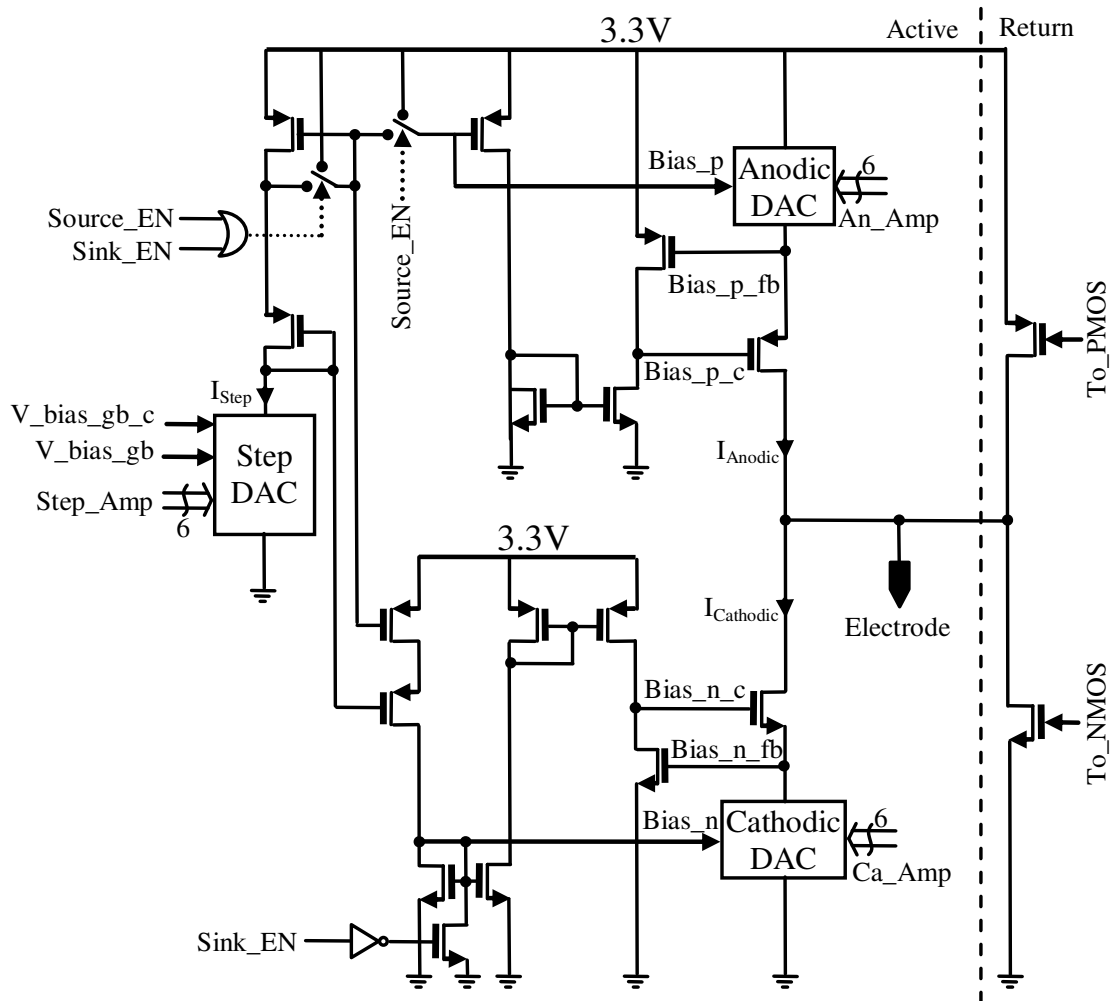


**Figure 53 Simulation result of the level shifter**

#### 4.5 Output stage

The analog output stage of each electrode driver consists of a threshold current generator and a stimulus current generator. Figure 54 shows schematic of the stimulus current generator. The schematic of the threshold current generator is similar to that of the stimulus current generator except the lack of the return path. In this figure, a 6-bit step DAC sets up the step current for the output DAC's. The global bias current of 80 nA is fed into the step DAC, which makes the step current vary from 0 nA to around 5  $\mu$ A in steps of 80 nA. The step current is then mirrored to form the anodic current and cathodic current by a 6-bit anodic DAC and a 6-bit cathodic DAC, respectively, via two regulated cascode current mirrors. The regulated cascode current mirrors are chosen as they provide high output impedance and low overdrive voltage [57, 59], which is ideal for current source. Digital controlling signal Act\_EN is used to activate the current generator. Two current mirror branches are controlled by the two signals Sink\_EN and Source\_EN so that when one branch is active, the other is powered down, so no power is wasted. The cathodic DAC's input (Ca\_amp) and anodic DAC's input (An\_amp) are separated, hence they can be different from each other. This feature together with the independent selection of cathodic phase and anodic phase durations allows the realization of asymmetrical stimulus waveform.





**Figure 54 Schematic of the electrode driver output stage**

The DAC's in the current generators are 6-bit binary-weighted DAC's, which are shown in Figure 55. The digital inputs control the switches connecting the bias voltages to the transistors' gates. Figure 55a shows schematic of the anodic DAC which generates anodic current, Figure 55b shows schematic of the cathodic DAC which generates cathodic current, and finally Figure 55c shows schematic of the step DAC which generates step current. The number of 6 bits was selected in order to relax the design of the DAC's and the global bias generator because the actual number of bits can be only 4 bits.

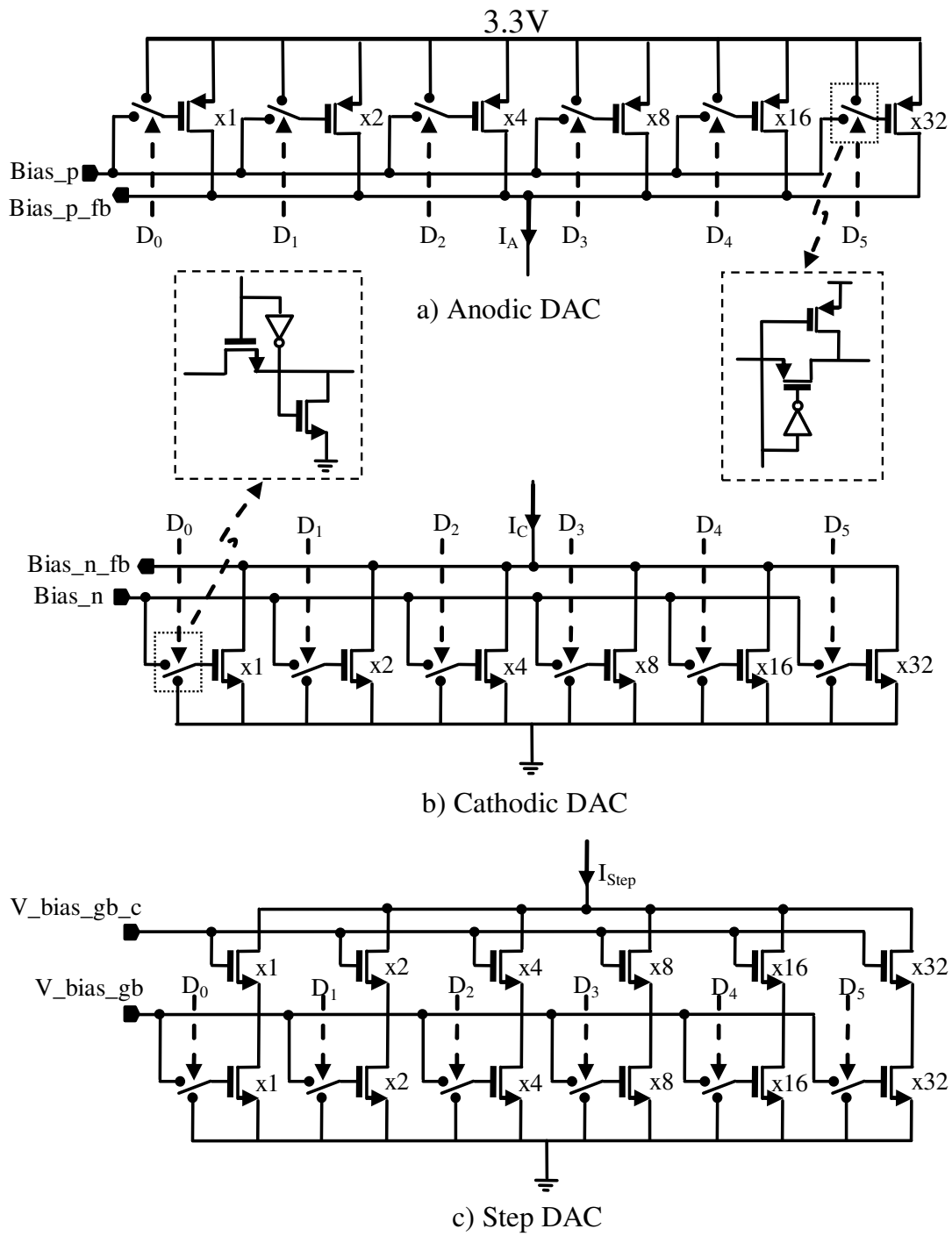


Figure 55 Schematic of the 6-bit binary weighted DAC's

## 4.6 Summary

A novel electrode driver architecture was proposed and implemented. Design complexity is distributed to every electrode driver to enhance flexibility and simplify routing issue. Layout of the electrode driver is shown in Figure 56, the total size of the electrode driver is  $200 \times 200 \mu\text{m}^2$ . Measurement results to evaluate electrode driver's performance will be presented in Chapter 6.

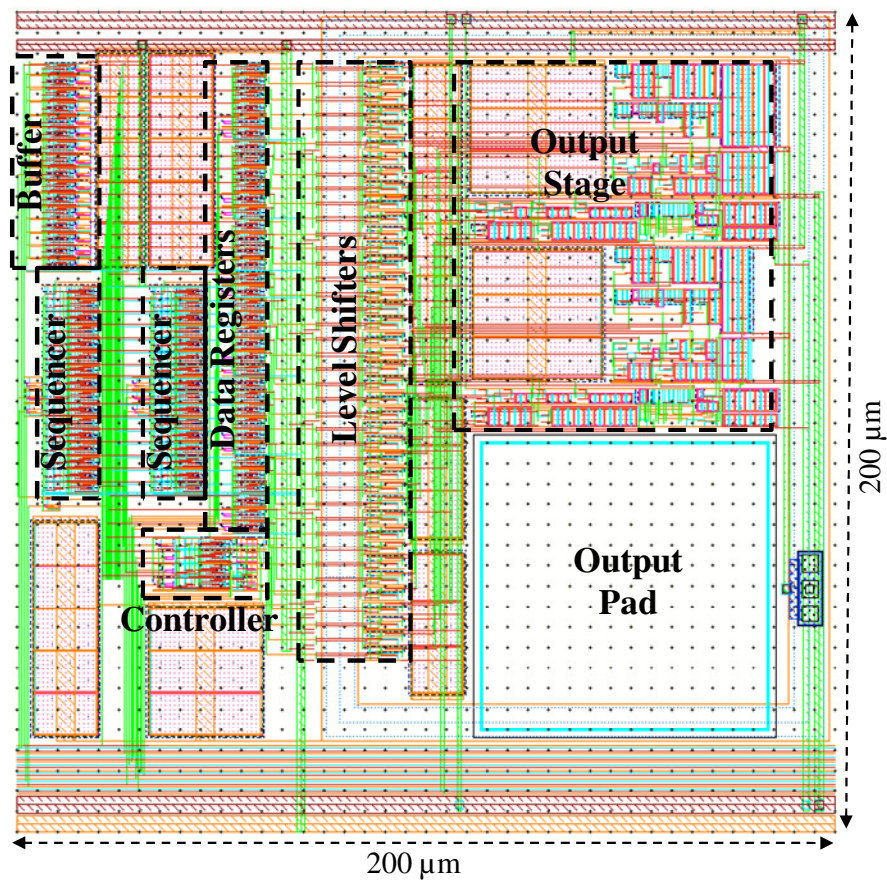


Figure 56 Layout of one electrode driver

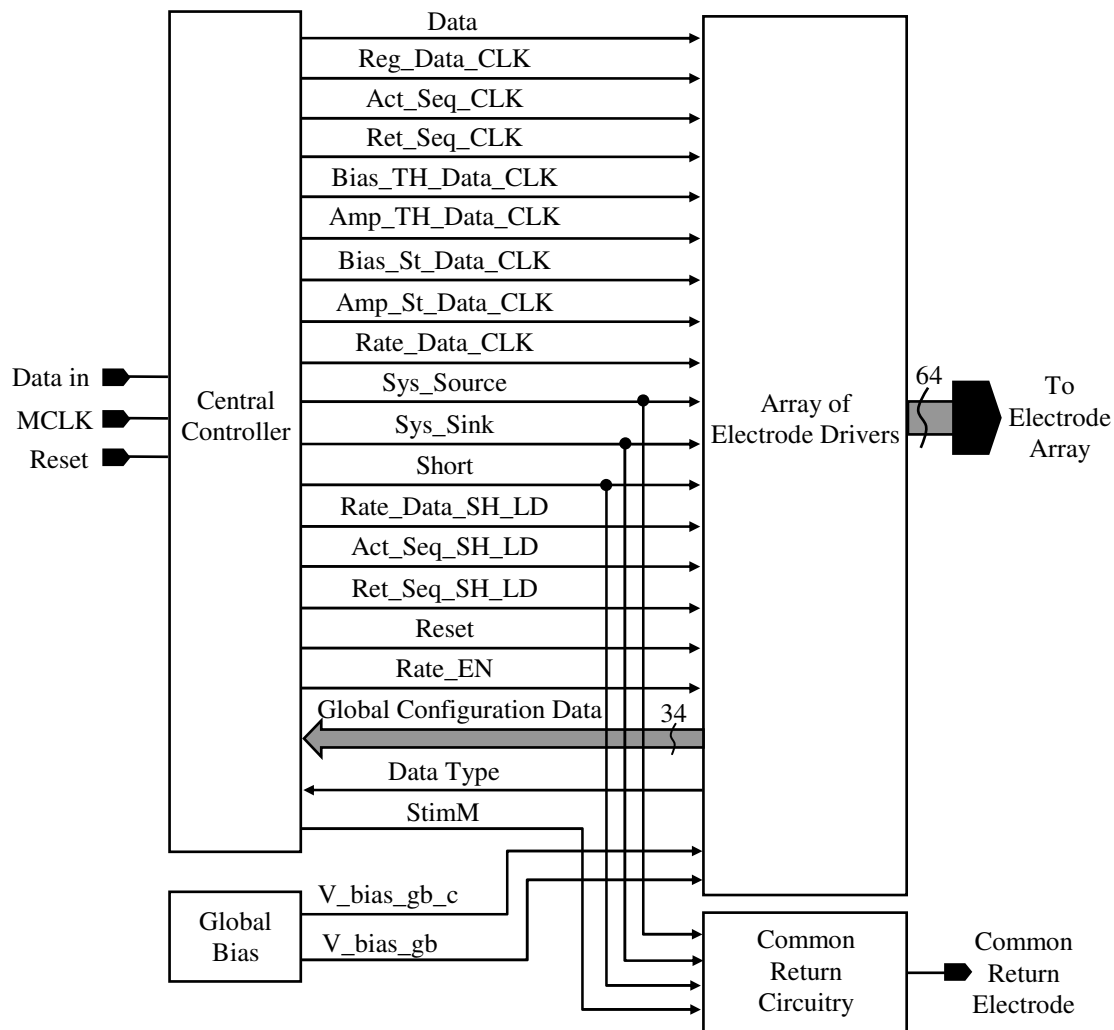


# Chapter 5    **Prototype 64-electrode stimulator**

Building a 1024-electrode stimulator chip is a very challenging task. Therefore, for the first chip fabrication, a prototype with 64-electrodes was designed, fabricated, and tested. This smaller-scaled chip design provides lots of benefits such as shorter design time, more space to put test circuits and easier debugging capability. This chapter introduces the design of this prototype stimulator. Baseband controller will be presented in detail, together with measurement results verifying the functionality.

## **5.1    Architecture**

The prototype stimulator includes a central digital controller, an array of 64 electrode drivers, a global bias circuit, and a common return circuitry as shown in Figure 57 . The global bias circuit and the common return circuitry have been presented in Chapter 3 while the electrode driver has been described in-depth in Chapter 4. The central digital controller receives and processes data (Data) from the receiver based on a master clock (MCLK) and a reset signal (Reset) to control the operation of the whole stimulator.



**Figure 57 Overall architecture of the prototype 64-electrode stimulator**

The operation of the stimulator can be divided into two stages: configuration and stimulation. In the configuration stage, all pre-defined stimulation parameters are set up by configuration data. Once the configuration stage is completed, the stimulator switches to the stimulation stage where real-time image data is received and converted into stimulus currents. In configuration stage, there are two kinds of configuration data: global and local. Global configuration data containing 34 bits is stored and processed by the central controller. Global configuration data defines timing parameters of the stimulus pulse (phase 1 duration, interphase gap, phase 2 duration, gap before shorting, shorting duration), time slice duration, unit clocks for each timing parameters of the stimulus pulse, leading pulse (cathodic first or anodic first), stimulation mode (bipolar

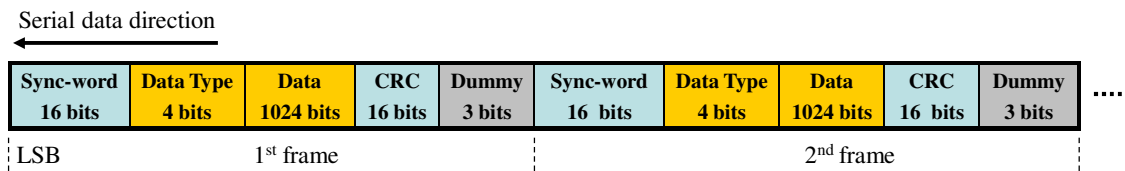
or monopolar), and brightness coding mode (amplitude coding or rate coding). Local configuration data is stored and processed by every electrode driver. Local configuration data at each electrode driver defines active sequence, return sequence (in bipolar stimulation), step current for threshold current, threshold current, and step current for stimulus current. At one electrode driver, different local configuration data types are stored in different data registers. However, they share only one 16-bit temporary buffer. Both global and local configuration data are pre-defined. This means they are transmitted only once at the beginning of the stimulator's operation, and can be re-transmitted occasionally when stimulation configuration needs to be changed. Real-time stimulation data can be stimulus current amplitude in amplitude coding mode, or stimulation rate in rate coding mode, or both current amplitude and stimulation rate in combined amplitude and rate coding mode. The combined amplitude and rate coding mode is an additional feature of the prototype 64-electrode stimulator, where data bandwidth is not a limitation due to much smaller number of electrodes (64 instead of 1024), and hence more data can be updated in real-time. In the ultimate 1024-electrode stimulator, however, if data bandwidth is enhanced somehow by a certain modulation technique, the combined amplitude and rate coding mode can also be included to allow more stimulation strategies.

In short, the prototype 64-electrode stimulator employs a central controller to control an array of 64 electrode drivers. All configuration data (global and local) is written at the beginning of the stimulator's operation and can be changed occasionally when needed. The data frame structure, details of global configuration data, and the design and implementation of the central controller will be presented in details in the following sections.

## **5.2 Data frame structure**

Data is serially transmitted to the central controller of the stimulator in frames. Figure 58 shows a data frame structure. Each data frame starts with a 16-bit frame synchronization pattern (sync-word) followed by 4-bit data type, then 1024-bit main data, and ends with a 16-bit CRC word. Main data has 1024 bits because each electrode driver needs maximum 16 bits at a time, and there are 64 electrode drivers ( $16 \times 64 =$

1024). Frames are separated by 3 dummy bits. Data stream is transmitted with the least significant bit (LSB) first except the CRC word, of which the most significant bit (MSB) arrives first.



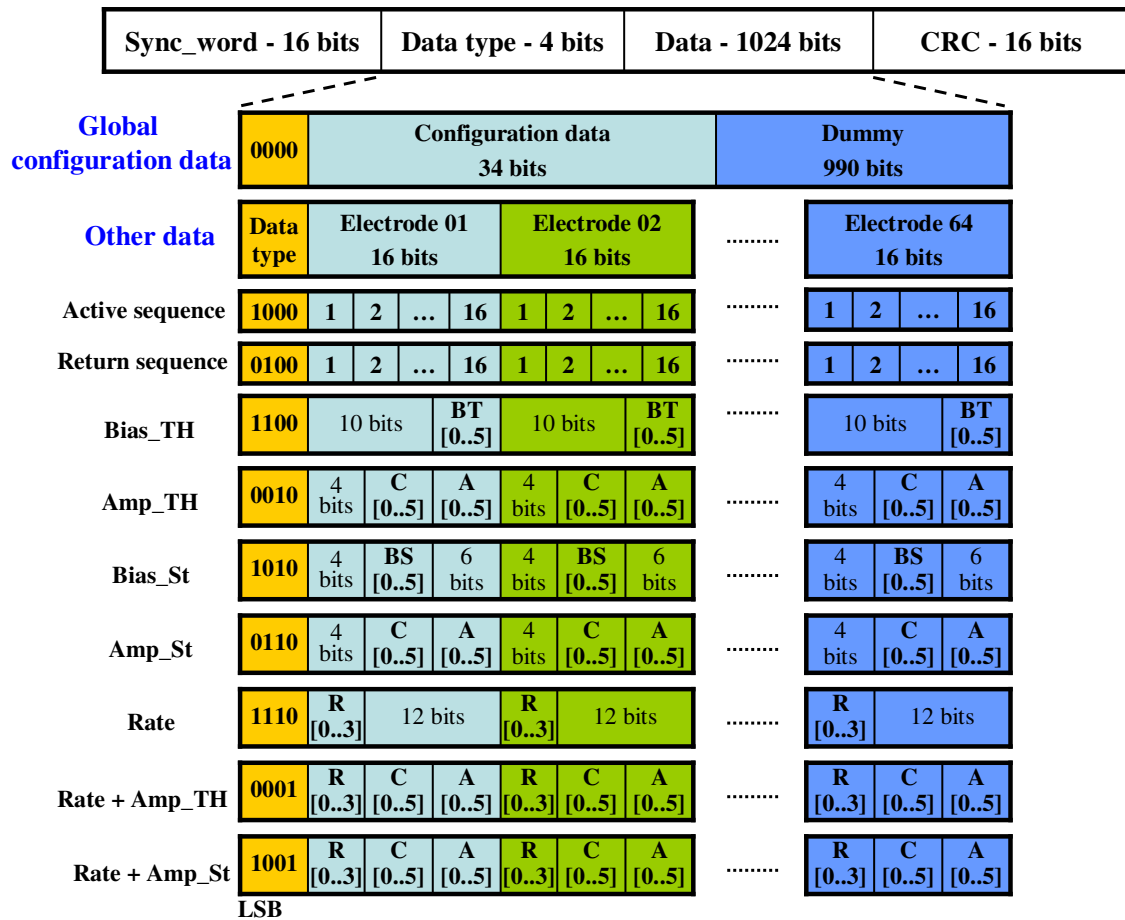
**Figure 58 Data frame structure**

The reason why 3 dummy bits were used can be explained as follows. With this data frame, useful data length is 1060 bits (sync-word + data type + data + CRC word). One more bit is needed for the controller to process data after a whole data frame has been received. Therefore, at least 1061 bits per data frame are needed. Data rate for this stimulator was selected to be 30 kbps, hence the frame time duration is  $1061 \times (1/30,000) = 35.367$  ms, or equivalently image data is updated in every 35.367 ms (approximately 28 image frames per second). In the rate coding mode, within one data update cycle, there are 128 time slices as shown in Figure 28 (16 time slices  $\times$  4 pulses  $\times$  2 refreshing times). Therefore, the time slice duration is  $35.367/128 = 276.3$   $\mu$ s. As this shortest time slice is generated by a divider from a master clock with frequency of 300 kHz as shown in Figure 36, the division ratio is  $300 \text{ kHz} \times 276.3 \mu\text{s} = 82.89$ , which must be rounded to 83 for the digital divider to work. With this division ratio, the shortest time slice is then  $1/(300 \text{ kHz}/83)$ . Therefore, the frame time duration becomes  $1/(300 \text{ kHz}/83) \times 128 = 35.413$  ms. New frame length becomes  $35.413 \text{ ms} \times 30 \text{ kHz} = 1062.4$  bits, which must be rounded to 1063, hence 3 dummy bits were added.

As mentioned above, there are configuration data and real-time stimulation data which need to be transmitted to the stimulator. Configuration data is then classified into 2 subsets: global and local. These different data types have different number of data bits. However, they share only one temporary buffer before being stored in their own data registers. Therefore, these different data types must be arranged in the data frame in a certain way in order to equally use the 16 output bits of the temporary buffers. The way data bits of different data types are arranged in data frames is illustrated in Figure 59. There are in total 10 data types:

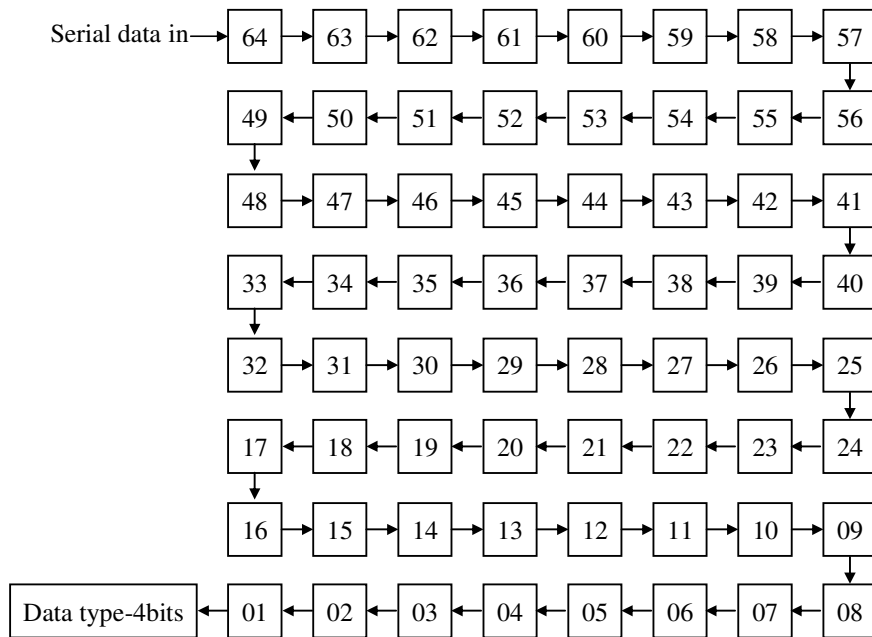


- Global configuration data: totally 34 bits, uses the first 34 bits of the main data, the remaining 990 bits are dummies (101010...).
- Active sequence: 16 bits per electrode driver, all allocated 16 bits are used.
- Return sequence: 16 bits per electrode driver, all allocated 16 bits are used.
- Step current for threshold current (Bias\_TH): 6 bits per electrode driver, uses the last 6 bits out of allocated 16 bits, the first 10 bits are dummies.
- Threshold amplitude (Amp\_TH): 12 bits per electrodes, used the last 12 bits out of allocated 16 bits, the first 4 bits are dummies.
- Step current for stimulus current (Bias\_St): 6 bits per electrodes, used the middle 6 bits out of allocated 16 bits, the first 4 bits and the last 6 bits are dummies.
- Stimulus amplitude (Amp\_St): 12 bits per electrodes, used the last 12 bits out of allocated 16 bits, the first 4 bits are dummies.
- Rate data (Rate): 4 bits per electrode, used the first 4 bits out of allocated 16 bits, the last 12 bits are dummies.
- Combined threshold amplitude and rate data (Rate + Amp\_TH): 16 bits per electrode driver, all allocated 16 bits are used.
- Combined stimulus amplitude and rate data (Rate + Amp\_St): 16 bits per electrode driver, all allocated 16 bits are used.



**Figure 59** Frame structure of different data types

After the sync-word has been detected, the data type and main data are stored in temporary buffers while CRC check is performed. As mentioned in Chapter 4, each electrode driver has only one 16-bit temporary data buffer, so 1024 bits of the main data are distributed equally to 64 electrode drivers. Four bits of the data type are stored in the central controller for the data type decoder to process. Figure 60 illustrates this data distribution. Data type is transmitted first, followed by data for electrode number 1 in the array, and so on to electrode number 64. Thirty four bits of the global configuration data are stored in the temporary buffers of electrode driver number 1, 2, and 3 (only 2 bits are used in the temporary buffer of electrode driver number 3), and then loaded in the 34-bit global configuration data register in the central controller if valid.

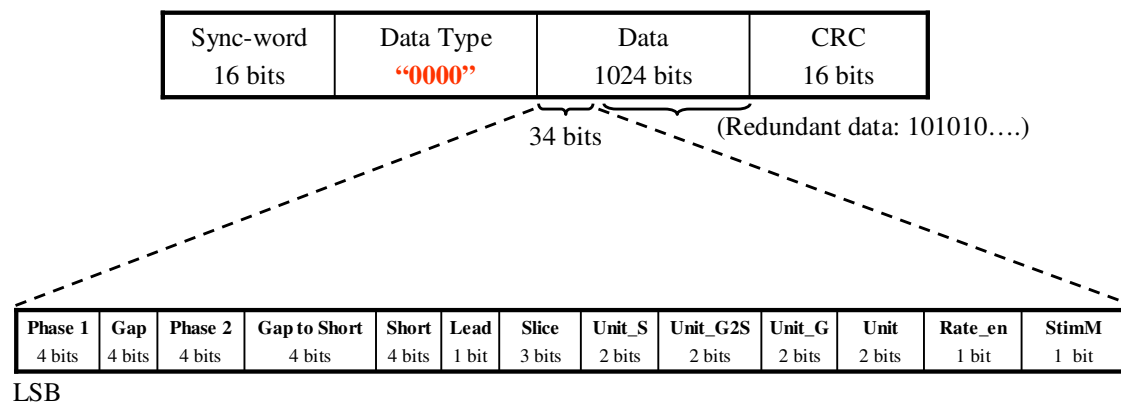


**Figure 60 Data distribution in the prototype stimulator**

In summary, data is serially transmitted to the stimulator frame by frame. The data type and main data of each data frame is distributed to a 4-bit temporary buffer in the central controller and 64 temporary buffers in 64 electrode drivers, respectively. Different data types have different number of bits and they are arranged in such a way that equally uses the output bits of the temporary buffers.

### 5.3 Global configuration data

Global configuration data consisting of 34 bits defines timing parameters of the stimulus pulse (phase 1 duration, interphase gap, phase 2 duration, gap before shorting, shorting duration), time slice duration, unit clocks for each timing parameters of the stimulus pulse, leading pulse (cathodic first or anodic first), stimulation mode (bipolar or monopolar), and brightness coding mode (amplitude coding or rate coding). The arrangement of those different parameters into a data frame is shown in Figure 61. Data type for global configuration data is '0000'. Global configuration data uses only 34 bits out of 1024 bits, therefore 990 bits are dummies. The dummies are a series of 1's and 0's to help maintaining data and clock alignment.



**Figure 61** Frame structure for the global configuration data

There are 13 different portions of the global configuration data frames, details of which are given in Table 4. Both stimulus phase (Phase 1) and return phase (Phase 2) of stimulus pulse use 4 bits to define their durations based on the same unit clock (Unit). The interphase gap (Gap) uses 4 bits to define its duration based on its own unit clock (Unit\_G). The gap before shorting (Gap to Short) and electrode shorting (Short) also use 4 bits to for their durations based on their own unit clocks (Gap to Short and Short, respectively).

Leading pulse of stimulus pulse is defined by one bit (Lead), which defines cathodic first if 0 and anodic first if 1. Eight different time slice durations from 277  $\mu$ s to 35.413 ms are programmed by 3 bits (CLK\_Slice). All unit clocks use 2 bits to select one out of 4 possible values of 10  $\mu$ s, 100  $\mu$ s, 500  $\mu$ s, and 1 ms to define any of the 5 components of the stimulus pulse. The brightness coding mode is defined by one bit (Rate\_EN), which selects amplitude coding if 0 and rate/both coding if 1. And finally, stimulation mode is also defined by one bit (StimM) with 0 for bipolar and 1 for monopolar. Table 5 lists time slice durations versus different values of the 3-bit CLK\_Slice.

**Table 4 Content of the global configuration data**

Type	# bits	Remarks
First pulse width (Phase 1)	4	Pulse duration = (Decimal value – 1) x Unit clock
Interphase gap (Gap)	4	
Second pulse width (Phase 2)	4	
Gap to short (Gap to Short)	4	
Short duration (Short)	4	
Leading pulse (Lead)	1	0: Cathodic first 1: Anodic first
CLK_slice (277µs, 553µs, 1.107ms, 2.213ms, 4.427ms, 8.853ms, 17.707ms, 35.413ms) (Slice)	3	Define time slice, the rate coding mode uses 277us time slice
CLK_unit_S (10µs, 100µs, 500µs, 1ms) (Unit_S)	2	Unit clock for the shorting pulse
CLK_unit_gap2S (10µs, 100µs, 500µs, 1ms) (Unit_G2S)	2	Unit clock for the gap between stimulus pulse and shorting pulse
CLK_unit_gap (10µs, 100µs, 500µs, 1ms) (Unit_Gap)	2	Unit clock for the interphase gap
CLK_unit (10µs, 100µs, 500µs, 1ms) (Unit)	2	Unit clock for the stimulation phase and return phase
Coding mode: Amp/Rate-Both (Rate_EN)	1	0: Amplitude coding 1: Rate/Both: if both, updating both amp and rate data
Stimulation mode: Bipolar/Monopolar (StimM)	1	0: Bipolar 1: Monopolar

**Table 5 Slice durations at different slice data inputs**

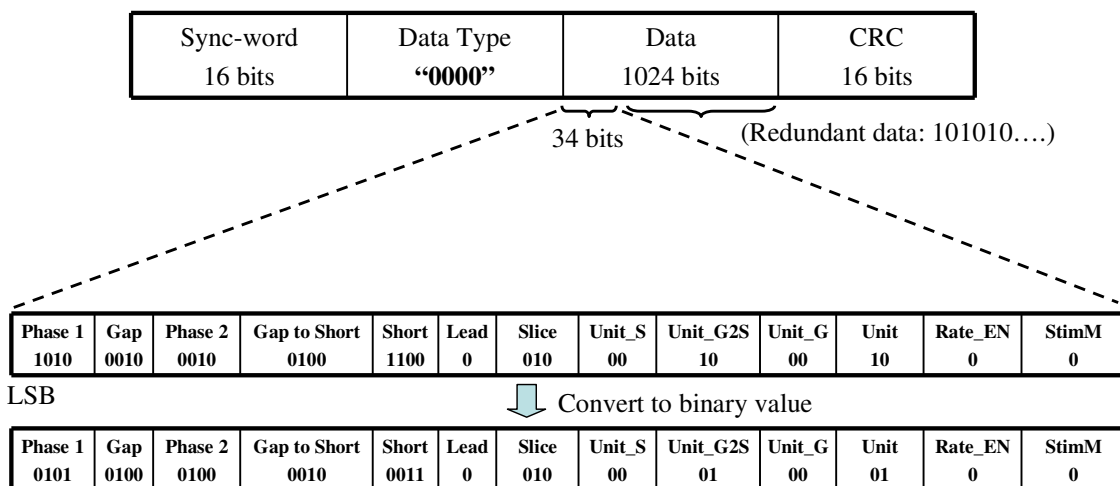
Binary value	Slice duration
000	277 µs
001	553 µs
010	1.107 ms
011	2.213 ms
100	4.427 ms
101	8.853 ms
110	17.707 ms
111	35.413 ms

All the unit clocks have 4 possible periods of 10 µs, 100 µs, 500 µs, and 1 ms defined by 2 bits. Table 6 lists the unit clock periods as a function of 2-bit data input.

**Table 6 Unit clock’s period at different unit clock data inputs**

CLK_Unit data	Unit clock’s period
00	10 $\mu$ s
01	100 $\mu$ s
10	500 $\mu$ s
11	1 ms

Figure 62 gives an example of a global configuration setup. Because the data is transmitted with the low significant bit (LSB) first, a conversion to binary values from the frame’s content is given to get an easier view of the data. From the frame’s content, the configuration can be expressed in Table 7.



**Figure 62 An example of global configuration data frame**

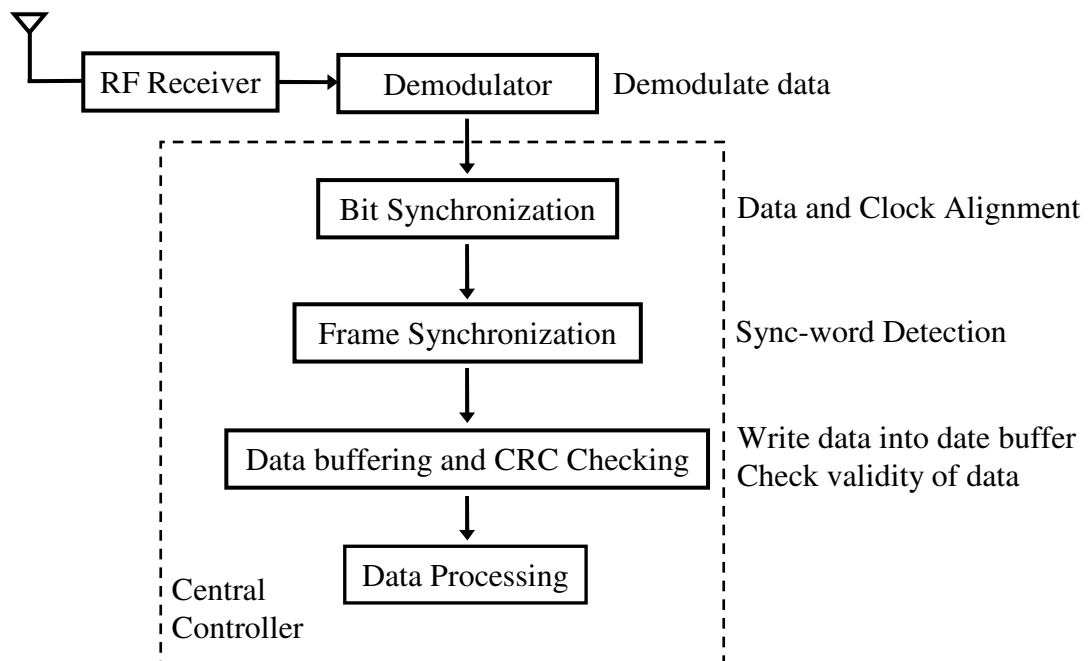
**Table 7 Example of a global configuration**

Data	Configuration
StimM = 0	Bipolar stimulation
Rate_EN = 0	Amplitude coding
Unit = 01	Unit clock for stimulation phase and return phase is 100 $\mu$ s
Unit_G = 00	Unit clock for the interphase gap is 10 $\mu$ s
Unit_G2S = 01	Unit clock for the gap to short is 100 $\mu$ s
Unit_S = 00	Unit clock for the short is 10 $\mu$ s
Slice = 010	Time slice duration is 1.107 ms
Lead = 0	Cathodic first
Short = 0011	Short duration = $(3-1) \times 10 \mu\text{s} = 20 \mu\text{s}$
Gap to Short = 0010	Gap to short duration = $(2-1) \times 100 \mu\text{s} = 100 \mu\text{s}$
Phase 2 = 0100	Phase 2 (Anodic) duration = $(4-1) \times 100 \mu\text{s} = 300 \mu\text{s}$
Gap = 0100	Interphase gap = $(4-1) \times 10 \mu\text{s} = 30 \mu\text{s}$
Phase 1 = 0101	Phase 1 (Cathodic) = $(5-1) \times 100 \mu\text{s} = 400 \mu\text{s}$

In summary, global configuration data mainly defines timing parameters for stimulus pulse, as well as stimulation mode and brightness coding mode.

#### 5.4 Central controller

The main function of the central controller is to process data received from the receiver and control the stimulation activity at the electrode driver array. Figure 63 illustrates the data flow controlled by the central controller. Raw data from the demodulator is first synchronized with the master clock through the bit synchronization stage. The synchronized data then goes through the frame synchronization stage to detect each data frame. Once a frame is detected, data in the frame will be stored in temporary buffers as well as be CRC checked for errors. The data will be processed further if no errors are detected.



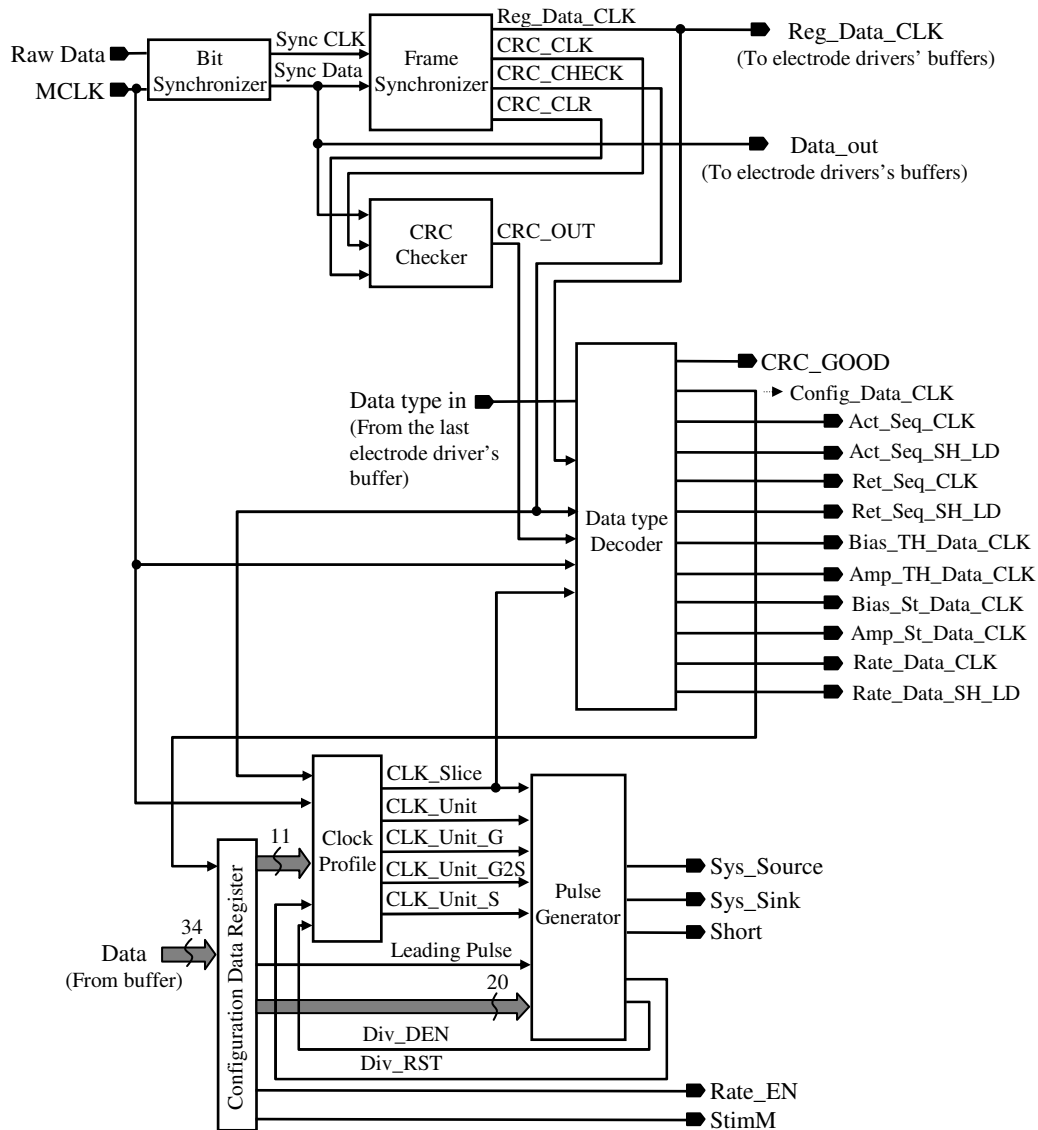
**Figure 63 Data flow of the central controller**

Figure 64 shows block diagram of the central controller. The bit synchronizer is used for bit synchronization to align received data and the master clock of the stimulator. The frame synchronizer is used to detect the beginning of each incoming data frame. The CRC checker is used to perform CRC calculation on the incoming data stream to verify the validation of the data. The data type decoder decodes different data types and allocates data to their corresponding registers. A 34-bit data register stores global configuration data. The clock profile and the stimulus pulse generator are used to provide global timing information for the stimulus pulse.

The operation of the central controller can be described as the following. The data stream first comes to the bit synchronizer to make it aligned with the master clock. The aligned data stream is then fed into the frame synchronizer until the frame synchronization pattern is detected. Once the synchronization pattern is detected, the next incoming bits are fed into both the data buffers in the electrode drivers and the CRC checker for CRC calculation. The control logic checks the CRC output after a full data frame has been shifted in. If the received data frame is error free, the data will be stored in the corresponding data registers controlled by the data type decoder based on the received data type. If the received data is global configuration data, it will be stored in the configuration data register, to function as inputs to the clock profile and the



stimulus pulse generator. If the received data is other data (local configuration data or real-time image data), the data type decoder will control to store it in corresponding data registers in the electrode drivers. In case the received data is not valid, if it is configuration data (either global or local), the stimulator will request the transmitter to re-transmit the frame. If it is real-time image data, the invalid received data will be ignored, and the previously valid image data is used for stimulation while waiting for new image data to arrive.



**Figure 64 Block diagram of the central controller**

In summary, the central controller is the heart of the stimulator, which controls all of the operations of the stimulation including data receiving and processing as well as

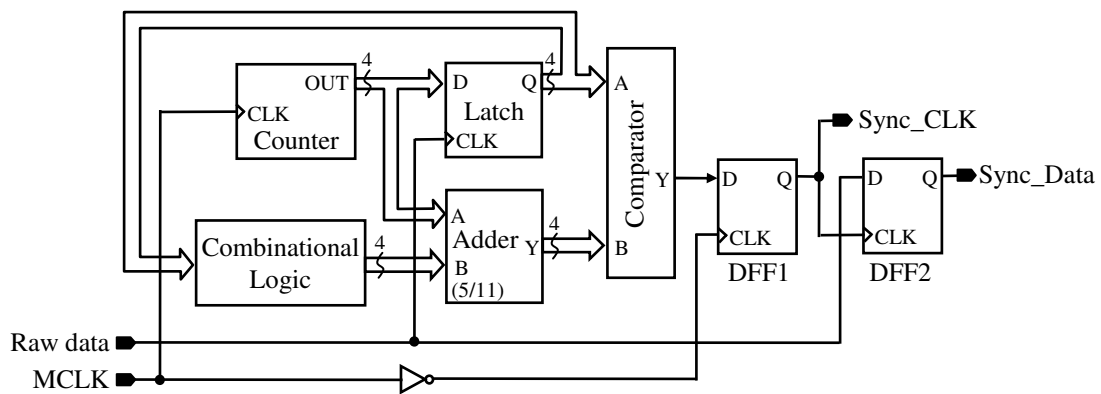
stimulating activities. Except the clock profile and the stimulus pulse generator which have been described in Chapter 3, other blocks will be presented in details in the following sections.

## 5.5 Bit synchronizer

The incoming data stream and the chip system clock are not synchronized, hence the data stream needs to be aligned with the system clock so that the controller can sample data correctly. A bit synchronizer is designed to achieve this. This is a modification to another bit synchronizer reported in [22]. The bit synchronizer shown in Figure 65 consists of a counting-to-10 counter, a 4-bit latch, a 4-bit adder, a comparator, some combinational logic, and 2 DFFs. Input master clock's frequency is 300 kHz, ten times higher than the raw data rate, or equivalently within one data bit duration, there are 10 cycles of the master clock. That is the reason why the counter in this design only counts to 10. The idea behind this architecture is that, every time raw data goes high, the counter clocked by master clock will count to 5 and then raw data is sampled. By doing this, raw data is always sampled at the middle of its bit after every rising edge. Once sampled at the middle of a bit after a rising edge, in every ten master clock cycles raw data is sampled again should no rising edge occurs, this ensures that raw data is always sampled at the middle of every bit. The operation of the circuit is described next.

The counter is kept counting from 0 to 9 all the time by the master clock. At the time when the raw data goes high ( $t = T_0$ ), the counter output  $C(T_0)$  is latched by the 4-bit latch and the counter keeps counting. The counter output is added with 5 or 11 by the 4-bit adder depending on the value of  $C(T_0)$ . The adder output is compared with the latched counter output  $C(T_0)$  by the 2-input 4-bit comparator. If the comparator's 2 inputs are the same, the comparator output goes high for one master clock cycle, which then causes the output of DFF1 to go high for one master clock cycle. The DFF1 output is used as new data clock and this samples the raw data to get the aligned data. Therefore, to sample the raw data at the middle of its bit after every rising edge, the two inputs of the comparator are expected to be the same when the counter counts 5 more cycles after being latched. This is done by the adder with the help of the combinational logic. Indeed, when the counter counts 5 more cycles after being latched, its output is

$C(T_5) = C(T_0) + 5$ , which is input A of the adder. Input B of the adder is either 5 or 11 depending on  $C(T_0)$ . Whether it is 5 or 11,  $C(T_5) + (5 \text{ or } 11)$  must be equal to  $C(T_0)$  in order for the comparator output to go high. If  $C(T_0)$  is from 0 to 4,  $C(T_5)$  will be from 5 to 9, hence 11 is selected so that  $C(T_5) + 11$  becomes from 0 to 4, equal to  $C(T_0)$ . For example,  $C(T_0)$  is 2,  $C(T_5)$  is then 7, hence  $C(T_5) + 11$  becomes 18 or 2 (modulo 16), which is equal to  $C(T_0)$ . If  $C(T_0)$  is from 5 to 9,  $C(T_5)$  will be from 0 to 4 (counter counts to 9 and then back to 0), hence 5 is selected so that  $C(T_5) + 5$  is from 5 to 9, equal to  $C(T_0)$ . For example,  $C(T_0)$  is 6,  $C(T_5)$  is then 1 (counter counts to 9 and then back to 0), hence  $C(T_5) + 5$  is 6, equal to  $C(T_0)$ . Summary of the adder's operation is given in Table 8.

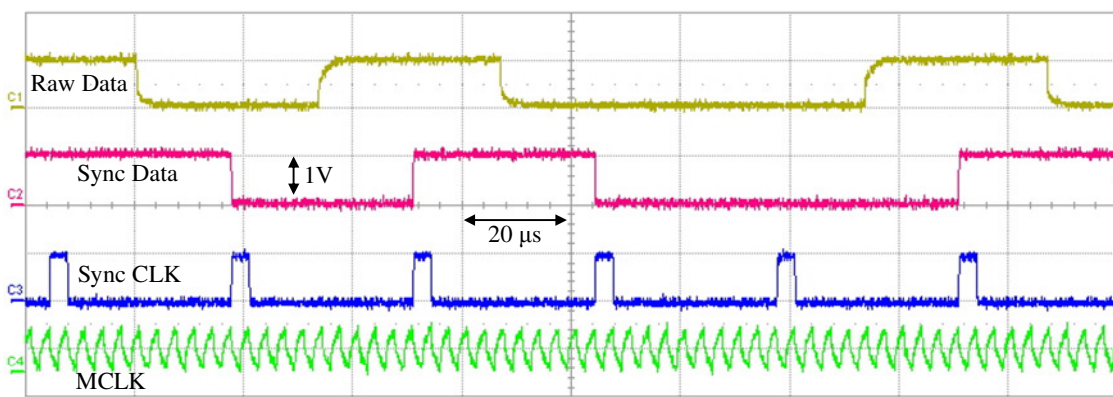


**Figure 65 Schematic of the bit synchronizer**

**Table 8 Summary of the bit synchronizer's adder**

$C(T_0)$	$C(T_5)$	Input B	Adder output: $C(T_5) + \text{Input B (modulo 16)}$
0	5	11	0
1	6		1
2	7		2
3	8		3
4	9		4
5	0	5	5
6	1		6
7	2		7
8	3		8
9	4		9

Figure 66 shows measurement result of the bit synchronizer. The master clock (MCLK) is 300 kHz and the raw data rate is 30 kHz. It can be seen that after being synchronized, the data and the clock are well aligned. The raw data is sampled at the middle of each bit, which minimizes the sampling error. The 'Sync CLK' has a duty cycle of 10%, which is one cycle of the master clock. The distortion of the raw data and the master clock is due to the measurement setup, which does not affect the bit synchronizer's performance.



**Figure 66 Measurement result of the bit synchronizer**

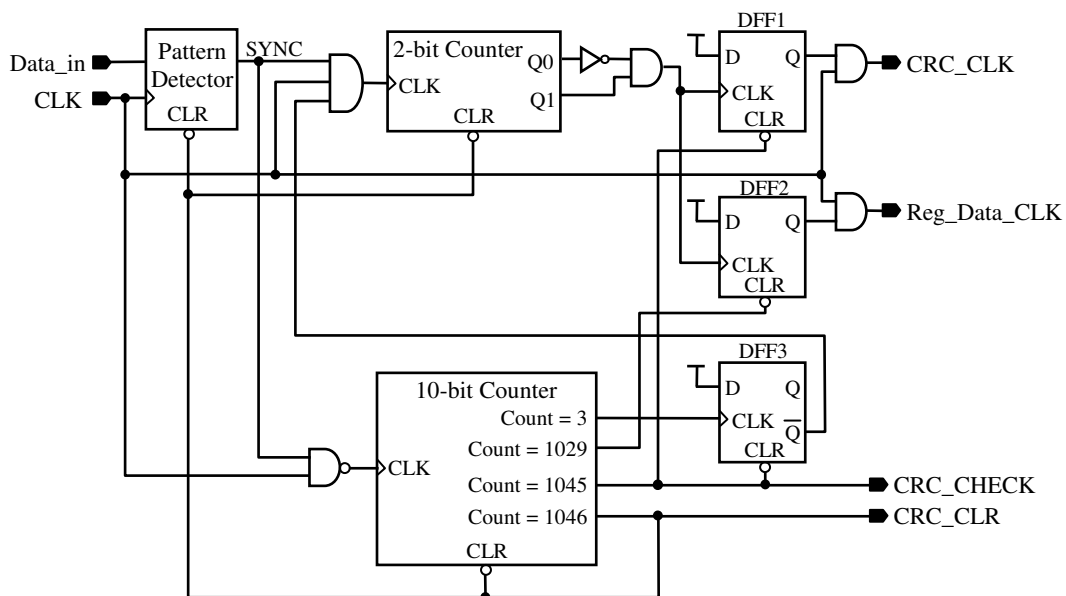
In short, the bit synchronizer was implemented to make sure received data is always aligned with the system clock of the stimulator.

## 5.6 Frame synchronizer

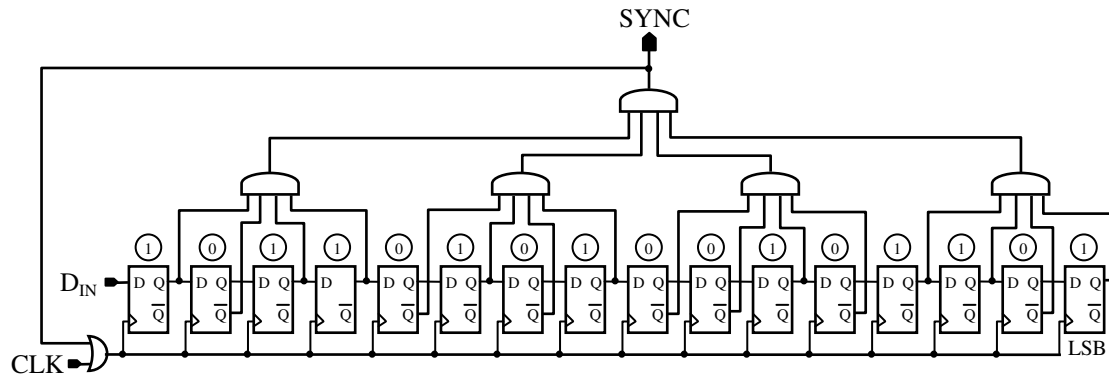
The frame synchronizer coordinates the processing of every received data frame. Figure 67 shows schematic of the frame synchronizer, which consists of a pattern detector, 2 counters, 3 DFFs, and some logic gates. Figure 68 shows the schematic of the pattern detector, which is a 16-bit shift register with some combinational logic at the output. The synchronization pattern was selected to be 1011010010101101 (MSB). The incoming data stream is fed into the shift register, when the synchronization pattern is detected, the output SYNC goes high. The SYNC is fed back to disable the clock signal so that no more synchronization pattern is detected until the whole data frame has been

received and CRC calculation has been finished. The output SYNC will then be reset to allow new data frame to come in.

A data frames starts with a pre-defined 16-bit pattern indicating the beginning of the incoming frame. The data stream keeps feeding the pattern detector until the pre-defined pattern is detected. Once the synchronization pattern has been detected, the following incoming bits are treated as data bits, so they are stored in the data buffers. CRC calculation is also performed to check the validity of the received data. The pattern detector is disabled until CRC calculation has been finished. The frame synchronizer controls all of these operations.

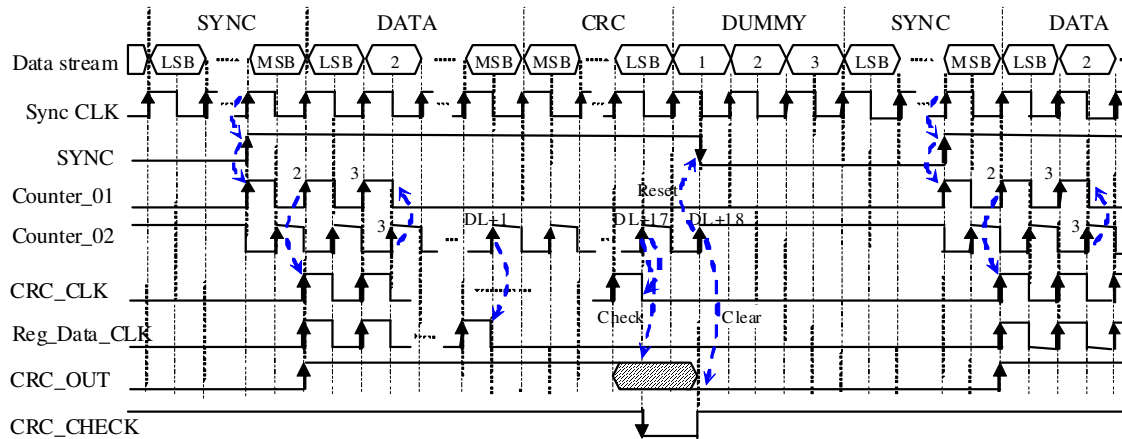


**Figure 67 Schematic of the frame synchronizer**



**Figure 68 Schematic of the pattern detector**

Figure 69 shows a waveform illustration of the frame synchronizer's operation. When the sync-word has been detected by the pattern detector, the SYNC goes high, which then triggers the two counters to start counting. The clocks for the two counters are non-overlapped to get a half bit delay between each other. When the 2-bit counter counts to 2 (at the time the first bit of the data type comes), data storing and CRC calculation are initiated by activating the Reg\_Data\_CLK and the CRC\_CLK, respectively. When the 10-bit counter counts to 3, the clock to the 2-bit counter is blocked, and the 2-bit counter stops counting to save power. When the 10-bit counter counts to 1029 (data length  $DL + 1$ ), the last bit of the main data has been stored, hence the data buffer clock Reg\_Data\_CLK is blocked. The 10-bit counter keeps counting until it reaches 1045 ( $DL + 17$ ) when the last bit of the CRC word has been shifted in, and CRC calculation has been finished. Therefore, the clock to the CRC checker CRC\_CLK is blocked and the CRC output is ready for checking. When the 10-bit counter counts to 1046 ( $DL + 18$ ), the CRC output is clear for being ready for next calculation, and the pattern detector output SYNC is reset to allow a new data frame to be shifted in. The two counters are also reset at this time to get ready for a new data frame.

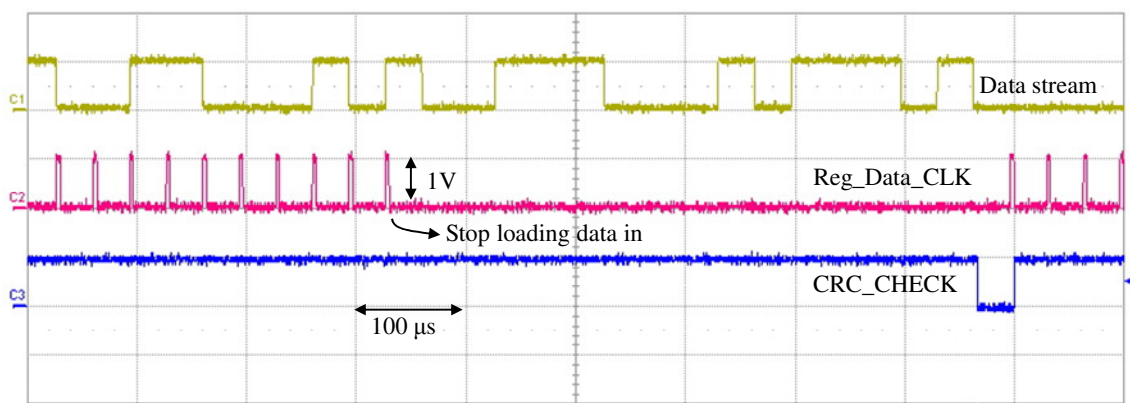


**Figure 69** Waveform illustration of the frame synchronizer's operation, DL is the data length including 4 bits of data type and 1024 bits of electrode data, hence  $DL = 1028$

The frame synchronizer works well in the way described above. However, what happens if something goes wrong? If the pattern detector does not detect the sync-word, 2 scenarios can happen. The first scenario is that among the data bits following the missed sync-word, there is one 16-bit pattern that is identical to the pre-defined sync-word. If the pattern detector detects this pattern and treats it as a normal sync-word, the next 1028 bits will be stored as data and CRC checking is also performed. However, it is likely that the CRC checker will verify that the data is not valid, and hence the stored data is ignored. In this case, at least two data frames are missed. One is the frame with the missed sync-word, the other is the next frame which is corrupted due to the inappropriate sync-word being detected in the middle of the missed frame. The second scenario is that there is no 16-bit pattern as identical as the sync-word among the bits following the missed sync-word, then only the data frame with the missed sync-word is missed. The missing of one frame does not affect the reception of the next frame.

Figure 70 shows measurement result of the frame synchronizer. Data stream, clock for data buffer (Reg\_Data\_CLK), and CRC\_CHECK signal are displayed. It can be seen that the Reg\_Data\_CLK is blocked at 16 bits before the CRC output is checked, which matches with the waveform description in Figure 69. The only difference between the measurement result and the waveform description is that the Reg\_Data\_CLK is activated right after the CRC\_CHECK in the measurement instead of right after the sync-word being detected in the waveform description. This is due to the reset action of

the frame synchronizer. Indeed, let's look back to schematic of the frame synchronizer in Figure 67. After the CRC calculation is finished, the 2-bit counter's outputs are reset from '11' to '00' creating an impulse which clocks DFF1 and DFF2 to make their outputs go high. This allows the CLK to pass through the two AND gates and become CRC\_CLK and Reg\_Data\_CLK. Nevertheless, the early activation of CRC\_CLK and Reg\_Data\_CLK does not affect at all to the frame synchronizer's operation because only the time when the storing data activity is stopped and the CRC checker output is checked matters.



**Figure 70 Measurement result of the frame synchronizer**

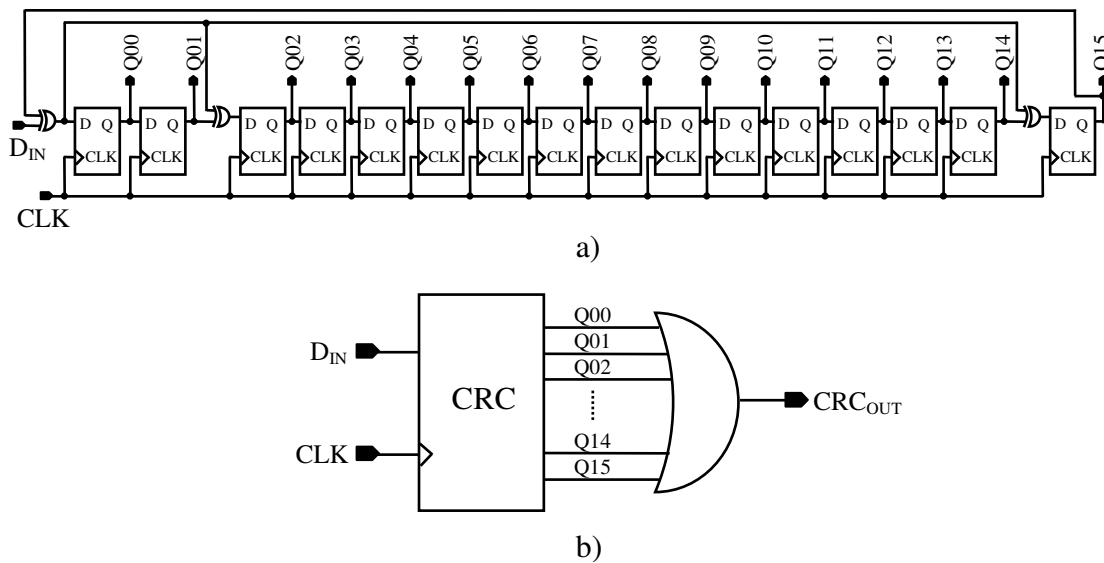
In summary, the frame synchronizer was implemented to coordinate the reception of data frames. Measurement results show good performance.

## 5.7 CRC checker and data type decoder

A 16-bit Cyclic Redundancy Check (CRC) pattern is calculated and attached to the end of each frame at the transmitter. CRC-16 was selected as it is enough to detect most of the possible errors [60]. The CRC-16 polynomial used is the disk controller generator polynomial, which is defined by:  $x^{16} + x^{15} + x^2 + 1$ . At the receiver, a 16-bit CRC calculator is used to calculate the incoming data stream, and then the calculated CRC pattern is compared with the received CRC to decide whether the frame is error-free or not.



Figure 71 shows the schematic of the CRC checker used in this stimulator. The CRC calculator is implemented by 16 DFFs and 3 XOR gates shown in Figure 71a to realize the polynomial above. When the calculated CRC pattern matches the attached CRC pattern, all the outputs of these DFFs become zeros. Therefore, by putting these outputs through an OR gate as in Figure 71b, one single output of the CRC checker can be accessed. If the output is low, the received data is valid, and vice versa.

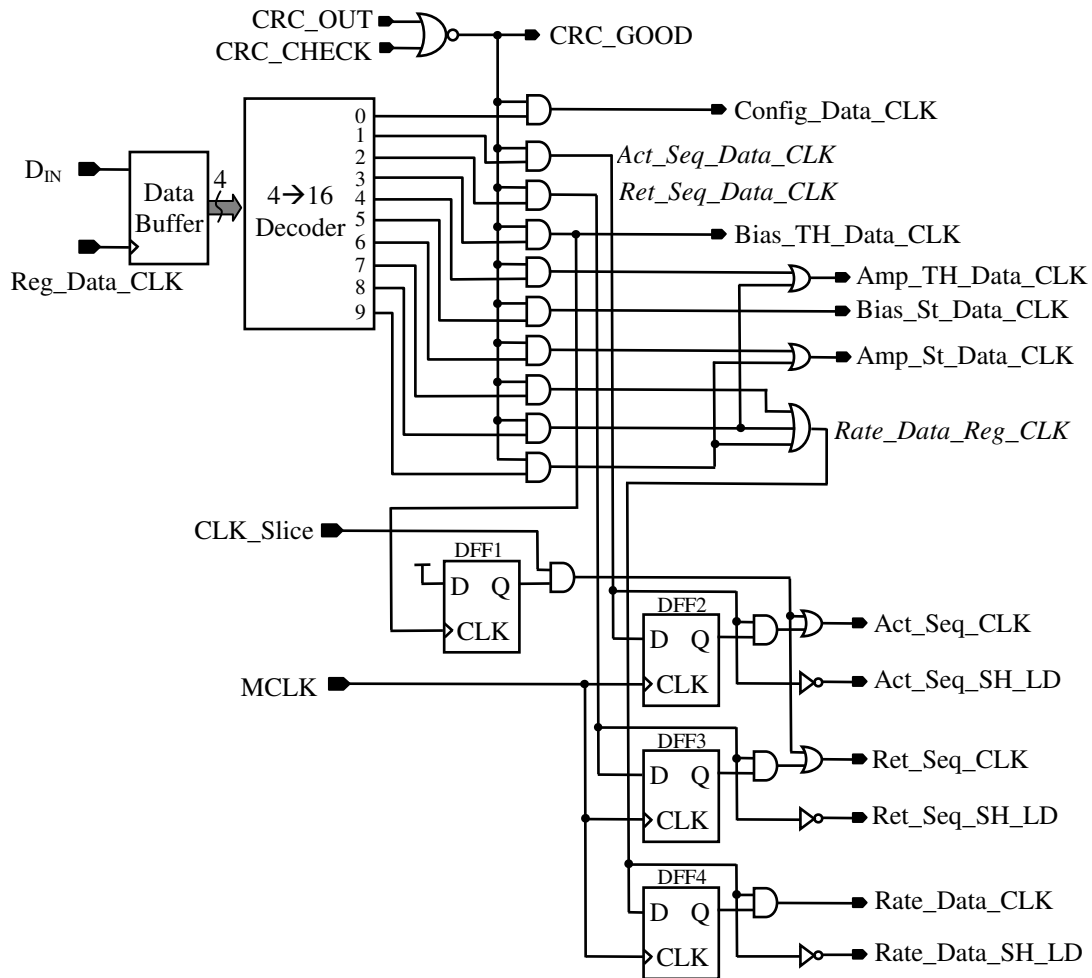


**Figure 71 Schematic of the CRC checker: a) CRC calculator; b) with combined output**

There are 10 different types of data the central controller can receive, and no matter what type the received data is, it is always stored in only one temporary buffer at the electrode driver to wait for CRC checking and data type classification before being stored in its appropriate data buffer. The data type decoder whose schematic is shown in Figure 72 was implemented to allocate received data to corresponding data registers based on data type. In the schematic, a 4-bit register plays role of a temporary buffer to store data type. Four output bits of the buffer are fed into a 4-to-16 decoder (with 10 outputs only, corresponding to 10 types of data). Once the data type has been loaded in the buffer, one out of 10 outputs of the decoder will become high while others are low. When the CRC checking is finished, CRC calculation's result will determine whether or not to load data into their corresponding registers from the temporary buffers. If CRC calculation's result is correct, CRC\_GOOD goes high, depending on the data type, one

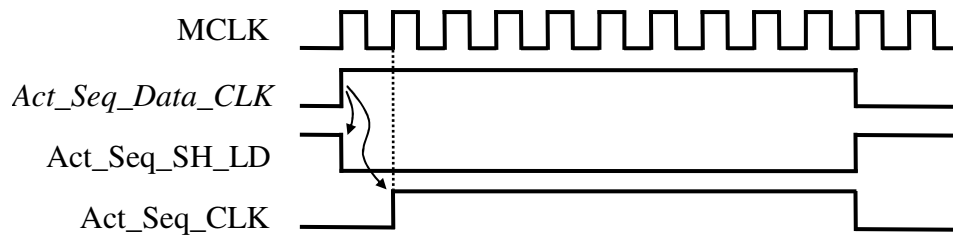
of the clocks to the data registers goes high correspondingly, which loads data into the registers. If CRC calculation's result is incorrect, CRC\_GOOD stays low, no matter what data type is, the data in the buffers is ignored. For example, the data type is '0000', if CRC\_GOOD goes high after the CRC calculation is done, Config\_Data\_CLK will go high to load global configuration into the global configuration data register in the central controller.

A normal data transmission starts with the global configuration data (Config\_Data\_CLK), followed by the active sequence data (Act\_Seq\_CLK), the return sequence data (Ret\_Seq\_CLK), and then the data for threshold current step (Bias\_TH\_Data\_CLK). The threshold current amplitude data (Amp\_TH\_Data\_CLK) follows after its current step data, and then is followed by the data for stimulus current step (Bias\_St\_Data\_CLK). Afterward the stimulus current amplitude data (Amp\_St\_Data\_CLK) is received. Depending on the stimulation mode, if it is the amplitude coding, the new stimulus current amplitude data will be transmitted. If it is the rate coding, the rate data (Rate\_Data\_CLK) will be transmitted. In case of combined amplitude and rate coding, both stimulus current amplitude (or threshold current amplitude) and rate data are transmitted. Once the data for threshold current step is correctly received, the active sequencer and return sequencer start to circulate. This is done with the help of DFF1. When Bias\_TH\_Data\_CLK goes high, it triggers DFF1, which makes CLK\_Slice passed through to Act\_Seq\_CLK and Ret\_Seq\_CLK, which are the clocks circulating the active and return sequencers, respectively.



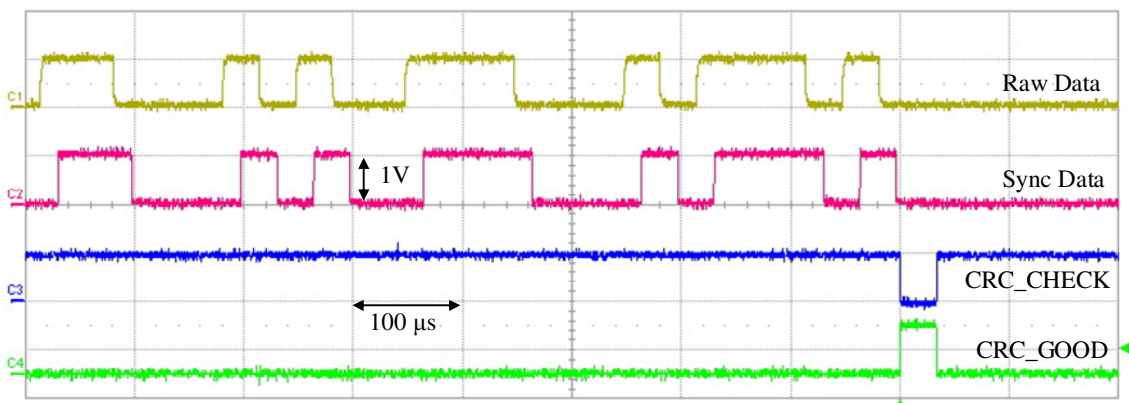
**Figure 72 Schematic of the data type decoder**

The active sequencer, the return sequencer, and the rate data sequencer have to load their data into synchronous input loading DFFs in Figure 47. The data is loaded in only when the SH\_LD signal is low at the rising edge of the clock. Therefore, for each of these data types, shift/load signal and data loading clock must be made based on the data type decoder outputs with the help of DFFs and logic gates as shown in the lower part of Figure 72. Figure 73 shows an illustration of generating shift/load signal and data loading clock for the active sequencer. When *Act\_Seq\_Data\_CLK* goes high, it is inverted to get *Act\_Seq\_SH\_LD*. It is also delayed by one master clock cycle to get *Act\_Seq\_CLK*. These two new signals are used to load data into the active sequencer.



**Figure 73** Waveform illustration of generating shift/load signal and loading clock for active sequencer

Measurement result of the CRC checker combined with the data type decoder is shown in Figure 74. It can be seen that CRC\_GOOD goes high when CRC\_CHECK goes low, which means a full frame has been correctly received. To verify the performance of the data type decoder, more results with different data types loaded will be shown in Chapter 6.

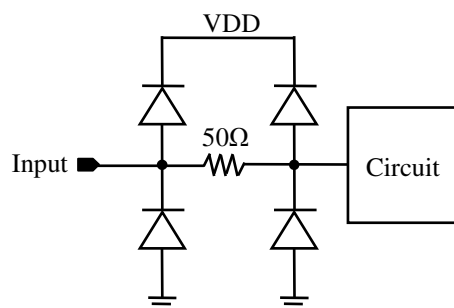


**Figure 74** Measurement result of the CRC checker combined with the data type decoder

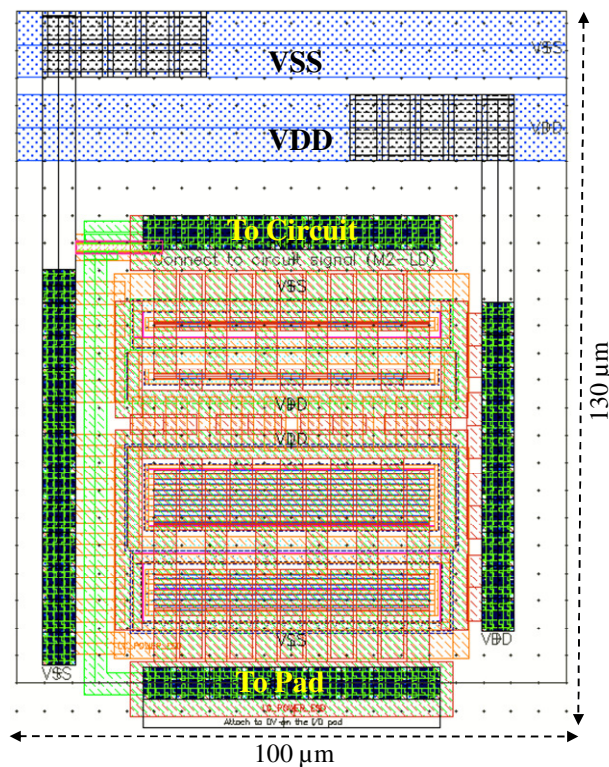
In summary, a 16-bit CRC checker was implemented to check the validation of received data in the stimulator. Measurement results showed good performance. A data type decoder was implemented to help the central controller store different data types into appropriate data registers.

## 5.8 ESD protection

The implantable device makes contact to human body (through the retina tissues) via 1024 electrodes and one common return plate. In addition, contact with human body and equipment during device assembly and surgery is unavoidable. Therefore, electric static discharge (ESD) protection is very important to protect the device from being damaged. In this prototype stimulator, all input signals and output signals (both 1V and 3.3V) are ESD protected by double diode ESD protection circuits as shown in Figure 75. Layout of this ESD protection circuit is shown in Figure 76. The area of the ESD protection circuit is  $100 \times 130 \mu\text{m}^2$ , which is pretty large as the area of each electrode driver in the high density stimulator will be  $150 \times 150 \mu\text{m}^2$ . However, this ESD area can be reduced further to around  $70 \times 70 \mu\text{m}^2$  and will be placed under the output pad of each electrode driver.



**Figure 75 ESD protection circuit – Double diode ESD protection circuit**



**Figure 76** Layout of the ESD protection circuit

## 5.9 Layout

The stimulator was laid out with lots of buffers for controlling signals. The layout of the whole stimulator is given in Figure 77. Sixty four electrode drivers are arranged in an array of 8 x 8 with a pitch of 200  $\mu\text{m}$ . There is one more row of 8 pads for inputs (Data, MCLK, Reset), power supplies (1V, 3.3V, VSS for 1V, and VSS for 3V3), and output (common return electrode), which makes a final array of 9 x 8. Total size of the stimulator is 1720 x 1940  $\mu\text{m}^2$ . This layout of the stimulator is put in a 5x5 mm<sup>2</sup> chip together with other blocks of the whole retinal prosthesis chip such as power harvesting circuit, data receiver, data demodulator, and some test circuits.

It can be seen that the layout is for the purpose of connecting the stimulator to an electrode array using flip-chip technique. However, to be able to easily evaluate the performance of the stimulator, all of the pads for flip-chip purpose are also wired to the chip's edges as shown in Figure 78. In addition to 72 pads from array that are wired out, other digital signals from the central controller are also wired to the chip's edges to be

able to test functions of each building circuit of the central controller. Some of these signals are CRC\_GOOD, CRC\_CHECK, serial data out and clock from the bit synchronizer, Sys\_Sink\_Sou (Sys\_Sink and Sys\_Source are combined by an OR gate), and Short. Wiring out signals to pads along chip's edges allows easier access to the pads using wire-bonding technique, which is much easier and quicker to do than flip-chip technique.

Figure 79 shows layout of a full  $5 \times 5 \text{ mm}^2$  chip including other blocks. Total number of pads along the chip's edges is 184. Also shown in the layout is another stimulator, which serves another purpose and is not related to the research in this thesis. More detail about the transceiver and power recovery circuits can be found in [51, 61-63] Figure 80 shows a microphotograph of the fabricated chip including the prototype stimulator.

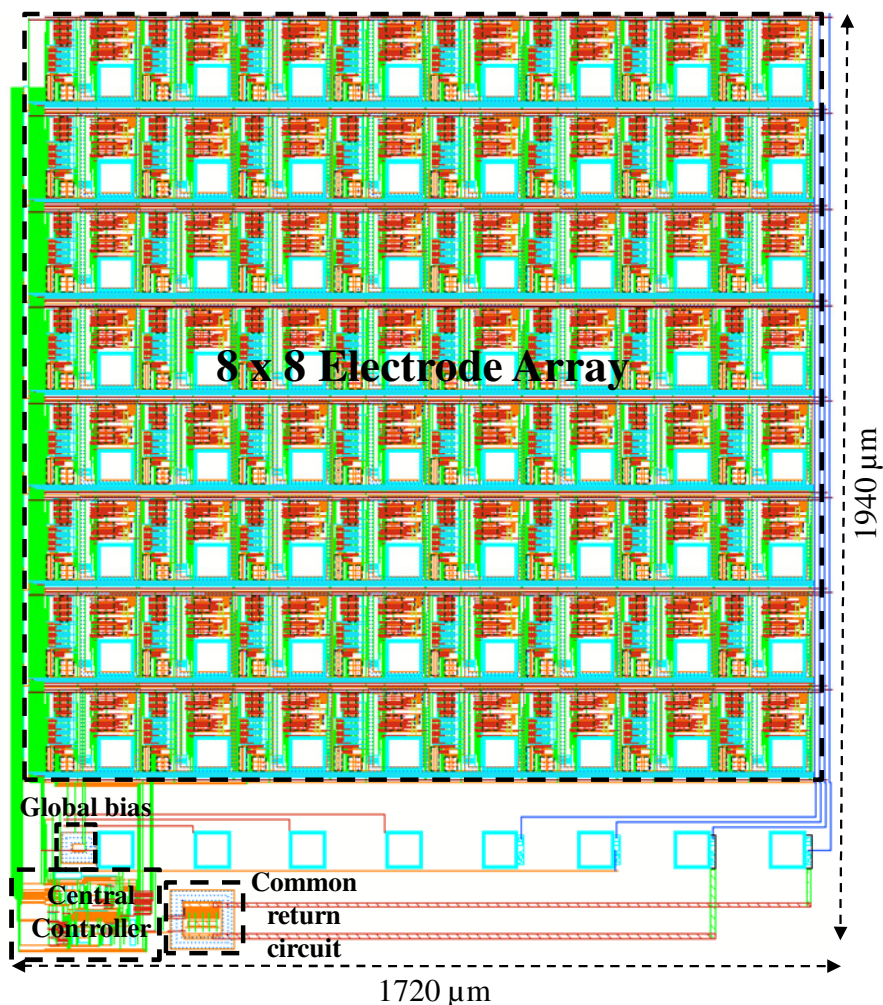


Figure 77 Layout of the prototype 64-electrode stimulator



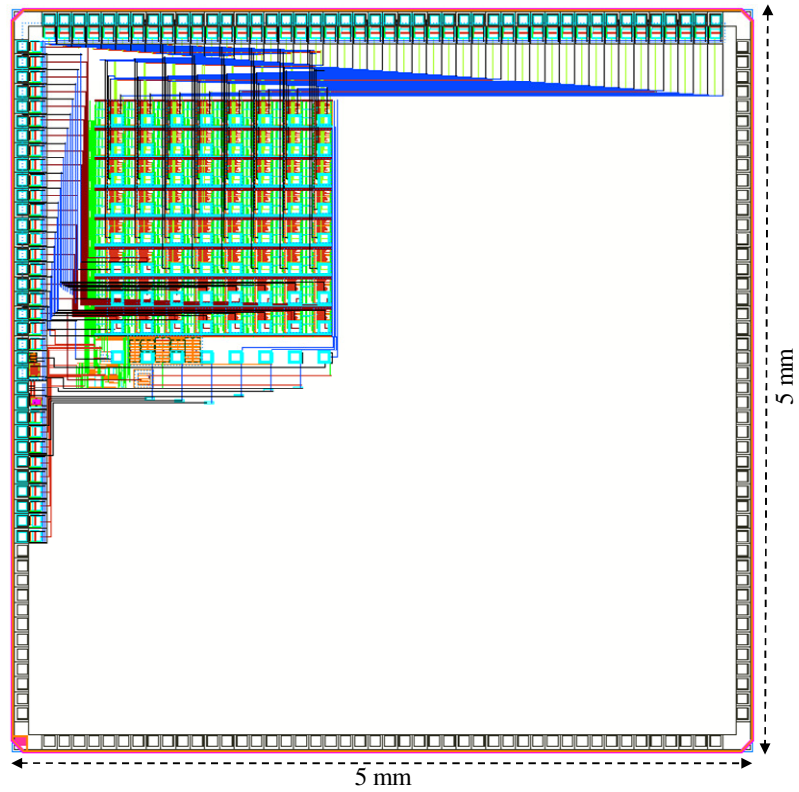


Figure 78 Layout of the stimulator with pads along chip's edges and ESD protection circuits

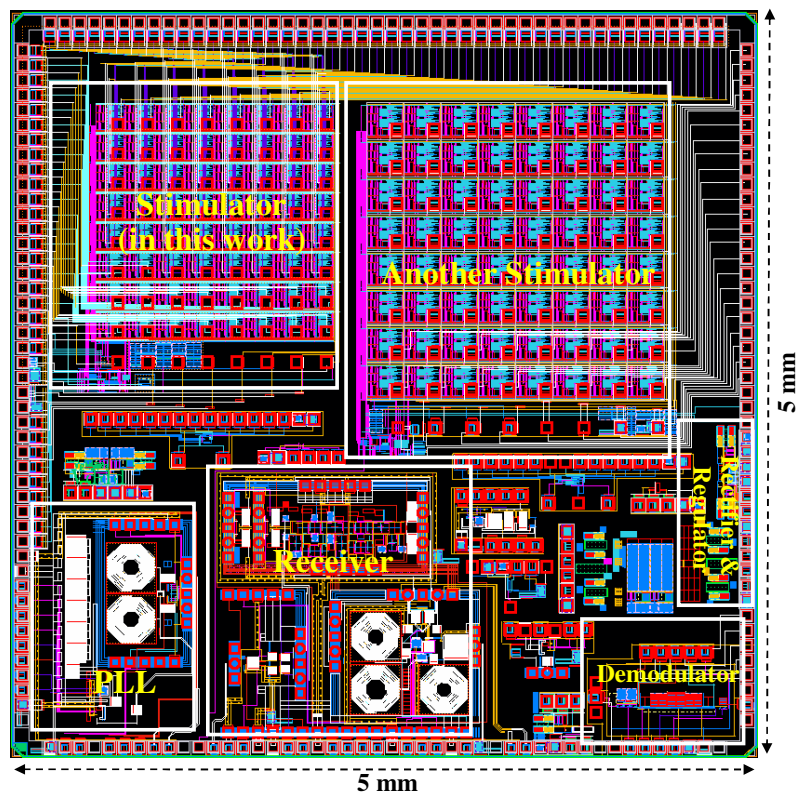
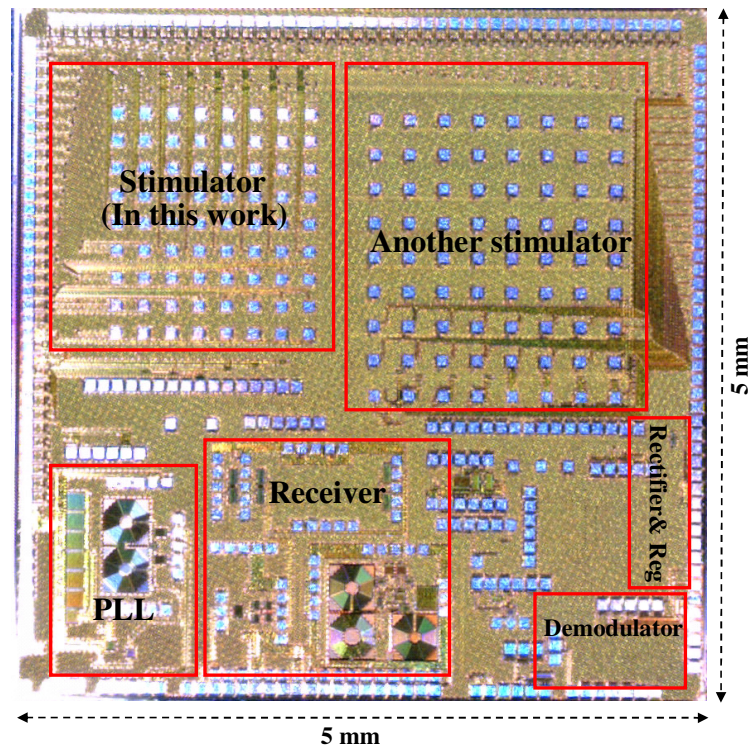


Figure 79 Chip layout, chip size is 5mm x 5mm





**Figure 80** Microphotograph of the fabricated chip

### 5.10 Summary

A prototype 64-electrode stimulator was designed, implemented, and fabricated. Individual building blocks of the stimulator were implemented with custom design and layout. The fabricated stimulator can be connected to the outside world either by flip-chip technique or wire-bonding method.

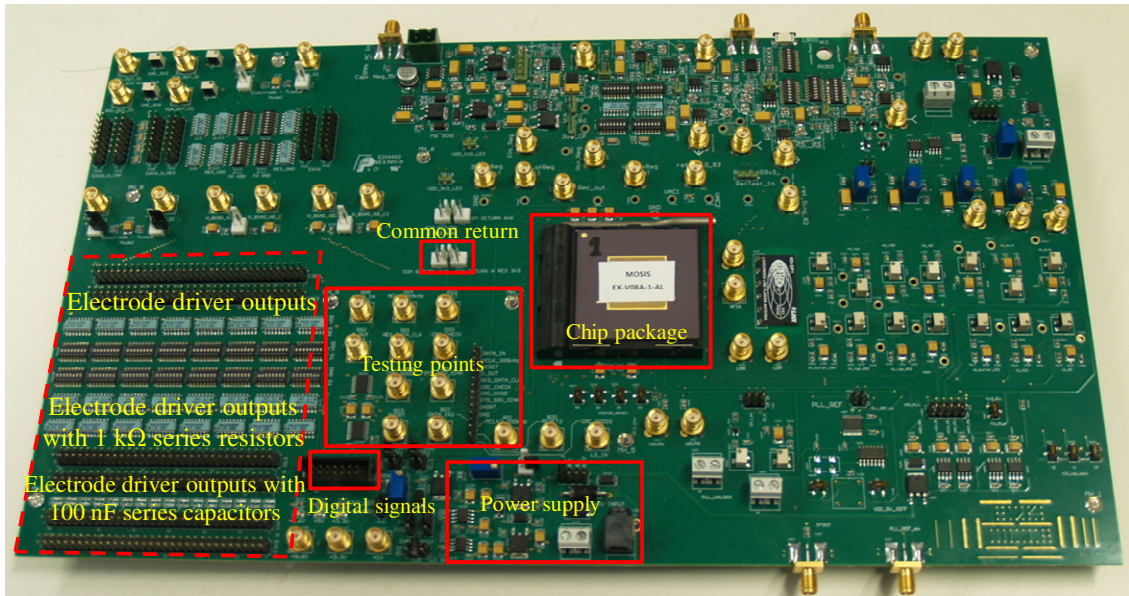


# Chapter 6 Measurement results

The fabricated prototype stimulator was intensively tested to verify all of the proposed flexibility. This chapter presents measurement results of the stimulator. The chapter starts with an introduction to the measurement setup, followed by the evaluation of the electrode driver's performance. The measurement results of all the functions of the central controller end the chapter.

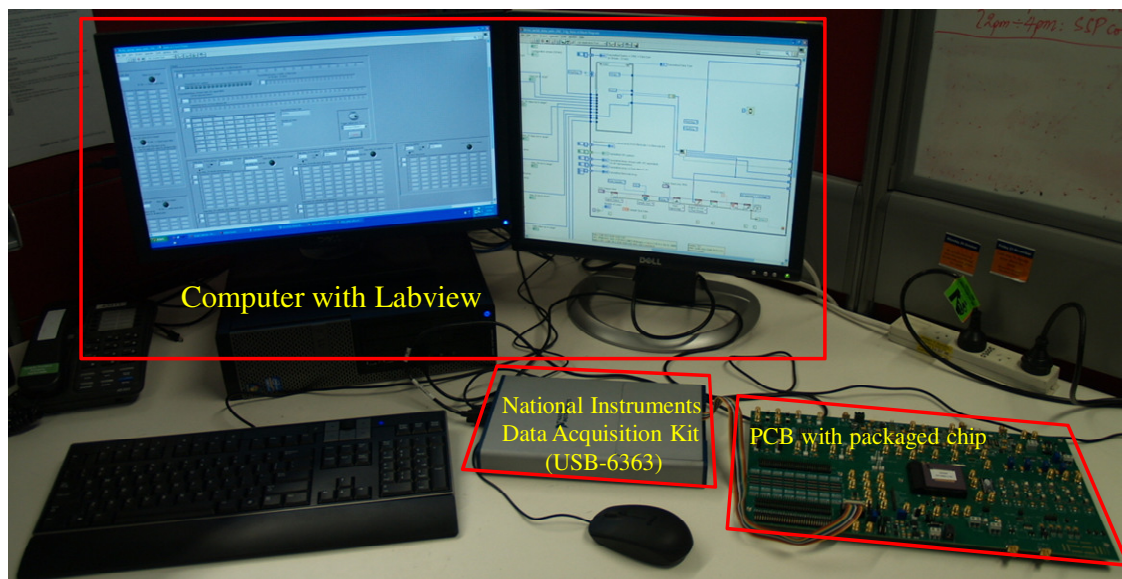
## 6.1 Measurement setup

The fabricated chip was wire-bonded on a 208-pin chip carrier, which is a ceramic pin grid array (CPGA) package. The chip carrier is then connected to the outside world via a zero insertion force socket placed on a printed circuit board (PCB) as shown in Figure 81. This PCB is pretty large as it was designed to test the whole chip including the prototype stimulator, and all other circuits such as data receiver, power harvesting circuit, and demodulator. Each of the 64 electrode driver outputs is connected to a series resistor and a series capacitor. Electrode array can be connected the electrode driver outputs at 3 different ways. It can be connected to the electrode driver outputs via 64-pin headers either directly, or via series 1-k $\Omega$  resistors, or via series 1-k $\Omega$  resistors and 100-nF capacitors. The 1-k $\Omega$  resistors will be used for measuring electrode currents while the 100-nF capacitors will be used as DC blocking capacitors when stimulating with electrode array. Power supplies for the stimulator are regulated from a single 12-V DC supply. Digital inputs and outputs of the stimulators are connected out via a 14-pin header. The output for the remote common return electrode driver is connected out using 2-pin header.



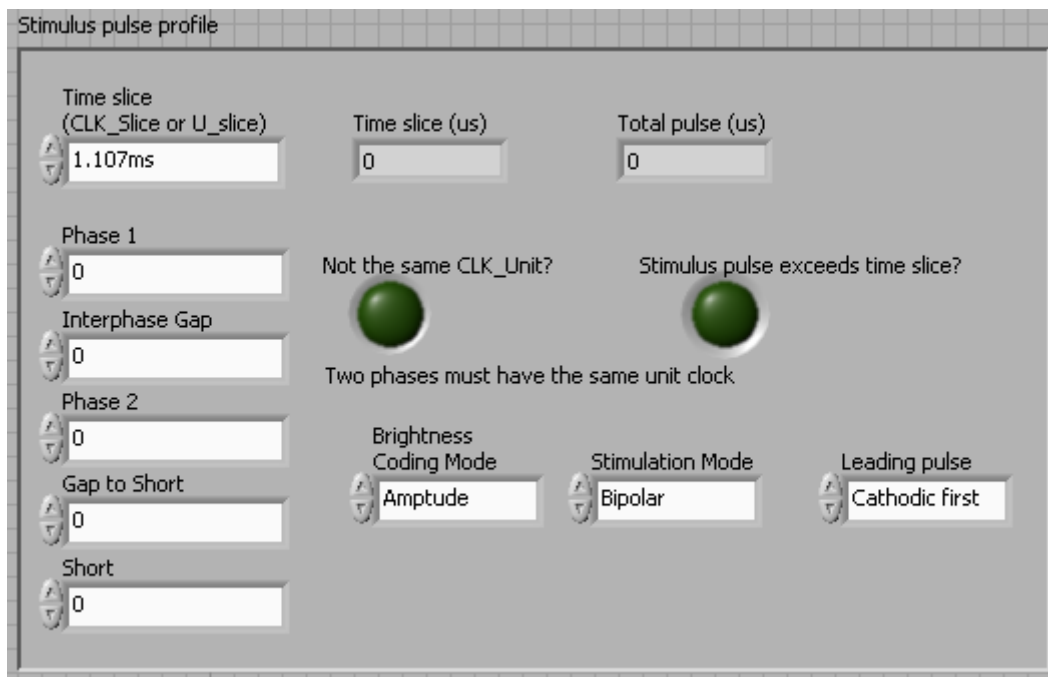
**Figure 81 PCB including the packaged stimulator chip**

The stimulator is digitally controlled by Laboratory Virtual Instrumentation Engineering Workbench (LabVIEW) programs on a computer via a National Instruments data acquisition device (NI-DAQ). The NI-DAQ used in this testing is the Universal Serial Bus 6363 (USB-6363). The whole measurement setup is shown in Figure 82. The USB-6363 kit is connected to computer via USB port, and interfaces with the PCB via a 14-wire ribbon cable.



**Figure 82 Measurement setup**

LabVIEW was chosen to control the stimulator because it is a graphical program language which is very user-friendly and quick to program. It also supports a wide range of data acquisition devices. The main functions of LabVIEW during the stimulator testing are to define the global configuration for the stimulator, to construct data frames for different data types, and to transmit them to the PCB via the USB-6363 kit. With certain data type and main data, the program performs the CRC calculation and attaches the resulted CRC word to the data frame. Figure 83 shows a snapshot of a portion of the LabVIEW program used to control the stimulator. The snapshot shown in the figure contains the global configuration control panel which defines brightness coding mode, stimulation mode, leading pulse, time slice duration, and the time durations for each component of the stimulus pulse.



**Figure 83** Snapshot of a portion of LabVIEW controlling program

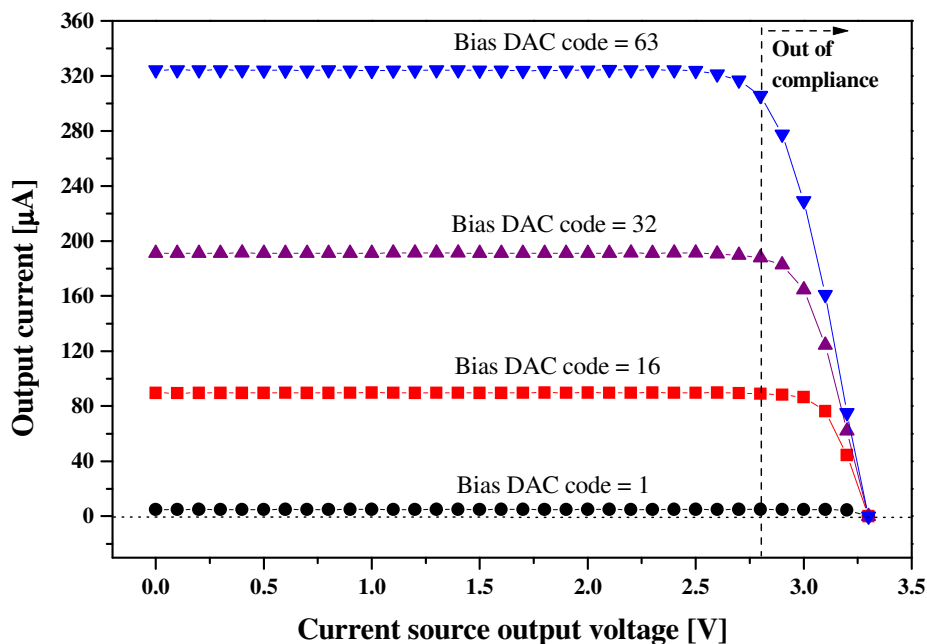
Exhaustive measurements were performed to check the entire operational range of the prototype stimulator. The following section will present all the measurement results including the performance of the electrode driver and the functionality of the central controller.

## 6.2 Electrode driver's performance

This section presents the measurement results for one electrode driver including output compliance voltage, DAC's INL/DNL and linearity.

### 6.2.1 Compliance voltage

Compliance voltage is a very important parameter of every electrical stimulator using current sources as it is the maximum voltage applied to stimulation electrodes with constant stimulation current. Figure 84 shows output currents versus a current source's output voltage at 4 different current steps from 80 nA to 5.04  $\mu$ A. It can be seen that the compliance voltage decreases with increasing output current. The compliance voltage for output current of about 100  $\mu$ A is approximately 3V, and for output current of about 200  $\mu$ A is around 2.8V. For the maximum output current of about 320  $\mu$ A, the compliance voltage is about 2.6V.



**Figure 84 Compliance voltage measurement result**

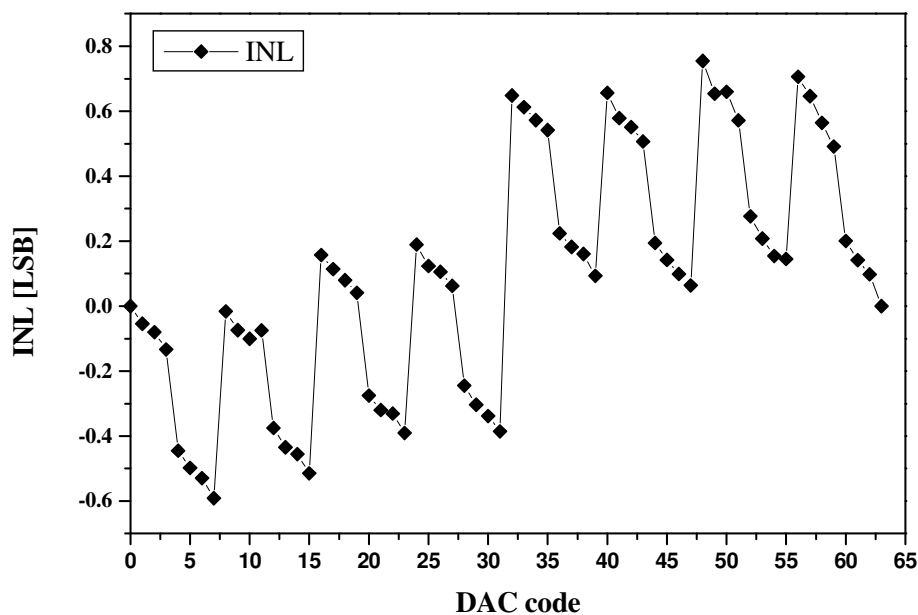
With electrode-tissue impedance of about 30  $k\Omega$  as in [36, 49], to achieve a compliance voltage of 3V, the maximum allowable current is 100  $\mu$ A. In high resolution retinal prostheses, electrode's size is much smaller, the electrode-tissue impedance is



probably higher, and hence the stimulus current required will be smaller. Therefore, with a supply of 3.3V, the designed electrode driver's current source is efficient enough with a useful output voltage of as high as 90% of the supply.

### 6.2.2 DAC's INL/DNL and linearity

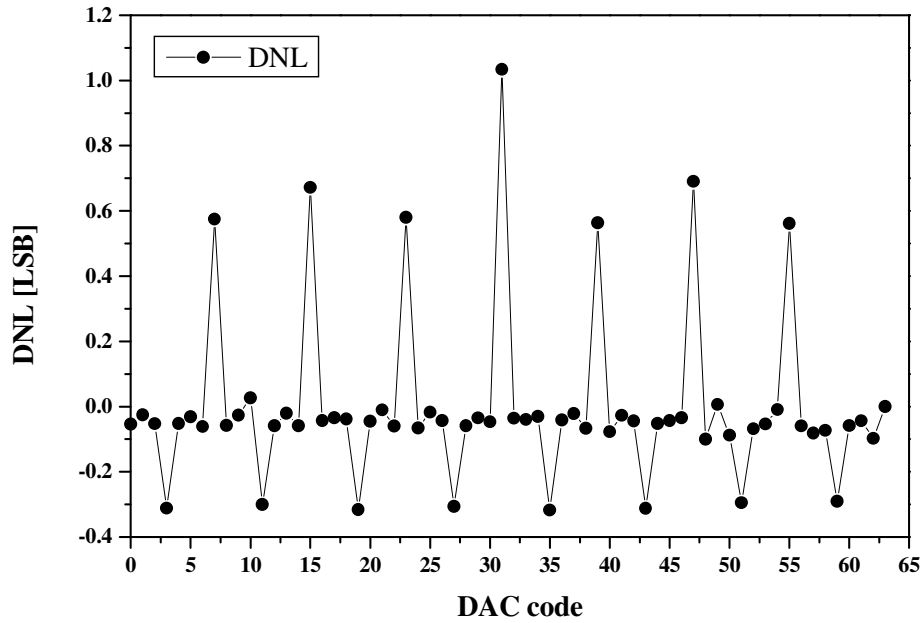
The linearity of the output DAC's is characterized by their integral non-linearity (INL) and differential non-linearity (DNL). Figure 85 shows the measurement INL of the output current source's DAC as a function of input code, the maximum INL is 0.8 LSB.



**Figure 85 INL of the driver's output DAC**

The DNL of the output current source's DAC is shown in Figure 86. The maximum DNL is about 1 LSB. The bias DAC code used for both INL and DNL results is 32. It can be seen that the maximum INL and DNL appears when the DAC input value changes from 31 to 32. This can be explained by looking into the 6-bit binary-weighted DAC's schematic shown in Figure 55 in Chapter 4. When the DAC input changes from '011111' to '100000', the combination of transistors to which the step current is mirrored changes from the combination of x1, x2, x4, x8, x16 transistors to a x32 transistor. The transition at this point has the biggest mismatch, hence causing highest INL and DNL. This big transition mismatch can be reduced by using thermometer-

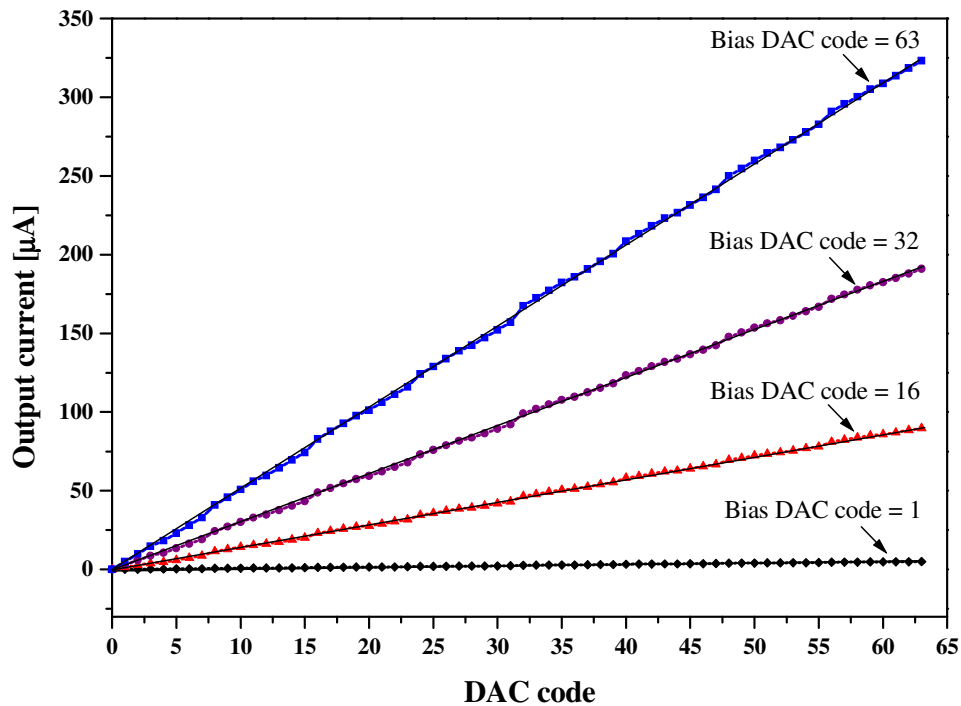
coded DAC instead of binary-weighted DAC [64]; however, more bits are needed to control the DAC.



**Figure 86** DNL of the driver's output DAC

Figure 87 shows output current as a function of DAC input code at 4 different current steps to get a more intuitive view of the DAC's linearity.





**Figure 87 DAC linearity**

Actually, the linearity of output current DAC's is not important in medical applications using electrical stimulation, because the response of tissues to electrical stimulation is not necessarily linear, and hence the amount of input stimulus current does not need to be linearly injected. In addition, the usage of 6 bits for output current DAC's results in 64 different output current levels which can compensate the non-linearity by reducing the number of levels. Indeed, the number of different stimulus current levels which evokes differently distinguishable responses of tissue is much smaller than 64.

### 6.3 Controller performance

This section presents all the measurement results to verify all the proposed stimulation flexibility the stimulator can provide.

#### 6.3.1 Different time slices and pulse width durations

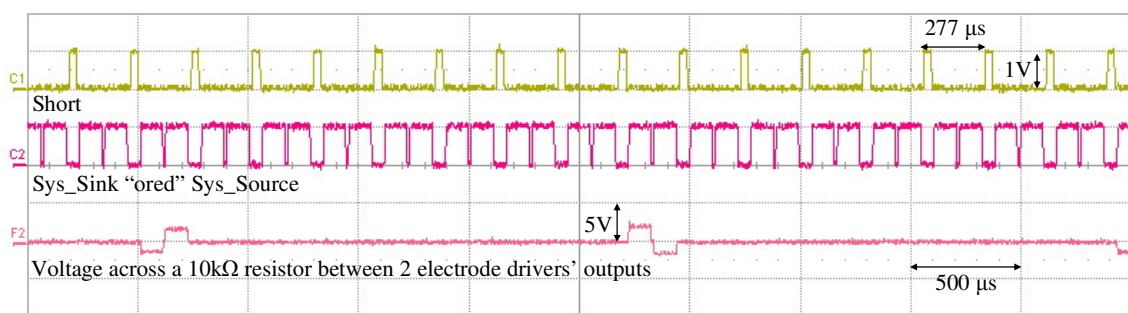
There are 8 time slice durations in each of which different pulse durations of stimulus pulse can be generated. Table 9 lists the measurement parameters to verify the ability of generating all of 8 time slice durations. Although any stimulus pulse widths can be

generated at each time slice duration as long as the total stimulus pulse duration fits within the time slice. However, only one pulse width per time slice is shown.

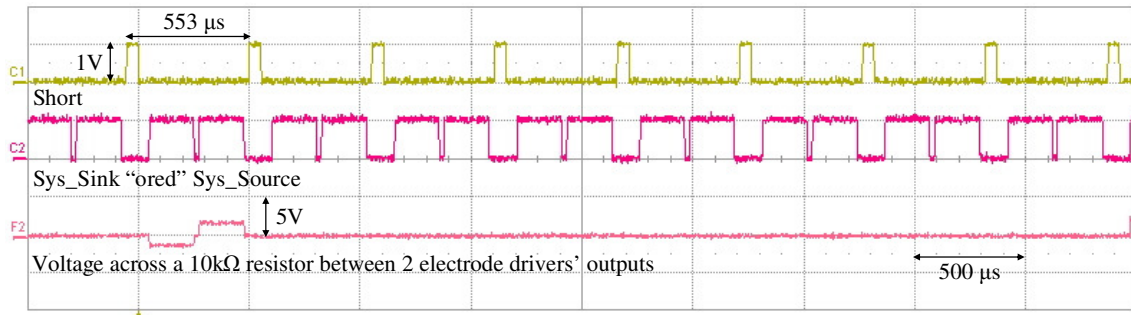
**Table 9 List of different time slices and pulse widths used in the measurement**

Time slice	Pulse width
277 $\mu$ s	100 $\mu$ s
553 $\mu$ s	200 $\mu$ s
1.107 ms	400 $\mu$ s
2.213 ms	800 $\mu$ s
4.427 ms	1.5 ms
8.853 ms	3 ms
17.707 ms	7 ms
35.413 ms	14 ms

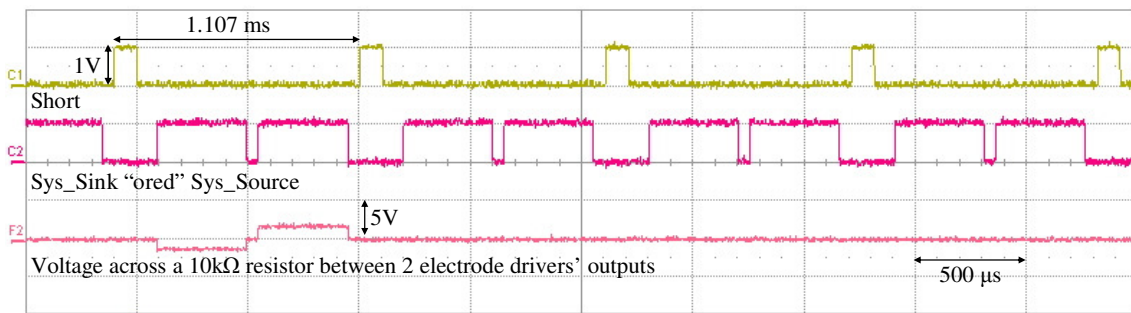
Figure 88, Figure 89, Figure 90, and Figure 91 show measurement results for time slice durations of 277  $\mu$ s, 553  $\mu$ s, 1.107 ms, 2.213 ms, respectively. The Short signal defines the short duration after each stimulus pulse. As mentioned in Section 5.9, the Sys\_Sink and Sys\_Source signals are combined by an OR gate which forms the signal Sys\_Sin\_Sou. The Sys\_Sin\_Sou signal defines durations for the stimulation phase, the interphase gap, and the return phase of stimulus pulse. The gap between the second pulse of Sys\_Sin\_Sou and Short defines the gap-before-shortening duration. To get biphasic waveform across a pair of electrode driver outputs, a 10-k $\Omega$  resistor is connected between one active electrode driver and one return electrode driver. The waveforms were captured by LeCroy WaveRunner 6100A 1GHz oscilloscope. As shown in the figures, the expected pulse durations for each time slice were achieved.



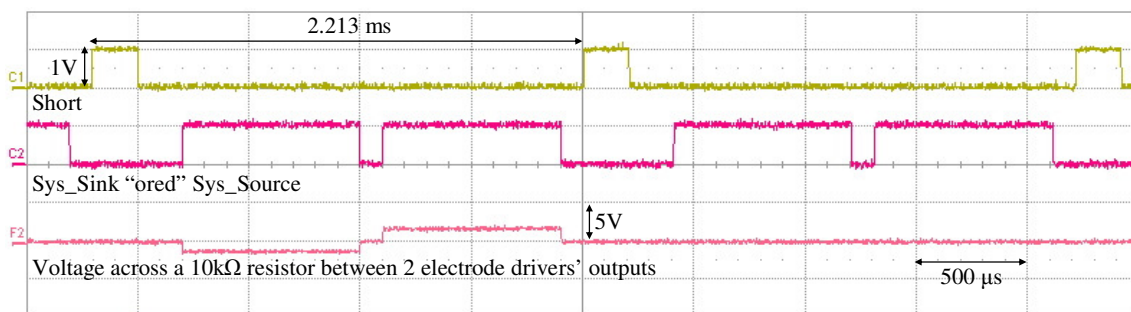
**Figure 88 Measurement result with time slice = 277  $\mu$ s and pulse width = 100  $\mu$ s**



**Figure 89** Measurement result with time slice = 553  $\mu\text{s}$  and pulse width = 200  $\mu\text{s}$

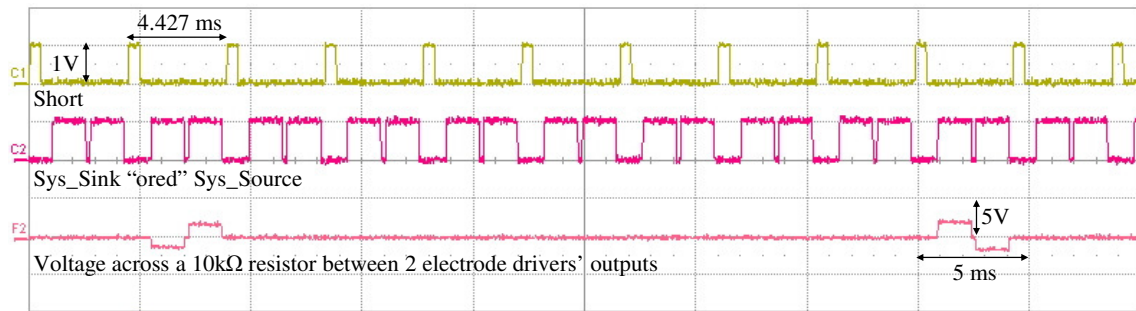


**Figure 90** Measurement result with time slice = 1.107 ms and pulse width = 400  $\mu\text{s}$

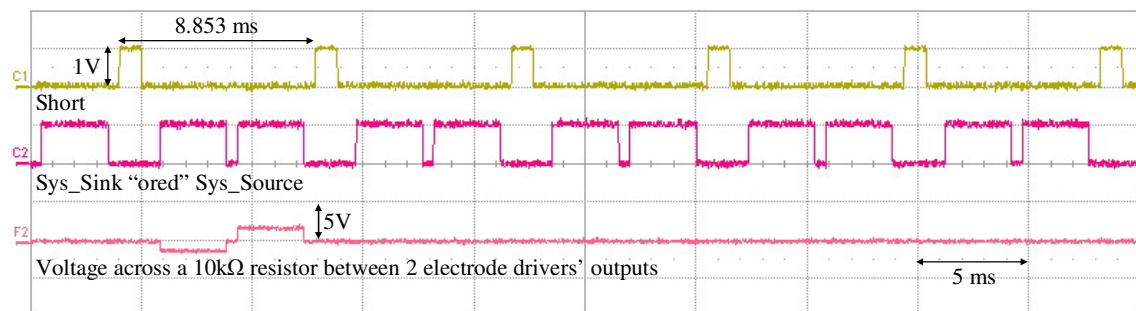


**Figure 91** Measurement result with time slice = 2.213 ms and pulse width = 800  $\mu\text{s}$

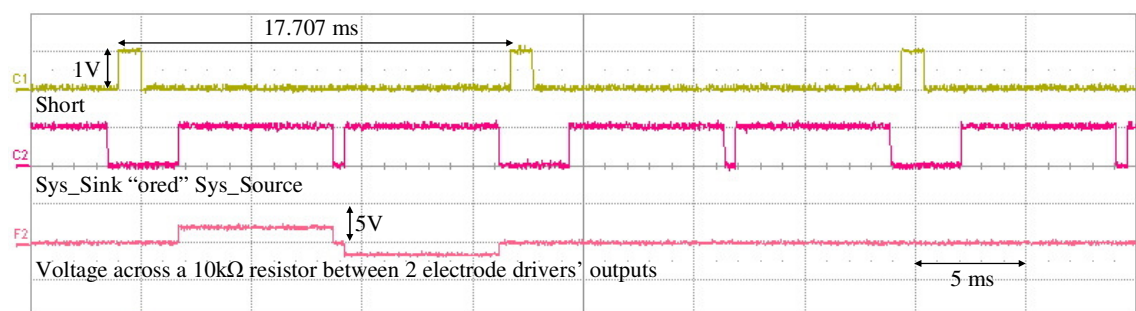
Similarly, Figure 92, Figure 93, Figure 94, and Figure 95 show measurement results for time slice durations of 4.427 ms, 8.853 ms, 17.707 ms, and 35.413 ms, respectively. Different pulse widths could be achieved for each of these time slice durations.



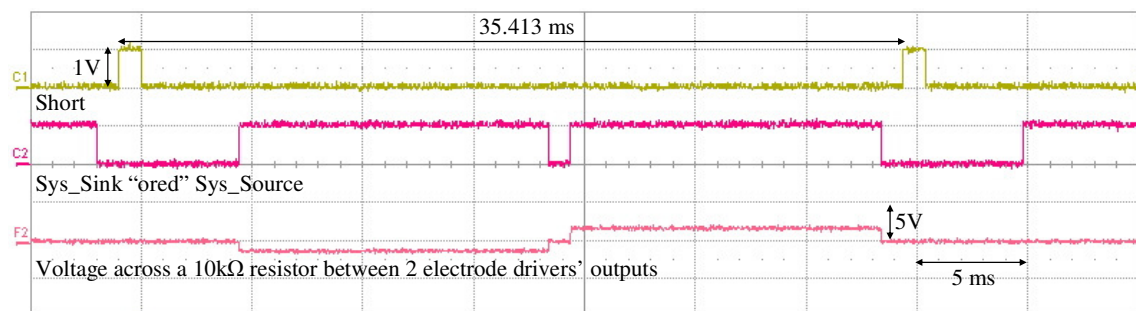
**Figure 92 Measurement result with time slice = 4.427 ms and pulse width = 1.5 ms**



**Figure 93 Measurement result with time slice = 8.853 ms and pulse width = 3 ms**



**Figure 94 Measurement result with time slice = 17.707 ms and pulse width = 7 ms**

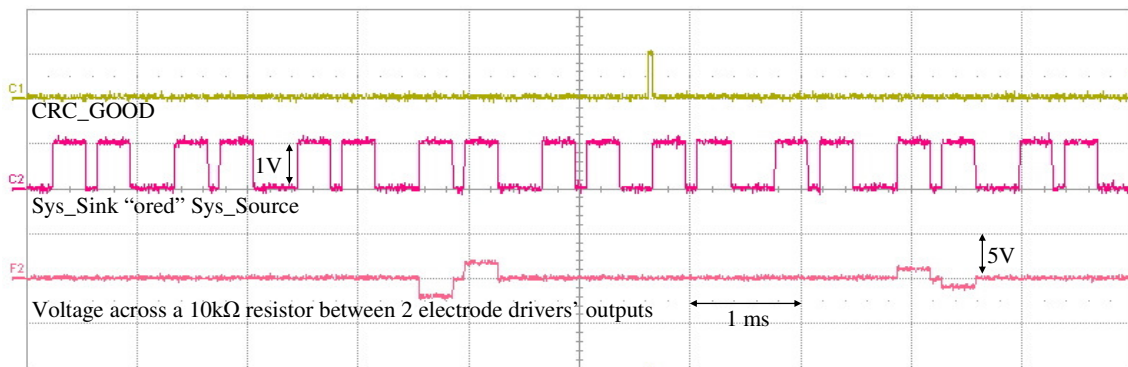


**Figure 95 Measurement result with time slice = 35.413 ms and pulse width = 14 ms**

In summary, wide range timing parameters of stimulus pulse have been achieved by the stimulator.

### 6.3.2 Amplitude coding

In amplitude coding mode to represent brightness, all timing parameters of stimulus pulse are fixed, only current amplitude are changed to represent different brightness levels. Figure 96 shows a stimulus current across a 10-k $\Omega$  resistor between two electrode drivers' outputs. It is shown that when new current amplitude data was updated (CRC\_GOOD went high), the current amplitude changed (decreased).



**Figure 96 Measurement result for amplitude coding**

### 6.3.3 Rate coding

In stimulation rate coding mode to represent brightness, stimulation rate is higher than that of the amplitude coding mode, and the pulse widths are shorter. However, stimulus current amplitude is fixed while the number of stimulus pulses within one stimulation cycle is changed to represent different brightness levels. Figure 97, Figure 98, Figure 99, Figure 100, and Figure 101 show biphasic current waveforms of stimulation using different rate data of '1010', '1000', '1100', '1110', and '1111', respectively. The time slice used was 277  $\mu$ s, both stimulation phase and return phase had the same duration of 100  $\mu$ s.



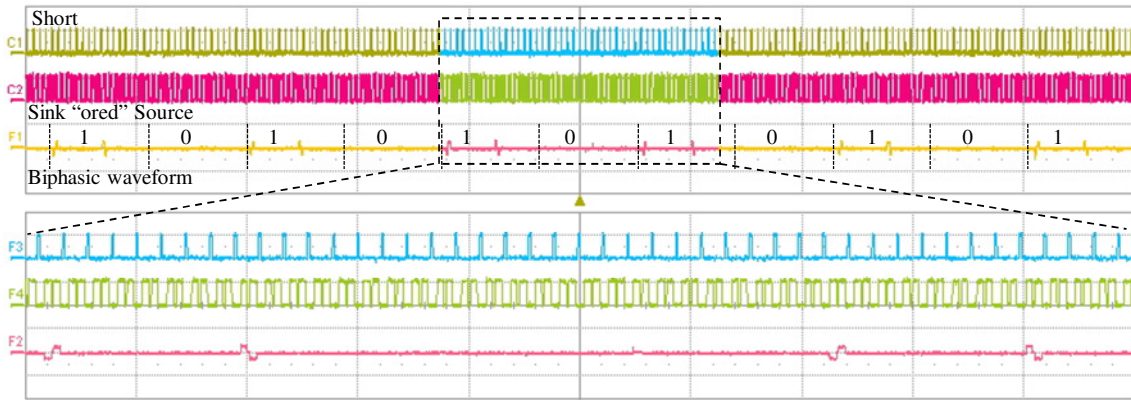


Figure 97 Measurement result for rate coding with rate data = 1010

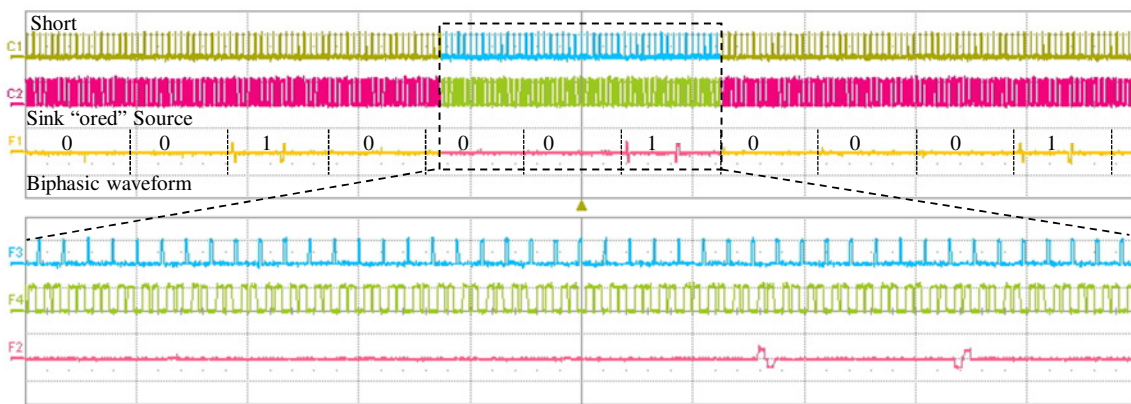


Figure 98 Measurement result for rate coding with rate data = 1000

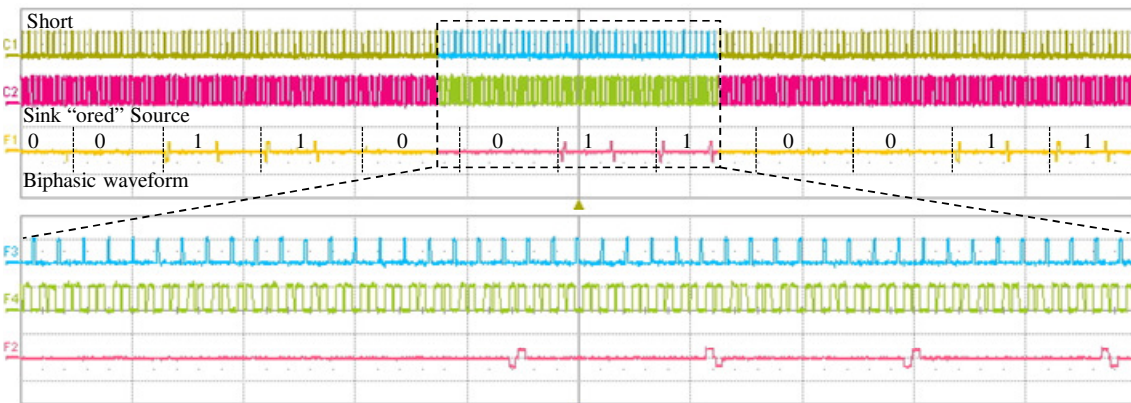
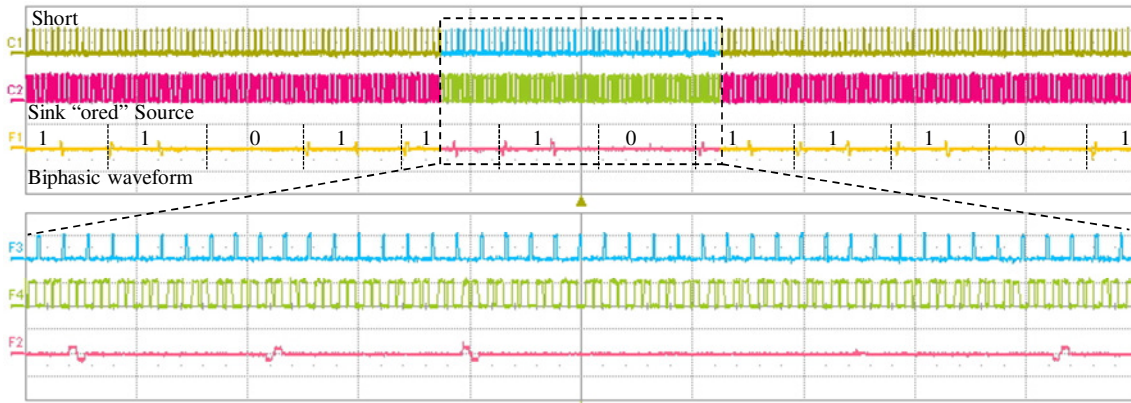
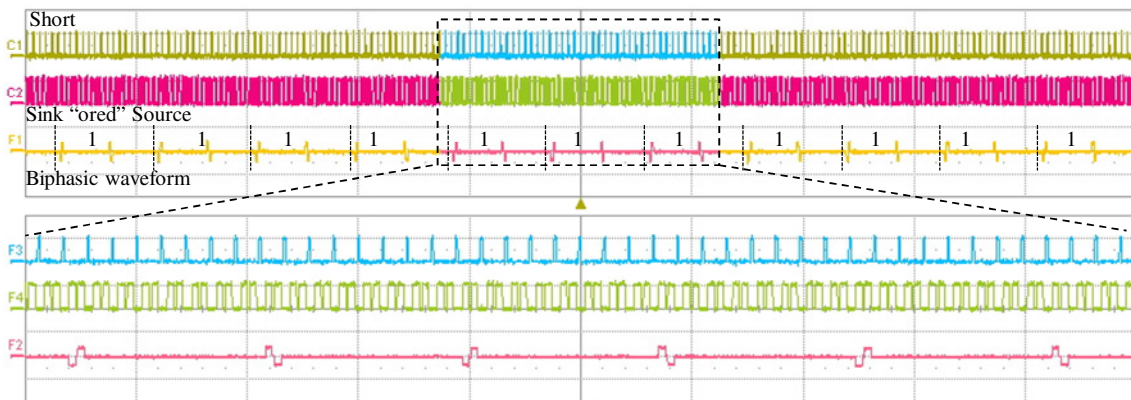


Figure 99 Measurement result for rate coding with rate data = 1100

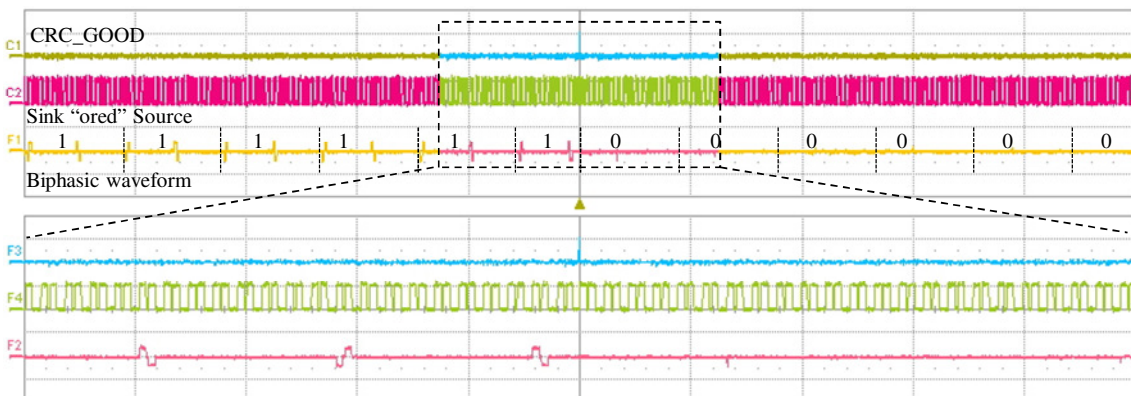


**Figure 100 Measurement result for rate coding with rate data = 1110**

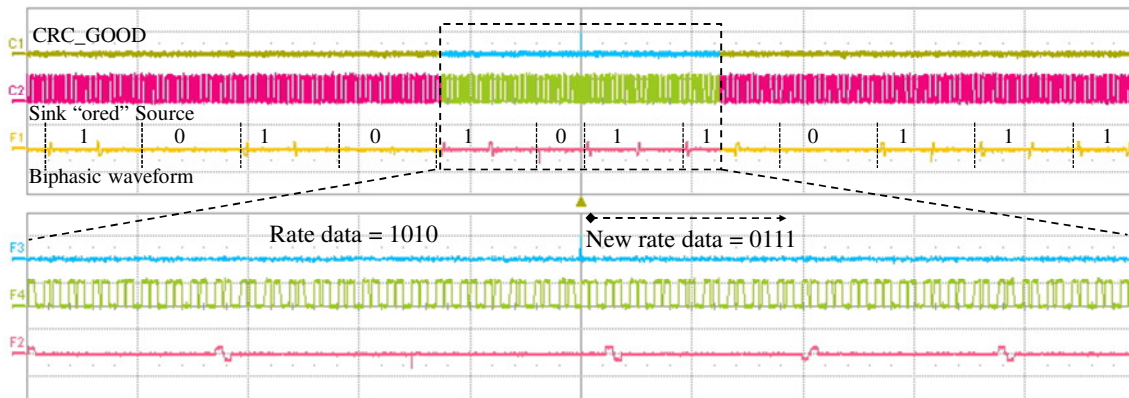


**Figure 101 Measurement result for rate coding with rate data = 1111**

Figure 102 and Figure 103 show biphasic current waveforms of stimulation where rate data changed from '1111' to '0000' and '1010' to '0111', respectively.



**Figure 102 Measurement result for updating rate coding with rate data from 1111 to 0000**



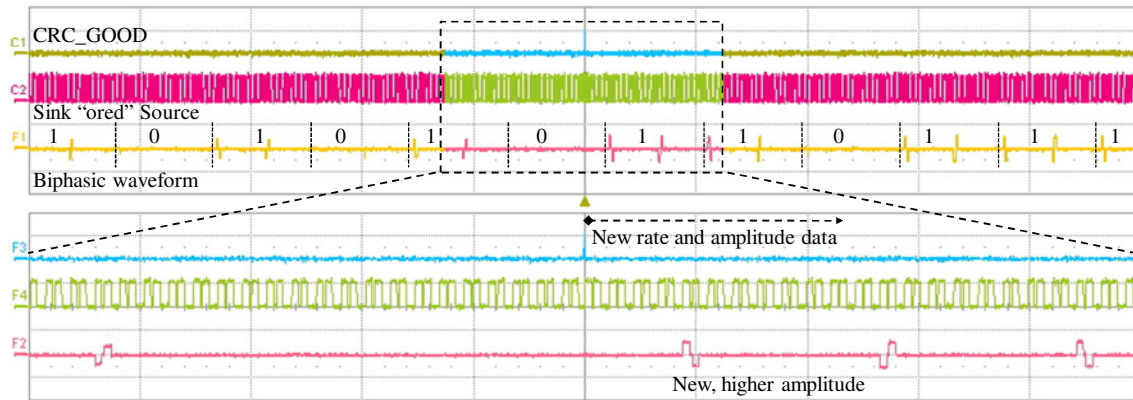
**Figure 103 Measurement result for updating rate coding with rate data from 1010 to 0111**

In short, stimulation with different stimulation rate data was shown to operate properly. The stimulation using different rates may result in different effects as compared to the stimulation using different current amplitudes when both delivering the same amount of charge.

### 6.3.4 Combined rate and amplitude coding

An additional feature of the prototype stimulator is that both amplitude and rate of stimulus pulse can be changed at the same time to represent brightness. This feature may help realizing new stimulation strategies. In the ultimate high resolution retinal stimulator, as long as the data transmission bandwidth is sufficient, the feature can be included. Figure 104 shows biphasic current waveform where data rate changed from '1010' to '0111', and amplitude increased.

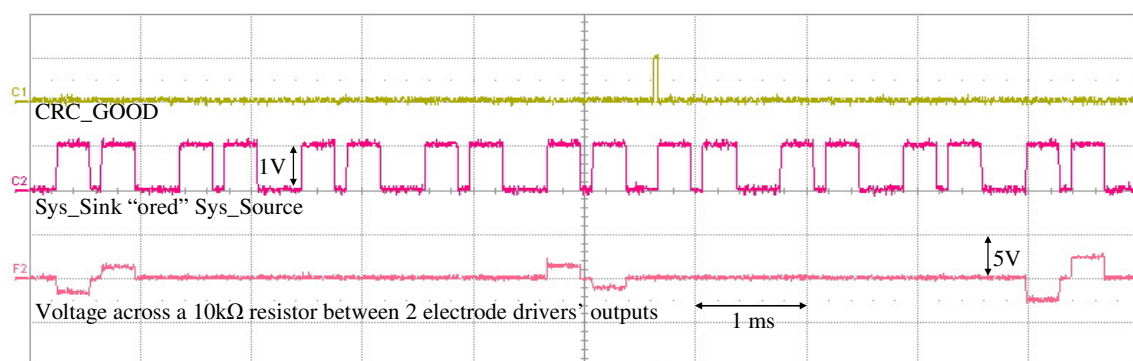




**Figure 104 Measurement result for combined amplitude and rate coding with rate data changing from 1010 to 0111 and higher amplitude**

### 6.3.5 Threshold and stimulus combination

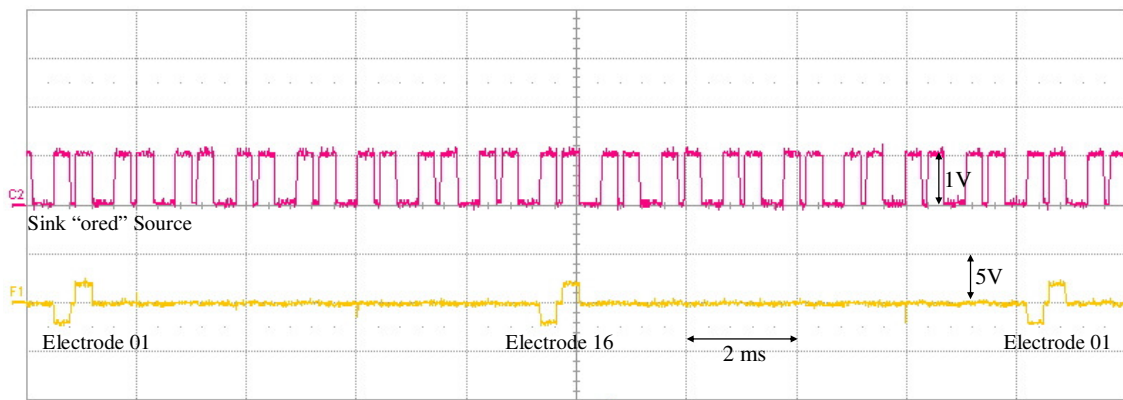
Combined threshold and stimulus current helps not only double the output current but also fully utilize 64 levels of stimulus current amplitude. Figure 105 shows biphasic current waveform of stimulation where threshold current and stimulus current were combined. At the beginning, the current was just a threshold current of  $120\ \mu\text{A}$ . When stimulus current's amplitude data was written (CRC\_GOOD went high), the current was doubled to  $240\ \mu\text{A}$  as the new current was the combination of the threshold current and the stimulus current, both with the same amplitude of  $120\ \mu\text{A}$ .



**Figure 105 Measurement result for the threshold and amplitude combination**

### 6.3.6 Common return

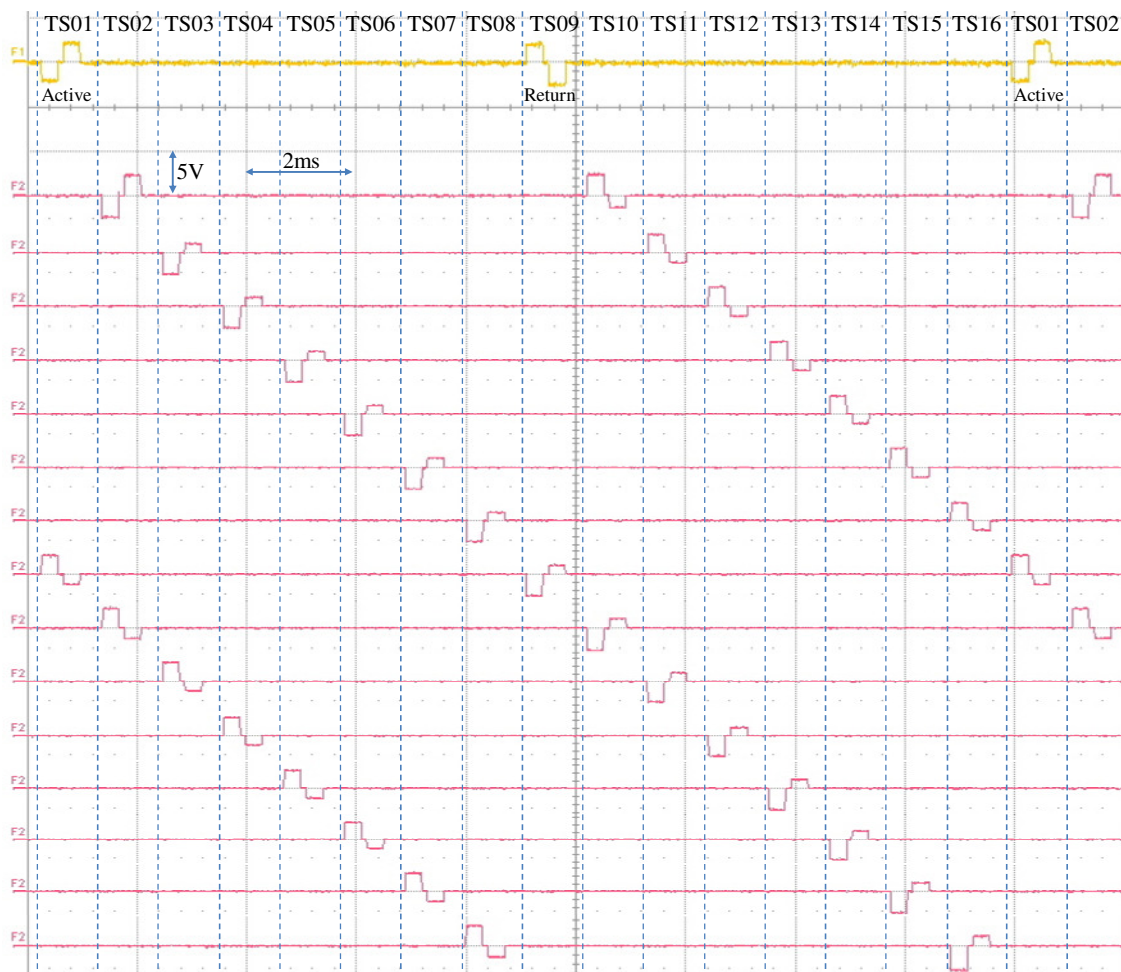
In monopolar stimulation mode, one remote electrode acts as a common return electrode while all electrodes in the array act as active. Figure 106 shows biphasic current waveform through the common return electrode. In this stimulation, the number of time slices was 16. In the array, electrode 1 was active at time slice number 1 and electrode number 16 was active at time slice number 8. The current flowing into the common return electrode was the sum of two currents from the two electrodes, each of which was  $100\ \mu\text{A}$ .



**Figure 106 Measurement result for the common return operation**

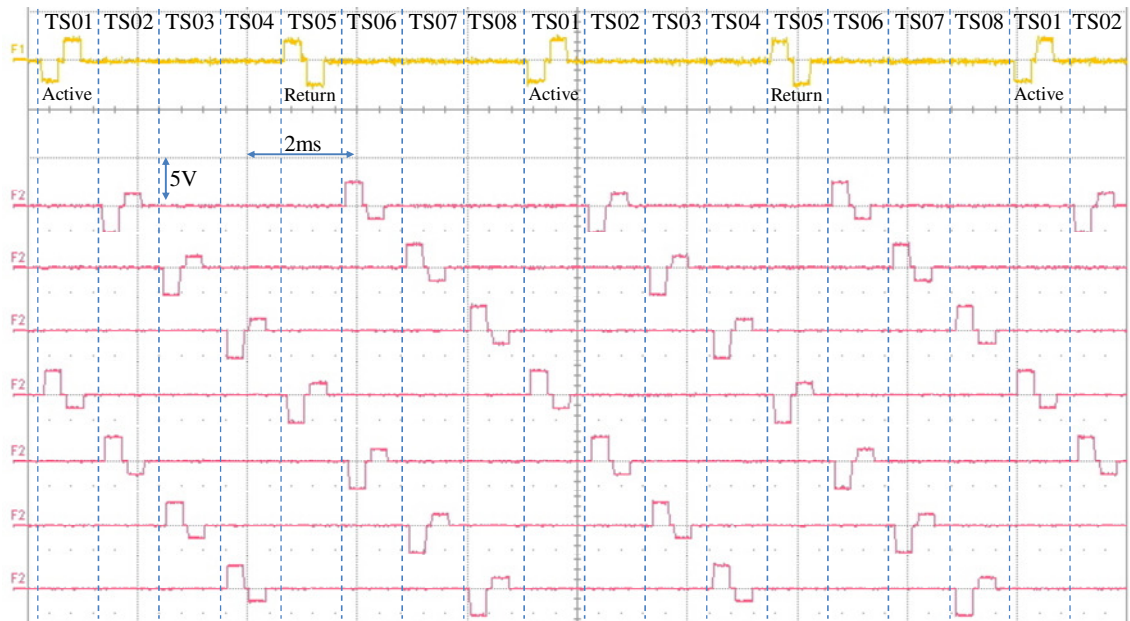
### 6.3.7 Electrode selection and different number of time slices

The number of time slices the stimulator is able to provide can be 16, 8, 4, 2, and 1. Within one time slice, any electrodes and any number of them can be selected as active or return. Figure 107 shows measurement result of stimulation using 16 time slices. 16 different pairs of electrodes were used to measure biphasic currents, each of which was stimulated at one time slice.

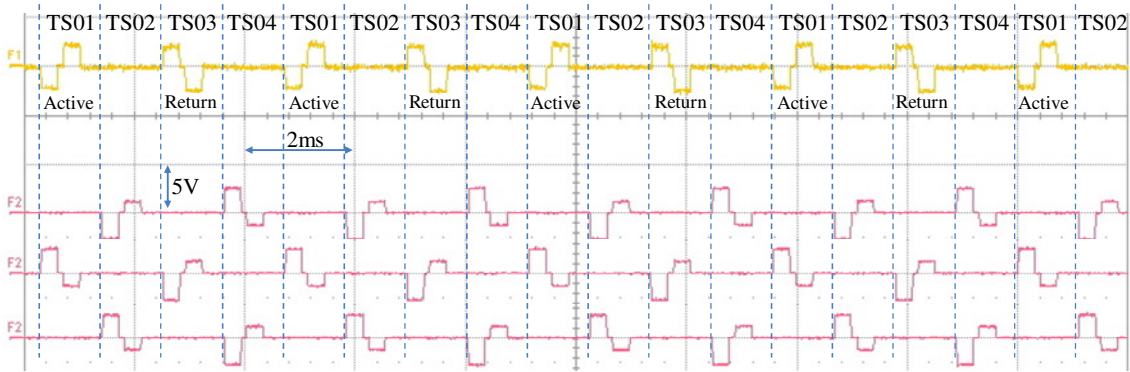


**Figure 107 Measurement result for the stimulator's operation with 16 time slices**

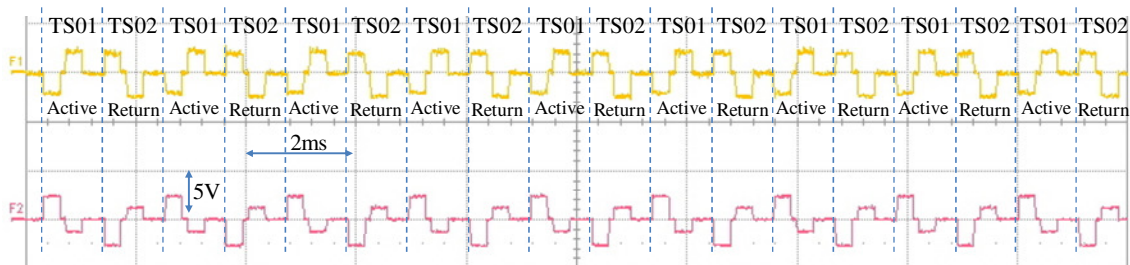
Figure 108 shows measurement result of stimulation using 8 time slices. Eight different pairs of electrodes were used to measure biphasic currents, each of which was stimulated at one time slice. Figure 109 and Figure 110 show measurement results of stimulation using 4 and 2 time slices, respectively. Stimulation using only one time slice is only applicable to monopolar stimulation mode. In these figures, one phase of all the currents except the first one has less amplitude compared to the other phase. It is due to the impedance mismatch among the probes for the oscilloscope. In fact, one of 4 probes of the oscilloscope was missed, and it was replaced by another one which caused the channel's input impedance to decrease, which then reduced the voltage measured at the electrode driver's output causing lower amplitude.



**Figure 108 Measurement result for the stimulator's operation with 8 time slices**



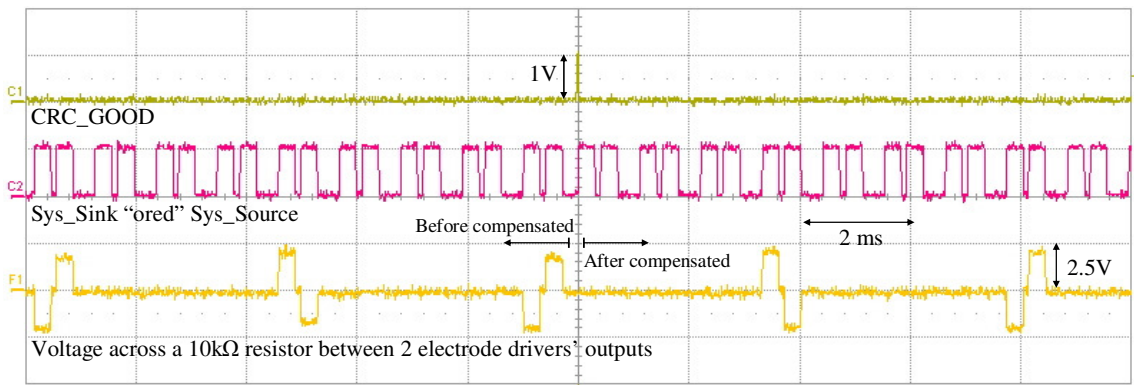
**Figure 109 Measurement result for the stimulator's operation with 4 time slices**



**Figure 110 Measurement result for the stimulator's operation with 2 time slices**

### 6.3.8 Current mismatch and compensation

The current sink and current source in the electrode driver are practically mismatched. One of the purposes of using 6-bit DAC rather than less number of bits is to compensate the mismatch. Figure 111 shows the stimulus current before and after compensated. Before compensated, the cathodic and anodic phases had the same values of bias ( $2\ \mu\text{A}$ ) and data (30). The currents at the two phases were supposed to be  $120\ \mu\text{A}$  (combined threshold and stimulus). However, the anodic phase (current source) always had lower amplitude than that of the cathodic phase (current sink). Therefore, the digital value written for the anodic phase must be greater. The anodic phase amplitude was then adjusted from 30 to 40, the mismatch no longer existed.

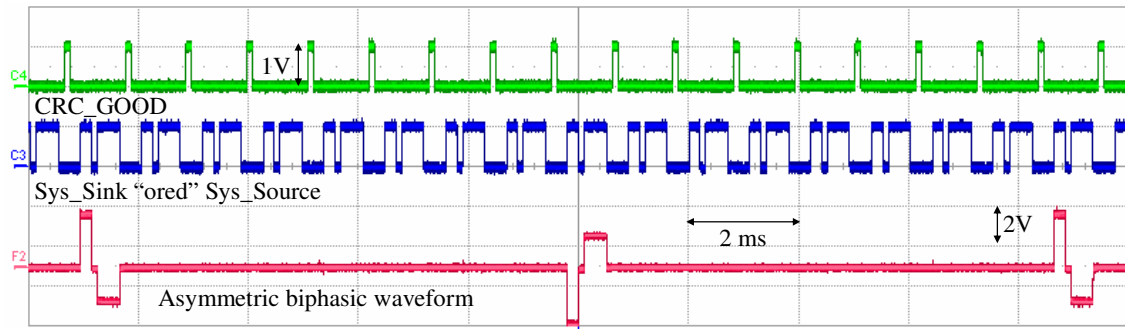


**Figure 111 Measurement result for the current mismatch and compensation**

### 6.3.9 Asymmetric waveform

Asymmetric waveform can be achieved to provide flexibility in providing different current waveforms. Figure 112 shows biphasic current waveform with two phases having different current amplitude and duration.





**Figure 112 Measurement result for the stimulation using asymmetric waveform**

#### 6.4 Summary

The prototype stimulator was fully tested to verify its functionality as well as all of the proposed stimulation flexibility. Measurement results confirmed all proper operations, all the circuits operated with good performance as designed. Table 10 summarizes specifications of the prototype stimulator. The total power consumption of the stimulator with all 64 electrodes being active at the same time with currents of  $100\mu\text{A}$  is 21.52 mW, which is well below the power budget of 50 mW from the inductive link [62].

**Table 10 Specifications of the prototype stimulator**

Technology	65 nm CMOS
Stimulator's size	$1720 \times 1940 \mu\text{m}^2$
Single electrode driver's size (with pad)	$200 \times 200 \mu\text{m}^2$
Supply voltage	
Core controller	1 V
Output driver	3.3 V
Power consumption	
Central controller	$200 \mu\text{W}$
Driver array (without stimulation)	$200 \mu\text{W}$
Total (64 active electrodes, $100\mu\text{A}$ each)	21.52 mW
Current source/sink compliance voltage	3 V
Number of electrode drivers	64
Data rate	30 kbps
DAC INL/DNL	0.8 LSB/1 LSB
DAC resolution	6 bits
Output current range	80 nA to $635 \mu\text{A}$

# Chapter 7 Conclusion and Future Work

## 7.1 Conclusion

A stimulator for 1024-electrode retinal prosthesis was designed for flexibility. The stimulator was implemented in 65 nm CMOS process to realize high integration and low power consumption. To date, this is the smallest-scale CMOS process ever used for retinal prostheses. Small-scale CMOS process with low supply voltage is probably unavoidable in order to realize high resolution retinal prosthesis with more than 1000 electrodes.

The flexibility includes the ability of stimulating using both stimulus current amplitude and stimulation rate to represent phosphene brightness, and the ability of stimulating using both bipolar and monopolar configuration. The ability of providing wide-range current amplitude from 80 nA to 317.5  $\mu$ A with 64 different step sizes is another flexible feature. The stimulator can provide various stimulation refresh rates ranging from as high as 226 Hz to as low as 1.76 Hz. Stimulus pulse widths, interphase delay, and after-each-stimulus-pulse electrode shorting duration also vary in a wide range from 10  $\mu$ s to 14 ms. Electrode selection is fully flexible where any electrodes and any number of them can be selected as active or return at any time slice. The separation of image data update rate and stimulation refresh rate helps reduce data bandwidth by a half, which is very beneficial because the bandwidth for the data receiver of the stimulator chip is limited to 300 kHz.

A prototype 64-electrode stimulator was designed, fabricated, and tested. This stimulator had all of the proposed flexibility for the high acuity stimulator. The prototype stimulator was extensively tested. All proposed stimulation flexibility was confirmed to operate properly. The fully functioned stimulator will be used for preclinical tests to help realize many stimulation strategies.

## 7.2 Future Work

In order to build the ultimate 1024-electrode stimulator, several circuits from the prototype 64-electrode stimulator can be re-used such as the clock profile, the stimulus pulse generator, the common return circuitry, the global bias circuit, the bit synchronizer, the CRC checker, the data type decoder, and especially the electrode driver. The only circuit of the prototype stimulator that needs to be re-designed is the frame synchronizer because the number of electrodes is increased, more data will be needed, and hence data frame structure may be changed. The frame synchronizer needs to be re-designed to deal with these changes.

Small size of the implantable device is one of the critical requirements due to the limited area of the retina. A  $6 \times 5 \text{ mm}^2$  silicon chip is planned to be used for the whole retinal prosthesis chip, in which  $5 \times 5 \text{ mm}^2$  is allocated to house the 1024- electrode stimulator. The electrode drivers are arranged in an array of  $32 \times 32$  with pitches of  $150 \mu\text{m}$  between adjacent drivers, resulting in an area of  $150 \times 150 \mu\text{m}^2$  per electrode driver. Therefore, the electrode driver needs to be re-laid out to reduce the area from  $200 \times 200 \mu\text{m}^2$  to  $150 \times 150 \mu\text{m}^2$ . This layout reduction can be done quite easily because in the fabricated prototype stimulator, the layout was not optimized with lots of unused space.

Charge balance is another important issue with the high density retinal stimulator. In the designed electrode driver, the mismatch between the current sink and the current source can be roughly compensated by using different digital values for their DAC's inputs. Applying electrode shorting after every stimulus pulse can help discharging any residual charge. However, with the high density retinal stimulator, simultaneous stimulation with multiple electrodes stimulated at a time is unavoidable. Simultaneous stimulation may result in current crosstalk between electrodes, which causes charge imbalanced. Therefore, other charge balancing techniques need to be considered to make sure charge balance is achievable in the ultimate 1024-electrode stimulator.



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