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# Probabilistic modeling of quantum-dot cellular automata

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# Probabilistic Modeling of Quantum-Dot Cellular Automata

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
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**DEDICATION**

To my loving wife and my parents.

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**Saket Srivastava**

## ABSTRACT

As CMOS scaling faces a technological barrier in the near future, novel design paradigms are being proposed to keep up with the ever growing need for computation power and speed. Most of these novel technologies have device sizes comparable to atomic and molecular scales. At these levels the quantum mechanical effects play a dominant role in device performance, thus inducing uncertainty. The wave nature of particle matter and the uncertainty associated with device operation make a case for probabilistic modeling of the device. As the dimensions go down to a molecular scale, functioning of a nano-device will be governed primarily by the atomic level device physics. Modeling a device at such a small scale will require taking into account the quantum mechanical phenomenon inherent to the device.

In this dissertation, we studied one such nano-device: Quantum-Dot Cellular Automata (QCA). We used probabilistic modeling to perform a fast approximation based method to estimate error, power and reliability in large QCA circuits. First, we associate the quantum mechanical probabilities associated with each QCA cell to design and build a probabilistic Bayesian network. Our proposed modeling is derived from density matrix-based quantum modeling, and it takes into account dependency patterns induced by clocking. Our modeling scheme is orders of magnitude faster than the coherent vector simulation method that uses quantum mechanical simulations. Furthermore, our output node polarization values

match those obtained from the state of the art simulations. Second, we use this model to approximate power dissipated in a QCA circuit during a non-adiabatic switching event and also to isolate the thermal hotspots in a design. Third, we also use a hierarchical probabilistic macromodeling scheme to model QCA designs at circuit level to isolate weak spots early in the design process. It can also be used to compare two functionally equivalent logic designs without performing the expensive quantum mechanical simulations. Finally, we perform optimization studies on different QCA layouts by analyzing the designs for error and power over a range of kink energies.

To the best of our knowledge the non-adiabatic power model presented in this dissertation is the first work that uses abrupt clocking scheme to estimate realistic power dissipation. All prior works used quasi-adiabatic power dissipation models. The hierarchical macromodel design is also the first work in QCA design that uses circuit level modeling and is faithful to the underlying layout level design. The effect of kink energy to study power-error tradeoffs will be of great use to circuit designers and fabrication scientists in choosing the most suitable design parameters such as cell size and grid spacing.

# CHAPTER 1

# INTRODUCTION

In late 1960's Gordon Moore, of Intel Corporation, predicted that the transistor density or the number of transistors on an IC chip will grow exponentially over time [1]. This trend of semiconductor scaling has been the benchmark for the growth of research and development activity all over the world. Until recently, semiconductor industry has been able to keep up with Moore's law over the years, packing more and more computational power into our microprocessors. With transistor size shrinking to nanometer scales, it has been a hard battle in the recent years for the industry to keep up with the scaling process. The smallest transistors in production today operate despite quantum effects. In the near future, the operation of transistors will be dominated by the physics of quantum world. Physical limitations of conventional transistors including power dissipation, interconnects and fabrication are becoming increasingly difficult to surmount with each technology generation [2, 3]. There will be an urgent need in the near future to replace the current device, the CMOS transistor, by one that embraces these quantum effects and takes advantage of the nanoscale physics. Keeping this in mind, novel design paradigms are being proposed to keep up with the ever growing need for computation power and speed. There needs to be a change in perspective from the designers and fabrication scientists alike to look beyond CMOS.

## 1.1 Motivation

While even the current generation CMOS technology is nanoscale, the issues related to doping regions, oxide thickness, sticking layers, diffusion barriers, power dissipation, and leakage currents etc. have put a big question on the feasibility of pursuing with CMOS technology in future [4, 5]. The big question for nanotechnology is, what happens after that and what kind of nanotechnology will be used to replace the standard CMOS transistors?

The question has two answers. In order to stay on the roadmap with its inexorable progress, nanotechnology is already required. It is clear that CMOS scaling will continue for at least 10 more years till around 2018 [6]. This will require the increasing use of nanotechnology in new materials for dielectrics, gates, interconnects, and channels. There will be new processes, materials, and structures that require engineering at the nanoscale. Thus, for at least 10 years, nanotechnology will extend and enhance standard CMOS VLSI technology. While in a decade or more much of the standard approach will be nanoscale, though it will not be a revolution but like an rapid evolution, it will still be a continuation of what has gone on before.

So the question again arises, what happens after that? Which device will be the new switch? Candidates include Quantum Cellular Automata [7],Carbon Nanotube Transistors [8, 9], silicon nanowires [10], spin transistors [11], superconducting electronics [12, 13], molecular electronics [14, 15], Single Electron Transistors [16, 17], Resonant Tunneling Devices [18] and Tunneling Phase Logic [19] as portrayed in Fig 1.1. The International Technology Roadmap for Semiconductors (ITRS) describes how these technologies work and discuss some of the challenges in implementing them. The ITRS roadmap [6] presents the ”best current estimate” based on an industry-wide consensus of its R&D needs for the next 15 years. It is considered to be an unbiased document that is used by industry and

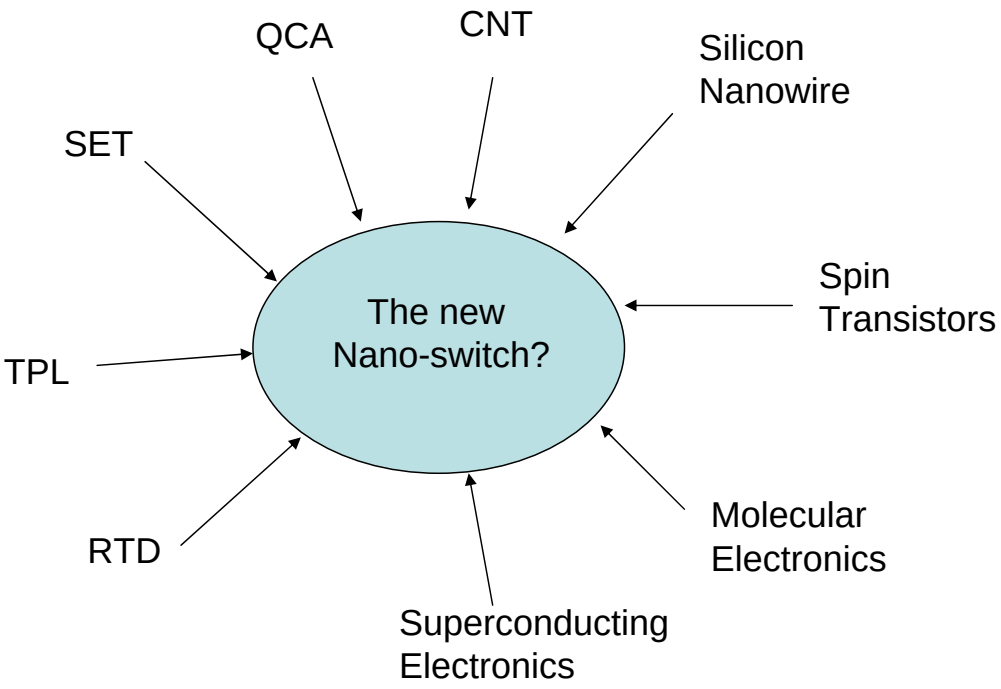



Figure 1.1. Candidates for the new nano-switch

research groups all around the world to keep themselves updated about the current level of research in several technologies.

The table shown in Fig 1.2. shows the results of the critical review assessment of emerging logic technologies highlighted in [6]. It is clear that a number of devices show a great promise for future research. Each of them can be considered novel and some even revolutionary. Some technologies offer tremendous scope for computation with high packing densities, while others offer extremely low power dissipation. At present it is required to continue research for devices that will be most suited [20] to support the ever growing computation needs by offering small sizes and high packing densities and at the same time providing tremendous saving in power dissipation. This will eliminate the bottleneck that exists in the scaling of CMOS devices.

Most of the proposed novel technologies discussed above have device sizes comparable to atomic and molecular scale. At these levels the quantum mechanical effects play a dominant role in device performance and induce uncertainty. Quantum-dot Cellular Automata (QCA) is one such emerging nanotechnology that offers a revolutionary approach to computing at nano-level. QCA technology tries to exploit the inevitable nano-level issues, such as device to device interaction, to perform computing. In the current technologies this device to device interaction at nano-level is one of the biggest roadblocks in further scaling of CMOS devices. Other advantages of QCA include: the lack of interconnects, potential for implementation in metal, and using molecules. Since QCA concept does not involve transfer of electrons, it has a potential for extremely low-power computing, even below the traditional $k_BT$ [21]. Magnetic and molecular implementations of QCA have a potential for room temperature operation.

**Table 1. Emerging Research Logic Devices—Projected Parameters.**

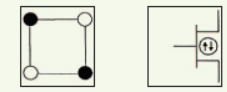
| Availability Sequence | 1 | 2 | 2–3 | 2–3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|---|
| Device |  |  |  |  |  |  |  |
| | FET [2] | RSFQ [3–5] | 1-D structures | Resonant Tunneling Devices | SET [30,31] | Molecular | QCA [39,40,49] | Spin transistor |
| Types | • Si CMOS | • JJ | • CNT FET<br>• NW FET<br>• NW hetero-structures<br>• Crossbar nanostructure | • RTD-FET<br>• RTT | • SET | • 2-terminal<br>• 3-terminal FET<br>• 3-terminal bipolar transistor<br>• NEMS<br>• Molecular QCA | • E: QCA<br>• M: QCA | • Spin FET (SFET)<br>• Spin-valve transistor (SVT) |
| Supported Architectures | • Conventional | • Pulse | • Conventional<br>• Cross-bar | • Conventional<br>• CNN | • CNN | • Memory-based<br>• QCA | • QCA | • Quantum<br>• Programmable logic |
| Cell Size (spatial pitch) | 150 nm* | 0.3 $\mu$m | 150 nm* | 150 nm* | 40 nm | Not known | 60 nm | 150 nm* |
| Density (device/cm$^2$) | 4.5E9 | 1E6 | 4.5E9 | 4.5E9 | 6E10 | 1E12 | 3E10 | 4.5E9 |
| Switch Speed | 9 THz | 1.2 THz | Not known | 1 THz [26] | 1 GHz | Not known | 30 MHz | 700 GHz |
| Circuit Speed | 53 GHz | 250–800 GHz | 53 GHz | 53 GHz | 1 GHz | <1 MHz (NEMS) | 1 MHz | 53 GHz |
| Switching Energy, J*** | $3 \times 10^{-18}$ | $2 \times 10^{-19}$ [Nb] {$> 1.4 \times 10^{-17}$}** | $3 \times 10^{-18}$ | $> 3 \times 10^{-18}$ | $1 \times 10^{-18}$ | Not known {$> 1.5 \times 10^{-17}$}** | $E$ :> $1 \times 10^{-18}$ [48]<br>M: $10^{-17}$ [49] | $3 \times 10^{-18}$ |
| Binary Throughput, GBit/ns/cm$^2$ | 238 | 0.4 | 238* | 238* | 10 | N/A | 0.06 | 238* |
| Gain | | | Must be $\gg 1$ for all devices. See Table 2 for experimental values | | | | | |
| Operational Temperature | RT | • 4 K (Nb)<br>• 77 K (HTS)<br>• 20 K($MgB_2$) | RT | RT | 20 K | RT | E: QCA Cryogenic<br>M: QCA RT | • Cryogenic (SFET)<br>• RT (SVT) |
| CD Tolerance | Critical | Not critical | Not critical | Very critical | Very critical | Not critical | Very critical<br>< 2% (M: QCA) | Critical |
| Materials System | Si | Nb<br>HTS | CNT<br>Si<br>III–V | III–V<br>Si-Ge | III–V<br>Si | Organic molecules | $Al/Al_2O_3$ (E: QCA) | • III–V (SFET)<br>• Si/FM (SVT) |
| Advantages | | • Very high circuit speed | | • Density (smaller cell size) | | • Identity of individual switches on sub-nm level<br>• Potential solution to interconnect problem | • Morphological simplicity | |
| Challenges | | • Cryogenic operations | | • Stand-by power<br>• Process integration | • Cryogenic operations | | | • Low spin injection efficiency<br>• Short coherence time |

Figure 1.2. Performance Evaluation for Emerging Logic Device Technologies. Image from [6]

## 1.2 Novelty of this Work

The underlying uncertainty in nanoscale device operation makes a case for probabilistic modeling of these technologies. In this work we develop a fast, Bayesian probabilistic computing model [22, 23] that exploits the induced causality of a clocked QCA circuit to arrive at a model with the minimum possible complexity. The probabilities directly model the quantum-mechanical steady-state probabilities (density matrix) or equivalently, the cell polarizations. The attractive feature of this model is that not only does it model the strong dependencies among the cells, but it can be used to compute the steady state cell polarizations, without iterations or the need for temporal simulation of quantum mechanical equations. The impact of our proposed modeling is that it is based on density matrix-based quantum modeling, takes into account dependency patterns induced by clocking, and is non-iterative. It allows for quick estimation and comparison of quantum-mechanical quantities for a QCA circuit, such as QCA-state occupancy probabilities or polarizations at any cell, their dependence on temperature, or any parameter that depends on them. This will enable one to quickly compare, contrast and fine tune clocked QCA circuits designs, before performing costly full quantum-mechanical simulation of the temporal dynamics. In [24, 25], it was shown that layout-level QCA cell probabilities can be modeled using Bayesian probabilistic networks.

In other words, we make use of a fast Bayesian computing model in which each QCA cell is defined by the quantum mechanical probabilities associated with the cell and its neighbors and the causality of the design is derived from the direction of propagation of clock signal. This probabilistic model has been shown to accurately capture the device characteristics and provide results that are orders of magnitude faster than the traditional methods involving time consuming quantum mechanical simulations. The research presented in this can be broadly categorized in the following areas:

- We use the Bayesian probabilistic model to estimate power dissipated in a QCA circuit during a non adiabatic switching event. To the best of our knowledge, this work is the first work that provides a realistic estimate of power dissipation using a non-adiabatic clocking scheme. We have termed this power dissipation as worst case power.

- The hierarchical circuit design scheme presented in this work makes use of probabilistic macromodels to design a QCA circuit. This not only reduces the complexity of circuit design by orders of magnitude, it has shown to be much more time efficient with results comparable to the layout level design. To the best of our knowledge, this is the first work in QCA that is used to isolate weak spots in a design at early on in a design process. It can also be used to perform design space exploration to compare two functionally equivalent circuits without having to design it at layout level.

- Device parameter variation to perform tradeoff studies have been the hallmark of research in CMOS and other technologies. It is natural to perform such studies to evaluate the optimum design parameters for a QCA circuit. In this work we undertake one such study in QCA design by varying the maximum kink energy of a QCA design.

## 1.3 Contribution of this Dissertation

In this section we provide a more detailed description of the novel contributions outlined in the previous section. As a developing technology, there are a number of research areas in QCA. We targetted the following three areas in this work.

### 1.3.1 Power Dissipation Model

Since QCA is a field-coupled computing paradigm, states of a cell change due to mutual interactions of either electrostatic or magnetic fields. Due to their small sizes, power is an important design parameter. We derive an upper bound for power loss to estimate power dissipated in large QCA circuits. We categorize power loss in clocked QCA circuits into two well known groups: switching power and leakage power. Leakage power loss is independent of input states and occurs when the clock energy is raised or lowered to depolarize or polarize a cell. Switching power is dependent on input combinations and occurs when the cell actually changes state. Total power loss can be made very small by controlling the rate of change of the clock, i.e. adiabatic clocking. Our model provides a realistic estimate of power loss in a QCA circuit under non-adiabatic clocking scheme. We derive expressions for upper bounds of switching and leakage power that are easy to compute. Upper bounds obviously are pessimistic estimates, but are necessary to design robust circuits, leaving room for manufacturing variability. Given that thermal issues are critical to QCA designs, we show how our model can be valuable for QCA design automation in multiple ways. It can be used to quickly locate potential thermal hot spots in a QCA circuit. The model can also be used to correlate power loss with different input vector switching; power loss is dependent on the input vector. We can study the trade-off between switching and leakage power in QCA circuits. And, we can use the model to vet different designs of the same logic, which we demonstrate for the full adder.

### 1.3.2 Hierarchical Circuit Design

To advance design with QCA, it is necessary to look beyond the layout level. Hierarchical design at multiple levels of abstraction, such as architectural, circuit, layout, and device levels, has been a successful paradigm for the design of complex CMOS circuits. It

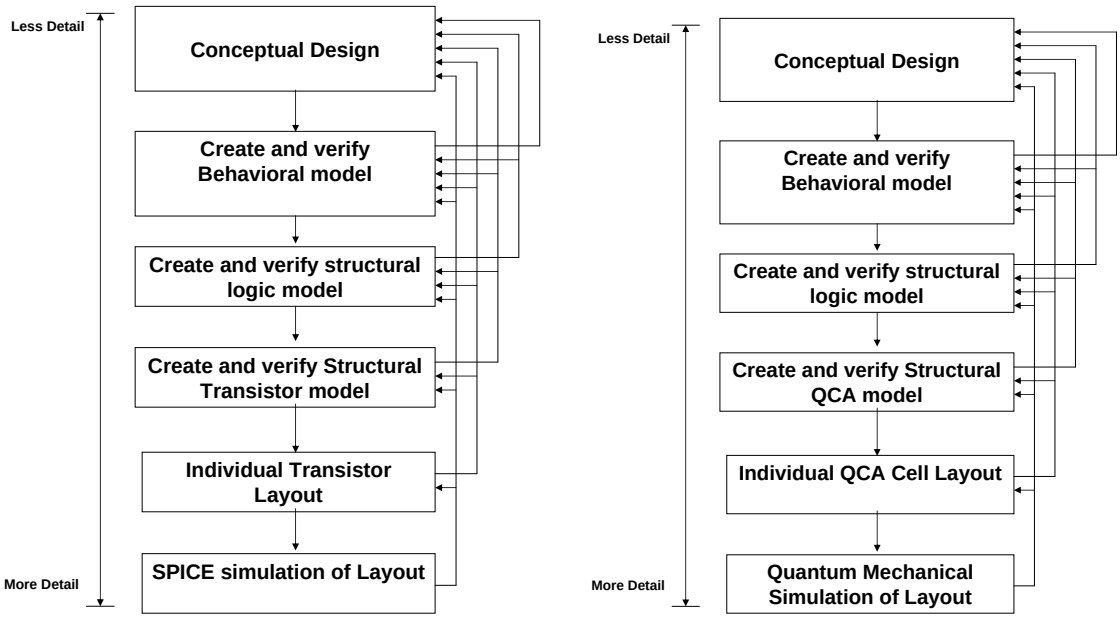



Figure 1.3. Parallel between design methodologies for (a) CMOS and that proposed for (b) QCA (Henderson et.al.[26]).

is only natural to seek to build a similar design structure for emerging technology. Henderson et al. [26] proposed a hierarchical CMOS-like top-down approach for QCA blocks that are analyzed with respect to the output logic states; this is somewhat similar to functional logic verification performed in CMOS (Fig 1.3.). We also advocate building a hierarchical design methodology for QCA circuits. However, such a hierarchy should be built based on not just the functionality of the circuit, but it should also allow the abstraction of important nano-device parameters [27, 28].

Recognizing that the basic operation of QCA is probabilistic in nature, we propose probabilistic macromodels for standard QCA circuit elements based on conditional probability characterization, defined over the output states given the input states. Any circuit model is constructed by chaining together the individual logic element macromodels, forming a Bayesian network, defining a joint probability distribution over the whole circuit.

We demonstrate three uses for these macromodel based circuits. First, the probabilistic macromodels allow us to model the logical function of QCA circuits at an abstract level; the'circuit-level' above the current practice of layout level in a time and space efficient manner. We show that the circuit level model is orders of magnitude faster and requires less space than layout level models, making the design and testing of large QCA circuits efficient and relegating the costly full quantum-mechanical simulation of the temporal dynamics to a later stage in the design process. Second, the probabilistic macromodels abstract crucial device level characteristics such as polarization and low-energy error state configurations at the circuit level. We demonstrate how this macromodel based circuit level representation can be used to infer the ground state probabilities, i.e. cell polarizations, a crucial QCA parameter. This allows us to study the thermal behavior of QCA circuits at a higher level of abstraction. Third, we demonstrate the use of these macromodels for error analysis. We show that that low-energy state configuration of the macromodel circuit matches those of the layout level, thus allowing us to isolate weak points in circuits design at the circuit level itself.

### 1.3.3 Study of Kink Energy Variation in QCA Design

While there have been experimental studies related to defect and fault talerance in QCA [29, 30, 31], not much work has been done to study the effects of variation device parameters on error and power in QCA design. Similar studies of his kind have been the hallmark of CMOS research over the years that contributed significantly in the development of CMOS technology. It is natural to perform such a study with respect to parameter variations in QCA. We perform a study of error and power dissipation in a clocked QCA design by varying one of the most crucial parameter in QCA design; the kink energy. Kink energy is the energy cost of keeping two adjacent cells in opposite polarization and varies with the size of a QCA cell and the grid spacing. We analyze the effects of kink energy

with a design perspective to help designers and fabrication scientists to choose the most optimum size of QCA cell and spacing between adjacent QCA cells.

## 1.4 Organization

This dissertation is organized as follows: Chapter 2 provides an overview of QCA technology and the logic logic asscociated with it. It also includes a brief discussion of various types of QCA implementation, currently under research. Chapter 3 describes the probabilistic model of QCA developed in this work. It elaborates the derivation of quantum mechanical probabilities associated with each QCA cell taking into account the dependancy patterns induced by clocking. These probabilities are then used to derive an overall joint probability distribution function of a QCA circuit represented as a Bayesian network. In chapter 4, we use this model to approximate power dissipated in a QCA circuit during a non-adiabatic switching event. In chapter 5, we make use of hierarchical probabilistic macromodeling scheme to model QCA designs at cirsuit level. We show the use of this hierarchical design scheme to isolate weak spots early on in the design process. Finally, in chapter 6, we show a set of studies related to error-power tradeoffs in QCA design. Concluding remarks are listed in chapter 7.

# CHAPTER 2

# QUANTUM-DOT CELLULAR AUTOMATA

The concept of a cellular automaton operating on quantum mechanical principles dates back to Richard Feynman [32], who suggested an initial approach to quantizing a model of cellular automata. Gerhard Grssing and Anton Zeilinger introduced the term ”quantum cellular automata” to refer to a model they defined in 1988 [33] however, their model has very little in common with the concepts developed in quantum computation after David Deutsch’s formal development of that subject in 1989 [34] and so has not been developed significantly as a model of computation.

A proposal for implementing classical cellular automata by systems designed with quantum dots has been proposed under the name ”Quantum Cellular Automata” by Paul Tougaw and Craig Lent, as a replacement for classical computation using CMOS technology [35, 36]. In order to better differentiate between this proposal and models of cellular automata which perform quantum computation, many authors working on this subject now refer to this as a Quantum-dot Cellular Automata.

QCA offers a revolutionary approach to computing at nano-level [37, 38]. It tries to exploit, rather than treat as nuisance properties, the inevitable nano-level issues, such as device to device interaction, to perform computing. Other advantages include the lack of interconnects, potential for implementation in metal [39], and using molecules [40, 41]. Magnetic and molecular implementationsof QCA have potential for room temperature operations.

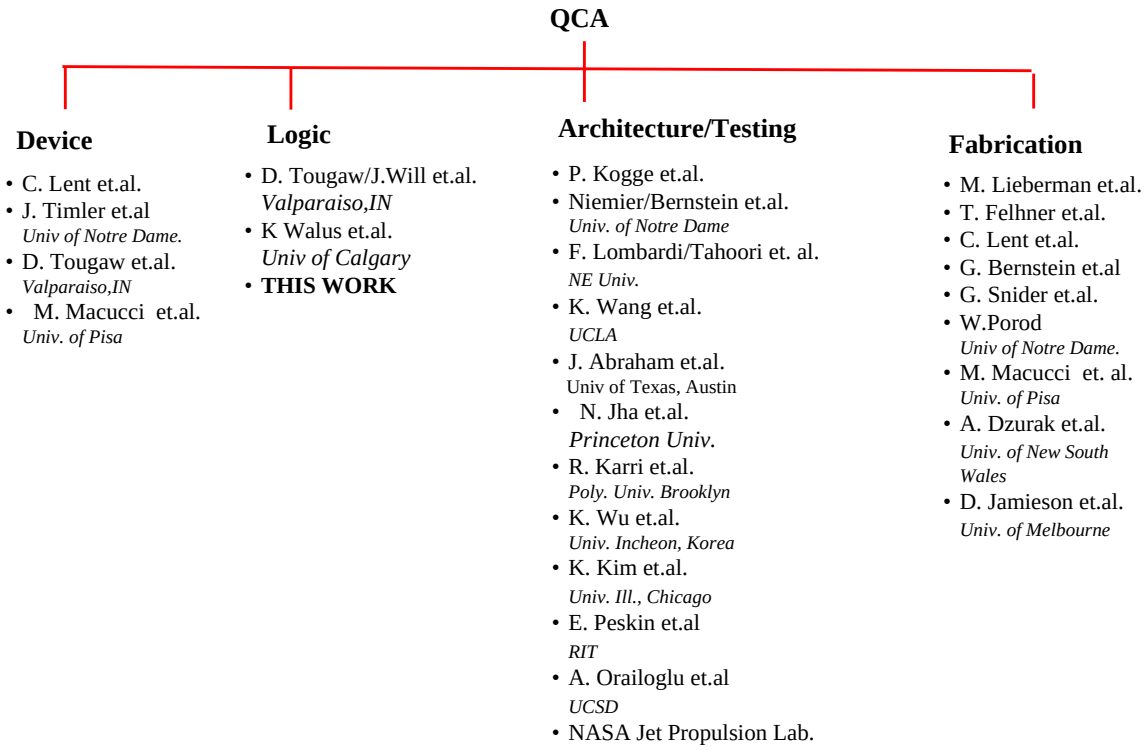



Figure 2.1. Various Groups involved in different areas of QCA research

There are a number of research groups in leading research labs around the world working on QCA. The research group at University of Notredame has been spearheading QCA research for more than a decade. Another group credited with the advancement of QCA research is from University of Pisa, Italy. This group lead by Dr. M. Macucci conducted a investigative research in QCA involving several institutions all over the world under the QUADRANT project. Fig 2.1. shows some of the leading research groups currently involved in different areas of QCA research. As we can see from the figure, most of the research groups are either involved in QCA testing and other architectural issues or in the fabrication of QCA. At the logic level, QCA research received a great boost from the work done at the University of Calgary, under Dr. Konrad Walus. This group introduced the first ever simulator known as QCADesigner [42]. Even today QCADesigner is amongst the leading QCA design and simulation tool used all over the world.

## 2.1 QCA Basics

In a QCA Cell, two electrons occupy diagonally opposite dots in the cell due to mutual repulsion of like charges. A simple unpolarized QCA cell consists of four quantum dots arranged in a square, shown in Fig 2.2.. Dots are simply places where a charge can be localized. There are two extra electrons in the cell that are free to move between the four dots. Tunneling in or out of a cell is suppressed. The numbering of the dots in the cell goes clockwise starting from the dot on the top right. A polarization P in a cell, which measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4} \tag{2.1}$$

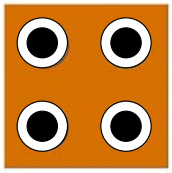



Figure 2.2. An simple 4-dot unpolarized QCA cell

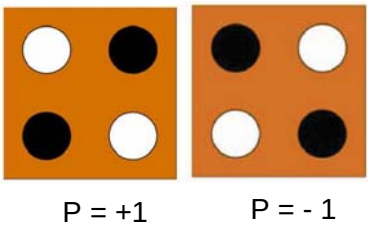



Figure 2.3. Two polarized states of a 4-dot QCA cell

Where $\rho_i$ is the electronic charge in each dot of a four dot QCA cell. Once polarized, a QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. Because of coulumbic repulision, the two most likely polarization states of QCA can be denoted as P = +1 and P = -1 as shown in Fig 2.3. The two states depicted here are called ”most likely” and not the only two polarization states is because of the small (almost negligible) likelihood of existance of an erroneous state.

In QCA architecture information is transferred between neighboring cells by mutual interaction from cell to cell. Hence, if we change the polarization of the driver cell (left most cell also know as input cell), first its nearest neighbor changes its polarization, then the next neighbor and so on. Fig 2.4. depicts the transfer of polarization between neighboring QCA cells. When the driver cell (input) is P = -1 (or P = +1), a linear transfer of information amongst its neighboring cells leads to all of them being polarized to P=-1 (or P = +1).

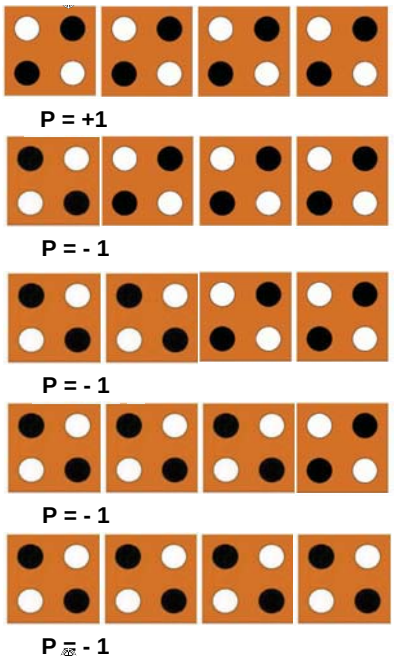



Figure 2.4. Transfer of polarization between adjacent QCA cells when the polarization of the driver cell is changed from P = +1 to P = -1

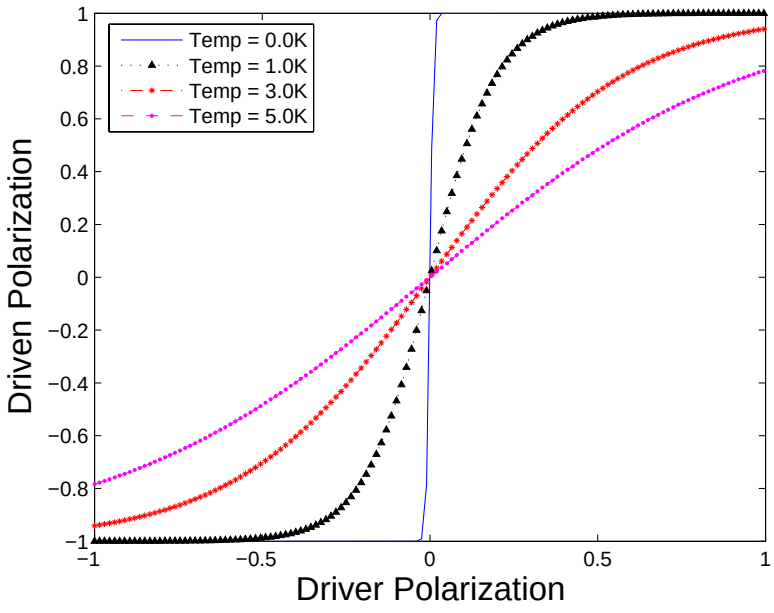



Figure 2.5. Temperature dependence on the polarization of a QCA cell with respect to the change in poalization of the driver cell.

As we can see, a change in polarization of the driver cell prompts all the neighboring cells to change polarization in order to attain the most stable configuration. The above example shows how information can be transferred in a linear fashion over a ”line” of QCA cells. Such a line of cells is used as interconnects between various QCA logic components that we will see in the following section. The speed of change in polarization of a QCA cell depends on a number of factors such as temperature, kink energy, clock energy and the quantum relaxation time. Fig 2.5. shows the thermal dependance of the polarization of a QCA cell with respect to the polarization of the driver cell.

## 2.2 Physics of QCA Device Operation

In order to understand the operation of a simple 4-dot QCA cell we first study the motion of an electron in an infinite potential well. The walls of this potential well prevent electron to tunnel between adjacent dots. Electrons in an infinite potential well exist as a wave function $\Psi(x,y,z)$ that gives us the probability of finding an electron within that potential well. This probability is proportional to $|\Psi(x,y,z)|^2$. Solution to the Schrodinger's wave equation for a free electron (V=0) is given by:

$$\frac{d^2\Psi}{dx} + \frac{2m}{\hbar}(E-V)\Psi = 0 \tag{2.2}$$

Where V is the potential acting on the paerticle, E is the energy of the particle and m is the mass. Taking V=0 for free electron we get:

$$\frac{d^2\Psi}{dx} + \frac{2m}{\hbar}(E)\Psi = 0 \tag{2.3}$$

Using $k^2 = 2m/\hbar^2$ this reduces to

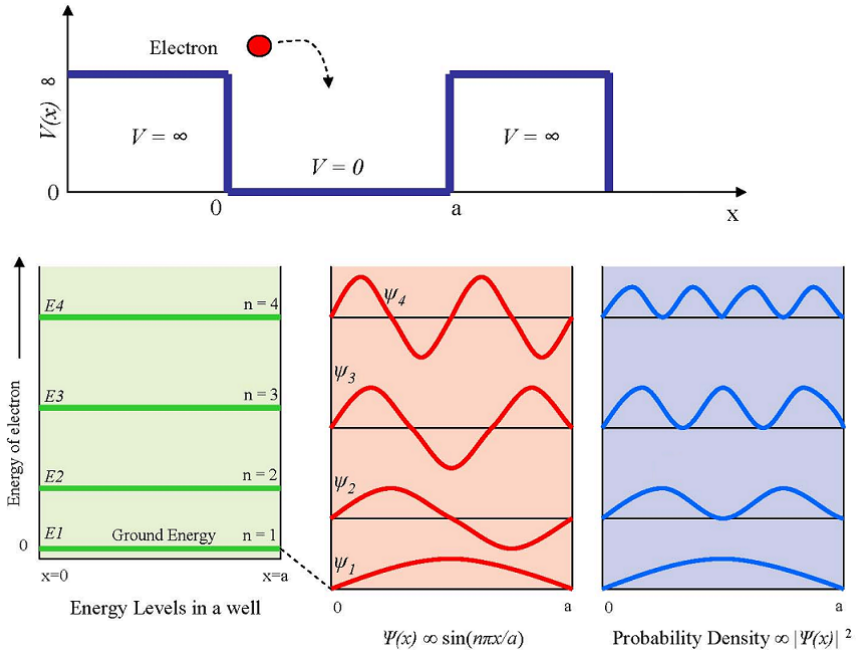



Figure 2.6. The various quantized energy states of an electron in a one dimensional infinite potential well. For each quantized state the possible wavefunctions and probability distributions for the electron are shown. Image redrawn from Principles of Electronic Materials and Devices [43].

$$\frac{d^2\Psi}{dx} + k^2\Psi = 0 \tag{2.4}$$

Solution of Schrodinger's equation for this wave function is a sin/cos function and it also gives the value of the energy of an electron within a potential well.The electron can only have certain discrete energies ($E_n$) matching the allowed wave functions. A lower (higher) energy electron will have a smaller (larger) value of $k$ (wavevector) and a larger (smaller) wavelength.

Since the boundary conditions demand the wavefunction to be zero at the walls of the well, the wavevector can only take discrete quantities and hence the electron can only exist in quantized energy levels. The spacing between adjacent energy levels depends on the

width of the potential well. If we consider the height of the potential well as finite, there is a possibility of electrons tunneling out of the potential well. Fig 2.7. shows an example of an electron tunneling across a finite potential well. The potential energy (PE) of point A is less than that of point D. Hence a car released from point A can at most make it to C but not E. When the car is at the bottom of the hill its energy is totally Kinetic Energy (KE). The energy barrier (between C and D) prevents the car from making it to E. In quantum theory, on the other hand, there is a chance that the car could tunnel through (leak) the energy barrier between C and E and emerge on the other side of the hill at E. Fig 2.7.(b) shows the the wavefunction of the electron when it is incident on a PE barrier ($V_o$). The interference of the incident and reflected waves give $y_I(x)$. There is no reflected wave in region III. In region II the wavefunction decays with $x$ because $E < V_o$.

Solving the Schrodinger equation for the finite barrier region (II) yields an exponential decay function. This is the main difference to the outer regions of the infinite well, where the wavefunction must be zero. Solutions for I and III are the same as for the infinite potential well. However, boundary conditions now demand that the wave function match the exponential function in region II, causing non-zero amplitude in region III. Since the probability of finding an electron is proportional to the square of the amplitude, therefore, there is a non-zero probability to find the electron on the outside, i.e. it can escape from region I.

Taking this into account we now look at a simple QCA cell with two electrons placed in neighboring potential wells (called dots). Incase of an infinite potential barrier between the dots, electrons are not allowed to tunnel within the dots. As the potential barrier decreases, the possibility of an electron to tunnel across the potential barrier increases. When the potential barriers are very low, electrons can tunnel freely across the two quantum dots. In QCA technology, clock energy is provided as a means to lower or raise the tunneling barriers as we will see in Section 2.5. Fig 2.8. shows how the tunneling barriers between

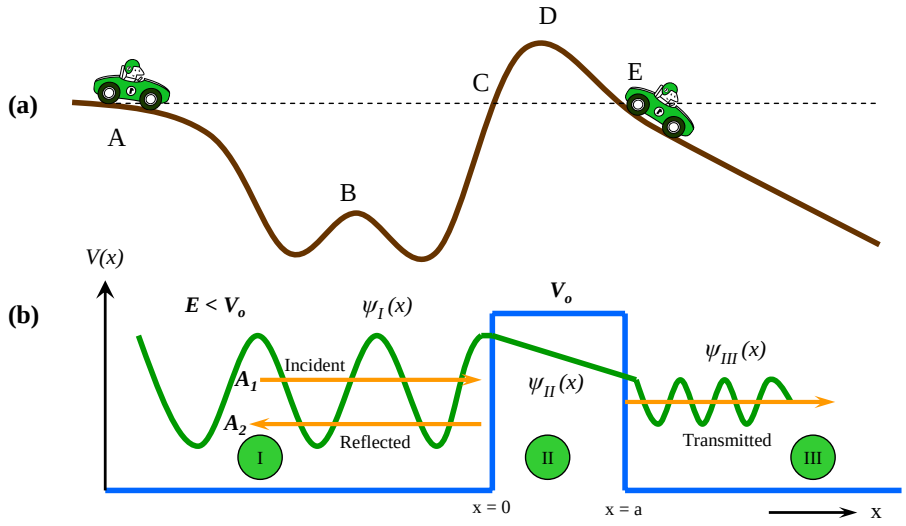



Figure 2.7. An an example of an electron tunneling across a finite potential well. Image redrawn from Principles of Electronic Materials and Devices [43].

two dots are lowered (raised) when the clock energy supplied to the QCA cell is raised (lowered).

The work done in raising and lowering of tunneling barriers controlled by the clock energy can be termed as leakage power dissipation as this will take place even if the QCA cell does not switch state. In a similar way a clock controls the tunneling barriers in a 4-dot QCA cell used in this work.

Since in practice it is not possible to implement an infinite potential well to prevent the electrons from tunneling across, there is always a finite possibility of some electronic charge escaping the QCA cell over a long period of time. However, in this work we have neglected any loss of charge. Electrons in higher energy states within a potential well are more prone to tunnel across if the tunneling potential is of finite height. Thermal errors are caused when the electrons to settle in higher energy orbits and are more likely to tunnel across the barriers as compared to when they are in ground state. We will see in later chapters how the output node polarization probability falls with the rise in temperature.

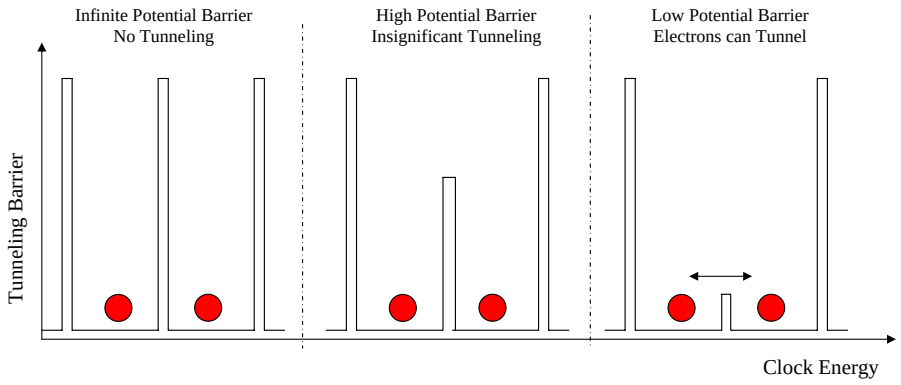



Figure 2.8. Controlling the tunneling barrier by variation of clock energy. As the clock energy supplied to a QCA cell increases, the tunneling barriers lower, making it possible for electron to tunnel across tot he other side.

## 2.3 Implementation of a QCA Cell

The basic element for QCA computation is a bistable cell capable of interacting with its local neighbors. The cell is not required to remain quantum-mechanically coherent at all times; therefore, many non-quantum-mechanical implementations of QCA have emerged. Generally speaking, there are four different classes of QCA implementations: Metal-Island, Semiconductor, Molecular and Magnetic. In this section, a brief description of each implementation is provided with its advantages and disadvantages.

### 2.3.1 Metal Island

The Metal-Island implementation [44, 39, 45] was the first fabrication technology created to demonstrate the concept of QCA. It was not originally intended to compete with current technology in the sense of speed and practicality, as its structural properties are not suitable for scalable designs. The method consists of building quantum dots using aluminum islands. Earlier experiments were implemented with metal islands as big as 1

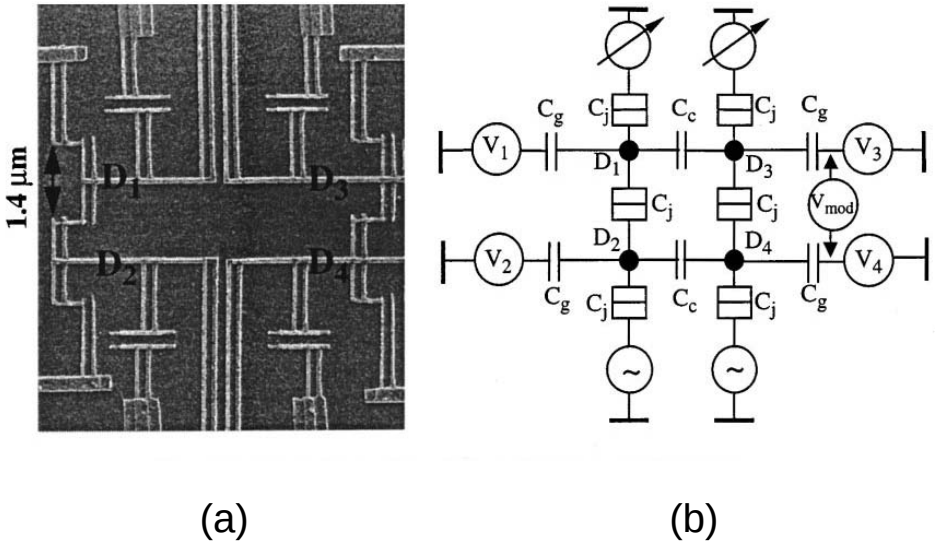



Figure 2.9. (a) SEM image of a Metallic Dot QCA and (b) Schematic diagram. Image from: Orlov et.al. [44]

micrometer in dimension. Because of the relatively large-sized islands, Metal-Island devices had to be kept at extremely low temperatures for quantum effects (electron switching) to be observable. Again, this method only served as means to prove that the concept is attainable in practice [46, 47]. A SPICE model development methodology for QCA cells was proposed in [48].

### 2.3.2 Semiconductor

Semiconductor (or solid state) QCA implementations [50] could potentially be used to implement QCA devices with the same highly advanced semiconductor fabrication processes used to implement CMOS devices [51]. Semiconductor quantum dots are nanostructures created from standard semiconductive materials such as InAs/GaAs [52] and GaAs/AlGaAs [53, 54]. These structures can be modeled as 3-dimensional quantum wells. As a result, they exhibit energy quantization effects even at distances several hundred times

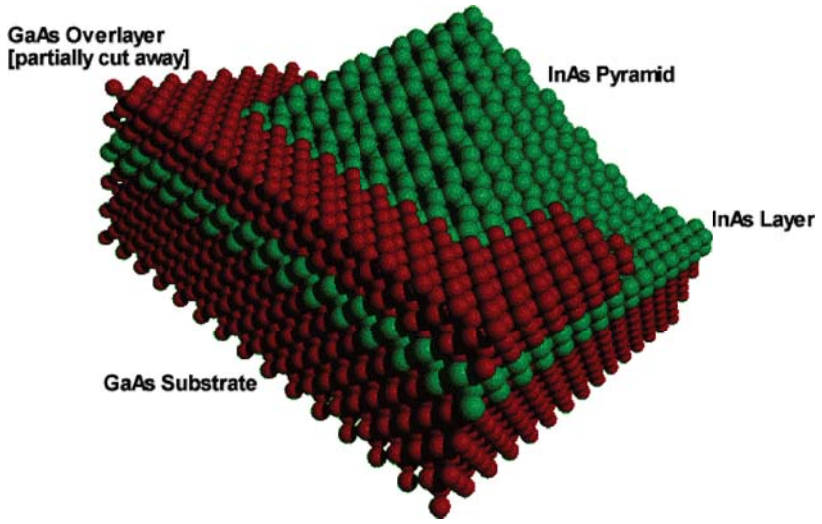



Figure 2.10. Example quantum dot pyramid created with InAs/GaAs. Image from: University of Newcastle: Condensed Matter Group [49]

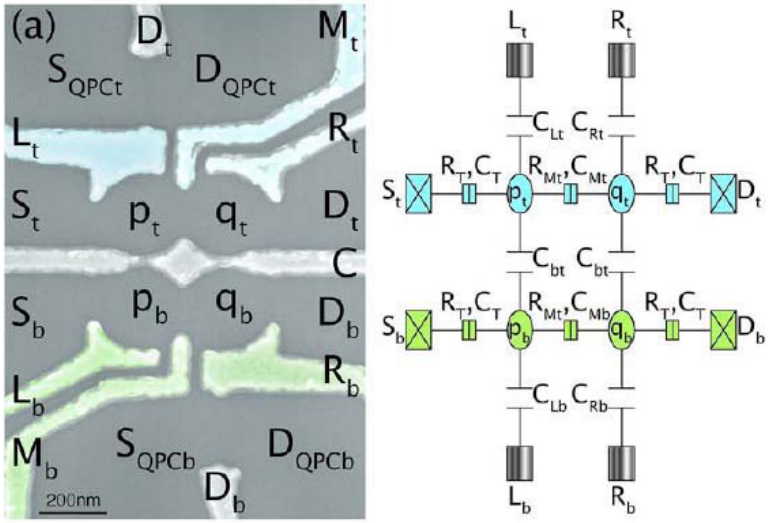
larger than the material system lattice constant. Cell polarization is encoded as charge position, and quantum-dot interactions rely on electrostatic coupling [55]. Today, most QCA prototyping experiments are done using this implementation technology [56].

Advantages:

- Easier to integrate in the fabrication process because of the success of semiconductors in microelectronics for which many tools and techniques have been developed.
- Easier to use existing facilities and methods to create a viable QCA solution.

Disadvantages:

- Current semiconductor processes have not yet reached a point where mass production of devices with such small features( 20 nanometers) is possible.
- Serial lithographic methods, however, make QCA solid state implementation achievable, but by no means practical. Serial lithography is slow, expensive and unsuitable for mass-production of solid-state QCA devices.




(a) (b)

Figure 2.11. (a) Electron micrograph of a GaAs/AlGaAs QCA cell. (b) Simplified circuit equivalent of the four-dot cell. Image from: Perez-Martinez et.al. [53]

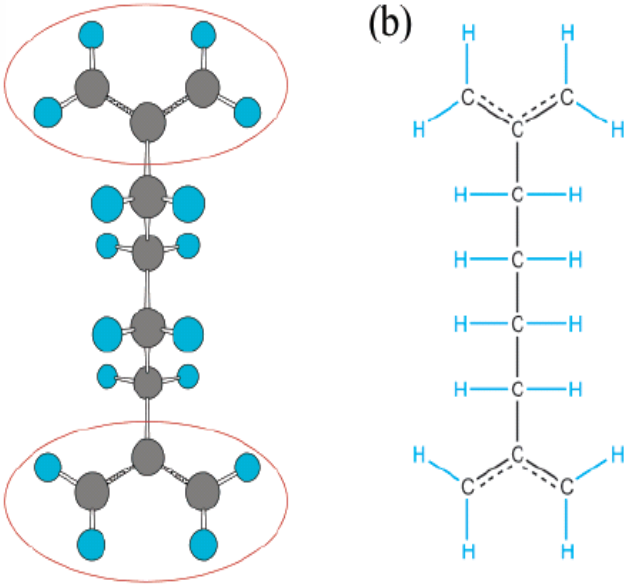



Figure 2.12. Two views of Molecule 1 as a QCA cell. Image from: Lent et.al. [57]

### 2.3.3 Molecular QCA

Molecular QCA [58, 41, 57, 59] concept consists of building QCA devices out of single molecules. Majority of the work so far has been presented by the research group at Notre Dame.

The basic cell for Molecular QCA in [57] consists of a pair of identical molecules (Fig 2.12.). The molecule of our discussion is Molecule 1 which is formally known as 1,4-diallyl butane radical cation. This molecule is comprised of two allyls connected to butyl bridge on one end and two more allyls connected to the same bridge on the other end. This particular molecule is neutral on one end while the other end behaves as a cation.

These molecules have an extra electron or hole that can tunnel from one side of the molecule to the other. By placing an electric field near one side of the molecule on can force the hole to either be attracted or repelled, this can be called the driver cell. It has been calculated that Molecule 1 has nonlinear switching characteristics making it an ideal switch. If the molecules can be placed very close to each other, about 7 angstroms, the electrostatic interactions will cause the holes to be at opposite ends. This allows propagation of the a state to other cells. The Fig 2.13. shows the different possible states the molecule can be in (a) shows a +1 (c) shows a -1 and (b)a non-ideal state that is a unwanted state.

While fabrication methods are currently being researched, no one method has been predominate. Efforts are on to fabricate molecular QCA circuits using self assembly monolayer methods [60, 61, 62, 63]. The molecules themselves are produced by standard chemical procedure [64, 65, 66, 67, 68].

Advantages:

- Room temperature operation
- Ultra small devices: density of device can be very high.
- Fast Switching: device should be able to operate in the Gigahertz range

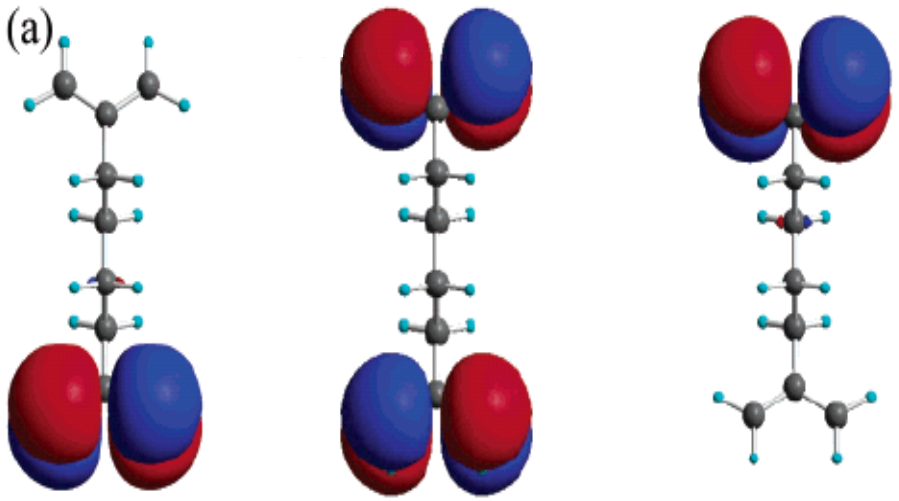
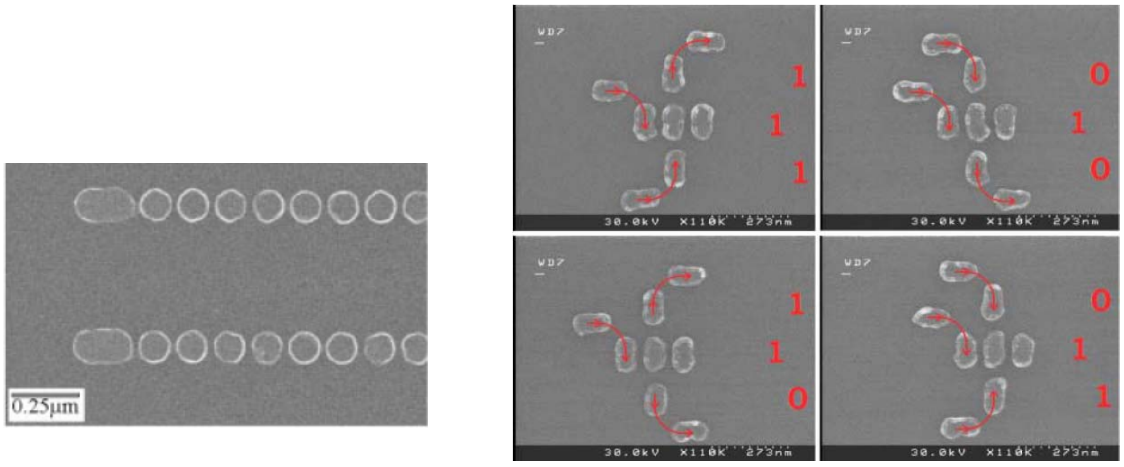



Figure 2.13. Different possible states of Molecule 1 (a) shows a +1 state (b)a non-ideal state that is a unwanted state and (c) shows a -1 state. Image from: Lent et.al. [57]

- Low Power consumption: The only power needed is to drive the input and for some type of clocking mechanism.
- Low Power loss: Calculations state that there should be low power loss due to heat produced from switching.

Disadvantages:

- Single Molecules are in existence and have been produced but the placement of these molecules in a regular pattern or fashion has not been done.
- Because of the size of the of the devices, to drive the input to a certain state and sensing the outputs can be very difficult. One does not want to influence other cells besides the intended driver cell and the output cells.
- Clocking Method: Though theoritical clocking methods have been proposed [69], no practical clocking method has been demonstrated.




(a) (b)

Figure 2.14. (a) SEM image of a room temperature MQCA network shown in (Cowburn et.al. [74]) (b) Majority gates designed for testing all input combinations of the majority-logic operation. The arrows drawn superimposed on the SEM images illustrate the resulting magnetization direction due toa horizontally applied external clock-field (Imre et.al. [79])

### 2.3.4 Magnetic QCA

A basic cell in Magnetic QCA is a nano-magnet [70, 71]. These nano-magnets are arranged in various grid-like fashions to accomplish computing [72]. Cells in Magnetic QCA are enumerated based on their single domain magnetic dipole moments and are inherently energy minimums [73]. There are several popular schemes of Magnetic QCA that have been proposed: Cowburn and Wellands nanodot QCA Automata [74], Parish and Forshaws Bi-stable Magnetic QCA [75, 76], and Csaba et al., Field Couple Nanomagnets [77, 78]. Cowburn and Wellands have fabricated the Magnetic QCA model that has been described here.

A nano-magnet consists of a single circular nanodot. These nanodots were made of a magnetic SuperMalloy (mainly Ni). The nanodots are 110nm in diameter and had a thickness of 10nm. In order to have a single domain in the nanodots it was found that the nanodots must have a size of about 100nm and below. Single domains were important when

analyzing the hysteresis loops and retaining information with no external energy present. The nanodots were fabricated using high resolution electron beam lithography.

The basic cell consists of a single nanodot. These nanodots were place about 20nm apart in a straight line as shown in Fig 2.14.(a) An elongated dot was placed at the beginning of the chain, this was used as the input dot. There was an oscillating field applied to dots which was +25 and -25 Oe. There was also a -10 Oe bias along the chain of dots. For this experiment if the dots were pointing to the right it was a logical 1, to the left was considered a 0. When the inputs where set to 1 a response was found where as when the dots where set to 0 no response was present.

There have been some progress recently in fabricating a majority logic gate using nanomagnets [79]. Fig 2.14.(b) shows the implementation of a majority gate using nanodots by Imre et al. Their approach to MQCA is similar to Cowburn et.al., but they use an additional shape-induced anisotropy component to separate the directions for magnetic information representation and information propagation in the array.

Advantages:

- Room temperature operation: Because Magnetic QCA use magnetostatic forces instead of columbic, this scheme can operate at room temperature
- Less stringent fab requirements than other QCA: Since it is not necessary to have feature sizes like 5-10nm and spacing of 2nm for operation
- High Density when compared to CMOS: Future outlook have been predicted to have device density as high as 250,000 million per squared cm
- Highly researched area: Other devices such as hard drives and memory use magnetism as their primary mechanism.

- Low power loss: Once the input is set the nanodots can settle into a local energy minimum needing no external energy to keep their state.
- Higher thermal robustness than other QCA: Currently other QCA implementations require cryogenic temperatures to operate. This scheme states $40k_BT$ will keep thermal errors below 1 per year.
- 3D Architectures Possible: Since the magnetic forces from the nanodots are in plane it is possible to have stacked multiple planes

Disadvantages:

- Individual sensing of dots: The sensing of states is done by measuring the total resultant magnetic field of the entire wire of dots and not a signal point on the wire.
- Frequency: Estimated speed of operation of magetic devices is lower than current technologies [75]. Even though this is not very fast it would have a nice niche for devices.
- Unknown under the 20nm sizes: Current predictions state that nanodots might become unstable under 20nm.

## 2.4 Logical Devices in QCA

As we know that present day logic architectures are based on Boolean algebra. In order to perform logical operation using QCA, we denote the two polarization states in terms of Boolean logic. We take P = -1 configuration as ”HIGH” and P = +1 configuration as ”LOW”. In Boolean logic the AND gate, the OR gate and Inverter form the most basic logic components. In QCA architecture, the majority gate and inverter form the most basic logic components [80]. There has also been a lot of research recently to present novel logic designs using QCA [81, 82, 83].

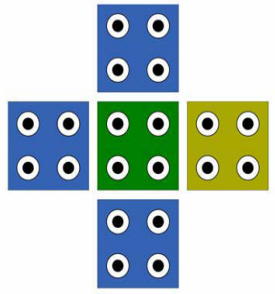


Figure 2.15. A QCA majority gate

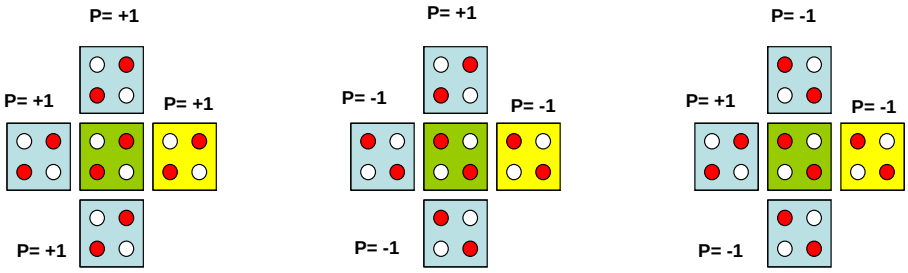



Figure 2.16. QCA majority gate logic with different inputs

A three input majority gate consists of three inputs and one output. The output is said to be HIGH (LOW) if at least two out of the three inputs are HIGH (LOW) and vice versa. Here HIGH (LOW) refers to the polarization state P = +1 (P = -1).

A Majority gate of three inputs A, B and C is denoted as:

Maj(A,B,C) = A.B + B.C + C.A

Fig 2.15. shows a simple three input majority gate in QCA. Different input configurations of a QCA majority gate is shown in Fig 2.16..

A QCA inverter design is shown in Fig 2.17.. The purpose of an inverter is to take one input and produce its inverse. So if the input is HIGH (LOW) the output is LOW (HIGH).

Using majority gates and inverters we can build logic circuits having similar functionality as that of functions implemented using the conventional logic gates (such as AND, OR and NOT). An AND gate and an OR gate can be easily built using a Majority gate by

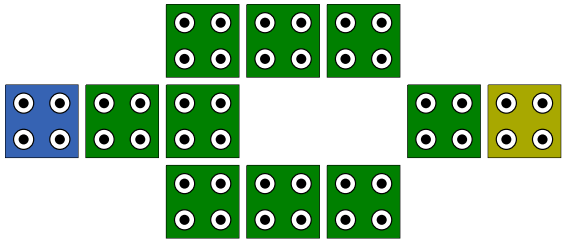


Figure 2.17. A QCA inverter

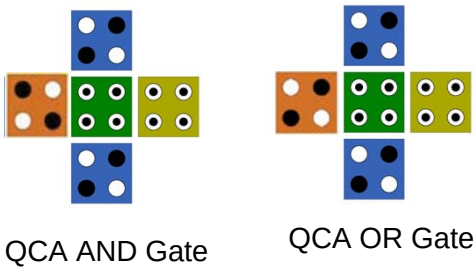



Figure 2.18. AND and OR gate representation of a majority gate by fixing one of the inputs as P=-1 or P=+1 respectively

setting one of its inputs to either P = -1 or P = +1 (LOW or HIGH) respectively. Once we fix the polarization of one of the inputs, the majority gate acts as a simple two input AND gate or an OR gate(Fig 2.18.).

Now that we have shown how we can implement an AND gate, OR gate and an Inverter, we can build any Boolean logic circuit in QCA. We show a small example of a NAND gate in QCA using a AND gate and Inverter in Fig. 2.19.. In fact, it is possible to implement most of the Boolean logic circuits in QCA using only three input majority gates and inverters [84, 85].

There are several synthesis algorithms [86, 87] available to convert a Boolean logic function to a Majority gate logic function. A single-bit adder circuit implemented using only Majority gates and inverters is shown in Fig 2.20..

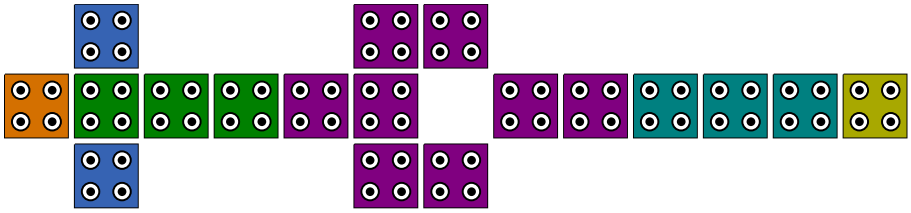


Figure 2.19. QCA NAND gate using an AND gate and an inverter

## 2.5 Clocking in QCA

A QCA cell can only be in one of two states and the conditional change of state in a cell is dictated by the state of its adjacent neighbors. However, a method to control data flow is necessary to define the direction in which state transition occurs in QCA cells. The clocks of a QCA system serve two purposes: providing power to the circuit, and controlling data flow direction. Like stated before, QCA requires very small amounts of power. This is due to the fact that cells do not require external power apart from the clocks. These clocks are areas of conductive material under the QCA lattice, modulating the electron tunneling barriers in the QCA cells above it.

A QCA clock [88] induces four stages in the tunneling barriers of the cells above it. In the first stage, the tunneling barriers start to rise (clock signal goes low). The second stage is reached when the tunneling barriers are high enough to prevent electrons from tunneling. The third stage occurs when the high barrier starts to lower (clock begins to rise again). And finally, in the fourth stage, the tunneling barriers allow electrons to freely tunnel again. In simple words, when the clock signal is high, electrons are free to tunnel. When the clock signal is low, the cell becomes latched. Fig 2.21. shows a clock signal with its four stages.

A typical QCA circuit requires four clocks, each of which is cyclically 90 degrees out of phase with the prior clock as shown in Fig 2.22.. If a vertical wire consisted of say, 8 cells

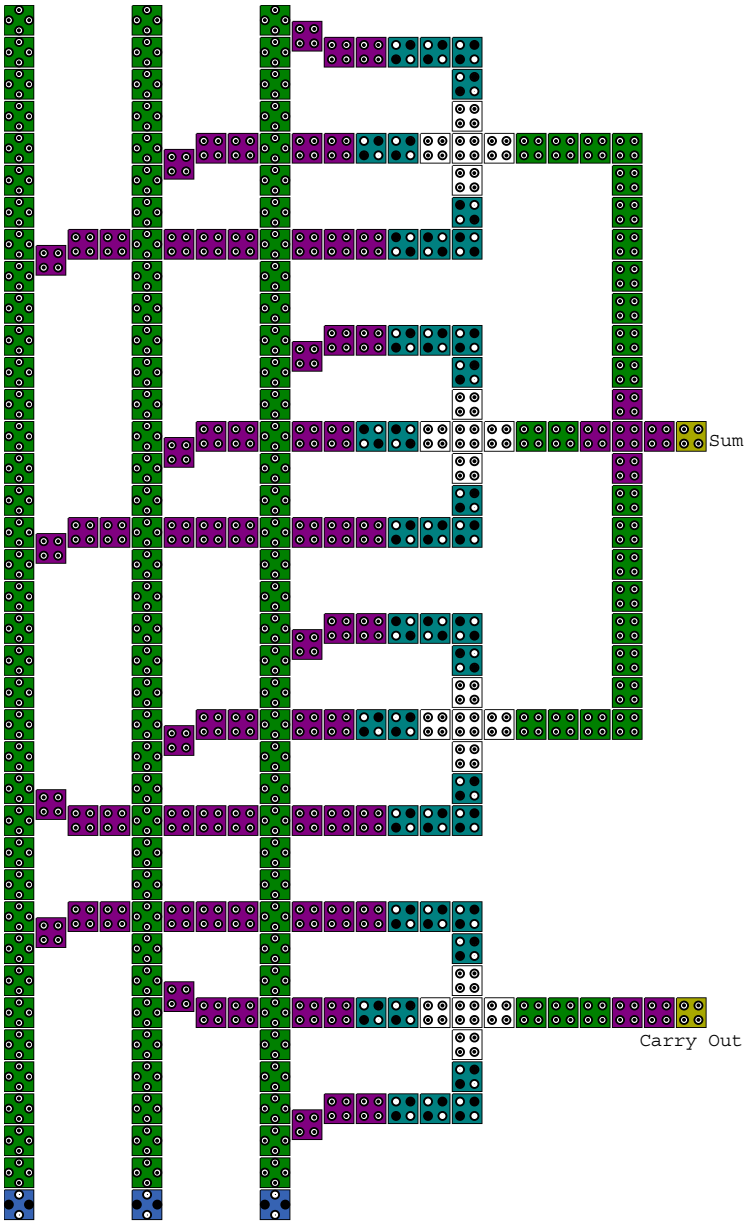



Figure 2.20. A single bit QCA adder design

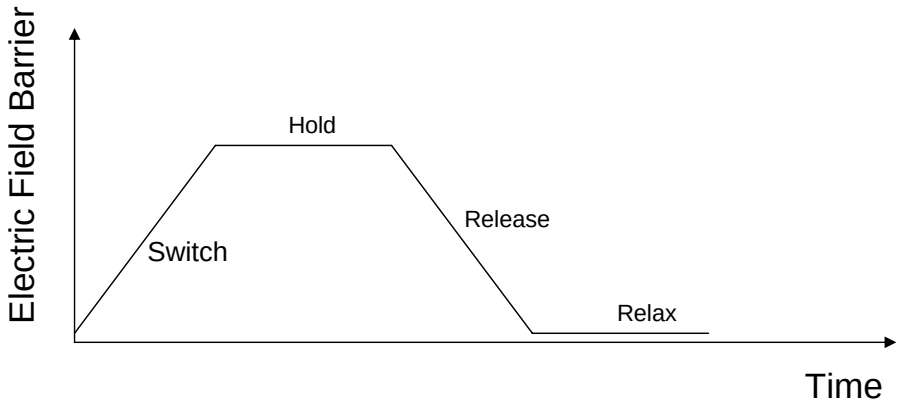



Figure 2.21. Four stages in a QCA clock (1) Tunneling barriers start to rise (2) High tunneling barriers prevent electrons from tunneling (3) Tunneling barriers begin to lower (4) Electrons are free to tunnel.

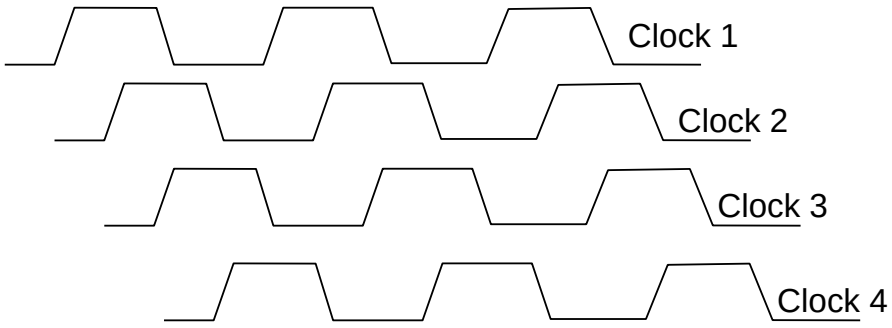



Figure 2.22. Four QCA clocks phase shifted by 90 degrees.

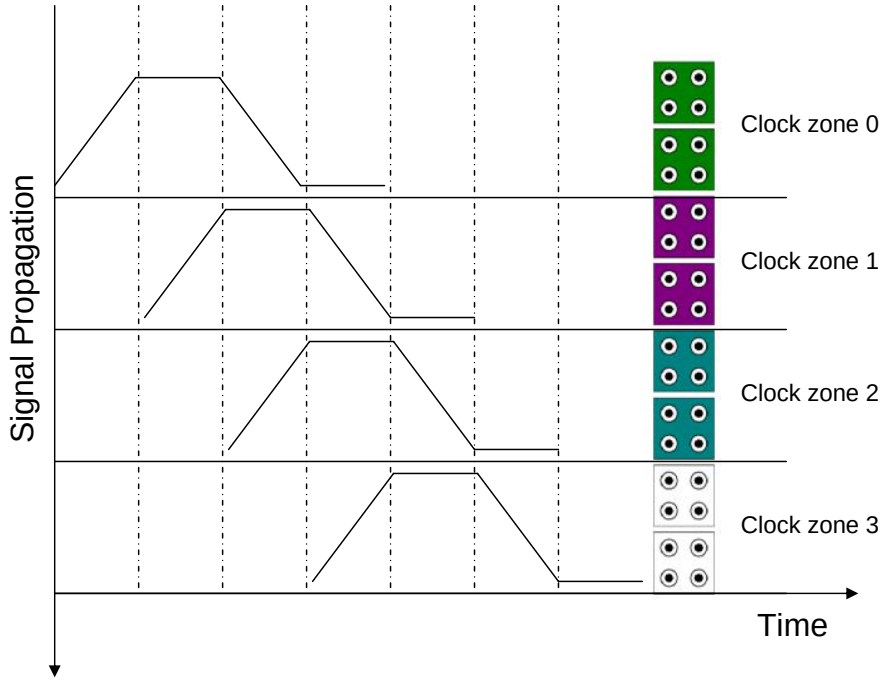



Figure 2.23. Flow of information in QCA line controlled by clock propagation

and each consecutive pair, starting from the top were to be connected to each consecutive clock, data would naturally flow from top to bottom. The first pair of cells will stay latched until the second pair of cells gets latched and so forth. In this way, data flow direction is controllable through clock zones [89]. This process is depicted in Fig 2.23..

In [90], Lent et.al. examine the efficacy of *Landauer-Bennett* clocking approach in molecular QCA circuits. Landauer clocking involves the adiabatic transition of a molecular cell from the null state to an active state carrying data that can result in power dissipation lesss than $k_B T ln(2)$. Landauer showed that for logically reversible computation there is no necessary minimum energy dissipation associated with reading a bit, but rather with erasing information. Bennett extended the Landauer result by showing that in principle any computation could be embedded in a logically reversible operation. This method suggests QCA as

a practical means to implement reversible computing. Bennett clocking scheme can reduce the power dissipated to much less than $k_B T ln(2)$ without changing circuit complexity.

Fig 2.24. shows Landauer and Bennett clocking of QCA circuits. Each figure represents a snapshot in time as the clocking fields move information across the circuit. The left column (L1)-(L5) represents Landauer clocking. A wave of activity sweeps across the circuit as the clocking field causes different cells to switch from null to active. The circuit shown includes a shift register on top and a three-input majority gate on the bottom. The right column (B1)-(B7) represents Bennett clocking for a computational block. Here as the computational edge moves across the circuit intermediate results are held in place. When the computation is complete (B4), the activity sweeps backwards, undoing the effect of the computation. This approach results in minimum energy dissipation.

There have been experimental studies to demonstrate the clocked QCA shift registers [91, 92]. Single walled CNTs have been proposed as a possible mechanism to provide clocking in QCA circuits [93]. Not only does a QCA clock clock provide a means to control data flow direction and power to the circuit, it has been also seen that clock energy also plays a significant role in the overall power dissipated by a circuit. This effect is less prominent if the the clocking scheme is adiabatic [94] however, if a non-adiabatic clocking scheme is applied to the circuit [95, 96], it contributes significantly to the overall power dissipated in the circuit, as we will see in the later part of this dissertation.

## 2.6 QCA Architecture

For any technology, architectural design is one of the most important parameters of its success. Any technology can prove to be reliable and efficient in terms of scaling and power requirements, but it is of little use unless one can implement architectural designs in it. QCA is considered to be one of the most complete emerging technologies when it comes

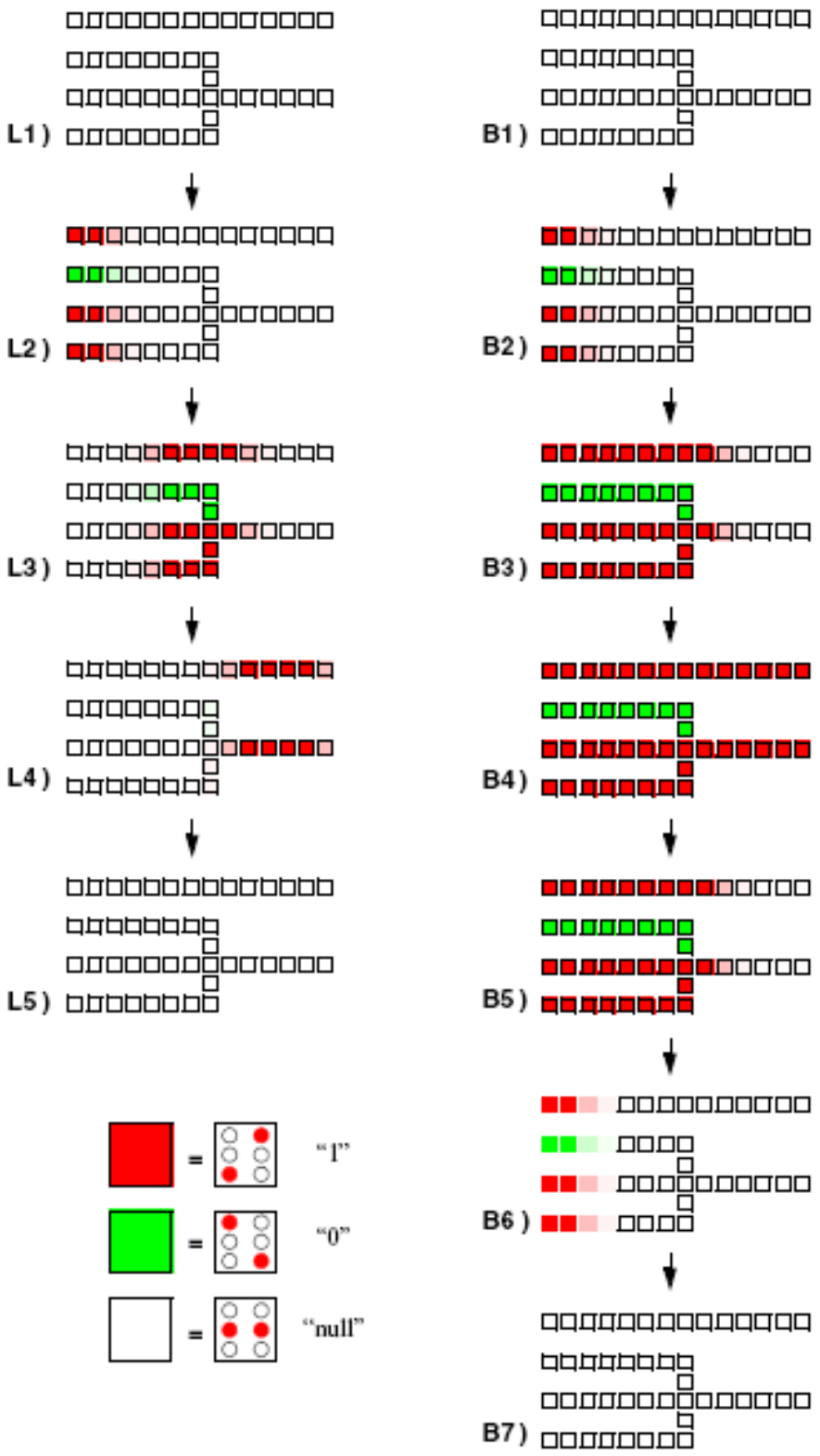



Figure 2.24. Landauer and Bennett clocking of QCA circuits. (Lent et.al. [90])

to architecture. Several novel architectures have been proposed both in logic and memory design. The majority logic design involved in QCA architecture presented an interesting challenge for researchers to design complex architectures [97] that used different logic compared with Boolean logic (NAND/NOR) used in CMOS.

Intitial logic gates and adder designs were proposed by Lent et.al. in [80, 98, 99]. While most of the recent work in QCA architecture has been performed under Dr. Kogge's group at University of Notredame, there are several other groups that have contributed significantly in the development of QCA based designs over the years. A number of combinational [100, 101] and sequential designs [102] have been proposed and simulated. Most prominent logic design that has been implemented in QCA is a single bit adder [103, 104, 105]. Several other complex architectural designs have been proposed in QCA such as a single bit ALU [106] and a simple 12 microprocessor design [107, 108]. Other logical designs proposed in QCA include multiplexers, decoders and shift registers. Many simple and complex QCA architectural designs are presented in later chapters.

QCA relies on novel design concepts such as "memory in motion" and "processing in wire" to implement unique paradigms [109, 110, 111]. Lack of interconnects and potential implementation of logic in wire makes QCA a very attractive technology for memory design [112]. A simple memory element is shown in Fig 2.25. As QCA is implemented on a grid based architecture, some promising FPGA and application specific architectures have also been proposed [113, 114, 115].

A number of groups also work in majority synthesis algorithms [87, 116] that provide a majority logic solution of common Boolean expressions. Once the logical expressions are synthesized they can be used for design circuits in QCA.

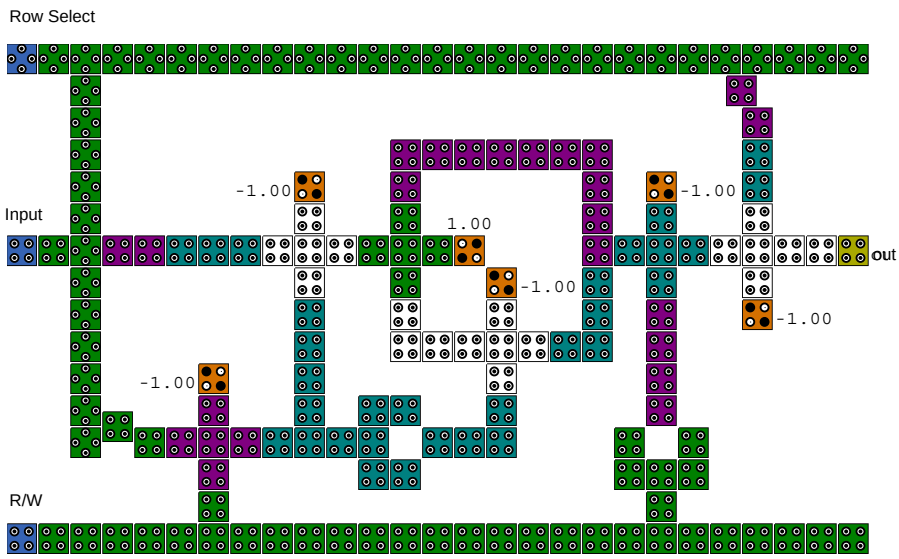



Figure 2.25. A QCA Memory Cell (Walus et.al. [42])

## 2.7 Defect Tolerance

Recently there has been a lot of work done in nano-level issues in QCA design relating to design issues such as cell size, polarization and defect tolerance [117, 118, 119]. Defect tolerance studies are crucial for any nanoscale technology because defects in layout are unavoidable. The QCA approach is inherently robust and can be made even more so by simply using wide (3- or 5-cell) wires to build in redundancy at every stage. Other defect-tolerant strategies in QCA are under investigation.

In [30] presents a study of defect characterization in QCA designs. Effects of defects are investigated at the logic level. Testing of QCA is also compared with testing of conventional CMOS implementations of these logic devices. Fig 2.26. shows the different configurations of a defective majority gate. Another work in [120] explores the use of *enlarged* lines and majority gates to study defects in coplanar crossings in QCA design.

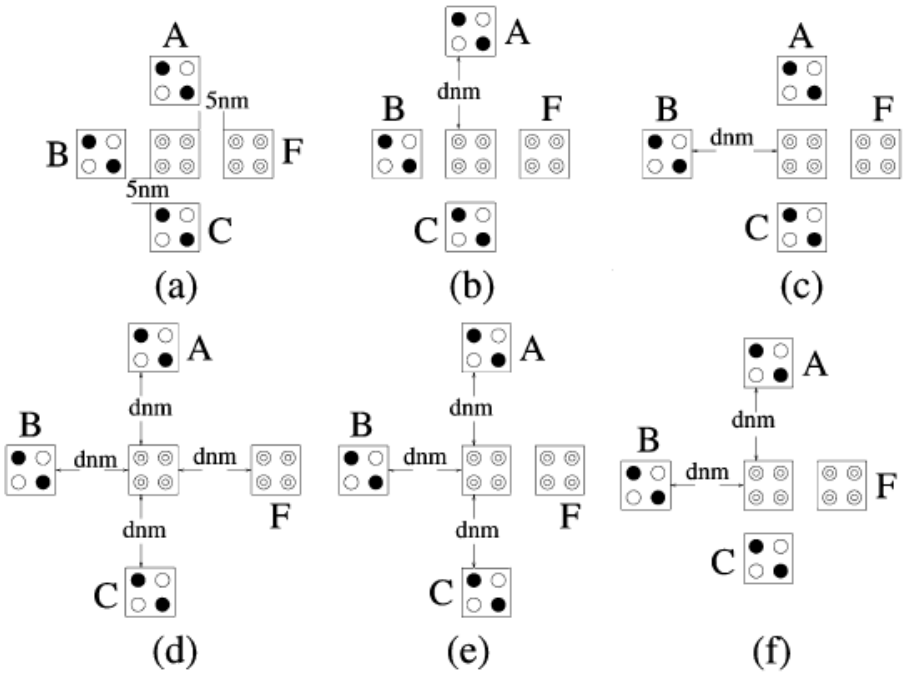



Figure 2.26. Different configurations of displaced QCA cells in a majority gate. Configuration (a) is fault free (Tahoori et.al. [30])

## 2.8 Modeling QCA Designs

There are several approximate simulators available at the layout level, such as the bistable simulation engine and the nonlinear approximation methods. These methods are iterative and do not produce steady state polarization estimates. In other words, they estimate just state assignments and not the probabilities of being in these states. The coherence vector based method does explicitly estimate the polarizations, but it is appropriate when one needs full temporal dynamics simulation (Bloch equation), and hence is extremely slow. Perhaps, the only approach that can estimate polarization for QCA cells, without full quantum-mechanical simulation is the thermodynamic model proposed in [121], but it is based on semi-classical Ising approximation. In the next chapter we demonstrate how we can use a Bayesian probabilistic computing model to exploit the induced causality of clocking in a QCA design to arrive at a model with the minimum possible complexity.

One of the major advantages of QCA logic design is that it is capable of extremely low power computation. Lent et al. proposed a model to estimate power dissipation during quasi-adiabatic switching event in a QCA shift register. Perhaps the most pure power model is the quantum-mechanical model of the temporal dynamics of power derived by Timler and Lent. They identified three components of power: clock power, cell to cell power gain, and power dissipation. While this model gives us physically close estimates, it is computationally expensive to estimate. When designing QCA circuits, we would like estimate power quickly in order to choose among many different alternatives and parameters. The need for full blown quantum-mechanical estimation will be relegated to the very end of the design process. To this end, some studies present lower bounds of power dissipated that are easy to compute. However, from a design automation point of view it is important to design for the worst case, leaving us with margin for errors due to process

variability. *Here worst case refers to the power dissipated during a non-adiabatic clocking scheme*. For worst case considerations, the upper bound for power is more relevant. In this dissertation, we present the results of this non-adiabatic power model in chapter 4.

As research progresses, it is natural to look beyond device level issues in QCA designs and explore circuit level issues so as to scope out the types of circuits that can be built. However, QCA modeling tools available for such designs have been at the layout level. The operations of nanoscale devices are dominated by quantum mechanics, making it difficult to model various issues, such as error or power dissipation with deterministic state models. This has implications in the structure of the design methodology to be applied. Hierarchical design at multiple levels of abstraction, such as architectural, circuit, layout, and device levels, is probably still possible. However, the nature of coupling of the issues between levels would be different and stronger.For this, we need computing models at higher levels of abstraction that are strongly determined by layout-level quantum-mechanical models. We present a hierarchical design scheme that uses probabilistic macromodels to implement circuit level QCA architecture in chapter 5. The probabilistic macromodels used as circuit blocks in this design scheme are derived from the layout level graphical models that are presented in the next chapter.

# CHAPTER 3

# PROBABILISTIC BAYESIAN NETWORK MODELING

## 3.1 Introduction

In this chapter [24, 25] we develop a fast, Bayesian Probabilistic Computing model that exploits the induced causality of clocking to arrive at a model with the minimum possible complexity. The probabilities directly model the quantum-mechanical steady-state probabilities (density matrix) or equivalently, the cell polarizations. The attractive feature of this model is that not only does it model the strong dependencies among the cells, but it can be used to compute the steady state cell polarizations, without iterations or the need for temporal simulation of quantum mechanical equations.

Our proposed modeling is based on density matrix-based quantum modeling, which takes into account dependency patterns induced by clocking, and is non-iterative. It allows for quick estimation and comparison of quantum-mechanical quantities for a QCA circuit, such as QCA-state occupancy probabilities or polarizations at any cell, their dependence on temperature, or any parameter that depends on them. This will enable one to quickly compare, contrast and fine tune clocked QCA circuits designs, before performing costly full quantum-mechanical simulation of the temporal dynamics.

We validate our modeling with coherence vector based temporal simulation for various QCA systems (Fig. 3.5.). We also show, using the *clocked* majority gate, how the model can used to study dependencies with respect to temperature and inputs (Fig. 3.5.).

### 3.2 Quantum Mechanical Probabilities

Following Tougaw and Lent [36] and other subsequent works on QCA, we use the two-state approximate model of a single QCA cell. We denote the two possible, orthogonal, eigenstates of a cell by $|1\rangle$ and $|0\rangle$. The state at time $t$, which is referred to as the wave-function and denoted by $|\Psi(t)\rangle$, is a linear combination of these two states, i.e. $|\Psi(t)\rangle = c_1(t)|1\rangle + c_2(t)|0\rangle$. Note that the coefficients are function of time. The expected value of any observable, $\langle\hat{A}(t)\rangle$, can be expressed in terms of the wave function as $\langle\hat{A}\rangle = \langle\Psi(t)|\hat{A}(t)|\Psi(t)\rangle$ or equivalently as $\mathrm{Tr}[\hat{A}(t)|\Psi\rangle(t)\langle\Psi(t)|]$, where Tr denotes the trace operation, $\mathrm{Tr}[\cdots] = \langle 1|\cdots|1\rangle + \langle 0|\cdots|0\rangle$. The term $|\Psi(t)\rangle\langle\Psi(t)|$ is known as the density operator, $\hat{\rho}(t)$. Expected value of any observable of a quantum system can be computed if $\hat{\rho}(t)$ is known.

A 2 by 2 matrix representation of the density operator, in which entries denoted by $\rho_{ij}(t)$ can be arrived at by considering the projections on the two eigenstates of the cell, i.e. $\rho_{ij}(t) = \langle i|\hat{\rho}(t)|j\rangle$. This can be simplified further.

$$\begin{aligned} \rho_{ij}(t) &= \langle i|\hat{\rho}(t)|j\rangle \\ &= \langle i|\Psi(t)\rangle\langle\Psi(t)|j\rangle = (\langle i|\Psi(t)\rangle)(\langle j|\Psi(t)\rangle)^* \\ &= c_i(t)c_j^*(t) \end{aligned} \tag{3.1}$$

The density operator is a function of time and using Loiuville equations we can capture the temporal evaluation of $\rho(t)$ in Eq. 3.2.

$$\hbar\frac{\partial}{\partial t}\rho(\mathbf{t}) = \mathbf{H}\rho(\mathbf{t}) - \rho(\mathbf{t})\mathbf{H} \tag{3.2}$$

where H is a 2 by 2 matrix representing the Hamiltonian of the cell and using Hartree approximation. Expression of Hamiltonian is shown in Eq. 3.3 [36].

$$\mathbf{H} = \begin{bmatrix} -\frac{1}{2}\sum_i E_k P_i f_i & -\gamma \\ -\gamma & \frac{1}{2}\sum_i E_k P_i f_i \end{bmatrix} = \begin{bmatrix} -\frac{1}{2}E_k\bar{P} & -\gamma \\ -\gamma & \frac{1}{2}E_k\bar{P} \end{bmatrix} \tag{3.3}$$

where the sums are over the cells in the local neighborhood. $E_k$ is the "kink energy" or the energy cost of two neighboring cells having opposite polarizations. $f_i$ is the geometric factor capturing electrostatic fall off with distance between cells. $P_i$ is the polarization of the $i$-th cell. And, $\gamma$ is the tunneling energy between two cell states, which is controlled by the clocking mechanism. The notation can be further simplified by using $\bar{P}$ to denote the weighted sum of the neighborhood polarizations $\sum_i P_i f_i$. Using this Hamiltonian the steady state polarization is given by

$$P^{ss} = -\lambda_{\mathbf{3}}^{\mathbf{ss}} = \rho_{11}^{ss} - \rho_{00}^{ss} = \frac{E_k\bar{P}}{\sqrt{E_k^2\bar{P}^2 + 4\gamma^2}} \tanh\left(\frac{\sqrt{E_k^2\bar{P}^2/4 + \gamma^2}}{kT}\right) \tag{3.4}$$

Eq. 3.4 can be written as

$$P^{ss} = \frac{E}{\Omega}\tanh(\Delta) \tag{3.5}$$

where $E = 0.5\sum_i E_k P_i f_i$, total kink energy and Rabi frequency $\Omega = \sqrt{E_k^2\bar{P}^2/4 + \gamma^2}$ and $\Delta = \frac{\Omega}{kT}$ is the thermal ratio. We will use the above equation to arrive at the probabilities of observing (upon making a measurement) the system in each of the two states. Specifically, $\rho_{11}^{ss} = 0.5(1 + P^{ss})$ and $\rho_{00}^{ss} = 0.5(1 - P^{ss})$, where we made use of the fact that $\rho_{00}^{ss} + \rho_{11}^{ss} = 1$.

### 3.3 Bayesian Modeling

We propose a Bayesian Network based modeling and inference for the QCA cell polarization. A Bayesian network[122, 22, 23] is a Directed Acyclic Graph (DAG) in which

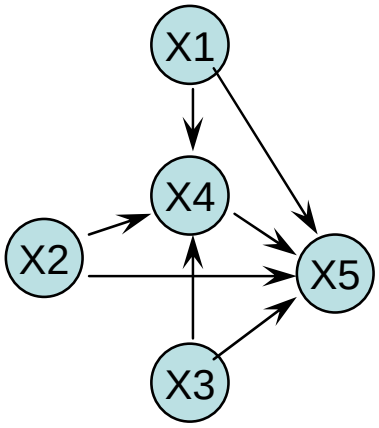


Figure 3.1. A small Bayesian network

the nodes of the network represent random variables and a set of directed links connect pairs of nodes. The links represent causal dependencies among the variables. Each node has a conditional probability table (CPT) except the root nodes. Each root node has a prior probability table. The CPT quantifies the effect the parents have on the node. Bayesian networks compute the joint probability distribution over all the variables in the network, based on the conditional probabilities and the observed evidence about a set of nodes.

Fig. 3.1. illustrates a small Bayesian network that is a subset of a Bayesian Network for a majority logic. In general, $x_i$ denotes some value of the variable $X_i$ and in the QCA context, each $X_i$ is the random variable representing an event that the cell is at steady-state logic "1" or at steady state logic "0". The exact joint probability distribution over the variables in this network is given by Eq. 3.6.

$$\begin{aligned} P(x_5, x_4, x_3, x_2, x_1) &= P(x_5|x_4, x_3, x_2, x_1) \\ &\quad P(x_4|x_3, x_2, x_1)P(x_3|x_2, x_1) \\ &\quad P(x_2|x_1)P(x_1). \end{aligned} \tag{3.6}$$

In this BN, the random variable, $X_5$ is independent of $X_1$, given the state of its parents $X_4$ This *conditional independence* can be expressed by Eq. 3.7.

$$P(x_5|x_4,x_3,x_2,x_1) \quad = \quad P(x_5|x_4) \tag{3.7}$$

Mathematically, this is denoted as $I(X_5,\{X_4\},\{X_1,X_2,X_3\})$. In general, in a Bayesian network, given the parents of a node *n*, *n* and its descendents are independent of all other nodes in the network. Let $U$ be the set of all random variables in a network. Using the conditional independencies in Eq. 3.7, we can arrive at the minimal factored representation shown in Eq. 3.8.

$$\begin{aligned} P(x_5,x_4,x_3,x_2,x_1) \quad &= \quad P(x_5|x_4)P(x_4|x_3,x_2,x_1) \\ & \qquad P(x_3)P(x_2)P(x_1). \end{aligned} \tag{3.8}$$

In general, if $x_i$ denotes some value of the variable $X_i$ and $pa(x_i)$ denotes some set of values for $X_i$'s parents, the minimal factored representation of exact joint probability distribution over *m* random variables can be expressed as in Eq. 3.9.

$$P(X) = \prod_{k=1}^{m} P(x_k|pa(x_k)) \tag{3.9}$$

Note that, Bayesian Networks are proven to be minimal representation that can model all the independencies in the probabilistic model. Also, the graphical representation in Fig. 3.1. and probabilistic model match in terms of the conditional independencies. Since Bayesian Networks uses directional property it is directly related to inference under causality. In a clockless QCA circuit, cause and effect between cells are hard to determine as the cells will affect one another irrespective of the flow of polarization. Clocked QCA circuits however have innate ordering sense in them. Part of the ordering is imposed by the clocking zones. Cells in the previous clock zone are the drivers or the causes of the change in

polarization of the current cell. Within each clocking zone, ordering is determined by the direction of propagation of the wave function [36].

Let $Ne(X)$ denote the set of all neighboring cells that can effect a cell, $X$. It consists of all cells within a pre-specified radius. Let $C(X)$ denote the clocking zone of cell $X$. We assume that we have phased clocking zones, as has been proposed for QCAs. Let $T(X)$ denote the time it takes for the wave function to propagate from the nodes nearest to the previous clock zone or from the inputs, if $X$ shares the clock with the inputs. Note that only the relative values of $T(X)$ are important to decide upon the causal ordering of the cells. Thus, given a set of cells, we can exactly predict (dependent on the effective radius of influence assumed) the parents of every cell and all the non-parent neighbors. In this work, we assume to use *four* clock zones. We denote this parent set by $Pa(X)$. This parent set is logically specified as follows.

$$Pa(X) = \{Y | Y \in Ne(X), (C(Y) <_{mod4} C(X)) \vee (T(Y) < T(X))\} \tag{3.10}$$

The *causes*, and hence the parents, of $X$ are the cells in the previous clocking zone and the cells are nearer to the previous clocking zone than $X$. The children set, $Ch(X)$, of a node, $X$, will be the neighbor nodes that are not parents, i.e. $Ch(X) = Ne(X)/Pa(X)$.

The next important part of a Bayesian network specification involves the conditional probabilities $P(x|pa(X))$, where $pa(X)$ represents the values taken on by the parent set, $Pa(X)$.

We choose the children states (or polarization) so as to maximize $\Omega = \sqrt{E_k^2 \bar{P}^2/4 + \gamma^2}$, which would minimize the ground state energy over all possible ground states of the cell. Thus, the chosen children states are

$$ch^*(X) = \arg\max_{ch(X)} \Omega = \arg\max_{ch(X)} \sum_{i \in (Pa(X) \cup Ch(X))} E_k \bar{P} \tag{3.11}$$

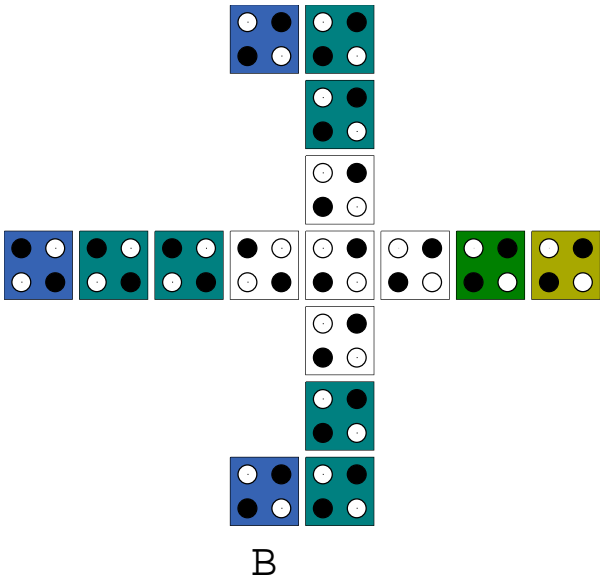



Figure 3.2. Clocked QCA majority gate layout

The steady state density matrix diagonal entries (Eq. 3.5 with these children state assignments are used to decide upon the conditional probabilities in the Bayesian network (BN).

$$\begin{aligned} P(X=0|pa(X)) &= \rho_{00}^{ss}(pa(X), ch^*(X)) \\ P(X=1|pa(X)) &= \rho_{11}^{ss}(pa(X), ch^*(X)) \end{aligned} \tag{3.12}$$

Once we compute all the conditional probabilities, we provide prior probabilities for the inputs. We can then infer the Bayesian Networks to obtain the steady state probability of observing all the cells including the outputs at “1” or “0”.

### 3.4 Experimental Results

In this section, we discuss the results of our model with a small example of three input majority gate as the cell layout of for QCA can be effectively drawn with synthesis using inverter and majority gates. Fig. 3.4 shows the cell layout of a clocked majority gate. The

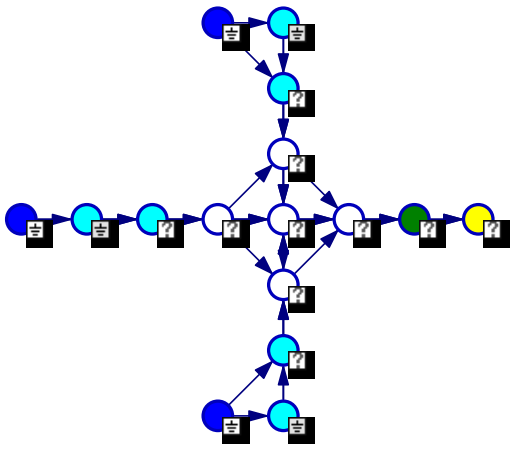


Figure 3.3. Bayesian net dependency structure corresponding to the QCA majority gate with nodes corresponding to the individual cells and links denoting direct dependencies.

Bayesian Network structure is shown in Fig 3.3. Note that we obtain the structure based on the causal flow of the wave function and the information regarding the clock zone. We use ”Genie” [123] software tool for Bayesian inference. We present the extended view of the Bayesian Network shown in Fig. 3.4. with the polarization of each cell shown for a particular input set.

In Fig 3.5., we report the steady state probabilities of the correct outputs w.r.t temperature and we show that the probability of correct output vary with the input space. As we can see that the temperature plays a key role in obtaining correct signal behavior. More effect of temperature is less for some inputs say $\{0,1,1\}$ than $\{0,0,1\}$. Also, the input set $\{0,0,1\}$ and $\{0,1,0\}$ shows different sensitivity. Hence layout plays an important role in the error behavior of QCA. We validated our model with respect to the QCADesigner (Fig 3.6.) and received the same accuracy using the temporal simulation. However, the time for the simulation is an order of magnitude faster.

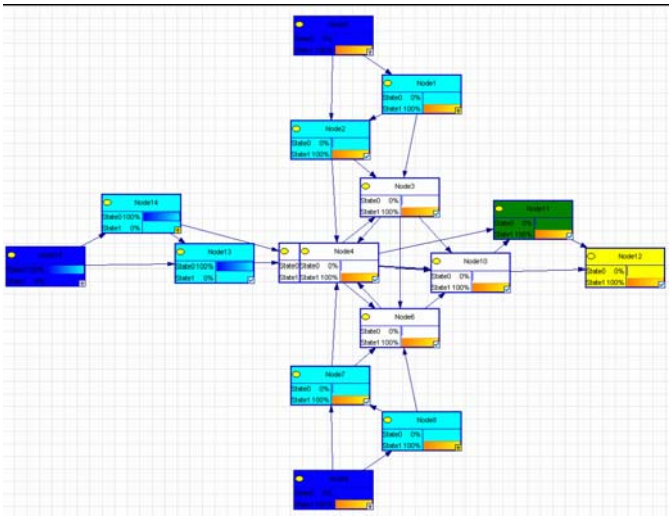


Figure 3.4. Exploded view of the Bayesian net structure, laying bare the directed link structure and the node information.

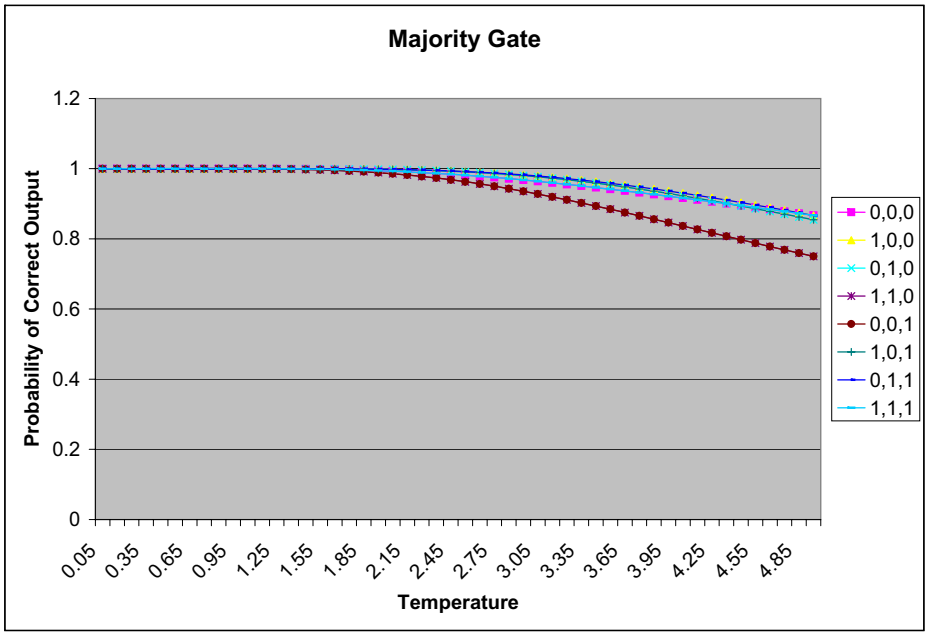



Figure 3.5. Dependence of probability of correct output of the majority gate with temperature *and* inputs. Note the dependence on inputs.

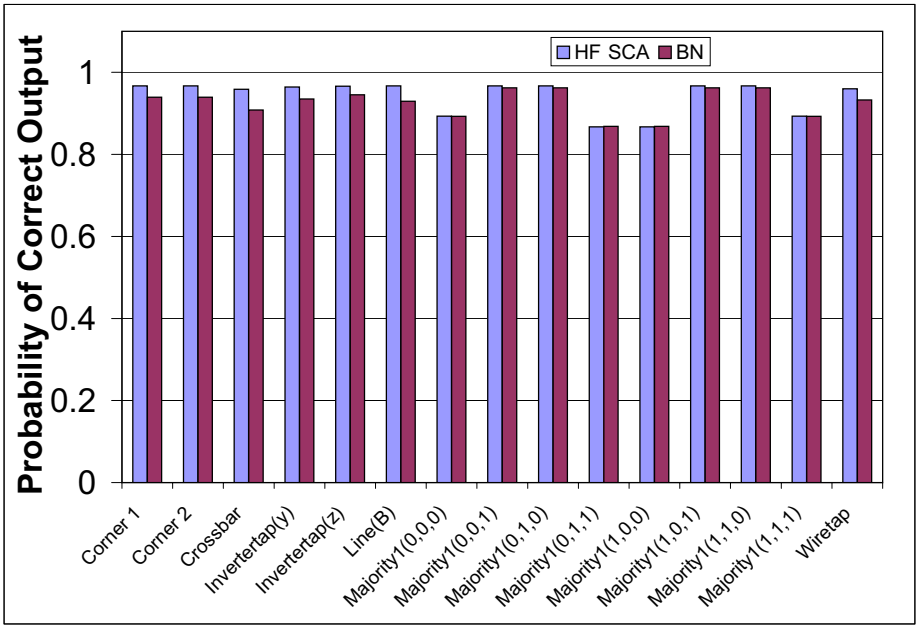



Figure 3.6. Validation of the Bayesian network modeling of QCA circuits with HartreeFock approximation based coherence vectorbased quantum mechanical simulation. Probabilities of correct output are compared for basic circuit elements

# CHAPTER 4

# POWER DISSIPATION IN QCA

## 4.1 Introduction

For computation mechanisms that involve the transfer or flow of electrons, such as CMOS gates, it has been shown that with continued scaling if single electrons are involved in the computation the power per gate would approach the $kT$ limit but the power density would be extremely high [124, 125]. Unlike computation mechanisms that involve the transfer or flow of electrons, such as CMOS gates, QCA computation does not involve electron transfer between adjacent QCA cells. Since only few electrons are involved in QCA computations, it is susceptible to thermal issues. Therefore it is important to model and to consider power as an important parameter during the QCA design process at multiple levels of design abstraction.

While work on defect and faults in QCA circuits, which are other important issues, have started [117, 118, 119], power issues have not been considered extensively. Perhaps the most pure power model is the quantum-mechanical model of the temporal dynamics of power derived by Timler and Lent [126, 127]. They identified three components of power: clock power, cell to cell power gain, and power dissipation. While this model gives us physically close estimates, it is computationally expensive to estimate. When designing QCA circuits, we would like estimate power quickly in order to choose among many different alternatives and parameters. The need for full blown quantum-mechanical estimation will be relegated to the very end of the design process. To this end, some studies [128, 90]

present lower bounds of power dissipated that are easy to compute. However, from a design automation point of view it is important to design for the worst case, leaving us with margin for errors due to process variability. *Here worst case refers to the power dissipated during a non-adiabatic clocking scheme*. For worst case considerations, the upper bound for power is more relevant. We derive such an upper bound and show how it can be relevant for QCA design automation. Some other relevant power related works include the energy vs. speed trade-off study in [129] for different clocking schemes, however, in the context of reversible computing. In [130], a RC model for a clocked QCA chain is used to investigate power dissipation under adiabatic clocking scheme.

Under the Hartree-Fock quantum mechanical approximation, which has been found to be adequate, the dynamics of a collection of QCA cells can be expressed in terms of the dynamics of individual cells. As a result, the power dissipation for a QCA circuit can expressed as the sum of power estimates computed on a per-cell basis. Each cell in a QCA circuit sees three types of events: (i) clock going from low to high so as to "depolarize" a cell, (ii) input or cells in previous clock zone switching states, and (iii) clock changing from high to low, latching and holding the cell state to the new state. Each of these events are associated with power loss. An interesting point is that the power dissipated during the first and the third transitions is due to the clock changing and occurs even if the state of a cell does not change. This is analogous to "leakage" power in CMOS circuits. The power loss due to the second event can be termed as the "switching" power since it is dependent on the cells actually changing state. Clock energy needs to be high to drive the cell into an intermediate, depolarized state. In a fully depolarized state, the change in driver polarization has no effect on the driven cell, hence the "switching" power is zero. This is the ideal case. However, to achieve this the clocking energy needs to be high and, consequently, the associated "leakage" power would be high. Thus, these two components of power are inversely related. The upper bounds derived in this paper will help us quantify

this relationship. However, a real clock implementation will also add to power loss in the clocking circuit itself. This will add to the overall power dissipation in a QCA circuit. In this study we do not account for this power loss.

A shortened version of this bound derivation is presented in in [95], however, using very small QCA logic elements. The theoretical contributions of this work are (i) the computation of upper bound of power dissipated in a QCA cell representing the worst case input switching vector set and (ii) the characterization of power into two components: leakage and switching. This upper bound, which is easy to compute, can be used in the QCA circuit design process. Further, we demonstrate how these estimates can be used (iii) to characterize the power dissipation in basic QCA elements like the inverter, majority gate, and crossbar, (iv) to compare two functionally equivalent adder circuits in terms of power dissipated during any switching event, (v) to compute power in large QCA circuit like a 4x1 Multiplexer and a single bit ALU, (vi) to study variation of power expended with different input states, and (vii) to locate the thermal weak spots in a design.

The organization of this chapter is as follows. Section 4.2 summarizes the quantum formulation of the power dissipation in QCAs as presented in [126]. Using this expression, we derive in Section 4.3 the upper bound for the power dissipated in a QCA cell during each clock cycle. We then use this per cell bound to estimate the power in the whole circuit as described in Section 4.4. In Section 4.5 we show simulation results using this upper bound. We first validate the bound using quantum mechanical simulations and show that the bound holds. We then demonstrate power the estimation process and study the power dissipation in a number of logic elements such as majority gates, inverter, single bit adders and also for large QCA circuits such as a 4x1 multiplexer and a single bit ALU [131].

### 4.2 Quantum Mechanical Power

We denote the eigen states of a cell, corresponding to the two ground states, of each cell by $|0\rangle$ and $|1\rangle$. This could represent the ground state of a cell with one electron in two dots, as in molecular-QCA, or a cell with two electrons with four dots. An array of cells can be modeled fairly well by considering cell-level quantum entanglement of these two states and just Coulombic interactions with nearby cells, using the Hartee-Fock (HF) approximation [36, 132]. This allows one to characterize the evolution of the individual wave functions. The state of a cell at time $t$, which is referred to as the wave-function and denoted by $|\Psi(t)\rangle$, is a linear combination of these two states, i.e. $|\Psi(t)\rangle = c_0(t)|0\rangle + c_1(t)|1\rangle$. The coefficients, $c_0(t)$ and $c_1(t)$, are functions of time. The expected value of any observable, $\langle\hat{A}(t)\rangle$, can be expressed in terms of the wave function as $\langle\hat{A}\rangle = \langle\Psi(t)|\hat{A}(t)|\Psi(t)\rangle$ or equivalently as $\mathrm{Tr}[\hat{A}(t)|\Psi(t)\rangle\langle\Psi(t)|]$, where Tr denotes the trace operation, $\mathrm{Tr}[\cdots] = \langle 0|\cdots|0\rangle + \langle 1|\cdots|1\rangle$. The term $|\Psi(t)\rangle\langle\Psi(t)|$ is known as the density operator, $\hat{\rho}(t)$. Expected value of any observable of a quantum system can be computed if $\hat{\rho}(t)$ is known.

The entries of the density matrix, $\rho_{ij}(t)$, is defined by $c_i(t)c_j^*(t)$ or $\rho(t) = \mathbf{c}(\mathbf{t})\mathbf{c}(\mathbf{t})^*$, where $^*$ denotes the conjugate transpose operation. Note that the density matrix is Hermitian, i.e. $\rho(t) = \rho(t)^*$. Each diagonal term, $\rho_{ii}(t) = |c_i(t)|^2$, represents the *probability* of finding the system in state $|i\rangle$. It can be easily shown that $\rho_{00}(t) + \rho_{11}(t) = 1$. In QCA device modeling literature, one uses the concept of *polarization*, $s$, to characterize the state of a cell and is simply $\rho_{11}(t) - \rho_{00}(t)$, the difference of the two probabilities. It ranges from -1 to 1.

The density operator is a function of time, $\hat{\rho}(t)$, and its dynamics is captured by the Loiuville equation or the von Neumann equation, which can derived from the basic Schrodinger

equations that capture the evolution of the wave function over time, $\Psi(t)$.

$$\hbar\frac{\partial}{\partial t}\rho(t) \;=\; \mathbf{H}\rho(t) - \rho(t)\mathbf{H} \tag{4.1}$$

where **H** is a 2 by 2 matrix representing the Hamiltonian of the cell. For arrangements of QCA cells, it is common to assume only Coulombic interactions between cells and use the Hartree-Fock approximation to arrive at the matrix representation of the Hamiltonian given by [36]

$$\mathbf{H} = \begin{bmatrix} -\frac{1}{2}\sum_i E_k s_i f_i & -\gamma \\ -\gamma & \frac{1}{2}\sum_i E_k s_i f_i \end{bmatrix} = \begin{bmatrix} -\frac{1}{2}S & -\gamma \\ -\gamma & \frac{1}{2}S \end{bmatrix} \tag{4.2}$$

where the sums are over the cells. $E_k$ is the energy cost of two neighboring cells with opposite polarizations; this is also referred to as the "kink energy". $f_i$ is the geometric factor capturing electrostatic fall off with distance between cells. $s_i$ is the polarization of the *i*-th neighboring cell. The tunneling energy between the two states of a cell, which is controlled by the clocking mechanism, is denoted by $\gamma$. For notational simplification, we will use $S$ to denote the total kink energy due to the polarized neighbors.

To arrive at a more compact mathematical representation we use the Bloch formulation of the Schrodinger equation that expresses the evolution of quantum systems in operator spaces. The density operator can be expressed as a linear combination of the SU(2), the Pauli's spin operators $\sigma_i$s

$$\rho(\mathbf{t}) = \sum_{i=1}^{3} \lambda_i \sigma_i \tag{4.3}$$

Here $\sigma_i$ are the Pauli's spin matrices given by:

$$\sigma_\mathbf{1} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \sigma_\mathbf{2} = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}, \sigma_\mathbf{3} = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} \tag{4.4}$$

The combination coefficients form the coherence vector ($\vec{\lambda}$) can be expressed by

$$\lambda_i = Tr\{\hat{\rho}\hat{\sigma}_i\}. \tag{4.5}$$

The two state Hamiltonian can be projected onto the basis of generators to form a real three-dimensional energy vector $\vec{\Gamma}$, whose components are

$$\Gamma = \frac{Tr\{\hat{H}\hat{\sigma}\}}{\hbar} = \frac{1}{\hbar}\begin{bmatrix} -2\gamma, & 0, & S \end{bmatrix}. \tag{4.6}$$

The Bloch equation governing the evolution of the coherence vector can be derived from the Liouville equation to be

$$\frac{d}{dt}\vec{\lambda} = \vec{\Gamma} \times \vec{\lambda} \tag{4.7}$$

This formulation does not account for the effect of dissipative coupling with heat bath. One reasonable approximation is to add an inhomogeneous linear term to this equation to account for damping.

$$\frac{d}{dt}\vec{\lambda} = \vec{\Gamma} \times \vec{\lambda} + \xi\vec{\lambda} + \vec{\eta} \tag{4.8}$$

We choose the parameters $\xi$ and $\vec{\eta}$ so that they represent inelastic dissipative heat bath coupling (open world), with the system moving towards the ground state [36, 132].

$$\vec{\eta} = \frac{1}{\tau}\vec{\lambda}^{ss} \text{ and } \xi = -\begin{bmatrix} \frac{1}{\tau} & 0 & 0 \\ 0 & \frac{1}{\tau} & 0 \\ 0 & 0 & \frac{1}{\tau} \end{bmatrix} \tag{4.9}$$

where $\vec{\lambda}^{ss}$ is the steady-state coherence vector and $\tau$ is the energy relaxation time. If $\tau \to \infty$, it represents the absence of any dissipation. Lower the value of $\tau$, faster the heat dissipation away from the cell. The steady-state coherence vector can be derived from the steady-state

density matrix at thermal equilibrium.

$$\rho^{ss} = \frac{e^{-\mathbf{H}/kT}}{\mathrm{Tr}[e^{-\mathbf{H}/kT}]} \tag{4.10}$$

where $k$ is the Boltzman constant and $T$ is the temperature. The corresponding steady state coherence vector is given by

$$\vec{\lambda}^{ss} = \mathrm{Tr}\{\rho^{ss}\sigma\} = -\frac{\vec{\Gamma}}{|\vec{\Gamma}|}\tanh\Delta \tag{4.11}$$

where $\Delta = \frac{\Omega}{kT}$, is the thermal ratio, with $\Omega = \sqrt{4\gamma^2 + S^2}$, the energy term (also known as the Rabi frequency).

The expected value of the Hamiltonian at each time instant is given by

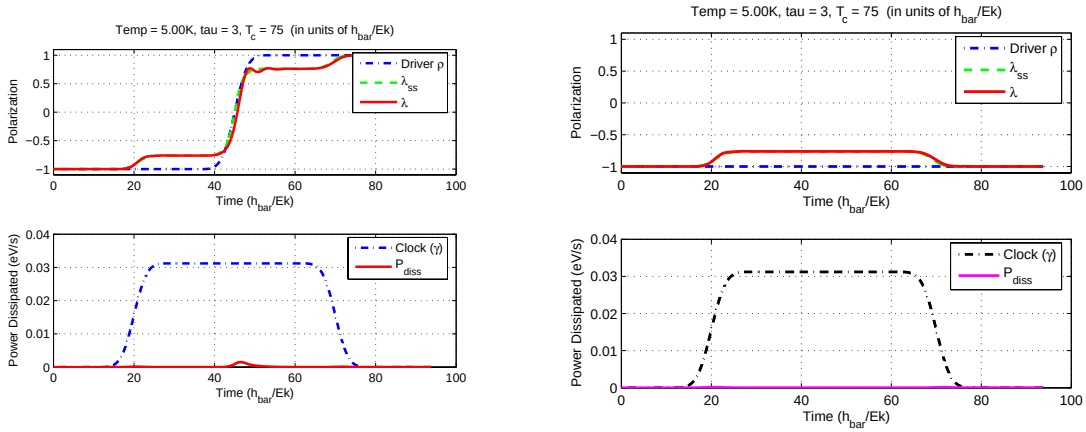
$$E = \langle H \rangle = \frac{\hbar}{2}\vec{\Gamma}\cdot\vec{\lambda} \tag{4.12}$$

The equation for the instantaneous power is given by

$$P_{total} = \frac{d}{dt}E = \frac{\hbar}{2}\left(\frac{d}{dt}\vec{\Gamma}\right)\cdot\vec{\lambda} + \frac{\hbar}{2}\vec{\Gamma}\cdot\left(\frac{d}{dt}\vec{\lambda}\right) \tag{4.13}$$

The first term captures the power in and out of the clock and cell to cell power flow. The second term represents the dissipated power. It is this quantity that we are interested in.

$$P_{diss}(t) = \frac{\hbar}{2}\vec{\Gamma}(t).\left(\frac{d}{dt}\vec{\lambda}(t)\right) \tag{4.14}$$




(a) (b)

Figure 4.1. Polarization change (top plot) and power loss (bottom plot) in a single cell when its polarization changes from (a) -1 to 1 (or 0 to 1 logic) and (b) -1 to -1 (remains at state 0) during a quasi-adiabatic clocking scheme.

### 4.3 Upper Bound for Power Dissipation

Coupling the expression for power dissipation with the damped Bloch equation we see that

$$P_{diss}(t) = -\frac{\hbar}{2\tau}\vec{\Gamma}(t).\left(\vec{\lambda}(t) - \vec{\lambda}^{ss}(t)\right) \tag{4.15}$$

If the instantaneous coherence vector tracks the steady state coherence vector for that time instant, i.e. $\vec{\lambda}(t) \approx \vec{\lambda}^{ss}(t)$ then the power dissipated is very low. Fig. 4.1.(a) (bottom plot) shows the instantaneous power dissipation when the driver polarization switches from -1 to 1. The top plot of Fig. 4.1.(a) shows the change in the driver polarization and the associated change in the steady state polarization $\vec{\lambda}_3^{ss}(t)$. Note that in this case, the cell polarization $\vec{\lambda}_3(t)$ tracks the steady state value quite well. The bottom plot of Fig. 4.1.(a) shows the clock energy change and the power dissipated. We note that there is only very slight loss of power during the switching of the driver polarization. Fig. 4.1.(b), which is for the case of no change in driver polarization, also tells the same story of low power loss.

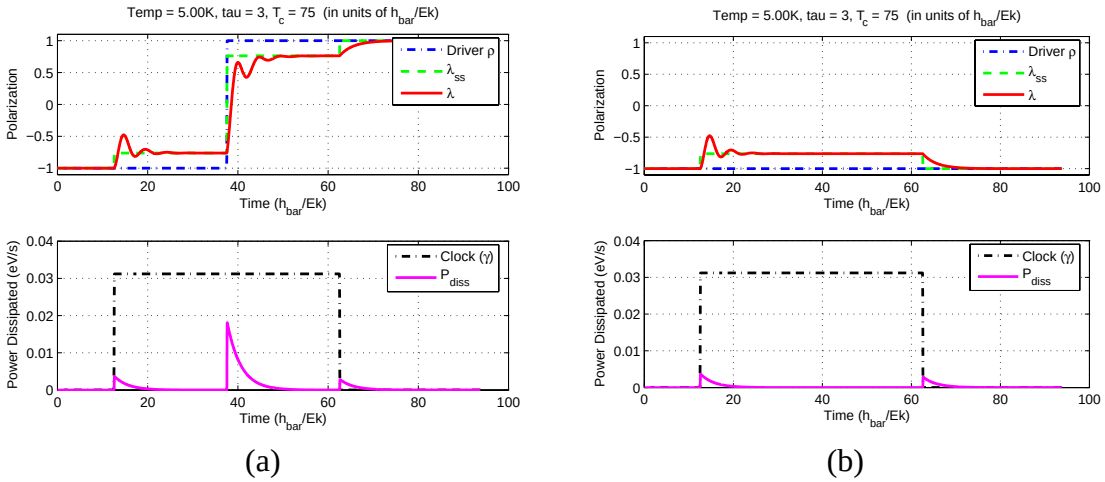



Figure 4.2. Polarization change (top plot) and power loss (bottom plot) in a single cell when its polarization changes from (a) -1 to 1 (or 0 to 1 logic) and (b) -1 to -1 (no change in state) during non-adiabatic clocking scheme

High dissipation situation arises when $\vec{\lambda}(t)$ lags the changing $\vec{\lambda}_{ss}(t)$. From Eq. 4.11 we can see that $\vec{\lambda}^{ss}$ changes whenever the underlying Hamiltonian changes, which happens when (i) clock goes from low to high ($\gamma_L \rightarrow \gamma_H$) so as to "depolarize" a cell, (ii) input or cells in previous clock zone switches states ($S_- \rightarrow S_+$), and (iii) clock changes from high to low ($\gamma_H \rightarrow \gamma_L$), latching and holding the cell state to the new state. Fig. 4.2.(a) shows the switching behavior and power dissipation for abrupt change in driver polarization and clocking. As we can see from the graph, the steady state polarization $\vec{\lambda}_3(t)$ of the cell is not able to follow the corresponding steady state polarization. There is some lag and ripple associated with the change. This leads to power loss, which is shown in the bottom plot of Fig. 4.2.(a) Note that there is power loss for all the three events. Fig. 4.2.(b) shows the same switching behavior and power dissipation in the cell during a non adiabatic event even when the driver polarization remains the same (-1 to -1 switching). As we can see from the graphs, the total power dissipated by the cell occurs not only when its polarization changes, but a significant amount of power loss also occurs when the clock energy barriers are raised and lowered. The faster the changes involved in these events, the more the power

dissipation. To arrive at the upper bound of the power loss, we consider the limiting case of instantaneous change; we model these events using as step functions.

We derive the energy dissipated for each of these three events by integrating around them. Without loss of generality, let the event under consideration be centered at $t = 0$. We integrate over $[-D, D]$, such that $D >> \tau$, i.e. the integration time period is much larger than the relaxation time constant. This, of course, places limit on the clock speed. This constraint is natural also for correct operation; clock period should be larger than the relaxation time constants otherwise errors will arise. Energy dissipated over a time period $[-D, D]$ can be arrived at by integrating $P_{diss}(t)$.

$$\begin{aligned} E_{diss} &= \frac{\hbar}{2}\int_{-D}^{D} \vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}dt \\ &= \frac{\hbar}{2}\left(\left[\vec{\Gamma}\cdot\vec{\lambda}\right]_{-D}^{D} - \int_{-D}^{D}\vec{\lambda}\cdot\frac{d\vec{\Gamma}}{dt}dt\right) \\ &= \frac{\hbar}{2}\left(\vec{\Gamma}_{+}\cdot\vec{\lambda}_{+} - \vec{\Gamma}_{-}\cdot\vec{\lambda}_{-} - \int_{-D}^{D}\vec{\lambda}\cdot\frac{d\vec{\Gamma}}{dt}dt\right) \end{aligned} \tag{4.16}$$

where we use the notation $\vec{\Gamma}_{-}$ and $\vec{\Gamma}_{+}$ to denote $\vec{\Gamma}(-D)$ and $\vec{\Gamma}(D)$, and similarly for $\vec{\lambda}$. This dissipated power to the bath will be maximum when the rate of change of $\vec{\Gamma}$ is the maximum, i.e. non-adiabatic. We model this mathematically using the delta function.

$$\frac{d\vec{\Gamma}}{dt} = \left(\vec{\Gamma}_{+} - \vec{\Gamma}_{-}\right)\delta(t) \tag{4.17}$$

where $\vec{\Gamma}_{+}$ and $\vec{\Gamma}_{-}$ are the values of the Hamiltonian "before" and the "after" the transition. Using this model and the integral property of the delta function, $\int f(t)\delta(t)dt = f(0)$, we have

$$E_{diss} < \frac{\hbar}{2}\left(\vec{\Gamma}_{+}\cdot\vec{\lambda}_{+} - \vec{\Gamma}_{-}\cdot\vec{\lambda}_{-} - \vec{\lambda}(0)\cdot(\vec{\Gamma}_{+} - \vec{\Gamma}_{-})\right) \tag{4.18}$$

Table 4.1. Bloch Hamiltonian before and after a change in clock or the neighboring polarization

| | Clock Up $\gamma_L \rightarrow \gamma_H$ | Driver Polarization $S_- \rightarrow S_+$ | Clock Down $\gamma_H \rightarrow \gamma_L$ |
|---|---|---|---|
| $\vec{\Gamma}_- =$ | $\frac{1}{\hbar}[\ -2\gamma_L,\ 0,\ S_-\ ]$ | $\frac{1}{\hbar}[\ -2\gamma_H,\ 0,\ S_-\ ]$ | $\frac{1}{\hbar}[\ -2\gamma_H,\ 0,\ S_+\ ]$ |
| $\vec{\Gamma}_+ =$ | $\frac{1}{\hbar}[\ -2\gamma_H,\ 0,\ S_-\ ]$ | $\frac{1}{\hbar}[\ -2\gamma_H,\ 0,\ S_+\ ]$ | $\frac{1}{\hbar}[\ -2\gamma_L,\ 0,\ S_+\ ]$ |

As mentioned before, we assume that $D >> \tau$, i.e. the system is in equilibrium with the heat bath at $t = -D$ and $t = D$. In such case, we have $\lambda(0) = \lambda_- = \lambda_-^{ss}$ and $\lambda_+ = \lambda_+^{ss}$. Using these observations, we can show that

$$E_{diss} < \frac{\hbar}{2}\vec{\Gamma}_+ \cdot \left(\vec{\lambda}_+^{ss} - \vec{\lambda}_-^{ss}\right) \tag{4.19}$$

$$P = \frac{E_{diss}}{T_c} < \frac{\hbar}{2T_c}\vec{\Gamma}_+ \cdot \left(-\frac{\vec{\Gamma}_+}{|\vec{\Gamma}_+|}\tanh\left(\frac{\hbar|\vec{\Gamma}_+|}{kT}\right) + \frac{\vec{\Gamma}_-}{|\vec{\Gamma}_-|}\tanh\left(\frac{\hbar|\vec{\Gamma}_-|}{kT}\right)\right) \tag{4.20}$$

where we have characterized the power dissipation as the energy per clock cycle; $T_c$ is the clock period. As is evident, the power upper bound can be derived once we have the before and after Hamiltonian for the three power dissipating events. These values of the Hamiltonian are as shown in Table 4.2. The "leakage" power dissipated (energy per clock cycle) is the energy dissipated during the first and the third event associated with clock change. And, the "switching" power (energy per clock cycle) is the energy loss due to the second event.

### 4.4 Energy Dissipated per Clock Cycle in a QCA Circuit

Since the physics governing the power dissipation at each cell in a QCA circuit is similar, we can compute the total power (energy per clock cycle) by aggregating the power computed for each cell. The effect of cells on each other is captured through the electrostatic

kink energy between them. Let us consider a circuit with $N$ cells, denoted by $X_1, \cdots, X_N$, with the first $r$ of them representing the input cells. Let the polarization of the $i$-th cell be denoted by $x_i \in [-1, 1]$. For each switching of the input cells, we compute the power by keeping track of the before and after polarization of the cells. Let $x_{i|k}$ be the polarization of the $i$-th cell for the $k$-th possible input combination. We can compute this polarization using any of the simulation methods that are available for QCA circuits [42]. In our experiments we use the Bayesian Network modeling technique in [25] to probabilistically determine the polarizations in an efficient manner. Since in this work, we are interested in a hard upper bound on the total power dissipated in a circuit, hence we actually round off the computed polarization of each cell to the nearest pure value, i.e. -1 or 1 value.

To compute the power dissipated at each cell, we need to compute the effective kink energy of rest of the cells, $S_{i-}$ and $S_{i+}$ as the input switches from $k$-th combination to the $m$-th combination. This is easily computed as

$$S_{i-} = \sum_{j \in Ne(X_i)} E_k f_j x_{j|k} \text{ and } S_{i+} = \sum_{j \in Ne(X_i)} E_k f_j x_{j|m} \tag{4.21}$$

where the sum can be restricted to a local neighborhood of the cell since the distance related term, $f_j$, falls off as 5-th power of the distance from the cell. Using these values, and knowledge of the low and the high clock energies, $\gamma_L$ and $\gamma_H$, we can compute the leakage $(P^{leak}_{i,k\to m})$ and the switching $(P^{switch}_{i,k\to m})$ power (energy per clock cycle) bounds at each cell (Eq. 4.20). Given these estimates we can compute different design related parameters as outlined below. Note that the quantities we compute are actually bounds of the respective quantities; we do not emphasize the bound aspect to reduce notational clutter.

- Total Dissipated Power: for transition from the *k*-th input state to the *m*-th input state is given by

$$P^{tot}_{k\to m} = \sum_{i=(r+1)}^{N} P^{leak}_{i,k\to m} + P^{switch}_{i,k\to m} \tag{4.22}$$

- Average Power (over all input transitions): is given by

$$P^{avg} = \frac{1}{2^r}\sum_{k,m} P^{tot}_{k\to m} \tag{4.23}$$

- Maximum Power (over all input transitions): is given by

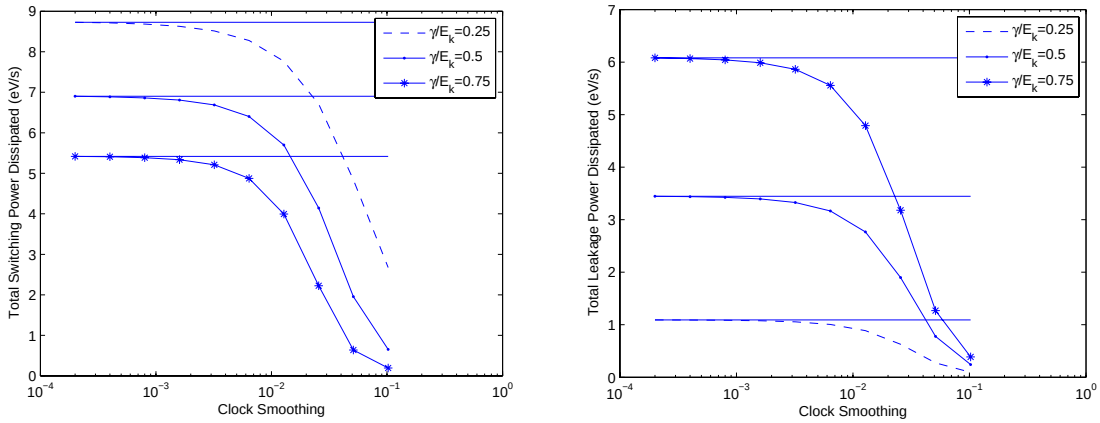
$$P^{max} = \max_{k,m} P^{tot}_{k\to m} \tag{4.24}$$

- Hot Spots: Power is not uniformly dissipated at each cell. It is important from a thermal error analysis point of view to identify the cells in a design where the power dissipation is high. Once we compute the average power dissipation at each cell over all input transitions, we can identify the hot-spot as the cells with *k* maximum power dissipation.

$$\arg\text{k-max}\{\frac{1}{2^r}\sum_{k,m} P_{i,k\to m} | i = r+1, N\} \tag{4.25}$$

## 4.5 Results

We first present empirical validation of the power bounds by computing exact power of one QCA cell under different clocking conditions and show that the bound holds. We follow this by showing examples of how this bound estimate can be used for QCA design automation. The size of QCA cells used in this study is 20nm x 20nm with a grid spacing of 20nm.We compute power dissipation bounds for some basic QCA logic elements such as the majority gate, inverter, AND gate, OR gate, crossbar and clocked majority gate. Since




(a) (b)

Figure 4.3. Variation of (a) switching power and (b) leakage power dissipated in a single cell with different amount of clock smoothing for different clock energy $\gamma$ levels. Adiabaticity of the switching process is controlled by smoothness of the clock transition. The horizontal line plots the upper bounds for each case as computed using the derived expressions.

power is dependent on the inputs, we show the maximum, minimum and average power dissipated in each of these circuits over all possible input transitions. Further, we make use of the power model to estimate power dissipated in two different designs of single bit adders and the thermal layout for both designs. Finally, we demonstrate the model for some large circuits – the 4x1 multiplexer and a single bit ALU design [131]. The ALU design consists of seven inputs and two outputs. The single bit ALU can be used to perform logical operations such a AND, OR and inversion. It can also perform mathematical operations such as addition and subtraction between two single bit numbers.

### 4.5.1 Energy Dissipation per Clock Cycle in a Single QCA Cell

The power dissipated at each cell is a function of the rate of change of the clock and the clock energy. We estimated the actual power dissipated using quantum model for various values of these parameter and compared them with the power bounds. Fig. 4.3.(a) and (b) shows the variation of switching and leakage power dissipation with varying amount clock

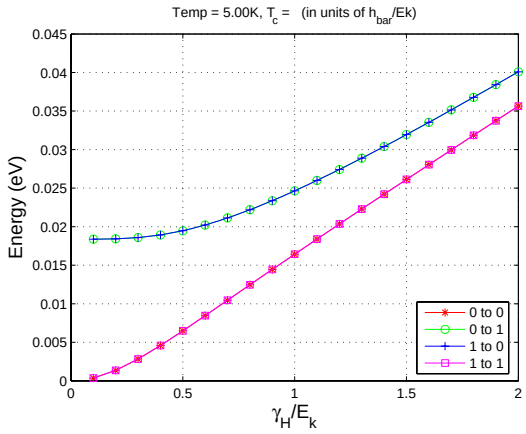



Figure 4.4. Dependence of energy dissipated (upper bound) in a cell with clock energy for different clock transitions. (a) 0→0 (b) 0→1 (c) 1→0 and (d) 1→1. Note that the plots for cases (a) and (d) overlap completely and so does the plots for cases (b) and (c).

smoothing and for different values of clock energy. The power bounds, which are functions of the clock energy(γ), are shown as horizontal lines. Adiabaticity of the system is directly proportional to the amount of clock smoothing. Higher clock smoothing implies more adiabaticity. We see that bounds do indeed hold and are reached when the clock smoothing is zero, i.e. abrupt clock changes, representing the fully non-adiabatic case.

Fig. 4.4. shows how the dissipated energy bound is different for different state transitions (a) 0→0 (b) 0→1 (c) 1→0 and (d) 1→1, as the clock energy supplied to the cell is increased from $0.05E_k$ to $2E_k$. Note that energy is dissipated even if the state of a cell does not change, i.e. for cases (a) and (d). This is because the high clock state only *partially* depolarizes a cell and there is change in this partial polarization with input change. As the high clock energy is increased, the cell gets depolarized to a greater extent and the contribution to overall dissipation due to switching states is less. However, as we see in Fig. 4.4., the total dissipated energy also increases; this is due to the contribution of dissipative event associated with clock transitions, i.e. "leakage power." So, even though high clock energy is desirable to depolarize the cell and ensure when the clock energy supplied to the cell is

increased from $0.05E_k$ to $2E_k$ for correct operation, it has to be limited from power considerations. Hence there is a trade-off between power and error when choosing the clock energy.

### 4.5.2 Energy Dissipation per Clock Cycle in Basic QCA Circuits

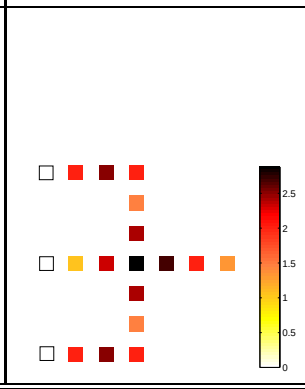
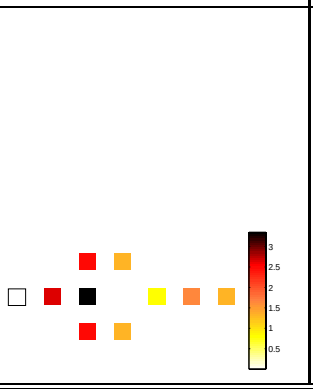
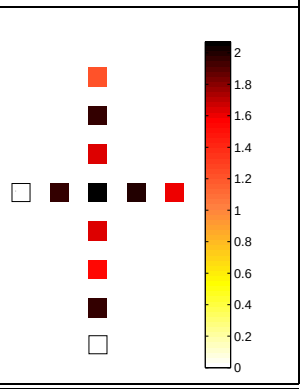
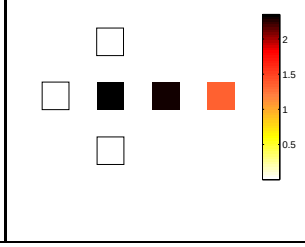
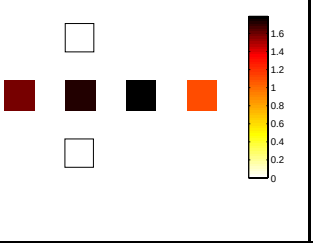
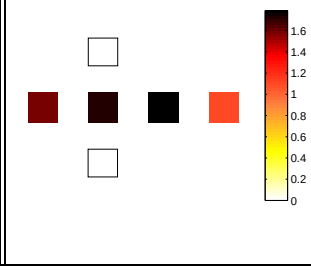
We consider arrangements of QCA cells implementing crucial QCA circuit elements. In Table 4.2. for each circuit, we visualize the energy dissipated at each cell, averaged over different input transitions. We use grayscale shading to visualize the dissipation at each cell – darker the cell, more the dissipation. We will refer to this kind of visualization as the *thermal layout*. Note that the dissipation scale for each circuit is different. We can clearly see that not all the cells of the circuits dissipate same amount of energy.

In addition to the energy dissipation, averaged over all input combinations, we also show the maximum dissipation over all input conditions and the minimum dissipation over all input conditions. The minimum energy dissipation case is when the input cells do not switch. These three quantities convey some idea about the overall variability of the dissipation with input. We have tabulated these results for three values of $E_k$.

The number of cells in the table refer to the number of cells that participate in energy dissipation. We do not include input cells in calculating the total energy dissipation. We can see, that in case of a clocked majority gate shown in Table 4.2.(a) even though the total energy dissipated is much higher than that of an inverter shown in Table 4.2.(b), weak spots in the inverter design dissipate higher amount of energy than in a majority logic. This is evident from the scale associated with the color code. Hence the inverter design is more susceptible to thermal breakdown.

We can also see that even though the energy dissipated for the circuits listed in Table 4.2. greatly depends on the number of cells for each design, still the average (over all input

Table 4.2. Thermal layout visualizing the energy dissipated at each cell averaged over different input transitions for some basic QCA logic elements. Darker the color, more the dissipation.

| | (a) Clocked Majority | | | (b) Inverter | | | (c) Crossbar | | |
|---|---|---|---|---|---|---|---|---|---|
| No. of Cells | 16 | | | 9 | | | 10 | | |
| Thermal Layout at $\gamma/E_K$=0.5 (Energy Dissipation scale is in terms of $10^{-3}$ eV) |  | | |  | | |  | | |
| $\gamma/E_K$ | 0.5 | 1.0 | 1.5 | 0.5 | 1.0 | 1.5 | 0.5 | 1.0 | 1.5 |
| Avg $E_{diss}$(meV) | 32.91 | 39.10 | 47.48 | 17.41 | 21.26 | 26.16 | 17.58 | 26.01 | 35.70 |
| Max $E_{diss}$(meV) | 71.99 | 73.84 | 77.76 | 31.76 | 33.54 | 36.58 | 28.52 | 33.67 | 41.36 |
| Min $E_{diss}$(meV) | 4.27 | 13.86 | 25.49 | 3.06 | 8.97 | 15.75 | 6.97 | 18.37 | 29.98 |
| | (d) Simple Majority | | | (e) AND Gate | | | (f) OR Gate | | |
| No. of Cells | 3 | | | 4 | | | 4 | | |
| Thermal Layout at $\gamma/E_K$=0.5 (Energy Dissipation scale is in terms of $10^{-3}$ eV) |  | | |  | | |  | | |
| $\gamma/E_K$ | 0.5 | 1.0 | 1.5 | 0.5 | 1.0 | 1.5 | 0.5 | 1.0 | 1.5 |
| Avg $E_{diss}$(meV) | 5.99 | 7.19 | 8.78 | 6.20 | 8.09 | 10.46 | 6.20 | 8.09 | 10.46 |
| Max $E_{diss}$(meV) | 14.71 | 15.03 | 15.70 | 18.72 | 18.61 | 19.21 | 18.72 | 18.61 | 19.21 |
| Min $E_{diss}$(meV) | 0.75 | 2.46 | 4.57 | 0.99 | 3.30 | 6.16 | 0.99 | 3.30 | 6.16 |

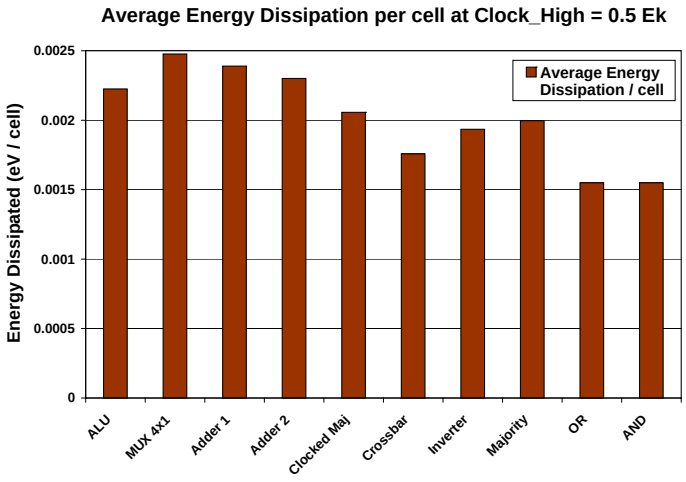


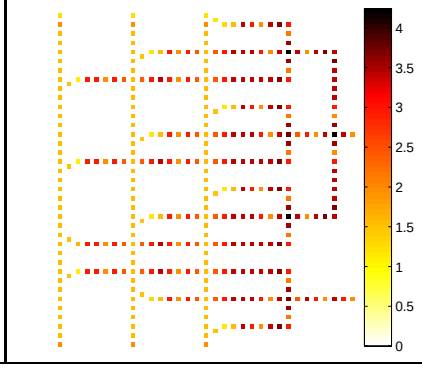
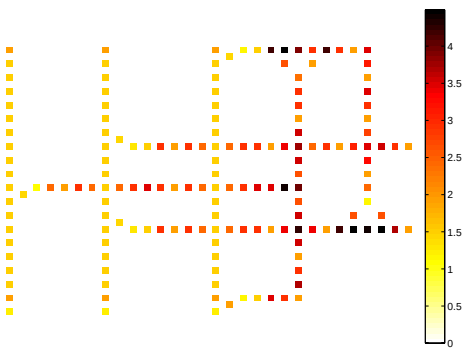

Figure 4.5. Energy dissipation bounds per cell for different QCA logic elements, averaged over different input combinations. The number of cells for each circuit refers to the number of cells that dissipate energy during a switching event. The graph shown here is for $\gamma/E_K$ = 0.5. Note that the color mapping scale for each circuit is different.

combinations) energy dissipation *per cell* for clocked majority gate, inverter, crossbar and simple majority gate does not vary greatly as can be seen from the graph shown in Fig 4.5.

### 4.5.3 Energy Dissipation per Clock Cycle in QCA Adder Circuits

Table 4.3. shows the comparative study of energy dissipated in two different QCA adders designs. As we can see from the table, Adder-1 has much higher energy dissipation, as it has 359 energy dissipating QCA cells present in its layout as compared to Adder-2 design that has only 165 such cells. We can see from the table that thermal energy layout for each design shows that the highest average energy dissipation for any particular cell in both designs is almost the same, even though the Adder-2 design has comparatively larger number of such 'high energy dissipation' dissipating cells present in its layout. We can also see from the graph in Fig. 4.5. that even though the total energy dissipation for both designs may vary greatly, still the average (over all input) power dissipation *per cell* is almost the

Table 4.3. Thermal layout visualizing the energy dissipation at each cell, averaged over all possible input combinations for two QCA adder designs.

| | (a) Adder 1 | | | (b) Adder 2 | | |
|---|---|---|---|---|---|---|
| No. of Cells | 359 | | | 165 | | |
| Thermal Layout at $\gamma/E_K$=0.5 (Energy Dissipation scale is in terms of $10^{-3}$ eV) |   | | |   | | |
| $\gamma/E_K$ | 0.5 | 1.0 | 1.5 | 0.5 | 1.0 | 1.5 |
| Avg $E_{diss}$ (meV) | 857.74 | 1110.45 | 1421.66 | 379.56 | 499.44 | 645.18 |
| Max $E_{diss}$ (meV) | 1524.42 | 1655.32 | 1868.33 | 671.80 | 736.98 | 840.29 |
| Min $E_{diss}$ (meV) | 203.82 | 576.53 | 984.33 | 97.42 | 271.06 | 458.34 |

same for both designs. For both designs, the maximum energy dissipation occurred when the input combinations switched from 000→111.

This result seem to be interesting because it has been already shown in [27] that Adder-2 design is more prone to error than Adder-1 design. Whereas, we can see that when it comes to power, Adder-2 is more energy efficient even though it has more hot-spots present in its layout.

### 4.5.4 Energy Dissipation per Clock Cycle in Large QCA Circuits

In order to demonstrate that this work is applicable to even larger designs, we also present the results for a 4x1 multiplexer and a single bit ALU designs. The ALU design consists of over 800 QCA cells. Fig. 4.6. shows the thermal layout for average power dissipated at each cell in a 4x1 multiplexer design and Fig. 4.7. shows the thermal layout for a single bit adder design. We can clearly see the thermal hot-spots in both designs. These hot spots dissipate large power, averaged over all input combinations, and in order to make the designs less susceptible to thermal breakdowns, designers can target these weak spots in the design for further reinforcements. The fabrication scientists can also use these results to select different types of devices.

In order to evaluate the multiplexer and ALU design we ran a simulation to model all possible input vector combinations and determine the average power dissipation over all possible input vector set transitions. In case of 4x1 multiplexer there were 6 inputs and hence we have a vector set comprising of 64 input vectors. In case of ALU since there are seven inputs, hence we have 128 possible input combinations. Table 4.4. shows the average (over all input combinations), maximum (over all input combinations), and minimum (over all input combinations) power dissipation bounds for these designs at $\gamma = 0.5E_K$, $\gamma = 1.0E_K$ and $\gamma = 1.5E_K$. Since the ALU design has much larger number of cells as compared to the multiplexer design, it obviously dissipates more energy compared to the multiplexer. It can

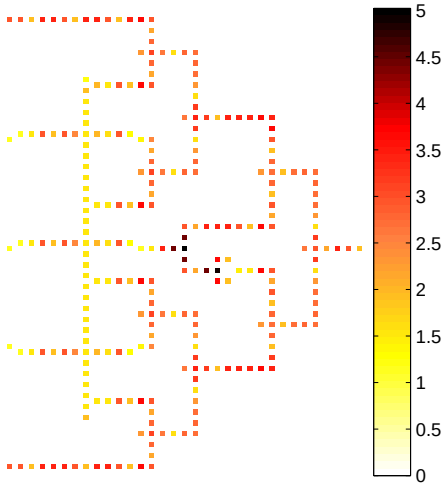



Figure 4.6. Thermal Layout for average energy dissipated in each cell of a 4x1 MUX circuit. The dark spots are the ones that dissipate larger amount of energy on an average. The layout was obtained by simulating over all possible input switching combinations from 000000 $\rightarrow$ 111111 for $\gamma/E_K$ = 0.5. The energy dissipation scale for each cell is in terms of $10^{-3}$ eV.

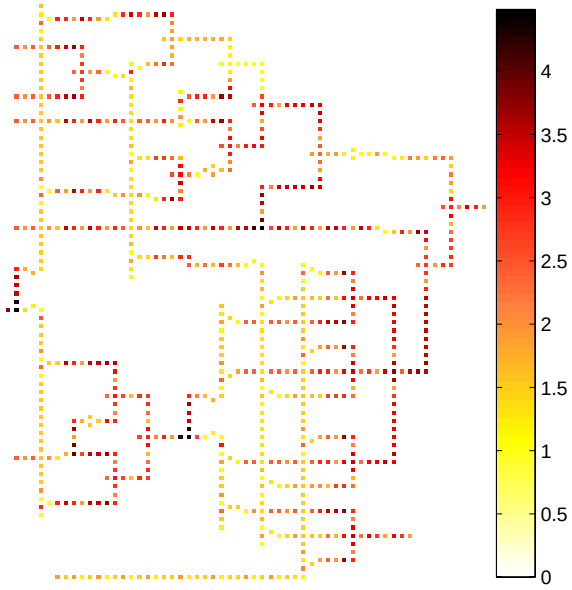


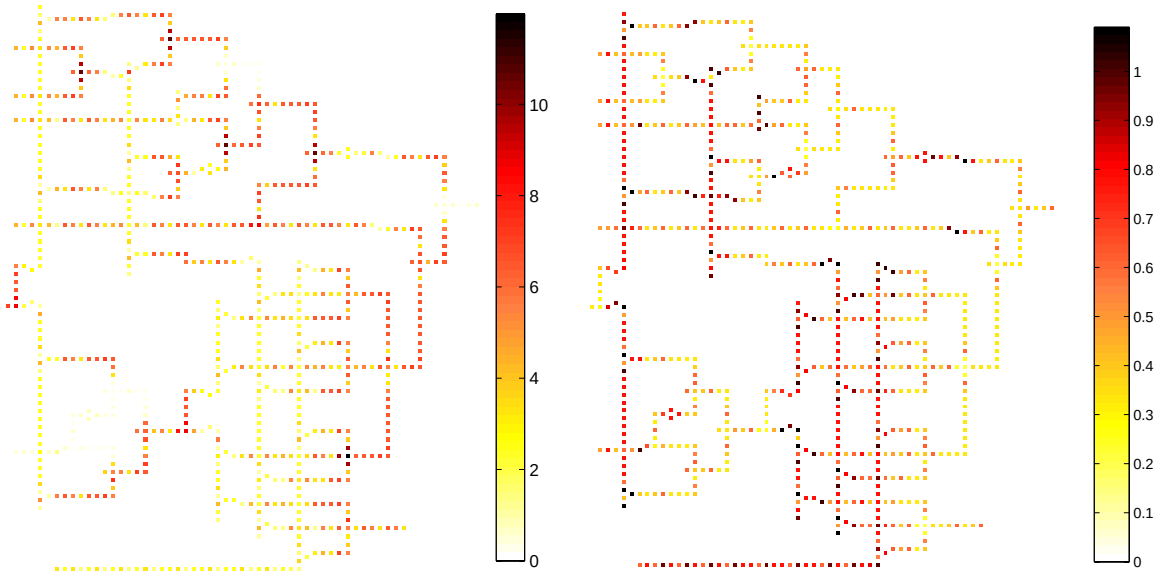

Figure 4.7. Thermal Layout for average energy dissipated in each cell of a single bit ALU circuit. The dark spots are the ones that dissipate larger amount of energy on an average. The layout was obtained by simulating over all possible input switching combinations from 0000000 $\rightarrow$ 1111111 for $\gamma/E_K$ = 0.5. The energy dissipation scale for each cell is in terms of $10^{-3}$ eV.

Table 4.4. Statistics of the energy dissipation per cell for a 4x1 MUX and a single bit ALU over all possible input combinations and for different possible clock energies. We show the average, maximum, and minimum energy per cell over all input combinations.

| | (a) Single Bit ALU | | | (b) 4x1 MUX | | |
|---|---|---|---|---|---|---|
| No. of Cells | 801 | | | 270 | | |
| $\gamma/E_K$ | 0.5 | 1.0 | 1.5 | 0.5 | 1.0 | 1.5 |
| Avg $E_{diss}$ (meV) | 1781.97 | 2370.33 | 3083.37 | 668.67 | 850.92 | 1080.00 |
| Max $E_{diss}$ (meV) | 3192.91 | 3525.86 | 4030.15 | 1174.97 | 1274.37 | 1432.77 |
| Min $E_{diss}$ (meV) | 456.62 | 1279.19 | 2185.83 | 136.69 | 404.03 | 707.49 |

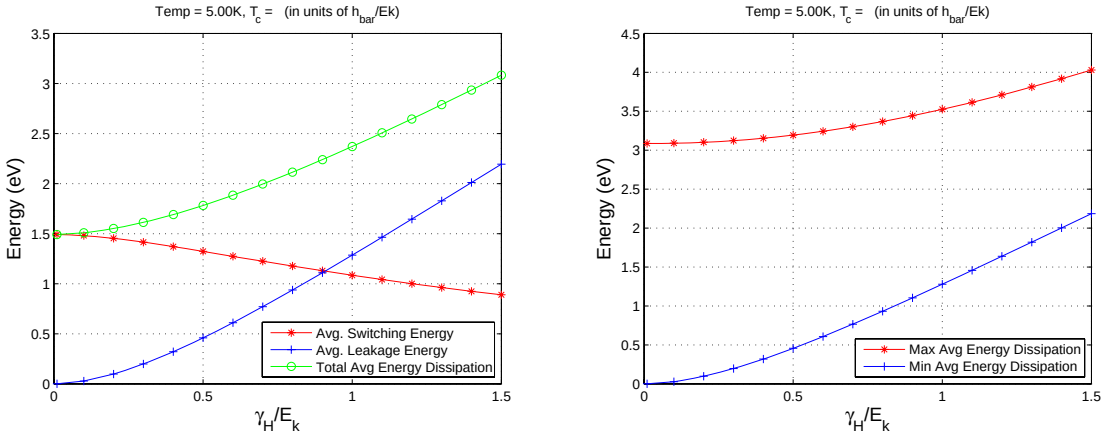
be seen that the per cell energy dissipation still remains more or less the same for both designs (in Fig. 4.5.). We also see from the thermal layout of the two designs that some of the cells in multiplexer dissipate much higher energy on an average than any cell in the ALU design.

Apart from calculating the thermal layout for the average energy dissipation in an ALU design, we also studied the thermal energy layout in case of maximum and minimum energy, over all input transitions. In Fig 4.8.(a) and (b) we show the thermal layout of ALU circuit for the maximum and minimum energy dissipation cases, respectively. The dark spots are the ones that dissipate larger amount of energy. The layout was obtained by simulating worst case and best case input switching vectors at $\gamma/E_K$ = 0.5. The energy dissipation scale in Fig 4.8.(b) is much smaller than that in Fig 4.8.(a) since energy is dissipated only due to leakage component and hence is much less than Fig 4.8.(a) where switching energy plays a dominant role in total energy dissipation of a cell. It can be clearly seen from the layouts that the energy dissipated in almost all cells of Fig. 4.8.(a) is more than that of cell dissipating highest energy in Fig 4.8.(b) On an average each cell in Fig 4.8.(a) dissipates a magnitude higher energy than that in case of Fig 4.8.(b) The reason behind this is that in case of minimum power dissipation, none of the input cells switch state. And the total energy dissipated at each cell in this case is only the leakage energy (which




(a) (b)

Figure 4.8. Thermal Layout for energy dissipated in each cell of an ALU circuit for (a) Maximum energy dissipating input combination and (b) for least energy dissipating input combination. Energy dissipation scale is in multiples of $10^{-3}$.




(a) (b)

Figure 4.9. Graphs showing energy dissipated in a QCA ALU circuit (a) Shows the variation of leakage and switching components of energy dissipated for various values of $\gamma/E_K$ (b) Shows the variation in maximum and minimum energy dissipated for various values of $\gamma/E_K$

is quite low compared to the switching component of energy). However, this conclusion is not valid for higher clock energies.

In Fig. 4.9.(a) we plot the variation of the dissipation (averaged over all input transitions) with clock energy. We see that switching component of energy reduces when we increase the clock energy, but the leakage component increases much more significantly, resulting in overall increase in power dissipation. At $\gamma \approx 0.9E_K$, the leakage component of energy and switching component contribute equally to the total energy dissipation of the circuit. Beyond this value of $\gamma$, the leakage component of energy dissipation contributes more than the switching component towards total energy dissipation. This result will be of great use to designers or even circuit fabricators to choose the most optimum clock energy to be supplied to a QCA circuit. Fig 4.9.(b) shows the variation of maximum and minimum energy dissipation in a QCA ALU design with respect to the clock energy. We can see that while it is desirable to have higher clock energy in order to reduce errors in QCA operation, it can be seen clearly from the results that if the clock energy is raised significantly, the energy dissipation is high.

# CHAPTER 5

# HIERARCHICAL DESIGN IN QCA USING PROBABILISTIC MACROMODELING

## 5.1 Introduction

Time is ripe to look beyond just device level research in emerging devices such as QCA and explore circuit level issues so as to scope out the types of circuits that can be built [133, 86, 134, 87, 110, 111]. However, QCA modeling tools available for such designs have been at the layout level. There are several approximate simulators available at the layout level, such as the bistable simulation engine and the nonlinear approximation methods [135, 136, 42]. These methods are iterative and do not produce steady state polarization estimates. In other words, they estimate just state assignments and not the probabilities of being in these states. The coherence vector based method [126, 42] does explicitly estimate the polarizations, but it is appropriate when one needs full temporal dynamics simulation (Bloch equation), and hence is extremely slow; for a full adder design with about 150 cells it takes about 500 seconds for 8 input vectors. Perhaps, the only approach that can estimate polarization for QCA cells, without full quantum-mechanical simulation is the thermodynamic model proposed in [121], but it is based on semi-classical Ising approximation. In [24, 137, 25], it was shown that layout-level QCA cell probabilities can be modeled using Bayesian probabilistic networks.

To advance design with QCA, it is necessary to look beyond the layout level. Hierarchical design at multiple levels of abstraction, such as architectural, circuit, layout, and device levels, has been a successful paradigm for the design of complex CMOS circuits. It

is only natural to seek to build a similar design structure for emerging technology. Henderson *et al.* [26] proposed an hierarchical CMOS-like top-down approach for QCA blocks that are analyzed with respect to the output logic states; this is somewhat similar to functional logic verification performed in CMOS. We also advocate building an hierarchical design methodology for QCA circuits. However, such an hierarchy should be built based on not just the functionality of the circuit, but it should also allow the abstraction of important nano-device parameters. It is not sufficient just to abstract a QCA circuit in terms of 0-1 boolean logic based majority gates and other logic components, we have to also represent the probabilistic nature of the operations. Thus, for each logic variable $X$, we have to assign the probabilities associated with the logic values, i.e. $P(X = 1)$ or $P(X = 0)$. In the parlance of QCA, the specific design variable is the "polarization" of cell, which is $P(X = 1) - P(X = 0)$. These probabilities (or polarizations), which are governed by quantum mechanics, are dependent on temperature, which is an important design variable for QCAs that needs to be represented at upper design levels. Another need for probabilistic representations arise due to the nature of the QCA operations. QCA circuits are designed so that the intended logic is mapped to the lowest-energy (ground state) of the cell arrangement. So, it is important that the circuit be kept near ground state during operations, using mechanisms such as four-phased adiabatic clocking. Logical errors in QCA circuits can arise due to the failure to the settle to the ground state. It is important to compute the difference between the probability of lowest-energy state configuration that results in *correct* output and the lowest-energy state configuration that results in *erroneous* output. It would indeed be useful to be able to compute these erroneous configurations at higher levels of design. Building a device-level characterization sensitive macromodel will facilitate answering the following kinds of questions at higher design levels of abstraction itself. What is expected polarization of the outputs? How does it change with temperature? How sensitive is the design with respect to operational errors?

In this chapter [27, 28], we formulate a probabilistic framework for higher level of abstraction of QCA circuits that would enable one to characterize designs with respect to thermal profiles and errors, the two most important design issues in nano-circuit design. Standard QCA circuit elements such as majority logic, lines, wire-taps, cross-overs, inverters, and corners are represented using conditional probability distributions defined over the output states *given* the input states. The probabilistic macromodels allow us to model QCA circuits at an abstract level above the current practice of layout level; we term this higher level as the "circuit" level. The full circuit level model is constructed by chaining together the individual logic element macromodels. This circuit represented using the graphical probabilistic models known as Bayesian networks, where the nodes of the graphs are the individual macromodels and the links represent the connection between them. The nodes are quantified by the macromodel conditional probabilities. The complete network represents a joint probability distribution over the whole circuit. Since conditional distribution over the inputs and outputs are obtained based on quantum mechanical probabilistic characterization, the circuit level model is also faithful to the underlying quantum-mechanical phenomena.

Computations using the macromodel translates to different kinds of probabilistic inference problems. For instance, computation of ground state polarization is done using the *average* likelihood propagation on the built Bayesian network macromodel. Similarly, the most-likely configuration of the internal nodes corresponding to first-excited, also called near-ground state or the most likely error state at the outputs, can be isolated at the macromodel circuit level itself using *maximum* likelihood propagation on the same Bayesian network macromodel. We demonstrate and validate our model using commonly studied QCA circuits and elements, whose behaviors are pretty well understood by others. First, we show that the ground state polarization probabilities of the output nodes as well as the intermediate nodes in the macromodel of the QCA logic circuit closely match with those

obtained from a full layout level implementation [24] at different temperatures. We show examples of characterization of thermal behavior of a QCA logic circuit that can be carried out. Second, we demonstrate that both the ground and the next excited (error) state configuration of the macromodel exactly match the corresponding configurations of the detailed layout cells. The mismatch between the ground and the next excited error state configuration can be used to identify weak spots in circuit design. Using the macromodel, this can now be done at an higher level of abstraction. Isolation of error-prone components would be useful in applying redundancy selectively to the necessary components rather than to the whole circuit. Third, we use the circuit level implementation to vet between alternate design choices. We show examples of this design space exploration process with the example of two adders. We find that one adder design, Adder-1, in spite of its larger area, is better in terms of polarization which is an extremely important measure for the QCA circuits. Also, we see that for Adder-1, number of error-prone components is less than a second adder design, Adder-2, and hence the needed redundancy measures would be less for Adder-1.

The organization of this chapter is as follows. In Section 5.2, we begin by explaining the hierarchical modeling scheme used in this work. Then we proceed in subsection 5.2.1 to summarize the quantum-mechanical nature of the probabilities associated with the QCA cells. In Section 5.2( 5.2.2), we show how an arrangement of QCA cells can be modeled by a joint probability function, represented as a Bayesian network. Further down in Section 5.2( 5.2.3) we present the theory behind the macromodels. We demonstrate how using these macromodels we can (i) model full circuits Section 5.2( 5.2.4), (ii) explore design space exploration in QCA circuit layouts (Section 5.4( 5.4.3)), and (iii) conduct error studies (Section 5.3). We comment on the computational advantage of the circuit level representation over the layout level one in Section 5.4 and we conclude with Section 7.

## 5.2 Modeling Theory

In this section, we explain the hierarchical modeling scheme. We focus on two levels: the layout level and the circuit level, where groups of QCA cells, corresponding to a basic logic element, are represented as one macroblock. For both these levels, we will use the graphical probabilistic model called Bayesian Networks to represent the underlying joint probability of the entire set of nodes. Note that probabilistic representation is essential to capture the inherently uncertain nature of the computing with QCAs.

Bayesian Networks[122] are efficient representations of the joint probability distribution over a set of random variables using a Directed Acyclic Graph (DAG). Each random variable of interest is represented as a node and links between the nodes denote direct dependencies (cause-effect interactions) between the random variables. For our problem, the random variables are the states of the QCA cells at the layout level or the I/O states of the macromodels. The links are guided by the interaction neighborhood of the cells and the logical flow of information from inputs to the outputs. For QCA circuits these cause-effect directions would be determined by direction of propagation of quantum-mechanical information propagation with change in input. Clocks determine the causal order between cells. Within each clock zone, ordering is determined by the direction of propagation of the wave function [36]. Since the Coulombic interaction between cells fall off faster than the fifth power of the distance between them, we need to consider links between cells that are within a small neighborhood of each other, typically 2 cell distance.

In Fig 5.1.(a), we show the QCA layout of a NAND gate. Fig 5.1.(b) shows the layout level Bayesian representation. Note that we have 18 random variables representing the state of 18 QCA cells. Fig 5.1.(c) shows the circuit level abstraction of a NAND gate. The Bayesian representation of circuit level abstraction as shown in Fig. 5.1.(d) has fewer cells. Note that each node at the circuit level is the collection of cells from the layout level.

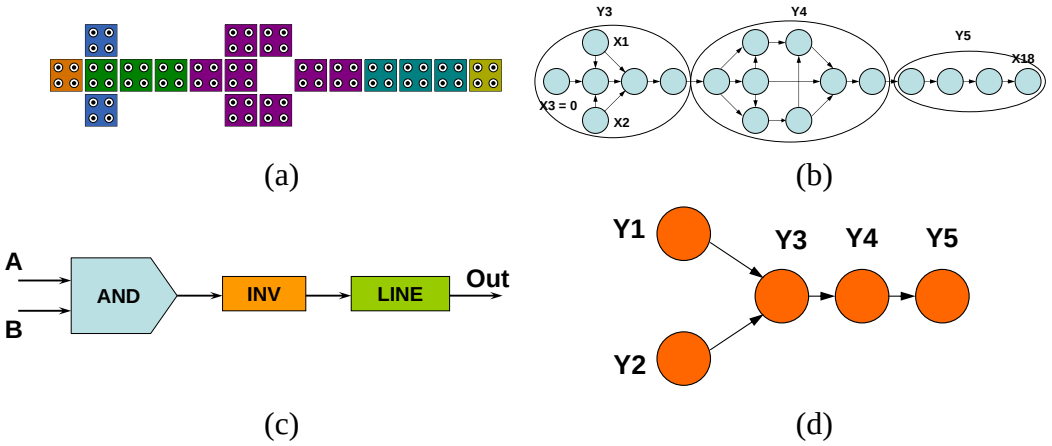



Figure 5.1. A NAND logic gate (a) QCA layout (b) Bayesian model of QCA layout (c) Macromodel block diagram (d) Bayesian network of macromodel block diagram.

In this work, we will use $X$ to represent the random variable denoting the states of a QCA cell at the layout level (Fig. 5.1.(b)). The input cell states will be denoted by $X_1, \cdots, X_r$, the non-input QCA cells will be $X_{r+1}, \cdots X_N$ and $X_s$ will denote one of the output cell where $r+1 \geq s \geq N$. Similarly for the circuit level, we will use $Y$ to represent the random variable denoting the line states. The $Y_1, \cdots, Y_r$ are set of input cells, $Y_{r+1}, \cdots Y_M$ are the non-input QCA cells and $Y_s$ denotes one of the output cell where $r+1 \geq s \geq M$.

The nodes of the Bayesian network are quantified by the conditional probabilities. At the layout level, we need to specify the conditional probability of the state of a cell given the states of parent neighbors, i.e. $P(x|pa(X))$ where $Pa(X)$ are the direct causes of the random variable $X$ or the parents of the node $X$ in the directed graph representation. We use lowercase to indicate value of a random variable. i.e. $P(x)$ denotes the probability of the event $X = x$ or $P(X = x)$. We estimate this using the quantum mechanical modeling of QCA cells. At the circuit level, we need to specify the conditional probability of the output states of a macromodel given the states of the inputs, $P(y|Pa(Y))$. These conditional probabilities are estimated from the conditional probabilities for in the layout level model of the QCA cells comprising the macromodel, at different temperatures.

In general, a Bayesian network encodes the joint probability function as a set of factored conditional probabilities, of minimal representational complexity. Proof of minimality can be found in standard Bayesian network texts such as [122].

$$P(x_1, \cdots, x_n) = \prod_{k=1}^{m} P(x_k | pa(x_k)) \tag{5.1}$$

In the conditional probability term $P(x|pa(X))$, $pa(X)$ represents the values taken on by the parent set, $Pa(X)$.

Inference or computation with Bayesian networks exploits the sparsely connected graph structure. The most common schemes involve passing messages among the nodes. As we shall see, for we will need to conduct both average case and maximum likelihood inferences. For both the *average* and *maximum* likelihood propagation, we adopt the cluster based exact inference scheme. We refer the reader to [122, 138, 137] for details on the inference scheme. However, it suffices to note that the propagation schemes are based on message passing and are similar, differing only in the kinds of messages that are passed. The original Bayesian network, which is a DAG structure, is first transformed into a junction tree of cliques and then marginal probabilities are computed by local message passing between the neighboring cliques. These methods result in exact inference of probabilities.

In the rest of this section, we provide details of the process. We start with discussion of the macromodel construction process by the Bayesian network model at the layout level, which was proposed in [137]. Then, we present the construction of the macromodels and circuit level Bayesian representation.

### 5.2.1 Quantum Mechanical Probabilities

We sketch how the state probabilities of a QCA cell are dependent on the state probabilities of its layout neighbors, distance to the neighbors, and temperature. Each cell has 2 electrons that can occupy 4 possible dots. Among all the possible occupancy configurations, there are two lowest energy configurations corresponding to the diagonal occupancy of the cells. These represent the two logical states, 0 or 1. So, following Tougaw and Lent [36] and other subsequent works on QCA, we use the two-state approximate model of a single QCA cell. We denote the two possible, orthogonal, eigenstates of a cell by $|1\rangle$ and $|0\rangle$. The state at time $t$, which is referred to as the wave-function and denoted by $|\Psi(t)\rangle$, is a linear combination of these two states, i.e. $|\Psi(t)\rangle = c_1(t)|1\rangle + c_2(t)|0\rangle$. Note that the coefficients are function of time. The expected value of any observable, $\langle\hat{A}(t)\rangle$, can be expressed in terms of the wave function as $\langle\hat{A}\rangle = \langle\Psi(t)|\hat{A}(t)|\Psi(t)\rangle$ or equivalently as $\mathrm{Tr}[\hat{A}(t)|\Psi\rangle(t)\langle\Psi(t)|]$, where Tr denotes the trace operation, $\mathrm{Tr}[\cdots] = \langle 1|\cdots|1\rangle + \langle 0|\cdots|0\rangle$. The term $|\Psi(t)\rangle\langle\Psi(t)|$ is known as the density operator, $\hat{\rho}(t)$. Expected value of any observable of a quantum system can be computed if $\hat{\rho}(t)$ is known.

A 2 by 2 matrix representation of the density operator, in which entries denoted by $\rho_{ij}(t)$ can be arrived at by considering the projections on the two eigenstates of the cell, i.e. $\rho_{ij}(t) = \langle i|\hat{\rho}(t)|j\rangle$. This can be simplified further.

$$\begin{aligned} \rho_{ij}(t) &= \langle i|\hat{\rho}(t)|j\rangle \\ &= \langle i|\Psi(t)\rangle\langle\Psi(t)|j\rangle = (\langle i|\Psi(t)\rangle)(\langle j|\Psi(t)\rangle)^* \\ &= c_i(t)c_j^*(t) \end{aligned} \tag{5.2}$$

The density operator is a function of time and using Loiuville equations we can capture the temporal evaluation of $\rho(t)$ in Eq. 5.3.

$$\hbar\frac{\partial}{\partial t}\rho(\mathbf{t}) = \mathbf{H}\rho(\mathbf{t}) - \rho(\mathbf{t})\mathbf{H} \tag{5.3}$$

where H is a 2 by 2 matrix representing the Hamiltonian of the cell and using Hartree approximation. Expression of Hamiltonian is shown in Eq. 5.4 [36].

$$\mathbf{H} = \begin{bmatrix} -\frac{1}{2}\sum_i E_k P_i f_i & -\gamma \\ -\gamma & \frac{1}{2}\sum_i E_k P_i f_i \end{bmatrix} = \begin{bmatrix} -\frac{1}{2}E_k\bar{P} & -\gamma \\ -\gamma & \frac{1}{2}E_k\bar{P} \end{bmatrix} \tag{5.4}$$

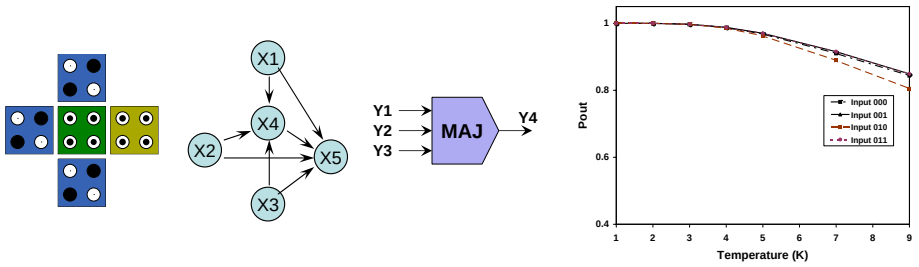
where the sums are over the cells in the local neighborhood. $E_k$ is the "kink energy" or the energy cost of two neighboring cells having opposite polarizations. $f_i$ is the geometric factor capturing electrostatic fall off with distance between cells. $P_i$ is the polarization of the $i$-th cell. And, $\gamma$ is the tunneling energy between two cell states, which is controlled by the clocking mechanism. The notation can be further simplified by using $\bar{P}$ to denote the weighted sum of the neighborhood polarizations $\sum_i P_i f_i$. Using this Hamiltonian the steady state polarization is given by

$$P^{ss} = -\lambda_{\mathbf{3}}^{\mathbf{ss}} = \rho_{11}^{ss} - \rho_{00}^{ss} = \frac{E_k\bar{P}}{\sqrt{E_k^2\bar{P^2} + 4\gamma^2}}\tanh\left(\frac{\sqrt{E_k^2\bar{P^2}/4 + \gamma^2}}{kT}\right) \tag{5.5}$$

Eq. 5.5 can be written as

$$P^{ss} = \frac{E}{\Omega}\tanh(\Delta) \tag{5.6}$$

where $E = 0.5\sum_i E_k P_i f_i$, the total kink energy, $\Omega = \sqrt{E_k^2\bar{P^2}/4 + \gamma^2}$, the Rabi frequency, and $\Delta = \frac{\Omega}{kT}$ is the thermal ratio. We use the above equation to arrive at the probabilities of observing (upon making a measurement) the system in each of the two states. Specifically, $P(X=1) = \rho_{11}^{ss} = 0.5(1+P^{ss})$ and $P(X=0) = \rho_{00}^{ss} = 0.5(1-P^{ss})$, where we made use of the fact that $\rho_{00}^{ss} + \rho_{11}^{ss} = 1$.




(a) (b) (c) (d)

Figure 5.2. Majority logic (a) QCA cell layout (b) Bayesian network model (c) Macromodel (d) Probability of the *correct* output value for a 5 cell majority gate at different temperatures and for different inputs.

### 5.2.2 Layout Level Model of Cell Arrangements

To enable us to form macromodels of various cell arrangements, we need to represent the joint state probabilities of a collection of cells at the layout level. In this section, we summarize how this joint probability can be efficiently represented using Bayesian networks, as shown in [137, 24]. We will use the majority logic arrangement of QCA cells in Fig. 5.2.(a) to illustrate the process.

Each cell is represented by a random variable, taking on two possible values, shown in the Bayesian network in Fig. 5.2.(b). Each node in the network has a conditional probability table (CPT), capturing the probabilities of that node, given the states of the parent (cause) nodes. For example, the center node $X4$, will be associated with the conditional probability $P(x4|x1,x2,x3)$. The product of these CPTs determine the joint probability distribution over all the variables in the network. Thus, the joint probability $P(x1,x2,x3,x4,x5) = P(x4|x1,x2,x3)P(x5|x4,x3,x2,x3)$. The polarization of the output cell $X5$ is a function of the remaining four cells in the layout. The center node $X4$ is actually the one which gets polarized based on the majority of inputs. The output cell depicted here receives the polarization of the central cell $X4$ and also the three inputs, $X1$, $X2$, and $X3$. The

interaction between the output cell and the central cell will be much more than the inputs. This is because the kink energy (which determines the amount of interaction between two neighboring cells), decays as the fifth power of distance.

For a given set of possible parent node assignments, the conditional probability values are computed using the Hartree-Fock approximation, applied locally. The parent states are constrained to be as specified in the required conditional probability. We fix the children states (or polarization) so as to maximize $\Omega = \sqrt{E_k^2 \bar{P^2}/4 + \gamma^2}$, which would minimize the ground state energy over all possible ground states of the cell. Thus, the chosen children states are

$$ch^*(X) = \arg\max_{ch(X)} \Omega = \arg\max_{ch(X)} \sum_{i \in (Pa(X) \cup Ch(X))} E_k \bar{P} \tag{5.7}$$

The steady state density matrix diagonal entries (Eq. 5.6 with these children state assignments are used to decide upon the conditional probabilities in the Bayesian network (BN).

$$\begin{aligned} P(X = 0 | pa(X)) &= \rho_{00}^{ss}(pa(X), ch^*(X)) \\ P(X = 1 | pa(X)) &= \rho_{11}^{ss}(pa(X), ch^*(X)) \end{aligned} \tag{5.8}$$

Note that once the conditional probabilities between the nodes and its parents are obtained the Bayesian Network is quantified completely. Some of the important parameters used in this model that effect the polarization of a cell apart from temperature are: *relative permitivity = 12.9, radius of effect = 4, cell dimension = 20nm, cell to cell pitch = 10nm,* $CLOCK\_HIGH = 6.1 * 10^{-2} eV$ *and* $CLOCK\_LOW = 1.9 * 10^{-15} eV$.

### 5.2.3 Macromodel

The basic circuit elements of a QCA circuit consists of typical logic elements, such as Majority, NAND, AND, OR, and NOT, and QCA specific elements such as wires and crossbars. The macromodels of different circuit elements are the conditional probability of

Table 5.1. Macromodel design blocks

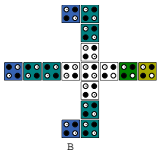
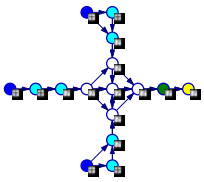
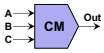
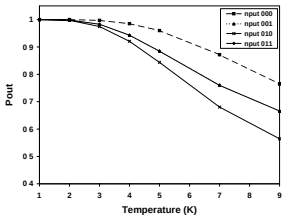
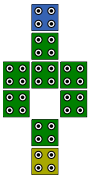
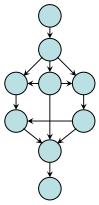
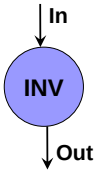
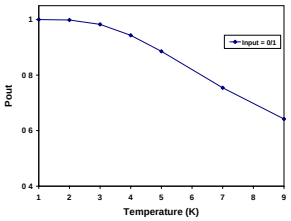
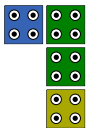
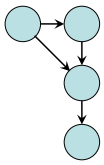
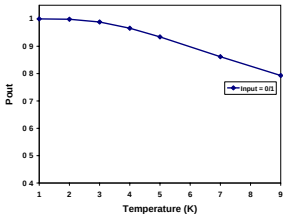
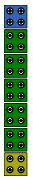
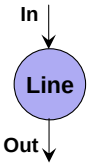
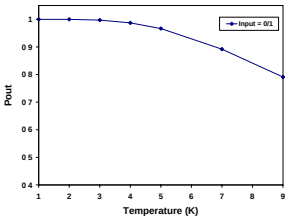
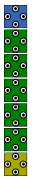
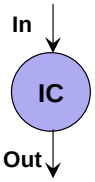
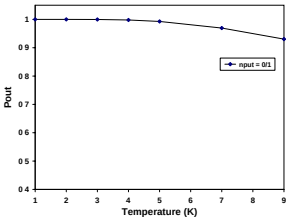
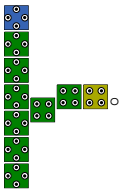
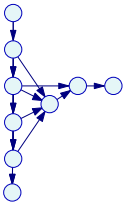
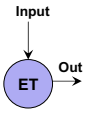
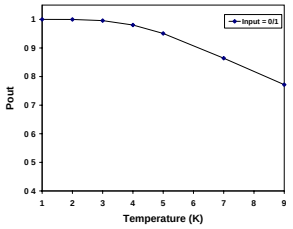
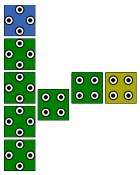
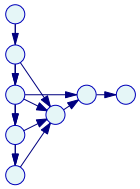
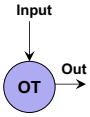
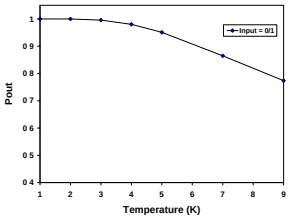
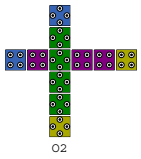
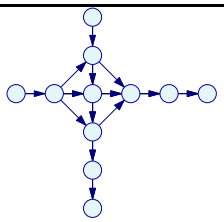
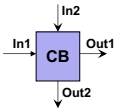
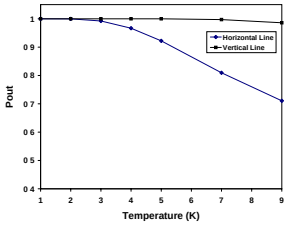
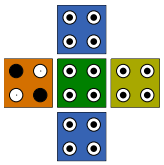
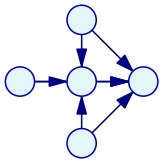
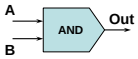
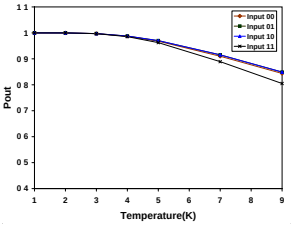
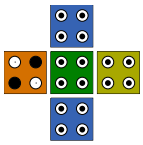
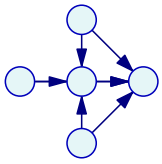
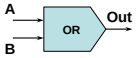
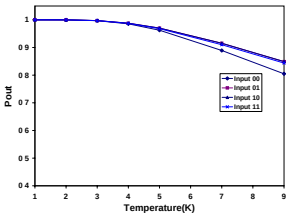
| Macromodel | QCA Layout | Bayesian Model | Block Diagram | Thermal Properties |
|---|---|---|---|---|
| (a) Clocked Majority |  |  |  |  |
| (b) Inverter |  |  |  |  |
| (c) Corner |  |  |  |  |
| (d) Line |  |  |  |  |
| (e) Inverter Chain |  |  |  |  |

Table 5.2. Macromodel design blocks

| Macromodel | QCA Layout | Bayesian Model | Block Diagram | Thermal Properties |
|---|---|---|---|---|
| (a) Even Tap |  |  |   |   |
| (b) Odd Tap |  |  |   |   |
| (c) Cross-bar |   |  |   |   |
| (c) And Gate |  |  |   |   |
| (c) OR Gate |  |  |   |   |

output cells given the values of the input cells. We compute this by marginalizing over the internal cells. The underlying premise of the macromodeling is that if the joint probability distribution function $P(x_1, \cdots, x_n)$ over all the $n$ cells in the layout is available, using the process outlined in the previous subsection 5.2.2, then we can always obtain the exact distribution over subset of cells by marginalizing the probabilities over rest of the variables. For instance, the joint probability over just three cells, $x_i, x_j,$ and $x_k$, can be obtained by

$$P(x_i, x_j, x_k) = \sum_{\forall x_m, m \neq i,j,k} P(x_1, \cdots, x_n) \tag{5.9}$$

Hence, at the circuit level, we do not represent all the $m$ internal cells. Note that at circuit level, we only represent $P(x_i, x_j, x_k)$ and represent them with different variable $Y$, which essentially captures the input-output dependence but is faithful to the layout level quantum interaction since the macromodel is built by marginalizing the layout level cells. This marginalizing is achieved by conducting *average* likelihood inference [122, 138] on the Bayesian network representation over all the cells in the macromodel unit. Note that Eq. 5.9 will yield different results at different temperatures and we store the conditional probabilities at various temperature points.

Fig. 5.2.(d) shows the thermal models for the majority gate in Fig. 5.2.(a). The macromodel probability distribution is defined over the output and the 3 input nodes. At a temperature of 1K, if inputs are 0, 0 and 0 then the probability of output node is at state 0 is "0.999963". As the temperature is increased, this probability decreases. We also notice that the thermal behavior is dependent on the input values. Note that, for correct operation, the probability of *correct* output should be greater than 0.5.

In the rest of this section, we present results for other basic building blocks: clocked majority gate (Table. 5.1.(a)),inverter (Table. 5.1.(b)), line (Table. 5.1.(c)), corner (Table. 5.1.(d)), inverter chain (Table. 5.1.(e)), even tap (Table. 5.2.(a)), odd tap (Table. 5.2.(b)),

crossbar (Table. 5.2.(c)), AND gate (Table. 5.2.(d)) and OR gate (Table. 5.2.(e)). For each macro-cell, we show the QCA layout, layout level Bayesian model, circuit level input-output relation and magnitude of polarization drop with temperature. All the conditional probabilities are stored at various point of temperatures.

We make three important observations. First, a clocked majority gate, which is necessary to synchronize all the input signals reaching the majority gate, has weaker polarization at higher temperature compared to the simple majority shown in Fig. 5.2.(d) as number of cells are higher in the clocked majority gate. Hence if inputs to a majority gate are arrive at the same time, then simple majority yields better polarizations at higher temperatures. Second, inverters have larger drop of polarization over the odd-tap structure at higher temperatures. Third, the crossbar structure, which allows two signal to cross each other in a coplanar way, has a different drop for the two signals.

### 5.2.4 Circuit Level Modeling

Table 5.3. lists all the symbols used for macromodel design blocks that we have used in our designs. A macromodel library stores the input-output characteristics (output node probabilities for each input vector set) of each macromodel block based on temperature. That means for each temperature, we have a library of macromodel blocks listed in the Table 5.3.. Once we know the logic components required to build a circuit, we simply extract the macromodel logic blocks and the required connectivity blocks (e.g. Line, Corner, Inverter Chain, etc.) from the library at a given temperature and use them to build the logic circuit. We form a Bayesian macromodel using the input-output probabilities of each block. The output from one macromodel block is fed to the input(s) of next macromodel block.

We illustrate the process using the full adder circuit, Adder-1, shown in Fig. 5.3.(a). It consists of five majority gates with no inverters. Fig. 5.3.(b) shows the corresponding

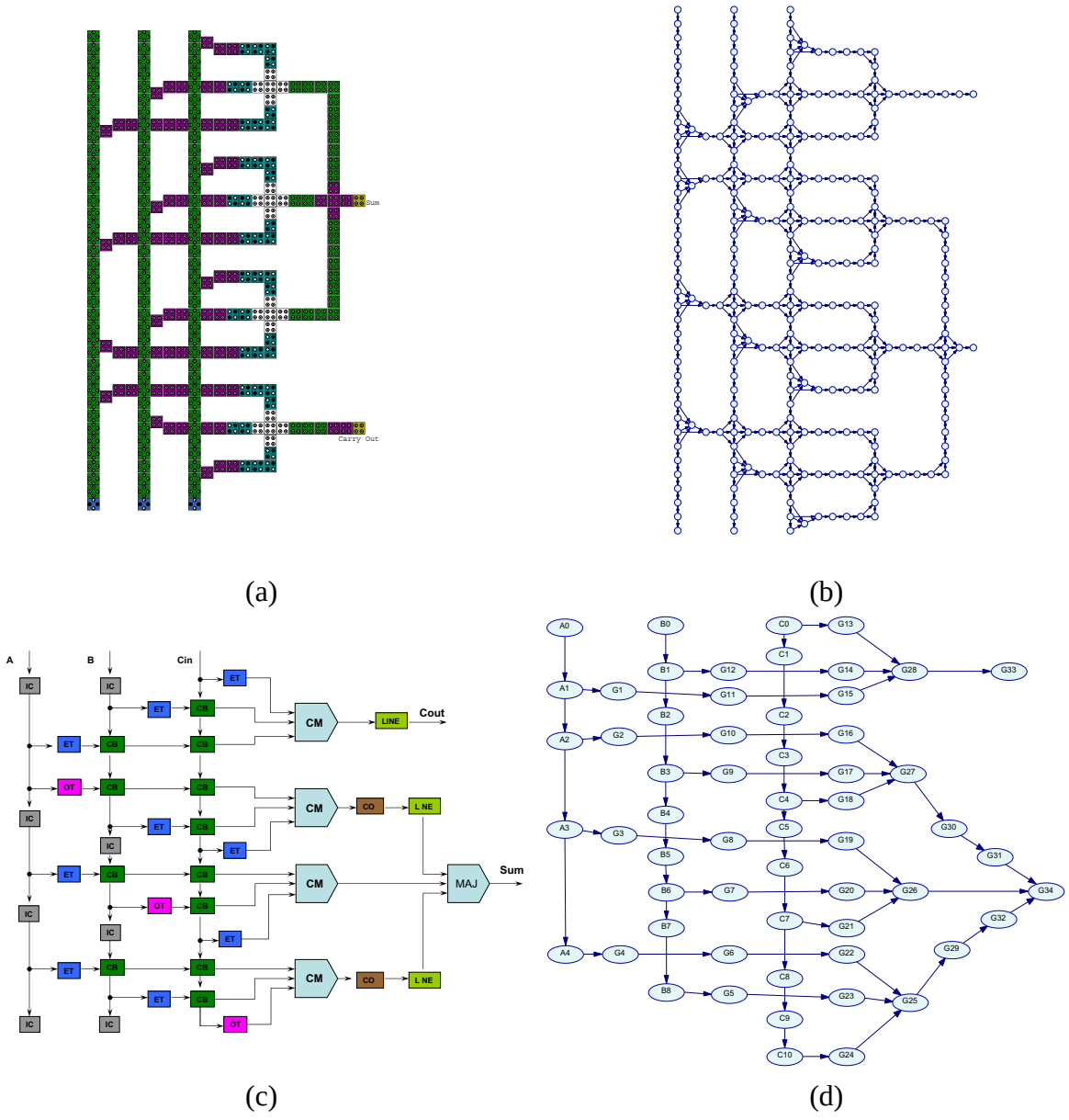



Figure 5.3. A full adder circuit (Adder-1) (a) QCA cell layout (b) Layout level Bayesian network representation. (c) Circuit level representation. (d) Circuit level Bayesian network macromodel. Note: Node elements are generic.

Table 5.3. Abbreviations used for Macromodel Blocks for designing QCA architectures of Full Adders and Multiplier

| Symbol | Macromodel |
|---|---|
| Maj | Simple Majority Gate |
| CM | Clocked Majority Gate |
| Inv | Inverter |
| Line | Line Segment |
| CO | Corner |
| IC | Inverter Chain |
| OT | Odd Tap |
| ET | Even Tap |
| CB | Crossover |
| AND | And Gate |
| OR | Or Gate |
| ZL | z-line |

layout level Bayesian network. We model the circuit level QCA macromodel shown in Fig. 5.3.(c) which is the circuit level abstraction of Fig. 5.3.(a). The Bayesian macromodel is shown in Fig. 5.3.(d). Each signal (node) can either be a primary input, or an output cell of a macroblock like line, inverter etc. The links are directed from the input to the output of each macroblock and are quantified by the device macromodels. Thus, we arrive at directed acyclic graph easily from the circuit model in Fig. 5.3.(c).

## 5.3 Error Computation

Apart of the computation of the polarization of each QCA cell or macromodel line, which we can arrive at by using *average* case propagation, another analysis of interest when comparing designs is the comparison of the least energy state configuration that results in correct output versus those that result in erroneous outputs. What is the probability of the minimum energy configuration that results in *error* at the output, $x_s$, for a given input assignment, $x_1, \cdots, x_r$? This can be arrived at by conditional maximum likelihood propagation. In essence, we compute $\arg\max_{x_1,x_2,\cdots,x_r} P(x_{r+1}, \cdots, x_N | x_1, \cdots, x_r, x_s)$ and the

minimum energy configuration of all the cells that generates the erroneous output $x_s$ is $\{x_1^e, x_2^e, \cdots x_{r+1}^e, \cdots x_N^e\}$. This configuration corresponds to the most likely error state at the output $x_s$. Whenever we have $x_i^g \neq x_i^e$, the $i^{th}$ cell is considered sensitive to error at output $x_s$ (also termed as weak spots).

The above computational problem of maximization of a product of probability functions can be factored as product of the maximization over each probability functions, these maximizations can also be computed by local message passing [122]. The exact maximum likelihood inference scheme is based on local message passing on a tree structure, whose nodes are subsets (cliques) of random variables in the original DAG [138]. This tree of cliques is obtained from the initial DAG structure via a series of transformations that preserve the represented dependencies. The details of the inference scheme can be found in [137]. At this transformed point, we have a tree of cliques where each clique is a sub-set of random variables. Two adjacent cliques that share a few common variable play a key role in inference. The joint probability of all the variables can be proven to be the product of individual clique probabilities. Since the problem of maximization of a product of probability functions can be factored as product of the maximization over each probability functions, this maximization can also be computed by local message passing [138]. The overall message passing scheme involves the neighboring cliques using the maximum operator where the clique probabilities are updated till the marginal probability of the shared variables are the same.

This kind of maximum likelihood analysis can be conducted both at the layout and the circuit levels. Let us say that the circuit level macroblocks have $Y_1, \cdots, Y_r$ as inputs and $Y_{r+1}, \cdots, Y_M$ as internal circuit level lines (nodes). Let us say that the ground state macroblock cell polarizations are denoted by $\{y_1^g, y_2^g, \cdots y_{r+1}^g, \cdots y_M^g\}$. With respect to the the erroneous output $y_s$, let the minimum energy configuration is $\{y_1^e, y_2^e, \cdots y_{r+1}^e, \cdots y_M^e\}$.

As in the case of layout, whenever we have $y_j^g \neq y_j^e$, the $j$-th cell is considered sensitive to error at output $y_s$.

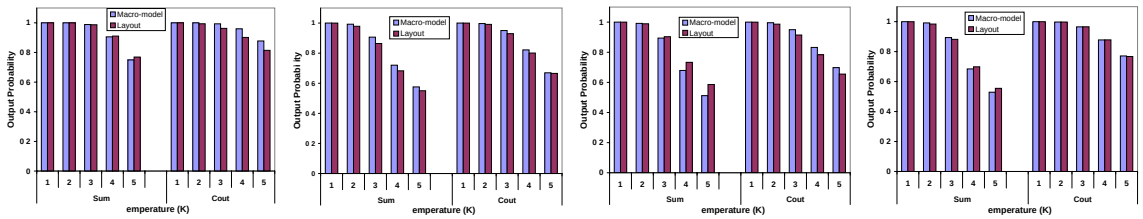
In the next section, we will presents results that show that the error modes of the circuit and layout levels match. That is, whenever $Y_j$ is sensitive to the first-excited error state for output $Y_s$, the corresponding layout level model, shows the set of $\{X_i\}$ that constituted the macroblock $Y_j$ is also sensitive . This is an extremely important finding that indicates that weak spot in the design can be identified at the circuit level itself without obtaining the cell layout. Also this is an important design metrics and can be used to vet one design over and above the thermal profile of the output polarization.

## 5.4 Results

We present results using the full adder design, which has been widely studied by others. We also use a multiplier design, which is a somewhat larger design. First, we will show that the ground state polarization probabilities of the output nodes as well as the intermediate nodes in the macromodel of the QCA logic circuit closely match with those obtained from a full layout level implementation [24] at various temperatures. Second, we demonstrate that both the ground and the next excited (error) state configuration of the macromodel exactly match the corresponding configurations of the detailed layout cells for two full adders designs. Third, we use the circuit level implementation to vet between alternate design choices. We show examples of this design space exploration process with the example of two adders.

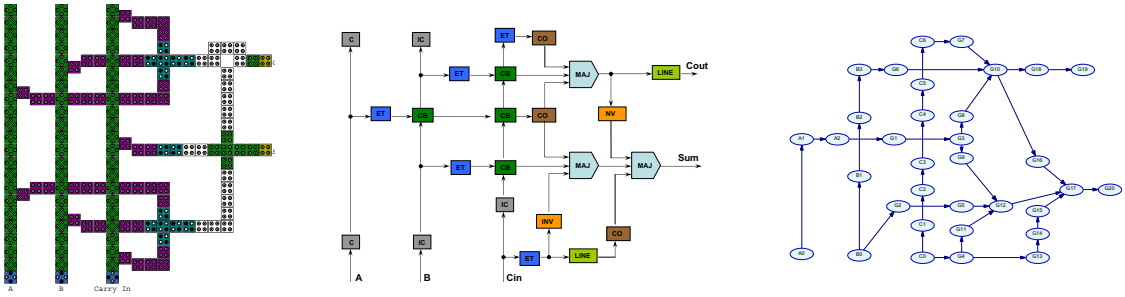
### 5.4.1 Polarization

Fig. 5.4. plots the polarization estimates at the layout and the circuit levels for various temperature, and for different inputs for Adder-1 architecture shown inFig. 5.3.a (layout



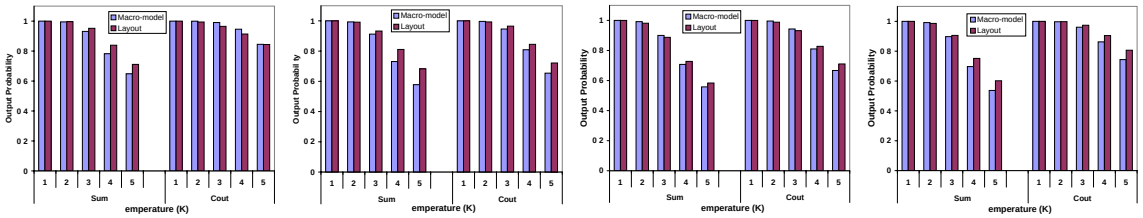

(a) (b) (c) (d)

Figure 5.4. Probability of correct output for sum and carry of Adder-1 based on the layout-level Bayesian net model and the circuit level macromodel, at different temperatures, for different inputs (a) (0,0,0) (b) (0,0,1) (c) (0,1,0) (d) (0,1,1).




(a) (b) (c)

Figure 5.5. A QCA Full Adder circuit (Adder-2) (a) QCA Fulladder cell layout (b) Macro-model representation (c) Macromodel Bayesian network. Note: Node elements are generic.




(a) (b) (c) (d)

Figure 5.6. Probability of correct output for sum and carry of Adder-2 based on the layout-level Bayesian net model and the circuit level macromodel, at different temperatures, for different inputs (a) (0,0,0) (b) (0,0,1) (c) (0,1,0) (d) (0,1,1).

level) and Fig. 5.3.c (circuit level). Fig. 5.5.(a) shows second adder architecture (Adder-2), consisting of three majority gates and two inverters [139]. Fig. 5.6. plots the polarization estimates at the layout and the circuit levels for various temperature, and for different inputs. We see that the difference in probability of correct output node between circuit and layout level model design is low for both the adders. We also see that in both layout and circuit level designs, the probability of the output node is dependent on the input vector set.

Similar trends is also seen for the 2x2 multiplier circuit shown in Fig. 5.7.(a). The multiplier circuit is somewhat larger than the full adder circuit and consists of two AND gates and two half adders. We made use of a half adder similar to Adder-2 full adder design, for the simple reason that it occupies less area. The polarization of the output nodes in the multiplier layout is almost similar to that obtained at the outputs of multiplier circuit designed using the macromodel blocks. In Fig. 5.9. and 5.10., we show the variation of output nodes C0,C1,C2 and C3 of the multiplier with respect to temperature for both layout and macromodel design.

### 5.4.2 Error Modes

We compute the near-ground state configurations that results in error in the output carry bit $C_{out}$ of the QCA full adders (Adder-1 and Adder-2) using both the layout and circuit level models. These are shown in Fig. 5.11. and 5.12. and Fig 5.13. and 5.14. We show four cases, for input vectors (0,0,0), (1,0,0), (0,1,0) and (1,1,1). The other four input vector sets will have similar results due to symmetry in design. We use red marker to point to the components that are weak (high error probabilities) in both the layout and circuit level. We can easily see that the nodes with high error probabilities in QCA layout are the ones that are clustered to form an erroneous node in the macromodel circuit design. In other words, if a node (a macromodel block) in macromodel circuit layout is highly error prone for a given input set, then some or all the QCA cells forming that macromodel block are highly

prone to error. This indicates that weak spot in the design can be identified early in the design process, at the circuit level itself.

### 5.4.3 Design Space Exploration

We show that even at the macromodel circuit level, we have the ability to explore the design space with respect to different criteria. In addition, to obvious criteria such as gate count, we can use polarization as a design metric. The probabilistic macromodel allows us very fast estimates of polarization that correlate very well with layout level estimates. As an example we use the two adders in Fig. 5.3.(a) and Fig. 5.5.(a). The two adders shown here have been designed using different macromodel blocks, occupying different design areas.

The outputs of Adder-1 circuit is given by

$$\begin{aligned} Sum &= A \cdot B \cdot C_{in} + \bar{A} \cdot \bar{B} \cdot C_{in} + \bar{A} \cdot B \cdot \bar{C_{in}} + A \cdot \bar{B} \cdot \bar{C_{in}} \\ &= m(m(\bar{A}, B, C_{in}), m(A, B, \bar{C_{in}}), m(A, \bar{B}, C_{in})) \\ C_{out} &= m(A, B, C_{in}) \end{aligned} \tag{5.10}$$

where $m(A, B, C_{in})$ is the majority gate containing A,B and $C_{in}$ as inputs. Similarly, for Adder-2 circuit the outputs are given by [139]

$$\begin{aligned} Sum &= m(\bar{C_{out}}, C_{in}, m(A, B, \bar{C_{in}})) \\ C_{out} &= m(A, B, C_{in}) \end{aligned} \tag{5.11}$$

We see that Adder-1 circuit uses five majority gates and three inverters for implementation while Adder-2 circuit uses three majority gates and two inverters. Hence the design circuit design of Adder-2 is certainly superior to Adder-1 in terms of area. However, as it can be seen from the thermal study, inverter has one of the worst polarization drop with respect to temperature and inverters in series path will reduce the overall polarization by a

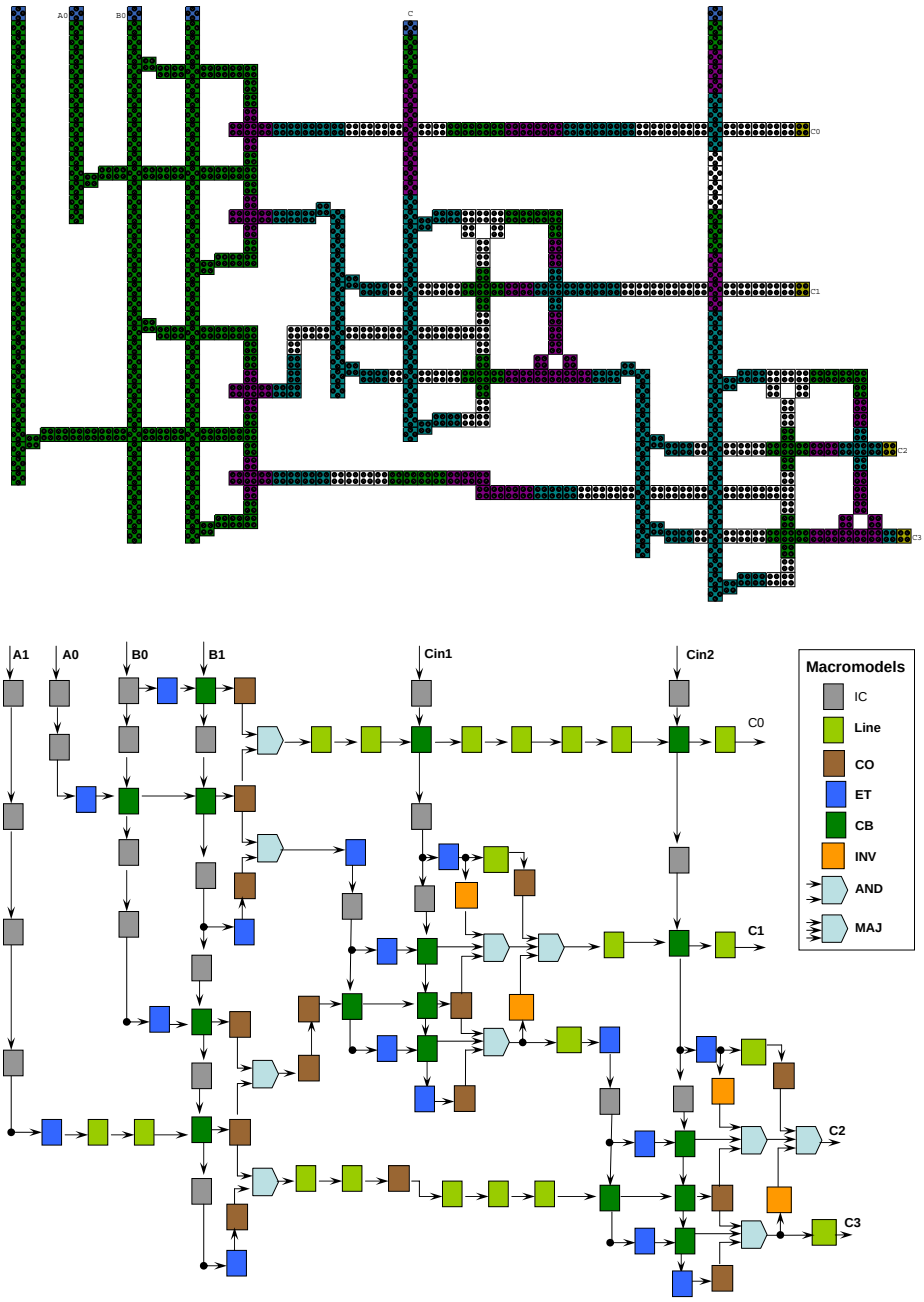



Figure 5.7. A QCA 2x2 Multiplier circuit(a) QCA multiplier cell layout (b) Macromodel representation

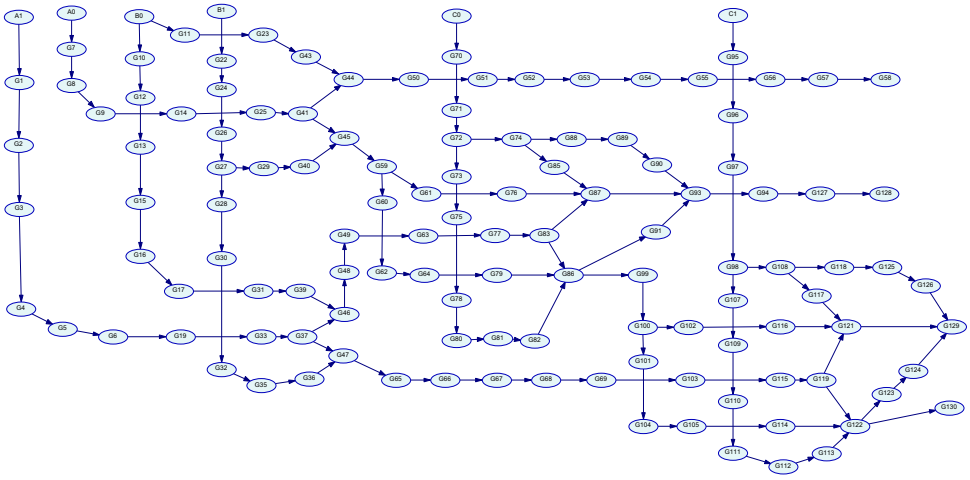


Figure 5.8. Macromodel Bayesian network of a QCA 2x2 Multiplier circuit. Note: Node elements are generic.

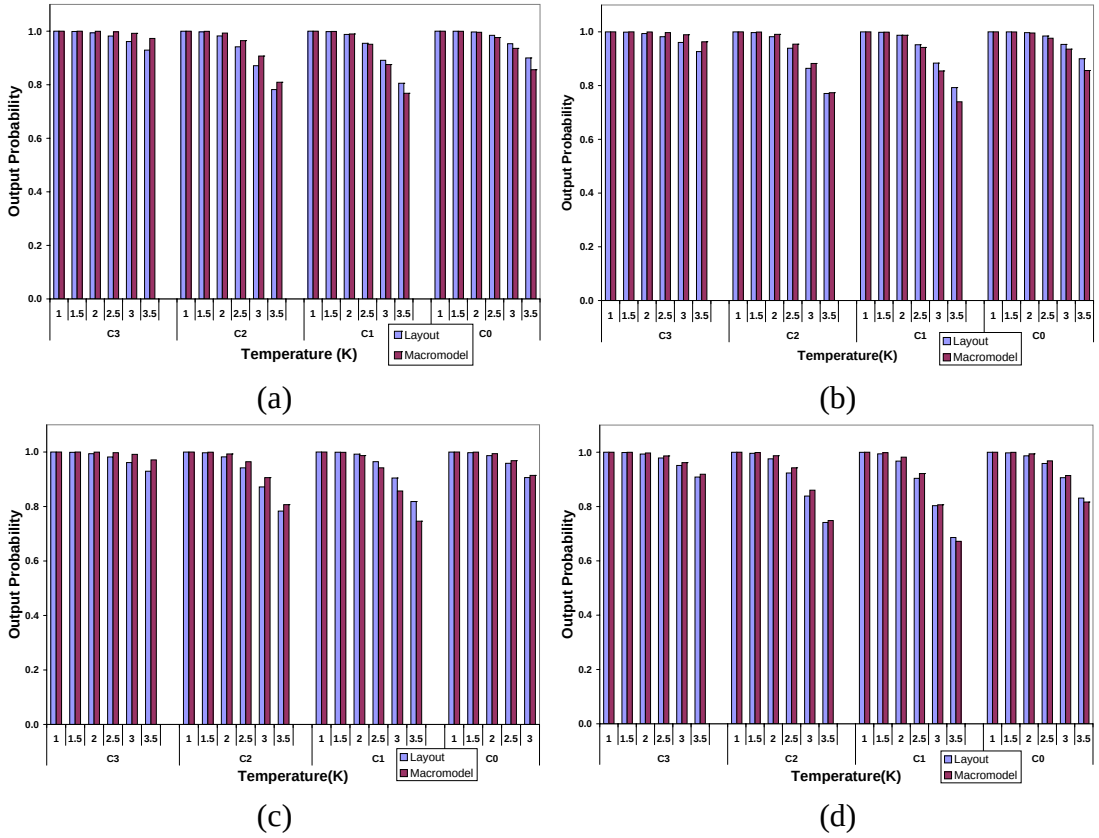



Figure 5.9. Probability of correct output at the four output nodes of 2x2 Multiplier circuit based on the layout-level Bayesian net model and the circuit level macromodel, at different temperatures, for different inputs (a) (0,0),(0,1) (b) (0,0),(1,1) (c) (0,1),(0,1) (d) (0,1),(1,1)

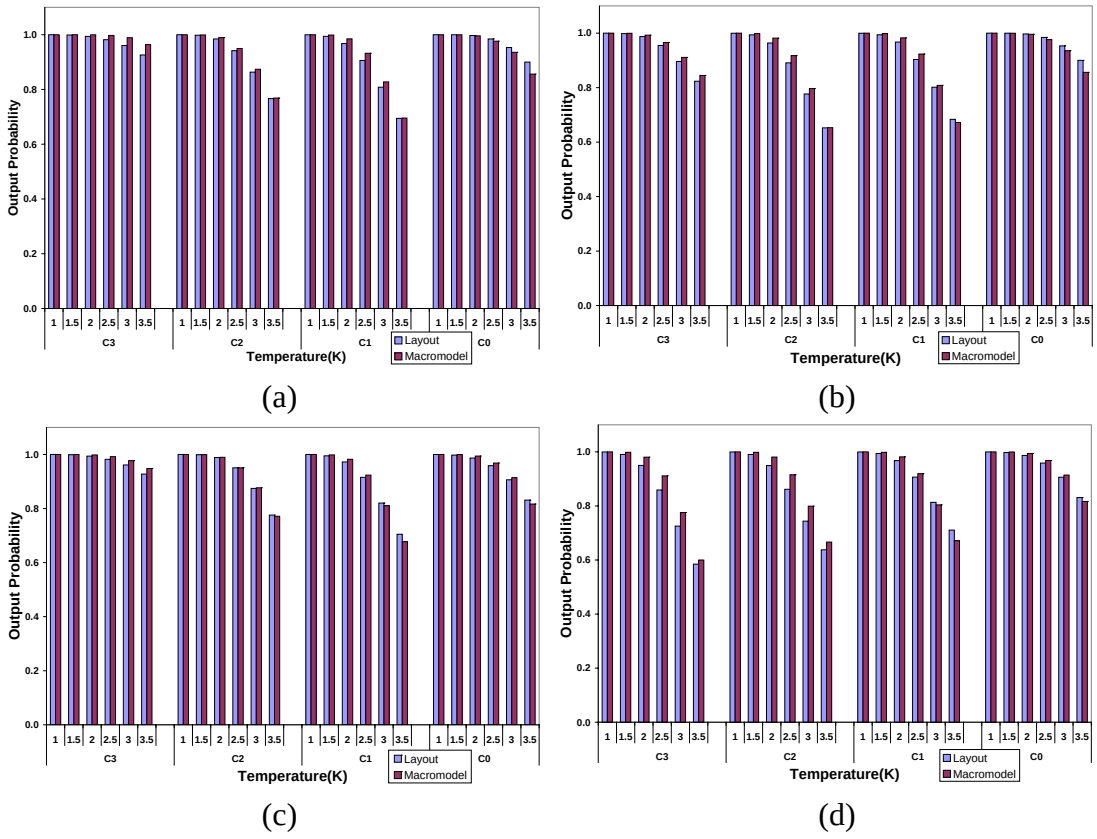



Figure 5.10. Probability of correct output at the four output nodes of 2x2 Multiplier circuit based on the layout-level Bayesian net model and the circuit level macromodel, at different temperatures, for different inputs (a)(1,0),(0,1) (b) (1,0),(1,1) (c) (1,1),(0,1) (d) (1,1),(1,1).

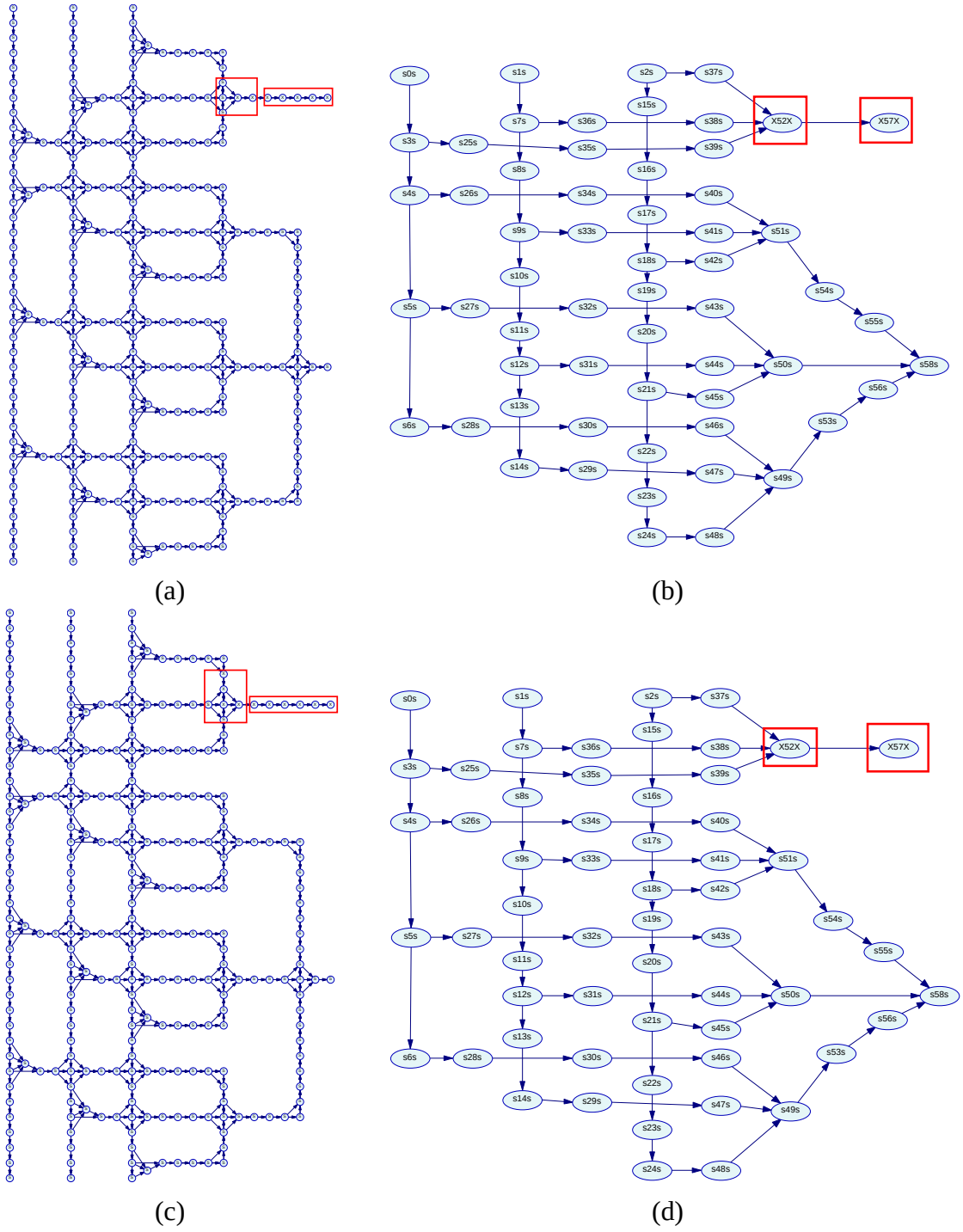



Figure 5.11. Error-prone nodes for first-excited state at carry output QCA Adder-1 Circuit and its Macromodel design. It can be seen that the erroneous nodes in the layout are effectively mapped in the macromodel design. Input vector set for (a) and (b) is (0,0,0) and that for (c) and (d) is (1,0,0). Note: Node elements are generic.

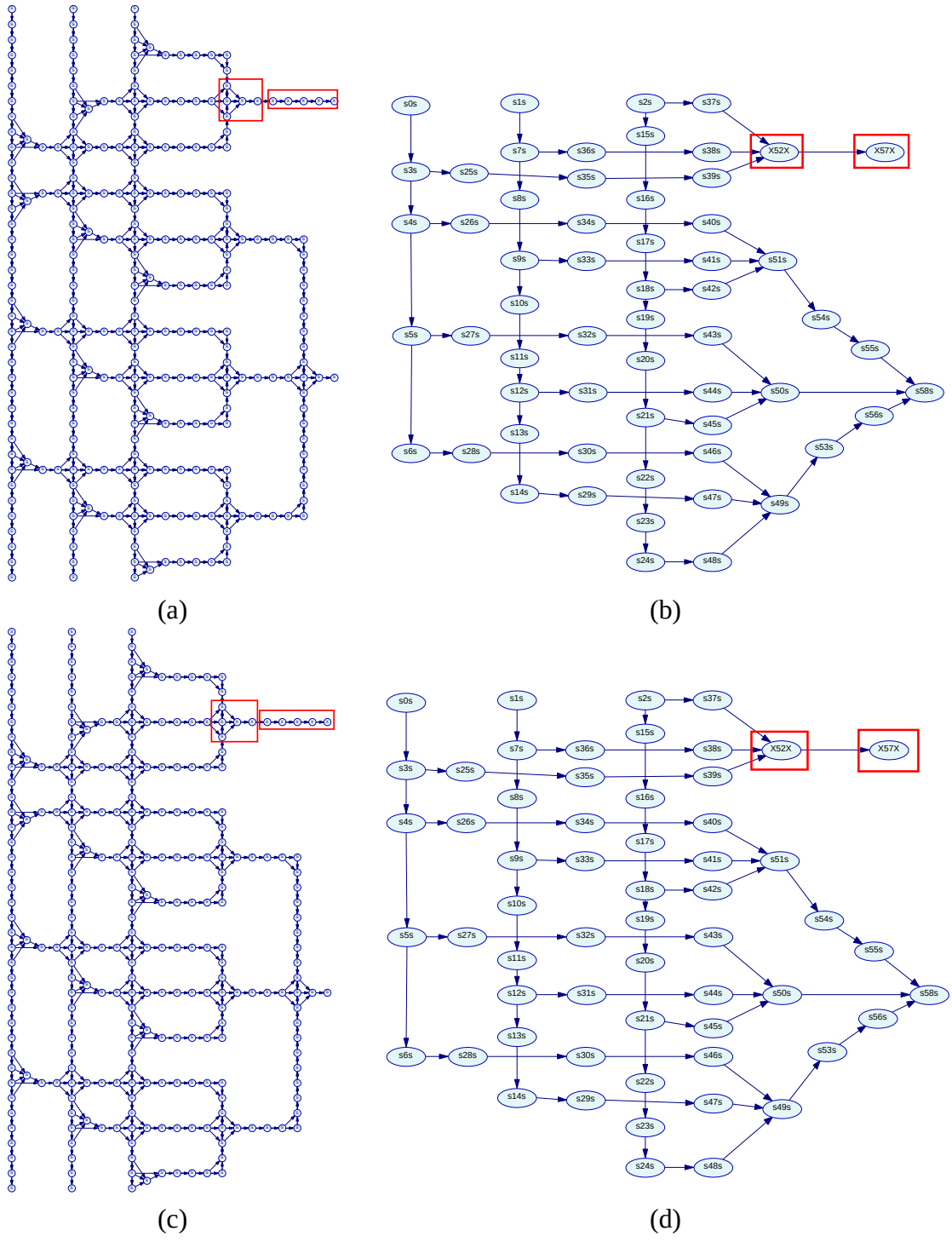



Figure 5.12. Error-prone nodes for first-excited state at carry output QCA Adder-1 Circuit and its Macromodel design. It can be seen that the erroneous nodes in the layout are effectively mapped in the macromodel design. Input vector set for (a) and (b) is (0,1,0) and that for (c) and (d) is (1,1,0). Note: Node elements are generic.

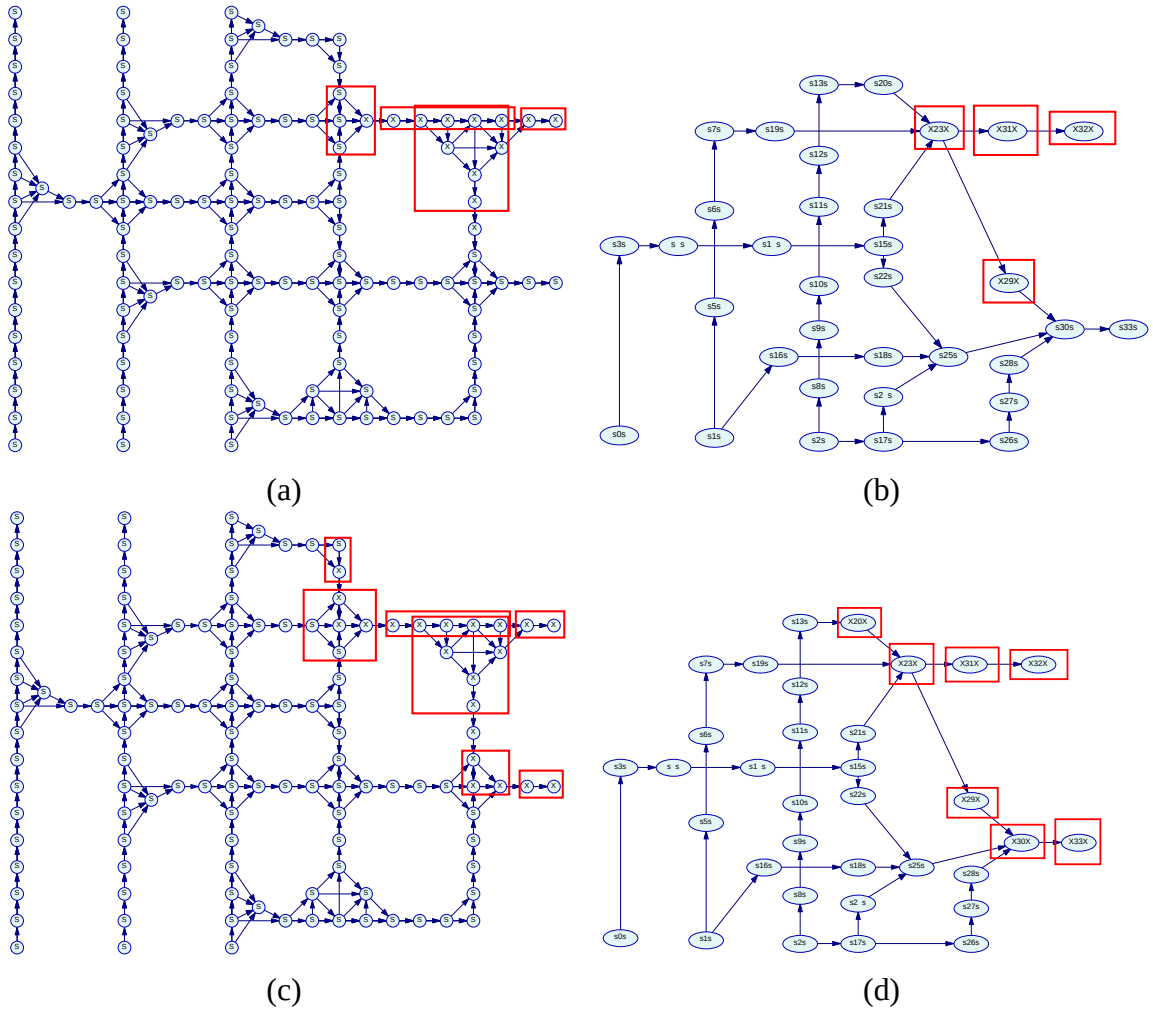



Figure 5.13. Error-prone nodes for first-excited state at carry output QCA Adder-2 Circuit and its Macromodel design. It can be seen that the erroneous nodes in the layout are effectively mapped in the macromodel design. Input vector set for (a) and (b) is (0,0,0) and that for (c) and (d) is (1,0,0). Note: Node elements are generic.

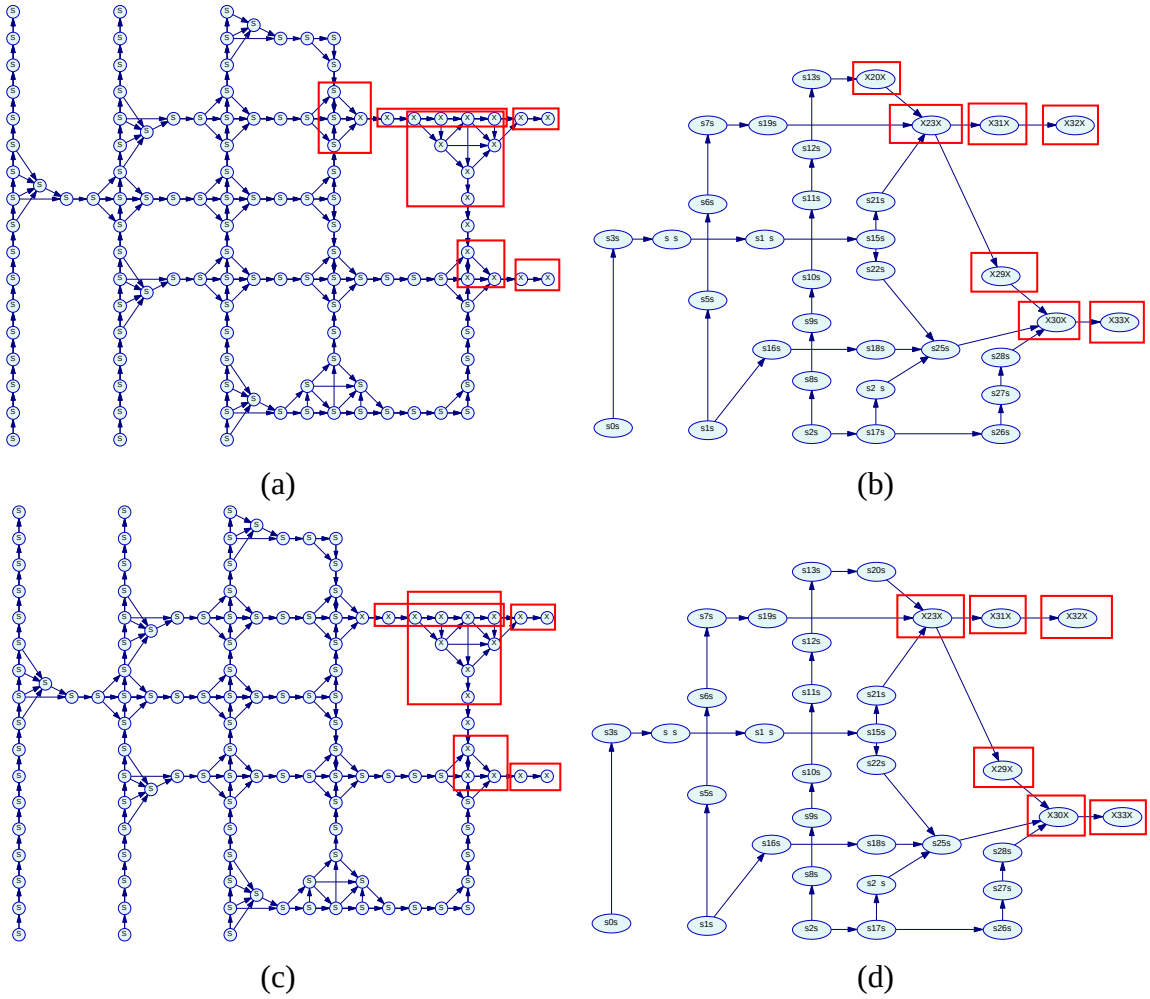



Figure 5.14. Error-prone nodes for first-excited state at carry output QCA Adder-2 Circuit and its Macromodel design. It can be seen that the erroneous nodes in the layout are effectively mapped in the macromodel design. Input vector set for (a) and (b) is (0,1,0) and that for (c) and (d) is (1,1,0). Note: Node elements are generic.

great extent. Hence for larger circuits, a design criteria might look at Adder-1 in a different light.

Note that in the context of error modes, presented earlier, we saw that Adder-1 again shows *less* number of error-prone nodes than Adder-2 (Fig. 5.11. shows error-prone nodes for first-excited state at carry output) for most likely errors in the outputs. Note that, ideally this conclusion requires the detailed layout, however, maximum-likelihood propagation of the circuit level Bayesian Network yields the same error modes as the detailed layout. This measure indicates that cost of addition error correction required for Adder-2 would be more than that of Adder-1.

Last but not the least, we observe that an odd tap shown in Section 5.2. is a good target for one inverter as the polarization loss is less than an inverter and an even tap works better than an even number of inverter chains. The multiplier design that we show, utilizes these facts to arrive at better design with respect to output polarization and this, in turn, improves the multiplier's thermal characteristics.

### 5.4.4 Computational Advantage

To quantify the computational advantage of a circuit level macromodel with a layout level model, we consider the complexity of the inference based on the Bayesian net models for each of them. As we mentioned earlier, in the cluster-based inference scheme, the Bayesian Network is converted into a junction tree of cliques and the probabilistic inference is performed on the junction tree by local computation between the neighboring cliques of the junction tree by local message passing [122, 24]. Space complexity of Bayesian inference is $O(n.2^{|C_{max}|})$ where $n$ is the number of variables, $|C_{max}|$ is the number of variables in the largest clique. Time complexity is $O(p.2^{|C_{max}|})$, where p is the number of cliques in the junction tree. We tabulate the complexity terms for the two adder designs in Table 5.4., along with the corresponding values for $n$, $p$ and $|C_{max}|$. We can see that macromodel is

Table 5.4. Layout and macromodel time ($T_c$) and space ($T_s$)complexities. Please see text for an explanation $C_{max}|$, $n$, and $p$.

| | Adder 1 | | Adder 2 | | Multiplier | |
|---|---|---|---|---|---|---|
| Parameters | Layout model | Macromodel | Layout model | Macromodel | Layout model | Macromodel |
| Cmax | 15 | 8 | 10 | 5 | 15 | 5 |
| p | 215 | 57 | 96 | 30 | 436 | 119 |
| n | 278 | 64 | 125 | 34 | 539 | 130 |
| $T_c = p.2^{\|C_{max}\|}$ | 7045120 | 14592 | 98304 | 960 | 14286848 | 3808 |
| $T_s = n.2^{\|C_{max}\|}$ | 9109504 | 16384 | 128000 | 1088 | 17661952 | 4160 |

order of magnitude faster especially due to the reduction in $|C_{max}|$ which would be important in synthesizing larger networks of QCA cells. Another observation is that Adder 2 is less expensive in terms of computation even though polarization drops are more due to the presence of inverters.

As we can see from the Table 5.5., the simulation time required to evaluate a circuit is orders of magnitude lower than that in QCADesigner tool. Moreover, we see that the simulation timing for bayesian macromodels of the adder circuit are much lower than bayesian full layout model. The graphs depicted in Fig. 5.4., Fig. 5.6., Fig. 5.9. and Fig. 5.10. present the crux of this work. The drooping characteristic of output node polarization with rise in temperature is a universally known fact. What we have shown in this work (as depicted in these graphs) is that the polarization of the output node in our macromodel design is showing the same drooping characteristics and is almost the same as that of the full layout. We can see that macromodel is order of magnitude faster specially due to the reduction in $|C_{max}|$ which would be important in synthesizing larger networks of QCA cells. Another observation is that Adder 2 is less expensive in terms of computation even though polarization drops are more due to the presence of inverters.

Table 5.5. Comparison between simulation timing (in seconds) of a Full Adder and Multiplier circuits in QCADesigner(QD) and Genie Bayesian Network(BN) Tool for Full Layout and Macromodel Layout

| Simulation Time | Adder-1 | Adder-2 | 2x2 Multiplier |
|---|---|---|---|
| | 278 cells | 125 cells | 539 cells |
| QD Coherence Vector | 566 | 253 | 966 |
| QD Bistable Approx. | 5 | 3 | 15 |
| QD Nonlinear Approx. | 3.5 | 2 | 8 |
| BN Full Layout model | 0.240 | 0.030 | 0.801 |
| BN Macromodel Layout | 0.010 | 0.000 | 0.08 |

# CHAPTER 6

# EFFECT OF KINK ENERGY IN QCA DESIGN

In chapter 3 we showed how to calculate the ground state polarization probabilities and build a graphical probabilistic model based on that. We used these graphical probabilistic models to detemine thermal error at the output at different temperatures. In [140], an efficient method, based on graphical probabilistic models was presented, to compute the N-lowest energy modes of a clocked QCA circuit. In QCA, an erroneous state may result due to the failure of the clocking scheme to switch portions of the circuit to its new ground state with change in input. This error state of a single cell in turn causes the error in the neighboring cells resulting in an erroneous output. Due to the quantum mechanical nature of operation of a QCA device, temperature plays an important role in determining the ground state polarization of each cell. Power dissipation in a QCA circuit primarily results due the the application of a non-adiabatic clocking scheme. We have also seen in chapter 4, how clock energy affects the overall power dissipation in a QCA circuit.

In this chapter we perform studies to determine the error and power tradeoff in a QCA circuit design by studying the effect of kink energy on the output error and power dissipation in a QCA circuit. We use three different sizes of QCA cells and grid spacing to study the polarization and power dissipation for basic QCA circuits using these cells.

We first simulate a number of basic QCA circuits such as majority gate and inverter to study the polarization error at the output for each input vector set. We also determine the power dissipation in these circuits for different kink energies. All other parameters such as temperature and clock energy are kept constant. We show how this study can be used

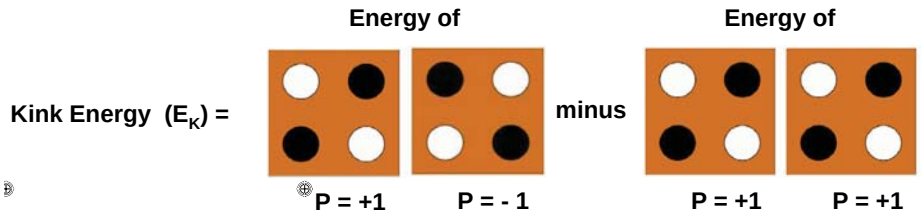



Figure 6.1. Kink energy between two neighboring QCA cells

by comparing two single bit adder designs. The study will be of great use to designers and fabrication scientists to choose the most optimum size and spacing of QCA cells to fabricate QCA logic designs.

## 6.1 Kink Energy

Two electrons in a a simple four dot QCA cell occupy diagonally opposite dots in the cell due to mutual repulsion of like charges. A QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. The two polarized states are represented as P = +1 and P = -1. Electrostatic interaction between charges in two QCA Cells is given as:

$$E^m = \frac{1}{4\pi\varepsilon_o\varepsilon_r}\sum_{i=1}^{4}\sum_{j=1}^{4}\frac{q_i{}^m q_j{}^k}{|r_i{}^m - r_j{}^k|} \tag{6.1}$$

This interaction is determines the kink energy between two cells.

$$E_{kink} = E_{opp.polarization} - E_{samepolarization} \tag{6.2}$$

Kink energy (Fig 6.1.) is the energy cost of two neighboring QCA cells having opposite polarization. Kink energy between two cells depends on the dimension of the QCA cell as well as the spacing between adjacent cells. It does not depend on the temperature.

Table 6.1. Different types of QCA cells and grid spacing used in this study

| QCA cell | Size | Grid Spacing | Associated Kink Energy |
|---|---|---|---|
| Cell-1 | 10nm | 5nm | $E_{k1} = 4E_k$ |
| Cell-2 | 20nm | 10nm | $E_{k2} = 2E_k$ |
| Cell-3 | 40nm | 20nm | $E_{k3} = E_k$ |

## 6.2 Results

In this section we present the results obtained from the study of variation of kink energy on error and power dissipated in the circuits. We obtained these results by simulating each of the circuits at a constant temperature of 2K. The three different types of cell sizes used in this study are elaborated in Table 6.1.

Here $E_{k1}$ is the maximum kink energy for the cell layout with smallest cell dimensions (and grid spacing). Similarly, $E_{k3}$ is the maximum kink energy for the QCA layout with largest cell dimensions (and grid spacing). As we can see from the table, $E_{k1} = 2E_{k2} = 4E_{k3}$.

### 6.2.1 Node Polarization Error

We quantify the error in a circuit as a measure of its output node polarization. In chapter 3, using temperature as a variable and keeping the kink energy constant we have shown how the output node polarization drops steadily with rise in temperature leading to more erroneous outputs. This effect becomes more and more significant with the increase in the number of cells in a design. Hence two different designs representing similar logic but having unequal number of cells will have different polarizations at the output nodes.

Similarly, in this study, by varying the kink energy of the circuit and keeping the temperature constant we see that the gain (drop) in output node polarization of a circuit is directly proportional to the increase (decrease) in maximum kink energy ($E_k$)of the circuit.

Table 6.2. Output node polarization of a simple majority gate for different Kink Energies

| | Maximum Kink Energy ($E_k$) | | |
|---|---|---|---|
| Input | $E_{k3}$ = 0.75 meV | $E_{k2}$ = 1.5 meV | $E_{k1}$ = 3.0 meV |
| 0 0 0 | 0.9278 | 0.9999 | 1.0000 |
| 0 0 1 | 0.9880 | 0.9999 | 1.0000 |
| 0 1 0 | 0.9880 | 0.9999 | 1.0000 |
| 0 1 1 | 0.9075 | 0.9999 | 1.0000 |
| 1 0 0 | 0.9075 | 0.9999 | 1.0000 |
| 1 0 1 | 0.9880 | 0.9999 | 1.0000 |
| 1 1 0 | 0.9880 | 0.9999 | 1.0000 |
| 1 1 1 | 0.9278 | 0.9999 | 1.0000 |

Table 6.3. Output node polarization of a QCA Inverter for different Kink Energies

| | Maximum Kink Energy ($E_k$) | | |
|---|---|---|---|
| Input | $E_{k3}$ = 0.75 meV | $E_{k2}$ = 1.5 meV | $E_{k1}$ = 3.0 meV |
| 0 | 0.9750 | 0.9998 | 1.0000 |
| 1 | 0.9843 | 0.9998 | 1.0000 |

Here increase in $E_k$ refers to decrease in QCA cell size and grid spacing. Similar effect was seen for different values of temperature.

As an example, refer to the output node polarization of a simple majority gate shown in Table 6.2. As we have shown earlier, we first form a Bayesian network of the QCA circuit and use a graphical simulator to obtain the polarization probability for each QCA cell (represented as a node) in the design. We can see that the polarization probability at the output of the Bayesian network rises with the increase in kink energy. Hence, we can infer that designs with lower value of maximum kink energy are more prone to error and this error is more significant when the number of cells in a design increase or the temperature is raised. Table 6.3. shows the output node polarization probability of a QCA inverter. We would liike to make a clarification on the term *error* used in this study. In chapter 5, we used the term *error* to signify the first excited state of a QCA cell. Here *error* refers to the drop in polarization probability at the output node of a QCA design.

Table 6.4. Power dissipation in QCA majority gate for different Kink Energies

| | Maximum Kink Energy ($E_k$) | | |
|---|---|---|---|
| | $E_{k3}$ = 3.0 meV | $E_{k2}$ = 1.5 meV | $E_{k1}$ = 0.75 meV |
| Max $E_{diss}$ (in meV) | 0.0294 | 0.0147 | 0.0051 |
| Avg $E_{diss}$ (in meV) | 0.0120 | 0.0060 | 0.0018 |
| Min $E_{diss}$ (in meV) | 0.0015 | 0.0008 | 0.0002 |
| Avg $E_{leak}$ (in meV) | 0.0018 | 0.0009 | 0.0003 |
| Avg $E_{sw}$ (in meV) | 0.0102 | 0.0051 | 0.0015 |

Table 6.5. Power dissipation in QCA Inverter for different Kink Energies

| | Maximum Kink Energy ($E_k$) | | |
|---|---|---|---|
| | $E_{k3}$ = 3.0 meV | $E_{k2}$ = 1.5 meV | $E_{k1}$ = 0.75 meV |
| Max $E_{diss}$ (in meV) | 0.0785 | 0.0392 | 0.0196 |
| Avg $E_{diss}$ (in meV) | 0.0425 | 0.0213 | 0.0106 |
| Min $E_{diss}$ (in meV) | 0.0066 | 0.0033 | 0.0016 |
| Avg $E_{leak}$ (in meV) | 0.0066 | 0.0033 | 0.0016 |
| Avg $E_{sw}$ (in meV) | 0.0359 | 0.0180 | 0.0090 |

### 6.2.2 Switching Power

We performed an exhaustive study on the effect of varying kink energy on the power dissipated during a switching event in a QCA circuit. While we have presented the result of power dissipated in a QCA circuit with varying clock energy in chapter 4, in this chapter we intend to analyze the effect of the size of a QCA cell and the kink energy associated with it on the power dissipated in the circuit. As can be seen from in Table 6.4., increasing the value of kink energy in a circuit leads to an increase in the overall average power dissipated in the circuit. Table 6.5. shows the energy dissipation in a QCA inverter for different values of kink energy.

Some very interesting observations were obtained from this study of effect of kink energy on the overall power dissipation and probability of error in QCA circuit design. We have seen that while it is desirable to design circuits with lower error probabilities (by increasing the kink energy between cells), it inadvertently increases the power dissipated in the circuit. This effect is more pronounced in larger circuits such as single bit adders.

Table 6.6. Output node polarization at SUM output node of Adder-1 and Adder-2 QCA designs

| | $E_{k3}$ = 1.09meV | | $E_{k2}$ = 2.18meV | | $E_{k1}$ = 4.36meV | |
|---|---|---|---|---|---|---|
| Input | Adder-1 | Adder-2 | Adder-1 | Adder-2 | Adder-1 | Adder-2 |
| 0 0 0 | 0.9110 | 0.8095 | 0.9998 | 0.9964 | 1.0000 | 1.0000 |
| 0 0 1 | 0.7311 | 0.8058 | 0.9935 | 0.9965 | 1.0000 | 1.0000 |
| 0 1 0 | 0.7440 | 0.6833 | 0.9944 | 0.9667 | 1.0000 | 0.9991 |
| 0 1 1 | 0.7090 | 0.6312 | 0.9931 | 0.9569 | 1.0000 | 0.9989 |
| 1 0 0 | 0.7090 | 0.6312 | 0.9931 | 0.9569 | 1.0000 | 0.9989 |
| 1 0 1 | 0.7440 | 0.6833 | 0.9944 | 0.9667 | 1.0000 | 0.9991 |
| 1 1 0 | 0.7311 | 0.8058 | 0.9935 | 0.9965 | 1.0000 | 1.0000 |
| 1 1 1 | 0.9110 | 0.8095 | 0.9998 | 0.9964 | 1.0000 | 1.0000 |

Table 6.7. Non-Adiabatic Energy dissipation in Adder-1 and Adder-2 QCA designs

| | $E_{k1}$ = 4.36meV | | $E_{k2}$ = 2.18meV | | $E_{k3}$ = 1.09meV | |
|---|---|---|---|---|---|---|
| | Adder-1 | Adder-2 | Adder-1 | Adder-2 | Adder-1 | Adder-2 |
| Max $E_{diss}$ (in meV) | 3.0939 | 1.3556 | 1.5404 | 0.6778 | 0.8127 | 0.3389 |
| Avg $E_{diss}$ (in meV) | 1.7398 | 0.7650 | 0.8665 | 0.3825 | 0.4556 | 0.1912 |
| Min $E_{diss}$ (in meV) | 0.4083 | 0.1949 | 0.2038 | 0.0974 | 0.1041 | 0.0487 |
| Avg $E_{leak}$ (in meV) | 0.4089 | 0.1956 | 0.2041 | 0.0978 | 0.1043 | 0.0489 |
| Avg $E_{sw}$ (in meV) | 1.3309 | 0.5693 | 0.6624 | 0.2847 | 0.3513 | 0.1423 |

Table 6.6. compares the results of output polarization at SUM node of two adders for different kink energies. As we can see that even though Adder-2 has a more efficient design and uses less number of cells, the polarization at its output is worse than that of Adder-1 for different input vector sets. Similarly, Table 6.7. compares the energy dissipation in the two adder designs. Power dissipation in Adder-2 is greater than that of Adder-1 since it has significantly more number of cells. However, we do see that the energy dissipation in a QCA circuit is almost linearly proportational to the maximum kink energy of the circuit.

As we can see from the results the output node polarization error *improves* while power dissipation *deteriorates* when the kink energy is increased. Hence designers need to choose the size of QCA cells based on circuit requirements to optimize power and error. This is different from thermal studies performed on QCA circuits which resulted in increase in output error and power dissipation at higher temperatures. From the results obtained for

polarization and power dissipation in small and big QCA circuits, we have clearly seen that kink energy is an important factor to design most optimum circuits at a given temperature and clock energy. Hence designers need to make careful use of kink energy as parameter for designing QCA circuits to optimize error and power.

# CHAPTER 7

# CONCLUSION AND FUTURE WORKS

In this dissertation, we proposed an efficient Bayesian Network based probabilistic scheme for QCA circuit design that can estimate cell polarizations, ground state probability, and lowest-energy error state probability, without the need for computationally expensive quantum-mechanical computations. Bayesian modeling captures the inherent causal nature of QCA devices and offers a fast approximation based method to estimate error, power and reliability in QCA design.

Some of the limitations and scope of this work are listed below:

- In hierarchical macromodeling it is assumed that the designer has some idea the layout level design of the same circuit
- In the power model we ave not taken into account the power dissipation in the clock circuit itself.
- In error-power tradeoff study by variation of maximum kink energy we have assumed that this model will accurately capture all the effects even at a smaller scale.
- Finally, the scope of this work is limited to a 4-dot electronic QCA implementation. The model will be different for other types of implementations such as molecular and magnetic QCAs.

For the purpose of this work we verified the ground truth using the coherence vector based method in QCADesigner simulator. A summary of important contributions of this dissertation is summarized below

- To the best of our knowledge, our non-adiabatic power dissipation modeling scheme is the first work in a QCA design which provides a realistic estimate of worst case power dissipated during a switching event. This model can be used to quickly compute the worst case power dissipated at each individual cell in a QCA layout for any input vector transition. This enables us to locate cells in a layout, early on in the design process, that are critical in terms of power dissipation and also identify the input vector transitions that result in large power dissipations. We have also demonstrated the effect of clock energy on overall power dissipated in a QCA design.

- To the best of our knowledge, the macromodel design scheme is the first work to model QCA designs at a hierarchical circuit level. Our results demonstrated that both the polarization and the error mode estimates at the circuit level match those at the layout level. The developed models in this work can be used to selectively identify weak components in a design early in the design process. It would then be possible to reinforce those weak spots in the design using reliability enhancing strategies.

- Study the effect of Kink energy on circuit design. We performed error-power tradeoff studies to by varying the kink energy of a QCA circuit. We found that the output node polarization error as well as the power dissipation decrease when the kink energy is increased. This is different from thermal studies which resulted in increase in output error and power dissipation at higher temperatures.

One interesting future study using this model could be to see the effect of highly error-prone cells on the thermal hotspots in a QCA design. That is to see if the highly error-prone cells are the same cells that cause the maximum energy dissipation.

Another possible future direction of this work involves the extension of the BN model to handle sequential logic. This is possible using an extension called the dynamic Bayesian networks, which have been used to model switching in CMOS sequential logic [141].

There is also a vast scope to conduct probabilistic modeling to estimate error, power and other design related issues on other emerging nanotech devices such as magnetic and molecular QCA, spintronics, nano-CMOS and photonic devices.

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