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Improved techniques for nonlinear electrothermal FET modeling and measurement validation

Charles Passant Baylis
University of South Florida

Improved Techniques for Nonlinear Electrothermal FET Modeling and Measurement Validation

by

Charles Passant Baylis II

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of the requirements for the degree of
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Department of Electrical Engineering
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Co-Major Professor: Lawrence P. Dunleavy, Ph.D.
Co-Major Professor: Arthur David Snider, Ph.D.
Thomas M. Weller, Ph.D.
Frank Pyrtle, III, Ph.D.
Dennis K. Killinger, Ph.D.

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DEDICATION

To my Lord and Savior Jesus Christ, with love and gratitude.

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IMPROVED TECHNIQUES FOR NONLINEAR ELECTROTHERMAL FET MODELING AND MEASUREMENT VALIDATION

Charles Passant Baylis II

ABSTRACT

Accurate transistor models are important in wireless and microwave circuit design. Large-signal field-effect transistor (FET) models are generally extracted from current-voltage (IV) characteristics, small-signal S-parameters, and large-signal measurements. This dissertation describes improved characterization and measurement validation techniques for FET models that correctly account for thermal and trapping effects.

Demonstration of a customized pulsed-bias, pulsed-RF S-parameter system constructed by the author using a traditional vector network analyzer is presented, along with the design of special bias tees to allow pulsing of the bias voltages. Pulsed IV and pulsed-bias S-parameter measurements can provide results that are electrodynamically accurate; that is, thermal and trapping effects in the measurements are similar to those of radio-frequency or microwave operation at a desired quiescent bias point. The custom pulsed S-parameter system is benchmarked using passive devices and advantages and tradeoffs of pulsed S-parameter measurements are explored. Pulsed- and continuous-bias measurement results for a high-power transistor are used to validate thermal S-parameter correction procedures.

A new implementation of the steepest-ascent search algorithm for load-pull is presented. This algorithm provides for high-resolution determination of the maximum power and associated load impedance using a small number of measured or simulated reflection-coefficient states. To perform a more thorough nonlinear model validation, it is often desired to find the impedance providing maximum output power or efficiency over variations of a parameter such as drain voltage, input power, or process variation. The new algorithm enables this type of validation that is otherwise extremely tedious or impractical with traditional load-pull.

A modified nonlinear FET model is presented in this work that allows characterization of both thermal and trapping effects. New parameters and equation terms providing a trapping-related quiescent-bias dependence have been added to a popular nonlinear ("Angelov") model. A

systematic method for fitting the quiescent-dependence parameters, temperature coefficients, and thermal resistance is presented, using a GaN high electron-mobility transistor as an example. The thermal resistance providing a good fit in the modeling procedure is shown to correspond well with infrared measurement results.

CHAPTER 1: INTRODUCTION

In modern wireless and microwave circuit design, increased demands are being placed on computer-aided design (CAD) simulation models. For circuit design success, emphasis must be placed on extracting models that accurately predict the behavior of a device, including effects resulting from self-heating and trapping. This chapter overviews motivation for improved extraction procedures and efficient validation methods for field-effect transistor (FET) transistor models, contributions made by this work to the modeling process, and the research methods used to accomplish these contributions.

1.1. Motivation

Accurate nonlinear models for transistors can assist in obtaining first-pass design success. If the design is not optimized correctly in the simulation stage, the resultant costs associated with repeating the design and fabrication processes can be significant, in addition to time expenditure. Accurate transistor models are needed for the design of power amplifiers, oscillators, mixers, and other nonlinear components that comprise modern communication systems. Because these components are used for both military and commercial purposes, accurate transistor model extraction and validation methods have a significantly broad positive impact.

Modern modulation techniques emphasize the necessity for time-domain, as well as frequency-domain, prediction. Common examples include ultra-wideband (UWB) [1], which is a time-domain modulation, waveform engineering, and Class E amplifier design [2]. In addition to accurate time-domain prediction, many circuits must be able to perform in a broad variety of environments. Furthermore, reconfigurable circuits that can work under different bias and frequency conditions are commonly designed for both military and commercial applications. These demands create several topics that transistor modeling research must address to improve the state-of-the-art.

Successfully separating thermal and trapping effects in modeling should give the model the capability to predict behavior over a wider range of bias conditions. Pulsed current-voltage (IV) and S-parameter measurements play an important role in the diagnosis of thermal and trap

effects and their accurate characterization [3]. In addition, discovering how to accurately account for these effects in the time domain would provide needed capabilities in the model to handle many of the complex modulation schemes mentioned.

More efficient large-signal validation methods are needed for models. Conventional load-pull measurements are extremely time-consuming. This prevents the efficient validation of models over a range of conditions. This will be necessary in the design of models to operate under different frequency conditions, bias voltages, and radio-frequency (RF) power levels.

Many of the transistors used in modern communication systems are designed for large output power and low heating. Accurate models are needed that take into account the thermal and trapping effects of the device, primarily for two reasons. First, the choice of an operating point to provide desired output power and efficiency is dependent upon the device IV characteristics [2], which are heavily dependent on channel temperature and trapping effects [3]. Second, the heating of a device under certain operating conditions and applied signals is important in the physical design of a circuit for heat-transfer purposes.

The present state-of-the-art in transistor modeling contains many measurement methods to extract models that are more accurate with respect to characterizing thermal and trapping effects; that is, more "electrodynamically" accurate models. Pulsed IV measurements have been used to measure the current during brief excursions in voltage from a quiescent bias point. The swiftness of the excursion allows the characteristics to be measured such that the thermal and trapping effects depend on the quiescent bias point. The benefits of pulsed IV measurements are heavily discussed in the literature [3], [4], as well as in the Master's thesis of the author [5]. Thermal resistance measurement methods using pulsed IV for devices with minimal trapping effects have also been developed by the author and others [6], [7].

Pulsed S-parameter measurements have been used to allow the self-heating and trapping effects to be those of a design quiescent bias point during multiple-bias small-signal S-parameter measurements. Such measurements, and the improved results from these effects, are discussed in the literature [8], [9], [10]. Construction of such a system requires many considerations, however. For example, bias tees must be designed that allow pulsing through their "DC" paths. In addition, the practicalities of performing the pulsed measurement result in a loss of dynamic range and precision. This work provides a method of benchmarking the dynamic range and precision to allow a satisfactory pulse length and duty cycle to be chosen.

Models typically contain a single parallel resistor and capacitor to model the time-dependent heating; however, it is suggested in the literature that multiple thermal time constants

may exist in a device. For example, the device itself would possess a short time constant, with the heat sink possessing a larger time constant [11]. This work compares the approaches of single and double time-constant modeling.

1.2. Contributions of this Work

Each of the contributions in this dissertation is aimed at improving the electrothermal modeling and model verification process. There are three major contributions of this work. First, modification of the popular Angelov model [12] has been performed that allows calculation of the quiescent-bias dependence of the drain current due to trapping effects and also simultaneously provides for accurate prediction of self-heating effects. While the model proposed in this work is a first approximation at a separation of trapping and thermal effects that may be later improved, the ability to obtain quiescent-dependent IV curves with reasonable accuracy based on thermal and trapping conditions provides a significant improvement to IV prediction capabilities over a pulsed IV measurement taken at a single quiescent bias point.

Second, a novel load-pull algorithm to efficiently validate model performance and characterize devices under swept conditions with a reasonably small number of reflection-coefficient states has been designed and tested. The results obtained indicate that a high level of precision has been achieved in the measurements and the method is shown to be robust over a range of search starting points.

Third, investigations on techniques for constructing and benchmarking a pulsed-bias, pulsed-RF S-parameter system using a conventional vector network analyzer (VNA) are presented. The design of bias tees, the use of an RF switch, and obtaining measures of the system precision and dynamic range degradation through measuring passive devices, topics heretofore not well explained in the literature, are presented herein.

1.3. Research Methods

To accomplish the development of a bias-dependent model that accounts for thermal and trapping effects, a research process was followed. The first step was the study of thermal effects through pulsed IV measurement on silicon devices, which are not expected to possess significant amounts of trapping [4], [5]. Previous methods of self-heating and trapping characterization were studied and attempts were made to employ these on GaN high electron-mobility transistors (HEMTs). This work presents the results from thermal and trap characterization as given in the literature. After examining the effect of drain and gate quiescent bias point on the device IV

characteristics and study of the physics of these effects, modifications were made to the Angelov model to account for the quiescent-bias dependence.

To develop the presented peak-search algorithm, the literature was reviewed in two areas: developments in efficient load-pull measurements and search algorithm theory. After this review, the steepest-ascent algorithm, which can be used for a variety of search types, was applied to develop a maximum-power load-pull search. The algorithm was tested for both measurement and simulation. The results appear to allow high-resolution determination of the maximum power and its associated reflection coefficient and also to facilitate measured-versus-simulated comparisons where multiple load-pull measurements are necessary.

Finally, the construction of the pulsed S-parameter system was performed incrementally, by reviewing available literature results studying the mechanics of pulsed RF measurements [13] and by carefully characterizing and benchmarking components within the system as the system was constructed. The bias tees were thoroughly tested for both RF and pulsed-bias performance, as shown in Chapter 5, before being used in the pulsed S-parameter system. The entire system was then carefully benchmarked using passive devices, as shown in Chapter 6. To construct the transient setup, similar analysis and measurements were studied in the literature [14], and the system constructed for this work is very similar. Analysis was performed on the transients using software, and an exponential equation was fit to the transient drain voltage data.

1.4. Organization

Because this dissertation focuses on improving nonlinear model extraction and validation, a typical extraction procedure is demonstrated on a GaAs pseudomorphic high electron-mobility transistor (PHEMT) in Chapter 2. The standard procedure shown includes comparison with current-voltage (IV) curves, multiple-bias small-signal S-parameters, power sweep, and load-pull data.

The remainder of the work focuses on improving these methods. To understand how a nonlinear model can be improved to better predict thermal and trapping effects, it is helpful to begin with a review of these effects. Thermal effects are discussed in Chapter 3. Thermal resistance extraction techniques and transient measurements are described for silicon devices. Chapter 4 discusses trapping effects, presenting physical results obtained from the literature and consolidating them into a strategy for diagnosing the types of traps present in a device.

Chapters 5 and 6 present the development of a custom pulsed S-parameter test system to allow isodynamic measurement of S-parameters. Chapter 5 presents the design and test

procedure of the pulsed-bias tee, while Chapter 6 presents the development and benchmarking of the pulsed-bias, pulsed-RF S-parameter system. It concludes by presenting a method for S-parameter thermal correction that is consistent with results presented in the literature [9].

Chapter 7 addresses the development of an innovative load-pull algorithm, presenting the search process and demonstrating it with both simulation and measurement results. An example of power-swept load-pull is given to illustrate types of measured-versus-simulated comparisons facilitated by this algorithm.

Chapter 8 discusses issues related to thermal resistance measurement with pulsed IV in the presence of traps. Thermal resistance measurement attempts with a pulsed IV method are presented along with independent infrared measurements. Chapter 9 presents the new proposed Quiescent-Bias Dependent Angelov model and shows that the value of thermal resistance measured in infrared measurement, along with the quiescent-bias dependence, seems to provide reasonable prediction of the pulsed IV results and concludes that the thermal resistance can be accurately extracted by using the quiescent-bias dependent model.

Chapter 10 provides conclusions and recommendations for future work in the area of electrodynamic model extraction techniques.

1.5. Chapter Summary

The motivation for improving large-signal FET model extraction techniques has been outlined. This work makes three main contributions: the development of a quiescent-bias dependent Angelov model to characterize thermal and trapping effects in devices, the design and implementation of a steepest-ascent load-pull algorithm, and the development of a design, benchmarking, and testing process for a custom pulsed S-parameter system.

CHAPTER 2: NONLINEAR MODELING PROCEDURES

In this chapter, general strategies for nonlinear transistor model extraction and verification are outlined. Knowledge of the procedural basics of model extraction is helpful in understanding the challenges of modeling and how they can be addressed. A large-signal model is often extracted from a large body of data, including IV, S-parameter, and large-signal measurements.

2.1. Large-Signal Transistor Modeling

Transistor modeling can be defined as extracting parameters for a set of equations to define the equivalent circuit parameters of the transistor. Different nonlinear models use different equations to define the different parameters; however, nonlinear models usually have similar equivalent-circuit topologies. Examples of nonlinear transistor models include the Angelov [12], EEHEMT [15], and Curtice [16] models.

What is the difference between a small-signal model and a large-signal model? A FET small-signal model defines behavior at a given quiescent (V_{GS}, V_{DS}) point for signal levels at which the behavior can be considered to be linear. In a small-signal model, the equivalent circuit parameters are constant values. In a large-signal model, behavior is defined for both linear (small-signal) and nonlinear (large-signal) operation. As the level of a signal increases, both the current and charge characteristics generally change. As a result, it is necessary to define many of the equivalent circuit parameters using voltage-dependent equations in nonlinear models.

The extraction of parameters in a small-signal model can be performed based on a set of S-parameter data taken at the desired (V_{GS}, V_{DS}) bias point. At a given bias point, software can be used to optimize or tune the equivalent circuit parameter values to match S_{11}, S_{12}, S_{21}, and S_{22}. The small-signal model requires only one set of data for an extraction and may be sufficient for small-signal applications, such as some low-noise amplifier designs.

In many cases, the FET will be operating in large-signal conditions. Examples of designs where this is the case are power amplifiers, mixers, and oscillators. It is necessary for these designs to predict behavior over a large operating range. For this purpose, a large-signal

(nonlinear) model is required. While, for a small-signal model, the parameters are constant values, many of the parameters in large-signal models are described by equations rather than fixed values and are functions of the instantaneous gate and drain voltages. The large-signal model also requires a larger body of data for accurate extraction. Large-signal models are typically extracted from current-voltage (IV) curves, S-parameters at multiple (V_{GS}, V_{DS}) bias conditions (perhaps up to 30 or more), and large-signal measurements, such as power sweep and load pull [17].

The Angelov model [12], a typical large-signal model, is shown in Figure 2.1, as taken from [18]. Some of the more critical components of this model are the current equation for Ids, the capacitor equations for Cgs and Cgd, and the constant value for Cds. Many of the other networks have been added to allow low-frequency effects and parasitic extrinsic effects to be taken into account. The equations for the Angelov model are given in the literature [12]. Figure 2.2 shows the EEHEMT large-signal FET model [15] as shown in [18]. While the equations are different, the circuit topology of this model is similar. The model contains a drain current source Ids and contains charge sources Qgy (which yields the gate-drain capacitance) and Qgc (which yields the gate-source capacitance), as well as drain-source capacitance Cdso. Most of the nonlinear FET models have similar topologies; many of the differences between models are in the equations used to define the currents and capacitances.

The following sections briefly describe modeling techniques using an example of an EEHEMT model extraction for a GaAs pseudomorphic high electron mobility transistor (PHEMT). This model was extracted as part of a modeling project by Modelithics, Inc., through the collaborative work of Modelithics engineers and the author. In this extraction, modeling software tools included Agilent Technologies ICCAP and Advanced Design System (ADS) [15]. ICCAP is a program that is designed specifically to take measurements required for model extraction and to extract model parameters using automatic optimization or manual tuning. An example template for ICCAP measurement used in this project is shown in Figure 2.3.

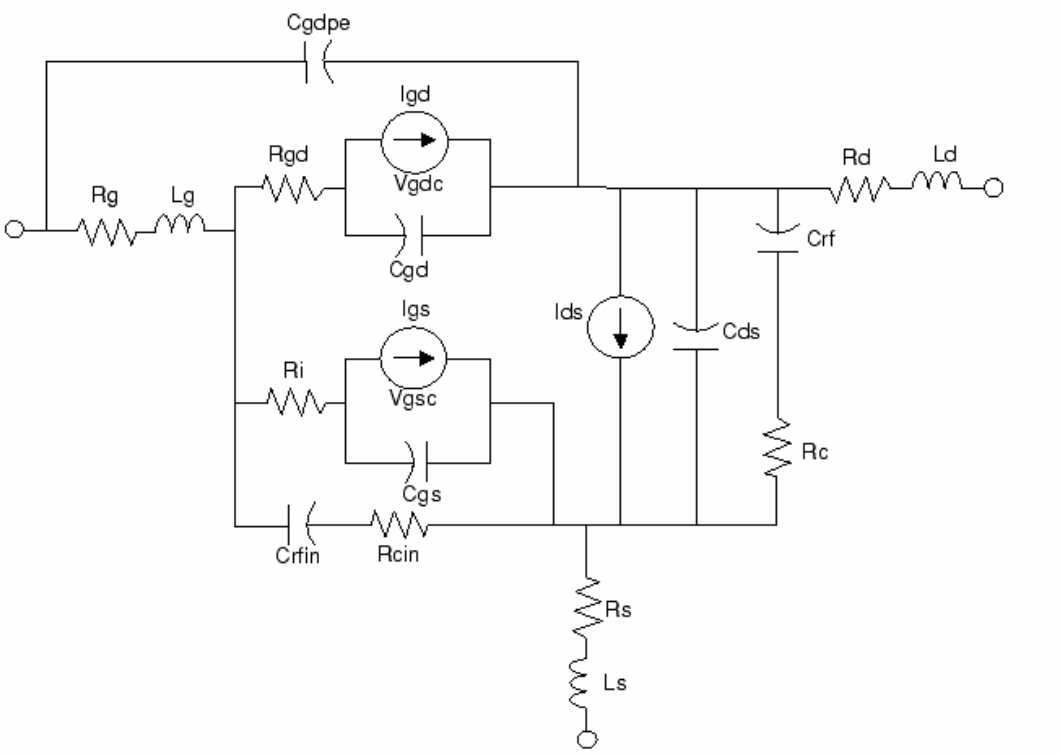


Figure 2.1. Angelov Large-Signal FET Model [12], Reprinted from [18]

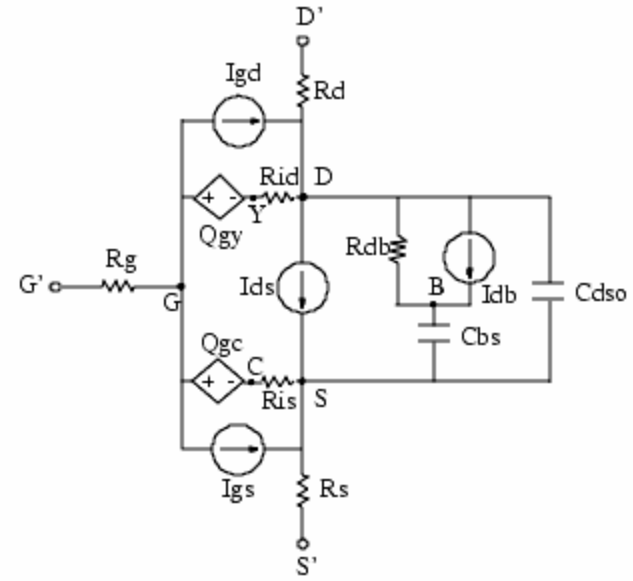


Figure 2.2. EEHEMT Large-Signal FET Model [15], Reprinted from [18]

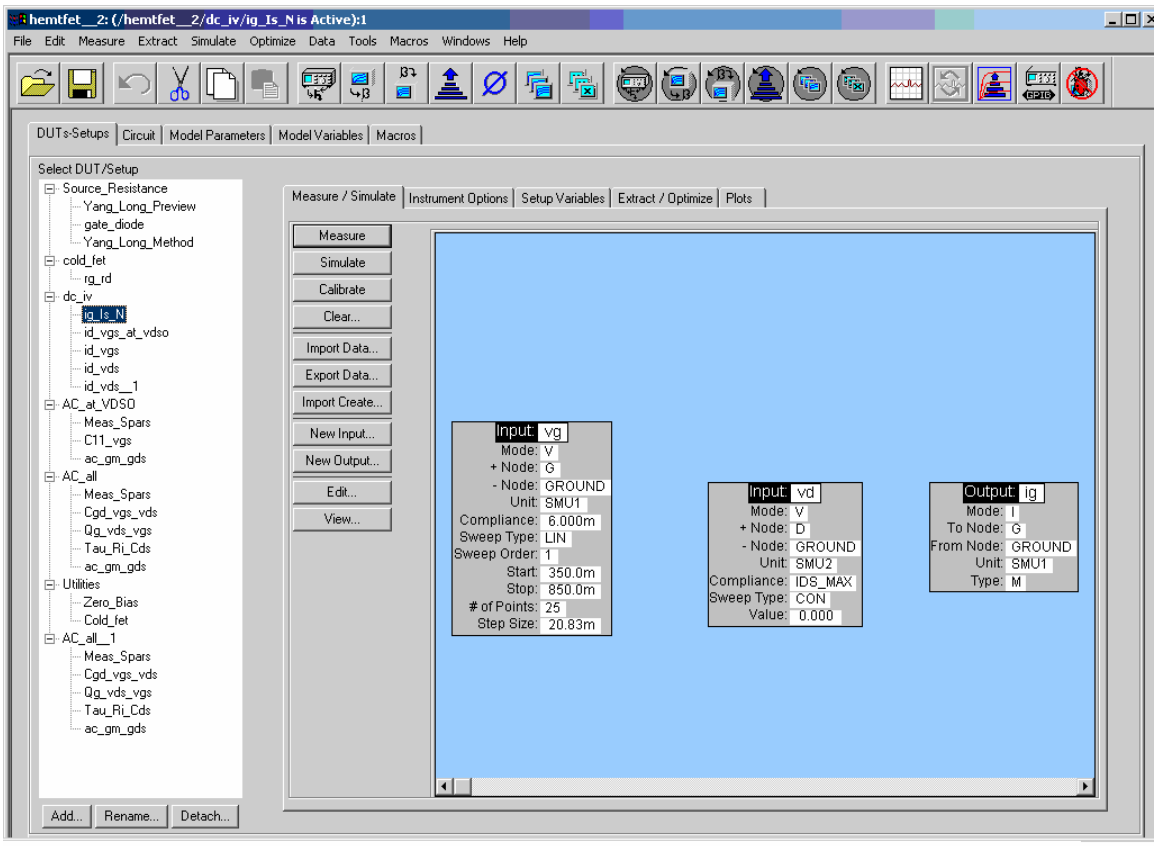


Figure 2.3. Template for ICCAP Measurement

2.2. IV Curves

Obtaining an accurate fit of the drain-source current (Ids) function to current-voltage (IV) curves is of utmost importance in being able to predict large-signal behavior. The IV curves can be thought as providing the boundaries for large-signal performance [2]. Figure 2.4 gives an intuitive description of the IV curve boundaries. The operation of the device is determined by a load line. The load line is based on the load impedance of the device, which includes the device parasitics [18]. The operation proceeds along the load line, with the boundaries of the signal swing being the maximum current on the upper end, the knee voltage on the left, zero current (threshold gate voltage) on the bottom, and drain-gate breakdown on the right. The load line shown in Figure 2.4 is a resistive load line and neglects output capacitance and device parasitics.

In fitting the IV parameters, it is helpful to first fit an I_D versus V_{GS} characteristic, as shown in Figure 2.5. This measurement should ideally be performed at a constant drain voltage

value close enough to the desired quiescent bias point of operation that the IV curves are similar, but at a low enough voltage that flattening of the characteristic can be observed.

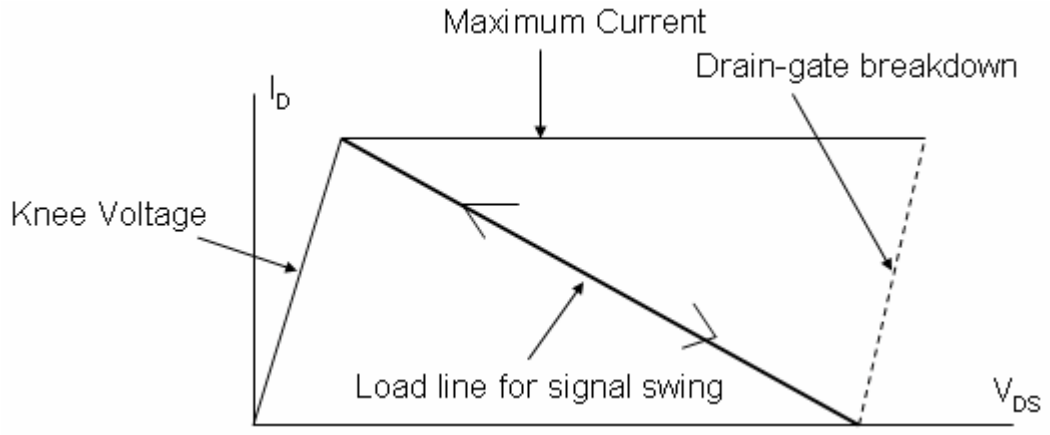


Figure 2.4. Intuitive Diagram of the Current-Voltage Boundaries

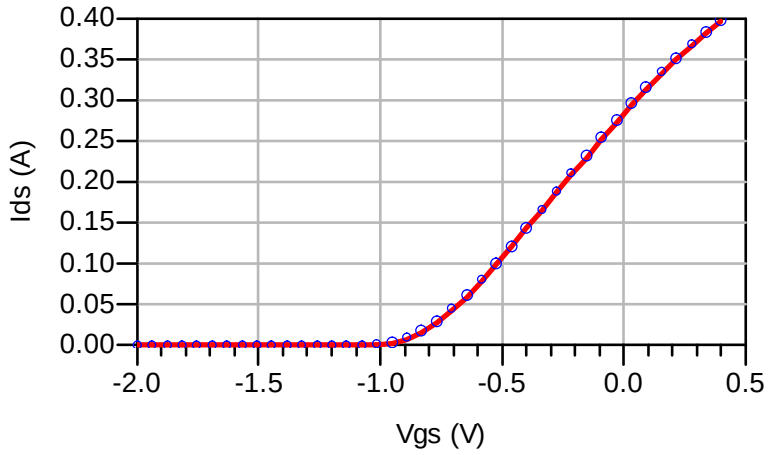


Figure 2.5. GaAs PHEMT I_D Versus V_{GS} Measured (Dots) and Simulated (Solid Line) Results

For many models, the IV tuning and optimization can be performed in ICCAP, in which the optimization setups are quite helpful. However, the work can also be performed in ADS by importing the measured data and using manual tuning to fit the characteristic. Once a reasonably close agreement has been achieved, an extraction of the remainder of the IV parameters should be

performed by fitting the I_D-versus-V_{GS} characteristic. Often this is done in more than one range; for example, a set of curves may be plotted for high V_{GS} and low V_{DS}. This ensures that a compromise, if necessary, is reached to provide an optimal fit in all areas that affect the signal swing of the device. Because the IV curves are used to determine the large-signal AC swing of the device, it is important that the boundaries of the operating region limiting the swing along potential load lines be extracted properly. Special attention should therefore be given to the knee region at high gate voltage and the threshold voltage for high drain voltages. Figures 2.6 and 2.7 show the results of the IV extraction for the GaAs PHEMT.

In many (if not most) cases, it is helpful to use pulsed IV measurements to extract a more accurate set of IV data, based on thermal and trapping considerations explained in the subsequent chapters. If pulsed measurements are used, it is important to take the pulsed IV measurements from a quiescent bias point as close to the design quiescent operating point as possible. It may also be helpful to consider the effect of load-line shift under large-signal operation and how this will affect IV behavior. However, for the example shown, static IV curves were used with temperature coefficients and the thermal resistance included as fitting parameters.

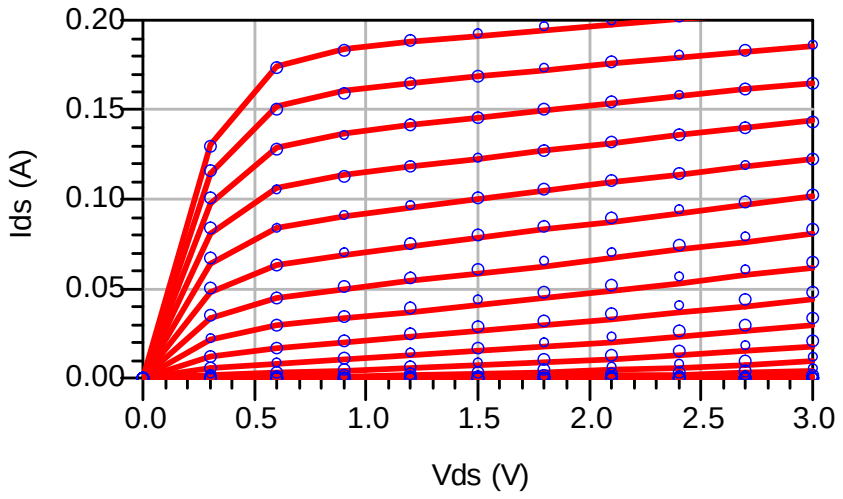


Figure 2.6. GaAs PHEMT Measured (Dots) and Simulated (Lines) IV Characteristics for V_{GS} from -1.5 V to -0.25 V, V_{DS} from 0 V to 3 V

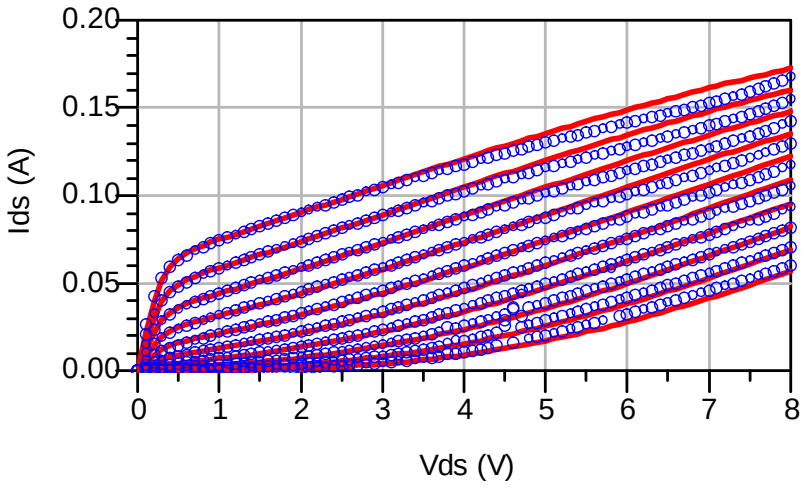


Figure 2.7. GaAs PHEMT Measured (Dots) and Simulated (Lines) IV Characteristics for V_{GS} from -1.5 V to -0.55 V, V_{DS} from 0 V to 8 V

2.3. Small-Signal S-Parameters for Capacitance Function and Parasitic Extraction

It is advisable to extract the parasitic element values: Rg, Rd, Rs, Lg, Ld, and Ls, and possibly shunt capacitances, before beginning the extraction of the intrinsic capacitance function parameters. An S-parameter measurement taken from bias point V_{GS} = 0 V, V_{DS} = 0 V can be used for this purpose. In the case of the EEHEMT model template in ICCAP, the Yang-Long method of finding source resistance is employed as part of the template. This measurement uses a zero drain bias and forward gate bias [19]. This leaves the other five parasitics to be extracted from the zero-bias S-parameters.

The ICCAP plots of the zero-bias S-parameter fits for the PHEMT up to 6 GHz are shown in Figure 2.8. In general, S_{11} can be used to extract Rg and Lg. To move the simulated characteristic toward the center of the Smith Chart, Rg should be increased, while to lengthen the characteristic, Lg should be increased. Ld and Rd can then be adjusted using the plot of S_{22} using a similar method: the inductance lengthens the characteristic, while the resistance moves the higher frequency portion toward the center of the Smith Chart. Because Rs and Ls can cause similar effects as the other parasitics, the S_{12} and S_{21} plots should then be consulted along with the S_{11} and S_{22} plots to determine a best-fit combination of the source parameters and gate and drain parasitics. The zero-bias simulation results also depend on the intrinsic model parameters, so it is

best to revisit the zero-bias S-parameters to adjust the parasitic element values after the capacitance functions. In addition, the values of Rd and Rs will affect the IV curves, so it is also advisable to check the IV curves for potential adjustments after parasitic extraction.

Following the parasitic extraction, the capacitance functions can be extracted. While an S-parameter comparison to 40 GHz was later performed, multiple-bias S-parameter data was initially measured to 6 GHz for the capacitance extraction. The multiple-bias data is put into formats in ICCAP to plot device port capacitances versus port voltages for the transistor. Essentially, parasitic element values are de-embedded from both the measurement and simulation, then desired port capacitance or transcapacitance values can be extracted from the Y- or Z-parameters of the device (taken from the S-parameters). A low frequency (for example, 500 MHz) should be used for extracting the capacitances, as parasitic elements begin to affect the S-parameters (and therefore the Z-parameters) at high frequencies. This operation can be set up in ADS as well. Figure 2.9 shows a plot of measured versus simulated C_{11} data versus gate voltage from ICCAP. Similar comparisons can be constructed for C_{12} and C_{22}. Definitions of these capacitances are given from the Y-parameters of the intrinsic model (not including the parasitics) as follows:

$$C_{11} = \mathrm{Im}(Y_{11}) \qquad (2.1)$$

$$C_{12} = \mathrm{Im}(Y_{12}) \qquad (2.2)$$

$$C_{22} = \mathrm{Im}(Y_{22}) \qquad (2.3)$$

In addition, it is advisable to ensure that the functions fit the plots of these capacitances versus drain voltage.

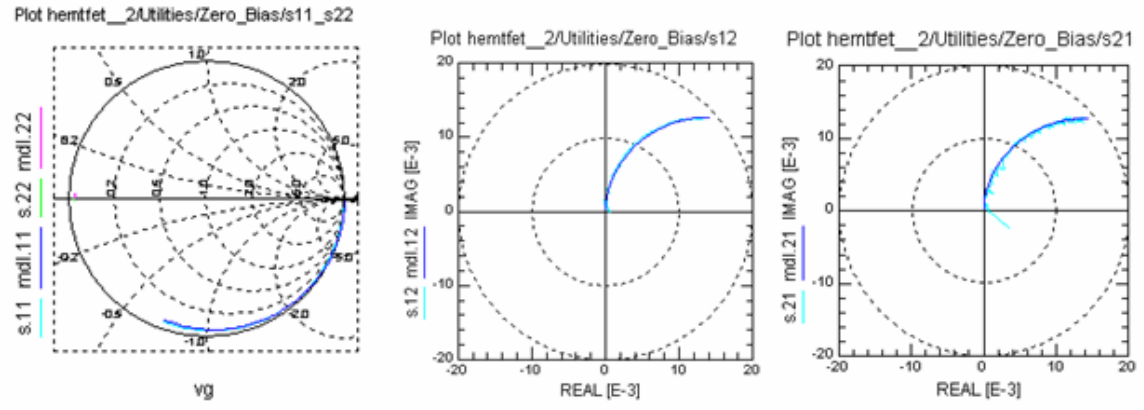


Figure 2.8. GaAs PHEMT Measured (Light Lines) and Simulated (Dark Lines) S-Parameters at V_{GS} = 0 V, V_{DS} = 0 V

After extraction of the capacitance functions, it is advisable to observe S-parameter fits at bias points surrounding the quiescent bias point of operation, as well as at (V_{GS} = 0 V, V_{DS} = 0 V). The full frequency range should be used in these comparisons. This allows manual tuning or optimization (often this step is performed in ADS) for improving the S-parameter fits at critical bias conditions. The S-parameter fits are determined by the IV and capacitance functions as well as parasitic elements. Figures 2.9 and 2.10 show measured-versus-simulated S-parameters to 40 GHz for the PHEMT at two quiescent bias points in the designed operating point range of V_{DS} = 4 V to 5 V.

At this point, several strategic adjustments can be made to improve model fitting. The drain-source capacitance often affects the length of the S_{22} characteristic on the Smith Chart; it also affects the shape of the $|S_{21}|$ characteristic. Adjusting the gate-drain capacitance equation parameters will alter S_{21} and S_{12}. The parameter Tau, present in many models, is the time delay of the gain and can be used to improve the fit of the phase of S_{21}.

At this stage of the modeling process, care should be taken to extract a model that matches the measured data quite well. While only a few bias points are examined, these points are the most critical and are likely very close to those that will be used for load-pull and power-sweep comparisons. Care spent at this point will help to make the load-pull and power-sweep comparisons match more optimally.

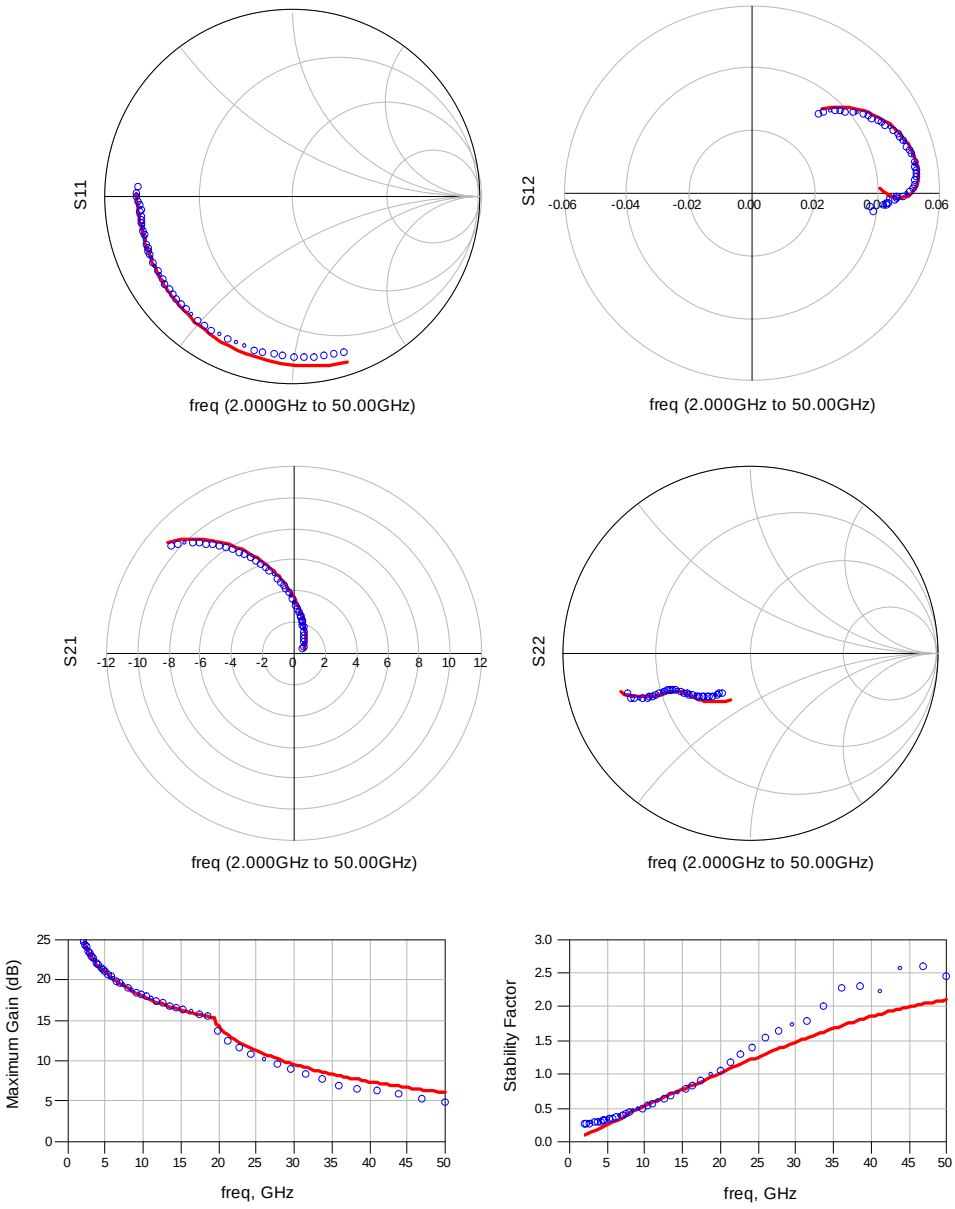


Figure 2.9. PHEMT S-Parameter Comparison Between Measured (Dots) and Simulated (Solid Lines) Data for V_{DS} = 4 V, I_{DS} = 72 mA

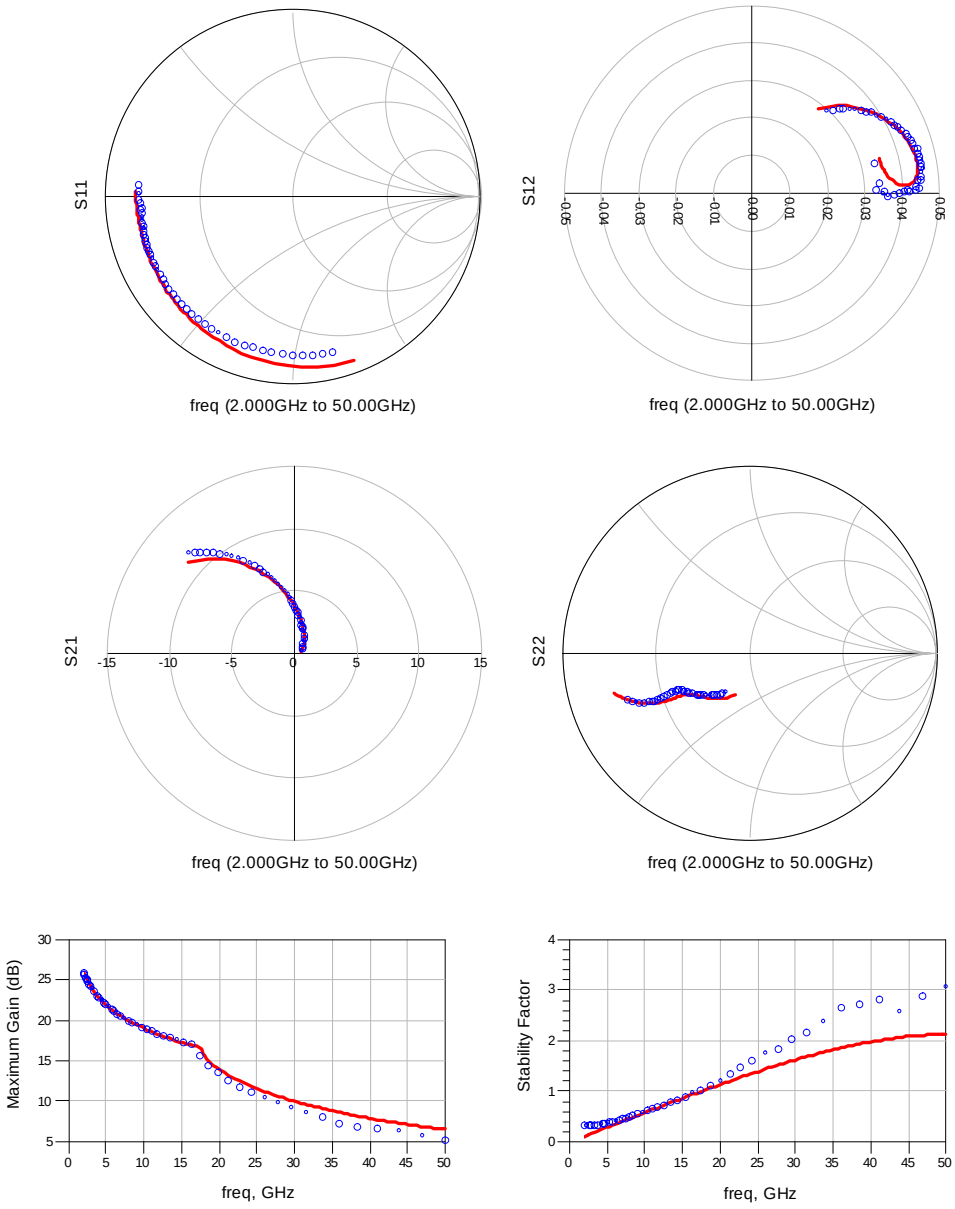


Figure 2.10. PHEMT S-Parameter Comparison Between Measured (Blue Dots) and Simulated (Red Lines) Data for V_{DS} = 5 V, I_{DS} = 126 mA

2.4. Power-Sweep and Load-Pull Comparisons

Power-sweep and load-pull measurement-to-simulation comparisons are often used to verify the large-signal performance of the model. If the model has been diligently extracted from IV and small-signal S-parameter simulations, the reward is often reaped in obtaining reasonable comparisons between measured and simulated data for the nonlinear power-sweep and load-pull measurements. Often, however, it will be noted from the large-signal comparisons that some parameter adjustments need to be made. The main purpose of this step, however, is to serve as large-signal verification of the results.

Power-sweep measurements provide different large-signal measures of the transistor as input power is increased. Figures 2.11 through 2.13 show transducer gain, power-added efficiency (PAE), and DC drain current, respectively, versus input power. Power-added efficiency is defined as

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}}, \qquad (2.1)$$

where $P_{RF,\,out}$ is the power in Watts of the first harmonic of the RF output signal, $P_{RF,\,in}$ is the power in Watts of the input RF signal, and P_{DC} is the input DC power [2]. Often compression parameters from the Ids equation can be adjusted if the gain is not optimal. However, if the shape of the simulated power sweep curve is not correct, it is often necessary to adjust a capacitance function parameter.

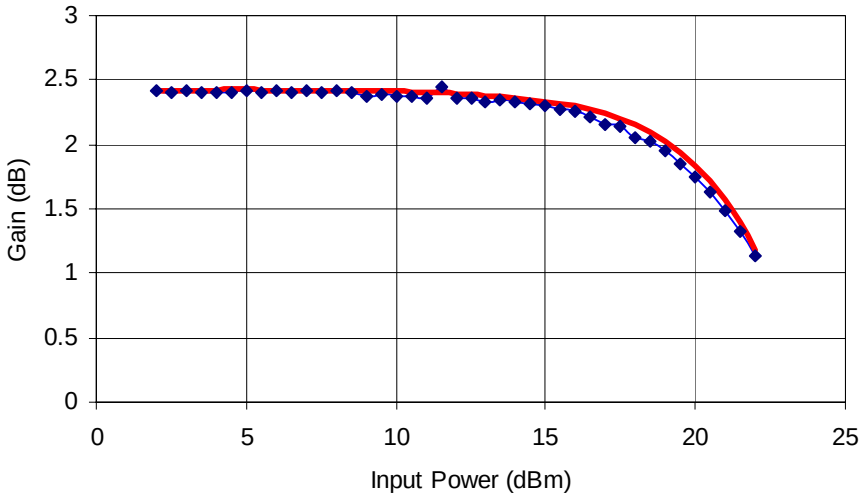


Figure 2.11. PHEMT Measured (Dots) and Simulated (Lines) Gain Versus Input Power for V_{DS} = 4.5 V, I_{DS} = 144 mA, with a Source Impedance of (23.711 – j1.789) Ohms and a Load Impedance of (18.751 + j5.151) Ohms

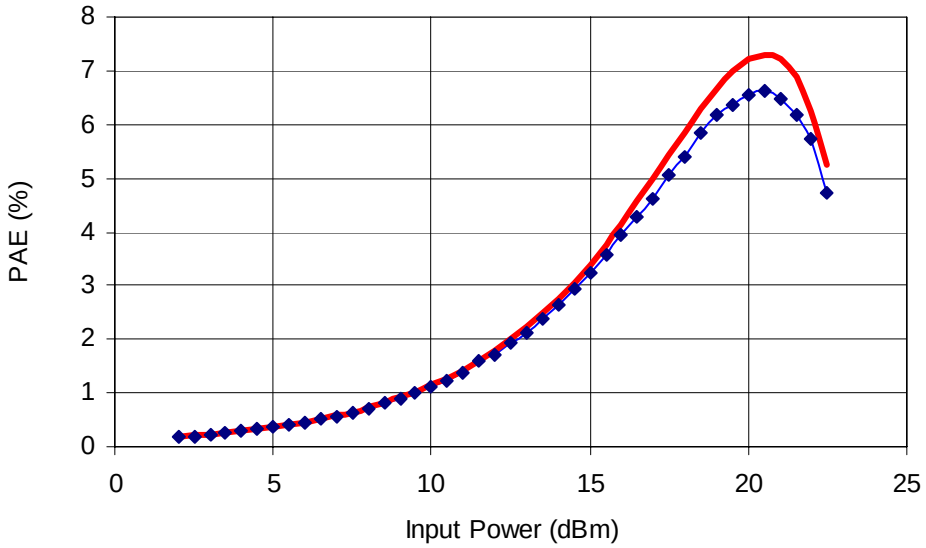


Figure 2.12. PHEMT Measured (Dots) and Simulated (Lines) Power Added Efficiency (PAE) Versus Input Power for V_{DS} = 4.5 V, I_{DS} = 144 mA, with a Source Impedance of (23.711 – j1.789) Ohms and a Load Impedance of (18.751 + j5.151) Ohms

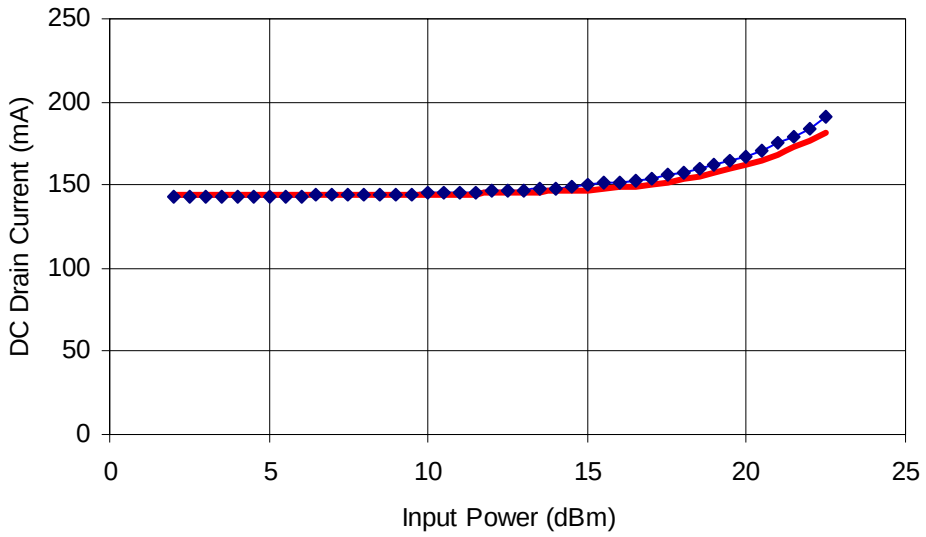


Figure 2.13. PHEMT Measured (Dots) and Simulated (Lines) Drain Current Versus Input Power for V_{DS} = 4.5 V, I_{DS} = 144 mA, with a Source Impedance of (23.711 – j1.789) Ohms and a Load Impedance of (18.751 + j5.151) Ohms

Finally, the load-pull measured-versus-simulation comparison should be performed. The simulation prediction of the load-pull position on the Smith Chart is heavily related to the output conductance (established by the partial derivative of the Ids function with respect to drain voltage) and the output capacitance. In many cases, due to test system losses, measurements cannot be performed beyond a certain radius on the Smith Chart, especially at higher frequencies. This was an issue with the case shown below. The measured and simulated 45 GHz load-pull results for the GaAs PHEMT are shown in Figures 2.14 and 2.15, respectively. For this comparison, the maximum measured output power is found to be 23.29 dBm, in comparison with a simulated value of 25.02 dBm; however, if the measurable radius were larger, it is likely that a higher power value would have been found at a higher-radius reflection coefficient state. In addition to these plots, it may often be helpful to perform a tabular comparison between the values of the maximum-power reflection coefficient and the output power values at these locations.

The resolution capabilities of a load-pull measurement and the parameter sweeps that can be performed are limited by available measurement time; however, a load-pull peak search algorithm is introduced later in this work that can allow for the maximum power impedance state and power value to be determined more efficiently and even plotted over varied parameters, such as power, bias, frequency, and process variation.

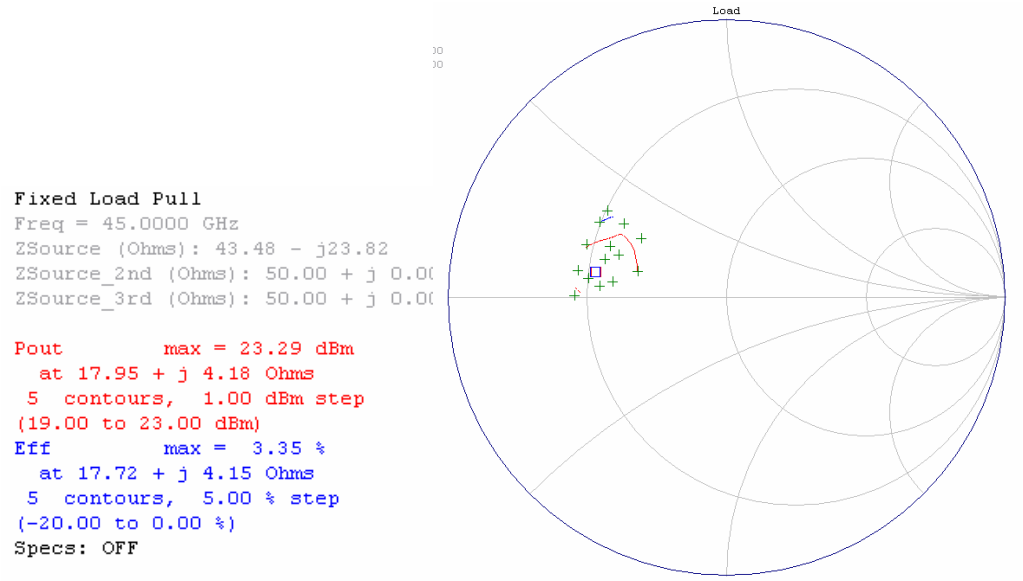


Figure 2.14. PHEMT Measured Output Power and PAE Load-Pull Results for a Bias of V_{DS} = 5 V, I_{DS} = 92.4 mA

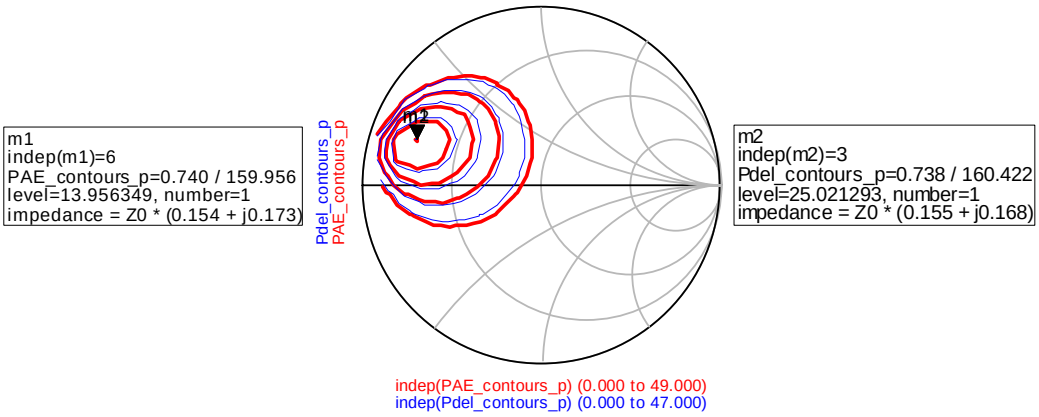


Figure 2.15. PHEMT Simulated Output Power and PAE Load-Pull Results for a Bias of V_{DS} = 5 V, I_{DS} = 92.4 mA

2.5. Chapter Summary

An outline of the extraction procedures for nonlinear FET models has been presented, through summarizing the development of a high-frequency model for a PHEMT. First, the equation for the drain current source is extracted to fit IV data. Second, parasitic element values are adjusted to fit small-signal S-parameter data taken with drain and gate bias voltages equal to zero. Capacitance functions can be extracted from voltage-swept S-parameter data and S-parameter results at bias conditions near the design operating quiescent point should be examined over the entire frequency range to ensure a good model fit. Finally, verification of the large-signal model capabilities should be performed with power-sweep and load-pull data. This chapter has summarized a typical large-signal model extraction procedure. In subsequent chapters, attention is given to improvements that can be made in obtaining the measurement data used to extract the models and modeling approaches that describe thermal and trapping conditions accurately.

CHAPTER 3: SELF-HEATING EFFECTS

Self-heating effects often play a significant role in determining the output characteristics of large devices. It is instructive to review some of the basics of device self-heating and methods that can be used to characterize this process in the development of improved methods to account for such effects in large-signal models. In this chapter, the effects of self-heating on transistor output characteristics are explored, followed by a review of methods used to obtain the thermal resistance of devices and a method for thermally correcting IV curves.

3.1. Physics of Self-Heating

Consideration of laws governing heat transfer through materials is quite valuable in allowing the conceptualization of electrothermal modeling. Thermal conductivity describes the ability of a material to allow heat transfer, much like electrical conductivity describes the ability of a material to allow electron flow. Kasap states that heat is transported in metals by the electron gas; that is, electrons are responsible for the distribution and dissipation of heat in the metal from a heat source [20]. In nonmetals, heat is conducted through lattice vibrations. Consider a block of material as shown in Figure 3.1. If the material is a metal, the rate of heat flow Q' is related to the cross-sectional area A of the material, the thermal conductivity κ, and the temperature gradient $\delta T/\delta x$ by the following equation [20]:

$$Q' = -A\kappa\frac{\delta T}{\delta x} \tag{3.1}$$

Equation (3.1) is known as Fourier's law of heat conduction. Fourier's law appears very similar to the following version of Ohm's law of electrical conduction:

$$I = -A\sigma\frac{\delta V}{\delta x}, \tag{3.2}$$

where I is the current, A is the cross-sectional area, σ is the conductivity, and $\delta V/\delta x$ is the electric potential gradient (voltage gradient). According to Kasap, because electrons participate in both heat and charge transportation, the thermal and electrical conductivities are thus related to each other [20] by an identity known as the Wiedemann-Franz Law.

$$\frac{\kappa}{\sigma T} = C_{WFL}, \qquad (3.3)$$

where C_{WFL} is a constant known as the Lorenz number:

$$C_{WFL} = \frac{\pi^2 k^2}{3q^2} = 2.44 \text{ x } 10^{-8} \text{ W } \Omega \text{ K}^{-2}. \qquad (3.4)$$

Electrical conductivity is inversely proportional to temperature for metals, so the thermal conductivity for metals is relatively independent of temperature [20].

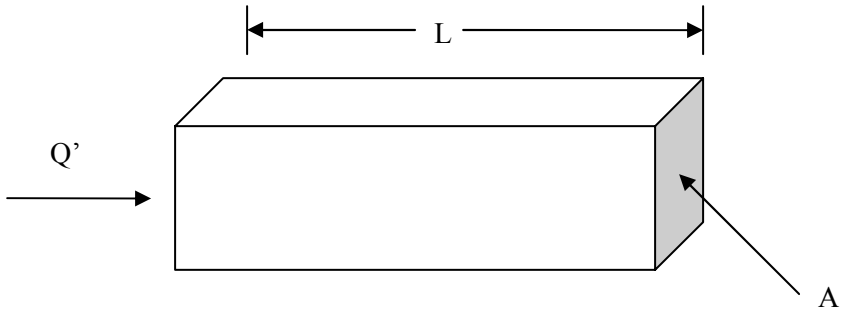


Figure 3.1. A Block of Material

For insulators, the transfer of thermal energy occurs through lattice vibrations; that is, the atoms in the crystal vibrate and the heat energy propagates through the crystal as a vibrational wave. Materials with stronger covalent bonds have atoms that are more closely coupled together, resulting in better heat transfer and thus higher thermal conductivity. Diamond has strong covalent bonds [20] and is presently being studied as a substrate for next-generation power devices due to its resultant high thermal conductivity.

For semiconductors, the thermal conductivity is composed of contributions from lattice vibrations, electron transportation, and mixed conduction [21], as shown in the following equation for the total thermal conductivity κ:

$$\kappa = \kappa_L + \frac{\left(\frac{5}{2} - s\right)k^2 \sigma T}{q^2} + \frac{k^2 \sigma T}{q^2} \frac{(5 - 2s + E_g / kT)^2 np\mu_n \mu_p}{(n\mu_n + p\mu_p)^2}, \qquad (3.5)$$

where κ_L is the thermal conductivity due to lattice vibrations, q is the unit charge associated with an electron, T is the temperature, s is a constant, n is the electron concentration, p is the hole

concentration, μ_n is the electron mobility, μ_p is the hole mobility, and E_g is the energy band gap, and k is the Boltzmann constant. The first term in equation (2.5) is the contribution from lattice vibrations, the second term is the contribution from electron conduction, and the third term is the contribution due to mixed conduction. Sze states that the third term can become fairly large if the energy bandgap $E_g >> kT$ [21]. For low temperatures, the thermal conductivity increases with increasing temperature due to the second term. For high temperatures, if $E_g >> kT$, the thermal conductivity decreases for increasing temperature due to the $1/T^2$ contribution from the third term. According to data for Ge, Si, and GaAs presented by Sze, the thermal conductivity decreases with increasing temperature at temperatures above 100 K, so thermal conductivity decreases with increasing temperature near typical room ambient conditions for these semiconductors [21]. This trend has also been noted by numerous other authors.

Nolas and Goldsmid state that for semiconductors with only one type of charge carrier (holes or electrons), the ratio of thermal conductivity to electrical conductivity is about the same as a metal, satisfying the Wiedemann-Franz Law of equation (3.3) [22].

The thermal resistance can be defined in terms of the thermal conductivity and the device geometry:

$$R_{th} = \frac{L}{\kappa A} \qquad (3.6)$$

The thermal resistance gives a measure of the resistance to heat flow of a material if a temperature source is placed on the material. For FET devices, the temperature source is electrical power dissipation. Transistor thermal resistance describes the amount of heat generated in the device channel for a given electrical power dissipation. For low-frequency electrical power dissipation P_D, the channel temperature T_C of the device is given by the following equation:

$$T_C = R_{th} P_D + T_A, \qquad (3.7)$$

where T_A is the ambient temperature.

3.2. The Electrothermal Subcircuit

Transistor self-heating is a time-dependent (and therefore frequency-dependent) phenomenon. The temperature of a device can be calculated through use of a thermal "circuit" analogy. This analogous circuit is shown in Figure 3.2 [23]; it is often used by nonlinear models to calculate the temperature in a device under a given excitation.

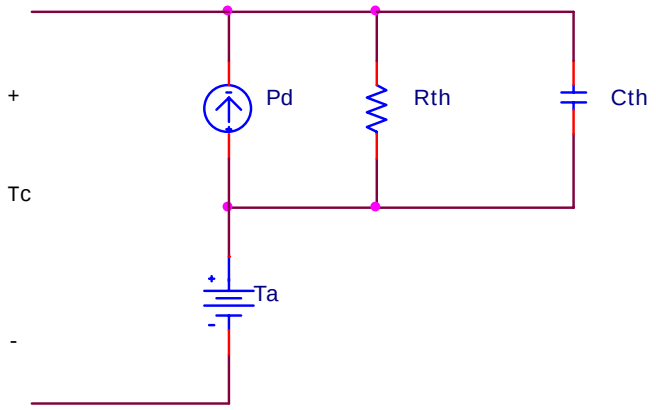


Figure 3.2. Thermal Subcircuit Used In Electrothermal Models

The channel temperature T_C of a device is given by the equation

$$T_C = Z_{th} P_D + T_A, \qquad (3.8)$$

where Z_{th} is the thermal impedance, P_D is the power dissipated in the channel of the device, and T_A is the ambient temperature. From Figure 3.2, the thermal impedance is given by the parallel combination of the thermal resistance and the thermal capacitance:

$$Z_{th} = R_{th} \,//\, \frac{1}{sC_{th}} = \frac{R_{th}}{1 + sR_{th}C_{th}} \qquad (3.9)$$

At high-frequency sinusoidal operation, $s = j\omega$ approaches infinity and

$$Z_{th}(s = j\omega \to \infty) = 0. \qquad (3.10)$$

At DC, $s = 0$ and

$$Z_{th}(s = 0) = R_{th}. \qquad (3.11)$$

Thus, a knowledge of R_{th} is sufficient to accurately and simultaneously predict both DC and continuous-wave RF behavior. However, in the situation of a more complex waveform, such as pulsed or modulated-signal behavior, a knowledge of C_{th} becomes important. Measurement techniques for the thermal resistance are reviewed here; measurement of the thermal capacitance is explored in Chapter 7. Conceptually, the thermal resistance tells how much the device channel is heated when an electrical power is dissipated in the channel.

3.3. The Effect of Heating on Device Characteristics

The effect of self-heating on transistor characteristics can be fairly significant. For example, IV curves measured in pulsed and static mode show tremendous differences, especially

for devices with significant values of thermal resistance. A good example of a device with significant self-heating effects is the VDMOSFET whose static and pulsed IV characteristics, measured at $T_A = 25$ ˚C, are shown in Figure 3.3. At large values of power dissipation, the static current sags greatly; take, for example, the curve corresponding to $V_{GS} = 8$ V. At $V_{DS} = 18$ V, the value of the current for the pulsed IV measurement is nearly 1200 mA, while the static IV measured current is less than 800 mA. This is a very large difference due to heating.

According to the results presented by Walker, Neidert, and Scott for MESFETs and by Sunde *et al.* for MOSFETs, current can be considered to be related to channel temperature by the following equation [24], [25], [26]:

$$\frac{I_{DS}(T_{C1})}{I_{DS}(T_{C2})} = \left(\frac{T_{C2}}{T_{C1}}\right)^{a}, \qquad (3.12)$$

where a is a material constant depending upon the doping concentration and the intrinsic material. The value of a is positive for most FET devices based upon results presented in the literature [26].

There are several approaches to estimating the thermal resistance of the IV curves for devices with minimal trapping effects; each is reviewed here. Two of the approaches to be considered are direct measurement approaches; the third is part of a model extraction approach that involves the extraction of the thermal resistance, along with the temperature coefficients of the current equation.

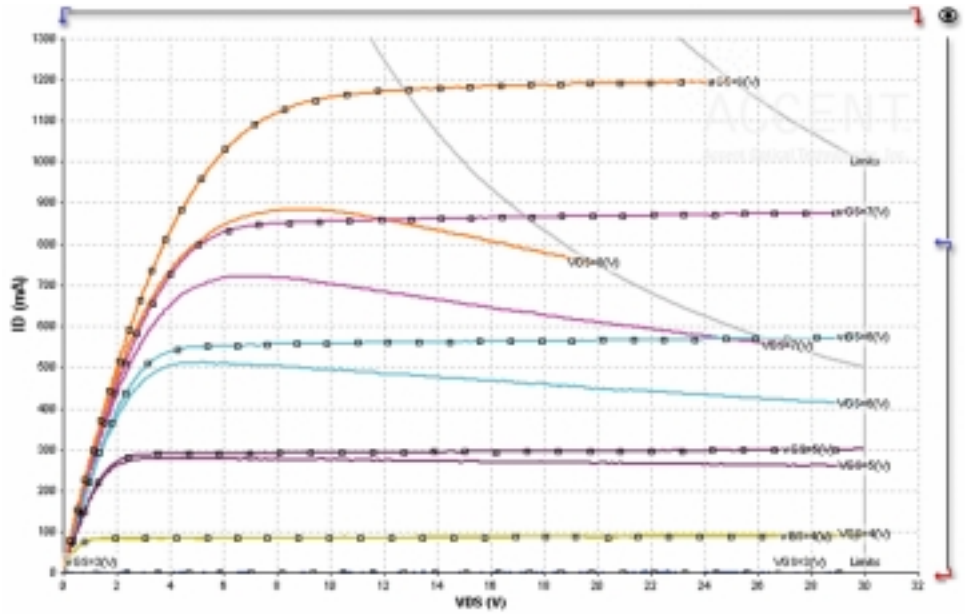


Figure 3.3. Static (No Squares) and Pulsed (Quiescent Bias: V_{DS} = 28 V, V_{GS} = 2 V, Lines with Squares) IV Curves at 25 °C to V_{DS} = 30 V

3.4. Thermal Resistance Measurement Techniques

From the circuit of Figure 3.2, the channel temperature at DC and low frequencies is related to the power dissipated in the channel by

$$T_C = R_{th} P_D + T_A, \qquad (3.13)$$

where R_{th} is the thermal resistance, P_D is the power dissipated in the channel of the device, and T_A is the ambient temperature. The $R_{th}P_D$ term accounts for the self-heating of the device. P_D is calculated using the signal drain voltage and current at DC and low frequencies, but the quiescent bias point voltage and current are used for the calculation for operation at frequencies significantly higher than the inverse of the thermal time constant [5] as follows:

$$P_D = V_{DSQ} I_{DQ} \qquad (3.14)$$

For high frequencies where the quiescent bias point has zero power dissipation, (3.13) reduces to

$$T_C = T_A. \qquad (3.15)$$

Based on (3.15), for short-pulse IV measurements from a quiescent bias point where no power is dissipated, the channel temperature is equal to the temperature of the thermal chuck on which the device is placed. In a short-pulse IV measurement from a quiescent bias point of nonzero power dissipation, P_D in equation (3.13) is calculated as the quiescent-point $V_D I_D$ product.

The extraction of thermal resistance using pulsed IV, presented in [5], is reviewed here. Using this theory, it was possible to measure the thermal resistance of a 1 Watt LDMOSFET cell supplied by Cree Microwave, Inc., for which the static and pulsed IV results are shown in Figure 3.4. The quiescent bias point for the pulsed IV curves is V_{GS} = 3.5 V, V_{DS} = 0 V, a bias point of approximately zero power dissipation. The droop seen in the static IV results in the region of high power dissipation is an indicator that this device exhibits significant thermal effects [27]. The curves were measured using a Accent Dynamic i(V) Analyzer (DiVA) model D225 [28]. A Cascade Summit 12000 Probe Station equipped with a temperature controller was used to perform measurements for different ambient temperatures.

First, pulsed IV results were measured with a quiescent bias point of zero power dissipation: V_{GS} = 3.5 V, V_{DS} = 0 V, for an ambient temperature T_{A1} = 75 ˚C. In this case, the channel temperature is equal to the ambient temperature, as described by (3.15). Another measurement was made with a quiescent point of nonzero power dissipation: V_{GS} = 5 V, V_{DS} = 5 V. For this measurement, the value of P_D in (3.13) is determined by the power dissipated at the quiescent bias point, calculated to be 0.3454 W. This measurement was repeated at different ambient temperatures until an optimal match was eventually achieved between the curves at T_{A2} = 47 ˚C. Figure 3.5 shows the V_{GS} = 8 V pulsed IV curve taken under three quiescent conditions: (A) V_{GS} = 3.5 V, V_{DS} = 0 V; T_A = 75 ˚C, (B) V_{GS} = 5 V, V_{DS} = 5 V, T_A = 75 ˚C, and (C) V_{GS} = 5 V, V_{DS} = 5 V, T_A = 47 ˚C. For setting (B), the curve is lower than the curve for setting (A), demonstrating that device self-heating is occurring due to the quiescent power dissipated in the device channel that causes the channel temperature to rise above the ambient level. In setting (C), the ambient temperature has been lowered to exactly compensate for the self-heating, and the curve is indistinguishable from the curve obtained for setting (A).

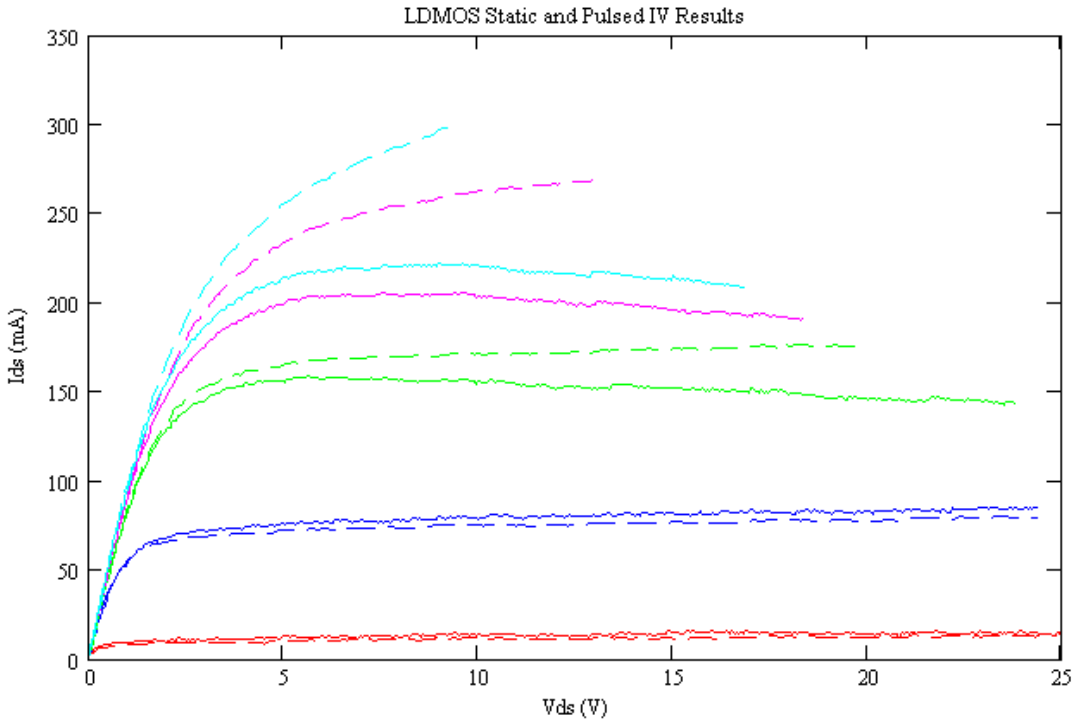


Figure 3.4. Static (Solid Lines) and Pulsed (Dashed Lines) IV Results for the LDMOSFET (V_{GS} = 4, 5, 6, 7, 8 V)

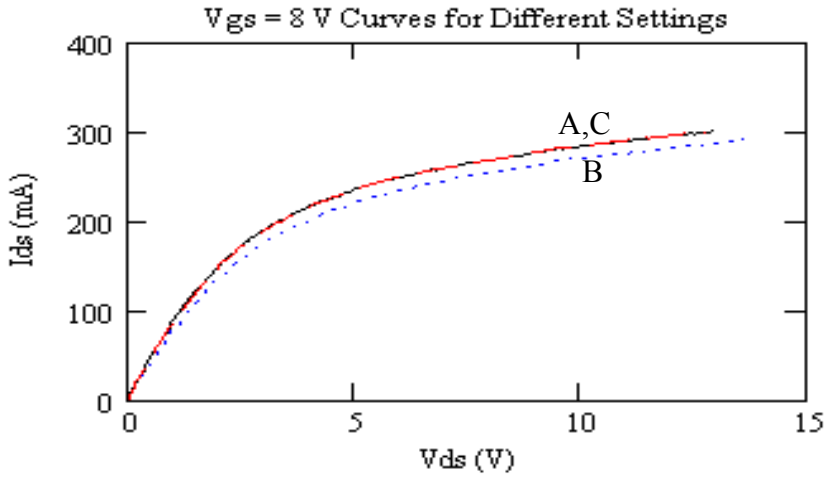


Figure 3.5. V_{GS} = 8 V Curves for (A) T_A = 75 ˚C, Quiescent Point: V_{GS} = 3.5 V, V_{DS} = 0 V (Zero Power Dissipation) (Solid Line); (B) T_A = 75 ˚C, Quiescent Point: V_{GS} = 5 V, V_{DS} = 5 V (Dotted Line); and (C) T_A = 47 ˚C, Quiescent Point: V_{GS} = 5 V, V_{DS} = 5 V (Dashed Lines, Indistinguishable from Curve Pertaining to Setting (A))

As pointed out by Jenkins, in the case of identical (V_{GS}, V_{DS}) points where I_D values are identical for two separate datasets (i.e. the IV curves cross), the device has roughly the same channel temperature [6], [29]. Thus, the channel temperatures for measurements of the curves with settings (A) and (C) are identical. The thermal resistance is obtained through use of (2.21) and the power dissipated in the channel:

$$75 = 0.3454R_{th} + 47$$
$$R_{th} = 81.06\ ^{\circ}\text{C/W}$$

A similar measurement technique was used for several quiescent bias settings and ambient temperatures. The overall average measured thermal resistance is 75.7 ˚C/W.

The results obtained using this thermal resistance measurement method were verified using a similar method developed by Jenkins [6], as shown in [5]. In this method, static and pulsed IV curve crossings are examined for different temperatures. The thermal resistance obtained from this method was 71.5 ˚C/W. This is close to the 75.7 ˚C/W obtained from the method developed in this work.

A third method of thermal resistance extraction is through the use of a nonlinear electrothermal model. In this case, the model current parameters are extracted for the nominal ambient temperature from pulsed IV data with a quiescent bias point of zero power dissipation. Second, the parameters describing the dependence of the current on temperature are extracted from another pulsed IV measurement, taken again at a quiescent bias point of zero power dissipation, but at a different chuck temperature. The extraction to fit these curves should be performed using only the temperature coefficients. Finally, a static IV measurement should be performed and the fitting should be accomplished by adjusting only the thermal resistance parameter.

Direct measurement of thermal resistance using optical and infrared techniques is also possible in many cases. Commercial infrared cameras with fine resolution are available [30] that perform a pixel-by-pixel emissivity correction, followed by the measurement of the temperature on a pixel-by-pixel basis. The maximum point temperature can be ascertained and used to calculate the thermal resistance. Chapter 8 contains an example of infrared measurement results.

3.5. Modeling the Temperature Dependence of IV Curves

Generation of IV curves with the correct temperature dependence is performed by the inclusion of temperature coefficients in nonlinear models. Temperature coefficients are

parameters within the model that determine the change of a certain model parameter for a unit increase in temperature. For example, in the Angelov model [12], there are three parameters in the IV equation that change with temperature; these parameters are IPK0, the current at the peak transconductance gate voltage; P1, part of the linear V_{GS} polynomial coefficient; and LSB0, a parameter that gives part of the breakdown information concerning the device. The corresponding temperature coefficients for these parameters are TCIPK0, TCP1, and TCLSB0, respectively. The model equations for these parameters are as follows [31]:

$$\text{Ipk0} = \text{IPK0} \times (1+\text{TCIPK0} \times (\text{Temp} - \text{Tnom})) \quad (3.16)$$

$$\text{P1} = \text{P1} \times (1 + \text{TCP1} \times (\text{Temp} - \text{Tnom})) \quad (3.17)$$

$$\text{Lsb0} = \text{LSB0} \times (1 + \text{TCLSB0} \times (\text{Temp} - \text{Tnom})) \quad (3.18)$$

The temperature coefficients should be extracted from pulsed IV measurements performed for the same quiescent bias condition but at different ambient temperatures. A substantial temperature difference should be used between these two measurements to ensure an accurate extraction of the temperature coefficients.

The temperature is calculated using (3.13) from the ambient temperature and the self-heating. Based on this temperature, the values of the above model parameters are calculated and the model is generated. All of the variations of the Angelov parameters with temperature are assumed to be linear.

3.6. Thermal Time Constant Measurement

The above sections have shown how to measure the thermal resistance of the thermal subcircuit shown in Figure 3.2. Attention is now directed to the extraction of the thermal capacitance. The capacitance can be found from the thermal time constant using the following relationship that can be derived from the circuit of Figure 3.2:

$$\tau_{th} = R_{th} C_{th} \quad (3.19)$$

From the circuit of Figure 3.2, the channel temperature is given by the equation

$$T_C = Z_{th} P_D + T_A, \quad (3.20)$$

where Z_{th} is the thermal impedance, P_D is the power dissipated in the channel of the device, and T_A is the ambient temperature. From the circuit, the thermal impedance is the parallel combination of the thermal resistance and the thermal capacitance and is expressed in the complex-frequency domain as

$$Z_{th} = R_{th} \,//\, \frac{1}{sC_{th}} = \frac{R_{th}}{1 + sR_{th}C_{th}}. \qquad (3.21)$$

For a short-pulse IV measurement from a quiescent bias point with $P_D = 0$, the thermal capacitor will be seen by the new power dissipation as a short circuit, so the channel temperature is given by

$$T_C = T_A. \qquad (3.22)$$

The thermal circuit can be considered as a system whose input is the power dissipation P_D and whose output is the change in channel temperature $\Delta T_C = T_C - T_A$. The transfer function of this system is thus defined as

$$H(s) = Z_{th}(s) = \frac{\Delta T_C(s)}{P_D(s)}, \qquad (3.23)$$

which can be identified as the thermal impedance. From (3.21) this transfer function is

$$Z_{th}(s) = \frac{R_{th}}{1 + sR_{th}C_{th}} = \frac{\frac{1}{C_{th}}}{s + \frac{1}{R_{th}C_{th}}} \qquad (3.24)$$

If a step increase in power dissipation is applied as the input, then

$$P_D(t) = P_D u(t) \qquad (3.25)$$

is the time-domain input, with Laplace transform

$$P_D(s) = \frac{P_D}{s}. \qquad (3.26)$$

The output $\Delta T_C(s)$ in the Laplace domain is equal to the product of the Laplace-domain representations of the transfer function and the input:

$$\Delta T_C(s) = Z_{th}(s)P_D(s) = \frac{\frac{P_D}{C_{th}}}{s\left(s + \frac{1}{R_{th}C_{th}}\right)}. \qquad (3.27)$$

This can be expanded using partial fraction expansion:

$$\Delta T_C(s) = \frac{R_{th}P_D}{s} - \frac{R_{th}P_D}{s + \frac{1}{R_{th}C_{th}}}. \qquad (3.28)$$

Taking the inverse Laplace transform gives the change in channel temperature as a function of time:

$$\Delta T_C(t) = R_{th} P_D (1 - e^{-t/R_{th}C_{th}}) u(t). \qquad (3.29)$$

From this expression, the thermal time constant (given by equation (3.19)) is the time at which the channel temperature has made approximately 63.2 percent of its change from its initial value to the steady-state value.

In many cases, a more accurate fit can be obtained to measured transient thermal characteristics through the use of additional thermal RC networks [32]. Yang *et al.* have proposed a network with parallel combinations of thermal resistance and capacitance in series. A general multiple-pole thermal network of this kind is displayed in Figure 3.6. It can be shown that the transient thermal impedance for the general nth order thermal network is given by

$$Z_{th}(t) = \sum_{i=1}^{N} R_i (1 - e^{-t/R_i C_i}), \qquad (3.30)$$

giving the following expression for channel temperature:

$$T_C(t) = P_D \sum_{i=1}^{N} R_i (1 - e^{-t/R_i C_i}) + T_A. \qquad (3.31)$$

Extraction of the thermal time constant can be performed using the results of a drain voltage transient measurement. The setup for this experiment is shown in Figure 3.7. A similar setup is shown to be used for a similar extraction in [14]. The experimental setup consists of the application of DC voltage V_{DD} and a step voltage $v_G(t)$. The drain voltage $v_D(t)$ is monitored on an oscilloscope. The initial value of the gate voltage is chosen below the threshold voltage of the device. With the gate voltage at this value, no current is being conducted through the drain of the FET, so no voltage is dropped across the resistor. The value of the drain voltage $v_D(t) = V_{DD}$. The gate voltage is then stepped to a value that causes significant bias current to be conducted (and thus significant self-heating to occur). Current begins to flow through the drain and also the resistor, causing the voltage across the resistor to increase. The drain voltage thus decreases. However, as the device begins to heat up, the current decreases, causing the voltage drop across the resistor to decrease and the drain voltage $v_D(t)$ to increase. This transient increase in $v_D(t)$ can be fit with an exponential function; the time constant of this exponential is the thermal time constant and can be used, along with knowledge of the thermal resistance, to calculate the thermal capacitance.

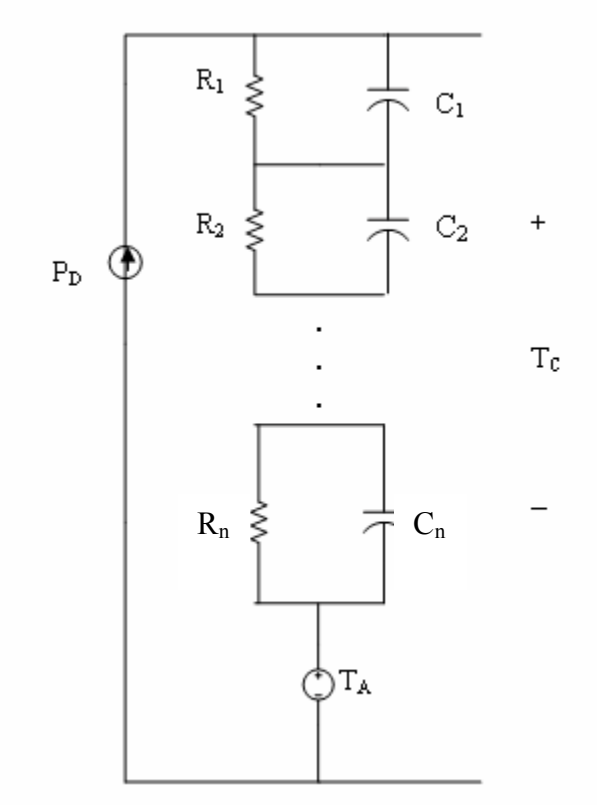


Figure 3.6. General nth Order Thermal Circuit

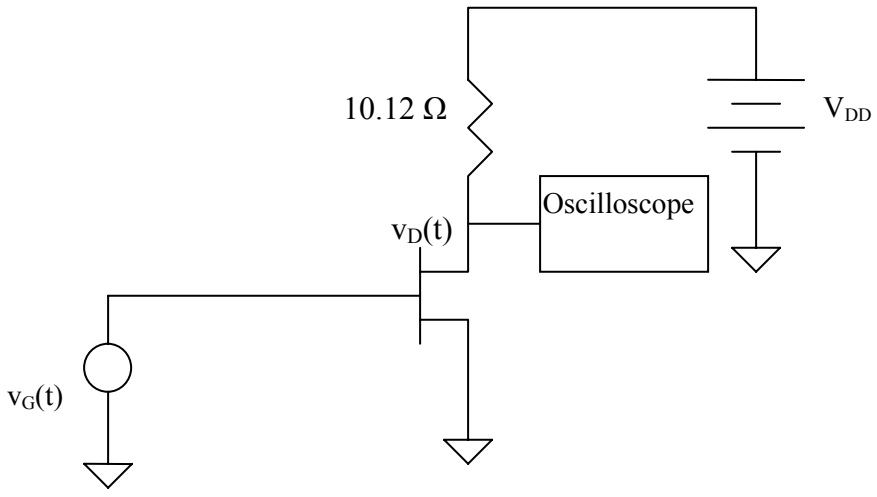


Figure 3.7. Experimental Setup for Transient Measurement

Theoretically, it can be shown that the time constant of the voltage transient is the same as the time constant of the current exponential. It has been shown for a FET that if the temperature increases exponentially, the current decreases exponentially with the same time constant [5]. Assuming that, for time t after the step in gate voltage, the current is given by the function

$$i(t) = A + Be^{-t/\tau_{th}}, \qquad (3.32)$$

then the drain voltage is given by the function

$$v_D(t) = V_{DD} - Ri(t), \qquad (3.33)$$

where R is the resistor in series with the drain in Figure 1. Thus

$$v_D(t) = V_{DD} - R(A + Be^{-t/\tau_{th}}). \qquad (3.34)$$

or

$$v_D(t) = C - De^{-t/\tau_{th}}. \qquad (3.35)$$

This functional form can be fit by finding C, D, and τ_{th} to best fit the voltage transient graph. Thus, the time constant of the voltage transient is the thermal time constant.

This method was used to extract the thermal time constant for a Si VDMOSFET. Two transient measurements were performed. In the first measurement, V_{DD} = 16 V and V_G was stepped from 0.3 V to 7.2 V. The measured results are shown, along with a fit of equation (3.35), in Figure 3.8. In equation (3.35), C = 9.2, D = 0.65, and τ_{th} = 0.25 ms. It can be seen that the measurement results are relatively noisy; however, the exponential shape of the drain voltage with time is visible. The noise is a result of the large DC component in the waveform. Because of the transient analysis, AC coupling could not be used on the oscilloscope. Because of this, the resolution with which the scope could be adjusted to view this signal was limited.

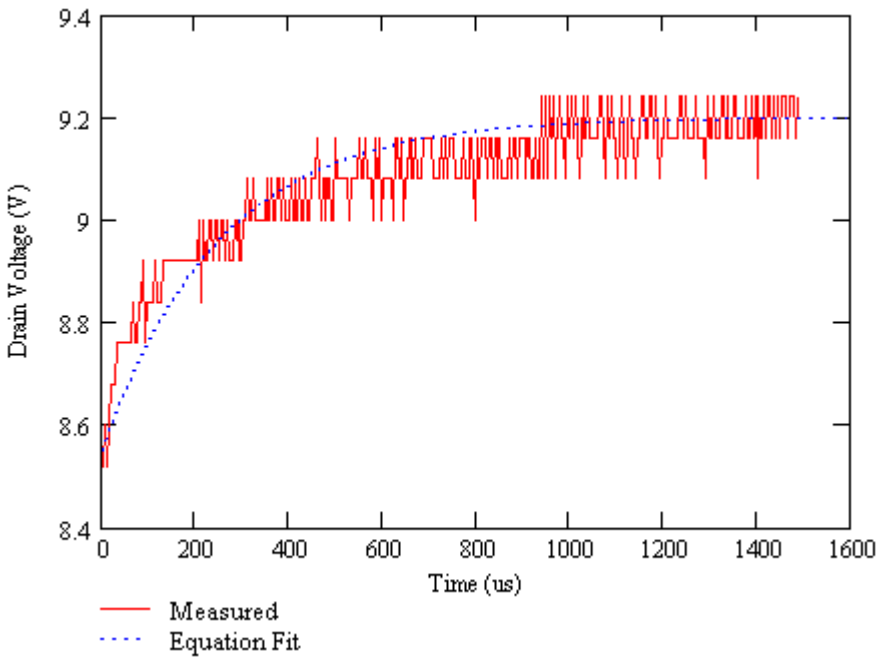


Figure 3.8. Drain Voltage Versus Time for Measured Results and Equation (3.35) Fit: V_{DD} = 16 V and V_G from 0.3 V to 7.2 V

As mentioned above, adding an additional parallel RC component to the thermal circuit can help in producing a more accurate fit to the model. This was attempted for this experiment. In the case of the two-pole circuit, the form of the drain voltage is

$$v_D(t) = F - Ge^{-t/\tau_1} - He^{-t/\tau_2} \qquad (3.36)$$

For the fit shown in Figure 3.9 for this measurement, the values used are F = 9.2, G = 0.4, τ_1 = 0.1 ms, H = 0.25, τ_2 = 0.6 ms. It can be seen from the Figure 3.9 plot that the equation seems to fit better in the time region of the rise in voltage, whereas the one-pole fit is reasonable but is not optimal in this region.

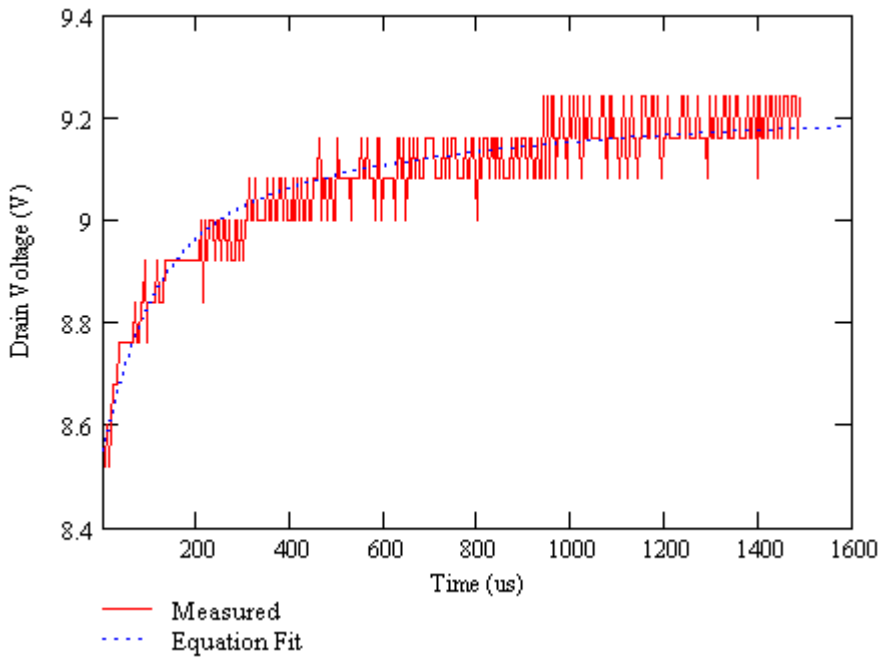


Figure 3.9. Two-Pole Fit to Measured Transient Data: V_{DD} = 16 V and V_G from 0.3 V to 7.2 V

A second experiment was performed. For this experiment, V_{DD} = 13.96 V and V_G was stepped from 0.3 V to 7.2 V. A single-pole fit was performed to the measured data. The results are provided in Figure 3.10. The fitting coefficients used in equation (3.32) were A = 6.96, B = 0.4, and τ_{th} = 0.25 ms. Notice that the same value for the thermal time constant was used as for the other voltage configuration. The double-pole results are shown in Figure 3.11. The values of the terms in equation (3.36) used were F = 6.96, G = 0.2, τ_1 = 0.1 ms, H = 0.2, τ_2 = 0.6 ms.

From both experiments, it appears that the double-pole fit may provide a slight improvement in the prediction of the transient. It appears that the ability to view the effectiveness of the fit is blurred due to the lack of resolution on the oscilloscope; however, the region of increase appears to be slightly more optimally fit with more poles. However, the single-pole thermal circuit appears to serve as a reasonable approximation to describe time-dependent thermal behavior in this case.

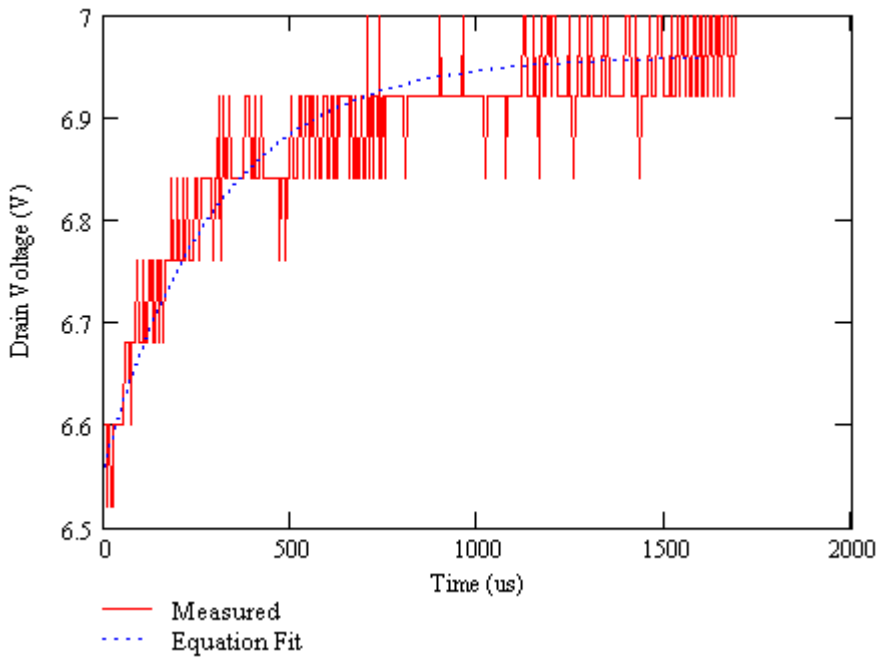


Figure 3.10. Drain Voltage Versus Time for Measured Results and Equation (3.35) Fit: V_{DD} = 13.96 V and V_G from 0.3 V to 7.2 V

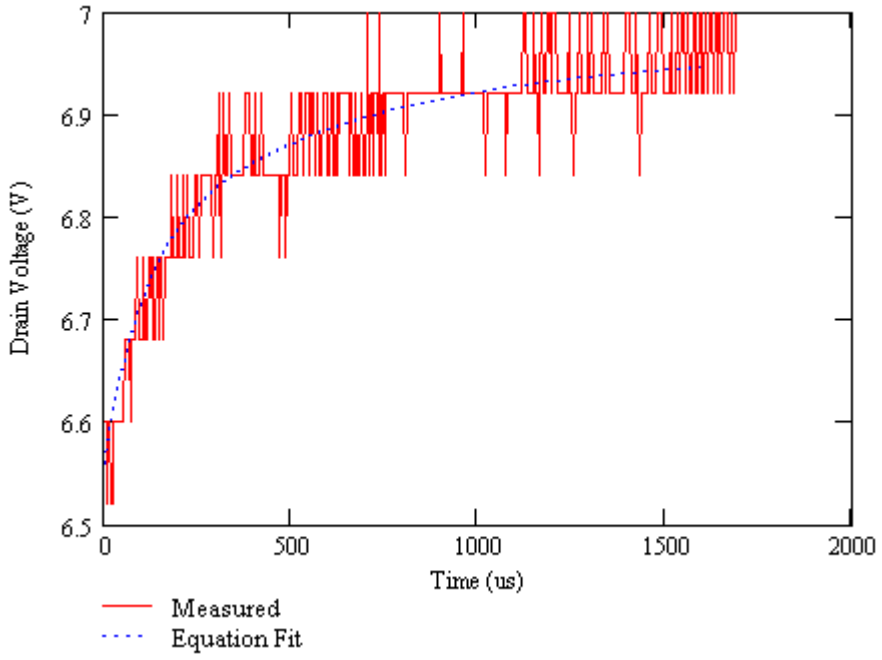


Figure 3.11. Two-Pole Fit to Measured Transient Data: V_{DD} = 13.96 V and V_G from 0.3 V to 7.2 V

3.7. Chapter Summary

Thermal resistance describes the temperature increase in a block of material due to electrical power dissipation. An electrothermal analogous circuit can be used for calculation of the channel temperature due to a given ambient temperature and power dissipation. In addition to thermal resistance, a device possesses at least one thermal time constant, leading to a thermal capacitance; this represents the time necessary for heat to be generated from an applied power dissipation.

Methods have been described that allow the thermal resistance to be measured for devices with minimal amounts of trapping, such as Si LDMOSFETs. In these methods, pulsed and/or static IV curves taken at different temperatures and quiescent bias conditions are compared to determine the thermal resistance. Using temperature coefficients that can be extracted from IV curve sets measured at different temperatures, a nonlinear electrothermal model can generate a set of IV curves with an accurate temperature dependence.

The thermal time constant, which along with the thermal resistance is used to determine the thermal capacitance, can be extracted using transient drain voltage measurements with a resistor placed in series with the drain of the transistor. The drain voltage transient is measured following a step input to the gate. The time constant of the drain voltage response is the thermal time constant. It appears that the single-pole exponential is quite effective in describing the thermally induced voltage change with time; furthermore, it appears that the addition of a second pole may increase the effectiveness of the thermal circuit to describe the time-dependent thermal behavior.

CHAPTER 4: TRAPPING EFFECTS

A second slow effect that causes time dependence of the device operating characteristics is the trapping effect. Trapping can be defined as the interchange of electrons between the conduction or valence band and a trap state located in the energy bandgap. Trapping can exist in two locations in FETs and HEMTs: (1) in the substrate beneath the channel and (2) at the surface of the device between the gate and drain. An intuitive description is provided in this chapter about trapping effects; furthermore, a strategy to determine the type(s) of trapping present in a device is presented and demonstrated.

4.1. Interaction of Electrons with Trap States

Electrical current consists of the flow of electrons. In semiconductor materials, the current consists of the flow of electrons through the conduction band and holes through the valence band. Because current is defined as charge per time (i.e. the flow of charge), it is dependent upon the number of electrons in the conduction band and the number of holes in the valence band. This charge can be affected by energy levels in between the bands that can "trap" electrons. These energy levels are considered in two different categories.

Recombination centers are usually located near the center of the energy bandgap. At these centers, a hole is first captured, followed by the capture of an electron. This causes an electron-hole pair to disappear, lowering the current through the semiconductor [33]. Trapping centers in the bandgap are often closer to the band edge and temporarily "trap" an electron or hole, but often release the carrier before recombination can occur. Trapping centers closer to the conduction band or valence band generally have time constants that are smaller than trapping or recombination centers closer to the center of the bandgap [33]. The energy band diagram of Figure 4.1 gives a simplistic description of the trap locations.

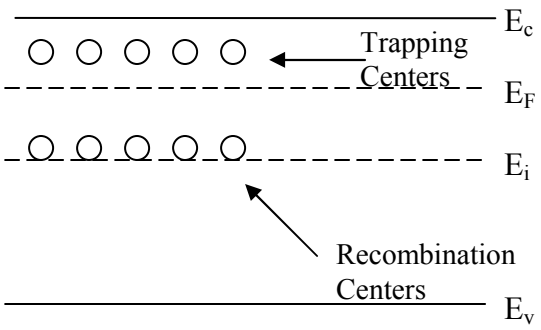


Figure 4.1. Energy Band Diagram of n-Type Semiconductor Including Trap Centers and Recombination Centers

The two basic effects that occur with trap states are electron capture by a trap state and electron emission from a trap state. The basic equation governing the density of filled trap states during electron capture is the following [34]:

$$n_T(t) = N_T - [N_T - n_T(0)]e^{-t/\tau_c}, \qquad (4.1)$$

where $n_T(t)$ is the density of filled trap states at time t, N_T is the density of available trap states, $n_T(0)$ is the number of filled states at the beginning of the capture process, and τ_c is the capture time constant. On the right side of equation (4.1), the first term (N_T) represents the density of trap states, while the second term represents the density of empty trap states at time t. The density of empty trap states exponentially decreases with time. Impurities that serve as trapping or recombination centers can be donors (having a positive charge when ionized) or acceptors (negative charge when ionized) [33].

The equation governing the density of filled trap states during electron emission is the following:

$$n_T(t) = n_T(0)e^{-t/\tau_e} \qquad (4.2)$$

The process is exponential; however, the time constant of the process is the emission time constant, τ_e.

What causes a change in the trapping state of a device? One contributor is voltage. In a field-effect transistor, the application of different drain and gate voltages changes the availability of electrons in different regions of the device that are susceptible to traps. A second contributor is temperature. Augaudy *et al.* state that trap effects are linked to temperature and that the

temperature affects the time constant of the effect. For example, thermal energy from a light source decreases the emission time constant, causing a rise in device drain current [35].

Consider an n-channel FET-type device (FET or HEMT). In such a device, the current consists of the flow of electrons through a doped channel. The channel width is controlled by the gate voltage, which, as it is decreased, results in a smaller channel (electrons are pushed away from the gate) and if increased, results in a larger channel. The number of electrons available to be swept through the channel, the channel size, and the electric field determine the amount of current passing through the device. Trapping states, however, exist in many compound semiconductor devices such as GaAs and GaN devices that can capture, or "trap", electrons attempting to contribute to current flow. There are two locations where trap states exist that tend to affect the current flow: the surface of the device between the drain and gate and the substrate level (Figure 4.2) [36].

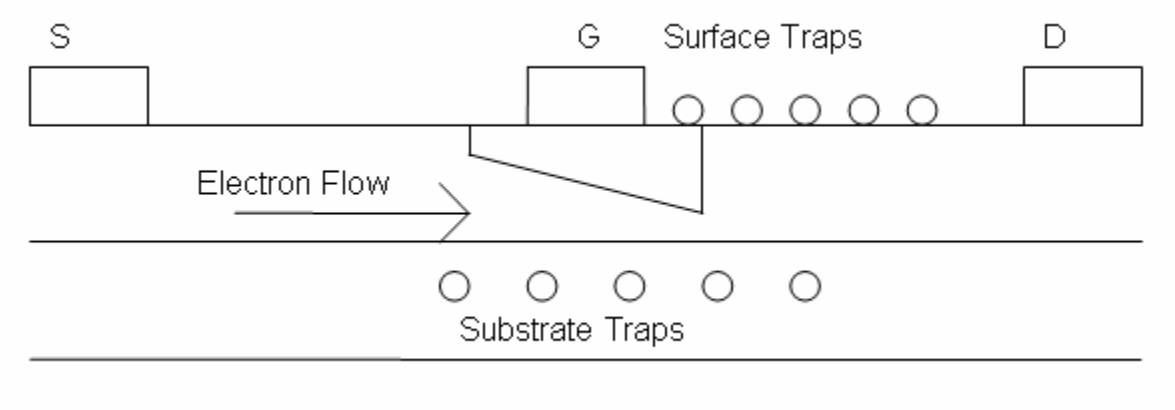


Figure 4.2. Locations of Substrate and Surface Traps

Substrate traps lie in the substrate beneath the channel and can cause a drain-lag effect, which is a slow change in drain current in response to a drain voltage step. Substrate traps can also cause gate-lag effects under certain conditions [37]. As the drain-source electric field is increased due to a step in the drain-source voltage, more electrons are swept through the channel. Many of these electrons are captured by substrate traps, a process that has a time constant on an order as low as nanoseconds [38]. If the drain voltage is decreased, the electrons will be emitted from the substrate traps, a process that is much slower than the capture process (on the order of milliseconds). Thus, a general rule has been set up by Siriex *et al.* for trap dependence based on the drain quiescent voltage V_{dsQ} and the "pulse-to" drain voltage V_{dsp} [38]:

Case 1: $V_{dsp} < V_{dsQ}$. Electrons begin to be emitted from substrate traps on pulse application. The emission time constant is significantly longer than the pulse length in short-pulse IV, and the trap state is dependent on V_{dsQ}.

Case 2: $V_{dsp} > V_{dsQ}$. Electrons are captured by substrate traps on application of the pulse. The capture process time constant is usually shorter than the pulse length and the trap state at the measurement time is dependent on V_{dsP}.

Surface states are often seen to produce a gate-lag; that is, a slowly changing current response to a step in gate voltage. During device operation, the difference between drain and gate voltages produces an electric field on the surface between the drain and gate that is highest near the gate electrode [4]. The number of filled surface trap states depends on the value of this electric field, which is dependent on the drain-gate voltage. The drain-gate electric field can be increased by making the gate voltage more negative (in a depletion-mode device) or by increasing the drain voltage. Thus the surface state occupancy is expected to be dependent upon both V_{GS} and V_{DS}.

A comprehensive study of the effects of surface traps in GaN/AlGaN HEMTs through simulation and pulsed IV measurement has been recently performed by Meneghesso *et al.* [39]. This paper states that whether the surface trapping is considered to be due to holes or electrons, the time constants for the trapping effects are approximately the same for similar processes. Thus electron capture and hole emission have similar time constants and occur under similar bias configurations, while electron emission and hole capture are also similar in these regards. In their work, it is shown that a pulse applied from high (less negative) gate voltage to lower (more negative) gate voltage causes hole emission (electron capture), a process which has a fairly short time constant. In this case the drain current reaches the new steady-state condition fairly quickly. Plots provided by Meneghesso show about 10 to 100 ns; the pulse length used in pulsed IV measurement is usually 100 to 200 ns [39]. The same response to surface states is shown to occur when the pulsing occurs from low to high drain voltage. This infers a reasonable approximate assumption: if the drain-gate voltage is increased, then hole emission (electron capture) is the dominant process in the surface states, and the trap condition should reach steady-state quickly. However, for increasing gate voltage, the dominant process is hole capture (electron emission), which has a considerably slower transient (Meneghesso shows plots where this transient takes 10

μs to 1 s depending on the location of the trap states with respect to the valence band) [39]. The two conditions for surface trapping in HEMTs can be formulated as follows:

Case 1: $V_{dgp} < V_{dgQ}$. Holes begin to be captured (or electrons begin to be emitted) by surface traps on the application of a pulse. The emission time constant is sufficiently longer than the pulse length in short-pulse IV, and the trap state is dependent on V_{dgQ}.

Case 2: $V_{dgp} > V_{dgQ}$. Holes are emitted (or electrons are captured) by surface traps on application of the pulse. The capture time constant can be considered to be shorter than the pulse length and the trap state at the measurement time is dependent on V_{gsp}.

4.2. Trapping Effects and Pulsed IV Measurement

Using the above conclusions concerning the occurrence of trap capture and emission, it is possible to form an idea about how trap effects will impact the pulsed IV results depending upon the quiescent bias condition. Figure 4.3 provides a conceptual summary of the effects that occur when pulsing in different directions in the IV plane. If the pulse-to drain-source voltage is larger than the quiescent drain-source voltage and the pulse-to drain-gate voltage is larger than the quiescent drain-gate voltage, the resultant change in the trap states will be electron emission, a fast process. Thus, the pulsed IV curves are expected to depend on the pulse-to voltages, rather than the quiescent voltages. However, if the drain-gate voltage and the drain voltage are reduced during the pulse, then electron emission is the dominant process. This process is much slower, so the resultant pulsed IV curves in this region will be dependent on the quiescent bias condition. This is the reason for the "current slump" often viewed in the knee region for pulsed IV characteristics of devices with significant surface and/or substrate trapping effects.

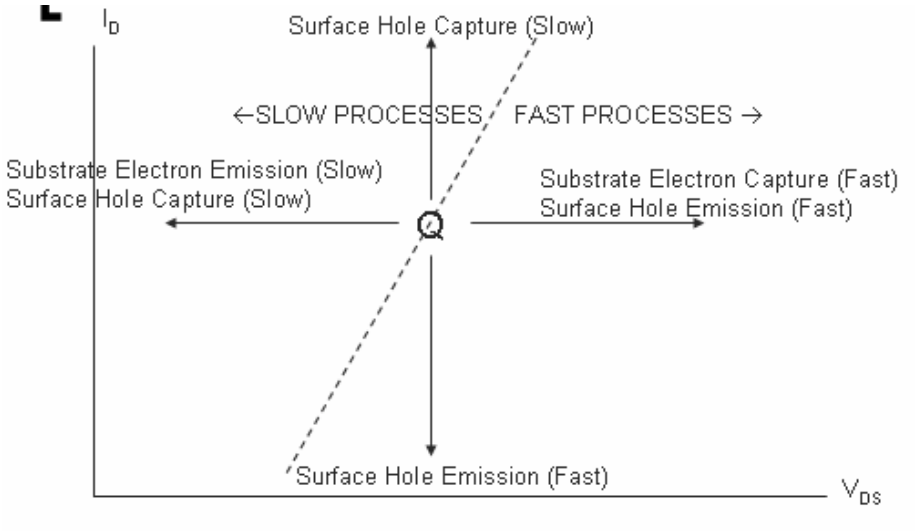


Figure 4.3. Trapping Effects Based on Pulsing from a Quiescent Bias Point "Q"

An analysis of pulsed IV curves taken with different quiescent bias conditions can be used to diagnose the types of trapping effects present in a device. As an example, the trap effects present in a GaN HEMT are diagnosed here. Figure 4.4 shows the static and pulsed IV characteristics for the GaN HEMT. Figure 4.5 shows two sets of pulsed IV characteristics from quiescent bias voltages differing only in the gate voltage (both have zero drain bias). Because the quiescent V_{DS} = 0 V for both of these bias settings, no quiescent power is dissipated in the channel of the device; therefore, the temperature is equal to that of the surrounding environment. The IV curves differ significantly; appearing to be offset by a multiplicative constant over the entire IV plane. The difference in the gate voltage causes electron emission to be the dominant effect in the measurement of the darker curves, because an increase in gate bias voltage occurs during the measurement (from -5 V to the measurement gate voltage). This process is slow and the most of the electrons are still in the trap states when the measurement is performed. Thus, the current is lower because there are not as many carriers contributing to current flow; the carriers remain trapped. However, for measurement of the darker curves, a decrease in gate bias occurred for each measurement; thus, the dominant effect is of the electron capture type, a relatively fast effect that has mostly reached steady-state at the measurement voltage setting by the time the measurement is taken. When the measurement is made, the electrons have been successfully released from the traps and contribute to the current, allowing the current to be larger.

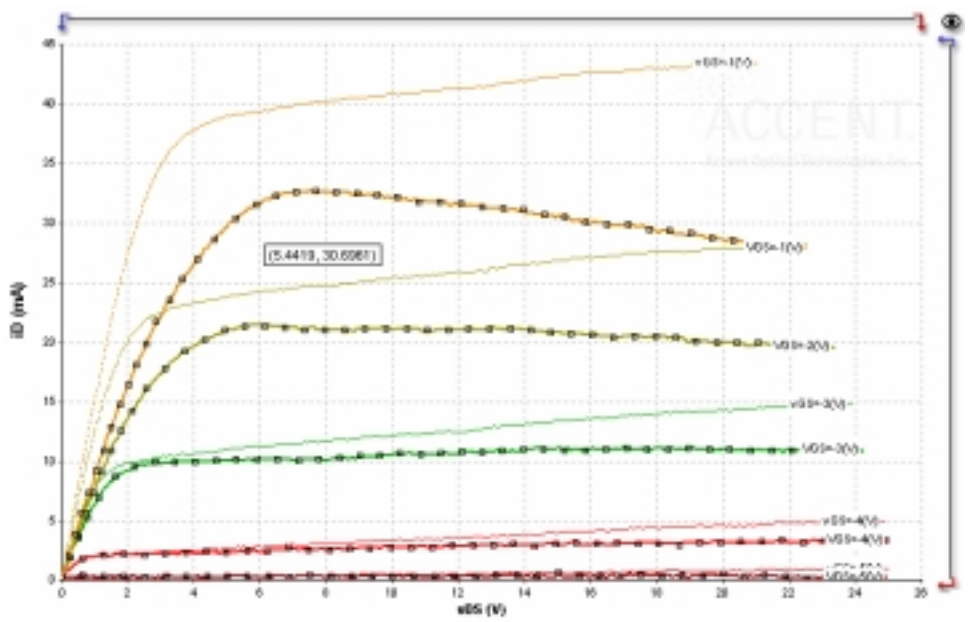


Figure 4.4. Static (Darker Curves) and Pulsed (V_{GSQ} = 0 V, V_{DSQ} = 0 V) (Lighter Curves) IV Curves for the GaN HEMT

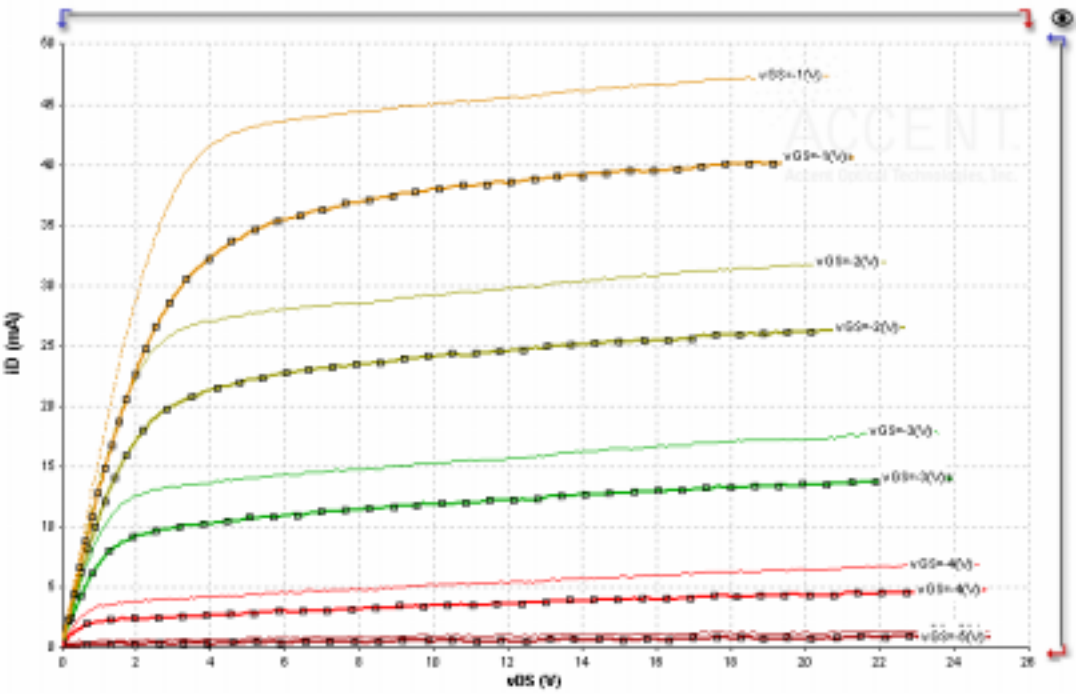


Figure 4.5. Pulsed IV from Quiescent Bias Points V_{GS} = - 5 V, V_{DS} = 0 V (Dark Curves with Dots) and V_{GS} = 0 V, V_{DS} = 0 V (Light Curves without Dots)

Figure 4.6 shows pulsed IV curves taken from the same quiescent gate voltage (at threshold), but differing drain voltages (0 V and 5 V). For drain voltages between the two quiescent drain voltages (between 0 V and 5 V), the IV curves are significantly different. This is because the trap state occupancy is not the same between the cases. However, as the measurement drain voltage increases significantly larger than both quiescent bias drain voltages, the IV curves sets converge. This is due to the fact that the electron capture effect will be approximately the same due in both cases due to the large drain voltage increase. Thus, for the measurement, the trap occupancy is approximately the same in both cases for very large drain voltage. As in the previous case, the device channel temperature is expected to be the same for both IV measurements, as a quiescent bias point of zero power dissipation was used in both cases.

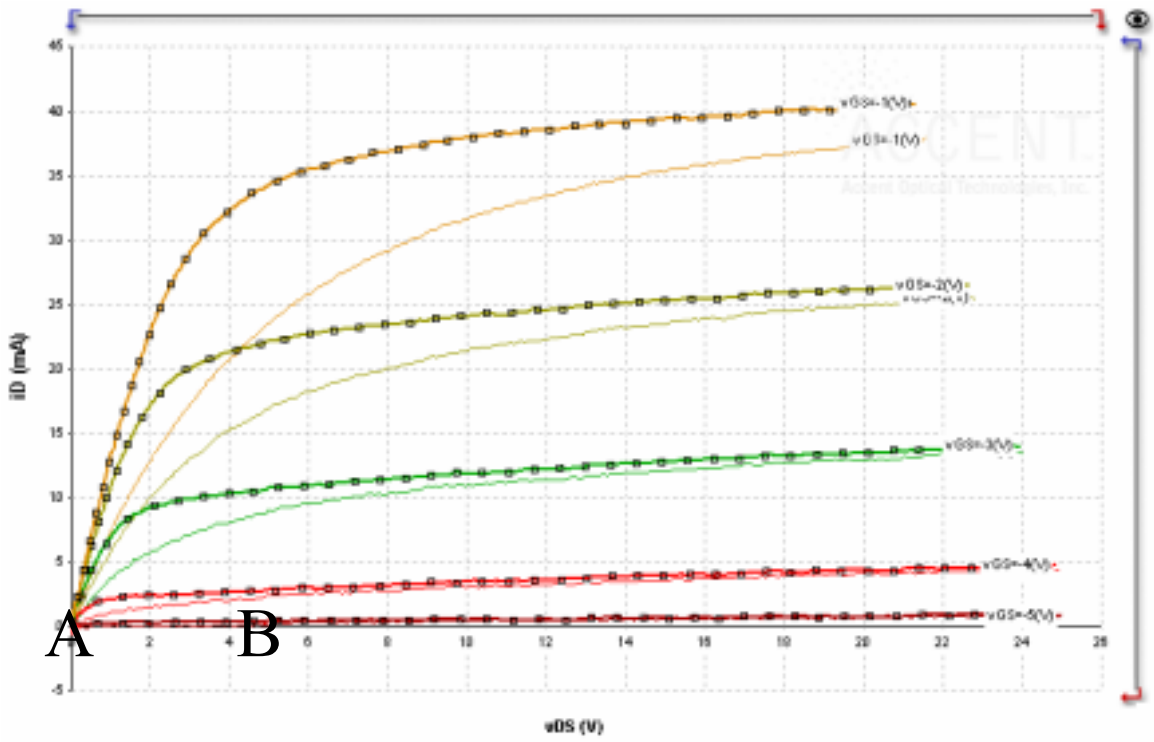


Figure 4.6. Pulsed IV from Quiescent Bias Points (A) V_{GS} = -5 V, V_{DS} = 0 V (Dark Curves with Dots) and (B) V_{GS} = -5 V, V_{DS} = 5 (Light Curves without Dots)

Because both significant drain and gate quiescent bias dependence has been observed for this device, it is concluded that the device possesses both substrate and surface trapping effects. In general, if a device shows a quiescent drain voltage dependence, it is likely to possess significant substrate trapping effects, whereas if a device shows a quiescent gate voltage dependence, it is likely to possess significant surface trapping effects.

4.3. Chapter Summary

The current in a FET is dependent upon the interaction of electrons with trap states on the surface of the device and in the substrate. The occupancy of trap states on the surface of the device depends predominantly on the drain-gate voltage, while the trap occupancy for states in the substrate depends predominantly on the drain-source voltage. When the drain-source voltage or the drain-gate voltage is stepped upward, more current flows and electrons are captured by trap states, reducing the current. The capture process is a fast process and can usually come near completion before data is taken in a pulsed IV measurement. When the drain-source or drain-gate voltage is stepped downward, electrons begin to be emitted as the states begin to adjust to the new bias setting. However, the emission process usually requires an amount of time that is much longer than the capture process, and the emission process usually has barely begun before the data is taken in a pulsed IV measurement. Thus, in a situation where capture is occurring, the results are dependent on the "pulse-to" voltage, whereas results are dependent on the quiescent voltage in a situation where emission is occurring. Strategic use of pulsed IV measurements can determine if substrate and surface trapping effects are present in a device.

CHAPTER 5: BIAS TEE DESIGN FOR PULSED-BIAS MEASUREMENTS

To perform pulsed-bias, pulsed-RF measurements, the bias network must be designed to allow a pulsed bias waveform to pass to the device undistorted. In the design described here, the cutoff frequency of the DC path was raised to allow pulsing of the bias signal. The theory of bias tee design for pulsed measurements is first presented. The simulation results from the design without the use of component parasitic models are presented, followed by simulation results obtained using improved component models for the inductor and capacitor. Agilent ADS was used for the simulations. The simulation results are then compared with S-parameter measurement results obtained using a TRL calibration and found to obtain good agreement. Finally, illustrations of the accurate use of the bias tees in performing both pulsed IV and pulsed S-parameter measurements are provided.

5.1. Design Approach

A typical bias tee circuit consists of an inductor and a capacitor, as shown in Figure 5.1. The function of the bias tee is to simultaneously allow a DC bias voltage and an AC test signal to be applied to the port of a transistor during measurement. For example, in an S-parameter measurement system, the DC bias is applied at the port labeled "DC", and the RF test signal from the vector network analyzer is applied to the port labeled "AC." At the AC + DC port, the AC and DC voltages are both applied to the port. The purpose of the inductor is to prevent the RF signal from entering the DC path, and the purpose of the capacitor is to keep the DC signal from entering the AC path.

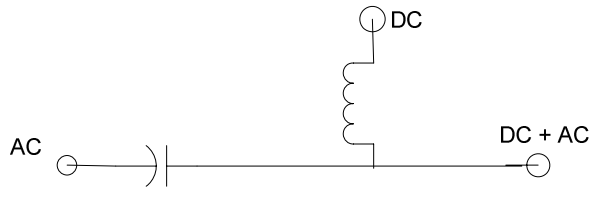


Figure 5.1. Bias Tee Circuit

The inductor and capacitor should be designed such that the upper cutoff frequency of the low-pass DC path is lower than the lower cutoff frequency of the high-pass AC path. If this is true, then the lower cutoff frequency of the AC path containing the capacitor (considering the inductor to be an open circuit) is given by

$$f_{c,AC} = \frac{1}{2\pi RC}, \qquad (5.1)$$

where R is the total resistance seen by the capacitor terminals. In this case, if the termination at the AC port is 50 ohms and the termination of the DC + AC port is large (either the input or output impedance of the device) in operation but will be 50 ohms in the test setup of the bias tee. In operation, however, the value of the input resistance will be fairly large, changing the cutoff frequency. However, in a 50-ohm test system, 50 ohms is the impedance at all test ports. This setup will be used for the purpose of benchmarking the behavior of the device through measurement and simulation. Thus R = 50 + 50 = 100 Ω for this case.

The cutoff frequency of the DC path, assuming that the capacitor appears an open circuit, is given by

$$f_{c,DC} = \frac{R}{2\pi L}. \qquad (5.2)$$

In this case, R is equal to the series combination of the impedance presented by the bias equipment and the input impedance to the device under test. For a 50-ohm test system, R = 50 + 50 = 100 Ω.

The design factor that is outstanding for pulsed bias tee design is that the cutoff frequency of the DC path must be high enough to allow the pulsed bias signal to proceed unabated from the DC to the DC + RF port. Based on available instrumentation,, the smallest pulse length to be used for pulsing the bias is approximately 100 ns. The frequency content of this pulse is a (sin x)/x function centered at a frequency of $1/(100 \times 10^{-9}) = 10$ MHz. Thus the upper cutoff frequency of the bias network should be greater than 10 MHz, large enough that the entire frequency content of the pulse can pass through the DC path without distortion; this will allow the integrity of the pulse shape to be maintained.

Initial values for the inductor and capacitor were chosen and simulations containing ideal elements were performed to ensure the selection of component values to provide adequate cutoff frequencies for the DC and AC paths. The simulation circuit and results for ideal component values of C = 100 pF and L = 27 nH are shown in Figures 5.2 and 5.3, respectively. For these component values, the 3 dB cutoff frequency of the AC path is shown to be 151 MHz and the cutoff frequency of the DC path is shown to be 61 MHz.

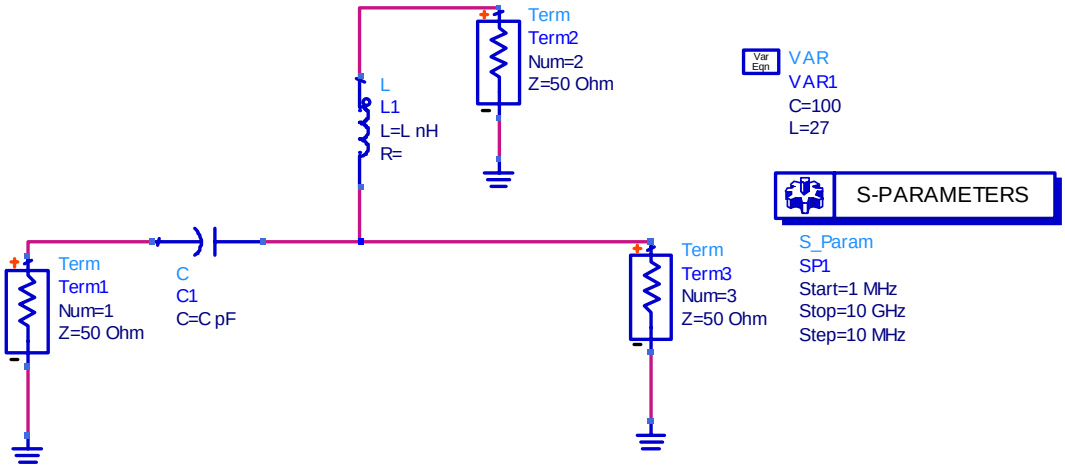
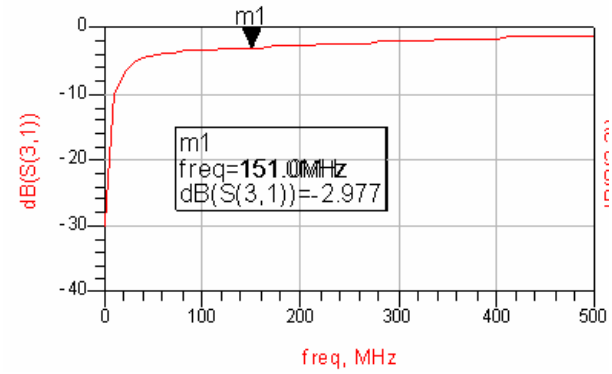
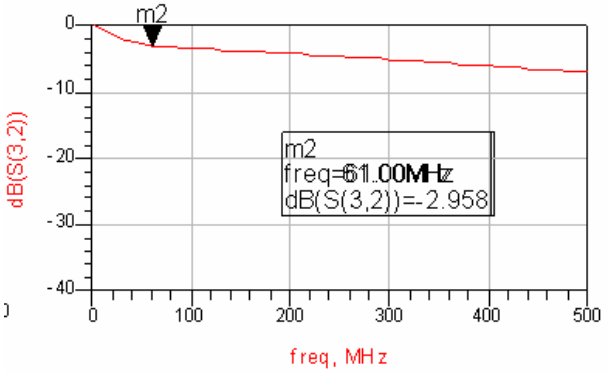


Figure 5.2. Simulation Circuit with Ideal Components and No Microstrip Lines



(a)



(b)

Figure 5.3. S-Parameter Simulation Results for Ideal (Figure 5.2) Circuit for (a) AC to DC+AC Transmission and (b) DC to DC + AC Transmission

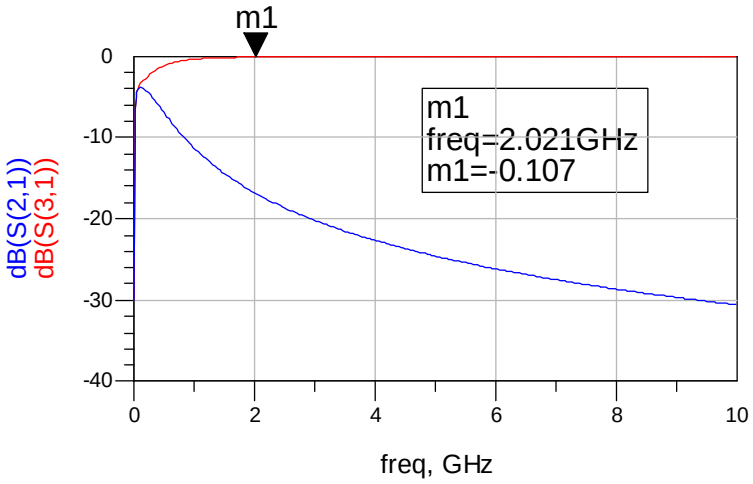
5.2. Simulation Results

Simulations were performed for the selected component values L = 27 nH and C = 100 pF. The simulation was performed at three different levels. At each level, both S-parameter and transient simulations were run. The purpose of the S-parameter simulations is to ensure that the RF path of the bias tee passes the signal while the DC path does not at RF frequencies. The transient simulations are used to show that the pulse can accurately reach the RF + DC port without being significantly distorted in the time domain.

Three levels of simulation were incorporated into this effort: (1) ideal components and no transmission lines, (2) ideal components with microstrip (FR-4 specifications) transmission lines, and (3) components with models supplied by Modelithics, Inc. with microstrip transmission lines. The first level was used to assess the optimum inductance and capacitance values, as shown in the previous section; the second and third levels are used to view non-idealities introduced by the substrate (second level) and component parasitics (third level).

For the first-level schematic shown in Figure 5.2, simulation results are displayed in Figures 5.4 and 5.5. Figure 5.4 shows that the S-parameter results are as desired. For about 500 MHz and above, S_{31} is high (this means that most of the signal is getting to the RF + DC output) and S_{21} is low (very little signal is going from the RF port to the DC port). Also, S_{11} is below about -20 dB for all frequencies greater than about 1.7 GHz. These results show that the choice of component values seems reasonable for a large RF passband.

The transient simulation reveals whether the bias tee will allow accurate transmission of pulses from the DC port to the RF +DC port. The results of Figure 5.5 show that a 1 μs square pulse sent from the DC port (left plot) appears virtually undistorted at the DC + RF port, and an 0.1 μs also goes through the system with only minimal overshoot at the rising and falling edges of the pulse (right plot). Since 0.1 μs is short enough for isodynamic measurements, it appears this bias tee is designed correctly with regard to the DC path passband.



(a)

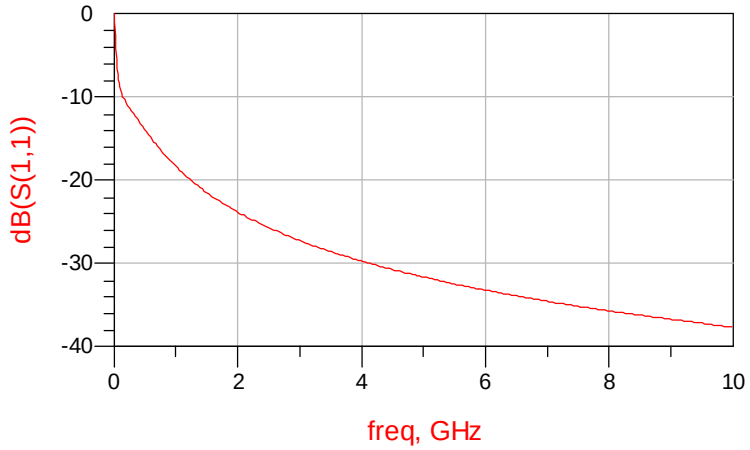
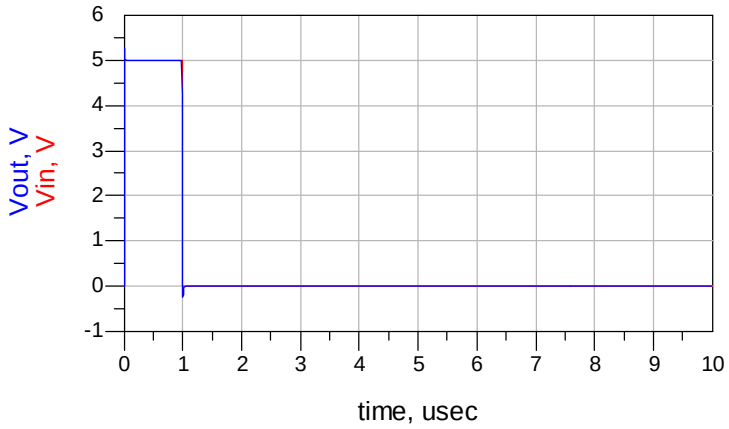
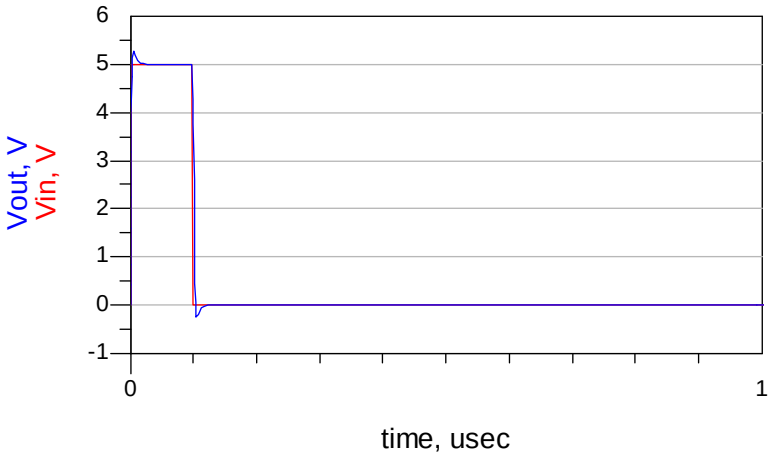


Figure 5.4. S-Parameter Simulation Results for Ideal (Figure 5.2) Circuit



(a)



(b)

Figure 5.5. Transient Simulation Results for DC to RF+DC Ports: (a) 1 µs Pulse, (b) 0.1 µs Pulse

The next step was the incorporation of microstrip lines into the simulation (ideal components, however, were still used for the inductor and capacitor), as in the schematic shown in Figure 5.6. The substrate parameters used in the "MSUB" element are those for the FR-4 substrate to be used in milling the circuit.

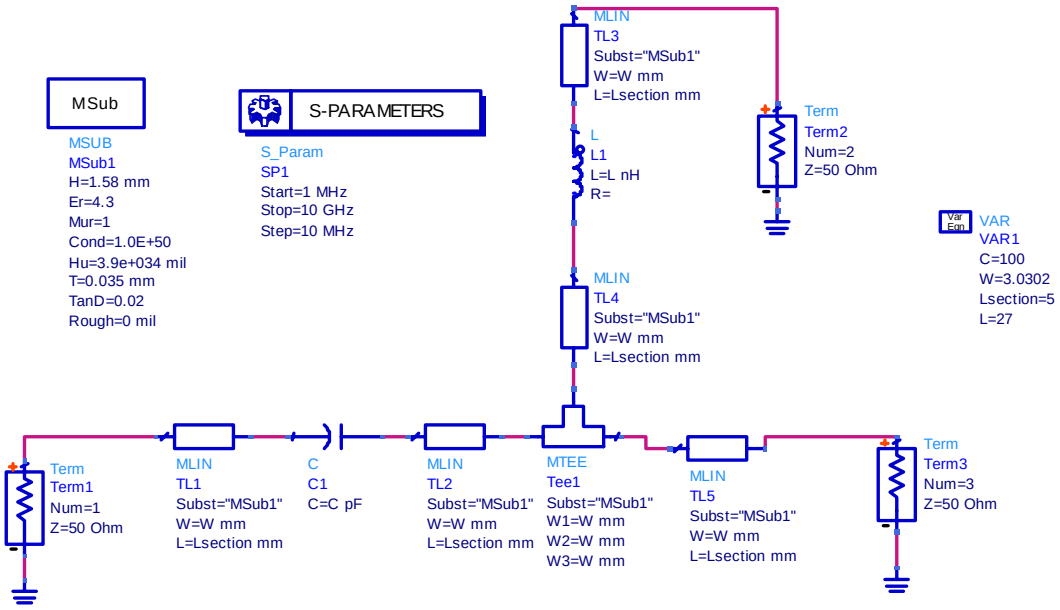


Figure 5.6. Simulation Circuit with Microstrip Lines and Ideal Components

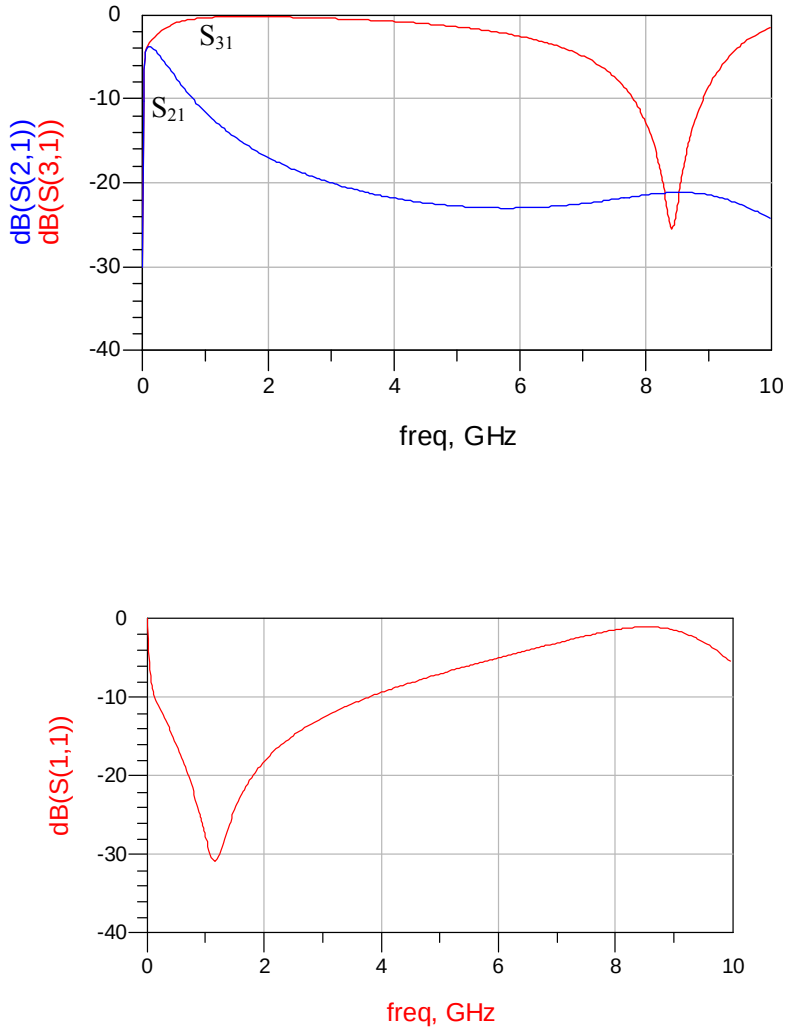
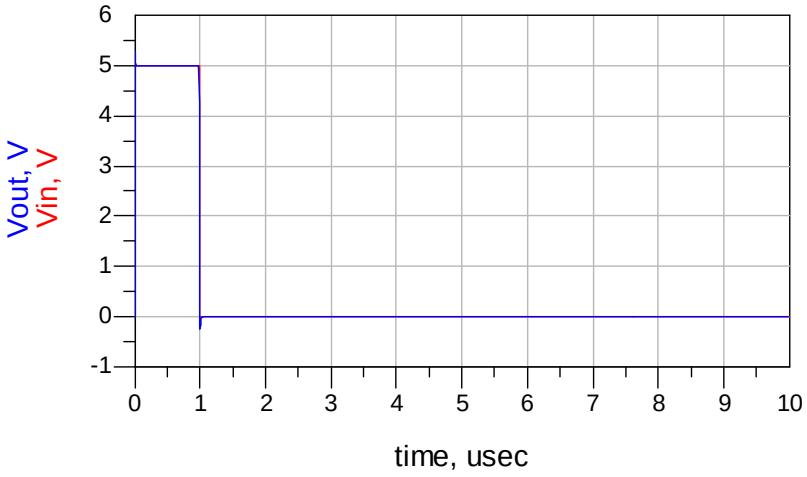
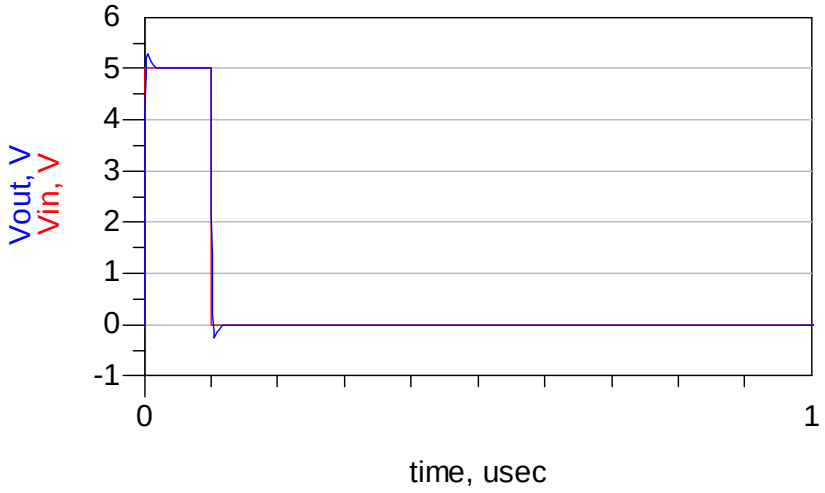


Figure 5.7. S-Parameter Simulation Results for Figure 5.6 Circuit

Figure 5.7 shows the S-parameter simulation results for the microstrip circuit. While behavior is still close to ideal up to about 5 GHz, there is a steep drop in S_{31} at about 8 GHz. In addition, the input match becomes worse as frequency raises, reaching a peak at the same location as the notch in S_{31}. However, these simulations indicate that the bias tee should be useful in applications up to 6 GHz. The transient simulations are shown in Figure 5.8. Excellent pulse integrity is obtained at the RF + DC port.



(a)



(b)

Figure 5.8. Transient Simulation Results: DC to RF+DC Ports for Microstrip Circuit: (a) 1 µs Pulse, (b) 0.1 µs Pulse

Finally, the simulations were performed using passive element models for the components to be used in the circuit: a TDK 27 nH size 0603 inductor and an ATC 100 pF size 0603 capacitor. The models include the bond pads, so these were not included in the microstrip components. However, it is necessary to include these bond pads in the schematic for the layout generation.

Figure 5.9 shows the schematic used for the simulation. Figure 5.10 displays the S-parameter simulation results.

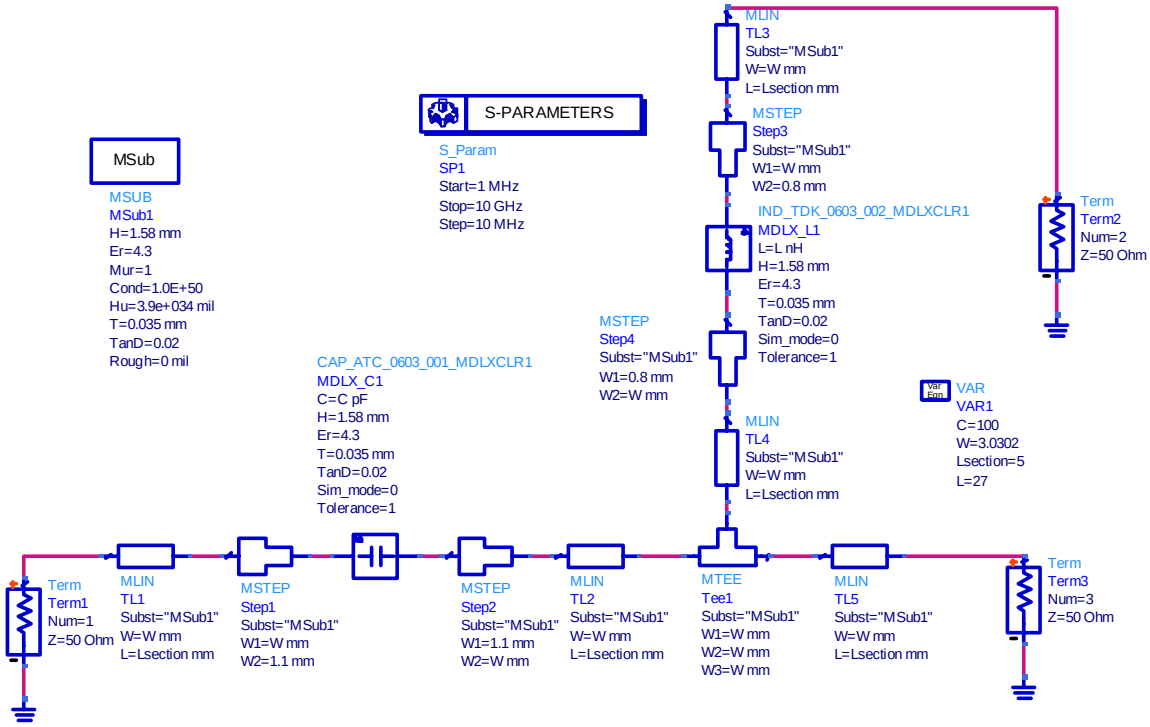


Figure 5.9. Schematic for Simulation with Passive Component Models and Microstrip Lines

The plots of Figure 5.10 show that the response concerning the RF to DC port and RF to RF+DC port transmission is now only desirable at frequencies below 4 GHz. However, at 4.5 GHz, more transmission is occurring from the RF port to the DC port than from the RF port to the RF + DC port. In addition, the input match at this frequency is relatively poor, as evidenced in the S_{11} plot of Figure 5.8. These non-ideal effects are evidently due to the component parasitics, as the microstip line elements added in the second stage did not cause such effects at these

frequencies. These effects will limit the frequency range for which the bias tee will be able to be accurately used in S-parameter measurements.

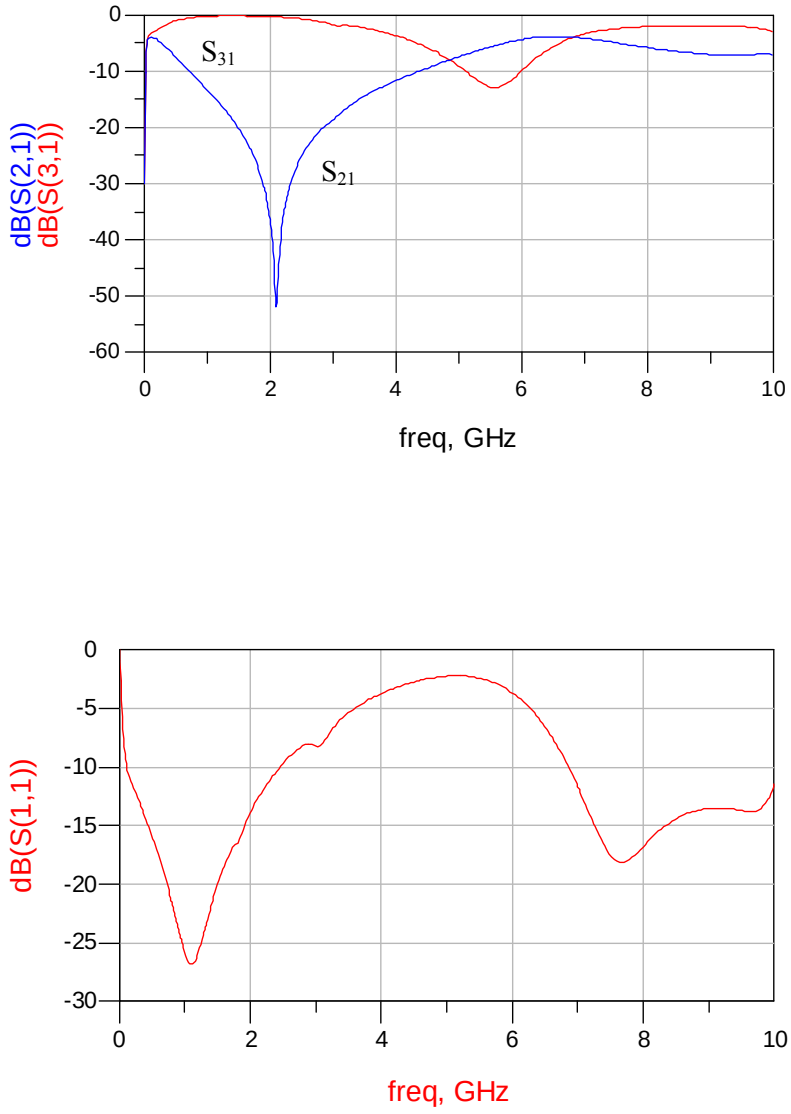
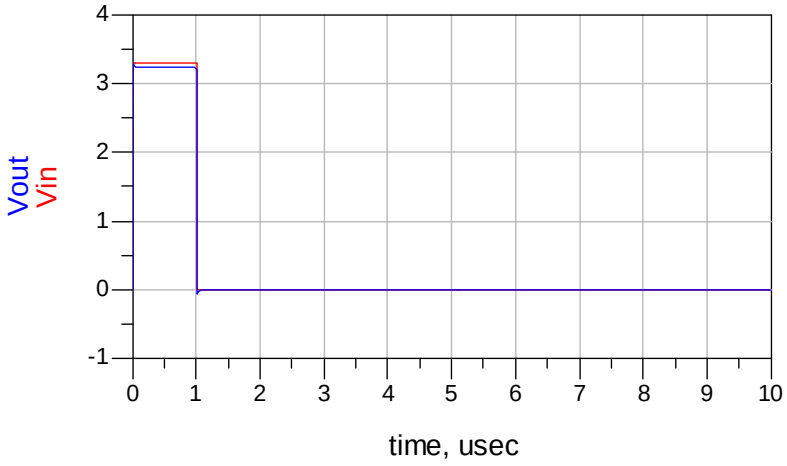


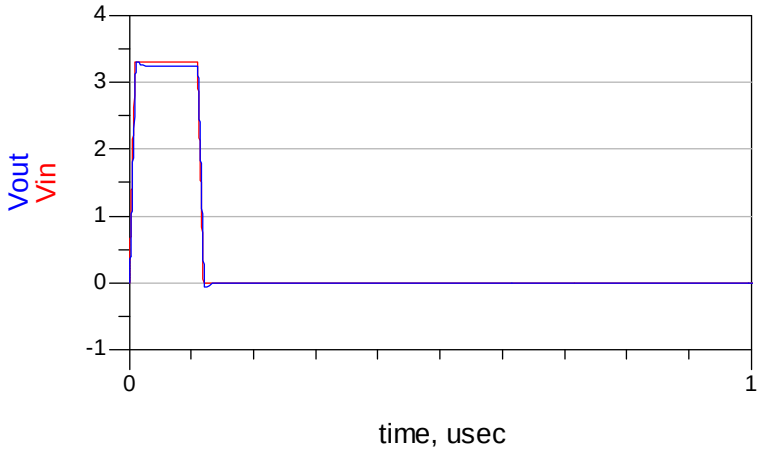
Figure 5.10. S-Parameter Simulation Results for Figure 5.9 Circuit

Figure 5.11 shows the transient simulation results for the bias tee. It appears that the height of the pulse at the RF+DC port is slightly lower than at the input. This is likely due to the

non-ideal resistance of the components that is included in the models but is not taken into account in the ideal component definitions used for the simulations whose results are previously displayed.



(a)



(b)

Figure 5.11. Transient Simulation Voltage (V) Versus Time (µs): DC to RF+DC Ports for Circuit Containing Microstrip Elements and Passive Component Models: (a) 1 µs Pulse, (b) 0.1 µs Pulse

The use of three levels of simulation has shown that both the transmission line elements and the parasitic effects of the components have a substantial impact on S-parameter simulation results. With the addition of the transmission line elements and component models, it was seen that some non-ideal effects are expected to occur above 4 GHz.

5.3. Layout and Fabrication

The bias tees were constructed by mounting the components on a 59-mil FR4 substrate. The circuit board was fabricated in the University of South Florida Wireless and Microwave Instructional (WAMI) Laboratory. The layout generated by ADS for milling is shown in Figure 5.12. After milling, the components and SMA-to-59 mil circuit board adapters were soldered onto the board.

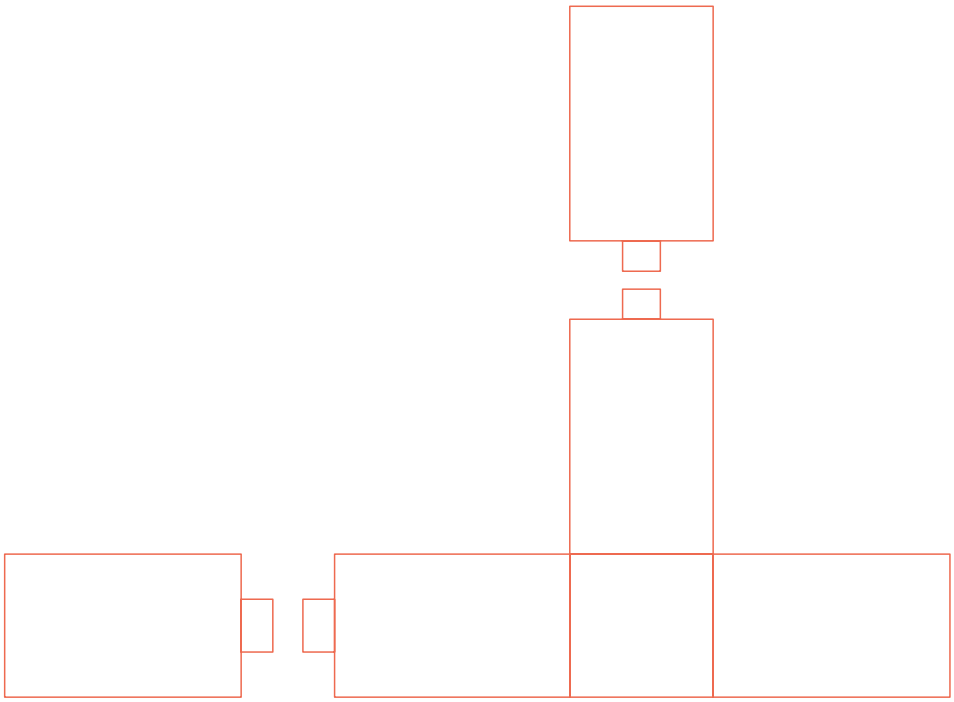


Figure 5.12. Bias Tee Layout for FR4 Milling

5.4. S-Parameter Measurements of Bias Tees

To test the prediction of bias-tee behavior, S-parameter measurements were performed for a frequency range of 40 MHz to 6 GHz using an Anritsu 37397C "Lightning" Vector Network Analyzer. A thru-reflect-line (TRL) calibration was used for the measurement. The 59-mil FR4

standards used for this calibration have coaxial to microstrip adapters on each port. The length of the standards was measured in the USF laboratory. The thru standard was measured to be 10.00 mm, while the delay standard was measured as 18.64 mm. The open was offset by half of the thru standard line length. The calibration was performed using the Multical Software created by the National Institute of Standards and Technology (NIST) [40]. A reference impedance of 50 ohms and an effective relative permittivity of 3.3 were used. The reference plane was set to be 5 mm from the center of the thru, placing it at the beginning of the microstrip line, just on the microstrip side of the coaxial-to-microstrip adapter at each port.

Figure 5.13 shows plots of S_{31}, the RF to RF+DC transmission, in dB magnitude and phase. The measured results seem to indicate accuracy of the component models used for the simulation. The largest difference between the results in both magnitude and phase between 5 and 6 GHz.

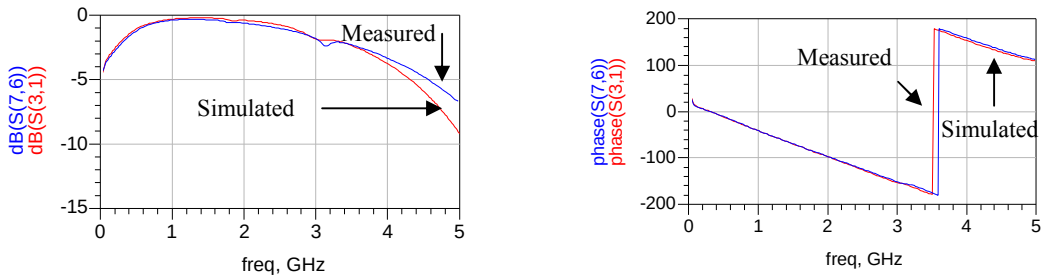


Figure 5.13. S_{31} (RF to DC+RF Transmission) Measured and Simulated dB Magnitude (Left) and Phase (Right)

The measured versus simulated (without microstrip-to-coaxial adapters) results for S_{21} (the RF to DC) transmission are shown in Figure 5.14. It is desired that this magnitude be low at all frequencies. A very good agreement is obtained between the measured and simulated data in both magnitude and phase. Measured and simulated results for S_{32} (DC to DC + RF transmission) are shown in Figure 5.15. The magnitude of this transmission is expected to be low except at low frequencies. The magnitude match is excellent between measured and simulated results over the entire measurement band for both S_{21} and S_{32}.

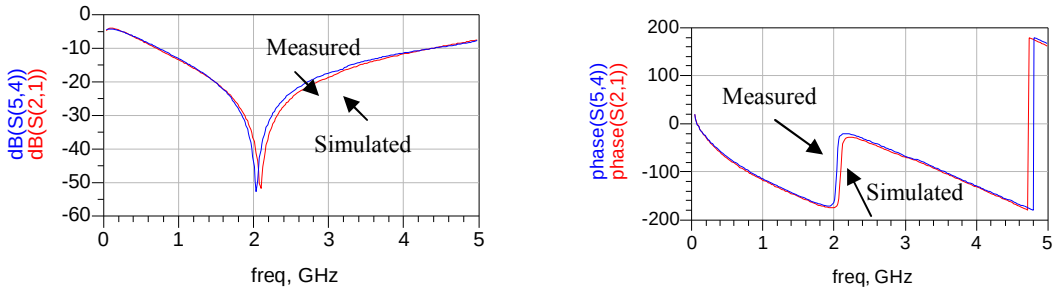


Figure 5.14. S_{21} (RF to DC Transmission) Measured and Simulated dB Magnitude (Left) and Phase (Right)

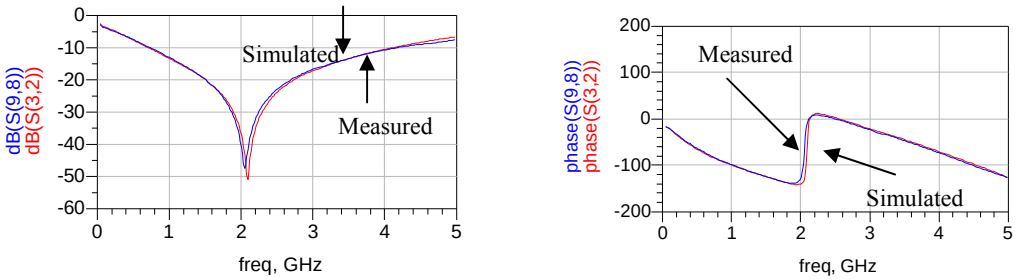


Figure 5.15. S_{32} (DC to DC+RF Transmission) Measured and Simulated dB Magnitude (Left) and Phase (Right)

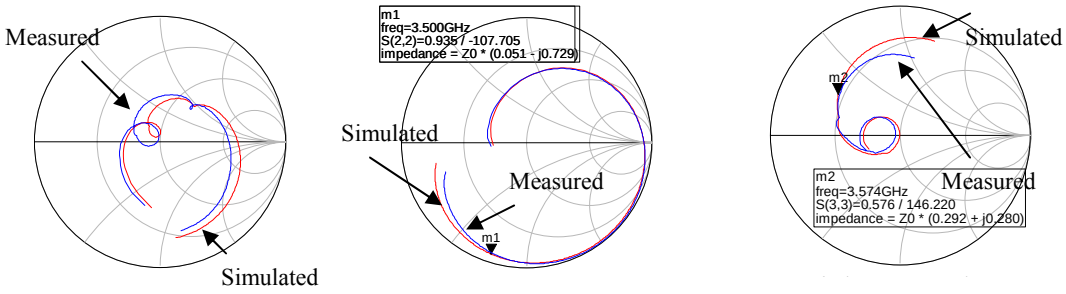
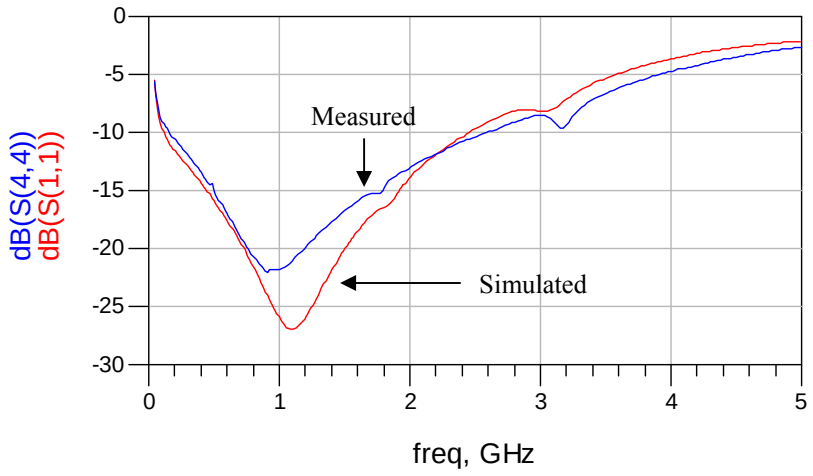


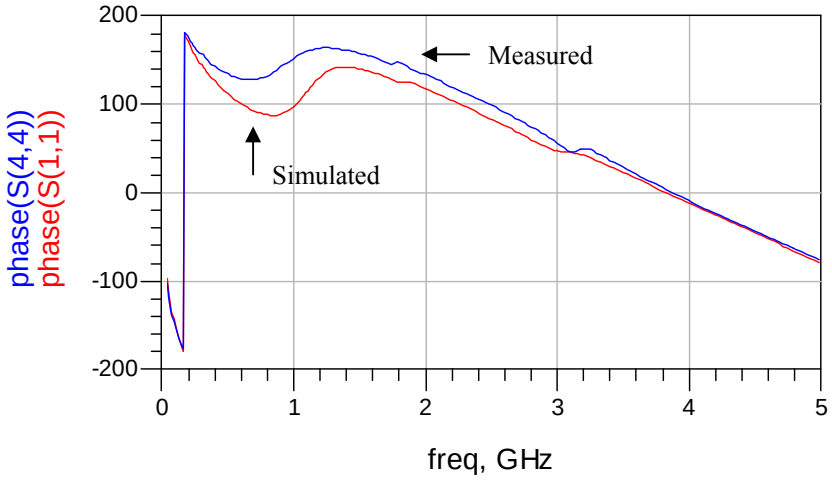
Figure 5.16. Simulated and Measured Results for S_{11} (Left), S_{22} (Center), and S_{33} (Right)

Figure 5.16 shows the input reflection coefficient measured and simulated results for all three ports. The simulation and measured reflection parameters match well at lower frequencies; however, some differences exist at higher frequencies. The simulated parameters have larger

magnitude in each case at the higher frequencies, especially S_{33}. This may be due to the difficulty of obtaining a good reflection calibration using 59 mil FR4 substrate with SMA-to-microstrip adapters at higher frequencies. Figures 5.17, 5.18, and 5.19 display the reflection parameters as magnitude and phase versus frequency.

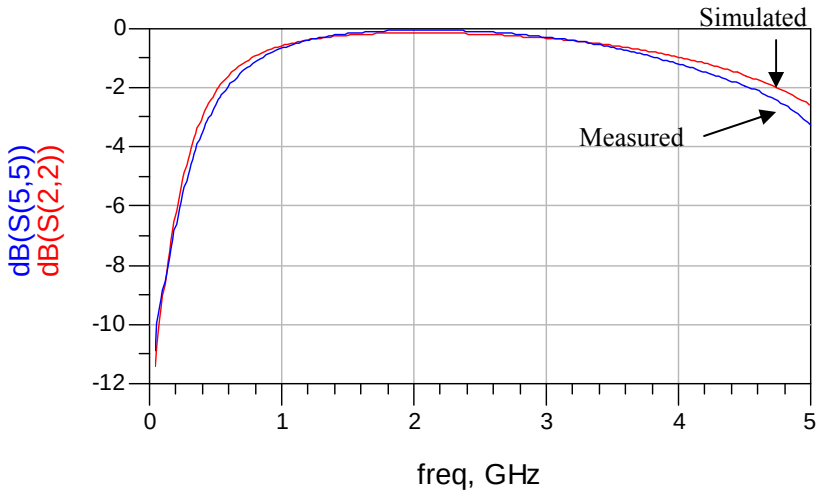


(a)

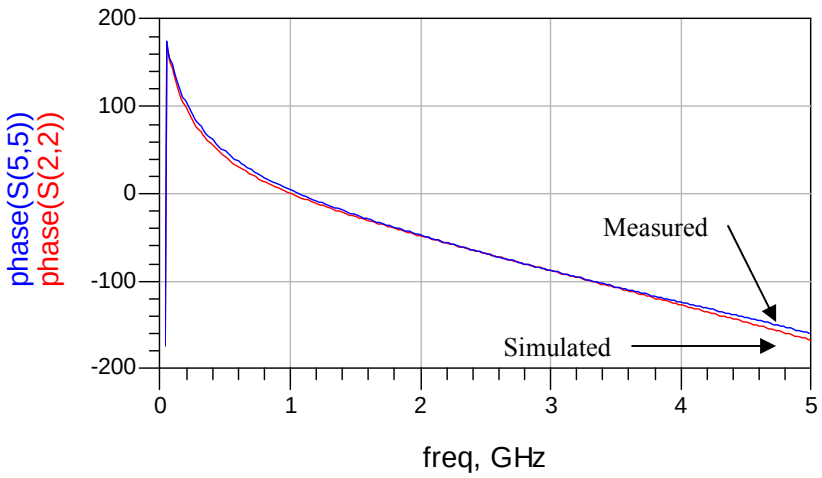


(b)

Figure 5.17. S_{11} Measured and Simulated (a) dB Magnitude and (b) Phase

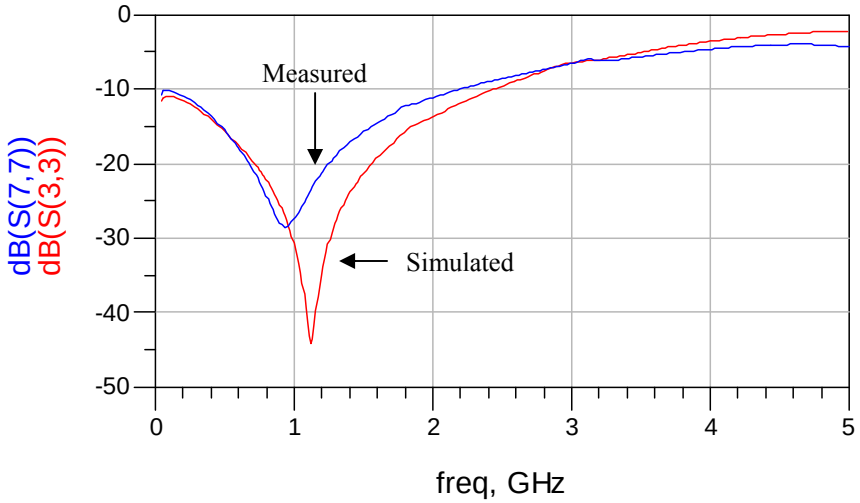


(a)

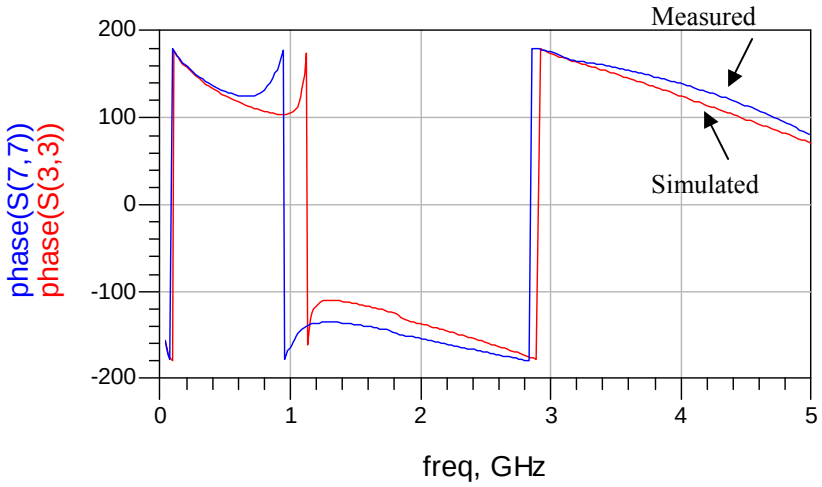


(b)

Figure 5.18. S_{22} Measured and Simulated (a) dB Magnitude and (b) Phase



(a)



(b)

Figure 5.19. S_{33} Measured and Simulated (a) dB Magnitude and (b) Phase

In general, the S-parameter results show good correspondence from 40 MHz to 5 GHz. This data seems to indicate that the models have accurately predicted the performance of the design on the first pass.

5.5. Pulsed IV Measurements Through Bias Tees

In addition to testing the RF performance of the bias tee, it is also important to ensure that the circuit allows a pulsed bias to be correctly applied to a device under test, as previously mentioned. A good method of test for this is to attempt to perform pulsed IV measurements through the bias tees as attempted in [41]; if the bias tees do not distort the IV curves, then they are adequate for applying a pulsed bias to an RF measurement system.

In this experiment, pulsed IV measurements with pulse lengths varying from 0.1 μs to 1000 μs were performed on a GaAs MESFET using an Accent Optical Technologies Dynamic i(V) Analyzer (DiVA) model D225. The measurements were performed for three setups: (1) no bias tees, (2) a set of commercially available bias tees, and (3) a set of USF custom bias tees. In the bias tee setups, the DiVA was connected to the DC ports of the bias tees and the RF ports of the bias tees were terminated in 50 Ω loads. The measurement setup is shown in Figure 5.20. For the commercially available bias tees, measurements were performed for pulse lengths varying from 1000 μs to 5 μs. When attempting to measure at 2 μs, the instrument reported that it could not complete the measurement due to the large amount of gate current. This was likely due to the fact that the necessary voltage level could not be reached and the instrument reached its maximum gate port current trying to produce the desired voltage. The results for several selected pulse lengths are shown in Figure 5.21.

Measurements were performed for the custom USF bias tees from 1000 μs to 0.1 μs. From simulation and initial transient measurement results, it was expected that the bias tee would function very well for pulse lengths as low as 0.1 μs. In addition, it is desired to perform pulsed IV within the pulsed S-parameter system, so it is critical that the IV characteristics be accurately measurable through the bias tees.

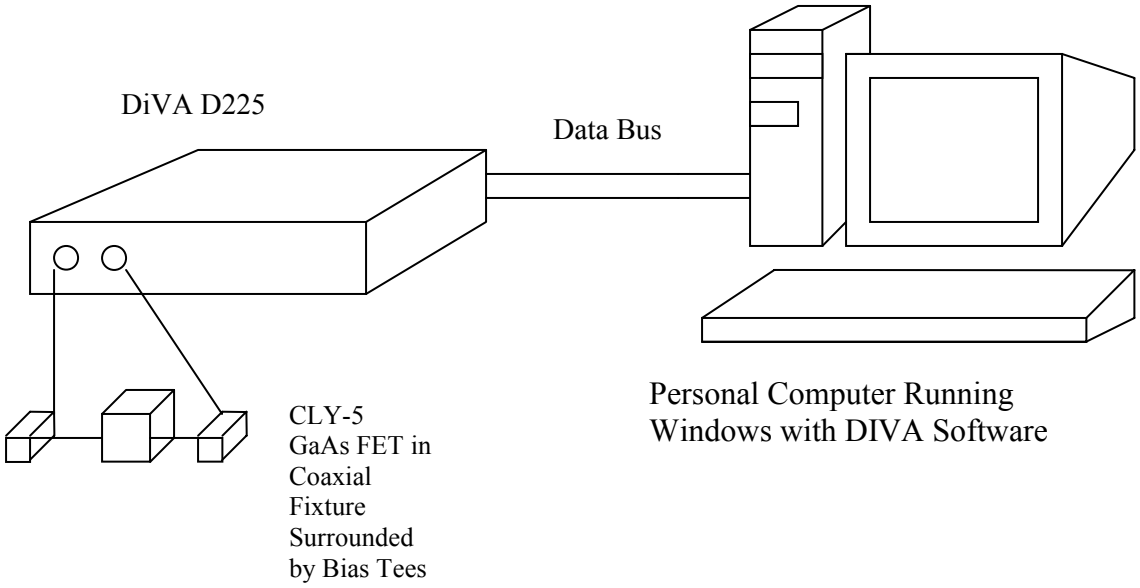


Figure 5.20. Measurement Setup

Figure 5.21 shows pulsed IV curves at different pulse lengths for the commercially available bias tees (left column) and the custom USF bias tees designed by the author (right column). In each plot, the dark set of curves is the measurement without bias tees. At 1000 μs, there is a "jog" in the knee region characteristic of the curves without bias tees. For measurement with the commercial bias tees, this jog is not measured; however, the USF bias tees correctly depict this shift in the curves. The physical phenomenon behind this shift may be due to trapping effects. The commercial bias tees may lengthen the resetting time between pulses, so this effect is likely not due to the pulse length, but the pulse separation, as shown in [42] for this device. If the pulse separation were lengthened, this result is likely to improve. However, even in this situation, it is interesting to note that the custom bias tees more closely represent the measurement environment where no bias tees are used.

The figure also shows that the commercially available bias tees cannot allow accurate pulsed IV measurement for pulse lengths below about 20 μs. Both bias tees allow accurate measurement of the 20 μs curves. At 10 μs, the IV curves measured through the commercial bias tees are much too greatly sloped (g_{ds} is too large), while the custom bias tees allow accurate measurement of the curves. For a pulse length of 5 μs, the commercial bias tees are very clearly in error. The 0.1 μs pulse length measurement through the custom bias tees is compared to a 0.1 μs pulse length measurement without bias tees in Figure 5.22.

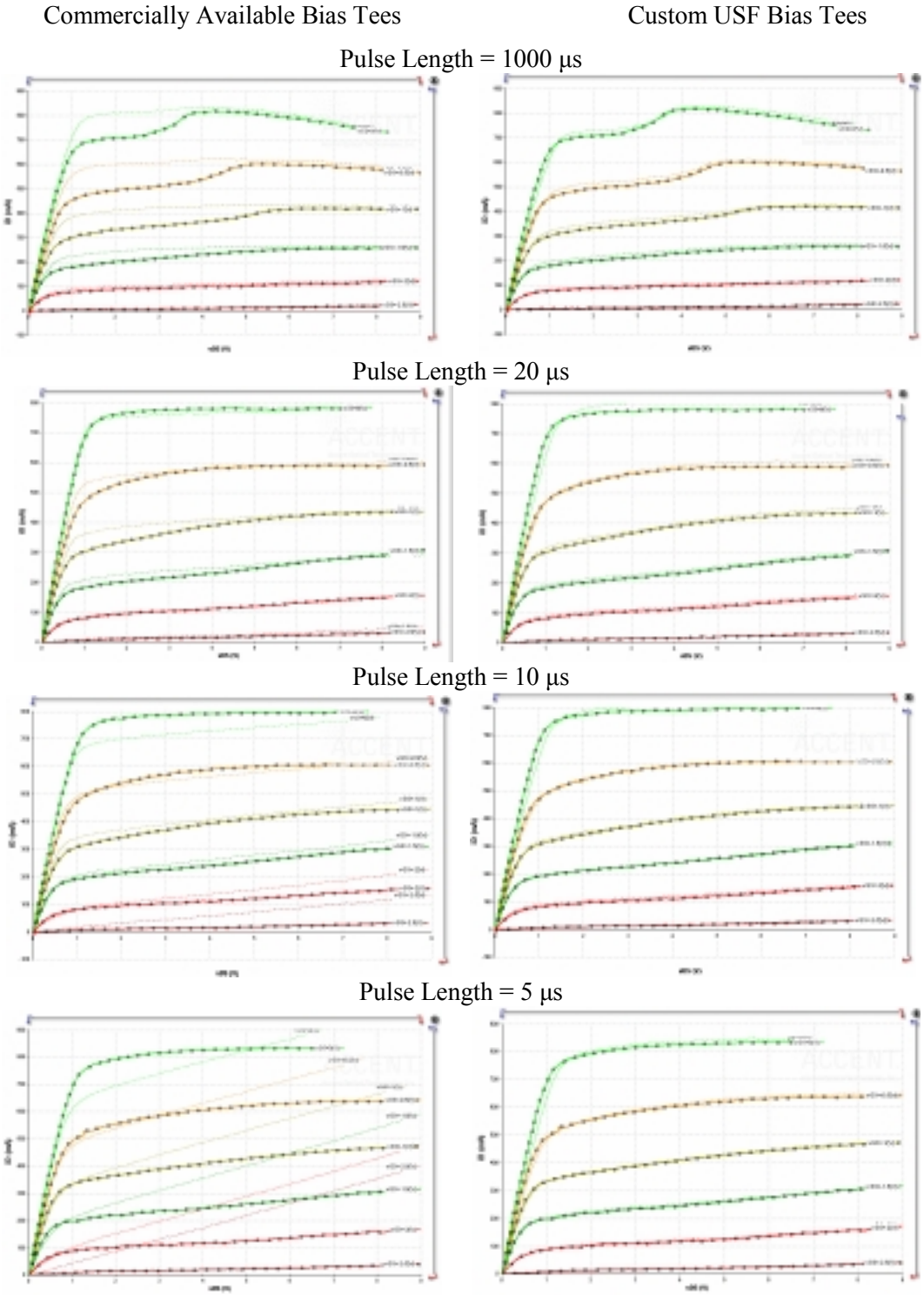


Figure 5.21. Pulsed IV Results for No Bias Tees (Dark Curves, Left and Right), Commercially Available Bias Tees (Light Curves, Left), and Custom USF Bias Tees (Light Curves, Right) at Different Pulse Lengths

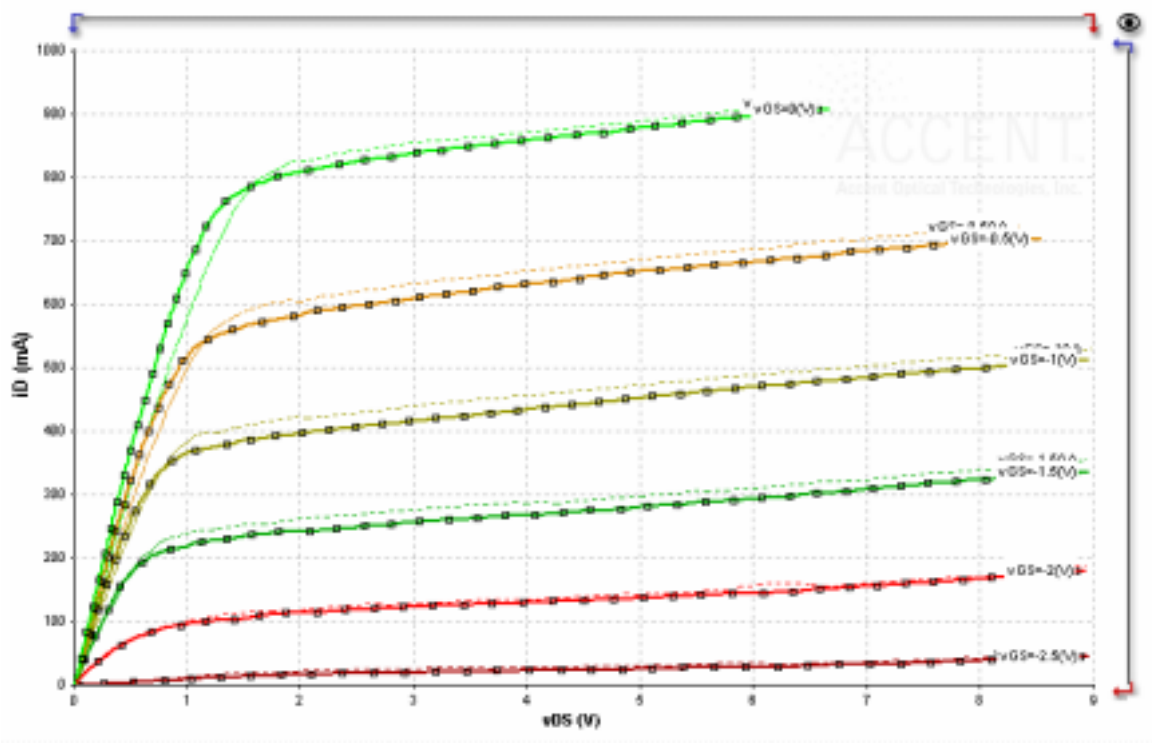


Figure 5.22. Pulsed IV Measurement with Pulse Length = 0.1 µs without Bias Tees (Darker Curves) and with USF Custom Bias Tees (Lighter Curves)

In the custom bias tee measurements, the knee appears to occur at a slightly larger value of V_{DS} than for the measurements without bias tees. This is likely due to the fact that the bias tees themselves add resistance to the drain side of the device, causing a lower voltage to be applied to the device than in the case where no bias tees are used. This DC resistive effect can be easily corrected using a Mathcad sheet if the resistance is measured. In addition, Figure 5.22 shows that the curves measured through the bias tees are slightly higher than the curves measured without bias tees.

5.6. Chapter Summary

A custom bias tee design has been performed with the assistance of accurate passive component models to accommodate pulsed-bias, pulsed-RF S-parameter measurements with pulse lengths on the order of 1 µs and lower. The simulation results for the time and frequency domains have been found to compare remarkably well for the use of the models. An incremental design procedure for this circuit has been demonstrated, followed by the results of performing pulsed IV through the bias tees. The pulsed IV results for the custom bias tees have been shown

to be far more accurate than those performed through commercially available bias tees, which are not normally designed to allow pulses to pass through the bias path. Finally, initial pulsed-bias, pulsed-RF S-parameter measurement results have been shown and found to correlate with expectations.

CHAPTER 6: PULSED S-PARAMETER MEASUREMENTS

In the multiple-bias, small-signal S-parameter measurements commonly used for the extraction of nonlinear models, the quiescent thermal and trap characteristics are dependent on the particular bias point used for each measurement. This means the thermal and trap conditions of each of the multiple-bias S-parameter measurements is different, in general [3], [43]; however pulsed S-parameter measurements with a pulse length on the order of 2 μs have been shown to alleviate this problem [8], [9]. An investigation of the signal issues introduced by performing S-parameter measurements in pulsed RF mode has been presented by Martens and Kapetanic [13].

In this work a pulsed-bias, pulsed-RF S-parameter system has been constructed through a thorough experimental process. The system was constructed using an Anritsu 37397C Lightning Vector Network Analyzer, along with a switch, a digital delay generator, and a custom bias tee. The pulsed-RF test signal spectrum can be represented by a (sin x)/x function, with the spacing of the components inversely proportional to the pulse period and the amplitude of the center component given by the duty cycle. The VNA was configured to operate in a 10 Hz bandwidth to insure measurement of only the central spectral component. It is critical that both calibration and measurement be performed under identical RF conditions. A reduction in dynamic range of

$$DRreduction(dB) = 20\log\left(\frac{period}{pulselength}\right) \tag{6.1}$$

occurs for measurements made in pulsed mode [13]. In addition, it was observed that precision decreases as the pulse length is decreased and/or the duty cycle is decreased.

Because the S-parameters for passive devices are expected to be identical under pulsed and continuous RF conditions, the system precision was studied by measuring calibration standards, an attenuator, and a 915 MHz bandpass filter under both continuous and pulsed RF conditions. These measurement results are shown in detail and the results are explained. After review of the passive DUT results, a pulse length of 1 μs with a period of 20 μs was chosen for the transistor measurement.

The passive measurements were attempted with the switch in the calibration loop and with the switch in the preamplifier loop of the VNA. It is shown that the precision and accuracy

of the reflection measurements suffers greatly when the switch is placed in the calibration path; however, placing the switch in the preamplifier loop allows reflection results to be obtained that possess the same order of precision as the transmission results.

Pulsed-RF, pulsed-bias S-parameter measurements of a Si LDMOSFET and a Si VDMOSFET performed with a pulse length of 1 μs and period of 20 μs are presented and compared to conventional continuous-RF measurements of the same device. The thermal correction of S-parameters, based on work presented in the literature, is performed for the VDMOSFET. Based on these results, an algorithm allowing adjustment of the ambient temperature to compensate for self-heating (rather than taking pulsed S-parameters) is presented.

6.1. Description of Pulsed RF Signal

In a pulsed-bias S-parameter system, it is necessary that the S-parameter measurements pertain to only the time when the quiescent bias is in the "pulse-to" position. Through experimentation, it was found that pulse lengths of less than 400 μs were difficult to achieve by placing the VNA in triggered mode. Thus a continuous RF measurement was made. However, the fact that the RF is turned "on" at the same time as the bias pulse is "on" allows the RF measurement to be made only under the proper bias conditions while continuously operating. Mathematically, the RF switch multiplies the sinusoidal signal at its input by a periodic pulse train with height 1. When the switch is on, the RF signal passes; when the switch is off, nothing passes.

Consider the spectrum of a periodic pulse train with pulse length τ and period T. The time-domain representation of the pulse train is displayed in Figure 6.1. The amplitude of the pulse is taken to be 1 for simplicity. The Fourier transform for this train can be easily derived from the Fourier series, which can be found using methods delineated in [44]. The frequency-domain representation of this pulse train is a series of impulses configured in a (sin x)/x arrangement around the origin, as shown in Figure 6.2. The frequency components are spaced by $2\pi/T$. The strength of the exponential Fourier series representation of the impulse at DC ($\omega = 0$) is given by Equation (3.65) in Lathi [44]:

$$c_0 = \frac{1}{T}\int_{-T/2}^{T/2} y(t)dt\,. \qquad (6.2)$$

The value of c_0 in this case is given by the area under one period of the pulse train divided by the period:

$$c_0 = \frac{\tau}{T}.$$

Hayt *et al.* state in [45] that the Fourier transform of a given periodic function is given in terms of its Fourier series coefficients as

$$f(t) \Leftrightarrow 2\pi \sum_{n=\infty}^{\infty} c_n \delta(\omega - n\omega_0) \qquad (6.3)$$

If the pulse length τ is increased, the amplitudes of all frequency components are increased. However, if τ is decreased, the amplitude of all frequency components are decreased. Increasing the period T decreases the amplitude of each frequency component, while decreasing T increases the amplitude of all components. Thus, for maximum amplitude, the duty cycle τ/T should be as large as possible. In the case of a continuous DC signal (the limiting case of 100 percent duty cycle), the spectral result is an impulse at ω = 0 with weight 2π.

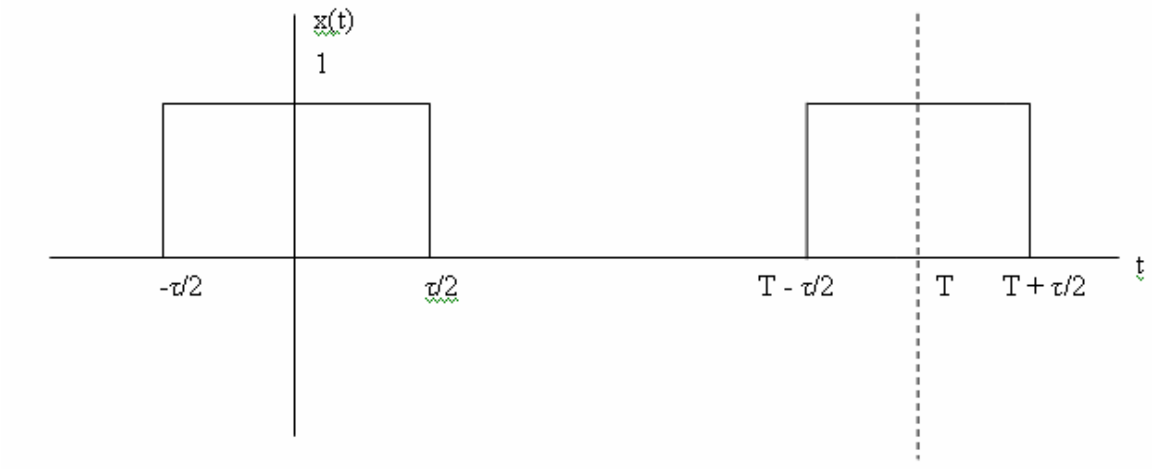


Figure 6.1. Periodic Pulse Train with Period T and Pulse Length τ

Consider now a sinusoidal signal with frequency ω_{RF} such that $\omega_{RF} >> 2\pi/T$ (i.e. many cycles of the RF signal can occur during the "on" time of a rectangular pulse in Figure 6.1). The frequency domain representation of this signal $f(t) = \cos \omega_{RF} t$ is an impulse at ω_{RF} with weight 1, as shown in Figure 6.3.

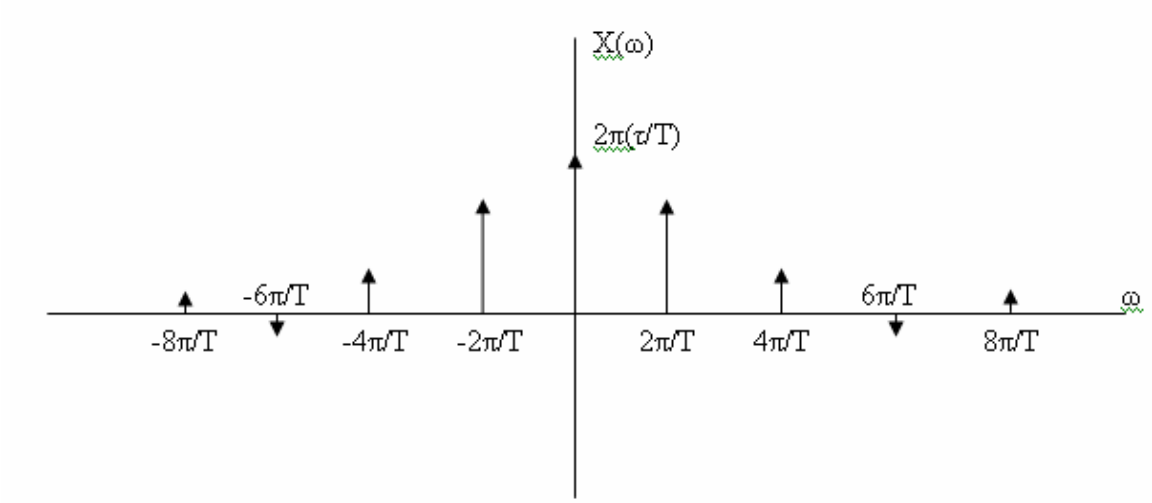


Figure 6.2. Frequency Domain Representation of Figure 6.1 Signal

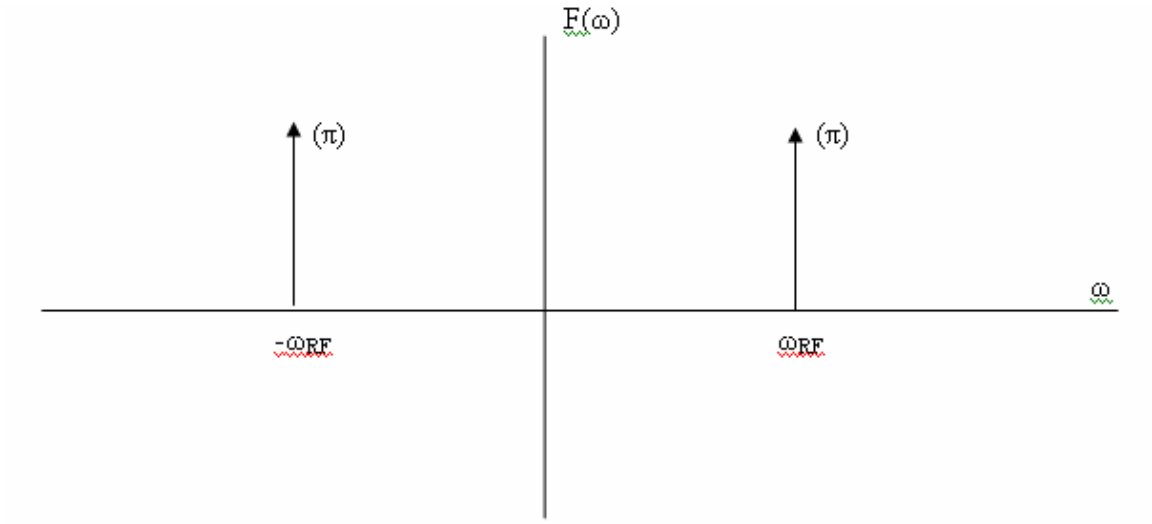


Figure 6.3. Frequency Domain Representation of RF Sinusoidal Waveform

Now consider a pulsed S-parameter measurement; let S_{21} be the parameter undergoing measurement. At the input to the RF switch, the signal possesses frequency content as shown in Figure 6.3. This signal is turned on and off by the function of the RF switch; a multiplication in the time domain. Because multiplication in the time domain is equivalent to convolution in the frequency domain, the resultant signal at the output of the RF switch will have a frequency content equal to the convolution of the frequency-domain representations of the signals shown in Figure 6.2 and Figure 6.3. The convolution of the two spectra will be a (sin x)/x function centered at ω_{RF}. The frequency-domain representation of the signal at the output of the RF

switch is shown in Figure 6.4. Mathematically, if x(t) is the input signal to the RF port of the RF switch, f(t) is the controlling function of the switch, and y(t) is the output of the switch, then the time domain output is given by

$$y(t) = x(t) f(t), \qquad (6.4)$$

and the frequency domain output is

$$Y(\omega) = X(\omega) * F(\omega). \qquad (6.5)$$

How are the calibration and measurement performed? First, it is advised that a narrow-bandwidth filter setting inside the VNA be used for measurement, so that only the center (peak) component of the (sin x)/x function is measured [46]. If this center component is measured for the incident and output signals, then an accurate S-parameter measurement should be obtained. The drawback is that this signal is τ/T times the height of the signal that would be used in a typical continuous-RF S-parameter measurement. If a pulse length of 1 μs is used, for example, with a pulse period of 100 μs, then the signal levels will be 1/100 of those used in a continuous-RF measurement (a 40 dB reduction). So while a small duty cycle is desirable to provide isothermal conditions, a balance trade-off exists between this goal and maintaining suitable signal levels for a measurement of sufficient precision and dynamic range.

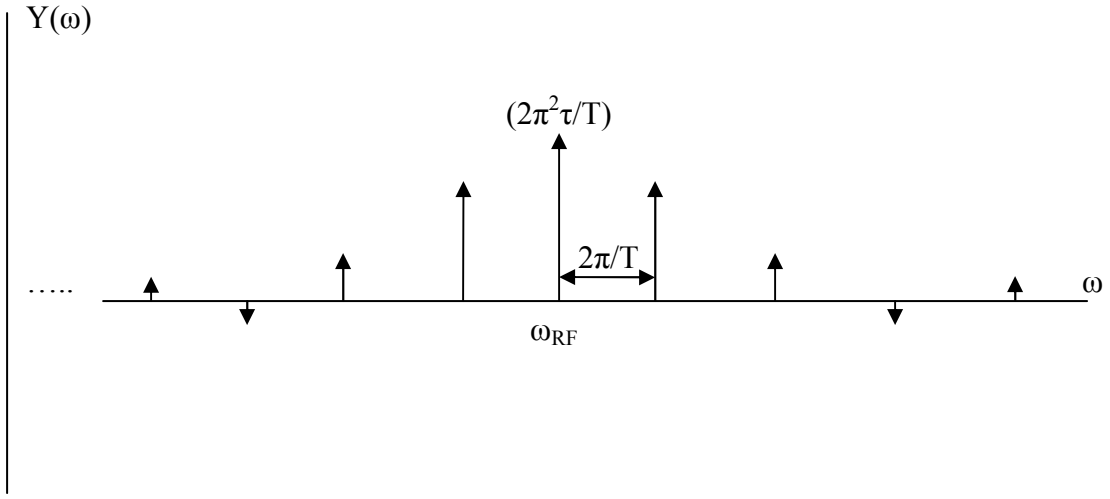


Figure 6.4. Frequency Domain Representation of Signal at Output of RF Switch

6.2 System Benchmarking Using Passive Devices

The system used for measurement is shown in Figure 6.5. S-parameter measurements of passive devices were performed under several different pulse conditions for frequencies from 300 MHz to 3 GHz. A calibration was performed using a K-connector coaxial calibration kit. The measurements were performed with an IF bandwidth of 10 Hz and an averaging factor of 16. The purpose of the small 10 Hz bandwidth is to allow only the center spectral component of the RF test signals to be measured. Averaging was used in an attempt to decrease the noise in the results.

A measure of the precision is the thru validation performed immediately after calibration. These results are shown in Figure 6.6. Settings 2 and 5 are the optimal of the pulsed settings regarding transmission precision. Their relative precision to standard S-parameter measurements can be seen by comparing to setting 1, which is the setting in which the switch is continually on. The second and fourth settings, while possessing identical duty cycles (5 percent) show vastly different precision levels. The measurement with the 1 μs pulse length is much more precise than the measurement with the 0.2 μs pulse length. This may be due partially due to the difference in pulse length and perhaps also caused by the possibility that the measurement with a pulse length of 0.2 μs and period of 4 μs could have spectral lines landing on a system image response.

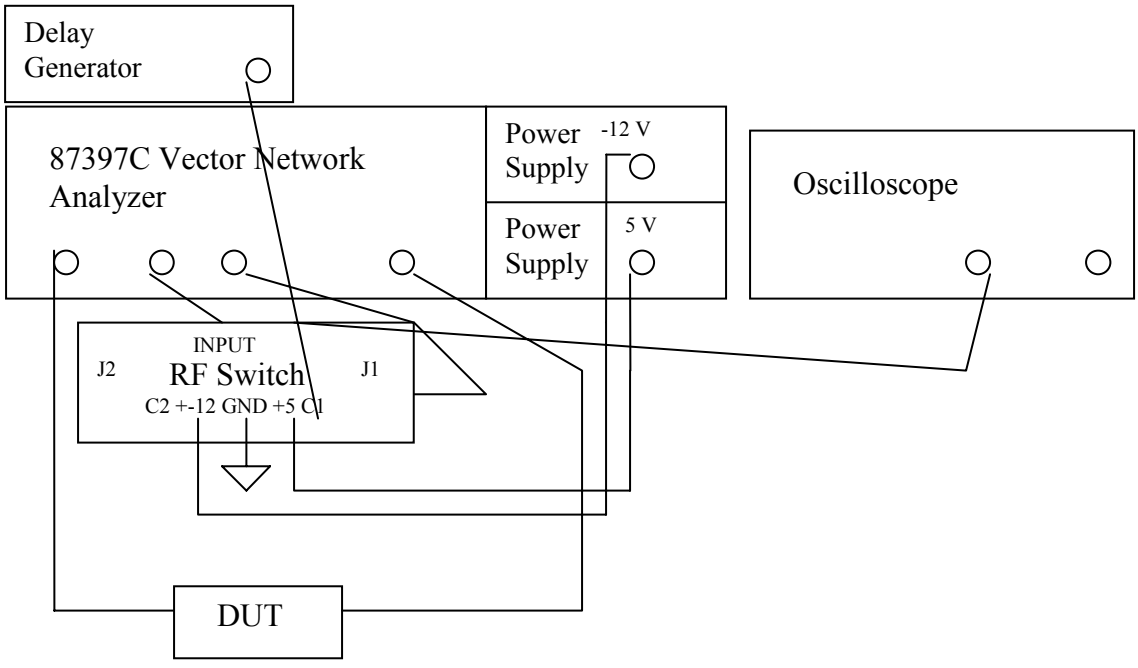


Figure 6.5. Pulsed-RF, Pulsed-Bias S-Parameter Measurement System (Bias Tees Used for Active Devices Not Shown)

The reflection (S_{11}) measurement of the open standard after calibration is shown in Figure 6.7. It can be seen that the precision of this measurement is comparable to that of the thru standard. For the 1 percent duty cycle measurement, the precision is very poor, leading to the conclusion that this setting is not recommended for use in pulsed RF measurements. While this setting is likely the most optimal setting of the five shown as far as obtaining an isothermal condition is concerned, it causes a lack of precision in the data. However, the second and fifth settings show reasonable results. It can be noted that there is a lower precision at the lower frequencies; this is concluded to be due to the RF switch used being designed for frequencies at 1 GHz and higher. As for the transmission measurements, the results seem to demonstrate that precision is a function not only of the duty cycle but also of the pulse length.

The reflection measurement in Figure 6.7 was performed with the switch in the preamplifier loop of the VNA. A similar experiment was performed with the RF switch in the calibration path. While the precision of the transmission measurements was found to be approximately the same, the reflection measurements showed a much lower level of precision, leading to the conclusion that the RF switch should be placed in the preamplifier loop if reflection measurements are to be performed. The S_{11} measurement of the open with the switch in the calibration path for a pulse length of 1 μs and a period of 20 μs is shown in Figure 5.8.

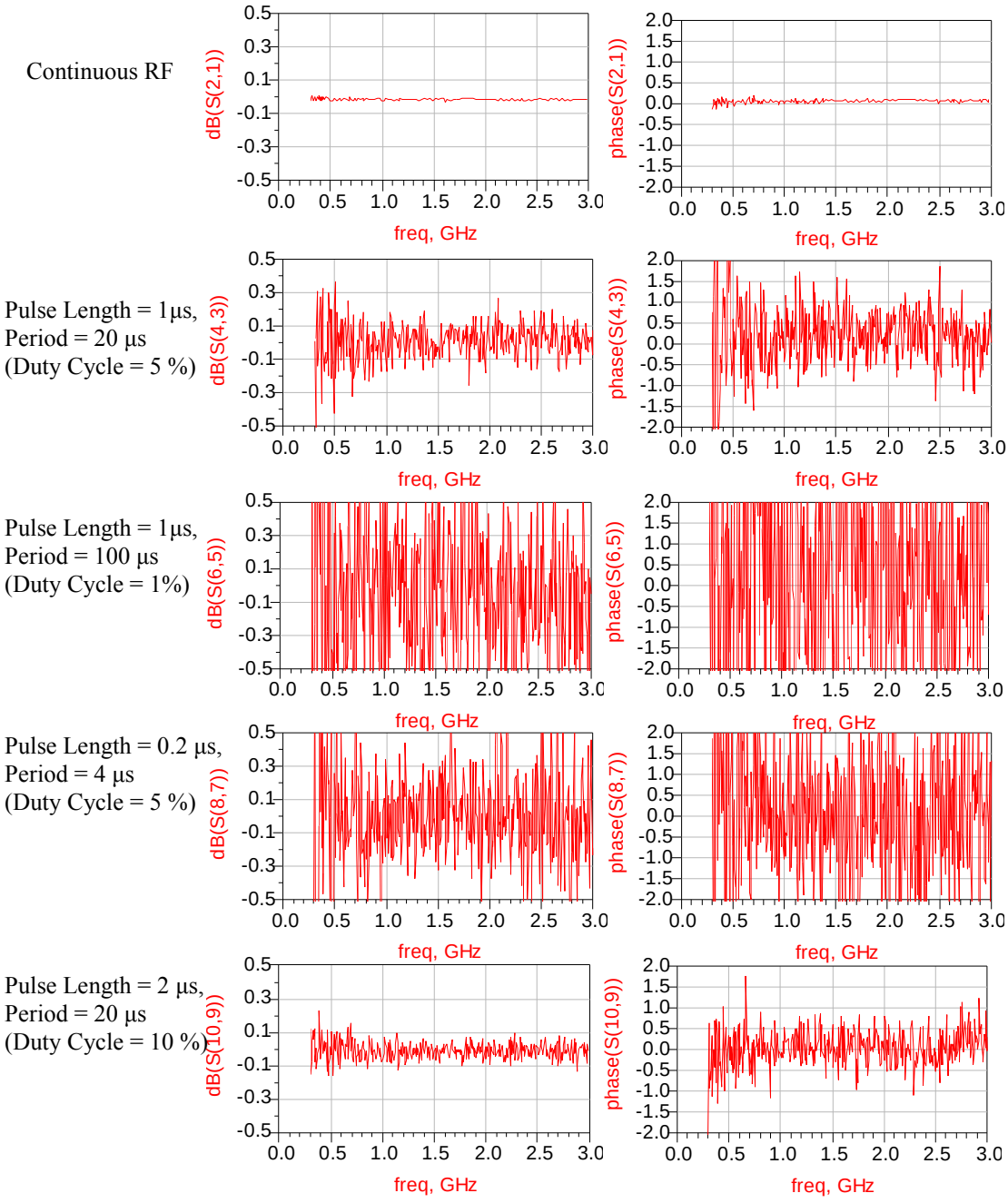


Figure 6.6. S_{21} dB Magnitude (Left) and Phase (Right) Measurements of Thru Immediately After Calibration for Various Pulse Settings

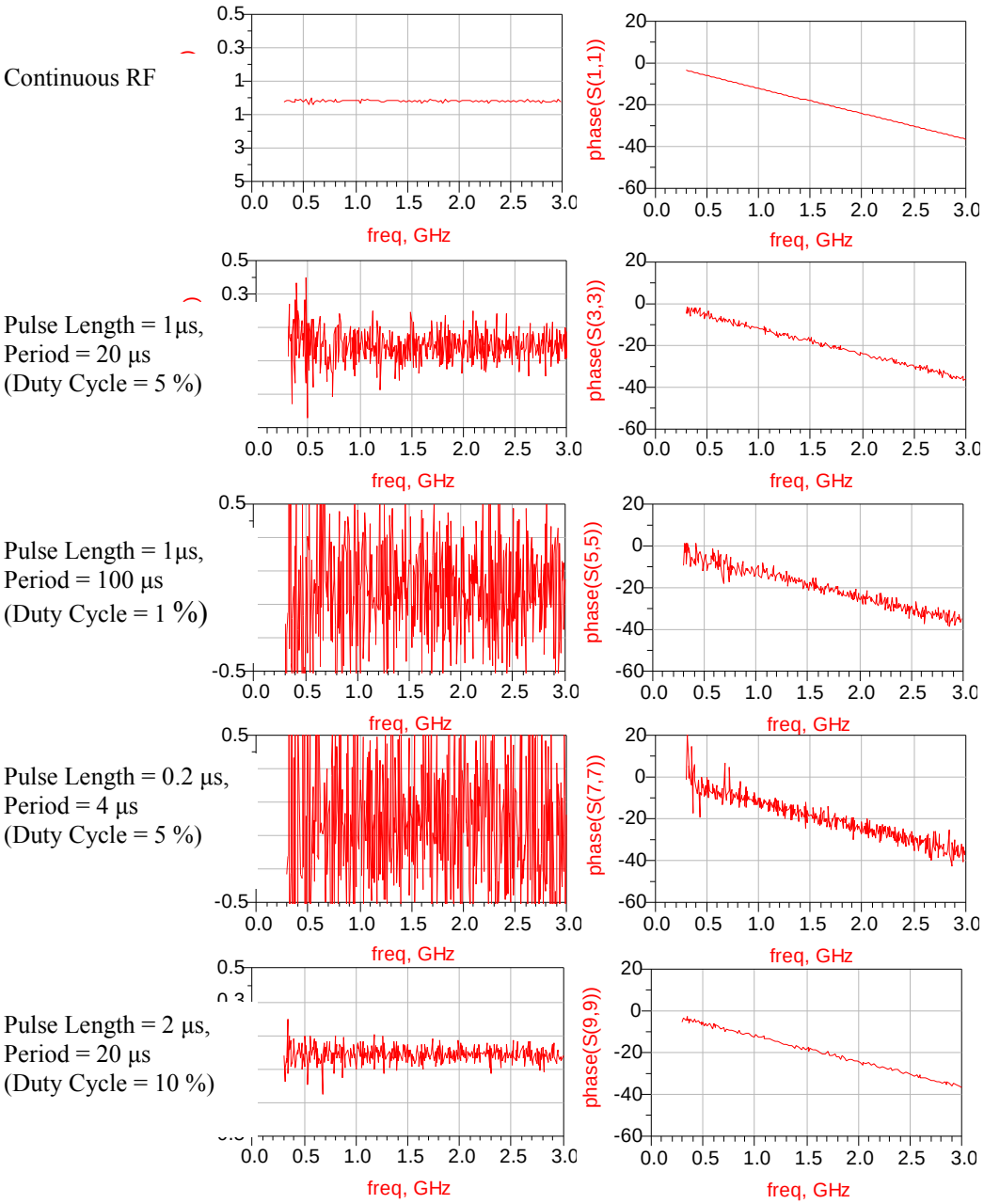


Figure 6.7. S_{11} dB Magnitude (Left) and Phase (Right) Measurements of Open Standard After Calibration for Various Pulse Settings

The dynamic ranges of the measurement settings are illustrated by the measurement of a 915 MHz bandpass filter. Pulsed RF measurements suffer a loss in dynamic range given by equation (6.1). The results show clearly that the measurement with the longest duty cycle (10 percent) has the best dynamic range of the pulsed settings. Also as expected, the setting with the smallest duty cycle (1 percent) has the worst dynamic range. These results are as expected. It can be noted that for the pulse length = 1 μs and period of 20 μs, the noise floor of the transmission measurement appears to be approximately -40 to -50 dB, a reasonable level.

Based on the results of the passive device benchmarking, a pulsed RF setting with a pulse length of 1 μs and period of 20 μs was recommended for use in the pulsed-RF, pulsed-bias S-parameter system.

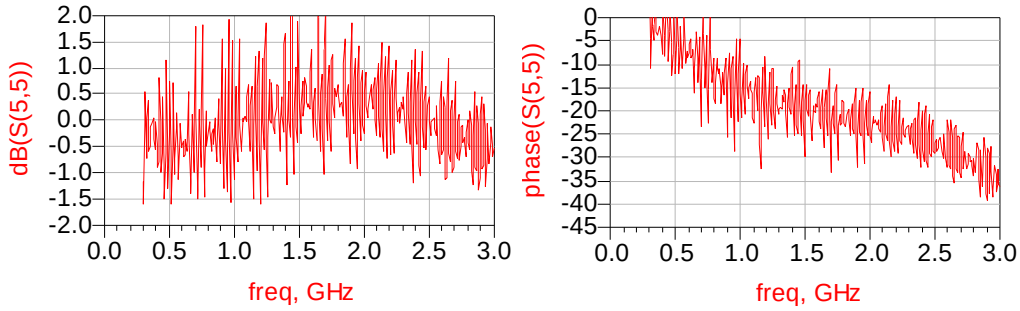


Figure 6.8. S_{11} dB Magnitude (Left) and Phase (Right) Measurements of Open Standard After Calibration with the RF Switch in the Calibration Path (Pulse Length = 1 μs, Period = 20 μs)

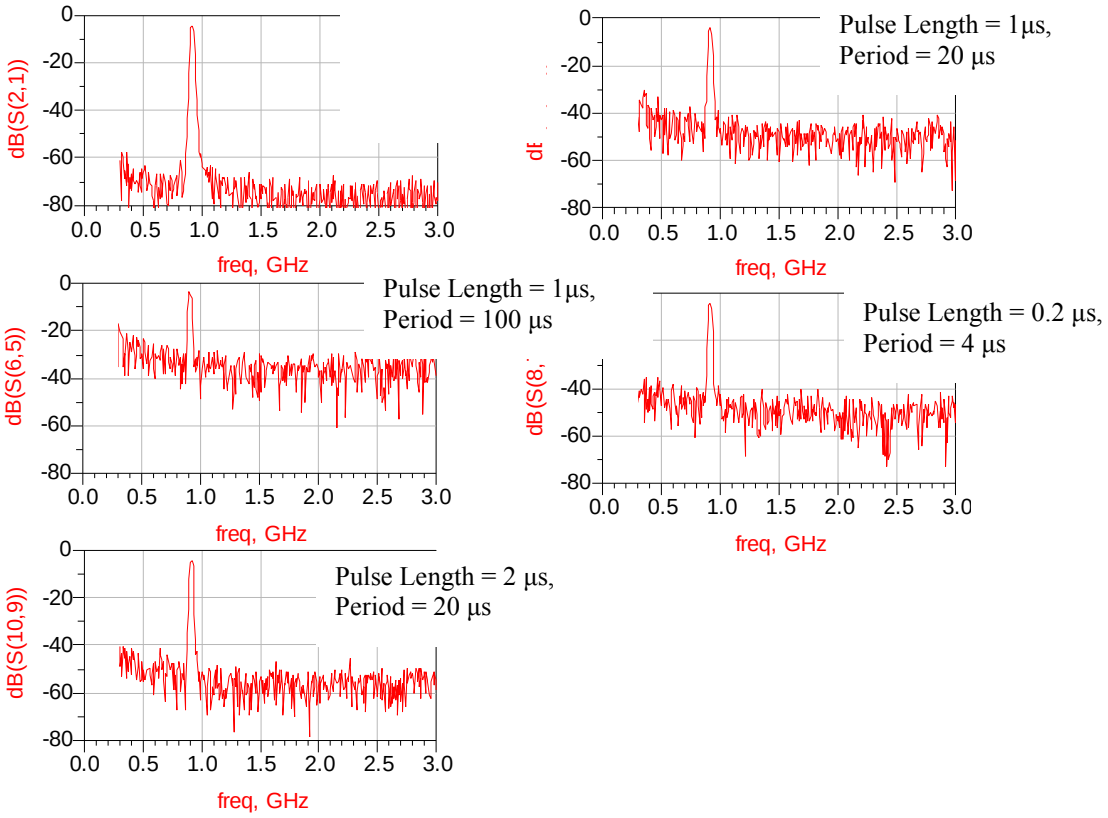


Figure 6.9. S_{21} dB Magnitude (Left) and Phase (Right) Measurements of 915 MHz Bandpass Filter After Calibration for Various Pulse Settings

6.3. Transistor Pulsed-RF, Pulsed-Bias S-Parameter Measurement

Measurement of S-parameters using pulsed conditions allow isothermal S-parameter results to be obtained. How are S-parameters affected by temperature? This question can be partially answered through an examination of the pulsed and static IV curves for a device. The pulsed and static IV curves for a 5 W Si LDMOSFET are shown in Figure 6.10. For a device with minimal trapping effects, it is concluded that these differences are caused by thermal effects that occur in the static IV curves. The transconductance, g_m, is defined as the partial derivative of the current with respect to the gate voltage:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \qquad (6.6)$$

This is manifested in an IV plot as the spacing between the curves. For a larger transconductance, the curves are farther apart, while for a smaller transconductance, the curves are closer together. In addition to a difference in spacing between the pulsed and static IV curves, a difference can be observed in the saturation-region slope of the curves; this illustrates a difference in the output resistance R_{ds} of the devices. If the value of R_{ds} in the device small-signal model is different at this bias point for the pulsed- and continuous-bias cases, it would be expected that the value of S_{22} at low frequencies would be different as well. However, at higher frequencies the drain-source capacitance prevails, causing S_{22} to be independent of R_{ds} at high frequencies. This theory is confirmed in an article by Parker *et al.*: significant differences between pulsed- and continuous-bias measurement results due to heating are observed for S_{21} for the entire band, while differences in S_{22} are observed over only part of the band [9].

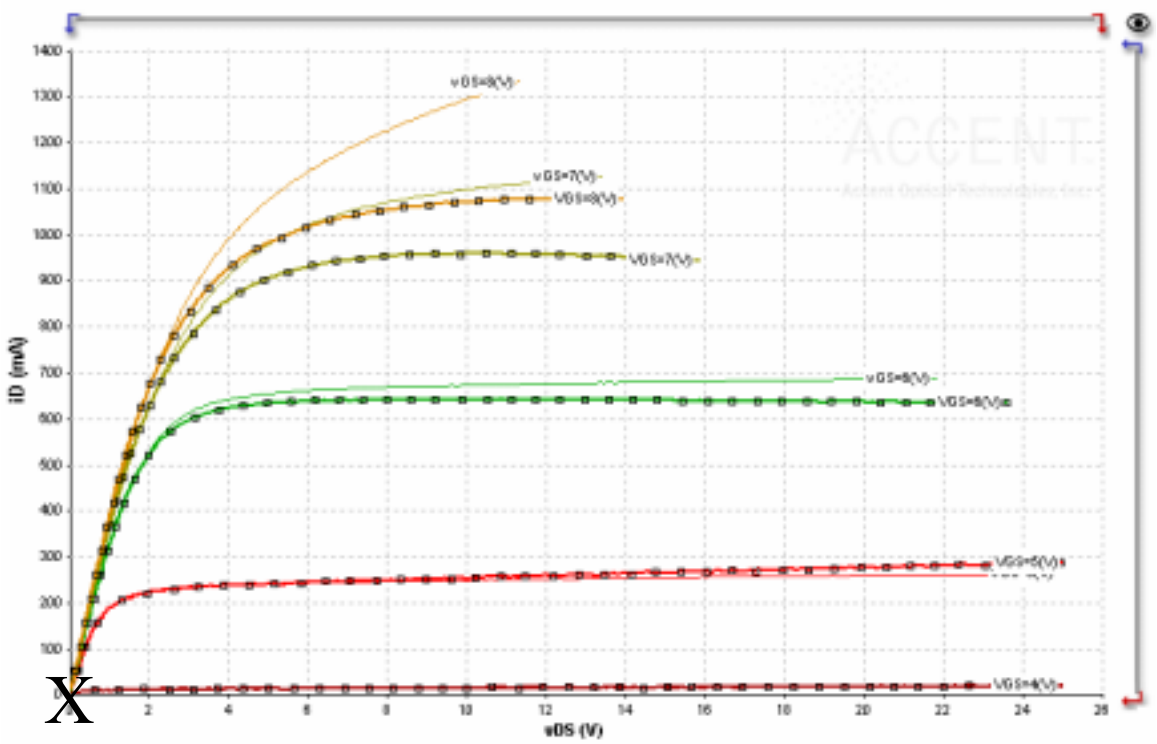


Figure 6.10. Static (Dark Curves) and Pulsed (Lighter Curves; Quiescent Bias Point: V_{GS} = 3.5 V, V_{DS} = 0 V, Shown with an "X") IV Curves for the 5 W Si LDMOSFET

For the Si LDMOSFET, it can be seen from Figure 6.10 that the transconductance of the static and pulsed IV curves is significantly different for the higher gate voltages. The transconductance for the pulsed IV curves at V_{GS} = 7 V, V_{DS} = 10 V is approximately 0.3 A/V,

while for the static IV curves, the transconductance is approximately 0.2 A/V. Because the small-signal, low-frequency voltage gain of a FET is given by

$$A_V = g_m R_L, \qquad (6.7)$$

it is expected that under static bias conditions, the small-signal voltage gain will be significantly lower than the small-signal voltage gain under short-pulse bias conditions for this bias point. This hypothesis was tested by performing a small-signal S_{21} measurement of the device under both continuous-bias and pulsed-bias conditions.

The small-signal S_{21} measurement was performed for the bias point V_{GS} = 7 V, V_{DS} = 10 V under both continuous- and pulsed-bias conditions. The timing of the measurement was as follows: the RF signal was operated during 1 μs pulses with a 20 μs period (duty cycle = 5 percent). This is the timing determined in the results of the previous chapter to provide a compromise between precision and isothermal conditions. In the continuous-bias measurement, the bias was kept at the measurement bias condition over the entire cycle, allowing the self-heating condition to reach steady-state corresponding to this bias. In the pulsed-RF measurement, the bias was pulsed from a subthreshold voltage (V_{GS} = 3.25 V, V_{DS} = 10 V) to the measurement voltage of V_{GS} = 7 V, V_{DS} = 10 V. The subthreshold quiescent bias provides a quiescent measurement condition of approximately zero self-heating, so it is expected that the S_{21} results should be significantly different in the pulsed- and continuous-bias cases due to self-heating in the continuous-bias case and the lack of self-heating in the pulsed-bias case. The bias voltage was set to "turn on" 0.1 μs before the RF and was "turned off" 0.1 μs after the RF, so the bias signal consisted of pulses 1.2 μs in length with a period of 20 μs. The pulsed-RF, pulsed-bias measurement was also repeated using a pulse length of 10 μs (10.2 μs for the bias signal) and a period of 200 μs. The results from the three measurements are shown in Figure 6.11.

It is apparent that the measurements performed with the pulse lengths of 1.2 μs and 10.2 μs show a significantly higher $|S_{21}|$ (the difference approaches 2 dB at some frequencies). Also, it can be noted that the value of $|S_{21}|$ appears to be slightly higher over the band for the pulse length of 1.2 μs than for the pulse length of 10.2 μs. Both of these are indications that the value of g_m is lower when the device is operated under continuous-bias conditions; this is consistent with observations from pulsed and static IV curves that g_m decreases with increasing temperature. This effect is exactly what is seen in the IV curves: the static IV curves are more closely spaced at higher gate voltages due to the effects of self-heating. This illustrates the importance of using pulsed S-parameter measurements for multiple-bias measurement routines used in large-signal

model extraction. It can also be noticed that the phase of S_{21} is approximately the same in all three cases.

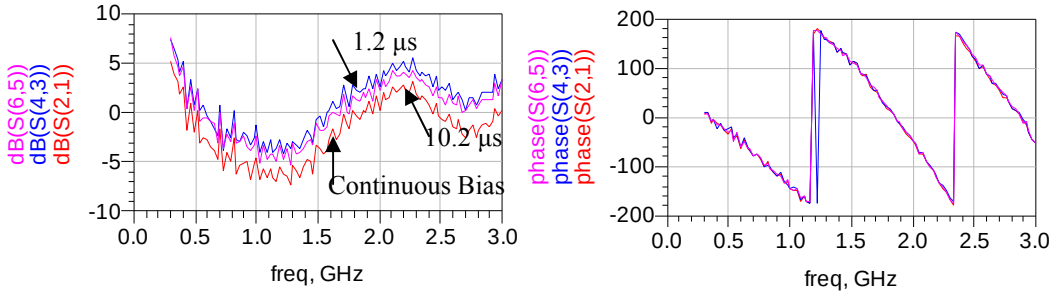


Figure 6.11. Continuous-Bias and Pulsed-Bias Results for Pulse Length = 1.2 µs, Period = 20 µs and Pulse Length = 10.2 µs, Period = 200 µs

In addition to the measurement of the LDMOSFET, S-parameter measurements were performed for the Si VDMOSFET discussed in previous chapters. The static IV curves and pulsed IV curves taken from a quiescent bias point of zero power dissipation are displayed in Figure 6.12. At a bias condition of V_{GS} = 7 V, V_{DS} = 10 V (labeled "B" in Figure 6.12), it can be observed from the IV curves that both the output resistance and transconductance of the FET are significantly different under pulsed and static bias conditions. This leads to the conclusion that differences should be observed between continuous- and pulsed-bias measurement data for the magnitude of S_{21} and possibly the low-frequency magnitude of S_{22}.

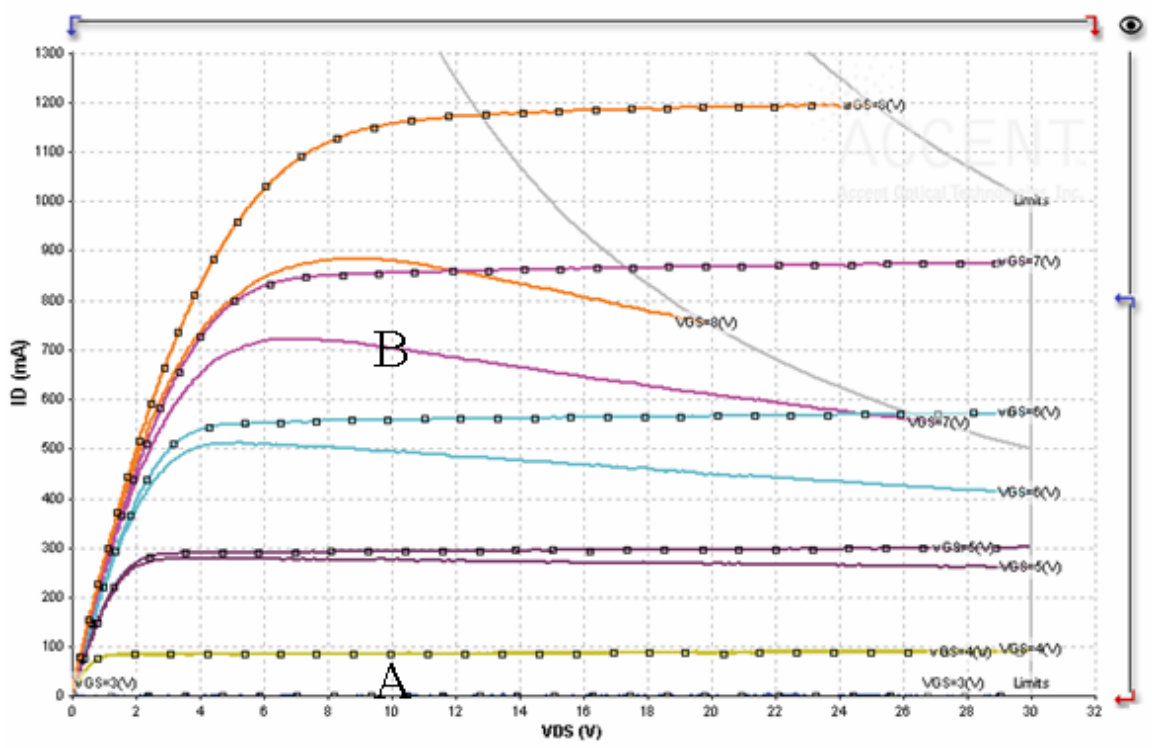


Figure 6.12. Si VDMOSFET Static (Solid Lines, No Squares) and Pulsed (Quiescent Bias: V_{DS} = 28 V, V_{GS} = 2 V, Lines with Squares) IV Curves at 25 °C to V_{DS} = 30 V

The S-parameters for the VDMOSFET were measured using an Anritsu 39397C "Lightning" Vector Network Analyzer. Custom calibration standards obtained from Modelithics, Inc. on a 14 mil FR4 substrate were used to perform a short-open-load-thru (SOLT) calibration. The calibration coefficients were loaded into the front panel of the VNA. The calibration standards were modeled using measurements performed with a thru-reflect-line (TRL) calibration. The S-parameter measurement was performed from 300 MHz to 3 GHz. Three different settings were used for measurement: (A) continuous-bias, continuous-RF, (B) continuous-bias, pulsed-RF, and (C) pulsed-bias, pulsed-RF. To measure all four S-parameters in pulsed mode with the 37397C VNA, it is necessary to perform two one-path, two-port measurements, one with the device oriented in the forward direction and the other with the device in the reverse direction. The reason for this is that placing the RF switch in the pre-amplifier loop only switches the RF signal delivered to port 1 of the VNA. Thus, for the RF to be switched for the device port 2 source (required for the measurement of S_{12} and S_{22}), it is necessary that the device be placed with the drain connected to port 1 of the VNA. In the results that follow, the

results of the forward path measurement (S_{11} and S_{21}) are first shown and analyzed, followed by presentation and analysis of the reverse path parameters (S_{12} and S_{22}).

A comparison of the forward-path results measured with a chuck temperature of 25 ˚C is provided in Figure 6.13. The first measurement was performed under continuous-bias, continuous-RF conditions. The bias was held constant at V_{GS} = 7 V, V_{DS} = 10 V for this measurement. The second measurement was performed under continuous-bias, pulsed-RF conditions. In this case, the RF test signal was operated with an "on" time of 1.0 µs and a period of 20 µs (a duty cycle of 5 percent). The third measurement was performed under pulsed-bias, pulsed-RF conditions. The RF test signal was operated with the same timing as the previous measurement; however, the bias pulsing was performed for a pulse length of 1.2 µs and a period of 20 µs. The timing of the bias pulses was designed such that the bias pulse begins 0.1 µs before the RF burst and ends 0.1 µs after conclusion of the RF burst.

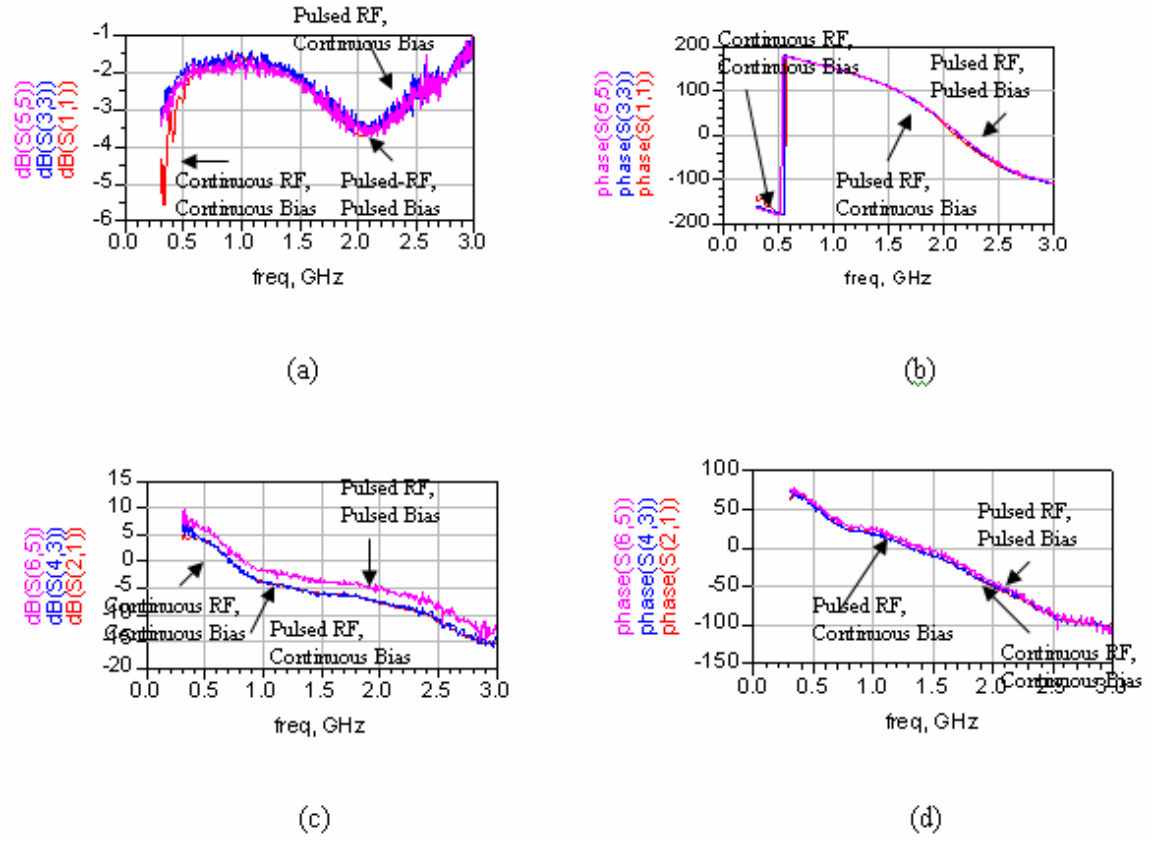


Figure 6.13. Pulsed-RF, Pulsed-Bias S-Parameter Measurement Results: (a) $|S_{11}|$ in dB, (b) $<S_{11}$ in Degrees (c) $|S_{21}|$ in dB, (d) $<S_{21}$ in Degrees

Figure 6.13 shows that the continuous-RF and continuous-bias results for the VDMOSFET are nearly identical to the pulsed-RF, continuous-bias results. However, it appears that the pulsed-RF, pulsed-bias results show a substantial difference from the other two settings for $|S_{21}|$, while that the pulsed-RF, pulsed-bias results are similar to the other two settings for all of the other measurements shown. The difference in $|S_{21}|$ is, in essence, predicted by the pulsed and static IV curve demonstration of the difference in transconductance between the two settings.

The reverse-path S-parameter (S_{12} and S_{22}) measurement results are shown in Figure 6.14. For the S_{22} results, no significant difference is observed between the pulsed-bias case and the continuous-bias cases; however, the pulsed-bias case results have much larger fluctuations over frequency than the continuous-bias cases. This coincides with expectations; the measurement was only performed down to 300 MHz, so it is likely that the drain-source capacitance is covering the effect of the output resistance difference between pulsed and static conditions.

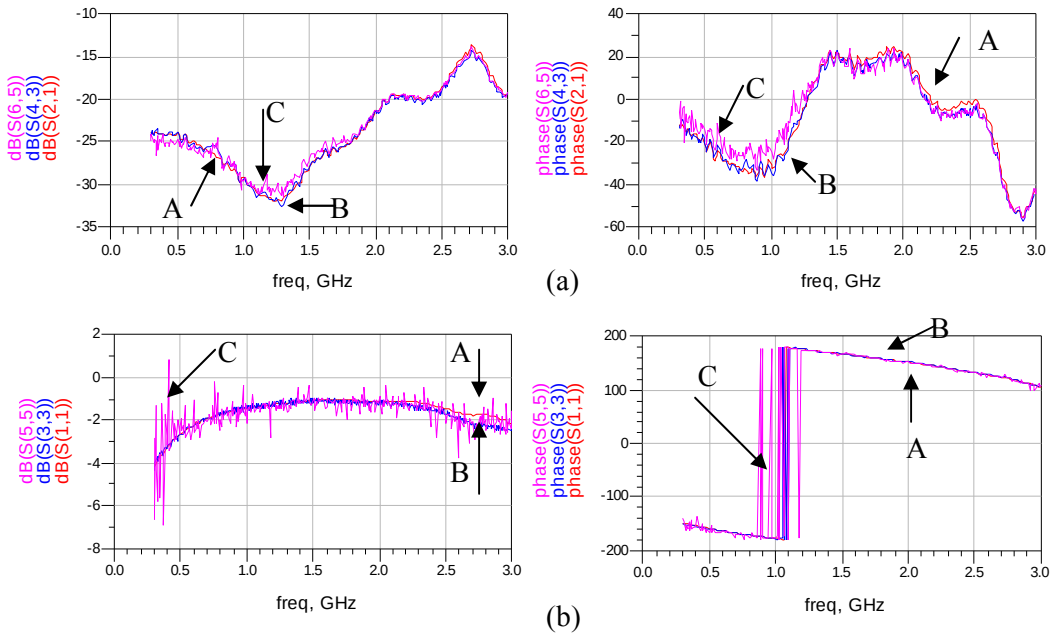


Figure 6.14. dB Magnitude (Left) and Phase (Right) Results for (a) S_{12} and (b) S_{21} under (A) Continuous-Bias, Continuous-RF, (B) Continuous-Bias, Pulsed-RF, and (C) Pulsed-Bias, Pulsed-RF Conditions at T_A = 25 °C

6.4. Temperature Compensation for Self-Heating in Continuous-Bias S-Parameter Measurements

Parker *et al.* have demonstrated that the adjustment of the ambient temperature by an appropriate amount allows S-parameter results to be obtained in continuous mode instead of using pulsed S-parameter measurements. In this paper, the authors suggest that this temperature can be predicted from static and pulsed IV curves [9]. A similar approach was used in this work, with an adjustment of the chuck temperature being used to compensate for the device self-heating difference from a desired quiescent operating point and the bias point used for S-parameter measurements.

Because a change is observed in the S_{21} value as a result of self-heating in the device channel, the measurement results taken in multiple-bias S-parameter measurements for use in large-signal model extraction may reflect an incorrect device channel temperature. However, the device channel temperature T_C is given by the oft-repeated equation

$$T_C = R_{th} P_D + T_A, \qquad (6.8)$$

where R_{th} is the thermal resistance of the device, P_D is the power dissipated at the bias point (equal to $V_{DS}I_D$), and T_A is the ambient temperature. Because the S-parameter results at a given bias point are concluded to be a function of the channel temperature T_C, then measurements performed at identical channel temperatures should yield identical results, regardless of what percentage of that channel temperature results from self-heating and what percentage results from the ambient chuck temperature. In the previous section, a continuous-bias S-parameter measurement was performed for the quiescent bias point V_{GS} = 7 V, V_{DS} = 10 V (marked "B" in Figure 6.12). From the static IV curves of Figure 6.12, it can be observed that the current at this bias point is approximately 700 mA. Thus the power dissipated for this quiescent bias point is

$$P_D = V_{DS} I_D = (10)(0.700) = 7 \text{ W}.$$

In model extraction procedures performed at Modelithics, Inc. for this device, the FET was found to have a thermal resistance of approximately 9 ˚C/W. Thus, the channel temperature in this device for a measurement performed at an ambient temperature of 25 ˚C is given by equation (6.7) as

$$T_C = 9(7) + 25 = 88\,^{\circ}\text{C}.$$

To test the hypothesis that the device S-parameter results depend on the channel temperature, a pulsed-bias S-parameter measurement was performed at approximately this channel temperature (the chuck temperature was measured at 93.4 ˚C for the measurement). The pulsed bias

measurement was performed from a quiescent bias point of zero power dissipation (V_{GS} = 3 V, V_{DS} = 10 V, marked "A" in Figure 6.12) and the measurement was performed for the above bias point (V_{GS} = 7 V, V_{DS} = 10 V, marked "B" in Figure 6.12). These pulsed-bias results are compared with the continuous-bias results from the previous section in Figure 6.15.

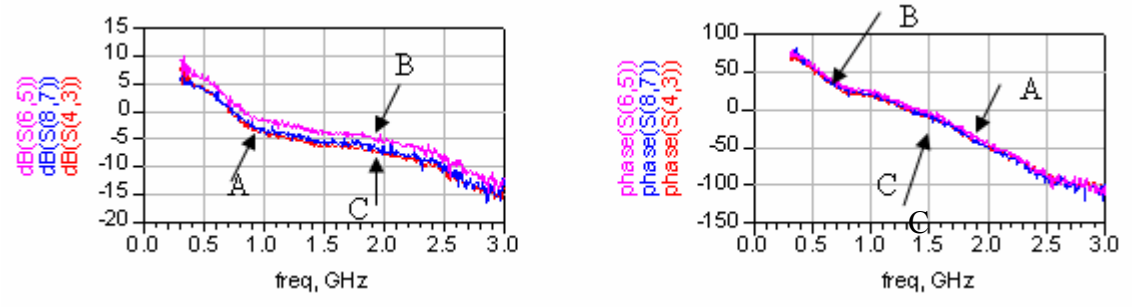


Figure 6.15. S_{21} Magnitude in dB (Left) and Phase in Degrees (Right) for (A) Continuous Bias at T_A = 25 ˚C, (B) Pulsed Bias at T_A = 25 ˚C, and (C) Pulsed Bias at T_A = 93 ˚C

Figure 6.15 shows that, as hypothesized, the increase in chuck temperature by the same amount as the calculated self-heating in the T_A = 25 ˚C, continuous-bias case has caused the magnitude of S_{21} for the pulsed-bias, T_A = 93 ˚C case to be identical. This yields the conclusion that an adjustment of the chuck temperature by a temperature equal to the difference between the self-heating of the non-quiescent bias point being used for the small-signal S-parameter measurement and the quiescent operating bias point for which the model is being developed allows S-parameter data to be obtained that has a thermal dependence on the desired quiescent operating point. This is a viable alternative to pulsed S-parameter measurements for devices with only thermal effects.

6.5. An Algorithm for Measuring Isothermal S-Parameters Under Continuous-Bias Conditions

A suggested procedure for measuring isothermal multiple-bias small-signal S-parameter measurements by thermal correction in devices with minimal trapping effects is as follows: Let the quiescent operating bias point for which the model is extracted be given by (V_{GSQ}, V_{DSQ}) with resultant quiescent current I_{DQ} and power dissipation P_{DQ}. Assume that the capacitance functions of the large-signal model are extracted from multiple-bias S-parameter measurements at N

different bias points given by (V_{GSi}, V_{DSi}) with resultant current I_{DSi} and power dissipation P_{Di}. Assume that it is desired to extract the large-signal model for the ambient temperature T_{AQ}. First, measure the thermal resistance R_{th} using methods described in [6] or [7]. Second, for each bias setting i = 1, 2, …, N, calculate the difference in self-heating between bias setting i and the quiescent bias setting (let this be denoted by d_i) :

$$d_i = R_{th}P_{Di} - R_{th}P_{DQ} \qquad (6.9)$$

Third, for each bias setting i = 1, 2, …, N, calculate the ambient temperature for which the small signal S-parameter measurement should be made at that bias point, given by T_{Ai}:

$$T_{Ai} = T_{AQ} - d_i . \qquad (6.10)$$

Finally, measure small-signal S-parameters at each bias setting i = 1, 2, …, N at ambient temperature T_{Ai} and insert the results into the computer extraction tool to extract the large-signal model capacitance functions for ambient temperature T_{AQ}.

The above algorithm is simple enough that it can be performed manually during small-signal S-parameter measurements, but it may eventually be able to be implemented in automated measurements, assuming that automatic control of the chuck temperature is available and necessary waiting times (to allow the device to reach steady-state ambient temperature conditions) can be programmed. This algorithm is powerful in that it allows isothermal S-parameter data to be obtained without the necessity of performing pulsed-bias S-parameter measurements for a large class of devices. Obviously, this is advantageous because the continuous-bias, continuous-RF measurement does not have the precision and dynamic-range challenges of the pulsed-bias, pulsed-RF measurements. Of course, such an algorithm is completely accurate only for devices whose trapping effects are negligible.

6.7. Chapter Summary

This chapter has described the benchmarking of a pulsed-RF, pulsed-bias S-parameter system using an Anritsu Lightning 37397C Vector Network Analyzer. The importance of the benchmarking process is to provide a feel for the precision and dynamic range achievable with a given pulsed setting and to establish the accuracy, precision, and dynamic range with which pulsed S-parameter measurements will be able to be performed with this system. This was achieved through measurement of calibration standards and a passive bandpass filter. Finally, a pulsed-RF, pulsed-bias S-parameter measurement of a Si LDMOSFET was performed.

The effect of temperature on small-signal S-parameter measurement results has been explored, both theoretically and experimentally. The channel temperature of a device affects the small-signal transconductance g_m and the output resistance R_{ds}. Pulsed- and continuous-bias S-parameter results were examined for a Si LDMOSFET and Si VDMOSFET and it was shown that the value of $|S_{21}|$, which is directly related to transconductance, is significantly different in the pulsed- and continuous-bias cases. It was also expected that differences might be seen in low-frequency S_{22} due to dispersion in the output resistance; however, measurements were only performed down to 300 MHz and no definite dispersion of this type was observed, likely due to the drain-source capacitance of the device.

A study in the thermal correction of continuous S-parameter results was performed. A continuous-bias S-parameter measurement of the VDMOSFET was performed at an ambient temperature of 25 ˚C. Using the thermal resistance of the device and calculating the power dissipated at the quiescent bias point of this measurement, it was calculated that self-heating of just under 65 ˚C was incurred due to the quiescent bias point. The chuck temperature was then raised by an amount approximately equal to this self-heating and a pulsed-bias S-parameter measurement was performed. The results nicely matched the original continuous-bias results. Based on the results of this measurement, an algorithm is proposed that allows chuck temperature adjustment in multiple-bias S-parameter measurements to allow results with the thermal dependences of the desired quiescent bias point to be obtained.

CHAPTER 7: A SEQUENTIAL SEARCH ALGORITHM FOR MORE EFFICIENT LOAD-PULL MEASUREMENTS

In this chapter, a new implementation of an efficient sequential search algorithm applied to microwave load-pull measurements is presented. The algorithm significantly reduces the number of reflection coefficient states necessary for determination of the maximum-power reflection coefficient and power value. This search routine has been implemented in software that can be used to control both measured and simulated load-pull. The reduction in the required number of reflection coefficient states facilitates a measurement-versus-simulation comparison, for example, power- or bias-swept load-pull, in which a load-pull is performed for several levels of input power or bias. Among the many advantages of this new technique over conventional load-pull are that it allows more efficient determination of peak-power performance on multiple devices or over varied conditions, such as input power, bias, or frequency.

7.1. The Need for Faster Load-Pull Measurements

In the design and configuration of power amplifiers, it is often desirable to find the optimal transistor load impedance using only a small number of load-pull measurements. A new algorithm has been designed that provides for the efficient determination of an optimal loading condition. Such an algorithm should be useful in many ways. A reconfigurable power amplifier designed to operate in different frequency ranges may need to efficiently perform an on-chip load-pull to determine the optimum loading condition for a new frequency range [47]. Ongoing studies have also shown that significant time and money can be saved by the use of such an algorithm in wafer-mapping and transistor-characterization related measurements. Figure 7.1, provided by Raytheon, Inc., shows output power, gain, and power-added efficiency (PAE) at the maximum-power load impedance over swept drain voltage. To obtain the data necessary to construct this plot, it is necessary to perform a load-pull measurement for each bias setting to determine the maximum power impedance. In such a characterization, it is desirable to converge to the maximum power impedance with only a small number of measured states.

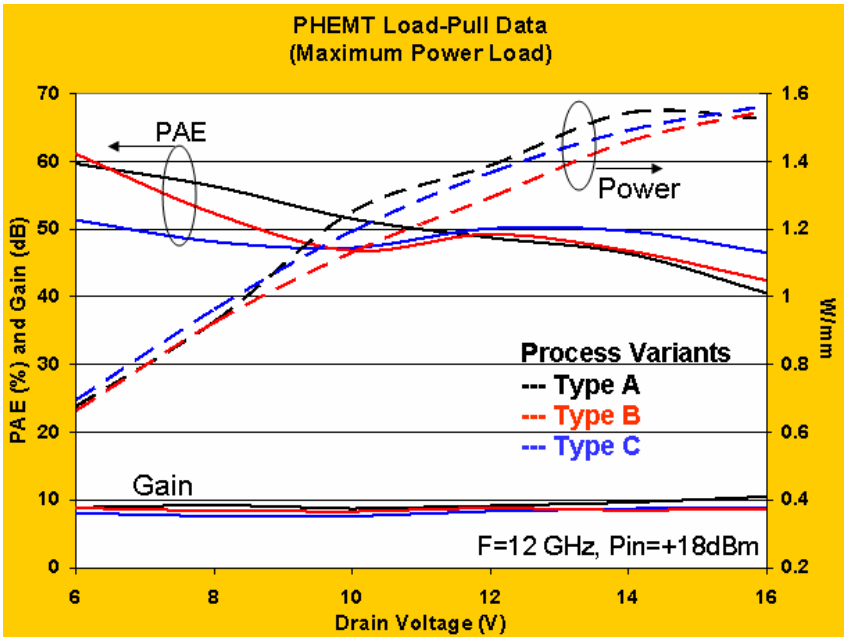


Figure 7.1. Power, Gain, and Power-Added Efficiency (PAE) Versus Drain Voltage at the Maximum Power Load Impedance (Provided by Raytheon, Inc., Used with Permission)

What are the requirements for the construction of an efficient algorithm? The measurement of each impedance state requires a significant amount of time; therefore, it is desired that the number of impedance states measured be minimized. By strategically choosing the measured data points to provide information on the power-versus-impedance characteristic, this can be accomplished. The steepest ascent algorithm uses a minimal number of points to obtain this information and proceeds intelligently and efficiently through its search. The implementation of this algorithm in MATLAB [48] is demonstrated; additionally, the use of MATLAB to control Agilent Advanced Design System (ADS) [15] is shown and the use of the algorithm to perform a load-pull simulation for a GaAs PHEMT model is provided. The results are compared with traditional load-pull simulation results and found to match very well. The algorithm has also been implemented in measurement of a GaAs PHEMT using the Maury Microwave Automated Tuner System (ATS) [49] software.

7.2. The Steepest Ascent Algorithm for Load-Pull

The problem at hand in the design of more efficient load-pull experiments is one of finding the optimum point of an unknown function, such as output power or power-added efficiency, with a minimum number of experiments. In a load-pull measurement or simulation,

several points are measured throughout the Smith Chart. The number of points depends on information that is previously available concerning the device and the level of precision required from the measurement. The measurement concludes upon finding the reflection coefficient providing, say, the maximum delivered output power. The output power is referred to as the *criterion*, the property for which other parameters are to be adjusted for optimization. The criterion is the dependent variable. In the load-pull measurement, this criterion is a function of a complex variable, the load reflection coefficient Γ_L. However, because the independent variable is complex, it can be treated as two real independent variables, $\Gamma_r = \mathrm{Re}(\Gamma_L)$ and $\Gamma_i = \mathrm{Im}(\Gamma_L)$. Thus, the problem under consideration is the optimization of the two-variable output power function $P(\Gamma_r, \Gamma_i)$.

There are two basic types of searches that can be used in the search for an optimum point. A *simultaneous search* is a search in which the reflection coefficient values where experiments will be performed are specified in advance of the search. A conventional load-pull measurement is an example of a simultaneous search. A *sequential search* is a search in which the reflection-coefficient values at which future experiments are performed are based upon the outcomes of previous experiments. A sequential search is advantageous for finding an optimum point due to the fact that it avoids performing unnecessary measurements; according to Wilde, this advantage increases significantly with the number of experiments performed [50].

It was decided to use a sequential algorithm to minimize the number of total measured impedance states. Several search methods are available. Perlow has described an algorithm that uses multiple measurements to determine the location of a contour and continues to ascend in the search [51]. De Hek et al have described a method that begins with measured points at a significant radius on the Smith Chart and calculates the location and value of the maximum power from a function fit to the data points. The search is repeatedly re-iterated at smaller radii until the solution converges with respect to power and Smith Chart location for decreasing radius of the measurements [52]. Genetic algorithms are often useful when a random search is desired [47]. The steepest ascent method is a commonly used deterministic search method and is the method adopted for this search.

The reasoning behind the choice of the steepest ascent method is based on the small number of measurements required and the flexibility of this method to overcome noisy measurement data. Qiao *et al.* propose that, while genetic algorithms are more robust, they often require more experiments for convergence [47]. Copalu *et al.* state that the steepest ascent method is often advantageous because it can work under arbitrary criterion functions; it is likely

that this algorithm will have more flexibility in finding the impedance for maximum efficiency, optimum ACPR, or linear combination of multiple criteria. In addition, it is very statistically likely to find an optimal solution, it is relatively easy to code, and normally provides a good answer, even if not converging to the actual maximum power impedance [53]. Though similar in concept, it is expected that the steepest ascent method proposed in this paper will converge with fewer measurements than the method of Perlow [51] in many cases and will likely be less likely to result in device failure than using the method of de Hek [52], which allows many measurements in regions of the Smith Chart far away from the optimum point, some of which could provide damage to the device due to the large power mismatch. Berghoff *et al.* have proposed a method in which the phase and attenuation of the load tuner are iteratively optimized one at a time [54]; however, Wilde notes that methods that optimize one variable at a time may not result in finding the maximum [50]. The literature also contains examples of methods that allow contours to be efficiently plotted [55]; however, the objective in this problem is to find the impedance of maximum power; the contours are not of as large a concern.

The steepest ascent method requires that the criterion function be unimodal. Unimodality implies that there exists only one interior maximum in the Smith Chart. This assumption is true for the transistor output power; this can be verified by the fact that contours can be drawn for given levels from the maximum power as ovals [2]. Practically, three situations could cause the measured power function not to possess perfect unimodality: uncertainty in measurement data, the existence of Smith Chart readings where the actual device output power is below the noise floor of the measurement, and oscillation during measurement, where a higher output power may be read than under stable conditions and derail the search. Regarding the first problem, the steepest ascent method is relatively robust due to the fact that it requires multiple measurements for a conclusion to be reached concerning the maximum power impedance; a mistake in direction due to a measurement uncertainty will likely be overcome. For the second case, which could occur in pulsed measurements (which inherently possess a lower dynamic range), for example, it might be advisable to allow a random search to be used to first direct the search into a region above the noise floor, then switch to the steepest ascent search. Likewise, the third issue could also be addressed by detection of oscillation and switching to a random search to change search regions. These topics are reserved for future work.

The search is divided into two parts. In the initial stage of the search, the region of the maximum point is found to within a specified neighboring_point_distance. In the second stage of the search, output power is measured for multiple impedances in the region of maximum power,

and a second-order function is constructed and used to calculate the maximum power and the reflection coefficient providing maximum power.

A good starting point for the development of the algorithm was taken from Wilde [50]; who suggests breaking the search into stages and provdes the following deriviation. The search can be divided into initial and final stages. In the initial stage, a good strategy is to take one point in each direction about the starting point, changing only one of the coordinates for each point. Thus, the experiment begins with the measurement of three reflection coefficient values. From these measurements, we can construct an equation for a plane tangent to the response at the starting point (being concerned only with the changes of P, Γ_r, and Γ_i from their values at the starting point):

$$\Delta P(\Delta\Gamma_r, \Delta\Gamma_i) = m_1\Delta\Gamma_r + m_2\Delta\Gamma_i . \qquad (7.1)$$

For the case of two independent variables (the case of a load-pull measurement), it can be shown that the direction of maximum rate of increase of the criterion is perpendicular to the contour. If ΔP is set to zero in the above equation, the equation for the contour tangent is obtained:

$$\Delta\Gamma_i = -\frac{m_1}{m_2}\Delta\Gamma_r \qquad (7.2)$$

The line perpendicular to this line has a slope that is the negative reciprocal of the slope of this line; hence the equation of the line along which the rate of increase is maximal is

$$\Delta\Gamma_i = \frac{m_2}{m_1}\Delta\Gamma_r . \qquad (7.3)$$

The first step is thus to find the equation of the tangent line. This can be accomplished by measuring two points, say in a constant radius, but at different angles from the starting point. This gives the coefficients for equation (7.1). If the points are measured in the same radius, the values $\Delta\Gamma_r$ and $\Delta\Gamma_i$ can be parameterized in terms of the angle from the starting point, θ:

$$\Gamma_r = r\cos\theta \qquad (7.4)$$

$$\Gamma_i = r\sin\theta \qquad (7.5)$$

In this case, the equation for the criterion can be written in terms of θ:

$$\Delta P = m_1(r\cos\theta) + m_2(r\sin\theta) \qquad (7.6)$$

To find the maximum direction of increase, ΔP is differentiated with respect to θ and the derivative is set to zero:

$$\frac{\partial P}{\partial\theta} = -m_1 r\sin\theta + m_2 r\cos\theta = 0 . \qquad (7.7)$$

It is now possible to substitute back into this equation for $\Delta\Gamma_r$ and $\Delta\Gamma_i$:

$$\frac{\partial P}{\partial \theta} = -m_1\Gamma_r + m_2\Gamma_i = 0\,. \qquad (7.8)$$

This gives the equation of a line in the direction of the minimum increase. The highest point on the circle of radius r is where this line, also written as

$$\Delta\Gamma_i = \frac{m_2}{m_1}\Delta\Gamma_r\,, \qquad (7.9)$$

intersects the circle on which the two points were measured:

$$\sqrt{\Gamma_r^{\,2} + \Gamma_i^{\,2}} = r \qquad (7.10)$$

where r is the distance from the present candidate point to the next candidate point. From these two points, the point which is calculated to have a value of $\Delta P > 0$ from equation (7.1) is the next point for measurement. There are, of course, two solutions for the intersection of the line and the circle. Both of these solutions can be entered into equation (7.1) and the direction from the center point to the maximum of these two points should be selected as the direction to proceed. Following this step, a new experimental point should be chosen along this direction. If the new reflection coefficient gives an increase in the output power value, the process is repeated at this new point. If this point causes a decrease in the criterion value, then the distance from the original point along this line should be reduced and a new point selected. This method for selecting the next experimental point is similar to that illustrated for the contour tangent elimination method. The distance should be substantial enough to allow movement; however, the distance increased should not be larger than the successful total increased distance along the previous direction.

At the end of the search, five points are chosen around the final candidate point to extract a second-order polynomial in the two reflection coefficient variables:

$$\Delta P = m_1\Delta\Gamma_r + m_2\Delta\Gamma_i + \frac{1}{2}\left(m_{11}(\Delta\Gamma_r)^2 + 2m_{12}(\Delta\Gamma_r)(\Delta\Gamma_i) + m_{22}(\Delta\Gamma_i)^2\right) \qquad (7.11)$$

The maximum of this function is obtained by setting its gradient equal to zero (thus the partial derivatives of ΔP with respect to $\Delta\Gamma_r$ and $\Delta\Gamma_i$ are each set to zero) and insuring that the result gives a positive ΔP. This gives the values of $\Delta\Gamma_r$ and $\Delta\Gamma_i$ providing maximum power. These values can be inserted into equation (7.11) to calculate the value of maximum power.

A description of the implementation of this algorithm and the associated measurement sequence follows. First, the user enters a value for *candidate_point*, the starting real and

imaginary reflection coefficient values for the search. The power at this reflection coefficient is measured, followed by which points a small distance (equal to the value of *neighboring_point_distance*) above and to the right of the candidate point are measured. From the measured power values at these three points, the tangent plane equation at *candidate_point* and the direction of maximum increase for output power (the criterion) is determined. An intuitive sketch of this is shown in Figure 7.2.

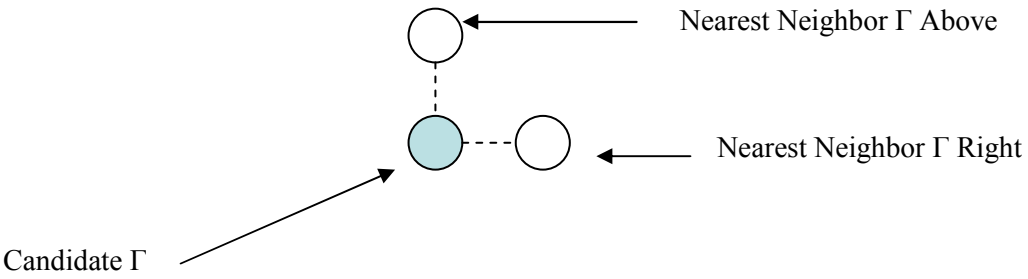


Figure 7.2. Measurements to Extract Tangent Plane Equation and Direction of Steepest Ascent

Following the calculation of the direction of maximum increase, the search proceeds a distance labeled *search_distance* from Candidate 1 in this direction and measures a second candidate point, Candidate 2, as shown in Figure 7.3. The value of output power at this reflection coefficient is compared with the power at Candidate 1. If the power at Candidate 2 is greater than the power at Candidate 1, then the tangent plane and maximum increase direction measurements and calculations are repeated at Candidate 2. If the power at Candidate 2 is not greater than the power at Candidate 1, however, the search distance is decreased and a candidate that is closer to Candidate 1 is measured.

This search process continues until the value of *search_distance* decreases below the *neighboring_point_distance*. When this happens, the search shifts into the end strategy and extracts a second order polynomial approximation of power in terms of the imaginary and real reflection coefficient variations about the final candidate point. To perform this extraction, five measurements are necessary. Each of the five measurements is taken a distance equal to neighboring_point_distance from the candidate. After the equation is extracted, the real and imaginary reflection coefficient values providing maximum output power can be calculated and the value of the function at this point is concluded to be the maximum power value. Figure 7.4 shows an intuitive diagram of the end strategy implementation.

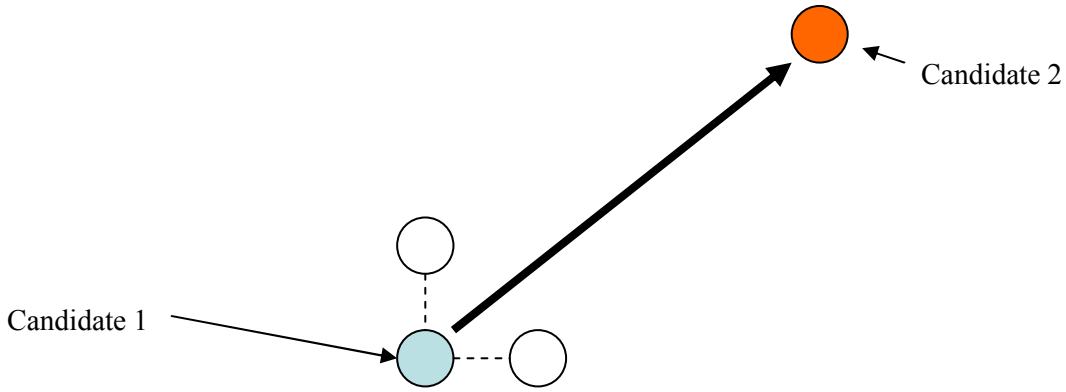


Figure 7.3. Measurement of Power at a New Candidate Point

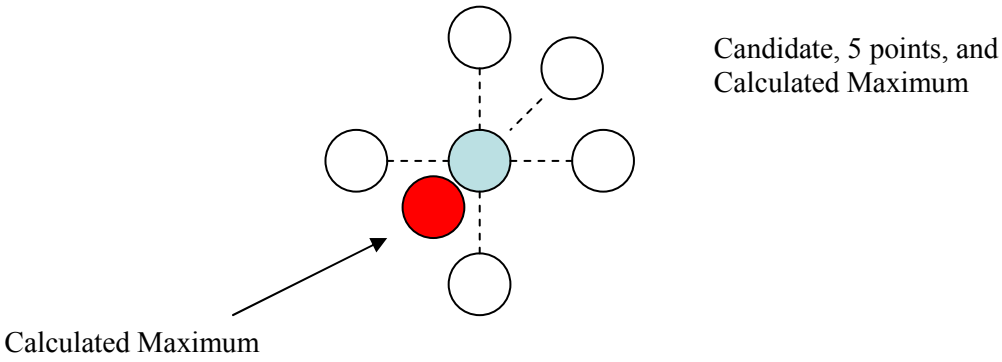


Figure 7.4. End Strategy Implementation

Figure 7.5 shows a flowchart of the algorithm. The search begins with the user entering the initial real and imaginary reflection coefficient values. The program then proceeds through a search of candidate points and measurements. When the *search_distance* decreases below *neighboring_point_distance*, the value of *search_distance* is set to *neighboring_point_distance*. When an increase cannot be obtained with this value of *search_distance*, the end strategy is implemented and the search is completed.

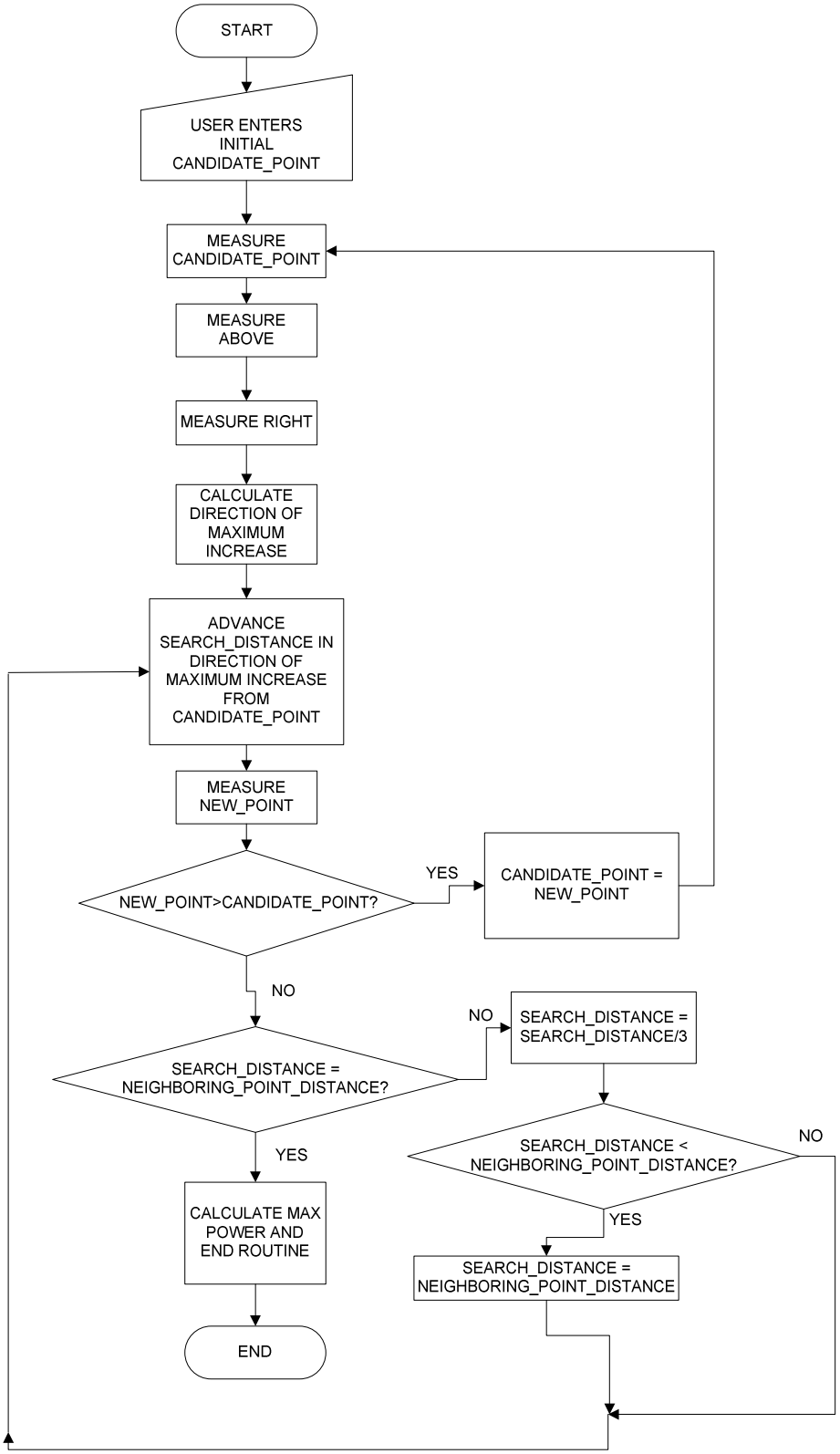


Figure 7.5. Load-Pull Search Algorithm Flowchart

The algorithm has been successfully implemented in MATLAB. A main script, called *maxpowerADSGUI*, receives inputs from the graphical user interface and iterates the functions of the flowchart. It calls other functions to perform the specific operations. A subfunction, called *paADSmodel* for measurement and *paATSmodel* for simulation , requests the simulation or measurement and returns the simulated or measured power value. The subfunction *pilot* calculates the subsequent candidate reflection coefficient based on power values for the candidate point and the nearest neighbors. The function *searchend* is the end routine and finds the second order polynomial describing the output power, calculating the final reflection coefficient and maximum power values.

7.3. Algorithm Implementation in Simulation

The results of the use of this algorithm in simulation are demonstrated in this section. The simulation is controlled by MATLAB, which operates with a given ADS simulation schematic. Figure 7.6 shows the schematic for simulation that should first be constructed in ADS. This schematic is a modified version of a standard load-pull template available in ADS. The model used for simulation is a large-signal model of an 8 x 100 μm GaAs PHEMT extracted by the author to fit IV and S-parameter data. The sequential simulation algorithm is controlled by MATLAB. Before each single-impedance-state power simulation is performed, MATLAB alters the ADS netlist file with the settings for the next simulation. The modified netlist file is then submitted to ADS for simulation. The results are written to an output text file through the command *write_var* in the modified ADS schematic. This text file is then read by MATLAB. This simulation setup allows the algorithmic strength of MATLAB to be utilized while allowing nonlinear transistor models that are compatible with ADS to be simulated using the Harmonic Balance method. The command

X = write_var(“usf_ads_result.txt”,“W”,“”,“\t”,“1”,6, Pout)

writes the calculated values of Pout into the text file “ife_ads_result.txt.” Pout is defined by a series of equations included near the bottom of the schematic.

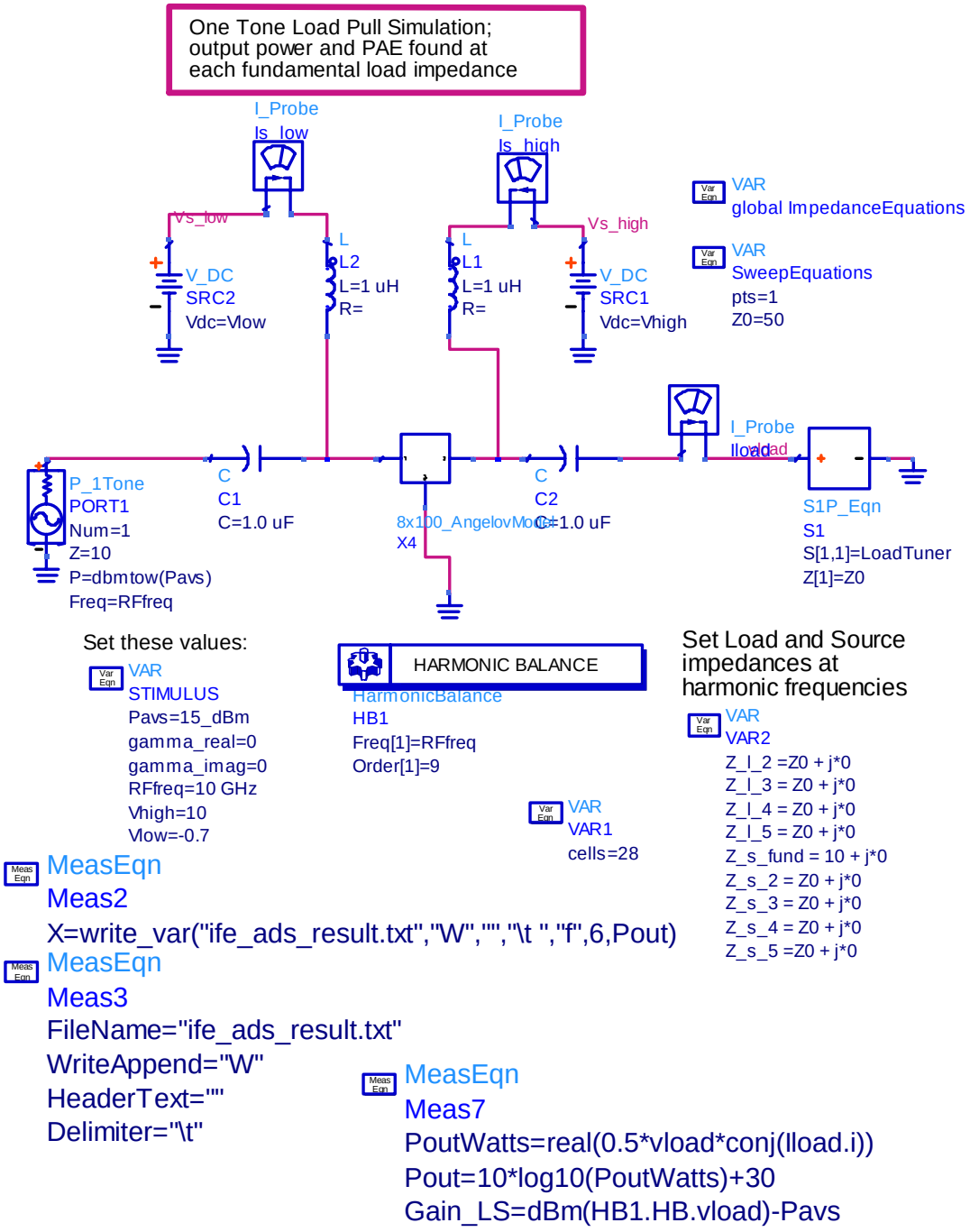


Figure 7.6. Advanced Design System Template for Simulation

In the simulation procedure, MATLAB modifies the ADS simulation netlist file and writes the modified netlist into the file "USF_netlist.log." MATLAB then calls the ADS simulator through the MATLAB command

```
!K:\ADS2004A\bin\hpeesofsim -q USF_netlist.log
```

This command runs the simulator using the netlist that has been written into this file. Using the command in the ADS schematic, ADS writes the Pout results to the file "usf_ads_result.txt." This file is read by MATLAB using the command

```
temp = dlmread('usf_ads_result.txt','\t').
```

The results are assigned to the vector "temp" in MATLAB and can then be manipulated.

The first step that must be performed is that the ADS schematic must be simulated (in ADS). This causes the netlist.log file to describe the schematic that the user desires to simulate. When the MATLAB script for the algorithm is executed, the user is prompted to enter the inputs. Figure 7.7 shows the MATLAB graphical user interface (GUI) for the simulation. This GUI allows the user to enter the frequency, search starting point, *neighboring_point_distance*, bias voltages, and input power. The user can choose to select the *search_distance* value or allow the program to perform this selection (the program averages the horizontal and vertical distances to the edge of the Smith Chart if this is set to "Auto").

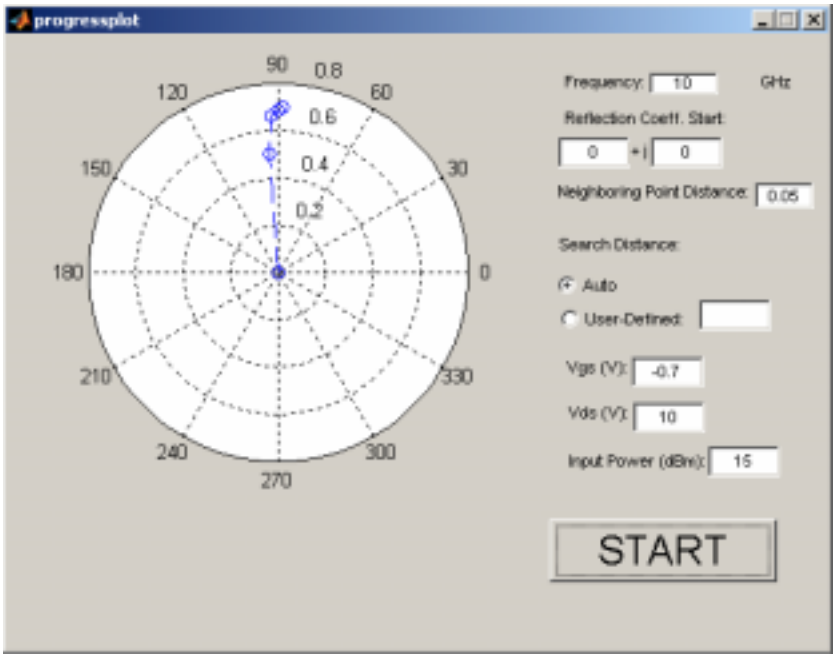
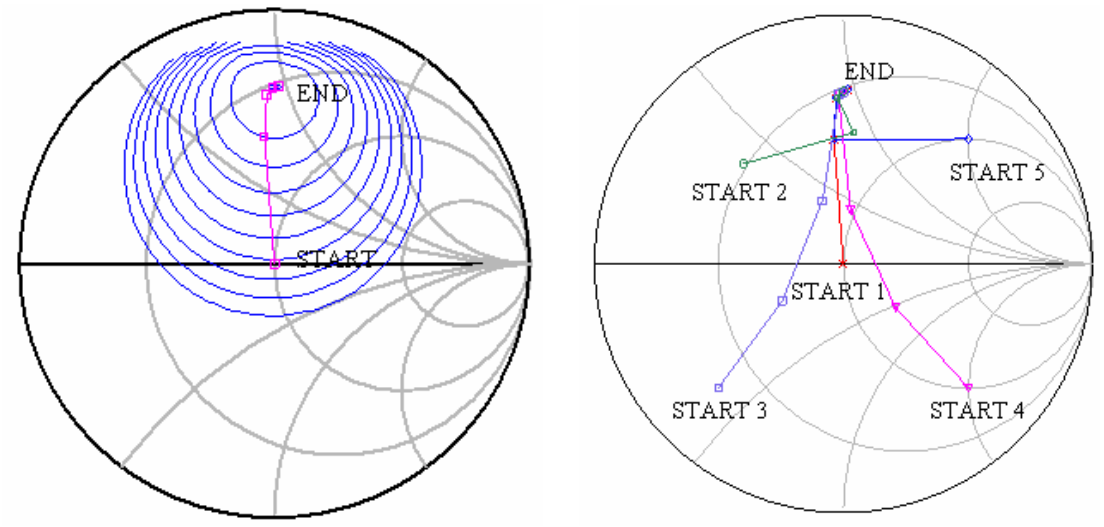


Figure 7.7. MATLAB Graphical User Interface for Load-Pull Search

Results obtained using the sequential simulation have shown excellent correspondence to traditional simultaneous load-pull simulations in ADS. Figure 7.8(a) shows load-pull contours constructed in ADS from a traditional simulation, along with the path followed by the newly implemented sequential steepest-ascent algorithm (candidate points are denoted by squares). The starting load reflection-coefficient state for the steepest-ascent simulation was selected to be the center of the Smith Chart. The new MATLAB/ADS co-simulation found the maximum power for the HEMT model to be 22.72 dBm with measurement of only 17 reflection coefficient states, while a simulation using a traditional ADS load-pull simulation with 400 states found the maximum power to be 22.76 dBm. Figure 7.8(a) shows that both simulations predict virtually identical reflection coefficient states for the maximum output power.

Figure 7.8(b) shows a plot of the candidate points and the search algorithm paths traversed from five different starting points. It can be seen that, for each of these starting points, the algorithm converges to essentially the same reflection coefficient value for the maximum power. Table 7.1 shows the starting reflection coefficient, the final reflection coefficient, the maximum-power reflection coefficient, the maximum power, and the number of simulated states for each starting point. For the results shown, the optimum load resistance and capacitance mean and standard deviation have been found. The mean load resistance is 17.705 Ω with a standard deviation of 0.101 Ω, while the equivalent load capacitance is 3.407 pF with a standard deviation of 0.5738 fF. Excellent agreement has been achieved for the optimal load impedance despite different starting points for the search iterations.



(a) (b)

Figure 7.8. (a) Load-Pull Search Path from MATLAB/ADS Algorithmic Implementation with Output Power Contours Generated from Traditional ADS Load-Pull Simulation, and (b) Search Algorithm Progress for Five Different Starting Points

Table 7.1. MATLAB/ADS Simulation Results for Different Searches

Starting Γ_L	Maximum Output Power Γ_L	Maximum Output Power (dBm)	Number of Sim. Points
0 + j0	-0.0006 + j 0.6892 = 0.689 <90.05°	22.7184	17
0.5 + j0.5	-0.0017 + j 0.6900 = 0.690 <90.14°	22.7178	17
0.5 – j0.5	-0.0006 + j 0.6897 = 0.690 <90.05°	22.7154	19
-0.5 – j 0.5	-0.0006 + j 0.6896 = 0.690 <90.05°	22.7154	17
-0.4 + j 0.4	0.0003 + j 0.6935 = 0.694 <89.98°	22.7143	14

7.4. Algorithm Implementation in Measurement

The algorithm was also used for measurement in conjunction with the Maury ATS 400 system. A .dll library containing native ATS commands allowing the control of this software with MATLAB was provided by Maury Microwave. Small-signal maximum power searches were first performed by measuring an 8 x 100 µm GaAs PHEMT device. From the theory, it is expected that the reflection coefficient providing maximum power under small-signal conditions

will be close to S_{22}*. From S-parameter measurements at nearby bias points, it was found that S_{22} = 0.445<-53.71˚. Using the load-pull search algorithm measurements at an input power of -7 dBm, it was found that the maximum power was obtained at a reflection coefficient of 0.4882<53.02˚, very close in magnitude and phase to S_{22}*.

Having verified the small-signal performance of the device, a power sweep measurement was performed with a 50 ohm load with the intention of examining the compression characteristic of the device. Figure 7.9 shows these power sweep results taken at a frequency of 3.5 GHz. From the power sweep results, it was ascertained that the input power corresponding to 1 dB compression is approximately 14.5 dBm.

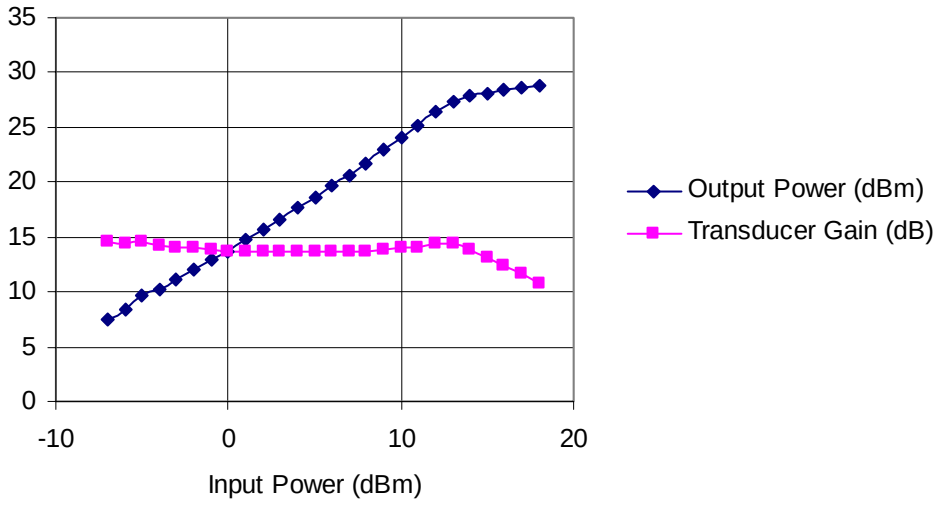


Figure 7.9. 3.5 GHz, 50 Ohm Power Sweep for the 8 x 100 GaAs PHEMT; V_{GS} = -0.7 V, V_{DS} = 10 V

A traditional load-pull measurement was then performed for the 1 dB compression input power of 14.5 dBm using the Maury ATS 400 software. This allowed the reflection coefficient providing maximum power to be found. The results are shown in Figure 7.10. The maximum output power was estimated as 28.26 dBm (transducer gain G_T = 13.76 dB) at Γ_L = 0.2158<96.31˚ = -0.0237 + j0.2145. The MATLAB algorithm was later run with the same conditions and the maximum output power was estimated to be 28.33 dBm at Γ_L = 0.0053 + j0.1944 = 0.1945<88.43˚. A very good correspondence was obtained for the maximum power and

reflection coefficient values found using the algorithm and performing traditional load-pull measurements with the ATS 400 software.

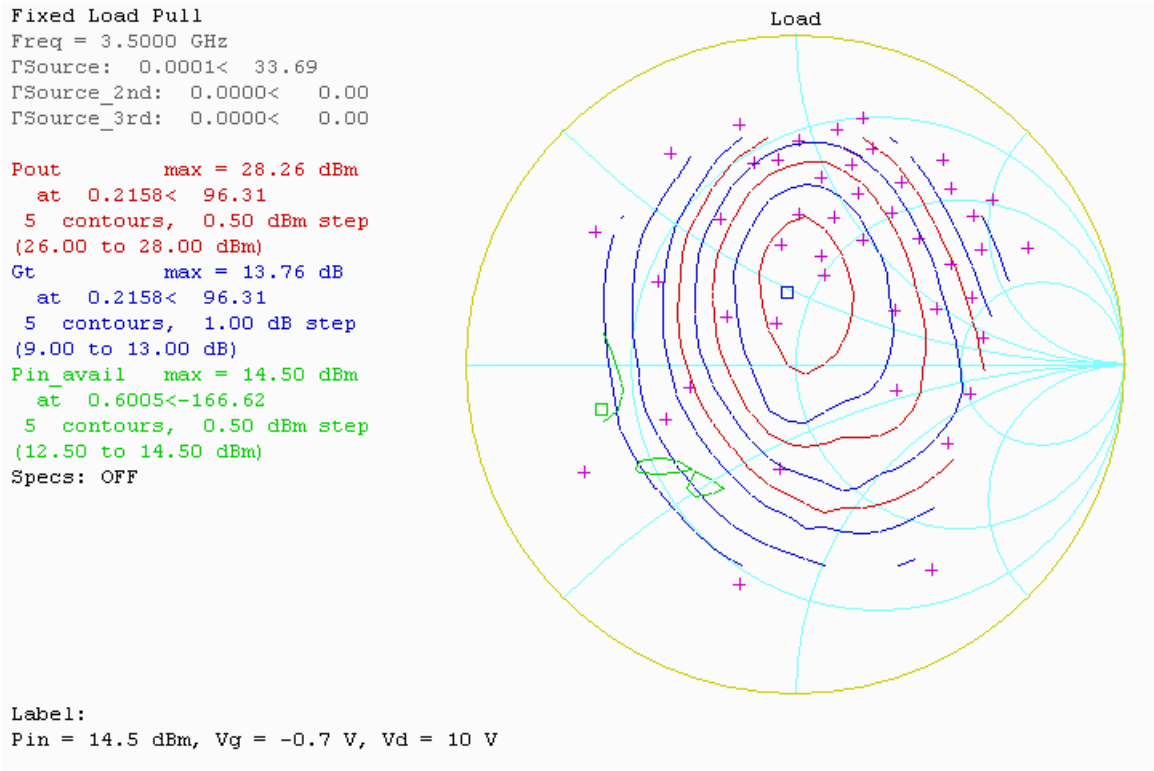


Figure 7.10. Measured 3.5 GHz Load-Pull Results for Pin = 14.5 dBm at V_{GS} = -0.7 V, V_{DS} = 10 V

Based on the good correspondence obtained between algorithm-driven measurements and the traditional load-pull measurements, a series of maximum power searches was performed with the algorithm at different input power values. Table 7.2 shows the search algorithm results for the different input power values.

Table 7.3 shows the P_{in} = 14.5 dBm (1 dB compression) search results for the use of different starting impedances. The mean values and standard deviations of the load resistance and capacitance providing optimum power was calculated from these results. The mean resistance was found to be 44.283 Ω, with a standard deviation of 1.443 Ω. The capacitance was found to have a mean value of -679.8 fF, with a standard deviation of 17 fF. The mean power value was found to be 28.311 dBm, with a standard deviation of 0.011 dBm. All four maximum

power values are within 0.03 dBm of each other. This experiment show good agreement between maximum power results obtained from different starting points.

Table 7.2. Search Algorithm Measurement Results for Different Input Power Values with a Starting Reflection Coefficient of 0 + j0

Pin (dBm)	Maximum Output Power Γ_L	Maximum Output Power(dBm)	Number of Meas. Points
-7	0.2937+j0.3900 = 0.488<53.0˚	9.9242	24
0	0.3378+j0.3908 = 0.517<49.2˚	15.6327	18
5	0.3103+jj0.4343 = 0.534<54.5˚	20.3879	21
10	0.1884+j0.3936 = 0.436<64.4˚	25.8117	27
12	0.0757+j0.2900 = 0.300<75.4˚	27.4354	18
13	0.0228+j0.2817 = 0.283<85.4˚	27.8654	18
14	-0.0345+j0.1941 = 0.197<101˚	28.1543	21
14.5(1 dB comp.)	0.0053+j0.1944 = 0.194<88.4˚	28.3264	24
15.5(2 dB comp.)	0.0246+j0.2315 = 0.233<83.9˚	28.8281	21
16.7(3 dB comp.)	0.0209+j0.1992 = 0.200<84.0˚	28.8479	15

Table 7.3. Measurement Results for Different Starting Reflection Coefficients at P_{in} = 14.5 dBm

Starting Γ_L	Maximum Output Power Γ_L	Maximum Output Power (dBm)	Number of Meas. Points
0 + j0	0.0160 + j 0.2322 = 0.233 <86.1˚	28.2962	18
0.5 + j0.5	0.0004 + j 0.2459 = 0.246 <89.9˚	28.3132	14
0.5 – j0.5	-0.0091+j 0.2603 = 0.261 <92.0˚	28.3220	23
-0.6 – j 0.5	-0.0033 + j0.2551 = 0.256 <90.7˚	28.3134	23

7.5. Power-Swept Load-Pull: Measured Versus Simulated Comparison

As shown in Table 7.2, the reflection coefficient providing maximum output power migrates as the device moves from small-signal to large-signal operation. As the input power is increased, a plot can be created of the maximum-power input impedance at different power levels. This provides a collection of measured data that can be used as another means of verifying the behavior of a nonlinear transistor model.

To compare with the measured data shown in Table 7.2, simulations were performed for these input power values using an Angelov model extracted by the author using pulsed IV, S-parameter, power sweep, and load-pull data. Figure 7.11 shows the measured and simulated migration of the maximum-power load reflection coefficient with increasing input power. It appears that the model predicts the migration of the maximum-power reflection coefficient with notable accuracy.

This type of comparison is insightful because it shows the performance of the model at low power, high power, and medium power conditions. The use of load pull at each of these power conditions lends insight into the signal swing prediction accuracy at each of the power settings.

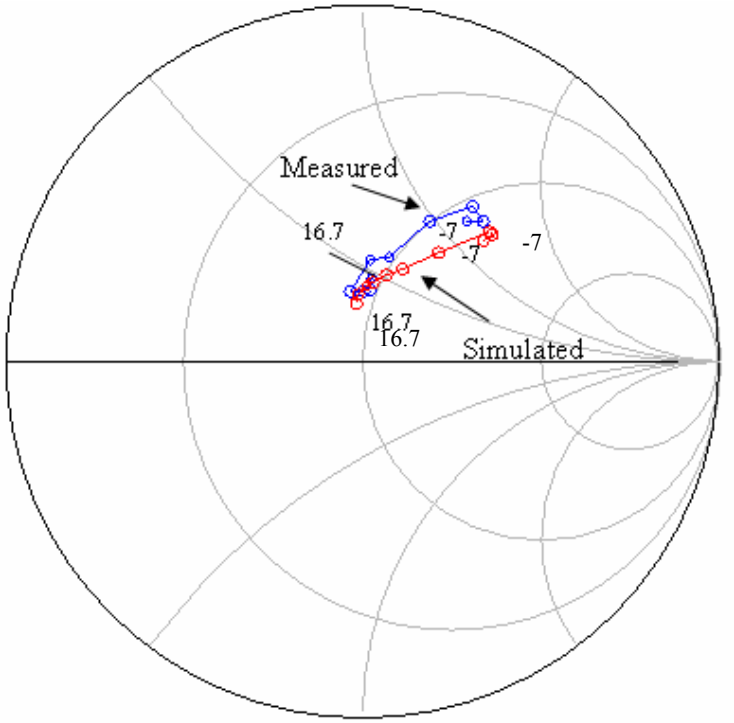


Figure 7.11. Measured (Blue) and Simulated (Red) Impedance States for Maximum Output Power at Varying Input Power Levels: -7, 0, 5, 10, 12, 13, 14, 14.5, 15.5, and 16.7 dBm

To decrease the time necessary to perform the power-swept load-pull measurement, a MATLAB script has been developed to run the maximum-power search algorithm more efficiently. A starting impedance state is specified for the first search (this would be the -7 dBm case in the above example). After the maximum-power impedence state is ascertained for this power setting, the search distance is reduced to the neighboring-point distance and the starting

point is set to the end-point of the previous search. In most cases, this decreases the number of measurements required to find the maximum-power impedance state for the next input power. The reason for the success of this method is that the maximum-power impedance for each subsequent state is in somewhat close proximity to its predecessor. Using a small search distance is optimal for such conditions. The script has also been designed to plot the migration of the maximum-power impedance with input power.

It can be noted from the data of Table 7.1 that the maximum number of measurements performed occurred in the first search; it appears a sizeable reduction in measurements was accomplished by using the endpoint of each measurement as the starting point for the subsequent search. Six measurements is the minimum number of measurements that can be performed in any iteration of the search algorithm, and the search was accomplished using the minimum six measurements four times in the ten searches. An additional three searches were accomplished with only nine measurements. It appears that as a larger migration is necessary on the Smith Chart from one setting to the next, more measurements are required.

Table 7.4. Starting Point, Ending Point, and Number of Measurements for Each Search in the Maximum-Power Impedance Migration Measurement

Input Power (dBm)	Starting Γ	Ending Γ	Max Pout (dBm)	# Meas
-7	0+j0	0.3090 + j0.5039	8.8443	17
0	0.3090+j0.5039	0.3104+j0.5040	15.8737	6
5	0.3104+j0.5040	0.2969+j0.4924	20.9064	6
10	0.2969+j0.4924	0.1578+j0.3906	25.2306	15
12	0.1578+j0.3906	0.0757+j0.3423	26.4747	12
13	0.0757+j0.3423	0.0366+j0.3192	27.0064	9
14	0.0366+j0.3192	0.0028+j0.2972	27.4824	9
14.5	0.0028+j0.2972	-0.0115+j0.2859	27.6977	6
15.5	-0.0115+j0.2859	-0.0316+j0.2648	28.0779	9
16.7	-0.0316+j0.2648	-0.0290+j0.2378	28.3899	6

The peak search algorithm appears to have a high potential to decrease both simulation and measurement time, as well as allowing additional methods of large-signal model verification.

7.6 Chapter Summary

A new algorithm for use in load-pull search measurements has been proposed and demonstrated. This algorithm allows for a reduced number of measurements in ascertaining the reflection coefficient providing a maximum value for a given criterion, such as output power or power-added efficiency. The algorithm has been coded in MATLAB, and MATLAB has been configured to control both simulations, using Agilent Advanced Design System, and measurements, using the Maury Automated Tuner System. The results have been seen to match results obtained through traditional load-pull simulations and measurements. The example of a power-swept load-pull measured-to-simulated comparison has been used to illustrate how the peak search algorithm can facilitate certain types of measurements and simulations for nonlinear model validation.

CHAPTER 8: THERMAL RESISTANCE MEASUREMENT FOR DEVICES WITH TRAPPING EFFECTS

The measurement of thermal resistance in devices with significant trapping effects has been difficult to perform to date due to the dependence of trapping effects on both the device terminal voltages and temperature. While pulsed IV measurement techniques have been successfully used for devices with very small amounts of trap effects, such as Si MOSFETs, the application of these techniques to wide bandgap devices, such as GaN HEMTs and MESFETs, has been difficult due to the large amounts of trapping effects. The advent of such devices for widespread use in communication system applications has caused a demand for the development of a simple electrical technique for thermal resistance measurement. In this paper, it is attempted to adapt the previous electrical method proposed for Si MOSFETs for use on a GaN HEMT based on a knowledge of device trapping physics. This method, however, is shown to be based on an incorrect assumption through an additional thermal resistance measurement of the same GaN HEMT using infrared techniques.

8.1. A Strategy for Avoiding Traps in the Thermal Resistance Measurement

Electrical measurement techniques have been proposed that have shown reasonable accuracy for the thermal resistance measurement of some transistors [6], [7], [56]. These methods use only pulsed IV and static IV measurements at varying temperatures to perform the measurements; no advanced optical techniques, such as spectroscopy or infrared imaging, are required. However, the applicability of some of these methods to devices with significant surface or substrate trapping effects, such as GaN HEMTs and GaAs MESFETs, has been limited due to the fact that the thermal effects cannot be easily distinguished from the trap effects. The trapping effects tend to "cloud" the thermal effects so that a clear visualization of the temperature effects on the IV curves is not possible; rather, the combined effect is observed. It is hypothesized that knowledge of some basic device physics may present a solution to this problem, allowing the pulsed IV method of [7] to be extended to measure thermal resistance in devices with either

surface traps, substrate traps, or both types of traps. The thermal resistance measurement of a GaN high electron mobility transistor (HEMT) possessing very significant trapping effects is attempted.

As mentioned in Chapter 3, the device channel temperature is based on the power dissipated in the channel of the FET or HEMT (P_D) and the ambient temperature (T_A). The average thermal resistance, R_{th}, is a property of the device that relates the channel temperature T_C to the dissipated power and the ambient temperature:

$$T_C = R_{th} P_D + T_A \qquad (8.1)$$

For measurement of thermal resistance in low-trapping devices, pulsed IV curves can be matched for different quiescent bias values (yielding different values of P_D) by adjusting the ambient temperature. When the curves match, the channel temperatures can be assumed to be equal, and the channel temperatures of the two curves can be equated, allowing solution for the thermal resistance. This is the method demonstrated in [7] and which has been found to achieve results that compare quite reasonably to those found by the gate-diode method used in [57] for a Si LDMOSFET device and to infrared imaging results.

It may be possible, under some conditions, to avoid the effects of surface and substrate traps in pulsed IV measurement through an appropriate choice of the quiescent bias points. IV curves can then be matched by adjusting the chuck temperature using the method of [7] to measure the channel temperature and calculate the thermal resistance. The results seem to be reasonable. However, following the experimentation of this chapter, it can be concluded that the method only appears to work under certain conditions. This method may provide a means to electrically extract the thermal resistance for some devices containing significant amounts of traps.

Recall from Chapter 3 that there are two basic types of trapping effects: surface traps and substrate traps. The substrate traps are affected primarily by the drain-source voltage, while the surface traps are affected primarily by the drain-gate voltage [36], [38]. As previously mentioned, the electron capture (or hole emission) effect is a fast effect, with a time constant of nanoseconds in many cases, while the electron emission (or hole capture) effect is a slow effect, with a time constant often on the order of milliseconds. In Chapter 4, some rules were set up regarding pulses in drain-source voltage and drain-gate voltage. They are summarized as follows. The rules presented by Siriex *et al.* for trap dependence based on the drain quiescent voltage V_{dsQ} and the "pulse-to" drain voltage V_{dsp} [38] are as follows:

Case 1: $V_{dsp} < V_{dsQ}$. Electrons begin to be emitted from substrate traps on pulse application. The emission time constant is significantly longer than the pulse length in short-pulse IV, and the trap state is dependent on V_{dsQ}.

Case 2: $V_{dsp} > V_{dsQ}$. Electrons are captured by substrate traps on application of the pulse. The capture process time constant may be shorter than the pulse length; if this is true, the trap state at the measurement time is dependent on V_{dsP}.

The pulsing conditions regarding surface states, given in Chapter 4 and in [39] are as follows:

Case 1: $V_{dgp} < V_{dgQ}$. Holes begin to be captured (or electrons begin to be emitted) by surface traps on the application of a pulse. The emission time constant is sufficiently longer than the pulse length in short-pulse IV, and the trap state is dependent on V_{dgQ}.

Case 2: $V_{dgp} > V_{dgQ}$. Holes are emitted (or electrons are captured) by surface traps on application of the pulse. The capture time constant may be shorter than the pulse length; if this is true, the trap state at the measurement time is dependent on V_{gsp}.

These results are summarized in Figure 8.1, reprinted from Figure 4.2 for convenience. The dashed line illustrates an approximate division between fast effects and slow effects.

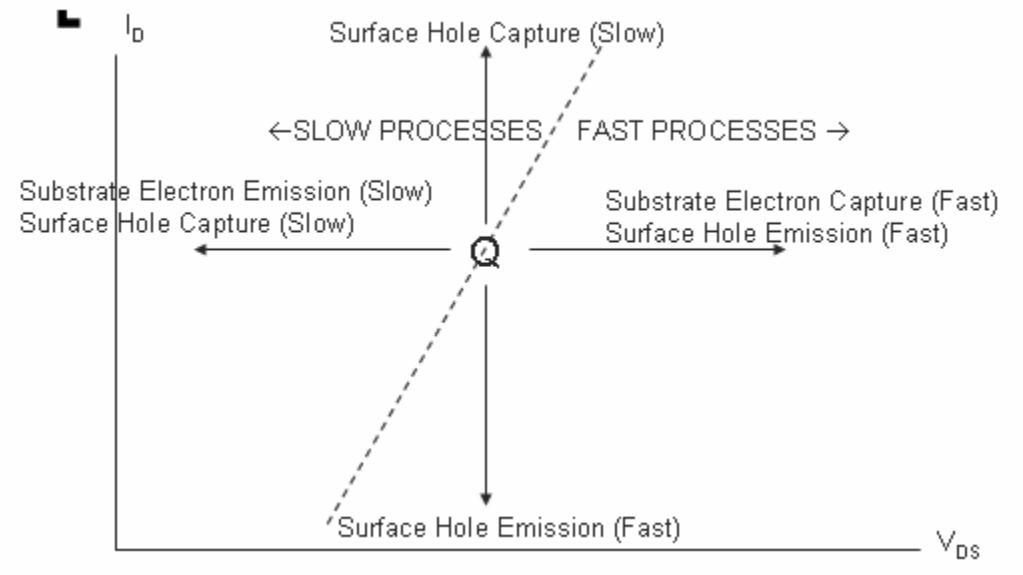


Figure 8.1. Trapping Effects Based on Pulsing from a Quiescent Bias Point "Q"

How does this allow determination of the necessary bias conditions for the pulsed IV measurement of thermal resistance? If pulsing is performed from a smaller V_{ds} to a larger V_{ds} and from a smaller V_{dg} to a larger V_{dg} , the predominant effect of traps on the IV curves will be from the relatively fast electron capture process. If the capture process is fast enough, the trapping state will be dependent on the measurement point, not the quiescent point. If the capture process time constant is larger than the pulse length, however, the number of filled trap states will be dependent on the quiescent bias point. Thus the ability to compare the IV curves to ascertain thermal resistance is dependent on the trap time constant being smaller than the pulse length. This assumption of a short capture time constant was made in this experiment; however, it appears to not be a valid assumption for the devices studied.

8.2. Pulsed IV Thermal Resistance Measurement Attempt for a GaN HEMT

In the experiment, a comparison of IV results similar to that in [7] was performed. However, a couple of restrictions were added to the measurement procedure to better ensure that the trap effects are approximately the same in both measurements. First, the quiescent gate voltage in both measurements was chosen so that gate voltage would become more negative during the pulse, decreasing V_{dg} and allowing the faster surface trap process of hole emission to occur. This minimizes differences in the two sets of measured IV data due to surface traps, as the behavior of surface states is dependent on the drain-gate electric field. Second, only a region of the IV plane in which $V_{dsp} > V_{dsQ1}$, V_{dsQ2} and $V_{dgp} > V_{dgQ}$ (the two quiescent drain voltages) was used for the curve comparison. This allows electron capture (a fast effect) to be the prevalent process for the substrate traps in the region of comparison.

Figure 8.2 shows static and pulsed (V_{gsQ} = 0 V, V_{dsQ} = 0 V) IV curves for the GaN HEMT, measured using a Dynamic i(V) Analyzer model D225, manufactured by Accent Optical Technologies. A significant current collapse can be observed in the static IV knee region, indicating the presence of significant trapping effects in this device. Also, the static IV curves are negatively sloped in the high-power region, indicating the presence of self-heating effects.

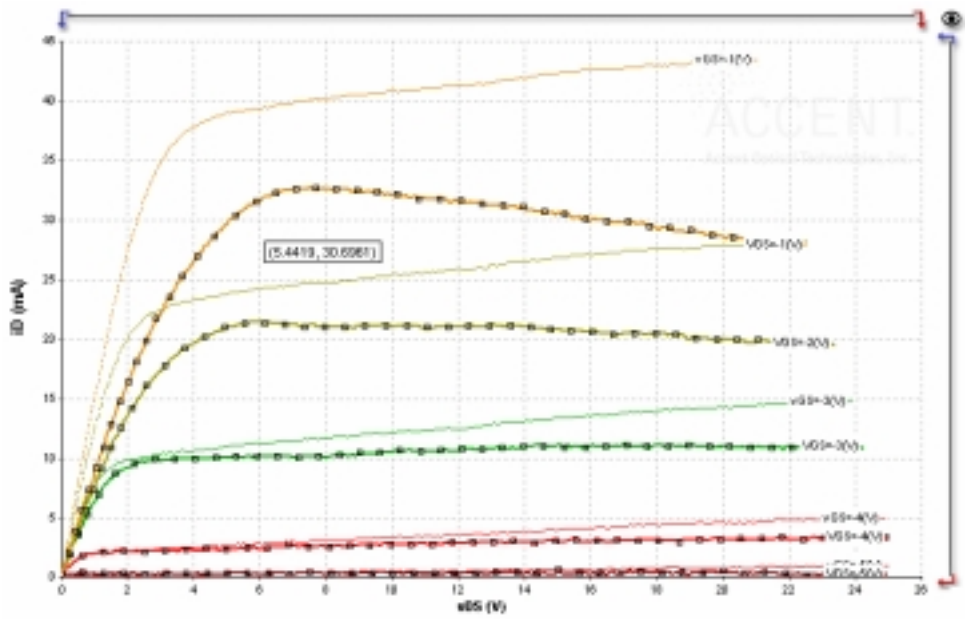


Figure 8.2. Static (Darker Curves) and Pulsed (V_{GSQ} = 0 V, V_{DSQ} = 0 V) (Lighter Curves) IV Curves for the GaN HEMT

Two thermal resistance measurements were performed using different quiescent gate voltages. In the first experiment, the quiescent bias points used for measurement were (A) V_{gsQ} = -1 V, V_{dsQ} = 4 V and (B) V_{gsQ} = -1 V, V_{dsQ} = 0 V. For the quiescent bias point A, the power dissipated was P_D = 132 mW. For quiescent bias point B, the power dissipated was approximately 0 W. The measured curves for the two quiescent points for an ambient temperature T_A = 40 ˚C are shown in Figure 8.3. The region of examination is shown by a dashed box. Inside this box, the primary effects should be due to temperature, as proposed in the previous section, because both the drain-source voltages and drain-gate voltages within the box are significantly larger than those of both quiescent bias points.

The ambient temperature was incremented and the measurement repeated for quiescent point B until a match was achieved for an ambient temperature of T_A = 68 ˚C. The matched curves are shown in Figure 8.4.

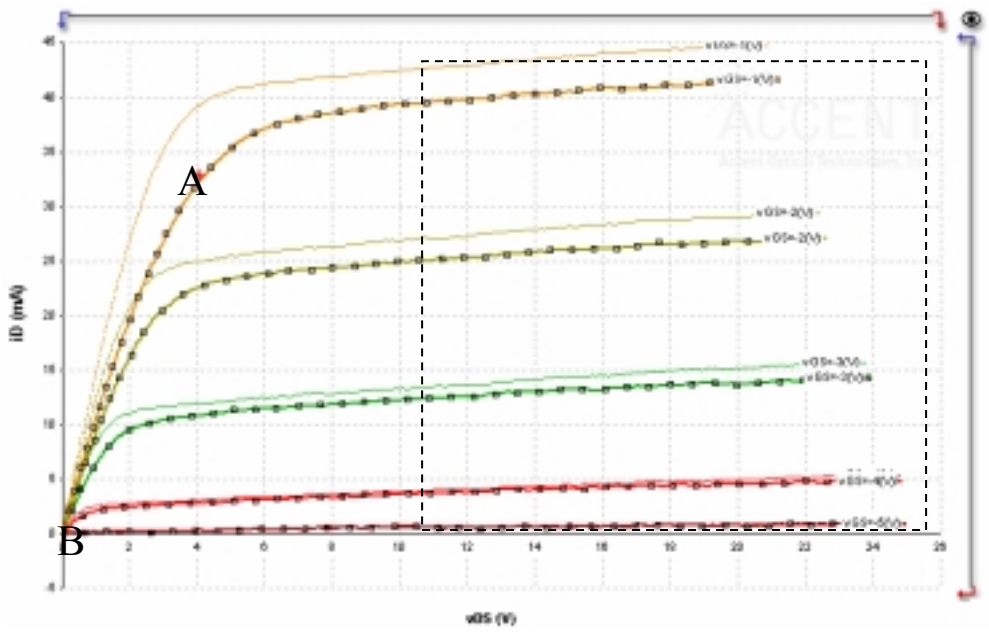


Figure 8.3. Pulsed IV Curves for Quiescent Points A (Darker Curves) and B (Lighter Curves) at T_A = 40 ˚C

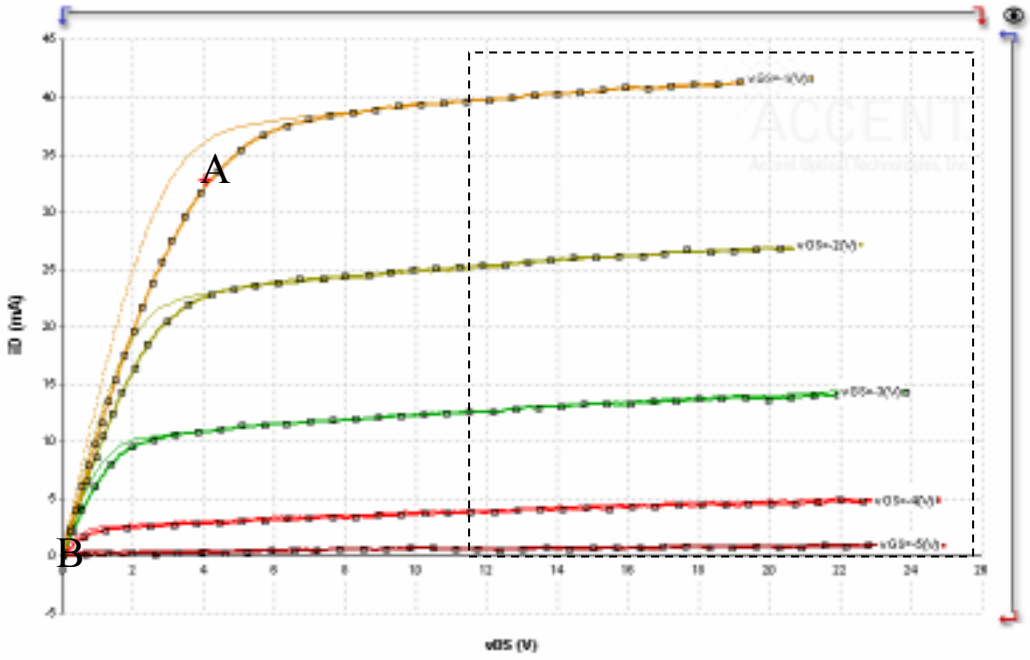


Figure 8.4. Curves for Quiescent Bias Point A at T_A = 40 ˚C (Darker Curves) and Quiescent Bias Point B at T_A = 68 ˚C (Lighter Curves)

The thermal resistance is calculated by equating the channel temperatures, as calculated by equation (8.1), for the two measurements (the power dissipated at quiescent bias point A was P_D = 132 mW):

$$R_{th}P_{D1} + T_{A1} = R_{th}P_{D2} + T_{A2}$$

$$0 + 68 = 0.132R_{th} + 40$$

$$R_{th} = 212 \ ^\circ\text{C/W}$$

A similar experiment was performed for two more quiescent bias points: (C) V_{gsQ} = -2 V, V_{dsQ} = 4 V and (D) V_{gsQ} = -2 V, V_{dsQ} = 0 V. A comparison of both sets of pulsed IV curves at T_A = 40 ˚C is given in Figure 8.5. The curves for quiescent point D were measured for different increments of temperature until a match in the desired region of comparison was obtained for an ambient temperature T_A = 64 ˚C. The matched curves are shown in Figure 8.6.

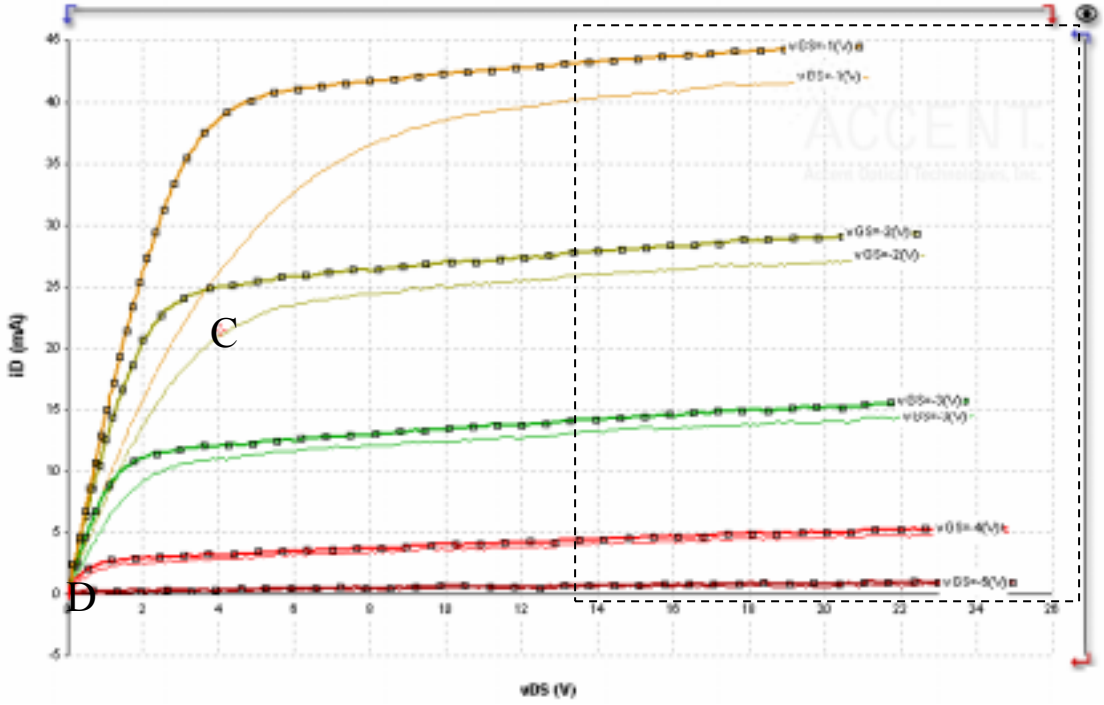


Figure 8.5. Curves for Quiescent Bias Points C and D at T_A = 40 ˚C; the Region of Examination is Roughly the Region in the Dashed Box

The equation to calculate thermal resistance is solved:

$$R_{th}P_{D1} + T_{A1} = R_{th2}P_{D2} + T_{A2}$$

$$0 + 64 = 0.086\,R_{th} + 40$$

$$R_{th} = 279\ ^{\circ}\text{C/W}$$

From these measurements, the average thermal resistance value measured is approximately 246 ˚C/W.

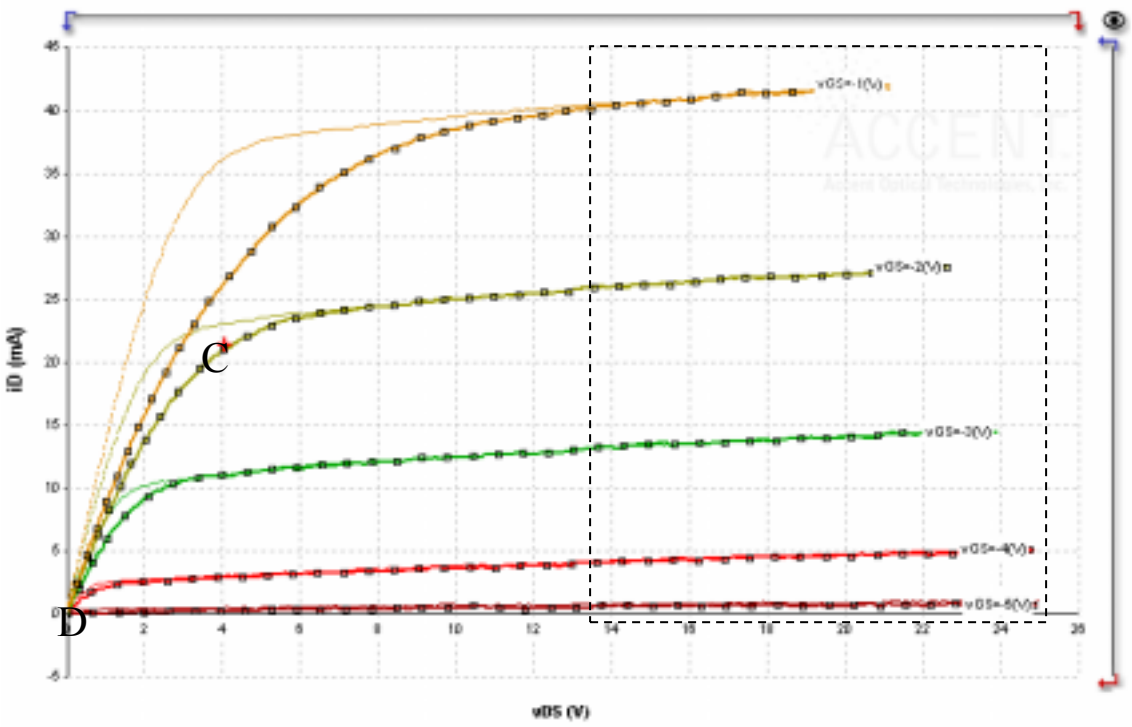


Figure 8.6. Curves for Quiescent Bias Point C at T_A = 40 ˚C (Darker Lines) and Quiescent Bias Point D at T_A = 68 ˚C (Lighter Lines)

While this method appears reasonably sound, Figure 8.7 shows pulsed IV measurements taken from a gate quiescent bias voltage at approximately the threshold with differing drain quiescent bias voltages: (A) V_{gsQ} = -5 V, V_{dsQ} = 0 V and (B) V_{gsQ} = -5 V, V_{dsQ} = 5 V. Unlike the results shown by Siriex [38], it appears that the IV curves may not match exactly for very large measured values of V_{DS}, despite the fact that the device possesses approximately the same channel temperature for measurements from quiescent bias points (A) and (B).

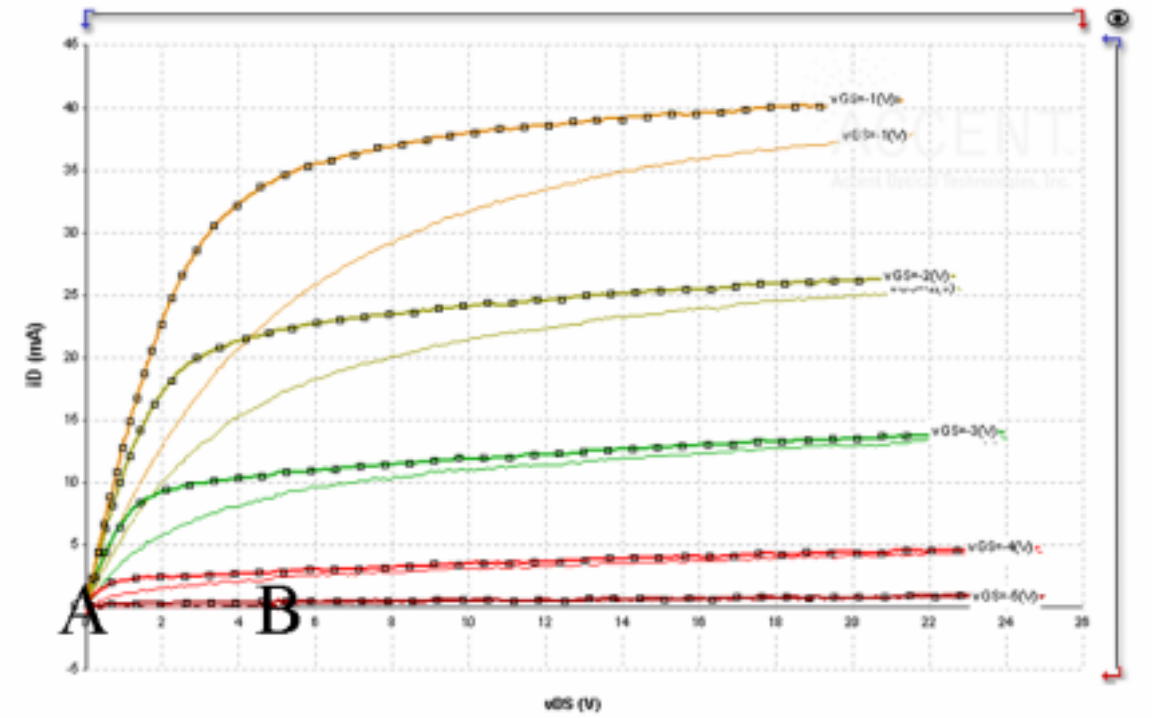


Figure 8.7. Pulsed IV for GaN HEMT Corresponding to Quiescent Bias Points A (Vgsq = -5 V, Vds = 0 V, Darker Curves) and B (Vgsq = -5 V, Vdsq = 5 V, Lighter Curves)

Why do the IV curves not match for large values of V_{DS}? The reason is not expected to be thermal effects, as the measurements were performed at the same ambient temperature and both were performed from quiescent bias points of zero power dissipation, so no self-heating is present in either measurement. The reason for the difference in IV curves must be traced to a trap effect that is dependent on V_{dsq}. From these results, it appears that the electron capture time constant is larger than the pulse length of the pulsed IV measurement. Despite the fact that, for large values of V_{dsm}, the pulses are coming from significantly lower drain voltages in both sets of curves, it appears that the trap effects are dependent on the quiescent drain voltages. The number of captured electrons in trap states (and hence the trap occupancy) seems to be dependent on the quiescent drain voltage. For larger quiescent drain voltages, the reasoning of Chapter 4 leads to the thought that more electrons would be captured by the substrate traps. This creates a depletion region near the bottom of the substrate, an effect known as "backgating", lowering the current values. The lower IV curves correspond to the higher quiescent drain voltage. Kwok [58] states that the backgate effect results in the multiplication of the FET I_{DS} equation by a factor

$$\frac{1}{1+K_1\left(\frac{Z}{L}\right)q\mu_n N_D V_{DS}}.$$

If the capture time constant is sufficiently fast, as in the case examined by Siriex [38], the backgating is the same for both measurements because the measured voltage $V_{DS} = V_{dsm}$ is used to determine the backgating. However, if the electron capture time constant is longer than the pulse length, then a partial dependence on V_{dsQ} must be included in this expression, and a decrease of the current with increasing quiescent drain voltage due to increased backgating is expected. To allow the capture effect to be completed, it may be possible to lengthen the pulse used for the measurement. However, the implications of this should be examined with thorough experimentation to ensure that unwanted self-heating effects are not incurred due to the longer pulses.

8.3. Infrared Measurement of GaN HEMT Thermal Resistance

An infrared measurement of the device channel temperature during steady-state bias of the device allows calculation of the thermal resistance. This provides an independent method for verifying electrical measurements. Measurement of thermal resistance for the same GaN HEMT demonstrated in the previous section was performed by the author at Quantum Focus Instruments (QFI) in Vista, California with the assistance of company technicians. The InfraScope II was used to perform the infrared measurements [30]. To perform these measurements, a standardized process is used, as explained by McDonald and Albright [59]. A pixel-by-pixel measurement of the device emissivity is taken without a bias applied to the device. The device should take on the temperature of its ambient surroundings during this measurement. Using these results as an emissivity calibration, the emissivity of the device during an applied bias is then measured. The emissivity changes from the initial calibration measurement due to the power dissipated in the channel. A pixel temperature map results from this emissivity measurement, allowing calculation of the maximum channel temperature. This temperature is then used, along with the electrical power dissipation during the measurement, to calculate the thermal resistance using equation (8.1). While the maximum pixel temperature was used to calculate the thermal resistance, a method for finding the temperature at the center of the maximum-temperature pixel is provided in Appendix A.

Figure 8.8 shows the temperature map of one of the infrared measurements performed on the GaN HEMT. The map shows temperatures ranging from 39.7 ˚C to 68.5 ˚C. The temperature of the baseplate (ambient temperature) was set to 40 ˚C for these measurements.

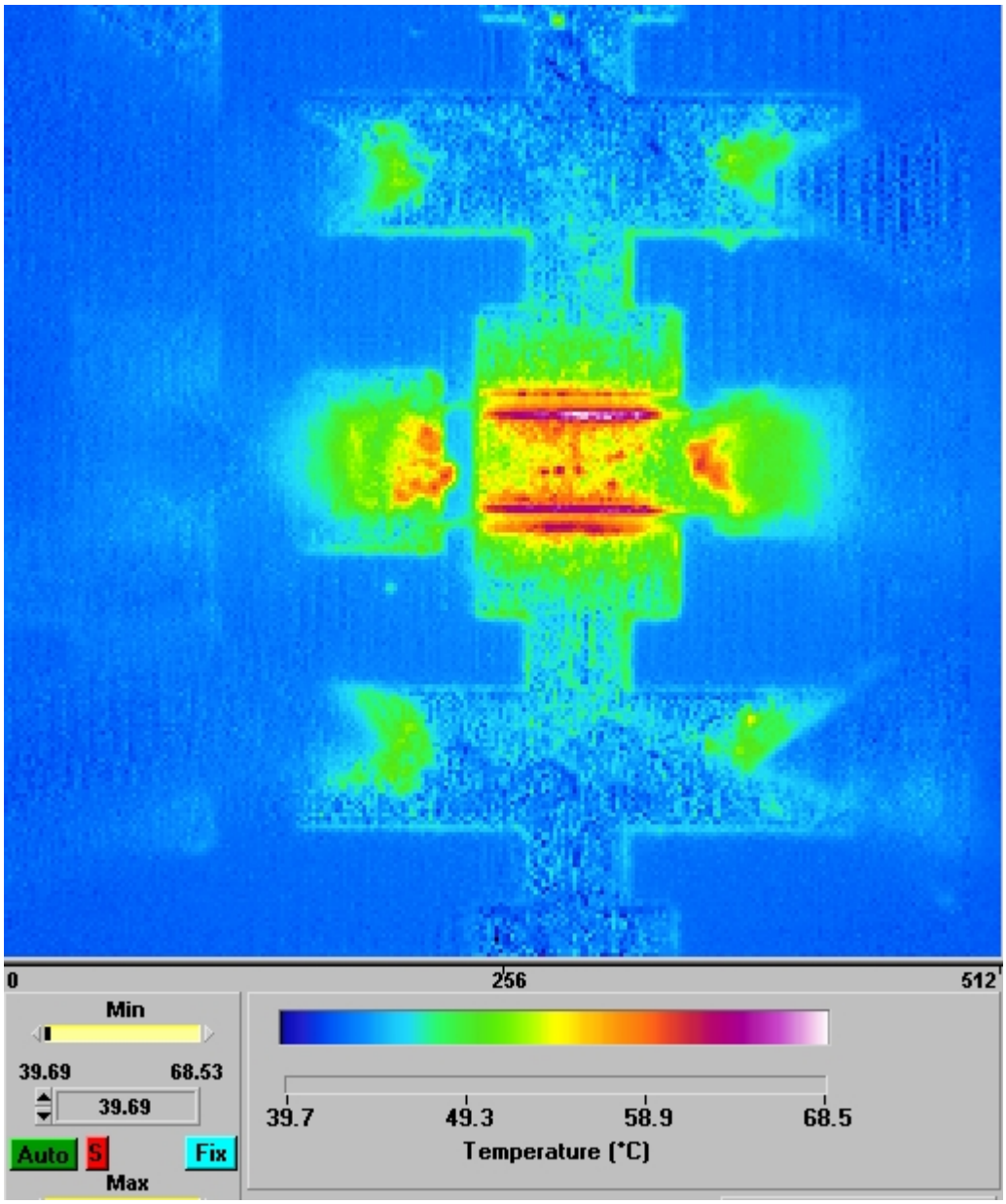


Figure 8.8. GaN HEMT Infrared Measurement Temperature Map Using Quantum Focus InfraScope Software [30]

Measurements were performed for three different gate and drain bias combinations at each of three power dissipation levels (0.2, 0.3, and 0.4 Watts). The thermal resistance measurement results are shown in Table 8.1. Over this total of nine measurements, the mean value of thermal resistance measured was 63.5 ˚C/W and the standard deviation was 6.77 ˚C/W. It can be noted from the data that the thermal resistance seems to increase for increasing power dissipation. This seems to be consistent with the theory, as thermal conductivity generally decreases with increasing temperature [21] due to the increased number of collisions between electrons at higher temperatures and the resultant decrease in conduction of heat through the material.

Table 8.1. Infrared Thermal Resistance Measurement Results

V_{GS} (V)	V_{DS} (V)	Power Dissipated (W)	Thermal Resistance (˚C/W)
-2	8	0.2	51.1
-2.7	12	0.2	56.2
-3.2	18	0.2	65.9
-1.8	12	0.3	66.4
-2.4	16	0.3	59.8
-3	22	0.3	63.4
-1.8	16	0.4	71.3
-2.2	20	0.4	71.3
-2.5	24	0.4	66.43
		Mean	63.5
		Standard Dev.	6.77

The thermal resistance of 63.5 ˚C/W from the infrared measurements is approximately one-fourth of that measured during electrical attempts. It appears that the quiescent-dependent backgating has posed as a thermal effect in the electrical experiments of the previous sections. This conclusion is further confirmed by the bias-dependent model extraction of the next chapter.

8.4. Chapter Summary

An electrical technique for measurement of thermal resistance in some devices with significant trapping effects has been devised. This technique can be used in devices where the

time constant of the electron capture process is smaller than the pulse length of the pulsed IV measurements used. The measurement was attempted for a GaN HEMT with significant trapping effects. A pulsed IV comparison, however, between results from two quiescent bias points of zero power dissipation shows significant variation in the level of the IV curves due to quiescent drain voltage. This seems to indicate that the time constant of the electron capture effect is not short enough for a valid measurement of thermal resistance. This conclusion seems to be supported by infrared measurement results, which give a result approximately one-fourth the size of the thermal resistance obtained from the pulsed IV measurements. The thermal resistance value extracted from the infrared measurement seems to be better for prediction of device behavior in the GaN HEMT, as shown using a quiescent-bias dependent Angelov model in the next chapter.

CHAPTER 9: A QUIESCENT-BIAS DEPENDENT ANGELOV MODEL FOR DEVICES WITH TRAPPING

In Chapter 4, it was discussed that trapping effects are heavily dependent on the operating point. This chapter demonstrates the modification of the Angelov/Chalmers nonlinear model to include three parameters providing dependence on the quiescent gate and drain voltages. These parameters can be extracted from pulsed IV measurements at different quiescent bias values of zero power dissipation. The temperature coefficients can be extracted from pulsed IV measurements taken from quiescent bias points of nonzero power dissipation. After quiescent bias and temperature dependence have been extracted, the thermal resistance can be extracted from a pulsed IV measurement taken from a quiescent bias point of nonzero power dissipation. This chapter demonstrates a modified Angelov model parameter extraction for a GaN HEMT device with significant trapping effects; furthermore, the thermal resistance estimation is found to correspond with independent infrared imaging thermal resistance measurements.

9.1. Modifications of the Angelov Current Equation for Trap-Related Quiescent Dependence

As discussed previously, surface trap effects are very sensitive to the quiescent drain-gate voltage, while substrate trap effects are sensitive to quiescent drain voltage. Figures 4.4 and 4.5 show that the IV characteristics of the GaN HEMT used for demonstration in Chapter 4 have a significant dependence on both gate and drain quiescent voltages. A modification of the Angelov model [12] drain current equation to allow appropriate quiescent voltage dependence is suggested and implemented here.

The Angelov Model for Drain-Source Current is as follows [31]:

$$Ids = IPK0 \times (1 + \tanh(\psi))\tanh(\alpha \times Vds)(1 + LAMBDA \times Vds + LSB0 \times \exp(Vdg - VTR) \quad (9.1)$$

This equation describes the current, for a given gate voltage, as a hyperbolic tangent of Vds. This mathematical model of the drain current is accurate for many devices.

Figure 9.1 shows pulsed IV data for the GaN HEMT device for quiescent bias Vgsq = -5 V, Vdsq = 0 V along with pulsed IV data for quiescent bias Vdsq = -5 V, Vdsq = 5 V. The gate

voltages are the same, and the power dissipated in the device is approximately 0 W. The "drain lag" in this device, the dependence on the quiescent bias drain voltage Vdsq, is quite significant, likely indicating that a significant amount of active substrate traps are present in the device. It appears that for higher values of Vdsq, two predominant effects occur: (1) the knee drain voltage is higher, and (2) the value of current at high values of Vds is lower. Two modifications are proposed to account for these two effects in the model.

The expansion of the tanh function with Vdsq is a result of the slow electron emission process occurring when pulsing from a higher drain voltage to a lower drain voltage. The emission effect, as explained in Chapter 4, is a slow effect and has a time constant significantly longer than that of the pulse used for the measurement. This effect can be partially modeled by adding a Vdsq-dependent expansion factor in the hyperbolic tangent. As the multiplying coefficient of the hyperbolic tangent, α, is increased, the hyperbolic tangent compresses in terms of drain voltage, that is, the drain voltage of the knee becomes lower. For a decrease in the value of α, the hyperbolic tangent expands over drain voltage and the knee region is more gradual. This is approximately the effect seen due to a change in the drain quiescent bias point. Figure 9.2 shows f(x) = tanh (αx) for three values of α. This compression and expansion appear very similar to that occurring due to a change in the drain-source voltage.

The Angelov model equation for α is as follows [31]:

$$\alpha = ALPHAR + ALPHAS \times (1 + \tanh(\psi)). \qquad (9.2)$$

Ψ is a polynomial in Vgs and builds a gate voltage dependence into the shape of the hyperbolic tangent function; that is, it accounts for the dependence of the drain voltage at the knee upon the gate voltage. It appears from Figure 9.1 that ALPHAS is nonzero for this device, as the knee drain voltage seems to be dependent on Vgs. If a proportional difference in the knee voltage is to be maintained as the quiescent drain voltage is changed, then both ALPHAR and ALPHAS need to be adjusted. The proposed adjustment to (9.2) to account for the slow Vdsq-dependent electron emission is as follows:

$$\alpha = \frac{1}{1 + Q1 \times Vdsq}\left(ALPHAR + ALPHAS \times (1 + \tanh(\psi))\right) \qquad (9.3)$$

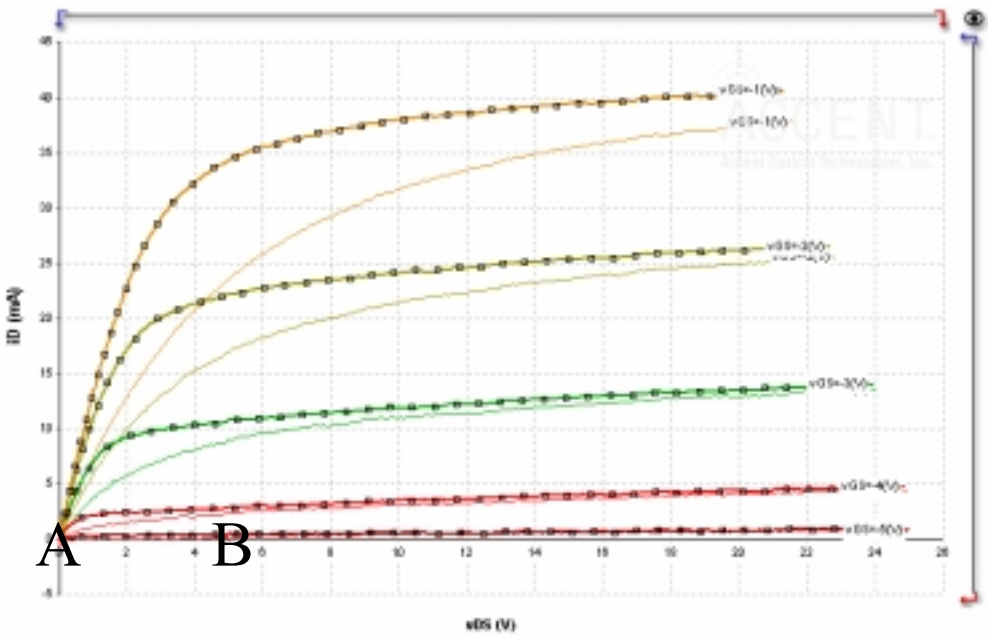


Figure 9.1. Pulsed IV Measurements for GaN HEMT Corresponding to Quiescent Bias Points A (Vgsq = -5 V, Vds = 0 V, Darker Curves) and B (Vgsq = -5 V, Vdsq = 5 V, Lighter Curves)

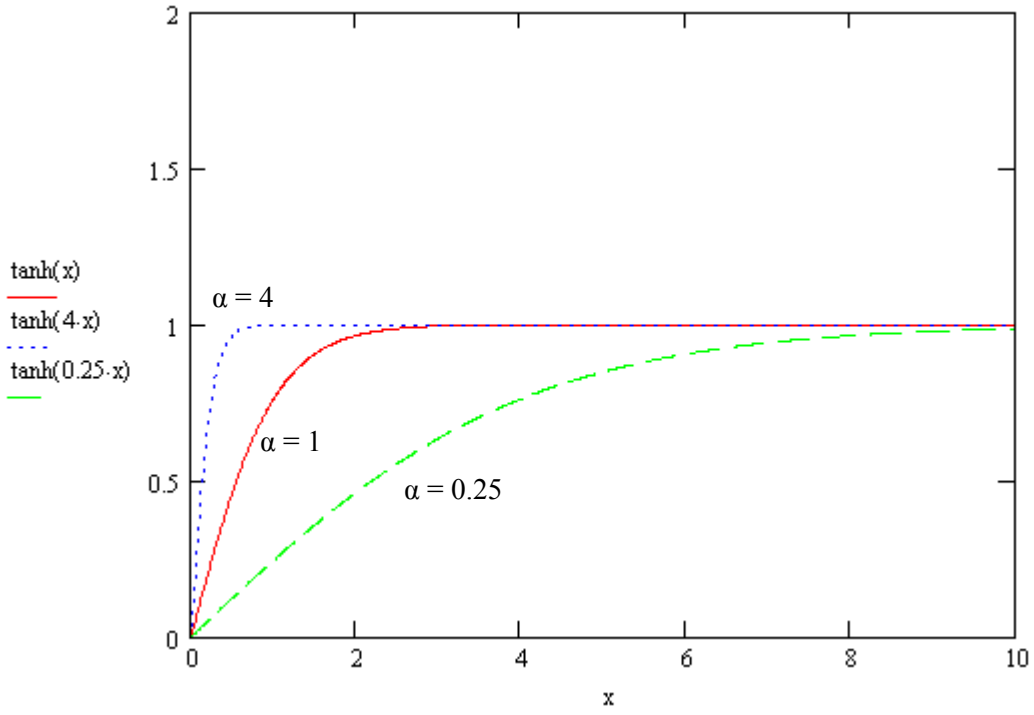


Figure 9.2. tanh (αx) Function for α = 4, α = 1, and α = 0.25

The second effect, the reduction of the IV curves at large drain voltage for higher values of Vdsq, must also be modeled. For devices with substrate traps, a positive drain voltage leads to the capture of electrons by trap states near the substrate at the bottom of the channel. This results in what is referred to by the literature as a "backgating" effect [58], [60]. The presence of the electrons in these trap states causes a depletion region to form near the bottom of the substrate, in addition to the depletion region surrounding the gate, as shown in Figure 9.3. This reduces the channel width, reducing the current. Kwok [58] states that the backgating effect results in the multiplication of the FET Ids equation by a factor

$$\frac{1}{1+K_1\left(\frac{Z}{L}\right)q\mu_n N_D V_{DS}}.$$

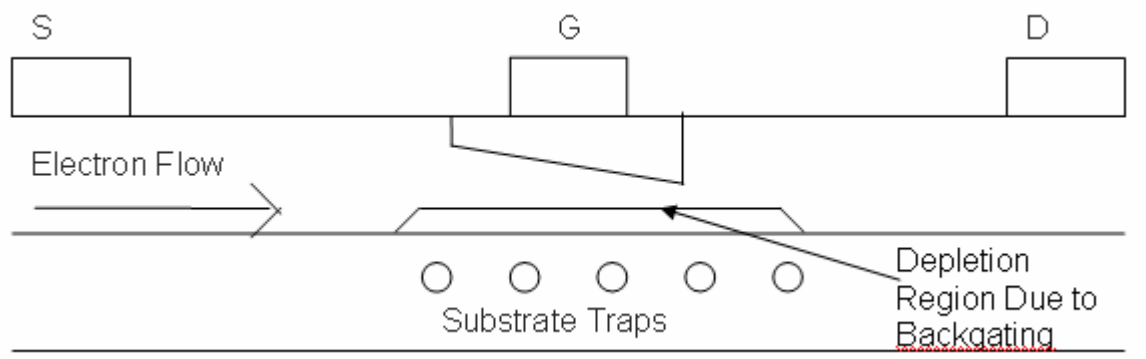


Figure 9.3. Diagram of Device Including Backgating Depletion Region

If the capture time constant is smaller than the pulse length, then the backgating is dependent on the measured ("pulse-to")Vds value and not on Vdsq; this appears to be the case examined by Siriex [38]. However, if the capture time constant is larger than the pulse length, the backgating is a function of Vdsq, as appears to be the case for this device. To include Vdsq-dependent backgating in the model, a new Vdsq dependent term with the same form is proposed that operates on the Ipk value (this term thus multiplies the entire Ids equation):

$$\frac{1}{1+Q3*Vdsq}$$

It is this backgating effect, if the time constant of the capture process is longer than the pulsed IV pulse length, that causes direct pulsed IV measurement attempts of the thermal resistance to fail, as shown in Chapter 8.

As far as the quiescent gate voltage is concerned, it can be observed from measured pulsed IV data that the current value for a given bias configuration increases as Vgsq is increased for this device. The quiescent gate voltage dependence is not present in all devices with trapping effects; it is most prominent in devices with significant surface trapping, as discussed in Chapter 4. Figure 9.4 shows the pulsed IV curves for the GaN HEMT for several quiescent bias points of zero drain voltage and differing gate voltages. It can be seen that the IV curves corresponding to higher gate quiescent voltages have higher values of current. Also noteworthy is that the percent change in the current due to the quiescent gate voltage change is nearly independent of drain voltage. It appears that the necessary change in the model equation can be accomplished by multiplying IPK0 by a function containing the gate voltage. Note that the value of α is redefined as shown in equation (9.2). The proposed modifications result in the following equation:

New Terms

$$Ids = IPK0 \times \left[(1+Q2*Vgsq)\left(\frac{1}{1+Q3*Vdsq}\right)\right](1+\tanh(\psi))\tanh(\alpha \times Vds)(1+LAMBDA \times Vds + LSB0 \times \exp(Vdg - VTR)) \quad (9.4)$$

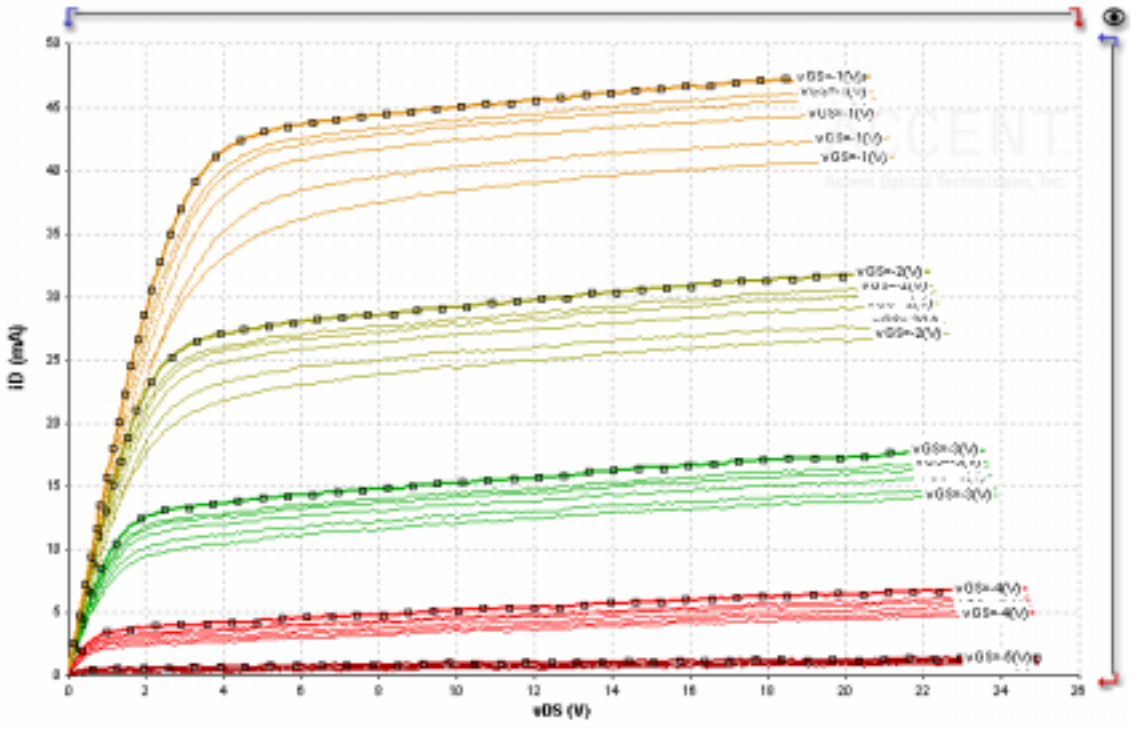


Figure 9.4. GaN HEMT Pulsed IV Curves for Vdsq = 0 V and Vgsq from -5 V (Lowest Curves) to 0 V (Highest Curves)

The expression (9.4) provides a linear change in the model current due to a change in the quiescent gate voltage. As previously mentioned concerning the drain voltage, the quiescent gate voltage can also be a parameter in the model; if the model is constructed to change dynamically over time, then the gate voltage can be calculated using the average-value expression.

To extract the equation properly, all parameters except Q1, Q2, and Q3 (the typical Angelov model parameters) should be extracted from a pulsed IV measurement for zero quiescent drain voltage (for this condition the equation is in its previous state), and Q1 should be extracted from a pulsed IV measurement at a nonzero quiescent drain voltage. Vdsq would be the quiescent bias point, which would need to be manually entered as a parameter in the model. Notice that a multiplication rather than an addition is used to effect the change; this is because the expansion/compression operation is multiplicative. As the development is continued and the model is applied to large-signal performance, it is possible that Vdsq could be dynamically calculated as the DC value of the drain voltage signal, where T_0 is the fundamental period:

$$Vdsq = \frac{1}{T_0}\int_{T_0} v_{DS}(t)dt\,. \qquad (9.5)$$

During device characterization, the drain voltage Vdsq is often held constant because a voltage is directly applied to the drain through an RF choke. Similar considerations can be applied to Idsq and Vgsq.

Will the proposed modifications be sufficient to allow the Angelov model to correctly operate over differing bias conditions in a device with significant trap states? It is here proposed that these simple modifications will vastly improve the performance. As will be shown in the following section, an alteration of model equations in the literature has also dealt with the argument of the hyperbolic tangent function as a function of both drain and gate voltages, the overall current value as a function of gate voltage, and the pinch-off voltage as a function of drain voltage [61]. It may be necessary to include more modifications to the model to perfectly predict performance for all devices; however, these simple additions should serve as a good starting point for building quiescent-bias dependence into the model.

9.2. Previous Attempts at Trap Characterization

Prior to this dissertation, some attempts have been made to correct for the bias-dependence associated with PHEMT devices. Many of these studies have been performed on GaAs and InGaP devices; however, the relatively recent emergence of GaN as a desirable material for high-power device construction makes its study particularly attractive.

Fernandez *et al.* proposed a modeling approach that takes into account the low-frequency thermal and trapping effects noticed in pulsed IV [62]. In that paper, the equation to describe the current was composed of a sum of two expressions: (1) the I_{ds} equation from the Materka model, dependent on the instantaneous drain and gate voltages, and (2) an additional drain current source that contains a dependence upon both instantaneous and quiescent bias voltages, representing the quiescent bias dependence of the IV characteristics. In effect, this modification proposes an additional current source added in parallel in the equivalent circuit for the transistor. While they acknowledge that the quiescent-bias dependence is based on both thermal and trapping effects, their paper also states that it is impossible to separate the effects; something that, at least in a pragmatic way, is demonstrated by the model presented in this dissertation. The model of Fernandez, however, seems to show reasonable results.

A contribution that perhaps is mathematically most similar to that proposed in this dissertation was published in 1997 by Roh *et al.* [61]. In their article, the equations for the Pedro channel-current model [63] are amended to include a quiescent-bias dependence. The modified equation for the RF current reads as follows [61]:

$$I_{dsRF} = \beta\left[u + \log(e^{u} + e^{-u})\right]\tanh(\alpha v_{ds}), \qquad (9.6)$$

where

$$\beta = \beta_0 + \beta_{gs0}V_{gs0} + \beta_T \Delta T_j \qquad (9.7)$$

and

$$\alpha = \alpha_0 + \alpha_{ds0}V_{ds0} + \alpha_{gs0}V_{gs0}\ . \qquad (9.8)$$

Because β is the multiplicative term in the current equation, the modification of this proposed by Roh is similar to that proposed for the Angelov modification proposed in this dissertation. As gate voltage becomes less negative, β increases linearly. The mathematics of this modification are consistent with the physical behavior of the device. Furthermore, this change is completely dependent on the gate quiescent bias voltage V_{gs0} and the change in junction temperature.

While Roh also modifies the coefficient of the hyperbolic tangent, α, as in the USF model, the mathematics of his adjustment seem to be less consistent with the actual device behavior. The hyperbolic tangent expands against drain voltage as the quiescent drain voltage is increased. This means that α will decrease with increasing V_{ds0}, resulting in a negative α_{ds0} in equation (9.8). However, if the drain voltage is increased to a very large value, the value of α will become negative, causing the equation to become inconsistent with the actual operating characteristic of the device. A better form of modification is the multiplication of α_0 by

$1/(1+\alpha_{ds0}V_{ds0})$, the form proposed in this dissertation. This will cause expansion as well; however, the hyperbolic tangent coefficient will approach zero (unlimited expansion), rather than becoming negative as the quiescent drain voltage is increased. A feature of the Roh modifications not included in the Quiescent-Bias Dependent Angelov model that may help to better describe the bias dependence is an inclusion of the hyperbolic tangent coefficient dependence on the quiescent gate voltage.

In two articles written by Koh *et al.*, a quiescent bias dependence is added to models to address the self-heating and trapping problem [64], [65]. In these papers, the problem is addressed by adding multiplicative terms to the current equation, in contrast to some of the other papers, where summing or coefficient modification approaches are used. The approach is written in equation form [64] as

$$I_{0,d}(v_{gs}, v_{ds}, V_{gs0}, V_{ds0}) = I_{ds0}(v_{gs}, v_{ds}) * f_{trap} * f_{thermal} \qquad (9.9)$$

The function I_{ds0} is the current at the quiescent bias point of zero gate voltage and zero drain voltage; this "baseline" approach has been utilized in the USF model. However, the description of the current by these multiplicative thermal and trapping functions, while in principle simple, seems to yield a much more difficult, less physically accurate approach of modeling the thermal and trapping effects; for example, what appears as an expansion of the tanh function in the device from the previous section is difficult to model using a multiplicative term. In addition, an assumption made by Koh while extracting the model is that the substrate traps dominate the surface traps below breakdown [64], a statement that is not true for all devices, including the device whose characteristics are shown in the previous section.

Modification to the Angelov model has been previously attempted. A paper by Cheng *et al.* proposes modification of the Angelov model; however, this modification is to the capacitance functions of the model [66]. This dissertation modifies the Ids equation of the model.

9.3. Modification of the Angelov Model for More Accurate Self-Heating Calculation

In addition to the changes to accurately describe trapping effects, it was necessary to change the Angelov model to describe the pulsed IV heating correctly. The typical model equation uses the thermal circuit of Figure 3.2 to perform the calculations; however, it assumes during IV simulation that the conditions are DC conditions. In pulsed IV measurement, the self-heating is different than in typical DC measurements: it is based on the quiescent bias Vdsq and Idsq, not on the instantaneous Vds and Ids. As a result, a modification was made to the model. The parameter LargeSignalHeat was created. If LargeSignalHeat = 0, the model calculates the

self-heating based on the quiescent bias voltages, as in a pulsed IV measurement. The quiescent drain current Idsq is calculated from the quiescent drain voltage Vdsq and the quiescent gate voltage Vgsq as follows:

$$Idsq = IPK0 \times (1 + Q2 * Vgsq)\left(\frac{1}{1 + Q3 * Vdsq}\right)(1 + \tanh(\psi_q))\tanh(\alpha_q \times Vdsq)(1 + LAMBDA \times Vdsq + LSB0 \times \exp(Vdsq - Vgsq - VTR)) \quad (9.6)$$

Ψ_q and α_q are the values of Ψ and α calculated from the quiescent voltage settings. Vdsq and Idsq are used to calculate the quiescent self-heating in the case where LargeSignalHeat = 0. The power dissipation is calculated from the quiescent drain current and voltage (notice that the product of the gate-source current and gate-source intrinsic voltage also contribute to the power dissipation, but that this contribution is very small):

$$P_D = Idsq \times Vdsq + Igs \times Vgsc \quad (9.7)$$

If LargeSignalHeat = 1, the default calculation of the Angelov model is used:

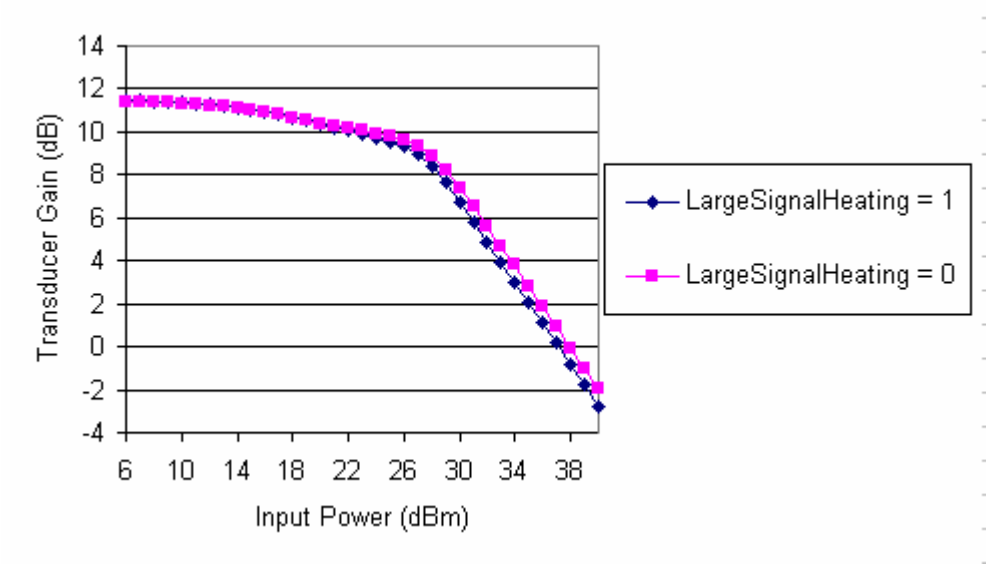
$$P_D = Ids \times Vds + Igs \times Vgsc \quad (9.8)$$

LargeSignalHeat should be set to 1 in large-signal simulations, as it allows changes in DC drain current due to large-signal conditions to be used in the self-heating calculations.

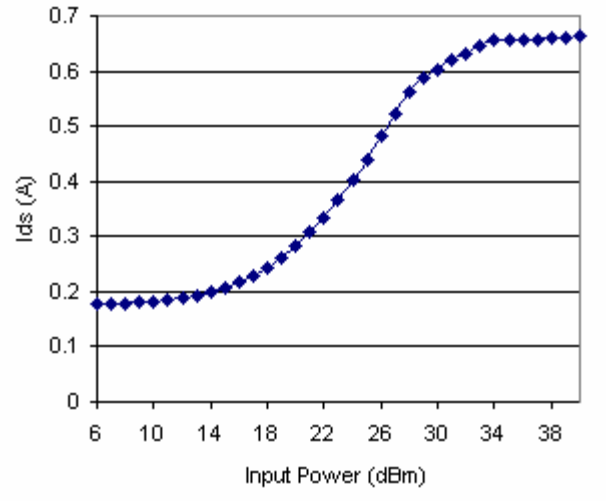
The following guidelines should be followed for the accurate use of the LargeSignalHeat parameter. If a pulsed IV simulation is being performed, the quiescent gate and drain bias values should be entered for Vgsq and Vdsq, respectively, and the parameter LargeSignalHeat should be set to 0. This will allow heating to be calculated according to the quiescent bias point. For small-signal S-parameter simulations, LargeSignalHeat can be set to 0 with appropriate entries for the quiescent bias voltages, as in the pulsed IV case, unless the low frequency of the simulation approaches the thermal cutoff frequency. For large-signal simulations, LargeSignalHeat should be set to 1, with appropriate entries for Vgsq and Vdsq to take trapping into effect. The value of Cth (the thermal capacitance) should be assigned to either a measured value (based on a thermal time constant measurement) or a value that places the thermal cutoff frequency between DC and the frequency content of the RF signal:

$$f_c = \frac{1}{2\pi R_{th} C_{th}} \quad (9.9)$$

Two power sweep simulations using a bias-dependent model extracted for a GaN HEMT (a different HEMT than demonstrated earlier in the chapter, hereafter referred to as "HEMT B"). The results are shown in Figure 9.5. Figure 9.5(a) shows the gain as a function of input power. For low input power values, the simulations produce identical results; however, for higher input power values, the results for LargeSignalHeat = 1 are lower due to the fact that the DC drain current increase is used in the heating calculation for LargeSignalHeat = 1, while for LargeSignalHeat = 0, the initial quiescent bias drain current is used and the self-heating is lower. Figure 9.5(b) shows a slight difference in the gain characteristics occurs for power levels at which the DC drain current is significantly higher (above 22 dBm input power), confirming this.



(a)



(b)

Figure 9.5. (a) Simulation Results for GaN HEMT B Input Power for LargeSignalHeat = 1 and LargeSignalHeat = 0 with (b) DC Drain Current Versus Input Power

9.4. Extraction of the Quiescent-Bias Dependence and Temperature Parameters

Figure 9.6 shows the ADS simulation schematic for the bias-dependent model. The parameters Q1, Q2, Q3, Vdsq, Vgsq, and LargeSignalHeat are available for user modification. Q1, Q2, and Q3 can be extracted from pulsed IV measurements taken from different quiescent bias conditions. As a first step, the "intrinsic" Ids equation parameters should be obtained from

pulsed IV curves taken from quiescent bias point Vgsq = 0 V, Vdsq = 0 V. Figure 9.6 shows the measured and simulated IV curves following model extraction for this quiescent bias condition.

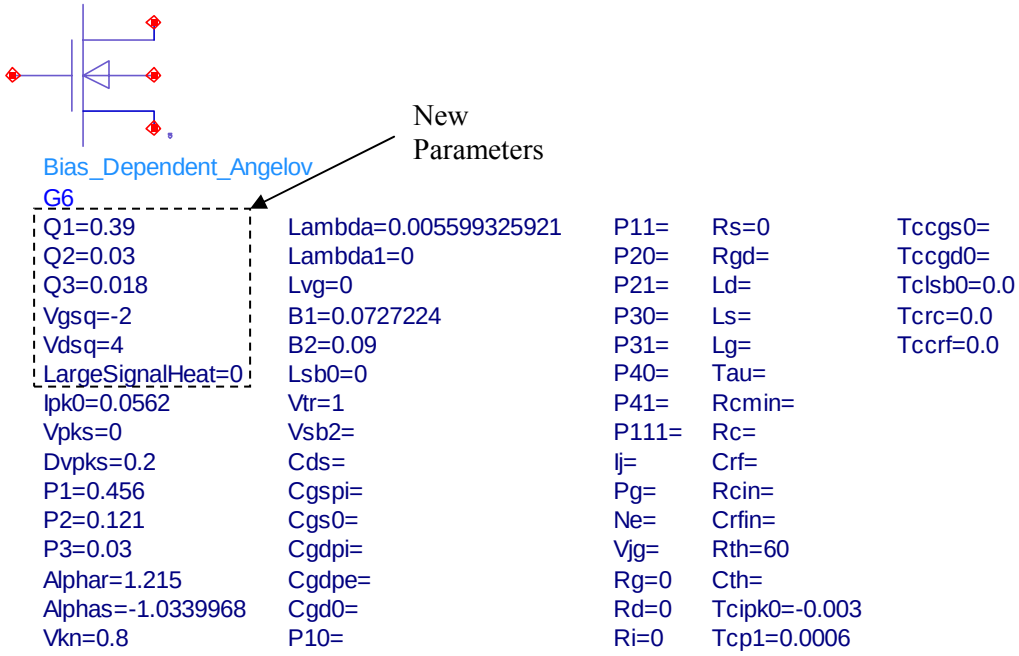


Figure 9.6. ADS Verilog-A Bias-Dependent Angelov Model Element

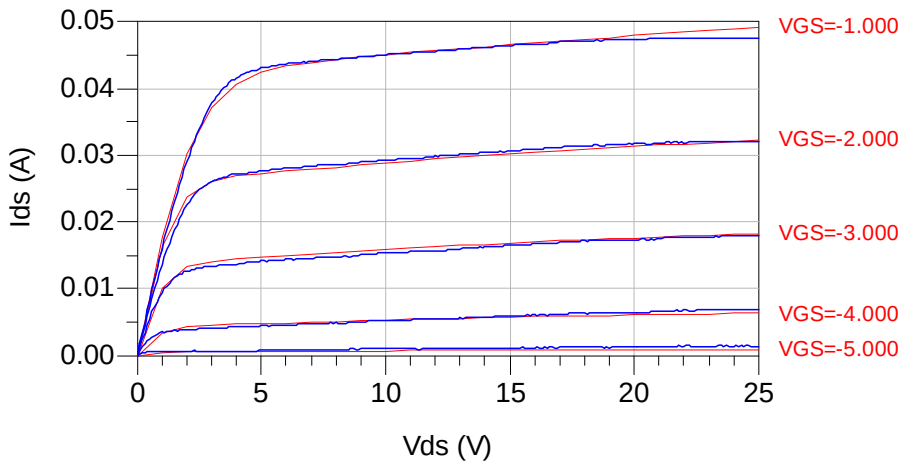
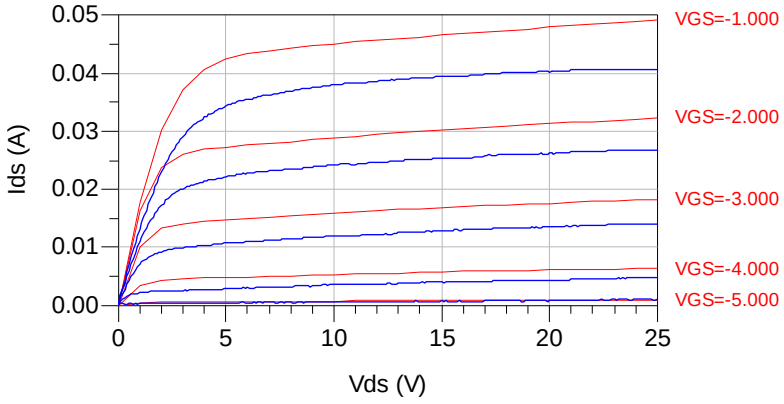
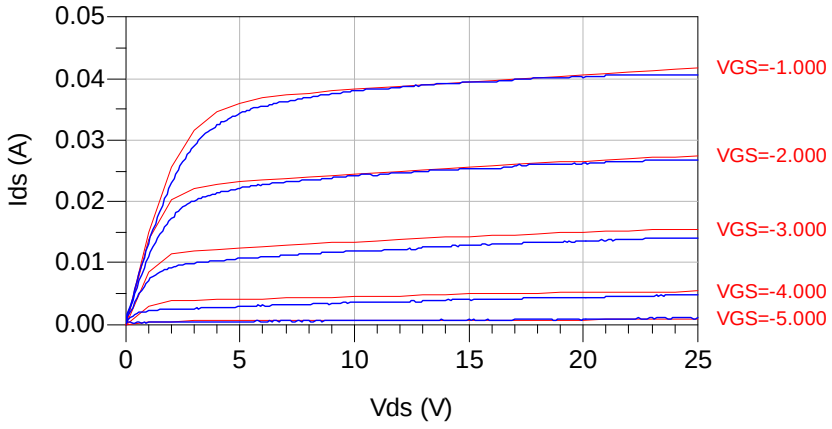


Figure 9.7. Measured (Darker, Blue Lines) and Simulated (Lighter, Red Lines) Pulsed IV Data for Vgsq = 0 V, Vdsq = 0 V

After this, the parameter providing the gate quiescent bias dependence, Q2, was tuned to fit the measured pulsed IV data from the quiescent bias Vgsq = -5 V, Vdsq = 0 V (the drain quiescent bias is the same as above but the gate quiescent voltage is changed). Figure 9.8 provides a measured-versus-simulation comparison of the results.



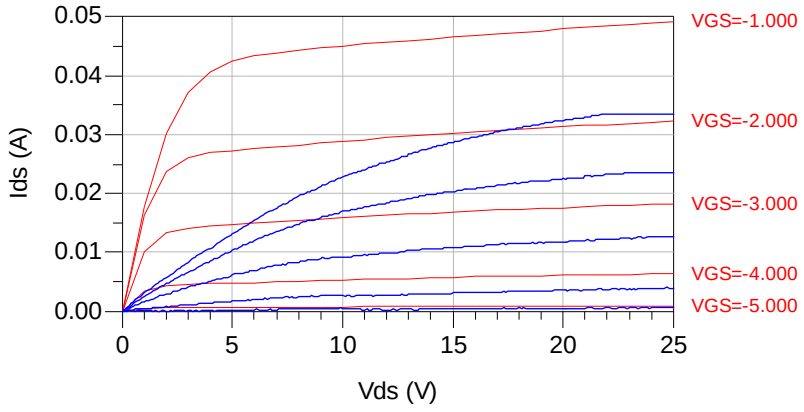
(a)



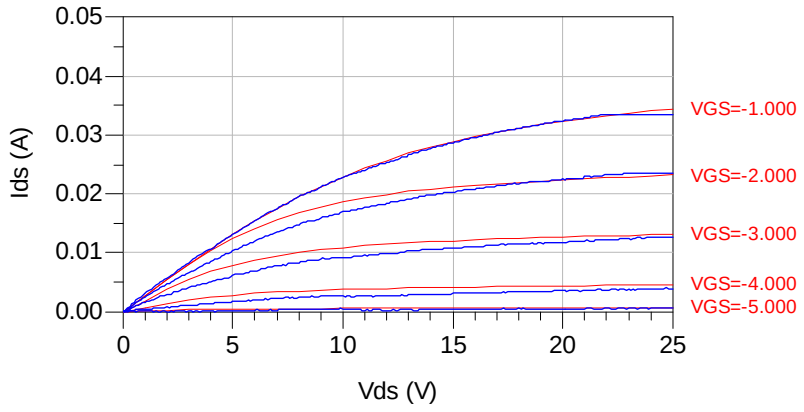
(b)

Figure 9.8. Measured Pulsed IV Data from Vgsq = -5 V, Vdsq = 0 V (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) No Bias Dependence and (b) Bias-Dependent Model

Q1 and Q3, the parameters giving the Vdsq dependence, were then tuned to fit pulsed IV measurements taken with the zero-power quiescent point Vgsq = -5 V, Vdsq = 10 V, as shown in Figure 9.9, and quiescent point Vgsq = -5 V, Vdsq = 5 V, as shown in Figure 9.10. In both cases, it can be seen that the quiescent-bias dependent model allows much better prediction of the results than a pulsed IV model obtained from Vgsq = 0 V, Vdsq = 0 V.

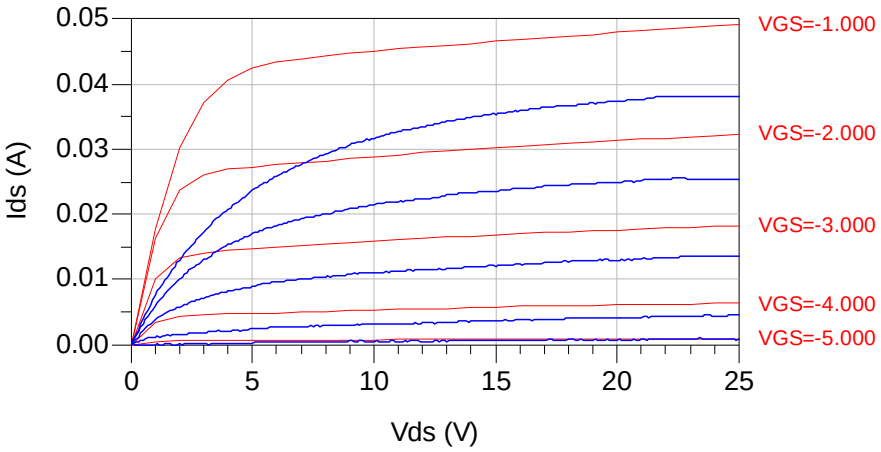


(a)

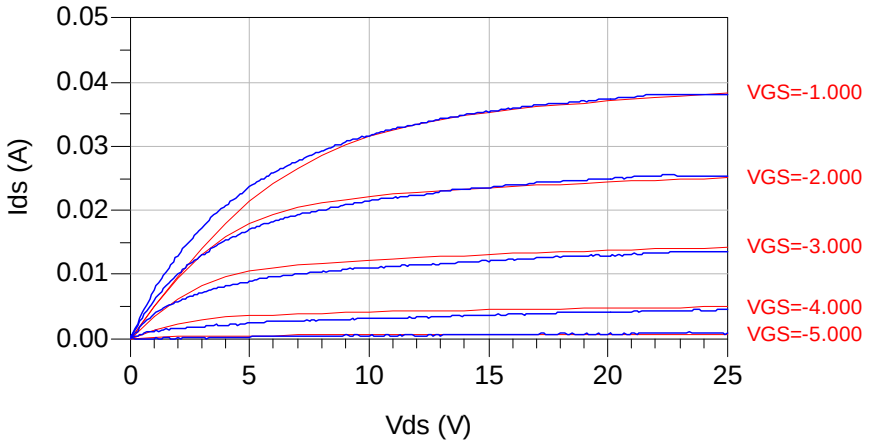


(b)

Figure 9.9. Measured Pulsed IV Data from Vgsq = -5 V, Vdsq = 10 V (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) No Bias Dependence and (b) Bias-Dependent Model



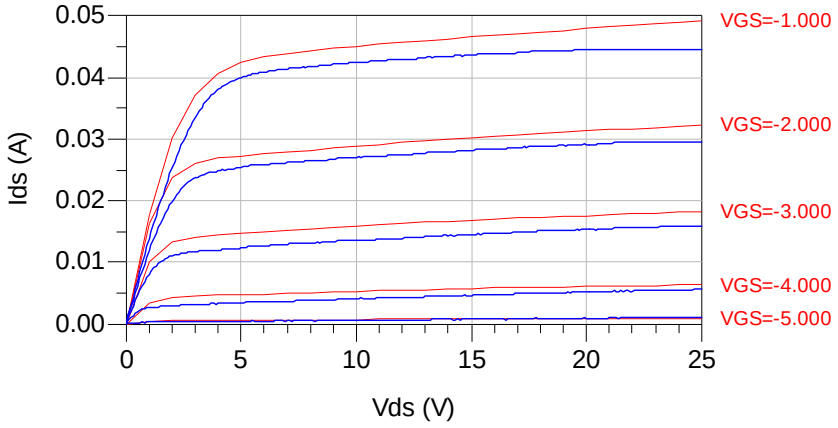
(a)



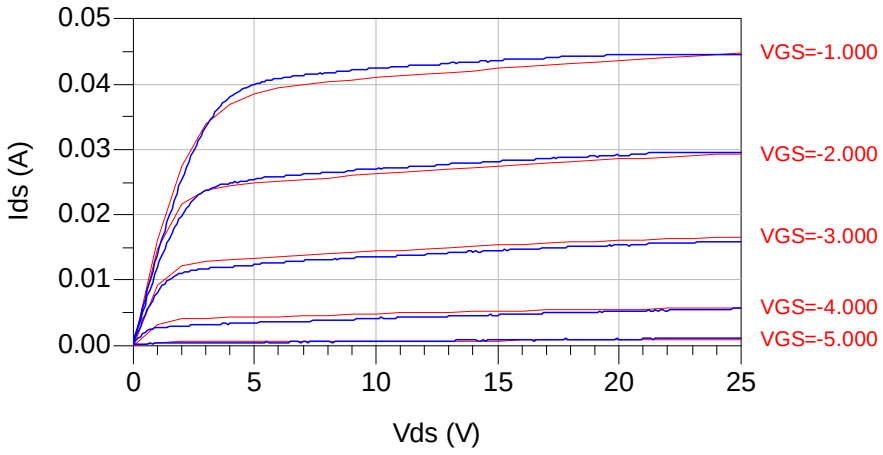
(b)

Figure 9.10. Measured Pulsed IV Data from Vgsq = -5 V, Vdsq = 5 V (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) No Bias Dependence and (b) Bias-Dependent Model

A verification of operation was performed for the quiescent bias condition Vgsq = -3 V, Vdsq = 0 V. Once again, the bias-dependent model seems to provide a nice improvement. Figure 9.11 shows the results.



(a)



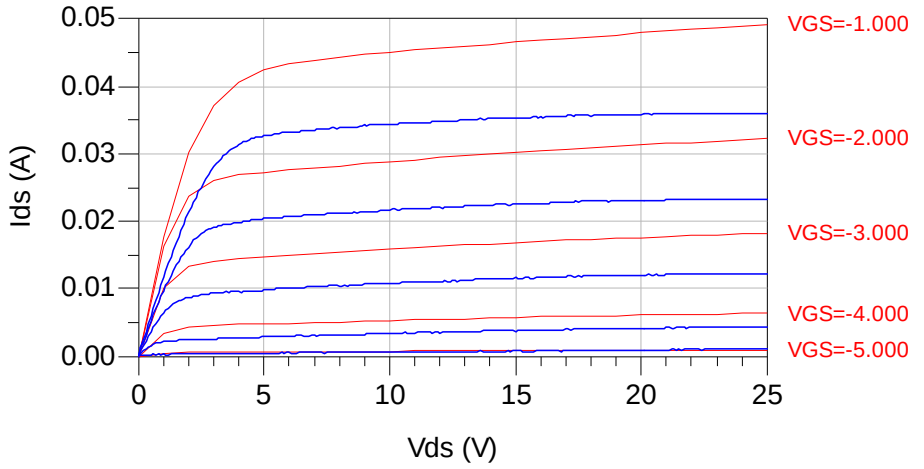
(b)

Figure 9.11. Measured Pulsed IV Data from Vgsq = -3 V, Vdsq = 0 V (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) No Bias Dependence and (b) Bias-Dependent Model

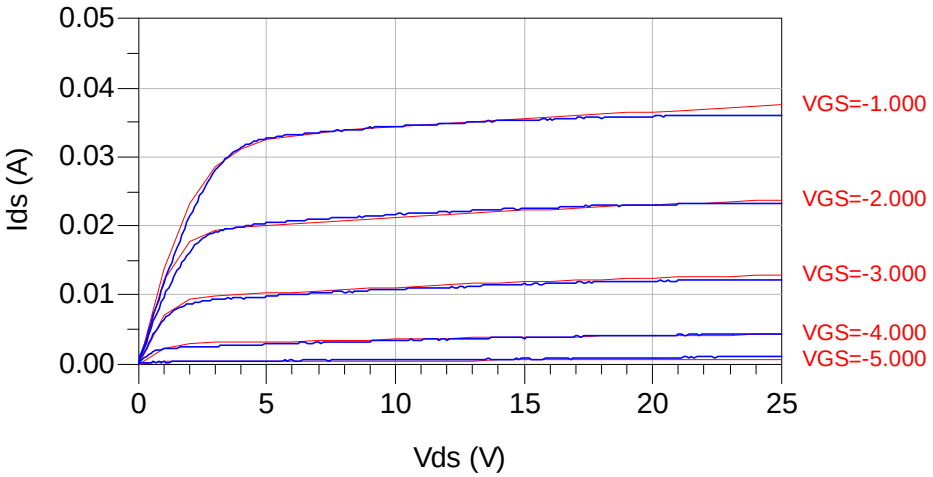
After obtaining the trap-related quiescent-bias dependence, the part of the model expressing the temperature dependence can be extracted. The proposed process for determining temperature dependence begins with the extraction of temperature dependence from pulsed IV measurements for Vgsq = 0 V, Vdsq = 0 V at different ambient temperatures. These results can be used to extract the coefficients Tcipk0 and Tcp1. As a second step, the thermal resistance value can be adjusted to match the model to a measurement taken at a quiescent bias condition of nonzero power dissipation.

The primary temperature-dependent parameters in the Angelov model are Tcipk0 (the temperature coefficient of Ipk0, and Tcp1 (the temperature coefficient of polynomial coefficient P1). These should be extracted from two or more sets of pulsed IV with identical quiescent bias voltages but different ambient temperature values.

The initial IV equation was obtained for an ambient temperature of 45 °C. A set of pulsed IV curves at the same bias condition (Vgsq = 0 V, Vdsq = 0 V) but different ambient temperature, was measured at an ambient temperature of 120 degrees Celsius. This is a temperature increase of 75 °C, enough to show significant effects on the IV curves. To perform the simulation, the value of Trise, the temperature difference between the temperature at which the listed Angelov parameters are valid and the simulation temperature, was changed from 0 to 75. The parameters Tcipk0 and Tcp1 were adjusted to provide a best fit to the new set of IV curves. The IV curves are shown in Figure 9.12.



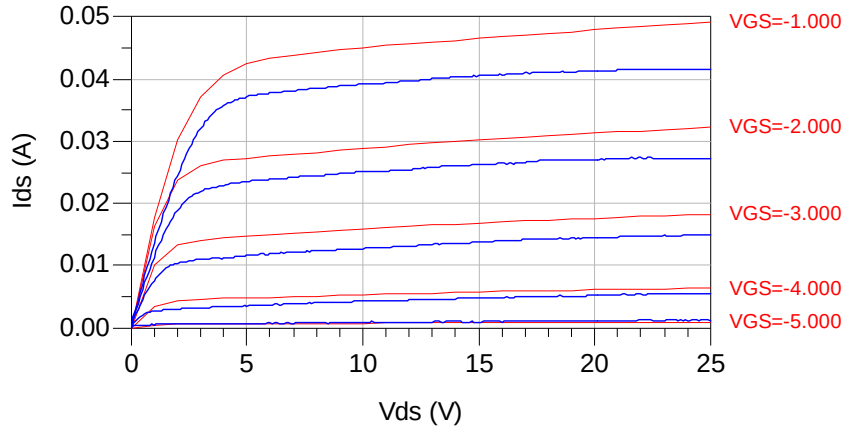
(a)



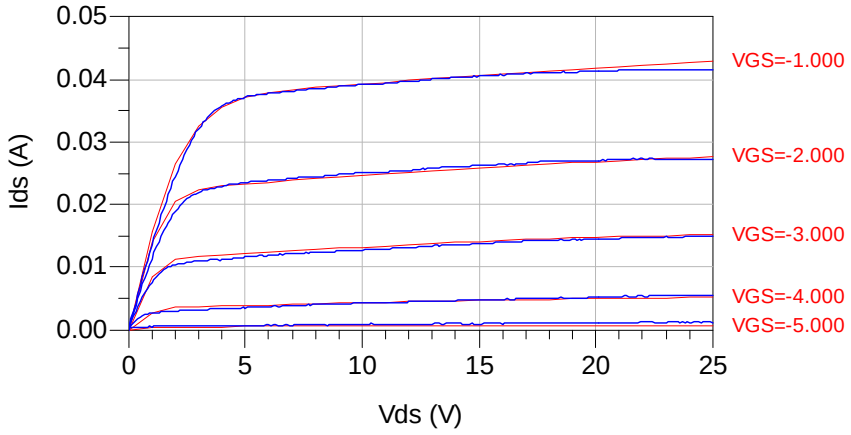
(b)

Figure 9.12. Measured Pulsed IV Data from Vgsq = 0 V, Vdsq = 0 V, and an Ambient Temperature of 120 °C (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) No Temperature Dependence of the Parameters and (b) Included Temperature Dependence of the Parameters

To demonstrate the accuracy of the temperature dependent parameters, the IV curves were measured at the same quiescent bias point with an ambient temperature of 85 °C (Trise = 40). The results are shown in Figure 9.13.



(a)

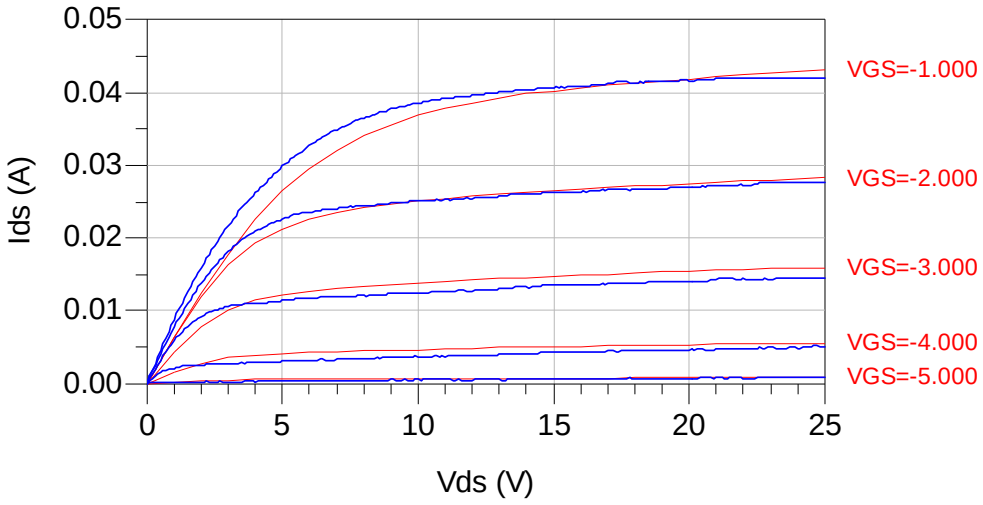


(b)

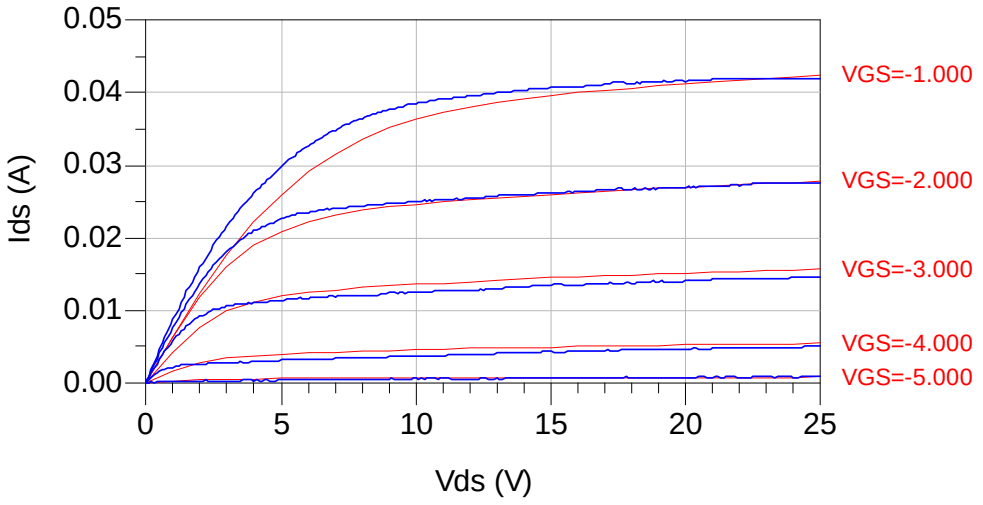
Figure 9.13. Measured Pulsed IV Data from Vgsq = 0 V, Vdsq = 0 V, and an Ambient Temperature of 85 °C (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) No Temperature Dependence of the Parameters and (b) Included Temperature Dependence of the Parameters

At this point, the thermal resistance can be used as a fitting parameter to the data corresponding to the nonzero-power quiescent bias point. Because temperature coefficients and trap fitting parameters have already been extracted, the only remaining piece of information is the self-heating caused by the dissipated power (the thermal resistance). The value of Rth should be adjusted until the best achievable fit to a set of IV curves from a quiescent bias point with nonzero power dissipation. Figure 9.14(a) shows the IV results with a small value of Rth (no self-heating, while Figure 9.14(b) shows that Rth = 60 ˚C/W provides a good match between the measured and simulated data for the quiescent bias condition Vgsq = -2 V, Vdsq = 4 V. As shown in Chapter 8, the thermal resistance for the GaN HEMT was measured using an infrared measurement at approximately 60 ˚C/W. Using pulsed IV measurements with the assumption that the electron capture time constant is less than the pulse length (200 ns) for this device, the thermal resistance was measured as approximately 240 °C/W, as shown in Chapter 8. Figure 9.15 compares the results for Rth = 60 ˚C/W (infrared) and 240 ˚C (pulsed IV, based on an apparently false assumption for this device). The value of Rth = 60 ˚C/W provides a much better fit. Using Rth = 240 ˚C/W seems to cause the simulated self-heating to be too large, as evidenced by the IV curve fit in the high-power regions.

These results demonstrate the accuracy of the quiescent-bias dependent model to generate electrodynamically accurate IV curves for different quiescent bias points and to characterize both trapping and self-heating in a device with reasonable accuracy. It appears that the thermal resistance can accurately be measured for devices with significant trapping effects through extraction of this model. In addition, the results show limitations of trying to measure the results directly with pulsed IV. The pulse length should be longer than the time constant of the electron capture process for this method to be used.

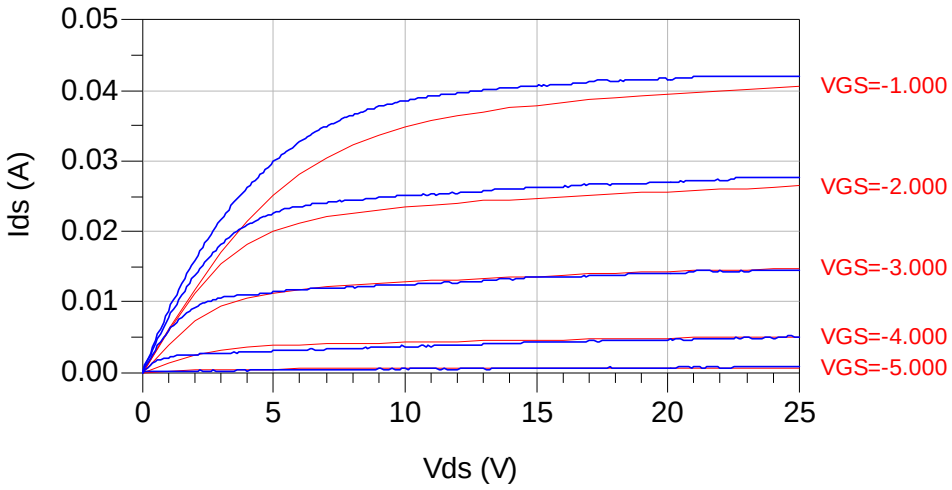


(a)

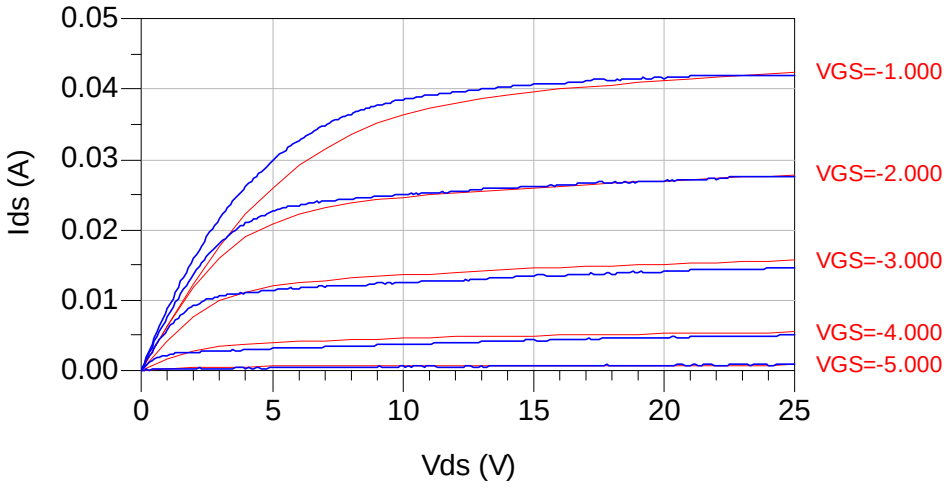


(b)

Figure 9.14. Measured Pulsed IV Data from Vgsq = -2 V, Vdsq = 4 V (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) Thermal Resistance = 0.001 (No Self-Heating) and (b) Thermal Resistance = 60 °C/W



(a)



(b)

Figure 9.15. Measured Pulsed IV Data from Vgsq = -2 V, Vdsq = 4 V (Darker, Blue Lines) and Simulated Pulsed IV Data (Lighter, Red Lines) for (a) Thermal Resistance = 240 °C/W (USF Pulsed IV Measured Value - Incorrect) and (b) Thermal Resistance = 60 °C/W (Infrared Imaging Measured Value)

The results shown in this chapter demonstrate that a reasonable approximation of thermal and trapping effects is obtained with the quiescent-bias dependence added to the Angelov model. In future work, it may be helpful and time-effective to allow parameters to be extracted through minimization routines designed to minimize the difference between simulated and measured pulsed IV data. A metric to provide the difference between these IV curves such as the normalized difference unit could be used [67].

9.5. Chapter Summary

A new quiescent-bias dependent Angelov model with self-heating developed by the author has been shown to provide significant improvement in predicting the device behavior at a nonzero-power quiescent bias condition. Methods have been given to extract the trapping-related quiescent bias dependence, followed by a method to extract the thermal resistance of the device. In addition, extracting the bias-dependent parameters appears to allow accurate extraction of the device thermal resistance, a significant accomplishment for devices with trapping effects. The value of thermal resistance that seems to provide a good match to pulsed IV data corresponds with the approximate thermal resistance value obtained using infrared measurements. Furthermore, the results seem to verify that caution must be used in attempting to measure thermal resistance directly with pulsed IV measurements, as stated in the previous chapter. The results should be very useful in developing GaN device models and often should allow improved nonlinear (load-pull, power sweep, third-order intercept) prediction capabilities of the model.

CHAPTER 10: CONCLUSIONS AND RECOMMENDATIONS

This dissertation provides an overview of improved methods for accurate FET device characterization and modeling that addresses thermal and trapping effects. The development of modifications to the Angelov model to allow these effects to be modeled and separated is presented, along with a method for more efficient load-pull validation of the models and a procedure for developing and benchmarking a pulsed S-parameter system.

10.1. Conclusions

Basic methods for extracting the thermal resistance and thermal capacitance in devices with insignificant trapping effects, such as Si MOSFETs, were examined. The thermal resistance can be measured by comparing pulsed and static IV curves, by measuring pulsed IV at different quiescent bias points and adjusting the chuck temperature to obtain a match between the curves, or by fitting static IV curves by tuning the thermal resistance parameter in a model. It was shown that the thermal time constants and the corresponding thermal capacitance network can be extracted using simple function fitting to transient measurement results. The idea of using multiple thermal time constants was examined. It was discovered that using two thermal time constants instead of one can allow improved modeling of the thermal effect in some cases. For the Si VDMOSFET examined, however, a reasonable fit to a thermal transient was obtained using one thermal time constant.

An examination of trapping effect physics revealed reasoning for the shape of the pulsed IV curves in devices with significant trapping effects, such as GaN HEMTs. Trap states, often associated with defect sites within the energy bandgap of a device, can be located near the device surface or beneath the channel in the substrate of the device. The behavior of the substrate traps tends to be heavily dependent on the drain-source voltage. For an increase in drain-source voltage, electron capture by the trap state is the dominant effect and normally happens relatively quickly. For a decrease in drain-source voltage, electron emission from the trap state is the dominant effect, an effect that can take as long as milliseconds. Surface trapping is heavily dependent on the drain-gate voltage. The electron capture (or hole emission) effect occurs for

increasing drain-gate voltage, while the electron emission (or hole capture) effect occurs for decreasing drain-gate voltage. The time constants of these effects are believed to be comparable to their substrate-trap counterparts.

A pulsed-RF, pulsed-bias S-parameter system was constructed. A critical step in this process is the design, simulation, and construction of bias tees to allow a pulsed bias to be applied to the device through the "DC" port of the bias tee. The capability of a custom bias-tee design was verified by measuring pulsed IV data through custom bias tees and comparing the data to the pulsed IV results measured through typical commercially available bias tees. The results have shown that many commercially available bias tees are inadequate for performing pulsed-bias measurements.

The construction of a pulsed-bias, pulsed-RF S-parameter system has been detailed. The system was designed based on the sin x/x spectrum of a pulsed RF signal and measurements can be performed on a typical VNA by measuring continuously; the RF signal, however, is only turned on during the bias application. The performance of this system has been extensively benchmarked using measurements on passive components. It was found that precision is decreased as pulse length is reduced; in addition, the measured results of a band-pass filter indicate that the dynamic range decreases with decreased duty cycle. It has been shown for two devices that the self-heating is lower in the pulsed-bias measurements, as illustrated by a higher $|S_{21}|$ than for continuous-bias measurements. Furthermore, thermal correction procedures suggested by results in the literature have been verified by using the system to measure a Si VDMOSFET. A procedure for thermally correcting S-parameters in devices with self-heating by adjusting the chuck temperature to compensate for unwanted bias self-heating variations has been proposed.

Measurements to validate nonlinear models are very important in the modeling process. A new peak-search algorithm for performing load-pull has been implemented and tested in both measurement and simulation. It has been shown that the results possess a high level of accuracy and precision and that the algorithm can find the maximum power and associated reflection coefficient with a relatively small number of measured Smith-Chart reflection coefficient points. The efficient measurement of the maximum-power reflection coefficient and power value has opened opportunities for additional measured-versus-simulated comparisons, such as the power-swept load-pull demonstrated in this work. In addition, the availability of this algorithm should facilitate peak searches over other swept parameters, such as bias and process variation.

The difficult problem of measuring thermal resistance for devices with significant trapping effects has been addressed. Based on the physics of trapping effects, a measurement procedure using pulsed IV measurements from different, strategically chosen quiescent bias points has been proposed that appears to be valid if the time constant of the electron capture effect is shorter than the pulse length used for the pulsed IV measurements. An example is shown of attempting to use this method for a trap-laden GaN HEMT; however, test results may indicate that the electron capture time constant is longer than the pulse length. This conclusion is consistent with the fact that the thermal resistance result from the pulsed IV measurement differs greatly from infrared measurements of the thermal resistance.

Finally, a quiescent-bias dependent Angelov model has been introduced. The Verilog-A code for the Angelov model was modified to include a quiescent-bias dependence based on trapping effects. In addition, the model was modified to allow accurate calculation of self-heating for both pulsed IV measurement and large-signal operation. The model is designed to emulate accurate IV characteristics for a user-entered quiescent bias point. A fitting procedure for this model has been detailed. The standard Angelov parameters are first determined from a set of pulsed IV data taken from zero-bias conditions. The parameters of quiescent dependence are then found by examination of pulsed IV from zero-power quiescent bias conditions. Temperature coefficients are fit by matching zero-bias pulsed IV data taken at different temperatures. Finally, the thermal resistance can be determined using pulsed IV curves from a nonzero-power quiescent bias point. For the GaN HEMT shown, it was found that the thermal resistance results agree with infrared measurement data. From the results presented in this work, it appears that the quiescent-bias dependent modeling approach reasonably predicts both thermal and trapping effects on the IV characteristics.

10.2. Recommendations

From the results presented in this dissertation, several areas in which future exploration should be performed can be examined. Techniques for constructing and benchmarking a pulsed-bias, pulsed-RF S-parameter system using a typical vector network analyzer have been demonstrated herein. In addition, the principle of thermal correction of S-parameters based on the thermal resistance of a device has been verified. A suggested next step would be to develop methods for generating electrothermally accurate S-parameters at given bias and temperature conditions. This could be performed by performing continuous bias S-parameter temperatures over a variety of bias and temperature conditions to develop a bias- and temperature-dependent

model, as outlined by Winson et al [68]. The device thermal resistance could be used to calculate the channel temperature from the dissipated power at the bias condition, and isothermal S-parameter results could be generated by this model.

Initial development of a load-pull peak-search algorithm has been performed. A next step in utilizing this algorithm to its full potential is strengthening the code to withstand difficulties that often occur in load-pull measurement and adapting it to be used in load-pull measurements with criteria other than maximum output power. For example, the algorithm could be improved to detect oscillation and then to move away from the region of the Smith Chart where this occurs. Another challenge that should be addressed is to enable the algorithm to function in situations where a high noise floor is present, such as pulsed measurements. In pulsed measurements, the dynamic range can be relatively small if the duty cycle is low. Thus it may be difficult to correctly identify the direction in which the peak search should proceed because the actual device output power may be below the noise floor of the measurement for some load impedances. In many of these cases, it may be interesting to implement a random search algorithm to ensure that points in a region of the Smith Chart resulting in output power above the noise floor are measured.

The peak-search algorithm has been tested to find the optimum impedance for maximum-power terminations; however, what if the maximum-PAE termination is desired? Examination and testing of the algorithm to ensure that it will work correctly to find maximum PAE should be performed. Furthermore, the algorithm should be tested to see if a defined function representing a compromise between output power and PAE can be used to define the "maximum point" and if the search will complete correctly in a variety of cases.

The development of a source- and load-pull technique to efficiently find both the optimum source and load terminations in one procedure would also be useful. In parallel with these explorations, higher-level algorithms should be implemented that can efficiently utilize the peak search over swept conditions, such as power-swept or bias-swept load pull.

Continued improvement of the quiescent-bias dependent Angelov model should be attempted. A specific change that should be examined is the re-centering of the quiescent-bias dependence. Presently, the trapping condition at which all trapping corrections vanish is at Vgsq = 0, Vdsq = 0. It is likely that re-centering this "zero-trapping" term to a bias condition of interest would result in improved performance in areas most meaningful to the application in which the model is to be used. While it may be necessary to choose a bias condition that does not include self-heating, re-centering this bias-dependence may ensure that the use of this model does

not degrade the ability to predict behavior in the regions of interest as compared to a traditional model, which would be extracted from pulsed IV characteristics at the quiescent bias point of most interest. In addition to re-centering the quiescent dependence, dynamic prediction of trapping effects should be explored. Extraction techniques for trapping-effect time constants should be developed and representation of the time-dependence in the model should be investigated.

The impact of the quiescent-bias dependence on the accuracy of large-signal prediction should be more closely examined. A comparison should be performed for load-pull and power-sweep prediction of two-models: a typical Angelov model and a quiescent-bias dependent Angelov model. It is hypothesized that, because the bias-dependence allows IV curves to be more accurately predicted over a range of bias conditions, the bias-dependent model will often show more accurate large-signal prediction over a wide range of bias conditions than a conventional Angelov model for many devices.

10.3. Chapter Summary

The purpose of this dissertation has been to improve electrothermal model extraction capabilities for FET devices, including FETs and HEMTs with significant trapping effects, and to investigate the accurate and more efficient performance of measurements related to the extraction and validation of the model. It is proposed that the results presented in this work represent a beneficial contribution to this effort; however, the continued improvement and exploration of the areas in which these contributions have been presented promises to result in enhanced electrothermal modeling capabilities and improved related measurement methods.

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APPENDICES

Appendix A: Estimating Maximum Point Temperature from an Infrared Image

Infrared imaging systems such as the Quantum Focus InfraScope (demonstrated in Chapter 8) [30] are often used to determine the maximum channel temperature in a transistor [58]. This measurement result is used to determine the thermal resistance. However, the maximum temperature may often appear slightly lower in infrared images due to the fact that, in actuality, point temperatures are not measured in this infrared system. Instead, the result shows a temperature for each pixel that is, in essence, an average taken by the detector over the spatial range covered by that pixel. This memo describes a procedure that uses the pixel showing the maximum temperature and the surrounding pixels to predict the point temperature at the center of the pixel with the maximum average temperature.

The area encompassed by each pixel, A, can be found from the description of the instrument. In addition, the temperature represented by each pixel is known. The first step is to find the pixel providing the maximum temperature. Following this, the temperatures at the pixels surrounding this maximum-temperature pixel should be recorded, to about four or five layers (depending on the order of fit required). An average of the pixel temperatures should be computed, first for the center pixel (with area A), then for the pixels immediately surrounding the center pixel (the total area can be computed), then going out to the next layer, and so on. After several layers have had averages computed, a plot can be constructed of average temperature versus the area over which the temperature is added. A function can be fit to this data. To find the maximum "point" temperature, the limit of this function can be taken as the area goes to zero (i.e. extrapolate the data-fitting curve to zero). This result should provide a rough estimate of the maximum point temperature, which, in general, will be higher than the maximum pixel temperature. An assumption is implicit in this analysis: it is assumed that the pixels are small enough relative to the area of heating that a function illustrating a significant increase in average temperature with decreasing area can be seen.

As usual, a tradeoff occurs in this result. For an accurate function to be fit, the pixel size must be relatively small compared to the size of the region of change. However, the situations where a large correction is needed are those where the pixel size is large relative to the region of change; that is, a large amount of averaging is present in each pixel and it is necessary to find the maximum value. Thus, in many situations where the averaging ability would be in the greatest demand, it will have reduced accuracy. However, in many cases, this theory, even if not completely accurate, may yield a more reasonable estimate for maximum temperature than simply using the highest average pixel temperature.

Appendix A: (Continued)

The maximum channel temperature was computed for a GaN HEMT was computed from infrared temperature data measured under bias. Figure A.1 shows the image of the HEMT taken with the device under bias against a temperature map. Table A.1 shows a temperature breakdown of the maximum temperature pixel and the pixels surrounding it.

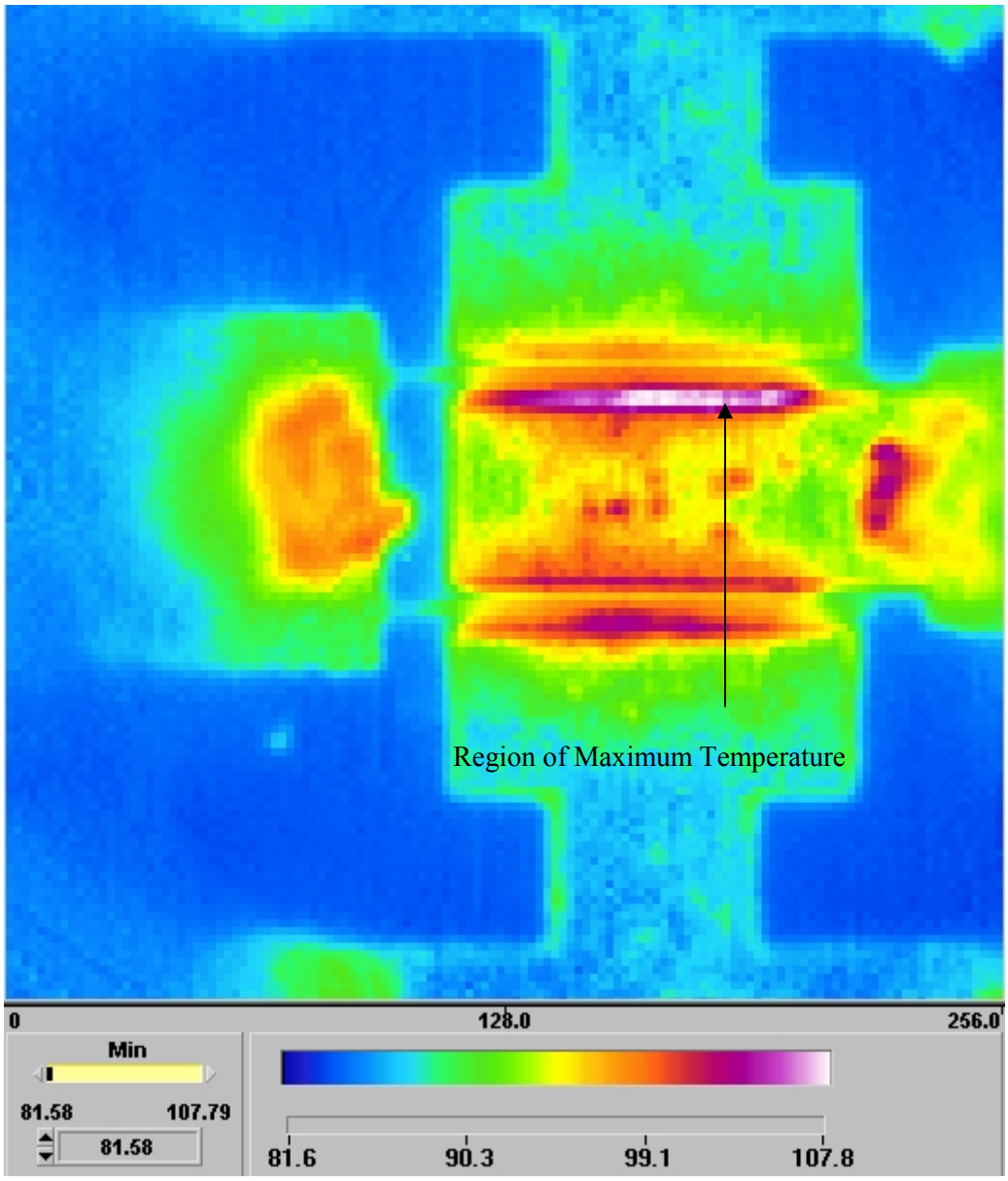

Figure A.1. Quantum Focus InfraScope [30] Infrared Image of GaN HEMT Showing the Region of Maximum Temperature

Appendix A: (Continued)

For the measurement taken, each pixel is a 1.6 μm x 1.6 μm pixel (Area = 2.56 μm^2). Each "layer" of pixels was used in an average. For the lowest layer, only the center pixel was used in the average. As the average was expanded, larger areas were measured. Table A.2 shows the details. It can be seen that the average temperature becomes lower as more pixels are used in the averaging.

The data was fitted and a polynomial fit was performed to the data. Figure A.2 shows that an excellent fit was achieved to the data. The limit of the fitting function as the area approaches zero is 108.01 ˚C. This is an increase of 0.22 ˚C over the maximum pixel temperature. While the maximum temperature increases, the difference in the thermal resistance results should be almost unnoticeable in this case. However, this algorithm may prove more effective in cases where the pixel size is larger and less spatial resolution is available.

Table A.1. Pixel-By-Pixel Temperature (˚C) Breakdown Around the Pixel of Maximum Temperature

99.87	99.52	99.47	99.36	99.27	99.31	98.85
101.77	102.32	102.13	102.06	101.91	101.62	101.55
101.57	107.22	107.35	107.60	107.45	107.05	106.76
107.51	107.60	107.30	107.79	107.54	107.27	107.33
103.57	103.80	103.74	103.69	103.57	103.48	103.34
100.32	99.99	99.98	99.55	99.86	99.23	103.22
98.81	97.92	98.17	98.20	98.23	97.66	99.84

Table A.2. Averaging Results

Layer	Area (μm^2)	Pixels	Average Temp. (˚C)
1	2.56	1	107.79
2	23.04	9	106.226
3	64.00	25	104.044
4	125.44	49	102.623

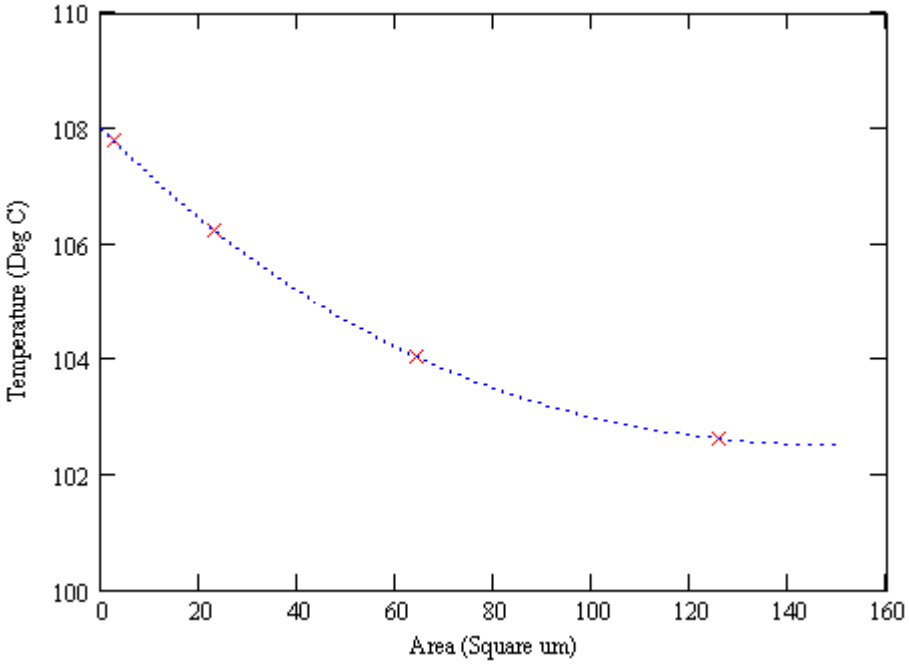

Figure A.2. Data Points (X's) and Fitting Function (Dotted Line)

While the estimated maximum point temperature in this case is only slightly larger than the maximum pixel temperature, the method may prove useful in cases where the pixel size is large compared with the size of the area of heating. Of course, the theory behind this technique could be applicable to other mapping situations performed on a pixel-by-pixel basis where a maximum value must be found. Further revision and attention to this approach may yield a method to find the maximum point temperature, which may not be located at the center of the pixel with the highest average temperature.

ABOUT THE AUTHOR

Charles Passant Baylis II received his B.S. in Electrical Engineering with a Minor in Mathematics from the University of South Florida in 2002 and his M.S. in Electrical Engineering from USF in 2004. He entered the Ph.D. program at USF in 2004, where he has served as an Adjunct Instructor and as a Research Assistant in the Center for Wireless and Microwave Information (WAMI) Systems housed in the Department of Electrical Engineering. His research interests are microwave transistor modeling and related measurement techniques; active RF and microwave circuit design, including silicon RFIC design and MMIC design; and related system applications. While at USF, he has authored several papers related to transistor modeling and associated measurements. He is a student member of the Institute of Electrical and Electronics Engineers (IEEE) and the IEEE Microwave Theory and Techniques Society.