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Impurity and back contact effects on CdTe/CdS thin film solar cells

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Impurity and Back Contact Effects on CdTe/CdS Thin Film Solar Cells

by

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A dissertation submitted in partial fulfillment
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DEDICATION

I dedicate this research and this Dissertation to my family for their love and support.

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ABSTRACT

CdTe/CdS thin film solar cells are the most promising cost-effective solar cells. The goal of this project is to improve the performance for CdS/CdTe devices by improving the open circuit voltage V_{oc} and current density J_{sc}. Efforts focused on increasing the V_{oc}, which include increasing the doping concentration by introducing Phosphorus and Antimony, finding and testing new back contact materials, and varying the ambient of CSS CdTe. In addition, the effect of Zn_2SnO_4 on the cells' performance was also studied.

Electrical characterization of the thin films and completed devices were carried out by Current-Voltage (J-V), Capacitance-Voltage (C-V), and Spectral Response (SR) measurements. Structural/chemical characterization was done by SEM, XRD and EDS analysis.

The ambient of CSS CdTe affects the growth rate, the grain size and electronic properties of CdTe. The N_2/O_2 mixture with varied ratio (N_2/O_2=9/1, 7/3, 5/5 and 1/9) was used in this study. The cells' performance and the net carrier concentration were studied as a function of the N_2/O_2 ratio. The net carrier concentration increases with the increasing O_2 concentration.

The extrinsic impurities (P and Sb) were incorporated into CdTe layer. Phosphorus was directly introduced into CSS CdTe source. The Sb was incorporated into CdTe by a diffusion process. The effects of the annealing parameters, the excess Sb on CdTe surface, the $CdCl_2$ treatment and the depth of Sb in CdTe were studied. Higher doping concentration up to 10^{16} cm^{-3} has been achieved, however, V_{oc} is still in the range of 830 mV.

CHAPTER 1

INTRODUCTION

The evolution of human beings is also the history of finding and using new energy. Utilizing fire to get energy was a big step for man's development. Two thousand years ago, men already learned how to use water to drive machines. Following that was the finding of fossil fuels. The invention of electric power is an important milestone of the evolution of man's use of energy. Since then, almost every kind of energy had to be converted into electric power.

There are various energy sources that have been found and utilized by man. These energy sources have been classified as nonrenewable and renewable energy sources. The nonrenewable energy sources include fossil fuels (used to generate 61% of the world's electric power, 95% of the world's total energy demands), such as coal, oil, natural gas, and nuclear power. The renewable energy sources include solar energy, wind, geothermal, hydropower, etc. Fossil fuels need millions of years to form. The main advantages of fossil fuels are low cost, easily transportable and store. However, burning coal produces sulphur dioxide, which causes acid rain and is harmful to the earth's environment. Burning any kind of fossil fuels will produce carbon dioxide, which is believed to be the cause of the green house effect. Nonrenewability of fossils is its biggest disadvantage. Once we have burned it all, there isn't any more unless you can wait for millions of years.

Nuclear power provides about 17% of the world's electricity. It is a very clean energy source. The main problem or disadvantage of nuclear power is the risk of radioactivity. Nuclear power accidents releasing radioactivity would be a major disaster like that of Chernobyl. The waste is toxic for centuries and there was no safe, permanent storage facility for it until now.

Wind energy is green and renewable. It is limitless, but it is not a stable energy source. It is only suitable for certain special areas. Hydropower doesn't produce harmful byproducts like fossil fuels, so it is a clean energy. The problems and risk caused by hydropower is the dam. The dam can negatively affect the ecosystem where it is built. It is already well developed wherever is suitable to build hydropower plant.

Solar energy is the cleanest energy we can use. Solar energy output could last 10 billion years. Using the photovoltaic effect, solar cell converts solar energy directly into electricity. Edmund Becquerel first discovered the photovoltaic effect in 1839. Thirty-four years later in 1877, the first solar cell made from selenium was invented by W.G. Adams. Before 1954, the development of solar cells was very slow. In 1914, the efficiency was only about 1%. The breakthrough was made by Chapinetc with a 6% efficiency silicon solar cell in 1954. By 1958, the silicon solar cell efficiency had already reached 14%. Now single crystal silicon solar cell efficiency is over 30%. But the single crystal silicon solar cell has its fatal disadvantage: it is expensive compared with conventional electricity. It was only used in space applications and some military related things where reliability is the main concern. In order to decrease the cost, polycrystalline silicon and amorphous silicon solar cells were developed. Hydrogenated amorphous silicon improves light absorption and the bandgap was increased. Hydrogenated

amorphous silicon behaves like a direct bandgap material. The main problem is its instability under light illumination. Besides silicon solar cells, there is another kind of solar cell called thin film solar cells. In 1954, Reynolds [1] reported the first thin film solar cell with a 6% efficiency, the Cu_xS/CdS hetero-junction solar cell. Two main thin film solar cells were widely researched: CIGS and CdTe based solar cells.

CIGS solar cells were developed from CIS. CIS solar cells show high current, but its efficiency is limited by its low bandgap (1.0eV). Researchers added Ga into CIS to open the bandgap to 1.1~1.2eV. So the V_{oc} was increased. The effect resulted in a decrease of current. The efficiency was improved. Usually, CIGS solar cells were made by coevaporation of Cu, In, Ga following the selenization process. CIGS solar cells with 18.8% efficiency have been achieved.

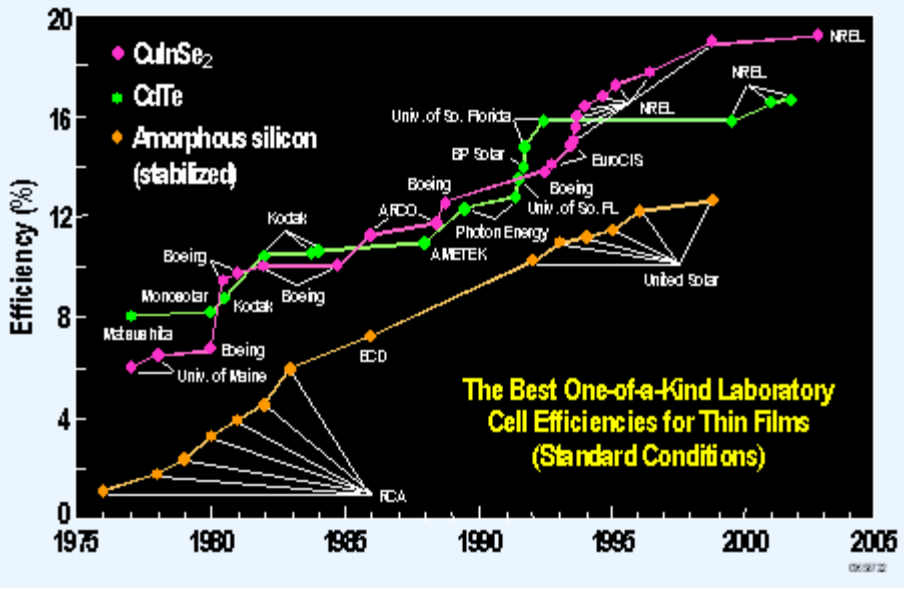


Figure 1 The Development History of Thin Film Solar Cells

CdTe/CdS solar cell is the most promising thin film solar cell. CdTe has nearly ideal band gap of 1.45eV to covert sunlight into electricity. It is a direct band gap material, and the absorption coefficient in visible range is more than 10^5 cm^{-1}, so only a few micrometers thick CdTe can absorb more than 90% of photons with energy above1.45eV. The material cost for solar cells is relatively low compared with Si solar cells, which need a much thicker film. On the other hand, CdTe thin film can be deposited by several low cost methods, such as close-space sublimation, spray deposition, electro deposition, screen-printing, and PVD. All these deposition methods can lead to high efficient devices.

The first CdTe thin film solar cells were prepared by Cusano [2] in 1963 with the structure of CdTe/$Cu_{2-x}Te$. In this structure CdTe was used as n layer and $Cu_{2-x}Te$ as the p layer. The cells have efficiencies close to 6% but not stable. The first CdTe/CdS solar cells were proposed by Andirovich [3] in 1968, but he only achieved 1 % efficiency devices at that time. Due to the energy crisis in early 1970's, more funding was put into the PV research. The progress of CdTe/CdS solar cell is very fast. In 1981, Kodak achieved 10% efficient devices. AveTEK achieved 12% devices in 1990. After 1990, USF, Photon Energy and BP alternatively lead the research. In 1992, Ferekides and J. Britt got 15.8% devices. The record was kept nearly 10 years. Now the world record efficiency is 16.5%, achieved by X.Wu [4] in NREL. Figure 1 shows the development histories of CuInSe2, CdTe and α-Si solar cells [5].

All the reported high efficient CdTe/CdS solar cells rely on a special treatment-$CdCl_2$ treatment [6-12]. It is still not completely understood. Studies show that $CdCl_2$ treatment leads to an intermixing and recrystallization at the interface, the lattice

mismatch is reduced. The carrier lifetime was increased, and the density of interface states is greatly reduced.

There are two main technology issues related to further improve the cells performance. One is to increase the p-type doping of CdTe, the other is to get ohmic contact to p type CdTe. We will talk about them in detail later. Long-term stability and the toxicity of cadmium are the other two main issues. Copper diffusion is considered to be the main reason for the degradation [13-15]. A copper free contact will be the reliever to this issue. As to the toxicity of cadmium, it is not as what people think at first glance. In fact, based on the studies of V. Fthenakis [16-17], most of the cadmium was captured into molten glass under 1000°C fire. It only produces 0.06mg/Gwh emission of cadmium, which is negligible within the context of life cycle analysis. On the other hand, end-of-life or broken modules can be recycled, so any environment concerns will be completely resolved.

After more than 30 years of research and development, the fabrication of PV module technology becomes more mature. There are several CdTe PV module factories in the world, such as Antec, Primestar Solar and First Solar. The average PV module efficiency is 7-9%. There is a big efficiency gap (7~9%) between the lab small cell and the large area PV modules. There is a long road to walk to reduce this gap for the CdTe solar cell to become cost-competitive.

Over the past 20 years, the demand for energy has grown consistently by 10~25% per year. The cost has reduced seven fold due to the progress of technology and the increased market volume. Even though, the electricity from solar cells is still not competitive compared with conventional electricity, if you only consider it from financial

point. Today, many governments recognized the benefit of using solar power. More money has and will continue to be invested on research in this area. This will lead to an increase in the technology's progress. The cost will be reduced further and become competitive with conventional electricity in the not far future. Solar energy will occupy more and more portions of the whole energy demand. The future must belong to renewable energy. Figure 2 shows the growth of PV modules installed in the world. In 2005, 1460 Megawatts of PV were installed. This increased to 1744 megawatts in 2006.

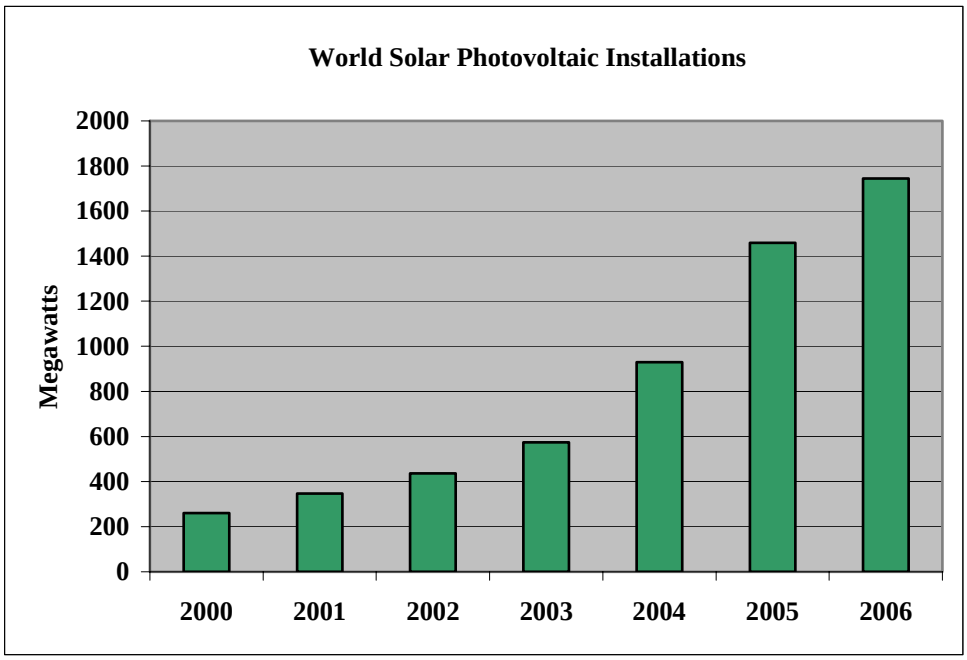


Figure 2 The Growth of PV Modules Installed in the World

CHAPTER 2

SOLAR CELL DEVICE PHYSICS

2.1 Semiconductors

Materials can be classified into three groups based on their conductivity: (1) Conductors, whose resistivity is $<10^{-4}\ \Omega$ m (2) Insulators, whose resistivity is $>10^{12}\ \Omega$ m (3) Semiconductors, whose resistivity is between conductors and insulators. The semiconductors are the corner stone of the modern electronic technologies.

Semiconductors can be classified into P type and N type based on their majority carriers. The most important characteristic of semiconductors is that their conductivity can be modified by adding impurities, which are called dopants. For example, adding one group III element into silicon makes the majority carriers holes and the silicon becomes P type. Adding a group V element into Si makes the majority carriers electrons, silicon becomes N type.

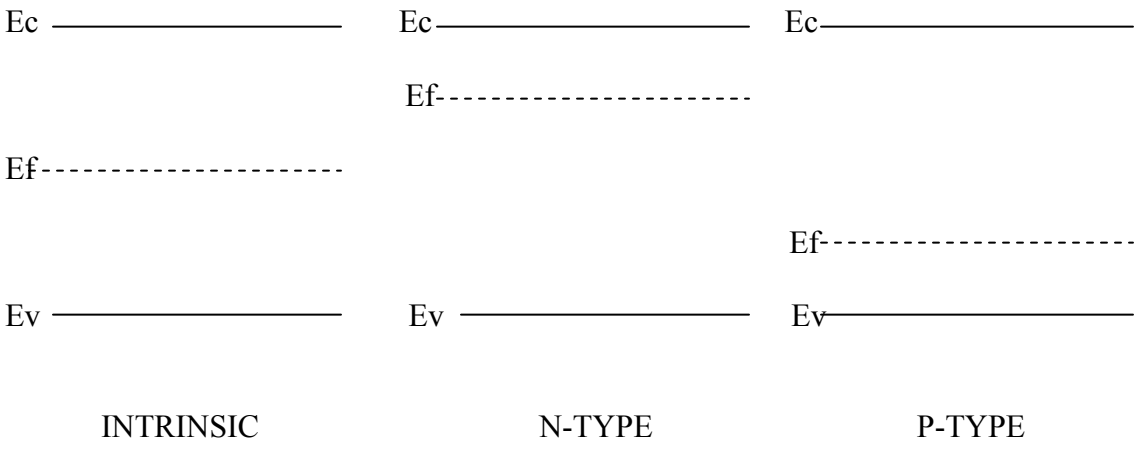


Figure 3 Energy Band Diagrams of Various Materials

There are two important concepts about semiconductors: Fermi energy E_f and bandgap Eg. The Fermi Energy is defined as the energy at which the probability of a state is occupied by an electron is 0.5. The bandgap Eg is defined as the energy difference between the energy of the highest valence band and the energy of the lowest conduction band. In this energy gap, no allowed energy states can exist.

2.2 PN Junction

For P type material, the majority carriers are holes. For N type material, the majority carriers are electrons. When these two types of materials contact with each other, a PN junction is formed. Because of the concentration gradient, the electrons diffuse into the P side and recombine with holes near the junction, while holes diffuse into the N side and recombine with electrons near the junction. The diffusion movement of these carriers forms the diffusion current. Adjacent to the PN interface, there are no free carriers on both sides. This region is called the depletion region (also called space charge region (SCR)). The result of the diffusion leads to the build up of positive charge on the N side and negative charge on the P side, and an internal electric field is established. This internal electric field tries to drift holes back to the p side and electrons back to the n side which led to the formation of drift current. Without any bias, the drift current is equal to the diffusion current, so the net current is zero. A flat Fermi level is established. Figure 3 shows the energy diagram for P type and N type material. Figure 4 shows the PN junction band diagram at equilibrium. V_{bi} is the band bending, called built-in potential, and can be expressed as the following equation:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{1}$$

Where N_A and N_D are the doping concentrations in the P and N type semiconductors, n_i is the intrinsic carrier concentration, k is Boltzmann's constant, and T is the absolute temperature.

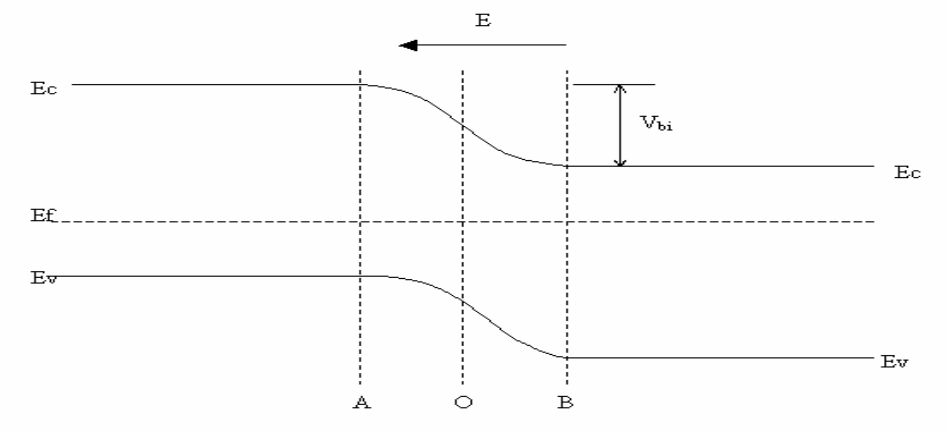


Figure 4 The PN Junction Band Diagram at Equilibrium

When a bias is applied across a PN junction, the equilibrium state is broken. When a positive terminal is connected to P side, the bias is called a forward bias; otherwise, it is a reverse bias. Figure 5 shows the forward and reverse biased band diagram. The current-voltage relationship of a biased PN junction can be expressed as:

$$J = J_0\left(\exp\left(\frac{qV}{AkT}\right) - 1\right) \tag{2}$$

Where J_0 is the reverse saturation current, and A is the diode factor.

2.3 Heterojunction

From the band structure shown in Figure 4, you can see that the materials on both the P and N side are identical. This kind of PN junction is called homojunction. There is another kind of PN junction called heterojunction. In a heterojunction, the material on the P side is different from that on the N side. Heterojunction can be classified as isotype

heterojunction, in which the two semiconductors have the same type conductivity; and anisotype heterojunction, in which the two semiconductors have the different type conductivity. CdTe/CdS thin film solar cells are anisotype heterojunctions. Figure 6 shows the energy band diagram of n type material and p type material without contacting each other. E_{GN} and Eg_P are the bandgaps, χ_P, χ_N are the electron affinities, and F_N and F_P are the Fermi levels. δ_n and δ_p are the displacement of the Fermi level from the conduction band edge and valence band edge in the n type and p type semiconductors.

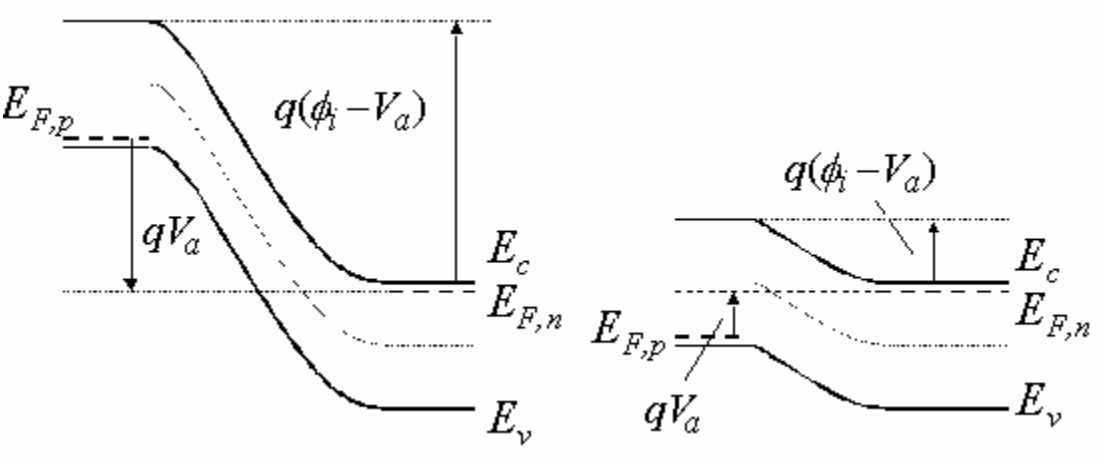


Figure 5 The Forward(right) and Reverse Biased (left)Band Diagram

Due to the different materials' properties, there are discontinuities called band offset in the conduction band and in the valence band. The conduction band offset can be defined as $\Delta E_c = \chi_P - \chi_N$. The valence band offset can be defined as $\Delta E_v = \left(E_{gp} - E_{GN} - \Delta E_c\right)$. ΔE_c can also be calculated as $\Delta E_c = \left(V_D + \delta_n + \delta_p - E_{gp}\right)$. Since χ_P, χ_N, E_{gp}, E_{GN} are independent of doping for nondegenerate semiconductors, so ΔE_c and ΔE_v are invariant for nondegenerate material. For an abrupt one-sided junction, V_D can be obtained from the capacitance measurement. Once the V_D is obtained, ΔE_c and

ΔE_v can be obtained using the aforementioned equations. When n type material contacts with the p type material, because F_N is higher than F_P, some electrons must flow from the N side to the P side, resulting in up band bending for the N side and down band bending for the P side near the junction. Figure 7 shows the heterojunction band structure after the junction formation. Compared with a homojunction, the band structure is much more difficult to calculate because of the discontinuity and the interface state. The first and most popular model is proposed by Anderson [18]. In this model, Anderson considers the material properties such as dielectric constants, electron affinities and energy gaps. In this model, the current flow is entirely by injection over the conduction or valence band barriers. The current has the form:

$$I = A\exp(-qV_{bp}/kT)[\exp(qV_p/kT) - \exp(-qV_n/kT)] \quad (3)$$

Where $A=XaqN_DD_n/L_{n,}$ V_{bp} is the band bending on the p side of the junction, V_p and V_n are applied voltage dropped on the p and n side of the junction. Further studies show that current-voltage behavior with temperature of most heterojunctions doesn't conform to equation 3. This is because Anderson's model doesn't consider tunneling and recombination effects. Later several models were proposed for recombination current, or tunneling current, or the combination of these mechanisms. Dolega proposed the recombination model assuming a lifetime approaching zero at the interface. The current is proportional to exp(qV/Akt), where A is the diode factor and depending on the ratio of the impurity concentration. Riben developed the tunneling current model. The tunneling current has the form: $J=J_0\exp(\partial K_pV)$, where $J_0=BXN_t\exp(-\partial V_b)$, where N_t is the density of available tunneling states, B is a constant, and X is the transmission coefficient for electrons to cross the interface.

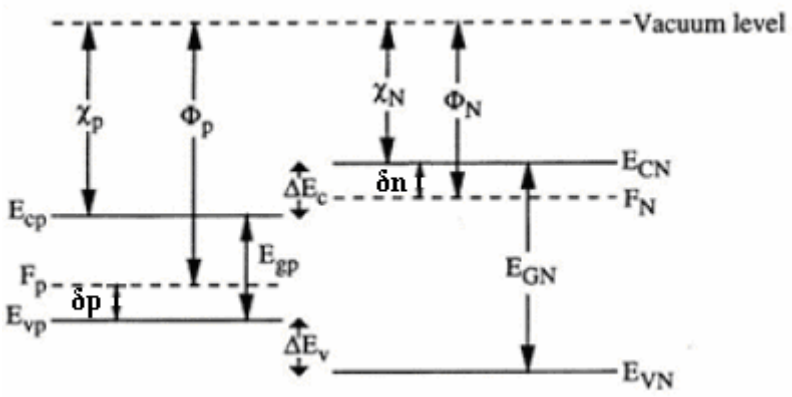


Figure 6 Energy Band Diagram for Two Isolated Semiconductors

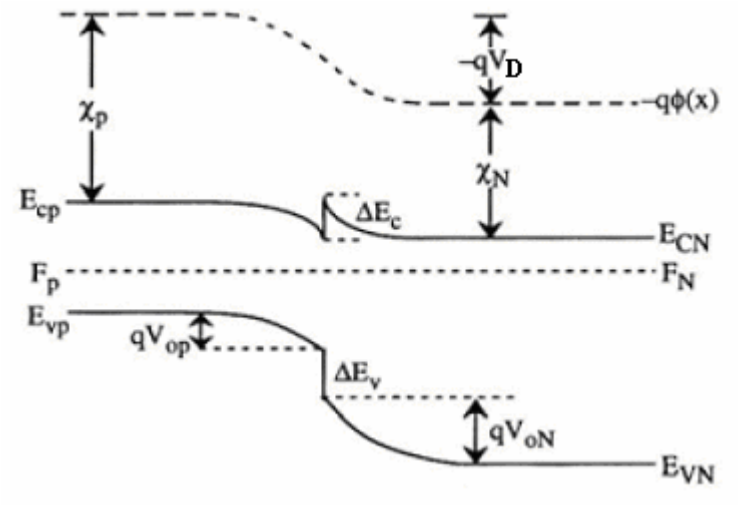


Figure 7 Energy Band Diagram for A Heterojunction at Thermal Equilibrium

The most important advantage of heterojunction devices is that the surface–recombination losses and sheet-resistance losses are greatly reduced due to the deep junction position. A special property of the heterojunction is that it makes it possible to use some materials which can only be doped either p-type or n-type to make solar cells. Without this constraint, many promising PV materials can be investigated to produce optimal cells. The window material can be made highly conductive, light-generated

electrons can easily flow laterally in the window layer to reach an electrical contact. Also, the window layer band gap can be wider than the absorber layer, allowing more light to be absorbed in absorber layer.

Most of the heterojunction solar cells have the structure of n type wide gap material and p type narrow gap material. One reason of selecting this structure is that most heterojunction pair's ΔE_c is considerably less than ΔE_v, so the barrier for electrons flowing from p side to n side is lower. The second reason is that most of the current is caused by electrons from p type narrow gap material, and the diffusion length of electrons is longer than that of holes.

Of course, heterojunction devices have their own problems like lattice mismatch and the discontinuity of electron affinity, which can produce interface states. The interface states act like recombination centers and should be minimized. Chemical compatibility, thermal expansion coefficient and long term stability are the other concerns.

The typical band structure of a CdS/CdTe solar cell is shown in figure 8. ΔE_c is a little bit less than or close to zero. The negative value usually calls cliff. There exists a back barrier due to the insufficient work function of the contact material. The conduction band discontinuity does not limit the electron photocurrent from CdTe to CdS. The hole photocurrent from CdS to CdTe is not limited either by the valence band discontinuity. James sites simulated the effect of ΔE_c [19]. He found that even a small spike ΔE_c could limit the ability to increase V_{oc} with band gap. Photons with energy $E< 3.5$ eV (355 nm) will pass through the SnO_2 layer. Part of photons (~30~60%, depending on the CdS thickness) with energy $2.43 \text{ eV}<E<3.5$ eV are absorbed by CdS. Most light with energy

1.45 eV<E<2.43 eV is absorbed by CdTe resulting in electron-hole pairs that produce the photo current. The light was absorbed by CdS doesn't contribute to the photocurrent. As a result, the CdS thickness should be minimized.

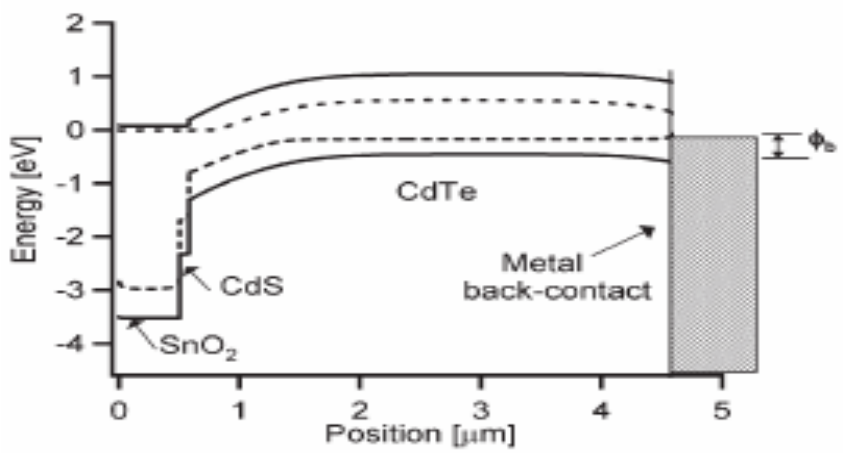


Figure 8 The Ideal Band Diagram at The CdS/CdTe Interface

2.4 Metal-Semiconductor Contacts

All semiconductor devices have contacts. They may be semiconductor – semiconductor contacts or metal- semiconductor contacts. Metal contacts are most common. This type of contact can be an ohmic or Schottky contact, depending on the relation of the work function and surface state.

2.4.1 Schottky Contact

Figure 9 shows the band diagrams of metal and the semiconductor (n type) before and after contacts. The work function is defined as the energy difference between the vacuum level and the Fermi level. The metal work function Φ_m is greater than the work function of the semiconductor in Figure 9. When the two solids contact each other, the more energetic electrons in the semiconductor can readily tunnel into the metal to occupy

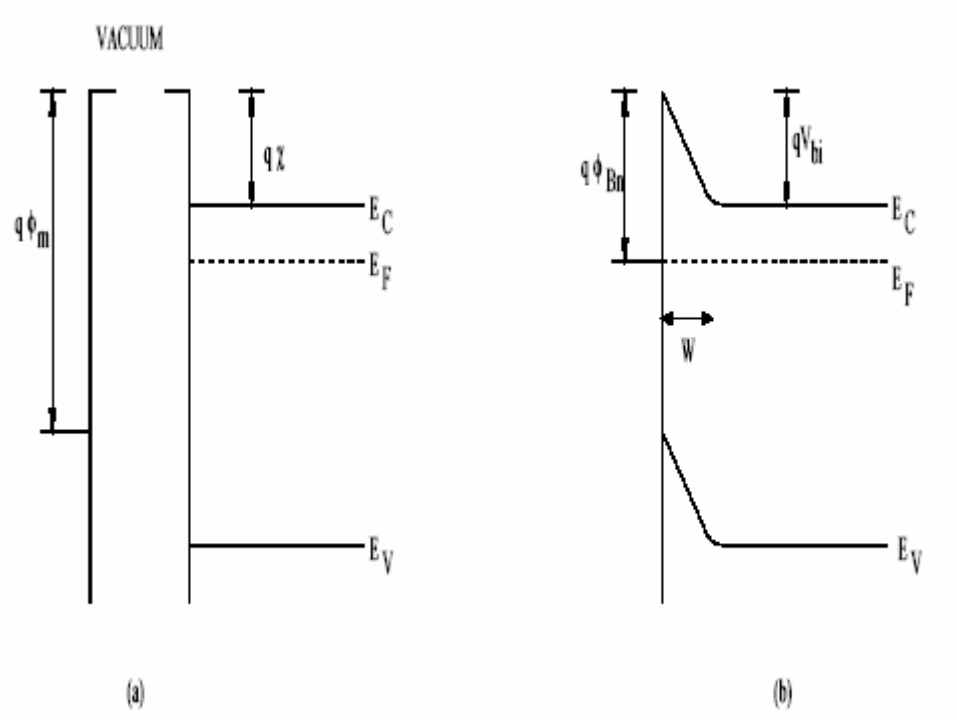


Figure 9 Energy Band Diagram for Metal-Semiconductor Contact (A) Before Contact (B) After Contact

lower energy levels, and accumulate near the metal surface, leaving behind an electron-depleted region near the junction. In the depletion region, the right side is positively charged donors, a built-in electric field pointing to the metal surface is developed. Finally this built-in potential prevents further accumulation of electrons at the metal surface. At this point, equilibrium is established. The Fermi level throughout the whole solid is uniform. In the depletion region, electrons are depleted, so the energy band must bend up toward the junction. The band bending creates a barrier for electrons moving from metal to semiconductor. This barrier height is given by

$$\Phi_B = \Phi_M - \chi \tag{4}$$

Where χ is the electron affinity of the semiconductor. In practice it is very difficult to change the barrier height by varying metal work functions. It is observed that the barrier

height for some semiconductors is almost independent of the work function of the metal. This phenomenon can be explained by surface states. If the density of surface states is high enough, the barrier height is pinned at some energy. The surface states may be dangling bonds at the surface or some other types of defects. They play an important role for contact formation.

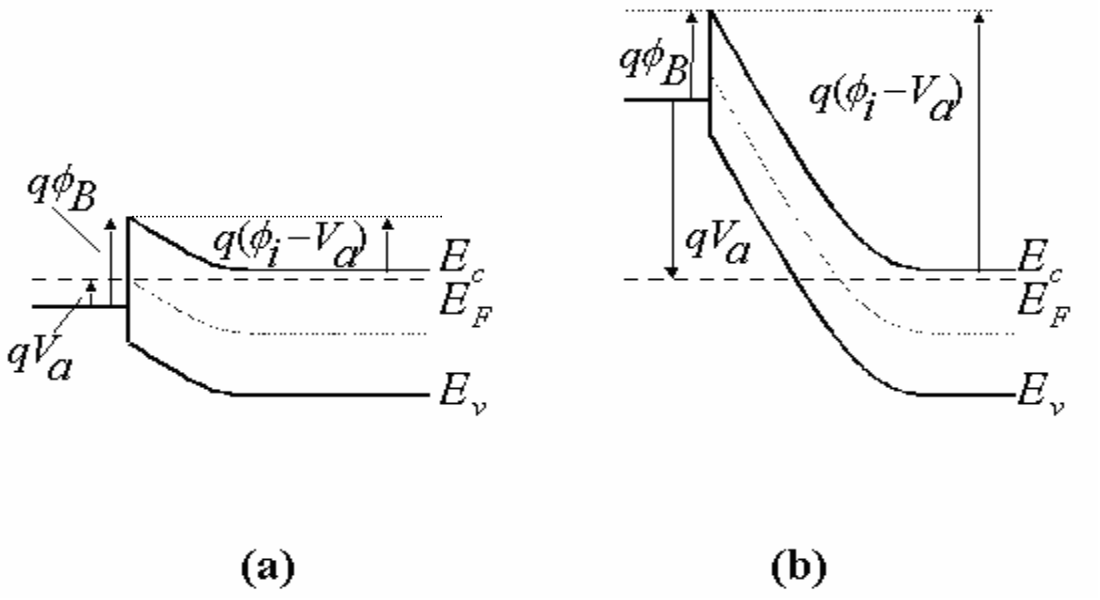


Figure 10 Energy Band Diagram of A Metal-Semiconductor Junction under (A) Forward Bias (B) Reverse Bias

When a Schottky junction is in an open circuit condition, the net current is zero. When it is reverse biased, the width of the depletion region is increased. Figure 10 shows the energy band diagram of a metal-semiconductor junction under forward bias and reverse bias. The barrier for electrons from semiconductor to metal is increased to $V_{bi}+V_R$, so the current from semiconductor to metal will decrease exponentially with V_R. The current is essentially limited by the current from metal to semiconductor. When the junction is forward biased, the barrier for electrons from semiconductor to metal is

decreased to V_{bi}-V_F. The current is primarily limited by this current, which is exponentially increased with V_F.

2.4.2 Ohmic Contact

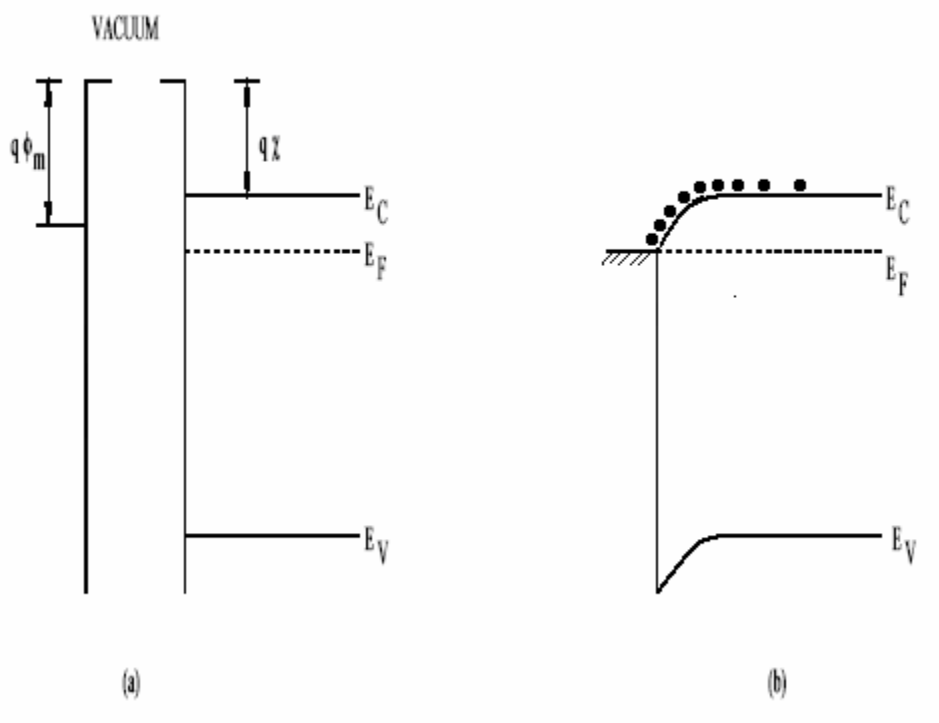


Figure 11 Band Structure of Ohmic Contact (A) Before Contact (B) After Contact

Figure 11 shows the band diagrams of metal and n type semiconductors before and after the contact. In this figure, the metal work function Φ_m is lower than the work function of semiconductor. The electrons in metal will tunnel into the semiconductor to seek lower energy levels. Electrons will accumulate in the semiconductor near the junction, and the band has to bend down to increase the electron concentration near the junction. So from the metal to the end of semiconductor side, there are always conduction electrons, meaning it is conductive throughout the whole solid. There is no barrier for electrons in either direction because the metal and the accumulation region have more

electrons compared with the bulk of the semiconductor. The current is mainly limited by the bulk resistance of the semiconductor. Here the ohmic contact doesn't mean linear I-V characteristics. It could be linear or quasi-linear. For a P-type semiconductor, the work function of metal has to be greater than the work function of the semiconductor to achieve ohmic contact.

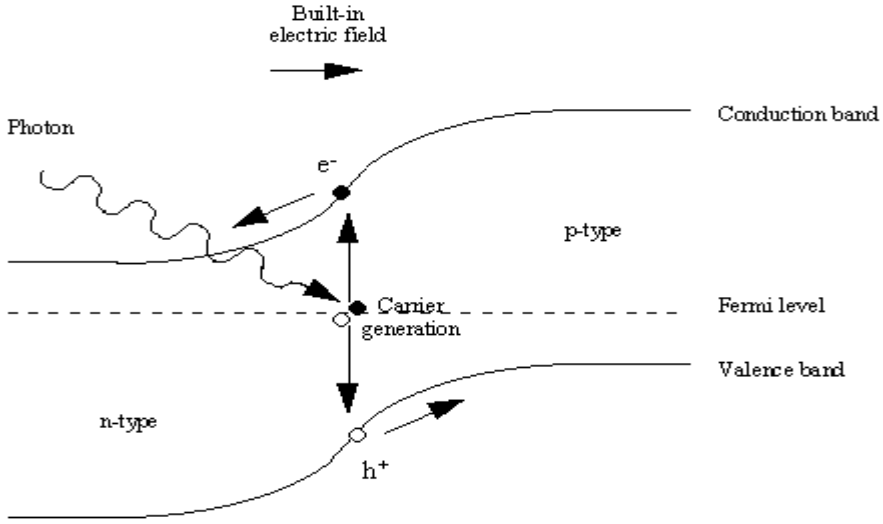


Figure 12 The Band Structure of Solar Cells

2.5 Solar Cells

A solar cell is a device that converts sunlight into electricity using the photovoltaic effect. Figure 12 shows the principle of the photovoltaic device. When sunlight strikes on the solar cell, the photons with energy greater than the absorber bandgap are absorbed to produce electron-hole pairs. The excess energy over Eg just wastes as heat. The photons with energy less than the bandgap will pass through the device and make no contribution to the cell output. The generated electron-hole pairs are transported to the junction region and separated by the built-in electric field of the

junction. Based on this mechanism, to achieve a high performance solar cell, several requirements must be met: (1) A large absorption coefficient, so only a thin film is enough to absorb most light. For CdTe, a 2μm thick film is enough to absorb more than 90% of the photons with energy above its bandgap. Since the absorber layer is very thin, the requirement of high quality materials is released. (2) An appropriate band gap. This means

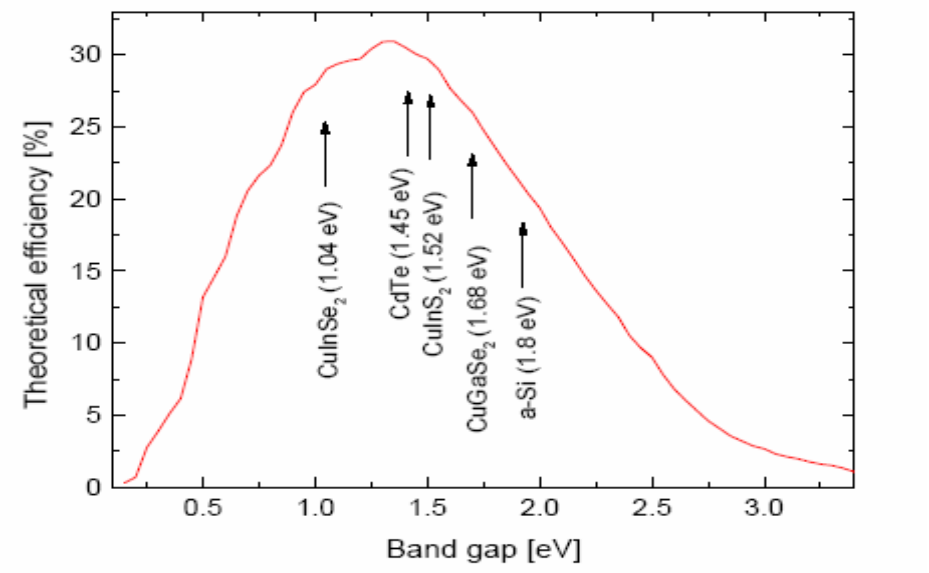


Figure 13 Theoretical Efficiency for A Given Band Gap (AM 1.5 Illumination)

the bandgap shouldn't be too large or too small. Theoretical ideal bandgap for solar cells is 1.28 eV. If it is large, most of the light will pass through the absorber layer leading to a high V_{oc} and a low J_{sc}. If it is too small, most part of the energy will be wasted as heat. The CdTe's bandgap is 1.45 eV. It is almost ideal. The theoretical maximum efficiency is 29.2% with V_{oc}=1.07 V, FF=89% and J_{sc}=29.5 mA/cm^2. Figure 13 shows the theoretical efficiency—bandgap relationship. (3) A low resistance ohmic contact, so most of the separated carrier can be transported to outside load device.

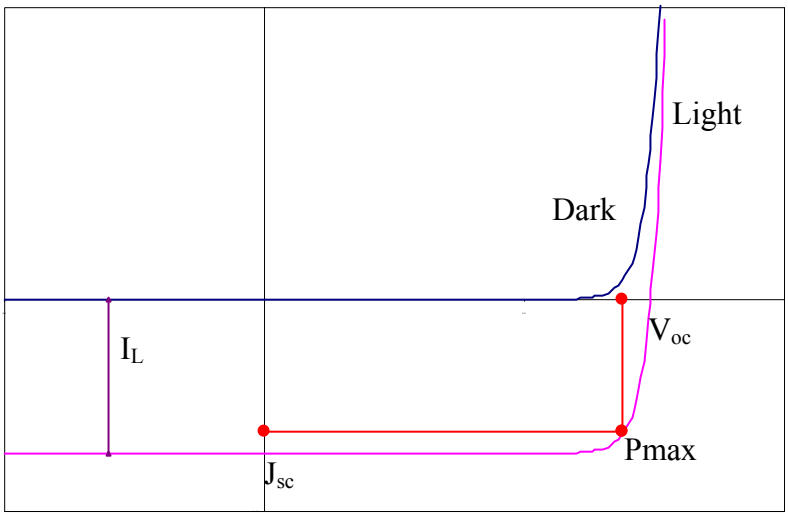


Figure 14 I-V Characterizations for Ideal Solar Cell in The Dark and Under Illumination

2.5.1 Basic Parameters

Whenever we evaluate a solar cell's performance, we always use the conversion efficiency. It is defined as the ratio of the maximum output electrical energy and the input light energy and is given by:

$$\eta = \frac{P_{max}}{P_{in}} \tag{5}$$

Where P_{max} is the maximum output electrical power, P_{in} is the incident light energy. In the laboratory, the light simulator is calibrated to $0.1 W/cm^2$, and the efficiency becomes:

$$\eta = P_{max} = V_{max} \times J_{max} = V_{oc} \times J_{sc} \times FF \tag{6}$$

Where V_{oc} is called open circuit voltage in Volt. It is the output voltage when the load has infinite resistance. J_{sc} is called short circuit current in mA/cm^2, when the load circuit is shorted. V_{max} and J_{max} are the voltage and current where the output power is maximum. FF is called fill factor, it is defined as the follow:

$$FF = \frac{V_{max} J_{max}}{V_{oc} J_{sc}} \tag{7}$$

From equation 6, in order to get higher conversion efficiency, the device must have higher V_{oc}, J_{sc} and FF.

Figure 14 shows the typical J-V curve of ideal solar cell measured both in the dark and under illumination. I_L is the current produced by light generated electron hole pairs separated by the electric field.

One should note that the current density from the J-V curve is not as accurate as the one calculated from the spectrum response due to the imprecise area measurement. Figure 15 shows the typical spectral response of a CdS/CdTe solar cell. It shows quantum efficiency varies with the wavelength. Basically, quantum efficiency is defined as the ratio of the collected electrons to the incident photons at each wavelength.

$$SR(\lambda) = \frac{J_L(\lambda)}{qF(\lambda)(1 - R(\lambda))} \tag{8}$$

Where J_L (λ) is the photo generated current as a function of the wavelength, F (λ) is the number of incident photons, and R (λ) is the reflected photons by the surface. If we take the derivative of function 8 with respect toλ, we get:

$$\frac{d J_L}{d\lambda} = qSR(\lambda)\frac{d(F(\lambda)(1 - R(\lambda)))}{d\lambda} \tag{9}$$

If the SR (λ) is known, the exact photocurrent density can be obtained by the integration of the right side of the equation from 0 to the maximum corresponding to the absorber bandgap. In ideal case, the SR should be 1, but in practice, it is usually less than 1. The loss due to reflection is usually 5%. In Figure 15, the main loss is due to the absorption of TCO and CdS.

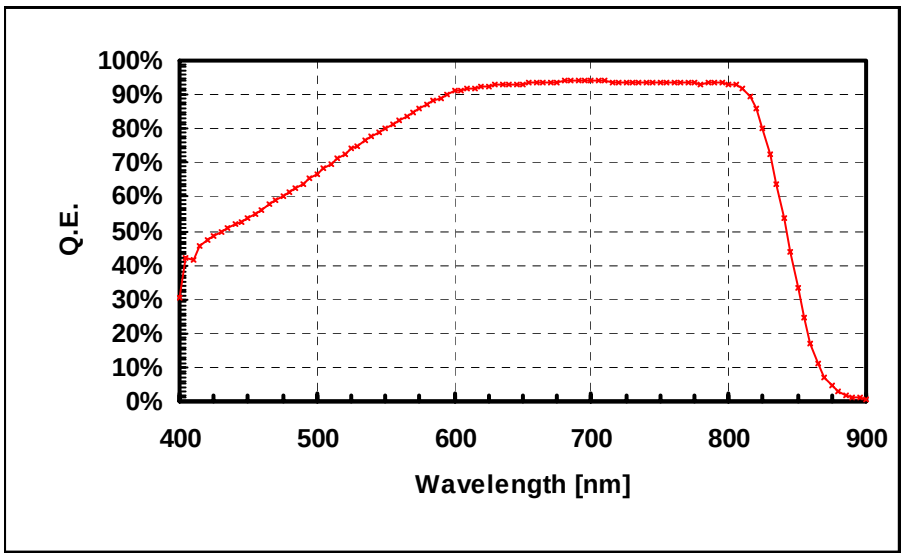


Figure 15 Typical Spectral Response of CdS/CdTe Solar Cells

Figure 16(a) shows the equivalent circuit of an ideal solar cell which has zero series resistance and infinite shunt resistance. For practical solar cells, R_s is not zero and R_{sh} is not infinite. Figure 16(b) shows the equivalent circuit of a solar cell with nonzero R_s and finite R_{sh}. For an ideal solar cell, from Figure16, the current-voltage relationship can be given by:

$$I = I_0\left[\exp\left(\frac{qV}{AkT}\right)-1\right]-I_L \tag{10}$$

Set V=0, we get $I_{sc}= I_L$

$$\text{Set I=0, we get } V_{oc}=\frac{AkT}{q}\ln\left(\frac{I_{SC}}{I_0}+1\right) \tag{11}$$

Where I_0 is reverse saturation current and k is the Boltzmann's constant.

When we take into account the R_s and the R_{sh} (Frequently they are assumed to be constant, but they may be light sensitive and time variant), equation 10 becomes

$$I = I_0\left(\exp\left(\frac{q(V-I\,R_s)}{AkT}\right)-1\right)-I_L+\frac{I_L+(V-I\,R_{sh})}{R_{sh}} \tag{12}$$

Equation 11 doesn't change. So we can say series resistance doesn't affect V_{oc} and reduces the short circuit current. It reduces the maximum power available from the device. The series resistance consists of the bulk resistance of the semiconductor, the bulk resistance of the contacts, and the contact resistance between the contacts and the semiconductor. Several methods have been used to determine R_s, such as dV/dj at forward

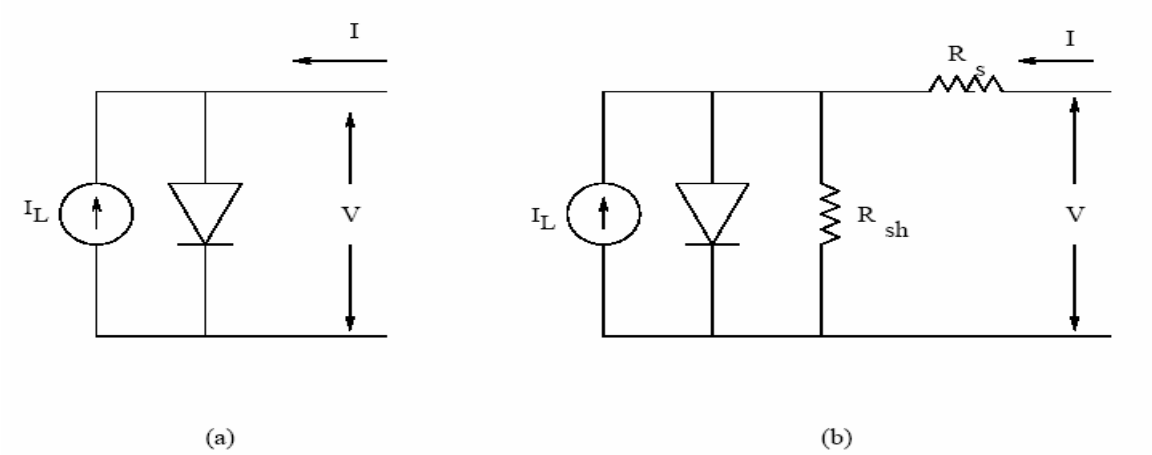


Figure 16 The Equivalent Circuit of A Solar Cell (A) Ideal Case (B) With Series and Shunt Resistance Case

bias (Used in this dissertation), multiple light intensities, constant light intensity, and $\frac{dV}{dI}$ versus $\frac{1}{I}$ plot, etc..

Here we discuss the $\frac{dV}{dI}$ versus $\frac{1}{I}$ plot method in detail. From equation 12, we can get:

$$\frac{q}{AkT}(V - I R_s) = \ln\left(\frac{I + I_L}{I_0} - \frac{V - I R_s}{I_0 R_{sh}} + 1\right) \tag{13}$$

Usually R_{Sh} is very large, so $\frac{V - IR_s}{I_0 R_{sh}}$ can be neglected. Equation 12 becomes:

$$\frac{q}{AkT}(V - I R_s) = \ln\left(\frac{I + I_L}{I_0} + 1\right) \tag{14}$$

From equation 14, we get

$$V = I R_s + \frac{AkT}{q}\ln\left(\frac{I + I_L}{I_0} + 1\right) \tag{15}$$

We take the derivative on both sides.

$$\frac{dV}{dI} = R_s + \frac{AkT}{q}\left(\frac{1}{I}\right) \tag{16}$$

If we plot $\frac{dV}{dI}$ versus $\frac{1}{I}$, the intercept with the y-axis will be R_s, and from the slope we can get the diode factor A. Usually A is about 1-2, and it is voltage dependent. Usually the second term is small compared with R_s and can be neglected, so we can roughly get the R_s from dV/dJ. This is what we used in our lab. More accurate R_s can be determined from multiple light intensities I-V measurement. This method is independent of I_0, A and R_{sh} and no limiting approximation, so the result is generally considered to be close to the real value.

If there are leakage paths across the junction, part of the current will be bypassed by these paths, resulting in the reduction of shunt resistance. The pinholes and grain boundaries can lower the shunt resistance. The FF and V_{oc} will be decreased with decreasing shunt resistance. We can get shunt resistance by taking the reciprocal of the slope of the J-V curve at the high reverse bias region.

CHAPTER 3

IMPORTANT ISSUES FOR CDTE SOLAR CELLS

3.1 Back Contact Effect

One of the most important issues for CdTe solar cells is it is very hard to get a good ohmic contact on p-type CdTe. This is because p-type CdTe has a high electron affinity (4.5eV) and a large band gap (1.45eV), so its work function is nearly 5.9eV. From contact theory, in order to get a barrier free contact, the work function of the metal must be greater than the work function of the p-type CdTe (5.9eV). But unfortunately, there is no such metal that satisfies this requirement. In practice, there are three strategies to get a good ohmic contact. First is etching CdTe to adjust and control surface stoichiometry. Etching can be classified as wet and dry etching based on the medium used. For wet chemical etching, two types of solutions are usually used. One is an acid solution, such as $7K_2Cr_2O_7{:}3H_2SO_4$, $K_2Cr_2O_7{:}HNO_3{:}H_2O$ [91], and $HNO_3{:}H_3PO_4{:}H_2O$ [92], the other one is Br_2 /CH_3OH. Dry etching can be classified into plasma etching, reactive ion etching and physical sputtering. The advantages of dry etching include: capability of anisotropic etching, eliminating handling, consumption and disposal of large amounts of liquid solvents used in wet chemical etching, and easily integrated into the production line. But the surface could be contaminated by redeposition of non-volatile species, and damaged by high-energy particles' bombardment. The second way is heavily doping the CdTe surface to produce a p+ layer; the barrier between CdTe and the

contact will be narrowed so that free carriers can tunnel freely through the barrier, such as Au-Cu, Au-Li and Au-P. The third is using another high electron affinity, high conductivity p-type semiconductor as a buffer layer, which contacts can be made more easily, such as HgTe and ZnTe.

Currently, different kinds of back contacts have been achieved, they can be classified into two categories: copper containing back contacts and copper-free contacts. Copper-free contacts include Ni-P, Sb_2Te_3, Mo, and HgTe. Copper-containing contacts include Au-Cu alloy [20, 21], ZnTe:Cu [22, 23], HgTe:Cu doped graphite paste [24, 25], and Cu_2Te [26, 27]. All of these kinds of contacts contain an elemental form of Cu or Cu compound. Copper is a fast diffuser. In a single crystal CdTe, Cu is considered to exist in the forms: Cu_i^+ and Cu_{cd}^-. Cu_i^+ is a shallow donor with activation energy 55 emV. Cu_{cd}^- is a deep acceptor with activation energy 0.28~0.34eV. Copper can also form a complex ($Cu_i^+ + V_{cd}^{-2}$, $Cu_i^+ + Cu_{cd}$). H.C. Chou's studies show that Cu plays dual roles in CdTe solar cells [93]. The good one is that it is giving a good ohmic contact by increasing the p doping near back contact. The best cell with the world record efficiency (16.5%) utilized a copper containing back contact. The negative effect is the migration of Cu from back contact to the main junction. It is responsible for degradation of long term cell performance.

Due to the stability problem caused by Cu, Copper-free back contacts have gained increased attention. Several materials have been studied, such as Sb_2Te_3, $VeSe_2$, and TiSe2 [32]. Sb_2Te_3 and Ni_2P have shown promise as back contacts to CdTe solar cells [28-31].

B.Ghosh et al. used electroless deposition Ni-P for contact fabrication to CdTe [28]. They found the optimum annealing temperature is 250°C. At this temperature, Ni_2P becomes more prominent. It is believed that the work function of this phase is similar as gold resulting in better contact properties. Above 250°C, the contact resistance is increased.

The group at USF used Ni_2P powder mixed with graphite paste to fabricate back contact to CdTe and demonstrated Ni_2P as a very promising candidate as a back contact material to CdTe [29]. In their study, they studied the effect of various processing parameters, such as annealing temperature, annealing time, and Ni_2P concentration. The best processing parameters they achieved: 25%wt Ni_2P, and 90 minutes annealing at 250°C. The best device has V_{oc} of 834 mV, FF of 70%, and 12% efficiency.

N. Remeo et al. studied Sb_2Te_3 as a back contact to CdTe [30, 31]. They sputtered Sb_2Te_3 at 300°C with a final layer of sputtered Moly. The resistivity is 10^{-4} Ω-cm. The best cell has V_{oc} of 857 mV, FF of 73% and efficiency of 15.1%. A stability study showed there is no change on cell performance after a 6 month, 1 sun soaking.

D. Kraft et al. studied VSe_2/CdTe and $TiSe_2$/CdTe interface properties [32]. VSe_2 and $TiSe_2$ have high work functions 5.7eV and 5.6eV, respectively. They could form ohmic contacts to CdTe due to their high work functions. In this study, CdTe was deposited on VSe_2 and $TiSe_2$ substrates to form VSe_2/CdTe and $TiSe_2$/CdTe interfaces. They found an excess of Cd exists at the interface due to higher sticking coefficient of Cd atoms. Due to the relatively small work function of Cd (4.22eV), an interface dipole occurs resulting in a vacuum level discontinuity of ΔE_{vac}=0.65eV for CdTe/ VSe_2 and ΔE_{vac}=0.55eV for $TiSe_2$/CdTe. This leads to a nonohmic contact to CdTe. This suggests

that if we can avoid the excess Cd by changing the processing conditions, the ohmic contact could be formed.

3.2 Doping Concentration Effect

From equation 11, $V_{oc} = \frac{AkT}{q} \ln\left(\frac{J_{SC}}{J_0} + 1\right)$, we can see V_{oc} increases with decreasing J_0. J_0 can be given by:

$$J_0 = \frac{qD_p p_{n0}}{L_p} + \frac{q D_n n_{p0}}{L_n} \tag{17}$$

Where L_P, L_n is the diffusion length of holes and electrons, respectively. D_p, D_n is the diffusion coefficient for holes and electrons, respectively. p_{n0} is the equilibrium hole concentration on the n side, given by $p_{n0} = \frac{n_i^{\,2}}{n_n}$. n_{p0} is the electron concentration on the P side, given by $n_{p0} = \frac{n_i^{\,2}}{p_p}$. If carrier concentrations on one side or both sides are increasing, p_{n0} or n_{p0} or both will decrease and V_{oc} will increase. For example, if the doping concentration can be increased one order of magnitude on both sides, V_{oc} could be increased about 90~120mV depending on diode factor A. On the other hand, with the increasing doping concentration, the surface recombination effect will become weaker and practically become eliminated when it is more than 10^{16} -10^{17} cm^{-3}. The recombination losses in space charge region will also decrease due to the increasing of the electric field with the increasing doping concentration. The collection will be improved, resulting in an increased FF.

3.2.1 Doping Limit

As we talked earlier, semiconductors resistivity is between conductors and insulators. In order to lower the resistivity, doping concentration must be high enough. For some semiconductors, it is not a very easy task. Some semiconductors can be doped as high as 10^{21} cm^{-3} in both p type and n type. Some semiconductors can be doped with very high concentration in only p type or only n type, and are not dopable in the other type. Some can be doped in both type but with low concentration. CdTe is the only one II-VI compound that can be doped relatively easy p type and n type. But doping ability is not same for n type and p type doping. For p type doping, the hole concentration becomes limited at 10^{17} cm^{-3}. For polycrystalline CdTe, the hole concentration is even lower due to boundary effects.

To obtain high doping concentration, three requirements must be satisfied. First, the solubility of the dopant must be high enough. For example, if you want to obtain $10^{21}cm^{-3}$ doping concentration, the solubility in that semiconductor must be $>=10^{21}$ cm^{-3} and these dopant atoms have to be at right place, generally in the substitution position. Second, the formation energy levels have to be low enough so that dopants can be easily ionized at normal operation temperatures to provide free carriers. Third, the incorporation of dopants in crystal must not spontaneously induce the oppositely charged defects or defect complexes to compensate the intentional dopant.

Several mechanisms have been proposed for explaining the doping limit. Sometimes one mechanism can explain the experimentally observed doping problems for one specific material, but not suitable for other materials. Sometimes two or more mechanisms have to combine together to explain the specific problem. What property of

material plays the main role to determine the doping limit? Can we predict it? The answer is yes, maybe it is not 100% right, but at least the trend can be predicted. This is the so-called phenomenon logical doping limit model. This model was first developed for III-V compounds by W. Walukiewicz [32-35], and then further developed for II-VI compounds by. W. Faschinger et al. [36-37] and S.B. Zhang et al. [38]. This model tries to predict the doping limit in semiconductors without knowing any compensating mechanism. It uses the conduction band minimum E_C and valence band maximum E_V, the vacuum energy level to determine Fermi stabilization energy levels. $E_{SI,\,p,n}$. At this level, the new creation of defects doesn't

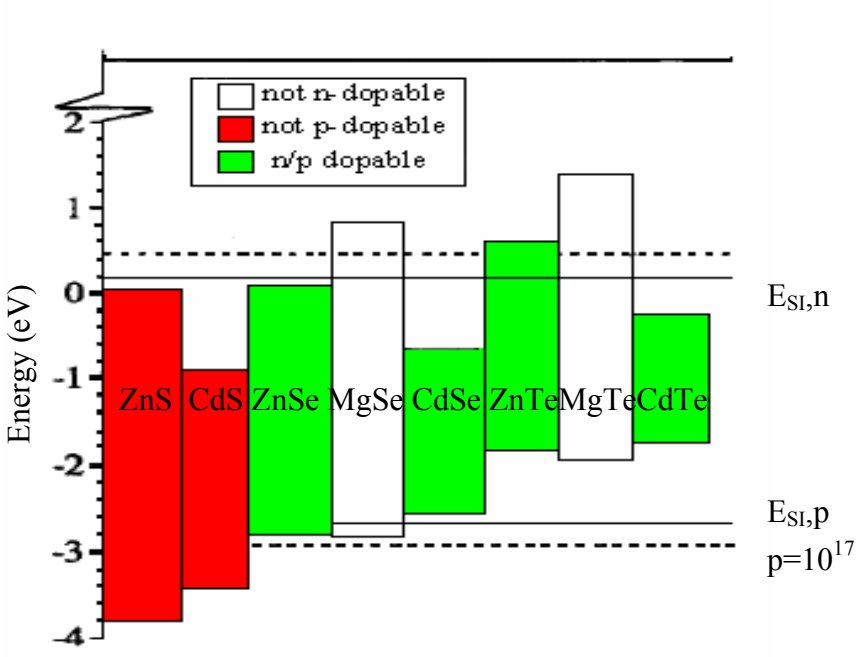


Figure 17 Relative Band Edge Positions of Various II-VI Compounds

change the free energy of the material, the Fermi level was pinned there, so the doping level cannot be beyond that level. For p type doping, the maximum doping is achieved when E_F is equal to $E_{SI,\,p}$. In the same way, the maximum n doping is obtained when E_F is

equal to $E_{SI,\ n}$. The model predict that material with high electron affinity are relatively easy to be doped as n type, while materials with low E_v will be difficult to be doped as p type. Figure 17 shows the relative band edge positions of various II-VI compounds and calculated $E_{SI,\ p,n}$. From this Figure, we can see that CdTe is the only II-VI compound that can be doped as n and p type. ZnS and CdS can't be doped as p type.

The ratio of concentrations between compensation defects N_{comp} and active doping concentration N_{active} is given by:

$$N_{comp} / N_{active} = \exp\left(-2\left(E_F - E_{SI,p,n}\right)\right) \tag{18}$$

Where $E_{SI,p,n}$ is constant with respect to the vacuum level for all compounds as long as the compensation mechanism is the same. But Y. Marfaing [39] showed that $E_{SI,p,n}$ depends on the material properties and compensation mechanism.

3.2.2 Doping Limitation Mechanism

3.2.2.1 Self-compensation

Self-compensation is defined as the intentional dopants were deactive by the spontaneous formation of native defects or spontaneous change of the position of dopant atom. Native point defects include native vacancies, native interstitials, and native antisites. Native point defects are the most widely accepted as the main cause for the doping limit. These native defects could be introduced during the crystal growth or by the post heat treatment. For wide band gap material, it is energy favorable to the formation of compensating defects, because the recombination of free carriers from dopants with oppositely charged compensation defects will lower the total energy of the crystal.

G. Mandel et al. [40] first proposed the self-compensation by spontaneous formed native vacancies. His prediction for n-ZnTe, n-CdTe and n GaAs is well in agreement with the experimental results. Later studies show that the number of possible native defects is much less<=$10^{16}cm^{-3}$. For the doped II-VI compounds, a high concentration of vacancies was observed by some researchers, but detail analysis showed they are dopant-vacancy pairs, not isolated vacancies.

U. V. Desnica [41] calculated the doping efficiency limited by native vacancies compensation showed in Figure 18. In his calculation, he used Phillips-Van Vechlen's two bands theory to calculate the vacancy formation energies and enthalpies. The calculated doping efficiency exactly followed the trend observed in experiments. We can also see that n type doping becomes easier and p type doping becomes more difficult with the increasing of the ratio of the atom size between II-VI group elements. This can be explained by the following: The formation energy of vacancy depends on the size of the vacancy. The larger the ratio, the bigger the ratio of the concentrations of the donor-like native vacancies to the acceptor-like native vacancies, leading to easier n doping. But the calculation is not sufficient to explain the extent of the experimentally observed doping problem. This indicated that the isolated vacancies are not the only reason for doping problem.

Native interstitials and antisites are the other two kinds of defects that could limit the doping effect. Up to today, there are no positive experimental results that can prove they play important roles for the doping limit in II-VI compounds.

The formation of dopant-native vacancy complexes is another kind of self-compensation. There are a number of experimental results in II-VI compounds that could

be explained by the dopant-native vacancy pairs. This self-compensation mechanism well explained the experimental results for In doped CdS [42], N doped ZnSe [43], n type ZnSe [44] and In doped CdTe [45]. It looks like it plays an important role for the doping limit.

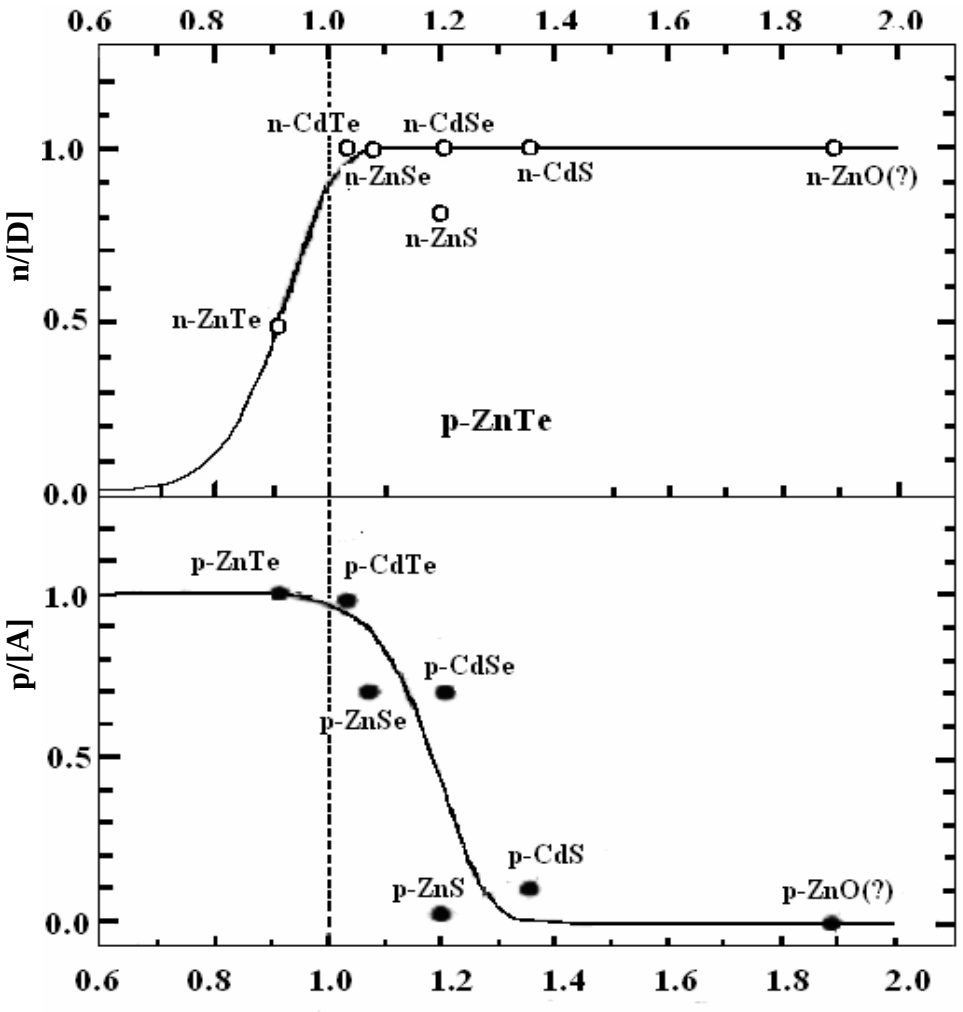


Figure 18 Calculated Maximum Doping Efficiency Limited by Self-Compensation with Native Vacancy

Dopant atoms usually have a different site and a different charge state. These dopant atoms disturb the periodicity of the crystal structure. If the disturbance is strong

enough, a band near the dopant atom can break and form a charged compensation defect center(AX or DX). The AX center forms when two host anion-cation bonds break and an anion-anion bond forms between second neighbor atoms. This rebinding process leads to the conversion of the standard substitution atom into the dopant displaced from its lattice site, resulting in the converted dopant atom.

$$a^- + 2h \rightarrow AX^+ \quad (19)$$

Equation 19 describes the reaction in which an acceptor captures two holes and forms an AX center. The calculated formation energy of AX center for N, P, As and Sb acceptor dopants for CdTe are -0.1, 0.25, 0, and -0.3, respectively. Negative values imply the formation of an AX center is energetically favorable. The AX formation energy for P in CdTe has the highest value, so P could be a better dopant compared with other dopants. Further calculation by S. B. Zhang et al. [46] indicates that the formation of the AX center is not a limiting factor for p-type doping in CdTe. The DX center has been observed for a number of different n type dopants in CdTe.

3.2.2.2 Auto Compensation

Besides intrinsic defect compensation for impurity doping, the doping concentration is also limited by the impurity itself. This is called auto compensation. For example, Cu could be either an acceptor or donor depending on the position it occupies. For Cu_{Cd}, it is a p-type dopant. For Cu_i, it is an n-type dopant. If the formation energy of Cu_{Cd} is lower than that of Cu_i, it acts as a p-type dopant. Vice versa, it acts as an n-type dopant. The formation energy will change with the changing of Fermi energy, which means if the impurity acts as a p-type dopant initially, with the increasing doping

concentration, the donor formation energy will increase or decrease, if it becomes lower than the formation energy of an acceptor, the further increasing of hole doping concentration will be limited. If the donor formation energy is higher than the acceptor formation energy, no limit exists for p-type doping under this condition. Calculation shows the formation energy of Cu_i is always higher than that of Cu_{Cd}. From this point of view, Cu could be a good dopant under the Te rich condition.

3.2.2.3 Solubility Limits of Dopants

The solubility limit is the ultimate doping limit. For the wide band gap materials, the solubility of most dopants is relatively low due to the high incorporation energy. The solubility also depends on Fermi level. The closer the Fermi level to the band, the lower the solubility. Usually, the best conditions for suppressing compensating defects are also the worst conditions for solubility. Solubility calculation of Na, Li and N in ZnSe and ZnTe performed by D.B Laks at al. [47,48] well followed the experimental results.

3.2.2.4 Ionization Energy Level Limit

To achieve a high carrier concentration, the dopant must have low ionization energy so that it can release electrons or holes at a normal operating temperature. Tables 1 and 2 list the ionization energy levels of acceptors and donors in Zn- and Cd-chalcogenides, respectively. Comparing figure 17, tables 1 and 2, they fit each other very well. When the phenomenon logical model predicts that one material is easily dopable, the experimental results show low ionization energy levels.

Table 1 Ionization Energies (in mV) of Various Foreign Donors in Different Zn-and Cd-Chalcodenides [41]

	ZnTe	ZnSe	ZnS	CdTe	CdSe	CdS
B	18.5 18.4 18.3	25.6 26				
Al		25.6 26.3 26	100 74	14.05		
Ga		27.2 27.0 27.9	400	13.88		33.1
In		28.2 28.1 28.9	400-600	14.5 14.15		33.8
F		28.2 28.8 29.3	13.67			35.1
Cl	20.1	26.2 26.1 26.9		14.1 14.48 14		32.7
Br		26.8				32.5
I		23.95 30.4	600			32.1
Li_i		21 17 20±2		13.9		28
Na_i		20				
N_i		29.1±1 26				

Table 2 Ionization Energies (in mV) of Various Foreign Acceptors in Different Zn- and Cd- Chalcodenides [41]

	ZnTe	ZnSe	ZnS	CdTe	CdSe	CdS
Li	60.5 61	114 113 111	150	57.8 58	109±8	165±6
Na	62.8	126 128	190	58.8 28.7		196±6
Cu	148 149 146 140	650	1250	147 146 140		1100 860

Table 2 (Continued)

	ZnTe	ZnSe	ZnS	CdTe	CdSe	CdS
Ag	121 123	430 113	720 113	108 107.5 92 123		260
Au	277	550		263		
N		100±15 110 111		56	21-31	
O		80	110	46		116
P	63.5	85 85.3 550 600-700		60 68.2 50	83±6	120 600
As	79 78.5	110 113		92		750
Sb				57 280		
Bi				300		

Table 3 Calculated Formation Energy [46]

Defect	Formation energy(eV)	Defect	Formation energy(eV)
V_{Cd}	2.67	Cd_{Te}	3.92
V_{Te}	3.24	Te_{Cd}	3.70
Te_i^a	3.52	Cd_i^a	2.26
Te_i^c	3.41	Cd_i^c	2.04
Na_{Cd}	0.45	Al_{Cd}	1.17
Cu_{Cd}	1.31	Ga_{Cd}	1.23
Ag_{Cd}	1.32	In_{Cd}	1.23
Au_{Cd}	1.30	F_{Te}	-0.08
N_{Te}	2.62	Cl_{Te}	0.48
P_{Te}	1.83	Br_{Te}	0.62
As_{Te}	1.68	I_{Te}	0.99
Sb_{Te}	1.72	Cu_i^a	2.14
Bi_{Te}	1.96	Cu_i^c	2.24
Na_i^a	0.60	Na_i^c	0.45

a: sites surrounded by anions c: sites surrounded by cations

3.2.3 Defects in CdTe

The defects in CdTe can exist in the form of point defects or complexes. The possible native point defects include neutral or ionized Cd interstitial Cd_i, Cd vacancy V_{cd}, Te interstitial Te_i, Te vacancy V_{Te}, Te anti-site Te_{Cd}, and Cd anti-site Cd_{Te}. Point defects can also form defect associations, i.e. (Te_{Cd}-V_{Cd}). It can also form complexes with impurities, i.e., $(Cl_{Te}\text{-}V_{Cd})^{-}$. Some defects act like donors, such as Cd_i, V_{Te} and Te_{Cd}. Some act like acceptors, such as Te_i, V_{Cd}. Cd_i is the main donor defect under the Cd rich condition, while V_{Cd} is often thought to be the main acceptor. Table 3 shows the calculated defect formation energy. For polycrystalline CdTe, the grain boundary acts like a donor.

3.2.4 Acceptors in CdTe

Acceptor centers are obtained when group IA and IB elements are substituted for Cd atoms or when group V elements are substituted for Te atoms. They can also be donors when group IA and IB are substituted for Te atoms or being interstitial or when group V elements are substituted for Cd atoms. Which positions they occupy depend on the defect formation energy.

3.2.4.1 Group IA Elements

3.2.4.1.1 Lithium

M. Restle et al. studied the Li atoms position in CdTe using ion implantation [49]. They found Li atoms are immobile and occupy mainly tetrahedral interstitial lattice sites below 130k and about 10% substitution Li above 130 K. They found a strong interaction

of interstitial Li with vacancy defects resulting in a formation of substitution Li until 470K. Above 470K, Li is unstable and diffuses out to the surface.

H. Pauli et al. studied Li doped CdTe by hot-wall-beam epitaxy [50]. Because Li itself is a highly reactive element, they chose lithium nitride(Li_3N) as a dopant source. In this study, they studied the effect of the dopant source temperature, and the effect of the illumination. They found the hole concentration increased from $4x10^{16}$ to $2x10^{18}cm^{-3}$ when the Li_3N temperature increased from 350 to 550˚C, and the mobility decreased from $100cm^2/Vs$ to $30cm^2/Vs$. They also found illumination significantly enhances the doping efficiency below 500˚C.

L. Svob and C. Grattepain [51] studied the diffusion of lithium at 300°C in CdTe. They found there were two diffusion forms, one with high diffusion coefficient depends on the cadmium vacancy concentration, while the other with low diffusion coefficient doesn't. The fast one is interstitial Li_i, and the slow one is substitution lithium, Li_{Cd}. L. Svob and Y. Marfaing [52] proposed a model of diffusion of lithium based on simultaneous diffusion of substitution Li acceptor and interstitial Li donors. This well explained the observation of the aging effect of Li doped CdTe.

3.2.4.1.2 Silver

Silver can be easily introduced in high concentration as a p-type dopant in CdTe. Interstitial Ag is a fast diffusing impurity and leads to a uniform occupation of Cd vacancy even at room temperature. The diffusion of Ag atoms depends on the external

partial pressures of Cd and Te. Under Te pressure, the concentration of V_{Cd} is higher, the Ag atoms occupy the V_{Cd} position and show slow diffusion.

H. Maqsood et al. studied the Ag-doped CdTe fabricated by CSS [53]. Different doping concentrations were achieved by dipping CdTe in $AgNO_3$-H_2O solution for different times as 0, 30s, 5 min, 10min, 20min, and 40minutes. The resulting Ag compositions (at%) were 0, 2.63, 8.23, 9.59, 12.25 and 17.6. The highest hole concentration exceeded 10^{17} cm^{-3} and mobility was 78 cm^2/Vs. The resistivity was 1.69-Ωcm. The systematic decrease in resistivity was observed at room temperature due to Ag doping.

At high Ag concentration, the substitution Ag_{Cd} acceptors and Ag_i donors are formed which passivate each other. H. Wolf proposed self-compensation by lattice relaxation and rebinding, transforming 50% of the acceptor impurities into donor-like defects, which are called AX- or double-broken-bond(DBB) centers [54].

3.2.4.1.3 Gold

Au doped CdTe has been investigated electrically and optically by MR Lorenz and B. Segall [55]. They measured the Au level at 0.34 eV and 0.4 eV above the valence band, respectively. W. Akutagawa et al. studied Au doped CdTe [56]. Au was incorporated by diffusion into CdTe crystals from the surface with an Au thickness of about 10μm by evaporation. They found substitution Au solubility increases with both increasing temperature and decreasing P_{Cd}. The net Au concentration is about 10^{17} cm^{-3}. But the Hall measurement shows the carrier concentration is less than $10^{10}cm^{-3}$, indicating that substantial charge self-compensation occurred through the cadmium

interstitial in the heavily doped CdTe. They found 50~80% of the Au atoms were in substitution. The other fraction may consist either of precipitated or interstitial Au.

3.2.4.1.4 Copper

In single crystal CdTe, Cu is considered to exist as an interstitial Cu_i^+ or substitute Cd atom to form a deep acceptor state (Cu_{Cd}^-) with activation energy of 0.28-0.34eV. The mobility of interstitial Cu is very high. Copper can also be able to form complexes between Cu^+ and V_{Cd}. These complexes are relatively shallow acceptors.

Copper plays two important roles for CdTe/CdS solar cells. As an acceptor dopant, it dopes CdTe surface layer as p^+ layer to assist the formation of an ohmic contact by tunneling contact. But interstitial Cu diffuses fast and accumulates on the interface of CdTe/CdS and is believed to be the main reason of degradation. But the study at USF [57], in which the Cu was introduced directly on CdS surface, showed that a suitable amount of Cu in the interface also improves the device performance.

C. R. Corwine et al. found the most probable Cu-related defect was a deep donor and may be a doubly ionized Cu interstitial ion (Cu^{2+})[58]. The highest concentration was at the CdTe/CdS interface and the substitution Cu impurities (acceptors) were only found in the bulk of the CdTe.

T.D. Dzhafarov et al. studied the thermal and photo stimulated diffusion of Cu in CdTe thin films [59]. They found the diffusion coefficient of photo stimulated diffusion of Cu is larger than that of thermal diffusion by 2-4 times. For thermal diffusion: D_t is $7.3x10^{-7}$exp (-0.33/kT). For photo stimulated diffusion, D_{ph} is $4.7x10^{-8}$exp(-0.20/kT). The activation energy for photo diffusion is smaller (0.2eV) than that of thermal diffusion

(0.33eV). Hall measurements show the hole concentration is $3x10^{10}cm^{-3}$, μ=40cm2/Vs, and ρ=0.5Ωcm.

3.2.4.1.5 Disadvantages of Group I Elements

B. Reinhold [60] and S.B. Zhang [61] found the dominant intrinsic defect that compensates acceptors is Cd_i. In order to avoid the intrinsic compensation, p-type doping should be carried out at the Te-rich condition because of the relatively large formation energy of Cd_i at this condition. IA and IB elements have the lowest formation energy under Te-rich condition, so it is relatively easier to get higher doping concentrations compared with group V elements. On the other hand, the fast diffusion of Ag, Li, Na and Cu at room temperature has been widely reported. N. V. Agrinskaya [62] found that the electrical conductivity and carrier concentration of Li and Na doped crystals decreased significantly after aging at room temperature for several months. For Li, Na, and Ag, this aging effect is attributed to the instability of these elements occupying Cd sites. This instability described by Mcd $\rightarrow M_i+V_{Cd}$. Further study by Y. Ishikawa et al. [63] found that besides the instability of these elements on Cd site, the formation of various complexes among native defects and impurities is also responsible for this aging effect.

The diffusion of Cu in CdTe is believed to be responsible for the instability of CdTe/CdS solar cell's performance. S. E. Asher et al. [64] found a significant amount of copper diffused through the CdTe/CdS layer to compensate the shallow donor levels with deep acceptors in CdS.

3.2.4.2 Group V Dopants (N, P, As, Sb, Bi)

Su-Huai Wei et al. studied the doping limit in CdTe [65]. They found the calculated (o/-) transition energy levels are at 0.01, 0.05, 0.1, 0.23 and 0.3 eV for N, P, As, Sb, and Bi, respectively. The shallow transition energy levels for N_{Te} and P_{Te} indicate that they could be very good dopants for CdTe, but their defect formation energies are large because of the large site mismatch. Their studies showed that the doping limit is due to the very low solubility at the Te rich condition.

3.2.4.2.1 Antimony

Sb is a suitable dopant because of its low ionization energy, low diffusion constant, and can easily incorporated into CdTe. At 400˚C for 30 minutes, the diffusion length is about 1 μm. A. Picos-Vcga et al. studied physical properties of CdTe-Sb thin films by RF sputtering [66]. They found that the increase in Sb content in the film is accompanied by a decrease in the Cd and Te content. Both decreasing at approximately the same rate, this is evidence of the amphoteric character of Sb substituting for Cd and Te in the CdTe lattice with about the same probability. If the concentration of Sb in CdTe is high (around $10^{19}cm^{-3}$), the CdTe is a semi-insulating material. At low concentration, the Sb substitutes Te as an acceptor. By increasing the concentration of Sb, more Sb atoms substitute Cd and compensate the acceptors of Sb_{Te}, $Sb_{Te}Sb_{Cd}$ was formed.

A vapor phase technique has been tried for Sb doped CdTe, but it was unsuccessful. Sb is not incorporated at low vapor pressure, where at high pressure metallic Sb precipitates.

R. N. Bichnell et al. [67] reported the first Sb doped p-type CdTe film by photo assisted MBE process. The film is highly conductive. The hole concentration is $5x10^{16}cm^{-3}$ and mobility is 40~45cm/Vs. The key point in their experiment is that they used an argon laser to assist the chemical reaction. They attributed this to the argon laser providing the energy needed to surmount surface potential energy barriers at the growing film surface, thus increasing the degree of dopant activation. J. D. Benson [68] found laser-illumination enhances Te-desorption and produces more sites for Sb incorporation. Complementary Auger studies indicate a 20% increase in Sb adsorption due to Sb filling both photons desorbed Te-sites and some equilibrium Te-site vacancies.

O.Zelaya-Angel et al. studied the influence of the growth parameters of Sb doped CdTe [69]. In their study, Sb doped CdTe thin films were carried out with targets containing different amounts of antimony (C_T:0, 2.5, 10 and 20 at.%). They found with low C_T values the structure is a mixture of zinc blended ZB and hexagonal wurzite phases. Sb atoms in the CdTe lattice favor the stable ZB Phase of CdTe, and W is considered the metastable crystalline phase. The resistivity is $9x10^5$ Ωcm with 10% of C_T at 100ºC, but a SIMS measurement shows the Sb is less than 1%. The resistivity decreases with the increasing of C_T . FWHM decreases when C_T increases from 0 to 10% indicating the increasing of grain size. It was also found that V_{oc} and J_{sc} increase with the increasing of substrate temperature.

The excimer laser doping technique has been used to obtain a heavy doping in II-VI semiconductors. Using excimer laser, the semiconductor surface first melts and then cools down rapidly. The bulk of the semiconductor is not affected. Y.Hatanaka et al. [70] reported Sb doped CdTe by excimer laser. The best doping characteristics are 0.027 Ωcm

resistivity, $5X10^{18}$ cm^{-3} hole concentration, and 45 cm^2/Vs mobility at 60 mJ/cm^2 irradiation.

P.K. Pandey et al. [71] reported they developed p-type CdTe by a non-aqueous bath in ethylene glyeol. Their study shows Sb can reduce oxygen impurity in CdTe. A thermo-emf study shows the film is p-type, but no hole carrier concentration was reported.

3.2.4.2.2 Phosphorous

Wei and Zhang have calculated p-type dopant energies in CdTe. N and P are the most attractive dopant elements because N and P create very shallow acceptor levels in CdTe. So if one can enhance the incorporation of N and P in CdTe though non-equilibrium processes, the doping concentration could be significantly enhanced. Table 4 summarizes the results of phosphorous doping of CdTe reported by various investigation groups. The highest hole concentration is $5x10^{19}cm^{-3}$, reported by H. L. Hwang and coworkers [72], who used P^+ implantation followed by pulsed electron beam annealing.

Phosphorus atoms are often associated with native defects and form complexes and precipitates, such as Cd_3P_2, P_2Te_3. It might exist as P_i, P_{Te}, and P_{Cd} in CdTe. It is an acceptor when it occupies the interstitial site and surrounded by Cd atoms, or it occupies Te site. When it is surrounded by tellurium atoms, or occupies Cd site it becomes a donor. Based on Kroger's model, the compensation mechanism can be described as : the shallow acceptors P_{Te} are compensated by Cd_i at high cadmium pressure annealing, while at low cadmium pressure annealing, the shallow acceptors V_{Cd} are compensated by P_{Cd}.

At high doping concentration, the neutral or charged complexes become dominant leading to a large degree of self-compensation.

A. D. Compan et al. [73] studied phosphorus doped CdTe films by reactive sputtering from $CdTe/Cd_3P_2$. In their study, they compared three structure solar cells' performance: CdS/CdTe/Au. CdS/CdTe:P/Au, and CdS/CdTe/CdTe:P/Au. They observed the effect of CdTe doping in improving device performance. A stability study shows the uniformly doped CdTe:P device has the poorest stability due to the degradation in both J_{sc} and FF. The other two structure devices show almost same stability but with a different degradation mechanism. For the CdS/CdTe:P/Au structure device, this is due to degradation in both V_{oc} and FF, while for CdS/CdTe/Au structure device, it is only due to the degradation in V_{oc}.

Table 4 Summarizes The Electrical Properties of Phosphorous-Doped CdTe and The Acceptor Energy Level of P Reported by Several Authors

Dopant concentration (cm^{-3})	Annealing condition (atm)	Hole concentration (cm^{-3})	Energy level E_A (eV)
$6.0x10^{16}$	P_{cd}, 0.01	$6.0x10^{16}$	0.034
$5.0x10^{19}$	P_{cd}, 0.01	$1.4x10^{17}$	0.03-0.038
$1.0x10^{19}$	P_{cd}, low	$8.0x10^{16}$	0.05
$1.0x10^{19}$	-	$6.7x10^{16}$	0.11
$1.2x10^{18}$ [a]	-	$1.2x10^{16}$	0.5
$2.5x10^{18}$	P_{cd}, $5x10^{-13}$	$2.2x10^{17}$	0.051
-	P_{cd}, sat	$3.0x10^{17}$	0.052
$6.5x10^{14}$ [b](cm^{-2})	600˚C	$5.2x10^{12}$(cm^{-2})	0.03
0.03 atomic percent	P_{cd}, $2x10^{-13}$	$2.2x10^{17}$	0.066
$5.0x10^{19}$ [a]	P_{cd}, 0.01	$5.0x10^{17}$	0.037
$5.0x10^{15}$ [a](cm^{-2})	Laser	$1.6x10^{17}$	-
$5.0x10^{15}$ [a](cm^{-2})	PEB	$5.0x10^{19}$	-

a) p+ implantation, b) p+ and Cd^+ co-implantation

3.2.4.2.3 Arsenic

A USF group [74] tried to use arsine as a dopant source to dope CdTe by MOCVD. The doping efficiency is very low and most incorporated arsenic atoms were electrically inactive due to compensation and complex formation.

S. K. Ghandhi et al. [75] first reported arsenic doped CdTe films grown by organometallic vapor epitaxy using arsine as the dopant gas. They studied the effect of arsine flow rate over the range from $8x10^{-9}$ to $3.5x10^{-7}$ atm. The doping concentration shows a linear relationship up to $2x10^{17}$ cm^{-3} and saturates as the arsine flow is increased further. The carrier concentration also depends on the partial pressure of DMCd and DETe. The acceptor ionization energy is about 62±4 meV.

J. M. Arias el al [76] also reported arsenic doped CdTe by photoassisted MBE. The dopant source is As_4. Acceptor concentration is in the range of $10^{14} – 10^{16}$ cm^{-3} and mobility is about 65 cm^2/Vs. The acceptor ionization energy is 118±16 meV. The doping efficiency is about 13%.

M. Ekawa et al. found higher doping of As could be achieved by Cd rich [77]. At this condition, the sticking rate of As onto Cd increases, which leads to an effective incorporation of As into Te site. Hole concentration increased linearly from $2x10^{15}$ to $3x10^{16}$ cm^{-3} with the increasing flow rate of triethylarsine.

It was reported that the CdTe doped with arsenic from AsH_3 source contains neutral arsenic-hydrogen pairs. This leads to the low doping efficiency in as-grown films. L.Svob et al. [78] found that short annealing leaded to the increase of hole concentration by dissociation of neutral As-H pairs. Almost full activation of the incorporated arsenic

was achieved at low concentration, and the maximum hole concentration was limited to (1.5-2)x10^{17} cm^{-3}.

3.2.4.2.4 Nitrogen

K.Saminadayar et al. investigated the nitrogen doping efficiency in MBE of Te-Based II-VI compounds [79]. They found the nitrogen doping efficiency is decreased as the decreasing of Zn content and the increasing of Mg content. One of the reasons they proposed is that the length of Zn-Te bonds is smaller than that of Mg-Te and Cd-Te bonds, thus the lattice distortion induced by N_{Te} is smaller and resulting in high doping efficiency. The other explanation they gave is by comparison of the formation enthalpies of the nitride compounds. Zn_3N_2 has lowest formation enthalpy while Mg_3Te_2 has the highest one. So there is less likely to form Zn_3N_2 resulting a higher doping efficiency. The highest doping concentration for CdTe-is 8X10^{16} cm^{-3}.

M. Niraula et al. studied N-doped CdTe using low-pressure plasma-radical-assisted MOCVD[80]. In this study, DMCd and DETe were used as the sources of Cd and Te. By changing the ratio of Cd/Te, the resistivity of CdTe film first decreased with the increasing ratio of Cd/Te, but then increased with further increasing the ratio of Cd/Te beyond 4. With the ratio of Cd/Te between 1 and 2, the Cd rich condition makes more Te vacancies where N-atoms can easily reside. When N_2 gas was used to produce nitrogen plasma source, the achieved CdTe film resistivity was not low enough to perform a Hall measurement. Due to the fact that it is difficult to dissociate nitrogen molecules into atomic nitrogen, by using ammonia, the high conductive p type layer is

successfully achieved. The highest doping concentration is $5x10^{18}$ cm^{-3} with the mobility $8.24cm^2/V.s$.

N. Romeo et al. [81] reported N doped p-type CdTe films with resistivity of about 100Ωcm. CdTe films were deposited by co-evaporating cadmium and tellurium from two separate sources. During deposition, neutral high energy nitrogen atoms were shot to the substrate from an atomic gun. The calculated activation energy is 55 meV.

K. A. Dhese et al. [82] tried to use RF nitrogen plasma to get p-type nitrogen doped CdTe by MBE. Although PL measurements show nitrogen is incorporated in CdTe films and confirmed by SIMS measurements, electrical measurements show CdTe films are n-type with donor concentrations < 10^{15} cm^{-3}.

3.2.4.2.5 Bismuth

Recently O. Vigil-Galan et al. [83] studied the physical properties of Bi doped CdTe. The CdTe films were deposited by CSVT using powdered CdTe:Bi crystals with nominal Bi doping concentration from 10^{17} to $8x10^{18}$ cm^{-3}. They found the resistivities were $1x10^8$, $1x10^{10}$, and $6x10^5$ Ωcm, respectively, and for undoped, $1x10^{17}$, and $8x10^{18}$ cm^{-3}. PL measurements show Bi atoms substitute Cd positions at low doping concentration. The V_{Cd} is compensated by Bi_{Cd}, leading to a semi-insulating film. At high concentrations, Bi atoms occupy Te positions, and the resulting film is p type. The resistivity can be reduced to 10^2-10^3 Ω cm.

3.3 How to Improve the Performance of CdS/CdTe

Table 5 compared the world-record CdTe cell and ideal one. We can see that J_{sc} is already 88% of theoretical value, while V_{oc} is only 79%. It will be very difficult to

increase J_{sc} and the space for V_{oc} is bigger. It is relative easier to increase V_{oc} than to increase J_{sc}.

Table 5 Comparison of World Record and Ideal Solar Cell

	Word record	Ideal	Record/Ideal
V_{oc}(mV)	847	1070	79%
J_{sc}(mA/cm^2)	25.88	29.5	88%
FF(%)	75.5	89	85%
η(%)	16.5	29.2	57%

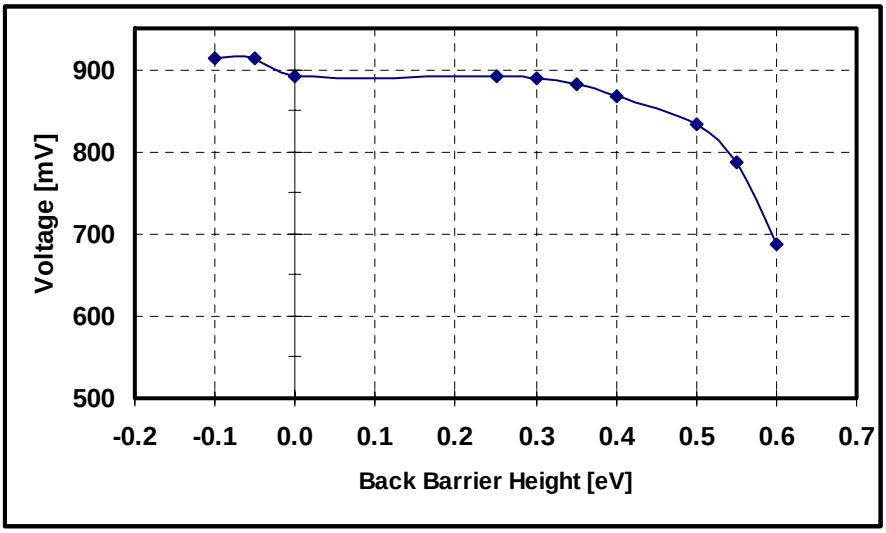


Figure 19 The Effect of Back Barrier on V_{oc}

There are three main factors to limit the V_{oc}. First, the back barrier. Figure 17 shows the V_{oc} as the function of back barrier(Φ_B). At low back barrier(<0.35eV), the V_{oc} is not significantly affected by back barrier height. When the back barrier is more than 0.35 eV, V_{oc} is decreased a lot. When back barrier is less than 0, which means there is no back barrier exists and the band bending is up near the back surface, often referred to as an electron reflector. Even a small electron reflector, the V_{oc} should increase

significantly. There are two way to achieve ohmic or near ohmic contact. One way is by heavily doped near back surface to get tunneling contact. The other way is by using high work function materials. The possible high work function materials are TiSe2 and Vse2 . ZnTe should work as an electron reflector material based on theoretical calculation.

The second factor is the low hole concentration. Figure 18 shows the simulated V_{oc} results with increased hole concentration. We can see the V_{oc} increases with the increasing of doping concentration. Typical hole concentration is about $1x10^{14}$ cm^{-3} for the present CdTe solar cells. In this dissertation, Sb is used as a dopant to increase the doping concentration for CdTe film.

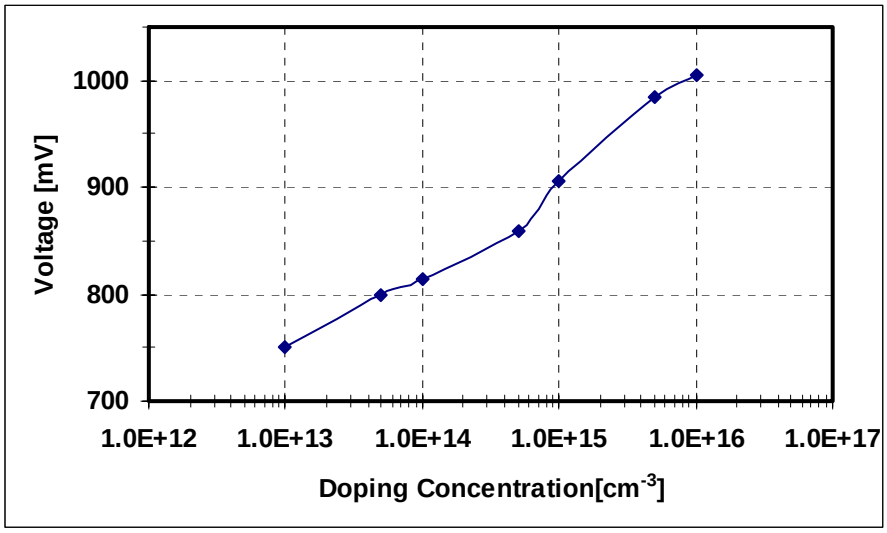


Figure 20 Effect of Doping Concentration on V_{oc}

The third factor is the uniformity of CdS, CdTe, and back contact. If the CdS film is not uniform, for an example, there exits pinholes, a weak diode between CdTe and TCO will form and reduce the V_{oc}. To eliminate pinholes on CdS film, the thickness of CdS film has to be thicker, and thicker CdS will reduce J_{sc}. There is a trade-off for high V_{oc} and J_{sc} for CdS. High resistive buffer layer between TCO and CdS can reduce the

required thickness of CdS and maintain high V_{oc}. Undoped SnO_2, In_2O_3 and Zn-Sn-O have been used as buffer layers. Further study on new buffer layer material has to be done to improve the cells' performance.

The nonuniform back contact will result in reach-through diode effect. This nonuniformity could be due to localized surface state, the diffusion of impurities, or the contamination from the process. Great care has to be taken prior to each deposition step to avoid contamination.

CHAPTER 4

EXPERIMENTAL METHODS

The basic structure of the CdS/CdTe solar cells used in this thesis is glass (7059) TCO/CdS/CdTe/back contact as shown in figure 19. The front contact TCO is ITO/SnO_2 or bilayer SnO_2. CdS is kept constant in all devices. All the other layers were changed as the experiment needed.

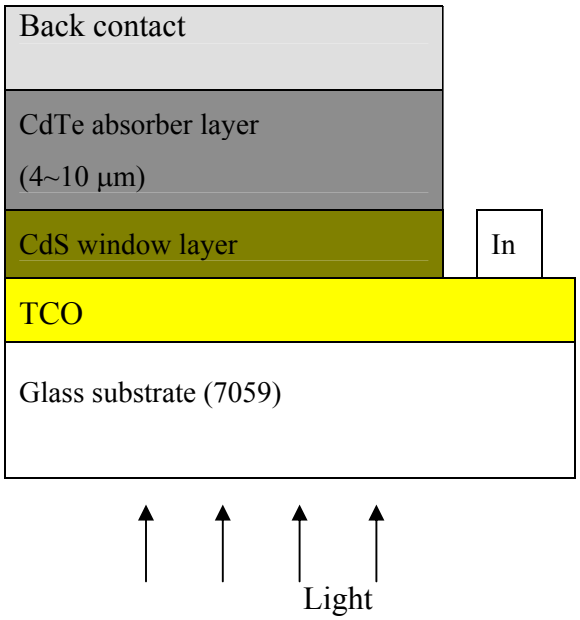


Figure 21 Configuration of CdTe Solar Cells as Used in This Dissertation

4.1 Chemical Bath Deposition

CdS forms the n-type junction partner of CdTe solar cells. Its bandgap is 2.4 eV, this allows the low energy light (above 510nm) can pass through it to reach CdTe absorber layer to generate photocurrent. The light absorbed by CdS can not contribute

photocurrent, so the thickness of CdS should be as low as possible. On the other hand, thin CdS leads to low V_{oc} due to the pinholes of CdS. CdS can be deposited by chemical bath deposition (CBD), closed-spaced sublimation (CSS) and RF sputtering. CBD gives

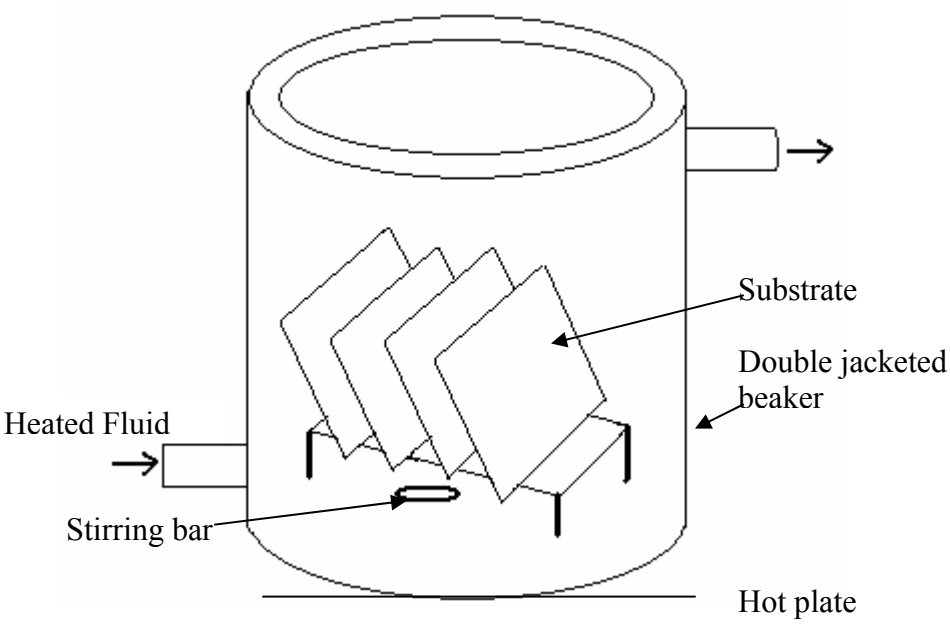


Figure 22 Diagram of CBD Set Up

the best result of CdTe solar cell. In this study, the CdS is deposited by CBD. Cadmium acetate is used as cadmium source. Thiourea is used as sulfur source, ammonium acetate (NH_4AC) and ammonium hydroxide (NH_4OH) are used as buffers to control the PH value. The SnO_2: F or ITO coated glass substrates are immersed in DI water. The SnO_2: F or ITO should face up to eliminate bubbles on the surface. The temperature is maintained at 80-90˚C during the deposition. Figure 22 shows the diagram of the set up. Solution A is prepared by mixing specific amount of CdAc, NH_4AC and NH_4OH solution. For every several minutes, 0.00003M CdAc and 0.00012M thiourea are added into reaction

container. The thickness of CdS can be changed by varying the deposition time. J. Herrero et al. [84] proposed the possible reactions as follows:

$$Cd(CH_3COO)_2 \leftrightarrow Cd^{2+} + 2CH_3COO^- \quad (20)$$

$$NH_3 + HOH \leftrightarrow NH_4^+ + OH^- \quad (21)$$

$$Cd(NH_3)_4^{2+} + 2OH^- \leftrightarrow [Cd(OH)_2(NH_3)_2] + 2NH_3 \quad (22)$$

$$[Cd(OH)_2(NH_3)_2] + SC(NH_2)_2 \rightarrow [Cd(OH)_2(NH_3)_2SC(NH_2)_2 \quad (23)$$

$$[Cd(OH)_2(NH_3)_2SC(NH_2)_2] \rightarrow CdS_{(S)} + CN_3H_5 + NH_3 + 2HOH \quad (24)$$

4.2 Close Space Sublimation

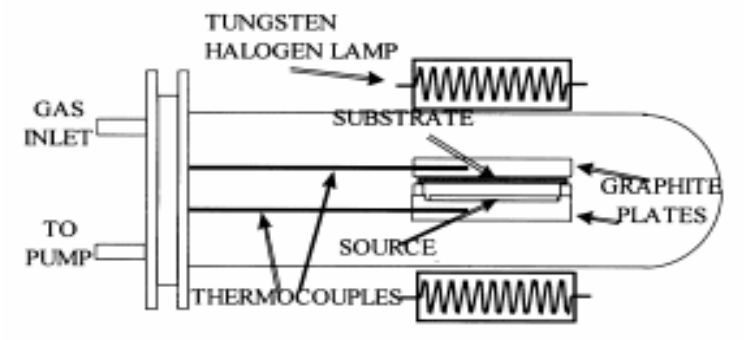


Figure 23 Schematic Diagram of CSS Deposition Chamber

The CdTe absorber film was deposited by close space sublimation (CSS). The deposition is based on the following reversible dissociation of CdTe at high temperature:

$$2CdTe(s) \leftrightarrow 2Cd(g) + Te_2(g) \quad (25)$$

The CdTe source and substrate are typically separated by a small space of several millimeters. The source temperature is maintained at around 100˚C higher than substrate temperature. At high temperature, the CdTe solid will dissociate into its elements gas (Cd

and Te), then they recombine on the substrate surface because of its lower temperature. In this research, the CdTe chunks were first sublimated onto a 7059 glass substrate to get a very thick CdTe layer. This is so called source substrate in this research. Before CdTe deposition, the CdS film was annealed at 390˚C for 10 minutes in H_2 ambient to remove unpreferred oxide compound like CdO. Halogen lamps are used to heat up the source and substrate. The temperature was controlled by OMEGA temperature controller. Figure 23 shows the diagram of CSS set up.

4.3 Sputtering Deposition

The moly back contact and antimony were deposited by sputtering deposition. Sputtering deposition is widely used in semiconductor industry. The advantages of sputtering deposition include: low temperature, good adhesion and can be used for any material, good stoichiometric. Disadvantage includes: surface damage and stress. It can be classified as reactive sputtering, which is by adding a gas which reacts with a sputter material in the presence of the plasma, and non-reactive sputtering, which is the gas doesn't react with the sputtered material. It can also classify as RF and DC sputtering. RF sputtering is suitable for both insulate and conductive materials and DC sputtering is only suitable for conductive materials.

The basic theory is at high enough electric filed, part of gas molecules are ionized, and the ionized particles are accelerated by the electric filed, these high speed particles bombard the target, knock loose the target surface material, transfer its energy to target molecules. When the target molecules impinge the substrate, they diffuse along the substrate surface and settle down to form thin film.

4.4 Device Characterization

The fabricated solar cells were characterized by light and dark current-voltage (I-V) measurements and spectral response measurements.

4.4.1 I-V Measurement

All I-V measurements are done by using four-terminal Kelvin connections. This minimizes measurement errors by eliminating voltage-drop losses that result from resistances due to cables, connections, series resistance. The data was collected by a lab view program, which can calculate V_{oc}, FF, and efficiency η automatically. The power supply is a Keithely 2410 source meter. The sun light simulator is calibrated using standard silicon solar cell. From light and dark I-V plots, all cells parameters can be determined, such as V_{oc}, J_{sc}, FF, R_s, R_{sh}, J_0 and A. Color I-V measurement was also performed for selected devices. In this measurement, Oriel color filters with 20nm bandwidth were used. The light intensity was adjusted to one sun intensity based on the current density calculated from SR for each wave length.

4.4.2 Spectral Response

Oriel monochromater (model 74100) is used for spectral response measurement. The light source is GE400w/120v Quartz Line lamp (model 43707). The light intensity is calibrated using a standard silicon solar cell calibrated by the National Renewable Energy Laboratory (NREL). The quantum efficiency is calculated by the following equation:

$$QE_{Sample} = \frac{I_{Device}}{I_{\mathrm{Re}\,ference}} QE_{\mathrm{Re}\,ference} \tag{26}$$

The device current density is calculated by integrating the product of QE and the standard cell current density.

4.4.3 Capacitance-Voltage Measurement

The C-V measurement was performed on selected devices. From C-V measurement, the doping concentration, doping profile and depletion width can be calculated. It relies on the fact that the depletion width of a reverse-biased P-N junction device depends on the applied voltage. From the definition of capacitance:

$$C = -\frac{dQ_s}{dV} \tag{27}$$

where $dQ_S = -qN_A(w)dw$, we get:

$$C = -qN_A(w)dw/dV \tag{28}$$

The depletion width can be given:

$$w = \left[\frac{2\varepsilon s(V_{bi}-V)}{qN_A}\right]^{\frac{1}{2}} \tag{29}$$

Differentiating equation 28 with respect to voltage and substituting dw/dV into equation 27 gives:

$$N_A(w) = \frac{2}{qK_s\varepsilon_0 A^2 d(1/c^2)/dV} \tag{30}$$

Ideally, for a one-sided abrupt junction, a plot of $1/C^2$ versus V should be a straight line. In this measurement, a HP4194 Gain Phase Analyzer is used.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Optimize the HgTe: Cu Doped Graphite Back Contact

The HgTe: Cu doped graphite paste is the standard back contact in our lab. It gives a good back contact resulting in good performance of CdTe/CdS solar cells. The previous used graphite paste was Acheson Electrodag 003, but the company stopped producing this product. The new one is Electrodag 502, which has the same nominal properties. But actually it has different properties. We cannot get good contact using same conditions as Electrodag 003.New conditions have to be developed. The annealing temperature effect, the annealing time effect, and the HgTe: Cu concentration effect were studied and optimized.

5.1.1 Annealing Temperature Effect

The previous recipe was 37.5% wt. HgTe:Cu doped graphite paste, and the annealing conditions were 270°C and 25 minutes. The same recipe was used first and then different annealing temperatures were used. Figure 24 shows the summary of the effect of the annealing temperature. From the figure we can see the annealing temperature plays an important role. It affects the amount of copper in CdTe, leading to different doping concentrations. The J-V characteristics for different annealing temperatures are shown in Figure 26. With the increasing annealing temperature, the turn-on voltage shifts

towards right which means the barrier across the main junction is increasing. This barrier is an indicator of doping concentration. This indicates the doping concentration is increased with increasing temperature. The cells annealed below 270˚C show similar series resistance, but the cell annealed at 270˚C shows higher series resistance although the dark J-V shows it has higher doping concentration. There are two possible reasons for this behavior. One reason is the high annealing temperature introduces excess Cu to the extend that it compensates the p-type dopant. The other is the high temperature annealing leads to the detriment of the interface between CdTe and back contact.Compared with the

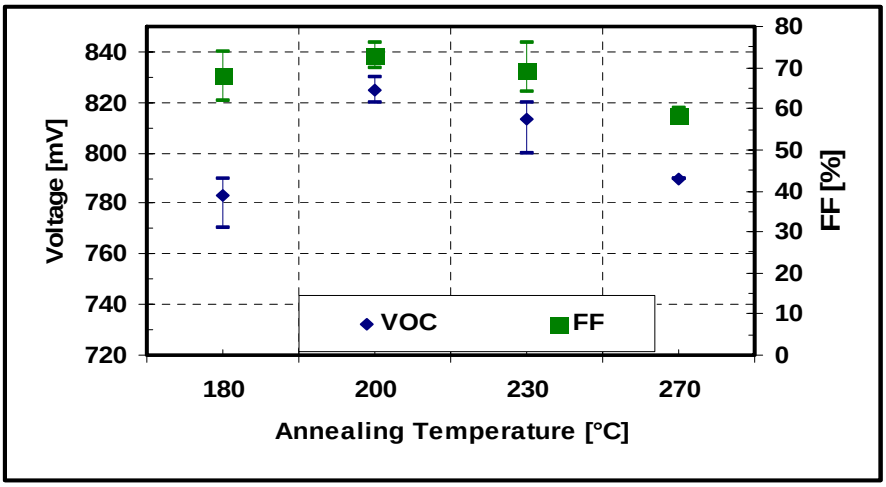


Figure 24 The Summary of the Effect of Temperature

previous graphite paste, the later reason is most probably responsible for the higher series resistance. We also tried the annealing conditions at 270°C for 5 minutes. The resulting devices are not good as those annealed at lower temperatures. This also verified the poor interface is the reason for higher series resistance. Figure25 shows the SR of the devices annealed at different temperatures. The device annealed at 270°C shows significant collection losses resulting in low J_{sc} and V_{oc}. Based on these results it was concluded that

high temperature has detrimental effect on the interface of the back contact and affect the doping in CdTe by changing the amount of Cu.

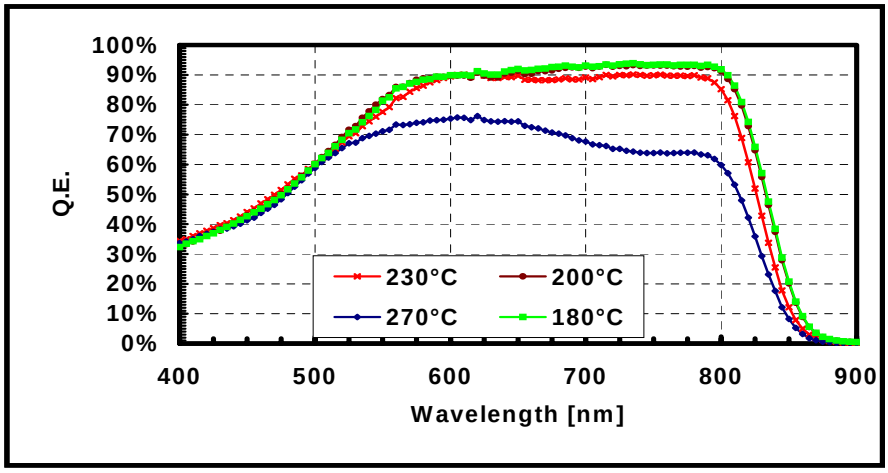


Figure 25 Spectral Response of the Effect of Temperature

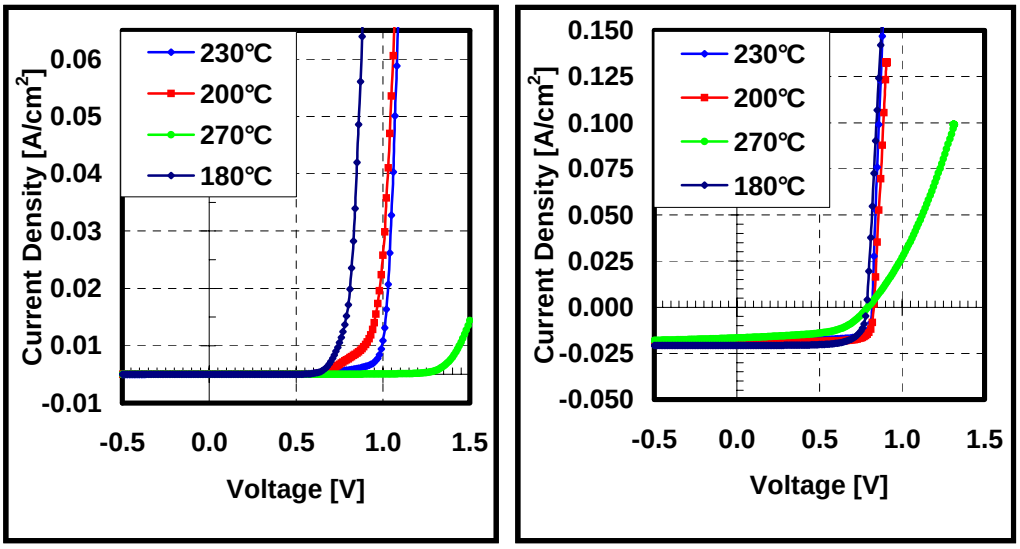


Figure 26 Light and Dark J-Vs for the Devices Treated at Different Temperatures

5.1.2 Annealing Time Effect

From the studies of the effect of the annealing temperature, we found the best annealing temperature was 200˚C, so the temperature was fixed at 200˚C and the

composition was kept as the same as before. Different annealing times (10, 20, 35, 45 and 60 minutes) were performed.

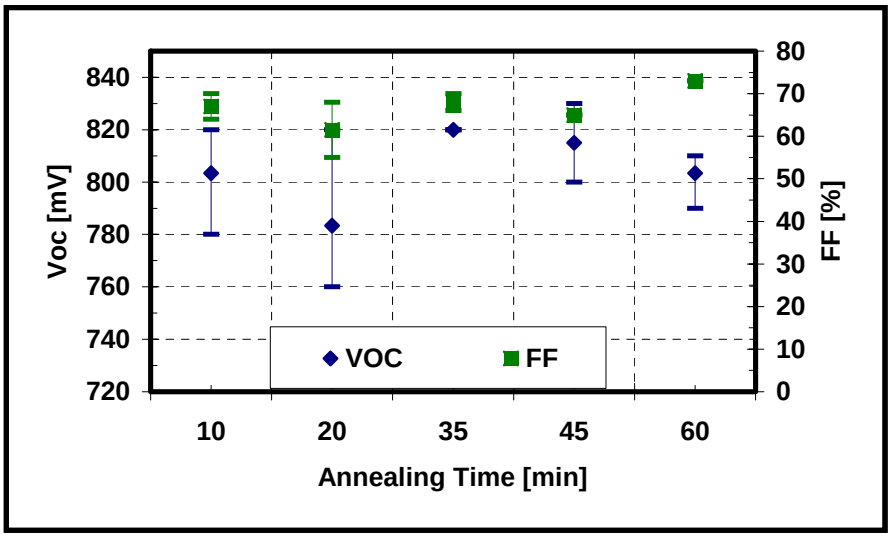


Figure 27 The Summary of the Effect of Annealing Time

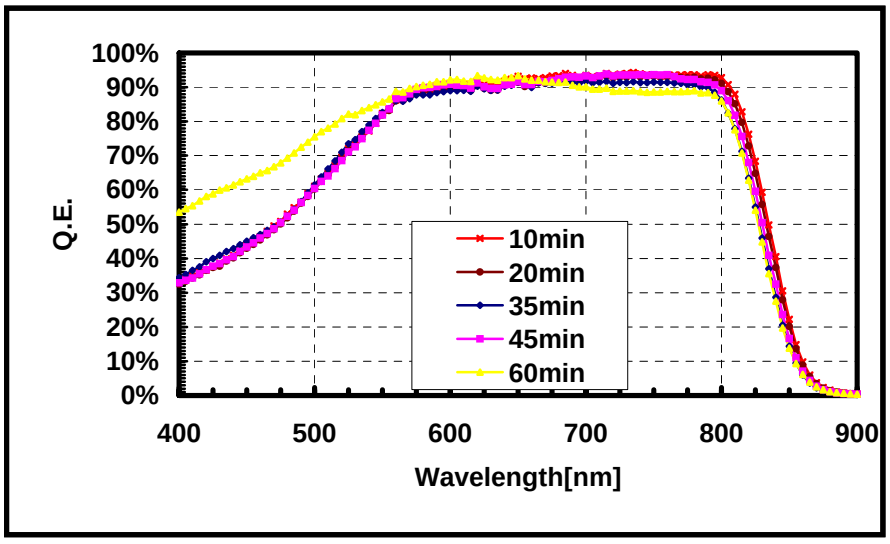


Figure 28 Spectral Response for Devices with Different Annealing Time

Figure 27 shows the summary of the devices' performance for different annealing times. The cell annealed for 60 minutes showed highest FF with fairly high V_{oc}. From the spectral response shown in Figure28, the cell annealed for 60 minutes has thin CdS, so

the relatively lower V_{oc} is mainly due to the thin CdS. The band gap was slightly increased with increasing the annealing time. The possible reason could be the formation of $CdTe_{1-x}S_x$. Figure 29 shows the J-V characteristics of the devices annealed for different times. No shunting was observed, which indicated that even for 60minues annealing the amount of Cu is not excess.

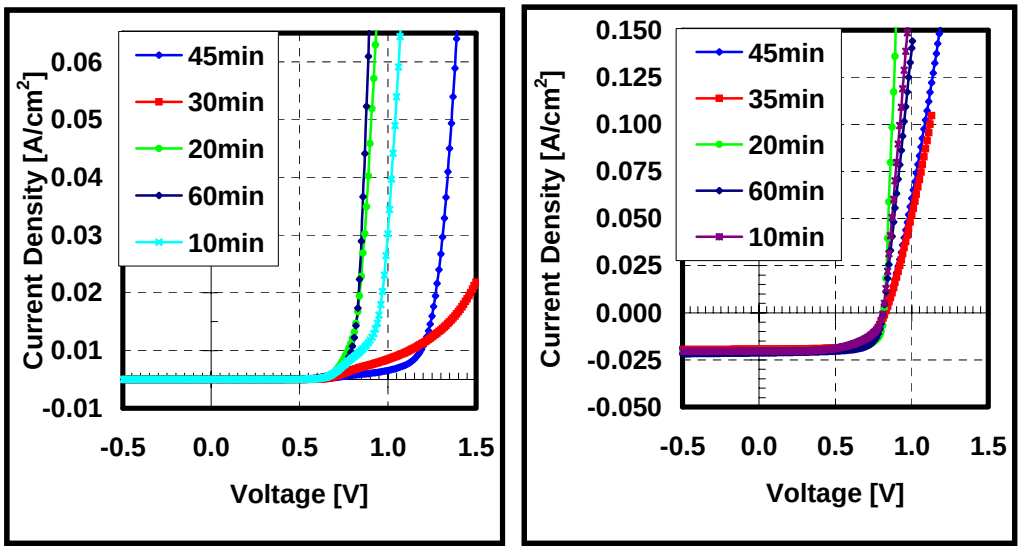


Figure 29 Light and Dark J-Vs for the Devices with Different Annealing Time

5.1.3 The Effect of the Concentration of HgTe: Cu

The concentration of HgTe: Cu affects the final amount of Cu in CdTe. Four concentrations were used (Table 6) to test the concentration effect. The devices were annealed at 200˚C for 60 minutes. The summary of the performance was shown in figure30. The performance is not very sensitive to the concentration of HgTe: Cu. The A gave the best overall performance. Figure 31 and figure 32 showed the SR and J-V characteristics for the devices with different contacts. They all have similar J_{sc} and V_{oc}.

from the dark J-V characteristics, A resulted best doping of CdTe. Based on all the results, the optimized back contact recipe is using A and anneal at 200˚C for 60 minutes.

Table 6 Different Concentrations Used in This Study

	A	B	C	D
Concentration (% wt.)	16.7	28.6	37.5	44.4

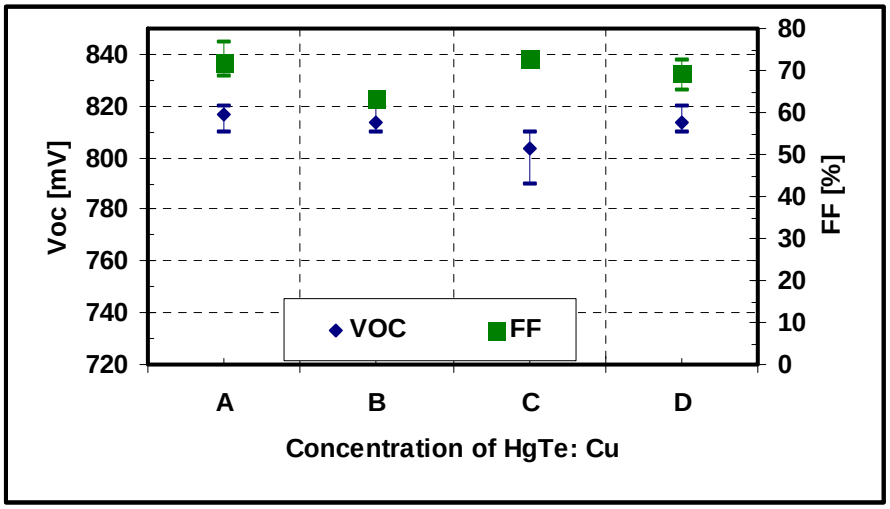


Figure 30 The Summary of the Effect of HgTe:Cu Concentration

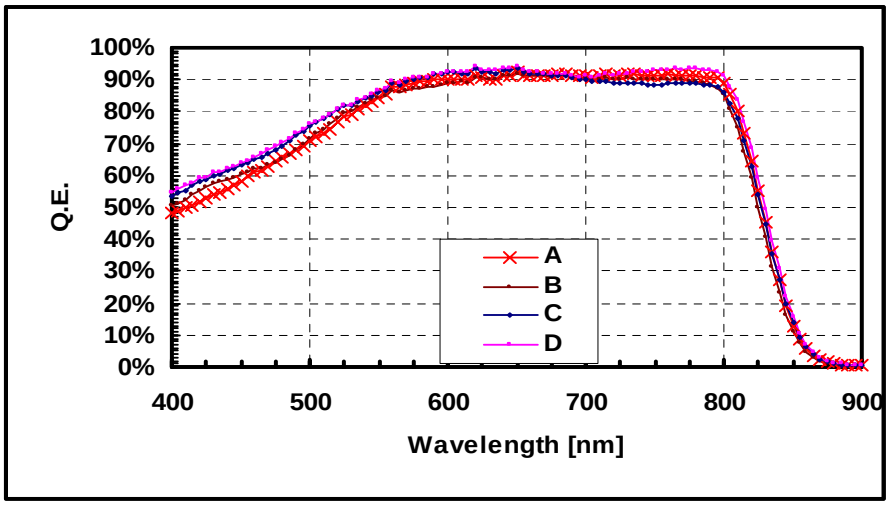


Figure 31 Spectral Response for Devices with Different Concentration of HgTe: Cu

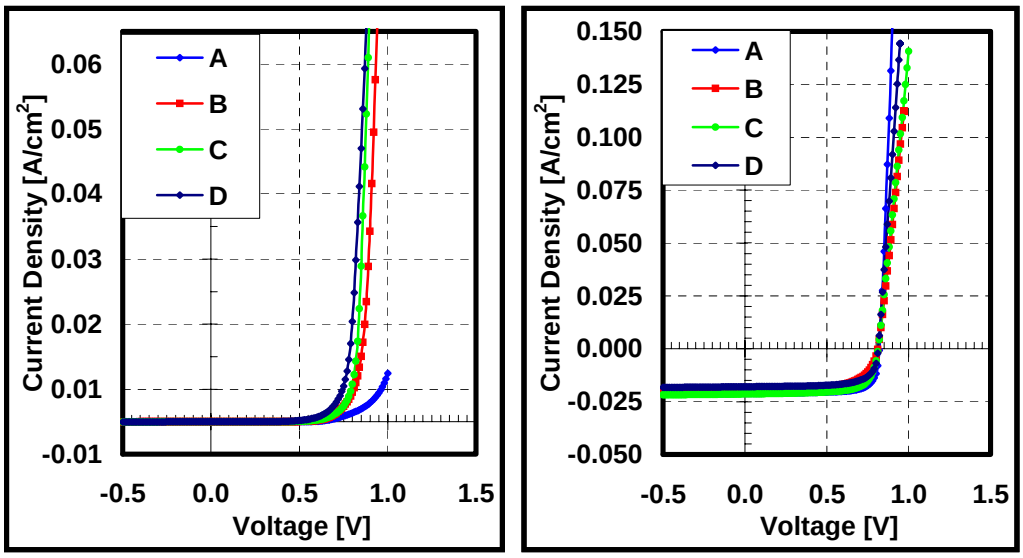


Figure 32 Light and Dark J-Vs for the Devices with Different Concentration of HgTe: Cu

5.2 High Work Function Materials

One of the main issues for CdTe solar cells is the back contact. Developing a new back contact material with high work function, high conductivity and chemical inertness is one of the key point to further improve cell performance. Chemical inertness is desired to limit chemical reactions at the interface with CdTe and improve the long term stability, and high work function is required to enable the formation of ohmic contacts. Potential compound candidates are the selenides $TiSe_2$, VSe_2, $NbSe_2$ and TaSe, as well as their corresponding sulfides.

Based on the existing deposition facilities the decision was made to first investigate $TiSe_2$ films. There are several methods can be used to deposit $TiSe_2$ films, however, the temperature has to be limited below 450°C due to the requirement for good performance of solar cells. Early efforts focused on preparing this compound by selenizing Ti. Metallic Ti films were sputtered on glass slides to a thickness of 200-400

Å, and subsequently exposed to a Se flux under high vacuum conditions; the selenization process is carried out in a CIGS chamber which contains excess Se. It was observed that the formation of $TiSe_2$ by this method depends on the substrate temperature. For temperatures below 400°C no $TiSe_2$ was detected. The Ti films appeared (to the naked eye) to change color at temperatures around 400°C. At selenization temperatures of 425°C the $TiSe_2$ phase was detected; this can be seen in Figure 33. The XRD spectrum of a Ti selenized film clearly shows diffraction peaks that have been found to correspond to $TiSe_2$.

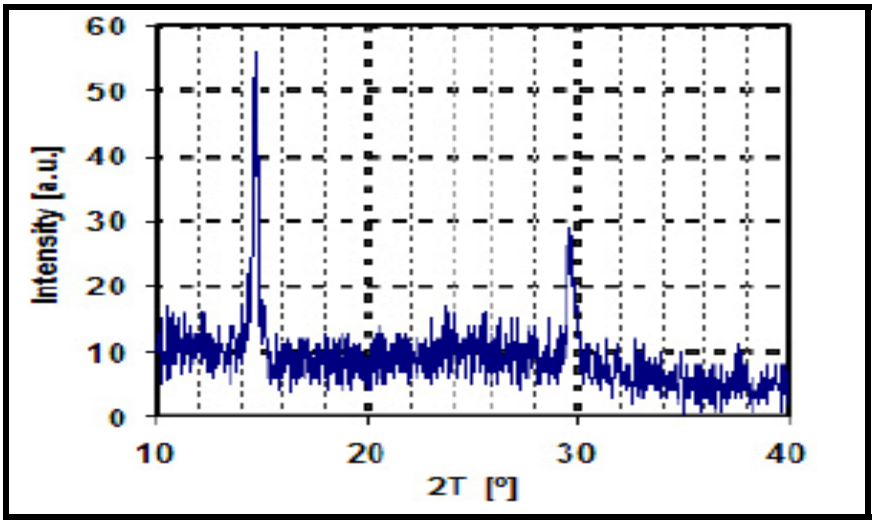


Figure 33 XRD Spectrum of a Selenized Ti Film

However, this is the case on glass substrates. Efforts to selenize Ti films deposited directly on CdTe have been made but failed. This is due to the fact that the selenization conditions (elevated substrate temperature/high vacuum) cause the evaporation of Ti film. The possibility of depositing $TiSe_2$ by co-evaporation at lower temperatures is being considered.

5.3 High Resistive Buffer Layers

Typical CdTe thin film solar cells have short circuit current density of 22-26 mA/cm^2, while the maximum theoretical J_{sc} is 30.5 mA/cm^2. The most part of current losses is due to the absorption of CdS at short wavelength (<510 nm). The electron-hole pairs in CdS produced by photons do not make any contribution to photocurrent due to essentially zero collection. In order to minimize this current loss, the thickness of CdS has to be as thin as possible. However, V_{oc} suffered from the thinning thickness of CdS. This is because a very thin and pinhole free film is difficult to deposit for polycrystalline films. If there is a pinhole, a weak diode will form between CdTe and TCO layer, and seriously harm the cells' performance. The adoption of a high resistive buffer layer between the high conductive TCO and CdS window layer successfully solved or at least mitigate this dilemma stated above. With the high resistive buffer layer, CdTe will not directly contact with the high conductive oxide and the chance for the weak diode formation is greatly suppressed.

The commonly used high resistive buffer layer materials for CdTe/CdS solar cells are intrinsic SnO_2, In_2O_3, and Zn_2SnO_4. They have excellent thermal and chemical stability and superior electro-optical properties. The buffer layer used in the world record efficiency devices is Zn_2SnO_4. We studied the effects of deposition parameters (substrate temperature, Zn-Sn ratio, and post annealing after the Zn_2SnO_4 deposition) in its electro-optical properties. The ZTO films were co-sputtered from SnO_2 and ZnO targets. It was found that the resistivity of films deposited at room temperature increases with the Zn/Sn ratio, and it decreases with increasing annealing temperature. The higher resistivity at low annealing temperatures can be attributed to the fact that the as-deposited films are

amorphous and remain as such for annealing temperatures up to 550 °C; they begin to crystallize at approximately 575 °C [95]. All ZTO films with different Zn/Sn ratios contain both zinc stannate phases: Zn_2SnO_4 and $ZnSnO_3$ [85]. Films deposited at 400°C are polycrystalline films and post annealing up to 600°C didn't affect the crystal structure. Besides Zn_2SnO_4 and $ZnSnO_3$, the films deposited at 400 °C also contain also contain the binary ZnO_2 phase.

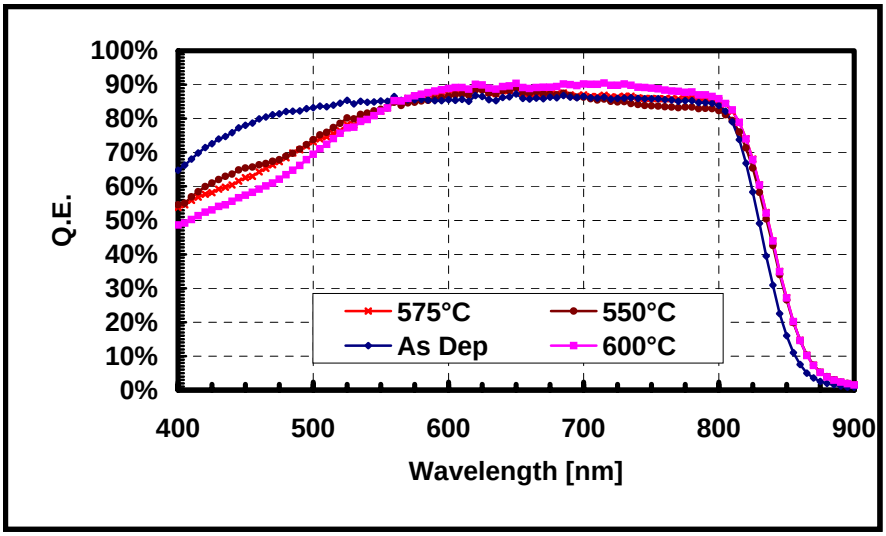


Figure 34 Spectral Response for Devices with ZTO Buffer Layer Annealed at Different Temperatures

Zn_2SnO_4 has a unique property that other buffer layers don't have, which is that Zn_2SnO_4 can consume CdS due to interdiffusion during the fabrication process. The extent of the consumption of CdS depends on the film structure which determined by the post annealing temperature as shown in figure 34. As can be seen, based on the blue spectral response, the final thickness of the CdS window layer is smaller for the devices with amorphous ZTO (as-deposited and annealed at 550 °C). Since the starting CdS

thickness for all these devices was identical, it is suggested that the consumption of CdS depends on the structure which is determined by the post annealing temperature. Nevertheless, the overall cell performance decreases due to losses in V_{oc} and FF. In this case, ZTO films didn't serve as effective buffer layers.

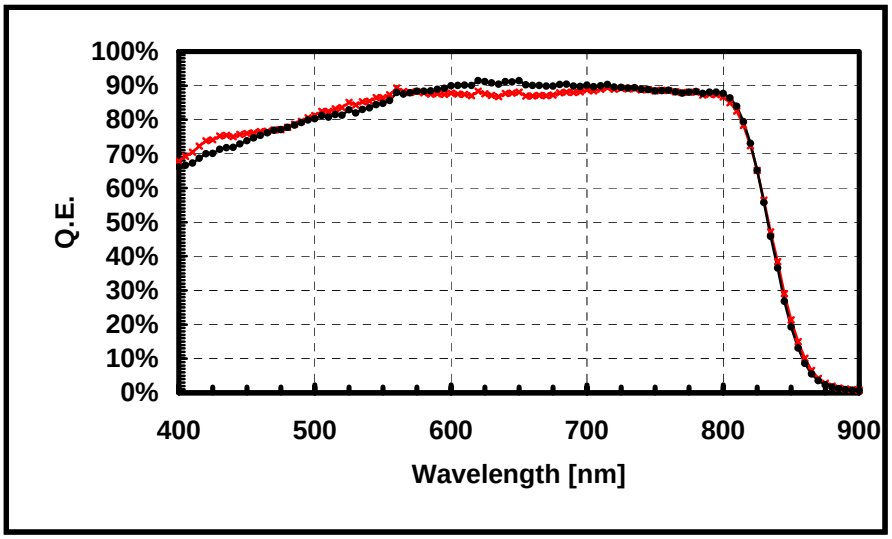


Figure 35 Spectral Response for Devices with ZTO (Zn/Sn=2) Buffer Layer Deposited at 400°C

For the cells with ZTO films deposited at 400°C, the blue spectral response at 450 nm is more than 70% as shown in figure 35. Since the starting thickness of CdS is the same as our baseline cells (QE≈50%@450nm), the high blue spectral response clearly reflected the significant consumption of CdS. Moreover, not like the case aforementioned, the V_{oc} and FF are maintained at high values.

All these results show that ZTO film only acts as an effective buffer layer at a specific composition and deposition conditions. It provides another way to reduce the current loss: Since it is difficult to deposit a very thin and pinhole free film, we can start from a thick film and then consume it through fabrication process.

5.4 Studies of the Effect of O_2 ambient for CSS CdTe

5.4.1 Device Fabrication

The substrate is 7059 boro-silicate glass. The front contact consisted of sputtered ITO and MOCVD-deposited undoped SnO_2 layer. Cadmium sulfide was deposited using chemical-bath deposition (CBD), followed by the deposition of CdTe by close-spaced sublimation (CSS) in different O_2 partial pressure. Before the contact application, the cells were heated treated in the presence of $CdCl_2$. Subsequently the CdTe surface was etched using a Br_2/Methanol solution. Two kinds of contacts were used: HgTe:Cu carbon paste and moly. The moly back contact is sputtered at room temperature. Then the cells were subjected to a post deposition annealing in an inert ambient. Solar cells were characterized using dark and light J-V and C-V measurements.

5.4.2 Structure Properties

The deposition ambient has a profound effect on film continuity and microstructure. It affects the growth rate, the grain size and some electronic properties. For thin film solar cell devices, both pinholes and grain size/grain boundary are known to have a direct effect on the conversion efficiency. For the case of CdTe growth by CSS, previous studies showed that the presence of O_2 in the processing ambient leads to more uniform coverage, smaller grain size and condensed film [86]. Figure 36 shows representative SEM images for films deposited under the four main process variations. As can be seen, film deposited at the lowest O_2 concentration (N_2/O_2=9/1) has the largest grain size. At higher O_2 content, and the grain size is reduced though the decrease is small. Although all films are observed as condensed films, there are more possibilities for

films with larger grains to have more voids that can degrade the quality of the main junction and the cell performance.

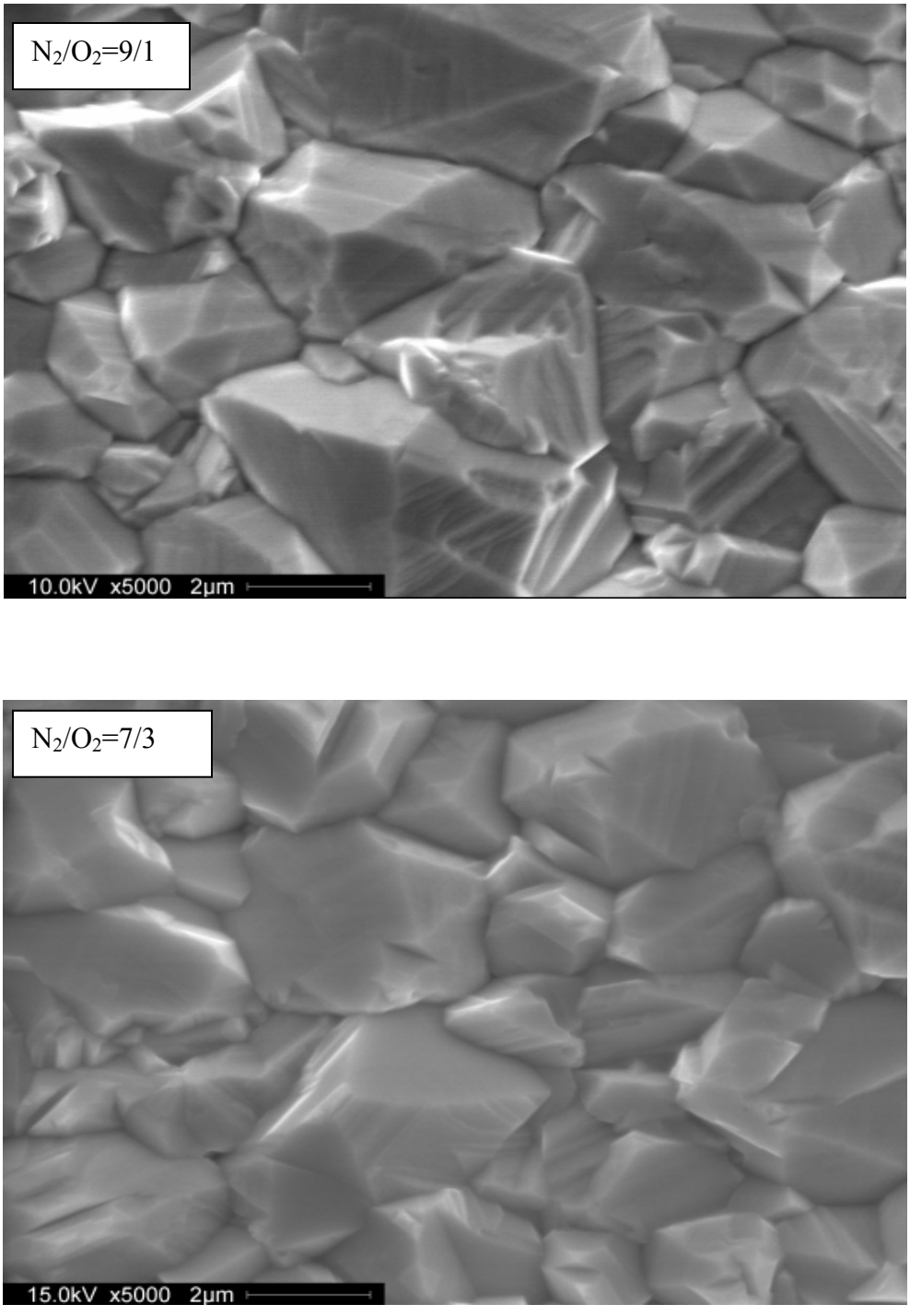
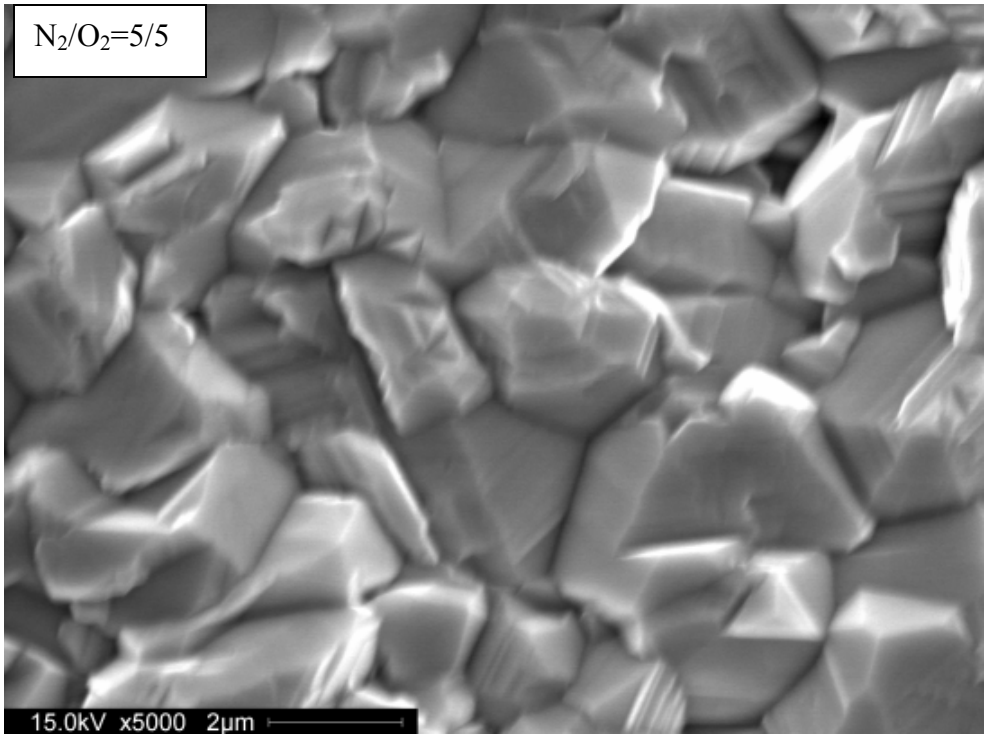


Figure 36 SEM Images of CdTe Films Deposited Under Different Conditions



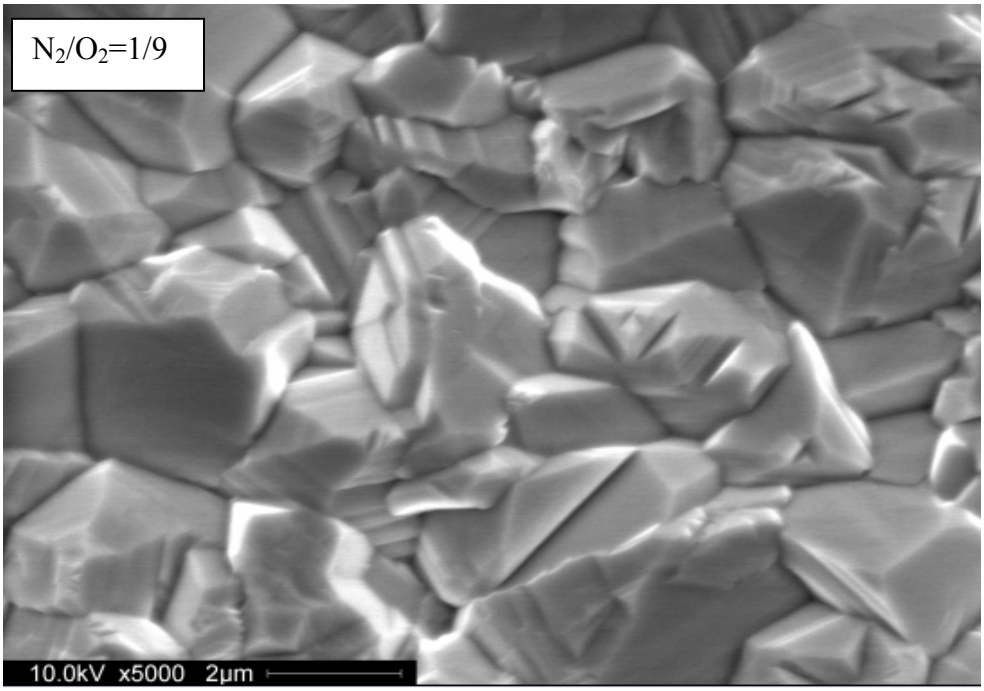


Figure 36 SEM Images of CdTe Films Deposited under Different Conditions (Continued)

5.4.3 O_2 Partial Pressure Effects

5.4.3.1 Thicker CdS

Figure 37 and figure 38 show the dark J-V and SR characteristics for devices with the CdTe deposited in different O_2 partial pressure. Except the O_2 partial pressure, all other processing parameters are all same. From the dark J-V curve, we can see that at

low O_2 (9/1/)partial pressure, the device shows high J_0, and it decreases with increasing O_2 partial pressure indicating that the junction quality is improved. This high J_0 is the main reason of the low V_{oc} for the device fabricated at the lowest O_2 partial pressure. The SR data shows a small higher QE in blue region for high O_2 partial pressure device, suggesting that more CdS was consumed at higher O_2 partial pressure since the starting thickness is same. There is more collection loss in the range of 600-700nm for the device produced at ratio 9/1, while the one fabricated at ratio 7/3 has a collection loss at longer wavelengths. Both of losses can attribute to the poor quality of CdTe layer. The

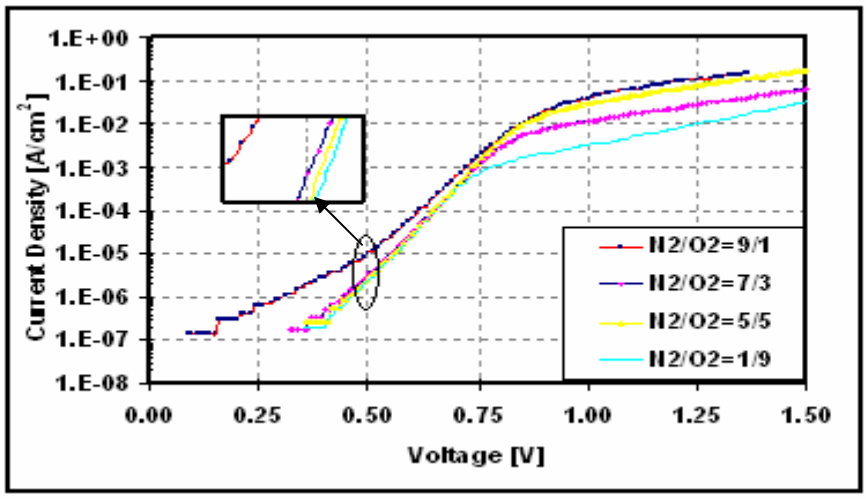


Figure 37: Dark I-V Characteristics for Devices Fabricated at Various O_2 Concentrations

overall current for highest O_2 partial pressure is 0.7mA/cm^2 higher than the one with lowest O_2 content. The higher current is attributed to better collection, which resulted from the higher quality junctions.

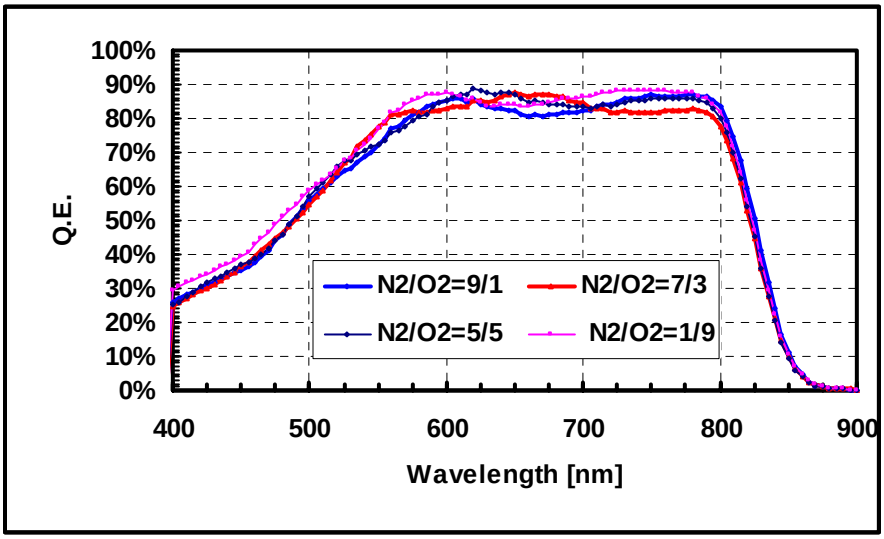


Figure 38 Spectral Response for Devices Fabricated at Various O_2 Concentrations

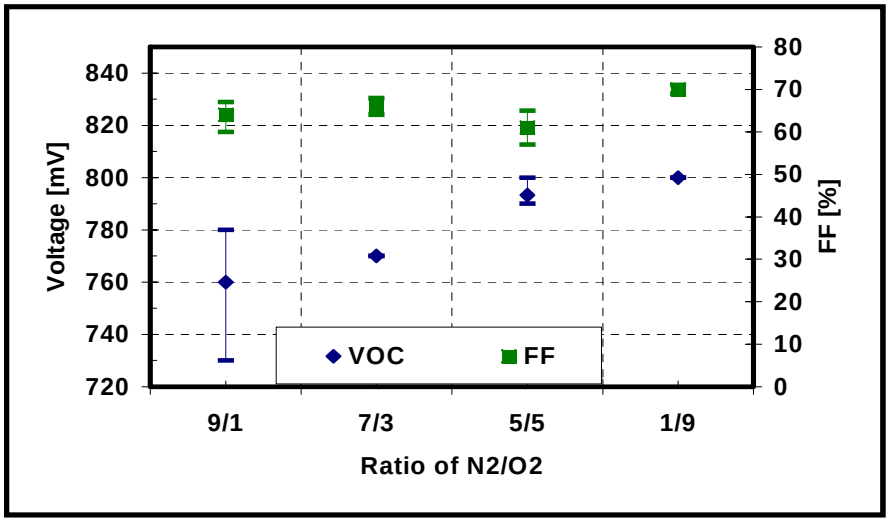


Figure 39 Summary Results for Devices Fabricated at Various O_2 Concentrations

Figure 39 shows the V_{oc} and FF for the devices. It shows that performance increases and more uniform with increasing O_2 partial pressure. The improvement of V_{oc}

is mainly due to the decrease of the saturation current with increasing O_2 partial pressure. It can also be observed the saturation effect of O_2. From 5/5 to 1/9, the performance difference is very small. The small difference can be attributed to the nature of the experiment variation.

5.4.3.2 Thinner CdS

Figure 40 and figure 41 show the dark J-V and SR characteristics for the devices with thinner CdS. All other processing parameters are all same as the devices discussed above. The dark J-V curve shows the same trend as the device with thicker CdS: the reverse saturation current current decrease with increasing O_2 partial pressure indicating better junction quality. For spectral response, it clearly shows that the QE increases with decreasing O_2 partial pressure in the range of 500-600nm, this indicates that the extend of interdiffusion increases with increasing O_2 partial pressure. Out of this range, their QEs

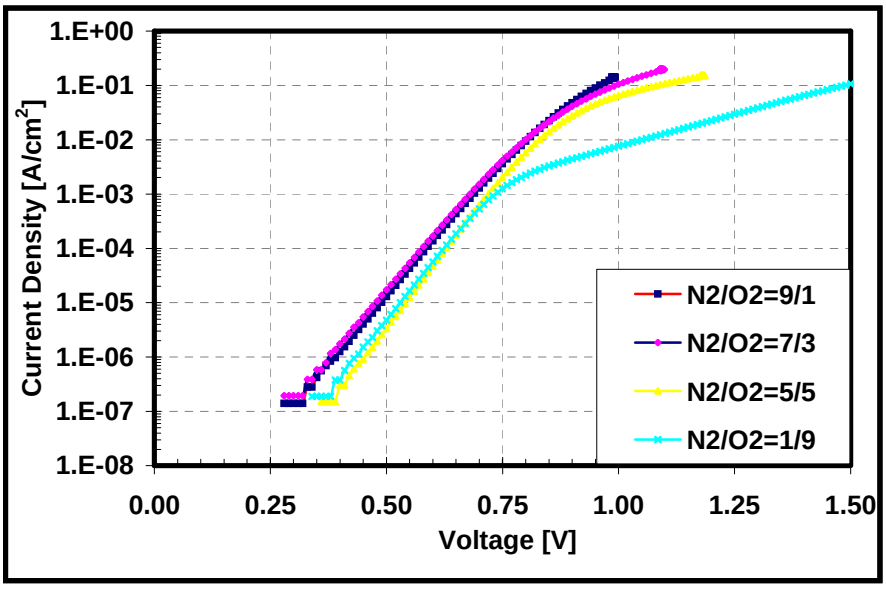


Figure 40 Dark I-V Characteristics for Device Fabricated at Various O_2 Concentrations (Thinner CdS)

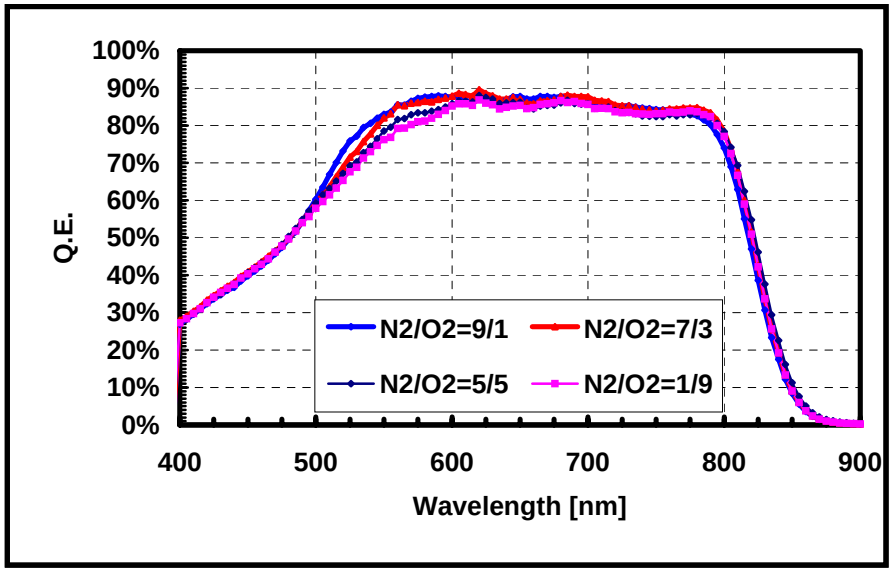


Figure 41 Spectral Response for Device Fabricated at Various O_2 Concentrations (Thinner CdS)

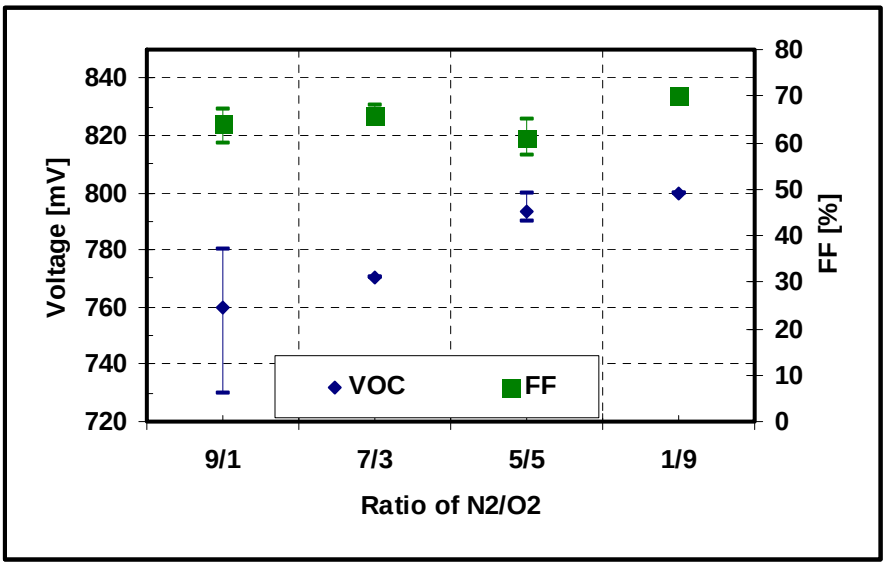


Figure 42 Summary Results for Device Fabricated At Various O_2 Concentrations (Thinner CdS)

are fairly same. Figure 42 shows the V_{oc} and FF with different O_2 partial pressure. The performance improves with increasing O_2 partial pressure, but at high O_2 partial pressure, no further improvement was observed.

5.4.4 Junction Properties with Different O_2 Partial Pressure

The diode factor A is an indicator of the quality of the main junction. Figures 43 and 44 show the parameters of the main junction versus the O_2 partial pressure. The diode factor A first decreases with increasing O_2 partial pressure and then increases at higher

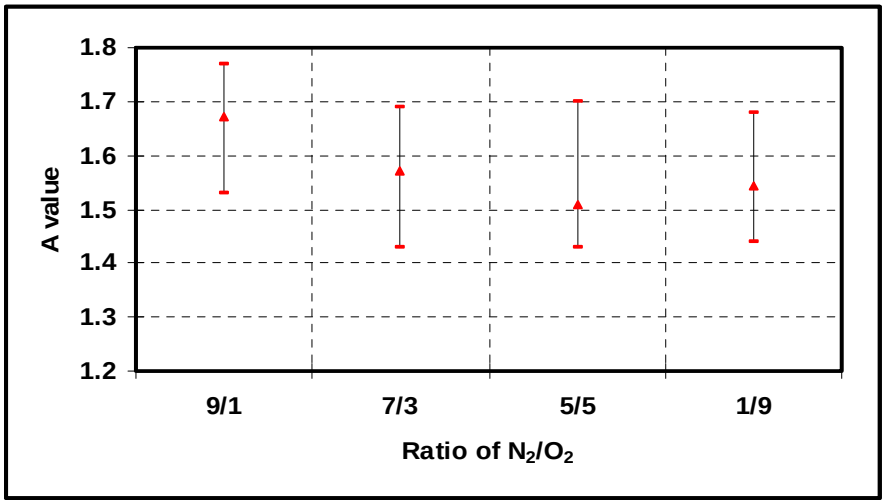


Figure 43 Diode Factor versus O_2 Partial Pressure

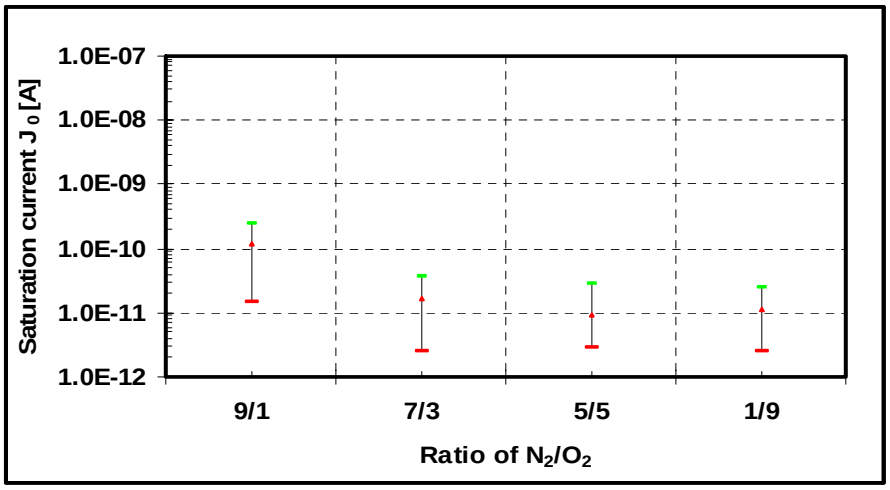


Figure 44: Saturation Current versus O_2 Partial Pressure

O_2 partial pressure, the same trend of junction saturation current is observed. Based on these two junction parameters, the quality of junction improves with increasing O_2 partial

pressure and reach highest quality at some point then degrades. The higher quality of the main junction is attributed to the condensed CdTe film, in which the shunting path was suppressed.

5.4.5 C-V Measurement

Figure 45 shows the C-V curves of the devices with different O_2 partial pressure. Table 7 shows the calculated depletion width and doping concentration based on these C-V measurements. In literature, O_2 can increase the hole concentration in CdTe. We did observe a small increase on hole concentration The doping concentration increases from $1.98x10^{14}$ to $3.46x10^{14}$ cm^{-3} with increasing O_2 partial pressure from N_2/O_2=9/1 to N_2/O_2=5/5 and then become saturated.

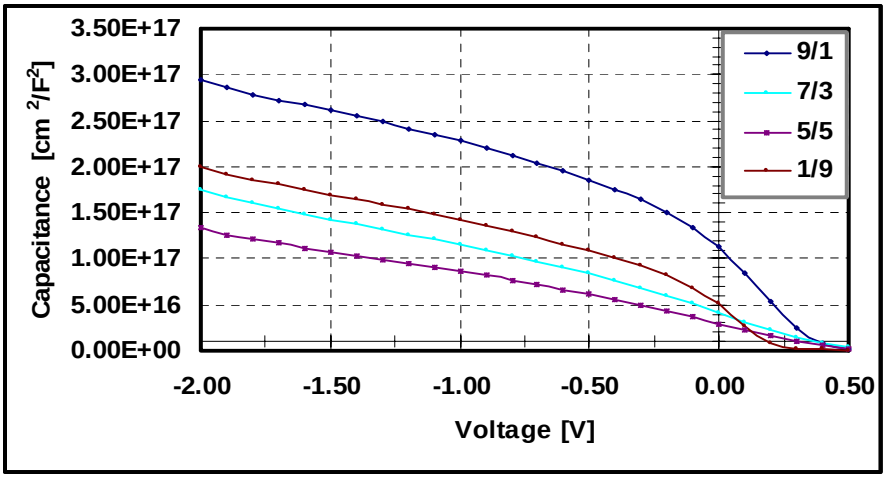


Figure 45: C-V Characteristics of Devices Fabricated with Different Partial Pressures

Table 7 Summary of Doping Concentrations for Varied Ratio of N_2/O_2

	N_2/O_2=9/1	N_2/O_2=3/7	N_2/O_2=5/5	N_2/O_2=1/9
N_A	1.98E14	2.77E14	3.46E14	3.4E14
W(μm)	3.03	1.82	1.98	2.03

5.5 Phosphorus Doped CdTe Devices

The CdTe cells used for this study were fabricated on 7059 boro-silicate glass substrates. The front contact consisted of MOCVD-deposited SnO_2: F and undoped SnO_2 layer. Cadmium sulfide was deposited using chemical-bath deposition (CBD), followed by the deposition of CdTe by close-spaced sublimation (CSS) in an inert ambient. We tried to incorporate P during CSS CdTe deposition by the mixture of CdTe and P powders. In order to achieve evenly mixed CdTe and Cd_2P_3 powder, the Cd_2P_3 powder and CdTe powder (approximately 5% at. of P) were mixed and sealed in an evacuated quartz ampoule. The quartz ampoule was gradually heated up to 700°C for about 48 hours. Then the mixture was removed, re-pulverized and remixed. The mixed powder was referred to as CdTe: P and was used to deposit CdTe: P film by CSS in He ambient. It has to be noted that the high efficiency solar cells in our lab were fabricated in O_2 ambient. Some CdTe films were subjected to $CdCl_2$ treatment and some were not. Two different $CdCl_2$ annealing temperatures were used. Subsequently the CdTe surface was etched using a Br_2/Methanol solution. The moly back contact is sputtered at room temperature in order to decouple the effects of the impurities from the graphite back contact. Then the cells were subjected to a post deposition annealing in inert ambient.

First we tried to deposit CdTe film directly from the powder mixture, but the film is unusually non-uniform; the reason for the observed non-uniformity is not clear, probably due to the non-evenly mixed powder. In order to get uniform film we made a very thick CdTe film from the powder mixture as the CdTe source for the deposition of CdTe thin film. The thick CdTe film was analyzed using EDS. EDS detects 3% at. of P

in the thick CdTe film, which is in relatively good agreement with the initial amount of P added in CdTe powder (5%at.).

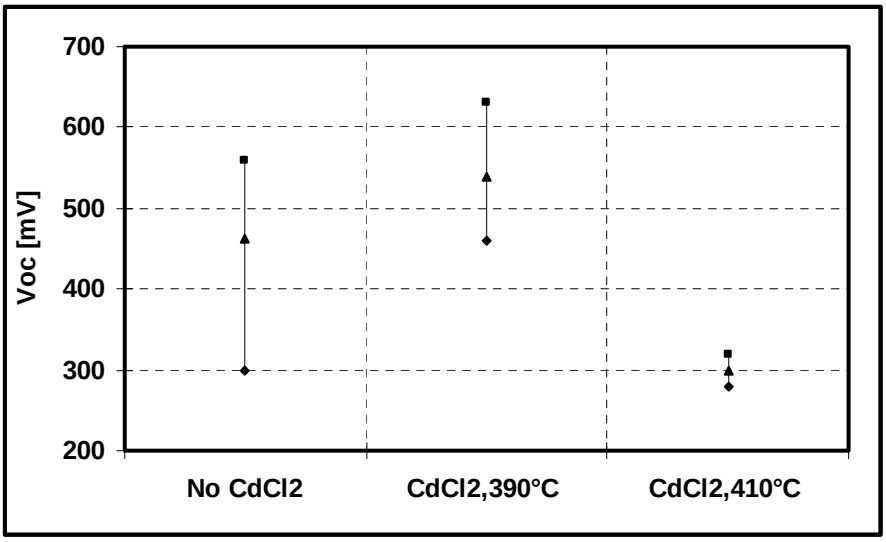


Figure 46 V_{oc} for Cells with Phosphorus

Figure 46 and 47 shows the cells performance with different $CdCl_2$ annealing conditions. All cells' performance is poor compared with our baseline cells. The V_{oc} is in the range of 300 to 620 mV; FF is in the range of 30 to 45%. The best cells form this group of cells were those $CdCl_2$ treated at 390°C. Figure 48 shows the I-V curve. These I-V curves indicate shunting is a main problem for the poor performance. The poor performance indicates the quality of the CdTe:P film is poor. One of these groups of CdTe:P films and again the thick source CdTe:P was analyzed using EDS. No P was detected; this doesn't mean there are no any P atoms in CdTe film and probably due to the limitation of EDS. These EDS results showed that P and CdTe have different transport rate during the CSS deposition process and the CdTe: P source may be depleted of P after several depositions. All these results showed the questionable quality of CdTe:P films indicating that CSS deposition technique is not suitable for the incorporation of P for doping purpose.

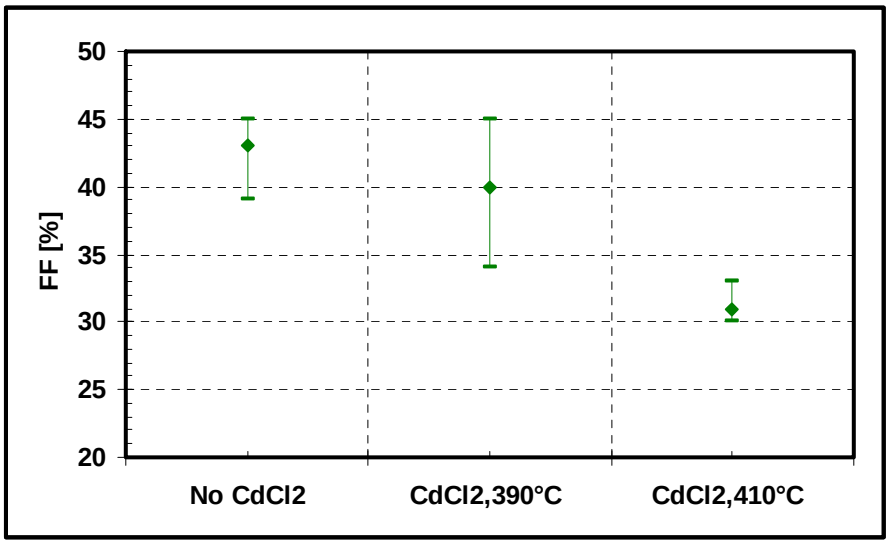


Figure 47 FF for Cells with Phosphorus

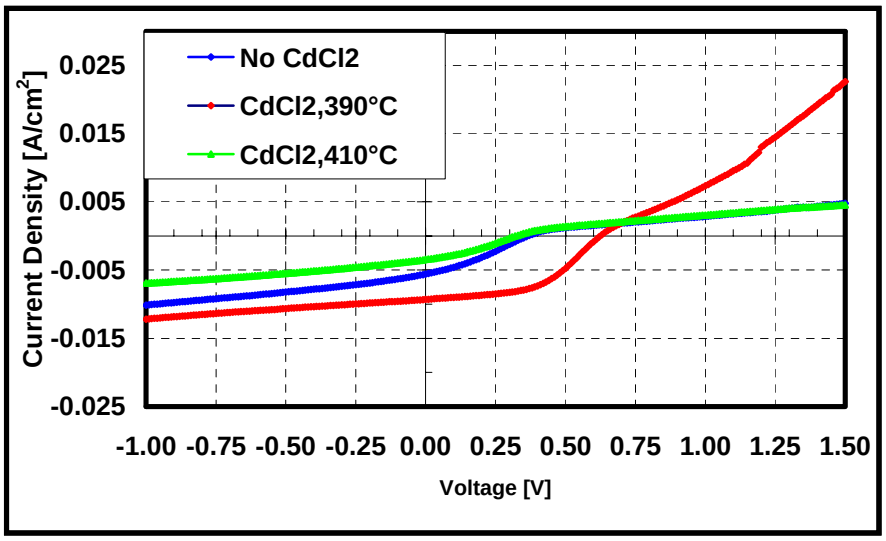


Figure 48 I-V Characteristics for Cells with Phosphorus

5.6 Antimony Doped CdTe Devices

Antimony (Sb) is another candidate of dopants for CdTe due to its low ionization energy, low diffusion coefficient, and easy of incorporation into CdTe. It has been used

as a back contact material to achieve high performance of CdTe solar cells [87]. Based on the experiments for P doped CdTe, we decided to incorporate Sb into CdTe through a post diffusion approach. Following the deposition of CdTe, a thin layer of Sb (20nm) was deposited onto CdTe by RF sputtering. The whole structure was subsequently heat-treated in an inert ambient at the near atmosphere pressure to suppress the evaporation. This heat treatment drives Sb to diffuse into CdTe. The annealing temperatures were varied from 300 to 525°C, and the durations from 20 to 160 minutes. The early experiments suggested that Sb could evaporate during the heat treatment; so another Sb coated glass (200nm) was used to cover the CdTe to act as an additional Sb source during the annealing. In order to investigate the role of Sb, the back contact was deposited by RF sputtered molybdenum at room temperature.

5.6.1 Effect of Sb

In order to investigate the Sb effect, two sets of cells were fabricated on the same substrate to eliminate experimental variations. The only difference between the two sets is that one set was subjected to the Sb-diffusion process and one set not. Figure 49 shows light J-V characteristics for cells with and without Sb. The J_{sc} was similar, but the V_{oc} for the set with Sb is 50 mV higher. The current at forward bias beyond V_{oc} was lower for the cells with Sb (Higher back barrier or roll-over). It is not clear at this moment what mechanism causes this behavior. One possible explanation is that the increased doping concentration near the back contact region results in larger band bending at the interface. The hole current was limited by this larger band bending. The doping profile shown in figure 50 partially supports this explanation. It must be mentioned that there is no

intentional copper in these devices. These results suggest that Sb could be used to increase the doping level in CdTe and avoid using copper to improve the long-term stability.

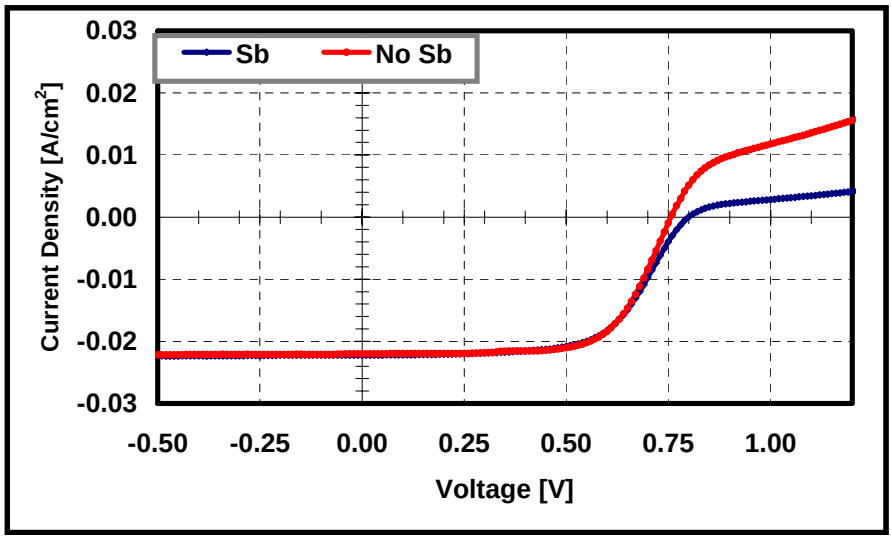


Figure 49 Light J-V Characteristics of CdTe Cells with and without Sb

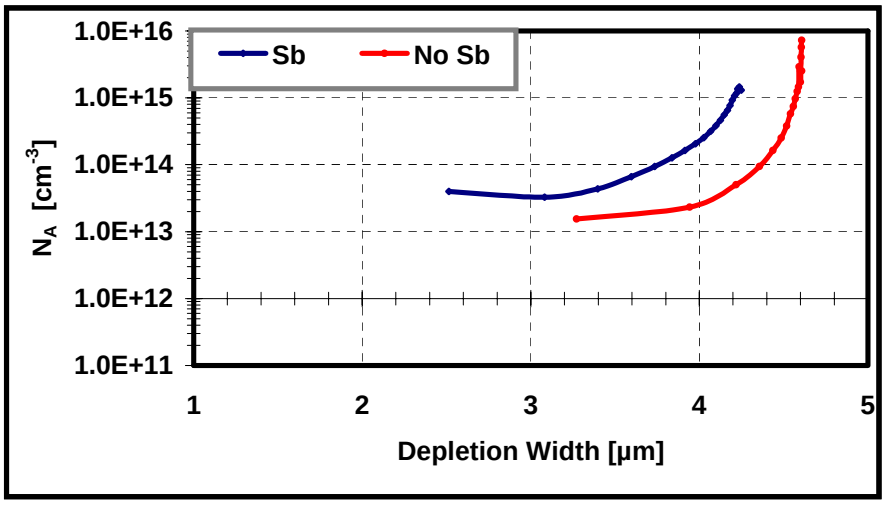


Figure 50 Doping Profile of CdTe Cells with and without Sb

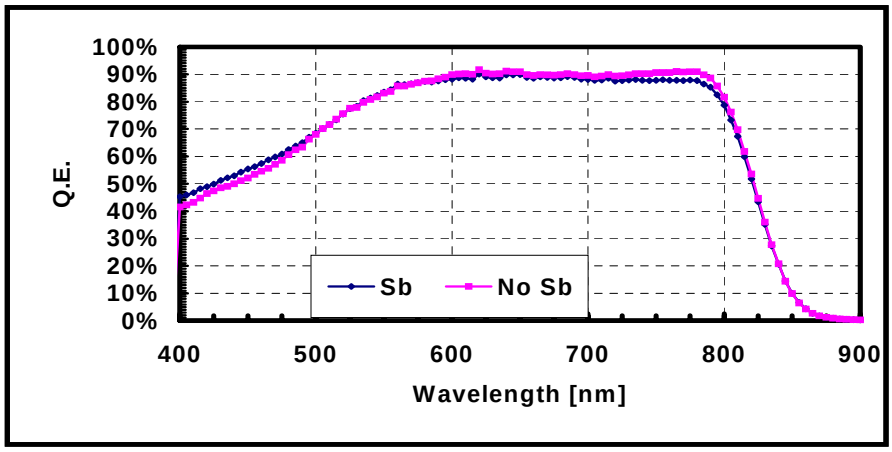


Figure 51 Spectral Response of CdTe Cells with and without Sb

The spectral response (figure 51) for the device without Sb is slightly higher than that of the device with Sb between 600 nm to approximately 825 nm. The difference becomes larger at longer wavelength although the absolute difference value is small. This is possibly because the higher carrier concentration in CdTe. Usually with the increasing of carrier concentration the collection efficiency decreases due to the shrinking of depletion with. From 400 nm to 500 nm, the QE is higher for the device with Sb. This is most probably due to the thinning of CdS during the Sb diffusion process. Table 8 summarizes these results.

Table 8 Summary of Results for the Devices with and without Sb

	J_{sc}[mA]	V_{oc} [mV]	FF[%]	Efficiency[%]
With Sb	21.99	800	62	11
Without Sb	22.14	750	68	11.3

5.6.2 Effect of the Sb Annealing Temperature

The diffusion depth and the amount of Sb in CdTe film depend on the annealing temperature and the duration. The annealing temperature also affects the properties of

CdS, CdTe, and the interface between CdS and CdTe. The annealing time was fixed for 25 minutes and the temperature varied from 400 to 525°C. NO $CdCl_2$ treatments were performed in this case. Table 9 summarized the process conditions and the cells' performance.

Table 9 The Process Conditions and The Cells' Performance with Different Annealing Temperature

	400°C	450°C	500°C	525°C
CdTe	O_2	O_2	O_2	O_2
Sb	200Å	200Å	200Å	200Å
HT	400°C, 25min with 2K Å coated glass	450°C, 25min with 2K Å coated glass	500°C, 25min with 2K Å coated glass	525°C, 25min with 2K Å coated glass
$CdCl_2$	N	N	N	N
Contact	Molybdenum	Molybdenum	Molybdenum	Molybdenum
V_{oc}	710-730	740-750	590	470
FF	37-41	41-44	29	38

The cell performance first increases when the temperature increased from 400 ˚C to 450˚C and then drastically dropped with the further increasing temperature. Figure 52 shows the spectral response with different annealing temperatures. At 400˚C and 450˚C, the QEs are fairly normal, but the QEs dropped drastically when the temperature is above 450˚C, further more, the QEs are constant with the wavelength up to 775nm. It looks like the cell's structure is CdS (n type)-CdTe (n type)-CdTe (p type), not the typical np junction structure. Figure 53 shows the QE simulation results of the nnp structure. In this simulation, the concentration of the n layer CdTe is fixed at $1x10^{16}$ cm^{-3}. The thickness of this n layer CdTe is varied from 0.02 to 1 μm. As can be seen, the QE drops with increasing thickness of n layer of CdTe. The difference between the simulated and the real cell's is that the QE of the simulated one is zero at short wavelengths and is

asymmetric. Due to this difference, the real case is not just the assumed nnp structure. A modified simulation was done. In the modified simulation, the structure is np, but donor defects are introduced. The acceptor concentration in CdTe is fixed at $1x10^{14}cm^{-3}$, donor

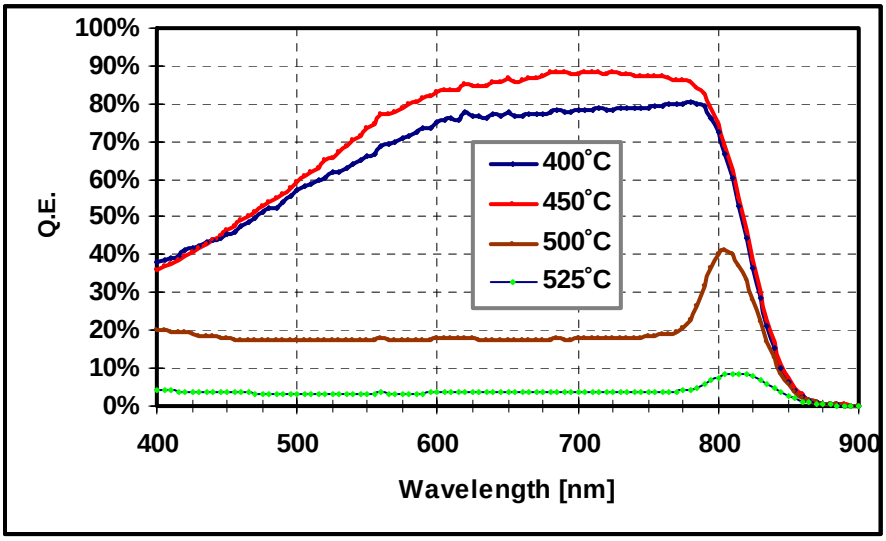


Figure 52 Spectral Responses for Device with Different Annealing Temperature

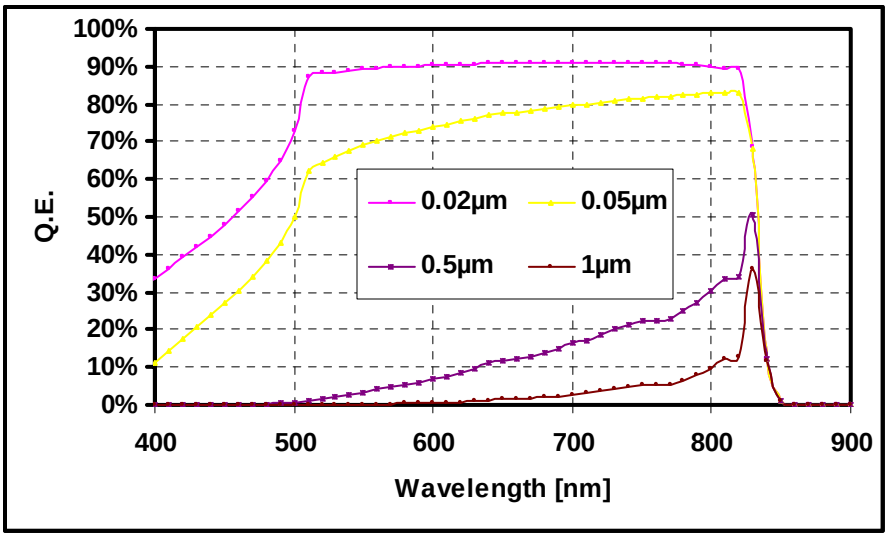


Figure 53 The Effect of The Thickness of N Layer CdTe on QE

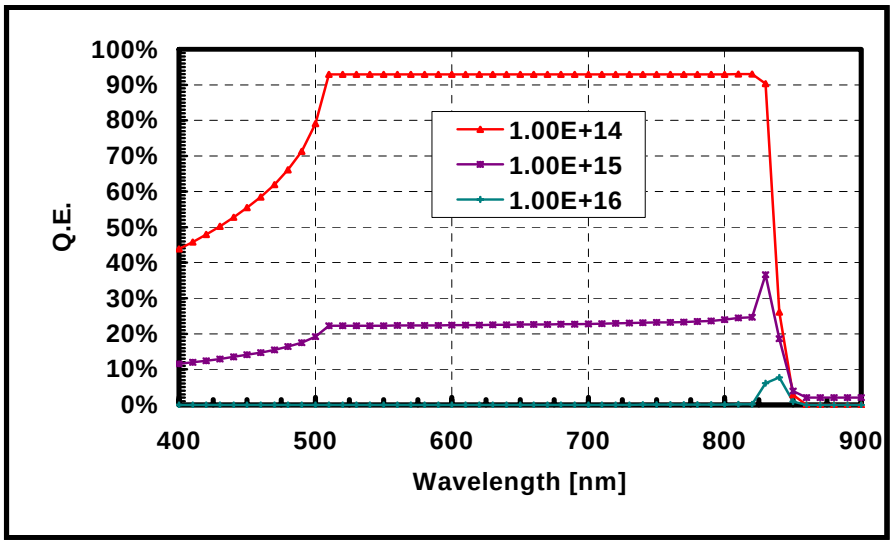


Figure 54 The Effect of Donor Defects in CdTe Bulk on QE

defects were varied from $1x10^{14}$ to $1x10^{16}$ cm^{-3}. Figure 54 shows the simulated QE curves. When the donor defects are higher than the acceptors, the QE shape is most likely close to the real case: constant below a specific wavelength depending on the level of donor defects. Based on this simulation, one tentative conclusion can be drawn: High temperature annealing results in high level donor defects in CdTe. The donor defects could be due to the diffusion of S from CdS at high temperature or due to the diffusion of Sb from the CdTe surface. Considering the high deposition temperature (>560˚C) of CdTe, the later one is closer to the truth: the high level donor defects are due to too much Sb diffused into CdTe and Sb atoms substitute the Cd atoms. It is already known that CdTe becomes semi-insulating material at very high concentration of Sb in CdTe and more Sb will occupy the Cd sites to compensate Sb_{Te} and V_{Cd} [88]. To verify this assumption, SIMS measurement has to be performed.

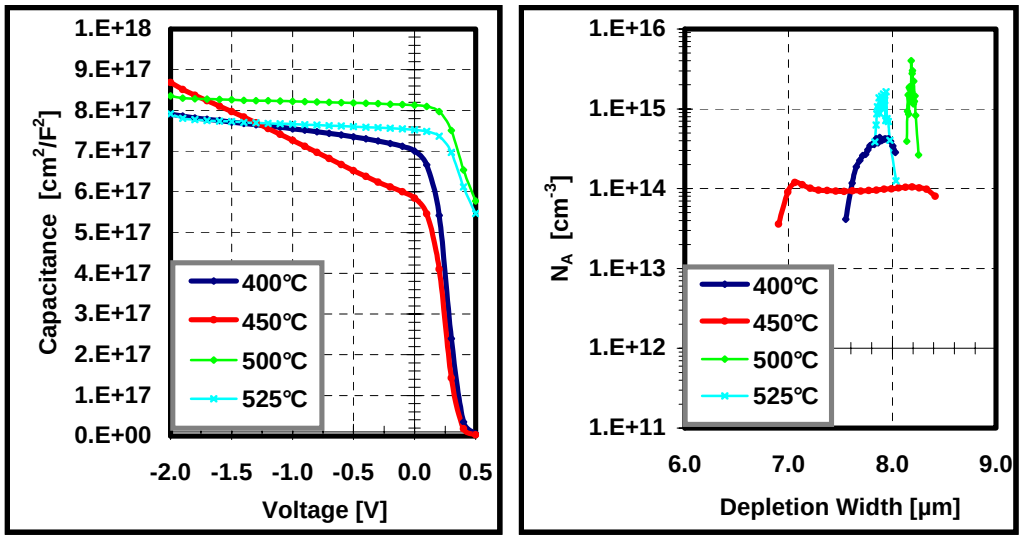


Figure 55: Doping Concentration Vs. Depletion Width (left) and C-V Characteristics (right)

Figure 55 shows the doping concentration and C-V characteristics. The doping concentration is deduced from C-V measurement. The higher annealing temperature leads to higher doping concentration. Table 10 shows the doping concentration at zero bias. The doping concentrations for 500 and 525˚C are up to $4x10^{14}cm^{-3}$. Considering the high defect density as we said before based on the QE, these high doping concentration may be over estimated, the real doping concentration should be lower or much lower than the deduced value from C-V measurement depending on the defect density.

Table 10 Doping Concentration and Depletion Width for the Cells Shown in Figure52

	400˚C	450˚C	500˚C	525˚C
W_D	7.55 µm	6.9µm	8.14 µm	7.83µm
N_A-N_D	4.1E13	1.2E14	3.9E14	3.8E14

5.6.3 Effect of Annealing Time

Due to the fact that high temperature annealing leads to high defect concentration, the Sb annealing temperature was fixed at 400˚C, while the annealing time was varied from 40 to 160 minutes. Table 11 shows the processing parameters and devices' performance. The cells treated for 40 minutes have the lowest performance, while the cells treated for 80-160minutes show basically same performance. The light J-Vs for representative cells are shown in figure 56. The cell with the lowest performance treated for 40 minutes also shows lowest back barrier (least roll-over). Again, it also shows lowest net carrier concentration (the same as we observed before: the cell with higher back barrier also shows higher net carrier concentration). To fully understand this phenomenon will require numerical modeling that can find a set of parameters to fit the experimental results such as light and dark J-V and SR. The essentially same performance for 80-160 minutes annealing may be due to the low diffusion coefficient.

Table 11 The Effect of Annealing Time

	40min	80min	120min	160min
CdTe	O_2	O_2	O_2	O_2
Sb	300Å	300Å	300Å	300Å
HT	400ºC,40min with 3KÅ coated glass	400ºC,80min with 3KÅ coated glass	400ºC,120min with 3KÅ coated glass	400ºC,160min with 3KÅ coated glass
$CdCl_2$	Y	Y	Y	Y
Contact	Molybdenum	Molybdenum	Molybdenum	Molybdenum
V_{oc} (mV)	700~730	750~770	730~770	740-770
FF(%)	58-63	60-62	61-63	61-64

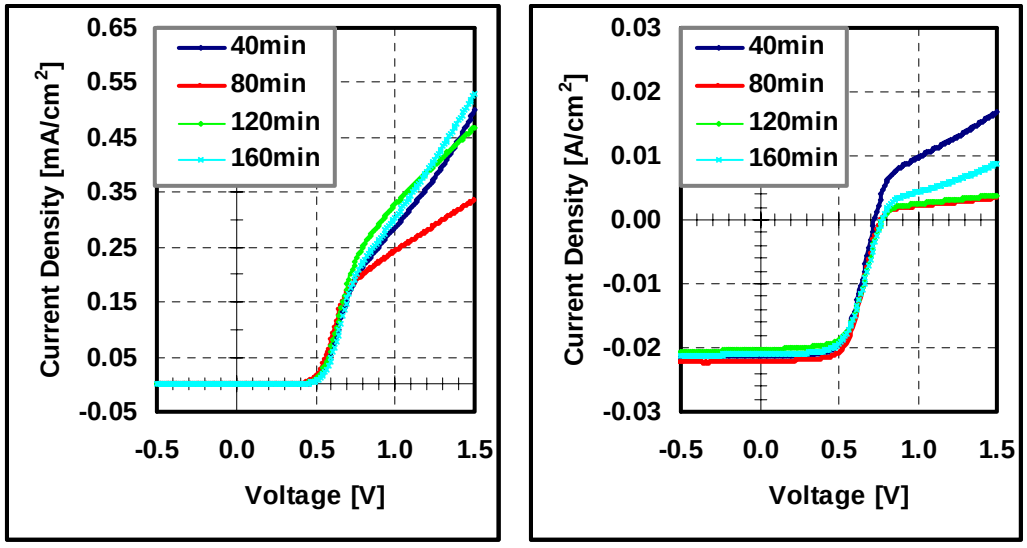


Figure 56 Dark (Left) and Light (Right) J-V Characteristics with Different Annealing Time

Figure 57 shows the spectral response of the devices shown in figure 56. The QEs' shape are all similar, 160 minutes annealing gives the best QE. The lowest QE is from the device annealed for 120 minutes. It is almost parallel to the highest one from 400nm to 900 nm, so this lowest QE is because of the thicker CdS, not caused by the Sb annealing.

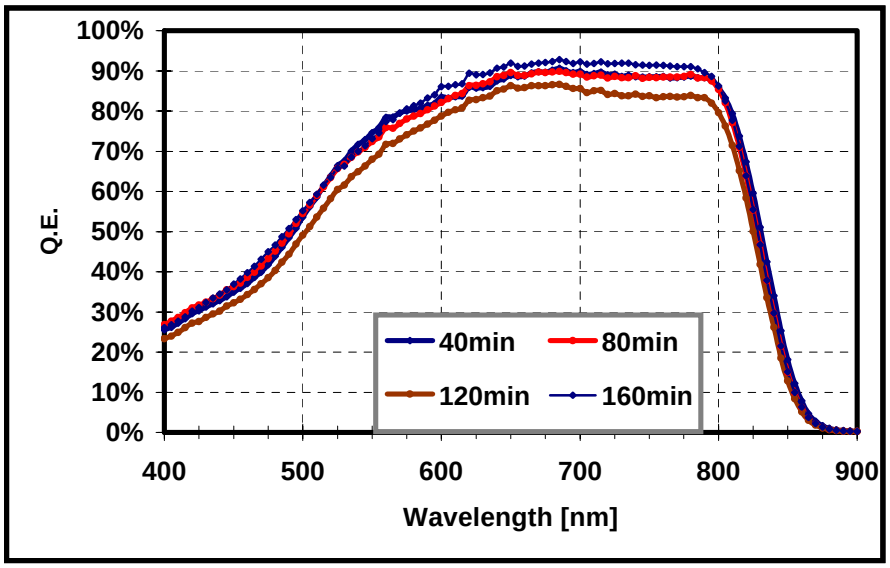


Figure 57 The QE of the Devices with Different Sb Annealing Time

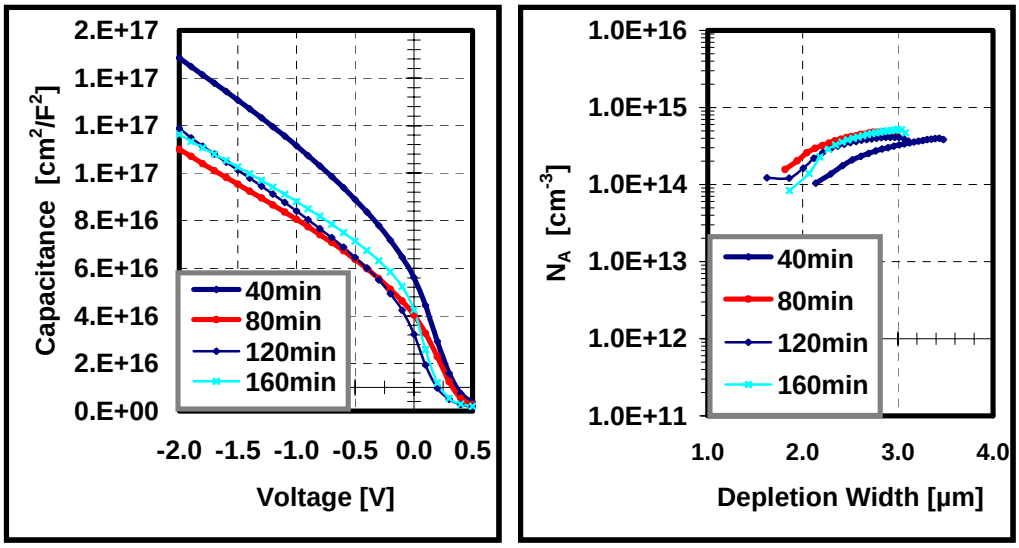


Figure 58 Doping Concentration Vs. Depletion Width (Left) and C-V Characteristics (Right)

Figure 58 shows the doping concentration and C-V characteristics with different annealing times. Although there is no single trend, but the highest doping concentration is from the longest annealing time, the shortest annealing times results in the lowest doping concentration. The partial conclusion we can draw from these experiments is that longer Sb annealing leads to higher doping concentration due to the diffusion of Sb into CdTe absorb layer.

5.6.4 The Effect of HCl Etching

After the Sb diffusion process, there is excess Sb (or Sb compound) left on the CdTe surface. It has been reported that Sb-Te can transform to Sb_2Te_3 under heat treatment [89]. In order to investigate its effect, the substrate was cut into two halves after Sb annealing; one half was subjected to HCl etching before the back contact application.

No $CdCl_2$ treatments were performed in this case. Table 12 summrizes the detail process conditions and devices' performance.

Table 12 The Effect of HCl Etching

	400ºC, HCl Etch	400ºC, No HCl Etch	450ºC, HCl Etch	450ºC, No HCl Etch
CdTe	O_2	O_2	O_2	O_2
Sb	200Å	200Å	200Å	200Å
HT	400ºC,25min with 2KÅ coated glass	400ºC,25min with 2KÅ coated glass	450ºC,25min with 2KÅ coated glass	450ºC,25min with 2KÅ coated glass
HCl	Y	N	Y	N
$CdCl_2$	N	N	N	N
Contact	Moly	Moly	Moly	Moly
V_{oc},FF	680-690,37-38	710-730,37-41	630-680,32-37	740-750,41-44

Figures 59 and 60 show the spectral response and the dark and light J-V plots. Although the performance is poor for both sets due to the no $CdCl_2$ treatment, the cells without HCl etching show higher V_{oc} and J_{sc}. The dark and light J-V show larger back barrier for the cells with HCl etching. For the HCl etched samples, the higher barrier could be due to the lower work function of molybdenum. For unetched samples, because Sb_2Te_3 has higher work function (4.93eV), it acts as a buffer layer between CdTe (5.1 eV) and molybdenum (4.49 eV) metal layer, so the barrier is reduced. The higher barrier for the HCl etched samples will limit the current flow, resulting in lower collection. The QE shown in figure 59 is consistent with this higher back barrier. It suggested that the excess "Sb" or Sb_2Te_3 compound at the surface of CdTe leads to a reduction in the back contact barrier. Antimony telluride has been used as an effective back contact to achieve high performance CdTe solar cells [30].

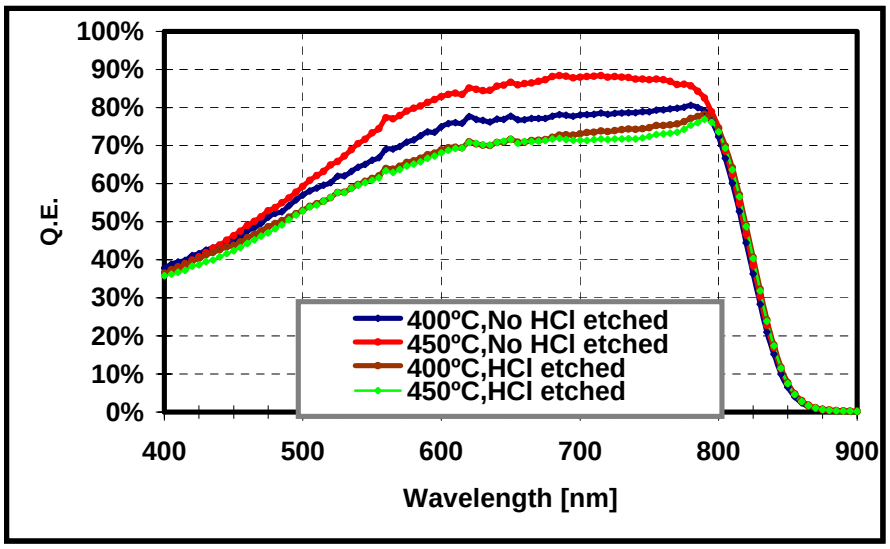


Figure 59: Spectral Response for HCl and No HCl Etched Devices

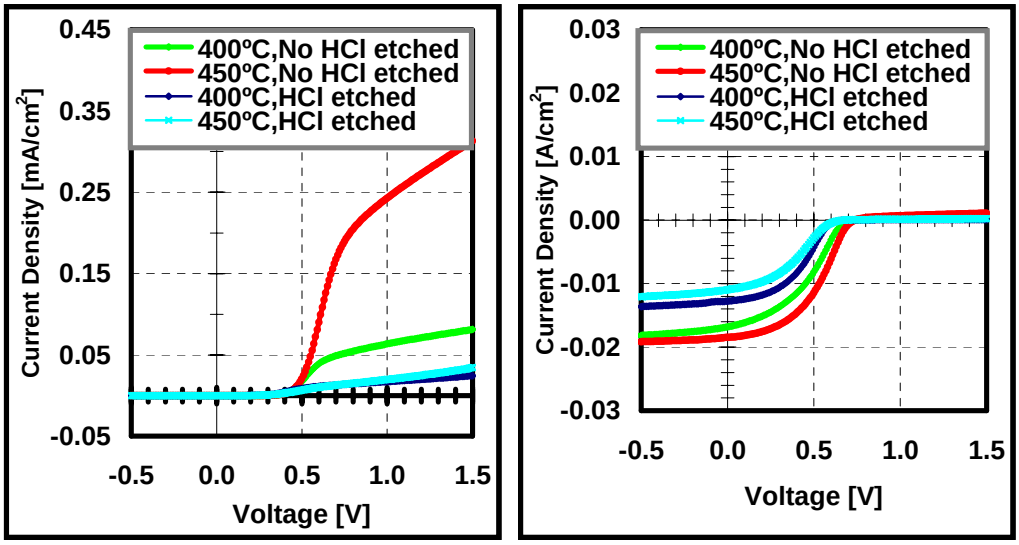


Figure 60 Light (Left) and Dark (Right) J-V for HCl and No HCl Etched Devices

5.6.5 $CdCl_2$ Effect on CdTe:Sb Devices

The cadmium chloride ($CdCl_2$) treatment is crucial in the device fabrication of polycrystalline CdTe/CdS solar cells. It can increase the grain size and passivate the grain boundaries (GBs) in the CdTe active layer. It also reduces recombination in these

devices. Recent investigations showed that $CdCl_2$ treatment affects the interior of CdTe grains by the potential incorporation of electrically active impurities. Here we studied the effect of $CdCl_2$ treatment on the Sb doped CdTe devices. Table 13 summaries the process and the comparative results. The devices with $CdCl_2$ treatment have much better V_{oc} and FF. The V_{oc} is increased from mid 700 mV to 830mV, FF from 40 to 62%.

Table 13 $CdCl_2$ Treatment on Sb Doped Devices

	No $CdCl_2$	No $CdCl_2$	$CdCl_2$ Treated	$CdCl_2$ Treated
CdTe	O_2	O_2	O_2	O_2
Sb	200Å	200Å	200Å	200Å
HT	400ºC,25min with 2K Å coated glass	450ºC,25min with 2K Å coated glass	430ºC,25min with 2K Å coated glass	430C,25min with 2K Å coated glass
$CdCl_2$	N	N	Y	Y
Contact	Molybdenum	Molybdenum	Molybdenum	Molybdenum
V_{oc}, FF	710-730,37-41	740-750,41-44	800-810,61-61	810-830,61-62

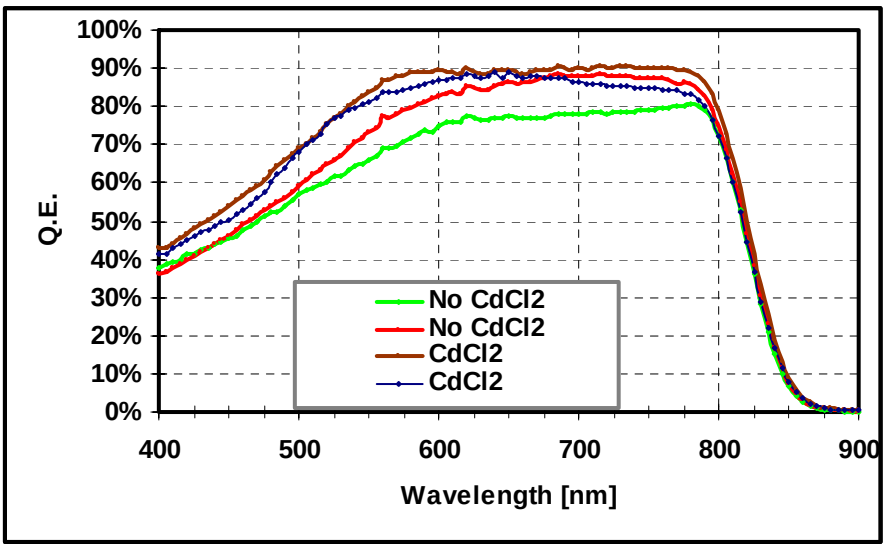


Figure 61 Spectral Response for The Devices with and without $CdCl_2$ Treatment

Figure 61 shows the spectral response for the devices with and without $CdCl_2$ treatment. The devices without $CdCl_2$ treatment have lower QE for the whole range from 400nm to 800 nm, especially in 400nm to 550nm. We assume the beginning CdS

thickness is same because of the same deposition parameters of CdS. It clearly shows the final thickness of CdS is thinner for $CdCl_2$ treated devices than those untreated (Based on the QE at 450nm). In the range of 500 to 600nm, the QEs for $CdCl_2$ treated devices are higher than untreated devices, indicated that $CdCl_2$ treatment promotes the formation of $CdTe_xS_{1-x}$ at the CdTe/CdS interface. This is consistent with the previous study from different groups.

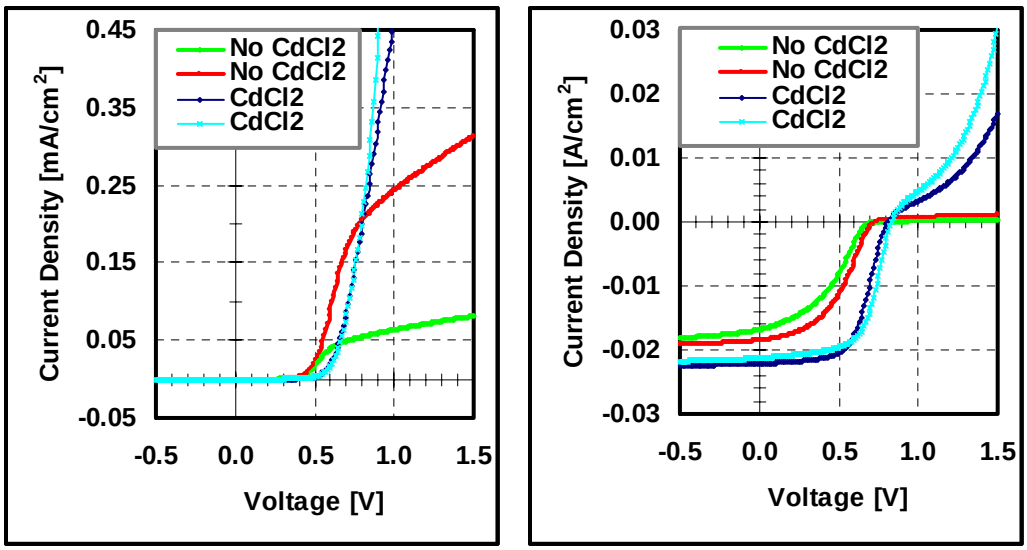


Figure 62 Light (Left) and Dark (Right) J-V for the Devices with and without $CdCl_2$ Treatment

J-V characteristics (Figure 62) show that the back barrier for the $CdCl_2$ treated devices is much lower than those untreated devices. This is primarily due to the passivation of the surface state. The untreated cells also showed lower short circuit current density J_{sc} and FF. This is mainly due to the large back barrier which limits the hole current and the collection efficiency.

We also compared the effect of $CdCl_2$ treatment before Sb deposition and after the Sb annealing. When the $CdCl_2$ treatment is done before Sb annealing, the performance is only a little bit better than untreated devices. This could be because Sb annealing leaves Sb related defects that can't not be passivated without $CdCl_2$ treatment.

5.6.6 Two-layer CdTe Devices

Based on the results for the different Sb annealing times, we suspected that Sb may not diffuse into the deep bulk of CdTe due to its low diffusion coefficient. A series of experiments have been done to investigate the effect of the "Sb depth" in CdTe. A layer of CdTe with different thickness was first deposited in O_2 ambient (Labeled with deposition time), and then the Sb was sputtered and diffused into CdTe. After Sb diffusion process, another layer of CdTe was deposited onto the first layer of CdTe. The thickness of the first layer (the antimony depth) and the CSS ambient of second layer CdTe were varied.

5.6.6.1 The Effect of the CSS Ambient of Second Layer CdTe

The CdTe of our baseline devices is deposited in O_2 ambient. As we already know that O_2 ambient can increase the doping concentration, reduce the grain size and improve the main junction properties, so the first layer of CdTe was deposited for two minutes in O_2 ambient in order to have a good main junction. In this study, the deposition ambient of of second layer CdTe was varied (Table 14). The label "O_2-O_2" means the both CdTe layers are deposited in O_2 ambient, O_2-He means the second layer CdTe was deposited in He ambient. Figure 63 and Figure 64 show the light and dark J-V characteristics. The O_2-

He cells have higher J_{sc}, FF, and lower Rs than O_2-O_2 cells. The cells for both cases have essentially the same V_{oc}. The roll-over observed in both light and dark curves at higher

Table 14 Summary of the Devices with Different Ambient for 2nd layer CdTe

1st CdTe	O_2	O_2
Sb	200Å	200 Å
HT	430ºC,60min with 2K Å coated glass	430ºC,60min with 2K Å coated glass
HCl etch	N	N
2nd CdTe	He	O_2
$CdCl_2$	Y	Y
Contact	Moly	Moly
V_{oc},FF	820, 62	780~810,32-38

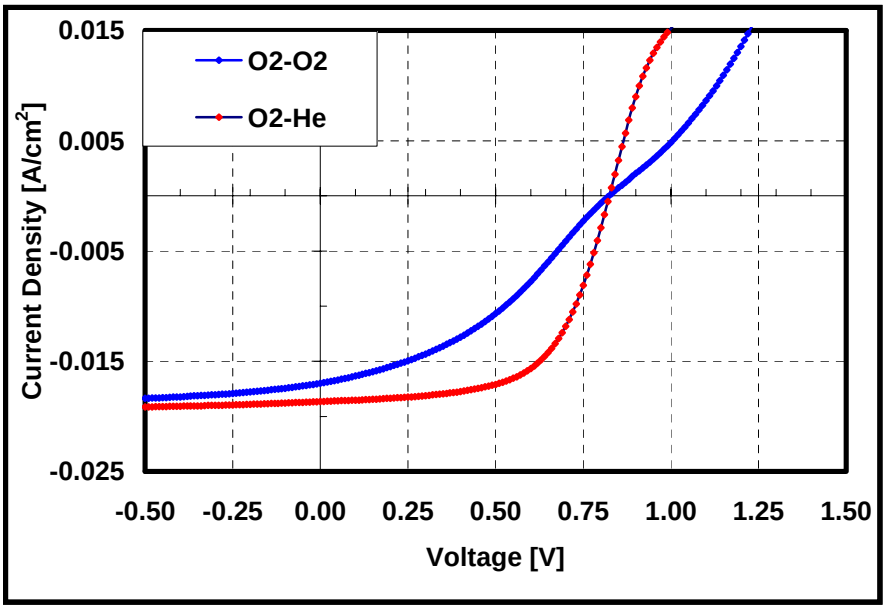


Figure 63 Light J-V of the Devices Fabricated in Different Ambients (2nd Layer)

forward bias, suggests that the contacts are rectifying. However at lower bias (close to V_{oc}) for O_2-He samples, the presence of a smaller barrier makes carrier transport easier thereby causing no adverse effects on the fill factor of the device. The reverse saturation

currents are similar. From the spectral response (Figure 65), we can see the recombination rate for O_2-O_2 cell increases towards main junction, while O_2-He cell doesn't. This may be due to the formation of some Sb-O related defects or a thin layer of Sb_2O_3.

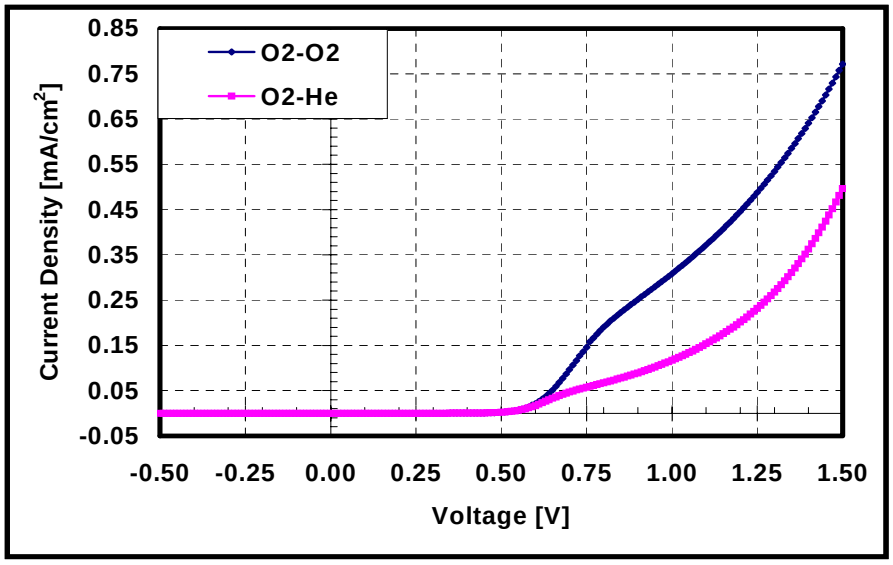


Figure 64 Dark J-V of the Devices Fabricated in Different Ambients (2nd Layer)

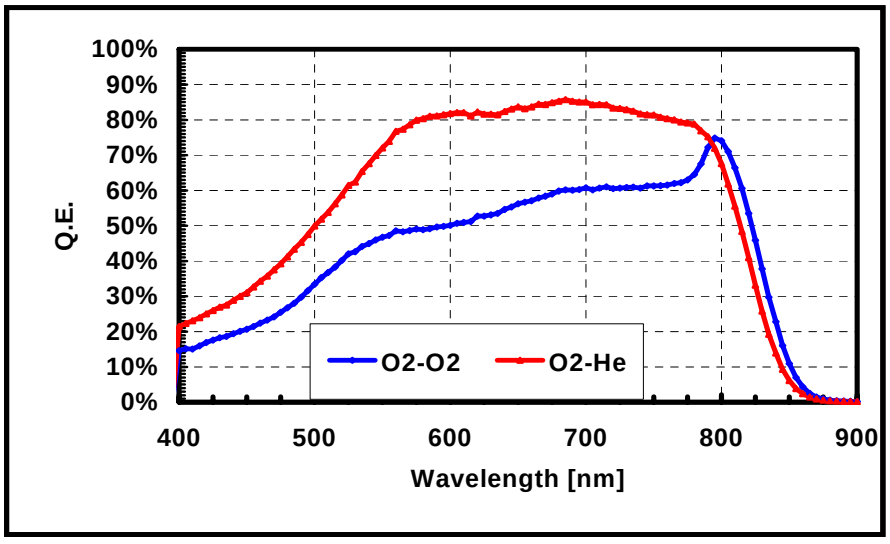


Figure 65 Spectral Response of the Devices Fabricated in Different Ambient (2nd Layer)

5.6.6.2 The Depth Effect of Sb in CdTe

By varying the thickness of the first layer of CdTe, the depth of Sb was varied. Figure 66 shows the dark J-V characteristics for the representative cells. As can be seen, the turn-on voltages are almost identical, but the current was suppressed more for thinner first CdTe layer beyond 0.8 volt. From the light J-V shown in figure 67, the back barriers are almost same. It seems the Sb diffused into the interface region and the properties of CdS was affected. The collection was increased at around the maximum power point for a thinner first CdTe layer. We can tentatively conclude that the increased doping level results in higher built-in potential that improved the collection. The calculated hole concentration from C-V measurement is $4X10^{16}$ cm^{-3}.

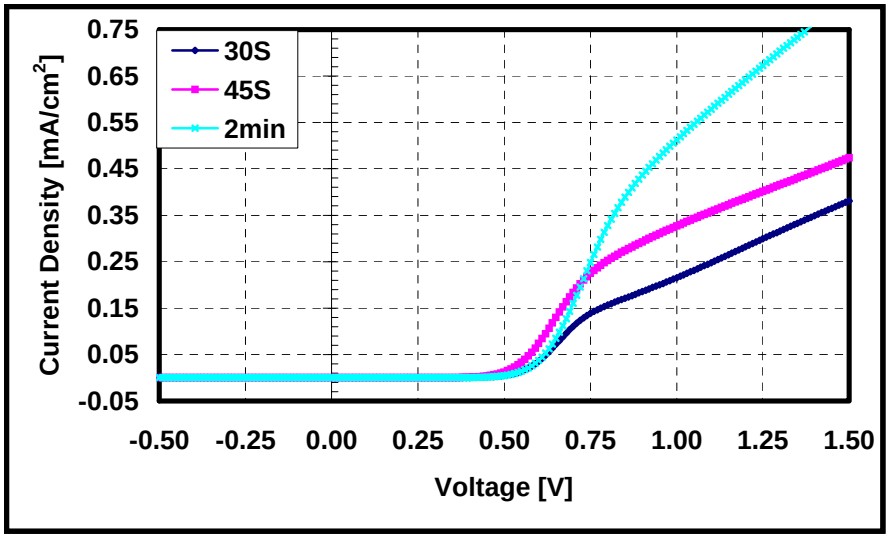


Figure 66 Dark J-V Characteristics of CdTe Cells with Different Thickness of First Layer

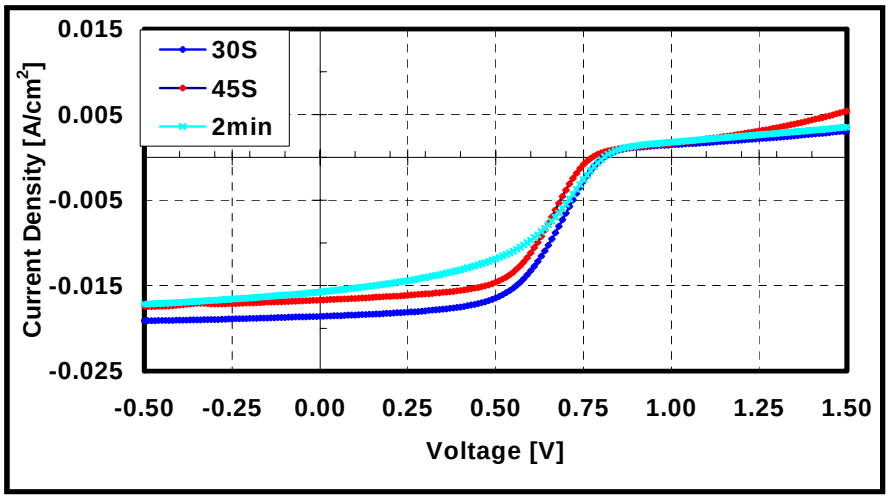


Figure 67 Light J-V Characteristics of CdTe Cells with Different Thickness of First Layer

5.6.7 The Effect of Back Contact

The effect of back contact deposition conditions is also studied. In this study, the sputtering pressure and sputtering rate are varied. Four combinations were used: high pressure- high sputtering power (L-H), low pressure-low sputtering power (L-L), high pressure-low sputtering power (H-L), and high pressure-high sputtering power (H-H). Table 14 shows the comparative device data for different back contact conditions. Figure 68 and 69 show the J-V characteristics.

Table 15 Comparative Device Data for Different Back Contact Conditions

	H-L	L-L	L-H	H-H
CdTe	O_2	O_2	O_2	O_2
Sb	300Å	300Å	300Å	300Å
HT	400°C,80min with 3KÅ coated glass	400°C, 80min with 3KÅ coated glass	400°C,80min with 3KÅ coated glass	400°C,80min with 3KÅ coated glass
$CdCl_2$	Y	Y	Y	Y
Contact	Molybdenum (H-L)	Molybdenum (L-L)	Molybdenum (L-H)	Molybdenum (H-H)
V_{oc} (mV)	740	790	780	710
FF (%)	53	50	57	51

It was observed that the best cell performance is from low pressure – high sputtering power condition and then the low pressure-low sputtering power. Both devices fabricated at high-pressure show poor performance and severe roll-over. It is clear that the low pressure is a key processing parameter to achieve a better back contact. G.Gordillollo's study shows that the resistivity is decreased by decreasing the sputtering pressure and increasing the glow discharge power. The reduction of the resistivity is attributed to the increasing carrier mobility due to an increment of the grain size. [90] Our studies also show the same trend. Although the decrease on resistivity is not obviously seen in the J-V curves due to the severe back barrier effect, it still could be an factor for the improvement of cell performance. Another reason for the improvement of cell performance is that at low pressure and high sputtering power, the sputtered particles have higher energy. These high energy particles can affect the surface state in a way which can lower the back barrier (see figures 68 and 69). The adhesion, though not yet confirmed, is suspected to be improved at low pressure-high power condition.

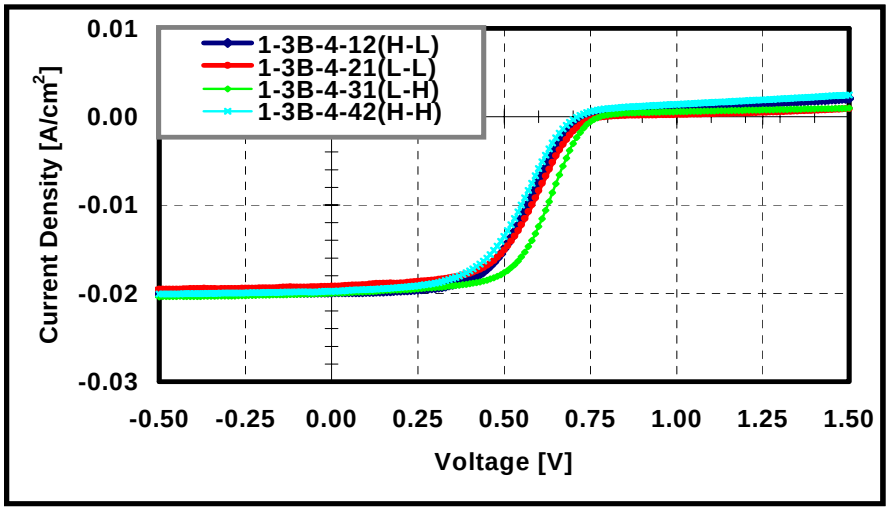


Figure 68 Light J-V for The Devices With Different Back Contact Conditions

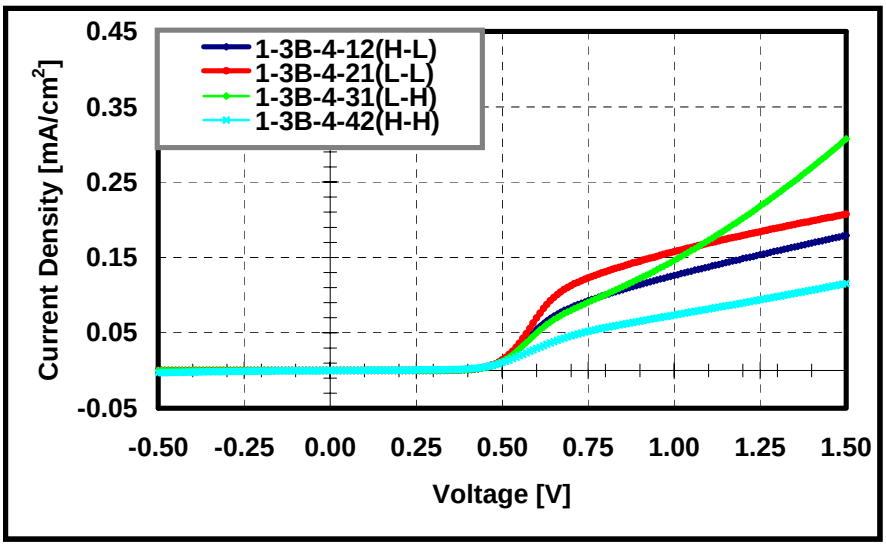


Figure 69 Dark J-V for the Devices with Different Back Contact Conditions

5.7 V_{oc} Versus Doping Concentration

So far we studied the CSS CdTe ambient effect and Sb effect on doping concentration. In the ambient effect study, a weak trend was observed: the doping concentration and V_{oc} increased with the O_2 partial pressure. In the Sb effect study, the effect of processing parameters on the carrier concentration was studied by varying the annealing temperature and annealing time. Carrier concentrations up to 10^{16} cm^{-3} were observed. Figure 70 shows the summary of V_{oc} versus doping concentration. Clearly, this graph can be partitioned into four regions (showed in figure 70). Regions 1 and 2 with empty legends show V_{oc} versus doping concentration for the $CdCl_2$ treated devices. Regions 3 and 4 with solid square legend is for the not $CdCl_2$ treated devices. More than 100 mV V_{oc} difference exists between the $CdCl_2$ treated and not $CdCl_2$ treated devices at similar doping concentrations.

In regions 1 and 3, although there is fluctuation, the general trend is up. While in regions 2 and 4, the trend reversed. It is also observed that depending on the process conditions, high V_{oc} (830mv) can be achieved at both low (10^{14}) and high concentrations (10^{16}). In order to understand what factors are mainly responsible for the reduction of Voc at different doping concentrations, simulation has been done to fit the curvature showed in figure 70 by varying back barriers, defect density, and carrier life time.

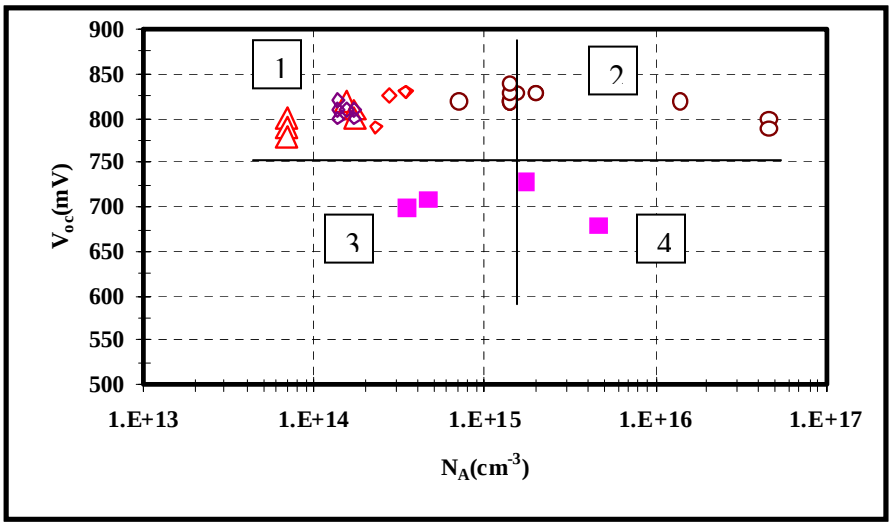


Figure 70 Voc Versus Doping Concentration at Different Process Conditions

It was founded that back barrier played an important role at regions 1 and 3. When N_A is 2.8×10^{14} cm^{-3} with perfect ohmic contact, the V_{oc} is 855 mV. In order to achieve 830 mV V_{oc}, the back contact barrier must be less than 0.13 eV. Above this value, even the CdTe is free of defects, the V_{oc} is still below 830 mV. Figure 71 shows the simulation result in which the parameters are: N_A: 2.8×10^{14} cm^{-3}, no any defects, and back barrier: 0 eV, 0.13 and 0.2 eV. We can see that the V_{oc} dropped to 780 mV when back barrier is 0.2 eV. This is the ideal case. Normally in CdTe solar cells, N_A is around 2×10^{14} cm^{-3}, and there always exist defects more or less depending on process

parameters. This indicates that the copper doped graphite contact is an near ohmic contact and the defect density is very low and has minor effect on V_{oc}. Due to the fact of the low work function of molybdenum (4.6eV), the V_{oc} is difficult to be above 830 mV at low doping concentration for the cells with Moly back contact unless there is high density and shallow acceptor-like defects. For example, if there is 0.3eV back barrier, the following parameters have to be used to achieve 830 mV Voc with 2×10^{14} cm^{-3} doping concentration: $N_T=2 \times 10^{16}$ cm^{-3}, $E_T=E_v + 0.1$ eV, $\delta_n= \delta_p=10^{-18}$.

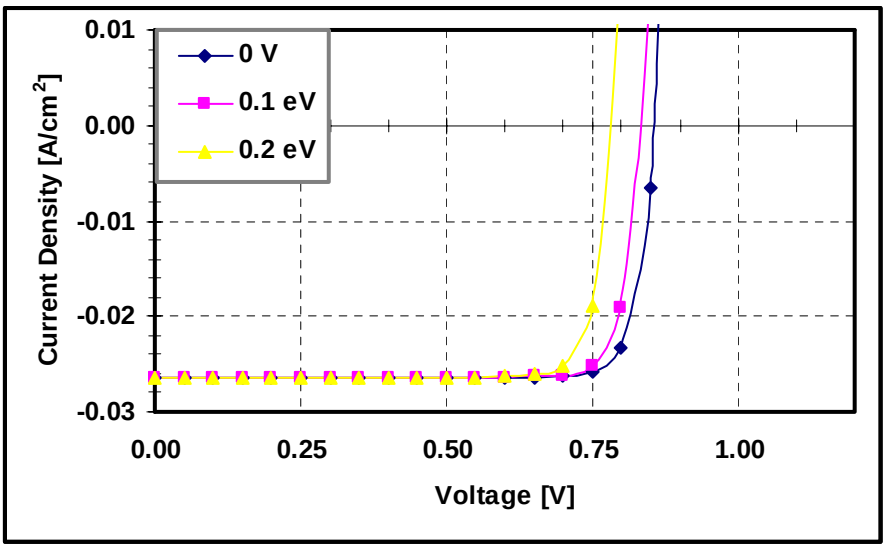


Figure 71 I-V Simulations with Different Back Barriers

In order to increase doping concentration, external impurity has to be introduced into CdTe by any means. On the other hand, the introduction of external dopant atoms, it is unavoidable to introduce some defects to compensate the acceptors and the defects density depends on the amount of external dopant atoms and process parameters. In figure 70, it looks like V_{oc} reaches its maximum value at the doping concentration of around 10^{15} cm^{-3}. Simulation shows that at such high doping concentration and 0 eV back barrier, without any defects, the V_{oc} could be 905mV. The experimental V_{oc} is 840 mV.

In order to fit this value, donor defect density up to 5×10^{14} cm^{-3} , electron capture cross section up to 10^{-12} , and with 0.2eV back barrier have to be used.

In region 2, when the doping concentration is 2×10^{16} cm^{-3}, the V_{oc} dropped to 820 mV. While the ideal V_{oc} is 968 mV. To fit this experimental value, parameters such as 0.37eV back barrier, electron and hole capture cross section up 10^{-11} and donor defect density up to 4×10^{13} cm^{-3} have to be used. It has to be noted that the V_{oc} is not sensitive to low back barrier. When the back barrier was reduced to 0.32 eV, the V_{oc} only changed several mVs, but the forward current increased, this kind of shape IV was just what we observed for some devices(Figure 72).

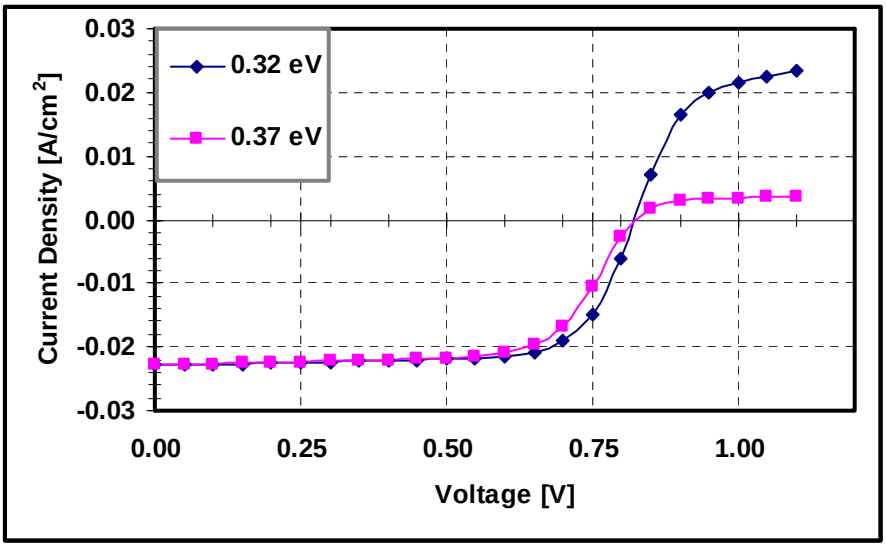


Figure 72 I-V Simulations with Different Back Barriers for 2×10^{16} cm^{-3}

J-V curves show higher back barrier for devices with higher doping concentration. At higher doping concentration, the Fermi level will shift downward, so the -work function of CdTe increases, resulting in an increase of the back barrier. The work

function of CdTe with 2×10^{16} cm^{-3} is 0.1 eV higher than that of CdTe with 2×10^{14} cm^{-3}. So the back back barrier of CdTe with 2×10^{16} cm^{-3} is 0.1 eV higher than that of CdTe with 2×10^{14} cm^{-3}. How ever, if the doping concentration is high enough, tunneling contact will form and the barrier will actually decrease. It is still questionable whether the contact is tunneling or not, however, our results show that $10^{16}cm^{-3}$ is not enough to form a tunneling contact.

QE data show that the recombination rate is higher at higher doping concentrations, which indicate that more defects were induced by the introduction of higher Sb content. This is consistent with the simulation results. Grain boundary exists in CSS CdTe in nature and defects tend to segregate there. Although the Sb diffusion process may not change the grain boundary density, the defect density at grain boundary would increase due to this process. In general, it is much more likely that GBs lead to a majority carrier depletion in p-type material, the Fermi-level is close to the valence band and deep states are most likely positively charged or neutral. What electrons (minority carriers) see is a potential well, so the recombination will increase. $CdCl_2$ treatment can passivate some defects at some degree. It is obvious that the defects concentration is over the capability of $CdCl_2$ treatment in this case. If the defects can be removed or reduced to some acceptable level, we should see an increase of V_{oc}.

CHAPTER 6

CONCLUSION

The primary objective of this project is to explore new materials and processes that will improve the performance of CdTe/CdS solar cells. The main efforts focused on improving the open circuit voltage by the following areas:

(1) Investigation the effect of the ambient of CSS CdTe on the performance and net doping concentration in CdTe layer.

(2) Investigation the effects of extrinsic impurities in CdTe absorber layer. In this case, we studied phosphorus (P) and antimony (Sb).

(3) The front contact with the case focused on Zn_2SnO_4 (ZTO) buffer layer.

Zn_2SnO_4 as a high resistive buffer layer was also studied. The effect of the deposition and annealing temperature on material structure and device performance was studied. The film deposited at 400°C yielded very high blue spectral response and high V_{oc} at the same time. A more thorough study of the buffer layer mechanism will further help optimize device performance.

The effect of the ambient of CSS CdTe was investigated. The mixture of N_2 and O_2 was used in this study. The morphology of the CdTe films is independent on the ratio of N_2/O_2 as long as there is O_2. The performance of the cells increases with the partial pressure of O_2. The net carrier concentration is in the normal range of 10^{14} cm^{-3}, but we

did observe a small increase with the concentration of O_2 and getting saturated at high content of O_2. The quality of the main junction is improved with the increasing partial pressure of O_2.

The effects of phosphorus and antimony in CdTe absorber layer were studied. The initial effort focused on incorporating phosphorus into CdTe by mixing P with CSS CdTe source. The attempt is not successful due to the inhomogenieties in the P-doped CdTe powder and different transportation rate of P and CdTe. The Sb effect was studied by diffusion approach. The effect of antimony annealing temperature and time, $CdCl_2$ treatment, the excess antimony on CdTe, and the depth of antimony in CdTe on cell performance was studied. The amount and the depth of Sb in CdTe were not known at this point due to the inability of the SIMS measurement in our laboratory. The junction of the devices annealed above 500°C crashed. It is not clear whether it is due to the diffusion of antimony or not. SIMS result and defects identification will help understand the causes. The excess Sb/orSb_2Te_3 is found to be helpful to reduce the back contact barrier. A consistent increase in the hole concentration was also observed. Our work clearly shows that the both V_{oc} and the doping levels in the CdTe:Sb device are higher (the V_{oc} by 50 mV), suggesting increasing the doping in CdTe further could potentially yield even higher V_{oc} as expected.

Since the doping study by this diffusion approach is not very successful, the future work should focus on other doping techniques such as sputtering and co-evaporation and also other p type dopants. Co-evaporation is recommended to be first investigated since it is favorable for manufacture. Introducing ionized N in CSS CdTe process is also worth to study.

In addition, an attempt has been made to synthesize $TiSe_2$, which has high work function and could be used to form ohmic back contact. Although it is failed to selenize the Ti film on CdTe due to the high temperature at this stage, it is worth to try other means like co-evaporation and sputtering to deposit $TiSe_2$ on CdTe to test the possibility as a candidate of an ohmic back contact material.

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