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Copper doped window layer for CdSe solar cells

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Copper Doped Window Layer for CdSe Solar Cells

by

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DEDICATION

To everyone who helped me in my endeavor

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Sheetal Kumar Chanda

ABSTRACT

CdSe solar cells with ZnTe as the window layer deposited by CSS process have shown V_{oc}'s around 630mV. However the currents were very low and also the voltages were not meeting the desired objectives. To improve the performance the contact energy at the ZnTe/Cu interface should be minimized by doping the window layer.

Thermal evaporation was used to deposit ZnTe to have more control over the composition of the film. Initial experiments were done by depositing Cu doped ZnTe films on plain glass by co-evaporating both ZnTe and Cu. The conductivity was in the order of 10e3 which shows copper present in the film in the order of 1e22 S/cm^3. This accomplishes a tunneling contact with the top electrode. Using the ZnTe:Cu contacts in complete devices resulted in disappointing voltages and currents.

Efforts were made to deal with the poor performance of the cells. Devices were made on different types of TCO coated glass substrates but, were resulting in the same numbers which shows the type of TCO has an insignificant effect on the performance. The Cu doping has been helping in raising the V_{oc}s but at the same time marred the currents whose effect has been unexplainable. Further experiments have been made changing the ZnTe thickness and concentration of Cu doping.

Experiments were done increasing the substrate temperature as high as 500^0C during ZnTe deposition and a Se flux has been introduced so as to compensate the loss of Se from CdSe at such high substrate temperature. But these experiments resulted in dismal performance indicating the domination of defects in the undoped ZnTe layer.

CHAPTER I

INTRODUCTION

1.1 Need for Solar Energy

Solar energy from the sun is free and inexhaustible. This enormous, reliable and clean energy resource represents a viable alternative to the fossil fuels that are currently polluting our air and water, threatening public health, and contributing to global warming. The amount of energy that falls on the Earth's surface from the sun is so enormous that all the energy stored in Earth's reserves of oil, coal, and natural gas is matched from just 20 days of sunshine. The sun's energy contains about 1,300 watts per square meter outside the Earth's atmosphere. About one-third of this light is reflected back into space, and some is absorbed by the atmosphere itself [1].

Over the next 50 years mankind has to face two big challenges of meeting the global energy demand and limiting the effects of global warming. The demand for energy is growing as the economies around the world are developing rapidly with constantly growing population. With supplies of fossil fuels diminishing daily, solar energy can be one solution to this problem. It is estimated that by 2100, solar energy will account for 80% of the total energy produced around the world [1]. Global warming is a danger unlike anything we have faced ever before. Turning to alternative energy sources, like solar, is one way to help.

1.2 History of Solar Cells

The photovoltaic effect was first reported by Edmund Bequerel in 1839. His observations of producing an electric current by the action of light on a silver coated platinum electrode immersed in electrolyte have given way to this discovery. In 1876 William Adams and Richard Day discovered that photocurrent could be produced in a sample of selenium when contacted by two heated platinum contacts [2]. The photovoltaic action of the selenium was found to be different from its photoconductive action in which current was produced spontaneously by the action of light. No external power supply was needed and a rectifying junction had been formed between the semiconductor and the metal contact. In 1894, Charles Fritts prepared what was probably the first large area solar cell by placing a layer of selenium between gold and another metal. Photovoltaic effects were observed in copper-copper oxide thin film structures, in lead sulphide and thallium sulphide in the following years. These early cells were thin film Schottky barrier devices, as a semitransparent layer of metal deposited on top of the semiconductor provided both the asymmetric electronic junction, which is necessary for photovoltaic action and access to the junction for the incident light. The photovoltaic effect of these related to the existence of a barrier to current flow at one of the semiconductor-metal interface (i.e., rectifying action) by Goldman and Brodsky in 1914. Later, during the 1930s, Walter Schottky, Neville Mott and others developed the theory of metal-semiconductor barrier layers.

However, researchers were not excited by the photovoltaic properties of materials like selenium, but the photoconductivity. The observations that the current produced from the materials was proportional to the intensity of the light and their relation to the wavelength meant that photoconductive materials were ideal for photographic light meters. The photovoltaic effect in barrier structures was an additional benefit because the light meter could operate without a power supply. During 1950s, the development of good quality silicon wafers for applications in the new solid state electronics produced potentially useful quantities of power by photovoltaic devices in crystalline silicon.

This followed the discovery of a way to manufacture p-n junctions in silicon. Better rectifying action and better photovoltaic effect was produced when developing p-type skin by exposing naturally n-type silicon wafers to the gas boron trichloride and later etching away part of the skin to give access to the n type layer beneath. Chapin, Fuller and Pearson in 1954 reported the first silicon solar cell with a conversion efficiency of 6%, six times higher than the best pervious attempt. An estimated production cost of some $200 per Watt hindered the consideration of these cells for power generation for several decades. However, these solar cells introduced the possibility of power generation in remote locations where fuel could not be easily delivered. Silicon solar cells were then widely developed for space applications when requirement of reliability and light weight made the cost of the cells unimportant.

In 1954, an efficiency of 6% was produced with cadmium sulphide p-n junction and in the following years higher efficiencies were indicated by simulation studies of p-n

junction photovoltaic characteristics in gallium arsenide, indium phosphide and cadmium telluride [2]. Silicon still remained and remains the foremost photovoltaic material because of its benefiting advances for the microelectronic industry.

The crisis in energy supply experienced by the oil-dependent western world in the 1970s led to an abrupt growth of interest in alternative sources of energy, and funding for research and development in those areas have also grown. Photovoltaics was of high interest during this period, and many strategies for producing photovoltaic devices and materials more cheaply and with more efficiency were explored. Means to lower cost included photoelectrochemical junctions and materials such as polycrystalline silicon, amorphous silicon, other 'thin film' materials and organic conductors whereas strategies for higher efficiency included tandem and other multiple band gap designs. But none of these efforts helped to achieve widespread commercial development

Again during the 1990s, interest in photovoltaics expanded with growing awareness of the need to secure sources of electricity alternative to fossil fuels. During this period, the economics of photovoltaics improved primarily through economies of sale. In the late 1990s there was an expansion in the photovoltaic production at a rate of 15-25% per annum, driving a reduction in cost.

1.3 Economics of Photovoltaics

Predicting economic futures is challenging. One thing we can guarantee is that as we produce more solar cells, the price will go down as shown in the figure 1.1. With PV module price in $/Wp on the left hand side shipments in MWp/year on the right hand side we can see that just like the computer industry when you produce more (red line), the price will drop substantially (blue line). It should be open to the US market for PV to directly compete with fossil fuel electricity if we break the $2/Wp mark. This was supposed to happen in 2006, but unfortunately, the price hasn't dropped as much. The reason being that majority of solar cells are made from silicon. Silicon that is not pure enough or defect-free enough for the semiconductor industry is good for making solar cells. Most solar cells are made from the cast of silicon from the semiconductor industry. This supply is now completely used up which created a shortage of silicon to make solar. Once this is corrected, the prices of solar cells will likely drop back down to the curve on the graph. The entire production of solar cells is just a GW, just like one power plant. The prices are around $3.56/Wp as they climbed from $3.12/Wp.

However, as the PV production is increasing rapidly and prices will drop. In order to know their course in the U.S., the Industry developed a Roadmap. This graph is an industry prediction in gigaWatts per Year. By 2020 the U.S. is expected to produce over 30GW and the world is up over 80GW.

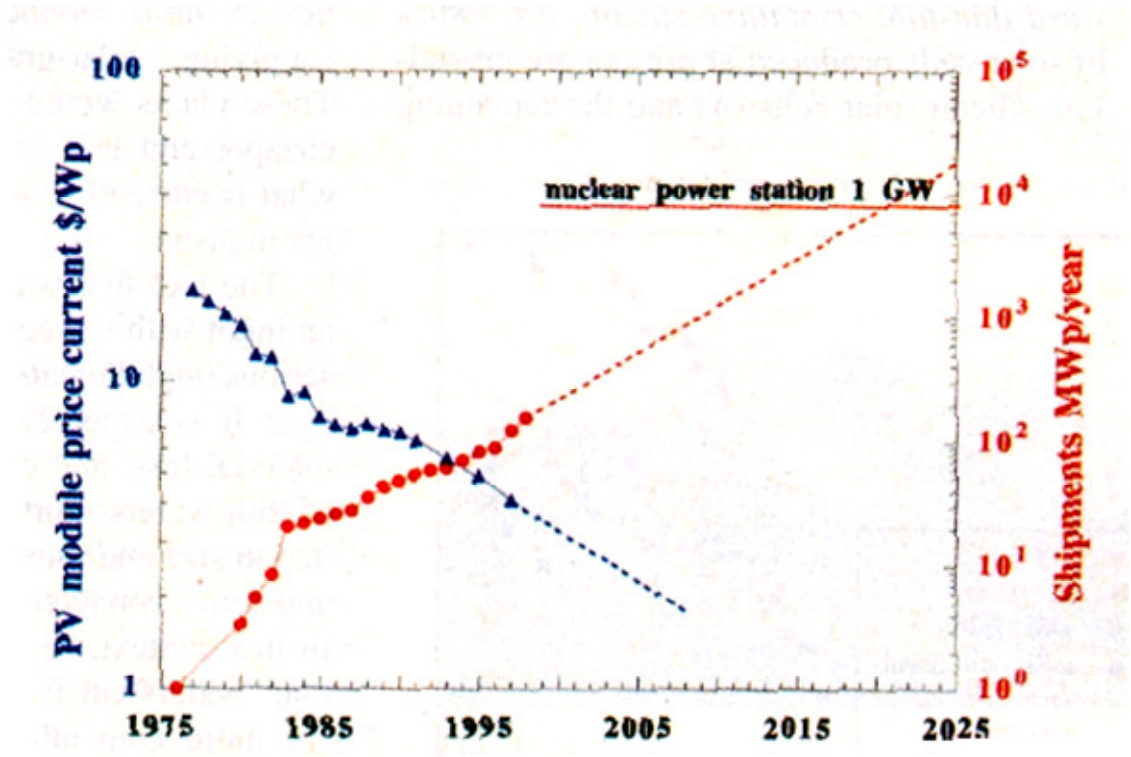


Figure 1.1 Economy of Scale. [3]

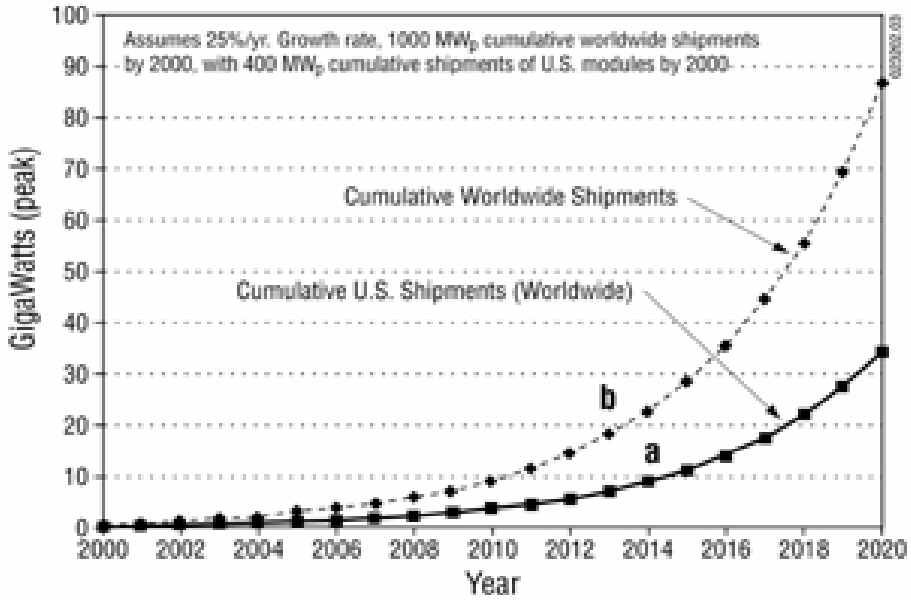


Figure 1.2 PV Roadmap Developed by the Industry. [4]

The world PV production is outpacing predictions. The world PV installations in 2004 rose to 0.93 GigaWatts (GW = 109W), representing growth of 62% over 2003 installations and the consolidated world production of PV increased to 1.15 GW. This growth rate, while impressive, must be kept in context of the global energy market. In 2000 the peak electrical generation capacity in the U.S. was 825 GW while the cumulative total global installed solar PV was less than a single GW [5].

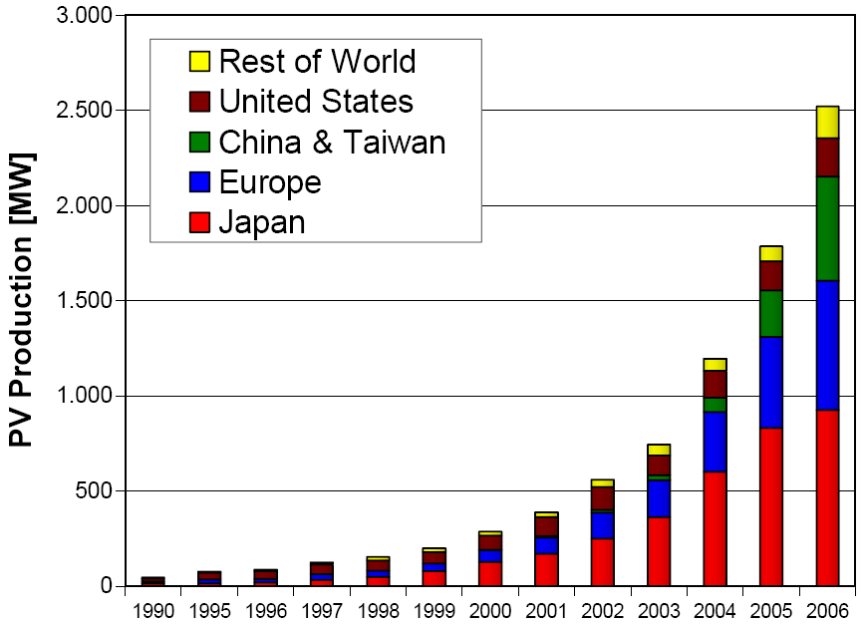


Figure 1.3 World PV Module Production. [6]

The global solar power market, as measured by annual solar power system installed capacity, grew at a CAGR of 47.4% from 598 MW in 2003 to 2,826 MW in 2007 [1]. According to a Solarbuzz forecast named "Green World," in one of several possible scenarios, annual solar power system installed capacity may increase to 9,917 MW in 2012, and solar power industry revenue may increase from $17.2 billion in 2007 to $39.5 billion in 2012, which we believe will be driven largely by surging market

demand, rising grid prices and government initiatives. The scope of the government incentives for solar power depends, to a large extent, on political and policy developments relating to environmental concerns in a given country, which could lead to a significant reduction in or a discontinuation of the support for renewable energies in such country. Federal, state and local governmental bodies in many of our key markets, most notably Germany, Italy, Spain, the United States, France and South Korea have provided subsidies and economic incentives in the form of rebates, tax credits and other incentives to end users, distributors, system integrators and manufacturers of solar power products to promote the use of solar energy in on-grid applications and to reduce dependency on other forms of energy. These government economic incentives could be reduced or eliminated altogether. In particular, political changes in a particular country could result in significant reductions or eliminations of subsidies or economic incentives. Electric utility companies that have significant political lobbying powers may also seek changes in the relevant legislation in their markets that may adversely affect the development and commercial acceptance of solar energy. While the challenges are enormous, so are the opportunities.

1.4 Benefits of Solar Energy

Solar power has several advantages over both forms of energy, conventional and renewable energy.

The energy coming from the sun is practically free and after the initial investment has been recovered solar energy reduces the dependence on conventional source of

energy. Solar energy supports local jobs and creates wealth, which elevates local economies.

Solar energy is clean, quiet as it has no moving parts, renewable and sustainable unlike other conventional energy sources such as gas, oil, and coal. It does not contribute to global warming, acid rain, or smog, on the contrary, it helps in lowering harmful green house gas emissions.

Solar energy reduces our dependence on foreign or centralized sources of energy. It can reduce electric bills and can also supply homes with electricity when there is a power outage. The solar energy systems can installed in a remote location as they can be operated entirely independent from a power or gas grid

Solar energy systems are virtually maintenance free and will last at least 25 years [1]. System sizes can be increased in the future as your electricity needs grow.

1.5 Thin Film Photovoltaics

Majority of commercial solar cells in use today are made of silicon, the same semiconductor material that is used in the microelectronics industry. Typical commercial solar cells have an efficiency ranging between 6% and 18%, meaning that for every 1,000 watts of sunlight striking a solar module, 60 to 180 watts of electricity will be produced [7]. Although silicon is abundant in the earth's surface, processing it to pure crystalline form is expensive, resulting in recent supply shortages and high costs. Uncertain raw

material costs for photovoltaic grade silicon continue to show a demand that far out paces the supply in near future.

Solar cells and modules made from certain thin film semiconductors have been shown to be much less expensive to produce in a larger volume and requiring much less raw material to produce when compared to silicon based PV cells. Recent advances in thin-film PV are beginning to gain interest in commercial and residential building markets, as well as interest in space and near-space applications. Extensive research and development on thin film cells has been conducted for more than 30 years, and recent advances in manufacturing and product commercialization have increased worldwide share of thin film photovoltaics to over 10% in 2007 [7].

The three most common thin-film technologies are amorphous silicon (a-Si), cadmium telluride (CdTe) and copper-indium-gallium-diselenide (CIGS). Of these three, CIGS currently has demonstrated the highest laboratory efficiency at 19.5% (NREL, measured in earth conditions) with CdTe close behind it [8]. CIGS thin-film technologies can be placed on a wide variety of substrate materials making it possible to manufacture very lightweight, flexible solar cells on metals and also plastics. To make it more understandable, the thickness of a flexible CIGS device is approximately the same as the thickness of a human hair, making it very flexible and lightweight.

Thin film solar cells and modules require a structural "substrate" to support them, such as glass which is low in cost and enables continuous and scaleable manufacturing. The expenditure required to establish large-volume thin film PV product manufacturing plants enables rapid capacity expansion and lowers the cost per watt of products as much of the equipment to process these substrates is used in other industries.

The substrate and raw materials used in thin film PV products are less expensive than the cost of most semiconductor materials. Product cost can be reduced with increasing thin film manufacturing capacity and process yield improvements.

Thin film photovoltaic technologies also exhibit performance advantages in generating energy in low light level and increased temperature environments and as a result position them particularly well for applications in regions with less direct sunlight, such as in Northern Europe.

CHAPTER II

PHOTOVOLTAIC DEVICE PHYSICS

2.1 Introduction

As the name itself suggests the word 'Photovoltaics' has two parts. Photo is derived from the Greek word for light and volt relating to electricity pioneer Alessandro Volta. So, Photovoltaic's could literally be translated as Light-electricity, which means they convert light energy into electrical energy (Photoelectric Effect) as discovered by a French physicist Edmond Becquerel in 1839. This device is commonly called as Solar cell, which can be defined as a simple p-n junction diode that generates the charge carriers up on light incidence. Before Getting into details of the behavior of the solar cells, it is very essential to understand the fundamentals of the materials, which the solar cell consists of.

All the elements can be categorized into three types, a conductor, an insulator, and a semiconductor and the key property that determines whether a material is an insulator, a conductor, or a semiconductor is the location of the Fermi energy relative to the valence and conduction bands, and the size of the energy gap between these two bands. In the case of insulators there is a large energy gap between the valence and conduction bands and the Fermi energy lies between the two bands. This means that the valence band is completely full and the conduction band is completely empty. If we apply a modest

voltage across the solid, electrons will try to respond to it by picking up energy from the electric field and moving along the field lines towards the positive end. It requires a lot of energy, 5-8 eV, to excite the electrons enough to get to the conduction band. So, it requires much energy to traverse the band gap, since the width of the band gap is very large. A metal is an excellent conductor because, at room temperature, it has electrons in its conduction band constantly, with little or no energy being applied to it. This may be because of its narrow or nonexistent band gap and the conduction band may be overlapping the valence band so they share the electrons. The band diagram would be drawn with E_c and E_v very close together, if not overlapping.

Now, the semiconductors are generally certain elements that allow, but still resist the flow of electricity. These semiconductors lie somewhere between good conductors and poor conductors. Semiconductors are very important because, semiconductors have a unique atomic structure that allows their conductivity to be controlled by stimulation with electric currents, electromagnetic fields, or even light. The band gap is wide enough to where current is not going through it at all times, but narrow enough to where it does not take a lot of energy to have electrons in the conduction band creating a current. They have fully occupied valence band, at T=0, but the forbidden energy gap is not very large, due to this they do not conduct in normal conditions but these electrons are loosely bound and so any excitation causes them to break the bond resulting in conduction. This makes it possible to construct devices from semiconductors that can amplify, switch, convert sunlight to electricity or produce light from electricity.

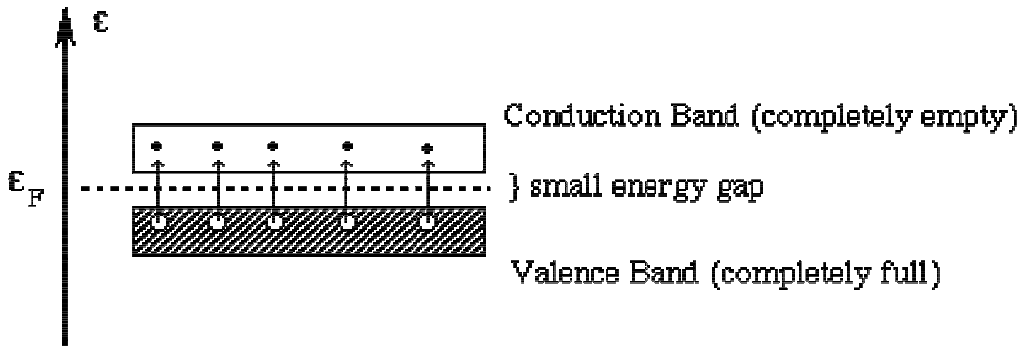


Figure 2.1 Energy Band Diagram for Electrons in a Semiconductor.

Semiconductors can be classified as intrinsic and extrinsic semiconductors. An intrinsic semiconductor is one, which is pure enough that impurities do not affect its electrical behavior. Here, all carriers are created due to thermally or optically excited electrons from the full valence band into the empty conduction band. Electrons and holes flow in opposite direction in an electric field, though they contribute to the same direction since they are oppositely charged. An extrinsic semiconductor is the one that has been doped with impurities to modify the number and type of free charge carriers. When a semiconductor is doped with a donor impurity it has an extra electron, which makes it an n-type semiconductor. Similarly when an acceptor impurity is incorporated; it gives rise to an extra hole, which makes it a p-type semiconductor.

The energy levels for an atom are discrete but they are so closely spaced that they form continuous energy bands. In any semiconductor there is a forbidden energy region in which allowed states cannot exist. The energy band above this energy gap is called the conduction band and the one below is called the valence band. And the forbidden energy

region is called the Energy Bandgap (Eg) which is one of the most important parameters in semiconductors.

The Fermi level is defined as the energy level below which all states will have at most two electrons of opposite spin according to Pauli's exclusion principle [9]. It can be also defined as the energy level where the probability of finding an electron is ½. The Fermi distribution function is given by

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}} \tag{2.1}$$

where k is the boltzman's constant, T is the absolute temperature, EF is the Fermi energy. For an intrinsic semiconductor the Fermi level lies approximately in the middle of the bandgap. This Fermi level shifts towards the conduction band for n-type and towards the valence band for p-type semiconductors. The Fermi levels can be calculated using the equations given below [10].

$$\text{For n-type} \quad E_F - E_C = kT \ln(N_D / N_C) \tag{2.2}$$

$$\text{For p-type} \quad E_V - E_F = kT \ln(N_A / N_V) \tag{2.3}$$

where k is the boltzman's constant, T is the absolute temperature, E_F is the Fermi energy, E_C is the energy level at the bottom of the conduction band, E_V is the topmost energy level of the valence band, N_C and N_V is the effective density of state in the conduction band and valence band respectively, N_D and N_A is the donor and acceptor concentration respectively [11].

2.2 Photovoltaic Effect

The "photovoltaic effect" is the basic physical process through which a solar cell converts light from the sun into electricity. Sunlight is composed of photons, or "packets" of energy that contain different amounts of energy corresponding to the different wavelengths of light. When photons are incident on a solar cell, they may get reflected or absorbed, or they may pass right through. When absorbed, the energy of the photon is transferred to an electron in an atom of the cell. With its newfound energy, the electron is able to escape from its normal position associated with that atom to become part of the current in an electrical circuit. By leaving this position, the electron causes a hole to form. Special electrical properties of the solar cell like built-in electric field provide the voltage needed to drive the current through an external load such as a light bulb [12].

2.3 P-N Junction

When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called a p-n junction. Most semiconductor devices contain one or more p-n junctions. The p-n junction is of great importance because it is the control element for the semiconductor devices.

P-n junction diodes form the basis of not only solar cells, but of many other electronic devices such as LEDs, lasers, photodiodes and bipolar junction transistors (BJTs). A p-n junction aggregates the effects of recombination, generation, diffusion and drift into a single device.

A simple p-n junction consists of two semiconductor regions with opposite doping type as shown in Figure 2.2. The region on the left is *p*-type with an acceptor density N_a, and the region on the right is *n*-type with a donor density N_d. The dopants are assumed to be shallow, so that the electron (hole) density in the *n*-type (*p*-type) region is approximately equal to the donor (acceptor) density.

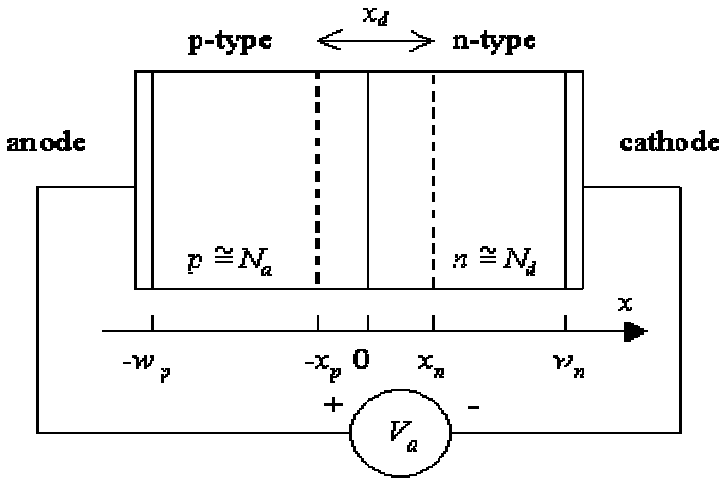


Figure 2.2 Cross Section of a P-N Junction. [13]

In an abrupt p-n junction device both the regions are uniformly doped and the transition between the two regions is abrupt. In p-n junctions where one side is distinctly higher-doped than the other will, it is found that only the low-doped region needs to be considered, since it primarily determines the device characteristics and this structure is referred to as a one-sided abrupt p-n junction.

The junction is biased with a voltage Va as shown in Figure 2.2. We call it a forward bias if a positive voltage is applied to the p-doped region and if a negative

voltage is applied to the p-doped region we call it reversed-biased. The contact to the p-type region is also called the anode, while the contact to the n-type region is called the cathode, in reference to the anions or positive carriers and cations or negative carriers in each of these regions.

The principle of operation will be explained using a *gedanken* experiment, an experiment, which is in theory possible but not necessarily executable in practice [14]. We imagine that one can bring both semiconductor regions together, aligning both the conduction and valence band energies of each region. This yields the so-called flatband diagram shown in Figure 2.3.

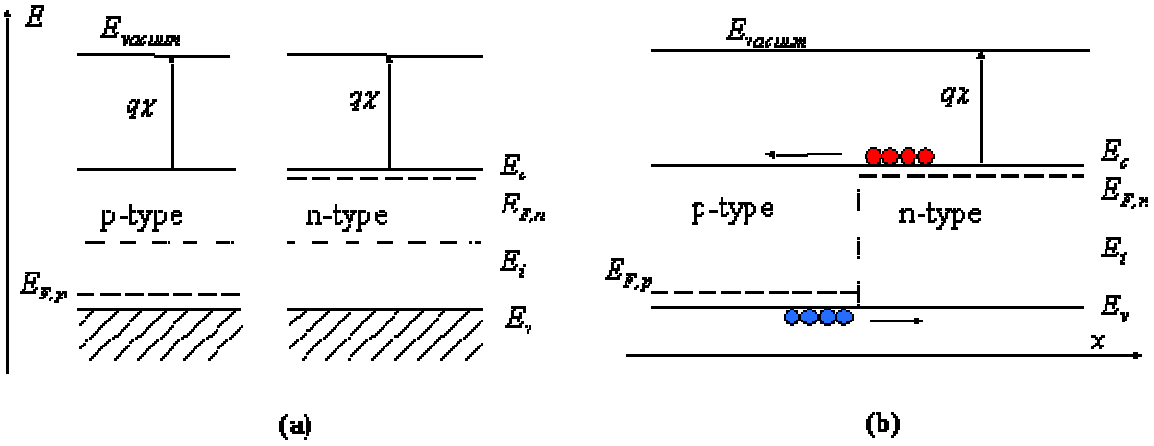


Figure 2.3 Energy Band Diagram of P-N Junction Before and After Merging the N-Type and P-Type Regions.

This does not automatically align the Fermi energies, $E_{F,n}$ and $E_{F,p}$. Also, this flatband diagram is not in equilibrium since both electrons and holes can lower their energy by crossing the junction. A motion of electrons and holes is therefore expected

before thermal equilibrium is obtained. The diagram shown in Figure 2.3 (b) is called a flatband diagram. It is named as flat band as it refers to the horizontal band edges. It also implies that there is no field and no net charge in the semiconductor.

In order to reach thermal equilibrium, electrons/holes close to the metallurgical junction diffuse across the junction into the *p*-type/*n*-type region where hardly any electrons/holes are present. This process leaves the ionized donors (acceptors) behind, creating a region around the junction, which is depleted of mobile carriers. We call this region the depletion region, extending from $x = -x_p$ to $x = x_n$. The charge due to the ionized donors and acceptors causes an electric field, which in turn causes a drift of carriers in the opposite direction. The diffusion of carriers continues until the drift current balances the diffusion current, thereby reaching thermal equilibrium as indicated by a constant Fermi energy. This situation is shown in Figure 2.4:

While in thermal equilibrium no external voltage is applied between the *n*-type and *p*-type material, there is an internal potential, ϕ_i, which is caused by the work function difference between the *n*-type and *p*-type semiconductors. This potential equals the *built-in* potential, which will be further discussed in the next section.

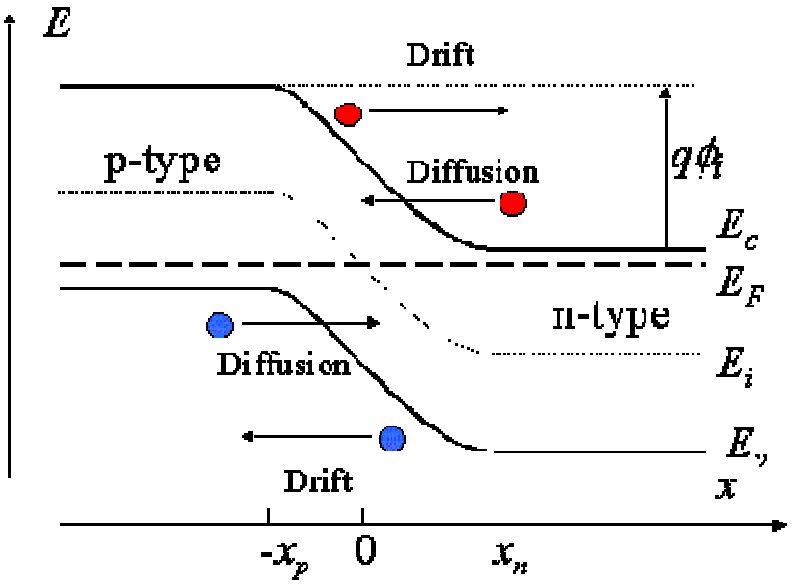


Figure 2.4 Energy Band Diagram of P-N Junction in Thermal Equilibrium. [15]

The built-in potential in a semiconductor equals the potential across the depletion region in thermal equilibrium. Since thermal equilibrium implies that the Fermi energy is constant throughout the p-n diode, the built-in potential equals the difference between the Fermi energies, E_{Fn} and E_{Fp}, divided by the electronic charge. It also equals the sum of the bulk potentials of each region, ϕ_n and ϕ_p, since the bulk potential quantifies the distance between the Fermi energy and the intrinsic energy. This yields the following expression for the built-in potential.

$$\phi_i = V_t \ln \frac{N_d N_a}{n_i^2} \tag{2.4}$$

We now consider a p-n diode with an applied bias voltage, V_a. A forward bias corresponds to applying a positive voltage to the anode (the p-type region) relative to the cathode (the n-type region). A reverse bias corresponds to a negative voltage applied to the cathode. Both bias modes are illustrated with Figure 2.5. The applied voltage is

proportional to the difference between the Fermi energy in the n-type and p-type quasi-neutral regions.

As a negative voltage is applied, the potential across the semiconductor increases and so does the depletion layer width. As a positive voltage is applied, the potential across the semiconductor decreases and with it the depletion layer width. The total potential across the semiconductor equals the built-in potential minus the applied voltage, or:

$$\phi = \phi_i - V_a \tag{2.5}$$

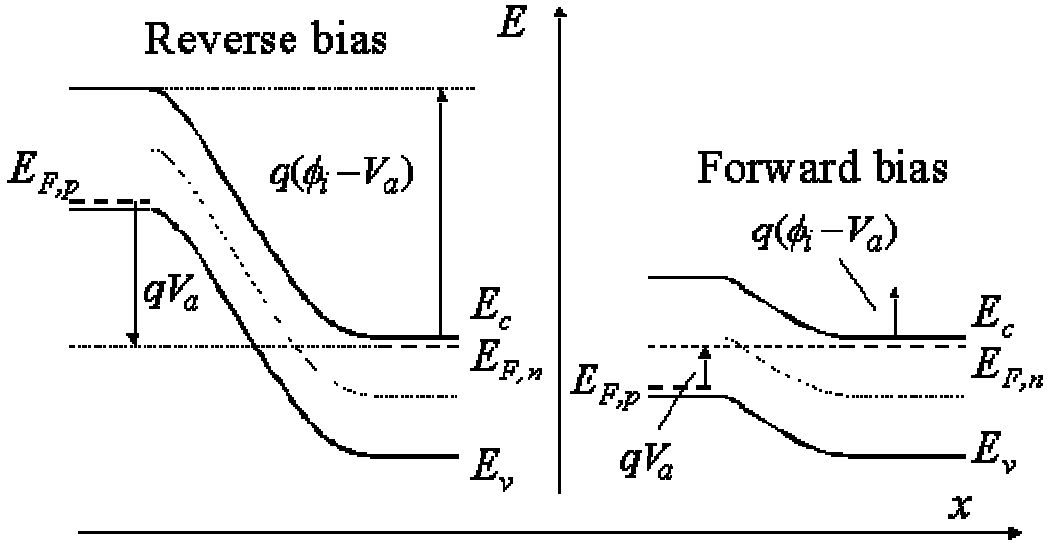


Figure 2.5 Energy Band Diagram of P-N Junction under Reverse and Forward Bias.[16]

2.4 P-N Heterojunction

Heterojunction p-n diodes can be found in a wide range of heterojunction devices including laser diodes, high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs). Such devices take advantage of the choice of different

materials, and the corresponding material properties, for each layer of the heterostructure. The heterojunction p-n diode is in principle very similar to a homojunction. The main problem that needs to be tackled is the effect of the bandgap discontinuities and the different material parameters, which make the actual calculations more complex even though the p-n diode concepts need almost no changing.

The flatband energy band diagram of a heterojunction p-n diode is shown in the figure below. As a convention we will assume ΔE_c to be positive if $E_{c,n} > E_{c,p}$ and ΔE_v to be positive if $E_{v,n} < E_{v,p}$.

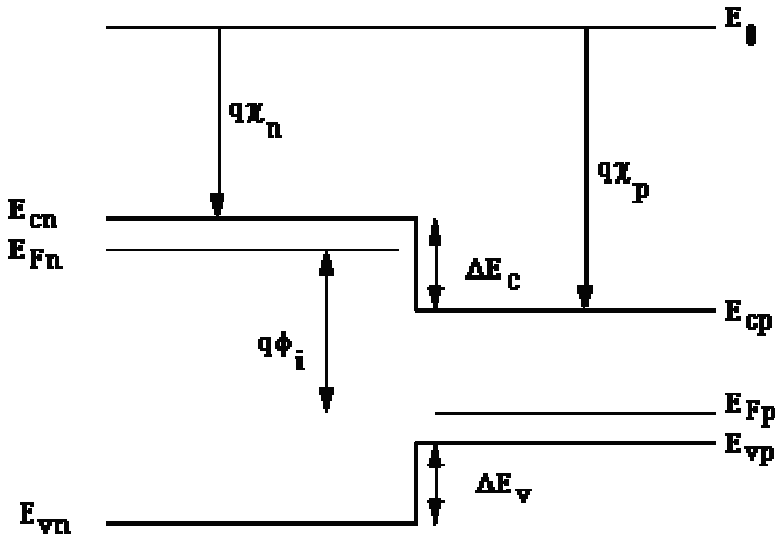


Figure 2.6 Flatband Energy Diagram of P-N Heterojunction. [17]

The built-in potential is defined as the difference between the Fermi levels in both the *n*-type and the *p*-type semiconductor. From the energy diagram we find:

$$q\phi_i = E_{F,n} - E_{F,p} \tag{2.6}$$

which can be expressed as a function of the electron concentrations and the effective densities of states in the conduction band:

$$q\phi_i = \Delta E_c + kT \ln \frac{n_{n0} N_{c,p}}{n_{p0} N_{c,n}} \tag{2.7}$$

The built-in voltage can also be related to the hole concentrations and the effective density of states of the valence band:

$$q\phi_i = -\Delta E_v + kT \ln \frac{p_{p0} N_{v,n}}{p_{n0} N_{v,p}} \tag{2.8}$$

Combining both expressions yields the built-in voltage independent of the free carrier concentrations:

$$q\phi_i = \frac{\Delta E_c - \Delta E_v}{2} + kT \ln \frac{N_d N_a}{n_{i,n} n_{i,p}} + \frac{kT}{2} \ln \frac{N_{v,n} N_{c,p}}{N_{c,n} N_{v,p}} \tag{2.9}$$

where $n_{i,n}$ and $n_{i,p}$ are the intrinsic carrier concentrations of the *n*-type and *p*-type region, respectively. ΔE_c and ΔE_v are positive quantities if the bandgap of the *n*-type region is smaller than that of the *p*-type region and the sum of both equals the bandgap difference. The band alignment must also be as shown in Figure 2.6. The above expression reduces to that of the built-in junction of a homojunction if the material parameters in the *n*-type region equal those in the *p*-type region. If the effective densities of states are the same, the expression for the heterojunction reduces to:

$$q\phi_i = \frac{\Delta E_c - \Delta E_v}{2} + kT \ln \frac{N_d N_a}{n_{i,n} n_{i,p}} \tag{2.10}$$

2.5 Solar Cell Parameters

Solar cells can be modeled as a current source in parallel with a diode. The solar cells behave like a diode when there is no light present to generate any current. As the intensity of incident light increases, current is generated by the PV cell, as illustrated in Figure 2.7.

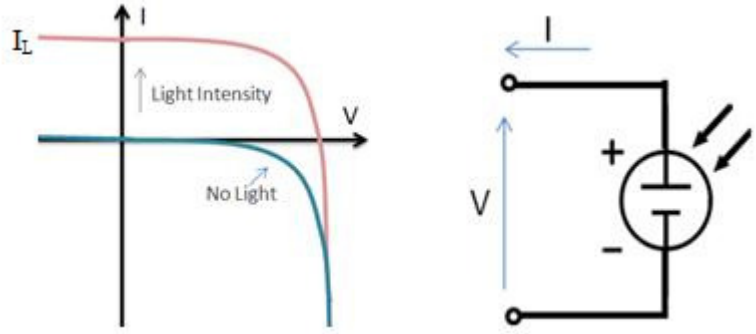


Figure 2.7 I-V Curve of a Solar Cell and its Electrical Circuit Diagram. [18]

In an ideal solar cell, the total current I is equal to the current I_ℓ generated by the photoelectric effect minus the diode current I_D, according to the equation:

$$I = I_l - I_D = I_l - I_0\left(e^{\frac{qV}{kT}} - 1\right) \tag{2.11}$$

where I_0 is the saturation current of the diode, q is the elementary charge $1.6\text{x}10^{-19}$ Coulombs, k is a constant of value $1.38\text{x}10^{-23}$J/K, T is the cell temperature in Kelvin, and V is the voltage produced by the cell.

I-V curve of an illuminated PV cell has the shape shown in Figure 2.8 as the voltage across the measuring load is swept from zero to V_{OC}, and many performance

parameters for the cell can be determined from this data, as described in the sections below.

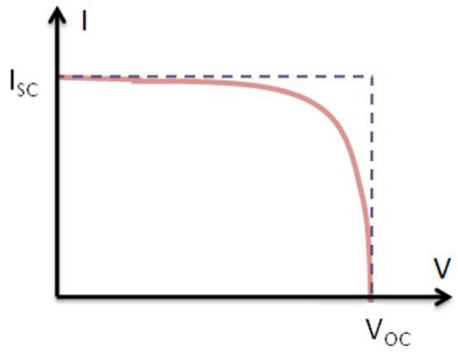


Figure 2.8 Illuminated I-V Sweep Curve.

I_{SC} represents to the maximum current that passes through the cell that corresponds to the short circuit condition when the impedance is low. It occurs at the beginning of the sweep when the voltage is zero. In an ideal cell, this maximum current value is the total current produced in the solar cell by photon excitation.

$I_{SC} = I_{MAX}$ at V=0

The open circuit voltage is the maximum voltage difference across the cell, and it occurs when there is no current passing through the cell.

$V_{OC} = V_{MAX}$ at I=0

The power produced by the cell in Watts can be easily calculated along the I-V sweep by the equation $P=IV$. At the I_{SC} and V_{OC} points, the power will be zero and the

maximum value for power will occur between the two. The voltage and current at this maximum power point are denoted as V_{MP} and I_{MP} respectively.

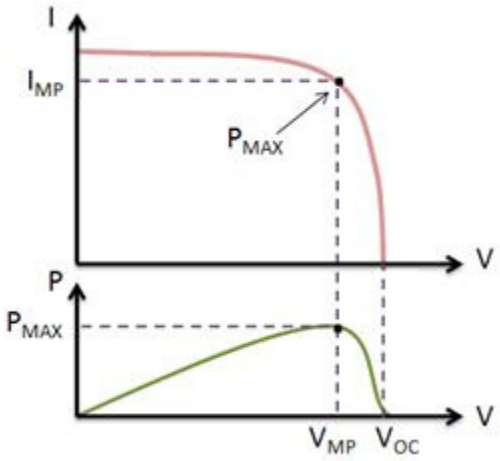


Figure 2.9 Maximum Power for an I-V Sweep.

The Fill Factor (FF) is essentially a measure of quality of the solar cell. It is calculated by comparing the maximum power to the theoretical power (P_T) that would be output at both the open circuit voltage and short circuit current together. Fill Factor can also be interpreted graphically as the ratio of the rectangular areas depicted in Figure 2.10.

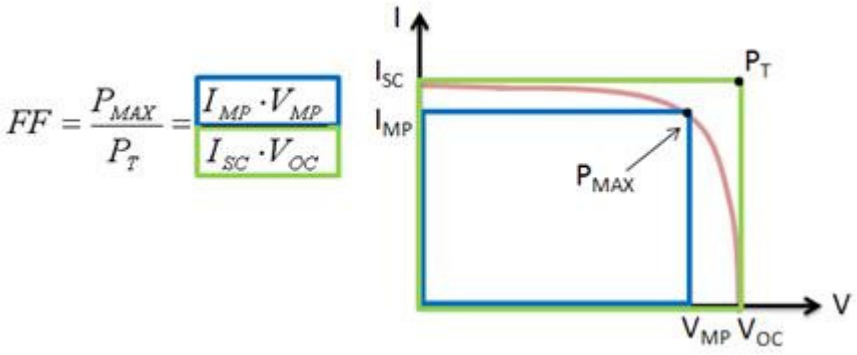


Figure 2.10 Fill Factor from the I-V Sweep.

A larger fill factor is desirable, and corresponds to an I-V sweep that is more square-like. Typical fill factors range from 0.5 to 0.82.

Efficiency is the ratio of the electrical power output P_{out}, compared to the solar power input, P_{in}, into the PV cell. P_{out} can be taken to be P_{MAX} since the solar cell can be operated up to its maximum power output to get the maximum efficiency.

$$\eta = \frac{P_{out}}{P_{in}} \Rightarrow \eta_{MAX} = \frac{P_{MAX}}{P_{in}} \tag{2.12}$$

P_{in} is taken as the product of the irradiance of the incident light, measured in W/m^2 or in suns (1000 W/m^2), with the surface area of the solar cell [m^2]. The maximum efficiency (η_{MAX}) found from a light test is not only an indication of the performance of the device under test, but, like all of the I-V parameters, can also be affected by ambient conditions such as temperature and the intensity and spectrum of the incident light. For this reason, it is recommended to test and compare PV cells using similar lighting and temperature conditions.

During operation, the efficiency of solar cells is reduced by the dissipation of power across internal resistances. These parasitic resistances can be modeled as a parallel shunt resistance (R_{SH}) and series resistance (R_S), as depicted in Figure 2.11.

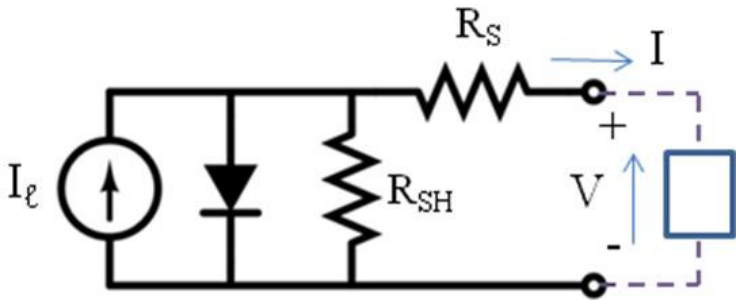


Figure 2.11 Simplified Equivalent Circuit Model for a Photovoltaic Cell.

For an ideal cell, R_{SH} would be infinite and would not provide an alternate path for current to flow, while R_S would be zero, resulting in no further voltage drop before the load.

Decreasing R_{SH} and increasing R_s will decrease the fill factor (FF) and P_{MAX} as shown in Figure 2.12. If R_{SH} is decreased too much, V_{OC} will drop, while increasing R_S excessively can cause I_{SC} to drop instead.

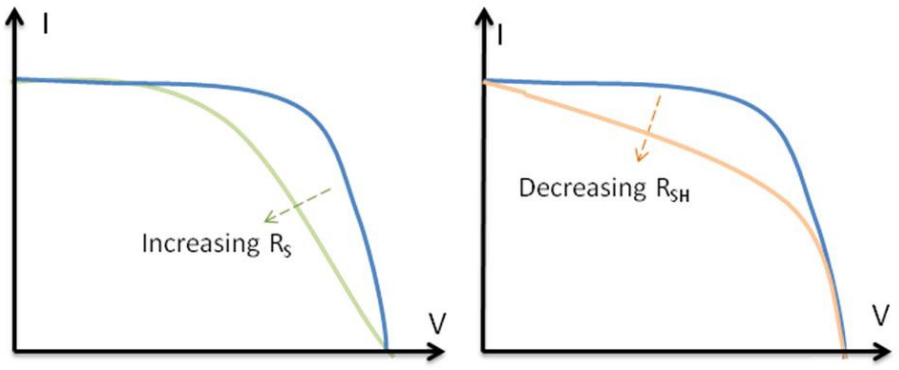


Figure 2.12 Effect of Series and Shunt Resistances.

The series and shunt resistances, R_S and R_{SH}, can be approximated from the I-V curve as shown in Figure 2.13.

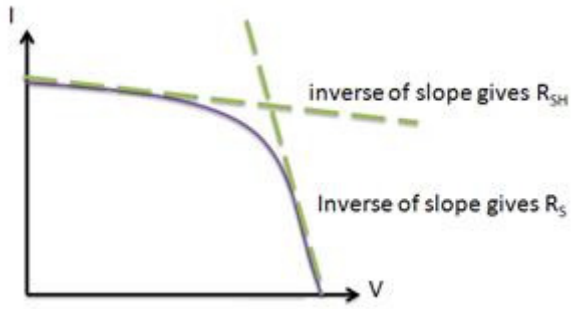


Figure 2.13 Shunt and Series Resistances from the I-V Curve.

If incident light is prevented from exciting the solar cell, the I-V curve shown in Figure 2.14 can be obtained. This I-V curve is simply a reflection of the "No Light" curve from Figure 1 about the V-axis. The slope of the linear region of the curve in the third quadrant (reverse-bias) is a continuation of the linear region in the first quadrant, which is the same linear region used to calculate R_{SH} in Figure 2.13. It follows that R_{SH} can be derived from the I-V plot obtained with or without providing light excitation, even when power is sourced to the cell.

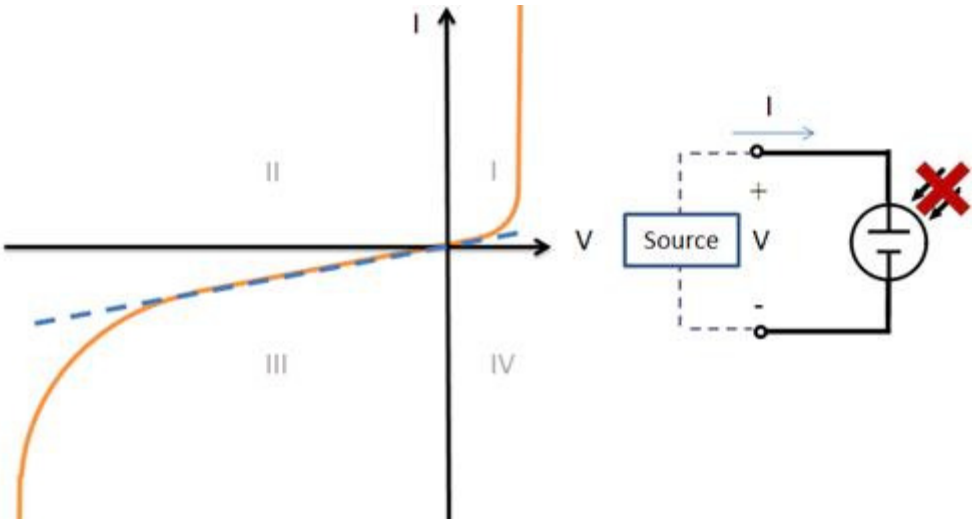


Figure 2.14 I-V Curve of Solar Cell without Light Excitation.

2.6 Tandem Solar Cells

These structures, also called a cascade or multijunction cells, can achieve a higher conversion efficiency by capturing a larger portion of the solar spectrum. In the typical tandem solar cell, individual cells with different bandgaps are stacked on top of one another in such a way that the sunlight falls first on the material having the highest bandgap. The top cell absorbs the high energy photons while remaining transparent to the low energy photons to allow them to fall on the cells below it where they are absorbed according to their appropriate bandgaps. These selective absorption processes continue through to the last cell, which has the smallest bandgap. The schematic of a typical tandem solar cell is shown in figure 2.15.

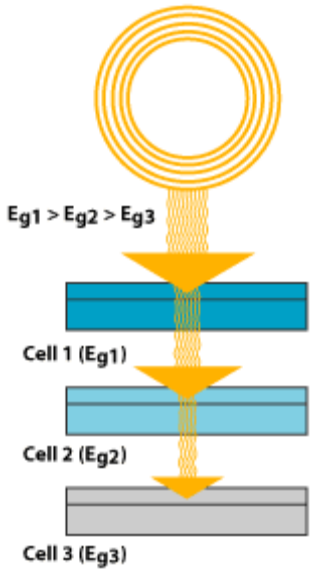


Figure 2.15 Schematic of Tandem Solar Cell. [19]

A tandem solar cell can be fabricated in two different ways. Two single junction solar cells are made independently in the mechanical stack approach, one with a high bandgap and one with a lower bandgap. Then the two cells are mechanically stacked, one on top of the other. In the monolithic approach, one complete solar cell is made first, and then the second cell is grown or deposited directly on the first cell.

Much of today's research in tandem solar cells focuses on gallium arsenide as one (or all) of the component cells. These cells have efficiencies of more than 35% under concentrated sunlight—which is very high for PV devices. The tandem solar cells in focus in our work are the CdSe – CIGS Solar Cells.

2.6.1 CdSe – CIGS Tandem Cells

For bandgaps of 1.7eV and 1.0eV for top cell and bottom cell respectively, efficiencies greater than 25% are achievable [20]. Simulations indicate that efficiencies of 25 – 30% can be achieved with CdSe/CIGS thin-film tandem devices [20]. The main objective to achieve this is to develop a transparent CdSe device of 16% conversion efficiency.

The tandem structure of a CdSe – CIGS Solar cell is shown in the figure 2.16.

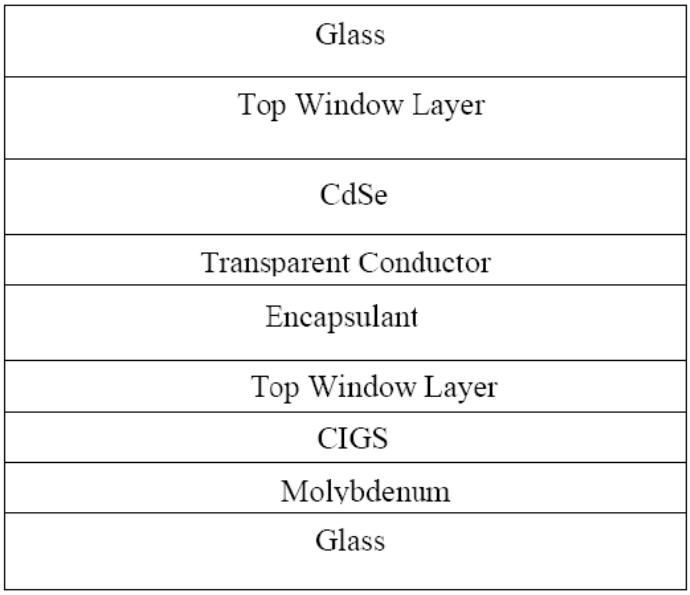


Figure 2.16 Structure of CdSe-CIGS Tandem Solar Cell.

2.6.2 CIGS Solar Cell

CIGS solar cells have been widely investigated as future generation thin film solar cells. Lab efficiencies of 19.9% [21] are reported while commercially manufactured CIGS solar cells have efficiencies ~ 10% [22]. CIGS (Copper Indium Gallium di Selenide) acts as a p-type absorber layer and has a very high absorption coefficient due to its direct bandgap. Cu vacancies are the reason for its p-type behavior. The n-type layer is

CdS. Molybdenum forms the p-type contact for CIGS and ZnO:Al forms the n-type contact for CdS. The devices fall under the classification of substrate configuration as light is incident through the top contact ZnO:Al. Soda lime glass is the most widely used substrate for CIGS Solar Cells. The low cost substrate contains an alkali and acts as a sodium source for CIS thin films which upon diffusion improves the grain growth and device performance. Addition of gallium not only increases bandgap but also improves the adhesion of the film to the Mo substrate. The schematic of the CIGS solar cell is as shown in the figure 2.17.

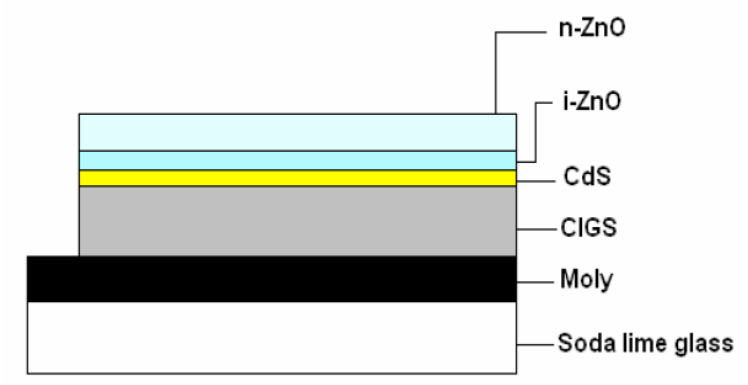


Figure 2.17 Structure of CIGS Solar Cell.

2.6.3 CdSe/ZnSe Solar Cell

The highest attained thin-film efficiencies for CdSe are around 6%, and were not transparent [20]. Extensive research has been done to make this structure transparent while restricting to the use of transparent contact. Transparent CdSe/ZnSe structures have been developed to demonstrate record Jsc's of 17.4 mA/cm^2 [21]. In this structure SnO_2 serves as the n contact and ZnSe:Cu as the p contact. These structures have also exhibited sub band gap transmission of 80% [23]. Inspite of a fairly favorable valance bad alignment, the Fermi level seems to be near the middle of the CdSe bandgap as the Voc's

achieved were only around 300mV with ZnSe:Cu. The structure of a typical device is shown in the figure 2.18.

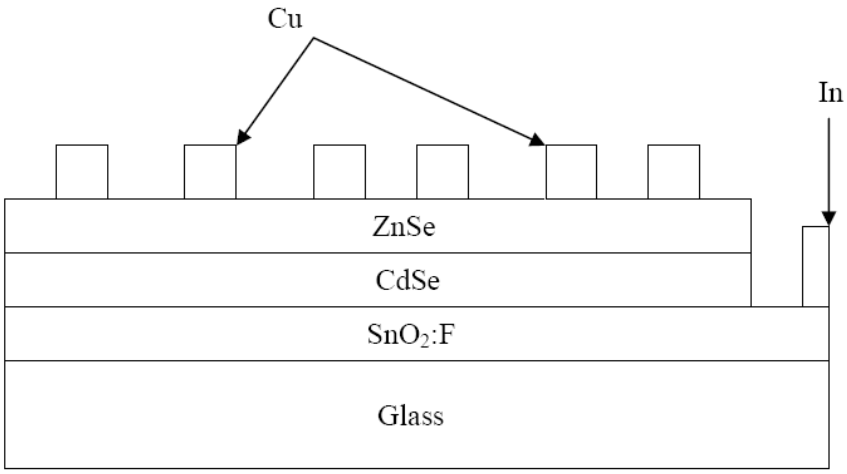


Figure 2.18 Structure of CdSe/ZnSe Solar Cell.

The current density of 17.4mA/cm^2 is the highest reported for a transparent thin-film CdSe device and it indicates the high electronic quality of the CdSe absorber layer. The device type that was targeted was metal/semiconductor/metal (MSM*)* in which the semiconductor is completely depleted, and thus Voc is determined by the contact energy of the two transparent p and n type contacts. Study has been done on the n-type contacts and SnO_2 was found to have superior performance over ZnO and CdS even though they contributed in a small increase in the Voc but the currents were low in comparision to the SnO_2[24]. Focus had been made on the p-type contacts which was a bigger challenge.

A reliable p-type contact should be transparent and should also have proper alignment of the valence band and Fermi level with the absorber layer. ZnSe and ZnTe were pursued as they were meeting of the criteria.

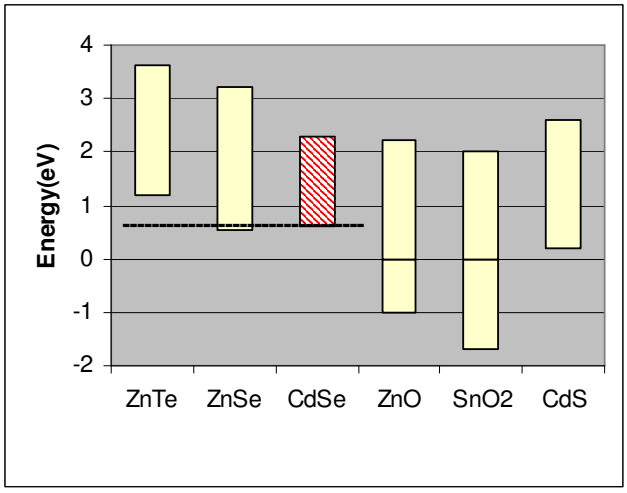


Figure 2.19 Band Alignments for CdSe and Transparent Contacts.

The valence band of ZnSe aligns well with that of CdSe with reference to the figure 2.19 and should be an ideal p contact. The dashed line in the figure is the demarcation line for p-type characteristics [24]. But from the earlier discussion, the low Voc's indicate the contact energies of ZnSe:Cu is not close to the valence band of CdSe assuming SnO_2 is close to the conduction band of CdSe. Thus a downward movement of the Fermi level is to be achieved to get the voltage as high as 1 Volt.

An approach has been made to solve this problem by doping the ZnSe layer with Nitrogen. Initial results showed successful incorporation of N but no trace of significant doping was observed [22]. An alternative approach of using ZnTe as the p-type layer was considered.

2.6.4 CdSe/ZnTe Solar Cell

As its higher valence band encourages p-type character, ZnTe is a good choice and previously reported achieved V_{oc} of 475mV [24] indicates lower contact energy than that of ZnSe. V_{oc} around 575 mV were achieved by a different deposition procedure with necessary increment of the thickness to $2000A^0$. An issue with the ZnTe layer is that the current densities were low in comparison to the ZnSe contacts. The currents were about $3mA/cm^2$. This was attributed to the thickness of the ZnTe and lower bandgap of 2.2eV compared to 2.6eV of ZnSe. Efforts were made to understand these devices. This thesis aims at doping the widow layer to improve device performance. Cu seemed to be an effective p-type dopant and is being investigated.

CHAPTER III

DEVICE FABRICATION AND MEASUREMENTS

3.1 Introduction

Fabrication details of CdSe Solar Cells will be discussed in this chapter.

3.2 Processing of CdSe Solar Cells

CdSe/ZnSe and CdSe/ZnTe form the top solar cell of the tandem stack. Temperatures during CdSe deposition process are very high. Corning 7059 glass is used as a substrate as it can withstand high processing temperatures above 700^0C. Fluorine doped tin oxide is used as an n-type ohmic contact to CdSe, while Cu is used as a front p-type contact to ZnSe and ZnTe. Processing details of the top cell are described below.

3.2.1 Substrate

Typical dimensions of the substrate are 1.25 X 1.35 X 0.05 inches.

3.2.2 Cleaning Procedure

The substrate goes through a regular cleaning procedure before depositing Fluorine doped SnO_2. This is a very important step as any contaminants present on the surface of the substrate could affect the succeeding deposition steps and the device performance as a whole. The substrate is first rinsed in DI water and scrubbed using a

brush to remove any particles present on the surface. To remove any further surface contamination due to particles absorbed chemically, the substrate is dipped in a 10% HF solution for 5 seconds and immediately rinsed with DI water. It is again dipped in the same solution for 2 seconds and after an immediate final rinse with DI water, the substrate is then blown dry with nitrogen.

3.2.3 Back Contact

The factors for being a good back contact are that it should be transparent, conductive and have appropriate contact energy. SnO_2: F, TEC glass and ITO are the three TCO's used as back contacts. Fluorine doped SnO_2 has a band gap of 3.5 eV and is a very good TCO because of its high transmission of 90 % and low sheet resistance of 7-10 ohms/sq.

Besides doped In_2O_3 and ZnO doped SnO_2 is the best known representative of the class of transparent conductors and finds use in form of poly-crystalline thin films. Metal-oxides often behave like semiconductors with a wide band gap due to their strong chemical bonds. To reduce its resistivity SnO_2 can be doped with fluorine (group VII). In this case F^{1-} substitutes O^{2-} and therefore acts as an electron donor resulting in a conduction mechanism of the n-type. The specific resistivity of polycrystalline doped SnO_2 can be as low as 10^{-3} Ωcm and is limited mainly by low mobility's in the order of 20 cm^2/Vs [25], smaller than in single crystals due to impurities, dislocations and grain boundary effects. The apparent band gap appears in total blue-shifted due to the degenerate doping level. Carrier concentrations in doped SnO_2 are lower than in In_2O_3:Sn

(ITO) by almost a factor of two, because the solubility of fluorine in SnO_2 is inferior to that of Sn in In_2O_3. This results in a lower infrared reflectivity and higher resistance of SnO2:F. Despite these drawbacks the lower costs make it an interesting alternative for applications, where large areas have to be coated. Furthermore it is chemically quite stable.

3.2.3.1 Fluorine Doped Tin Oxide

The Fluorine doped SnO_2 is deposited by the MOCVD process and is the n-type contact to CdSe. During MOCVD, a series of surface reactions occur. These reactions include adsorption and desorption of the precursor molecules, surface diffusion, nucleation and growth, and desorption of reaction products. The source for tin is TMT (Tetra Methyl Tin). The source for Fluorine is Halocarbon 13B1 (Difluoroethylene) and acts as the dopant and Helium as the carrier gas. To prevent the diffusion of Fluorine atoms, a bi-layer comprising undoped and doped tin oxide is deposited. During the deposition of undoped layer only Oxygen and TMT are reacted and 13B1 is added to them during the deposition of the doped layer. The Schematic of the CVD reactor is shown if Figure 3.1. The substrate temperature during the whole process is maintained at 440^0C using the RF coils encircling the reactor and are water cooled. Four samples can be accommodated at a time on the graphite sample holder and it is placed at an elevated angle of 5 degrees to improve uniformity of the deposited layer. For the first 8 minutes- TMT, Halocarbon 13B1 and oxygen are flown through the reactor to deposit the n-type Fluorine doped layer of SnO_2. The substrates are annealed in the presence of oxygen for

the next 5 minutes. For the last 5 minutes an undoped layer of SnO_2 is deposited. The thickness of the film is approximately half micron.

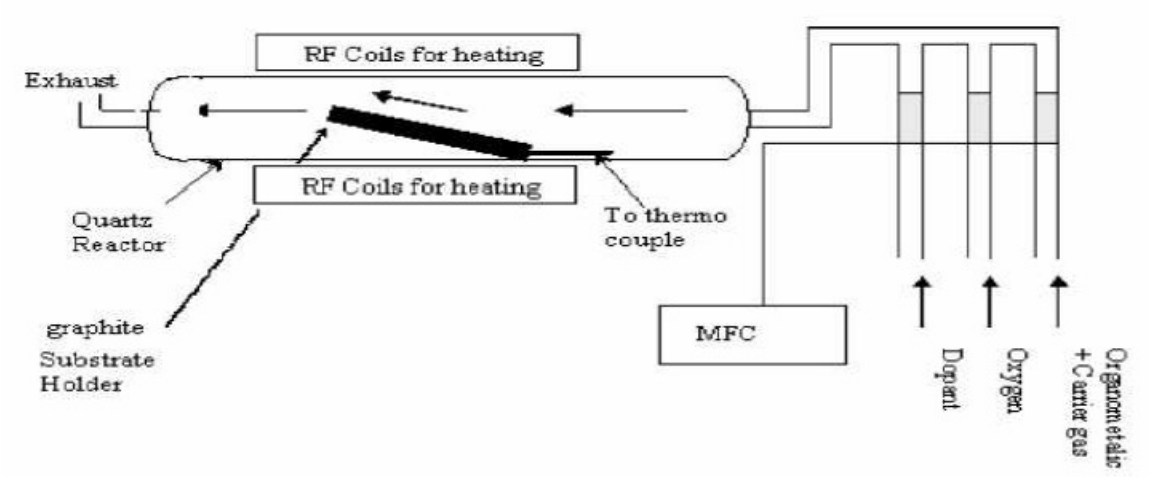


Figure 3.1 Schematic of MOCVD Reactor. [26]

The technique allows for relatively fast deposition that is controlled by adjusting the numerous deposition parameters such as precursor partial pressure, gas flow, substrate temperature, chamber temperature, reactor back pressure and so forth.

3.2.3.2 Tech Glass

SnO2:F is commercially available in a multilayer structure as Tech glass. Current applications include photovoltaics, electrochromics and displays. Optical design of these and other applications requires knowledge of the optical constants, in some cases, over the whole solar spectrum. This material is deposited in several steps and has a fairly complex structure.

The commercially available transparent conductive substrates Tech20 and Tech15 glass by Libbey Owens Ford are commonly referred to as tin-oxide glass, but in reality they are multilayer structures composed by different materials. On a soda-lime-silicate (glass) substrate a thin intrinsic SnO_2 layer is deposited. It is then followed by a thin SiO_2 film and finally a thick SnO_2:F layer. The numbers 20 and 15 refer to the nominal sheet resistance of 20 Ω/□ and 15 Ω/□ respectively [25], where the sheet resistance is defined as the ratio of specific resistivity and film thickness.

ema (SnO_2:F)/50% void	27 nm
SnO_2:F	226 nm
SiO_2	27 nm
SnO_2	24 nm
glass	3 mm

Figure 3.2 Structural Model for Tech 20 Glass. [25]

Undoped SnO_2 is a defect compound tending to form numerous oxygen vacancies resulting in carrier concentrations of 10^{17}-10^{19} cm^{-3}. Although the conductivity is much smaller than that of SnO_2:F, the free electron influence should nevertheless be observable. It must be pointed out that the SnO_2:F layer turns opaque above 1.5 μm due to its free carriers' influence.

Tech 20 is the glass we used in our work. The glass was cut into pieces nearly to the dimensions of Corning 7059 substrates. The substrates were rinsed with soap water

and then put in a beaker of methanol which is then kept in ultrasonic for about 1 hour to remove any chemically absorbed dust particles from the surface of the substrate and then dried out with blowing nitrogen.

3.2.4 Absorber Layer

Cadmium Selenide, which belongs to the II-VI group of the periodic table, is used as the absorber layer because of its fixed optical bandgap of 1.7 eV and a high chemical stability. Cd and Se have 2 and 6 electrons respectively in their outer most orbit. Every Cadmium atom transfers its 2 electrons to 6 valence electrons of Se to form CdSe and a vacancy of a Selenium atom frees two electrons of Cadmium making CdSe n-type. CdSe crystallizes in two forms, either wurtzite (Hexagonal) or cubic (Zinc blende) structures. CdSe deposited in this work has Hexagonal structure. CdSe films grown with larger grain size have better quality and also enhance the transport properties of minority charge carriers.

3.2.4.1 Preparation of CdSe Source

The CdSe source is prepared by using a high purity (99.999%) CdSe powder. Utmost care is taken so that the material is contaminant free as they may affect the device performance. By pressing CdSe powder in a circular mold a circular disk of 2 mm thick and 1 inch in diameter is prepared.

3.2.4.2 Deposition Procedure for CdSe

CdSe can be deposited by various methods like Thermal evaporation, Sputtering, Chemical vapor deposition, Electrodeposition, CBD and CSS. CSS is a simpler process

and can also produce films of good electronic properties. The deposition rate is high so that 1-2μm thick films can be deposited in a short time. The source is kept on a graphite holder and is separated by 4 mm from the substrate by quartz spacers. Each of the two quartz lamps is fixed to a reflector and are placed one over the other so that the heat is localized. A Schematic of the CSS tube is shown in Figure 3.3. The chamber is pumped down to less than 1 Torr through a mechanical pump and purged with Helium thrice. It is then pumped down to a base pressure of 0.92 Torr and backfilled with Helium to a pressure of 3.92 Torr. The source and the substrate are then heated to 670^0C and 560^0C respectively using temperature controllers. The deposition is carried out for 17 minutes after which both the lamps are turned off and a 2 micron thick CdSe film having wurzite structure is formed. Increasing the substrate temperature was found to reduce the sticking coefficient of the Cd and Se atoms, resulting in a thinner film. The sticking coefficient of Se is low at high temperatures, so the films are Cd rich, which causes them to be n-type. Films deposited by CSS were found to be free of pin holes and of a high electronic quality. The quality of the films mainly depends on the parameters like pressure, substrate and source temperatures and the spacing between them.

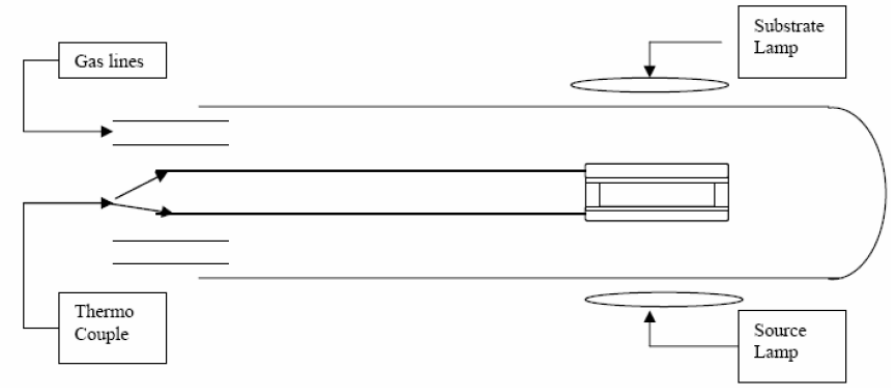


Figure 3.3 Schematic of CSS Chamber. [27]

3.2.5 Window Layer

To transmit maximum amount of light to the absorber layer, we need a window layer with a high bandgap. Zinc Selenide with a band gap of 2.7 eV can be used as a window layer. It is a II-VI semiconductor widely used in many opto-electronic applications. The crystal structure of ZnSe is shown in Fig 4.11. It crystallizes into a Zincblende structure.

3.2.5.1 Deposition Procedure for ZnSe

The source used is High purity (99.999%) ZnSe powder. ZnSe is thermally evaporated at room temperature and deposited on films deposited with CdSe. The evaporation chamber is pumped down below $3x10^{-6}$ Torr and the source is heated in radak furnace to get desired deposition rates.

A schematic diagram of the evaporation chamber is shown in Figure 3.4 [28]. The chamber has 4 radak furnaces with a capability to heat up 3 sources at the same time. The temperature of the sources and the substrate was controlled by temperature controllers.

3.2.5.2 Deposition Procedure for ZnTe

ZnTe is also deposited by thermal evaporation but in a different vacuum chamber from that of ZnSe. The chamber has three radak furnaces and all the three can be heated at the same time. The sources are loaded with ZnTe, Se and Copper. The chamber is pumped down to micro torr range and ZnTe is deposited onto the substrate deposited with

CdSe. The thickness is registered in the thickness monitor and the temperature controlled by temperature controllers.

3.2.5.3 Deposition Procedure for Cu Doped Window Layer

Copper doping of ZnTe is achieved by co-evaporating both Cu and ZnTe. Several experiments were done changing the thicknesses of the undoped and doped layers of ZnTe. Experiments were also done changing the concentration of copper during the deposition of the doped layer of ZnTe by varying the deposition rate.

3.2.6 Front Contact

Higher conductivity, transparency nad ability to form an ohmic contact with the window layer are the prome characteristics of the front contact. Copper is deposited as front contact by thermal evaporating Copper pellets (99.999% pure) in the chamber shown in Fig 3.5. The pellets are loaded onto tungsten boats and heated to desired temperatures. To keep the reflection losses minimum, the thickness was maintained at 30A. A mask of 0.1 cm^2 area dots was used for depositing copper on the ZnSe film. The chamber is initially pumped to the micro Torr range. The chamber used to evaporate is shown in figure 3.5. The source is heated using a variac following a specific voltage-time profile.

After Cu deposition, the samples were left to sit in air for about 12 hours before measuring the parameters. The 12 hour exposure to air showed significantly better response and could be attributed to Cu diffusion into ZnSe and doping it, resulting in higher V_{oc}'s.

3.3 Device Characterization

Fabricated solar cells were characterized using I-V and Spectral response measurements. Data from these measurements was used to improve device performance by changing process parameters.

Current-voltage (I-V) measurements were carried out using a Keithley 2410 sourcemeter. The sourcemeter was connected to a computer through an interface and measurement was performed using a Labview program. Voltage is swept from -0.2V to 0.7V in light and dark conditions. The software program calculates and generates precise values for V_{oc}, J_{sc}, and FF automatically.

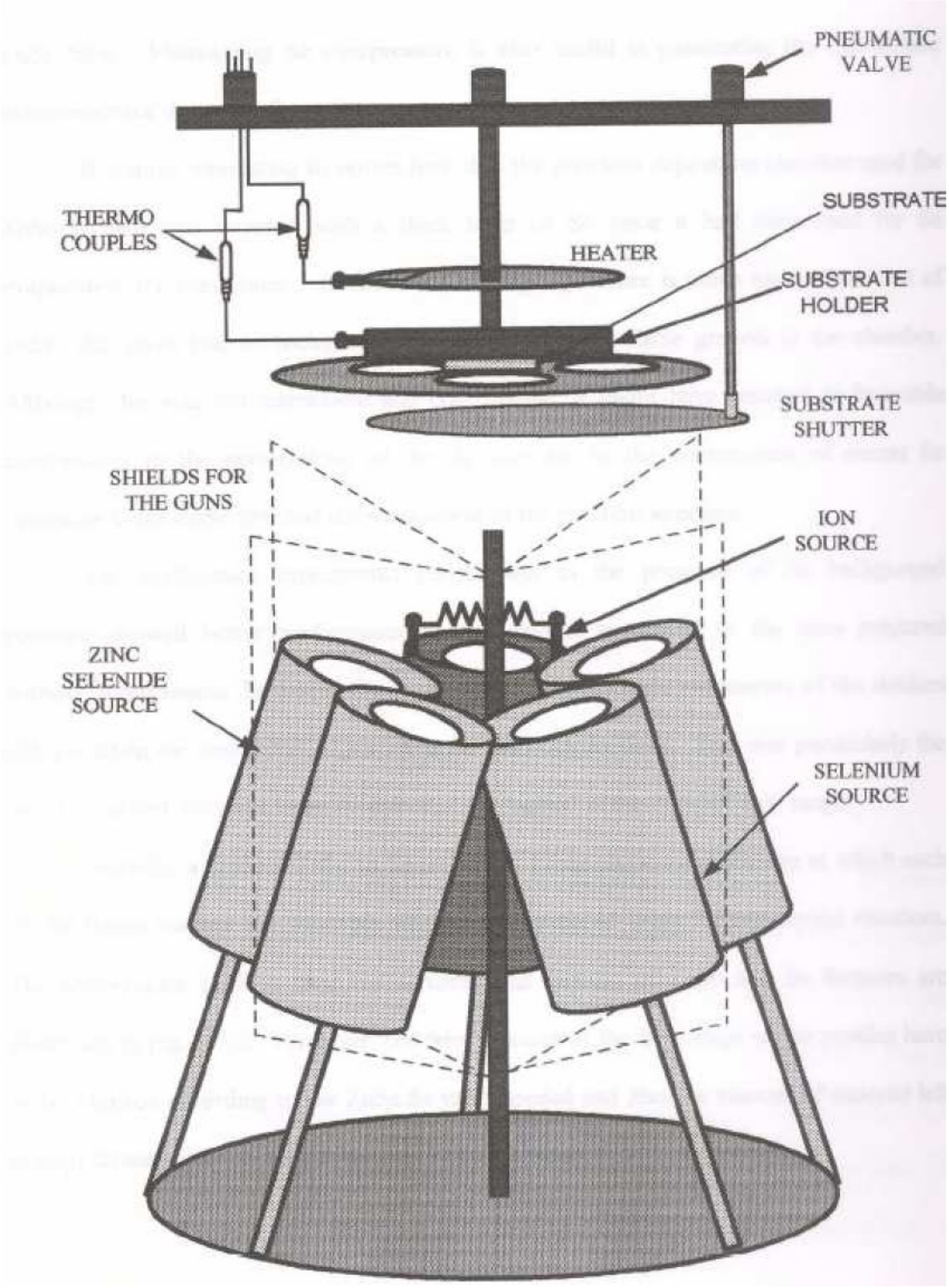


Figure 3.4 Schematic of ZnSe Evaporation Chamber. [22]

External Quantum Efficiency (Q.E.) measurement was done using an Oriel cornerstone 260 monochrometer. Q.E is defined as the number of electron-hole pairs collected for each incident photon. The measurements were calibrated using a Silicon reference cell for 400-900nm. The output current at each wavelength is measured using

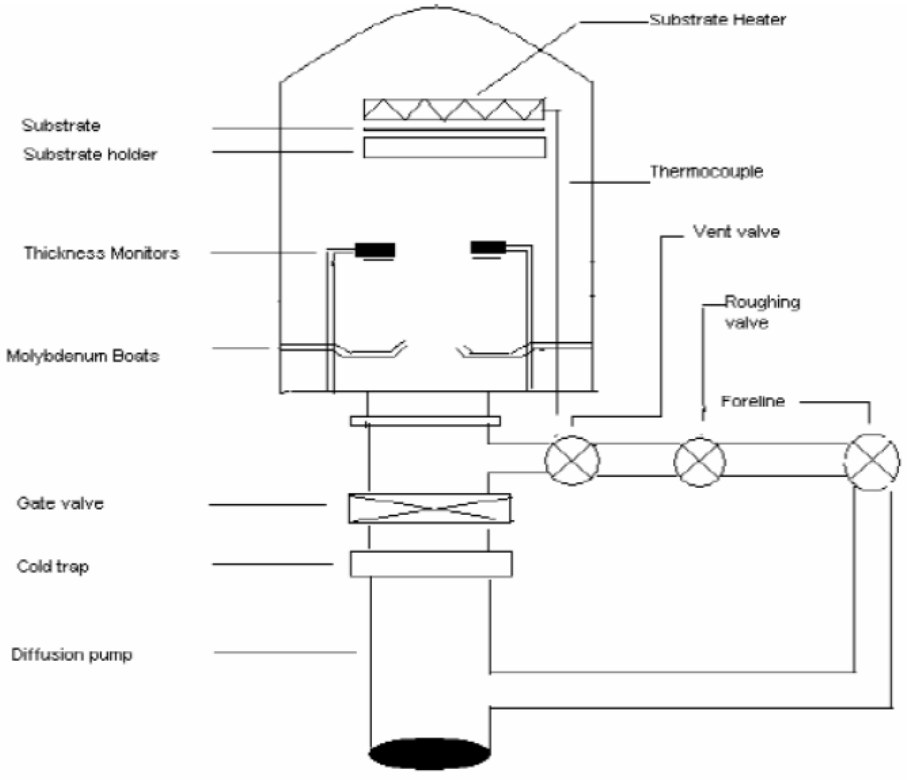


Figure 3.5 Schematic of Cu Evaporation Chamber. [27]

an ammeter and was normalized to the current from the silicon reference cell for CdSe cells and Silicon. The normalized current is multiplied with the Q.E of the reference cell to obtain Q.E of the sample. Current Density J_{sc} is calculated by integrating the area under the Q.E curve.

CHAPTER IV

RESULTS AND DISCUSSIONS

4.1 Results

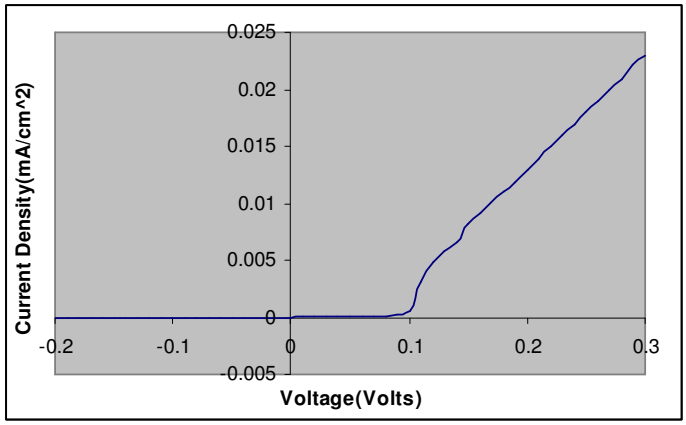
The main objective of this work was to improve the device performance by doping the window layer of the CdSe solar cells. But before experimenting with the doping of the window layer, the CdSe absorber layer had to be optimized. A new CdSe source that was prepared as mentioned in the previous chapter. After which a series of experiments were conducted to develop and optimize the conditions of CdSe deposition in order to achieve the standard performance of devices.

4.1.1 Optimization of CdSe as Absorber Layer

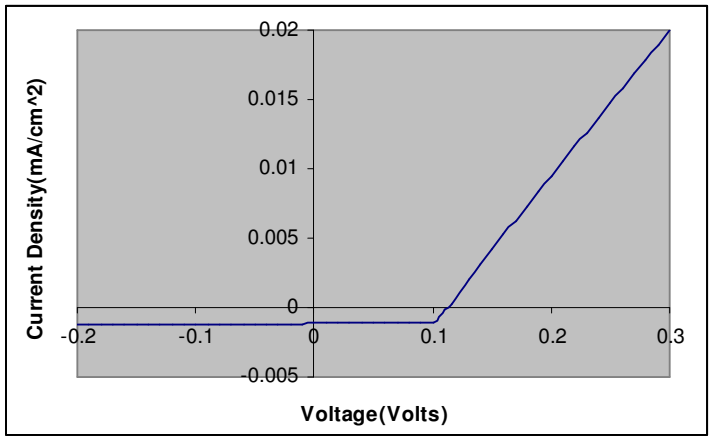
CdSe layer deposition was tried in a different way by depositing a thick layer of CdSe on a Corning 7059 glass substrate by CSS process and then using the same glass substrate as the source for depositing the CdSe layer of desired thickness. Initial depositions of CdSe were done with the same temperatures for substrate and source that were used to deposit with CdSe pellet as source. The resulting films were not as thick as 2 microns and had a large thickness gradient with thickness tapering towards the edges. The temperature of the source was lowered in 10^0C increments and a change in the uniformity of the deposited layer was observed. Uniformity in the CdSe layer was not observed until the temperature of the source was dropped down to 640^0C, but the films

still had a small thickness gradient which can be overlooked as the Cu dots are deposited on the central portion of the substrate.

Devices were made by depositing a ZnSe window layer on top of the CdSe layer. The device performance was not as good as the cells deposited by standard deposition procedures using a pellet as the source [27]. The Dark and Light IV curves are shown in figure 4.1 (a) and (b) respectively.



(a)



(b)

Figure 4.1 Dark and Light IV Curves for CdSe Glass Source.

As a result, we had to go back to the former procedure where CdSe was deposited by the CdSe pellet source directly by CSS.

4.1.2 CdSe/ZnSe Solar Cells

The performance of the CdSe had to be verified, and to achieve this, a ZnSe window layer was deposited on the top of CdSe layer. Standard CdSe/ZnSe solar cells that were fabricated previously were redone [27]. The best of the cells produced a voltage around 320mV and currents about 12.41mA/cm^2 with a fill factor of 40% as shown in figure 4.2 and 4.3. This showed that the CdSe layer has been optimized and ready for the next step of depositing a ZnTe layer on top of it.

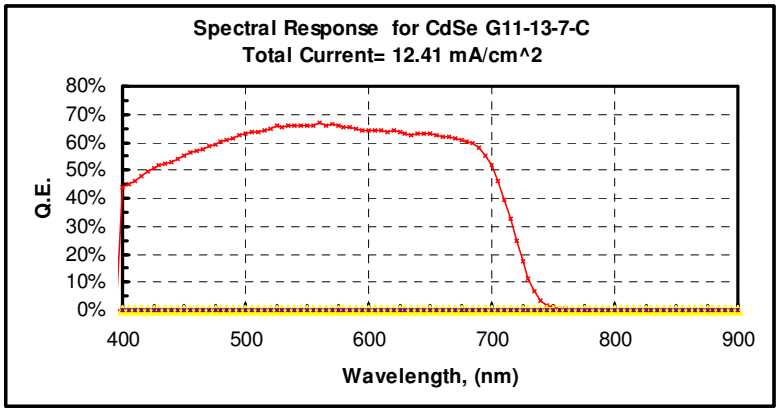
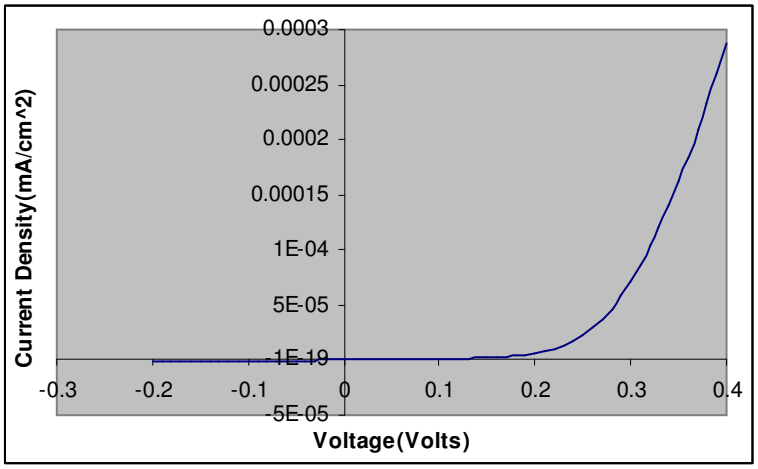
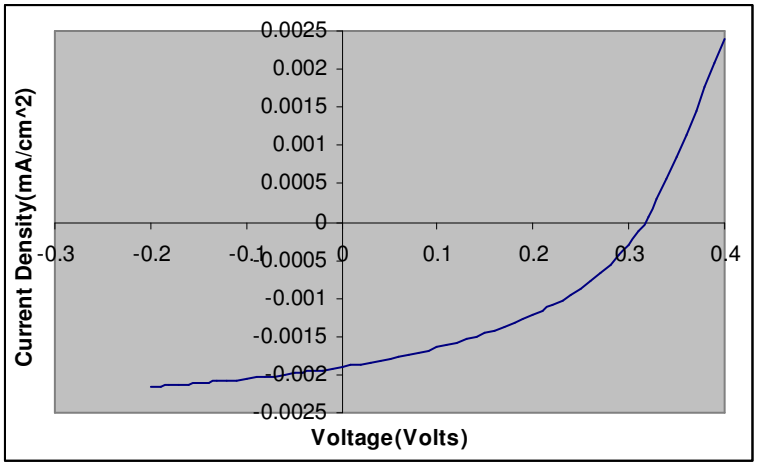


Figure 4.2 Spectral Response of CdSe/ZnSe Solar Cell.



(a)



(b)

Figure 4.3 Dark and Light IV Curves for CdSe/ZnSe Solar Cell.

4.1.3 CdSe/ZnTe Solar Cells

CdSe/ZnTe solar cells prepared by vacuum evaporation have exhibited a voltage of 400mV but the currents were as low as 3mA [22]. The ZnTe powder source in use was tellurium rich (Zn 45%, Te 55%). So, the substrate was heated in order to prevent excess tellurium from sticking to the growth surface and as a result making the film tellurium deficient. 200^0C was selected as the starting temperature and increased in steps of 50^0C.

The cells deposited at 300^0C exhibited the highest voltages but the currents were less than 1mA. The voltages at each temperature are shown in the table.

Table 4.1 Voltages for CdSe/ZnTe Solar Cells at Different Substrate Temperatures.

Substrate Temperature(^{0}C)	Voltage(milli Volts)
200	40
250	130
300	160
350	80
400	50
500	0

Due to equipment failure the deposition of the ZnTe was switched to the CIGS chamber. Unfortunately at the same time the MOCVD chamber for Tin Oxide deposition also had problems. We started using the TEC 25 glass substrates and the device performance was inferior compared to the cells fabricated in the old chamber. The TEC glass was suspected of playing an important role in this failure, and a series of experiments were done to investigate the effect of the TCO.

4.1.4 Effect of TCO on Device Performance

Devices made on TEC glass in the CIGS chamber did not perform as devices fabricated in the old chamber. As both the ZnTe chamber and the MOCVD chamber had

problems at the same time, it was necessary to determine the influence of these changes independently. So, devices had to be made using a transparent back contact which was known to give good results. ITO that was being used to make CdTe solar cells was used as the TCO to compare the performance with TEC glass. Devices made with ITO had no significant effect on the performance but improved the currents by a very small value. So, concluding that the TCO had no significant effect on the device performance, it was apparent that the ZnTe layer was limiting performance.

4.1.5 Copper Doping of ZnTe

Voltages around 630mV were achieved with ZnTe/CdSe where the ZnTe was deposited by CSS from a ZnTe/glass source that was deposited from powder by CSS [23]. Using vacuum deposition of ZnTe produced lower V_{oc}'s [20]. However doping was not possible in a CSS reactor due to process constraints, and it was desired to revisit ZnTe by vacuum evaporation and use Cu doping.

The copper doped ZnTe films were deposited by co-evaporation. Cu dots were deposited, and results of dot to dot resistance measurements are plotted as shown in figure 4.4. From the slopes the conductivity of the film was calculated to be 1.7e3 S/cm. Assuming a mobility of 1 cm^2/Vs results in doping concentration of order 1e22 $holes/cm^3$ which indicates a substantial doping. However, extrapolation of the slopes indicates a 200-300 Ω contact resistance with the Cu dots. This was puzzling as tunneling contact should have been realized at these charge densities. This was overlooked then, since Voc was the primary target and should not be affected by contact resistance.

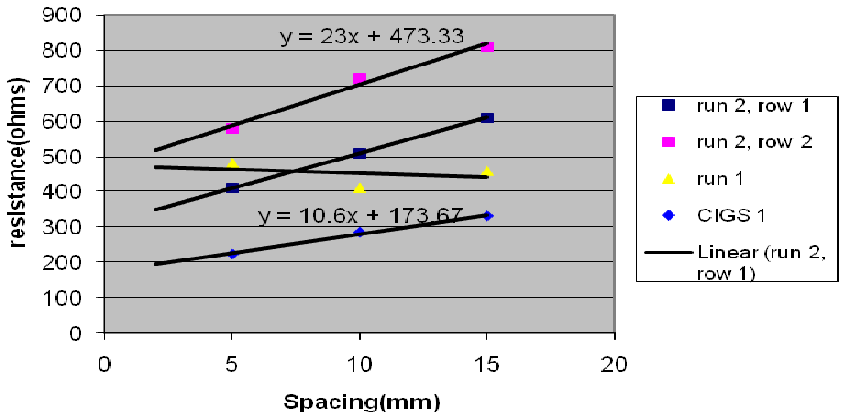


Figure 4.4 Plot of Dot to Dot Resistance Measurements.

Efforts were then directed to device fabrication. In the following the ZnTe:Cu is deposited in the CIGS deposition chamber. Typical Voc's are of order 250 mV and Jsc's are 1 mA/cm^2. Typical dark and light IV curves are shown below. It is obvious that there is significant shunting which is hurting Voc.

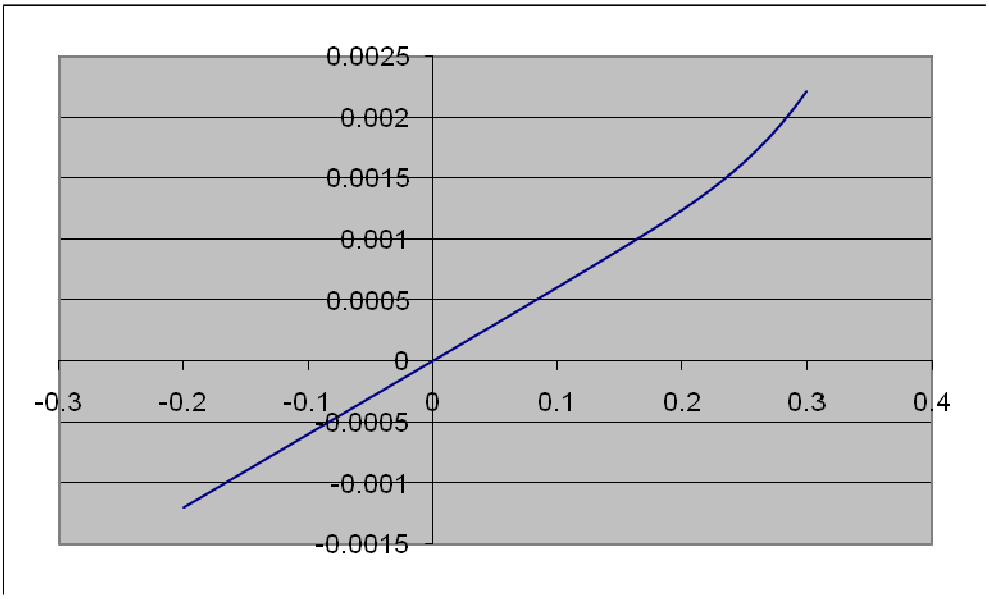


Figure 4.5(a) Dark IV Curves for Cu Doped CdSe/ZnTe Solar Cell.

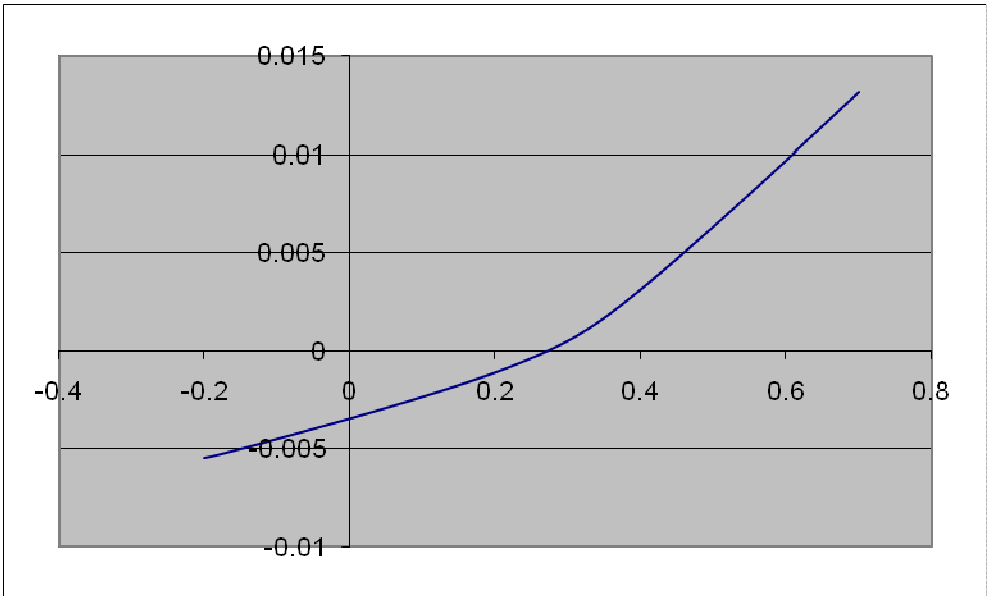


Figure 4.5(b) Light IV Curves for Cu Doped CdSe/ZnTe Solar Cell.

The above IV curves are for a 200 nm thick ZnTe:Cu layer. It is speculated that the Cu is the cause of shunting. To reduce its influence a sample was made in which the first 100 nm of ZnTe was undoped, and a 100 nm doped layer deposited on top of it. The effect on the IV is shown below in figure 4.6.

The undoped sample shows minimal shunting, while the doped is still clearly shunted even though the 100 nm doped layer is isolated from the junction by a 100 nm undoped layer.

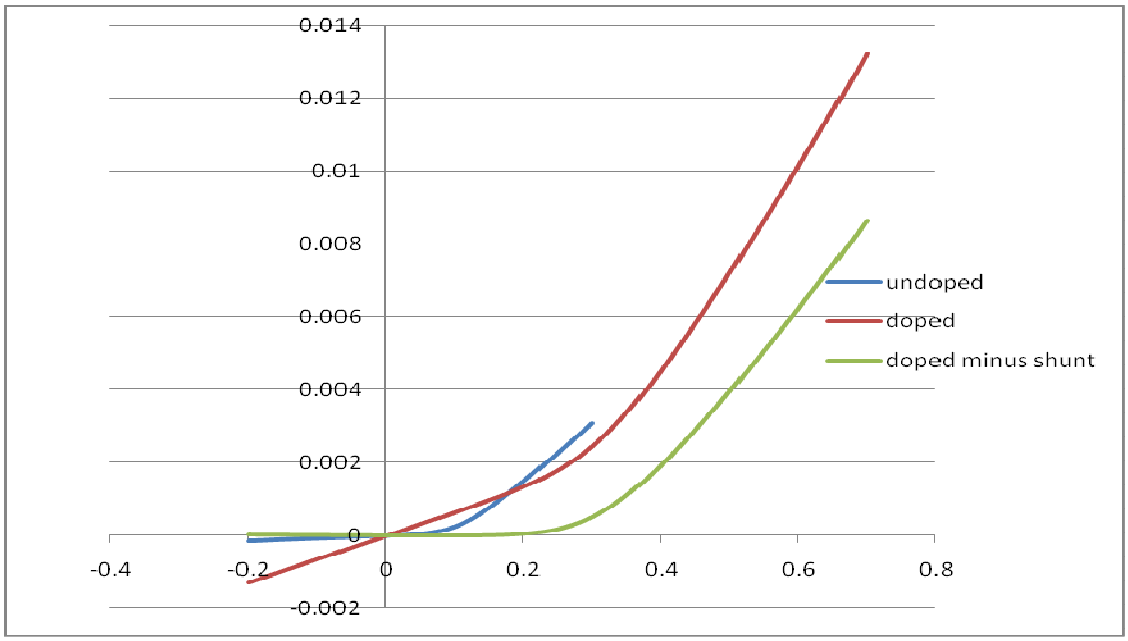


Figure 4.6 Dark IV Curves for 100nm Undoped and Cu Doped CdSe/ZnTe Solar Cell.

Subtracting the shunt from the doped IV curve produces a net dark IV that with superposition would result in a Voc of order 500 mV. The QE response for these devices is shown below.

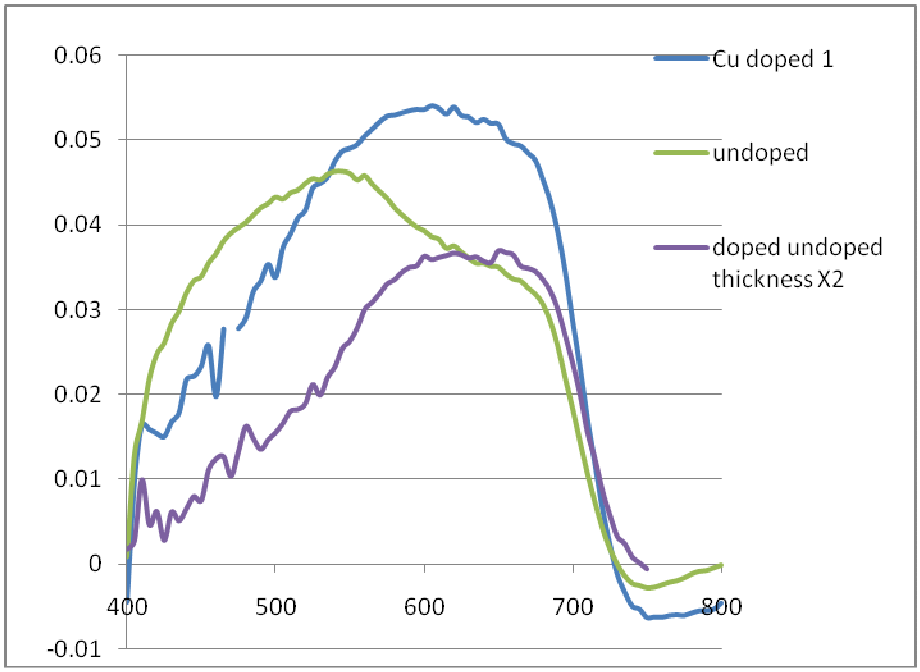


Figure 4.7 QE Response for 100nm Cu Doped CdSe/ZnTe Solar Cell.

As can be seen, there is notable difference in the spectra for doped vs. undoped. In particular the QE is lower in the region below 550 nm where ZnTe absorbs most for the doped film. To check this further another sample was made the same as the doped sample except that the undoped region was increased from 100 to 200 nm. This resulted in the drop in QE shown above. To compare directly, the ratio of the 100 nm doped to 200 nm doped is plotted below.

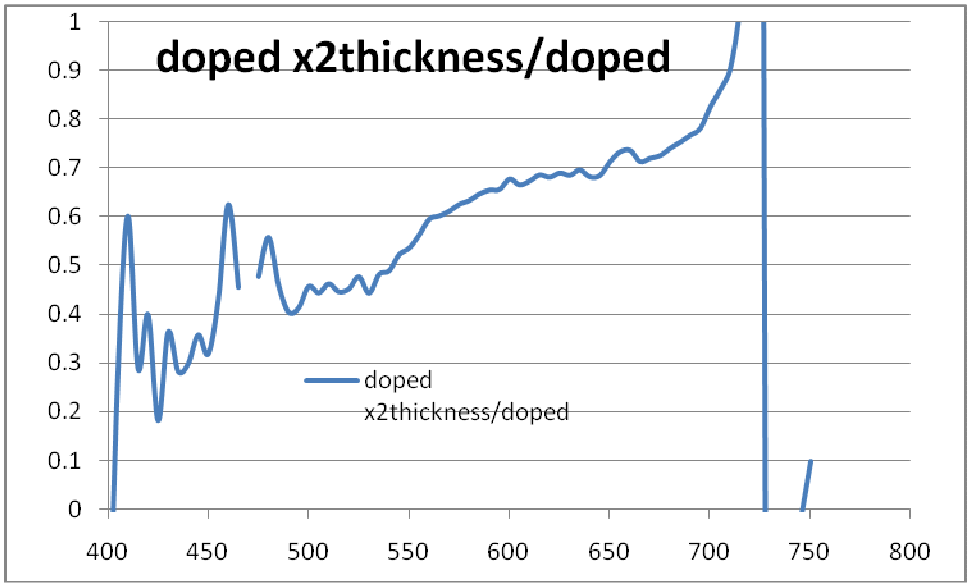


Figure 4.8 QE Response of Undopedx2 Thickness/Doped CdSe/ZnTe Solar Cell.

As can be seen, the ratio is about 0.5 in the region below 550 suggesting that doubling of the undoped thickness cut the QE in half. This indicates that even the undoped ZnTe layer is dead. Further, the transmission for 200 nm of ZnTe is about 65% in the region 550-750 nm which is consistent with the ratio in that region shown above. Also, the shunting showed little improvement indicating that it is very difficult to keep the Cu from reaching the junction region with ZnTe.

4.1.6 CdSe/$ZnTe_xSe_{1-x}$ Solar Cells

From the doping results it was evident that the doping really helped the device performance but was being limited by the undoped ZnTe layer. So, efforts were made to improve the undoped ZnTe layer. The substrate temperature was raised to 500^0C to prevent incorporation of excess Tellurium. In the process of heating the substrate to 500^0C, the CdSe may start losing Se from it. So, Se flux was introduced to compensate this loss. The Se fills any tellurium vacancies produced at such a high temperature. Care has been taken by adjusting the deposition rates to prevent Se from driving off Te from ZnTe.

Early experiments resulted in bad devices, and the IV curves were electrically shorted. The same ZnTe deposition with Se flux was done on glass to see the properties of the layer. Surprisingly, the glass substrate had only slight traces of a deposited material on the substrate. The ZnTe was deposited at 5 times the rate of Se for this run. The Se flux at the growth surface of the substrate might have been stopping the ZnTe from being deposited on the substrate. So, for the next run, the rate of the ZnTe has been further increased by 5 times. A thick layer of ZnTe with Se was evident on the substrate. The transmission response showed the presence of a fair amount of Se. This was repeated on top of a CdSe layer which still resulted in shorted IV curves. The ZnTe with Se might have crystallized and would be leaving spaces in between the grain boundaries and there by allowing the copper dots to reach the interface and as a result shorting the junction. Efforts were made to make this layer thicker, but had the same results were the same.

CHAPTER V

CONCLUSIONS

As discussed in the first chapter, the goal of achieving efficiencies greater than 25-30 % in a solar cell is possible only by fabricating a Tandem cell. A 4-terminal tandem solar cell has two cells of suitable band gaps placed one over the other with a proper encapsulant between them. According to the initial investigation, low band gap CIGS serves well as an absorber layer in the bottom cell. Significant efforts have been put in finding the suitable absorber for the top cell. In order to attain high efficiencies the band gap of the material should be between 1.5 eV and 2.0 eV. Further investigation resulted in opting for CdSe. The band gap of CdSe is 1.7 eV.

As a part of this study, the doping of the window layer for the CdSe solar cell has been investigated. The experiments performed partly confirmed positive effect of copper doping. The various experiments performed showed that the copper diffuse readily into ZnTe window layer and is hard to prevent copper from reaching the CdSe/ZnTe interface. Experiments confirmed insignificant influence of the TCO on device performance. ITO was used to confirm this result, and it resulted in the increase of current by a very small value. Doping has been varied with thickness and was found to help the device performance but showed a huge amount of shunting in the IV Curves. Efforts were made to make the undoped layer thick, and results showed reduction in shunting but the device

performance was still inferior. This confirmed the undoped ZnTe layer to be defective, and a series of experiments were conducted to make the undoped ZnTe layer better. Se flux was introduced to make the layer better but initial experiments done at high substrate temperatures resulted in electrically shorted cells. This was assumed to happen due to crystallization of the $ZnTe_xSe_{1-x}$ layer allowing the copper to pass through grain boundaries and reach the interface. Further experiments consisted of depositing a undoped ZnTe layer and depositing a $ZnTe_xSe_{1-x}$ later on top of it but resulted in shorted IV curves with voltages of around 30mV. This showed the positive effects of copper doping on the ZnTe window layer.

The future works that can be suggested is to optimize the undoped layer before doping it with copper. Depositing a $1000A^0$ ZnTe layer by CSS and depositing a doped layer of $1000A^0$ on top of it can also give some important information about the behavior of the ZnTe layer.

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