THERMAL ANALYSIS OF HIGH POWER LED ARRAYS

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THERMAL ANALYSIS OF HIGH POWER LED ARRAYS

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Looking back over my Master's study, it was not only the time to pursue my academic degree but also a growth process for me. I have learned how to do research by myself and collaborate with others and how to complete my task. These valuable experiences will benefit for my Ph.D. study and for the rest of my life.

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SUMMARY

LEDs are being developed as the next generation lighting source due to their high efficiency and long life time, with a potential to save $15 billion per year in energy cost by 2020 [1]. State of the art LEDs are capable of emitting light at ~115 lm/W and have lifetime over 50,000 hours. It has already surpassed the efficiency of incandescent light sources, and is even comparable to that of fluorescent lamps. Since the total luminous flux generated by a single LED is considerably lower than other light sources, to be competitive the total light output must be increased with higher forward currents and packages of multiple LEDs. However, both of these solutions would increase the junction temperature, which degrades the performance of the LED—as the operating temperature goes up, the light intensity decreases, the lifetime is reduced, and the light color changes. The word "junction" refers to the p-n junction within the LED-chips. Critical to the temperature rise in high powered LED sources is the very large heat flux at the die level (100 – 500 W/cm2) which must be addressed in order to lower the operating temperature in the die. It is possible to address the spreading requirements of high powered LED die through the use of power electronic substrates for efficient heat dissipation, especially when the die are directly mounted to the power substrate in a chip-on-board (COB) architecture. COB is a very attractive technology for packaging power LEDs which can lead improved price competiveness, package integration and thermal performance.

In our work high power LED-chips (>1W/die) implementing COB architectures were designed and studied. Substrates for these packaging configurations include two types of power electronic substrates; insulated-metal-substrates (IMS) and direct-bonded-

copper (DBC). To lower the operating temperature both the thermal impedance of the dielectric layer and the heat spreading in the copper circuit layers must be studied. In the analysis of our architectures, several lead free solders and thermal interface materials were considered. We start with the analysis of single-chip LED package and extend the result to the multi-chip arrays. The thermal resistance of the system is only a function of geometry and thermal conductivity if temperature-independent properties are used. Thus through finite element analysis (ANSYS) the effect of geometry and thermal conductivity on the thermal resistance was investigated. The drawback of finite element analysis is that many simulations must be conducted whenever the geometry or the thermal conductivity is changed. To bypass same of the computational load, a thermal resistance network was developed. We developed analytical expressions of the thermal resistance, especially focusing on the heat spreading effect at the substrate level. Finally, multi-chip LED arrays were analyzed through finite element analysis and an analytical analysis; where die-spacing is another important factor to determine the junction temperature. With this thermal analysis, critical design considerations were investigated in order to minimize device temperatures and thereby maximizing light output while also maximizing device reliability.

CHAPTER 1

INTRODUCTION

1.1 Motivation of Research

1.1.1 High-Power LEDs as a General Light Source

Solid-state lighting (SSL) is a technology which uses semiconductor materials to convert electricity into light. SSL comes in two basic categories; light-emitting diodes (LEDs) based on inorganic (non-carbon based) materials, and organic light-emitting diodes (OLEDs) based on organic (carbon based) materials. SSL was discovered in the early twentieth century, and LEDs were introduced as practical electronic components in 1962 [2]. Early LEDs emitted low-intensity light with limited color and mainly used as signal components in electrical system. These low-power LEDs are still very widely used as indicators and signs. The applications of modern LEDs became very diverse since they generate all range of visible light and even ultraviolet light with very high brightness. One of the main applications of modern LEDs is a general light source using high-power white LEDs. These high-power LEDs have high efficiency comparable to fluorescent lamps and very long life time exceeding any other traditional light sources. By implementing LEDs into a light source, it is expected to save $15 billion per year in energy cost by 2020 [1]. The main breakthroughs in LEDs as a light source came from the development of synthesis and fabrication in gallium nitride (GaN). Before the advent of GaN based LEDs, the lack of blue and ultraviolet (UV) light which are necessary to produce white light hindered the development of LEDs into a light source. GaN is a wide bandgap (3.4eV) material used in high-power and high frequency device. Therefore, LEDs based on GaN not only generate blue and ultraviolet light, which can produce

white light, but also operate at high power. Although the current application is limited due to their high cost, LEDs will gradually replace other general light sources over time, saving significant energy and money.

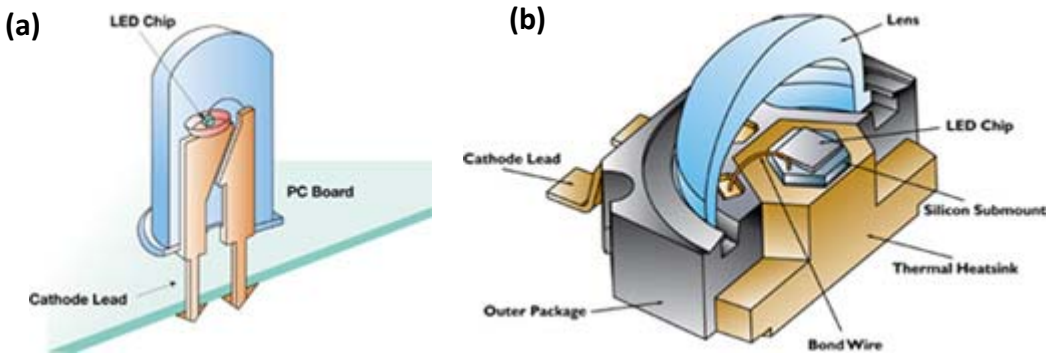


Figure 1. (a) typical construction of low-power LED, 5 mm type (b) construction of a high-power LED, LUXEON® K2 Power LED [3]

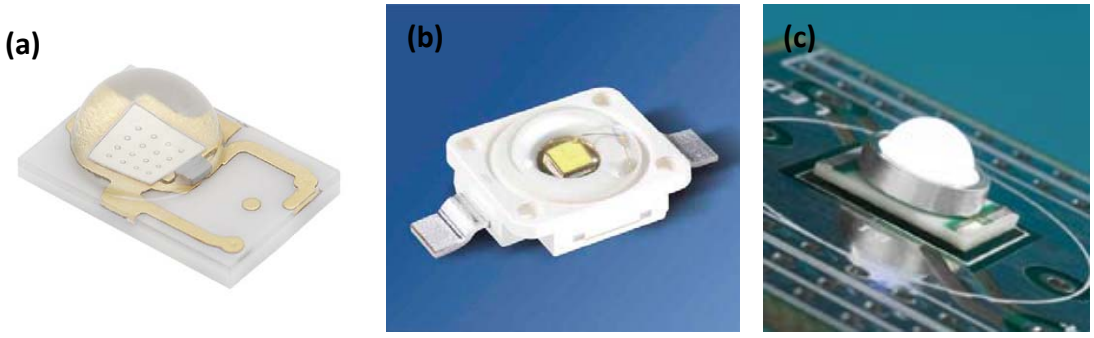


Figure 2. High-power LEDs (a) LUXEON Rebel, Philips Lumileds [3]. (b) Golden DRAGON Plus, OSRAM Opto Semiconductors [4] (c) XLamp XR-E, Cree Inc [5].

1.1.2 Advantages of LEDs as a General Light Source

There are many advantages in using LEDs as a general light source. First of all, LEDs have high luminous efficiency. Table 1 shows luminous efficacy and efficiency of incandescent, fluorescent and LED light. Energy efficiency of a light source is typically measured in lumens per watt (lm/W) known as luminous efficacy, meaning the amount of light produced for each watt of electricity consumed by the light source. Luminous efficiency the ratio of the actual efficacy to the theoretically maximum efficacy, 683-lm/W. The efficiency of LEDs has already surpassed that of incandescent light sources,

and is even comparable to that of fluorescent light. Currently the highest efficiency of high-power white LED is claimed by Philips Lumileds with a luminous efficacy of 115-lm/W at 350 mA. Moreover, the efficiency of LEDs is on a path to exceed that of fluorescent lighting in the near future. In fact, Cree Inc. issued a press release in November 2008 concerning a laboratory prototype LED achieving 161 lm/W at room temperature [6].

Table 1. Luminous efficacy and efficiency of various light sources [7]

Light Source	Type	Luminous efficacy (lm/W)	Luminous efficiency
Incandescent	40 W tungsten incandescent (120V)	12.6	1.9%
	100 W tungsten incandescent	17.5	2.6%
	Quartz halogen (12-24 V)	24	3.5%
Fluorescent	9-26 W compact fluorescent	57-72	8-11%
	T8 tube with magnetic ballast	80-100	12-15%
HID	Metal halide	65-115	9.5-16.8%
LED	High-Power White LED	-115	-16.8%

LEDs also have a very long lifetime. The lifetimes of the various light sources are compared in Table 2. The most common way for LEDs to fail is the gradual lowering of light output and loss of efficiency, while sudden failures which commonly occur in incandescent lamps are very rare. To standardize the lifetime of LEDs, the terms L_{70} and L_{50} are used, which refers to the time it will take LEDs to reach 70% and 50% light output compared to the initial light output, respectively. Most manufacturers of high-power white LEDs estimate a lifetime of around 35,000-50,000 hours with L_{70}, assuming operation at 350 mA constant current and maintaining junction temperature at no higher than 90°C. Currently LED durability continues to improve, allowing for higher drive currents and higher operating temperature.

Table 2. Life time of various light sources. [8]

Light Source	Range of Typical Rated Life (hours)
Incandescent	750-2,000
Halogen incandescent	3,000-4,000
Compact fluorescent	8,000-10,000
Metal halide	7,500-20,000
Linear fluorescent	20,000-30,000
High-Power White LED (estimated useful life by L_{70})	35,000-50,000

Another advantage of LEDs is that their lamps are amenable to having a compact size and low profile. A LED single chip is typically 1 mm^2 or smaller in size which allows for unique form factors for LED light sources not obtainable from other technologies. In order to produce equivalent light output as obtained with traditional light sources, it is required to use multiple LEDs in most luminaires. Since multiple LEDs increase the amount of heat that must be dissipated, a heat-sink is needed for proper thermal management which results in a large LED fixture. However, based on a given luminous output, LED light sources are typically smaller than their conventional lighting counterparts. Due to their compact size, LEDs are an excellent option where size or weight is a concern. In addition to these major benefits, there are many other advantages. LED lamps are robust and non-toxic. LEDs are semiconductor devices and usually do not use any glass and filament, while incandescent, fluorescent, and high-intensity discharge (HID) lamps do. Also, LEDs do not contain mercury, unlike fluorescent lamps. Directional light emission of LEDs reduces wasted light. LEDs emit light hemi-spherically, while other light sources emit light in all directions. Optics and reflectors can be used to make directional light sources, but they cause light losses and additional cost.

1.1.3 Energy Saving

In spite of many advantages, the high price of LEDs is the main obstacle in using LEDs as a light source. LEDs are currently more expensive, price per lumen, on an initial cost basis, than other light sources. However, considering the total cost which includes energy and maintenance costs, LEDs are competitive enough at present and continues to improve. The economic analysis of using LEDs as general light source was conducted by the U.S. Department of Energy (DOE) [9]. In this project high-pressure sodium (HPS) fixtures were replaced with LED Luminaires as shown in Figure 3. Table 3 summarizes the energy savings for this project and shows that the LED installation both saved energy and improved the lighting quality in this demonstration. For this application a 3-bar (60 LEDs) luminaires were designed to produce similar illumination level to the existing HPS luminaires. However, 2-bar (40 LEDs) luminaires would also easily provide the recommended minimum level of illumination needed for this application (0.5 fc, foot-candle), while going to the lower wattage luminaire would significantly improve the economic payback achieved.

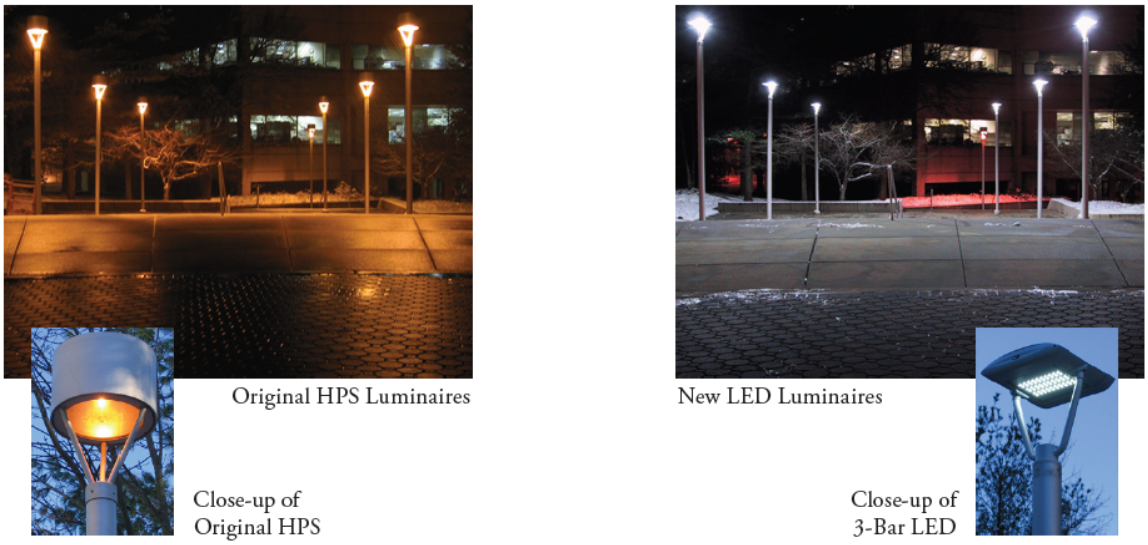


Figure 3. High-pressure sodium (HPS) fixtures (left) were replaced with LED pole-top mounted luminaires (right) to illuminate a pedestrian area at a Federal Aviation Administration facility in Atlantic City, NJ. [9]

Table 3. Existing Lighting Data and Results from LED Replacement Luminaires [9].

	Existing 70W* HPS	New 3-bar Luminaire	Optional 2-bar Luminaire
Average illumination levels	3.54 fc	3.63 fc	2.42 fc
Max/Min Ratio**	6.04:1	2.68:1	2.68:1
Minimum illuminance	1.25 fc	1.90 fc	1.27fc***
Total power draw****	97W	72W	48W
Energy consumption per luminaire	425 kWh/yr	311 kWh/yr	210 kWh/yr
Energy savings per luminaire	N/A	114 kWh/yr (26.8%)	215 KWh/yr (50.6%)

*Nominal wattage.
**Measurement of lighting uniformity; lower ratios indicate more uniformly lighted area.
***Calculated value
****Energy consumption for the HPS system is based on manufacturer-rated power levels for lamps and ballasts, multiplied by 4380 hours per year. Energy consumption for the 3-bar LED unit is based on laboratory power measurements multiplied by 4380 hours per year. Energy consumption for the 2-bar unit is based on manufacturer-rated power levels multiplied by 4380 hours per year.

Table 4. Results of Economic Analysis for Replacing Fixtures at End of Life [9].

Base Case	Alternative Case	Net Savings*	Savings to Investment Ratio (SIR)	Adjusted Internal Rate of Return (AIRR)	Simple Payback (Years)†	Discounted Payback (Years)†
HPS, replace fixture, energy only (no maintenance)	3-bar SSL	($224)	0.36	-1.45%	—	—
HPS, replace fixture, including maintenance	3-bar SSL	$513	2.46	7.14%	7	7
HPS, replace fixture, energy only (no maintenance)	2-bar SSL	$103	1.51	4.87%	10	12
HPS, replace fixture, including maintenance	2-bar SSL	$839	5.16	10.67%	3	3

*Net Savings is the Life Cycle Cost (LCC) of the Alternative Case subtracted from the LCC of the Base Case.

†A blank space indicates that payback is not achieved within the design lifetime of the LED (23 years or 100,000 hrs).

In this project, the LED product demonstrated energy savings of more than 25% while maintaining illuminance levels and improving illuminance uniformity. Table 4 displays the results of an economic analysis using 2-bar and 3-bar LED luminaires across a range of scenarios. The scenarios vary two important aspects of the situation: whether or not maintenance savings are included in the estimates and whether or not the original HPS fixtures are destined for replacement regardless of what they will be replaced with. Payback ranges vary widely depending on how these factors are treated.

In 2007 the United State used 4.157 billion kWh of electricity and 22 to 25% was used for lighting alone [10]. The U.S. Department of Energy (DOE) is expecting to save $15 billion per year in energy cost by 2020 by adapting LED luminaires [1].

1.1.4 Why Thermal Management?

Like a normal diode, the LED consists of p-type and n-type semiconductor materials creating a p-n junction. Once power is applied, the luminescence reaction occurs at p-n junction and energy is released in the form of light, also known as luminous flux. In the reaction only some portion of energy turns into luminous flux, and the rest turns into the form of heat. By this heat generation, the p-n junction has the highest temperature in the device and this is called as junction temperature. The junction temperature of LEDs is very important because parameters such as lifetime and luminous flux largely depend on it. All light sources convert electric energy into radiant energy and thermal energy in various proportions (see Table 5). The portion of heat generated which must be dissipated by conduction and convection in LEDs is remarkably larger than other light sources. Therefore, without proper thermal management the junction temperature goes up excessively.

Table 5. Power Conversion of White Light Sources [8]

	Incandescent (60W)	Fluorescent (Typical)	Metal Halide	LED
Visible Light	8%	21%	27%	15-25%
IR	73%	37%	17%	0%
UV	0%	0%	19%	0%
Total Radiant Energy	81%	58%	63%	15-25%
Heat (Conduction+Convection)	19%	42%	37%	75-85%
Total	100%	100%	100%	100%

Let's consider the high-power LEDs which have 1 mm^2 chip and operate at 5 W. Assuming 20% efficiency, the heat generation is 4 W and the heat flux in the chip through the board goes up to 400 W/cm^2. When considering that the heat flux of CPU is 50 to 100 W/cm^2 [11], the thermal resistance of LEDs should be very large and very high junction temperature is expected without proper thermal management.

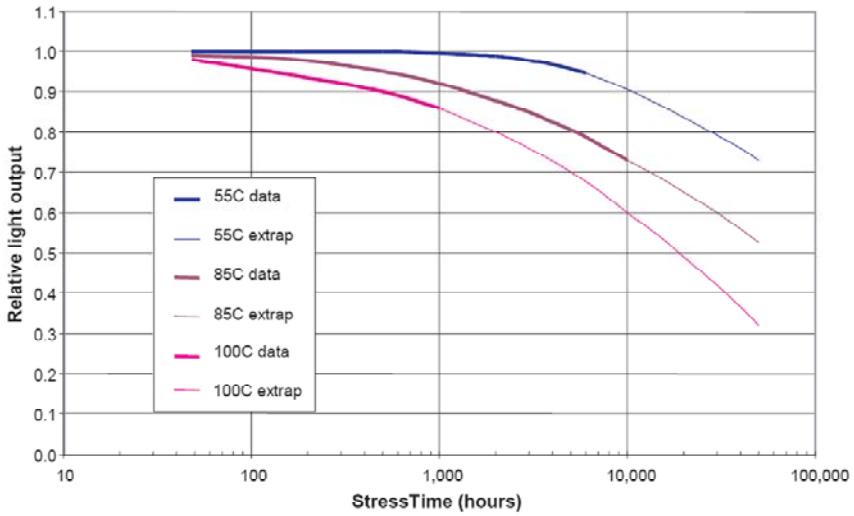


Figure 4. Relative light output vs. Stress time, LUXEON AlInGaP, LUMILED, driven at 350 mA at slug temperatures of 55°C, 85°C and 100°C (junction temperatures of 71°C, 101°C, and 116°C, respectively). [12]

One of the key impacts of the high junction temperature in LEDs is reduced expected lifetime. Continuous operation at elevated temperature dramatically reduces the lifetime of LEDs. For example, the Figure 4 shows the luminous flux characteristic of a LUXEON Rebel by Philips Lumileds over time. Three identical LEDs are used with the same current but with different junction temperature. Estimated lifetime by L_{70} is 5,000 hours, 11,000 hours, and 30,000 hours respectively with 116°C, 101°C, and 71°C of junction temperature. Overall, a higher junction temperature reduces the lifetime significantly. This characteristic also can be expressed in terms of lifetime as a function of junction temperature or thermal pad temperature (see Figure 5). Besides, most LED manufacturers specify the maximum junction temperature, which is usually between 130-

185°C and can be reached with high power input. Operating LEDs over the maximum junction temperature may cause immediate damage and failure in devices.

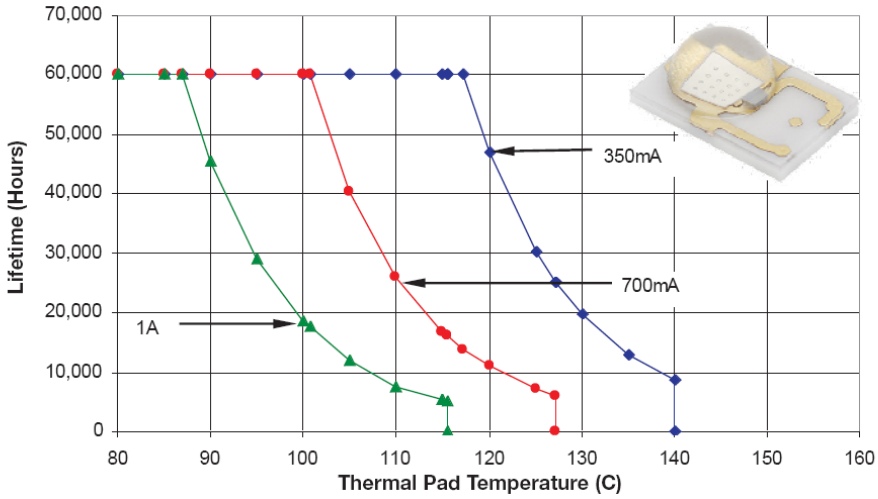


Figure 5. Expected lifetimes for InGaN LUXEON Rebel by Philips Lumileds (L_{70}) [13]

Reduced luminous flux is another important impact of high junction temperature in LEDs. As a result, luminous efficiency of LEDs is also reduced. The luminous flux decline depends on its wavelength or color, and generally a linear function of increasing junction temperature as shown in Figure 6. The luminous efficiency specified by a LED manufacturer is typically based on 25°C of junction temperature or thermal pad temperature. For example, the luminous efficacy of a LUXEON Rebel shown on its datasheet is 100 lm/W in cool white at 350mA. However, if it operates at 70 °C of thermal pad temperature, its luminous efficacy is decreased by 10% and produces 90-lm/W. Moreover, since the luminous flux generated by a single LED is considerably smaller than other light sources, the total luminous flux must be increased with higher forward currents and packages of multiple LEDs to be competitive. However, both of these solutions would increase the junction temperature, which is detrimental to the performance of the LED.

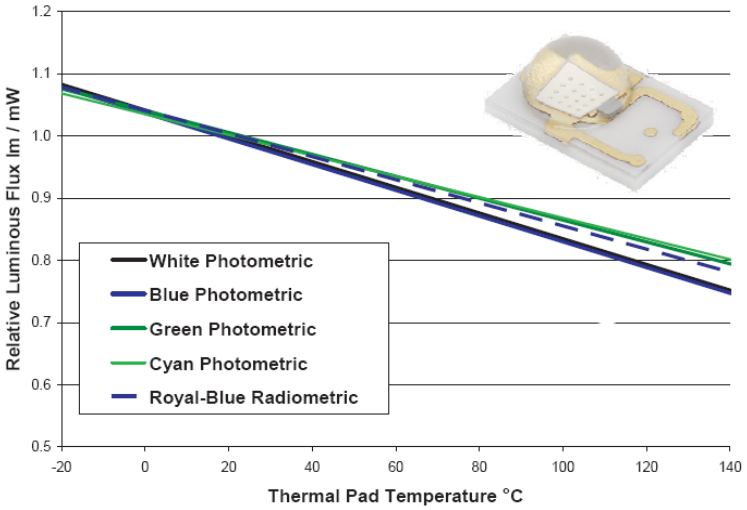


Figure 6. Relative Light Output vs. Thermal Pad Temperature for White, Green, Cyan, Blue and Royal-Blue, LUXEON Rebel, LUMILED [14]

As addressed previously, excess heat directly affects both short-term and long-term LED performance. With increasing luminous efficiency and reducing price, thermal management is one of the key issues for LEDs to be a next generation lighting source.

1.2 Thesis Overview

The purpose of this study is to investigate the thermal response of single chip and multichip LED-arrays and packaging methods which can be used to lower the junction temperature. In this work LED-chips implementing COB architectures were designed and studied. Substrates for these packaging included two types of power electronic substrates: insulated-metal-substrates (IMS) and direct-bonded-copper (DBC). In the analysis of our architectures, several lead free solders and thermal interface materials were considered. We present an analysis of the integration of power substrates in the packaging of high power LED (>1W/die) through finite element analysis (ANSYS) and an analytical analysis. With this thermal analysis, critical design considerations were

investigated in order to minimize device temperatures which will ultimately improve both light output and device lifetime and reliability.

Chapter 2 provides a background of LED devices. It discusses the basic principles of LEDs and the materials used for high-power white LEDs. The structure of LED-chips and the development of LED-arrays are included, and their advantages and disadvantages are discussed. Finally, current thermal management approaches are investigated. Chapter 3 focuses on the finite element analysis of single chip-LED packages. The effect of each layer in the package architecture on the junction temperature is studied and the resistances for a thermal circuit model are analyzed by FEA. Chapter 4 discusses the analytical modeling of a single chip-LED package. The LED package is divided into three components and the analytical expression of thermal resistance of each component is derived. Comparisons with FEA analysis show the power and utility of the analytical technique which provides a major contribution of my thesis. Chapter 5 then provides an array analysis and simulations of actual devices. Based on the analytical modeling of a single-chip LED package, the LED array is also analyzed analytically and some design considerations are made through the use of these simulations. Chapter 6 states the final conclusions and proposes future work to further the development of the thermal management of LEDs.

CHAPTER 2

BACKGROUND

2.1 LED Basics

2.1.1 How LEDs work

LEDs are different from traditional light sources in the way they produce light. In an incandescent lamp, a tungsten filament is heated by electric current until it glows or emits light. In a fluorescent lamp, mercury atoms are excited by an electric arc and emit UV radiation. By striking the phosphor coating on the inside of glass tubes, the UV radiation is converted and emitted as visible light. In contrast, LEDs are based on a semiconductor diode. Like a normal diode, the LED consists of a chip of semiconducting material doped with impurities creating a p-n junction. When the LED is connected to a power source, current flows from the p-side or anode to the n-side, or cathode, but not in the reverse direction. Charge-carriers (electrons and electron holes) flow into the junction from electrodes. When an electron meets a hole, it falls into a lower energy level, and releases energy in the form of photons (light) (see Figure 7).

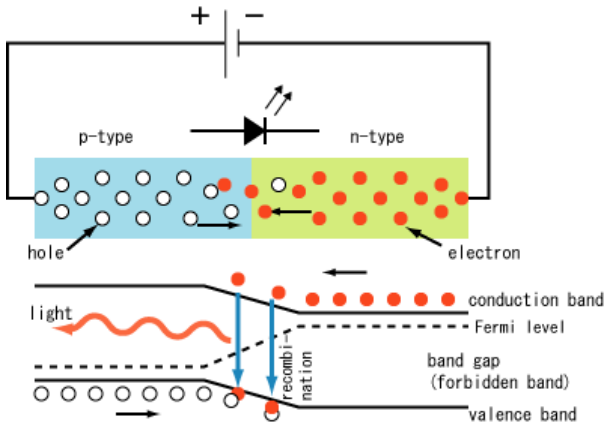


Figure 7. The inner working of an LED [7]

The specific wavelength or color emitted by the LED depends on the materials used to make the diode. Red LEDs are based on aluminum gallium arsenide (AlGaAs). Blue LEDs are made from indium gallium nitride (InGaN) and green from aluminum gallium phosphide (AlGaP). "White" light is created by combining the light from red, green, and blue (RGB) LEDs or by coating a blue LED with yellow phosphor.

2.1.2 White Light with LEDs

White light can be achieved with LEDs in two main ways; phosphor conversion and RGB systems. In phosphor conversion a blue or near-ultraviolet (UV) chip is coated with phosphor(s) to emit white light, while in RGB systems light from multiple monochromatic LEDs (red, green, and blue) is mixed, resulting in white light. The phosphor conversion approach is most commonly based on a blue LED. When combined with a yellow phosphor (usually cerium-doped yttrium aluminum garnet or YAG:Ce), the light will appear white to the human eye. Research continues to improve the efficiency and color quality of phosphor conversion. Each approach to producing white light with LEDs has certain advantages and disadvantages. The key trade-offs are among color quality, light output, luminous efficacy, and cost. The primary pros and cons of each approach at the current level of technology development are outlined in Table 6. Most currently available white LED products are based on the blue LED + phosphor approach. Phosphor-converted chips are produced in large volumes and in various packages (light engines, arrays, etc.) that are integrated into lighting fixtures. RGB systems are more often custom designed for use in architectural settings.

Table 6. Comparison of White Light LED Technologies [8].

	Phosphor conversion	RGB
Pros	- Most mature technology - High-volume manufacturing processes - Relatively high luminous flux - Relatively high efficacy - Comparatively lower cost	- Color flexibility, both in multi-color displays and different shades of white
Cons	- High CCT (cool/blue appearance) - Warmer CCT may be less available or more expensive - May have color variability in beam	- Individual colored LEDs respond differently to drive current, operating temperature, dimming, and operating time - Controls needed for color consistency add expense - Often have low CRI score, in spite of good color rendering

2.2 Structures of LED-chip

The conventional lateral-type of high power LEDs based on III-V nitrides (see Figure 8(a)) was firstly demonstrated by Nichia Chemical Industries, Ltd [15]. This structure consists of sapphire substrate, GaN buffer layer, n-GaN layer, active layer, p-GaN layer, and electrodes. Around 30 nm of the low-temperature GaN (LT-GaN) buffer layer is grown on a sapphire substrate. By growing LT-GaN layer firstly, the high quality n-GaN structure can be achieved. The n-GaN is 3 to 4 μm of thickness and usually doped by using Si. The active layer is around 50 nm, and consists of several different combinations of GaN related materials. A single-quantum well (SQW) or multi-quantum well (MQW) is formed inside the active layer, which make it possible to combine electrons and holes that have different energy levels and to emit light. Mg-doped p-GaN is deposited on top of the active layer can be achieved by following processes. A low-temperature GaN buffer layer is firstly grown at 550°C, followed by an n-GaN layer, an -Al Ga N cladding, a 50 nm In Ga N Zn-doped active region, a p-Al Ga N cladding, and an Mg-doped p-GaN layer. The LED process was completed by evaporating a p-type

contact consisting of NiAu and a thin NiAu current spreading layer. After chlorine RIE of the mesa, TiAl was evaporated as n-contact metal.

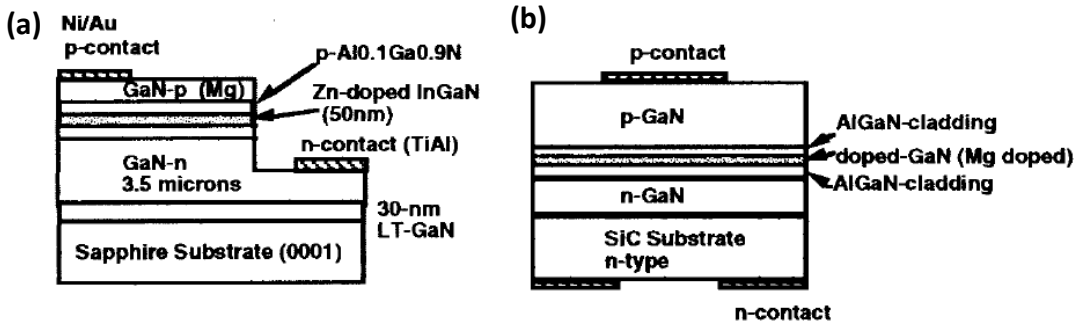


Figure 8. Two types of commercially available blue LEDs. (a) Laterally contacted devices with Zn-doped InGaN active region on sapphire substrates. (b) Vertically contacted devices on conducting SiC substrates.[15]

Another structure is the vertical type LED, which is grown on n-type SiC substrate by Cree Research, Inc. The main structural difference between the lateral and the vertical type is that the electrodes of vertical type LEDs are located the top and bottom of LED-chips and generally devices are placed on patterned circuit, while lateral type LEDs are connected using two wire-bonds. The vertical structure is advantageous due to its small residual stress and good thermal dissipation due to SiC substrate compare to the lateral structure which uses sapphire substrate. This is because SiC has a small lattice mismatch and small coefficient of thermal expansion (CTE) mismatch to GaN based materials, and high thermal conductivity (See Table7). Nevertheless, sapphire substrate is still competitive because SiC substrate is extraordinary expensive.

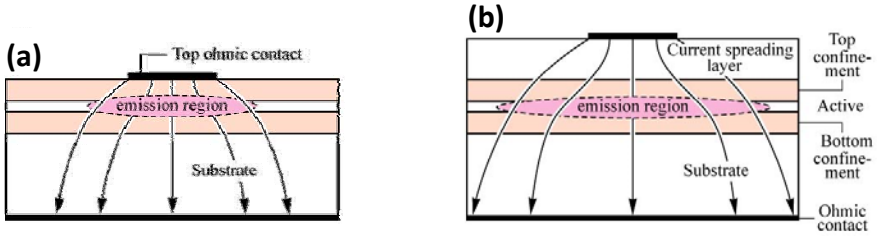


Figure 9. Illustrations of the effect of a current-spreading layer for vertical type high-power LEDs (a) without and (b) with a spreading layer [16]

The problem of these conventional structures is their low extraction efficiency. The extraction efficiency is the ratio of light generated to light extracted from device. The p-GaN has low electrical conductivity and must be grown after n-GaN due to Mg memory effect during MOCVD process [17]. Therefore, the current spreading layer is required on the top of devices. The nickel-gold composite (Ni/Au) and indium tin oxide (ITO) are generally used. By using a current spreading layer, significant degradation of light output takes place because they are semi-transparent. Ideally, this current spreading layer should be thick (>500 Å) to spread the current (see Figure 9), but in practice, it must be thin to minimize light absorption. Thus, a trade off exists between light extraction and spreading resistance. Also, another problem is the low thermal conductivity of sapphire substrates, 30 W/mK. The relatively poor thermal conductivity of sapphire substrates is one of the major limitations for its application in high power LEDs. Thus, it is difficult to extract heat through the die when using such thermally resistive materials.

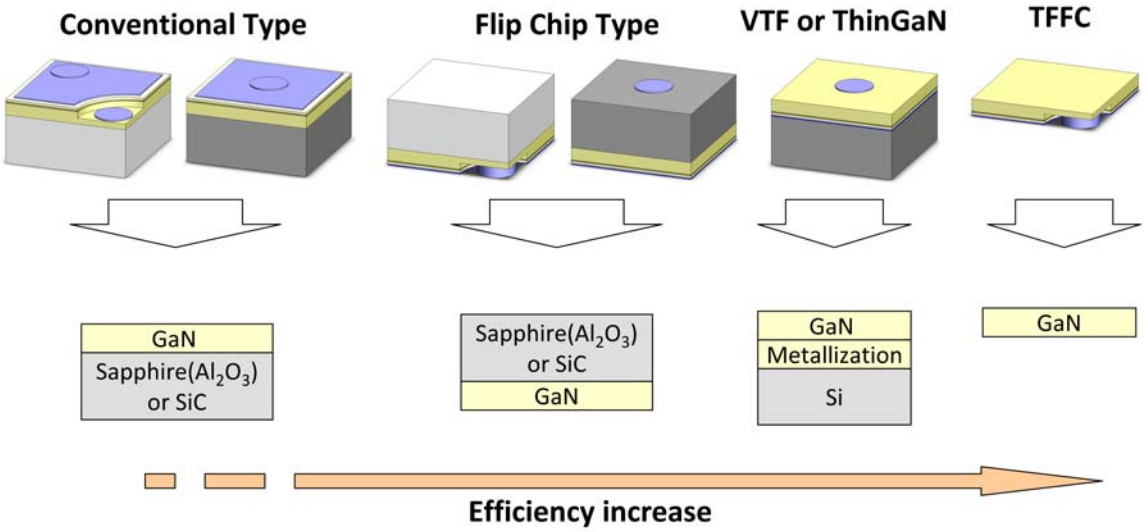


Figure 10. Illustrations of LED-chip structures.

The flip chip structure is one solution for these problems (see Figure 10). By flipping the chip, a current spreading layer can be placed on the bottom surface, therefore the extraction efficiency increases. The Osram ATON chip, which is a vertical type LED-chip grown on a SiC substrate, has a 52% extraction efficiency and the Osram NOTA chip, which is the flip-chip variant of ATON chip, has a 60% extraction efficiency [4]. Moreover, since the sapphire substrate is placed out of the path of heat dissipation, the junction temperature can be significantly reduced. In a flip-chip structure, however, because the sapphire substrate plays a role as light absorber, the extraction efficiency does not increase much. Also, high cost and technically demanding mountings are other disadvantages. Recently, more improvement has been achieved by the laser lift-off (LLO) technique [18-21]. The LLO technique involves substrate removal and transfer of the active device to alternative substrate by laser heating, therefore a p-side-down structure can be obtained (see Figure 11). The LED structure by LLO technique is shown in Figure 12, which is generally called ThinGaN or vertical thin-film (VTF) LED.

There are many advantages in ThinGaN structure. First of all, it is possible to eliminate the need for a current spreading layer that degrades light output because the high electrical conductivity of the n-GaN layer is placed on the top of the device. Osram ThinGaN chip has accomplished 75% of extraction efficiency [4]. Secondly, a low junction temperature can be achieved with high power input because the thermal conductivity of Si is 4 to 5 times higher than that of sapphire (see Table 7). Although we can use SiC as a substrate instead of Si and also achieve even lower junction temperatures, it is less competitive because SiC is extraordinary expensive. Thirdly, the residual stress in GaN device is reduced by the LLO process as well. GaN epi-layer grown on sapphire is under very high compressive stresses because of a large lattice mismatch and large coefficient of thermal expansion (CTE) mismatch between GaN and sapphire. Although CTE mismatch between GaN and Si substrate is larger than that between GaN and sapphire, the process results in relief in compressive stress since stress

induced by lattice mismatch is vanished and the transfer process is conducted much lower temperature.

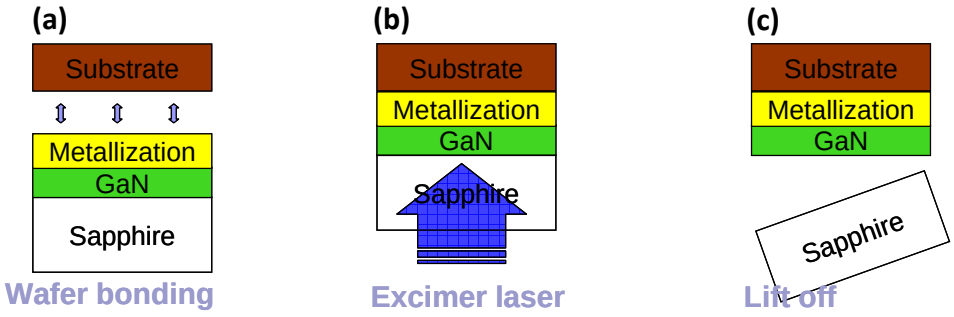


Figure 11. The procedure of LLO technique. (a) Depositing a high-reflectivity metal contact on to the p-side of GaN epi-wafer and bonding this structure to the other substrate, usually p-doped Si for VTF or intermediate substrate for TFFC. (b) Exposure to excimer laser and breaking the bonding between the sapphire and GaN. (c) Removing sapphire and adding n-contact. (removing intermediate substrate for TFFC)

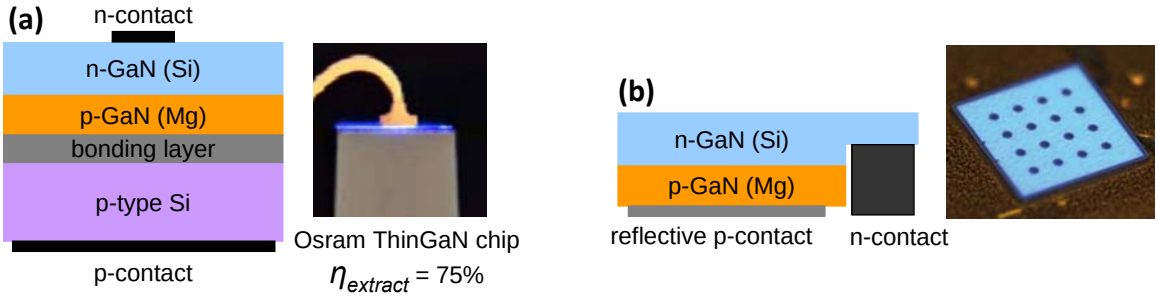


Figure 12. Illustrations and pictures of Thin-film LED by LLO technique. (a) ThinGaN of VTF structure with Si substrate, ThinGaN by Osram [4], and (b) TFFC structure, TFFC by Philips LUMILEDS [3]

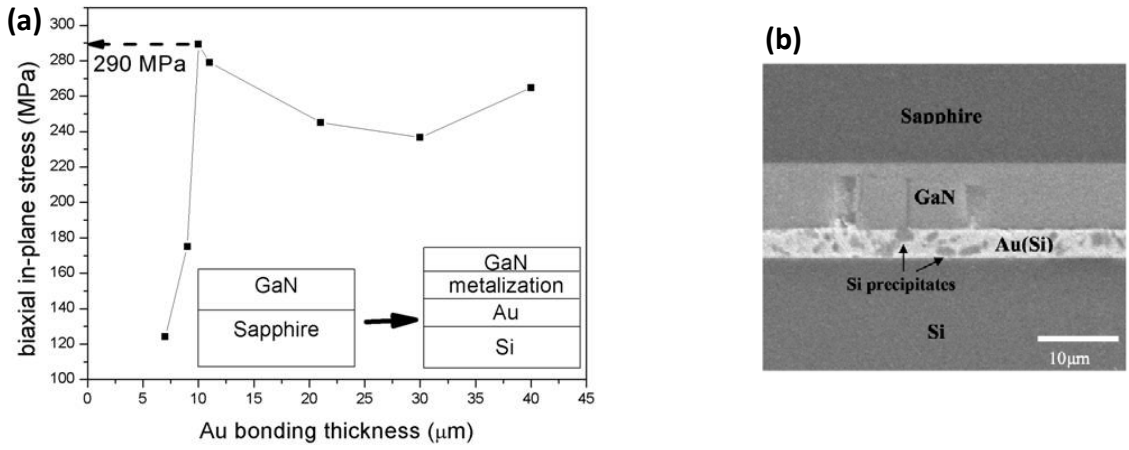


Figure 13. (a) The stress relaxation vs Au bonding layer thickness. The maximum compressive stress relief is observed to be around 290 MPa [18]. (b) SEM cross-sectional image of the Au–Si bonded interlayer [19].

Table 7. Material properties of GaN and substrates [20-22].

	Lattice constant (Å)	CTE (10^{-6} K^{-1})	Thermal conductivity (W/mK)
GaN (Wurtzite)	3.189 (a-axis)	5.59 (a-axis)	130
Sapphire	4.758	7.4	30
SiC (4H)	3.073	4.3	370
Si	-	2.6	124

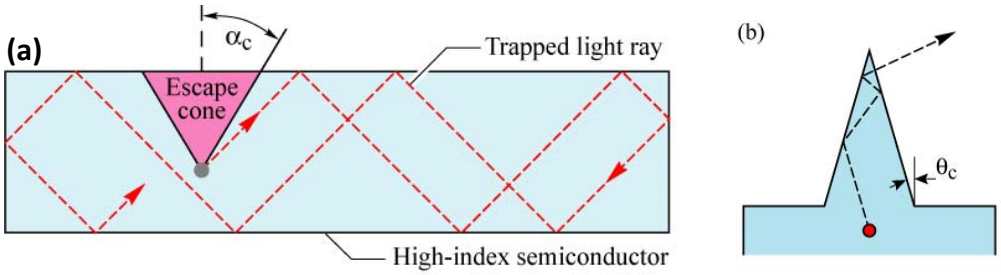


Figure 14. (a) "Trapped light" in smooth surface unable to escape for emission angles greater than α_c due to total internal reflection. (b) Increasing extraction efficiency with roughened surface [16]

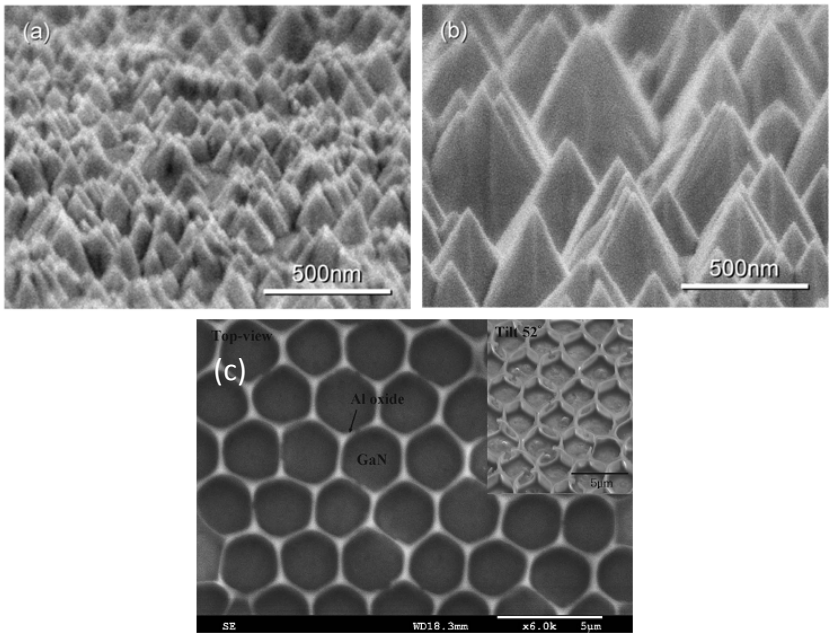


Figure 15. Increasing extraction efficiency by surface roughening and texturing. SEM micrographs of an n-face GaN surface etched by a KOH based PEC method (a) 2-min etching and (b)10-min etching [20], and (c) Al oxide honeycomb nanostructure [21]

The TFFC structure is more desirable than ThinGaN structure optically and thermally. Since the substrate is not used any more, it can eliminate the thermal resistance of the substrate and reduce the residual stress. Moreover, since any pattern and obstacles are not placed in the light emitting path, the efficiency is slightly increased; in case of ThinGaN structure, the patterned n-contact on the top of the device reduces its effective emitting area and the wire bonds obstruct light emission. However, the difficulty in dealing and packaging of TFFC should be solved to be more competitive.

The n-side up structure of ThinGaN and TFFC has another advantage besides eliminating current spreading layer on top of the device. Slightly larger extraction efficiency can be achieved by the n-side up structure due to the smaller refraction index of the n-GaN compared to the p-GaN—the refractive index of n-GaN and p-GaN are 2.42 and 2.45, respectively. Moreover, the thicker n-GaN layer, 2-3 μm, is better for the subsequent texturing process on the n-GaN surface, which enhances the extraction efficiency significantly (see Figure 14). The thickness of the p-GaN layer is only about a few hundred nanometers, so the roughening process can easily cause damage during the surface texturing process. There are many efforts to enhance extraction efficiency by texturing process, and it is reported that 35% of enhancement was achieved compared to bare surface LEDs (see Figure 15).

In sum, the extraction efficiency is significantly increased by employing ThinGaN and TFFC structure due to no current spreading layer, slightly small refraction index of n-GaN, and easiness of texturing thick n-GaN layer. Also, the high compressive residual stress in GaN layer is relieved as well. Moreover, ThinGaN and TFFC structure can achieve much lower thermal resistance than conventional structure by eliminating sapphire substrate, which has low thermal conductivity. The low thermal resistance makes it possible for the device to operate with high power input, more than 3W. The extraction efficiency with respect to the structure is shown in Figure 16. ThinGaN and

TFFC are the most promising structure for high power LEDs, and it has already been used for the state-of-the-art high power LEDs.

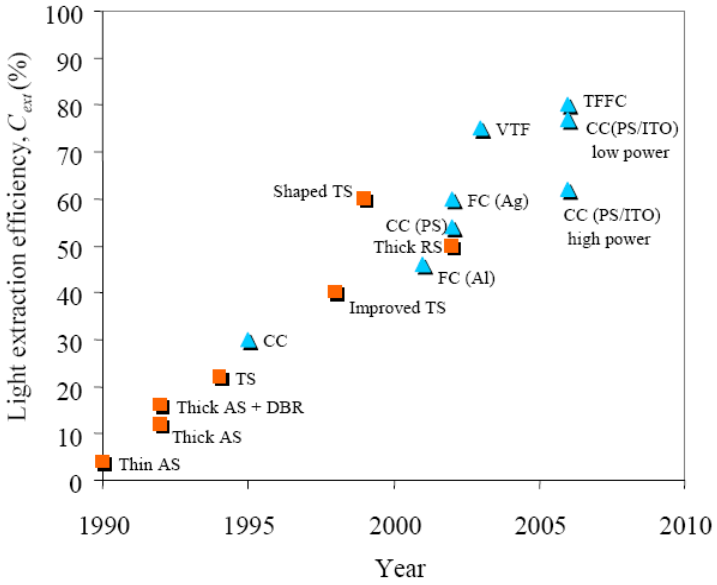


Figure 16. Extraction efficiencies for encapsulated AlGaInP (orange squares) and InGaN-GaN (blue triangles) LEDs. Conventional chip (CC), patterned substrate (PS), flip chip (FC), VTF, and TFFC are shown [22].

2.3 LED Array for General Light Source

As mentioned previously, although LEDs have high luminous efficiency, since the luminous flux from single LED is very small, the array of LEDs is required to compete with other general light sources. The array of LEDs that is used for a general light source is also called the LED light engine. There are two methods to build up LED arrays. One is to arrange surface mount type (SMT) high power LED packages, also called high power LED module, on printed circuit board (PCB) and the other is to arrange LED-chips directly on PCB, which is called chip-on-board (COB) array (see Figure 17). In both cases, a power electronic substrate is used rather than general FR4 PCB.

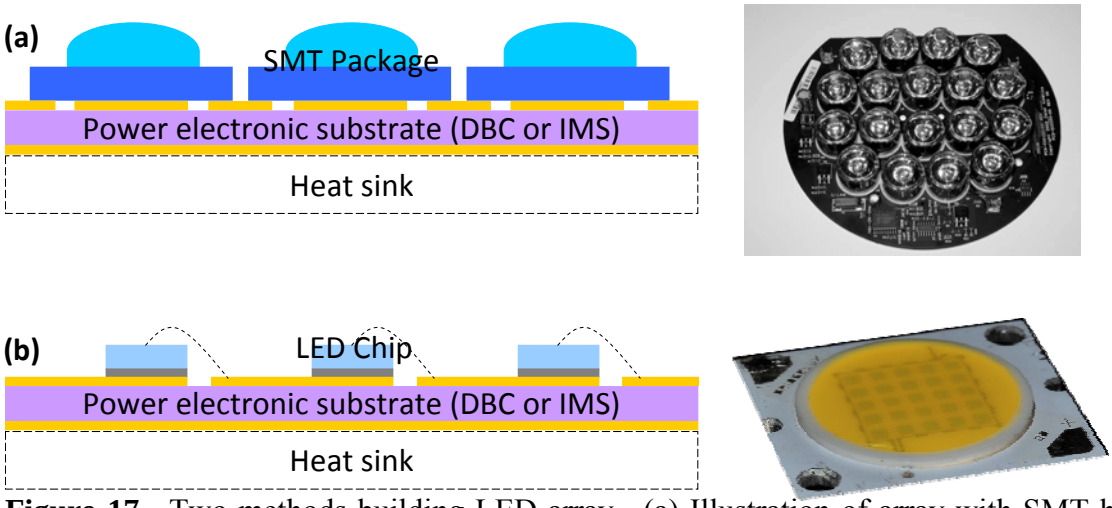


Figure 17. Two methods building LED array. (a) Illustration of array with SMT high power LED packages (left), Philips color kinetics DLE C-302 (right) and (b) Illustration of COB (left), BridgeLux BXRA-C2000 5×5 array (right)

2.3.1 Power Electronic Substrate

Like other electronic devices, LEDs need an electric circuit. Also, as we looked into previously, high power LED-chip such as VTF and TFFC should be placed on a circuit because the electrode is placed on the bottom of the chip or the chip and die structure. Therefore, the printed circuit board (PCB) is conducive for developing LED arrays. Typical FR4 PCB cannot be used because of its high thermal resistance. However, FR4 PCB can achieve low thermal resistance incorporated with a copper thermal via. For more thermal management, power electronic substrates can be used such as Direct Bonded Copper (DBC) substrate and Insulated Material Substrate (IMS) (see Figure 18).

IMS, also known as Metal Core PCB (MCPCB), is composed of a metal base-plate, a thin layer of dielectric, and a layer of copper. The dielectric is usually thin, about 100 μm, because it has poor thermal conductivity. A metal base-plate can be either copper or aluminum. In most applications, the base-plate is attached to a heat sink to

provide cooling, usually using thermal grease and screws. Compared to a classical printed circuit board, the IMS provides a better heat dissipation. It is one of the simplest ways to provide efficient cooling to surface mount type electronics. The technology of IMS resides in the dielectric layer; excellent electrical isolation properties and low thermal impedance. Bergquist Co. is one of the major manufacturers of IMS and the dielectric characteristic of its product is shown in Table 8.

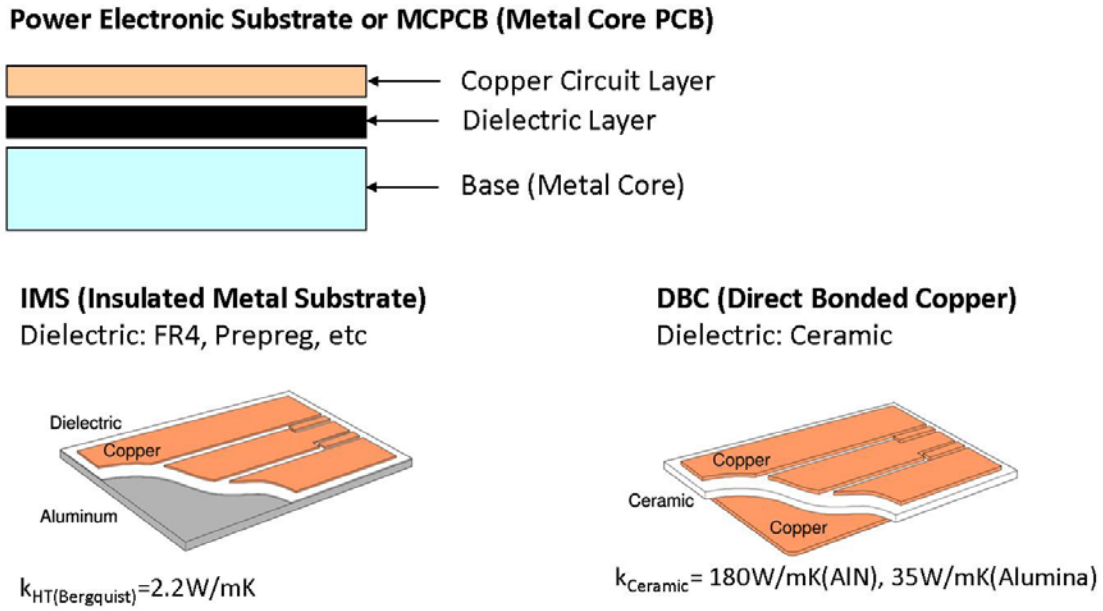


Figure 18. Structure of a direct bonded copper (DBC) substrate and an insulated metal substrate (IMS) [7].

DBC is composed of a ceramic tile (commonly alumina) with a sheet of copper bonded to one or both sides by high-temperature oxidation process that takes place around 1065°C [23]. Although a one side copper layer is possible, coating both sides of the ceramic is generally used to prevent failure by bending of ceramic due to CTE mismatch. The top copper layer can be chemically etched to form an electrical circuit, while the bottom copper is usually kept plain. There are three ceramic materials that generally used in DBC substrate; alumina (Al_2O_3), aluminum nitride (AlN), and beryllium oxide (BeO). Al_2O_3 is widely used because of its low costs, however it is not a

really good thermal conductor (30 W/mK). AlN is more expensive but it has far better thermal conductivity (180 W/mK). Although BeO has even higher thermal conductivity, it is often avoided because of its toxicity in powder form. Another advantage of the DBC substrate is their low CTE that is close to that of silicon, which guarantees good thermal cycling performances. Curamik is one of the major manufacturers of DBC substrate.

Table 8. Dielectric characteristic of Thermal Clad (Bergquist Co.) [24]

SINGLE LAYER		THERMAL PERFORMANCE			DIELECTRIC PERFORMANCE		OTHER		
Part Number	Thickness[1] [.000"/µm]	Impedance[2] [°C/W]	Impedance[3] [°C in²/W] / [°C cm²/W]	Conductivity[4] [W/m-K]	Breakdown[5] [kVAC]	Permittivity[6] [Dielectric Constant]	Glass Transition[7] [°C]	U.L. Index[8] [°C]	Peel Strength[9] [lb/in] / [N/mm]
HT-04503	3/76	0.45	0.05 / 0.32	2.2	6.0	7	150	140/140	6 / 1.1
HT-07006	6/152	0.70	0.11/ 0.71	2.2	11.0	7	150	140/140	6 / 1.1
MP-06503	3/76	0.65	0.09 / 0.58	1.3	8.5	6	90	130/140	9 / 1.6
MULTI-LAYER									
HT-09009	9/229	0.90	0.16 / 1.03	2.2	20.0	7	150	150/150	6 / 1.1
HT-07006	6/152	0.70	0.11/ 0.71	2.2	11.0	7	150	140/140	6 / 1.1
CML-11006*	6/152	1.10	0.21 / 1.35	1.1	10.0	7	90	130/130	10 / 1.8
HIGH POWER LIGHTING									
HPL-03015	1.5/38	0.30	0.02 / 0.13	3.0	2.5	6	185	**	5 / 0.9

Method Description
1 - Optical
2- Internal TO-220 test RD 2018
3 - Calculation from ASTM 5470
4 - Extended ASTM 5470
5 - ASTM D149
6 - ASTM D150
7 - Internal MDSC test RD 2014
8 - U.L. 746 E
9 - ASTM D2861
*CML is available in prepreg form
**Pending

Note: For applications with an expected voltage over 480 Volts AC, Bergquist recommends a dielectric thickness greater than 0.003" (76µm).
Note: Maximum test voltage is a function of material and circuit design. Typical proof test does not represent the maximum.
Note: Circuit design is the most important consideration for determining safety agency compliance.

2.3.2 Array of SMT High Power LEDs

SMT high power LEDs or high power LED modules are one of the main products of major LED companies. Since they are modularized, there are many applications such as back light unit (BLU) for LCD televisions as well as LED light engines. Before investigating the structure of COB LED package, it is needed to look into the structure of SMT high power LEDs. This is because the datasheets of SMT high power LEDs are revealed very well by the vendors and COB structure is also similar to SMT high power LEDs. Although there are several structures for single LED packages, SMT structure is mostly used for high power LEDs because it is the most suitable for heat dissipation.

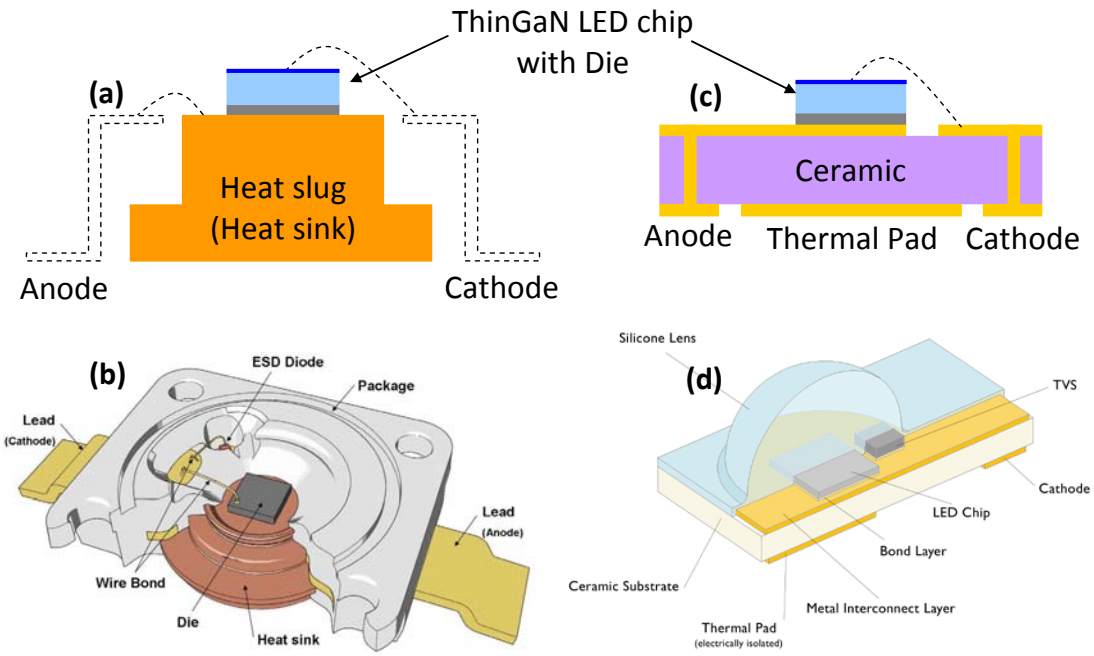


Figure 19. Illustrations of two types of SMT high power LED packages (a) LED-chip mounted on heat slug. (b) The structure of Dragon series that has heat slug, Osram opto semiconductors [4]. (c) LED-chip mounted on ceramic package with electrically isolated thermal pad. (d) LUXEON Rebel that is ceramic package, Philips Lumileds [3].

There are two package structures for SMT high power LEDs (see Figure 19). One is the structure that LED-chip is mounted on a heat slug and attached using die-attach material such as lead free solder. Copper and aluminum are usually used for the heat slug, therefore low thermal resistance can be achieved due to high thermal conductivity of the heat slug. However, since the heat slug is not isolated electrically, care is required when assembling packages to prevent shorting and electrical crosstalk. In addition, due to electrically non-isolated heat slug, thermal vias cannot be employed on the bottom of the heat slug. The LUXEON K2 series of Philips Lumileds and Dragon series of Osram opto semiconductors are heat slug type packages. The others involve packages that use ceramics as dielectric material. The anode and cathode are connected through electrical vias, and the thermal pad is electrically isolated. The ceramic package is easier to assemble into an array and it is possible to use thermal vias on the bottom of thermal pad. Also, the low thermal resistance can be achieved by using high thermal

conductivity ceramic such as AlN, 180 W/mK. LUXEON Rebel of Philips Lumileds and Xlamp series of Cree Inc. are ceramic type packages.

The efficiency, the chip structure, the package type, and the thermal resistance of state-of-the-art high-power LEDs are compared in Table 9. The efficiency is shown for white light LEDs operating at 350 mA. Generally, the efficiency decreases as forward current increases. The ceramic package shows slightly higher thermal resistance than the heat slug package. In this respect, the heat slug package is superior to the ceramic package. One of the most important features of the ceramic packages is their electrically neutral thermal path. This feature allows array to build by using FR4 PCB with thermal vias, which is 8 to 10 times less expensive than IMS. However, IMS generally shows better heat dissipation compared to FR4 PCB with thermal vias.

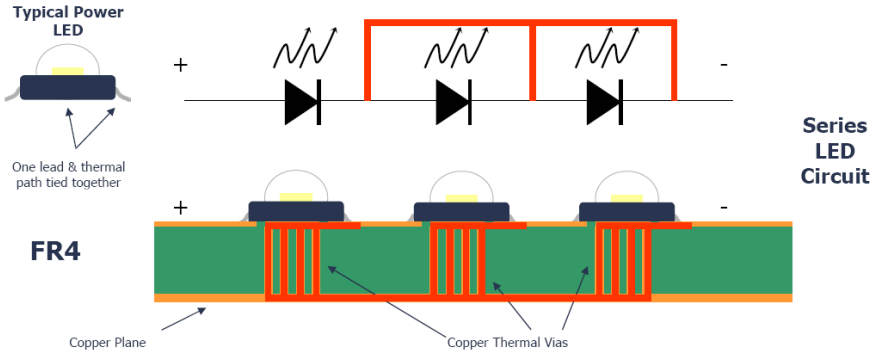


Figure 20. The heat slug type package on FR4 PCB with thermal via will cause a short between LEDs [5].

Figure 21. The heat slug package cannot be directly placed on a heat sink because the heat slug is not electrically isolated. IMS (MCPCB) makes the heat slug to be isolated and helps heat dissipation. The package shown in figure is LUXEON K2 Warm-White LEDs and Star Aluminum MCPCB [3].

Table 9. Comparison among SMT high power LED packages. The efficiency of ultra white or white light is used at 350 mA. The efficiencies with parentheses are estimated from data sheets. The chip structure of Xlamp is presumed as ThinGaN structure. Thermal resistance is that between the junction and solder point.

	Model	Efficiency (lm/W)	Chip Structure	Package Type	R_{th} (°C/W)
Philips Lumileds	LUXEON Rebel	(90.7)	TFFC	Ceramic	10
	LUXEON K2 TFFC	(90.9)	TFFC	Heat slug	5.5
Osram Opto Semicondutors	Golden Dragon Plus	93	ThinGaN	Heat slug	6.5
	Diamond Dragon	65	ThinGaN	Heat slug	2.5-5
Cree Inc.	Xlamp XR-E	(92.6)	(ThinGaN)	Ceramic	8

2.3.3 COB Array

In COB technology, LED-chips are bonded to a substrate that can be directly packaged on a heat sink or any kind of cooling unit. Although it is not as common as array of SMT packages, several LED lamps based on COB technology are available (see Figure 22). COB arrays have many advantages compared to the array of SMT high power LEDs. First of all, it is cost effective by reducing the number of assembly parts and the overall manufacturing processes. Secondly, high packaging density is possible. Due to their overall size, arrays of SMT packages do not allow for high packaging densities, which results in a restriction of the radiant flux output per unit area. COB arrays offer the high packaging density that is mandatory for space savings or highest luminance. Thirdly, high precision chip placement and color mixing is possible. Fourthly, better thermal management can be expected with COB technology. By using COB technology, it is possible to eliminate several layers such as one solder layer and the SMT substrate which may cause higher junction temperatures. The low junction temperature allows higher efficiencies and longer lifetimes. Therefore, COB arrays are

more suitable for general light sources and will be used more widely. Although their design specification is not very revealing, the structure of the COB array can be easily assumed. A copper circuit layer is required on the top of the substrate to make LEDs into an array without complex wire bonding. Also, a dielectric layer is required for each LED-chip to be electrically isolated. The most important thing is having a high thermal conductivity of substrate. Power electronic substrates meet these qualifications well. In this respect, COB arrays with DBC substrates have a lot of similarities with ceramic SMT high power packages. Therefore, the thermal analysis of COB can be started with the analysis of SMT high power packages. And then it can be extended to COB array by superposition of thermal analysis of each component.

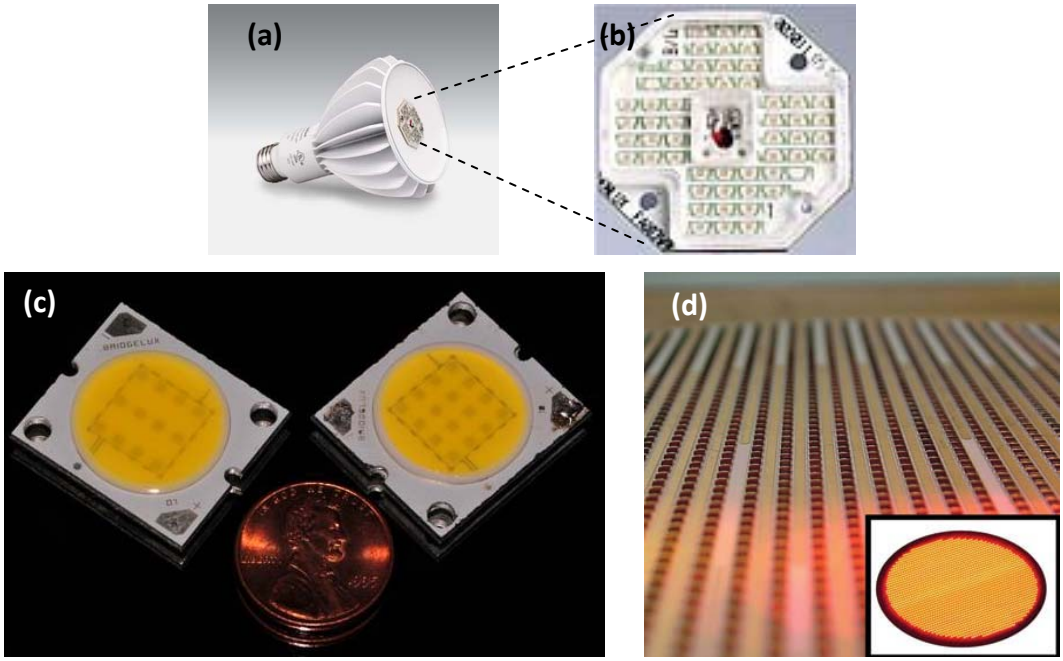


Figure 22. (a) LED lamp with COB technology, enLux R-30 series, enLux Lighting. (b) enLux light engine that employ COB technology [25]. (c) BridgeLux BXRA-C0800 with 3×4 array and BXRA-C2000 5×5 array [26]. (d) The "3 kW-LED" high power COB array, with nearly 2000 1 mm^2 chips, produced by PerkinElmer Elcos [27].

2.4 Current Thermal Management of LED Packages

There are three major things that affect the junction temperature of an LED; forward current or input power, thermal path, and ambient temperature. The higher power input, the greater the heat generated at the die. Heat must be removed from the die in order to maintain expected light output, life, and color. The amount of heat that can be removed depends upon the ambient temperature and the design of the thermal path from the die to the surroundings. The thermal dissipation path of LEDs is different from other power electronic device counterparts.

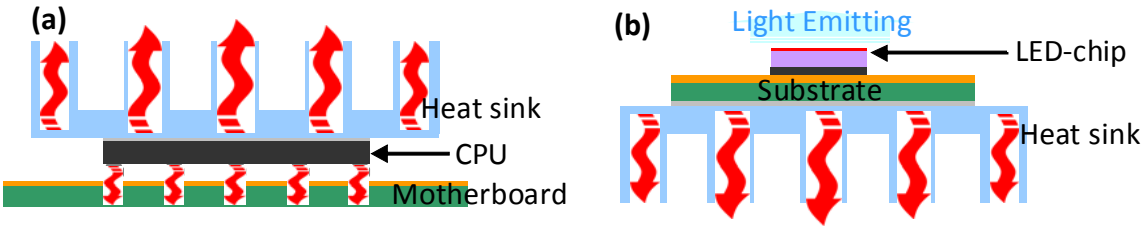


Figure 23. Schematic of thermal path of (a) general power electronics, (b) LED package

In the case of other high power electronic device such as CPUs, heat can dissipate along two different paths; one is through the board and the other is through the heat sink that is directly attached on the chip, as shown in Figure 23 (a). In this case most of heat dissipates through heat sink because the contact resistance between chip and board is very large. In case of an LED package, however, the heat sink cannot be directly placed on the chip because it will block the path for light emission. Heat should dissipate through only one side and there are many layers between a heat source and a heat sink. Moreover, while the typical heat flux of a CPU is less than 100 W/cm^2, that of an LED is up to 500 W/cm^2 or more. Therefore, the study of the thermal dissipation path is very important. Currently, the study of thermal management of LED packages are generally provided by LED companies [28-30]. Here, they only provide thermal resistance of SMT

high power LED packages from their datasheets but do not show the chip level thermal management. Also, they simply introduce thermal management of LED arrays using a thermal resistance model, but not provide enough guidance for the thermal management of LED arrays. Most of the thermal management resources provided by vendors employ thermal resistance models, which are very useful to simplify the system and to predict the junction temperature. Therefore, we need to look into the definition of thermal resistance models, and look at how to use resistance models in both single chip model and multi chip arrays. Thermal resistance models from many resources are very similar, therefore the definition and explanation based on "Thermal Design Using LUXEON Power Light Sources" [28] will be discussed here.

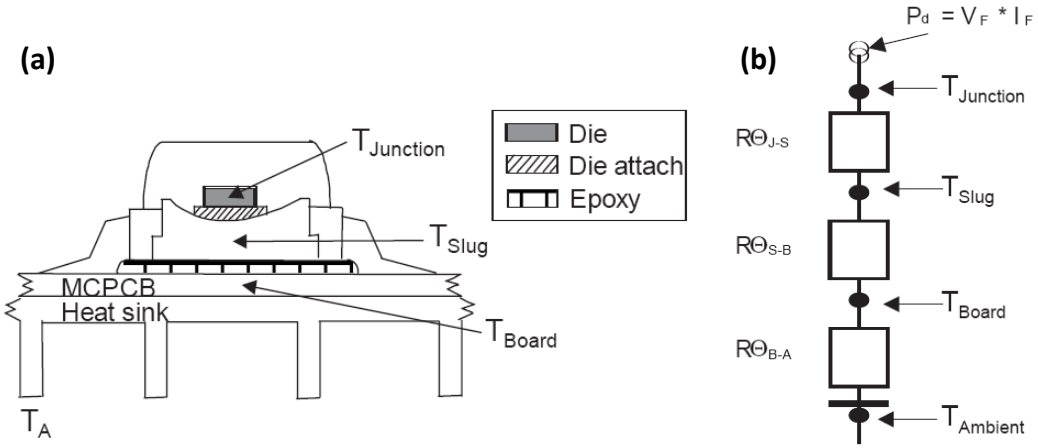


Figure 24. (a) The schematic of SMT high power LED package, (b) simplified thermal circuit model [28]

First of all, thermal resistance is defined as follows;

$$R_{\theta,Junction-Ambient} = \frac{\Delta T_{Junction-Ambient}}{P_d} \tag{2.2}$$

where, $\Delta T_{Junction\text{-}Ambient} = T_{Junction} - T_{Ambient}$ (°C), P_d = Power dissipated (W) = Forward current (I_f) × Forward voltage (V_f). For the entire systems, it can be simplified a series of thermal resistance circuits, as shown in Figure 24. The overall thermal resistance of the system can be expressed as the sum of the individual resistances as shown in Equation 2.3.

$$R_{\theta,Junction-Ambient} = R_{\theta,Junction-Slug} + R_{\theta,Slug-Board} + R_{\theta,Board-Ambient} \quad (2.3)$$

where, $R_{\Theta,\ Junctioin\text{-}Slug\ (J\text{-}S)}$ is R_Θ of the die attach combined with die and slug material in contact with the die attach. $R_{\Theta,\ Slug\text{-}Board\ (S\text{-}B)}$ is R_Θ of the epoxy combined with slug and board materials in contact with the epoxy. $R_{\Theta,\ Board\text{-}Ambient\ (B\text{-}A)}$ is the combined R_Θ of the surface contact or adhesive between the heat sink and the board and the heat sink into ambient air. Once the thermal resistance of the system is determined by experiment or simulation, Equation 2.4, which is derived from Equation 2.2, can be used to calculate the junction temperature of the system.

$$T_{Junction} = T_{Ambient} + P_d \times R_{\theta,Junction-Ambient} \quad (2.4)$$

Thermal resistance of a multi-chip LED array can be determined using the parallel thermal resistance model as shown in Figure 25. In this model, each LED is represented by individual, parallel thermal resistances. The $R_{\Theta,\ J\text{-}B}$ of the multi-chip LED array is obtained by using the parallel resistance equation, as shown in Equation 2.5a. If we assume that all LEDs in the array are identical, the equation simplifies to Equation 2.5b.

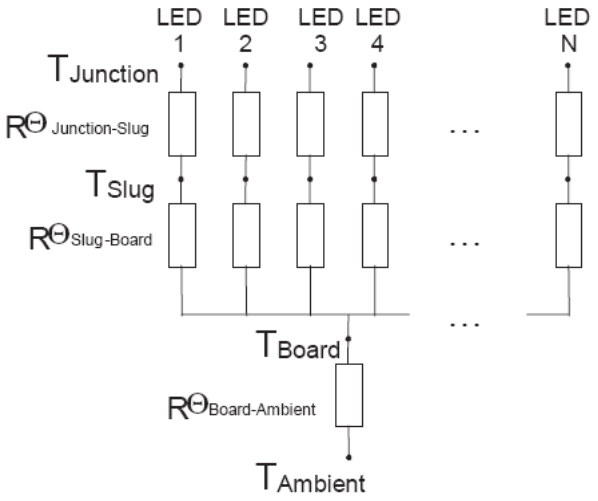


Figure 25. Parallel thermal resistance model of multiple LED array [28].

$$\frac{1}{\left(R_{\theta,Junction-Board}\right)_{Total\_Array}} = \frac{1}{\left(R_{\theta,Junction-Board}\right)_{LED\_1}} + \ldots + \frac{1}{\left(R_{\theta,Junction-Board}\right)_{LED\_N}} \tag{2.5a}$$

$$\left(R_{\theta,Junction-Board}\right)_{Total\_Array} = \frac{R_{\theta,Junction-Board}}{N} \tag{2.5b}$$

By using a thermal resistance model, once the thermal resistance of each component is determined, the junction temperature of the multi-chip LED array can be determined easily. However, the problem of this thermal resistance model does not include heat spreading effects in substrates (or boards) and heat sinks, which are very important in thermal management of LED arrays. Although there are several studies on the thermal management of multi-chip LED arrays [31, 32], since they used specific designs and conditions, they do not give generalized guidance for arbitrary array design. One of thermal design guidelines is shown in Figure 26, which was done by Christensen et al. [32]. It shows the maximum available power per LED for various packing densities with specific heat sink.

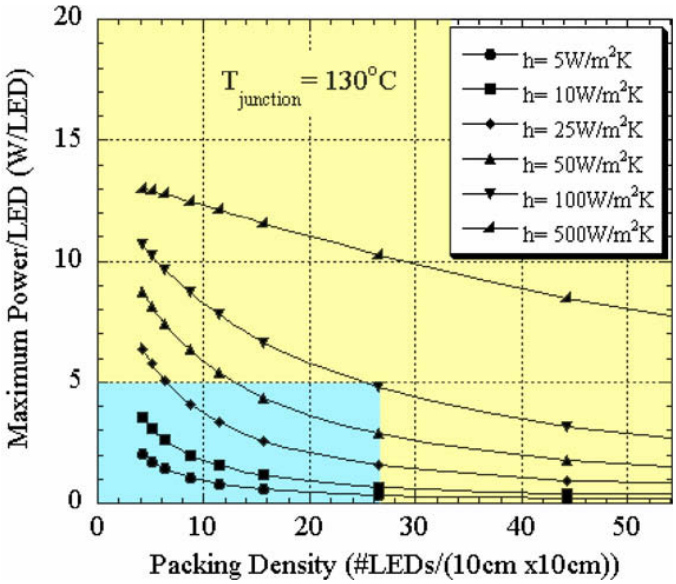


Figure 26. Maximum power dissipated for a junction temperature of 130°C for various packing densities of high power LED components on a square flat plate heat sink under different convection conditions. The blue region is considered to be obtainable with current technologies, while the yellow region presents new challenges for efficient heat removal [32].

CHAPTER 3

FINITE ELEMENT ANALYSIS OF SINGLE CHIP LED PACKAGE

3.1 Motivation

The purpose of this chapter is to outline a simple methodology to analyze the performance of heat dissipation from single chip LED packages. Since analyzing multi chip LED arrays would be complicate, we start from single chip packages and extend the result to the arrays. In this work high power LED-chips (>1W/die) implementing COB architectures were designed and studied (see Figure 27).

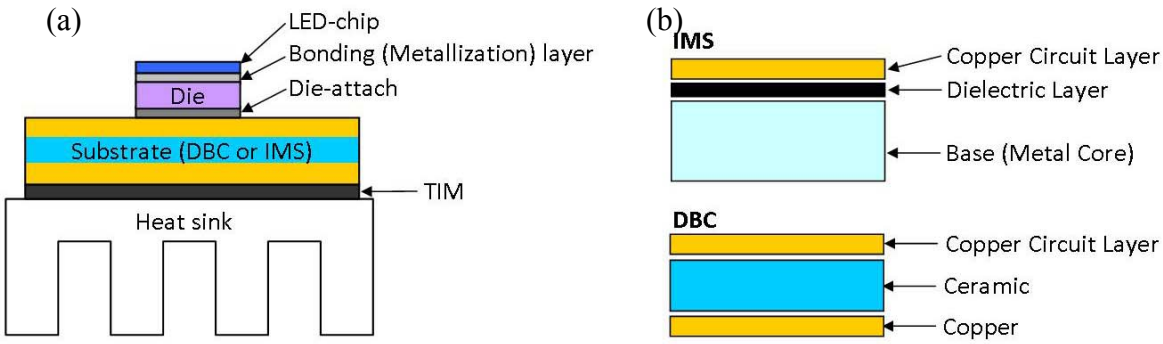


Figure 27. (a) The structure of the simplified LED package and (b) the structures of IMS and DBC substrate.

The LED-chip has VTF structure, which is the most promising chip structure for the high power LEDs together with the TFFC structure. We assume that the LED-chip is GaN and the dimensions are 1mm by 1mm and 4 μm thick. Also, we assume uniform heat generation in the volume of the chip. The chip is mounted on a Si die and attached using a eutectic bonding such as Au-Si. The chip and the bonding (or metallization) layer are so thin that they are not modeled—the impact of neglecting GaN layer will be shown. In this case the heat generation in the chip can be substituted by a uniform heat flux on

the top surface of the die. The Si die is placed on a power electronic substrate, DBC or IMS, and attached using lead-free solders. This structure can be regarded as a single-chip LED package with ceramic substrate or a part of LED arrays implementing COB architecture (see Figure 28).

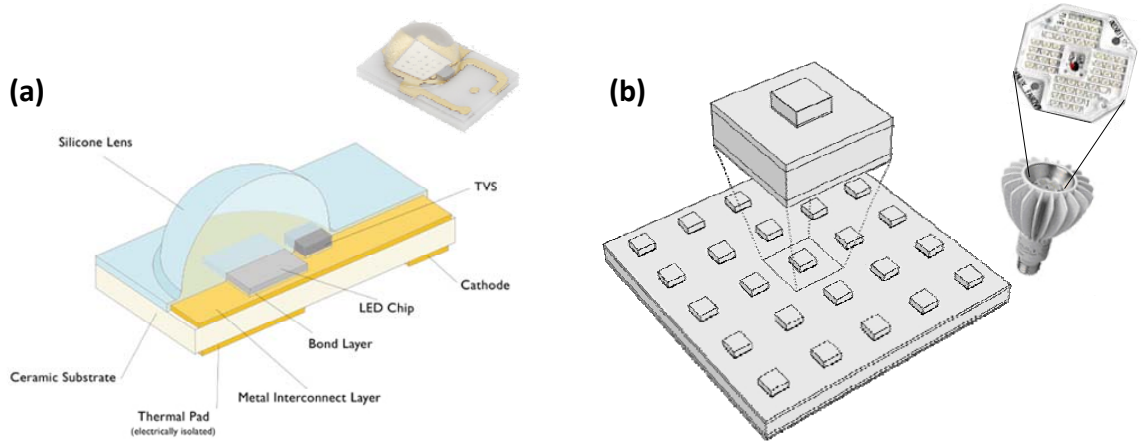


Figure 28. (a) LUXEON Rebel of Philips Lumileds [3], which has similar to single chip-LED on DBC substrate. (b) The schematic of the array implementing COB architecture and LED bulb of enLux Lighting [25]. The simplified model used in this study can be regarded as single chip-LED or a part of LED arrays implementing COB architecture.

3.1.1 Modeling

The materials, dimensions, and thermal conductivities of materials are summarized in Table 10. We assumed that materials are homogeneous and isotropic, and their thermal conductivities are independent of temperature. The simplified heat sink design is shown in Figure 29 that based on LPD19-3B of Alpha Novatech, Inc, which is a commercially available heat sink for natural convection. The effect of heat sink design will be considered later. Boundary conditions are shown in Figure 30. All surfaces around the die and substrate are adiabatic except the top of the die. This assumption is reasonable because most of the heat generated in LEDs is dissipated by conduction. The heat dissipation by convection around the die and substrate is negligible because they are placed inside the package, which usually has very low thermal conductivity. The general

heat dissipation by conduction in LED package is known as more than 90%. The heat that passes through the LED package structure is dissipated through heat sink. We assume the free convection around heat sink and apply a uniform convective heat transfer coefficient, h=10 W/m^{2}K, at 25°C ambient temperature (see Table 11).

Table 10. Details of structural dimensions and thermal conductivities at 25°C [33].

	Thickness	Size	Materials		Thermal conductivity (W/m^{2}K)
LED-chip	4 μm	1mm × 1mm	GaN		130
Metallization	10 μm	"	Au-Si eutectic bonding		27
Die	375 μm	"	Si		124
Die-attach	50 μm	"	Lead free solder	100In	82
				Au-20Sn	57
				Sn-3.5Ag	33
Substrate	-	1cm × 1cm	Copper		385
			DBC	AlN	180
				Al_2O_3	30
			IMS	Dielectric	1.1
				Al	150
TIM	50 μm	"	Thermal grease		3
Heat sink	-	-	Al		150

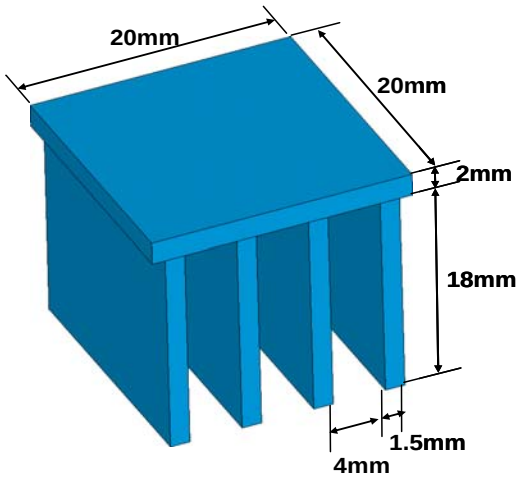


Figure 29. The structure and dimensions of the heat sink

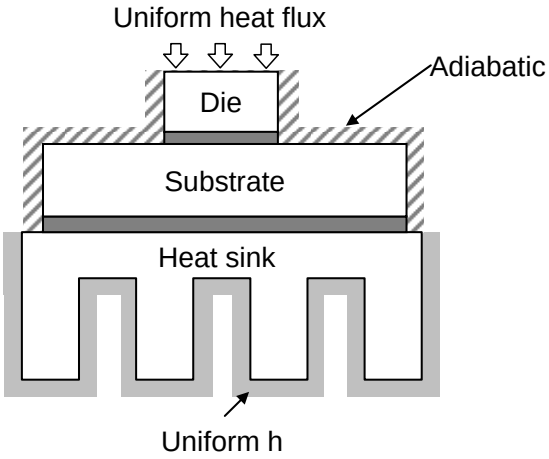


Figure 30. Boundary conditions used in this study; Uniform heat flux on top of the die, uniform convection heat transfer coefficient around heat sink, and all other surfaces adiabatic.

Table 11. Typical values of the convection heat transfer coefficient [34]

Process	h (W/m^2K)
Free convection	
Gases	2-25
Liquids	50-1000
Forced convection	
Gases	25-250
Liquids	100-20,000
Convection with phase change	
Boiling or condensation	2500-100,000

In this study we focus more on how to reduce thermal resistance inside package rather than how to increase convection around heat sink. Thus using a uniform convection heat transfer coefficient is a good assumption to simplify the problems. The heat generation in LED-chips can be substituted for the heat flux on the top surface of the die because the LED-chip and the metallization layer are very thin. Typical forward current of a high power white LED currently available is from 330 mA to 350 mA with the driving voltage being from 3.3 V to 3.4 V. This means that the operating power is around 1.1 W to 1.2 W. If we assume that a LED has 100 lm/W of luminous efficacy,

which is 15% of the luminous efficiency, the heat generation is 0.9 W to 1 W. Therefore, the simulation using 1 W of the heat flux on the top of the die is consistent with currently available LEDs with typical power input. Also, the higher power LED package can be simulated by applying a larger heat flux.

3.1.2 ANSYS Modeling

To study the thermal performance of an LED package, an ANSYS simulation was utilized. The finite element mesh of the typical design used in this study is shown in Figure 31. Only ¼ of the problem was modeled due to symmetry. Although the accuracy of the solution can be improved with a fine mesh, using a large number of elements is limited by system memory and simulation time. Instead of using a fine mesh in the entire model, we can improve the accuracy by using a fine mesh only over the interested region. Therefore, the top of the die was meshed finely for this study as shown in Figure 31 (b). The boundary condition of the symmetric surfaces is adiabatic for the thermal analysis. One of the FEA results is shown in Figure 32 with the simulation conditions.

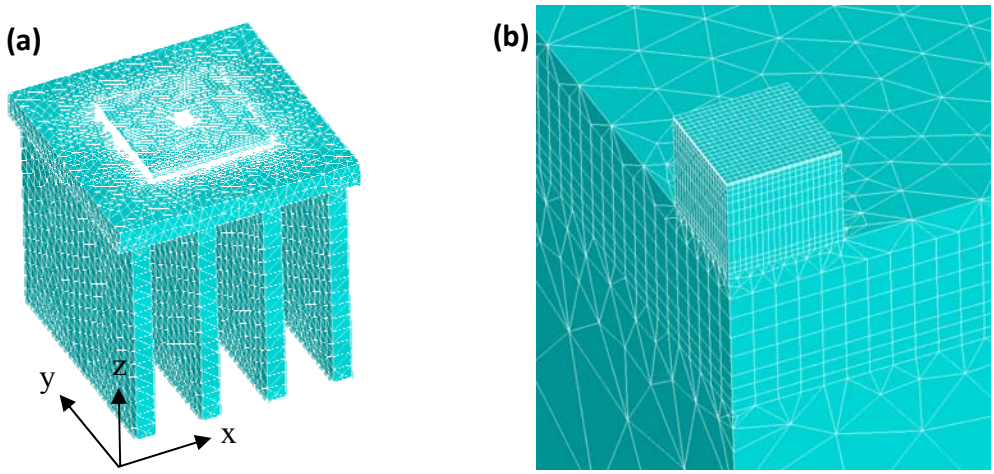
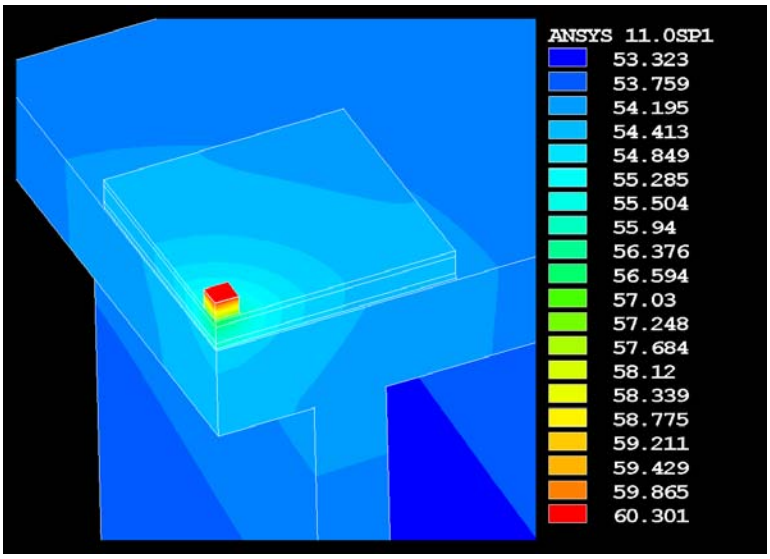


Figure 31. (a) Finite element mesh for a single LED package with a heat sink. The coordinate axes are indicated by the arrows. (b) Only ¼ of the problem is used due to symmetry. The interested region, the top of the die, is meshed very finely.



LED-chip (GaN)
4µm, *k*=130W/mK
Metallization (Au)
10µm, *k*=301W/mK
Die (Si)
375µm, *k*=127W/mK
Die-attach (Au-20Sn)
50µm, *k*=57W/mK
Substrate (DBC)
Cu 127µm, *k*=385W/mK
AlN 381µm, *k*=180W/mK
TIM
50 µm, *k*=3W/mK

1W Heat Generation
h=10 W/m²K, T_∞=25 °C

Figure 32. The contour plot of temperature distribution in LED package. The simulation conditions are shown in the right.

3.1.3 Impact of Neglecting the GaN Layer in the Thermal Model

Since the LED-chip and its metallization are very thin, meshing such aspect ratios becomes difficult. Thus, we assume that the effect of LED-chip on the junction temperature is negligible. By this assumption, we can conduct simulations without modeling structural details of the LED-chip and reduce the difficulties in meshing. The heat generation in LED-chip can be approximated by a uniform heat flux on the top of the die when the chip is not modeled. To validate this assumption, simulations with and without the LED-chip details were conducted and compared (see Figure 33). The junction temperatures were 60.30°C and 60.26°C respectively, and the difference was only 0.04°C, which is negligible. Therefore, the assumption of the use of the uniform heat flux was seen as been sufficient, and the LED-chip will not be modeled in further simulations.

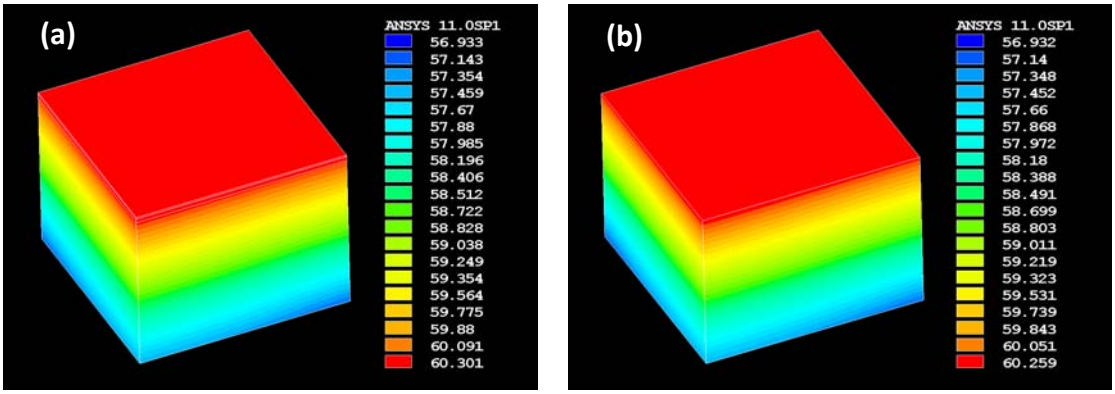


Figure 33. (a) The contour plot of temperature distribution in LED-chip and die. The LED-chip and metallization layer were modeled. (b) The contour plot of temperature distribution in die. Only die was modeled. The conditions Figure 32 were used.

3.1.4 Mesh Convergence

While a fine mesh can improve the accuracy of the simulation, it increases the simulation time and the memory used. Contrarily, a coarse mesh can shorten the simulation time and reduce the memory used, albeit, a tradeoff in reduced accuracy is obtained. Therefore, we need to determine the proper mesh size that guarantees the accuracy of the simulation through a mesh convergence analysis.

There are two element types generally used in a 3D thermal analysis in ANSYS—solid-70 and solid-90 (see Figure 34). Solid-70 is the hexahedron element which has 8-nodes on each vertex, and the behavior of each edge is linear. Solid-90 has nodes in the middle of edges and on vertexes, therefore it has 20 nodes total. Since each edge of solid-90 element behaves as a spline function, it is more suitable for complex simulations. The mesh convergence was examined using solid-70 and solid-90 elements, respectively, and plots of the junction temperature as a function of the number of nodes are shown in Figure 35. In the case of solid-90 elements, the junction temperature converges to 60.26°C. When using solid-70 elements, the temperature is still increasing even after 5×10^5 of nodes. Overall, the difference between the junction temperatures is

only 0.01°C. Therefore, the models having 2×10^4 to 3×10^4 nodes with solid-90 element were used for further simulations.

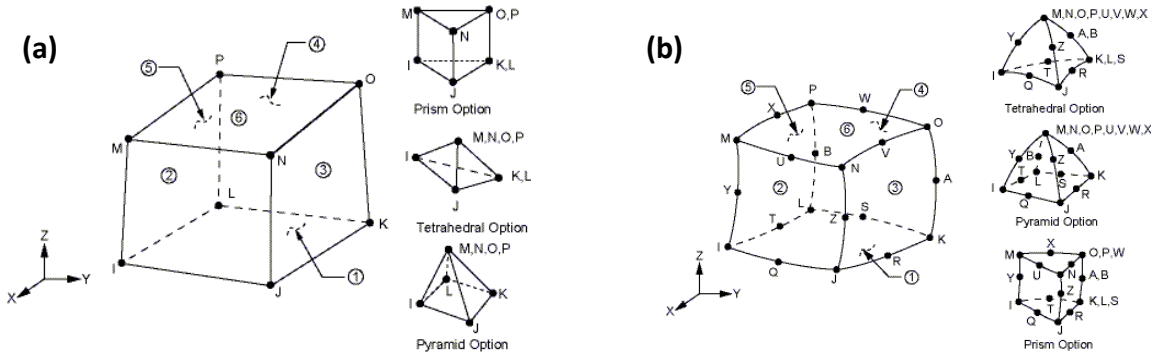


Figure 34. (a) Solid-70 element, (b) Solid-90 element [35]

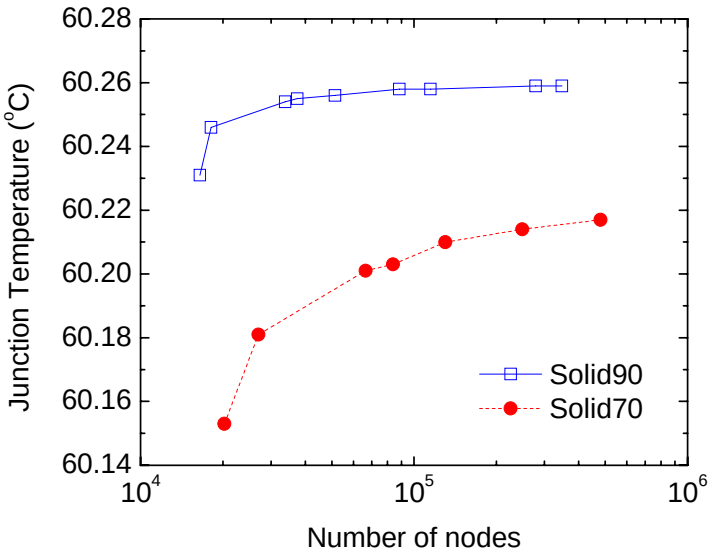


Figure 35. The examination of the mesh convergence using solid-90 and solid-70 element.

3.2 Vertical Temperature Profile & Thermal Resistance Analysis

3.2.1 Vertical Temperature Profile

To assess the thermal management of our system, we need to analyze thermal characteristics of the system. The vertical profiles of temperature and heat flux along the center line give very good insight into the thermal resistance of the system. Also, using the temperature profile, we can estimate the thermal resistance of each layer and the change in thermal resistance with the change of design. The vertical profiles of temperature and heat flux along the center line was investigated through the use of conduction thermal resistances (see Figure 36). The one-dimensional form of Fourier's law and thermal resistance, R_{th}, are shown in Equation 4.1, which is used for many simple applications.

$$q'' = \frac{Q}{A} = -k\frac{\Delta T}{L} \tag{4.1a}$$

$$R_{th} \equiv \frac{-\Delta T}{Q} = \frac{L}{kA} \tag{4.1b}$$

where, q'' is the local heat flux (W/m^2), Q is total heat load (W), A is heat flux area (m^2), k is the thermal conductivity (W/mK), ΔT is the temperature difference between two surfaces (°C), and L is the distance between two surfaces (m). From Equation 4.1 assuming a 1 W/m^2 heat flux, the temperature difference between two points directly gives the area dependent thermal resistance between two points. Also, the gradient of the vertical temperature profile, which is determined by the thermal conductivity and the heat flux area, can be considered as the thermal resistance per unit length.

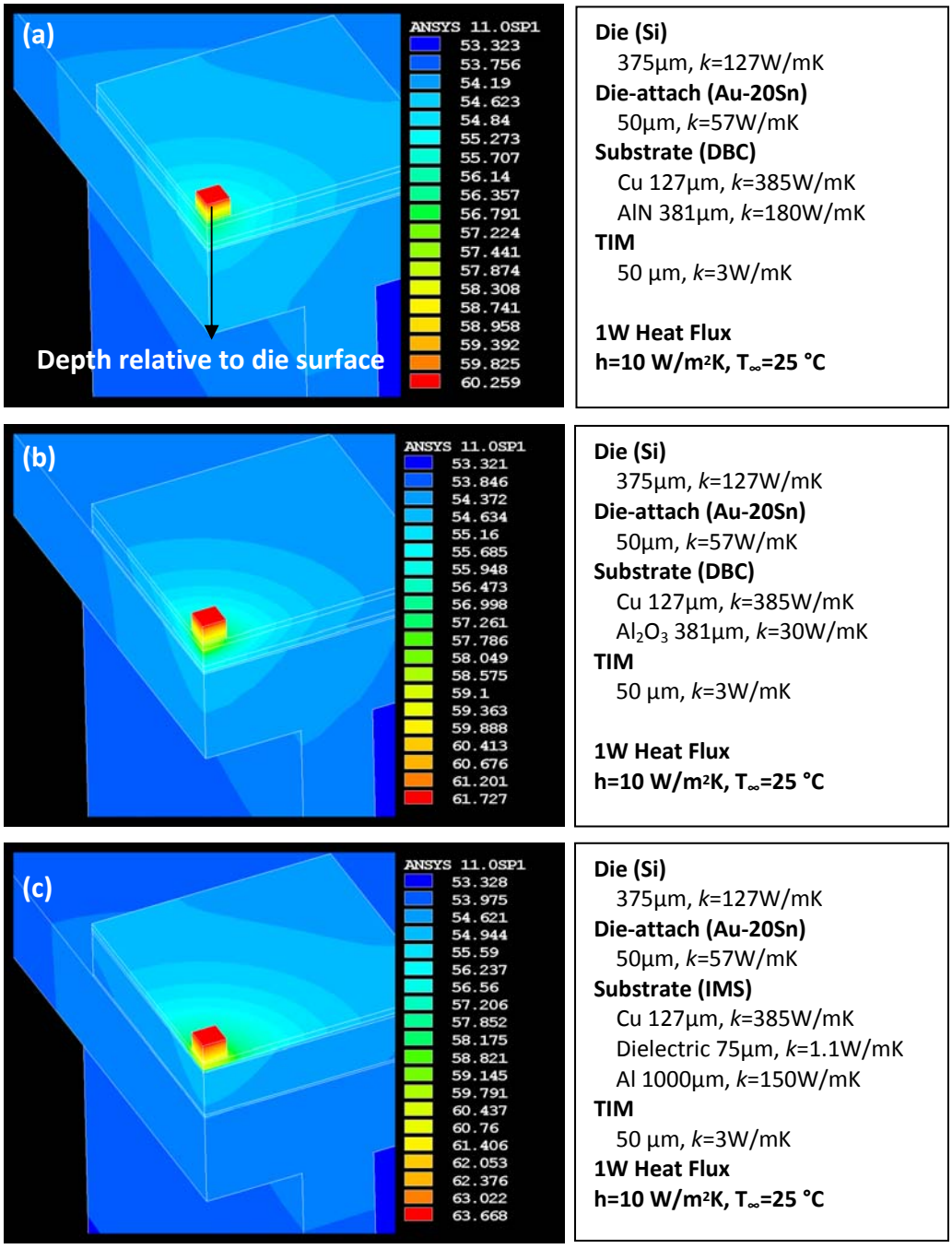
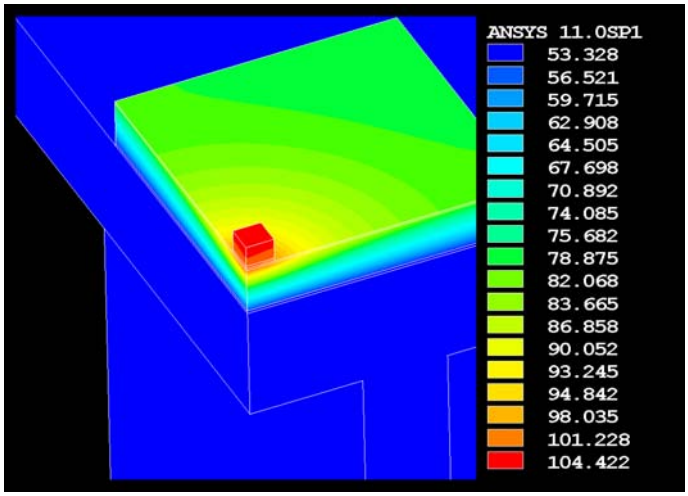


Figure 36. The contour plots of temperature distribution of LED package using power electronic substrate. (a) AlN DBC substrate, (b) Al_2O_3 DBC substrate, and (c) IMS. The simulation condition of each result is shown in the right side.



Die (Si)
375µm, *k*=127W/mK
Die-attach (Au-20Sn)
50µm, *k*=57W/mK
Substrate (FR4)
Cu 35µm, *k*=385W/mK
FR4 800µm, *kx*&*ky*=0.8W/mK
kz=0.3W/mK
TIM
50 µm, *k*=3W/mK

1W Heat Flux
h=10 W/m²K, T_∞=25 °C

Figure 37. The contour plot of the temperature distribution in LED package with FR4 PCB and its simulation conditions.

The vertical profiles of temperature and heat flux along the center line are shown in Figure 38. The temperature difference between the top and bottom of each layer becomes the thermal resistance of each layer. The thermal resistance of the package without a heat sink is 5.7°C/W, which is much smaller than that of the heat sink, 29.57°C/W. This is because a DBC substrate with good thermal performance was used for the package while a relatively small size for the heat sink was simulated. In other words, there is room to optimize the performance of the heat sink, but this is outside of the focus of this study. For the purpose of comparison, a simulation was conducted using the package with a standard PCB substrate, and the result is shown in Figure 37. With a standard PCB, the thermal resistances of the package and the heat sink are 50.13°C/W and 29.29°C/W, respectively. This simulation clearly shows the reason why power electronic substrates should be used for LED packages. The gradient of the vertical temperature profile is large in the die, the die-attach, and TIM. The gradient of the die-attach and TIM is large because of their low thermal conductivities, while the gradient of the Si die is large because of the large heat flux (100 W/cm^2 for a 1 mm^2 die dissipating 1 W). For layers that have large temperature gradients, they should be made as thin as possible to reduce the thermal resistance of the system. The vertical profile of the heat

flux along the center line is also shown in Figure 38. The heat flux along the center line in the die, the die-attach, and the TIM barely changes, which indicates that little or no heat spreading has occurred. On the contrary, the heat flux along the center line in substrate changes a lot, which indicates large heat spreading. The reduction of the heat flux also makes the thermal resistance of the TIM small despite its very low thermal conductivity, 3 W/mK.

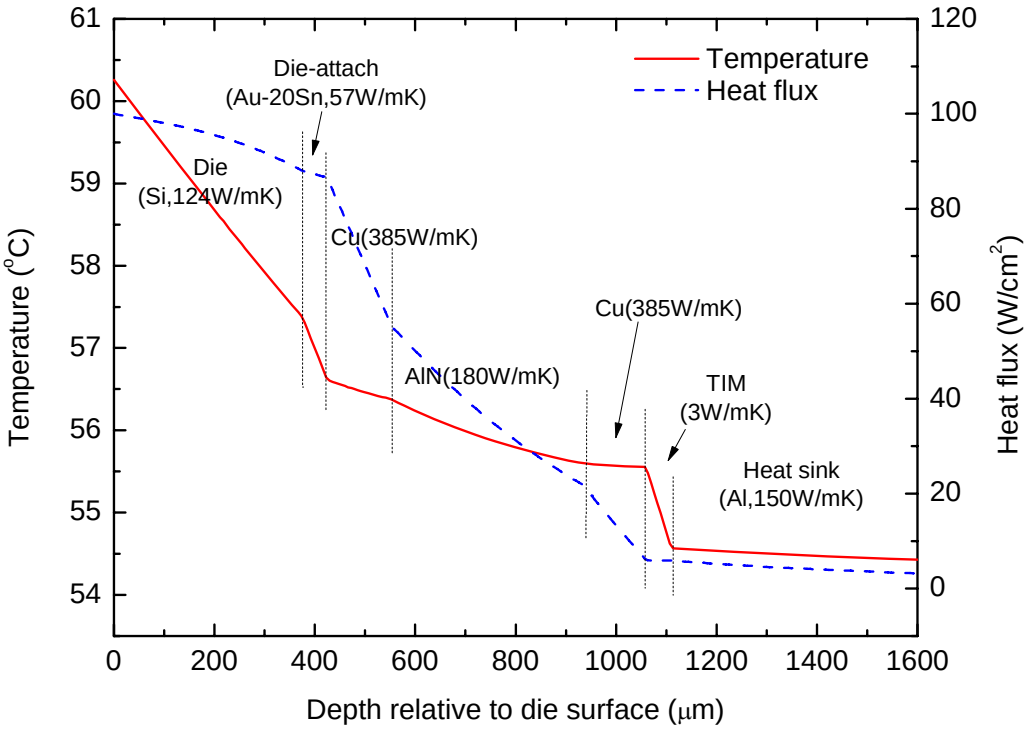


Figure 38. Vertical (z-axis) temperature and heat flux profile along the center line. The result of simulation shown in Figure 36(a) was used.

To investigate the thermal characteristic with respect to different substrates, the vertical temperature profiles of the packages, which use Al_2O_3-DBC substrate and a dielectric-IMS structure, were also plotted, and compared with that of an AlN-DBC substrate (see Figure 40). The same design and conditions were used for these simulations, with only changes in the dielectric material and overall substrate thickness. The same thickness of the copper layer in the substrate, 127 μm, was used. Since the

same geometry and materials were used in the die and the die-attach, the slopes of three simulations are almost same in the die and die-attach.

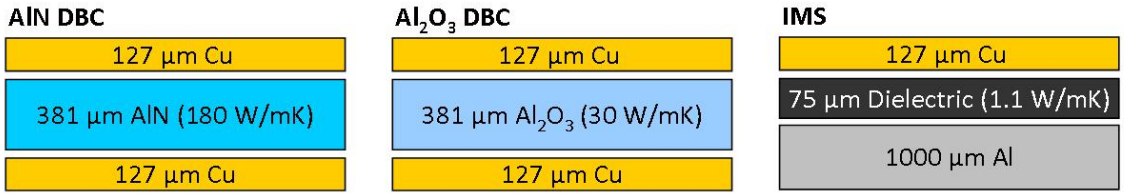


Figure 39. The specifications of the substrate used in the simulations shown in Figure 36

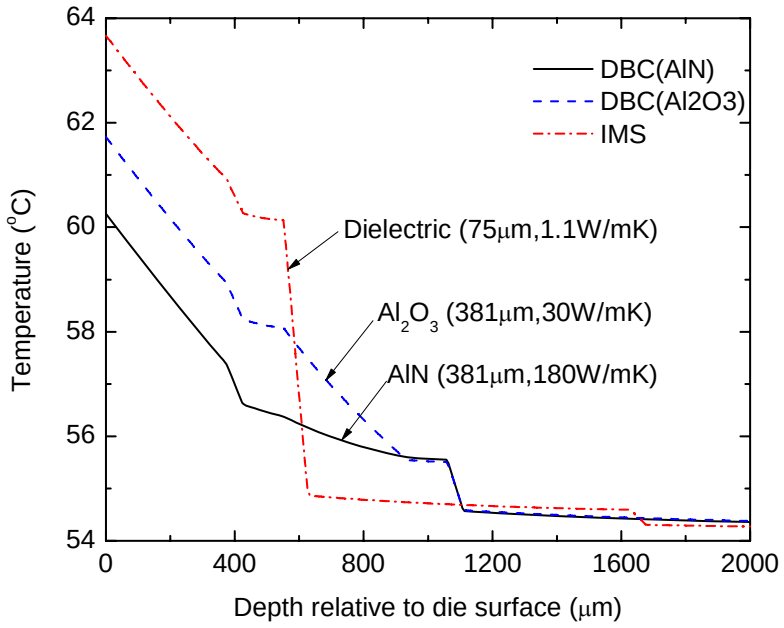


Figure 40. Vertical (*z*-axis) temperature profiles through the package along the center line. The results of simulations shown in Figure 36 were used.

The large difference is shown in the substrate because different substrates are used. The thermal resistance of IMS is about 5 times larger than that of AlN DBC substrate. This is not a large difference compared to the difference between thermal conductivities of the dielectric (IMS) and AlN (DBC) layers; 1.1 W/mK and 180 W/mK, respectively. If we assume that the system is one-dimensional, which means that the heat flux area is same through the system, the thermal resistance of dielectric should be more

than 30 times larger than that of AlN even considering the thickness of the ceramic and the dielectric layer, 381 μm and 75 μm respectively. Nevertheless, the reason why the difference is so small is the effect of heat spreading. Since the heat flux is spread by the top copper circuit layer and then flows through the dielectric layer, it increases the heat flux area and the thermal resistance of dielectric layer is reduced. Therefore, the thickness and the area size of the copper circuit layer are important for the reduction of the thermal resistance of overall power substrate. The heat spreading effect in substrate will be discussed in the latter part of this chapter.

3.2.2 Thermal Resistance Analysis

From vertical profile of temperature, we can easily calculate the thermal resistance of each layer. This calculation is based on the maximum temperature of each interface. Although the maximum temperature calculation is simple, using the average temperature of each interface could be more accurate. Here, we will determine which method is more reasonable by simple comparison. A circular substrate that has two layers was modeled, and a 1 mm^2 of uniform heat flux area was placed at the center of the substrate (see Figure 41). When the substrate size was small, the maximum temperature of substrate decreased as the substrate size increased due to the heat spreading. However, after the substrate exceeded a certain size, the maximum temperature became independent of substrate size. This is because heat spreading occurs only over a limited area. In this simulation, when the radius of substrate is four times larger than that of heat flux area, the maximum temperature, the spreading profile, and the thermal resistance of the entire system are nearly independent of the substrate size. Contrarily if we use thermal resistance based on the average interface temperature, thermal resistance changes as substrate size increases even though the temperature

distribution profile does not change. This is because a redundant area, or area not involved in heat spreading, is used in calculating thermal resistance. If we can determine the effective area for heat spreading, using the average temperature of interface over this effective area could be more accurate. However, determining the effective area is much more difficult than determining the maximum temperature of the interface. Moreover, we can predict the highest temperature of the system by using thermal resistance based on the maximum temperature. Therefore, thermal resistance based on the maximum temperature gives simpler and clearer understanding of the system with a heat spreading effect, and it will be used in this study.

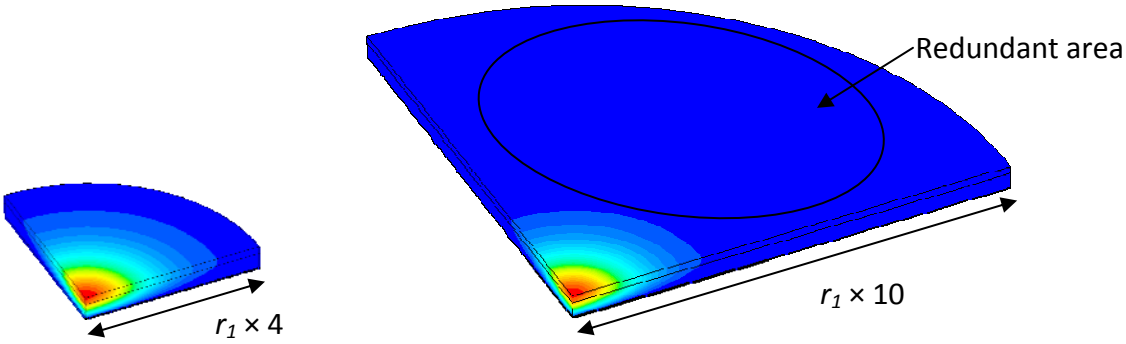


Figure 41. Comparison between two different simulations. The same design, material, and conditions are used except the substrate size. The radius of the heat flux area, r_1, is 564.19 μm. The layer-1 is 100 μm of thickness and 30 W/mK of thermal conductivity, and the layer-2 is 200 μm and 3 W/mK. Heat flux is 1 W/mm^2 and bottom temperature is 0°C. The maximum temperatures are nearly same as 34.466°C and 34.452°C.

Table 12. Thermal resistance calculations with two different methods.

R_{th} / radius	R_{th} calculated by Maximum temperature (°C/W)			R_{th} calculated by Average temperature (°C/W)		
	Total	Layer-1	Layer-2	Total	Layer-1	Layer-2
$r_1 \times 4$	34.466	2.516	31.950	29.099	24.927	4.172
$r_1 \times 10$	34.452	2.513	31.939	27.457	26.788	0.668

The thermal resistances of the packages with the two DBC and one IMS substrates are calculated and shown in Table 13. In spite of the same thickness and thermal conductivity of the TIM used in the package, its thermal resistance varies with different substrates utilized. This is due to the heat spreading characteristics in substrates which vary with the substrate type.

Table 13. Thermal resistance of each layer with different substrates, calculated based on the temperature along the center line—the maximum temperature of the interface.

R_{th} / Material	Thermal Resistance R_{th} (°C/W)		
	AlN DBC	Al_2O_3 DBC	IMS
Die	2.89	2.81	2.74
Die-attach	0.74	0.66	0.64
Substrate	1.15	2.82	5.72
TIM	0.92	0.86	0.26
Heat sink	29.57	29.59	29.31
Total (R_{tot})	35.26	36.73	38.67

Once the thermal resistance of a specific system is calculated by FEA results, the junction temperature as a function of arbitrary power input and ambient temperature can be easily calculated using following relationship.

$$T_j = R_{tot} \times P + T_{Ambient} \tag{4.2}$$

where R_{tot} is total thermal resistance, P is power input, and $T_{Ambient}$ is ambient temperature. The simulations were conducted with different power inputs using the same modeling shown in Figure 36, and the junction temperatures were compared with that calculated using Equation 4.2 (see Figure 42). The results of the FEA and thermal resistance model are exactly the same. It confirms that the thermal resistance of the system is neither a function of power input nor a function of ambient temperature, but a

function of geometry and thermal conductivity. This is valid only if a temperature-independent thermal conductivity and uniform convection heat transfer coefficient are used.

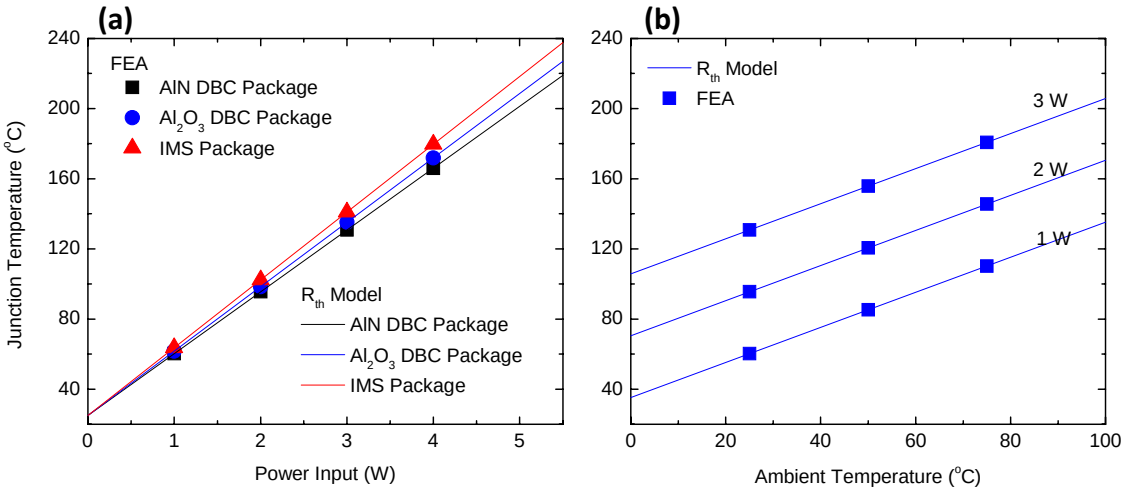


Figure 42. (a) The junction temperature as a function of power input and (b) The junction temperature as a function of ambient temperature (AlN DBC)

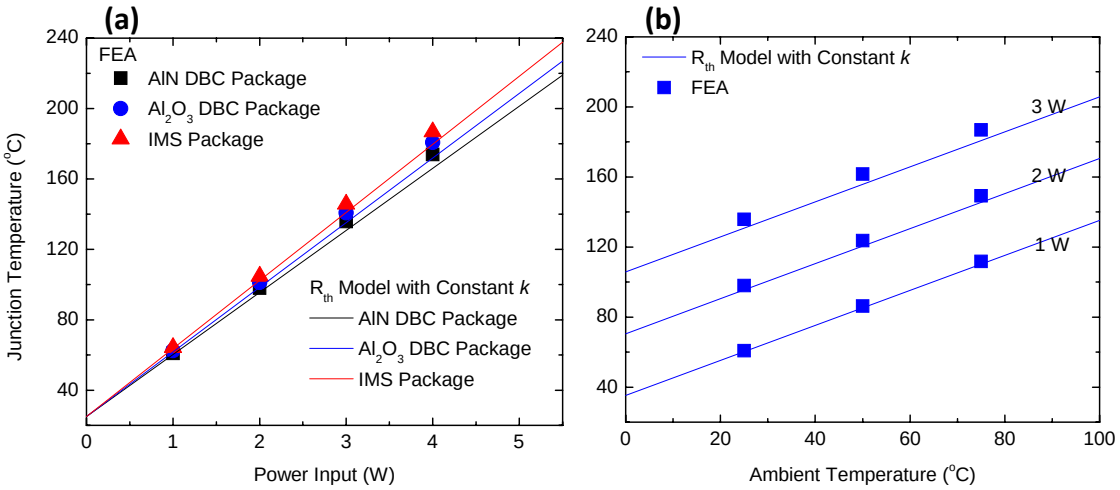


Figure 43. (a) The junction temperature as a function of power input, and (b) as a function of ambient temperature. Lines were estimated by thermal resistance model with constant *k*, and symbols were from FEA results with temperature dependant k, shown in Figure 44. We assumed that thermal conductivities of Au-20Sn, TIM, and dielectric are temperature independent.

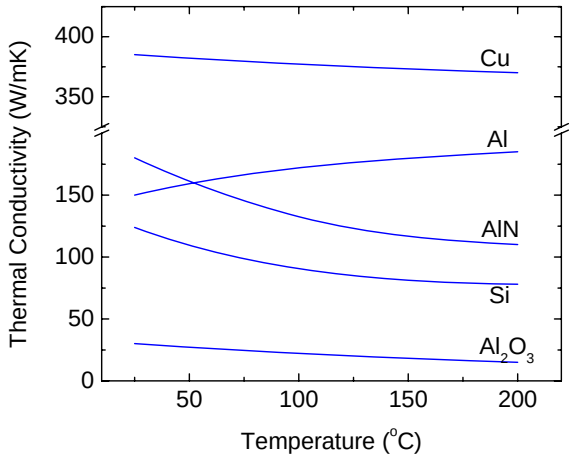


Figure 44. Temperature dependant thermal conductivity [33, 34, 36, 37]

In most practical cases, the thermal conductivity is a function of temperature (see Figure 44). Thermal conductivity of most materials decreases as temperature increases in the region of concern (0-200°C). Therefore, as the operating temperature becomes higher, the junction temperature estimated by thermal resistance model underpredicts the actual case. The junction temperatures of LED packages were estimated with temperature-dependant and -independent thermal conductivities and compared in Figure 43. Despite a mismatch, since it is not significant, the thermal resistance model with temperature-independent thermal conductivity is still useful. For example, if we use AlN DBC package with 3 W power input at 25°C ambient temperature, the junction temperature is 135.82°C by temperature-dependant thermal conductivity and 130.78°C when an independent thermal conductivity is used.

3.3 Thermal Characterization of Subcomponents

As studied previously, if temperature-independent thermal conductivity and uniform convection heat transfer coefficient are used, the thermal resistance of the system is only a function of thermal conductivities and design parameters. Therefore, we need to study the effect of thermal conductivities and design parameters on the thermal resistance of the system. In this study, we divide the system into three parts (die and die-attach, substrate, and TIM and heat sink) and will study the thermal characteristic of each part.

3.3.1 Die and Die-attach

3.3.1.1 Die (Submount)

Since the heat flux in the die and die-attach is very high, the junction temperature is very sensitive to the thermal conductivity and the thickness of the die and die-attach. Here, we will study the junction temperature change with respect to different materials and thicknesses of the die and die-attach. The simulation conditions are shown in Figure 45. We consider vertical thin film structure and available materials for die are Si and SiC. Si is very widely used because of its cheap price, easiness in processing, and fairly high thermal conductivity, 124 W/mK. SiC is an alternative material that has not only high thermal conductivity, 370 W/mK, but also well-matched CTE with GaN. Nevertheless, it is not used generally due to its extraordinary high price. Material properties of Si, SiC, and GaN are shown in Table 7 and Table 10.

The junction temperature as a function of thickness is shown in Figure 47. The behavior of junction temperature with respect to thickness is almost linear, which implies that the thermal resistance of die can be assumed as a one-dimensional form. Therefore, the thinner die is definitely better for thermal management. For example, the difference of the junction temperature between 525 μm and 100 μm die is 3.2°C with 1 W power input, but the difference increases to 16°C with 5 W. The die is attached to the chip and

mainly used for easy handling of the chip because the LED-chip by itself is so thin, less than 4 μm, such that very elaborate processing is required.

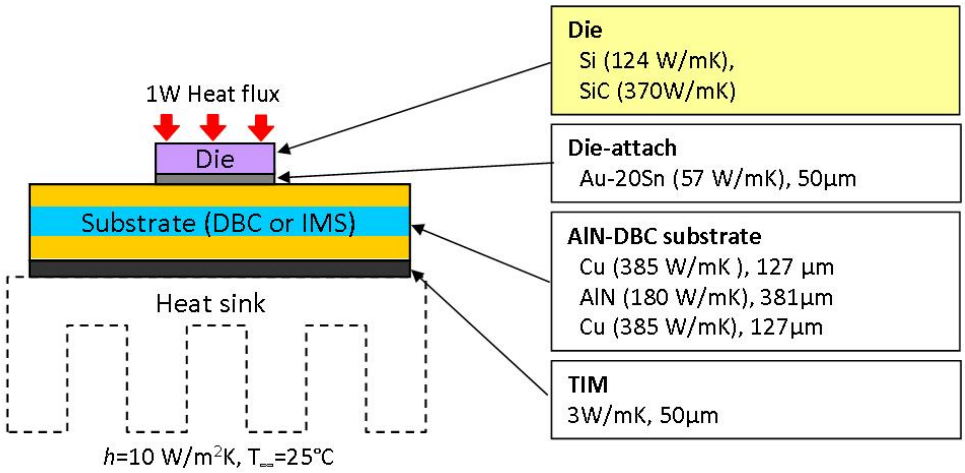


Figure 45. The simulation conditions for the thermal characteristic analysis of die. Two different die materials, Si and SiC, were used with thicknesses of 100 μm, 275 μm, 375-μm, and 525 μm, which are standard thicknesses of Si wafers.

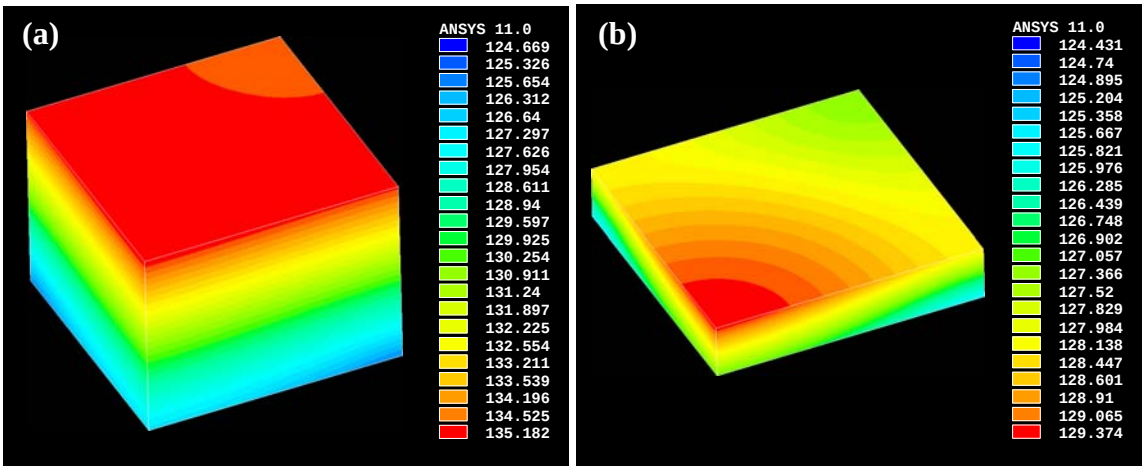


Figure 46. The contour plot of the temperature distribution in die with 3W power input. (a) 375 μm of Si die and (b) 100 μm of Si die. The simulation conditions are shown in Figure 45 with 3 W power input.

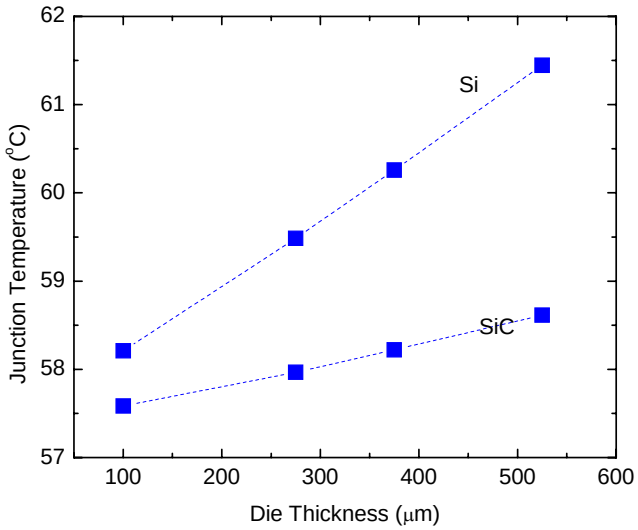


Figure 47. The junction temperature as a function of die thickness. Two different dies were used; Si (124 W/mK) and SiC (370 W/mK). The simulation conditions are shown in Figure 45.

3.3.1.2 Die-attach

All dies are bonded to the next assembly, which is a substrate or a package, with a die-attach. It provides the absorption of the thermal mismatch between the die and substrate as well as bonding. There are many candidates for the die-attach materials, and gold-based and silver-based solders are generally used due to their superior mechanical and thermal properties. In this study, we considered Au-20Sn, Sn-3.5Ag, and 100In solders as die-attach materials. The junction temperature as a function of die-attach thickness was plotted in Figure 49. Like the die, the behavior of junction temperature with respect to die-attach thickness is almost linear. Although the thermal conductivities of die-attach materials are lower than those of die materials, their thermal resistances are not significantly high because of their relatively small thickness. Considering the general thickness of die-attach, less than 50 μm, the junction temperatures of the packages using Sn-3.5Ag, Au-20Sn, and 100In are 60.26°C, 60.90°C, and 59.98°C, respectively. Despite its very high price, hard eutectic 80Au-20Sn (wt%) solder is commonly used for

the LED package because a very uniform thickness and composition, a smooth plating surface and very high precision solder placement are all possible, resulting in major advantages for optoelectronic packaging applications.

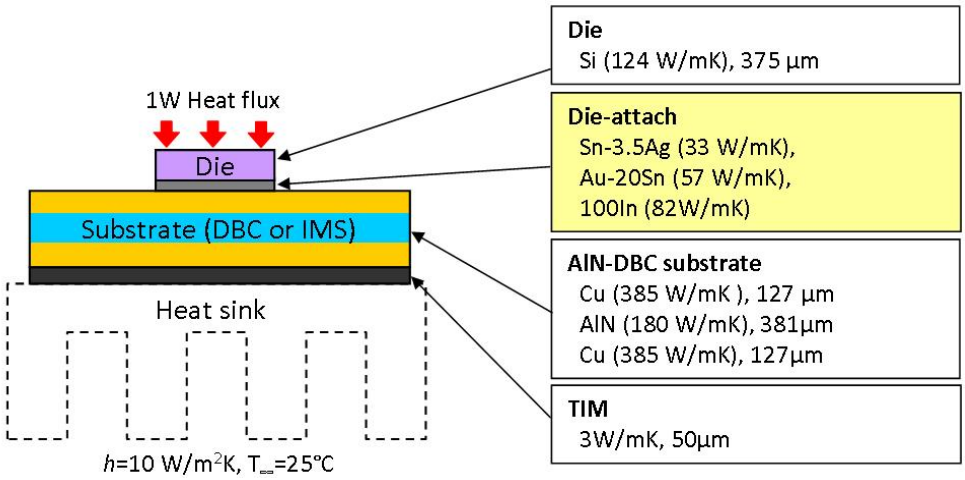


Figure 48. The simulation conditions for the thermal characteristic analysis of die-attach. Three different die-attach materials were used with different thicknesses.

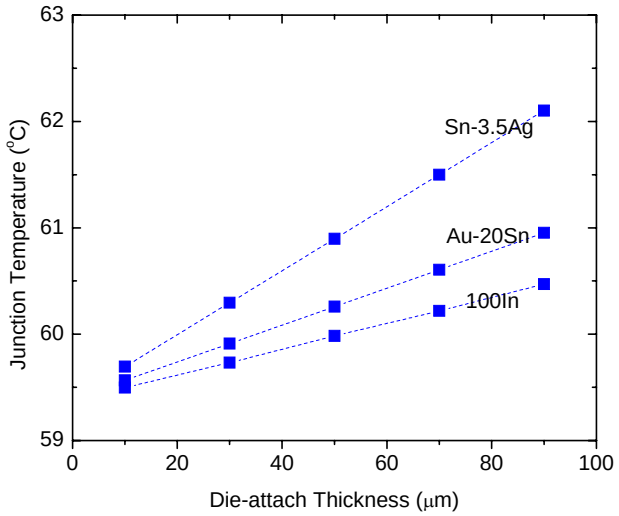


Figure 49. The junction temperature as a function of die-attach thickness. Three different solders were used; Sn-3.5Ag (33 W/mK), Au-20Sn (57 W/mK), and 100In (82 W/mK). The simulation conditions are shown in Figure 48.

3.3.2 Substrate

The relatively high thermal conductivity of ceramics in DBC substrates and thin dielectric layers in IMS are very beneficial to reduce thermal resistance in substrate level. In addition, heat spreading in copper circuit layers is another important factor for good thermal management. The thick copper circuit layer is called "heavy copper" and considered as an effective way for thermal management of high power electronics. Since the copper circuit layer is the path for heat spreading, the lateral size of copper circuit layer should be maximized (see Figure 51). In this study we assume that copper circuit layer has the same size as the substrate, and the size effect of copper circuit layer will be considered later. In case of the array of LEDs, the placement of LED-chips is important to avoid the interference of the heat spreading effect. If LED-chips are placed so closely with one another, the heat will not spread enough and the junction temperature will increase. Half of the distance between LED-chips can be modeled with adiabatic boundary conditions to account for the periodic array of LEDs as shown in Figure 28(b). Since the heat spreading of the substrate level mainly occurs in the copper circuit layer, the important factors to determine the thermal resistance of a substrate are the thickness of the copper circuit layer and the size of the substrate. Several simulations using different thickness of the copper layer and different size of substrates were performed.

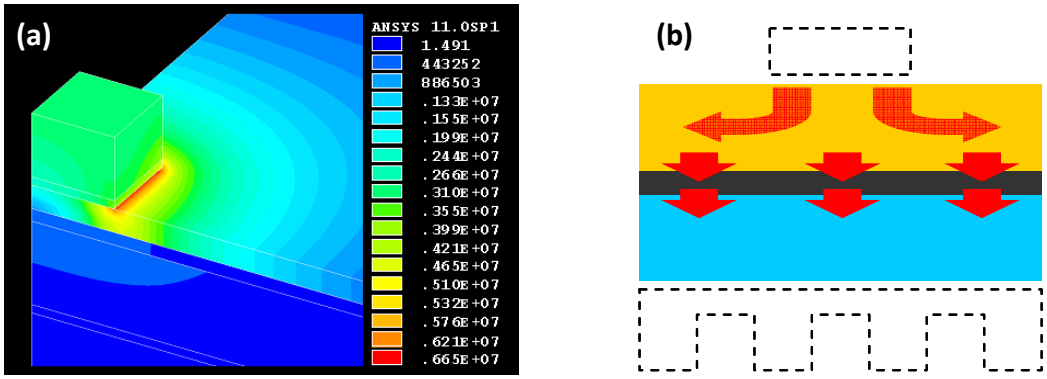


Figure 50. (a) The contour plot of the heat flux distribution in IMS. (b) The schematic of heat spreading.

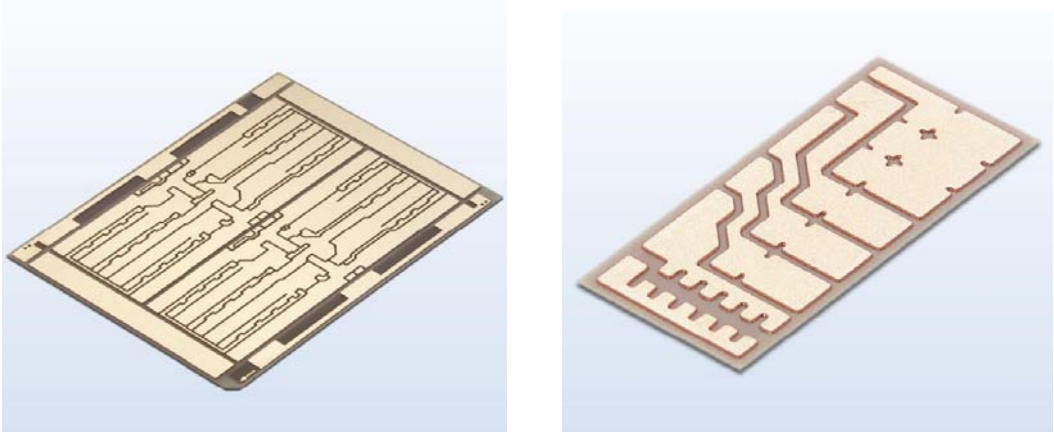


Figure 51. The copper circuit layer of DBC substrate. The area of copper circuit layer should be as large as possible for good thermal spreading. *Source: Curamik* [37].

3.3.2.1 The Thickness of Copper Circuit Layer

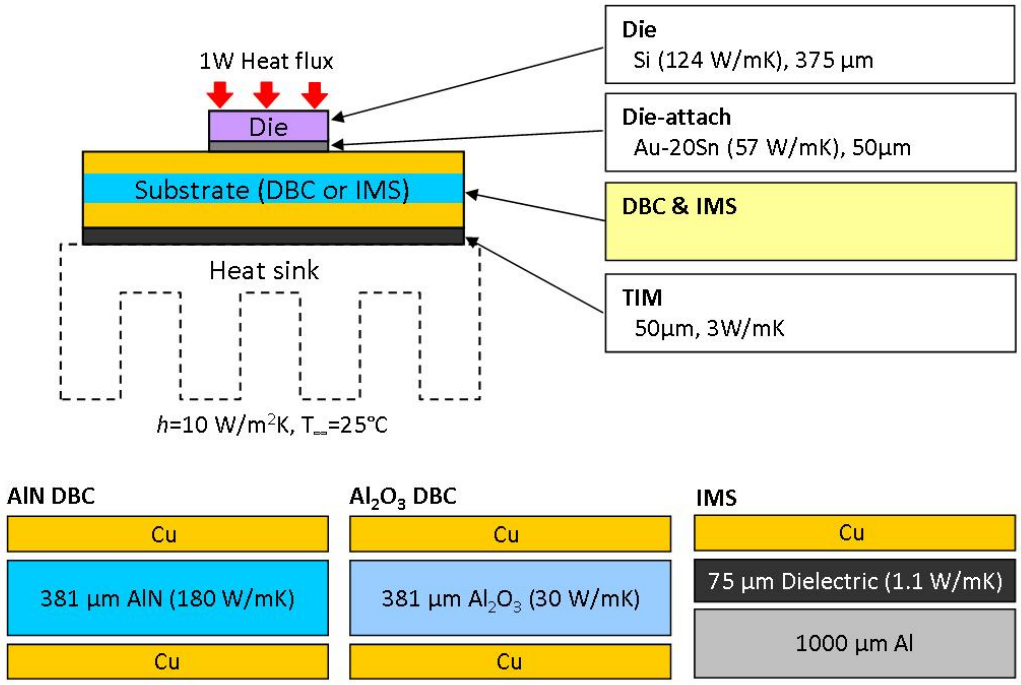


Figure 52. The simulation conditions for the thermal characteristic analysis of substrate. Three different substrates were used. The junction temperatures as a function of copper thickness and as a function of substrate size were studied.

The difference of temperature distribution in substrates with different copper thickness is shown in Figure 53, and the junction temperature as a function of thickness of copper circuit layer is shown in Figure 54. It confirms that a thicker copper layer can achieve a lower thermal resistance. However, the impact of copper thickness varies with types of the substrate and their property. In case of the LED package with the AlN DBC substrate, the junction temperature difference between 35 μm and 350 μm of copper layer is only 1.38°C with 1 W operation. This is because the AlN with its large thermal conductivity (180 W/mK) contributes to the heat spreading, assisting thinner copper circuit layers. In case of the LED package with IMS, due to the low thermal conductivity of dielectric, the junction temperature difference is 9.1°C with 1 W operation. In this case, the heat spreading is mainly coming from the copper circuit layer with very little contribution from the dielectric.

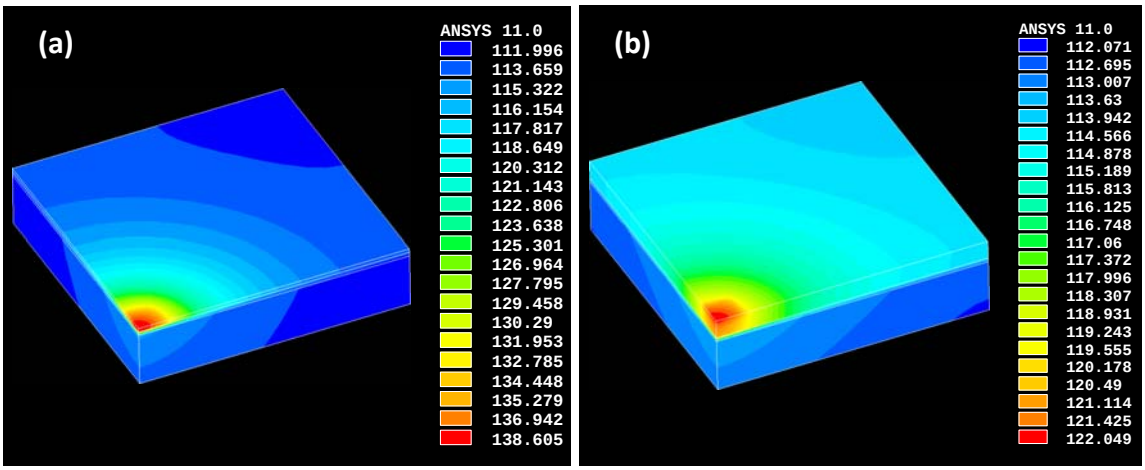


Figure 53. The contour plots of the temperature distribution in IMS. (a) 70 μm copper circuit layer (b) 350 μm copper circuit layer. The conditions shown in Figure 52 were used with a 1 cm by 1 cm substrate and 3 W power input.

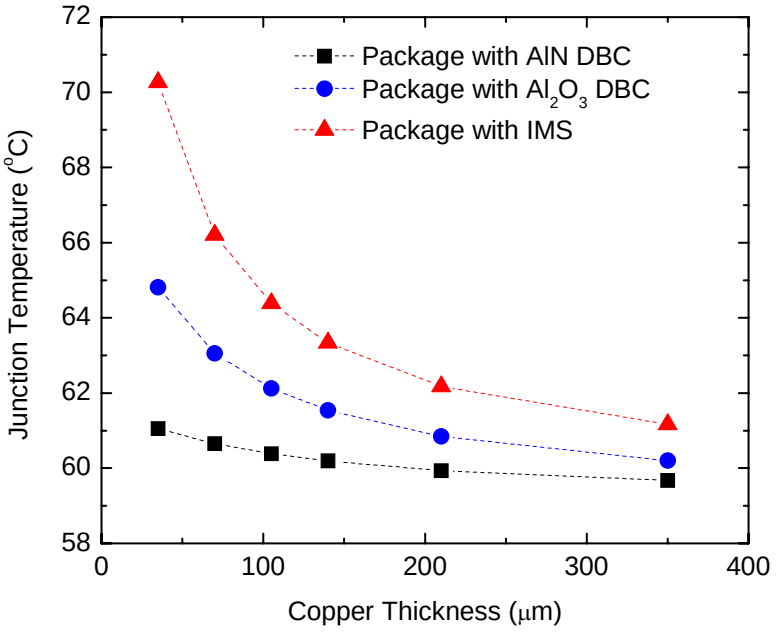


Figure 54. The junction temperature as a function of the thickness of the copper circuit layer. The conditions shown in Figure 52 were used with 1 cm by 1 cm substrate size.

3.3.2.2 The Lateral Size of Copper Circuit Layer

The difference of temperature distribution in substrates with different lateral size of substrate is shown in Figure 55 and Figure 56, and the junction temperature as a function of the thickness of the copper circuit layer is shown in Figure 54. It confirms that a larger substrate can achieve a lower thermal resistance. When the size of a substrate is small, the rate of decrease in junction temperature is large. This is because a certain size of substrate is required to spread heat enough in the substrate and the size is determined by the design and materials used. For example, 20 to 30 mm^2 is enough to spread heat for DBC substrate, while 40 to 50 mm^2 is required for IMS under the design and conditions used for Figure 56.

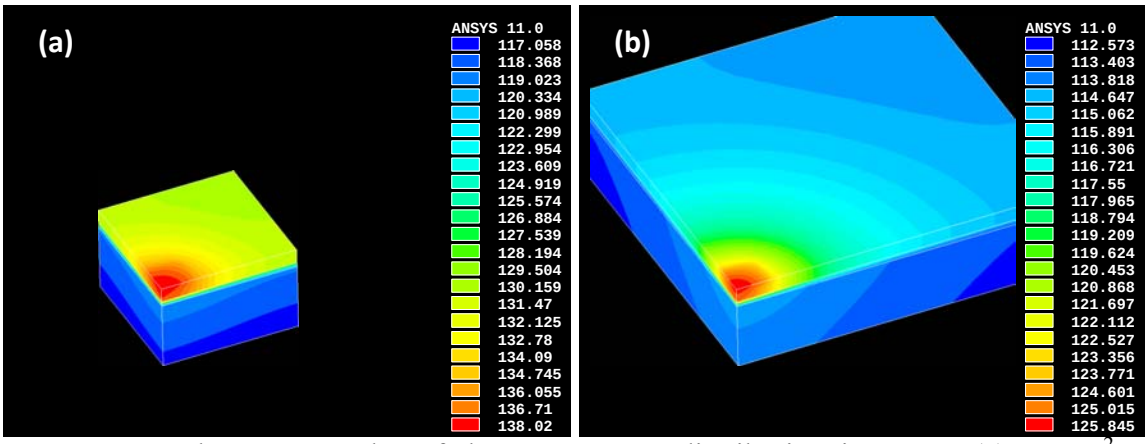


Figure 55. The contour plot of the temperature distribution in IMS. (a) 16mm^2 of substrate (b) 100mm^2 of substrate. The conditions shown in Figure 52 were used with 210 μm copper circuit layer and 3 W power input.

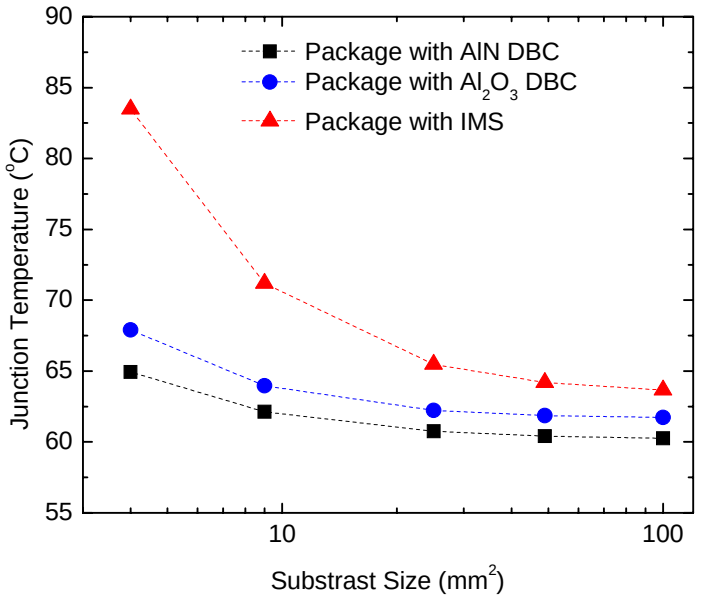


Figure 56. The junction temperature as a function of the substrate size. The conditions shown in Figure 52 were used with 210 μm copper circuit layer.

3.3.2.3 Restriction of Design

A thicker copper circuit layer is typically better for thermal management. However, the copper circuit layer's thickness is limited by the cost and by the ability to pattern thick circuit layers. The required resolution of the circuit pattern is strongly

dependant on the application. Although a high resolution circuit is not require for most general LED structures, it may be required for the flip-chip structure because n-electrode and p-electrode must be placed very close together. The degree of resolution is generally specified as pitch rate, which is the distance between 2 pads as a minimum need. The restriction mainly comes from the isotropic etching of copper and the breakdown voltage of the dielectric. The available pitch rate depends on the copper thickness, and the available pitch rate of DBC substrate with standard $CuCl_2$ etching is shown in Table 14. Commercialized DBC and IMS substrates have their design guidelines provided by the vendors and it specifies the pitch rate or minimum space between the circuits. As the copper circuit layer becomes thicker, the pitch rate becomes larger. That is to say, the thickness of circuit is limited by the resolution. In addition, a thicker copper layer needs a longer processing time. Not only the price of copper but also the incidental expenses of manufacturing are another limitation of using thick copper.

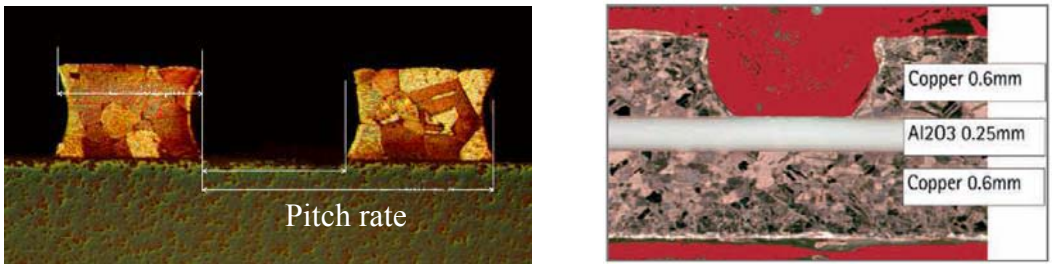


Figure 57. Example of etched DBC substrate cross section view [38].

Table 14. The available pitch rate of DBC substrate with standard $CuCl_2$ etching [38].

Cu thickness (mm)	Pitch rate (mm)
0.2	0.8
0.3	1.0
0.4	1.2

3.3.4 TIM & Heat sink

3.3.4.1 TIM

A TIM is used to fill the gaps between the LED package and a heat sink, in order to decrease thermal contact resistance. These gaps are normally filled with air, which is a very poor conductor (k=0.026 W/mK), and it must be eliminated from the thermal path. Materials used for gap filling include solder, thermal grease, phase change materials, adhesive tapes, gap filling material and others. The properties of the various TIM are summarized in Table 15.

Table 15. Thermal Properties of Interface materials [24, 39-42]

Material	Manufacture (Model)	Typical Thickness (inch/ mm)	Thermal Conductivity (W/mK)	Thermal impedance (°C-in^2/W)
Solder	100In	-	82	-
	90In-10Ag	-	67	-
	80Au-20Sn	-	57	-
	77.2Sn-20In-2.8Ag	-	54	-
	88Au-12Ge	-	44	-
	96.5Sn-3.5Ag	-	33	-
Thermal Grease	Momentive Performance Material (YG6260-5)	-	0.84	-
	Shin-etsu Chemical (G751-1)	-	4.5	-
Phase Change Material	Laird Technologies (T-PCM 905)	0.005 / 0.127	0.7	0.048 @ 10 psi
Adhesive Tape	Chomerics (T412)	0.009 / 0.229	1.4	0.25 @ < 1 psi
	Bergquist (BP105)	0.005 / 0.127	0.8	0.86 @ < 1 psi
	3M (8815)	0.015 / 0.381	0.6	1.20 @ < 1 psi
Gap Filling Material	Laird Technoligies (T-pli 210)	0.010 / 0.254	6	0.16 @ 20 psi
	Laird Technoligies (T-flex 640)	0.040 / 1.016	3	0.62 @ 10 psi

Typical thickness of a TIM depends on the type of material used and usually ranges from 50 μm to 1 mm. In this study, we considered TIMs in the form of 100In and Sn-3.5Ag solders, and a 3 W/mK of thermal grease. Several simulations using different thickness were performed, and the results were plotted and shown in Figure 59. The impact of TIM thickness on thermal resistance of package is negligible. For example, the differences of the junction temperature between the package with 50 μm and 400 μm TIM are less than 0.25°C in case of solders, and 1.5 °C in case of 3 W/mK of thermal grease. Also, the type of TIM, which is the thermal conductivity of TIM, is not important in thermal management of the system. It is shown more clearly in Figure 60. The junction temperature difference between the package with 10 W/mK TIM and 100 W/mK TIM is only less than 0.26°C.

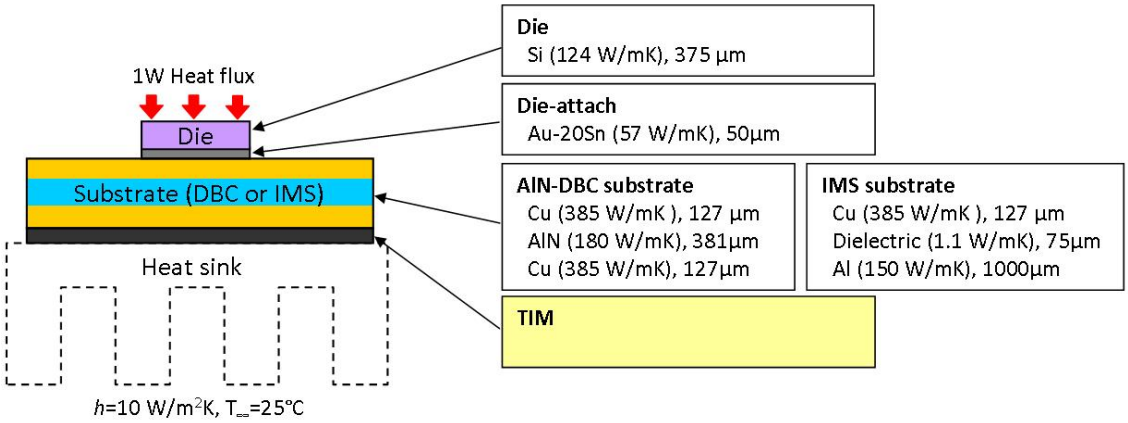


Figure 58. The simulation conditions for the thermal characteristic analysis of TIM. Three different TIMs were considered; 100In (82 W/mK), Sn-3.5Ag (33 W/mK), and thermal grease (3 W/mK). The junction temperatures as a function of TIM thickness and as a function of thermal conductivity of TIM were studied.

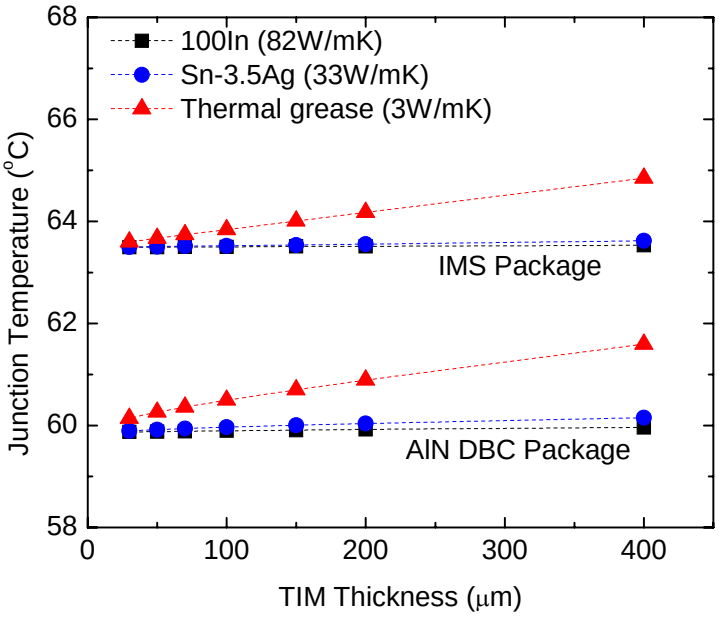


Figure 59. The junction temperature as a function of the thickness of TIM. The conditions shown in Figure 58 were used with 3 W/mK TIM.

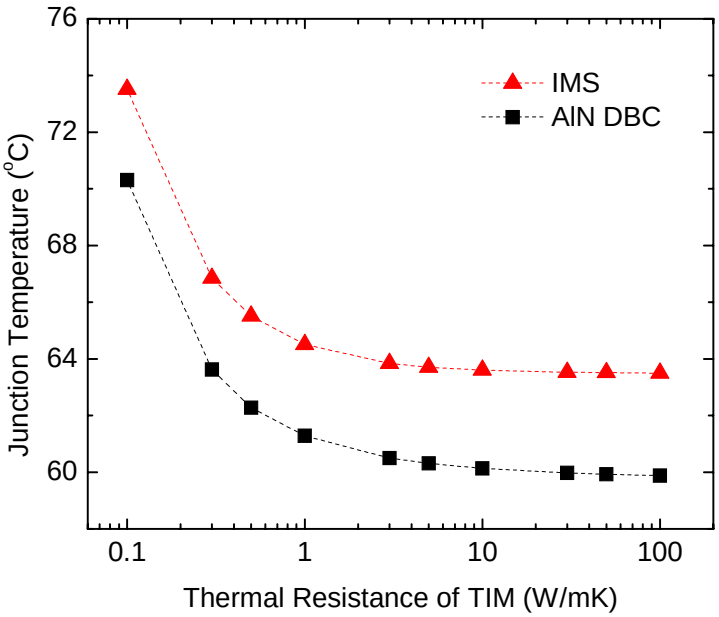


Figure 60. The junction temperature as a function of thermal conductivity of TIM. The conditions shown in Figure 58 were used with 100 μm of TIM.

3.3.4.2 Heat Sink

Heat sink is one of the most important factors in reducing the thermal resistance. The most effective way to increase the efficiency of a heat sink is to use a large heat sink with forced convection. However, both solutions are not suitable in many cases because a large heat sink is restricted by the design criteria for the LED fixture and forced convection requires additional power input. Therefore, effective design of a heat sink for a large convection heat transfer coefficient is another big subject. In this study, we only consider the heat sink with straight fins, and examine the effect of material, size and convection heat transfer coefficient.

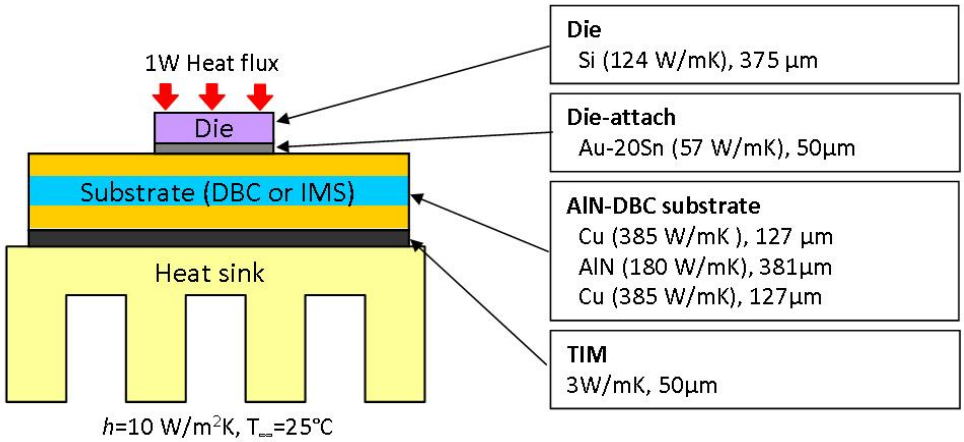


Figure 61. The simulation conditions for the thermal characteristic analysis of heat sink.

Firstly, two different materials were examined; Al and Cu. Although Cu has much higher thermal conductivity than Al, 385 W/mK and 150 W/mK respectively, both cases have almost same thermal resistances (see Figure 62). With different size and convection heat transfer coefficient, the materials of heat sink made no significant difference. It is limited only in case that heat spreads enough before a heat sink. If a localized high heat flux is applied on top of a heat sink, its material would be an important factor to increase the efficiency. The junction temperature as a function of the heat sink size with different convection heat transfer coefficient was studied (see Figure

63). As expected, size of a heat sink is a very important factor to determine the thermal resistance of a heat sink. The effect of convection heat transfer coefficient is much larger in a small heat sink than in a large heat sink. With a very large heat sink the benefit of high convection heat transfer coefficient becomes small since the entire heat sink is not uniformly heated or effectively used due to limited heat spreading.

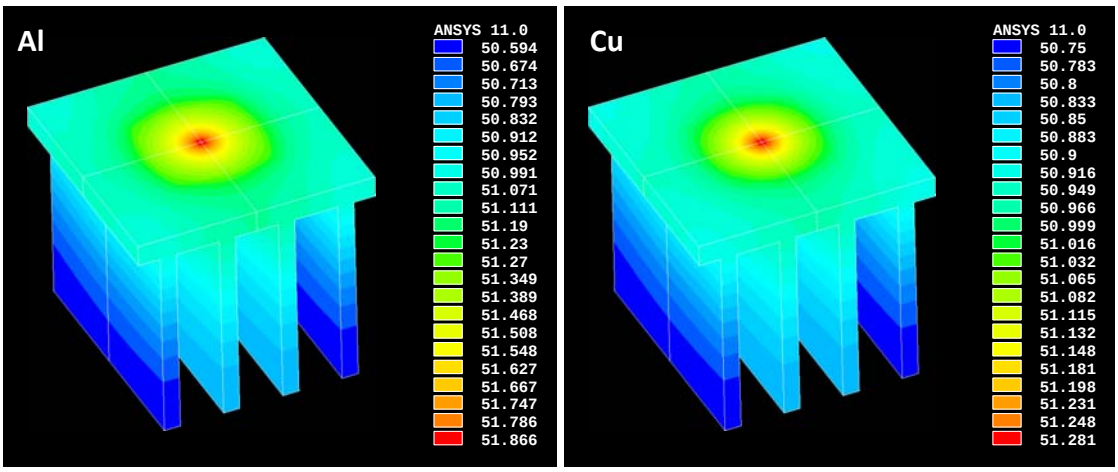


Figure 62. The contour plot of the temperature distribution in heat sink. The conditions shown in Figure 61 were used with two different heat sink materials; Al (150 W/mK) and Cu (385 W/mK)

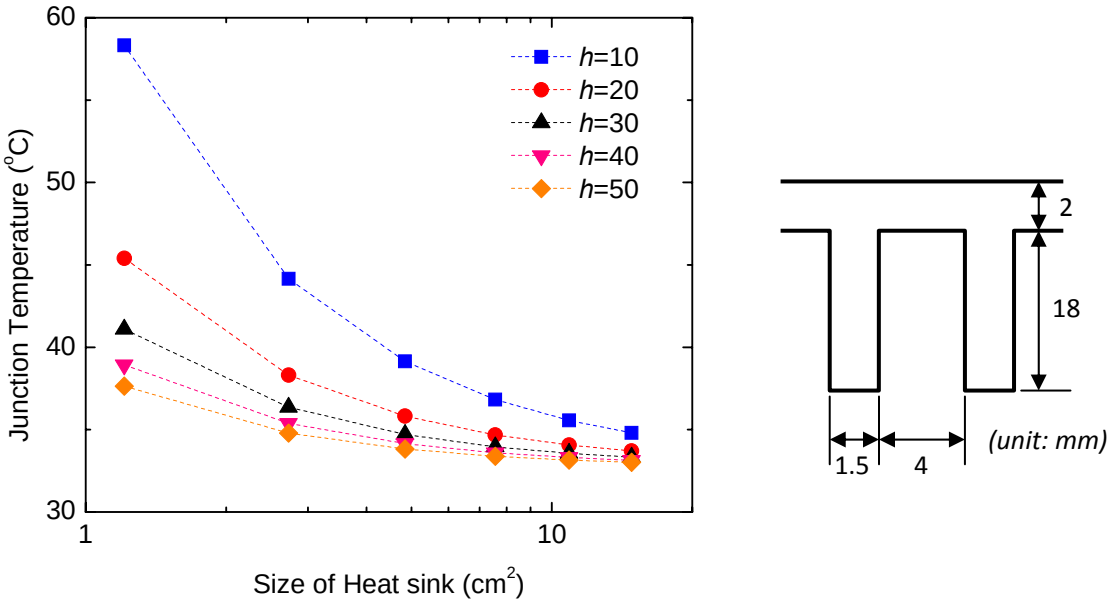


Figure 63. The junction temperature as a function of the size of heat sink with different convection heat transfer coefficient. The conditions shown in Figure 61 were used with the heat sink design shown here.

3.4 Summary

Thermal resistance of a system can be easily estimated by simulation. If temperature independent thermal conductivities are used, thermal resistance is neither a function of input power nor a function of ambient temperature. Therefore, the thermal resistance of the system can be estimated by only one simulation with a fixed design and temperature independent thermal conductivity. Then, various responses with respect to different power input and ambient temperature can be easily calculated by using a simple thermal resistance model (see Equation 4.2). In actual cases, the thermal conductivity is temperature-dependant property and the thermal resistance of the system increases slightly as power input and ambient temperature increase.

In order to analyze the thermal characteristics of each layer, estimating the thermal resistance of each layer is required. When estimating the thermal resistance, it is more reasonable to use the temperature along the center line, where the maximum heat flux exists, than using the average temperature of each layer. That is because the heat spreading makes it very difficult to determine the effective heat flux area.

In die and die-attach their thermal resistances are very sensitive to the thermal conductivities and the thickness because of very high heat flux in them, 100 W/cm^2 to 500 W/cm^2 with 1 W to 5 W power input. Since the die and die-attach can be assumed as one-dimensional heat flux structure, their thermal resistances are directly proportional to their thicknesses.

The power electronic substrates have two advantages compared to a conventional FR4 PCB. One is in their dielectric materials. In the case of a DBC substrate, ceramics, which have very high thermal conductivities; AlN (180 W/mK) and Al_2O_3 (30 W/mK), are used as dielectric material. Although the thermal conductivities of dielectrics are not so high in the case of IMS, 1 to 2 W/mK, low thermal resistance can be achieved using thin layers. The other point is that they take an advantage of “heavy copper.” By spreading heat in thick copper circuit layer, the effective heat transfer can be achieved.

Therefore, high thermal conductivity of dielectric, the thicker copper circuit layer, and large size of a substrate are required to achieve low thermal resistance.

Thermal conductivity and thickness of the TIM are not critical factors to determine the thermal resistance of the package. That is because the heat flux after the substrate drops to only 2 to 6% of that of die level due to heat spreading in substrate. The thermal resistance of the system largely depends on a heat sink. Its material is not important if heat spreads enough in substrate level. The size and convection heat transfer coefficient are important for the thermal management. The role of the convection heat transfer coefficient is large in the small heat sink and it becomes smaller as the size increases.

In this chapter the simplified structure of a high power LED was analyzed by FEA and the effect of each layer on the junction temperature was studied. The optimized thermal design is not always acceptable because the design is restricted by other design considerations, cost and so on. The optimized design should be determined by considering trade-offs with all other factors. Therefore, the guideline for the thermal management with respect to each design parameter should be provided. FEA is time consuming for the parametric studies because a large number of simulations are required. If the thermal resistance of the system is expressed analytically, the importance of each parameter will be understood more easily. In the next chapter, we will analyze the thermal resistance of the system analytically and investigate the effect of each design parameter.

CHAPTER 4

ANALYTICAL MODELING

4.1 Motivation

In this chapter, we develop an analytical thermal circuit model for single chip LED packaging. Strictly a thermal design for LEDs is not always the optimal route to take because there are many other factors which must be determined. These include the electrical and optical design, the manufacturing costs, the restrictions induced by applications and so on. However, focusing on the thermal design, it is possible to perform FEA parametric studies as shown in Chapter 3. However, it becomes time consuming and tedious to create a new mesh every time a design parameter is changes. It would be beneficial if there was an analytical model which could help to address the need for parametric design analysis without the use of FEA. Therefore, an analytical model of the high power LED was developed for easy parametric studies, especially focusing on spreading effects at substrate level. If the thermal resistance of the system is expressed by accounting for each parameter and system subcomponent, the importance of each parameter will be understood more easily.

4.2 Construction of Thermal Circuit Model

First of all we need to divide the system into several components for the simplification of the problem. In this study we divide the system into three components; die and die-attach, substrate and TIM, and a heat sink. The thermal circuit model of the entire system is shown in Figure 64.

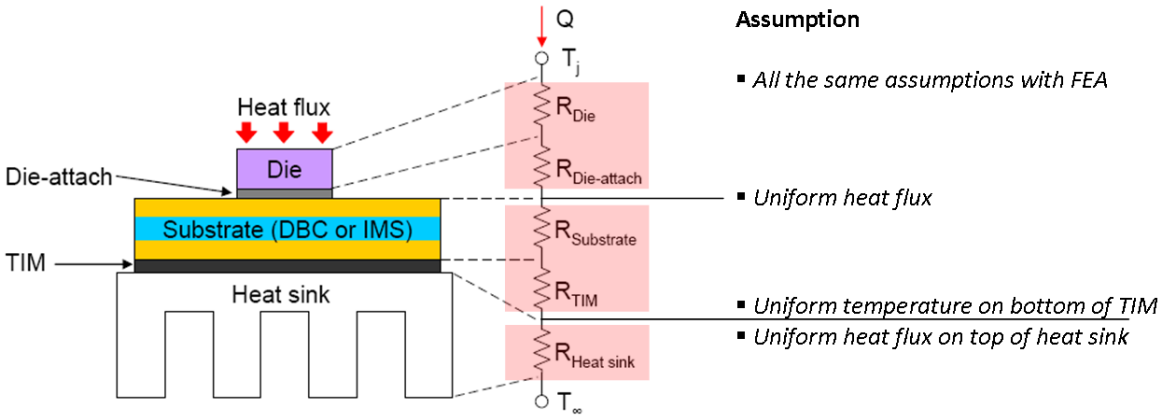


Figure 64. Equivalent thermal circuit for LED package. We divide the system into three components and make assumptions between components.

By FEA we knew that the junction temperature is almost linear with respect to the thickness of die and die-attach (Figure 47and Figure 49). Therefore, we can assume die and die-attach as one dimensional structure. To estimate thermal resistance of the substrate, a three-dimensional heat equation should be solved due to the heat spreading effect. Power electronic substrate such as DBC substrate and IMS consists of three layers. We may solve each layer separately; however it is more difficult because heat conducting area between the layers must be determined, which is not defined clearly. In addition, heat conducting area simultaneously changes with even other layers' parameters. For the same reason, considering TIM, together with substrate, makes the problem easier. Also, the possible boundary condition that we can apply at the bottom of component is isothermal, and it is more suitable before the high thermal conductivity layer. Therefore, considering TIM together with substrate gives more accurate calculation of thermal resistance of substrate in the system as well.

For the boundary conditions of substrate and TIM, we assumed uniform heat flux between die-attach and substrate and uniform temperature on the bottom of TIM. Although Figure 65 shows that heat flux at the bottom of die-attach, the difference is not significant except at the very edge. Once we use uniform heat flux assumption, and then will validate the result by comparing with that of FEA. The temperature at the bottom of

TIM is shown in Figure 66. The difference of temperature distribution at the bottom of TIM is only 0.6°C and even that on the top of heat sink is less than 0.8°C. Therefore, we assume uniform temperature at the bottom of TIM.

Although we assume uniform temperature at the bottom of TIM, we used uniform heat flux with the size of substrate on the top of heat sink because of energy balance. By FEA we knew that the thermal resistance of heat sink is hardly affected by the other structures and vice versa if heat spreads sufficiently in substrate level. That is to say whatever heat flux area is used, the thermal resistance of heat sink is almost same. Therefore, we assume that heat flux area at the top of heat sink is the same with substrate size, and then will examine this assumption.

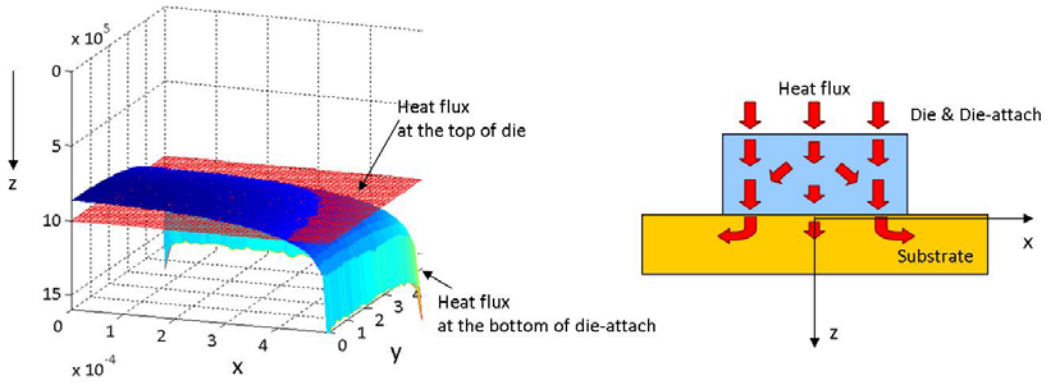


Figure 65. Heat flux at the top of die and at the bottom of die-attach. Due to heat spreading in substrate, heat flux at the edge is large

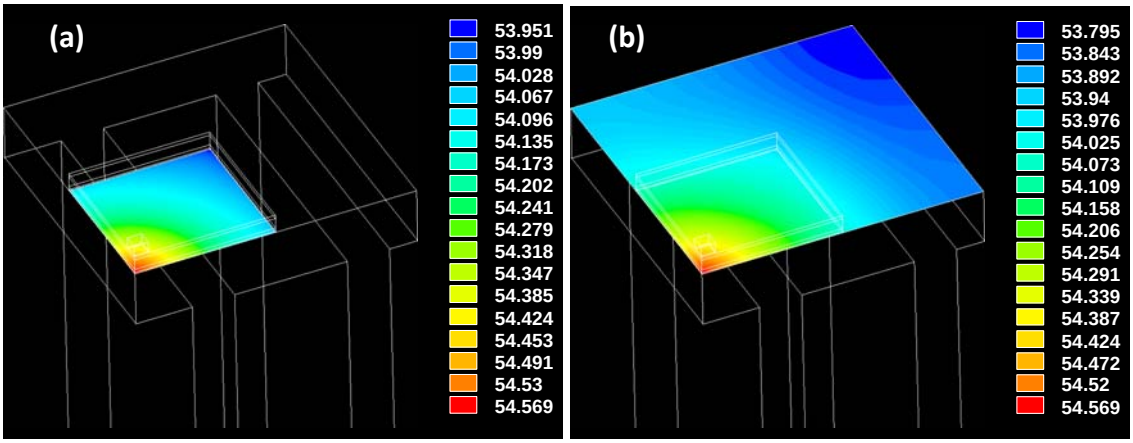


Figure 66. The contour plot of temperature distribution (a) at the bottom of TIM and (b) at the top of heat sink.

4.3 Die and Die-attach

In this study we assume that the heat flux on the top of the die is uniform, and heat flux area does not change in die and die-attach. From Figure 38 we can see that temperature gradient is nearly linear and that heat flux changes a little through the die and die-attach. Also, thermal resistances of die and die-attach shown in Table 13 are almost same regardless of the different substrates. Therefore, the thermal resistance of die and die-attach can be expressed using one-dimensional thermal resistance for conduction in a plane wall.

$$R_{Die} = \frac{t_{Die}}{k_{Die} A_{Die}} \tag{4.1a}$$

$$R_{Die-attach} = \frac{t_{Die-attach}}{k_{Die-attach} A_{Die-attach}} \tag{4.1b}$$

where t is the thickness, k is the thermal conductivity, and A is the size of the heat flux area. Thermal resistance calculated using Equation 4.1 is compared with thermal resistance of total system estimated using FEA.

Although slight disagreement exists in Figure 67, the results agree well. The disagreement is caused by heat spreading effect, especially when a thick die is used. As discussed with FEA results in previous chapter, in spite of relatively high thermal conductivity, the thermal resistance of die is large because of high heat flux. Die-attach has low thermal conductivity compared to die, however, thermal resistance is not significant because it is much thinner than the die. With the typical thickness of die-attach, 50 μm, the difference of thermal resistance between using Au-20Sn (57 W/mK) and using 100In (82 W/mK) is less than 0.7°C/W.

Using the same calculation, the thermal resistance of Au-Si eutectic bonding layer can be calculated, which was neglected because of its very small thickness. Au-Si eutectic bonding is usually used when transferring GaN LED-chip into Si by LLO

technique. It is approximately 25.4 μm thick and has a thermal conductivity of 27 W/mK [36]. Therefore, calculated thermal resistance of bonding layer is 0.941°C/W.

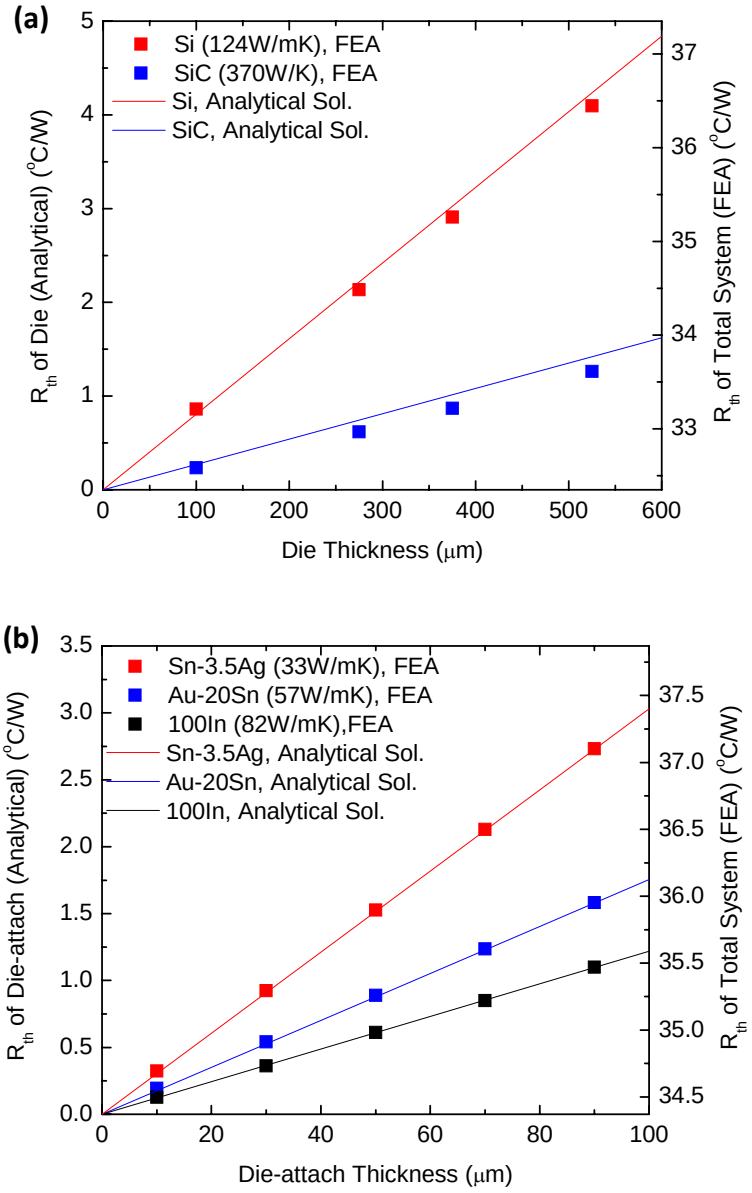


Figure 67. Validation of thermal circuit model of die and die-attach. The simulation conditions shown in Figure 45 were used, and only thickness of die and die-attach were changed. Left and right y-axis has the same scale.

4.4 Substrate and TIM

Heat spreading effect should be considered in substrate and TIM layer, and solving substrate and TIM together gives the most accurate result. Therefore, to analyze the characteristic of DBC or IMS with TIM, we need to solve four layers with the constant bottom temperature. It is not easy to determine thermal resistance of multi-layer substrate which has heat spreading effect. This is because thermal resistance of each layer is a function of other layers' dimension and conductivity as well as a function of its own.

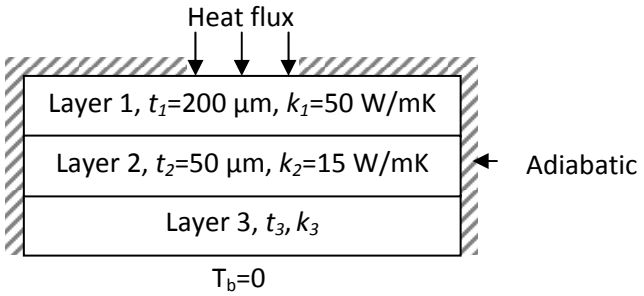


Figure 68. The schematic of the three-layer substrate with heat spreading effect. 1 mm^2 of circular heat flux in the center of 16mm^2 of 3 layers of circular disks is used.

Table 16. Thermal resistance of each layer with the different t3 & k3. The model shown in Figure 68 was used.

t_3 & k_3 / R_{th} (°C/W)	t_3 = 200 µm k_3 = 30 W/mK	t_3 = 200 µm k_3 = 3 W/mK	t_3 = 50 µm k_3 = 3 W/mK
R_{th} of layer-1	3.24	2.59	2.96
R_{th} of layer-2	2.08	0.91	1.57
R_{th} of layer-3	3.79	15.57	7.55

The difficulty of layer-by-layer analysis is well explained in the following example. Let us consider the three-layer substrate that has heat spreading effect (see Figure 68). We can readily know that if the thickness and thermal conductivity of layer-1 are changed, the thermal resistances of the layer-2 and layer-3 will be changed.

However, it is not easy to predict that the change of the layer-3 will also affects thermal resistances of the upper layers. This characteristic is shown in Table 16. Three-layers of circular disks are modeled, and dimensions and conductivities of upper two layers are fixed. The results show that as thermal conductivity of layer-3 is changed, the thermal resistances of the upper layers are changed. Similar results are seen when we change the layer thickness. It implies that if we estimate the thermal resistance with layer by layer calculation without considering other layers, it would make large errors on total thermal resistance of the system. Therefore, all layers should be considered together for the accurate estimation of the thermal resistance of multi-layer structure that has heat spreading effect.

4.4.1 Current Available Solutions for Spreading Resistance

The single layer solution in cylindrical system was derived first by D. P. Kennedy [43]. Although the solutions with different geometry and boundary conditions have been derived so far, there are not many solutions for multi-layer heat spreading problem. The only analytical solution for four-layer structure was derived by Palisoc et al. [45, 46]. However, the solution is very complex and requires large amount of calculation that is not suitable for parametric study. Also, since it is solved for an infinite plate problem, the solution does not account for the effect of a finite substrate size. Yovanovich et al. calculated thermal resistance of various geometries and various boundary conditions [48-54]. However, their analytical solutions are applicable only up to two layers. They used the effective thermal conductivity for more than two layers. It gives overall tendency of thermal resistance of multi-layer structure with various boundary conditions, but shows large errors in some cases.

Table 17. Comparison of available thermal spreading calculation.

Author	Geometry	Edge Boundary	Bottom Boundary	# of Layers
D.P. Kennedy, 1960[43]	Cylinder With circular source	Isothermal or Adiabatic	Isothermal or Adiabatic	1
R.D. Lindsted et al, 1993[44]	Rectangular plate with rectangular source	Adiabatic	Isothermal	2
A.L. Palisoc et al, 1988[45, 46]	Infinite Plate with rectangular source	(Infinite)	Isothermal	4
P. Hui et al, 1993[47]	Cylinder with circular source on infinite heat sink	Adiabatic	(Infinite)	2
M.M. Yovanovich, J.R. Culham, Y.S. Muzychka, 1998-2006[48-54]	Various geometry	Isothermal, Adiabatic, or Convection (Infinite)	Isothermal, Adiabatic, or Convection (Infinite)	2
F.N. Masana 1996[55-57]	Rectangular plate with rectangular source	Adiabatic	Isothermal	∞

Masana [55-57] calculated thermal resistance using spreading angle, based on analytical analysis and this solution is simple and gives fairly accurate result. Also it is possible to solve with strip heat source and eccentric heat source, and is not restricted by the number of layers. The general solution is as follows;

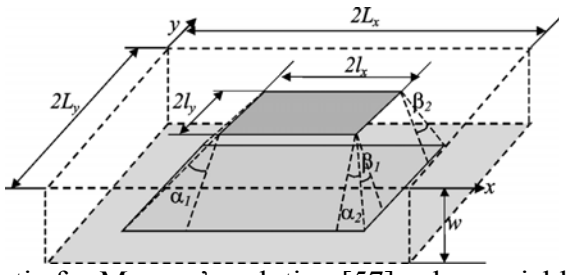


Figure 69. The schematic for Masana's solution [57], a.k.a variable angle model (VAM)

$$R_{\text{th}} = \frac{1}{4kl_x}\frac{1}{(\gamma_e \tan\alpha - \tan\beta)}\ln\frac{l_x + w\tan\alpha}{l_x + w\tan\beta/\gamma_e} \tag{4.2}$$

$$\begin{aligned}(\tan\alpha)_i &= \frac{(\tan\alpha_1 + \tan\alpha_2)_i}{2} \\ &= \left(1 + \frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_x^2}\right)\frac{w_n + [\rho_S/(1+\rho_S)]l_{xn}}{w_n + [1/(1+\rho_S)]l_{xn}}\Bigg|_i \\ (\tan\beta)_i &= \frac{(\tan\beta_1 + \tan\beta_2)_i}{2} \\ &= \left(1 + \frac{1-\rho_L}{1+\rho_L}\frac{l_{xn}}{\varepsilon_y^2}\frac{\gamma_e}{\gamma_s}\right)\frac{w_n + [\rho_S/(1+\rho_S)]l_{xn}\gamma_e}{w_n + [1/(1+\rho_S)]l_{xn}\gamma_e}\Bigg|_i\end{aligned} \tag{4.3}$$

$$\rho_S = \frac{k_i}{k_{i+1}}; \quad \rho_L = \frac{k_i}{k_L} \tag{4.3}$$

$$\varepsilon_x = \frac{\sqrt{L_{x1}L_{x2}}}{L_x}; \qquad \varepsilon_y = \frac{\sqrt{L_{y1}L_{y2}}}{L_y} \tag{4.4}$$

where $\gamma_e = l_y/l_x$ and $\gamma_s = L_y/L_x$, k_i and k_{i+1} is the thermal conductivity of the present and next layer respectively, k_L is thermal conductivity of the lateral boundary of the system, and $l_{xn} = l_x/L_x$ and $w_n = w/L_x$. Although this method is fairly accurate in most cases, it gives large errors if a layer with very small thermal conductivity exists among the multi-layers. If we have simple analytical solution for four-layer problem, we can analyze the system more precisely. Therefore, exact analytical solution of a four-layer problem was derived and compared with other solutions. We solved the multi-layer structure with circular disks instead of rectangular disks because the problem is simplified into two-dimensional problem due to circular symmetry.

4.4.2 Analytical Solution for Spreading Resistance of four-layer Circular Disk

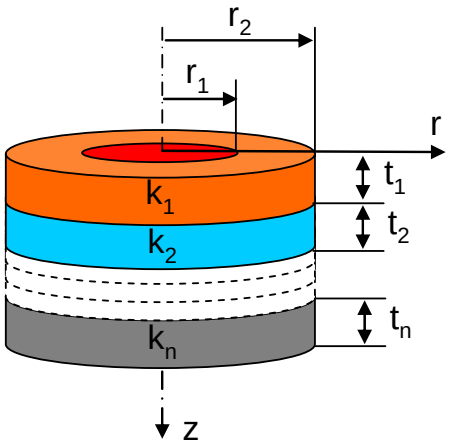


Figure 70. The schematic of multi-layer circular disk

We assume that each i^{th} layer of the disk is a homogeneous solid of isotropic media, and no heat generation is inside the cylinder. Therefore, the temperature distribution must satisfy the Laplace equation;

$$\nabla^2 T_i(r,z,\theta) = 0 \tag{4.6}$$

Due to circular symmetry, Equation 4.6 can be written with only two variables

$$\frac{\partial^2 T_i}{\partial r^2} + \frac{1}{r}\frac{\partial T_i}{\partial r} + \frac{\partial^2 T_i}{\partial z^2} = 0 \tag{4.7}$$

The appropriate boundary conditions are summarized as follows;

$$\left.\frac{\partial T_i}{\partial r}\right|_{r=r_2} = 0 \qquad 0 < z < z_n \tag{4.8}$$

$$T_n(r,z_n) = 0 \qquad 0 < r < r_2 \tag{4.9}$$

$$\left.\frac{\partial T_1}{\partial z}\right|_{z=0} = \begin{cases} -q''/k_1 & 0 < r < r_1 \\ 0 & r_1 < r < r_2 \end{cases} \tag{4.10}$$

$$T_i(r,z) = T_{i+1}(r,z) \qquad z = z_i, \quad i = 1,2,\ldots,n \tag{4.11}$$

$$k_i \frac{\partial T_i}{\partial z} = k_{i+1} \frac{\partial T_{i+1}}{\partial z} \qquad z = z_i, \quad i = 1, 2, ..., n \tag{4.12}$$

where $z_n = t_1 + t_2 + \ldots + t_n$. The solution for this problem can be obtained by separation of variables in Equation 4.7, and the total thermal resistance of this multi-layer becomes

$$R_{th} = \frac{1}{\pi r_2^2}\left(\sum_{i=1}^{n} \frac{t_i}{k_i}\right) + \frac{2}{k_1 \pi r_1} \sum_{l=1}^{\infty} \frac{J_1\left(\frac{r_1}{r_2}\alpha_l\right)}{\alpha_l^2 J_0^2(\alpha_l)} \varphi_n \tag{4.13}$$

where α_l is the roots of the zero-order Bessel function, $J_0(x)$; the summation is conducted over ascending values of α_l. The details of derivation are shown in APPENDIX B. α_l is approximated using Stokes approximation [52, 58]. A modified Stokes approximation is

$$\alpha_l = \frac{\beta_l}{4}\left(1 - \frac{6}{\beta_l^2} + \frac{6}{\beta_l^4} - \frac{4716}{5\beta_l^4} + \frac{3,902,418}{70\beta_l^4}\right) \tag{4.14}$$

where $\beta_l = \pi(4l+1)$ and $l \geq 1$. φ_n is determined by total number of layers, n, and it can be calculated using following relationship

$$\varphi_1 = \tanh(t_1 \lambda_l) \tag{4.15}$$

$$\varphi_2 = \frac{\frac{\tanh(t_1\lambda_l)}{k_1} + \frac{\tanh(t_2\lambda_l)}{k_2}}{\frac{1}{k_1} + \frac{\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)}{k_2}} \tag{4.16}$$

$$\varphi_3 = \frac{\frac{\tanh(t_1\lambda_l)}{k_1} + \frac{\tanh(t_2\lambda_l)}{k_2} + \frac{\tanh(t_3\lambda_l)}{k_3} + \frac{k_2}{k_1 k_3}\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)}{\frac{1}{k_1} + \frac{\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)}{k_2} + \frac{\tanh(t_1\lambda_l)\tanh(t_3\lambda_l)}{k_3} + \frac{k_2}{k_1 k_3}\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)} \tag{4.17}$$

$$\varphi_4 = \frac{\left[\begin{array}{l} \dfrac{\tanh(t_1\lambda_l)}{k_1}+\dfrac{\tanh(t_2\lambda_l)}{k_2}+\dfrac{\tanh(t_3\lambda_l)}{k_3}+\dfrac{\tanh(t_4\lambda_l)}{k_4} \\ +\dfrac{k_2}{k_1k_3}\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)+\dfrac{k_2}{k_1k_4}\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)\tanh(t_4\lambda_l) \\ +\dfrac{k_3}{k_1k_4}\tanh(t_1\lambda_l)\tanh(t_3\lambda_l)\tanh(t_3\lambda_l)+\dfrac{k_3}{k_2k_4}\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)\tanh(t_4\lambda_l) \end{array}\right]}{\left[\begin{array}{l} \dfrac{1}{k_1}+\dfrac{\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)}{k_2}+\dfrac{\tanh(t_1\lambda_l)\tanh(t_3\lambda_l)}{k_3}+\dfrac{\tanh(t_1\lambda_l)\tanh(t_4\lambda_l)}{k_4} \\ +\dfrac{k_2}{k_1k_3}\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)+\dfrac{k_2}{k_1k_4}\tanh(t_2\lambda_l)\tanh(t_4\lambda_l)+\dfrac{k_3}{k_1k_4}\tanh(t_3\lambda_l)\tanh(t_4\lambda_l) \\ +\dfrac{k_3}{k_2k_4}\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)\tanh(t_4\lambda_l) \end{array}\right]} \tag{4.18}$$

where $\lambda_l = \alpha_l / r_2$. When calculating the thermal resistance, as discussed previously, we used the maximum temperature of the top surface, $T_1(0,0)$, rather than the average temperature of heat flux area. In Equation 4.13, the first term is 1D thermal resistance, and the second term represents a constraint by reduced heat flux area—spreading resistance. Similarly, we can get the solution of infinite plates with circular heat source and it can be expressed as follows;

$$R_{th} = \frac{1}{k_1\pi r_1}\int_0^\infty \frac{J_1(r_1\lambda)}{\lambda}\varphi_n d\lambda \tag{4.19}$$

where φ_n can be obtained from previous solution by substituting λ in place of λ_l. The solution of the infinite plates can be assumed as lower limit of thermal resistance when considering the effect of substrate area size.

To validate this solution, it was compared with FEA and other analytical solutions (see Figure 71). Thermal resistances were calculated as a function of copper thickness with fixed substrate size, and also calculated as a function of substrate size with fixed copper thickness. Two different geometries were used for FEA; circular heat source with circular substrate, and the same size of square heat source and square substrate. FEA results of two different geometries match exactly. Also current analytical solution agrees well with the FEA result. Although Masana's solution gives fairly accurate results in DBC substrates, it shows large mismatch in IMS. This is because heat tends to spread wider before the layer that has very low thermal conductivity and the spreading shape becomes non-linear. Also Yovanovich's solution can provide thermal resistance of DBC substrate roughly. Masana's and Yovanovich's solutions can be used with wider application regardless of the shape and placement of the heat source and substrate. However, the current analytical solution gives the best description of the thermal spreading resistance of the multi-layer substrate, up to four layers, with centered heat source.

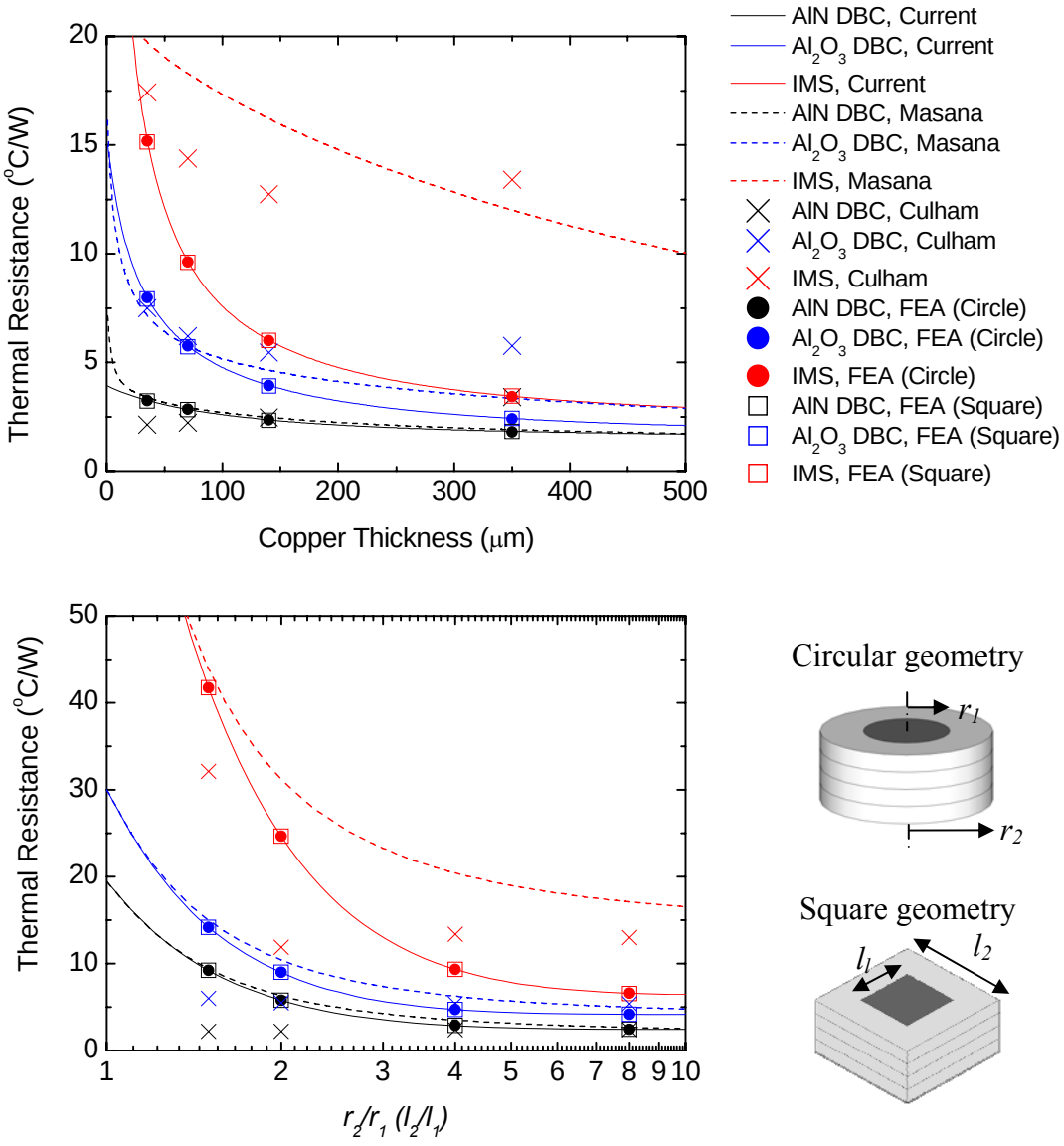


Figure 71. The validation of thermal circuit model of substrate with TIM. 1 mm^2 heat source is placed at the center of substrate. Fixed substrate size, 1 cm^2, used for the first plot and fixed copper thickness, 127 μm, for the second plot. Three different substrates are used; AlN DBC, Al_2O_3 DBC, and IMS. 381 μm of ceramic was used for DBC, and 75 μm of dielectric and 1000 μm of base for IMS. Uniform heat flux at top surface and uniform temperature at bottom surface were assumed. FEA with two different geometries was used.

We need to verify that the analytical model of substrate and TIM works well inside the entire system; i.e. validation of the assumptions that the heat flux on the top of the substrate and the temperature of the bottom of TIM are uniform. The thermal

resistance of substrate calculated by our analytical solution is compared with the FEA results conducted on entire system (see Figure 72). Our analytical solution describes the thermal behavior of the substrate inside the system as well as substrate alone very well. Therefore, we can study the characteristic of each layer with different parameters by utilizing current solution.

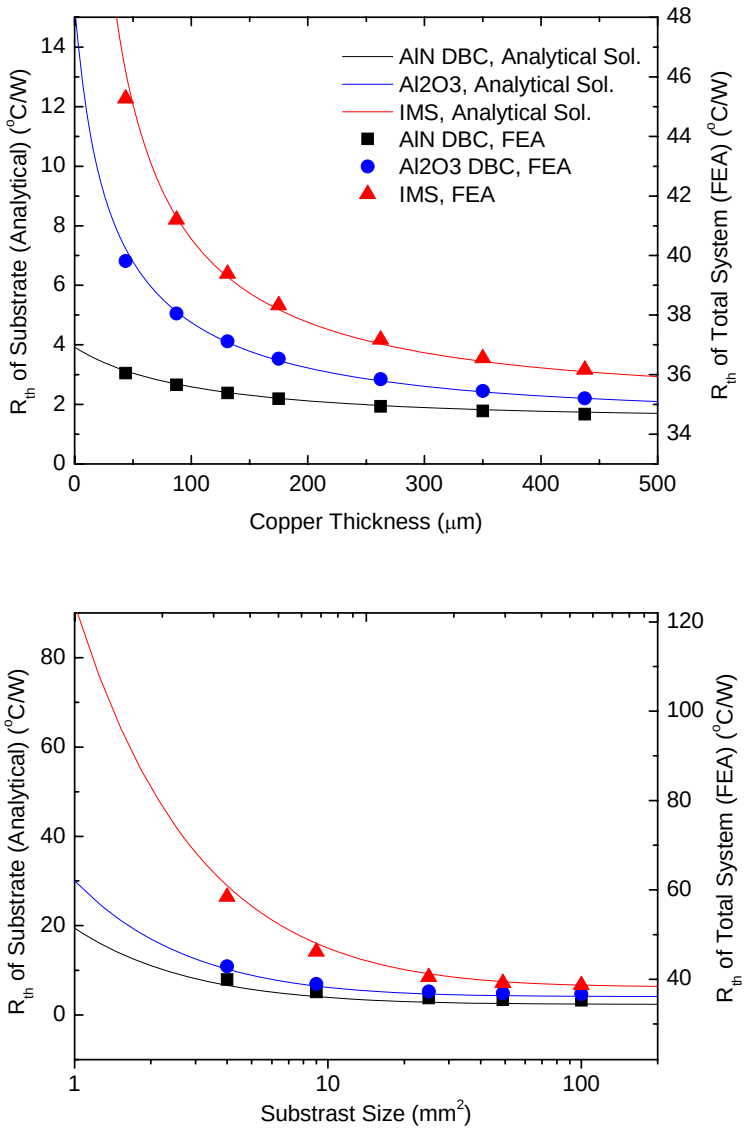


Figure 72. The validation of thermal resistance model. Comparison between analytical model and FEA with entire system. Analytical model used the conditions shown in Figure 71, and FEA model used that shown in Figure 36. Left and right y-axis has the same scale.

4.4.3 Thermal Characterizations of Power Electronic Substrates

4.4.3.1 DBC Substrates

We studied the effect of copper thickness of DBC substrates on the thermal resistance (see Figure 73). Due to heat spreading through copper layer, lower thermal resistance can be obtained with thicker copper layer.

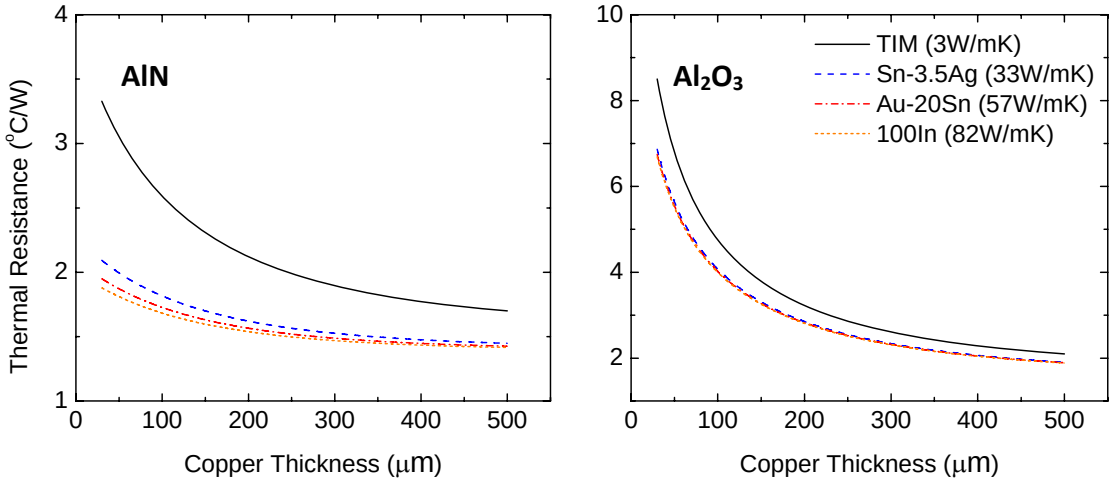


Figure 73. Thermal resistance of DBC as a function of copper thickness. 1mm^2 heat source is placed at the center of 1 cm^2 substrate. 381 μm of ceramic 50 μm of solder or TIM was used.

From the result we can notice that the difference of the thermal resistance is negligible regardless of types of TIMs. Also, the difference is less than 1.5°C/W if 3-W/mK of TIM is used. This is because there is sufficient heat spreading in the DBC substrate and the heat flux drops sufficiently after passing through the substrate. Therefore, we do not need to use very high thermal conductivity solder to attach the substrate to the heat sink or to other structures. Also, soldering large area without void requires very elaborate process and may cause high stress or failure. In this case, we can use thermal grease or thermal tape instead of solder with slight increase of thermal resistance of the system. Also, we can notice that the thermal resistance of the DBC substrate largely depends on the ceramic and the thickness of copper. In the case of AlN

DBC substrate, thermal resistance is around 2°C/W with a 35 μm copper layer and the difference of thermal resistance between thin and thick copper layer is very small. For example, the difference of the thermal resistance between 35 μm and 500 μm of copper layers is less than 0.4°C/W. This is because of the high thermal conductivity of AlN. While in case of Al_2O_3 DBC, a thicker layer of copper is required to reduce thermal resistance.

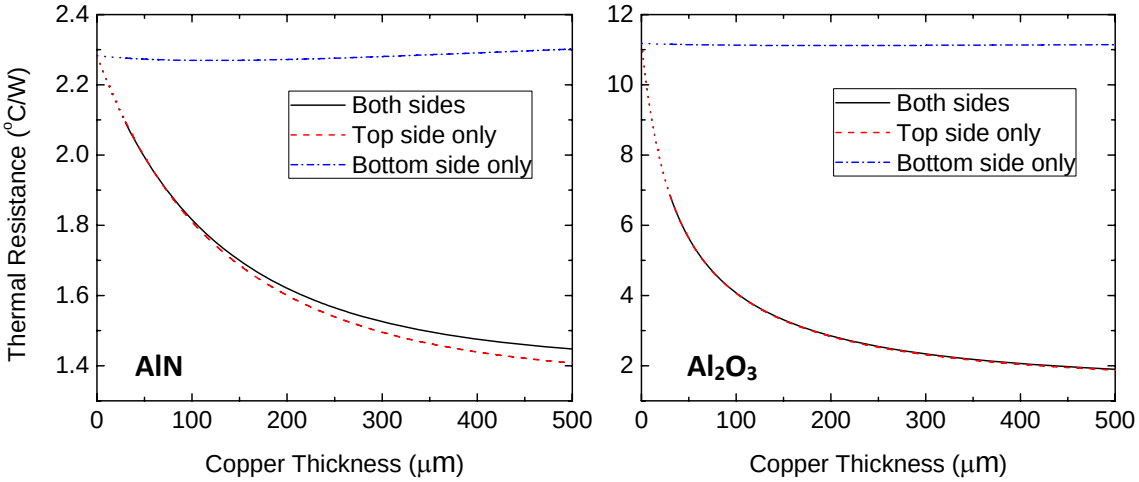


Figure 74. Thermal resistance of DBC as a function of copper thickness. The same design and condition with Figure 73 and Sn-3.5Ag solder was used as TIM. The copper thickness of each side was changed respectively and the results were compared to the result when both sides were changed.

With this result, it is not clear which layer has more impact on lowering thermal resistance between top and bottom copper layer because the thicknesses of both sides of DBC substrate are changed equally. Therefore, the copper thickness of the top, the bottom, and both sides were changed respectively and the results were compared in Figure 74. It shows that the change of thermal resistance mostly depends on top side copper thickness, and the role of the bottom side copper is negligible. However, we still need the bottom side copper layer in order to prevent the failure of substrate from stresses due to CTE mismatch.

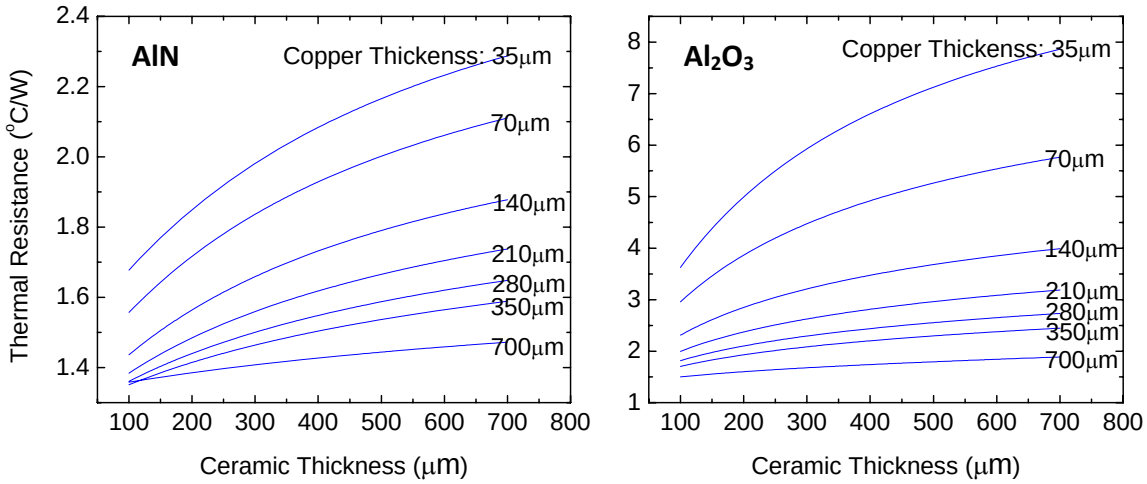


Figure 75. Thermal resistance of DBC as a function of ceramic thickness. 1mm^2 heat source is placed at the center of 1 cm^2 substrate. 50 μm of Sn-3.5Ag is used for TIM.

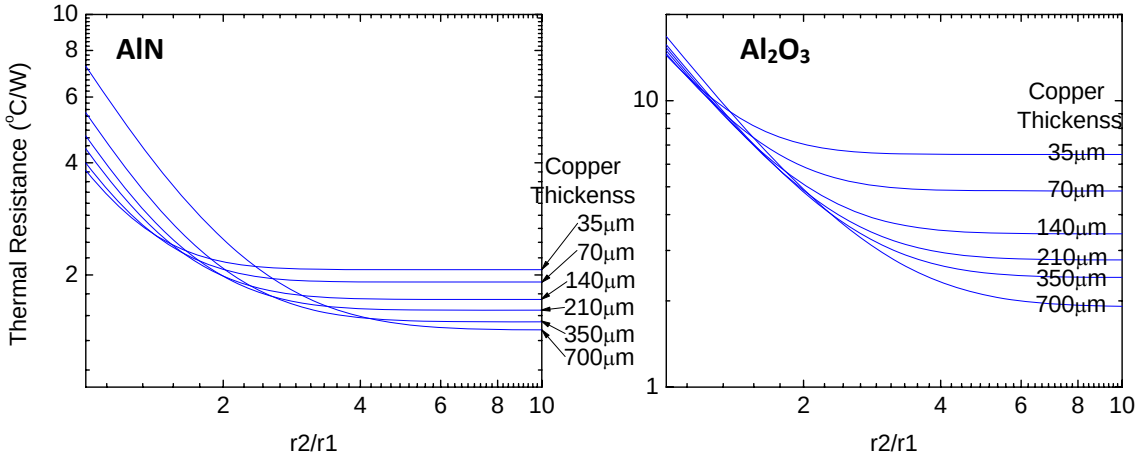


Figure 76. Thermal resistance of DBC as a function of substrate size. 1mm^2 heat source is placed at the center of substrate. 381 μm of ceramic is used and 50 μm of Sn-3.5Ag for TIM.

Thermal resistances of DBC were also studied as a function of ceramic thickness and as a function of substrate size (see Figure 75 and Figure 76). Thermal resistance of substrate increases as ceramic thickness increases, and the gradient becomes smaller as copper thickness increases due to heat spreading. However, the difference is so small for AlN DBC that any thickness of copper and ceramic can be used. Also, if we use a thick copper layer for Al_2O_3 DBC, the thickness of ceramic does not matter and it can be

determined by other factors such as breakdown voltage and stresses induced or handled by the substrate. Figure 76 shows that heat spreading area becomes larger as thickness of the copper increases. Considering that more than 300 μm of copper is not used typically due to high cost and difficulty of process, a substrate, which has 4 times radius of heat spreading with a 1mm^2 heat source, is used.

4.4.3.2 Characteristics of IMS

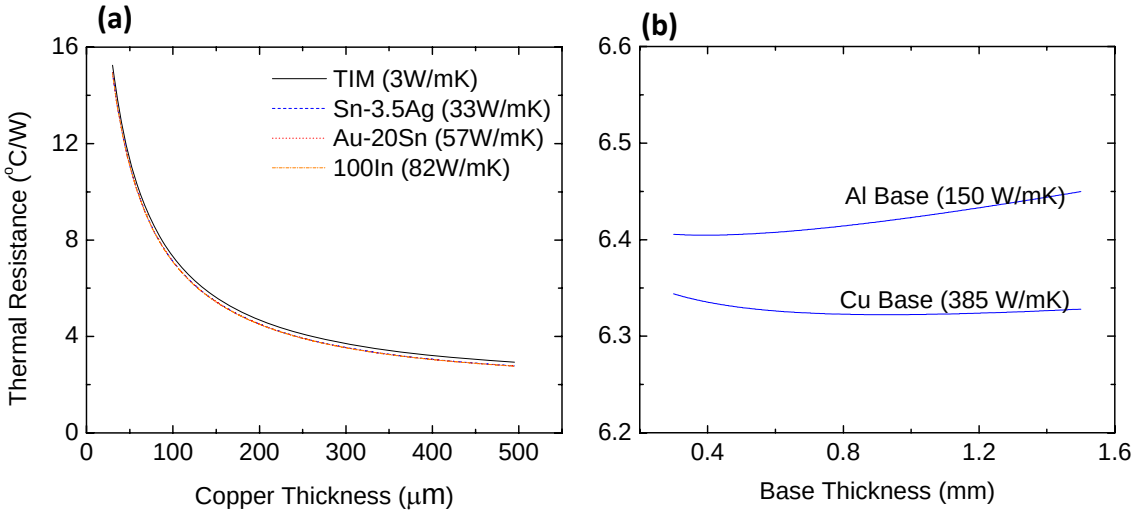


Figure 77. (a) Thermal resistance of IMS as a function of copper thickness. 1mm^2 heat source is placed at the center of 1 cm^2 substrate. 75 μm and 1.1 W/mK of dielectric and 50 μm of TIM were used. (b) Thermal resistance of IMS as a function of base thickness. 127 μm of copper was used and others are same with previous ones.

Thermal resistances of IMS as a function of copper thickness and as a function of base thickness were calculated (see Figure 77). The thermal resistance difference between 3 W/mK of TIM and 82 W/mK of solder is very small, less than 0.4°C/W. This is less than DBC substrate and it means that heat spreads wider in IMS than in DBC substrate. Therefore, when we attach IMS onto a heat sink, we do not need to use high price and difficult-to-process solders. Like DBC substrates, the thermal resistance decreases as the copper thickness increases. The thickness of copper in IMS is a more

critical factor to reduce the thermal resistance than seen in DBC. The thickness of bottom metal layer, called base layer, has little contribution to spreading heat. The thermal resistance of substrate is nearly independent of the type of base material and thickness of the base layer (see Figure 77). Therefore, the role of base material in IMS is to enhance the robustness of the substrate rather than heat spreading.

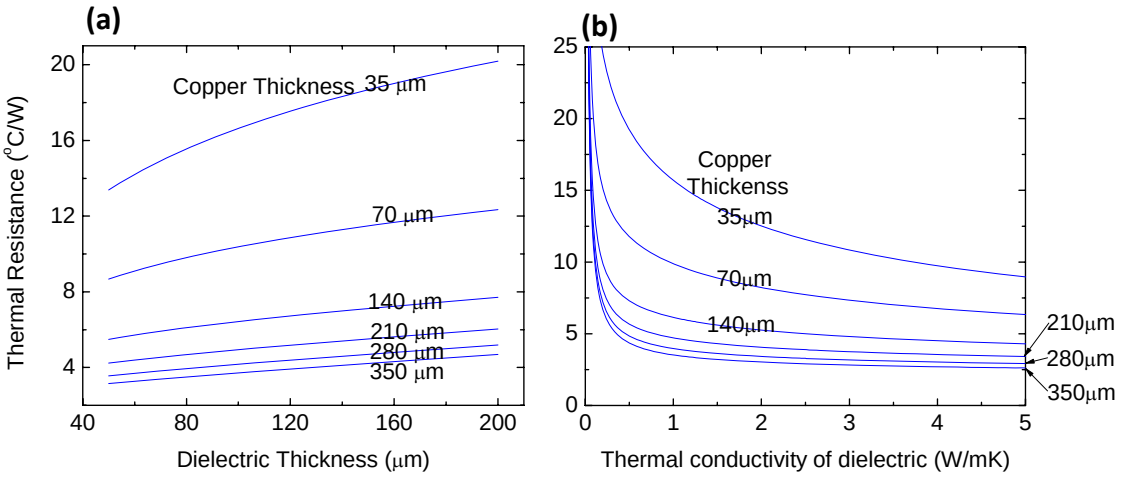


Figure 78. (a) Thermal resistance of IMS as a function of dielectric thickness. 1mm^2 heat source is placed at the center of 1 cm^2 substrate. 1.1 W/mK of dielectric and 3-W/mK and 50 μm of TIM were used. (b) Thermal resistance of IMS as a function of thermal conductivity of dielectric. 75 μm of dielectric was used and others are same with previous one.

In Figure 78 (a), thermal resistance of IMS increases almost linearly as dielectric thickness increases. This can be explained as follows; due to very low thermal conductivity of dielectric, heat barely spreads in dielectric. Therefore, heat flux in dielectric can be assumed as one-dimensional heat flow with heat flux area determined by heat spreading in copper layer. Also, slightly curved lines with thin copper layer are shown. This is because heat does not spread in copper layer and heat spreading effect occurs in dielectric layer; however the effect is very small. By using thick copper layer, we can exclude the effect of the low thermal conductivity of dielectric. For example, when 210 μm of copper layer is used, the thermal conductivity difference between 1-

W/mK and 5 W/mK dielectrics is only 1.3°C/W. However, very low thermal conductivity dielectric should be avoided (see Figure 78)

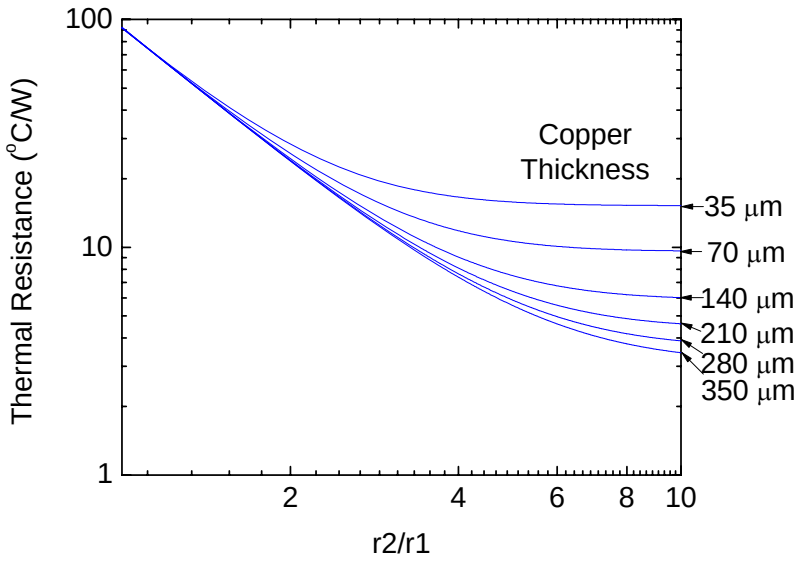


Figure 79. Thermal resistance of IMS as a function of substrate size. 1mm^2 heat source is placed at the center of substrate. 75 μm and 1.1 W/mK of dielectric and 50 μm and 3-W/mK of TIM are used.

The thermal resistance as a function of substrate size was calculated and shown in Figure 79. Due to very low thermal conductivity of dielectric, heat tend to spread wider than DBC. Therefore wider area size is needed for IMS than DBC to take advantage of thick copper.

4.4.4 Size Effect of Copper Circuit Layer

So far, we assumed that the copper circuit layer has the same size with a substrate. Although this assumption is reasonable because practically the etched area of copper circuit layer in power electronic substrate is as small as possible (see Figure 51), it is not always acceptable. Therefore, we will consider smaller size of copper circuit layer than

that of substrate. Since heat spreading mainly occurs in copper circuit layer, its size could be critical factor in determining the thermal resistance of the substrate and TIM.

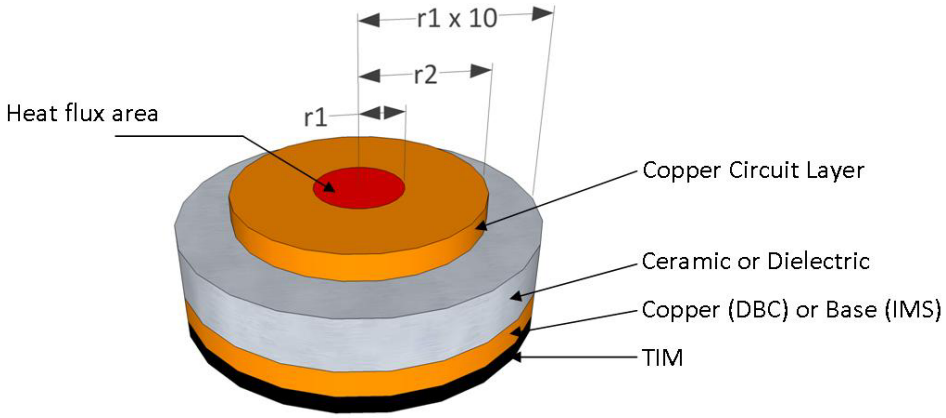


Figure 80. The schematic of substrate and TIM with reduced size of copper circuit layer. The heat flux area is 1 mm^2 and the size of substrate is fixed as 100 mm^2. The radius of copper circuit layer is defined as r_2.

The geometry shown in Figure 80 is used for FEA. The same geometry is also used for the analytical solution but r_2 assumed as substrate size. The results are compared and plotted in Figure 82. In the case of AlN DBC substrate, the lateral size of copper circuit layer does not show any effect on the thermal resistance. Contrarily, in case of IMS, the size of copper circuit layer behaves like the size of substrate. That is to say, IMS should have enough large copper circuit layer for proper thermal management while AlN DBC substrate does not need it. The thermal resistance of Al_2O_3 DBC substrate is slightly affected by the size of the copper circuit layer.

From the result we need to be careful when designing copper circuit layer of IMS. To maximize the advantage of IMS, the lateral size of copper circuit pattern should be as large as possible. Also, when heat does not spread enough due to small copper circuit layer, the effect of thermal conductivity of dielectric on the thermal resistance becomes larger. An example is shown in Figure 81. If the copper circuit layer is large enough, r_1/r_2 is 6, the thermal resistance difference between substrates with two different dielectrics is only 1.8°C. However, if r_2/r_1 is 1.5, the difference becomes 14°C.

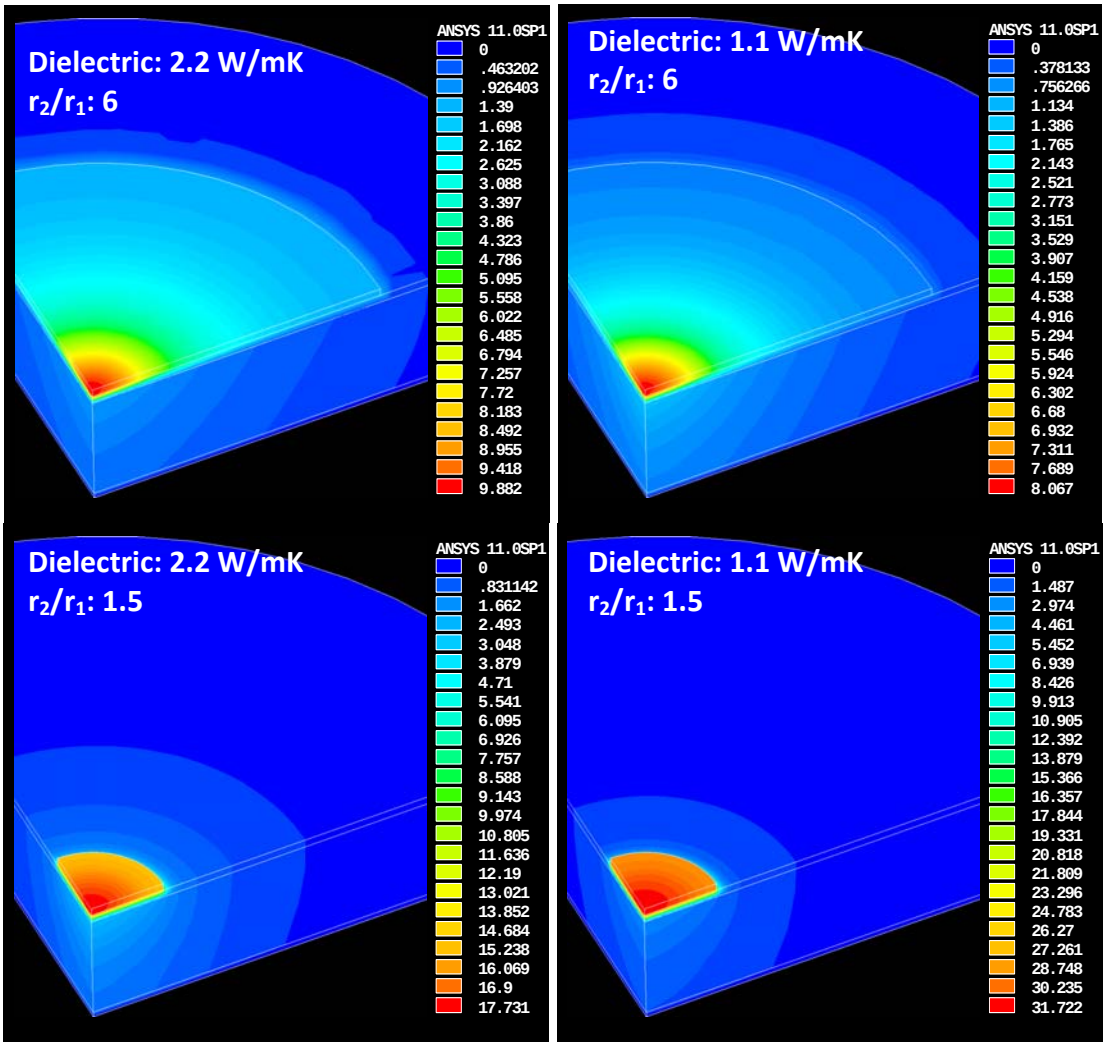


Figure 81. The contour plots of temperature distribution in IMS. The heat flux area is 1-mm^2 and the size of substrate is fixed as 100 mm^2. The radius of copper circuit layer is defined as r_2. The thickness of copper, dielectric, and base is 70 μm, 75 μm, and 1 mm, respectively. 381 μm ceramic is used for DBC substrate. 75 μm and 1.1 W/mK dielectric and 1mm Al-base are used for IMS. 50 μm and 3 W/mK thermal grease is used for TIM. The result shows that the effect of thermal conductivity of dielectric becomes larger when the size of copper circuit layer.

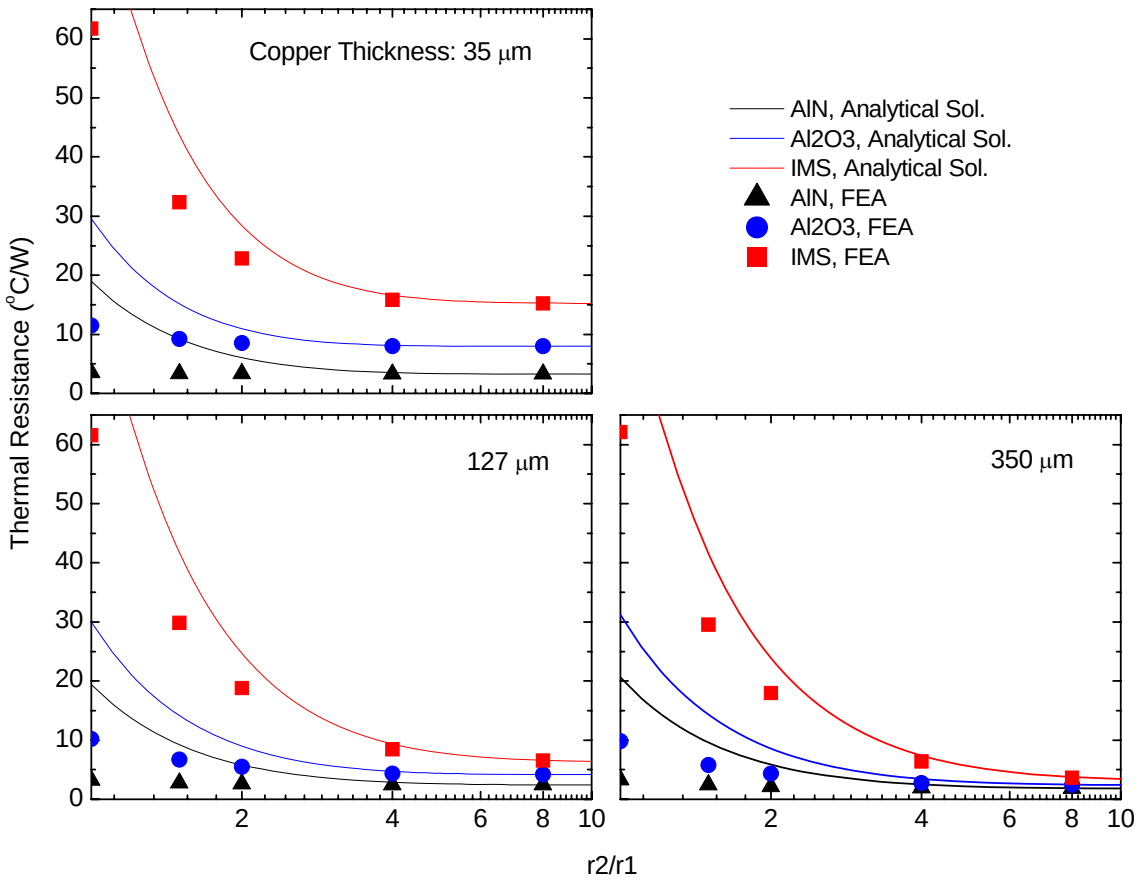


Figure 82. Thermal resistance as a function of r_2/r_1. In analytical solutions, copper circuit layers, which have the radius r_2, are considered as substrate size. 381 μm ceramic is used for DBC substrate. 75 μm and 1.1 W/mK dielectric and 1 mm Al-base are used for IMS. 50 μm and 3 W/mK thermal grease is used for TIM.

4.4.5 TIM

The thermal resistance of TIM as a function of the thermal conductivity and the thickness of TIM was investigated. However, since the thermal resistance of TIM is subject to the heat spreading in the substrate level, i.e. the type of the substrate, the thermal resistance of TIM together with the specific substrate was investigated.

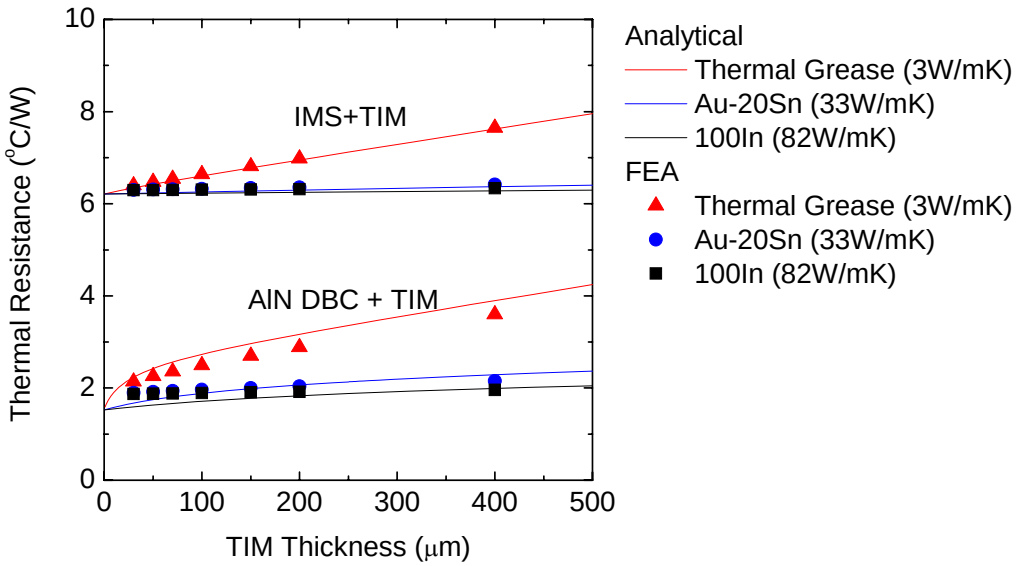


Figure 83. The thermal resistance of substrate and TIM as a function of the TIM thickness. The results between analytical model and FEA with entire system are compared. The simulation conditions shown in Figure 36 except TIM were used. When estimating the thermal resistance from the FEA result, 3.9 W/mK is used for die and die-attach, and 29.1 W/mK for IMS and 28.3 W/mK for AlN DBC substrate.

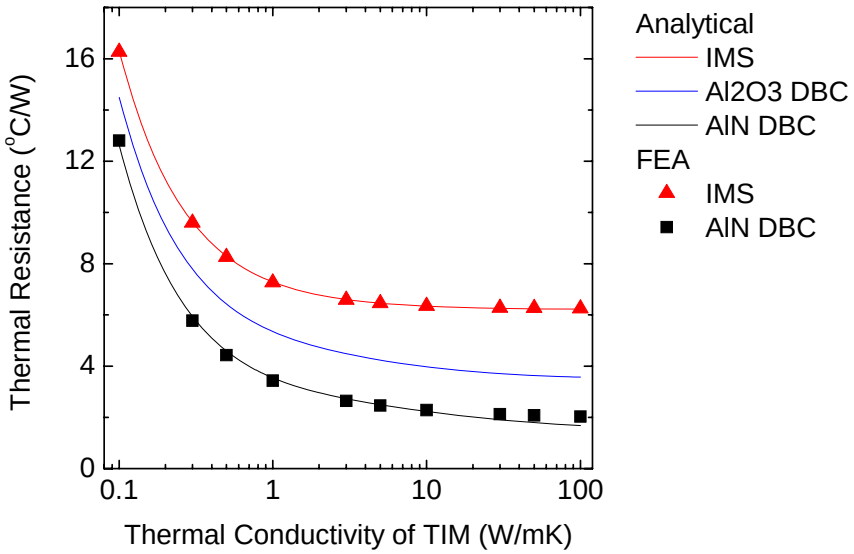


Figure 84. The thermal resistance of substrate and TIM as a function of the thermal conductivity of TIMs. The results between analytical model and FEA with entire system are compared. The simulation conditions shown in Figure 36 except TIM were used. TIM thickness is 100 μm. When estimating the thermal resistance from the FEA result, 3.9 W/mK is used for die and die-attach, and 29.1 W/mK for IMS and 28.3 W/mK for AlN DBC substrate.

The effect of TIM thickness on the thermal resistance is shown in Figure 83. The results between the analytical and FEA solutions agree very well. The thermal resistance with respect to the TIM thickness is almost linear. In case of the AlN DBC substrate, the heat spreading characteristic is slightly subject to the thickness of TIM due to high thermal conductivity of the substrate. Therefore, the slight mismatch is shown between the Analytical and FEA result. The effect of the thermal conductivity of TIM on the thermal resistance is shown in Figure 84. The results between the analytical and FEA solutions agree very well, also. Although the characteristic varies with the type of a substrate and its thickness, the effect of the thermal conductivity of TIM on the thermal resistance is negligible if the conductivity is larger than 1 W/mK. For example, when considering the general thickness of TIM is less than 100 μm, the thermal resistance difference between using 1 W/mK of TIM and 100 W/mK of TIM is only 1.5°C/W. This is only valid with enough heat spreading in substrate level. Therefore, when we attach the power electronic substrate to a heat sink, the thermal conductivity of TIM used between the substrate and TIM is not the important factor to reduce the thermal resistance of the system.

4.5 Heat sink

The thermal resistance of a heat sink can be easily estimated by using the result of the FEA. From Table 16, the thermal resistances of the heat sink with three different substrates are 29.57°C/W, 29.59°C/W, and 29.31°C/W, respectively. It seems that the thermal resistance of the heat sink is hardly affected by the structure mounted on it. Therefore, it is possible to estimate the thermal resistance of the heat sink by FEA and to use it for other analytical modeling that uses the same heat sink. Also, it can be determined more accurately by a computational fluid dynamics (CFD) program or by an

experiment. Although these methods give the accurate result of the specific geometry and condition, an analytical solution provides general understanding of thermal performance with respect to each parameter. For the analytical study, we also assume uniform convection heat transfer coefficient around the heat sink. Two steps of calculations are required for the analytical modeling of a heat sink. One is the thermal resistance without heat spreading effect and the other is spreading resistance in a base plate. In case of simple geometry such as straight fin array shown in Figure 85(a), the thermal resistance without heat spreading effect is easily estimated by using overall surface efficiency relation shown in Equation 4.20 [34].

$$R_{Heatsink} = \frac{1}{\eta_o h A_t} \tag{4.20}$$

where $\eta_0 = 1-(NA_f/A_t)(1-\eta_f)$, $A_t = NA_f+A_b$, $\eta_f = \tanh(mL_c) / mL_c$, $L_c = L+t/2$, $A_f = 2\omega L_c$, $m = (2h/kt)^{1/2}$, N is the number of fins in the array, and A_b is the area of the prime surface.

$$h_{eff} = \frac{1}{R_{Heatsink} A_b} \tag{4.21}$$

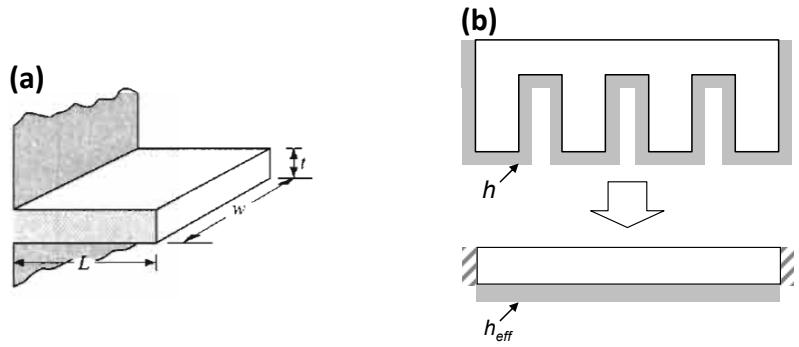


Figure 85. (a) A straight fin, (b) conversion of h into h_{eff}

To estimate the thermal spreading resistance in a base layer of a heat sink, we need to convert the convection heat transfer coefficient, h, into the effective convection heat transfer coefficient, h_{eff}, which can be done with Equation 4.21.

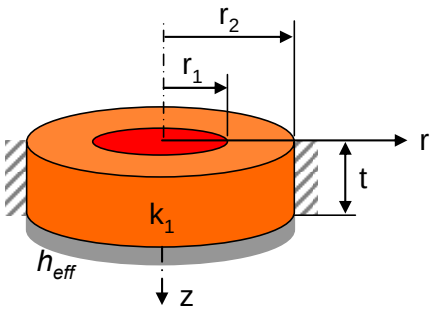


Figure 86. The schematic for heat spreading effect in one layer of circular disk. The red circle with radius r_1 is the area of the uniform heat flux, and the other side is convection heat transfer.

Like the previous solution of the substrate, if the heat source is placed at the center, the solution of circular disk is the exactly same with that of square one. Therefore, the three-dimensional problem can be simplified into two-dimensional one due to circular symmetry. It is solved by Yovanovich et al [54] and the modified solution is shown in Equation 4.23.

$$R_{th} = \frac{1}{\pi r_2^2}\left(\frac{t}{k}+\frac{1}{h_{eff}}\right)+\frac{2}{k\pi r_1}\sum_{l=1}^{\infty}\frac{J_1\left(\frac{r_1}{r_2}\alpha_l\right)}{\alpha_l^2 J_0^2(\alpha_l)}\frac{\frac{\alpha_l}{Bi}+\tanh\left(\frac{t}{r_2}\alpha_l\right)}{1+\frac{\alpha_l}{Bi}\tanh\left(\frac{t}{r_2}\alpha_l\right)} \tag{4.22}$$

where $Bi=h_{eff}\times t/k$. The thermal resistance of the heat sink as a function of the area size of the heat flux is estimated by FEA and analytical solution and plotted in Figure 87. There is a mismatch between FEA and analytical solution because analytical solution does not account for the edge cooling. If we neglect the edge cooling, the results of both solutions agree very well. The first term of Equation 4.23 is the thermal resistance of the heat sink without spreading resistance, which means that the heat flux area is the entire surface of the top of the heat sink, and it is shown in Figure 87 as dashed line. The second summation term is the thermal spreading resistance and the total thermal resistance is shown in Figure 87 as solid line. Although the thermal spreading resistance becomes

very large when the heat flux area is very small, it becomes negligible, less than 0.5°C, if the heat flux area is larger than 50 mm^2.

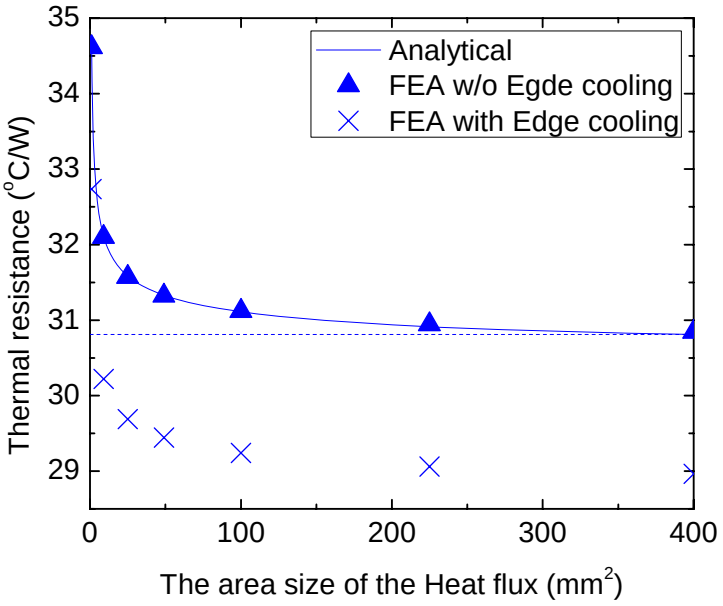


Figure 87. The thermal resistance of a heat sink as a function of the area size of the heat flux. The geometry of the heat sink shown in Figure 29 was used.

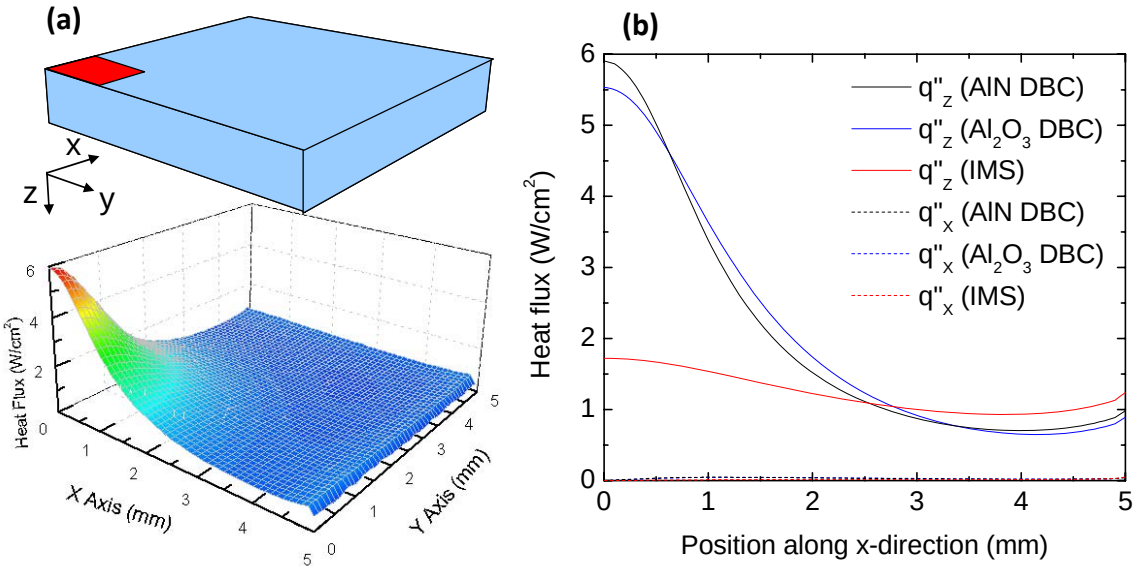


Figure 88. Heat flux at the interface between TIM and the heat sink. (a) Three-dimensional plot of q''_z (AlN DBC) and (b) two-dimensional plot. The conditions shown in Figure 36 were used.

The issue in using the analytical solution of the heat sink is the heat flux area at the top of the heat sink. It is very difficult to determine analytically because it varies with the structure on the heat sink and is not even uniform. The actual heat flux between TIM and the heat sink is shown in Figure 88. Nevertheless, we can roughly determine the heat flux area by the comparison between FEA and analytical result. The equivalent areas of the heat on top of the heat sink with DBC substrate and with IMS are from 30 to 40 mm^2 and from 75 to 85 mm^2, respectively. As mentioned previously, the thermal spreading resistance in the heat sink is remarkable only if the heat flux area is very small. Therefore, the thermal spreading resistance in the heat sink is not significant with DBC substrate and IMS.

4.6 Summary

We divided the system into three components—die and die-attach, substrate and TIM, and a heat sink. We also made assumptions at the interfaces between the components to analyze each component separately. The analytical expression of each component was derived and compared with FEA result to validate it. Although slight disagreement exists between FEA and analytical methods, they agree well. The analytical solutions give good understanding on thermal resistance with respect to each parameter as well. The solution of heat spreading in muti-layer, which was derived through this study, gives very accurate result under certain geometry and condition. Masana's solution[57] has much wider application; unlimited number of layers, rectangular heat source, eccentric heat source, etc. However, when the layer that has very low thermal conductivity exists among the multi-layer, it shows large errors.

CHAPTER 5

LED ARRAY ANALYSIS AND DEVICE SIMULATIONS

5.1 Array Analysis

Since the light output of a single LED is considerably lower than other light sources, the total light output must be increased with the use of an array of multiple LEDs. The increased power input and the interference of heat spreading in LED-arrays causes an increase in the junction temperature. Therefore, we need to study the relation between the placement of LEDs and the junction temperature. Also, we need to verify that the thermal characteristics that we studied in the previous chapter are still valid for LED-arrays.

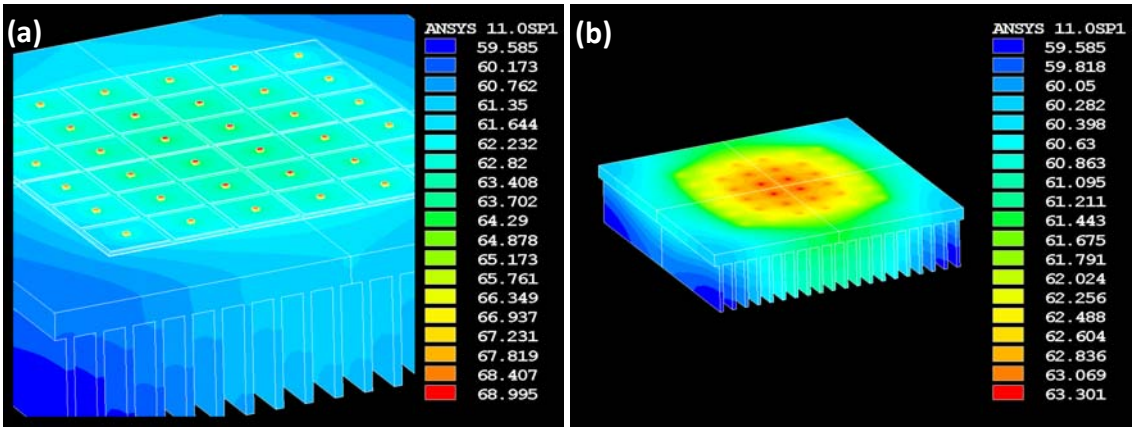


Figure 89. The contour plot of temperature distribution by FEA. (a) Entire structure and (b) only heat sink. The 6 by 6 LED array based on COB structure was modeled. The condition shown in Figure 36(a) is used except the substrate size and the heat sink size. The substrate size is 72 mm×72 mm, and the distance between two adjacent LEDs, pitch, is 12 mm. The base plate of the heat sink is 110 mm×110 mm with 5mm thickness, and 20 straight fins have 1.5 mm thickness and 20 mm height. 1 W power input was applied in each LED.

Firstly, a 6 by 6 LED-array based on COB structure was modeled and analyzed by FEA (see Figure 89). Through the several simulations, we can easily confirm that the

distance between two adjacent LEDs is the key parameter in determining the junction temperature as well as other parameters such as the copper thickness. To obtain a more general understanding, a thermal circuit model of the LED-array was built (see Figure 90). The number of LEDs is *N* and the power input at each LED is the same as q. The thermal resistance of the total system can be estimated by using Equation 5.1.

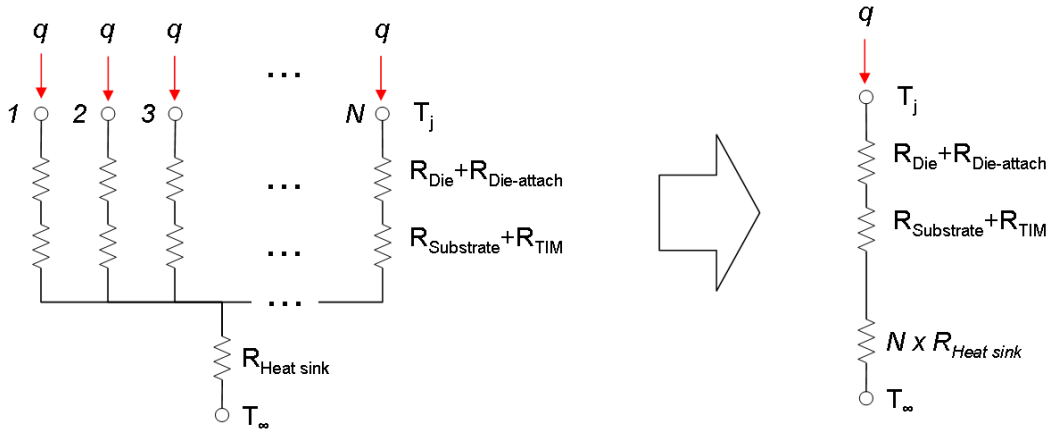


Figure 90. The equivalent thermal resistance model of LED array. If the power used and structure is the same, it can be simplified as the right side.

$$R_{tot} = R_{Die} + R_{Die-attach} + R_{Substrate} + R_{TIM} + N \times R_{Heatsink} \tag{5.1}$$

where R_{Die} and $R_{Die\text{-}attach}$, and $R_{Substrate}$+R_{TIM} can be easily estimated by using Equation 4.1 and Equation 4.13, respectively. When using Equation 4.13, we need to determine r_2, the radius of the substrate. As mentioned previously, in the case of the array, the mid-surface between the LEDs can be assumed adiabatic (see Figure 91). Therefore, if the array is arranged with uniform distance, r_2 can be determined by Equation 5.2.

$$r_2 = \frac{Pitch}{\sqrt{\pi}} \tag{5.2}$$

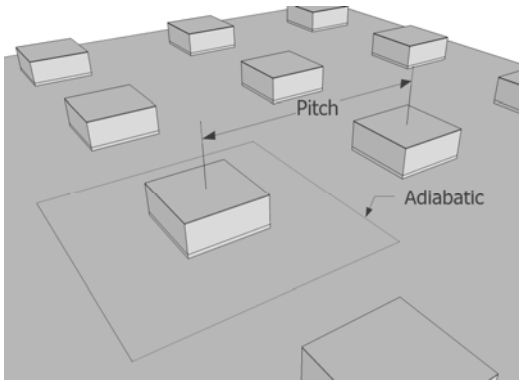


Figure 91. The schematic of the array of multiple LEDs. LEDs are placed evenly in the substrate and the distance between the adjacent LEDs is defined as pitch.

The last term in Equation 5.1, $N \times R_{Heatsink}$, cannot be determined easily because the simple calculation does not account for the thermal spreading resistance affected by the placement of LEDs. For example, the thermal resistance of the heat sink shown in Figure 89 is 1.01°C/W without the thermal spreading resistance. Since 36 LEDs are used, $N \times R_{Heatsink}$ becomes 36.36°C/W. Compared to the thermal resistance of the heat sink by FEA, 38.3°C/W, it is lower than that of FEA by 1.94°C/W. Although not significant in this case, the error becomes larger as the pitch become smaller. The thermal resistance of the heat sink including thermal spreading resistance can be calculated by Muzychka's solution [50] (see Figure 92).

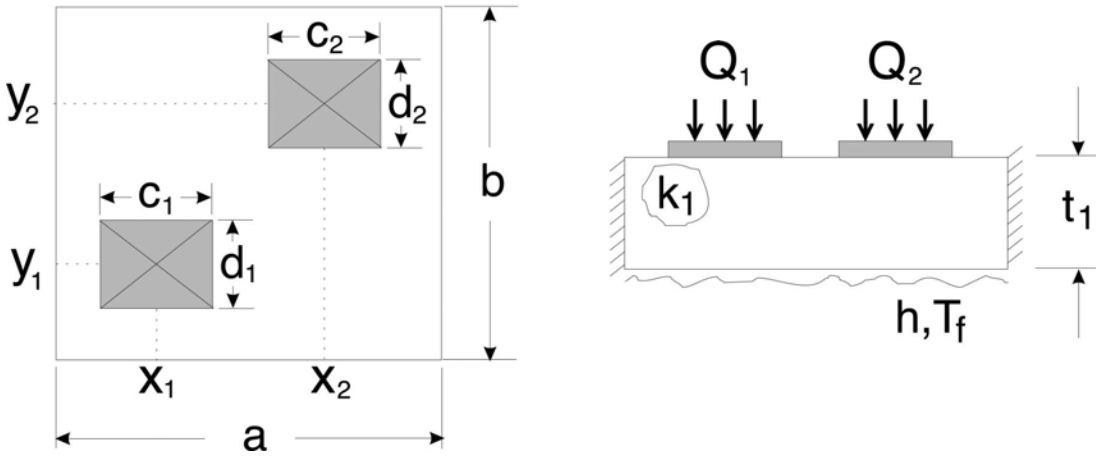


Figure 92. Isotropic plate with eccentric heat source [50]

The solution for the temperature distribution on the heat sink can be obtained using superposition. For N discrete heat sources, the surface temperature distribution is given by

$$T(x,y,0)-T_f=\sum_{i=1}^{N}\theta_i(x,y,0) \tag{5.3}$$

$$\theta_i(x,y,0)=A_0^i+\sum_{m=1}^{\infty}A_m^i\cos(\lambda x)+\sum_{n=1}^{\infty}A_n^i\cos(\delta y)+\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}A_{mn}^i\cos(\lambda x)\cos(\delta y) \tag{5.4}$$

$$A_m^i=\frac{2Q_i\left[\sin\left(\frac{(2x_i+c_i)}{2}\lambda_m\right)-\sin\left(\frac{(2x_i-c_i)}{2}\lambda_m\right)\right]}{abc_ik_1\lambda_m^2\phi(\lambda_m)} \tag{5.5}$$

$$A_n^i=\frac{2Q_i\left[\sin\left(\frac{(2y_i+d_i)}{2}\delta_n\right)-\sin\left(\frac{(2y_i-d_i)}{2}\delta_n\right)\right]}{abd_ik_1\delta_n^2\phi(\delta_n)} \tag{5.6}$$

$$A_{mn}^i=\frac{16Q_i\cos(\lambda_m x_i)\sin\left(\frac{1}{2}\lambda_n c_i\right)\cos(\delta_n y_i)\sin\left(\frac{1}{2}\delta_n d_i\right)}{abc_id_ik_1\beta_{m,n}\lambda_m\delta_n\phi(\beta_{m,n})} \tag{5.7}$$

where $\lambda=\frac{m\pi}{a}$, $\delta=\frac{n\pi}{b}$, $\beta=\sqrt{\lambda^2+\delta^2}$, $\phi(\zeta)=\frac{\zeta\sinh(\zeta t_1)+h_{eff}/k_1\cosh(\zeta t_1)}{\zeta\cosh(\zeta t_1)+h_{eff}/k_1\sinh(\zeta t_1)}$ and ζ is replaced by λ, δ, and β. Since our concern is the maximum junction temperature of the system, if we put the location of *x*, *y* as the center of the innermost LED in the array, the maximum $N\times R_{Heatsink}$ can be obtained by

$$N\times R_{Heat\ sink}=\frac{T(x,y,0)}{\sum_{i=1}^{N}Q_i} \tag{5.8}$$

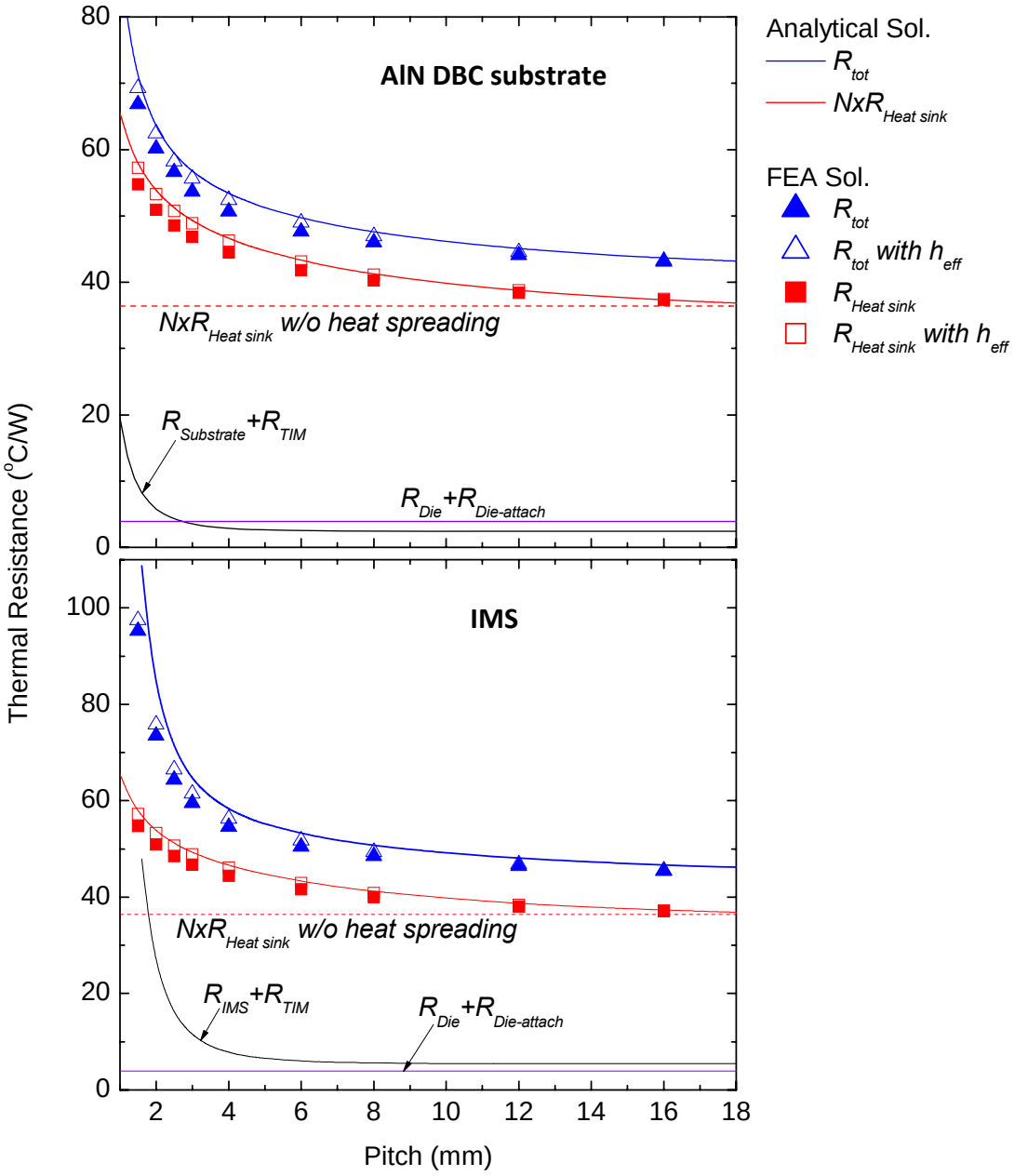


Figure 93. The thermal resistance of LED-array as a function of pitch. Lines are analytical results and symbols are FEA results. The conditions shown in Figure 89 were used for the LED-array with AlN DBC substrate. 127 μm copper, 50 μm and 1.1 W/mK dielectric, and 1 mm Al base is used for IMS.

The thermal resistance of LED-array as a function of pitch was estimated by the analytical method and compared with the FEA result (see Figure 93). The results obtained by two different methods agree well. The total thermal resistance of the system

is the sum of three components. The violet solid line is the thermal resistance of the die and die-attach. Since its geometry and thermal conductivity does not change, it remains constant as 3.9°C/W. The black solid line is the thermal resistance of the substrate. When the pitch is small, the thermal resistance of the substrate is large because the heat does not spread enough. Once the pitch is larger than a certain distance, the restriction of the heat spreading in substrate becomes negligible. Approximately, it is 6 mm for DBC substrate and 9 mm for IMS in this case. From this approximation, we assumed that the heat conducting area is 36 mm^2 between DBC package and the heat sink and 81 mm^2 between IMS package and heat sink. The red solid line is the thermal resistance of the heat sink. The square of the pitch is used as heat flux area if it is smaller than typical heat flux area. The red dashed is the thermal resistance of heat sink without thermal spreading resistance, which means the heat flux area is the entire top surface of the heat sink. It is the lowest thermal resistance of the heat sink. The black solid line is the total thermal resistance of the system and it is the sum of the other three solid lines. There is small mismatch between the analytical and FEA solutions. The FEA result which uses h_{eff} without the fin array of the heat sink agrees fairly well with the analytical solution, while the FEA results with the fin array shows a slightly lower thermal resistance and it becomes much lower as the pitch becomes smaller. This means that the simulations using h_{eff} and h are not the exactly same, and small area of cooling near the heat source is more effective than large area of cooling with an average h.

The pitch of the LEDs in the array is also an important factor in determining the thermal resistance of LED-array. Although the larger pitch can achieve a lower thermal resistance, the pitch is usually determined by considering other factors such as optics. For effective thermal management of the system, we should avoid the interference of heat spreading in the substrate level. It depends on the type of substrate, the thickness of each layer, etc, and typically 4 mm for a DBC substrate and 6 mm for a IMS is in the range of concern for the industrial use.

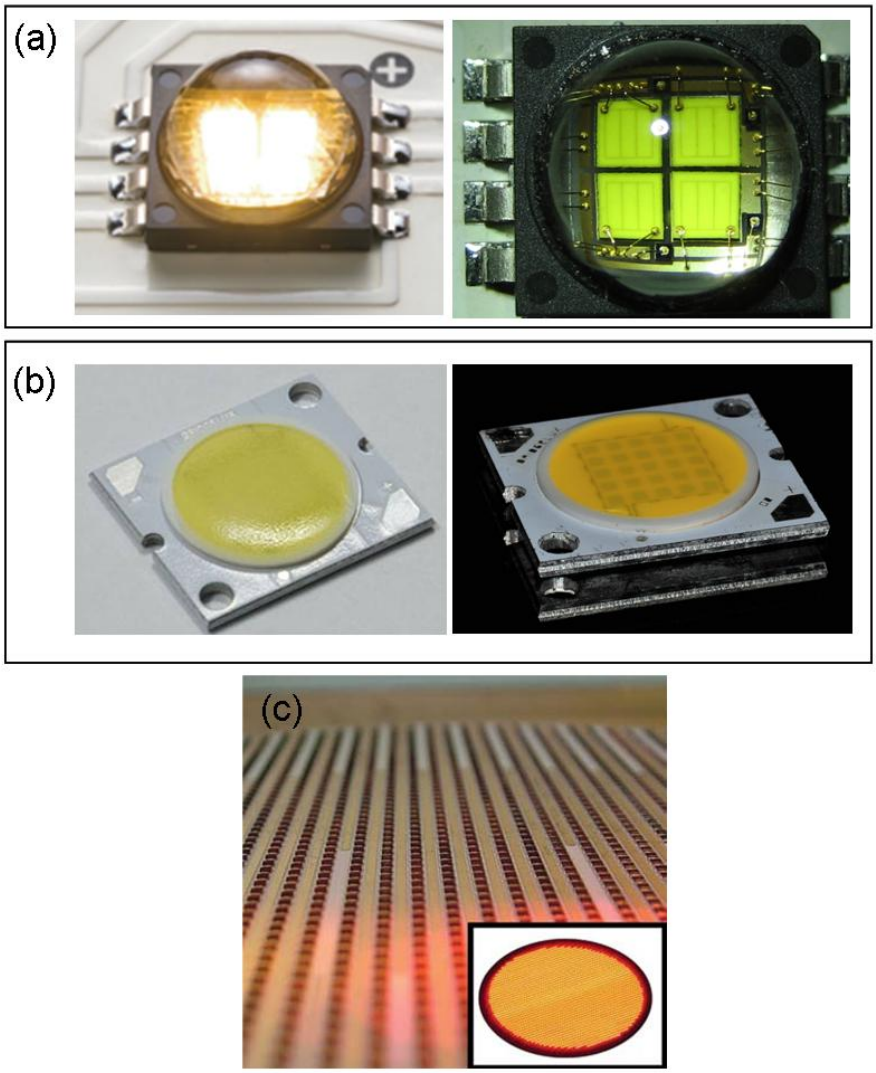


Figure 94. (a) Cree XLamp MC-E [5], (b) BridgeLux BXRA-C2000 [26]. (c) Perkin-Elmer Elcos, high power COB array with nearly 2000 1 mm^2 chips [27].

Several COB arrays are shown in Figure 94. All products employ a 1 mm^2 LED-chip. The pitch is less than 2 mm in all products, which may cause a severe increase in the junction temperature. In case of Cree XLamp MC-E, although LED-chips are placed so closely, there is a path of heat spreading and the thermal resistance of the package is not large. On the contrary, in case of BridgeLux BXRA-C2000 and PerkinElmer Elcos's COB array, the thermal resistance of the package could be very large due to the small pitch. If the operating power is low, less than 1W, the increase in the junction

temperature will not be significant. However, if these devices operate at high power, the pitch should increase.

5.2 Simulations of Actual Devices

5.2.1 UV LED

The thermal management of UV LEDs was studied. The LED-chip is a flip chip structure and is mounted on a AlN DBC substrate. A picture of an actual device and the schematic of its structure are shown in Figure 95. This design was from the Army Research Labs and provided by Dr. Meredith L. Reed.

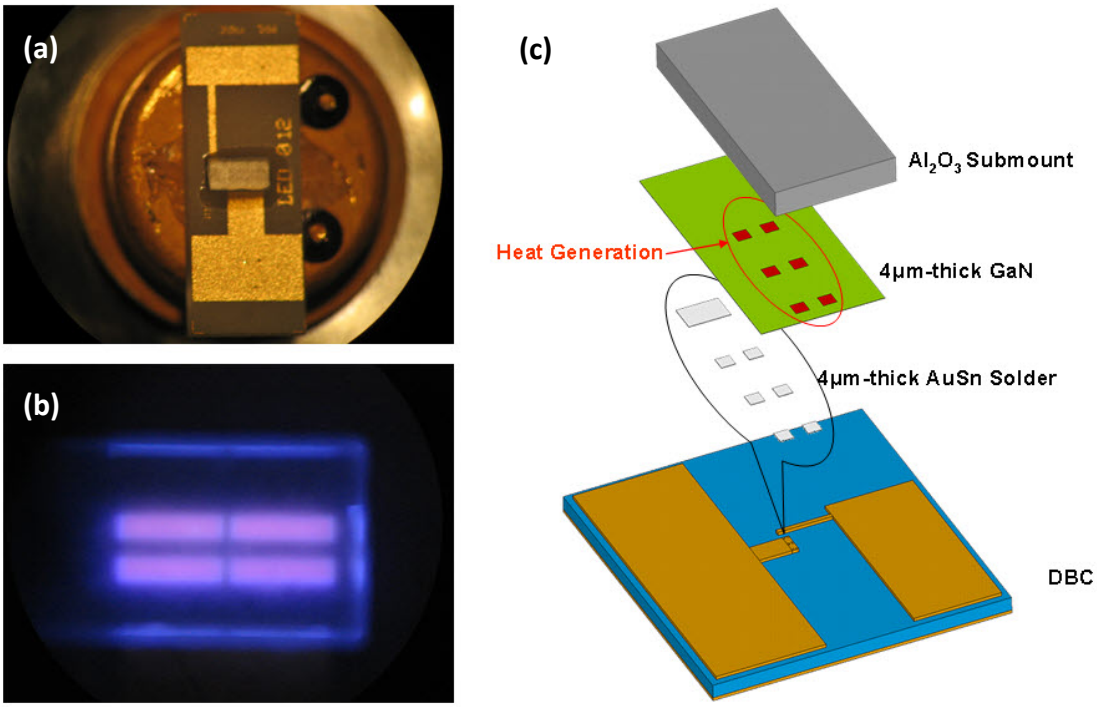


Figure 95. (a) Top view of UV LED, (b) UV LED when operating, and (c) the structure of UV LED. This design was from the Army Research Labs and provided by Dr. Meredith L. Reed.

Several different designs of the p-mesa interconnectors are considered as shown in Figure 96, and the junction temperature with respect to the design is studied by FEA. Several assumptions are made for this simulation. Firstly, we assume that all power applied turns into heat. The UV LED operates at 80 mA and 7 V—0.56 W is used as heat generation. Secondly, we assume that heat generation occurs inside the GaN device just upper side of p-mesa interconnections. The other assumptions are the same with those shown in chapter 3. The AlN DBC substrate, which has 203 μm of Cu and 635 μm of AlN, and the heat sink design shown in Figure 29 was used. The material properties are shown in Table 10. The results of simulations with 5 different p-mesa interconnector designs are shown in Figure 97. The lowest junction temperature is 43.7°C in the 1-pixel device and the highest one is 45.5°C in the 6-pixel device. The difference is 1.8°C and the thermal resistance difference becomes 3.21°C/W. The difference mainly comes from the heat generation area. Since the area of power generation is the largest in the 1-pixel device, the junction temperature is the lowest, while since the area is the smallest in 6-pixel device, the junction temperature is the highest.

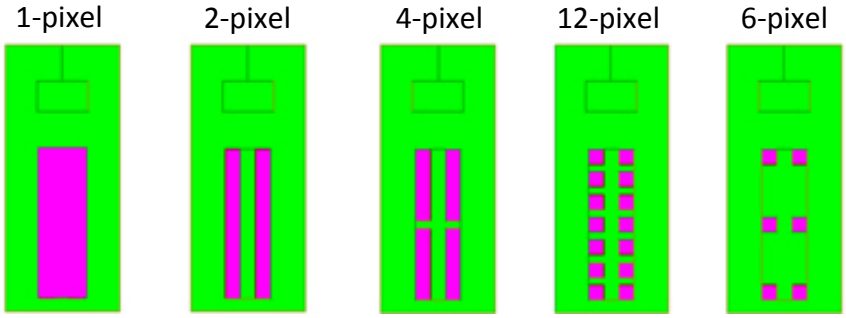


Figure 96. The designs of the p-mesa interconnectors

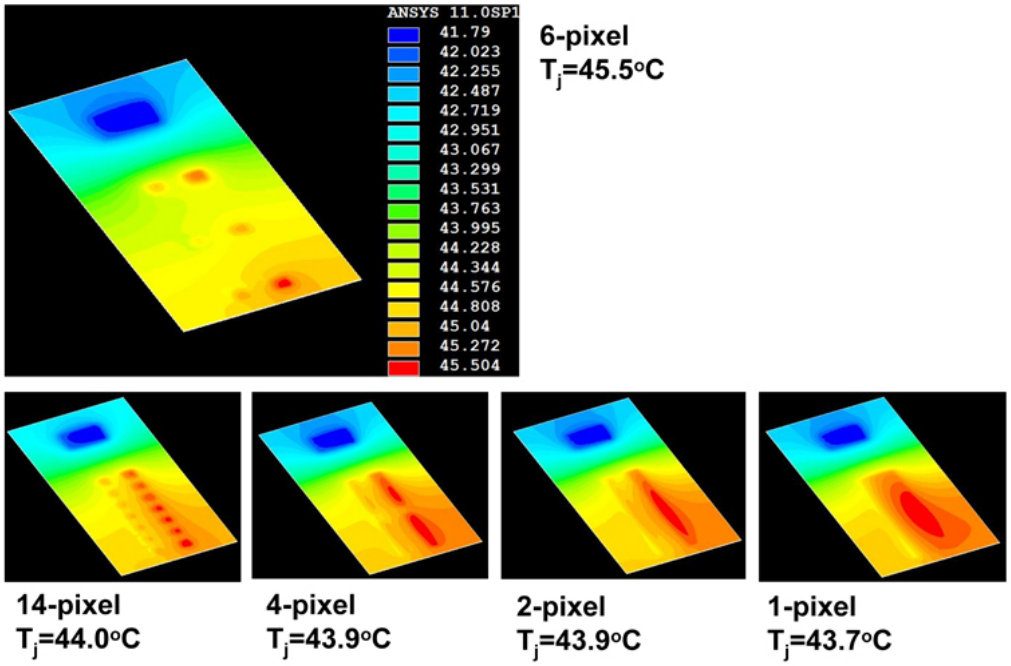


Figure 97. The contour plots of temperature distribution in GaN device with 5 different p-mesa interconnectors.

Another study on the selection of the substrate and the thickness of the copper layer was conducted. From the previous study, the thickness of the copper layer and its area size are not important factors in determining the thermal resistance in the substrate. However, since the heat flux area is 1 mm by 0.3 mm in the case of the 1-pixel device, which is smaller than a typical device, there could be some difference. Therefore, several FEA simulations were conducted and compared with analytical solution Figure 98. For this study, we used the 1-pixel device. Firstly, the thermal resistance as a function of copper thickness was calculated by an analytical method with 0.3 mm^2 of heat flux area. The thermal resistance of the same structure was estimated by FEA with two different heat flux areas; a 1 mm by 0.3 mm rectangle and 0.3 mm^2 square. The analytical solution agrees exactly with the FEA result with square heat source; however the FEA result with rectangular heat source is slightly lower than the analytical one. The difference of thermal resistance between the substrates of 70 μm and 350 μm of copper is 1.31°C/W with the square heat source and 1.15°C/W with the rectangular heat source. The

differences are only 0.74°C and 0.65°C with 0.56 W power input. A simulation of the entire package shows the difference in the junction temperature is 0.025°C, which is much smaller than that of the analytical solution (see Figure 99). This is because generated heat can spread in the GaN device and Al_2O_3 submount and flow through the n-electrode. As mentioned previously, thick copper is not suitable for flip chip structure because of its low etching resolution. Therefore, a thin copper layer is much better for the AlN DBC substrate of UV LED.

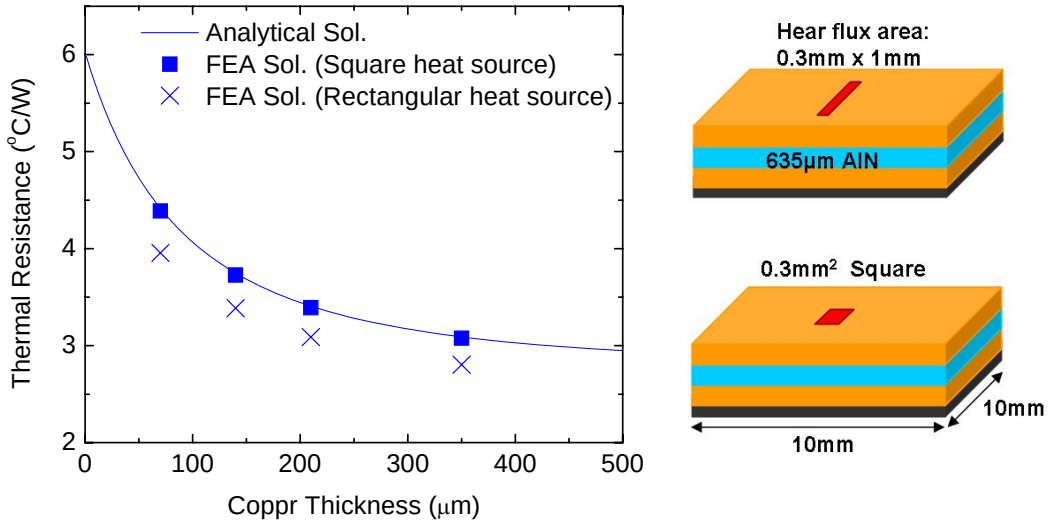


Figure 98. The thermal resistance of substrate and TIM as a function of copper thickness. 50 μm and 3 W/mK of TIM was used.

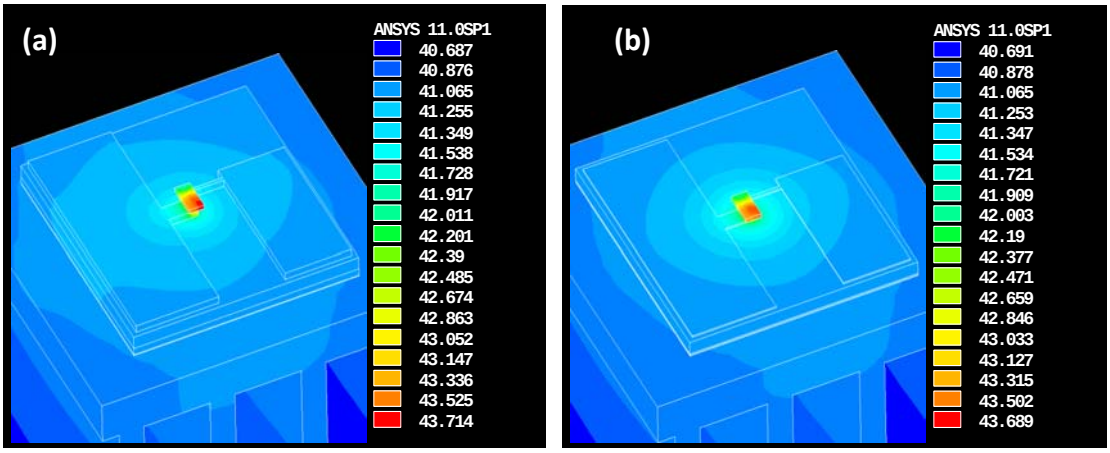


Figure 99. The contour plot of temperature distribution of UV LED. (a) 350 μm copper layer, and (b) 70 μm copper layer AlN DBC were used.

In Figure 97, asymmetric distribution of temperature in GaN device is shown. This is because asymmetric design of copper circuit layer. Although the effect of copper circuit layer on heat spreading is very small, the temperature difference between p-mesa is also small. However, if the device operates at high power or uses different substrate such as IMS, the circuit design should be changed. The recommended design is shown in Figure 100. Since most of heat generates at the top of p-mesa in this case, the circuit layer that contacts with p-electrode should has large area.

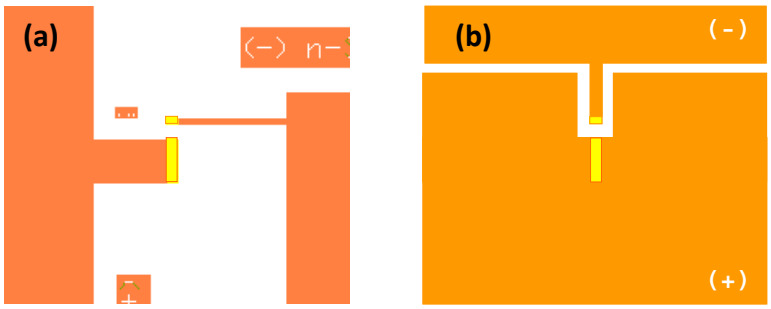


Figure 100. The design of copper circuit layer. (a) Current design and (b) recommended design.

5.2.2 Cree XLamp XR-E

Cree XLamp XR-E is one of the representative packages of single chip LED. It is ceramic package and has electrically neutral thermal path. It typically operates at 3.3 V and 350 mA, and emits 107 lm in white. Its estimated luminous efficacy is 92.6 lm/W. The maximum forwarding current is 1000 mA and the maximum junction temperature should not exceed 150°C. The thermal resistance from the junction to solder point is 8°C/W. Since its structure is well revealed by the vendor, its thermal characteristic was studied and compared with analytical solution. The appearance and structure is shown in Figure 101. To estimate its thermal resistance, the structure was simplified by eliminating the lens and reflector, which hardly affect the thermal resistance. The LED-chip used for XLamp XR-E is Cree EZ1000 (see Figure 102). Although its size is

980×980 μm^2, we assumed that it is 1mm^2 square. The height of silicon die is assumed as 100 μm and heat flux was directly applied on top of the die without modeling InGaN device and metal layer. 50 μm of Au-80Sn was used for die-attach. The ceramic substrate consists of three layers and shown in Figure 101(d). The ceramic was assumed as Al_2O_3. Based on the structure, the thermal simulation was conducted and shown in Figure 103.

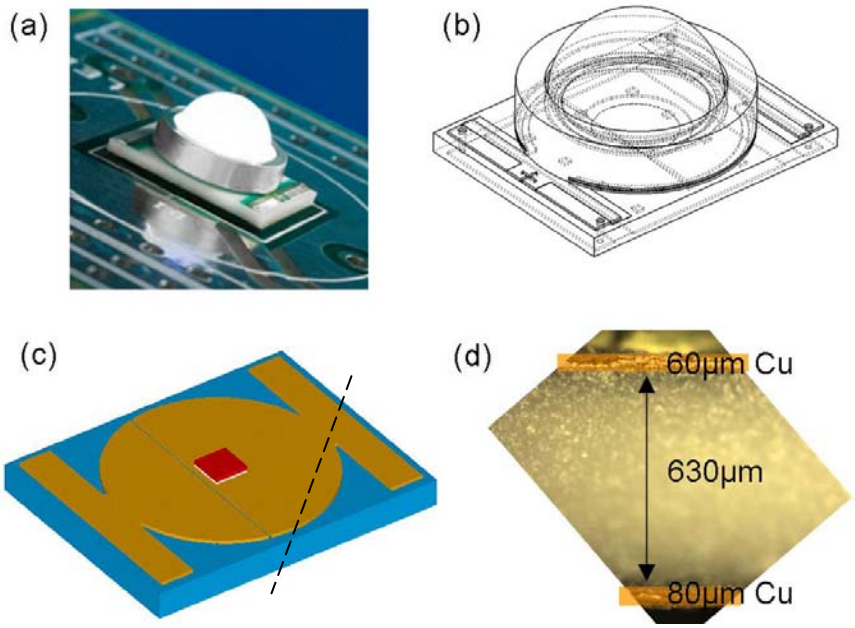


Figure 101. (a) Cree XLamp XR-E[5], (b) 3D model provided by Cree[5], (c) simplified model for thermal analysis, and (d) the cross section of the device along the dash line shown in (c).

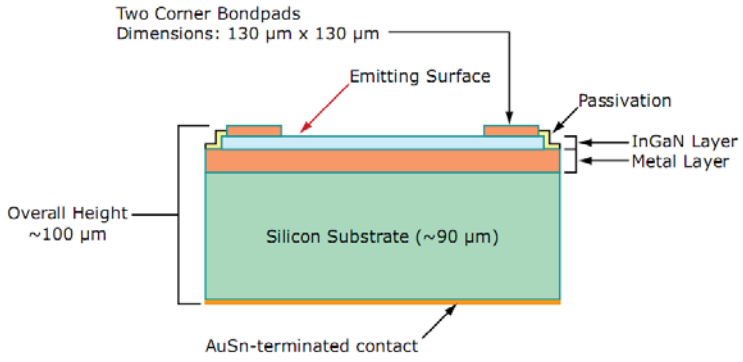


Figure 3: EZ1000 LED schematic cross-sectional view [dimensions are nominal]

Figure 102. Cree EZ1000 LED-chip in XLamp XR-E. The size is 980×980 μm^2.

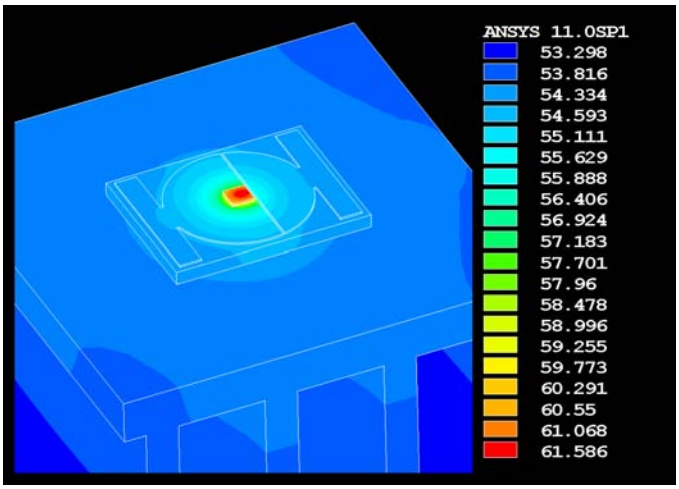


Figure 103. The contour plot of temperature distribution of Cree XLamp XR-E. The LED package is directly mounted on the heat sink using 50 μm TIM. The heat sink design shown in Figure 29 was used.

The thermal resistances from the junction to solder point estimated by FEA are 7.18°C/W with Sn-3.5Ag TIM, and 7.96°C/W with thermal grease TIM. They are almost similar to the thermal resistance shown in the datasheet, 8°C/W. It can be estimated by analytical method as well. Although there will be disagreement between FEA result and analytical solution mainly due to the etched copper circuit layer, we can have good understanding of the thermal characteristic by analytical solution and make an improvement. The electrical via does not play any role in estimating the thermal resistance because it is far from the heat source (see Figure 104).

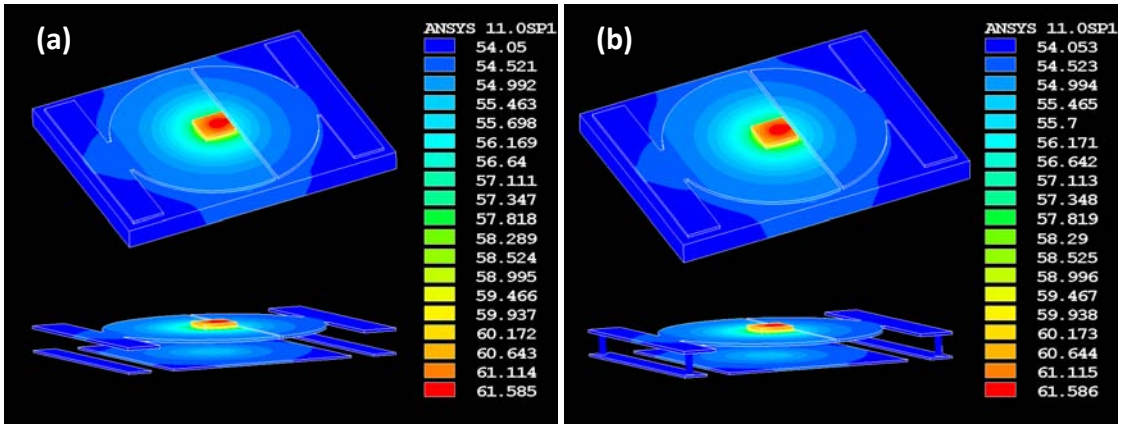


Figure 104. The contour plot of temperature distribution of Cree XLamp XR-E. (a) Result without electrical vias and (b) result with electrical vias.

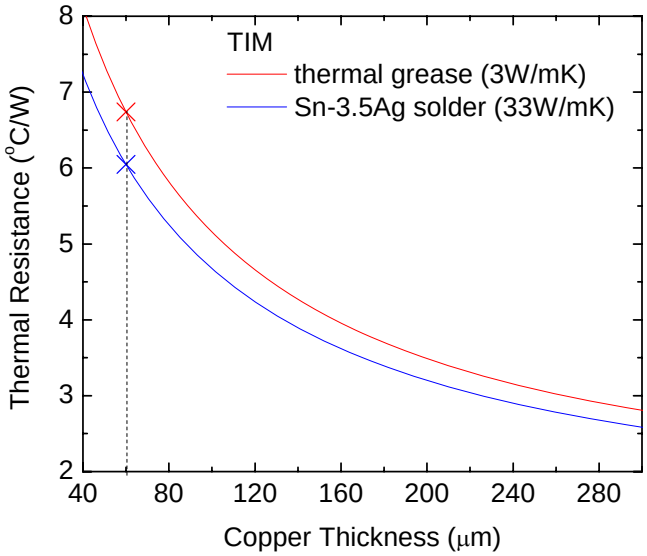


Figure 105. The thermal resistance of the substrate and TIM as a function of copper thickenss. Two different TIMs are used for estimation; 3 W/mK thermal grease and 33-W/mk Sn-3.5Ag solder. The thickness of bottom copper was fixed as 80 μm.

The thermal resistances of die and die-attach can be estimated by using Equation 4.1, and they are 0.806°C/W and 0.877°C/W, respectively. Also can that of the substrates and TIM by using Equation 4.13. The thermal resistance as a function of copper thickness was estimated and plotted in Figure 105. When the copper thickness is 60 μm, the thermal resistances of the substrate are 6.05°C/W with Sn-3.5Ag TIM and 6.74°C/W with thermal grease TIM. Therefore, the thermal resistances from the junction to solder point become 7.73°C/W with Sn-3.5Ag TIM, and 8.42°C/W with thermal grease TIM. We can notice that most of the thermal resistance is that of substrate and TIM. Therefore, to reduce thermal resistance of the substrate and TIM is the most effective way to reduce the thermal resistance of package. We can also notice that the TIM is not important factor to reduce the thermal resistance. The difference of the thermal resistance between using Sn-3.5Ag (33 W/mK) and using thermal grease (3-W/mK) is less than 0.8°C/W. Although there is disagreement between the FEA result and analytical solution, we can roughly estimate the change of the thermal resistance with respect to the copper thickness. For example, if the copper thickness increases from 60

μm to 140 μm, the expected decrease in the thermal resistance is 2.2°C/W by analytical solution, which is 1.8°C/W by FEA result.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 CONCLUSION

In this study, the thermal resistance of high power LEDs implementing COB architecture was analyzed by FEA and analytical analysis. The first contribution of this work was the analysis of the thermal response of high power LED packages, elucidating the thermal resistance imposed by each constituent layer. The thermal characteristics and design consideration of each layer are summarized as follows;

In the die and die-attach layers, the thermal resistance is very sensitive to the thermal conductivities and the layer thickness because of the very high heat flux transported through them. The die and die-attach can be assumed as one dimensional heat flux structures and their thermal resistances were developed based on one-dimensional thermal resistance for conduction in a plane wall. As die material, Si is a good choice because alternative materials like SiC are extraordinary expensive. Using thin layers of Si could be economical way to reduce thermal resistance of die rather than using SiC. In a practical case, 90 μm of Si die is used for Cree EZ1000 LED-chip to achieve a low thermal resistance [59, 60] (see Figure 106).

In the case of die-attach layers, the effect of thermal conductivity of the die-attach on the thermal conductivity is not significant. Any void or delimitation could be more critical than the thermal conductivity of the die-attach material. Au-20Sn is mostly used for the die-attach material of high power LEDs because of its excellent wettability, excellent resistance to corrosion, high thermal conductivity, high joint strength, and fluxless process. Also, the CTE matches well with other package material such as Si,

ceramics, Copper and etc. Moreover, the excellent wettability makes very thin die-attach possible, from a few microns to 10 μm.

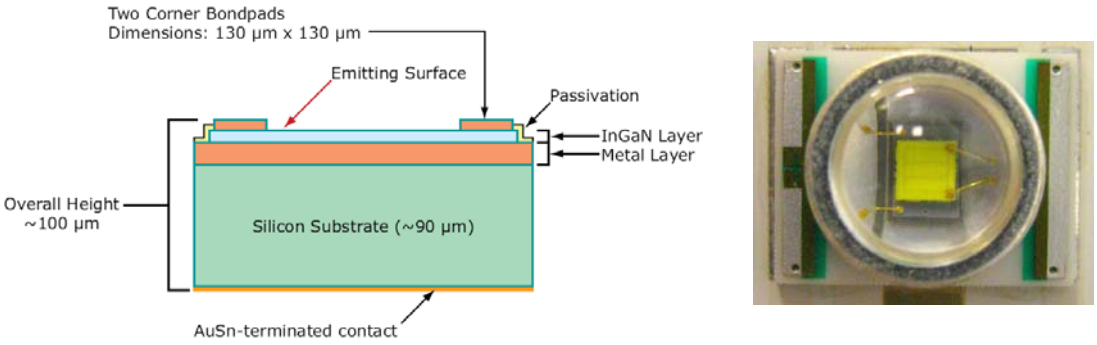


Figure 106. (a) The schematic cross-sectional view of Cree EZ1000 LED-chip (dimensions are nominal) and (b) Cree XLamp XR-E SMT package using this chip [59].

Power electronic substrates can dissipate heat very efficiently compared to a conventional FR4-PCB, and this is because of low thermal impedance of dielectric layer and effective heat spreading in thick copper circuit layer. In the case of a DBC substrate, ceramics are used as the dielectric material, which have very high thermal conductivities; AlN is 180 W/mK and Al_2O_3 is 30 W/mK. In the case of IMS, although the dielectric has very low thermal conductivity, 1 to 2 W/mK, low thermal impedance can be achieved by using very thin layers. These substrates can take advantage of the use of "heavy copper". By spreading heat in a thick copper circuit layer, effective heat transfer can be achieved. From the analysis, we found that the most important parameters in substrates are the thickness of the copper circuit layer and the lateral size of the substrate. Thick copper layers can dramatically reduce thermal resistance and at the same time it requires a large substrate area. However, in case of AlN DBC substrates, the impact of copper thickness is negligible because of the high thermal conductivity of AlN, 180 W/mK. Although AlN DBC substrates show better thermal performance than Al_2O_3 DBC substrate or IMS, it is more expensive than others. The copper thickness is the main factor to increase the price.

The thermal conductivity and thickness of the TIM are not critical factors to determine the thermal resistance of the package. That is because the heat flux magnitude after passing through the power substrate reduces to only 2 to 6% of that of die level due to heat spreading in substrate. Solder can be used to mount the SMT package on the substrate or the board; however it is not suitable for the substrate of COB array because of large contact area. The large contact area may cause non-uniform thickness and voids, which are damaging for reliability and thermal management. The most common is thermal grease, typically silicone grease filled with aluminum oxide, zinc oxide, or boron nitride. Another type is the phase-change materials (PCM). These are solid at room temperature but liquefy and behave like grease at operating temperatures. The main advantage of PCM is that they can achieve low thermal contact resistance at operating temperature while they are easy to handle and are not messy at room temperature.

The second contribution of this work is the development of an analytical model which accounts for the thermal resistance of the LED system to allow for parametric design studies. For the analysis, analytical solution of heat spreading problem for multi-layer (up to four layers) was derived. Although there are two existing solutions, they have restrictions or errors; Palisoc's solution[45] is too complicate for parametric studies and does not account for lateral substrate size, and Masana's solution[57] shows large error if low thermal conductivity layer exists in multi-layer. Our analytical solution provides very accurate result under some conditions; heat flux at the center of substrates and uniform temperature at the bottom of substrate. By using our solution, we provided the characteristic of IMS and DBC substrates with $1mm^2$ heat flux area.

The analytical analysis of the thermal circuit model of LED arrays is possible by using the Muzychka's solution[50]. The thermal resistance of LED-array largely depends on the pitch, which is the distance between two adjacent LED-chips, as well as other parameters that mentioned previously. The design shows that LED-chips placed evenly on the heat sink have the lowest thermal resistance and it increases gradually as the pitch

decreases. Although the placement of LED-chip on the substrate depends on other design considerations, the pitch should be larger than the distance which causes significant incensement in the thermal resistance by the interference of heat spreading in the substrate level. The value varies with the type of substrate and the thickness of each layer in the substrate as well as heat source size. The analytical solution derived in this study can provide simple and easy way to find the response with respect to the change of each design parameter.

The optimized thermal design is not always acceptable because the design is restricted by other design considerations, cost and so on. The optimized design should be determined by considering trade-offs with all other factors. The general guideline for the thermal management of LED-array implementing COB technology can be provided by this study. After determining the general design by using analytical solutions, the specific design can be examined by FEA or experimental methods.

6.2 Future Work

This research has been focused on the thermal analysis of LED packages through FEA and analytical analysis. The result shown here could be different from practical cases because of simplifications in modeling, thermal contact resistance, and so on. Thus it is always required to compare with experimental results. Also, thermal stress is another issue. Because of the CTE mismatch between the GaN-based device and Si die, solder, substrate, etc, large thermal stresses would exist in the device and it may affect the reliability. Currently most high power LEDs have the VTF structure, in which the GaN-based device is transferred to Si die after growing on sapphire substrate. A new technology is under development, which involves directly growing GaN on a Si wafer, and an overall 90% reduction in production costs is expected [61]. In this technology, stresses induced by lattice mismatch and CTE mismatch are the main challenge to achieve reasonable reliability. Therefore, analyzing thermal stress and finding the way to reduce thermal stress should be studied. Also, investigation of alternative material for die-attach and TIM such as carbon nanotubes (CNTs) should be studied.

APPENDIX A

ANSYS PARAMETRIC DESIGN LANGUAGE (APDL)

FOR LED ARRAYS

```
FINISH
/CLEAR

!!!!!!!!!!!!!!Changeable parameter!!!!!!!!!!
room_temp=25                        ! Room temperature (degree C)
conv_coef=10                        ! Convection coefficient (W/m^2K)
die_thk=375e-6                      ! Die thickness (m)
crct_thk=127e-6                     ! Copper Circuit Layer Thickness (m)
dlct_thk=381e-6                     ! Ceramic Thickness (m)
base_thk=127e-6                     ! Base Thickness (m)
distance=8000e-6                    ! Distance between copper circuit layers (m)
die_sz=1000e-6                      ! Side length of Die (m)
crct_sz=4000e-6                     ! Side length of Copper Circuit Layer (m)
sbstrt_sz=2*(crct_sz*3+distance*3)  ! Side length of Substrate (m)
htsnk_sz=120000e-6                  ! Side length of Heat sink (m)
heat_flux=1/(die_sz*die_sz)         ! Heat flux density (W/m^2)

/PREP7
ET,1,SOLID90
                                    !! Thermal conductivity (W/mK)
MP,KXX,2,124                        ! Die
MP,KXX,3,  57                       ! Solder
MP,KXX,4,385                        ! Copper Circuit
MP,KXX,5,180                        ! Ceramic
MP,KXX,6,385                        ! Base
MP,KXX,7, 3                         ! TIM
MP,KXX,8,150                        ! Heat Sink

!Solder between Substrate and Heatsink
WPOFFS,,,20000e-6
BLC4,,,sbstrt_sz/2,sbstrt_sz/2,50e-6
WPOFFS,,,50e-6

!Substrate
BLC4,,,sbstrt_sz/2,sbstrt_sz/2,base_thk
WPOFFS,,,base_thk
BLC4,,,sbstrt_sz/2,sbstrt_sz/2,dlct_thk
WPOFFS,,,dlct_thk
*DO,I,0,2
```

```
*DO,J,0,2
BLC5,(distance+crct_sz)/2*(2*i+1),(distance+crct_sz)/2*(2*j+1),crct_sz,crct_sz,crct_thk
*ENDDO
*ENDDO
WPOFFS,,,crct_thk

!Solder between SiC Die & Substrate
*DO,I,0,2
*DO,J,0,2
BLC5,(distance+crct_sz)/2*(2*i+1),(distance+crct_sz)/2*(2*j+1),die_sz,die_sz,50e-6
*ENDDO
*ENDDO
WPOFFS,,,50e-6

!SiC Die
*DO,I,0,2
*DO,J,0,2
BLC5,(distance+crct_sz)/2*(2*i+1),(distance+crct_sz)/2*(2*j+1),die_sz,die_sz,die_thk
*ENDDO
*ENDDO
WPOFFS,,,die_thk

!Heat Sink
WPOFFS,,,-(die_thk +50e-6 +crct_thk +dlct_thk +base_thk +50e-6 +20000e-6)
VSEL,NONE
BLOCK,(2000e-6:htsnk_sz/2:5500e-6),(3500e-6:htsnk_sz/2:5500e-6),,htsnk_sz/2,
,18000e-6
BLOCK,0,htsnk_sz/2,0,htsnk_sz/2,18000e-6,20000e-6
VADD,ALL

ALLSEL,ALL
VGLUE,ALL

!!!!!!!!!!!!!!!!!!meshing!!!!!!!!!!!!!!!!!!!!
!Die
LSEL,S,LOC,Z,50e-6 +crct_thk +dlct_thk +base_thk +50e-6 +20000e-6 +1e-6, die_thk
+50e-6 +crct_thk +dlct_thk +base_thk +50e-6 +20000e-6 -1e-6
LESIZE,ALL,,,5
VSEL,S,LOC,Z,50e-6 +crct_thk +dlct_thk +base_thk +50e-6 +20000e-6      , die_thk
+50e-6 +crct_thk +dlct_thk +base_thk +50e-6 +20000e-6
ASLV,S
LSLA,S
LESIZE,ALL,50e-6
MAT,2
MSHAPE,0,3D
VMESH,ALL
```

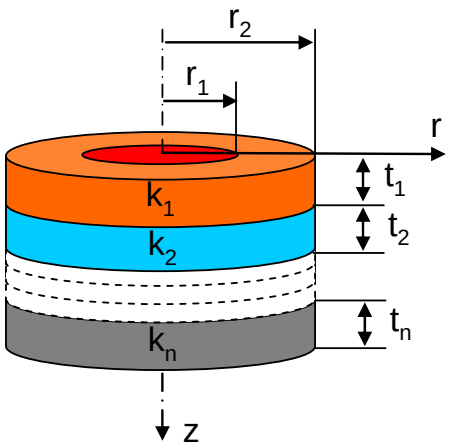
```
!Solder between Die and Substrate
LSEL,S,LOC,Z,crct_thk +dlct_thk +base_thk +50e-6 +20000e-6 +1e-6, 50e-6 +crct_thk
+dlct_thk +base_thk +50e-6 +20000e-6 -1e-6
LESIZE,ALL,,,2
VSEL,S,LOC,Z,crct_thk +dlct_thk +base_thk +50e-6 +20000e-6      , 50e-6 +crct_thk
+dlct_thk +base_thk +50e-6 +20000e-6
MAT,3
MSHAPE,0,3D
VMESH,ALL

!Solder between Substrate and Heatsink
LSEL,S,LOC,Z,20000e-6 +1e-6, 50e-6 +20000e-6 -1e-6
LESIZE,ALL,,,2
VSEL,S,LOC,Z,20000e-6      , 50e-6 +20000e-6
ASLV,S
AESIZE,ALL,500e-6
MAT,7
MSHAPE,0,3D
VMESH,ALL

!Substrate Base Layer
LSEL,S,LOC,z,50e-6 +20000e-6 +1e-6, base_thk +50e-6 +20000e-6 -1e-6
LESIZE,ALL,,,2
VSEL,S,LOC,Z,50e-6 +20000e-6 +1e-6, base_thk +50e-6 +20000e-6 -1e-6
MAT,6
MSHAPE,0,3D
VMESH,ALL

!Substrate Circuit Layer
LSEL,S,LOC,Z,dlct_thk +base_thk + 50e-6 +20000e-6 +1e-6, crct_thk +dlct_thk
+base_thk +50e-6 +20000e-6 -1e-6
LESIZE,ALL,,,2
VSEL,S,LOC,Z,dlct_thk +base_thk + 50e-6 +20000e-6 +1e-6, crct_thk +dlct_thk
+base_thk +50e-6 +20000e-6 -1e-6
MAT,4
MSHAPE,1,3D
VMESH,ALL

!Substrate Dielectric Layer
LSEL,S,LOC,Z,base_thk + 50e-6 +20000e-6 +1e-6, dlct_thk +base_thk +50e-6 +20000e-
6 -1e-6
LESIZE,ALL,,,2
VSEL,S,LOC,Z,base_thk + 50e-6 +20000e-6 +1e-6, dlct_thk +base_thk +50e-6
+20000e-6 -1e-6
ASLV,S
```

```
AESIZE,ALL,500e-6
MAT,5
MSHAPE,1,3D
VMESH,ALL

!Heatsink
VSEL,S,LOC,Z,0,20000e-6
MAT,8
MSHAPE,1,3D
VMESH,ALL

!!!!!!!!Solve for operating temperature!!!!!!!!
/SOLU
ANTYPE,0

!Heat boundary condition--heat flux
ALLSEL,ALL
ASEL,S,LOC,Z,die_thk +50e-6 +crct_thk +dlct_thk +base_thk +50e-6 +20000e-6 -1e-6,
die_thk +50e-6 +crct_thk +dlct_thk +base_thk +50e-6 +20000e-6 +1e-6
SFA,ALL,,HFLUX,heat_flux

!Heat boundary condition--convection
ALLSEL,ALL
ASEL,S,LOC,Z,17999e-6,18001e-6
SFA,ALL,,CONV, conv_coef,room_temp

ALLSEL,ALL
SOLVE
FINISH

/POST1
PLNSOL,TEMP,,0
```

APPENDIX B

EXACT SOLUTION

FOR HEAT SPREADING RESISTANCE IN MULTI-LAYER



The solution is based on Kennedy's solution

$$\frac{\partial^2 T_i}{\partial r^2}+\frac{1}{r}\frac{\partial T_i}{\partial r}+\frac{\partial^2 T_i}{\partial z^2}=0 \tag{B.1}$$

Separation of variables in Equation B.1 is accomplished by assuming a solution of the form

$$T_i(r,z)=A_i+B_i z+U_i(r)V_i(z) \tag{B.2}$$

Substitution Equation B.2 into Equation B.1 yields the separated equations

$$\frac{\partial^2 U_i}{\partial r^2}+\frac{1}{r}\frac{\partial U}{\partial r}+\lambda^2 U_i=0 \tag{B.3}$$

$$\frac{\partial^2 V_i}{\partial z^2}-\lambda^2 V=0 \tag{B.4}$$

where λ is the constant of separation. Solutions involving Neumann functions are excluded since the desired temperature distribution must be well behaved at the origin

The general solution of Laplace's equation which is applicable to this problem has the form

$$T_i(r,z) = A_i + B_i z + \left[c_i \cosh(\lambda z) + c_i^* \sinh(\lambda z) \right] J_0(\lambda r) \tag{B.5}$$

Equation B.5 must satisfy the boundary conditions;

$$\left.\frac{\partial T_i}{\partial r}\right|_{r=r_2} = 0 \qquad 0 < z < z_n \tag{B.6}$$

$$\left.\frac{\partial T_1}{\partial z}\right|_{z=0} = \begin{cases} -q''/k_1 & 0 < r < r_1 \\ 0 & r_1 < r < r_2 \end{cases} \tag{B.7}$$

$$T_n(r,z_n) = 0 \qquad 0 < r < r_2 \tag{B.8}$$

$$T_i(r,z) = T_{i+1}(r,z) \qquad z = d_i, \quad i = 1,2,...,n \tag{B.9}$$

$$k_i \frac{\partial T_i}{\partial z} = k_{i+1} \frac{\partial T_{i+1}}{\partial z} \qquad z = d_i, \quad i = 1,2,...,n \tag{B.10}$$

Substituting Equation B.5 into Equation B.6 yields the relation

$$T_i(r,z) = A_i + B_i z + \sum_{l=1}^{\infty} \left[C_i \sinh\left(\frac{\alpha_l}{r_2} z\right) + D_i \cosh\left(\frac{\alpha_l}{r_2} z\right) \right] J_0\left(\frac{\alpha_l}{r_2} r\right) \tag{B.11}$$

where α_l is the root of the first-order Bessel function, $J_1(x)$. The summation is conducted over ascending values of α_l. Substituting Equation B.11 into Equation B.7 and applying Fourier-Bessel transform yields Equation B.12 and by solving it Equation B.13 is obtained.

$$\int_0^{r_2} \left.\frac{\partial T_1}{\partial z}\right|_{z=0} r dr = \int_0^{r_1} -\frac{q''}{k_1} r dr \tag{B.12}$$

$$B_1 = -\frac{q''}{k_1} \left(\frac{r_1}{r_2}\right)^2 \tag{B.13}$$

Multiplying the Bessel function both sides of Equation B.12 and applying Fourier-Bessel transform yields Equation B.14 and by solving it Equation B.15 is obtained.

$$\int_0^{r_2} \left.\frac{\partial T_1}{\partial z}\right|_{z=0} J_0\left(\frac{\alpha_k}{r_2} r\right) r dr = \int_0^{r_1} -\frac{q''}{k_1} J_0\left(\frac{\alpha_k}{r_2} r\right) r dr \tag{B.14}$$

$$C_1 = -\frac{2q'' r_1}{k_1} \frac{J_1\left(\frac{r_1}{r_2}\alpha_l\right)}{\alpha_l^2 J_0^2(\alpha_l)} \tag{B.15}$$

Substituting Equation B.11 into Equation B.8 and applying Fourier-Bessel transform yields Equation B.16 and by solving it Equation B.17 is obtained.

$$\int_0^{r_2} T_n(r,z)\, r dr = 0 \tag{B.16}$$

$$A_n + B_n d_n = 0 \tag{B.17}$$

Multiplying the Bessel function both sides of Equation B.16 and applying Fourier-Bessel transform yields Equation B.18 and by solving it Equation B.19 is obtained.

$$\int_0^{r_2} T_n(r,z) J_0\left(\frac{\alpha_k}{r_2} r\right) r dr = 0 \tag{B.18}$$

$$D_{n,k} = -\tanh\left(\frac{\alpha_k}{r_2} d_n\right) \times C_{n,k} \tag{B.19}$$

Substituting Equation B.11 into Equation B.9 and applying Fourier-Bessel transform yields Equation B.20 and by solving it Equation B.21 is obtained.

$$\int_0^{r_2} T_i(r,d_i)\, r dr = \int_0^{r_2} T_{i+1}(r,d_i)\, r dr \tag{B.20}$$

$$A_i + B_i d_i = A_{i+1} + B_{i+1} d_i \tag{B.21}$$

Multiplying the Bessel function both sides of Equation B.20 and applying Fourier-Bessel transform yields Equation B.22 and by solving it Equation B.23 is obtained.

$$\int_0^{r_2} T_i(r,d_i) J_0\left(\frac{\alpha_k}{r_2} r\right) r dr = \int_0^{r_2} T_{i+1}(r,d_i) J_0\left(\frac{\alpha_k}{r_2} r\right) r dr \tag{B.22}$$

$$D_{i+1,l} - D_{i,l} = -\tanh\left(\frac{d_1}{r_2}\alpha_l\right) \times \left(C_{i+1,l} - C_{i,l}\right) \tag{B.23}$$

Substituting Equation B.11 into Equation B.10 and applying Fourier-Bessel transform yields Equation B.24 and by solving it Equation B.25 is obtained.

$$\int_0^{r_2} k_i \left.\frac{\partial T_i}{\partial z}\right|_{z=d_i} rdr = \int_0^{r_2} k_{i+1} \left.\frac{\partial T_{i+1}}{\partial z}\right|_{z=d_i} rdr \tag{B.24}$$

$$k_i B_i = k_{i+1} B_{i+1} \tag{B.25}$$

Multiplying the Bessel function both sides of Equation B.24 and applying Fourier-Bessel transform yields Equation B.26 and by solving it Equation B.27 is obtained.

$$\int_0^{r_2} k_i \left.\frac{\partial T_i}{\partial z}\right|_{z=d_i} J_0\left(\frac{\alpha_k}{r_2} r\right) rdr = \int_0^{r_2} k_{i+1} \left.\frac{\partial T_{i+1}}{\partial z}\right|_{z=d_i} J_0\left(\frac{\alpha_k}{r_2} r\right) rdr \tag{B.26}$$

$$k_{i+1} D_{i+1,l} - k_i D_{i,l} = -\coth\left(\frac{d_1}{r_2}\alpha_l\right) \times \left(k_{i+1} C_{i+1,l} - k_i C_{i,l}\right) \tag{B.27}$$

For n-layers Equation B.13, B.17, B.21, B.25 provides *2n* equations and there are *2n* unknowns; $A_1, A_2, \ldots, A_n, B_1, B_2, \ldots, B_n$

For n-layers Equation B.15, B.19, B.23, B.27 provides *2n* equations and there are *2n* unknowns; $C_1, C_2, \ldots, C_n, D_1, D_2, \ldots, D_n$

Simultaneous equations are solved implementing commercial program, Mathematica. The temperature distribution in the first layer yields Equation B.28

$$T_1(r,z) = q''\left(\frac{r_1}{r_2}\right)^2 \left(\sum_{i=1}^{n} \frac{t_i}{k_i} - \frac{1}{k_1} z\right) - \frac{2q''r_1}{k_1} \sum_{l=1}^{\infty} C_{1,l} \left[\sinh\left(\frac{\alpha_l}{r_2} z\right) - \varphi_{n,l} \cosh\left(\frac{\alpha_l}{r_2} z\right)\right] J_0\left(\frac{\alpha_l}{r_2} r\right) \tag{B.28}$$

The thermal resistance based on the maximum temperature yields Equation B.29

$$R_{th} = \frac{T_1(0,0)}{\pi r_1^2 q''} = \frac{1}{\pi r_2^2} \sum_{i=1}^{n} \frac{t_i}{k_i} + \frac{2r_1}{k_1 r_2^2} \left(\frac{r_1}{r_2}\right)^2 \sum_{l=1}^{\infty} \frac{J_1\left(\frac{r_1}{r_2}\alpha_l\right)}{\alpha_l^2 J_0^2(\alpha_l)} \varphi_{n,l} \tag{B.29}$$

where, $\varphi_{n,l}$ is determined by the number of the total layers and the values up to 4 layers are calculated;

$$\varphi_{1,l} = \tanh(t_1 \lambda_l) \tag{B.30}$$

$$\varphi_{2,l}=\frac{\dfrac{\tanh\left(t_1\lambda_l\right)}{k_1}+\dfrac{\tanh\left(t_2\lambda_l\right)}{k_2}}{\dfrac{1}{k_1}+\dfrac{\tanh\left(t_1\lambda_l\right)\tanh\left(t_2\lambda_l\right)}{k_2}} \tag{B.31}$$

$$\varphi_{3,l}=\frac{\dfrac{\tanh\left(t_1\lambda_l\right)}{k_1}+\dfrac{\tanh\left(t_2\lambda_l\right)}{k_2}+\dfrac{\tanh\left(t_3\lambda_l\right)}{k_3}+\dfrac{k_2}{k_1k_3}\tanh\left(t_1\lambda_l\right)\tanh\left(t_2\lambda_l\right)\tanh\left(t_3\lambda_l\right)}{\dfrac{1}{k_1}+\dfrac{\tanh\left(t_1\lambda_l\right)\tanh\left(t_2\lambda_l\right)}{k_2}+\dfrac{\tanh\left(t_1\lambda_l\right)\tanh\left(t_3\lambda_l\right)}{k_3}+\dfrac{k_2}{k_1k_3}\tanh\left(t_2\lambda_l\right)\tanh\left(t_3\lambda_l\right)} \tag{B.32}$$

$$\varphi_{4,l}=\frac{\left[\begin{array}{l}\dfrac{\tanh\left(t_1\lambda_l\right)}{k_1}+\dfrac{\tanh\left(t_2\lambda_l\right)}{k_2}+\dfrac{\tanh\left(t_3\lambda_l\right)}{k_3}+\dfrac{\tanh\left(t_4\lambda_l\right)}{k_4}\\ +\dfrac{k_2}{k_1k_3}\tanh\left(t_1\lambda_l\right)\tanh\left(t_2\lambda_l\right)\tanh\left(t_3\lambda_l\right)+\dfrac{k_2}{k_1k_4}\tanh\left(t_1\lambda_l\right)\tanh\left(t_2\lambda_l\right)\tanh\left(t_4\lambda_l\right)\\ +\dfrac{k_3}{k_1k_4}\tanh\left(t_1\lambda_l\right)\tanh\left(t_3\lambda_l\right)\tanh\left(t_3\lambda_l\right)+\dfrac{k_3}{k_2k_4}\tanh\left(t_2\lambda_l\right)\tanh\left(t_3\lambda_l\right)\tanh\left(t_4\lambda_l\right)\end{array}\right]}{\left[\begin{array}{l}\dfrac{1}{k_1}+\dfrac{\tanh\left(t_1\lambda_l\right)\tanh\left(t_2\lambda_l\right)}{k_2}+\dfrac{\tanh\left(t_1\lambda_l\right)\tanh\left(t_3\lambda_l\right)}{k_3}+\dfrac{\tanh\left(t_1\lambda_l\right)\tanh\left(t_4\lambda_l\right)}{k_4}\\ +\dfrac{k_2}{k_1k_3}\tanh\left(t_2\lambda_l\right)\tanh\left(t_3\lambda_l\right)+\dfrac{k_2}{k_1k_4}\tanh\left(t_2\lambda_l\right)\tanh\left(t_4\lambda_l\right)+\dfrac{k_3}{k_1k_4}\tanh\left(t_3\lambda_l\right)\tanh\left(t_4\lambda_l\right)\\ +\dfrac{k_3}{k_2k_4}\tanh\left(t_1\lambda_l\right)\tanh\left(t_2\lambda_l\right)\tanh\left(t_3\lambda_l\right)\tanh\left(t_4\lambda_l\right)\end{array}\right]} \tag{B.33}$$

where $\lambda_l=\alpha_l/r_2$.

Matlab Code for Thermal Resistance of Multi-layer Structure

```
r1=564.189e-6;
r2=r1*10;

k1=385;
k2=180;
k3=385;
k4=3;

t1=127e-6;
t2=381e-6;
t3=127e-6;
t4=50e-6;

beta=pi*(4*[1:1500]'+1);
alpha=beta/4.*(1-6./beta.^2+6./beta.^4-4716./(5*beta.^6)+3902418./(70*beta.^8));

C1=-2/(pi*r1*k1) * besselj(1,r1/r2*alpha)./(alpha.*besselj(0,alpha)).^2;
lambda=alpha/r2;

A1=(t1/k1+t2/k2+t3/k3+t4/k4)/(pi*r2^2);
num=tanh(t1*lambda)/k1+tanh(t2*lambda)/k2+tanh(t3*lambda)/k3+tanh(t4*lambda)/k4.
..
   +k2/(k1*k3)*tanh(t1*lambda).*tanh(t2*lambda).*tanh(t3*lambda)...
   +k2/(k1*k4)*tanh(t1*lambda).*tanh(t2*lambda).*tanh(t4*lambda)...
   +k3/(k1*k4)*tanh(t1*lambda).*tanh(t3*lambda).*tanh(t4*lambda)...
   +k3/(k2*k4)*tanh(t2*lambda).*tanh(t3*lambda).*tanh(t4*lambda);
den=1/k1+tanh(t1*lambda).*tanh(t2*lambda)/k2...
   +tanh(t1*lambda).*tanh(t3*lambda)/k3...
   +tanh(t1*lambda).*tanh(t4*lambda)/k4...
   +k2/(k1*k3)*tanh(t2*lambda).*tanh(t3*lambda)...
   +k2/(k1*k4)*tanh(t2*lambda).*tanh(t4*lambda)...
   +k3/(k1*k4)*tanh(t3*lambda).*tanh(t4*lambda)...
   +k3/(k2*k4)*tanh(t1*lambda).*tanh(t2*lambda).*tanh(t3*lambda).*tanh(t4*lambda);

D1_4=-num./den.*C1;
Rth=(A1 + sum(D1_4));
```

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