FUNDAMENTAL STUDY OF UNDERFILL VOID FORMATION IN FLIP CHIP ASSEMBLY

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Sangil Lee

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FUNDAMENTAL STUDY OF UNDERFILL VOID FORMATION IN FLIP CHIP ASSEMBLY

Approved by:

Dr. Daniel F. Baldwin, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Rao Tummala
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Jonathan S. Colton
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Jack Moon
Materials Science and Engineering
Georgia Institute of Technology

Dr. Mostafa Ghiaasiaan
School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: [May 12, 2009]

To my parents, Youngsul Lee and Boksoon Jo
To my brother and sister, Sanghyun Lee and Sangmi Lee
To my wife, Ranghee Kim
Thanks for your love and support through the years

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NOMENCLATURE

A	Isothermal constant for idea gas [s^2/m^2]
A_{LG}	Surface geometric factor between liquid and gas [m^2]
A_{SG}	Surface geometric factor between solid and gas [m^2]
a	van der Waals constant [$bar(m^3/mole)^2$]
b	van der Waals constant [m^3/mole]
C	Concentration of available heterogeneous nucleation sites [sites/m^2]
c	Gas concentration [kg(gas)/kg(underfill)]
D_0	Diffusivity coefficient [m^2/s]
D	Diffusivity of gas [m^2/s]
E_D	Activation energy for diffusion [J]
f	Frequency factor of gas molecules joining a heterogeneous nucleus [1/s]
G	Gibbs free energy [J]
ΔG^*_{het}	Gibbs free energy for heterogeneous nucleation [J]
K_H	Henry's law constant [s^2/m^2]
k	Boltzmann's constant [J/K]
M_w	Molecular weight [mole/g]
ΔP	Difference in the pressure of the gas in the void and ambient [Pa]
P_G	Pressure of the gas phase in the void [Pa]
P_L	Pressure of the liquid phase in the underfill [Pa]
R_0	Radius of a void at critical point [m]
R	Radius of a void [m]
R	Universal gas constant [J/moleK]

r	Radial coordinate relative to the center of the void [m]
T	Absolute temperature [K]
T_g	Glass transition temperature [K]
V_G	Volume of a spherical void [m^3]
v	Molecular volume [m^3]
γ_{ij}	Interfacial energy between phase i and j [N/m]
μ_L	Newtonian viscosity of no-flow underfill [Pa s]
η	Non-Newtonian viscosity of no-flow underfill [Pa s]
ρ_L	Density of underfill [Kg/m^3]
σ_{N2}	Molecular diameter of a nitrogen gas [Å]
σ_x	Molecular diameter of a gas [Å]
Re	Reynolds number

Subscripts

1	Solvent or gas
2	No-underfill
*	Dimensionless form
G	Gas phase
L	Liquid phase
S	Solid phase
Max	Maximum
Min	Minimum

SUMMARY

Flip Chip in Package (FCIP) has been developed to achieve the assembly process with area array interconnects. Particularly, a high I/O count coupled with finer pitch area array interconnects structured FCIP can be achieved using no-flow underfill assembly process. Using the assembly process, a high, stable yield assembly process recently reported with eutectic lead-tin solder interconnections, 150 μm pitch, and I/O counts in excess of 3000. The assembly process reported created a large number of voids among solder interconnects in FCIP.

The voids formed among solder interconnections can propagate, grow, and produce defects such as solder joint cracking and solder bridging. Moreover, these voids can severely reduce reliability performance. Indeed, many studies were conducted to examine the void formation in FCIP. Based on the studies, flip chip geometric design, process conditions, and material formulation have been considered as the potential causes of void formation. However, the present research won't be able to identify the mechanism of void formation, causing a lot of voids in assembly process without consideration of chemical reaction in the assembly process with a fine-pitch, high I/O density FCIP.

Therefore, this research will present process technology necessary to achieve high yields in FCIP assemblies using no-flow underfills and investigate the underlying problem of underfill void formation in these assemblies. The plausible causes of void formation will be investigated using experimental techniques. The techniques will identify the primary source of the void formation. Besides, theoretical models will be established to predict the number of voids and to explain the growth behavior of voids in the FCIP. The established theoretical models will be verified by experiments. These

models will validate with respect to the relationship between process parameters to achieve a high yield and to minimize voids in FCIP assemblies using no-flow underfill materials regarding process as well as material stand points. Eventually, this research provides design guideline achieving a high, stable yield and void-free assembly process.

CHAPTER 1

INTRODUCTION

1.1 PROBLEM STATEMENT

Increasing demands on high performance devices such as microprocessors, graphic devices, and high speed memory applications initiated the advent of Flip Chip in Package (FCIP) technology in the electronics packaging industry. Such high demands are driving Input/Output (I/O) counts from 1,000 to 5,000 and bumping pitches down to 100 um, according to the International Technology Roadmap for Semiconductors (ITRS). Indeed FCIP has been widely used for high performance device packaging solutions with high I/O, fine pitch flip chips due to advanced electrical, thermal, and form fact performance of FCIP technology. The FCIP assembly process can be achieved using advanced materials systems called underfills, which help to mitigate the effects of large CTE mismatch between silicon die and organic substrate. The conventional material is capillary flow underfill; a more recently developed material is a no-flow underfill containing fluxing agents. The no-flow underfill materials are deposited onto the substrate before a chip is placed. Next, the silicon chip is placed on the substrate causing squeezing flow of the underfill material. Then, both metallurgical solder interconnects and underfill curing is simultaneously achieved during a single reflow process. Consequently, several process steps can be eliminated to save the process time and cost using no-flow underfill, compared to conventional capillary flow underfill process as illustrated in Figure 2-3 [1, 2]. On the other hand, the assembly process using no-flow underfills has narrowed the feasible assembly process conditions for high, stable assembly yields and high performance in reliability. In spite of such material limitation, a

high, stable yield assembly process was recently developed with a next generation commercial FCIP comprising high-lead solder bumps with eutectic lead-tin solder interconnects using no-flow underfill material [3-5]. The reported reflow process conditions were developed using systematic experiments. The methodologies are described in Figure 1-1. First, the underfill material evaluation determined the stable temperature range of no-flow underfills for the solder wetting. Afterwards, the solder wetting quality was quantitatively determined to determine process conditions using the wetting study. Next, the assembly conditions was optimized using low cost flip chip packages with full area array solder interconnects, FA10. Then a high yield, stable assembly process was achieved as described in Appendix A. The systematic experiments achieved a high yield assembly process with a wide process window that was validated using Design of Experiment (DOE) technique. Meanwhile, a large number of voids were observed, that could cause defects such as solder bridges and solder joint cracks possibly resulting in early failure in thermal reliability [6-10]. The underfill voiding among solder joints was observed using an optical micrograph of a cross section of FCIP structures in Figure 1-2-(a) and (b). In addition, a C-mode Scanning Acoustic Microscopy (C-SAM) in-plane view confirms multiple void areas in the underfill between the test ASIC and substrate as shown in Figure 1-2-(c).

Typically, a high yield assembly process can be achieved with high values of reflow process design parameters such as high ramp rate, long time above liquidus, and high peak temperature. Potentially, the high values can cause a large number of voids in FCIP. Actually, a large number of voids is found among solder interconnects in FCIP (see Figure 1-2). They can propagate, grow, and produce defects such as solder joint cracking

and solder bridging, which can severely reduce reliability [6],[7]. Indeed, while a number of studies have addressed the effect of voids on reliability in FCIP, none has identified the causes of void formation in the FCIP using no-flow underfills by theoretical consideration. In addition, the plausible causes of void formation have been thoroughly investigated by several works. However, existing research does not provide a general answer to the cause of void formation in FCIP assembly using no-flow underfills.

In order to reduce the underfill voids or to achieve the void-free flip chip assembly using no-flow underfill materials in high I/O and fine pitch interconnects by proper material selection and process development, it is necessary to understand the void formation mechanism. Therefore, this thesis research investigated the effects of three plausible causes, including process conditions, material properties and chemical reactions, of void formation in FCIP using no-flow underfill through a systematic experimental approach. The primary goal was to identify the primary factors and the main source of underfill voiding in FCIP during assembly process. The secondary goal was to determine process conditions enabling a high, stable yield and void-free assembly process using experimental techniques. Next, these investigations were modeled to explain the mechanism of void formation in assembly process with high I/O, fine-pitch flip chip. Classical theories were adapted to predict the behavior of voids in the FCIP. These theoretical models were verified by experimental techniques. The above mentioned systematic research provided a physical understanding of mechanism of void formation, nucleation, and dynamic behavior in a flip chip assembly process using no-flow underfill.

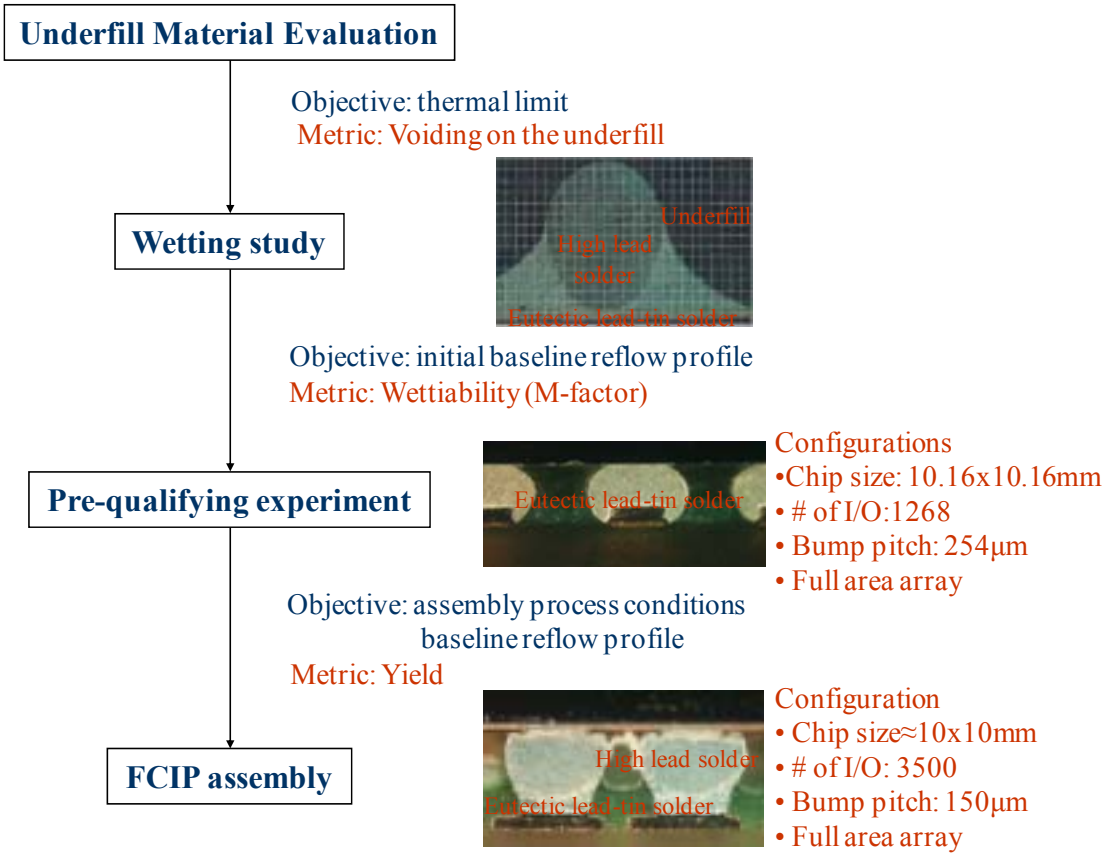
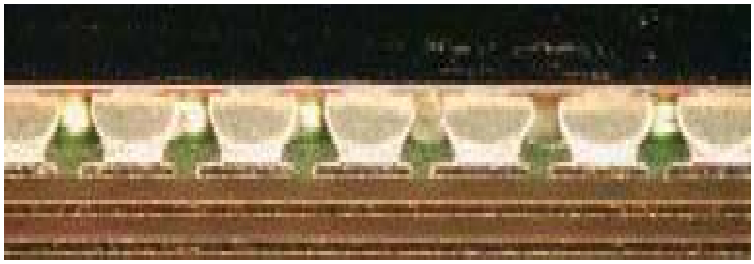
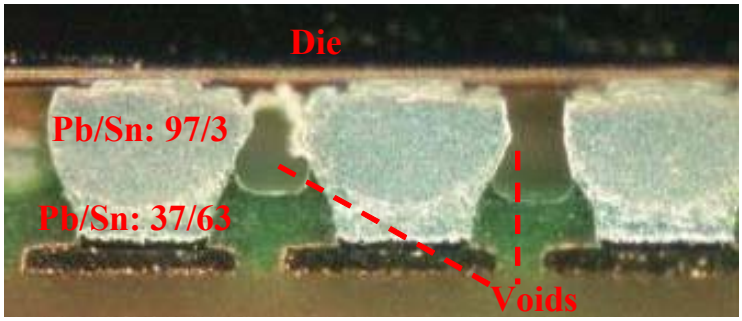


Figure 1-1 Assembly process development procedure using commercial no-flow underfill materials with a high I/O, fine-pitch flip chip



(a)



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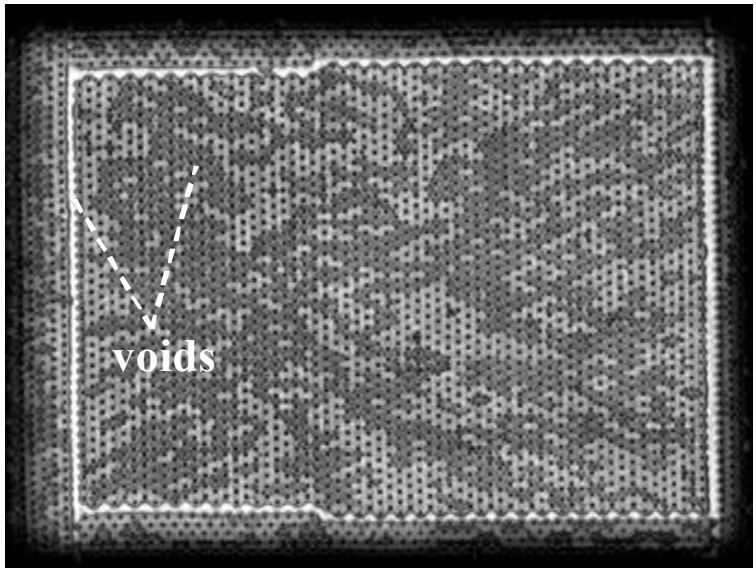


(c)

Figure 1-2 Micrographs of FCIP built using no-flow underfill material under the reflow conditions of ramp rate: 2.1 °C/s, reflow time: 70sec, peak temp: 225 °C

(a) cross-sectional view of flip chip solders joints (magnification: 100X), (b) cross-sectional view of flip chip solders joints(magnification: 200X), and (c) C-SAM analysis [8]

1.2 RESEARCH OBJECTIVE

The main research objective is to provide a physical understanding of the plausible causes of voiding for flip chip in package assemblies enabling assembly of high I/O density, fine pitch ASICs using analytical experimental techniques supplied by classical bubble nucleation and growth theories and experimental validation. The following tasks were performed in this research.

(1) Investigation of plausible causes of void formation in no-flow assembly process: The source of void formation in Flip Chip in Package (FCIP) was studied by many other researchers. Upon the review of literature, process conditions, material properties and chemical reaction are potential causes for void formation in FCIP. The plausible causes were investigated to identify the primary factor affecting underfill voiding using experimental techniques.

(2) Development of a void mechanism induced by chemical reaction: The first task found the primary factor of voiding. The findings suggested that a chemical reaction plays a role in underfill voiding in no-flow assembly process. The chemically induced voiding would be validated using analytical experimental techniques.

(3) Development of a void nucleation and growth model: A classical bubble nucleation theory was applied to explain void nucleation in molten no-flow underfill in conjunction with thermal effects of reflow process. Indeed, the thermal energy was transferred to the source of the void and the void then grew to critical size, which can produce a void in underfill. Once a void has grown to critical size, the behavior of the void was explained using classical bubble growth dynamics. The theoretical model could be used to model voiding particularly, the primary source of voids, the nucleation of

voids, and the behavior of voids in assembly process. Moreover, the developed model validated experimentally using commercial FCIP and several types of test vehicles.

(4) Determination of the assembly process conditions to minimize the amount of underfill voiding and to achieve a high, stable yield process (Design Guidelines): The process parameters were optimized to reduce the number of voids using parametric studies in FCIP using no-flow underfills based on the void formation model. Thus, the methodologies would find the feasible process conditions for a high, stable yield and void-free assembly process with high I/O, fine-pitch flip chip using no-flow underfill materials.

1.3 THESIS STRUCTURE

Chapter 2 presents the flip chip technology of microelectronics packaging and the typical assembly processes such as capillary assembly process and no-flow assembly process. In addition, this chapter reviews the previous studies on the causes of void formation in microelectronics packaging industry and in general manufacturing industry.

Chapter 3 describes experimental techniques to investigate the plausible causes of void formation, such as process conditions, material properties and chemical reactions in underfill and to suggest the mechanism of void formation. Thus, this chapter describes the experimental setup and test vehicle configuration.

Chapter 4 presents the identification of the primary source of void formation to provide a design guideline for the process conditions of a free-void assembly process by characterizing underfill materials.

Chapter 5 describes experimental techniques to investigate the effects on underfill voiding to minimize the number of voids in the assembly process by characterizing process and material.

Chapter 6 presents the modeling of void nucleation and void growth with thermal effects from the reflow assembly process using classical nucleation theory and bubble dynamics respectively.

Chapter 7 provides design guidelines to minimize underfill voiding.

Chapter 8 summarizes the conclusions of this research.

Chapter 9 discusses the contribution from this novel research and presents several recommendations for future work.

CHAPTER 2

BACKGROUND

2.1 OVERVIEW OF FLIP CHIP PACKAGING TECHNOLOGY

2.1.1 Introduction

Extremely fine pitch, small diameter I/O, and high I/O density can be achieved by flip chip technology [9-12]. Flip chip components differ in several ways from traditional packaging technologies such as wire-bonding and Tape Automated Bonding (TAB). For one, the I/O face downward and are typically connected to the substrate by solder bumps in a perimeter or area array I/O configuration. Secondly, the flip chip is a bare die, meaning that no additional packaging covers the silicon chip as shown in Figure 2-2. Flip chip technology was first seen in 1964 when IBM developed C4 (controlled collapse chip connection) technology for use in their mainframe computers. The C4 design used different Under Bump Metallization (UBM) and solders bump metallization. Figure 2-1 illustrates a typical schematic of Under Bump Metallization (UBM) structure. The UBM in the second step of the flip chip manufacturing process is to deposit metal layers. UBM consists of several layers, each with a specific purpose. The first deposited layer is an adhesive that adheres well to the bond pad metallization and the silicon dioxide or silicon nitride passivation layer. Chromium or Titanium-Tungsten is usually used for the adhesion layer. A barrier layer is deposited to prevent diffusion of metals or ionic contaminants into the chip metallization in the second layer. Barrier layer metallurgies can be Chromium, Tungsten, Chromium-Copper, or Nickel, among others. Copper is usually deposited on the wetting layer in the third layer. Nickel, Palladium, etc. can also

be applied to the wetting layer. The final layer, applied to prevent the formation of oxides, is a protective thin layer of gold.

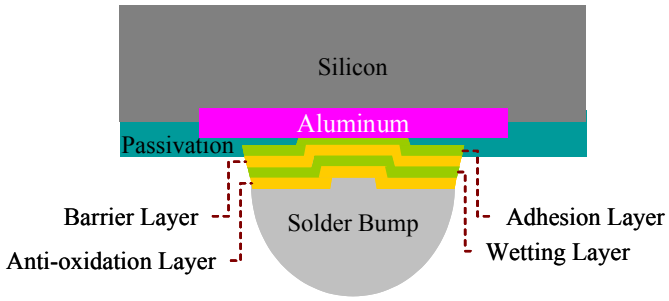


Figure 2-1 Schematic of flip chip UBM structure

The solder metallization of C4 Technology uses high-lead solder bumps (usually 93Pb-7Sn). The solder bumps are deposited on the active surface of the semiconductor chip that connects to matching wettable substrate pads. The active face of a chip is flipped over on its face to substrate and thus this technology is commonly referred to as a flip chip.

Typically, the flip chip has four interconnection methodologies as described in Figure 2-2. The Figure 2-2-(a) shows a schematic of the high lead on eutectic solder interconnection. This technology serves to help maintain the offset gap between chip and substrate since the high lead sphere does not melt during the eutectic solder reflow. Therefore, the offset gap between chip and substrate allows for proportionately smaller pitches than eutectic solder (37Sn-63Pb) joints as shown in Figure 2-2-(b) since the eutectic solder requires significantly wide distances between bump centers during a reflow process. Consequently, the composite high lead on eutectic solder joint has a higher fatigue life than eutectic solder since the taller standoff height is providing a lower CTE gradient between chip and substrate. Meanwhile, the singular eutectic solder

interconnect is more cost effective than any other methodologies. Thus, eutectic solder interconnect has been most widely accepted in Surface Mount Technology.

Gold stud bumped die is used in both interconnection illustrated in Figure 2-2-(c) and (d). The application of Figure 2-2-(c) adapts an Anisotropic Conductive Film (ACF) which has metallic conductive filler spheres (nickel and gold coated nickel or gold coated or nickel-gold coated polymer) to form the interconnection with substrate pads. The interconnection using ACF requires high accuracy placement because the materials do not provide self-alignment like solders wetting. Besides, anisotropic conductive adhesive require relatively high bonding forces in order to make good electrical contact.

In the interconnection of Figure 2-2-(d), gold bumped flip chips was bonded to the substrate metallization using a conductive adhesive paste. Typically, the isotropic conductive adhesive is a thermosetting polymer filled with conductive particles. The conductive adhesive commonly uses an epoxy filled with silver flake particles.

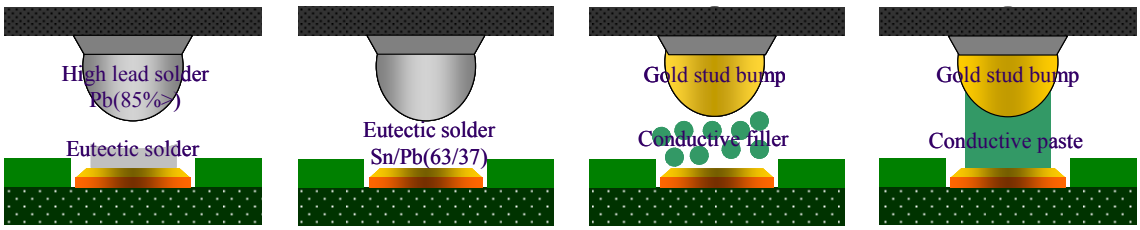


Figure 2-2 Flip chip interconnection methodologies: (a) high-lead bumped chip with a eutectic pad on the substrate, (b) eutectic bumped chip, (c) gold stud bump in an anisotropic conductive film, and (d) gold stud bumped chip

2.1.2 Conventional Capillary Flow Underfill Flip Chip Assembly Process

Figure 2-3-(a) illustrates the conventional capillary flow flip chip process. First, the flux is applied to the substrate pad or the die is dipped into a flux reservoir in order to remove solder oxidation and reduce solder surface tensions to support wetting. Then the chip is aligned with the substrate and placed on the substrate by a precise chip placement machine. Once it is aligned, the assembled package is reflowed in a reflow oven to make the solder bumps wet on the bond pad. After the reflow process, flux residues are cleaned off and underfill is dispensed along the edge of the chip, filling the narrow gap between the chip and the substrate by capillary force. Finally the underfill is cured in a thermal batch oven.

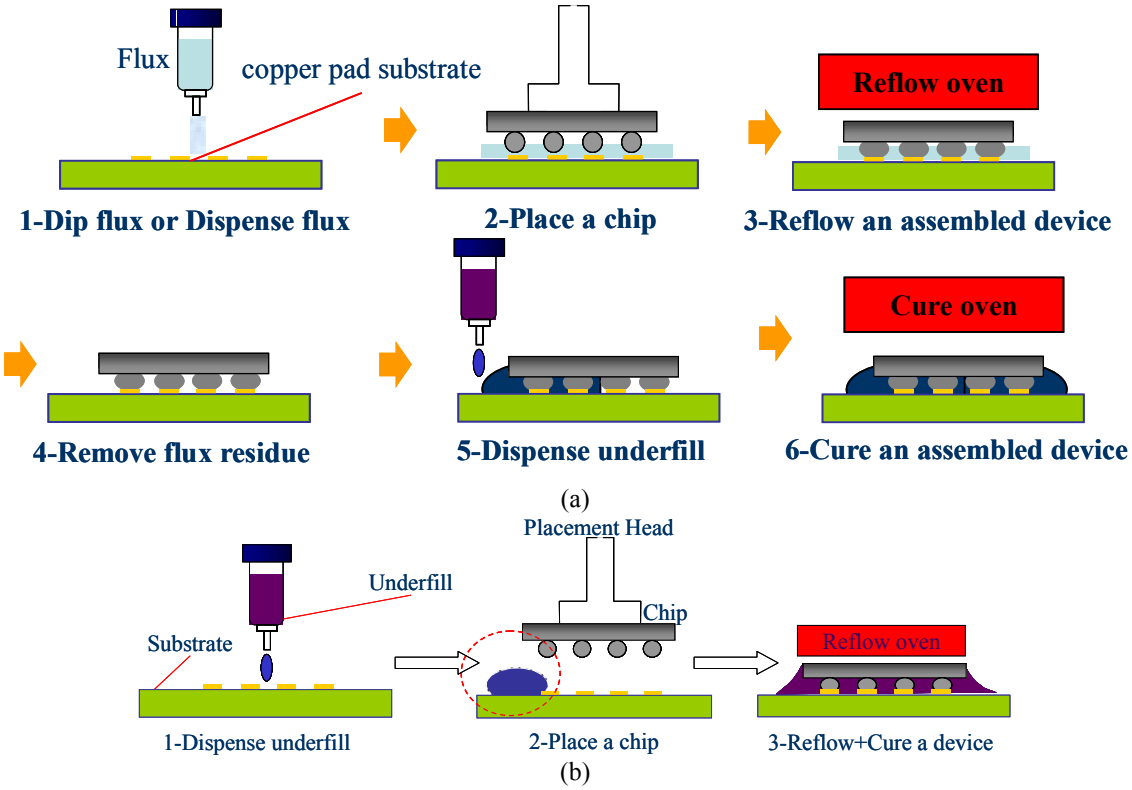


Figure 2-3 Schematic of flip chip assembly process: (a) conventional assembly process and (b) hybrid no-flow assembly process [8]

2.1.3 No-Flow Underfill Flip Chip Assembly Process

Motorola pioneered a process that combined the underfill and flux into one material. This process later became known as a no-flow underfill process, because the underfill is dispensed onto the substrate and flows quickly by compressive force when a die is placed. The no-flow underfill material does not contain silica filler because it interferes with solder interconnects. The absence of silica filler increases the Coefficient of Thermal Expansion (CTE) of no-flow underfill. The higher CTE of the no-flow underfills result in higher solder interconnect stresses, causing delaminating and cracks. Such limitation prevents high reliability.

Meanwhile, the hybrid nearly void-free flip chip assembly process using no-flow underfill, shown in Figure 2-3, eliminates the most time consuming steps such as flux cleaning, underfill flowing, and underfill curing that are found in the conventional assembly process [13]. First, a controlled volume of underfill material is dispensed along the edges of the bond pads on the substrate. Next, the chips are aligned to the bond site and are placed on the substrate, compressing the liquid underfill to form a compression bond to the substrate. Finally, the solder interconnects are reflowed while the polymer encapsulant underfills are simultaneously cured. Care is taken here to prevent premature gelation of the underfill prior to solder reflow using innovative no-flow underfill material. This no-flow underfill provides latent gelation such that the cure reaction is inhibited until a critical temperature is reached above the solder liquidus temperature [14]. In addition, this no-flow assembly process increases the throughput of flip chip processing [15-17].

2.2 OVERVIEW OF VOID FORMATION

On the review of existing studies, the source of void formation was not induced by a single factor. Several complicated factors combined together affecting void formation in a flip chip assembly process. This chapter reviews the negative effect of voids on the performance in thermal reliability, and classical void nucleation and growth theories. Besides, void formation mechanisms will be reviewed in polymers industry and electronics packaging industry.

2.2.1 The Effect of Underfill Voids on Thermal Reliability in the Electronics Package Industry

The effect of voids in solder joints or underfill has received significant attention in the literature because it has been considered a critical defect, causing early failure in reliability tests. In general, thermal reliability testing exposes electronic devices to cyclic thermal stress. The thermal stress in thermal cyclic tests was reviewed by others using theoretical analysis and experiments [18, 19]. Typically Michaelides investigated the effect of void size on fatigue life thermal reliability using Finite Element Method [20]. Colleara found a void adjacent to solders induced short failure due to solders bridge. The cyclic stress causes solder bumps to slowly move through the existing underfill voids and deforms permanently. The tendency is called creep. The creep mechanism drives a solder to extrude through the voids, subsequently causing bridges between solders. It occurs as a result of long-term exposure to levels of stress below the yield strength of solders. Consequently, the deformation makes a bridge between solder joints causing failure due to electrical shorts [21].

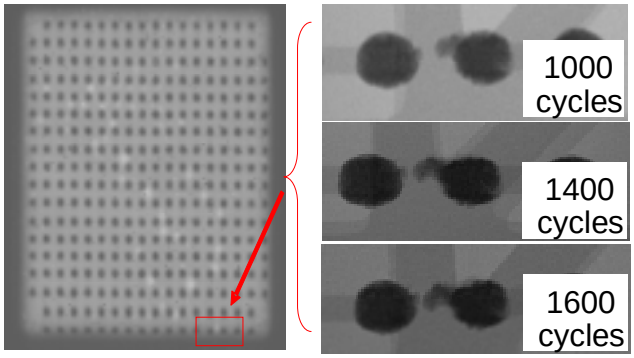


Figure 2-4 Micrographs of FA10-2 failure due to sold bumps extrusion in a void during thermal cyclic testing

Yunus et al. investigated the effect of voids on the reliability of Ball Grid Array (BGA) / Chip Scale Packaging (CSP) [22]. His study focused on investigating the effect of void size, location and frequency on the reliability of solder joints. Basaran et al. studied the effect of pre-existing underfill flow-induced voids on the failure mechanism of flip chip solder joints under high electrical current density using experiments [23]. Colella et al. showed solder extrusion failure in thermal reliability testing caused by existing voids using experimental techniques [24]. Orain et al. showed the risk of void with crack occurrence using the finite element method. They also studied the interaction of these two failure modes (voiding and cracking) [25].

2.2.2 Classical Bubble Nucleation and Bubble Growth

A void nucleation and a void growth in flip chip assembly process have similar mechanisms compared to the classical bubble nucleation and bubble growth. The classical theories have been widely studied by others. Bubble nucleation in a homogenous liquid was studied by many researchers [26-30]. Gibbs established the generalized formulation widely used recently for predicting the formation of a bubble nucleus in a homogenous fluid [31]. Then, nucleation at the interface between two homogenous liquids was studied, defined as heterogeneous nucleation [32-34]. Later on, Fisher examined bubble nucleation at a smooth rigid interface which can be applied to the voiding nucleation model between solders and no-flow underfills [35]. Turnbull developed the kinetics of heterogeneous nucleation theory between liquid and glass surfaces [36]. With the above mentioned theories, numerous adaptations have been proposed in polymers. The free energy has been modified to account for changes in the polymer free-volume by Colton. In addition, Colton studied on the void nucleation to determine the density of voids in polymers, which is relatively similar to the core materials of no-flow underfills [37]. The nucleated voids larger than the critical size will further grow by the gas diffusion through liquid underfill. The bubble growth model was described by Advani et al. in a Newtonian fluid driven by gas diffusion [38-41]. Venerus et. al analyzed the growth of a single spherical gas bubble surrounded by a viscoelastic liquid under isothermal conditions. The diffusion-induced growth of bubbles in a fluid presented a complete set of equations for bubble growth [41]. The bubble growth was examined in an infinite expanse of viscoelastic fluid [38, 42-44]. Afterwards, studies were conducted on diffusion-driven bubble growth in Newtonian, power-law, and

viscoelastic melts with the mass and momentum transfer properly coupled [39-41]. In a polymer industry application, Youn intentionally foamed micro size bubbles to produce light-weight polyester composites. In addition, he explained gas diffusion induced bubble growth in a polymer melt using a theoretical analysis [45]. Later on, Feng et al. developed a bubble growth model formed by a physical blowing agent dissolved in a polymer melt that contains particulate nucleating agents. Once nucleated, the bubbles grew as the dissolved gas diffuses through the polymer melt into the bubbles in isothermal condition [46]. On the contrary, Wang et al. modeled bubble growth dynamics in polymer under non-isothermal condition [47].

2.2.3 Void Formation Research in Polymers Industry

The core material of no-flow underfill is polymers. Therefore, void formation in polymers industry was reviewed. Several researches were conducted to control bubbles for the development of polymer assembly process in manufacturing industry. Most of all focused on development of polymers assembly process to save raw materials with maintaining original mechanical properties. First, Youn developed an assembly process to reduce the weight of polyester composites without sacrificing mechanical property by replacing filler particles with microcellular voids [45]. Next, Colton explained bubble nucleation in thermoplastic polymers and developed the model predicting the number of bubble nucleation [48]. Then, Baldwin developed a processing system for the continuous production of microcellular thermoplastic sheets using gas and polymer solution [49].

2.2.4 Void Formation Research in Electronics Package Industry

A large number of existing studies on void formation can be classified into thermal induced voids and non-thermal induced voids. For thermally induced voids, Goenka et al. determined factors affecting the formation and growth of voids in flip chip solder bumps with thermal effect from the assembly process using a theoretical approach. The theoretical analysis was conducted with the assumption that unidentified reactions caused bubble nucleation during the reflow process [50]. They also predicted the motion and coalescence of bubbles in flip chip solder bumps during the reflow process [51]. Later on, Hurley et al. suggested a combined model for void formation with solder melting, underfill curing, and underfill volatilization to explain the mechanism of voiding in a flip chip device using experimental techniques [52]. On their conclusion, some uncured volatile components exposed to temperatures above the boiling point explode, thereby producing voiding. Wang studied the formation of voids during the reflow process by carrying out experiments to investigate the effect of the heat flux on void nucleation. His investigations were to provide the best reflow profile to minimize voids in his assembly process [53]. Later on, he reported a series of studies of void bubbles within molten solder bumps in flip-chip connections using experimental techniques, the results characterized direction of heating influences on the formation of void [54, 55].

Afterwards, Lee et al. also studied the motion of void bubbles within molten solder bumps. In this work, surface tension variation on the outer surface of the molten bump drives a flow that is transmitted to the bump interior by viscosity. Bubbles inside the molten bump grow from collisions with other bubbles. A computer model of this process has been developed to simulate the motion of molten solder [56]. Similarly, Lai studied

the mechanism of pore growth in solder and conducted an investigation on pore-free reflow soldering using an experimental approach [57]. His investigation enabled the control of pore growth and the development of a pore-free soldering process.

Regarding non-thermal induced, Milner et al. studied the effect of substrate design and substrate features on underfill flow induced void formation [1]. They investigated the effect of pad geometry on the underfill void formation and found the underfill flow characteristics had a major effect on voids. Colella et al. identified that the process design parameters such as underfill dispense pattern, placement parameters, and pad design are some significant factors, affecting void formation in no-flow assembly process [17].

The above-mentioned research on the formation of voids in the electronics packaging industry has typically assumed that the source of void formation is volatilization of uncured components in the no-flow fluxing underfill material, and the research mainly focused on the growth or behavior of formed voids. Otherwise, the source of voids was investigated with the view point of an underfill flow, which can explain a small amount of voiding. That is, no theoretical fundamentals for the formation of large numbers of voids induced by chemical reaction have been established. The chemical reaction has been considered as the main source of voids in existing studies, but the assumption has not been verified for the source of the chemical reaction induced voids. Namely, current literature is not able to provide a general and explicit answer to the needs. It is imperative to investigate the primary factor and identify the source of underfill voiding. Furthermore a theoretical model of void formation is required to relate chemical reaction with conservative mechanical models to examine void nucleation, void formation, and void growth during reflow process in flip chip.

CHAPTER 3

VOID FORMATION IN FLIP CHIP

3.1 INTRODUCTION

In this chapter, systematic experimentations investigate the plausible causes of void formation in FCIP using no-flow underfill with different types of test vehicles. Figure 3-1 describe the plausible causes of void formation in flip chip assembly process using no-flow underfill on the existing studies [1, 16, 17, 24, 52, 58-60]. From review of literature, the plausible causes of underfill voids can consider process conditions, material properties and chemical reactions between the solder bumps and no-flow underfill materials. Among them, the chemical reaction between solder and underfill during solder wetting and underfill curing process were suspected as one of the most significant factors for void formation in high I/O and fine pitch FCIP using no-flow underfill materials. The hypothesis was verified to identify the causes of void formation using experimental techniques.

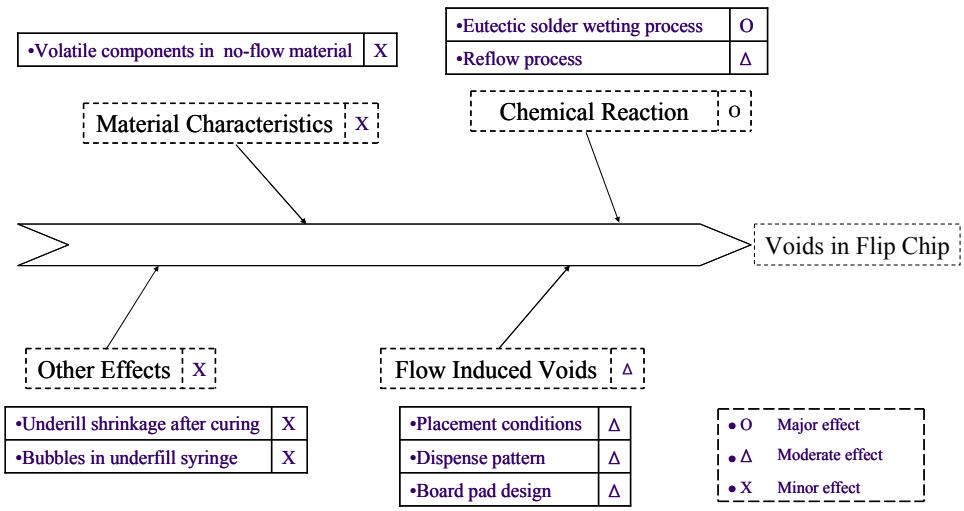


Figure 3-1 Plausible causes of void formation in no-flow assembly process

Commonly occurring void patterns in FCIP assemblies are shown in Figure 3-2. The central scanned figure, which was achieved using a C-mode Scanning Acoustic Microscopy Technology (C-SAM), has a large number of voids. The amount of voiding is large enough to cause critical reliability failure during operation. This pattern is also verified using planar cross sectioning. Both analytical technologies confirm that FCIP has a lot of voids the after reflow process which produces high assembly yield. Therefore, the fundamental study of void formation is required to explain void formation resulting from an assembly process with high yield.

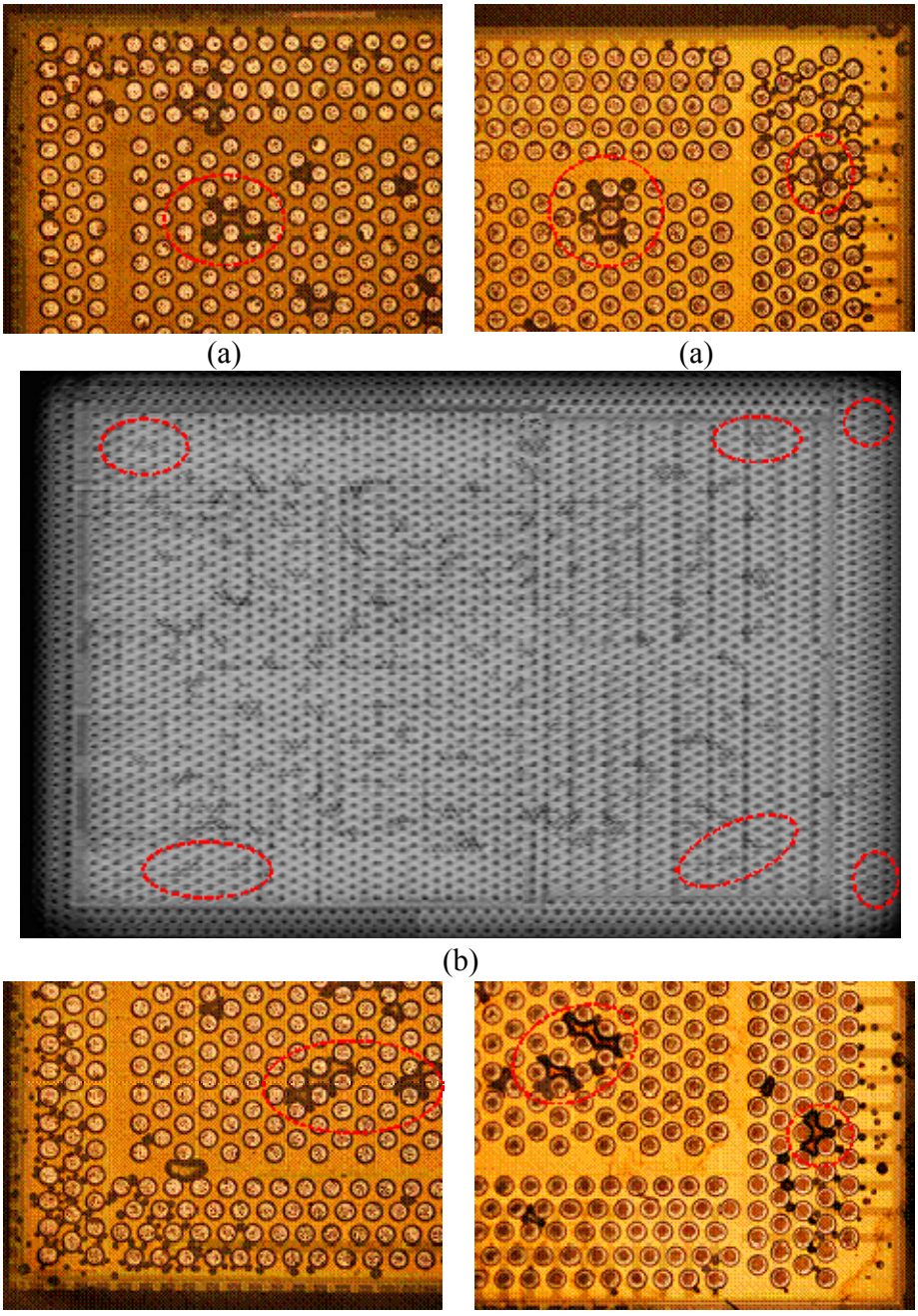


Figure 3-2 Micrographs of a high yield assembly with underfill voiding: (a) C-SAM analysis and (b) planar section showing voids in the FCIP

Three void formation studies were conducted to investigate plausible causes of void formation in this FCIP assembly process using several test vehicles described in Table 3-2 with a commercial no-flow underfill (see Table 3-1). The commercial no-flow was used as the baseline underfill to characterize process conditions and to formulate material to minimize the amount of underfill voiding in the further studies of described in the other chapters.

Table 3-1 Material property of a commercial no-flow underfill

Material property	Value
Glass transition temp. (Tg)	81 °C
Viscosity @ 25°C	3,100 cp
Flexural modulus	2.6 GPa
Thermal conductivity	0.18 W/mK
Coefficient of thermal expansion below Tg	190 ppm/°C
Cure condition	a standard SMT reflow incorporating at 150-170°C dwell prior to ramp up to reflow temperature

Table 3-2 Configuration of test vehicles used in the study 1, 2 and 3

Experiment	Test vehicle	Category	
Void formation study1 (Effect of underfill flow on void)	Test vehicle1-1	Bump material	97Pb-3Sn
		Chip size(mm)	< 10 x 10
		Bump count	3000 >
		Bump pitch	< 200μm
		Bump layout	Full area
		Substrate material	36Pb-63Sn
Void formation study2 (Effect of material characteristic on void)	Test vehicle 2-1	Die material	Glass cover
		Substrate size(cm)	1x1
		Substrate material	ENIG
		Underfill	No-flow underfill
	Test vehicle 2-2 / Test vehicle 2-3	Die material	Glass cover
		Bump material	36Pb-63Sn / In
		Substrate size(cm)	1x1
		Substrate material	ENIG
		Underfill	No-flow underfill
Void formation study3 (Effect of chemical reaction on void)	Test vehicle 3-1 (FA10-4 substrate)	Die material	Glass cover
		Bond pad	copper
	Test vehicle 3-2 (FA10-4 die)	Bump material	36Pb-63Sn
		Chip size(mm)	10.16x10.16
		Bump count	1268
		Bump pitch	254 μm
		Bump layout	Full area
	Test vehicle 3-3 (FCIP substrate)	Die material	Glass cover
		Bond pad	36Pb-63Sn
	Test vehicle 3-4 (FCIP die)	Bump material	97Pb-3Sn
		Chip size(mm)	< 10 x 10
		Bump count	3000 >
		Bump pitch	< 200μm
		Bump layout	Full area

3.2 EXPERIMENTAL APPROACH

Three experiments were designed to investigate the plausible causes of void formation with FCIP using commercial no-flow underfills. Each experiment was designed on the results from preceding studies due to a limited number of commercial FCIP test vehicles (TVs) available. A placement process void formation study, termed void formation study 1, was conducted to check the effect of underfill flow on the void formation. A material characteristics void formation study, termed void formation study 2, was performed to investigate whether one of the components in the no-flow underfill was volatile and subsequently outgassed to form a void in the FCIP under reflow process conditions. A chemical reaction void formation study, termed void formation study 3, was conducted to understand how the no-flow underfill material reacted with the eutectic solder plated substrate pads and the high lead solder bumps during the reflow process. This study also sought to find any possible chemical reaction that would cause underfill voiding.

3.2.1 Void Formation Study 1 (Effect of Underfill Flow on Void)

The main objective of void formation study 1 was to determine the effects of the substrate pretreatment and chip placement process conditions on underfill flow as it impacts void formation in high I/O density, fine pitch FCIP. The commercial no-flow underfill material, which showed the best performance in an assembly process development as described in Appendix A, was selected for this void formation study 1 [4, 5]. The material properties of no-flow underfill used in this study are shown in Table 3-1. The process specifications of pretreatment, placement force, and placement dwell time are summarized in Table 3-3. The placement force is defined as the applied force on a

chip during the placement process, and placement dwell time is defined as the time the placed chip is held during a chip placement process. As the chip placement speed, among the placement control parameters, was reported as an insignificant factor affecting underfill voids [17], the placement speed was not included in the design matrix for the void formation study 1.

Table 3-3 Variation of parameters in void formation study 1

Levels/Factors	Pretreatment	Placement force	Placement dwell time
Per Underfill (3 replicates)	Plasma 1	Low (5N)	Low (0 sec)
	Plasma 2	High (15N)	High (10 sec)

Prior to the assembly process, all moisture was driven out of the boards with exposure to an isothermal environment at 125 ºC for 3 hours. This bake out time was determined from a previous bake out experiment and was sufficient to avoid moisture out-gassing of the boards [61], [62]. The plasma pretreatment for substrate surface cleaning was applied to the moisture free FCIP test vehicle using a March AP-1000 plasma treatment system with two recipes for 10 minutes. The recipes were applied at the conditions of 150 mTorr (pressure) and 200 W (power). In detail, the plasma 1 recipe was a plasma treatment using pure argon (Ar) to remove contamination, and the plasma 2 recipe was a plasma treatment using 90% nitrogen (N_2) and 10% hydrogen (H_2) mixture to activate the surface and change the surface energy.

The FCIP test vehicle (TV) 1-1 used in void formations study 1 is specified in Table 3-2. The amount of underfill voiding was measured at different pretreatment and placement process conditions based on a full factorial Design of Experiment (DOE). According to the DOE shown in Table 3-4, FCIP TVs were assembled using a

commercial no-flow underfill and then were cured at an isothermal temperature of 130°C for 1 hour in a convection oven to eliminate the reflow process thermal impact on void formation. The impact of underfill flow on voids was determined by the area percentage of voids.

Table 3-4 DOE of void formation study 1

Run order	Pretreatment	Placement Force	Placement dwell time
1	1	1 (Low: 5N)	2 (High: 10 sec)
2	2	1 (Low: 5N)	1 (Low: 0 sec)
3	2	2 (High: 15N)	2 (High: 10 sec)
4	2	2 (High: 15N)	2 (High: 10 sec)
5	2	1 (Low: 5N)	1 (Low: 0 sec)
6	1	2 (High: 15N)	1 (Low: 0 sec)
7	1	2 (High: 15N)	1 (Low: 0 sec)
8	2	2 (High: 15N)	2 (High: 10 sec)
9	1	1 (Low: 5N)	2 (High: 10 sec)
10	2	1 (Low: 5N)	1 (Low: 0 sec)
11	1	2 (High: 15N)	1 (Low: 0 sec)
12	1	1 (Low: 5N)	2 (High: 10 sec)

3.2.2 Void Formation Study 2 (Effect of Material Characteristic on Void)

Void formation study 2 was designed to investigate whether the volatilization of uncured low-molecular weight components in no-flow underfill were the cause of voiding. The low-molecular weight components might be the main source for underfill voiding when exposed to temperatures above the low molecular weight compounds boiling point during the reflow process.

Void formation study 2 used three test vehicles, designated test vehicle 2-1, test vehicle 2-2, and test vehicle 2-3. Test vehicle (TV) 2-1 consisted of a covered glass slide and an Electroless Nickel Immersion Gold (ENIG) plated substrate. Test vehicle (TV) 2-2 consisted of a cover glass slide, four Sn/Pb (63/37) solder spheres, and an ENIG plated substrate. Besides, TV 2-3 was prepared to investigate the effect of solder materials on underfill voiding. Instead of Sn/Pb (63/37), a pure indium was placed on the underfill deposited substrate. The melting temperature of indium and eutectic (Sn63-Pb37) is 156°C and 183°C respectively. A major difference between TV 2-1, and TV 2-2 and T V2-3 is the presence of Sn/Pb (63/37) solder or Indium solder in the TV.

Prior to assembly, isopropyl alcohol (IPA) was applied to the surfaces of the test vehicles to clean them. After this cleaning process, the test substrates were baked at 125°C for 3 hours to avoid out-gassing from moisture on the substrate. Next, four solder spheres were placed on the ENIG substrate and a commercial no-flow underfill was dispensed onto the ENIG substrate. The Sn/Pb (63/37) solder spheres and Indium solders were placed on the underfill deposited ENIG substrate covered with a glass cover slide for TV2-2 and TV2-3 respectively as illustrated in Figure 3-3.

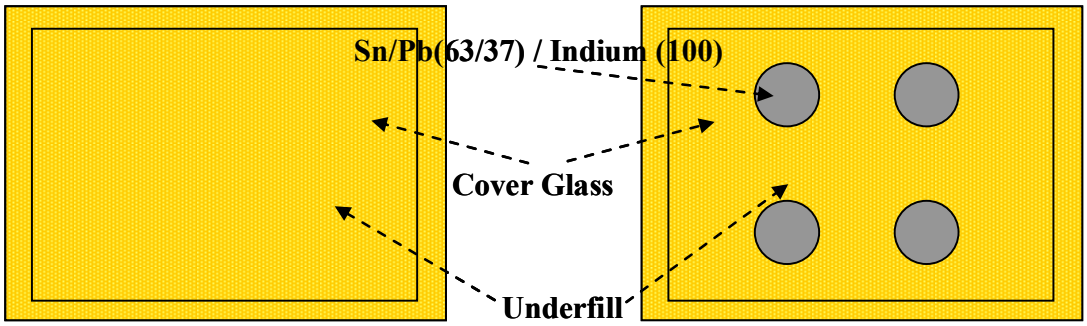


Figure 3-3 Schematic of test vehicles configuration used in void formation study 2: (a) TV2-1 without Sn/Pb (63/37) solders and (b)TV2-2 with Sn/Pb (63/37) solders and TV2-3 with Indium solders

The presence of initial voids trapped by placing a glass cover on the underfill deposited substrate was determined using an optical microscope. TV assemblies used in this study had no voids induced by a glass cover placement.

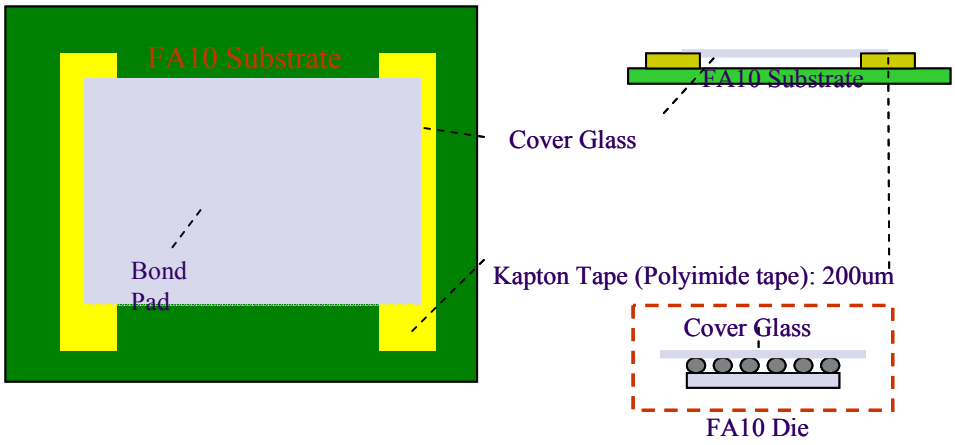
The TV 2-1 and 2-2 were reflowed on a digital hotplate with a thermocouple attached to the ENIG substrate to measure the surface temperature of the TVs. Two test vehicles were placed next to a thermocouple coupon on the heated plate. The assembled TV 2-1 and TV2-2 were reflowed from 100 °C preheating to 225 °C peak temperature, which was held for 1 minute to give enough time for solder wetting and underfill curing. Similarly, the TV 2-3 was reflowed at 180 °C peak temperature. The void formation behaviors of no-flow underfill material were observed during the reflow process under the optical microscope. Each test vehicle process was performed in replicates of three.

3.2.3 Void Formation Study 3 (Effect of Chemical Reaction on Void)

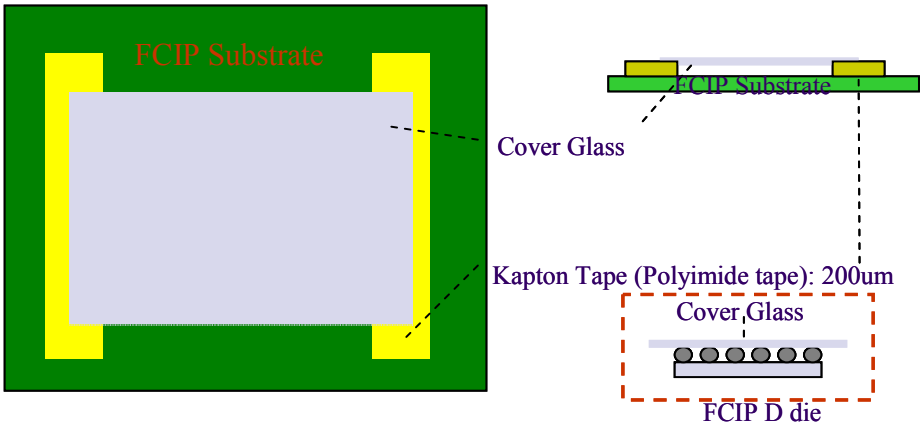
Void formation study 3 was designed to investigate the effect of chemical reactions between wetting molten solder and no-flow underfill using four test vehicles specified in Table 3-2. The first test vehicle is TV 3-1 which consisted of a glass cover on an underfill deposited FA10-4 organic substrate with copper finished metallization as illustrated in Figure 3-4-(a). The stand-off gap height was controlled using polyimide tape of 200μm thickness. Test vehicle 3-2 consisted of a glass cover and underfill deposited on a FA10-4 die as specified in Table 3-2 to confirm that Sn/Pb (63/37) has a strong impact on underfill voiding. Test vehicle 3-3 consisted of a glass cover and a FCIP organic substrate which had flip chip bond pads capped with a eutectic lead-tin (37-67) solder. A glass cover was put on the underfill deposited substrate with 200 μm standoff gap height using polyimide tape. Test vehicle 3-4 consisted of a glass cover on the underfill deposited FCIP die as specified in Table 3-2 to investigate the effect of high lead solder on underfill voiding at the lead-tin (37-67) solder reflow process condition. All four TVs were reflowed at the assembly process conditions specified in Table 3-5, which was used for achieving the high electrical yields with a flip chip assembly consisting of high lead solder bumps mounted on eutectic solder caps.

Table 3-5 Reflow profile for a high yield assembly

Ramp rate	Soak temperature	Soak time	183°C >	Peak temperature
2.1 °C/s	140 ~ 170 °C	50 sec	70 sec	225 °C



(a)



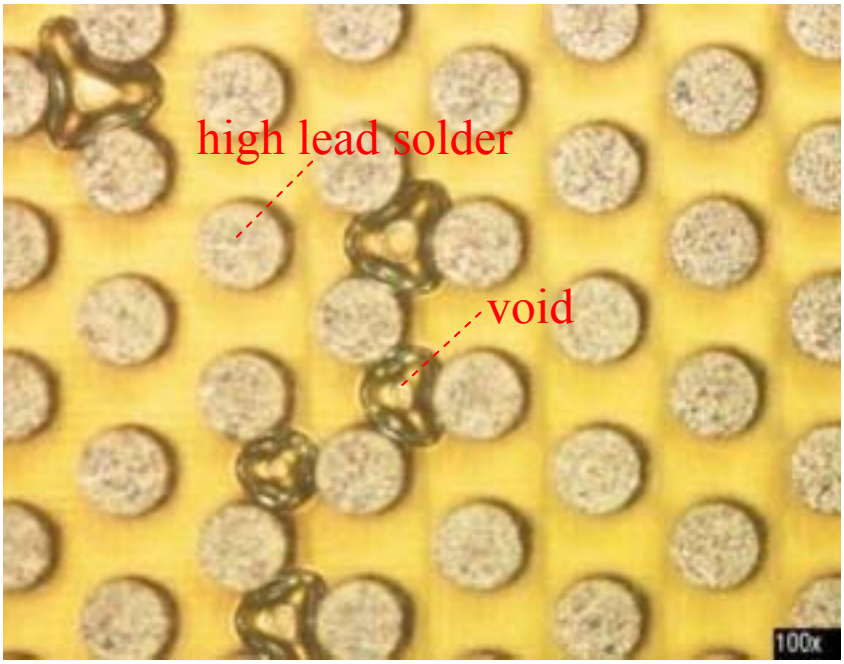
(b)

Figure 3-4 Schematic of test vehicles configuration used in void formation study 3: (a) TV3-1 (FA10-4 substrate) and TV3-2 (FA10-4 die), (b) TV3-3 (FCIP substrate) and TV3-4 (FCIP die)

3.3 EXPERIMENTAL RESULTS

3.3.1 Void Formation Study 1 (Effect of Underfill Flow on Void)

Figure 5-4-(a) shows a typical micrograph of a no-flow underfill voiding pattern among solder bumps under a particular reflow condition observed by planar cross-sectional analysis. Figure 5-4-(b) shows a typical scanned micrograph of no-flow underfill voiding using C-SAM. The C-SAM technique combined with MATLAB were used for quantitative analysis to compute the percentage of underfill voiding at different reflow conditions using image processing techniques. Post processing, the TVs were scanned using C-SAM, and an example scanned C-SAM image is shown in Figure 3-6-(a). The figure shows a grayscale pattern, where the darker gray and white regions indicate the regions of TVs containing underfill voids. The boundary of the voiding area is shown in Figure 3-6-(b) as detected on the converted image. The image was converted to black and white using own code on a commercial image processing program (MATLAB image process toolbox) for further analysis. At the same time, the area of underfill voiding in the FCIP TV was calculated using the software where white regions indicate regions of voids in the FCIP as shown in Figure 3-6-(c).



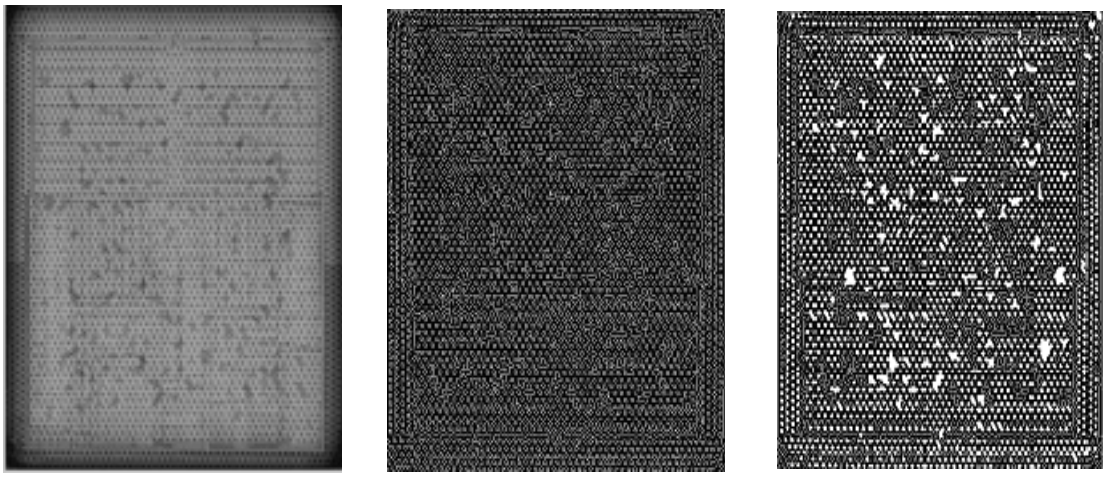
(a)

(b)

pretreatment: argon (10min), placement force: low (5 N), placement dwell time: high (10sec)

Figure 3-5 Micrographs of void formation study 1: (a) Planar-sectional view of a FCIP and (b) C-SAM analysis

Percent area voiding is defined as the percentage of the void area over the area of the die. The percent area voiding of the FCIP TV using no-flow underfill at each process condition was collected as shown in Table 3-6. The percent area voiding of the FCIP ranged from 0.000 to 0.706%. Analysis of Variance (ANOVA) technique was applied to the collected data in void formation study 1 to determine the magnitude level of each process factor to underfill void formation [63]. The sign "+" represents the intensity of process factor on the underfill voiding. The magnitude of main effects on underfill voids was described in Table 3-7 according to statistical analysis. The primarily, main effects plots, as shown in Figure 3-7, indicate the relative effect of each process parameter on voiding for the no-flow underfill.



(a) (b) (c)

Figure 3-6 Micrographs of image processing for voids detection: (a) original image using C-SAM, (b) detected the boundary of voids, and (c) detected voids

Table 3-6 Void percent area of void formation study 1 according to the design matrix

Order	Plasma pretreatment	Placement force	Placement dwell time	Voids (%)
1	1	1 (Low: 5N)	2 (High: 10 sec)	0.385
2	2	1 (Low: 5N)	1 (Low: 0 sec)	0.570
3	2	2 (High: 15N)	2 (High: 10 sec)	0.487
4	2	2 (High: 15N)	2 (High: 10 sec)	0.706
5	2	1 (Low: 5N)	1 (Low: 0 sec)	0.000
6	1	2 (High: 15N)	1 (Low: 0 sec)	0.071
7	1	2 (High: 15N)	1 (Low: 0 sec)	0.000
8	2	2 (High: 15N)	2 (High: 10 sec)	0.702
9	1	1 (Low: 5N)	2 (High: 10 sec)	0.215
10	2	1 (Low: 5N)	1 (Low: 0 sec)	0.567
11	1	2 (High: 15N)	1 (Low: 0 sec)	0.060
12	1	1 (Low: 5N)	2 (High: 10 sec)	0.432

Table 3-7 Summary of voiding results significance

	Cleaning	Force	time
p-value	++	0.887	+

\+ = <0.10 ANOVA p-value
++ = <0.05 ANOVA p-value
+++ = <0.01 ANOVA p-value

As a result, the plasma cleaning process might be a statistically moderate factor influencing the amount of underfill voiding. Placement dwell time appeared as a notable factor on the amount of underfill void formation. Placement force did not appear to be a major factor in void formation. A high value for placement dwell time increased the amount of void area. A detailed consideration of the results is necessary to explain the mechanism behind the statistical analysis. For example, the plasma 1 recipe using Argon gas is commonly used to remove contamination or micro-size particles on the surface, eventually achieving smoother surface. Therefore, TVs exposed to plasma 1 have fewer voids due to the laminar flow of underfill. On the contrary, the 90% nitrogen and 10% hydrogen mixture, used widely in the package industry as pretreatment, was selected for the plasma 2 recipe. Nitrogen was employed to promote the performance of wetting by activating the surface and hydrogen is used for the etching process. Thus, the roughness of TVs exposed to plasma 2 might be increased preventing the flow of underfill due to typical hydrogen etching characteristics thus causing an increased number of voids [64].

The effect of placement dwell time on voids can be explained only with further research. The current void formation study was designed narrowly to identify whether the underfill flow affects a large number of voids in high I/O, fine pitch FCIP assemblies not subject to a reflow process.

The percentage of voiding induced by underfill flow was lower than 0.0706%, as shown in Figure 3-6, whereas the current high yield assembly process resulted in approximately 65% voiding [4, 5, 58]. Thus, the underfill flow is not believed to induce the high percent area of void without a thermal effect such as the reflow process. The underfill flow-induced voiding pattern (as an example shown in Figure 1-2) which

formed among solders is not desirable for long-term reliability [17]. That is, the void percentages between high and low parameter levels in all three cases were not sufficient to account for the process induced voids. Hence, underfill flow-induced void design parameters generally have only minor effects on underfill voiding for the configuration studied.

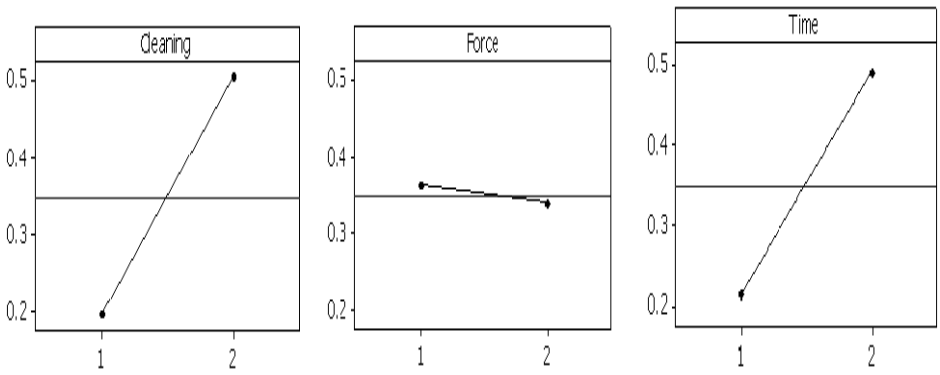


Figure 3-7 Main effect plots on void: (a) cleaning vs. void, (b) force vs. void, and (c) dwell time vs. void

3.3.2 Void Formation Study2 (Effect of Material Characteristic on Void)

The no-flow underfill was evaluated in void formation study 2 to investigate whether an underfill material has a volatile component which can potentially expand creating voids during the reflow process. Furthermore, the effect of solder melting on underfill voiding was examined as shown in Figure 3-8. Two micrographs of void formation study 2 compare TV 2-1 and TV 2-2 after the reflow process (see Figure 3-8). Test vehicle 2-1, consisting of a glass cover slide on the underfill deposited substrate without lead-tin solder, did not show any voids after the reflow process. A thermally activated volatile component such as a low molecular weight polymer component would tend to outgas once a critical temperature is reached. Voids should appear in test vehicle 2-1 after the reflow process in order to validate the hypothesis that some uncured volatile components outgass due to exposure of the components to high temperature above the volatile components' boiling point. Therefore, the result using TVs 2-1 indicated that the reflow process has a process window for any low-molecular weight components such that they fully participate in the underfill cure process and do not outgass.

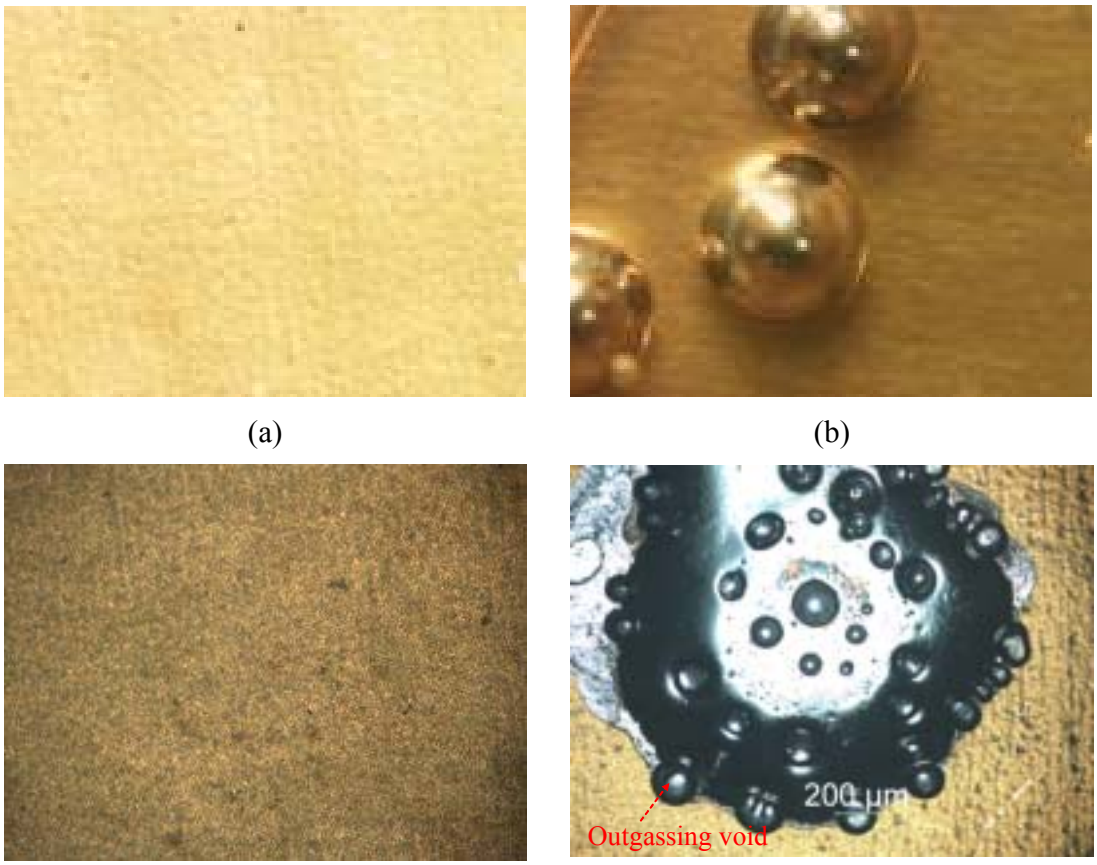
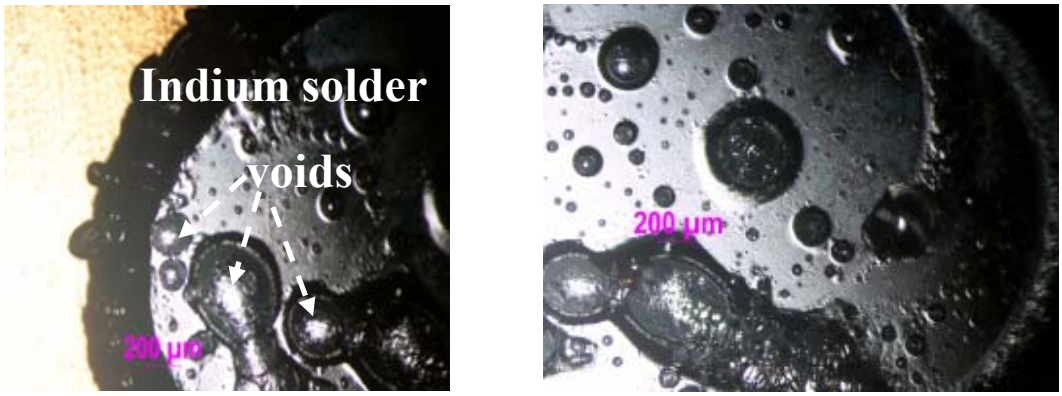


Figure 3-8 Micrographs of void formation study 2: (a) TV2-1 before heating, (b)TV2-2 before heating, (c)TV2-1 after heating at 225 °C, and (d)TV2-2 with tin-lead (Sn/Pb: 63/37) solders after heating at 225 °C

On the contrary, a significant amount of underfill voiding was detected around a merged Sn/Pb (63/37) solder sphere on the TVs 2-2, which had four small Sn/Pb (63/37) solders on the underfill deposited ENIG substrate. The size of the underfill voids around the solder spheres was observed to be on the average of 200 um. Thus, the potential existence of low-molecular weight volatile components within the no-flow underfill material is not the sole source for underfill voids. Solder ball reflow is required for voiding to occur. The reflow process of solder balls in the presents of the no-flow

underfill material is necessary for underfill voiding to occur near Sn/Pb (63/37) solder based on void formation study 2. That is, this void formation study indicated that the presence of voids was strongly dependent on the presence of solder within the no-flow underfill material during the reflow process. Similarly, a large number of voids around Indium solders was observed on TV2-3 reflowed at 180 °C as shown in Figure 3-9. Even though the TV2-3 was reflowed at significantly lower temperatures compared to the peak temperature used for the experiments using TV2-1 and TV2-2, a large number of voids were observed. Therefore, this observation indicated voids can be produced at low temperature in the case of solders wetting.



(a) (b)

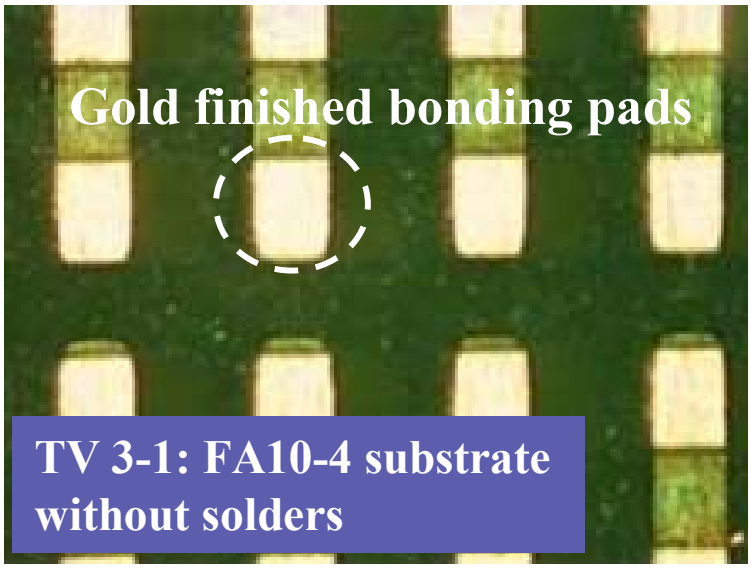
Figure 3-9 Micrographs of void formation study 2: (a) and (b) TV2-3 with pure indium (In/100) solders after heating 180 °C

3.3.3 Void Formation Study 3 (Effect of Chemical Reaction on Void)

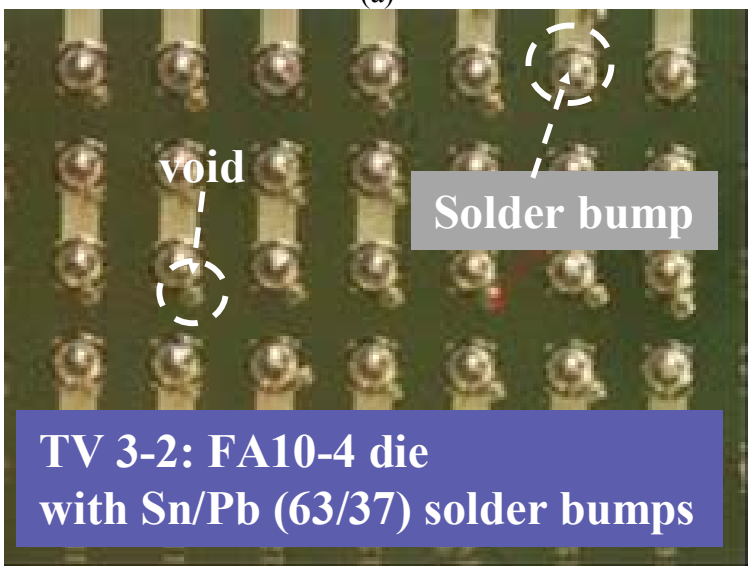
The test vehicles were assembled and the assembled parts were inspected via a microscope to confirm void-free assemblies in the TV prior to the reflow process. The assembled TVs were reflowed in a convection reflow oven using the controlled reflow process conditions specified in Table 3-5, selected based on yielding a robust interconnect for high lead solder bumps and an eutectic solder cap FCIP test vehicle system using no-flow underfill materials.

After the robust reflow process was completed, TV 3-1, which consists of a glass cover slide on the no-flow underfill deposited FA10-4 substrate, did not show any voids as shown in Figure 3-10-(a). However, the optical micrograph of TV 3-2, which consists of a glass cover slide on no-flow underfill, deposited FA10-4 die, showed voids around every eutectic Sn/Pb (63/37) solder bump as shown in Figure 3-10-(b).

Furthermore, a large number of voids on the TV 3-3 (FCIP substrate), which consists of a glass die and organic substrate with eutectic Sn/Pb (63/37) solders bonding pads, was observed as shown in Figure 3-11-(a). However, no voids were detected on the TV 3-4 (FCIP die), which consists of a glass cover slide on the high lead solder balls bumped FCIP die as shown in Figure 3-11-(b) after the reflow process.

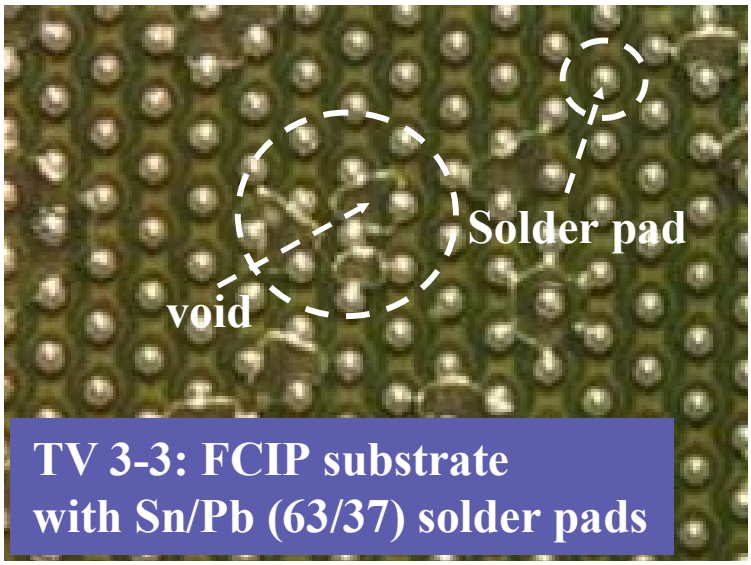


(a)

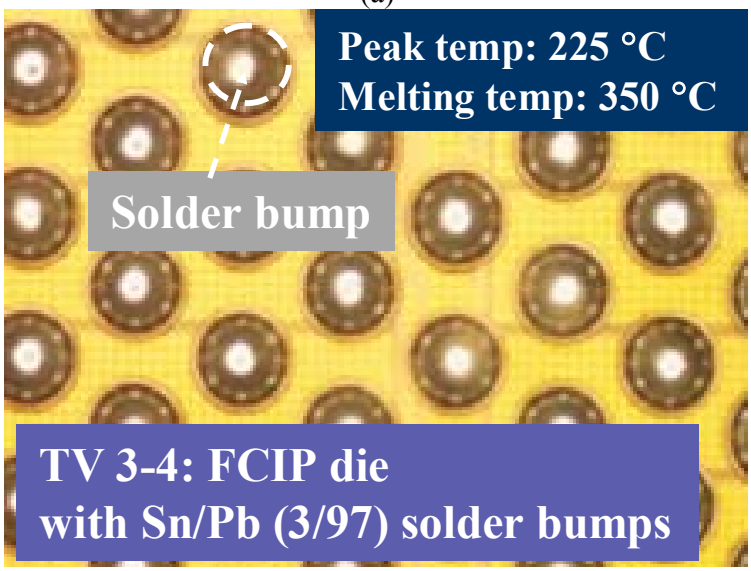


(b)

Figure 3-10 Micrographs of void formation study 3 using FA10 TVs:
(a) TV3-1 (FA10-4 substrate) and (b) TV3-2 (FA10-4 die)



(a)



(b)

Figure 3-11 Micrographs of void formation study 3 using FCIP TVs:
(a) TV3-3 (FCIP substrate) and (b) TV-3-4 (FCIP die)

The reflow process conditions were mainly designed for eutectic Sn/Pb (63/37) solder wetting for the interconnection of the high lead solder bumps (Sn/Pb-3/97) on eutectic caps (Sn/Pb-63/37). Therefore, the evidence of void formation study 3 demonstrates that the interaction of solder melting, no-flow underfill fluxing, and no-flow underfill curing has a strong effect on underfill voiding.

Indeed, solder melting is influenced by the flux agents in a no-flow underfill. The fluxing agent removes the oxide layer on both the surfaces of the solder bumps and the metal pads during the reflow process. Such fluxing capability mainly depends on the functionality and concentration of fluxing agents, and surface finished material properties. In general, carboxylic acid is one possible material used for organic acid based fluxing agents in no-flow underfills, as it simultaneously reacts with the solder oxide and with the epoxy ring during the underfill cure process as shown in Figure 3-12 [65].

Similarly, the organic acid-based fluxing agents in the no-flow underfill participate in underfill curing without eutectic solder melting. If solder is present during the no-flow underfill cure process, the fluxing agents simultaneously participate in the underfill curing process and the fluxing function near the eutectic solder balls. In other words, some amount of fluxing agents directly participate in underfill curing, and some portion of the fluxing agents, which remove oxidation around solders bumps, are restored to fluxing agents. Then the restored fluxing agents around solder bumps are exposed to temperatures above their boiling temperature due to solder melting endothermic reaction and are less likely to participate in the underfill curing process due to partially cured underfill material. The endothermic reaction results in heat energy concentration around the solder surface. The concentrated heat energy instantly transfers to the potential

nucleation sites causing underfill voiding during the reflow process using high reflow parameters for high yields with high I/O density, fine pitch flip chips.

3.4 SUGGESTED VOID FORMATION MECHANISM

The function of flux agents in the no-flow underfill is to remove the oxide layer on both the surfaces of the solder bump and the metal pad during the reflow process in which the fluxing capability mainly depends on the functionality, concentration of fluxing agents, and surface material properties. There are no oxides on the metal pad because all metal pads used in this study were coated with inert gold (Au) metal. So, the fluxing agents, basically organic acids, react with solder oxide and also partly with the epoxy ring during the underfill cure process as shown in Figure 3-12.

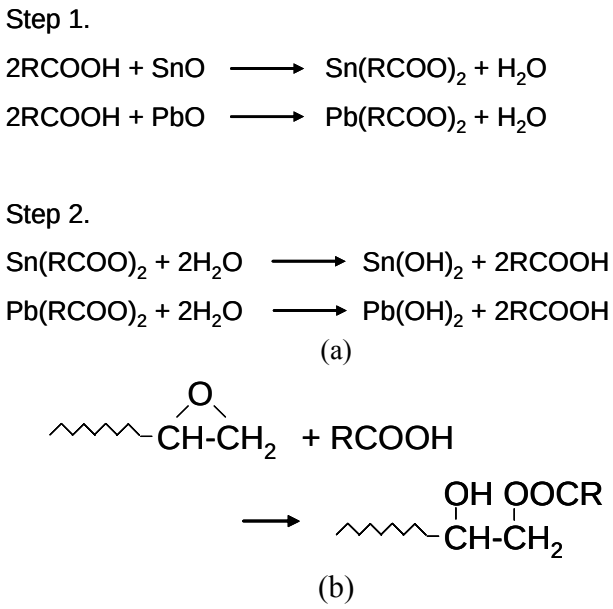


Figure 3-12 (a) Possible fluxing mechanism for organic acid-based fluxes and (b) its reaction with oxirane of epoxy resins [8]

Alcohol is also alternatively used for a fluxing agent as described in Figure 3-13. The figure shows a typical fluxing mechanism using ethanol (CH_3CH_2OH). The alcohol removes oxidation around solders. Then, the oxidation reduction reaction will produce acetic acid (CH_3COOH) and water (H_2O). The acetic acid is a typical carboxylic acid

used for organic acid fluxing mechanism. The resulting functional group similarly coincides with by-products such carboxylic acid (RCOOH) and water (H_2O) in the reaction as described in Figure 3-12.

$$CH_3CH_2OH + 2SnO \longrightarrow CH_3COOH + H_20$$
$$CH_3CH_2OH + 2PbO \longrightarrow CH_3COOH + H_20$$

Figure 3-13 Possible fluxing mechanism for ethanol-based fluxes

In general, the selection of fluxing agent depends on the application of the no-flow underfill. –COOH (acid base) group is more reactive than –OH (alcohol). Hence, no-flow underfills including an acid base fluxing agent will react and cure faster than materials including an alcohol base fluxing agent. Regardless of the base materials, similar chemical components will be created. These materials are carboxylic acid (RCOOH) and water (H_2O).

Therefore, the fluxing agents in the no-flow underfill material near the eutectic solder balls could participate in the fluxing mechanism and have little chance to react with the underfill cure process resulting in fluxing agent trapped inside the underfill during the reflow process. These fluxing agents trapped in the partly cured underfill near the solder balls, could coalescence and evaporate under high temperature, finally resulting in voids.

This chapter has presented research that identifies the plausible causes of underfill void formation in the flip chip assembly via structured experimentation. The results from these experimental void formation studies have shown that a chemical reaction between the solder interconnection system and no-flow underfill during solder reflow process was a main cause of void formation in FCIP. The process parameters such as the effect of

pretreatment on the substrate, placement force, and dwell time, have shown little contribution to void formation.

The findings in this study provide the fundamental understanding of void formation in the underfill after high I/O, fine pitch flip chip assembly using solder and no-flow underfill materials and can be attributed to the establishment of design a guideline for the development of advanced no-flow underfill materials systems and the novel FCIP assembly process for high reliability with minimized voids formation.

3.5 DISCUSSION AND CONCLUSIONS

The possible causes of void formation were reviewed to explain the high number of underfill voids. They can be classified into thermal effect induced voids and non-thermal induced voids. Regarding non-thermal induced voids, the void formation study 1 found the effect of non-thermal characteristics does not have a major effect on voids relative to the total quantity of voids. Therefore, the non-thermal induced voids could not explain the current large number of voids in flip chip package using no-flow underfills. On the contrary, void formation study 2 and 3 found chemically activated fluxing mechanism removing oxidation around solders to make better wetting conditions while causing underfill voiding. Besides, void formation mechanism induced by the chemical reaction was developed in order to explain current the large number of voids in the no-flow assembly process for flip chip in the package [8, 58].

The wetting process of eutectic solders might evolve a high concentration of gases forming voids in the flip chip package. The wetting eutectic solder interacted with no-flow underfill curing affecting underfill voiding as suggested in this chapter using void formation studies [8]. It is suggested that studies found the oxidation removal for the solder wetting delayed the fluxing agents' restoration to participate in underfill curing in step 1 as described in Figure 3-14. Hence, the material was exposed to temperatures above its boiling temperature in step 2 as described in Figure 3-14. Therefore, the chemical reactions increased volatile components during underfill curing and solder wetting. Similarly, the organic acid-based fluxing agents in the no-flow underfill participate in underfill curing without solder melting. If solder is present during the no-

flow underfill curing process, the fluxing agents simultaneously participate in the underfill curing process and the fluxing function near the eutectic solder balls.

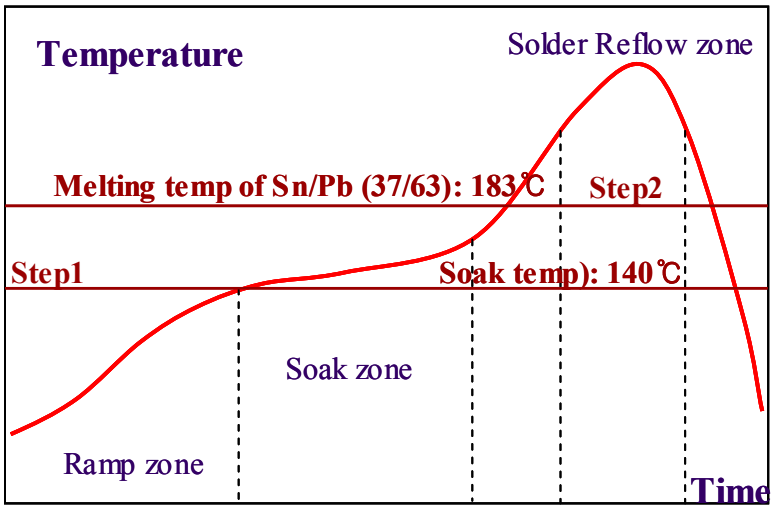


Figure 3-14 Typical reflow profile of no-flow underfills

In other words, some amount of fluxing agents directly participate in underfill curing, and some portion of the fluxing agents, which remove oxidation around solders bumps, are restored to fluxing agents. Then the restored fluxing agents around solder bumps are exposed to temperatures above their boiling temperature due to solder melting endothermic reaction and are less likely to participate in the underfill curing process due to partially cured underfill material. The endothermic reaction results in thermal energy concentration around the solder surface. The concentrated thermal energy instantly transfers excessive energy to the potential nucleation sites causing underfill voiding during the reflow process using high reflow parameters for high yields with high I/O density, fine pitch flip chips.

Therefore, the underfill voiding amount can be reduced by providing the fluxing agent for oxidation removal and underfill curing with stable temperature conditions. From a manufacturing standpoint, a stable temperature enables a robust interconnection between a die and a substrate without producing underfill voiding. In addition, the source of void formation will be investigated to validate the suggested void formation mechanism in Chapter 4. Experimental techniques will be used to determine the process conditions enabling the robust interconnection without underfill voiding in Chapter 5.

CHAPTER 4

VALIDATION OF VOID FORMATION MECHANISM

4.1 INTRODUCTION

From the result of Chapter 3, the underfill voiding potentially can be induced by the thermal effect of the reflow process with high I/O density and fine pitch flip chip. The assembly process causes some of low weight molecular components, such as the fluxing agent, to become volatile with expose to temperatures above its boiling temperature as explained in the previous Chapter. This mechanism of chemical reaction and thermal effect induced voids won't activate without the solder wetting process. The volatile components become the source of the massive amount of underfill voiding, thereby preventing high reliability.

For the validation of the above described mechanism of underfill voiding, this study investigates the effect of solder wetting on chemical reaction causing underfill voiding. Thus, the identification could validate the mechanism of voiding described in Chapters 3 and 4.

Therefore, this study investigated the void formation mechanism induced by chemical interaction between eutectic solder (Sn63/Pb37) wetting and no-flow underfill material curing during flip chip in package assembly. During the process, low weight molecular components, such as fluxing agents and water molecules, can induce voids with the chemical interaction between solder wetting and underfill curing when these components are heated to melt and cure respectively. The low weight molecular components become volatile with exposure to temperatures above their boiling points; this was found to be the

main source of the extensive underfill voiding. This mechanism of chemically and thermally induced voids was explained using Differential Scanning Calorimetry (DSC) thermo-gram comparison and Gas Chromatography and Mass Spectrum (GC-MS) chemical composition identification on the suggested chemical reaction formula. The technique is widely used in the analysis and identification of unknown chemical components [31-33].

Consequently, this finding can validate the mechanism that drives no-flow underfill voiding as well as enhance understanding of void formation. Furthermore, these understandings enable the development of a void-free flip chip assembly process using no-flow underfill material (Table 3-1 Material property of a commercial no-flow underfill) for cost effective and high performance electronics packaging applications.

4.2 EXPERIMENTAL APPROACH

4.2.1 Investigation of Solder Wetting and Underfill Curing Using a Differential Scanning Calorimetry

The effect of solder wetting on underfill curing was investigated using a DSC instrument (by TA Instruments, Model 2920) [66, 67]. The thermo-analytical technique measures the amount of heat required to increase the temperature of a sample. Thus, the process can be determined as exothermic or endothermic by using this technique.

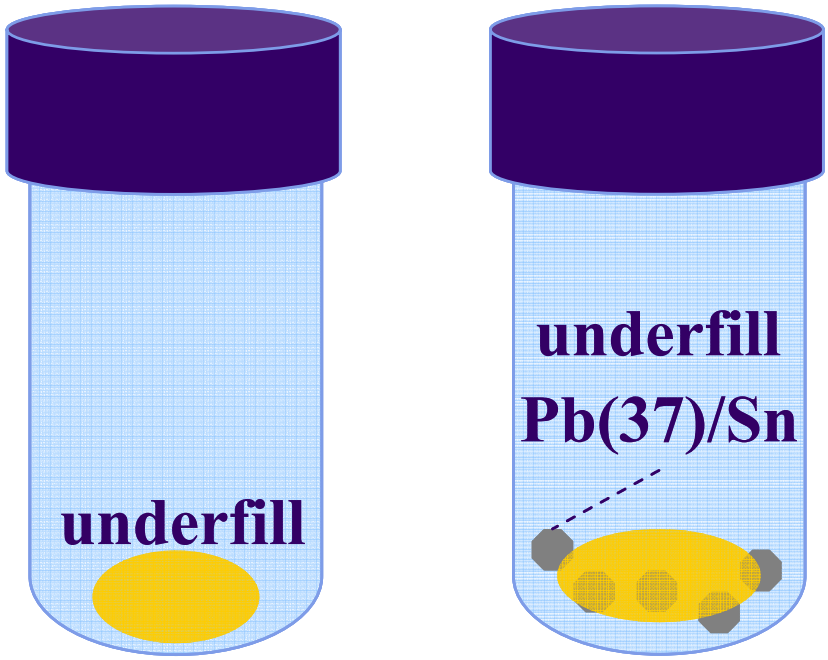
Based on the suggested mechanism of underfill voiding, voids were induced by the chemical and endothermic thermal reactions between solder wetting and underfill curing. Typically, underfill curing and solder wetting present an exothermic reaction and an endothermic reaction respectively. The DSC measured the amount of heat flow in the samples A (No-flow underfill without eutectic Sn/Pb (63/37) solder balls and sample B (No-flow underfill with eutectic Sn/Pb (63/37) solder balls). Sample A was prepared with 10 mg no-flow underfill. Sample B was prepared with 10 mg underfill and 2mg Sn/Pb (63/37) solders. Both samples had been warmed to room temperature from -40°C, and were placed into a hermetic DSC sample pan. For the thermal effect investigation, the samples were heated in DSC cell at a specified heating rate (30°C/min.) to 250°C to obtain thermodiagrams.

4.2.2 Identification of Evolved Gas Using a Gas Chromatography and Mass Spectrometry Study

The fluxing agent was suggested as the source of underfill voiding in the previous Chapter. The large number of voids was produced by the chemical reaction with thermal effect from the reflow process because solder wetting delayed some of the flux agent to restore and participate in underfill curing. Consequently, the flux agents become volatile components causing outgassing voids. Hence, two test vehicles were prepared to investigate the effect of Sn/Pb (63/37) wetting on the underfill voiding and the source of underfill voiding using an experimental technique. Figure 4-1 illustrated test vehicle 1 (TV 1: Without Sn/Pb-63/37) and test vehicle 2 (TV 2: With Sn/Pb-63/37). Both TVs were used to investigate evolved gases caused by the effect of Sn/Pb (63/37) wetting affecting underfill voiding using a Gas Chromatography and Mass Spectrometry (GC-MS: Agilent Technology 6890N) with two replicates. The GC-MS is composed of two major components: the gas chromatography and the mass spectrometry. GC will separate the different chemical molecules in a mixture as the sample travels the column. The molecules take different amounts of time (called the retention time) to come out of the gas chromatography, and this allows the mass spectrometer downstream to capture, ionize, accelerate, deflect, and detect the ionized molecules separately. The mass spectrometer does this by breaking each molecule into ionized fragments and detecting these fragments using their mass to charge ratio. Thus, the mass spectrometry detects multiple molecules [68].

Next, 20 mg of commercial no-flow underfill was put into two vials as illustrated in Figure 4-1 to eliminate the effect of amount of underfill on the voiding. Then, vial TV 1

was closed with a rubber stopper and a metal cap. In similar, the vial in Figure 4-1-(b) was prepared with 5 mg eutectic solders and 20 mg underfill for TV2. Afterwards, both prepared vials were exposed to 250 °C for 5 minutes, which are similar to solder wetting process and enables to evolve a plenty amount of gases from the samples. Eventually, evolved gases in vials were extracted [69] using a solid-phase micro-extraction (SPME) technique. Approximately 1cm of a fiber needle was dipped into the two vials for five minutes so that the fiber could absorb any evolved gases. The fiber was plugged into the injector of GS-MS to identify any gases evolved from reflow process.



(a) (b)

Figure 4-1 (a) test vehicle 1: no-flow underfill in vial and (b) test vehicle 2: no-flow underfill and lead-tin (Sn/Pb: 63/37) solders

4.3 EXPERIMENTAL RESULTS

4.3.1 Mechanism of Solder Wetting and Underfill Curing Using a Differential Scanning Calorimetry

A noticeable exothermic reaction was initiated in step 2 at around 115 °C for Samples A and B as shown in Figure 4-2 because epoxy based underfills cure via thermally initiated chemical reactions by linking to another polymer chains. Cross-linking typically is exothermic reaction [70, 71]. The temperature corresponds to the step 2 in the suggested possible fluxing mechanism of no-flow underfill process (see Figure 3-12). With Sn/Pb (63/37) solder wetting, the endothermic reaction was observed in only Sample B at around 183 °C, which is the melting temperature of Sn/Pb (63/37). The heat energy was absorbed by the solder surface and the absorbed heat energy was concentrated on the surface of solder to wet during reflow process. If solder is present during the no-flow underfill cure process, the concentrated heat instantly might be transferred to the potential nucleation sites causing underfill voiding during the reflow process using high reflow parameters for high yields with high I/O density, fine pitch flip chips. For that reason, voids were observed on TV-2 without eutectic solder and no-flow underfill in the void formation study.

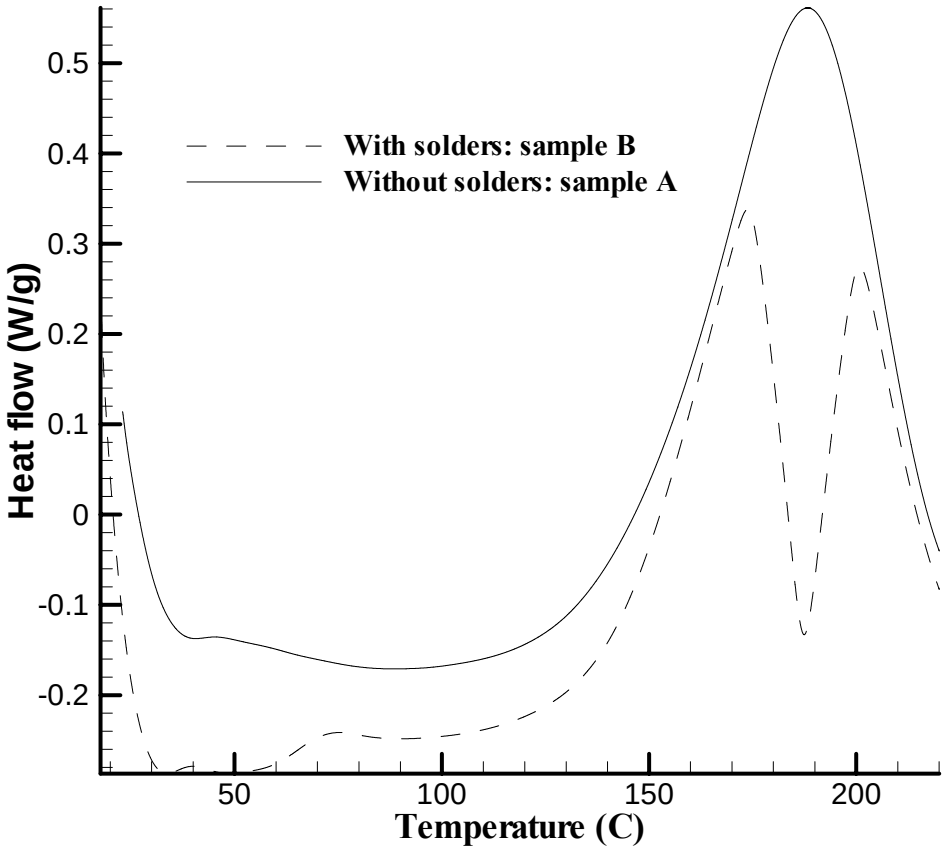


Figure 4-2 DSC measured heat flow diagrams of and sample A (Without solders) and sample B (With solders)

4.3.2 Gases Evolved From Solder Wetting and No-Flow Underfill Curing Using a Gas Chromatography and Mass Spectrum Study

The analysis using a GC-MS found a significant difference between TV 1 and TV 2. TV 2 (the no-flow underfill with Sn/Pb (63/37) solders) had higher gas intensity than TV 1 (the no-flow underfill without Sn/Pb solders) as shown in Figure 4-3.

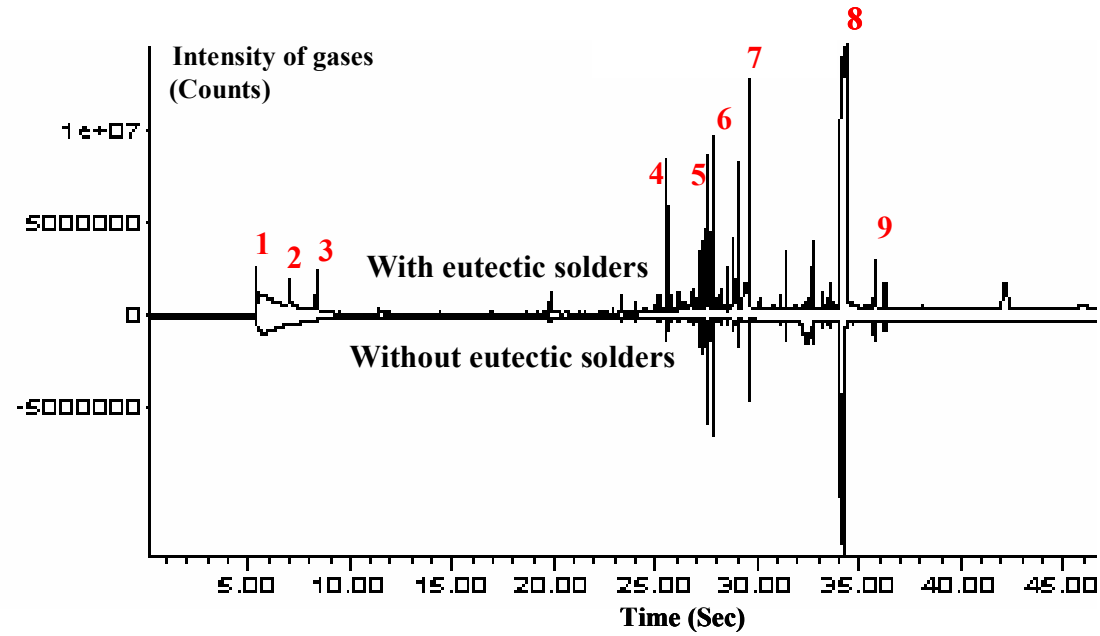


Figure 4-3 Spectrums of evolved gases in underfill reflow process of with eutectic solders and without eutectic solders using GC-MS

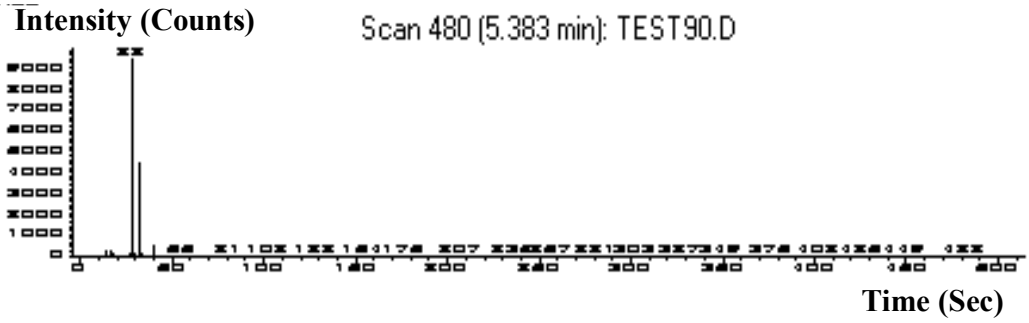
In the figure, the area of the peak is associated with the amount of gases evolved during the reflow process, meaning that the high peak implies high intensity of evolved gases. The intensity difference is shown in the spectrum of Figure 4-3. In the Figure 4-3, where the upper section presents the case of TV 2 with the effect of solder wetting and the lower section presents the case of TV 1. The observed gases with high intensity can be considered as the potential source of the no-flow underfill voiding in no-flow assembly

process. Therefore, the potential source of underfill voiding could be dihydrofuran (1), water vaporization (2), acetic acid (1st trial)/carbamic acid (2nd trial) evaporation (3), benzene (4), hexadecane (5), and cyclohexene (8), which are chemical components identified with high percent of matching (90%≥) to the GC-MS library. However, dihydrofuran and hexadecane could be neglected as the source of voiding due to low boiling point and high boiling point respectively. Benzene (4), hexadecane (5), and cyclohexene (8) were evolved from both samples regardless of solder wetting. Consequently, these gases might be produced by hidden chemical reactions, which might not be the dominant factor of underfill voiding in an actual assembly process. Indeed, the applied process condition for this study has 250 °C peak temperature and 5 minutes reflow time. The process conditions are relatively higher than typical assembly conditions (225 °C peak temperature and 1 minutes reflow time). Therefore, high peak temperature with longer reflow time might induce the heavy molecular weight components.

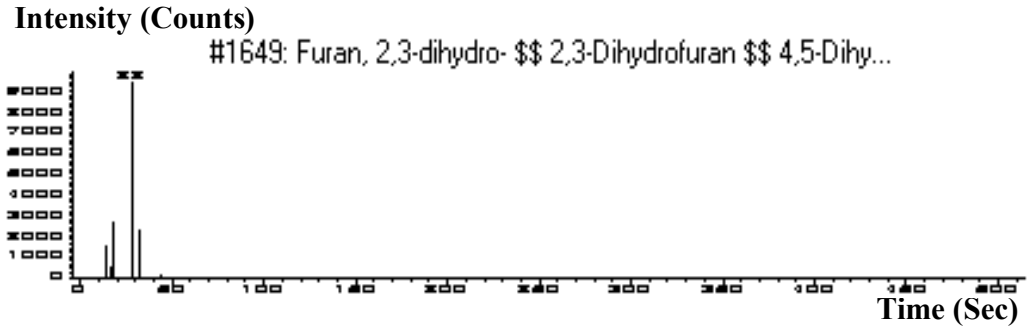
From the comparative study, another noticeable result was the identification of water vapor (1) and carboxylic acid vapor (2) in only TV 2 with Sn/Pb solders wetting as the mechanism of underfill voiding. The evolved acid has –COOH which is a common chemical component of carboxylic acid in both trials. Actually, both carboxylic acids have similar molecular weights as described in Table 4-3.

This gas identification validated the mechanism of chemically induced voids presented in Chapter 3. Indeed, the flux agents of no-flow underfill remove the oxide layer on both the surfaces of the solder bumps and the metal pads during the reflow process. In general, carboxylic acid is used for organic acid based fluxing agents in no-flow underfills, as it simultaneously reacts with the solder oxide and with the epoxy ring during the underfill

cure process as shown in Figure 3-12 [65]. Step 1 and step 2 of Figure 3-12 produced water and carboxylic acid, respectively, which might be the source of underfill voiding. Similarly, the organic acid-based fluxing agents in the no-flow underfill participate in underfill curing without eutectic solder melting. If solder is present during the no-flow underfill cure process, the fluxing agents simultaneously participate in the underfill curing process and the fluxing function near the eutectic solder balls. In other words, some amount of fluxing agents directly participate in underfill curing, and some portion of the fluxing agents, which remove oxidation around solders bumps, are restored to fluxing agents. Then the restored fluxing agents around solder bumps are exposed to temperatures above its boiling temperature due to solder melting endothermic reaction and are less likely to participate in the underfill curing process due to partially cured underfill material. The endothermic reaction results in heat energy concentration around the solder surface. The concentrated heat energy instantly transfers to the potential nucleation sites causing underfill voiding during the reflow process using high reflow parameters for high yields with high I/O density, fine pitch flip chips. Therefore, water gas and carboxylic acid gas were observed in TV 2 with solder wetting in the contrast of TV 1.



(a)

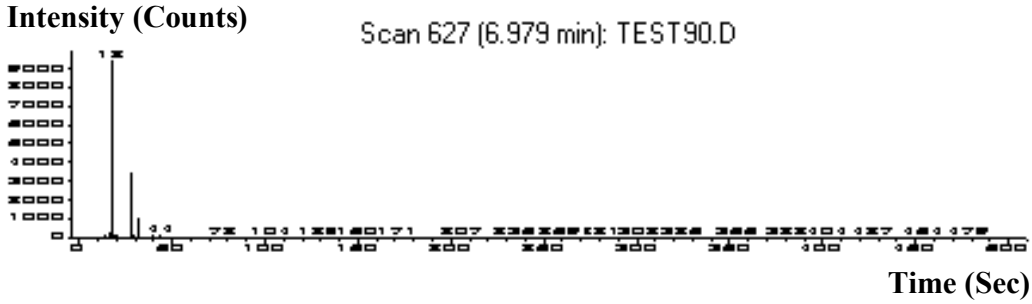


(b)

Figure 4-4 Identification of gas 1: (a) scanned spectrum of evolved gas 1 and (b) spectrum of GC-MS library

Table 4-1 Material property of dihydrofuran

CAS No.	1191-99-7
Formula	C_4H_6O
Molecular weight	70.09 g/mol
Boiling point	54°C



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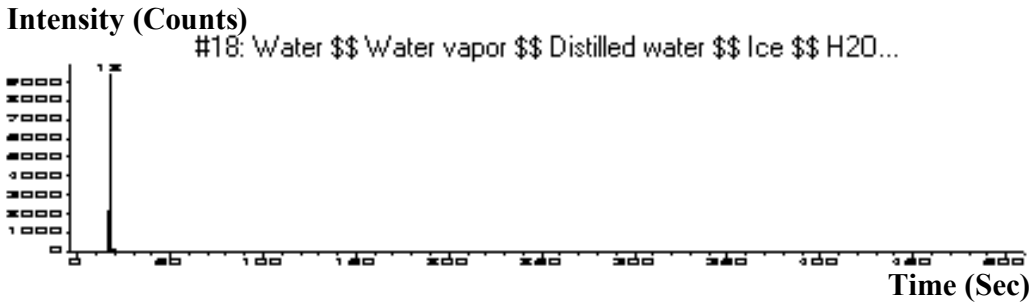
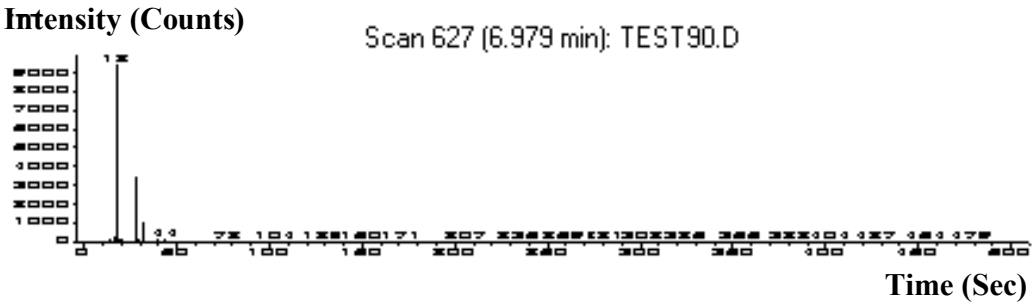


(b)

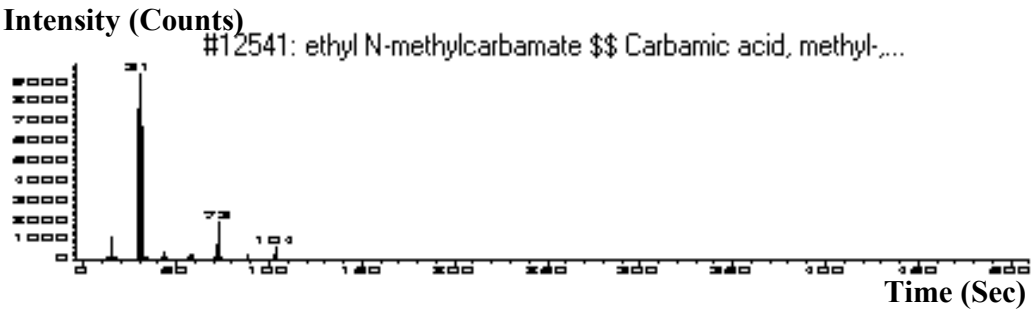
Figure 4-5 Identification of gas 2: (a) scanned spectrum of evolved gas 2 and (b) spectrum of GC-MS library

Table 4-2 Material property of water

CAS No.	7732-18-5
Formula	H_2O
Molecular weight	18.01g/mol
Boiling point	99°C



(a)

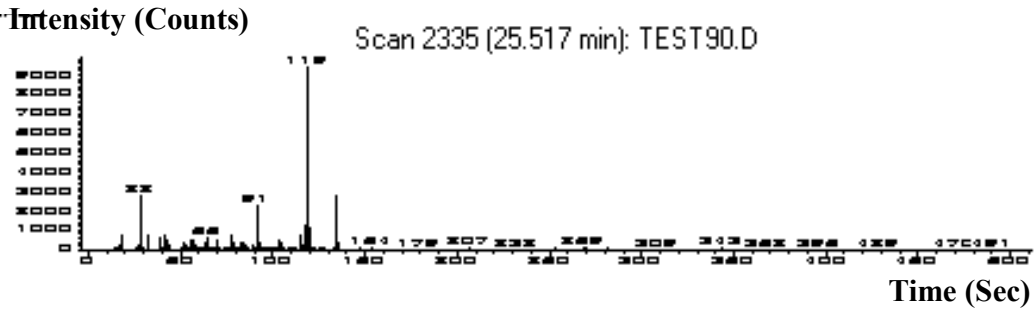


(b)

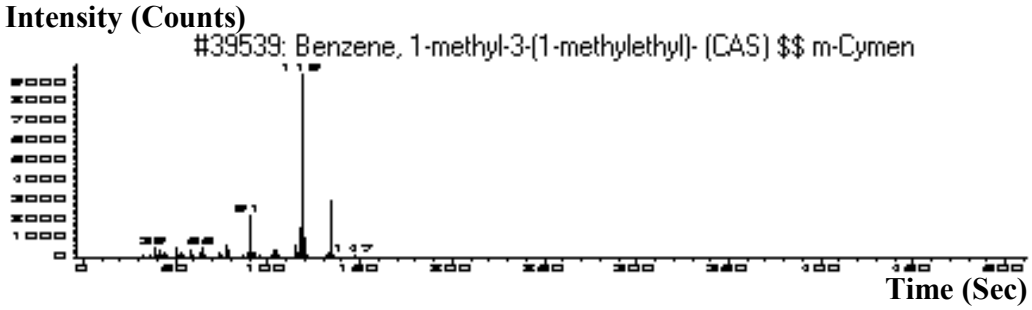
Figure 4-6 Identification of gas 3: (a) scanned spectrum of evolved gas 3 and (b) spectrum of GC-MS library

Table 4-3 Material property of acetic / carbamic acid

CAS No.	64-19-7 (Acetic acid)	463-77-4 (Carbamic acid)
Formula	CH_3COOH	NH_2COOH
Molecular weight	60.05 g/mol	61.04 g/mol
Boiling point	118 °C	120 °C



(a)

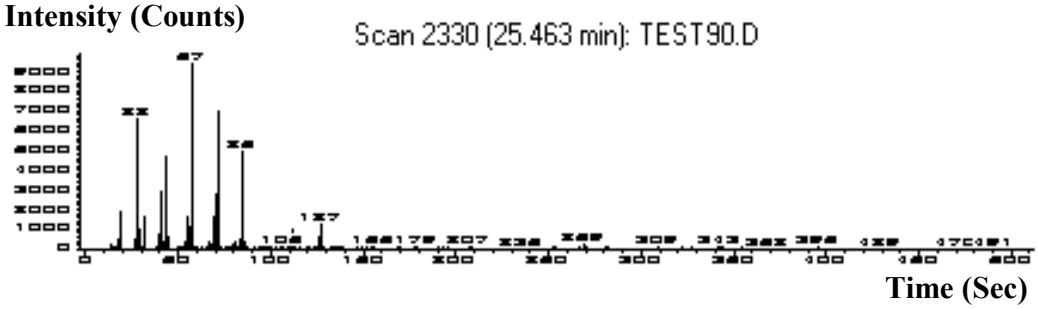


(b)

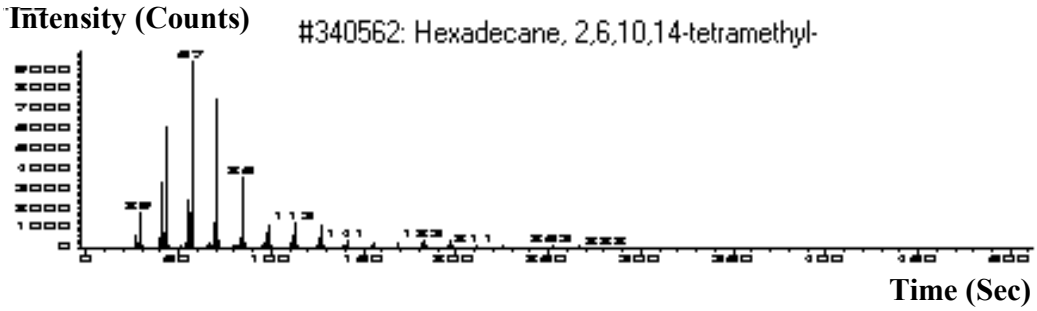
Figure 4-7 Identification of gas 4: (a) scanned spectrum of evolved gas 4 and (b) spectrum of GC-MS library

Table 4-4 Material property of benzene

CAS No.	71-43-2
Formula	C_6H_6
Molecular weight	78.11 g/mol
Boiling point	80°C



(a)

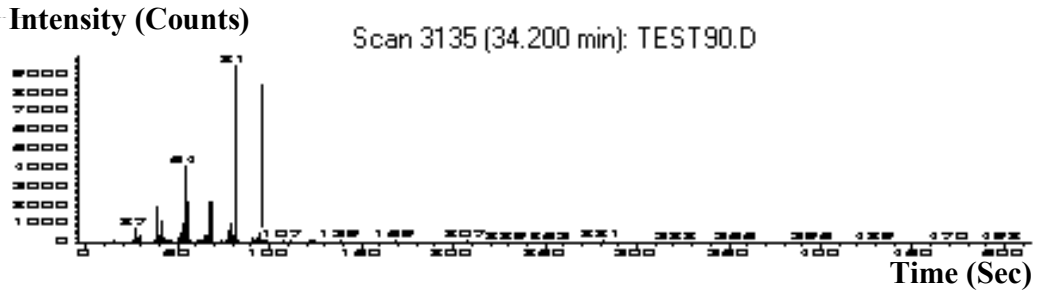


(b)

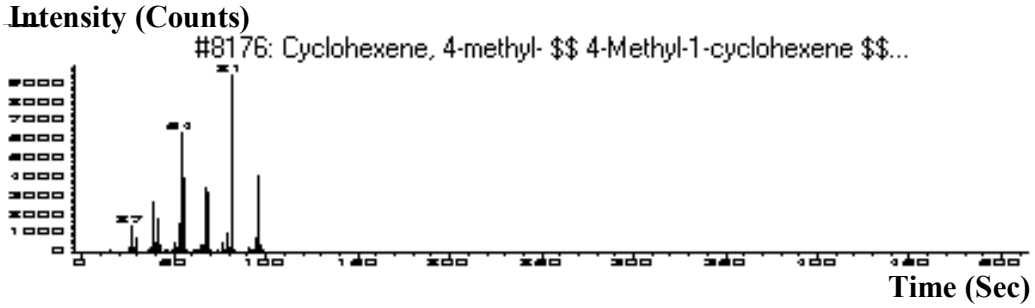
Figure 4-8 Identification of gas 5: (a) scanned spectrum of evolved gas 5 and (b) spectrum of GC-MS library

Table 4-5 Material property of hexadecane

CAS No.	544-76-3
Formula	$C_{16}H_{34}$
Molecular weight	226.44 g/mol
Boiling point	287 °C



(a)



(b)

Figure 4-9 Identification of gas 8: (a) scanned spectrum of evolved gas 8 and (b) spectrum of GC-MS library

Table 4-6 Material property of cyclohexene

CAS No.	110-82-7
Formula	C_6H_{12}
Molecular weight	84.16 g/mol
Boiling point	80°C

4.4 DISCUSSION AND CONCLUSIONS

This work validated the mechanism of thermally induced void formation which causes a large number of voids in the flip chip package. The DSC identified the thermodiagram during reflow process by measuring heat flow. The heat flow with solder wetting has an endothermic reaction as shown in Figure 4-2. The reaction corresponds to step 2 in . At that step, the endothermic reaction resulted in a concentrated heat flow on the surface of the solder. The concentrated thermal energy activated the potential nucleation sites, which were induced by the thermal and chemical reaction during reflow process. Besides, the GC-MS identified the interaction of solder wetting on underfill curing by identifying the chemical composition and measuring the intensity of evolved gases. The dominant gasses indentified were water vapor and carboxylic acid vapor, which were only detected with Sn/Pb (63/37) solder wetting and underfill curing. Therefore, the by-product of fluxing mechanism, water, was proved to be the source of voids (see the step 1 of Figure 3-12). In addition, carboxylic acid became volatile due to solder wetting and induced a large number of voids in the packages (see the step 2 of Figure 3-12).

The accomplishments in this study contribute to a fundamental understanding of void formation in the no-flow underfill. Furthermore, these finding could establish design guidelines for the development of advanced no-flow underfill materials systems and for the development of high I/O, fine pitch flip chip assembly process for high yield and long-term thermo-mechanical reliability. Indeed, this investigation of void sources and the understanding of the void formation mechanism are important steps to reduce the number of voids by modifying reflow parameters to provide stable conditions, enabling

the flux agent to remove oxidation from the solder surface and stably participate in underfill curing. Eventually, no-flow underfill can achieve a void-free assembly with high I/O, fine pitch devices. Therefore, the next chapter investigated the effect of reflow parameters on underfill voiding and solder interconnects using a systematic experimental approach with commercial no-flow underfill (Table 3-1 Material property of a commercial no-flow underfill).

CHAPTER 5

PROCESS AND MATERIAL CHARACTERIZATION FOR THE MIINMAZATION OF UNDERFILL VOIDING

5.1 INTRODUCTION

A series of systematic void formation studies was conducted using simple structured test vehicles to investigate the plausible causes of underfill voiding, as shown in the Chapter 3. In addition, Chapter 3 found the underfill voids were induced by a chemical reaction in solder wetting process. Without the solder wetting process, the underfill voids were not nucleated. On the studies, a fluxing agent of no-flow underfill was suspected as a potential source of voids. Then, Chapter 4 validated, using GC-MS, that primary source of underfill voiding was the fluxing agent of no-flow underfill in solder wetting process. The fluxing agent was activated during soak zone and some of the components are exposed to its boiling temperature in the current high yield process [3]. The assembly process uses a soak temperature in the range of between 140ºC and 170ºC for conventional packaging. The conventional reflow profile is illustrated in Figure 3-14. Instead of a typical soak temperature, a low soak temperature range (120 ~ 130ºC) was selected to activate the fluxing agent in stable temperature range, preventing underfill voiding. On the low soak temperature range, parametric experimental studies were designed to investigate the effect of potential parameters on voiding to achieve a void-free assembly process. First, void formation characterization 1 investigated the effect of soak temperature and soak time on voiding to validate the void formation mechanism suggested in chapter 3 and chapter 4. Then, void reduction study 1 determined soak zone

conditions for high assembly yield and minimum number of voids. Void formation characterization 2 investigated the effect of peak temperature on underfill voiding. Next, void reduction study 2 determined the peak temperature enabling robust interconnection without producing underfill voiding. Finally, the large scale of assembly run validated the stability of a high, stable yield and void-free assembly process with 30 assemblies of a high I/O, fine-pitch flip.

In addition, this chapter characterized no-flow underfill to minimize underfill voiding using nano-size particles. In the presence of particles, the underfill voiding depends on heterogeneous nucleation since a void was nucleated the interface of two homogenous materials such as a solder and an underfill. The nucleated void needs excessive energy above required energy at critical point for a macro-size void growth. Otherwise, the unstable void will disappear due to insufficient energy. In the flip chip assembly process, a reflow process can be the energy source for a void nucleation and growth. The void nucleation is governed as the following heterogeneous bubble nucleation theory

$$N_{het} = Cf \exp\left(\frac{-\Delta G^*_{het}}{kT}\right)$$

where $\Delta G^*_{het} = \frac{16\pi\gamma_{LG}{}^3}{3\Delta P^2} S(\theta)$, C is concentration of available heterogeneous nucleation sites, f is frequency factor of gas molecules, T is temperature, and k is Boltzmann's constant. If the available heterogeneous nucleation, C, is significantly increased by creating more heterogeneous nucleation sites, the nucleation sites distributes the fixed amount of gas available induced by a chemical reaction during solder reflow process over the large number of nucleation sites. The resulting gas distribution diminishes a gas available per void nucleated. Without the necessary gas supply, the voids nucleated

cannot grow to the critical radius size. Alternatively, void nucleation sites might influence free energy required at critical point, ΔG^*_{het}. The energy typically concentrated on solders to melt and wet during assembly process. The concentrated energy was distributed by adding potential nano nucleation sites into commercial underfill material. The potential nucleation sites can abate the excessive energy below required energy for a void nucleation, typically concentrated on the molten solders. Thus, the excessive thermal energy will be distributed on additional nano nucleation sites. The absorbed energy by nano particles decreases energy concentration below the required energy of stable conditions for a void nucleation and growth by distributing the energy to each nano nucleation sites. Consequently, the nucleated void will be unstable and disappear. On this heterogeneous nucleation theory, these studies investigated the feasibility of minimizing the amount of underfill voiding by characterizing material formulation using nano particles.

5.2 PROCESS CHARTERIZATION EXPERIMENTAL APPROACH

On the studies in previous Chapters, four experiments were designed to investigate the effect of reflow process parameters on voiding and to achieve the high, stable yield and void-free assembly process with FCIP using a commercial no-flow underfill (see Table 3-1) and simple structure test vehicles. Table 5-1 describes the specification of test vehicles used for this chapter.

Table 5-1 Summary of test vehicles configuration used in the void formation characterization and void reduction studies

Experiment	Category	
Void formation characterization 1 (The effect of soak zone on voids)	Die material	Glass cover
	Substrate material	37Pb-63Sn
	Chip size(mm)	< 10 x 10
	Bump count	3000 >
	Bump pitch	< 200μm
	Bump layout	Full area
Void formation characterization 2 (The effect of peak temperature on voids)	Die material	Glass cover
	Substrate size(cm)	1x1
	Substrate material	ENIG
	Bond pad	37Pb-63Sn
Void reduction study 1 (The effect of soak temperature and soak time on voids) Void reduction study 2 (The effect of peak temp on voids) Large scale assembly	Die material	Silicon
	Bump material	97Pb-3Sn
	Chip size(mm)	< 10 x 10
	Bump count	3000 >
	Bump pitch	< 200μm
	Bump layout	Full area

5.2.1 Void Formation Characterization 1 (Effect of Soak Temperature and Soak Time on Voids)

The most significant effect on no-flow underfill voiding was reported as the chemical reaction between solder melting and underfill curing, which affects a large number of voids in the FCIP [8, 52]. The chemical reaction is mainly induced by the fluxing agents reaction in no-flow underfill processing. The flux material will remove oxidation around solder bumps or pads, and reduce surface tension of molten solder causing good wetting condition. The conditions conventionally used are from 140 to 170 °C, which is the soak temperature as shown in Figure 3-14 [16, 17, 24, 72, 73]. This activation temperature enables the fluxing agent of no-flow underfill to function during the assembly process. Thus, the conventional range from 140 to 170 °C was chosen for the soak temperature in the high yield assembly process with high I/O, fine pitch FCIP using a commercial no-flow underfill. The commercial no-flow underfill typically uses carboxylic acid for a fluxing agent. Carboxylic acid boils at around 130 °C. As a result, the fluxing agent is exposed to temperatures above its boiling point during assembly, causing out-gassing and voids. Similarly, the current soak temperature of the high yield assembly process might be higher than fluxing agent's boiling temperature in the commercial no-flow underfill [8]. Therefore, a test vehicle, illustrated in Figure 5-1 and described in Table 5-1, was used to investigate the effect of soak temperature on underfill voiding using a commercial no-flow underfill on the reflow process conditions described in Table 5-2.

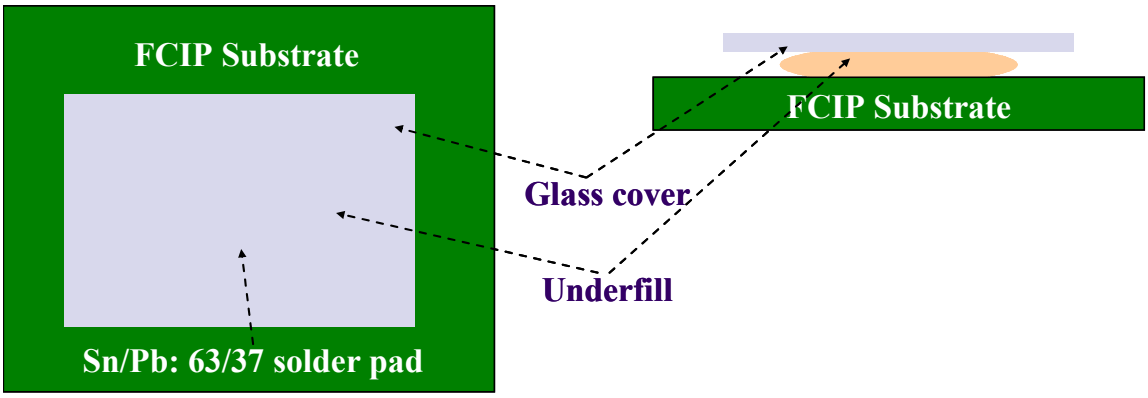


Figure 5-1 Schematic of test vehicle used for void formation characterization 1

Two different temperature ranges were considered in this study. The experimental study tested ranges from 140 to 170 °C (see Appendix A) and from 120 to 130 °C (see Table 5-2). The former was used for the high yield assembly process and the latter was selected for alternative condition for a void-free process. The lower soak temperature range can cause the fluxing agent to remove oxidation and to participate in underfill curing below its boiling temperature.

Table 5-2 Reflow process conditions used for void formation characterization 1

	Ramp rate	Soak temp	Soak time	Time above liquidus	Peak temp
Condition (1)	1.3°C/s	140 ~ 170 °C	90 sec	70 sec	225 °C
Condition (2)	1.3°C/s	120 ~ 130 °C	90 sec	70 sec	225°C

The pre-baking and pre-treatment used in the experiments are given in Appendix A and were applied to void formation characterization 1 [4, 5, 58-60]. Next, underfill was

dispensed on the FCIP substrate and a glass slide cover was placed on the underfill deposited substrate. A glass slide cover allowed visually investigating voiding pattern right after a reflow process without extra treatments. Then assembled test vehicles were reflowed at both the high yield assembly process with 140 through 170 °C and 120 through 130 °C. Finally, the underfill voiding was inspected using a visual microscope.

5.2.2 Void Reduction Study 1 (Effect of Soak Temperature and Soak Time on Voids)

The objective of void reduction study 1 was to validate the result of void characterization using commercial high I/O, fine pitch FCIP packages (see Table 5-1). In addition, this study optimized reflow process parameters to minimize the amount of underfill voiding by modifying soak temperature and soak time as described in Table 5-3. The pre-treatments used in previous studies were applied to the void reduction study 1. Next, underfill was dispensed on the FCIP substrate and a silicon die was placed on the underfill deposited substrate. Then assembled test vehicles were reflowed at four different assembly process conditions as shown in Table 5-3. Afterwards, each sample was scanned using a Scanning Acoustic Microscopy (C-SAM). The amount of underfill voiding was defined as the void percent area. It presented the total void area of total flip chip device area.

Table 5-3 Reflow conditions for void reduction study 1

Condition	(1)	(2)	(3)	(4)
Ramp rate	1.3°C/s	1.3°C/s	1.3°C/s	1.3°C/s
Soak temp	140~170 °C	120~130 °C	120~130 °C	120~130 °C
Soak time	50 sec	90 sec	120 sec	150 sec
Time above liquidus	70 sec	70 sec	70 sec	70 sec
Peak temp	225 °C	225 °C	225 °C	225 °C

5.2.3 Void Formation Characterization 2 (Effect of Peak Temperature on Voids)

The main objective of void formation characterization 2 was to investigate the effects of peak temperature and reflow time on underfill voiding and solder wetting. Prior to the assembly process, all moisture was driven out of the boards by exposure to an isothermal environment of 125 ºC for 3 hours. This bake-out time was determined from a previous bake-out experiment and was sufficient to avoid moisture out-gassing of the boards [61], [62]. Next, no-flow underfill was dispensed on the test vehicle and a cover glass was put on the underfill deposited test vehicle as illustrated in Figure 5-2. Then, the test vehicles were reflowed at four levels of peak temperature (180, 190, 200, and 220 °C) with three replicates. Thus, the thermal limit of a no-flow underfill was determined prevent underfill voiding during reflow process, while the same thermal limit should enable solders to wet for reflow stand point. After the solders melted, the test vehicles were held for three minutes at constant temperature to investigate the effect of reflow time on underfill voiding and eutectic solder wetting respectively. Typically, 90 seconds was used for reflow time.

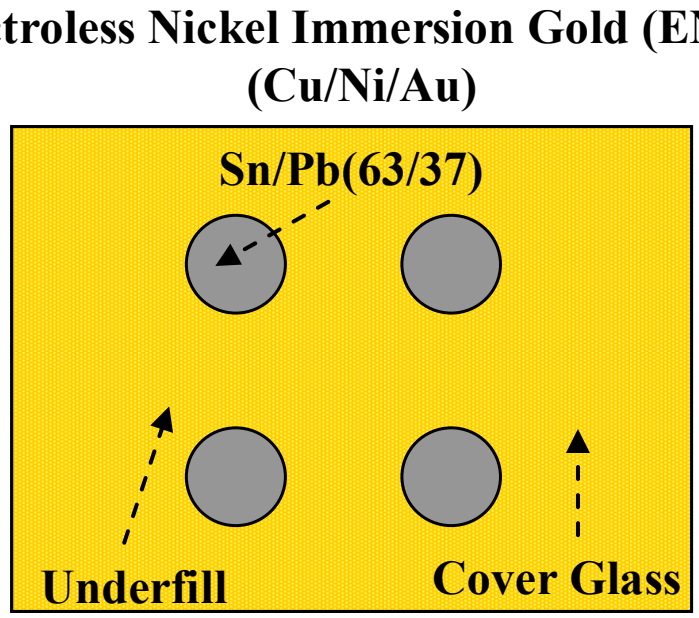


Figure 5-2 Schematic of test vehicle configuration used for void formation characterization 2

5.2.4 Void Reduction Study 2 (Effect of Peak Temperature on Voids)

The objective of void reduction study 2 was to validate the determined stable peak temperature enabling Sn/Pb (63/37) solder wet without outgassing using a commercial high IO, fine-pitch flip chip in package. Furthermore, this study characterized the reflow process to determine the process window for achieving high, stable yield and void-free assemblies. The reflow process parameters consider only peak temperature in two levels. The other parameters such as ramp rate, soak temperature, soak time, and reflow time were determined on past research to achieve a high, reliable yield assembly process [4, 5, 7] as described in Table 5-3. Thus, this study found the best reflow process conditions for high yield and for the minimum number of voids.

Prior to the assembly process, all moisture was driven out of the boards with exposure to an isothermal environment at 125 ºC for 3 hours. Next, the plasma pretreatment for substrate surface cleaning was applied to the moisture free FCIP test vehicle using pure argon (Ar) for 10 minutes to remove contamination. Then, high I/O, fine pitch flip chips were assembled using a commercial no-flow underfill with two replicates and reflowed on the process conditions described in Table 5-4.

Table 5-4 Design matrix used for void formation reduction study 2

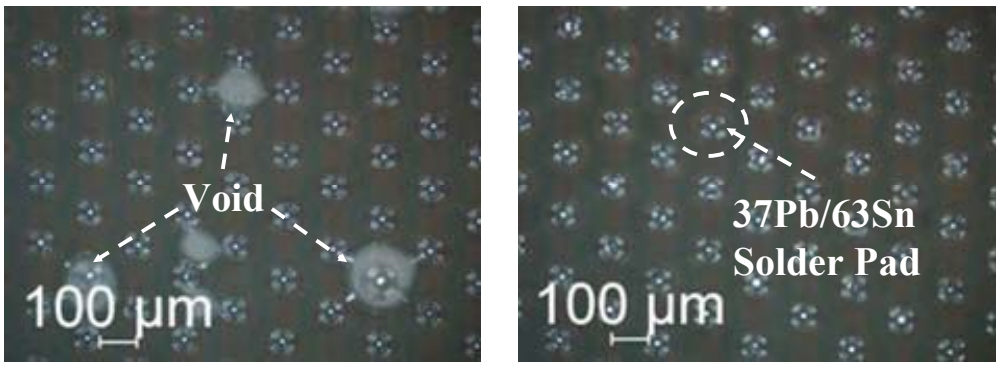
	Ramp rate	Soak temp	Soak time	Time above liquidus	Time above liquidus	Peak temp
Level 1	1.3°C/s	120 ~130 °C	120 sec	170 °C >	90 sec	180 °C
Level 2						190 °C

Finally, two void formation characterization and two void reduction studies determined the best reflow process conditions for a high yield and void-free assemblies using experimental techniques. The experimentally determined conditions were validated for mass production with large scale assemblies with more than 30 assemblies. The quantity is large enough to predict the result of mass production prior to actual assembly process on statistics.

5.3 PROCESS CHARTERIZATION EXPERIMENT RESULTS

5.3.1 Void formation characterization 1 (Effect of Soak Temperature and Soak Time on Voids)

The effect of soak temperature on void formation was investigated using a commercial no-flow underfill. The underfill did not exhibit underfill voiding as shown in Figure 5-3-(b) at a low soak temperature range from 120 to 130°C. On the other hand, voids were observed with the high soak temperature as shown in Figure 5-3-(a). Thus, the void formation characterization found that the soak temperature has a strong effect on underfill voiding with the high I/O, fine pitch flip chip.



(a) (b)

Figure 5-3 Micrographs of test vehicle in void formation characterization 1: (a) 140~170 °C soak temperature and (b) 120~130 °C soak temperature

Void formation characterization 1 found a low soak temperature could reduce the amount of underfill voiding. Hence, the underfill voiding could be controlled by optimizing conditions of the soak temperature and soak time. Next, void reduction study 1 investigated the effect of soak temperature and soak time with multiple levels using FCIP with a commercial no-flow underfill.

5.3.2 Void Reduction Study 1 (Effect of Soak Temperature and Soak Time on Voids)

A parametric study was designed to optimize the effect of soak temperature and soak time with four levels of conditions. This study found the limit of the reflow process, which achieved a high yield and minimum number of voids. The new suggested low soak temperature dramatically reduced the percent void area to 7.1% from 64.7% with high soak temperature as shown in Table 5-5 and Figure 5-4. The dark gray and white represent the underfill voiding in the micrograph from C-SAM (see Chapter 3). Underfill voiding could be controlled by modifying soak temperature and soak time in void formation characterization 1 and void reduction study 1 using a quantitative analysis. The low soak temperature and long soak time might be substantial factors in minimizing void area during the process.

Table 5-5 Void percent area of void reduction study 1

Condition	(1)	(2)	(3)	(4)
Ramp rate	1.3°C/s	1.3°C/s	1.3°C/s	1.3°C/s
Soak temp	140~170 °C	120~130 °C	120~130 °C	120~130 °C
Soak time	50 sec	90 sec	120 sec	150 sec
Time above liquidus	70 sec	70 sec	70 sec	70 sec
Peak temp	225 °C	225 °C	225 °C	225 °C
Void percent	64.7%	32.2%	19.8%	7.1%

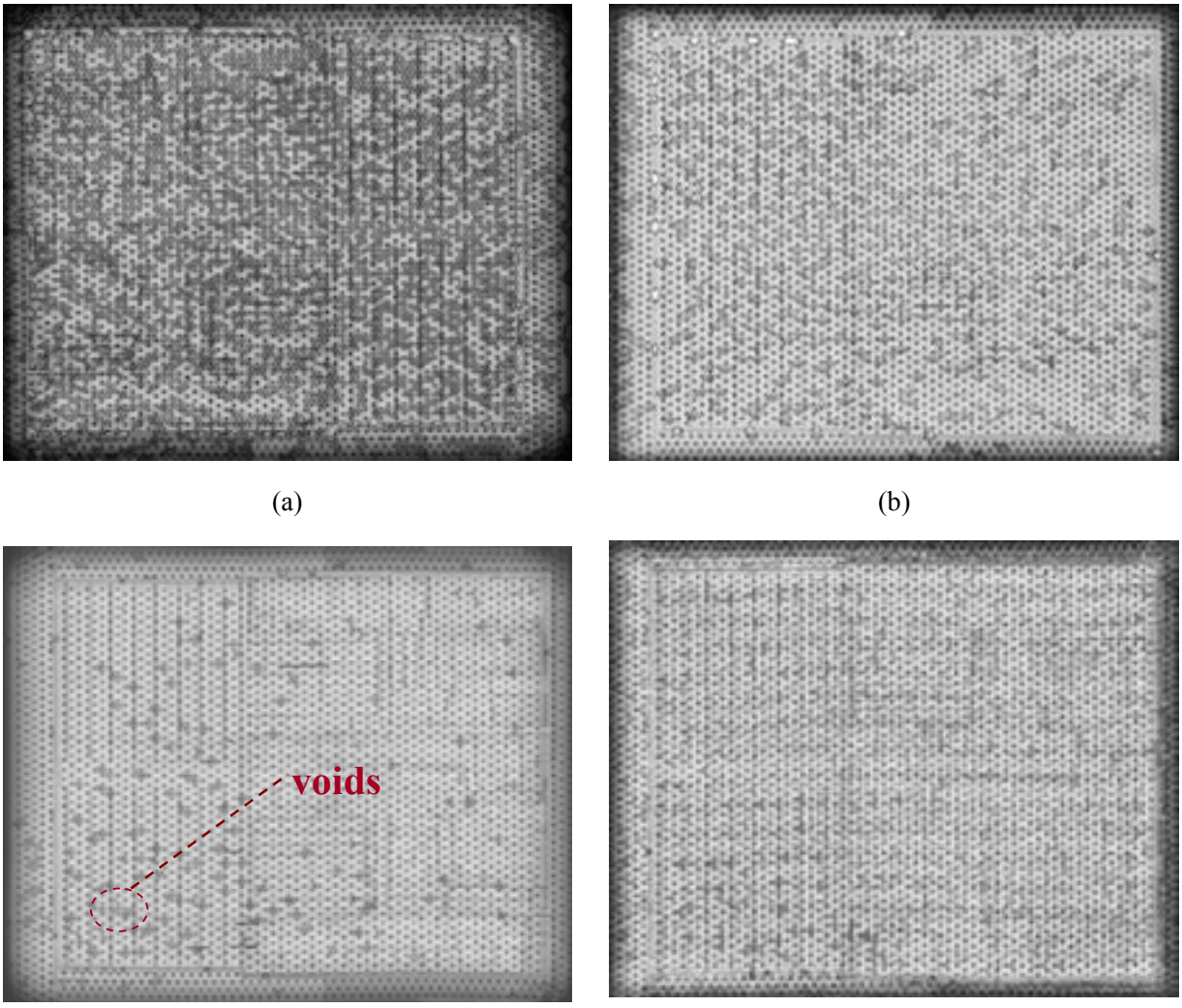
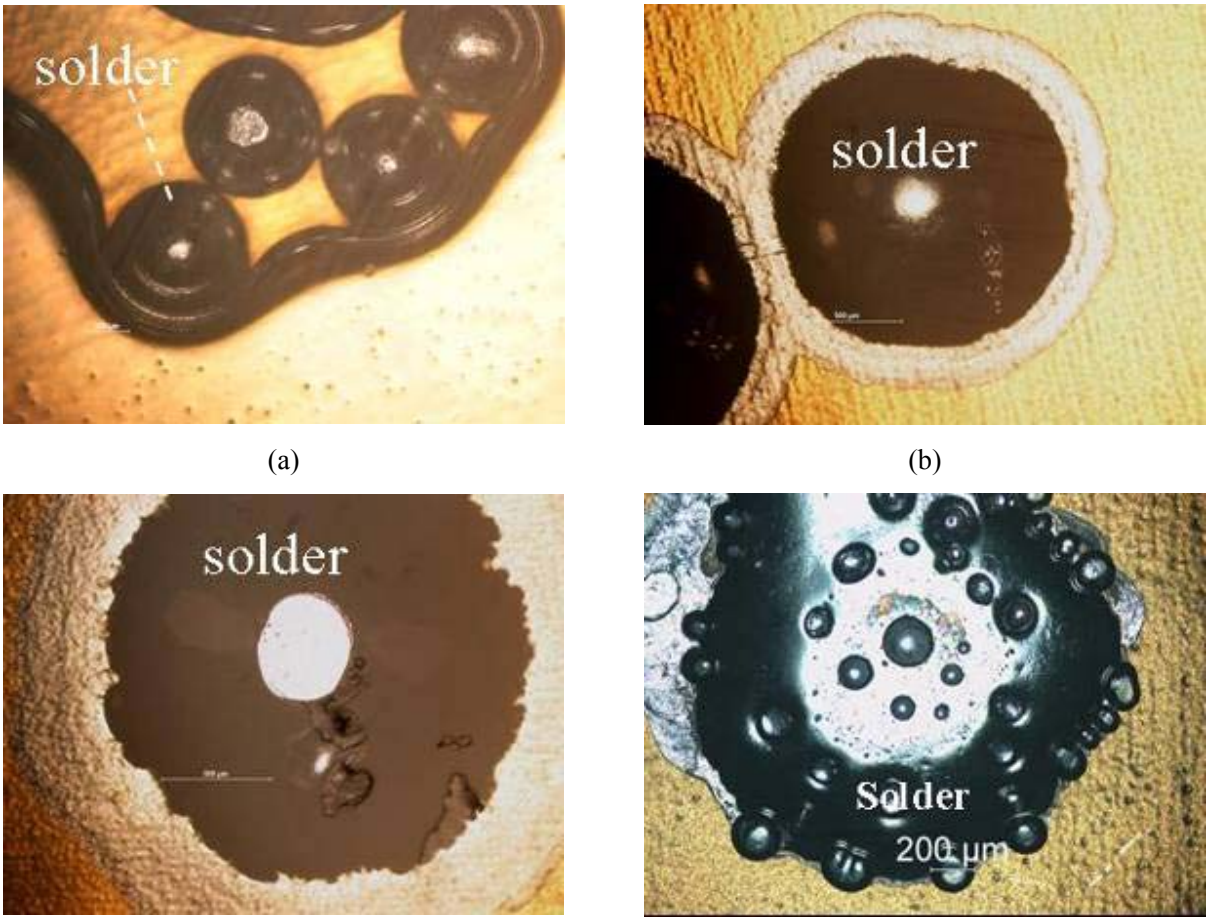


Figure 5-4 Micrographs of C-SAM in void reduction study 1 (ramp rate: 1.3°C/s, time above liquidus: 70 sec, peak temp: 225°C): void percent area (a) 64.7% (condition 1(soak temp/time): 140 ~ 170°C, 50sec), (b) 32.2% (condition 2: 120 ~ 130°C, 90sec), (c) 19.8% (condition 3: 120 ~ 130°C, 120sec), and (d) 7.1 % (condition 4, 120 ~ 130°C, 150sec)

5.3.3 Void Formation Characterization 2 (Effect of Peak Temperature on Voids)

The objective of this study was to investigate the effect of reflow process parameters such as peak temperature and reflow time on the void formation using parametric studies. These studies reviewed the stability of peak temperature, which ranged from 180ºC to 220ºC. No voids were observed in Figure 5-5-(a) and (b). In similar, a single void was observed in Figure 5-5-(c). At a result, temperature 190 ºC could be the best condition for Sn/Pb (63/37) solders wetting as well as underfill voiding during a wetting process. In contrast, a large number of voids were observed at 220 ºC. Void formation characterization 2 found that the high peak temperature and long reflow time generally increased the amount of underfill voiding. However, the reflow time does not have significant effect on the amount of underfill voiding at a low peak temperature range.



(a) (b)

(c) (d)

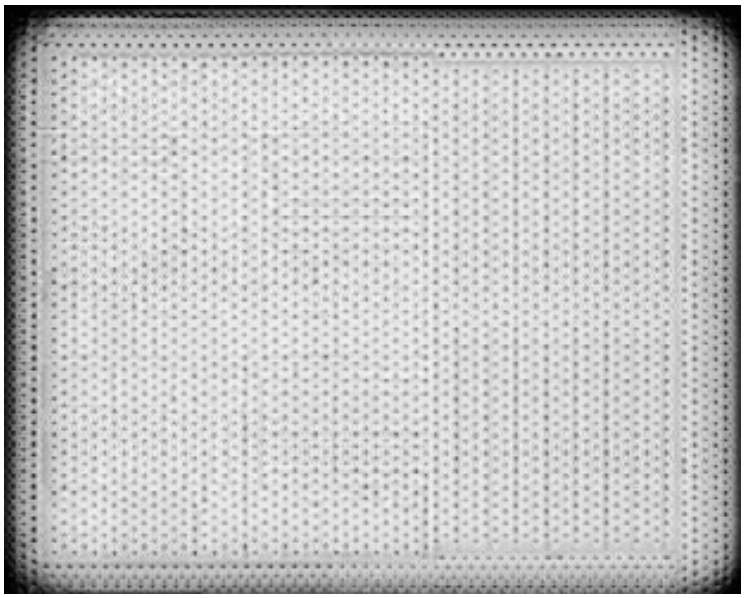
Figure 5-5 Micrographs of test vehicles in void formation characterization 2 reflow at : (a) 180 °C, (b) 190 °C, (c) 200 °C, and (d) 220 °C

5.3.4 Void Reduction Study 2 (Effect of Peak Temperature on Voids)

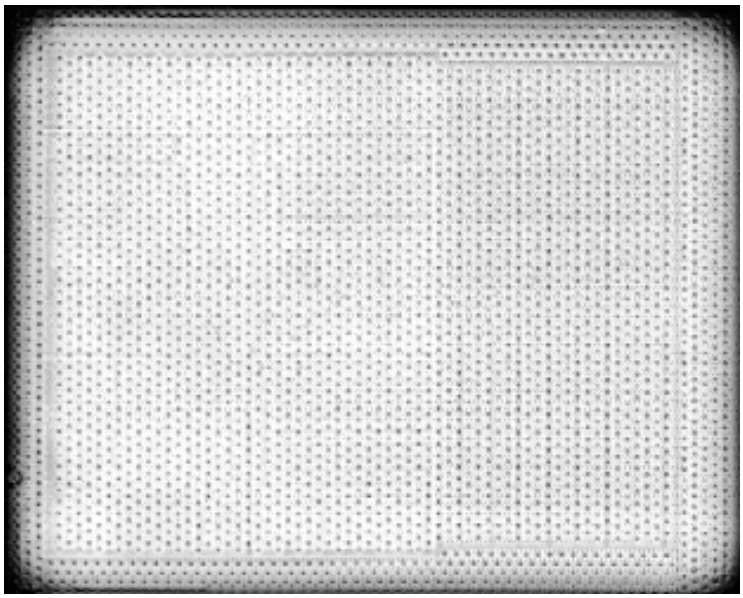
Underfill voiding could be controlled by modifying soak temperature and soak time in the void formation characterization 1 and void reduction study 1 [8, 58]. The studies minimized the void percent area of total flip chip from 64% to 7% with low soak temperature and long soak time. Namely, the best conditions could be achieved with low soak temperature and long soak time for minimum underfill voiding. With an understanding of the effect of soak zone conditions on underfill voiding, void formation characterization 2 determined the stable peak temperature range enabling Sn/Pb (63/37) solder to wet without producing any voids. Thus, these temperature ranges were used for the peak temperature of reflow process conditions in this void reduction study 2. Consequently, no voids were observed in both reflow conditions as shown in Figure 5-6 and Figure 5-7. In addition, 100% interconnects were achieved with 180 °C and 190 °C in peak temperatures respectively. Furthermore, the stability of the assembly process was evaluated using a large number of assemblies (30 parts) with 190 °C peak temperature as described in Table 5-6. The voids were not observed and the no yield loss occurred in any assembled part. Thus, these series of systematic studies determined a high, stable yield and void-free assembly process.

Table 5-6 Reflow profile conditions used for void reduction study 2 and experimental results

Ramp rate	Soak temp	Soak time	Time above liquidus (170 °C >)	Peak Temp	Assembled	Yielded
1.3°C/s	120 ~130 °C	120 sec	90 sec	190 °C	30	30

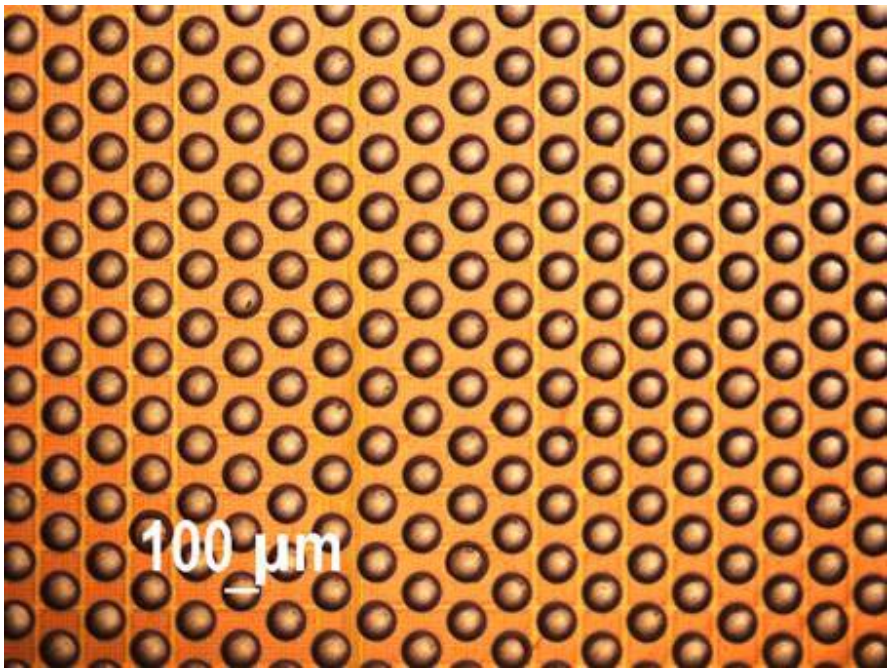


(a)



(b)

Figure 5-6 Micrographs of C-SAM for void reduction study 2:(ramp rate: 1.3°C/s , soak temp: 120 ~130 °C, soak time: 120 sec, time above 170°C: 90s) (a) peak temperature:180 °C (level 1) and (b) peak temperature: 190 °C (level 2)



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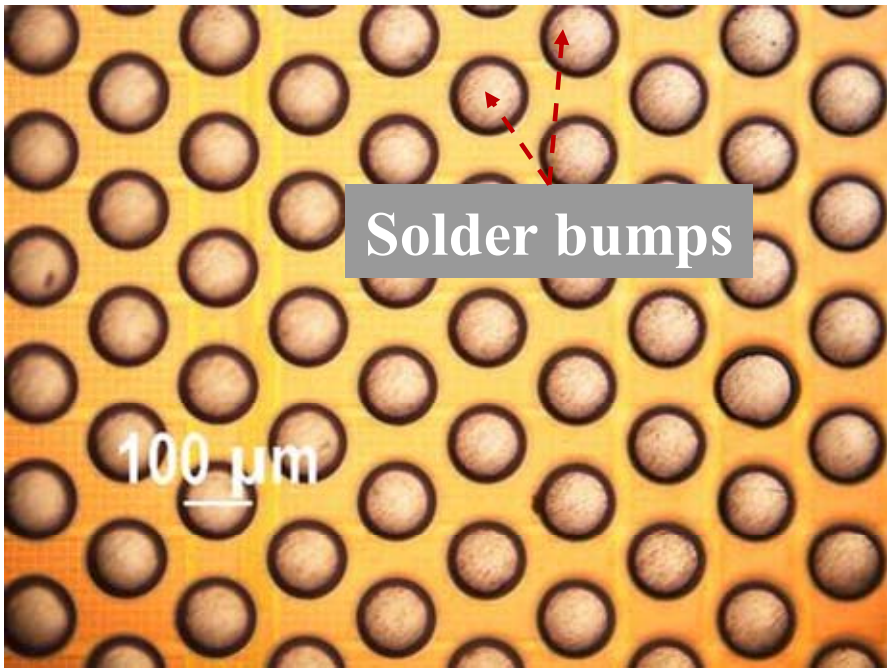


(b)

Figure 5-7 Micrographs of planar-sectional view of FCIP in void reduction study 2 (ramp rate: 1.3°C/s , soak temp: 120 ~130 °C, soak time: 120 sec, time above 170°C: 90s, peak temp: 190 °C): (a) magnification x50 and (b) x100

5.4 NO-FLOW UNDERFILL MATERIAL CHARACTERIZATION USING NANO-SIZE PARTICLES EXPERMENTAL APPPROACH

The objective of this study was to examine the feasibility of controlling void nucleation by modifying a no-flow underfill formulation. However, the formulation change was limited because the no-flow underfill used was commercially developed by a major electronics packaging material supplier. Thus, the underfill was reformulated by adding nano material to minimize underfill voiding. The idea was to intentionally distribute the supplied thermal energy to potential nucleation sites made by adding nano particles in underfill material. The nano sites act as a heterogeneous nucleation sites where nucleation occurs between two different materials. Indeed, a void is nucleated on the interface of the liquid underfill and a molten solder. For the void nucleation, thermal energy should exceed the Gibbs free energy (ΔG^*) at a critical radius (r^*) as shown in Figure 5-8. Then the void is stable and can grow to a macro size bubble. Below the critical Gibbs free energy, nucleated void is unstable and can perish. Thus, the potential nano sites will distribute thermal energy on the solder. The resulting energy will be below the critical Gibbs free energy. Consequently, a nucleated void is unstable and can't grow to macro size.

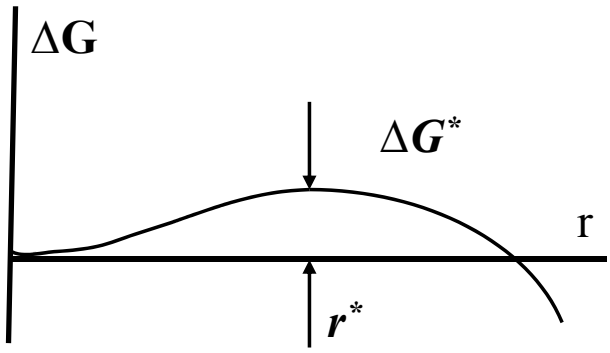


Figure 5-8 Typical Gibbs free energy for a heterogonous nucleation

This idea was validated using two different nano particles summarized in Table 5-7 [74-76].

Table 5-7 Summary of nano materials properties used for underfill material characterization

Name	Aluminum oxide	Bismuth
Symbol	Al_2O_3	Bi
CAS / Atomic number	1344-28-1	83
Density (g/cm^3)	3.97	9.78
Melting point (°C)	2054	272
Molar mass (g/mol)	101.96	208.98
Bulk surface energy (N/m)	0.0364	0.55

The effect of nano material on voiding was investigated using experimental techniques. Three studies were designed to investigate the effect of weight percent, size, and type of nano material on underfill voiding using a test vehicle illustrated in Figure 5-9 with a commercial no-flow underfill (see Table 3-1).

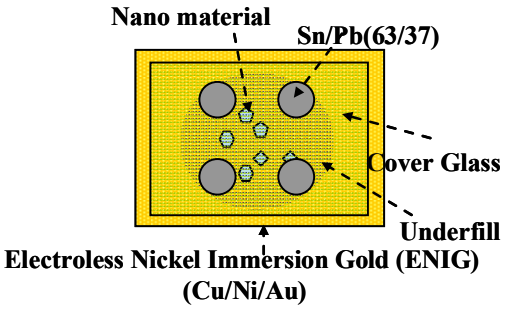


Figure 5-9 Schematic of a typical test vehicle configuration used in material characterization with nano materials

The test vehicle (TV) used consisted of a glass slide cover, four Sn/Pb (63/37) solder spheres, nano material, and an ENIG plated substrate. Prior to assembly, isopropyl

alcohol (IPA) was applied to the surfaces of the test vehicles to clean them. After this cleaning process, the test substrates were baked at 125°C for 3 hours to avoid out-gassing from moisture on the substrate. Next, four solder spheres were placed on the ENIG substrate. Then, the mixture of a commercial no-flow underfill and nano material was dispensed onto the ENIG substrate. The agglomerated nano particles could not be well distributed into no-flow underfill system using hand mixing. The presence of initial voids trapped by placing a glass cover on the underfill deposited substrate was inspected using an optical microscope. The TV was reflowed on a digital hotplate with a thermocouple attached to the ENIG substrate to measure the surface temperature of the TV. The assembled TV was reflowed from 100 °C preheating to 225 °C peak temperature which was held for 1 minute to give enough time for solder wetting and underfill curing. The void formation behaviors of no-flow underfill material were observed during the reflow process under the optical microscope. Each test vehicle process was performed in replicates of three.

First, the effect of quantity on voiding was investigated with three level of a weight percent composition of nano-size material as described in Table 5-8. The study used 50 nm of aluminum oxide (see Table 5-7).

Table 5-8 Effect of 50nm aluminum oxide weight percent on underfill voiding

Case	Weight percent (%)
Case 1	10.0
Case 2	3.0
Case 3	1.0

Second, the effect of size on voiding considered three levels such as 50nm, 75nm, and 100nm. Third, two nano materials, aluminum oxide and bismuth, were used to test the effect of nano material type on voiding as described in Table 5-9.

Table 5-9 Summary of underfill formulation using nano materials

Experiment	Name	Symbol	Size (nm)	Weight percent (%)
Effect of size on voiding	Aluminum Oxide	Al_2O_3	50, 100	3.0
	Bismuth	Bi	75	3.0
Effect of material type on voiding	Aluminum Oxide	Al_2O_3	50	3.0
	Bismuth	Bi	75	3.0

5.5 NO-FLOW UNDERFILL MATERIAL CHARACTERIZATION USING NANO-SIZE PARTICLES EXPERMENTAL RESULTS

In general, no voids were observed on the reformulated underfill deposited test vehicle (see Figure 5-10) with nano material at high yield assembly conditions, which produced a large number voids in the void formation study of chapter 3. The no-flow underfill was reformulated using nano materials such as aluminum oxide and bismuth. In detail, no voids were observed in case 1 (50nm Al_2O_3: 10.0%) and case 2 (50nm Al_2O_3: 3.0%). On the contrary, small number of voids was observed with case 3 (50nm Al_2O_3: 1.0%). Similarly, several voids were observed on the surface of solders formulated with 100nm aluminum oxide (100nm Al_2O_3: 3.0%) and bismuth (75nm Bi: 3.0%) as shown in Figure 5-11. Voids were not nucleated around the interface of solders and underfill with 100nm aluminum oxide (100nm Al_2O_3: 3.0%).

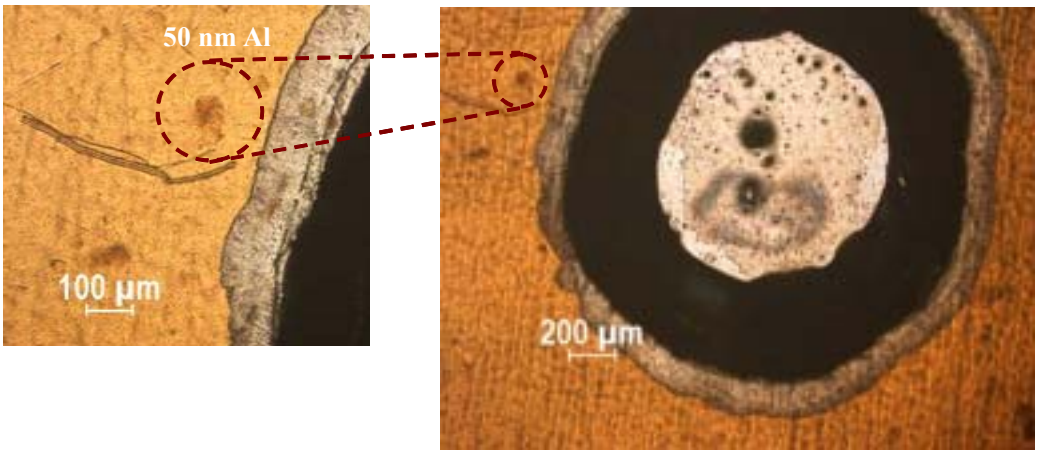
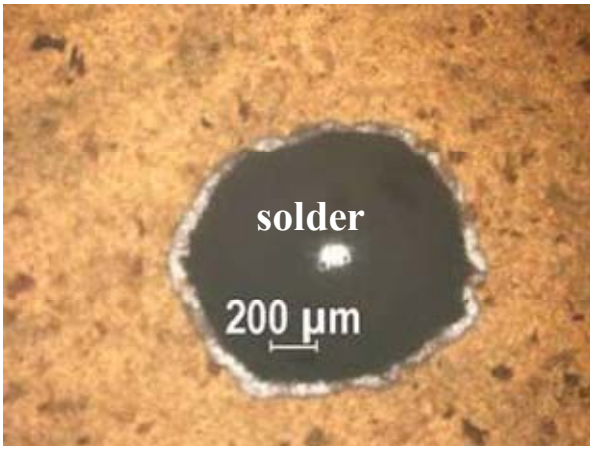
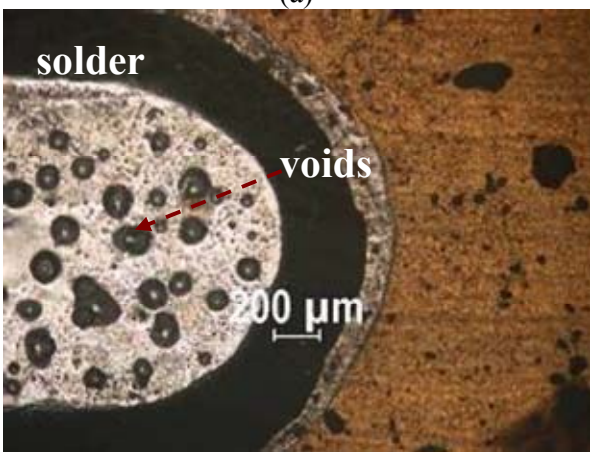


Figure 5-10 Micrographs of test vehicles used for underfill material formulation using 3.0% nano materials (case 2)



(a)



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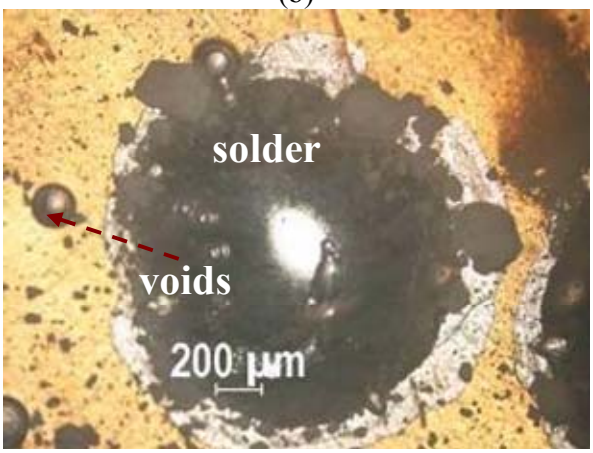


(c)

Figure 5-11 Micrographs of test vehicles with nano materials: (a) 50nm Al_2O_3 (10%), (b) 100nm Al_2O_3 (3%), and (c) 75nm Bi (3%)

5.5.1 Effect of Nano Particle Size and Weight Percent on Underfill Void Nucleation

Table 5-10 summarized the experimental results in underfill material characterization to minimize the amount of underfill voiding. In characterization, the weight percent and material particle size were significant factors affecting underfill voiding.

Table 5-10 Effect of particle weight percent and raw material size on underfill voids

Nano particle weight percent (%)	**Voids (Intensity)**	**Comments**
10.0 (50 nm Al_2O_3)	X	
3.0 (50 nm Al_2O_3)	X	
1.0 (50 nm Al_2O_3)	O (+)	Voids nucleated around molten solders.
Raw material particle size(nm)	**Voids (Intensity)**	**Comments**
50 (3.0% Al_2O_3)	X	
100 (3.0% Al_2O_3)	O (+)	Voids nucleated around molten solders.

One the results, above three weight percent of 50 nm aluminum oxide (Al_2O_3) distributed thermal energy on each heterogeneous nano site, substantially decreasing excessive energy below required thermal energy at critical point. In contrast, moderate amount of underfill voiding was nucleated on the test vehicles assembled using no-flow

underfill formulated with three percent of 100nm aluminum oxide (Al_2O_3). The 100nm aluminum oxide (Al_2O_3) failed to prevent the energy concentration below critical point on the molten solders. Because 100nm aluminum oxide (Al_2O_3) created less number of nucleation sites comparing to 50nm aluminum oxide (Al_2O_3) at the same weight percent, the insufficient number of nucleation sites failed to decrease substantially energy concentration below the critical point. Namely, some number of heterogeneous nucleation sites is necessary required to abate the excessive energy below the critical point to prevent void nucleation in the assembly process.

5.5.2 Effect of Nano Materials on Underfill Void Nucleation

Aluminum oxide (Al_2O_3) and bismuth (Bi) were used for heterogeneous nucleation sites to control underfill voids. With 75nm bismuth (Bi), a large number of voids were nucleated on the interface between a molten solder and no-flow underfill. Besides, voids nucleation was observed on the no-flow underfill far from the molten solder. The bismuth in the underfill acted as a heterogeneous nucleation site, producing voids. In contrast, 50nm aluminum oxide (Al_2O_3) in the no-flow underfill prevented void nucleation by distributing thermal energy on the additional heterogeneous nucleation sites using nano particles.

Table 5-11 Effect of nano materials type on underfill voids

Material	Voids (Intensity)	Comments
50 nm Al_2O_3	X	Bulk surface energy (N/m): 0.0364
75nm Bi	O (+++)	Bulk surface energy (N/m): 0.55 Voids nucleated around molten solders and on the liquidus underfill.

As described in Table 5-11, a significant difference between two nano particles was observed in the surface energy. Indeed, the surface energy can be a control parameter of the required Gibbs free energy at critical point for a heterogeneous void nucleation as described in equation (5-1). On the equation, the nano materials type influences surface energy between a heterogeneous nucleation site in solid state and a void in gas state, γ_{SG}. Typically, bismuth (γ_S: 0.55 N/m) exhibits relatively high γ_{SG} comparing to aluminum oxide (γ_S: 0.0364 N/m).

$$\Delta G^*_{het} = \frac{16\pi\gamma_{LG}{}^3}{3\Delta P^2} S(\theta) = \frac{16\pi(\gamma_{LS}-\gamma_{SG})^3}{3\Delta P^2 \cos\theta^3} \times \frac{(2+\cos\theta)(1-\cos\theta)^2}{4} \qquad (5\text{-}1)$$

where $\gamma_{SG} = \gamma_S + \gamma_G - 2(\gamma_S\gamma_G)^{1/2}$.

The relatively high surface energy of a nucleation site (γ_S) with bismuth subsequently decreased the required Gibbs free energy. With a decrease of energy requirement for a void nucleation using bismuth, a heterogeneous void nucleation can occur at comparatively low energy. Therefore, void intensity was increased using bismuth nano particles.

5.6 DISCUSSION AND CONCLUSIONS

A large number of voids was created by the chemical reaction between solder wetting and no-flow underfill curing during the reflow process [8]. The result of Chapters 3, 4, and 5, the mechanism of underfill suggested a low soak temperature range from 120 ~ 130 °C in order to reduce the amount of underfill voiding by providing stable conditions for underfill processing.

Void formation characterization 1 investigated the effect of soak temperature and soak time on underfill voiding. With a low soak temperature from 120 to 130°C, no voids were observed in the simple device consisting of a glass slide cover on the underfill deposited substrate. Therefore, low soak temperature could be the potential way to minimize underfill voiding in the flip chip with high I/O density and fine pitch. With the effect of soak zone conditions on underfill voiding, the void reduction study 1 optimized process conditions to minimize the amount of underfill voiding using parametric studies. The parametric study dramatically reduced the void percent area from 64% to 7% by modifying the reflow process conditions. Next, void formation characterization 2 found the stable peak temperatures for a robust Sn/Pb (63/37) solder wetting not producing voids using a simple TV as illustrated in Figure 5-5. Then, the result of void formation characterization 2 was validated using a commercial high I/O, fine pitch assemblies with 30 replicates in void reduction study 2. Thus, the stability of the assembly process was accomplished with high repeatability. The stable process used low soak temperature and peak temperature. The low soak temperature enabled the fluxing agents to remove oxidation around solders and restore it to participate into underfill curing at stable

condition. Consequently, the void area percent could be reduced from 64% to 7%. Low peak temperature, 190 °C, provided enough thermal energy solders to wet in the assembly process while the energy was below than critical point for stable void nucleation. Consequently, the resulting energy eliminated voids in assembly process.

In addition, classical bubble nucleation was explored to change underfill material formulation using nano particles. Through the study, three factors were examined for the underfill material characterization using 50 nm aluminum oxide (Al_2O_3), 75nm bismuth (Bi), and 100nm aluminum oxide (Al_2O_3). As the result, above 3.0 weight percent of 50nm aluminum oxide could eliminate underfill voids using reformulated underfill combined with nano particles. One the results, above three weight percent of 50 nm aluminum oxide (Al_2O_3) distributed thermal energy on each heterogeneous nano site, substantially decreasing excessive energy below required thermal energy at critical point. In contrast, the three weigh percent of the 100nm aluminum oxide (Al_2O_3) failed to prevent the energy below critical point, because the 100nm Al_2O_3 created less number of nucleation sites comparing to 50nm aluminum oxide (Al_2O_3) at the same weight percent. Similarly, the heterogeneous nucleation sites created using nano particles dissipated gas available without a source of continuous supply. These results in a less gas available per void nucleated. Without the necessary gas supply for stable nucleation, the void cannot grow to the critical size. Namely, some number of heterogeneous nucleation sites is necessary required to abate the excessive energy below the critical point or dissipate gas available to prevent void nucleation in the assembly process.

The three weight percent of 75nm bismuth (Bi) induced a large number of voids nucleated on the interface between a molten solder and no-flow underfill. Besides, voids nucleation was observed on the no-flow underfill far from the molten solder. The bismuth in the underfill acted as a heterogeneous nucleation site, producing voids. A significant difference between Bi and Al_2O_3 was observed in the surface energy. Indeed, the surface energy can be a control parameter of the required Gibbs free energy at critical point, ΔG^*_{het}, for a heterogeneous void nucleation

$$\Delta G^*_{het} = \frac{16\pi\gamma_{LG}{}^3}{3\Delta P^2} S(\theta) = \frac{16\pi(\gamma_{LS}-\gamma_{SG})^3}{3\Delta P^2 \cos\theta^3} \times \frac{(2+\cos\theta)(1-\cos\theta)^2}{4}.$$

On the equation, the nano materials type influences surface energy between a heterogeneous nucleation site in solid state and a void in gas state, γ_{SG}. Typically, bismuth (γ_S: 0.55 N/m) exhibits relatively high γ_{SG} comparing to aluminum oxide (γ_S: 0.0364 N/m). The relatively high surface energy of a nucleation site (γ_S) with bismuth subsequently decreased the required Gibbs free energy. With a decrease of energy requirement for a void nucleation using bismuth, a heterogeneous void nucleation can occur at comparatively low energy. Therefore, void intensity was increased using bismuth nano particles.

Consequently, the findings in this chapter provide the design guideline for the high, reliable yield and void-free assembly process using no-flow underfill with high I/O, fine pitch flip chip. This study enables a no-flow underfill process applicable to industry, which has great advantages such as low cost and high throughput. In addition, underfill material characterization tests found conditions preventing underfill voiding during solder wetting and underfill curing. At the high range of temperature, no voids were

observed using reformulated with nano-size particles. The reformulated underfill can be applied to lead-tin eutectic as well as lead-free applications.

CHAPTER 6

DYNAMIC ANALYSIS OF VOID NUCLEATION AND VOID GROWTH IN FLIP CHIP PACKAGE

6.1 INTRODUCTION

Chapter 3 investigated the plausible causes of void formation. From the experimental investigation, the root cause of void formation was determined to be chemical reactions between solder wetting and underfill curing combined with a thermal effect from the reflow process. In addition, sources of void formation could be water vapor or flux agent vapor. Chapter 4 examined the source of chemical reactions and identified the chemical compounds present in the reaction. The chemical compounds were water and acetic acid, which were suspected as the sources of void formation in chapter 3. Thus, Chapter 6 provided the physical understanding of void formation induced by the chemical reaction of a flux agent combined with a thermal effect using classical nucleation theory. This study developed a void nucleation and void growth model respectively during flip chip assembly process using classical bubble nucleation theory and bubble growth dynamics. The classical bubble nucleation and bubble growth theories were reviewed in detail in the Chapter 2: literature review. These previous studies were modified to apply to void nucleation and void growth to flip chip packaging during assembly processes. Furthermore, these understandings can provide the theoretical foundation to achieve a high, stable yield and void-free assembly process. Hence, the assembly process can

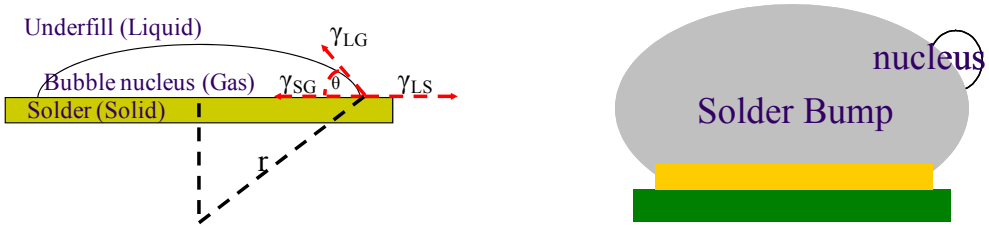
achieve high performance, thermal reliability with a high I/O, fine-pitch flip chips using no-flow materials.

6.2 UNDERFILL VOIDING MODELS

6.2.1 Heterogeneous Void Nucleation Model

The mechanism of voiding in FCIP will be modeled using the classical nucleation theory. Nucleation was considered to be heterogeneous, because the voids are nucleated at the interface of two homogenous materials such as no-flow underfill and solder. On the interface, solder melting with underfill curing process transferred thermal energy on the void nucleation site. The nucleation is the formation of fluctuations in phase transitions. After the critical nuclei are formed by the phase transitions, some becomes so large that they are stable in case of excessive transferred energy above required Gibbs free energy at critical point. Then the void will grow to macroscopic dimensions under isothermal condition. The Figure 6-1 illustrates a schematic of void nucleation on the surface of a solder sphere at the interface between the solder and underfill during the reflow process.

The formation of a void has an associated excess energy equal to the Gibbs free energy of void formation. The change in Gibbs free energy during a gas formation is given by the energy associated with forming a new interface among the solder, the no-flow underfill, and the void plus the volumetric work performed to produce the volume of a void. This change in Gibbs free energy for the application of FCIP happens on the smooth surface of hot molten solder as illustrated in Figure 6-1 under heterogeneous nucleation, assuming a reversible, isothermal thermodynamic process.



(a) (b)

Figure 6-1 Schematic of heterogeneous bubble nucleation on smooth surface: (a) on the smooth surface of a rigid glass and (b) on the smooth surface of a rigid solder

Thus, the heterogeneous nucleation accounts for void nucleation on the smooth solder surface, given by equation (6-1) [32, 36, 37, 39, 77-79]. Assume that the void forms a wetting angle, θ.

$$\Delta G_{het} = -V_G \Delta P + \gamma_{LG} A_{LG} + \gamma_{SG} A_{SG} - \gamma_{LS} A_{SG} \tag{6-1}$$

where A_{LG} and A_{SG} are surface geometric factors $A_{LG} = 2\pi\left(1-\cos\theta\right)r^2$ and $A_{SG} = \pi\left(\sin^2\theta\right)r^2$.

V_G is the volume of the spherical cap of a void as follows:

$$V_G = \frac{4\pi r^3}{3}\left(\frac{2-3\cos\theta+\cos^3\theta}{4}\right). \tag{6-2}$$

In addition, ΔP is the difference in the pressure of the gas in the void and the environmental nucleation pressure, γ is interfacial surface energy between liquid and gas (LG), solid and gas (SG), liquid and solid (LS), and r is the radius of a spherical void on the solder bump (Figure 6-1). The surface tension balance gives the following:

$$\gamma_{LS} = \gamma_{SG} + \gamma_{LG}\cos\theta. \tag{6-3}$$

With algebraic manipulation, equation (6-1) can be written as

$$\Delta G_{het} = \left[-\frac{4\pi r^3}{3}\Delta P + 4\pi r^2 \gamma_{LG}\right] S(\theta) \tag{6-4}$$

where $$S(\theta)=\frac{(2+\cos\theta)(1-\cos\theta)^2}{4}. \tag{6-5}$$

The equation (6-4) determines the maximum of the Gibbs free energy where

$$\frac{d(\Delta G_{het})}{dr}=0 \qquad\qquad \frac{d^2(\Delta G_{het})}{dr^2}<0$$

yielding the critical radius of void $$\therefore R_0=\frac{2\gamma_{LG}}{P_G-P_L}=\frac{2\gamma_{LG}}{\Delta P} \tag{6-6}$$

The minimum required energy can be calculated by plugging equation (6-6) into

equation (6-4) and then yielding $$\Delta G^*_{het}=\frac{16\pi\gamma_{LG}^{\ 3}}{3\Delta P^2}S(\theta). \tag{6-7}$$

Next, The Gibbs free energy is associated with a maximum excess free energy, termed the critical point. With the Gibbs free energy at the critical point, the heterogeneous nucleation rate N_{het}, equation(6-8), represents the rate of formation of voids per unit time per unit volume.

$$N_{het}=Cf\exp\left(\frac{-\Delta G^*_{het}}{kT}\right) \tag{6-8}$$

where C is concentration of available heterogeneous nucleation sites, f is frequency factor of gas molecules, T is temperature, and k is Boltzmann's constant. The natural logarithm of equation (6-8) is taken, yielding where C is concentration of available heterogeneous nucleation sites, f is frequency factor of gas molecules, and k is Boltzmann's constant.

$$\ln N_{het}=\ln\left[Cf\exp\left(\frac{-\Delta G^*_{het}}{kT}\right)\right] \tag{6-9}$$

$$\ln N_{het}=\frac{-\Delta G^*_{het}}{k}\frac{1}{T}+\ln Cf\ . \tag{6-10}$$

Experimental techniques determined the nucleation rate by counting the number of voids in the device at different temperatures. Then, the nucleation rate can determine the ΔG^*_{het} (Gibbs free energy) and $\ln Cf$ with Arrhenius equation relationship using equation (6-10). Namely, a plot of $\ln N_{het}$ versus T^{-1} gives a straight line, whose slope and intercept can be used to determine ΔG^*_{het} and $\ln Cf$.

6.2.2 Void Growth Model

This study examined void growth in molten underfill. The underfill is approximated as a Newtonian fluid depending on its rheological characteristics. The experimentally measured rheology exhibits Newtonian, shear thinning and shear thickening characteristics over the shear rates and temperatures studied [15]. The void grows driven by gas diffusion. A void nucleated under high pressure P_{G0} with the uniform gas concentration of $c_0 = K_H P_{G0}$. Then, the gas pressure is suddenly reduced to liquid underfill pressure, P_a. Simultaneously the void proceeds to grow as the gas diffuses into the void. The void growth in underfill could be investigated using the Rayleigh-Plesset equation (see equation(6-11)) widely used for bubble growth in a Newtonian fluid during the assembly process. Indeed, the equation considered the relation between the growing void and the gas pressure using mass conservation at the interface with initial conditions of $R(0) = R_0$ and $\dot{R}(0) = 0$. The initial conditions are the critical conditions at thermodynamic and mechanical equilibrium. The equilibrium conditions using Young-Laplace equation, $P_G = P_L + \frac{2\gamma_{LG}}{R}$, determined the critical void size, R_0, for an initial condition. After the gas concentration and gas pressure decrease to the nearly equilibrium level of environment of a growing void, the void growth will be ceased. This described mechanism exhibits quasi-equilibrium state during a void growth. Thus, this void growth could be assumed to be at thermodynamic equilibrium. Besides, the temperature change of the system was negligible so that an isothermal process could be assumed.

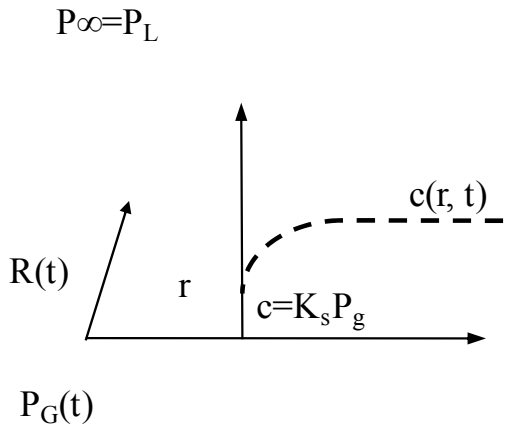


Figure 6-2 Schematic of a void growth induced by gas diffusion in molten no-flow underfill during assembly process

First, the voids are approximated as spherical and the growth process is approximated as isothermal. The molten underfill was assumed to be incompressible. Under these considerations, the system is schematically illustrated in Figure 6-2. The illustrated dynamic model of growing void is employed given by:

$$\rho_L\left(\frac{3}{2}\dot{R}^2+R\ddot{R}\right)=-\frac{4\mu_L\dot{R}}{R}+\left(P_G-P_L-\frac{2\gamma_{LG}}{R}\right) \tag{6-11}$$

where R is radius of the void, ρ_L is the density of molten underfill*, and* μ_L is the viscosity of molten underfill. In order to determine the radius and pressure of the void, additional equations are needed. The gas inside the voids is assumed to be ideal with uniform pressure. Applying continuity to the interface between void and no-flow underfill yields:

$$\frac{\partial}{\partial t}\left(P_G R^3\right)=3\rho_L D R^2\left.\frac{\partial c}{\partial r}\right|_{r=R} \tag{6-12}$$

where D is the diffusivity, ρ_L is underfill density, t is time, r is spatial variable, and c is the local gas concentration. The diffusivity of a gas into underfill was determined using an analytical study (see Appendix B) [70, 71]. As the gas concentration of equation (6-13) depends on the rate that gas diffuses towards the void and the rate at which the void expands, the local gas concentration is governed by:

$$\frac{\partial c}{\partial t} + v_r \frac{\partial c}{\partial r} = \frac{1}{r^2}\frac{\partial}{\partial r}\left(r^2 D \frac{\partial c}{\partial r} \right) \tag{6-13}$$

The governing equation was supplemented by the following initial and boundary conditions: $c(r,0) = K_H P_{G0} = c_0$, $c(\infty,t) = c_0$, and $c(R,t) = K_H P_G(t)$. Because the gas inside the voids was assumed to be an ideal gas, the gas concentration is governed by Henry's law $c = K_H P_G$, where K_H is Henry's law constant at the interface between gas and liquid underfill (see Appendix C) [80-82]. At the infinite depleted zone of the gas concentration, Neumann boundary condition $\left.\frac{\partial c}{\partial r}\right|_{t,r\to\infty} = 0$ (gas concentration gradient) was applied to the outer of the gas because mass conservation can be expressed as a no-mass flux condition at the boundary. At far distance from a void, gas concentration has some level of gradient outer of the gas in the liquid underfill since the gas was produced locally on the interface between solder and underfill. However, the gas concentration outside the void nucleated was assumed to be uniform and in equilibrium with P_G. Even though gas concentration is non-uniform at the infinite region of a void outside, the gas region dominant for a void growth has a negligible gradient since the region is relatively close to the uniform gas concentration region created [38, 46, 83]. In addition, the effect of growing void should be negligible at a far distance from the void and gas from the outer boundary of molten underfill diffused into a void. Therefore the concentration at

any time can assumed to be the initial concentration. Consequently, the Neumann boundary conditions could be replaced with $c(\infty,t)=c_0$ The void will be expanded by gas diffusion from underfill outgassing. The major source of gas was identified as carboxylic acid, which is typically used as a fluxing agent in no-flow underfill [8]. Therefore, model constants such as diffusivity and Henry's constant follow the material property of carboxylic acid (see Appendix B and C) [84-87]. Thus, the void growth can be explained by simultaneously solving equations (6-11), (6-12) and (6-13).

6.3 MODELS ANALYSIS

6.3.1 Heterogeneous Void Nucleation

The heterogeneous void nucleation rate was measured using experimental techniques with a simple Test Vehicle (TV) as depicted in Figure 6-3. Figure 6-3-(a) and Figure 6-3-(b) illustrated the top-view and the planar-view of the schematic of a typical test vehicle configuration used for heterogeneous nucleation rate measurement respectively.

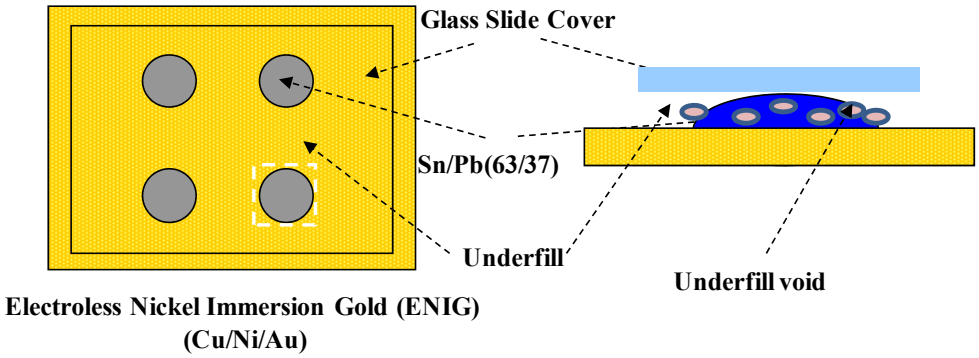


Figure 6-3 (a) Top-view of schematic of a typical test vehicle configuration used for heterogeneous nucleation and (b) Planar-view of the schematic of a test vehicle

First, the TV placed on the hot plate was inspected using a visual microscope. Simultaneously, the time was measured between the start and the end of voiding. Finally, the experiment was conducted when the voiding stopped. Next, a visual microscopy was used to count the number of voids on the surface of a solder in a unit area (5.51mm^2) as shown in Figure 6-3. The white square of Figure 6-3-(a) was magnified using visual microscopy as shown in Figure 6-4. The magnified area shows 15 nucleated voids in the area of 0.202 cm x 0.271 cm at 230 °C. Indeed, void nucleation occurred on the 3-D molten solder as shown in Figure 6-3-(b). Therefore, the number of voids could be

counted in a unit volume to calculate Gibbs energy change at critical condition (ΔG^*_{het}) and material properties (ln*Cf),* instead of a unit area. However, the voids were nucleated only on the surface of a molten solder. The height of molten solder (< 2μm) relatively small comparing to the area of the molten solder spread. Hence, the interesting region of void nucleation rate could consider 2-D molten solder area to determine the model constants, instead of a 3-D sphere. Besides, the Gibbs energy change at critical condition (ΔG^*_{het}), used for the model of a void growth, was calculated by counting number of voids at certain temperature regardless of interesting for void nucleation rate measurement since ΔG^*_{het} corresponds to slope of equation (6-14). In contrast, material properties, ln*Cf,* depends on the interesting region of void nucleation. The ln*Cf* was not significant for the model of nucleation and the model of a void growth. It implies that unit area could be acceptable for an interesting region to calculate nucleation rate.

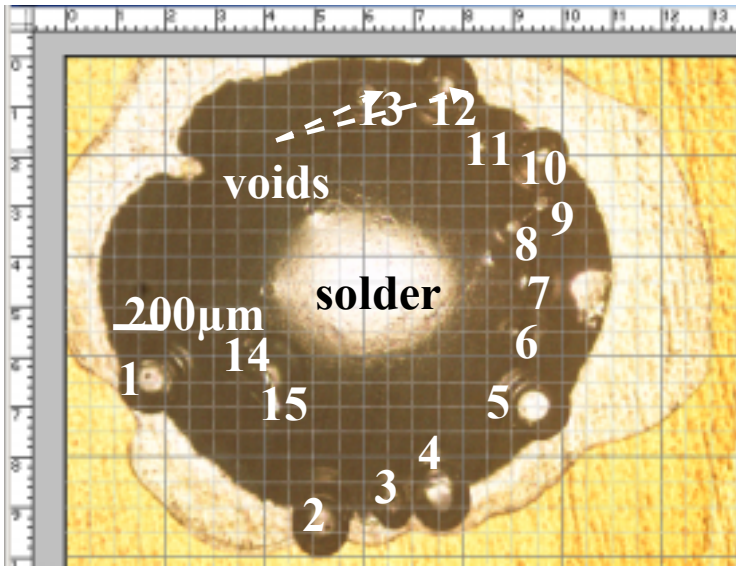


Figure 6-4 Micrograph of a typical visually magnified test vehicle with 15 nucleated voids after heating at 230° C

At each temperature, the number of voids was counted using the above explained experimental procedure. As according to the experiment, Table 6-1 presented the number of voids nucleated during process with five duplicates. The mean value was selected for the calculation of void nucleation rate.

Table 6-1 Counted the number of voids at the five level of temperature

Temperature	230 °C	237 °C	240 °C	245 °C	250 °C
Nucleation time	25.63 sec	16.82 sec	17.19 sec	7.56 sec	5.84 sec
# of voids	15	19	19	15	18
	16	16	17	23	18
	17	20	20	19	25
	16	15	18	19	22
	15	18	19	20	15
Average	15.8	17.6	18.6	19.2	19.6
Stand deviation	0.836	2.073	1.140	2.863	3.911

The number of voids divided by the measured time was defined as the nucleation rate:

$$\ln N_{het} = \frac{-\Delta G^*_{het}}{k}\frac{1}{T} + \ln Cf \ . \tag{6-14}$$

The number of voids calculated nucleation rate by dividing the number of nucleated voids by unit region and nucleated time. Thus, nucleation rate was measured as a function of temperature using simple test vehicles as shown in Table 6-2 at five temperatures with five replicates.

Table 6-2 Measured void nucleation rate at the five level of temperature

T	230 °C	237 °C	240 °C	245 °C	250 °C
1/T	0.001988	0.001960	0.001949	0.001930	0.00191
lnN	2.4280	2.9445	2.9780	3.8312	4.1099

Nucleation rate and temperature were measured by experiment and were plugged into equation (6-14) to determine the Gibbs free energy at critical condition (ΔG^*_{het}) and ln*Cf*. This equation was expressed as the Arrhenius relationship as shown in Figure 6-5.

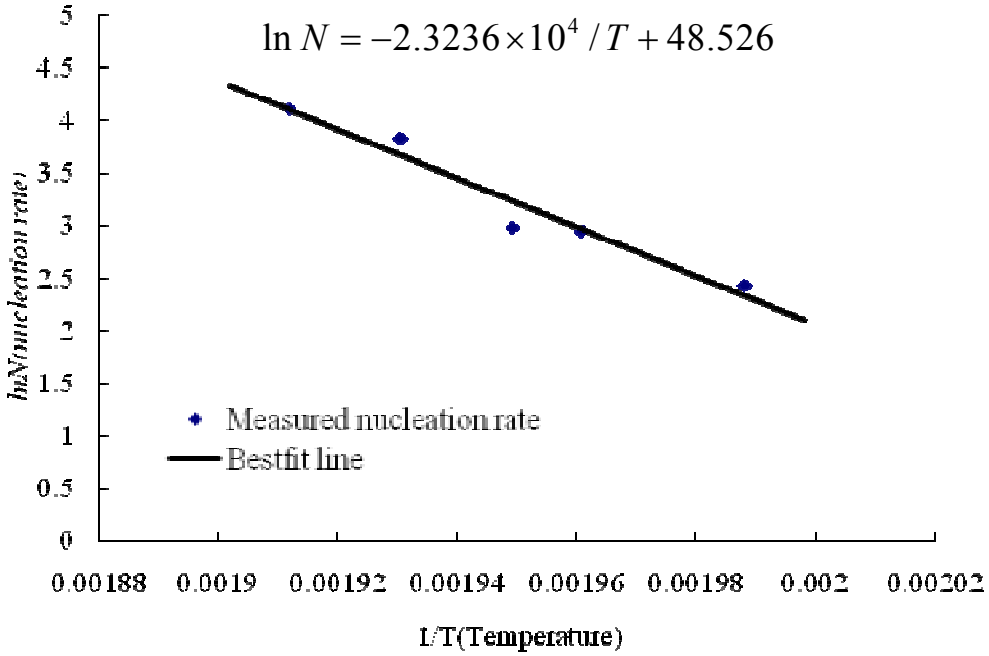


Figure 6-5 Void nucleation rate versus 1/T(Temperature)

A plot of ln N_{het} versus T^{-1} gives a straight line, whose slope and intercept can be used to determine ΔG^*_{het} and ln*Cf*. The slope presents the Gibbs free energy and the y intersect is associated with the ln*Cf*. The Gibbs free energy and ln*Cf* are presented in Table 6-3.

Table 6-3 Calculated Gibbs free energy and ln*Cf* of void nucleation in unit area

Gibbs free energy (kg cm^2/s^2)	Cf (void/cm^2s)	area (mm^2)
3.207×10^{-15}	1.187 $x10^{21}$	5.51

Next, the surface tension among solders, underfill, and void was calculated using the experimental data [88, 89] to determine the critical void size for the initial conditions of

void growth models. Equation (6-3) can calculate the contact angle among solid, liquid and gas with interfacial energy between each state. The interfacial energies, $\gamma_{LG,}$ $\gamma_{LS,}$ and γ_{GS}, were calculated using equation (6-15) with surface energy at each condition as described in Table 6-4. However, the referred surface tension did not meet the surface energy equilibrium equation(6-3). Besides, the high surface tension of solder exhibits high wettability of a gas on the solder, subsequently causing a low contact angle. The contact angle of a void was assumed to be 20° and determined the geometric factor, S(θ) as described in Table 6-4 on other research regarding a void growth in polymer solution [36, 37, 90]. Table 6-4 presents the interfacial energy of underfill at liquid and gas interface. The surface tension between underfill and a gas void was calculated using surface tension balance equation (6-15) [88, 89].

$$\gamma_{LG} = \gamma_L + \gamma_G - 2\left(\gamma_L \gamma_G\right)^{1/2}. \tag{6-15}$$

Table 6-4 Surface tension in void dynamics

Surface tension underfill (γ_L, liquid) (dym/cm)	Surface tension of acetic acid void (γ_G, gas) (dym/cm)	Surface tension between liquid and gas (γ_{LG}) (dym/cm)	Surface tension of eutectic solder (γ_S, solid) (dym/cm)	θ	S(θ)
20	100	30.557	440	20°	0.00267

The surface tension (γ_{LG}), geometric factor (S(θ)), and measured Gibbs free energy were used to determine the pressure difference (ΔP) between a void gas and liquid underfill from equation (6-16).

$$\Delta G^*_{het} = \frac{16\pi\gamma_{LG}{}^3}{3\Delta P^2} S(\theta) \tag{6-16}$$

where $$S(\theta) = \frac{(2+\cos\theta)(1-\cos\theta)^2}{4}$$

$$\Delta P = \sqrt{\frac{16\pi\gamma_{LG}{}^3}{3\Delta G^*_{het}} \times \frac{(2+\cos\theta)(1-\cos\theta)^2}{4}}\,.$$

All three parameters were plugged into equation (6-16) to determine pressure difference between a void gas and ambient. ΔP was 1995.8 KPa.

$$R_0 = \frac{2\gamma_{LG}}{P_G - P_L} = \frac{2\gamma_{LG}}{\Delta P} \tag{6-17}$$

Finally, the equation (6-17) determined the critical void size (R_0), 3.06×10^{-8} m, with surface tension and pressure difference. The molecular diameter of main source of the void (acetic acid) is 3.8×10^{-10} m. On the molecular diameter, the critical void size was reasonably calculated. The critical size would be used for an initial condition for a void growth model.

6.3.2 Void Dynamics Mathematical Formulation and Simulation

Consider the growth of a single spherical gas void surrounded by a liquidus underfill of infinite extent. The void was nucleated with thermal energy provided around a molten solder during reflow process as described in Chapter 3. The solder wetting process exhibits endothermic reaction as measured in Chapter 4. The temperature of a system would be constant. Thus, the entire system could be assumed to be isothermal for a void growth model. Mass diffusion is governed by Ficks' Law with a constant diffusivity, D. It should be noted that the mass diffusivity can be a strong function of concentration in

some polymeric systems [43, 91]. The diffusivity of void source gases into underfill could be calculated by appendix B.

Three governing equations were transformed into non-dimensional form to avoid numerical instability which can be induced in computation. Indeed, the micro size voids nucleated at high pressure. The bubble size was calculated by dividing the pressure by the very small bubble size close to zero. Consequently, the solution could be unstable. Non-dimensional analysis was applied prevent the instability of solution in computation. Therefore, time scale and length scale were transformed using, R_0^2/D, and R_0 respectively [41]. Afterwards, these three non-dimensional governing equations were solved simultaneously using the Runge Kutta method. The initial pressure is reduced to ambient pressure outside the voids, hence the voids will grow instantly.

6.3.2.1 Momentum equation

Eventually, governing equation (6-18) is transformed into dimensionless form, equation (6-19). Super script * note a dimension less form.

$$\rho_L\left(\frac{3}{2}\dot{R}^2+R\ddot{R}\right)=-\frac{4\mu_L\dot{R}}{R}+\left(P_G-P_L-\frac{2\gamma_{LG}}{R}\right) \quad \text{I.C:} \quad R(0)=R_0,\dot{R}(0)=0 \qquad (6\text{-}18)$$

$$\mathrm{Re}\left(\frac{3}{2}\dot{R}^{*2}+R^*\ddot{R}^*\right)=-4\left(\frac{\dot{R}^*}{R^*}\right)+\left(P_G^*-P_L^*-\frac{1}{Ca}\frac{2}{R^*}\right) \quad \text{I.C:} \quad R^*(0)=1,\dot{R}^*(0)=0 \qquad (6\text{-}19)$$

The dimensionless numbers follow:

$$R^*=R/R_0,\ P_G^*=\frac{P_GR_0^2}{\mu_LD},\ P_L^*=\frac{P_LR_0^2}{\mu_LD},\ Ca=\frac{\mu_LD}{\gamma_{LG}R_0},\ \text{and}\ \mathrm{Re}=\frac{\rho_LD}{\mu_L}. \qquad (6\text{-}20)$$

The model constants were given from the nucleation model and literature review in the heterogeneous void nucleation and growth. The pressure difference (ΔP=1995.828 KPa) between inside the void in gas phase (P_G) and outside the void in liquid underfill ($P_L \approx P_{ambient}$) was calculated using heterogeneous nucleation experiments. The experimental study also calculated initial conditions determined at the critical point of a void nucleation (R_0: 3.06×10^{-8} m) because a nucleated void will be stable and grow to macro dimension. In addition, the surface energy, γ_{LG}, between a gas and a liquid was determined as described in Table 6-4 [88, 89]. No-flow underfill data sheet determined viscosity ($\mu_L=0.001Pa\cdot s$) and density ($\rho_L=1680kg/m^3$) [92]. A diffusion coefficient (D) of an acetic acid gas into underfill was calculated as $1.421\times10^{-9}m^2/s^2$ as according to Appendix B [70, 71].

6.3.2.2 Gas Diffusion equation

$$\frac{\partial c}{\partial t}+v_r\frac{\partial c}{\partial r}=\frac{1}{r^2}\frac{\partial}{\partial r}\left(r^2 D\frac{\partial c}{\partial r}\right) \quad \text{B.C:} \quad c(r,0)=c_0 \quad \text{I.C:} \quad c\left(\infty,t\right)=c_0\,,c\left(R,t\right)=K_H P_G\left(t\right) \tag{6-21}$$

$$\frac{\partial c^*}{\partial t^*}+v_r^*\frac{\partial c^*}{\partial r^*}=\frac{1}{r^{*2}}\frac{\partial}{\partial r^*}\left(r^{*2}\frac{\partial c^*}{\partial r^*}\right) \quad \text{B.C:} \quad c^*(r,0)=1 \quad \text{I.C:} \quad c^*\left(\infty,t^*\right)=1\,,c^*\left(R^*,t^*\right)=K_H^* P_G^*\left(t^*\right) \tag{6-22}$$

where $v_r^*=\frac{R^{*2}\dot{R}^*}{r^{*2}}$, $t^*=t/\frac{R_0{}^2}{D}$, $r^*=\frac{r}{r_0}$, $c^*=\frac{c}{c_0}$, and $K_H{}^*=K_H\mu_L D/(c_0 R_0{}^2)$. c is the gas concentration in the depleted region of a gas outside a void. This governing equation is subject to initial and boundary conditions. These conditions were determined at the void interface using Henry's law. As according to the law, the gas concentration in a liquid is proportional to the pressure of that gas above the liquid. Namely, the gas concentration, c, is equal to the product of Henry's law constant, K_H, and gas pressure, P_G. To track the transient computational domain of a void growth, a Lagrangian coordinate transformation was applied to simulation. The infinite region was necessarily to provide more accurate representation of the void diffusion and convention equation because the void growth was induced from finite size to the infinite size. Namely, the moving boundary of void growth needs to be considered in the infinite region. Therefore, a transformation was applied to infinite region as suggested by Duda et al [91]. Their transformation for the moving boundary is $y=1-\exp\left[-\alpha\left(\frac{r^*}{R_0^*}-1\right)\right]$, which converts equation (6-21) for $R_0^*\le r^*\le\infty$ into (6-22) for $0\le y\le 1$. The constant α controls the spatial coordinate which used 0.3 for this simulation [46]. The coarse (α=0.3) still achieve the high accuracy of a void growth in elastic-polymer on the previous study. Therefore, coarse mesh was adapted due to computation speed.

$$\frac{R^{*2}}{(1-y)\alpha}\frac{\partial c^*}{\partial t^*}+\frac{\dot{R}^* R^*}{\left[1-\frac{\ln(1-y)}{\alpha}\right]^2}\frac{\partial c^*}{\partial r^*}$$

$$=\frac{2}{\left[1-\frac{\ln(1-y)}{\alpha}\right]}\frac{\partial c^*}{\partial r^*}+(1-y)\alpha\frac{\partial^2 c^*}{\partial t^{*2}} \tag{6-23}$$

6.3.2.3 Mass balance for gas in a void

$$\frac{d}{dt}\left(P_G R^3\right) = 3\rho_L D R^2 \left.\frac{\partial c}{\partial r}\right|_{r=R} \tag{6-24}$$

$$\frac{d}{dt}\left(P_G^* R^{*3}\right) = \frac{3}{A^* K_H{}^*} R^{*2} \left.\frac{\partial c^*}{\partial r^*}\right|_{r^*=R^*} \tag{6-25}$$

where $P_G^* = \frac{P_G R_0^2}{\mu_L D}$, $A^*=A/K_H$, $A = M/\mathbf{R}T$ and $K_H^*=K_H\mu_L D/(c_0 R_0{}^2)$. M is the molecular weight of a gas. **R** is ideal gas constant and T is temperature. This void growth model was examined at 200°C. The derivative of equation (6-25) in dimensionless form was taken as function of time, yielding equation (6-26).

$$\dot{P}_G^* R^{*3} + P_G^* 3\dot{R}^* R^{*2} = \frac{3}{A^* K_H{}^*} R^{*2} \left.\frac{\partial c^*}{\partial r^*}\right|_{r^*=R^*} \qquad \text{I.C:} \quad P_G^*(0) = P_{G0}^* \tag{6-26}$$

where $\left.\frac{\partial c^*}{\partial r^*}\right|_{r=R} = \frac{\alpha(1-y)}{R_0^*} \left.\frac{\partial c^*}{\partial y}\right|_{y=0}$, governed by diffusion equation and derived from $y = 1 - \exp\left[-\alpha\left(\frac{r^*}{R_0^*} - 1\right)\right]$. The y ranged from 0 to 1 with control constant, α=0.3 for this simulation.

6.4 EXPERIMENTAL APPORACH FOR MODEL VALIDATION

Heterogeneous void nucleation (see Chapter 6.3.1), Henry's law constant model (see Appendix B), Diffusivity model (see Appendix C), and literature review determined the initial conditions and model constants as described in Table 6-5.

Table 6-5 Initial condition and model constants for a void growth

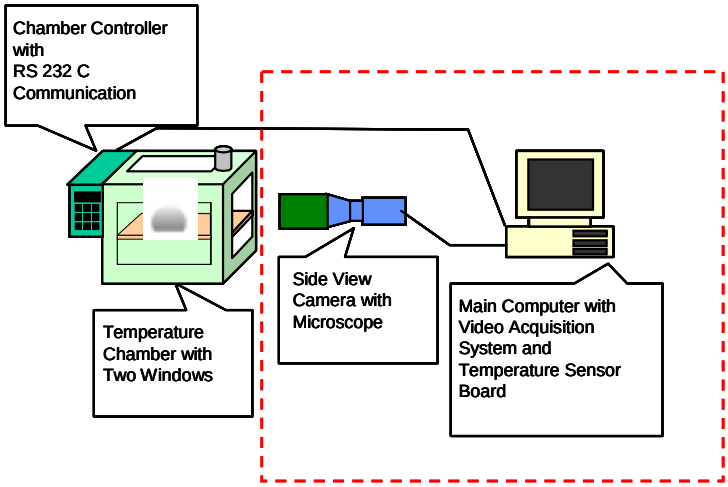
Temperature	200°C
Surface tension (γ_{LG})	*30.557 dym/cm*[88, 89]
Underfill viscosity (μ_L)	*0.001Pa·s*[92]
Underfill density (ρ_L)	*1680kg/m*^{3}[92]
Diffusivity of carboxylic acid (D)	1.421×10^{-9}m^2/s (Appendix B)
Thermal conductivity of underfill (K)	0.18*1000 m^2·kg/K·s^3[92]
Henry's law constant of acetic acid (K_H)	$3.253\times10^{-5}\ s^2/m^2$ (Appendix C)
Pressure in change between gas and liquid (ΔP)	*1995.828KPa* (Nucleation experiment)
Critical radius of void (R_0)	$3.062\times10^{-2}\mu m$ (Nucleation experiment)

With above given constants, Figure 6-6 describes the non-dimensional governing equations for numerical analysis. The growth models predicted the size of the voids as a function of time. Then, the size of the voids was measured to validate the accuracy of the void growth models using a high speed camera technique as shown in Figure 6-6. The camera technique is capable of capturing 1,000 frames per second. The resolution was 640x512 pixels with 7X magnification. The experimental setup consists of a temperature

chamber and a video monitoring system. The experimental setup is illustrated schematically in Figure 6-8-(a).

Table 6-6 Overview of dimensionless analysis

Conversion factor	$K_H^* = \frac{K_H \mu_L D}{c_0 R_0^2}$, $v^* = \frac{R^{*2}\dot{R}^*}{r^{*2}}$, $A^* = \frac{A}{K_H}$, $P^* = \frac{PR_0^2}{\mu_L D}$, $t^* = t / \frac{R_0^{\ 2}}{D}$, $R^* = R / R_0$, $r^* = \frac{r}{r_0}$ and $c^* = \frac{c}{c_0}$
Momentum equation	$\mathrm{Re}\left(\frac{3}{2}\dot{R}^{*2} + R^*\ddot{R}^*\right) = -4\left(\frac{\dot{R}^*}{R^*}\right) + \left(P_G^* - P_L^* - \frac{1}{Ca}\frac{2}{R^*}\right)$
Diffusion equation	$\frac{\partial c^*}{\partial t^*} + v_r^* \frac{\partial c^*}{\partial r^*} = \frac{1}{r^{*2}} \frac{\partial}{\partial r^*}\left(r^{*2} \frac{\partial c^*}{\partial r^*}\right)$
Mass balance for gas	$\frac{d}{dt}\left(P_G^* R^{*3}\right) = \frac{3}{A^* K_H^*} R^{*2} \left.\frac{\partial c^*}{\partial r^*}\right\|_{r^*=R^*}$
Dimensionless number	$Ca = \frac{\mu D}{\gamma_{LG} R_0}$ and $\mathrm{Re} = \frac{\rho D}{\mu}$



(a)

(b)

Figure 6-6 (a) Schematic of a high speed camera configuration and (b) high speed camera configuration (source: [11])

First, a test vehicle (see Figure 6-3) was placed in a programmable temperature chamber. Then, the chamber was immediately heated up to 200°C from room temperature. The isothermal condition was maintained within ± 0.1 °C. Once the TV reached temperature above eutectic solder melting point, the solders on the TV were

reflowed. During the wetting process, voids were nucleated and grew to macro size on the molten solders. The voids nucleation and growth were recorded using a Redlake PCI-2000 color high speed camera technique. The recorded images were transferred on Photoshop to measure the radius of a void as a function of time. These described experiments were conducted with six replicates.

6.5 EXPERIMENTAL RESULTS

The recorded images were transferred on Photoshop to measure the radius of a void as a function of time as shown in Figure 6-7. On the Figure, two voids were observed on the molten solder and the diameter of a void at 120 milliseconds was 9 cm on the Photoshop. 1 cm on the Photoshop corresponds to 21.987 μm in actual size for Exp 1, 2, 3, and 4. Exp 5 and Exp 6 used the scaling factor converting 1cm to 25.4 μm. Thus, the 4.5 cm of a void radius could be 98.534 μm.

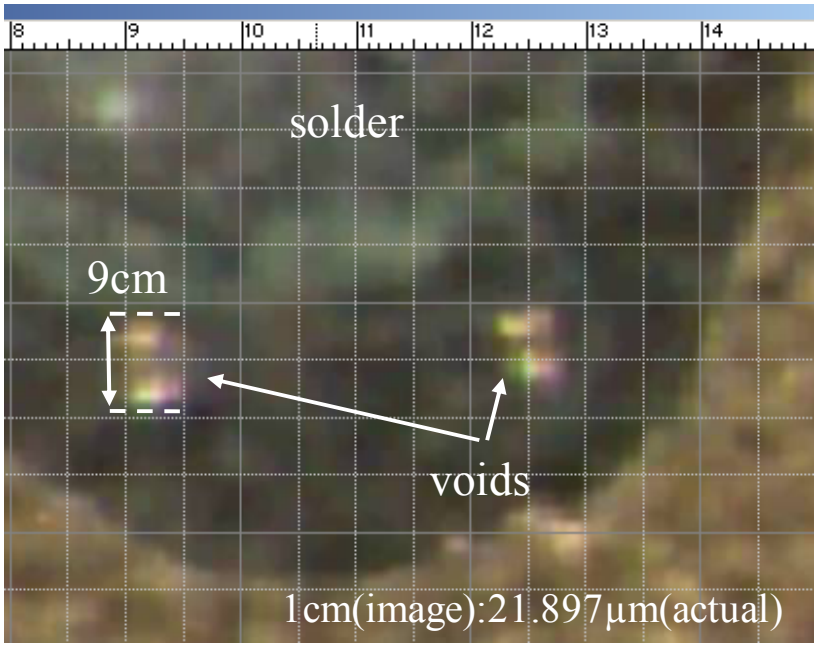


Figure 6-7 Measured radius of Exp 2 void on Photoshop at 120 milliseconds

Using the high speed camera technique, Figure 6-8 shows void growth as a function of time at 200 °C. Two voids were nucleated on the surface of a molten solder after solder wetting as shown in Figure 6-8-(b) at 27 milliseconds. The voids nucleated grew instantly.

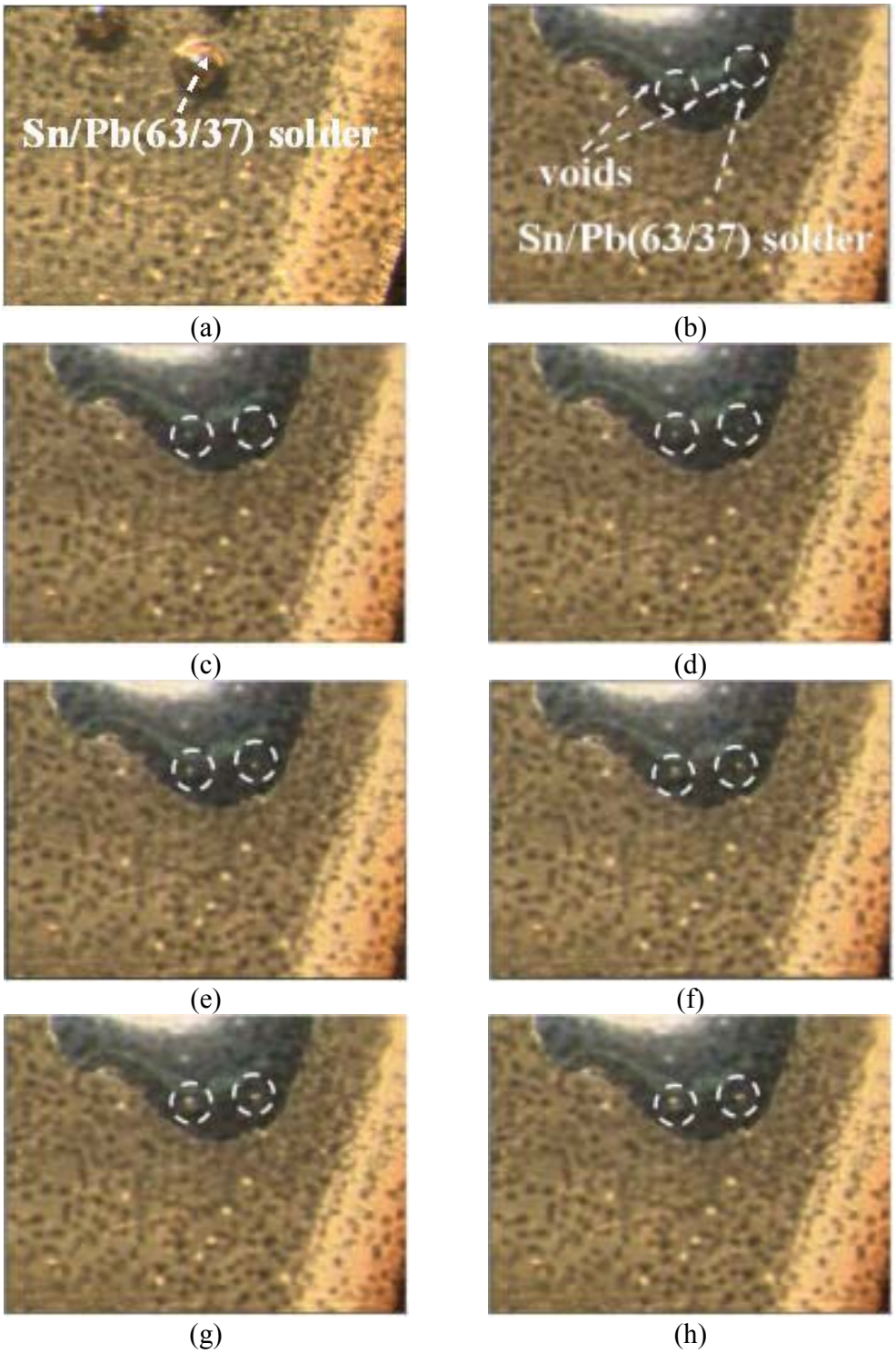


Figure 6-8 Micrographs of void growth on the surface during a solder reflowed at 200°C : (a) 0 millisecond, (b) 27, (c) 33, (d) 40, (e) 53,(f)73 (g)93, and (h) 100

These described experiments were conducted with six replicates as collected in Table 6-7.

Table 6-7 Measured radius of a void from experiments using high speed technique

Sec	image radius (cm)		actual radius (μm)		Sec	image radius (cm)		actual radius (μm)		Sec	image radius (cm)		actual radius (μm)	
	Exp1	Exp2	Exp1	Exp2		Exp3	Exp4	Exp3	Exp4		Exp5	Exp6	Exp5	Exp6
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0.02	0.75	0.85	16.422	18.612	0.013	0.85	0.60	18.612	13.137	0.027	0.91	1.00	23.495	25.4
0.027	0.85	0.90	18.612	19.706	0.04	1.25	1.15	27.37	25.181	0.047	1.40	1.25	35.56	31.75
0.033	1.1	1.15	24.086	25.181	0.06	1.65	1.65	36.129	36.129	0.067	1.60	1.50	40.64	38.10
0.04	1.15	1.25	25.181	27.370	0.08	1.9	1.85	41.603	40.508	0.087	1.85	1.78	46.99	45.085
0.053	1.2	1.31	26.275	29.012	0.093	2.5	2.5	54.741	54.741	0.17	2.50	2.00	63.50	50.80
0.073	1.65	1.75	36.129	38.318	0.107	3.1	3.75	67.879	82.112					
0.093	2.35	2.5	51.459	54.741										
0.1	2.65	3.05	58.025	66.784										
0.12	3.6	4.5	78.827	98.534										

Figure 6-9 presents a small discrepancy between the void growth model and experimental results. Due to the limitation of experiments, the pressure change in gas was calculated using simulation (see Figure 6-10). Consequently, Figure 6-9 and Figure 6-10 predict the size of a gas growth and the pressure change of the gas using classical bubble dynamics models. Once a void is nucleated, the void instantly grew with a rapid drop of pressure. Simultaneously, the pressure change inside a void is abruptly reduced as shown in Figure 6-10. Thus, void growth models were developed to predict the dynamic behavior of voids.

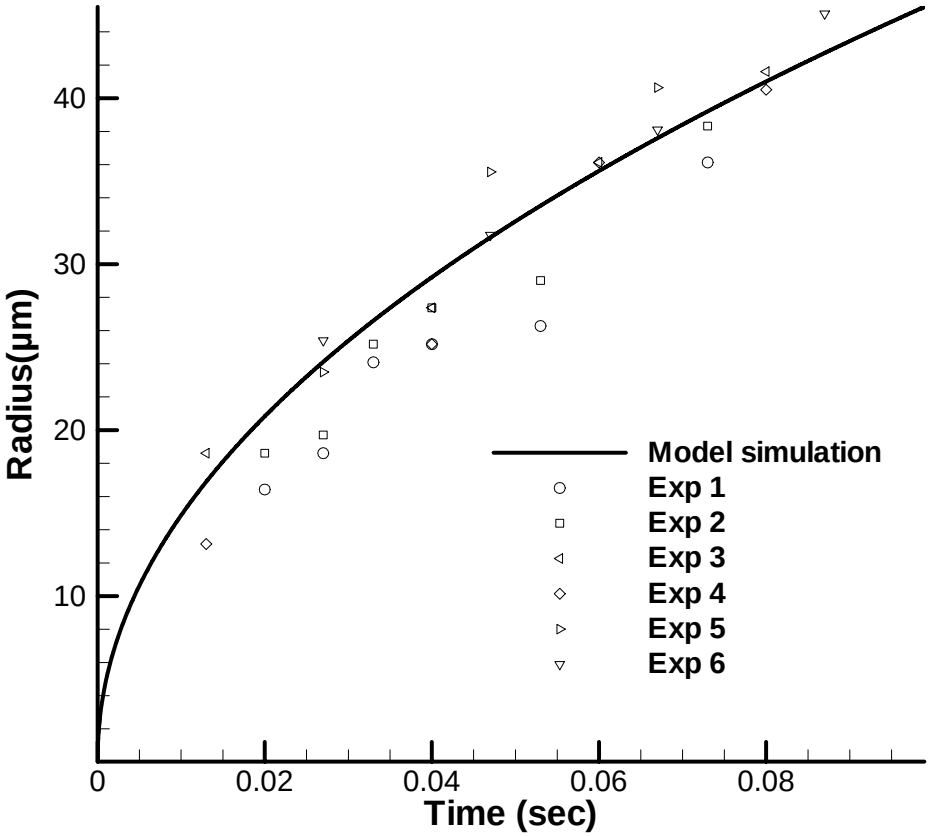


Figure 6-9 Comparison of size of void growth model simulation and experimental data

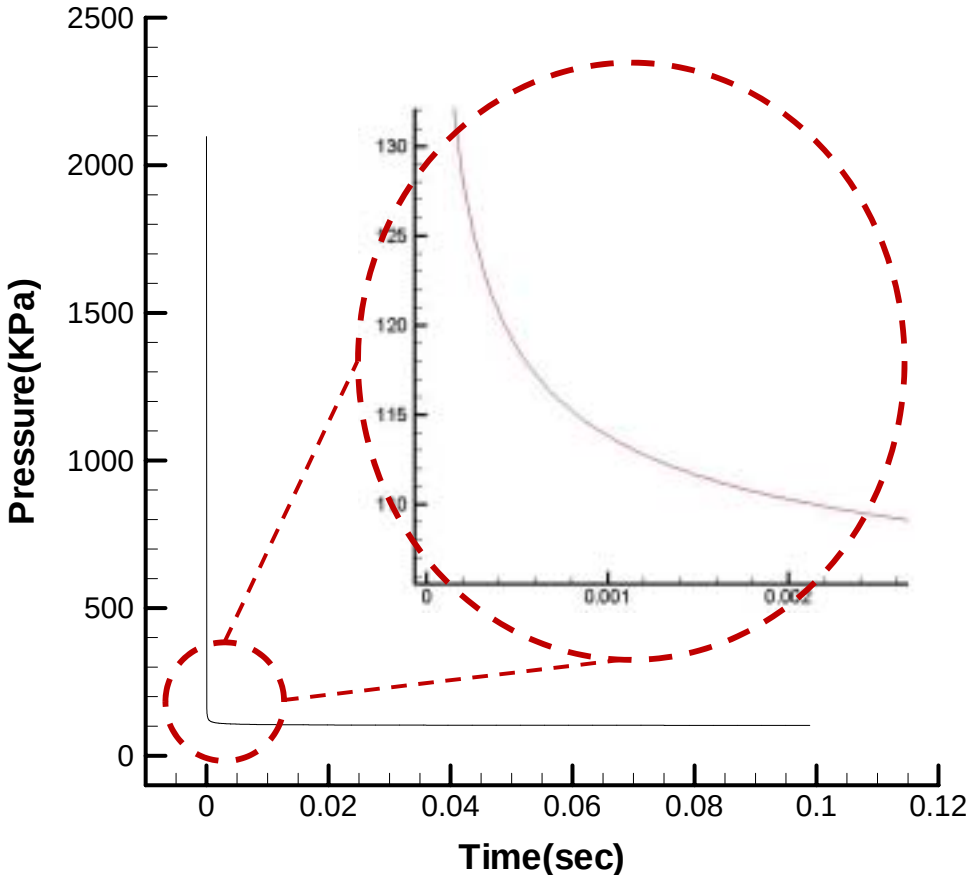


Figure 6-10 Prediction of pressure inside void by a model simulation

6.6 DISCUSSION AND CONCLUSIONS

The void nucleation model could measure the critical condition, at which voids nucleate and grow. The void size at critical condition, R_0, was used for a void growth model. Super script * note a dimension less form.

$$\rho\left(\frac{3}{2}\dot{R}^2 + R\ddot{R}\right) = -\frac{4\mu\dot{R}}{R} + \left(P_G - P_L - \frac{2\gamma_{LG}}{R}\right) \qquad R(0) = R_0, \dot{R}(0) = 0$$

$$\mathrm{Re}\left(\frac{3}{2}\dot{R}^{*2} + R^*\ddot{R}^*\right) = -4\left(\frac{\dot{R}^*}{R^*}\right) + \left(P_G^* - P_L^* - \frac{1}{Ca}\frac{2}{R^*}\right)$$

where $R^* = R/R_0$, $P_G^* = \frac{P_G R_0^2}{\mu_L D}$, $P_L^* = \frac{P_L R_0^2}{\mu_L D}$, $Ca = \frac{\mu_L D}{\gamma_{LG} R_0}$, and $\mathrm{Re} = \frac{\rho_L D}{\mu_L}$. On the equation, a significant factor affecting the rate of a void growth is the pressure of a void, P_G. High pressure can cause rapid void growth. The void growth model could predict the dynamic behavior as a function of time at certain temperatures with good agreement between experimentally measurement and theoretical prediction as shown in Figure 6-9. The theoretical studies could predict the density of void nucleation and the radius of a growing void at specific temperature with a fair precision. The small discrepancy was inevitable due to the assumptions used for modeling and the limitations of experimental techniques.

Major assumptions were mostly made on the gas diffusion model. One of assumptions was that the void was surrounded by a liquid underfill of infinite extent that has a spherically uniform gas concentration and a uniform gas pressure. However, the gas concentration has a gradient at far distance from the growing void. The gradient of gas potentially affects gas diffusion, driving a void growth. In addition, gas concentration and diffusion equations were modeled on the assumption of a spherical uniformly distributed gas region. In reality, gas diffusion occurs locally on the interface between a molten

solder and no-flow underfill. As the results, the gas locally evolved might supply less gas source than spherically uniform gas concentration in the model. Consequently, the local region of gas diffusion and the non-spherical geometric shape of a void created small discrepancy between simulation and experiments. For these reasons, the measured radius of voids was typically smaller than predicted one.

Secondly, the interface of the gas void and liquid underfill was governed by Henry's law with thermodynamic equilibrium. At the void nucleation stage or after the void nucleated ceased to grow, the equilibrium is nearly achieved. During the process of the void growth, the system exhibits quasi-equilibrium. The non-equilibrium condition can induce substantial driving forces such as pressure change.

Similarly, the calculated diffusivity can contribute to some level of error in the void growth model (Appendix C). The diffusivity was could be calculated at certain temperature by determining E_D and D_0. These constants are dependent on the gas molecule and polymer system.

$$D = D_0 \exp\left(-E_D / RT\right)$$

where R is ideal gas constant and T is temperature. E_D is the activation energy required for the diffusion of a gas molecule into polymer. Therefore, the size of a gas molecule and the status of polymer determine the activation energy. The status polymer will be instantly changed around glass transition temperature. The activation energy of diffusivity calculated was calculated on the assumption of liquid polymer. However, the liquid polymer will cure by a cross-linking to each other polymer molecules in a void growth. Therefore, the diffusivity calculated in liquid might be bigger than actual

diffusivity in transition status. The a bit small diffusivity decreases the velocity of pressure change. The resulting pressure change decreases the growing velocity of a void.

$$\frac{\partial}{\partial t}\left(P_G R^3\right) = 3\rho_L D R^2 \left.\frac{\partial c}{\partial r}\right|_{r=R}.$$

This constant could be considered as a minor factor inducing error in modeling.

Review the limitation of the void growth model presented in this chapter. The developed void model has a limited capability of predicting the dynamic behavior of a single void in the assembly process. Particularly, heterogeneous nucleation model experiments found that temperatures above 200 °C induced a large number of voids. At the high temperature, the voids nucleated coalesced to grow with the effect of gas diffusion. The void growth is governed by the combined driving forces of the gas diffusion and voids coalescence. The dynamic behavior of a growing void by the effect combined with gas diffusion and voids coalescence is beyond the developed model's capability.

From the experimental results of heterogeneous void nucleation, the nucleation rate was approximately zero below 190 °C. The temperature range might not provide thermal energy to exceed the free energy required at critical point. Thus, voids nucleated were unstable and could not sustain growth. In similar, no voids were observed at below 190 °C in void formation characterization study 2 conducted in Chapter 5. The heterogeneous nucleation allows alternative methodology to control nucleation by creating significantly high density of nucleation sites using nano materials. The nano materials play a role of nucleation sties, subsequently dissipating thermal energy and gas

concentration on each site. Thus, nucleation site cannot produce a stable nucleation with insufficient free energy and gas supply.

CHAPTER 7

DESIGN GUIDELINES FOR VOID REDUCTION

7.1 INTRODUCTION

The research conducted in this thesis achieved a high yield, stable and void-free assembly process using no-flow with a high I/O, fine-pitch commercial flip chip. The process was established using experimental techniques and classical bubble theories. These studies eliminated a large number of voids using soak temperature, ranging from 120 to 130 °C, and 190 °C peak temperature while a high, stable assembly yields still was maintained. For the results presented, this chapter provides design guidelines to establish a high yield, stable and void-free assemblies using no-flow underfill for other applications.

7.2 ASSEMBLY PROCESS CHARACTERIZATION

On the suggested void formation mechanism, the typical soak temperature, 140 ~ 170 °C, might be higher than fluxing agent's boiling point in no-flow underfill during solder reflow process. The soak temperature was modified to supply the fluxing agent with a stable condition below its boiling temperature. Typically, the organic acid based fluxing agent will boil at around 120 °C. Chapter 5 decreased the void percent area from 64 % to 7 % using a low soak temperature, ranging 120 and 130 °C. The soak

temperature presented is applicable to establish a nearly void-free reflow process without modification regardless of application using no-flow underfill.

In contrast, peak temperature needs to be customized according to material properties used in applications due to solder wettability. Typically, the melting point of a solder material needs a careful consideration for the process design. Indeed, 190 °C peak temperature was optimized to enable eutectic solders (Sn/Pb-63/37) to melt without producing underfill voids. As according to solder materials, the peak temperature should be designed using parametric studies. The studies will explore several levels of peak temperatures at around melting point. Unless the levels of temperatures induce voids with robust wettability, the temperatures can be chosen for the peak temperature in assembly process.

Above described methodologies can design assembly process conditions. The stability of assembly process will be validated using a large scale of assemblies. Eventually, a high, stable yield, and void-free process can be established.

7.3 UNDERFILL MATERIAL CHARACTERIZATION

The underfill voids alternatively can be minimized by modifying the formulation of no-flow underfill on the classical bubble nucleation theory. For the void nucleation, the thermal energy provided should exceed the free energy required at critical point, ΔG^*_{het}. Then the void is stable and can grow to a macro size bubble. Below the critical free energy, nucleated void is unstable and can perish.

$$N_{het} = Cf \exp\left(\frac{-\Delta G^*_{het}}{kT}\right)$$

$$\Delta G^*_{het} = \frac{16\pi\gamma_{LG}{}^3}{3\Delta P^2} S(\theta) = \frac{16\pi\left(\gamma_{LS}-\gamma_{SG}\right)^3}{3\Delta P^2 \cos\theta^3} \times \frac{(2+\cos\theta)(1-\cos\theta)^2}{4}$$

On the heterogeneous nucleation theory, free energy required at critical point, ΔG^*_{het} is function of surface energy, pressure change between a gas and surrounding, and geometric effects, $S(\Theta)$. These constants can be used for the control parameters of void nucleation. To eliminate void nucleation in assembly process, the most efficient way is to increase the free energy required at critical point. The free energy required is increased higher than thermal energy provided from assembly process. Therefore, high pressure gradient between a void and surrounding, change of geometric factor, modification of surface energy are candidate to increase the free energy required preventing void nucleation. Among the candidates, a high pressure device could not be implemented due to cost and assembly process standpoint. Besides, the change of geometric factor depending contact angle between a solder and a void is beyond assembly process limits. Thus, Chapter 5 modified surface energy between a void and solid, γ_{SG}, to eliminate underfill voiding using no-flow underfill combined with nano particles. The particles increased significantly heterogeneous nucleation sites, subsequently dissipating the free energy below critical point. The resulting free energy made voids unstable. This mechanism was achieved with above three weight percent of 50nm aluminum oxide. Besides, the study found low surface energy material might be a potential candidate to minimize underfill voids.

For these studies, no-flow underfill can be formulated using low surface energy materials with a high weight percent regarding underfill voiding characteristics. The underfill formulated with nano particles might show an excellent performance to eliminate underfill voiding at high temperature. However, nano particles in the formulated underfill can interfere solder interconnections between solder bumps and pad

in assemblies like fillers. Even though the fillers can improve performance in the thermal reliability of no-flow assembly process, the no-flow underfill typically does not include fillers due to assemblies yield loss. The small particles, fillers, can prevent solder bumps from touching the pad, consequently causing I/O opening. For this reason, the effect of nano materials on assembly yields is highly required to be investigated for the future application.

CHAPTER 8

CONCLUSIONS

The void formation mechanism in flip chip assemblies using no-flow underfills was identified using experimental and theoretical studies. The fundamental studies indentified the primary source of void formation in the assembly process. The results suggested that the void formation mechanism was induced by a chemical reaction with thermal effect during the solder reflow process. A series of experiments found the optimal process achieving a high, stable yield and void-free assemblies. Then classical bubble nucleation and growth theories were applied to explain theoretically the void formation mechanism. On the theoretical studies, voids nucleated in the assembly process were controlled to minimize underfill voids by characterizing material formulation.

Indeed, initial results from the assembly process development have shown that new commercially developed no-flow underfills can provide robust yields in Flip Chip in Package applications. Moreover, these materials and the associated process technology have demonstrated robust interconnects in typical FCIP interconnect systems comprising high lead solder bumps with eutectic lead-tin solder interconnects, 150 μm pitch, and I/O counts in excess of 3000. Interconnect yields were found to be sensitive to reflow process parameters and specific to the underfill formulation. Reflow design parameters were determined to increase assembly yield using statistical analysis of the main effects on yield and failure analysis for each commercial underfill material.

First, the simple structured test vehicles were used to determine the best wetting conditions for high lead solder bump and lead-tin pad interconnect systems. The best wetting conditions achieved were used for the baseline of the pre-qualifying experiment

using low-cost FA10-4 flip chip packages to validate the process prior to the assembly process with high I/O, fine pitch flip chip in package (FCIP) coupled with a full area array structure. The validated assembly process was optimized to accomplish a high yield assembly process by investigating the effect of reflow parameters on electrical yield using high I/O, fine-pitch FCIP. Eventually, the high yield assembly process with a wide reflow process window was achieved with the FCIP. On the other hand, the high yield assembly process created a large number of voids on the FCIP device (see Figure 1-2). Actually, the large number of voids can be a critical defect that causes early failure in thermal reliability.

Void formation studies were conducted to investigate the plausible causes of no-flow underfill voiding with high I/O, fine pitch FCIP. The experimental study found a chemical reaction, oxidation reduction, for solder wetting, causing underfill voids. The oxidation reduction was conducted by a fluxing agent of no-flow underfill. The fluxing agent of no-flow underfill was suspected as the main source of void formation with thermal effect from the reflow process. On the void formation studies, a void mechanism was suggested to explain the void nucleation induced by the chemical reaction of the fluxing agent in the assembly process. The mechanism explained that the fluxing agent in no-flow underfill is exposed to temperatures above its boiling point in the soak zone, causing underfill voiding. The fluxing reaction created water vapor and carboxylic acid, which can vaporize at elevated temperature. Such gases evolved could induce underfill voiding. The mechanism of underfill voiding was validated using Gas-Chromatography and Mass-Spectrometry by identifying evolved gases.

A void reduction study was used to decrease the amount of underfill voiding using a parametric study with high assembly yield using a commercial no-flow underfill. The analysis identified that low soak temperature and high soaks time could decrease underfill voiding from 64% to 7%. An assembly characterization study investigated the effect of the peak temperature on the underfill voiding using experimental techniques. The series of experimental studies designed process conditions, achieving a high, stable yield and void-free assembly process regarding process stand point with a large scale of assemblies.

Furthermore, the commercial no-flow underfill was characterized for voiding and analyzed modified with nano particles on the classical heterogeneous theory. A heterogeneous nucleation needs excessive energy of required critical energy for stable void nucleation. Below the critical energy, voids nucleated will be unstable and disappear. The reformulated no-flow underfill with nano particles (3%, 50 nm aluminum oxide) distributed free energy below required energy, subsequently preventing voids nucleation in the assembly process.

The dynamic behavior of a void in the process was predicted using classical bubble mechanics. A void was nucleated on the interface of between a molten solder and a liquid underfill. Thus, heterogeneous nucleation was applied to the underfill voiding. Thus, number of voids was predicted at certain process condition. The voids nucleated grew instantly and the growth was driven by gas diffusion into a void from liquid underfill. The void growth model was developed to predict the dynamic behavior of a growing void in assembly process as following assumptions:

1. The system was a spherical gas void.
2. The system was isothermal.

3. The gas concentration was spherically symmetric.

4. Equilibrium existed at interface of the gas void and liquid underfill was governed by Henry's law.

5. The velocity field was purely radial and was spherically symmetric. Gravitational effects can be neglected.

6. The underfill liquid was an incompressible Newtonian fluid with constant density and viscosity.

7. The void was surrounded by a liquid underfill of infinite extent that has uniform gas concentration and uniform gas pressure. With these assumptions, the developed model achieved a fair agreement with between experimental results.

In conclusion, the fundamental study represents a significant achievement in flip chip assembly process using no-flow underfill. The study may apply to the industrial production of high I/O, fine-pitch flip chip using underfill material. Besides, the experimental and theoretical studies presented in this thesis provide design guidelines of commercialization of innovative no-flow underfill process and material to achieve a high, stable yield, and void-free assembly process in the near future.

CHAPTER 9

CONTRIBUTIONS AND FUTURE RECOMMENDATIONS

9.1 CONTRIBUTIONS

The following contributions were accomplished by conducting the study of void formation for the application of flip chip assembly process development in this thesis.

1. Developed the experimental setup and experimental method to achieve an assembly process using no-flow underfills with a commercial high I/O, fine pitch flip chip.

2. Investigated the plausible causes of void formation in flip chip assembly process using no-flow underfills.

3. Suggested a void formation mechanism based on a combined chemical reaction and the thermal effect from assembly process.

4. Identified the main chemical source of void formation induced by chemical reaction with thermal effect in the assembly process using no-flow underfills.

5. Investigated the effect of the reflow process on underfill voiding to minimize the amount of underfill voiding using experimental techniques.

6. Provided the design guideline for an assembly process to achieve a high yield and void-free assembly process.

7. Developed a void nucleation model and a dynamic void growth model that predicted the number of voids and the size of voids respectively. The developed model was validated using experimental techniques.

8. Developed a high, stable yield and void-free assembly process using a commercial no-flow underfill with a commercial high I/O, fine pitch flip chip package.

9.2 RECOMMENDED FUTURE WORK

Based on the research, three areas of future works are recommended. A major concern is to extend the material characterization study formulated with nano materials. A void-free assembly process was achieved with a high I/O counts and fine-pitch commercial flip chip using a no-flow underfill by modifying temperature conditions of reflow profile. Indeed, the void nucleation depends on the temperature, pressure, and material properties. Therefore, no-flow underfill material characterization investigated the effect of nano materials on underfill voiding. The voids can be eliminated by changing the underfill's formulation by modifying particle size, weight percent, and type of nano materials. As a consequence, aluminum oxide plays the role of potential nucleation sites, dissipating the free energy below the required energy and greatly increasing the number of nucleation sites, subsequently eliminating voids. On the contrary, bismuth particles could not distribute energy to eliminate the underfill voiding. While the studies conducted provides a reasonable understanding of the effect of nano material on voids, the mechanism of voiding nucleation with a nano particle do not yield reliable design guideline of assembly process using underfill material formulated with nano materials. Therefore, a future contribution can be made in this area using experiments and theoretical analysis.

Second, thermal reliability testing can be conducted to validate the high performance of developed assembly process in reliability. Actually, the reliability tests are in progress and are delayed due to the limitation of the number of commercial parts available.

In general, existing voids are widely known as a critical defect affecting the performance in the thermal reliability, causing solder fatigue cracking or solder bridge. However, a normally distributed micro-size of voids in an epoxy based material such as no-flow underfill might have the positive effect on assembly process. Thus, future studies can be also conducted to investigate the effects of voids size and density on thermal reliability and assembly process.

VITA

SANGIL LEE

Sangil Lee was born in Incheon, South Korea. He received his B.S. from the School of Mechanical Engineering from Inha University, South Korea in 2000. After that, he joined in Republic of Korea (ROK), Navy as an officer and served in ROK Navy Head Quarters and Ministry of Defense from 2000 to 2003 as an IT expert before coming to Georgia Tech. In 2005, he obtained a M.S. from Aerospace Engineering. Then he transferred to Mechanical Engineering to pursue a doctorate in electronics devices packaging area.

APPENDIX A

ASSEMBLY PROCESS DEVELOPMENT WITH HIGH I/O DENSITY AND FINE PITCH FLIP CHIP

A.1 INTRODUCTION

Next generation FCIP applications have high I/O counts coupled with finer pitch area array interconnect structures, and they present challenges for interconnect yield. Such challenges push conventional capillary flow underfill processing beyond its processing limits, precluding underfill of these next generation FCIP assemblies. Therefore, the test vehicles, flip chip in package (FCIP) with high I/O density, large chip size, and small interconnect pitch, are used for assembly process development. The process design parameters for improved assembly yields depend strongly on the underfill material's characteristics and particularly the reflow profile. A number of commercially developed no-flow underfills are evaluated to determine the thermal material characteristics in terms of interconnect yield. This chapter presents a methodology for evaluating new commercial no-flow underfill materials, techniques for establishing baseline reflow profiles for yielding FCIP devices, initial yield sensitivity analysis, and initial void sensitivity analysis for the FCIP assembly process.

A.2 EXPERIMENTAL APPROACH

This study evaluates no-flow underfills and their associated processing as an alternative to conventional capillary flow underfill processing. No-flow underfill processing utilizes fluxing underfills that are deposited onto the substrate before chip placement. The chip is placed into the underfill causing squeeze flow of the underfill material during placement. The assembled device is reflowed and cured simultaneously in a reflow oven [73]. Among the key assembly process control parameters for no-flow processing, the reflow profile is one of the most important factors in determining quality of interconnect wetting and yield and has a narrow feasible process window for interconnect yield. This Chapter presents a methodology for evaluating new commercial no-flow underfill materials, techniques for establishing baseline reflow profiles yielding FCIP devices, and initial yield and void sensitivity analysis for the FCIP assembly process.

Experimental analysis was conducted on fifteen commercially developed no-flow underfill materials. Materials were first screened for wetting and voiding performance. Baseline reflow profiles were then established for down selected underfills. Reflow profiles were then further optimized using eutectic lead-tin (Pb/36-Sn/63) area array flip chip test vehicles (FA10-4). Finally, a process yield analysis was conducted for a select set of no-flow underfills using a FCIP test vehicle.

Temperature limits of the materials initially were determined using thermal testing based on both conduction and convection heating techniques. Conduction and convection mode thermal testing provided insight into the thermal process limits of the materials as well as initial temperature ranges for robust solder wetting. The peak processing

temperature defined by the temperature at which outgassing occurs was also determined using thermal testing.

The reflow process, being one of the most important factors for wetting, was established by investigating the wetting and voiding characteristics of the materials to various thermal excitations using high lead solder spheres reflowed on a eutectic lead-tin coated surface.

Refinement of the reflow parameters was achieved using a eutectic solder bump area array flip chip test vehicle and analysis of the interconnect yield based on design of experiment techniques. Baseline reflow conditions for each no-flow underfill were determined from profiles providing the highest chip yield for eutectic solder flip chip test vehicles.

The ultimate goal of this study was to determine no-flow underfill process yields for FCIP assemblies which incorporate interconnect systems comparable to commercial microprocessor packages. These assemblies have high lead solder bumps and eutectic lead-tin solder caps on the substrate that provide the interconnect to the high lead solder bump. To this end, the baseline reflow profiles determined for the eutectic lead-tin flip chip test vehicles were further refined to yield high lead – eutectic solder cap FCIP test vehicle assemblies.

An assembly process for the FCIP described in Figure A-1 is established by executing several steps such as thermal testing, wetting study, and pre-qualifying assembly. The optimized reflow profiles from pre-qualifying assembly were then applied to the FCIP test vehicle assembly process using the best performing no-flow underfill materials.

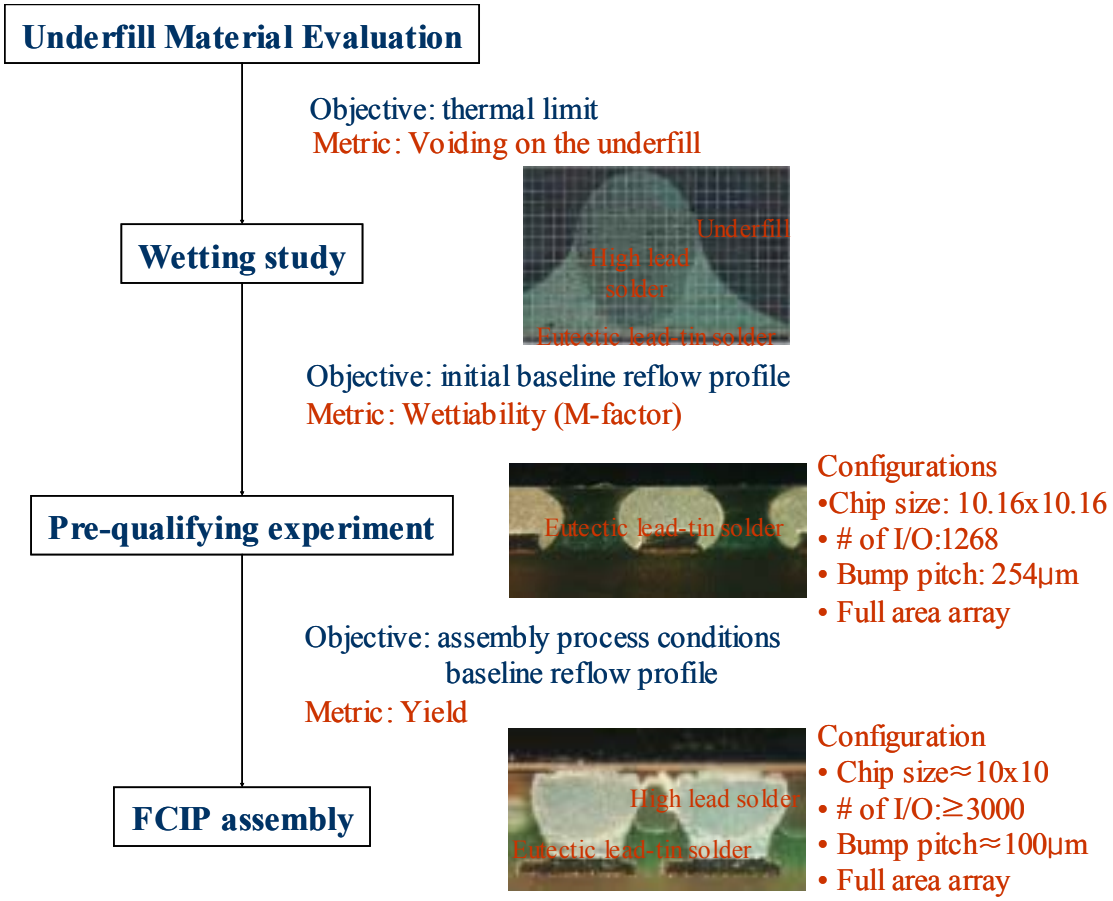


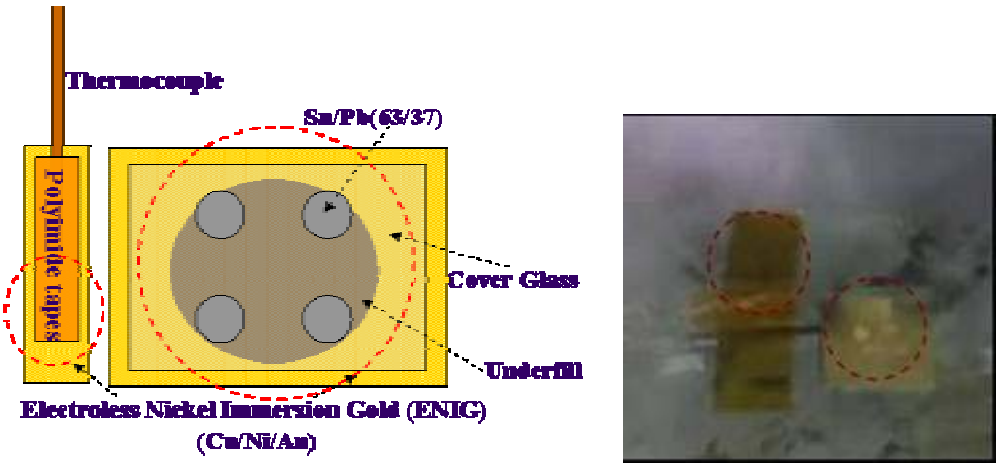
Figure A-1 Assembly process development procedures

A.2.1 Underfill Material Evaluation

The test vehicle consisted of a glass slide cover, four Sn/Pb(63/37) solder spheres, and an Electroless Nickel Immersion Gold (ENIG) plated substrate. Before assembly, a cleaning process using IPA was applied to test coupons and the test coupons were baked at 125°C for 3 hours to avoid out-gassing from moisture on the substrate. Four solder spheres were placed on the ENIG substrate and no-flow underfill was dispensed onto the substrate. The cover glass slide was put on top of the solder spheres on the underfill deposited ENIG substrate. This test vehicle illustrated in Figure A-2-(a) was used in both conduction mode and convection mode thermal tests.

A.2.1.1 Conduction Mode Thermal Test

A thermocouple attached to the ENIG substrate was used to measure the temperature of the TV relative to the hot plate. The hot plate was preheated to 100°C. Next, the test vehicle was placed next to a thermocouple coupon on the plate as illustrated in Figure A-2-(b).



(a) a typical configuration of test vehicle (b) on the hot plate

Figure A-2 Conduction mode equipment configuration

The test vehicle was placed on the hot plate and was observed under a microscope to determine the behavior of no-flow underfill material. The temperature was recorded when outgas voiding occurred in the underfill. The temperate at which outgassing occurs is defined as the peak temperature of the underfill material.

A.2.1.2 Convection Mode Test

To closely replicate the actual reflow process used in flip chip assembly, a convectional heating mode was used for the wetting and voiding study using a programmable convection oven (see Figure A-3). The convection thermal test enabled a more precise determination of the peak temperature of the underfill resulting in outgassing. The TV was then placed in a pre-heated hot chamber at 100°C in a high ramp rate convection oven used to simulate reflow conditions. The assembly was ramped to a maximum test temperature, and heated for one minute at constant temperature. Four maximum temperature levels were investigated in this test including 220/230/240/250°C. The test temperature at which outgassing voids occurred was recorded as the underfill peak temperature. Optical microscopy was used to inspect the test coupon to determine wetting quality and the extent of outgassing voids.

The convection oven used provided a ramp rate up to 100°C/min and a high temperature capability up to 350°C. All process functions and thermal profile functions of the chamber were PC controlled via RS 232 communication.

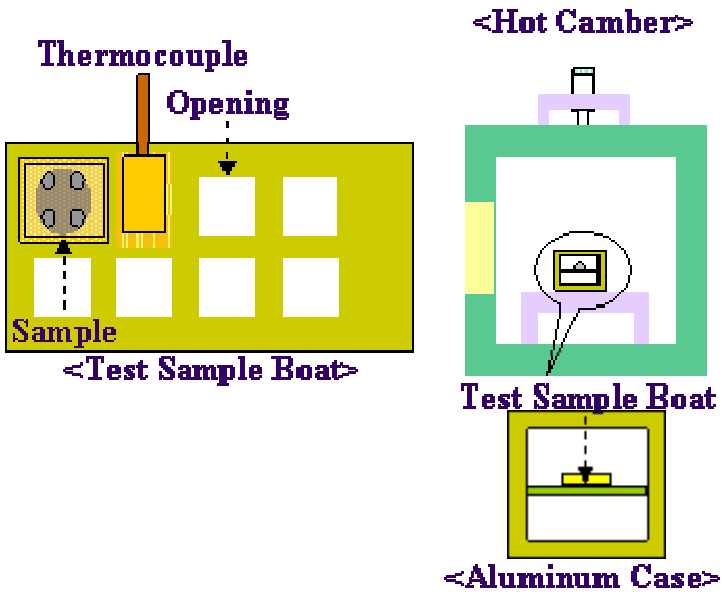


Figure A-3 Convection mode equipment configuration

A.2.2 High Lead and Eutectic Solder Wetting Study

With the thermal limits of the underfills determined, solder wetting studies were performed using test coupons consisting of eutectic solder coated substrates, high lead solder spheres, and no-flow underfill deposits encapsulating the solder spheres. This test method was used to determine initial baseline reflow profiles for each no flow underfill material. This test method was adopted from the work of Milner et al. [3].

A one inch square copper laminated substrate was coated with eutectic lead-tin solder (~50 μm thick) as shown in Figure A-4. A high lead solder sphere (90 Pb/10 Sn solder sphere with a 406.5μm diameter) was placed on the solder coupon with a dispensed no-flow underfill. The assembled coupons were passed through a convection reflow oven under a controlled thermal profile.

The reflow profiles used in this testing were designed as parametric experiments analyzing the main effects of reflow profile parameter variations on wetting performance for each no-flow underfill material. The reflow profiles were based on the general step profile. Table A-1 shows the reflow parameter settings used for the parametric wetting study. Parameter levels were based on the observations from the conduction and convection thermal test experiments.

Table A-1 Parameters variations matrix for wetting study

Material	Parameter	Level 1	Level 2	Level 3
Underfill A~E	Ramp Rate	0.4°C/s	0.8 °C/s	1.2 °C/s
	Peak Temperature	210 °C	220 °C	235 °C
	Time > 183 °C	60 s	70 s	80 s
	Soak Time	90 s	90 s	90 s
Underfill 1~2	Ramp Rate	1.0 °C/s	1.5 °C/s	2.35 °C/s
	Peak Temperature	210 °C	225 °C	240 °C
	Time > 183 °C	50 s	65 s	80s
	Soak Time	60 s	120 s	180 s

The primary goal of this study was to determine the main effects of reflow profile variations on wetting of Sn/Pb(63/37) solder to a high lead sphere. The setup was a basic configuration of a high lead solder bump mounted to a eutectic cap substrate as is often used in FCIP interconnects systems. A wetting parameter was used to quantify the degree of solder wetting observed in cross sections of the wetted spheres. The wetting parameter was defined as a combination of the fractional height of solder that wetted up the side of the high lead bump multiplied by with the fractional area of solder diffused into the high lead bump. The equation defined for the wetting response was based upon percent ratios of solder fillet rise and solder area diffusion as shown in Figure A-4. These ratios were multiplied together to give a single response measurement of overall solder wetting for each test case. Three replicates were performed for each reflow profile defined in

Table A-1. The wetting parameter was defined by the M-factor of Figure A-4. The best reflow profile conditions were chosen through this parametric study for pre-qualifying assembly of eutectic solder bump area array flip chip test vehicles.

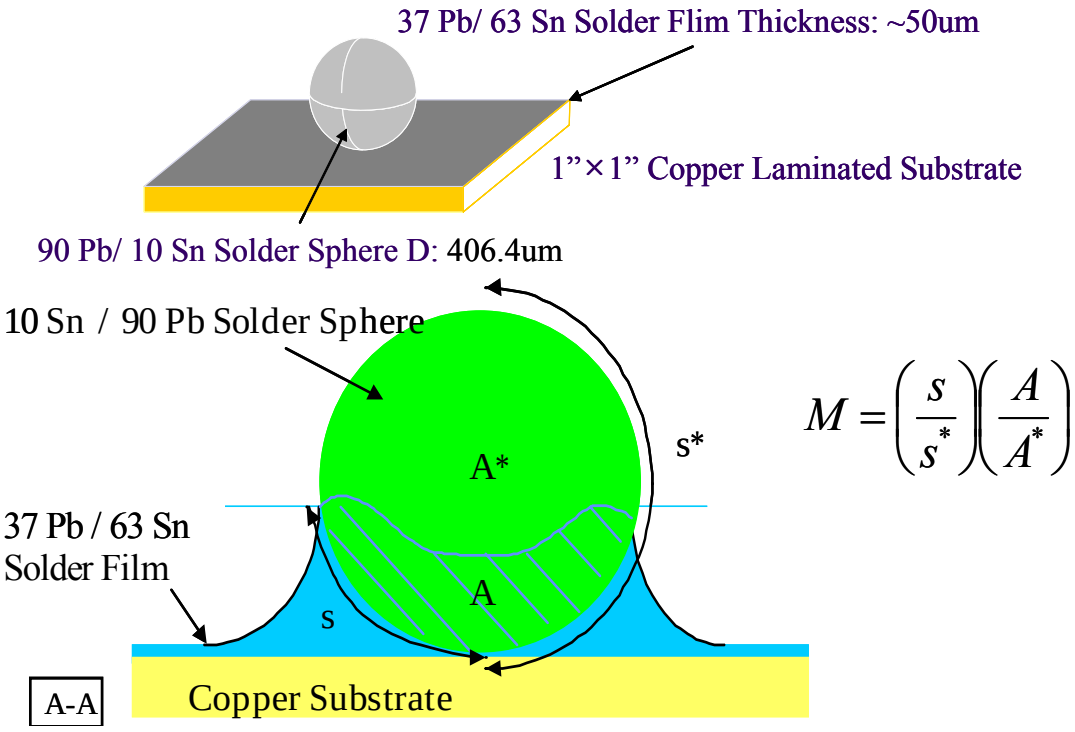


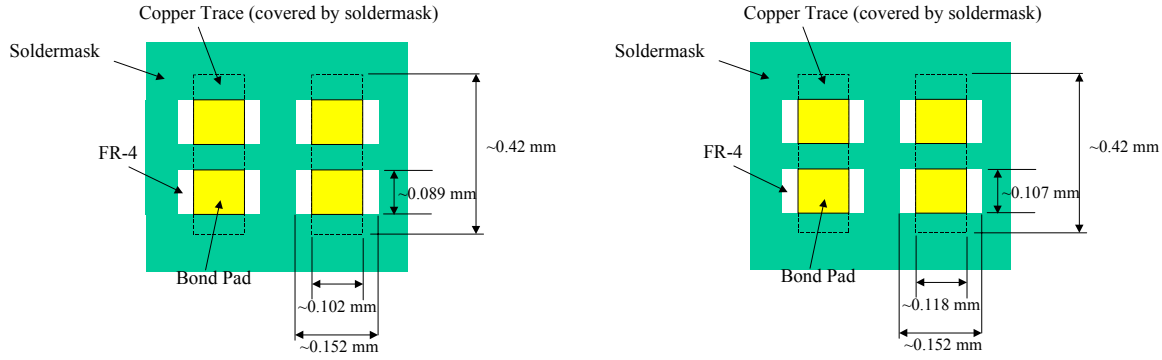
Figure A-4 Defined wetting parameters[3]

A.2.3 Pre-qualifying Assembly Using Lead-Tin Flip Chip Test Vehicles (FA10)

The FA10-4 chip (Table A-2) was 10.16 x 10.16 mm and had 1268 interconnects at a bump to bump pitch of 254µm. The bond pad metallization shown in Figure A-5 consisted of 0.034 mm of copper, 4.3mm of electroplated Nickel, and an immersion gold layer 0.05 to 0.30 mm thick. The solder mask design (Figure A-5) consisted of rectangular solder mask openings, which produced rectangular bond pads.

Table A-2 Test chip characteristics

Chip Type	Chip Size (mm)	Bump Count	Bump Pitch	Bump Height	Bump Layout
FA10-2	5.08 x 5.08	317	254 µm	110 µm	Full area array
FA10-4	10.16x10.16	1268	254 µm	110 µm	Full area array



FA10-2 FA10-4

Source: Ryan Thrope Masters' Thesis

Figure A-5 Solder mask design

The baseline reflow profile found from the high lead and eutectic solder wetting study was further refined by a pre-qualifying flip chip assembly using eutectic solder bump area array flip chip test vehicles (FA10-4).

A FA10-4 test vehicle was used for all assemblies. Prior to assembly, the substrates were cleaned and baked out at 125 ºC for 3 hours. The boards were stored in a nitrogen desiccant chamber after bakeout for no more than 2 hours before assembly. The test vehicles for each process condition were assembled according to the hybrid no-flow process flow in Figure A-6 (see reference[17]). After assembly, the boards were analyzed using acoustic microscopy, x-ray, and cross sectioning.

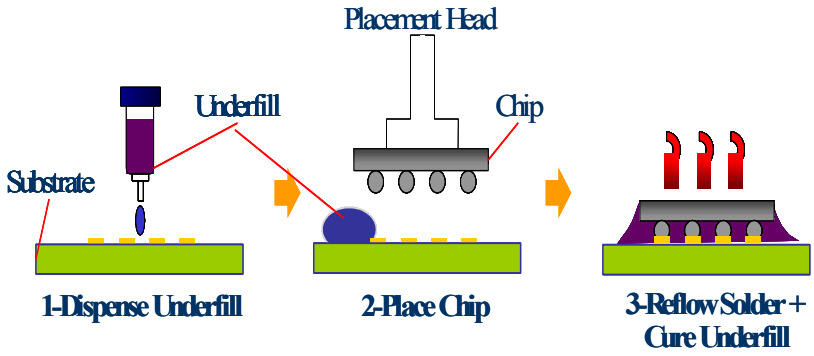


Figure A-6 Schematic of hybrid no-flow assembly process

The test vehicle consisted of an area array flip chip mounted on a high Tg FR-4 substrate with ten bond sites. The test chips were supplied by Flip Chip International and had daisy chain test structures. The FA10-4 chip was a 10.16 x 10.16 mm full area array and had 1268 eutectic lead-tin solder interconnects at a bump pitch of 254μm. The substrate bond pad metallization consisted of Cu, electroplated Ni, and immersion Au. There are probe points on the board that enable continuity testing of full columns of interconnects.

The assembly parameters used for test vehicle assembly were 23mg of no-flow underfill, a dot underfill dispense pattern, a placement force of 10N, and a placement dwell time of 2sec.

A.2.4 Assembly Process Development with High I/O, Fine-Pitch Flip Chip

The optimized reflow profiles were then applied to the FCIP test vehicle assembly process using the best performing no-flow underfill materials. The FCIP test vehicle consisted of a full area array flip chip mounted on a high Tg, organic substrate. The FCIP flip chip devices had high I/O counts (over 3000 I/O) and fine pitch (down to 150 μm). The flip chip devices consisted of high lead solder bumps and the organic substrates had flip chip bond pads capped with eutectic lead-tin solder.

Prior to assembly the boards were baked out at 125 ºC for 3 hours and were cleaned using a pure argon gas for 10 min. All other assembly procedures followed the process flow used in the pre-qualifying assembly of the FA10-4 test vehicles. The assembly process design parameters were 17mg of no-flow underfill, a dot underfill dispense pattern, a placement force of 10N, and a placement dwell time of 3 sec. After assembly, the parts were analyzed using acoustic microscopy, x-ray, cross sectioning and SEM.

Table A-3 Flip chip in package configuration

Bump material	Chip size (mm)	Bump count	Bump pitch	Radius of solder	Bump layout
97Pb-3Sn	10 x 10>	3000>	<200μm	<100μm	Full area array

The design of experiments process described in Table A-4 was used in order to determine the assembly process window with FCIP using no-flow underfills. The FCIP was assembled according to this DOE using hybrid no-flow assembly technology. The hybrid no-flow assembly technology developed by hybrid no-flow process [1, 16, 17, 24, 73] was applied to the FCIP assembly process described in Table A-4 with DOE. Reflow parameters of the DOE have about a 20% margin between level 1 and level 2,

but a ramp rate of 10 % between level 1 and level 2 in DOE. The electrical interconnection used as a metric determined assembly yield. Finally, the main effect of reflow parameters on assembly yield was analyzed using statistically.

Table A-4 Design of experiment for FCIP assembly

Run Order	Ramp rate	Soak time	Reflow time	Peak temp
1,2	Level 1	Level 1	Level 1	Level 1
3,4	Level 2	Level 1	Level 2	Level 1
5,6	Level 1	Level 1	Level 2	Level 2
7,8	Level 2	Level 1	Level 1	Level 2
9,10	Level 2	Level 2	Level 1	Level 1
11,12	Level 1	Level 2	Level 2	Level 1
13,14	Level 1	Level 2	Level 1	Level 2
15,16	Level 2	Level 2	Level 2	Level 2
Total Builds	16			

In addition, conservative process parameters (Table A-5) were chosen to achieve a high yield assembly process using no-flow underfills from the existing literature.

Table A-5 FCIP assembly conditions

Plasma cleaning	Board baking	Placement force	Placement dwell time	Dispense pattern	Dispense underfill amount
Argon, 10 min	3 hour @ 125 °C	10N	3 sec	Dot dispense	17±0.5mg

Consequently, good yield processes were achieved using four different no-flow underfills. The no-flow underfills obtained a high quality of interconnection in FCIP with

the current high yield assembly process, and multiple voids can be detected among the solder interconnections in the cross-section image (see Figure 1-2-(b)). The large number of voids was also detected as shown in Figure 1-2-(c) due to high values in reflow parameters using C-SAM analysis.

A.3 EXPERIMENTAL RESULTS

A.3.1 Underfill Material Evaluation

The objective of the material evaluation experiments was to investigate the temperature range and limits of the no-flow underfill materials. The peak temperature of each no-flow underfill was collected based on temperatures at which voiding was generated as shown in Figure A-7.

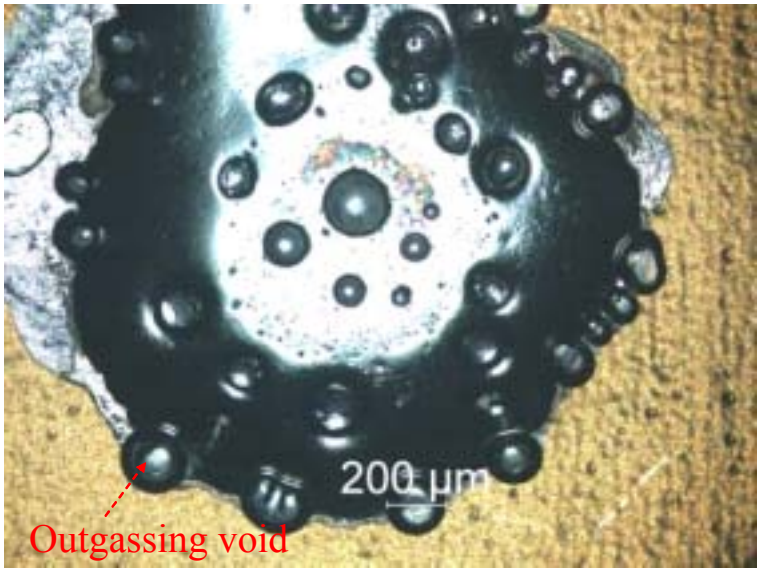


Figure A-7 Underfill G, Typical micrograph of conduction thermal testing

As shown in Table A-6, the peak temperatures for the no-flow underfills were similar based on conduction and convection conditions.

Table A-6 Material thermal characteristics for the first round evaluation

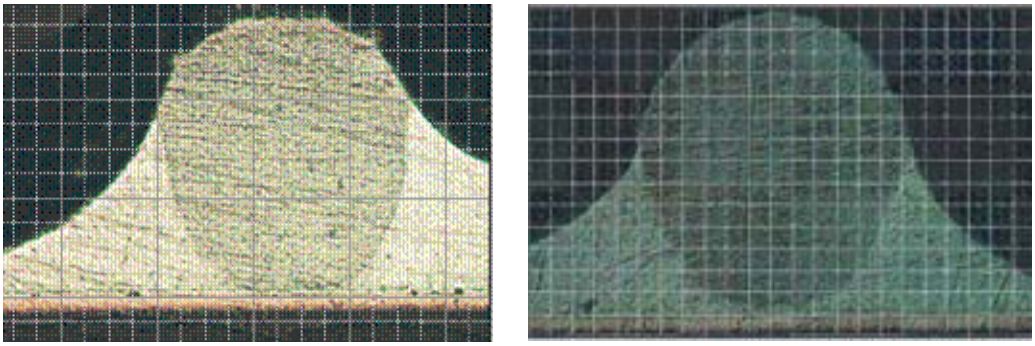
Product	Conduction Peak Temp °C	Convection Peak Temp °C	Selection for FCIP test vehicle assembly x = not selected O = selected
Underfill A	199.4	230	x
Underfill B	207.6	230	X
Underfill C	209.8	220	O
Underfill D	NA	240	X
Underfill E	NA	220	x
Underfill F	NA	220	X
Underfill G	NA	230	O
Underfill 1	247.4	230	x
Underfill 2	228.4	230	x
Underfill 3	NA	230	O
Underfill 4	NA	230	O

Two rounds of thermal material evaluations were conducted to find the thermal limit of underfill materials. Underfill A ~ E and underfill 1 ~ 2 were evaluated in the first round study. The second round of material evaluations determined the temperature range of Underfill F, G, 3, and 4. The underfill materials were developed based on the formulation of underfills which achieved high yield in pre-qualifying assembly using eutectic lead-tin area array flip chip test vehicles in the first round of material evaluations. The process development procedures such as thermal testing and wetting study were skipped in the second material evaluation and previously established high yields assembly processes were applied to underfills which were developed for the second

round material evaluations. The underfills that achieved high yields in pre-qualifying assembly using eutectic lead-tin area array flip chip test vehicles were chosen for application of FCIP. Eventually, Underfill C was selected in the first round and underfills G, 3, and 4 were selected in the second round for the FCIP assembly process development respectively.

A.3.2 High Lead and Eutectic Solder Wetting Study

A typical micrograph of the test coupon used in the solder wetting study is shown in Figure A-8. Notice the wetting of the eutectic solder up the high lead solder sphere. The micrograph of Figure A-8 was formed using cross section analysis of a solder wetting coupon. The digital images were imported into an image analysis software package and grid lines added to the images. The M-factor (wetter factor) was calculated using a commercial image analysis software package.



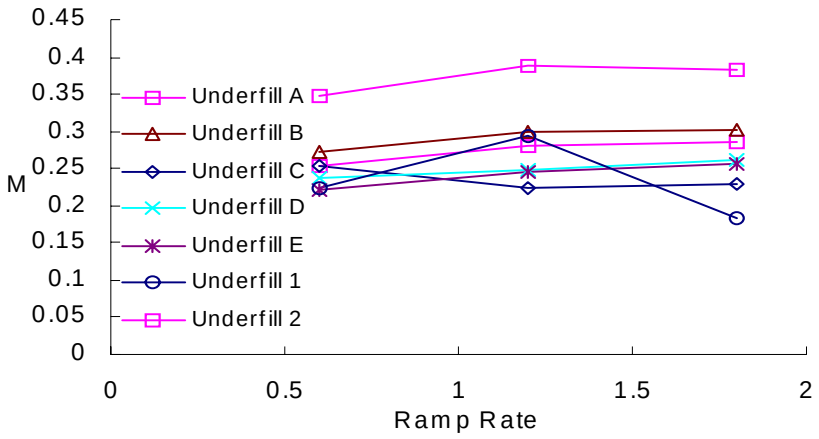
Underfill 1 Underfill C

Figure A-8 Micrograph of high lead solder on the Sn/Pb (63/37) pad in wetting study

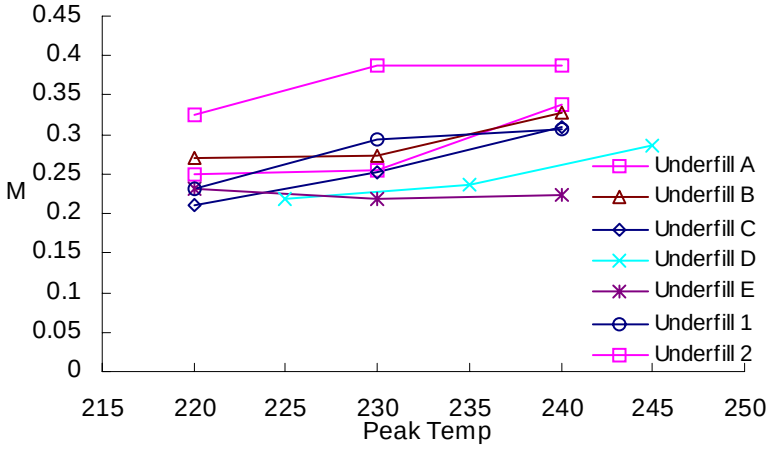
Parametric analysis of the reflow parameters produced the M-factor variations shown in Figure A-9 with respect to ramp rate, peak temperature, and time above liquidus. A high M-factor represents a high degree of wetting. Generally speaking, underfill C and underfill 1 showed higher M-factors. Hence, underfill C and underfill 1 were considered to have good wettablity.

Table A-7 M-factor of wetting study

Run order	Underfill A	Underfill B	Underfill C	Underfill D	Underfill E	Underfill 1	Underfill 2
1	0.2541	0.2724	0.2535	0.2363	0.2198	0.2238	0.3474
2	0.2803	0.3002	0.2237	0.2470	0.2462	0.2948	0.3883
3	0.2861	0.3009	0.2303	0.2617	0.2568	0.1838	0.3836
4	0.2495	0.2708	0.2094	0.2194	0.2336	0.2303	0.3264
5	0.3383	0.3269	0.3108	0.2849	0.2257	0.3066	0.3695
6	0.2997	0.2318	0.3151	0.2435	0.2386	0.2339	0.3492
7	0.3019	0.2280	0.3028	0.2779	0.2673	0.4111	0.3716



(a)



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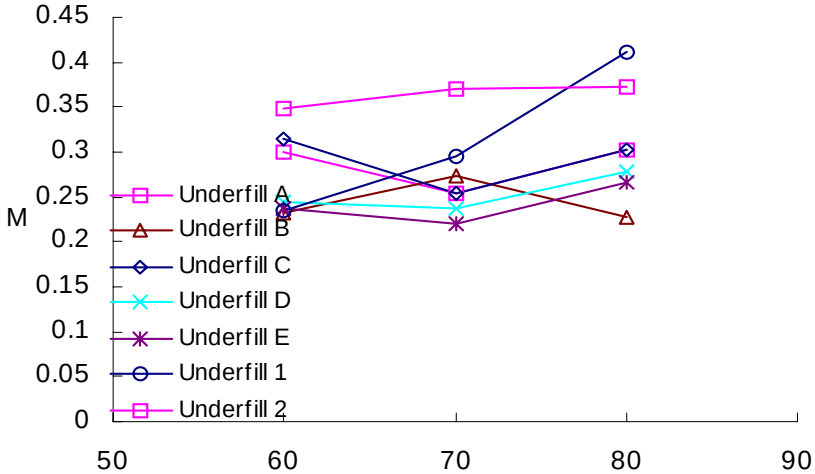


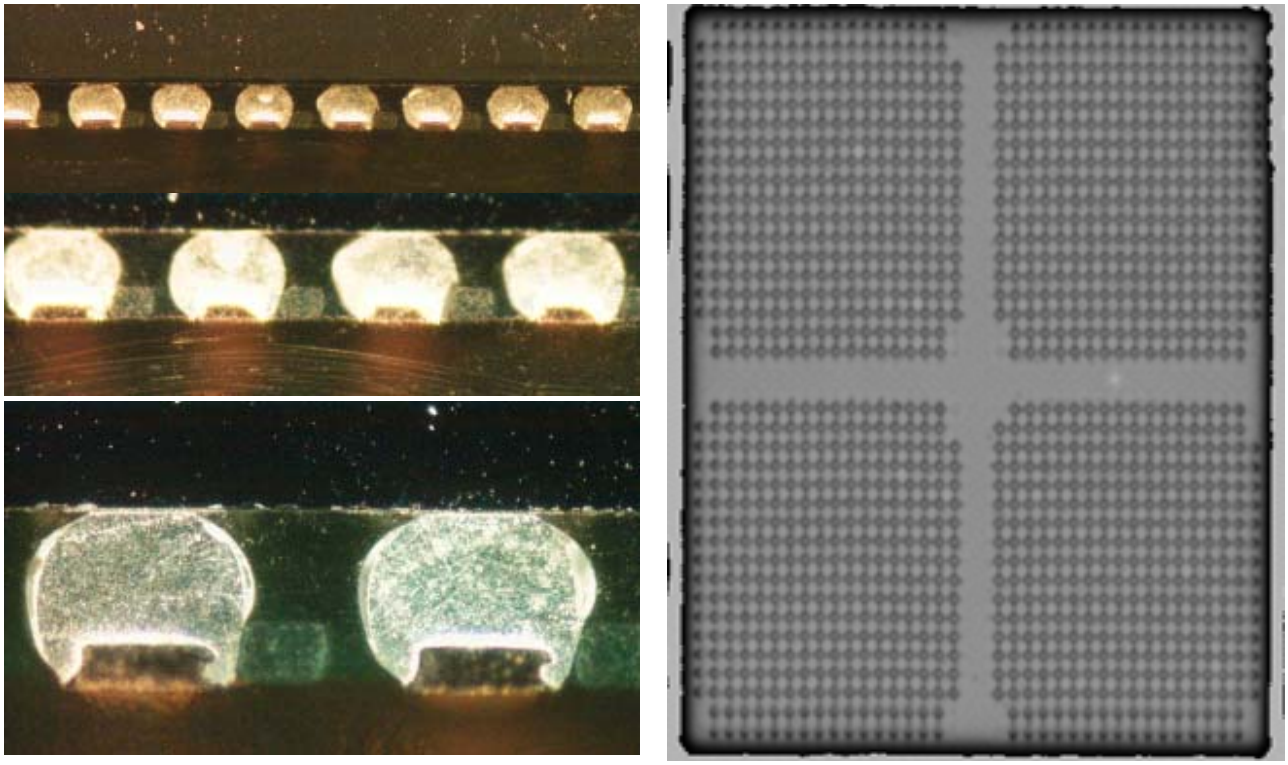
(c)

Figure A-9 M-factor chart of wetting study: (a) M-factor vs. ramp rate, (b) M-factor vs. peak temp, and (c) M-factor vs. time above liquidus

A.3.3 Pre-qualifying Assembly Using Lead-Tin Flip Chip Test Vehicles (FA10)

A total of 11 commercially developed no-flow underfill materials were studied in the material evaluation experiments. From these results, several no-flow underfill materials were utilized in the pre-qualifying flip chip assembly testing.

Underfills C, G, 3 and 4 achieved higher yields (>99%) in processing the eutectic lead-tin FA10-4 test vehicles. The high quality of wetting can be seen in Figure A-10. Underfill 5 also had relatively low voiding as shown in Figure A-10, compared to the other no-flow underfills.



Ramp rate: 1.3 °C/s, Soak Temp: 140 ~ 165 °C

Soak time: 100 sec, Time >183°C: 90sec, Peak Temp: 225 °C

Figure A-10 Micrographs of FA10-4 built using Underfill 5

Table A-8 Optimized reflow parameter setting for wetting

UF	Initial ramp rate	Soak time	Final ramp rate	Time >183°C	Peak temp
underfill A	1.8 °C/s	90 sec (Temp: 150 ~170°C)	1.2 °C/s	80 Sec	235 °C
underfill B			1.2 °C/s	70 Sec	235 °C
underfill C			0.6 °C/s	80 Sec	235 °C
underfill D			1.2 °C/s	80 Sec	240 °C
underfill E			1.2 °C/s	70 Sec	235 °C
underfill 1	1.3 °C/s	100 sec (Temp: 140 ~160°C)	1.2 °C/s	80 Sec	235 °C
underfill 2			1.2 °C/s	70 Sec	235 °C

The FCIP test vehicle was expected to be more challenging in terms of no-flow underfill process yield compared with the FA10-4 eutectic lead-tin test vehicle. Recall that the FCIP test vehicles had high lead solder bumps interconnected with eutectic lead tin solder, I/O counts over 3000 and a pitch down to 150 μm. Successful assembly of these advanced flip chip packages has yet to be reported.

The five best performing no-flow underfill materials from the FA10-4 test vehicle assemblies were used for process development and assembly of the FCIP test vehicles. While five underfill candidates were evaluated in this experiment, Underfill 5 will be used to illustrate the typical experimental analysis performed on each of the no-flow underfill materials.

To begin to establish a FCIP process window, a design of experiments was conducted based on variations of reflow parameters as shown in Table A-9. The reflow profile design of experiments was based on a step profile and utilized 2 levels of ramp rate, soak time, time above liquidus, and peak temperature. The placement process parameters were

held constant for all assemblies and were based on conservative process conditions to minimize yield from placement related issues.

Table A-9 Design matrix for reflow process parameters

Ramp rate	Soak time (140 ~ 170 °C)	Time above liquidus	Peak temperature
Level 1 (1.1 °C/s)	Level 1 (50sec)	Level 1 (95 sec)	Level 1 (225 °C)
Level 2 (1.3 °C/s)	Level 2 (60sec)	Level 2 (115 sec)	Level 2 (235°C)

Metrics included electrical interconnect yield, quality of wetting, and underfill void formation. Two replicates were executed for each assembly condition. Each of the five no-flow underfill materials had 16 builds with eight different reflow conditions as shown in Table A-10. Table A-10 is an example of the design matrix used in reflow process parameterization DOE for underfill 5.

Table A-10 Underfill 5, Design of experiment matrix listing reflow parameter levels

Run order	Ramp rate	Soak time	Reflow time	Peak temp	Short/Open testing
1	1	1	1	1	Pass
2	1	1	1	1	Pass
3	2	1	2	1	Pass
4	2	1	2	1	Pass
5	1	1	2	2	Pass
6	1	1	2	2	Pass
7	2	1	1	2	Fail(Short)
8	2	1	1	2	Pass
9	2	2	1	1	Pass
10	2	2	1	1	Fail(Open)
11	1	2	2	1	Pass
12	1	2	2	1	Pass
13	1	2	1	2	Pass
14	1	2	1	2	Pass
15	2	2	2	2	Pass
16	2	2	2	2	Pass
Total builds	16				14(87.5%)

A.3.4 Assembly Process Development with High I/O, Fine-Pitch Flip Chip

Many commercial underfills did not achieve high yields process due to high I/O density (over 1300), large chip size (over 10 mm), and fine pitch (down to 150 micron) of FA10-4. The FCIP device also has more difficulty changing to get high yields process in terms of IO density, chip size and pitch. The high yield assembly process established in the pre-qualifying experiment using FA10-TV was applied to the FCIP-TV assembly process for reflow parameter evaluation. Reflow parameter evaluation according to design of experiment (DOE) was executed to achieve a high yields process for FCIP flip chip device. Each reflow parameter has a 20% margin between level 1 and level 2 in DOE; the ramp rate has 10 % between level 1 and level 2.

Electrical interconnection was the main metric for reflow parameter evaluation and statistical analysis determined reflow parameters for an improvement of electrical yield. Then the improved reflow process will be the baseline process in placement characterization and dispense characterization to achieve a nearly void-free process. Conservative process parameters will be used for assembly. For example, a high placement force (10N) and low placement speed (3sec) were used in placement process respectively. The metric was electrical interconnect. In general, each design matrix for each material has an 8 partial factorial with two replicates.

A.3.4.1 Reflow Parameter Evaluation using Underfill C

Table A-11 Underfill C, Design matrix of a DOE

Levels/Factors	Ramp rate	Soak time (140 ~ 165 °C)	Time above liquidus	Peak temperature
(2 replicates)	Level 1 (1.8 °C/s)	Level 1 (0sec)	Level 1 (70 sec)	Level 1 (220 °C)
	Level 2 (2.0 °C/s)	Level 2 (40sec)	Level 2 (90 sec)	Level 2 (230°C)

Table A-12 Underfill C, Design of experiment

Run order	Ramp rate	Soak time	Reflow time	Peak temp	Yields
1	1	1	1	1	Pass
2	1	1	1	1	Pass
3	2	1	2	1	Fail(Open)
4	2	1	2	1	Pass
5	1	1	2	2	Pass
6	1	1	2	2	Fail(Open)
7	2	1	1	2	Pass
8	2	1	1	2	Fail(Open)
9	2	2	1	1	Pass
10	2	2	1	1	Fail(Open)
11	1	2	2	1	Pass
12	1	2	2	1	Pass
13	1	2	1	2	Pass
14	1	2	1	2	Pass
15	2	2	2	2	Pass
16	2	2	2	2	Pass
Total Builds	16				12 (75%)

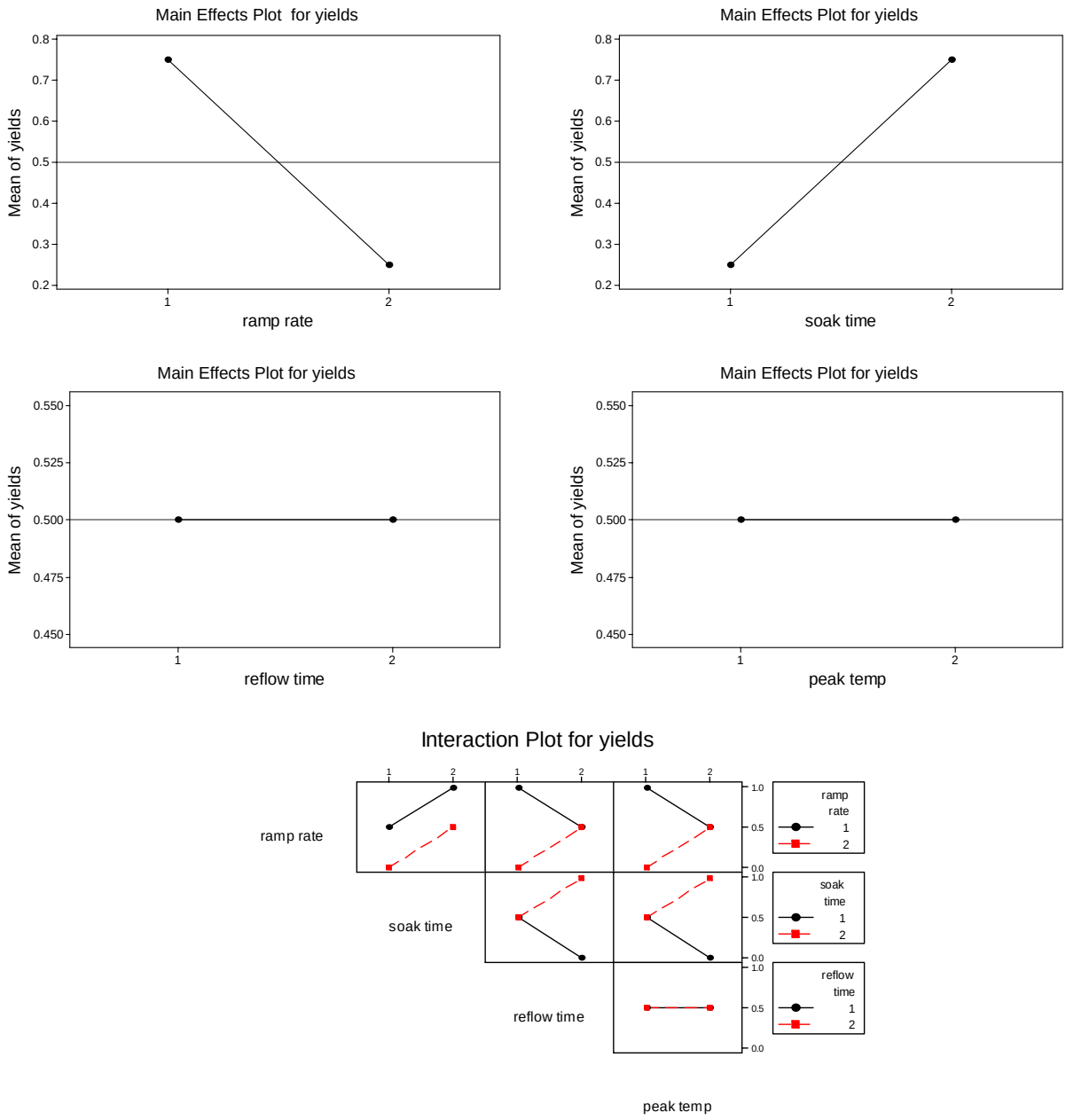
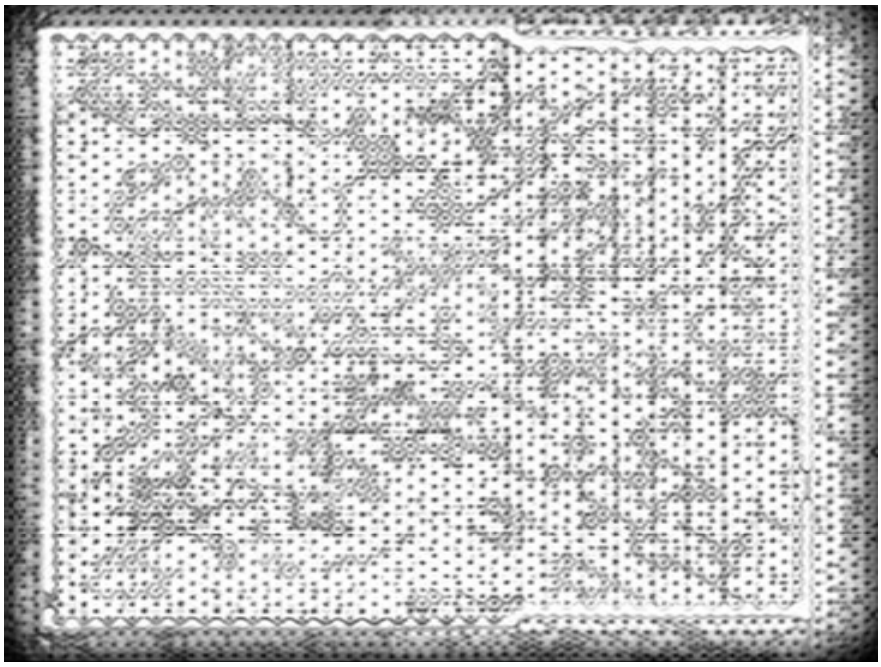


Figure A-11 Underfill C, Main effect and interactive effect plots for electrical yield

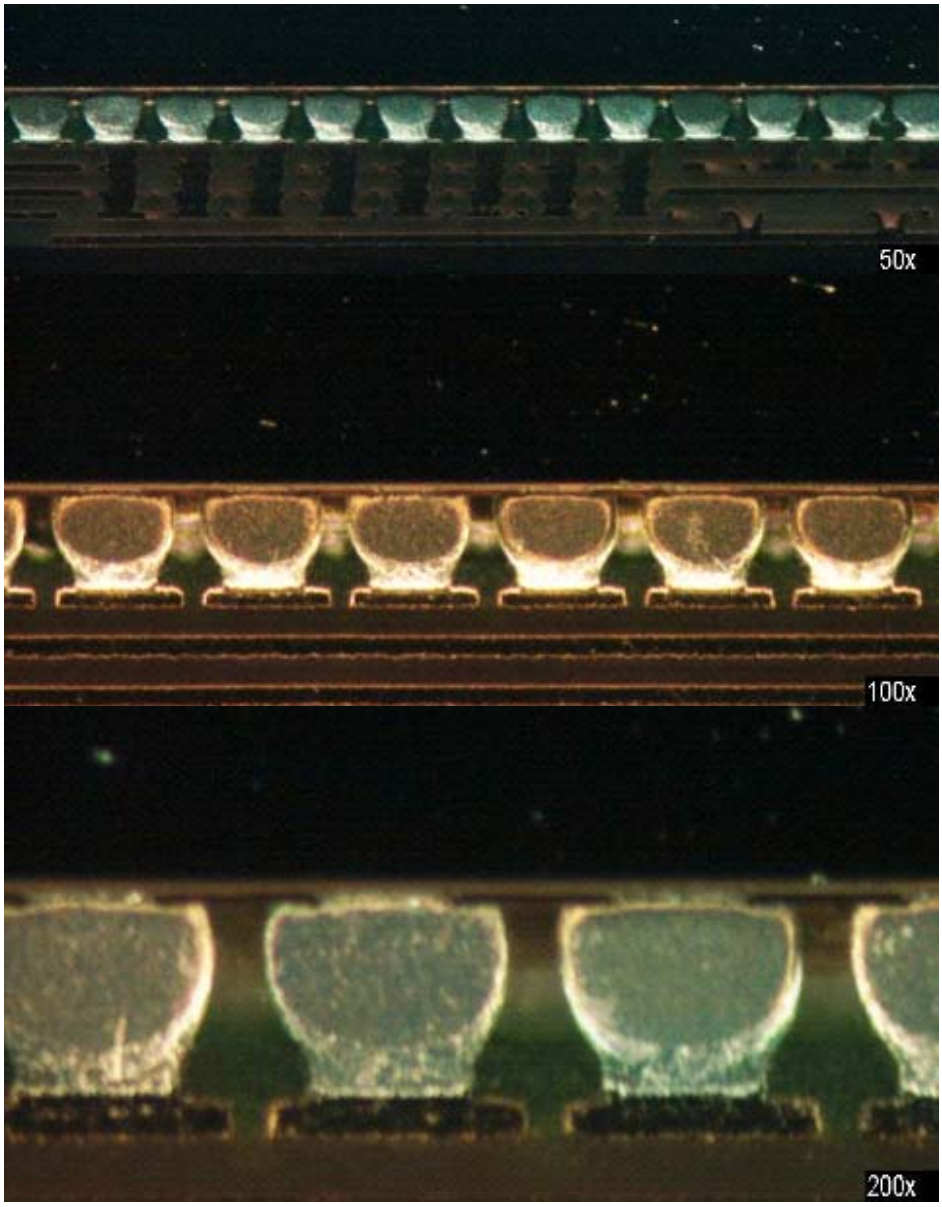
The results presented in Figure A-11 are based on the electrical interconnection yield as the response metric. A change in reflow time and peak temperature do not affect the

electrical yield based on main effect plots. An increase in ramp rate is seen to decrease the yield.



Ramp Rate: 1.8°C/s, Soak Time: 0sec,
Reflow Time: 70 sec, Peak Temp: 220 °C

Figure A-12 Underfill C, Micrographs of C-SAM



Ramp Rate: 2.0 °C/s, Soak Temp: 140 ~165 °C
Soak Time: 40 sec, Reflow time: 70sec, Peak Temp: 220 °C

Figure A-13 Underfill C, Micrographs of destructive analysis

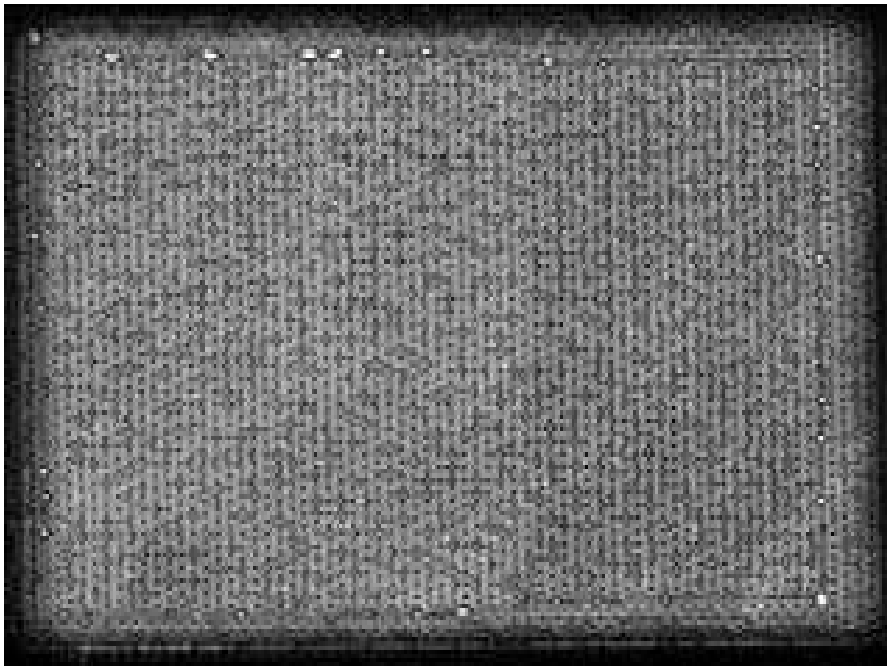
A.3.4.2 Reflow Parameter Evaluation using Underfill G

Table A-13 Underfill G, Design matrix of a DOE

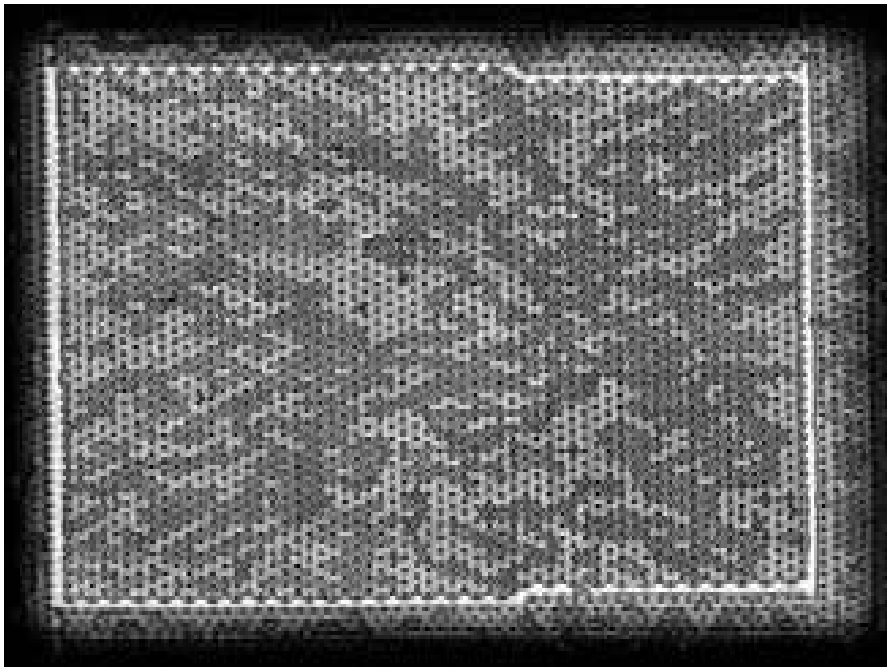
Levels/Factors	Ramp rate	Soak time (140 ~ 165 °C)	Time above liquidus	Peak temperature
(2 replicates)	Level 1 (2.1 °C/s)	Level 1 (0sec)	Level 1 (70 sec)	Level 1 (225 °C)
	Level 2 (2.3 °C/s)	Level 2 (50sec)	Level 2 (80 sec)	Level 2 (235°C)

Table A-14 Underfill G, Design of experiment

Run order	Ramp rate	Soak time	Reflow time	Peak temp	Yields
1,2	1	1	1	1	Pass
3,4	2	1	2	1	Pass
5,6	1	1	2	2	Pass
7,8	2	1	1	2	Pass
9,10	2	2	1	1	Pass
11,12	1	2	2	1	Pass
13,14	1	2	1	2	Pass
15,16	2	2	2	2	Pass
Total Builds	16				16 (100%)

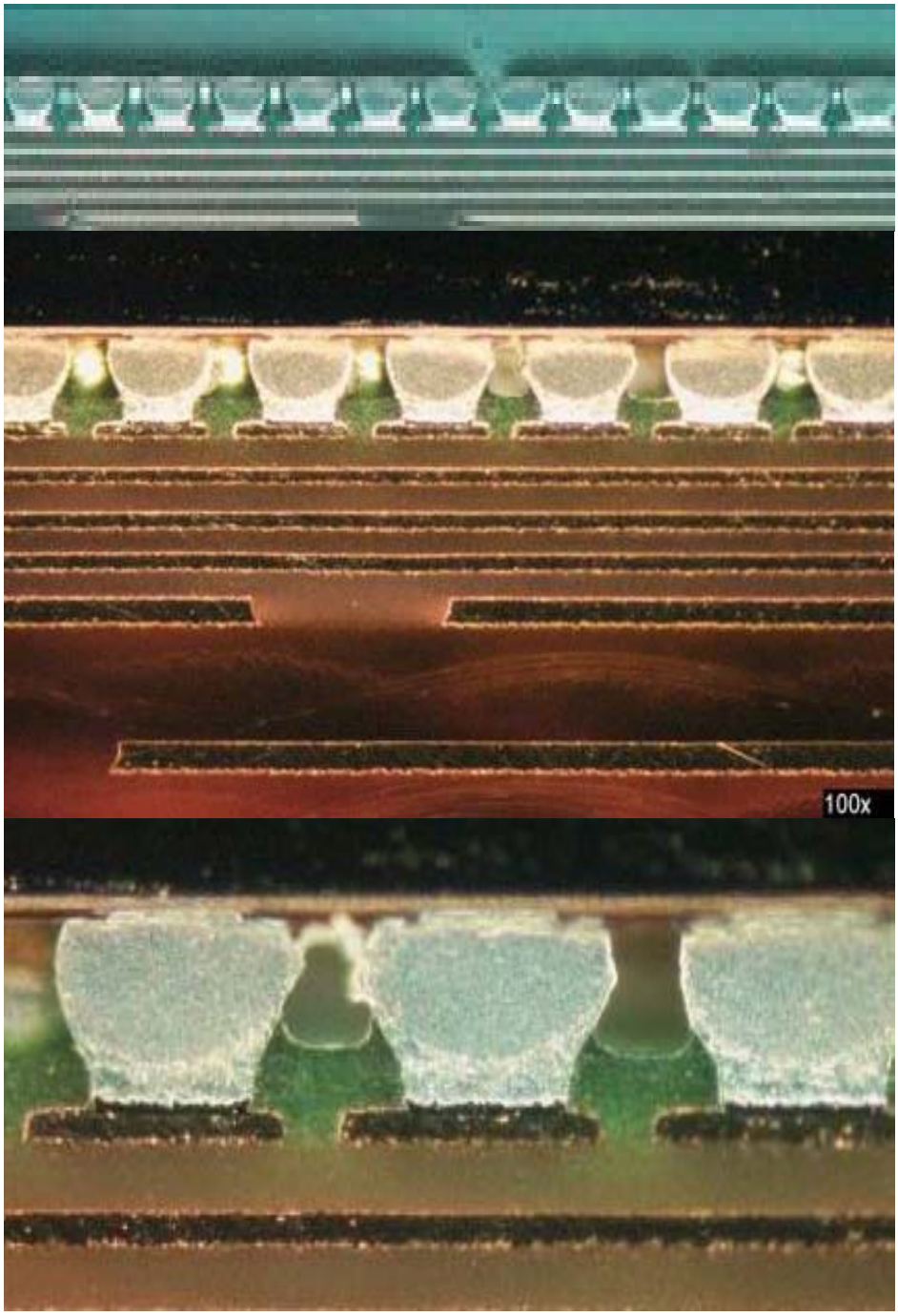


Baseline Step Profile: Ramp Rate: 2.1°C/s, Soak Time: 50 Sec, Reflow Time: 70 sec, Peak Temp: 225 °C



Baseline Ramp Profile: Ramp Rate: 2.1 °C/s, Reflow Time: 70 sec, Peak Temp: 225 °C

Figure A-14 Underfill G, Micrographs of FCIP device using C-SAM



Ramp Rate: 2.1 °C/s, Reflow time: 70sec, Peak Temp: 225 °C

Figure A-15 Underfill G, Micrographs of destructive analysis

A.3.4.3 Reflow Parameter Evaluation using Underfill 3

Table A-15 Underfill 3, Design matrix of a DOE

Levels/Factors	Ramp rate	Soak time (140 ~ 165 °C)	Time above liquidus	Peak temperature
(2 replicates)	Level 1 (1.1 °C/s)	Level 1 (50sec)	Level 1 (95 sec)	Level 1 (225 °C)
	Level 2 (1.3 °C/s)	Level 2 (60sec)	Level 2 (115 sec)	Level 2 (235°C)

Table A-16 Underfill 3, Design of experiment

Run order	Ramp rate	Soak time	Reflow time	Peak temp	Yields
1	1	1	1	1	Pass
2	1	1	1	1	Pass
3	2	1	2	1	Pass
4	2	1	2	1	Pass
5	1	1	2	2	Pass
6	1	1	2	2	Pass
7	2	1	1	2	Fail(Short)
8	2	1	1	2	Pass
9	2	2	1	1	Pass
10	2	2	1	1	Fail(Open)
11	1	2	2	1	Pass
12	1	2	2	1	Pass
13	1	2	1	2	Pass
14	1	2	1	2	Pass
15	2	2	2	2	Pass
16	2	2	2	2	Pass
Total Builds	16				14 (87.5%)

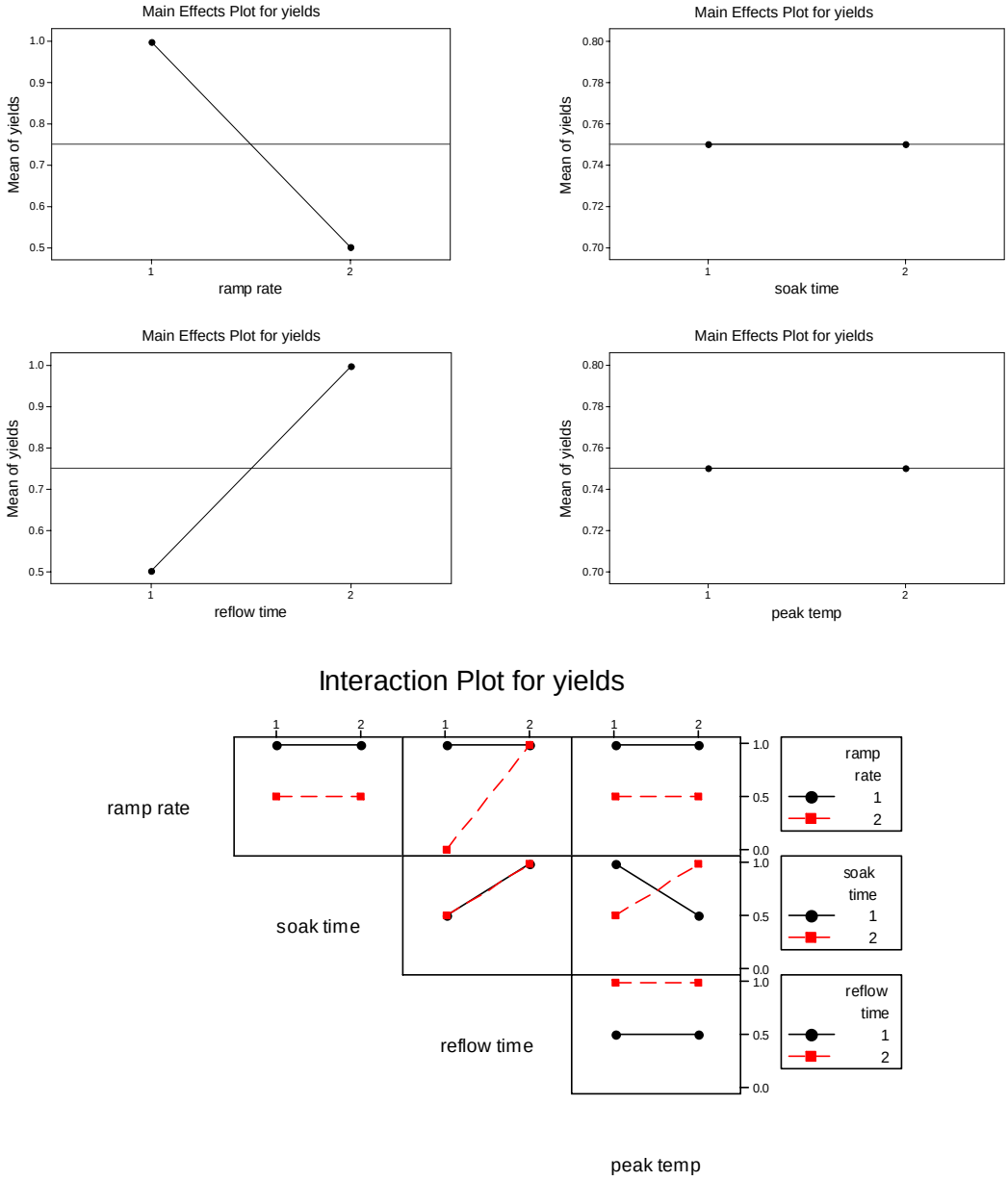
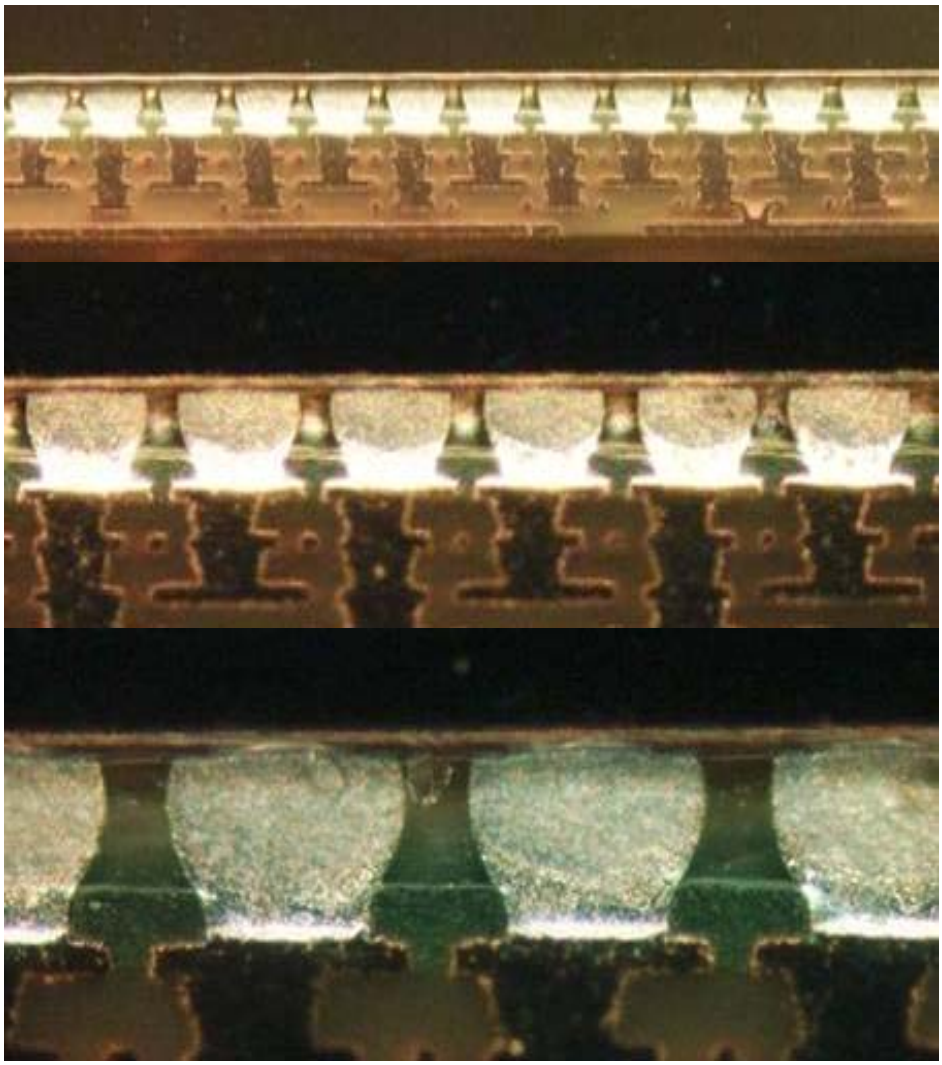


Figure A-16 Underfill 3, Main effect and interactive effect plots for electrical yield

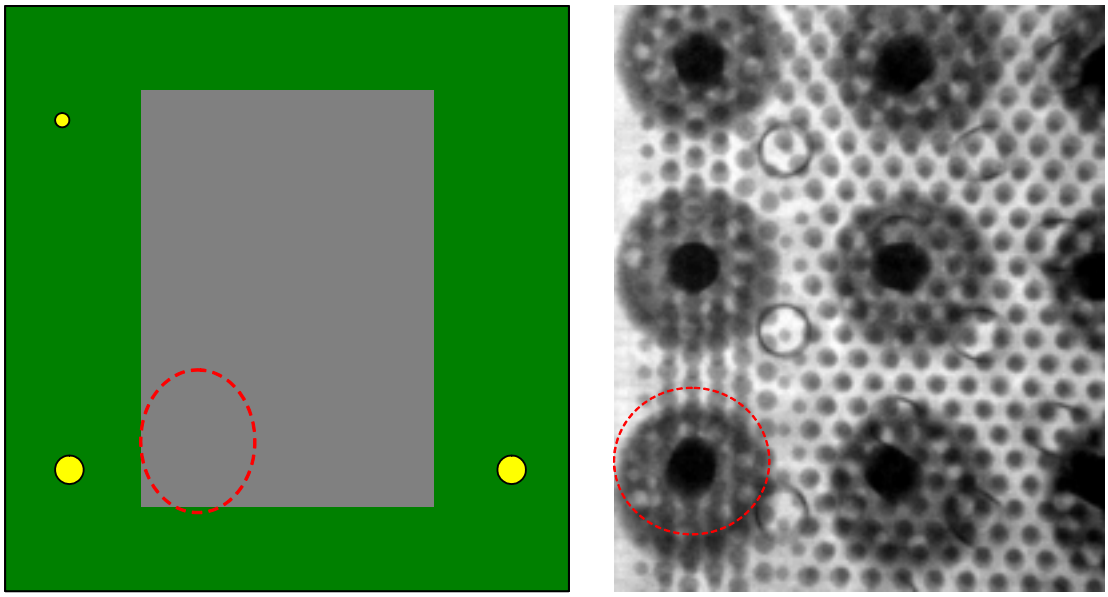
The results presented in Figure A-16 are based on the electrical interconnection yield as the response metric. A change in soak time and peak temperature do not affect the

electrical yield based on main effect plots. High ramp rate is seen to decrease the yield. However, an increase in reflow time will increase yield.



Ramp Rate: 1.1°C/s, Soak Temp: 140 ~165 °C, Soak Time: 50sec,
Reflow Time: 95 sec, Peak Temp: 225 °C

Figure A-17 Underfill 3, Micrographs of destructive analysis



a) FCIP TV b) X-Ray Microscopy

Figure A-18 Underfill 3, Micrograph of a failed part due to short failure

Micrograph of X-Ray in Figure A-18 showed yield failure due to electrical short. The high lead solder bump in red circle wetted on the two eutectic solder pads.

A.3.4.4 Reflow Parameter Evaluation using Underfill 4

Table A-17 Underfill 4, Design matrix of a DOE

Levels/Factors	Ramp rate	Soak time (140 ~ 165 °C)	Time above liquidus	Peak temperature
(2 replicates)	Level 1 (1.1 °C/s)	Level 1 (50sec)	Level 1 (95 sec)	Level 1 (225 °C)
	Level 2 (1.3 °C/s)	Level 2 (60sec)	Level 2 (115 sec)	Level 2 (235°C)

Table A-18 Underfill 4, Design of experiment

Run order	Ramp rate	Soak time	Reflow time	Peak temp	Yields
1	1	1	1	1	Pass
2	1	1	1	1	Pass
3	2	1	2	1	Pass
4	2	1	2	1	Pass
5	1	1	2	2	Pass
6	1	1	2	2	Fail(Short)
7	2	1	1	2	Pass
8	2	1	1	2	Fail(Open)
9	2	2	1	1	Fail(Open)
10	2	2	1	1	Fail(Open)
11	1	2	2	1	Pass
12	1	2	2	1	Pass
13	1	2	1	2	Pass
14	1	2	1	2	Pass
15	2	2	2	2	Pass
16	2	2	2	2	Fail (Misalignment)
Total Builds	16				11 (68.75%)

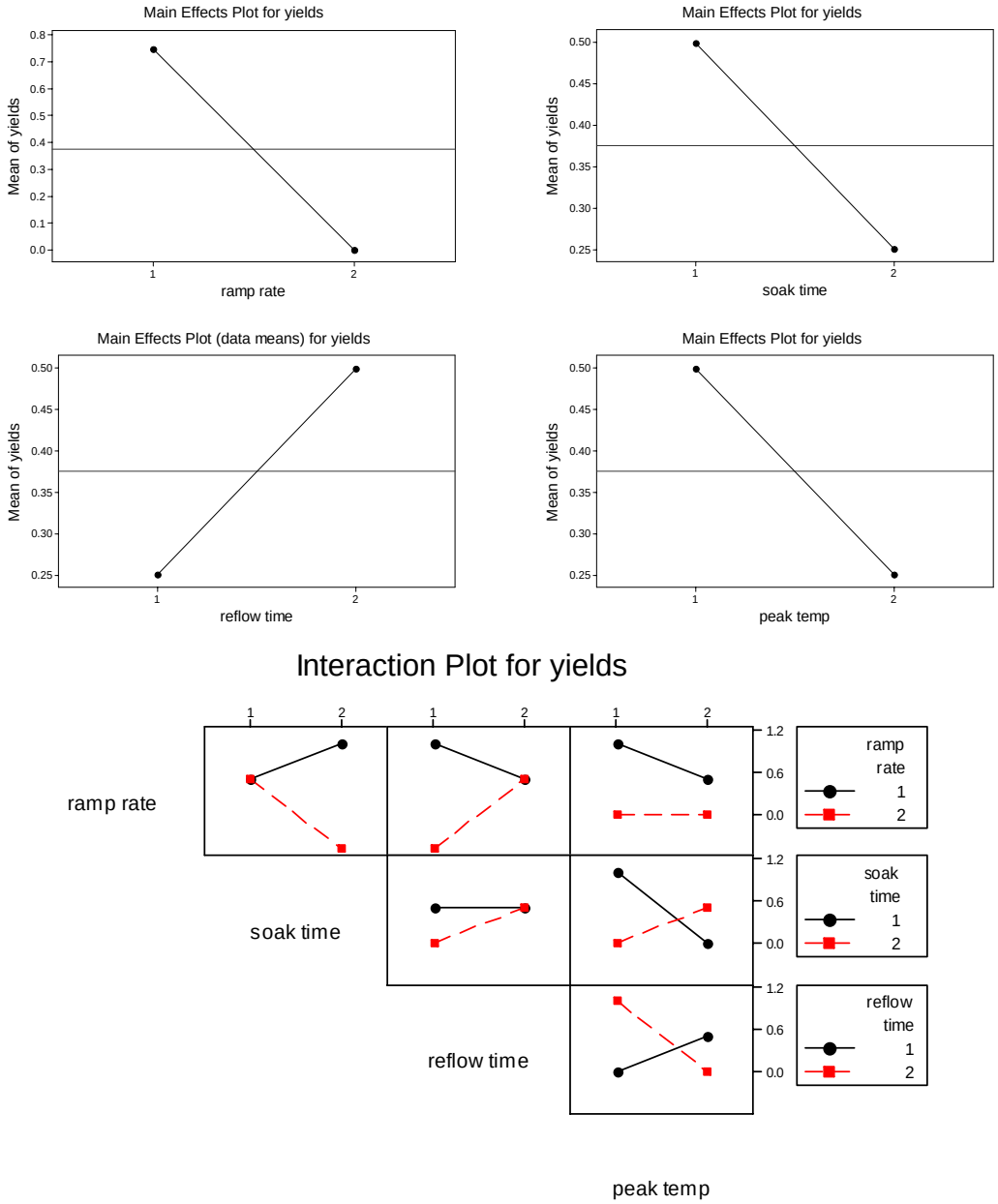
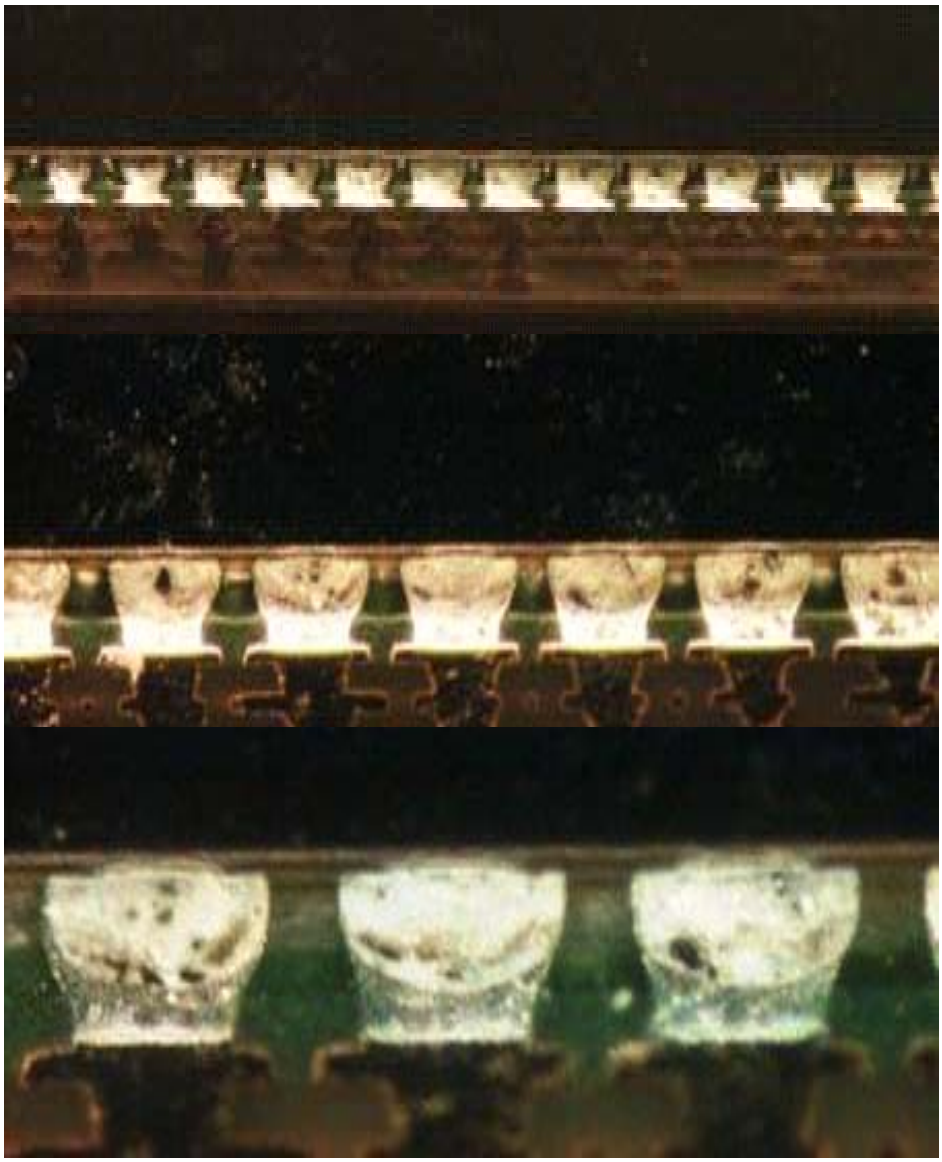


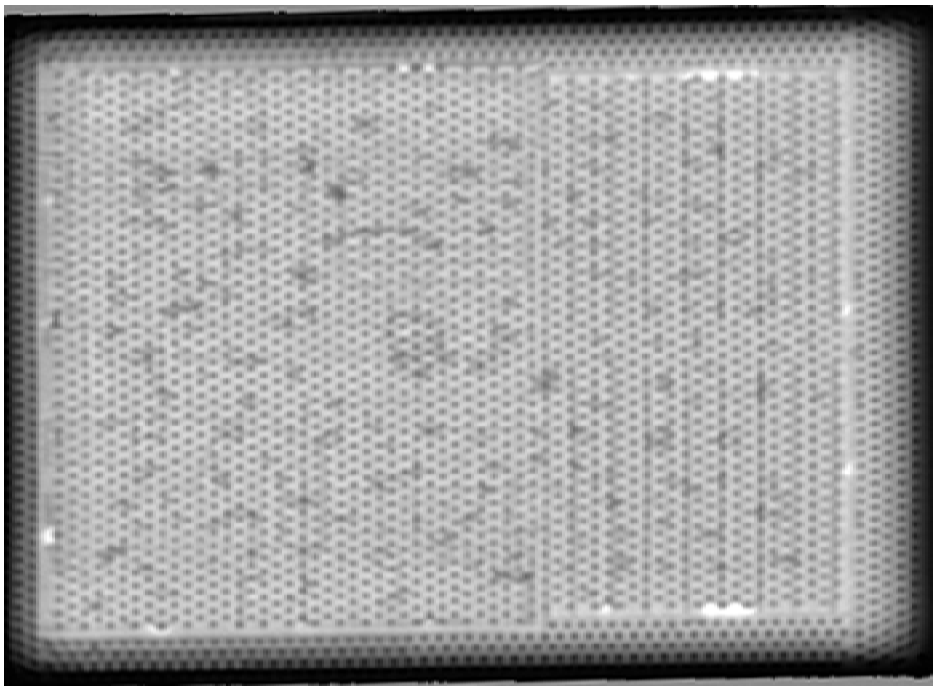
Figure A-19 Underfill 4, Main effect and interactive effect plots for electrical yield

The results, presented in Figure A-19, are based on electrical interconnection yield as the response metric. An increase in ramp rate, soak time and peak temperature decreases the yield. Similar to Underfill E result, an increase in reflow time increases the yield.



Ramp Rate: 1.1°C/s, Soak Temp: 140 ~165 °C, Soak Time: 50sec, Reflow Time: 95 sec, Peak Temp: 225 °C

Figure A-20 Underfill 4, Micrographs of destructive analysis



Ramp Rate: 1.1°C/s, Soak Temp: 140 ~165 °C, Soak Time: 50sec, Reflow Time: 95 sec, Peak Temp: 225 °C

Figure A-21 Underfill 4, Micrographs of destructive analysis

5) Failure mode analysis

Ramp rate: 1.3 °C/s, Soak time: 60sec, Reflow time: 95 sec, Peak Temp: 225 °C

Figure A-22 Underfill 4, Micrograph of chip floating in 100% IO opening failure

Chip floating appeared at high ramp rate and high soak time, causing failure in electrical interconnection. Eutectic solders on the FCIP substrate melt during reflow process as shown in Figure A-22.

APPENDIX B

DIFFUSION COEFFICIENT MODEL

A large amount of research studied the diffusion using experimental or theoretical methods [42, 84, 87, 93-105]. Some studied the diffusion of carboxylic acid into aqueous solutions [84, 87, 94]. Krevelen explained the diffusion of gases into polymer solutions considering solvent molecule diameters based on experimental results [70, 71]. His study has wide application for gas diffusion into polymer. Thus, the gas diffusion model could be applicable to underfill voiding because the underfill is an epoxy-based material, which is a thermosetting polymer. Actually, the main material of no-flow underfill is epoxy. Therefore, his diffusion model was used to determine gas diffusion coefficients in molten underfills. Chapter 4 identified the main source of a gas as carboxylic acid (acetic acid) using GS-MS. Acetic acid was used for the diffusion model.

Typically, polymers can be classified into elastomers and glassy polymers depending on their glass transition temperatures (T_g). If the T_g is above typical room temperature (25 °C), polymers are glassy. If the T_g below room temperature, the polymers are elastomers. Epoxy, the main material of no-flow underfill, can be classified as a glassy polymer as described in Table B-1.

Table B-1 Polymer classification with T_g

Polymer	
Elastomers $T_g < 298K$	Silicone rubber Butyl rubber Natural rubber
Glassy polymers $T_g > 298K$	Epoxy resin Polystyrene Poly(bispheol) Poly(vinyl acetate)

The diffusion of gases can be considered a thermally activated process described by an Arrhenius type equation:

$$D = D_0 \exp\left(-E_D / RT\right) \tag{B-1}$$

where D_0 and E_D are constants for the particular gas and polymer. The data on the diffusivity of gases in various polymers were collected by Stannett [105]. Using collected data, Krevelen investigated the diffusion of gases into polymers[70, 71]. In his book, he suggested the relationship between activation energy (E_D) and molecular diameter by taking nitrogen as the standard gas of comparison as follows:

$$\left(\frac{\sigma_{N_2}}{\sigma_x}\right)\frac{E_D \times 10^{-3}}{\mathbf{R}} = p \tag{B-2}$$

where E_D is the activation energy, σ is the diameter of gas molecules, **R** is the gas constant, and p is the influence of the diffusion gas. The parameter p is plotted as a function of glass transition temperature (T_g) in Figure B-1.

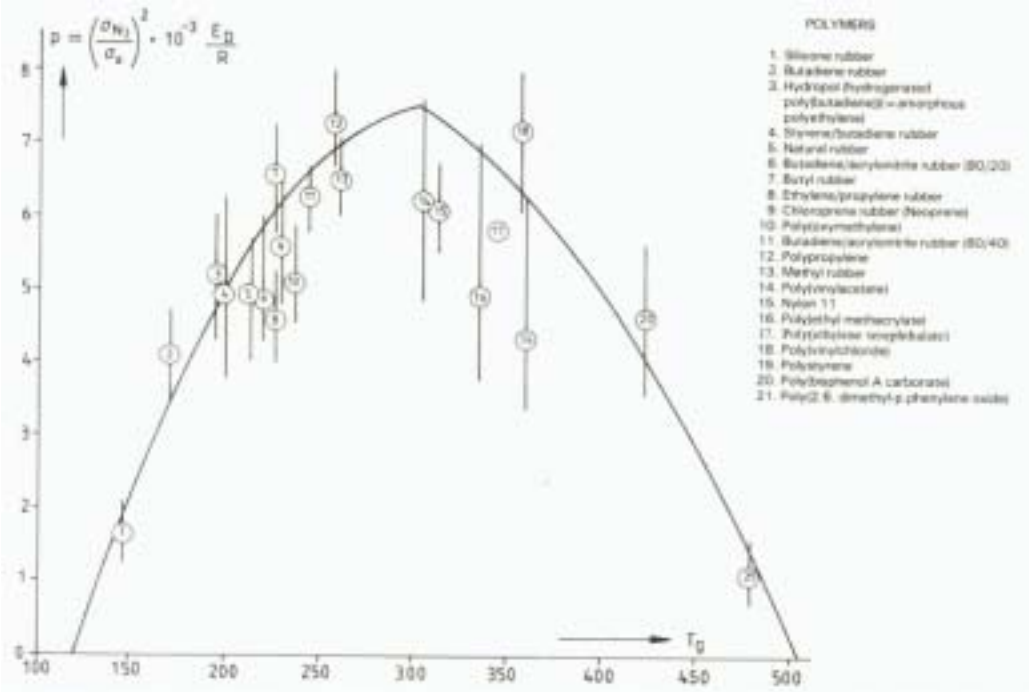


Figure B-1 Activation energy of diffusion as a function of T_g [70, 71]

The drawn curves as shown in Figure B-1 correspond to the following equations: for elastomers:

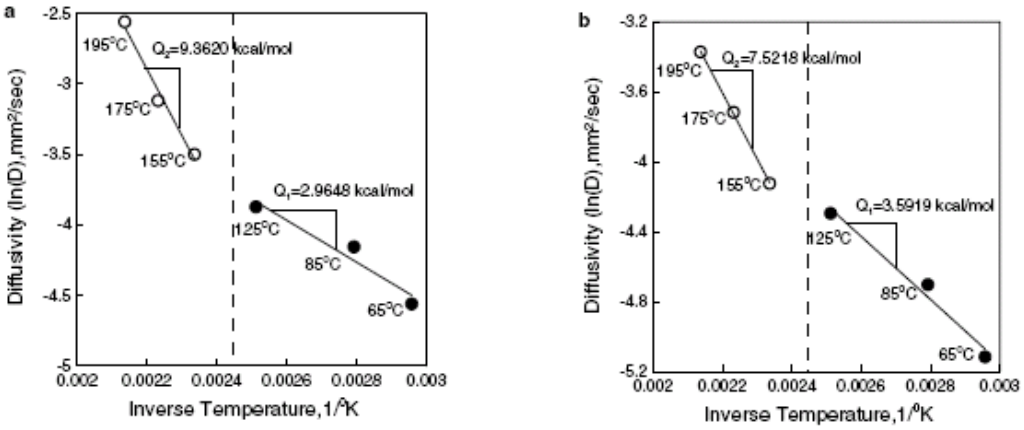
$$p = 7.5 - 2.5 \cdot 10^{-4} \left(298 - T_g\right)^2 \qquad (T_g < 298\ K) \qquad \text{(B-3)}$$

for glassy polymers:

$$p = 7.5 - 2.5 \cdot 10^{-4} \left(T_g - 298\right)^{3/2} \qquad (T_g > 298\ K). \qquad \text{(B-4)}$$

With simple algebraic manipulation, the activation energy can be calculated using equations (B-2) and (B-4) for epoxy. T_g is 354K, σ_{N2} is 3.7A, and σ_x is 3.8 A. Hence, the activation energy is calculated in the solid state. The solid state might have limitation to predict the diffusion coefficient in the molten state at high temperature. Typically, underfill voiding nucleated at 200 °C. Actually, Lin et al. predicted the activation energy of moisture diffusion into epoxy [95] in the solid state and liquid states to improve the

accuracy of gas diffusion model using molecular dynamics as shown in Figure B-2. In addition, they validated the model with experimental results. $E_{D\ solid}/E_{D\ liquid}$ was 3.15. For this reason, the correction factor could predict the activation energy in a liquid using the activation energy calculated in the solid state.



(a) (b)

Figure B-2 Activation energy of diffusion as a function of temperature: (a) experiment and (b) molecular dynamics simulation

Next, the liquid state activation energy was used to determine D_0 using the following relationship:

$$\log D_0 \approx \frac{E_D \times 10^{-3}}{R} - 5.0 \tag{B-5}$$

The log of equation B-1 was taken, yielding

$$\log D(T) = \log D_0 - \frac{435}{T} \cdot 10^{-3} \frac{E_D}{R} \tag{B-6}$$

Eventually, the diffusion coefficient of acetic acid into molten underfill was computed using equations (B-5) and (B-6) at 200 °C with the activation energy calculated using equations (B-2) and (B-4). Table B-2 presents the model constants used to predict the diffusivity of a carboxylic acid into molten underfill.

Table B-2 Overview of diffusion coefficient model

Parameters	Value
Glass transition (T_g)	81.0 °C
Model constant (p)	7.395
Gas molecular diameter	3.8×10^{-9} m
Gas constant (**R**)	8.314 J/Kmol
$E_{Dliquid}$ (E_{Dsolid} E_{Dsolid}=*3.15*)	26170.630 J/mole
Diffusivity (D)	1.421×10^{-9} m^2/s

APPENDIX C

HENRY'S LAW CONSTANT MODEL

There are several reviews on models predicting Henry's law constant. [59, 60, 69-75]. This chapter presented a predictive scheme of Henry's law constant using a van der Waals equation of state [81, 82, 106, 107]:

$$P = \frac{\mathbf{R}T}{V-b} - \frac{a}{V^2} \tag{C-1}$$

where P denotes pressure, T temperature, V molar volume and R the ideal gas constant. a and b are co-volume parameters at critical point defined with $\frac{\partial P}{\partial V} = 0$ and $\frac{\partial^2 P}{\partial V^2} = 0$

Thus, a and b could be determined as a function of critical temperature, pressure, and accentric factor.

$$a = \frac{27}{64}\frac{\left(\mathbf{R}T_C\right)^2}{P_C} \text{ and } b = \frac{1}{8}\frac{\mathbf{R}T_C}{P_C} \tag{C-2}$$

For the mixture of polymer and solvent, mixing rules and combining rules were adopted [106-108].

$$a_{12} = \left(a_1 a_2\right)^{1/2} \tag{C-3}$$

Henry's law constant can be defined as follows based on [109] and using above mentioned mixing and combining rules of van der Waals:

$$H_{12} = \lim_{x_1 \to 0} \varphi_1 P = \frac{\mathbf{R}T}{V_2 - b_2} \cdot \exp\left(\frac{b_1}{V_2 - b_2} - \frac{2a_{12}}{RTV_2}\right) \tag{C-4}$$

with subscript 1 corresponding to the solvent and 2 to the polymer. φ_1 is the fugacity coefficient of the solvent in the mixture, which could be calculated using the van der Waals equation of state. Later on, Georgis et al. determined a and b to predict Henry's law constant of several polymers as described in Table C-1 using an equation (C-4).

Table C-1: Equation of state parameters for several polymers using volumetric data

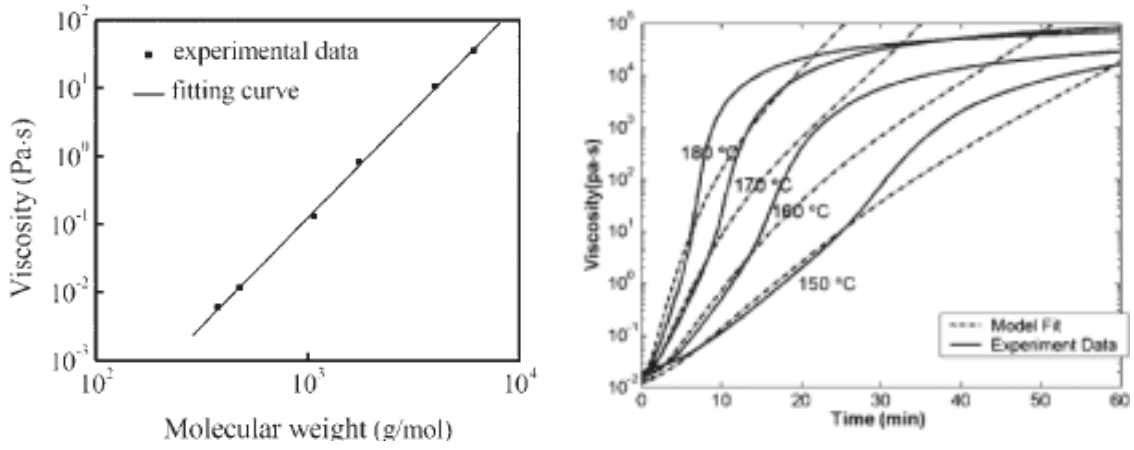
Polymers	% Average absolute Error in Henry constant	a $bar(cm^3/mol)^2$	b cm^3/mol	Error %
LDPE	1.4 (397~573K)	0.440E10	0.176E5	0.3
PS	0.7 (398~498K)	0.251E11	0.933E5	0.0
PDMS	1.1 (313~498K)	0.479E10	0.260E5	0.3
PVAC	1.5 (398~473K)	0.165E11	0.776E5	0.1
Acetic acid	N/A	$17.82*10^6$	168	0.0 (Exp)

Equation (C-4) has a small discrepancy with experimental results. Besides, Henry's law constant predicted the constant with wide temperature ranges.

$$a = \mathbf{R}\frac{T_{\max}v_{\max}^2 - T_{\min}v_{\min}^2}{v_{\min} - v_{\min}} \text{ and } b = \frac{v_{\min}v_{\max}\left(T_{\max}v_{\max} - T_{\min}v_{\min}\right)}{T_{\max}v_{\max}^2 - T_{\min}v_{\min}^2} \quad \text{(C-5)}$$

where T is temperature, **R** is the gas constant, and v_i is molecular volume at temperature i. At the temperature range, the model can predict Henry's law constant with the good agreement to experimental results using equations (C-4) and (C-5). To apply above mentioned model to underfill voiding, the molecular volume of epoxy needs determined at two different temperatures. Due to the limitation of experimental techniques, the molecular volume was computed using Sun's model [110]. They studied the relationship between viscosity and molecular weight of the epoxy at different temperatures. In addition, they measured the viscosity at the melting temperature of eutectic solder (183°C) and high lead solder (217°C) respectively. The model has good agreement before epoxy is fully cured as shown in Figure C-1. Therefore, their model determined

molecular weight of epoxy at 183°C and 217°C with measured viscosity using equation (C-6).



(a) (b)

Figure C-1: (a) logarithmic plot of viscosity as a function of the polymer molecular weight for epoxies at 183 °C and (b) Data fitting of the viscosity model at isothermal condition

The calculated molecular weight computed molecular volume considering density. Afterwards, the resulting computed molecular volumes at two temperatures were plugged into the equation (C-5). Then van der Waals constant was determined. Eventually, equation (C-4) computed Henry's law constant of underfill voiding with van der Waals constants of acetic acid and epoxy.

$$\ln \eta = -42.54 + 3.27 \ln \overline{M}_w + 8608 \frac{1}{T} \qquad \text{(C-6)}$$

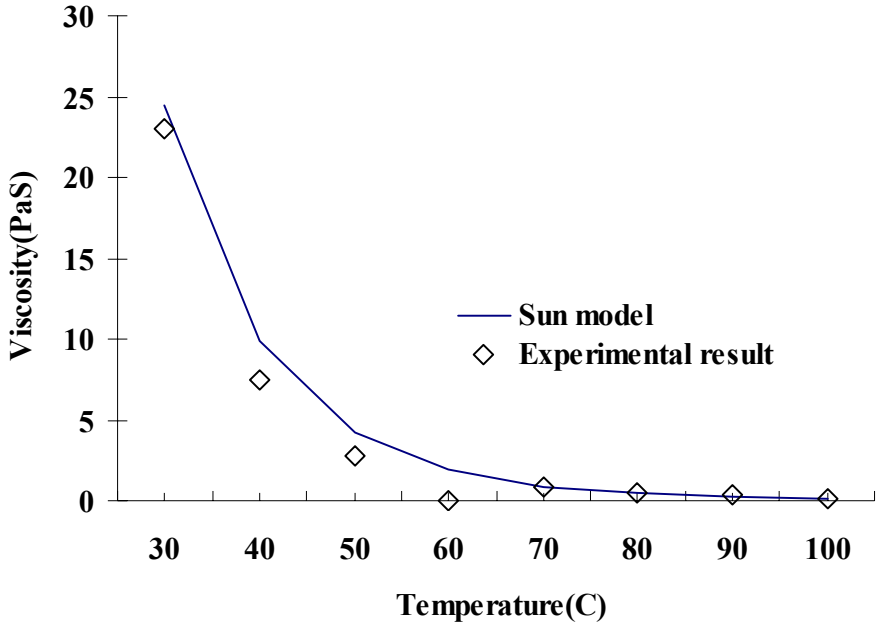


Figure C-2: Rheology of no-flow underfill and epoxy

Table C-2 Overview of Henry's law constant model

Polymer		
Viscosity (Pa·s)	T_1(187°C)	0.06
	T_2(217°C)	0.05
M_w (mole/g)	T_1(187°C)	617.797
	T_2(217°C)	829.456
Density(g/m^3)		1680000
Volume (m^3)	T_1(187°C)	0.00036774
	T_2(217°C)	0.00049372
a_2 (bar(m^3/mole)^2)		3.777×10^{-5}
b_2 (m^3/mole)		2.308×10^{-4}
vc (m^3/mole)		$6.924E\times10^{-4}$
Gas		
M_w (mole/g)		60
a_2 (bar(m^3/mole)^2)		0.00001782
b_2 (m^3/mole)		0.000168
Henry's constant (m^2/s^2)		3.253×10^{-5}

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