Development and modelling of a versatile active micro-electrode array for high density in-vivo and in-vitro neural signal investigation

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Development and modelling of a versatile active micro-electrode array for high density *in-vivo* and *in-vitro* neural signal investigation

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Abstract

The electrophysiological observation of neurological cells has allowed much knowledge to be gathered regarding how living organisms are believed to acquire and process sensation. Although much has been learned about neurons in isolation, there is much more to be discovered in how these neurons communicate within large networks. The challenges of measuring neurological networks at the scale, density and chronic level of non invasiveness required to observe neurological processing and decision making are manifold, however methods have been suggested that have allowed small scale networks to be observed using arrays of micro-fabricated electrodes. These arrays transduce ionic perturbations local to the cell membrane in the extracellular fluid into small electrical signals within the metal that may be measured.

A device was designed for optimal electrical matching to the electrode interface and maximal signal preservation of the received extracellular neural signals. Design parameters were developed from electrophysiological computer simulations and experimentally obtained empirical models of the electrode-electrolyte interface. From this information, a novel interface based signal filtering method was developed that enabled high density amplifier interface circuitry to be realised.

A novel prototype monolithic active electrode was developed using CMOS microfabrication technology. The device uses the top metallization of a selected process to form the electrode substrate and compact amplification circuitry fabricated directly beneath the electrode to amplify and separate the neural signal from the baseline offsets and noise of the electrode interface. The signal is then buffered for high speed sampling and switched signal routing. Prototype 16 and 256 active electrode array with custom support circuitry is presented at the layout stage for a 20 μm diameter 100 μm pitch electrode array. Each device consumes 26.4 μW of power and contributes 4.509 μV (rms) of noise to the received signal over a controlled bandwidth of 10 Hz - 5 kHz.

The research has provided a fundamental insight into the challenges of high density neural network observation, both in the passive and the active manner. The thesis concludes that power consumption is the fundamental limiting factor of high density integrated MEA circuitry; low power dissipation being crucial for the existence of the surface adhered cells under measurement. With transistor sizing, noise and signal slewing each being inversely proportional to the dc supply current and the large power requirements of desirable ancillary circuitry such as analogue-to-digital converters, a situation of compromise is approached that must be carefully considered for specific application design.

This thesis is dedicated to my father Roland Frederick Curry

Acknowledgements

I would like to thank Dr. Sherri Johnstone for stepping in as my supervisor towards the final stages of this project. It is unlikely that I would have succeeded without her invaluable help.

I would also like to express my thanks to Mark Rosamond and Dr. Andrew Gallant for helping me to perfect the microelectrode fabrication process for the experiments in chapters 6 & 7. Their assistance produced some fantastically reproducible 'merchandise' that gave me the means to identify the different capacitance mechanisms given by gold and platinum electrodes in saline.

I express my gratitude to Ian Hutchinson, Colin Wintrip, Neil Clarey and John Gibson of the school's technical staff for their assistance and advice during thesis work and the many other side projects during my time at Durham. I also wish to thank everyone in room E208 (the CES office) for their help and company during the PhD.

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Declaration

The work presented in this thesis is based on research carried out in the School of Engineering, University of Durham, UK. No part of this thesis has been submitted elsewhere for any other degree or qualification. The work is my own unless referenced to the contrary in the text.

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Chapter 1

Introduction

The work presented in this thesis develops the theoretical investigation and design of an active (transistor integrated circuit) bioelectric sensor device, capable of measuring and extracting the neural network activity of living neurons on a high spatiotemporal basis. The device is geared towards the electrophysiological study of cultured or dissected tissue (*in vitro*) and possible applications with tissue remaining intact inside the body (*in vivo*) of the studied organism.

Living neural networks are the basis for all biological sensation and processing. From the recognition of shapes to the enjoyment of music, the evidence strongly suggests that every isolated feeling and reaction is facilitated by relative neural positioning, interconnection and coordinated electrochemical activity formed by the vast parallel connection morphologies between billions of cells.

To understand the cumulative functionality of neurons, one must ideally be able to observe many such connected cells over a suitably long period of time. Considering that these cells are often much smaller than 100 μm and that complex functional networks may require the cooperation of many thousands of such cells, the task of observing each and every cell in the network during its operation becomes very difficult. Furthermore,

these cells are very fragile in nature and will only survive in environments closely resembling the in vivo state of their host species.

Fortunately for the curious researcher, neurons communicate using electrical signals that we may measure passively using many different electrical measurement approaches. However, many of these methods are harmful to the cell and do not allow the cell to function naturally over long periods of time. This may not be a problem in primary physiological research but for the study of network formation and operation it obviously reduces the link between *in vivo* (within the organism) and *in vitro* (outside of the organism) study and may terminate the operation of the cultured cells prematurely.

Further difficulties manifest themselves with the micron scale of discrete cells and the large numbers of such cells required to deliver mental functionality. There are for example thousands of billions of cells that constitute our own human thought processes and tens of thousands that constitute the simple nervous system of large pond snails, with each cell measuring many times less than 100 μm. It would be very difficult, if not impossible at this stage in neural signal interfacing to study every neuron in such a large network as presented by the snail.

We can however study smaller network connections that contribute to these larger systems to determine certain behavioural mechanisms of the neuron networks. Just as *in vitro* cultures were developed to isolate and simplify the dependencies of organ cells and neurons we may dissect and study small network groups with the final aim of understanding the larger system.

Solutions have been presented that utilise the measurable electrical activity of single and multiple communicating cells to observe network activity using penetrating and non-penetrating metallic electrode elements. However the only method capable of measuring large spatial signal distributions is the planar Micro Electrode Array (MEA). The cost for this flexibility is that only the local extracellular electrical activity of the neuron may be measured. This signal is very small in magnitude and may be in many situations very

close to the fundamental electrical noise floor of the measurement equipment. For high density recording MEAs it may be shown that the available number of electrodes is primarily limited by the connectivity of each electrode to external signal conditioning and monitoring equipment. For this reason electrode arrays rarely exceed 60-100 recording sites and do not come close to providing a one-to-one recording density with the studied neurons for large functional cultures. Because of these topological and electrical bottlenecks, integrated circuitry has been piggybacked with customised passive arrays to extend their versatility. Such circuitry, often termed 'neurochips' require large arrays of connective wiring and consume much larger physical areas than the neurons they are measuring. Due to the small magnitude of the extracellular signal that is measured there must be a low resistance path between the cell and the amplification circuitry to maintain the quality of the measured signal.

Objectives of this Work

This work represents an electronic engineer's attempt to investigate the interface between the biological and electronic domains for the purpose of neural signal measurement. By understanding the principles and mechanisms of this interface it is believed that a novel high density active transduction method may be developed to advance the measurement of high density neuron network communication.

The design of the device is developed using information gained from a generic physical model and computer simulation of the neural interface and the experimental characterisation of a suitable transducer microelectrode. By integrating the recording electrode with a dedicated amplification and conditioning circuitry, it is believed that many of the limitations of passive devices may be overcome, thus allowing a higher recording site density for larger numbers of channels. Electrode connectivity and access may also be improved by using digital channel selection and multiplexing schemes to reduce the number of device connections making the device more versatile and easy to use.

The ultimate goal of this work is to provide an active signal amplifying front end that approaches or is reduced below the size of a typical cultured neuron, such that a 1:1 ratio between neuron and active electrode may be reached. By providing immediate amplification to the neural signal at the source of transduction, many of the topological and operational constraints of passive MEAs may be reduced to a manageable level for large arrays, thus allowing the study of larger networks to further develop the current knowledge of neurological processing.

In addition, the advent of a cellular size active transducer may have relevance in other neighbouring biological fields such as cellular drug screening and smart biological sensors whereby the reaction of the cell to chemical or other stimuli may be detected by the electrical response patterns of the exposed culture.

This project was funded by the EPSRC (Engineering and Physical Sciences Research Council) under the EPPIC (Electronic and Photonics Packaging and Inter-Connection) Faraday partnership with additional funding from CELS (Centre of Excellence for Life Sciences) in the form of a CASE (Cooperative Awards in Science and Engineering).

Despite the interdisciplinary theme of the research it remains strongly placed in the field of electronic engineering. It may therefore be necessary to familiarise the reader with aspects of the neurological system under consideration before describing the development within the main body of work. It is hoped that this will provide an interesting and informative introduction to neurophysiology and this thesis.

1.1 Thesis Structure

This thesis is split into three main parts. The first discusses the relevant background and theoretical framework from which the work is built and considers the variety of methods that are used to observe neural signals. This begins in section 1.2 with an introduction to neurophysiology that establishes key concepts and physiological descriptions of neural

physiology. Chapter 2 gives a comprehensive comparison of various methods that are used to measure the electrophysiological signals of neurons and assesses their suitability for use in a high density recording site integrated device. Chapter 3 analyses and discusses the general problems that are associated with the passive and the active MEA systems as they approach higher densities.

Chapters 4 to 7 cover the second part of this thesis and address the modelling, simulation and experimental characterisation of the system around which the design and design methodology are centred. Chapter 4 develops an electrical model of a neuron based upon the empirical work of Hodgkin and Huxley and the theory of extracellular signal recording. A novel SPICE model is developed that is a 2D nodal representation of a neuron. The model is scalable for different neuron geometries and action potential signal durations. In chapter 5, the model is fitted to real extracellular microelectrode recordings. The simulation is then used to determine the electrical characteristics of the extracellular source signal for a range of neuron sizes and neuron-electrode coupling configurations to determine the electrical requirements fro an optimised measurement circuit.

Chapter 6 develops the electrochemical theory of the electrode-electrolyte interface for biological systems and a model is formed to describe the ac and dc electrical properties based upon the literature. Chapter 7 investigates the ac and dc properties of thin film platinum and gold electrodes presents a set of experimental results and an empirical model that characterises this interface. It is then demonstrated that the most challenging aspect of the interface, the interface offset potential, may be removed by careful selection of the input characteristics of the measurement circuit. This method exploits the large capacitance of the electrode to remove the need for dc blocking capacitance at the input. A design method is developed to ensure that the low level neural signal is preserved as the offset is removed.

The third part of this thesis, consisting of chapters 8 and 9, proposes an area efficient design for an active MEA front end. The design utilizes the capacitive properties of the electrode interface developed in chapter 7 to reduce the area of the circuit on silicon. The

resulting amplifier front end may be fabricated for neural measurement at much higher spatial densities. The device bridges the spatial recording gap between single transistor input devices and full amplifier devices while retaining the low power and high signal recording quality of full amplifier devices.

Chapter 8 develops the front end into a compact CMOS transistor based circuit. The process of schematic design and simulation for the selected CMOS process is discussed along with layout implementation. Chapter 10 considers the overall layout of the device and the additional circuits required to give functionality as a stand alone neural monitoring device. A 16 and 256 element array layout is presented for test and packaging. Issues are considered for biocompatibility and application. Chapter 9 considers the device floorplan and packaging development to allow for versatility within *in vivo* and *in vitro* use. The issues of high thermal power dissipation are discussed as device compactness and on board sampling and digitization functionality is added.

The thesis is concluded in chapter 10. An overview of the thesis is given and the achievements of the work are highlighted. The features and benefits of the design are discussed and possible future challenges to such devices are highlighted.

1.2 Introduction to Neurophysiology

To the engineer, close inspection of the living cell shows an amazing system of complex mechanical and chemical processing that is based upon the efficient manipulation of environmental charge carriers. At the fundamental cellular level, it may be shown that nature harnesses the charges of different chemical and ionic particles to perform absolute functionality; from replication to locomotion and inter-cellular communication.
Although we are composed of billions of these composite cells, we are oblivious to their operation and properties in our natural state. Their existence and functionality has only become apparent to our consciousness due to the explorative observation of physiological

researchers who have endeavoured to understand the fundamentals of our physical operation.

This section outlines some of the basic concepts of neural physiology that creates this functionality and develops the basic theory of the electrophysiological phenomenon whereby we may study their behaviour.

1.2.1 Classification of Cells

There are many different cells within nature, each identified by their morphological and behavioural traits. Some exist in isolation and others exist collectively. This thesis is concerned with the classification of cells known as neurons. Neuron is the descriptive name for electrically excitable cells that form the nervous systems and process and transmit information. Due to the electrical excitability of these cells the researcher may monitor and stimulate them by electrical means. This allows a method of direct study that is not present with other cell types.

Neurons may be sub-categorised into the sub-group of the central nervous system (CNS) or the peripheral nervous system (PNS) depending upon its position in the nervous system hierarchy of the host organism.

Neurons are differentiated into different sub-groups, depending on their placement in the body and the cells that surround them. The morphology of each can be very different given the task it is required to perform, this includes size, number of connections and dendrite and terminal configurations. Some have few dendritic branches; others are highly branched and receive large amounts of signal data. Typical neuron sizes are illustrated in figure 1.1.

The afferent PNS can be loosely split into the sensation gathering receptor cells and projection neurons, with their distinct elongated axons that carry the signals to the CNS.

Receptor cells, such as the auditory hair cell, olfactory granule cell and the retinal bipolar cell are generally termed intrinsic neurons and have very little or no axon protrusions but many terminal branches. As a general rule, afferent cells do not require dendritic inputs due to their depolarisation on physical stimuli such as light, pressure, temperature, etc.

Efferent neurons that provide motor function are generally much larger than their afferent counterparts. These cells typically have axon protrusions many tens to thousands of times longer than the diameter of the constituent soma. The purpose of these cells is the stimulation of end effectors throughout the body's extremities providing the recruitment of muscle fibre. In humans single axons can be up to a metre in length, as found in the sciatic nerve trunk, for the routing of axons beyond the spinal cord to the extremities. Large axons of this kind are typically wrapped in myelin sheaths.

Neurons within the CNS typically follow the general neuron structure given in figure 1.3. They are densely packed and necessitate many connections, resulting in many dendrite outgrowths and connective axon terminals. Purkinje cells in the cerebellum, for example, can have over one thousand dendritic branches.

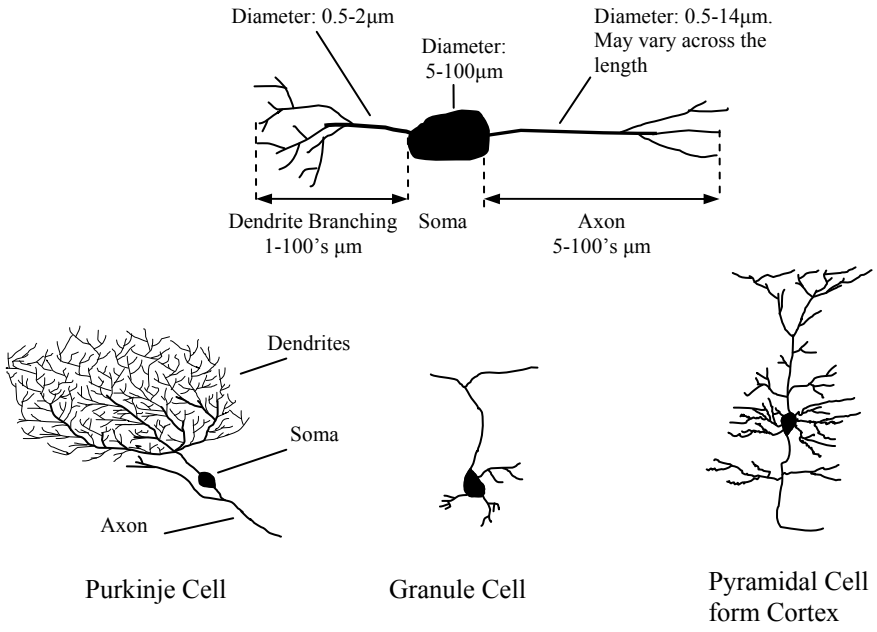

Fig 1.1

Illustration of generic cell dimensions and a selection of CNS neuron cell types.

The cells are structured within a matrix of glial cells that shape their growth and provide myelination. The axons of CNS neurons vary in length depending on function and the connections required, but are typically no longer than a few tens of microns.

1.2.2 The Molecular Structure of the Cell

Biological cells are complex systems of molecular building blocks that provide protection and functionality within the natural environment. It is believed that life developed amongst the planet's abundant surface waters and as a result it is geared to operation within such conditions. In essence the cell is an enforced compartment with an aqueous interior that is physically separated from its surrounding electrolyte. The barrier presents a control over the flux of solute particles and is termed the cell membrane. The interior electrolyte is termed the intracellular fluid and the exterior is termed the extracellular fluid.

The barrier is formed by two layers of phospholipid molecules. Phospholipids present asymmetrical properties over their length; they have an electrically charged 'head' and an uncharged 'tail' that influences the behaviour of the surrounding water molecules. The structure is commonly referred to as the 'hydrophilic head' and 'hydrophobic tail' of the molecule. As water molecules are dipolar (they possess a net positive charge on their H_2 and net negative charge on the O) physical forces will present themselves when the two molecules are brought in contact. Due to these forces, the lipid molecules spontaneously orient themselves, forming a bi-layer with a depth of approximately 10nm. The lipid bi-layer is structured with the hydrophilic heads presented to the water molecules and the hydrophobic tails facing inwards, ensuring an impenetrable barrier between the intracellular and extracellular fluid. The structure is illustrated in figure 1.2. The tails of the lipids form an oily core which is also impermeable to polar, non-organic molecules or ions. Small non-polar molecules such as O_2 may pass through this layer due to their partial solubility within lipids.

Smaller quantities of other various lipids and proteins are moved into the phospholipid tail structure that structurally stabilise the membrane and allow the cell to distort in a fluid like manner while maintaining integrity, or promote rigidity as and when required. Such proteins are what form the basis of cell morphology, cell division and movement and are discussed further in section 1.2.3. Other proteins form carriers that shuttle nutrients and ions across the membrane or provide a selective ionic pathways that operate under mechanical, electrical or chemical stimulus. It is these protein types that enable the electrogenic properties of the neuron.

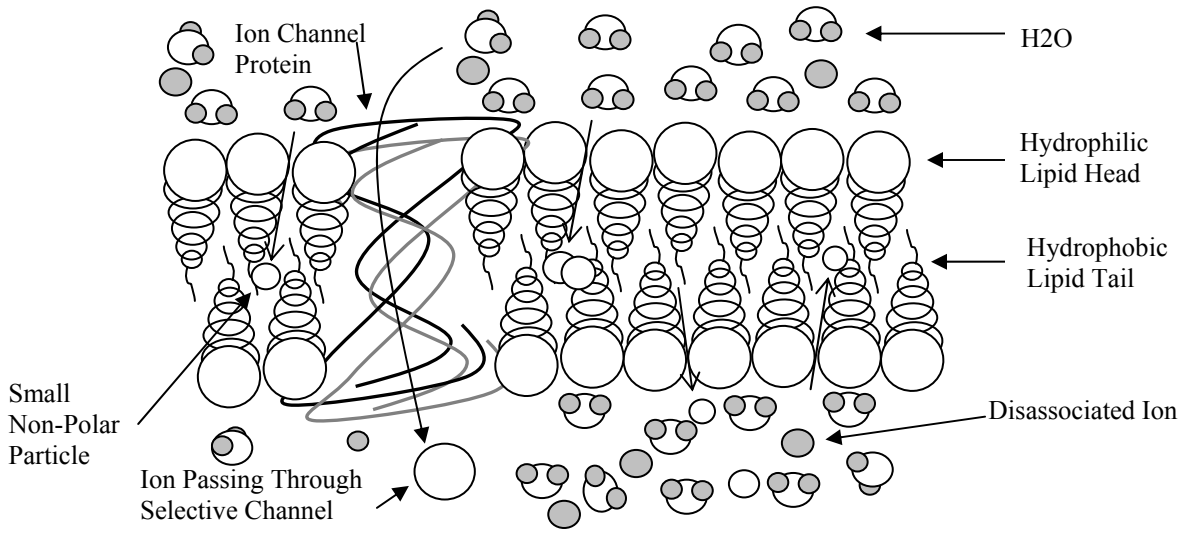

Figure 1.2

Arrangement of the lipid bi-layer that is the basis for the plasma membrane, separating the intracellular fluid from the extracellular plasma. the diagram also shows the peripheral arrangement of selected ions.

The intracellular fluid within the lipid membrane contains the cells functional parts. These are termed organelles and consist of the nucleus, endoplasmic reticulum, mitochondria, lysosomes, etc. In eukaryotic cells (animal cells) these components may be compartmentalised within the cell by further membrane structures.

As the work presented in the thesis is more concerned with the direct properties of the membrane the organelles will not be described further. For more information on these cellular components the reader is referred to the texts [1, 2, 3].

1.2.3 Cell Locomotion and Adhesion

It is commonly noted that mature neurons and developing neuroblast precursors do not remain at their point of genesis and migrate to their functional position. This fact is important in the consideration of developmental cellular study *in vivo* and especially in cultured *in vitro* preparations. This phenomenon is caused by proteins within the cell such

as tubulin and actin whose branching filaments form its structural skeleton. In neurons, locomotion is directly controlled by the constriction of structural actin bundles and polymeric extension of the tubulin proteins by the interaction of enzymes such as myosin and the hydrolysis of ATP. In the basic cell locomotion process the extension of the tubulin microtubes from their anchor point in the nucleus locally stretches and extends the lipid cell membrane to form a small outgrowth known as Lamellipodia. These structures have been observed to bond to other cells *in vivo* and substrates *in vitro*. The cell moves to this new anchorage point by actin constriction and de-polymerisation of the microtubulin. It is by similar processes that functional cell structures such as axons and dendrites are formed.

The bonding of the cell to the substrate occurs as a result of the properties of the extracellular matrix that is composed of lipids and collagen proteins. Certain protein types within the matrix such as fibronectin are believed to form strong bonds with the cells surrounding environment. As portions of the extracellular matrix come into contact with the substrate, oval foot like structures emerge of approximately 1μm known as focal adhesion points. These adhesion points are generally extended from the cell by several nm and are structurally connected to actin bundles within the cell via transmembrane proteins. These adhesion points are believed collectively to form the ohmic seal observed between electrogenic cells and measurement electrodes. This seal has been determined experimentally within the range of 100 kΩ to 5 MΩ [4, 5].

Neurons tend to migrate in accordance to the surfaces and structures of their immediate surroundings. In the *in vivo* environment neural growth is directed by the glial cells which also serve to hold the cells in a fixed orientation to one another and relative to their functionality within the organism.

The study of dissected excitable cells is generally more predictable for this reason; mature hippocampal slices retain their glial enforced cellular structuring as do retinal dissections, allowing fixed positioning of the neurons over their experimental lifetime.

Cultures of isolated neurons have been grown specifically for in vitro study since the late 1960's. Typically such cultures, being absent of glial guidance, tend to grow randomly and with sub optimal connection rates between the synapses of neighbouring cells. When fully grown the cells may also continue their migration to a limited extent across the containing substrate.

1.2.4 The Layout of the Cell

A generic neural cell is shown in figure 1.3. The neuron is formed by the lipid by-layer and structural proteins that give it a shape that may be identified by several distinct compartments. The largest of these is the cell body or Soma. This is the main functional compartment of the cell and presents a spherical shape with a physical diameter of approximately 10 μm to 150 μm. The Soma contains the nucleus and the bulk of the functional proteins and organelles required for operation. Developing cells originate from spherical neuroblast precursors of the simple Soma shape and grow thin tubular extensions known as Axons and Dendrites as they form for functionality in their environment.

Dendrites are branching 'tree-like' processes and form the 'input' of the cell. The Dendrite branches form the input to the cell and contain chemical sensitive proteins at their tips that register neurotransmitter that is released locally by the axon terminals of other neurons. The signals activate a regenerative electrical response signal, known as the action potential that passes through the branches and the Soma into the axon. Neurons typically display many long complex Dendrite branches that form neurotransmitter sensitive connections with neighbouring neurons.

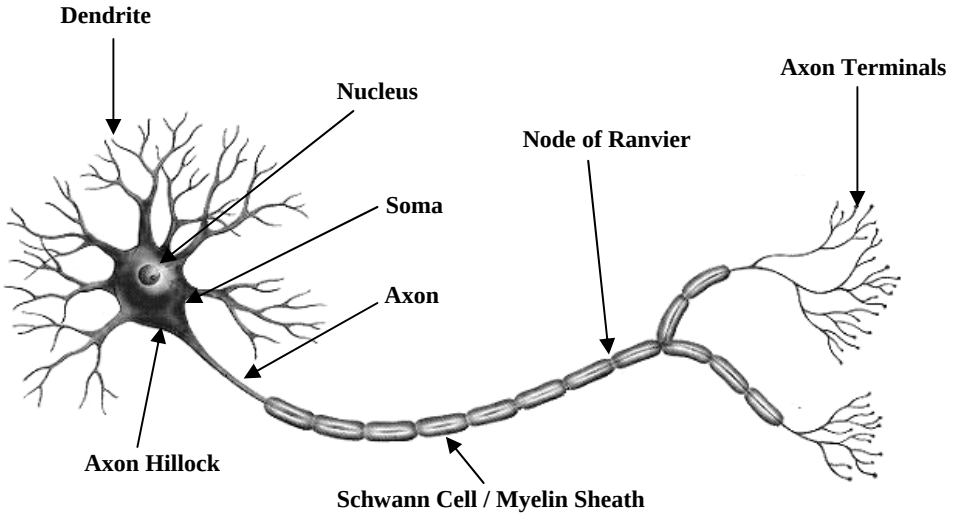

Figure 1.3

A typical neuron

The axon is physically cylindrical in shape with diameters ranging from 1-20 μm [6] in vertebrate neurons, depending on its connection or function, to 20 μm - 1 mm in invertebrate cells. Axons can be found in lengths of several micrometres up to tens of centimetres. Axons are generally found grouped together in protective bundles or cords commonly described as 'nerves' e.g. the ulna and radial nerves in the human forearm. In these cords, protective tissue known as Myelin that is formed by Schwann cells, are wrapped around the constituent axons forming an insulating barrier to ionic flux across the cell membrane (see section 1.2.3). At frequent intervals of up to a few millimetres, gaps known as nodes of Ranvier between the neighbouring myelinated cells are present, and are important in the conduction process along the length of the axon for certain neurons.

The axon terminals are a series of outgrowths that branch out from the cell at the end of the conduction path. These terminals function as signal relays between cells of a specific pathway or grouping. The dendrites and axon terminals of such cells are separated by a fine channel known as the synaptic cleft. In order for communication to occur between neurons, an electrical impulse must conduct through the axon to the terminal. When received the impulse triggers the release of vesicles containing neurotransmitter from the

pre-synaptic ending of the terminal into the synaptic membrane. The vesicles then release a chemical known as neurotransmitter into the synaptic cleft, which proceeds to diffuse across the cleft, binding with receptor sites on the dendrite and postsynaptic ending of applicable neurons.

When the neurotransmitter binds to a receptor on the dendrite it modulates the cells excitability, either making it more or less susceptible to initiating an impulse. A large enough concentration of neurotransmitter received at the postsynaptic ending will itself initiate an impulse or 'Action Potential' within the neuron and continue the propagation of the preceding cells' signal. It is in this manner that neurons communicate and process data; tasks such as pattern recognition, decision making and memory are all performed by large numbers of neurons interacting in structures often referred to as neural networks. A basic summary of this cellular signal flow is illustrated in figure 1.4 below.

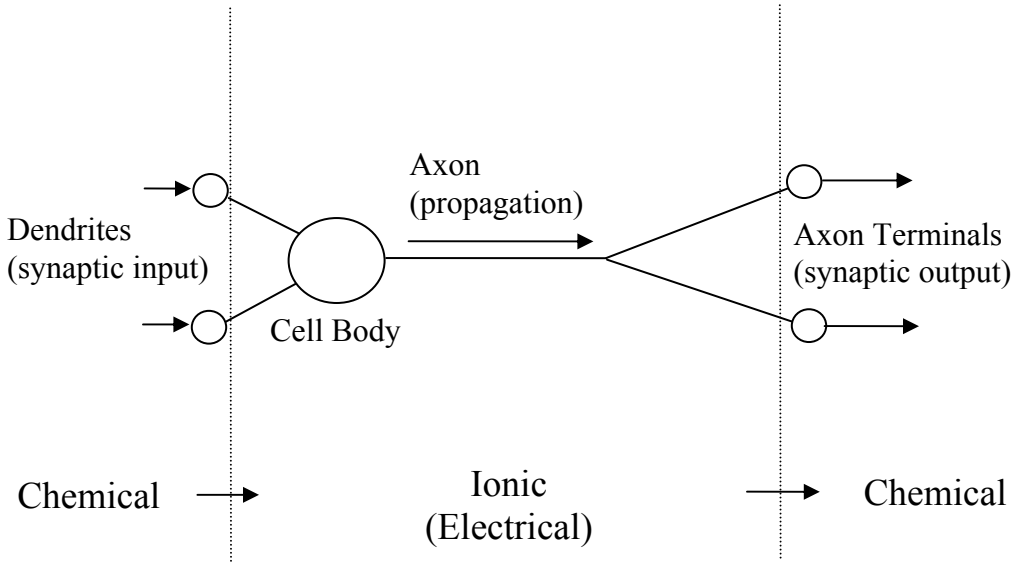

Figure 1.4

The basic mechanism of cellular communication. for sensory cells the dendrites are replaced with specialised sensory elements around the cell body

1.2.5 Other Important Cells

The neural cells within both the CNS and PNS are surrounded by satellite cells that protect and can aid or provide additional functionality. These cells are termed Schwann cells in the PNS and Neuroglial cells in the CNS. These cells do not form Action Potentials as the active neural cells do, although they do contain similar membrane structures, complete with ion pumps, ion channels and neurotransmitter receptors.

Schwann cells and Neuroglia are generally found tightly packed with neural tissue. The cells types are usually separated by tiny fluidic channels in the order of 20nm wide, constituting the neurons extracellular fluid reservoir. These cells work interactively with the neurons, secreting the necessary ions and nutrients into the neurons extracellular reservoir and absorb excess transmitters and ions.

In the PNS the Schwann Cells provide myelination, wrapping themselves around the developing cells axon as it grows. The functionality achieved by this cellular cooperation is a manifold increase in axonal conduction velocity of the nerve impulse. The Schwann cells also provide a guide to growing neurons, directing their growth to achieve functional and structured connections. This process defines the multiple neural pathways seen in nerve trunks, whereby hundreds of thousands of large axons are wrapped in a protective series of Schwann cells. A typical example of this structure can be seen in the human Ulna or Radial nerves.

A similar function is also provided by the Neuroglia. In the brain it is estimated that over half of the cells present fall into this category of cell. The cells have been observed to aid neural connection and guide neural axons to their target connections.
A subdivision of these cells termed Microglia, aid the repair of damaged neural tissue by occupying affected areas and processing the dead matter or removing or enveloping the source.

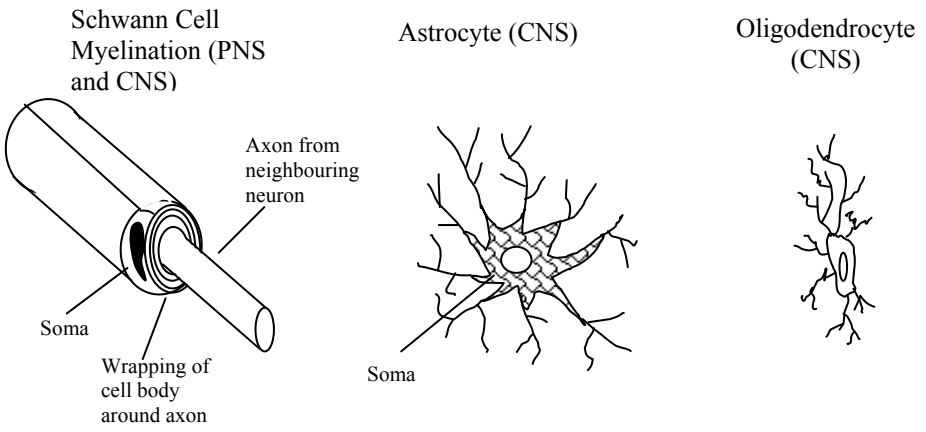

Figure 1.5

Illustrating the form of Schwann cells and neuroglia

1.2.6 Charge Manipulation for Communication

The functional behaviour of the cell membrane has been identified to be provided by the inclusion of function specific proteins within its structure. These proteins are most important to neural signal conduction and traverse the bi-layer to form an aperture selective to certain types of ion. Selectivity is achieved by the protein having a charged head and fixed structural diameter. Sodium and potassium channels would thus have a negatively charged head and a sizing relative to the ionic diameter of the respective ion, whereas chlorine channels would conversely have a positively charged head.

There is a further subdivision of proteins that deform in the presence of a chemical, mechanical, heat or electrical stimulus. These are termed gated channels, and will only allow a specific ion to cross the barrier under given conditions. Such cells are shaped as to either block or permit the passage of ions, depending on their exact function and distort when the stimulus is applied to provide the opposite gating function. Further to this, more complex proteins can act as ionic pumps pushing charges through the membrane against any opposing potential difference between the inner and outer fluids due to uneven ionic distribution. A common example of a metabolic pump is the Na-KATPase protein, that

hydrolyzes ATP as energy to exchange a 3:2 ratio of Sodium to Potassium ions across the membrane. Such proteins are generally termed ‘electrogenic pumps’ due to the creation of a potential gradient across the cell membrane.

1.2.6.1 Resting Potential of the Cell Membrane

Neurons maintain an ionic concentration gradient between the intracellular and extracellular fluids. This, together with the ion specific channels spanning the membrane, causes diffusion of the ionic species down their given concentration gradient and a resulting electrical charge separation. This effect results in a dynamic equilibrium between ionic diffusion and electrical drift that creates a static membrane potential that is related to the concentration gradient.

Generically cells and their surrounding fluids contain a number of ions and polar molecules. These are abundantly sodium (Na^+), potassium (K^+), and chloride (Cl^-), however, calcium (Ca^{2+}), magnesium (Mg^{2+}) and bicarbonates (HCO_3^-) are additionally present in much smaller concentrations, as are polar proteins and glucose which also contribute to cell function. At rest, neurons generally contain a constant surplus of K^+ ions relative to the surrounding extracellular fluid and lack of Na^+ and Cl^-. The result of this is a constant potential difference across the membrane. Table 1.1 lists the Equivalent Molar concentrations of the four main ionic species responsible for the resting potential in the invertebrate squid. The apparent positive charge surplus in the intracellular fluid is balanced by bicarbonate ions and negatively charged amino acids spread throughout the solution. The negative charge excess in the extracellular fluid is similarly balanced by Magnesium ions and H^+ shifting the pH of the solution.

	Intracellular Concentration (mM)	Extracellular Concentration (mM)
Potassium (K^+)	400	10
Sodium (Na^+)	50	440
Chloride (Cl^-)	60	540
Calcium (Ca^{2+})	10^{-4}	10

Table 1.1:
Concentration of ionic species for squid axon [7]

The passive state of an impermeable membrane containing ion-specific channels is one of dynamic equilibrium, in which a definite membrane potential exists due to the effects of selective diffusion. This can be understood by considering a solution with an arbitrary concentration of a dissolved salt. When initially placed in the solution the ions will disperse down the concentration gradient until an equal amount of ions per unit volume is reached, i.e the concentration gradient throughout the solution is zero, and the ions of opposing charge arrange themselves so as to create a net neutral charge.

If this solution is then placed adjacent to another solution of the same solvent with a lesser concentration solute and the barrier is lifted between them, we will find that in a short time both solvent compartments will contain an equal concentration of the solute. If however, we immediately separate the compartments on contact, with a membrane permeable only to a single ionic species of the solute, an interesting process occurs. The particular species, being able to diffuse across the membrane in to the solution of lower concentration takes its charge across the barrier with it. This creates a state of charge imbalance in the solution of the first compartment from the vacancy of the balancing charge. The second compartment will also see a surplus of charge and a potential difference occurs between the solutions. An electric field is thus set up across the membrane in opposition to the diffusion gradient, causing a drift of the charges back into the original compartment.

The constant resting potential of this cell is the resulting potential required to create a dynamic equilibrium of net charge transfer equal to zero, with diffusion current equal to the drift current across the membrane. Thus a highly localised charge distribution is created either side of the membrane, demonstrating the essential force harnessed by the cell to do work.

For any ionic species, this equilibrium potential (V_{eq}) can be calculated by the Nernst equation:

$$V_{eq} = \frac{RT}{zF} \ln \frac{[C]_o}{[C]_i} \qquad 1.1$$

Where R is the gas constant, T is the absolute temperature, F is the faraday constant and z is the valence or fundamental charge of the species. With respect to position $[C]_o$ is the outer or extracellular concentration and $[C]_i$ is the concentration of the reference or intracellular solution.

Using the concentrations for Potassium, given in Table 1.1 at a laboratory temperature of 21ºC, we find that $V_{eq} = -91.4mV$.

The negativity of V_{eq} signifies that the intercellular region is negative with respect to the reference extracellular fluid. The inverse is true for positive V_{eq}.

The work of Goldman in the early 1940's [8] modified the ionic theory outlined in the Nernst equation to apply to the situation of the multi-species biological cell. His description assumed that the electric field across the membrane was constant and resulted in the following ionic current $[I_s]$ equations for the three main species: (note a full derivation of this can be found in the text [9])

$$I_K = \frac{P_K E F^2}{RT} \frac{[K]_o - [K]_i e^{EF/RT}}{1 - e^{EF/RT}} \qquad 1.2$$

$$I_{Na} = \frac{P_{Na} EF^2}{RT} \frac{[Na]_o - [Na]_i e^{EF/RT}}{1 - e^{EF/RT}} \quad 1.3$$

$$I_{Cl} = \frac{P_{Cl} EF^2}{RT} \frac{[Cl]_o - [Cl]_i e^{EF/RT}}{1 - e^{EF/RT}} \quad 1.4$$

Here, E is the change in membrane voltage away from equilibrium and the P_s term is the permeability constant for the relevant species and is described as the speed of diffusion for the proportion of the species that is in the membrane.

P_s is defined in units of cm s^{-1} :

$$P_s = \frac{D_s \beta_s}{dF} \quad 1.5$$

Where D_s is the Diffusion constant of the species and β_s is the proportion of the bulk concentration present in the membrane. F is the Faraday constant, and d is the thickness of the membrane.

It can be expressed that the net current across the membrane as a result of these three separate species is:

$$I_T = \frac{EF^2 P_K}{RT} \frac{\alpha - \chi \cdot e^{EF/RT}}{1 - e^{EF/RT}} \quad 1.6$$

$$\text{where } \alpha = [K]_o + \frac{P_{Na}}{P_K}[Na]_o + \frac{P_{Cl}}{P_K}[Cl]_i \quad 1.7$$

and $\chi = [K]_i + \frac{P_{Na}}{P_K}[Na]_i + \frac{P_{Cl}}{P_K}[Cl]_o$ 1.8

when the membrane potential stabilises due to the drift current being equal to that of the diffusion current, I=0. When I = 0; $\alpha - \chi \cdot e^{EF/RT} = 0$, thus the transmembrane potential becomes:

$$V_r = \frac{RT}{F} \ln \frac{P_K[K]_o + P_{Na}[Na]_o + P_{Cl}[Cl]_i}{P_K[K]_i + P_{Na}[Na]_i + P_{Cl}[Cl]_o} \quad 1.9$$

Equation 1.9 is commonly referred to as the Goldman-Hodgkin-Katz equation, and reverts back to the Nernst Equation (1.1) when $\frac{P_{Na}}{P_K} = \frac{P_{Cl}}{P_K} = 0$

A major assumption of equation 1.9 is that the concentrations of the intracellular ions remain constant.

This state would not be possible in a purely inactive system especially when it is considered that the measured resting potential of a mammalian neuron would not allow an equilibrium state. The neuron requires a further mechanism to 'top up' the Potassium levels and reduce the climbing Sodium levels within the intracellular fluid due to the equalisation down the ions respective concentration gradients as the positive ions interchange. These molecular 'charge pumps' either operate electrogenically, using the charge of the ions to flip it across the membrane or by expending ATP; with the reduction of the molecule at the metabolic pump providing the force for exchange.

The understanding of gating channel proteins and charge pumps are a complex sphere of much current research and will not be covered further here; it being sufficient to understand that their presence provides conservation of energy for ionic depletion within the system.

1.2.6.2 Depolarisation as a Signalling Mechanism: The Action Potential

From equations 1.6 through 1.9 the Sodium hypotheses of the neurons signalling mechanism were developed. The physical signal itself possesses a very distinct shape when measured that is termed the Action Potential of the cell.

Membrane depolarisation will only occur upon the recruitment of a sufficient proportion of active voltage gated Na channels. Channels move from a closed to open state, or vice versa upon the force of an electric field elicited from the localised ionic charges in their vicinity. This can be quantitatively analysed using Hodgkin and Huxley's explorative analysis of the giant squid axon [10] based upon calculations of the gradient of the voltage dependence of gating.

The necessity of this recruitment defines a certain threshold potential with which a given number of channels are opened, sufficient to overwhelm the charge pumping of the electrogenic and ATP powered exchange proteins. The resting potential held by these metabolic pumps is then lost across the membrane and the cell is momentarily 'depolarised'. Upon depolarisation, the potential gradient is lost across the voltage gated channel and ions cease to diffuse across the membrane. With the absence of the potential gradient the channel returns to the closed state and the resting potential is quickly re-established by the ionic pumps. This process follows quite a distinct potential waveform with respect to time, commonly referred to as the Action Potential. This is due to the voltage responses of the two main ionic pathways; that of Sodium and Potassium. The shape of the action potential is given in figure 1.6 below.

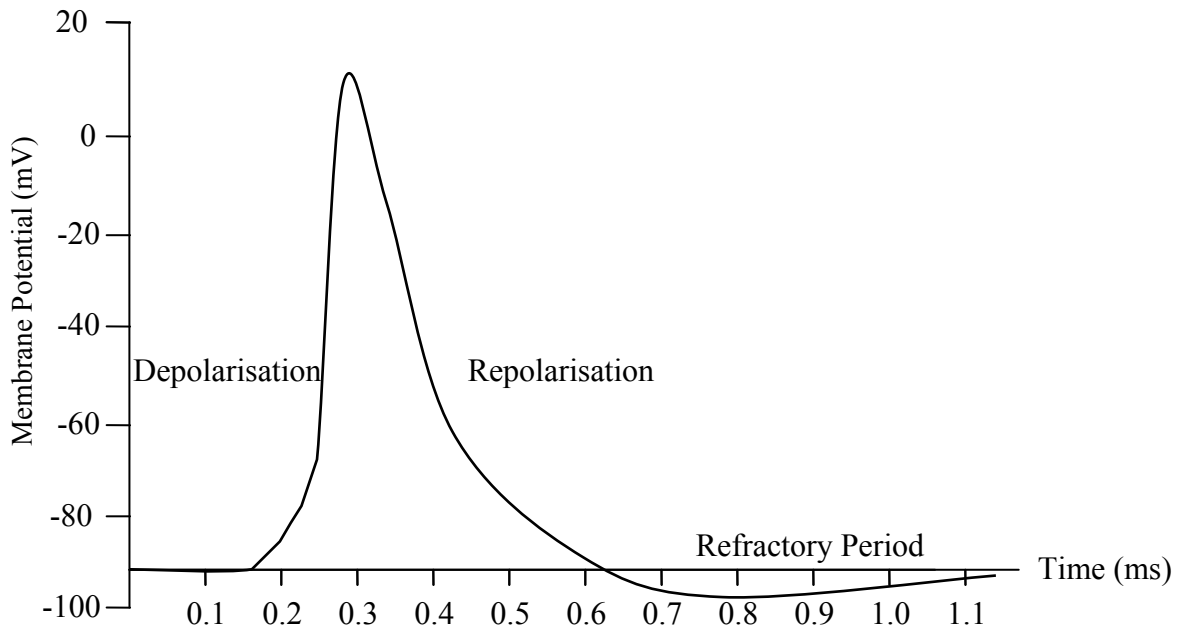

Figure 1.6

Typical shape of an action potential

The role of the membrane proteins in the depolarisation and repolarisation process is summarised in figure 1.7. The re-polarisation process generally occurs over a time period several times that of depolarisation giving the Action Potential its distinct shape.

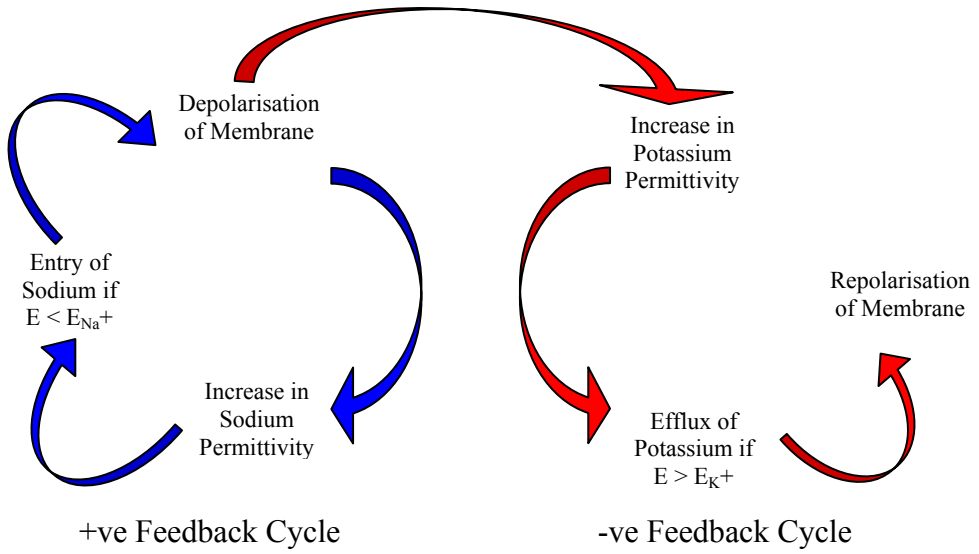

Figure 1.7

The sodium cycle theory of membrane depolarisation and the potassium cycle theory of aided repolarisation

1.2.6.3 Propagation of the Action Potential

The localised initiation of an Action Potential in the cell membrane of an excitable cell will trigger a propagating wave of similar form throughout the rest of the membrane. Under typical conditions, initiation of the Action Potential depolarisation process within a given area of the membrane will provide sufficient charge movement from adjacent areas of the membrane to drive their potential past the threshold and continue the depolarisation process down the length of the cell. By this method the cell can relay a stimulus event from the dendritic synapses to its axon terminals over relatively large distances without incurring cable losses or signal corruption from environmental electromagnetic disturbances.

1.2.6.4 The Influence of the Soma

The Soma is the control point of the cell. It contains the nucleus, structural proteins, mitochondria and other organelle essential for reproduction, respiration and basic cellular function. However the Soma also plays an important part in the communicative recruitment of the neuron. The axons and dendrites of a neuron serve as communication pathways and route stimulus in and out of the Soma in the form of the Action Potential. The Soma in many situations may be considered as a multiple input multiple output (MIMO) signal integration block.

The Somas importance to the cellular signal relay process requires its large surface area to contain voltage gated channels, especially in the region comprising the axon hillock where the channel density is much greater. For this reason, the Soma was traditionally, and is often still the main area of electrophysiological examination; having a large accessible, unmyelinated active area.

Invasive cellular potential measurement, such as penetrative voltage clamping and patch clamping, will often concentrate wholly on the Soma for the reasons stated above unless the dendritic or axonal branches are the specific target for study. Extracellular field potential measurement is almost solely concerned with potential dipoles created by Somatic depolarisation currents around the outer circumference of the cell due to the overwhelmingly large active surface area participating with respect to that of the out-branchings. This is especially true in myelinated neurons.

1.2.6.5 Myelinated and Non Myelinated Axons

Typically there are two subtle forms of this signal transmission found in axons. The first occurs as described above; whereby the cell depolarises as an Action Potential wave down the length of the axon. Changes in the localised membrane potential cause the capacitive surface charges built up on the membrane to depolarise. This forms a localised

current due to the transient charge imbalance and in turn depolarises the area of the membrane that has now lost its surface charge. Once this potential change reaches the threshold for voltage gated channel recruitment, the affected area depolarises as did the neighbouring area and the signal is carried down the length of the axon towards the terminals. Back propagation of Action Potentials is inhibited by the duration of the depolarised membranes refractory period. The principle of this propagation method can be seen in figure 1.8(a).

In myelinated axons, the Schwann cells, discussed in section 1.2.1.2, have altered the structure of the active membrane so that the Action Potential currents do not occur uniformly along the fibre. The close proximity of the Schwann cell to the cell membrane effectively breaks up the membrane into small active nodes, termed Ranvier (see Figure 1.3) and larger passive areas where the ion channels are effectively blocked off by the myelin sheath formed by Schwann cells. This provides a more efficient method of signal propagation, needing far less metabolic and voltage gated channels along the axon to occur. The membrane relies upon the conductance of the intracellular fluid between nodes to carry the signal by ionic diffusion. Myelinated fibres can operate at much smaller diameters due to this mechanism and typically propagate signals 10 times faster than non myelinated axons of a similar diameter.

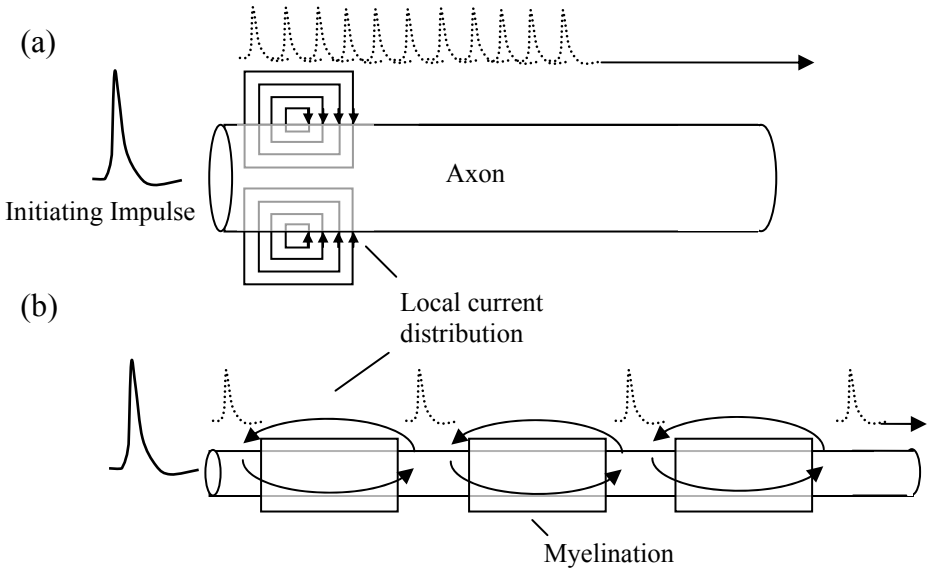

Figure 1.8

Diagram of action potential propagation mechanism in non-myelinated (a) and (b) myelinated fibres

The propagation of the Action Potential now occurs in a modified manner to the non myelinated axon, in that the localised depolarisation currents and more importantly, the magnitude of the resultant field potential, is not hindered by the localised depolarisation spread travelling with it down the axon. The depolarisation of an excited node of Ranvier provides sufficient potential gradient to induce capacitive discharge at the node of the adjacent membrane and activate the voltage gated channels. Once the threshold potential has been reached at the node by this process, the node will depolarise, thus spreading the Action Potential from node to node down the length of the axon. This process is shown in figure 1.8 (b). The myelinated fibre signal conduction process is often termed saltatory conduction, named by Tasaki and Takeuchi from the latin saltare: to jump, leap or dance.

1.2.6.6 Dendrites

The basic function of the dendrite is to encode chemically based signals received at the presynaptic terminals into Action Potential signals via gated channel modulation. Modulation can be active, by direct channel opening or inhibitory, retarding the response of the membrane to stimulus.

Historically the dendritic branches were thought to only provide their electrical stimulus to the cell passively by ionic conduction currents through the intracellular fluid. This has recently been revised to account for the observation of 'hot spots'; small areas of active membrane irregularly placed along the longer dendritic branches. These 'hot spots' are necessary to regenerate the signal by further depolarisation to overcome the relatively high resistance path to the Soma posed by the narrow diameter of the dendrite across lengths that can range between 10's to 100's of microns. Thus, when the signal reaches the Soma it is of a magnitude great enough to exceed the required threshold to initiate an Action Potential.

1.2.7 Electrical Connections and Couples between Cells

In section 1.2.4 it was briefly discussed that communication between neurons occurs by the release and absorption of chemical neurotransmitters in the synapses. The ionic discharge of a cell across the membrane is universally unable in typical circumstances, to force the depolarisation of neighbouring cells due to the severe localisation and the finite charge that actually partakes in this action.

It is worthwhile to note that this is not the only mechanism of neural communication, as to limited extent, electrical communication pathways are available between excitable cells in certain situations. When excitable cells are tightly clustered together in a biological network, a situation can occur whereby a *gap junction* forms. This junction is created by an accumulation of protein based particles, called *connexons,* spanning the cell membranes of the contacting cells and allows ions and small molecules to pass freely.

Electrical conductivity of single connexion molecules has been measured to be 100 pS [11] and such connections are as a rule formed by single or small numbers of these protein bridges.

These electrical synapses are believed to play important roles in coupling the responses of sensory neurons, spinal interneurons and certain motorneurons. Recent findings [12], suggest that the role of electrical synapses within the CNS and brain are extensive and enable adjacent grouped neurons to process information simultaneously in a collective manner. It has been suggested that certain localised communication within the brain does not involve the Action Potential at all and is dependent upon the spread of small synaptic potentials.

1.3 References

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Chapter 2

The Development of Cellular Recording Technology

The focus of this Thesis is the development of an integrated system to provide an efficient method for high resolution monitoring of neural signals. This chapter provides the background for existing techniques that have been developed over more than a century of electrophysiological research. These techniques are quite varied in their fundamental approach to transduce the basic communication method of the cell into a signal that can be easily visualised and analysed by neuroscientists.

The tree diagram given in figure 2.1 highlights the main areas of electrophysiological analysis methods and gives some of the current branches and convergences currently occurring in modern research.

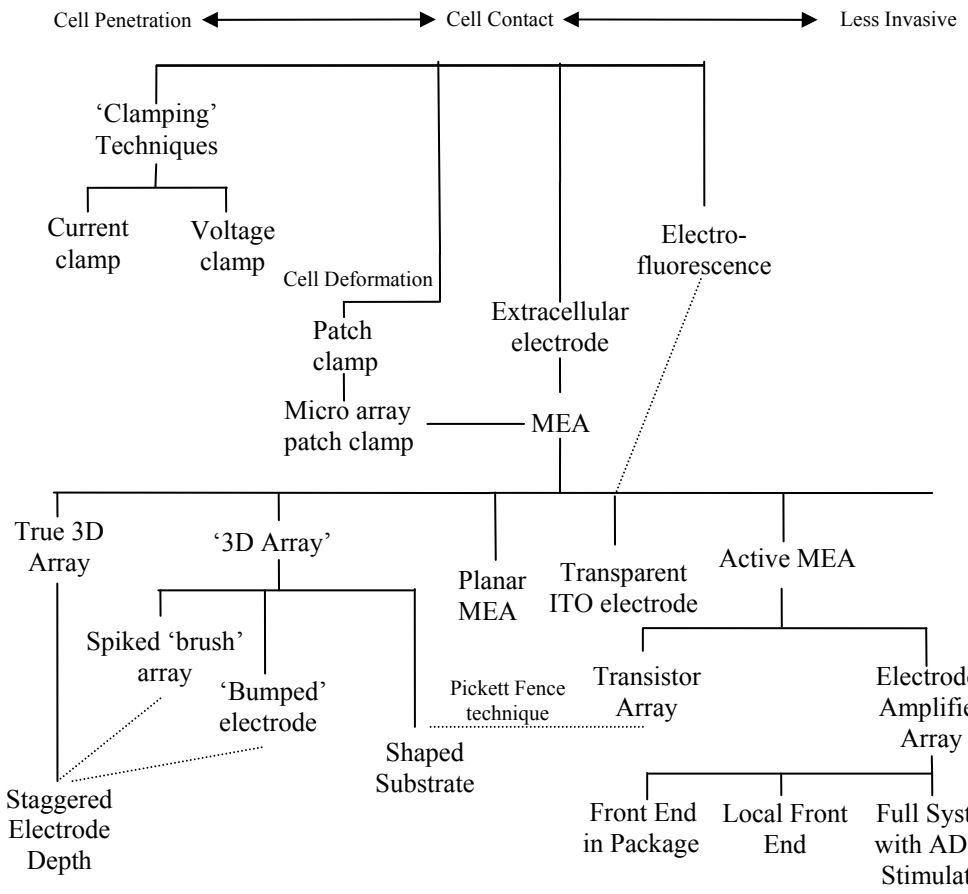

Figure 2.1

The four main branches of electrophysiological research categorised in terms of invasiveness and showing typical links (dotted lines) between methods.

2.1 In Vitro and In Vivo Methods

The preparation of isolated tissues outside the body for analysis has taken many forms throughout the long history of electrophysiological research. From the crude but crucial initial experiments of Galvani [1] in the 18th Century to the identification of axons by Harrison in 1910 [2] and the understanding of excitable membrane functionality pioneered by Hodgkin and Huxley [3] in the 1950's; the increasingly subtle isolation of living functional units for experimentation has provided an invaluable path to understanding the mechanisms of life.

In vitro methods greatly simplify control of the system under study and provide the researcher with a way to focus their study to specific areas of interest, such as cell

responses to pharmaceuticals (both single and multiple cells if required) or even the responses of cell ion channels. They also provide a method to test implantable devices before *in vivo*.

This section introduces a number of methods used by electrophysiologists to extract the electrogenic responses of in vitro preparations that may include cell cultures, tissue slices and isolated nerve trunks or axons.

2.2 Recording Electrodes

Recording electrodes developed from early configurations that recognised the electrical behaviour of the neuron and the conductive properties of the supporting solution. The original experiments typically involved a dissected axon or nerve trunk being placed upon a series of silver wires in a hermetically sealed container [4] or metallic pins penetrating the sheath of an isolated nerve trunk.

As experimental knowledge accumulated, smaller and more electrically stable designs were fabricated and used to gain higher magnitude and lower noise signals, often incorporating the technological advances of the time. In 1949 Ling and Gerard [5] demonstrated the glass micropipette as an electrode, essentially a narrow glass tube filled with an isotonic KCl solution. The tip of the glass tube was drawn to a sub μm diameter, (figure 2.2) allowing single cell fibres to be perforated, from which several hours of recording could be made. Such methods are however limited to the study of relatively large cells.

The above electrode techniques are still in common use today. Due to improvements in the fabrication of micro scale electrodes, it is possible to measure extracellular potentials from single cells taken from cultures or dissections. Better knowledge of materials and electrochemical reactions, which have been developed over the years, has allowed longer sample lifetime and higher electrical matching between the recording device and the cells.

Intracellular measurements are still commonly taken using the glass micropipette, although micrometre or sub-micrometre diameter, penetrating solid state conductive electrodes can also be used. The material of such electrodes must be chosen carefully so as to not decompose into toxic substances that may poison and kill the cells under observation. The term 'bio-compatible' is often used to describe non-degradable electrodes that are metallic, or otherwise, that remain inert within the highly corrosive biological environment.

In this practice the intracellular potential is measured with respect to the extracellular, by the penetration of the membrane, and with the use of a relatively large area externally placed reference electrode. The reference electrode can be protected from movement and other artefacts by containing it in an open ended saline-agar gel chamber but this is not a necessity.

It is desirable for biopotential recording electrodes to have low input impedance and infinite impedance at the measurement device to minimise noise, resistive signal loss and to limit the effects of the recording process upon the small signal potentials created by the finite charge movement across the cell membrane.

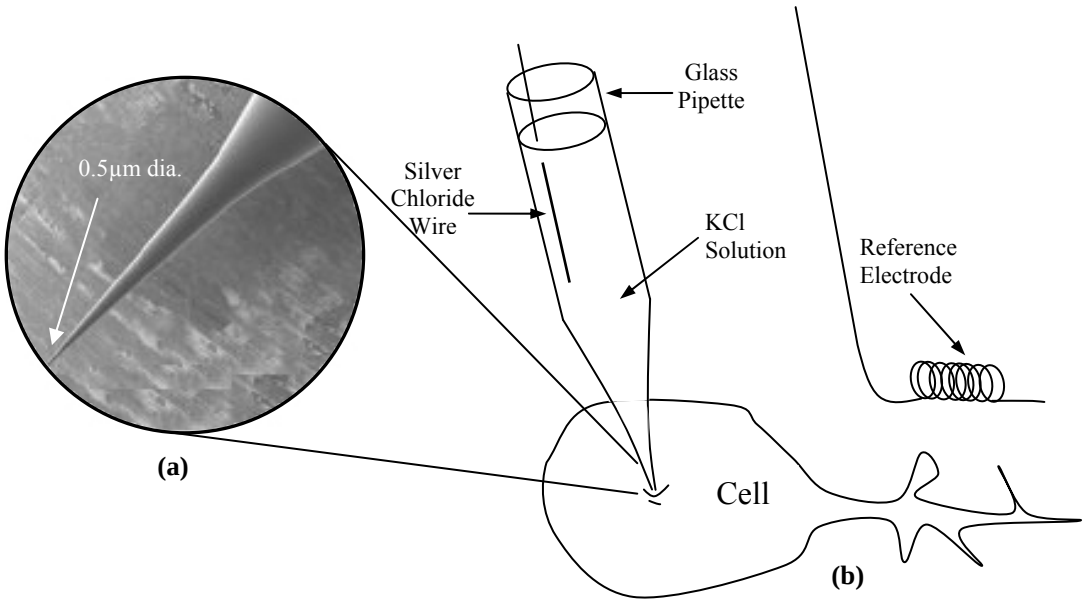

Figure 2.2
The Use of a Glass Micropipette for Intracellular Potential Measurement: (a) Microscope photograph of a typical micropipette, (b) Typical schematic of intracellular penetrative measurement scheme with large area reference electrode.

Many important discoveries were made using these simple electrode procedures, one of particular notice being what is now universally accepted as the typical cell depolarisation shape, or Action Potential. Much information was gathered from the shape and magnitude of the Action Potential which lead to the theory of dynamic ionic channels and provided the means for pioneering researchers such as Hodgkin, Huxley and Katz to develop their empirical models of cell depolarisation of which variations on the basic principles of these models are still used today for prosthetic design [6], pharmaceutical testing and bioinformatics [7].

The recording of the precise shape of an Action Potential was only possible due an important electrode configuration known as the Voltage Clamp. This technique was developed by Cole [8] and Marmount [9] in the 1940's and used a subtle amplifier feedback circuit to hold the cell membrane potential at a level set by the experimenter, as shown below in figure 2.3.

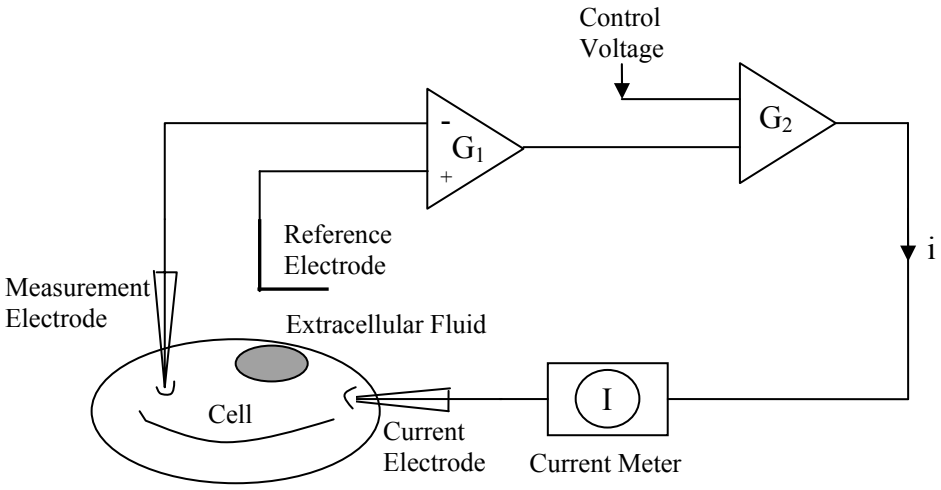

Figure 2.3

Illustration of the voltage clamp measurement configuration

It is clear to see that negative feedback is used to 'clamp' the cell at a user dictated potential. Because the cell potential is held at a constant level there is no capacitive current and the current passed into the cell reflects the response of the ion channels alone.

Upon the initiation of an action potential across the cell membrane, the amplifier magnifies the difference and supplies the cell with enough current to re-establish the membrane potential. Thus a current opposite and equal to that of the ionic current of depolarisation can be measured at the current meter, giving an accurate measurement of the ionic channel response alone.

Using this method, single ionic species pathways were characterised. Experiments were undertaken using toxins that were known to selectively block a particular type of ion channel such as tetrodotoxin (TTX) for Sodium channels and tetraethylammonium (TEA) for Potassium channels and thus measure the current response of the circuit to characterise the remaining active channels.

The current clamp is the electrical dual of the voltage clamp, whereby a forced electric current is applied across the membrane and the voltage fluctuations resulting from ion channel activity are measured. By these methods, the well known Action potential shape can be reconstructed from the measured responses of the cell at different clamped potentials or applied currents.

2.2.1 Planar Electrodes and MEAs

Planar Micro Electrode Arrays (MEA) offer a versatile non invasive technique for biomedical study; allowing the possibility of long term recording from both single cells, large cultures and dissected networks. Using photo lithographic IC fabrication methods, large reproducible arrays of micrometer scale, high dimensional precision electrodes are possible. IC Fabricated MEA's can provide minimal physical length connective leads and recording site densities far greater than that possible using the bulky and somewhat cumbersome methods discussed in the previous section.

Development of planar electrode arrays for biopotential recording began in the late 1960's to provide a means for the concurrent stimulation and monitoring of multiple cells in vitro, from which the often used terms: Multi-Electrode Array (MEA), Micro Electrode Array (also MEA) and Multi Micro Electrode Array were coined. Such devices brought in the consideration of mass production and a high level of feature

reproductability between active electrodes and multiply produced arrays. One of the first existing devices of this nature was a 30 element array of rather large 250 μm diameter electrodes fabricated upon a flexible plastic sheet by medics G.R. Hanna and R.N. Johnson in 1968 [10]. In the successive years, work upon a number of similar devices was published, refining the original etching techniques used in the first demonstrations, following the trend of improvement in microfabrication methods and steering the current designs towards other areas of electrophysiological interest, such as the microfabricated probes of Wise et al. in 1970 [11].

Thomas *et al.* in 1972 [12] demonstrated possibly the first true multi-microelectrode devices manufactured by standard photolithographic methods. A two row, 30 electrode array was produced on a glass substrate with sub 100 μm spaced features.
The fabrication method used by Thomas et al. is still commonly used today and allows the various effective MEA structures to be easily produced with basic microfabrication (or good PCB plant) facilities. The process in its basic form requires two masks. One to characterise the electrode and its connection to the devices output pins, and another to define the insulation of the connective wires and the exposed electrode shape and dimensions.
The metallization layer is usually (as with Thomas et al.) vacuum deposited onto an insulating, biocompatible substrate (usually Glass or Si-SiO2) and then coated with a photoactive polymer. The exposure of the polymer through the first mask and subsequent acidic etching of exposed metallization provides the electrode features with a similar process to insulate the connections and expose the active electrode surfaces. Depending on the type of metal used and its corrosion properties / biocompatibility, further processing steps may be required, as was the case with Thomas et al. where the exposed nickel electrodes were subsequently electroplated with gold and later platinum black before use. This process is illustrated in figure 2.4.

Through the late 1970's and early 1980's further devices using this process were made and work regarding their use was published. Pine [13] developed a cell culture dish with 32 electrodes of approximately 8 μm x 10 μm dimensions to study field potentials of grown cultures of rat superia cervical ganglia. Jobling et al. demonstrated an active microelectrode array in in vitro studies of mammalian CNS [14] and Gross

et al. fabricated a transparent electrode MEA using indium-tin oxide with an exposed electrode area of 100 μm² using a laser processing step to form the electrode craters [15]. The transparent tracks allowed the device to be used in conjunction with optical methods.

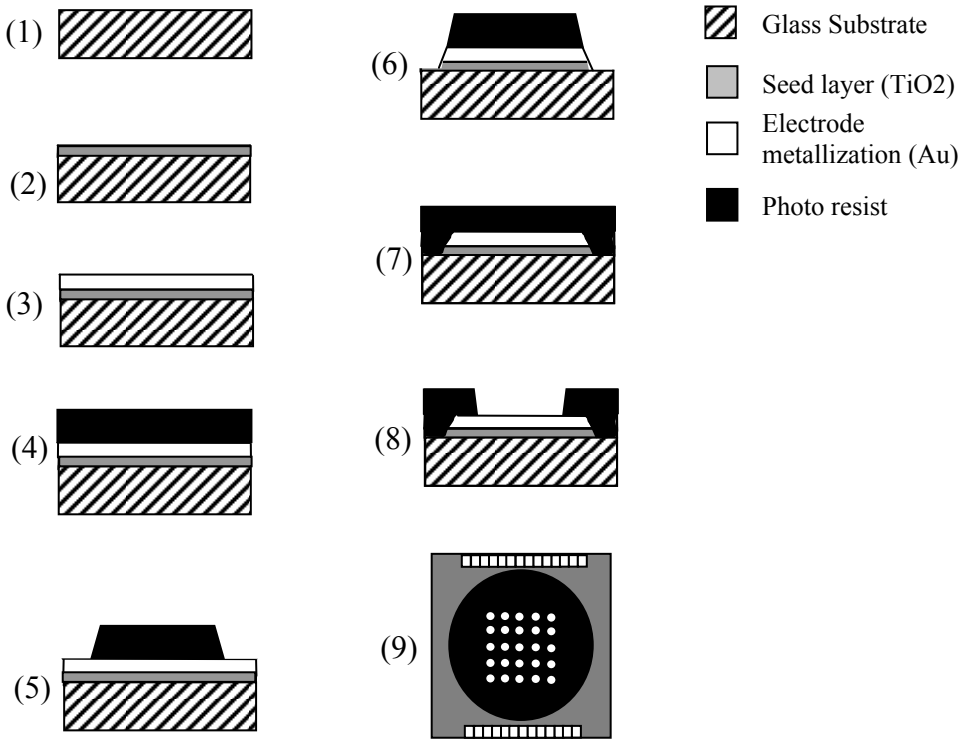

Figure 2.4

Cross sectional illustration of basic photolithographic process. (1) Cleaning of the substrate. (2) Vacuum deposition of seed layer (~2 Å) if necessary. (3) Vacuum deposition of metallization layer (~ 200nm). (4) Application of photoresist. (5) Photo exposure through metallization pattern mask. (6) Etching of metal to form electrodes and connection wires and removal of resist (7) Re-coating with photoresist and photo exposure through electrode feature mask. (8) Etching of photoresist to expose electrode surface. (9) Top view of hypothetical 25 element array.

Over the years such arrays have been steadily refined. Wheeler et al. in the mid to late 1980's developed a reliable 32 channel electrode array recording system from which neural signal processing methods were developed [16, 17, 18, 19]. The array consisted of an 8 by 4 matrix of 20 μm diameter electrodes, with 200 μm spacing centres. The devices were formed using conventional fabrication methods, with polymide surface

insulation and platinized electrodes. This group later began development of flexible porous electrode arrays to improve the signal quality for their experimentation on hippocampal slices [20].

Other work by Regehr, Pine and Rutledge [21] and Regehr et al. [22] in the late 1980's was introduced that used standard IC technologies to increase the connectivity between neurons and electrodes by increasing the so called 'seal resistance' using 'diving board' structures of cantilevers that applied additional force to the neurons, holding them down to the substrate. This work can be seen to approximate the patch clamp method of cell recording and included detailed circuit characterisation of the system for chronic stimulation and recording.

Recently there has been a renaissance in MEA development with many new and subtle applications being published from in vitro drug evaluation [23, 24, 25] to protein screening [26] and research into functionality of physiological processing (brain slice, retinal ganglia), [27, 28, 29]. Non planar surface topologies and neuro-phillic coatings [30] have been developed to promote controlled cellular bonding at the electrode and substrate, and signal conditioning circuitry has been integrated. This is discussed in section 2.4.

Current state of the art MEAs for electrophysiological research provide relatively low electrode impedance of the order of 1 MΩ at 1 kHz, good cellular bonding increasing the electrode-cell seal and use high charge delivery capacity (high CDC) metalizations such as IrOx for high level reversible stimulation of the cell. Some specialised MEAs may provide a transparent substrate and electrodes for retinal study [31] or 3D electrode structures for deeper access to sample as discussed in section 2.2.2. Organic surface coatings are often used to promote controlled cellular attachment.

Much of today's electrophysiological research is conducted using commercial systems that include amplification, data conditioning and acquisition equipment. Such 'off the shelf' devices have been available from a number of sources for well over a decade. Companies such as Cyberkinetics, MeaSystems, Axon, Plexon, and Multi Channel Systems, provide anything from well made in vitro Platinum or Gold electrode array dishes (up to 100 microelectrodes) with connecting equipment to specialised multi-

electrode in vivo devices, complete with high capability processing boxes and computer software to filter and condition the signals developed at the electrode surfaces. Specialised structures and transparent arrangements are also offered by some of these manufacturers.

2.2.2 Non Planar Electrode Arrays.

A subset of MEAs, often for specialised *in vivo* experimentation upon the exposed brain, began to emerge with the advent of the micro-fabricated MEA. These devices are often called 3D or spike arrays and aimed to progress the invasive electrode insertion techniques pioneered in the 1950's [32, 33, 34] by providing easily manufactured components of high tolerance and dense recording sites.
This concept is a fairly new one with respect to the planar array and can be differentiated into two sub domains; the 3D Electrode array which consists of raised, often conical electrodes and Spike or intrafascicular arrays, which exhibit long penetrating spiked shafts much longer than the electrode diameter. Both of these groups can be further differentiated into what is sometimes termed as 'true' 3D arrays whereby a variable depth electrode topology provides the third dimension of measurements.

Three dimensional arrays were developed to counter the problem of dead surface tissue often encountered during the analysis of dissected samples such as brain slices. The fabrication of these electrodes often involves an additional deposition stage to raise the profile of the electrodes in the array. MEA Systems currently offer a commercial Pt array of this type with 40 μm diameter base and 50 μm -70 μm height.

The first true intrafascicular micro electrode array was developed by Kruger and Bach in 1980 [35] to explore the activity of intracortical neurones. A mesh grid substrate of 64, 250 μm spaced electrodes was manufactured using a potting compound to hold the electrodes to the substrate. Although pioneering in its time, the device was very time consuming in the making and difficult to manufacture accurately, regarding electrode precision and height.

The development of micro-fabricated intrafascicular electrode arrays was initiated in the late 1980's by the work of Normann et al. at Utah while conducting acute and chronic studies of multiple point intracortical stimulation [36]. Problems involving the strength and rigidity of platinum/iridium electrodes, control of the electrode height and the drive to simplify the manufacturability of such multi-component devices led to the development of what was later known as the Utah Array.

Normann's group began to develop a process to fabricate so called 'hair brush' arrays from silicon [37] using variations of standard IC fabrication methods to provide separate connectivity to each of the 100 spikes that had been etched into and sharpened on die [38]. The prototype array consisted of 100 square spike electrodes of 1.5 mm height and 90 μm base. A diagram of a typical 3D 'Utah' MEA is given in figure 2.5.

The fabrication of a similar device was published in 1995 by Rutten et al. [39] at Jan Meier's group in the Netherlands. The device used a sawing procedure to micromachine silicon wafers into a series of 128 electrodes on a silicon base. Electrode spacing of 120 μm, 55 μm x 55 μm base and three different height profiles (600 μm, 400 μm, 200 μm) was achieved with iridium oxide tips and silicon nitride (Si_3Ni_4) insulation. This staggered topology of spike depths is often termed a 'true' 3D MEA due to the selectivity to deeper tissue giving a third axis to the devices recording ability.

Cyberkinetics currently supply semi-commercial versions of the Utah Array, including a staggered electrode depth version, that are used extensively for their BrainGate project.

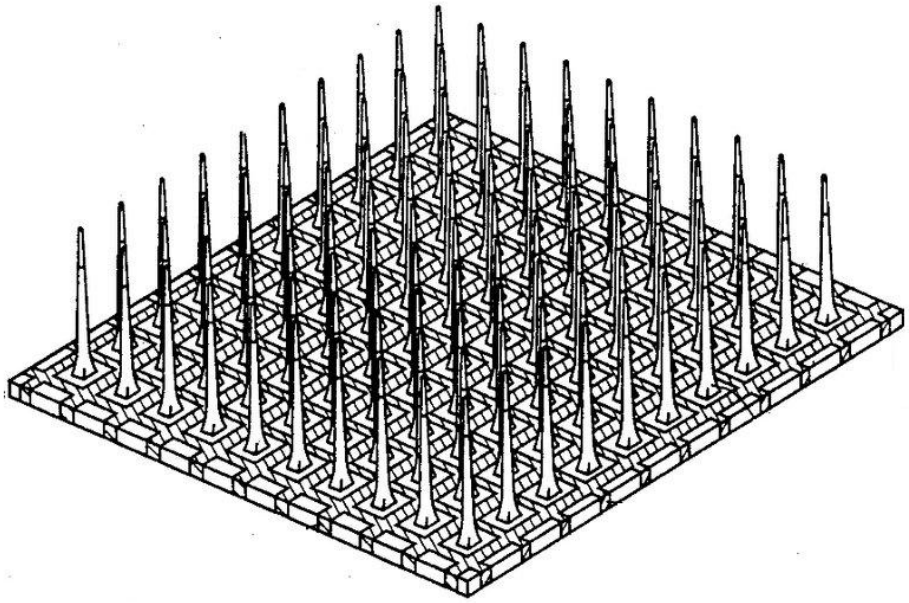

Figure 2.5

The Utah Array: diagram taken from Richard A. Normann's patent application. US Patent #5,215,088: Three-dimensional electrode device

2.3 The Patch Clamp

Patch clamps are essentially the logical conclusion of the application of the micro-pipette electrode developed by Neher and Sakmann at the University of Göttingen in the late 1970's to the early 1980's [40, 41, 42] for which they received a Nobel Prize in 1991. The instant success of the technique meant that commercial versions were available soon after the initial publication.

The device is customarily an open tipped glass pipette, similar to the glass electrodes described at the beginning of the previous section, with a smooth circular drawn end of 1μm or less. The smooth end profile of the patch clamp pipette contrasts from that of the traditional electrode which is usually a sharp point and allows a sealed fit to the cell membrane for ion channel recording.

For cellular recordings, a micropipette controlled by a micromanipulator and microscope arrangement is moved onto the cell membrane. An isotonic solution

mimicking the cells intracellular fluid is placed in the pipette with an immersed metal electrode, as in figure 2.2, and the pipette is pressed against the cell membrane and a low partial vacuum is applied to the pipette. The suction force of this vacuum allows the pipette to form a tight seal on the cells surface membrane, providing a closed measurement system for the channels enclosed by the pipettes tip. The seal is commonly termed the 'Giga-Ohm Seal' due to the equivalent electrical resistance of the seal being in excess of 1 GΩ. The seal lowers the electrical noise contributions at the interface allowing individual ion channels or channels with low conductance to be effectively measured. After the attachment procedure, a bond of high mechanical strength will remain between cell and tip. A diagram of the technique is shown in figure 2.6.

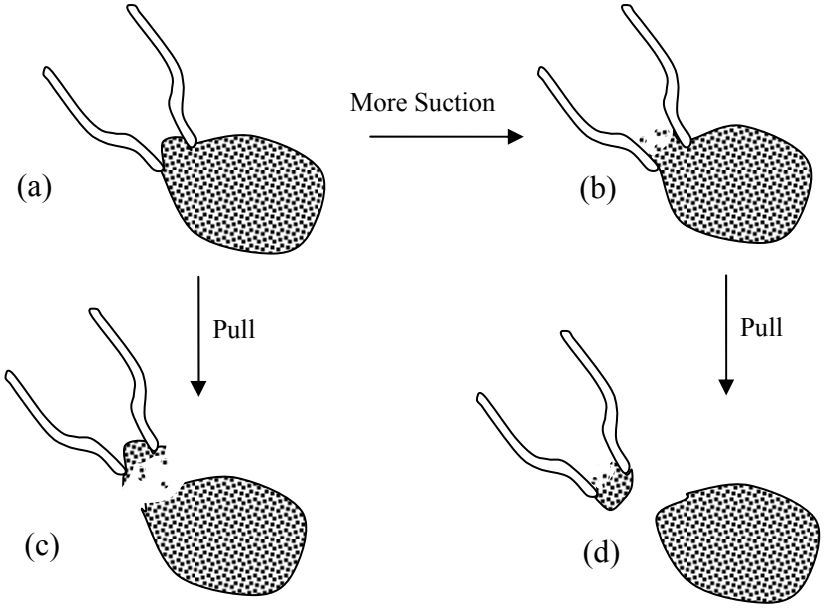

Figure 2.6

The attachment of the tip of a micropipette to a cell in the four patch clamp arrangements; forming the Giga Ohm seal. (a) The Cell Attached Patch, (b) The Whole-Cell Patch, (c) The Inside-Out Patch, (d) The Outside-In Patch. [Adapted from Hille [43]]

The patch clamp can be used in a number of configurations. For research where the cell is not required to remain living as a functional unit and only the properties of the excitable membrane are of concern, the 'Inside-Out Patch' or 'Outside-In Patch' techniques can be used. These methods involve the portion of the membrane that is sucked into the tip being excised from the cell causing cell death. The Inside-Out

Patch causes the membrane to remain attached to the tip, allowing the ion channels to be studied between the fluid contained within the pipette and an artificial intracellular fluid. The Outside-Out Patch involves the careful manipulation of an extracted section of membrane from which a small ball of active membrane forms, shielding the inner membrane from the outside fluid. Such methods are of little relevance to the current work but the interested reader is referred to the following texts for further information [42, 43].

Two further modes of operation are open to the Patch Clamp pipette electrode; the so called 'Cell-attached patch' and 'Whole-cell patch'. With these methods recordings can be made from single living cells, either in isolation or part of a culture.
The cell-attached patch is the original mode pipette arrangement, whereby a seal is made between the tip and the cell providing isolation of an area of ion channels during the recording of cell depolarisation. Isolation of the currents of single ion channels is possible by careful selection of the cell surface to patch. This method is often used for the evaluation of drugs upon cells in pharmacology tests.

The Whole-cell patch method applies more suction to the cell and ruptures the patched area of the cell. This provides access to the intracellular space while sealing the cell to the pipette, thus preventing contamination from the extracellular space or cellular leakage. Due to the greater surface area of the electrode tip, as compared to the perforating electrode of the original voltage clamp electrodes, a smaller electrode resistance is encountered and thus improved electrical access to the cell. Typically, recording times of no more than 10 minutes are possible using this method as the cell is dialysed by the much greater fluid volume held within the pipette, whereby the intracellular plasma is exchanged with the electrode fluid.

The patch clamp method is often a laborious process and requires great precision in the manipulation and the preparation of the medium for success. The microscope objective must be carefully positioned vertically above the pipette and great care must be taken in the selection of the correctly connected cells of interest when multiple networked cells are considered. It also becomes very difficult to make a large number of parallel cell recordings within a culture using standard equipment, as each patch requires its own micromanipulator.

The manufacture of the pipettes is also often performed by the researcher and requires a great amount of skill to provide an adequate tip diameter and surface.

2.3.1 The Micro-Array Patch Clamp

Micro array patch clamps have evolved with similar ambitions to that of the MEA; the manufacture of a device using reproducible micro-fabrication methods that can multiply the effectiveness of the method over a large number of parallel sites.
This is a particularly new field and work has been published on a number of devices since 1999 that use various micro-fabrication methods to achieve the cell-attached patch method on a microchip [44, 45, 46, 47]. Such devices tend to use a flat substrate, often of the 'glass like' Polydimethylsiloxane (PDMS), with a planar array of pores etched vertically in a horizontally placed membrane that separates the surface from an inner compartment or horizontally into side chambers housing the recording electrode [48], see figure 2.7. The suction to 'trap' a cell is controlled by a fluidic channel connection to the electrode compartment.

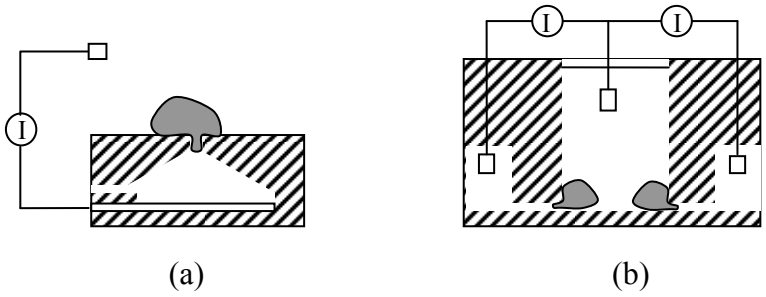

Figure 2.7

Illustrations of two current topologies for on chip patch clamp techniques: (a) shows a typical structure with aperture in horizontally placed membrane and (b) shows the horizontal side chamber methods.

Such devices are promising for loose patch applications, i.e. drug evaluation processes of cellular response but are not as precise as the micropipette method as they do not provide a high enough seal resistance for single channel measurements; the cellular sealing resistance has only been measured at values up to 200 MΩ [49]. Patched cell

lifetime is equivalent to that of the traditional patch clamp method and is not deemed sufficient for chronic applications.

2.4 Active MEA Technologies

The current renaissance in IC and MEMS technology for biomedical applications often conceals the reality that such devices have been considered and developed, albeit intermittently, for over 30 years. The concept of integrating amplification and other signal conditioning circuitry as part of the electrode fabrication followed on quite quickly from the original electrode array attempts in the early 70's. In 1970 Wise et al. published work on one of the first Integrated Circuit extracellular electrode arrays [50]. In 1975, the group demonstrated a photo engraved device with an integrated pair of JFET transistors in the input circuitry to reduce electrode input impedance [51]. The device was connected to an external amplification stage but demonstrated the beginning of the active element integration for a so called *active* Micro Electrode Array (*a*-MEA).

The term Active Microelectrode Array was coined in 1981, in a paper presented by Jobling et al. [52] describing an array of nine active electrodes complete with a supporting array of monolithic buffers and amplifiers and off chip multiplexing circuitry; this device being one of the first truly 'active' demonstrations of the current mould.

Subsequently, a device was published in 1985 leading on from the work of Wise et al. a decade earlier. In this paper Wise and Najafi [54] described work on a 4 electrode array (3 active electrodes) that included on chip 40 dB amplification and signal path multiplexing. The presented design was twofold; a novel microfabricated intrafascicular electrode wire bonded to a surface mounted custom integrated circuit to raise the amplitude of the measured neural signals to a stable level before wiring out to external amplifiers and monitoring equipment. The device also included a rudimentary high pass filtering circuit, using the intrinsic capacitance of the electrode combined with a reverse biased diode to overcome the electrode half cell potential. The active components dissipated 5mW during operation.

An improved Najafi and Wise array was again presented a year later as a 10 active electrode array [54], fabricated in 6 μm NMOS technology, with a 1.3 mm² active silicon area shown diagrammatically with the device of Jobling in figure 2.8

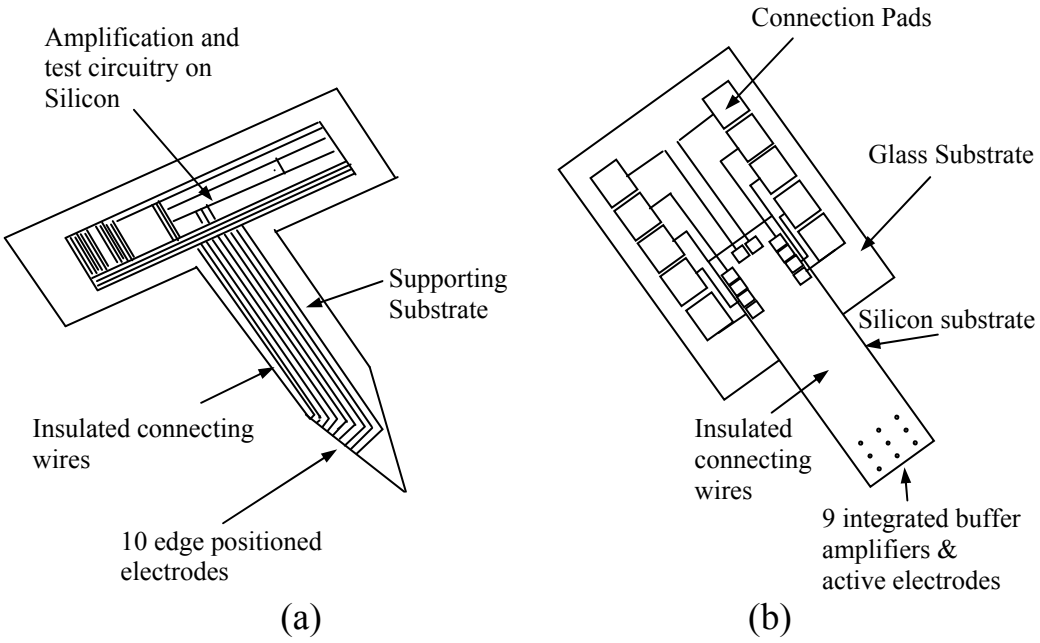

Figure 2.8

Illustrations of the early active MEA Architectures offered by (a) Wise and Najafi and (b) Jobling et al.

In 1987 Steyaert, Sansen and Zhongyuan [55] presented an implantable instrumentation amplifier with low power (150 μA / channel) and low noise design (13 μV rms) that could provide a controllable gain factor between 14 dB – 40 dB programmable by software. The device did not exhibit integrated electrodes but is included here as many of the design principles became important for future devices, particularly concerning the power consumption per channel and the input noise floor; considerations that may have not been optimised, intentionally or not, in the proving of the benefits of an active monolithic electrode array.

The 1990's saw the development of Fromherz's earlier theories regarding transistor-neuron junctions [56] for functionality being tested on silicon. Fromherz, whose original interests lay with optical signal extraction methods, made the conceptual link between the voltage gated properties of neurons and silicon gate transistors. Rather

than using processed silicon devices to detect the voltage dependent changes of the dye, he envisioned a method whereby very high definition imaging of cell depolarisation could be achieved using micro-scale transistor arrays and be used for functional devices. This topic is expanded upon in section 2.4.1.

The Wise array at Michigan was further developed into the early 90's as a much more complex 32 element array [57] with minimised device I/O architecture, built in self test (BIST), higher gain and lower input noise (15 μV rms) and lower power dissipation per channel (1.5 mW / 32 channels). At this point Najafi, a collaborator with Wise at Michigan began looking at 'sieve' electrodes and utilizing monolithic amplification and processing in connection with such arrays. In 1998 the group published the development of a wirelessly connected neural recording system using a sieve electrode configuration [58]. The device featured 32 recording channels actively processed and transmitted by a 24 mm² integrated circuit, consuming 90 mW of power.

Towards the end of the 1990's slightly more interest began gathering in this niche area of CMOS-neurophysiology. Pancrazio et al. in 1998 [59] produced a device capable of stimulation coupled with the recording methodology of previous devices using industry standard thin film technology. The monolithic device consisted of 32 platinized 14 μm diameter electrodes with 16 instrumentation amplifiers, band pass filtering (0.7 Hz – 50 kHz) and on board logic to independently set the electrodes to either stimulate or record. Connectivity to monitoring equipment was provided by ribbon cable to an external 16 bit analogue to digital converter. The device demonstrated the principle but suffered a somewhat non ideal level of noise from signal crosstalk and relatively high power consumption (105 mW).

The Wise et al. array concurrently developed a stimulatory functionality at this time; their latest offering consisting of a four probe, 64 active electrode array.

The next decade marked a sudden increase in the development of aMEA and pseudo aMEA devices, with many more groups worldwide publishing work in this field. With the benefits of complete integrated systems now being fully appreciated, combined with the sophisticated VLSI micro-fabrication technologies available for prototypical

research, many more traditional electrophysiological and analogue design research groups began to focus on the development of the new bio-electronic frontier.

Krause et al. published work in 2000 in collaboration with Offenhausser [60] of Fromherz's group at the Max Plank institute, consisting of an Extended Gate Electrode (EGE) solution to extracellular potential recording. The device used the JFET input isolation method as used by Wise et al. 25 years earlier. Krause's design used commercial JFET devices connected directly to the 64 element electrode array structure, thus providing the so called 'extended gate', from which the source-drain voltage modulation was amplified by additional stages.

Schwartz et al. of the Fraunhofer institute, Germany published work in the late 90's and early 00's regarding a retinal implant system [61] using CMOS imagers and flexible microelectrode stimulation circuitry to demonstrate a method for visual prosthesis. The concept device offered a 400 x 300 pixel photodiode array fabricated in 1 μm CMOS technology wirelessly connected to a 16 element implantable array to stimulate the root ganglia.

Grumet, Wyatt and Rizzo [62] (MIT) published similar work in 2000 from a series of investigative studies into the feasibility of retinal stimulation. Using a custom fabricated array of 10 μm platinum black coated disc electrodes on a glass substrate connected to external amplification and stimulation devices the group demonstrated the recording of spontaneous and light evoked electrical neural responses and the versatility of such a device for retinal experimentation.

An interest in retinal implant systems was also being developed by Litke et al., at CERN at about this time, as a spin off from their work on microelectrode arrays for particle detection experiments. Litke had originally proposed the 'Retinal Readout System' in a 1991 paper [63], an investigation into what signals the retina sent to the brain using microelectrodes at the ganglia before the optic nerve. A status report on the project was published in 1998 [64] however serious active methods weren't developed until the 00's where PCB type systems with dedicated ASICs were implemented for in vitro study in collaboration with Debrowski at the University of Krackow, Poland, or with Mathieson and Cunningham at Glasgow, England which

consisted of an array of 512 electrodes connected to a custom ASIC amplifier array [66], [67], [68].

Obeid et al. presented two 16 channel ‘neurochips’ in 2003 for in vitro study [68]. The chips were fabricated in 0.8 μm and 0.5 μm technologies, used on board amplifiers, multiplexing circuitry and filter circuits that utilized large off chip capacitors due the prohibitively large capacitance values required in the design. A minimum noise level of 4.4 μV rms was achieved in the 0.5 μm device, which consumed 0.95 mW per channel for a gain of 53.4 dB. This device was one of the many neural specific signal conditioning ASIC designs that would begin to emerge at this time. Dabrowski [69, 70] and Harrison [71] published work in the following years for devices solely intended for use with microelectrode arrays and electrogenic cell cultures or dissections. The design criteria was heavily weighted on passband filter design, low power consumption, low input signal noise and high circuit matching between channels. The use of subthreshold or diode connected transistors to compensate for the high resistance values (MΩ - GΩ) needed in the high pass filter circuitry also appeared in both of these 2003 / 2004 publications and again in Mohseni and Najafi [72] and Heer et al. [73]. Subthreshold MOS resistors were deemed more flexible because of their variability by voltage control, although they increase complexity due to the need for accurate bias control.

The Wise-Najafi group had developed their neural measurement ASIC devices through the 90’s and early 00’s to a high level of sophistication, including multiplexing, analogue to digital conversion, wireless telemetry and stimulation [74, 75] all of the ASICs produced remained separate from the electrodes for versatility in different microelectrode structures such as sieve and intrafascicular electrodes.

An impressive 2003 effort by Eversmann et al, [76] also discussed in section 2.4.1 included 16384 capacitive transistor buffers (128 x 128) with 128 column readout amplifiers using a row switching technique to access each neural recording ‘pixel’. The device concept was similar to that of Jobling in ’81, with a more sophisticated detection and amplification system local to the electrodes. The device used on board 8:1 multiplexing scheme (3 bit) to reduce the off chip analogue signal channels to a PCB buffer scheme and PC card for digitization and analysis.

The Heer et al. papers presented work in 2004 - 2006 [77] of an active array with the amplification circuitry in close proximity to the working electrodes. This work marked a major collaboration between scientific disciplines, including a Physicist (the main author), several Physical Chemists, an Analogue Design Engineer, and a Biochemical Engineer. The monolithic circuit used traditional CMOS circuit architectures that with the 0.6 μm were now compact enough to integrate on the same substrate as the electrodes. The device demonstrated a lowinput referred noise level (<10 μV rms), and was packaged with a thick passivation layer suitable for biological environments and 16 40 μm x 40 μm electrodes on the chip surface with 250 μm minimum pitch. Each electrode was capable of recording or stimulating and the device included filtering and multiplexing circuitry, and both Analogue to Digital and Digital to Analogue circuitry for digitising the recorded signals and generating the stimulatory waveforms respectively. Interfacing hardware was also included on chip to control the device and handle I/O between the device and off-chip computer hardware. Functionality of the IC was demonstrated using embryonic chicken cardiomyocytes. The project was developed almost concurrently with the work developed for this thesis [78], with publications showing similar thinking towards overall system methodology; the integration of amplifier and electrode directly on a single chip, which may imply a new trend in array design methodology for improved signal quality and density through integration.

Recent to the submission of this thesis, the Litke-Dabrowski, Harrison and Heer devices were republished with revisions and refinements. The Litke group are currently working with a 512 electrode device for retinal implants, Harrison is working with Richard Normann of the 'Utah Array' fame with 100 channel recording systems from his 100 element spike array and Heer has published successful results for a 128 element active MEA system [79]. In addition, a number of commercial 'spin-off' companies have developed from such research groups as that of Wyatt and Rizzo at MIT, Humayun at the Intraocular Research Group at Southern California, Chow at Illinois and that of the German research partnerships, forming the companies BRIP (Boston Retinal Implant Project), Second Sight, Optobionics and Retina Implant GmbH respectively - specialising in the development of retinal prosthetics.

2.4.1 Neuron-Transistor Array

The transistor array methods discussed briefly in the previous chapter were conceptualised by a German Group at the University of Ulm headed by Peter Fromherz (’85 - ‘94) and further developed by Fromherz at the Max-Planck Institute for Biophysical Chemistry in Gottingen (’94 -). Fromherz began promoting his neuron-silicon interface theories in 1985 with the concept of the neuron-to-silicon and silicon-to-neuron synapse; whereby a neuron is grown directly on top of a p- or n-doped silicon surface and transient electrical responses are translated between the two. Fromherz believed that the influx of ionic current across the silicon-neuron ‘synaptic cleft’ (see figure 2.9) as the cell depolarised could modulate the depletion region of the doped semiconductor (formed by its interface with the electrolyte) via capacitive coupling. It was also argued that the neuron could be stimulated by a current across the semiconductor flowing along the cleft.

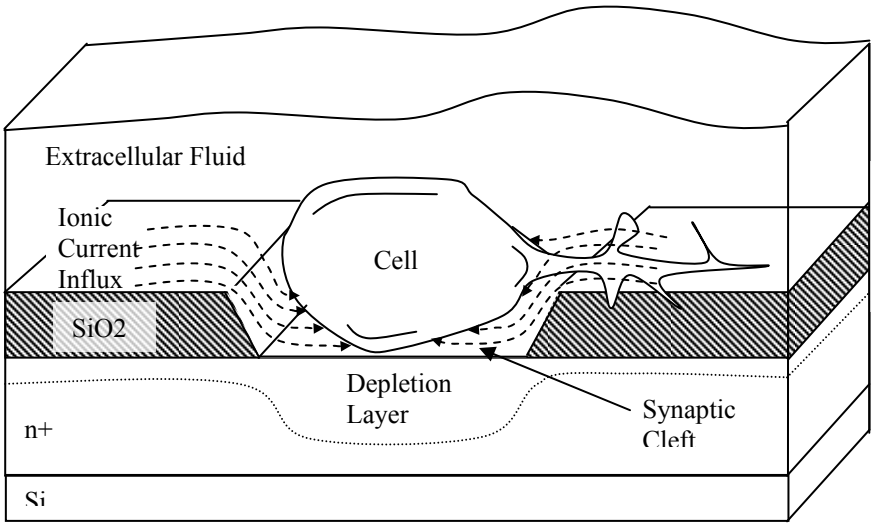

Figure 2.9

Fromherz’ neuron-silicon junction, adapted from [79].

In the first generation implementation of this concept, Leech neurons were placed upon a 4 x 4 array of thin oxide FET transistors and a neuron was stimulated using the patch clamp technique [80]. The FETs were fabricated devoid of the Aluminium gate metal of the standard MOSFET process, using instead a 1 μm oxide layer to provide capacitive coupling between the silicon gate and the extracellular surface of the neuron.

As predicted, potential changes in the local extracellular fluid, caused by ionic current flux through the neuron's cell wall modulated the transistors Drain-to Source current by providing a transient gate voltage. An equivalent circuit was developed to describe the resistive-capacitive response of the system at the neuron-FET junction. Fromherz described the system as a 'Neuron Transistor' due to 'efficient coupling' between the neuron and device between 0.1 Hz to 1000 Hz.

The Fromherz method can be shown to be very similar to the Jobling et al. device discussed in section 2.4 in that a biased input transistor is used directly beneath the cell to record the extracellular response, however Fromherz' omission of the metal top gate layer can be argued to provide a more direct coupling mechanism between cell and the successive amplification circuitry, reducing half cell potential offsets and other effects.

Between 1995 and 2001 a series of papers were released regarding individual aspects of the techniques, interface characterisation, the use of adhesion coatings and neurons from differing species aimed at refining the process of demonstrating neuron-silicon coupling.

The Fromherz device was further developed to incorporate a large p-doped silicon/SiO2 'stimulation spot' that allowed cell stimulation to be achieved on chip without using the invasive patch method [81]. In a further paper [82] Jenkner, Müller and Fromherz reported a two way interface between the chip and cultured neurons. A chip-neuron-neuron and neuron-neuron-chip communication network was demonstrated but reproducibility and long term operation was seen to be very dependent upon where the cultured neurons decided to bond to the chip, neuron migration and the strength of 'neuroelectronic' coupling.

The control of cell bonding and growth was tackled in later work using the 'picket fence' technique whereby microfabricated polymide structures were etched on chip to trap the somata of L.Stagnalis (pond snails) neurons [83] with much success. Work was also undertaken involving the use of coating materials for cell adhesion and substrate shaping profiles to proliferate the cellular contact and control the direction of growth.

In 2003 the Max-Planck group published work on a 128 x 128 device array with Thewes et al. using the electrolyte-oxide-metal-oxide-semiconductor (EOMOS) transistors in contact with the neurons [76]. The sensor transistors provided high density imaging of the cultures examined, using a 4.5 μm diameter recording area and 7.8μm pitch between active recording sites. The device exhibited relatively high power consumption (656 mW at 5 V), problematic kT/C noise at the EOMOS gates reducing recording resolution and required a periodic calibration of each sensing pixel each 200 read cycles during 2 kHz sampling. However, at 128 x 128 pixels it is far ahead of the competition in terms of channel density.

2.5 Optical Recording Methods

The discovery of several dyes in the early 1970's brought forward the possibility of optical detection of Action Potentials. These dyes showed an increased absorption of applied light during cell depolarisation and were used in conjunction with photo detector arrays to image the spatial spread of action potentials through neurological samples.

Grivald, Salzberg and Cohen developed this method in the following years using merocyanine dyes. They demonstrated the possibility of recording the activity of several neurons simultaneously using 14 carefully placed photodiodes coupled to an image enlarged by a microscope objective through fibre-optic light guides [84].
This work showed that a high signal to noise ratio could be achieved using this method and membrane potential changes as small as 1 mV could be distinguished with modest averaging techniques.
Many application specific voltage sensitive dyes have been developed over the years, along with ion specific dyes that fluoresce on contact with a specific species such as Calcium (chlortetracycline). Modern devices use high density charged coupled devices (CCD) similar to that of a digital camera and thus do not require fibre-optic guides. Commercial products are available with spatial resolutions up to 1024 x 1024 pixels.

Optical recording methods are particularly good for showing transients deep within tissue but many of the dyes are toxic and may damage the cells under analysis over time. The method is also inappropriate for in vivo study due to toxicity, dispersal of the dye over time and the difficulty of illuminating (and possibly magnifying) the viewed area for the CCD to image.

2.6 Remarks

In this chapter, the key methods employed for electrophysiological research have been reviewed. These methods have been appraised for their general strengths and weaknesses within this field, with the Active MEA method being selected as the only suitable method in terms of chronic observation and high spatiotemporal cell observation.

The potential strength of the Active MEA, including the Fromherz method, can immediately be seen from a generic system point of view. Micro (or even sub-micro) MEA's can be produced with standard CMOS fabrication technologies that can be combined on chip with channel routing, signal conditioning circuitry and output multiplexing. A few contemporary publications have demonstrated these strengths with designs that use standard analogue design to measure, condition and digitise neural signals on a single chip. These designs have also demonstrated very dense arrays of active electrodes that are sized and spaced at a sub cellular level. Some have included controlled methods of stimulation and rudimentary wireless telemetry.
A second area of merit is the versatility of the Active MEA. A carefully designed Active MEA could additionally be used as a generic substrate for other measurement methods, bringing enhanced functionality to a piggy-backed passive 'Utah Array' or prefabricated Micro-Patch, while still functioning as a stand alone device before and possibly after, such a connection. Such a device could also act as a localised high precision routing point for hard wired off chip 'sieve' electrodes, cuff electrodes, flexible electrode arrays and low density intra-fascicular electrodes.

In addition, CMOS technology has been around for over thirty years and there are many sophisticated circuits that have been developed to provide powerful

functionality for analogue and digital applications while maintaining low power, low noise and high speed. Circuits, which were originally motivated by and designed for the development of popular, more research intensive projects, such as low noise particle detection, sound or image capture and processing, or high speed analogue to digital conversion, may be directly relevant to the needs of an Active MEA data acquisition and transmission system.

There appears to be much room for improvement in this field, especially in the understanding of the signals measured, namely the electrogenic mechanism of neurons, the non linear behaviour of transducer electrodes and the front end circuitry of the device; an area few designers have developed in much detail, save as to regard as a problematic source of offset and noise. As this interface is the key element in neural signal transduction the understanding of its properties and methods of charge transfer between the liquid to solid phase should be an essential motivation to match the sensing equipment to the transducer for optimal design.

Additionally, many of the devices are arranged in a two part connection scheme, whereby the MEA substrate is connected to an external amplification chip by PCB or chip stacking methods. Such devices may be greatly improved by the integration of the amplification circuitry directly beneath the MEA substrate, as demonstrated by Fromherz and Heer. However, the difficulty in packaging such dedicated amplification circuitry directly beneath the electrode has typically led to large inter-electrode spacing and complex transistor readout schemes.

It is proposed that a bottom up approach, developing a firm understanding of the interface between biological and electronic devices, may display a focussed path towards design optimisation, whereby a dedicated front end amplification circuit may be integrated more compactly beneath the electrode with inter-electrode spacing approaching that of the cells that are studied. By understanding the interface, the mechanism of its signal transduction and its fundamental noise floor an application specific design may be developed that can provide optimal amplifier and conditioning characteristics at a lower area overhead, thus optimising the active front end sensors for high spatial density and signal preservation.

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Chapter 3

Analysis of Passive and Active Micro Electrode Array Systems

For the chronic observation and analysis of multiple cell networks, reproducing the traditional methods of the single cell voltage clamp and patch clamp on a cell to cell basis is impossible. Microfabricated microelectrode arrays (MEA) can provide long term multipoint study of many neurons with less operator skill and higher flexibility than previous methods. Much study has been conducted regarding the processing circuits of small cultured neural networks using this method. However, in depth neural network observation and analysis of cultures, brains slices or otherwise demand higher density recording electrode arrays than are possible with current passive MEAs. This is due to interconnection issues at the MEA itself and to off-board conditioning and analysis circuitry. Integration of the off-board circuitry within the MEA substrate is a possible solution to this limitation.

This chapter characterises the MEA and considers the extent of these limitations and how they may be reduced by integration. Electrical issues of the microfabricated MEA layout and interconnection are explored as the device is pushed to a higher level of individually accessible recording sites and possible integrated solutions discussed.

3.1 Analysis of the MEA System

Passive MEAs allow the user to electrically monitor the excitation of multiple neurons as they communicate within a spatiotemporal environment. The diameter of the microelectrodes is typically close to that of the studied cells and allows spatial selectivity and isolation of measured signals. Microelectrodes provide sufficient electrical coupling to the conductive extracellular fluid surrounding the cell that the ionic charge flux that occurs during an Action Potential can be measured electrically as electrochemical perturbations at the electrode interface. By this method cellular communication and behaviour can be monitored by measuring the low level emf generated within the conductive electrode circuit.

3.1.1 The MEA Measurement Circuit

The microelectrode to neuron coupling is often modelled as a simple electrical circuit similar to that given in figure 3.1.

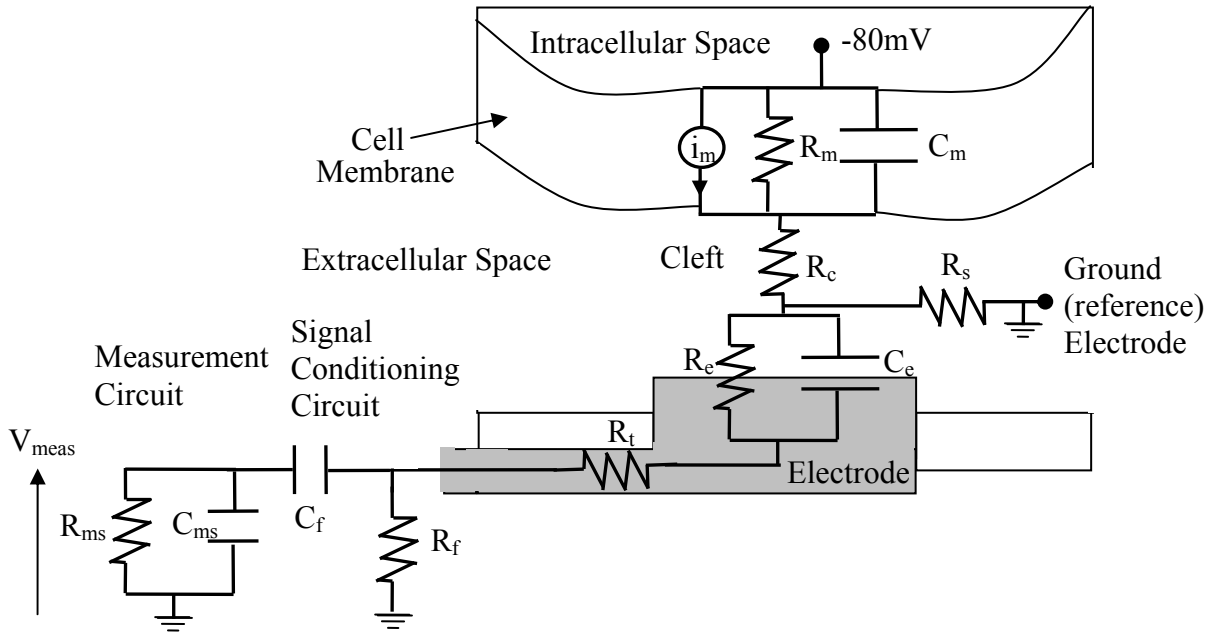

Figure 3.1

Circuit diagram for the extracellular recording of neural signals.

In such a circuit the electrical path between the neuron and electrode are described in terms of a simple RC network. The electrode interface is described by resistance R_e and capacitance C_e, the properties of cell membrane are described similarly with R_m and C_m and the ionic flux is described by a transient current of nanoamps in magnitude. There will also be offsets and drift occurring at the liquid to metal interface. The extracellular space between the excited neuron and the electrode is characterised by an attenuating potential divider between a small cleft resistance R_c and the seal resistance of cell adhesion R_s. The resistance of the interconnecting track between the electrode and the front end of the amplification and conditioning circuitry is represented by R_t, the front end filter by R_f and C_f and the measurement circuit input by R_{ms} and C_{ms}. V_{meas} represent the final signal measured by the measurement circuit.

When the electrical properties of the neuron and electrode interface are quantified it can be shown that the resistive and capacitive properties of the MEA, as well as other parasitic parameters that will be covered later, must be carefully developed to ensure that V_{meas} is a maximised and undistorted translation of the generated biological signal. Some distortion is unavoidable as will be shown in chapter 5

The above statement can be best appreciated by developing the circuit between the cell membrane and the electrode bulk into a Thevenin equivalent source. This is shown later in section 3.2. At this point in the thesis it is sufficient to assume that the signal sensed by the measurement circuit is somewhat degraded in its path between the wet and dry phases of the interface. For this reason the signal measured at the electrode requires much more amplification and conditioning than it would from intracellular measurement before it can be analysed by the user. The low magnitude extracellular signals are also dangerously close to that of typical electromagnetic and intrinsic noise levels that conductive tracks and cables are unfortunately prone to, causing some signals to be totally lost even in well designed systems.

Figure 3.2 shows a photograph of a typical commercial MEA and an analysis system showing the typical MEA surface interconnection and the large off-board cabling

arrangement. Such devices are unsuitable for *in vivo* applications simply because of the size and wiring complications.

a.) b.)

Figure 3.2

a.) A commercial passive MEA with 60 Gold electrodes wired to bond pads outside of the extracellular chamber. b.) photograph of a commercial MEA system

In the past, neuroscientists have used electronic amplifier circuits to raise the peak to peak voltage of the measured signal to drive the deflecting magnets of a polygraph machine, modulate the magnetic head of a tape recorder, or drive a speaker coil, each requiring several volts. It is still common practice within current biological research to 'listen' to the chatter of neurons to confirm the suitability of an electrode connection, especially in the analysis of multiple fibres within nerve trunks; a practice made possible by the fact that the frequencies of neural signals fall into the frequency range of human hearing.

More recently, the analysis of neurons has reached the personal computer, digital signal processing and analysis tools provide the researcher with unparalleled processing power, both real time and post recording, that allow concurrent multi neuron analysis to further the understanding of the larger neural system. Such modern systems still require much amplification and conditioning of the low level neural signals before they can be digitised and processed in hardware.

3.1.2 Front End Signal Conditioning

The signal measured by the MEA is very weak; the voltage may be microvolts to millivolts and the current in the order of nanoamps. Before the signal can be observed or analysed by the neuroscientist it must be conditioned to comply with the monitoring equipment or personal computer used. A typical conditioning system that may be used to reduce the artefacts discussed in the previous section is presented in Figure 3.3. The system consists of a filter and preamplifier at the front end, in direct electrical connection to the MEA channel. The front end filter is required to remove the electrochemical half cell potential and low frequency thermodynamic noise of the electrode surface that are typically many orders of magnitude greater than the signal. This is usually performed by a capacitively coupled high pass filter. Once the signal has been filtered in this way it can be amplified by the preamplifier to the desired voltage and driving current level without causing saturation. The main task of the front end amplifier is to preserve the signal by raising its level above that of intrinsic device and circuit noise, thus preventing any further loss or contamination.

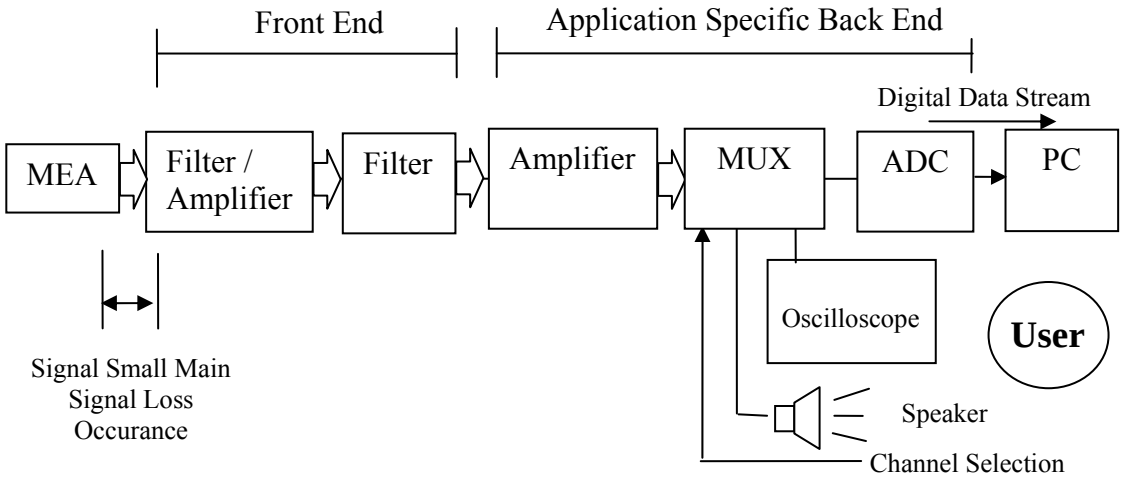

Figure 3.3

Overall MEA recording system from the microelectrode to the end user, showing the classification of front end and back end.

The second stage filter is typically used to reduce the noise of the system by removing the high frequency contributions of the Johnson thermal noise and other high frequency sources, thus reducing their additive contamination of the signal of interest.

An additional amplification stage may follow the front end. If present, this second stage amplification block is used to boost the conditioned signal to a level that can be usefully registered by a viewing or recording device. This value is typically in the region of volts, requiring a total overall amplification of some 100 – 100,000 times (60 - 100 dB) between the electrode and the device, for signals from 10 μV to 10 mV.

3.1.3 Further Conditioning: The Back End

If the signal is to be analysed by a personal computer or specialised digital hardware that is essential for a large scale neural network analysis, further processing is required in the form of analogue to digital conversion (ADC). This may be performed by the device itself or by ancillary hardware. Whichever is the case, the amplified signal must be within the conversion range of the ADC. ADCs operate by converting analogue voltage levels into digital binary representations by comparison to an internal reference that is typically equivalent to its supply voltage. For example, an 8bit ADC operating at 5 volts will compare an incoming signal to 256 equally spaced reference voltages between 0 Volts and 5 Volts, in increments of 19.5 mV. The binary output word will correspond to the multiples of this value taken from an internal reference table, with 0-19.5 mV being 00000000, 19.5-39 mV being 00000001, 39-58.5 mV being 00000010 and so on. In order to capitalise from the functionality of the device, the gain of the system must be geared to amplify the largest neural signal voltages to a value close to the ADCs maximum without exceeding that value. This is termed maintaining the headroom. Signals that fall out of bounds of this headroom will ‘saturate’ in a similar way to an amplifier; the binary output word will hang at the binary value of the maxima or minima that has been exceeded. If the signal converted falls within this range but is too small, the specified accuracy of the ADC, in this case 8bit, will be unexploited and the level of accuracy reduced. The bit rate

of the converter must be chosen carefully to ensure that the smaller recorded signals of interest are not lost between the digitisation levels.

The ADC will discretize the time base as well as the magnitude of the signal. Care must be taken to specify the correct sampling frequency for later reconstruction and analysis of the signal. As a rule of thumb, the Nyquist Sampling theorem is often quoted, whereby a sinusoidal signal must be sampled at twice its frequency of oscillation for accurate reproduction in the digital domain. A signal composed of many composite sinusoids, such as that found in neural signals must be sampled at twice highest frequency of these composites to have its temporal shape reproduced faithfully. Typically, such signals are purposely under-sampled by neuroscientists studying neural networks and multi-fibre nerve trunks, as they are more interested in the spatiotemporal recording of the event rather than its form. The bandwidth of neural signals is often quoted in the literature as spanning from 300 Hz to 10 kHz, yet many neuroscientists prefer a sampling rate in the low 100 Hz's. It must be noted that such low sampling rates will inherently give erroneous signal magnitudes and events may be lost between samples, as the peak of the extracellular signal waveform may fall outside of the discrete sampling points. For single source, multiple signal analysis, such as may be necessary in a spatially under sampled array, high temporal sampling is a must if knowledge about the composite signals are to be extracted.

3.2 The MEA Interconnection Problem.

As discussed in the previous chapter, the main challenge of the passive MEA is the isolated interconnection between each electrode and the conditioning circuitry. When the system is pushed towards large arrays with closely spaced electrodes the functionality of the system is challenged by increasing interface impedance and interconnection track resistance that raise the performance required from the substrate, insulating materials and front end circuitry. This goes hand in hand with the topological constraints of electrode and track routing; each electrode requires a separate transmission line to the amplification

and signal conditioning circuitry and again to the monitoring device. This leads to a large number of conductive tracks being present on the fabricated planar MEA surface that limit the area available for recording electrodes and introduce relatively large capacitive and resistive parasitics between the electrodes and the recording device. An additional constraint may also lie with the available fabrication process. This could also limit the tolerances of width and spacing. For these reasons, current, commercial state of the art MEAs rarely exceed 60-100 recording electrodes.

3.2.1 Electrical Limitations of the MEA

Figure 3.4 summarises the parasitic conduction paths that are typical to an MEA. The inter-track resistance R_i and capacitance C_i occurs across the insulation between tracks.. Substrate to track resistance and capacitance (R_{st} and C_{st}) may be present with some materials and a certain shunt impedance (R_{sh} and C_{sh}) will exist between the track insulation and the electrolyte. If these parasitics are considered in conjunction with those described in figure 3.1 the electrical limitations of the MEA may be mathematically analysed in terms of source impedance through to that of the input of the measurement device.

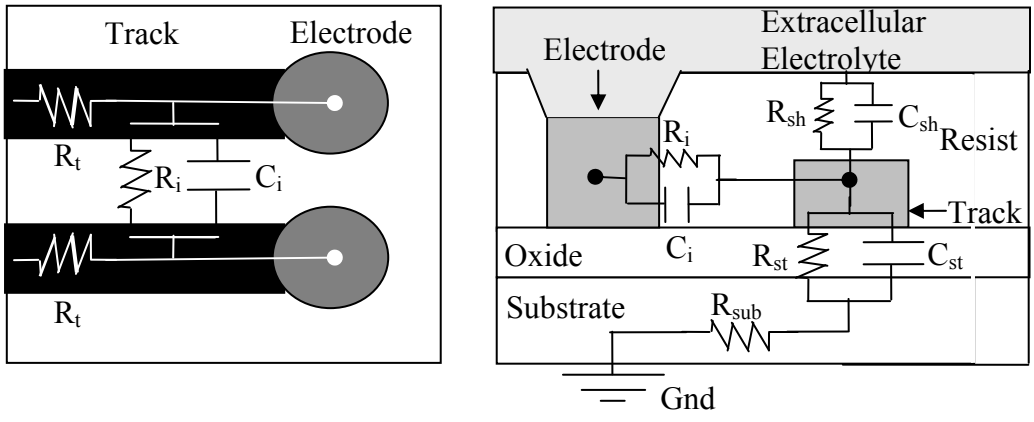

Figure 3.4

Track parasitics of the MEA

3.2.1.1 The Source Impedance

The impedance of the signal source is the most important part to consider when designing any low level measurement system. Generally in electronic systems the engineer is faced with components that interface with electrical magnitudes of volts and milliamps which are easily accommodated in the solid state by basic cabling and transistor technology. When interfacing neurons we are presented with liquid to solid state transduction of ionic source signals with incompatible charge carriers that are many orders of magnitude smaller than volts or milliamps making careful selection of materials and devices an unavoidable necessity.

Beginning with the neuron, the signal we wish to measure is created by a transient ionic influx of Na^+ into the neuron, followed by a slower equalising efflux of K^+. This may be defined as a signal source with impedance relative to the electrical resistance of the cells membrane during the open state of the voltage gated channels and the capacitance of the membrane surface. We must then define what charge movement the electrode 'sees' during this open state. To simplify matters it is useful to freeze time and consider the membrane impedance at its fully open and fully closed states. Figure 3.5 shows a generic non-ion-specific plot of the membrane resistance during an Action Potential. The plot was generated using the simulation program that is discussed in detail in chapter 4 and describes the electrical behaviour of the membrane of a Giant Squid axon. The figure illustrates that the resistance of the membrane reduces by almost 3 orders of magnitude during an Action Potential event. The important values to be taken from this simulated data for now are that the source surface impedance varies between 200 Ωcm^2 at the open state and 200 $k\Omega cm^2$ at the closed state. The heightened resistance of 6 $M\Omega cm^2$ is neglected as this occurs during the refractory period when we do not expect a signal to occur.

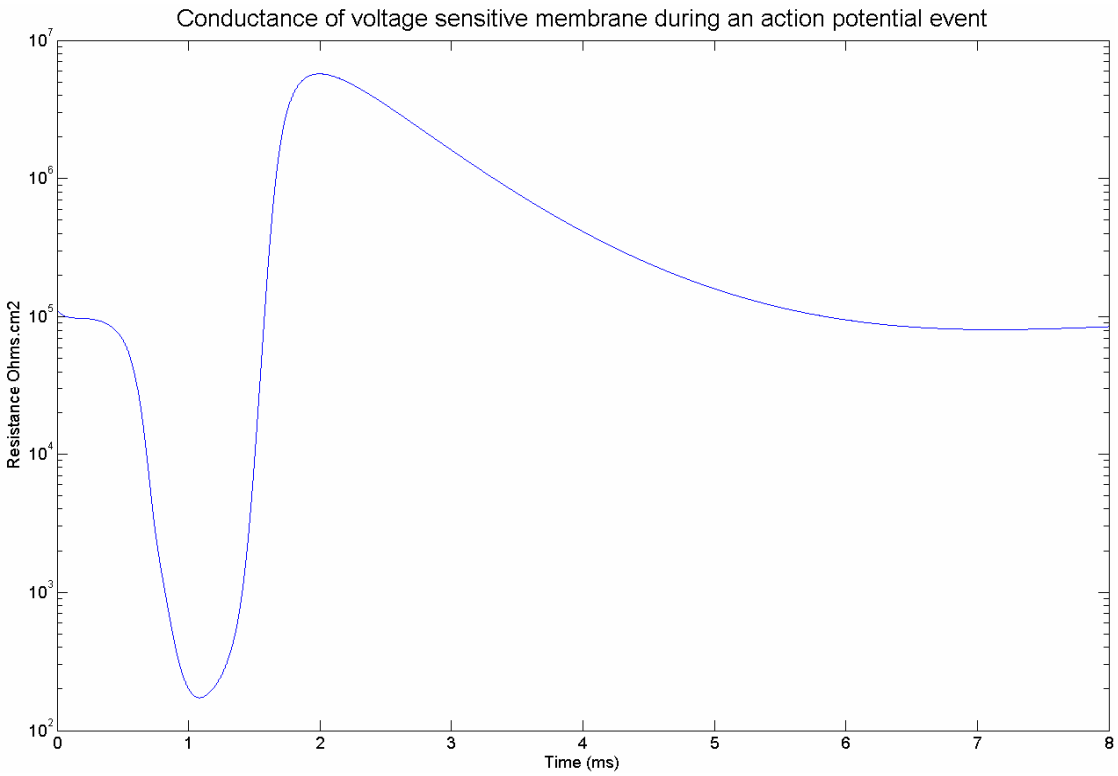

Figure 3.5

Membrane resistance during an action potential calculated using computer simulation of Hodgkin and Huxley model [1]

The second property for consideration is the physical interaction between the neuron and the substrate including the electrodes. It is typically observed that a cultured cell will attempt to anchor itself to the boundaries of an artificial environment as it would within its host organism. The adhesion molecules present within (or that are transported to) the plasma membrane will form adhesion points or plaques with the substrate to anchor the cell down and facilitate its controlled migration through the culture environment (this is discussed briefly in the introduction). As gravity pulls the suspension of cells down to the substrate the neurons will bond with the surface and more importantly over the electrode surface. The adhesion process will form a finite extracellular reservoir between the Soma and the substrate surface that facilitates the extracellular measurement process. This reservoir is often physically and electrically restricted from the outer bulk electrolyte of the culture and is commonly termed a ‘cleft’. Similar adhesion processes occur at the

boundary between dissected slices of neural matter and accommodating substrates *in vitro*. This creates the so called seal resistance (R_s) shown in figure 3.1.

The source signal may now be described as it is presented to the electrode surface as a Thevenin source:

$$V_{TH} = \frac{V_{mem} \cdot R_s}{R_s + \left(C_m j\omega + \frac{1}{R_m} \right)^{-1}} \tag{3.1}$$

With source impedance:

$$Z_{TH} = \frac{R_s}{R_s \left(C_m j\omega + \frac{1}{R_m} \right) + 1} \tag{3.2}$$

This is only sufficient however to describe the signal magnitude within the cleft. Before the signal may be measured electrically it must be transduced from the ionic form to electronic potential and current. This occurs in a somewhat complex manner at the electrode interface by electrochemical reaction and capacitive charge 'mirroring'. The ratio of these charge transfer mechanisms differ greatly for different materials. This topic is covered later in great detail in chapters 6 and 7 but for the current exercise it is sufficient to generalise this interface as the parallel, linear resistor and capacitor pair (R_e and C_e) shown in figure 3.1.

The effect of the interface on the source magnitude ineffectual, however the source impedance is raised to the sum of Z_{th} and the impedance of the interface:

$$Z_{Source} = \frac{R_s}{R_s \left(C_m j\omega + \frac{1}{R_m} \right) + 1} + \frac{R_e}{R_e C_e j\omega + 1} \tag{3.3}$$

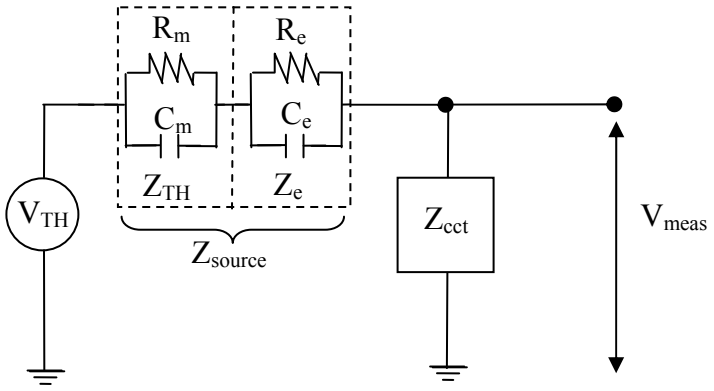

Figure 3.6

Reduced component equivalent circuit of the neuron-measurement circuit interface

The source impedance Z_{source} dictates a level of minimum impedance that the rest of the passive circuit must exhibit. Ideally all the ground connected circuit components following the interface shown in figure 3.1, including the parasitic resistances and capacitances given in figure 3.4 should be many times larger than Z_{source} to prevent V_{TH} from being attenuated in the resulting potential divider circuit illustrated in figure 3.6.

Using typical values for the membrane surface capacitance C_m = 1 μF/cm² [1], electrode interface surface capacitance c_e =10 μF/cm² [2], electrode interface dc surface resistivity r_e = 5 MΩcm² [3] and taking a minimum membrane surface resistivity r_e of 200 Ωcm² from figure 3.5, the impedance may be approximated. Figure 3.7 shows an impedance plot for a hypothetical 50 μm diameter soma attached to a 50 μm electrode from 1 Hz to 100 kHz. In the plot the seal resistance is assumed infinite.

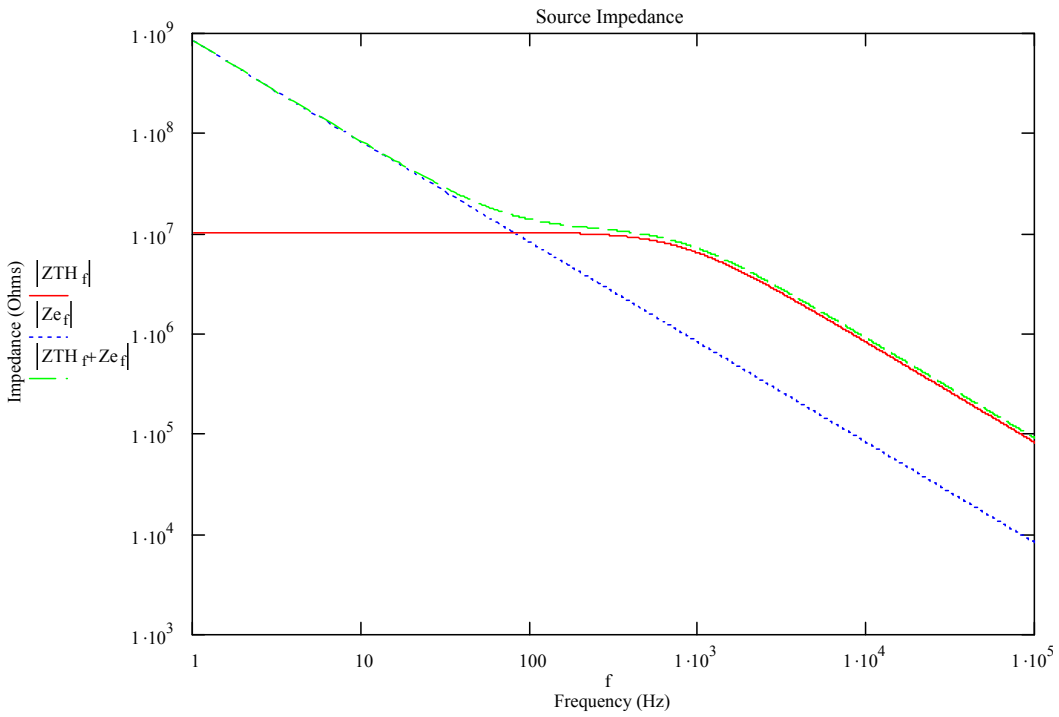

Figure 3.7

Component parts of frequency dependent source impedance Z_{TH} (red) and ZE (blue) and their combined value (green) for a 50µm diameter cell-electrode interface

For this particular system care must be taken within the design to maintain the minimum impedance dictated by the source within the frequencies of interest to insure that unwanted attenuation does not occur (of course some attenuation may be required at certain frequencies to remove noise and other unwanted signals). Attenuation is governed by:

$$V_{meas} = \frac{V_{TH} Z_{cct}}{Z_{source} + Z_{cct}} \qquad 3.4$$

To ensure that attenuation is below 1 % Z_{cct} must be at least 100 times greater than Z_{source}.

The lower the frequencies of interest are and the smaller the electrode/cell interface becomes the greater the need for high quality fabrication materials and components. As

measurement circuits with Field Effect Transistor (FET) inputs generally have input impedances greater than $10^{14}\Omega$ it is beneficial to place the FET input as close to the electrode interface as possible.

3.2.1.2 Track Resistance and Parasitic Shunt Impedance

When considering the fabrication techniques of MEAs it becomes clear that the track resistance of these interconnect lines is significant. The example of a typical photolithographic process given in figure 3.4, shows a generously thick metallization layer of roughly 200 nm thickness.

This value will typically never exceed 1 µm. For a relatively wide gold track of 10 µm width the resistance per millimetre length of each track will be:

$$r_{track} = \rho \frac{l}{A} = 23.25 \times 10^{-9} \frac{1 \times 10^{-3}}{1 \times 10^{-5} \cdot 2 \times 10^{-7}} = 11.6 \Omega/mm \qquad (3.5)$$

Causing a 10mm track length to accumulate 116 Ω of resistance.

Although the value may seem trivially small upon first glance, the effect can be damaging to the sub milli-Volt potentials translated from the extracellular potentials by the electrode surface. Passive MEAS will generally require several centimetres of such tracks to connect to bond pads and the local hardware of an Active MEA package may require several millimetres to several centimetres depending upon design. As will be shown in section 3.2.2, the resistance of the track also becomes a source of noise.

Parasitic shunt impedances are problematic. Although they are usually very high in value and unnoticeable in many other circuits, they manifest themselves when the signal source impedance and measurement impedance are high. In situations where track lengths are large this can increase the overall input impedance. The parasitic resistances are inversely cumulative over the track path whereas the track resistance is directly cumulative. In such

situations, the ratio between track resistance and parasitic resistances converge. The resulting potential divider will further reduce the signal available to the front end. For compact MEA designs built upon highly resistant dielectric surfaces such as glass, with thick, high resistance passivation layers such Silicon Nitride (Si_3N_4) this will only become a problem in very extreme cases of track length and width.

Parasitic effects may worsen as process defects such as uneven resist coatings, pin holes and particle contamination effects reduce their impedance value.

Similar effects also occur as a result of the cabling of the signals off the MEA substrate, including cable resistance and inter wire resistance and capacitance, especially as the wires have minimal diameters and are minimally insulated to reduce the overall cable diameter for convenience of use.

More of a problem is the effect of parasitic capacitances between neighbouring tracks (C_i), their dielectric separation from the substrate (C_s) and electrolyte (C_{sh}). The measured signal transients within the tracks during operation will capacitively couple to these conductive device planes. The extent of the coupling is relative to the ease of conductance experienced by the signal through the track and the level of capacitance between the planes for each frequency component. In the case of two capacitively coupled parallel tracks, the signal lost from one will appear as interference on the other and vice versa. The extracellular fluid and substrate, due to their volume relative to the tracks may be assumed as ground.

The inter-track capacitance may be approximated by the solution to Gauss' theorem for two uniform line charges in a dielectric, if the track separation is greater than the track width:

$$C_i = \frac{q}{V} = \frac{\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{s - w/2}{w/2}\right)} \quad \text{F/m} \qquad 3.6$$

Where w is the track width, s is the track to track or track to plane separation and ε_0 and ε_r are the permittivity of free space and the relative permeability of the separating material. For a track routed between two others the value calculated by equation 3.6 must be doubled due to the parallel coupling effect on each side of that track.

The capacitance formed between the substrate and track and the electrolyte and track are much more complicated due to the high resistance of the plate formed by the substrate and the nature of the ionic charge carriers in the electrolyte (both would typically be empirically characterised for a particular device). As a guide we may however just simply assume each form conductive plates that mirror the track, separated by dielectric:

$$C = \varepsilon_0 \varepsilon_r \frac{w \cdot l}{d} \qquad 3.7$$

Where d is the depth of the separating dielectric.

For glass substrates d is large and C is small as the bulk of the material is not sufficiently conductive to form an equivalent mirror plate. For other materials such as SiO_2 grown on silicon, the semiconductor is conductive enough to form a mirrored plate and C will depend upon the depth of the SiO_2 passivation and the effective depth of the equivalent centre of mass of the mirrored charges in the material. In the case of the track coupling to the extracellular fluid, C will be highly dependent upon the relative permittivity and thickness of the top layer passivation. As the capacitances are parallel-connected to the track they will be cumulative with the total capacitance being the sum of the three component capacitances.

As an example of coupling losses from a track, the attenuation may be modelled by a simple RC potential divider forming an effective low pass filter circuit. For the hypothetical track dimensions used in equation 3.5, assuming the device is fabricated on a glass substrate with a 10 μm inter-track spacing and has a 200 nm passivation layer of

Si_2N_3 with $\varepsilon_r \approx 7$, the total capacitance would be $c_T = 3.5$ pF/mm of track length and is dominated by C_{sh}.

Losses may be calculated according to the transfer function:

$$H(f) = \frac{1}{1 + L^2 \cdot c_T \cdot r_{track} \cdot 2\pi f} \qquad 3.8$$

Where L is the length continuation of the track in mm's.

The attenuation is determined by the roll-off point of this filter transfer function that is proportional to L^2. As the track length increases the filter roll-off point lowers and frequencies within the 300 Hz to 5 kHz range are increasingly affected, with the higher frequencies attenuating first. For the given example with L = 1 mm the 3 dB roll-off point is at the GHz level and will cause no more than a 0.0005 % signal loss, or noise input at 5 kHz. As L increases to 10 mm and 100 mm the attenuation level rises to 0.05 % and 5 %. It can also be seen from equations 3.2 to 3.5 that a trade off occurs between capacitive coupling, noise and ultimately routing topology. In most cases, resistive losses, capacitive losses and noise may all be controlled by minimal track lengths, but this may place great burden upon topological issues such as bond pad formation and fundamental area distribution of amplification circuitry.

For localised integrated conditioning chips, such as the derivatives of the early Najafi and Wise [3] devices along with the devices used by Dabrowski [4], Regehr et al. [5] and Pancrazio et al. [6] the parasitics effects were typically reduced due to the short track lengths between the working electrodes and the active signal buffers. However signal degrading effects were still reported that raised the effective noise levels. Typically the shorter the tracks between the electrode and the amplifier, the lower these effects will be. Once the signal has been amplified by active circuitry further effects of track and cabling noise will be much less significant, the effect being reduced by the gain level.

Placing a buffer directly below the electrodes will theoretically solve many of the problems associated with the track resistance and the parasitic interaction between the tracks and substrate. The methods of Jobling [7] and Fromherz, Eversmann [8] and Heer [9] provide a signal regeneration immediate to the sensing electrode. This provides an effective open circuit barrier between the measured signal and the electrode, thus regenerating the signal to a more stable level and eliminating any undesirable circuit noise and losses from the removal of the electrode to device connecting tracks. In these examples noise levels are a result of the interface, input transistor sizing, technology used and intrinsic and extrinsic circuitry noise.

3.2.2 Track and Cabling Noise

Random potential fluctuations occur in all electrical systems that are termed noise. Noise occurs as a result of several identifiable physical phenomena intrinsic and extrinsic to the system that are discussed within this section. This section concentrates on noise occurring within the interconnection between electrode and the front end system input. Other sources attributed to the biological interface and the active elements of an active MEA are discussed in chapter 5.

The signal to noise ratio (SNR) of a measurement system may be described as:

$$SNR(dB) = 20 \cdot \log_{10} \frac{V_s}{V_n} \tag{3.9}$$

As random noise is uncorrelated, the total uncorrelated noise of a given conducting track is calculated by the square root of the added squares of each noise source:

$$V_{noise}(total) = \sqrt{\left(V_{noise\_1}\right)^2 + \left(V_{noise\_2}\right)^2 + \ldots + \left(V_{noise\_n}\right)^2} \tag{3.10}$$

The sources of these noise components can come from conduction mechanisms, intrinsic material properties, external electromagnetic fluctuations, or environmental disturbances.

It is assumed that the time average of the track noise has no DC component, i.e. its time average is zero.

3.2.2.1 Thermal Noise

The first noise source under consideration is thermal or Johnson noise that is proportional to this resistance of the track from the electrode to the front end. This is calculated in terms of root mean square (rms).

$$V_{jn}(rms) = \sqrt{4kTRB} \tag{3.11}$$

Where :

k = Boltzman's constant = 1.38 x 10^{-23} J/K

T = Temperature of the conducting wire in K

R = Resistance of the conductive wire path Ω

B = Bandwidth in Hz

It is often more useful to convert the rms noise into a peak-to-peak value for purposes of comparison. The peak-to-peak value may be defined within certain confidence intervals with knowledge of its statistical behaviour. Thermal noise is characterised as white Gaussian noise. It is thus possible to define a peak-to-peak ($V_{pk\text{-}pk}$) value and percentage confidence that this value will not be exceeded over a given time period. This may be calculated by the normal cumulative distribution function for values around zero of which the rms value is one standard deviation. For confidence that the noise will exceed the predicted value only 1% of the time $V_{pk\text{-}pk}$ should be 5.2 times that of V_{rms}.

The average peak to peak magnitude of this signal is typically defined as:

$$V_{jn}(pk\_pk) = 6 \cdot V_{jn}(rms) \tag{3.12}$$

For a confidence interval of 99.9 %

In some cases the neural signals that are measured may not be much greater than the thermal noise occurring within the connective tracks. For a 100 Ω track at mammalian body temperature (310 K) and a signal bandwidth of interest between 0 – 20 kHz the noise resulting from these calculations would be 1.11 μV pk-pk. This value is quite conservative. Values greater than several kΩ may be experienced for larger paths and other track materials. The intrinsic noise of the track dictates the minimum signal level that may be accessed by the track. Care must be taken to ensure the noise from track resistance and track coupling does not exceed the intrinsic noise of the input signal for optimised design.

The importance of signal filtering to reduce noise can also be appreciated here. If the signal bandwidth were relaxed to 100 MHz, that of a well designed operational amplifier, the thermal noise contribution would become 78.5 μV, which may exceed the amplitude for small extracellular potentials.

Typically, thermal noise is simulated by a Gaussian distribution:

$$P(V_{jn}) = \left(\frac{1}{\sqrt{(2\pi)\sigma}} \right) e^{\frac{-V_{jn}^{\ 2}}{2\sigma^2}} \tag{3.13}$$

Where:

$P(V_{jn})$ is the probability of a voltage occurrence of value V_{jn}

σ is the standard deviation of the noise.

3.2.2.2 Shot and Flicker Noise

Shot noise occurs due to a quantized flow of current at a potential barrier typical of semiconductor diode or material phase barrier. As with thermal noise it follows Gaussian time and frequency domain characteristics.

For a semiconductor diode, this noise is described by:

$$I_s(rms) = \sqrt{2qI_{DC}B} \tag{3.14}$$

Where:
q is the charge of a single electron: 1.6 x 10^{-19} C.
And I_{DC} is the DC bias of the junction in Amps

Flicker noise is an empirical noise characteristic found in many passive and active devices that varies inversely with frequency. Flicker noise must be extracted experimentally from the device under scrutiny with its centre frequency and magnitude constant determined empirically. Flicker noise can then be described by:

$$I_{fn} \approx \frac{KI_{DC}\sqrt{B}}{\sqrt{f}} \tag{3.15}$$

Where:
K is the material constant that can also vary with device assembly.
I_{DC} is the DC current flow through the device.
B is the bandwidth centred around f.
f is the centre frequency.

Both of these noise sources will be assumed zero in the calculation of the track noise, but are included for completeness and for use later in the thesis.

3.2.2.3 Electromagnetic Interference

The conductive tracks of the MEA interconnect can act like an antenna, picking up electromagnetic signals passing through their position. This interference source can be defined as originating from near field or far field emission. Such interference sources are difficult to quantify exactly for a device as they are highly dependent upon position and environment.

Electromagnetic noise sources are governed by Maxwell's equations:

$$\begin{aligned} \nabla \times H &= \varepsilon_0 \frac{\partial E}{\partial t} \qquad & \nabla \cdot H &= 0 \\ \nabla \times E &= -\mu_0 \frac{\partial H}{\partial t} \qquad & \nabla \cdot E &= 0 \end{aligned} \tag{3.16}$$

Where ε_0 is the permittivity of free space ($\varepsilon_0 = 8.854 \times 10^{-12} F/m$) and μ_0 is the permeability of free space ($\mu_0 = 1.25 \times 10^{8} H/m$).

In a propagating wave, the time varying E and H fields cannot exist independently.

Far field interference typically originates from radio transmissions, wireless networks, mobile telephones, etc. Interference can therefore occur within a wide bandwidth of hundreds of kilohertz to several Gigahertz (100 kHz – 5 GHz).

A near field source is commonly defined as originating at a source within $\lambda/2\pi$ of the electromagnetic wave with wavelength λ (meters). Typical examples of near field sources problematic to MEA measurement are mains transformers, mains connected wiring, laboratory lighting and switched power supplies.

The impedance of the source is always important for near field characterisation due to its effect upon the emission as it is generated. Low source impedance emissions typically originate from high current flow within the circuit. This presents an electromagnetic emission with an increased relative magnetic field component H, over that of the electric field E in the propagating wave. The E/H ratio will be reduced below the standard far field impedance for free space:

$$E/H < 377\Omega \tag{3.17}$$

In this situation the H field will attenuate with a $1/r^3$ distribution at distance r from the source, whereas the E field will attenuate with a reduced $1/r^2$ distribution until the $\lambda/2\pi$ boundary is approached and both values are equalised allowing normal far field propagation from beyond this point.

The inverse is true for high impedance sources such as that emitted from ancillary analogue circuitry and digital devices. The E field will dominate the H field propagation component within the $\lambda/2\pi$ boundary causing the wave impedance to become:

$$E/H > 377\Omega \tag{3.18}$$

Near field noise can be much reduced by simply increasing the distance between the emission source and the MEA device, allowing the $1/r^2$ or $1/r^3$ attenuation to reduce the influence of the field. This however may be impossible in the case of most far field sources due to their considerable power output and the extent of electromagnetic signalling for everyday communication. The problem may be solved however by considering equation 3.16; if the E field component of the propagating wavefront encounters a conductive shield, it will dissipate. As one field cannot exist without the other and the H field is much smaller than the E field, the wavefront will cease at the

boundary. A conductive shield or Faraday cage surrounding the MEA and wiring will thus eliminate the effects of any external near and far field noise.

Additional noise reduction practices may be considered specifically for low impedance sources, whose transmission is governed mainly by inductive coupling. Reducing the track lengths of the interconnections on the MEA and correct normal orientation of directional emission sources relative to the track length will supply less flux coupling between the noise source and the tracks.

Immunity to high impedance sources may be increased by providing low impedance tracks and ensuring a differential measurement of the signal relative to a matched impedance ground on the MEA array connected to the extracellular domain, thus eliminating common mode artefacts. For circuitry integrated on and off the MEA, it is also good practice to ensure good low impedance grounding between all active devices and isolate digital components to ensure that a good measured signal is not contaminated.

3.2.2.4 Power Supply Noise

Supply noise is produced to some degree by most mains powered DC electronic power supplies. It is very difficult and often expensive to produce DC power supplies that do not retain some of the characteristics of the 50 - 60 Hz supply and the resulting conversion harmonics. Electronic devices that are powered with mains converters often translate the fluctuating harmonics within their supply into the analogue signals that are being amplified or filtered by active circuits.

The effects of this noise can be much reduced on ASIC devices by good power supply rejection ratio design and more simply by using well manufactured AC to DC converters or batteries to supply power. Typically all devices pick up mains supply noise to some degree. Many of the effects can be reduced by signal filtering techniques used after the input signal has been conditioned at the front end.

3.2.2.5 Noise Summary

Sub-sections 3.2.2.2 to 3.2.2.4 covered the many sources of noise that are applicable to both the passive MEA and the AMEA. These sources are summarised in figure 3.5 overleaf.

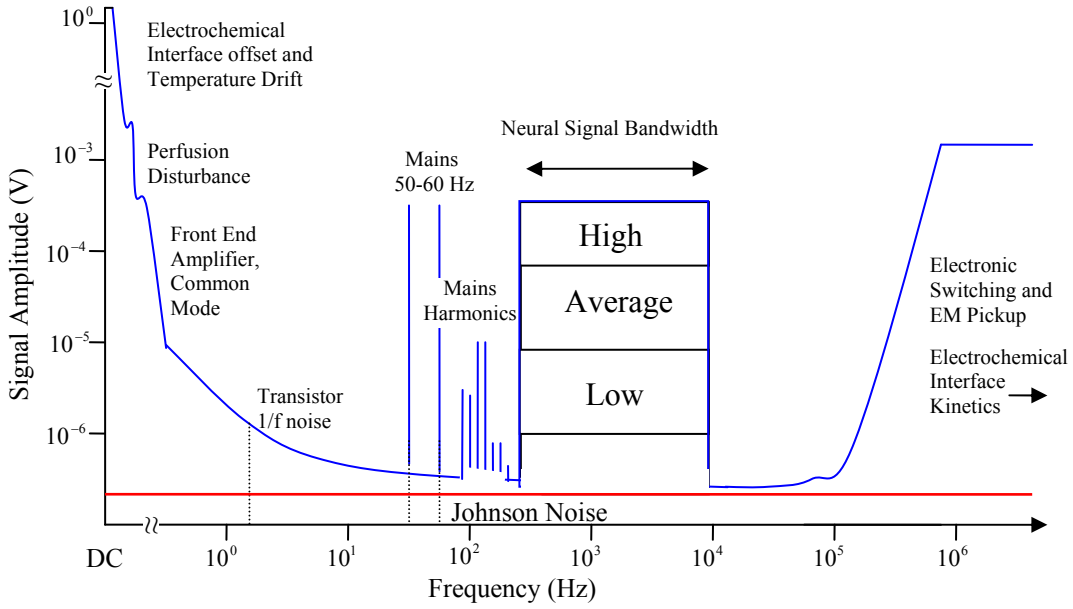

Figure 3.8

Illustrative summary of the many noise sources that may affect the MEA and AMEA devices. Also shown is the approximate bandwidth and amplitude of the neural signals of interest

As the bandwidth of the neural signals we are interested in is placed in a relatively interference free area of the spectrum, the use of filtering techniques to overcome the larger noise sources is possible. Electromagnetic noise, electrochemical interface noise and power supply noise can be greatly attenuated by filtering the signal, however careful system design and shielding will still be necessary for a high overall signal to noise ratio. Sensible electrode interconnection track design will also reduce the effect of the noise, both from intrinsic and extrinsic sources.

3.3 Analysis of the Interconnection Bottleneck

The interconnection bottleneck applies to both passive and active MEAs. The situation can be viewed as a design trade-off. For a planar single metal layer process, the number of interconnected electrodes present upon the MEA becomes proportional to the size of the electrodes and the inter-electrode spacing. The electrode size is typically defined in accordance to the size of the neurons soma or the groups of neurons it is desirable to measure. Likewise, the inter-electrode spacing should be relative to the spacing between the somas of adjacent neurons or defined by the intended spatial sampling of the neural network. It is difficult to immediately quantify these values when considering the variation between soma size, axon and dendrite lengths and distances between neurons and the typically random placing of cells within a dissected slice or culture; however, if we assume a regular structured network of equal size neurons we can begin to quantify the problem.

Assuming a cultured neural network in which each soma is 50 μm diameter and the centre to centre distance between each neuron is 100 μm, a simplified MEA would demonstrate an electrode diameter slightly less than the cell diameter with 100 μm centre to centre electrode spacing. The resulting configuration is a popular one amongst many commercially available MEAs.

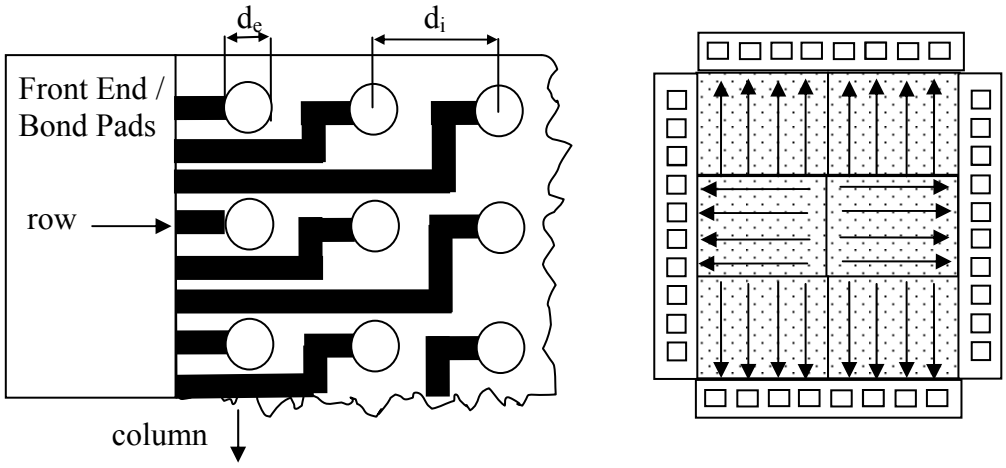

Figure 3.9

MEA interconnection diagram

By looking at the situation illustrated in figure 3.9 it is clear that the larger the number of columns of electrodes the greater the density of interconnecting wires become between the rows of electrodes. The number of columns n_c available with this topology will be proportional to the width of each interconnect; w, the electrode size; d_e and the inter-electrode spacing; d_i.

Roughly:

$$n_c = \frac{d_e - 0.5d_i}{w} \tag{3.19}$$

Without consideration of the processes minimum track spacing and the carried signals tolerance to resistive breakdown between tracks.

This gives the maximum number of allowable electrodes; e_{max} as:

$$e_{\max} = n_r \cdot n_c = n_r \left[\frac{d_e - 0.5d_i}{w} \right] \tag{3.20}$$

where n_r is the number of rows according to figure 3.9,

As a possible solution to include more rows, each interconnection track could be thinned, but would result in a proportional increase in resistance, resulting in greater track susceptibility to track parasitic issues discussed in section 3.2. This may also be limited by fabrication technology.

Commercial MEAs typically provide perimeter bond pad connections that are passively connected to each individual electrode. This positioning has the dual purpose of loosening the interconnection constraints of wiring density between and around the microelectrodes and providing a large easily accessible set of connections for off-board wiring to conditioning and analysis equipment. Such devices are typically produced with no more than 60 electrodes due to interconnection density issues and retaining bondpad accessibility; see figure 3.2a. An example of such an electrode and bondpad arrangement configuration is presented in figure 3.9b above.

For such an arrangement of electrode, bondpad and interconnection as that shown in figure 3.6b, whereby the array is composed of interconnect routed blocks similar to that of figure 3.1a, the number of available electrodes according to the variables of equation 3.13 is six fold. If a square arrangement is necessary, the increase would be reduced to four fold. Differing array topologies are often used for specific tasks, including circular electrode arrangements with similar results

Many high density designs have incorporated track tapering to lower the overall effective resistance of the channel and reduce the effects of noise and parasitics. Such designs are still limited by process parameters and the ability of the tracks to taper to larger widths within the electrode matrix.

3.4 Improvement by Integration

Research had been conducted into MEA development by the electronic integration of some of the functional blocks described in section 3.1.3 as reviewed in chapter 2.
Early examples of microfabricated arrays with closely positioned devices were published by Bergveld [10] and Wise and Angell [11] in which buffers were positioned on the supporting substrates of microelectrode arrays to objectively elevate the extracellular signal measured by the microelectrode above the noise level of the interconnecting tracks and greatly reduce the cable losses incurred in the passive MEA between the electrode and off-board amplifier

This concept of close proximity active support was further developed Jobling et al. [12] in 1981. Seeking to reduce the losses and noise from the signal path, the group took the next logical step from passive microfabricated arrays to active arrays by integrating buffer amplifiers directly beneath the electrode. The Jobling device suffered from unavoidable power supply noise that reduced the baseline sensitivity of the device to 50 μV, however this was lower than that presented in other contemporary microfabricated MEA research.

The many active devices that followed over the next two decades seemed to favour the development of Wise-type close proximity integrated solutions rather than the active electrode format of Jobling, possibly because of the additional Field Effect Transistor (FET) processing steps required to stabilize the device for immersed use in physiological saline. Possibly this was also because the development of such prototypical devices with little interconnection requirements; off-board custom Application Specific Integrated Circuits (ASIC) are more flexible to develop and test. The development of 16, 32 and even 64 electrode microelectrode arrays with sub 100 μm spacing is still below the limit to sufficiently challenge the interconnect spacing and routing bottleneck to the closely positioned supporting ASIC, and so fabrication of the integrated front end was not an issue. Also, the cost of the silicon per mm² would be prohibitive for these designs using conventional industrial processes. Much post processing would also be. To reduce these

dependencies, the microelectrode arrays were produced separately, reducing total processing by placing the active integrated circuitry on a separate substrate for later wire bond connection.

The supporting ASICs developed by Wise et al, Najafi et al, Pancrazio et al, Oka et al, Krause et al and those that followed demonstrated that closely positioned conditioning ASICs much reduced the noise, as low as several μV rms and signal losses of the early MEAs and allowed integration of additional local functionality such as filtering, channel multiplexing, digital conversion and RF telemetry. Each of these integrated functions increased the appeal of the devices compared to the traditional MEA by reducing device dependencies and functional application specific restrictions of cabling and cumbersome connections.

However, as the need for more microelectrode recording sites increases to provide optimally spatially sampled signal recording from larger networks, providing the interconnection between the electrode and the conditioning circuitry will prove difficult.

3.4.1 Integration Area Issues

The integrated conditioning circuits take up a substantial on chip area. For each electrode present on the device a corresponding front end circuit must be used to condition the signal of that channel before it can be observed and analysed by the researcher.

The circuits must first condition the signal to comply with the operating ranges of the amplifiers used in the front end. Problematic DC potential offsets and drift caused by the electrode interface to the neuron and extracellular fluid must first be dealt with. These phenomena are discussed in further detail later in the thesis, but at the present time it is only required to know that they exist.

A front end high pass filter stage is normally the first conditioning block the delicate neural signals encounter. In off board systems, where component area is not at a premium, large elaborate filtering systems can be easily assembled that use many discrete packaged chips mounted on one or several large printed circuit boards. As previously discussed the versatility available from off board circuitry is unfortunately severely limited for large scale applications where small neural signals are to be studied.

With a fully integrated solution, all of the active and passive components have to be provided with space on die for the design. This can be a problem both for sophisticated low noise amplifiers and the passive circuit components such as capacitors and resistors that are necessary to stabilise amplifier gain and filter characteristics. Capacitors and resistors are the fundamental building blocks of passive and active filter circuits and unfortunately to produce them with a standard CMOS process they require a high surface area compared to their discrete counterparts.

Filter circuits are governed by the relation:

$$f = \frac{1}{2\pi RC} \tag{3.21}$$

where:

R is the resistance of the circuit.
C is the capacitance.
f is the corner frequency of the filter where the signal will attenuate by 3 dB.

For the 300 Hz to 6 kHz bandwidth usually attributed to neural signals, a 5.31×10^{-4} s·rad^{-1} to 2.65×10^{-5} s·rad^{-1} RC time constant must be provided. To provide for such time constants a relatively large area of silicon must be consumed in the design simply by the filter passives.

Assuming a differential input to each amplifier in the conditioning circuitry, a front end high pass filter providing a 300 Hz cut-off frequency formed using a typical 0.35 µm CMOS process utilizing minimum width resistors, will occupy an area roughly calculated by:

$$2 \cdot \left(70\,\Omega/\mu m \cdot L_r \cdot A_c \cdot 1\times10^{-15}\ F/\mu m^2\right) = 5.31\times10^{-4}\, s \cdot rad^{-1} \tag{3.22}$$

Where:

L_r is the polysilicon resistor length.

A_c is the capacitor area.

s is seconds.

Assuming that the polysilicon resistor is formed by snaking into a given area A_r it can be calculated by:

$$A_r = L_r \cdot w_{r\_\min} \tag{3.23}$$

Where w_{r_min} is the minimum track width of the poly-resistor.

Substituting 3.19 into 3.18 then gives:

$$2 \cdot \left(70\,\Omega/\mu m \cdot \frac{A_r}{2 \cdot w_{r\_\min}} \cdot A_c \cdot 1\times10^{-15}\ F/\mu m^2 \right) = 5.31\times10^{-4}\, s \cdot rad^{-1} \tag{3.24}$$

Where the factor of 2 multiplication accounts for minimum spacing between the snaked polyresitor tracks.

This gives:

$$A_c \cdot \frac{A_r}{w_{r\_\min}} = 7.59\times10^{9}\,\mu m^3 \tag{3.25}$$

For a 0.4μm track width polyresist, this becomes:

$$A_c \cdot A_r = 3 \times 10^9 \, \mu m^4 \tag{3.26}$$

Now, for compact design a minimum perimeter structure is preferable to keep each conditioning channel modular and its components together. This is provided by a square device topology. The overall perimeter is also at a minimum when both resistor and capacitor are of equal size; $A_c = A_r = A$.

From this, equation 3.19 can be rewritten as:

$$A_c \cdot A_r = A^2 = 3 \times 10^9 \, \mu m^4 \tag{3.27}$$

Where the total occupied area A_{total} for each device is:

$$A_{total} = 2A \tag{3.28}$$

From this we can calculate that a minimum area for a differential high or low pass filter stage with a 3 dB cutoff at 300 Hz would require 109.5 x 10^3 μm^2 of area, occupying 468 x 468 μm^2 per channel per filter stage per passive type. In the same 0.35 μm process, a well designed open loop amplifier may only occupy a 150 x 150 μm^2 area or smaller.

For this particular application, due to the need for a high pass filter to prevent amplifier saturation and the small value of the filter cut-off frequency, passive integrated components will dominate the on chip area by over 9:1, assuming the active area stated above.

The number of devices available on chip will be dictated by the passive rather than the active amplification circuitry. This will be problematic in terms of device cost and will

become a limiting factor as the array becomes large, in that the active area occupied for each channel becomes much larger than the desired inter-electrode spacing for optimal spatial signal observation.

There are few applications where an integrated solid state continuous time filter is required with such a low cut-off frequency and thus very few refined solutions to this problem. However, several possible area reduction techniques are possible by replacing the standard polysilicon resistor path with modified active circuit elements.

One solution is the use of a silicon diode structure. A simple p-n^+ diode biased at 0V, will for small voltages less than kT/q, show ohmic characteristics with resistance $R_{p\text{-}n}$ approximated by:

$$R_{pn} = \frac{4kT}{q^2} \frac{\tau}{A_{pn} n_i W_D} \tag{3.29}$$

Where:
k is Boltzmans constant.
T is temperature in K.
q is the fundamental electronic charge.
τ is the carrier lifetime.
A_{pn} is the area of the pn junction.
n_i is the concentration of intrinsic carriers.
W_D is the width of depletion.

This method was used by Najafi and Wise [3] to provide dc baseline stabilisation where good ohmic behaviour was experimentally observed between ± 12 mV for a 750 μm² area device in an early 6 μm process. The device demonstrated a 1.4 x 10^{10} Ω resistance; however non linearity and noise were not discussed.

A second method involves using diode connected MOSFET transistors to provide a pseudo-resistance from the resulting parasitic p-n-p bipolar structure. For low voltages, such a structure has been shown to demonstrate high predictable resistance (>10^{12} Ohms) for constant voltages. This resistance however, was shown experimentally [13] to vary exponentially with the input voltage; a 0.2 V increase in voltage causing the resistance to vary by three orders of magnitude. The device benefited from a small (4 μm x 4 μm) area and required no external biasing.

A third method, used recently by Heer et al. used a MOS transistor with gate length 100μm and width 1μm as described in [14]. The resulting MOS resistor provided a voltage controllable value between 800 MΩ and 800 GΩ, allowing a tuneable cut-off between 1 Hz to 1 kHz. The device is characterised by:

$$R = \frac{1}{G_m} = \frac{L}{W}\frac{1}{\mu C'_{ox}(V_{GS} - V_T)} \tag{3.30}$$

Where:

μ is the carrier mobility.

Cox is the oxide capacitance.

L and W are the device Length and Width respectively.

V_{gs} is the control voltage at the gate of the transistor.

VT is the threshold voltage of the transistor.

The paper achieved unusually high values for the MOS resistor and it was not stated whether the transistor was operated in sub-threshold to achieve this value. The parasitic capacitances resulting from the long device and their effect upon the filter characteristics were not discussed. In addition, such a large feedback resistance must impart a large source of noise into the device according to equation 3.11 that could potentially swamp the signals the device intends to measure. The MOS resistor method is also used by Debrowski et al. although to a much lower resistance value.

Sub-threshold MOS transistors have been used by Mohseni and Najafi [15] and follow:

$$R = r_{ds} \cong \frac{L}{n\mu C_{ox} W V_t} \exp^{\left(-\frac{V_{GS}-V_T-nV_t}{nV_t}\right)} \tag{3.31}$$

Where:
n is the sub-threshold slope factor and the rest of the symbols are as above.

Also, PMOS transistors inherently display higher on chip impedance as hole mobility is approximately two to three times less than that of electrons in silicon.

Using the sub-threshold device in this way, several hundred Megaohms of resistance were achieved within a 5 μm x 25 μm area of the device.

Other methods for achieving low frequency filters such as MOSFET-C integrators and electronic multipliers [16] have been shown to demonstrate favourable area reduction. However due to the switching schemes required so close to the electrodes and signal carrying tracks it was deemed to be to noisy for the immediate front end. Such devices also require additional active circuitry, causing higher power and routing overheads to the device.

Each of the above methods reduces the resistive overhead considerably and also drives back the need for a large capacitance in accordance to equation 3.18. For the larger resistances approaching 1 GΩ, the area required by the capacitor from equation 3.20 would reduce to 531 μm^2 or 23 x 23 μm^2 per input of the differential system, as only 0.531 pF of capacitance would be required to achieve the necessary filter cut off frequency.

Each of these methods, although presenting immediate attraction for reducing the passive area consumption may present non ideal effects and higher device complexity, making such devices difficult to use. Sub-threshold devices are exponentially sensitive to

temperature fluctuations and source voltage changes, variables that are difficult to predict and control during operation. Also, the use of resistances approaching tera-ohms to compensate for small capacitive circuit elements may exceed the resistance of the layers of the microfabricated device. This may cause unpredictable operation and greatly increase the devices susceptibility to channel cross talk, near field noise, thermal noise and parasitics.

Even without the presence of such phenomena, we are still left with a relatively large area necessary for the remaining capacitance value to achieve the filter characteristic cut-off. The poly-poly capacitors used by Harrison [13] consumed 67% of each amplification circuit block. Similarly Heer was left with approximately 4400 μm² (58.7 μm x 89.4 μm) of capacitance area which constituted 25 % of a larger, fully differential filter circuit even with an 800 GΩ resistive component.

3.5 Proposed Active MEA Design

The first three sections of this chapter developed an analytical examination of some of the most prevalent problems associated with MEAs. Knowing the characteristics that govern these issues it is possible to consider the development of an optimised solution that maximises the number of available electrodes and minimises the effects of the undesirable elements by design. The remainder of the chapter considers the design solution with reference to the concepts developed in the first four sections and discusses how its development will be laid out through the rest of the thesis.

3.5.1 Front End Design

It was decided that a fully integrated front end would be developed to ensure that a high impedance measurement of the neural signal is possible and that the signal voltage and current is amplified at the source to reduce signal losses, distortion and noise. By amplifying the signal at the source the electrical constraints of the signal path are loosened and higher density signal interconnections are possible without reducing the signal quality. IC technology also allows other functional components such as channel switching and multiplexing to be incorporated directly into the design, thus further reducing the interconnection demands and the resulting channel bottlenecks.

The front end design was developed by considering the pros and cons of the various techniques currently used for active extracellular signal recording arrays. The front end circuitry used can be split into two main groups:

1. The single transistor method used by Fromherz et al.
2. The whole amplifier technique used by Heer et al.

The Fromherz technique, illustrated in figure 3.10 was described in section 2.4.1. Fromherz uses a single transistor placed beneath the neuron to modulate the transistor drain current I_D with the extracellular cleft voltage that is coupled to the gate. This method appears compact in that only requires a single transistor to be placed beneath each neuron. However, the transistor still requires an amplification stage to convert I_D back to a voltage signal with appropriate driving current for external measurement. For single transistor devices the drain and source voltages are modified to ensure that the gate voltage V_{GS} is at the correct bias point for measurement. The value of the amplifier reference source V_1 is also matched to the gate offset to ensure that the amplifier output offset is controlled. This method is not feasible for large arrays.

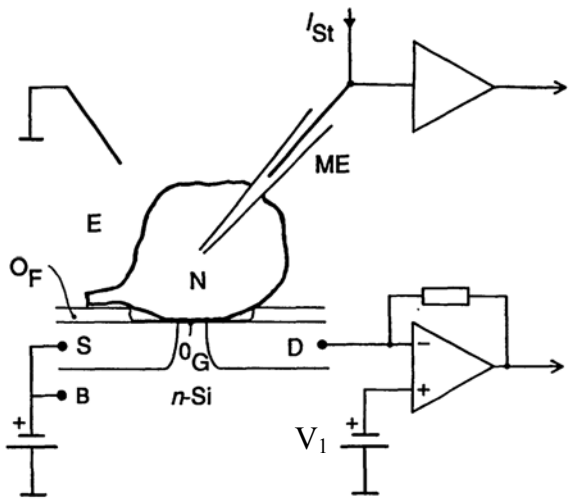

Figure 3.10

The measurement circuit for the Fromherz method: taken from [17]. The stimulus arrangement is also shown connected to node ME.

When extended to large arrays, the Fromherz method requires switched calibration at the gate of the transistor sensor. This ensures that each transistor is operating at a similar current and alleviates effects of process variations such as the value of the threshold voltage V_T.

Calibration is performed by setting the transistor gate voltage to an appropriate value by momentarily diode connecting the device [8, 18]. The duration of the switched diode connection is calculated to be long enough to charge the gate of the transistor but short enough to prevent dc shorting of the I_D current through the electrode to the ground potential of the extracellular fluid. Shorting through the electrolyte will occur the electrode interface will become a good dc conductor for potentials larger than approximately ± 1 V; the electrochemical reactions causing this are explained in chapter 6, section 6.13. The potentials of the transistor drain will exceed this potential window during diode connection as the current path to ground for the Fromherz device is large due to the connection to the current to voltage amplifier.

The small area of the input transistor increases the thermal and 1/f noise of the signal. For large arrays with switched calibration this is combined with high frequency switching noise and gate drift between calibration periods. The state of the art Fromherz inspired array exhibits a noise of 250μV rms [8, 18]. This device has 16,384 recording sites with transistor electrode pitch of 7.8 μm x 7.8 μm suitable for high spatial resolution imaging of small, sub 20 μm mammalian neurons. The advantage of the Fromherz method is very high spatial resolution imaging but the downside is increased complexity from calibration and switching circuitry.

An additional issue with the Fromherz array is power consumption. The transistors must be used in the saturation region to ensure that the transistor remains on and that the current signal responds in a linear way. For high density arrays using switched channels the current must also be adequate to give fast settling times. This presents a large thermal power dissipation burden upon the circuit requiring heat sinking and active cooling techniques to ensure that the neurons are not damaged by the measurement equipment.

The full amplifier method may be configured to give very low input referred noise [13], subthreshold transistor operation for low power and low thermal dissipation and can amplify both the voltage and the current of the signal above the interference and electrical imperfections of passive interconnections. This is the ideal circuit to place at the source of the signal. This removes the need for external amplification circuitry; the circuit is fully analogue and does not have the added complication of switching.

However, the disadvantage of this method is that the circuit size will be much greater. This is caused by the additional transistors that make up the amplifier circuit and much more importantly the need for passive circuit elements (discussed in section 3.4.1) to remove the interfacial potential of the electrode. This is not a problem associated with the Fromherz device as there is no voltage gain associated with the transistor input.

Methods have been developed to reduce the area of passive components for low frequency continuous time high pass filters. It has been shown that by using subthreshold

MOS resistors, this passive area may be much reduced. However, non-ideal aspects of these circuit elements must be characterised and weighed against their benefits. The use of a subthreshold 800 GΩ MOS resistor may present unwanted nonlinearities and create large offset voltages due to the gate leakage current of the device. Also, the capacitance, although it is a small value still requires a substantial area of the circuit if one thinks at a neuron size scale. The use of small capacitor values to form the RC product will be problematic in terms of correct matching and parasitic control. The large total impedance presented at the input of the amplifier will make the device more susceptible to near field noise emitted from other circuit components, especially digital.

There is an important balance between R and C when considering CMOS implementation that enforces an unavoidable scaling bottleneck upon the front end design, thus reducing the effectiveness of on site active front ends for high density applications. The use of high value active resistance elements on chip has pushed back the extent of this area to some extent but fundamental limitations of device operation and process dependent matching considerations presents a definite limit. For optimal scaling, it is a major motivational issue to reduce or remove the dependence of these devices upon such large passive circuit elements.

The full front end amplifier method presents a superior method for neural signal measurement with comparison to the Fromherz method. The compromise is the integrated area that is required. This is strongly dependent upon the need to use dc blocking capacitors to remove the input offset and drift of the electrode-electrolyte interface.

The following chapters investigate the electrical properties of the neural signal and the electrode-electrolyte interface to identify the minimum requirements of a front end amplifier circuit. This is approached with a view to reduce the physical size of the integrated circuit to an area equivalent to that typically occupied by neurons on the MEA substrate in vitro.

3.6 Summary

Key aspects of the MEA have been investigated to determine the effects upon the recorded signal as the electrode and recording channel density increases. Problems intrinsic to the high impedance signal source and the measurement device, such as channel routing, track resistance and fabrication parasitics were shown to limit the signal level, recording density and ultimately the effective number of available channels.

Integration of active CMOS electronics within the MEA package provides improvement to many of these problems; however it is difficult to fabricate CMOS continuous time filters within the small surface area available.

The best active MEA solution to give the best signal to noise ratio, lowest circuit complexity and lowest thermal dissipation was identified as the full amplifier method. The disadvantage of this method is the need to remove the dc potential and drift caused by the electrode-electrolyte interface. It was determined that if an alternative solution could be found to remove the need for integrated capacitors and resistors, this method may be used to fabricate an input amplifier small enough to fit beneath the recording electrode as part of a high spatial resolution active MEA. This would then present an active MEA solution that will bridge the spatial resolution gap between the Heer method and the Fromherz method whilst retaining the high dynamic range and simplicity of the full amplifier method.

3.7 References

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Chapter 4

Development of an Electrical Neuron Model for Computer Simulation

In this chapter an electrical model of the neuron and its environment is developed to aid the design of the front end circuitry of the multi-channel extracellular signal measurement IC. Modelling is a useful tool when access to real neural signals is not immediately available to the research or when specific physical properties are difficult to control during experimentation.

The model presented in this chapter is a novel culmination of many previously published models that have been refined to define the best available electrical description of a neuron and the mechanisms for extracellular measurement. The model was developed in the electronics industry standard format: SPICE to ensure portability and immediate accessibility of the concepts to electronic engineers.

The model contains the nonlinear electrical membrane model of Hodgkin and Huxley [1] to define the behaviour of the cell membrane. This is used together with geometrical descriptions of the neuron components; including the membrane area and intra- and extra-cellular space as defined by Cupitt [2], Roth et al. [3], Frijns et al. [4] and Rattay [5,6,7], used previously to describe and predict magnetic and electrical stimulation of neural tissue. The model is completed by modelling the extracellular electrical connection between the neuron and a planar microelectrode using the extracellular 'cleft' models

identified by Regehr [8] and Zeck and Fromherz [9] to explain the amplitude of neural signals recorded using planar MEAs.

The model consists of a compartmental model combined with a passive model of the neuron's electrolytic extracellular environment *in vitro*, complete with planar recording microelectrode positioned at the substrate. Extracellular signal measurements are defined between the recording electrode and a reference electrode in the bulk of the extracellular space. Strong electrical coupling between the neuron and the recording electrode is described by the sealed electrical cleft model. Weak coupling is described using volume conduction. A block diagram of the model overview is presented in Figure 4.1.

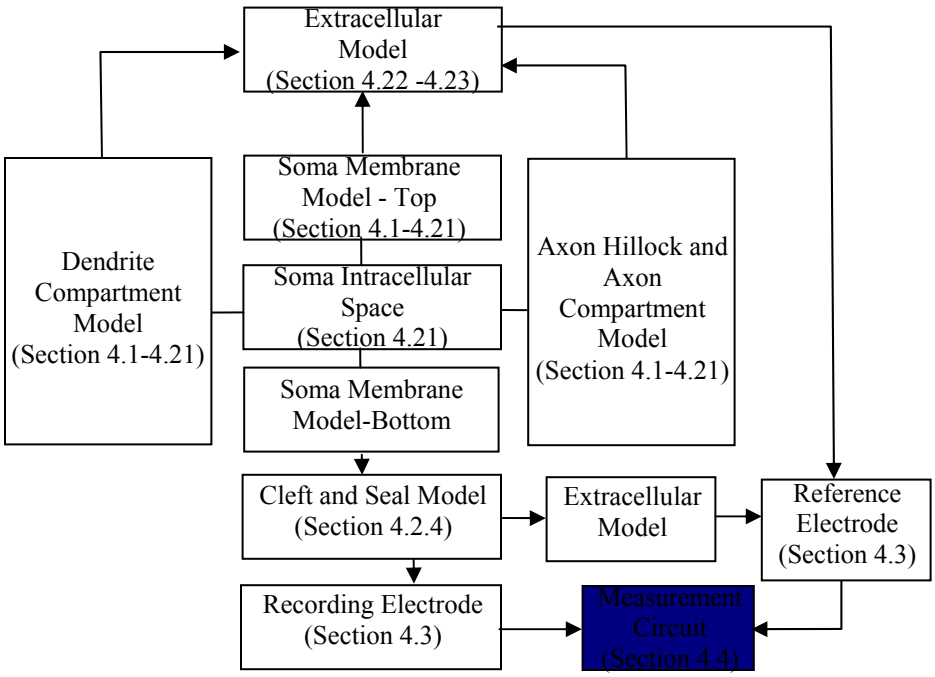

Figure 4.1

Overview of the *in vitro* planar microelectrode model including corresponding chapter sections for each modelled component.

The model is prepared for SPICE simulation using a novel SPICE-VerilogA method for describing the differential Hodgkin and Huxley ion channel equations. This removes the need to characterise and employ complex circuit models based upon standard SPICE

library components [10] or modify and recompile the original SPICE source code [11] to simulate the differential equations of the voltage gated channels in the SPICE environment.

This chapter begins by identifying a suitable membrane model and building a two dimensional electrical circuit description of a neuron. Electrical parameters are calculated from a compartmental approximation of the physiology that is developed from peer reviewed methods. Following this, the extracellular space is defined by an approximation of the node to node resistance of the extracellular space and volume spreading resistance for each extracellular node to the solution bulk. The theory of planar microelectrode recording is then added to the model. This includes the electrical modelling of the physical coupling between the neuron and the recording electrode through the cleft, the seal resistance and a basic microelectrode model. Finally a model of the measurement circuit load is also included for completeness.

4.1 The Active Membrane

The basic neural theory presented in Chapter 1 described the signal propagation mechanism of the neuron as electrical through ionic charge manipulation at the cell membrane. The cell builds up a resting potential across the membrane by controlling the concentration of K^+ and Na^+ ions within the intracellular fluid. Signal propagation occurs by the depolarisation of this potential as voltage gated ion channels open in response to localised potential changes. These potential changes may be elicited by the localised current flow of a propagating action potential or initiated by sensory receptors. The opening and closing response of the ion channels describe the observed finite current flux across the membrane, giving the action potential its characteristic shape.

Channel opening and cell depolarisation may also be artificially induced by current injection. This observation enabled electrical characterisation of these channels to be performed in a controlled repeatable manner. The identification of ion channel specific toxins (Tetraethylammonium (TEA) inhibits K^+ channels, tetrodotoxin (TTX) inhibits

Na^+ channels) also allowed the individual contribution from individual ionic pathways to be identified during stimulation.

The electrical characterisation of living neural membrane by this method was pioneered in 1952 by Hodgkin and Huxley for the squid giant axon, for which they were awarded the Nobel Prize in 1963 [1]. Many other investigators have since used this method to characterise the behaviour of different neural membranes from many different species.

The membrane models, when incorporated with physical models of the investigated system, are typically used in the prediction of pharmaceutical or Functional Electrical Stimulation (FES) techniques such as cochlear prosthetic modelling. The simulated membrane response offers close prediction of actual neural tissue as it is based upon empirically extracted data.

As these membrane models accurately describe activation, depolarisation and current flux they may also be used to simulate the neuron as an electrical signal source.

4.1.1 The Hodgkin and Huxley Model

This model describes the cell membrane of a neuron as an electrical circuit. The electrical properties of the membrane are described as resistive or capacitive elements as shown in figure 4.2 and relate the intracellular potential of the neuron V_i relative to the extracellular potential V_e.

The circuit consists of a compartmental unit area membrane capacitance c_m, the ionic potentials E_{Na}, E_K and E_L, the variable unit area channel conductances g_{Na} and g_K, and the unit area leakage conductance $\bar{g}_L$. The opening of these conductance channels gives rise to the current densities i_{Na}, i_K and i_L. The Na, K and L subscripts indicate the specific pathway of the potential and resistance, with Na representing sodium ions, K representing potassium ions and L representing an additional leakage pathway that was included to

account for chloride and other ions that are not active, or make a small contribution to the process.

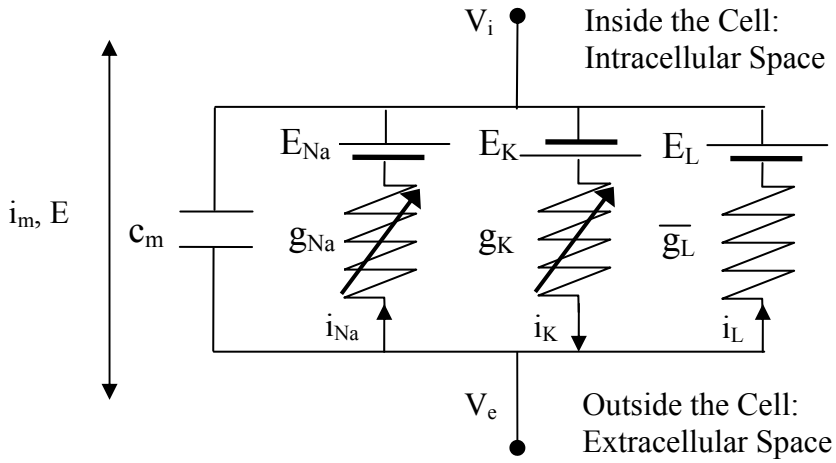

Figure 4.2

Electrical equivalent circuit of the cell membrane; reproduced from [1].

Cell depolarisation is described in terms of the currents i_{Na}, i_K and i_L that are characterised by the change in channel conductance and the channel potential according to Ohms law such that:

$$i_{Na} = g_{na}(E - E_{Na}) \quad 4.1$$

$$i_K = g_K(E - E_K) \quad 4.2$$

$$i_L = \overline{g}_L(E - E_L) \quad 4.3$$

Where the g terms are channel conductance variables per unit area. g_{Na} and g_K are variables in time and are discussed further in the next section, $\overline{g}_L$ is a time invariant constant. E_{Na}, E_K and E_L are the equilibrium potentials of the channels and E is the membrane potential.

The total membrane current is divided into corresponding capacitive and ionic components:

$$i_m = c_m \frac{dV}{dt} + i_i \qquad 4.4$$

Where i_m and i_i are the membrane current and combined ionic current per unit area respectively, c_m is the membrane capacitance per unit area. V is the displacement of the membrane potential from its resting value and t is time.

The ionic current i_i, per unit area is the sum of the channel specific ionic currents per unit area, so that:

$$i_i = i_{Na} + i_K + i_L \qquad 4.5$$

Equations 4.1-4.3 may be written in terms of a 'displacement voltage' V, as described by Hodgkin and Huxley, to normalise the model around zero volts:

$$V = E - E_r \qquad 4.6$$

where E_r is the resting potential of the unexcited neuron.

For the model described in this chapter such simplification is avoided to produce a physiologically accurate SPICE model.

Equation 4.4 is typically written in terms of the individual ionic contributions of equation 4.5 given as in equations 4.1 - 4.3. The displacement voltage V may also be substituted by E in this case:

$$i_m = c_m \frac{dE}{dt} + g_{Na}(E - E_{Na}) + g_K(E - E_K) + \overline{g}_L(E - E_L) \qquad 4.7$$

4.1.2 Characterising the Ionic Conductance

Equation 4.7 presents the general equation for a three channel model of the membrane. The constants c_m, $\bar{g}_L$ and the variables g_{Na}, g_K may vary between species or type of neural tissue and must be evaluated experimentally.

Using channel selective toxins to individually disable the Na+ and K+ voltage gated channels, the behaviour of each channel type was observed. The recruitment of channels relative to a steady state potential across the membrane was demonstrated with respect to time by the simultaneous measurement of the membrane current. As the voltage across the membrane was held constant during each successive measurement, capacitive current contributions were eliminated.

It is believed that individual channels operate by a probabilistic nature whose lumped contributions could be described by:

$$g_{Na} = m^3 h \bar{g}_{Na} \qquad 4.8$$

$$g_K = n^4 \bar{g}_K \qquad 4.9$$

Where $\bar{g}_{Na}$ and $\bar{g}_K$ are constants of the measured maximum conductance values for each channel. The variable m is known as the sodium channel activation parameter. This particular variable determines the probabilistic recruitment of sodium channels towards an 'open' state given a certain displacement voltage in time. The m parameter varies between zero and one according to equations 4.10 and 4.11.

The *h* parameter represents the sodium channel's inactivation characteristics, in that once activated 'open' channels seemed to return to a 'closed' state. The probability that a sodium channel will be in a state of inactivation during displacement of the membrane potential is (1 - h). The sodium conductance is thus described in terms of voltage

displacement and time according to the product of equation 4.8. The third power of m is needed to describe the observed build up of g_{Na}.

The n parameter is the potassium channel activation parameter. The principle of operation is similar to that of m, with the fourth power dependence providing slower build up characteristics for the potassium current. The potassium channels were observed to have no associated inactivation characteristic and are accordingly only described in terms of the n parameter.

The activation and inactivation parameters are governed by the following differential equations:

$$\frac{dm}{dt} = \left[\alpha_m(1-m) - \beta_m \cdot m\right] \cdot K \qquad 4.10$$

$$\frac{dh}{dt} = \left[\alpha_h(1-h) - \beta_h \cdot h\right] \cdot K \qquad 4.11$$

$$\frac{dn}{dt} = \left[\alpha_n(1-n) - \beta_n \cdot n\right] \cdot K \qquad 4.12$$

where $\alpha_m, \beta_{m,} \alpha_h, \beta_h, \alpha_n$ and β_n are rate variables that vary only with voltage and are calculated by empirical equations based upon experimental observation. For the squid giant axon model K is a temperature correction term that is calculated by:

$$K = 3^{0.1T-0.63} \qquad 4.13$$

where T is temperature in °C.

K may also be varied to account for faster gating processes observed across different cell types as described by Rattay [12]. The relationship between K and the duration of the

action potential may be determined empirically from the Hodgkin Huxley model to assist in fitting the general model to faster or slower neural signals. The relationship between the peak to peak time of the cleft action potential (CAP) T_{pk} and K is illustrated in figure 4.3.

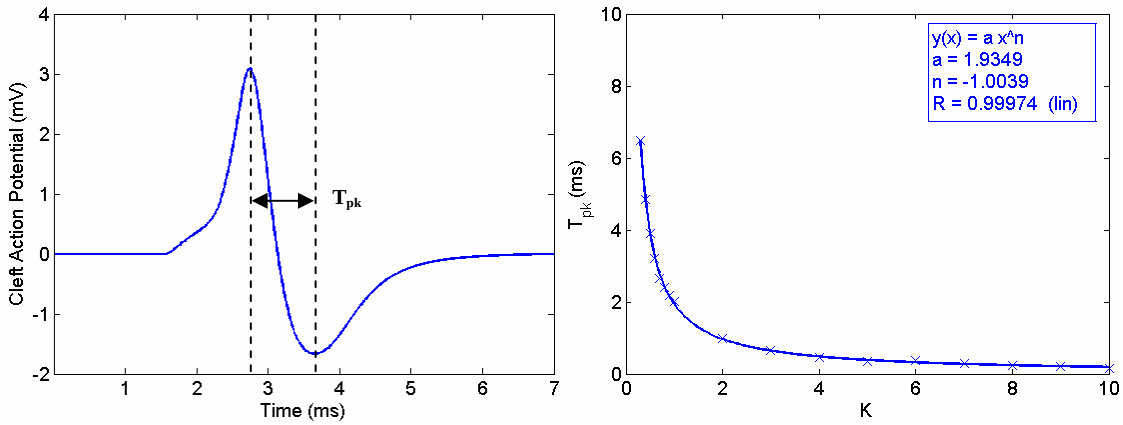

Figure 4.3

Relationship between K and peak to peak time T_{pk}

The value of K may be chosen for a given peak to peak time according to equation 4.14:

$$K = \frac{1.935}{T_{pk}} \qquad 4.14$$

By substituting the numerical values of m_0, h_0 and n_0 into equations 4.11 and 4.12 the ion specific conductance of each channel can be calculated during the resting phase of the membrane.

In the model the rate variables are described by:

$$\alpha_m = \frac{0.1(V_d - 25)}{\exp\left(\frac{V_d + 25}{10} - 1\right)} \qquad \beta_m = 4 \cdot \exp\left(\frac{V_d}{18}\right) \qquad 4.15$$

$$\alpha_h = 0.07 \exp\left(\frac{V_d}{20}\right) \qquad \beta_h = \frac{1}{\exp\left(\frac{V_d + 30}{10} + 1\right)} \qquad 4.16$$

$$\alpha_n = \frac{0.01(V_d + 10)}{\exp\left(\frac{V_d + 10}{10} - 1\right)} \qquad \beta_m = 0.125 \cdot \exp\left(\frac{V_d}{80}\right) \qquad 4.17$$

where the dimensionless displacement voltage V_d is scaled for the SPICE model as:

$$V_d = 1000 \cdot \text{Volts}^{-1} \times (E - E_r) \qquad 4.18$$

When in the resting state, the membrane must remain semi-permeable to the Na^+, K^+ and Cl^- ions in order to retain the cell resting potential described in section 1.2.2.2. This phenomenon is retained within the empirical rate constants due to a small baseline ionic conductance level that is present when the cell is clamped at its resting potential during the voltage clamp parameter extraction. The baseline channel activation is calculated for equations 4.10 – 4.12 by assuming that $V_d = 0$ and is used for initial conditions at t = 0.

This gives:

$$m_0 = \frac{\alpha_m}{\alpha_m + \beta_m} \qquad 4.19$$

Initial conditions for h_0 and n_0 are calculated accordingly.

4.1.3 Summary

Section 4.1 introduces an electrical model for the cell membrane and defines the equations that will be developed and used in the SPICE model of the neuron membrane.

This includes a description of the membrane scaled to the physiological situation of geometrical model of a neuron. By using an electrical model that quantitatively describes the dynamics of the ion channels a good approximation of the neurons electrical signals may be simulated for the planar microelectrode recording environment. The connectivity between the model neuron, the extracellular space and the measurement circuit are described in the following sections with connectivity as shown in figure 4.1.

4.2 Electrical Model of the Neuron

A geometrical model of the neuron physiology was developed from which scaled equivalent component values for a two-dimensional cable equation could be calculated. The model, shown in figure 4.3, consists of four discrete compartment geometries defining the dimension and shape of the dendrite, soma, axon hillock and axon. Each compartment can then be broken up into a series of nodes of length Δx to provide spatial distribution of the active membrane, demonstrate the propagation of membrane depolarisation and its velocity and conserve the accuracy of the applied cable equation. This model is then combined with a model for the extracellular space.

4.2.1 The Compartment Structure

The compartment model was developed as described in the work of Rattay [5, 6, 7, 12] for the simulation of electrical neural stimulation. The neuron was divided up into four main compartments that would comprise the dendrite, soma, axon hillock and the axon to approximate the real physical structure of cultured neurons. These compartments were then subdivided into smaller sub units where required.

The axon terminals and the complex branching structure of the dendrites were omitted from the model. The axon and dendrite processes were terminated by an open circuit between the intracellular and extracellular space. This is acceptable as the model does not require the simulation of neurotransmitter sensitivity at the dendrite or secretion at the axon terminals. Each compartment is comprised of one or more nodes from which the

surface area of the membrane is split into two branches, representing the top and the bottom of the membrane. The membrane of the whole neuron was split in this way to allow the simulation of the measurement of extracellular potentials at the processes. The soma was given a spherical volume and the processes were given cylindrical form as illustrated in figure 4.4.

The resulting network provides a Spatially Extended Non-linear Node (SENN) model as first presented by McNeal [15]. Nodal and inter-nodal connections are represented by linear electrical circuit components. The conductance paths of membrane model, g_{Na}, g_K, g_L and the membrane capacitance c_m, presented in section 4.1 are scaled according to the geometry of the compartmental nodes giving:

$$G_{m,c} \frac{(g_{Na} + g_K + g_L) \cdot A_{surf,c}}{2}$$
$$C_{m,c} = \frac{c_m \cdot A_{surf}}{2} \qquad 4.20$$

$G_{m,c}$ and $C_{m,c}$ represent the total values of conductance and capacitance for each membrane compartment. $A_{surf,c} / 2$ is the surface area of the axial **c**ompartment of length Δx split into an upper and lower section. Δx is assumed constant throughout the dendrite, axon hillock and axon. $G_{m,c}$ and $C_{m,c}$ are labelled with the subscript of the component type (**s**oma, **a**xon, **h**illock, **d**endrite) in figure 4.4.

The resistance of the intracellular axoplasm is calculated for the cylindrical nodes as:

$$R_a = \frac{4\rho_i \Delta x}{\pi d_p^{\,2}} \qquad 4.21$$

where ρ_i is the intracellular resistivity taken as 300 Ωcm [2, 4] and d_p is the diameter of the process (axon, hillock or dendrite). The axial resistance R_p takes the form of R_d, R_h and R_a in figure 4.4 where the process subscript **p** is replaced by **d**, **h**, or **a** depending upon the process type (**a**xon, **h**illock or **d**endrite).

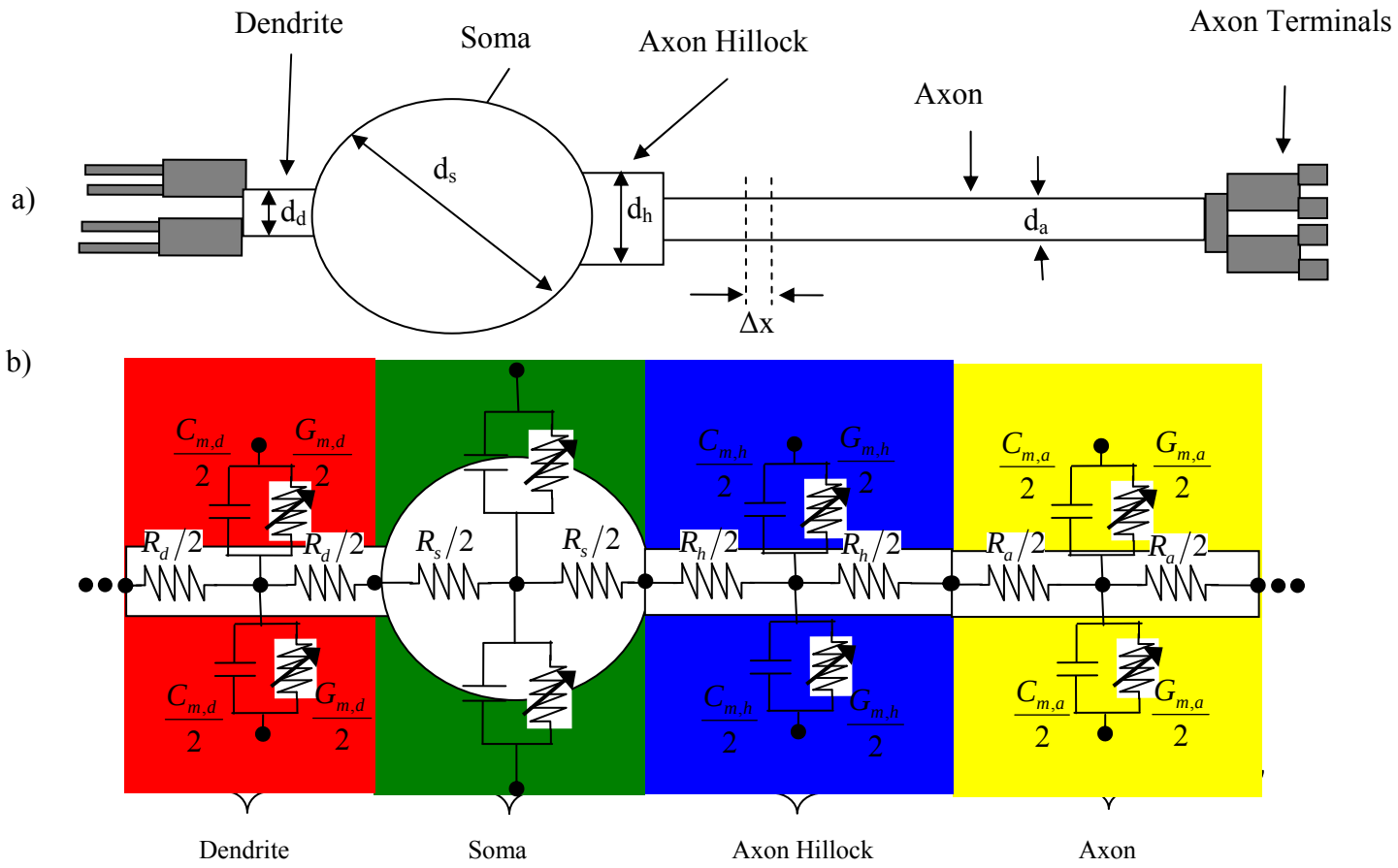

Figure 4.4

Diagram of the neuron model. a) Shows the form of the model including each of the subunits. The grey shaded sections of the diagram indicate the areas that are omitted from the model. b) Shows the equivalent 2-dimensional circuit model including the active membrane. Membrane capacitance, conductance and intracellular axial resistance are subscripted for their respective compartments and channel potentials have been removed for simplicity. The V_e terms represent the extracellular potentials of the membrane. Upper extracellular potentials are over-lined.

As a numerical rule of thumb, Δx should not exceed the value $\lambda/4$ where λ is the so called space constant [5] and is calculated by:

$$\lambda = \sqrt{\frac{d_p}{4\rho_i g_m}} \qquad 4.22$$

The space constant defines the minimum compartmental length that allows V_i and V_e to be represented by a mean value numerically for a given compartment. For $\Delta x < \lambda/4$ an error compared to the continuous cable equation solution is of the order of 1 % [5].

The resistance through the soma is calculated for two connected hemispherical zones that are joined axially to the cylindrical branches of the dendrite and axon hillock. An approximate geometrical model for the equivalent conductance was presented by Rattay [14] that is calculated by considering the equivalent cross sectional area between the somatic node and the diameter of the cylindrical branch as:

$$R_s = \frac{2\rho_i}{\pi r_s} \cdot \ln\left(\frac{(d_s/2) + \sqrt{(d_s/2)^2 - (d_{branch}/2)^2}}{(d_s/2) - \sqrt{(d_s/2)^2 - (d_{branch}/2)^2}} \right) \qquad 4.23$$

The value d_{branch} is the diameter of the branch corresponding to d_h for the left hand side soma intracellular resistance and d_d for the right hand side intracellular resistance with respect to figure 4.3.

The G_m and C_m values are calculated by multiplication of the surface area of the active membrane at each node with membrane capacitance c_m and variable conductance g_m. For the axon and axon hillock this area becomes:

$$A_{surf,a} = A_{axon} = \pi d_a \Delta x \qquad 4.24$$

$$A_{surf,h} = A_{hillock} = \pi d_h \Delta x \qquad 4.25$$

The surface area of the soma is calculated:

$$A_{surf,s} = A_{soma} = \left(\pi d_s^{\,2} - \frac{\pi d_d^{\,2}}{4} - \frac{\pi d_h^{\,2}}{4} \right) \qquad 4.26$$

taking into account the area lost by the connection to the dendrite and hillock.

4.2.2 Electrical Connection to the Extracellular Bulk

For an isolated neuron suspended within a large relative volume of extracellular fluid, the electrical connection between the extracellular membrane nodes and the solution bulk may be modelled by a volume spreading resistance to an infinite ground. Various approximations have been derived in the literature to represent distributed resistances. For this investigation, half sphere, rectangle and node to node geometries have been considered to model the distributed resistances from the soma, axon and dendrites respectively to the bulk solution. These geometries were chosen to give a simple mathematical representation of the electrical connection between the neuron components and the extracellular region by virtue of similar shapes. The connectivity of the spreading resistances that are discussed in the following paragraphs are summarised in figure 4.5.

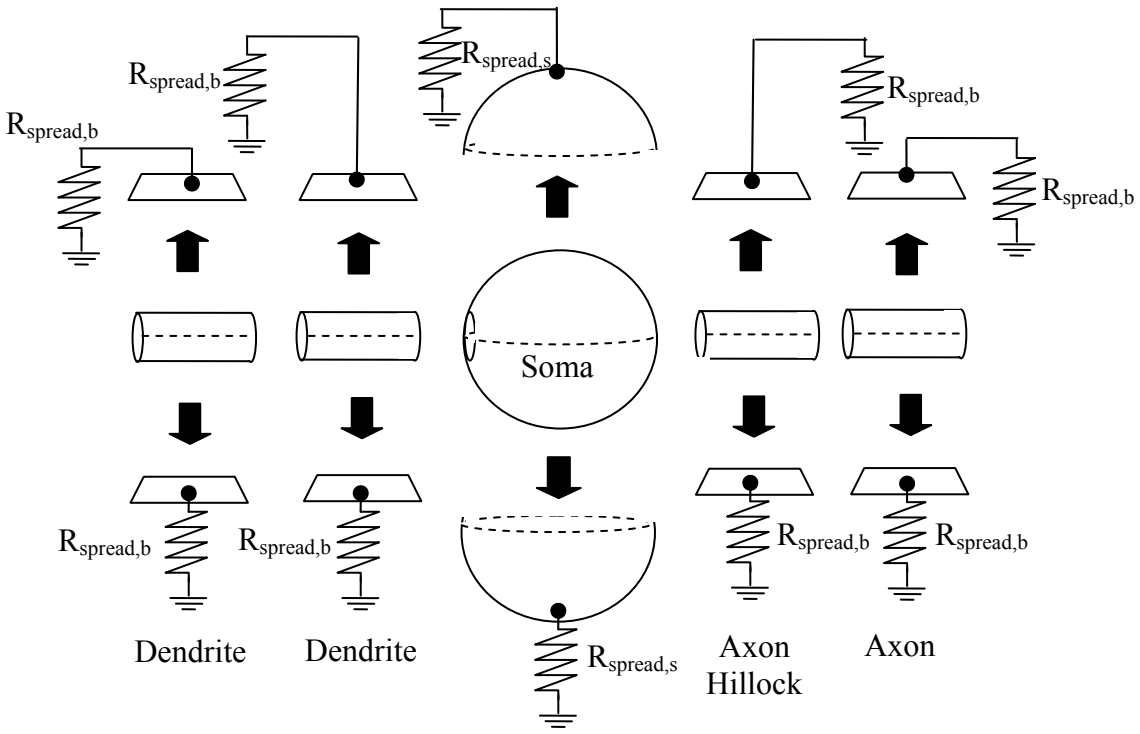

Figure 4.5

Expanded view of the neuron model showing the use of the hemispherical and rectangular spreading resistances to represent the electrical connection between the neuron compartment nodes to the bulk solution.

The spread from each hemisphere of the soma may be described by a spreading resistance according to Newman [17] as:

$$R_{spread,s} = R_{spread,hemisphere} = \frac{\rho_e}{\pi d_{soma}} \qquad 4.27$$

Where ρ_e is the extracellular resistivity.

The surface of the cylindrical process nodes (the dendrite, axon hillock and axon) are modelled by rolling out the half cylinder surface to give an equivalent rectangle of length Δx and width $\pi d/2$. The spreading resistance from a rectangular source on an infinite isotropic half-space may be calculated by [18]:

$$R_{spread,b} = \frac{\rho_e}{\pi\sqrt{A_{surf}/2}}\sqrt{Q}\left(\sinh^{-1}\left(\frac{1}{Q}\right)+\frac{1}{Q}\sinh^{-1}(Q)+\frac{Q}{3}\left[1+\frac{1}{Q^3}-\left(1+\frac{1}{Q^2}\right)^{3/2}\right]\right) \quad 4.28$$

where,

$$Q = \frac{\pi d}{2\Delta x} \quad 4.29$$

For ratios of d:Δx close to 5:1, equation 4.27 may be simplified to:

$$R_{spread,b} = \frac{\rho_e}{\pi\sqrt{A_{surf}/2}} \quad 4.30$$

This condition may be maintained by setting Δx to $1/5^{th}$ of the process node diameter.

4.2.3 Extracellular Nodal Connectivity

The electrical connection between adjacent nodes must also be modelled to complete the electrical circuit. The extracellular nodal connection is not enclosed like that of the intracellular fluid and is thus more difficult to define in terms of the area and length of the current path.

The resistance is simply defined as the mean length and area arising from the approximation of a radially distended current path, as shown in figure 4.6a. This approximation is mapped to a planar geometry by the simple approximation illustrated in figure 4.6b.

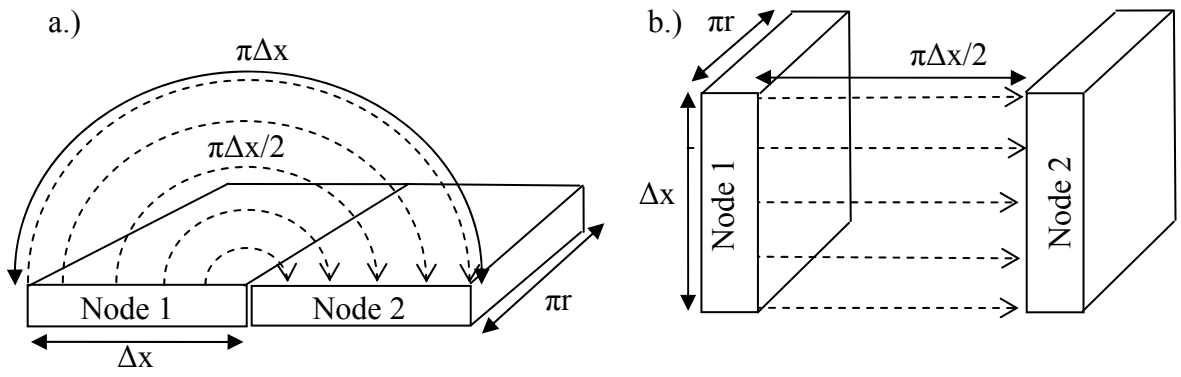

Figure 4.6

Approximation of extracellular nodal current path between two adjacent nodes

This corresponds to an extracellular resistance between process nodes calculated by:

$$R_{ext,p} = \frac{\rho}{2 \cdot r_p} = \frac{\rho}{d_p} \qquad 4.31a$$

A similar method may be used for the circular geometry of the soma to process connection giving:

$$R_{ext,s} = \frac{\rho\left(d_{soma} + \Delta x\right)}{2\left(d_{soma}{}^2 + d_p \Delta x\right)} \qquad 4.31b$$

The placement of the extracellular resistances within the neuron SPICE model are shown in figure 4.7. Nodes A-A', B-B', C-C' and D-D' are left unconnected in the model as during the axial propagation of an action potential the top and bottom of the membrane are symmetrical equipotential surfaces and no current is expected to pass between the nodes.

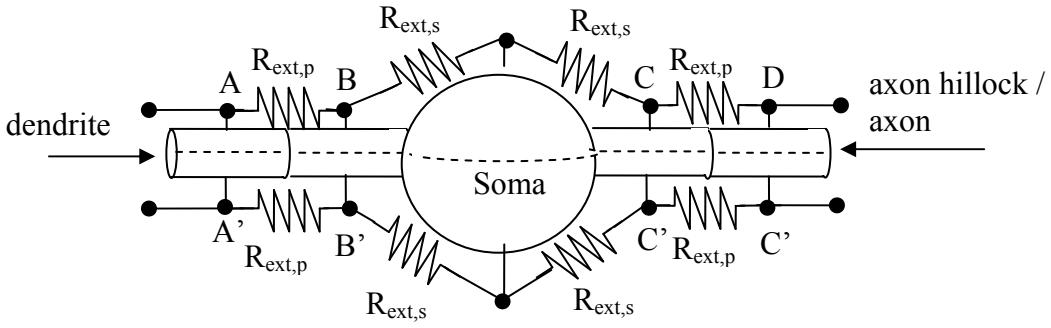

Figure 4.7

The extracellular connectivity between the compartmental nodes

4.2.4 Cell Coupling to the Recording Electrode

The recording and reference electrodes may be defined as described by Regehr et al. [8], as a planar microelectrode mounted in the substrate of an *in vitro* culture dish as part of a larger microelectrode array. In this work, and similar studies by Fromherz et al. [19, 20] and Breckenridge et al. [14], it has been identified that the measurement of the extracellular action potential is facilitated by the partial adhesion of the soma's underside to the substrate forming an ohmic seal. Typical values of the seal resistance R_{seal} have been measured to be 100s kΩ to several MΩ [8, 19].

In vivo, a displaced cell will naturally attach itself to the extracellular matrix and other cells, adapting its shape and forming connections to begin its functional purpose. In an artificial culture environment the extracellular matrix is not present and neurons may be well spaced in the *in vitro* suspension. Nonetheless the neuron will attempt to anchor itself to hospitable surfaces that it encounters. In such cultures gravity will ensure that the contact surface will be the substrate.

As described briefly in Chapter 1, the surface of the soma underside does not adhere uniformly to the substrate; it prefers to adhere around a circumferential contact area. This forms a finite enclosure of extracellular fluid known as the cleft in which the unbound

membrane surface is free to depolarise as normal. The recording electrode will ideally be enclosed within this cleft. This concept is illustrated in figure 4.8. The area of active membrane within the cleft is modelled as a disk of diameter equal to that of d_{soma}. The bottom hemisphere is assumed to have flattened to this geometry with the remaining area of the membrane is assumed to be performing the circumferential adhesion to the insulating substrate and is electrically inactive. Thus the surface area of the active membrane in the cleft is calculated by:

$$A_{cleft} = \pi d_{soma} \qquad 4.32$$

The value of R_{spread} from the underside of the soma will remain that of a hemisphere for simplicity as the exact geometry is unknown. The cleft circuit is shown in figure 4.8; the spreading resistance from both hemispheres may be lumped giving a value of $R_{spread,s}/2$. It is assumed that the recording electrode is positioned beneath the soma within this cleft and that the reference electrode is placed far away from the neuron and is in direct electrical contact with the bulk solution.

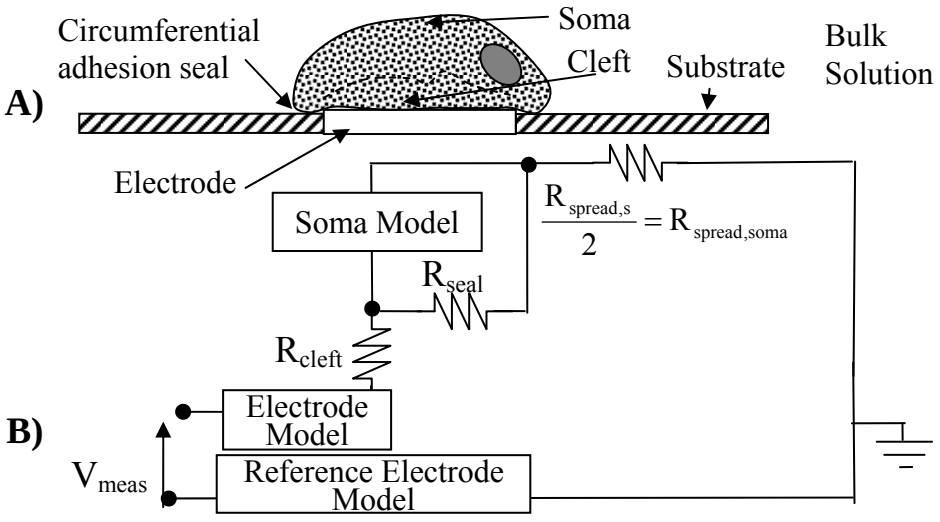

Figure 4.8
A) Schematic of soma - electrode interface
B) Lumped electrical model of extracellular microelectrode recording reproduced from Regehr [8], Fromherz [9] and Rutten [26].

Measurements are made between the recording electrode and the reference electrode. During an action potential it is assumed that local extracellular electrical potential within the cleft resulting from depolarisation is dropped across the electrical resistance maintained by the ohmic seal R_{seal} between soma and substrate. The electrical model shown in Figure 4.8 is often used to describe the degree of coupling between the neuron membrane and the electrode. Other unsealed nodes are electrically connected to the bulk by much lower electrical resistances defined by volume spread and are omitted.

As an example; for a 50 μm diameter soma, the spreading resistance from the surface of one component hemisphere to the bulk may be calculated by equation 4.27 (using ρ_e = 70 Ωcm [2,4]) giving 4.5 kΩ. Regehr et al. [8] and Fromherz et al. [20] have reported seal resistances several orders of magnitude greater than this (100 kΩ - 4 MΩ), allowing signal magnitudes ranging between 10 μV – 10 mV to be measured. Similar signal magnitudes from *in vitro* microelectrode recordings of others, such as Thomas [21] and Breckenridge [14] substantiate the presence of this seal.

In the presented model the seal resistance is defined as a single resistance. The resistance is series connected from the cleft to the spreading resistance to the bulk solution; the spreading resistance may be calculated by equation 4.27. The spreading resistance presents a substantial resistance between the soma, processes and the bulk solution.

The resistance of the cleft volume between the enclosed membrane surface and the electrode surface may also be estimated with a simple cylindrical geometry; using the cleft diameter and height to calculate the cleft resistance. A cleft height, l_{cleft} of 37 nm is used to coincide with the maximum values of cleft depth reported in a recent transmission electron microscopy study [22]. The value of d_{cleft} is assumed to be equal to the diameter of the soma (d_{soma}) in the model giving:

$$R_{cleft} = \rho_e \frac{\rho_e l_{cleft}}{\pi\left(\frac{d_{cleft}}{2}\right)^2} \qquad 4.33$$

R_{cleft} is several orders of magnitude lower than R_{spread} and R_{seal}.

4.2.4.1 Neural Signal Measurements in the Absence of R_{seal}

This section presents a model to calculate the potential between a recording electrode placed close to the soma and a reference electrode placed in the bulk solution. This enables an estimate to be made of the spreading resistance between the microelectrode and the bulk that will facilitate the recording of extracellular soma potentials in the absence of R_{seal}.

Variations in the seal resistance are modelled by directly changing the value of the seal resistor in the circuit. The model suggests that at seal values approaching 1 GΩ the electrode coupling simulates that of a Patch Clamp, from which the true magnitude and shape of the trans-membrane action potential may be measured. Referring to figure 4.8, as R_{seal} tends to zero, the spreading resistance will still provide a finite resistance to ground.

Thus, at the opposite extreme of minimal adhesion with zero seal resistance the electrode coupling may be modelled as a volume conduction problem that may be solved by using the method of images. In this case the electrode is assumed to be external to the soma but in close proximity.

The potential difference between the recording electrode and the reference electrode of the measurement circuit may be predicted by modelling the soma as a point current source from its centre. Referring to figure 4.9; the point current source I_p is positioned a distance r_a away from the centre point, O_e of a spherical electrode of radius r_e where $r_a > r_e$.

The extracellular space is modelled as an infinite volume of resistivity ρ_e and the recording electrode is modelled as a perfect conductor. The resistivity of the material in the extracellular volume is therefore much larger than that of the electrode. The reference electrode is placed far away from the recording electrode in the bulk of the conducting extracellular space, ie. $V_{ref} = 0$ V.

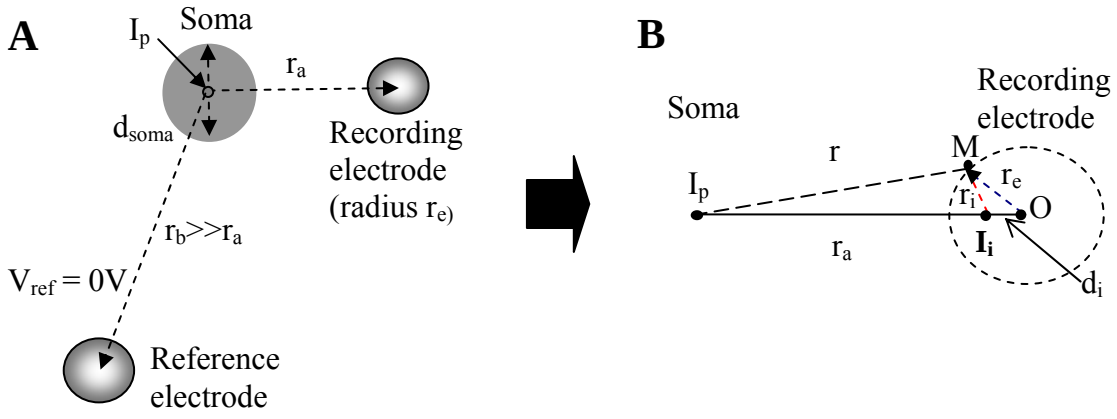

Figure 4.9

Illustration of A. The physical model of the soma and the electrodes with the soma membrane current modelled as a point source, and B. the method of images model showing I_p with its image source I_i placed within the volume of the spherical recording electrode.

Using the method of images, a negative image current source I_i will be situated inside the sphere representing the geometry of the electrode on the line separating I_i and O_e.

The value of I_i may be calculated by considering the potential V_M at point M. If the surface of the recording electrode is grounded (set to 0 V) the calculation for V_M is:

$$V_M = \frac{\rho}{4\pi}\left(\frac{I_p}{r} + \frac{I_i}{r_i}\right) = 0 \qquad 4.34$$

Since it is an equipotential surface.

$$\frac{r_i}{r} = -\frac{I_i}{I_p} = \text{constant} \qquad 4.35a$$

By virtue of similar triangles:

$$\frac{r_e}{r_a} = \frac{r_i}{r} = -\frac{I_i}{I_p} \qquad 4.35b$$

Thus:

$$I_i = -\frac{r_e}{r_a} I_p \qquad 4.35c$$

Now for the case of an electrically neutral spherical electrode (i.e. an ideal probe with infinite impedance to ground), the point current source I_i would still be required at distance d_i from the centre to make the surface equipotential. An additional image source is also required at the centre of the electrode (point O_e) to make the net current zero [27]:

$$I' = -I_i = \frac{r_e}{r_a} I_p \qquad 4.36$$

The potential V_M at the electrode surface is now non zero and is calculated by:

$$V_M = \frac{\rho}{4\pi}\left(\frac{I_p}{r} + \frac{I_i}{r_i} + \frac{I'}{r_e}\right) = \frac{\rho}{4\pi}\left(\frac{I_p}{r} + \frac{I_i}{r_i} + \frac{r_e I_p}{r_a r_e}\right) \qquad 4.37$$

As $\frac{I_p}{r} + \frac{I_i}{r_i} = 0$, equation 4.37 may be written as:

$$V_M = \frac{\rho}{4\pi}\frac{I_p}{r_a} \qquad 4.38$$

This is the potential measured by the recording electrode when its centre is positioned a distance r_a from the centre of the soma. The potential is dependent solely upon r_a as long as $r_a > d_{soma}/2 + r_e$, i.e. the electrode surface is external to the soma. The potential at the electrode surface may be calculated with accuracy as long as r_a is measured between the centre of the soma and the centre of the recording electrode.

Equation 4.38 may be rearranged to calculate the spreading resistance between the recording electrode and ground. With reference to figure 4.8, equation 4.38 may be used to verify the potential between the recording electrode and the reference electrode with their centres at a distance r_a and r_b respectively from the centre of the soma:

$$V_{meas} = V_{rec} - V_{ref} = \frac{\rho}{4\pi}\frac{I_p}{r_a} - \frac{\rho}{4\pi}\frac{I_p}{r_b} \qquad 4.39$$

r_b is far enough away to be assumed infinity, reducing the right hand side term of 4.39 representing V_{ref} to 0 V.

The resistance between the recording and reference electrode at the ground point may be calculated by:

$$R_{a-b} = \frac{V_{meas}}{I_p} = \frac{\rho}{4\pi \cdot r_a} \qquad 4.40a$$

As the surface of the recording electrode is brought close to the soma surface at radius $d_{soma}/2$ from I_p and $r_e << d_{soma}$ equation 4.39 will tend towards:

$$R_{a-b} = \frac{\rho}{4\pi \cdot \left(\frac{d_{soma}}{2}\right)} = \frac{\rho}{2\pi \cdot d_{soma}} = R_{spread,soma} \qquad 4.40b$$

This is the spreading resistance of a sphere and is used in the SPICE model to estimate the spreading resistance between the soma and the bulk solution. $R_{spread,soma}$ is in series with R_{seal} in the circuit path between the cleft and the bulk electrolyte solution as shown in figure 4.8.

4.3 The Electrode Model

The interface between the electrode and the saline electrolyte comprising the extracellular fluid is a complex affair requiring the interaction between charge across the solid and liquid phase. Real resistive current may occur by decomposition of the electrode, mass transport of metal ions, oxidation and reduction of the solvent, solvated ions or dissolved gasses. A large complex capacitive current occurs due to an interfacial dipolar water layer, adsorption of ions and ionic migration in the area approaching the interface.

Electrode materials considered suitable for electrophysiological recordings must be non reactive within the physiological saline solution. The noble metals gold and platinum are often used due to their stability in this aggressively corrosive situation. For the measurement of small AC perturbations (defined as $< kT/q$) these electrodes approach the definition of an ideally polarisable electrode [24]; i.e. wholly capacitive. Some small dc charge transfer will still occur due to electrode reactions involving dissolved species such as H^+, OH^- and Cl^-.

In simple small signal measurement situations the electrode may be represented by a parallel resistance and capacitance circuit as shown in figure 4.10. Typical small signal values about equilibrium for the unit area electrode capacitance, c_e and surface resistivity, r_e are of the order of 10 μFcm^{-2} [24] and 10 $M\Omega cm^2$ [25] respectively. Frequency dependent effects are avoided for simplicity but may be shown to have limited influence upon the signal within the frequencies of interest provided $C_e \geq C_m$, where C_e is the total capacitance of the electrode and C_m is the total capacitance of the neuron membrane within the cleft and the input impedance of the measurement circuit is sufficiently large.

The electrode half cell potential E^0, often a problematic cause of offset, is included in the model as a voltage source in series with r_e. As in real measurement systems the half cell potential is current limited by the interface resistance which restricts its influence upon the measurement circuit unless R_{meas} (see figure 4.11) is much greater than R_e, where R_e is the total resistance of the electrode for a given surface area $Area_e$ ($Re = r_e / Area_e$).

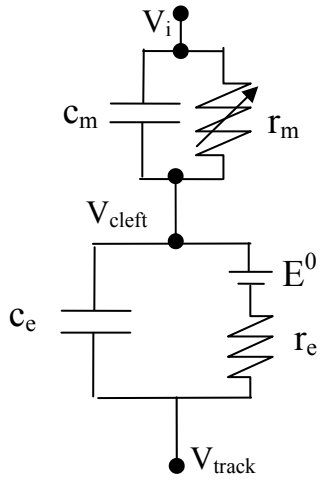

Figure 4.10

The electrode model showing the unit area capacitances, c_e, and the surface resistivity r_e. The position of the circuit in the model is indicated by the nodes labelled V_{cleft} and V_{track}; V_{cleft} being the voltage in the cleft (Section 4.2.4) and V_{track} being the voltage leading into the measurement circuit (Section 4.4).

4.4 The Input Front End

The input front end simulates the input properties of the solid state amplifier measurement circuitry. This is often modelled as a parallel resistor-capacitor circuit connected to ground representing the degree of loading the input device places upon the signal source. For small signal measurements an input offset current is also placed in parallel with these elements. The circuit for this model is presented in Figure 4.11.

There is much variation between different technology families. Bipolar transistor technologies have input impedance in the order of $0.3\times10^6\Omega$ - $2\times10^6\Omega$ and input bias current of 0.5μA (example source National Semiconductor LM741), whereas FET type

devices have impedances of $10^{13}\ \Omega$ with 1 pF input loading capacitance and gate leakage bias currents of several pA (source example Texas instruments OPA121) .

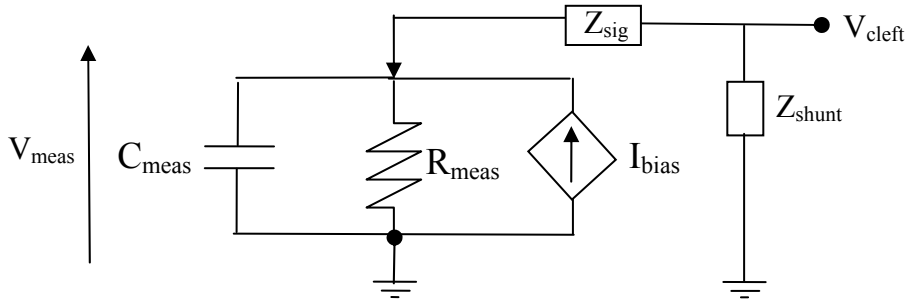

Figure 4.11

Input load model for measurement circuit. Z_{sig} is the lumped impedance of the series elements of the signal path, Z_{shunt} is the lumped shunt impedance of the parasitics shown in figure 4.10, V_{cleft} is the cleft potential.

For FET input amplifiers without feedback on the input path the input may be assumed to be an open circuit. For lower impedance devices such as BJTs care must be taken to ensure that the input circuit does not influence the shape and magnitude of the received signal.

4.4.1 Electrode Interconnection Parasitics

Parasitic resistance and capacitance may also be introduced into the model at this stage. As discussed in chapter 3, electrode interconnection parasitics result from the capacitive and resistive properties between adjacent conductive tracks that carry the electrical signal from the electrode to the measurement circuitry. Additional parasitics occur between track and substrate and track and electrolyte across the insulation layer. If the lumped parasitic capacitance is large and the lumped parasitic resistance small with respect to the signal source impedance the recorded signal may be attenuated or distorted. If this effect is large the signal may be indistinguishable from background noise and electrical interference.

Track to substrate and track to electrolyte parasitics may be modelled as a lumped parallel resistor-capacitor to ground. Track to track parasitics may also be incorporated in this lumped description for single channel analysis or described as a separate parallel resistor-capacitor pair between adjacent tracks to model channel cross-talk effects. The values of these components may be calculated as described in equations 3.1 – 3.3. Values will vary by many orders of magnitude depending upon the intrinsic properties of the materials used. Properties such as material geometry, fabrication methods and process contamination levels may also have a marked effect. The lumped circuit model used in the simulation is presented in figure 4.12 a.

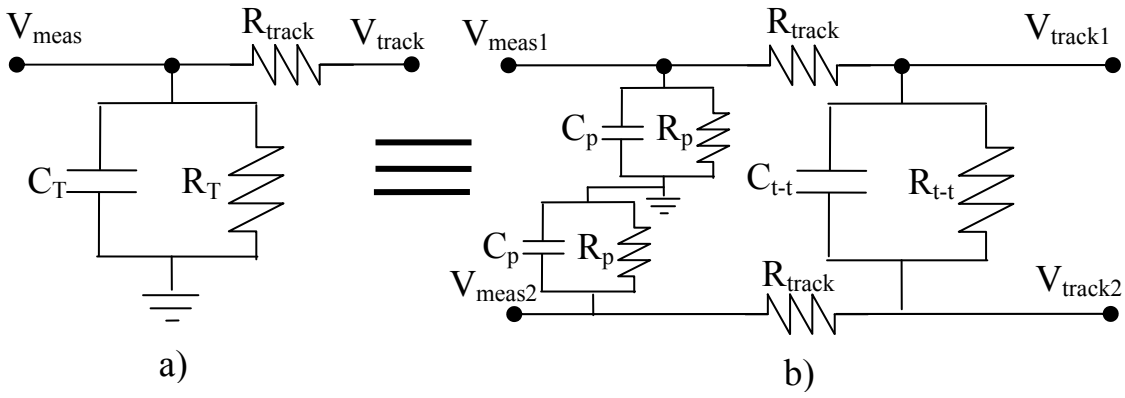

Figure 4.12

Track parasitics: a) lumped model for single track, b) break down of contributing paths. R_{track} is the track resistance and C_T and R_T the total lumped capacitance and resistance.$C_{t\text{-}t}$ and $R_{t\text{-}t}$ are the track to track capacitance and resistance and C_p and R_p are the lumped substrate and bulk parasitic capacitance and resistance paths to ground.

In an array, the lowest value of R_T will be for the inner electrodes and tracks, i.e. those that have tracks placed adjacently at either side. From figure 4.12 this may be calculated as:

$$R_T = \frac{R_p\left(R_{t-t} + R_p\right)}{2\left(R_{t-t} + 2R_p\right)} \qquad 4.41$$

For end electrode tracks, i.e. those with only one adjacent track this becomes:

$$R_T = \frac{R_p\left(R_{t-t} + R_p\right)}{\left(R_{t-t} + 2R_p\right)} \qquad 4.42$$

The lumped capacitance C_T may be calculated for the inner tracks as:

$$C_T = 2\left(C_p + \frac{C_{t-t}C_p}{C_{t-t} + C_p}\right) \qquad 4.43$$

and for the end electrode tracks:

$$C_T = \left(C_p + \frac{C_{t-t}C_p}{C_{t-t} + C_p}\right) \qquad 4.44$$

Rtrack is neglected as the value is small in comparison to R_p and $R_{t\text{-}t}$

4.5 Developing the Model for SPICE

The model was developed for SPICE as it is the industrial and institutional standard for circuit simulation. SPICE provides a simple solution to the numerical calculation of multi-node circuit problems.

4.5.1 Modelling the Ionic Conductance in SPICE

As the ionic conductance equations are non-linear and vary differentially with respect to time they are a little more difficult to simulate in SPICE as standard circuit components. For this reason the hardware description language VerilogA was used to define i_{Na}, i_K and i_L. The script for each cell is given in Appendix A. The full Cadence Library and Cell views for the simulation will be available online on the Durham University, Centre for Electronic Systems website following the publication of the model. The surface area parameters were included as 'Parameter' variables within the code to allow easy modification in the Virtuoso simulation environment. A time-step of 100 ns was defined to maintain numerical accuracy.

4.5.2 The SPICE Circuit Layout

The SPICE model was developed in Cadence Vertuoso using standard *AnalogLib* library passive components. The modelled neuron consists of 45 intracellular nodes; 1 soma node, 25 dendrite nodes, 17 axon nodes and 2 hillock nodes. The model terminates at open circuit ends at the tip of the extreme dendrite and axon nodes. Each compartment is created as a discrete module built up from discrete cells describing the circuit elements. Each compartment may have parameters set independently to one another.

Action potentials are initiated by a transient current pulse at the dendrite tip and propagate left to right, with reference to the diagram in figure 4.13, from the dendrite through the soma and continue on through the hillock and the axon to the final node at the axon tip. The extended length of the dendrite and axon compartments reduces the boundary effects upon the propagating signal before it reaches the soma where the signals of interest will be measured. This extended model ensures both the removal of boundary effects and stimulus artefacts, allowing a signal shape resembling spontaneous action potentials to be produced.

The modular nature of the compartment cells and the inclusion of scale variables allow more complex neuron models to be built with easily defined physical properties. Additional membrane models may also be included in the VerilogA script to describe specific membrane properties.

The circuit layout is given in Figure 4.13 and includes all of the modelling considerations described in this chapter. A summary list of significant design parameters is also presented in Table 4.1.

Parameter			
	Symbol	Value	Unit
Membrane capacitance per unit area	c_m	1	$\mu F /cm^2$
Resistivity of intracellular fluid	ρ_i	0.3	kΩ cm
Resistivity of extracellular fluid	ρ_e	0.07	kΩ cm
Absolute temperature	T	293.15	K
Sodium potential	E_{Na}	115	mV
Potassium potential	E_K	-12	mV
Leakage potential	E_L	10.6	mV
Sodium channel conductance per unit area	g_{Na}	120	mS /cm^2
Potassium channel conductance	g_K	36	mS /cm^2
Leakage conductance per unit area	g_L	0.3	mS /cm^2
Soma diameter	d_s	20-100	µm
Dendrite diameter	d_d	1-5	µm
Axon hillock diameter	d_h	5-20	µm
Axon diameter	d_a	1-5	µm
Nodal length	Δx	0.2 -1	µm
Cleft seal resistance	R_{seal}	0-10	MΩ
Electrode capacitance per unit area	c_e	10	$\mu F /cm^2$
Electrode resistance area product	r_e	10	$M\Omega cm^2$
Electrode half cell potential	E_e	± 0 - 1	V
FET input capacitance [OPA121]	C_{meas}	1	pF
FET input resistance	R_{meas}	10^4	GΩ
FET input bias current	I_{bias}	3	pA
Total shunt parasitic resistance	R_T	0.01 - 1000	GΩ/cm
Track resistance	R_t	11.6	Ω/cm
Total shunt parasitic capacitance	C_T	35	pF/cm

Table 4.1

Significant design parameters in SPICE model

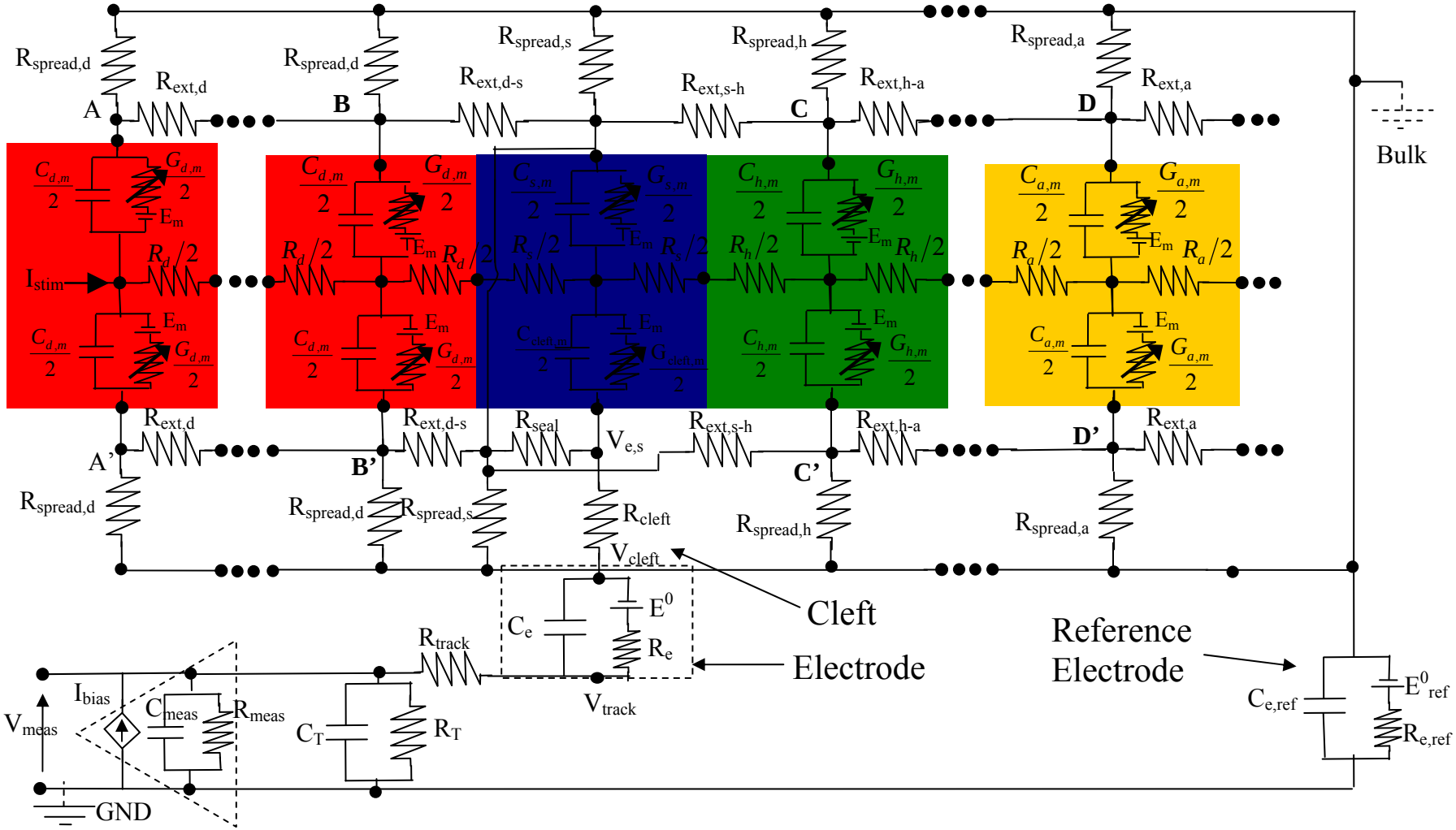

Figure 4.13

The complete circuit model used in SPICE simulation. Conductances and potentials are grouped for simplicity. Compartments are coloured following from figure 4.4

The model allows the action potential duration to be modified relative to the K value parameter presented in equation 4.13. The value of K may be selected to fit the peak to peak time of the cleft action potential.

4.6 Conclusion

This chapter presents a novel computer simulation based upon mathematical models of the physiology, geometry and electrical properties of the *in vitro* electrophysiological recording system for planar microelectrodes. The model is used in chapter 5 to define key signal properties of the extracellularly measured action potential for amplifier design and sampling considerations. By modelling the neural recording system in this way, signals may be simulated over a range of controllable variables that would be very difficult to define and monitor in the lab by *in vitro* study.

The model was developed in a well trusted numerical simulation method: SPICE. This facilitates portability and ensures accuracy of the electrical predictions. The modular architecture of the SPICE model provides a simple method for interchanging membrane models for future expansion.

4.7 References

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Chapter 5
Analysis of the Model Neuron

This chapter develops the model proposed in chapter 4 to predict the shape and amplitude of extracellular signals. This method was developed to overcome difficulties in accessing neural cultures to study variation in recorded electrical signals from planar microelectrode arrays. The motivation for this work was to observe the relationship between the cell to electrode seal, cell diameter and the signal amplitude and frequency spectrum. It is of great importance to understand the range of the signal properties when designing optimised neural signal recording circuitry.

The model is tested to ensure that it successfully recreates the transmembrane action potential (TMAP) following the results presented by Hodgkin and Huxley [4]. The extracellular signal is also analysed within the cleft to identify the critical point at which the cleft action potential (CAP) differentiates in shape and amplitude from the TMAP. The cleft model is analysed for expected thermal noise contributions that will define the lower level for signal detection within the cleft for an ideal probe situation.

To validate the simulated waveforms the model is calibrated to intracellular and extracellular signals published in peer reviewed journals by Regehr [1, 2] and Fromherz [3].

After demonstrating the close similarities between the simulation and published data the model is then used to predict the variation in extracellular signal at the cleft as the seal and soma diameter vary for an ideal probe situation. Signal amplitude, signal frequency spectrum are presented over the selected range of soma diameters (20 μm -100 μm) and

seal resistances (10 kΩ - 10 MΩ). The rms noise of the cleft circuit is analysed both analytically and in SPICE and the signal to noise ratio of the extracellular CAP is estimated over the range of applicable values.

The effects of measurement electrode parasitics and input amplifier impedance are simulated to define the critical point at which the extracellular signal will be affected. This is found to be dependent upon the seal resistance R_{seal} and the total membrane capacitance C_m enclosed within the cleft. A general design rule for MEA devices is proposed based upon these findings.

The chapter concludes by discussing the application of the simulation results to the front end design of the measurement circuit and signal sampling for digitisation. A suitable gain and bandwidth are selected for the design together with a suitable input circuit configuration.

5.1 Validation of the Model

This section demonstrates the validity of the model by verifying that it responds similarly to other published models and behaves electrically as a neuron.
This is achieved in the first instance by demonstrating that the form of the TMAP is as expected and that the TMAP propagates in the expected fashion between the axial nodes of the model.

The relationship between the CAP and TMAP signal shape is analysed for seal resistances ranging from infinity to zero to determine the critical point where the CAP begins to distort towards the typical extracellular signal shape. Thermal noise contributions are also estimated for the CAP signal path within the cleft from the ohmic resistance of the extracellular cleft volume.

5.1.1 Comparison to Hodgkin Huxley Signal Shape

A neuron was simulated in SPICE using the model presented in Chapter 4. The TMAP was directly compared to the published plots from the source journal introducing the

Hodgkin Huxley membrane model [4]. Hodgkin and Huxley's plotted results for simulations at 6.3 °C and 18.5 °C were optically scanned from the print copies and processed in Matlab to threshold and convert the 2D image array into an appropriately scaled x,y graphical plot.

The scanned plots are directly compared with the simulated results from the SPICE model in figure 5.1 below. The similarity between the plots verifies that the SPICE model is effective in simulating the electrical properties of the non-linear ion channels as defined by Hodgkin and Huxley.

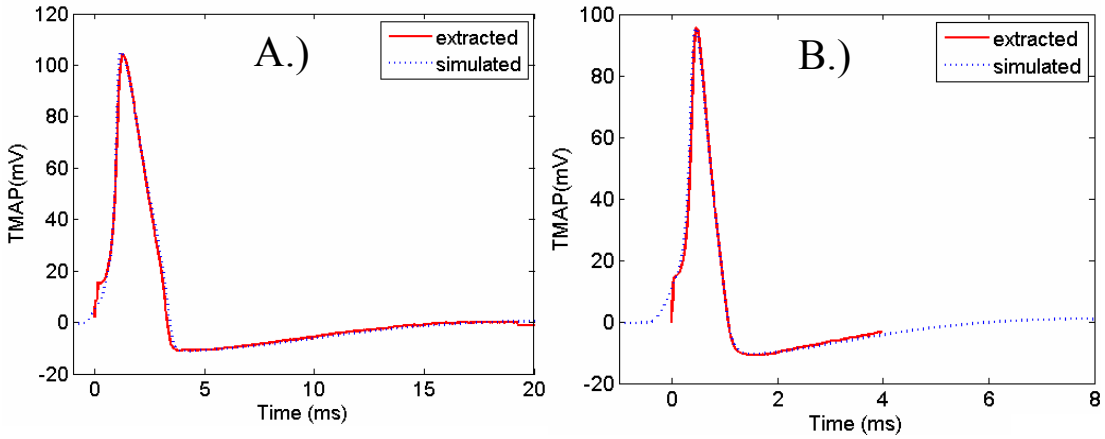

Figure 5.1

Comparison of SPICE membrane simulation with original numerical simulation of Hodgkin and Huxley for: A.) 6.3°C and B.) 18.5°C Presented as figures 13 & 14 in [4].

5.1.2 Verification of TMAP Propagation through the Model

Action potentials propagate down the neuron from the dendrites to the axon terminals. This is the fundamental electrical signal transmission pathway in life. This SPICE model uses the spatially extended non-linear node model (SENN) circuit method to extend the single node membrane model of Hodgkin and Huxley to simulate the propagation of the action potential.

The model proposed in chapter 4 was stimulated with a small cathodic current pulse at the dendritic tip. The propagation of the TMAP signal was measured by probing each intracellular node in the model. The progress of the TMAP is plotted with respect to time in a surface plot in figure 5.2 for selected nodes. The plot displays TMAP vs. time

vs. node. The presented results are for a model with 70 μm diameter soma and K at 2.3. All other model variables are as stated in figure 4.1.

It is challenging to measure the TMAP of real neurons in this way due to the dimensions of the neuron and its processes. The measurement would require the positioning of many closely spaced transmembrane electrodes down the length of a neuron. In the absence of such data, the depolarisation map is presented adjacent to results from a similar SENN model presented by Rattay [5]. In Rattay's simulation model, a current stimulus was presented at the node labelled N2 in figure 5.2, causing TMAP signals to propagate axially from this point. The results of the model presented in this thesis show a similar depolarisation pattern to that presented by Rattay, including the delay in the propagating signal occurring before the soma. The TMAP width in time is much shorter in Rattay's simulation as he used the Hodgkin Huxley model with a K value of 12 to mimic mammalian neurons. Figure 5.2 demonstrates the ability of the model to simulate the propagation of the TMAP from the dendrite to the axon terminal and shows a similar response to other peer reviewed work.

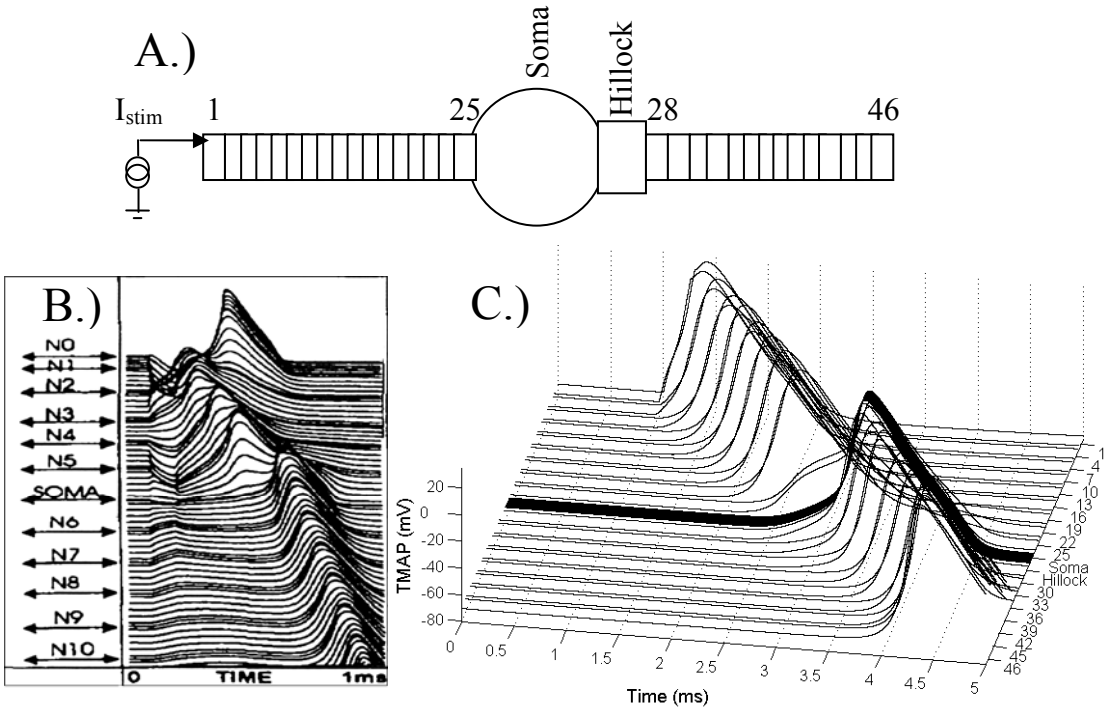

Figure 5.2

Comparison of TMAP propagation through the neuron model shown in A.): B.) is taken from Rattay [5], C.) shows simulation results from the model described in chapter 4.

5.1.3 Relationship between CAP and TMAP

The CAP is observed from infinite seal resistance R_{seal}, between the cleft volume and the bulk solution, to zero seal resistance. This was performed to determine the relationship between the CAP and the TMAP for different values of the seal resistance. It is well known that a large value of R_{seal} can facilitate the direct measurement of the TMAP in a technique known as whole cell patch clamping. The shape of the signal is explored from this point to the critical point where the CAP gains its typical bipolar signal shape.

The critical seal resistance for the CAP is defined as the point where the CAP ceases to closely follow the form of the TMAP; this value may be calculated for the Hodgkin and Huxley model with respect to specified range of soma diameters.

Section 5.1.3.1 determines the critical point for situations where the ionic current contributes to the signal, as in the case of negative leading spike (NLS) signals defined in section 5.2. Section 5.1.3.2 discusses the critical point for positive leading spike (PLS) signals also discussed in section 5.2.

5.1.3.1 The Critical Point for Negative Leading Spike (NLS) CAP Signals

In the NLS CAP signal the ionic transmembrane current is identified as the dominant factor in the signal shape. To produce this signal shape the voltage gated ion channels must open in the section of membrane within the cleft. The voltage gated ion channels will only open as the intracellular potential V_{int} (resting at -70mV relative to V_{ext}) is raised to approach a threshold level relative to the extracellular potential V_{ext} (assumed 0V). For the *in vivo* neuron, the extracellular matrix provides an electrical connection with finite resistance between the cell membrane and the bulk extracellular fluid. This situation is also observed *in vitro* cultures and allows the neuron to depolarise in a similar way to *in vivo*. The electrical model of the cell in vitro is shown in figure 5.3 and includes the cleft as defined in section 4.2.4.

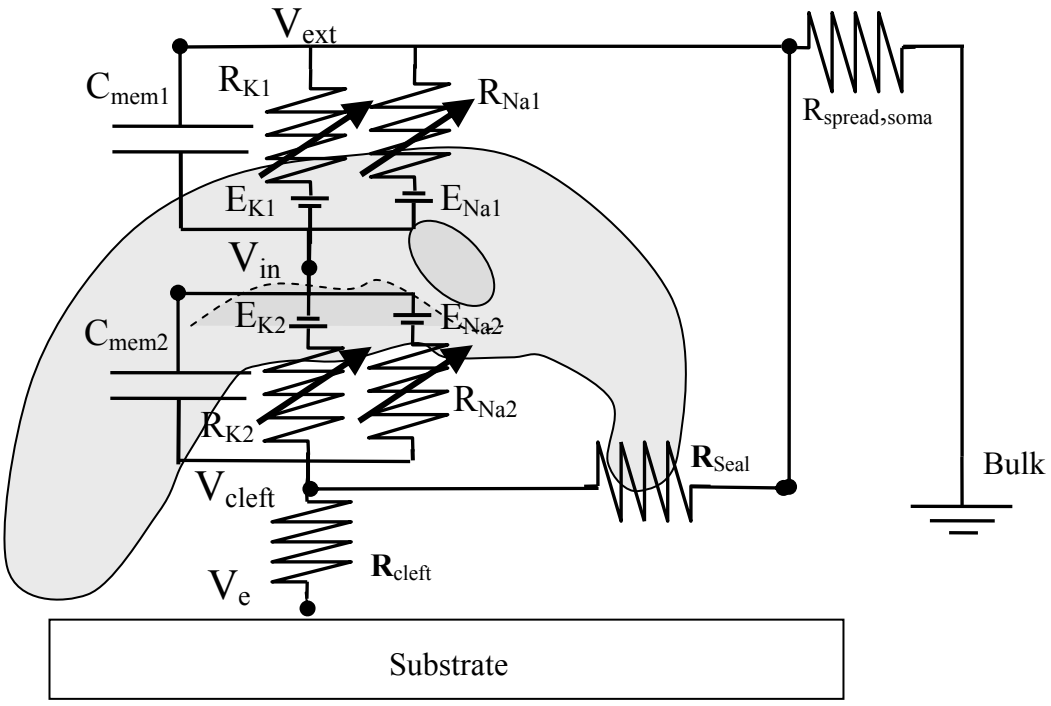

Figure 5.3

The neuron-cleft circuit

For the ion channels to open the membrane potential $V_{in} - V_{ext}$ and $V_{in} - V_{cleft}$ must depolarise from the resting potential of approximately -70mV. When the cleft to bulk seal resistance R_{seal} is small V_{cleft} is held at a stable potential close to that of the bulk. The node V_e is connected to a measurement circuit of infinite impedance. V_e does not draw current and thus will not influence the value of V_{cleft}. The membrane capacitance on the cleft side of the circuit will quickly discharge and a potential difference will occur across the membrane capacitor. The voltage gated ion channels will open and the membrane will depolarise producing an action potential. Such is the situation for neurons *in vivo* and *in vitro*; the cleft seal resistance of a neuron-microelectrode connection will always be below the critical resistance that will prevent voltage gated ion channels from opening, otherwise the TMAP would not propagate.

If the value of R_{seal} is infinite, the extracellular potential within the cleft is electrically isolated from the bulk. The extracellular plate of the membrane capacitor will follow the intracellular potential and the voltage gated channels in the membrane presented at the cleft will not see a change in the potential across the membrane.

Using the SPICE neuron model, the activation of the ion channels can be directly observed by monitoring the sodium channel activation parameter m. For depolarisation to occur in the model, m must approach unity allowing the channel conductance g_{Na} to realise its maximum value as defined by equation 4.10.

The activation of the ion channels in this way is illustrated in the following paragraphs from the results of a simulation using the Hodgkin Huxley membrane model at 6.3°C with a 70µm diameter soma.

If one considers the lower half of the circuit presented in figure 5.3 with the plots presented in figure 5.4, the sodium channels, represented by R_{Na2} will only open if there is sufficient conductance between the cleft and the extracellular bulk. The membrane will only depolarise for seal resistances of approximately 103 MΩ and below. For resistances approaching this value there is significant delay in the response of the channels. This principle is similar to that often observed in strength-duration curves of stimulating currents.

At values of R_{seal} close to the critical point, the delayed depolarisation is observed in the cleft as an abnormal inverted contribution to the CAP. This occurs due to the delayed sodium current falling behind the capacitive current during the propagation of the TMAP. The signal shape is illustrated in figure 5.5.

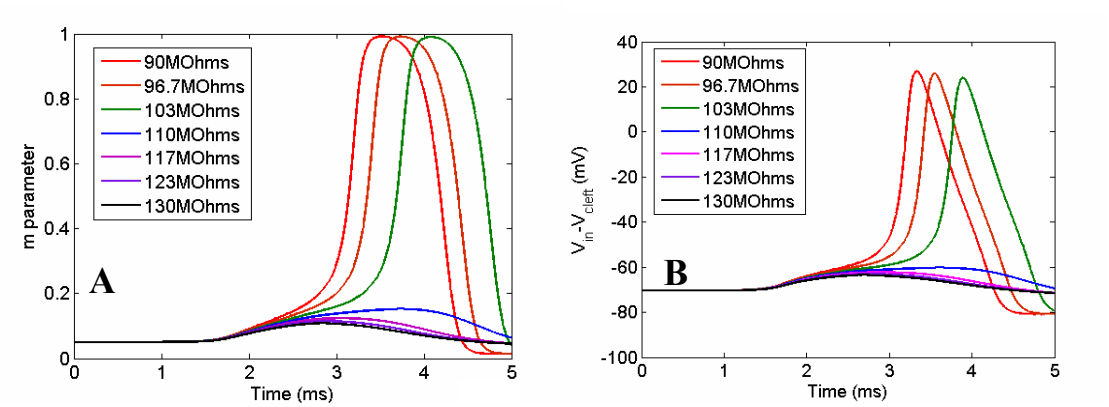

Figure 5.4

A.) Activation of the m parameter and B.) the TMAP produced for a range of R_{seal} values around the critical point for the Hodgkin Huxley model at 6.3°C

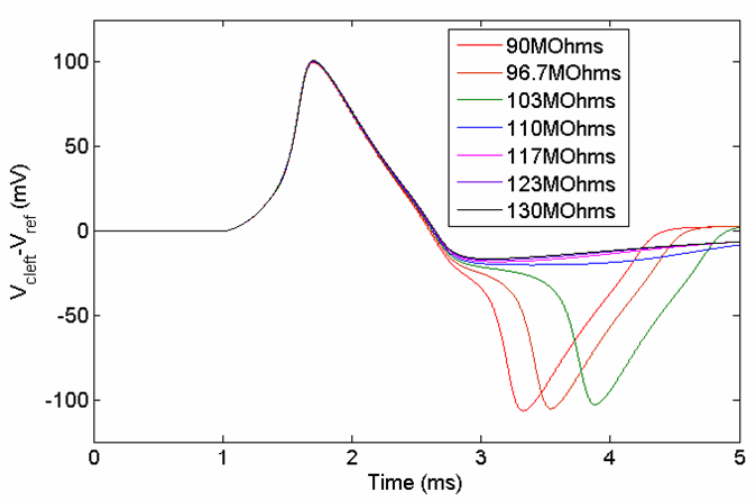

Figure 5.5

Anomalous CAP signal due to the value of R_{seal} being close to the critical point

The critical point is dependent upon membrane capacitance, membrane area and kinetics of the ion channels. The critical seal resistance may be predicted for a given membrane capacitance occurring within the cleft. For the ion channels to open the potential drop across the capacitor V_{Cmem} must exceed a critical level over a given period of time. From figure 5.4 B.), the lowest critical potential was observed to be 10mV over the 1.3ms duration of the action potential. This is illustrated in figure 5.6.

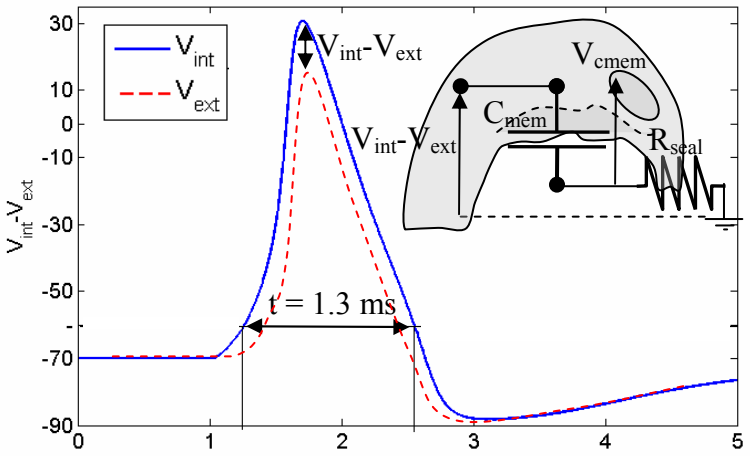

Figure 5.6.

Simulated intracellular potential V_{int} at soma due to propagating TMAP. The required amplitude of V_{ext} is plotted and the duration of the TMAP is noted for the critical point for the ion channels to open. The equivalent electrical circuit during this process is inset top right.

The critical value of R_{seal} may be estimated by considering the depolarisation of the intracellular space as a step change in the potential across the membrane. For the reduced circuit presented in the inset to figure 5.6, the step voltage response may be calculated by:

$$V_{Cmem} = V_i \cdot \left[1 - \exp\left(\frac{-t}{R_{seal} \cdot C_{mem}} \right) \right] \qquad 5.1$$

where t is the duration of the step voltage across the membrane in the cleft during the action potential.

This may be rearranged in terms of R_{seal}:

$$R_{seal} = \frac{-t}{\ln\left(\frac{V_{int} - V_{Cmem}}{V_{int}} \right) \cdot C_{mem}} \qquad 5.2$$

This may be further developed to predict the seal required for a given cleft surface area. Assuming the area of the membrane within the cleft is proportional to the diameter of the soma and that a circular area is enclosed, the area may be approximated by $\pi d_{soma}^2/4$ for the soma underside giving:

$$R_{seal} = \frac{-t}{\ln\left(\frac{V_{int} - V_{Cmem}}{V_{int}} \right) \cdot c_{mem} \cdot \pi \cdot \frac{d_{soma}^{\ 2}}{4}} \qquad 5.3$$

Figure 5.7 shows plotted curves of the critical value of R_{seal} for a range of soma diameters given action potential durations between 0.5 ms and 30 ms.

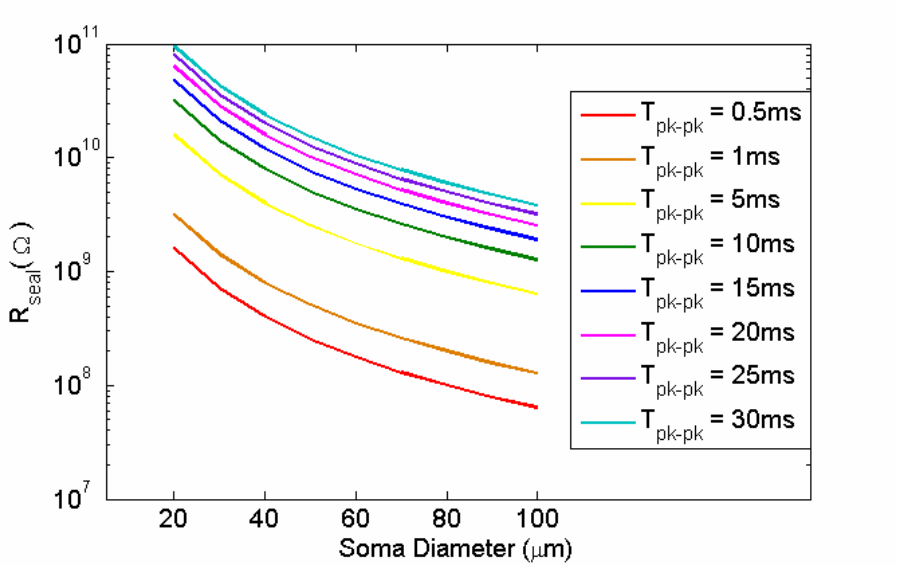

Figure 5.7

Critical values of R_{seal} for soma diameters between 20μm and 100μm and action potential durations of 0.5ms to 30ms.

The critical point values of R_{seal} required to ensure that the extracellularly measured signal is beyond this critical point are unrealistically large for simple cell-electrode adhesion. The maximum recorded seal of an extracellular system was that of Regehr [1] giving 4 MΩ from a 10 μm diameter electrode. Typical seal levels are lower than 1 MΩ [2,15] Patch clamp seals would need to be greater than this critical value, hence the GΩ seal requirement for good signal extraction.

5.1.3.2 The Critical Point for Positive Leading Spike (PLS) CAP signals

In the PLS CAP signal the capacitive transmembrane current is identified as the dominant factor in the signal shape. This signal is capacitively coupled to the cleft across the membrane capacitance. Extracellularly measured action potential signals are often the differential of the TMAP signal due to this mechanism.

Referring to figure 5.3, the open channel values of R_{Na2} and R_{K2} are much larger than the values for the original Hodgkin Huxley model in the soma membrane. This reduces the transmembrane ionic current to a value that is much lower than the capacitive current through C_{mem2} during the action potential.

Similarly to the NLS CAP, for large values of R_{seal} approaching infinity, the CAP will be identical to the TMAP. As R_{seal} is lowered there is a critical point where the CAP will distort from the TMAP signal and move towards the differential form.

The CAP signal may be calculated in the time domain as:

$$V_{ext} = R_{seal}\left(C_{mem2} \cdot \frac{d(V_{int} - V_{ext})}{dt}\right) \qquad 5.4$$

Or in the frequency domain:

$$V_{ext} = R_{seal}\left(C_{mem2} \cdot 2\pi jf\left(V_{int} - V_{ext}\right)\right) \qquad 5.5$$

giving,

$$\left|\frac{V_{ext}}{V_{in}}\right| = \frac{R_{seal} \cdot C_{mem2} \cdot 2\pi f}{1 + R_{seal} \cdot C_{mem2} \cdot 2\pi f} = \frac{R_{seal} \cdot C_{mem2} \cdot 2\pi f}{1 + R_{seal} \cdot 2\pi f \cdot c_{mem2} \cdot \pi \cdot d_{soma}{}^2 / 4} \qquad 5.6$$

This is the transfer function for a high pass filter. When R_{seal} is infinite V_{ext} is equal to V_{in} for all frequencies. As R_{seal} is lowered, one must consider the spectral frequencies present in a particular TMAP together with the RC time constant in equation 5.6.

To assist in the analysis the value of R_{seal} may be chosen to ensure that the lower frequency component of the neural signal spectrum is within 10% of its original value giving:

$$R_{seal} = \frac{9}{2\pi f \cdot c_m \cdot \pi \cdot d_{soma}{}^2 / 4} \qquad 5.7$$

The normalised spectral power of the TMAP from Helisoma B19 neuron and Aplysia MCC neuron [2] are presented in figure 5.8. The critical point for signal distortion of PLS action potentials may be calculated for these neurons by considering the minimum spectral frequency of the signal and equation 5.7.

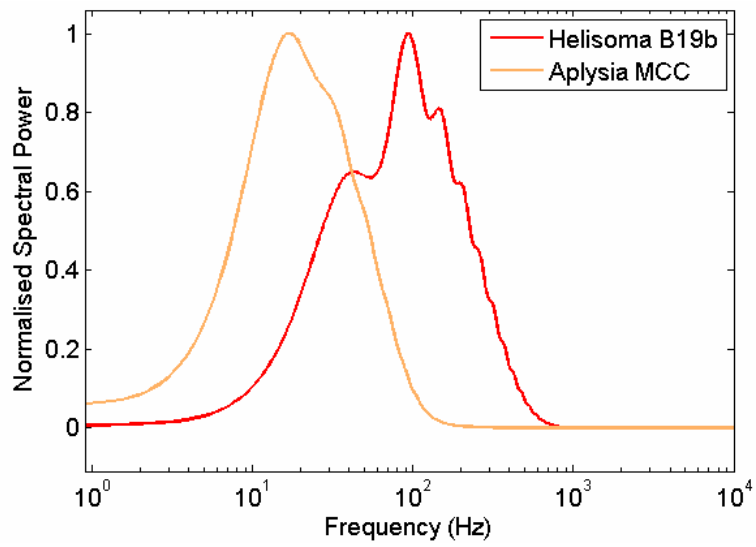

Figure 5.8

Normalised TMAP spectral power from Helisoma B19 neuron and Aplysia MCC neuron [2]

The Aplysia neuron shows a minimum power below 1 Hz. The Helisoma neuron shows a minimum power at approximately 2 Hz. If the high pass filter formed by the values of the membrane capacitance C_m and seal resistance R_{seal} presents a cut off frequency above these values the signal will begin to distort. Using equation 5.7, values of R_{seal} may be calculated. Figure 5.9 shows the possible range of R_{seal} values for signals with minimal spectral frequencies at 10 mHz to 100 Hz.

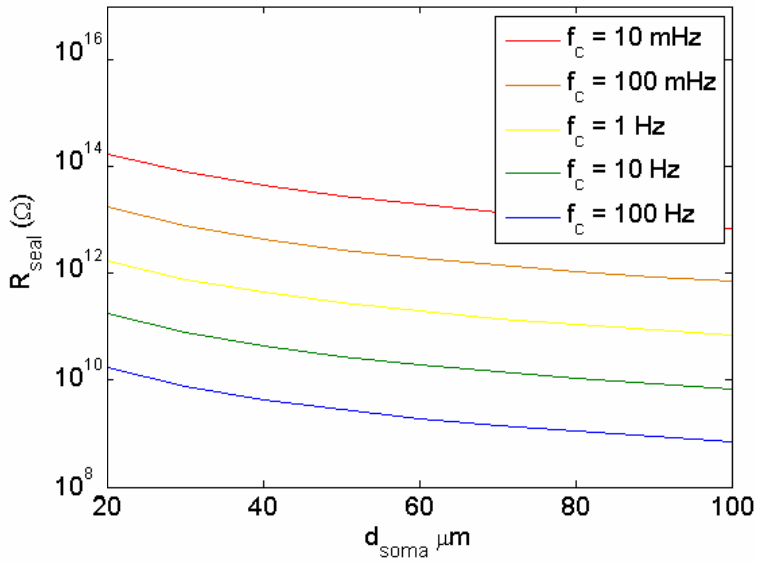

Figure 5.9

Critical values of R_{seal} for PLS CAP for soma diameters between 20 µm and 100 µm

For a 1 Hz cut-off frequency R_{seal} must be greater than 10 GΩ to ensure that the signal is above the critical point. This value will be lower for slower TMAP signals and higher for faster TMAP signals.

As with the NLS signal, the value of R_{seal} is much lower than the critical point for real extracellular measurements from neural cultures causing the differential signal to be dominant in most recorded data.

5.2 Calibration of the Model

This section uses extracted published data to calibrate the duration of the TMAP and CAP. Results from two prominent researchers in the field of extracellular measurement are used to calibrate the simulated signals and compare the resulting waveforms.

There are two distinct types of extracellular CAP signals that have been identified in the literature [2, 3]. These signal types are the positive leading spike PLS and the negative leading spike NLS. The mechanism for these signal types is due to the density of the voltage gated ion channels within the cleft. It has been shown in the literature that the ionic conductance per unit area may vary for different compartments in a real neuron [6, 8].

Considering the circuit in figure 5.3, the following relationships between the transmembrane currents and the CAP signal may be elucidated:

$$C_{mem}\frac{dV_{in}}{dt} << \left(I_{Na}+I_{k}\right): \qquad V_{cleft} \approx R_{seal}\left(I_{Na}+I_{K}\right) \tag{5.10}$$

$$C_{mem}\frac{dV_{in}}{dt} >> \left(I_{Na}+I_{k}\right): \qquad V_{cleft} \approx R_{seal}\left(C_{mem}\frac{dV_{in}}{dt}\right) \tag{5.11}$$

$$C_{mem}\frac{dV_{in}}{dt} \approx \left(I_{Na}+I_{k}\right): \qquad V_{cleft} \approx R_{seal}\left(C_{mem}\frac{dV_{in}}{dt}+I_{Na}+I_{k}\right) \tag{5.12}$$

Equation 5.10 is identified as the mechanism for the NLS, equation 5.11 is identified as the mechanism for the PLS. Equation 5.12 would give a hybrid signal between the two signal types.

Typically the values of g_{Na} and g_K are much lower at the soma than in the axon hillock and axon compartments. The effect of scaling the value of g_{Na} and g_K at the soma compartment upon the extra-cellular cleft potential is shown in figure 5.10. The plots were generated in SPICE using the model presented in figure 4.12 and general parameters from table 4.1.

The ratio between g_{Na} and g_K was left unaltered to preserve the shape of the action potential signal. Figure 5.10 shows the influence of the ionic currents upon the extracellular signal. Figure 5.10 A corresponds to equation 5.12 and figure 5.10 parts B, C and D correspond to equation 5.11.

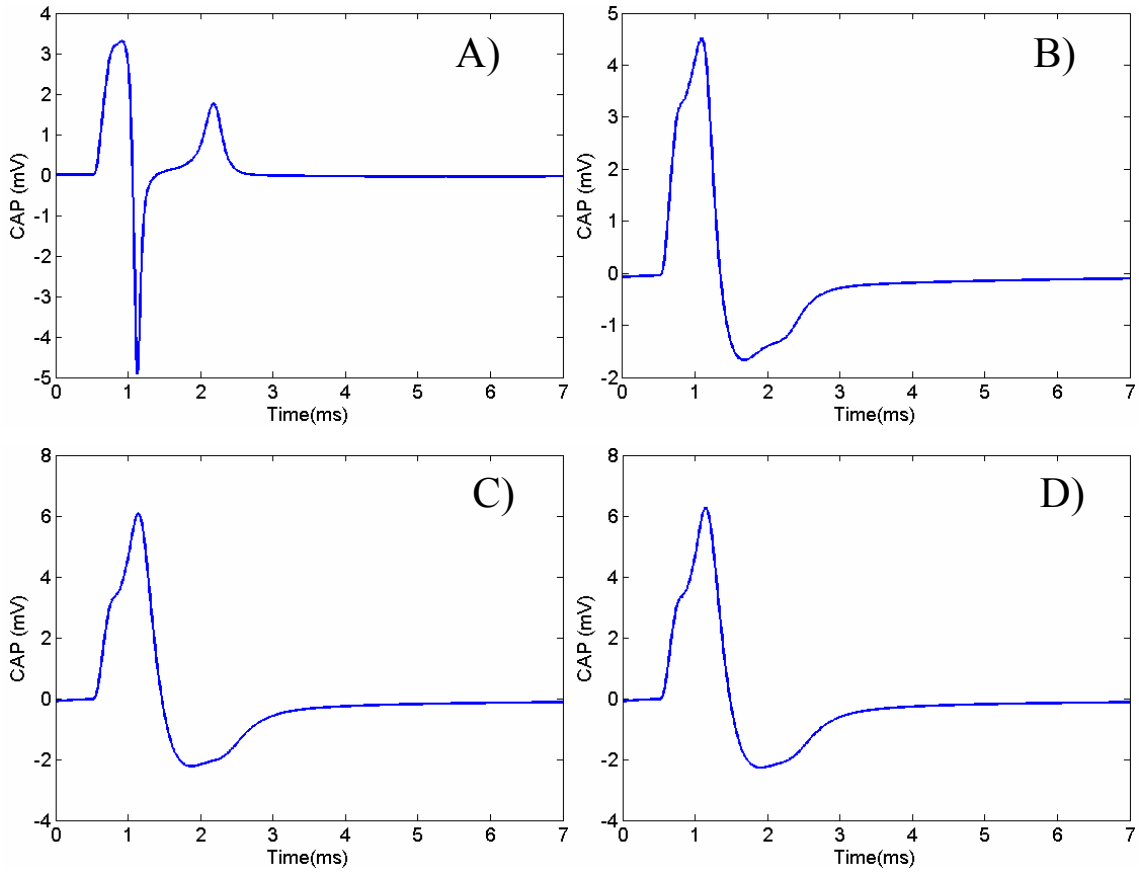

Figure 5.10

CAP signals from the Hodgkin and Huxley model with varying values of g_{Na} and g_K: A.) $g_{Na} = 120mS/cm^2$, $g_K = 36mS/cm^2$. B.) $g_{Na} = 12mS/cm^2$, $g_K = 3.6mS/cm^2$. C.) $g_{Na} = 1.2mS/cm^2$, $g_K = 360\mu S/cm^2$. D.) $g_{Na} = 120\mu S/cm^2$, $g_K = 36\mu S/cm^2$.

Signals recorded at the soma by Regehr [2] and Fromherz [3] show definite properties of equation 5.11 and give a PLS signal similar to that shown in figure 5.10 parts B to D. An example of a PLS signal taken from the work of Regehr is shown in figure 5.11 A. Signals showing a NLS signal have also been demonstrated by Regehr and Fromherz and are attributed by both authors to the extracellular microelectrode being positioned beneath the axon hillock where there is typically a very high density of Na^+ and K^+ channels. Heer et al. [7] have recorded NLS signals from the somas of chicken cardiomyocite cells. Examples of the NLS signals are shown in figure 5.11 B.), taken from Heer et al. and C.), taken from Regehr et al.

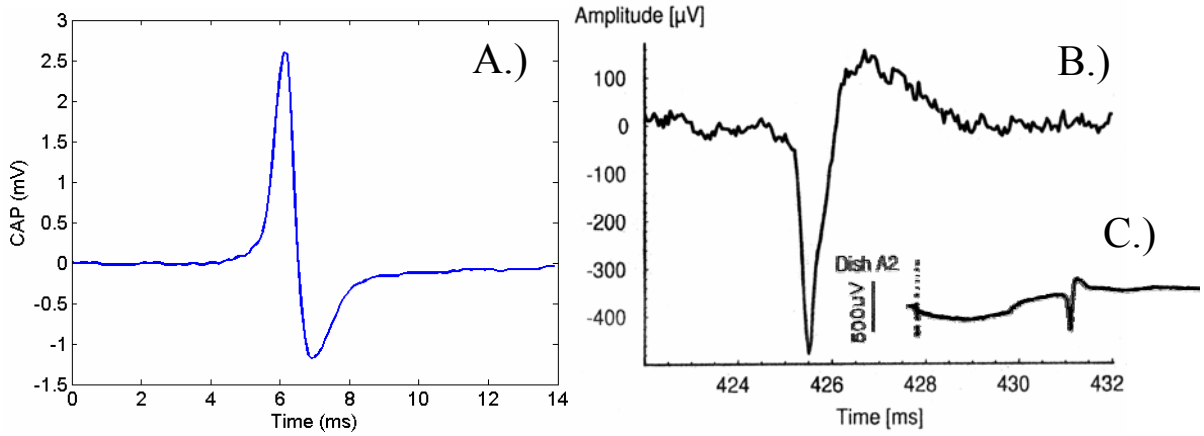

Figure 5.11

A.) The positive first spike CAP. B.) and C.) the negative first spike CAP. Data taken from Regehr et al [2] and Heer et al.[7]

The PLS spike in figure 5.11 A may be reproduced in SPICE by reducing the values of g_{Na} and g_K by a factor of one tenth or more. The intracellular signal at the soma is driven by the ion channels in the hillock. The CAP signal is the differential of the TMAP initiated in the hillock. The NLS spike in figure 5.11 B may be reproduced with the values of g_{Na} and g_K as specified by Hodgkin and Huxley only when the action potential is initiated within the soma by direct intracellular stimulation rather than by the propagation of a TMAP through the compartment model. When the action potential is initiated in the compartment the depolarisation is dominated by the ionic current and does not have an additional leading capacitive component due to the propagation of the TMAP.

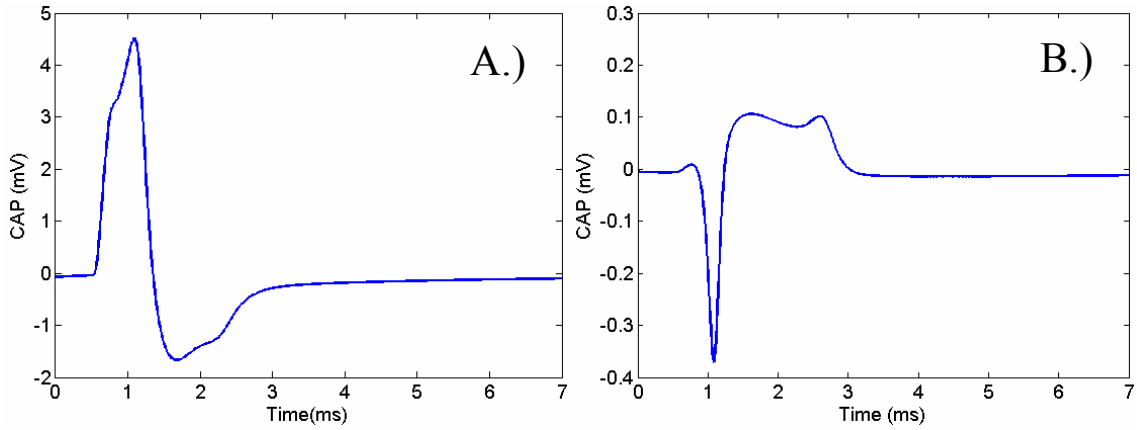

Figure 5.12

Simulated PLS and NLS signals. A.) PLS at soma, normal TMAP propagation, with g_{Na} = 12mS/cm^2, g_K = 3.6mS/cm^2. B.) NLS initiated at soma with g_{Na} = 120mS/cm^2, g_K = 36mS/cm^2.

5.2.1 Selection of Published Extracellular Signals for Comparison

Extracellular neural signals were extracted from a selection of peer reviewed publications containing extracellular microelectrode recording traces from snail, slug and leech neurons; these neuron types have typically been favoured for extracellular measurement as they are simple to acquire and work with. Only recordings identified by the authors as being the result of electrodes positioned within a sealed cleft on or beneath the soma were used, i.e. PLS action potentials.

Data was extracted from the print copies by optical scanning and processed in Matlab to threshold and convert the 2D image arrays into appropriately scaled x,y graphical plots.

The x,y data was then resampled in Matlab to a common time base of 10 μs per sample for direct comparison.

5.2.2 Comparison with Extracellular Soma Recordings from Helisoma B19, Hirudo Retzius and Aplysia MCC Neurons

The measurement of the CAP signal in figure 5.13 was taken using a novel extracellular microelectrode fabricated into the tip of a micro cantilever structure. The structure was named the 'diving board' electrode by Regehr et al. [1]. The cantilever applies vertical pressure to a suitably placed soma, forming a tight surface fit between the membrane and the electrode to augment the seal resistance. The microelectrode and the cleft area in this measurement was 10 μm. The soma diameter was measured to be 70 μm from photographs of the culture published in the source journal using the scale provided.

Measurement of the CAP neural signals in figures 5.14, 5.15 and 5.16 were taken by 12 μm diameter extracellular planar disc microelectrodes. The electrodes were fabricated into the substrate of the culture dish, following the procedure described in [2]. Electrodes were positioned directly beneath the soma of the neurons during measurements giving the large signal amplitudes shown in the figures. Seal resistances are indicated where values were given in the literature. CAP signals are presented with corresponding TMAP signals except figure 5.14 where the TMAP data was not presented in the source journal. The soma diameter measured to be 80μm for the signal presented in figure 5.14 and 70μm for the signals presented figures 5.15 and 5.16.

Figure 5.17 presents data published by Fromherz et al. using a field effect transistor (FET) to measure the extracellular CAP signals from Hirudo Retzius neurons [3]. The transistor is positioned in the substrate as with the typical extracellular MEA. The CAP signal is electrically coupled to the gate of the transistor and modulates the source to drain current. The CAP signal is then calculated by measuring the current and applying the transconductance equation of a FET. The soma diameter was also approximately 70μm diameter in this example.

The variables used in the simulation to fit the CAP to the extracted data are presented in table 5.1.

Variable	Helisoma B19a Regehr[1]	Helisoma B19b Regehr[2]	MCC Aplysia Regehr[2]	Hirudo Retzius Regehr[2]	Hirudo Retzius Fromherz [3]	Units
K	1.384	2.5836	0.3945	1.1398	1.55	-
d_{soma}	70	80	70	70	70	µm
R_{seal}	4	0.7	2.1	0.125	0.7	MΩ
I_{stim}	2	2	2	2	2	nA
t_{stim}	2	2	2	2	2	ms

Table 5.1

Pertinent model variables modified from generic values to reproduce extracted signal form

The fitted CAP signals are plotted in figures 5.13 – 5.17 together with the extracted source CAP.

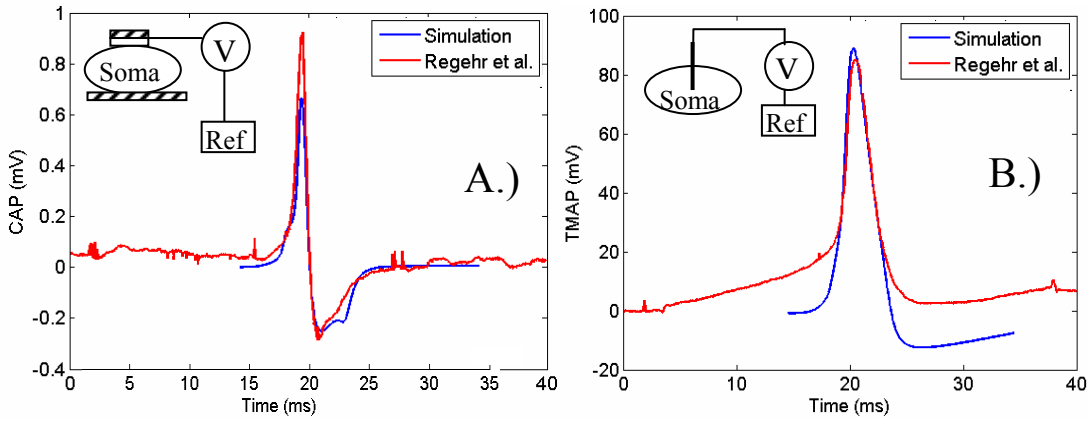

Figure 5.13

Real signals for Helisoma B19 neuron compared with simulated signals from model: A.) CAP and B.) TMAP. Diagram shows electrode connection to neuron indicated in source journal and reproduced in simulation. Real signals extracted from figure 9A [1]. Seal resistance indicated in literature as 4 MΩ.

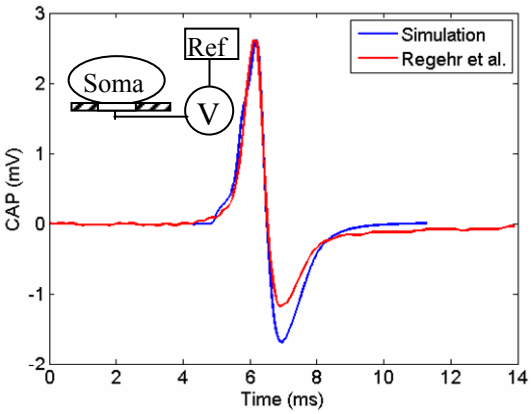

Figure 5.14

Real CAP signal for Helisoma B19 neuron compared with simulated signals from model. There was no intracellular TMAP signal published in this instance. Real signal extracted from figure 4B [2]. Seal resistance not indicated in source journal.

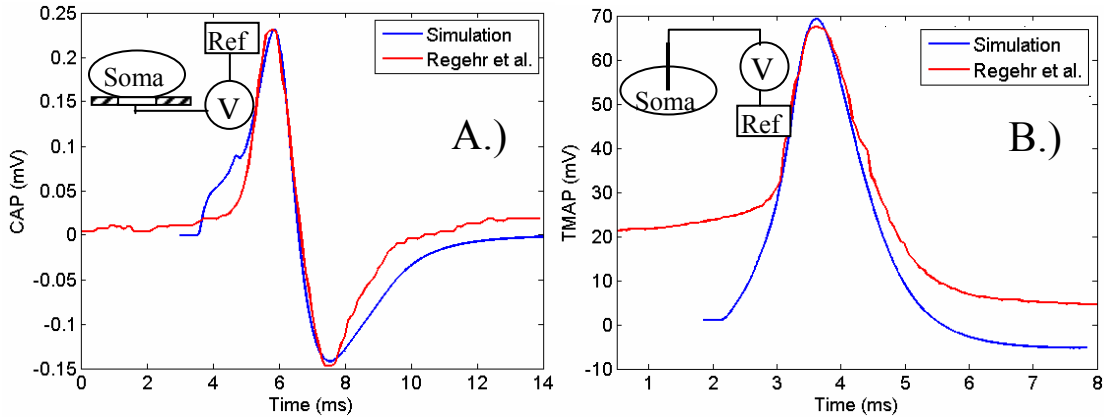

Figure 5.15

Real signals for Hirudo Retzius neuron compared with simulated signals from model: A.) CAP and B.) TMAP. Real signals extracted from figure 6.f [2]. Seal resistance not indicated in source journal.

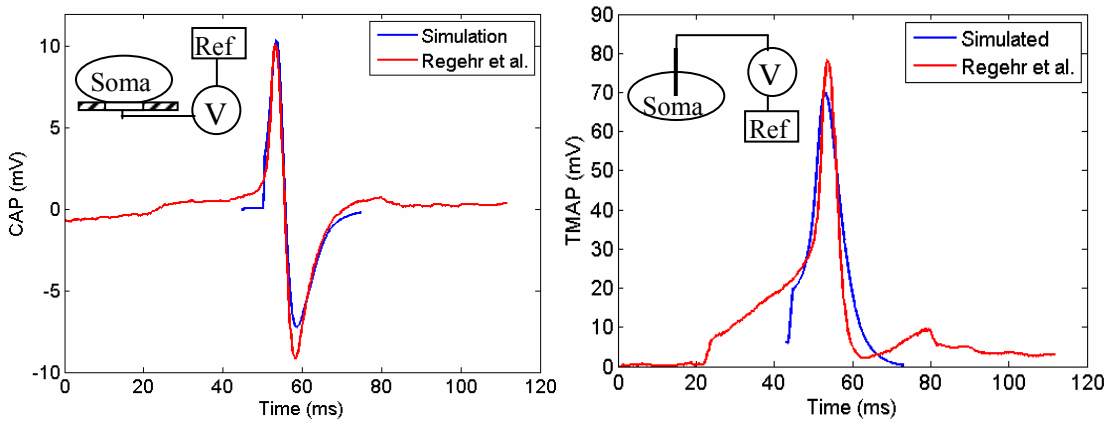

Figure 5.16

Real signals for Aplysia MCC neuron compared with simulated signals from model: A.) CAP and B.) TMAP. Real signals extracted from figure 8 [2]. Seal resistance not indicated in source journal.

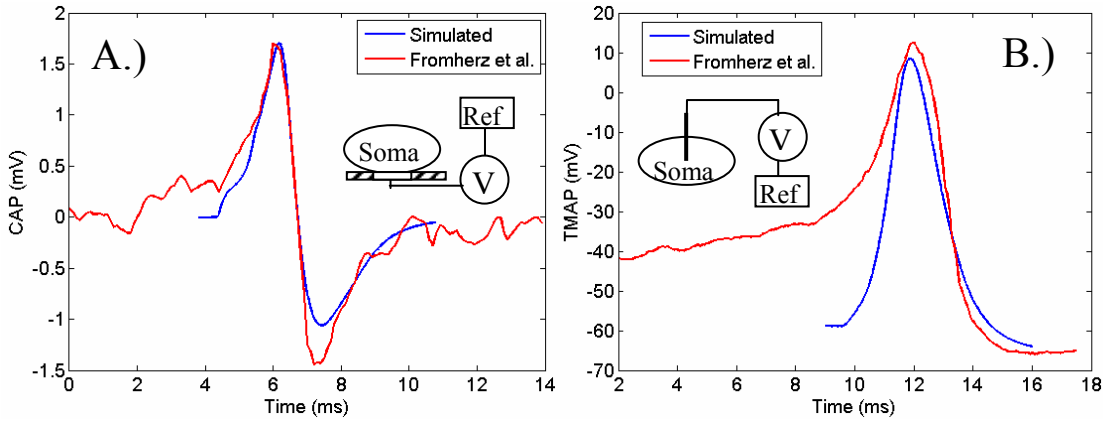

Figure 5.17

Real signals for Hirudo Retzius neuron compared with simulated signals from model: A.) CAP and B.) TMAP. Real signals extracted from figure 6A [3]. Seal resistance not indicated in source journal.

The fitted CAP signals indicate that the duration of the CAP and TMAP for different species of invertebrate and neuron is dependent upon the dynamics of ion channel opening and closing in the hillock.

5.2.3 Analysis of Simulated Extracellular Signals

The simulated signals were compared to the extracted data from the literature and the mean square error for the data was calculated. The root mean squared error (RMSE) for the simulated data may be calculated using the formula:

$$\mathrm{RMSE} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(e_i)^2} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(\mathrm{Vmeas}_i - \mathrm{Vsim}_i)^2} \qquad 5.5$$

where *n* is the total number of compared samples, *i* is the sample indices. Vmeas is the measured signal and Vsim is the simulated signal.

The normalised RMS error (NRMSE) for the simulated CAP signals in figures 5.13 – 5.17 are summarised in table 5.2. This is calculated by:

$$\mathrm{NRMSE} = \frac{\mathrm{RMSE}}{\mathrm{Vmeas}_{pk-pk}} \qquad 5.6$$

This allows direct comparison between the different signals source which each have different amplitudes.

Variable	Helisoma B19a (Regehr) [1]	Helisoma B19b (Regehr) [2]	MCC Aplysia (Regehr) [2]	Hirudo Retzius (Regehr) [2]	Hirudo Retzius (Fromherz) [3]	Units
RMSE	0.0654	0.3782	1.0066	0.0271	0.206	mV
NRMSE	0.054	0.090	0.0524	0.0714	0.0655	-

Table 5.2

Mean squared error for the simulated neural signals

The Hodgkin Huxley PLS model presents a good fit to the CAP signals with a NRMSE value between 5.4% and 9% across the fitted data.

5.3 Investigation of Simulated Action Potentials

In this section the fitted variables from table 5.1 are applied to the model to simulate the CAP over a defined range of values of d_{soma}, R_{seal} and channel opening dynamics as defined by the K variable in section 5.2.2. The values of the component circuit elements used in the model are calculated using values taken from the literature. These values are summarised in table 5.3. The equations for calculating the circuit elements in the cleft circuit are summarised in table 5.4.

Parameter	Value(s)	Units	Source
d_{soma}	20 -100	μm	Table 4.1
l_{cleft}	37	nm	[9]
c_{mem}	1	$\mu F/cm^2$	Table 4.1
ρ_e	70	Ωcm	Table 4.1
R_{seal}	0-10	MΩ	[1,2,3,15]
g_{Na}	120	mS/cm^2	Table 4.1
g_K	36	mS/cm^2	Table 4.1
g_L	0.3	mS/cm^2	Table 4.1
m(rest)	0.05	-	[4]
h(rest)	0.6	-	[4]
n(rest)	0.32	-	[4]
m(peak)	0.65	-	[4]
h(peak)	0.3	-	[4]
n(peak)	0.6	-	[4]

Table 5.3

Summary of intrinsic values of components forming the cleft circuit

Parameter	Min	Max	Units	Equation	Source
A_{cleft}	3.1	79	$10^{-6}\,cm^2$	$\pi\left(\frac{d_{soma}}{2}\right)^2$	4.32
R_{spread}	1	5	kΩ	$\rho/2\pi d_{soma}$	4.39b
C_{mem}	3.1	79	pF	$c_m A_{cleft}$	[4]
R_{mem} (rest)	18.6	464	MΩ	$\left[\left(g_{Na}m^3h + g_K n^4 + g_L\right)A_{cleft}\right]^{-1}$	4.8, 4.9 [4]
R_{mem} (peak)	0.86	21.4	MΩ	$\left[\left(g_{Na}m^3h + g_K n^4 + g_L\right)A_{cleft}\right]^{-1}$	4.8, 4.9 [4]
R_{cleft}	3	80	Ω	$\frac{\rho_e l_{cleft}}{A_{cleft}}$	4.33

Table 5.4

Equations and range of values for cleft circuit components

The simulation is performed to define the range of signal amplitude and spectral frequencies that may occur in planar microelectrode recordings. The results are to be used in chapter 9 and 10 to define the input circuitry and minimum sampling rate for the active microelectrode array (MEA) system on chip.

5.3.1 Effect of Soma Diameter and R_{seal} upon CAP Amplitude

The simulation was set using variables from table 4.1, 5.1 and 5.4 to reproduce the CAP signal shape for Helisoma B19b and Aplysia MCC neurons. The simulation was repeated for soma diameters between 20 μm and 100 μm and values of R_{seal} between 10 kΩ and 10 MΩ for the Helisoma B19 model and between 10 kΩ and 100 MΩ for the Aplysia MCC model. The CAP signal amplitude was measured for each simulation repetition and plotted in figure 5.18 for the Helisoma B19 model and figure 5.19 for the Aplysia MCC model to show the range in values between the fastest and slowest peak to peak fitted signals.

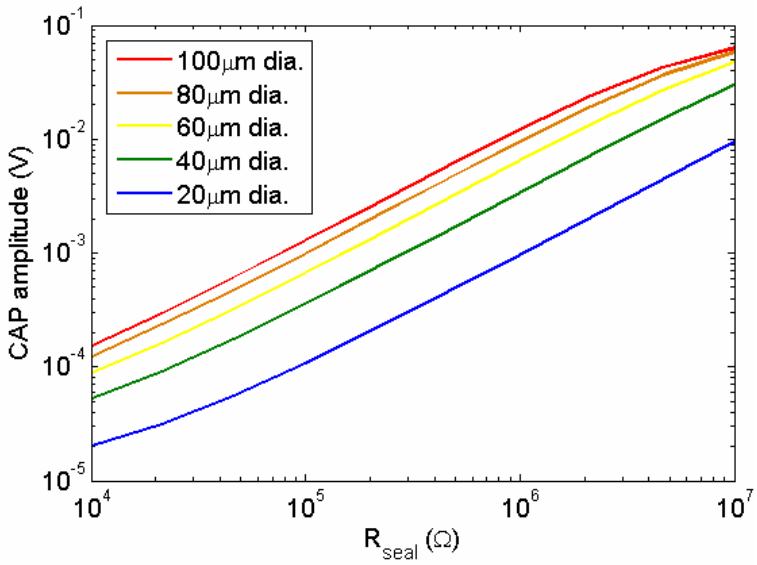

Figure 5.18

Effect of R_{seal} upon CAP amplitude for Helisoma B19 type model

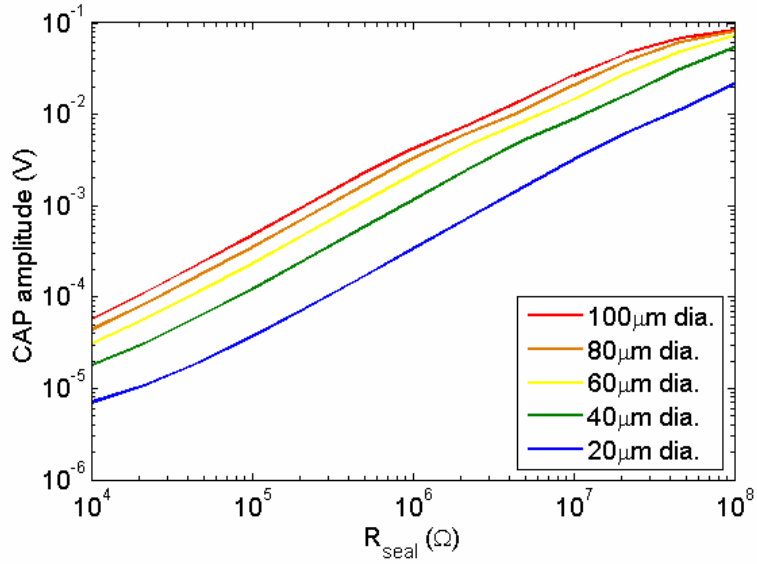

Figure 5.19

Effect of R_{seal} upon CAP amplitude for Aplysia MCC type model

5.3.2 Effect of Soma Diameter and R_{seal} upon the Spectral Frequencies of the CAP.

The simulated CAP signal waveforms generated for section 5.3.1 were processed in Matlab to determine the spectral frequency range of the Helisoma B19 and Aplysia

MCC. The value of the soma diameter and R_{seal} were shown to shift the higher power spectral frequencies. Smaller diameter somas demonstrated shifts of the higher power spectral frequency to higher frequencies as did lower values of R_{seal}. Larger soma diameters and higher R_{seal} values each demonstrated shifts to lower frequencies.

The spectral frequencies of the maximum and minimum higher power spectral frequency CAP signals are shown for the two models in figure 5.20 and 5.21. The frequency of peak spectral power is approximately twice the inverse of the CAP peak to peak time.

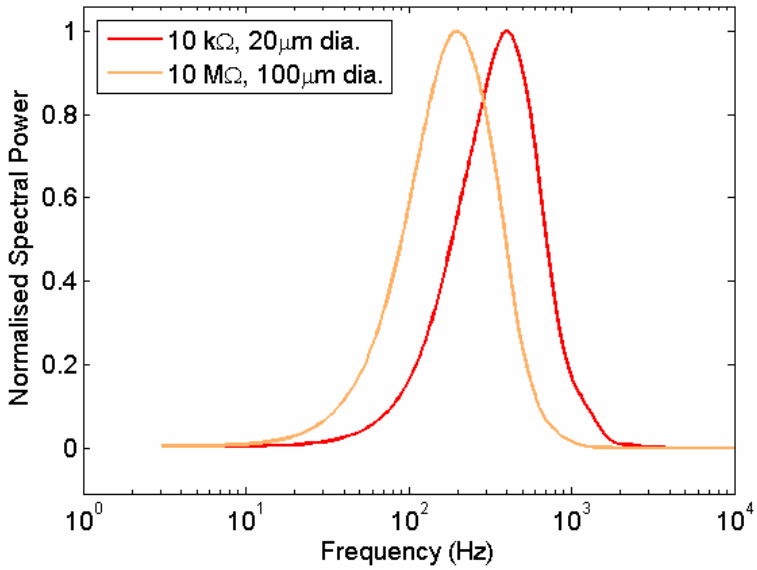

Figure 5.20

Normalised spectral power density for Helisoma B19 type model showing maximum and minimum curves

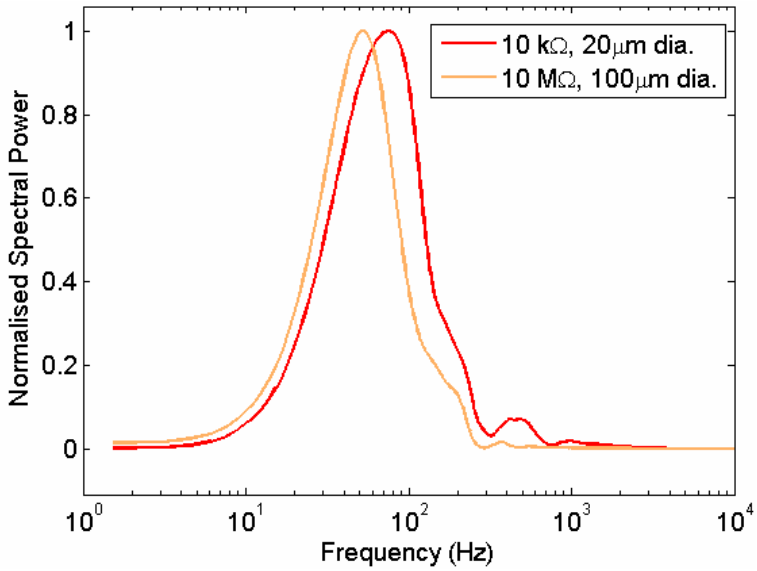

Figure 5.21

Normalised spectral power density for Aplysia type model showing maximum and minimum curves

The implication of these results is discussed in section 5.5.2.

5.3.3 Thermal Noise within the Cleft

This may be approximated by assuming that the noise of the system occurs predominantly from thermal fluctuations within the signal path. The thermal or Johnson noise may be calculated for real electrolytic impedances as well as those in the solid state as outlined by Johnson and Nyquist [10, 11].For the cleft-seal interface model, as shown in Figure 5.3, the circuit elements within the CAP signal path are: C_{mem2}, R_{K2}, R_{Na2}, R_{cleft}, R_{Seal} and R_{spread}. The cleft circuit is redrawn in figure 5.22A with R_{K2} and R_{Na2} replaced by the parallel equivalent resistance R_{mem}. C_{mem2} is replaced by C_{mem} for the analysis. The relevant noise sources associated to each resistor are included in the figure. The noise analysis model is presented in 5.22B as advised in the texts [12, 13].

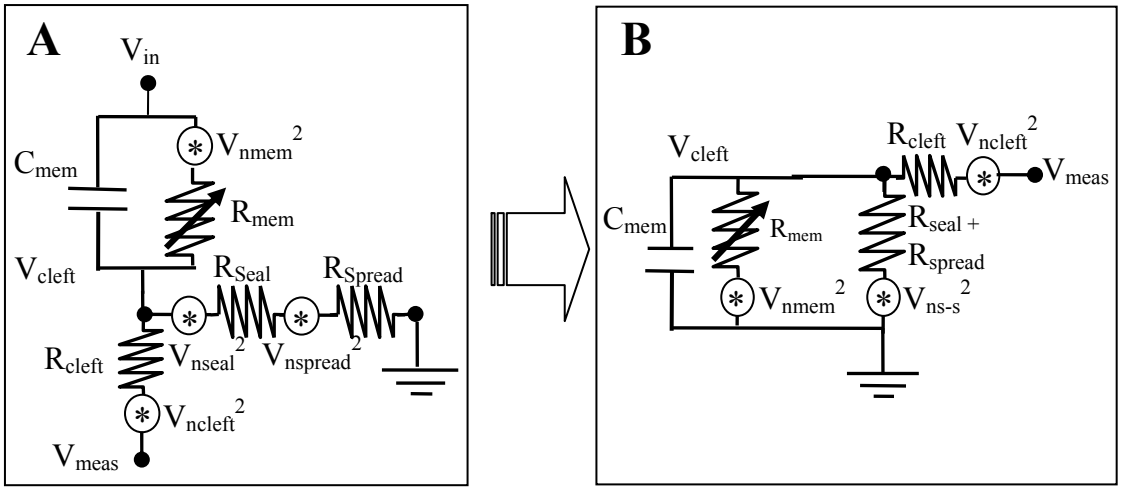

Figure 5.22

Thermal noise sources in the CAP signal path: A. the cleft model, B the noise analysis model

The thermal noise of a resistive circuit element is characterised by the Johnson-Nyquist equation:

$$V_{jn}(\text{rms}) = \sqrt{4kTRf} \qquad 5.8a$$

Where

k is Boltzmans constant.

T is the absolute temperature

R is the equivalent noise resistance

f is the frequency range of the measurement circuit

As shown in figure 5.22, thermal noise is only generated by the resistances in the circuit. R_{cleft} is shown to be several orders of magnitude smaller than R_{mem} and $R_{seal+spread}$ in table 5.3. As it is small and in series connection to $R_{mem} \,||\, R_{seal+spread}$ it may be removed from the analysis as its noise contribution will be negligible. The rms noise voltage presented to the electrode at node V_{meas} is:

$$V_n = \sqrt{4kT\left(\frac{R_{seal+spread}R_{mem}}{\left(R_{mem}+R_{seal+spread}\right)}\right)\cdot f}\ . \qquad 5.8b$$

The frequency range f is selected to be 5 kHz, which overlaps the spectral range of the simulated neural signals presented in section 5.3.2.

The capacitance C_{mem} does not contribute to the total noise within the cleft but may filter its value if the time constant of the circuit falls within the bandwidth of the measurement circuit. This is known as the noise effective bandwidth (NEB) [14]. This limits the bandwidth of the noise within the circuit to a fixed value, dependent upon $R_{seal+spread}$, R_{mem} and C_{mem}. The NEB will replace the measurement frequency range f in equation 5.8b. The NEB may be calculated by integrating the transfer function of the circuit in figure 5.22B with respect to the angular frequency:

$$NEB = \frac{1}{2\pi} \frac{R_{mem} + R_{seal+spread}}{C_{mem} R_{mem} R_{seal+spread}} \left[\tan^{-1} \left(\frac{2\pi \cdot f \cdot C_{mem} R_{mem} R_{seal+spread}}{R_{mem} + R_{seal+spread}} \right) \right]_0^f \qquad 5.9$$

The rms thermal cleft noise for a range of soma diameters was calculated using the maximum and minimum values for the variable R_{mem} (which is dependent upon d_{soma}) given in table 5.4 (d_{soma}). R_{seal} takes the range of values given in table 5.3. This encompasses typical values as measured by Regehr et al. [1, 2] and Fromherz [3, 15] The lower level of R_{spread} is held at 10 kΩ to simplify the analysis and allow direct comparison with the simulation data generated for section 5.3.1.. This presents the lowest value of $R_{seal+spread}$ and simplifies the presentation of data on table 5.5.

Resting state						
d_{soma} (µm)	**R_{mem}** (MΩ)	**$R_{seal+spread}$ = 10 kΩ**	**$R_{seal+spread}$ = 100 kΩ**	**$R_{seal+spread}$ = 1 MΩ**	**$R_{seal+spread}$ = 10 MΩ**	**$R_{seal+spread}$ = ∞**
20	463.7	0.9 µV (rms)	2.8 µV (rms)	8.9 µV (rms)	25 µV (rms)	35.8 µV (rms)
50	74.5	0.9 µV (rms)	2.8 µV (rms)	8.5 µV (rms)	13.5 µV (rms)	14.4 µV (rms)
100	18.5	0.9 µV (rms)	2.8 µV (rms)	6.1 µV (rms)	7 µV (rms)	7.2 µV (rms)
Action potential peak						
d_{soma} (µm)	**R_{mem}** (MΩ)	**$R_{seal+spread}$ = 10 kΩ**	**$R_{seal+spread}$ = 100 kΩ**	**$R_{seal+spread}$ = 1 MΩ**	**$R_{seal+spread}$ = 10 MΩ**	**$R_{seal+spread}$ = ∞**
20	21.4	0.9 µV (rms)	2.8 µV (rms)	8.8 µV (rms)	22 µV (rms)	35.8 µV (rms)
50	3.4	0.9 µV (rms)	2.8 µV (rms)	7.6 µV (rms)	11.5 µV (rms)	14.4 µV (rms)
100	0.9	0.9 µV (rms)	2.7 µV (rms)	5.3 µV (rms)	5.9 µV (rms)	7.2 µV (rms)

Table 5.5

Summary table of rms noise within the cleft for varying resistances of R_s and R_{mem}

The analysis shows that the rms thermal noise within the cleft circuit is capped at kT/C_{mem} as f, R_{mem} and $R_{seal+spread}$ tend to infinity due to the influence of C_{mem} upon the NEB. This has been verified by simulating the noise of the cleft node in SPICE. The SPICE simulation results are presented in figure 5.23 and 5.24 during the membrane resting state and the action potential peak respectively, to verify the analytical calculation.

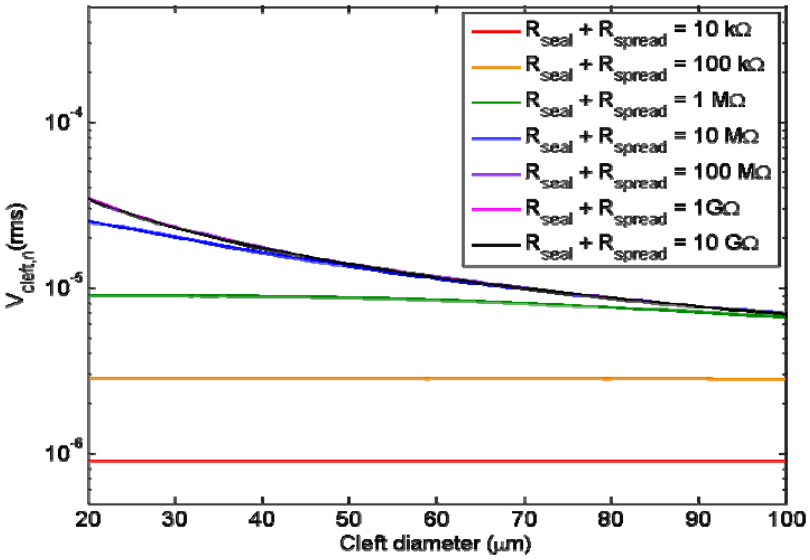

Figure 5.23

SPICE (Cadence Virtuoso) simulation of rms noise voltage within the cleft during membrane resting state.

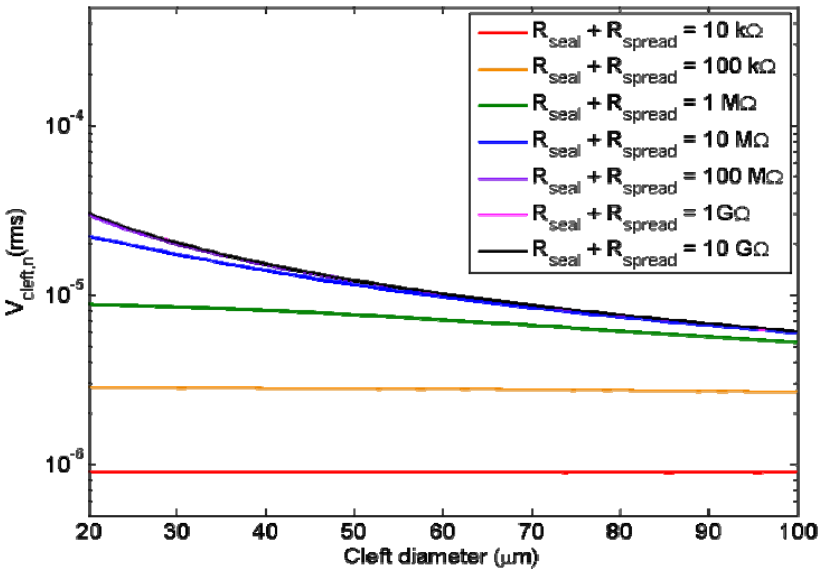

Figure 5.24

SPICE (Cadence Virtuoso) simulation of rms noise voltage within the cleft during action potential peak.

$R_{seal+spread}$ may be shown to be the dominant thermal noise source in the cleft circuit for the range of R_{mem} during the resting state as its range of values (10 kΩ – 10 MΩ) are smaller than R_{mem} (18.5 MΩ – 464 MΩ). During the action potential peak, the range of values for $R_{seal+spread}$ and R_{mem} may intersect. For large diameter somas with large associated $R_{seal+spread,}$ R_{mem} will begin to dominate the noise; however the overall noise contribution is shown to be close to that of the resting state as shown in table 5.5.

The signal to noise ratio of the CAP signal for the Helisoma B19 and Aplysia MCC neuron models was calculated using data from SPICE simulations of the cleft model presented previously in figures 5.18-5.19 over the range of variables:
d_{soma} = 20 µm - 100 µm and $R_{seal+spread}$ = 10 kΩ – 10 MΩ. The results are plotted in figure 5.25. The peak to peak noise was determined for a 99% confidence interval (CI). This is 6x the rms value.

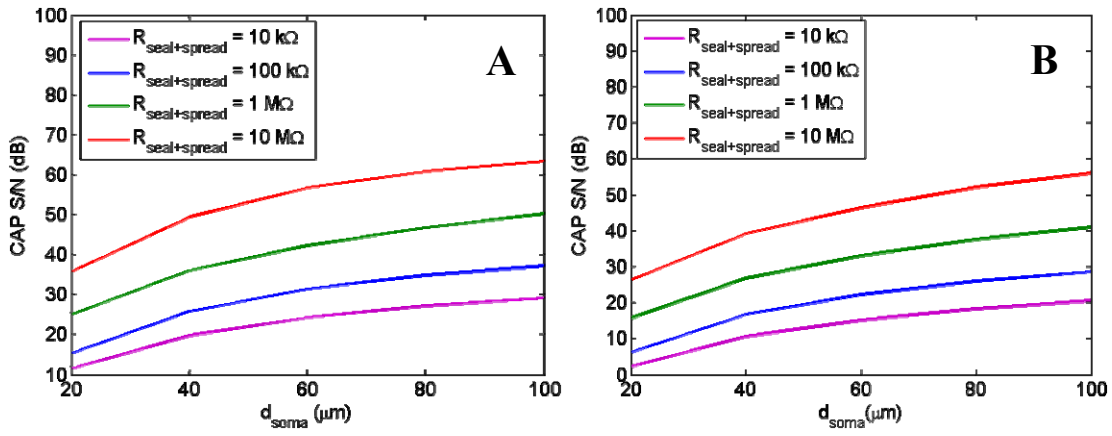

Figure 5.25

Signal to noise ratio range for A, Helisoma B19 neuron model and B, Aplysia MCC neuron model over the range of d_{soma} and $R_{seal+spread}$ values given in table 5.3 and 5.4

It was shown in figures 5.18 and 5.19 that the amplitude of the CAP signal for a given soma diameter is proportional to the value of the seal resistance (R_{seal}). Similarly the rms noise within the cleft is shown to be proportional to $\sqrt{R_{seal+spread} \parallel R_{mem}}$. For large values of $R_{seal+rspread}$, large signal to noise ratios are observed (20 dB – 60 dB) due to the limiting of the noise by k_BT / C_{mem}. As R_{seal} tends to infinity, the CAP signal will become equal to the TMAP as shown in section 5.1.3.1. It is proposed that this is the

mechanism that allows patch-clamp signals to be measured without being obscured by the noise generated by values of R_{seal} upwards of 10 GΩ.

The signal to noise is at its lowest when d_{soma} and $R_{seal+spread}$ are small. This is due to the CAP signal being attenuated by the circuit to an amplitude where it is close to the peak to peak noise level. Consulting figures 5.18 - 5.19; when d_{soma} = 20 μm and $R_{seal\ +spread}$ = 10 kΩ the peak-peak amplitude of the CAP signal is 7 μV - 20 μV over the two models (this represents the upper and lower amplitudes across the five fitted models presented in section 5.2.2.). By consulting table 5.5; the noise in the cleft when d_{soma} = 20 μm and $R_{seal\ +spread}$ = 10 kΩ is 0.9 μV rms or 5.4 μV peak-peak (99% CI). This will result in a 2 dB signal to noise ratio for the Aplysia MCC model and 11.5 dB for the Helisoma B19 model as shown in figure 5.25A and 5.25B respectively.

In the region of operation where $R_{seal+spread}$ is small noise from the measurement circuit, including the microelectrode and the amplifier, may begin to obscure the CAP signal before the signal to noise level within the cleft reaches the practical minimum for CAP signal extraction (the microelectrode noise in particular is expected to be of the order of several μV rms over the applicable frequency range [14]). For an optimal CAP amplitude recording range, the measurement circuitry must be designed to introduce minimal additional noise to the signal. Thus, the noise of the electrode and measurement circuit will determine the practical noise floor.

The noise predictions from the simulation present similar noise levels to that of experimentally recorded data of CAP signals. The noise floor - including the electrode interface and instrumentation noise - is small compared to the neural signals, such that signals with 10s μV amplitudes have been observed [1, 2]. This gives confidence that the extracellular method utilising the cleft seal to measure action potentials is possible. The simulations presented in this chapter build upon this assumption.

5.4 Offsets and Loading Errors from the Measurement Circuit

This section examines the effects of the measurement circuit upon the CAP signal. Ideally the measurement circuit should draw no charge from the signal source; however the amplifier input, the MEA substrate, the electrode to amplifier interconnection tracks and any front end filter circuitry will present a lumped high impedance path to ground. For signals with large source impedances such as the CAP we must ensure that the impedance of the source signal is much smaller than the lumped shunt input impedance of the measurement circuit.

5.4.1 The Electrode

The electrode is considered to provide a wholly capacitive coupling between the measurement circuitry and the extracellular cleft. For Au or Pt electrodes, this is a good assumption as for small signals around the electrodes equilibrium potential, the electrode dc surface resistivity r_{ct} is very large [16] and the phase of the ac impedance is close to -90°; this is investigated in more depth in chapters 6 and 7. Assuming a perfect seal the circuit between the neuron and electrode is as presented in figure 5.26.

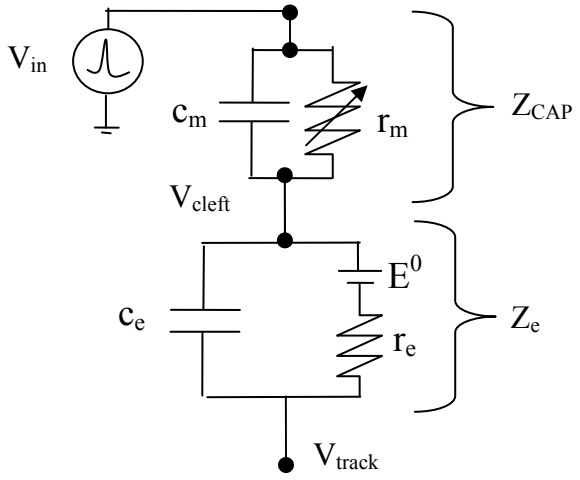

Figure 5.26

Electrical circuit between the TMAP and the recording electrode

5.4.1.1 Electrode Impedance

The interfacial capacitance per unit area is of the order of 10 μF/cm^2 [16] within the frequency spectrum of the CAP for an electrode with smooth surface profile. The series resistance of the cleft volume R_{cleft} is again neglected due to its much lower relative value.

It was proposed in section 5.3 that for somatic clefts of Helisoma, Aplysia and Hirudo cultured neurons, the CAP is dominated by the capacitive current resulting from $C_m dV_i/dt$. The CAP source impedance is therefore calculated by:

$$Z_{CAP} = \frac{1}{2\pi f C_m} = \frac{1}{2\pi f c_m \cdot A_{cleft}} \qquad 5.13$$

Where C_m is the total membrane capacitance within the cleft, c_m is the membrane capacitance per unit area and A_{cleft} is the surface area of the membrane contained within the cleft.

Similarly, for the electrode, assuming that it is enclosed by the cleft:

$$Z_e = \frac{1}{2\pi f C_e} = \frac{1}{2\pi f c_e \cdot A_{electrode}} \qquad 5.14$$

Typically the value of c_m is no more than 1μF/cm^2, indicating that for electrode sizes equivalent to that of the cleft area and down to one tenth of the area of the enclosed membrane the electrode will not increase the impedance of the signal path as measured by the amplifier circuit. Below this value the source impedance of the signal will be influenced by the capacitance of the electrode.

The source impedance must be considered during the measurement circuit design. The measurement circuit load impedance must be much greater than the signal source impedance. For smooth electrodes with surface areas many times smaller than the cleft formed by the neuron, the impedance of the electrode Z_e may be used as the basis for this calculation, otherwise the membrane capacitance Z_{CAP} must be used. For extracellular CAP signal measurements the constraints of the electrode impedance are

loosened by the seal resistance R_{seal} which is typically much lower than either Z_{CAP} or Z_e and will ultimately define the requirements for the measurement circuit. This is discussed further in section 5.5.1.

5.4.1.2 Electrode-Electrolyte Interface Potential

The interface between the electrode and the extracellular fluid presents a dc offset potential, E^0 that is of the order of tens of mV. If the electrode is connected directly to the input of a high gain, high input impedance amplifier, the offset will be super-imposed onto the neural signal. This offset must be removed as it will be amplified together with the offset signal and cause saturation due to the finite output voltage range of the amplifier. For the metals Pt and Au in physiological saline there is insufficient electrochemical charge transfer to drive current at the equilibrium potential. Therefore a cell formed between the measurement electrode and the recording electrode will have insignificant driving current to sustain the potential for all but open circuit measurements, facilitated by the high impedance (>1 TΩ) of the inputs. This is physically investigated in chapter 7, section 7.4.2. In the simulation, the effects of E^0 may be removed by placing a decoupling capacitor between the electrode and the amplifier input or by lowering the dc input impedance of the input measurement circuit by several orders of magnitude below R_{ct}.

5.4.2 Parasitic Losses

Parasitic signal losses are caused by shunting from track to substrate and track to track leakage conductances and capacitances. The amplifier input can also introduce similar shunting effects depending upon the input transistor type. FETs as a rule have input impedances that are many orders of magnitude larger than that of bipolar transistors. Circuit parasitic resistances and capacitances were discussed in section 3.2.1 and were included into the SPICE model as described in chapter 4 for analysis. The lumped circuit model is illustrated in figure 5.27.

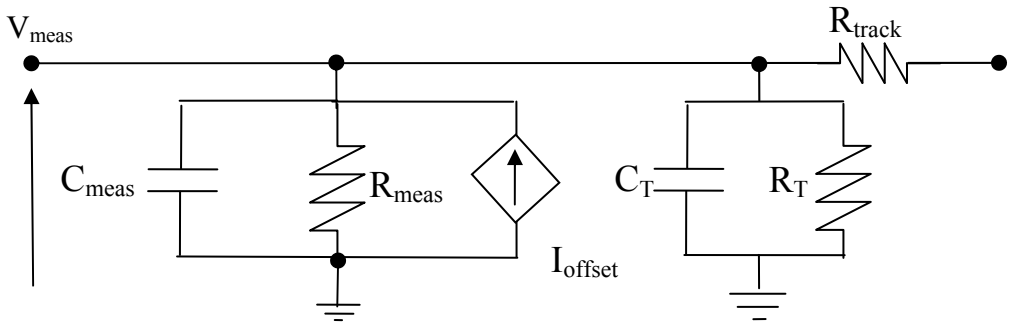

Figure 5.27

Lumped circuit model for input circuit parasitic resistances and capacitances

5.4.2.1 Lumped Shunt Resistance

The lumped shunt resistance R_T was simulated using the Helisoma B19 model presented in table 5.2. The model set R_{seal} of 1 MΩ, electrode diameter of 10µm and R_T was varied between 1 kΩ and 1 GΩ. The effect of varying R_T upon the measured CAP signal is plotted in figure 5.28.

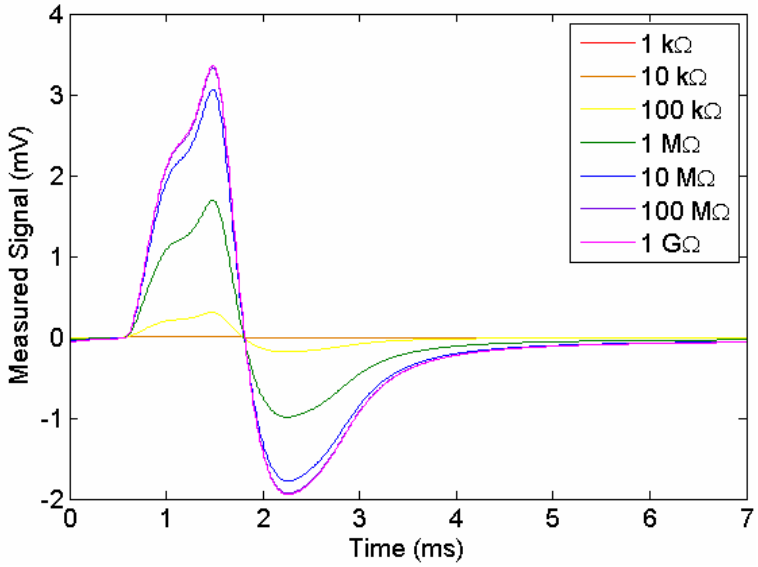

Figure 5.28

Effect of R_L upon signal amplitude

As the source impedance of the CAP is dependent upon the value of R_{seal} rather than the impedance of the membrane, the relationship between R_T and the signal amplitude is applicable to all the neuron models presented in table 5.1.

5.4.3.2 Lumped Shunt Capacitance

The effect of the lumped shunt impedance from the parasitic capacitance was simulated for the B19 model presented in table 5.2. The model had R_{seal} of 1 MΩ, and C_T was varied relative to the total capacitance per unit area of the membrane. The effect of the lumped capacitance C_T upon the CAP signal is plotted in figure 5.29 for a range of values of C_T. Significant distortion occurs at values of parasitic capacitance greater than c_m.

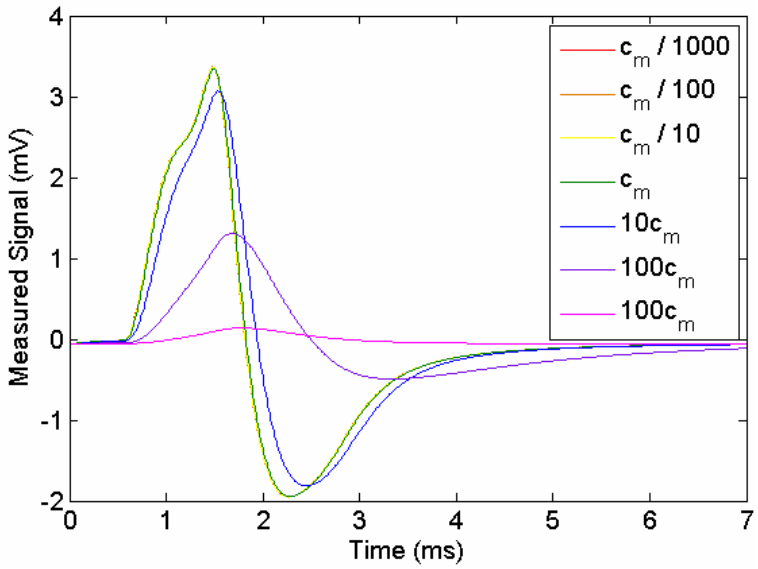

Figure 5.29

Relationship between the amplitude of the measured signal and the total shunt capacitance C_T. C_T is chosen relative to the capacitance per unit area of the membrane to illustrate the dependence upon the membrane area within the cleft.

The capacitance for the surface area of membrane within the cleft is approximated for a soma of a given diameter by:

$$C_m = c_m \cdot \pi \cdot \frac{d_{soma}^{\ 2}}{4} \qquad 5.15$$

For a 20 μm diameter soma, C_m is 3.2 pF. For a 100 μm diameter soma this raises to 79 pF. A lumped parasitic capacitance with value lower than 3.2 pF would therefore be the aim during the design of the measurement circuit to ensure that the neural signals will be free of attenuation and distortion.

The calculations for the parasitic capacitance of the MEA interconnection tracks in section 3.2.1.2 were 3.5 pF per mm of track length. The calculations were based upon common properties of commercial passive MEA devices. Typically the electrode-to-bondpad interconnection tracks are several cm in length. It is inevitable that when using these MEA devices that some signal attenuation and distortion will occur for smaller cleft membrane enclosure areas.
This further highlights the need to boost the signal current and voltage at the measurement source before the signal is carried down the interconnecting tracks.

5.4.2.3 Amplifier Input Bias Current and Input Load Impedance

The non ideal electrical aspects of the amplifier input are the bias current and the input load impedance. The input load impedance may be grouped with the lumped shunt resistance and lumped shunt capacitance as described in the previous subsections since it will present the same signal attenuation and distortion if the input transistor has equivalent values. Table 4.1 lists values for a commercial field effect transistor (FET) amplifier; R_{meas} = 10 TΩ and C_{meas} = 1 pF. From the simulation data presented in figures 5.28 and 5.29 it is unlikely that amplifier input loads with these values will cause appreciable signal attenuation or distortion. Caution may be needed when using amplifiers based upon bipolar technology however as the input resistances are very often much lower than 10 MΩ.

Bias current is more correctly termed leakage current. This is the low level leakage of charge into or out of the FET gate (or bipolar base). The bias current is troublesome for

circuits with high input impedance measuring from high impedance sources such as the system required for neural signal measurements.

The point may be illustrated using the value of i_{bias} presented in table 4.1 and the circuit in figure 5.30. The circuit shows the amplifier input capacitance, resistance and bias current; C_{meas} , R_{meas} and I_{bias} respectively, together with the electrode interface capacitance and resistance C_e and R_e. Considering this small current of 3 pA and the dc interface impedance R_e for a noble metal electrode (calculated from the surface resistivity of 10 $M\Omega cm^2$ for an Au electrode as predicted by Wise [16]).

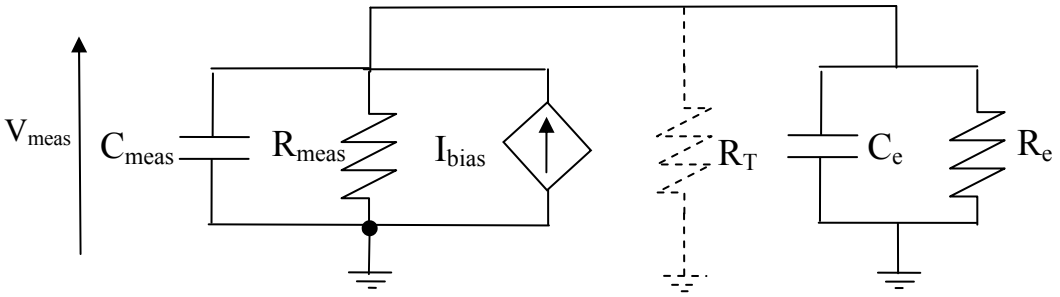

Figure 5.30

The amplifier input circuit together with the electrode circuit and parasitic shunt resistance R_T

For an electrode of 10μm diameter, the value of R_e is 12.7 TΩ; for a 100 μm diameter electrode R_e is 127 GΩ.

If the value of R_T is assumed infinite the dc value of the potential measured at the input of the amplifier V_{meas}, may be calculated by:

$$V_{meas} = I_{bias} \cdot \frac{R_e \cdot R_{meas}}{R_{meas} + R_e} \qquad 5.16$$

As R_{meas} is 10 TΩ, the input offset from a 3 pA current is 0.38 V for the 100 μm diameter electrode and 16.7 V for the 10 μm diameter electrode (this value will in reality never reach such a high value as the interfacial resistance R_e lowers as the interfacial

potential rises). In the SPICE simulation, amplifier saturation is evident using these values.

In most practical situations, the effect of the bias current is negligible due to the parasitic shunt resistances of circuit tracks on PCB and other substrates. The shunt resistance R_T will effectively never be more than several hundred MΩ for standard fibreglass PCB. If R_T is now included with a value of 100 MΩ equation 5.16 becomes:

$$V_{meas} = I_{bias} \cdot \frac{R_e \cdot R_{meas} \cdot R_T}{R_{meas}R_e + R_{meas}R_T + R_eR_T} \approx I_{bias} \cdot R_T \qquad 5.17$$

Equation 5.17 is true when $R_T << R_e$ and $R_T << R_{meas}$.

Giving V_{meas} = 300 μV. This will correspond to an output offset of 300 mV for a 60 dB gain amplifier.

The simplest way to remove the effects of the input offset is to insert a resistor between the inputs of the amplifier and ground. The value of the resister must be large enough to ensure that shunting effects of the source signal do not occur. Section 5.4.2.1 showed that significant amplitude losses occur at shunt resistance values lower than 10 MΩ. Placing a 10 MΩ resistor between the amplifier inputs and ground would reduce the offset down to 30 μV and ensure that the amplitude of CAP signal is not significantly affected. There are also low bias current FET based amplifiers available with bias currents approaching 1 fA that may be more appropriate for measuring neural signals with very small microelectrodes.

Amplifiers based upon bipolar technology may present an input bias current of several nA that presents similar offsets to the FET. As the input impedance of the base is generally as low as several MΩ, the bias current, which is typically three orders of magnitude higher than the FET bias current, causes V_{meas} to be of a similar value.

5.4.3 Input Filter Circuitry

An investigation was carried out into the effects of an input filter circuit upon the simulated CAP signals. Two signals types are presented; one for the fast Helisoma B19b signal , the other is the slow Aplysia MCC signal type to show the range between the fastest and slowest signals as defined by table 4.1. The simulation was set with an R_{seal} of 1 MΩ, a recording electrode diameter of 10μm and the value of R_f was chosen to be 1 GΩ to prevent signal shunting at the input as shown in section 5.4.2.1.

The resulting signal shapes are presented in figure 5.31 for filter cutoff frequencies ranging from 1 Hz to 300 Hz.

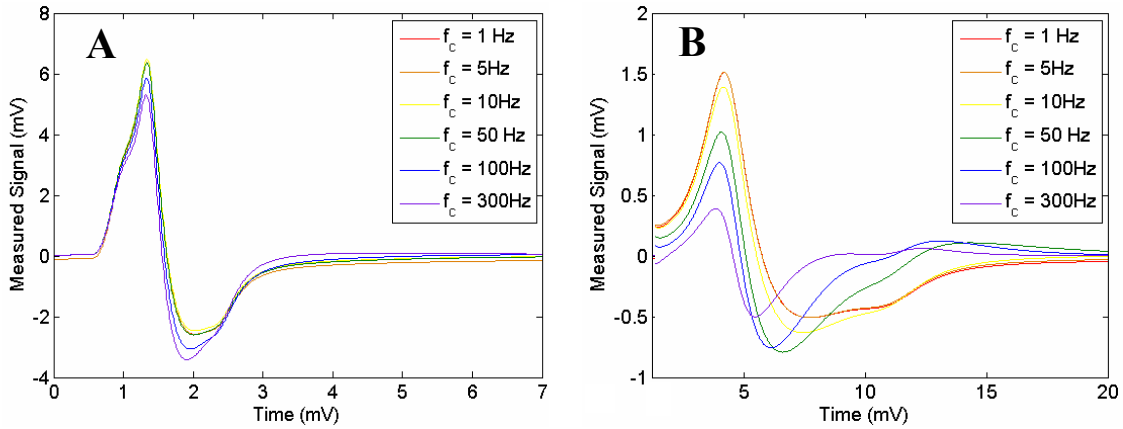

Figure 5.31

Effect of high pass input filter circuit with varying f_c on simulated Helisoma B19 and Aplysia MCC neurons

Considering the Helisoma B19b CAP signal in figure 5.31 A , it is clear that noticeable signal distortion occurs for cutoff frequencies larger than 50Hz; however even with a 300 Hz cutoff frequency the signal is still close to its original form. The distortion reduces the amplitude of the signal, the ratio between the positive and negative spikes and reduces the overall duration of the CAP signal.

The simulated Aplysia MCC CAP signal in figure 5.31 B shows distortion for cutoff frequencies greater than 5 Hz. At 50 Hz the distortion is quite noticeable and affects the amplitude, length and shape of the signal.

5.5 Application of Simulated data to the Design of an Optimised ASIC

The SPICE simulation presented in chapter 4 was used to determine the electrical properties of the extracellular CAP as an electrical signal source. The Hodgkin and Huxley model was expanded to reproduce the CAP and TMAP signal shapes of real extracellular microelectrode recordings. A possible mechanism for the PLS and NLS CAP types was identified. The analysis concentrated upon the PLS as it was the most common signal type in extracellular microelectrode recordings of cultured Helisoma, Hirudo and Aplysia in the source journals for signal fitting. The results from the simulation data is now used to predict the best circuit configuration for an optimised input amplifier.

Important design parameters were identified as:

1. Minimum and maximum input impedance
2. Amplifier bandwidth and signal sampling frequency
3. Gain

5.5.1 Input Impedance

The first parameter is the input impedance of the amplifier. It was shown in section 5.1.3.1 and 5.1.3.2 that the distorted TMAP signal that forms the CAP signal shape is due to the finite electrical resistance of R_{seal} and the capacitance of the membrane C_m. R_{seal} is the result of adhesion between the neuron and the microelectrode array substrate.

The critical value of R_{seal} for TMAP signals was calculated in equation 5.3 and equation 5.7 for NLS and PLS type signals. The critical value of R_{seal} is several orders of magnitude larger than the largest experimentally determined value of R_{seal} (4 MΩ [1]) for cultured neurons. It is proposed that the TMAP signal will always be attenuated and distorted by the cleft coupling to the electrode. The source impedance of the resulting CAP signal is therefore strongly dependent upon the value of R_{seal} rather than the larger

impedance of the membrane capacitance and ion channels within the cleft during a TMAP.

To ensure that the CAP signal is not attenuated by the measurement circuit, the dc input resistance, R_{in} should be calculated relative to the value of R_{seal}.

The required value of R_{in} is calculated according to:

$$V_{meas} = \frac{I_{mem} \cdot R_{in} R_{seal}}{R_{in} + R_{seal}} \qquad 5.17$$

With gain calculated by:

$$G = \frac{V_{meas}}{I_{mem} R_{seal}} = \frac{R_{in}}{R_{in} + R_{seal}} \qquad 5.18$$

If R_{seal} is set to a conservative value of 10 MΩ; to ensure less than 10% attenuation of the CAP, R_{in} must be greater than 100 MΩ. If the value of R_{in} is required to be larger than this an amplifier with a high performance input bias must be chosen. An amplifier with 25 fA input bias, such as the INA 116 would give an input offset of 2.5 μV for the above value of R_{in}.

This value must also be taken into account when designing a high pass input filter circuit to reduce the effect of loading of the source signal by the amplifier.

Similarly, the input capacitance of the amplifier circuit, C_{in} should be lower than the capacitance for the smallest soma diameter of interest. This is calculated in section 5.4.2.2 as 3.2 pF.

It may be difficult to ensure that the values of R_{in} and C_{in} fit the criterion specified above for passive MEA circuits, especially where long interconnection paths are required between the electrode and the amplification circuitry. One solution is to amplify the signal at the source to boost the current and the voltage. A larger signal current would

reduce the attenuation and distortion presented by cabling and raises the signal voltage above potential noise and interference.

5.5.2 Amplifier Bandwidth and Signal Sampling Frequency

Section 5.3.2 shows the normalised spectral power of the slowest and fastest CAP signals produced by the simulation for a wide range of values of R_{seal} and soma diameters. The frequency range of the spectral power is shown in figure 5.32.

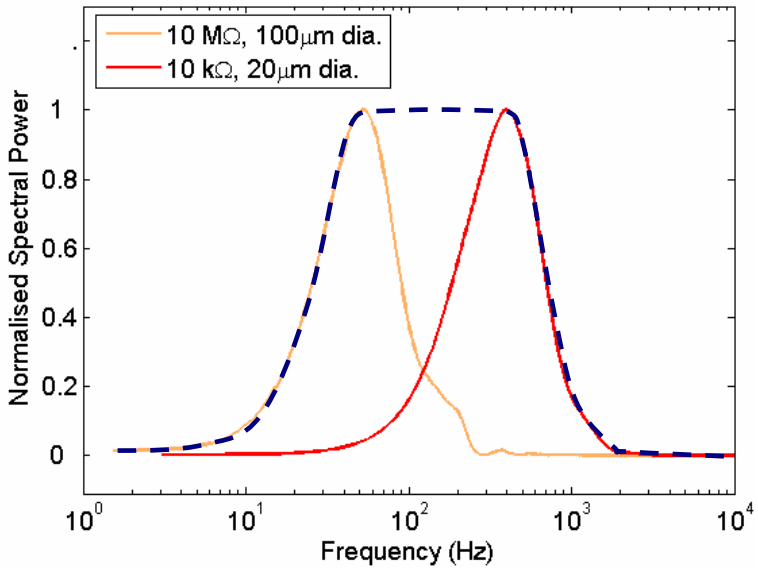

Figure 5.32

Normalised spectral power density of neural signals from SPICE model incorporating fitted values from figure 5.20 and 5.21

Spectral frequency range for all signals simulated in the Spice model is between 2 Hz and 3 kHz. To ensure that all the frequency components of the neural signal are amplified equally the amplifier bandwidth must encompass these values.

It was demonstrated in section 5.4.3 however, that a filter cutoff frequency as high as 50 Hz may be used for the Helisoma B19 type neuron and 10 Hz for the Aplysia MCC type neuron without significant distortion of the CAP signal in each case.

Following the Nyquist sampling theorem, signals should be sampled at a rate of twice the highest frequency component within the CAP signal to ensure that aliasing does not occur and that the frequency of the signal may be faithfully reconstructed after digitisation. The sampling rate should therefore be greater than 6 kHz. This will encompass the spectral frequencies for all of the models fitted in table 5.1.

5.5.3 Amplifier Gain

Section 5.3.1 presented simulation results that demonstrated the relationship between the amplitude of the CAP signal and the value of R_{seal} and the soma diameter for the Helisoma B19 and the Aplysia MCC neuron types.
For values of R_{seal} between 10 kΩ and 1 MΩ the CAP signals from the simulated Helisoma B19 neurons show an amplitude range from 10mV for the 100μm diameter soma at R_{seal} = 1 MΩ to 20 μV for the 20 μm soma at 10 kΩ.

The slower Aplysia MCC neurons show an amplitude range from 4mV for the 100μm diameter soma at R_{seal} = 1 MΩ to 7 μV for the 20 μm soma at 10 kΩ.

A value of R_{seal} between 100 kΩ and 1 MΩ is typically thought of as being a 'good' seal [1, 2, 13]. The cultured Helisoma, Hirudo and Aplysia neurons are approximately 70 μm in diameter. It is proposed that the amplitude range for CAP signals will be between 300 μV and 4mV.

For an amplifier with a 3V output voltage range, a gain of 750 (57dB) would be required to amplify a 4 mV amplitude signal to this level. The 300 μV amplitude signal would be raised to 225 mV. The large spread of signal amplitudes indicates that an amplifier with controllable gain would be useful to prevent saturation from large CAP signals and allow signals to be measured from neurons with poor seals or small diameters.

5.6 Summary

This chapter has presented the simulation results for a novel SPICE based neuron model. The model was used to simulate the extracellular CAP signal to understand its relationship to the TMAP and determine the electrical properties of the signal. The source impedance, amplitude and spectral frequency range were extracted for a range of signal types that were fitted to published CAP data and extrapolated to a range of seal resistances and soma diameters. The results are used in chapter 8 for the design of a compact optimised neural signal amplifier circuit.

Important design parameters determined from the simulation are presented in table 5.6.

Variable	Value	Units
Min R_T	100	MΩ
Max C_T	< 3.2	pF
Max C_{in}	< 1	pF
Max R_{in}	100	MΩ
I_{bias}	<1	pA
Max G_{amp}	57	dB
f_{min}	10	Hz
f_{max}	3	kHz

Table 5.6

Summary of design parameters.

5.7 References

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Chapter 6

Properties of the Electrode Interface for Pt and Au in Physiological Saline.

The results of the *in vitro* extracellular signal modelling presented inn chapter 5 defined the mechanism of the extracellular cleft action potential (CAP). This allowed the source impedance, the signal spectrum and signal amplitude to be estimated for a selection of electrical coupling configurations between the neuron and the electrode.

The properties of the measurement electrode are now considered. This chapter investigates the theoretical and experimentally published electrical properties of the electrode interface for dc and ac modes. These properties are analysed with a view to removing the need for dc decoupling capacitors placed at the front end of neural amplifier circuits; thus reducing the overall integrated circuit area as defined in section 3.4.1. The electrode interface components that are considered in this chapter are presented in figure 6.1. The sections describing each electrical component are labelled to assist the reader in navigating the chapter.

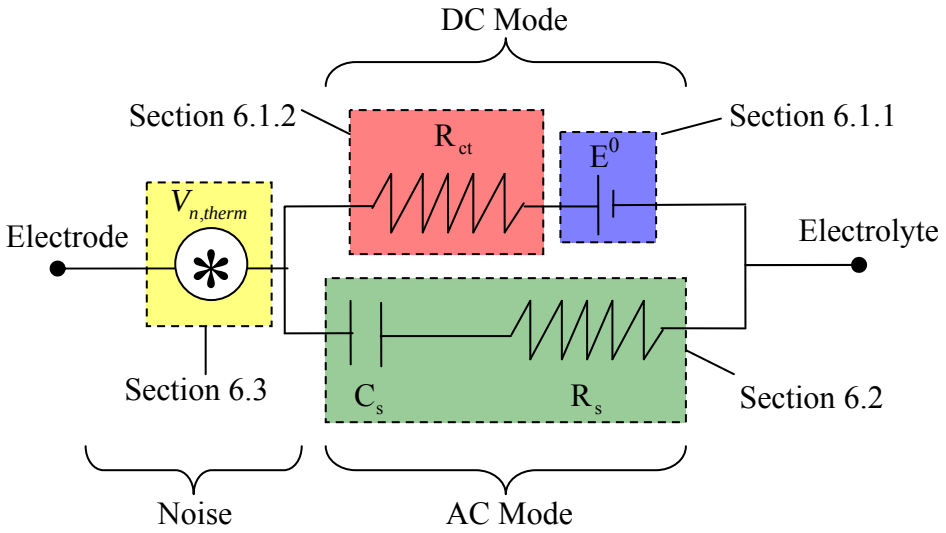

Figure 6.1

Electrical properties of the electrode electrolyte interface

6.1 Characterising the DC Electrical Properties of Au and Pt Electrodes in Physiological Saline

The phase boundary between the aqueous electrolytic phase of the extracellular fluid and the solid state of the noble metal electrode presents a non linear electrical signal pathway between the neuron and integrated measurement circuitry. Neural signals are propagated by ionic charge carriers within a liquid material. Metal electrodes and electronic circuits transfer signals using electrons. The ionic charge cannot pass through the crystal structure of the metal and electrons cannot move freely between the solid and liquid phase.

The surface of the immersed electrode is required to transduce the ionic signals into electronic signals before the neural signal can be measured. The interface introduces several non ideal properties to the signal path between the neuron and the measurement circuit. These properties can be split into two modes; ac and dc.

The dc mode of the interface presents a voltage offset known as the equilibrium half cell potential. This is several orders of magnitude larger than the amplitude of the CAP and must be removed before amplification. For noble metals such as Pt and Au, the dc mode also presents a very large dc resistance.

The ac mode of the interface presents a non-ideal capacitance that is dependent on physical properties of the electrode material. The value of this capacitance is inversely proportional to frequency and can be described as a constant phase element (CPE). The ac mode is discussed in section 6.2.

6.1.1 Electrode – Electrolyte Interface Potential

Metallic electrodes may interact with aqueous solutions in several ways depending upon the reactivity of the metal within the electrolyte and the ionic composition of the electrolyte. An ideal biocompatible electrode is one that will partake in a surface electrochemical reaction without disassociation of mass and the resulting formation of free chemical products within the electrolyte. This is necessary to ensure a satisfactory electrode lifetime and prevent the formation of salts that may be toxic to the organism. For this reason, only noble metals such as Pt and Au are considered here. These metals are highly stable within a saline solution, even when they are subjected to an externally applied potential exceeding the electrolysis window of water to create stimulus currents for neural excitation.

Pt and Au electrodes do not react with to the ionic and solvent composition of the electrolyte. The only common particle between the two phases is the electron, and charge transfer will ideally only take place with the oxidation and reduction of the surface water molecules.

When an electrode is placed into an aqueous electrolyte, there is a difference in charge density between the two materials. There is also a difference between the electron work function of the metal and the equivalent electron energy of the electrolyte. The difference in energy is the basis of the equilibrium half cell potential.

The interface potential is defined by [1]:

$$E^0 = \frac{\Phi^M}{F} - \chi^S - V_{pzc} \qquad 6.2$$

where:

Φ_M is the work function of the metal

χ^S is the surface potential of the interface due to the net orientation of surface H_2O dipoles

F is the Faraday constant

V_{pzc} is the potential of zero charge for a given electrode immersed in a given solution

The high work function of the noble metals causes a positive potential to occur at the interface; the metal will donate an electron to the interface rather than accept one. Less stable metals with a lower work function than the liquid phase will readily accept electrons from ions at the interface to form a salt. The work function will vary for different metallic species, surface conditions and lattice structures at the interface. Changes in the surface of the electrode, such as the specific adsorption ions have been found to affect the average work function of the material and may modulate the half cell potential.

The half cell potential is defined by the symbol E^0. To be used correctly, the term half cell potential should apply only to an electrode immersed in a solution containing the dissolved ions of the electrode material. It is however often used to describe the open circuit potential (OCP) at equilibrium of noble metal electrodes that do not comply with this definition. The OCP is often also referred to as the reversible cell voltage (RCV). For the remainder of this thesis the symbol E^0 will be used to describe the OCP of the noble metal electrodes in saline.

Measured values of E^0 for Pt and Au electrodes in physiological saline have been published in the literature. Direct open circuit measurements were performed by Franks et al. and Najafi et al. The equilibrium potential of Pt was stated by Franks et al. [2] as: 318 mV ± 37 mV relative to a saturated calomel electrode reference (SCE) indicating a

value of 560 mV (SHE). Najafi et al.[3] published electrode potentials for Au as 216 mV ± 60 mV (-25 mV ± 60 mV relative to the SCE).

In an alternative method performed by Chou, Frenkel and Ovadia [4] using three electrode linear scan voltammetry (LSV), the standard electrode potentials of Pt and Au electrodes was calculated to be -166 mV ± 54 mV and -166 mV ± 19 mV respectively. The experiments performed in this study cycled the potential around a zero current potential described as a 'null current' point that defined the standard electrode potential.

From these comparisons there appears to be some variation between the measured values of E^0 for Au and Pt electrodes. This is not a surprising phenomenon if one considers that it is likely that electrode fabrication, preparation and measurement circuitry may well have varied between authors. The value of E^0 may vary for many reasons, including variations in the dominant surface crystal face orientation [5, 6] resulting from electrode formation, e.g. metal vapour deposition, drawn wire, etc.

The value of E^0 for Au and Pt electrodes placed within solutions that do not contain an abundance of chemical species with which the metal will react (i.e. providing a sustained charge transfer reaction as in a battery cell) is highly dependent upon conditions at the electrode surface and the input impedance of the measurement circuit. Surface variation is inevitable, even in the most stringent clean room fabrication conditions and it is similarly inevitable that variations will occur at the surface through time as such electrodes are used.

The value of E^0 potential for a Pt or Au electrode is typically several hundred millivolts. The amplitude of neural signals has been shown in chapter 5 to vary between tens of microvolts to millivolts and requires high gain amplification to bring the voltage of the signal to useful amplitude. The equilibrium potential presents a problem to the direct measurement of the signal as it will be amplified by the same gain. If the equilibrium potential is not removed the output of the measurement circuitry will be driven beyond its output voltage range, saturating the amplifier. Many researchers have used decoupling capacitors and low frequency continuous time filters at the front end of the circuitry to address this challenge.

6.1.2 Charge Transfer Reactions

For the noble metals Pt and Au in physiological saline, sustained charge transfer is only possible with the oxidation or reduction of water molecules at the surface. Charge transfer that is limited in time and current may occur with the 'water window' due to adsorption of dissolved H^+, OH^- , or Cl^- ions at the surface or oxidation of the electrode surface.

6.1.3 Identification of Reactions and Sorptions at Pt and Au Electrodes in Physiological Saline within the Water Window

Brummer, Turner and Loeb [7,8,9] used chronopotentiommetry to identify reversible, biologically safe charge transfer reactions in physiologically comparable aqueous solutions. This method was adopted to identify the double layer charging, sorption and charge transfer reactions occurring at the Pt and Au electrode interface in physiological saline. Figures 6.2 and 6.3 show typical chronopotentiometric results for Pt and Au wire electrodes in saline at a constant current density of 100 $\mu A/cm^2$. The measurements were made using a three electrode technique, using an Ag/AgCl reference electrode on a Perkin – Elmer VMP potentiostat. The electrochemical reactions and sorptions are described relative to the literature in section 6.1.3.2 and 6.1.3.3 for Pt and Au respectively. The reactions and potential ranges for both metals are summarised in figure 6.4.

The results presented in this section closely follow the shape and form in time of similar experiments presented in earlier work by Hickling for Pt and Au [10, 11] respectively and Brummer et al. for Pt [7, 8].

Hickling presented data recorded on plate from an anodic +10 mA/cm^2 constant current density within aqueous acidic (1M H_2SO_4), neutral (0.2M KH_2PO_4 + 0.2M Na_2HPO_4 at pH 6.8) and alkali solution (1M KOH) to ascertain the mechanisms of the electrode reactions involved. Hickling noted that the final potential for water oxidation is weakly proportional to the applied current density. Final potentials for Pt in neutral solution

were similar to those shown in figure 6.2 at 1.5 V (SHE). This rose to 1.75 V for acid and lowered to 1.0 V for alkali. Final potentials for Au in neutral solution were similar to those shown in figure 6.3 at 1.75 V (SHE). In acid the potential rose to 2.0 V and in alkali it lowered to 1.3 V.

Brummer et al. used current densities of 33 mA/cm^2 [7] and 100 mA/cm^2 [8] followed by various reversal current densities in acidic (1M $HClO_4$) and buffered saline solutions (0.13 NaCl buffered at pH 7.3 with HCO_3^-/CO_2). In this work the final potential of water oxidation was shown to be approximately +1.25 V relative to the reversible hydrogen electrode (RHE) for a 33 mA/cm^2 current density. The RHE is equivalent to the SHE to within 5 mV. For 100 mA/cm^2 current density the final potential was raised to 1.9 V (RHE). This corresponds to the findings of Hickling and indicates that the proportionality between current density and final potential becomes much stronger for current densities above 33 mA/cm^2.

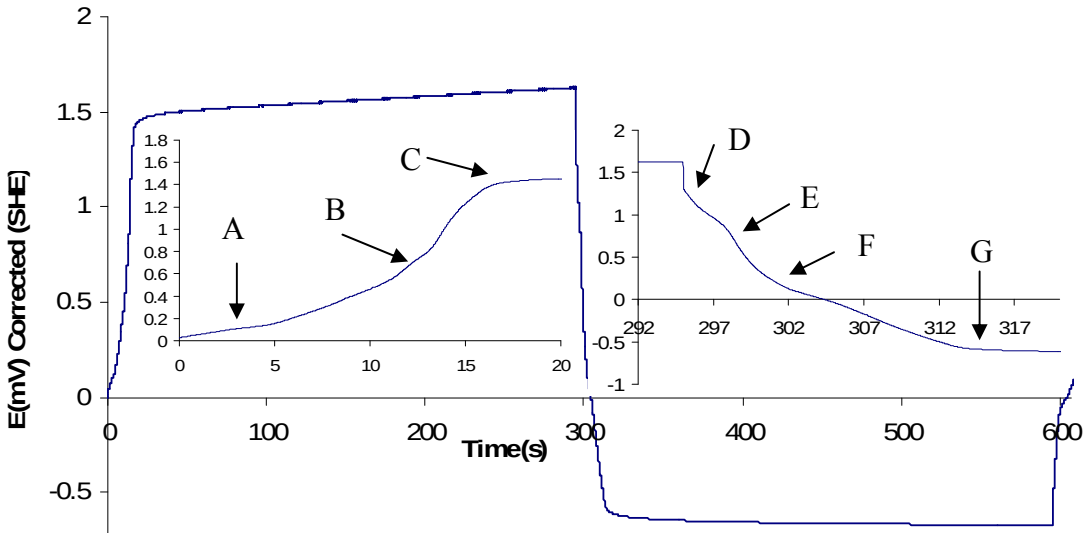

Figure 6.2

Chronopotentiometric response of Pt electrode at +/-100 μA/cm^2 in physiological saline solution

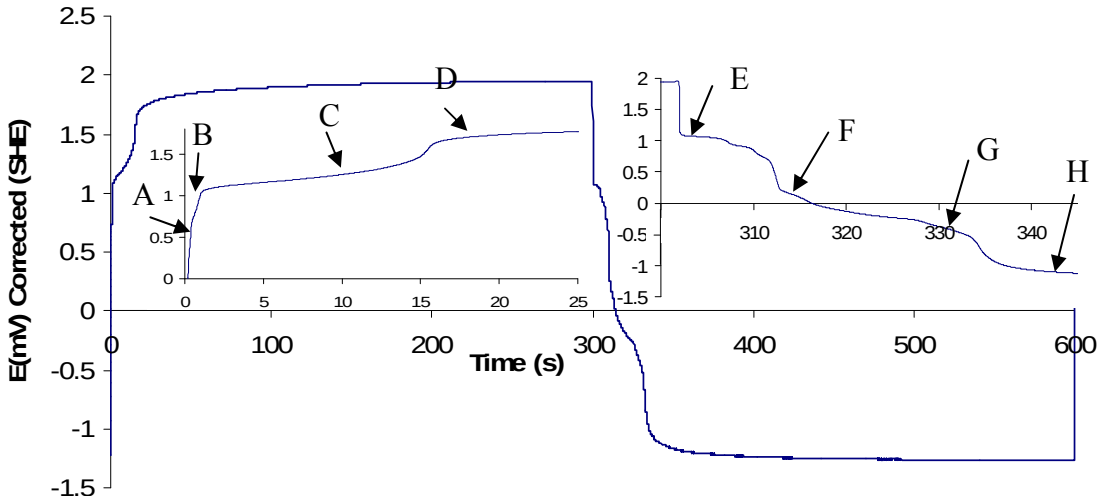

Figure 6.3

Chronopotentiometric response of Au electrode at +/-100 μA/cm^2 in physiological saline solution

6.1.3.1 Charge Transfer Regions for Pt

Referring to figure 6.2; point A, between 0 V – 0.2 V, is a capacitive slope which suggests that the charging of the double layer occurs in this region; this being due to the orientation of H_20 to face the negative pole to the electrode surface, and diffuse layer charging by attracting Cl^- ions closer to the electrode. It is also favourable in this region for de-sorption of H-atoms. This has been defined to occur between 0 V - 0.4 V by Loeb [9]. The capacitance will therefore be a combination of both processes.

Point B, between 0.2 V - 0.6 V, draws out of the reversible sorption region of the electrode as defined by Loeb. This region, defined as between 0.35 V - 0.6 V by Gilroy and Conway [12] will correspond to further double layer and diffuse layer charging and much less, if any further desorption of plated H-atoms. It is likely that Cl^- adsorption occurs in this region between 0.31 V < E < 0.66 V as detailed by Garcia-Araez et al. [13] and Hackerman et al. [14]. This process has been shown to be pH independent and is applicable to pH neutral physiological saline solution. Cl^- adsorption inhibits the adsorption of OH^- that will also occur in this region [15].

The gradient steadily increases after 0.6 V indicating that the double and diffuse layer is close to saturation. As the working electrode potential approaches 1 V it is possible that platinum oxidation occurs [9]:

$$PtO + 2H^+ + 2e^- \leftrightarrow Pt + H_2O \qquad (0.98\ V) \qquad 6.1$$

However this process is known to be inhibited in Cl^- containing solutions [16, 8]:

Point C, at 1.4 V represents a constant charge transfer reaction. The electrode now has sufficient potential to overcome the energy barrier at the interface and oxidise the neighbouring water molecules, evolving O_2 gas:

$$O_2(g) + 4H^+ + 4e^- \leftrightarrow 2H_2O \qquad (1.23\ V) \qquad 6.2$$

Following point C a slight slope is present (1.4 - 1.6) in the constant charge transfer region. This is most likely caused by ohmic losses within the electrolyte from diffusion and drift of reacting species that maintain the reaction [9] and surface saturation of O deposited on the platinum surface before evolution [10, 16].

On reversal of the current to cathodic operation at -100 $\mu A/cm^2$; point D follows an IR drop corresponding to recovery from the ohmic loss, presenting a capacitive slope from double layer relaxation and charging from the repulsion of Cl^- ions between 1.3 V and 0.9 V. Desorption of Cl^- will also begin in this region.

Point E presents a steeper capacitive slope indicating the saturation of double layer charging and desorption of adsorbed Cl^-. This occurs between 0.9 V and 0.4 V. In this region, reduction of surface oxide is possible in the reversal of reaction 7.5 as H^+ drifts to the electrode surface.

Point F is a capacitive de-charging region between 0.4 V – 0 V from re-plating of H-atoms at the electrode surface.

Beyond point F, as the working electrode potential drops to below 0 V, the density of H-atoms will increase and H_2 gas will form and evolve:

$$2H^+ + 2e^- \leftrightarrow H_2 \qquad (0.0\ V) \qquad 6.3$$

H-atom plating, formation and evolution of H_2 gas will continue presenting a mix of capacitive and real charge transfer. The electrode potential remains constant at - 0.7 V to - 0.8 V, at which the saline solution visibly evolves gas bubbles, indicating that reduction of H_2O is occurring.

These measurements indicate that there is no sustained charge transfer at the Pt electrode within the water window. At the Pt equilibrium potential measured by Franks, as described in section 6.1.1, there will be no direct charge transfer. In the region around 0.56 V (SHE) the electrode will be capacitive. From this evidence it is proposed that the small signal capacitance around this value will be due to double layer charging and sorption of Cl^-.

6.1.3.2 Charge Transfer Reactions for Au

Referring to figure 6.3, for an equal current density, Au electrodes present a lower level of capacitve sorption regions when compared to Pt. Au has much sharper voltage curves in time.

Point A shows a fast double layer charging region devoid of the slow charging capacitance present at the Pt electrode within the H-atom de-sorption potential range. This region steps from 0 V to 0.6 V in less than 0.1 s. The evidence indicates that for Au the capacitive properties of the electrode in this region are due to double layer charging with much lower H-atom sorption than demonstrated for platinum. The literature states that there may be some OH- adsorption in this region (between 0 V – 0.2 V), but this process has been identified to be inhibited aqueous solutions containing Cl^- [17]. Blizerack et al. have shown that OH- adsorption may occur between 0.2 V – 0.7 V in parallel to double layer charging in both acidic and alkaline solutions [18]. It was also shown in their work that the ‘pseudo-capacitance’ contribution from Cl^- increases

substantially with the addition of a small (10^{-6} M) concentration of Cl^- to a Cl^- free solution.

Point B shows a decrease in the charging slope between 0.6 V and 1.1 V. It is likely that this results from the increasing adsorption of Cl^- within these potentials [17]. The slope is much steeper than that in the same region for Pt indicating that Cl^- sorption is much less pronounced. Sorption of OH- is possible in this region leading to the reaction:

$$Au - OH_{ads} + e^- \leftrightarrow Au + OH^- \qquad (0\ V - 0.2\ V) \qquad 6.4$$

but it will be limited by the inhibiting Cl^-.

Point C shows a time limited charge transfer reaction between 1.1 V and 1.4 V. Reactions of the adsorbed Cl^- with the Au surface to form Aurous-Chlorides are possible at these potentials, however there was no physical evidence of solution discolouration to verify this.

Another possible reaction is:

$$AuO + H^+ + e^- \leftrightarrow Au - OH_{ads} \qquad 6.5$$

However, it has been proposed that OH^- adsorption is inhibited in saline. The most likely cause of this region's upward slope is the saturation of the electrode with adsorbed O before evolution occurs and the subsequent kinetics of oxygen evolution away from the electrode as reaction 6.2 progresses.
Point D at 1.5 V – 1.7 V shows a similar form to the ohmic loss region of the Pt electrode that is attributed in this case to oxygen saturation at the electrode.

Upon current reversal to cathodic current a large ohmic drop occurs, dropping the electrode potential quickly down to 1.1 V.

Point E shows a charge transfer region between 1.1 V and 0.6 V that is most likely due to de-sorption of Cl^-. It is also possible that oxides that may have been formed around

reaction 6.2 are being reduced. OH^- de-sorption and double layer charging are also possible in this region.

Point F is between 0.2 V and -0.1 V. This region follows a sharp drop from 0.6 V. The slope presented in this region looks similar to that presented by point F in the Pt curve and may indicate that some oxidation, double layer charging and possibly small levels of H^+ adsorption are occurring.

Points G and H are between -0.1 V and -1 V and are separated by a drop that mirrors the step between points C and D. The region within point G looks similar to point G for the platinum curve, indicating that it is due to reduction of H^+ at the electrode and evolution of H_2.

The step between G and H indicates that another reaction is occurring at H in parallel to H_2 evolution. This reaction is likely to be the reduction of water and subsequent additional H_2 evolution.

$$2H^2O + 2e^- \leftrightarrow H_2(g) + 2OH^- \qquad \text{(-0.828 V)} \qquad 6.6$$

The increased potential at Au within the H-atom sorption region identified for Pt would be necessary to maintain the charge transfer rate if Au had a much reduced ability to adsorb H^+.

These measurements indicate that Au does not have sustained charge transfer paths within the water window. Within the water window the electrode behaves capacitively, but demonstrates much less capacitance than Pt for positive electrode potentials relative to the SHE. At the equilibrium potential of 0.25 V (SHE) proposed by Najafi there will be no direct charge transfer. It is proposed that capacitance will be dominated by the double layer charging.

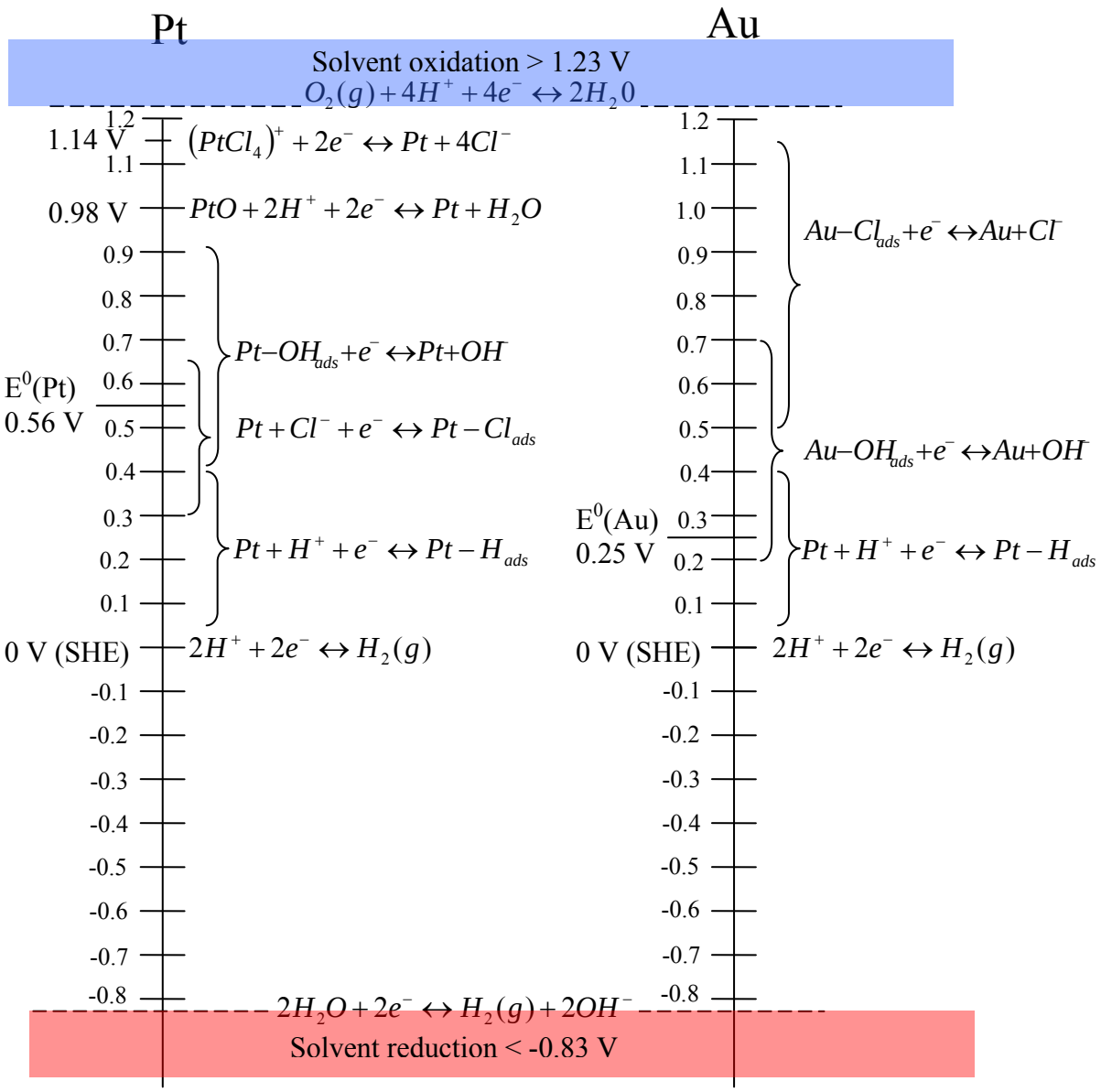

Figure 6.4

Table of electrochemical reactions and sorptions in physiological saline

6.1.4 DC Charge Transfer Resistance at Equilibrium

Section 6.1.3 provided a detailed analysis of the capacitive and resistive charge transfer mechanisms occurring at the Pt and Au interface with physiological saline. It was clear from the literature and the chronopotentiometric analysis that in saline the main charge transfer reaction within the water window at the Pt interface is H^+ sorption and evolution

at potentials between 0 V -0.4 V and Cl^- sorption at 0.3 V - 0.65 V. For potentials lower than 0 V there is insufficient free H^+ in the cell to supply constant charge transfer and insufficient potential to drive H_2 evolution. Charge transfer of H^+ will be limited by surface saturation of the adsorbed H^+. Charge transfer is predominantly capacitive and due to charging of the electrode double layer and sorption. At large overpotentials, approaching 1.23 V or -0.7 V, relative to the SHE, charge transfer may occur by oxidation of H_2O surface and H+ atom reduction, evolving H_2, respectively.

Similarly with Au, charge transfer is capacitive with a much lower apparent capacitance due to a reduced tendency for Au to adsorb H^+ and Cl^-. Sustained electronic charge transfer occurs at overpotentials of 1.6 V and -1.1 V. There is theoretically an infinite real dc charge transfer resistance at the interface, but some sustained charge transfer, however small, must occur to sustain the equilibrium potential.

Measurements of the charge transfer resistance of Pt and Au electrodes in phosphate-buffered saline were published by Wise et al. [19]. The published V-I plot is shown in figure 6.5. No information was given in this work regarding the time between measurements or the measurement system used; therefore the results are to be used with caution as capacitive sorption effects may be included in the measurements.

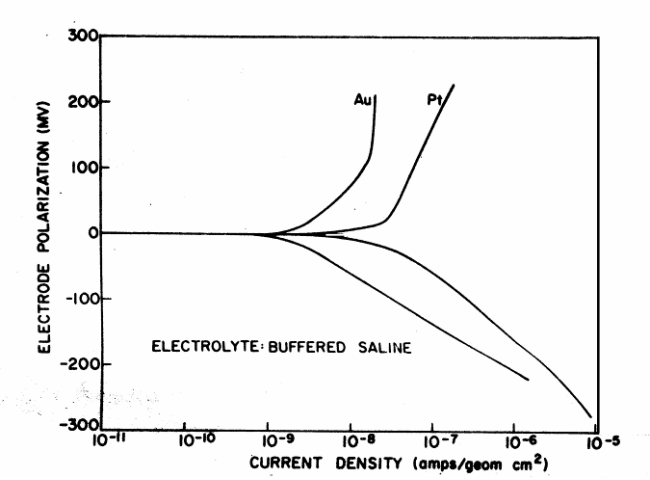

Figure 6.5

V-I plot for Pt and Au electrodes in phosphate buffered physiological saline; adapted from Wise et al. [19]

Considering the linear regions of the Pt and Au curves between ± 100 mV electrode polarisation one can extrapolate values of 1.5 $M\Omega cm^2$ (+ve) and 5.0 $M\Omega cm^2$ (-ve) for Pt and 10 $M\Omega cm^2$ (+ve) and 7.5 $M\Omega cm^2$ (-ve) for Au.

Wise used these results to estimate the equilibrium current density of Pt and Au electrodes I_0 using the small signal approximation of the Butler-Volmer equation:

$$r_{ct} = \frac{RT}{i_0 zF} \qquad 6.7$$

For Pt and Au in physiological saline the value of i_0 was experimentally defined to be approximately 1 x 10^{-9} A/cm^2 for small signals conforming to the Butler-Volmer low field criteria. As correct use of the Butler-Volmer equation requires that the reaction is not diffusion limited this result should be considered cautiously.

6.2 Characterising the AC Electrical Properties of Au and Pt Electrodes in Physiological Saline

The inability of the electrode and the electrolyte to exchange their fundamental charge carriers inhibits dc conduction. However capacitive ac conduction is possible across the phase boundary as free charge movement occurs in both phases and the phase boundary. This is augmented by sorption of ions on the electrode surface. Sorption is a surface limited charge transfer reaction with specific ions that is measured electrically as a capacitance. The capacitance is not constant with frequency in contrast to linear circuit capacitors. This has been observed experimentally. It has been proposed that the frequency dependence is caused by the kinetics of adsorption. Other research has concluded that the frequency dependence is entirely caused by the surface roughness of the interface with lateral charge transfer at the surface producing branched RC ladder networks. It is expected that the frequency dependence will be dependent on both these factors especially with metals that display large sorption capacitances, e.g. Pt in saline. As capacitance is by definition frequency invariant, the interfacial capacitance of the electrode-electrolyte interface has at times been described as a ‘pseudo-capacitance’ in the literature.

The following sections present the theory and a review of the published material relevant to the electrical properties of Pt and Au electrodes in physiological saline.

6.2.1 The Double Layer

The charge barrier and electrochemical polarisation effects at the interface cause the formation of a somewhat predictable structure of the solvent dipoles at the electrode surface. This structure was termed the double layer due to the original concepts of charge arrangement at the surface of the electrode. Sections 6.2.2 to 6.2.4 describe the theories developed to describe the interface capacitance.

6.2.2 The Helmholtz Double Layer

The double layer model was first considered by Helmholtz who calculated the resulting capacitance, C_{dl} as:

$$C_{dl} = \frac{\varepsilon_r \varepsilon_0}{x_H} \qquad 6.8$$

where x_H is the distance of closest approach (approximately 2.8 Å) between the dissimilar charge carriers. The relative permeability ε_r is much lower than that for bulk saline due to the surface arrangement of the dipoles and is considered to have a value of around 6. Typically values of C_{dl} are between 10 – 20 μF cm^{-2}.

The limitations of this first model were that the capacitance value remains independent of applied electrode potential and ionic concentrations.

6.2.3 The Gouy-Chapman Model

This model describes the capacitance of the aqueous interface in terms of the applied potential and electrolytic concentration. The capacitance was considered as a diffuse layer of solvent and ionic particles where the distance between hypothetical capacitor plates is proportional to the applied potential to the electrode and the concentration of ionic species in the bulk. Boltzmann's law is used in the derivation to describe the distribution of the ionic species from the electrode. This is combined with the Poisson equation to relate electrode potential to charge distribution in the electrolyte.

The general solution for the Gouy-Chapman capacitance, C_d is:

$$C_d = \left(\frac{2z^2 e^2 \varepsilon_r \varepsilon_0 n_i^0}{k_B T} \right)^{\frac{1}{2}} \cosh\left(\frac{ze\Delta E_0}{2k_B T} \right) \qquad 6.9$$

where,
n^0_i is the ionic concentration of physiological saline
z is the valence of the participating ionic species
e is the unit of electronic charge
k_B is Boltzmann's constant
ΔE_0 is the variation from the equilibrium potential

The model provides a good approximation of the capacitive effect of the diffuse layers for dilute aqueous solutions with electrodes maintained around their equilibrium potential.

Values of the Gouy-Chapman capacitance are tens of microfarads per cm² with the actual value dependent upon the ionic concentration and the electrode potential.

6.2.4 The Stern Model

The Stern model unifies the Helmholtz and Gouy-Chapman models, considering a system composed of a rigid double layer structure of water dipoles at the interface combined with a diffuse ionic charge capacity that spans the region between the outer layer and the bulk solution.

The model is defined simply by the series circuit connection of the Helmholtz capacitance and the Gouy-Chapman capacitance giving the Stern capacitance, C_{St} as:

$$C_{St} = \frac{C_{dl}C_d}{C_{dl} + C_d} \qquad 6.10$$

Upon analysis of this model, using the descriptions of C_{dl} and C_d from 6.2.3 and 6.2.4, if the solution is very dilute or the electrode potential is close to equilibrium, then C_{dl} is much greater than C_d, giving:

$$C_{St} \approx C_d \qquad 6.11$$

Conversely, when the solution is concentrated or the electrode potential is far from equilibrium, C_{dl} is much less than C_d giving:

$$C_{St} \approx C_{dl} \qquad 6.12$$

Equations 6.11 and 6.12 summarise the assumptions of this model in that the charge ordering potential drop from the electrode into the electrolyte becomes more abrupt for high ionic concentrations and large variations upon the equilibrium potential, thus appearing more like a compact Helmholtz double layer.

The Stern capacitance is often very close to the value predicted by the Helmholtz or Gouy-Chapman capacitances for ionic concentrations such as found in physiological saline. The value of the Stern capacitance often ranges from 10-15 μF/cm²

6.2.5 Frequency Dependence of the Interfacial Impedance

Static field descriptions of the interface impedance provide a good physical description of the mechanisms behind the double and diffuse layers. However experimental analysis of the interface for metals within aqueous solutions has shown that the capacitance values are inversely proportional to frequency and also demonstrate resistive losses with related frequency dependence.

This phenomenon has been recognised for over a century, beginning with the investigations and surface diffusion models of Warburg [20]. This characterisation was later augmented by Fricke to include data for different metals over a larger frequency range [21]. The interface impedance was described empirically for any given conductive material immersed within an aqueous electrolyte, as:

$$C_s \propto f^{-m}; \qquad R_s \propto f^{-(1-m)} \quad \text{and} \quad \delta = \frac{m\pi}{2} \tag{6.13a}$$

where m is a fractional constant between 0 and 1, R_s and C_s is the polarisation resistance and capacitance and δ is the phase angle between measured real and reactive components and is given by:

$$\tan(\delta) = \left(\frac{1}{\omega C_s R_s}\right) \tag{6.13b}$$

The phase angle for the impedance indicates the ratio between the real resistive component of the series equivalent circuit shown in figure 6.1 and the imaginary capacitive component. This defines the deviation of the interface properties from that of an ideal capacitor. A phase of – π/2 or - 90° would indicate pure capacitance without resistive losses. A phase of 0° indicates a purely resistive interface. A linear circuit element capacitor would display a phase very close to - 90°. This description of the electrode impedance is commonly referred to as Fricke's Law or the constant phase law and is derived empirically from observation of the interface as a series resistance and capacitance that increase as the frequency is lowered. This constant phase angle is therefore between - 90° and 0°.

Fricke's law was developed by Cole [39] to describe the ac conductance of biological materials. The impedance of the frequency dependent series circuit formed by R_s and C_s was written as:

$$Z_p = \frac{b}{A(j\omega)^{\alpha}} \qquad 6.14$$

Where b is a constant, ω is the angular frequency and α is a constant defining the slope of the impedance relative to frequency. The value of α is equal to – (1-m).

Cole related this impedance to the charging of the material by a constant current. As a material with infinite impedance at dc is charged by a constant current, the resistance to the current R_s increases with time and the capacitive reactance X_c lowers. This is due to charge saturation of the dielectric material. Both R_s and X_c are dependent upon the electrical properties of the material and to one another. The relationship is characterised empirically by the value of α and the constant phase angle.

The electrical energy required to charge the material is reflected in the phase of the impedance which may be used to determine the ratio between R_s and X_s and thus a material exhibiting high electrical losses relative to capacitive charging will have a phase close to zero. A material exhibiting small electrical losses relative to capacitive charging will have a phase of - 90°. As the frequency of the ac measurement signal is increased the interface has less time to charge and discharge causing a lower apparent capacitance and resistance; it is easier for the material to partially charge at a higher frequency than a lower frequency due to the overall charging current supplied in each ac cycle.

The frequency dependence of the electrode-electrolyte interface has been measured by many authors for many materials over the last century in an attempt to characterise the electrical response and define the underlying physical mechanisms.

The work of Graham in 1946 [22] and 1952 [23] demonstrated an absence of frequency dependence with the dropping mercury electrode that strongly indicated a material or material surface dependency upon the frequency response. Other theories developed

regarding the assumption that frequency dependence of impedance may be dependent on the roughness of the electrode, leading to a number of later models based on fractal surface descriptions. This line of theory was reinforced by the work of Scheider in 1977 [24] that demonstrated that in irregular surfaces, lateral charge transfer is the major cause of frequency dependence. Scheider showed that for electrodeposited and machined Au electrodes, the roughness of the surface results in frequency dependent losses that are comparable to infinite branched RC ladder networks. Scheider believed that this ruled out sorption due to the lack of correlation between frequency dispersion and ionic concentration.

Bokris and Conway, in the late 1960's [25] disagreed with the earlier conclusions of Graham, stating surface conditions of solid electrodes are also more prone to adsorption effects than mercury, and theorised that surface structures of H^2O molecules may by responsible for the apparent surface roughness effects.

Much more recently, the work of Bates and Chu 1992 [26, 27] has indicated that the frequency dependence of an electrode may not be solely attributed to the average surface roughness, but a combination of electrode topography and diffusion effects, whereby the locally distributed ions within the solution accumulate quickly at the edges of large surface protrusions, screening deeper regions of the electrode surface.

In each case the frequency dependence, whether caused by sorption or transmission line losses from lateral charge transfer, may be modelled by Fricke's Law or the Cole impedance Z_p. The phase of the measured impedance of the electrode interface indicates the resistive losses occurring at a given frequency due to the underlying mechanism for the interfacial impedance.

6.2.6 Comparison of Published Data for AC Electrical Properties of Au and Pt in Physiological Saline Solutions

A selection of published data was gathered from the work of several groups to compare the values of the interfacial capacitance, resistance and the m parameter defined by Fricke's Law. The data was standardised to capacitance per unit area (c_s) and surface

resistivity cm^2 (r_s) to allow direct comparison between the differing electrode surface areas used in the measurements.

6.2.6.1 Collected Published Data

The relationship between r_s, c_s and the frequency f is characterised by:

$$c_s = c_0 f^{-m} \quad 6.15$$

$$r_s = r_0 f^{-n} \quad 6.16$$

Where n should be equal to (1-m) to conform to Fricke's Law.

The gathered data is presented in table 6.1 for Pt and table 6.2 for Au

Author	c_0 $\left(\frac{\mu F \cdot \sqrt[m]{Hz}}{cm^2}\right)$	r_0 $\left(k\Omega \cdot \sqrt[(1-m)]{Hz} \cdot cm^2\right)$	m	n	Range (Hz)	Roughness
Mirtaheri et al. [28]	65.4	2.716	0.67	0.44	10 m – 1.0	<10µm
	56.5	3.171	0.3	0.7	1.0 – 1 k	<10µm
De Boer et al. [29]	387.3	0.133	0.18	0.82	10 – 10 k	unpolished
Liu et al. [30]	-	0.266	0.17	0.83	20 -100 k	diamond saw cut
Onaral et al. [31]	585	1.587	1	0.349	10 m – 1.0	microscopic
	154	1.493.4	0.41	0.96	10 – 1 k	microscopic
Schwan et al. [32]	380	0.260	0.384	0.54	10 m – 200	unknown

Table 6.1

Values of c_0, r_0, m and n from published data for Pt electrodes

Author	c_0 $\left(\frac{\mu F \cdot \sqrt[m]{Hz}}{cm^2}\right)$	r_0 $\left(k\Omega \cdot \sqrt[(1-m)]{Hz} \cdot cm^2\right)$	m	n	Range (Hz)	Roughness
Mirtaheri et al [28]	70.9	0.675	0.389	0.85	10m - 1	< 10 μm
	69.5	-	0.193	-	1 – 1k	< 10 μm
Wise. [33]	44.97	0.560	0.1	0.9	10 – 10k	Semi bright (electroplated)

Table 6.2

Values of c_0, r_0, m and n from published data for Au electrodes

6.2.6.2 Discussion

The electrode-electrolyte interface for Pt and Au electrodes presents a large capacitance per unit area that is frequency dependent within the spectrum of extracellular neural signals. For the published data presented, Pt in comparison to Au, presents a larger capacitance per unit area c_s and higher surface resistivity r_s at lower frequencies, as defined by the values of c_0 and r_0. Pt also presents higher frequency dependence for c_s and lower frequency dependence for r_s; this is determined by the value of m and n. It is proposed that this is due to the increased sorption of ions at the Pt interface. The Pt electrodes appear to present a large variation in the value of the m and n parameters across the published material. For frequencies between 10 Hz and 1 kHz, this value varies between 0.17 and 0.41 and appears to be independent of surface roughness. The values of c_0 appear proportional to the roughness of the electrode. It is difficult to determine a valid relationship between these parameters from the published data as there is no true basis for comparison between the actual surface roughnesses of the electrodes.

As there are only two examples for Au, the comparison is again not ideal. The capacitance per unit area is not as large as that shown for Pt and the frequency dependence is lower. The surface resistivity is also lower and shows a higher frequency dependence than Pt overall. It is proposed that this is determined by the lower susceptibility of Au to the adsorption of ions.

6.3 Noise at the Interface

The real part of the electrode-electrolyte interface impedance, the series resistance R_s, gives us information about the dissipation of electrical energy at the interface. Physically, this is caused by the electrophoretic movement of ionic charge towards and away from the electrode interface. This will also include the mechanisms and kinetics of surface sorption for H^+, OH^- and Cl^-.

When measuring neural signals with Pt and Au electrodes, the electrical resistance presented by R_s is directly within the signal path. The fluctuation dissipation theorem of thermodynamics states that for a system in thermal equilibrium, the noise may be identified by its dissipative properties. It is from this theorem that Nyquist explained Johnson's experimental observation of thermal noise in solid and liquid state conductors. R_s will therefore introduce thermal noise into the system. If the electrode is in equilibrium, i.e. there are no sustained electrochemical reactions occurring at the interface, R_s will present the main noise contribution to the signal path.

The relationship between R_s and the rms noise of a noble metal electrode was demonstrated by Gesteland et al. for Pt microelectrodes in saline at frequencies between 10 Hz and 50 kHz [35]. In this work Gesteland et al. also discussed a similar response for Ag/AgCl electrodes.

Loeb et al. [34] and Wise et al. [3] have also referred to the relationship between the noise of a microelectrode and the real part of the impedance in their work.

More recently, experimental data presented by authors using Ag/AgCl electrodes has shown that the noise at frequencies between 0.5 Hz -500 Hz may be an order of magnitude greater than that predicated by R_s [36, 37], although similar frequency dependent profiles were observed to that predicted by the R_s slope.

Ag/AgCl is not polarisable and has an interfacial surface resistivity that is several orders of magnitude lower than Pt or Au. This is due to the reaction between the AgCl

membrane and Cl^- within saline. It is proposed that for this material the noise that is not predicted by R_s may be the result of the lower dc charge transfer resistance: R_{ct}. At a given electrode, the lower vale of R_{ct} will reduce the shunt of the parallel connected CPE upon R_{ct}. If the ratio between R_{ct} and the impedance of the CPE is low enough then the thermal noise contribution of R_{ct} will become significant.

Further data was presented by McAdams et al. that showed at low frequencies, the noise of the Au electrode may be attributed to the real part of the electrode impedance [38]. However, in this work McAdams at al. concentrated upon the parallel value of R_{ct}. The value of R_{ct} calculated for the electrodes in this work is much smaller than values published by Wise at al. [19] and indicates that Au is not a polarizable electrode. There was also no attempt to compare the series real part of the CPE to the results.

Recently, Liu et al. [30] have used contemporary high performance measurement equipment to measure the power spectral density of the noise of the platinum-physiological saline interface. Liu et al. showed that the electrode noise is equivalent to the series resistance R_s or real part of the complex series impedance measurement for frequencies within the electro-neurogram spectrum.

From the evidence in these papers, it is proposed that the noise of Pt and Au electrodes in saline will be dominated by the thermal contribution. For polarisable electrodes such as Au and Pt the thermal movement of ions and dipoles within the double layer and small fluctuations in the sorption of ions such as H^+, OH^- or Cl^- is the most physically probable source of noise. Liu et al. attributed the noise at platinum electrodes to oxide or hydride sorption following the reactions presented in figure 6.4.

As Au displays a much lower propensity to adsorption at equilibrium it is proposed that the interfacial noise is dominated by ionic and dipolar thermal agitation.

The rms thermal noise resulting from R_s may be calculated according to equation 3.11: The noise profile will follow the frequency dependence of the R_s giving larger contributions at the lower frequencies. Thus, the spectral distribution of rms thermal noise is calculated by:

$$V_{n,therm} = \sqrt{4k_B \cdot T \cdot R_s} = \sqrt{4k_B \cdot T \cdot R_0 f^{-n}} \qquad 6.17$$

where the symbols have their usual meanings.

Equation 6.17 may be used with measured values of R_0 and –n to estimate the intrinsic noise of a Pt or Au microelectrode. The total noise for a given frequency range may be calculated by integration.

6.4 Discussion: A Proposed Method to Remove the DC Half Cell Potential and Low Frequency Drift

This chapter has investigated the published theoretical and measured values of the dc and ac electrical properties of the electrode electrolyte interface for Pt and Au. For direct extracellular neural signal measurement using Pt and Au electrodes the main challenge has been identified as the removal of the equilibrium potential before the signal is amplified.

An immediate solution is to capacitively decouple the amplifier input from the electrode. As discussed in chapter 3, this solution works well for external amplification and conditioning circuitry where circuit area is not at a premium. For many contemporary fully integrated amplifier based MEA microchips, the large decoupling capacitance of the input dominates the circuit area and inevitably constrains the inter-electrode pitch to distances many times greater than the spacing of neurons in culture.

An alternative method is proposed that exploits the interfacial properties of the electrode-saline interface to remove the dc offset and low frequency drift. A similar method was originally investigated by the pioneering work of Wise et al. in the 1970's [33, 19] during the first steps in packaging integrated circuits into neural sensing devices. The motivation of Wise et al. was to determine the properties of the interface to assist in the design of a custom integrated circuit that was packaged at the back end of a Si multi electrode spike for extracellular signal recording *in vivo* [3]. This method was

termed ‘dc stabilization’ and used a p-n junction based resistor to assist in the removal of the interfacial potential E^0. This device is discussed in section chapter 2, section 2.4. Wise used this technique to reduce the complexity of fabrication by removing the necessity for extra masks and processing steps required to produce a linear capacitor on chip.

Here the method is re-investigated as an effective method to reduce the area of each input channel.

For Au and Pt electrodes in physiological saline there are no sustainable electrochemical charge transfer reactions within the potentials of water electrolysis known as the ‘water window’. Surface sorption of dissolved H^+, OH^- and Cl^- has been observed in acidic, alkaline and neutral solutions containing these ions within defined potential ranges. This charge transfer path is slow and is limited by surface coverage.

Sorption is measured electrically as an ac property. This presents a frequency dependent capacitance that augments the frequency independent interfacial capacitance predicted by Stern. Sorption capacitance is thus a factor of the ac impedance characterised by C_s and R_s.

It is proposed that the lack of a specific and sustainable charge transfer path in saline may be exploited to overcome the interfacial potential E^0. E^0 typically has a value of several hundred millivolts and is present at the metal-electrolyte interface between a microelectrode and the cleft in neural signal measurement.

6.4.1 Proposed Electrode Model

The electrode model presented in figure 6.1 is used to describe the electrical properties of the electrode electrolyte interface. The model includes the charge transfer resistance R_{ct}, the open circuit interfacial potential at equillibrium E^0, the lumped series interface resistance R_s and capacitance C_s. The frequency dependent noise contribution $V_{n,therm}$ is included as part of the circuit. The model is repeated in figure 6.6 with the circuit parameters R_{ct}, R_s and C_s described in terms of the electrode surface area; r_{ct} and r_s are the surface resistivity parameters and c_s is the capacitance per unit area of the electrode surface. The values of r_s and c_s are presented in terms of equation 6.15 and 6.16 to show the empirical form.

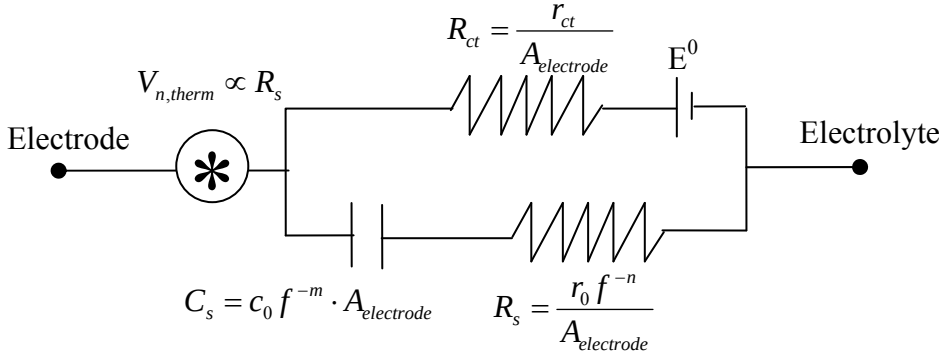

Figure 6.6

Electrical model of the electrode-electrolyte interface

The model may be used with the measured values of the electrical parameters to predict the behaviour of the electrode-electrolyte interface.

6.4.2 Removal of the DC Half Cell Potential

It is proposed that effects of E^0 may be much reduced at the amplifier input by reducing the input impedance to ground. In order to fully measure E^0 for noble metals, the input impedance of the amplifier must be large enough to approximate a perfect open circuit measurement. FET amplifiers are favoured for neural signal measurement due to their high input impedance and low input current leakage. A FET amplifier input will typically provide load impedance greater than 1 TΩ. This is sufficient load for the amplifier to preserve and amplify the full value of E^0 at the input.

The electrochemical charge transfer mechanism that drives the measurement of the dc potential can be modelled as an ideal voltage source, E^0, in series with a resistor, R_{ct}, as shown in figure 6.7, with E^0_{ref} and $R_{ct,ref}$ representing the dc electrical properties of the reference electrode. The reference electrode circuit may be removed from the analysis as it is the chosen reference point. The potential measured by the measurement circuit is given by

$$V_{meas} = E^0 - I_{load} \times R_{ct} \qquad 6.18$$

where V_{meas} is the measured output voltage of the battery and I_{load} is the current drawn by the input load resistance R_1.

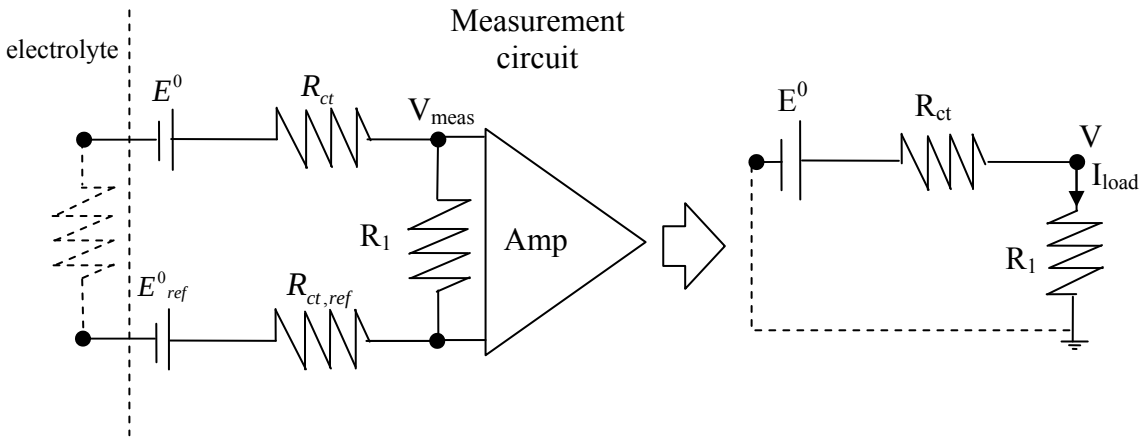

Figure 6.7
Electrode interface potential electrical equivalent circuit

Equation 6.18 may be rewritten in terms of E^0 and R_1 as:

$$V_{meas} = \frac{E^0}{\left(1 + \frac{R_{ct}}{R_1}\right)} \qquad 6.19$$

If R_1 is chosen to be much smaller than R_{ct}, the potential measured at the input of the measurement circuit will be attenuated relative to equation 6.19.

This indicates that the input offset problem of the half cell potential may be controlled by the placement of a resistive load element within the measurement circuit (as is already the case with most front end high pass filter circuits) that meets the criteria of equation 6.19. This is an important result for controlling the extent of the interfacial potential offset without employing dc blocking capacitors that exert a high area cost on chip. As this technique would effectively reduce the input impedance of the measurement circuit one must ensure that the value of R_1 remains significantly greater than the magnitude of the neural signal source impedance to ensure the neural signal is not also attenuated.

6.4.3 Exploiting the Interface Capacitance for Removal of Low Frequency Interference

It is proposed that for Pt and Au electrodes the series capacitance C_s and resistance R_s shown in figure 6.6 may be exploited as part of an intrinsic high pass filter. The circuit model was substituted into the transfer function for a high pass filter to simulate the response of the interface as part of the input circuit. The resulting circuit is presented in figure 6.8.

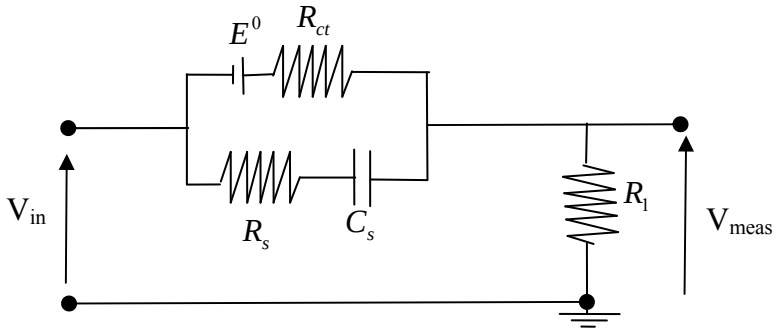

Figure 6.8
The modelled interface high-pass filter circuit

For small ac signals around the electrode equilibrium potential the transfer function is:

$$H(jf) = \frac{R_1\left(1 + C_s \cdot 2\pi \cdot f \cdot j \cdot \left(R_{ct} + R_s\right)\right)}{R_{ct} \cdot \left(\left(1 + R_s \cdot C_s \cdot 2\pi \cdot f \cdot j\right) + R_1 \cdot C_s \cdot 2\pi \cdot f \cdot j \cdot \left(1 + \left(R_{ct} + R_s\right)\right)\right)} \qquad 6.20$$

Where R_1 is the resistive component of the filter shown in figure 6.8, C_s is the frequency dependent series capacitance, R_s is the frequency dependent frequency resistance, R_{ct} is the charge transfer resistance, f is the signal frequency and j is $\sqrt{-1}$.

The Au-saline interface presents an R_{ct} many orders of magnitude larger than the current path presented by C_s and R_s. Similarly, if R_1 is chosen so that it is much larger than R_s equation 8.1 may be reduced to the much simpler form:

$$H(jf) = \frac{R_1 \cdot C_s \cdot 2\pi \cdot f \cdot j}{1 + R_1 \cdot C_s \cdot 2\pi \cdot f \cdot j} \qquad 6.21$$

Using equations 6.15 and 6.16, the gain of equation 6.21 may be described by:

$$G(f) = \left|H(jf)\right| = \frac{R_1 \cdot C_0 \cdot f^{-m} \cdot 2\pi \cdot f}{\sqrt{1 + (R_1 \cdot C_0 \cdot f^{-m} \cdot 2\pi \cdot f)^2}} = \frac{R_1 \cdot C_0 \cdot 2\pi \cdot f^{(1-m)}}{\sqrt{1 + (R_1 \cdot C_0 \cdot 2\pi \cdot f^{(1-m)})^2}} \qquad 6.22$$

where

$$C_0 = c_o \cdot A_{electrode} \qquad 6.23$$

and $A_{electrode}$ is the surface area of the electrode.

The dc signal measured at V_{out} is equal to equation 6.19. The response of an RC filter would typically produce an attenuation factor or 'roll-off' of 20 dB/decade, calculated by:

$$A_{dB}(f) = 20\log_{10}\left[H(f)\right] \qquad 6.24$$

Due to the frequency dependency of C_s, the roll off will be sub optimal. The value of the rolloff for frequency dependent capacitors may be calculated by:

$$A_{dB}(f) \approx 20\log_{10}\left[\{H(f)\}^{1-m}\right] = 20\cdot(1-m)\log_{10}[H(f)] \qquad 6.25$$

Using values for thin film Au electrodes taken from table 6.1 and 6.2, the model predicts a minimum roll off of 11.8 dB for Pt and 16.16 dB for Au.

The roll off is sub-optimal in comparison to a linear capacitor. The results presented by Mirtaheri [21], Onaral [31] and Schwan [32] also indicate that the filter roll off will become less steep for signals below 1 Hz. However the circuit will still provide a rudimentary filter function that will assist in the removal of interference at frequencies below the extracellular neural signal spectrum.

6.5 Conclusion

It is proposed in this chapter that the properties of the Pt and Au interfaces may be exploited to remove the need for a dc decoupling capacitor to be placed between the electrode and the signal measurement circuitry. The ability for the circuit to remove E^0 and low frequency interference while retaining the neural signal will be dependent upon the careful selection of the electrode material and the value of R_1.

The chapter concludes that the properties of the electrode-electrolyte interface for Pt and Au may be exploited by the amplifier input circuitry to remove the interference from dc offset and drift. This is investigated experimentally in chapter 7 using Pt and Au electrodes formed using microfabrication techniques. This electrode fabrication method was chosen as it is the same method that will be used as part of the post processing of an integrated neural signal measurement array.

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Chapter 7

Experimental Investigation into Thin Film Pt and Au Electrodes for a Novel, Reproducible CAP Signal Amplifier Area Reduction Method

This chapter investigates the electrical properties of the extracellular microelectrode interface with the physiological saline system for smooth thin film Pt and Au electrodes. These properties are not available from any single source in the literature. The properties of smooth thin film electrodes were investigated as this method reproduces the electrode surface that will be formed on an application specific integrated circuit (ASIC) microelectrode array (MEA) as part of post processing. The electrodes were fabricated using microfabrication techniques; this is described in section 7.1. Measurements were taken to characterise the electrical properties of the interface as defined in chapter 6. The measured values of E^0, C_s and R_s are presented in section 7.2. Au is selected as the best electrode material for this application as the interface capacitance is much less dependent upon frequency and Au is a much easier material to work with for electrode fabrication.

Section 7.3 develops the method proposed in section 6.4 in which the electrode-electrolyte interface can be integrated into the measurement circuit such that the smaller higher frequency neural signals can be extracted from the larger dc half cell potentials and drift. Design rules are presented to define a range of values for R_1 to remove E^0 and low frequency interference while preserving the neural signal.

Further experiments are then described to characterise the design parameters of the thin film Au electrodes including the half cell potentials, dc interface resistance and ac electrode

impedance and an electrical design model is proposed in section 7.4. The removal of the dc potential and filter characteristics of the circuit are investigated for a range of electrode sizes and input load resistances. The method is then verified by measuring the performance of the proposed circuit as part of an amplification circuit.

7.1 Thin Film Electrodes

Thin film electrodes were fabricated using conventional micro fabrication methods that would typically be used to manufacture MEAs or be performed post-process to apply Pt or Au. Electrodes were formed as an array on polished 50 mm dia. quartz crystal wafer substrate (SAWYER). SAWYER Quartz substrates are guaranteed to have a surface flatness within a 0.66 nm standard deviation; this is defined between surface peaks and troughs. Electrodes were spaced by 4 mm to prevent inter-electrode interference. Polished quartz crystal was used due to its excellent insulating properties. Electrodes were fabricated from high vacuum evaporated Pt and Au (Goodfellow) with an SU-8 (Chestech) insulation layer. The electrode pattern was designed to provide eight 150 µm diameter disc electrodes, with 2 mm spacing using a two mask process. The electrodes and tracks were formed on a 20 nm thick seed layer of Ti. The electrode and track metallization was 130 nm thick for Pt and 200 nm thick for Au. Fabrication recipes and the materials used are given in more detail in Appendix C and D. Masks were drawn in L-Edit software package and written to 3" Borosilicate-Chrome masks (Telic) using a Heidelberg DWL66 mask writer. A photograph of the array is shown in figure 7.1 beside a magnified image of an Au electrode.

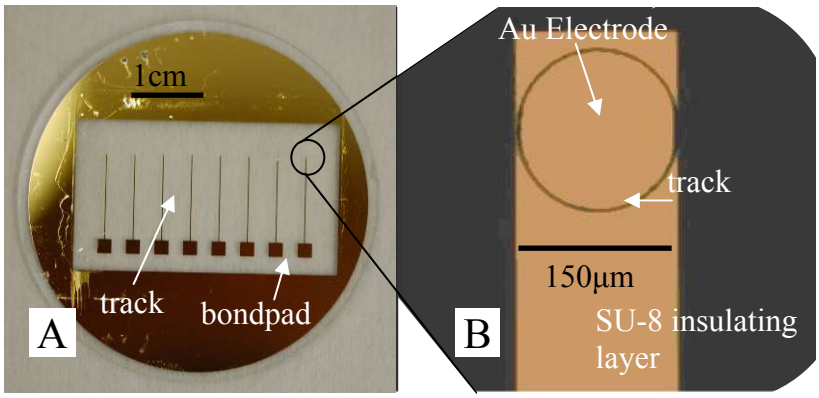

Figure 7.1

Photograph of A, an Au on quartz electrode array, B, a magnified single electrode

Reactive ion etching was performed on the array post fabrication to remove non-cross linked SU8 and SU8 developer contamination from the electrodes.

7.1.1 Surface Roughness of Thin Film Electrodes

The electrodes were optically smooth. Electrodes were scanned using an atomic force microscope (AFM) to determine the average surface roughness at feature sizes below the limits of optical detection. Selected surface scans of the thin film electrodes are shown in figures 7.2 for Pt and 7.3 for Au. The images are false coloured to represent the natural colour of the native material.

The AFM scans showed that the thin film Pt and Au electrodes presented a roughness on the nm scale. The Pt electrodes presented a total surface area, including the measured roughness that was 0.502 % greater than the geometric area. Au electrodes had a surface area that was determined to be 1.63 % greater than the geometric area.

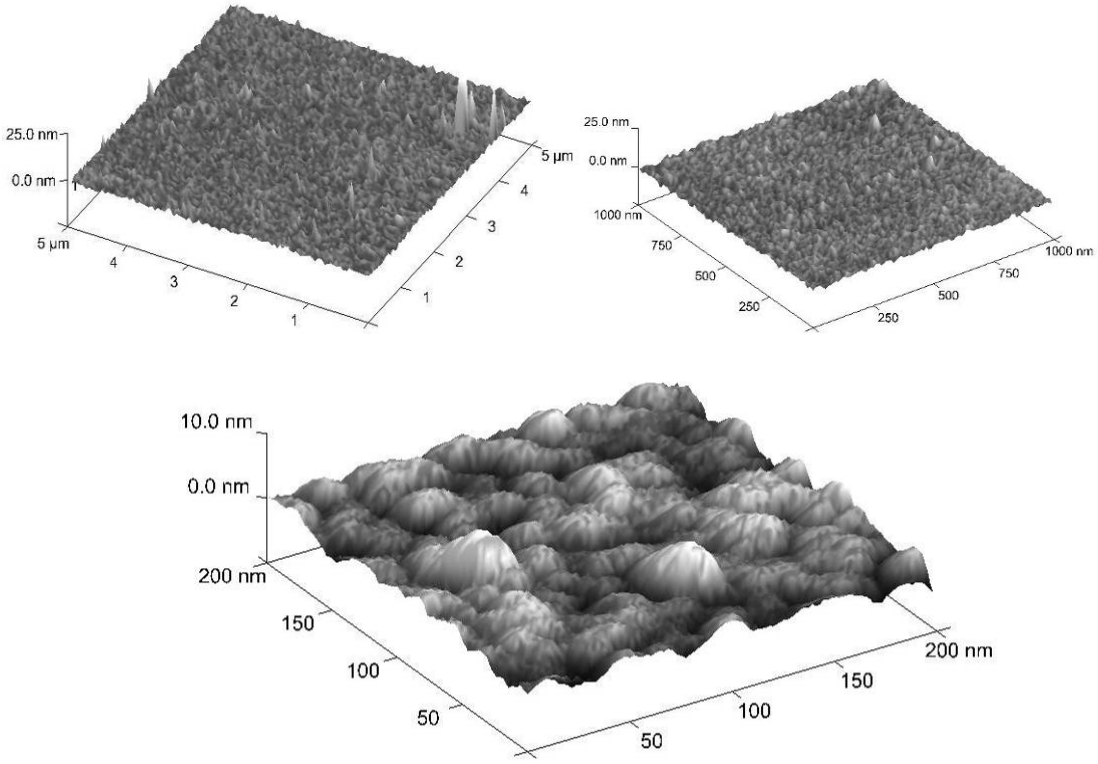

Figure 7.2

AFM 3D Surface profile of thin film platinum electrode at 5 µm x 5 µm, 1 µm x 1 µm and 200 nm x 200 nm area

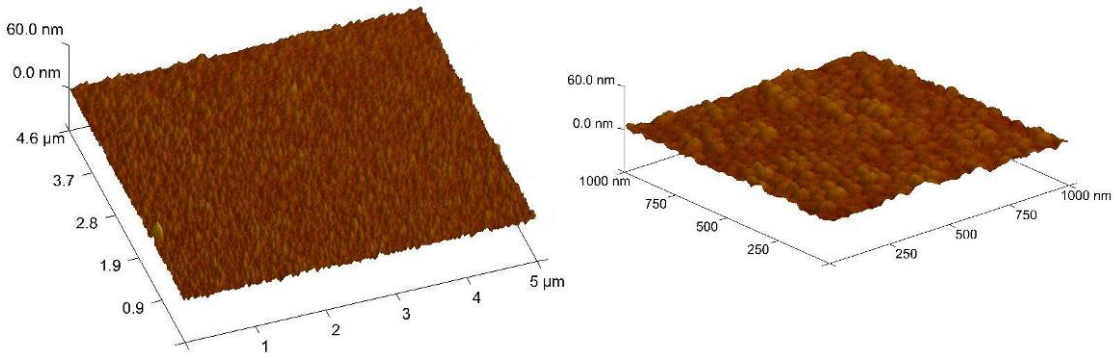

Figure 7.3

AFM 3D Surface profile of thin film gold electrode at 5 µm x 5 µm and 1 µm x 1 µm area

7.2 Electrical Properties of Pt and Au Thin Film Electrodes

The electrical properties of the interface between the thin film electrodes and physiological saline were measured to define the electrical properties of the dc and ac modes as defined in chapter 6.

7.2.1 The DC Mode

The dc mode includes the values of E^0 and R_{ct} as defined in chapter 6. This section investigates the values of E^0 and R_{ct} experimentally for thin film Pt and Au electrodes fabricated using photolithographic methods.

7.2.1.1 Measured Values of E^0

A Keithley 6514 electrometer was used to provide high impedance measurements of Pt and Au thin film electrodes. A two electrode cell was formed between the Au or Pt electrode and a commercial Ag/AgCl reference electrode (BASI) with 3M filling solution. The Ag/AgCl reference electrode provides a stable reference potential of +0.222 V relative to the standard hydrogen electrode (SHE). The electrochemical cell measurements were made

within a grounded Faraday cage to minimise interference that may influence the interface potential.

Over eight thin film electrodes, Pt had a mean equilibrium potential of 381.3 mV relative to saturated Ag/AgCl with a standard deviation of 29.8 mV. Au electrodes had a mean of 536.9 mV relative to saturated Ag/AgCl with a standard deviation of 91.3 mV.

From these measurements the equilibrium potential relative to the standard hydrogen electrode (SHE) is:

E^0(Pt) vs. SHE= E(meas) + 222 mV = 603.3 mV ± 29.8 mV

E^0(Au) vs. SHE= E(meas) + 222 mV = 758.9 mV ± 91.3 mV

7.2.1.2 The DC interface resistance R_{ct} near E^0

Values for R_{ct} could not be measured directly at potentials near E^0 or within the water window for the thin film electrodes. Several attempts were made using a slow cyclic voltammetry program using a three electrode potentiostat (Perkin Elmer VMP) at potentials +/- 100 mV around E^0. Step changes of 1 mV / second were applied to the electrodes to ensure that the capacitive current remains lower than the dc charge transfer current, however the measured current was in each case below the 10 nA noise floor of the potentiostat arrangement. This was also the case for much larger drawn wire Pt and Au electrodes with surface areas up to 1 cm^2. This indicated that the surface resistivity of the interface is much greater than 1 $M\Omega/cm^2$. An alternative method to determine R_{ct} is proposed in section 7.4.2.1.

7.2.2 The AC Mode

The response of the interface to small ac signals was measured between 40 Hz and 100 kHz. This range exceeds the highest spectral frequency range of extracellular neural signals

as defined in chapter 5. From this analysis the model parameters for thin film Pt and Au electrodes were formed.

7.2.2.1 Method

The impedance of the interface was characterised using an Agilent 4294A impedance analyser. The 4294A is a two point probe measurement device. The impedance analyser was connected to the electrodes as shown in figure 7.4. Circuit calibration was performed to eliminate cable and fixture parasitic impedance before the saline was poured into the containers. The impedance analyser was programmed to calculate the series equivalent capacitance C_s and resistance R_s. A series method was used as it has been determined that the physical charge transfer resistance in the electrode's intended region of operation is negligible. This method conforms to the work of other authors to allow direct comparison.

The electrode impedance was measured at frequencies between 40 Hz and 100 kHz with at amplitudes of 5 mV pk-pk. The experiment was conducted at a laboratory temperature of 21ºC.

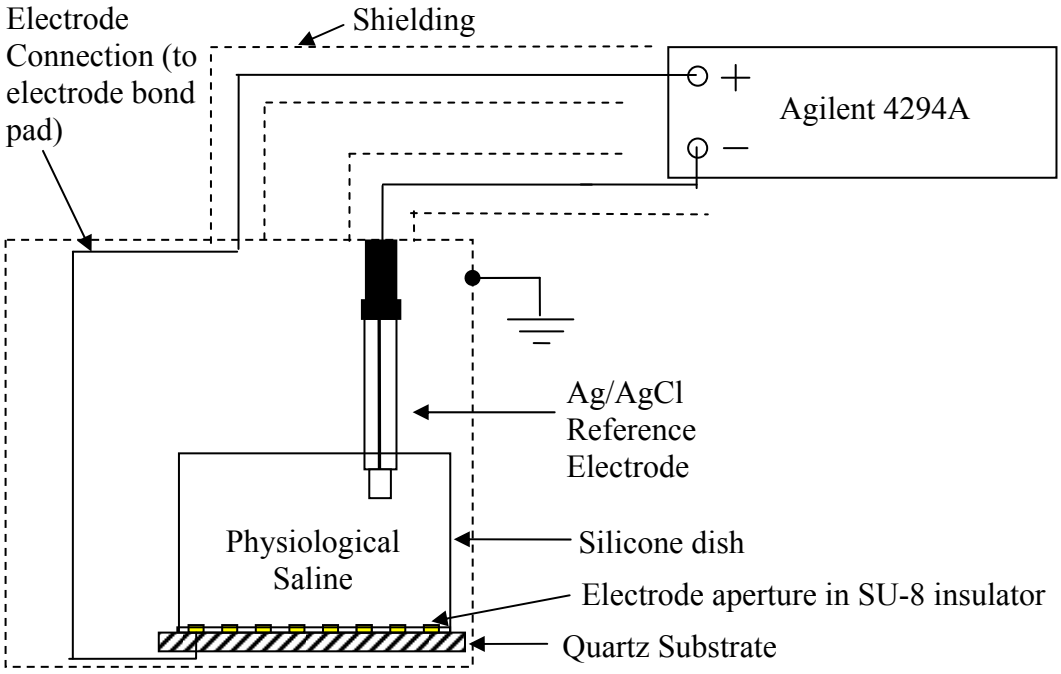

Figure 7.4

Connection of array to impedance analyser

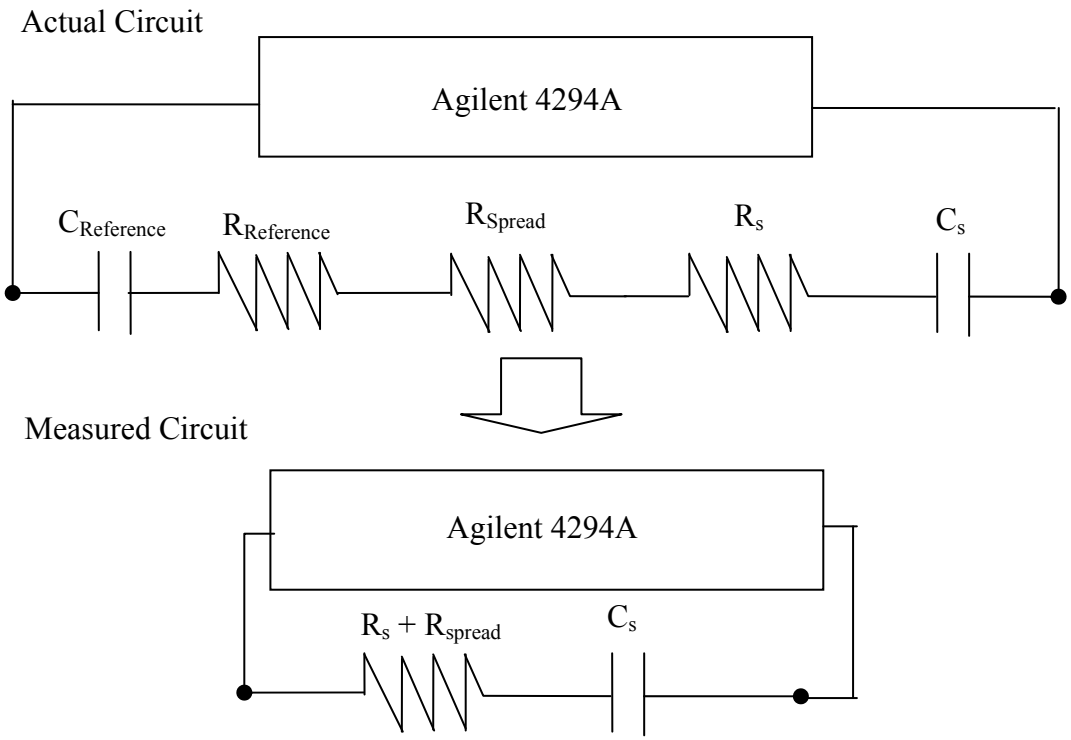

Figure 7.5

Comparison of the actual series circuit with the measured series circuit.

A commercial Ag/AgCl reference electrode (BASI) was used to complete the series impedance measurement circuit.

The contact surface area of the reference electrode was several of magnitude larger than that of the working electrode. Ag/AgCl electrodes also have a much larger interfacial surface capacitance and much lower interfacial surface resistivity than Au electrodes.
The result is that their effect is negligible upon the measured series resistance. The measured capacitance and resistance of the circuit is equivalent to that of the working electrodes as shown in figure 7.5.

Hence, it is assured that $R_{Reference}$ and $C_{Reference}$ can be neglected. Thus the value of C_s is taken as the measured series resistance between the measurement nodes. R_s may be calculated by subtracting the spreading resistance of the electrode from the total measured series resistance. The spreading resistance in physiological saline is calculated using the

Newman spreading resistance model for a disk and the resistivity of extracellular fluid given in table 4.1:

$$R_{spread} = \frac{\rho}{2r} \qquad 7.1$$

where ρ is the resistivity of physiological saline (~70 Ωcm) and r is the radius of the electrode.

7.2.2.2 Results

The measurements of C_s and R_s from the individual electrodes E1 to E8 in the array are plotted in figure 7.6 for Pt and figure 7.8 for Au. The plots were analysed statistically to calculate the mean curves and standard deviation for C_s and R_s to develop the model in section 7.2.4. Pertinent statistical values are presented in table 7.1. The mean curves for C_s and R_s are presented in the figures with the experimental data showing error bars to one standard deviation. The data was fitted to C_s and R_s using the power fit relationships presented in chapter 6; equation 6.15 and 6.16. The equations are rewritten in this chapter for clarity and are modified to calculate the total values as opposed to the unit area values:

$$C_s(f) = C_0 \cdot f^{-m} \qquad 7.2$$

$$R_s(f) = R_0 \cdot f^{-n} \qquad 7.3$$

The data fitting was performed in Matlab. All fits have an R^2 value greater than 0.96. R_s was fitted for Pt between 40 Hz and 3 kHz. The phase of the reactance is plotted for the experimental values of C_s and R_s according to equation 6.14 in figure 7.7 for Pt and 7.9 for Au.

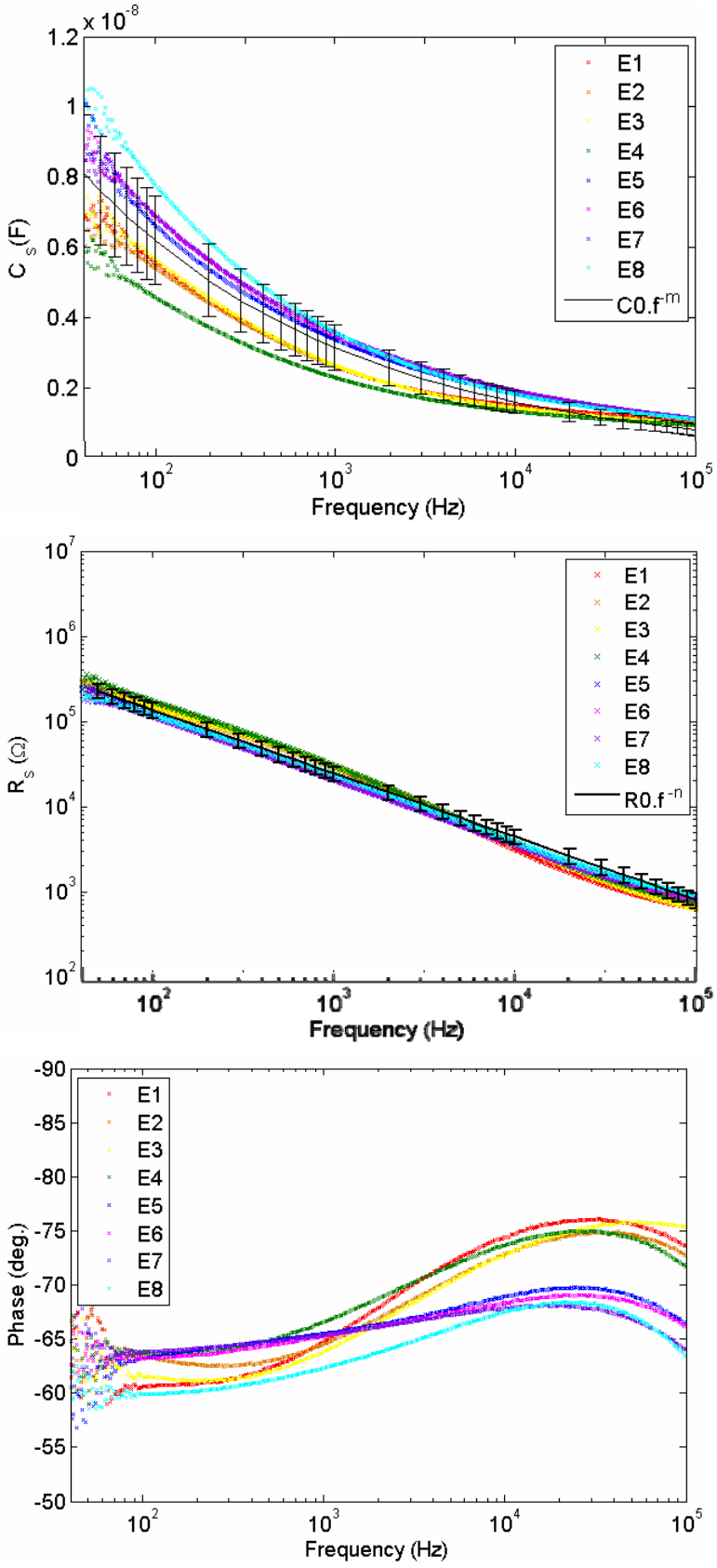

Figure 7.6

Series capacitance, resistance and phase of thin film Pt electrode interface with physiological saline

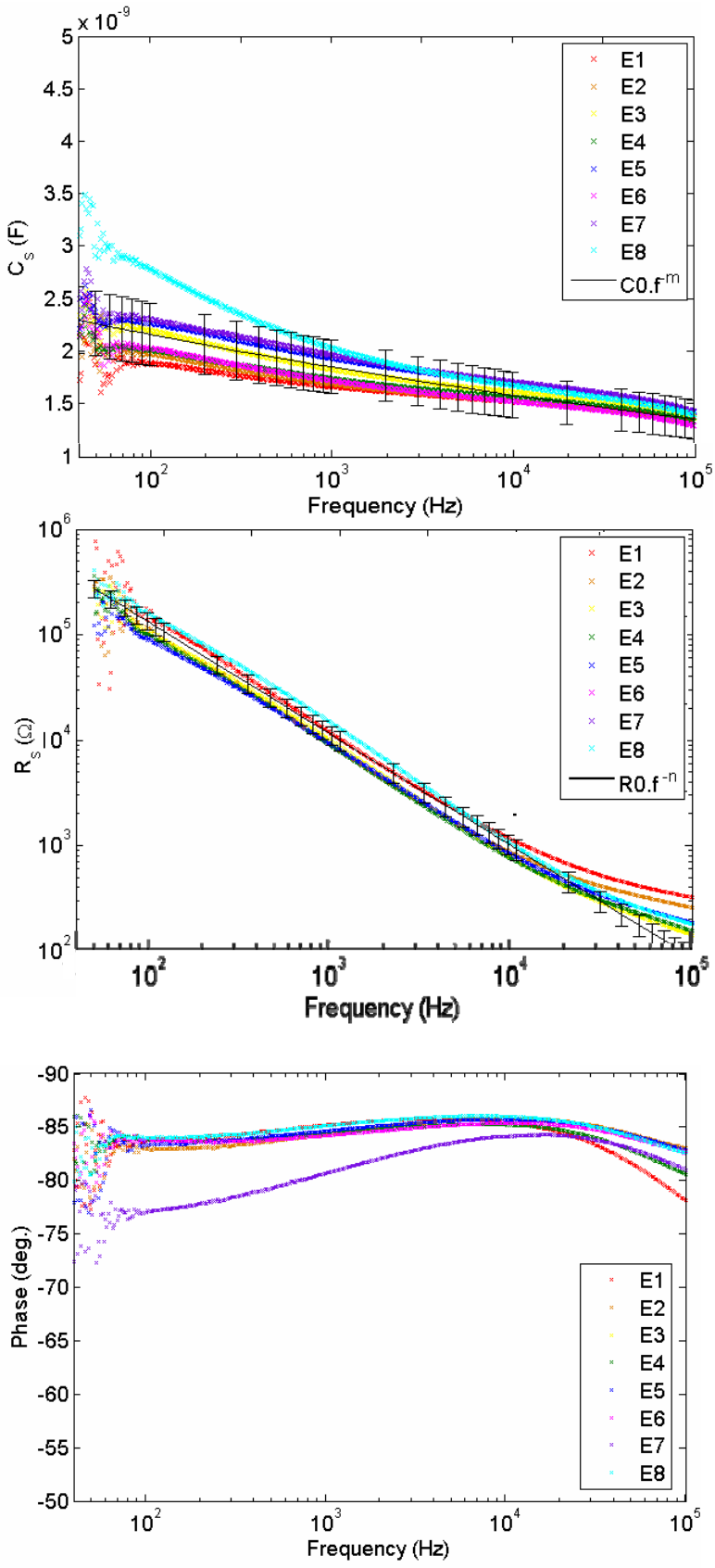

Figure 7.7

Series capacitance, resistance and phase of thin film Au electrode interface with physiological saline

Pt	C_0 $\left(nF \cdot \sqrt[m]{Hz}\right)$	R_0 $\left(M\Omega \cdot \sqrt[(1-m)]{Hz}\right)$	-m	-n
Maximum	34.78	5.958	-0.281	-0.7148
Minimum	17.28	3.17	-0.326	-0.778
Mean	24.09	4.165	-0.295	-0.744
Std. Deviation	4.908	0.8184	0.017	0.053

Table 7.1

Statistical information for the Pt array

Au	C_0 $\left(nF \cdot \sqrt[m]{Hz}\right)$	R_0 $\left(M\Omega \cdot \sqrt[(1-m)]{Hz}\right)$	-m	-n
Maximum	4.807	11.85	-0.056	-0.939
Minimum	2.703	5.432	-0.1	-0.997
Mean	2.95	7.83	-0.068	-0.9712
Std. Deviation	0.8106	1.978	0.0182	0.0204

Table 7.2

Statistical information for the Au array

7.2.2.3 Discussion

The ac electrical characteristics of thin film electrodes were measured over and above extracellular neural signal spectrum. The results show that the electrode interface behaves as a non-ideal capacitance following Frick's Law with the frequency dependent capacitance and resistance more or less forming a constant phase circuit element. The values of m and n are close to the expected relationship:

$$n = 1 - m \qquad 7.4$$

The capacitance of Au is less frequency dependent than Pt and the resistance is more frequency dependent. The phase and R_s curves show that the interfacial impedence of Au

also has lower resistive losses than Pt. Pt shows a phase that varies between – 65 ° to - 75 °, whereas Au shows a phase between – 80 ° to – 85 °. It is proposed that this is due to a much lower level of sorption occurring at the Au interface at the measurement equilibrium potential. This proposal is substantiated by the chronopotentiometric plots presented in section 6.1.3 and referenced information from the literature.

The thin film Au and Pt electrodes are much smoother than other electrodes used in the literature. The work referenced in chapter 6, section 6.2.6 for Pt and Au electrodes were either mechanically polished, diamond saw cut or electrodeposited. None of these techniques can achieve the level of surface smoothness possible with thermal vapour deposition upon ground and polished quartz substrates in high vacuum.

Table 7.1 and 7.2 are reproduced below with values of C_s and R_s converted to the capacitance per unit area c_s and surface resistivity r_s for direct comparison to table 6.1 and 6.2 .

Pt	$c_0 \left(\mu F \cdot \sqrt[m]{Hz}\right)$	$r_0 \left(k\Omega \cdot \sqrt[(1-m)]{Hz}\right)$	-m	-n
Maximum	196.8	1.053	-0.281	-0.7148
Minimum	97.78	0.56	-0.326	-0.778
Mean	136.32	0.736	-0.295	-0.744
Std. Deviation	27.8	0.145	0.017	0.053

Table 7.3

Statistical values of Pt per unit area electrode

Au	$c_0 \left(\mu F \cdot \sqrt[m]{Hz}\right)$	$r_0 \left(k\Omega \cdot \sqrt[(1-m)]{Hz}\right)$	-m	-n
Maximum	23.1	2.1	-0.056	-0.939
Minimum	15.29	0.96	-0.1	-0.997
Mean	16.69	1.38	-0.068	-0.9712
Std. Deviation	4.59	0.349	0.0182	0.0204

Table 7.4

Statistical values of Au per unit area electrode

Platinum Electrodes

The Pt electrodes show a mean value of c_0 that is lower than the data presented by De Boer et al. [1], Onaral et al. [2], and Schwan et al. [3] for equivalent measurements in physiological saline. It is proposed that this is due to the increased surface area presented by the polished and unpolished surfaces in these previous studies. The mean value of r_0 is higher than the data in the literature, with the exception of Onaral et al. This is attributed to the lower surface area of the smooth electrodes. Mirtaheri's values of c_0 are lower [4] and values of r_0 are higher for Pt electrodes, however he used saline of 77 mM NaCl concentration. It is proposed that this lower value of c_0 is due to a lower concentration of Cl^- ions reducing the sorption capacitance, as the ionic concentration presents a significant difference in the experimental conditions, other than the surface roughness between Mirtaheri's experiments and the other referenced experiments.

The frequency dependence of the Pt electrodes would be expected to reduce if Scheider's theory of lateral charge transfer [5] was the main cause of the frequency dependence. Table 7.3 shows that –m varies between -0.281 and -0.326 for thin film electrodes. This indicates higher frequency dependence for smooth thin film electrodes in comparison to the unpolished examples from Liu et al. and De Boer et al. Onaral et al. and Schwan et al. show higher values, whereas Mirtaheri's results show a value close to the mean value in table 7.3. As discussed in chapter 6, section 6.2.6 there is no definite trend between the value of –m and the surface roughness. It has been proposed that sorption is the main cause for the capacitance and frequency dependence in Pt; one may speculate that the sorption process and lateral charge transfer process compete to produce a more complex relationship between roughness, sorption and –m. To determine this relationship one would require full knowledge of the surface roughness and cleanness of the electrodes for each referenced dataset. Unfortunately this information is not given for each case. The surface of the thin film Pt electrodes is investigated further in section 7.2.3 to determine whether the evaporation process formed defects in the surface that were not picked up with the AFM scans.

Gold Electrodes

The Au electrodes show a mean value of c_0 that is approximately half the value of the data published by Mirtaheri and Wise [6]. The mean value of r_0 is approximately twice that of Mirtaheri and Wise. As with Pt this is attributed to the increased surface area of the polished and electroplated electrodes over those of the thin film Au electrodes. The data presented by Mirtaheri for Au does not show a lower value of c_0 as with the Pt electrodes, it is proposed that this is caused by the lower level of sorption at the Au electrode; the capacitance is dominated by the charging of the double layer, which according to the Stern model is less sensitive to changes in ionic concentration within one order of magnitude.

Comparing the frequency dependence between the two examples from the literature with those presented in table 7.4, there is noticeable trend between roughness and –m. The –m value is observed to be proportional to roughness; Mirtaheri's polished electrode has the highest frequency dependence with –m = - 0.193, followed by Wise's electroplated electrode: –m = -0.1, followed by the mean value for the thin film electrode: -m = -0.068.

The Au - saline electrode interface closely resembles a linear circuit element capacitance. The frequency dependence is small, c_s only changes by a factor of 1.5 over three decades of frequency and the phase is very close to – 90 °. The value of c_s for Au is very close to that predicted by the frequency independent Stern capacitance that is discussed in chapter 6, section 6.2.4.

The Pt – saline interface presents a larger value of c_s at each given frequency that has much more pronounced frequency dependence. The value of c_s reduces by approximately five times over three decades of frequency. The phase is not as close to -90° as with Au indicating that the Pt interface incurs a greater proportion of resistive losses in comparison.

7.2.3 Processing Issues with Pt

The similarities between the larger rough platinum electrode and the microelectrode indicated that there may be some undetected surface defects that were missed by the AFM scans of the surface in which a randomly picked scanning area of 5 μm x 5 μm may miss.

metallization layers were formed on a Ti seed layer. This process is prone to cracking of the Pt film; Pt does not have enough energy when nucleated causing intrinsic stress in the film. The Pt electrodes were formed by a lift-off process due to Pt's nobility and difficulties in finding a suitable etchant (aqua regia at >75°C did etch the Pt film but was very slow and stripped the 1813 photoresist in the extended etching time). The lift off process caused ragged edges on the electrode tracks that may have propagated as cracks into the metal.

A sacrificial electrode array of 130 nm thick Pt on a 20 nm thick Ti seed layer was formed to investigate surface cracks. This array was not covered in SU-8 but placed in HF:H20 1:1 mixture for one minute to ensure that cracked areas exposing Ti would be etched, extending and exposing the cracks so that they could be optically identified. A typical photographed microscope image of the surface is shown in figure 7.8.

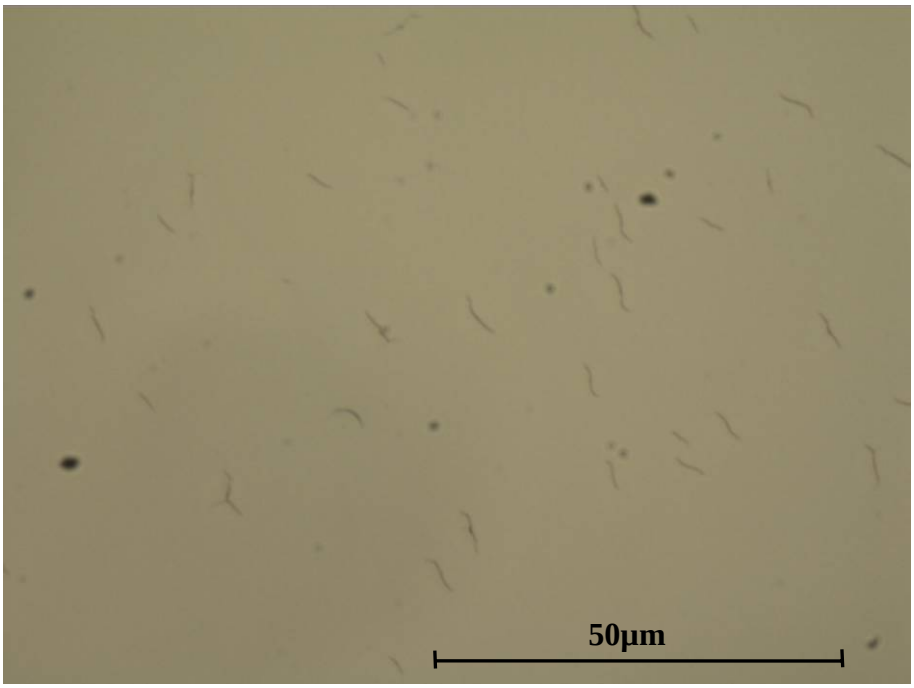

Figure 7.8

Microscope images of typical density of surface cracks in thin film Pt electrodes

There was no evidence of surface cracks travelling from the rough edges of the lift off process. There was however a number of small micron-scale cracks of approximately 2 µm – 7 µm length spread across the electrode surface. The density of these cracks was

approximately 20 – 40 per 100 μm x 100 μm area. The cracks caused a raised area of the electrode to occur in its vicinity due to Pt – Ti interfacial stress and the resulting partial lift off as illustrated in figure 7.8. This alone is not deemed a sufficient surface roughness to produce the extent of frequency dependent capacitance presented in figure 7.6. This indicates that sorption may be the primary cause of the larger unit area capacitance at the thin film electrodes. It may also be considered that the surface roughness may restrict the sorption process due to the need for the adsorbing ions to navigate the roughened surface as they are drawn and expelled from the surface. Further investigation will be required to fully understand this process.

7.2.4 Modelling

The experimental results from the Pt and Au electrodes were fitted to the model defined in chapter 6, section 6.4.1. The value of the potential at the electrode E is noted to define the mechanism for c_s and r_s. As the measurement was made using an Ag/AgCl reference electrode at 0 V bias the value will be brought down to the electrode potential for Ag/AgCl rather than the measured open circuit charge value E^0. At this potential it is proposed that the capacitance and noise will be caused by H^+ sorption for Pt and H^+ and OH^- sorption for Au. The potential table is reproduced from figure 6.4 with E^0 defined for the thin film Au and Pt electrodes in figure 7.9.

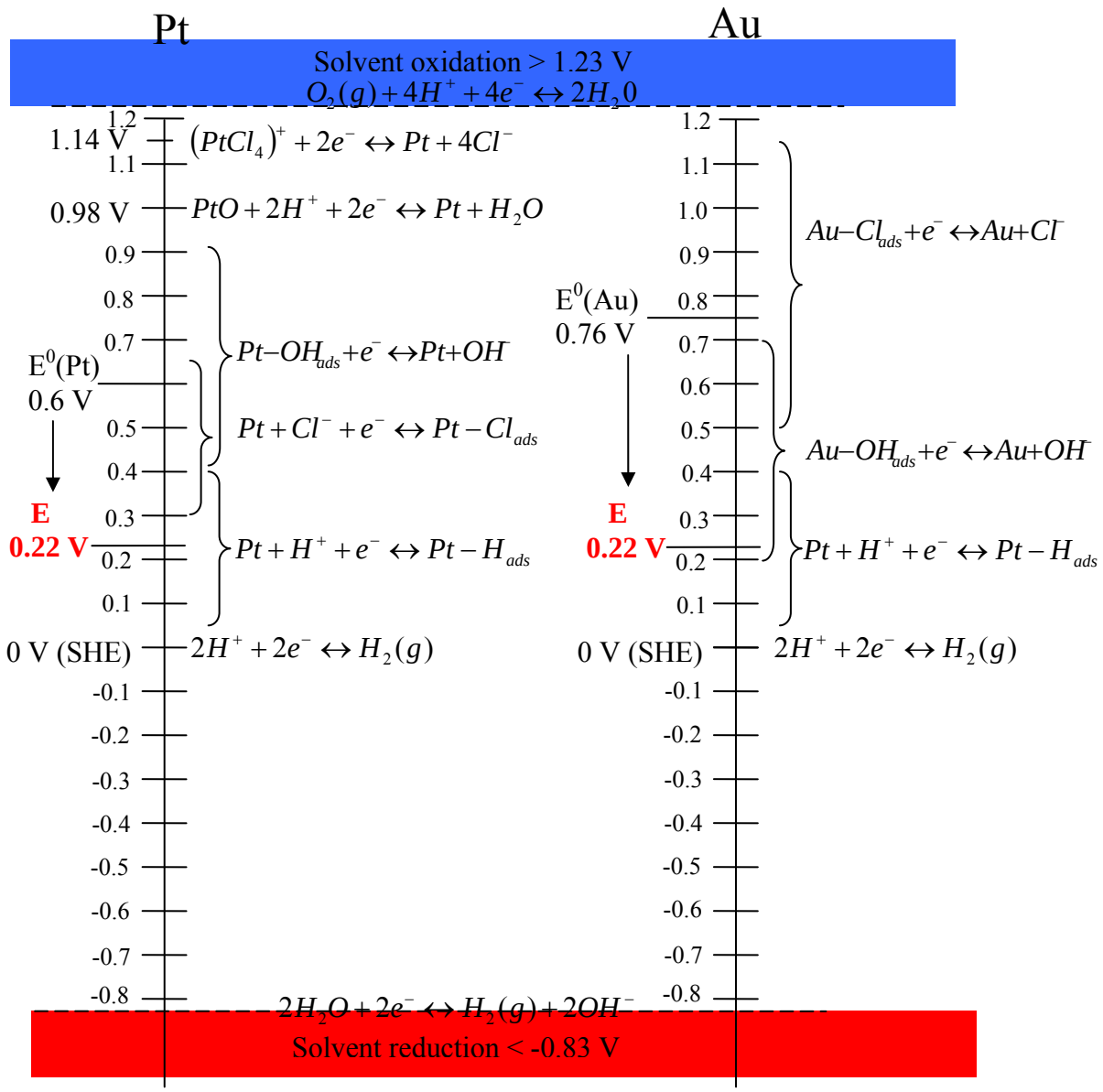

Figure 7.9

Table of electrochemical reactions and sorptions in physiological saline noting the experimentally measured value of E^0 for thin film Pt and Au electrodes.

The electrode model is presented in figure 7.10 together with fitted values taken from the data presented in figure 7.6 and 7.7. Fitted data is scaled to capacitance per unit area and surface resistivity from the area of the 150 µm diameter electrode and is calculated by:

$$c_0 = \frac{C_o}{A_{electrode}} \qquad 7.4$$

$$r_0 = R_o \cdot A_{electrode} \qquad 7.5$$

The noise values are calculated as defined in chapter 6, section 6.3 and scaled relative to the electrode area. The scaled thermal noise root area $V_{n,thermal}$, is calculated by:

$$V_{n,thermal} = \sqrt{4 \cdot k_B \cdot T \cdot \left(\int_{f=0}^{f=5000} r_0 \cdot f^{-n} df \right)} \qquad 7.6$$

Where k_B is Boltzmanns constant, T is the absolute temperature.

The noise values in table 7.3 are calculated for a laboratory temperature of 21°.

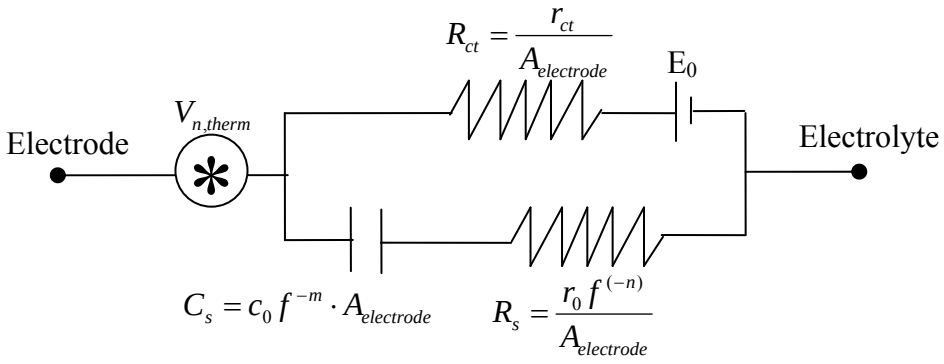

Figure 7.10

Electrode Model for Pt and Au electrodes

	Pt Thin Film	Pt Thin Film (stdev)	Au Thin Film	Au Thin Film (stdev)	Units
r_{ct}	> 1	N/A	> 5	N/A	$M\Omega \cdot cm^2$
r_0	0.736	0.145	1.380	0.350	$k\Omega \cdot \sqrt[(1-m)]{Hz} \cdot cm^2$
c_0	136.30	27.80	16.69	4.59	$\frac{\mu F \cdot \sqrt[m]{Hz}}{cm^2}$
-m	-0.2950	0.0170	-0.0680	0.0182	-
-n	-0.7440	0.0530	-0.9710	0.0204	-
E_0 vs. SHE	603.30	29.83	758.90	91.27	mV
$Vn_{thermal} \cdot \sqrt{A_{real}}$	22.50	9.90	13.40	6.70	$nV(rms) \cdot cm$

Table 7.5

Mean parameter summary for thin film electrode model (40 Hz -100 kHz)

The model may be used to calculate the electrical properties of the interface to design the circuit proposed in chapter 6, section 6.4 to remove the dc offset and filter low frequency drift.

7.2.5 Conclusion

Thin film Pt and Au electrodes were formed using photolithographic techniques to reproduce the post processing methods required to form noble metal electrodes on CMOS devices. AFM scans measurements shows that the electrodes had a peak to peak surface roughness that was of the order of several tens of nm. This corresponds to an average surface roughness of 0.502 % for Pt electrodes and 1.63 % for Au electrodes. The electrode roughness will be caused by the roughness of the quartz substrate rather than the deposition process.

The values of c_s and r_s for vacuum deposited thin film Pt electrodes in physiological saline showed considerable frequency dependence. The frequency dependence was comparable to

that of roughened Pt electrodes published by other authors that is presented in chapter 6, section 6.2.6.1 even with a much smoother surface. This is in contrast to Au which shows much less frequency dependence for c_s and r_s for smooth vacuum deposited thin films in physiological saline. It is proposed that this is due to the increased sorption of dissolved ions in the saline upon the Pt electrode surface. It is also proposed that the dominant mechanism for the frequency dependence of Au electrodes in physiological saline is the surface roughness, whereas for Pt electrodes the dominant mechanism is sorption.

Au electrodes are more favourable for CMOS post processing. This is due to two reasons; the first is that thermal vapour deposition of Pt produces stressed thin films, the second is that Pt is much more difficult to etch. The stressed films form micro cracks as shown in figure 7.4 and etching with boiling aqua regia removes the photoresist layer before the metal has been etched to the defined pattern. A lift off process was used but this forms ragged edges around the edge of the patterned Pt feature. The edges are sharp and protrude by several microns and may damage the cell membrane of a neuron situated on top of the electrode. This challenge was overcome in the electrodes used in this work by designing the interconnection tracks to be wider than the electrode diameter; the resulting electrode being formed by the aperture in the SU-8 layer. However, this may be problematic when defining small Pt electrodes on the surface of an application specific integrated circuit (ASIC) device. Au can be patterned and etched simply using $KI:I_2$ forming well defined electrode features.

The Pt thin film electrodes present a larger value of c_s than Au which may be useful in the interfacial filter circuit proposed in chapter 6, section 6.4.3 as a smaller value of R_1 is required. This may reduce the circuit area of an ASIC based design as the value of on chip passive resistance is proportional to the consumed area as defined in chapter 3, section 3.4.1. However, the higher frequency dependence of Pt electrodes will reduce the filter attenuation response according to equation 6.25 and produce a higher noise relative to Au for the same electrode area.

For these reasons and especially due to the post processing fabrication issues, Au was chosen as the electrode material for the ASIC device. The following sections develop the investigation into the electrical properties of Au thin film electrodes for the design of an

amplifier input circuit that removes E^0 and low frequency drift without using an input decoupling capacitor.

7.3 Interface Circuit Design using Au Thin Film Electrodes

The input circuit may be designed to satisfy equations 6.19 and 6.22 from chapter 6 using values from the thin film Au model presented in table 7.3. Certain tradeoffs have to be made for the front end designs that are considered in the proposed design rules:

1. The dc offset potential of the circuit, V_{meas} (dc) must be much lower than the differential input required to saturate the amplifier output at the output voltage V_{sat} for the selected gain G_{amp}: $\left|V_{meas}(dc)\right| << \left|\frac{V_{sat}}{G_{amp}}\right|$

2. The high pass filter cuttoff frequency should be lower than the minimum frequency of the neural signal spectrum: $f_{3db} < f_{\min}$

3. The input impedance of the circuit should be much higher than the source impedance of the neural signal: $Z_{neuron} << Z_{input}$

7.3.1 Circuit Design Procedure

As an example, an input circuit is defined for a 50 μm diameter thin film Au electrode using the parameters from table 7.3. If the recommended gain of 57 dB, advised in chapter 5, section 5.6.2 is rounded up to 60 dB and an amplifier with V_{sat} = 1.5 V is estimated for a 0.35 μm process the maximum dc offset of V_{meas} may be defined. For a dc offset at the amplifier output of one tenth of the output range, the dc component of V_{meas} must be less than 300 μV.

The required value of $R_{1,}$ from equation 6.19 may be calculated by rearranging equation 6.19 and substituting in the value of the charge transfer resistance for a 50 μm electrode:

$$R_1 < \frac{r_{ct}/A_e}{\frac{E^0}{V_{meas}} - 1} \qquad 7.7$$

Where A_e is the surface area of the 50 μm diameter thin film Au electrode.

This inequality sets the upper limit for R_1 as 100 MΩ. R_1 must be below this value for this electrode diameter to ensure that the offset will not compromise the amplifiers ability to amplify the signal without causing output saturation.

The second step involves calculating the value for R_1 as part of the input filter circuit, using equation 6.22 and noting the minimum bandwidth of the neural signal. This is defined in the simulations in chapter 5 as being 50 Hz for the Helisoma B19 neuron and 10 Hz for the Aplysia neuron. To ensure that the circuit is designed to keep below this frequency the minimum capacitance and –m value is determined from the mean value of c_0 and –m. The model can be used to design the circuit for a maximum cutoff frequency for a given confidence interval.

The minimum value of R_1 is calculated by:

$$R_1 > \frac{1}{2\pi \cdot c_0 \cdot A_e \cdot f^{-n}} \qquad 7.8$$

The third factor is the source impedance of the neural signal. As shown in chapter 5, section 5.5.2.2 the input impedance of the measurement circuit must be greater than 10 MΩ to ensure that the measured signal amplitude is within 10 % of the cleft action potential (CAP) signal, assuming a maximum seal resistance of 1 MΩ.

From equation 5.18, the value of R_1 may be calculated for a pre-determined gain as:

$$\mathrm{R_1} = \frac{\mathrm{G_{amp}R_{seal}}}{\left(1 - \mathrm{G_{amp}}\right)} \qquad 7.9$$

Choosing a higher value of 5 MΩ for R_{seal}, above the values found in the literature for neurons on planar extracellular microelectrode arrays, the signal amplitude may be measured within 90% accuracy (G = 0.9), giving R_1 = 45 MΩ.

By rearranging equation 7.8 and substituting R_1, the cutoff frequency may be calculated to be 30 Hz. If it is critical that the cutoff frequency is higher or lower the electrode diameter may be reduced or raised to compensate. The design variables are summarised in figure 7.11.

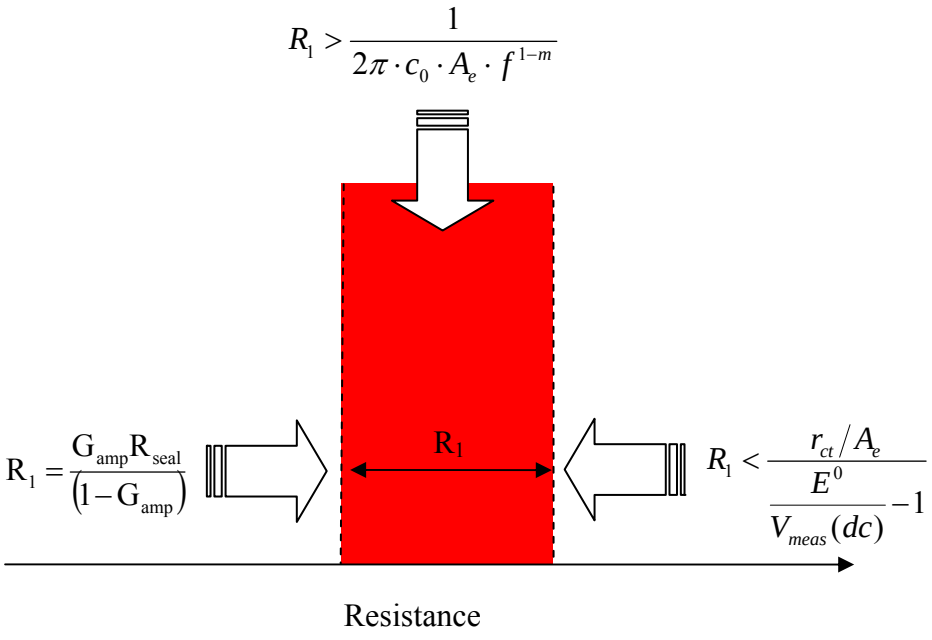

Figure 7.11

Summary of the relationship between pertinent design variables

7.4 Verifying the Electrical Properties of the Interface as Part of an Input Filter Circuit

Firstly, the values of C_s and R_s were measured from a newly fabricated array of Au electrodes scaled in size between 1 mm to 30 μm to verify the assumption that C_s and R_s scale linearly with area. Following this, the circuit in chapter 6, figure 6.8 was considered to verify the design rules proposed in section 7.3. The circuit is tested with a high

performance Burr-Brown INA121 FET input instrumentation amplifier connected differentially to a measuring and reference electrode as shown in the figure 7.14.

The amplifier was chosen due to its high dc input impedance of 1 TΩ, leakage current of 4 pA.

7.4.1 Electrode Scaling

An additional electrode array was fabricated in a two mask process following the method given in Appendix C. The array consisted of a further eight electrodes with diameters ranging from 1 mm to 30 µm. The arrangement of the array is illustrated in figure 7.12. C_s and R_s measurements were again taken between 40 Hz and 100 kHz as described in section 7.2.2 and are presented in figure 7.13 and 7.14. The statistics are presented in table 7.4 with values given in terms of the capacitance per unit area c_s and surface resistivity r_s.

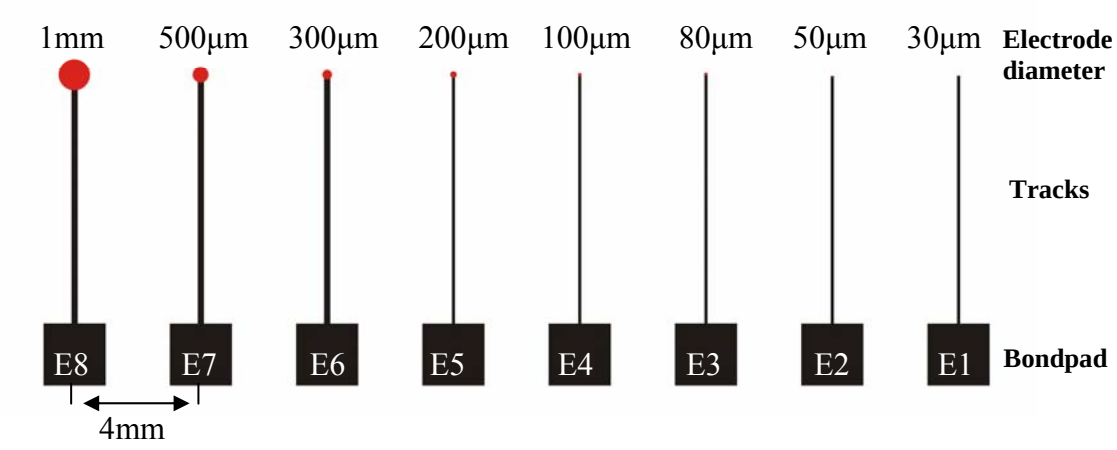

Figure 7.12
Layout of the scaled thin film Au array.

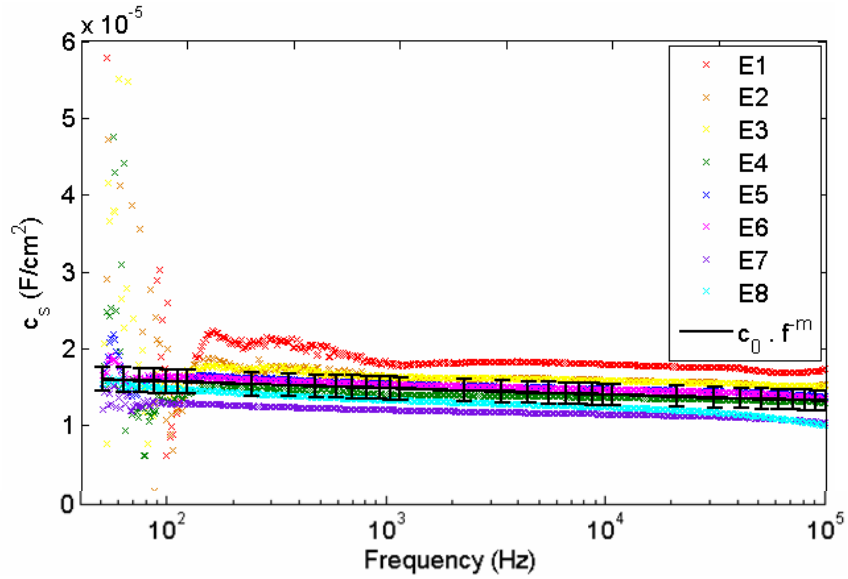

Figure 7.13
Comparison of capacitance per unit area for scaled Au thin film array with model defined in table 7.4. Error bars are to one standard deviation.

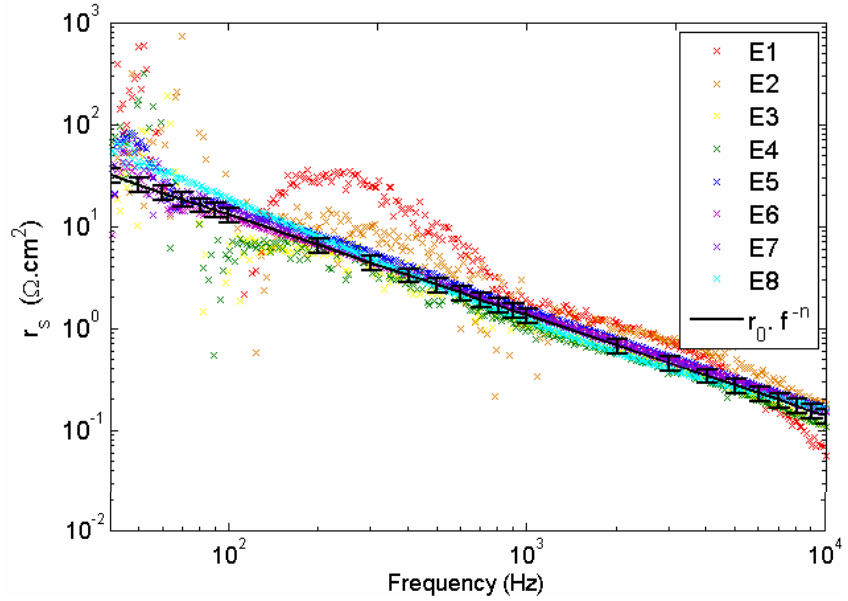

Figure 7.14
Comparison of capacitance per unit area for scaled Au thin film array with model defined in table 7.4. Error bars are to one standard deviation.

Au	c_0 $\frac{\mu F \cdot \sqrt[m]{Hz}}{cm^2}$	r_0 $k\Omega \cdot \sqrt[(1-m)]{Hz} \cdot cm^2$	-m	-n
Maximum	19.206	1543	-0.0417	-0.985
Minimum	14.31	0.957	-0.019	-0.9987
Mean	17.512	1.212	-0.0244	0.986
Std. Deviation	1.731	0.196	0.008	0.005

Table 7.6
Statistical information for the scaled Au array

The values of c_s and r_s are observed to be reproducible with a standard deviation within 10 % of the mean for c_s and 17 % of the mean for r_s. The variance of the measurements between the electrodes does not show an identifiable trend between capacitance per unit area and the electrode area or surface resistivity and electrode area. Thus it is shown that there is a linear scaling relationship between C_s and R_s and the electrode area.

The data for c_s and r_s from the scaled array were compared with the electrode data for the 150 μm diameter electrodes presented in section 7.2.2.2. The values are plotted together for comparison in figure 7.15 for c_s and 7.16 for r_s.

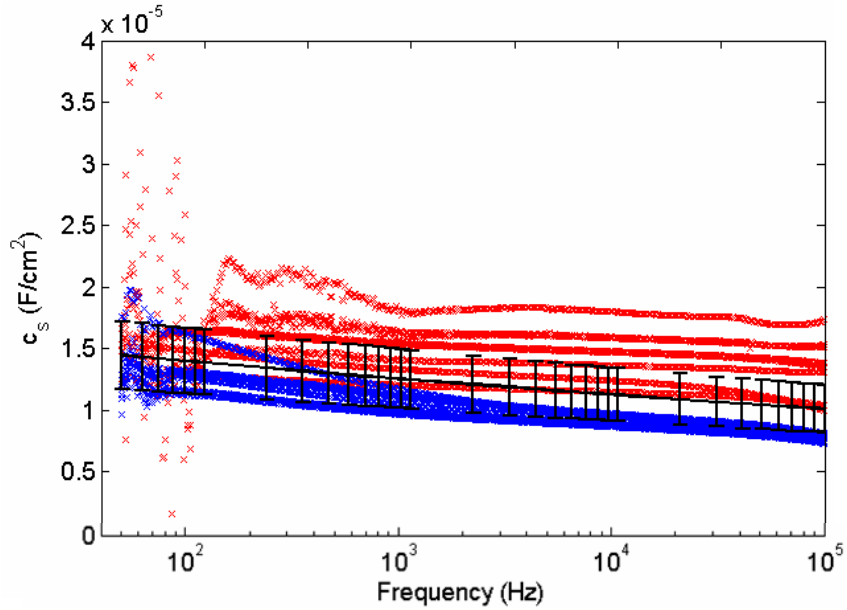

Figure 7.15

Comparison between c_s for the scaled electrode array (red) and the 150 µm diameter electrode array (blue)

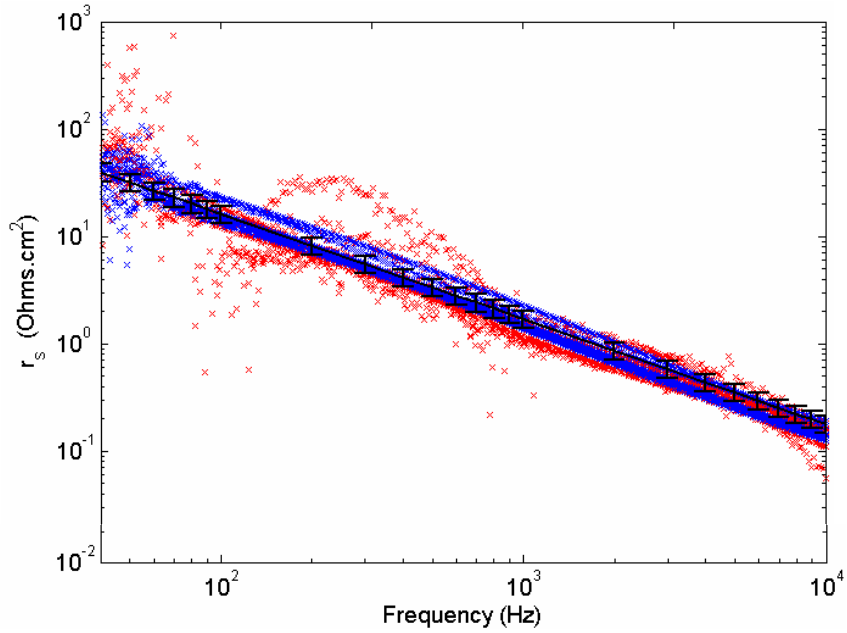

Figure 7.16

Comparison between r_s for the scaled electrode array (red) and the 150 µm diameter electrode array (blue)

The values of c_s and r_s are very similar for both arrays, indicating that for electrodes fabricated by high vacuum vapour deposition and photolithographic techniques show good

repeatability. The combined data was used to update the mean values of the parameters for the model presented in table 7.3. The updated values are presented in table 7.5.

	Au Thin Film (mean)	Au Thin Film (stdev)	Units
r_{ct}	> 5.0	N/A	$M\Omega \cdot cm^2$
r_0	1.46	0.27	$k\Omega \cdot \sqrt[(1-m)]{Hz} \cdot cm^2$
c_0	17.10	3.27	$\frac{\mu F \cdot \sqrt[m]{Hz}}{cm^2}$
-m	-0.0460	0.0182	-
-n	-0.9780	0.0204	-
E_0 vs. SHE	758.90	91.27	mV
$Vn_{thermal} \cdot \sqrt{A_{real}}$	13.45	5.80	$nV(rms) \cdot cm$

Table 7.7

Updated mean parameter summary for thin film electrode model (40 Hz -100 kHz)

7.4.2 Verifying the Removal of the Half Cell Potential

The half cell potential was removed as defined in section 7.2.4. This was verified by measurement of the dc offset using the amplifier circuit shown in figure 7.17. The value of R_1 was modified for several electrode sizes. The thin film Au electrodes from the scaled array were used to make these measurements. Measurements were taken from electrodes with diameters of 1 mm, 500 μm, 100 μm and 50 μm for comparison. Measurements were taken using the arrangement illustrated in figure 7.18.

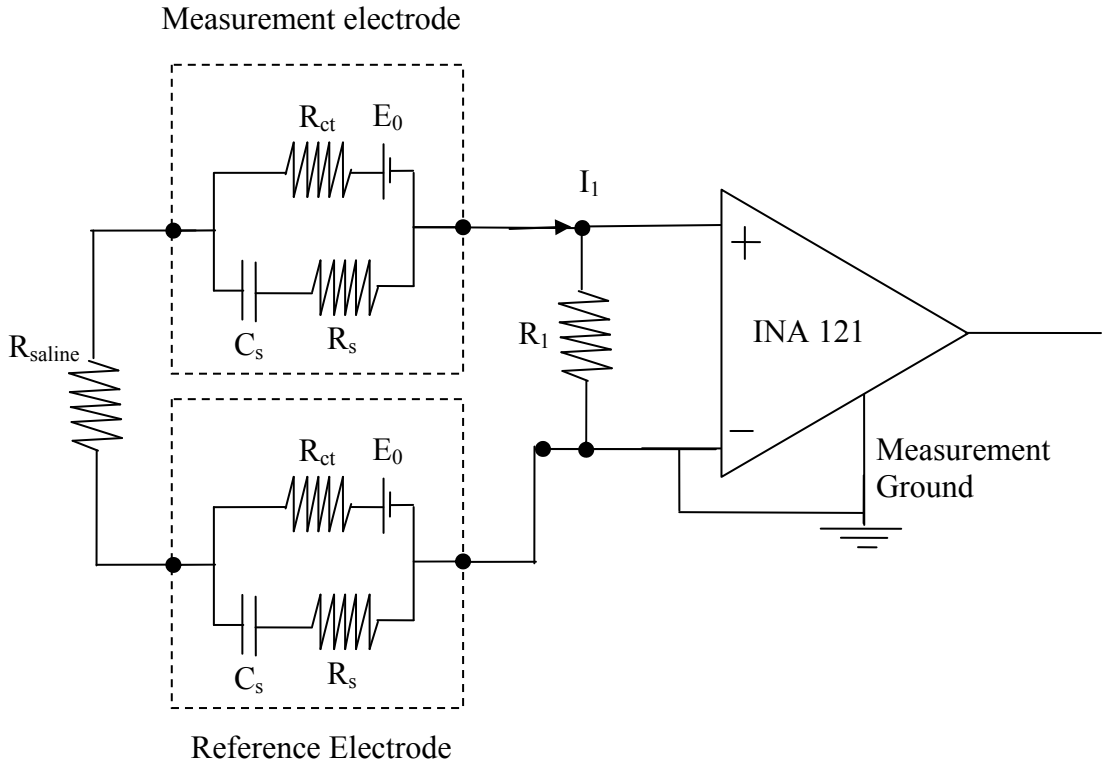

Figure 7.17

The configuration of the circuit

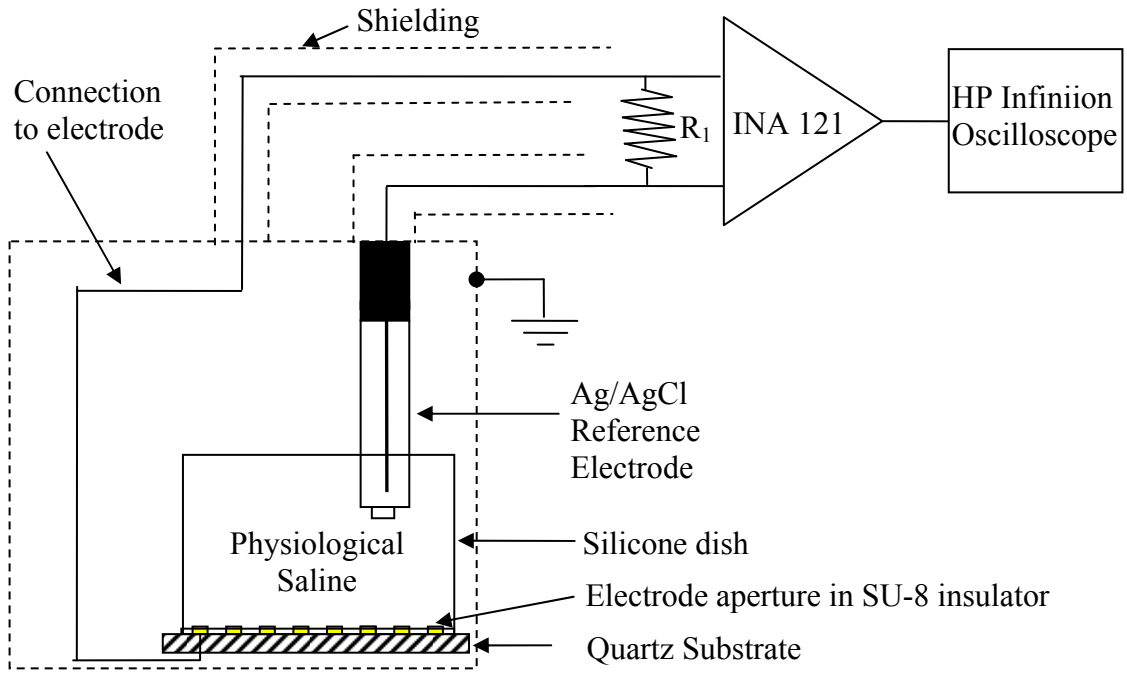

Figure 7.18

Amplifier circuit to measure the half cell offset potential

The op-amp circuit was designed to give a gain of 40 dB to allow a 10 kHz bandwidth and the electrodes were connected directly to the FET input with a manually changeable resistance connected directly between the input nodes. The circuit was connected to an Agilent E3620A power supply and shielded in a grounded Faraday cage. The electrodes were connected by shielded coaxial cable to the device.

The amplifier output was measured by a Hewlett-Packard Infiniion digital storage oscilloscope. Measurements were stored once the signal had visibly stopped drifting on the scope. Ac noise was removed by averaging the signal over 20 ms.

The amplifier and the reference electrode were connected to the power supply reference and the amplifier was powered by ± 5 V.

7.4.2.1 Results

With open circuit measurement ($R_1 \sim \infty$), i.e. by removing the resistor from the circuit, the amplifier saturated to the + 5 V rail. The amplifier output offset voltage was determined by measuring the amplifier output when the input terminals have been shorted. This is subtracted from the values presented. The measured amplifier output voltages for $R_1 = 0$ Ω to 10 MΩ are presented in figure 7.19.

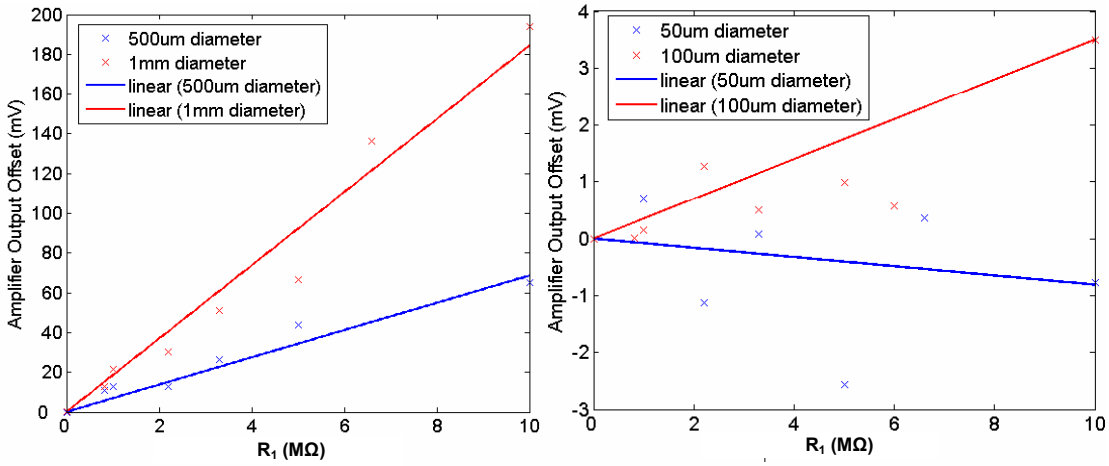

Figure 7.19

Measured amplifier offset potentials for resistances ranging from 0 Ω to 10 MΩ

7.4.2.2 Discussion

The trend in the input offset potential presented by the electrode interface indicates a linear dependence on the load resistance R_1. The input offset potential measured at the 50 µm electrode interface was below the noise floor of the amplifier at all values of R_1 and could not be experimentally determined.

Equation 6.19 from chapter 6, section 6.4.2 was fitted to the potential vs. resistance curves using the value of r_{ct} as a fitting parameter. The equation is repeated here for convenience:

$$V_{meas} = \frac{E^0}{\left(1 + \frac{R_{ct}}{R_1}\right)} \qquad 7.10$$

Linear fits with confidence intervals greater than 95 % for the 1 mm diameter ($R^2 = 0.96$) and 500 µm diameter ($R^2 = 0.951$) electrodes with r_{ct} = 32.5 MΩ/cm^2 and 21.5 MΩ/cm^2 as the respective fitting parameter. The 100 µm diameter electrode fitted to a 17.6 MΩ/cm^2 value of r_{ct} with a confidence interval of 74.2 %. The fitted data is presented in figure 7.20.

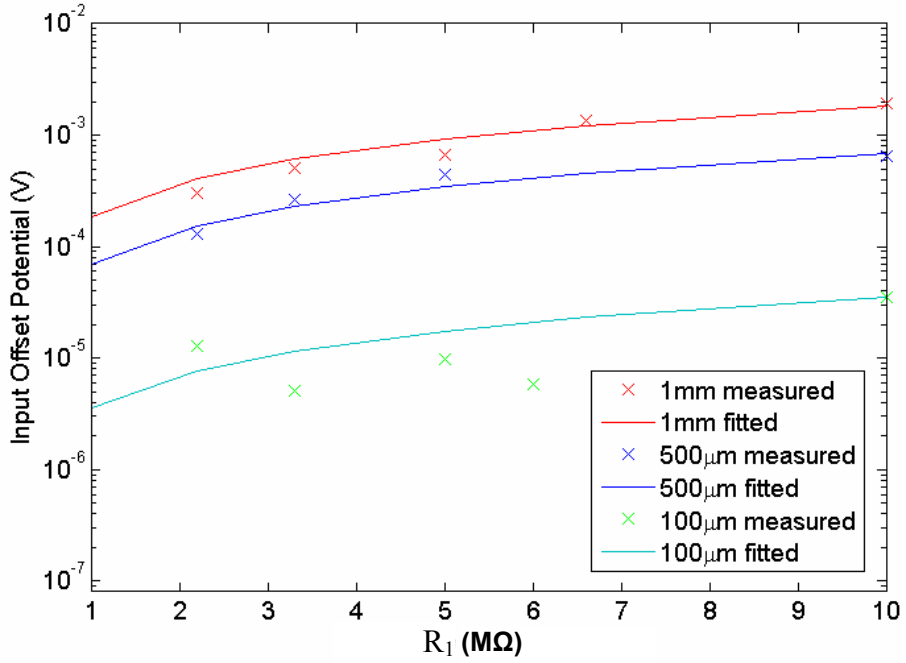

Figure 7.20

Calculated and measured values of input offset vs. R_1

This verifies that the assumption $r_{ct} > 5\ M\Omega/cm^2$ is valid for the model values proposed in table 7.3 and 7.5. The variation in the value of r_{ct} required for the fit is not understood but is assumed to be an artefact of the noise averaging required in determining the values of the offset potential. As the measured value of r_{ct} is greater than 5 $M\Omega/cm^2$, the value may be increased with confidence to a value approaching 20 $M\Omega/cm^2$ in the model for measurements around the electrodes equilibrium potential. This will give greater freedom to the selection of R_1 in the design.

7.4.3 The Filter Response

The filter response was measured using the circuit presented in figure 7.21 using the scaled thin film Au electrode array.

An ac signal was generated by an Agilent 33220A Arbitrary Waveform Generator connected to the saline solution by a 99.99 % pure Pt electrode with a surface area of 2 cm^2. The large surface area was chosen to eliminate the effect of the probes interfacial capacitance C_{ref} and resistance R_{ref} upon the measurement circuit as described in section 7.2.2. The ac signal amplitude was held at 10 mV with 10 kΩ source impedance.

An electrode was connected to an INA 121 instrumentation amplifier with 40 dB gain as defined in figure 7.21 with R_1 presenting the resistance of the resistor-capacitor RC filter circuit. Measurements were taken from the output of the amplifier and stored on a Hewlet-Packard Infiniium digital storage oscilloscope and transferred to PC for analysis is Matlab. The electrical circuit for the experiment is shown in figure 7.22 together with its reduced form. The series capacitance and resistance of the measurement electrode are defined by C_s and R_s. R_{spread} is the spreading resistance of the measurement electrode. An additional INA 121 was connected across the waveform generator to independently measure the signal. The output was connected to the oscilloscope to allow amplitude and phase comparison.

The test circuit was fully shielded from electromagnetic interference. All sensitive wiring was coaxially connected between the amplifier, signal generator and electrolyte dish, which were also shielded during the experiments.

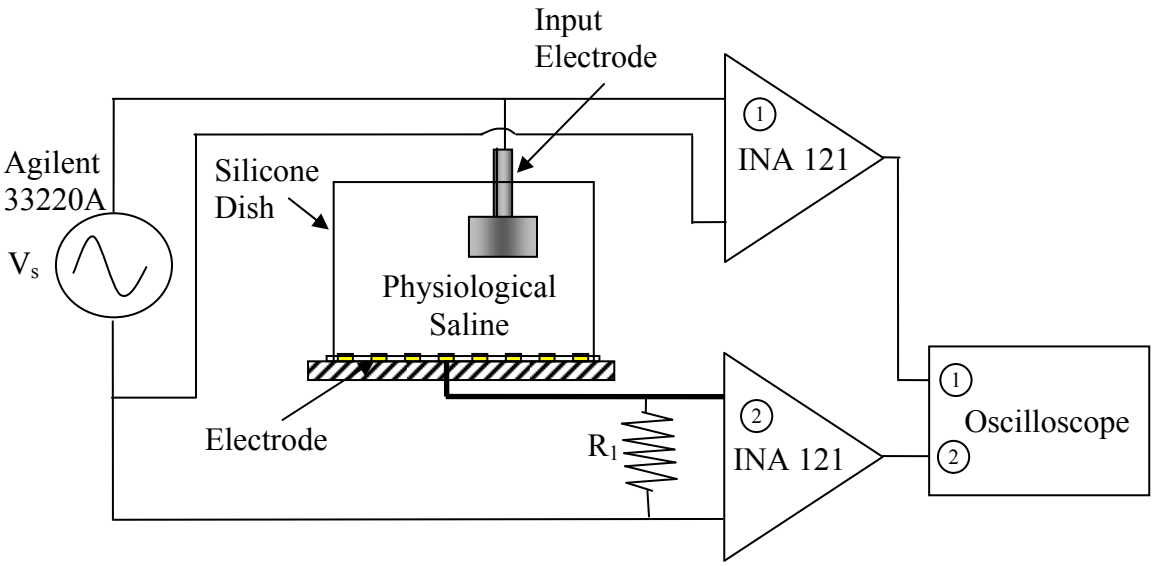

Figure 7.21

Illustration of measurement circuit

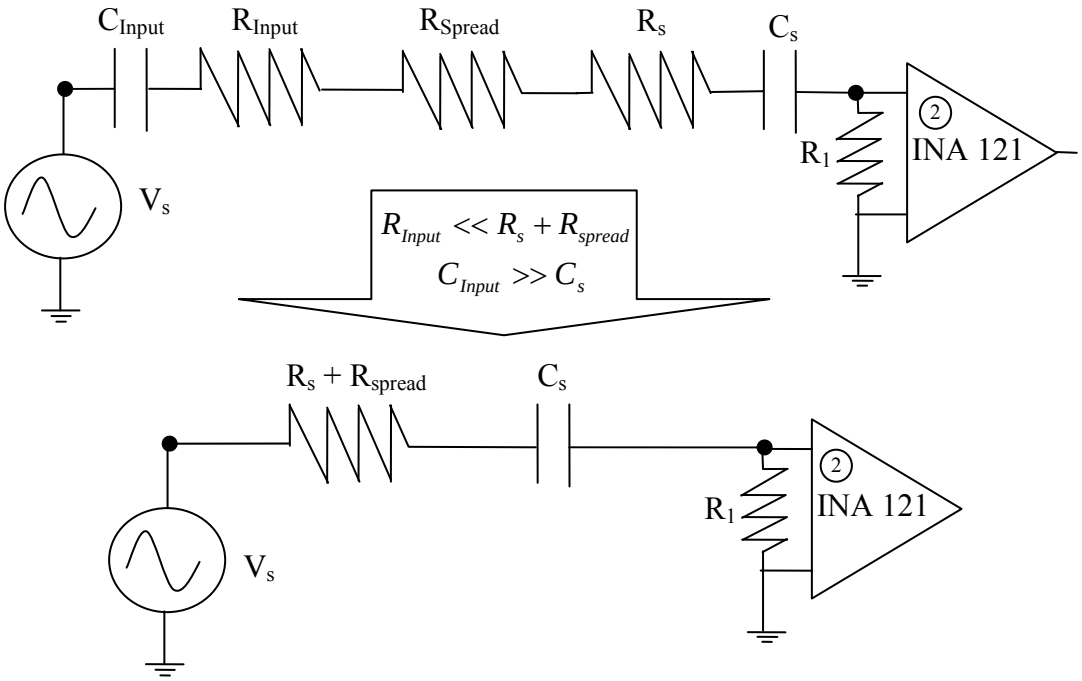

Figure 7.22

Electrical circuit of the experiment arrangement

Measurements were taken from Au electrodes with 50 µm diameter and 30 µm diameter using resistance values of R_1 between 560 kΩ and 10 MΩ. The gain and phase from these experiments are presented in the following section. The phase is of the current through R_1 relative to the voltage of the source signal. The amplitude of the current through the electrode is kept below 20 nA by virtue of the minimum resistance of 560 kΩ. A maximum current density of 900 µA is thus presented at the 50 µm diameter electrode. The circuit response was measured between 1 Hz and 10 kHz which includes the extracellular neural signal frequency range.

Gain and phase were extracted using Matlab code to compare simultaneously recorded and stored digital waveforms from amplifier 1 and amplifier 2 as illustrated in figure 7.21.

7.4.4 Experimental Filter Response

Figures 7.23 and 7.24 present the experimental response of the filter circuit for selected values of R_1.

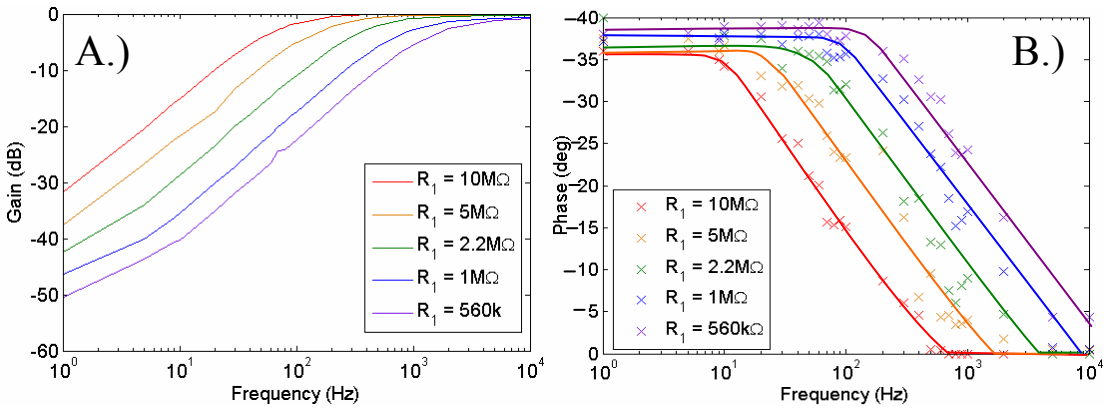

Figure 7.23

A) Measured gain and B) phase of current through R_1, of amplifier circuit input filter for 50 µm diameter thin film Au electrode

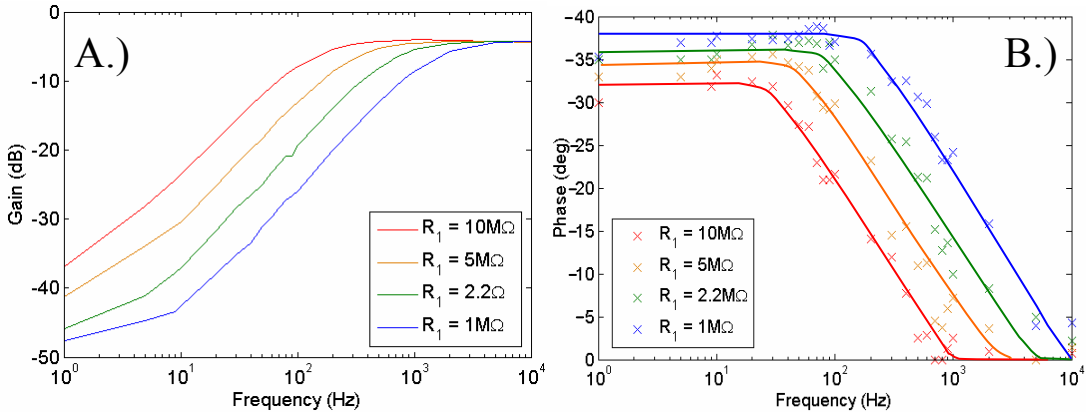

Figure 7.24

A.) Measured gain and B.) phase of current through R_1, of amplifier circuit input filter for 30 µm diameter thin film Au electrode.

The gain response of the 30µm electrode showed a loss of - 4 dB in the pass band. The reason for this has not been determined. The logical reason for this attenuation is that the potential divider, formed by R_{spread}, R_s and R_1, does not have sufficiently large values of $R_{spread} + R_s$ to give – 4 dB.

The filter presents a slope greater than -18 dB/decade at frequencies above 10 Hz as predicted by equation 6.25 in chapter 6. Below this frequency the slope appears to reduce for some of the curves. The apparent lowering of the slope is attributed to augmentation of the measured signal amplitude due to noise and interference. As the signal is attenuated, it becomes similar in amplitude to the noise and cannot be easily compared to the original signal for the gain calculation. An example of this effect is shown in figure 7.25 where the recorded waveforms for the input and output signals are compared for the 30 µm electrode with $R_1 = 1$ MΩ.

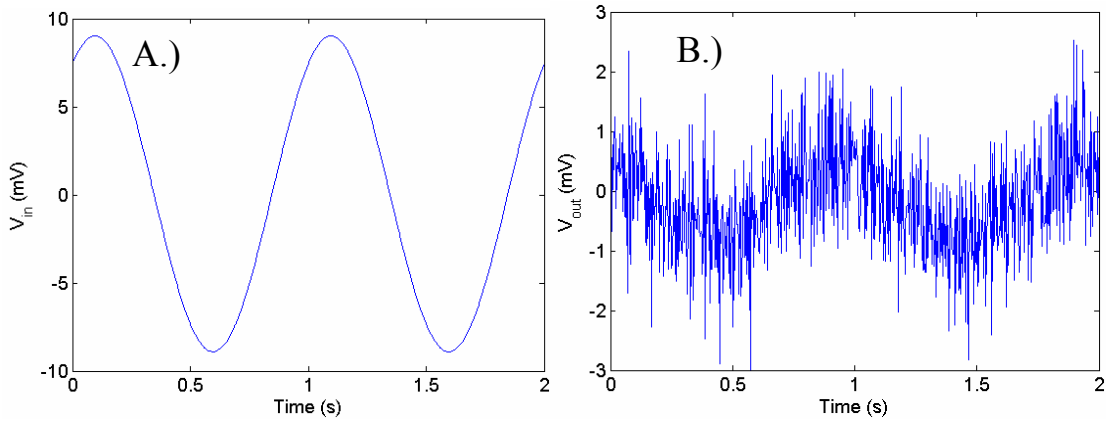

Figure 7.25

Comparison of recorded waveforms for the A.) input signal and B.) output signal for measurements from the 30µm electrode with R1 = 1 MΩ.

As the signal frequency becomes lower than 1 Hz there is no guarantee that the capacitance will remain as predicted by the model. Beyond this frequency, the work of Mirtaheri [5] et al. indicates that for both Au and Pt the interface capacitance will increase as will the frequency dependence factor –m. Schwan et al. have indicated otherwise [7]. As this work uses thin film Au electrodes, that have shown much less frequency dependence than polished wire electrodes, there is no guarantee that the electrodes will behave either way.

For applications where lower cut off frequencies are required, lower frequency measurements of the interface between thin film electrodes and physiological saline would be required.

The phase does not reach - 90° as one would expect in a RC filter implementation using linear passive circuit elements. This is due to the series resistive losses in the circuit resulting from the spreading resistance R_{spread} and the interfacial resistance R_s. The losses occurring due to R_{spread} will not be present for signal measurements at the cleft due to the close proximity of the electrode to the membrane during measurement of the cleft action potential (CAP). For these measurements, it is proposed that the phase will reach the values measured for Au thin film electrodes in section 7.2.2 of below - 80°.

7.4.5 Discussion

The response of the interfacial filter circuit presented by the 50 µm and 30 µm electrodes was compared to the theoretical response to within 2.5 standard deviation as defined by the model in section 7.2.4 and table 7.5. The comparative data is presented in figure 7.26 and 7.27.

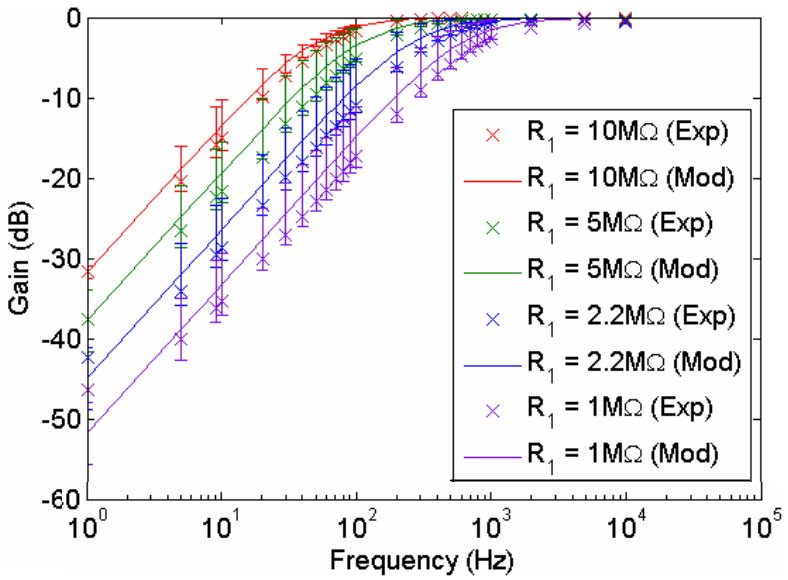

Figure 7.26

Comparison of experimental (Exp) and predicted gain (Mod) response for 50 µm diameter electrode.

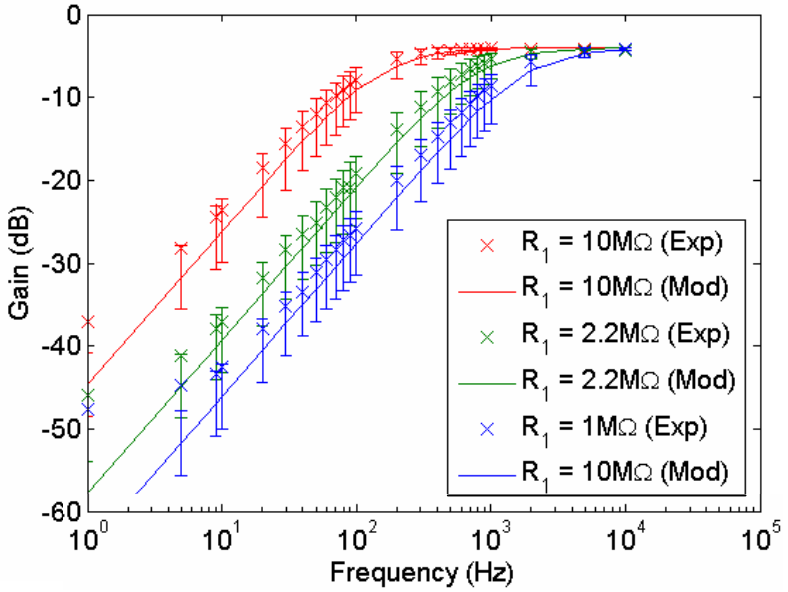

Figure 7.27

Comparison of experimental (Exp) and predicted gain (Mod) response for 30 µm diameter electrode.

Figure 7.26 and 7.27 demonstrate that the amplifier input circuit behaves as predicted by the model. The repeatability of the interface as a predicable circuit element is not as that of linear passive circuit elements, but as long as a cautious design procedure is used the interference from E^0, the low frequency electrode noise and low frequency drift may be removed.

7.5 Discussion

The results presented in section 7.4 demonstrate that by careful selection of electrode materials, electrode diameter and the value of the measurement circuit input resistance R_1, the dc offset and low frequency drift may be removed without the use of an additional capacitor at the circuit front end. This is of great importance to the miniaturisation of integrated neural amplifiers as most of the on chip area in contemporary designs is expended in integrating passive high pass input filter circuits.

The method developed by Wise et al. [7, 8, 9] is verified for thin film Au electrodes. Wise's dc baseline stabilisation method is extended in the design methodology proposed in section 7.3. The new method includes the source impedance of the neural signal defined in chapter 5, section 5.6 and the filter response of the interfacial circuit created by C_s and R_1. The method has been applied to the novel application of minimising the area of the integrated neural signal amplification circuit.

In comparison to contemporary integrated neural signal amplifier array designs, the capacitance per unit area provided by the Au - saline interface is over two orders of magnitude larger than the equivalent capacitance per unit area available from modern semiconductor processes (10 μF/cm² c.f. 100 nF/cm^2). This will further assist in the miniaturisation of the design.

For Au, the charge transfer resistance R_{ct}, is sufficiently large relative to the capacitance C_s, such that the input offset potential is negligible for the cutoff frequency range of interest. This input offset potential is shown to be proportional to R_1 / R_{ct} (section 7.4.2.2). However it should be ensured that the value of R_1 is not below the minimum value required to satisfy

the neural source signal impedance. For the current application, with electrode diameters of tens of micrometers this will not be a concern.

The filter response of the circuit, presented in figure 7.26 and 7.27 is within the 95 % confidence interval (2.5 x standard deviation) of the modelled transfer function response using the electrode circuit model and parameters proposed from new experimental work. This gives confidence that Au thin films will provide predictable values of C_s, R_s, -m and -(1-m) that may be developed into design rules for a compact neural amplifier that exploits the interfacial properties.

Calculation of the -3dB point of the filter circuit response for filter circuit design may be derived from the transfer function presented in chapter 6, equation 6.22. The required RC time constant is shifted by f^{1-m} as may be experimentally characterised by impedance analysis of the intended electrodes. The value of R_1 may be selected according to:

$$R_1 = \frac{1}{2\pi \cdot C_S \cdot \left(f_{-3dB}\right)^{1-m}} \qquad 7.13$$

The values for the electrode model proposed in section 7.4.1 are based on measurements that begin at 40 Hz. For this reason there is no certainty that the slope of the filter response will continue at frequencies below this value. For example the filter response below 1Hz may alter and become less steep due to changes in the interface capacitance. Below this frequency, the work of Mirtaheri et al. [5] indicates that for both Au and Pt the value of c_0 will increase as will the frequency dependence factor -m, as is summarised in table 6.1. Schwan et al. have showed similar experimental evidence for Pt electrodes [7]. Such behaviour is likely to be the result of sorption kinetics. If the value of c_0 is of importance for lower frequency filtering schemes it must be characterised for the electrode surface to be used.

The circuit of figure 7.13 is presented as an effective front end solution for neural signal measurement amplifiers. The method exploits the large capacitance per unit area of the Au-saline interface to provide a high pass filter and remove the dc interface potential. As the circuit utilises the capacitance of the electrode electrolyte interface, it is proposed that

additional linear solid state capacitors are not required in the implementation of integrated extracellular neural measurement circuitry. It was shown in chapter 3 that the removal of these components will significantly reduce the on chip amplifier area. As the interfacial capacitance per unit area is two orders of magnitude larger than that available monolithically for linear passive components, the RC time constant of the filter circuit will require a much lower resistance value than typically used with equivalent solid state capacitors. This offers the opportunity of further decreasing the consumed on chip area required to realise the front end interface circuitry.

It has been shown that the filter performance of this method is strictly non ideal in that it exhibits a lower filter roll-off proportional to the frequency dependence of the capacitance. For Au thin film electrodes this deviation is minimal and represents an 18 dB/decade roll off as opposed to 20 dB/decade expected from filters composed of linear circuit elements.

The circuit implemented using the interfacial capacitance method is also prone to much larger variation in capacitance values than can be achieved with solid state linear passive circuit elements on chip. However, this compromise is outweighed by the usefulness of reducing the area consumed by each device.

7.6 Summary

A simple electrode measurement circuit has been proposed without solid-state capacitors which can remove the dc offset and low frequency drifting potential of the interface. The circuit shows similar performance to a first order solid state high pass filter circuit but with a slightly degraded roll off characteristic. From this, a set of design variables were presented for an electronic neural signal measurement circuit. It is proposed that this circuit configuration may reduce the consumed on chip area of the front end active electrode circuit.

7.7 References

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Chapter 8

Front End ASIC Design

To continue the development of the Active MEA front end, the circuit design presented in chapter 7 was applied to the design of an application specific integrated circuit for fabrication and testing. The active electrode circuit was designed to be fabricated within a standard CMOS process, utilizing standard aspects of the process to form the exposed electrode directly above the measurement and amplification circuit. The amplifier was designed to the criteria of gain bandwidth, and signal source impedance and amplitude as specified in chapter 5 and incorporates the properties of the thin film Au electrode interface, including the thermal noise of the interface. The final area of the amplifier circuit proposed in this chapter is 60 x 60 μm^2, this being below the projected area of the Helisoma B19 , Hirudo Retzius and Aplysia MCC neurons used for the modelling in chapter 5. The amplifier was also designed for low power operation.

Put into context with the design flow of this research, the initial design work presented in this chapter would have followed chapter 5, including the system and ADC structure considered in the following chapter. Circuitry was developed for a neural signal amplifier to condition the projected signal properties predicted in chapter 5 and facilitate optimal signal capture for the system presented. It was at this key stage in development that the initial understanding of the interface between the solid and liquid phases was determined. As knowledge of the interface, the spectral density of the neural signals and the geometric

attributes of integrated circuit design increased it then became important to develop a suitable alternative to the monolithic continuous time filter circuitry required to overcome the non ideal effects the interface may present to the circuit. The basic design of the circuit was halted when it was determined that the circuit size would become much larger than the intended pixel size. The finalising of the design was recommenced following the exploitation of the electrical properties of the interface as defined in chapter 6 and 7.

This chapter combines the design considerations and the development of the amplifier from basic circuit schematic design and simulation to layout design. Common mode aspects of the design are also considered such as the realisation of a common low resistance ground pathway between the power supply, the amplifier and the reference electrode.

8.1 Proposed Structure

The concept of the active MEA was to incorporate dedicated front end circuitry directly beneath the electrode using ASIC technology to remove the shunt impedance and interference susceptibility of passive MEAs. The small neural signal is then amplified above the thermal noise and parasitic losses experienced during signal transmission at the source of electrode transduction. This structure places large restraints upon the realisation of the front end signal conditioning device and the internal connectivity of the integrated circuitry. This defines the need for unorthodox circuit design and utilisation of parasitic effects of the circuit and interface to slacken these demands.

8.1.1 Input Device Structure

Figure 8.1 shows a typical example of the layered structure in which ICs are fabricated and how the active and passive circuit components may be connected. Device interconnection is arbitrarily defined within the metallization layers that are themselves

interconnected by through-layer vias. The four metal layer structure allows a good level of interconnecting freedom within such a device that enables compact circuit designs to be realised. An additional low conductivity connective path for non current drawing nodes is available within the lower insulation layer. This is formed by polysilicon.

Typically the top passivation layers would serve to electrically and hermetically insulate the internal circuitry. For the proposed device these layers will be selectively removed to form the electrode from the top metal. As the top metal is typically aluminium and will corrode within the biological environment it is proposed that it may be coated with Au in an additional non standard processing step.

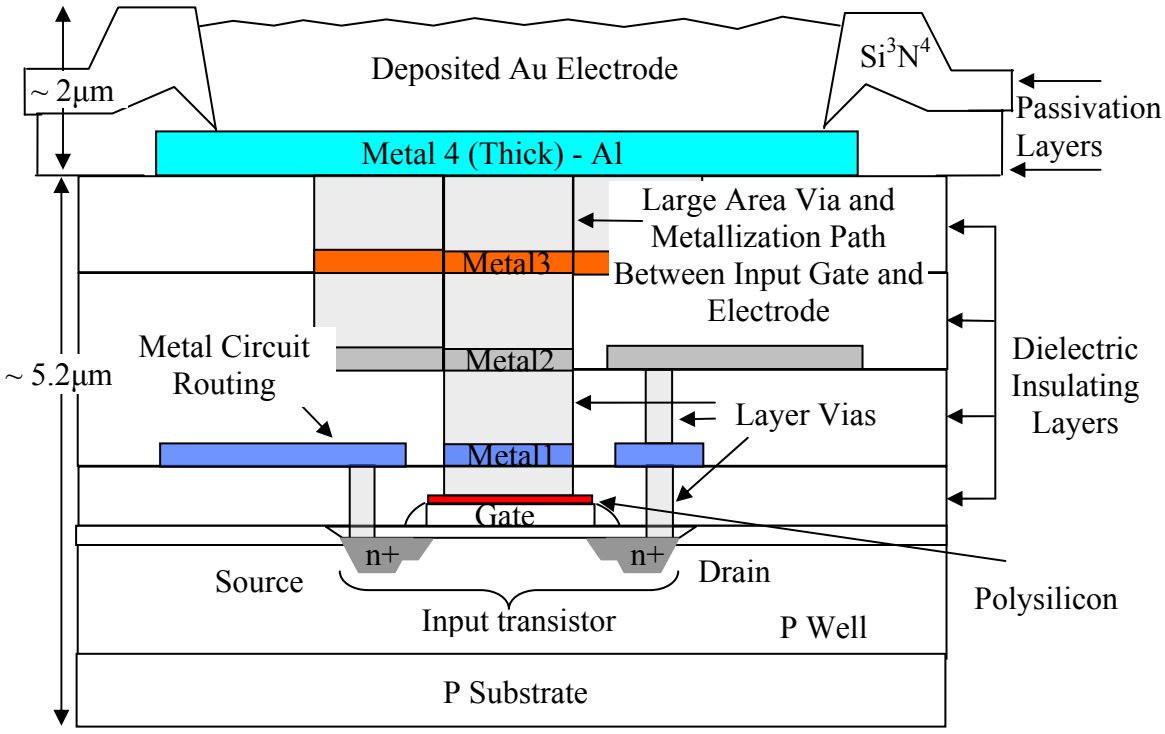


Figure 8.1

Wafer cross section illustrating direct placement of amplifier beneath electrode forming active electrode ‘pixel’. The diagram shows a typical 4 metal process. The layers are not drawn to scale.

As a commercial IC fabrication process will have to be used to manufacture the array, the design must be compliant with the standard process used by the fabrication foundary. Typically, CMOS circuits are structured in layers. The substrate and first layers form the transistor, the next layer consists of the polysilicon used for high impedance tracks and passive components. The following layers define the interconnection metallization layers. For standard low cost processes there are generally no more than four layers. The metallization layers are separated by grown insulation layers that allow overlapping interconnection structures that can be connected together with filed holes or vias that form a conductive pathway between the insulating layers. This allows the formation of functional high density circuit topologies.

By this method a low resistance path may be formed between the electrode and the input transistor of the integrated amplifier. Metallization layers have a typical resistance of 1.5 mΩ/□ and the vias give an additional 1.2 Ω per via of 0.5 x 0.5 μm² area connection. The total path resistance between the electrode surface on top of metal layer 4 and the transistors polysilicon gate will be limited by the lowest area connection between the gate and the electrode surface; that of the vias.

Through the 4 metal layers the total input resistance, R_{in} may be approximated by:

$$R_{in} \approx \frac{4 \cdot R_{via}}{N_{via}} \qquad 8.1$$

Where R_{via} is the via resistance and N_{via} is the number of via connections in the area between the electrode and the input transistor. For a single via stack this would be no more than several ohms, for optimised gate coverage of a 100 μm² gate, this may be reduced to several mΩ total track resistance. This will effectively negate the thermal noise and parasitic contamination experienced by the long tracks of parasitic devices.

8.1.2 General IC Floor Plan

As the IC will be required to provide many recording sites the amplifier circuit must be reproduced in a tiled fashion across the chip. For a one to one electrode to amplifier set up, the amplifier circuitry must optimally consume no more area than that of the electrode and the inter-electrode spacing. Additionally, the device must be supplied with output and supply connections to the output buffers or digital processing placed elsewhere on the chip. For this reason a conservative maximum allowable area of 100 x 100 μm² was set for the chip design and connection routing. This suggested topological constraint would provide for an electrode diameter and inter-electrode spacing each of 50 μm, although electrode size may be arbitrarily decided below or above this level. This is illustrated in figure 8.2.

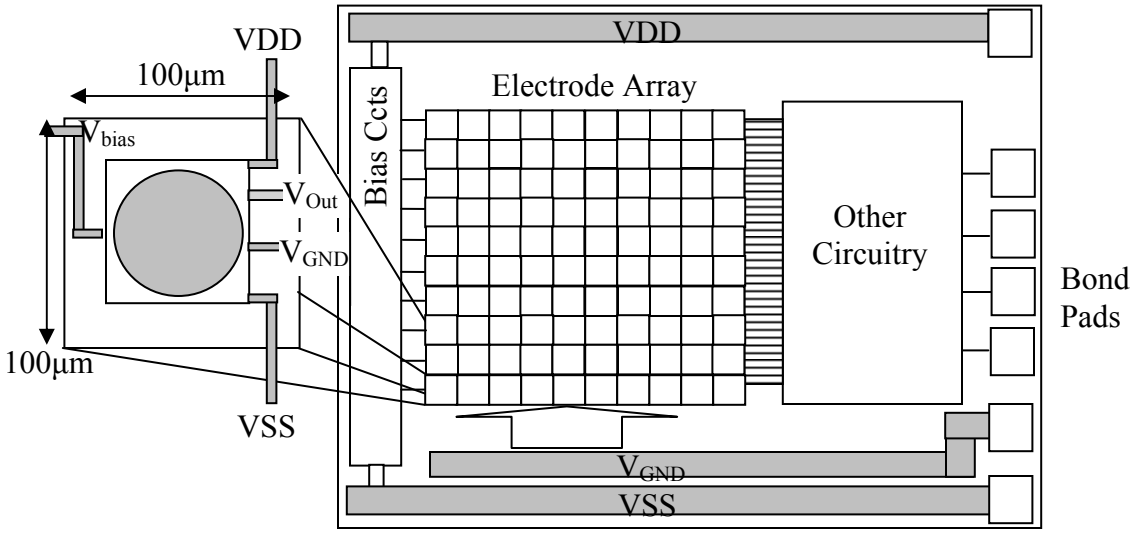


Figure 8.2

First stage conceptual floorplan

As the powering and output of each amplifier is dependent upon the above interconnections the flexibility of the four metal process and the inter device spacing

must be carefully controlled throughout the design to make the concept physically achievable.

8.2 Design Constraints and Topology Selection

The circuit structure to be used with any given circuit design is based entirely upon the given design criteria. Specific amplifier topologies have been developed to satisfy criteria such as high gain, high bandwidth, low power and low noise, amongst other more subtle requirements. However, there is no single analogue circuit that can provide all of these desirable properties simultaneously. In many cases compromise must be accepted, it is the role of the engineer to choose and develop a given circuit to satisfy the requirements of the application.

8.2.1 Summary of Amplifier Design Requirements

The requirements of the amplifier circuit were developed in chapters 4 through to 7 through simulation and experimental work. To summarise these results; beginning with chapter 5 it was determined that the amplifier would need to facilitate a maximum gain of 57dB in chapter 5, section 5.6. It was also determined that the amplifier input impedance must be higher than the cleft resistance according to equation 5.6 so as to preserve the neural signal within a given amplitude error. The amplifier input must also present a low input leakage current to prevent device saturation from the dc IR drop across the electrode interface. The simulations also indicated that a recording bandwidth of 10 Hz to 3 kHz would be optimal to ensure that the amplifier gain spans the spectrum of the extracellular neural signal and removes interference. This will include the frequency spectrum of each of the neuron types modelled in chapter 5.

Chapter 7 indicated that the electrode interface may provide a suitable ‘free area’ of capacitance as part of an amplifier filter circuit under the correct conditions. The capacitance per unit area of the thin film Au interface with physiological saline is over

100 times greater than that of an equivalent monolithic capacitance per unit area, allowing much lower value resistive passives to be used for an equivalent circuit. The chapter also indicated that the electrode polarisation potential could not be assumed to be a perfect voltage source and that the dc offset of the amplifier input signal may be removed by careful circuit design.

In chapter 7 a set of design rules were specified and the removal of the dc electrode potential was verified. The circuit presented in section 7.4.3 was shown to exploit the electrode capacitance as part of a high pass filter circuit. The investigation verified that the circuit demonstrated that a high pass, dc rejecting amplifier could be built without the addition of a monolithic capacitive ac coupled input.

8.2.2 Design Parameters

From the design parameters for extracellular neural signal measurement, the required amplifier was to be designed with a 57 dB gain over a relatively low bandwidth. The amplifier gain achieved in this chapter is 60 dB but this value may be easily reduced at a later stage using a differential input drain coupling method without compromising the performance. This method can also be used to provide a voltage controlled gain. The amplifier must have a FET input for the circuit to have sufficient input impedance and a low input bias current. The amplifier should be configured to not have feedback at the input to prevent current leaking to the electrode. The amplifier circuit must also provide a large value resistance element between the input terminals as defined in chapter 6 to form the input filter. The resistance value should be selected relative to the 10 Hz cut-off frequency and the capacitance formed by the surface area of the electrode according to equation 6.22.

In addition to these signal specific requirements there are also physical requirements that must be adhered to. The device is intended to provide a spatial resolution improvement as well as a signal quality improvement upon the passive MEA. For this reason each

dedicated front end block must be of comparable area to that consumed on the surface by the electrodes and the cell size and density. The amplifier circuit and peripheral interconnection pathways were therefore constrained to an area no greater than 100 µm x 100 µm, and would preferably be much smaller.

Other characteristics of the circuit, such as power consumption must also be incorporated into the design. This is for two reasons; the first being the intention for the device to be used in remote situations for chronic study. For remote *in vitro* and *in vivo* applications where the device would be most useful, batteries would be the most suitable method of power. This would ensure lower noise and high portability. Low power operation would also allow the later development of remote communication methods such as this device is ultimately intended.

The second reason is the thermal effects of heat dissipation. The high density of microelectronic circuits causes cumulative thermal power dissipation within a small area. This is due to the current between each path from source to ground over all integrated circuits. As most of this consumed electrical power will be converted into heat energy, this can be approximated by:

$$P = \frac{\sum_{n} (I_n \cdot V_{dd})}{A} \quad (W/cm^2) \qquad 8.1$$

where:

I_n is the current for each of n paths to ground on the device

V_{dd} is the voltage supply of the device

A is the surface area of the device in cm^2

This thermal by-product of device operation is problematic and may be harmful to the biological cells that are expected to rest upon the surface of the device. For this reason the power consumption per device must be kept as low as possible. This is a problem that does not occur with passive arrays.

The power dissipation strategy of Harrison and Charles [1] was incorporated in the circuit design. This was based upon the *in vivo* observation of Seese et al. [2] that determined a chronic heat flux threshold of 80 mW/cm^2 for muscle tissue from which necrosis and device fibrosis encapsulation may occur over 2 to 7 weeks. Seese also observed a cooling perfusion effect upon the local tissue at lower heat flux densities. Liu et al. [3] observed similar effects for lung and muscle tissue whereby 120 mW/cm² caused acute necrosis. However, for the density required, that of 10^{-3} cm^2, it was immediately clear that an exceptionally low power amplifier would be required. Using equation 9.1 and the maximum heat flux determined by Seese, it was apparent that each amplifier would be required to consume less than 8 μW.

This requires an extremely low operating current point. As the implantable Harrison and Charles device is large and removed from the electrode and thus will not be in direct contact with the measured neurons, its overall surface area and placement greatly reduce the effect the power dissipation may have upon the measured cells. For this reason the implantable device was within the bounds set by Seese et al. was persued with a power dissipation of 80 μW per device. With direct placement of neurons above active electronics it may not be possible to maintain this criterion passively through design; however additional heat sinks / Peltier coolers could theoretically added to the device packaging at a later stage to reduce the concentration of power dissipation. This is a method that was a must in the high density transistor based circuit of Eversman et al. [11] due to each transistor input requiring saturation region operation.

It is difficult to ascertain the effect of concentrated heat flux of the device upon the neurological cells. Typically, for a medially conductive system, such as that of biological matter the temperature spread through the membrane may not occur as evenly as through homogenous material. This may cause ‘hot spots’ within the cleft and any other contained areas between the cell and the substrate. The analysis of such a system is beyond the scope of this work but is nonetheless very important in providing a reliable chronic monitoring device. In this work the guideline value of Seese was adopted and a circuit power consumption of 8 μW was set as the initial design goal of the device.

8.2.3 Amplifier Architecture Selection

From the design outlines above there are several possible amplifier topologies that could be developed for the front end circuit. For reasons of power dissipation and overall device area the device should ideally have as few resistive paths to ground as possible while providing the input circuit function developed in the previous chapter.

The differential current mirror amplifier architecture was chosen. This circuit is suitable as it can be biased for micropower operation. The push pull output stage is ideal for the main gain bock of the amplifier as it requires very little input current and can be designed quite simply to provide an adequate slew rate to drive the capacitive load circuitry following the amplifier. The circuitry provides a good output swing and noise efficiency, adequate bandwidth and gain and requires very little support circuitry for operation. This is in contrast to other possible architectures, such as the telescopic and folded cascode methods, that may require larger, more complex subcircuits for functionality. The differential input was selected as it increases the common mode rejection.

8.3 Circuit Design

The fundamental amplifier circuit was designed as advised in the texts by Allen and Holberg [4] and Martin and Johns [5] and suitable introductory on-line lecture notes for sub-threshold design provided by Harrison [6]. The design was developed for fabrication in the Austria Micro Systems (AMS) 0.35 μm CMOS process.

The first stage of the circuit is driven internally by low impedance nodes. The gain is produced at the second stage from the high impedance configuration of the output nodes. The structure of the amplifier is given in figure 8.3.

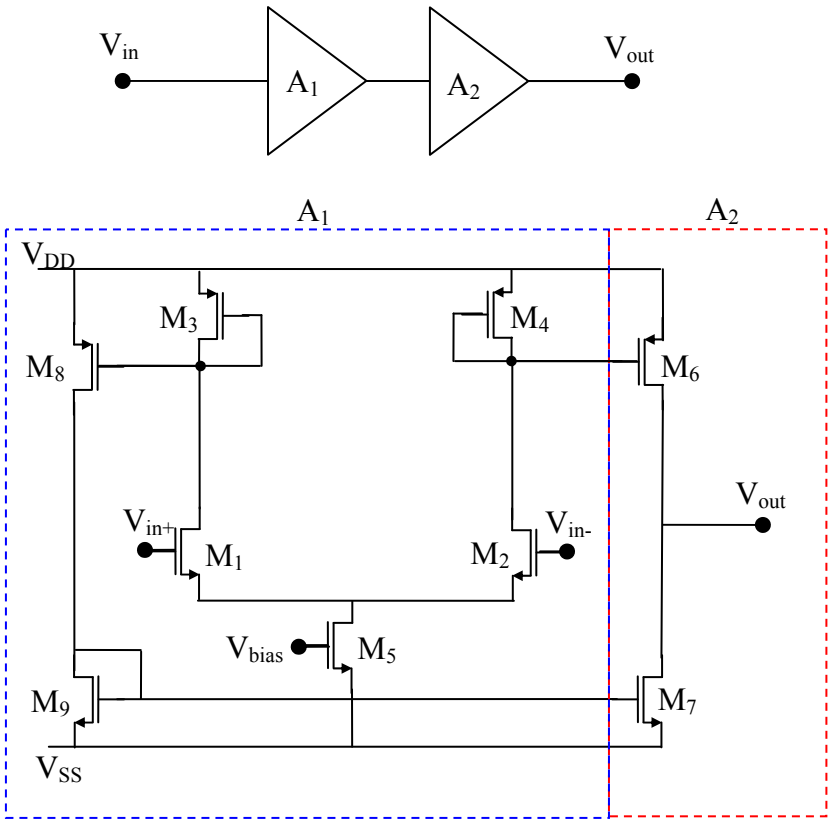


Figure 8.3

Schematic of push-pull current mirror operational amplifier

For this amplifier architecture, the gain is approximated by:

$$Av = A_1 \cdot A_2 = \frac{g_{m2}}{g_{m4}} \cdot \frac{g_{m1}\left(\frac{W_6}{L_6} / \frac{W_4}{L_4}\right)}{g_{ds6} + g_{ds7}} \approx \frac{\left(W_6 L_4 / W_4 L_6\right)}{\left(\lambda_6 + \lambda_7\right) \cdot n_1 V_t} \qquad 8.2$$

Where:

A_1 and A_2 are the first and second stage gains respectively

g_m is the gate transconductance of the transistors; numbered as presented in figure 8.3

g_{ds} is the drain to source transconductance of the numbered transistors

λ is the channel length modulation of the numbered transistors (typically $\lambda \approx 0.01$)

n is the reciprocal of the change in device surface potential relative to the change in gate to body voltage (≈ 0.7).

W and L are the respective widths and lengths of the numbered transistors
V_t is the thermal voltage of the device (V_t = 0.0259 V at 25 °C)

From hand calculations, the device is shown to be capable of gains exceeding 60 dB without large transistor ratios or reaching the performance limits of the circuit. The amplifier structure is also ideal for low power operation as the low impedance current mirror structure requires little internal driving current and the second stage output transistors are configured to slew just enough current to drive the capacitive load of a next stage device. As this next stage will be the MOS gate input of a pre-multiplexer stage buffer the required slewing current will be minimal.

Additional design criteria must also be considered concerning the intrinsic noise of the amplifier circuit within the physical area it will consume. The design must be developed satisfying the gain and noise criteria while holding the resulting transistor areas at an appreciable minimum.

8.3.1 Noise

Noise presented into the system by the active circuit components take the form as presented for the passive circuit elements in chapter 3.

The thermal noise of the above circuit may be derived as:

$$e^2_n(Thermal) \approx \frac{16kT}{3g_{m1}}\left[1+2\frac{g_{m4}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right]\cdot\Delta f \quad (\text{V}^2\text{ rms}) \qquad 8.3$$

Where g_m is the transistor gate to channel transconductance. In the saturation region of operation this may be roughly approximated by:

$$g_m = \sqrt{2K'(W/L)|I_D|}) \quad \text{(S)} \qquad 8.4$$

Where K' is the device transconductance parameter and I_D is the source to drain bias current

As the device enters the subthreshold region this reliance upon W/L is reduced and the resulting g_m equation becomes:

$$g_m = \frac{I_D}{nV_t} \qquad 8.5$$

Where the g_m of each transistor becomes relative.

The limit that this occurs is determined by the equation defined by Enz et al. [7]:

$$I_s = 2nK'V_t^2 \frac{W}{L} \qquad 8.6$$

Where the region of operation is defined by the ratio of the supplied drain current I_D with that of I_S. This is defined as subthreshold for $I_D/I_S < 1$ and strong inversion operation for $I_D/I_S > 10$. Between these two regions a state of 'moderate' inversion exists that is a mixture of the subthreshold and strong inversion characteristics. This region has been empirically modelled by Enz, Krummenacher and Vittoz in the EKV model:

$$g_m = g_{m,sub} G(I_D) \qquad 8.7$$

This gives a fitted response curve between the two regions of operation that is approximately equal to:

$$g_m \approx \frac{I_D}{nV_t} \cdot \frac{2}{1+\sqrt{1+4 \cdot IC}} \qquad 8.8$$

Where IC is defined as the ratio between I_D and I_S.

Thermal noise may be minimised within the allowable area using this model and considering equation 9.2, whereby the thermal noise becomes proportional to the square root of the ratio of the device W/L.

At its worst this noise will be equal to:

$$e^2_n(Thermal) \approx \frac{64kT}{3g_{m1}} \cdot \Delta f = \frac{64kTnV_t}{3 \cdot I_D} \cdot \Delta f \qquad 8.9$$

Which gives $V_{n,Thermal}$ (rms) = 5.228μV (rms) integrated across dc to 10 kHz for a 0.6 μA bias current. At best this noise would become 2.75 μV (rms) for $g_{m1} >> g_{m4} \mid g_{m7}$ for the given bias current, where g_m has been shown to depend with the square root of the W/L ratio in the moderate inversion region.

Other noise may be introduced into the circuit by carrier traps culminating in 1/f or flicker noise. This is by far the most difficult noise to calculate analytically and is generally measured and fitted to the KF design variable in the process documentation. For modern processes this is typically of the order of 10^{-28}.

Flicker noise may be calculated at the input device according to:

$$e_n^{\,2}(Flic\,\mathrm{ker}) = \frac{KF \cdot I_D^{\,AF}}{f \cdot C_{ox}^{\,2} W \cdot L \cdot g_{m1}^{\,2}} \Delta f \quad (\mathrm{V^2\ rms}) \qquad 8.10$$

where:

AF is the dimensionless flicker noise exponent and ranges from 1-2 units.

KF is the empirical flicker noise coefficient in units of $(F/m)^2 \cdot A^{2-AF}$:

($KF_{n\text{-}type} = 2.17 \times 10^{-26}$, $KF_{p\text{-}type} = 1.19 \times 10^{-26}$).

f is the spectral frequency

C_{ox} is the gate oxide capacitance (4.54 fF/μm²)

W and L are the input transistor width and length

g_m is again the device transconductance.

The total input referred noise for each of the presented mechanisms is calculated by integrating the rms noise over the device operating frequency range. The equivalent peak to peak noise voltage level for a 99 % confidence interval that presented at the input of the device is then calculated by:

$$V_{n,pk-pkl} = \left[\sqrt{e_n^{\,2}(Flic\,\mathrm{ker})} + \sqrt{e_n^{\,2}(Thermal)} \right] \cdot 6 \qquad 8.11$$

Values are given for the AMS 0.35μm process as published in the process parameters documentation and defined in BSim3v3 Cadence SPICE Model.

The noise models were considered along with the implications of the EKV model during design.

As the AMS 0.35 μm process has a large intrinsic 1/f noise characteristic and the device is severely area constrained the lowest achievable noise for the given constraints (and other later iterations not covered here such as input offset matching to 0 V) was 4.213 μV (rms). This is not ideal but it was deemed to be close to the best achievable for the process for this particular design situation. To achieve this value the device drain current

was raised to 2 μA (in each amplifier leg) giving a 68 % reduction in the noise from the 0.6μA biased device. A larger drain current was also desirable to ensure that the device area criteria was satisfied as lower bias currents require longer channel devices and larger P to N ratios within the current mirror to ensure a balanced output between the rails. Such sizing demands were found to become too difficult to satisfy for bias currents below 2 μA in the given process.

An alternative device was also developed to minimise the noise of the interface as far as possible with the given fabrication process. A low thermal noise circuit was developed as part of another proposed design that incorporated chopper stabilisation at the device input to modulate the input signal to the high frequency harmonics of the chopping frequency and above the dominant low frequency 1/f noise. This design was published in [8] but was later rejected for the final design due to the concern that inevitable charge injection from switching effects and capacitive coupling to the high frequency chopping signal (± 1.5 V) would introduce additional switching interference at the input. It was also decided that this additional routing and support circuitry would make the design far too complex. The paper is included in Appendix D.

The noise level of the presented device, at 4.213 μV (rms) is lower than the noise for a for a 20 μm diameter thin film electrode as calculated from the electrode noise model value given in table 7.5.

The noise may be calculated as:

$$V_n(rms) = \frac{V_{n,thermal}}{\sqrt{A_e}} = \frac{13.45nV \cdot cm}{\sqrt{\pi \cdot d_{soma}{}^2/4}} = 7.88\mu V(rms) \qquad 8.12$$

The input transistor choice, that of an n-type over a p-type, was made due to the relatively poor $KF_{p\text{-}type}$ exhibited by the AMS 0.35 μm process. Typically, KF can be several orders of magnitude lower for the p-type transistor due to the lower probability of hole trapping within the device. For this reason a p-type input has been favoured in other

low noise input amplifier attempts and is always advisable to minimise the 1/f noise. It was found during the simulation of similar n-type and p-type input devices, performed to validate the above assumptions, that the n-type input device would always provide approximately 5 % less total noise than an equally sized p-type. This was attributed to the fact that the n-type transistor possesses a transconductance parameter 2.9 times greater than the p-type, which not only affects the thermal noise but has a knock on effect upon the flicker noise where the higher gm of the n-type device effectively cancels the improvement provided by the twice lower KP parameter of the p-type device.

From the hand calculations and the requirements laid out in the previous section, a first approximation device was developed. The amplifier was described in netlist form and simulated in Eldo, a commercial SPICE simulation tool. From the simulation results, the device parameters were amended to provide the required gain, power consumption and output symmetry.

The device was then ported to the Cadence graphical capture and simulation platform for more sophisticated analysis with additional circuit components that would contribute to the front end.

8.3.2 Closed Loop Stability and Input Node Biasing

In practice operational amplifiers typically have negative feedback to ensure a constant input offset, predictable gain that is immune to process variations and to fix the gain bandwidth. Positive feedback would drive the output to an unstable state resulting in the input exceeding the output voltage range and saturating the output. The feedback loop may be resistive or capacitive depending upon the application.

The feedback configuration for the amplifier circuit was challenging. Considering the need for the device to have a very low input bias, the device input would ideally require an isolated FET input node without output node feedback currents. An inverting amplifier configuration is not possible with these demands. A non inverting amplifier circuit would

be better suited, however to set the gain to the desired level, a large ratio between feedback resistors or capacitors would be required. Providing such feedback places high demands upon the area of the circuit.

A hybrid feedback circuit was designed to control the bandwidth of the amplifier and increase the stability. An indirect design approach was developed that would provide an agreeable operating bias point, gain control and a fixed 5 kHz upper bandwidth limit without compromising the overall device area and input signal conditions.

8.3.2.1 Upper Bandwidth Limiting

An internal compensation scheme was developed based upon using a small compensation capacitance between the two transconductance stages.

By analysing the small signal response of the amplifier in figure 8.3, the frequency dependent poles may be determined by the response of transistors M2 and M7. The hand calculation equations are presented in the following paragraphs.

A reduced small signal model of the amplifier stages is presented in figure 8.4. In open loop configuration, the frequency response of the amplifier is controlled by poles at:

$$p_2 = \frac{-1}{R_2 C_2} \quad , \quad p_7 = \frac{-1}{R_7 C_7} \tag{8.13}$$

p_2 sets the 3db point and p_7 forms an additional rolloff point that increases the attenuation level to -40dB/decade around the zero gain point.

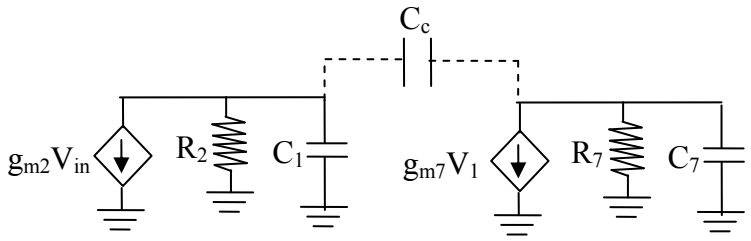


Figure 8.4
Small signal circuit for compensation capacitor

The compensation capacitor C_c, when placed between the drains of transistor M1 and M7, lowers the impedance between the two stages at high frequency. This results in the modification of the system poles to:

$$p_2' = \frac{-1}{g_{m7} R_2 R_7 C_c} \;,\; p_7' = \frac{-g_{m7} Cc}{C_2 Cc + C_7 Cc + C_2 C_c} \qquad 8.14$$

And introduces an additional closed loop zero calculated by:

$$z_{cc} = GB = \frac{g_{m7}}{C_c} \qquad 8.15$$

This results in the movement of p2 to p2'. The new value is closer to the origin of the complex frequency plane by an amount relative to the second stage gain. P_7 moves in the opposite direction to a larger complex value. For large values of C_c relative to that of C_2 and C_7 the bandwidth can be set relative to the new frequency pole at p_2 providing a low pass filter circuit and giving ac feedback to the circuit to improve stability. A 550 fF compensation capacitor was determined within the simulation software to draw the amplifiers 3 dB point to 5 kHz.

8.3.3 Output Current Slewing

The aim of the amplifier is to provide adequate gain, noise and input characteristics to provide optimised amplification for extracellular neural signals, while consuming a small physical device area.

One must consider the output slewing of the device, this being the ability to source enough current to register its output voltage value to the gate of the successive circuit. The micropower operation of the device limits the range at which the device may do this. Slew rate is calculated by:

$$SR = \frac{I_O}{C_L} \qquad \text{V/s} \qquad 8.12$$

For a 2μA output and a typical device input capacitance of 0.2 pF (200 μm x 1 μm gate), this translates to a slew rate of 10 V/μs. To get the most out of the device it must be part of a multiplexed array, which will increase the required performance criteria of the slewing current. For an array with 256 amplifier channels, with each channel sampled at 10 kHz, the amplifier output must slew the signal quickly enough to register the output voltage at the output buffers or digitizing circuit. As an additional requirement in switched operation, the signal must settle well within the switching period. A recommended guideline for settling is 10 times that of the switching frequency.

Considering that the output buffers or ADC input may contribute a load capacitance of up to one pico Farad and that the multiplexer will introduce a path resistance of several kΩ with a transistor channel capacitance of several hundred femto Farads, the load upon the output signal becomes divisive.

From hand calculations it is evident that low power devices connected in a switched array configuration such as this will not provide sufficient output current for high frequency

signal sampling. Thus a dedicated output buffer will be required for arrays larger than approximately ten amplifier channels.

8.3.4 Resolving the Input Coupling Resistor

To achieve an RC filter circuit between the electrode interface and the device, an input coupling resistor must be realised.
The input circuit discussed in chapter 7 uses a resistor R_1, connected between the input terminals to form the circuit presented in figure 7.22. The value of this resistor is dependent upon the high pass cut-off frequency required for the device and the material and geometric properties of the electrode.

It was decided that for the prototype chip design, the MEA electrode model given in chapter 7 would be used to define the input electrode capacitance for a 20 μm diameter electrode. The required internal resistance value was calculated using equation 7.8 and values from table 7.5 for a cut-off frequency of 10 Hz.

$$R_1 > \frac{1}{2\pi \cdot c_0 \cdot A_e \cdot f^{-n}} = \frac{1}{2\pi \cdot 17.1\mu F \cdot \pi \cdot \left(10 \times 10^{-4} cm\right)^2 \cdot 10^{0.975} Hz} = 313.2 M\Omega \qquad 8.13$$

The formation of an integrated resistor of this magnitude would be impractical. Similarly, a transistor based MOS-R resister would more area than allowed in the design specifications for the entire amplifier circuitry.
For this reason a subthreshold MOS-R resistor was implemented in the moderate inversion region.

The resistance of a subthreshold MOS-R is calculated by:

$$R_{MOS-R} = \frac{1}{g_m} = \frac{V_T}{\kappa I_D} G\left(I_D\right)^{-1} \qquad 8.14$$

Where V_T is the switching threshold voltage of the transistor and $G(I_D)$ is calculated by:

$$G(I_D) = \frac{1 - e^{-\sqrt{\frac{I_D}{I_S}}}}{\sqrt{I_D / I_S}} \qquad 8.15$$

Where I_S is calculated by equation 8.6.

The resistance value calculated in equation 8.13 is provided by an n-type transistor of 10 μm width and 10 μm length with a bias current of 615 mV supplied by V_{bias2} in the circuit proposed in section 8.3.5.

As the resistance is voltage controlled there remains the possibility of combining the bias control to an ancillary circuit for a variable controllable cut-off relative to the device transconductance characteristics. This feature was not pursued in this work.

8.3.5 Biasing

To overcome the problem of output offset the device was designed to operate around a symmetrical input bias point relative to the positive and negative power supplies. The bias point was referenced directly to the power supply and the ground electrode (+ ve amplifier input node) to maintain the operation bias point of the amplifier when in contact with the electrolyte. Symmetrical biasing was achieved by sizing transistors M7 and M6 and the tail transistor M5 to give an equal g_m for the output pair.

The Bias circuitry is a very important part of the overall amplifier design. For the amplifier to operate as intended around a stable operating point it must have a current or voltage reference point that maintains the quiescent current flow through the transistors. Ideally such a circuit should be totally independent of any internal or external influences.

The importance of setting this bias point has led to many novel and complex methods to achieve a stable bias point and reduce the dependency of the circuit upon power supply, temperature and fabrication mismatch.

The circuit described in section 8.3, requires a single bias reference. This was provided using the circuit drawn in figure 8.5. The circuit in the figure includes solder dots to prevent confusion regarding the connection of nodes in the circuit. The circuit structure is commonly known as a beta multiplier bias and is moderately resilient to power supply and temperature variations. Although not as sophisticated or parameter independent as many models, this circuit provides a good reliable current source through M_6 that is controlled by the current flowing to ground through R_{ref}. The circuit uses positive feedback to control the bias current. The reference current may be calculated according to:

$$I_{ref} = \frac{2}{R_{ref}{}^2 \cdot Kp_n \cdot \frac{W_5}{L_5}} \left(1 - \frac{1}{\sqrt{\frac{\beta_7}{\beta_5}}} \right)^2 \qquad 8.16$$

Where β is Kp.W/L for the numerated transistor of interest. The calculation is mathematically independent of the supply voltages.

The bias circuitry includes a start up network that guarantees that the device will be pulled to the desired operating level when powered up.

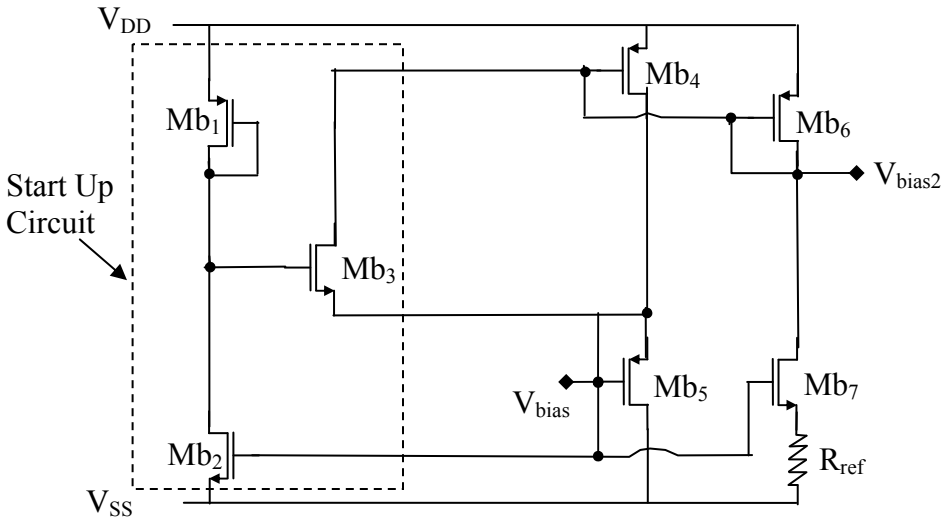


Figure 8.5

Amplifier bias circuit

The transistor M6 forms a current mirror with transistor M5 in figure 9.3.

Device	W/L (μm)
Mb1	10 / 100
Mb2	10 / 2
Mb3	10 / 1
Mb4,Mb6	30 / 2
Mb5	200 / 1
Mb7	100/1
R_{ref}	0.8 / 1100 (100 kΩ rpoly2 – snaked)

Table 8.1

Bias circuit design variables

The bias circuit consumes an area of 55 x 123 μm² and dissipates 212 μW of power.

8.4 Simulation Based Design

The Cadence analogue circuit design and simulation package is the industry standard for mixed signal device design and fabrication mask generation. The software provides prediction of device behaviour using SPICE and higher order device characterisation. The device was designed to be manufactured in the AMS 0.35µm. The AMS foundary provide a custom bolt-on software package known as the AMS-HIT KIT that allows the user to model and adjust the schematic circuit transistor widths and lengths to a process specific predicted response that will operate to within a narrow tolerance level. The process variations may themselves be modelled as worst and best case corners to provide confidence in the final performance characteristic range of the device. With careful design, following the stringent design rules of the process, the physical device has the best possible chance of performing as required.

The final transistor sizing regime is listed in Table 8.1 with reference to figure 8.6 and the general device performance results are summarised in Table 8.2. A plot of the gain-frequency performance is presented in figure 8.8. This was measured using the testbench circuit in figure 8.7. The bias circuit is omitted for clarity.

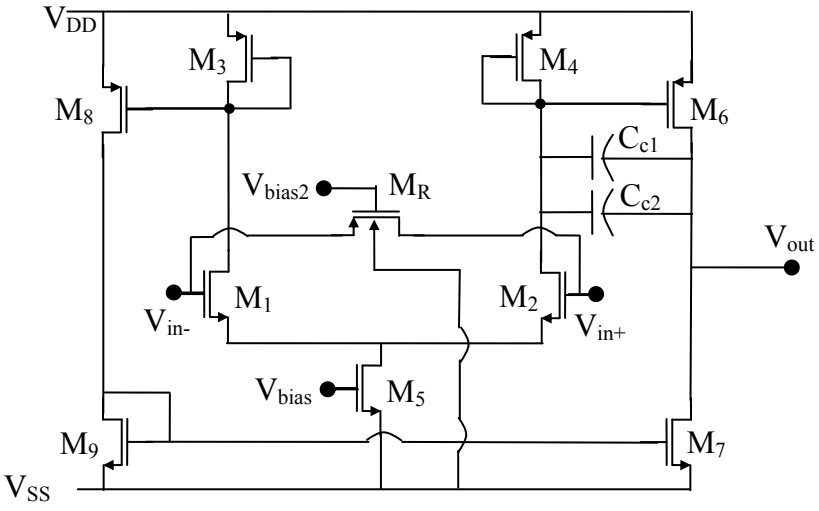


Figure 8.6

Final amplifier circuit schematic

Device	W/L (μm)
M1,M2	100.0/1.2
M3,M4,M6,M8	15/2
M7,M9	34.3/1
M5	10/1
MR (320 MΩ)	10/10
C_{c1} (350 fF)	16/24.9
C_{c2} (200 fF)	16/14.2

Table 8.2

Table of Device Sizes

Design Parameter	Value	
Area	64 x 54 μm²	
DC Gain	62 dB	
Power Dissipation	26.4 μW	
3dB point	4.95 kHz	
DC offset	400 μV	
Headroom	±0.7 V	
Noise (100Hz-10kHz)	4.509 μV_{rms}	
Process Variation Effects (Operational Corners)	Gain (dB) ± 2.25	Filter Corner
	Output offset ±75 mV	± 2 kHz
PSRR (1Hz-600kHz)	41 dB	
CMRR (1Hz-100kHz)	75 dB	

Table 8.3

Simulated device performance results

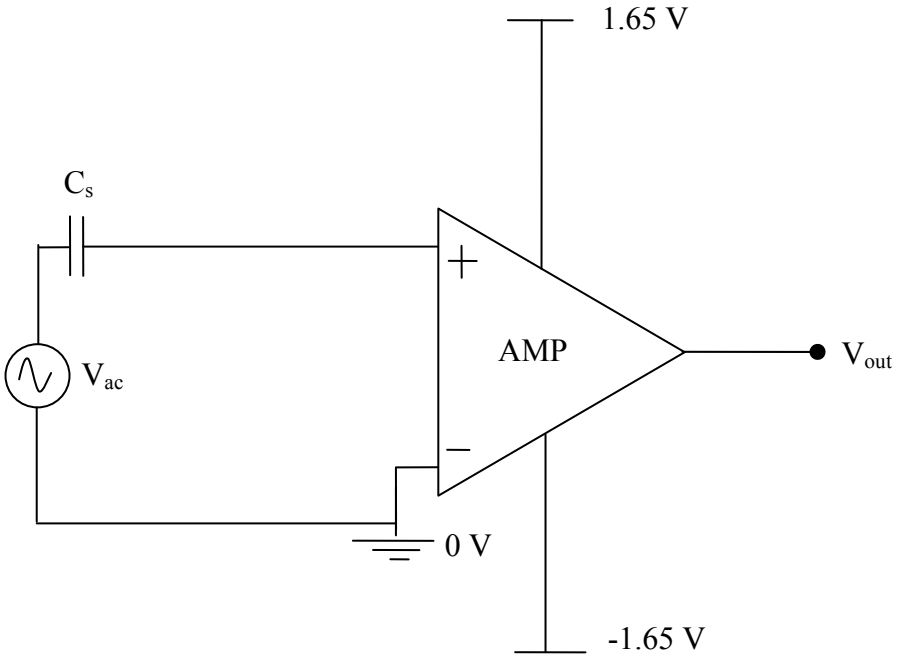


Figure 8.7

Amplifier testbench circuit configuration as simulated in Virtuoso

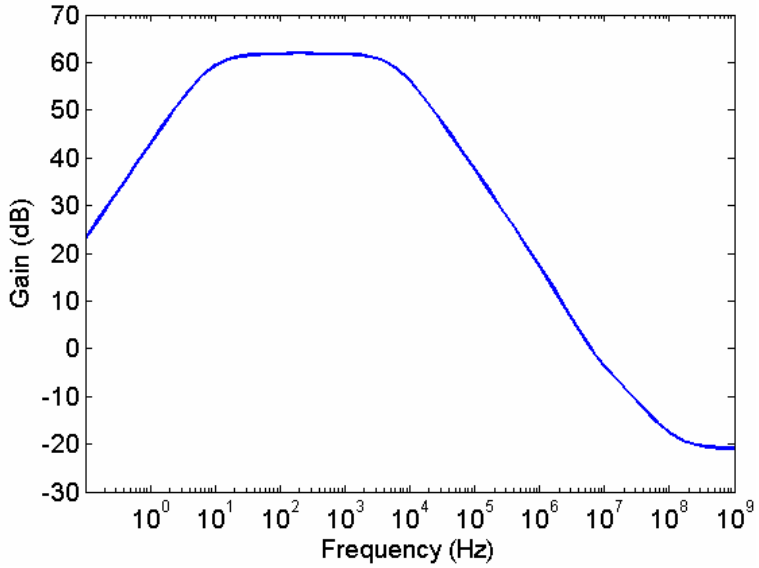


Figure 8.8

Gain performance of amplifier between 0.1 Hz and 1 GHz using Cadence AnalogLib with a linear input capacitance of 50 pF for C_s

8.5 In-Situ Circuit Simulation

The behaviour of the finished circuit design was verified for the intended application by simulation. This was performed in SPICE using the Cadence Virtuoso package. The amplifier designed in this chapter was ported over to the neuron SPICE model and placed according to figure 4.12. The circuit was tested for the Helisoma B19 and Aplysia MCC neuron SPICE models developed in chapter 5 with R_{seal} = 100 kΩ. The value of R_{ct} was modified to determine its effect upon the circuit's removal of E^0. The simulated amplifier output signal was observed for distortion against the CAP signal simulated with infinite measurement impedance. Figure 8.9 shows the amplifier connection to the SPICE model. Figure 8.10 shows the response of the simulated Helisoma B19 neural signal and Figure 8.11 shows the response of the simulated Aplysia MCC neural signal.

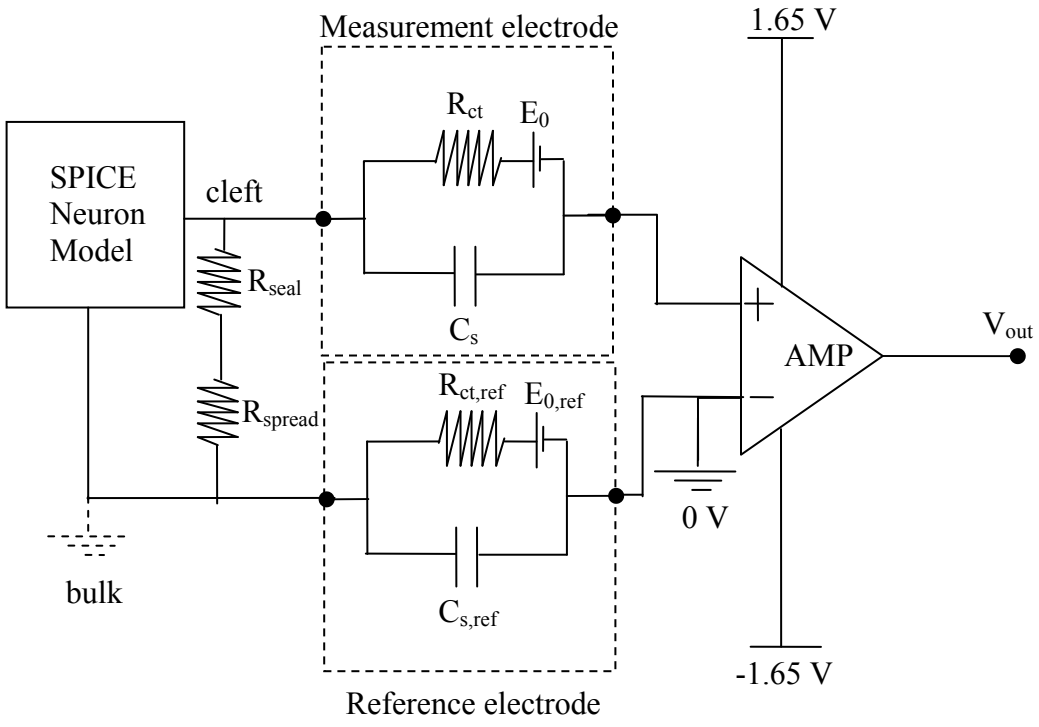


Figure 8.9

Testbench schematic for connection between the amplifier and SPICE model

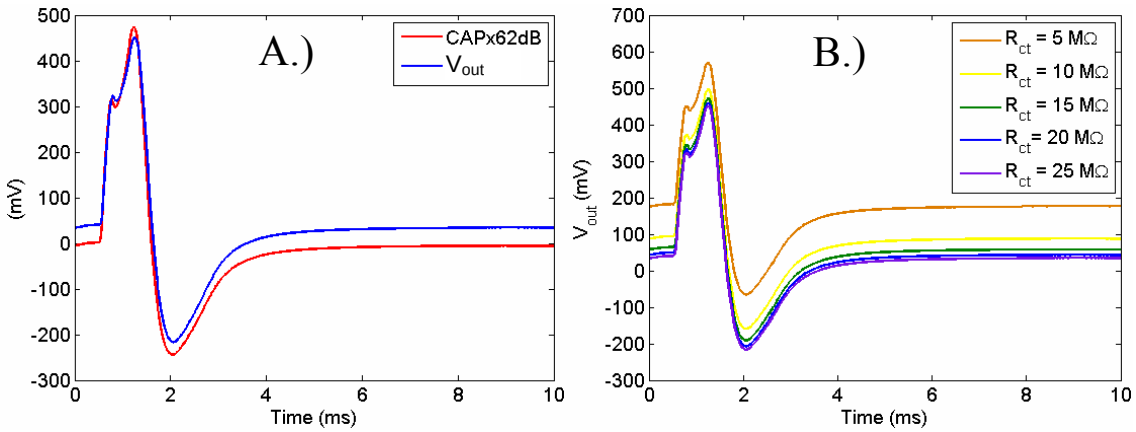


Figure 8.10

Simulated response for Helisoma B19 neuron model. A.) shows the comparison between the CAP signal (multiplied by 62 dB) and the amplifier output. B.) the effect of varying R_{ct} within the model upon the dc output offset voltage.

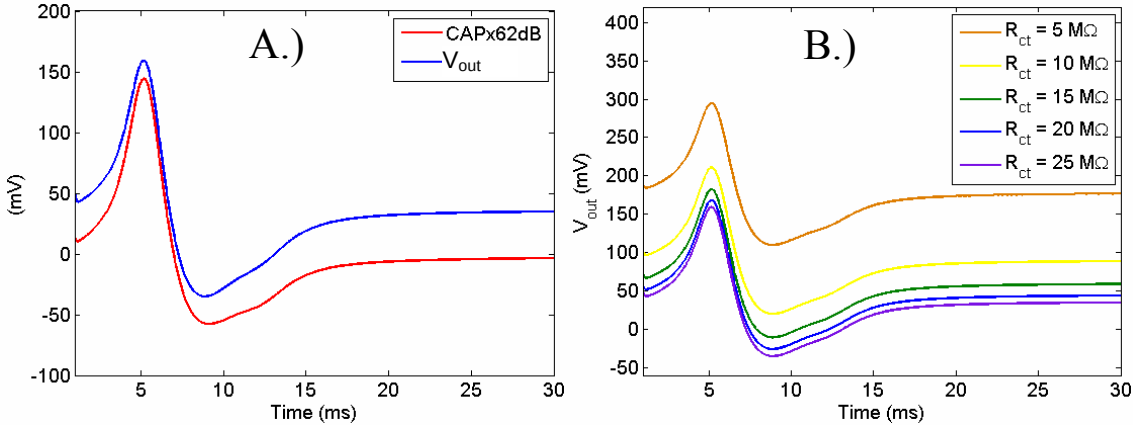


Figure 8.11

Simulated response for Aplysia MCC neuron model. A.) shows the comparison between the CAP signal (multiplied by 62 dB) and the amplifier output. B.) the effect of varying R_{ct} within the model upon the dc output offset voltage.

8.6 Circuit Layout

The schematic design of the amplifier circuit must be realised in terms of physical geometries that define the operation and connectivity of the transistor and passive devices. The layout stage is a very important step in the design process and involves the

formation and interconnection of the devices on a planar silicon substrate according to the deposition of the relevant materials and the strict observation of the fabrication design rules. Fortunately these steps are assisted by computer software that aids the design process on-line rule checking and assisted generation of the more complex devices (P-Cells). The layout tool Layout-XL was used as part of the Cadence Mixed Signal Design Suite to develop the design from schematic to device generation, placement and routing and back-annotation for verification and geometry based parasitic control. This was used in conjunction with the AMS HiT-KiT v3.60 to ensure compatibility with the fabrication house. The iterative procedure of design and layout is summarised in figure 8.12.

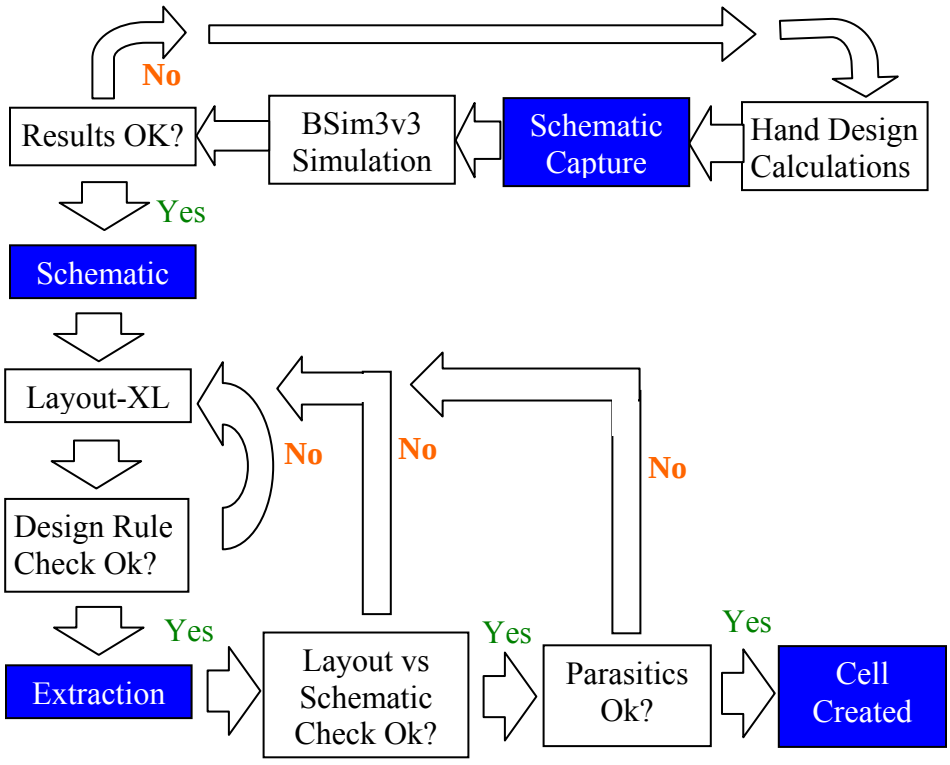
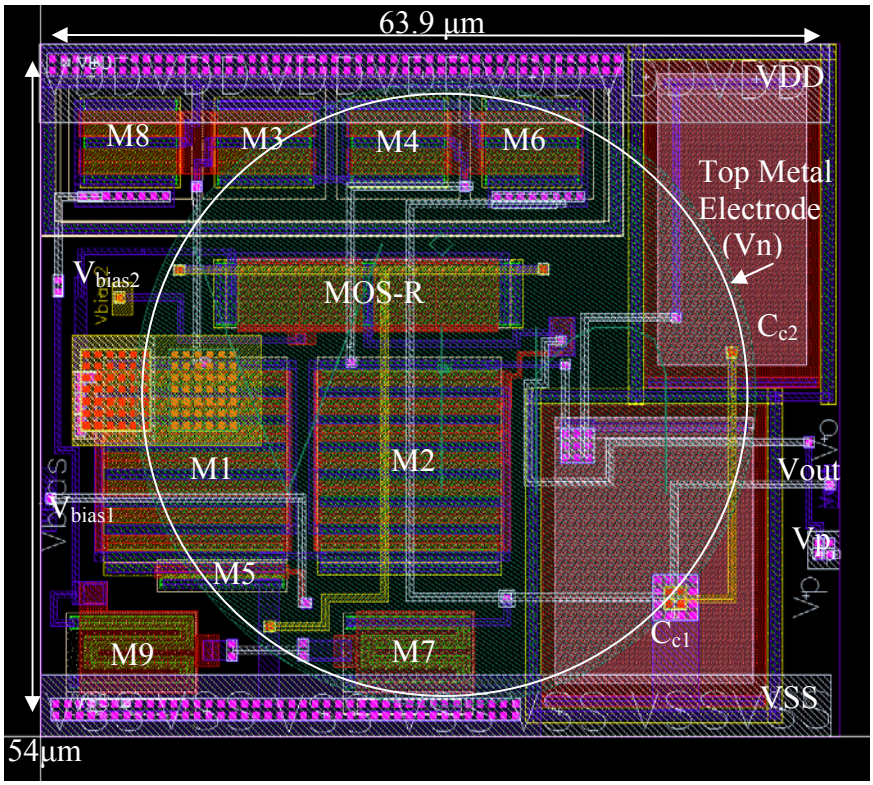


Figure 8.12

Analogue circuit design and layout flow

Following these design stages the amplifier and bias circuitry was transformed from a simple schematic design to the final layout cells. The cells are presented in annotated form in figure 8.13 with the input pins, output pins and devices labelled for reference to figures 8.5 and 8.6.

A



B

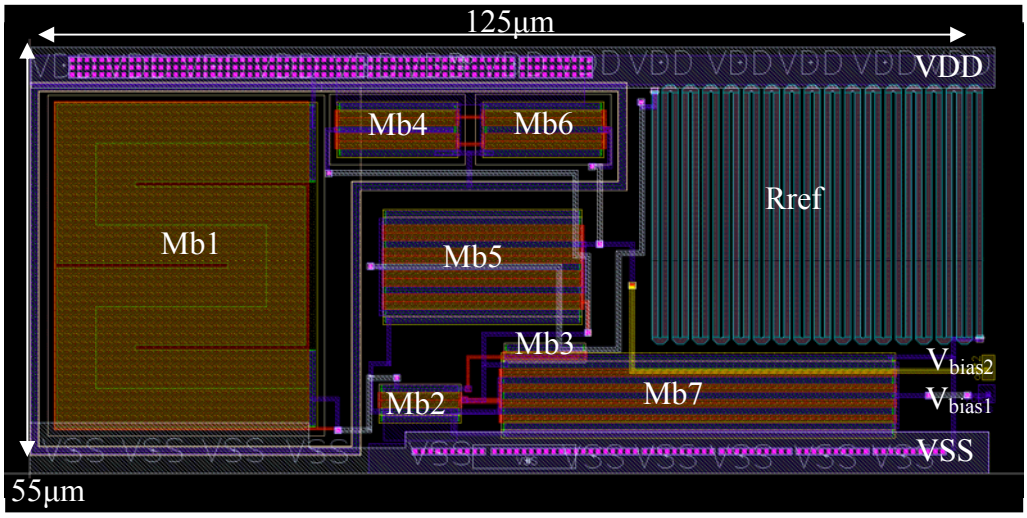


Figure 8.13

Front end device layout: A.) Input amplifier, B.) Bias circuit

The amplifier circuit consumes an area of less than 3.4 x 10^{-3} mm² (63.7 μm x 54 μm) and the bias circuit consumes 6.82 x 10^{-3} mm² (124 μm x 50 μm). The bias circuitry may supply several amplifiers during operation spreading its large equivalent area consumption and power dissipation over several devices.

8.7 Discussion

The integrated circuit design presented in this chapter represents the culmination of the investigative work described in the first two parts of this thesis. By sacrificing the use of large passive circuit elements as part of the device design and using a compact current mirror amplifier topology the device was realised within an area comparable to a large neurological cell. This small size will allow the device to be used as the front end of high density neural signal measurement arrays, where the electrode may be integrated directly above the device on the process top metal for direct coupling with the cell.

To achieve this level of compact design the amplifier was stripped down to the bare minimum size and feedback compensation. This will inevitably cause gain variation between devices greater than may be expected with resistive feedback methods. The gain may also drift as the amplifier ages and output offset voltages ranging in mV may also be observed between devices during operation. These problems are in general not disastrous to device operation and may be resolved, if necessary at a later stage by external calibration.

More problematic is the disobliging relationship between the device area, power density and noise. The compact area of the device dictates the need for microwatt power; unfortunately the device input referred noise is inversely proportional to both the area and supply current. Lower currents generate more thermal and flicker noise due to reduced device transconductance and higher drain to source resistances. Similarly, smaller areas also reduce achievable transconductance and increase the devices susceptibility to flicker noise and reduce the ability to design balanced current mirrors. For this reason, an

optimal input referred noise that was less than the predicted interface noise was not possible within the given area. Also the final design indicated a 26.4 μW power dissipation that is over 3 times the level determined safe for tissue contact. This was a difficult decision during the design as the main point of the active electrode is to present a more versatile, less obtrusive solution to the passive MEA. Further issues with device design, output transistor current matching and predicted slew rates demanded that the bias current be raised to a more workable level. It is believed that although the recommended power density threshold has been exceeded, this prototype is being developed as a proof of concept device that may be refined at a later stage. It is assumed that the heat density issue it is not by too extreme a level and ancillary heat sinking methods will control any detrimental effects upon tissue.

It is useful to compare this device to other contemporary neural signal ASICs to determine its relative performance. The first such device is the formidable effort of Heer et al [9]. This device has dedicated amplifier circuitry beneath the electrode array with the electrodes AC coupled to the amplifier input. The input amplifier is of a fully differential folded cascode architecture (6 legs) and consumes an active area of 130 x 105 μm² and a projected passive area (calculated from capacitor values) of 4400 μm² (approx. 66 x 66 μm²). The device uses high value subthreshold MOS-R resistors to compensate for the low capacitors and provide a tuneable resistance between 800 GΩ and 800 TΩ for a 1 Hz to 1 kHz high pass filter cutoff point. The device dissipates 160 μW of power, has a gain of 20 dB, input referred noise of 5.9 μV rms, a CMRR of 70 dB and PSRR of 90 dB. This input stage also requires an additional passive low pass filter stage before multiplexing, which is lumped with the main amplifier consuming an additional 90 x 45 μm² to the interface area overhead. A novel stimulation ‘pixel’ was also included in this versatile device giving an overall front end area of approximately 250 x 250 μm².

In light of the high constraints of the front end presented in this chapter, the overall performance of the amplifier is good. Ignoring the area of the stimulus circuitry in the Heer device, this work presents almost a 7-fold decrease in the front end area consumption, this being mainly due to the removal of non essential passives. In terms of

power dissipation, this device consumes 6 times less power than Heers' front end device (the power dissipation of the MOSFET-C filter and buffer amplifier are not discussed), however the power consumption per active unit area is equivalent for both devices (247 mW/cm² this work in 100 x 100 μm² and 256 mW/cm² for Heer in 250 x 250 μm²). The devices offer similar CMRR but the area restrictions of this design are manifested in the PSRR. The Heer et al. device demonstrates a large 90 dB rejection of power supply noise due to the folded cascode architecture used that typically shows an inherent resilience power supply variations. The capacitive feedback presented in this work presents a lower 41 dB rejection of such influences.

The noise comparison was quite surprising as a rather small n-type input transistor was used in this work due to the poor KF constant of the AMS process and the area restrictions. Heer et al. use p-type input transistors but does not discuss their size or the KF constant for the XFAB process used. It is likely that the group faced similar problems to that faced in this work regarding allowable input transistor space resulting in a suboptimal sizing regime.

The second comparison is made with the Harrison and Charles devices [1], which consisted of two similar neural signal amplifiers, one operating at 4 μA and the other at 32 nA. The first device consumed an area of 0.16 mm² (~ 400 x 400 μm²) and the second 0.22 mm² (470 x 470 μm²) with over 67% of this area being consumed in passives. Both of these devices demonstrated a very large p-type (KF $=10^{-27}\left(F/m\right)^2 \cdot A^{2-AF}$) input transistor of 3200 μm² to reduce the effects of 1/f noise but still suffered heavily from thermal noise contributions. The 4 μA biased device delivered an excellent 2.2 μV rms noise floor between 0.5 Hz – 50 kHz, an 80 μW power dissipation and CMRR and PSRR greater than 80 dB. The 32 nA device demonstrated a 1.6 μV rms noise floor, 640 nA power consumption and similar PSRR and CMRR to the 4 μA device.

It is clear that this device is far superior in terms of low noise operation, however a 3-fold reduction in noise can be seen to cost double the supply current and almost 30 times the consumed silicon area (excluding the passives). The low power operation also comes at

an area price as discovered with the design of the work presented in this chapter. To effectively bias and balance the current mirrors in low power regimes requires increasingly long channel lengths that will quickly increase the consumed silicon area. Harrison's device also showed very good PSRR and CMRR (> 80 dB), the second of which is comparable to this work. The low PSRR of the presented design appears to be the main casualty of the reduced size minimal feedback design.

Another similar device is the high performance neural signal measurement device of Dabrowski, Grybos and Litke [10] of CERN. This device consists of an off-board neural measurement ASIC that is designed for high resolution capture of neuronal signals with high density MEAs. The device, being separate to the MEA substrate has much lower constraints in terms of power and area, however as discussed in chapter 3 this is at the cost of electrode track routing and the introduction of parasitics.

Due to the large available area away from the culture, this device uses massive 3000 μm² p-type input transistors and consumes 750 μW per input device. This and careful design reduces the noise to 1.22 μVrms for the process used. The device allows control of filter cut-off circuitry and gain. Each input device consumes 0.35 mm² (3500 x 100 μm²), CMRR and PSRR are not discussed. The amplifier presented in this chapter only displays a 4 times increase in noise for a 90 times decrease in size when compared to the Dabrowski et al. amplifier, however this may be critical in some neural signal observations where poor seals are expected or direct field potentials are to be measured. The increased functionality of this device such as amplification and bandwidth control may also be necessary in some applications; however these functions may also be implemented the presented design with the resulting increase in interconnection complexity and possibly area consumption.

A final comparison may be made with the Eversmann et al. device [11]. This device provides an un-equalled electrode density of 16,384 electrodes within a 1 mm² area, with each neural imaging 'pixel' occupying a sub cellular sized 7.8 μm x 7.8 μm area. To achieve this, the device has a single transistor beneath each electrode forming a 'buffer'

between the electrode and dedicated amplifier units placed approximately 1mm away. This high density design suffers heavily from matching effects of the small uncompensated input transistors and is more susceptible to noise with the signal being in the current mode. Very little information is given in this publication regarding the exact bias current used for the input transistors, however in an unpublished correspondence with Thewes, one of the researchers on this project, each of the sensing transistors had to be biased in the saturation mode to ensure that the measurement circuit could operate at a suitable speed. This caused significant heat dissipation requiring heat-sinking and active cooling to prevent damage to the neural cultures. The noise contribution of the sensing transistors are also not numerically defined, however noise is discussed in terms of optimisation and may be visually inspected from the presented data as being approximately 10 $\mu V_{pk\text{-}pk}$. This is very low considering the size of the input transistor and the switched connection methods used. The device provides a 2 kHz sampling rate per channel with a total data output of 32 MHz. Direct comparison is not possible with this device due to the lack of shared device operational information. This device can be seen as the extreme end of high density signal transduction, whereby the front end amplifier is split into two separate sub units that are spatially distributed on chip to increase the density of active sites. This will inevitably lead to sub optimal noise characteristics and added system complexity, but for such high resolution this may be an acceptable compromise.

The design of neural ASICs is quickly becoming a very large area of funding and research and there are many concurrent areas of emerging research from many institutions. The design presented here, although a prototypical exercise in density enhancement and device minimisation presents a favourable comparison with some of the leading research groups in terms of active electrode characterisation and design.
The method presented that uses the interface capacitance of the electrode as an effective low frequency continuous time filter element demonstrates a suitable solution to the area issues facing the fully integrated active electrode circuit.

This comparison will however only be certain once the device has been fabricated and fully tested on a neurological test bench for the qualities indicated by the simulation. The confidence of accurate device prediction from the simulation process would indicate that the device will perform closely to the way the simulations specify; however it is understood that it may take several fabrication iterations to get the most out of the physical realisation.

8.8 Summary

The design presented in chapter 8 was developed into a fully integrated circuit to symbiotically use the interface capacitance of the electrode as part of a transient charge measurement circuit for neural signal measurement. The design considerations for a compact 60 x 60 μm² (approx.) device using this principle were developed into a physical transistor amplifier block with supporting circuitry for fabrication as part of a high density active electrode array. The device uses the top metallization layer for electrode deposition to allow direct high conductance contact between the electrode and the amplifier input. The design demonstrates a gain of 62 dB, a noise floor of 4.509 μVrms within the passband range and filter passband between 100 Hz to 10 kHz.

8.9 References

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Chapter 9

Front End Development for System on Chip (SoC)

This chapter develops the front end integrated design for complete System on Chip architecture. Array arrangement and the interconnection challenges discussed in section 3.3 are considered and an analogue multiplexing solution is presented. The design description is discussed towards its final state for a prototypical 256 pixel array. The chapter concludes with the further work necessary to complete the ASIC for tape out and fabrication. The functional structure of the chip design is presented in figure 9.1 below. The design and layout of the main functional blocks are described throughout this chapter.

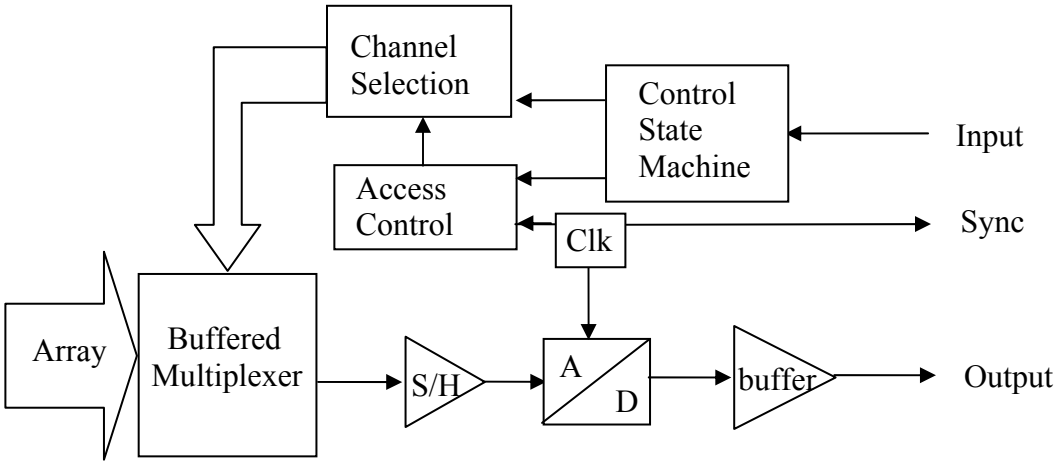

Figure 9.1

Chip functional structure

9.1 Amplifier Channel Handling

By multiplexing each of the recording channels to a single output the device connection overhead may be reduced to that of a single output. By this method, neural signal recording channels can be sampled in an ad-hoc manner dictated by the spatial interest of the researcher. Each channel is hardwired to a unique digital address and may be accessed by applying that address to the multiplexer circuit address bus.

9.1.1 Verifying the Track Parasitic Capacitance

The amplification of the neural signal will raise the signal above the resistive noise and capacitive losses of the tracks. It is important to verify this as part of the design process to ensure that the micrometer scale signal paths do not present unforeseen problems based upon this assumption.

The track sizing and interconnection length is dependent upon the number of array elements and the topological issues discussed in chapter 3, section 3.3. For a square arrangement 256 electrode array, this presents a maximum track length of 15 x 100 μm = 1.5 mm and following the 100 μm inter-electrode spacing scheme, a 40 μm available routing area between devices.

Considering the implementation of this in a single metal layer this may be achieved easily with a 1μm track thickness and 1μm spacing. For a 150 mΩ/□ Metal 1 layer, this will present a maximum track resistance of 225 Ω for the amplifier that is furthest away from the buffer / multiplexer and several Ω for the closest amplifiers. In terms of noise this will present a $\sqrt{4kTRB}$ presence from DC to 10 kHz, unless an additional high pass filter stage is introduced. This is calculated at 0.2 μVrms and is well below the neural signals that are now amplified to mV.

Secondly, capacitive parasitics may be estimated. This was achieved by using the estimation techniques of Sakurai and Tamaru [1] for VLSI on chip routing capacitance. This technique estimates the capacitance for side by side tracks and track to ground cases for SiO_2 encased tracks. Numerical accuracy is determined in terms of S, H, W and T ratios as shown in figure 9.2 below. The effects of additional metal layer tracks may be assumed negligible as long as they do not run parallel to the signal tracks.

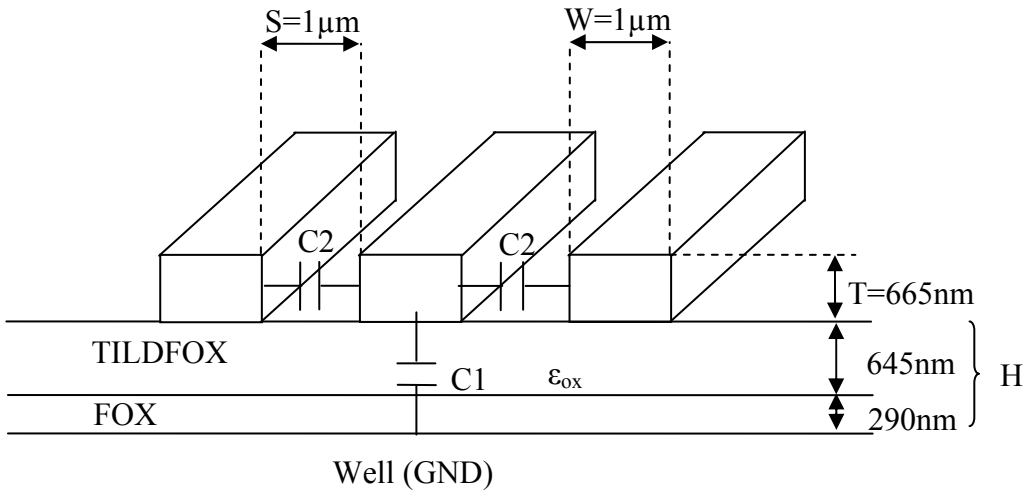

Figure 9.2

VLSI signal routing capacitance parameters for AMS 0.35µm process

For a 1µm thick Metal 1 track for the AMS 0.35 µm process, T is equal to 0.665 µm, H is approximately equal to 1 µm and S will also be 1 µm. This determines that the calculations will be accurate to within 2.3 % of a numerically solved finite element solution.

The capacitance is calculated per track in terms of C3 = (C1 + 2C2) for symmetrically placed layouts:

$$C3 = \varepsilon_{ox}\left(\begin{array}{l} 1.15\left(\frac{W}{H}\right)+2.8\left(\frac{T}{H}\right)^{0.222} \\ +2\left[0.03\left(\frac{W}{H}\right)+0.83\left(\frac{T}{H}\right)-0.07\left(\frac{T}{H}\right)^{0.222}\right]\cdot\left(\frac{S}{H}\right)^{-1.34} \end{array}\right) \qquad 9.1$$

From these simple but accurate empirical calculations the capacitance experienced by the tracks ranges from 25 fF to much less than 1fF. The cross talk effect of this will be negligible upon the signal and the RC time constant of the track loss is well above the signal frequency. The greatest effect will occur due to a small percentage increase in the effective load capacitance experienced by the slewing amplifier, e.g. for a 200 fF load this will increase by approximately 10 % in the worst case.

9.1.2 The Multiplexer Circuit

The multiplexing circuit must be designed and characterised before the buffer circuit as its electrical properties will influence the load experienced by the buffer circuit. If the current of the buffer does not clear the total slew rate signal errors will result as the signal struggles to slew the ADC input.

Analogue multiplexers are formed using transistors as resistive switches. As a result they are presented with a 'on resistance' proportional to the drain-source resistance of the amplifier and additional parasitic capacitances associated with the charging and discharging of the semiconductor inversion region during switching. The gate capacitance is also responsible for charge injection noise due to this phenomenon. The gate must be wide to lower resistance and small to minimise capacitance. Because of this, one is faced with the trade off between operating speed and operating resistance.

One is also faced with the operating characteristics of the transistor in the 'on' state. The transconductance of the transistor is dependent upon the drain to source voltage V_{ds} from basic transistor theory, causing the on resistance to vary with the change in the applied signal. This may be overcome to some extent by employing complementary type

transistors. By matching these devices in terms of transconductance the on resistance may be somewhat stabilised and charge injection noise much reduced.

The multiplexing circuit therefore consisted of matched complimentary pairs with attached inverter as shown in figure 9.3.

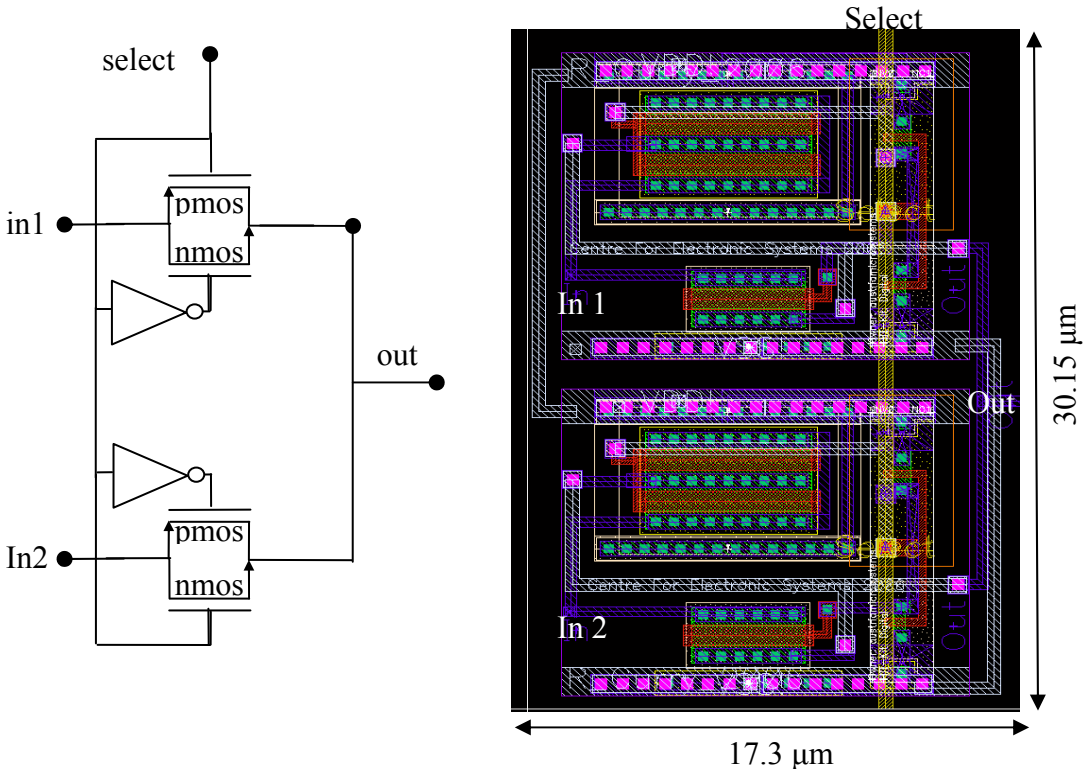

Figure 9.3

Schematic and layout of multiplexer circuit

Sizing was chosen by the ratio of the AMS process tarnsconductances K'_p and K'_n according to:

$$\frac{W_n}{L_n} K'_n = \frac{W_p}{L_p} K'_p \qquad 9.2$$

Where W_n and L_p are 5 µm and 1 µm respectively, with $K'_n/K'_p = 2.931$; giving W_p = 14.7 µm and Lp = 1 µm. Each Multiplexer stage added a load resistance of approximately 500 Ω and 25 fF capacitance.

9.1.3 Pre-Multiplexer Buffer

It was determined in the previous section that the low power operation of the input amplifiers would not be sufficient to slew the resistive load of the multiplexer circuit at high frequencies. For an example 256 active electrode array with each channel sampled by 10 kHz the required settling time at the ADC is less than 200 ns per device. For this reason each channel is presented with a dedicated high speed buffer circuit that precedes the first stage of the multiplexer. In comparison to the input amplifier this circuit has much less constrained design criteria; area, power consumption and input referred noise may be quite liberal, however current slewing must be sufficient to supply the input of the ADC with an accurate signal potential and without additional signal offsets.

The buffer was designed with the slew rate as its main concern. The required output current I_O for a given slew rate is calculated by:

$$SR = 10\left(\frac{V_{dd} - V_{ss}}{2T_s}\right) = \frac{I_O}{C_L} \qquad 9.3$$

Where V_{ss} and V_{dd} are the amplifier supply rails (1.65 V and -1.65 V) and T_s is the switching time for the ADC samples. For 256 channels at 10 kHz this is a slew rate of 42.3 V/µs. With a load capacitance C_L of 0.8 pF ($\approx C_{Track} + 8xC_{mux} + C_L$) the required current is above 42 µA; over 20 times higher than available from the input amplifier.

A buffer amplifier design presented here is a differential voltage follower circuit. The device was designed for output current above 90 µA, a bandwidth of above 10 MHz to

ensure a good settling response at 2.56 MHz and an open loop gain above 60 dB to ensure the effects of finite gain errors are minimal. The effect of gain error is presented for interest in equation 9.4.

$$gain\_error = 1 - \left(\frac{A_{OL}}{1 + A_{OL}} \right) = 1 - \left(\frac{1000}{1 + 1000} \right) = 0.1\% \qquad 9.4$$

Mathcad was used as a starting point for all circuit hand calculations presented in this thesis due to its blackboard style calculation interface. The buffer was designed to operate using the input amplifier bias circuit for component device simplicity.

The final buffer amplifier circuit is shown schematically in figure 9.4. Transistor and passive sizes are given in Table 9.1. The buffer performance characteristics are presented in table 9.2.

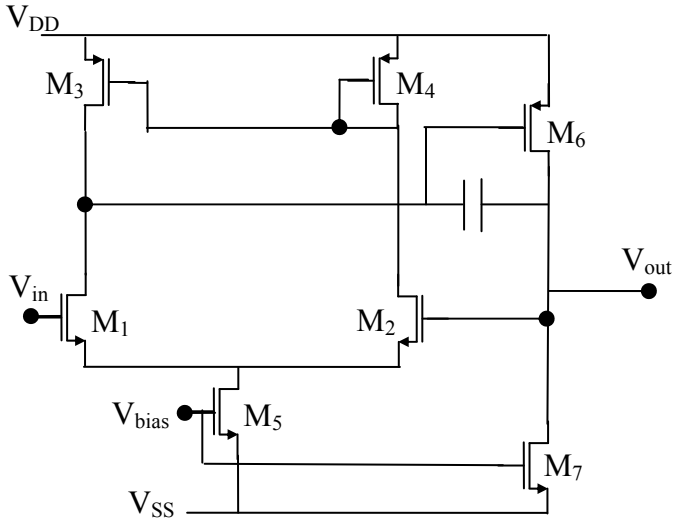

Figure 9.4
Buffer amplifier schematic

Device	W/L (μm)
M1,M2	7.5/1
M3,M4	20/1
M5	10/1
M6	234.9/1
M7	47/1
C_c	6 x 26.6 fF 6x (5 x 5.75 μm²)

Table 9.1

Buffer amplifier transistor sizes

Variable	Value
DC Gain (open-loop)	78 dB
Finite Gain Error	< 0.1 %
Power Dissipation	425.7 μW
3dB point (closed loop)	50 MHz
Output Current	109 μA
Headroom	± 0.7 mV
Noise (DC-10MHz)	48 μV_{rms}
PSRR	> 70 dB
CMRR	> 70 dB

Table 9.2

Summary of buffer circuit performance

The buffer layout was developed to provide a thin 25 μm x 128 μm area to reduce the path spreading of the input amplifier output channels on chip and also to reduce the overall width of the parallel buffer block. Even in light of this the buffer block will consume a formidable chip width. With 256 channels and 25 μm width for each buffer,

this fans out the active chip width to 6.14 mm. For this reason the buffers may need to be staggered depending upon the budget of available microchip area.

The layout of the buffer is presented in figure 9.5.

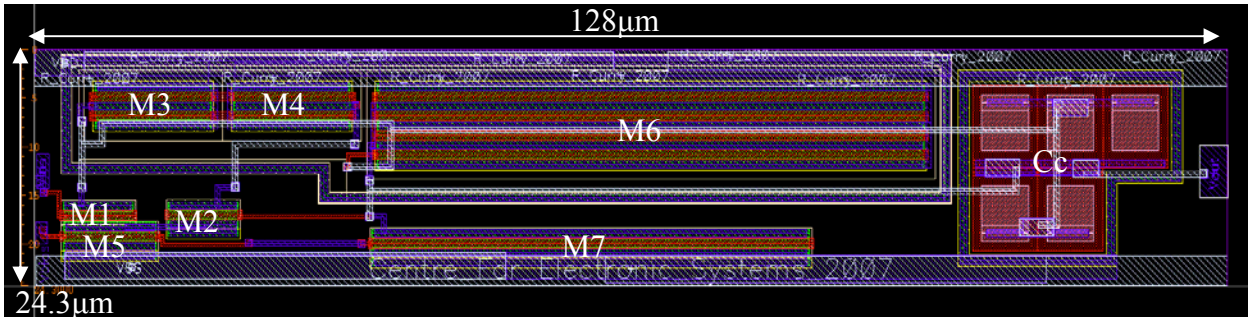

Figure 9.5

Layout of buffer circuit

9.2 Front End Layout Assembly

Each of the front end blocks were assembled into a prototype 256 element array including bias circuitry, input amplifiers, buffer circuitry and multiplexing circuitry to form a demonstration device for fabrication and analysis. The front end topology was carefully designed to make the most of the limited silicon area. This arrangement is illustrated in figure 9.6.

To conserve area, bias circuits were shared between input amplifier rows and buffer amplifier columns.

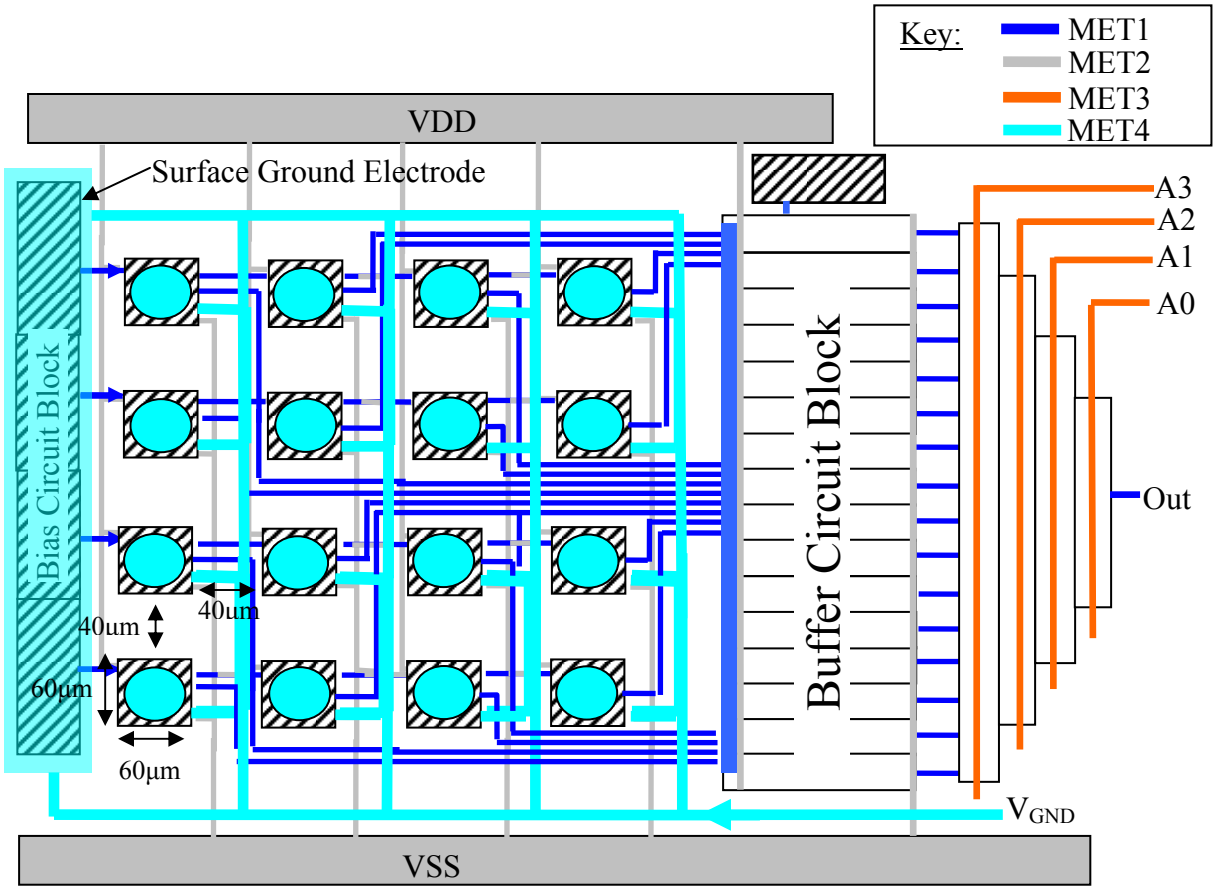

Figure 9.6

Diagram of active electrode connectivity.

The buffer amplifiers used a column sharing of bias circuitry. As the bias circuits are not required to slew current to the dependent devices, merely keep constant voltage this was seen as a sensible solution to the general lack of appropriate space for one to one connectivity. VDD and VSS are presented to the devices on an alternative column scheme using Metal 2 and the ground electrode connection (discussed further in section 9.3) is provided by a thick Metal 4 that forms a grid around the exposed Metal 4 electrodes.

A 256 active electrode prototype front end implementation is shown in a large foldout page in Appendix E. A smaller 16 active electrode array is shown in figure 9.7 (and again as a foldout in Appendix E) to show the layout arrangement of the composite blocks in a front end design test structure.

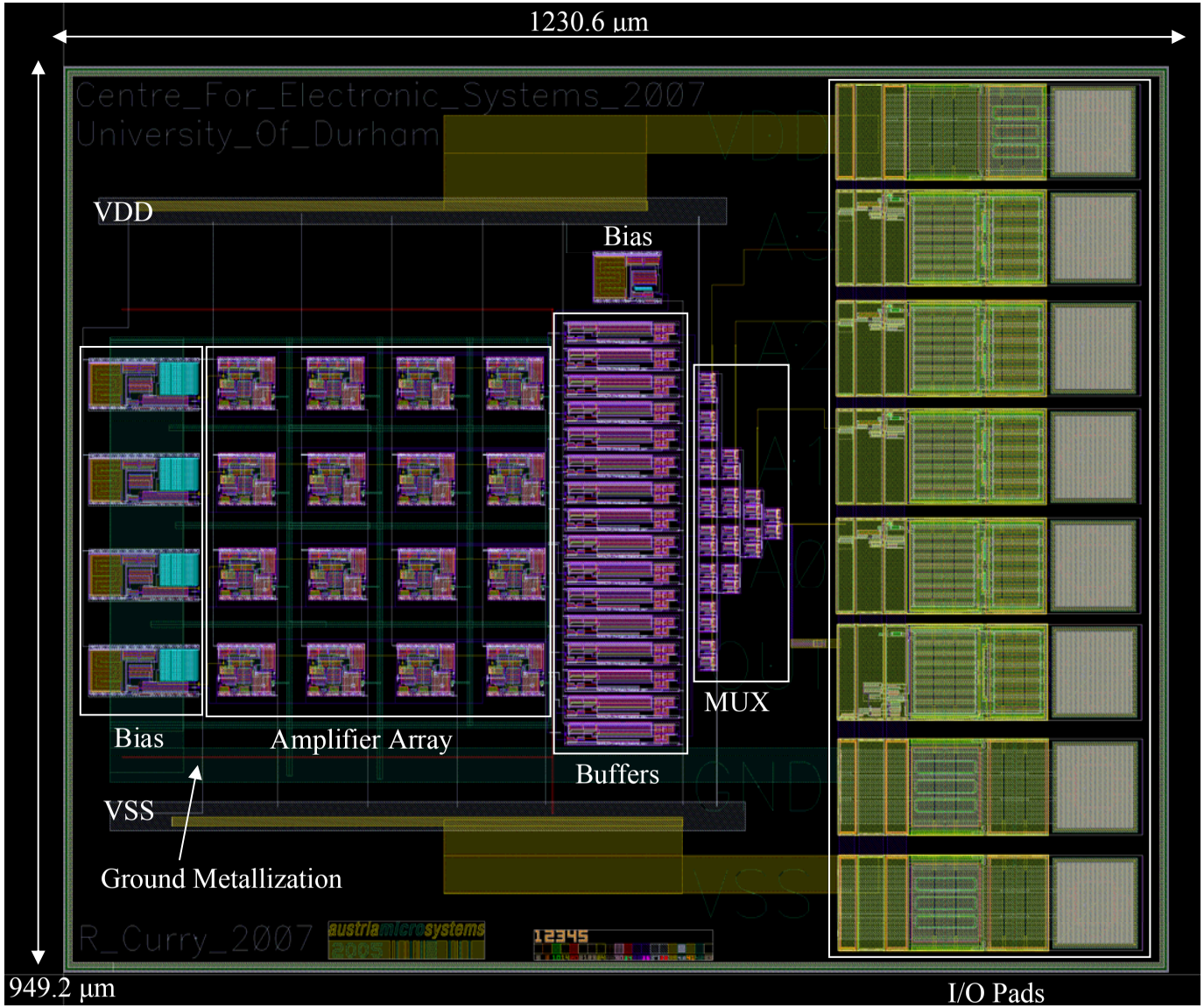

Figure 9.7
An example layout for a 16 active electrode array

9.3 Forming the Ground Electrode Network

The ground electrode and its connections are very important to the overall operation of the device. Each input amplifier circuit must be provided with a low resistance path to the ground electrode in order for the circuit to operate as a high pass filter and maintain its common mode bias from the 0 V ground of the power supply and its reference to the electrolyte. The interface ground is provided by a large 1 mm x 0.1 mm Metal 4 stripe positioned above the electrodes at the front of the chip. The ground electrode will be fabricated by the same process as the recording electrodes using post process etching and Au deposition. The arrangement can be viewed in figures 9.5 and 9.6 for a 16 array element example.

Many different configurations are possible as the top metal will only be used within the array for electrode formation. To ensure that the capacitance per unit area and surface resistivity of the measurement electrodes in the array are close to the values as measured in chapter 7, Ag/AgCl should be deposited onto the reference electrode surface. This may be performed by evaporating or plating a layer of Ag onto the surface of the reference electrode as part of post processing and electroplating the Cl layer onto the Ag within HCl solution.

9.4 A 256 Electrode Test Structure

A 256 electrode test structure was developed that incorporated each of the presented design blocks. The design was assembled with the Cadence Virtuoso package with program assisted routing. The active electrode devices are interspaced by 100 μm and consume a total area of 1.6 x 1.6 mm², the total silicon area required to realise the design is 3.0 x 3.760 mm². The test structure, along with the 16 element array will allow the operation of the amplifier circuitry to be analysed on a laboratory testbench to determine whether further analogue design iterations are necessary before other integrated circuit elements are added. The test procedure will involve direct electrical signal stimulus

through the input electrodes to be measured at the output pads before further testing may be performed in physiological saline. The latter test stage will require additional chip passivation, Au electrode deposition and device packaging before verification analysis can be performed. This will be performed using standard IC packaging techniques for electronic analysis within the laboratory before physiological environment tests may be performed.

The development of the IC was taken as far as the Design Rules / Parasitic Extraction procedure for each of the composite blocks. The software provides confidence that the device will operate as simulated, however further modifications may be necessary if the device does not perform as expected. Discussions with the foundry would be beneficial to discuss the non standard features of the device such as the decision to use the oversized top metal as the base of a working electrode.

9.5. Further Work

It was not possible to develop the presented system in its entirety during the time available, as a result there still remains several aspects of the design that require further effort to complete the high density versatile active MEA. These areas are covered briefly in the following subsections and include signal digitisation, array access control and conceptual packaging schemes.

9.5.1 Analogue to Digital Conversion

Further signal processing may be performed on chip to reduce the need for external resources in conditioning the recorded signal for analysis. In order to maximise the spatiotemporal versatility of the device, discrete channel sampling and digital manipulation of the data is preferable, especially considering the ability of modern

personal computers. Before a computer can process the sampled neural data it must be converted from the amplified time based voltage into a time referenced digital signal. This may be achieved by intermediate components or implemented directly on chip for little extra manufacturing cost. The second option is more favourable as it reduces the overall number of required components and removes the lossy analogue signal transmission mechanism at the source, replacing it with more robust switched digital communication.

For this reason an on board ADC is suggested as part of the final device design. There are many ADC architectures to choose from in design, each with its own advantages to given design specifications such as digitising resolution, sampling speed, allowable area and power consumption that must be enumerated before a method is selected.

For an excellent introductory review of the comparative tradeoffs between ADC architectures one is referred to the texts [2, 3].

The prototype circuit contains 256 active electrodes and thus 256 channels, denoted n_c to be sampled. Each channel has a 5 kHz maximum bandwidth. This was chosen to provide an additional 2 kHz headroom to the maximum spectral frequency for the Helisoma B19 neuron as determined in chapter 5. To ensure that all frequencies in the extracellular neural signal spectrum are preserved, the minimum sampling frequency f_s, as defined by Nyquist is 2x the maximum spectral frequency. The ADC would have to sample each of the channels at this frequency and would therefore require a minimum sampling frequency of:

$$F_{sampling} = n_c \times f_s = 256 \times 10kHz = 2.56MHz \qquad 9.5$$

This sampling rate is towards the higher end of ADC speeds, requiring flash and algorithmic architectures such as the pipeline ADC. The multiplexed nature of the sampled signals a Sigma-Delta ADC type would not be satisfactory due to oversampling and latency issues with the constantly switching input.

The second consideration that must be made regarding the ADC is the resolution. The trade-off between sampling speed, accuracy and consumed area is much less critical for modern ADC architectures than it was in previous years. Resolution is typically proportional to the area consumed by the device, mainly due to the number of physically large, high precision comparators within the circuit. The number of these comparator circuits is also proportional to power consumption; for example a 10 bit flash ADC requires 2^{10} comparators. In this situation, algorithmic ADCs are more amenable as they require N x 2^n comparator circuits for a N stage n bit resolution device. A 10 bit, 1.5 bit per stage pipeline ADC is ideal for low area, low power design within the 2-20 Ms/s range of operation due to its relaxed precision 20 comparator architecture. The majority of power in these devices is consumed by the N-1 amplifiers required to multiply the pipelined signal during the conversion. The 1.5 bit pipeline, originally developed at Berkeley by Gray et al. is now commonly used in many medium to fast, 10 – 16 bit resolution applications and several designs have been published with relatively low area consumption and power dissipation that is more suited than others to this particular application.

The suitability of the 1.5 bit / stage pipeline ADC for the SoC design encouraged the development of a custom ADC device for this design. Unfortunately, the overall complexity and time required to realise such a device from scratch in silicon was beyond the constraints of this work and the device was reluctantly abandoned.

The AMS fabrication foundry offer (at additional cost) a 10 bit, 20 Ms/s Pipeline ADC cell that may be incorporated into the integrated circuit on request. Once the amplification and channel selection circuitry has been verified this may be a simple solution to integrate on-chip digitization into the design. The device consumes 200 mW of power and covers an area of 2.1897 x 0.7174 mm². The input capacitance is 1 pF which is just within the slew rate range of the signal buffer amplifiers for a 2.56 Ms/s sampling rate.

The power dissipation of the ADC is not ideal. 200 mW within the specified chip area constitutes 12.7 W/cm² which is 160 times greater than the 80 mW / cm² specified by Seese et al. for cellular necrosis. Within the given area consumed by this ADC, a total power consumption of less than 1.2 mW would be required which may be impossible for such a high performance device. Pipeline designs have been published that consume as little as 36 mW [4] using novel amplifier schemes, hence the motivation to produce a full custom design for this device. Ultimately parallel low speed architectures may be considered at the expense of consumed area and more complex channel control schemes, or lower resolution conversion.

Although the ADC portion of the IC will not be placed directly in contact with the measured neurons, this high power consumption still presents a problem in terms of additional conducted heat through the substrate. This strongly suggests that a heat sink must be considered as part of the final device packaging to reduce this problem to within tolerable levels.

9.5.2 Programmable Array Access Scheme

A simple method was developed to allow the user to control the sampling rate and order of channel selection in the fully integrated device. The method allows the device to run in two modes of operation. The first mode is a default state whereby the multiplexer address lines are selected in numerical order by a counting circuit connected directly to the multiplexer select lines. In this mode the counter will count from 0 - 256 and sequentially access the array at 2.56 MHz, sampling each amplifier at the 10 kHz sampling rate.

The second mode is a user addressable scheme that may be useful for larger arrays of electrodes above the optimal sampling range of the ADC. For example, an array may be produced with the option of sampling each amplifier at a sub-optimal sample rate, sampling a user defined set of electrodes at the full sample rate or a mixture of both. This

method may be performed by strobing the address lines of the device with real time commands from an external computer interface. To reduce the input path overhead a state machine controlled serial input scheme will be necessary with synchronised input shift registers. The clock speed of this circuitry will be required to operate at M times the ADC sampling rate to ensure that each bit of the programmed address is loaded into the registers (and the array element is accessed) before the ADC samples the channel. This is illustrated in figure 9.8 for an 8 bit (256 element) array.

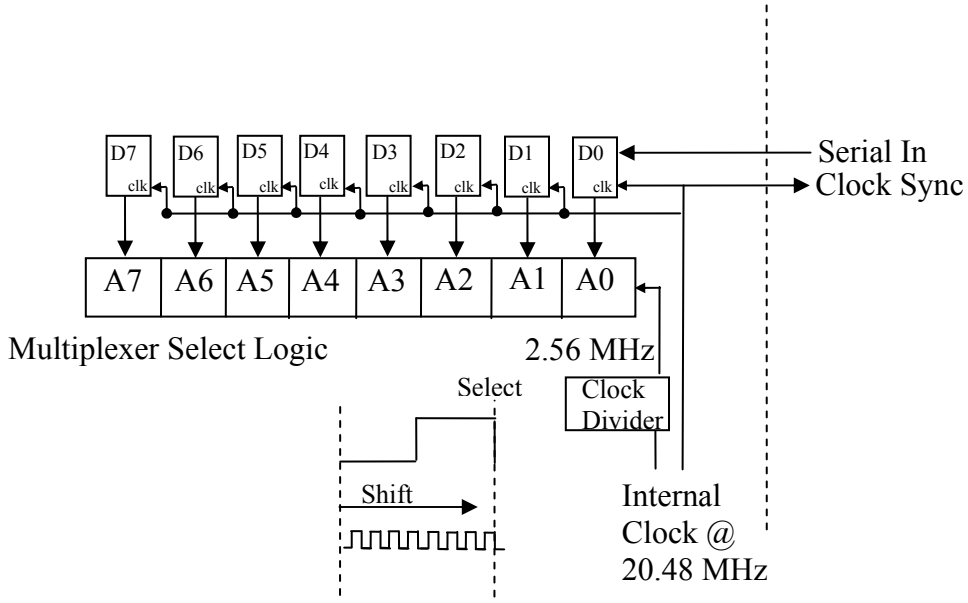

Figure 9.8

Simple schematic and timing diagram for externally controlled array access

A less timing dependent scheme is to incorporate user defined pre-programmable array by loading a predefined address list into internal SRAM block. By setting a minimum sample rate of 2 kHz a 5 kB memory block would be required to provide a looped lookup table for all possible multiplexer addresses that may be sampled by a 2.56 Ms/s back end for up to 65, 536 electrodes. This proposed scheme is shown in figure 9.1 and 9.9.

Once the signal has been digitized there are also many digital processing steps that may be performed upon the sampled signal in hardware before the signal is sent off chip. The

reduction of the many channels of analogue signal information into compact digital bytes also enables the future option of wireless signal transmission and device control, thus making the device even less obtrusive in both *in vitro* and *in vivo* use.

9.5.3 Chip Floorplan

The overall chip floorplan will take the form presented in figure 9.9 below. It is desirable in this chip design to create larger than average V_{dd}, V_{ss} and Ground supply lines due to the problems associated with high resistance ground 'bounce' and supply 'droop'. This phenomenon occurs as the result of the high resistance supply paths that may be up to several kΩ, resulting in an ohmic potential drop as the power current is supplied resulting in a sharp transient decay in the supply (visualised as a supply bounce on the oscilloscope). Typically such problems may be resolved by the use of large decoupling capacitors placed between the V_{ss} and V_{dd} of each effected circuit to keep the supply at V_{dd} and supply transient charge when required. In the case of the presented amplifier circuitry this is non ideal as we wish to keep the consumed area per device as low as possible. The main device supply rails are therefore to be oversized to over 50μm minimum thickness and several 100 μm at their largest to ensure a minimal supply resistance through the circuitry. This will ensure a supply resistance of several ohms over a 3mm chip length as opposed to over 1 kΩ if a 0.5μm track width were employed. The resistive losses are dominated by the shorter top-to-bottom supply tracks sized at 2 μm width, causing a total path resistance of approximately 140 Ω for the longest path. This will constitute a V_{dd} supply voltage droop of:

$$V_{DD}(device) = V_{DD} - (I_{device} \cdot R_{track}) = 1.65V - 6\mu A \cdot 140\Omega = 1.649V \qquad 9.6$$

This value must be observed with caution for large array topologies, especially for larger current consuming devices such as the buffer amplifiers, whereby a 2 kΩ supply track resistance will lower the supply by 5 % per rail.

The analogue front end, consisting of input amplifiers, buffers and multiplexing circuitry are physically separated from the digital back end to reduce clock feed through effects and switching noise. The ADC which is essentially a hybrid of both domains will ideally be positioned between the two.

The effects of power dissipation from the various circuit components will present a large problem to the circuit during electrophysiological measurements. The circuit has been structured in an attempt to minimise the local effects of dissipative heating, with the separation of the input amplifiers from the buffer circuitry and the positioning of the ADC towards the back end of the chip.

The combined system on chip, complete with ADC, serial input device selection and communication synchronisation will require no more than seven bonding pins. Three of these pins will be attributed to V_{dd}, V_{ss} and G_{nd}. Of the remaining four, two will form the input data loading and state control, and the final pin will supply the multiplexed digital output data from the device.

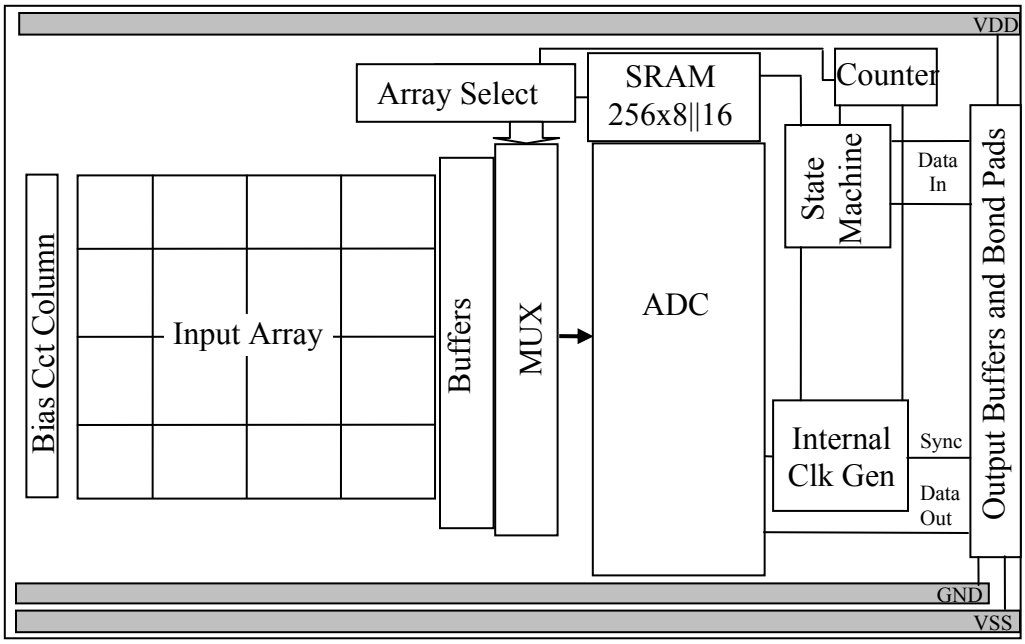

Figure 9.9

Envisaged floorplan of fully integrated active MEA soc with minimal input/output connections

9.5.4 Packaging

The ASIC design presents the possibility of an unobtrusive neural signal monitoring device that may be applied to many different applications. The final system will allow all channels to be monitored by a single digital output pin. Similarly, the system control will require a maximum of two pins, giving the MEA system a data capture versatility and control that is not possible with the passive array methods. As the electrode array is not constrained by the discrete channel interconnections of passive MEA a whole new area of possibilities for both *in vitro* and *in vivo* neural network investigation.

The selected application will become dependent upon the packaging method used for the device. For in vitro, the culture dish method will typically be reproduced, with a reduced wiring overhead and higher density features; whereas for *in vivo*, a series of application

specific packages will need to be developed. Two simple conceptual packaged devices are discussed generally in this section for further work. It is hoped that the device, or similarly developed future devices may find use in the *in vitro* and *in vivo* experimental domains for high density signal capture.

The method of packaging is perhaps one of the most important considerations for the design. The bare post fabrication device will find the biological environment aggressively corrosive and will require further processing steps to ensure that it operatively stable for its intended use. The exposed top metal electrodes and bondpads, formed from aluminium, will oxidise and allow the saline to attack the internal interconnection pathways within the chip. As these interconnections are functional voltage carriers, their electrical potential may even speed up the corrosion process when presented with an electrolytic breach.

Furthermore, the overall effect of the packaged system upon the biological matter must be carefully considered. Upon corrosion the surface will form salts within the saline and poison the biological system. Essentially, the packaging material must be as inert as possible. If the device is to be used *in vivo* toxicity may become more apparent in chronic use, the materials must also be non inflammatory and nonallergenic and possible non carcinogenic in longer term studies.

In general, the integrated circuit solution is beneficial to the *in vivo* and *in vitro* neural signal measurement domain. Integration reduces the need for analogue signal carrying wires to a minimal digital situation. For the *in vivo* study of living organisms this reduces the dependency upon mechanical wiring failure or wiring insulation failure. Additionally, over the last 20 years there has been much research into the uses of semiconductor packaging for biological sensors for mechanical and electrical observation. Materials such as Silicon Nitride (Si_3N_4), anodically bonded Pyrex, SU8 and other various encapsulation polymers have been demonstrated to not only present negligible water absorption and permeation but also excellent substrate adhesion, allowing chronic device use without temperature and stress related fracturing.

Si_2N_4 coating of up to 1μm thickness has been shown to provide adequate protection of the silicon in biological environments and is often used in fabrication for the final passivation layer. The chip should be impervious to physiological corrosion once the final post process Au deposition and etching is performed. This is illustrated in figure 9.10 below. A Titanium seed layer will be necessary preceding the Au deposition to ensure that the deposited gold forms a good bond with the Si_3N_4 side walls. The bond pads, once connected to the final packaging will require polymeric encapsulation to prevent the system from shorting within the physiological saline during biological testing.

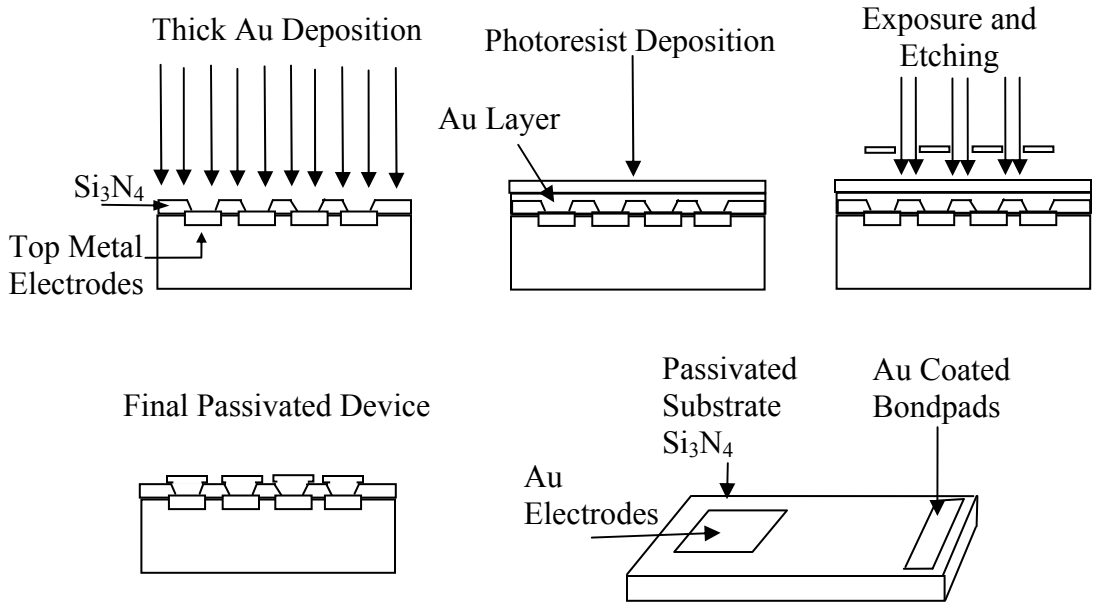

Figure 9.10

Illustration of final Au deposition process for passivation

Two prototype packaging schemes are considered for the final deployment of the device. The first is for the *in vitro* MEA style measurement. The substrate will be formed by dual inline carriage style package (DIP) with the chip. The chip will be physically very small (no more than 3-4 mm in length and 3 mm and may be bonded into a die cavity of up to 1cm² for handling purposes, usually performed by the fabrication house. The die cavity may then be glued into the DIP with further wire-bonding providing the connections to

the package pins. The package must then be hermetically sealed around the bond wires and pads while leaving the active area of the chip exposed. This may be performed with a biologically compatible epoxy resin compound. A bottomless plastic or glass culture dish may be glued to the substrate, protecting the electrodes and forming a sealed culture area before the package is flooded with the protective epoxy. This process is illustrated in figure 9.11. Larger arrays may be formed with multiple devices bonded to the die cavity.

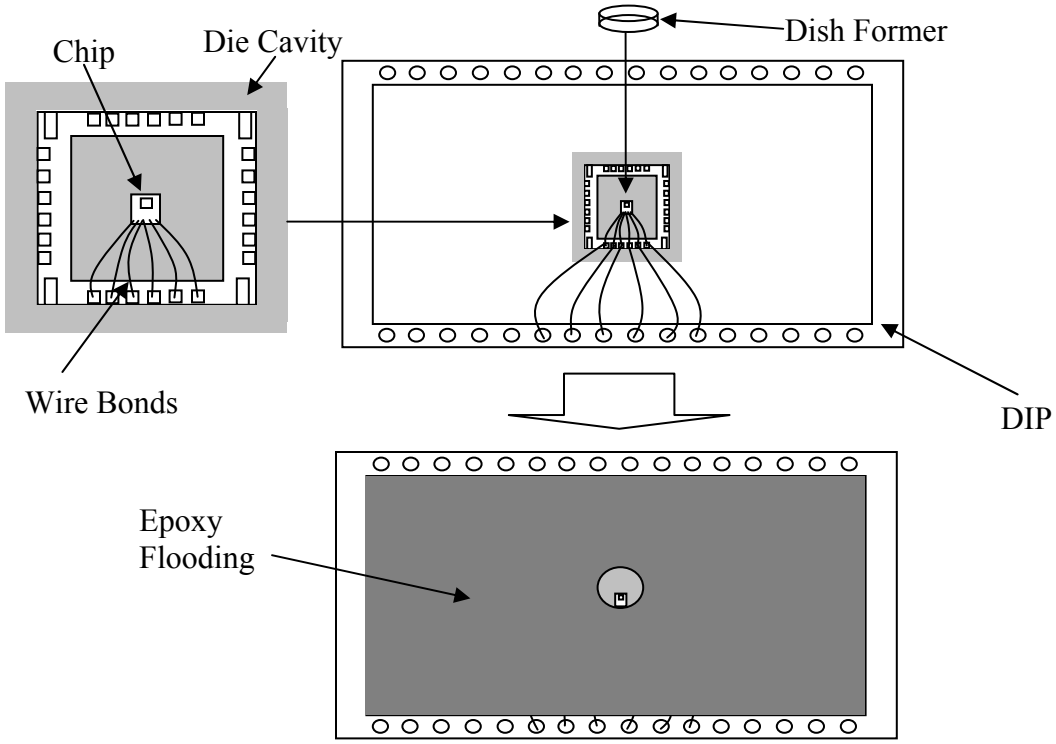

Figure 9.11
Prospective MEA style DIP packaging scheme

For *in vivo* applications, much more thought must be invested in the packaging scheme, which itself will also be dependent upon the application it is driven towards. For CNS intracranial signal measurement intrafascicular spiked electrodes are often used, and cuff electrodes are generally utilised for PNS axon monitoring applications. Due to the small form factor and high density signal capture of the presented device it is not unreasonable

to assume that it may be used as part of these structures. A fully passivated device, forgoing the die cavity may be bonded to an intrafascicular shank for localised spatiotemporal monitoring of grey matter. Such a device, if attached to a heat conducting shank may also present less of a heat dissipation issue than otherwise. The speculative form of such a device is shown in figure 9.12 below. Additionally, much thinner form factors may be possible by spreading the active electrode recording sites and processing circuitry longitudally down the silicon for much narrower arrays. Wiring may also be reduced by use of local batteries for power.

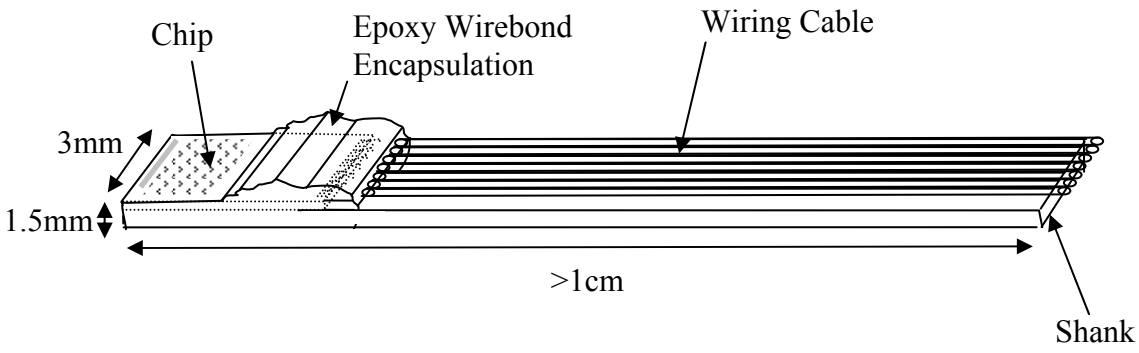

Figure 9.12
Use of the device as a hypothetical shank header

9.5.5 The Effects of Power Dissipation

In chapter 8 the need for stringent power dissipation control was noted based upon the published observation that chronic *in vivo* heating above 80 mW/cm² may cause cellular necrosis. Clearly, it is very difficult for the presented high density system and others like it to perform adequately within these design specifications. The power consumed by amplifier circuitry is inversely proportional to the input referred noise and ultimately the

required on chip area for adequate functionality. Low power operation below this level also presents signal slew rate issues for optimally sampled high density arrays. Higher current slewing support circuitry must also be incorporated into the design to boost the signal before channel selection and sampling. The buffer circuitry may be placed away from the input amplifiers and the physiological area of interest; however it will still heat the substrate and system accordingly. At the back end of the device the majority of the power dissipation will result from the analogue circuit components such as the precision amplifiers within the ADC circuitry. The presence of the ADC close to the multiplexing stage ensures minimal signal drop and noise contamination, however its power consumption may very well eclipse that presented by all of the other on chip components combined.

The overall power consumption for the 256 active electrode prototype device presented in this thesis is summarised per unit area for each of the major analogue blocks in figure 9.13. The power consumption of the AMS ADC is also included for comparison.

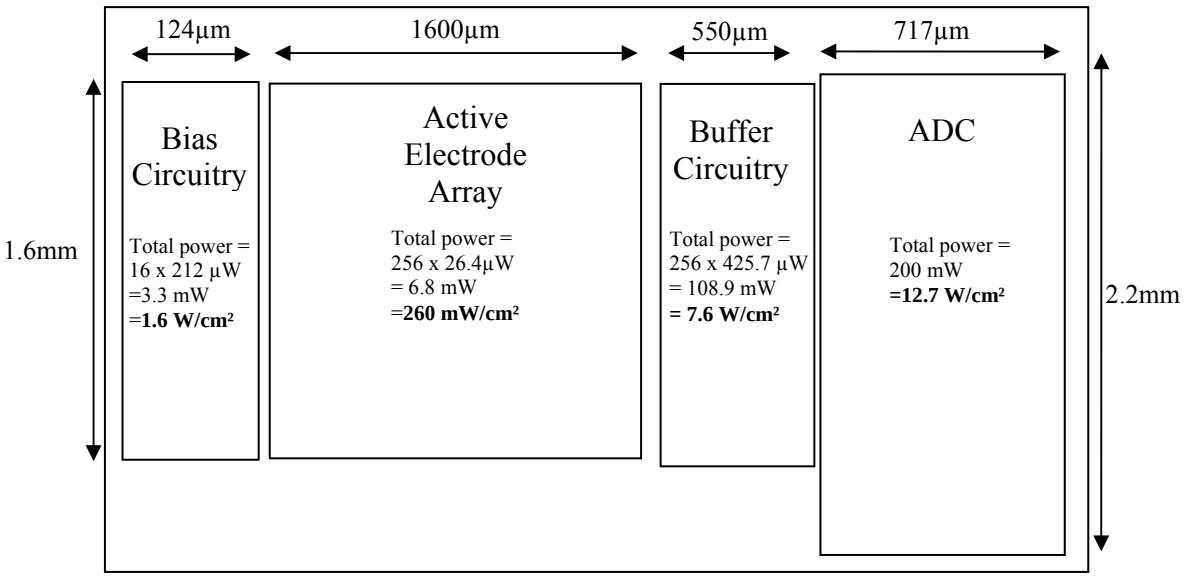

Figure 9.13

Power consumption of the composite functional analogue blocks

On analysis it seems that such a device may be intrinsically unsuitable for direct cell contact *in vivo* where enclosed, unaided thermal power dissipation is unavoidable. This is predicted to be a future issue of concern for such devices as they are increasingly applied to in vivo situations. The trade off between low power and the drive for high spatiotemporal recording is fundamentally difficult to overcome.

On the other hand, for *in vitro* cultures, the ability of such devices to overcome the noise and data gathering issues of passive devices far outweighs the need to provide assisted cooling. In such cases the power consumption constraints of the front end may be loosened in favour of compact high performance design.

9.6 Conclusion

A good first attempt at a low power design architecture IC has been developed to locally amplify extracellular neural signals and transport the sampled data to the user with minimal off chip interconnection issues. The system proposes on chip buffers, multiplexing and analogue to digital conversion to preserve and compress the bandwidth of the data onto a single digital track for increased noise immunity and operational simplicity. A controllable sampling scheme has also been suggested for increased versatility with high density arrays.

On chip device arrangement and wiring schemes have been discussed and appropriate packaging methods have been considered for prototypical test.

It has been strongly identified that further research must be made to improve the thermal power dissipation of such functional integrated circuitry. The inclusion of heat sinks, Peltier coolers and other methods may present a solution for *in vitro* neural signal measurement where external space, and heat drawing temperature gradients are not at a premium. However if such a device is to be chronically used within an *in vivo* environment, where both heat sinking space and temperature gradients are much more

limited, there is much more work to be performed before the device may be used with the confidence that it is biologically inert. Additionally, there may be much to learn about the effects such devices may have upon the observed neurons during operation as the culture succumbs to the generated heat flux.

9.7 References

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Chapter 10

Thesis Overview and Conclusion

This thesis presented an investigation into a method for recording neural signals at high spatial and temporal resolution. Chapter 2 offered a thorough literature review of the many possible methods that are used for neural signal measurement. Of all these methods, planar micro electrode arrays (MEA) for extracellular signal measurement presented the best method for chronic study of multiple neurons within a single culture or brain slice. It was identified in chapter 3 that planar MEAs must move to CMOS integration in order to overcome routing constraints that limit these devices to less than 100 recording sites per array. Integration would also alleviate the electrical losses that are critical to accurately preserve the low level neural signal. These losses are caused by the unavoidable ground coupled parasitic resistances and capacitances of the connecting tracks and wiring. Amplifying the signal directly at the electrode increases the signal voltage and current. This eliminates the accumulated electrical losses presented by the materials of the substrate tracks and reduces the effects of interference.

The literature review in chapter 2 identified two contemporary integrated circuit methods for measuring neural signals. The first method, denoted the Heer [1] method, required an integrated amplifier circuit per channel that amplified the signal voltage and current of the extracellular neural signal. The second method, denoted the Fromherz [2] method, measured the modulation of the drain current of a transistor that was gate coupled to the extracellular neural signal. Integrated amplifier circuits can provide high gain at a consistent value with little output offset and may be designed to

have a much lower power density than the single transistor implementation. Amplification of the signal at the source reduces the effects of interference as the signal is conducted to the processing circuitry. However, amplifier circuits consume a higher area of the integrated circuit that may be several times greater than that presented to the substrate by a large neuron.

Single transistor devices may theoretically be packed much more densely, but suffer from uncompensated gain inconsistencies and offsets from process variation, require saturation mode operation when used for multiple channels and need switched input offset calibration techniques to overcome systematic drift. These devices also require a current to voltage amplifier circuit to convert the current back to voltage before the signal can be processed or analysed.

It was proposed in this thesis that the point of measurement, full amplifier method was superior to the single transistor method from the point of view of signal preservation and power dissipation. It was proposed that this method could become competitive for high spatial resolution integrated MEAs if the large overhead from passive circuit elements could be overcome. The input capacitors and resistors that form the dc blocking circuit at the front end of neural signal amplifiers were identified as the main cause of this problem. Dc blocking high pass filters are used to remove the dc offset potential and drift that is present at the electrode-electrolyte interface.

It was proposed that a series of new investigations should be made to:

1. Better define the voltage range, source impedance and frequency spectrum for extracellular neural signals.
2. Define the electrical properties of the electrode-electrolyte interface for typical extracellular signal measurement electrodes.

The purpose of the investigation was to concisely define the properties of the signal as it is received by the amplifier input and optimise the amplifier design for these properties with minimal IC area consumption.

The signal properties of extracellularly measured neural action potentials were defined using a novel SPICE circuit model. The model was the culmination of the geometrical descriptions of McNeal [3], Rattay [4, 5, 6] together with the models of Regehr [7, 8] and Fromherz [2] that described the extracellular cleft to electrode coupling for extracellular planar microelectrode arrays. The model used the Hodgkin Huxley [9] equations to describe the non linear conductivities of the ion channels and to simulate the expected waveforms. The duration of the simulated action potential could be controlled to describe a range of extracellular neural signals. The model showed good correlation to the experimentally recorded data presented by Regehr [7, 8] and Fromherz [2]. The fitted model was used to simulate the extracellular neural signals in the cleft over a range of physical parameters such as neuron diameter and seal resistance to determine the effect of these physical parameters upon the electrical properties of the signal. The results were used in chapter 8 to assist in the design of a compact optimised neural signal amplifier circuit.

Chapter 6 and 7 investigated the electrical properties of the measurement electrode interface with the neuron's extracellular fluid. The investigation was performed with a view to exploit the interfacial properties of Pt and Au electrodes to reduce the area of the recording circuit.

Chapter 6 proposed an electrode model that incorporated the dc and ac properties of Pt and Au electrodes. The chapter showed that the interface between Pt or Au electrodes and saline could not present a dc signal path due to the low electrochemical reactivity of the metal. The interface also displayed an intrinsic dc offset potential of several hundred millivolts that must be removed to prevent input amplifier saturation. The electrical noise of the interface was determined in the literature to be due to thermal noise caused by the dissipative real part of the interfacial impedance.

Chronopotentiometric measurements and other experimental evidence from the literature showed that between - 0.83 V and 1.23 V relative to the standard hydrogen electrode the charge transfer between Pt, Au and saline was limited to sorption of dissolved ions such as H^+ and Cl^- within the saline solution. This presented a large frequency dependent surface capacitance combined in series with a dissipative

frequency dependent resistance. Beyond this potential range, dc charge transfer is possible by the electrolysis of H_2O.

The chapter concluded that under equilibrium conditions the electrode-electrolyte interface presented a large surface capacitance and large dc surface resistivity that may be exploited to remove the interfacial offset potential. This would remove the need for on chip passive circuit elements that were identified in chapter 3 as the main reason that the amplifier circuits could not be reduced to the much smaller surface area required for 1:1 neural signal measurement. A method was proposed that was based upon the pioneering work of Wise et al. [9, 10, 11] for the novel application of reducing the amplifier circuit to a minimal area for high spatial density neural signal recording. A front end circuit was proposed to remove the dc offset and low frequency drift without reducing the quality of the measured neural signal. This was ensured by considering the electrical properties of the simulated CAP signal.

Chapter 7 investigated the electrical properties of thin film Pt and Au electrodes. Thin film electrodes were fabricated on quartz substrates to emulate the CMOS post processing that would be required in the development of an active MEA circuit. The ac and dc electrical properties of Pt and Au electrodes were extracted and applied to the model defined in chapter 6. Au was decided to be the most suitable electrode material as the electrode capacitance is much less dependent upon frequency and Au is a much easier metal to pattern and process with photolithographic methods. The model was applied to the circuit proposed in chapter 6 and the offset removal and high pass filter properties of the circuit were demonstrated using thin film Au microelectrodes and an off the shelf amplifier integrated circuit. The circuit showed good correlation to the predicted response.

Chapter 8 developed this circuit into a novel transistor based amplifier circuit for fabrication on silicon. The device was custom designed to the specifications determined in the previous chapters and uses the interface capacitance of the surface electrode to reduce the area cost exacted by monolithic passive devices. The amplifier circuit was designed to be integrated beneath the electrode (formed by the top metal) and consumed an area of less than 60 µm x 60 µm. The design determined that the power consumption, noise performance and size of the amplifier were inversely

interdependent and at this level of operation certain compromises had to be made to ensure adequate operation. As a result, for the device to fit into the specified area and display a reduced input referred noise, the current had to be raised to a level four times greater than that deemed acceptable for direct connection to neurons without additional cooling. However, the power density of the device was much lower than several contemporary devices, such as presented by Heer [1] and Eversmann et al. [12]. Active cooling was suggested as a solution to the thermal power dissipation problem. The device was developed to provide a fundamental low pass filter function at 5 kHz and included an input coupling MOS-R resistor to form a 10 Hz high pass filter circuit at the amplifier input using the interfacial capacitance of the Au electrode. The electrode model developed in chapter 7 was used to determine the sizing of the MOS-R resistor. The device was developed to the layout stage for fabrication.

Chapter 9 developed the amplifier design to constitute a prototype active MEA design and discussed the peripheral circuitry that would be required to develop the system into the final versatile device. Issues such as the challenges of fast switching and sampling of low current signals were discussed and the need for intermediate higher power buffers was developed. A buffer circuit was presented for a 256 element array to be sequentially sampled at 2.56 Mhz. The device consumed 426 µW (17 times that of the input amp) and is presented in the layout stage for fabrication. Prototype 16 element and 256 element arrays were presented at the layout stage and a hypothetical full system design was discussed for further work. Several packaging schemes were discussed for the final fabricated IC for use *in vitro* and *in vitro* situations.

The chapter concluded with the observation that for such active MEA circuits as the one presented in this thesis, the fundamental limiting factor will become the device power dissipation. For large arrays of many high density active electrodes this limiting factor is expressed by the necessity of low power devices to exhibit large transistor lengths to reduce the fundamental noise of the amplification circuitry, maintain the gain generating output resistance of the device and balance the output current mirrors by moving the transconductance out of the subthreshold region. For extreme low power operation, the area of the device may become many times larger than that of the neurons to be measured and reduce the available recording density.

Furthermore, high density active electrodes will require high sampling rates and thus larger currents to slew the signal to the input of the ADC. The current required to slew the ADC input capacitance at the necessary sample rate will typically be far greater than that provided by the low power amplifiers. This may be solved by the use of dedicated buffer circuitry for each device negating the benefits of the low power front end. This challenge is further compounded by the power dissipation of ancillary ADC circuitry that is also desirable for an integrated system.

In conclusion, this thesis has presented the concept of a compact amplifier circuit design motivated by the desire to increase the spatial density of MEAs and integrated circuit MEA solutions. The circuit properties were designed to accommodate the spectral frequency range of the extracellular neural signal and provide adequate gain and input impedance to amplify and preserve the signal amplitude and shape. The signal properties of the extracellular neural signal were extracted from a novel SPICE simulation of the extracellular cleft action potential (CAP) that was based upon quantitative physiological modelling.

The electrical properties of Au electrodes in saline were investigated to exploit the properties of the interface for a novel circuit area reduction technique. It has been determined that the high capacitance per unit area of this interface, which is typically two orders of magnitude greater than that available on chip, can be used to reduce the passive device overhead of integrated circuitry. A circuit design has been proposed that removes the non-ideal effects of this interface such as drift and the halfcell potential to an adequate level that does not reduce the effectiveness of the amplifier. By using this method, the front end circuitry may be reduced to a far more compact size.

A 24.7 µW ASIC amplifier circuit has been developed in the AMS 0.35 µm process to the layout stage with a 20 µm diameter and 100 µm pitch between devices. The need for peripheral circuitry for high density active electrode integration has been identified due to the demands of switched channel handling and effective signal sampling criteria. A conceptual full system design, including analogue to digital conversion, selective channel handling and sampling control has been outlined and two prototype devices have been developed to the layout stage for fabrication and testing. The

device will allow high signal integrity, low noise monitoring of neuron networks approaching a one to one level of cell observation.

Packaging schemes have been discussed for prospective *in vitro* and *in vivo* applications to provide protection of the device and the cellular matter it is in contact with during use.

This device, along with the recent attempts of others, has been deemed more suitable for *in vitro* neurological measurement than for *in vivo* due to the issues associated with device cooling and cellular necrosis from heating effects from thermal power densities exceeds 80 mW / cm². It is predicted that the predominant limitation to active MEA devices will be this unavoidable power dissipation and the unfavourable relationship between device sizes, power density, input referred noise and signal slewing. However, knowledge of such challenges will aid the developmental strategy of subsequent work and provide insight into possible future solutions.

10.1 References

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Appendices

Appendix A

VerilogA Model and Structure for Cadence Virtuoso

Part 1: Hodgkin and Huxley Model

Na^+ Channel Model

```
// VerilogA for NEURON, Na_channel, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Na_channel(vi,ve,hh,mm,gnd);


inout vi,ve,gnd;

output hh, mm;

//set parameters accessible in Virtuouso properties manager

electrical vi, ve, hh, mm,gnd;
parameter real m_zero=0.05;
parameter real h_zero=0.6;
parameter real g_na_bar = 0.120;
parameter real vrest = -0.07;
parameter real surfarea = 1;

//siemens/cm2

parameter real V_na= 0.115;

parameter real k_temp=2.3;

real vr, vr2, vred, alpha_m, alpha_h, beta_m, beta_h, m_val, h_val,
i_na, m_dot, h_dot;

analog begin

@ (initial_step) begin
m_val = m_zero;
h_val = h_zero;
i_na = 0.0;

end

vr = (V(vi,ve)-vrest);
```

```
vr2 = (V(vi,ve)-vrest);



alpha_m =(2.5 - (vr2  * 100.0) )  / ( exp (2.5 - ( vr2 * 100.0) ) -
1.0);

beta_m = 4.0 *  exp( -vr2  / 0.018);

beta_h = 1.0 / ( exp( 3.0 - (vr2  * 100.0) ) + 1.0 );

alpha_h = 0.07 * exp( -vr2   / 0.020 );

m_dot = ( alpha_m * (1 - m_val) - (beta_m * m_val) ) *k_temp;
h_dot = ( alpha_h * ( 1 - h_val) - (beta_h * h_val) ) *k_temp;

m_val = m_val + (m_dot*1e-4);
h_val = h_val + (h_dot*1e-4);


i_na = g_na_bar*m_val*m_val*m_val*h_val*(vr-V_na)*surfarea ;


I(vi,ve) <+ i_na;

V(gnd) <+ vr;
V(hh) <+ h_val;
V(mm) <+ m_val;

$bound_step(0.1e-6);

end


endmodule
```

K^+ Channel Model

```
// VerilogA for NEURON, K_channel, veriloga

`include "constants.vams"
`include "disciplines.vams"

module K_channel( vi, ve, nn, v_r );

inout vi, ve;

output nn, v_r;

//set parameters accessible in Virtuouso properties manager

electrical vi, ve, nn, v_r;
parameter real n_zero=0.32;
parameter real g_k_bar=0.036;
parameter real surfarea = 1;
```

```
parameter real V_k=-0.012;
parameter real vrest=-0.07;
parameter real k_temp=2.3;
real vr, vr2, alpha_n, beta_n, n_val, i_k, n_dot;

analog begin

@(initial_step) begin
n_val = n_zero;
i_k = 0.0;

end

vr = ((V(vi,ve)-vrest));
vr2 = ((V(vi,ve)-vrest));

alpha_n = (0.1 - (vr2*10.0)) / ( (exp( 1.0-(vr2*100.0) ) -1.0)) ;

beta_n = 0.125*exp(-vr2/0.080);

n_dot = (( -alpha_n - beta_n) * (n_val) + alpha_n ) *k_temp;

n_val = n_val + (n_dot*1e-4);

i_k = g_k_bar*n_val*n_val*n_val*n_val*(vr - V_k )*surfarea;

I(vi,ve) <+ i_k;

V(v_r) <+ vr;
V(nn) <+ n_val;

$bound_step(0.1e-6);

end

endmodule
```

Leak Channel Model

```
// VerilogA for NEURON, leak, veriloga

`include "constants.vams"
`include "disciplines.vams"

module leak(vi,ve);

inout vi,ve;

electrical vi, ve;

//set parameters accessible in Virtuouso properties manager

parameter real V_l=0.0106;
parameter real vrest=-0.07;
parameter real g_l = 0.0003;
```

```
parameter real surfarea = 1;
real i_l, vr;

analog begin

@(initial_step) begin
i_l = 0;
vr = 0;

end
vr = ((V(vi,ve)-vrest));


i_l = g_l*(vr-V_l)*surfarea;

I(vi,ve) <+ i_l;

$bound_step(0.1e-6);

end

endmodule
```

Part 2 Model Cell Structure in SPICE

The VerilogA models were combined with the membrane capacitance into modular cells for Cadence Virtuoso as shown in figure A1. Figure A1 is the cell block representing figure 4.2 in the main thesis body. Each VerilogA ion channel description may be individually modified in the GUI property manager allowing simple access to the model parameters as shown in figure A2. Passive component variables may be set similarly. Parameters are set to define the electrical properties for the defined geometries for each sub-compartment in the model as illustrated in figure A3. Access to internal properties of each cell, such as rate variables m, h and n, is included for circuit debugging.

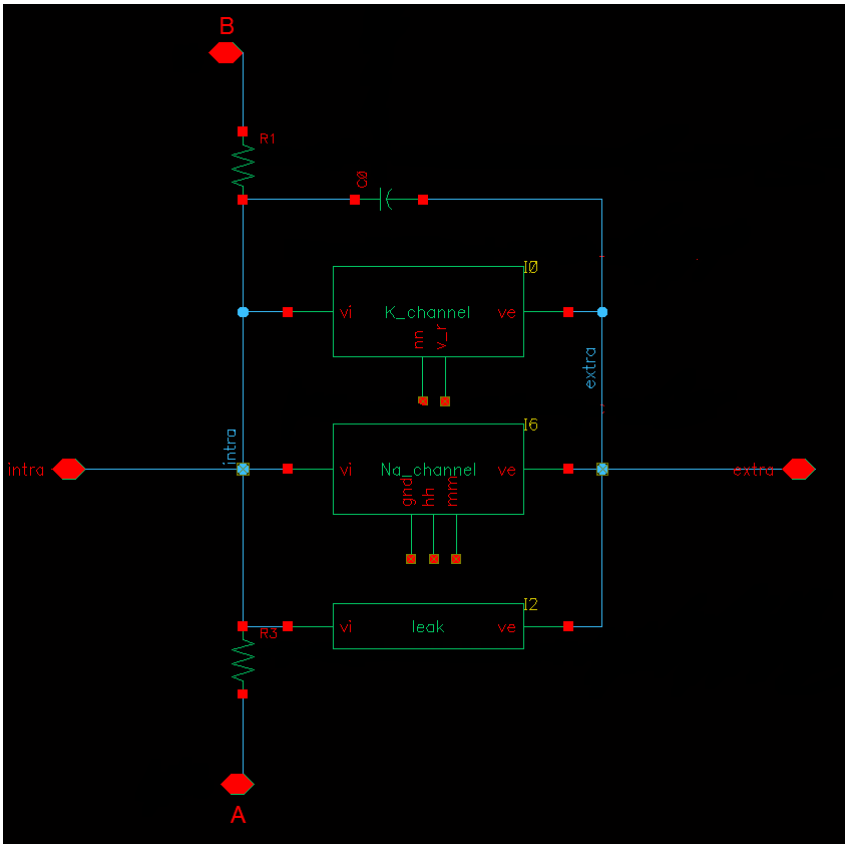

Figure A1

A Hodgkin Huxley Cell

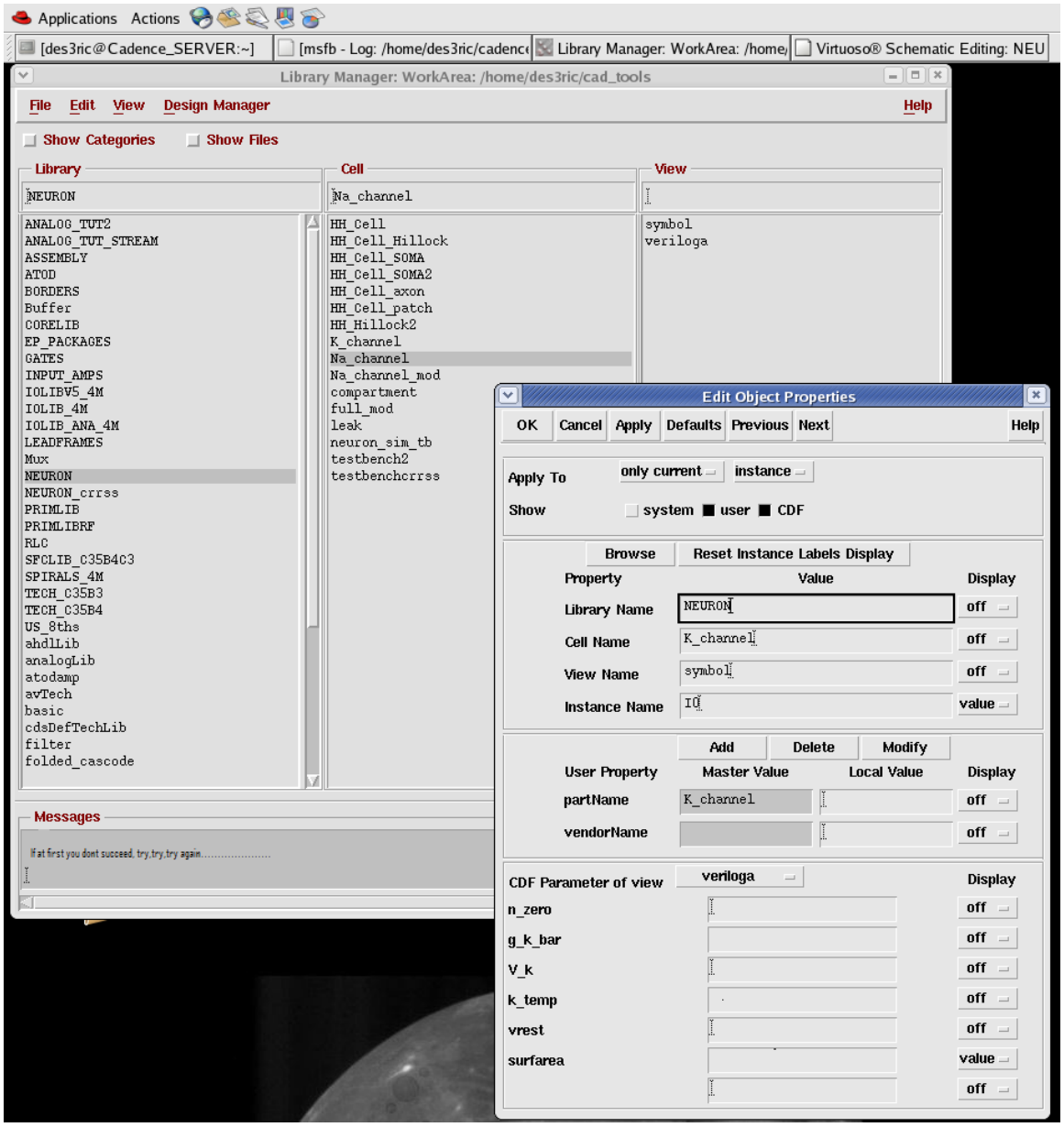

Figure A2

GUI Access of the Model Parameters. The example shows the properties editor for a generic K channel

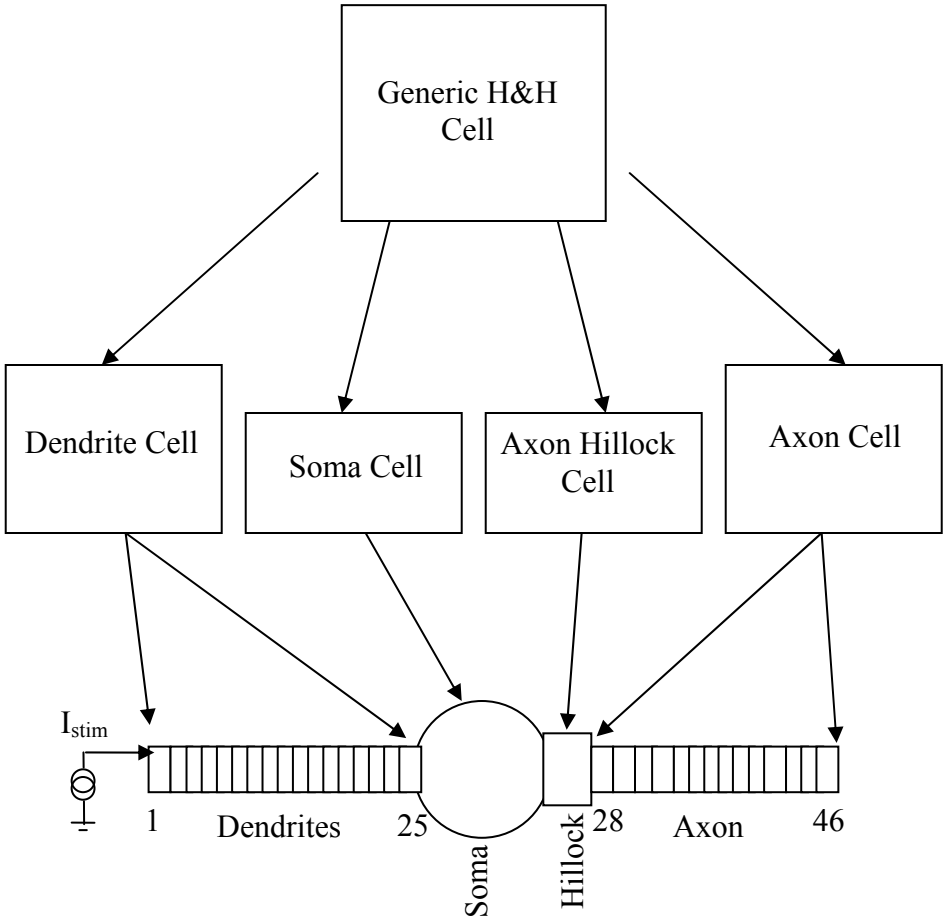

Figure A3

Each sub-compartment model is defined from the master cell by modifying relevant variables

Once variables have been set for each sub-compartment type they may be accessed and modified directly by the Analog Design Environment program. This is shown in figure A4.

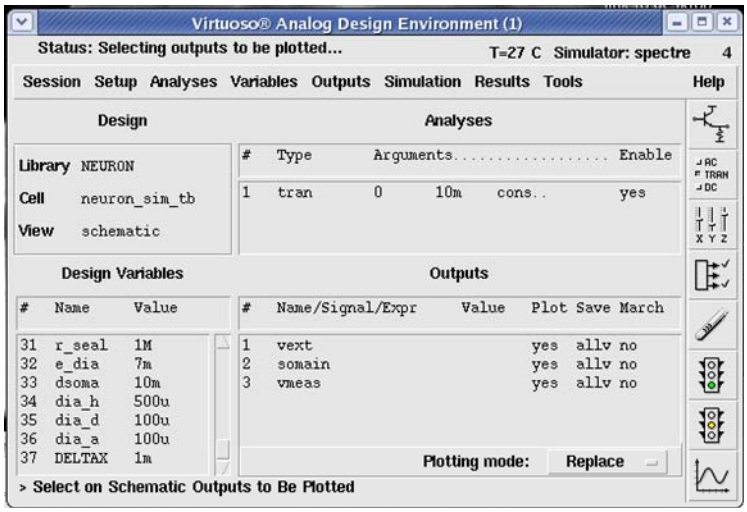

Figure A4.

Design Variable Access in the Analog Design Environment Simulation Window

The model is built up as shown in figure 4.11 with each compartment's individual physical properties set using the GUI. In the simulation test bench the sub-compartment models are combined to form the neuron model defined in chapter 4. Extracellular electrical connections and passive components are defined as described in 4.2-4.4. Design Variables within the Analog Design Environment (ADE) are listed in Table A1 with a corresponding property description.

ADE Variable	Description	Symbol	Range	Units
r_seal	Cleft seal resistance	Rseal	0-10	MΩ
dia_h	Axon hillock diameter	d_h	5-20	µm
dia_d	Dendrite diameter	d_d	1-5	µm
dia_a	Axon diameter	d_a	1-5	µm
DELTAX	Sub-compartment length	Δx	0.2-1	µm
dsoma	Soma diameter	d_s	10-100	µm
cm	Membrane capacitance	c_m	1	µF/cm²
stim_amp	Amplitude of stimulus current	-	0.5-10	nA
stim_width	Width of stimulus current	-	300	µs
rho_i	Intracellular resistivity	ρ_i	0.3	kΩ cm
rho_e	Extracellular resistivity	ρ_e	0.07	kΩ cm
K_temp	Ion channel velocity correction	K	0.2 - 9	-
e_dia	Extracellular electrode diamter	d_e	1-100	µm
gkbar_soma	Maximum potassium conductance at soma	-	0 - 36	mS cm^{-2}
gnabar_soma	Maximum sodium conductance at soma	-	0 - 120	mS cm^{-2}
gl_soma	Leakage conductance at soma	-	0.3	mS cm^{-2}
gkbar_hillock	Maximum potassium conductance at hillock	-	36	mS cm^{-2}
gnabar_hillock	Maximum sodium conductance at hillock	-	120	mS cm^{-2}
gl_hillock	Leakage conductance at hillock	-	0.3	mS cm^{-2}
gkbar_dendrite	Maximum potassium conductance at dendrite	-	-	mS cm^{-2}
gnabar_dendrite	Maximum sodium conductance at dendrite	-	-	mS cm^{-2}
gl_dendrite	Leakage conductance at dendrite	-	-	mS cm^{-2}
gkbar_axon	Maximum potassium conductance at axon	-	36	mS cm^{-2}
gnabar_axon	Maximum sodium conductance at axon	-	120	mS cm^{-2}
gl_axon	Leakage conductance at axon	-	0.3	mS cm^{-2}

Table A1

Default Simulation Variables

Appendix B

Electrode Array Fabrication Materials

Materials

Substrate and Metalisation

Quartz Wafers 50 mm dia. x 2 mm. (Multilab)
Titanium e-beam target (Goodfellow)
Platinum Wire (Goodfellow)
Gold Wire (Goodfellow)

Lithography

Shipley Microposit S-1813 (Chestech).
Shipley 351 Developer (Chestech).
Shipley 1112A Remover (Chestech).
SU-8 10 (Chestech).
Shipley Microposit EC Solvent [SU-8 developer] (Chestech).
ECA Solvent (Chestech).
Shipley Microposit MF 319 [sidewall developer for overhang in lift off process] (Chestech).

Masks

3” x 3”x.060” Sodalime Chrome Blanks: Grade PG, Optical Density 2.8, Reflectivity 8%, Resist type AZ1500, Resist Thickness 5300 Å, with 30 min bake time @ 103°C. (TELIC)

Etchants

Gold Etch (KI: I_2: H_2O 4 g:1 g:40 ml) .
KI (Sigma).
I_2 (Sigma).

Chrome Etch ($(\underline{NH_4})_2Ce(NO_3)_6$: HNO_3: H_2O 20 ml: 6 ml: 74 ml to make up 100 ml vol.).
$(\underline{NH_4})_2Ce(NO_3)_6$ (Sigma).
HNO_3 (Sigma).

Titanium Etch (HF: H_20) 1:1

HF (Sigma)

Appendix C: Electrode Array Fabrication Recipes

Substrate Preparation

Sonic cleaning in Decon90 : H_2O, 1:1 , 15 mins.
Immersion in 'Piranha' solution (H2O2 : H2SO4 3:1), 30 mins.
Immerse remove and rinse in H_2O.
Bake 5 mins 90 °C.

Mask Patterning

Heidelberg Mask Writing: 405 nm Coherent Cube Laser (100 mW):
4mm write head: Defoc 2800, Power 18 mW.
Develop in 351 : H_2O (1 : 5) for 40 sec -1 min.
Chrome etch (until clear, ~40 sec-1 min).

Gold Patterning

E-beam evaporative deposition of Ti to 20 nm at 1 x 10^{-6} torr.
E-beam evaporative deposition of Au to 200 nm at 1x10^{-6} torr.
Spin coating 1813:
Spreading Stage @ 500 rpm for 5 sec.
Spin Coating Stage @ 3700 rpm for 30 sec.
95 °C contact bake for 5 min.
Align Au Mask and expose (Vacuum Hard Contact) 72.6 mJ/cm^2. [EVG Broadband Source 350 nm - 450 nm].
Develop in 351 : H_2O (1 : 5) for 40 sec -1 min.
Rinse in H_2O and blow dry with nitrogen.
Gold Etch (40 sec - 1 min).
Rinse in H_2O and blow dry with nitrogen.
Titanium Etch (40 sec – 1 min).
Rinse in H_2O and blow dry with nitrogen.
Strip resist layers with 112A Remover 5 mins.
Immerse in Acetone then H_2O. Rinse with H_2O.

Platinum Patterning (Lift off process)

Spin coating 1813:
Spreading Stage @ 500 rpm for 5 sec.
Spin Coating Stage @ 3700 rpm for 30 sec.
95 °C contact bake for 5 min.

Soak in MF319 (inhibition soak top layer).
Align Pt Liftoff Mask and expose 5.5 sec (Hard Contact Vacuum), (72.6 mJ/cm^2).
2 min bake.
4 min development in MF319.
Immerse in H_2O and then rinse in H_20.
95 °C contact bake for 1 min.
E-beam evaporative deposition of Ti to 20 nm at 1 x 10^{-6} torr.
E-beam evaporative deposition of Pt to 130nm at 1x10^{-6} torr.
Immerse in Acetone to Strip 1813 and Lift off un-adhered Pt.
Rinse in H_2O and blow dry with nitrogen.

SU-8 patterning

160 °C dehydration bake 5 mins.
Spin coating SU-8 10:

Spreading Stage @ 500 rpm for 5 sec.
Spin Coating Stage @ 2000 rpm for 30 sec.

Prebake @ 65 °C for 2 min, slow ramp up to 95 °C and leave for further 5 mins.
Align SU-8 Mask and expose 11.5 sec (Hard Contact Vacuum), (150 mJ/cm^2).
Post bake @ 65 °C for 1 min. Slowly ramp up to 95 °C for 2 min.
Immerse in EC solvent for 1.5 min.
Wash in ECA solvent.
Wash in isopropyl alcohol.
Wash in H_2O.

Post Fabrication Ion Etch

The etching was performed in an Oxford instruments Plasma Lab 80 Plus reactive ion etcher.

The configuration was as follows:
8 inch platen with quartz cover plate
Chamber pressure 200 mtorr
RF power 100 W
Oxygen flow rate 50 sccm
Stage temperature 20 °C

Etch for 5 mins.
Generated electrode self bias: 186 V

Appendix D

Published Paper in IEEE PhD Research in Microelectronics and Electronics

A Versatile Low Power Integrated Circuit for the Recording and Analysis of In-Vivo and In-Vitro Neural Signals

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ABSTRACT

This paper proposes a high resolution recording device for medical and biological research applications investigating nerve firing patterns, especially where a high degree of spatial discrimination is required. The device has been designed for low power operation with the intention of powering by RF frequency carrier wave which will is also expected to be the basis of communication between the device and the monitoring unit. A 10bit signal resolution at variable sample rates, adjustable between 10-100 kHz by internal control logic, combined with 128 spatially orientated channels will allow a highly detailed capture system suitable for complex DSP evaluation.

1. INTRODUCTION

In recent years there has been a significant growth of active interest in the application of the latest generations of VLSI technology toward niche areas within the biological domain. Complex functionality, combined with the current low power and wireless communication technologies available presents the possibility for developing convenient implantable medical devices suitable for chronic disease monitoring, physiological investigation, or nerve signal control of motorized prosthetics. High data conversion rates, sensor density equivalent to neural cell spacing and remote powering schemes make such devices ideal instrumentation for nerve culture or dissection study within the laboratory.

This paper presents the full custom design of a low power, high resolution device capable of the accurate recording and presentation of Action Potential data recorded from 128 spatially orientated points. The device was originally intended for nerve bundle signal recording and discrimination but can be easily adapted to other less ambitious applications. A general system block diagram is presented in Fig. 1.

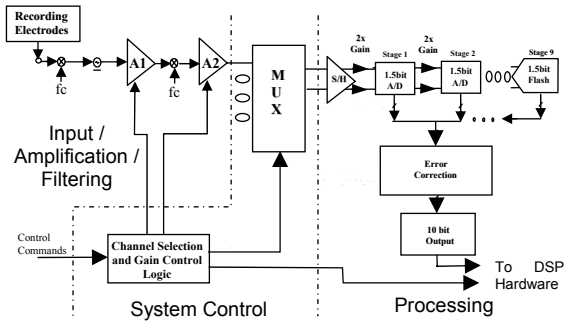

Figure 1. System Block Diagram

2. INPUT SYSTEM

The system described in this paper consists of the measurement, amplification and digital conversion of neural signals into 'raw' continuous time data for intended 'on chip' processing. It is intended that the device will be initially manufactured as a flat array with electrodes presented on the surface of the insulated chip allowing direct contact testing with the biological media. An example of this structure type is illustrated in Fig. 2.

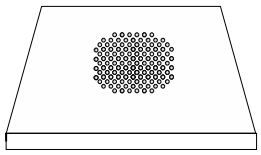

Figure 2. Illustration of on-Chip Electrode Layout Concept.

2.1 Electrode Materials

The contacts will be coated accordingly for two separate methods of ionic charge detection; capacitive coupling and direct charge transfer with a metallic layer. To investigate capacitive detection, the protruding electrodes will be passivated with SiO_2 grown over the surface of half of the electrodes. Encompassing the remaining electrodes, a non reactive, high charge delivery capacity metal such as IrOx or Pt [1] will be used, ensuring low impedance between the ion/electron charge based domains and preventing media contamination with reaction byproducts.

The application of two signal sensing materials will demonstrate the performance of each recording method on chip, with respect to interfacial noise, transferred signal magnitude and cellular interaction at the electrodes. It is of course the ideal case that a totally passivated fully operational I.C could be developed for immersion in biological media, both in terms of manufacturing and general biocompatibility.

It is intended that various biological materials, ranging from cell cultures and dissected retinas, to in-vivo invertebrate ventral nerve trunks, can be monitored using this platform.

2.2 Input Amplifier

The input amplifier array consists of 128 separate Class A-B high gain differential pre-amplifiers (Fig. 3) connected to a low gain, high swing second stage.

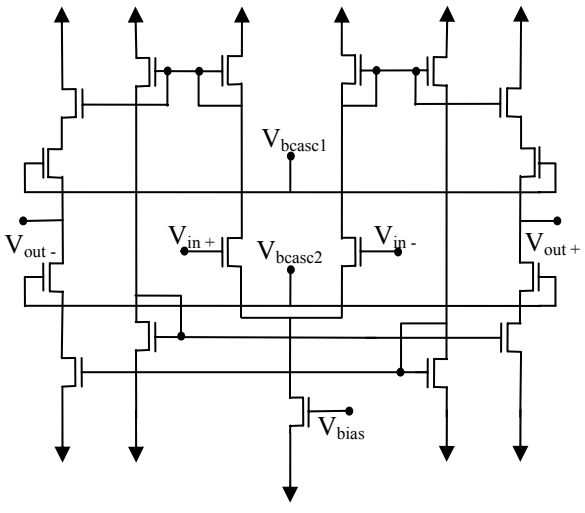

Figure 3: Class A-B Amplifier Topology

The Amplifiers are connected in a chopper-stabilized [2] manner with simple transmission gate style input switches and bootstrapped [3] intermediate stage switches. The first stage amplifiers were designed to give good frequency response and low thermal noise characteristics, the second stage designed for low 1/f noise characteristics and poor frequency response.

A high signal to noise ratio is obtained by the modulation of the input signals to the chopper switching frequency of 500 kHz before amplification. The process shifts the low frequency input signal onto the high frequency side band harmonics of the +/- 1 multiplying square wave function. The harmonics are therefore far above the 1/f noise corner of the preamplifier and consequently are not swamped by this contamination. This method alleviates the necessity for very large, slower p-type transistors for input devices and higher bias currents.

Directly after the preamplifier the signal is demodulated back down to its original frequency and the noise is modulated to the square wave sidebands by the same principle. A bootstrapped switch is used in this instance preventing FET resistive variations between source and drain altering the signal. The signal is amplified again by a low frequency output amplifier acting as a filter/buffer, attenuating the high frequency components of the signal now attributed solely to noise. This process is illustrated in Fig. 4.

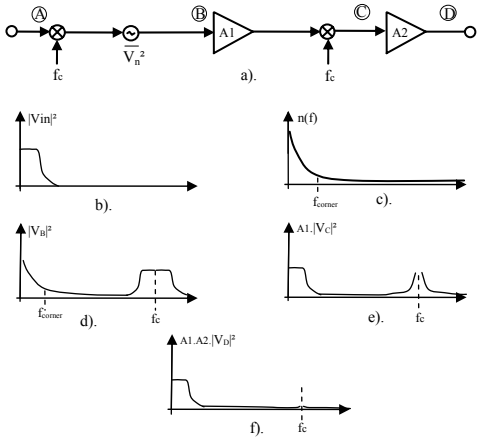

Figure 4: Chopper Modulated Input Amplifier [4]
(a) block diagram, (b) input spectrum (node A), (c) noise spectrum, (d) node B spectrum, (e) node C spectrum, (f) node D spectrum.

By using this modulation technique the dominating effects of 1/f noise on the frequencies of interest are all but eliminated, however thermal noise effects must also be considered. Noise analysis of the circuit illustrated in Figure 3 produces the following relationship between the rms noise and the transistor dimensions:

$$eni^2_{Thermal} = \frac{16kT}{3gm_1}\left[\left(1+\eta_{m_1}\right)+2\left(1+\eta_{m_1}\right)\cdot\frac{gm_3}{gm_1}+\left(1+\eta_{m_1}\right)\cdot\frac{gm_7}{gm_1}\right]$$

As η_{m1} is small, the topology ideally suited for minimal thermal noise is dominated by having the input devices much larger than that of the output. A resulting trade off is thus presented between the minimum desired noise contamination, consumed chip area and device speed; however this is not as severe as it would be with 1/f noise across the frequency band of interest.

The gain of the circuit is controllable between 70-90dB via control of the cascode compensated output resistance.

The amplification circuit has been designed and simulated with the AMS 0.35µm process parameters and exhibits an RMS noise floor between DC and 2 kHz of less than 0.5µV. Power consumption per amplifier has been simulated at under 100µW.

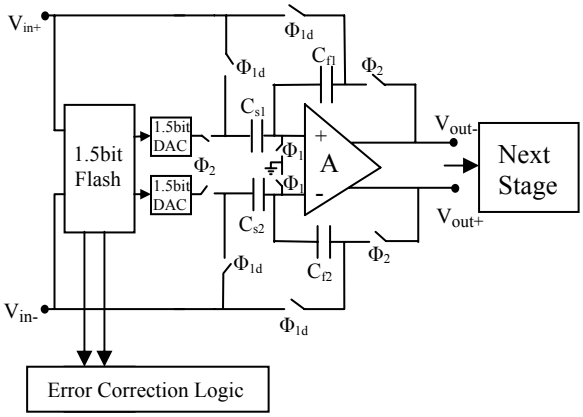

Figure 5. 1.5 Bit Pipelined A/D Stage

3. ANALOGUE TO DIGITAL CONVERSION

All 128 signal channels are multiplexed onto a single high performance 10bit, 1.5 bit / stage pipeline A/D converter. The multiplexer is programmable as described in section 4, in that certain address combinations can be accessed more frequently, at the expense of others, if instructed by the monitoring computer.

This particular A/D architecture is preferable to the design because of its high speed, ease of obtaining the proposed 10bit accuracy and relatively low power implementation. The A/D is designed to operate at a sample rate of 1.5Ms/s to accommodate a minimum sampling rate of 10 kHz per channel. Each stage is composed of a switched, cascode compensated amplifier [5], [6], [3] and two low power dynamic comparators, allowing the full circuit to operate at under 8mW. Common mode feedback is provided by a simple switched capacitor technique [7].

The power dissipation through the pipeline is proportional to the charging and discharging of the sampling capacitors. As the sampled signal travels down the amplified stages less and less accuracy is demanded from both the amplifiers and the sampling/feedback capacitors. Careful scaling of the capacitors and the amplifiers considering stage gain accuracy and noise / process errors enabled the final simulated design to remain well below the 10mW goal.

The 1.5bit/stage architecture (see Fig. 1 and Fig. 5) was adopted due to its high level of immunity from comparator offset error and overall low power prospects with a small complexity overhead of digital error correction. The digital error correction logic comprises of a standard predictive carry adder circuit that corrects comparator offset errors of up to $V_{REF}/4$ per stage and allows much smaller, less power consuming, fully dynamic comparators to be used in the design [8].

The single stage circuit shown in figure 5 operates by first taking a 1.5bit flash conversion of the input voltage (V_{in}) at $t = \Phi_{1d}$. This is value is then routed to the error correction logic for conversion into the digital output. At this time V_{in} is also sampled onto the both the feedback capacitor C_f, and the input sampling capacitor C_s, while the amplifier input is reset to ground. The advanced amplifier input reset Φ_1, allows total discharge of charge residue on capacitors C_s and C_f before the input is sampled.

At $t = \Phi_2$, the analogue input is disconnected and the capacitors C_s and C_f remain charged to V_{in}. C_f forms a negative feedback loop around the amplifier and the input capacitors are now switched to the DAC output V_{DAC} which provides either V_{ref}, 0 or $-V_{ref}$; the quantized 1.5 bit representation of the analogue input voltage level. This value is subtracted from the capacitor C_s and the residue is passed to the next stage. The overall transfer function of the closed loop circuit at $t = \Phi_2$ is:

$$V_o = \left[1 + \frac{C_s}{C_f}\right] \cdot V_{in} - V_{DAC}$$

For a 1.5bit architecture $C_f = C_s$ giving a residue at V_{out} of $2V_{in} - V_{DAC}$.

The design is implemented in a fully differential manner to maximize the signal to noise ratio and address the compromise between the high gain of the amplifier and resulting limited signal swing inherent to the single stage architecture.

4. RECONFIGURABLE RECORDING ARRAY

When analyzing neural firing patterns, the relative positioning of recording sites with respect to the cells of interest, combined with adequate sampling rate is imperative for optimal information extraction. It is therefore desirable to implement control over both the position of the active recording sites and the frequency at which they are sampled. For this purpose an amplifier array of 128 electrodes will be created on the device from which all can be sampled at 10kHz, or a selection at a multiple of 10kHz.

An internal state machine will control the addressing of the amplifiers via the updating of a programmable look up table controlling the multiplexer, by the external monitoring computer. Thus the amplifiers can be accessed randomly for any given sample period within the maximum sampling rate. Amplifier gain is also state machine controlled, with all amplifiers collectively locked at the specified gain level to ensure linearity in the signal processing blocks.

5. POWER AND COMMUNICATION

The device is ideally suited to RF powering as it is designed to consume less than 25mW at 3V supply. Recent publications have demonstrated implantable devices obtaining up to 100mW from antenna coils of approximately 10mm diameter [9]. The low power consumption of the device, combined with even distribution of dissipated heat and careful antenna packaging would fall well below the biologically safe heating criterion of 60mW/cm² [10].

It is intended that a further processing block will be incorporated into the design to alleviate some of the high data throughput demanded of the R.F communication system by the 'raw' sampled recording data.

These areas of design will be formalised when the input and digital conversion system have been physically proven.

6. CONCLUSION

A multi-channel, high resolution device for the study of neural signals has been presented. The device is low power and ideally suited for RF powering, making it an ideal candidate for chronic study where either implantable or an unmolested measurement process is preferable. The device has been designed with an inbuilt selective gain and sample rate control and exhibits a low input referred noise floor allowing minimum 8dB signal to noise ratio when studying neural spikes with magnitudes as low as 2μV.

It is anticipated that with the portable analysis of multiply sourced spikes at high resolution and sample rate, combined with spatial, time referenced algorithms, a greater understanding of neural systems can be gained. With such methods traditional techniques of single axon and jumbled compound measurement may be de-convolved into meaningful power distribution patterns describing network functionality and signalling pathways in biological systems.

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Appendix E

ASIC Prototype Arrays for Test

This appendix contains the layout schematics for the 16 and 256 element test arrays.

Centre_For_Electronic_Systems_2007
University_Of_Durham

VDD

A3

A2

A1

A0

OUT

GND

VSS

R_Curry_2007

austriamicrosystems
2003

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R Curry 2007