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Sowmya Kolli
University of Louisville

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VERTICAL GALLIUM NITRIDE SCHOTTKY DIODES FOR POWER SWITCHING APPLICATIONS

By

Sowmya Kolli
B.S., Jawaharlal Nehru Technological University, 2010
MS., University of Louisville, 2012

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A Dissertation Approved on

December 14, 2017

by the following Dissertation Committee:

Dissertation Director
Dr. Bruce W. Alphenaar

Dr. Mahendra K. Sunkara

Dr. Shamus McNamara

Dr. Kevin Walsh

DEDICATION

This dissertation is dedicated to my parents, grandmother, and brother. I thank my family for the confidence and support they have shown on me throughout my life. This work is also dedicated to my husband, Viraj who has been a constant source of support and encouragement during the challenges of grad school and life.

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current lab mates Kasun, Austin, and George. The group has been a source of friendships as well as good advice and collaboration. I would also like to thank other graduate students in Shumaker research building for working together late nights before deadlines. Over the course of my stay at the University of Louisville, I had the opportunity to work with students, researchers, and staff from CONN center and Electrical engineering and I thank all of them for their support and help.

ABSTRACT

VERTICAL GALLIUM NITRIDE SCHOTTKY DIODES FOR POWER SWITCHING APPLICATIONS

Sowmya Kolli

December 14, 2017

Gallium nitride (GaN) has enormous potential for use in devices operating at high power, frequency and temperature. Its wide band gap, high critical electric field and favorable carrier properties lead to lower switching losses and conduction losses in power electronic devices. However, most GaN rectifiers reported to date exhibit an ON-resistance (Ron) versus breakdown voltage much below theoretical predictions. Heteroepitaxial growth of GaN on substrates such as SiC, Si, and sapphire suffer from a high density of threading dislocations defects due to the mismatch in lattice constants and thermal expansion coefficients. Vertical devices, in which a bulk GaN substrate is used, have much lower defect densities. However, field crowding at the periphery of the rectifying contact remains a problem and results in avalanche break down at much lower voltages than the theoretical maximum. This work will describe the design, simulation and fabrication of a novel wraparound field plate termination structure for high voltage Schottky diodes. Simulations show that the wrap around structure has an improved electric field distribution leading to higher breakdown voltages than conventional diode designs.

The fabrication process was first developed using low-cost commercially grown HVPE GaN on sapphire substrates. This is the first work in the field of GaN based devices at University of Louisville, so all fabrication processes, including ICP/RIE based dry etch, ohmic metal contact deposition and dielectric deposition steps, were developed and optimized. Current-voltage (I-V) measurements were used to extract on-resistance and break down voltage and these results were compared to simulation. Experimentally found breakdown values differed from the theoretical predictions. Device failure analysis based on I-V characterization showed the presence of additional current conduction paths along the SiNx and the defective HVPE films. To prevent these leakage currents a less defective MOCVD film grown on Ammono bulk GaN was used to fabricate the wrap-around diode.

Planar GaN diodes, and diodes with standard field plate and our novel wraparound field plate were built and tested. Interestingly, planar diodes showed higher performance compared to standard field plate and wraparound field plate designs, contradicting to simulation results. Also, the diodes with a standard and a wraparound field plate structures showed higher leakage currents in both forward and reverse bias. To trace out the source of leakage currents, device failure analysis based on I-V measurements were carried out after each fabrication step of the diode. In this process, initially planar diodes were tested with a Schottky and ohmic contacts formed on top and on the back side of the wafer. Then, diodes with mesa are built and tested. The diodes with mesa showed an improvement in breakdown values, with the highest breakdown voltage of

421V and on resistance of 3 mOhms-cm^2. Also, the experimentally determined breakdown voltages in mesa diodes were found to match with simulation results. Proving that modification in device geometry results in uniform field distribution at the edges and improving the breakdown. Then, a thick SiNx was deposited on mesa diodes using PECVD. The I-V after dielectric deposition showed almost 3 orders higher currents in both forward and reverse bias currents. A similar increase in leakage currents was observed in earlier diodes made on HVPE films. This indicates that PECVD deposited SiNx is modifying the GaN surface and is resulting in additional currents along the GaN and SiNx interface. To overcome these passive currents, a higher K dielectric material was deposited using ALD prior to SiNx. The new bilayer passivation was successful in preventing the leakage currents and resulted in improved breakdown voltages. However, the breakdown values were still below the theoretical predictions and also lower than the diode with a standalone mesa and no additional dielectric layer. Indicating that improvement produced by the device geometry modification is negated by dielectric deposition.

Further, we compared some of our diodes with best breakdown characteristics to the literature. We found that with the given material quality and drift layer thickness, we were able to achieve higher breakdown compared to most of the devices reported in the literature. However, there are few diodes with better on resistance and breakdown values compared to ours. As these diodes used almost 60 to 100 times thicker films compared to ours.

We were able to make Schottky diodes with relatively high breakdown voltages. However, to utilize the effect of wraparound field plate to its fullest potential, there is a need to develop an alternative dielectric material and deposition technique in future.

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CHAPTER 1 INTRODUCTION

1.1 Energy Challenge

In the modern-day energy is generated from a variety of sources such as solar energy, wind energy, fossil fuels, hydel energy and nuclear energy. Generated energy is stored, transported, converted and consumed. The mode of energy consumed can be classified as electricity, heat, chemical, and other forms. Among these, energy consumed in the form of electricity is increasing and is expected to grow more in the future. Figure 1-1 shows the end use of electricity in sectors including residential, commercial, industrial and transportation from 1990 to 2040 in United states.

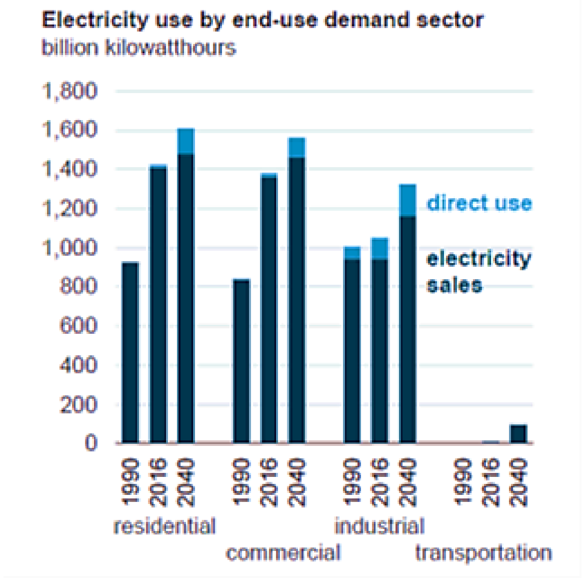


Figure 1-1: Demand for electricity in residential, commercial, industrial and transportation sector (source: US Energy Information Administration)

In 2015, the U.S. Energy Information Administration (EIA) estimated a loss of about 6.31% of electricity in the process of transmission and distribution of electricity. From percentage viewpoint this might appear to be relatively low, but the total estimated electricity loss was 10.8 quads. With the increased need of electricity there is a demand for the efficient and reliable management of electrical energy, and power electronics is a technological domain that deals with the electrical energy conversion by switching for dynamic power management[1]. These power conversions can range from milli watts to thousands of megawatts. Power electronics translate the properties such as voltage, current and frequency to required specifications according to the intended application. These conversions are found in solar inverters[2], automotive industry[3], robotics, and power supplies for electronics[4]. The main principle of power conversion is digital switching. For ideal power electronic switches

(i) The voltage drop in the forward bias (on state) should be zero, i.e. no conducting losses.

(ii) The transition from on state to off state should be instantaneous with no switching losses.

(iii) Leakage current in reverse bias (off state) should be zero, i.e., infinite off resistance.

However, in every conversion process, the power losses[5] are inevitable due to switching. Thus, reduction of this energy loss during power conversions is indispensable for efficient management of electric power in the grid.

Silicon(Si) has served the power electronics industry exceptionally well, in the form of MOSFET, and various adaptations such as IGBT, BJT, and diodes for over 45 years. However, to meet the demand for electricity in future, and to efficiently reduce the losses during modulation of electric power, requires the development of new materials that can operate at higher frequency to shrink the size of passive components and reduce the overall copper loss and higher operating temperatures to cut the additional energy required by heat sinks.

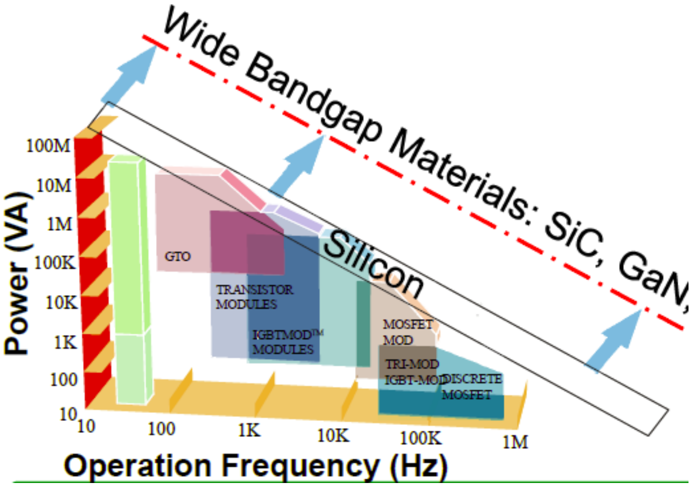


Figure 1-2: Widebandgap material operation range in terms of frequency and power

Also Silicon-based devices have reached the theoretical performance limit set by fundamental material properties and there is considerable attention in the development of wide bandgap materials such as Silicon Carbide (SiC), Gallium Nitride (GaN),Gallium Oxide(Ga_2O_3) and Dimond[6]. The wide bandgap semiconductors because of their material properties as listed in table 1-1, such as bandgap, critical electric field, and higher drift velocity are predicted to have low loss and improved efficiency compared to Si devices.

Semiconductor material	**Units**	**Silicon**	**SiC**	**GaN**	**Ga_2O_3**	**Diamond**
Bandgap	Ev	1.12	3.26	3.45	4.5-4.9	5.5
Dielectric constant(ε_s)		11.8	9.7	10.4	10	5.5
Mobility (μ_n)	cm^2/Vs	1400	950	1245	300	2000
Critical Electric field (E_c)	MV/cm	.25	2.2	3.5	8	10

Table 1-1: Material parameters for Si, SiC[7],GaN[8], Ga2O3 and Diamond[9]

1.2 Wide bandgap material properties and their advantages

1.2. (a) Chemical stability

Group III nitrides and SiC are covalent bond crystals composed of light elements of the second period of the periodic table, which have characteristics of small bond length between the constituent atoms and wide bandgap energy in comparison with Si and GaAs[10]. Figure 1-3 illustrates the relationship between bond length and bandgap for various semiconductor materials. SiC and GaN are in a different domain from conventional elemental and compound semiconductors. These materials have a lower bond length which means that the bonding energy between the constituent atoms is strong and as a result, the chemical stability of WBG materials is extremely high.

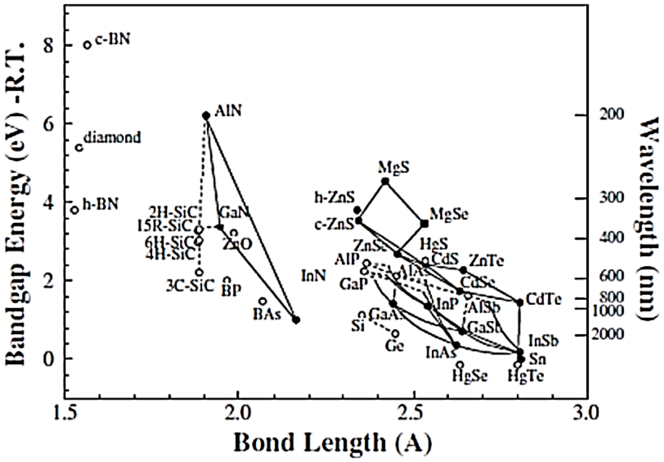


Figure 1-3: Bandgap Vs bond length for different semiconductors [11]

1.2 (b) Higher operating temperatures

The wider bandgap energies in these materials result in lower intrinsic carrier concentration compared to Si or GaAs. Also, due to wide bandgaps, these semiconductor materials can withstand higher operating temperatures (250^{0}C-300^{0}C) before undergoing thermal runaway. On the other hand, Si devices can only operate at temperatures lower than 100^{0}C due to their lower bandgap and higher intrinsic carrier concentration. Thus, the lower intrinsic carrier concentration and wider bandgap make WBG materials attractive for higher temperature function at an ambient temperature >150^{0}C without additional cooling requirements, potentially reducing the volume, weight, and cost of the converter.

1.2 (c) Higher blocking voltages

In reverse bias, the electric field in the drift layer is illustrated in figure 1-3. An avalanche breakdown occurs when the electric field at the junction reaches the critical electric field of the material. As the Critical electric field of WBG materials is ten times higher than Si. This enables devices based on SiC and GaN to block higher voltages for a given drift region width.

$$V_{BD} = \frac{E_c W_d}{2} \quad (1\text{-}1)$$

W_d: Drift layer width
Ec: Critical electric field

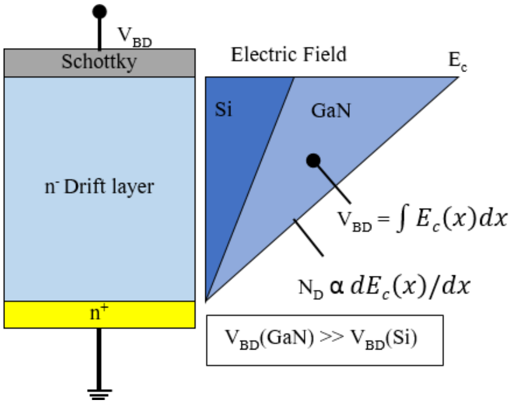


Figure 1-4: Electric field distribution in reverse bias for a vertical Schottky diode

1.2 (d) Lower On-resistance

In the forward bias the potential drop across the drift layer is defined as the specific resistance and is expressed as a function of drift layer width and carrier concentration(N_D). N_D as mentioned earlier is directly proportional to the critical electric field (refer Eq (1-3)) of the material. Since, WBG materials have higher E_C, compared to Si, WBG drift layers can be doped more than ten times higher, and thus the drift layer width can be 1/10 times thinner than Si assuming same breakdown voltage as illustrated in figure 1-5. Substituting, V_{BD} and N_D into Eq (1-2), gives R_{ON} in terms of E_C, μ_n and V_{BD}. From Eq 1-4, it is apparent that material with high Ec and mobility will result in lower Ron for similar breakdown values. A plot of on-resistance and breakdown, are the two critical parameters for evaluating any material system as a switch. As shown in figure 1-6, for a given breakdown voltage WBG materials offer lower R_{ON} there by decreasing the conduction loss in a switch (I^2R_{ON})

$$R_{ON} = \frac{W_D}{q u_n N_D} \qquad (1\text{-}2)$$

$$N_D = \left(\frac{\varepsilon_S}{q}\right)\left(\frac{E_c}{W_D}\right) \qquad (1\text{-}3)$$

$$R_{ON} = \frac{4{V_{BD}}^2}{\varepsilon_S u_n E_C^3} \qquad (1\text{-}4)$$

q: Electron charge

μ_n: Electron mobility

ε_S: Specific dielectric constant

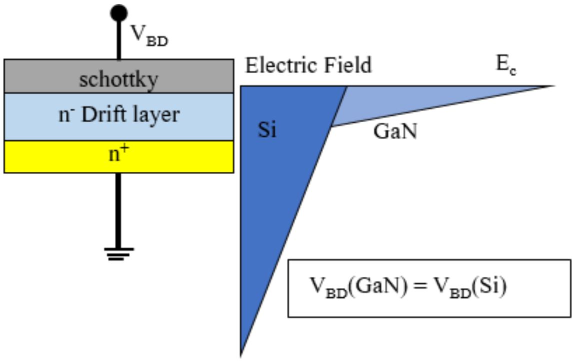


Figure 1-5: Field distribution at the breakdown for Si and wide bandgap (GaN) based Schottky diode

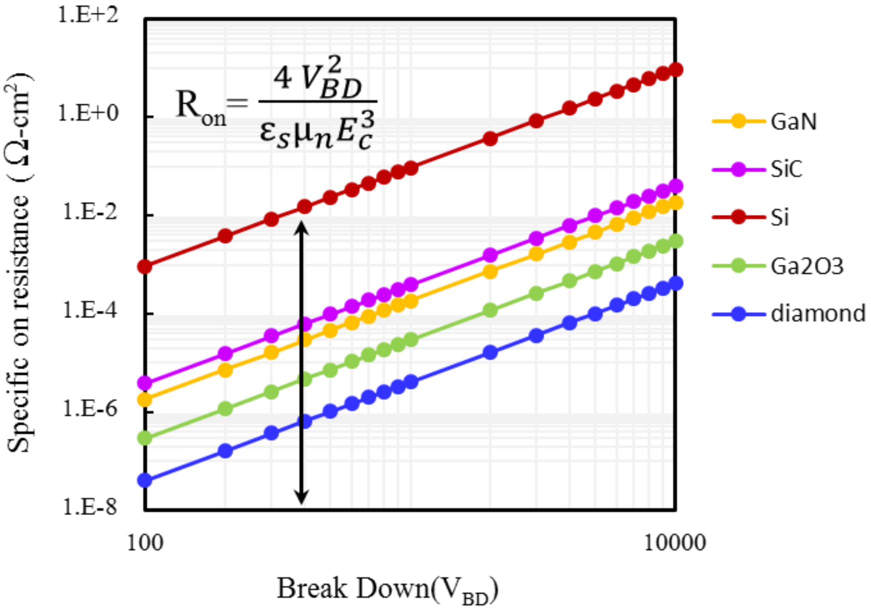


Figure 1-6: Ron Vs Breakdown voltage limit for Si, SiC, GaN, Ga2O3 and Diamond.

Thus, the characteristics of wide bandgap materials such as, high critical electric field, high-temperature stability and high saturation drift velocity equate to a low loss, requiring smaller heats sinks, reduced cooling costs, high-efficiency power conversion and theoretically make these materials a potential substitute for Si to develop high power devices. Among the SiC and GaN material systems, SiC is more matured[12-15], and SiC-based devices such as Schottky diodes, MOSFETs are commercially produced by manufacturing companies such as Rohm, Infineon, CREE, and others. GaN with a higher bandgap, and higher electron mobility than SiC, is at a nascent phase in the field of power electronics. The commercialization of GaN-based power devices is slowed down mainly due to lack of availability of GaN bulk substrates.

Typically, GaN is grown either on sapphire or SiC. When grown on SiC, the material itself is more expensive and defective than SiC. Interestingly, GaN grown on heterosubstrates with a high density of defects are widely used for LEDs development[16, 17]. In fact, GaN along with its ternary alloys based LEDs can cover a wide spectral range from green to ultraviolet. However, for power devices, these defects can drastically impair the efficiencies. Lately, GaN growth is optimized, and various techniques were instigated by different groups at universities and industries to realize bulk GaN substrates and high-quality GaN films for high power applications.

The following section describes various growth methods reported in the literature along with the advantages and disadvantages of each technique.

1.3 Growth techniques

(a) Hydride vapor phase epitaxy(HVPE)

HVPE is one of the most commonly used epitaxial growth process, in which HCl reacts with liquid Gallium to form GaCl. Subsequently GaCl along with NH_3 are carried to process chamber (typically a quartz furnace) using H_2 or N_2 or argon gas to form GaN. Figure 1-8, illustrates the HVPE growth steps. This technique results in higher growth rate compared to any other methods on the order of 200 - 300 μmh^{-1}, on relatively large (2 -in.) substrate. However, films grown using HVPE technique suffer from higher threading dislocation density (TDD) on the order of $10^9 cm^{-2}$ when grown on heterosubstrates[18]. For instance, the lattice mismatch between GaN and substrates such as Si, SiC, and sapphire are reported to be 17%,3.3%, and 13%

respectively[19]. Additionally, HVPE layers are rough and suffer from high strain resulting in bowing[20]and cracking at the GaN/Substrate interface[21].

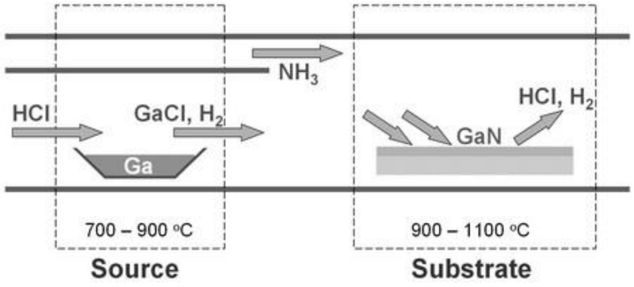


Figure 1-7: HVPE growth of GaN[22, 23]

HVPE Bulk substrates: To reduce the threading dislocations, thicker GaN films are grown on sapphire, as the threading dislocation density (TDD) is higher at the interface and the defects propagate along the direction of the growth for several microns. For the layers on the order of 350 - 500 um thick, the number of defect lines that extend to the surface tends to decrease. Further, GaN layers are peeled off from substrates resulting in a bulk substrate lower TDD values of 10^6cm^{-2}[24]. But, even after the separation of the freestanding GaN layer from heterosubstrates, GaN wafers are typically bowed.

(b) Metal organic chemical vapor deposition (MOCVD)

After HVPE, MOCVD is the most widely implemented method to grow high-quality GaN films on heterosubstrates. MOCVD is a two-step process, involving in (i) transportation of metalorganic and nitrogen precursors to the process chamber and then (ii) reaction on the surface of the heated substrate. Trimethylgallium (TMGa) and NH$_3$ are typically used sources for Ga, and N. TMGa is initially vaporized by flowing hydrogen gas through the bubbler and is then mixed with NH3 in the main channel. The two precursors are then flowed in parallel into the chamber, to decompose and form GaN on the heated substrate. Also, a secondary gas is flowed perpendicular to the substrate to maintain the reactants closer to the substrate (shown in figure 1-9). Further, using a low temperature grown buffer layer[25], the films produced by MOCVD have resulted in substantially lower TDD on the order of 10^5 cm^{-2} even when grown on heterosubstrates.

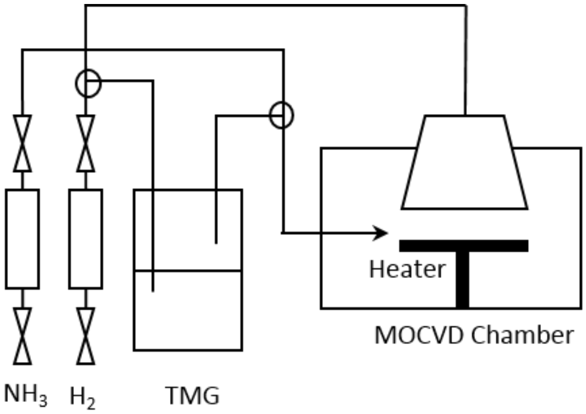


Figure 1-8: MOCVD reactor set up for GaN growth

Although the MOCVD technique can produce high-quality films[26], the growth rate of this method is very low on the order of 1-2 μm/h only.

(c) Ammono thermal

Both the growth techniques discussed above completely rely on heterosubstrates such as silicon carbide and sapphire due to lack of freestanding and high-quality GaN substrates. Due to the thermodynamic limitation of GaN, e.g., decomposition at 877^{0}C under atmospheric conditions

[27] , it cannot be grown from the stoichiometric melt without extreme pressure and temperature of > 6 GPa at 2220^{0}C[28]. Hence, only vapor phase and solution techniques are appropriate to produce group-III nitride crystals in an economic way. More recently, however, the ammonothermal growth of GaN has emerged as a powerful technique for the mass-production of large size GaN crystals [29].

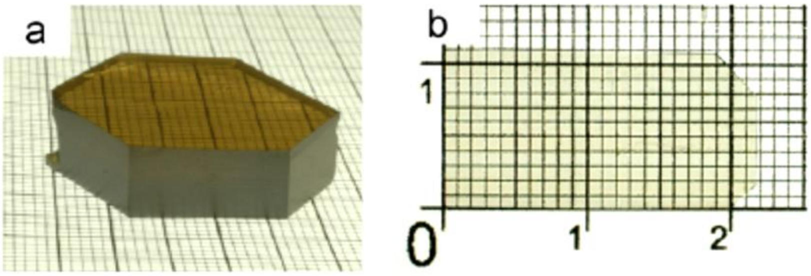


Figure 1-9: GaN bulk crystals obtained by Ammono thermal method [30]

The ammonothermal technique belongs to the wide family of solvothermal techniques, employing a polar solvent of inorganic or organic nature under subcritical or even supercritical conditions to dissolve and re-crystallize a polar material. The process to grow GaN crystals uses a solvent comprised of supercritical ammonia with added mineralizers to grow GaN via recrystallization at seed crystals[31]. Ammonothermal growth is a bulk process that does not use non-native starting substrates. This method has yielded the lowest defect density of 5x10^3 cm^{-2} in a 1-in. wafer. Following table summarizes all the growth techniques

Growth Technique	Advantages	Disadvantages
Hydride Vapor Phase epitaxy (HVPE)	High growth rate (200 – 300 μmh^{-1})	High defect density (10^9 cm^{-2})
Metal organic chemical vapor deposition (MOCVD)	Low defect densities (10^5 cm^{-2})	Low growth rate (1- 2 μmh^{-1})
Bulk Hydride Vapor Phase epitaxy	High growth rate (200 – 300 μmh^{-1})	Cracking at the interface and bowing of the wafer
Ammono thermal	Low defect density ($5x10^3$ cm^{-2})	Long growth time

Table 1-2: Summary of GaN growth techniques

1.4 Motivation

The recent development in the bulk substrate technology has boosted the prospects of GaN devices into power arena, beyond the Light industry. Particularly, the expanding automotive industry and the rising prominence of electric vehicles in the global automotive sector is a crucial driver for the GaN power devices market in the coming years[32]. According to US Energy information administration, a rise of 6 and 4% in battery electric and plug in hybrid vehicle sales is predicted in next 20 years.

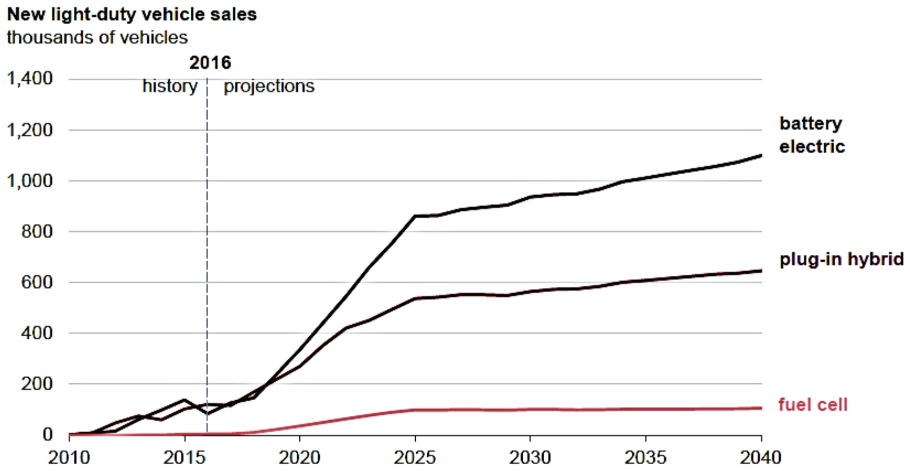


Figure 1-10:Light-duty vehicle sales from 2010 to 2040 (source: US Energy Information Administration)

To understand the role of GaN in battery electric vehicles better, take the example of an electric car. Figure 1-12(a) shows the simple block diagram comprising of various units such as HV battery, boost converter, inverter, electric motor, accessory load DC-DC converter and electric accessory load. Consider the case of high voltage battery connected to a boost converter followed by inverter and then connected to electric motor that generates the torque to drive the vehicle as shown in figure 1-12(b). A battery provides a DC voltage in the range of 200V to 400V, whereas the electric motor needs much higher AC voltages to generate magnetic fields, to run the motor. Therefore, the voltage from the battery is typically fed to a boost converter that steps up the voltage to 650V from 200V and is then fed to an inverter circuit that converts DC to AC as required by the load (electric motor).

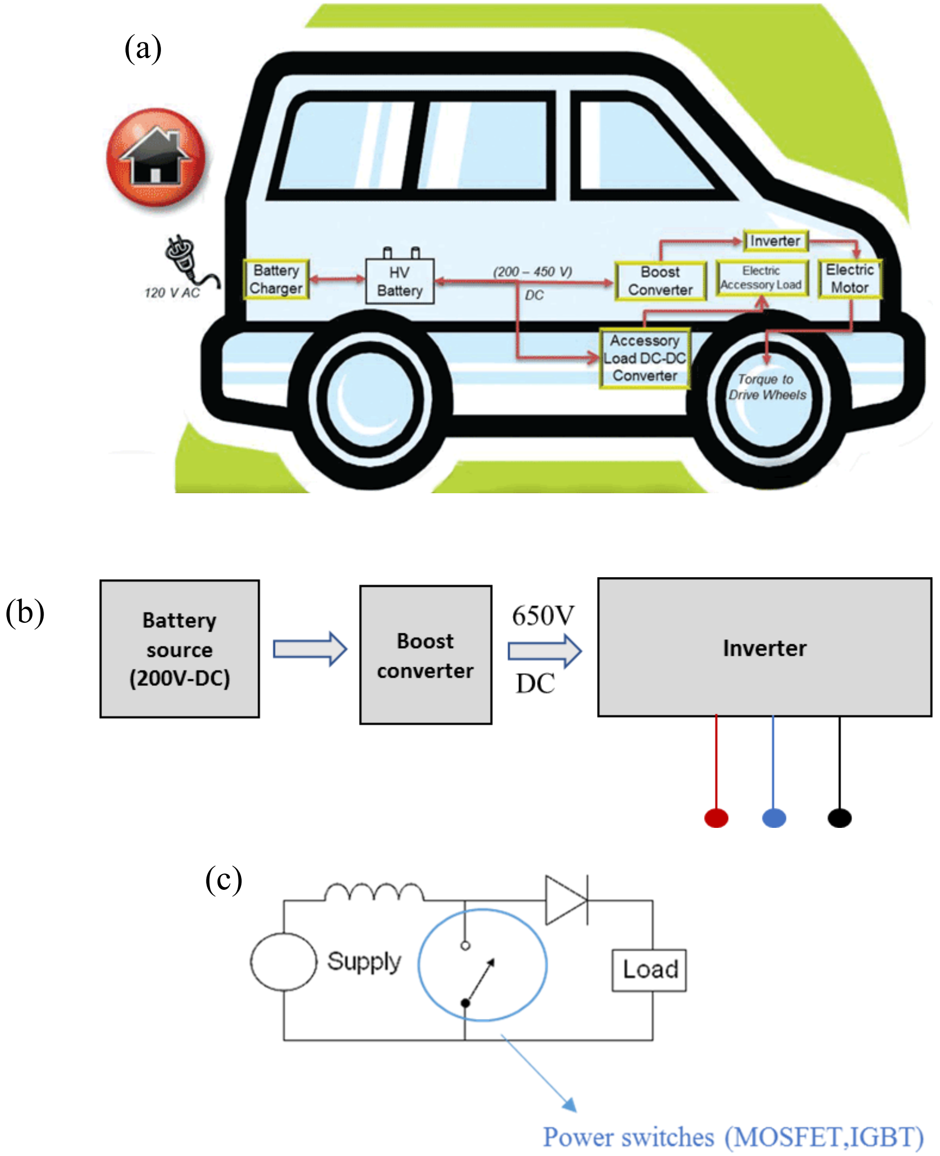


Figure 1-11:(a) Block diagram of an electric car (b) simplified representation of driver circuit (c) boost converter circuit

Fundamentally, booster converter or inverter blocks are made up of several power switches such as insulated gate bipolar junction transistors(IGBT), MOSFETS and passive components such as capacitors and inductors. Figure 1-12(c) shows the electric circuit for a boost converter.

Conventional Si switches as discussed earlier in this chapter can operate at temperatures $\leq 150^0$C. However, booster and inverter are located near the electric motor, where temperature typically rise up to 300^0C, therefore Si switches need additional heat sinks which make overall system bulkier and adding extra load on motor. There by affecting efficiency of electric motor. Also, as discussed before, Si based devices because of high on-resistance and lower switching speeds decrease the overall power conversion efficiency. Therefore, automotive industry is showing interest in wide bandgap material systems such as SiC and GaN to replace Si based switches in medium operating power ranges (400V-2000V).

Though, there are good prospects for development of GaN-based devices for the automotive industry, high substrate cost, smaller GaN substrate sizes (2" wafers) and yield-related issues are restraining the expansion of GaN power device market. Thus, leaving scope for developing low-cost material systems and novel device designs that can endure in the medium power regime efficiently. Till date, several groups have reported various GaN-based diodes and transistors (will be discussed in the next chapter) with breakdown voltage ranging from 100's to several 1000's. However, most of them seem to have performance lower than the theoretical maximum due to various factors such as quality of the GaN films, device design[33], fabrication process and others[34].

We particularly got motivated to develop novel device designs that can operate in the medium power regime (400V – 2000V). So, we have started off with two terminal Schottky diodes since we are developing GaN-based power devices for the first time.

1.5 Outline

In chapter 2, the basic principle of the metal-semiconductor contact is discussed. Followed by a complete background on various types Schottky diodes reported till date is presented. The impact of the factors such as a quality of the drift layers and device geometry on the diode performance are also discussed.

In Chapter 3, our new wraparound field plate architecture is presented to address the field crowding-related issues more efficiently than the conventional geometries. The impact of each geometrical aspect on the wraparound diode is studied, and an optimized structure with the breakdown voltage suitable for automotive applications in the range of 400V to 1600V is developed. The field distribution in various diodes including an ideal diode, a diode with finite Schottky contact length and a standard field plate at breakdown are simulated and compared to wraparound.

Chapter 4 discusses the fabrication and electrical characterization of lateral diodes built from HVPE grown films on sapphire. A standard field plate and a wraparound field plate are tested and compared to simulation results. The impact of surface defects and bulk defects on the diode breakdown voltage are studied. Also, the effect of surface passivation using ammonium sulfide is described.

In chapter 5, vertical diodes built on low defective films grown using MOCVD on Ammono bulk substrate are discussed. Issues related to etch induced defects, parasitic currents across the GaN and dielectric interface that were encountered in lateral diodes are studied systematically by electrical characterization of the diode after each fabrication step. Also, an optimized dry etch process is developed to minimize the surface currents. Further, a bilayer dielectric structure is employed to overcome the issues introduced by PECVD deposited dielectric film.

Chapter 6 and 7 summarizes the challenges in the device fabrication and discusses the future directions in terms of material growth and fabrication processes to realize diodes with higher efficiencies.

CHAPTER 2 LITERATURE REVIEW AND BACKGROUND

2.1 Introduction

A Schottky rectifier is formed by making an electrically nonlinear contact between a metal and a semiconductor. The Schottky rectifier is a unipolar device attractive for power applications due to its relatively low on-resistance and fast switching speed. Si-based Schottky diodes have been used extensively in power supply circuits with low operating voltages. However, for automotive applications, devices with higher operating temperatures, voltages > 400V and higher switching speeds are required. In the case of Si, commercial Si Schottky diodes can operate at voltages <100V and the novel device geometry that uses charge-coupling[35] have improved the breakdown values up to 200V only. As discussed in chapter 1, GaN because of its higher critical electric field will result in lower on-resistance and can simultaneously operate at voltages >400 V.

In this chapter, the basic structure of Schottky diode is introduced. Then a discussion of the principle of the metal-semiconductor junction is provided, followed by a state of the art review of various Schottky diodes reported in the literature to date.

2.2 Schottky Rectifier

Nonlinear current flow across a metal-semiconductor contact has been known for a long time. Walter Schottky in 1938, explained the way specific combination of metals and semiconductors can rectify current.

A Schottky diode junction is formed by depositing a metal with high work function (typically by evaporation or sputtering under vacuum) onto a wafer that has been doped either n-type or p-type. In the case of GaN due to the presence of background impurities, GaN intrinsically acts like n-doped material. Figure 2-1 illustrates the energy bandgap of metal and an n-type semiconductor.

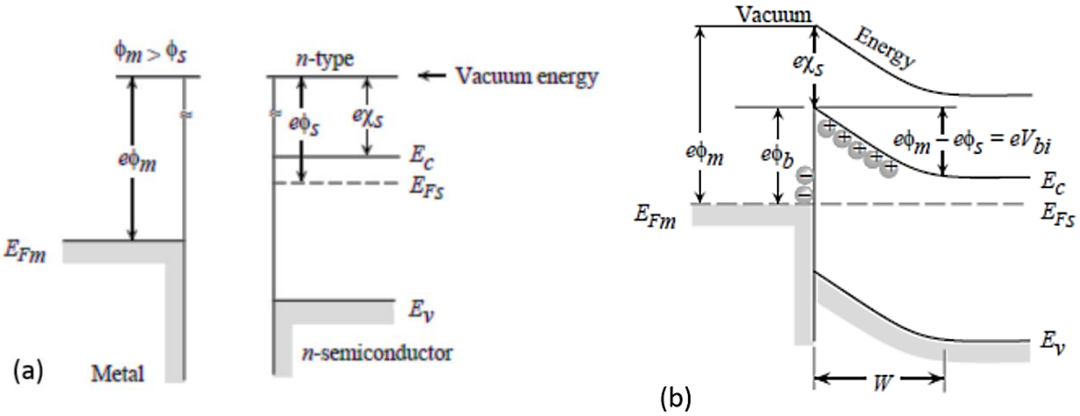


Figure 2-1: Energy band diagram for a metal and semiconductor (a) in isolation (b) after making and electrical connection [96]

When metal is brought into contact with an n-type semiconductor, electrons diffuse into the metal until thermal equilibrium is established. This transfer of electrons leaves positive charges within a depletion region as shown in the figure 2-1. The depletion region formed at the surface of the semiconductor supports the entire contact potential. The internal voltage difference between metal and semiconductor is referred as the built-in potential(V_{bi}).

The Schottky barrier height (φ_B) is related to built-in potential by

$$\varphi_B = qV_{bi} + (E_C - E_{FS}) \qquad (2\text{-}1)$$

$$\varphi_B = \varphi_M - X_S \qquad (2\text{-}2)$$

φ_M : work function of metal
X_S: electron affinity of semiconductor

The built-in potential creates a zero-bias depletion region within the semiconductor, whose width is given by Eq 2-3

$$W_0 = \sqrt{\frac{2\varepsilon_S V_{bi}}{qN_D}} \qquad (2\text{-}3)$$

2.2.1 Forward Conduction

When a positive voltage is applied to the metal, the depletion width decreases, the built-in potential reduces, and current flows across the junction by transport of electrons from the semiconductor to the metal over the barrier. This current is referred to as thermionic emission current [36], and these thermionic emission currents are the most dominant mode of current flow in the Schottky power diodes.

Unlike, p-n junction diodes, the injection of minority carriers is negligible. In a power Schottky rectifiers, the barrier height is intentionally reduced to lower the on-voltage drop making the minority carrier current small. Therefore, if the forward voltage is removed, the current stops within a few picoseconds and reverse voltage can be established. Thus, there is no delay effect due to charge storage as in p-n junction diodes.

Also, in a power rectifier the doping concentration is relatively low to block the high reverse voltage. This spreads the depletion region over a substantial distance. Consequently, the potential barrier is not sharp enough to allow significant current via tunneling.

The thermionic emission current flow across the Schottky barrier interface is given by Eq 2-4

$$J = AT^2 e^{-(q\varphi_{BN}/kT)}\ [e^{(qV/kT)} - 1] \qquad (2\text{-}4)$$

Where A is the effective Richardson's constant, T is the absolute temperature, k is the Boltzmann's constant, and V is the applied bias. The Richardson's constant value for GaN in the literature spans from 3.23 x 10^{-5} to 26 $\mathrm{Acm^{-2}K^{-2}}$[37-39]. Hacke et al. suggested that this variation in A values was caused by the presence of a barrier through which the electron must tunnel[40]. Guo et al. suggested that the decrease of the effective contact area may also cause the low value of A*[41].

When a forward bias is applied across the two terminals, the first term in the square brackets of the equation becomes more dominant, resulting in forward current density given by

$$J_F = \mathrm{AT^2 e^{-(q\varphi_{BN}/kT)}\ e^{(qV_{FS}/kT)}} \qquad (2\text{-}5)$$

Where V_{FS} is the voltage drop across the Schottky contact. In the case of power Schottky rectifiers, to support high reverse blocking voltages, lightly doped drift regions are used. As a result, there is an additional voltage drop across the drift layer (V_R), which increases the voltage drop across Schottky contact further. The on-state voltage drop (V_F) for a power Schottky rectifier, after including the resistive voltage drops, is given by

$$V_F = V_{FS} + V_R \qquad (2\text{-}6)$$

$$V_F = \frac{kT}{q}\ln\left[\frac{J_F}{J_S}\right] + R_{S,SP}J_F \qquad (2\text{-}7)$$

$$J_S = AT^2 e^{-(q\varphi_{BN}/kT)} \qquad (2\text{-}8)$$

J_F : Forward current density
J_S: Saturation current dnsity
$R_{S,SP}$: Total series specific resistance

The total series specific resistance ($R_{S,\,SP}$) is determined by the diode structure, and is discussed in detail in section 2.3

2.2.2 Reverse blocking

When a reverse bias is applied, the depletion region extends into the lightly doped semiconductor. The voltage is supported across the drift region with the maximum electric field located at the metal semiconductor junction. The Poisson's equation for the n- region is then given by

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_s} = \frac{qN_D}{\varepsilon_s} \qquad (2\text{-}9)$$

Where Q(x) is charge within depletion region due to the ionized donors, ε_s is dielectric constant for the semiconductor and N_D is the donor concentration of the drift region. Integrating Eq 2-9 provides the electric field distribution

$$E(x) = \frac{qN_D}{\varepsilon_s}(W_D - x)$$

The maximum electric field is at the interface i.e., x=0

$$E_M = \frac{qN_D}{\varepsilon_s}(W_D) \qquad (2\text{-}10)$$

$$W_D = \sqrt{\frac{2\varepsilon_S V_a}{qN_D}} \qquad (2\text{-}11)$$

$$E_M = \sqrt{\frac{2qN_D V_a}{\varepsilon_S}} \qquad (2\text{-}12)$$

When the applied voltage increases, the maximum electric field increases, resulting in the acceleration of carriers at higher velocities. With further increase in electric field, carriers gain sufficient kinetic energy so that their interaction with lattice generates more charge carriers. These charge carriers further gain momentum from the high electric field in the drift region and will further multiply the charge carriers through impact ionization. Consequently, impact ionization results in high current flow leading to avalanche breakdown of the diode. The maximum electric field before which the diode undergoes breakdown is referred to as critical electric field of the semiconductor. From Eq 2-12, it is evident that the breakdown voltage is inversely related to doping concentration. Therefore, drift regions are preferred with lower doping concentration to sustain higher voltages in the reverse bias. Figure 2-2 illustrates the relationship between doping concentration and the breakdown voltage in GaN.

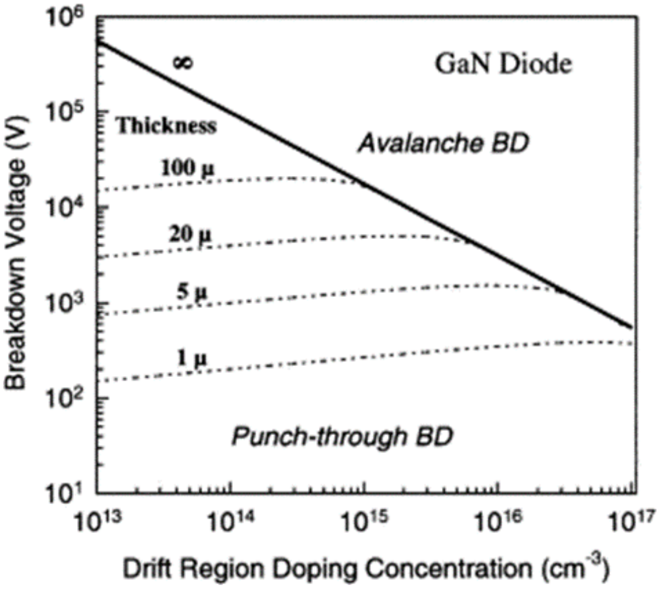


Figure 2-2: Break down Vs. drift region doping concentration of GaN [11]

However, in forward bias lower doping results in higher on-resistance which is not desirable. As increased on-resistance leads to increase in conduction losses. Therefore, there is a tradeoff between on-resistance and breakdown voltage of a diode.

2.3 Material systems

Schottky diodes primarily can be classified into vertical and lateral geometry depending on the type of the substrate.

2.3.1 Vertical diodes

Vertical diodes are comprised of a lightly doped drift layer grown on a highly conducting GaN bulk substrate. A Schottky rectifier formed at metal and epilayer interface and an ohmic contact is formed on the back side of the conducting substrate. So, current flows through the epilayer, buffer, and substrate as shown in figure 2-3. Thus, there is additional potential drop across the drift layer (I*Repi), bulk substrate (I*Rsub) and ohmic contact(I*Rc). The resistance contributed by the substrate must be included in analysis because it can be comparable with that of the drift region [42]. Resistance due to the epilayer depends on the width, mobility and doping concentration. Resistance due to the substrate depends on the thickness and resistivity of the bulk substrate as shown in below Eq 2-14 & 2-15.

$$\mathrm{R_{ON}} = \mathrm{R_{epi}} + \mathrm{R_{sub}} + \mathrm{R_C} \qquad (2\text{-}13)$$

$$\mathrm{R_{epi}} = \frac{\mathrm{W_d}}{\mathrm{qu_nN_d}} = \frac{4\,\mathrm{V_{BD}^2}}{\varepsilon_S \mu_n \mathrm{E_C^3}} \qquad (2\text{-}14)$$

$$\mathrm{R_{sub}} = \rho_{\mathrm{sub}} * \mathrm{d} \qquad (2\text{-}15)$$

To block higher voltages across the drift layer, vertical geometry is preferred over the lateral due to less scattering of electrons and absence of leakage currents at the epilayer and substrate interface. These factors are discussed in detail in the following section. The most common vertical device uses an unintentionally doped epilayers are grown using MOVPE or MOCVD[43] on a free-standing bulk HVPE substrate [44]. Both the MOCVD and MOVPE growth techniques result in high background impurity concentrations of carbon(c), oxygen (O) and hydrogen (H). These impurities occupy Ga site and form shallow donor states near the band edge resulting in increase in the leakage currents across the junction in the reverse bias. To reduce the background impurities, recently HVPE has been used to grow the epilayer on HVPE bulk substrates. However, these diodes have inferior breakdown values compared to films grown by MOCVD or MOVPE[45].

2.3.2 Lateral diodes

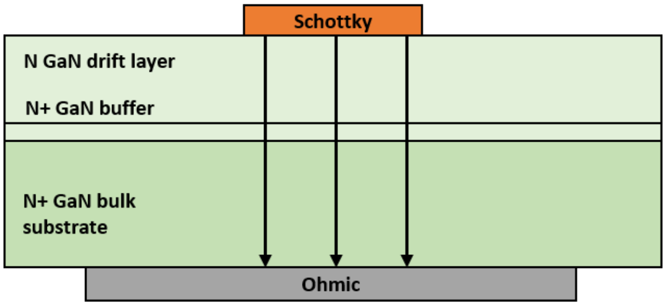
In lateral devices epilayers are grown on heterosubstrates such as Si or sapphire due to the lack of GaN bulk substrates. Usually, epilayers grown on heterosubstrates suffer a high-density threading dislocation originating at the interface due to mismatch in the lattice parameters. These threading defects propagate along the growth direction, and some reach the surface. Eventually, with the development of a two-step growth technique that uses a low-temperature buffer prior to the growth of epilayer have improved the quality of epilayer grown on heterosubstrates. In the two step growth, initially buffer film consists of disordered hexagonal islands[46] is grown. Then, the temperature is ramped up to anneal the buffer layer and then to grow the epilayer which decreases defect densities.

The diodes built on these epilayers grown on heterosubstrates have both ohmic and Schottky contact on the top surface of the epilayer. Thus, the current flow is within the drift layer, unlike vertical diode as illustrated in figure 2-3. In forward bias, since the current is no longer flowing through the substrate, the only factors contributing to forward resistance are the epilayer resistance and the contact resistance. Since the substrate resistance is absent in lateral diodes, the on-resistance is expected to be lower than in the vertical devices. However, it was observed that threading defects that propagate along the growth direction are normal to the current flow (blue lines in figure 2-3), trap the free flow of electrons laterally. Also, these defects are reported to scatter the electrons and thereby increase the on-resistance.

$$R_{ON} = R_{epi} + R_C \qquad (2\text{-}16)$$

$$R_{epi} = \frac{W_d}{qu_nN_d} = \frac{4\,V_{BD}^2}{\varepsilon_S \mu_n E_C^3} \qquad (2\text{-}17)$$

Lateral diodes do not show consistent properties due to the presence of a high number defects that are randomly distributed across the film. Also, these diodes are limited to lower voltage applications. Especially, when GaN layers are grown on conducting substrates such as Si, with the increase in bias voltage, the depletion width extends deeper into the epilayer, reaching the GaN and buffer interface. Since silicon is conducting, when the space charge region reaches the silicon interface, it causes additional conduction along the interface.



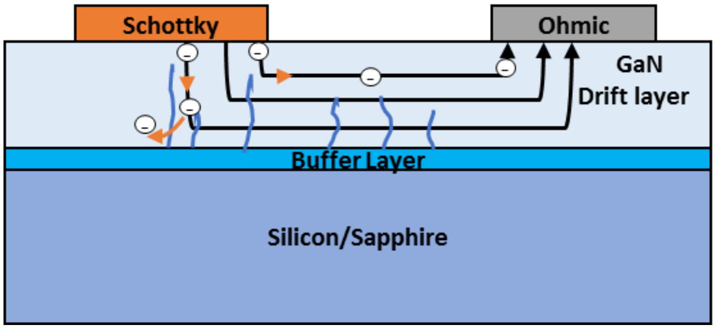


Figure 2-3: Current flow in vertical device and in lateral device

2.4 Literature review

In this section, various kinds of Schottky diodes reported in the literature from 1999 to present are discussed. As mentioned earlier, for a Schottky diode the two critical parameters to evaluate the performance are the on-resistance in the forward bias and the breakdown voltage in the reverse bias. For the following diodes, these two values are presented. Also, the factors such a drift layer thickness, donor concentration, defect densities that affect the diode characteristics are also summarized.

As stated before due to lack of a bulk substrates, diodes initially used drift layers grown on heterosubstrates. Bandic et al., used 8-10 um thick hydride vapor phase epitaxy grown GaN on a sapphire substrate to fabricate a Schottky rectifier. A cross-sectional transmission electron microscopy (XTEM) study of their HVPE films showed that the region adjoining the interface was highly disordered and included several subgrain boundaries, stacking faults and prismatic plane fault. The electron concentrations and mobilities at the thin interface and at the top surface layer were $2x10^{20}$ cm^{-3} and 35 cm^2/Vs, and $2x10^{16}$ cm^{-3} and 265 cm^2/Vs, respectively. These values correspond to conductivities of 1120 and 0.85 S cm-1 for the interface layer and the surface layer, indicating that the interface layer is approximately three times more conductive. The authors tested lateral geometries with standard circular contacts, diodes with field plate overlapping a SiO2 layer, and quasi-vertical diodes with mesa structure as shown in figure 2-4. The field plate diodes showed the highest breakdown values between 250-450V, with an on-state voltage of 5V. The high on voltages were attributed to low carrier concentration on the surface layers. On the other hand, mesa devices formed by etching away the top 5 um film have resulted in on-voltage of 4.2V at the expense of higher leakage currents due to highly conducting layers near the interface. The best devices were reported to have a current density of 100 A/cm2 at voltage of 4.2 V at a and a saturation current density of 10^{-5} A/cm2 at a reverse bias of 100 V[47].

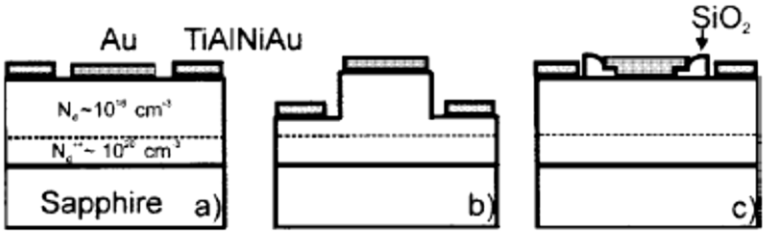


Figure 2-4: Schematic of GaN Schottky rectifier built from HVPE grown layers on sapphire. (a) lateral diode (b) mesa diode (c) lateral diode with a field plate extending over SiO2[47]

Dang et al., used films grown by MOCVD on c-plane sapphire to fabricate Schottky diodes. Two types of MOCVD films (i) 11 µm unintentionally doped GaN was grown using 1 µm n+ doped GaN as a buffer (ii) and a 3 µm thick highly resistive layer was grown using 300A^0 novel buffer. The carrier concentration of a 11µm and 3 µm epilayers were $2x10^{16}$ and $\leq 10^{15}$ respectively. The low carrier concentration in 3um layers was attributed to a novel buffer. Mesa devices were built using 11um layers by etching the GaN layer with the ohmic contacts deposited on the n+ layer and Schottky contacts on top of the mesa. A standard circular ohmic and Schottky contacts are made on 3um GaN without any etching. A breakdown value of 550V and 2000V were reported using 11um (nominal buffer) and 3um (modified buffer). The on-resistance of the mesa devices was three orders lower than the planar diodes. Authors also tested the diodes made on films grown by HVPE and MBE techniques and obtained the highest breakdown of 200V and 80V as listed in table 2-1.

Method	**Thickness(μm)**	**Doping(cm^{-3})**	**V_{BD}(V)**
HVPE	60-100	$2x10^{17}$	60-200
MBE	2-5	$5x10^{16}$	60-80
MOCVD(nominal)	5-12	$2x10^{16}$	350-550
MOCVD(modified)	3	$\leq 10^{15}$	2000

Table 2-1: Drift layer thickness, doping concentration and breakdown voltages of the diodes built on films grown by HVPE, MBE, MOCVD (nominal buffer) and MOCVD (modified buffer)[48]

Later, with the development of HVPE bulk substrates, Johnson et al., used HVPE bulk substrates that are separated from sapphire using laser beam heating. Then an unintentionally doped GaN layer with about 6μm thickness were deposited using MOCVD. Schottky diodes built from these layers with carrier concentration of $5x10^{16}$ cm^{-3} were reported to have a breakdown of 450V and on-resistance value of 20 mΩ.cm^2 [49].

K.Ip et al., reported Schottky diodes built on bulk HVPE crystals with a standard field and damage implants as shown in figure 2-5 and compared to simulated values. A 75um diameter diode displayed a breakdown voltage of 120V while the simulations predicted a higher breakdown of 600V. The disparity between the theoretical and experimental values was ascribed to crystal defects such as micropipes and dislocations that initiate carrier multiplication resulting in the premature failure of the diode.

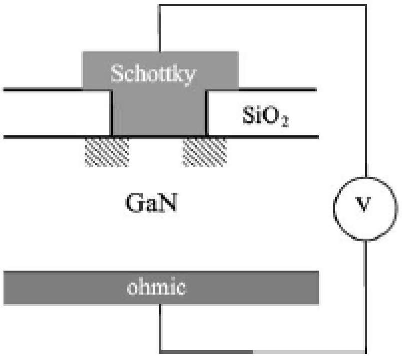


Figure 2-5: Schematic of Schottky rectifier fabricated on free-standing GaN with field termination [50]

Zou et al. used 10 mm x 10 mm HVPE bulk substrates of 450μm thickness without epitaxial layers provided by Kyma Technologies, with a doping level of $7x10^{15}$ cm^{-3} and a defect density of 10^6 cm^{-2}. Pt Schottky diodes with different diameters (50um, 150u, 300um), without field termination, were built and tested. An average breakdown value of 630V, 600V and 220V were reported for 50um,150um, and 300um diodes. Also, the 50um diode offered a low on resistance of 2.2 mΩ-cm^{-2}.

Hashimoto et al. compared the quality of films grown using MOVPE on a low defective HVPE bulk substrate (10^6 cm^{-2}) and a sapphire substrate with a GaN buffer. Both the films were grown under similar conditions. However, films grown on a sapphire substrate using buffer layers were rough with the several pits on the surface. Also, they have higher C, O and H impurities and higher defects. Authors speculated higher background impurities due to accumulation of impurities on the surface of the defect pits. Figure 2-6 shows the dependence of the impurity concentration on the defect density

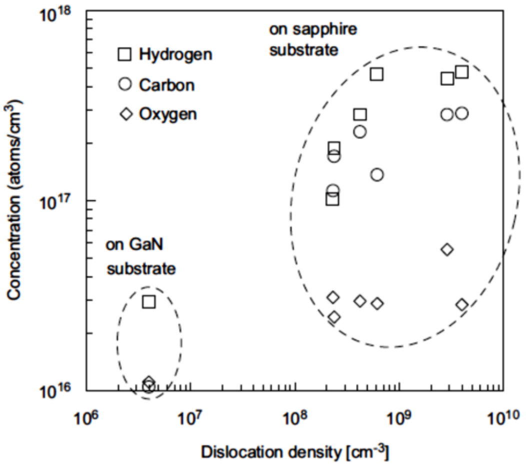


Figure 2-6: Dependence of impurity concentration on the defect density[51]

Schottky barrier diodes built on bulk substrate were reported to have the breakdown voltage of 580V and on-resistance of 1.3 m**Ω**-cm^{-2}. The lateral diodes built on sapphire showed higher leakage currents and a lower breakdown voltage of 163V. The on-resistance values were much higher on the order of 14.4 mOhms-cm^{-2} in lateral diodes and was associated to the poor quality of the drift layer even after using a buffer layer.

Lu et al. developed a vertical GaN Schottky rectifier on a freestanding bulk GaN substrate by employing homoepitaxial growth technique. The *n*− /*n*+ epilayers were grown on a HVPE bulk GaN substrate by metal-organic chemical vapor deposition. The dislocation density of the epitaxial layer determined by cathodoluminescence mapping technique was 6x10^{6} cm^{-2}.

The surface roughness was reported to be less than 1 nm. The SIMS data showed Si carrier concentration of $6x10^{16}$ cm^{-3} in the drift layers. The Schottky rectifiers used standard field termination as shown in figure 2-7. Low leakage current of $3x10^{-8}$A at −100 V was recorded due to low dislocation density in the epilayer. The reverse breakdown voltage for these diodes was defined at the reverse current level of 0.1 A/cm2, and the breakdown values down values were distributed between 260 to 430 V[52].

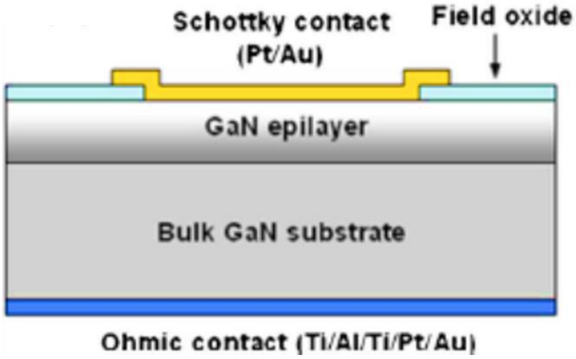


Figure 2-7: Schematic of vertical Schottky rectifier fabricated on bulk GaN substrate[52]

Saitoh et al. reported diodes with efficiency closest to ideal values for the first time in 2010. HVPE produced GaN substrates were used to build Schottky rectifiers with threading dislocation densities < $1x\ 10^6$ cm^{-2} and have exhibited n-type conductivity with resistivity value as low as .01 Ωcm. A 5 μm epitaxial layer was deposited on top of the bulk substrate using MOCVD[53] with Si concentration of $8x10^{15}$ cm^{-3} . 1 μm thick PECVD deposited SiN_X was used as the dielectric layer, and the field plate structure was formed by Schottky contact overlapped with dielectric as illustrated in the figure 2-8. The breakdown voltage and the specific on-resistance of these Schottky barrier diodes were 1100V and 0.71 mΩ.cm^2 and respectively.

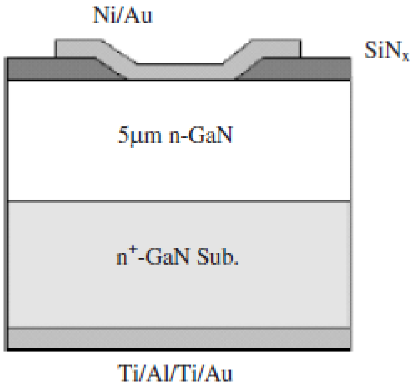


Figure 2-8: Schottky rectifier structure with the field plate reported by Saitoh et al.[53]

The electron mobility in these drift layer was reported to be 930cm^{2}V^{-1}s^{-1}, which is close to theoretically predicted value[54]. There were several other groups, who also used MOCVD to deposit the epitaxial layer. However, the mobility values reported by Saitoh are the optimum by far.

J.Suda et al., have tested 3 different bulk HVPE samples without a field termination and an epilayer. Doping of the substrates varied from 10^{16} to $2x10^{17}$ cm^{-3} and the dislocation densities were estimated to be 2-3 x 10^6 cm^{-2}. They reported an increase in leakage currents with the increased doping concentration as illustrated in the figure 2-6.

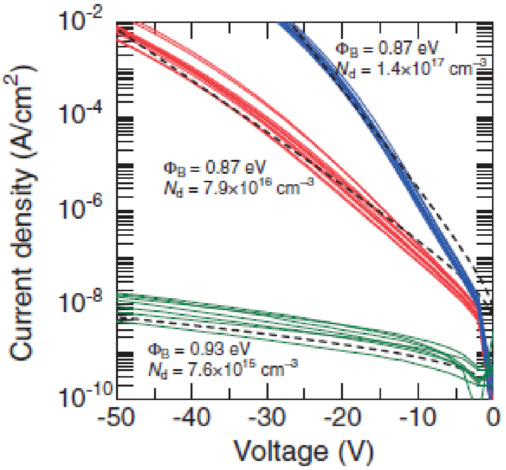


Figure 2-9: Reverse I-V characteristics of GaN Schottky barrier diodes with different donor concentration of 7.6 x 10^{15}, 7.9 x 10^{16} and 1.4 x 10^{17} cm^{-3} [55]

Obzek et al., implemented argon implantation at the contact edge to passivate the high electric fields at the contact periphery. Diodes fabricated on n-type doped layers (10^{14} cm^{-3}) grown by MOCVD on a bulk substrate have resulted in a breakdown voltage of 300V. With the edge termination, the breakdown value increased to1650V[56]. Compared to field plate architecture reported by Saitoh, diode with argon implantation have a higher breakdown, but the leakage currents are almost 3-4 orders higher.

There were several other diodes reported in the literature that used bulk HVPE. The growth conditions were varied, and different doping concentration were produced and tested [42, 57]. The break down showed a dependence on the carrier concentration, with the samples having low doping exhibiting a higher breakdown and the on-resistance values also showed dependence on doping concentration and the thickness of the bulk substrate.

The on-resistance vs. breakdown values for all the diodes that were discussed in this section are plotted in the figure 2-7. The green squares correspond to the diodes that are built either on bulk HVPE substrate or epilayers grown on HVPE substrate, and the orange squares represent diodes that used epilayers grown on heterosubstrates such as Si or sapphire. Solid blue yellow, dotted blue and red lines correspond to Si, GaN, Ga2O3, and diamond materials theoretical limit. Most of the didoes have on-resistance and the breakdown values higher than the standard Si, however they are still far below the GaN theoretical limit.

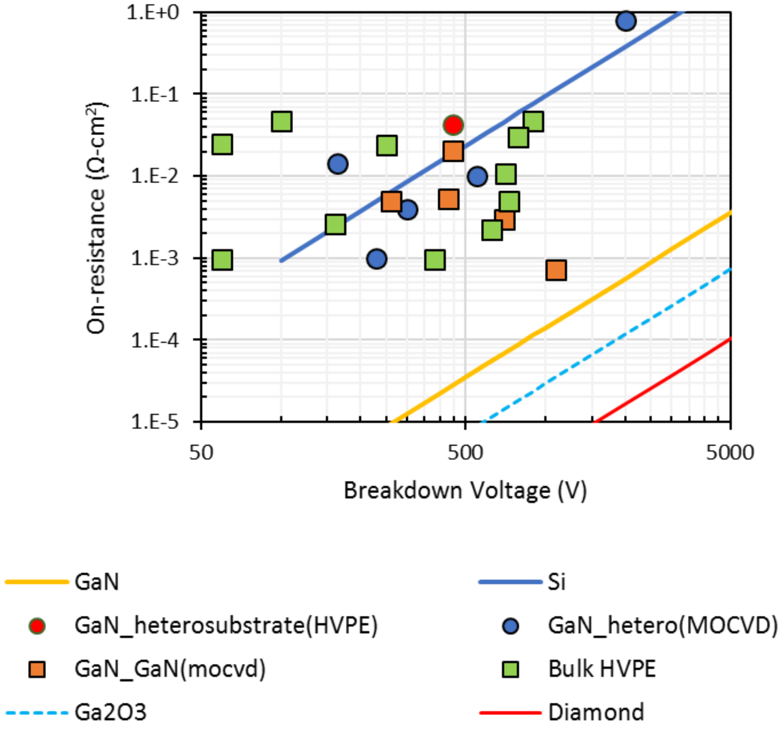


Figure 2-10: On resistance Vs. Breakdown voltages for Schottky rectifiers reported in the literature.

Some Schottky diodes in the literature have used an alloy of GaN with Al to produce AlGaN. The bandgap can then be tuned depending on the Al composition from 3.4 eV to 6.4 eV.

Similar to the GaAs/AlGaAs system, GaN/ AlGaN confines the electrons in 2-dimensional electron gas(DEG), and the mobility of the carriers is predicted to be as high as 2000Vcm-1s-1. AlGaN/GaN is predominantly used for high electron mobility transistors (HEMTs) due to its superior carrier mobility. However, Mignda et al. have used AlGaN/GaN grown on Si to build a Schottky diode, and have used multiple field plate structure for uniform field distribution at the contact edges. This device design has exhibited a breakdown voltage of 1900V with an on resistance of 5.12 mΩ-cm^2. Since this work is more focused on GaN diodes, GaN/AlGaN is not discussed in detail here. Moving to back to GaN material systems.

Among the various growth techniques that were discussed so far, HVPE has evolved so much in the last decade, that its free-standing bulk substrate use in power devices have become ubiquitous. Also, these substrates are grown commercially by vendors such as Kyma, Agnitron, Structured materials and others. However, field crowding at the edge of the contact and the high background impurity concentration in drift regions that are typically deposited by MOCVD or MOVPE are critical issues that are yet to be addressed to utilize the GaN to its fullest potential.

2.5 Field crowding

In an ideal diode structure, electric field is uniformly distributed along the lateral direction, and there are no fringing field issues. However, for a real diode with finite size Schottky and ohmic contacts, the electric field is non-uniform which leads to early device breakdown. The non-uniform electric field is concentrated at the Schottky contact edges. The goal of edge termination techniques is to achieve an electric field distribution as close to the ideal case as possible. A number of edge modification techniques have been used in the literature, such as field plates[53], damage implants[56], guard rings[33], and different combinations of these strategies[58-60], as shown in figure 2-11. In a field plate structure, the Schottky contact extends over the dielectric. This extended contact acts like a freestanding metal-insulator-semiconductor (MIS) electrode and distributes the field away from the contact periphery along the epitaxial layer surface. Damage implant techniques use high dose ion implantation to create defects located near the mid-band gap of GaN. These implants create a high resistive layer at the diode edge and promote the spreading of potential along the surface, resulting in reduced edge electric field. Guard ring techniques, like damage implants, use p-type implants instead of damage implants to deflect the field along floating p-n junctions.

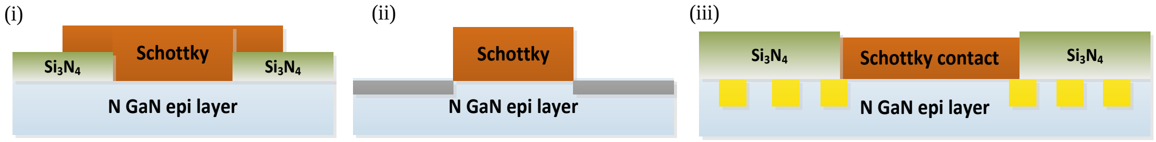


Figure 2-11: Common field termination techniques (i) field plate design (ii) damage implant(iii) guard-ring using p implants

In all edge techniques overviewed thus far, the breakdown is still below the expected ideal diode breakdown voltage because some amount of field crowding still occurs.

CHAPTER 3 SIMULATIONS

This chapter presents the simulations used in the development of a novel wraparound field plate structure, that promotes uniform field distribution across the active device area by confining high intensity fields in the dielectric and thereby improving the breakdown voltages. It also studies the effect of various geometrical aspects on device performance. Breakdown characteristics for an ideal diode, a real diode with finite contact length and a conventional field plate technique used in the literature are simulated and compared to the novel wraparound field plate.

3.1 Introduction

We present our new wrap-around field plate structure[61] that surrounds the active device area along with the conventional field plate structure and compare the breakdown voltages. Also, we study the factors that affect the device performance.

A standard field plate technique(refer to figure 2-1) is chosen for efficiency comparisons with the proposed wraparound. The standard field plate technique exhibited higher efficiencies in terms of breakdown values among the various field termination techniques reported in literature till date. It also has the added benefit of being the easiest to build among all the reported field termination techniques. The standard field plate structure involves no ion implantation, unlike other techniques, which need to be carried out under controlled conditions. If not, higher energy ions tend to travel to bulk of the semiconductor and knock the Ga, N atoms out of the lattice and create defects. These knocked out free atoms will further collide with other atoms in the lattice causing impact ionization. Thus, the standard field plate in which Schottky contact is extended over the deposited dielectric is the more often chosen technique as it does not create additional defects during device fabrication resulting in comparatively improved breakdown characteristics than other device structures.

3.2 Simulation

Silvaco tool, DevEdit was used to define the device geometry parameters, such as thickness and carrier concentration for the substrate, buffer layer and epitaxial layer. Material-specific constants such as bandgap, dielectric constant, density of states, intrinsic carrier concentration, mobilities and lattice constants (shown in table 3-1) are taken from literature for Wurtzite GaN and are used in the code. However, as the GaN is far from being mature as an electronic semiconductor material, it is not rare to find discrepancies between the theoretically calculated material properties and those that are experimentally measured. (The complete code for various device architectures used in this study is available in the appendix).

Parameter	GaN	Units
Band gap	3.42	eV
Lattice constant	3.189	
Critical Electric Field (E_c)	3.75	MV/cm
Hole life time(auger)	1e-9	s
Electron life time(auger)	1e-9	s
Valence band effective density of states@ 300K (N_v)	4.6×10^{19}	cm^{-3}
Conduction band effective density of states @ 300k (N_c)	2.3×10^{18}	cm^{-3}
Intrinsic carrier concentration(n_i)	2.9×10^{-9}	cm^{-3}
Dielectric	8.9	
Peak velocity	2.2×10^7	cm/s
Saturation Velocity	1.125×10^7	cm/s
Hole mobility	10	cm^2/Vs
Electron mobility	525	cm^2/Vs
Donor energy level	0.016	eV
Acceptor energy level	0.175	eV

Table 3-1 Material parameters used in GaN Schottky diode simulation[62-64]

Device simulations were carried out using Silvaco ATLAS. Special models such as field dependent mobility (FLDMOB), concentration dependent mobility (CONMOB), bandgap narrowing (BGN), Shockley Read Hall (SRH) and auger recombination (AUGER) were used to simulate the Schottky diode.

3.2.1 IDEAL DIODE SIMULATIONS

We start with an n-type free-standing GaN substrate with a 2 µm buffer and 5µm thick epitaxial layer. The carrier concentrations for this GaN buffer and epitaxial layer are $5\text{x}10^{18}$cm^3 and $5\text{x}10^{15}$ cm^3 respectively.

An ideal diode with infinite long contacts was simulated (see Fig. 3-1) so that it could be used as a reference for comparing the breakdown characteristics of other device designs. An ideal-diode acts like a parallel plate capacitor with the field varying longitudinally between plates. Further, the electric field in the lateral direction remains uniform across the drift layer.

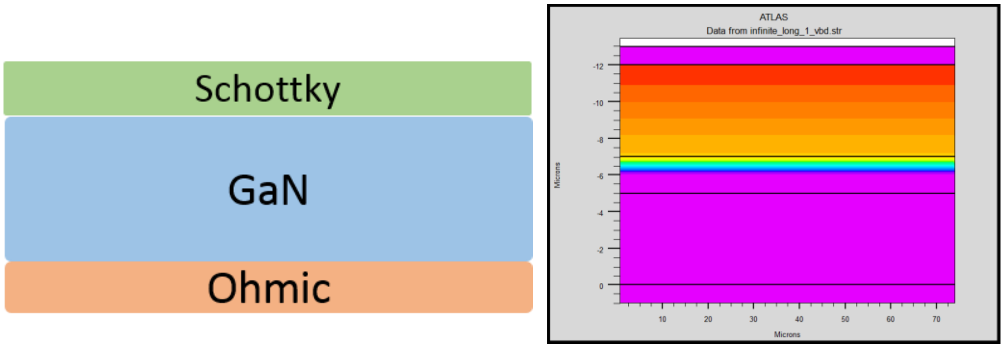


Figure 3-1: Ideal diode with infinitely long contacts(left) Field distribution during the breakdown of ideal diode at 1600V (right)

In reverse bias, with an increase in bias, the depletion width extends deeper into the epitaxial layer with high electric field concentrating at the Schottky and GaN interface. The field intensity gradually drops when moving towards buffer epilayer interface (see fig. 3-1). At the breakdown, the field at the metal semicoductor interface reaches the critical electric field of the semiconductor and results in avalanche breakdown. Simulation of an ideal diode, with a 5µm thick epilayer and a critical electrical field strength of 3.2×10^6 V/cm resulted in breakdown at 1600V, which falls in our medium power range of interest

3.2.2 REAL DIODE WITH FINITE LENGTH CONTACT

An actual diode with a finite Schottky contact length of 10µm on a 5µm epitaxial layer without surface passivation or field termination was simulated. This device had an uneven field across the epilayer, with field lines crowded at the edge. Figure: 3-2 shows the field distribution for a real diode at 500V breakdown. At the edges, the intensity of the field reaches the critical field strength of GaN, i.e. 3.3MV/cm. In most other regions the field intensity is only 1.2MV/cm which is far below the critical field strength of GaN. Due to the device geometry, the field across the epilayer is poorly managed, resulting in an early breakdown voltage of 500V as opposed to 1600V achieved for an ideal diode with similar epilayer thickness, and carrier concentrations.

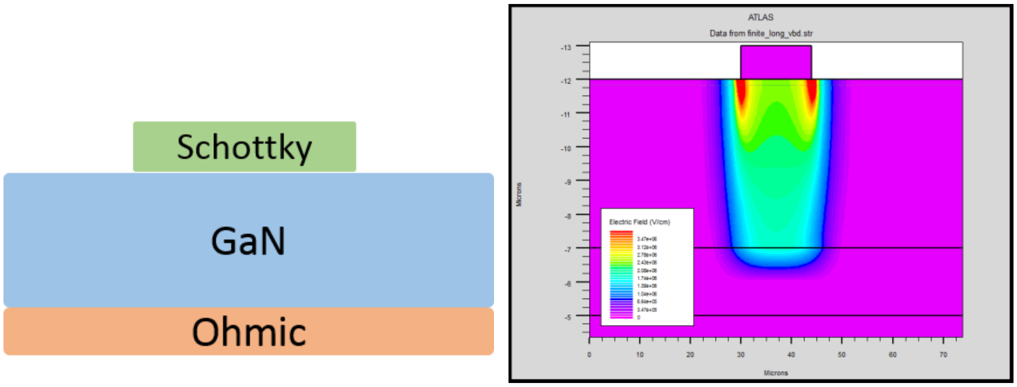


Figure 3-2: Field distribution in a real diode at the breakdown voltage of 500V

3.2.3 FIELD PLATE DESIGN SIMULATION

In this section, the most commonly used standard field plate design is describe and the impact of each geometrical aspect on its breakdown is presented.

For a standard field plate design, epilayer thickness, dielectric thickness, and field plate length are crucial parameters in determining diode breakdown. In all device simulations, SiNx acts as the dielectric layer. To estimate the impact of each parameter independently on diode performance three different sets of simulations were carried out by modifying dimensions of one factor at a time. First, the field plate length was varied from 0.3µm to 5µm, and epi and dielectric layer thicknesses were fixed to 4µm and 0.5µm respectively. As seen in figure 3-3, with every 0.2µm increase in field plate length, breakdown voltage increases by 150V uptil 3 µm, after which there is only a 100V increase in breakdown voltage for 1µm increase in field plate length.

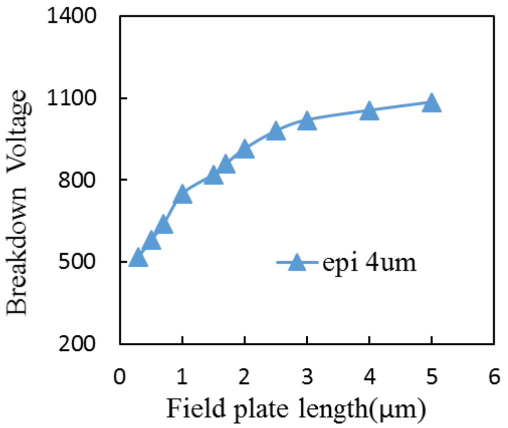


Figure 3-3: Breakdown Vs. Field plate length for a standard filed plate geometry

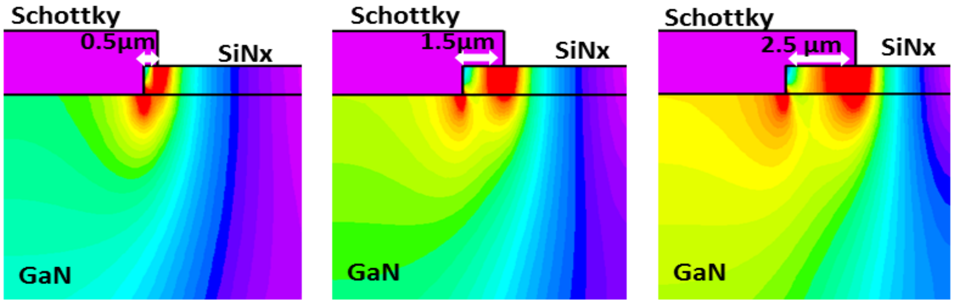


Figure 3-4: Field distribution at different field plate length

The increase in breadown voltage with the field plate length can be comprehend from the field distribution in each case as shown in figure 3-4. As the field plate length increases, the high-intensity field gets spread over a wider region away from the edge as shown. Thus, the breakdown voltage (V_{BD}) improves with an increase in field plate length, reaching a maximum value at an optimum length after which extension of the field plate will not affect the breakdown voltage. Based on simulation results, 5 um is determined as the optimum field plate length.

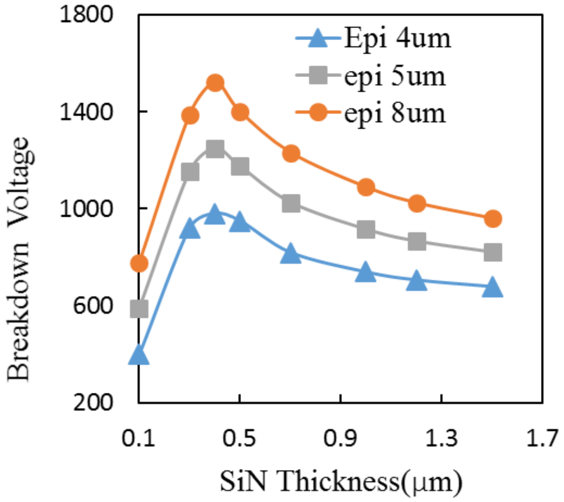


Figure 3-5: Breakdown Vs. SiNx thickness

Second, with determined field plate length of 5 um, breakdown voltage as a function of SiNx thickness is simulated for 4µm, 5µm and an 8um thick epitaxial layers as shown in figure 3-5. Breakdown values for thicker epilayers are higher. Also, for a given epilayer, increase in SiNx thickness results in Vbd increase till it reaches a peak value. With further increment, Vbd tends to decrease. For diode simulation using 5µm thick epilayer, Vbd varied between 600V to 1250V depending on the SiNx layer thickness. This dependence of Vbd on SiNx thickness is explained in the following section.

Epitaxial Layer thickness (µm)	**Breakdown Voltage (V)**	**Field plate length(µm)**	**Silicon Nitride thickness (µm)**
4	980	5	0.4
5	1250		
8	1520		

Table 3-2: simulated breakdown values for different field plate diodes

The above table is a summary of the obtained simulation results for field plate architecture. Compared to an ideal diode that used 5µm epitaxial resulting in 1600V breakdown, field plate diodes show lower break down voltage of 1250V. However, this is higher than the breakdown voltage of 500V observed in a normal diode without field termination.

3.2.4 WRAP AROUND DESIGN SIMULATIONS

This section discusses the wraparound technique and factors that affect diode breakdown. The wraparound architecture uses a mesa, in combination with a field plate that surrounds the active device area as shown in figure 3-6. Ohmic contacts are on the highly doped bulk substrate at the back of the wafer, and platinum on top of the mesa forms the Schottky contact. SiNx (light green region in fig. 3-6) acts as the dielectric layer.

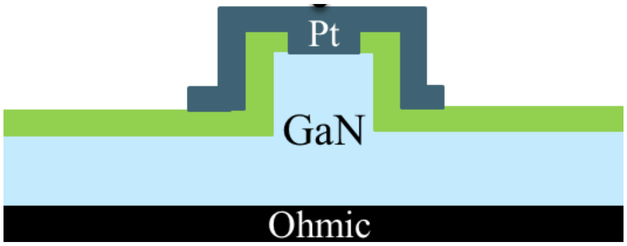


Figure 3-6: Wraparound architectures

Similar to the field plate, the breakdown voltage of the wraparound structure depends on factors such as mesa depth, epi layer thickness, dielectric thickness and SiNx neck length over the GaN. Figure 3-7 shows the simulated breakdown voltage as a function of dielectric thickness for different mesa depths. For any specific mesa depth and varying dielectric thickness, the breakdown voltage of the device displays an optimum peak value at a certain dielectric thickness. At any value above or below this optimum thickness, the device shows lower breakdown voltage.

The breakdown voltage dependence on SiNx thickness followed the same trend in both field plate designs. This variation in breakdown voltage for different SiNx thicknesses can be explained in 2 stages- (i) dielectric breakdown (ii) ineffective field control. At lower thicknesses breakdown of the device is predominantly due to the failure of SiNx rather than GaN breakdown. As layer thickness increases breakdown values improve reaching an optimum at which high-intensity fields move from GaN and are confined within the SiNx. Since SiNx has higher dielectric field strength compared to GaN, it can withstand field crowding at a higher bias. With further increase in the SiNx thickness, the effects of surface band bending and charge depletion decay. At higher dielectric thicknesses, as the field plate moves away from the semiconductor surface, it will have less control over the field in the semiconductor which results in early breakdown.

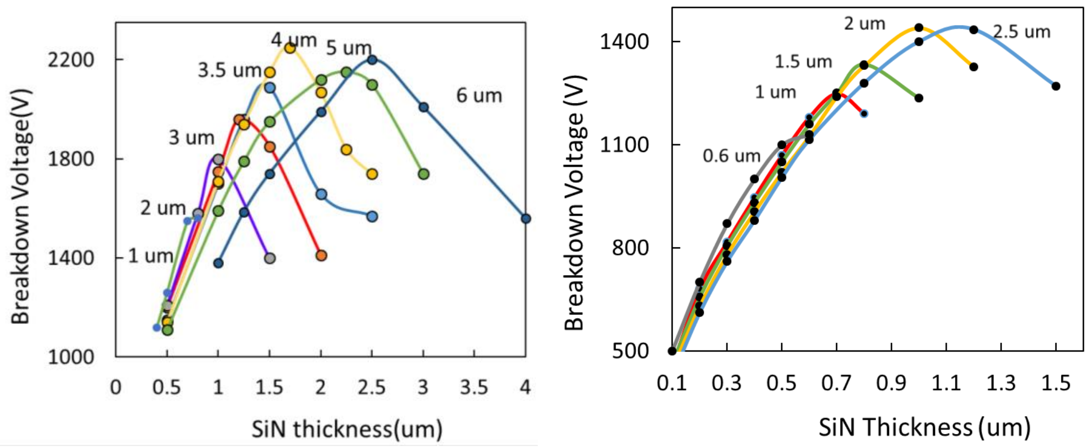


Figure 3-7: Breakdown voltage Vs. Dielectric thickness for different mesa depth for an 8µm epilayer (left) 5µm epilayer (right)

Breakdown also depends on the mesa depth. For a given SiNx and an epilayer thickness, breakdown voltage increases with increasing mesa depth reaching a maximum value, with further increase in mesa depth, the breakdwon value decreases as shown in figure 3-7.The optimal depth is observed to be half of the epilayer thickness. Therefore for a 5um and 8um epilayers, a high breakdown of 1450V and 2210V respectively was observed with mesa of 2.5um and 4um.

The breakdown voltage also varies with the SiNx neck length, i.e., the distance between the edge of the Schottky contact to the mesa edge. Breakdown values are high for SiNx neck length of 1 -2 µm. With further increase in neck length, the edge of the field plate moves farther away from the edge of the contact and thus, will have less control over the field distribution as shown in fig. 3-8. With these simulations, the impact of each geometrical aspect on field distribution and breakdown characteristics is assessed, and subsequently, an optimized device geometry for both the field plate architectures was chosen to meet medium power regime voltages.

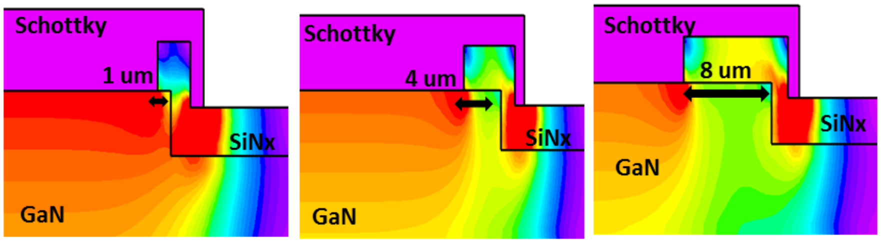


Figure 3-8: Field distribution for diodes with different SiNx neck length

Figure 3-9 compares electric field distributions at breakdown, in a diode without field termination, a standard field plate and a wraparound field plate. It is evident that in a basic diode, field crowding is severe at the metal contact periphery, and the field in the epitaxial layer is non-uniform. With the standard field plate, the peak electric field is distributed at the contact edge; however, the field intensity is non-uniform with the peak intensities remaining at the surface. This results in early breakdown of the device. With the wraparound structure, the potential along the epitaxial layer of the device is found to be more uniform. The device is designed to confine high-intensity fields within the dielectric and to maintain a uniform field across the epitaxial layer.

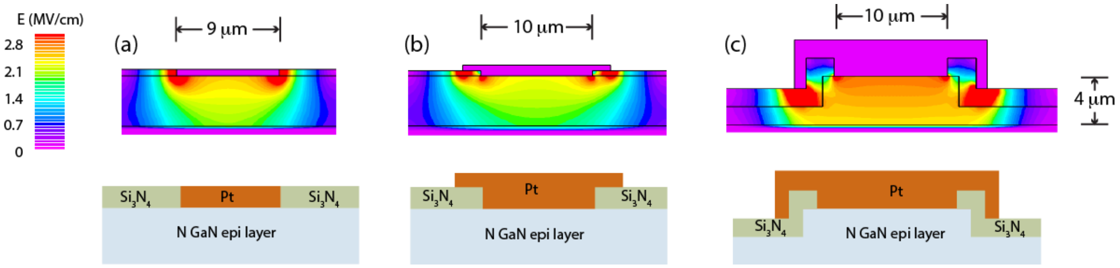


Figure 3-9: Field distribution in basic diode (a)without field plate, (b) with field plate, (c) with wrap around field plate

3.2.5 FORWARD CHARACTERISTICS

So far, we worked on device optimization to achieve a higher breakdown voltage. For a power diode, it is also essential to have a lower on-resistance in the forward bias along with blocking higher voltages in the reverse bias.

On-resistance is typically measured at which the current density reaches 100 mA/cm^2. However, since these simulations are based on 2-dimensional design, it is not feasible to measure the current density. Therefore, forward currents for diodes with standard field plate and wraparound field plate with similar Schottky contact length and epilayer thickness are compared. As shown in fig.3-10 the standard field plate (yellow trace) and wraparound field plate (red trace) have similar on-currents on the order of 10^{-5} A at 0.8V indicating the same on-resistance. Therefore taking both on and off characteristics into consideration, it is evident that wraparound design has an edge over the standard field plate with both similar on-resistance and higher breakdown voltage.

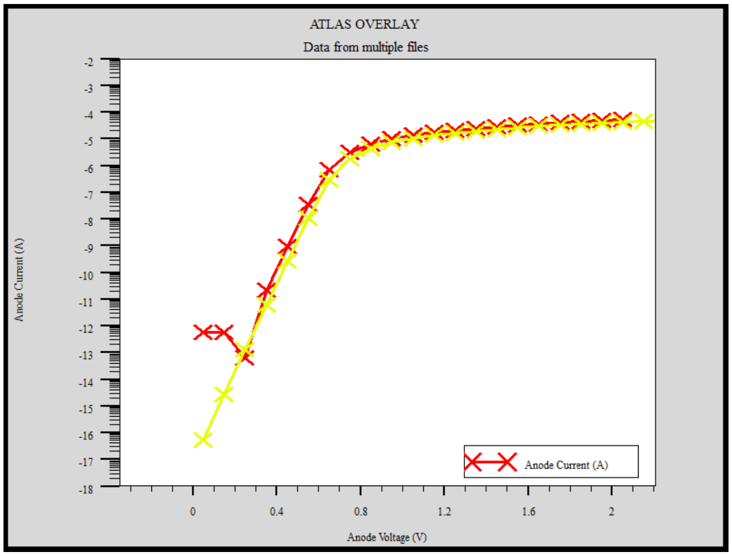


Figure 3-10: forward bias for wrap around(red) and standard field plate design(yellow)

3.3 Conclusion

This chapter discussed the design and simulation of a new wrap-around field plate termination structure for high voltage Schottky diodes. The electric field distribution patterns in various other field termination techniques are compared and it was proven that the wrap around structure has an electric field distribution closer to the ideal compared to other conventional designs. These geometric improvements result in improved breakdown voltages of 1450V using a wraparound design and 1250V using a standard field plate compared to 500V in a normal diode without field termination. The next chapter discusses the physical manifestation of the wrap around diode using GaN grown on sapphire substrate.

CHAPTER 4 LATERAL GAN SCHOTTKY DIODES ON HVPE GROWN FILMS ON SAPPHIRE

In this chapter, the device fabrication and testing aspects of the wraparound diodes built from low-cost hydride vapor phase epitaxy (HVPE) films grown on sapphire are discussed. A standard field plate diode is also built, and is compared to a wraparound diode. Further, the impact of intrinsic defects of HVPE grown films, and defects induced during fabrication on the diode breakdown performance are presented. The initial set of passivation studies performed on these diodes is also discussed.

4.1 Introduction

GaN as previously mentioned has superior material properties such as wide bandgap, higher critical electric field strength and a higher drift velocity. Theoretically then, GaN has a superior figure of merit than Silicon for power device applications. However, due to high substrate cost and lack of availability of single crystalline bulk substrates, high power GaN devices have had limited commercial application. Most of the lateral devices reported in the literature use films grown on heterosubstrates by metal organic chemical vapor deposition(MOCVD)[57, 65] or Metalorganic Vapour Phase Epitaxy (MOVPE)[51] on hetero substrate. There are limited diodes that used films grown using hydride vapor phase epitaxy (HVPE)[47] on foreign substrate, mainly due to HVPE grown films suffer from a high threading dislocation density(TDD) on the order of 10^9cm^2 due to the lattice mismatch between the GaN and the substrate, despite being less expensive method of deposition.

The lateral diodes in literature that used HVPE grown films on heterosubstrates, either used layers on the order of 8-10μm thick[47], or 100-400μm thick layers[40]. And recently vertical diodes using drift regions grown by HVPE instead of conventional MOCVD on bulk HVPE substrates[45] are reported. These HVPE on HVPE are almost 7-10 times more expensive than typical HVPE grown on heterosubstrates.

In this chapter, suboptimal 5μm thick GaN drift layer grown by HVPE on sapphire is used despite the high TDD for the diode fabrication, firstly to optimize the fabrication steps, secondly to study the behavior of diodes built on thin HVPE layers (compared to the thick ones reported in literature) and lastly these substrates are less expensive ($100/wafer) compared to bulk HVPE GaN($700/wafer).

4.2 Material characterization

To evaluate the quality of the HVPE grown film on sapphire, the photoluminescence(PL) of the drift layer was measured at room temperature as shown in Figure 4-1. A renishaw RL633 spectrometer with a UV laser emitting at 332nm with 5mW power, and a CCD detector were used. The PL signal was composed of two peaks and with maximum peak intensity at 2.2 eV and a lower intensity peak at 3.4 Ev as shown in Figure 4-1. The PL peak at 2.2Ev is commonly referred as defect or yellow PL for Gan and is associated to traps formed by Carbon occupying Ga site to form C_{Ga} or N site to form C_N by which it behaves as shallow donor or acceptor[66]. These trap states impact the device performance in terms of the forward current, and breakdown voltage. Saitoh et.al reported a correlation in the leakage currents in vertical diodes with the normalized yellow band and indicated yellow PL could be a signature for carbon contamination in GaN. Also, the SIMS data provided by the manufacturing company indicated a background impurities concentration of C ($4x10^{15}$ cm^{-3}), O (2 $x10^{18}cm^{-3}$), Si ($1x10^{18}cm^{-3}$) and H($2x10^{16}cm^{-3}$).

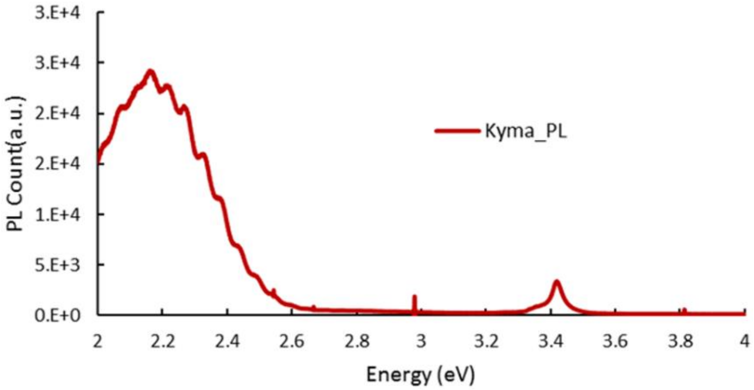


Figure 4-1: PL spectrum for HVPE grown GaN film on Sapphire

Later, these substrates were etched in hot phosphoric acid at 110^0C, to estimate the defect density quantitatively[67]. According to the literature, the wet etching results in selective etching at the defect sites forming hexagonal pits as shown in figure 4-3. The total number of defects were determined by manually counting the number of pits in an SEM image of about $1\mu m^2$ area, and then the defect density for a unit sq-cm was estimated to be $5\text{x}10^{8}$ cm^{-2}. This value matches with the standard values ($<10^{9}$ cm^{-2}) provided by the manufacturing company for the unintentionally doped GaN films on sapphire.

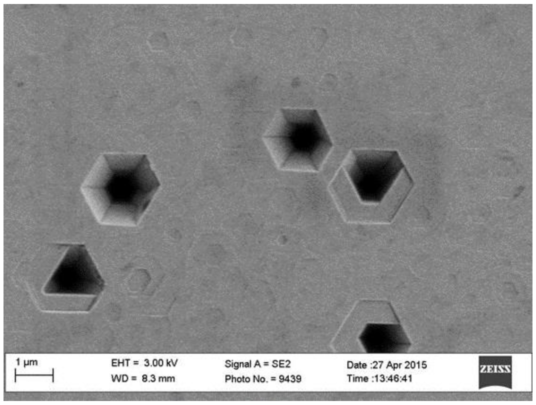


Figure 4-3*:* Selectively etching of defects using phosphoric acid at 110C

Figure 4-2: cross-sectional view of GaN on Sapphire

To estimate the difference in the quality of HVPE grown film to MOCVD films(discussed in the later chapter), high resolution rocking curves were measured. A Rocking curve is used to study dislocation density in epitaxial films. A crystalline material will produce a sharp peak and while films with defects such as mosaicity, dislocations, or curvature create disruptions in the perfect parallelism of atomic planes and thus result in broadening of the rocking curve. For HVPE films a full-width-at-half-maximum (FWHM) of the ω rocking curve from (0002) reflection is 721 arcsec (shown in fig.4-4) which is relatively a higher value than usual HVPE films reported in the literature[45].

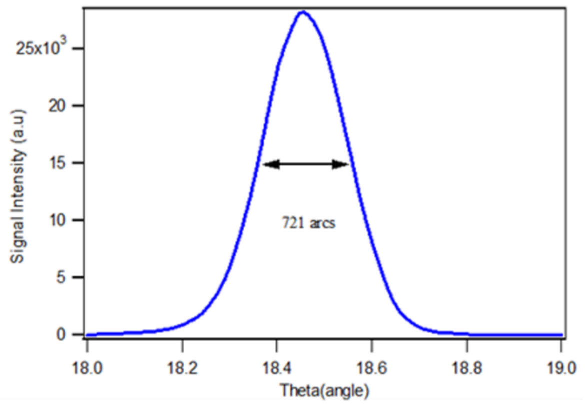


Figure 4-4: Rocking curve for HVPE GaN on sapphire from (0002) reflection

From these characterization techniques, it is evident that these HVPE films have high impurity traces of C, O and Si along with the treading dislocations originating due to lattice mismatch.

4.3 Device fabrication

Schottky diodes were fabricated on a 5±1 µm thick, unintentionally doped GaN layer grown on a 2-in sapphire substrate with a 300 nm AlN buffer. According to the company provided data sheet the threading dislocation density of GaN epi layer was 10^9 cm^{-2}. Before fabrication, the wafer was cleaned with acetone (5 min), methanol (5 min), and HCl: H20 (5 min), followed by DI water flushing/N_2 blow drying to get rid of native oxide and organic contaminants from the surface. Then 5-6 um thick positive photoresist AZ4620 was spin coated at 4000 rpm for 10seconds, followed by a soft bake at 115^0C for 5min. Photoresist was then exposed to UV for 51 seconds and was developed in 3:1 AZ400.

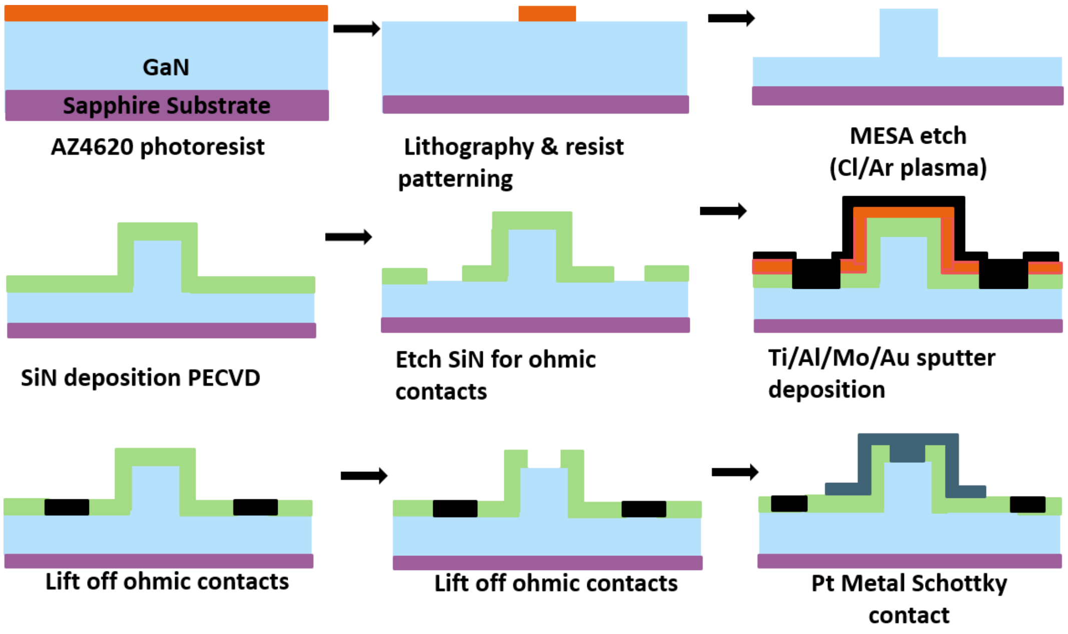


Figure 4-5: Process flow for lateral wrap around field plate

Once the pattern was transferred onto the substrate, the substrate was again heated at 115^{0}C for 2 minutes to harden the resist. Hard baking is a crucial step, to get rid of any leftover solvent and to harden the resist so that it can withstand high power plasma. Using photoresist as a mask a 2±0.5 µm deep MESA structures were etched at the rate of 0.2µm/min in Cl2(14 sccm) and Ar (6 sccm) based optimized plasma in ICP(400W) and RIE(60W) at 10mTorr chamber pressure. Sample was cleaned in acetone, IPA and DI water to get rid of the photoresist that was used as mask and to remove any organic byproducts that got sputtered on to the surface during etching. Then a 100-nm thick amorphous SiN_x film was deposited by PECVD at a stage temperature of 350^{0}C, with NH_3, SiH_4, and N_2 as source gases. SiN_x windows using O_2 and SF_6 plasma were etched around the mesa as shown in the figure 4-6 . An ohmic contact was then formed on GaN surface by dc magnetron sputtering of Ti/Al/Mo/Au in Ar ambient. Metal liftoff from the wafer leaves the concentric ohmic rings with the mesa at the center. Contacts were annealed in N2 atmosphere at 650^0C for the 30s. Later SiNx windows were etched one more time on top of mesa. Then, a Schottky contact was formed by sputter deposition of platinum. Metal liftoff from the wafer leaves a circular platinum contact with a wrap-around field plate in the unmasked region. Figure 4-6 shows the microscopic images of each process.


Resist after Hard bake after etching for 650 s (2 um) Ohmic windows SiN windows Schottky contact

Figure 4-6: Microscopic images for each step involved in the device fabrication.

Later diodes with standard field plate were also made on HVPE grown on sapphire substrates. The process flow for the field plate diode was similar to wraparound except for etching. The field plate design does not need additional etching as shown in figure 4-7.

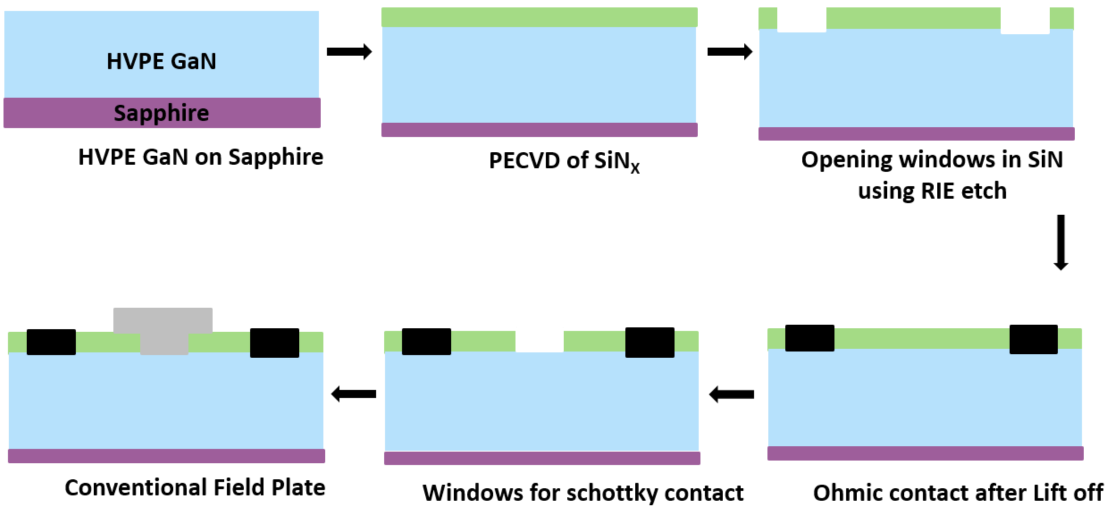


Figure 4-7: Process flow for lateral field plate diode

4.4 Electrical measurements

To estimate the carrier concentration of the drift layer, capacitance-voltage (C-V) measurements were done using a Keithley model 4200 semiconductor characterization system. A reverse DC bias ranged from 0 to 2V with a superimposed 20 mV AC signal with a frequency of 200 kHz was applied across the Schottky contact. Under reverse bias, the region of uncovered charge in the GaN makes up the depletion region and define the depletion width. As the reverse bias potential increases, the width increases, which in turn decreases the capacitance. Figure 4-8 shows the plot of $1/C^2$ Vs. reverse bias voltage applied. The carrier concentration of the depletion width is obtained by using the eq. 4-1 The carrier concentration of the unintentionally doped epitaxial layer was found to be 6 x10^{16} - 10^{17}cm^{-3}. This value is higher than typical unintentionally doped HVPE films.

$$N_D = \frac{2}{qA^2\varepsilon_S}\left[-\frac{1}{d(1/C^2)/dV}\right] \qquad (4\text{-}1)$$

N_D: Carrier concentration

A: Schottky contact area

ε_s: Dielectric constant

C: Measured capacitance

V: Applied bias

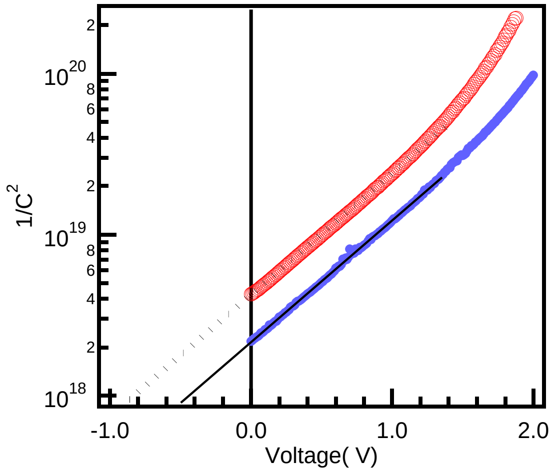


Figure 4-8: $1/C^2$ - V for HVPE grown on sapphire at room temperature

The I-V characteristics for several diodes with radii of 25 µm, 50 µm, and 100 µm were measured using a Keithley 2100 source meter at room temperature using a probe station in air under ambient conditions. The bias was swept from 0V to 5V in the forward direction and then reverse bias characteristics were obtained by sweeping the voltage from 0V to -150V.

4.5 Results and discussion

A number of diodes with both the field plate designs were tested. The on-resistance for these diodes was calculated at the point where the current density reaches 100 mA/cm^2. The voltage at which the diode undergoes irreversible physical damage was considered as the breakdown voltage.

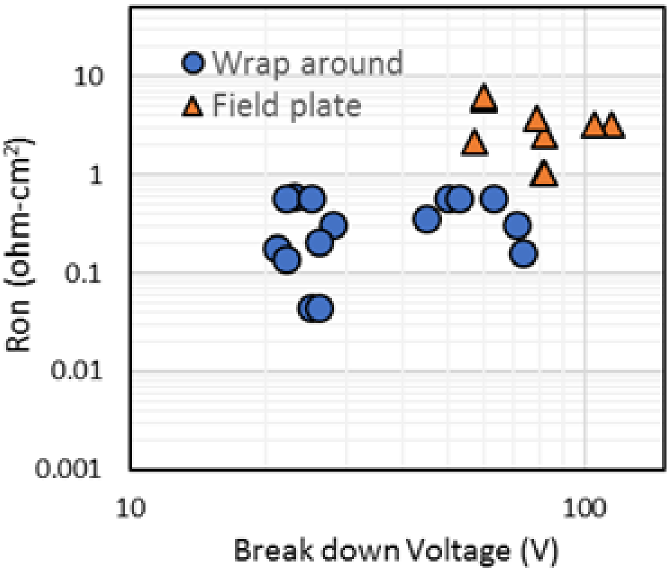


Figure 4-9: Ron versus breakdown for diodes with field plate and wraparound

The on-resistance versus breakdown for all the diodes with both the field plate geometries is shown in figure 4-9. The breakdown voltage varies from 50V to 120V for the lateral field-plate diodes and from 22V to 73V for the wraparound field plate diodes. This variation in breakdown voltage is due to the non-uniform distribution of defect states across the drift layer. According to theoretical calculations, the wraparound field plate diodes should have higher breakdown voltage than lateral field plate diodes because of the more uniform field distribution at the periphery of the contact [68]. However, experimentally the wraparound field plate diodes break down at a lower voltage than the standard diodes. In addition, the wraparound field plate diodes have a lower forward bias on resistance than the lateral-field plate diodes. As shown in Fig. 4-9, (R_{on} vs. breakdown voltage plot), the standard diodes have R_{on} values ranging from 1 to 10 ohm-cm2 while the wraparound field plate diodes have R_{on} ranging was 0.003 to 0.7 Ohms-cm2.The discrepancy in on-resistance values between these two diode structures was surprising considering that the radius of the Schottky contact was designed to be identical in each case.

Figure 4-10 shows the forward and reverse bias characteristics of a 25 µm radius diode with a standard lateral field plate (dashed blue line) and with a wraparound field-plate (solid red line).

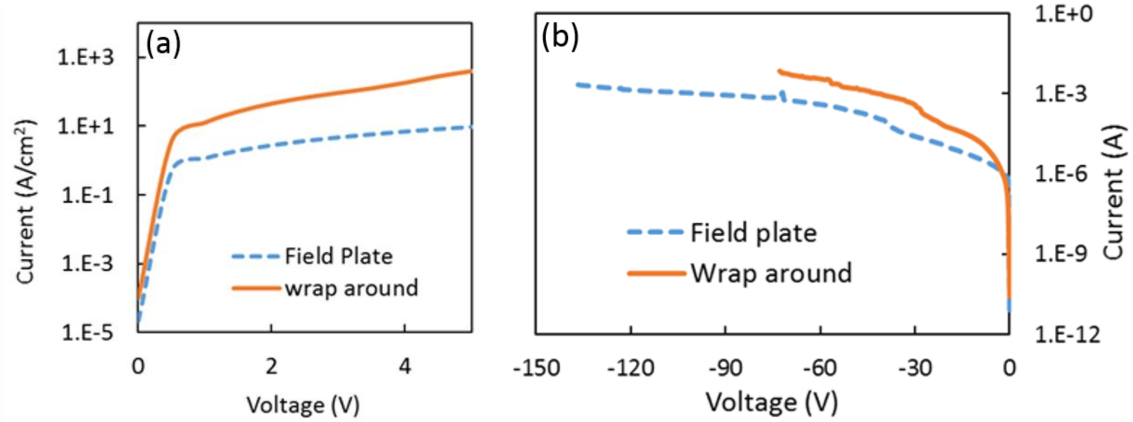


Figure 4-10: I-V for 25µm radius diode with standard field plate (dash line) and wrap around structure (solid line) (a)forward characteristics (b)reverse characteristics

It is evident that the current density is about an order of magnitude higher in the wraparound field plate dieodes compared to the standard field plate diodes.The higher forward current bias could be due to leakage at the GaN / SiN_x interface[69, 70]. To verify this, mesa diodes without amorphous SiN_x layer were fabricated and tested.

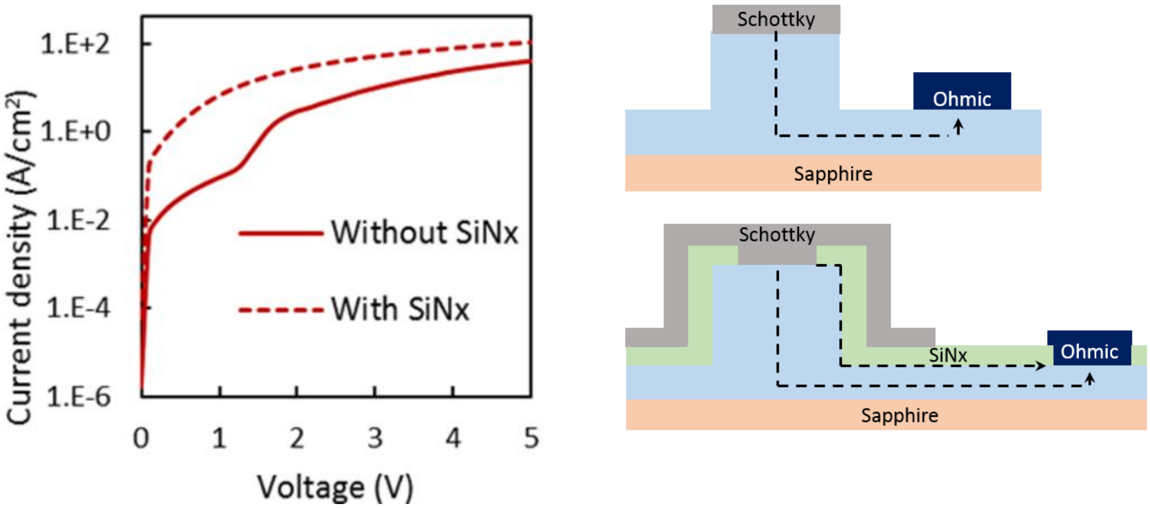


Figure 4-11: I-V for mesa with and without PECVD SiNx(left) diode schematic showing the current paths with and without SiNx(right)

Figure 4-11 shows the I-V characteristics for a 100um radius diode with (dashed line) and without (solid line) an amorphous SiN_x layer. There is a two order of magnitude increase in on current with the deposition of the amorphous SiN_x layer, confirming that the SiN_x deposition is providing an additional current path between the GaN and the contact. However, in the standard field plate diodes that also use the SiNx dielectric, there are no high current densities.

The difference between the two geometries is that the standard-field plate diode does not require any etching while the wrap-around field plate diode requires a high power plasma to create the mesa structure. Etching exposes underlying defect layers [71-74]. These could contribute to the leakage currents at the GaN / dielectric interface. To isolate the impact of each of these factors, the IV characteristics between the sidewalls of a 2 µm deep trench was measured at three different etch depths: (i) with the probes placed on the unetched top surface (5µm away from the buffer epitaxial layer interface) (ii) on the sidewalls, at a 4 µm distance away from the interface (iii) on the etched surface at 3μm away from the interface (see inset to Fig. 4-12). With every 1 um increase in etch depth there is a 100 x increase in the current between the probes. This indicates that as we move deeper towards the interface, the defect density increases, and lowers the resistance. The observation that resistance decreases with etch depth is specific to HVPE films. Similar measurements (not shown here) showed no similar effect in MOCVD grown films.

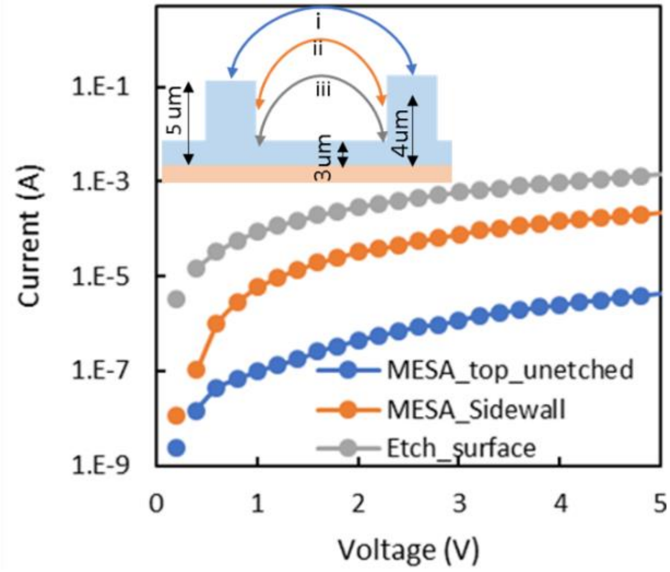


Figure 4-12: I-V measured by placing the probes on top of mesa surface (unetched), sidewall and the etched surface

To confirm this, a standard field plate architecture was used. The top 150 -200 nm surface layer was etched and then a standard field plate with SiN_x layer was built. The field plate diodes on etched surface have higher on currents and lower breakdown voltages (20-30V) similar to wraparound diodes. Confirming that SiNx allows contact to the high defect region and there by increasing the current densities in both forward and reverse bias.

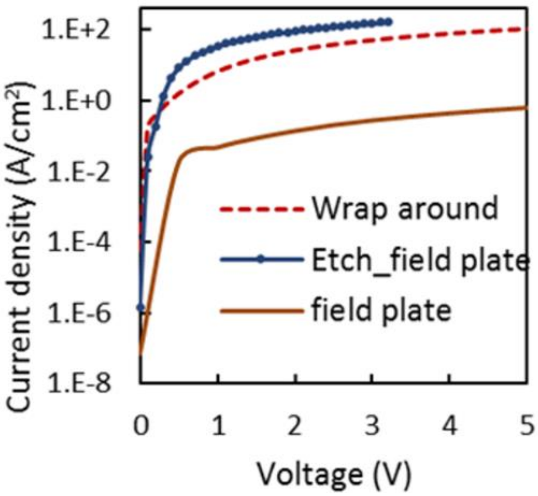


Figure 4-13: Forward characteristics for a wraparound, standard field plate and etched field plate

From the above discussion, it is established that any potential improvement that might be provided by the wrap-around field plate design is negated by the leakage currents along SiNx and the defective GaN surface. These defects could be either etch induced surface defects or the intrinsic bulk defects that surface after etching the mesa. This will be studied further in the next chapter. Without this, the field plate diode is a better design for the defect rich HVPE material. The standard field plate architecture does not need the additional etching, which only worsens the HVPE grown diode performance.

4.5.1 Surface passivation

Etching results in the formation of non-stoichiometric surface due to non-preferential removal of Ga and N atoms from surface, leaving behind dangling bonds on the surface. These surface defects introduced by etching might additionally contribute to the leakage currents in the wraparound diodes. To mitigate these etch induced defects [75] ,GaN samples after etching were treated in tert-butanol and ammonium sulfide [$(NH_4)2S_X$] solution at 60C for 5 min. According to Martinez et al., sulfide passivation results in decreasing the dangling bond density by Sulphur atoms occupying the nitrogen-related vacancies and forming Ga-S[76].

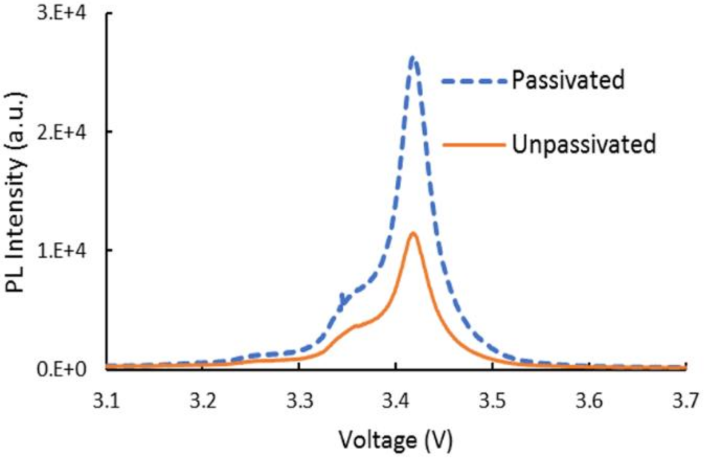
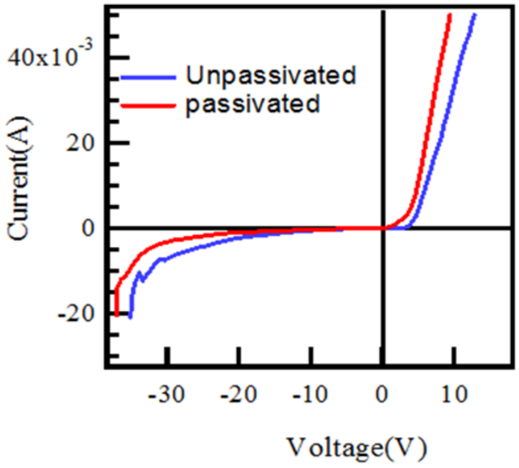


Figure 4-14: PL for passivated and un-passivated samples at room temperature

Following passivation treatment, samples were cleaned in DI water and blown dry in N2. The next step was to verify, the effect of passivation on the surface prior to device fabrication. So, the PL for the passivated samples was measured. As shown in figure 3-14, Sulphide treated sample showed a stronger photoluminescence intensity by a factor of 2.5 with respect to an untreated sample. This indicates that the effect of surface states has been substantially reduced by the treatment.

After this, wraparound diodes with radii of 25um,50um and 50um were built using these passivated samples. It was found that passivation did not produce a significant difference in the diode behavior, though there is a strong improvement in PL intensity. Figure 4-15 shows the I-V for a 50um radius diode with passivation and without passivation.



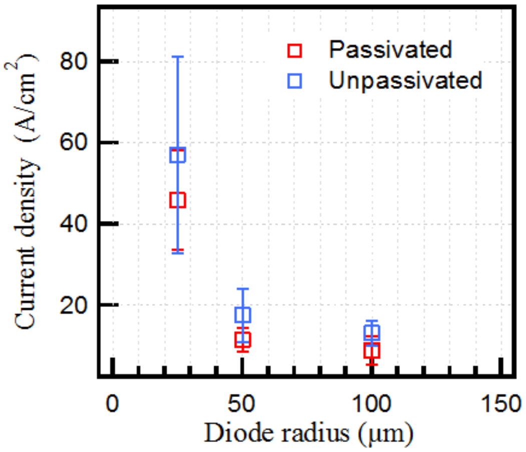


Figure 4-15: I-V for a 50um radius diode passivated (red) Vs. un-passivated(blue)

Figure 4-16: Average leakage current density Versus diode radius for passivated and Unpassivated diodes

To estimate the effect of passivation more accurately on leakage currents, the average of current density in the reverse bias at - 20V for 4 diodes of each radius was measured and compared to un-passivated diodes as shown in figure 4-16. Though there was not a substantial improvement in the breakdown values. It was interesting to notice that the change in the average leakage current densities is relatively higher in smaller diodes with 25 μm radius compared to 50μm and 100μm radius diodes. Indicating that in diodes with large radius, bulk defects are the major source for leakage paths than the surface states. And with the decrease in diode radius, the leakage currents along the surface states becomes significant as the number bulk defects in the smaller area will likely reduce compared to large diodes. Therefore, bulk defects are crucial in determining the diode performance and passivation was more effective in smaller diodes with less bulk defects compared to large diodes. Further, from figure 4-16, the deviation is higher is the smaller diodes compared to others, due to variation in the bulk defect distribution in smaller diodes.

4.6 Conclusion

In this chapter, a physical diode with wraparound field plate and a standard field plate were built from a low cost highly defective HVPE grown film on sapphire and tested. Each process step involved in the diode fabrication was developed and optimized. The wraparound diodes showed lower breakdown voltages than field plate diodes in disagreement with theoretical predictions. Lower performance in the wraparound devices was found to be due to its geomerty that reveals defective surface which further with the SiNx deposition, makes additional conducting paths along the interface resulting in the early breakdown of the diode.

Also, the impact of the surface states was estimated by comparing the diodes with and without sulphide passivation. The Surface passivation, using ammonium sulphide was efficient in suppressing the impact of surface states, however the impact of passivation on overall diode performance is not significant particularly in diodes with larger radius as bulk defects are the major source for the leakage currents.

CHAPTER 5 VERTICAL SCHOTTKY DIODES ON BULK GAN SUBSTRATES

5.1 Introduction

From chapter 4, it was evident that intrinsic bulk defects and additional bulk defects that are exposed during etching, in combination with SiNx are the major leakage current paths hindering the wraparound diode performance. To overcome this issue related to leakage currents, a less defective MOCVD grown layers on bulk Ammono GaN are used to build diodes in this chapter.

5.2 Material characterization

GaN layers grown by MOCVD; on bulk GaN are purchased from Ammono(Poland) [30]. A 5um thick unintentionally doped GaN is grown on a highly doped 350um thick bulk Ammono GaN substrate. MOCVD growth results in a high carbon impurity, as carbon is an intrinsic component of the trimethylgallium (TMGa) source causing the high background n-type carriers. According to the SIMS data provided by the manufacturing company, the epilayer contains C~1.8x $10^{17}cm^{-3}$ and O~9x10^{15} cm^{-3}, with net carrier concentration of $1*10^{16}cm^{-3}$ to $1*10^{17}$ cm^{-3}.

The carrier mobility for these films was estimated to be < 200 cm^2/V-s by the manufacturer. The mobility is far below the theoretically predicted value of 1245 cm^2/V-s[77, 78] .

A full-width-at-half-maximum (FWHM) of the ω rocking curve from (0002) reflection is 28 arcsec indicating a low threading dislocation defect density in film.

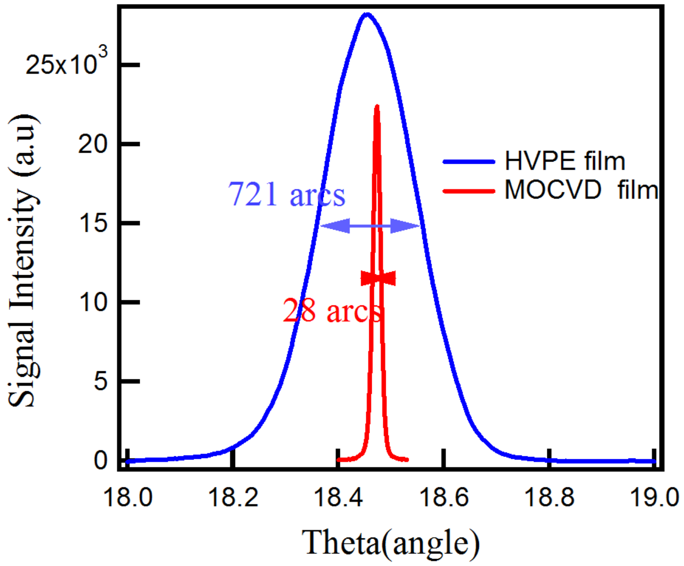


Figure 5-1: XRD rocking curve for MOCVD grown GaN film bulk Ammono thermal(red) and HVPE grown on sapphire (blue)

5.3 Device fabrication

The device fabrication followed the same sequence of steps as described in the lateral diodes. Prior to fabrication, the substrates were cleaned in HCl, acetone, IPA and DI water followed by blow drying in N_2. Ohmic contacts were deposited using DC magnetron sputtering on the back side of GaN substrate. Then a mesa structure was etched, using a new etch recipe as discussed below, to reduce etch induced surface. Followed by SiNx deposition, etching of SiNx windows and finally deposition of platinum to create the wraparound architecture (figure 5-2 shows complete process flow for vertical wraparound diodes).

Diode fabrication processes including ohmic contacts and dry etch recipe were modified to reduce the impact of surface defects caused during diode fabrication. Also, a highly conducting substrate was used instead of sapphire.

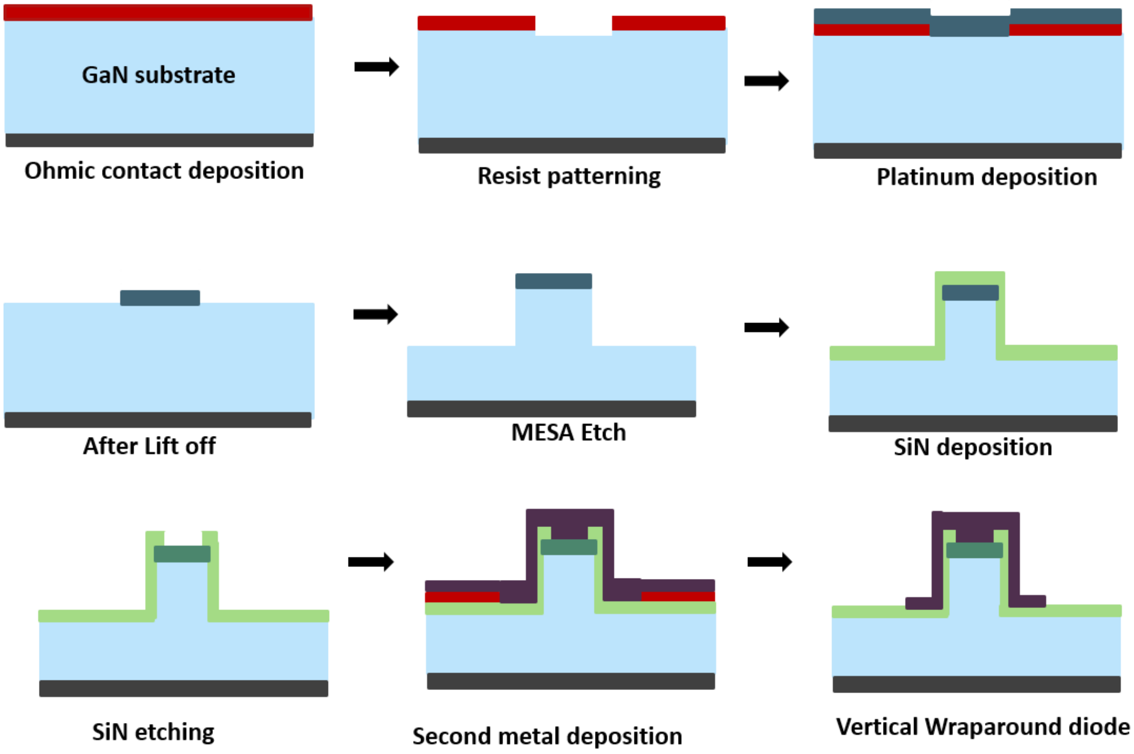


Figure 5-2: Process flow for vertical wraparound diode

(a) **Ohmic contacts**: In vertical diodes, unintentionally doped drift layers are grown on a highly doped substrate, and therefore ohmic contacts were deposited on the back side of highly doped GaN substrate. This is unlike; lateral diodes in which both ohmic and Schottky contacts were made on top surface, as HVPE film is grown on insulating sapphire substrate. Also, in vertical diodes instead of Ti/Al/Mo/Au, a more feasible and commonly used Ti/Al metal stack is used as ohmic contact[79].

(b) **Dry etching**: In the previous chapter, mesa was etched using a Cl2 and Ar gas based plasma at the rate of 0.2µm/min in a ICP/RIE etch tool. Any kind of etch induced defects will impact the diode. Therefore, to rectify the surface defects incurred due to exposure to a high-density plasma, Ar gas flow was reduced from 6sccm to 1sccm. Instead, an additional BCl3 gas (4 sccm) was used along with Cl2(16 sccm) at 5 mTorr chamber pressure. RIE power was maintained at 60W and 500W ICP with a DC bias of 80V resulted in a etch rate of 137 nm/min .According to [80], high energy Ar atoms sputter the GaN surface resulting in a non-stoichiometric surface layer while BCl3 results in a chemical etching of GaN instead of sputtering.

Also, previously photoresist mask used to etch mesa structures, was not stable in high density ICP/RIE plasma. Particularly, due to the erosion of photoresist at the edges resulted in rough side walls. To obtain much smoother surface, a platinum metal mask was used instead of photoresist. The metal mask in combination with BCl3/Cl2/Ar have resulted in a physically smooth side wall surface as shown in figure 5-3(a).

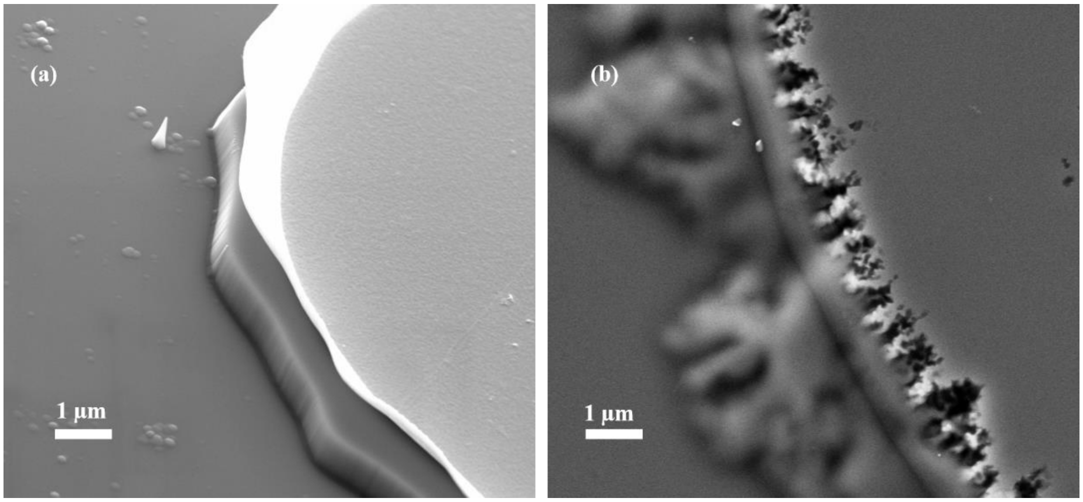


Figure 5-3: Mesa side wall surface after dry etching in Cl2/BCl3/Ar (a) metal mask (b) photoresist mask

(c) Thicker SiNx: SiNx is deposited using NH_3(20 sccm), N_2 (600 sccm) and 5% SiH_4/Ar (400 sccm) gases at 50W RF pulsed plasma at the rate of 20nm/min, with heater at 350^0C and chiller at 70^0C [81]. For lateral diodes, 100nm thick SiNx was used as a dielectric layer. However, it was found that 100nm was not thick enough to withstand high electric fields. Therefore, thicker SiNx layers were deposited on a highly doped Si wafers to test the quality and dielectric strength of SiNx films. Circular platinum contacts were deposited on top of SiNx layer to form a metal insulator semiconductor (MIS) structure. Further, bias was applied between the metal and semiconductor to test the strength of the SiNx layers. Breakdown voltage for different SiNx layer thickness are shown in figure

5-4. The electric field strength for SiNx with different thickness are calculated and listed in the table 5-1.

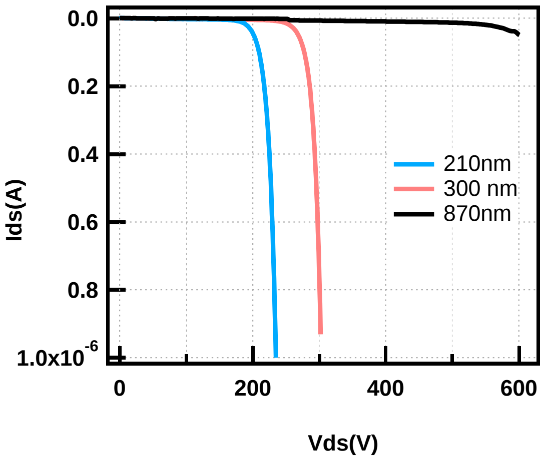


Figure 5-4: Breakdown characterization for SiNx layer for different thickness

SiNx thickness(nm)	Breakdown Voltage(V)	Electric field strength(MV/cm)
210	235	11.1
300	300	10.1
870	601	6.9*

Table 5-1: Electric field strength for PECVD deposited SiNx layers of different thicknesses

*measured at a bias lower than the breakdown voltage

The electric field strength for PECVD deposited SiNx is reported to be 11MV/cm[82] and the measured values for different thickness match with reported. Based on these calculations, a SiNx layer of about 600nm thick was used in the fabrication of vertical wrap around diodes.

5.4 Electrical measurements

The I-V characteristics for several diodes with radii of 25 µm, 50 µm, and 100 µm using a standard field plate and a wraparound were measured using Keithley 2100 source meter, at room temperature using a probe station in air under ambient conditions. The bias was increased in steps of 0.1V from 0V to 10V in the forward direction and then in steps of 1V in reverse bias from 0V to -500V. The breakdown voltage is commonly defined at which reverse current density reaches 100 mA/cm^2. However, the reverse I-V was measured beyond this voltage point to estimate the avalanche breakdown point for the diode.

5.5 Results and discussion

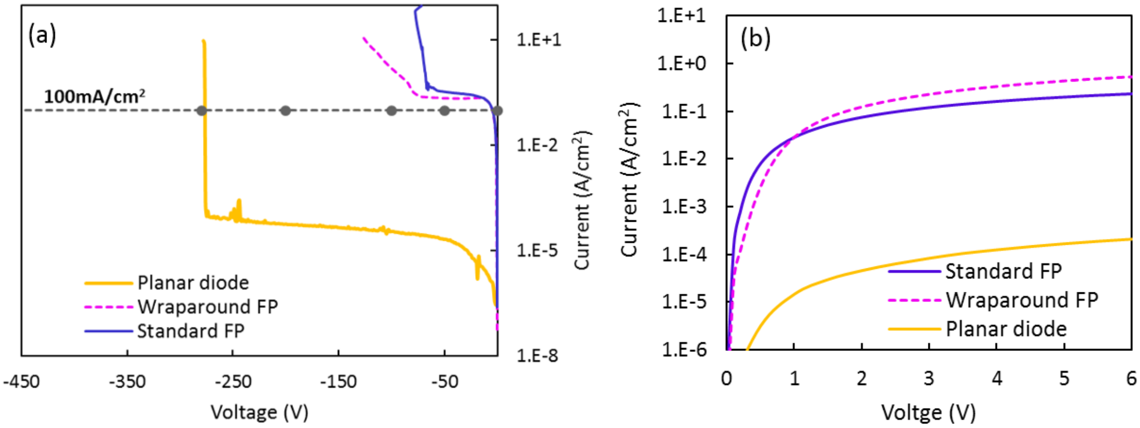


Figure 5-5:I-V for a standard field plate, wraparound and planar diode (a) reverse (b) forward bias

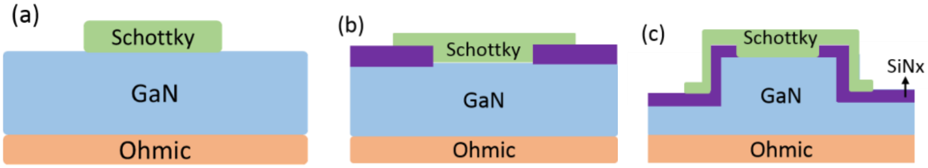


Figure 5-6:Schematic for (a) planar diode (b) standard field plate (c) wraparound field plate

Figure 5-5(a) shows the reverse I-V characteristics for a 100 µm radius diode with a standard field plate (solid blue line), a wraparound (dotted pink line) and a planar diode (solid yellow) formed by depositing a circular Schottky contact on the top surface without dielectric layer or field termination plate. The blue dotted horizontal curve at 100 mA/cm^{-2} is defined as the breakdown voltage in the literature. The schematic for each diode is illustrated in figure 5-6. From the above graphs, a planar diode with a Schottky contact, without a dielectric layer or field termination have a leakage current density on the order of 10^{-5}Acm^{-2} with a breakdown voltage of 260V, while diodes with the field plates have leakage current density of 10^{-1}Acm^{-2} greater than the breakdown current density(100mAcm^{-2}) at a lower voltage compared to planar diode.

In forward bias, diodes with the field plate structures however, had lower resistance compared to planar diodes resulting in higher current densities as showed shown in figure 5-5(b).

The reverse bias result contradicts the simulation data, which predicted a higher break down voltage for a diode with a standard field plate and wrap around compared to planar diode. Also, the diodes with field plate did not show physical signs of breakdown such as dark spots that are typically observed either on the edges or on the diode indicating the breakdown point of diode (illustrated in figure 5-7). To understand this variation in the theoretical prediction and experimental data, more diodes were built, but were tested after each fabrication step to identify the factors that affect the performance of the wrap around diode before the final diodes were tested.

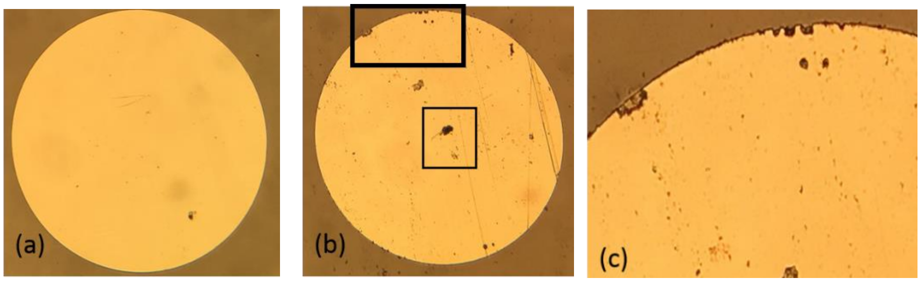


Figure 5-7: Microscope images of the diode(a) before applying bias (b) at the breakdown with the black spots appearing on the edges and on the diode (square regions). (c) Zoomed in view of the breakdown spots at the edges

To quantify the impact of dry etching on MOCVD films, diode with mesa alone was built compared to a planar diode as shown in figure 5-8. The reverse bias current densities for the planar diode and the mesa diode were same on the order of 10^{-5}A-cm^{-2}. This shows that leakage current pathways are either not created by the etching or do not form an electrical pathway between the two contacts[83]. Furthermore, the diodes with the mesa geometry showed higher breakdown values than the planar diodes. The breakdown voltage for planar diodes varied from 150V to 230V, and for mesa diodes between 230V-420 V. (shown in figure 5-15)

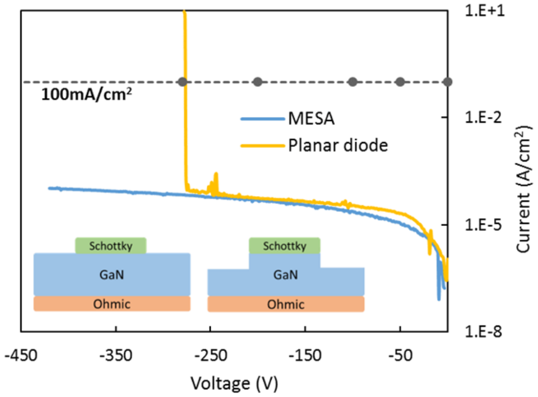


Figure 5-8: Reverse bias I-V for a planar diode and a mesa diode. Blue horizontal dotted line indicates the current density at the breakdown. Insite showing a planar and mesa diode.

The improved breakdown performance can be explained in terms of alleviation of hot spots caused due to field crowding at the edges of the contact. For instance, in case of a normal diode with circular contacts, as mentioned earlier due to field crowing, the intensity of the fields is high at the edge of the contact and on the surface of GaN resulting in early breakdown. In case of mesa diode, GaN adjacent to contact is etched, so that the field crowding will not occur in the semiconductor instead they crop up in free air that has higher electric field strength than GaN causing an improvement in the breakdown. To corroborate this further, diode with mesa of 1.5μm deep in a 5μm epilayer was simulated using silvaco tools. Simulations showed a higher breakdown of 630V in mesa diode and 500V in normal diode with circular contact (shown in Figure 5-9)

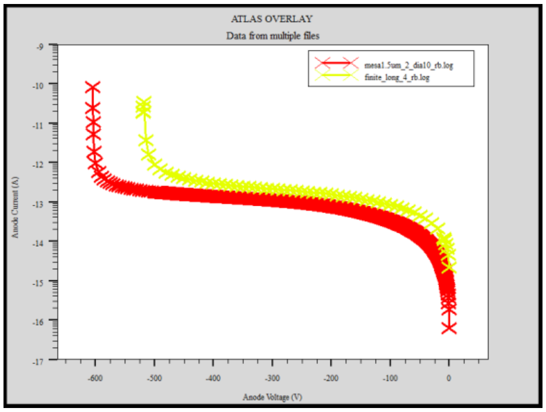


Figure 5-9: I-V comparing the breakdown voltage of a mesa diode(red) and a planar diode(yellow)

In the next step, a 600nm thick SiN_x was deposited using PECVD on the previously tested diodes with mesa. Then windows were opened on top of mesa to probe the Schottky contact. The I-V for SiNx deposited mesa diode was tested and compared to prior mesa diode with out SiNx. Figure 5-4 shows the I-V for 100 μm radius mesa diode with and without SiNx layer. After, SiNx deposition the current density increased by almost 3 and 4 orders of magnitude in reverse and forward bias respectively.

The similar increase in current density was observed in HVPE diodes in the previous chapter and was imputed due conducting path along the defect GaN and SiNx. But, it was not well understood if the defects were etch induced or due additional bulk defects that were reaveled after etch. In the current case, it was already established that etching was not affecting the surface properties, instead mesa diodes showed improvement in the breakdown voltage compared to normal diode (see figure 5-6). Next feasible factor based on HVPE diodes, was with etching the defective underneath HVPE layers are exposed that aid in extra conduction through the etched GaN and SiNx interface[84]. As, there was an obvious increase in leakage currents in wrap around compared to field plate, as wrap around geometry reveals the deeper defective layers. However, in MOCVD diodes, the reverse leakage current densities were found to be similar in a standard field plate and a wraparound diode (refer to figure 5-5) implying the absence of defective layer at the epi substrate layer interface. Also, the MOCVD layer is grown on homogeneous bulk Ammono GaN substrate as opposed to HVPE films grown on heterosubstrates with different lattice parameters. So, it is evident that neither etching nor defective layers are responsible for leakage currents in the diodes with SiNx.

In mesa diodes without SiNx, at the breakdown visible dark spots appeared at the edges, and beyond this voltage the currents are higher than compliance of the source meter and the voltage jumps to lower values. However, in diodes with SiNx layers there weren't any signs of dark spots appearing even though the current densities are beyond 100 mA/cm^2. From the figure 5-10, blue trace corresponds to mesa without SiNx and at 410V, a dark spot is observed indicating breakdown point and these marks are absent in the diode with the SiNx layer, indicating that diode is not blocking the voltage instead passing the excess currents through the interface.

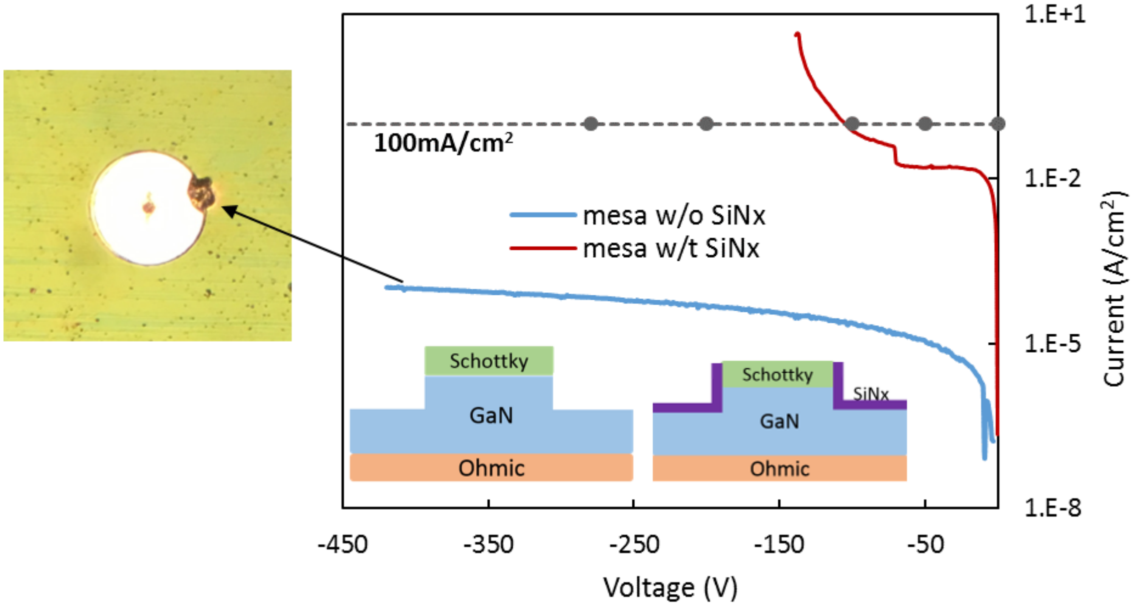


Figure 5-10: Reverse bias characteristics for a mesa diode with(blue) and without(red) SiNx layer. Dotted horizontal trace corresponds to current density at which diodes breakdown is defined.

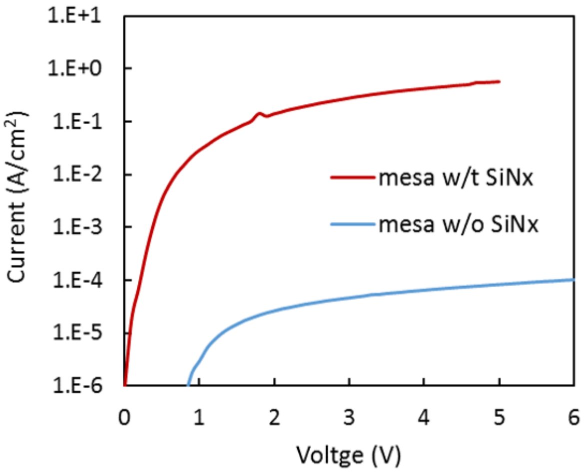


Figure 5-11: Forward I-V for a mesa diode at room temperature, with and without SiNx layer

Figure 5-11 shows the forward I-V for mesa diode with and without SiNx, and a similar increase in on current density is observed in diodes with SiNx. The is analogous to the results obtained in HVPE diodes.

In literature, saitoh et al., have reported most efficient vertical diodes in terms of low on resistance and high breakdown values using 1 μm thick PECVD SiNx along with field plate[53]. However, according to B. Luo et al., PECVD of SiNx passivation layers were reported to have a profound effect on the I–V characteristics of GaN Schottky rectifiers. They observed a decrease in reverse breakdown voltage and an in increase the forward leakage currents. This degradation in the diode performance was attributed to preferential loss of nitrogen from the GaN surface and ion damage. At higher deposition pressures, hydrogen reacts with nitrogen leaving behind nitrogen vacancies (N_V).

$GaN + H^0 \longrightarrow NH_3 + GaN + N_V$

Nitrogen vacancies have shallow donor states in the GaN band gap. The increased n-type doping near the surface would produce surface-initiated breakdown at lower biases than in stoichiometric material. During the thicker layer deposition of SiN_X, GaN surface is exposed to the ion flux and atomic hydrogen neutral flux, for a relatively longer time hence result in degradation of the GaN surface[85].

There are various reports evaluating the properties of dielectrics for GaN, some reported the interface state density between GaN and SiO_2 is 3 orders higher than GaN and SiNx[34], while others reported converse. Since, GaN do not have native oxide; despite of uncertainty in the dielectric layer, SiN_x and SiO_2 are prevalently used to passivate the surface. Lately, the device community started exploring different deposition methods such as sputter deposition of SiNx instead of PECVD[86], N2 plasma pretreatment before SiN deposition[87], low pressure chemical vapor deposition[88], in situ MOCVD growth of SiNx layers[89, 90], spin on glass (SOG) and SiO_2 bilayer[91]. Reduction of interface states is particularly important in Gan/AlGaN layers that are widely used in HEMTs, as SiNx deposited using PECVD is reported to interfere with the carrier mobilities in 2 DEG channel with high energy flux penetrating to bulk during deposition and scatter the electrons. To avoid this kind of carrier scattering, atomic layer deposition (ALD) of higher K dielectric materials such as HfO2, CeO2 are deposited prior to PECVD deposition of SiNx or SiO_2 is developed.

Dielectric material used	Deposition type
SiNx	ALD, InSitu, MOCVD, LPCVD
SiO_2	ALD, MOCVD, LPCVD
Al_2O_3	ALD
SOG / SiO_2	Not available
CeO_2/SiO_2	MOCVD

Available resources	
SiNx	Sputtering PECVD
SiO_2	Sputtering PECVD
Al_2O_3	Sputtering/ALD
TiO_2	ALD
ZnO	ALD

Table 5-2: Dielectric materials and deposition type used in literature(left) currently available resources(right)

In our case diodes built on both HVPE films and MOCVD films deteriorated by channeling parasitic currents across the GaN and SiNx after PECVD deposition. So, we adapted a similar deposition method used in HEMTs, i.e., depositing an ALD passivation layer prior to PECVD deposition of SiNx. Initially a 10-nm thick Al2O3, a high k dielectric was deposited using TMA (Aluminum source) and Ozone (oxygen source) at 350^0C in 135 cycles on mesa diodes. Followed by deposition of 650nm thick SiNx, using NH_3(20 sccm), N_2 (600 sccm) and 5% SiH_4/Ar (400 sccm) gases at 350^0C. For Al_2O_3 deposition, Ozone was used instead of commonly used H2O as oxygen source, as H from H2O will interact with the GaN surface and result in nitrogen vacancies as described above that again support surface leakage currents[92]

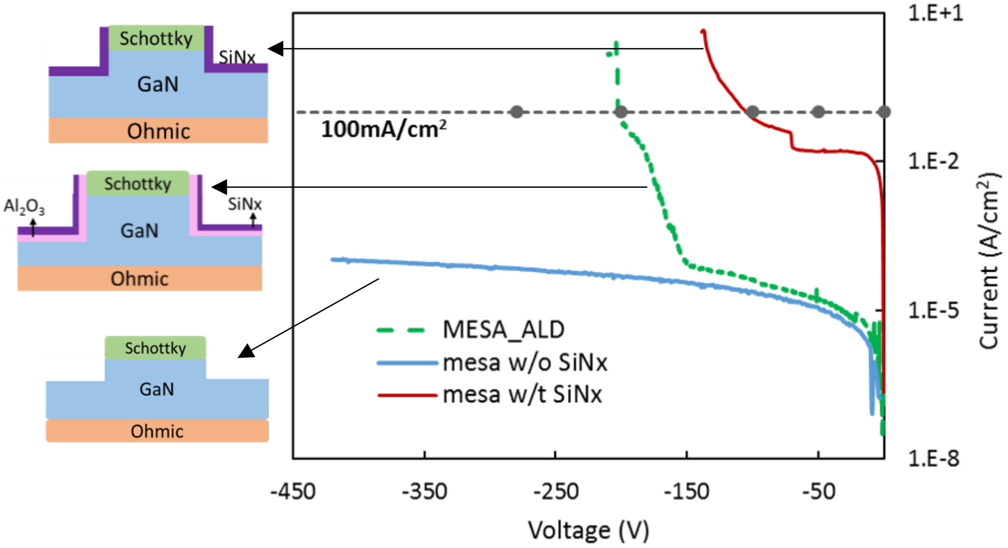
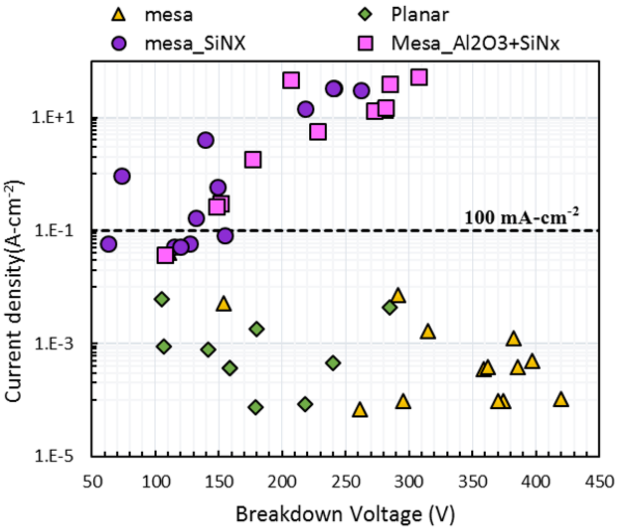


Figure 5-12: Comparing reverse bias I-V for mesa diode with different surface passivation

Mesa diodes with bilayer passivation (Al_2O_3+SiN_x) were then tested and compared to mesa diodes with and without SiNx. Figure 5-12 illustrates the I-V for mesa diodes with three different surface passivation. The additional Al_2O_3 have substantially restored the current density in the reverse bias similar to standalone mesa diode up to 150V and beyond this voltage the leakage current again increased resulting in breakdown. The breakdown values of mesa diodes after Al_2O_3 varied from 150V to 307V. The breakdown values are still below the mesa diodes without surface passivation. Figure 5-13, shows the overall breakdown values and respective breakdown currents for mesa diodes different surface passivation and planar diodes(green). In the forward bias, current densities are reduced compared to mesa diodes with SiNx, as the additional conducting paths along the interface no longer exist (see figure 5-14).



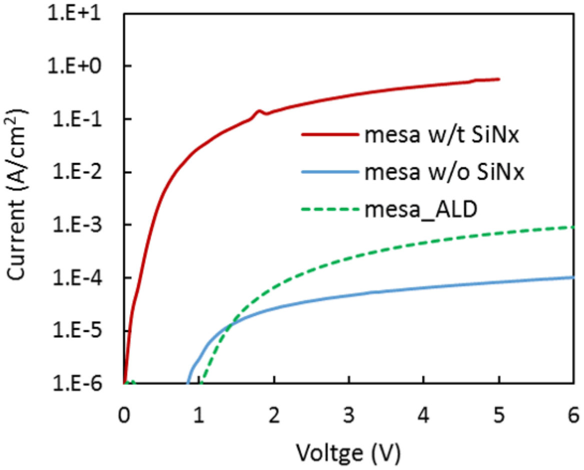


Figure 5-13: Reverse bias current density Vs. breakdown voltages for mesa diodes with different passivation and a planar diode

Figure 5-14: Comparing forward bias I-V for mesa diode with different surface passivation

Further to understand the impact of Al2O3 passivation layers on wrap around diodes, a bilayer dielectric was implemented in wrap around diodes as well. Wraparound diodes also showed

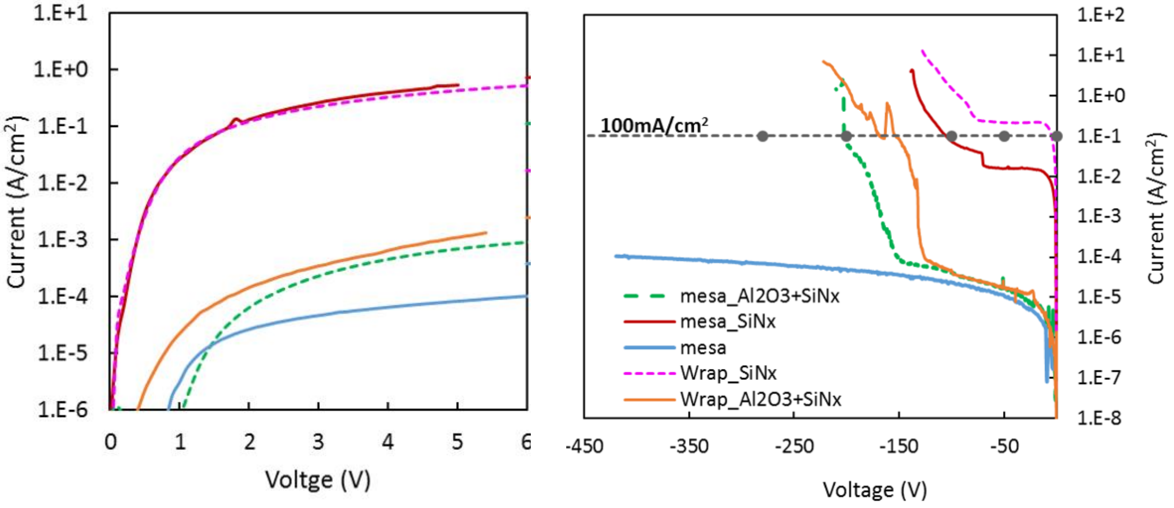


Figure 5-15: I-V characteristics of a mesa and a wraparound diode with SiNx and with Al2O3 & SiNx

improvement like mesa diodes. In the reverse bias, among wrap around and mesa diodes with SiNx, wrap around showed higher leakage current >1E-1. Interestingly, in case of Al2O3 bilayer passivation, wrap around and mesa showed similar leakage current densities on the order of 1E-5 unlike the SiNx passivated ones.

In a normal diode without any surface passivation or field plate, the current in the reverse bias is mainly due to transport of current over the metal semiconductor barrier height. In wide bandgap semiconductors as the reverse bias increases, due to imaging force, barrier lowers at the junction resulting in increased leakage currents at the higher bias.

In case of diodes with PECVD deposited SiNx, due to the creation of extra interface states during the deposition as discussed earlier results in higher leakage currents along the interface. However, there is a difference in a mesa and wraparound diode. This variation could be due to the wrap around field plate structure, which on top of mesa acts like a simple metal semiconductor junction and on the side walls with the dielectric and field plate combination, results in a metal insulator semiconductor structure(MOS). In SiNx diodes along with thermionic current transport across the barrier height, due to Frenkel Poole emissions along high-density interface states electrons might tunnel through the dielectric resulting in higher leakage currents in wrap around compared to mesa with SiNx.

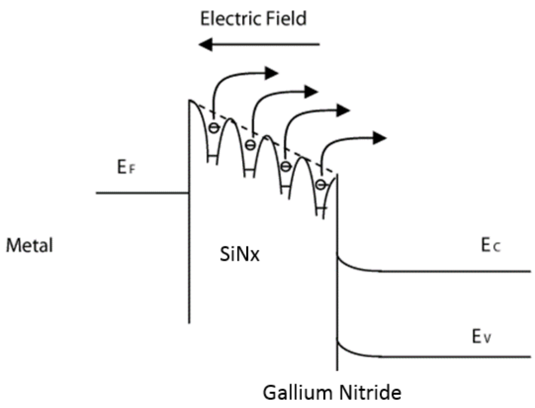


Figure 5-16:Tunneling currents across the gate, SiNx and GaN interface

In the case of Al2O3 passivation, according to literature depending on the surface cleaning prior to deposition of Al2O3 and depending on the deposition techniques different interface density state (D_{it}) across the GaN and Al2O3 are reported. For instance HCl cleaning of the surface prior to ALD deposition of Al2O3 results in a interface states density of 4 -9 x10^{11} $cm^{-2}eV^{-1}$ near mid bandgap[93]. In our case we didn't evaluate the interface density, but based on the surface treatments and deposition method we expect a similar D_{it} in these diodes resulting in a higher leakage currents at bias >100V and resulting in a premature breakdown of the diode.

Figure 5-17 summarizes the breakdown voltage for all the diodes and the corresponding current densities at the breakdown (not the leakage current density).

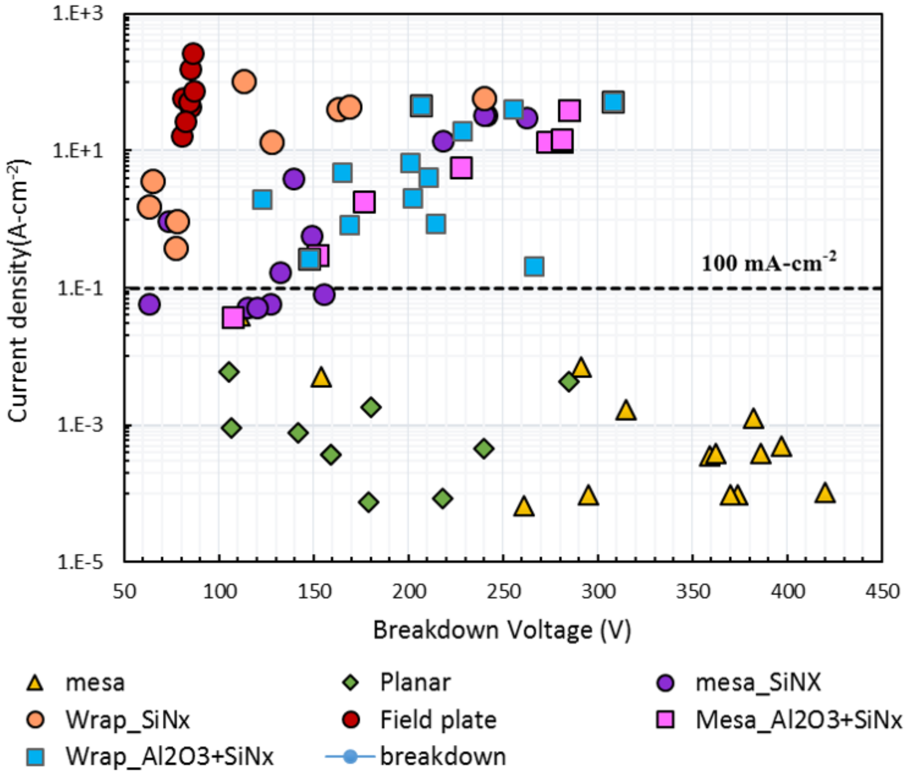


Figure 5-17: Current density for all diodes and corresponding breakdown values

So, far the emphasis was mainly on breakdown voltages and the leakage current densities. For an ideal diode it is not only important to have higher breakdown voltage, but it should also offer less resistance in the forward bias to minimize the conduction losses. For a Schottky diode, the turn on voltage is the sum of built in potential across the metal semiconductor junction, potential drop across the drift layer and contact.

$$\mathrm{V_F} = \mathrm{V_{FS}} + \mathrm{R_{S,SP}J_F}$$

$$\mathrm{R_{S,SP}} = R_{ON} = \mathrm{R_{epi}} + \mathrm{R_{sub}} + \mathrm{R_C}$$

$$\mathrm{R_{epi}} = \frac{4\,\mathrm{V_{BD}^2}}{\varepsilon_S \mu_n \mathrm{E_C^3}}$$

$$\mathrm{R_{sub}} = \rho_{\mathrm{sub}} * \mathrm{d}$$

Material parameter		**Values provided by wafer manufacturer**
Substrate thickness	d	350 µm
Dielectric constant	ε_S	8.9 F/cm
Mobility	μ_n	180 cm^2/V-s
Critical Electric field	E_C	1.1 MV/cm [94]
Substrate resistivity	ρ_{sub}	10^{-3} Ωcm
Carbon concentration		1.8 x 10^{17}cm^{-3}
Oxygen concentration		9 x 10^{15} cm^{-3}
Net doping	N_D	~ 5.5 x 10^{16} cm^{-3}

Table 5-3 : MOCVD grown epilayer and Ammono bulk substrate properties provided by the manufacturing company

MOCVD films have relatively high impurity concentration compared to the material used in most of the diodes reported in the literature. As a result, the mobility value was lower than the theoretically predicted value. Also, the critical electric field value of 1.1 MV/cm is adapted from literature based on the carrier concentration, which is also again low compared to the theoretical value. By plugging in these values in the above equations Ron was obtained by adding the epilayer resistance the substrate resistance and contact resistance is neglected. Figure 5-18 shows the on-resistance Vs breakdown for various diodes reported in the literature and the diodes with best performance obtained in this work.

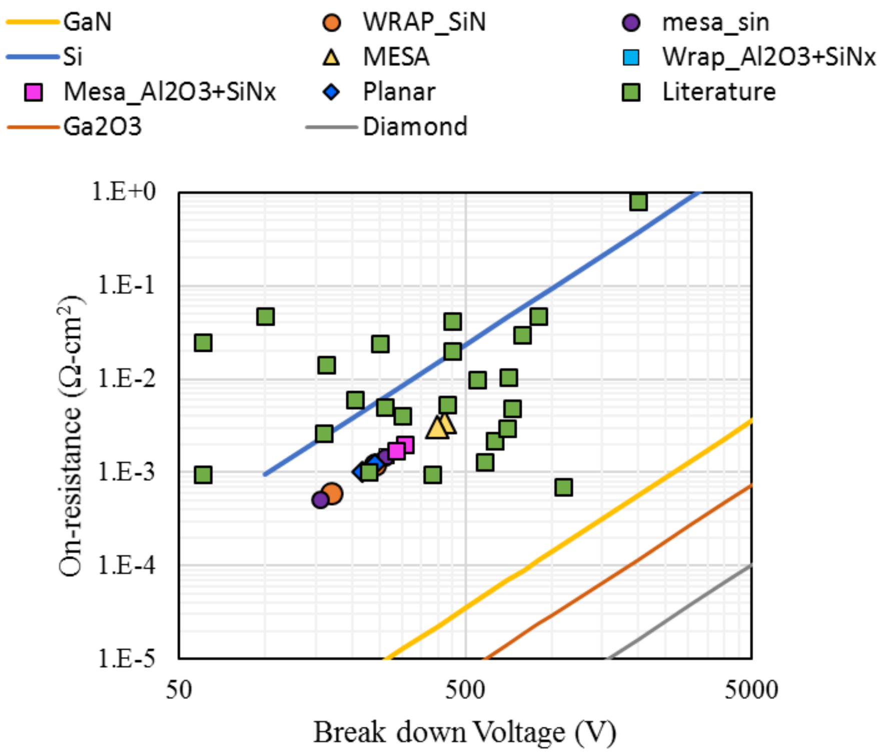


Figure 5-18: On resistance Vs breakdown voltage of the diodes in the literature and for the diodes from the current work.

Some of the diodes have superior Ron values and some have higher breakdown voltage than diodes from this work. Even though, the diodes from this work have lower breakdown voltages, it is interesting to note that compared to planar diode with a normal Schottky contact, diodes with field termination architectures improved the breakdown. The improvement in breakdown is obvious with the mesa. In case of mesa and wraparound with Al2O3+SiNx passivation, even though diodes have higher leakage currents, the best devices showed improved breakdown and Ron compared to planar, demonstrating the impact of the field termination geometry on the diode performance. However, compared to the best diodes from this work, some of the diodes reported in literature have higher breakdown and on-resistance values. To evaluate the scope for further improvement of the present work, the diodes with higher breakdown values along with the diodes from this work are plotted on breakdown voltage vs carrier concentration as shown in figure 5-17. Data points in red represent the diodes from literature (circles correspond to diodes built from MOCVD layers square represents a MOCVPE epilayer and triangles correspond to thick HVPE bulk substrates), and yellow points refer to the diodes from this work (circle represents a planar diode and square corresponds to mesa diode). The corresponding epi layers thickness used in each kind of diodes is labeled next to the data point. Diodes on bulk HVPE substrates have carrier concentration 10^{15} -10^{16} cm^{-3} and the thickness of these substrates varied from 350μm to 500μm. The diodes on MOCVD and MOVPE layers have carrier concentration 5 x 10^{15} and 1.1 x10^{16} cm^{-3} and with drift layers of 5μm and 13μm thick. In all these diodes, drift regions have lower doping concentration than the mocvd layers used in the current work whose net doping is 5.5 x 10^{16} cm^{-3}. There are a couple of data points in red in extreme right which again correspond to MOCVD layers but with doping concentration on the order of 7 x 10^{16} cm^{-3}, and these diodes used a field termination on a 7μm drift layers resulting in breakdown of 430V and 203V. Based on the material properties, the diodes from the current work are comparable to other diodes in the literature.

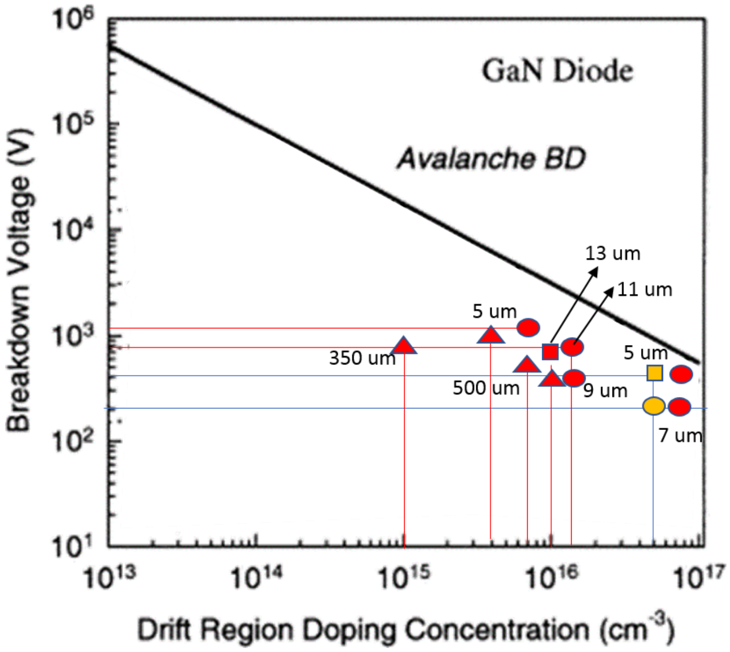


Figure 5-19: Breakdown voltage Vs. doping concentration for diodes reported in literature(red) and the diodes from this work(yellow).

The normal diode with 100 μm radius showed a breakdown voltage of only 240V and diode with the mesa geometry showed breakdown of 421V. The novel wrap around theoretically showed higher breakdown than a mesa diode. However, the physical device with a bilayer passivation showed a highest breakdown of only 307V.This value is still lower than the mesa diodes, indicating development of better surface passivation layer to reduce the leakage currents in wraparound diode

5.6 Conclusion

In this chapter, Schottky diodes are built from drift layers grown by MOCVD on Ammono substrates for the first time. Dry etching is optimized and resulted in relatively smoother side walls compared to HVPE diodes. Different device geometries including a normal diode without surface passivation or field termination, diode with mesa, a standard field plate and a wraparound field plate are studied. The impact of factors such as etching, defective interface layer was studied by measuring the diode I-V after each fabrication process. Leakage currents across the SiNx and GaN were found to be dominant even in diodes made on less defective MOCVD layers. A bilayer dielectric was used to reduce the leakage currents, which efficiently suppressed the leakage currents at lower voltage. However, at higher voltages an increase in leakage currents are again observed. Among the three edge terminations, the mesa without any surface passivation resulted in highest breakdown voltage of 421V. Surface passivation through any kind of dielectric deposition lowers the performance of the diode. Further, the breakdown and on-resistance for the best diodes obtained in this work are compared to the diodes in literature and found that the diodes studied here have lower figure of merit compared to some diodes. Later, analysis based on the drift layer doping showed that the diodes studied here have lower breakdown values due to higher impurity concentration

CHAPTER 6 CONCLUSION

From this work, we can conclude that GaN devices have potential to replace Si based devices, however there are some challenges that are to be addressed to utilize the GaN material to its complete potential. This work was specifically focused on optimization of device geometry to improve the Schottky diode figure of merit in terms of breakdown voltage and on-resistance, so that GaN devices can potentially be used for electric vehicle applications. And following list summarizes the main takeaways from this work.

- A new wraparound field plate design for Schottky diodes that passivates the high intensity electric fields which arise at the edges of the Schottky contact in the reverse bias was developed. If the field crowding at the contact periphery not addressed, it will impair the breakdown characteristics of diodes by lowering breakdown voltages. Therefore, with the new wraparound design, the electric field across the device active area was uniformly distributed close to an ideal diode which acts like a capacitor with infinitely long contacts.
- Initially, an optimized wraparound field plate was developed by varying the device dimensions in terms on epilayer thickness, dielectric thickness and mesa thickness using

silvaco tools. Schottky diodes with breakdown voltage between 400V to 2000V were simulated. Further, the electric field distribution in wraparound field plate device was compared to ideal diode and a standard field plate. Simulation results showed that wraparound geometry was efficient in distributing the electric fields uniformly across the device by confining high intensity fields in the dielectric layers. Also, the breakdown voltage of wraparound(1400V) was higher than a standard field plate(1230V).

- Later, Schottky diodes with wraparound field plate and a standard field plate were fabricated on suboptimum, low cost HVPE films to develop and optimize the fabrication processes including dry etching, dielectric deposition, ohmic contact deposition and annealing and Schottky contact deposition.

Further, the impact of two field plate structures on the Schottky diode were tested in terms of breakdown voltage and on-resistance. Diodes with standard field plate exhibited higher breakdown values compared to the wraparound design contradicting the simulation results. To understand the discrepancy between the simulation and experimental results, the on-resistance vs breakdown for all the Schottky diodes were compared. It was found that though diodes with the field plate have higher breakdown voltages, their on-resistance values were almost an order higher to wraparound diodes. To investigate this variation, Schottky diodes were further tested to estimate the impact of etching and dielectric deposition on diode performance. It was found that for wraparound geometry, in HVPE films with the etching defective layers closer to the interface are exposed and have lower resistance compared to the surface. A similar transformation in the quality film was reported earlier in literature for HVPE films of 8 to 10 μm thick, when etched half way through to 4 to 5μm deep. However, in the current work, HVPE films with 5±1 μm were used and a significant variation in the resistance was observed with just a few nanometers etching down from the surface.

Further, we found that the PECVD deposited SiNx on these etched surfaces allows flow of additional currents along these defective layers and SiNx interface resulting in high current densities and low breakdown voltage in wraparound design. Then, surface defects that were either generated during dry etching or due to exposed deeper layers closer to interface in wrapround diodes were passivated using ammonium sulphide. Optical characterization using PL spectroscopy showed a clear difference between passivated and unpassivated samples. However, the electrical characterization of the wraparound diodes did not a similar increment in the breakdown voltages. Instead, a minor variation in the leakage current densities was noticed. The average leakage current densities for wrapround diodes with 25μm, 50μm and 100μm radius for both passivated and Unpassivated were then extracted from reverse I-V and compared. It was found that with the decrease in diode radius, the leakage current density decreased in passivated samples, indicating that as surface to volume decrease, the impact surface states becomes significant along with bulk defects. In diodes with large radius, the intrinsic bulk defects are the main source of leakage currents. These bulk defects and surface defects therefore lower the impact of device geometry on diode performance. Later, to estimate the impact our novel wraparound field plate structure, MOCVD grown epilayer on bulk Ammono thermal substrate was used.

- For the first time, a less defective 5μm thick MOCVD grown film on Ammono bulk substrates were used to fabricate vertical Schottky diodes in this study. Initially, a planar Schottky diode and Schottky diodes with a standard field plate and a wraparound field plate were built and tested. It was found that both field plate structures showed a similar breakdown voltage and on resistance range, unlike diodes made on HVPE films. However, planar diodes with no additional geometric modification and dielectric passivation and a simple Schottky contact showed a higher breakdown compared to other Schottky diodes that employed field termination structures.

Device failure analysis based on I-V measurements after each fabrication process was carried out. After the initial mesa structure formation step involved in wraparound fabrication process, the break down voltages improved without impacting on-characteristics of a diode prior to etching. Indicating that altering the diode geometry aids in improved electric field distribution and further improving the breakdown characteristics of the diode. Later, SiN_x was deposited on these diodes with mesa diodes, 3 to 4 orders increase in current densities in both forward and reverse bias was observed. This indicated that PECVD deposited SiN_x resulted in additional leakage currents in field plate diodes. There by revoking the improvement caused by geometrical modeling of the device.

Therefore, to passivate the parasitic currents that arise due to PECVD deposition of SiN_x, a bilayer dielectric layer was developed by depositing an additional 10nm thick high K dielectric layer i.e., Al_2O_3 using ALD prior to SiN_x deposition. The new bilayer dielectric layer has significantly lowered the leakage currents across the SiNx and GaN interface and have improved the breakdown voltage value. However, we noticed that a standalone mesa diode without dielectric passivation have resulted in higher improvement in diode performance in terms on breakdown voltage compared to SiN_x or $Al_2O_3/SiN_{x.}$

- We then compared Schottky diodes with mesa to the literature data points and found that for the given epilayer specifications such as epilayer thickness, net carrier concentration and background impurity concentration, breakdown values achieved was either comparable or higher than most of the diodes reported in literature. However, there are few Schottky diodes that have higher figure of merit compare to diodes from current work. This higher performance in these diodes was possible because most of these diodes either HVPE bulk substrates that are almost 60 to 100 times thicker than epilayers used in this study. Also, HVPE films have the advantage of lower carbon doping compared to MOCVD as there is no use of TMGa which is the main source of carbon contamination in MOCVD films.

CHAPTER 7 FUTURE WORK

From the previous chapter, it is evident that to develop Schottky diodes with ideal figure of merit in future, it is essential to address following factors in future.

- **Home grown GaN substrates with lower defects and contamination**: From the previous chapters, it is evident that the substrates that were purchased from various vendors either have high carbon background impurities (MOCVD) or high defect densities (HVPE) compared to the drift regions of the diodes reported in literature with higher performance. It is therefore, important to improve the quality of the epilayers by reducing the background impurity concentrations and defects. With the current growth capabilities that are available, we should focus on home grown epilayers and test them for power applications
- **To develop alternative fabrication processes to reduce the process induced defects**: SiNx deposited using PECVD resulted in high leakage currents across the interface due to modification of surface when exposed to plasma during deposition. Later, a less damaging ALD was employed to deposit 10nm thick Al2O3. This suppressed leakage currents until 100 -150V, and at higher bias tunneling across the dielectric layers increased resulting in breakdown at voltages lower than the diode without a surface passivation. In future, it is critical to adapt alternative deposition technique such as LPCVD or in situ MOCVD that are less destructive compared to PECVD to deposit SiNx. Other possibility is to deposit thicker

Al2O3 layers using ALD on GaN and test if thicker layers can with stand higher voltage using MIS structures instead of fabricating complete diode.

- **To deposit and test alternative dielectric materials**: Specifically, for field plate geometries with a MOS structure tunneling currents at higher bias will deter the device performance. Thus, there is a need to do a systematic c-v characterization of dielectric and GaN interfaces properties and explore other dielectric materials beyond SiNx and SiO2 as shown in figure 6-1. Study based on C-V measurements to estimate the interface state density between dielectric materials and GaN is crucial to develop MISFETs that can operate at higher temperature and voltages without any parasitic currents for stable operation.

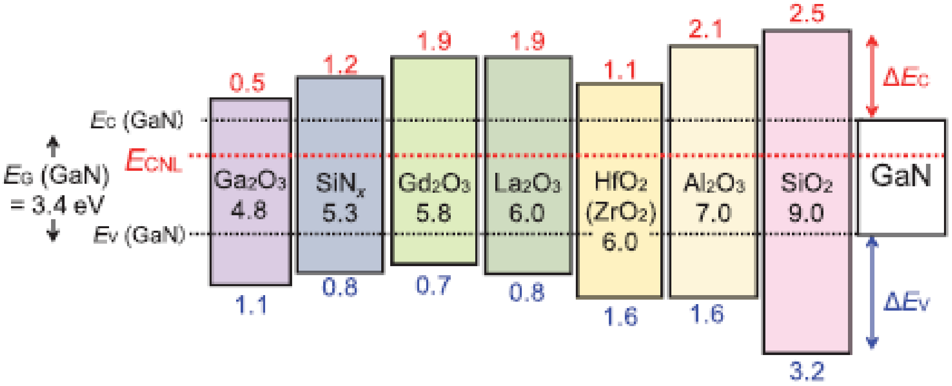


Figure 7-1: Dielectric materials and the energy gaps between their conduction band with respect to GaN [95]

- **Testing the efficiency of the wrap around field plate on bulk HVPE diodes**: Following the dielectric material and deposition optimization. Implement the wrap around field plate on bulk HVPE to evaluate the efficiency of novel field plate on the diode breakdown characteristics.

- **To perform a high temperature I-V testing**: Most of this work was focused on improving the operating voltage of the diode. It is also important to test stability of diode at higher temperature for practical applications.

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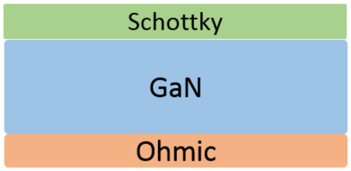
APPENDIX: A

Devedit code used for ideal diode, standard diode and different field plate architectures that are discussed in chapter 3

1. Ideal diode with infinitely long contacts

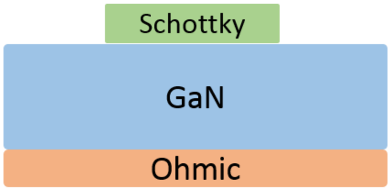


```
go atlas
## Material thickness ##
set sub_th=-5
set buf_th=-2
set epi_th=-5
set anode_th=-1
set cathode_th=1
set start_anode=0
set end_anode=74
################ dimensions_substarte ##################
set x0=$start_width
set y0=$start_width
set x1=$end_width
set y1=$start_width
set x2=$end_width
set y2=$sub_th
set x3=$start_width
set y3=$sub_th
################### dimentions_ buffer ##################
set x4=$start_width
set y4=$sub_th
set x5=$end_width
set y5=$sub_th
set x6=$end_width
set y6=$sub_th+$buf_th
set x7=$start_width
set y7=$sub_th+$buf_th
###################dimensions_epitaxy  ##################
set x8=$start_width
set y8=$sub_th+$buf_th
set x9=$end_width
set y9=$sub_th+$buf_th
set x10=$end_width
set y10=$sub_th+$buf_th+$epi_th
set x11=$start_width
set y11=$sub_th+$buf_th+$epi_th
########### anode #############
set x41=$start_anode
set y41=$sub_th+$buf_th+$epi_th
set x42=$end_anode
set y42=$sub_th+$buf_th+$epi_th
set x43=$end_anode
set y43=$sub_th+$buf_th+$epi_th+$anode_th
set x44=$start_anode
set y44=$sub_th+$buf_th+$epi_th+$anode_th
set light=5e-5
```

```
set GaN_Eg=3.42
set GaN_diel=8.9
set GaN_Emob=1000*0.525
set GaN_Pmob=10
set GaN_satvel=1.125e7
set GaN_peak_vel=2.2e7
set GaN_intris_conc=2.9e-9
set GaN_Nc300=2.3e18
set GaN_Nv300=4.6e19
set GaN_Eab=0.175
set GaN_Edb=0.016
set GaN_taun=1e-9
set GaN_taup=1e-9
set GaN_Ec=3.75e6
set GaN_lattice=3.189

set simrun=infinite_long

#### dev edit ######
go devedit
region id=1 name=substrate material=GaN points="$x0,$y0 $x1,$y1 $x2,$y2
$x3,$y3 $x0,$y0"
impurity id=1 region.id=1 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply

region id=2 name=buffer material=GaN points="$x4,$y4 $x5,$y5 $x6,$y6
$x7,$y7 $x4,$y4"
impurity id=1 region.id=2 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply

region id=3 name=epitaxy material=GaN points="$x8,$y8 $x9,$y9 $x10,$y10
$x11,$y11 $x12,$y12 $x13,$y13 $x14,$y14 $x15,$y15 $x8,$y8"
impurity id=1 region.id=3 impurity=donors peak.value=5.e15
ref.value=1e12 comb.function=multiply

region id=6 name=cathode material=contact  elec.id=1
points="$start_width,$start_width $end_width,$start_width
$end_width,$cathode_th $start_width,$cathode_th
$start_width,$start_width"

region id=7 name=anode material=contact  elec.id=2  points="$x41,$y41
$x42,$y42 $x43,$y43 $x44,$y44 $x41,$y41"

## base mesh ##
base.mesh height=0.5 width=0.5
bound.cond max.slope=28 max.ratio=300 rnd.unit=0.01
line.straightening=1 align.points when=automatic
## global constraint##
constr.mesh material.type=semiconductor max.angle= 90 max.ratio=100
max.width=1 max.height=1 min.height=0.01 min.width=0.01
constr.mesh x1=$start_width y1=$start_width x2=$end_width y2=$sub_th
default max.height=1 max.width=1
structure outfile=$"simrun"_init.str
tonyplot $"simrun"_init.str
go atlas
region number=1 material=GaN substrate modify
region number=2 material=GaN modify
```

```
region number=3 material=GaN modify

material material=GaN real.index=2.67 imag.index=0.001
vsatn=$GaN_satvel ni.min=$GaN_intris_conc eg300=$GaN_Eg taun0=$GaN_taun
taup0=$GaN_taup mun0=$GaN_Emob mup0=$GaN_Pmob ALATTICE=$GaN_lattice
permittivity=$GaN_diel nc300=$GaN_Nc300 nv300=$GaN_Nv300 edb=$GaN_Edb
eab=$GaN_Eab

model fermi conmob fldmob srh auger bgn ten. polar print
impact selb material=GaN
beam number=1 x.o=0 y.o=-24 angle=90 min.window=$start_width
max.window=$end_width  wavelength=0.3

Output con.band val.band charge e.field ex.field ey.field devdeg
polar.charge traps Schottky flowlines
contact name=anode workf=5.3
method newton trap maxtrap=30 carriers=2
solve init
solve b1=$light index.check
solve vanode=0 vcathode=0 b1=$light
save outfile=$"simrun"_0bias.str
log outfile=$"simrun"_fb.log
solve vanode=0.05  vstep=.1  vfinal=2  name=anode b1=$light
save outfile=$"simrun"_fb.str
log off
log outfile=$"simrun"_rb.log
solve vanode=-0.001  vstep=-2  vfinal=-700  name=anode b1=$light
solve vanode=-700 vstep=-5 vfinal=-1300  name=anode b1=$light
cname=anode compl=-6e-11
solve vanode=-1300  vstep=-5 vfinal=-3000  name=anode b1=$light
cname=anode compl=-1e-13
save outfile=$"simrun"_vbd.str
log off
quit
```

2. Schottky diode with finite contact length



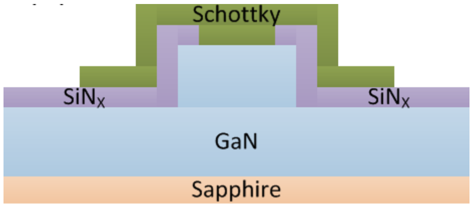
```
go atlas
## Material thickness ##
set sub_th=-5
set buf_th=-2
set epi_th=-5
set anode_th=-1
set cathode_th=1
set start_anode=30
set end_anode=44
set start_width=0
set end_width=74
################ dimensions_substarte ##################
set x0=$start_width
set y0=$start_width
set x1=$end_width
set y1=$start_width
set x2=$end_width
set y2=$sub_th
set x3=$start_width
```

```
set y3=$sub_th
################### dimentions_ buffer ###################
set x4=$start_width
set y4=$sub_th
set x5=$end_width
set y5=$sub_th
set x6=$end_width
set y6=$sub_th+$buf_th
set x7=$start_width
set y7=$sub_th+$buf_th
###################dimensions_epitaxy  ################
set x8=$start_width
set y8=$sub_th+$buf_th
set x9=$end_width
set y9=$sub_th+$buf_th
set x10=$end_width
set y10=$sub_th+$buf_th+$epi_th
set x11=$start_width
set y11=$sub_th+$buf_th+$epi_th
########### anode #############
set x41=$start_anode
set y41=$sub_th+$buf_th+$epi_th
set x42=$end_anode
set y42=$sub_th+$buf_th+$epi_th
set x43=$end_anode
set y43=$sub_th+$buf_th+$epi_th+$anode_th
set x44=$start_anode
set y44=$sub_th+$buf_th+$epi_th+$anode_th

set light=5e-5
set GaN_Eg=3.42
set GaN_diel=8.9
set GaN_Emob=1000*0.525
set GaN_Pmob=10
set GaN_satvel=1.125e7
set GaN_peak_vel=2.2e7
set GaN_intris_conc=2.9e-9
set GaN_Nc300=2.3e18
set GaN_Nv300=4.6e19
set GaN_Eab=0.175
set GaN_Edb=0.016
set GaN_taun=1e-9
set GaN_taup=1e-9
set GaN_Ec=3.75e6
set GaN_lattice=3.189
set simrun=finite_long

#### dev edit ######
go devedit
region id=1 name=substrate material=GaN points="$x0,$y0 $x1,$y1 $x2,$y2
$x3,$y3 $x0,$y0"
impurity id=1 region.id=1 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply

region id=2 name=buffer material=GaN points="$x4,$y4 $x5,$y5 $x6,$y6
$x7,$y7 $x4,$y4"
```

```
impurity id=1 region.id=2 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply

region id=3 name=epitaxy material=GaN points="$x8,$y8 $x9,$y9 $x10,$y10
$x11,$y11 $x8,$y8"
impurity id=1 region.id=3 impurity=donors peak.value=5.e15
ref.value=1e12 comb.function=multiply

region id=4 name=cathode material=contact  elec.id=1
points="$start_width,$start_width $end_width,$start_width
$end_width,$cathode_th $start_width,$cathode_th
$start_width,$start_width"
region id=5 name=anode material=contact  elec.id=2  points="$x41,$y41
$x42,$y42 $x43,$y43 $x44,$y44 $x41,$y41"
## base mesh ##
base.mesh height=0.5 width=0.5
bound.cond max.slope=28 max.ratio=300 rnd.unit=0.01
line.straightening=1 align.points when=automatic
## global constraint##
constr.mesh material.type=semiconductor max.angle= 90 max.ratio=100
max.width=1 max.height=1 min.height=0.01 min.width=0.01
constr.mesh x1=$start_width y1=$start_width x2=$end_width y2=$sub_th
default max.height=1 max.width=1
mesh
structure outfile=$"simrun"_init.str
tonyplot $"simrun"_init.str

go atlas
region number=1 material=GaN  substrate modify
region number=2 material=GaN  modify
region number=3 material=GaN  modify
material material=GaN real.index=2.67 imag.index=0.001
vsatn=$GaN_satvel ni.min=$GaN_intris_conc eg300=$GaN_Eg taun0=$GaN_taun
taup0=$GaN_taup mun0=$GaN_Emob mup0=$GaN_Pmob ALATTICE=$GaN_lattice
permittivity=$GaN_diel nc300=$GaN_Nc300 nv300=$GaN_Nv300 edb=$GaN_Edb
eab=$GaN_Eab
model  fermi  conmob  fldmob  srh  auger  bgn ten.polar print
impact selb material=GaN
beam number=1 x.o=0 y.o=-24 angle=90 min.window=$start_width
max.window=$end_width  wavelength=0.3
Output con.band val.band charge e.field ex.field ey.field devdeg
polar.charge traps Schottky flowlines
contact name=anode workf=5.3
method newton  trap maxtrap=30 carriers=2
solve init
solve b1=$light index.check
#solve vanode=0 vcathode=0 b1=$light
save outfile=$"simrun"_0bias.str
log off
log outfile=$"simrun"_rb.log
solve vanode=-0.001  vstep=-2  vfinal=-700  name=anode b1=$light
cname=anode compl=-6e-12
solve vanode=-700 vstep=-5 vfinal=-1300  name=anode b1=$light
cname=anode compl=-6e-11
solve vanode=-1300  vstep=-5 vfinal=-3000  name=anode b1=$light
cname=anode compl=-1e-13
save outfile=$"simrun"_vbd.str
```

```
log off
quit
```

3. Schottky diode with a wraparound filed plate



```
go atlas
## Material thickness ##
set sub_th=-1
set buf_th=-0.3
set epi_th=-5
set anode_th=-0.1
set cathode_th=0.1
set sin_th=-.05
set sin_m_th=-0.9
set sin_t_th=-.05
set sin_bk_th=-0.0

set start_anode_left_left=3
set start_anode_left=7.5
set end_anode_right=66.5
set end_anode_right_last=70.5
set start_cathode= 130
set end_width=150
set start_width=0
set end_sin_left=10
set start_sin_m_left=9.95
set start_sin_bk_left=7.5
set end_sin_t_left=25
set start_sin_right=64
set end_sin_m_right=64.05
set start_sin_t_right=49
set end_sin_bk_right=22.5
################# dimensions_substarte ##################
set x0=$start_width
set y0=$start_width
set x1=$end_width
set y1=$start_width
set x2=$end_width
set y2=$sub_th
set x3=$start_width
set y3=$sub_th
################### dimentions_ buffer ####################
set x4=$start_width
set y4=$sub_th
set x5=$end_width
set y5=$sub_th
set x6=$end_width
set y6=$sub_th+$buf_th
set x7=$start_width
set y7=$sub_th+$buf_th
###################dimensions_epitaxy  ###################
set x8=$start_width
set y8=$sub_th+$buf_th
set x9=$end_width
set y9=$sub_th+$buf_th
set x10=$end_width
```

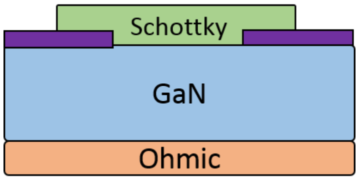
```
set y10=$sub_th+$buf_th+$epi_th
set x11=$start_sin_right
set y11=$sub_th+$buf_th+$epi_th
set x12=$start_sin_right
set y12=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x13=$end_sin_left
set y13=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x14=$end_sin_left
set y14=$sub_th+$buf_th+$epi_th
set x15=$start_width
set y15=$sub_th+$buf_th+$epi_th
################ SiN_Left ##############################
set x16=$start_width
set y16=$sub_th+$buf_th+$epi_th
set x17=$end_sin_left
set y17=$sub_th+$buf_th+$epi_th
set x18=$end_sin_left
set y18=$sub_th+$buf_th+$epi_th+$sin_th
set x19=$end_sin_left
set y19=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x20=$end_sin_t_left
set y20=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x21=$end_sin_t_left
set y21=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x22=$start_sin_m_left
set y22=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x23=$start_sin_m_left
set y23=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x24=$start_sin_m_left
set y24=$sub_th+$buf_th+$epi_th+$sin_th
set x25=$start_width
set y25=$sub_th+$buf_th+$epi_th+$sin_th
################ Sin_right ###################
set x26=$start_sin_right
set y26=$sub_th+$buf_th+$epi_th
set x27=$end_width
set y27=$sub_th+$buf_th+$epi_th
set x28=$end_width
set y28=$sub_th+$buf_th+$epi_th+$sin_th
set x29=$end_sin_m_right
set y29=$sub_th+$buf_th+$epi_th+$sin_th
set x30=$end_sin_m_right
set y30=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x31=$end_sin_m_right
set y31=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x32=$start_sin_t_right
set y32=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x33=$start_sin_t_right
set y33=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x34=$start_sin_right
set y34=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x35=$start_sin_right
set y35=$sub_th+$buf_th+$epi_th+$sin_th
set x36=$start_sin_right
set y36=$sub_th+$buf_th+$epi_th+$sin_th
########### anode #############
set x41=$start_anode_left_left
```

```
set y41=$sub_th+$buf_th+$epi_th+$sin_th
set x42=$start_anode_left_left
set y42=$sub_th+$buf_th+$epi_th+$sin_th+$anode_th
set x43=$start_anode_left
set y43=$sub_th+$buf_th+$epi_th+$sin_th+$anode_th
set x44=$start_anode_left
set
y44=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th+$anode_th+$anod
e_th
set x45=$end_anode_right
set
y45=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th+$anode_th+$anod
e_th
set x46=$end_anode_right
set y46=$sub_th+$buf_th+$epi_th+$sin_th+$anode_th
set x47=$end_anode_right_last
set y47=$sub_th+$buf_th+$epi_th+$sin_th+$anode_th
set x48=$end_anode_right_last
set y48=$sub_th+$buf_th+$epi_th+$sin_th
set x49=$end_sin_m_right
set y49=$sub_th+$buf_th+$epi_th+$sin_th
set x50=$end_sin_m_right
set y50=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x51=$end_sin_m_right
set y51=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x52=$start_sin_t_right
set y52=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x53=$start_sin_t_right
set y53=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x54=$end_sin_t_left
set y54=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x55=$end_sin_t_left
set y55=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x56=$start_sin_m_left
set y56=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th+$sin_t_th
set x57=$start_sin_m_left
set y57=$sub_th+$buf_th+$epi_th+$sin_th+$sin_m_th
set x58=$start_sin_m_left
set y58=$sub_th+$buf_th+$epi_th+$sin_th
###########cathode###############
set x60=$start_cathode
set y60=$sub_th+$buf_th+$epi_th+$sin_th
set x61=$end_width
set y61=$sub_th+$buf_th+$epi_th+$sin_th
set x62=$end_width
set y62=$sub_th+$buf_th+$epi_th+$sin_th+$cathode_th
set x63=$start_cathode
set y63=$sub_th+$buf_th+$epi_th+$sin_th+$cathode_th
set light=5e-5
set GaN_Eg=3.42
set GaN_diel=8.9
set GaN_Emob=1000*0.525
set GaN_Pmob=10
set GaN_satvel=1.125e7
set GaN_peak_vel=2.2e7
set GaN_intris_conc=2.9e-9
set GaN_Nc300=2.3e18
```

```
set GaN_Nv300=4.6e19
set GaN_Eab=0.175
set GaN_Edb=0.016
set GaN_taun=1e-9
set GaN_taup=1e-9
set GaN_Ec=3.75e6
set GaN_lattice=3.189
set simrun=capgate_epi5_sinb1.5_sinm0.5_sint1.5_sin15um_dia10
#### dev edit ######
go devedit
region id=1 name=substrate material=sapphire points="$x0,$y0 $x1,$y1
$x2,$y2 $x3,$y3 $x0,$y0"
impurity id=1 region.id=1 impurity=donors peak.value=5.e9
ref.value=1e12 comb.function=multiply
region id=2 name=buffer material=GaN points="$x4,$y4 $x5,$y5 $x6,$y6
$x7,$y7 $x4,$y4"
impurity id=1 region.id=2 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply

region id=3 name=epitaxy material=GaN points="$x8,$y8 $x9,$y9 $x10,$y10
$x11,$y11 $x12,$y12 $x13,$y13 $x14,$y14 $x15,$y15 $x8,$y8"
impurity id=1 region.id=3 impurity=donors peak.value=5.e15
ref.value=1e12 comb.function=multiply

region id=4 name=dielectric material=SiN points="$x26,$y26 $x27,$y27
$x28,$y28 $x29,$y29 $x30,$y30 $x31,$y31 $x32,$y32 $x33,$y33 $x34,$y34
$x35,$y35 $x36,$y36 $x26,$y26"

region id=5 name=dielectric material=SiN points="$x16,$y16 $x17,$y17
$x18,$y18 $x19,$y19 $x20,$y20 $x21,$y21 $x22,$y22 $x23,$y23 $x24,$y24
$x25,$y25 $x16,$y16"

region id=6 name=cathode material=contact  elec.id=1  points="$x60,$y60
$x61,$y61 $x62,$y62 $x63,$y63 $x60,$y60"
region id=7 name=anode material=contact  elec.id=2  points="$x41,$y41
$x42,$y42 $x43,$y43 $x44,$y44 $x45,$y45 $x46,$y46 $x47,$y47 $x48,$y48
$x49,$y49 $x50,$y50 $x51,$y51 $x52,$y52 $x53,$y53 $x54,$y54 $x55,$y55
$x56,$y56 $x57,$y57 $x58,$y58 $x41,$y41"

## base mesh ##
base.mesh height=0.5 width=0.5
bound.cond max.slope=28 max.ratio=300 rnd.unit=0.01
line.straightening=1 align.points when=automatic
## global constraint##
constr.mesh material.type=semiconductor max.angle= 90 max.ratio=100
max.width=1 max.height=1 min.height=0.01 min.width=0.01
constr.mesh x1=$start_width y1=$start_width x2=$end_width y2=$sub_th
default max.height=1 max.width=1
#### interface ####
set epi_top_y=$y10-0.1
set epi_bot_y=$y10+0.1
constr.mesh x1=$start_width y1=$epi_top_y x2=$end_width y2=$epi_bot_y
default max.height=0.1 max.width=0.1
set end_sin_left_x1=$x18-0.1
set end_sin_left_x2=$x18+0.1
constr.mesh x1=$end_sin_left_x1 y1=$y19 x2=$end_sin_left_x2 y2=$y17
max.height=0.1 max.width=0.1
```

```
set end_sin_left_x1=$x26-0.1
set end_sin_left_x2=$x26+0.1
constr.mesh x1=$end_sin_left_x1 y1=$y26 x2=$end_sin_left_x2 y2=$y34
max.height=0.1 max.width=0.1
set sin_m_top_y=$y19+0.1
set sin_m_bot_y=$y19-1
constr.mesh x1=$x19 y1=$sin_m_top_y x2=$x34 y2=$sin_m_bot_y
max.height=0.1 max.width=0.1
structure outfile=$"simrun"_init.str
tonyplot $"simrun"_init.str

go atlas
region number=1 material=Sapphire  substrate modify
region number=2 material=GaN  modify
region number=3 material=GaN  modify
material material=GaN real.index=2.67 imag.index=0.001
vsatn=$GaN_satvel ni.min=$GaN_intris_conc eg300=$GaN_Eg taun0=$GaN_taun
taup0=$GaN_taup mun0=$GaN_Emob mup0=$GaN_Pmob ALATTICE=$GaN_lattice
permittivity=$GaN_diel nc300=$GaN_Nc300 nv300=$GaN_Nv300 edb=$GaN_Edb
eab=$GaN_Eab
model  fermi  conmob  fldmob  srh  auger  bgn print
impact selb material=GaN
beam number=1 x.o=0 y.o=-24 angle=90 min.window=$start_width
max.window=$end_width  wavelength=0.3
Output con.band val.band charge e.field ex.field ey.field devdeg
polar.charge traps Schottky flowlines
contact name=anode workf=5.3
method newton  trap maxtrap=30 carriers=2
solve init
solve b1=$light index.check
solve vanode=0 vcathode=0 b1=$light
save outfile=$"simrun"_0bias.str
log outfile=$"simrun"_fb.log
solve vanode=0.05 vstep=.1  vfinal=2  name=anode b1=$light
save outfile=$"simrun"_fb.str
log off
log outfile=$"simrun"_rb.log
solve vanode=-0.001 vstep=-0.5 vfinal=-6000 name=anode b1=$light
cname=anode compl=-1e-12
save outfile=$"simrun"_vbd.str
log off
quit
```

4. Schottky diode with standard field plate



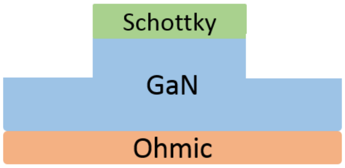
```
   go atlas
## Material thickness ##
set sub_th=-5
set buf_th=-2
set epi_th=-4
set anode_th=-1
set cathode_th=1
set sin_th=-0.5
set start_anode=0
set end_anode=21
set end_width=21
set start_width=0
```

```
set end_sin_left=6
set start_sin_right=15
################# dimensions_substarte ##################
set x0=$start_width
set y0=$start_width
set x1=$end_width
set y1=$start_width
set x2=$end_width
set y2=$sub_th
set x3=$start_width
set y3=$sub_th
################### dimentions_ buffer #################
set x4=$start_width
set y4=$sub_th
set x5=$end_width
set y5=$sub_th
set x6=$end_width
set y6=$sub_th+$buf_th
set x7=$start_width
set y7=$sub_th+$buf_th
###################dimensions_epitaxy  #################
set x8=$start_width
set y8=$sub_th+$buf_th
set x9=$end_width
set y9=$sub_th+$buf_th
set x10=$end_width
set y10=$sub_th+$buf_th+$epi_th
set x11=$start_width
set y11=$sub_th+$buf_th+$epi_th
################# SiN_Left #############################
set x12=$start_width
set y12=$sub_th+$buf_th+$epi_th
set x13=$end_sin_left
set y13=$sub_th+$buf_th+$epi_th
set x14=$end_sin_left
set y14=$sub_th+$buf_th+$epi_th+$sin_th
set x15=$start_width
set y15=$sub_th+$buf_th+$epi_th+$sin_th
################# Sin_right ###################
set x16=$start_sin_right
set y16=$sub_th+$buf_th+$epi_th
set x17=$end_width
set y17=$sub_th+$buf_th+$epi_th
set x18=$end_width
set y18=$sub_th+$buf_th+$epi_th+$sin_th
set x19=$start_sin_right
set y19=$sub_th+$buf_th+$epi_th+$sin_th
########### anode #############
set x20=$start_anode
set y20=$sub_th+$buf_th+$epi_th+$sin_th+$anode_th
set x21=$end_anode
set y21=$sub_th+$buf_th+$epi_th+$sin_th+$anode_th
set x22=$end_anode
set y22=$sub_th+$buf_th+$epi_th+$sin_th
set x23=$start_sin_right
set y23=$sub_th+$buf_th+$epi_th+$sin_th
set x24=$start_sin_right
```

```
set y24=$sub_th+$buf_th+$epi_th
set x25=$end_sin_left
set y25=$sub_th+$buf_th+$epi_th
set x26=$end_sin_left
set y26=$sub_th+$buf_th+$epi_th+$sin_th
set x27=$start_anode
set y27=$sub_th+$buf_th+$epi_th+$sin_th
set light=5e-5
set GaN_Eg=3.42
set GaN_diel=8.9
set GaN_Emob=1000*0.525
set GaN_Pmob=10
set GaN_satvel=1.125e7
set GaN_peak_vel=2.2e7
set GaN_intris_conc=2.9e-9
set GaN_Nc300=2.3e18
set GaN_Nv300=4.6e19
set GaN_Eab=0.175
set GaN_Edb=0.016
set GaN_taun=1e-9
set GaN_taup=1e-9
set GaN_Ec=3.75e6
set GaN_lattice=3.189
set simrun=basic_epi4_sin0.5_dia10_plate6
#### dev edit ######
go devedit
region id=1 name=substrate material=GaN points="$x0,$y0 $x1,$y1 $x2,$y2
$x3,$y3 $x0,$y0"
impurity id=1 region.id=1 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply
region id=2 name=buffer material=GaN points="$x4,$y4 $x5,$y5 $x6,$y6
$x7,$y7 $x4,$y4"
impurity id=1 region.id=2 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply
region id=3 name=epitaxy material=GaN points="$x8,$y8 $x9,$y9 $x10,$y10
$x11,$y11 $x8,$y8"
impurity id=1 region.id=3 impurity=donors peak.value=5.e15
ref.value=1e12 comb.function=multiply
region id=4 name=dielectric material=SiN points="$x12,$y12 $x13,$y13
$x14,$y14 $x15,$y15 $x12,$y12"
region id=5 name=dielectric material=SiN points="$x16,$y16 $x17,$y17
$x18,$y18 $x19,$y19 $x16,$y16"
region id=6 name=cathode material=contact  elec.id=1
points="$start_width,$start_width $end_width,$start_width
$end_width,$cathode_th $start_width,$cathode_th
$start_width,$start_width"
region id=7 name=anode material=contact  elec.id=2  points="$x20,$y20
$x21,$y21 $x22,$y22 $x23,$y23 $x24,$y24 $x25,$y25 $x26,$y26 $x27,$y27
$x20,$y20"
## base mesh ##
base.mesh height=0.5 width=0.5
bound.cond max.slope=28 max.ratio=300 rnd.unit=0.01
line.straightening=1 align.points when=automatic
## global constraint##
constr.mesh material.type=semiconductor max.angle= 90 max.ratio=100
max.width=1 max.height=1 min.height=0.01 min.width=0.01
```

```
constr.mesh x1=$start_width y1=$start_width x2=$end_width y2=$sub_th
default max.height=1 max.width=1
#### interface ####
set sub_top_y=$sub_th-0.5
set sub_bot_y=$sub_th+0.5
constr.mesh x1=$start_width y1=$sub_top_y x2=$end_width y2=$sub_bot_y
default max.height=0.1 max.width=0.1
constr.mesh x1=$start_width y1=$sub_bot_y x2=$end_width y2=$y6 default
max.height=0.25 max.width=0.25
set buf_top_y=$y6-0.5
set buf_bot_y=$y6+0.5
constr.mesh x1=$start_width y1=$buf_top_y x2=$end_width y2=$buf_bot_y
default max.height=0.2 max.width=0.2
constr.mesh x1=$start_width y1=$buf_bot_y x2=$end_width y2=$y10 default
max.height=0.2 max.width=0.2
set epi_top_y=$y10-0.1
set epi_bot_y=$y10+0.1
constr.mesh x1=$start_width y1=$epi_top_y x2=$end_width y2=$epi_bot_y
default max.height=0.05 max.width=0.05
mesh
structure outfile=$"simrun"_init.str
tonyplot $"simrun"_init.str
go atlas
region number=1 material=GaN  substrate modify
region number=2 material=GaN  modify
region number=3 material=GaN  modify
material material=GaN real.index=2.67 imag.index=0.001
vsatn=$GaN_satvel ni.min=$GaN_intris_conc eg300=$GaN_Eg taun0=$GaN_taun
taup0=$GaN_taup mun0=$GaN_Emob mup0=$GaN_Pmob ALATTICE=$GaN_lattice
permittivity=$GaN_diel nc300=$GaN_Nc300 nv300=$GaN_Nv300 edb=$GaN_Edb
eab=$GaN_Eab
model  fermi  conmob  fldmob  srh  auger  bgn ten.polar print
impact selb material=GaN
beam number=1 x.o=0 y.o=-20 angle=90 min.window=$start_width
max.window=$end_width  wavelength=0.3
Output con.band val.band charge e.field ex.field ey.field devdeg
polar.charge traps Schottky flowlines
contact name=anode workf=5.3
method newton  trap maxtrap=30 carriers=2
solve init
solve b1=$light index.check
solve vanode=0 vcathode=0 b1=$light
save outfile=$"simrun"_0bias.str
log outfile=$"simrun"_fb.log
solve vanode=0.05 vstep=.1 vfinal=4 name=anode b1=$light
save outfile=$"simrun"_fb.str
log off
log outfile=$"simrun"_rb.log
solve vanode=-0.001  vstep=-10 vfinal=-1000  name=anode b1=$light
cname=anode compl=-8e11
save outfile=$"simrun"_vbd.str
log off
quit
```

1. Schottky diode with a mesa



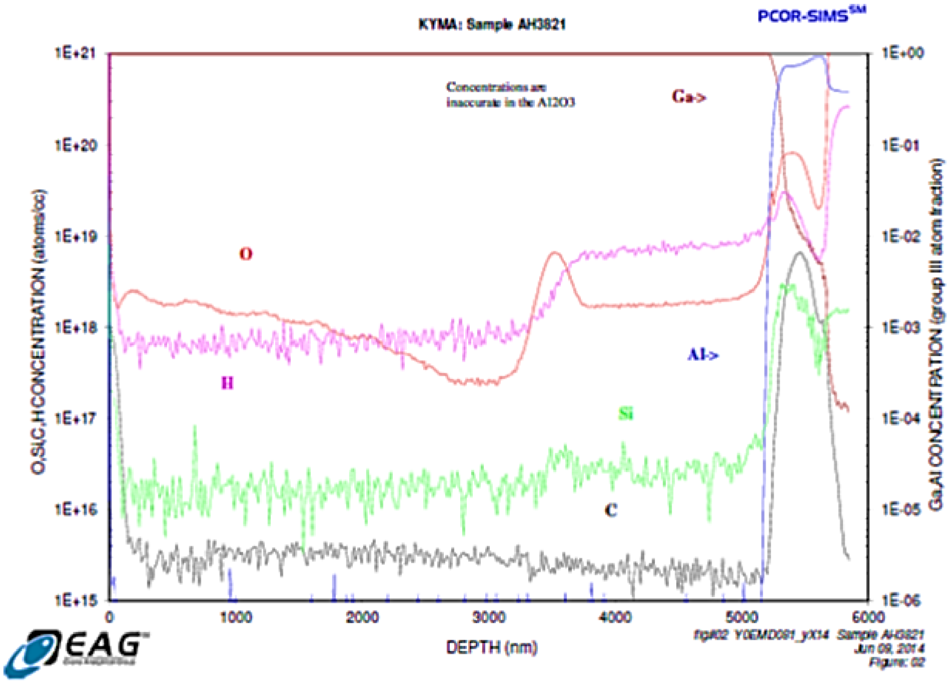
```
go atlas
## Material thickness ##
set sub_th=-1
set buf_th=-0.3
set epi_th=-3.5
set mesa_th=-1.5
set anode_th=-0.1
set cathode_th=-0.1
set start_anode_left=10
set start_anode_right=20
set end_width=30
set start_width=0
################# dimensions_substarte ##################
set x0=$start_width
set y0=$start_width
set x1=$end_width
set y1=$start_width
set x2=$end_width
set y2=$sub_th+$cathode_th
set x3=$start_width
set y3=$sub_th+$cathode_th
################### dimentions_ buffer ############################
set x4=$start_width
set y4=$sub_th+$cathode_th
set x5=$end_width
set y5=$sub_th+$cathode_th
set x6=$end_width
set y6=$sub_th+$buf_th+$cathode_th
set x7=$start_width
set y7=$sub_th+$buf_th+$cathode_th
###################dimensions_epitaxy  ###############################
set x8=$start_width
set y8=$buf_th+$sub_th+$cathode_th
set x9=$end_width
set y9=$buf_th+$sub_th+$cathode_th
set x10=$end_width
set y10=$sub_th+$buf_th+$epi_th+$cathode_th
set x11=$start_width
set y11=$sub_th+$buf_th+$epi_th+$cathode_th
########### MESA ##############
set x12=$start_anode_left
set y12=$buf_th+$sub_th+$epi_th+$cathode_th
set x13=$start_anode_right
set y13=$buf_th+$sub_th+$epi_th+$cathode_th
set x14=$start_anode_right
set y14=$sub_th+$buf_th+$epi_th+$mesa_th+$cathode_th
set x15=$start_anode_left
set y15=$sub_th+$buf_th+$epi_th+$mesa_th+$cathode_th
########### cathode #############
set x16=$start_width
set y16=$start_width
set x17=$end_width
set y17=$start_width
set x18=$end_width
set y18=$cathode_th
set x19=$start_width
set y19=$cathode_th
```

```
###########anode###############
set x20=$start_anode_left
set y20=$sub_th+$buf_th+$epi_th+$mesa_th
set x21=$start_anode_right
set y21=$sub_th+$buf_th+$epi_th+$mesa_th
set x22=$start_anode_right
set y22=$sub_th+$buf_th+$epi_th+$cathode_th+$mesa_th
set x23=$start_anode_left
set y23=$sub_th+$buf_th+$epi_th+$cathode_th+$mesa_th
set light=5e-5
set GaN_Eg=3.42
set GaN_diel=8.9
set GaN_Emob=1000*0.525
set GaN_Pmob=10
set GaN_satvel=1.125e7
set GaN_peak_vel=2.2e7
set GaN_intris_conc=2.9e-9
set GaN_Nc300=2.3e18
set GaN_Nv300=4.6e19
set GaN_Eab=0.175
set GaN_Edb=0.016
set GaN_taun=1e-9
set GaN_taup=1e-9
set GaN_Ec=3.75e6
set GaN_lattice=3.189
set simrun=mesa1.5um_ammono_dia10

#### dev edit ######
go devedit
region id=1 name=substrate material=GaN points="$x0,$y0 $x1,$y1 $x2,$y2
$x3,$y3 $x0,$y0"
impurity id=1 region.id=1 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply
region id=2 name=buffer material=GaN points="$x4,$y4 $x5,$y5 $x6,$y6
$x7,$y7 $x4,$y4"
impurity id=1 region.id=2 impurity=donors peak.value=5.e18
ref.value=1e12 comb.function=multiply
region id=3 name=epitaxy material=GaN points="$x8,$y8 $x9,$y9 $x10,$y10
$x11,$y11 $x8,$y8"
impurity id=1 region.id=3 impurity=donors peak.value=5.e16
ref.value=1e12 comb.function=multiply
region id=4 name=mesa material=GaN points="$x12,$y12 $x13,$y13
$x14,$y14 $x15,$y15 $x12,$y12"
impurity id=1 region.id=3 impurity=donors peak.value=5.e16
ref.value=1e12 comb.function=multiply
region id=6 name=anode material=contact  elec.id=1  points="$x20,$y20
$x21,$y21 $x22,$y22 $x23,$y23 $x20,$y20"
region id=7 name=cathode material=contact  elec.id=2  points="$x16,$y16
$x17,$y17 $x18,$y18 $x19,$y19 $x16,$y16"

## base mesh ##
base.mesh height=0.5 width=0.5
bound.cond max.slope=28 max.ratio=300 rnd.unit=0.01
line.straightening=1 align.points when=automatic
## global constraint##
constr.mesh material.type=semiconductor max.angle= 90 max.ratio=100
max.width=1 max.height=1 min.height=0.01 min.width=0.01
```

```
constr.mesh x1=$start_width y1=$start_width x2=$end_width y2=$sub_th
default max.height=1 max.width=1
set epi_top_y=$y10-0.1
set epi_bot_y=$y10+0.1
constr.mesh x1=$start_width y1=$epi_top_y x2=$end_width y2=$epi_bot_y
default max.height=0.1 max.width=0.1
maxadjacent=5 max.height=1 max.width=1 min.width=0.1 min.height=0.1
mesh
structure outfile=$"simrun"_init.str
tonyplot $"simrun"_init.str

go atlas
region number=1 material=GaN  substrate modify
region number=2 material=GaN  modify
region number=3 material=GaN  modify
material material=GaN real.index=2.67 imag.index=0.001
vsatn=$GaN_satvel ni.min=$GaN_intris_conc eg300=$GaN_Eg taun0=$GaN_taun
taup0=$GaN_taup mun0=$GaN_Emob mup0=$GaN_Pmob ALATTICE=$GaN_lattice
permittivity=$GaN_diel nc300=$GaN_Nc300 nv300=$GaN_Nv300 edb=$GaN_Edb
eab=$GaN_Eab
model  fermi  conmob  fldmob  srh  auger  bgn ten.polar print
impact selb material=GaN
beam number=1 x.o=0 y.o=-24 angle=90 min.window=$start_width
max.window=$end_width  wavelength=0.3
Output con.band val.band charge e.field ex.field ey.field devdeg
polar.charge traps Schottky flowlines
contact name=anode workf=5.3
method newton  trap maxtrap=30 carriers=2
solve init
solve b1=$light index.check
solve vanode=0 vcathode=0 b1=$light
save outfile=$"simrun"_0bias.str
log outfile=$"simrun"_fb.log
solve vanode=0.05  vstep=.1  vfinal=2  name=anode b1=$light
save outfile=$"simrun"_fb.str
log off
log outfile=$"simrun"_rb.log
solve vanode=-0.001  vstep=-0.5  vfinal=-3000  name=anode b1=$light
cname=anode compl=-1e-12
save outfile=$"simrun"_vbd.str
log off
quit
```

APPENDIX: B

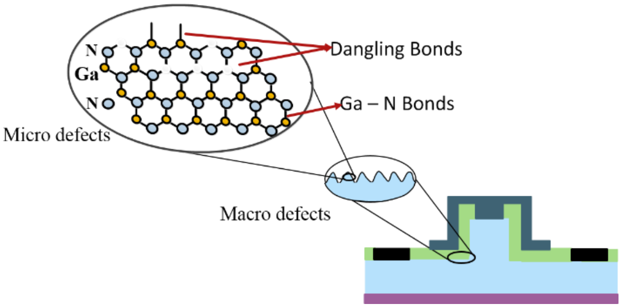
SIMS data for 5 ± 1 μm HVPE grown epilayer on sapphire provided by the manufacturing company



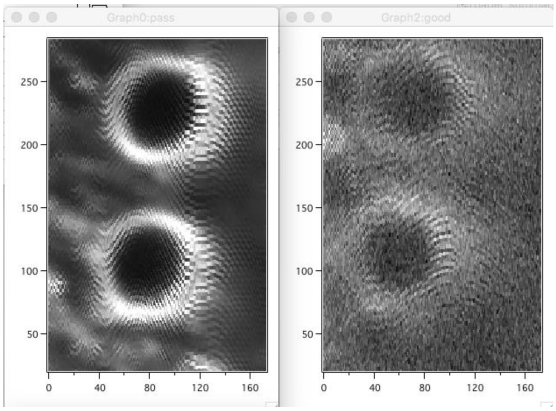
APPENDIX: C

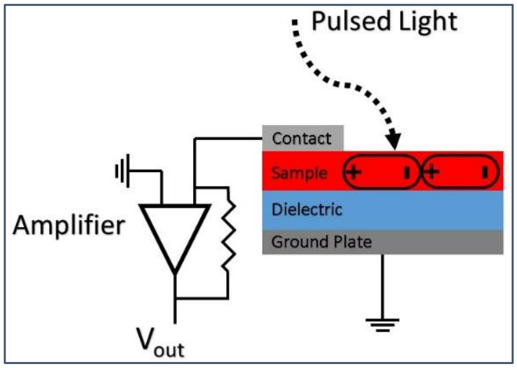
Capacitive photo current surface spectroscopy:

Dry etching changes the surface physical and chemical properties. ICP/RIE etching of GaN using Cl/Ar results in rough side walls and due to non-preferential loss of Ga and N atoms leaves behind dangling bonds on the surface generating defective states. The defect states on surface will further affect the electrical properties of the wrap around diodes made on these trench structures. Therefore, passivation of these surface states is necessary to restore the surface.



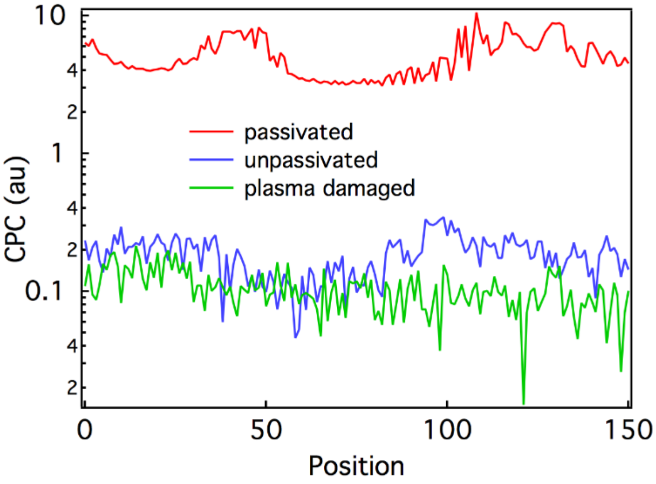
After dry etch, samples are cleaned in HCl followed by DI water flushing/N_2 blow drying. Then etched samples are passivated in Tert-butanol and ammonium sulphide [$(NH_4)2S_X$ solution at 60^0C for 5 mins. This will lead to bonding of Sulphur atoms with the Ga and will reduce the defect states. To verify the impact of surface passivation, the PL for samples is measured before and after the passivation. The band edge PL peak at 3.4 eV showed an increase in the intensity indicating the effect of surface states have been substantially reduced by the treatment. However, to verify the electrical properties, instead of fabricating the entire diode, capacitive photo current (CPC) measurements were made on the trenches.





A pulsed laser is shine on the samples, to generate electron hole pairs in GaN. Charge separation in material creates potential difference between sense and reference electrodes as shown in above figure(right).

Depending on the etch conditions, the capacitive photocurrent intensity varied. Sample with the sulphide passivation showed higher current signal than the ones that are not passivated. Indicating an improved electron hole pair generation in samples with the passivation.



CURRICULUM VITAE

Sowmya Kolli
Louisville, KY 40217
Sowmya.kolli17@gmail.com
(502) 594 – 6993

Summary

PhD candidate in electrical engineering with strong academic background and 6 years of research experience in III-V semiconductors, device design, fabrication and characterization

Education

Doctor of Philosophy in Electrical Engineering December 2017(Expected)
University of Louisville, KY
Thesis: Fabrication and Characterization of Gallium Nitride based Schottky diodes
Advisor: Dr. Bruce W Alphenaar

Master of Science in Electrical Engineering May 2012
University of Louisville, KY
Thermally activated Luminesce in Indium Nitride nanowires
Advisor: Dr. Bruce W Alphenaar & Dr. Mahendra Sunkara

Bachelor of Technology in Electronics and Communication Engineering May 2010
Jawaharlal Nehru Technological University (JNTU), Hyderabad, India

Research and Work Experience

Research Assistant August 2012 - Present

- Developed a novel field termination design to alleviate field crowding in GaN diodes
- Studied and optimized the etch rate, side wall angle and roughness of GaN using ICP/RIE based dry etching with corrosive Cl_2 and BCl_3 gas chemistries
- Built and tested lateral GaN Schottky diodes, and further analyzed the effect of bulk and etch induced defects on diode breakdown voltages

- Investigated the effect of dielectric (SiN) layer thickness on diode performance
- Currently working on the fabrication and characterization of vertical GaN diodes in a class 100 and class 1000 clean room

Research Assistant, University of Louisville, KY August 2010 – August 2012

- Synthesized group III-V nanomaterials specifically indium nitride, gallium nitride nanowires using chemical vapor deposition (CVD) technique
- Studied the luminescence properties of InN nanowires at high temperatures, which revealed the presence of a long lived trap state near the conduction band
- Gained expertise is CVD reactor and was responsible for maintenance and calibration

Teaching Assistant, University of Louisville

- Assisting the department of Electrical and Computer engineering in conducting and grading the course" Logic Design Lab" (5/15- 6/17)
- Conducted labs for ~200 students on "Dye sensitized Solar Cells" as part of freshman course

Technical Expertise

- Extensive research experience in the field of micro/nano fabrication, synthesis and characterization of nanomaterials
- Semiconductor processes and cleanroom techniques including contact photolithography, etching, thin film deposition and RTP
- Thin film Deposition: E-beam evaporation, DC Sputtering, PECVD
- Etching: Wet etching, ICP and Reactive Ion etching
- Material/surface characterization: SEM, XRD, EDX, UV-Vis-IR, Photoluminescence
- Knowledge of design of experiments (DOE) principles and statistical methods
- SOFTWARES: L-Edit, Silvaco (ATLAS, DEV EDIT), Igor, VHDL

Publications

- Kolli S., Hickman R. and Alphenaar B. "Wrap around field plate technique for GaN Schottky barrier diodes", MRS Proceedings, 1736, (**2014**) mrsf14-1736-t02-07 doi:10.1557/opl.2014.943.

- Kolli S., Sunkara M and Alphenaar B" Lateral GaN Schottky diodes with drift layer grown by HVPE", (Manuscript under review)
- Kolli S., Sunkara M and Alphenaar B" Vertical GaN Schottky diodes with drift layer grown by MOCVD on Ammono thermal substrates", (Manuscript under preparation)
- Kolli S., Jasinski J., Sunkara M. and Alphenaar B.," Thermally activated Luminescence in Indium Nitride nanowire arrays", Journal of Luminescence 141 (**2013**) 162–165
- Shah H., Carver A., Kolli S., Fernando K., Abeyweera B., Lisenkov, Menon M. and Alphenaar B., "Optical Generation and Detection of Polaronic States in PCBM", J. Phys. Chem. C (**2013**), 117, 26538−26542

Presentations

- Wrap around field plate technique for GaN Schottky barrier diodes, Materials research society, November **2014**
- Photo induced charge transfer across an organic/contact interface: Polaronic state spectroscopy, Physical Chemistry of Interfaces and Nanomaterials XII SPIE, September 11, **2013**
- Photo electrochemical Characterization of inxGa1-Xn Alloys Grown on GaN Nanowire Substrates, 223th ECS, May **2013**
- Fundamental light absorption studies in nanowire arrays, Poster presentation, 16th KY EPSCoR and Annual KY Innovation & Entrepreneurship Conference (KIEC) Joint Annual Conference Louisville, KY, May **2011**
- Synthesis of Indium Nitride Nanowires using reactive vapor deposition technique, Poster presentation Renewable energy & energy efficiency work shop, KY, **2011**

Awards/Affiliations

- Graduate Research Assistantship, CONN center for renewable energy research, University of Louisville (8/10-7/12)
- Grosscurth fellowship, University of Louisville (8/12-7/14)
- Golden Key International Honor society
- Materials Research society