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Low power strain sensor based on MOS tunneling current.

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LOW POWER STRAIN SENSOR BASED ON MOS TUNNELING CURRENT

By

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B.S., Beijing Institute of Technology, China, 2007

M.S., Beijing Institute of Technology, China, 2009

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A Dissertation Approved on

April 21, 2014

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DEDICATION

This dissertation is dedicated to my family, especially

to my parents, Xingqi Zhu and Hongmei Zhang, who guide me and support me for over 20 years;

to my wife, Mingxia, for being a great wife;

to my new born lovely boy, Yicheng, for his cheerful smile.

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ABSTRACT

LOW POWER STRAIN SENSOR BASED ON MOS TUNNELING CURRENT

Li Zhu

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Sensors, such as pressure sensors, accelerometers and gyroscopes, are very important components in modern portable electronics. A limited source of power in portable electronics is motivating research on new low power sensors. Piezoresistive and capacitive sensing technologies are the most commonly utilized technologies, which typically consume power in the μW to mW range. Tunneling current sensing is attractive for low power applications because the typical tunneling current is in the nA range.

This dissertation demonstrates a low power strain sensor based on the tunneling current in a metal-oxide-semiconductor (MOS) structure with a power consumption of a couple of nano-Watts (nW) with a minimum detectable strain of 0.00036%. Both DC and AC measurements were used to characterize the MOS tunneling current strain sensor. The noise level is found to be smallest in the inversion region, and therefore it is best to bias the device in the inversion region.

To study the sensitivity in the inversion region, a model is developed to compute the tunneling current as a function of strain in the semiconductor. The model calculates the tunneling current due to electrons tunneling from the

conduction band of the semiconductor to the gate (ECB tunneling current) and the tunneling current due to electrons tunneling from the valence band of the semiconductor to the gate (EVB tunneling current). It is found that the ECB tunneling current is sufficient to explain experimental gate leakage current results reported in the literature for MOSFETs with low substrate doping concentration. However, for the tunneling current strain sensor with a higher substrate doping concentration reported here, a model using both ECB and EVB tunneling current is required. The model fits our experiments.

During both DC and AC measurements, the MOS tunneling current is found to drift with time. The drift could arise from the trap states within the oxide. The current drift makes it difficult to obtain an absolute measurement of the strain. Combining the tunneling current strain sensor with a resonant sensor may be a good choice because it measures changes in the mechanical resonant frequency, independent of a drift of the tunneling current amplitude.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Since the research about the piezoresistance of silicon was published by Smith from Bell Telephones Laboratories in 1954, people have been studying the possibility of making micro sensors which have a superior performance to macro sensors at power consumption, reliability and size [1, 2]. According to different applications, microelectromechanical systems (MEMS) sensors can be cataloged into pressure sensors, accelerometers, gyroscopes, flow sensors, etc. Among these MEMS sensors, pressure sensors and accelerometers have a leading position in the markets [3]. The MEMS sensors can also be grouped to piezoresistive sensors, piezoelectric sensors, capacitivive sensors, etc. Piezoresistive sensors are among the earliest sensors, which are now being replaced by capacitive sensors.

Although MEMS pressure sensors and accelerometers have been widely researched and commercialized for decades, the recent increased demand for low power sensors is motivating research on new techniques. Portable electronics and biosensors in vivo usually require low power sensor to conserve power. Piezoresistive and capacitive sensing technologies are the most common technologies, which have been widely used to measure strain, pressure and acceleration [2, 4]. They both typically consume power from μW

to mW [5].

As for the piezoresistive sensors, to achieve low power consumption, the doping concentration of the piezoresistor has to be decreased For example, to have a minimum detectable strain of 0.001%, the doping concentration should be at least 10^{16} atoms/cm^3 [6], and this doping concentration gives a resistivity of 1 ohm-cm. Information from [7] indicates that the MOS tunneling current through a 3.8 nm thick and 1 mm × 1 mm area SiO_2 layer is around 1 nA at 1 V, which results in a resistivity of 10^{13} ohm-cm. It is obvious a good alternative for low power sensing compared with piezoresistive technology [7]. Besides the power consumption, another disadvantage of piezoresistive technology is that it is not easy to control the doping profile of the piezoresistive layer especially for a very thin layer [1]. The SiO_2 layer of the MOS tunneling sensor can be grown to less than 1 nm.

Capacitive sensors are the most common MEMS sensors now. They provide excellent low noise performance, high sensitivity, small temperature dependency and low power consumption. However parasitic capacitance of bond pads and small signal hinder the miniaturization of the capacitive sensors. Interface circuit is usually much more complex than piezoresistive sensors. The response is nonlinear, and both electrical and physical shielding is necessary [8, 9].

Besides adopting tunneling current through a MOS capacitor, tunneling sensors also employ tunneling current through an air gap between a tip and a plate which also have the merit of low power consumption. Pressure or acceleration induces displacement between the tip and the plate, which is read by the voltage or current changing [10-12]. The fabrication process of

this type of sensors is very complex. Like capacitive sensors, the response is also nonlinear. The interface circuit is very complex, which requires closed-loop control to maintain the gap distance. The reliability is also impacted due to deterioration of the tip.

The MOS tunneling sensors measure the current change induced by strain in silicon. The tunneling current is determined by the tunneling barrier between the silicon band edges and the gate dielectric band edges, as well as the effective mass. When a uniaxial strain is induced, the silicon band edges will be shift and split, which will change the tunneling barrier. As a result, the tunneling current changes with the strain. Detailed theory about the MOS tunneling sensors will be elaborated in the theory chapters.

Table 1 summarizes the advantages and the disadvantages of different MEMS sensors. The advantages are that the MOS tunneling current strain sensors are easy to fabricate and they are Complementary metal–oxide–semiconductor (CMOS) process compatible. However, the MOS tunneling current strain sensors are very sensitive to temperature like the piezoresistive sensors. Another disadvantage is that electrostatic discharge (ESD) protection is necessary, since the MOS tunneling current strain sensor is mainly a MOS capacitor.

Table 2 compares the gauge factor, the response linearity and the power consumption of different MEMS sensors. We can see that the gauge factor of MOS tunneling current strain sensor is in the same range of piezoresistive sensors, while its power consumption is much smaller. Here gauge factor is defined as $GF = \frac{\Delta R/R}{\varepsilon} = \frac{\Delta I/I}{\varepsilon} = \frac{\Delta C/C}{\varepsilon}$.

Table 1

Summaries of advantages and disadvantages for different sensing methods

	Advantages	Disadvantages
Piezoresistive	• Simple interface circuit	• Large temperature dependency • Difficult to control Doping profile in the nm range • High power consumption
Capacitive	• Excellent noise performance • High sensitivity • Small temperature dependency • Low power consumption	• Large area • Complex circuit • Need electrical and physical shield • Non-linear
Air gap Tunneling	• High sensitivity • Small temperature dependency	• Complex interface circuit • Tip deterioration • Non-linear
MOS tunneling	• Low power consumption • Easy to miniaturize	• Temperature dependent • Need ESD protection

Table 2

Summaries of gauge factor, linearity and power consumption for different sensing methods

Principle	Gauge Factor	Linearity	Power consumption
Piezoresistive	100 [9]	Linear	10 ~ 1000 uW [13, 14]
Capacitive	249 [15]	Nonlinear	~100 uW [16]
MOS Tunneling current	35 [7, 17]	Linear	1~100 nW [7]

1.2 Relevance of the research

This dissertation demonstrates the first use of tunneling current sensing for a sensor that is based on the effects of strain in the semiconductor substrate. Prior efforts to create tunneling current sensors all utilize the tunneling current through a gap between two materials, and thus inherently measure the gap between the electrodes. In this dissertation, it is fundamentally the strain in the semiconductor, and not the gap, that is measured.

Along with metal–oxide–semiconductor field-effect transistor (MOSFET) scaling, gate oxide is scaled down and MOS tunneling current or gate leakage current arises [18-20]. Since then, a lot of research on this MOS tunneling current has been done in both experimental and theoretical way [21-26]. Most of this research is focused on the performance of new high-k dielectric materials by studying their MOS tunneling current. Strained MOSFET can improve carries' mobility, which has been studied extensively. In the same time, MOS tunneling current in strained MOSFET is also studied by several groups [27-30]. However in this research, MOS tunneling current is treated as an unpleasant phenomenon, and very few study are done to use this MOS tunneling current. For example, MOS tunneling current can be a very competitive alternative for low power strain sensors because of its high resistivity.

In the dissertation, it is the first time that a strain sensor based on MOS tunneling current is made and characterized. Parameters like noise, drift and sensitivity of MOS tunneling current strain sensor are characterized. It is found that noise is very small when MOS devices are in the inversion region.

We perform both DC measurement and AC measurement for the characterization. We find that an AC method using lock-in amplifier is more efficient to reduce noise than normal DC method.

To study sensitivity, a computationally efficient model for MOS tunneling current is built. Other groups only study ECB tunneling current for MOS in inversion region, which is enough for current density study. It is found that both the ECB and the EVB tunneling current must be considered when calculating the sensitivity for high doping concentrations and high voltages. The model fits our experiment very well.

A RF resonator based on MOS tunneling current strain sensor is also made. The first try was not successful. However, some tips to improve the design for future research are learned from this first try.

1.3 Outline of Dissertation

The research goals of this project are to characterize the properties of MOS tunneling sensors, solve problems hindering the performance of the MOS tunneling sensors and make a resonator based on the MOS tunneling current strain sensor as an application.

Chapter 2 introduces research history of tunneling current as well as theories of MOS tunneling current. Different types of MOS tunneling current are discussed, like Fowler-Nordheim tunneling, direct tunneling and trap-assist-tunneling. In this chapter, an approximation method to calculate tunneling probability, the WKB method, is elaborated, as well as other basic formulas for MOS tunneling current. This WKB method will be used in the modeling for direct tunneling in Chapter 5.

Chapter 3 discusses strain effect on Silicon and MOS tunneling

current. First, the silicon band structure is briefly introduced. Then, the basic theory of strain tensor and stress tensor are introduced. In the end, strain effect on silicon band structure is discussed.

Chapter 4 characterizes the MOS tunneling current strain sensors experimentally using DC and AC method. The demonstration device is a cantilever beam. The MOS tunneling current strain sensor is fabricated near the fix end of the cantilever beam. Strain is induced by bending the free end. In the DC experiment, a semiconductor parameter analyzer is used to apply DC voltage and measure the DC current. During the AC experiment, a lock-in amplifier is used to isolate the MOS tunneling current. The reason of using AC method is to reduce noise in a faster way, which is very important especially when band width is considered for a sensor. From the experiments, it is found that the noise of NMOS tunneling current strain sensor in inversion region is much less than others.

Chapter 5 discusses modeling for NMOS tunneling current strain sensor in inversion region, which MOS tunneling current comprises two parts. One is the ECB tunneling current, in which electrons tunnel from conduction band. Another one is the EVB tunneling current, in which electrons tunnels from valence band. Sensitivity is extensively studied by modeling. In this chapter, it also shows that substrate doping concentration has a very large influence on MOS tunneling current.

Chapter 6 explores one application of MOS tunneling current strain sensor, which is a longitudinal bulk acoustic RF resonator. In this chapter, we design, simulate, fabricate and test a 13 MHz longitudinal bulk acoustic RF resonator. The difficulties of the fabrication are discussed in this chapter. The

resonator does not work. The reasons that may lead the resonator to fail are analyzed, and some modifications for future design are proposed.

In the end, Chapter 7 does a summary of this dissertation as well as a proposal of future research.

CHAPTER 2

INTRODUCTION TO MOS TUNNELING CURRENT

2.1 History of quantum tunneling studying

This chapter gives a brief introduction of the history of quantum tunneling studying. Quantum tunneling is a phenomenon that a particle can penetrate a barrier which potential is higher than the particle's kinetic energy. Taking tunneling current as an example, the carrier (hole or electron) can surmount a potential barrier which is larger than its kinetic energy. This phenomenon is impossible in classic physics [18, 31].

After the discovery of natural alpha radioactivity in 1896, the law of exponential decay was established through the efforts of Elster, Rutherford, etc. [31, 32]. The theory of α-radioactivity on the basis of quantum tunneling was proposed by Gamow in 1928. Classically, the particle confined to the nucleus lacks the energy to surmount the nucleus potential wall, but in quantum mechanics there is a probability at which a particle can tunnel out of the nucleus. Gamow solved a model potential for the nucleus by combining the attractive nuclear forces with the Coulomb repulsion and derived from a relationship between the half-life of the alpha-decay event process and the energy of the emission, the Geiger-Nuttall formula, which had been previously discovered empirically [32, 33]. At nearly the same time, the problem was also solved by Gurney and Condon qualitatively [32].

During the same period, tunneling was used to explain electron emission from cold metal by Fowler and Nordheim [34]. They proposed a one-dimensional model. Metal electrons are confined by a potential wall whose height is determined by the work function plus the Fermi energy, and the wall becomes triangle like and thinned with an applied high electric field. The electrons tunneling through the potential wall change with applied electric field. Along with this model, they came up with the famous Fowler-Nordheim equation [31],

$$J = AF^2 \exp\left(-\frac{\sqrt{2m_{eff}}}{\hbar}\frac{4}{3}\frac{(\Phi_B)^{\frac{3}{2}}}{qF}\right) \tag{2.1}$$

where $\hbar$ is Planck's constant, q is electronic charge, F is electric field in the oxide, Φ_B is barrier height, and m_{eff} is electron effective mass of the insulator.

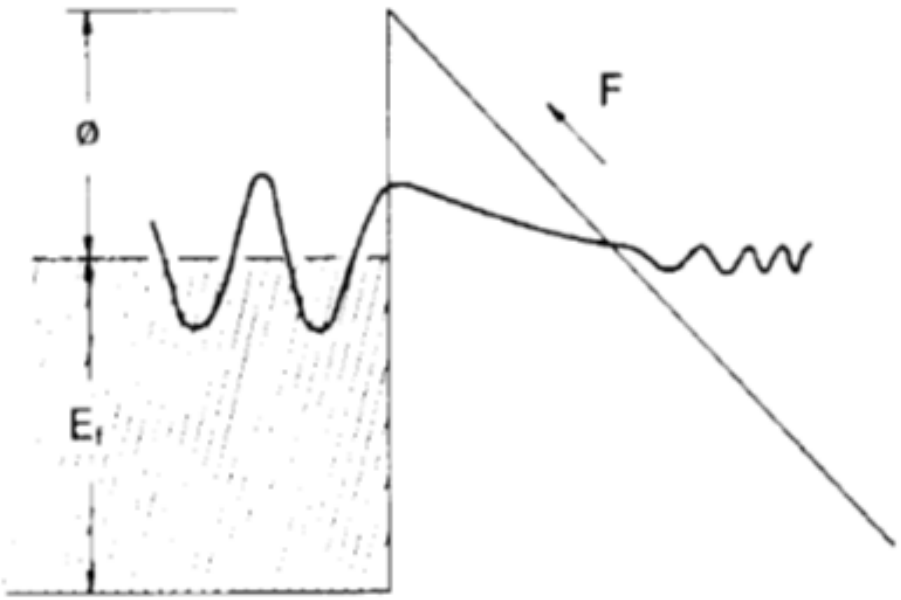


Figure 2.1 FN tunneling (Figure is from [31]).

During the 1930s and 1940s, tunneling was proposed to explain the transportation of electrical contacts between two solids. In 1930, Frenkel [35]

proposed that the anomalous temperature independence of contact resistance between metals could be explained in terms of tunneling across a narrow vacuum separation. Holm and Meissner verified that by experiment. In 1932, Wilson [36], Frenkel and Joffe [37] and Nordheim [38] applied quantum mechanical tunneling to the interpretation of metal-semiconductor contacts (rectifiers), but it was late proved to be wrong about the direction of rectifying in reality.

In 1950, with the development of diodes and transistors, the tunneling of electrons received new attention. In 1957 Esaki discovered the tunneling diode and this discovery proved the electron tunneling in solids conclusively [31]. The tunneling diode shows a negative resistive region as shown in Figure 2.2. This negative resistance can be interpreted by Figure 2.3. Both p and n type semiconductor are heavily doped to degeneration. When V_1 is applied, electrons tunnel from n type conduction band to the p type valence band. When the voltage is increased to V_2, there is no energy level for electrons to tunnel, so the current decreases. As the voltage continuously increases, the tunnel diode works like a normal p-n diode.

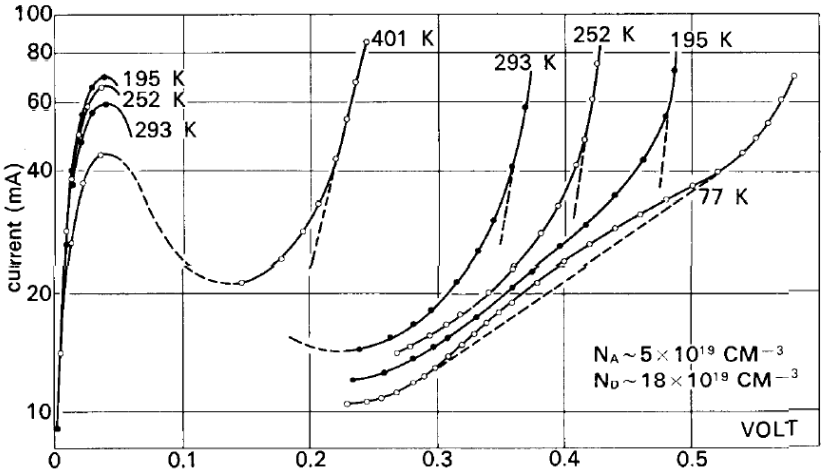


Figure 2.2 Current-Voltage relation of a tunneling diode [31].

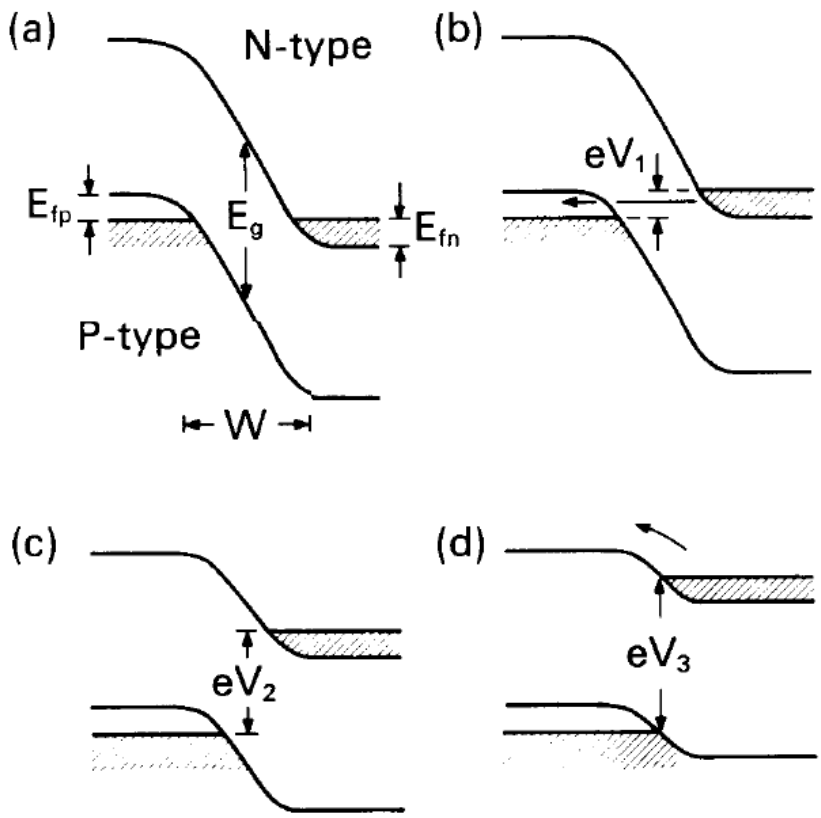


Figure 2.3 Band diagram of a tunneling diode at varies biases [31].

Tunneling was also researched in superconducting. In 1960, Giaever observed tunneling current between two conductors. At least one of the metals is a superconductor. This experiment enabled measurement of the energy gap in superconductors. This gap appears with Cooper pairs, and the gap plays an essential role in the BCS theory [39].

2.2 Different Types of Tunneling current in MOS capacitor

In the previous section, the history of research on quantum tunneling was reviewed briefly. This section will focus on MOS tunneling current. There are mainly three types of tunneling current in MOS capacitor, Fowler-Nordheim tunneling current, direct tunneling current and trap-assist-tunneling current.

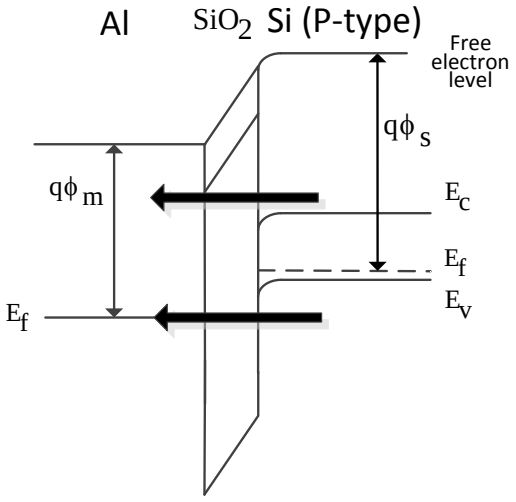
As mentioned in the previous section, Fowler and Nordheim give a complete theory of Fowler-Norheim tunneling. However it is complicated. Lenzlinger and Snow simplify the equation by ignoring the effects of finite temperature and image-force barrier lowering [40]. The simplified equation is,

$$J = \frac{q^3 F^2}{16\pi^2 \hbar \Phi_B} \exp\left(-\frac{\sqrt{2m_{eff}}}{\hbar} \frac{4}{3} \frac{(\Phi_B)^{\frac{3}{2}}}{qF} \right) \tag{2.2}$$

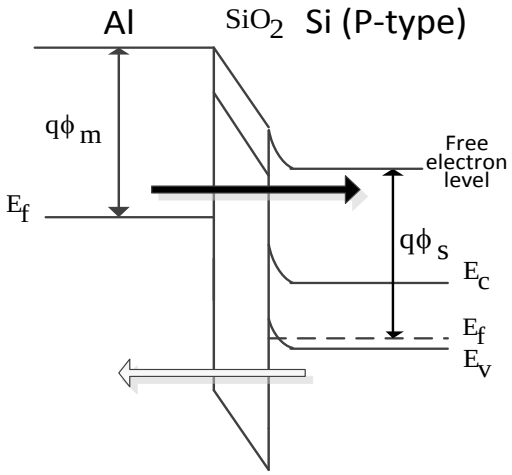
where $\hbar$ is Planck's constant, q is electronic charge, F is electric field in the oxide, Φ_B is barrier height, and m_{eff} is electron effective mass of the insulator. Section 2.3 will derive this equation for Fowler-Norheim tunneling current. The reason that Equation 2.2 is derived is to get deep understanding of MOS tunneling current. In the same time, some concepts from Fowler-Norheim tunneling current are used to derive models for direct tunneling current, like WKB method.

If the gate oxide is less than 4 nm, direct tunneling current will arise and become much larger than Fowler-Norheim tunneling current. As shown in the Figure 2.4 (a), when the gate voltage applied to the metal gate MOS devices is positive, there are two types of MOS tunneling current. One is ECB, where the electrons tunnel from the conduction band of silicon to aluminum; another one is EVB, where the electrons tunnel from the valence band of silicon to aluminum. When a negative gate voltage is applied to the gate as shown in Figure 2.4 (b), there are also two components of tunneling current. One is tunneling current from aluminum; another one is HVB, where the holes tunnel from the valence band of silicon to aluminum. The following chapters will focus on direct tunneling current, since the gate oxide of our MOS tunneling current strain sensor is less than 4 nm. Modeling of direct tunneling

current will be fully discussed in Chapter 5.



(a)



(b)

Figure 2.4 Illustration of direct tunneling in MOS structure. (a) positive bias; (b) negative bias.

The last type of MOS tunneling current is the trap-assist-tunneling current, which is shown in Figure 2.5. Electrons from the cathode first tunnel into the traps in the insulator layer, and then tunnel into the anode from the traps in the insulator layer. Traps are usually defects in the insulator layer.

During the trapping procedure, electrons usually exchange energy with insulator lattice through phonons. Large tunneling current at large gate voltage usually will introduce defects in the insulator layer, which will eventually break the insulator layer. Trap-assist-tunneling current is commonly recognized as one of the sources of noise in MOS tunneling current.

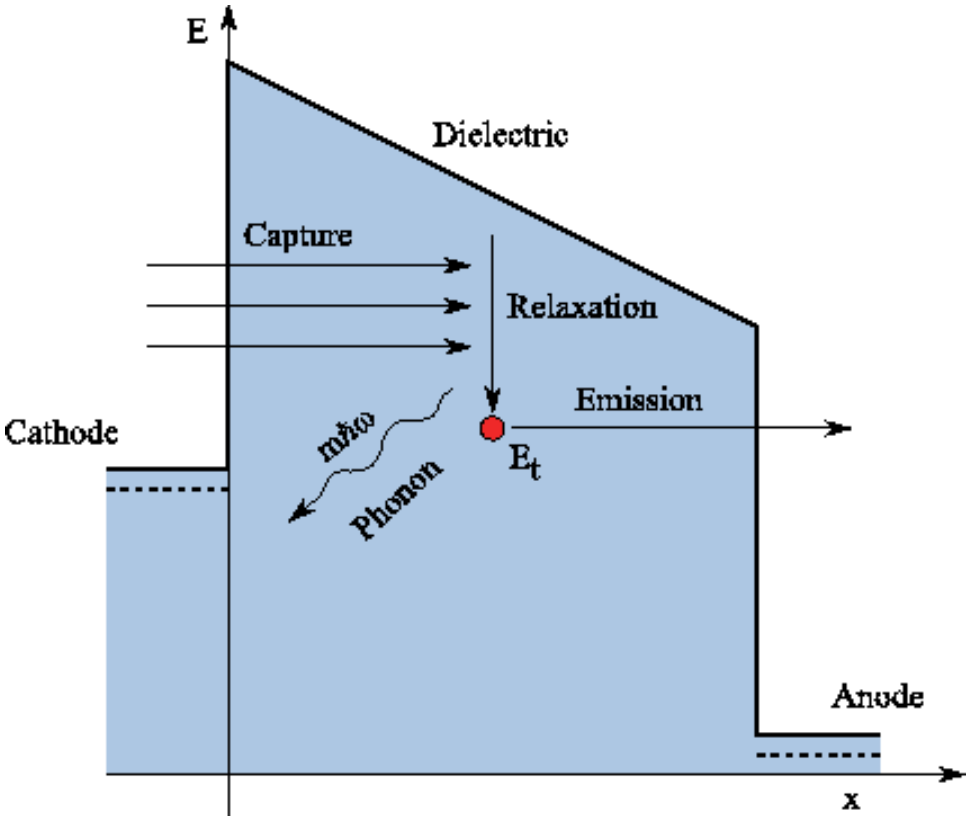


Figure 2.5 Schematic illustrating the Trap-assist-Tunneling current. The figure is from [41].

2.3 Derivation of Fowler-Nordheim tunneling current equation in MOS structure

This section will derive Fowler-Nordheim tunneling Equation 2.2. The purpose of this derivation is to understand MOS tunneling current deeper. The derivation for Equation 2.2 will also be partly adopted in the derivation of

formula for direct tunneling current. The Tsu and Esaki model and the WKB method will be used to formulate a general equation for Fowler-Nordheim tunneling current. After the general equation is derived, by setting temperature to 0 K to remove temperature influence, Equation 2.2 can be derived.

2.3.1 Tsu and Esaki model for Fowler-Nordheim tunneling current equation

The formula for Fowler-Nordheim tunneling can be derived by the Tsu and Esaki model [42]. In the Tsu and Esaki model, as shown in Figure 2.6, it is assumed that the net tunneling current is determined by difference between the current flow from side 1 to side 2 ($J_{1\rightarrow 2}$) and the current flow from side 2 to side 1 ($J_{2\rightarrow 1}$).

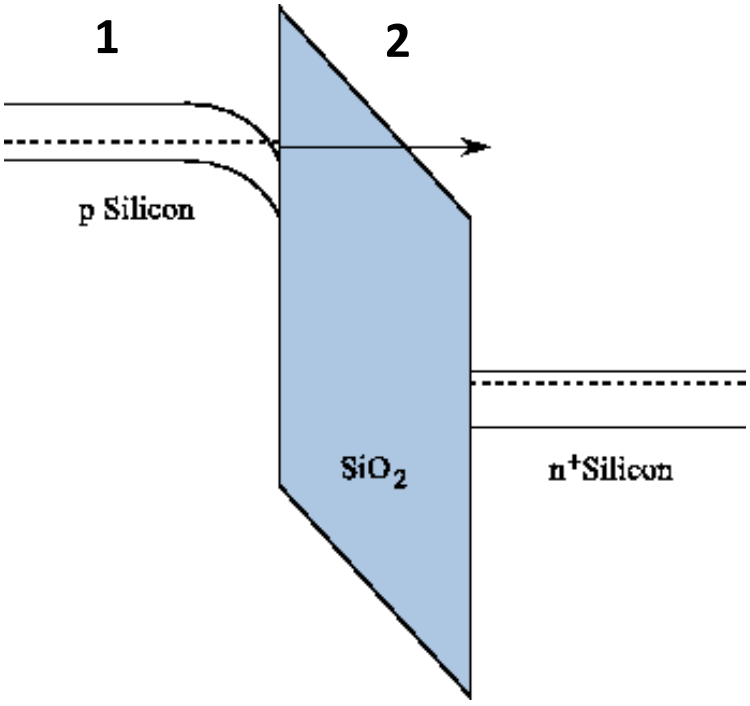


Figure 2.6 Schematic illustrating Fowler-Nordheim Tunneling current. The figure is from [41].

$$dJ_{1\to2} = qTC_1(k_x)v_x g_1(k_x)f_1(E)(1-f_2(E))dk_x$$
$$dJ_{2\to1} = qTC_2(k_x)v_x g_2(k_x)f_2(E)(1-f_1(E))dk_x \quad (2.3)$$

The current density through the two interfaces depends on the perpendicular component of the wave vector k_x , the transmission coefficient TC, the perpendicular velocity v_x, the density of states $g(k_x)$, and the Fermi-Dirac distribution function $f(E)$ at both sides of the barrier. For the Fowler-Nordheim tunneling, side 2 is the conduction band edge of SiO_2. Since SiO_2 is an insulator, $f_2(E)$ is almost 0 for energies above the conduction band edge of SiO_2. As a result, $J_{2\to1}$ is ignored and only $J_{1\to2}$ exists, which can be written as,

$$\mathrm{d}J = qTC(k_x)v_x g(k_x)f(E)dk_x \quad (2.4)$$

Here the density of states $\mathrm{g(k_x)}$ is

$$g(k_x) = \int_0^\infty \int_0^\infty g(k_x, k_y, k_z)dk_y\, dk_z \quad (2.5)$$

where $g(k_x, k_y, k_z)$ denotes the three-dimensional density of states in the momentum space. Considering the quantized wave vector components within a cube of side length L,

$$\Delta k_x = \frac{2\pi}{L}, \Delta k_y = \frac{2\pi}{L}, \Delta k_z = \frac{2\pi}{L} \quad (2.6)$$

The density of states within the cube can be written as

$$g(k_x, k_y, k_z) = 2\frac{1}{\Delta k_x \Delta k_y \Delta k_z}\frac{1}{L^3} = \frac{1}{4\pi^3} \quad (2.7)$$

where the factor 2 comes from spin degeneracy. For the parabolic dispersion relation, the velocity and energy components in tunneling direction obey

$$v_x = \frac{1}{\hbar}\frac{\partial E}{\partial k_x} = \frac{\hbar k_x}{m_{eff}},\ E_x = \frac{\hbar^2 {k_x}^2}{2m_{eff}},\ v_x dk_x = \frac{1}{\hbar} dE_x \tag{2.8}$$

Then Equation 2.4 can be rewritten as

$$dJ = \frac{q}{4\pi^3 \hbar} TC(E_x) dE_x \int_0^\infty \int_0^\infty f(E_x) dk_y\, dk_z \tag{2.9}$$

Next, let's transfer Equation 2.6 from Cartesian coordinate to Polar coordinate, which is

$$\begin{gathered} k_r = \sqrt{{k_y}^2 + {k_z}^2},\ \theta = \arctan(\frac{k_z}{k_y}) \\ k_y = k_r \cos(\theta),\ k_z = k_r\, sin(\theta) \end{gathered} \tag{2.10}$$

So the 3D dispersion equations can be rewritten as,

$$\begin{gathered} E_r = \frac{\hbar^2({k_y}^2 + {k_z}^2)}{2m_{eff}} = \frac{\hbar^2 {k_r}^2}{2m_{eff}} \\ E_x = \frac{\hbar^2 {k_x}^2}{2m_{eff}} \end{gathered} \tag{2.11}$$

As $\int_0^\infty dk_y \int_0^\infty dk_z = \int_0^{2\pi} d\theta \int_0^\infty k_r\, dk_r$, current density can be rewritten as

$$\begin{aligned} J &= \frac{4\pi q m_{eff}}{h^3} \int_{E_{min}}^{E_{max}} TC(E_x) dE_x \int_0^\infty f(E) dE_r \\ &= \frac{4\pi q m_{eff}}{h^3} \int_{E_{min}}^{E_{max}} TC(E_x) dE_x \int_{E_x}^\infty f(E) dE \end{aligned} \tag{2.12}$$

Here $E = E_r + E_x$, so $dE = dE_r$. The lower limitation 0 of $\int_0^\infty f(E) dE_r$ becomes E_x for $\int_{E_x}^\infty f(E) dE$. Putting the equation of Fermi-Dirac distribution $f(E) = \frac{1}{e^{(\frac{E-E_f}{\kappa T})}+1}$ into Equation 2.12 results in

$$
\begin{aligned}
J &= \frac{4\pi q m_{eff}}{h^3}\int_{E_{min}}^{E_{max}} TC(E_x)dE_x \int_{E_x}^{\infty} f(E)dE \\
&= \frac{4\pi q m_{eff}}{h^3}\int_{E_{min}}^{E_{max}} TC(E_x)dE_x \int_{E_x}^{\infty} \frac{1}{e^{\left(\frac{E-E_f}{k_BT}\right)}+1} dE \\
&= \frac{4\pi q m_{eff}}{h^3}\int_{E_{min}}^{E_{max}} TC(E_x)dE_x\, k_BT\, (-\ln\left(e^{\left(-\frac{E-E_f}{k_BT}\right)}+1\right)\Big|_{E_x}^{\infty} \\
&= \frac{4\pi q m_{eff} k_B T}{h^3}\int_{E_{min}}^{E_{max}} TC(E_x)\ln\left(e^{\left(-\frac{E_x-E_f}{k_BT}\right)}+1\right)dE_x
\end{aligned}
\tag{2.13}
$$

Now the general equation for Fowler-Nordheim tunneling current has been derived. In the next section, the formula for the tunneling probability $TC(E_x)$ will be solved based on the WKB method.

2.3.2 The WKB method

The WKB method is an approach to get an approximate solution for a linear partial differential equation with spatially varying coefficient. It is also known as the LG or Liouville–Green method [43]. In the tunneling cases, this spatially varying coefficient is the slowly varying potential in the gate oxide. In this section, general formula for the tunneling probability $TC(E_x)$ will be deduced, which is then put into Equation 2.13 to get the final general Fowler-Nordheim tunneling current formula. The derivation can be found in any quantum mechanics book. It should be pointed out that WKB method is not only used for Fowler-Nordheim tunneling current equation, it is also used for direct tunneling current equation. This will be elaborated in the following sections.

For simplicity, as shown in Figure 2.7, only formula in one dimension is considered, though the WKB method can be applied to 3D. Electrons move along x direction. Here electrons tunnel from left to right. There are three regions in this schematic. Region 1 is the incident region, region 2 is the

forbidden region and region 3 is the transmitted region. Here E_f is the Fermi level, E_B is the work function, W is the thickness of the gate oxide, V_x is the linear varying potential in the gate oxide. E_z is forbidden energy at the position of Z along x direction.

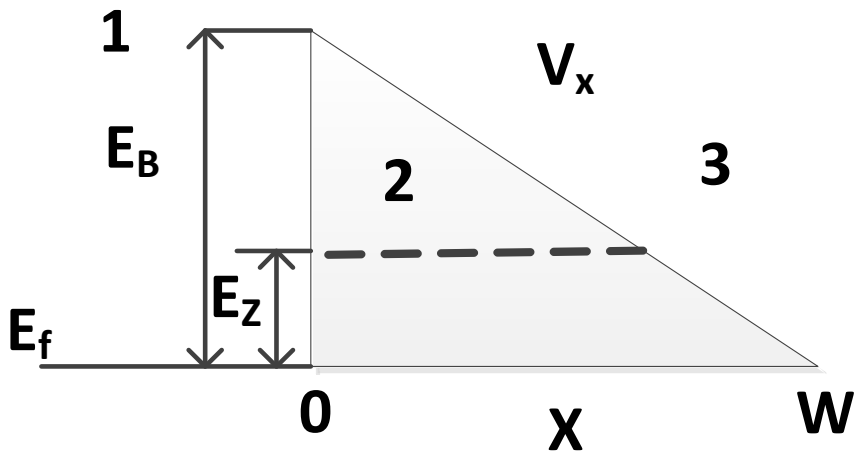


Figure 2.7 Schematic Illustrating for the WKB method.

Schrodinger equation can be solved under these boundary conditions. The Schrodinger equation for an electron moving along x direction is

$$-\frac{\hbar^2}{2m}\frac{d^2\psi}{d^2x}+V(x)\psi(x)=E\psi(x) \tag{2.14}$$

Or

$$\frac{d^2\psi}{d^2x}+\frac{1}{\hbar^2}p^2(x)\psi(x)=0 \tag{2.15}$$

where $p(x)$ is the classical momentum along x direction, $p(x)=\sqrt{2m(E-V(x))}$. m is the effective mass along the tunneling direction, which is x direction here. For the forbidden region which is the gate oxide, $V(x)$ varies linearly. It is easy to obtain the wave functions for the incident region and transmitted region respectively,

$$\psi_1(x) = \psi_{incident}(x) + \psi_{reflected}(x) = Ae^{ip_0x/\hbar} + Be^{-ip_0x/\hbar} \tag{2.16}$$

$$\psi_3(x) = \psi_{transmitted}(x) = Te^{ip_0x/\hbar} \tag{2.17}$$

where $\psi_1(x)$ is the wave function in the incident region and $\psi_3(x)$ is the wave function in the transmitted region. A, B and T are the amplitudes of the incident, reflected and transmitted waves respectively. $p_0 = \sqrt{2mE}$ is the momentum. The solution of the WKB method for the forbidden region assumes a form like,

$$\psi(x) = A(x)e^{iS(x)/\hbar} \tag{2.18}$$

where $A(x)$ is the amplitude and $S(x)$ is the phase, and they both are real functions. Substituting (2.18) into (2.15), we get

$$A[\frac{\hbar^2}{A}\frac{d^2\psi}{d^2x} - (\frac{dS}{dx})^2 + p^2(x)] + i\hbar[2\frac{dA}{dx}\frac{dS}{dx} + A\frac{d^2S}{d^2x}] = 0 \tag{2.19}$$

Only when both the real part and the imaginary part equal to 0, Equation 2.19 makes sense. Besides, since $\hbar$ is a small number, $\frac{\hbar^2}{A}\frac{d^2\psi}{d^2x}$ can be neglected. Thus,

$$\frac{dS}{dx} = \pm p(x) = \pm\sqrt{2m(E-V)} \tag{2.20}$$

$$2\frac{dA}{dx}\frac{dS}{dx} + A\frac{d^2S}{d^2x} = 0 \tag{2.21}$$

Integrating Equation 2.20 gives

$$S(x) = \pm\int\sqrt{2m(E-V)}dx \tag{2.22}$$

Rewriting Equation 2.21 yields

$$2\left(\frac{d}{dx}lnA\right)p(x)+\frac{d}{dx}p(x)=0$$

$$\xrightarrow{\text{yields}}\frac{\mathrm{d}}{\mathrm{dx}}(2lnA+lnp)=0 \tag{2.23}$$

$$\xrightarrow{\text{yields}}A=\frac{C}{\sqrt{|p(x)|}}$$

where C is a constant. Inserting Equation 2.22 and 2.23 into 2.18 indicates

$$\psi_{\pm}(x)=\frac{C_{\pm}}{\sqrt{|p(x)|}}\exp\left(\pm\frac{i}{\hbar}\int_{x_1}^{x}p(x')\,dx'\right) \tag{2.24}$$

Consider that E<V, which is known as the classically forbidden region, then (2.24) becomes,

$$\psi_2(x)=\frac{C}{\sqrt{|p(x)|}}\exp\left(-\frac{1}{\hbar}\int_{x_1}^{x}|p(x')|\,dx'\right)+\frac{D}{\sqrt{|p(x)|}}\exp\left(\frac{1}{\hbar}\int_{x_1}^{x}|p(x')|dx'\right) \tag{2.25}$$

Since $\exp\left(\frac{i}{\hbar}\int_{x_1}^{x}|p(x')|dx'\right)$ increase exponentially with x, which is impossible in Physics, it is neglected for $\psi_2(x)$. Then,

$$\psi_2(x)=\frac{C}{\sqrt{|p(x)|}}exp\left(-\frac{1}{\hbar}\int_{x_1}^{x}|p(x')|\,dx'\right) \tag{2.26}$$

Now the wave functions for three regions (incident region, forbidden region and transmitted region) are derived. The probability of tunneling (TC) can be expressed as

$$TC=\frac{v_{trans}}{v_{inc}}\frac{|\psi_{trans}(x)|^2}{|\psi_{inc}(x)|^2}=\frac{|T|^2}{|A|^2} \tag{2.27}$$

where the speed of incident (v_{inc}) and the speed of transmitted (v_{trans}) particles are equal. To get TC, $\psi_{inc}(x)$ and $\psi_{trans}(x)$ must be solved. By using the continuity relations between incident region and forbidden region $\psi_1(x_1)=$

$\psi_2(x_1)$ and $\psi_1{}'(x_1) = \psi_2{}'(x_1)$ indicates

$$Ae^{ip_0x_1/\hbar} + Be^{-ip_0x_1/\hbar} = \frac{C}{\sqrt{|p(x_1)|}} \tag{2.28}$$

$$\frac{i}{\hbar}(Ae^{ip_0x_1/\hbar} - Be^{-ip_0x_1/\hbar}) = -\frac{C|p(x_1)|}{\hbar\sqrt{|p(x_1)|}} \tag{2.29}$$

Adding Equation 2.28 and 2.29, it yields

$$C = 2A\sqrt{|p(x_1)|}/(1 - \sqrt{|p(x_1)|}/ip_0) \tag{2.30}$$

Using the continuity relations between forbidden region and transmitted region $\psi_2(x_2) = \psi_3(x_2)$ and $\psi_2{}'(x_2) = \psi_3{}'(x_2)$ can obtain,

$$\frac{C}{\sqrt{|p(x_2)|}}\exp\left(-\frac{1}{\hbar}\int_{x_1}^{x_2}|p(x')|\,dx'\right) = Te^{ip_0x_2/\hbar} \tag{2.31}$$

$$-\frac{|p(x_2)|C}{\hbar\sqrt{|p(x_2)|}}\exp\left(-\frac{1}{\hbar}\int_{x_1}^{x_2}|p(x')|\,dx'\right) = \frac{ip_0}{\hbar}Te^{ip_0x_2/\hbar} \tag{2.32}$$

Inserting Equation 2.31 into 2.30 results in

$$\frac{T}{A} = \frac{2}{1 - \sqrt{|p(x_1)|}/ip_0}\sqrt{\frac{p(x_1)}{p(x_2)}}\exp(ip_0(x_1 - x_2)/\hbar)\exp\left(-\frac{1}{\hbar}\int_{x_1}^{x_2}|p(x')|\,dx'\right) \tag{2.33}$$

So the tunneling probability is

$$\begin{aligned} TC &= \left|\frac{T}{A}\right|^2 \\ &= \frac{4}{\frac{|p(x_2)|}{|p(x_1)|} + \frac{|p(x_1)||p(x_2)|}{{p_0}^2}}\exp\left(-\frac{2}{\hbar}\int_{x_1}^{x_2}\sqrt{2m(V(x) - E)}\,dx\right) \\ &\sim \exp\left(-\tfrac{2}{\hbar}\textstyle\int_{x_1}^{x_2}\sqrt{2m(V(x) - E)}\,dx\right) \end{aligned} \tag{2.34}$$

Now the general tunneling probability from WKB method is obtained,

which is Equation 2.34. Next TC for Fowler-Nordheim tunneling current will be derived. For Fowler-Nordheim tunneling current, the potential barrier is like a triangle, so the tunneling probability for the Fowler-Nordheim tunneling current can be calculated. As shown in Fig. 2.7, it is assumed that the thickness of the barrier is *W*, the barrier height is E_B, the tunneling length of an energy of E_Z (which is relative to E_f) is *Z*. Thus,

$$V(x) = \left(1 - \frac{x}{W}\right) E_B + E_f \tag{2.35}$$

So TC can be derived as

$$\begin{aligned}
TC(E_Z + E_f) &= \exp\left(-\frac{\sqrt{8m}}{\hbar}\int_0^Z \sqrt{(1-\frac{x}{W})E_B - E_Z}\, dx\right) \\
&= \exp\left(-\frac{\sqrt{8m}}{\hbar}[-\frac{2}{3}\frac{W}{E_B}((1-\frac{x}{W})E_B - E_Z)^{3/2}\Big|_0^Z]\right) \\
&= \exp\left(\frac{\sqrt{8m}}{\hbar}\frac{2}{3}\frac{W}{E_B}\left[\left(\left(1-\frac{Z}{W}\right)E_B - E_Z\right)^{\frac{3}{2}} - (E_B - E_Z)^{\frac{3}{2}}\right]\right) \\
&= \exp\left(\frac{\sqrt{8m}}{\hbar}\frac{2}{3}\frac{W}{E_B}\left[-(E_B - E_Z)^{\frac{3}{2}}\right]\right) \\
&\cong \exp\left(-\frac{2\sqrt{8mE_B}W}{3\hbar}(1-\frac{3}{2}\frac{E_Z}{E_B})\right) \\
&= \exp\left(-\frac{2\sqrt{8mE_B}W}{3\hbar}\right)\exp(\frac{\sqrt{8mE_B}WE_Z}{\hbar E_B}) \\
&= T_0\, exp(\frac{E_Z}{E_0})
\end{aligned} \tag{2.36}$$

where

$$T_0 = \exp\left(-\frac{2\sqrt{8mE_B}W}{3\hbar}\right) \tag{2.37}$$

$$E_0 = \frac{\hbar E_B}{W\sqrt{8mE_B}}$$

Inserting Equation 2.36 into 2.13 gives

$$J = \frac{4\pi q m_{eff} k_B T}{h^3} T_0 \int_{E_{min}}^{E_{max}} exp(\frac{E_x - E_f}{E_0}) \ln\left(e^{\left(-\frac{E_x - E_f}{k_B T}\right)} + 1\right) dE_x \tag{2.38}$$

Here $E_x - E_f = E_Z$. We assume $E_{min} = -\infty$ and $E_{max} = +\infty$. We can obtain

$$J = \frac{4\pi q m_{eff} k_B T}{h^3} T_0 \int_{-\infty}^{+\infty} \exp(\frac{E_x - E_f}{E_0}) \ln\left(e^{\left(-\frac{E_x - E_f}{k_B T}\right)} + 1\right) dE_x \tag{2.39}$$

Using the variable change $u = e^{\left(-\frac{E_x - E_f}{k_B T}\right)}$ and $du = \frac{-1}{k_B T} u dE_x$ gives the current density,

$$\begin{aligned} J &= \frac{4\pi q m_{eff} k_B T}{h^3} T_0 (-k_B T) \int_{+\infty}^{0} u^{-\frac{k_B T}{E_0} - 1} \ln(u+1) du \\ &= \frac{4\pi q m_{eff} k_B T}{h^3} T_0 (k_B T) \int_{0}^{+\infty} u^{-\frac{k_B T}{E_0} - 1} \ln(u+1)\, du \\ &= \frac{4\pi q m_{eff} k_B T}{h^3} T_0 (k_B T) \frac{\pi}{\left(\frac{k_B T}{E_0}\right) \sin(\frac{k_B T}{E_0}\pi)} \\ &= \frac{4\pi q m_{eff} (k_B T)^2}{h^3 \left(\frac{k_B T}{E_0}\right)^2} T_0 \frac{\left(\frac{k_B T}{E_0}\right)\pi}{\sin(\frac{k_B T}{E_0}\pi)} \end{aligned} \tag{2.40}$$

Since

$$\begin{aligned} T_0 &= \exp\left(-\frac{2\sqrt{8mE_B}W}{3\hbar}\right) \\ &= \exp\left(\frac{\sqrt{8m}}{\hbar}\frac{2}{3}\frac{W}{E_B}\left[-(E_B)^{\frac{3}{2}}\right]\right) \end{aligned} \tag{2.41}$$

and

$$E_B = qFW \tag{2.42}$$

where F is the electrical field in the insulator, Equation 2.40 can be written as

$$J = \frac{4\pi q m_{eff}\left(\frac{\hbar E_B}{W\sqrt{8m_{eff}E_B}}\right)^2}{\hbar^3 8\pi^3}\exp\left(-\frac{\sqrt{2m_{eff}}}{\hbar}\frac{4}{3}\frac{(E_B)^{\frac{3}{2}}}{qF}\right)\frac{\left(\frac{k_B T}{E_0}\right)\pi}{\sin\left(\frac{k_B T}{E_0}\pi\right)}$$

$$= \frac{q^3F^2}{16\pi^2\hbar E_B}\exp\left(-\frac{\sqrt{2m_{eff}}}{\hbar}\frac{4}{3}\frac{(E_B)^{\frac{3}{2}}}{qF}\right)\frac{\left(\frac{k_B T}{E_0}\right)\pi}{\sin\left(\frac{k_B T}{E_0}\pi\right)} \tag{2.43}$$

For the special case of T =0 K, the classic Fowler-Nordheim tunneling current formula without temperature influence can be obtained

$$J = \frac{q^3F^2}{16\pi^2\hbar E_B}\exp\left(-\frac{\sqrt{2m_{eff}}}{\hbar}\frac{4}{3}\frac{(E_B)^{\frac{3}{2}}}{qF}\right) \tag{2.44}$$

Now the derivation for the Fowler-Nordheim tunneling current is completed, but several things should be paid attention to,

1) The electrons in the emitted electrode are assumed to be free Fermi gas.
2) The barrier lowering due to the image force is neglected.
3) The effective mass in the formula is the effective mass in the forbidden region. Since the effective mass is related to energy which varies in the forbidden region slowly, it is usually averaged through the whole region.

2.4 Direct tunneling in MOS structure

Direct tunneling is a mechanism that the electrons tunnel directly into the other electrode instead of the conduction band of the insulator. Taking

MOS structure as an example, when the thickness of insulator (SiO_2) is less than 4 nm, direct tunneling dominates. However when the thickness of insulator is more than 4 nm, Fowler-Nordheim tunneling current dominates. There are several different components of a direct tunneling current, depending on the gate voltage polarization and amplitude of voltages and the material of the conductors.

2.4.1 Derivation of the direct tunneling formula

During the derivation of Fowler-Nordheim tunneling current formula, we use WKB method to calculate the tunneling probability which is only valid when the oxide layer is thicker than 4 nm. When the thickness of the oxide layer is less than 1 nm, the assumption that the barrier changes slowly, which is the fundamental assumption of the WKB method, may not be very accurate. For gate oxide thickness larger than 1 nm, we still can use WKB method for TC. There are also several alternative methods to derive the direct tunneling formula. The results from these methods are close and fit to the measurement well [44]. Here we only briefly introduce the transfer matrix method to calculate the tunneling probability.

The general direct tunneling current formula can also be derived by the Tsu and Esaki model. When deriving the FN tunneling formula, it is assumed that $J_{2\to1}$ (the current from the conduction band of SiO_2) can be ignored and obtain Equation 2.13. However for the direct tunneling, $J_{2\to1}$ (the current from the conduction band of substrate) is kept, so the total net tunneling current is,

$$J = J_{2\to1} - J_{1\to2} = \frac{4\pi q m_{eff} k_B T}{h^3} \int_{E_{min}}^{E_{max}} TC(E_x) \ln\left(\frac{e^{\left(-\frac{E_x - E_{f2}}{k_B T}\right)} + 1}{e^{\left(-\frac{E_x - E_{f1}}{k_B T}\right)} + 1}\right) dE_x \quad (2.45)$$

where E_{f1} or E_{f2} is the Fermi level in the side 1 or 2. The next step is to find $TC(E_x)$ using transfer matrix method. To apply transfer matrix method, the whole scattering barrier is partitioned in to many small slab regions, and in every slab region the barrier is assumed constant so that the Schrodinger equation can be solved analytically. The transfer matrix between two neighboring slabs is obtained by applying the continuity of the wave functions and their derivatives at the boundaries, and the overall transfer matrix is obtained by multiplying all these transfer matrices. For example, a barrier shown in Figure 2.8 can be divided into small slabs. The wave functions of slab j and slab j+1 are,

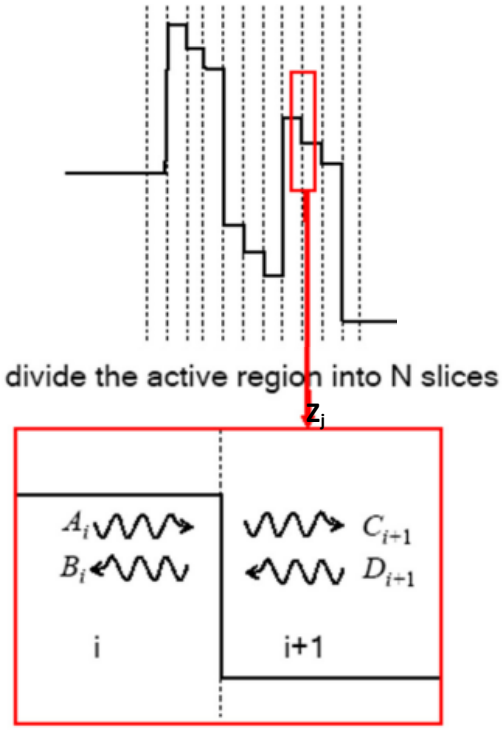


Figure 2.8 Transfer matrix method [45].

$$\psi_j(x) = A_j e^{ik_j x} + B_j e^{-ik_j x} \tag{2.46}$$

$$\psi_{j+1}(x) = C_{j+1} e^{ik_{j+1} x} + D_{j+1} e^{-ik_{j+1} x} \tag{2.47}$$

Using the continuity conditions,

$$\psi_j(Z_j) = \psi_{j+1}(Z_j)$$
$$\frac{\partial \psi_j(Z_j)}{\partial Z} = \frac{\partial \psi_{j+1}(Z_j)}{\partial Z} \tag{2.48}$$

The transfer matrix T_j is

$$\begin{bmatrix} C_{j+1} \\ \mathrm{D}_{j+1} \end{bmatrix} = T_j \begin{bmatrix} A_j \\ \mathrm{B}_j \end{bmatrix} \tag{2.49}$$

Therefore, the overall transfer matrix TC is

$$TC = T_1 T_2 T_3 \cdots T_j \cdots T_{max} \tag{2.50}$$

It is obvious that we cannot get an analytic solution from transfer matrix method.

2.5 Summary

This chapter reviews the history of tunneling from the early 20 centuries' research on alpha radioactivity to recently extensive research on superconducting. Then MOS tunneling current is elaborated. First, three types of MOS tunneling current, Fowler-Nordheim tunneling current, direct tunneling current and trap-assist-tunneling current are introduced. Since the Fowler-Nordheim tunneling current and direct tunneling current are the main tunneling current in MOS capacitor, to deep understand these two types of tunneling current, the general tunneling current formula for these two types of tunneling current are derived. Two approaches to solve tunneling probability are discussed, which are WKB method and transfer matrix method. WKB method can be used in both Fowler-Nordheim tunneling current and direct tunneling current (which gate oxide thickness is larger than 1 nm and less than 4 nm), while transfer matrix method is mainly used in direct tunneling

current. The advantage of the WKB method is its simplicity and it is analytically expressed.

As shown in Chapter 4, the proposed experimental device's gate oxide is less than 4 nm, so direct tunneling current dominates. Therefore in Chapter 5, how to solve direct tunneling current based on this chapter as well as other factors like inversion layer energy quantization will be elaborated in detail.

CHAPTER 3

STRAIN EFFECTS IN SILICON

Chapter 2 discusses MOS tunneling current, especially the Fowler-Nordheim tunneling current and direct tunneling current. In this chapter, strain effects in silicon will be introduced. First, silicon band structure will be discussed, and then some concepts about stress and strain will be investigated. In the end, how strain affects band structure and eventually MOS tunneling current will be explored.

3.1 Silicon band structure

To calculate the band structure of a crystal like Silicon, the single electron Schrodinger equation must be solved [46],

$$H\psi(\boldsymbol{r}) = \left(\frac{p^2}{2m} + V(\boldsymbol{r})\right)\psi(\boldsymbol{r}) = E\psi(\boldsymbol{r}) \tag{3.1}$$

where $\mathrm{V}(\mathbf{r})$ is the effective crystal potential, m is the effective mass. $\mathbf{r}$ is the movement direction of electrons. The difference among different materials is $\mathrm{V}(\mathbf{r})$ and m. It is the single crystal silicon that is studied here. A crystal is constructed of replicas of lattice, which is an array of atoms or molecules repeating periodically in three dimensions. The lattice of silicon is face centered cubic (FCC) as shown in Figure 3.1. The FCC lattice is point symmetry, and there are a total of 48 symmetry operations. Since the arrangement of atoms influence effective crystal potential, the effective crystal

potential is also periodic and symmetric. Here we define lattice constant is a.

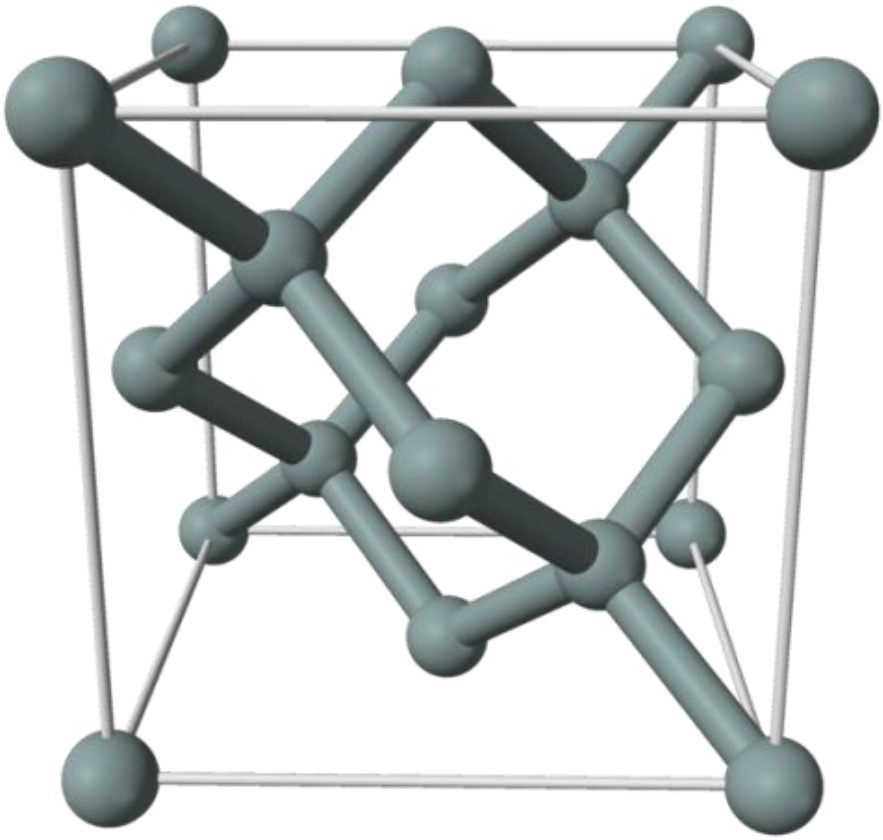


Figure 3.1 FCC lattice [47].

The band structure of Silicon solved by the Schrodinger equation is shown in Figure 3.2, which is constructed in the reciprocal space (k space) of the real lattice space. The reciprocal lattice for an FCC lattice is a body centered cubic (BCC) lattice. Due to the translation of the reciprocal lattice, it is conventionally only plotting the energy levels in the first Brillouin zone, which is defined as the space enclosed by the planes perpendicular to and bisecting the lines connecting a reciprocal lattice point and its neighbors. The first Brillouin zone of Silicon is shown in Figure 3.3. In the figure, Γ point is the center point of the first Brillouin zone. X point is located at 2π/a(0, 1, 0)

labeling the center of the square surfaces, and the direction from Γ to X is named as Δ. L point is located at 2π/a(0.5, 0.5, 0.5) labeling the center of the hexagonal surfaces, and the direction from Γ to L is labeled as Λ. Thus, the valley of valence band of Silicon is at the point of Γ, and its valley of conduction band is located between Γ and X along the direction of Δ. Since there are six equivalent directions of Δ, the valley of conduction band is six folded degenerated. The band gap is 1.12 ev for silicon [46, 48].

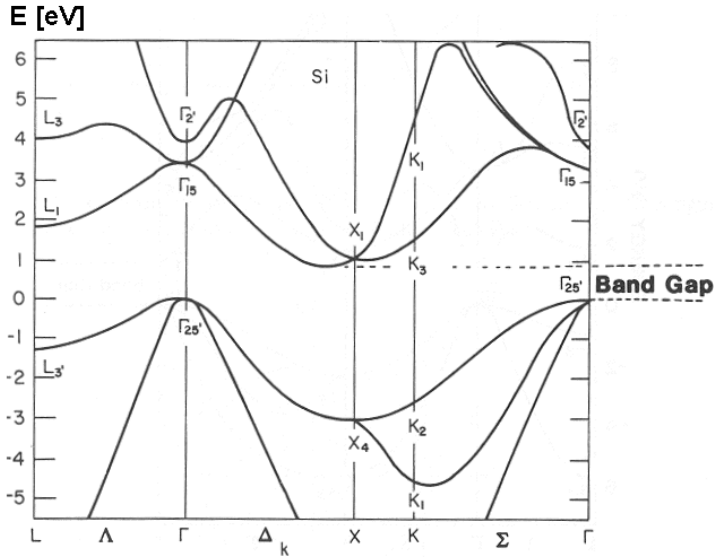


Figure 3.2 Band structure of Silicon [49].

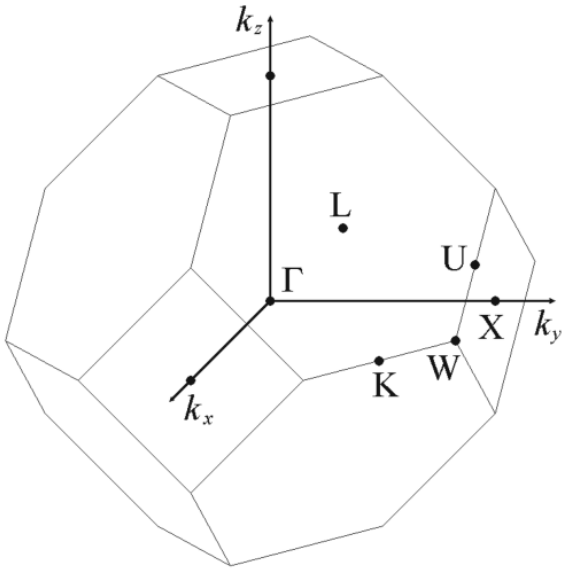


Figure 3.3 The first Brillouin zone of Silicon [50].

The band structure and the first Brillouin zone are based on the crystal lattice free of stress. The following sections will show how the stresses change the band structure of silicon.

3.2 Stress tensor

Tensors describe linear relations between two physical quantities. It can be a scalar, a vector or a matrix, depending on the order (rank) of the tensor. Stress is a force upon a unit area. The stress on an infinitesimal volume cube is shown in Figure 3.4. σ_{xx}, σ_{yy} and σ_{zz} are normal stresses, which are along the direction of surface. σ_{xy} is defined as the shear stress along x direction at the surface which out-of-plane direction is along y direction. According to the force equilibrium principal, $\sigma_{xy}=\sigma_{yx}$ and $\sigma_{zy}=\sigma_{yz}$.

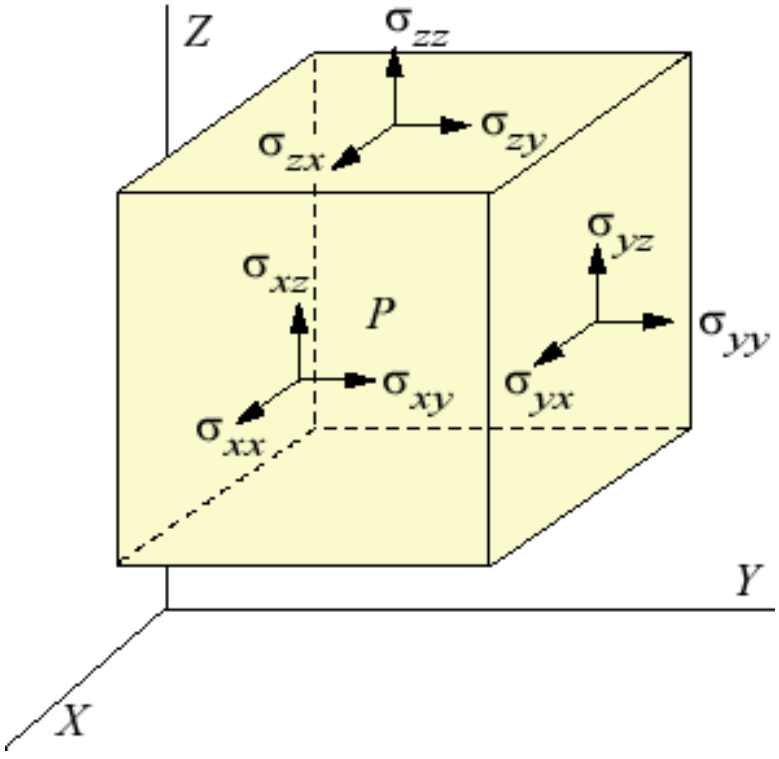


Figure 3.4 Stress components on the surfaces of an infinitesimal cube [51].

The Stress tensor is a second rank tensor of nine elements, including all of the normal stress and shear stress, which equals to,

$$\sigma = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix} \tag{3.2}$$

3.3 Strain tensor

Strain is caused by deformation and representing the relative displacement between lattice point. The strain tensor is defined as following,

$$\varepsilon = \begin{bmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} \end{bmatrix} \tag{3.3}$$

where ε_{xx}, ε_{yy} and ε_{zz} represent the distortion of along the length, the other parts represent the distortion created by rotation. Like stress tensor, according to equilibrium principal, $\varepsilon_{xy} = \varepsilon_{yx}$, $\varepsilon_{xz} = \varepsilon_{zx}$ and $\varepsilon_{yz} = \varepsilon_{zy}$. Therefore, six elements should be enough to express stress tensor and strain tensor. We can rewrite the stress and strain tensors to,

$$\varepsilon = \begin{bmatrix} \varepsilon_{xx} & \varepsilon_{yy} & \varepsilon_{zz} & \varepsilon_{yz} & \varepsilon_{zx} & \varepsilon_{xy} \end{bmatrix} \tag{3.4}$$

$$\sigma = \begin{bmatrix} \sigma_{xx} & \sigma_{yy} & \sigma_{zz} & \sigma_{yz} & \sigma_{zx} & \sigma_{xy} \end{bmatrix} \tag{3.5}$$

In the linear elastic body, Hooke's law introduces a linear relation between stress and strain, so we can get a matrix expression for the relation between stress and strain, which is shown below,

$$\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{zx}\\ \sigma_{xy}\end{bmatrix}=\begin{bmatrix}C_{11} & C_{12} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & C_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & C_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & C_{44}\end{bmatrix}\begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ \varepsilon_{yz}\\ \varepsilon_{zx}\\ \varepsilon_{xy}\end{bmatrix} \tag{3.6}$$

where the coefficients C_{ij} are called elastic stiffness constants. The elastic stiffness constants are determined by materials. It has to be pointed out that there are only three independent components for the cubic crystal for its high symmetry. In most cases, it is more common to use the inverse of the elastic stiff tensor, the compliance tensor which is defined as,

$$S=\begin{bmatrix}S_{11} & S_{12} & S_{12} & 0 & 0 & 0\\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0\\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & S_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & S_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & S_{44}\end{bmatrix} \tag{3.7}$$

where S_{ij} is called the compliance. Therefore, the new relation between strain and stress is

$$\varepsilon = S\sigma \tag{3.8}$$

From this relation listed above, strain (or stress) can be caculated, if the stress (or strain) of a material is known.

A strain tensor can be decomposed into three separate tensors,

$$\begin{bmatrix}\varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz}\\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz}\\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz}\end{bmatrix}=\frac{1}{3}\begin{bmatrix}\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz} & 0 & 0\\ 0 & \varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz} & 0\\ 0 & 0 & \varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}\end{bmatrix}$$

$$+\frac{1}{3}\begin{bmatrix}2\varepsilon_{xx}-(\varepsilon_{yy}+\varepsilon_{zz}) & 0 & 0\\ 0 & 2\varepsilon_{yy}-(\varepsilon_{zz}+\varepsilon_{xx}) & 0\\ 0 & 0 & 2\varepsilon_{zz}-(\varepsilon_{xx}+\varepsilon_{yy})\end{bmatrix} \tag{3.9}$$

$$+\begin{bmatrix}0 & \varepsilon_{xy} & \varepsilon_{xz}\\ \varepsilon_{yx} & 0 & \varepsilon_{yz}\\ \varepsilon_{zx} & \varepsilon_{zy} & 0\end{bmatrix}$$

where the first one describes the effect of a hydrostatic strain, and the last two tensors represent the shear strain. For a cubic crystal, when a uniaxial stress is applied along <100> axes, only the first type of shear strain is introduced. When there are stresses along <110> or <111>, the second type of shear strain exists plus first type of shear strain.

The hydrostatic strain only changes the volume of the cubic, the first shear strain changes the length of cubic along x, y and z, and the second shear strain rotates the axes. When only the first type shear strain is non-zero and $\varepsilon_{xx} \neq \varepsilon_{yy} \neq \varepsilon_{zz}$, the cubic deforms to an orthorhombic. If two of them equal, the orthorhombic degenerates to a tetragonal. When the second type shear strain exists and $\varepsilon_{xy} \neq \varepsilon_{yz} \neq \varepsilon_{xz}$ the cubic becomes triclinic. However, if two of the shear strain are zero, the triclinic degenerates to an orthorhombic. For example, when a biaxial stress is applied, after decomposing the strain tensor, only the hydrostatic and the first type shear strain is not zero, plus $\varepsilon_{xx} = \varepsilon_{yy}$, so the cubic changes to an tetragonal. When a stress along <110> is applied, all of the three strain tensors exist and $\varepsilon_{yz} = \varepsilon_{xz}$, so the cubic becomes the orthorhombic.

3.4 Strain effects on silicon band structure

If we know what kind of strain in silicon, how the band structure changes qualitatively can be predicted. It is possible to get a quantitive result for the band structure, but the solution requires group theory which is very complex [52], and therefore the quantitive solution will not be elaborated here. The following sections discuss two most common stresses, the biaxial stress and the <110> uniaxial stress.

Assuming the biaxial stress is in the XY plane shown in Figure 3.5.

$\sigma_{xx} = \sigma_{yy} = T$ and the rest components equal to zero. According to the relation between strain and stress get,

$$\varepsilon_{xx} = \varepsilon_{yy} = (S_{11} + S_{12})T \tag{3.10}$$

$$\varepsilon_{zz} = 2S_{12}T \tag{3.11}$$

Thus the strain tensor becomes,

$$\varepsilon = \begin{bmatrix} \varepsilon_{xx} & 0 & 0 \\ 0 & \varepsilon_{xx} & 0 \\ 0 & 0 & \varepsilon_{zz} \end{bmatrix} \tag{3.12}$$

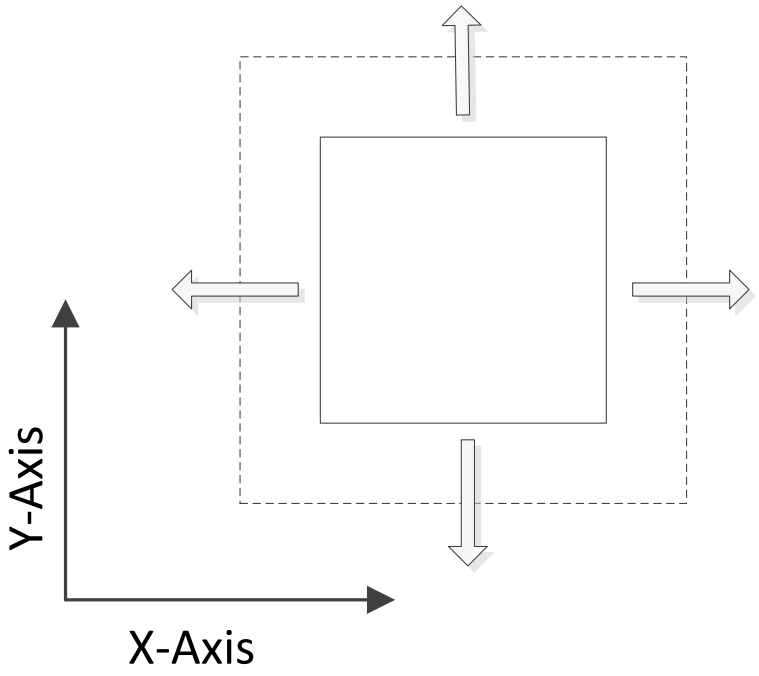


Figure 3.5 Biaxial stress .

It is obvious that only hydrostatic strain and the first shear strain exist, and the cubic lattice becomes tetragonal. For the hydrostatic strain, the shape doesn't change, but the distance between lattice points changes. As a result, the symmetry of the lattice does not change, as well as the symmetry of the

band structure, but the band gap changes. The shear strain degenerate the symmetry. The lattice constant along X and Y still equals, but the lattice constant along Z direction doesn't equal to lattice constant along X or Y, so the six degenerated Δ valleys in the conduction band split into two groups, Δ_2 (longitudinal effective mass along <001>) and Δ_4 (longitudinal effective mass along <100> and <010>). Besides the splitting of the conduction band, the degenerate heavy hole (HH) and light hole (LH) valence bands of Si also split into separate HH and LH bands. The band structure changing under a biaxial tensile stress in the shown in Figure 3.6. For the conduction band, Δ_2 is lowered and Δ_4 is lifted. For the valence band, LH is lifted and HH is lowered.

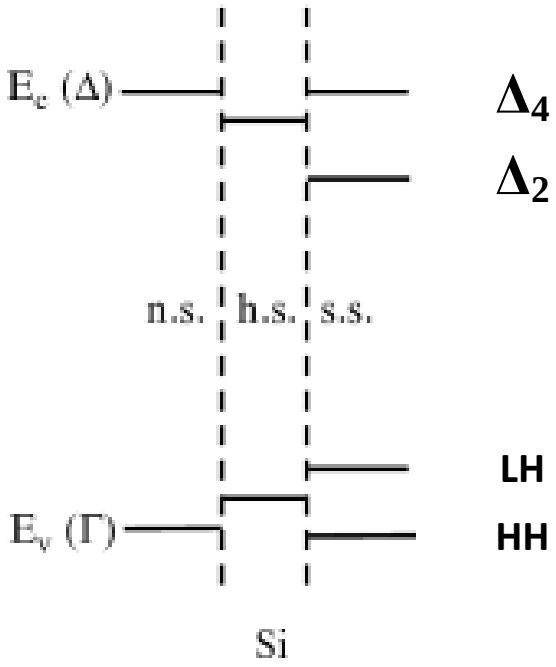


Figure 3.6 Band splitting of Si under biaxial tensile stress [52] .

For a uniaxial stress along <110> shown in Figure 3.7, $\sigma_{xx} = \sigma_{yy} = \sigma_{xy} = T/2$ and the rest are zero. Thus

$$\varepsilon_{xx} = \varepsilon_{yy} = (S_{11} + S_{12})T/2$$

$$\varepsilon_{xy} = S_{44}T/2 \tag{3.13}$$

$$\varepsilon_{zz} = S_{12}T$$

Thus the strain tensor is,

$$\varepsilon = \begin{bmatrix} \varepsilon_{xx} & \varepsilon_{xy} & 0 \\ \varepsilon_{xy} & \varepsilon_{xx} & 0 \\ 0 & 0 & \varepsilon_{zz} \end{bmatrix} \tag{3.14}$$

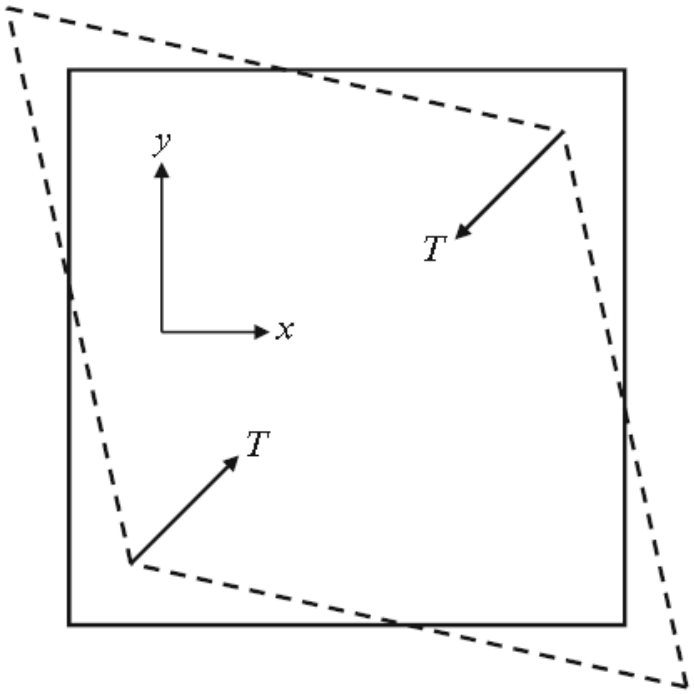


Figure 3.7 Uniaxial <110> stress [52].

The uniaxial stress introduces all of the three strains. Due to lattice constant along X and Y still are the same, and the lattice constant along Z is different, it is not difficult to get a similar conclusion that the six degenerate conduction band valleys split into Δ_2 and Δ_4, as well as the band gap changes and a splitting between the HH bands and LH bands. The band structure

under <110> uniaxial compressive stress is shown in Figure 3.8.

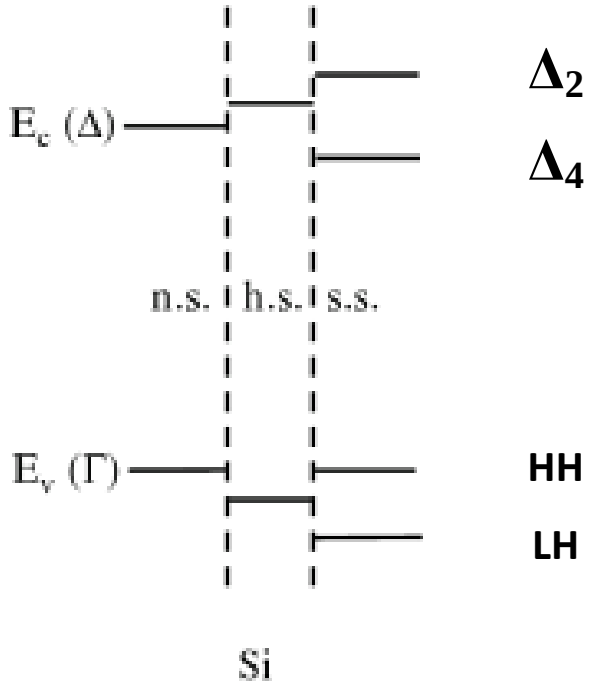


Figure 3.8 Band splitting of Si under uniaxial <110> compressive stress [52].

Band warping is another phenomenon due to the strain. Taking the conduction band valleys of silicon for example, the Δ_6 valleys are at the axes from Γ to X. Since X is at the center of the square surface, the constant energy surface at the valleys should be symmetrical around the axes, which makes the constant energy surface an ellipsoid. When a <110> uniaxial stress is applied to Si, the XY plane of the FCC lattice shifts from square to prismatic. The constant energy surface is no longer symmetrical around <001>, so the constant energy surface becomes an ellipse with major and minor axes along <110>. Figure 3.9 shows band warping under <110> uniaxial stress.

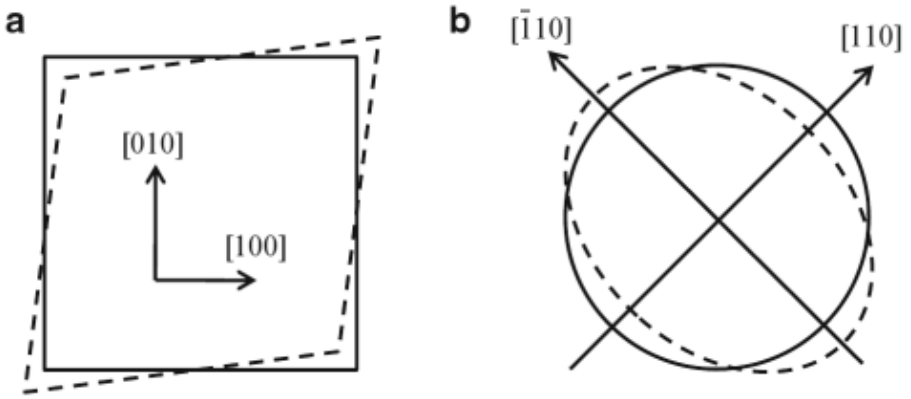


Figure 3.9 Uniaxial stress on constant energy surface. (a) Deformation under uniaxial <110> stress. (b) Constant energy contour in (001) plane [52].

3.5 Summary

Chapter 3 discusses silicon lattice and band structure, stress tensor and strain tensor, and how stress changes silicon lattice and band structure. Because silicon has an FCC cubic crystal, silicon lattice poses high symmetry. The conduction band valleys are six folded degenerated. Strain in silicon diminishes this high symmetry. Every strain tensor has three different components. They are hydrostatic strain and two types of shear strain. Hydrostatic strain does not change symmetry, only changes band gap. Shear strain destroys symmetry, which then splits degenerated bands valleys and warp bands.

CHAPTER 4

EXPERIMENTS ON MOS TUNNELING CURRENT

4.1 Introduction

This chapter will experimentally investigate MOS tunneling current strain sensor. Two approaches are employed. One is DC method. Another one is AC method. For the DC method, a semiconductor parameter analyzer Hp4156c is used, which applies DC voltage and measures DC current. For the AC method, a function generator is used to generate an AC voltage which is applied to MOS tunneling strain sensor and a TTL reference signal to the lock in amplifier. The tunneling current of MOS tunneling strain sensor is then fed into a pre-amplifier and then a lock-in amplifier. The MOS tunneling current strain sensor is made on a cantilever, which is deformed by a micrometer at the free end, and the MOS capacitor is near the fixed end. The readout of the micrometer can be converted to strain.

As discussed in Chapter 3, uniaxial <110> stress in silicon splits both conduction band valleys and valence band valleys, changing band gaps and warping band structure. Among these three effects, the first two influence tunneling current more than the band structure warping. The following sections will focus on uniaxial <110> stress influence on tunneling current.

When the gate oxide is less than 4 nm and the gate voltage is lower than 2.5V, direct tunneling current dominates. When a positive gate voltage is

applied, the gate current comes from the electrons tunneling from Si to Al. There are two different kinds of tunneling current in gate current. One is electrons tunneling from conduction band, named as ECB tunneling current. Another one is electrons tunneling from valence band, named as EVB tunneling current.

As shown in Figure 2.4, ECB tunneling current is comprised of two parts, the two-fold degenerate Δ2 group which longitudinal effective mass is along the <001> direction and the four-fold degenerate Δ4 group which transverse effective mass is along the <001> direction. When NMOS is in inversion region, electrons limited in the 2D surface become quantized. Since the longitudinal effective mass is larger than the transverse effective mass, Δ2 group has lower energy levels than that of Δ4 group. Therefore, electrons are mainly located in the ground state of Δ2, which dominates ECB tunneling current. The MOS capacitor's tunneling current through the Silicon dioxide is mainly determined by the energy barrier height between the Silicon conduction band edge and the SiO2 conduction band edge [28, 53, 54].

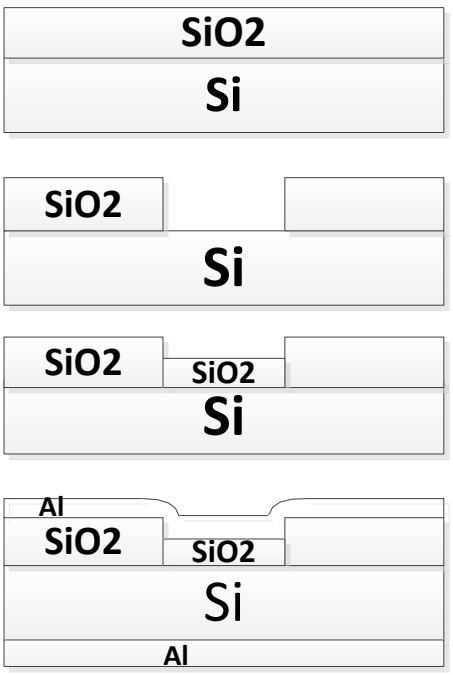
For EVB tunneling current, electrons in valence band are not confined in a 2D layer at the surface, so there is no quantization. Since valence band is full of electrons, especially when positively biased, there is no repopulation when uniaxial stress is applied. EVB tunneling current is also comprised of two components, J_{hh} and J_{lh}. J_{hh} has a heavy hole effective mass. J_{lh} has a light hole effective mass. Like ECB tunneling current, EVB tunneling current is also determined by barrier height which is the difference between SiO_2 conduction band and Si valence band, and out-of-plane effective mass.

When a negative voltage is applied on Al, the tunneling current is

composed by electrons tunneling from Al to Si and holes tunneling from Si to Al as shown in Fig. 2.4 (b). Because the barrier height of holes in Si is higher than that of electrons in Al, the tunneling current mainly depends on the electrons from Al. The tunneling current is then only determined by Al's work function. Uniaxial tensile strain causes Al's work function to decrease, so the tunneling current increases. Uniaxial compressive strain causes Al's work function to increase, so the tunneling current decreases.

4.2 Fabrication and Measurement setup

Figure 4.1 shows the fabrication process of a cantilever beam with a tunneling oxide. The starting wafer is a heavily doped P-type (100) Silicon wafer, which is around 500 um thick. A 500 nm thick thermally grown oxide layer is patterned by wet etching. Then, a thin oxide layer (around 3.8 nm) is grown with an area of 1 mm^2. Finally, Aluminum is sputtered and patterned as contacts. The length of the device is around 2 cm, and the width is 0.5 cm.



(a)

(b)

Figure 4.1 Fabrication process and the figure of MOS tunneling current strain sensor. (a). Fabrication process; (b). Picture of the device.

To minimize noise in MOS tunneling current, a very high quality gate oxide is desired. Four different methods are employed to grow gate oxide. They are PECVD, ALD, RTP and dry oxidation in furnace. Among these methods, it is found that dry oxidation in furnace provides the highest quality. At 800 ^{o}C, a heavily doped p type wafer grows 2.4 nm thick oxide in one minute. The uniformity of gate oxide can be characterized by an ellipsometer. Figure 4.2 shows that five positions on a wafer are chosen for the uniformity measurement. Table 3 gives the measurement result.

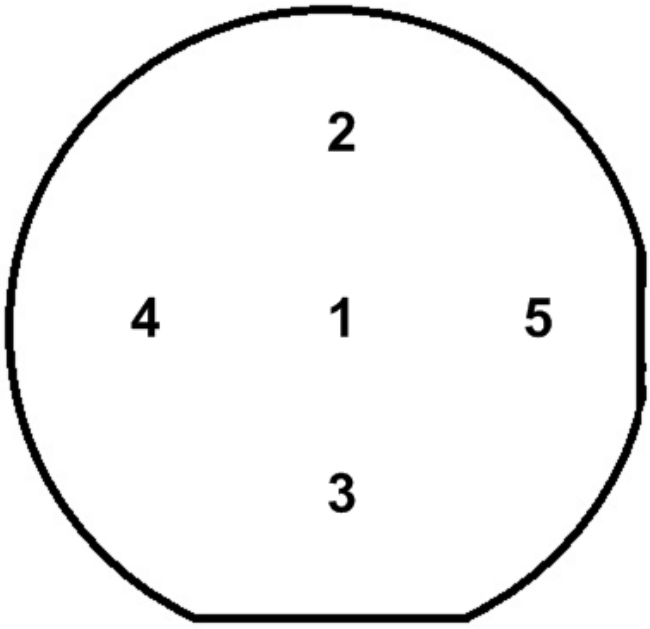


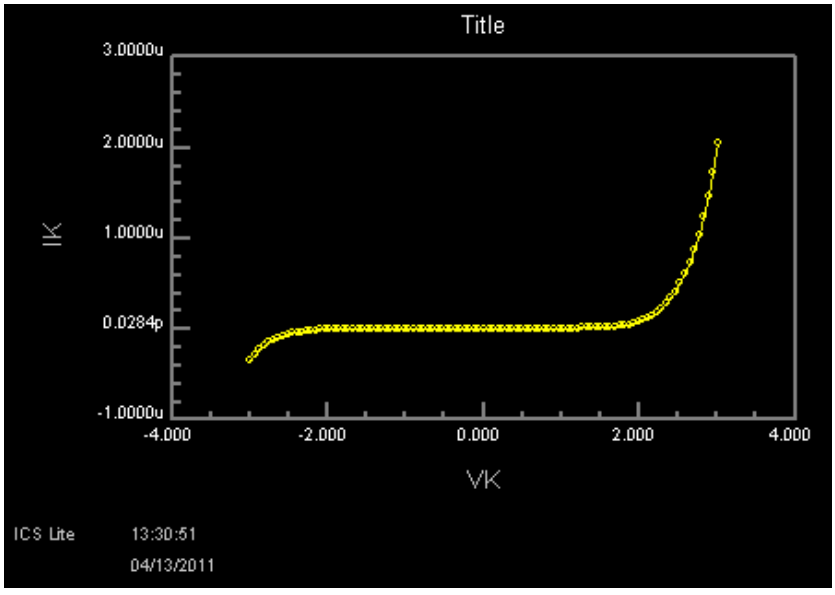
Figure 4.2 P type wafer for uniformity measurement using ellipsometer.

Table 3

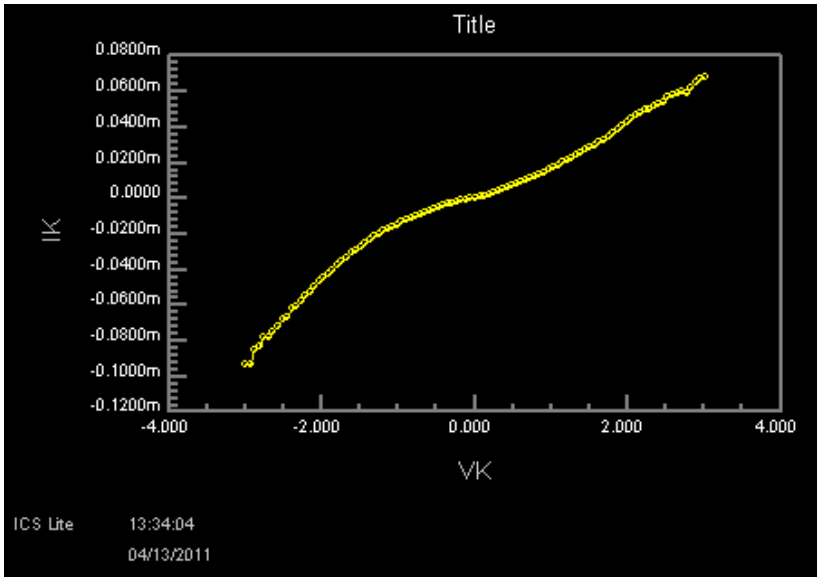
Uniformity measurement result

Positions	Thickness (nm)
1	2.38
2	2.45
3	2.39
4	2.41
5	2.39

One quick method to know whether the gate oxide is good or not is to measure current vs. gate voltage (IV curve). Figure 4.3 (a) shows a good gate oxide, which IV curve is more like log function. Figure 4.3 (b) shows a bad gate oxide, which IV is close to linear function. Besides, the current of good device is much smaller than the bad device. However, a device with a log function like IV curve does not mean the device has a very high quality gate oxide. Further measurement like noise characterization is needed, which will be discussed in later sections.



(a)

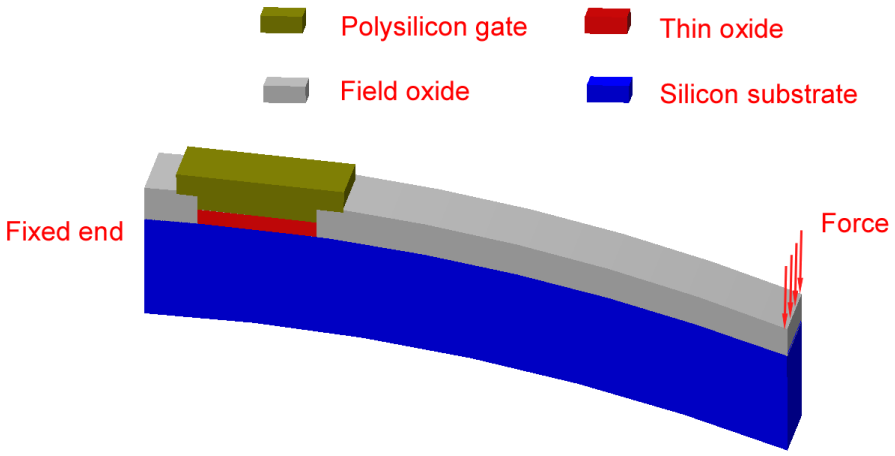


(b)

Figure 4.3 IV curve for MOS capacitor. (a). Good device; (b). Bad device.

Figure 4.4 shows the measurement setup. One end of the beam was glued to a metal stage by conductive epoxy, while the other end was deformed by scrolling a micrometer. The MOS capacitor is located in the fixed end. The micrometer positions are converted to strain. The tunneling current was recorded by an HP4156c Semiconductor Parameter Analyzer. Both uniaxial tensile strain and uniaxial compressive strain are in the <110> direction.

(a)



(b)

Figure 4.4 Photograph of measurement setup, and illustration of MOS tunneling current strain sensor using cantilever beam. The MOS device is near the fixed end. (a). Measurement setup; (b). Illustration of MOS tunneling current strain sensor using cantilever beam.

All the measurements were done by increasing the strain from 0% to 0.112% at the step of 0.016%, and then decreasing the strain from 0.112% to 0% at the step of 0.016%. During each step, there are 25 samples with a sampling time of 2 seconds.

4.3 DC experiments of strain effects on tunneling current

The results of tensile strain and compressive strain are given in the Table 4, Figures 4.5 & 4.6 and Figures 4.7 & 4.8 respectively. The blue solid lines are the measured tunneling currents, which drifts with time. Since in the beginning the currents decrease or increase sharply, only data captured after 50 seconds which is stable, is considered. To calculate noise and sensitivity, drift has to be removed which is shown as the red dot line. There are some

spikes in the measured results of 1V, 0.5V and -1V. These spikes appear at the time that the strains are changed, which are introduced by human body and are ignored in the analysis.

Table 4

Analysis of experiment data

Voltages (V)	Avg (nA)	SD (A)	$\frac{\mathbf{SD}}{\mathbf{avg}}$ (%)	$\mathbf{\Delta Ig/Ig}$ 200 MPa (%)	GF	Drift rate (% per minute)
2 (tensile)	76.22	1.7E-11	0.022	-2.5	22.3	0.456
1.5	14.17	5E-12	0.03	-2.0	17.8	0.413
1	1.415	1.0E-13	0.007	-2.2	19	0.124
0.5	0.031	2.3E-13	0.7			-0.104
-1	0.147	3.6E-13	0.24	0.38	3.4	-0.52
2 (compressive)	75	2.0E-11	0.026	2.1	19	0.416
1	1.085	4.4E-13	0.04	1.8	16	0.608
0.5	0.039	1.5E-14	0.038	1.2	11.2	-0.464
-1	0.155	1.1E-13	0.07	-0.38	3.4	-1.48

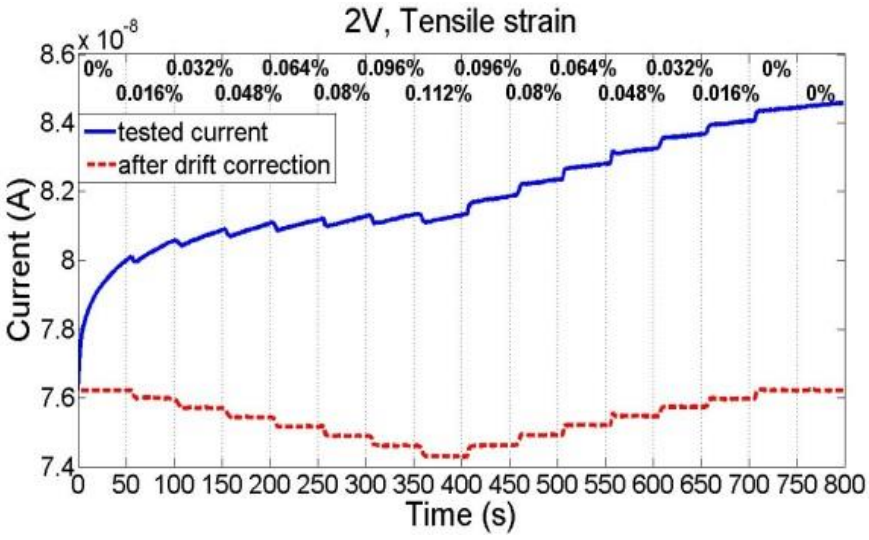
Table 4 analyzes noise (SD or SD/avg), sensitivity (ΔIg/Ig or GF) and drift. Here avg is the average tunneling current of 25 samples with a sampling time of two seconds at zero strain. SD is standard deviation of 25 samples with a sampling time of two seconds at zero strain. Drift which unit is % per minute is calculated from 50 seconds to 800 seconds. Drift shows that tunneling current changes slowly even when there is no strain. GF is the gauge factor which equals to $\frac{\Delta Ig/Ig}{\varepsilon}$, where $\varepsilon = 0.112\%$.

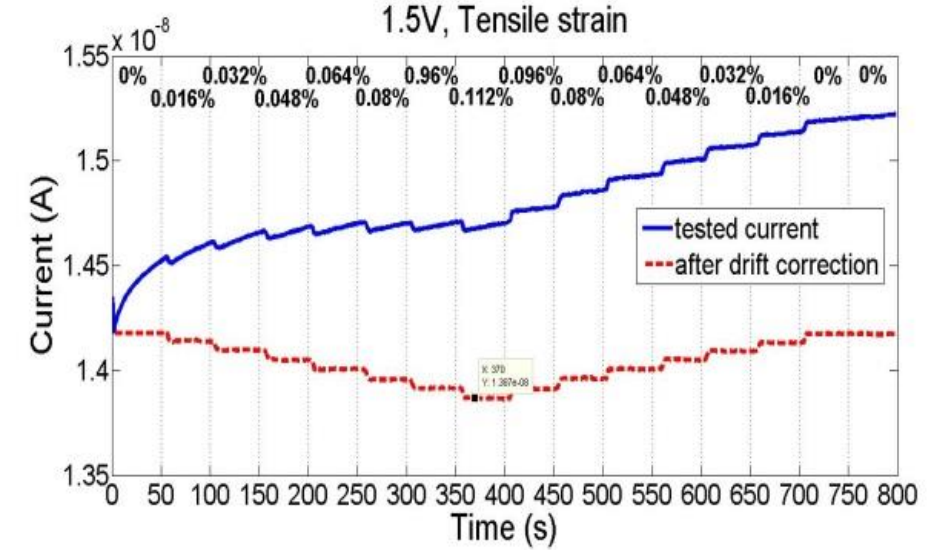
4.3.1 Tensile strain

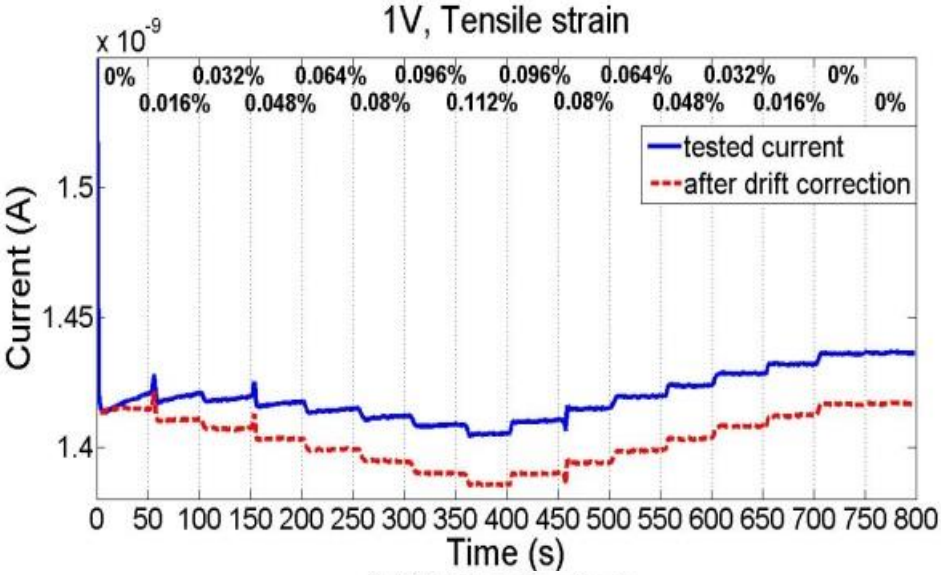
From the analysis in the Table 4 and Figure 4.5, it can be seen that tunneling current increases as gate voltage increases. The noise or SD decreases two orders of magnitude from 0.5V to 1V, and it keeps the same order of magnitude from 1V to 2V. SD/avg at 2V is 0.022%, which means a

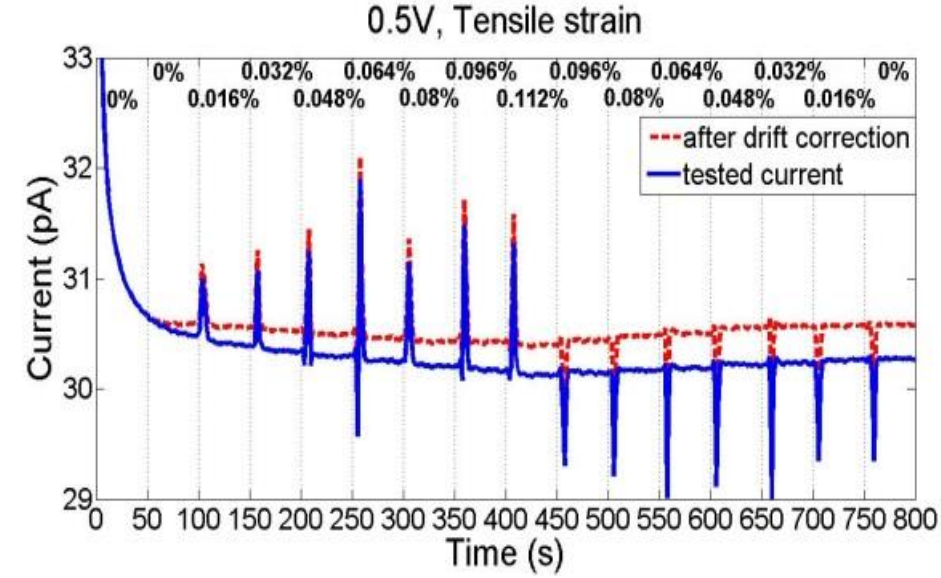
strain induced current changing less than 0.022% at 2V cannot be measured. The sensitivity at 2V at the strain of 0.112% is -2.5%. Therefore, if minimum detectable strain at 2V equals to 0.112% / (2.5% / 0.022%), which is 0.001%. Likewise, the minimum detectable strain at 1V is around 0.0005%. The minimum detectable strain at 0.5V and -1V are around 0.112%, which are large.

The current drifting is observed. Table 4 and Figure 4.5 show that the drift rate changes from negative to positives as gate voltage increases from 0.5V to 2V. From 1V to 2V of tensile experiment, it seems like drift rate increases. However, as find in compressive experiment, from 1V to 2V, drift rate decreases a little bit. Since the same device is used, the drift rate should show the same result, but it did not. Therefore, drift in tunneling current need more experiment to characterize.




1.5V, Tensile strain
x 10^-8
0% 0.032% 0.064% 0.96% 0.096% 0.064% 0.032% 0% 0%
0.016% 0.048% 0.08% 0.112% 0.08% 0.048% 0.016%
tested current
after drift correction
Current (A)
Time (s)


1V, Tensile strain
x 10^-9
0% 0.032% 0.064% 0.096% 0.096% 0.064% 0.032% 0%
0.016% 0.048% 0.08% 0.112% 0.08% 0.048% 0.016% 0%
tested current
after drift correction
Current (A)
Time (s)


0.5V, Tensile strain
0% 0.032% 0.064% 0.096% 0.096% 0.064% 0.032% 0%
0% 0.016% 0.048% 0.08% 0.112% 0.08% 0.048% 0.016%
after drift correction
tested current
Current (pA)
Time (s)

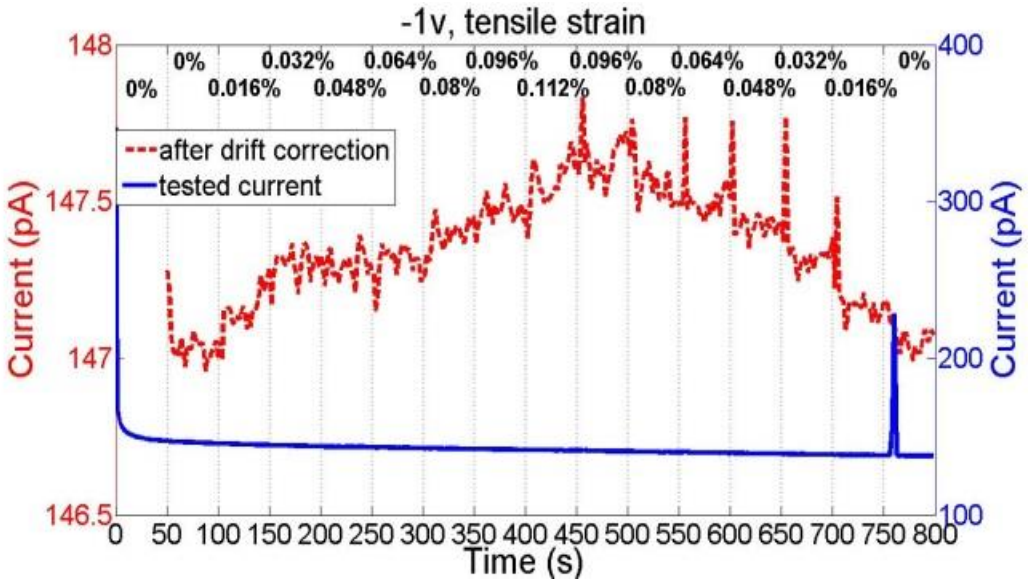
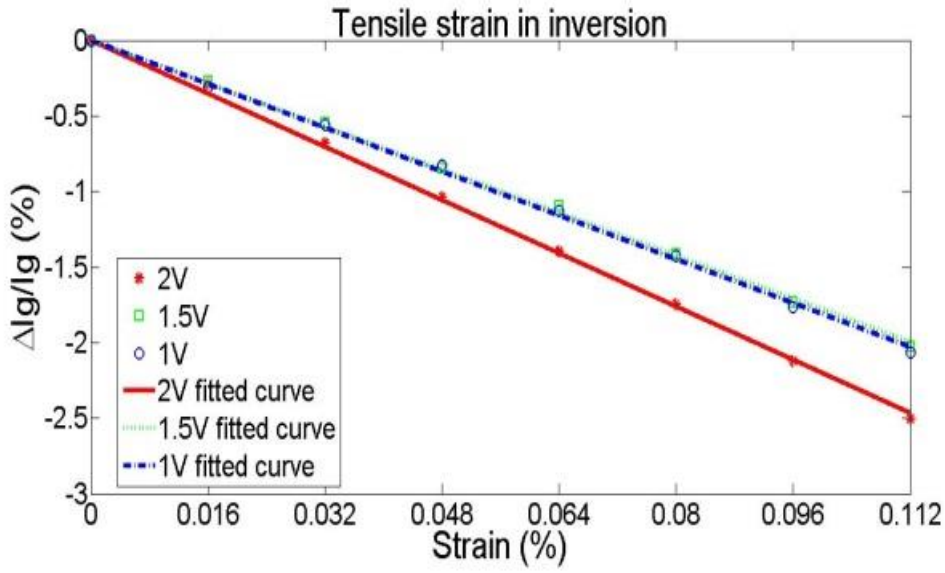


Figure 4.5 Tunneling current versus time at different gate voltages and different tensile strain.

In Figure 4.6, as the theories predict, tensile stress causes the MOS tunneling current to decrease at the positive voltage. In the other hand, tensile stress causes the MOS tunneling current from metal to Silicon to increase at the negative voltage. The sensitivity (ΔIg/Ig) and gauge factor decreases from 1V to 1.5V, but increases from 1.5V to 2V.



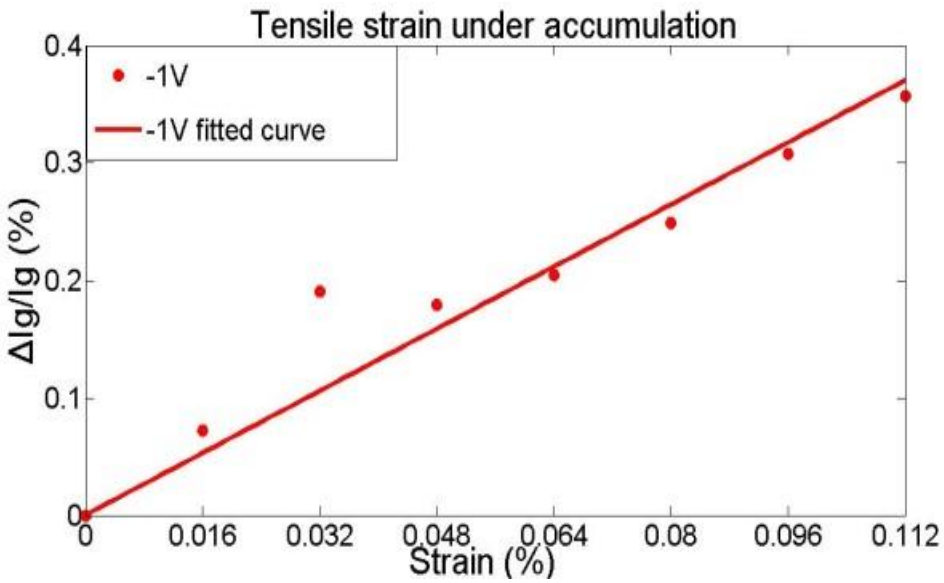
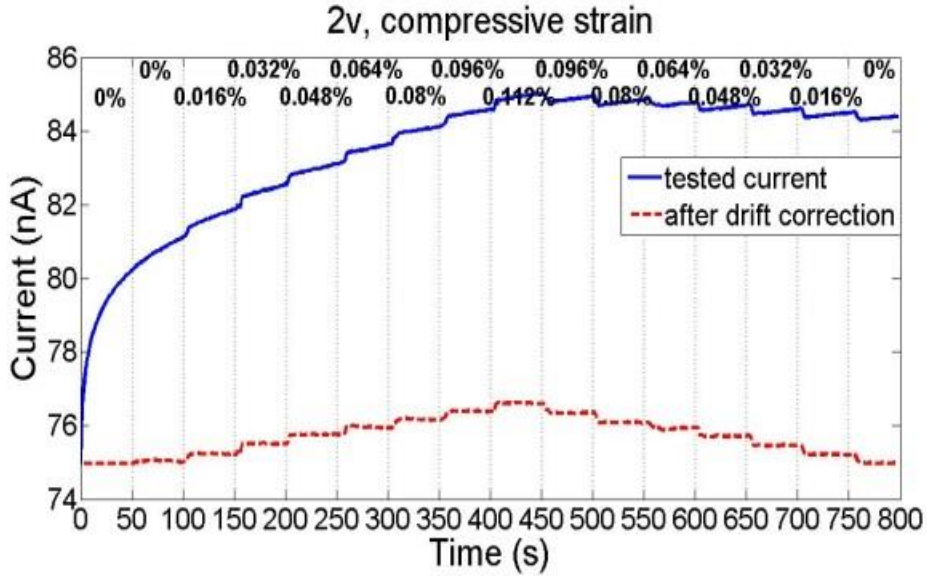


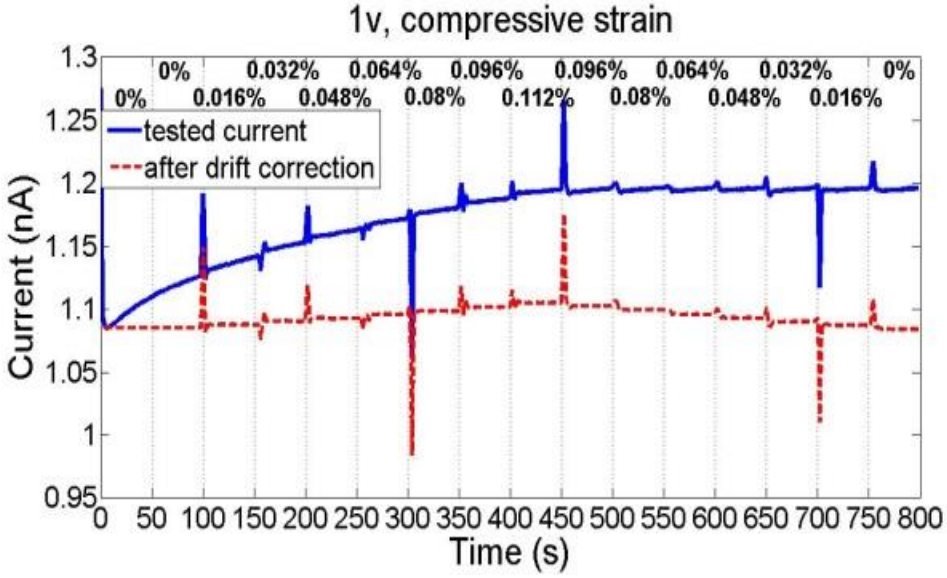
Figure 4.6 Tunneling current change versus tensile strain.

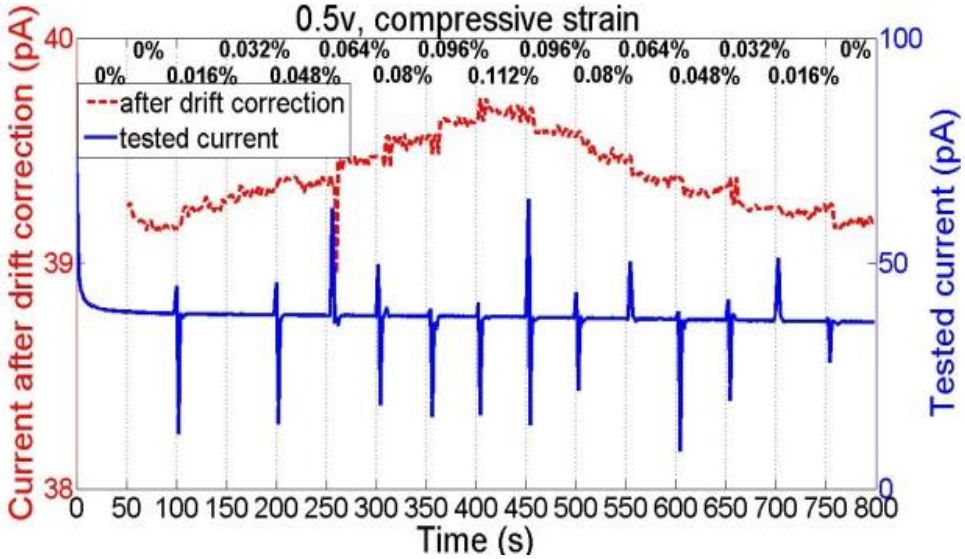
4.3.2 Compressive strain

Figures 4.7 & 4.8 show that the compressive stress responses are contrary to the tensile stress responses. Compressive stress causes MOS tunneling current to increase at positive gate voltages, while decrease at negative gate voltages.

Since the same device is used for both tensile and compressive stress measurement, the SD should be close to those of tensile strain. However, the SD at 1V is four times larger than that of tensile strain, while the SD at 0.5V is ten times smaller and the SD at -1V is three times smaller. The difference may come from the electrode contact or environment like temperature, since the compressive strain measurement was conducted at different time. Sensitivity at 2V and 1V are better than those at 0.5V and -1V.


2v, compressive strain
0%
0.032%
0.064%
0.096%
0.096%
0.064%
0.032%
0%
0%
0.016%
0.048%
0.08%
0.112%
0.08%
0.048%
0.016%
tested current
after drift correction
Current (nA)
Time (s)


1v, compressive strain
0%
0.032%
0.064%
0.096%
0.096%
0.064%
0.032%
0%
0%
0.016%
0.048%
0.08%
0.112%
0.08%
0.048%
0.016%
tested current
after drift correction
Current (nA)
Time (s)


0.5v, compressive strain
0%
0.032%
0.064%
0.096%
0.096%
0.064%
0.032%
0%
0%
0.016%
0.048%
0.08%
0.112%
0.08%
0.048%
0.016%
after drift correction
tested current
Current after drift correction (pA)
Tested current (pA)
Time (s)

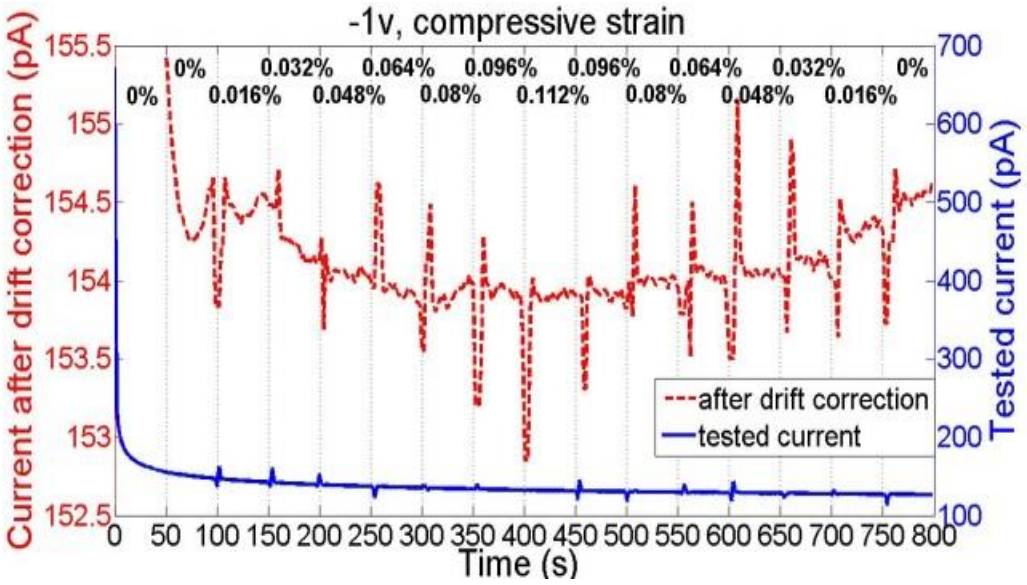
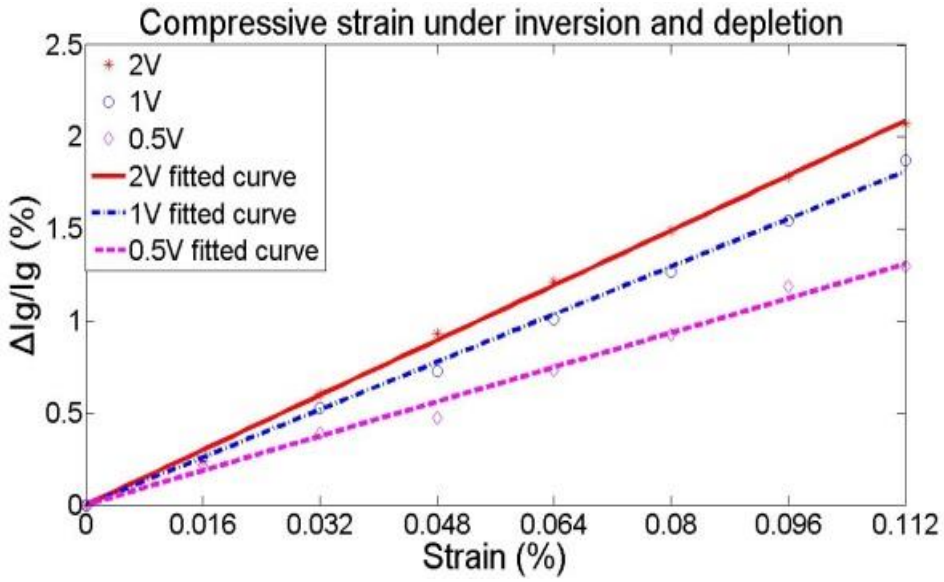


Figure 4.7 Tunneling current versus time at compressive strain.



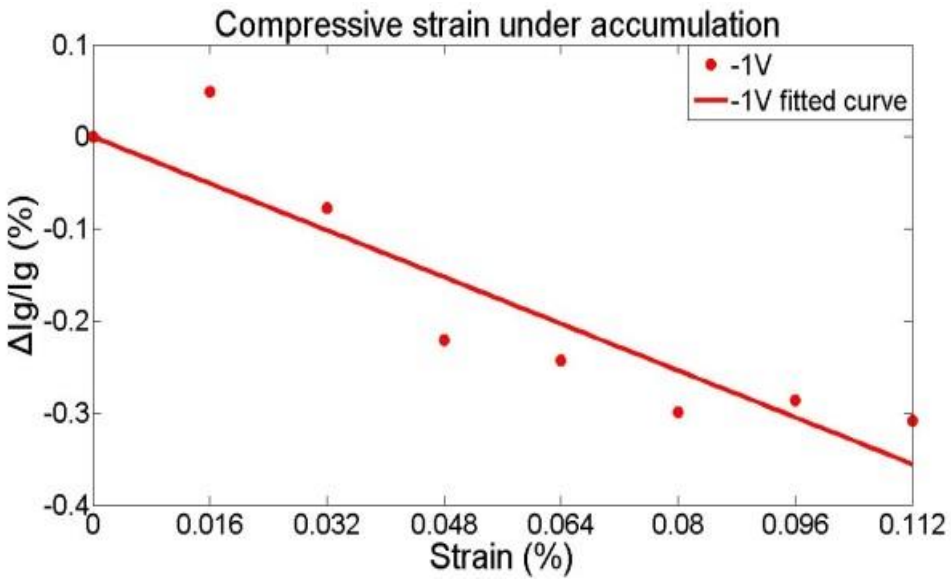


Figure 4.8 Tunneling current change versus compressive strain.

4.3.3 Discussion

As part of the experiment, noise, sensitivity and drift of MOS tunneling current strains sensor were studied. Noise of positively biased tunneling current is less than that of negatively biased tunneling current. Besides, noise decreases as gate voltage increases. Tensile stress decreases positively biased MOS tunneling current, and increases negatively biased MOS tunneling current. Compressive stress shows an opposite effect on MOS tunneling current. Sensitivity of MOS tunneling current strain sensor increases as gate voltage increases. However, under tensile stress, sensitivity of positively biased MOS tunneling current strain sensor decreases a little and then increases. Drift does not show a clear pattern from the experiment, which requires further study.

Since it is preferred for noise as small as possible, it is better to let MOS tunneling current strain sensor work in inversion region. The following sections will show the building of models for ECB tunneling current and EVB

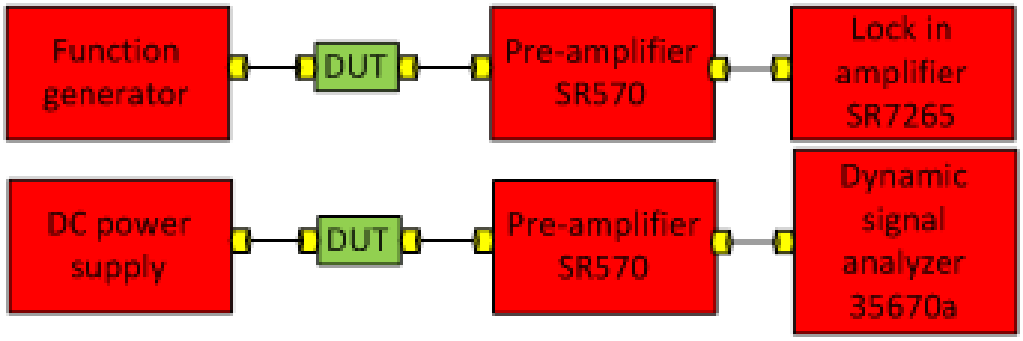
tunneling current to theoretically study sensitivity of MOS tunneling current strain sensor in inversion region.

4.4 AC experiments of strain effects on tunneling current

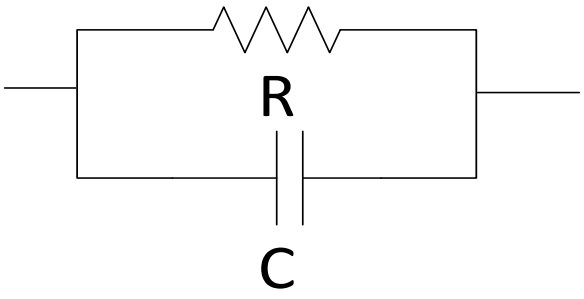
During the DC experiment of strain effects on tunneling current, strain was measured by measuring the strain-induced tunneling current changing through a Metal-Oxide-Semiconductor sandwich from a DC voltage. To overcome the electronic noise, substantial averaging was utilized. In this section an improved method of measuring the strain from the tunneling current is demonstrated in which an AC signal is utilized, and the AC current is measured. This approach substantially reduces the noise by avoiding the 1/f noise. The optimal conditions for the AC technique are to use a high frequency to avoid 1/f noise and a low DC bias. The MOS tunneling current strain sensor used to compare the performance has a 2.3 nm thick SiO_2 gate oxide. To compare the performance, both DC method and AC method are performed. Only uniaxial <110> tensile stress at positive bias is studied, which is enough to compare the performance to DC method. The way to apply stress to the device is the same as Figure 4.4.

4.4.1 The principle of AC measurement

The setup of the AC measurement is shown in Figure 4.9. A function generator is used to generate a sine wave AC voltage and a TTL reference signal. The AC voltage is applied to the device. Tunneling current from the device is fed into a pre-amplifier and lock-in amplifier. The silicon cantilever is deformed by a micrometer at the free end, and the micrometer positions are converted to strain.



(a)



(b)

Figure 4.9 (a) The top one is the setup for strain measurement and the bottom one is the setup for noise spectrum measurement. (b) The equivalent circuit for a MOS tunneling sensor.

A lock in amplifier is an efficient tool to extract signal from noise. The noise reduction depends on the bandwidth (time constant, τ) of low pass filter and the modulation frequency. The general principal of lock in amplifier can be described by the following equations. The equivalent circuit of the MOS tunneling device is a RC network in parallel (Figure 4.9(b)), so the signal from the preamplifier and the reference from the function generator are,

$$V_s = V_0 \cos(w_0 t) + V_1 \sin(w_0 t) + \delta_t \quad (4.1)$$

$$V_{ref}=cos(w_0t+\phi) \tag{4.2}$$

where $V_0cos(w_0t)$ is the signal from the resistor, $V_1sin(w_0t)$ is the signal from the capacitor, δ_t is the noise, ϕ is the phase delay between reference channel and signal channel and V_{ref} is the reference signal. After supplying both signal and reference to the lock in amplifier have

$$\begin{aligned} V_sV_{ref}&=(V_0cos(w_0t)+V_1sin(w_0t)+\delta_t) cos(w_0t+\phi) \\ &=1/2V_0cos(\phi)+1/2V_0cos(2\, w_0t+\phi)\ldots \\ &+1/2V_1sin(\phi)+1/2V_1sin(2\, w_0t+\phi)\ldots \\ &+\delta_t\, cos(w_0t+\phi) \end{aligned} \tag{4.3}$$

After a low pass filter, the final signal becomes,

$$V=1/2V_0cos(\phi)+1/2V_1sin(\phi) \tag{4.4}$$

The signal is $1/2V_0cos(\phi)$, however due to the phase delay, the final signal includes a signal from the capacitor. If V_1 is close to V_0, the influence from the capacitor could be very large, and it will harm the accuracy of measurement. There are several sources causing this phase delay, like the amplifiers and the BNC cables. In our measurement, the major phase delay comes from the function generator, Agilent 33220a, which means the phase of the AC voltage and the TTL reference signal are not same. This phase delay varies with frequencies. For example, there is a 15 degree delay at 1 kHz compared to 1 Hz. In order to get an accurate signal, it is necessary to exclude the phase delay by adjusting the phase of the reference channel of the lock in amplifier.

4.4.2 Results and discussion

4.4.2.1 Noise and drift current

Before using lock in amplifier, a proper modulation frequency must be determined by the analysis of the noise spectrum of the device. The noise spectrum at a DC voltage of 0.7 V is shown in Figure 4.10. From the noise spectrum, we find that there is a 1/f noise in the low frequency region. It should be expect that the as the modulation frequency moves from the low frequency region to the white noise region, the noise should drop.

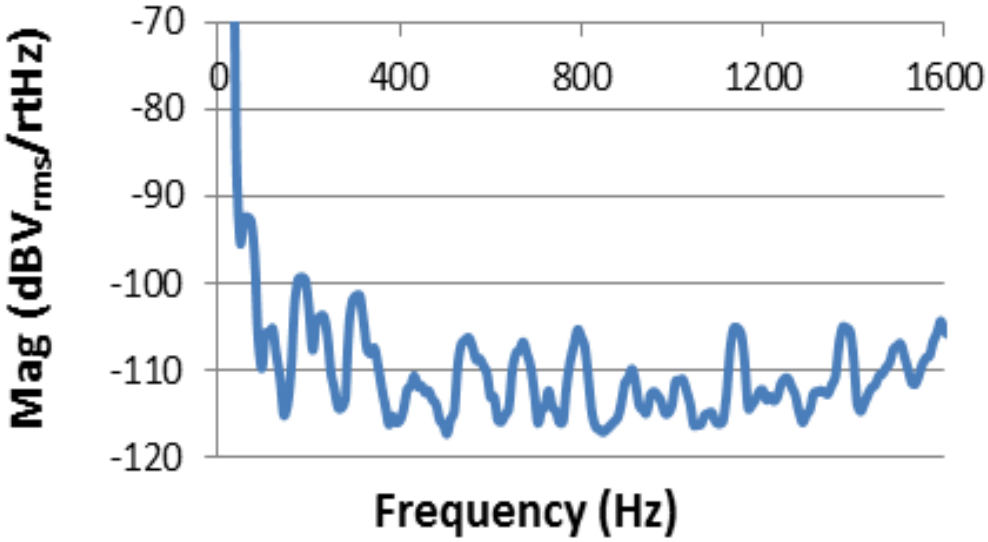


Figure 4.10 Noise spectrum.

The modulation frequencies we choose are 10 Hz, 100 Hz and 1 kHz, and the time constant is kept at 100 ms. The gain of the preamplifier is 5 μA/V, which provides a 10 kHz band width. The measurement results are shown in Figure 4.11, and the standard deviations/average (SD/avg) are given in Table 5. Both standard deviation and average are calculated from 50 continuous samples. It is clear that when the modulation frequency changes from the 1/f noise region to the white noise region, the noise decreases.

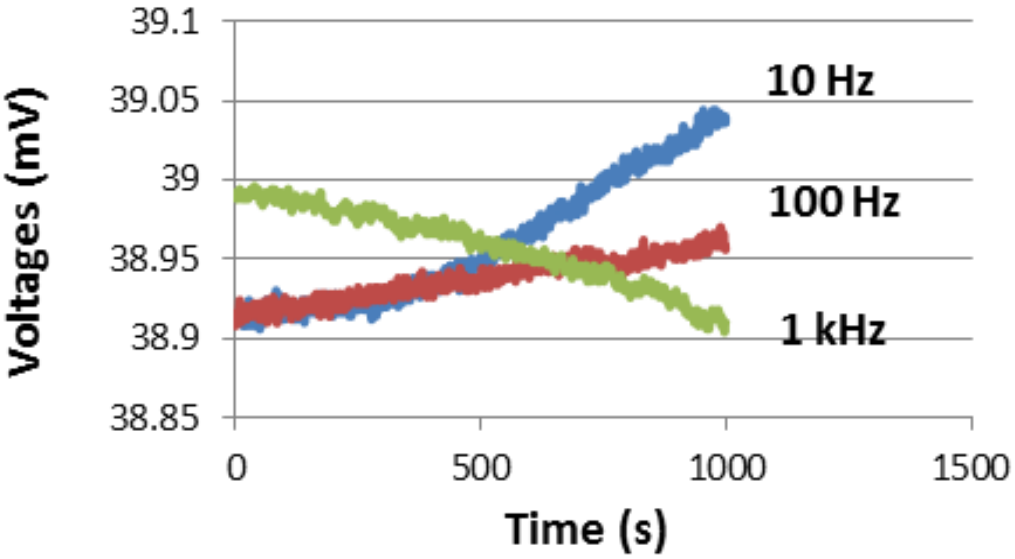


Figure 4.11 AC measurement at different frequencies when the time constant is 100 ms.

Table 5

Noise measurement at different frequencies

	10 Hz	**100 Hz**	**1 kHz**
SD/avg	0.012%	0.009%	0.002%

Figure 4.11 also show that the drift tunneling current observed in the DC method is not improved by the AC measurement, which can be explained by the following equations. Adding a modulation signal to (4.1) and only consider the resistor part get

$$V_s' = \cos(w_1 t) V_0 \cos(w_0 t) \quad (4.5)$$

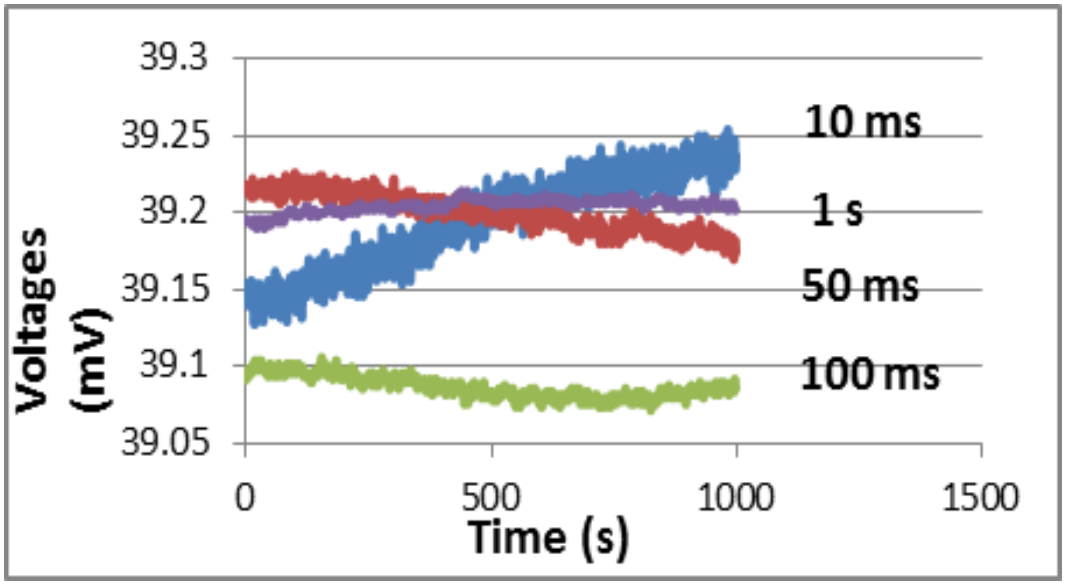
where $cos(w_1 t)$ is introduced by the drift tunneling current and w_1 is usually a very small frequency which is far less than w_0. The drift tunneling current may not be a simple sine wave, but if the drifting is very slow, an assumption of a

sine wave is enough for the analysis. According to our experiment, it is true that the drifting is at a very low frequency which is far less than 1 Hz. The output of lock in amplifier is,

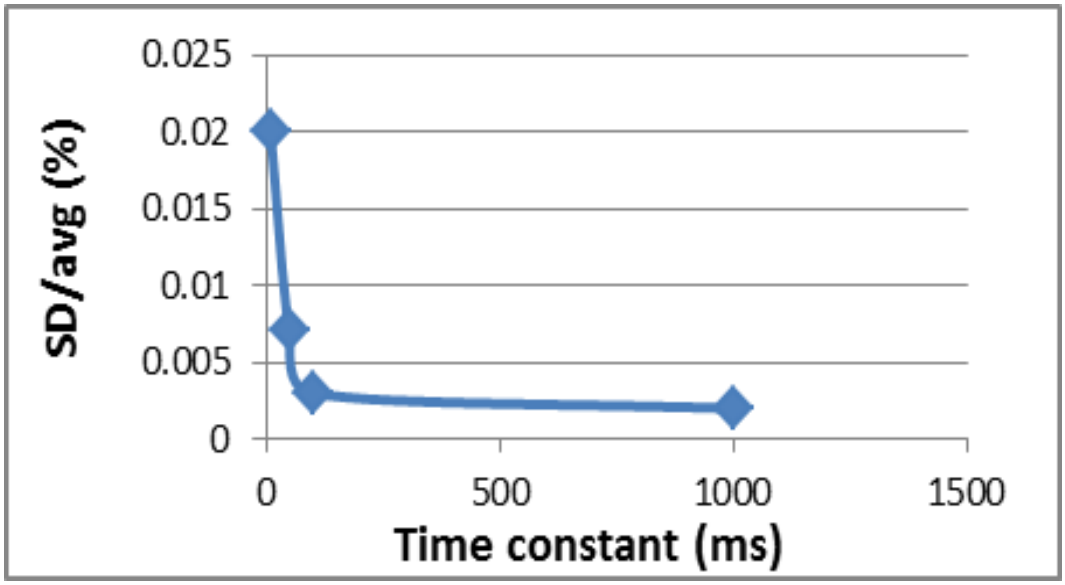
$$V' = 1/2\cos(w_1 t) V_0 \cos(\phi) \quad (4.6)$$

Thus the AC measurement using lock in amplifier cannot get rid of the drift tunneling current.

To see the effects of the time constant, 1 kHz is chosen as the modulation frequency and vary time constant τ from 10 ms to 1 s. Figure 4.12 and Table 6 show the results. The noise decreases substantially as the time constant is increased. In Table 6, the noise observed from the DC measurement (Figure 4.14(a)) is also included. The time constant of DC measurement is 0.6 s, and its noise is close to that of the AC method at 0.08 s. To have a noise of 0.005%, AC method is almost eight times faster than the DC method. Figure 4.12(b) shows that noise reduction below 100 ms is more efficient.



(a)



(b)

Figure 4.12 (a) AC measurement of different time constant at 1 kHz; (b) SD/avg vs. time constant.

Table 6

Noise measurement at different time constant

	10 ms	50 ms	100 ms	1 s	DC
SD/avg	0.02%	0.007%	0.003%	0.002%	0.005%
SD/avg/τ	2%	0.14%	0.03%	0.002%	0.008%

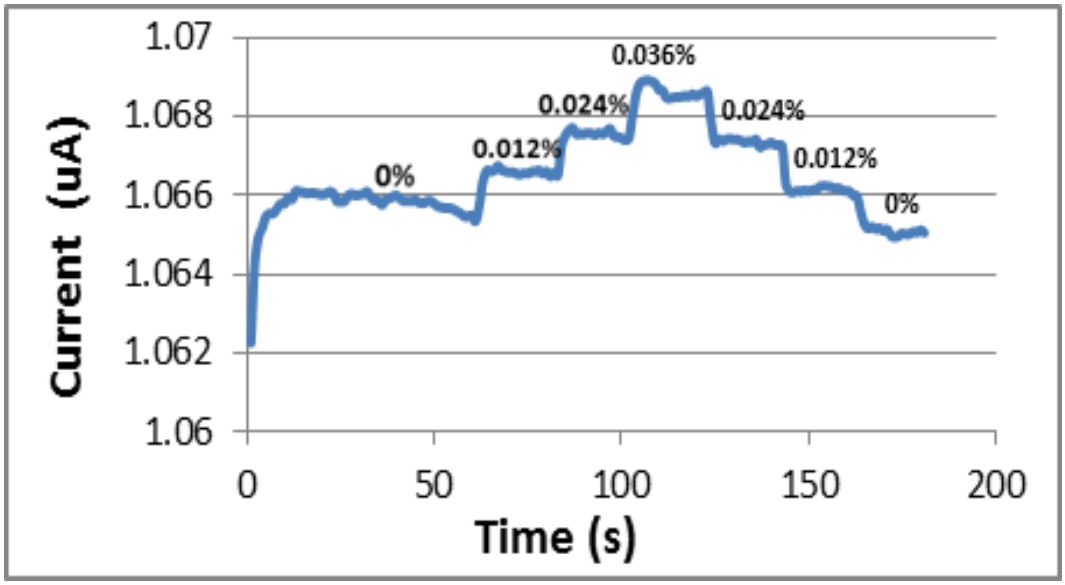
4.4.2.2 Sensitivity

The sensitivity for both the DC and the AC method is defined as ΔIg/Ig, where Ig is the tunneling current. Although it is the voltage from the lock in amplifier that is measured for the AC method, ΔIg/Ig equals ΔVg/Vg.

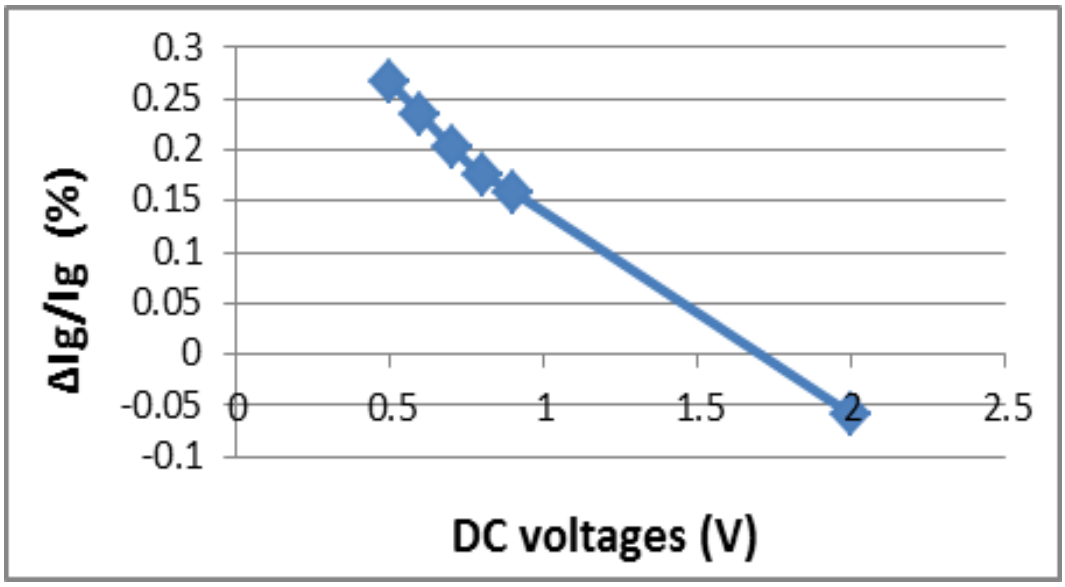
Figure 4.13(a) presents how the tunneling current at Vdc=0.7 V changes with the tensile strain which is along [110] direction. The strain is increased from 0% to 0.036% and then decreased to 0% at a step of 0.012%. The same procedure is also applied to the DC voltages at 0.5 V, 0.6 V, 0.8 V,

0.9 V and 2 V. Figure 4.13(b) shows how the sensitivity changing with the DC voltages at the strain of 0.012%. As the theory predicts, the sensitivity drops and eventually becomes negative.

The amplitudes of AC voltages chosen for the AC measurements are 20 Vrms, 50 Vrms, 100 Vrms and 200 Vrms, while the device is biased at 0.7 V. The results are given in Figure 4.14. The measurement procedure is the same as the DC measurement. Figure 4.14(b) shows that the sensitivity of AC method first increases, but then decreases with the increasing of the AC amplitude. This can be explained by that the AC method measures the slope of the current vs. voltage curve of the DC method. Taking 20 mV as an example, as the amplitude is small, the current is determined by both the high peak 0.7+0.028=0.728 V and the low peak 0.7-0.028=0.672 V. At tensile strain, the sensitivity at the low peak is larger than that of the high peak, which in turn reduces the slope changing, so the sensitivity is reduced. As the amplitude increases, the influence from the low peak weakens and the sensitivity tries to increase, but the sensitivity at high peak decreases, so there is a competition. When the amplitude is smaller than 100 mV, the low peak weakening has more influence on the sensitivity, so we see the sensitivity increase. When the amplitude is larger than 100 mV, the sensitivity at high peak dominates, decreasing sensitivity is observed. As a result, the AC method will have a lower sensitivity than the DC method at the same DC offset.

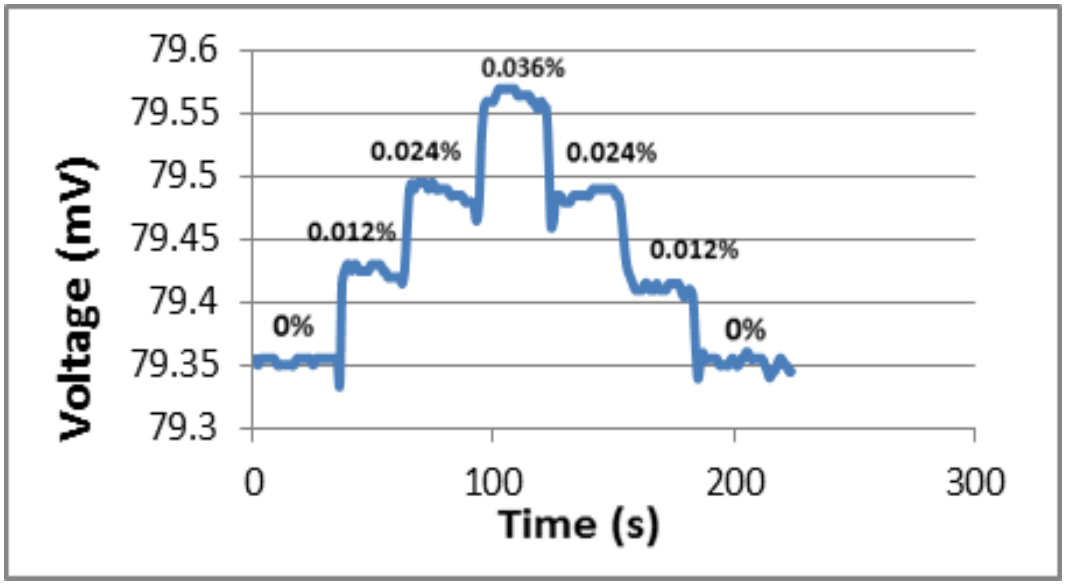


(a)

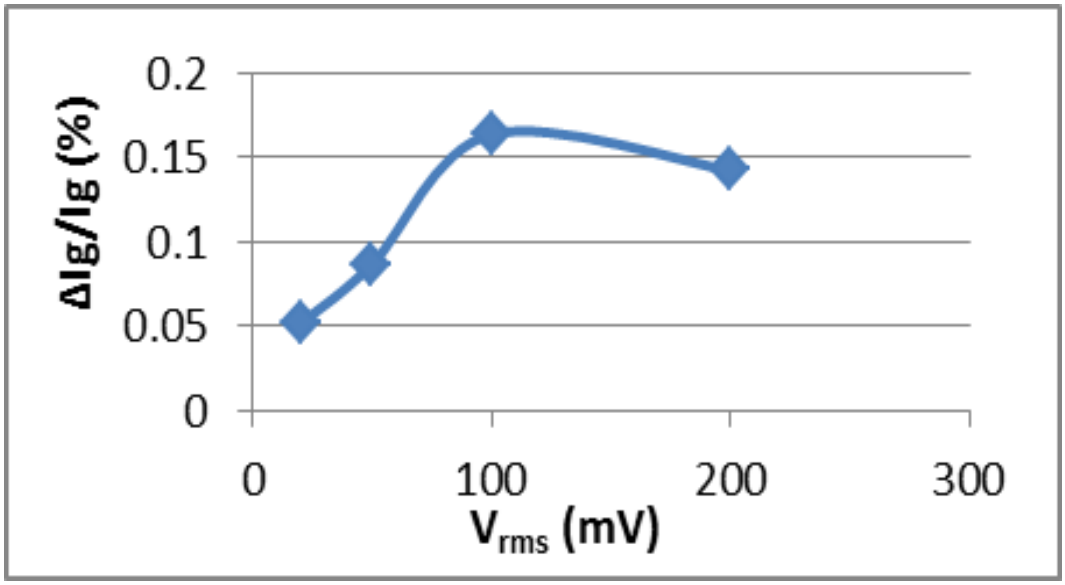


(b)

Figure 4.13 DC method. (a) tunneling current at V_{dc}=0.7 V; (b) strain response at different DC voltages at the strain of 0.012%.



(a)



(b)

Figure 4.14 AC method. (a) tunneling current at Vrms= 100 mV, Vdc=0.7 V and 1 kHz; (b) strain response at different DC voltages at the strain of 0.012%.

4.4.3 Conclusions

The DC and the AC measurement techniques for the MOS tunneling strain sensor are compared, and it is found that AC method has a better performance in noise reduction. When the modulation frequency used in the AC measurement is far from the 1/f noise, the AC measurement technique is

found to eight times faster than the DC measurement to get a same level of noise. The sensitivity of AC method is close to the sensitivity of the DC technique. However, a drift current is observed in both methods, and it is impossible to be removed by the AC method.

CHAPTER 5

MOS STRAIN SENSOR SENSITI.ITY STUDY BASED ON ECB AND E.B MODELING

5.1 Introduction

This chapter builds simulation models for MOS tunneling current strain sensor. The purpose of modeling is to provide an explanation for the experimental results, and to better understand how to optimize a tunneling current strain sensor.

The tunneling current through an MOS structure has been well studied. However, there is very little literature on the change of the tunneling current with respect to strain. Several groups have studied the change of the NMOS gate current in the inversion region, but they only considered tunneling from the conduction band of the substrate to the gate (ECB tunneling) [55-57]. ECB tunneling has been successfully applied to explain the gate tunneling current in NMOS transistors for zero strain, or for a strained MOSFET with low substrate doping concentrations. This chapter will show that the valence band tunneling (EVB tunneling) is necessary to explain the sensitivity of a MOS tunneling current strain sensor, especially when the substrate doping concentration is high to minimize series resistance, or when a large gate voltage is applied. The tunneling current was calculated using both ECB and EVB tunneling, and the effects of doping concentration were studied. The

model used is appropriate for a NMOS tunneling current strain sensor made on a (001) silicon wafer which is positively biased to the inversion region.

Section 5.2 and Section 5.3 discuss ECB modeling and EVB modeling and verify the modeling results with experiment results from other groups. Then Section 5.4 uses models to simulate the proposed devices used in DC measurement. Section 5.5 studies the influence from substrate doping concentration.

5.2 ECB modeling

For ECB tunneling current, Thompson's group built a model to simulate the stress altered gate current by self-consistently solving Schrodinger equation and Poisson equation for the quantized carrier layers and solving the tunneling probability using the transfer-matrix-method [17, 55]. The model requires a lot of effort and time to compute. To predict how MOS tunneling current changes with strain in the inversion region quickly and accurately, computationally efficient models are built. Here approximate methods are used to solve the energy quantization and the WKB method to solve the tunneling probability. The strain induced energy shift can be expressed by deformation potential theory [58]. Two approximate methods to solve the energy quantization are employed and compared. For the energy quantization, the tunneling current is computed as a function of stress for each method.

The models are built for n-type MOS capacitor on a (001) wafer with a heavily doped n-type poly-silicon gate. The gate current and electron energy quantization are along the <001> direction or Z direction. As shown in Figure 5.1, the MOS capacitor is positively biased to the inversion region, in which

the electrons' energies are quantized. The six degenerate conduction band minimum are divided into two groups, the two-fold degenerate Δ_2 group whose longitudinal effective mass is along the <001> direction, and the four-fold degenerate Δ_4 group whose transverse effective mass is along the <001> direction. Since the longitudinal effective mass is larger than the transverse effective mass, the Δ_2 group has lower energy levels. The MOS capacitor's tunneling current through the silicon dioxide is determined by (1) the energy barrier height between the silicon conduction band edge and the SiO_2 conduction band edge; and (2) the electrons' out of plane effective mass. When a <110> uniaxial tensile strain is induced, the band gap of silicon is decreased and conduction band edge of silicon is lowered. In addition, the Δ_2 valleys are lowered in energy and the Δ_4 valleys are raised in energy. As a result, both effects decrease the tunneling current. In contrast, as a <110> compressive strain is applied, the tunneling current is increased.

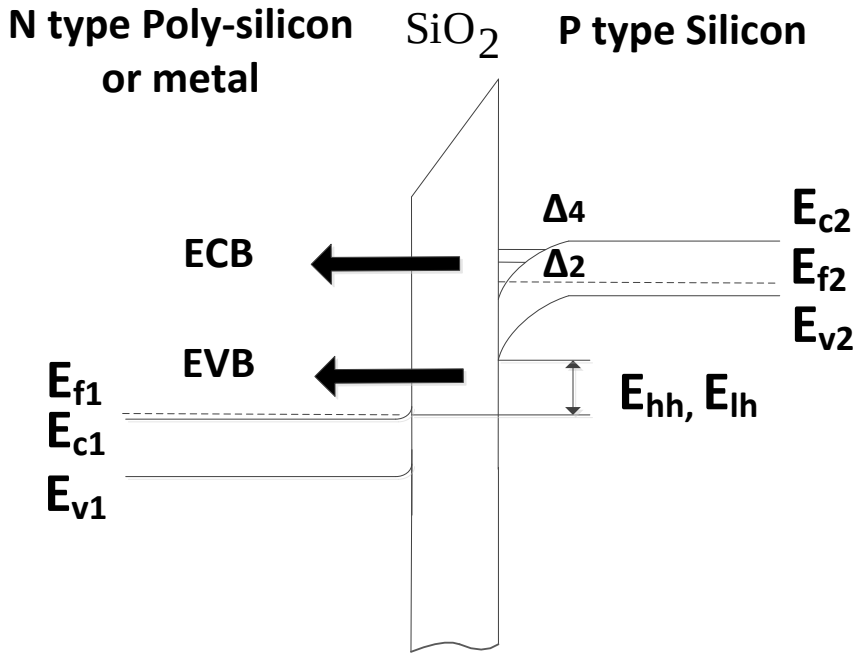


Figure 5.1 NMOS in inversion region.

5.2.1 Approximate methods for quantized inversion layer

The sub-bands of inversion layer of NMOS capacitor can be obtained by self-consistently solving the Schrodinger equation and Poisson equation. Using the effective mass approximation, the electronic wave function can be written as [59],

$$\psi_{i,j}(x,y,z) = \zeta_{i,j}(z)e^{i\theta z}e^{ik_1 x + ik_2 y} \tag{5.1}$$

where $\psi_{i,j}(x,y,z)$ is the envelope of the ith energy level, $\zeta_{i,j}(z)$ is the envelope along the z direction, θ is determined by k_1 and k_2, i denotes Δ_2 and Δ_4 and equals to 2 for Δ_2 or 4 for Δ_4, j denotes the sub-bands levels. This approximation decouples the 3D Schrodinger equation into a 1D equation,

$$\left[-\frac{\hbar^2}{2m_{z,i}} - \frac{d^2}{dz^2} + eV(z)\right]\zeta_{i,j}(z) = E_{i,j}\zeta_{i,j}(z) \tag{5.2}$$

where $E_{i,j}$ is the sub-band energy level (the conduction band edge at the surface is the relative 0 ev), e is the electron charge, $\hbar$ is Plank's constant, $m_{z,i}$ is the electron effective mass in the z-direction, and $V(z)$ is the potential well which is determined by the Poisson equation,

$$\frac{d^2V(z)}{dz^2} = -\rho(z)/\varepsilon_{Si} \tag{5.3}$$

where $\rho(z)$ is the charge density including both depletion layer and inversion layer, and ε_{Si} is the dielectric constant of silicon. Since the charge density solved from the Schrodinger equation will influence the potential well and the potential well in turn determines the charge density, a self-consistent way to solve Schrodinger equation and Poisson equation is needed. To obtain accurate results, a numerical method to solve differential equations may be

employed which is quite time consuming and costly. Alternatively, a triangular potential well approximation method may be used to simplify the self-consistent coupling, which leads to the well-known Airy equation solutions [60],

$$\zeta_{i,j}(z) = A_{i,j}(2m_z eF_s/\hbar^2)^{1/3}[z - E_{i,j}/eF_s] \tag{5.4}$$

$$E_{i,j} = (\hbar^2/2m_{z,i})^{1/3}[3/2\pi eF_s(j + 3/4)]^{2/3} \tag{5.5}$$

Where

$$Z_{i,j} = 2E_{i,j}/3eF_s \tag{5.6}$$

$$F_s = \frac{e\left(N_{depl} + N_{inv}\right)}{\varepsilon_{Si}} \tag{5.7}$$

$$N_{depl} = \sqrt{2\varepsilon_{Si}\psi_d N_a/e} \tag{5.8}$$

$$N_{inv} = \sum_{i,j} N_{inv_{i,j}} \tag{5.9}$$

$$N_{inv_{i,j}} = \frac{k_B T m_{d,i} g_{\Delta_{2/4}}}{\pi\hbar^2} \ln[1 + e^{-\left(\frac{E_{i,j} - E_f}{k_B T}\right)}] \tag{5.10}$$

$$\psi_d = \psi_s - \frac{k_B T}{e} - eN_{inv}Z_{av}/\varepsilon_{Si} \tag{5.11}$$

$$Z_{av} = \sum_{i,j} N_{inv_{i,j}} Z_{i,j} / N_{inv} \tag{5.12}$$

$$E_f = -E_g + e\psi_s - k_B T \ln(N_v/N_a) \tag{5.13}$$

where $Z_{i,j}$ is the penetration distance of the inversion layer carriers

from the surface, F_s is the surface electric field, N_{depl} is depletion layer charge concentration, N_{inv} is the total inversion layer charge concentration, ψ_d is the surface band bending without contribution of inversion layer, N_a is substrate doping concentration, $N_{inv_{i,j}}$ is the sub-bands charge concentration, k_B is the Boltzmann constant, T is the temperature, $m_{d,i}$ is the density of states effective mass per valley, $g_{\Delta_{2/4}}$ is the valley degeneracy, E_f is the Fermi level relative to the surface conduction band edge, ψ_s is the surface potential, Z_{av} is the average distance inversion layer carriers from the surface, E_g is the band gap and n_i is the intrinsic carrier concentration. However, this triangular potential well method only provides good approximate results when the inversion layer charge density is smaller than the depletion charge density. A variational method was proposed by assuming that most of charges occupy the ground sub band and using a trial eigenfunction. The ground energy levels can be described as [60, 61],

$$E_{i,1} = \left(\frac{3}{2}\right)^{\frac{5}{3}} \left(\frac{e^2 h}{m_{z,i}^{\frac{1}{2}} \varepsilon_{Si}}\right)^{\frac{2}{3}} \frac{(N_{depl}+\frac{55}{96}N_{inv})}{(N_{depl}+\frac{11}{32}N_{inv})^{1/3}} \tag{5.14}$$

$$Z_{i,1} = \left(\frac{9\varepsilon_{Si}\hbar^2}{4m_{z,i}e^2\left(N_{depl}+\frac{11}{32}N_{inv}\right)}\right)^{\frac{1}{3}} + 4Na\left(\frac{9\varepsilon_{Si}\hbar^2}{4m_{z,i}e^2\left(N_{depl}+\frac{11}{32}N_{inv}\right)}\right)^{2/3} / 9\left(N_{depl}+\frac{11}{32}N_{inv}\right) \tag{5.15}$$

This equation can be applied to both Δ_2 and Δ_4 by using different out of plane effective masses, $m_{z,i}$, for Δ_2 and Δ_4. Since the higher states have less influence, we still use (5.5) & (5.6) for the higher states. Table 7 gives the value of parameters used in the modeling. m_e is the free space electron mass.

Table 7

Values of effective masses used in this paper.

$m_{z,2}$	$0.98m_e$
$m_{z,4}$	$0.19m_e$
$m_{d,2}$	$0.19m_e$
$m_{d,4}$	$0.417m_e$

Figure 5.2 shows the sub-bands and the Fermi level for the triangle approximation method and the variational method, as well as the self-consistent method solving differential equations using Schred [62]. E_{21} is the ground state for the Δ_2 valley, and E_{41} is the ground state for the Δ_4 valley. From Figure 3, it is observed that at low voltages the sub-bands from the two approximate methods are close to the results from Schred. However, the difference between the approximate methods and Schred becomes large as the voltage increases. It is clear that compared with the triangle approximate method, the variational method gives a better fit.

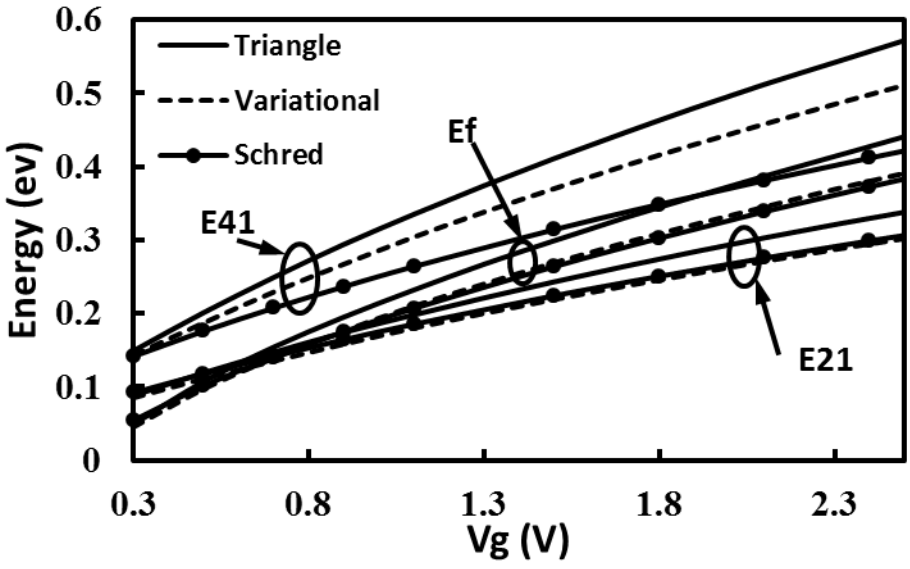


Figure 5.2 Sub-bands vs. gate voltage. The doping concentration of p-type substrate is 1e17 cm^{-3}. The doping concentration of n-type poly gate is 1e20 cm^{-3}. The thickness of gate oxide is 2.19 nm.

5.2.2 ECB tunneling current using WKB approximation

After obtaining the sub-bands, the WKB approximation method is used to obtain the direct tunneling current,

$$J = \sum_{i,j} \frac{qN_{inv_{i,j}}}{\tau_{i,j}} \tag{5.16}$$

where

$$\tau_{i,j} = \frac{j\pi\hbar}{E_{i,j}TR} \tag{5.17}$$

Here TR is the modified WKB approach tunneling probability [56, 57, 63]. $TR_{i,j}$ is the modified WKB approach tunneling probability, which is expressed as [57]:

$$\mathrm{TR} = \mathrm{WKB_{i,j}T_{i,j}} \tag{5.18}$$

where $\mathrm{WKB_{i,j}}$ is the classic WKB approach tunneling probability for each sub-bands. $\mathrm{T_{i,j}}$ is the correction factor considering reflection within the gate oxide. $\mathrm{WKB_{i,j}}$ and $\mathrm{T_{i,j}}$ are expressed below:

$$\mathrm{WKB_{i,j}} = \mathrm{e}^{\frac{\mathrm{E_g}\sqrt{2\mathrm{m_{ox}}}}{4\hbar\mathrm{qF_{ox}}}[2\left(1-\frac{2\mathrm{E_{ox}}}{\mathrm{E_g}}\right)\sqrt{\mathrm{E_{ox}}\left(1-\frac{2\mathrm{E_{ox}}}{\mathrm{E_g}}\right)}+\sqrt{\mathrm{E_g}}\mathrm{asin}(1-\frac{2\mathrm{E_{ox}}}{\mathrm{E_g}})]}\Big|_{\mathrm{E_{ox}=\psi_{an}}}^{\mathrm{E_{ox}=\psi_{cath}}} \tag{5.19}$$

$$\mathrm{T_{i,j}} = \frac{4\mathrm{vs1_{i,j}voxcath_{i,j}}}{\mathrm{vs1_{i,j}}^2 + \mathrm{voxcath_{i,j}}^2}\frac{4\mathrm{vs2_{i,j}voxan_{i,j}}}{\mathrm{vs2_{i,j}}^2 + \mathrm{voxan_{i,j}}^2} \tag{5.20}$$

where the Franz dispersion relation is used to calculate $\mathrm{WKB_{i,j}}$. E_g is the gate oxide band gap, which is equal to $9.3\ \mathrm{eV}$. m_{ox} is the electron effective

mass, which equals to $0.38m_0$ for an Al gate and $0.55m_0$ for a poly-Silicon gate, where $\mathrm{m_0}$ is free space electron mass. F_{ox} is electrical field in oxide. E_{ox} is electron energy referred to the gate oxide conduction band edge, which equals to $\psi_{cath} = q\chi_c - E_{i,j}$ at the cathode side and $\psi_{an} = q\chi_c - E_{i,j} - qF_{ox}t_{ox}$ at the anode side. χ_c is the tunneling barrier between the edge of oxide conduction band and the edge of Silicon conduction band, which equals to $3.1\ \mathrm{eV}$. This analysis ignores the electron kinetic energy parallel to interface. Using the parabolic dispersion relation, $vs1_{i,j} = \sqrt{\frac{2E_{i,j}}{m_{i,z}}}$ and $vs2_{i,j} = \sqrt{\frac{2E_{i,j}+qF_{ox}t_{ox}}{m_{i,z}}}$ are the electron group velocity incident and leaving the oxide, respectively, where $m_{i,z}$ is the electron out-of-plane effective mass. Under the Franz dispersion relation, $voxcath_{i,j} = \frac{1}{2\psi_{cath}/E_g}\sqrt{\frac{2\psi_{cath}(1-\psi_{cath}/E_g)}{m_{ox}}}$ and $voxan_{i,j} = \frac{1}{2\psi_{an}/E_g}\sqrt{\frac{2\psi_{an}(1-\psi_{an}/E_g)}{m_{ox}}}$ are the group velocity of electrons at the cathode and the anode within gate oxide. Other parameters used in modeling are the same as [64]. Details about TR refer to Chapter 2.

Figure 5.3 shows the gate current from modeling and experiment. Both methods give a gate current that is similar compared to the experimental result for voltages larger than 1 V. There is minimal difference between the two modeling methods from the gate current modeling with zero stress.

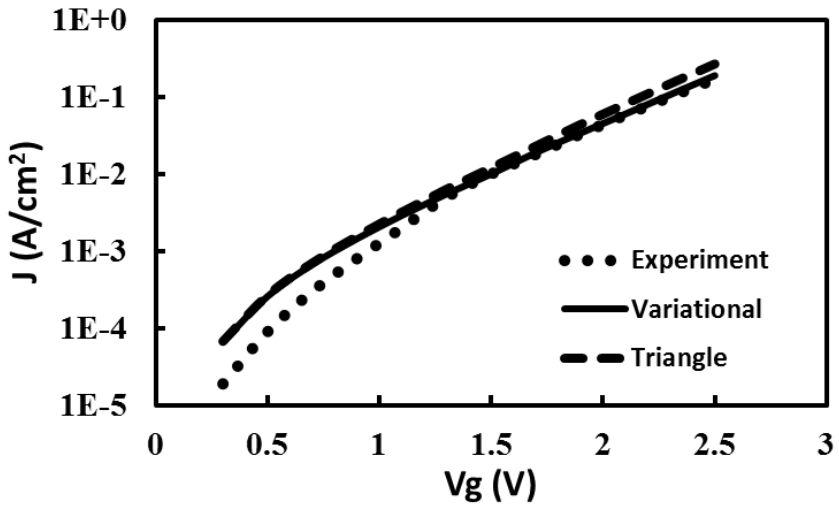


Figure 5.3 Gate current density vs. gate voltage. The device parameters are the same as used in Figure 5.2. The experiment results are from [65].

5.2.3 Strain induced ECB tunneling current changing

Considering an <110> uniaxial stress is applied to the wafer, and applying deformation potential theory, the sub-bands with stress can be obtained,

$$E'_{2,j} = E_{\Delta_2,j} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})\sigma + \left(\frac{\Xi_u}{3}\right)(S_{12} - S_{11})\sigma \quad (5.21)$$

$$E'_{4,j} = E_{4,j} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})\sigma - \left(\frac{\Xi_u}{6}\right)(S_{12} - S_{11})\sigma \quad (5.22)$$

where $\Xi_d = 1.13\,eV$, $\Xi_u = 9.16\,eV$, $S_{11} = 7.68\,e-12\,m^2/N$, $S_{11} = -2.14\,e-12\,m^2/N$. As a result, the tunneling current with stress can be obtained by substituting the sub bands with stress into (5.16), which is,

$$J'(\sigma) = \sum_j \frac{qN'_{inv2,j}(\sigma)}{\tau'_{2,j}(\sigma)} + \sum_j \frac{qN'_{inv4,j}(\sigma)}{\tau'_{4,j}(\sigma)} \quad (5.23)$$

The change in tunneling current can be expressed as,

$$\Delta J/J\,(\sigma) = \frac{(J'(\sigma)-J)}{J} \tag{5.24}$$

Figure 5.4 shows the comparison between triangle potential approach and the variational approach for $\Delta J/J\,(\sigma)$, as well as the comparison to the experimental results for both approaches. Figure 5.4 indicates that the variational approach is closer to the experimental results.

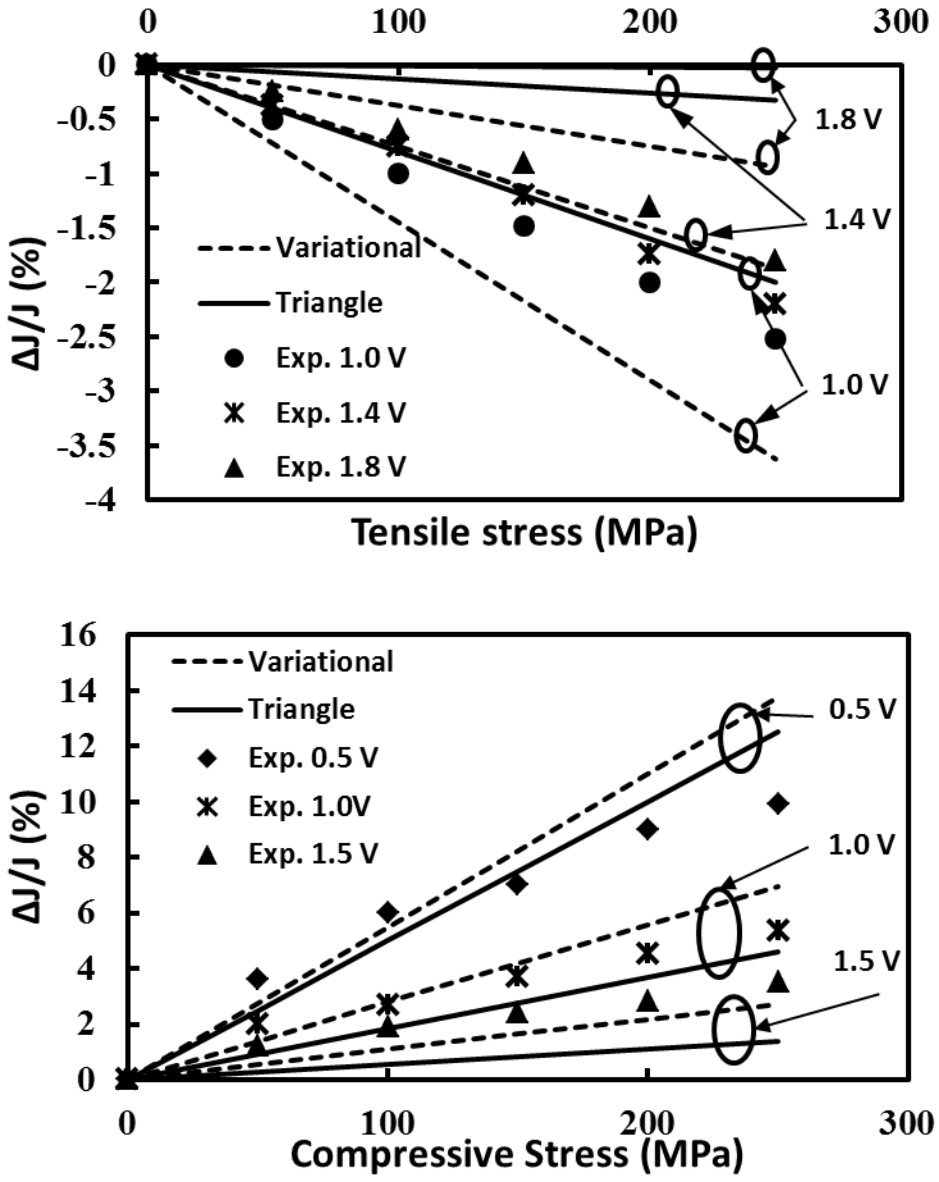


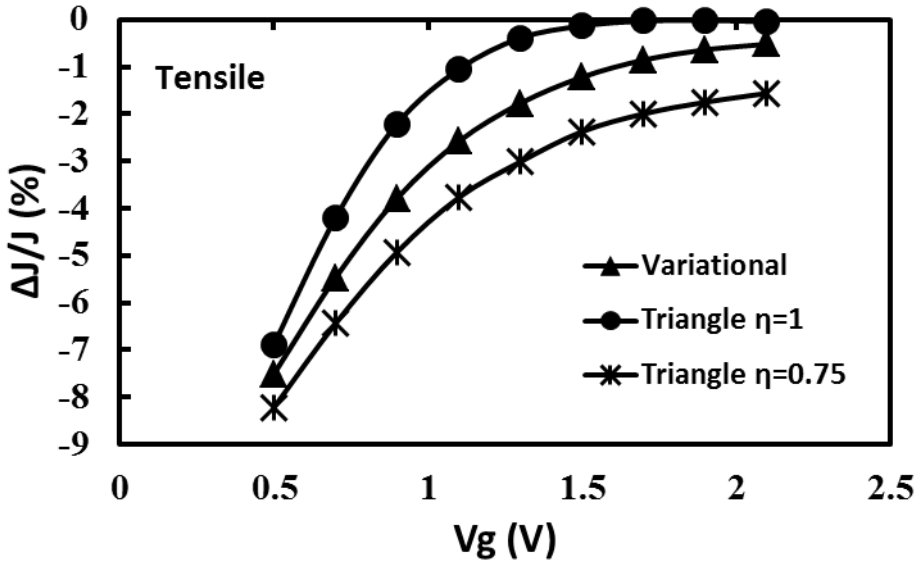
Figure 5.4 Modeling vs. experimental results. For the tensile case, the doping concentration is 5e17 cm^{-3} for the p-type substrate and 1e20 cm^{-3} for the n-type poly gate. The thickness of gate oxide is 1.3 nm. The experimental

data for the tensile is from [55]. For the compressive case, the doping concentration is 1e17 cm^{-3} for the p-type substrate and 1e20 cm^{-3} for the n-type poly gate. The thickness of gate oxide is 1.3 nm. The experimental data for the tensile is from [66].

In some papers, a correction coefficient η is used in (5.7), which is modified to,

$$F_s = \frac{e\left(N_{depl} + \eta N_{inv}\right)}{\varepsilon_{Si}} \tag{5.25}$$

It is typically some number between 0.5 and 1 [66-68]. In Figure 5.5, $\Delta J/J$ vs. voltage are plotted for ±200 MPa stress. The sensitivity decreases as the voltage increases for both tensile stress and compressive stress. The triangle method with $\eta = 0.75$ has a larger change in current than for $\eta = 1$. The correction factor may be chosen to fit experiment, but it is not known *a priori*.



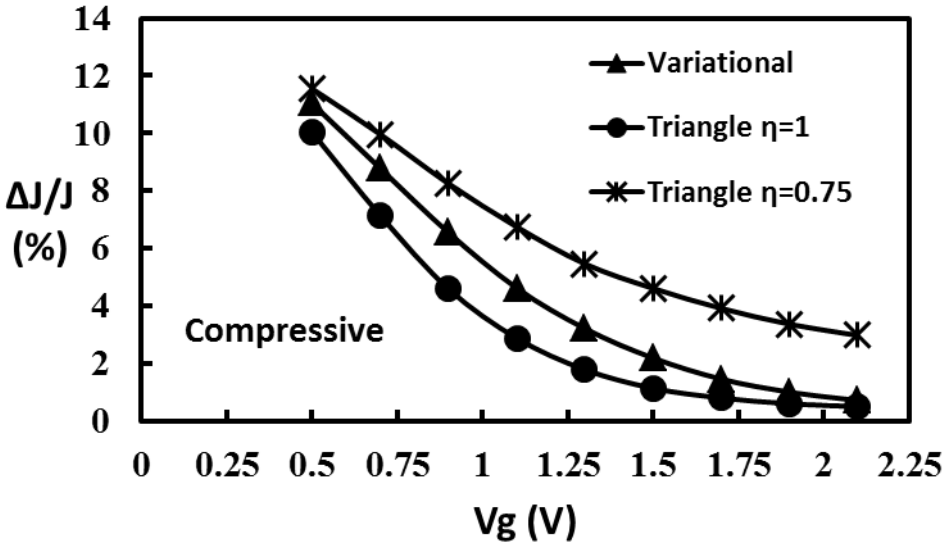


Figure 5.5 Percent change in current density versus voltage. The tensile and compressive stress are both 200 MPa. The parameters are the same as Figure 5.4.

5.2.4 Summary of ECB tunneling current modeling

For this study, two computationally efficient models are built to study stress induced gate current changing for NMOS capacitor which is biased to inversion region. The computational efficiency comes from the adoption of approximate method for the sub-bands and WKB method for the tunneling probability. The sub-bands from these two models are compared with Schred which solves differential equations self-consistently, which shows that the results from the variational method are closer to Schred than the triangle approximate method. The two approximation methods provide nearly the same current without stress, but when stress is applied, the variational method provides an answer that is much closer to experiment. This model can be used to better model and understand MOS tunneling current sensors.

5.3 EVB modeling

Unlike ECB tunneling current, the electrons in the valence band are not

confined in a 2D layer at the surface, so quantization is not necessary. As shown in Figure 5.1, the Fermi level at gate, E_{f1}, is set to be the relative 0 energy level. E_{f2} is the Fermi level in substrate. E_{c1} and E_{c2} are the conduction band edges of the gate and substrate, respectively. E_{v1} and E_{v2} are the valence band edges of the gate and substrate, respectively.

E_{hh} and E_{lh} are the difference between E_{v2} and E_{f1} for the heavy hole band and the light hole band. When there is no stress, $E_{hh} = E_{lh} = E_{v2} - E_{f1}$. When there is uniaxial stress, the heavy hole band and the light hole band are split. For a metal gate, there is no band gap, so E_{hh} and E_{lh} do not have to be larger than 0 for tunneling to occur. The EVB tunneling current can be expressed as:

$$J_{evb} = J_{hh} + J_{lh} \tag{5.26}$$

where J_{hh} is the component in which electrons have a heavy hole effective mass and J_{lh} is the component in which electrons have a light hole effective mass. Adopting a model from Tsu and Esaki [69], J_{hh} and J_{lh} may be obtained:

$$\begin{aligned} J_{hh} &= \frac{4\pi q m_{hh}}{h^3} \int_{E_{min}}^{E_{hh}} TR_{hh}(E_x)dE_x \int_0^{E_{hh}-E_x} \big(1 - f_1(E)\big) f_2(E) dE_r \\ &= \frac{4\pi q m_{hh}}{h^3} \int_{E_{min}}^{E_{hh}} TR_{hh}(E_x) \big(1 - f_1(E)\big)(E_{hh} - E_x) dE_x \end{aligned} \tag{5.27}$$

$$\begin{aligned} J_{lh} &= \frac{4\pi q m_{lh}}{h^3} \int_{E_{min}}^{E_{lh}} TR_{lh}(E_x)dE_x \int_0^{E_{lh}-E_x} (1 - f_1(E)) f_2(E) dE_r \\ &= \frac{4\pi q m_{lh}}{h^3} \int_{E_{min}}^{E_{lh}} TR_{lh}(E_x) \big(1 - f_1(E)\big)(E_{lh} - E_x) dE_x \end{aligned} \tag{5.28}$$

where m_{hh} equals $0.49m_0$ and m_{lh} equals $0.16m_0$. $f_1(E)$ and $f_2(E)$ are

the Fermi-Dirac distribution for electrons in the gate and the substrate, respectively, where $E = E_x + E_r$. In the inversion region, because the difference between E_{f2} and E_{v2} is much larger than $k_B T$, $f_2(E) \approx 1$, where k_B is Boltzmann's constant and T is room temperature. TR_{hh} and TR_{lh} are modified WKB approach tunneling probability similar to TR used for ECB tunneling current modeling, but for the valence band. The tunneling barrier in TR_{hh} and TR_{lh} is the difference between the oxide conduction band edge and E_{v2}, which equals to $4.15\ eV$. For the aluminum gate, without a band gap in the gate, E_{min} could be less than $0\ eV$. In (5.27) and (5.28), E_r is assumed to be neglectable in $f_1(E)$ and $f_2(E)$.

Figure 5.6 shows EVB modeling results compared with a compact model [70]. Since it is poly-gate, (5.26), (5.27) and (5.28) are only valid, when $\mathrm{E_{hh}}$ and $\mathrm{E_{lh}}$ are ≥ 0 eV. Besides, $\mathrm{E_{min}} = 0$ eV.

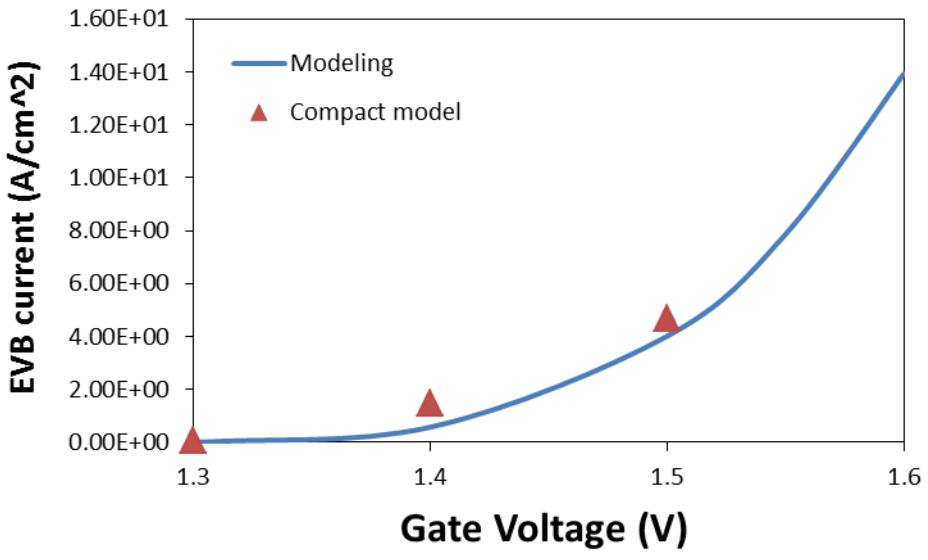


Figure 5.6 EVB modeling. The parameters used in EVB modeling are the same as those in Figure 2 in [70].

When <110> uniaxial stress is applied, the heavy hole band and light hole band are split as follows:

$$E_{hh} = E_{v2} - E_{f1} + \Delta E_{hh} \tag{5.29}$$

$$E_{lh} = E_{v2} - E_{f1} + \Delta E_{lh} \tag{5.30}$$

where $\Delta E_{hh} = -0.035 * 10^{-9}\sigma$ and $\Delta E_{lh} = 0.018 * 10^{-9}\sigma$. ΔE_{hh} and ΔE_{lh} are the band shift for heavy hole band and light hole band, respectively. It is difficult to get an analytic equation for the valence band shift under uniaxial stress. For this work, the valence band shift was interpolated from the simulation results from [71]. The sensitivity expression for EVB tunneling current is similar to (5.24).

5.4 ECB and EVB tunneling current modeling for the MOS tunneling current strain sensor used in the DC measurement

In the previous sections, models for ECB and EVB tunneling current are built. The section uses these models to simulate the MOS tunneling current strain sensor used in the DC measurement. The device is NMOS capacitor with Al gate. The thickness of gate oxide is 3.7 nm. The substrate doping concentration is 2.0e18 /cm^3. Table 8 give sensitivity vs. gate voltage from DC measurement in Chapter 4. The models discussed later fit this table.

Table 8

Sensitivity vs. gate voltage from our group's experiment.

Gate voltage (V)	Sensitivity (%)
1	-2.2
1.5	-2.0
2	-2.5

Figure 5.7 shows the current density versus gate voltage. It is clear that at a low voltage, the ECB tunneling current dominates. However as the gate voltage increases, the EVB tunneling current increases rapidly and becomes nearly the same as the ECB tunneling current. Then the total current density is determined by both ECB tunneling current and EVB tunneling current. As discussed in the following section, the sensitivity is also expected to be determined by the ECB tunneling at low voltage, but the influence from the EVB tunneling current becomes more important as the gate voltage increases.

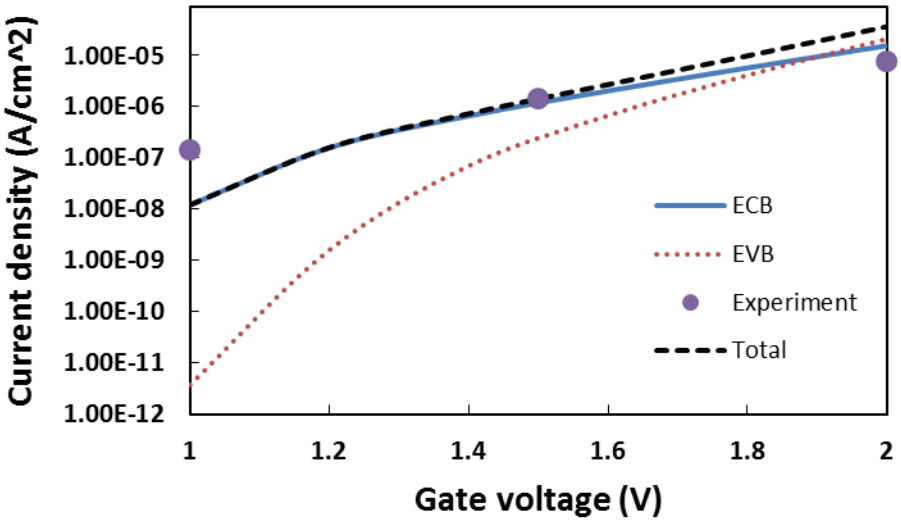


Figure 5.7 Calculated current density for the MOS strain sensor without strain, including the ECB tunneling current, EVB tunneling current, and the total tunneling current. A comparison to the experimental results are also shown.

Figure 5.8 shows sensitivity vs. gate voltage for ECB under 200 MPa <110> uniaxial tensile stress. It is clear that sensitivity decreases with increasing gate voltage for ECB.

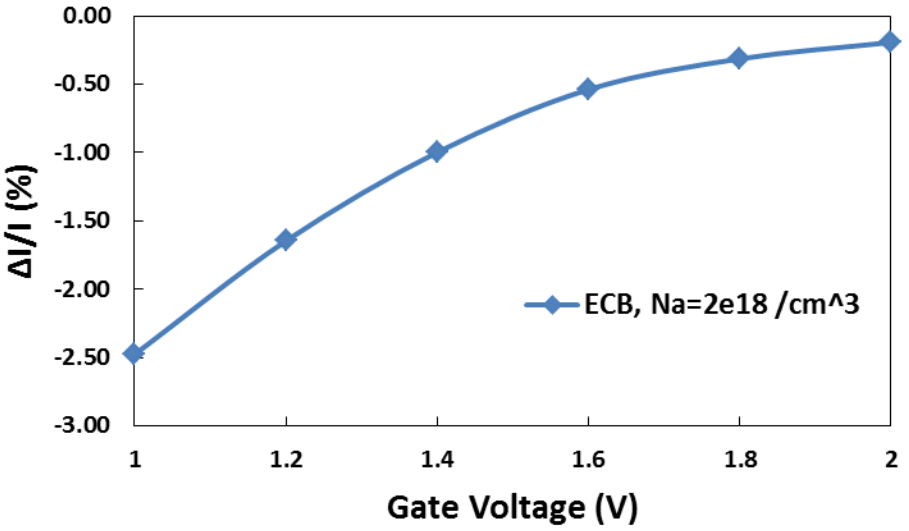


Figure 5.8 Sensitivity vs. gate voltage for ECB.

Figure 5.9 shows the sensitivity versus gate voltage for EVB tunneling current under 200 MPa <110> tensile stress. Like the sensitivity versus gate voltage for ECB tunneling current, the sensitivity for EVB tunneling current also decreases as gate voltage increases. However, the sensitivity is much greater than for the ECB tunneling current, and never drops below 4%.

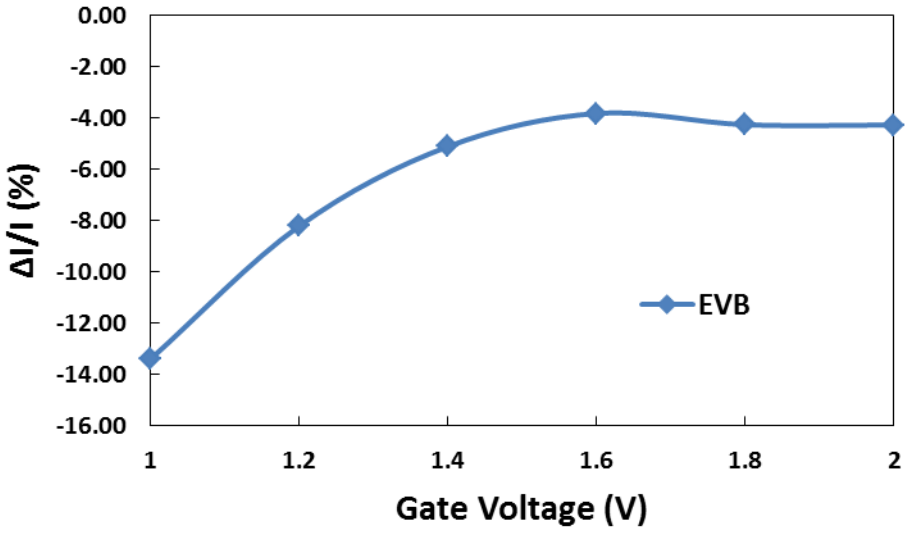


Figure 5.9 Calculated sensitivity vs. gate voltage for EVB tunneling current.

The NMOS tunneling current is comprised of both the ECB tunneling current and the EVB tunneling current and are discussed in this section. The total current density, J, equals $J_{ecb} + J_{evb}$. $J'(\sigma)$ is the total current density under stress. Similar to (5.24), the sensitivity is expressed as:

$$\Delta J/J\,(\sigma) = \frac{(J'(\sigma) - J)}{J} \tag{5.31}$$

Figure 5.10 shows the calculated sensitivity versus the gate voltage for our group's device, which agrees with the tensile results in our experiment. The total sensitivity does not simply decrease as the gate voltage increases, even though it decreases for both ECB tunneling current and EVB tunneling current. It is noticed that at the same gate voltage, the sensitivity for EVB tunneling current is larger than ECB tunneling current. When the gate voltage is small, the ECB tunneling current dominates total tunneling current, so its sensitivity dominates the total sensitivity. As the gate voltage increases, the EVB tunneling current becomes close to the ECB tunneling current, so the influence of the EVB sensitivity increases. Because the EVB tunneling current sensitivity is larger than ECB tunneling current sensitivity, it should be expected that the overall sensitivity increases as the gate voltage increases.

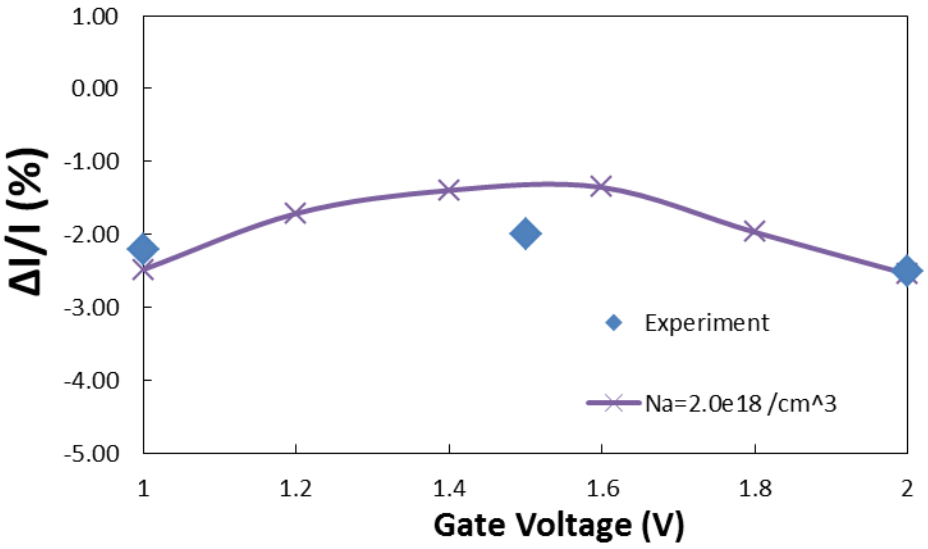
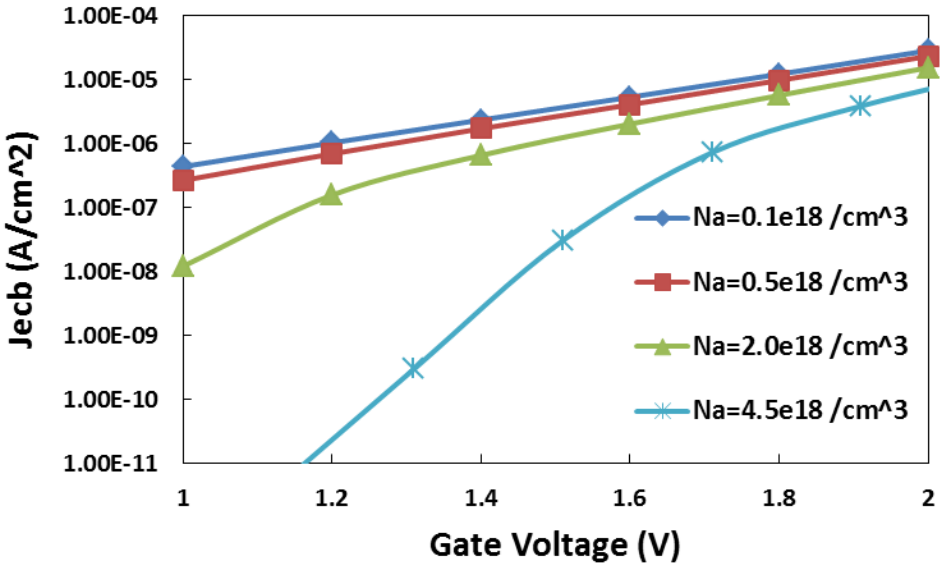


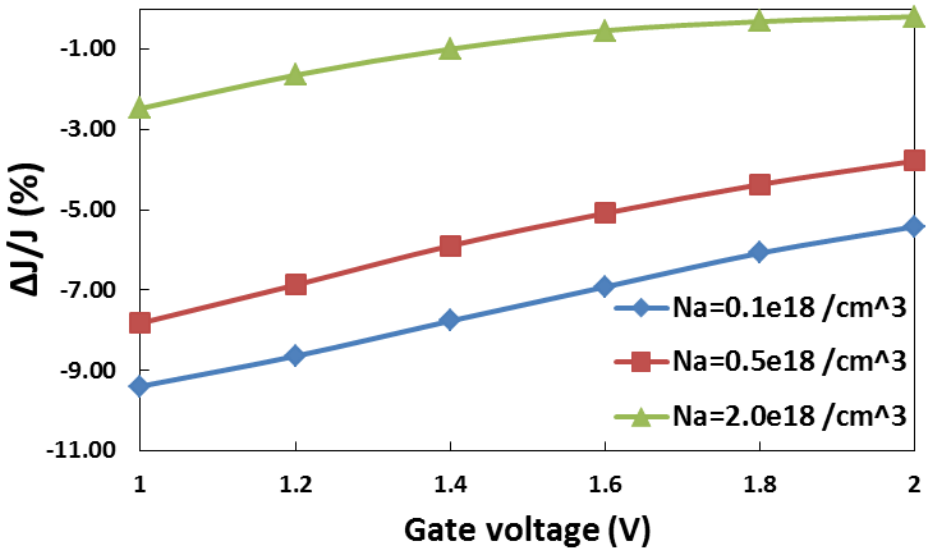
Figure 5.10 Sensitivity vs. gate voltage for total tunneling current. The line is calculated from the model, and the diamonds are the measured experimental results.

5.5 Different doping concentration

Doping concentration's influence on sensitivity is studied in this section. Figure 5.11 shows current density and sensitivity vs. gate voltage for ECB for different doping concentration. As doping concentration increases, both current density and sensitivity for ECB decrease.



(a)

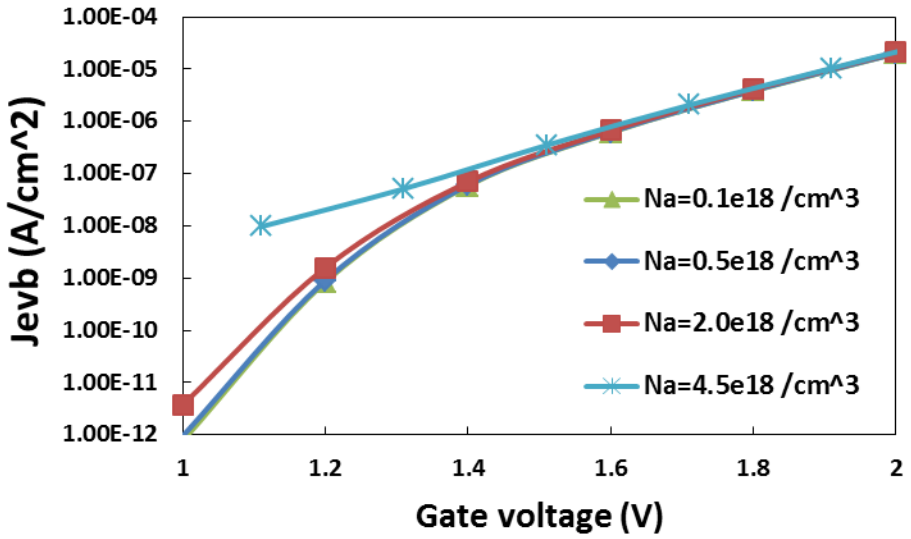


(b)

Figure 5.11 ECB modeling for different doping concentration. Parameters are the same as MOS tunneling current strain sensor in DC measurement. (a). Current density vs. gate voltage for ECB; (b). Sensitivity vs. gate current for ECB.

Figure 5.12 shows current density and sensitivity vs. gate voltage for

EVB for different doping concentration. For EVB current density, doping concentration has larger influence at lower voltage, but less influence at higher voltage. For sensitivity, unlike ECB, doping concentration has little influence on EVB.



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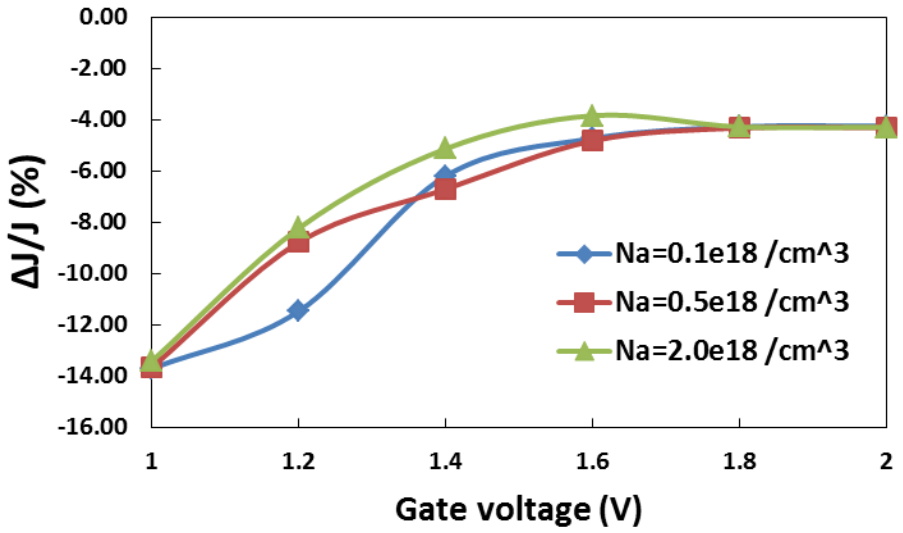


(b)

Figure 5.12 EVB modeling for different doping concentration. Parameters are the same as MOS tunneling current strain sensor in DC measurement. (a).

Current density vs. gate voltage for EVB; (b). Sensitivity vs. gate current for EVB.

Figure 5.13 shows the total gate current sensitivity vs. gate voltage at different doping concentration. The same device from MOS tunneling current strain sensor in DC measurement is used here. At low doping concentration, sensitivity decreases as gate voltage increases, which is similar to [55]. At high doping concentration, sensitivity decreases and then increases as gate voltage increases, which is similar to Table 7.

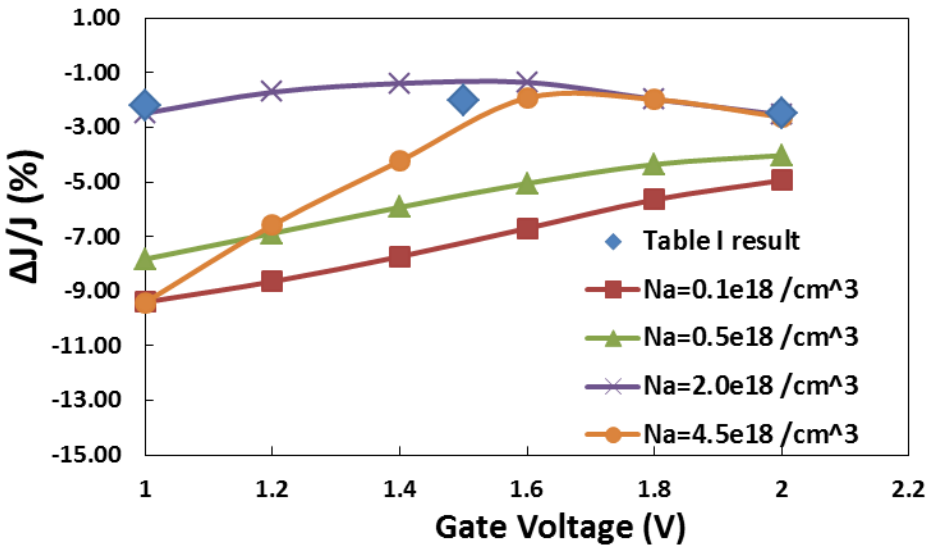


Figure 5.13 Total sensitivity vs. gate voltage at different doping concentration. Parameters are the same as MOS tunneling current strain sensor in DC measurement.

The difference comes from doping concentration, which changes both ECB and EVB and sensitivity. To explain this result, gate voltage and doping concentration are divided into three groups, low doping concentration (0.1e18

and 0.5e18 /cm3), low voltage and high doping concentration (2e18 and 4.5e18 /cm3), and high voltage and high doping concentration.

1) At low doping concentration, ECB current density is much larger than EVB current density at low voltage, and comparable to EVB current density at high voltage. In the same time, ECB sensitivity is larger than EVB sensitivity. Therefore, ECB has a larger influence on total gate current sensitivity at low doping concentration, which makes total gate current sensitivity decreases like ECB.
2) At low voltage and high doping concentration, ECB is larger than EVB, and its sensitivity is larger than that of EVB, so ECB has a larger influence on sensitivity, which decreases.
3) At high voltage and high doping concentration, EVB and ECB becomes comparable, and EVB sensitivity is larger than that of ECB, so EVB sensitivity makes total gate current sensitivity increase.

As doping concentration continues to increase, we should expect that EVB dominates eventually in total MOS tunneling current, and its sensitivity will also eventually dominates which makes total gate current sensitivity decreases.

5.6 Summary

To better understand the sensitivity, we built computationally efficient models for both ECB tunneling current and EVB tunneling current. The computational efficiency comes from the adoption of approximate methods for the sub-bands for ECB tunneling current and WKB method for the tunneling probability for both ECB tunneling current and EVB tunneling current. The modeling results fit both this dissertation and other groups' experiments. From

modeling, it is seen that at low voltages, ECB tunneling current dominates total tunneling current. However, at high voltages, EVB tunneling current becomes very important and comparable to ECB tunneling current, which will influence both total tunneling current and total sensitivity. Substrate doping concentration also changes the total tunneling current and total sensitivity. Therefore, when calculating the sensitivity for a MOS tunneling current strain sensor, it is important to consider both the ECB and EVB tunneling currents, especially for high voltages or high doping concentrations. These results are consistent with the measured results in this dissertation.

CHAPTER 6

BULK ACOUSTIC LONGITUDINAL RF RESONATOR BASED ON MOS TUNNELING CURRENT STRAIN SENSOR

6.1 Introduction to RF MEMS resonator

The measurements in Chapter 4 shows that drift cannot be removed in both DC method and AC method. However, instead of measuring amplitude of MOS tunneling current, we can measure frequency changing by making a resonator sensor based on MOS tunneling current strain sensor.

Resonator has been used vastly in oscillators, filters and sensors [72-77]. Due to its high quality factor (Q), compatibility with CMOS process, low power, low cost batch fabrication and easy to miniaturize, RF MEMS resonator has been attractive alternative to Quartz crystal and SAW devices. RF MEMS resonator can also be integrated to CMOS circuit in one chip to reduce parasitic impedance and time delay for high frequency applications. Quartz crystal resonator and SAW resonator offer a large Q, great temperature stability and high reliability. However they cannot be made on-chip and suffer from poor resistance to shock [78-83].

There are basically three categories of RF MEMS resonator. They are capacitive resonator, piezoelectric and piezoresistive resonators. Capacitive resonator usually actuates resonation using electrostatic force and senses resonation through capacitance changing during resonation. The benefit of

capacitive sensing is low temperature dependence. However the capacitance changes can be extremely small, which can be buried in noise and parasitic capacitance [84-86]. Piezoelectricity is a phenomenon that in some materials an electrical field can be generated when these materials are subject to mechanical deformation. Piezoelectric sensing only applies to applications under non-static strain. Piezoelectric resonators usually adopt metal - piezoelectric material - metal sandwich structure. The most common piezoelectric materials used in RF MEMS resonators are aluminum nitride. The disadvantage of piezoelectric resonators is that it is not able to integrate with IC in one die [87-89]. Piezoresistive sensing detects resistance changing due to resonation. Although the theory and fabrication process of these accelerometers are simple, the temperature sensitivity and poor noise limit the performance [90, 91].

According to shapes, anchors and actuation, there are several different categories of resonators [92]. Table 9 lists some common types of resonators. Each type has several different modes depends on how it is actuated. For example, when the electrode pad of a clamp – free resonator is placed below the beam, beam vibrates up and down. However if the electrode is placed along the beam and at the free end, the beam vibrates longitudinally.

Table 9

Summary of vibrating shapes

Resonator types	Description	Performance
Clamp – clamp [93]	An electrode is placed in plane or under the clamp – clamp beam to form transducer capacitor.	1 MHz - 100MHz; Q degraded due to anchor dissipation at high frequency.
Clamp – free [94]	The clamp can be at one end or in the middle of the beam.	High Q; lower anchor dissipation.
Free – free [95]	The anchor is located at the vibration node point and suspended by other beams.	10 MHz – 100 MHz; high Q at high frequency.
Square [96]	A square plate is suspended. It can zooming in and out in-plane or vibrate out-of-plane.	10 MHz - 500MHz; high output power; high Q at high frequency.
Disk [97]	A disk plate is suspended. It is like square plate.	20 MHz – 1.5 GHz; high output power;
Ring [98]	A ring is suspended like square plate.	100 MHz – 5 GHz; Q is around 1 K – 10 K.

This chapter proposes a new type of RF MEMS resonator based on MOS tunneling current strain sensor. This new type of RF MEMS resonator will be thoroughly discussed from design, fabrication to measurement.

6.2 Bulk Acoustic RF resonator based on MOS tunneling current strain sensor

The goal is to demonstrate a RF resonator based on MOS tunneling current strain sensor. A simple structure which can provide enough strain is preferred. Therefore, the bulk acoustic resonator, which is easy to fabricate, provides high Q and enough strain is adopted. The following sections will thoroughly discuss this type of resonator, including basic theories about resonators.

6.2.1 Principle of bulk acoustic RF resonator

Figure 6.1 shows the 3D structure of a bulk acoustic RF resonator and a schematic showing work principle. In Figure 6.1 (a), the green parts represent beam, electrodes and anchor. The white parts are insulators which isolate beam and electrodes. The yellow part is the substrate. The anchor is located in the middle of the beam, which is the vibration node point. The beam and anchor are normally grounded, while the driving signal is feed on the electrodes on both sides. As shown in Figure 6.1 (b), under electric static force, the two ends of the beam move along opposite direction. One of the benefits of this type of structure is less energy dissipation to anchor and substrate, which leads to high quality factor.

The lowest resonance frequency (f_0), effective mass (m), damping coefficient (γ) and the spring constant (k) can be expressed as

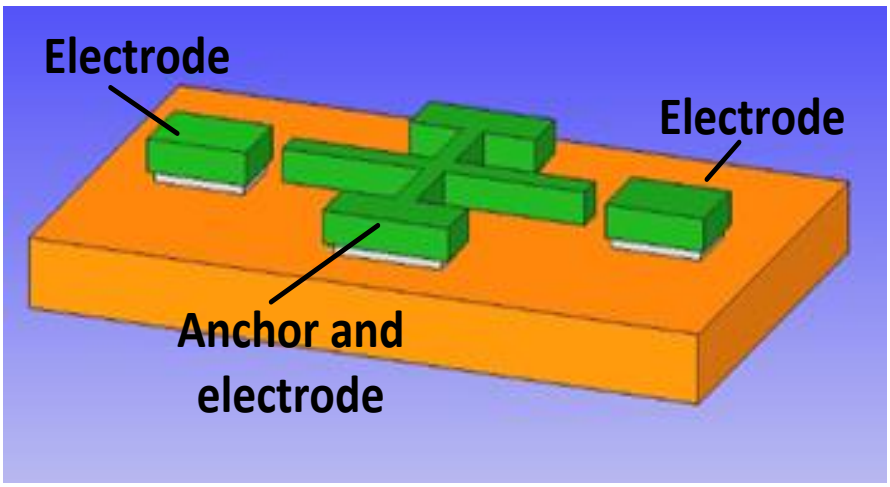
$$f_0 = \frac{1}{2L}\sqrt{\frac{E}{\rho}} \tag{6.1}$$

$$m = \frac{\rho AL}{2} \tag{6.2}$$

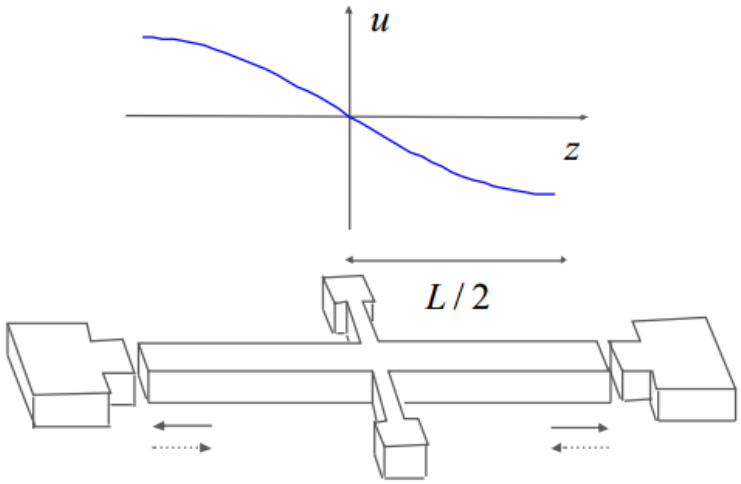
$$\gamma = \frac{bAL}{2} \tag{6.3}$$

$$k = \frac{\pi^2 EA}{2L} \tag{6.4}$$

Where ρ is the material density, A is the beam cross sectional area, L is the length of the beam, b is the viscous damping losses, E is the Young's modulus.



(a)



(b)

Figure 6.1 (a) 3D structure of a bulk acoustic RF resonator; (b) a schematic showing working principle of longitudinal mode beam resonator [9].

6.2.2 Fabrication of Bulk Acoustic RF resonator based on MOS tunneling current strain sensor

A silicon on insulator (SOI) wafer is used to make the device. The SOI wafer has a lightly doped P-type substrate, a 1 μm thick oxide layer and a 20 μm heavily doped P-type top layer silicon. The resistivity of top layer silicon is

0.01 Ohm-cm, while the resistivity of the substrate is 20 Ohm-cm. It is easy to fabricate a bulk acoustic RF resonator using standard MEMS process on SOI wafer. It is also very easy to make MOS capacitors. Therefore, there is no need to elaborate every process. However, it is very tricky to make a resonator together with a MOS capacitor on the resonator beam. Several issues during fabrication and what we do to solve these issues are discussed here.

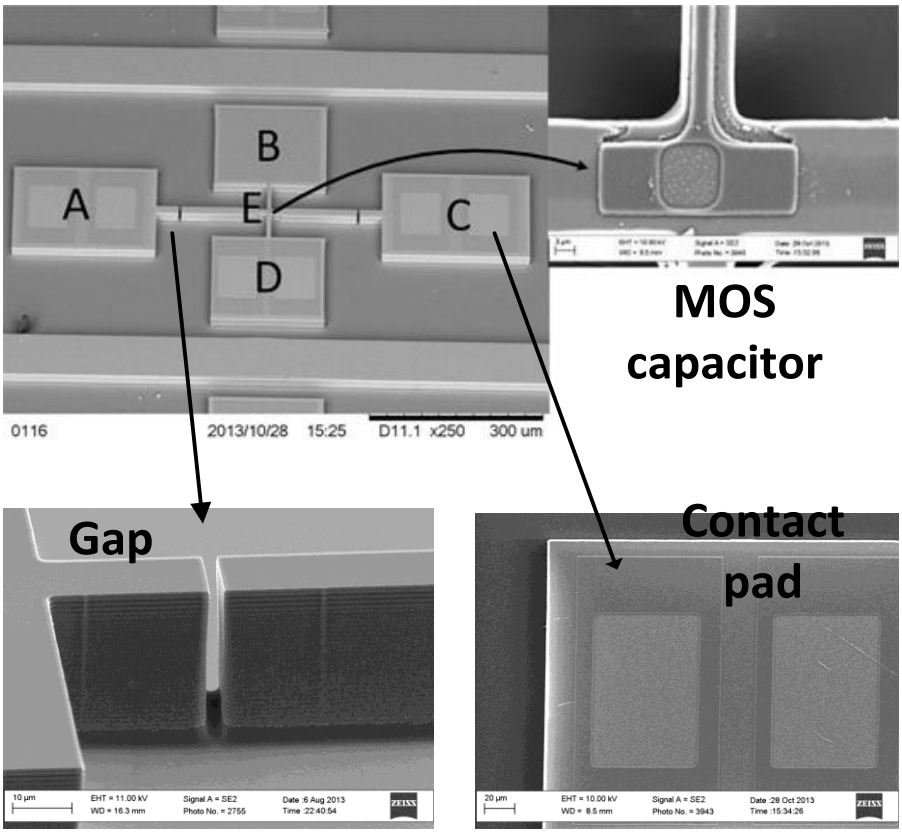
1) If DRIE is done first to etch silicon to form the resonator, there will be 20 μm thick steps on the surface. It is difficult to spin on photoresist smoothly on such surface, thus it is difficult to pattern MOS capacitors on the beams. Therefore, the MOS capacitors have to be made first
2) Another issue is contact. A perfect contact of electrodes between metal gate and silicon requires none oxide and clean silicon surface. Since we thin gate oxide has to be grown for the MOS capacitors, there is also gate oxide grown on the contact pads. One way to remove gate oxide on the contact pads is to use one more mask to pattern a protection layer for MOS capacitors and etch thin gate oxide for electrode, however this step may damage MOS capacitors during BOE. Besides, lift off for metal has to be performed, after sputtering. This step would also damage MOS capacitors. Therefore, gate oxide on the contact pads has to be kept. After the fabrication is completed, a high DC voltage can applied on the contact pads to break this thin oxide.
3) Traditionally, people usually do BOE to etch oxide layer in SOI to release resonator beams. Since this step takes several hours, it could be a serious threat to MOS capacitors. Therefore, one more step to etch

substrate silicon layer to open a window is proposed, which makes the etching oxide layer much faster through the bottom.

4) It is also a problem when comes to which silicon layer to etch first. To etch a 400 μm thick silicon layer, it could take several hours. If we etch bottom layer first, the photoresist on the top layer could be deteriorated badly, which was supposed to be perfect for DRIE for resonators. If the top layer of silicon is etched to form resonators before substrate etch, this long time DRIE could also damage the shape of resonators. A very good protection layer covering top layer after top layer is etch probably a better choice than the deterioration of the photoresist on the top layer. Therefore, it is proposed that top layer is etched first and then the bottom substrate.
5) After open a window in the substrate, there are two options to etch the sacrificial oxide layer. One is BOE. Another one is RIE. Both need protection layer. Since some dies could be etched off during DRIE, it is difficult to spin photoresist layer as a protection layer. Therefore, a crystal bond is used as the protection layer. BOE will not attack silicon, so it can preserve the shapes of resonators. RIE is an isotropic way to etch SiO_2 which also etches silicon more or less depending on the precursors, so RIE could damage the devices. Therefore, BOE is chosen to etch sacrificial layer of SOI wafer.

As a summary of the process, first, the MOS capacitors are made and then make resonators. When the resonators are made, the top layer is etched first and then substrate layer. Both use DRIE. Before etching the sacrificial layer in BOE, the top layer is covered with crystal bond. In the end, acetone is

used to remove crystal bond. However, it should be pointed out that every step in DRIE and BOE could damage MOS capacitors. Figure 6.2 (a) shows the resonators with MOS capacitors before the sacrificial layer is etched. Figure 6.2 (b) to Figure 6.2 (d) shows the final device. Unfortunately, there is a misalignment between top layer and the substrate. The resonator should be located in the middle of the substrate window. The misalignment comes from misalignment of the optical system of bottom side alignment (BSA) in Karl SUSS Mask Aligner MA6/BA6. This misalignment of the optical system should not happen, if a routine maintenance is carried. This misalignment make most beams' release fail, like devices in Figure 6.2 (b) & (c). Even if some beams are released fully, the resonators could suffer from energy dissipation to anchors due to loss of symmetry, like device in Figure 6.2 (d). Figure 6.2 (e) shows the packaged device for testing.



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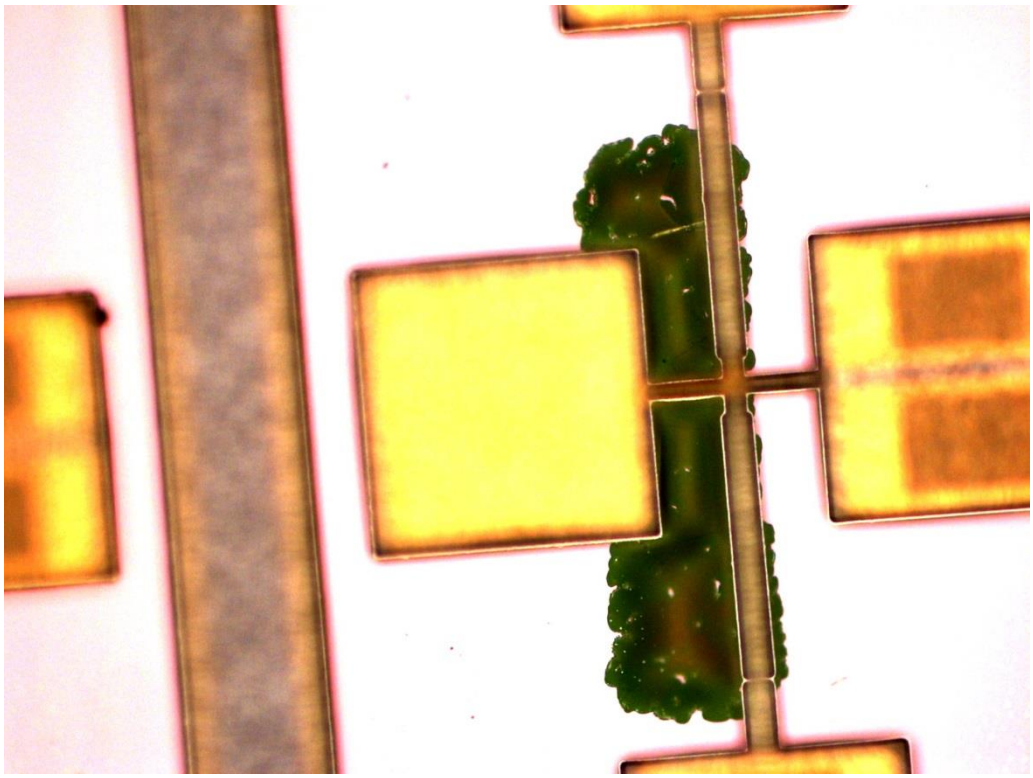

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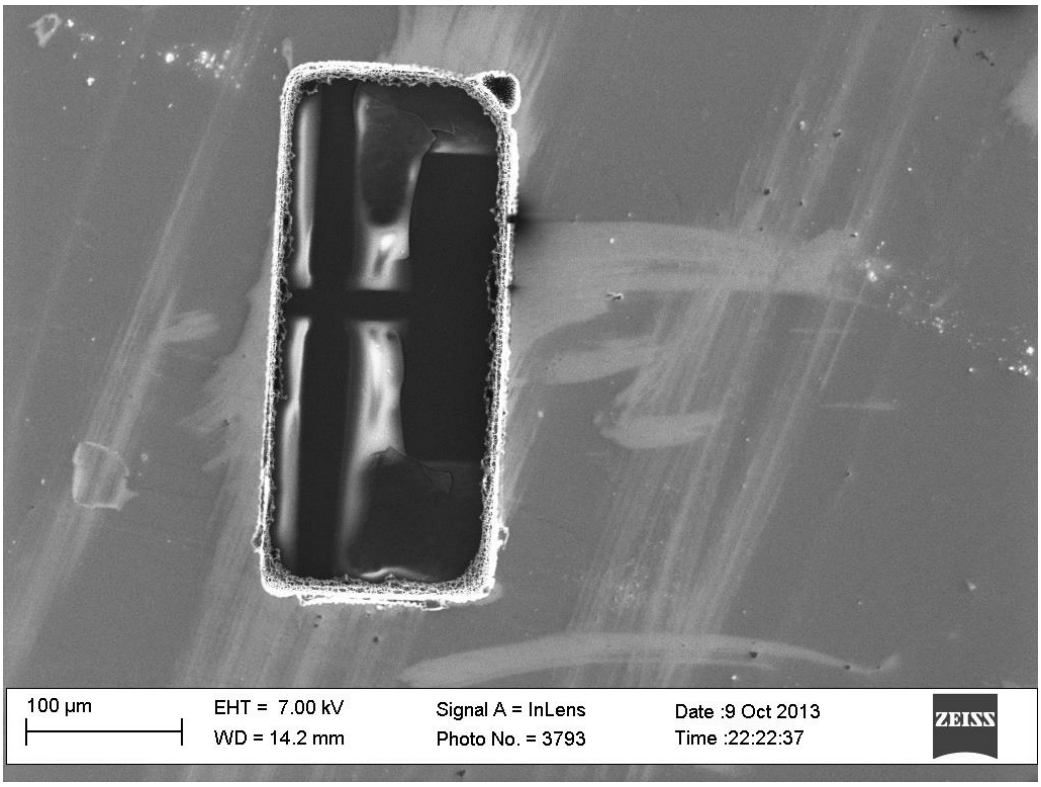
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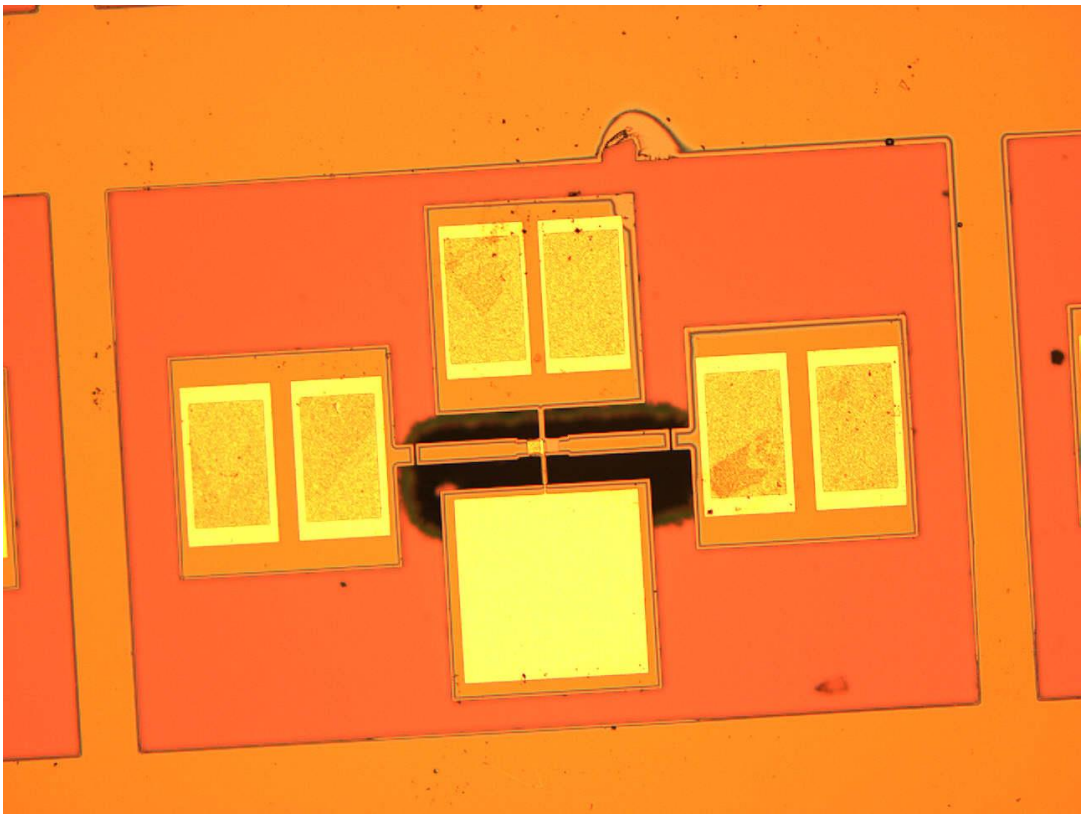

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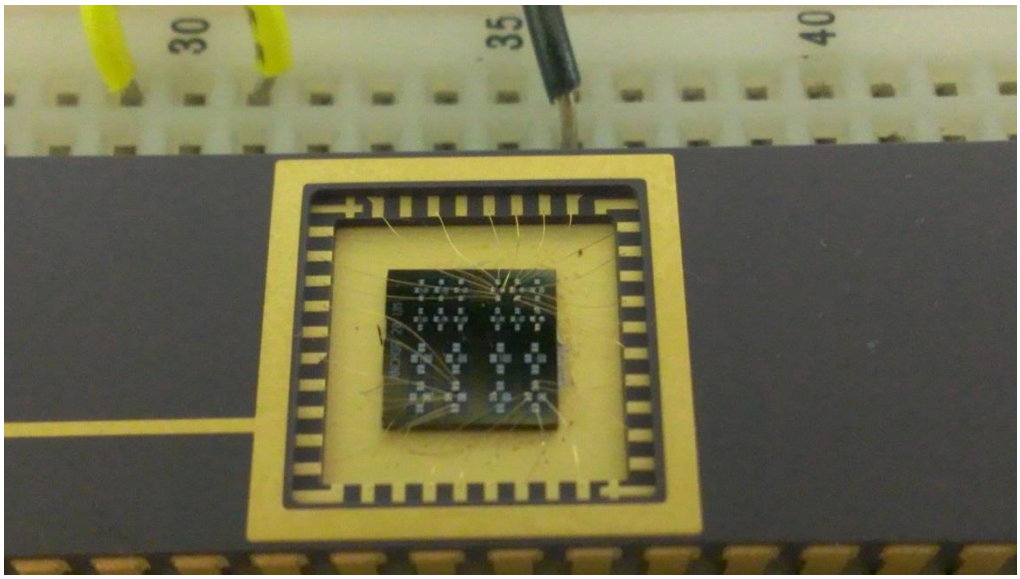


(e)

Figure 6.2 SEM picture and microscope picture of fabricated devices. (a) SEM pictures for top layer before etching sacrificial layer of SOI wafer. (b)

Optical microscope picture for the final device which is misaligned and not fully released. (c) SEM picture of substrate layer for the final device which is misaligned. (d) Optical microscope picture of the final device which is misaligned but full released. (e) Packaged devices for testing.

In Figure 6.2 (a), the contact pads for the AC driving voltage are labelled as A & C, pad B is DC input on the MOS capacitor, pad D is the ground, and E is the place where the MOS capacitor is. Aluminum on pads A, C & D is sputtered onto a thin oxide which will be broken through high voltage. Between aluminum and silicon on pad B, there is a 315 nm thick SiO_2. Table 10 gives dimensions of the resonator. On each die, there are several devices. There are two grounds on the device. One is pad D, and another one is the substrate layer on the bottom. A ground on the substrate layer is necessary to minimize the driving voltage crosstalk with pad B & D through the substrate layer.

Table 10

Parameters of the resonator

Parameter	Definition	Value
L	The length of pads	340 μm
L1	The length of Al contact of pad B	300 μm
T1	The thickness of oxide layer of SOI wafer	1 μm
T2	The thickness of oxide layer of pad B	315 nm
l	The length of beam	310 μm
w	The width of beam	35 μm
h	The height of beam	20 μm
g	The gap between beam and pad A or C	2 μm
LL	The length of one die	6 mm

An equivalent circuit for MOS tunneling current sensing method including equivalent circuit for resonator, driving circuit and parasitic components is shown in Figure 6.3. Table 11 explains the definition of the components in the equivalent circuit, and gives the theoretical number from fabrication. Here A, B, C and D in the definition mean silicon on these pads.

Table 11

Definition of components used in equivalent circuit

Component	Definition	Value
Ca	Capacitor between A and resonator beam	3.1 fF
Cag	Capacitor between A and handler layer	4 pF
Cbb	Capacitor between Aluminum contact and beam on pad B	9.861 pF
Cbdg	Capacitor between B and handler layer in parallel with capacitor between D and handler layer	8 pF
Cc	Capacitor between C and beam	3.1 fF
Ccg	Capacitor between C and handler layer	4 pF
Cg	Capacitor between handler layer and package	400 pF
Cmos	The MOS capacitor between B and beam	6.9 pF, 17.2 pF, 20.7 pF, 100.1 pF (Dependent on area)
Rmos	The MOS capacitor's resistance	Dependent on area & voltage
Rg	The resistor between substrate and package	>220 (10 MHz)
R1	The resistor at the DC input	Best close to Rmos

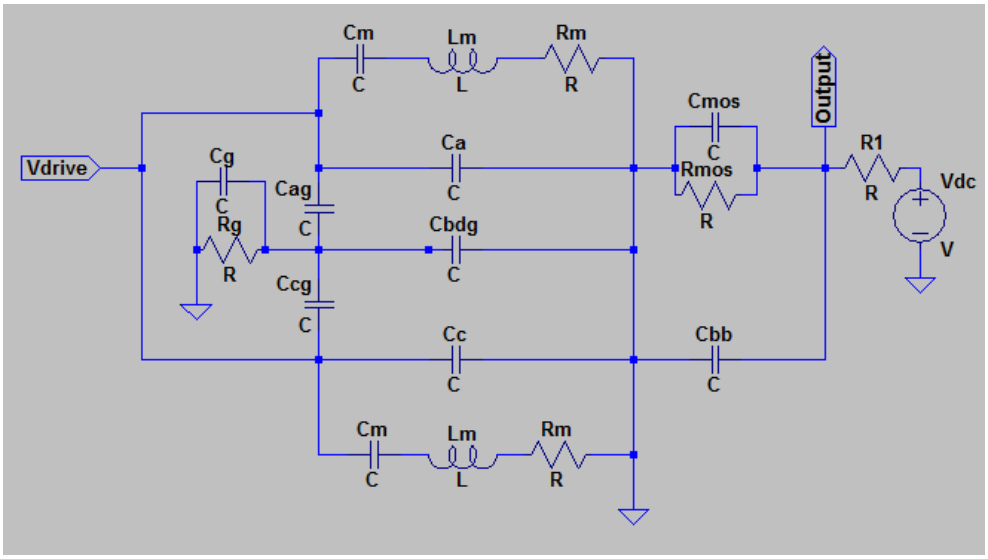


Figure 6.3 Equivalent circuit for MOS tunneling current sensing method.

Cmos depends on the area of MOS capacitors and thickness of gate oxide. Here they are calculated for 2 nm thick gate oxide and several different areas. Rmos not only depends on the area of MOS capacitors and thickness of gate oxide, but the gate voltage, since gate voltage vs. tunneling current is not linear.

The resistor at the DC input, R1, should be chosen carefully to output a detectable AC voltage. Assuming DC supply is V and Rmos equals $R(1+\alpha cos\theta)$ at resonance, where $\theta = 2\pi ft$, α is related to stress, which is far less than 1. Thus,

$$Vmos = V\frac{Rmos}{Rmos + R_1} = V\frac{R(1+\alpha cos\theta)}{R(1+\alpha cos\theta) + R_1} \tag{6.5}$$

If $R \gg R_1$,

$$Vmos = V \tag{6.6}$$

If $R \ll R_1$,

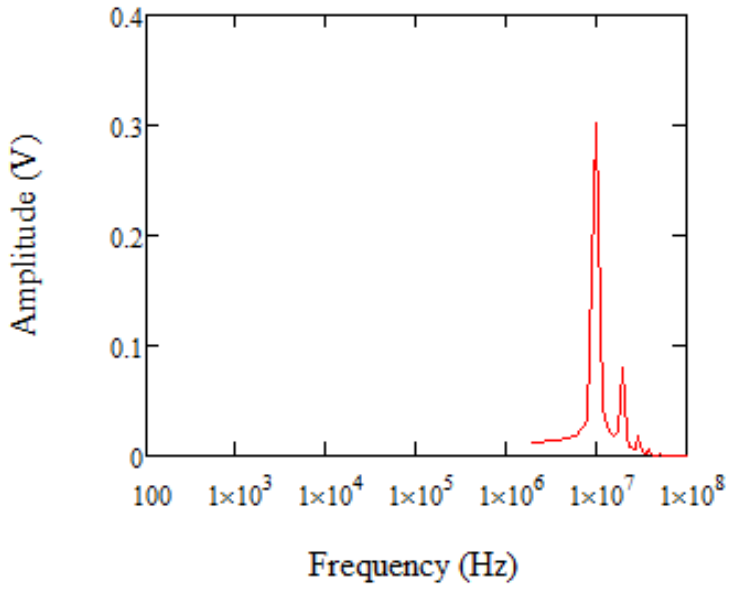
$$Vmos = V\frac{R(1+\alpha cos\theta)}{R_1} \tag{6.7}$$

The AC component is very small, and it makes measurement difficult especially with RF crosstalk present.

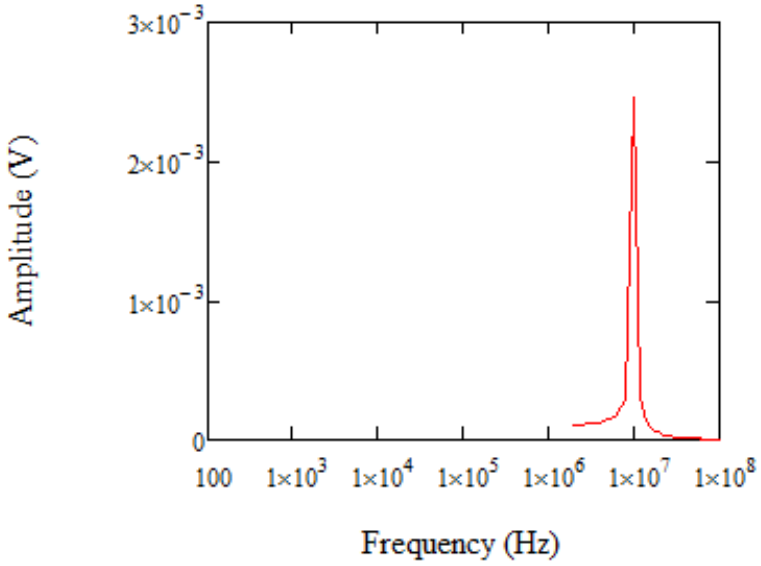
If $R \approx R_1$,

$$Vmos = V\frac{1+\alpha cos\theta}{2+\alpha cos\theta} = V - V\frac{1}{2+\alpha cos\theta} \tag{6.8}$$

This output distorts the pure sine wave of AC output and induces harmonics. The output spectrum of this output in the frequency domain can be analyzed using FFT. Assuming $f = 10\,MHz$, $V = 1\,V$, the output spectrum is shown in Figure 6.4. In Figure 6.4 (a), when $\alpha \gg 1$, the harmonics are present. In Figure 6.4 (b), when $\alpha \ll 1$, the harmonics are depressed and the output is an almost pure sine wave. In most cases, α is far less than 1. Therefore, it is best to choose a resistance close to the MOS capacitor's resistance.



(a)



(b)

Figure 6.4 The output spectrum when $R \approx R_1$. (a) $\alpha \gg 1$. (b) $\alpha \ll 1$.

6.2.3 Bulk acoustic RF resonator testing

This section discusses testing setup for the bulk acoustic RF resonator. The resonator is made to demonstrate the sensing method using MOS tunneling current strain sensor. However, the resonator can also work as a capacitive resonator. The resonator will be tested first using the traditional capacitive sensing method, and then using MOS tunneling current strain sensor way.

Figure 6.5 gives the measurement setups for capacitive sensing and MOS tunneling current sensing. A RF impedance analyzer Hp4294a is used to measurement the resonator. The schematic in Figure 6.5 (a) shows the setup for capacitive sensing method. Hp4294a outputs both DC bias and AC voltage from the connectors of Hpot and Hcur to the left and right electrodes. The connectors of Lpot and Lcur receive signal from the top electrode which

is in contact with beam. The schematic in Figure 6.5 (b) shows the set up for MOS tunneling current sensing method. The driving signal is supplied by a network analyzer and a DC source in the right of the schematic. The DC source in the left of the schematic is applied to the MOS capacitor, and tunneling current through the MOS capacitor is fed into the network analyzer. Figure 6.5 (c) is the picture of measurement set up for the capacitive sensing method. The device is put on a breadboard and put in an aluminum vacuum box. The aluminum box has vacuum BNC connectors to the outside instruments.

Next, the motional resistance R_m, the motional capacitance C_m, and the motional inductance L_m for equivalent circuit of resonator are defined. They can be expressed as

$$R_m = \frac{\sqrt{km}}{Q\eta^2} \tag{6.9}$$

$$C_m = \frac{\eta^2}{k} \tag{6.10}$$

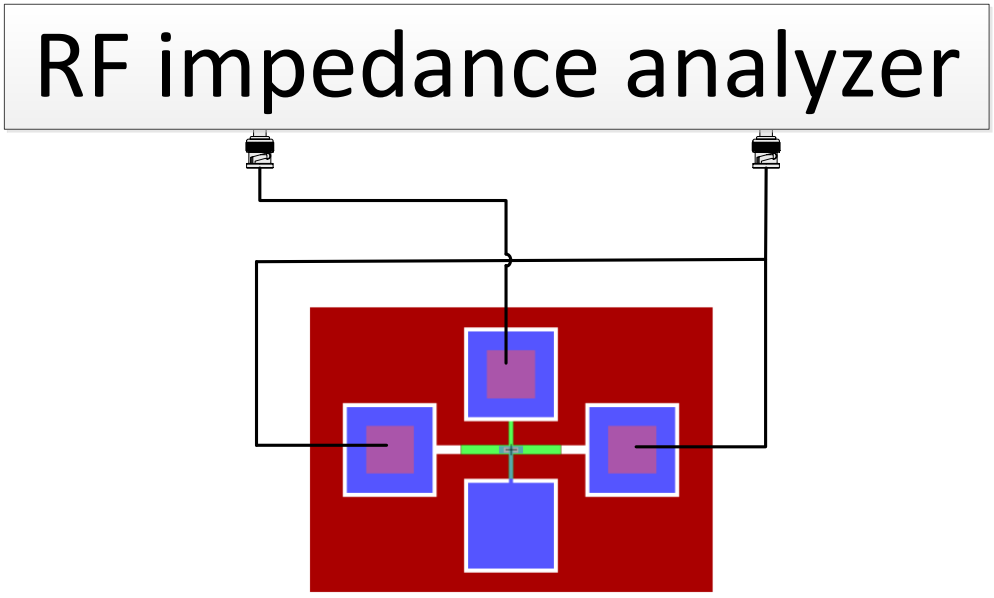
$$L_m = \frac{m}{\eta^2} \tag{6.11}$$

Where η is the electromechanical transduction factor, which relates vibration velocity to the motional current or the ac voltage to the actuation force. For the capacitive sensing method, η can be expressed as

$$\eta \approx V_{dc}\frac{\varepsilon A}{g^2} \tag{6.12}$$

Where ε is the permittivity, A is the cross section area, V_{dc} is the dc bias, g is the distance between beam and electrode pad. Assuming $V_{dc} = 50\,V$ and $Q = 1.8e15$ [85], according to the parameters in Table IX and equations (6.1) – (6.4) and (6.9) – (6.12), we can get $f_0 = 13.643\,MHz$,

$R_m = 10.038\,M\Omega$, $C_m = 0.006456aF$ and $L_m = 21080H$.



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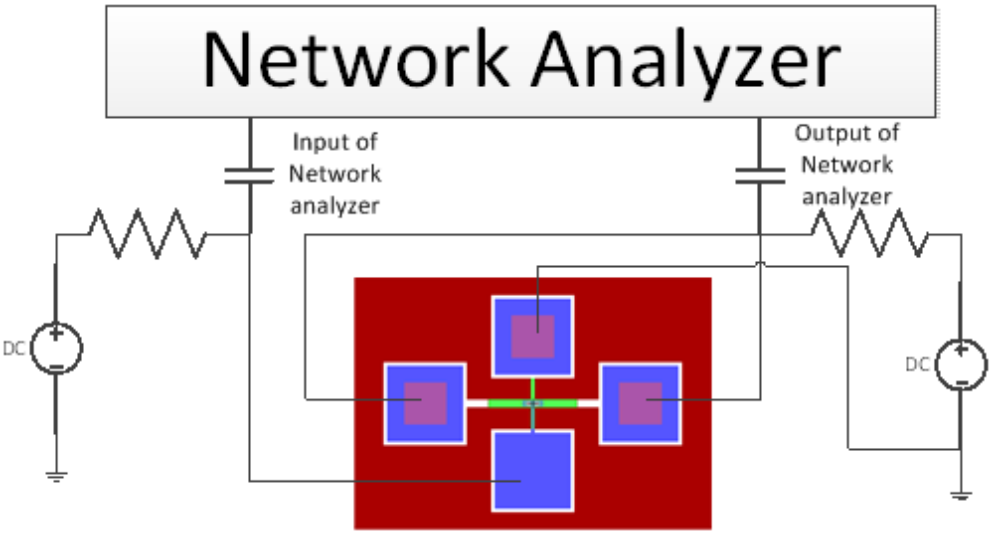

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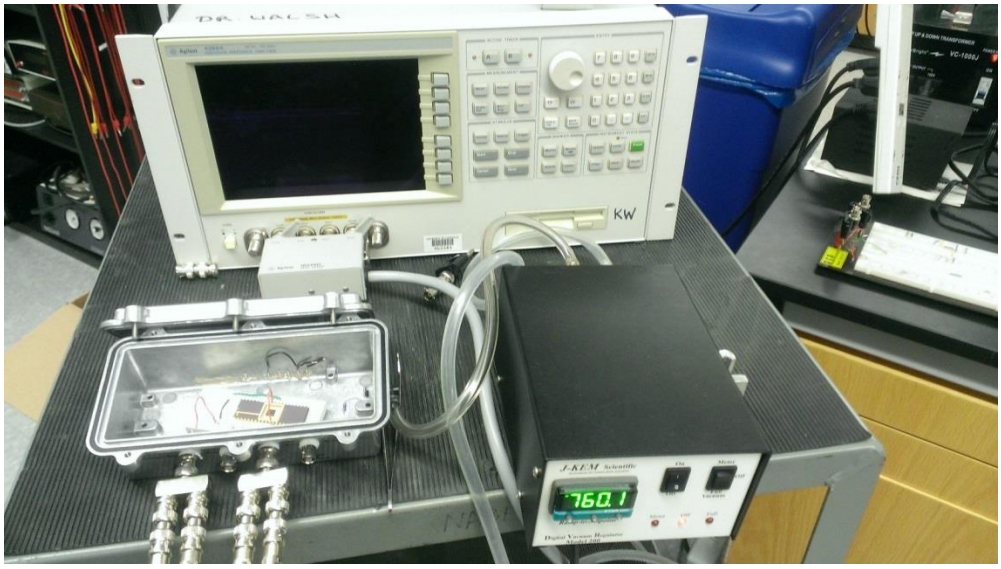


(c)

Figure 6.5 Schematic for measurement set up. (a) Capacitive sensing method measurement set up. (b) MOS tunneling current sensing method measurement set up. (c) Picture of the measurement set up.

6.2.4 Testing and discussion

Unfortunately, the first try to make a bulk acoustic resonator based on MOS tunneling strain sensor was not successful. The MOS capacitors are broken, which were good before DRIE. There is a very large possibility that MOS capacitors can be damaged during DRIE and sacrificial layer etching as discussed in Section 6.2.2. However, even the capacitive sensing method doesn't work. Here several facts that could make the capacitive sensing test fail are listed.

1) Degraded Q due to misalignment. One of the benefits of this design is the driving force symmetrically actuate the beam and anchor is located at the vibration node point. However due to misalignment, the symmetry could be degraded.

2) Cross-talking in testing circuit. A breadboard is used in test, which is not a good choice for RF testing, but should be fine for 10MHz. Short and neat wiring, plus grounding all unused pins should prevent large cross-talking. Replacing device with resistor shows that there is very little cross-talking in testing circuit.
3) Cross-talking in device. There is always cross-talking through substrate. Usually substrate should be grounded to minimize this cross-talking. However, we didn't sputter any metal on the bottom of the substrate, but used conductive epoxy to glue device to package. This conductive epoxy works well for DC measurement, but could be a problem for RF measurement.

Among all of these three facts, cross-talking in device is the most suspicious one. The device is pasted to the package by silver epoxy, which contact impedance is unknown. A RF impedance analyzer, Hp4294a, is used to measure the impedance on the substrate. Three groups of capacitance and resistance, A or C to Bottom, B to Bottom and D to Bottom (refer to Figure 6.2 (a) and Table 10 for definitions) are measured. The results are shown in Table 12. From A (or C) to Bottom, we can see that the capacitance keeps consistent and is close to Cag or Ccg from Table 10, but the resistance decreases with increasing frequency. The resistance from B to Bottom and D to Bottom are close to A or C to Bottom. The capacitance is almost twice of A or C to Bottom, because B and D are connected through beam.

Table 12

Measurement results for substrate impedance

	Frequency (Hz)	R (Ω)	C (pF)
A (or C) to Bottom	50K	8K	4.85
	100K	6.6K	4.75
	1000K	667	4.5
	10 M	331	4.4
B to Bottom	1000K	459	7.66
	10 M	220	7
D to Bottom	1000K	344	8.6

From Table 12, it is found that at 10 MHz, the substrate resistance is at least 220 Ω. This resistance can come from the resistance of substrate itself, or the contact on the bottom of substrate. However COMSOL can be used to verify that the resistance of substrate itself is small. Figure 6.6 shows the modeling results. The total current is calculated using surface integration of the current density, which is 0.054 A at 1 V. Therefore the resistance is around 18 Ω. Therefore this high resistance comes from the poor contact on the bottom of substrate.

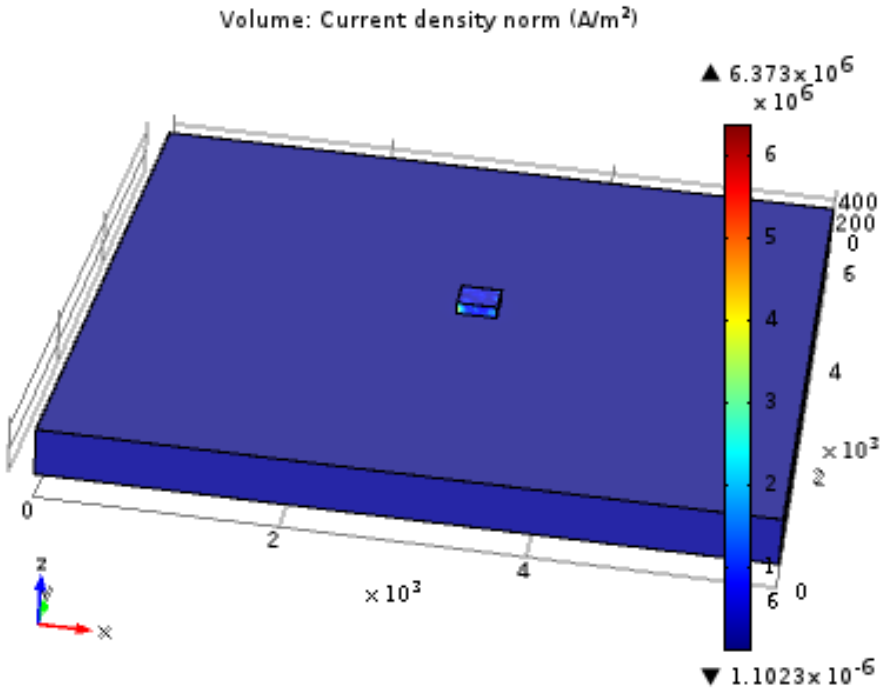
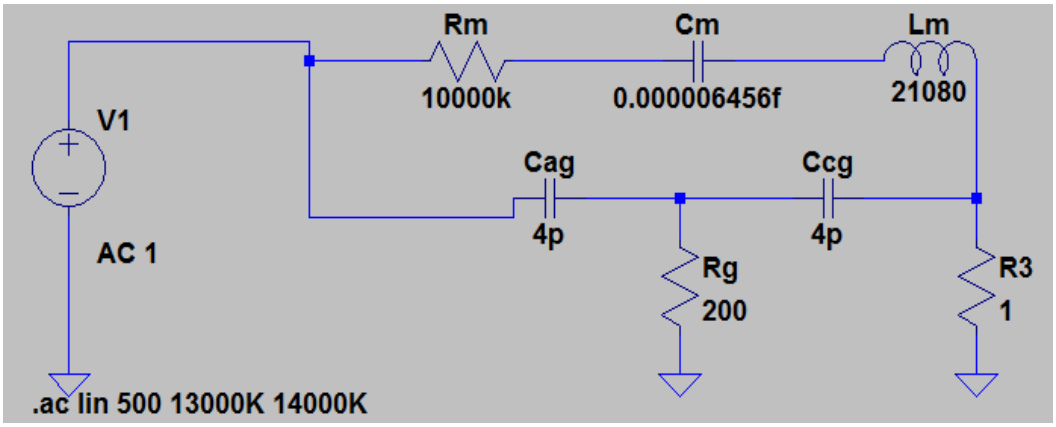


Figure 6.6 COMSOL modeling. The top bulk is contact which is 340 μm (x) *340 μm (y) *100 μm (z). The bottom bulk is Silicon which is 6mm (x)* 6mm (y)* 400μm (z). The voltage is 1 V.

A SPICE simulation is used to find out why this high substrate contact resistance hinders the capacitive sensing testing. Figure 6.7 (a) shows a simplified equivalent circuit for capacitive sensing. R3 is the output. Figure 6.7 (b) shows the simulation result with $Rg = 200\ \Omega$. It is clear that the response is so small that it is easy to be buried in noise. Figure 6.7 (c) shows the simulation result with $Rg = 1\ \Omega$, which has a larger output.



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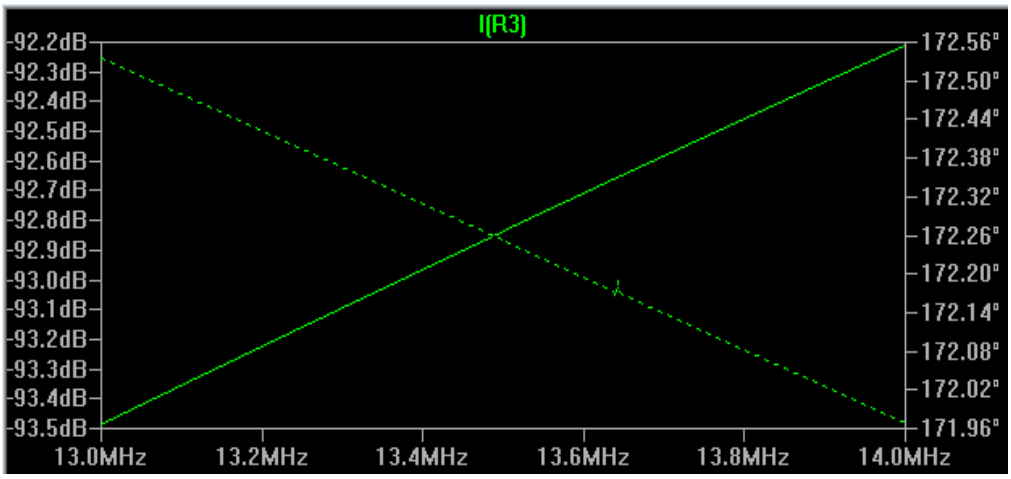

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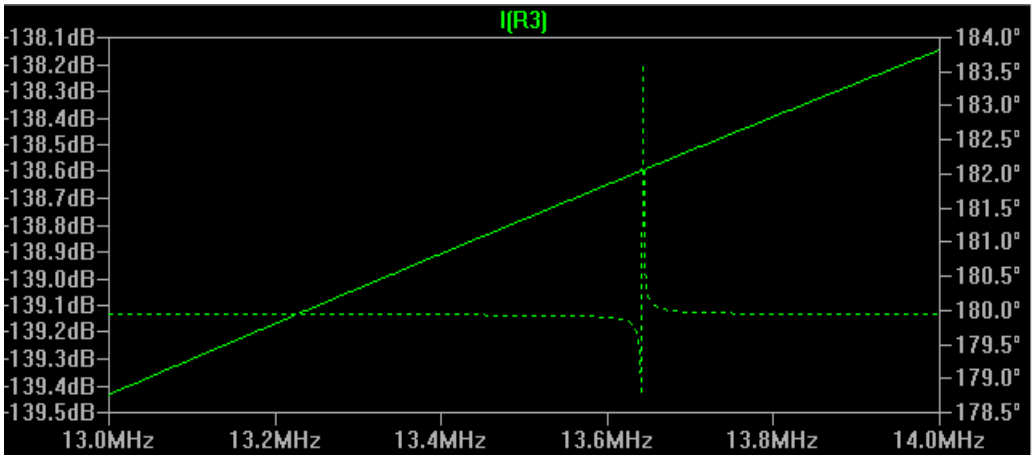

(c)

Figure 6.7 Spice modeling of substrate contact influence on capacitive sensing method. (a) Equivalent circuit for capacitive sensing method. R3 is the output. (b) Simulation result with $Rg = 200\ \Omega$. (c) Simulation result with $Rg = 1\ \Omega$.

6.3 Suggestions for improvement in future

Although the first try is not successful, some useful tips for next try are learned. To easy measure resonance using capacitive method, the impedance of substrate contact has to be reduced. This can be done by sputtering metal on the bottom instead of using conductive epoxy. The area of contact pads can also be reduced to reduce cross-talking among them. The motional resistance R_m can be reduced by increasing electromechanical transduction factor η or reducing effective mass. Since the goal is to make a RF resonator based on MOS tunneling current strain sensor, the most important thing is to protect MOS capacitors during DRIE and sacrificial layer etching. Perhaps some process protocols from integrated CMOS-MEMS products can be adopt to protect MOS capacitors.

CHAPTER 7

CONCLUSIONS AND FUTURE DIRECTIONS

7.1 Conclusions

MEMS strain sensors have been widely researched and commercialized for decades, which can be used in pressure sensor, accelerometer and gyroscope. Nowadays, portable electronics have an increasing requirement for low power sensors, which motivates our research on MOS tunneling current strain sensor. Due to high resistivity of gate oxide, the tunneling current can be in the nano-amp range, which is a good alternative for low power sensing. In this dissertation, a low power MOS tunneling current strain sensor is demonstrated. In the experiment, the noise, sensitivity and drift are characterized. A computationally efficient model for MOS tunneling current is built, which fits this dissertation's experiments as well as other groups' experiments. A bulk acoustic RF resonator based on MOS tunneling current strain sensor is also made. The resonator doesn't work. The reasons why the resonator does not work are discussed, and possible modifications for future research are proposed. In conclusion, the main contributions of this dissertation can be summarized as:

1) A low power strain sensor was made. From DC measurement, it is found that the minimum detectable strain with regards to noise and sensitivity. It is also found that the gauge factor of MOS

tunneling current strain sensor is in the range of piezoresistive strain sensor.

2) In DC measurement, the MOS tunneling current strain sensor is studied thoroughly from positively bias to negatively bias. With regards to noise, it is found that the device performs best in the inversion region.
3) The current drift in MOS tunneling current is studied at different biases. It is found that at different bias, drift behaves different. At high bias, the drift rate is large and MOS tunneling current increases. At low bias, MOS tunneling current decreases.
4) A lock-in amplifier is used to perform AC measurement to characterize MOS tunneling current strain sensor. It is found that sensitivity of AC method is close to DC method, but AC method is more efficient in reducing noise than DC method. As for drift, it is fount that it is impossible to remove drift using AC method.
5) Computationally efficient models are built for MOS tunneling current considering both ECB tunneling current and EVB tunneling current. The computational efficiency comes from the adoption of approximate methods for the sub-bands for ECB tunneling current and WKB method for the tunneling probability for both ECB tunneling current and EVB tunneling current. The model fits experimental results well. It is found that it is acceptable for current density modeling if only ECB tunneling current is considered like other groups did. However, when substrate doping concentration is large, EVB tunneling current has to be included for sensitivity study.

6) A bulk acoustic RF resonator based on MOS tunneling current strain sensor is made. Although the resonator did not work, possible reasons for not working are discussed, which is helpful for future research. From this first try, it is also found that which processes are critical.

7.2 Future directions

Directions of future research are proposed and discussed in this section. They are sensitivity study at different stresses, bolometer based on MOS tunneling current and continuing research on RF resonator based on MOS tunneling current strain sensor.

7.2.1 Sensitivity study at different stresses

The purpose of sensitivity study at different stresses is to improve the performance of the sensors. The minimum detectable strain is determined by both the sensitivity and the noise. Increasing the sensitivity and lowering the noise both can achieve a smaller the minimum detectable strain. Making very high quality ultrathin SiO_2 is the fundamental way to reduce noise. It requires very high quality of wafers, very precise control of gas flow rate, temperature and ultra-low contaminations, which is very time consuming. Therefore an alternative approach is to study sensitivity at stresses along different orientations. Silicon at different type of stresses may cause different changes to the band structure, which will change the sensitivity of tunneling current response to stress.

The setup of the experiment is shown in Figure 7.1. A (001) wafer with MOS devices arranged circularly is laid on an O-ring. A micrometer presses the center of the wafer to introduce stress to the wafer, so stresses at different

directions will be applied to MOS devices at different locations. Tunneling current is measured by a semiconductor parameter analyzer.

Figure 7.1 Setup for sensitivity study at different stresses.

7.2.2 Continuing research on RF resonator based on MOS tunneling current strain sensor

Some ideas are learned from this first failure try on RF resonator based on MOS tunneling current strain sensor.

1) It is best to make a capacitive resonator without MOS tunneling current strain sensor. This capacitive resonator can be used to verify whether the resonator will resonate. Without MOS tunneling strain sensor, process will be simple and it is easy to control process quality.
2) Reduce contact pads to reduce parasitic capacitors which will then decrease cross-talking.

3) Use a SOI wafer with both top layer and substrate layer heavily doped. This can decrease resistance in the substrate, which also helps reduce cross-talking.
4) Use SOI wafer with a thinner top layer which will make DRIE much easier, and in the same time decreases motional resistance.
5) To easy measure resonance using capacitive method, we need to reduce the impedance of substrate contact. Sputtering metal on the bottom instead of using conductive epoxy is necessary.
6) Since the goal is to make a RF resonator based on MOS tunneling current strain sensor, the most important thing is to protect MOS capacitors during DRIE and sacrificial layer etching. Perhaps some process protocols from integrated CMOS-MEMS products can be adopt to protect MOS capacitors.

7.3 Bolometer based on MOS tunneling current

During the research, it is found that MOS tunneling current is also very temperature sensitive, which makes it a potential technology for bolometer. There are several facts about MOS tunneling current's response to temperature changing:

1) For ultrathin gate oxide, there are two main MOS tunneling current. Above 348 K, MOS tunneling current exponentially depends on 1/T, which means thermionic type of emission dominates. Below 348 K, MOS tunneling current weakly depends on temperature, which means direct tunneling current dominates [26].
2) Another fact is that the thinner the gate oxide and the lower the doping concentration, the higher sensitive the direct tunneling

current responses to temperature changing [99].

3) The third fact is that MOS capacitor at low electric field gives more sensitive to temperature changing [100].

Figure 7.2 lists parameters of some commercial and state-of-art uncool infrared bolometers. Table 13 gives some measurement results using the MOS capacitors. The measurement is done using a temperature controllable vacuum chamber and a semiconductor parameter analyzer. To achieve at least the performance of the existing bolometers, future research needs to reduce noise by growing high quality gate oxide or increase MOS tunneling current response to temperature.

Table 1: *Commercial and state-of-the-art R&D uncooled infrared bolometer arrays.*

Company	Bolometer type	Array format (pixels)	Pixel pitch (μm)	Detector NETD (F=1, 20-60 Hz)
FLIR, USA	VO_x bolometer	160x120 - 640x480	25	35 mK
L-3, USA	VO_x bolometer	320x240	37.5	50 mK
	α-Si bolometer	160x120 - 320x240	30	50 mK
BAE, USA	VO_x bolometer	320x240 - 640x480	28	30-50 mK
	VO_x bolometer (standard design)	160x120 - 640x480	R&D: 17	50 mK
DRS, USA	VO_x bolometer (umbrella design)	320x240	25	35 mK
	VO_x bolometer (umbrella design)	320x240	R&D: 17	50 mK
Raytheon, USA	VO_x bolometer	320x240 - 640x480	25	30-40 mK
	VO_x bolometer (umbrella design)	640x512	R&D: 17	50 mK
ULIS, France	α-Si bolometer	160x120, 640x480	25-50	35-100 mK
Mitsubishi, Japan	Si diode bolometer	320x240	25	50 mK
NEC, Japan	VO_x bolometer	320x240	23.5	75 mK
SCD, Israel	VO_x bolometer	384x288	25	50 mK

Figure 7.2 Table of commercial and state-of-the-art R&D uncooled infrared bolometers.

Table 13

Experiment result

Devices	NETD
3.9 nm gate oxide, aluminum gate	290 mK
3.9 nm gate oxide, nickel gate	110 mK

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EXPERIENCE

Research Assistant
University of Louisville
Aug. 2009 – Present (4 years 7 months)
Dissertation:
Low power strain sensor based on MOS tunneling current

- Built models for MOS tunneling current in strain sensor.
- Fabricated MOS tunneling strain sensor in cleanroom.
- Tested the device using both DC and AC method. HP4145a was used in the DC method. For the AC method, designed a preamplifier circuit to transfer tunneling current to voltage and used SR7265 lock-in amplifier to measure the tunneling current. Used Labview to control Hp4145a semiconductor analyzer and SR7265 lock-in amplifier.

- Developed MOS tunneling current RF resonator (12 MHz). Coventorware and COMSOL were used to design the resonator. Fabricated in University of Louisville's cleanroom. Tested using network analyzer, LCR meter and oscilloscope.

Research Assistant
Beijing Institute of Technology
Jan. 2007 – June 2009 (2 years 5 months)
Thesis:
System design and simulation of 0.2 THz radar

- System design of a 0.2 THz stepped frequency transmitter and receiver.
- Used Simulink in Matlab to simulate the space resolution of the radar in a system level.
- Used ADS to simulate power and noise of the output of the transmitter line by using parameters from actual parts.

TEACHING EXPERIENCE

- Introduction to microelectronics (lab in the cleanroom and lecture), Spring semester, 2012 & 2013;
- Microelectronics design and fabrication (lab in the cleanroom and part time lecture), Spring semester, 2013;
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AWARDS

- University Fellowship, University of Louisville, 2009;
- Graduate admission with qualification exams waiver, Beijing Institute of Technology (BIT), 2007;
- Renmin scholarship, first class, BIT, 2005 – 2006;
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PUBLICATIONS & POSTERS

[1]. Li Zhu, Ruchira Dharmasena and Shamus McNamara, "MOS Tunneling Strain Sensor Using an AC Measurement Technique," *IEEE NEMS, 2013 Suzhou, China: p.1159-1162.*

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