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# Driving microfluidic flows with three dimensional electrodes.

Yehya Mohamed Senousy 1982-  
*University of Louisville*

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DRIVING MICROFLUIDIC FLOWS WITH THREE DIMENSIONAL  
ELECTRODES

By

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Submitted to the Faculty of the  
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in Partial Fulfillment of the Requirements  
for the Degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering  
University of Louisville  
Louisville, Kentucky

May 2012

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A Dissertation Approved on

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## DEDICATION

This dissertation is dedicated to  
my loving parents who have always supported me in all of my decisions and gave me a  
huge amount of encouragement, even though I was far away from them.

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First, I would like to thank God the merciful and the compassionate for all of the blessings and for granting me the opportunity to accomplish my Ph.D. degree successfully.

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## ABSTRACT

### DRIVING MICROFLUIDIC FLOWS WITH THREE DIMENSIONAL ELECTRODES

Yehya Mohamed Senousy

February 10<sup>th</sup>, 2012

Most of the structures in submillimeter-scale engineering are created from thin films, making them essentially two-dimensional (2D). Significant work has been done to fabricate 3D structures using self-folding, a deterministic form of self-assembly, and three dimensional lithographic and non-lithographic patterning.

The objective of this work is to propose different fabrication and patterning strategies of 3D structures used as pumping electrodes for microfluidic applications. 3D electrodes drive flows over the whole channel height while 2D electrodes stay near one wall.

The first application of the 3D electrodes is mixing chemical or biological samples with reagents for chemical analysis which is one of the most time consuming operations in microfluidic platforms. The mixer used is based on the electrokinetic phenomenon of induced charge electro-osmosis (ICEO). ICEO creates microvortices around polarized posts with gold coated sidewalls, connected to embedded electrodes, by application of alternating current (AC) electric fields. These microvortices around posts help in mixing the two reagents very quickly. These vertical sidewall gold coated posts



and embedded electrodes are fabricated using 3D photolithographic patterning and an ion milling fabrication technique.

The second application is fast ac electro-osmotic (ACEO) pumps using 3D electrodes. These 3D electrodes dramatically improve the flow rate and frequency range of ACEO pumps over the planar electrodes. A non-photolithographic electrode patterning method is proposed to fabricate such electrodes. The method is based on shadowed evaporation of metal on an insulating substrate. This method is considered to be simple and cost effective compared to others used to create these stepped 3D electrodes.

Finally, a self-folding technique is proposed to create out-of plane three dimensional electrodes for ACEO tube pumps. The technique depends on the strain mismatch between two different layered sheets of material. One layer usually has compressive stress, i.e. thermally grown  $\text{SiO}_2$ , and the other has relatively tensile stress, i.e. metals. The design is similar to the planar electrodes design in the literature, except as a 3D electrode it interacts with a larger volume of fluid for a more efficient pump.

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## CHAPTER I

### INTRODUCTION

Three-dimensional electrodes are investigated in this dissertation because of their ability to drive and sense flows in microfluidic devices. One of the major challenges in the microscale industry is the fabrication of three dimensional structures, especially when considering how to fabricate them in a parallel and cost effective manner. This is because most semiconductor processing equipment is designed to produce thin-film planar electrical connections. Driven by the need to connect multiple layers of circuitry, and also by emerging applications such as lab-on-a-chip devices, many new techniques have been developed over the last two decades to fabricate submillimeter three dimensional structures. Some of these include lithographic patterning, non-lithographic patterning, and self-folding techniques.

Lithographic patterning is widely used to fabricate miniaturized electronic, mechanical, and microfluidic devices. There are many lithographic patterning processes that have been used to create three dimensional structures, such as surface [1] and bulk micromachining [2], electron beam lithography [3], focused ion beam (ion milling) [4] and X-Ray lithography [5]. There is also electrochemical fabrication (EFAB), which is combined conventional photolithography lithography with other techniques (electrodeposition, etching, and planarization) ([6], [7]).

Many non-lithographic processes have also been developed to obtain three dimensional structures without using expensive photolithography techniques. Laser shots followed by wet chemical etching have been used to fabricate arrays of silicon pillars, and macropores [8]. Pen shaped microneedles ( [9], [10]) have been fabricated using anisotropic wet etching and dicing technology. Nanoscaled interdigitated electrodes have been fabricated using a cost effective method based on the directionality of a vacuum evaporation process, which omits expensive lithography steps completely [11].

The self-folding technique is a self -assembly technique. It is used to obtain three dimensional out of plane structures. This technique depends on the strain mismatch between two thin films. Such structures are desired in many applications where microelectromechanical systems must interface with items in the external environment such as, mirrors [12], stages [13], shutters [14], corner-cube reflectors [15] to handle optical signals, out of plane directed cantilevers to act as field emitters [16], nanopipelines to handle fluids [17] and microscopic containers for sample archiving in environmental and biomedical sensors [18]. The technique is used to produce electrostatic, chemical and thermal actuators for cell manipulation [19].

Three dimensional structures are used as micro electrodes for many applications including, electrochemical sensing and detection( [20], [21], [22] and [23]),Li-ion microbatteries [24], neuroscience( [25], [26] and [27]) and lab-on-a chip applications, i.e. cell manipulation( [28], [29]) and cell separation( [30], [31] and [32]). This chapter, a brief introduction of the fabrication techniques used to obtain three dimensional electrodes for different microfluidic devices will be given.

## **A. Induced Charge Electroosmosis (ICEO) microfluidic mixers**

Mixing chemical or biological samples with reagents for chemical analysis is one of the most time consuming operations in microfluidic platforms. This is primarily due to the low rate of diffusive transport in liquid systems. Induced charge electroosmosis (ICEO), a novel electrokinetic phenomenon, is a very efficient method of mixing fluids at microscales in a very short amount of time at low potential and low frequency. ICEO creates microvortices within a fluidic channel by application of alternating current (AC) electric fields. The microvortices are driven by electrostatic forces which act on the ionic charge, which is induced by the field near three-dimensional (3D) metal structures.

The contribution of the dissertation in the area of ICEO is as follows:

1. Development of a new microfabrication process is developed for three-dimensional posts with vertical sidewalls, which have conductive metal coatings and embedded three-dimensional electrodes.
2. Carry out mixing experiments are carried out in the devices and then compare the results to a three dimensional model based on a finite volume method.

## **B. 3D Alternating current electro osmosis (ACEO) microfluidic pumps using:**

### **1. Shadowing evaporation for electrode patterning**

Electroosmosis is a pumping technique which has been explored to replace the traditional pressure driven flows. ACEO is a specific realization of the ICEO. AC electroosmosis has been used to pump fluids over two dimensional, co-planar electrodes by applying alternating voltages across the electrodes. It has been called “ACEO” because the peak velocity of the fluid over the electrodes occurs at a particular AC

frequency and decays above and below this frequency. Three dimensional (3D) electrodes dramatically improve the flow rate and frequency range of AC electro-osmotic pumps compared to planar electrodes. However, the fabrication of 3D stepped electrodes for AC electroosmosis (ACEO) pumps usually involves several expensive steps.

The contribution of the dissertation in the area of ACEO is as follows:

1. Fabrication of stepped 3D electrodes using a faster and less expensive method.

The method is based on shadowed evaporation of metal on an insulating substrate such as injection molds.

2. Measurement of the flow velocity of the fluid over the electrodes at different frequency and voltage settings for comparison to the settings in the previous work.

## **2. Out of plane 3D electrodes**

Recently, techniques known as ‘micro-origami’ or strain architecture’ have emerged for the fabrication of out-of-plane micro and nanostructures by relaxation of a pair of strain-mismatched thin films. This technique is considered to be a self-folding technique, which is a deterministic form of self-assembly that is simple and cost effective. Applications of such structures include optical reflectors, actuators and micropositioners. The structures remain planar until released by  $\text{XeF}_2$  dry silicon etching, making it possible to integrate them with other MEMS and microelectronic devices.

The contribution of the dissertation in the area of self-folded microfluidic devices is applying self-folding to create strong out -of- plane electrodes for ACEO pumping of fluid inside a tube of these electrodes.

### **C. Dissertation Organization**

This dissertation consists of five chapters of which this introductory chapter is the first. Chapter two includes an introduction to chip mixing, the background on ICEO, the micofabrication process of the 3D embedded electrodes and the mixing device, the numerical model of the mixing device, experimental results and finally, the comparison between the experimental results and the numerical model.

Chapter three includes the origin of the three dimensional AC electro-osmotic (ACEO) pumps, low cost fabrication process, production of interdigitated electrodes by shadow evaporation, the making of fluidic and electrical connections, and the process of testing the fabricated pump and comparing the results to the outcomes obtained by other methods.

Chapter four focuses on the strain mismatch technique, one of the self-folding techniques to fabricate 3D out of plane structures. It describes the theory of the technique to obtain the out of plane structures. In addition, the chapter will show the future applications of the technique to obtain free standing electrodes for ACEO pumps. Finally, Chapter five outlines a brief summary of the contribution presented in the dissertation in addition to the future work.

## CHAPTER II

### INDUCED CHARGE ELECTRO-OSMOTIC MIXERS

Mixing chemical or biological samples with reagents for chemical analysis is one of the most time consuming operations on microfluidic platforms. This is primarily due to the low rate of diffusive transport in liquid systems. To overcome this problem, a mixer for microfluidic sample preparation based on the electrokinetic phenomenon of induced-charge-electroosmosis (ICEO) is introduced. ICEO creates microvortices within a fluidic channel by application of alternating current (AC) electric fields. The microvortices are driven by electrostatic forces acting on the ionic charge induced by the field near polarizable materials. By enabling mixing to be turned on or off within a channel of fixed volume, these electronically controlled mixers prevent sample dilution—a common problem with continuous flow strategies. A new microfabrication process was developed for ICEO mixing devices with vertical sidewalls having conductive metal coatings and embedded electrodes. Experiments were carried out to evaluate mixing efficiency in the devices and the results will be compared to the numerical model.

#### **A. Introduction**

The low rate of diffusive transport in liquid systems is an obstacle when mixing chemical or biological samples with reagents. In recognition of the need for more efficient and effective mixing methods, ongoing research and development of microfluidic devices has been reported in previous work.

Devices for on chip integration can be divided into two broad classes, passive and active. Passive devices rely on the fluid transport mechanism to create flows for mixing. Dispersion is a main problem in passive devices that rely on flow streamlines to mix the liquids as they move down a channel, because the sample spreads out longitudinally into a volume that increases for the duration of the passive mixing process. Active devices do not suffer from this problem because they are stationary. They use an independent source of motion. Oddy et al. [33] developed a mixing device based on conventional electroosmosis that requires large electric fields to drive an oscillating motion in a large microfluidic channel. This method basically shakes the fluid back and forth with sufficient force to create instability in the fluid motion resulting in mixing. However, it requires a large electric field at a very low frequency, where it is at risk of forming bubbles by electrolysis.

Induced Charge Electroosmosis (ICEO) has been considered for performing microfluidic mixing operations [34]. Wang et al. developed a mixer based on ICEO using a free-floating metal granule placed within a microfluidic channel to provide the polarizable material [35]. A mixing device is considered here based on the ICEO mechanism that results when an electrical conductor is present in a liquid where an electric field is applied [36]. The ability to control the position, shape, and potential of the flow 'inducing surfaces' in microchannels helps in confining the mixing operation in a prescribed volume and prevents dispersion of the sample occurred in the passive mixing devices. The proposed ICEO device is designed and developed without using moving parts and with a large number of polarizable surfaces to take greater advantage of the ICEO phenomenon.

## **B. Background on ICEO**

ICEO results when an electrical conductor (polarizable material) is placed in a liquid (electrolyte) with an electric field present. Consider a cylindrical conductor immersed in an electrolyte with an electric field present as shown in Figure 2.1(a). The conductor has a free floating voltage and is free of current. It becomes polarized so as to make the field within it zero to maintain zero internal current. The resulting distribution of free charge on the surface of the conductor attracts counter ions in the surrounding electrolyte such that an electrical double layer is formed adjacent to the conductor surface. The applied field acts on this ionic charge layer, which has been created by the field itself. The mobile ions move in response to the electric field, and the ions drag the surrounding fluid with them by viscous forces.

The ICEO flow pattern depends on the shape of the conductor. A symmetric shape typically results in symmetric recirculating flows surrounding the conductor. In the case of the cylindrical conductor, shown in Figure 2.1(a), the flow will be composed of four symmetric vortices. There may be many of these conductors resulting in a periodic flow pattern. An asymmetric shape, such as the triangle shown in Figure 2.1(b), creates non-symmetric flows because the flow streamlines follow the non-symmetric shape of the post itself ([36], [34], [37] and [38]). ICEO can drive steady flows using either AC or DC fields.

In the case of AC field, when the field switches direction, the polarization direction of the conductor switches with it as does the sign of the ionic charge in the double layer. As a result, the direction of fluid motion remains unchanged. This theory assumes that the electric field is small, where the ICEO phenomenon is in the weakly



nonlinear regime. It assumes that there are no faradaic currents at the conductor surfaces, which would decrease the charge in the double layer and thus, the flow velocity.

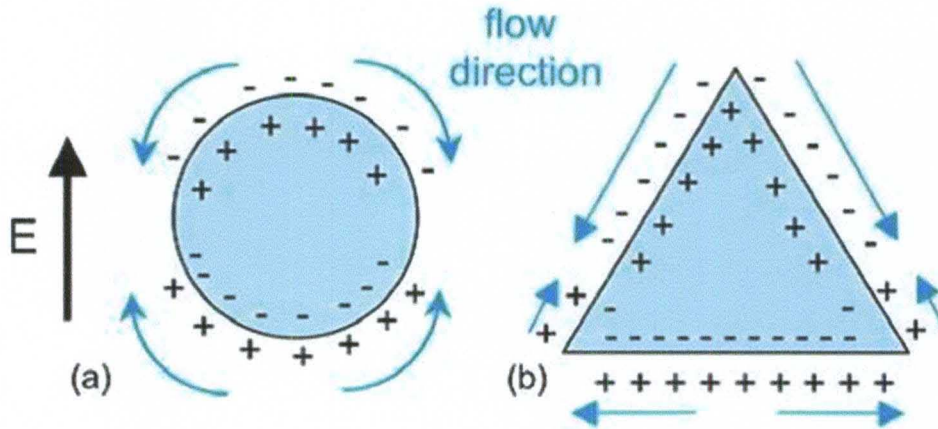


FIGURE 2.1: Schematics of ICEO flow directions in the double layers surrounding cylindrical and triangular conductors [39].

### C. ICEO Devices

Two categories of ICEO devices were fabricated: (1) Devices with isolated cylindrical conductive posts ("Ninja Star" chips), and (2) Devices with through-wafer contacts to electrode structures within the microfluidic channels ("Rectangle" chips). Devices with isolated posts were fabricated on silicon wafers, while integrated electrode devices were fabricated on silicon-on-insulator (SOI) wafers. Ninja Star chips can perform global mixing over long distances (meaning more than one pillar) by chaotic stirring. The vortex pattern is periodically switched so particles escape their home vortex. Meanwhile, the Rectangle chips do not do inter-pillar mixing. They operate by loading different fluids on each half of a pillar by co-flow, and then stirring in each individual vortex achieves local mixing of the two fluids. There is no switching of the vortex pattern in the Rectangle chips, making them simpler to operate. The Rectangle

chips also are more versatile because they can be operated in continuous or batch mode, while Ninja Star, with its longer dwell time, works best in batch mode.

## **1. Devices with isolated cylindrical conductive posts on silicon substrate (Ninja Star Chip)**

### **1.1. Experiments for model validation**

Simple test chips made on polymer substrates were used to validate the model of the cylindrical posts. The chip contains a channel of 50  $\mu\text{m}$  deep, 10000  $\mu\text{m}$  long (1cm) and 1000  $\mu\text{m}$  wide (1mm). At the center of the channel is a 10x5 array of posts with a cylindrical shape 150  $\mu\text{m}$  in diameter. The posts have a “volcano” shape due to the use of an isotropic etch method to make the channel. A gold coating was applied to the lateral surfaces of the posts and chip dimensions were measured and entered into the model. The test chip was then filled with a solution of KCl (typically 0.1 mM) and 200 nm fluorescent polystyrene beads. An electric field was applied to this solution using platinum wire electrodes inserted into the vias located at the ends of the chip. The velocity field was quantified with particle image velocimetry (PIV) using an inverted fluorescence microscope. A computer model was used to calculate the velocity vectors around a single post with voltage applied. The symmetric post shapes, such as cylinders, generate symmetric flows that do not mix beyond the inter-post spacing when a simple AC potential is applied. Figure 2.2 shows details of the fabricated and modeled test chip. Figure 2.3 (a) shows an RMS image of the particle image velocimetry experiments using the test chip. The flow is composed of four vortex structures located around each post. Figure 2.3 (b) also shows the results from the simulations of the ICEO flow in the test chip. The agreement between the experiments and the model is good in the terms of the overall flow structure. The test chip has curving sidewalls and low aspect ratio. Silicon

substrates replaced the polymer substrates in fabricating the cylindrical conductive posts.

The advantages of the use of silicon substrates over the polymer substrates are as follows:

1. The posts fabricated on the polymer substrates have curved sidewalls and low aspect ratio. The silicon substrate will enable the production of vertical sidewalls which put more pumping surface within the microfluidic channel.
2. The silicon substrates will enable the production of fluid via ports by photolithography and chemical etching.
3. Ion milling will be used to pattern the conductive metal on the ICEO devices rather than photolithography and chemical etching.

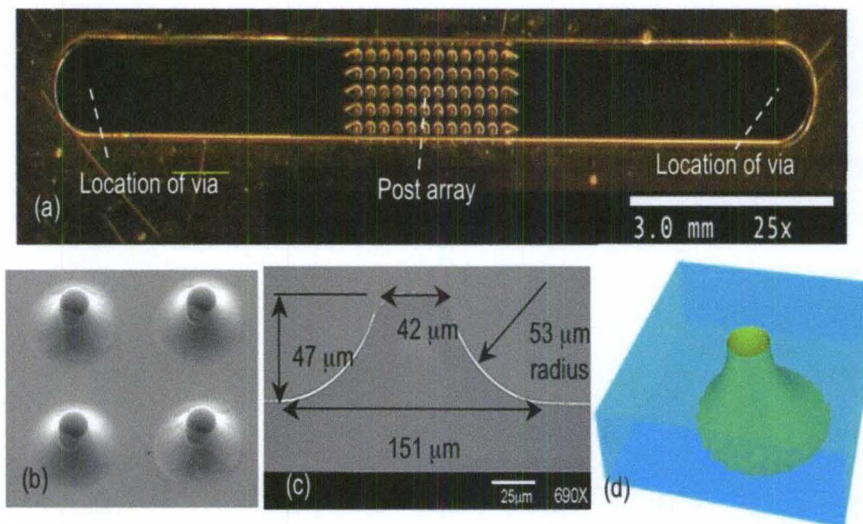


FIGURE 2.2: a) The metallized polymer test chip used to characterize ICEO flows. b) An oblique scanning electron micrograph of a volcano shaped post and (c) a micrograph of a cross section of the posts. (d) The computer model incorporates the measured shape and the observed off center alignment of the metal pad [39].

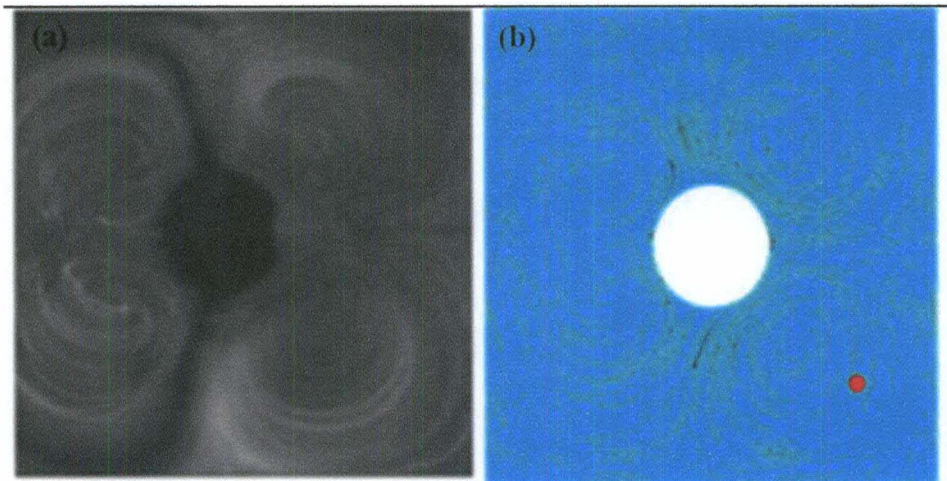


FIGURE 2.3: a) The flow of the solution around the post. b) The simulated flow of solution around the post [39].

## 1.2. Design and Fabrication

The ICEO device consists of an array of 32 cylindrical posts. The diameter of each post is  $200\ \mu\text{m}$  and the gap between the posts is  $50\ \mu\text{m}$ . The device contains 4 vias with dimensions  $1.25\ \text{cm} \times 1.25\ \text{cm}$ . The PDMS (Polydimethylsiloxane) molds design has a channel with a width  $1\ \text{cm}$ . Figure 2.4 illustrates the 1-edit design of the device. The device was fabricated on four -inch diameter,  $500\ \mu\text{m}$  thick, (100) orientation, single-side polished silicon wafers with a resistivity of  $5\text{-}20\ \text{ohm-cm}$ . Photoresist was patterned on the wafer through Mask 1 (red layer). The wafer was then etched at a depth of  $260\ \mu\text{m}$  using Deep Reactive Ion Etching (DRIE) to create the posts. The wafer was oxidized to create an insulation layer between the posts. Photoresist was patterned on the backside using Mask 2 (purple layer) to create opening windows (vias) for oxide and silicon etch. A conducting layer (titanium and gold) was deposited on the front side of the wafer to coat the vertical sidewalls of the post. Ion milling was then used to remove the entire conducting metal layer except at the vertical side walls of the posts.

**Details of the fabrication are as follows:**

1. Photoresist (Shipley 1827) was dispensed on the polished side with spread speed 500 rpm for one second rpm and spin speed 4000 rpm for 10 seconds, and then baked on the hotplate at a temperature of 115 Celsius degrees for 1 minute.
2. The wafer was then exposed for 11 seconds to Mask 1 on ABM aligner and developed in MF-319 for approximately 40 seconds (Figure 2.5a).

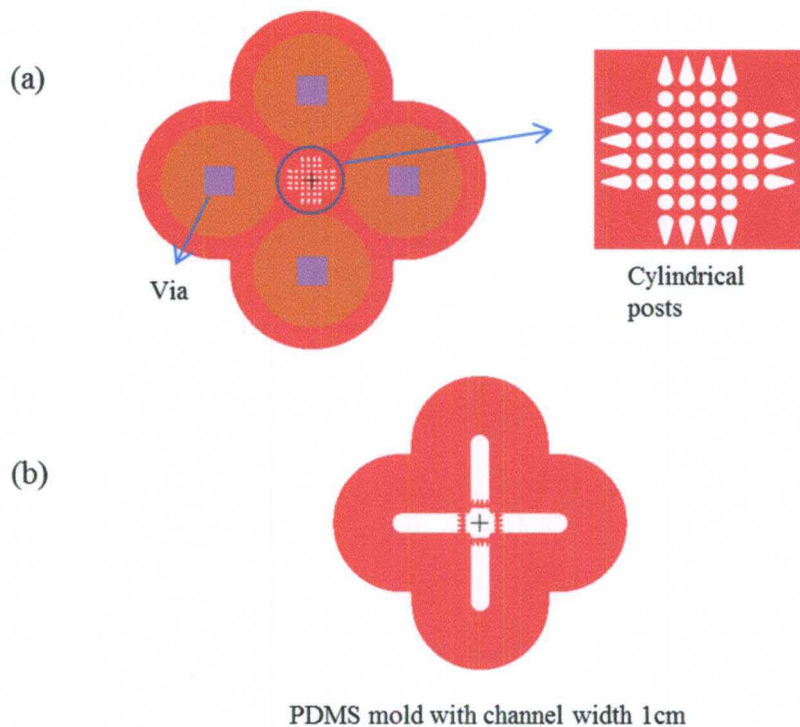


FIGURE 2.4: (a) The L-edit design of the ICEO device contains 32 cylindrical posts of diameter  $200\ \mu\text{m}$  and  $50\ \mu\text{m}$  spacing between the posts. (b) The design of the PDMS mold with channel width 1cm.

3. The “Bosch” process [40] in the DRIE machine was used to etch the channels 260 um depth through the wafer followed by an oxygen post process for 10 minutes to get rid of the “teflon” coating from the silicon etch process (Figure 2.5(b)).
4. The wafers were put in a nanostrip for 5-10 minutes at room temperature to remove any traces of resist, and then rinsed in DI water, and followed by a rinse with isopropanol and acetone.
5. The wafers were oxidized in a wet oxidation furnace for two hours at 1000 Celsius degrees. Shipley 1827 photoresist was spun on the front (patterned) side to protect it, and then it is baked for 115 Celsius degrees for one minute (Figure 2.5c).
6. Photoresist (Shipley 1827) was dispensed and spun, with the same parameters mentioned in step one, on the backside to open windows for the oxide etch. The aligner (Karl Suss Inc.) was used to align the backside of the wafers with the front side using the second Mask (Mask 2) (Figure 2.5(d)).
7. The oxide is etched in the March Etcher. The process used in the March Etcher is process 4, which contains the following recipe. CF<sub>4</sub>:H<sub>2</sub> is 40:7, Pressure is 300 m torr, power is 200 watt RF and the etch time is 20 minutes.
8. Anisotropic etching was performed using a solution of a 1450 ml TMAH of 25% concentration and 300 ml of isopropanol (IPA). A condenser with cooling water and electrical tape were used to recycle vapors. The settings were set to stir the wafers at 200 rpm and set hotplate temperature at 180 Celsius degrees, which corresponds to a probe temperature of about 65-75 Celsius degrees. The Etch rate was about 12-14 microns per hour. The junction of the beaker and condenser was surrounded by an electrical tape to

keep the solution from evaporation. The depth was measured periodically with profilometer. When the etching is done, the wafers are rinsed in DI water, and then dried (Figure 2.5 (e)).

9. The wafers were etched in the March etcher with Mask 2 side up to remove membranes and the jagged pieces around the edges.

10. The wafer were dipped in a nanostrip for 5-10 minutes, and then rinsed with DI water.

11. The wafers were oxidized to a depth of at least 650 nm by a wet oxidation furnace for two hours, which puts an insulating oxide on the pyramidal sidewalls that were exposed during the TMAH etch (Figure 2.5(f)).

12. A conducting metal was deposited on the front side of the wafer. The conditions used were sputtering titanium at 350 watts (RF power) for two minutes and gold at 120 watts (DC power) for three minutes. This created a total approximate metal thickness of 185nm (Figure 2.5(g)).

13. The top half was separated from the lower half of the wafers. The lower half was used as a mold for the PDMS lid.

14. To produce isolated conducting posts, the metalized side of the wafer was ion milled (Veeco Ion Mill, Cornell Nanofabrication Facility, Ithaca, NY) at 500 V for 4 minutes in a 100 m torr argon atmosphere. Since the ion milling rate is highly dependent on the incident angle, especially for gold films, the resulting devices had metalized vertical sidewalls and an insulating floor (Figure 2.5(h)). Figure 2.6 shows a SEM image for cylindrical posts of 200 um diameter, etched 260 um deep.

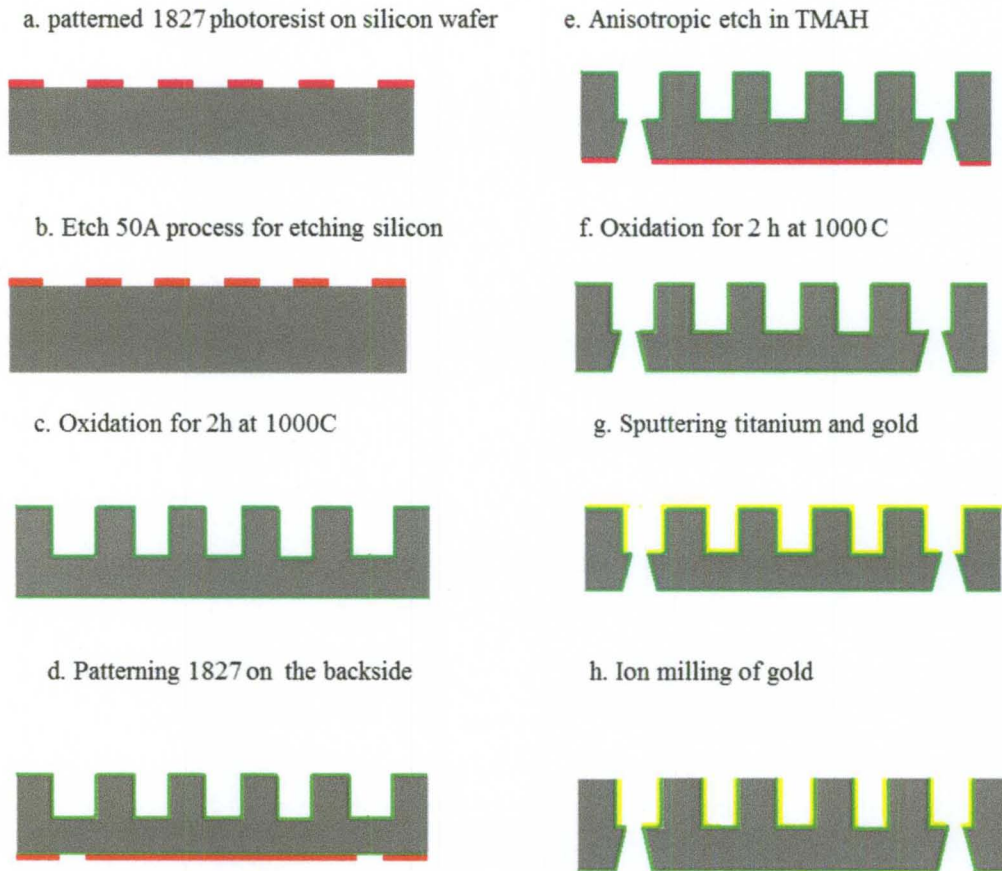


FIGURE 2.5: Fabrication process for the electrodes of the Ninja Star chip.

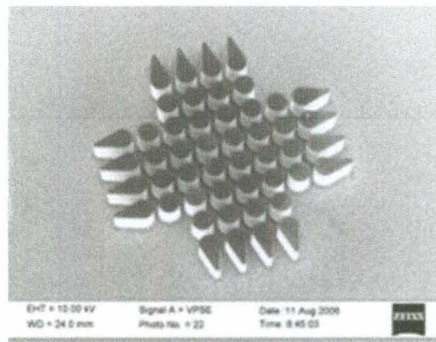


FIGURE 2.6: SEM image for the cylindrical posts of the Ninja Stars chip.



### **1.3. Fluidic and electrical connections**

After ion milling, fluid ports were attached to the top side of the devices using epoxy (3 M scotch weld DP-420) as shown in Figure 2.8(a). PDMS parts that served as both lids and the channel walls for the devices are produced by casting Sylgard 182 (Dow Corning) into the silicon molds. The PDMS is mixed in a weight ratio of 10 resin to 1 part curing agent, vacuum pumped to remove bubbles, and allowed to cure in the molds for at least three days at room temperature or one hour at 60 C. After removing from the molds, the patterned side of the PDMS is exposed to air plasma at 9 watts (RF power) and approximately 100 mtorr pressure. This treatment makes the channels hydrophilic, for easier introduction for aqueous solutions from the fluid ports. Figure 2.7 shows the process of making microfluidics devices with PDMS. Plasma-treated PDMS channels are then aligned with silicon devices by mechanical interlocking as shown in Figure 2.8 (b). The PDMS served several purposes. It confined the liquid to the area of the channel where the ICEO posts are located, enabled inverted fluorescence microscopy of the channel contents, and it provided an insulating barrier between the liquid and the other silicon channel sidewalls, which remained conducting from the non-photolithographic sputter/ion milling process. In the ninja stars chips, a high voltage square wave generator (See Appendix A for more details) was used because the electrodes are 1 cm apart. The square wave generator consists of two channels with phase difference of 180 degrees. The voltage ranges from 70 to 300 volts peak to peak and the frequency ranges from 25 to 2500 Hz. The square wave generator produces a square wave signal of voltage with ranges between 70vpp and 300vpp, and frequency ranges between 20 Hz and 2500 Hz with 50% duty cycle.

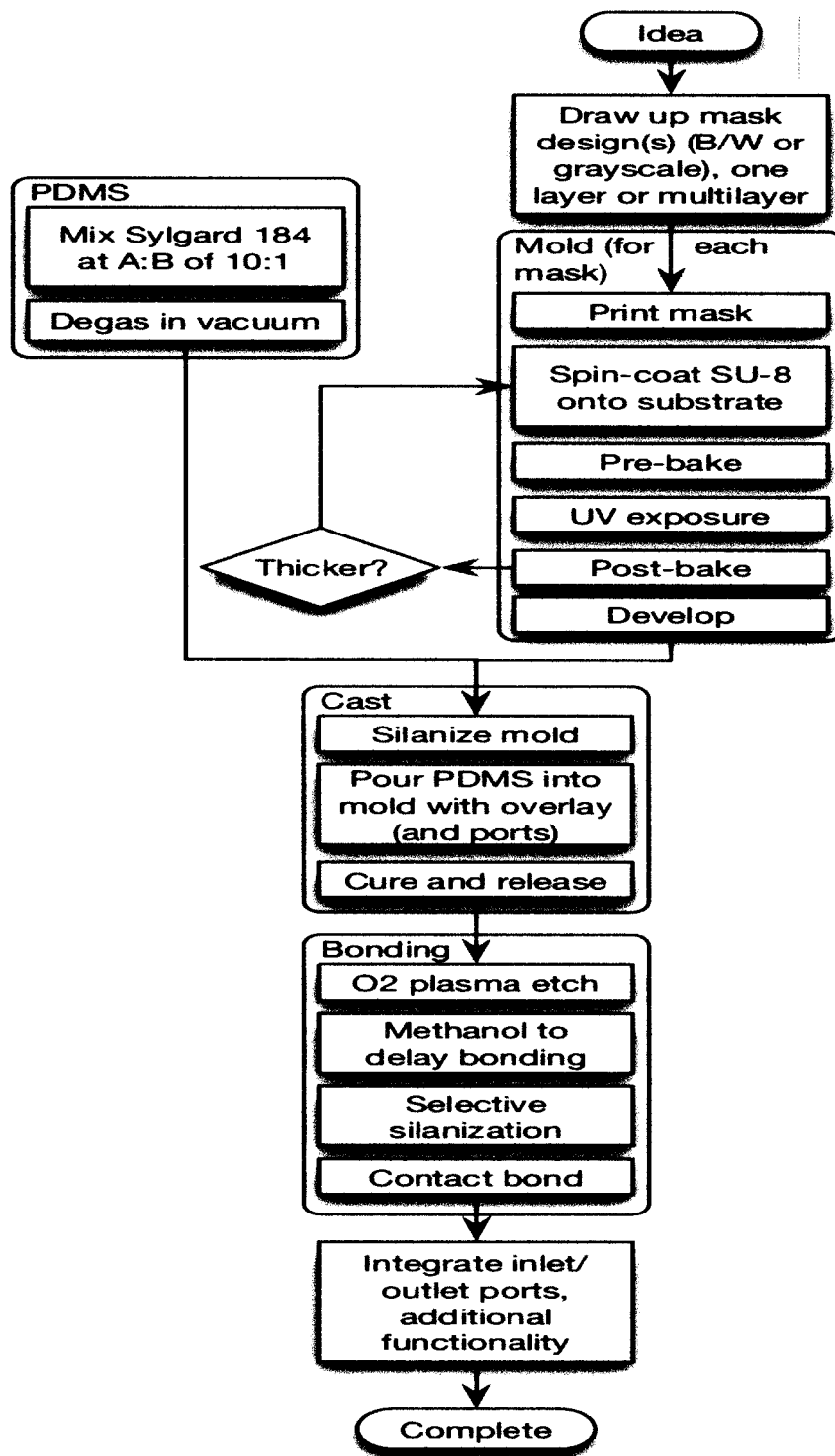


FIGURE 2.7: Process of making microfluidic devices with PDMS [41].

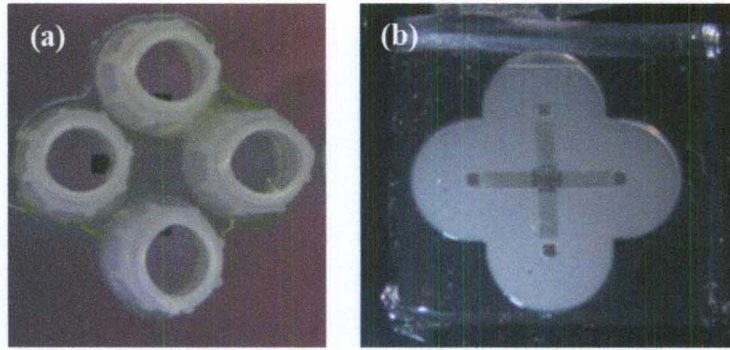


FIGURE 2.8: (a) The combination of the PDMS and the device. (b) The ports connected to the vias on the back of the chip.

The four ports of the two channel device are connected to the two channels of the high voltage power supply via two switches (Figure 2.9(a)). The switches are connected to a function generator whose frequency is 0.2 hertz. So, the switches are on together and off together every 2.5 seconds. The electric field is horizontal when the switches are off and the electric field is diagonal when they are on. The first state is when Switch 1 and Switch 2 are off and Port 3 and Port 4 are connected to the high voltage power supply as shown in Figure 2.10a and the electrical field is horizontal. The second state when Switch 1 and Switch 2 are on; Port 1 and Port 4 are connected together; Port 2 and Port 3 are connected together, the electric field is diagonal (Figure 2.9(b)).

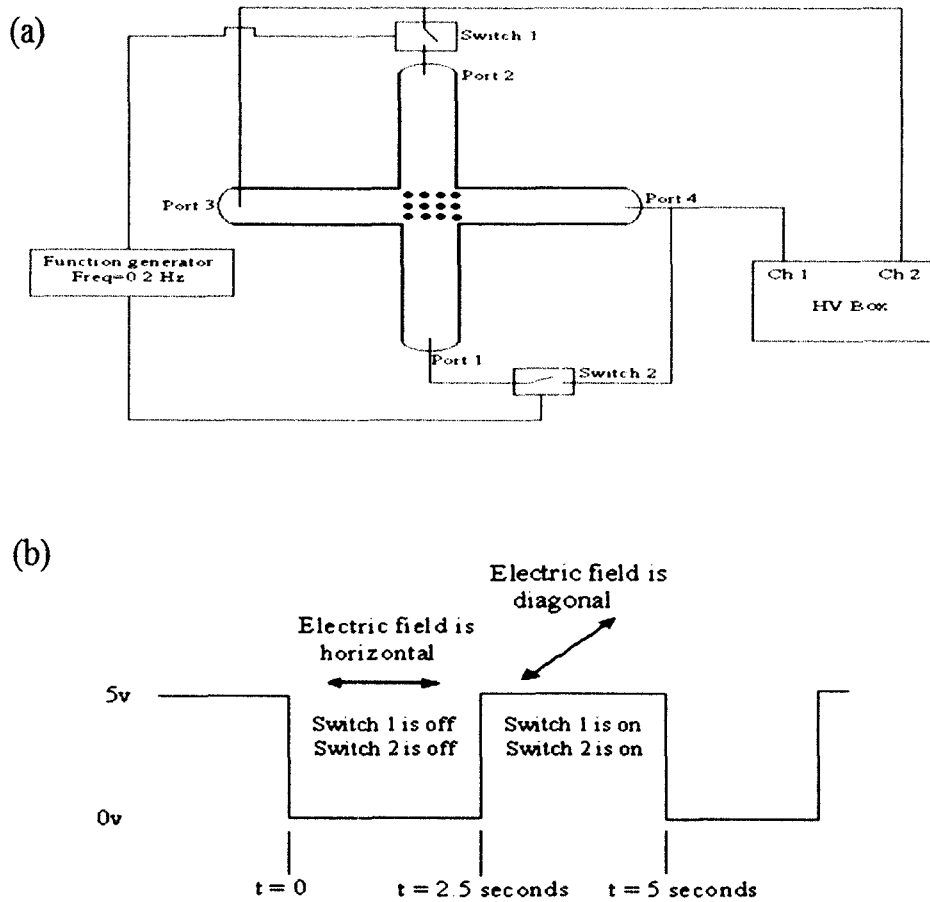


FIGURE 2.9: (a) The connection of the HV box and the function generator with two channel device (b) the electrical field directions with the operation of the switches of the function generators.

#### 1.4. Results and Discussions

The typical 70-Hz AC, 300 Vp-p electric field varies approximately every 2.5 seconds between a horizontal electric field and a diagonal electric field. When the electric field is horizontal, the motion of the particles of the fluid moves around the conductive post as shown in Figure 2.10(a), and when the field is diagonal, the motion of the particles around the post is as shown in Figure 2.10(b).

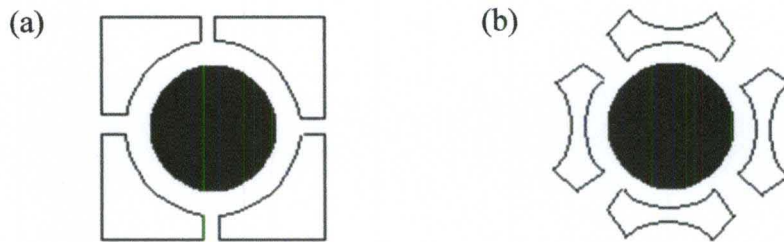


FIGURE 2.10: The direction of the particles when the electric field is (a) horizontal and (b) diagonal.

The chip was loaded via the ports with a solution of KCl with concentration typically 0.1mM and KCl solution with 200 nm fluorescent polystyrene beads. The electric field was applied to the fluid by dipping platinum wire electrodes into the fluidic ports at each end of the channel as shown Figure 2.11.

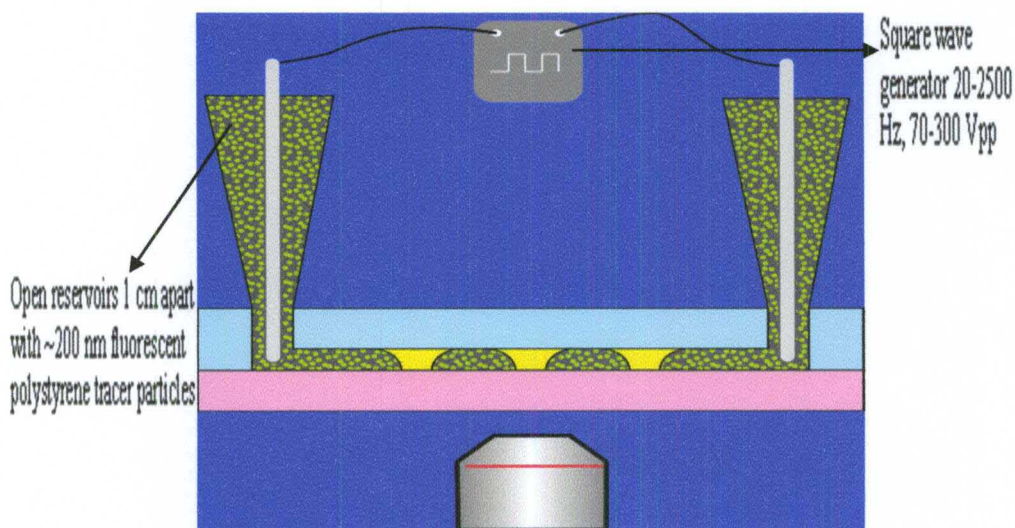


FIGURE 2.11: The experiment setup for testing the device.

The video was captured using an inverted microscope (Olympus IX71). Figure 2.12 shows selected frames for the video captured to mix two solutions together with the existence of the electric field. The change in the direction of the electric field changes the location of the circular motion of the particles around the posts. This makes the particles

in the two solutions migrate from one post to another. This helps mixing takes place between the two solutions as shown in figure 2.12.

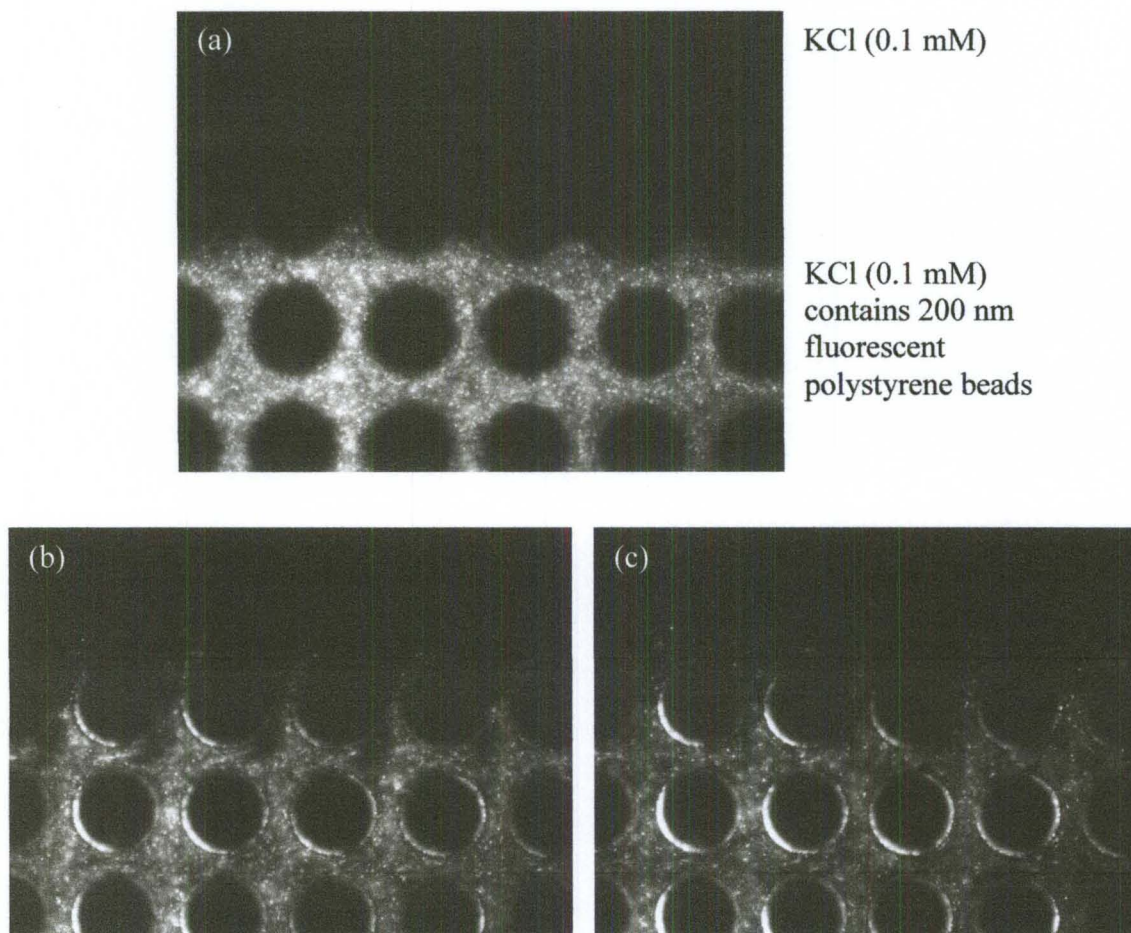


FIGURE 2.12: (a) Start frame of the video captured from the microscope for the ninja stars device after applying electric field. The first half of the frame shows the KCl solution without bead while the other half shows the KCl solution containing the 200 nm fluorescent beads. Frames in (b) and (c) show the mixing between the two solutions.

## 2. Devices with asymmetric posts and embedded electrodes (Rectangle chips)

### 2.1. Model based design

A computer model was developed by collaborators at Sandia National Laboratories to consider a wide range of designs where arrays of posts of various shapes and arrangements within microfluidic channels were used to generate the ICEO flow. Thus, a key design principle for a high performance device calls for the use of non-symmetric post shapes that generate non-symmetric flows that mix beyond the inter-post spacing. A variety of designs were considered with the model, and the best performer was identified and chosen for fabrication. The best performer was determined from the calculation of a mixing metric,

$$M = 1 - \frac{M'}{M'_o} \quad , \quad M' = \frac{\int |m - \bar{m}| dV}{V} \quad , \quad (2.1)$$

Where  $\bar{m}$  the average concentration of solute is in the liquid mixture and the integral was carried out over the volume of the mixing domain.

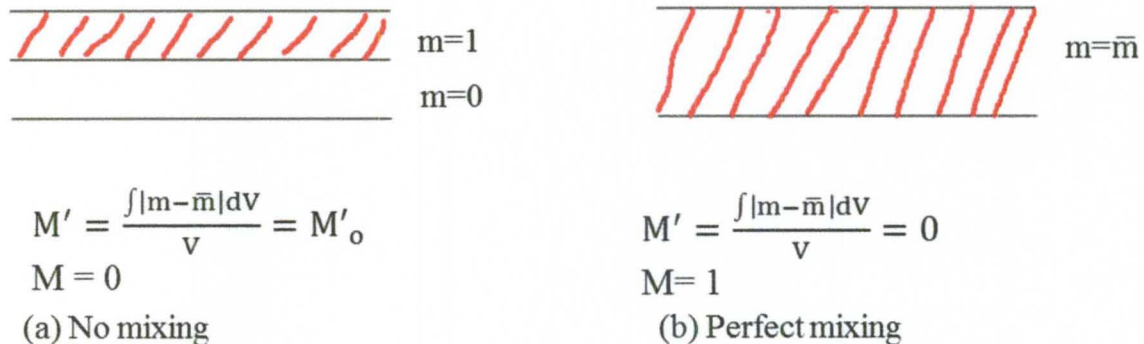


FIGURE 2.13: The metric value of mixing between two solutions inside microchannel in two cases: (a) no mixing (b) perfect mixing.

Figure 2.13 shows a schematic diagram for the mixing metric values between two solutions inside microchannel. The figure shows two cases. The first case is when no mixing between the two solutions inside the microchannel ( $M=0$ ). In the second case the mixing metric is one ( $M=1$ ) when perfect mixing is achieved between the two solutions.

Figure 2.14 shows the basic features along with results from the model for its operational characteristics. It makes use of a pair of embedded electrodes oriented lengthwise on either side of a linear array of triangular posts. The posts are assumed to be conductors. The Figure shows the process of loading the liquids into the device (Figure 2.14(a)). Loading both liquids simultaneously helps stretch the interface between the two streams, with the interface winding between the posts. At this point the liquid injection into the device was stopped in the simulation to mix the liquids in batch mode. An electric potential was applied to the electrodes (Figure 2.14(b)) creating a transverse field that generates the flow field shown (Figure 2.14(c)). The inter-triangle flow field consists of a long, slightly warped recirculation zone. Since this zone extends from a triangle base to its tip, the transport of fluid through this zone exchanges fluids between the top and bottom of the channel.



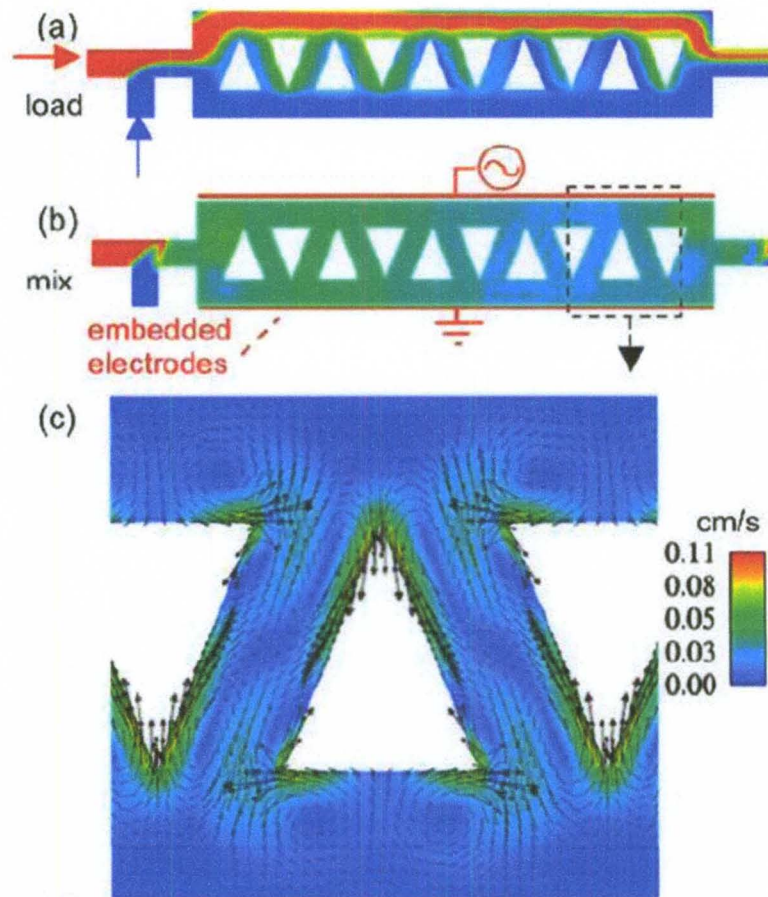
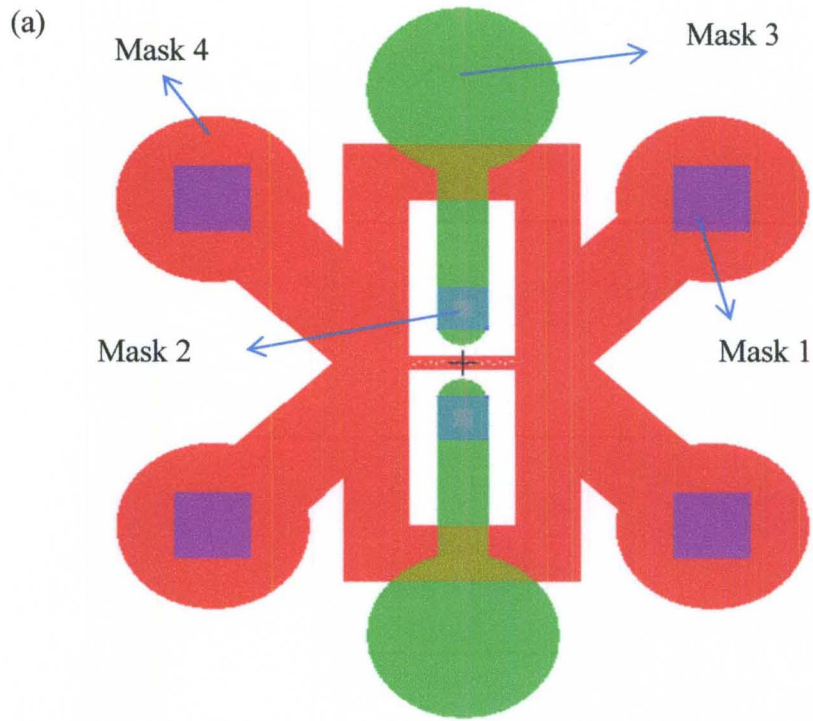


FIGURE 2.14: Numerical models of the device (a) after loading, and (b) after mixing (c) The flow field during mixing [39].

## 2.2. Device design and fabrication

The design of the device consists of four layers. The first layer (blue) represents the electrical and fluidic vias on one side of the wafer. This layer consists of four squares of dimensions (1.2 mm x 1.2 mm) and two squares of dimensions (0.8mm x 0.8mm). Layer two (purple) represents the opening windows for the oxide etch using the March etcher. The third layer (green layer) is the patterned gold on the back of the wafer connected to the electrodes on the other side through the electrical vias created using layer two. The fourth layer (red) represents the embedded electrodes and the triangular

posts inside a rectangle channel. The channel width is 200 $\mu\text{m}$  and the post dimension is 80  $\mu\text{m}$  (width) and 100  $\mu\text{m}$  (height). The PDMS mold design has channel width of 100  $\mu\text{m}$ . The L-edit design is shown in Figure 2.15. The devices were fabricated on 4-inch diameter, (100)-orientation silicon-on-insulator (SOI) substrates typically having a 100-micron thick high resistivity ( $>5000$  ohm-cm) silicon layer on the via side, a 2 micron thick buried oxide layer, and a 300 micron thick, low resistivity ( $<0.02$  ohm-cm) highly doped silicon device side. The thick device layer is different from most off-the-shelf SOI substrates, which typically have a thick handle layer and thinner device layer. The wafers were oxidized for two hours to grow 650 nm of oxide on the wafer. Fluid and electrical via holes were produced on the low conductivity side (thinner side). The photoresist was patterned using Mask 1 (blue). Buffered oxide etch (BOE) is used to etch the silicon dioxide followed by anisotropic silicon etch using tetramethylammonium hydroxide (TMAH). The etch was stopped at the buried oxide in the SOI wafer. To insulate the sidewalls of the etch pits from the contact electrodes, a 650 nm thick oxide layer was applied by thermal oxidation. For electrical contacts, photoresist was patterned using Mask 2 (purple). This Mask created open windows to etch silicon dioxide using the March etcher. A metal layer (chromium and gold) is patterned on the etched side, using Mask 3 (green layer), to create pads and traces where the electrical wires were connected. This metal layer touched the highly doped side via the etched open windows. Mask 4 (red layer) was used to pattern the triangular posts inside the rectangular channel on the highly doped side. The silicon was etched deep down to the buried oxide layer and fluid vias. Titanium and gold are sputtered to coat the electrodes. Ion milling was used to remove the metal from the top of the posts and the channel floor.



(b)



(c)

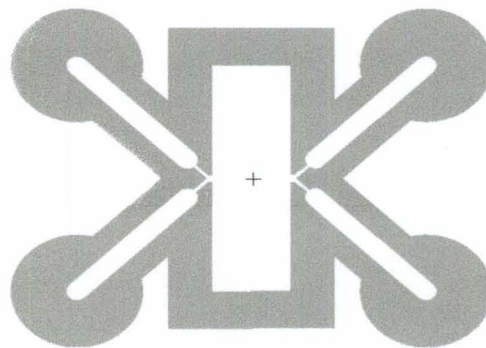


FIGURE 2.15: The 1-edit design of (a) the whole chip (b) the posts inside the channel (c) the PDMS molds layout.

**Details of the fabrication process are as follows:**

1. The wafers were oxidized for two hours in a 1000 C furnace to grow approximately 650 nm of oxide (Figure 2.16 (b)).
2. HMDS primer and Shipley 1827 photoresist were spun on the handle side of the SOI wafer to protect it, and on the device side to pattern the wafer. Square fluid and electrical ports were aligned with the flat side of the wafer. After patterning and development, the wafer was hard baked at 115 Celsius degrees for three minutes (Figure 2.16 (c)).
3. The wafers were etched in Buffered Oxide Etch (BOE) in a beaker for eleven minutes to remove the oxide from the squares. The patterned side was faced up so that the bubbles do not block BOE from touching the wafer. Air bubbles got trapped on the underside of the wafer (Figure 2.16 (d)).
4. The wafers were put in a 1450 ml TMAH solution of 25% concentration and 300 ml of isopropanol (IPA) to etch the silicon. The etching stopped at the buried oxide in the SOI wafers (Figure 2.16 (e)).
5. The thick buried oxide was etched using March Etcher on TMAH-etched side. The oxide on the back side may be completely removed. BOE was not used because it may undercut the silicon and make electrical contact difficult (Figure 2.16 (f)).
6. The TMAH-etched sidewalls were insulated with a 500 nm insulating oxide layer by putting the wafers inside the oxide furnace for one hour at 1000 C in an oxygen atmosphere (Figure 2.16 (g)).
7. Mask 2 was used to open windows on the etched side for the oxide etch using the March Etcher with the same recipe used previously with the Ninja Star chip.

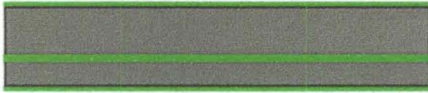
8. Using the Technics sputtering machine, a 50 nm layer of chromium and 200 nm layer of gold were deposited on the etched back side for the electrode layer (Figure 2.16(h)).
9. Shipley 1827 was patterned on the metal side using Mask 3. The wafers were placed into gold etchant (potassium iodide) solution for 3-5 minutes to remove unprotected gold and they are rinsed in water and placed into chromium etch for 3-5 minutes to remove Cr from the unprotected areas.
10. A 50 nm layer of chromium was deposited on the front side of the wafer to improve the adhesion to the oxide, followed by HMDS and Shipley 1827 photoresist. Channels were aligned and patterned in the photoresist, and wafers are temporarily bonded to a silicon wafer for DRIE etching down to the oxide layer and fluidic vias (Figure 2.16 (i)).
11. After etching, the chromium and photoresist were removed. An insulating oxide layer was not needed because the channel floor, made from the buried SOI oxide, serves to isolate the individual ICEO posts.
12. Titanium and gold were sputtered and ion milling was carried out as described above to put a conducting layer on the sidewalls of the ICEO posts (Figure 2.16 (j)).

Figure 2.17 shows a SEM image for the triangular posts and the channel floor. The microfabricated device has 18 mixing triangles. The vertical sidewalls of the triangles and electrodes were coated with a 200 nm thick conducting gold layer, while the channel floor, ceiling and the inlet/exit channels were insulating. The channel width is 200 microns and its depth is 300 microns.

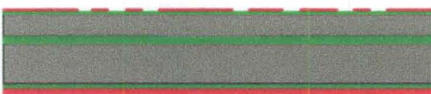
(a) SOI wafers



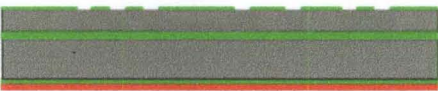
(b) Oxidized SOI wafers



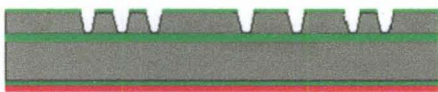
(c) pattern photoresist



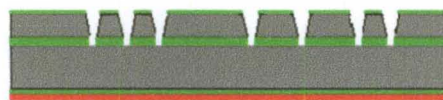
(d) Removing photoresist



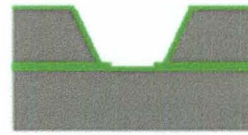
(e) Anisotropic etching through open squares



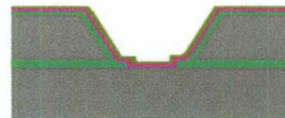
(f) Etching oxide from the holes



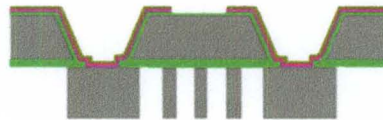
(g) Oxidization to insulate the walls



(h) Sputtering of chromium and gold



(i) Silicon isotropic etch using DRIE



(j) Sputtering and ion milling for the top of the posts

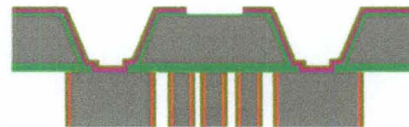


FIGURE 2.16: The fabrication process of devices with integrated electrodes and metalized post.

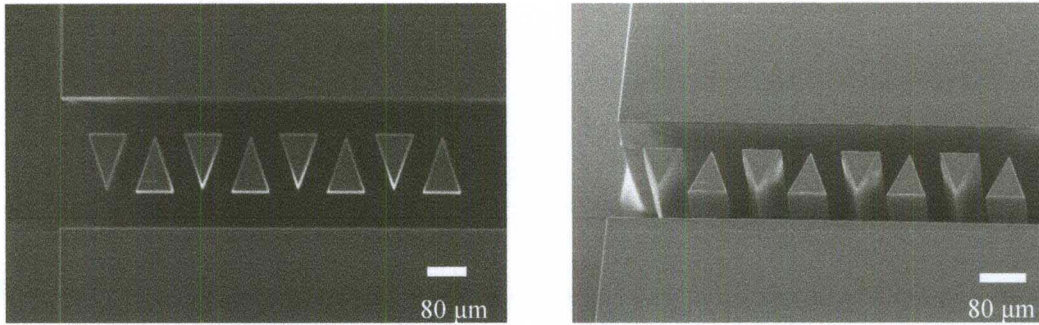


FIGURE 2.17: SEM image shows the triangular posts and the electrodes of the rectangular chip.

### 2.3. Fluidic and electrical connections

Fluidic fittings were bonded to the top-side of the devices over the fluid via ports, and wires were soldered to the bond pads for electrical contact as shown in Figure 2.18(a-d). PDMS lids (Figure 2.18(e)) were fabricated as described previously, this time on a separate mold wafer etched to the same depth as the SOI devices. The chip was tested by applying five volts on the wires and then measuring the voltage across the electrode is measured. The conductive epoxy was used on the gold layer of wafer for one hour in the oven and the voltage across the electrodes is measured and it is close to 5V. The voltage across the electrodes in a bad chip is less than 2.5 volts. The chip was capped with the PDMS lid as mentioned above. A 300 volt, 30-2500 KHz square wave generator was previously developed to run the ICEO devices with wire electrodes immersed in the channels. In contrast, the voltage source used in the rectangle chip was simply a function generator. The function generator was able to drive flows in the rectangle chip because the electrodes are 200 micrometers apart, so its maximum output of 12 volts generates more than enough electric field to cause mixing. Switching the directions of the electric field in the presence of two electrodes was impossible. This made the circuit simpler than

the complex ninja star circuit. The experiment setup and the device connection to the function generator are shown in Figure 2.19.

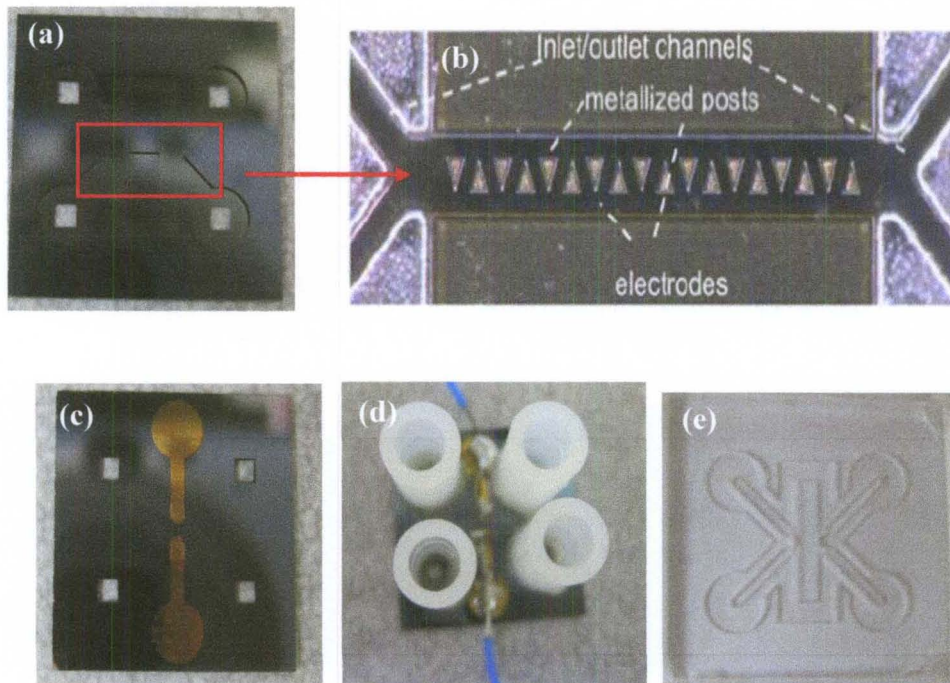


FIGURE 2.18: (a) The top side of the chip (b) micrograph of the fabricated device with 18 triangles [39] (c) backside of the chip with gold connections to the embedded electrodes (d) the ports and the wires glued on the backside of the chip (e) PDMS lid.

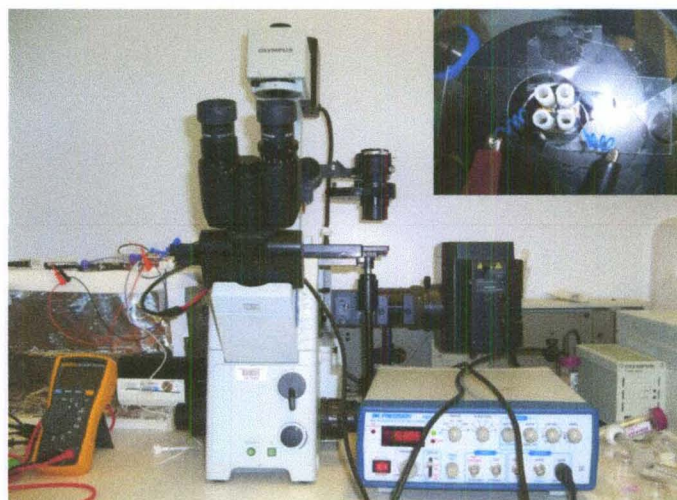


FIGURE 2.19: Experiment setup used and the picture on the top right corner shows the device connected to the function generator.



## 2.4. Results and discussions

Figure 2.20 shows the mixing between two solutions inside microchannels of the rectangular chip using a square wave signal of amplitude 6Vp-p and frequency of 100 Hertz (one side of the channel is grounded, while the other side went from +3 to -3 V at 100Hz for a DC component of zero). With electrodes directly in the channel, any DC voltage above the electrolysis threshold for water, or even AC voltages that are too large will form bubbles within the channel which prevent the red and green dyes to flow. The bead solutions contained 20 microliters of red and green carboxyl beads of diameter 0.02 microns per 1 ml 0.1 mM KCl. The next step was to wait for the two dyes to stop flowing by attaining equal levels in their reservoirs. When the balance between the red and the green dyes was achieved as shown in Figure 2.20 (a), the voltage was applied. Figure 2.20 (b) shows an image for the calculated results after loading the two solutions. Figure 2.20(c) shows an RMS image of the bead distribution. A number of distinctive shapes of species interfaces are shared by the experimental results and model (Figure 2.20 (d)). Near the top of the posts, the interface has ‘wave’, ‘circular’ and ‘elongated’ shapes that repeat itself with a frequency matching that of the post pattern. The similarity between the model and the experiment proved that the model predicts the fluid motion and the mixing process correctly. Figure 2.21 shows another video captured at 8 Vp-p and frequency 100 Hertz. The video shows that mixing is happening beyond the inter-post spacing.

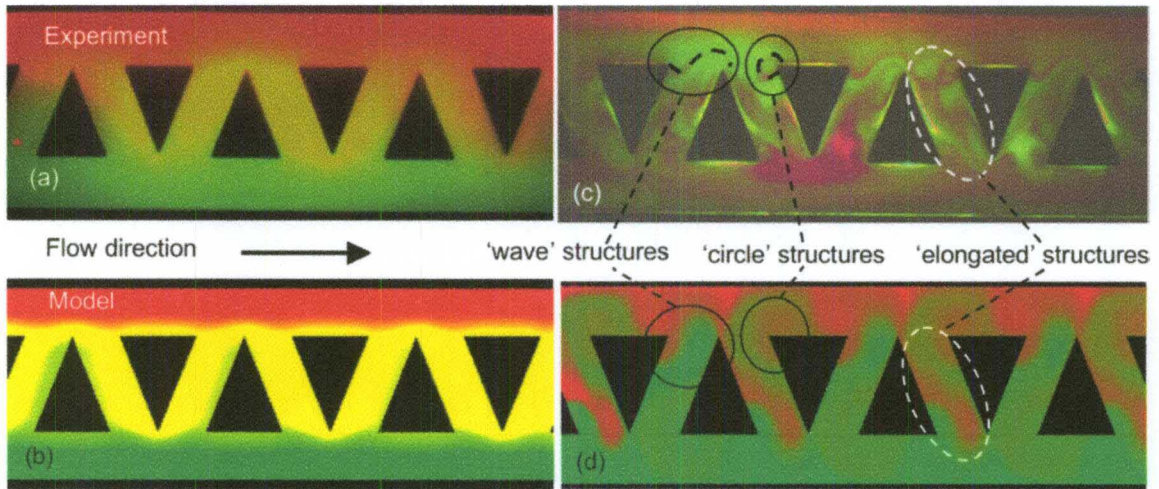


FIGURE 2.20: Experimental (a,c) and modeling (b,d) results for the distribution of red and green fluorescent beads after loading (a,b) during mixing (c,d) [39].

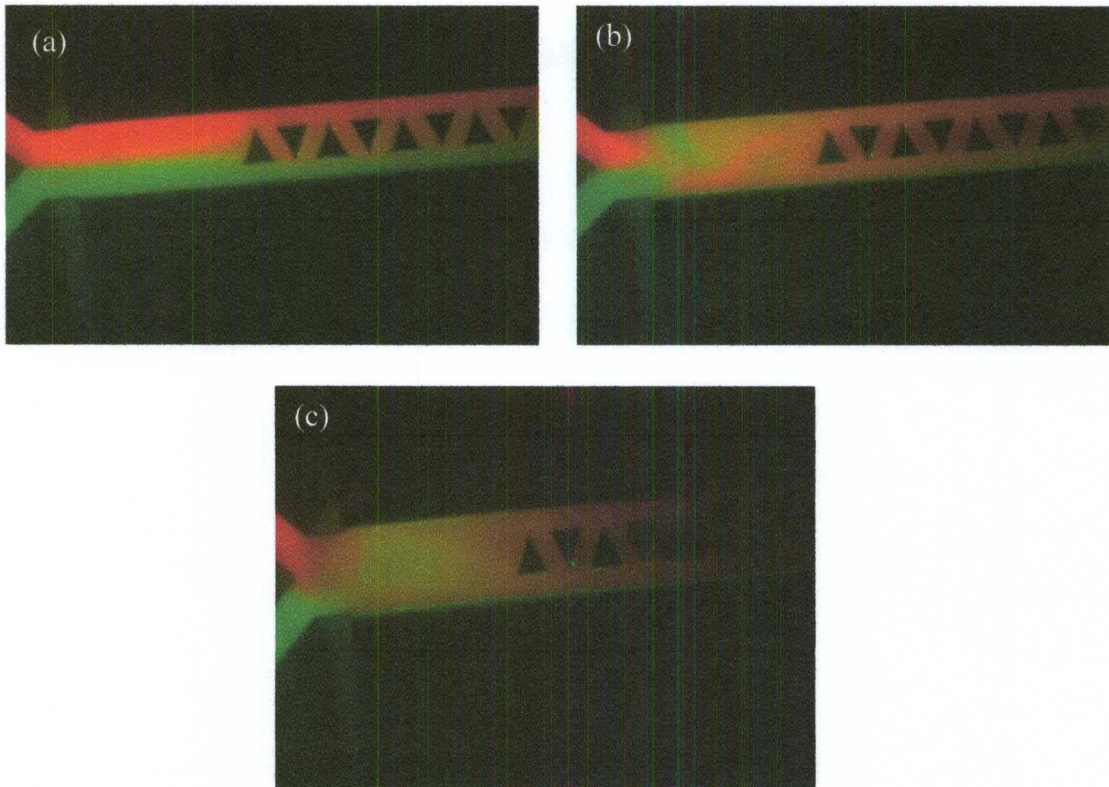


FIGURE 2.21: (a) Balance between two dyes achieved. Flow is stopped. (b) When the power is on (mixing starts). (c) Full mixing is achieved.

Figure 2.22 shows images of video taken for the device at voltage 10Vpp and frequency 37 Hz, where there is continuous flow of 2  $\mu\text{L}/\text{min}$  driven from a syringe pump. The images show the steady state dye distribution of the dyes before and after applying electric field. The video was taken in black and white to facilitate the evaluation of the mixing metric [39]. The fluids were clear 0.1 mM KCl solution loaded in the upper channel from the left side and 0.1 mM KCl solution that had also dextrans dye loaded in the bottom channel from the left side. Both experimental (Figure 2.22(a,c)) and modeling results (Figure 2.22 (b,d)) are shown. The mixing metric is measured over one third of the device on the inlet side. The metric is zero before applying the voltage. After turning on the voltage at  $t=0$ , the metric begins to increase until it reached the value of 0.63 at  $t= 6.4\text{s}$  as shown in Figure 2.22. The metric approaches a value of one (perfect mixing) near the outlet of the device. Figure 2.23 also shows that the mixing metric of the model and experiments behave similarly, however the model over predicts the mixing rate speed by a factor of four. This is linked to over prediction of the flow velocities by the ICEO theory, which does not account for surface roughness, surface conduction within the double layer and Faradic reactions at the posts. The choice of length scale is also critical in determining the mixing speed. The model does predict the appearance of flow features well [39].

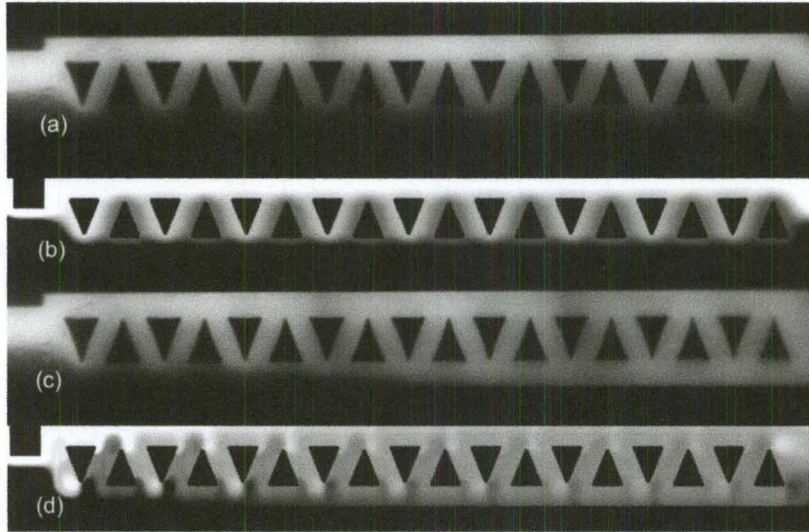


FIGURE 2.22: Comparison of experimental (a,c) and calculated (b,d) results for the solute distribution during steady flow of dyed and un-dyed solutions ( $2 \mu\text{l}/\text{min}$  combined flow rate) without power (a,b) and with power (c,d). Flow is from left to right [39].

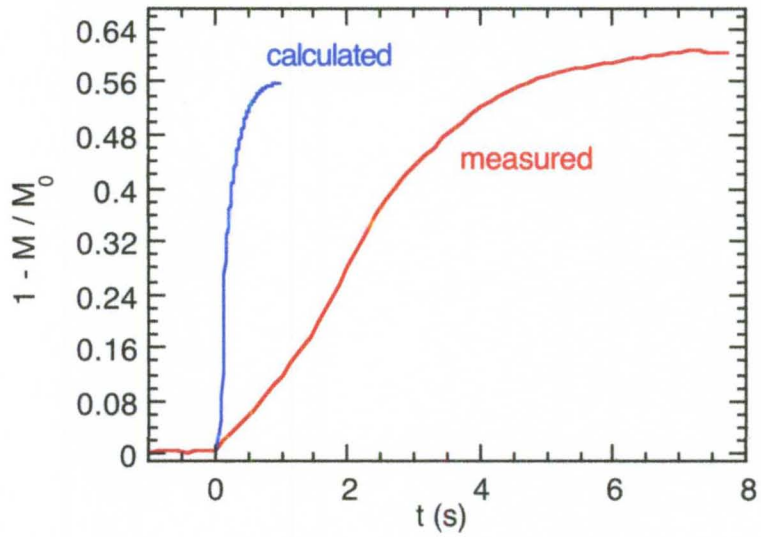


FIGURE 2.23: Measured and calculated results for the mixing metric for the mixing device [39].

#### **D. Summary**

A microfluidic device is designed and fabricated to do sample preparation for biological agent detection. The device carries out the mixing process of a biological sample with reagents, one of the most time consuming steps in the detection process. It is based on an electrokinetic phenomenon, called induced charge electroosmosis, to create micro-vortices within an otherwise stationary liquid so that the mixing process occurs within a fixed volume of liquid. Thus, it does not suffer from sample dilution and preserves detection sensitivity. A numerical model was used to design several different devices for microfluidic mixing. Out of these, the triangular-post design was identified as a good performer and constructed using microfabrication techniques. The key to the integrated electrode fabrication process was ion milling, which made it possible to fabricate isolated posts with vertical metal-coated walls. The fabrication may also be carried out on plastic substrates, opening the door to a non-lithographic high-volume production process in which ICEO devices are molded, metallized over their entire surface, then ion milled and capped with molded polymer lids. Experiments were carried out using the integrated-electrode device to mix aqueous liquids. Rapid mixing was observed and quantified through video microscopy.

## CHAPTER III

### FAST THREE DIMENSIONAL AC ELECTRO-OSMOTIC PUMPS WITH NON-PHOTOLITHOGRAPHIC ELECTRODE PATTERNING

Three dimensional (3D) stepped electrodes dramatically improve the flow rate and frequency range of ac electro-osmotic pumps, compared to planar electrodes. However, the fabrication of 3D stepped electrodes for ac electro-osmotic (ACEO) pumps usually involves several processing steps. This chapter demonstrates results from ACEO pumps produced by a faster and less expensive method to fabricate the 3D electrodes—extending the previous work to disposable devices. The method is based on shadowed evaporation of metal on an insulating substrate that can be injection molded. Flow velocities through the 3D ACEO pump are similar to those seen in the previous work.

#### **A. Introduction**

The miniaturization of fluidic systems requires new techniques for pumping fluids. Pressure driven flow is acceptable for many applications [42] but causes sample dispersion and requires bulky equipment. Electro-osmosis (EO) is a pumping technique which has been explored to replace the traditional pressure driven flows. Electro-osmotic pumps (EOPs) have many outstanding features: 1) Capability of generating constant and pulse free flows. 2) Controlling the magnitude and the direction of the flow. 3) Integration with Lab-on-chip (LOC) devices. 4) No moving parts. EOPs have been used in several applications including high performance liquid chromatography (HPLC)

separations ( [43], [44]), microelectronic equipment cooling [45] and drug delivery systems [46]. The majority of EOPs are operated under a direct current (DC) voltage.

In DC EO an electric field is applied across the channel of the microfluidic device using DC voltage. Direct current causes unwanted side effects, such as bubble production due to faradic reactions, consumption of metal electrodes through electrolysis, and the need for high voltage (>10 V) which can be an obstacle in the miniaturization of the device and electronics. To avoid the problems and drawbacks of using DCEOP, ACEO pumps are developed. Planar ACEO pumps ( [47], [48]) have been introduced to obtain fluid flow with a speed of 0.1 mm/sec in dilute electrolytes with few volts, but reversal of the flow at higher frequencies. A dramatic improvement of the fluid flow velocity (1mm/sec) in the ACEO pumps is predicted and noticed by using 3D stepped electrodes ( [49] , [29] and [50]).

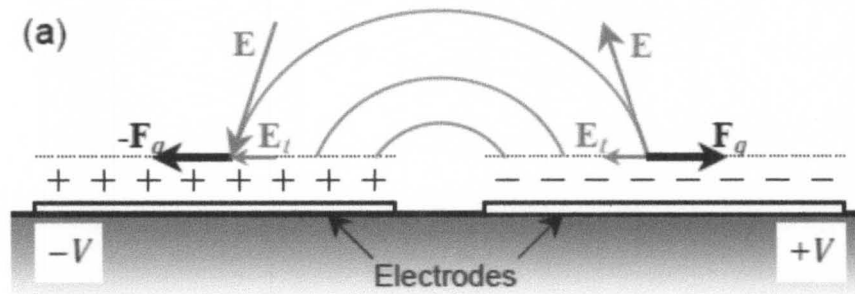
Even with the improved 3D ACEO pumps, there is still a need for a cheaper and simpler method to fabricate the 3D stepped metal electrode arrays that does not involve multiple photolithography steps. In this chapter, a new fabrication technique eliminates the need for microlithographic patterning of each individual device. The new method depends on the shadowing effect caused by the directionality of thin metal film evaporation. This dissertation discusses how to produce an insulating stepped substrate (here from SU-8 negative photoresist but a similar structure could be injection molded) for shadowed metal deposition; the only metal patterning required is a large-scale (1cm) stencil. Similar techniques have previously produced nanoscale interdigitated electrodes [11].

## B. Background on ACEO

Electroosmosis is a common technique for pumping fluids in micro-channels. If a surface has electric charges, a double layer of counter ions (Stern layer and diffuse layer) will form at the surface (see Appendix B). When a tangential electric field is applied to the surface, a Coulombic force is exerted on the mobile ions in the double layer. This causes the charges in the diffuse layer to move and pull the bulk fluid along which generates a flow. The magnitude of the velocity of the flow in a DC electric field is given by

$$u_x = \frac{E_t \sigma_q}{\kappa \eta} , \quad (3.1)$$

Where  $E_t$  is the tangential electric field,  $\sigma_q$  is the charge density in the double layer,  $\kappa$  is the reciprocal of the Debye length and  $\eta$  is the viscosity of the fluid. The proof of this formula is shown in Appendix B. If a uniform AC electric field is used, the fluid will move in an oscillatory motion with no displacement.





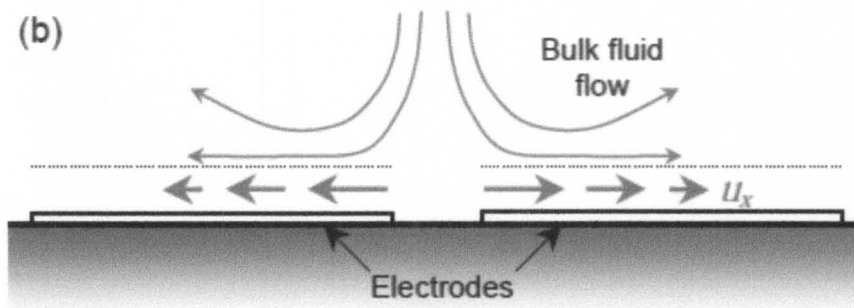


FIGURE 3.1: (a) Schematic diagram shows the mechanism of the AC electroosmosis on planar symmetric electrodes. (b) The mobile charges in the double layer move with velocity  $u_x$ , resulting in motion in the bulk fluid [51].

Ramos et al. [47] proposed the first microfluidic pump based on a nonlinear electro-osmotic flow, which is commonly known as “ac electro-osmosis” (ACEO). The device used symmetric planar electrodes. Figure 3.1 shows the schematic of the ACEO mechanism on symmetric planar electrodes. When AC voltage is applied to the electrodes, the double layer experiences force  $F_q$  due to the tangential electric field ( $E_t$ ), resulting in the fluid flow. The change in the polarity of the AC voltage does not affect the direction of the force, as the direction of the tangential  $E_t$  and the sign of the charges in the double layer change.

In the previous chapter, the ICEO phenomenon was discussed. The primary difference between ICEO and ACEO is the location of the double layers that serve as the origin for the flow. In AC electroosmosis the double layers on the electrodes provide the origin and in ICEO, the origin is provided by electrical conductors that may or may not be energized.

Brown et al. [48] proposed asymmetric interdigitated microelectrode arrays which are different in width and gap spacings. The surface slip velocity of ions on the wider electrode will be more than that on the narrower one; this will achieve net pumping in one direction. The fluid is observed to flow from the small electrode across the narrow gap, toward the wide electrode as illustrated in Figure 3.2 (a).

Bazant and Ben [49] simulated a dramatic improvement of the fluid flow velocity in ACEO pumps by an arrangement of three dimensional (3D) electrodes that they described as a “fluid conveyor belt”. Figure 3.2 (b) shows how these step electrodes are expected to increase the flow velocity by aligning the flow direction of the pair of counter-rotating vortices that are created at each electrode. Thorsen et al. [50] then demonstrated experimentally a dramatic improvement compared to planar ACEO pumps using electroplated gold electrodes.

Recently, Huang et al. [29] introduced an ultrafast ACEO pump to achieve higher velocities ( $>1$  mm/ s) and much larger pressure ( $>1\%$  atm). They eliminated the costly electroplating process by using three layers of photolithography for etching, metal deposition, and lift-off. Currently, the above ACEO pumps do not work well at physiological salt concentrations for reasons suggested in [52] and explored further in [53], but such devices can pump a dilute electrolyte (for example, de-ionized water) to push on biological solutions [29].

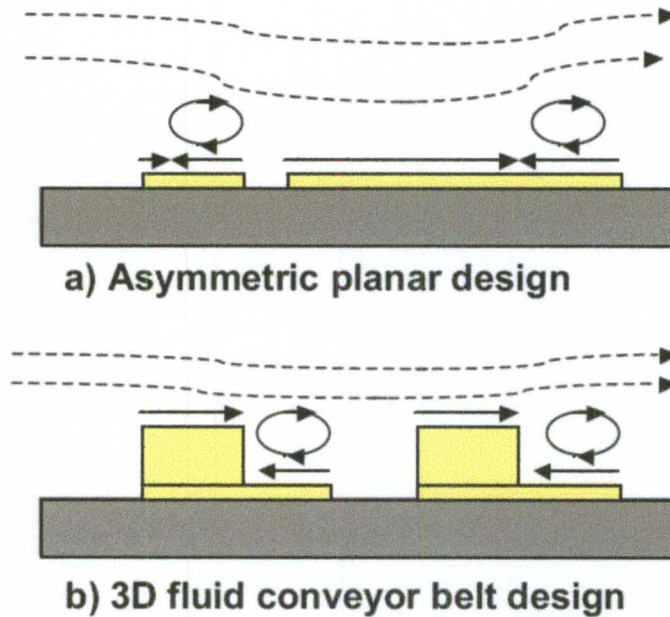


FIGURE 3.2: Schematic of the surface slip velocity (solid line) and resulting pumping streamlines (dashed lines) of (a) asymmetric planar electrodes and (b) optimal 3D electrodes (the fluid conveyor belt proposed in [49]).

### C. Design of the 3D stepped electrodes

The device shown in Figure 3.2(b) will work with solid metal electrodes, or with a thin metal film covering the surface of a three-dimensional insulating structure. The vertical metalized parts of the structure do not contribute significantly to pumping. A shadow evaporation technique can coat the working parts of the structure with metal. However, the coating must not electrically connect the left and right structure shown in Figure 3.2(b) because it would cause the interdigitated electrodes to be shorted out. Careful design of the three dimensional pattern can produce a shadow that interrupts the metal film between adjacent structures.

A two-height insulating substrate is needed because, as shown in Figure 3.3, a one layered electrode does not sufficiently interrupt the conducting metal path at the tip of the adjacent electrode. The first layer will provide the electrode steps and a taller feature at

the end of each electrode will create a shadow that interrupts the conducting metal path between adjacent electrodes. Figure 3.4 shows the L-edit design of the two layered stepped electrodes with the dimensions. Figure 3.5 illustrates this structure and the resulting shadows.

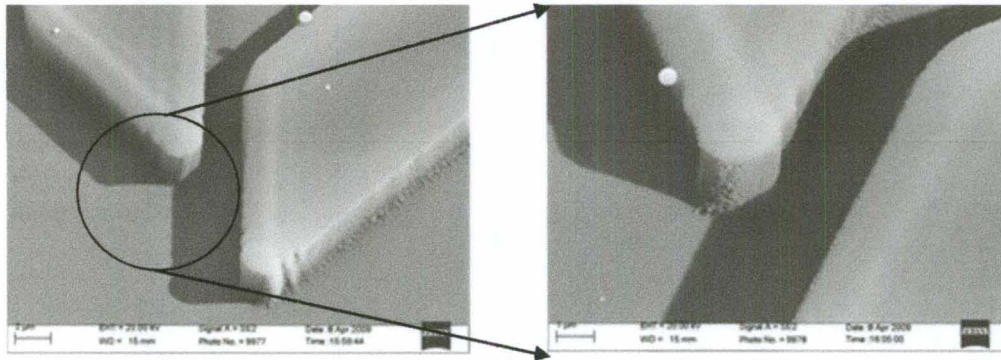


FIGURE 3.3: An SEM image of one layered electrode. The shadow coming from one electrode is not reliably interrupting the metal path at the tip of the adjacent electrode.

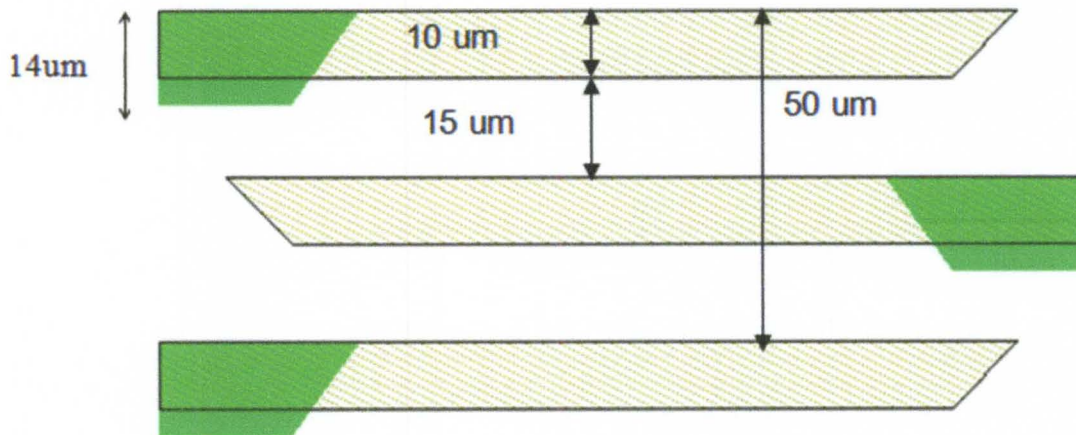


FIGURE 3.4: The L-edit design of the two layered stepped electrodes. The transparent layer is the electrode step and the green layer is the tall layer that creates the shadow that interrupts the conducting metal path between adjacent electrodes.

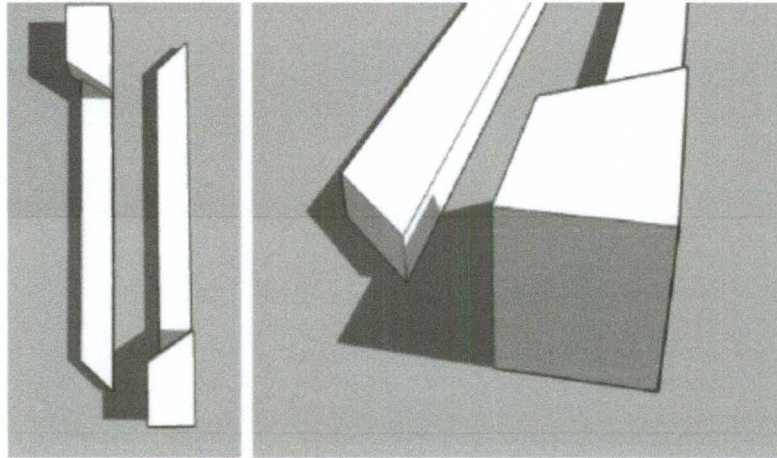


FIGURE 3.5: Illustration of shadow evaporation on a two-layer stepped electrode. (a) Top view. (b) Detail view. The barrier at the end of the electrode creates a shadow that breaks the connection between adjacent electrodes

#### **D. Device Fabrication**

SU-8, an epoxy-based negative photoresist (Microchem, Inc.), has been used to produce the 3D two layered structure in this work. While SU-8 is a good material for prototyping, these structures have no overhangs and could be replicated by casting or injection molding rather than photolithography. The fabrication process is illustrated in Figure 3.5.

**Details of the fabrication steps are as follows.**

1. Fabrication starts with thermal deposition of a 300–400 nm  $\text{SiO}_2$  layer on a silicon wafer to create an insulating floor for the pump channel.
2. To improve the adhesion of the SU-8 films, the oxidized wafers were cleaned using acetone and isopropyl alcohol, and then dehydration baked on a hot plate at 200 °C for at least 20 minutes.
3. A thin layer of SU-8(5) was used to produce the 5  $\mu\text{m}$  thick electrode layer. SU-8 was spread at 500 rpm for 2 seconds, and then spun at 3000 rpm for 10 seconds. The coated

wafer was soft baked on a hot plate for two minutes at 75 °C followed by five minutes at 105 °C (Figure 3.6(a)).

4. The first layer (electrode pattern) was then exposed to ultraviolet (UV) in a photoaligner (Karl Suss). Cross-linked features appear after a post exposure bake (PEB) for one minute at 75 °C and two minutes at 105 °C; this PEB time can be increased for extra one or two minutes to increase adhesion if needed (Figure 3.6(b)).

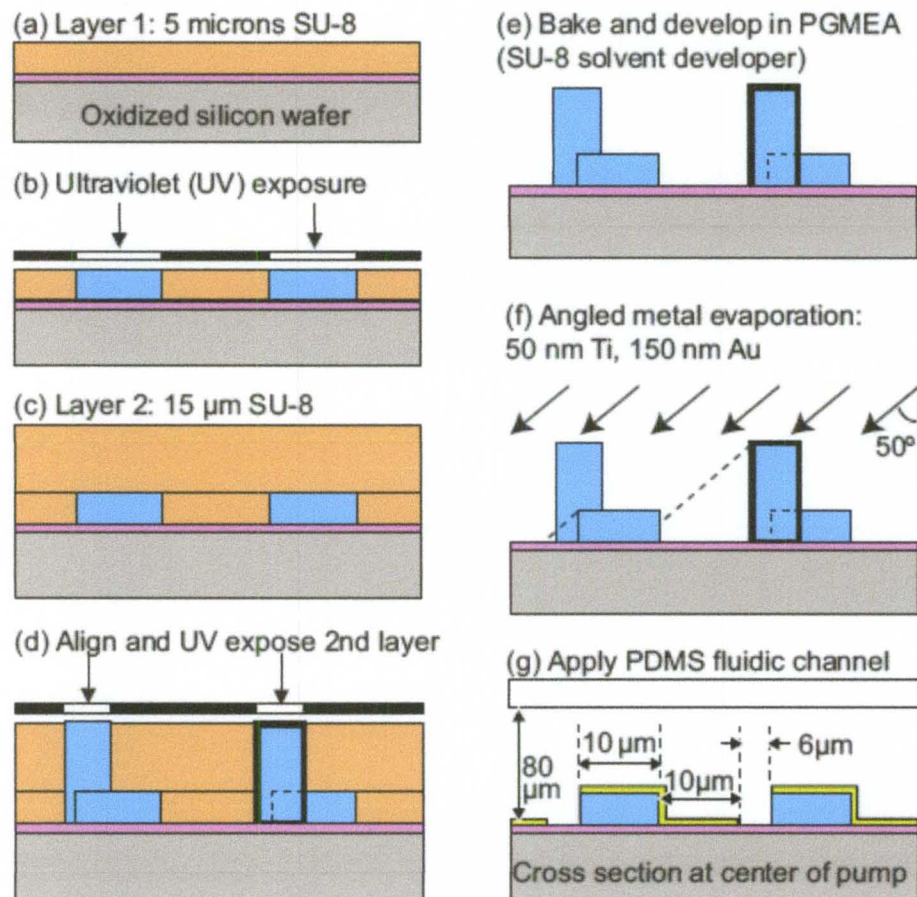


FIGURE 3.6: Fabrication process for the three dimensional electrode pump.

5. These steps were repeated again with different parameters to obtain a 15  $\mu\text{m}$  second layer. The spin speed was slower (1375 rpm) and the soft bake was longer (four minutes at 75  $^{\circ}\text{C}$  and seven minutes at 105  $^{\circ}\text{C}$ ) (Figure 3.6(c)).
6. Mask 2 (with the shadowing features) was aligned and the UV exposure in the system was 20 s instead of 16 s for the electrode layer. The PEB was one minute at 75  $^{\circ}\text{C}$  and three minutes at 105  $^{\circ}\text{C}$  (Figure 3.6(d)).
7. Both layers of SU-8 were then developed in propylene glycol methyl ether acetate for four minutes with gentle agitation, followed by rinsing in isopropanol and drying in nitrogen (Figure 3.6(e)).

To separate the interdigitated electrodes at the ends of the electrode arrays, tape was applied to the wafer across the ends of the arrays, as illustrated in Figure 3.7. The alignment is not critical in this step, as long as the tape extends some distance into the electrode array, and the tape is relatively wide (5 mm). This step could therefore be accomplished with a stencil during manufacturing. After Masking, the wafer was centered on the stage and tilted at an angle of 50 $^{\circ}$  with respect to the substrate normal in a vacuum electron-beam evaporator (Kurt J. Lesker) (Figure 3.6(f)). Shadowing by the thick SU-8 feature served to cut the connection between adjacent electrodes, while shadowing by the thinner layer creates the uncoated region on the channel floor between electrodes. Figures 3.8(a) and 3.8(b) show the shadowing effect that occurs between the electrodes due to deposition of metals at an angle. Figure 3.8(c) is a voltage contrast scanning electron micrograph (SEM) image, which shows the electrical isolation of the interdigitated electrode pair. The choice of the deposition angle and the height of the second layer are critical to obtain interdigitation.

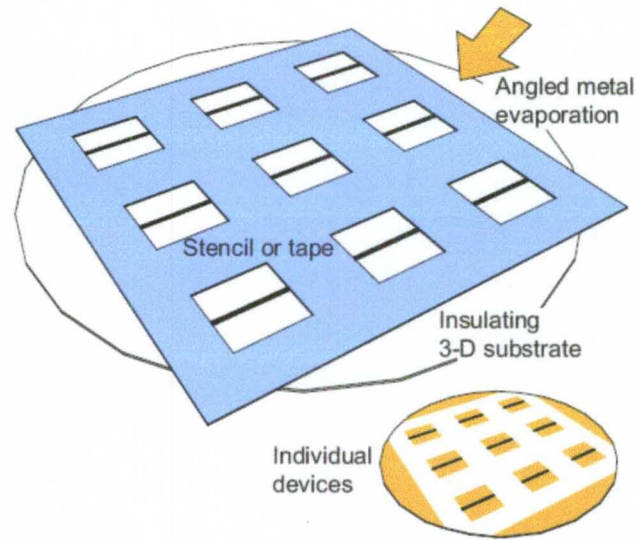


FIGURE 3.7: Large-scale stencil to isolate left and right interdigitated electrodes at the ends of the electrode array.

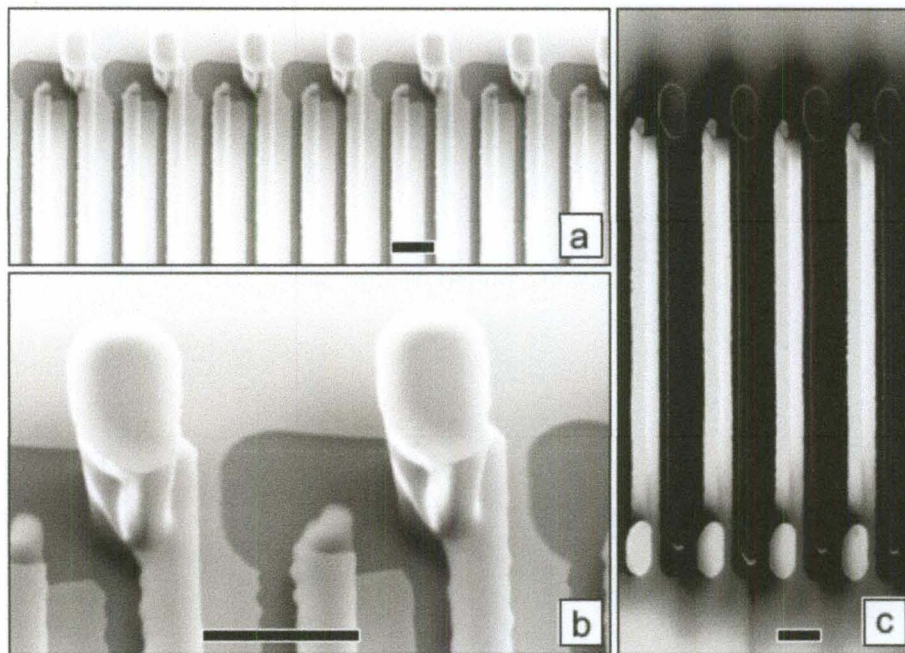


FIGURE 3.8: SEM shows (a) disconnection between the electrodes due to shadowing effect. Gold appears light while shadows appear dark (b) detail of disconnection area (c) voltage contrast electron microscopy shows electrical isolation of the interdigitated electrode pair. Grounded electrodes appear white, while positive electrodes appear black. Scale bars are 25  $\mu\text{m}$ .



To create fluid inlets and outlets, poly (dimethylsiloxane) (PDMS) elastomer microchannels were aligned and sealed over the electrodes. Standard soft lithography techniques were used with SU-8(50) molds to create channels with a typical height of 80  $\mu\text{m}$  ([54], [41]). To make more efficient use of the cleanroom-fabricated SU-8 molds, new PDMS channels were cast on replicated PDMS elastomer molds of opposite “polarity” that were sprayed with Ease Release 200 (Mann Release Technologies). After removal of the second molded PDMS from the PDMS mold, the channels were cleaned in isopropyl alcohol and water to remove the release agent. The PDMS piece was cut to size and holes were punched for fluidic connections.

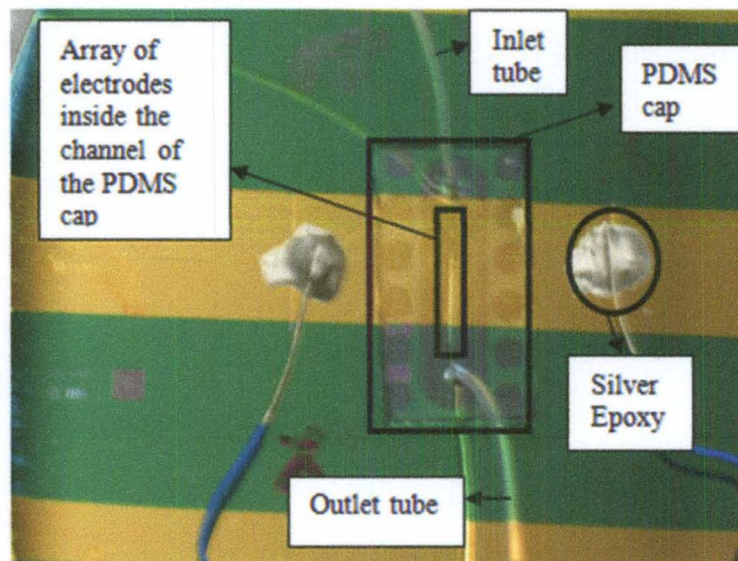


FIGURE 3.9: A photographic picture of the ACEO device shows the electrodes, PDMS cap, inlet and outlet tubes and the conductive epoxy to connect the wires across the device.

The PDMS channels and the 3D electrode devices were then rinsed in water and dried, exposed to air plasma at 9 W RF and 100 mTorr pressure for 30 seconds, aligned under a binocular microscope and pressed together. This sealed the PDMS to metal and

oxide surfaces, with two large metal pads extending beyond the PDMS on the sides of the channel, each connected to opposite sides of the interdigitated electrode array.

Electrical contact wires were bonded to these pads using silver conductive epoxy (MG Chemicals). The entire device was heated to 60 °C in a gravity convection oven for at least one hour to improve the bond between the PDMS and substrate and to cure the conductive epoxy. Figure 3.9 shows a photographic picture for the ACEO device.

## **E. Results and discussions**

### **1. Testing the ACEO pump**

The shadow evaporation method produces a structure with a few differences from the original 3D ACEO pump. Self-shadowing produces a nonconductive wall on the back edge of the step, and there is a conductive pillar at the end of each electrode. For evaluating the performance of this new design, we fabricated a pump with 144 electrode pairs having total length of 5 mm and width of 260  $\mu\text{m}$ . The electrode height was 5  $\mu\text{m}$ , the electrode width was 10  $\mu\text{m}$ , and the spacing between the electrode pairs was 25  $\mu\text{m}$ . The design dimensions are shown in Figure 3.4. These width and spacing, and the 80  $\mu\text{m}$  PDMS channel height were taken from Reference [55], a detailed study of 3D ACEO pump geometry where the electrode height was varied systematically from 0 to 10  $\mu\text{m}$ . The shadowing pillars at the end of the array were 15  $\mu\text{m}$  tall.

Particle imaging velocimetry experiments were then carried out as follows. Tubes used for loading the fluid were connected to the PDMS cap through the inlet and outlet ports as shown in Figure 3.8. The fluid used was de-ionized water with red fluorescent polystyrene beads with 2  $\mu\text{m}$  diameter (fluospheres, Invitrogen Inc.). The

fluid was loaded using a syringe, and experiments were not started until pressure driven flow reached equilibrium and the particles were no longer moving.

Figure 3.10 shows the experiment setup for testing the ACEO device. A function generator (BK Precision 4003A) was used to run the ACEO pumps at different ac frequencies (0.5–100 kHz) at 1  $V_{p,p}$  [peak-to-peak (p.p.)] and 2  $V_{p,p}$ . Videos were captured using a charge coupled device camera (ProgRes CF, JenOptik) and noninverted fluorescence microscope (Zeiss Axioskop2 Plus). Figure 3.11 shows images from the videos captured at frequencies 1 kHz, 20 kHz and 50 kHz and voltage  $2V_{p,p}$ .

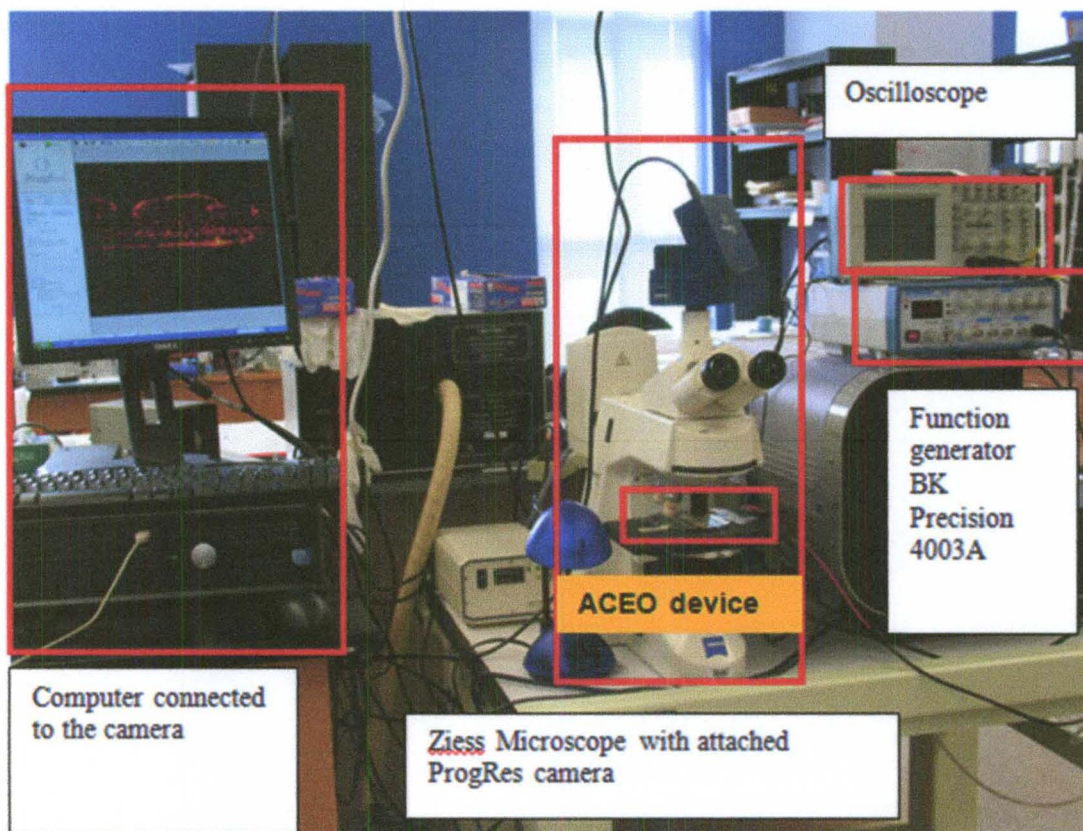


FIGURE 3.10: The experiment setup for testing the ACEO device.

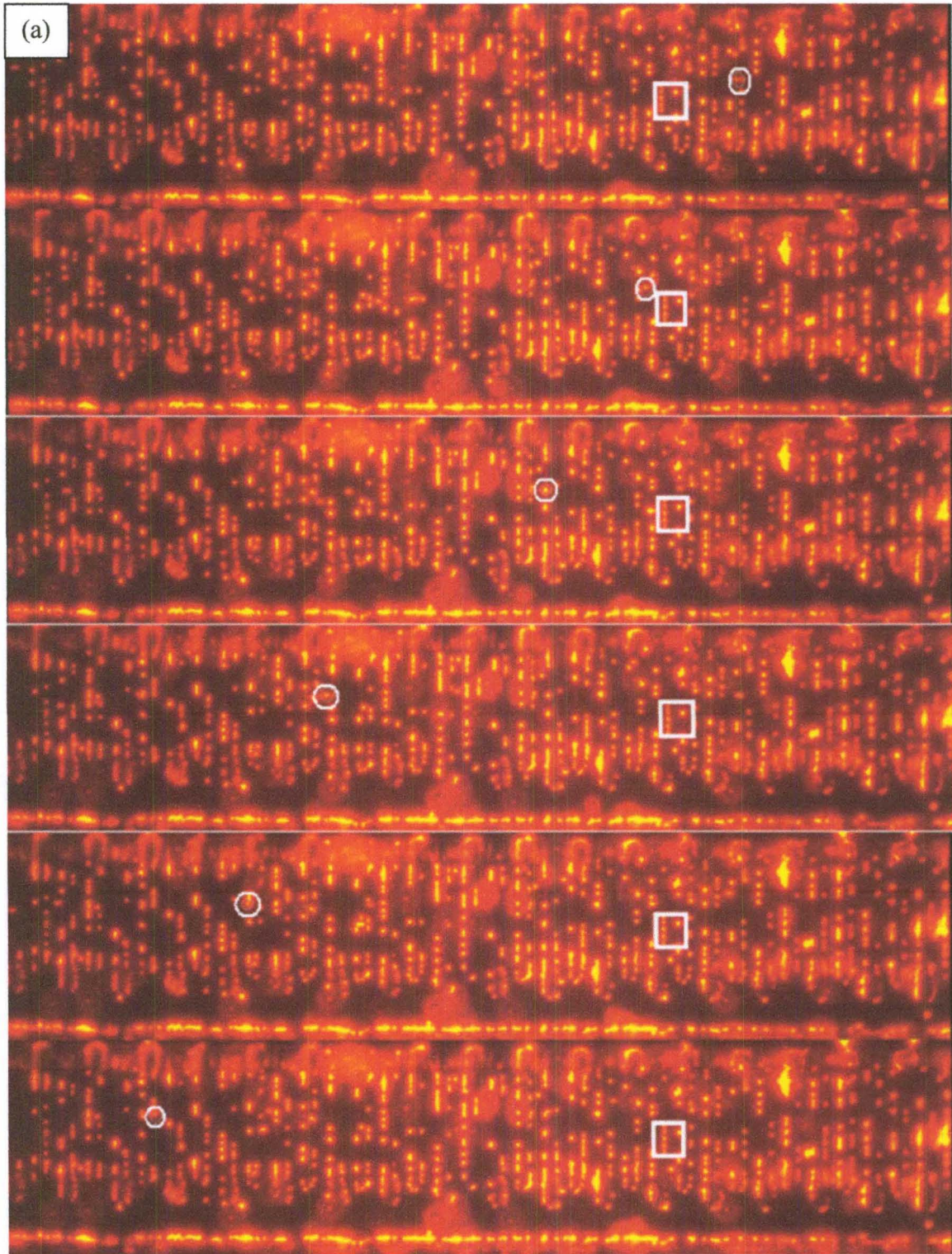


FIGURE 3.11(a): The tracking of a red fluorescent bead (white circle) inside the channel with respect to a reference point (white square) after applying a sinusoidal wave with 2Vpp and frequency 1 KHz.

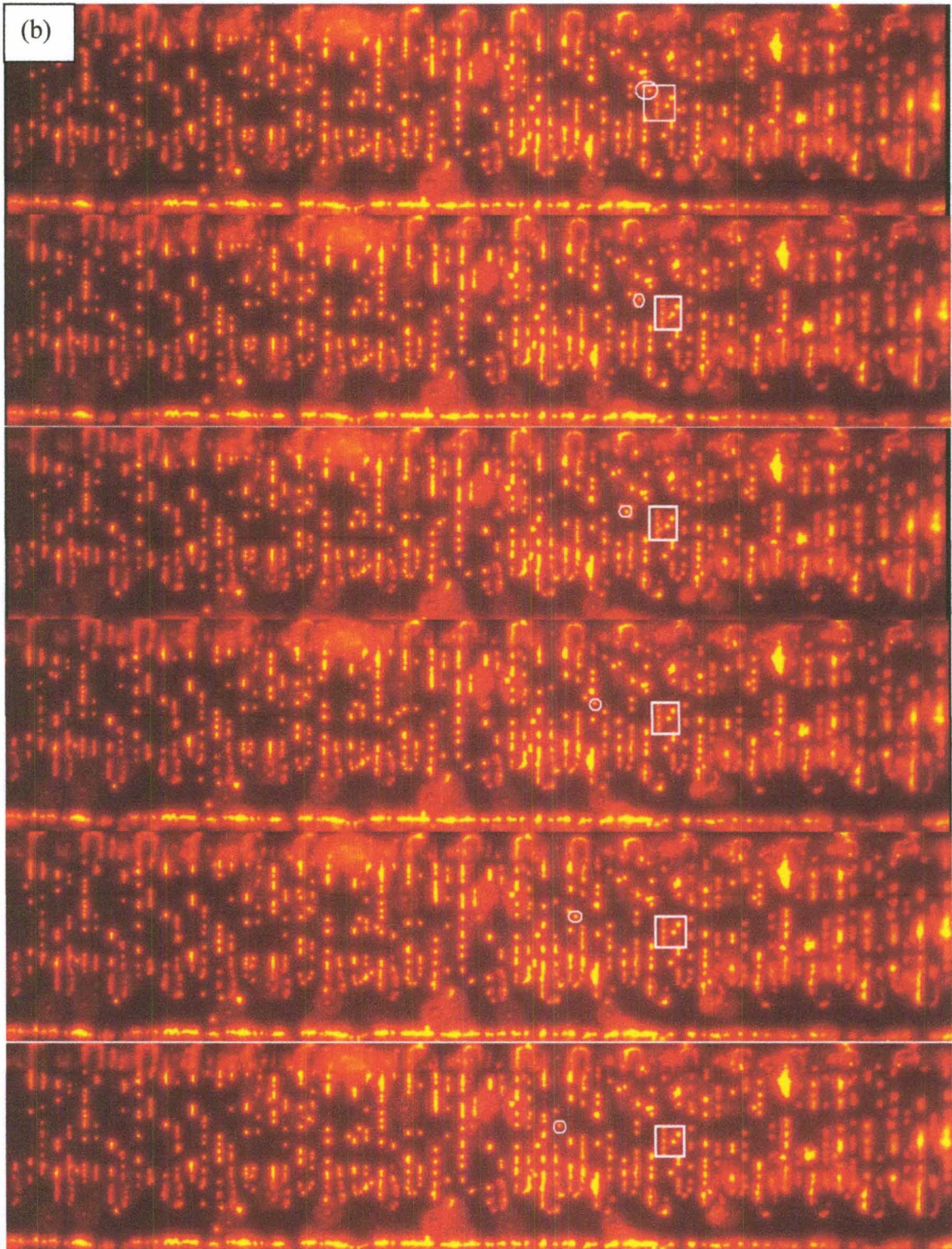


FIGURE 3.11(b): The tracking of a red fluorescent bead (white circle) inside the channel with respect to a reference point (white square) after applying a sinusoidal wave with 2Vpp and frequency 20 KHz.

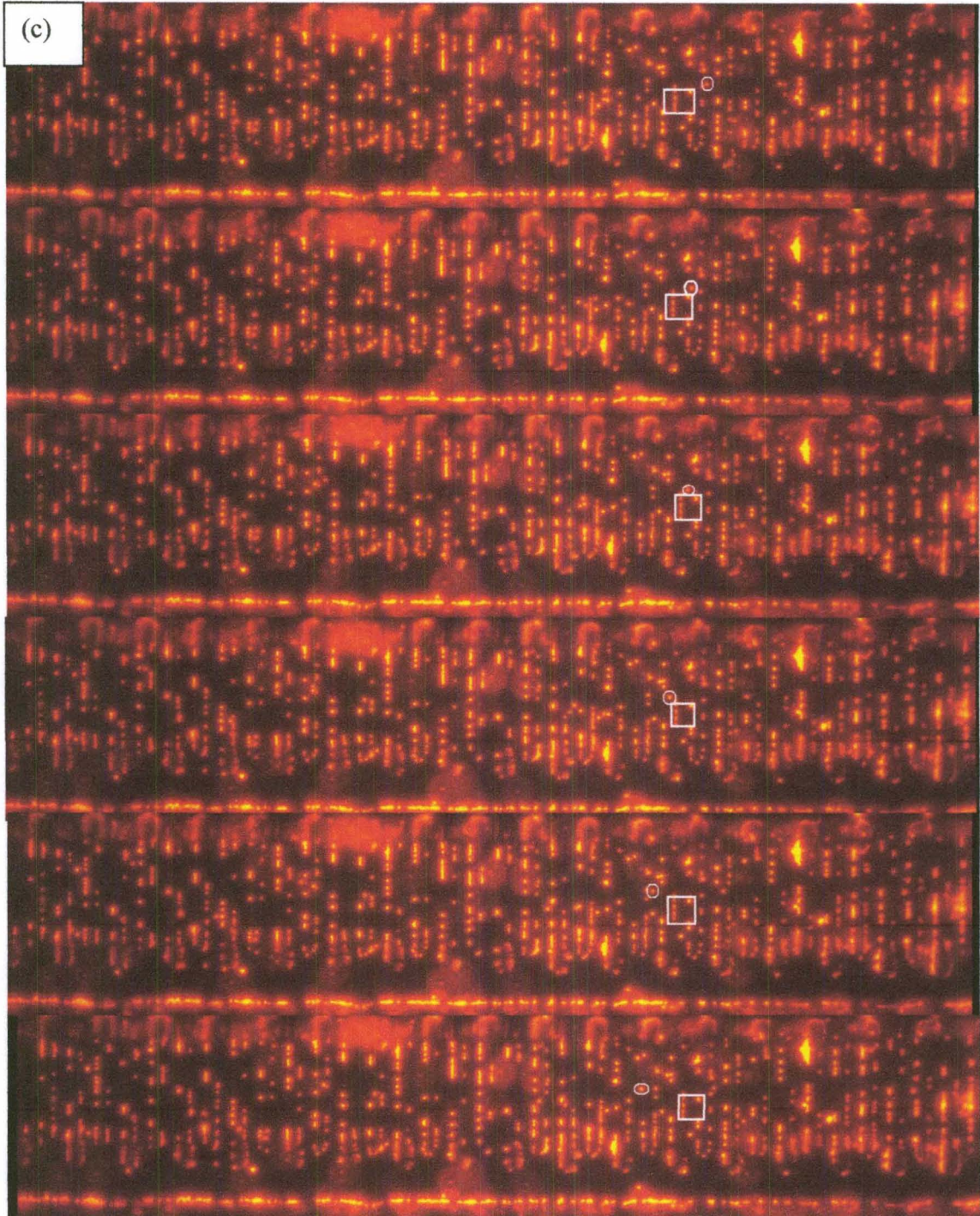


FIGURE 3.11(c): The tracking of a red fluorescent bead (white circle) inside the channel with respect to a reference point (white square) after applying a sinusoidal wave with 2Vpp and frequency 50 KHz.

The centroids of particles in 50 sequential frames were tracked using Imagepro 6 plus software. This software provided the accumulative distances of the tracks in pixels, while the ProgRes camera driver provided a file of frame timestamps.

The velocity was calculated from the slope by plotting the accumulative distance versus time. The mean and the standard deviation of the velocities of the particles inside the channels were calculated based on velocities measured for 3–27 particles at each voltage/frequency setting. Figure 3.12 shows velocity versus frequency for 1 and 2  $V_{p,p}$  driving signals. All velocity measurements were conducted on particles in focus near the pumping surface because there was a recirculating flow observed at the top of the PDMS channel due to buildup of back pressure in the channel and the long tubes used to load the fluid into the device.

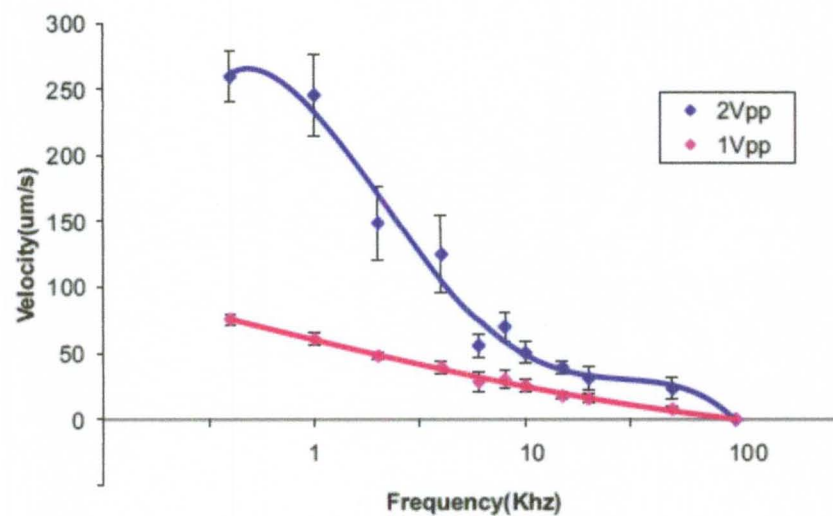


FIGURE 3.12: Semi-logarithmic plot of velocity vs. frequency for the pump at 1 and 2  $V_{p,p}$ .

## 2. Comparison to pumps fabricated by other methods

Figure 3.13 shows the average velocity of the particles inside the channel for this pump along with velocities for three other ACEO pumps extracted from literature, over a frequency range of 0.5–100 kHz at  $2 V_{p,p}$ . The peak velocity at  $2 V_{p,p}$  is  $260 \mu\text{m/s}$  at 500 Hz and the velocity slightly decreases to  $246 \mu\text{m/s}$  at 1 kHz. After 1 kHz, the velocity decays with frequency, then there is a small increase in velocity ( $70 \mu\text{m/s}$ ) around 8 kHz, then it decays again until it reaches almost zero at 100 kHz. The performance is in line with that of previous 3D ACEO pumps, in the range of hundreds of microns per second, and all generate faster flow velocities than the planar ACEO pump. Slight differences in electrode geometry from one publication to another make direct comparison difficult, but these 3D ACEO pumps are qualitatively similar in performance.

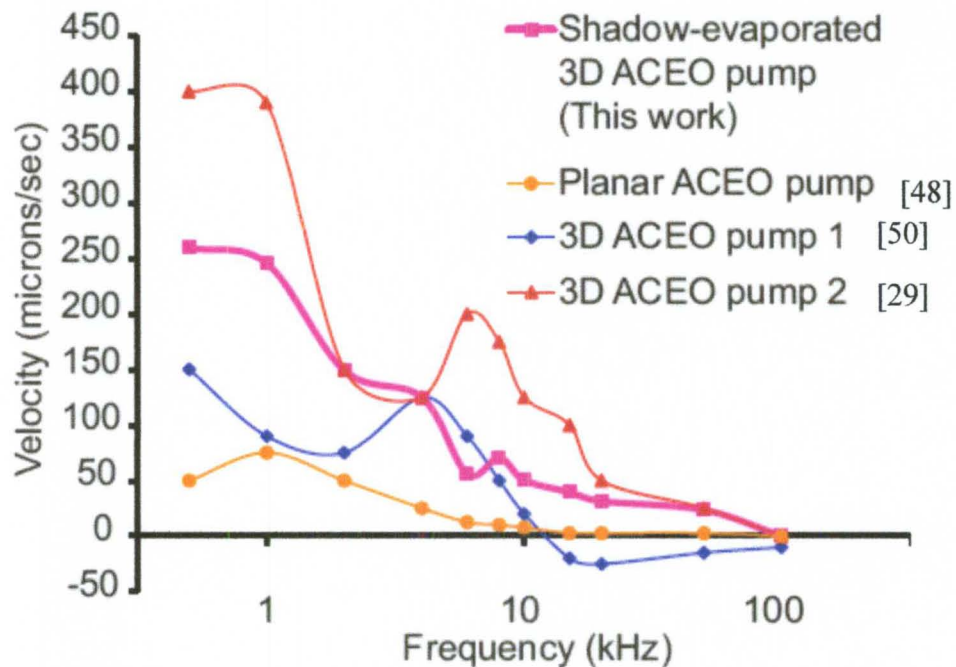


FIGURE 3.13: Semi-logarithmic plot of velocity vs. frequency, comparing the low-cost shadow evaporated ACEO pump in this work to three other published pumps at  $2 V_{p,p}$ . ([48], [50], and [29]).



The velocity of the flow decreases at higher operating frequencies. At low frequencies, most of the voltage applied drops across the double layer, while the voltage across the suspending medium, and therefore the  $E_t$ , are almost zero. This makes the fluid velocity zero. At high frequencies, there is not enough time for the double layer to form and the fluid velocity is zero. So, the fluid flow is zero at low and high frequencies and maximum at a certain frequency.

A second peak of velocity at a higher frequency is observed. This secondary peak [29], [55] is possibly explained by different frequency responses for positive and negative charging in asymmetric electrolytes at high voltages [52]. However, the secondary peak velocity in the proposed pump is not as prominent as the ones in the other 3D ACEO pumps.

## **F. Summary**

This chapter has demonstrated a simple and inexpensive fabrication process to obtain three dimensional interdigitated stepped electrodes. The behavior of the flow of the fluid inside the microchannel of the ACEO pump device was studied at different frequency/voltage settings and found consistent with 3D pumps created by other methods.

## CHAPTER IV

### FABRICATION OF OUT-OF-PLANE ELECTRODES FOR ACEO PUMPS USING SELF-FOLDING TECHNIQUE

This chapter reports the fabrication process of a novel AC Electroosmosis (ACEO) pump with out of plane asymmetric interdigitated electrodes. A self-folding technique is used to fabricate the electrodes, that depends on the strain mismatch between a tensile stressed film (metal layer) and a compressively stressed film (oxidized silicon layer). The electrodes roll up with a well-defined radius of curvature in the range of 100-200 microns. Two different electrical signals are connected to alternating electrodes using an insulating silicon nitride barrier that allows circuits to cross over each other without shorting. The original ACEO microfluidic pump was created with planar arrays of asymmetric interdigitated electrodes at the bottom of the channel. This rolled-up tube design improves on the planar design by including the channel walls and ceiling in the active pumping surface area of the device.

#### **A. Introduction**

Electroosmotic micropumps are essential for low-cost, power-efficient microfluidic lab-on-chip devices used in diverse application such as analytical probes, drug delivery systems and surgical tools.

ACEO pumps have been developed to address the drawbacks of the DCEO pumps such as the faradic reaction and gas bubbles. ACEO pump include arrays of asymmetric

planar microelectrodes have been fabricated [48] to produce a net flow of fluid after their subjection to AC electric field. Rather than using planar microelectrodes, out-of plane three dimensional electrodes will be used to help pump fluids in microchannels when an AC electric field is applied. The method used to create such electrodes is a self-folding technique, which relies on the strain mismatch between layered sheets of materials. The electrodes roll up with a well-defined radius of curvature. This technique is known as ‘strain architecture’.

### **B. Background on Thin Film Stress based assembly (Strain Architecture)**

Self-folding is a deterministic self-assembly method, which is used to obtain a predictable and constrained three dimensional structures. Self -folded structures can be fabricated with diverse mechanisms. These mechanisms include pneumatics ( [56], [57]) magnetic forces ( [58], [59]), swelling of electroactive polymers( [60], [61]), thermal and shape memory alloy actuation( [62], [63]), ultrasonic pulse impact [64], muscular actuation( [65], [66]), stressed thin film ( [67], [68], [69], [70] and [71]) and surface forces [72]. Reference [73] summarized the notable characteristics of these mechanisms in the table below.

“Strain Architecture” or “micro origami” is a self-folding technique used to form uniform out of plane micro/nano structures with a well-defined radius of curvature. This technique utilizes the strain mismatch between two layered sheets of materials. This principle has been used to produce coiled cantilevers and tubes with internal radii down to 2nm by using bilayers of epitaxially grown semiconductor films ( [12], [74], [75]and [76]).

Table 4.1. Self-folding mechanisms [73]

Method	Demonstrated resolution	Notable Characteristics
Pneumatic	mm	Microballoon hinges expand when filled with fluid. Reversible and biocompatible but must remain tethered to fluid supply.
External magnet	$\mu\text{m}$	Ferromagnetic material folds when external magnetic field applied. Must be tethered during actuation and contain locking mechanism.
Permanent Magnet	nm to mm	Attractive force of permanent magnets folds flexible shape when released from rigid substrate.
Electroactive swelling	$\mu\text{m}$	Ionic polymer in electrolyte swells upon application of externally applied electric/ chemical potential.
Thermal bimorph actuation	$\mu\text{m}$	Difference in thermal expansion between two layers causes folding when heated, but requires very high temperatures for even very small folding angles.
Polyimide shrinkage	$\mu\text{m}$	Highly flexible elastic hinges can be selectively activated but require very high temperatures.
Shape memory alloy actuation	$\mu\text{m}$ to mm	Specific materials deflect to predetermined orientation upon heating. Can achieve large gripping force with low actuation voltage. Difficult to deposit and pattern and requires programming of motion.
Ultra sonic pulse impact	$\mu\text{m}$	Ultrasonic pulses are used either to directly actuate a structure in place (via vibration) or indirectly by reducing the static friction of the structure allowing a thermo-kinetic effect to lift structures in place when coupled with heating. Only works at partial vacuum due to drag forces.
Muscular actuation	mm to cm	Harnesses contracting power of muscle cells to bend flexible substrate. Activated by biochemical or electric triggers. Involves biomaterial which may not be stable under many conditions.
Thin film stress	nm to $\mu\text{m}$	Multilayer films deposited with specific process to achieve stress. Active actuation not required for folding.
Surface forces	nm to mm	Utilizes surface curvature of liquids to move attached structures. Mechanically robust if the liquid solidifies into position, but often requires relatively high temperatures that are not biocompatible.

Figure 4.1 shows SEM images of various nanostructures formed from strained Si/SiGe bilayer films. Bilayers of metal and semiconductor also can be used to obtain nanoscrolls with radii less than 500 nm [77] as shown in Figure 4.2 .

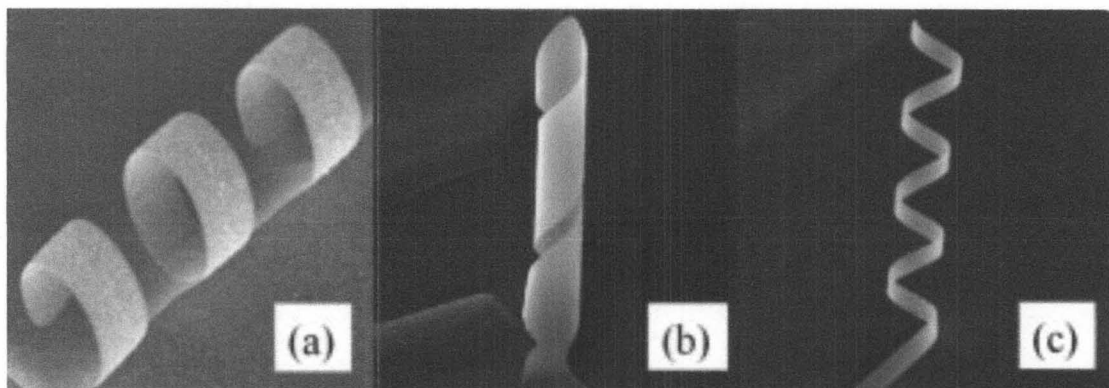


FIGURE 4.1: SEM images of strained bilayer Si/SiGe structures. a) Nanorings of radius  $3\mu\text{m}$ . b) Nanodrills of radius  $2.4\mu\text{m}$  c) Nanocoils of radius  $2.4\mu\text{m}$  [75].

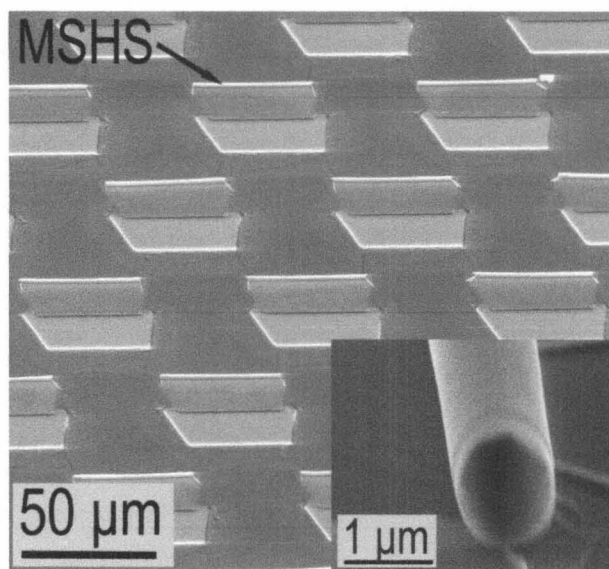


FIGURE 4.2: Array of metal-semiconductor-hybrid sheet (MSHS consisting of a 5 nm chromium layer on a  $6\text{ nm In}_{0.23}\text{Ga}_{0.77}\text{As}$  substrate. The inlay shows a zoom of a MSHS with an outside radius of  $600\text{ nm}$  [77].

Moiseeva et al. [69] use metal-oxide strained bilayers to generate many complex three dimensional structures. Figure 4.3(a,b) shows SEM images of released straight and tilted toroids with 400 nm oxide, 50-60-50 nm Cr-Ni-Cr film and radius of curvature 64  $\mu\text{m}$ . All metal strained bimorph has been produced (Figure 4.4) by controlling the stress in titanium-tungsten (TiW) sputtered thin film [78].

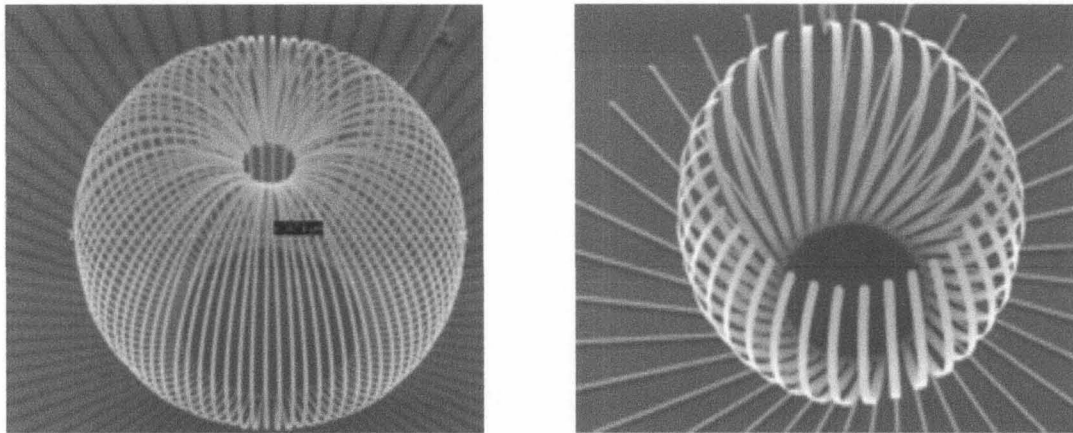


FIGURE 4.3: (a) Released toroid with 400 nm oxide, 50–60–50 nm Cr–Ni–Cr film. Radius of curvature = 64 $\mu\text{m}$ . (b) Released tilted structure with same materials and thicknesses [69].

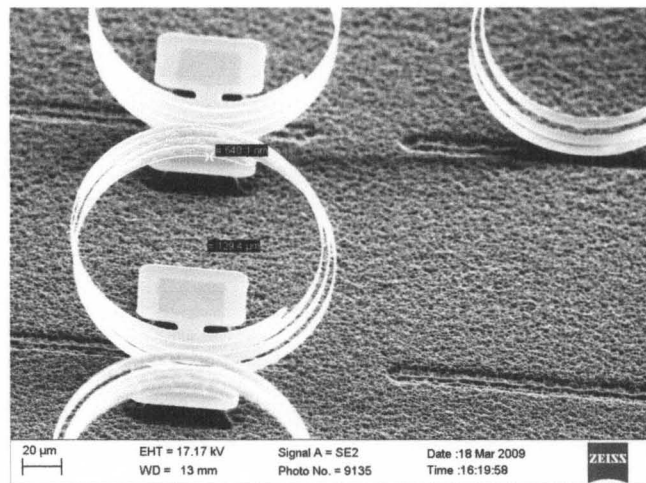


FIGURE 4.4: Microcoils of radius 65  $\mu\text{m}$  made from strained bilayers of titanium tungsten [78].

### C. Applications of Out-of-plane micro- and nanostructures

Figure 4.5 shows SEM images of out of plane micro- and nanostructures have been used as mirrors ([12], [79]), stages [13], shutters [14] and cantilevers to act as field emitters [16]. Figure 4.6 shows an SEM image of nanopipelines to handle fluids [76]. Out-of-plane micro-and nanostructures are used as chemical actuators [80], and electrostatic actuators ([14], [81]) and thermal actuators ([18], [80] and [82]). These actuators are used for manipulating cells and other small objects ([18], [83]). Figure 4.7 shows SEM images of electrostatic micro actuators and thermal actuators.

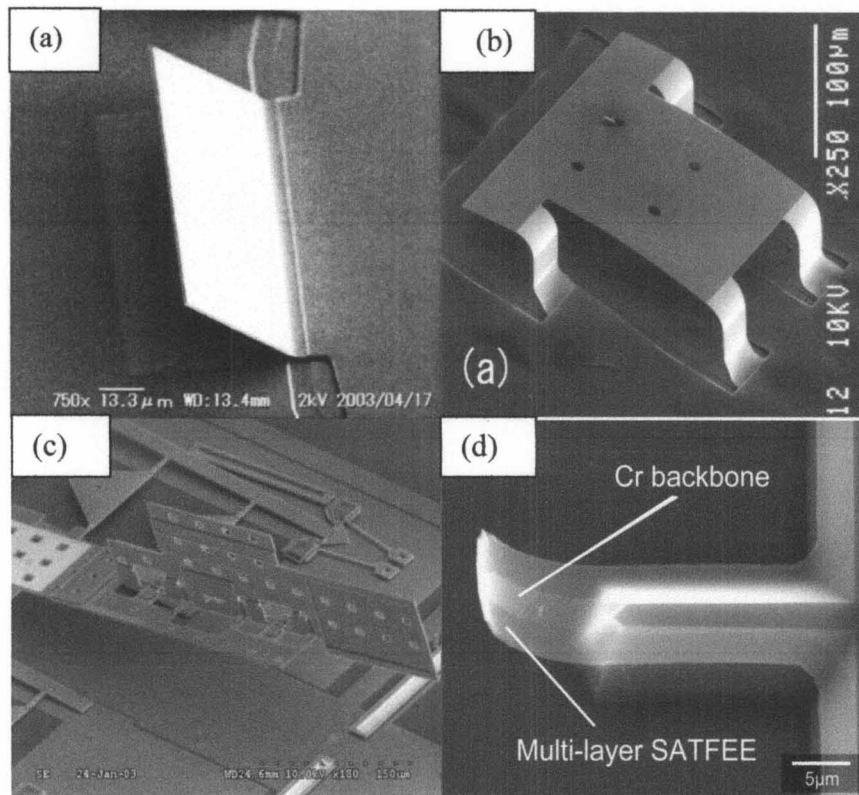


FIGURE 4.5: (a) Standing mirror at an angle of around  $45^\circ$  with respect to the substrate [79] [77]. (b) SEM pictures of micro-stage with hinge length 27  $\mu\text{m}$  [13]. (c) Pop-up shutter chip after full completion of the self-assembly process [14]. (d) Example of a self-assembled thin film edge field emitter SATFEE [16].

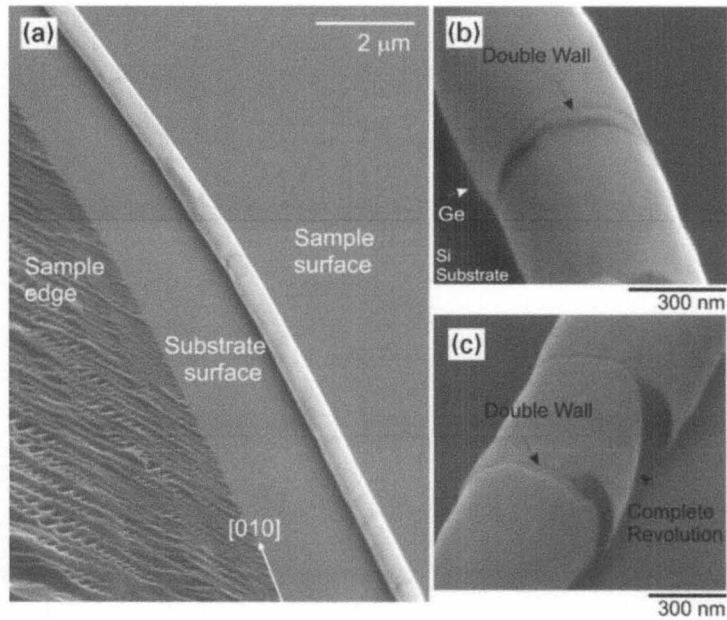


FIGURE 4.6: (a) Rolled up Si/SiGe tube rolled-up. (b) and(c) show that the tube has at least Performed one full rotation [76].

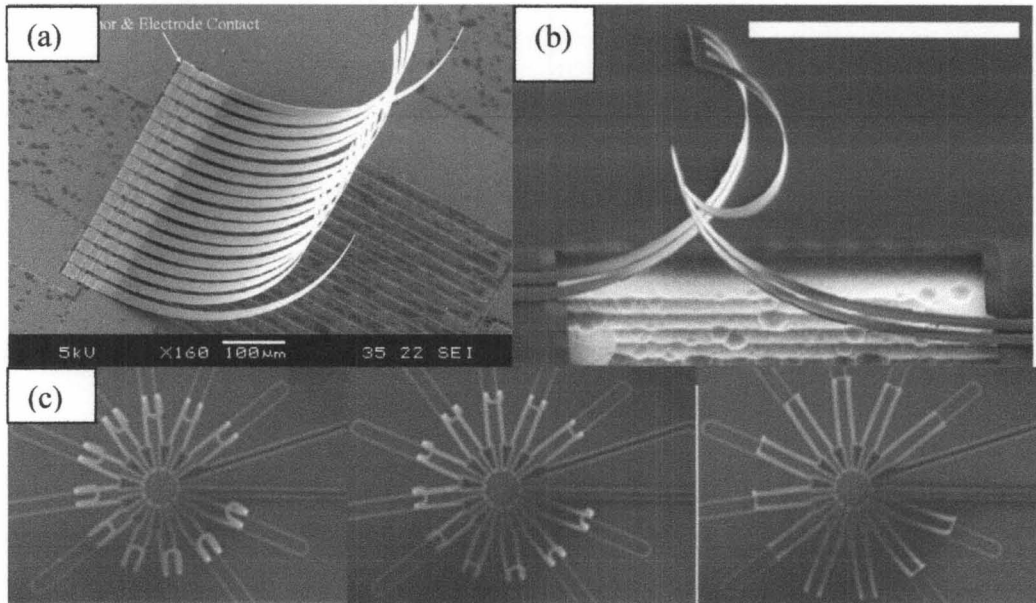


FIGURE 4.7: (a) SEM image of electrostatic micro-actuator [81] (b) SEM of bistable out-of-plane stress-mismatched thermally actuated bilayer devices with large deflection. Scale bars are 200  $\mu\text{m}$  [82]. (c) SEM images of microcage opening as temperature increases from 25C (left) to approximately 160 C (right) by driving a current through the entire structure from contact pads to the right of each frame. Sphere diameter is 250 microns (left most image) [18].



The strain architecture has been used to create three dimensional metamaterials microdevices( [70], [84]) and microtools for biomedical devices [85]. Figure 4.8 shows an SEM image of multi-axis coils which can be used as isotropic electromagnetic resonators.

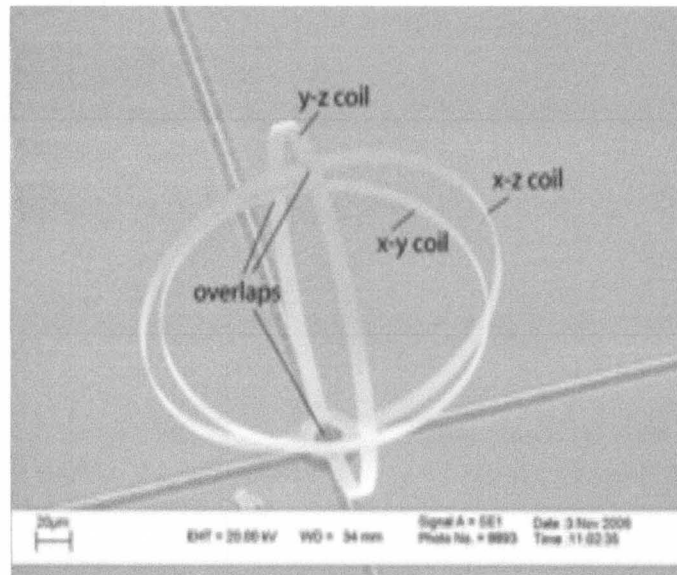


FIGURE 4.8: SEM of multi-axis coils which have potential applications as isotropic electromagnetic resonators [69].

#### D. Strain Architecture Theory

If a thin film layer having compressive stress is coated with another layer having less compressive or more tensile stress, the two thin films will store a potential energy. This strain mismatched structure “wants” to minimize this energy, the same behavior as a spring storing elastic energy. Minimizing the energy is achieved by releasing the material underneath this structure causing this bilayer film to curl uniformly from the substrate. This out-of-plane bending is illustrated in Figure 4.9.

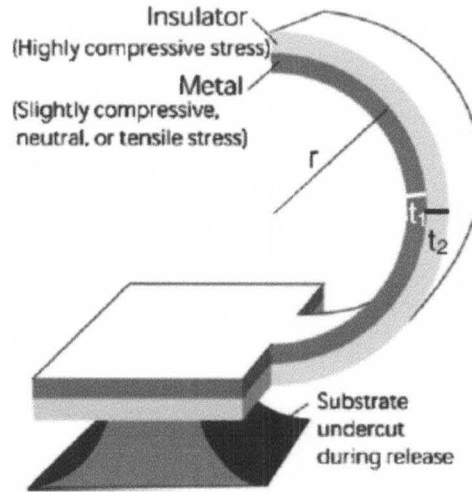


FIGURE 4.9: Schematic of a metal–insulator bimorph bending because of strain-mismatch induced curvature upon release from the substrate.

Beam equations developed for much larger structures can account for most of the features seen in microscale strain architecture devices, although the approximations become less accurate as the curvature radius becomes small relative to beam thickness [81]. For a released beam of uniform width, with no applied moments, the reciprocal of the radius of curvature is given by equation ([12], [69] and [74]).

$$\frac{1}{\rho} = \frac{6 \varepsilon (1 + m)^2}{d [3(1 + m)^2 + (1 + mn) \{ m^2 + (mn)^{-1} \}]} \quad (1)$$

In the above equation,  $\rho$  is the radius of curvature,  $d$  is the combined thickness of the two layers ( $d_1 + d_2$ ),  $\varepsilon$  is the strain mismatch or fractional difference in the unconstrained relaxed lengths of the two layers  $(l_2 - l_1)/l_0$ ,  $n$  is the ratio of the elastic modulus of the layers ( $E_1/E_2$ ) and  $m$  is the ratio of their thicknesses, ( $d_1/d_2$ ). Subscripts 1 and 2 refer to the upper and lower layers, respectively. Bi-directional curvature, important even when the cantilever is narrow, can be accounted for by replacing the

elastic modulus with the biaxial modulus  $E' = E / (1-\nu)$ , where  $\nu$  is Poisson's ratio and  $E$  is the elastic modulus [86]. For many choices of materials, the biaxial moduli are similar ( $n = 0.5-2$ ), making this parameter's effect on the radius of curvature small compared to the effects of strain mismatch and film thickness. The strain mismatch  $\varepsilon$  was computed from this equation (2)

$$\varepsilon = \frac{\sigma_{metal}(1-\nu_{metal})}{E_{metal}} - \frac{\sigma_{oxide}(1-\nu_{oxide})}{E_{oxide}} \quad (2)$$

In equation 2, sigma is the biaxial stress of the oxide and the metal as measured by a profilometer before and after the film deposition. Considerable insight can be gained by assuming that both layers have the same biaxial moduli ( $n = 1$ ). Equation (1) then becomes

$$\frac{1}{\rho} = \frac{6\varepsilon d_1 d_2}{d^3} \quad (3)$$

For two layers with equal biaxial modulus ( $n = 1$ ) and a fixed total thickness  $d$ , the minimum radius occurs when the top and bottom layers have equal thicknesses ( $d_1 = d_2$ ). However, from a practical standpoint, oxidized wafers are typically purchased in a large batch, or oxide is grown on several wafers in one run, so the bottom layer often has a fixed lower layer thickness  $d_2$ , while the upper metal layer thickness  $d_1$  is varied in subsequent processing. In this case, when both materials have equal modulus, the radius is minimized when the top layer's thickness is half that of the lower layer. Adding more material to the top layer only increases the total thickness  $d$  in the denominator, producing a larger radius of curvature. This case is illustrated in Figure 4.10. In general, to minimize the radius if the biaxial moduli are unequal, the layer with the larger modulus

must be thinner than the limits set by the above design rules. From equation 3, the inverse radius of curvature is directly proportional to the strain mismatch  $\epsilon$  (See Figure 4.10).

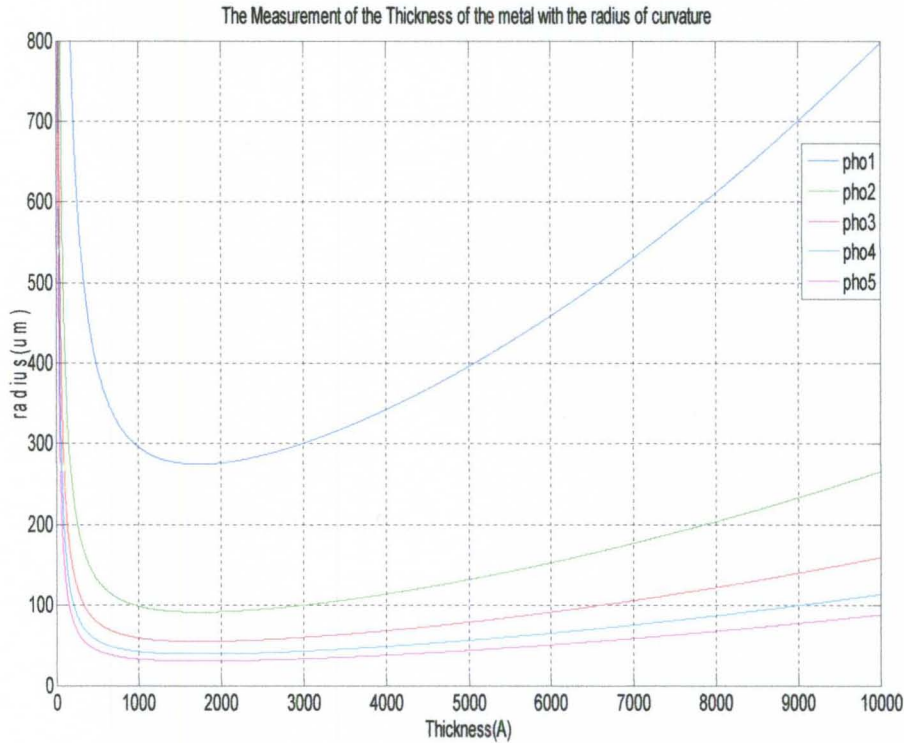


FIGURE 4.10: Plot of the radius of curvature ( $\rho$ ) vs. the thickness of the upper metal ( $d_1$ ) with different strain mismatch values ( $\epsilon$ ). As ( $\epsilon$ ) increases the radius of curvature ( $\rho$ ) decreases.

## E. Out-of plane interdigitated electrodes for ACEO tube pump

### 1. Device design

A two layered design was used to produce the out of plane electrodes. The original electrodes were extremely fragile in facing the water flow, and needed to be linked together by an insulator (See Appendix C for more details).

The new design consists of four layers as shown in Figure 4.11. This will help the electrodes to fold in a sheet of silicon dioxide. The first layer (Red layer) represents an array of interdigitated electrodes connected to a large pad (Pad 1). An array of

interdigitated electrodes (135 repetitions of length 5.5 mm) was built consisting of a small electrode (4.2  $\mu\text{m}$  wide) separated from the large electrode (15.6  $\mu\text{m}$  wide) by a 4.6  $\mu\text{m}$  gap. Pairs of electrodes are separated by 15.5  $\mu\text{m}$ . The length of the electrodes is 1050  $\mu\text{m}$ . The second layer (blue layer) represents the dielectric layer (Polyimide or Silicon nitride) which insulates the first metal layer (red layer) and the second metal layer (green layer) connected to the small electrodes.

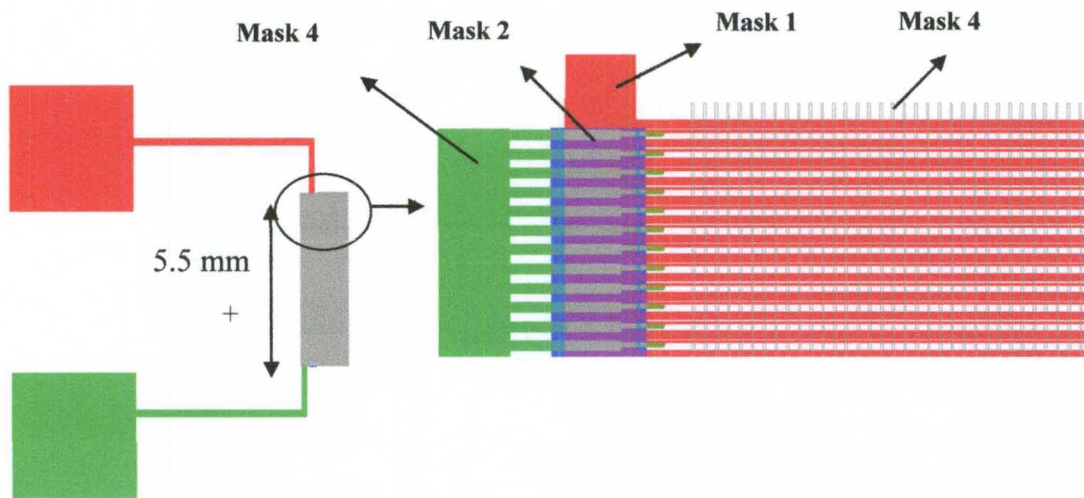


FIGURE 4.11: The layout design of the (a) whole device and (b) part of the interdigitated electrodes showing the four Masks.

The fourth layer (transparent) consists of stripes of thickness five microns. These stripes are the opening windows, where the silicon dioxide and silicon are etched to release the sheet of electrodes.

Figure 4.12 shows the release of five interdigitated electrodes using the coventorware 2010 simulation package. The thickness of the compressive layer (silicon dioxide) is 450 nm, while the gold thickness is 1  $\mu\text{m}$ . As the gold deposition temperature increases the strain mismatch between gold and silicon dioxide increases, this will reduce the radius of curvature of the rolled up sheet of electrodes.

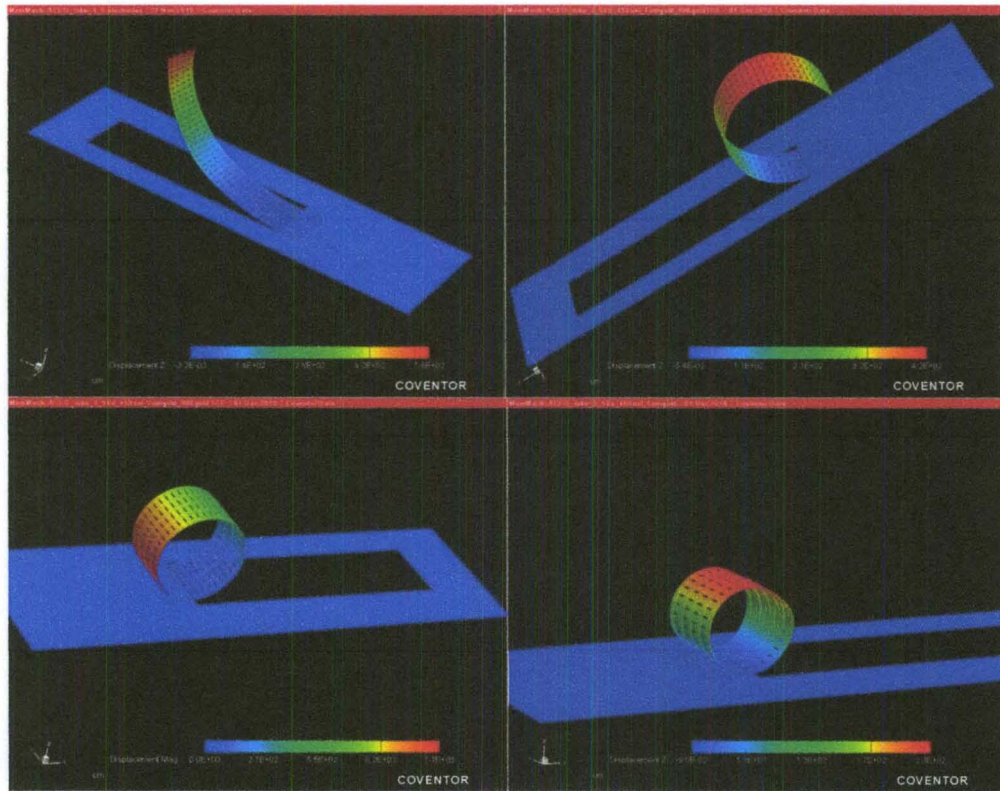


FIGURE 4.12: Coventorware simulation results of five released interdigitated electrode with different TCE of gold with 1µm thickness of gold and 450 nm of oxide.

## 2. Fabrication Process

Thermal oxide ( $\text{SiO}_2$ ) was grown on the silicon wafer (Figure 4.13(a)). The oxide has very high compressive stress due to the differential thermal expansion of the coating and substrate as the wafer cools. Photoresist was patterned on the oxide for liftoff using the Mask 1, and topped with sputtered titanium and gold (Figure 4.13(b)). Gold is chosen as electrode material because it does not form an oxide layer in water. The metal was patterned after removing the photoresist in the acetone liftoff bath (Figure 4.13(c)). Silicon nitride can be used as an insulator layer between two metal layers. Silicon nitride was deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) machine (Figure (4.13 (d))).

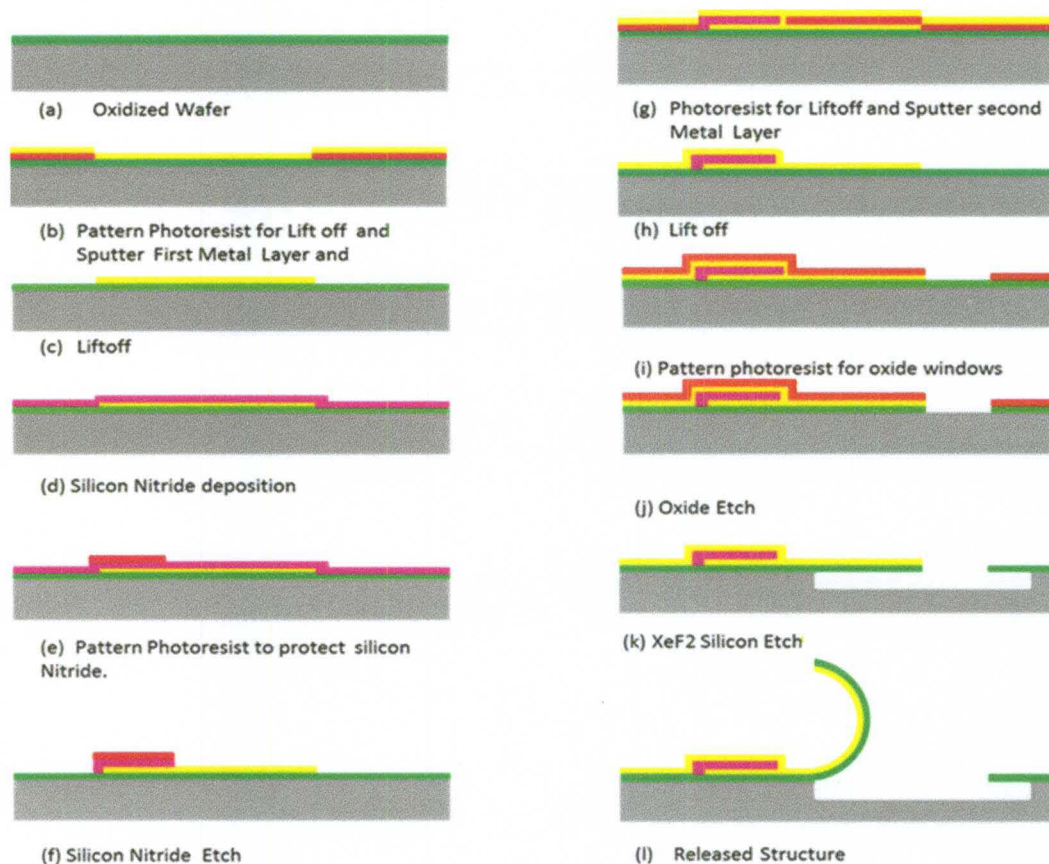


FIGURE 4.13: Microfabrication process of ACEO tube.

Photoresist was patterned using Mask 2 (blue layer) (Figure 4.13(e)) to protect the silicon nitride in the areas where the second metal layer crossed over. The silicon nitride was etched using the March reactive ion etcher (Figure 4.13(f)). The metal layer was patterned using Mask 3 (green layer) to connect the thinner electrode to the second pad (Pad 2) (Figure 4.13 (g and h)). Another layer of patterned photoresist using Mask 4 (transparent layer) was used to create opening windows for the plasma to etch the oxide (Figure 4.13 (i and j)). The resulting patterned bimorphs were then released from the silicon substrate by xenon difluoride ( $\text{XeF}_2$ ) vapor etching, curling out of the wafer plane to relieve the compressive stress in the oxide (Figure 4.13(k and l)). The  $\text{XeF}_2$  etch

process is highly selective to silicon, enabling a wide range of metals and other materials to be used in the process.

**Details of the fabrication steps are as follows.**

1. Wet thermal oxide deposition

Batches of 4 inch, p-doped, 5–20 ohm cm (100) silicon wafers were coated with 400 nm of thermal oxide by a one hour treatment in a tube furnace at 1000 C, with 440 sccm O<sub>2</sub> gas flowing into the furnace through a bubbler filled with 95 C deionized water.

2. Metal patterning by liftoff

The oxidized wafers were treated with hexamethyldisilazane (HMDS) adhesion promoter, followed by coating with LOR 3A photoresist at 4000 RPM for 10 seconds. After 5 minutes of hotplate baking, Shipley 1813 photoresist (Rohm and Haas Electronic Materials) was coated at 4000 RPM for 10 seconds. After 90 seconds hotplate solvent-removal bake at 115 C, the photosensitized wafers were exposed to UV light through a photoMask on a Karl Suss contact aligner. The photoresist was cleared from exposed areas by a two minute development step in MF319 developer (Rohm and Haas), then rinsed in deionized water and dried under nitrogen gas. Wafers with patterned resist were then sputter coated with Titanium gold (Ti-Au) in a Technics sputtering system as follows:

For the titanium adhesion layer, sputter conditions were 120W DC power, 30mTorr argon chamber pressure, for two minutes. For gold, 120 W dc power, 30 mTorr argon pressure and 5–10 min sputter time were used to obtain various thicknesses. Combined layer thickness was measured at 470 nm (for five minutes) using a Dektak profilometer. Following sputtering, the excess metal was removed from the unexposed



resist by liftoff in acetone overnight, or within two hours using ultrasonic agitation in acetone.

### 3. Dielectric deposition

First, polyimide (PI2611) was used as a dielectric insulator between the two gold layers due to its low stress, thermal stability and excellent mechanical properties. However, the polyimide requires a long curing process (seven hours) and the vertical metal deposition is unable to coat the edges of polyimide due to its thickness (1 to 5 microns) (See Figure 4.14).

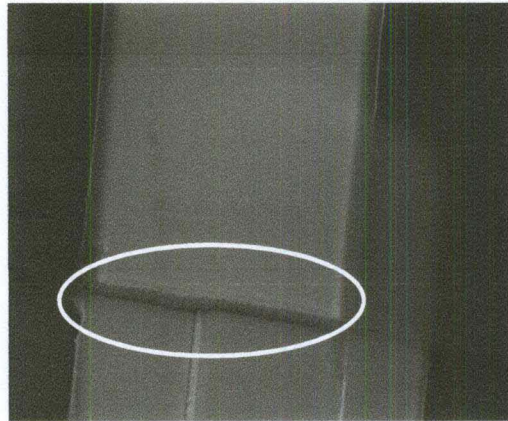


FIGURE 4.14: SEM image for the polyimide showing that vertical sputtering of gold did not succeed to coat the sidewalls.

Polyimide was replaced by silicon nitride to overcome these drawbacks. Plasma etched chemical vapor deposition (PECVD) technology was used to obtain films of silicon nitride with thickness 120-150nm. The silicon nitride had to be thick enough to avoid the pin holes problem. Photoresist 1813 was patterned using Layer 2 (blue) to protect the silicon nitride in the areas where crossovers took place. The March etcher was used to etch the silicon nitride. The parameters used were 200 mTorr pressure of  $\text{CF}_4:\text{H}_2$  at a partial pressure ratio of 40:2 and a RF power of 200W. The time needed to etch 120-

150 nm of silicon nitride was three minutes. Figure 4.15 shows a microscopic image of the device after three steps and it also shows a magnified image of the crossover of the gold on the silicon nitride to connect the thin electrode to the second pad. The voltage contrast analysis using the SEM is useful in determining the separation between the electrodes (See Figure 4.16).

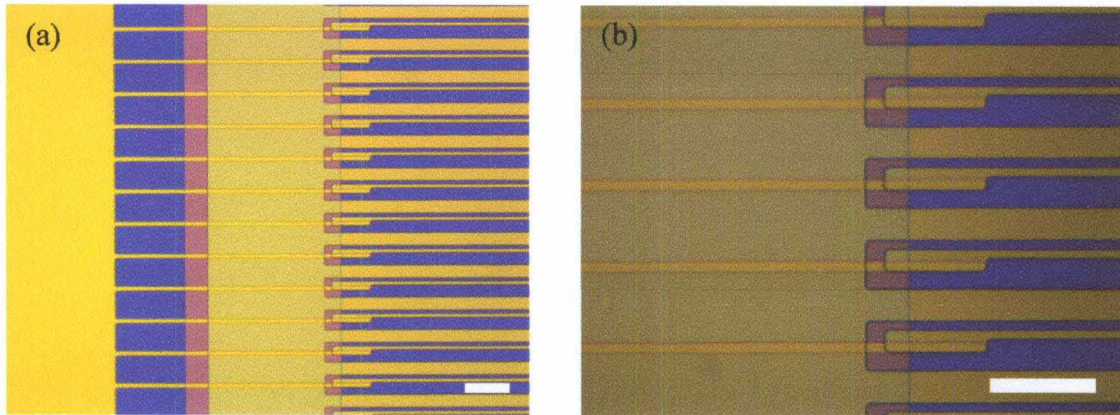


FIGURE 4.15: (a) Microscopic image of the device after three steps. (b) Magnified image of the crossover of the gold on the silicon nitride to connect the thin electrode to the second pad. Scale bars are 50 um.

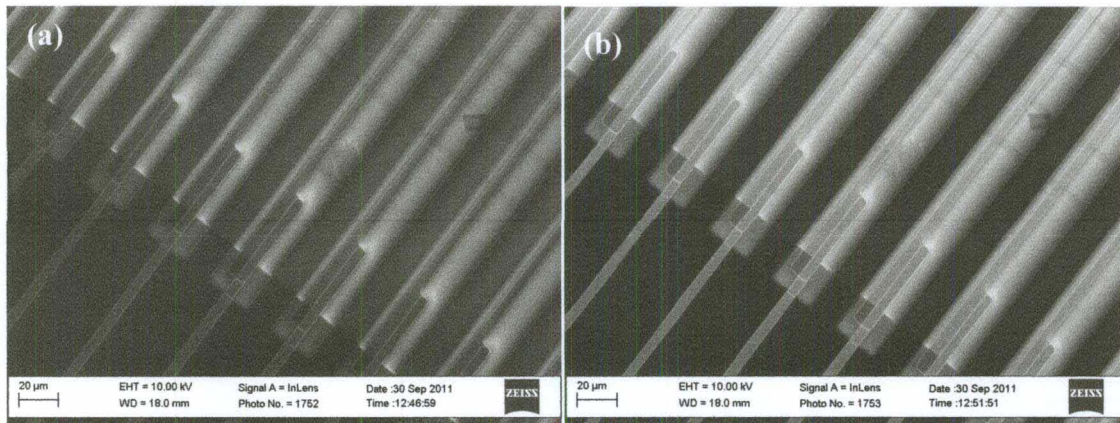


FIGURE 4.16: Voltage contrast SEM images (a) before applying voltage (b) after applying voltage.

#### 4. Oxide etching

Vertical wide stripes were patterned using 1827 photoresist. The stripes and the metal both protected the oxide from etch except for small gaps between the metal and the stripes. These gaps later exposed the underlying silicon to be etched in the  $\text{XeF}_2$  vapor. Wafers were processed in a March plasma etcher, with 240 mTorr pressure of  $\text{CF}_4:\text{H}_2$  at a partial pressure ratio of 50:3 and a RF power of 260W. After ten minutes of etching, the 400 nm oxide was completely removed from any areas unprotected by metal and stripes(See Figure 4.17).

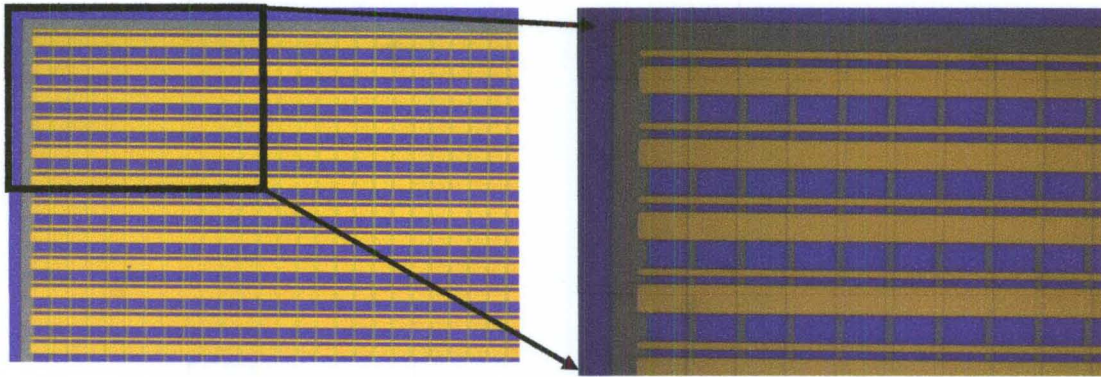


FIGURE 4.17: Microscopic image showing the windows where the  $\text{XeF}_2$  etches the silicon.

#### 5. Release by isotropic silicon etch

Bimorphs were released from the wafer by undercutting in a  $\text{XeF}_2$  dry silicon etcher (Xactix). This isotropic etch process completely removed silicon from the underside of the oxide layer, and left a silicon cusp on the substrate at the centerline of the released structure. The etch process required 20 or more 30 second cycles of exposure to an atmosphere of 3 Torr  $\text{XeF}_2$  for complete release. The etch rate depended on the area of exposed silicon and varied from pattern to pattern. Figure 4.18(a) shows

SEM images of the electrodes after the release by the XeF<sub>2</sub> machine. Figure 4.18(b) shows a tube of the rolled up electrodes and the oxide stripes, which help the wide and thin electrodes release at the same time. The voltage contrast SEM images in Figure 4.19 show that the adjacent electrodes in the rolled-up tube are separated.

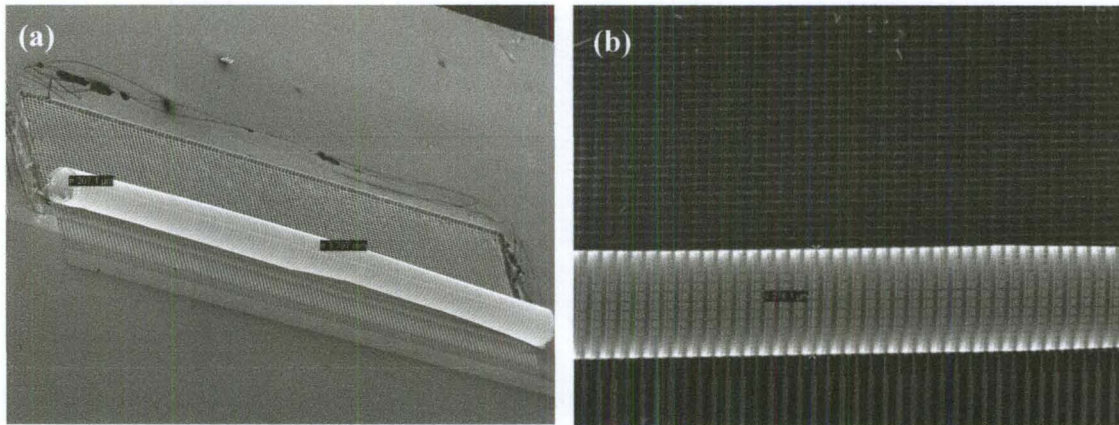


FIGURE 4.18: SEM images of (a) the rolled up interdigitated electrodes (b) the zoomed-in image of the tube showing the details of the thin, wide electrodes and the oxide stripes connecting the electrodes together.

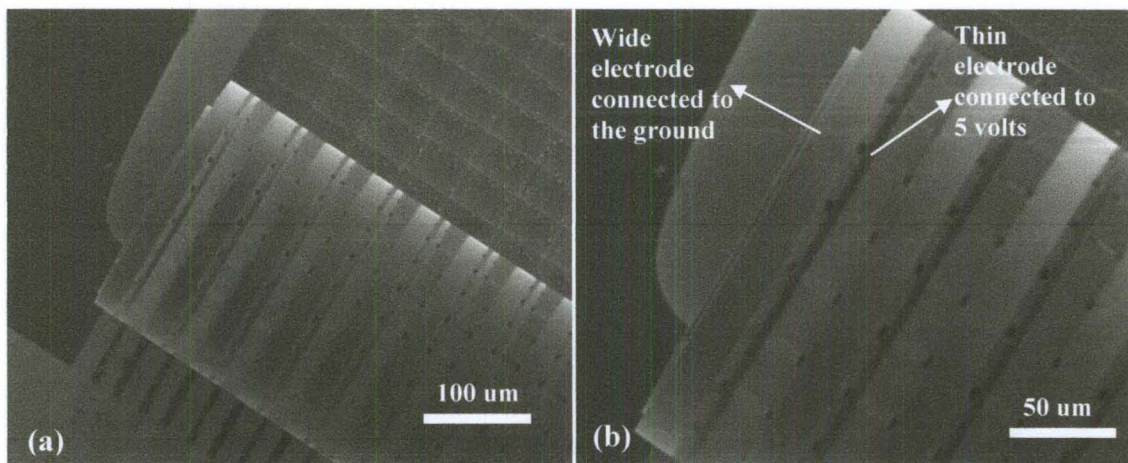


FIGURE 4.19: Voltage Contrast SEM image for the electrodes after being released (a) with no voltage applied (b) after applying 5 volts across the electrodes.

## F. Testing the device

The rolled-up tube was capped with a PDMS lid removed from a mold with a channel depth of 300  $\mu\text{m}$  and width 750  $\mu\text{m}$  to cap the tube without damaging it. The mold shown in Figure 4.20(a) was fabricated using 150  $\mu\text{m}$  of SU-8 100 followed by DRIE step to etch 150 microns from the silicon substrate. Figure 4.20(b) shows the whole device after capping the PDMS lid over the electrodes, the inlet and outlet for loading the fluid and the wires connected to the Pads using silver epoxy. After capping the device with the PDMS lid, the resistance across the electrodes is reduced dramatically to few ohms.

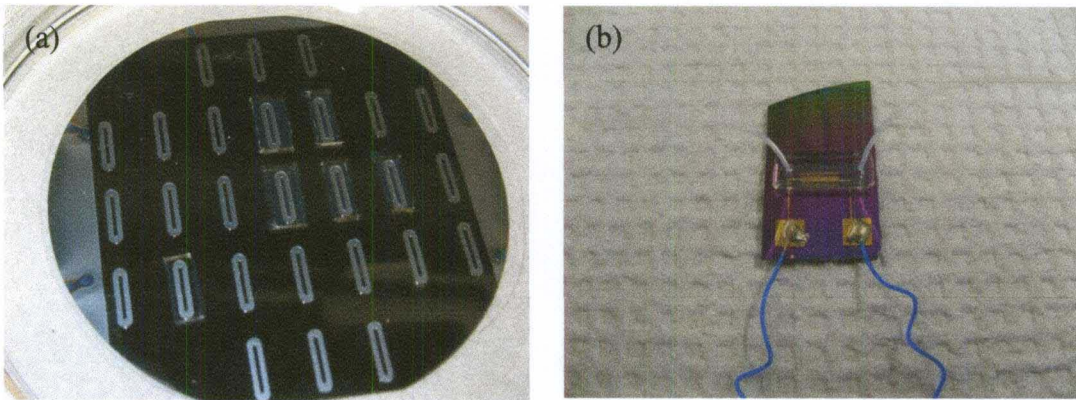


FIGURE 4.20: (a) The PDMS mold. (b) The whole device after capping the PDMS lid over the electrodes.

In some devices, the resistance across the electrodes was in kilo ohms after capping them with PDMS lid. These devices were tested using the same experiment setup shown in Figure 3.10 and the fluid used was de-ionized water with red fluorescent polystyrene beads with 2  $\mu\text{m}$  diameter (fluospheres, Invitrogen Inc.). After applying the voltage across the device (1vpp and frequency 500 Hz), no pumping was observed.

## **G. Summary**

The strain architecture technique managed to produce a rolled up layer of silicon dioxide containing asymmetric interdigitated electrodes. Coventorware was used to simulate this rolled up sheet of electrodes. Capping the rolled up electrodes with the PDMS lid reduced the resistance across the electrodes to kilo or hundred ohms and no fluid pumping was observed. Although it did not happen in this case, the rolled up tube can likely enhance the fluid flow because all of the channel walls can be used in pumping the fluid.

## CHAPTER V

### CONCLUSION AND FUTURE WORK

The dissertation presented different fabrication techniques which have been used to create three dimensional electrodes for driving and sensing flow in microfluidic devices. Lithographic patterning and ion milling, as discussed in chapter two, have been used to create three-dimensional symmetric and asymmetric posts with vertical sidewalls, which have conductive metal coatings and embedded three-dimensional electrodes. Electrokinetic phenomenon, called induced charge electroosmosis, creates micro-vortices around the posts which mixes the biological sample with reagents, one of the most time consuming steps in the detection process. A numerical model was used to design several different devices for microfluidic mixing. Out of these the triangular-post design was identified as a good performer and was constructed using microfabrication techniques. Rapid mixing was observed and quantified through video microscopy.

The dissertation in chapter three introduces a simple, cost effective method for the fabrication of three dimensional stepped electrodes for fast ac electro-osmotic pumps. The fabrication method is based on shadowing evaporation of metal on a three-dimensional insulating substrate. The velocity of the fluid (DI water) was measured at different voltages and frequencies and was consistent with published results from more complex fabrication methods. This work can be extended by fabricating serpentine 3D stepped interdigitated electrodes using the shadowing e-beam evaporation; this will

increase the speed of flow and reduce the back pressure [29]. The behavior of the flow can be studied with DI water and ionic electrolytes such as, KCl and NaCl with different concentrations. The electrodes can be injection molded, which will reduce the cost of the chip. The shadowing beam evaporation technique can also be used to produce 3D stepped electrodes in the nanoscale.

The dissertation in chapter four introduces the strain architecture technique, which was used to produce a rolled up layer of silicon dioxide containing asymmetric interdigitated electrodes which can be used as an ACEO pump. Capping the rolled up electrodes with the PDMS lid reduced the resistance across the electrodes to a few ohms and no fluid pumping was observed. Although no pumping was observed, the rolled up sheet can likely enhance the performance of the ACEO pumps over the ACEO pump using planar electrodes because all of the channel walls can be used in pumping the fluid. This rolled up tube can be also used in pumping gases. The future work for this project can be focused on troubleshooting the problem of the resistance reduction which happened across the electrodes after capping them with the PDMS lid. The capillary action technique can be used as a substitute for the PDMS lid. A new design is recommended to avoid the use of the dielectric insulator; this will reduce the number of masks and the fabrication steps used. A simulation package like Covntorware or Comsol can be used to guide the new design of the rolled up electrodes and simulate the behavior of the fluid inside the rolled-up tube. Microsolidics is a fabrication method used to create 3D metallic microstructures in PDMS [87]. The asymmetric electrodes can be patterned and rolled up in a PDMS layer. After finishing the device fabrication, the behavior of the fluid flow inside the tube can be measured with different voltages and frequencies.



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## APPENDIX A

The main parts of the circuits of the square wave generator which lead to the required output to drive the mixing in the Ninja Star device will be discussed. The LM555 chip is to generate a signal that varies in time. The flip flop is responsible to make the signal with duty cycle 50%.The inverter generates two signals which are 180 degrees out of phase by running one of the signals through the inverter twice. The inverter also sources current that the 555 cannot provide. The voltage control module is to control the level of voltage going to the EMCO Q02-5. The EMCO Q02-5 produces the high voltage and the high voltage depends on the output of the voltage control. The switching circuit takes the output signals from the inverters and the voltage level from the EMCO chip to get the required output (Figure 1).

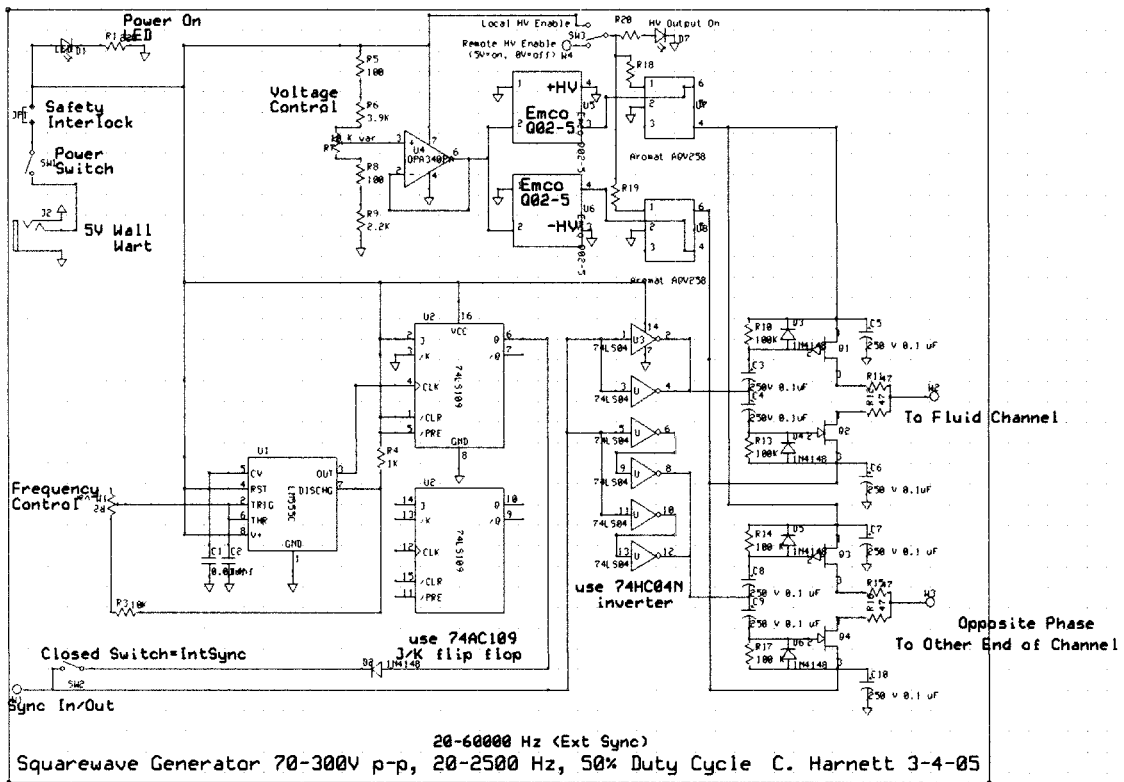


Figure 1: The schematic layout of the HV power supply.



## APPENDIX B

### INDUCED CHARGE ELECTROSMOTIC THEORY

If an electric field is applied to an electrode immersed in an electrolyte, the electrode will be charged with a surface charge ( $\sigma_{q0}$ ). The electrode will then attract ions of opposite charge (counter-ions) from the electrolyte and repel ions with like charge (co-ions). The counter-ions layer can be subdivided into two layers (this termed the double layer). The first layer with charge density  $\sigma_{qs}$ , referred as Stern layer, is strictly bound to the surface of the electrode. The second layer with charge density  $\sigma_{qd}$ , referred to as diffuse layer, contains a high density of counter-ions and low density of co-ions. The charged electrode, Stern layer and the diffuse layer are called Electrical Double Layer (EDL). The counter-ions in the double layer are completely screening the electrode surface charge so the overall charge in the bulk medium is zero. The charged electrode has electrostatic potential  $\Phi_0$ . The value of the electric potential at the slipping plane (the boundary between the Stern and diffuse layer) is called Zeta potential ( $\zeta$ ), which is a very important parameter in the theory of interaction of colloidal particles. The potential decays exponentially with a characteristics length  $\kappa^{-1}$ , Debye length, from the charged electrode. Figure 1 shows a schematic of the double layer of counter-ions near the charged electrode. It also shows a graph of the decay of the potential with the distance  $y$  from the electrode [88].

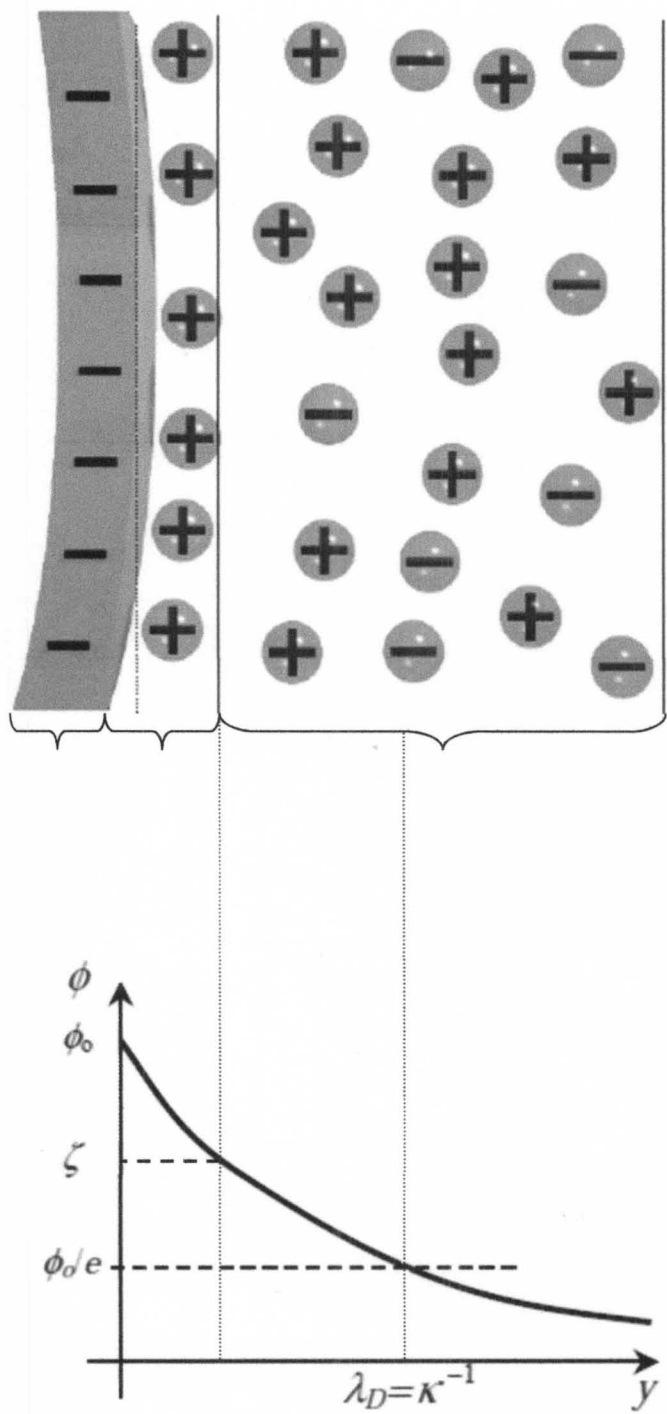


FIGURE 1: Schematic diagram of the negatively charged electrode with surface charge ( $\sigma_0$ ), the stern layer with charge density  $\sigma_s$  and the diffuse layer with charge density ( $\sigma_d$ ). Also shown is the potential decay with distance  $y$  from the charged electrode [88].

### Electroosmosis velocity in DC electric field

Figure 2 shows a schematic model of a fluid element of volume  $A dy$  in an infinitely wide planar channel ( $y=\infty$ ). When a voltage is applied to the electrode, a coulomb force ( $F_x$ ) is acting on the fluid element.

$$F_x = E_x \rho A dy, \quad (1.1)$$

$E_x$  is the tangential component of the electric field and  $\rho$  is the charge density per unit volume. The Coulomb force is opposed by frictional forces ( $F_\eta$ ) due to the viscosity of the fluid ( $\eta$ ).

$$F_\eta = \eta A \left( \left( \frac{du_x}{dy} \right)_y - \left( \frac{du_x}{dy} \right)_{y+dy} \right) = - \eta A \frac{d^2 u_x}{dy^2} dy \quad (1.2)$$

$$F_x = F_\eta \quad (1.3)$$

$$E_x \rho A dy = - \eta A \frac{d^2 u_x}{dy^2} dy \quad (1.4)$$

The charge density From Poisson's equation is

$$\rho = - \epsilon \nabla^2 \Phi = - \epsilon \frac{d^2 \Phi}{dy^2}, \quad (1.5)$$

After substituting the charge density in equation (3.5) can be written as

$$E_x \epsilon \left( \frac{d^2 \Phi}{dy^2} \right) dy = - \eta \left( \frac{d^2 u_x}{dy^2} \right) dy \quad (1.6)$$

Integrating from  $y = \infty$  to the slipping plane where the potential becomes equal to the zeta potential ( $\zeta$ ) and the fluid velocity is zero, the fluid velocity equation will be

$$u_x = - \frac{\epsilon E_x \zeta}{\eta} = \frac{E_x \sigma_q}{\kappa \eta} \quad (1.7)$$

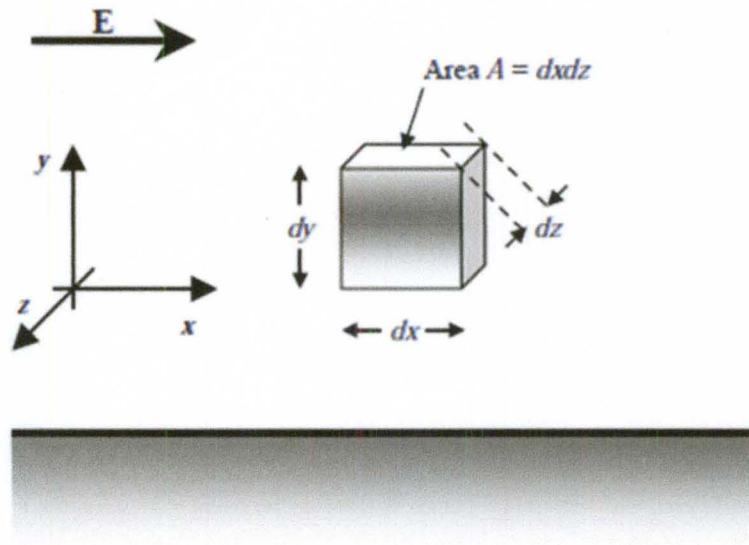


FIGURE 2: Schematic of the Fluid model of volume  $A dy$  in the presence of the Electric field ( $E$ ) [88].

The electroosmosis velocity is directly proportional to the tangential electric field and the charge density in the double layer.

## APPENDIX C

### Device design

The first design to create the out of plane electrodes consists of two Masks as shown in Figure 1. The first layer contains 200 interdigitated electrodes with dimensions 15  $\mu\text{m}$  for the wide electrode, 5  $\mu\text{m}$  for the thin electrode and five microns gap between the electrodes. The length of the electrodes is 650  $\mu\text{m}$ . The second layer (blue) has openings to protect the silicon dioxide and silicon from etching. The silicon dioxide connects the pair of electrodes together. SEM images in Figure 2 show the top and side views of the released electrodes.

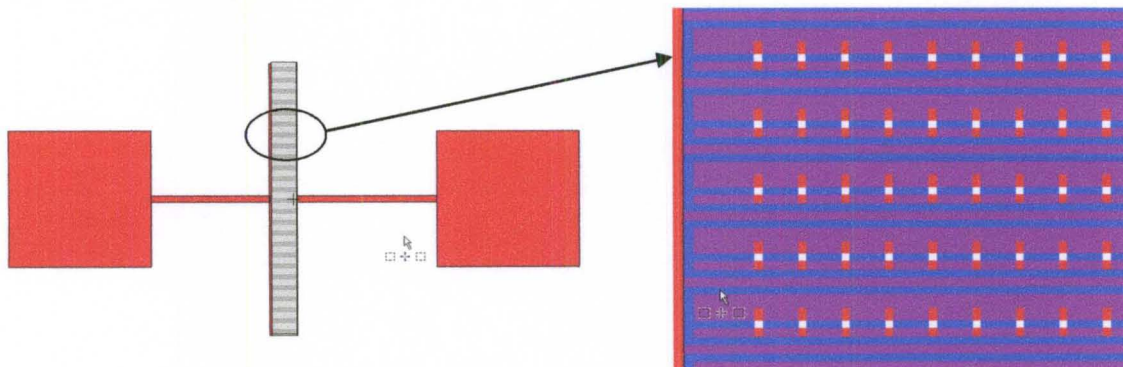


FIGURE 1: a) The device layout shows an array of electrodes connected to contact pads b) Magnified picture for the electrodes (red) topped with layer two (blue), which creates windows to etch the silicon dioxide and silicon.

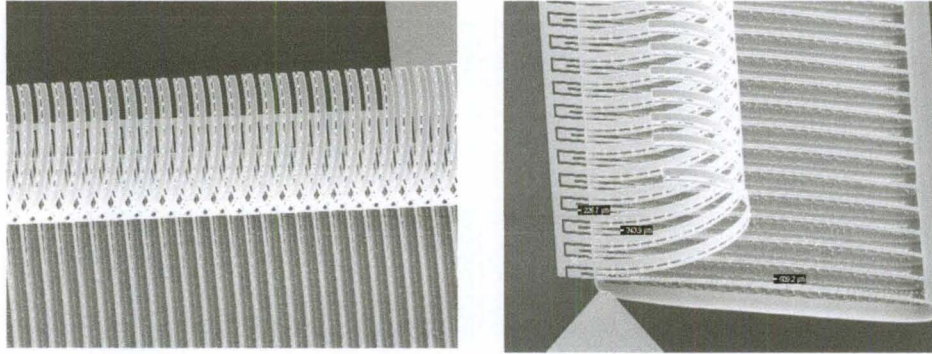


FIGURE 2: a) Top view and b) Side view SEM images for the released structures

There are two drawbacks of this design. 1) The weakness of the released electrodes, which are damaged when it is subjected to fluid (DI water) as shown in Figure 3. 2) The silicon under the metal lines connecting the thin electrodes to the contact pad is etched which makes the connecting line are so fragile. To overcome these two drawbacks, the design has been modified to produce a released sheet of silicon dioxide containing the electrodes as discussed in chapter 4.



FIGURE 3: Microscopic image of the damaged electrodes after the water flow.

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