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An Electronically Reconfigurable Three Band Low-Noise Amplifier in 0.5 μm GaAs pHEMT Technology

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AN ELECTRONICALLY RECONFIGURABLE THREE BAND LOW-NOISE AMPLIFIER IN 0.5 µm GaAs pHEMT TECHNOLOGY

A Thesis Presented

by

JEFFREY A. SHATZMAN

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To my sister for showing me there is more than one way to get things done and to my parents for always supporting me with whatever crazy thing I've been up to.

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ABSTRACT

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May 2011

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State-of-the-art RF front-end circuits are typically designed to operate at a single frequency. With an increasing number of available wireless standards, personal mobile communication devices require an increasing number of individually designed RF circuits. To save space and cost, one alternative possibility is to reuse much of the circuitry by utilizing electronically reconfigurable topologies. The ubiquitous low-noise amplifier is one of the many circuits that can be redesigned with the reconfigurable aspect in mind. In this thesis, previous work in reconfigurable LNAs is reviewed as well as a brief comparison of CMOS and GaAs processes used for RF amplifiers. Three new reconfigurable LNA topologies are also presented. The first two topologies, based on the common-gate stage and synchronous filters, are investigated but not manufactured. The third design, based on the cascode topology, was manufactured in a 0.5 μm GaAs process with enhancement-mode and depletion-mode pHEMTs. The LNA features 12.7 dB, 13.6 dB, and 13.9 dB of gain and noise figures of 2.7 dB, 3.5 dB, and 4.2 dB at 2.5, 3.6 and 5.8 GHz, respectively. The LNA draws 41 mA from a 3.3 V supply.

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CHAPTER 1

INTRODUCTION

1.1 History and Motivation

Wireless transceivers are found in an increasing number of consumer electronic products. High end devices connect users to each other as well as to the internet using numerous dedicated RF links. Each link operates in a single frequency band, and for each band, dedicated hardware is required. There is active research into reorganizing these RF circuits and the systems they work in. Instead of having separate circuits for each separate RF band, researchers have proposed the use of electronically reconfigurable circuitry capable of operating across the frequency bands used by the different wireless protocols. There are several advantages to having a system that is adjustable and electronically controlled: (1) separate RF circuits in a product take up IC space and reducing the number of circuits and overall circuit area reduces cost (2) a reconfigurable circuit can communicate via new wireless standards as they are introduced without requiring new hardware, and (3) as circuit parameters shift over time due to deterioration, onboard computers can adjust the RF circuit parameters to maintain optimum system performance.

On the receiver side of the RF system, antennas, low-noise amplifiers, filters, mixers, switches, power splitters, and oscillators must all be reconfigurable for the entire receiver to be considered reconfigurable. Low-noise amplifiers are interesting circuits because their design includes many of the problems associated with active circuits such

as stability and linearity. LNAs also need to meet other specs such as gain, match, isolation, and noise.

One modern LNA design is the source degenerated cascode. For a typical cascode, the frequency band is set by as few as two lumped element circuit components, which can - for the most part - be independently designed. By electronically adjusting just these two key components, the frequency response of the entire amplifier can be readjusted without need to physically change the circuit topology.

The source degenerated cascode is not the only LNA topology amenable to electronically adjustable components, though. The common-gate amplifier has the advantageous property of having a very wide bandwidth into microwave frequencies. By adding a frequency dependent negative feedback loop, the circuit can display the desired narrow-band operation. The frequency response can be adjusted by a single reactive component. For this design, the electronically controlled components can be hidden away in the feedback loop. Typically the electronically reconfigurable components are more lossy than their traditional counterparts. By putting them in the feedback loop, they potentially can be isolated from the main signal path.

A third possibility is to use synchronous filters to select a desired channel. Synchronous filters convert RF energy to a different frequency band, filter at the different band, and reconvert back to the original band of operation. The advantage of synchronous filters is that the frequency response of the system can be controlled by the frequency of a single oscillator. By adjusting the oscillator frequency, the frequency response of the filter can be re-tuned.

1.2 Summary of Chapters

The remainder of this thesis is organized as follows. Chapter 2 reviews the basic theory behind LNA design, the important circuit parameters, compares GaAs to CMOS for RFICs, and reviews previous work in reconfigurable LNA design. Chapter 3 introduces two new LNA designs. The circuits are described in detail and the advantages and disadvantages of each circuit are discussed. Chapter 4 introduces a modification to the state-of-the-art cascode LNA that was fabricated and includes a comparison of the new reconfigurable LNA to a traditional receiver which is composed of two separate single band LNAs and a switching network to select one of the two LNAs. Chapter 5 presents the measured data of the fabricated LNA including S-Parameters (gain, isolation, input match and output match), noise figure, input and output third-order intercept points, and input referred gain compression. Chapter 6 concludes the thesis and presents ideas for future work.

CHAPTER 2

BACKGROUND INFORMATION

This chapter gives a short background of low-noise amplifiers and reviews previous work in reconfigurable designs. It also contains a brief comparison of GaAs and CMOS technology.

2.1 Low-Noise Amplifiers for Mobile Applications

The low-noise amplifier is a critically important component in both analog and digital down-converting RF receivers. In digital systems, the bit error rate improves as the signal to noise ratio of received signals improves. Likewise, in analog systems, signal fidelity improves when there is less noise to corrupt the desired signal. To maximize the ratio of signal strength to noise strength, an LNA is required. According to the Friss Formula, the noise figure of a system of cascaded components is dominated by the first stage noise if the gain of the first stage is sufficiently large. Hence, the primary job of the LNA is to have large gain and low noise.

Noise and gain are not the only important parameters of the LNA. Other factors to consider include the stability, the linearity, the input match, the output match, the power consumption, and the physical size of the IC.

The linearity of an LNA impacts distortion, and signal distortion translates into effective noise. For LNAs the non-linear effects are due to non-linear transconductance and non-linear resistance. Gain compression and intermodulation distortion are common problems.

The input and output match influence other parameters. The match can be used to maximize gain or minimize noise figure. A narrow-band match at the input can protect non-linear devices from strong out of band interferers. Typically there are tradeoffs that have to be made in order to achieve acceptable values for gain, noise, and bandwidth.

Die size is an important factor in determining the cost to manufacture an integrated circuit. In the same technology, a smaller die will be less expensive.

Power consumption is an important consideration for any electronic circuit but in mobile devices its importance is magnified. The power supply for a mobile device - a battery - holds a limited charge. If the circuit consumes less power, the battery stays charged longer. Power consumption is traded off for improvements or worsening of gain, noise, and linear range.

When designing a low-noise amplifier, all these factors have to be taken into consideration. And typically they are not independent of each other. Different amplifier topologies have their own advantages and disadvantages. For example, common-gate amplifiers can be used for wide-band applications but typically suffer from poor noise figure.

2.2 Semiconductor Technology

2.2.1 GaAs pHEMT

The gallium-arsenide pseudomorphic high-electron mobility transistor has historically been a popular transistor for building active microwave circuits. The pHMET is a field effect transistor with a gate, source, and drain. When a voltage is

applied from drain to source, a voltage on the gate controls the current that travels though a channel between the drain and source. The channel forms in an undoped layer of semiconductor material which yields carriers with a very high mobility. This mobility translates into a large transconductance which results in devices that are capable of high gain and low noise. The devices are ideal for LNAs and active mixers. The pHEMT also demonstrates low on-resistance and a large off-resistance making the pHEMT ideal for switches and resistive FET mixers. Other structural additions to the pHEMT can further increase the current carrying capabilities of the channel allowing the pHEMT to operate well as a power amplifier [1].

2.2.2 GaAs pHEMT vs. CMOS

Compound semiconductors have historically been at the forefront of microwave frequency active circuits. Processes such as gallium arsenide have been industry favorites because of better gain and noise figure compared to the cheaper, ubiquitous silicon CMOS technology.

Recent advances in CMOS, most importantly the ever present scaling down of transistor sizes, have made silicon a viable choice for RF circuits. The scaling of the transistors has yielded higher and higher operating frequencies. For 65 nm CMOS, the f_t of the NMOS device optimized for RF performance has been pushed to 250 GHz and the f_{max} has been pushed to 220 GHz. The noise performance is also improved. At 2.4 GHz, the minimum noise figure for the NFET device has been improved to 0.2 dB and at 5.8 GHz improved to 0.3 dB [2].

Compound semiconductors still dominate in terms of highest speed, though. A modified 50 nm gate length InGaAs/InAlAs/InP HEMT had measurable gain over 15 dB at 340 GHz in a three stage amplifier. By extrapolating the measured results, the designers claimed to have created a HEMT with an f_{max} of just over 1 THz [3].

Gallium arsenide still plays a pivotal role in RF MMICs and particularly in power amplifiers. One of the strongest points is the power efficiency of the GaAs technology especially at high frequencies. The improved efficiency is due to the higher breakdown voltage of the GaAs transistor over the MOSFET. As MOSFET sizes scale smaller, their maximum operating voltage decreases. When the operating voltage is low, current must be high. With such a large operating current, losses through any resistance are significant [1]. The low Q inductors in silicon have a considerable resistance associated with them; thus, the power delivered to the load is lowered and the efficiency is decreased. With GaAs, the higher operating voltage means less current is required for the same output power. The load of the output stage of the PA is higher and therefore the losses in the matching networks are lower and a higher percentage of the power from the transistor is delivered to the load. The higher Q inductors available on a semi-insulating GaAs substrate are also beneficial in reducing loss. In implementation, a 60 GHz power amplifier in GaAs pHEMT technology has demonstrated a PAE as high as 30.6% [4]. In comparison, a CMOS power amplifier has demonstrated a PAE of 14% at 60 GHz [5].

One major advantage of building GaAs LNAs is that the LNA, power amplifier, and any switches can be integrated onto a single die reducing required space in any product and reducing overall manufacturing costs. In addition, at higher frequencies, GaAs still demonstrates better noise figure. For example a 150 nm GaAs process offers a

depletion mode pHEMT with a minimum noise figure of 0.7 dB at 15 GHz [6]. In contrast, in an optimized 65 nm CMOS process, the NFET device offers a minimum noise figure of around 1.3 dB at 15 GHz [2].

2.3 Prior Work on Reconfigurable LNAs

There has been a significant amount of effort already placed into the design of reconfigurable low-noise amplifiers. The designs vary widely and include the cascode, common-gate LNAs, and wide-band common-source topologies.

2.3.1 Source Degenerated Cascode

The source degenerated cascode low-noise amplifier is a very popular choice of low-noise amplifier. It features low noise, high gain, low power consumption, and good linearity. The source degeneration adds a narrow bandwidth and good quality input match. The topology of the circuit without biasing is shown in Figure 2.1.

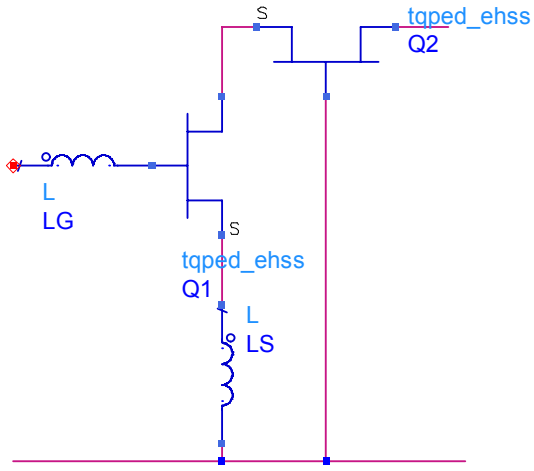


Figure 2.1 - Source Degenerated Cascode

The first order model input impedance is

$$Z_{in} = \frac{g_{m1} L_S}{C_{GS1}} + j\left(\omega(L_S + L_G) - \frac{1}{\omega C_{GS1}}\right) \tag{2.1}$$

where g_{m1} and C_{GS1} are the transconductance and the gate-source parasitic capacitance of transistor Q_1. L_S is used to raise the real part of the input impedance to match the source impedance. L_G is added to tune out the parasitic capacitance at the desired frequency of operation. The frequency response of the circuit's gain is often controlled by an LC tank after the common-gate stage.

The cascode is also an excellent topology for reconfigurable amplifiers. As few as two components can control the frequency of operation: the input inductor and one of the two reactive components in the output tank. Several new circuits have been proposed that take advantage of this. One such circuit uses two inductors in series with a switch to short circuit one of the two inductors [7]. The schematic is shown in Figure 2.2.

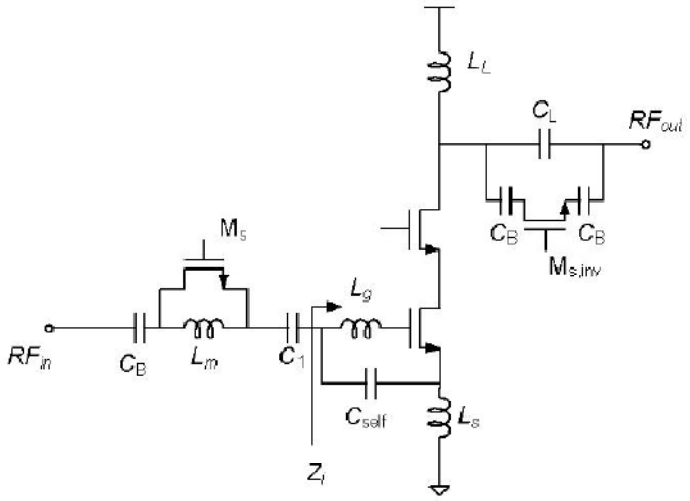


Figure 2.2 - Cascode LNA with switching inductor [7]

At the output, another switch is placed in parallel with the DC blocking capacitor C_L. When the switch, made by MOSFET $M_{s,inv}$, is off, the DC blocking capacitor determines the output match because the off switch acts primarily as a large resistance. When the switch is on, the switch looks like a small resistance. The output match is then determined by the DC blocking capacitor C_L and the switch's DC blocking capacitors C_B. By turning just two switches on, the amplifier can be tuned to two separate bands: 2.4 GHz and 5.2 GHz.

Another proposed circuit replaces gate inductor L_G with an electronically tunable floating inductor [8]. The schematic of the circuit is shown in Figure 2.3. In the circuit, if capacitor C_C is large enough to be considered a short circuit at RF and inductor *RFC* is large enough to be considered an open circuit at RF then the impedance Z_{inA} is

$$Z_{inA} = \frac{j\omega L_g}{1 + g_{mMS1} R_A} \tag{2.2}$$

If R_A is replaced with a FET operating in the triode region, the resistance R_A can be controlled by the gate-source voltage of the FET M_A. The resulting impedance is continuously tunable. The limiting factor is how accurately the gate voltage of the triode FET can be controlled. At the output, the capacitor of a parallel LC tank is augmented with a varactor yielding a continuously tunable frequency response for the gain of the circuit.

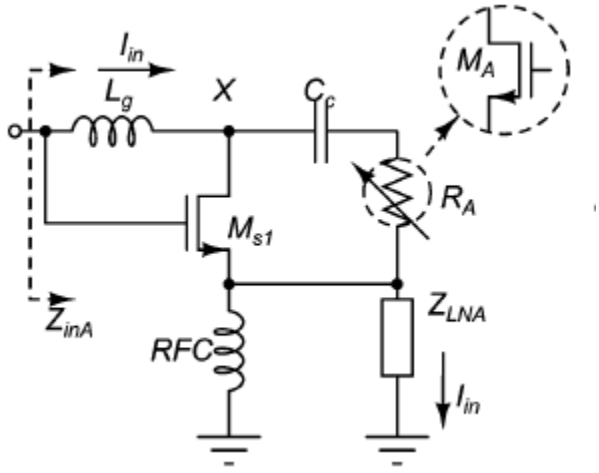


Figure 2.3 - Tunable floating inductor [8]

2.3.2 Two Stage LNA

Another recently proposed reconfigurable LNA is shown in Figure 2.4. The amplifier is broken into two stages.

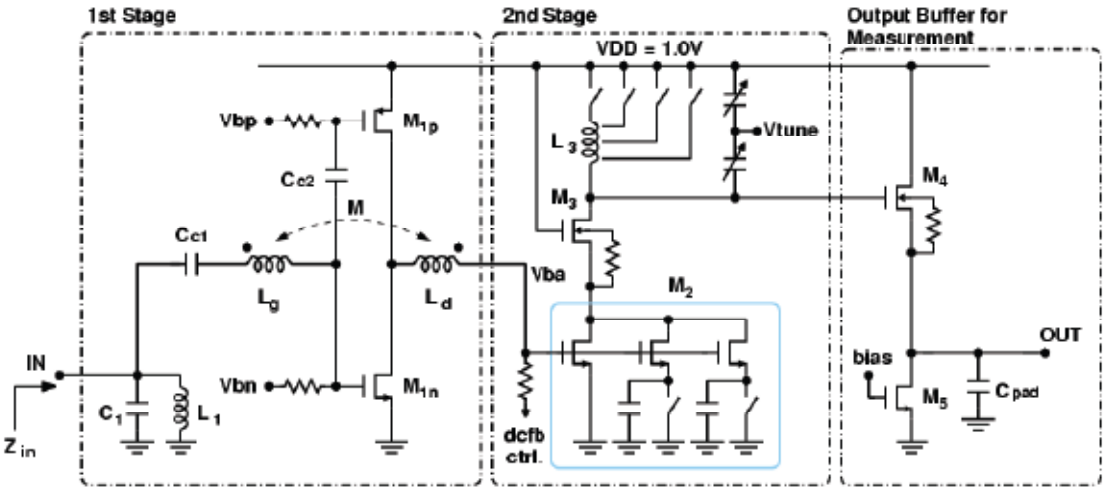


Figure 2.4 - Two Stage LNA [9]

The first stage is a wideband amplifier. The input matching network is designed to deliver power to the first common-source stage from 2 GHz to 6 GHz. The second stage is a cascode with an LC tank as a load. The common-source stage of the cascode is made of several transistors in parallel which can be turned on or off to control the gain of the LNA. The LC tank at the output of the cascode is used to tune the frequency response and give the amplifier a band-pass characteristic. The tank is adjustable using several varactors and a spiral inductor with many taps as shown in Figure 2.5. Each tap of the spiral has an associated MOSFET switch. When the switch is on, the outer rings of the spiral are shorted out effectively lowering the inductance value.

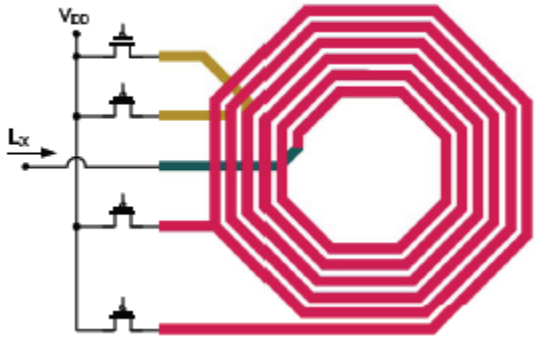


Figure 2.5 - Spiral inductor with many taps [9]

2.3.3 Common-Gate

Common-gate amplifiers are another useful amplifier topology. Both their gain and input match are wide-band into RF. The gate-source parasitic capacitance that plagues the common-source and common-drain topologies has a much smaller effect on circuit performance in the common-gate. At frequencies of interest for RF amplifiers, the zeroth order input impedance is the inverse of the transistor's transconductance.

A wide-band match is implemented by setting the transconductance, g_m, to the inverse of the source impedance. The drawback is that noise figure is inversely proportional to the transconductance. To maintain a good input match there is a limit on increasing the transconductance. The voltage gain of the common-gate can be large if the load is a large impedance such as a high input impedance buffer.

Liscidini et al. have taken advantage of the wide-band properties of the common-gate topology, but have improved the design through the use of two feedback networks as depicted in Figure 2.6 [11].

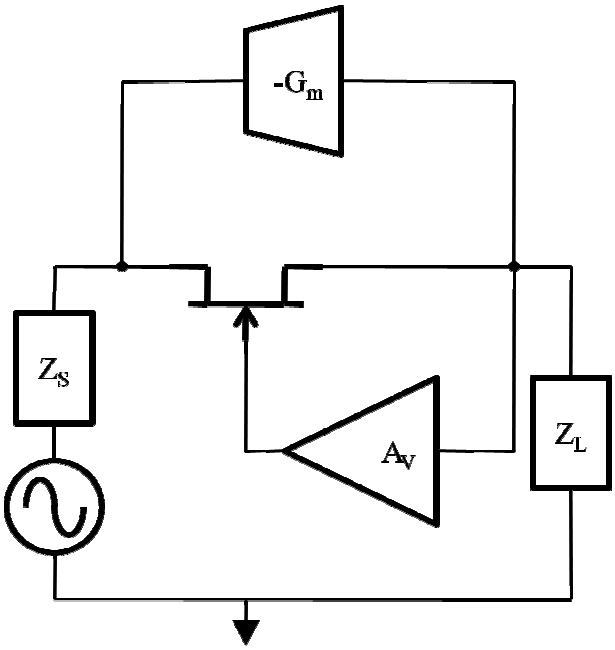


Figure 2.6 - Common-gate LNA with two types of feedback

The two feedback paths allow the transconductance of the main common-gate stage to increase while maintaining the wide-band input match. Assuming noiseless feedback, the noise figure is reduced because the FET transconductance can be increased while the circuit still provides a good match to Z_S. Simulation shows that the noise from the feedback is low enough that the LNA noise figure is indeed reduced.

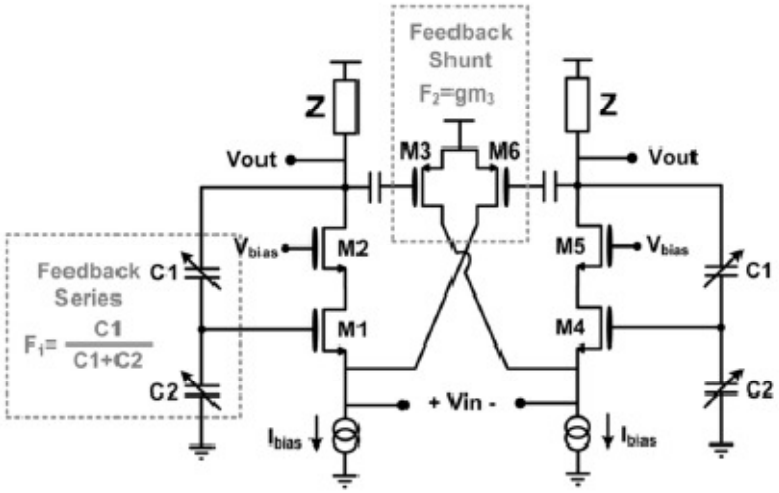


Figure 2.7 - Common-gate LNA with dual feedback [11]

A simplified circuit schematic simulated by Liscidini et al. is shown in Figure 2.7. The circuit is implemented in a differential form. Capacitors C_1 and C_2 on each side form the voltage feedback of Figure 2.6 and transistors M_3 and M_6 form the transconductance feedback. Table 2.1 contains the results of the simulations. By adjusting the feedback, the authors were able to reconfigure the LNA to operate in various modes depending on system requirements. For example, in "High IIP3 Mode," by increasing the power consumption, they were able to greatly improve the linearity and noise figure.

Table 2.1 - Common-gate LNA performance [11]

	Low Power Mode	High IIP3 Mode	High Gain Mode
DC Power (mW)	4	8	8
Noise figure (dB)	3.4	2.2	2.2
IIP3 (dBm)	5	16	3
Gain (dB)	20	20	26

Unfortunately, there is no configurable control over the frequency response of the amplifier.

2.3.4 Synchronous Filters

The source degenerated cascode is the state-of-the-art LNA topology. But like any receiver, interference from nearby transmitters can couple into the receiver chain. The transmitter signals are strong and can act as potential blocking signals which can result in gain compression of the LNA. In order to block these strong interferers from nearby transmitters, Vladimir Aparin suggests using a synchronous filter in a feedback loop around the LNA to cancel out any unwanted signals. The synchronous filter itself is a band-pass filter but when placed in the feedback loop it changes the overall amplifier into a band-stop filter capable of removing a narrow-band of strong interferers [12]. The block diagram of the circuit is shown in Figure 2.8.

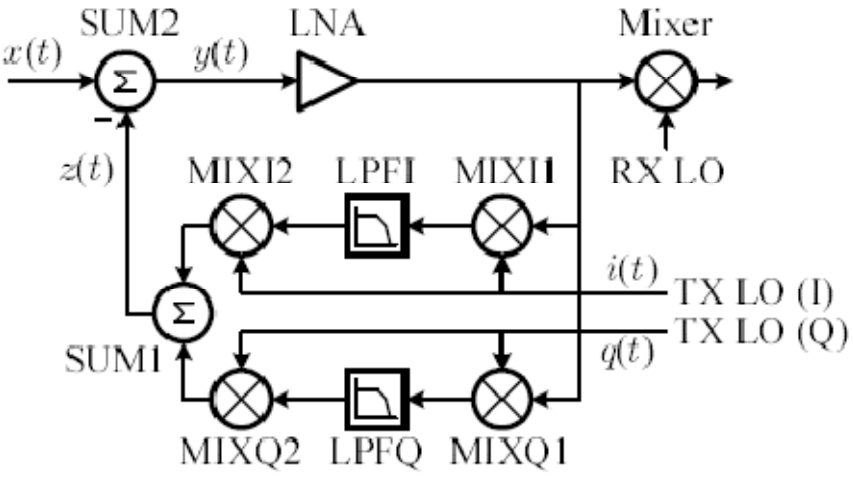


Figure 2.8 - Synchronous filter in feedback [12]

CHAPTER 3

RECONFIGURABLE COMMON-GATE LNA AND SYNCHRONOUS FILTER LNA

Two new LNA topologies are studied in this chapter. The first design is based around a common-gate amplifier with active negative feedback to give a band-pass response. The second LNA uses a synchronous filter and two feedback loops to create a band-pass LNA. In the end, neither of these designs were completed and therefore never fabricated.

3.1 Reconfigurable Common-Gate Low-Noise Amplifiers

The common-gate amplifier topology is shown in Figure 3.1. The ideal lumped element inductors and capacitors are infinite and used to provide bias that does not influence the frequency performance of the circuit. In a practical circuit, the voltage source biasing the gate could be replaced with a current mirror or a resistive voltage divider.

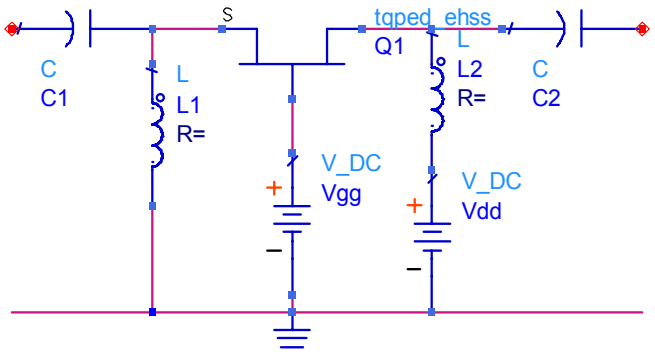


Figure 3.1 - Common-gate amplifier

The common-gate is most often used as a transimpedance amplifier. The input is a current and the output is a voltage. The current gain of the device is less than unity but the voltage gain can be large and depends on the load of the stage. The input impedance is determined primarily by the transconductance of the device. For a small device, the output impedance is large.

A small signal model is shown in Figure 3.2. In the small signal model, only the most influential parasitic components remain to simplify hand calculations. First, the gate-source capacitance, C_{GS}, plays a pivotal role in the input impedance and gain. The parasitics in parallel with the current source, R_{DS} and C_{DS}, significantly determine the output impedance and isolation of the amplifier stage.

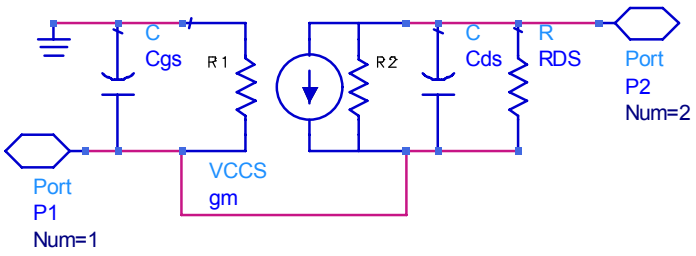


Figure 3.2 - Common-gate small signal model

Using the small signal model, the input admittance, where Z_L is the load of the common-gate stage, can be calculated to be

$$Y_{IN} = g_m + \frac{1}{R_{DS}} + s\left(C_{GS} + C_{DS}\right) - \frac{\left(\frac{1}{R_{DS}} + sC_{DS}\right)\left(\frac{1}{R_{DS}} + sC_{DS} + g_m\right)}{\frac{1}{Z_L} + \frac{1}{R_{DS}} + sC_{DS}} \quad (3.1)$$

.

At frequencies even several octaves past unity-gain frequency, ω_t, of the device, the fraction on the right half side is small compared to the remainder of the right half side. If

$$g_m >> \frac{1}{R_{DS}} \quad (3.2)$$

and

$$C_{GS} >> C_{GD} \quad (3.3)$$

the input admittance can be simplified and rewritten as

$$Y_{IN} = g_m + sC_{GS} \quad (3.4)$$

.

This is the same as if a conductance with value g_m were in parallel with a capacitor C_{GS}. Assuming that the ω_T is roughly the ratio of g_m to C_{GS}, equation (3.4) can be rewritten as

$$Y_{IN} = g_m\left(1+\frac{s}{\omega_T}\right). \tag{3.5}$$

At frequencies well below ω_T, the input admittance is approximately equal to the transconductance of the FET. Therefore, the input impedance is roughly

$$Z_{IN} = \frac{1}{g_m}. \tag{3.6}$$

The voltage gain of the circuit in Figure 3.2 is

$$A_V = \frac{1}{R_s}\frac{1}{\frac{\left(\frac{1}{Z_L}+\frac{1}{R_{DS}}+sC_{DS}\right)\left(\frac{1}{R_S}+sC_{GS}+g_m+\frac{1}{R_{DS}}+sC_{DS}\right)}{\left(g_m+\frac{1}{R_{DS}}+sC_{DS}\right)}-\left(\frac{1}{R_{DS}}+sC_{DS}\right)} \tag{3.7}$$

where R_S is defined as the source resistance.

Making the assumptions that

$$g_m >> \frac{1}{R_{DS}} \tag{3.8}$$

and

$$C_{GS} >> C_{GD} \tag{3.9}$$

the voltage gain is approximately

$$A_V = \frac{R_L g_m}{\left(1 + g_m R_S\right)\left(1 + \frac{sC_{GS}R_S}{1 + g_m R_S}\right)}. \tag{3.10}$$

Substituting ω_T for g_m/C_{GS} yields the dominant pole at

$$\omega_0 = \omega_T \frac{1 + g_m R_S}{g_m R_S}. \tag{3.11}$$

The output admittance is

$$Y_{OUT} = \frac{1}{R_{DS}} + sC_{DS} - \frac{\left(\frac{1}{R_{DS}} + sC_{DS}\right)\left(g_m + \frac{1}{R_{DS}} + sC_{DS}\right)}{\frac{1}{R_S} + \frac{1}{R_{DS}} + g_m + sC_{GS} + sC_{DS}}. \tag{3.12}$$

$$Y_{OUT} = \frac{1 + R_S sC_{GS} + R_{DS} sC_{DS} + R_{DS} R_S s^2 C_{DS} C_{GS}}{R_{DS} + R_S + g_m R_{DS} R_S + R_{DS} R_S s\left(C_{GS} + C_{DS}\right)}. \tag{3.13}$$

A dramatically simplified small signal model with a single noise source is shown in Figure 3.3. The single noise source is back-fit to a model based on physical measurements. The single source is a close approximation to a more detailed model which could potentially include a gate noise source and more noise sources for the small parasitic resistances at the gate, source, and drain which are not used in this small signal model.

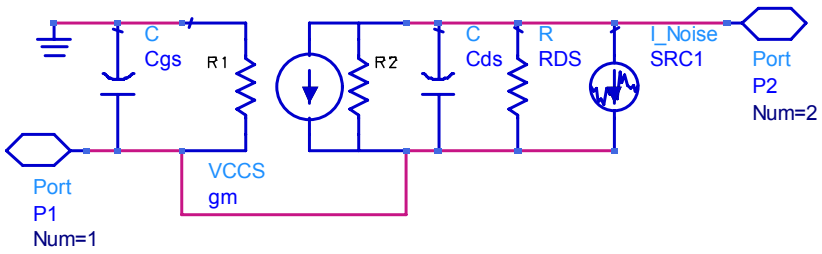


Figure 3.3 - Noise figure small signal model

Assuming

$$g_m >> \frac{1}{R_{DS}} \tag{3.14}$$

and

$$C_{GS} >> C_{GD} \tag{3.15}$$

The noise figure for the common-gate amplifier is

$$F = 1 + \frac{|I_{DN}|^2}{|V_N|^2} R_s{}^2 \frac{\frac{1}{R_S{}^2} + \omega^2 C_{GS}{}^2}{g_m{}^2 + \omega^2 C_{DS}{}^2} \tag{3.16}$$

where V_N is the noise from the noisy generator source and R_S is the source impedance. Substituting for V_N yields

$$F = 1 + \frac{|I_{DN}|^2}{4\kappa T \Delta f} R_s \frac{\frac{1}{R_S{}^2} + \omega^2 C_{GS}{}^2}{g_m{}^2 + \omega^2 C_{DS}{}^2} . \tag{3.17}$$

The input impedance, output impedance, voltage gain, and noise figure of the common-gate amplifier are summarized below in Table 3.1.

Table 3.1 - Common-gate amplifier parameters

Input Impedance	Output Admittance
$Z_{IN} = \frac{1}{g_m\left(1+\frac{s}{\omega_T}\right)}$	$Y_{OUT} = \frac{1 + R_S sC_{GS} + R_{DS} sC_{DS} + R_{DS} R_S s^2 C_{DS} C_{GS}}{R_{DS} + R_S + g_m R_{DS} R_S + R_{DS} R_S s\left(C_{GS} + C_{DS}\right)}$
Voltage Gain	Noise Figure
$A_V = \frac{R_L g_m}{\left(1+g_m R_S\right)\left(1+\frac{sC_{GS}R_S}{1+g_m R_S}\right)}$ $\omega_0 = \omega_T \frac{1+g_m R_S}{g_m R_S}$	$F = 1 + \frac{\left\|I_{DN}\right\|^2}{4\kappa T \Delta f} R_s \frac{\frac{1}{R_S{}^2} + \omega^2 C_{GS}{}^2}{g_m{}^2 + \omega^2 C_{DS}{}^2}$

3.1.1 Common-Gate Amplifier With Negative Feedback

Adding negative feedback is a useful circuit design technique that typically sacrifices gain to improve sensitivity. Although the common-gate has a current gain of less than unity, it can achieve a large voltage gain if the load impedance is large. Taking advantage of this, it is possible to add a negative feedback circuit around a common-gate amplifier. The feedback circuit shown in Figure 3.4 samples the voltage at the output of the common-gate amplifier and applies a current to the input of the common-gate stage.

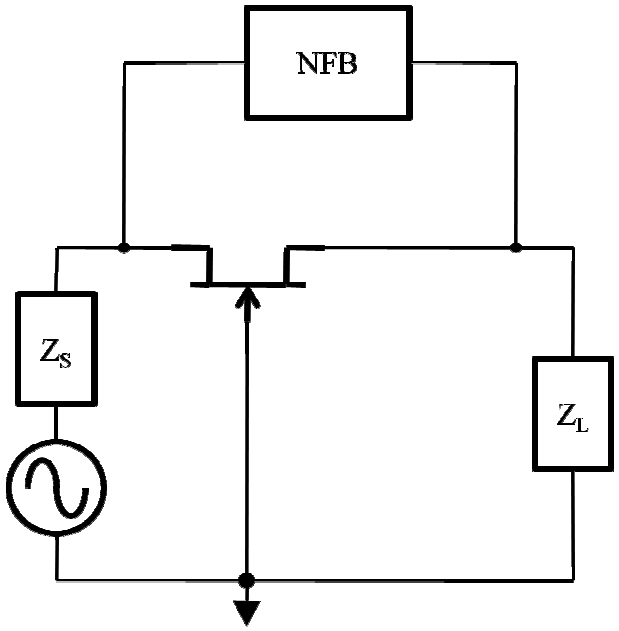


Figure 3.4 - Common gate amplifier with negative feedback

If the negative feedback block is band-stop in nature, the complete amplifier will demonstrate a band-pass response. The ideal negative feedback system is shown in Figure 3.5.

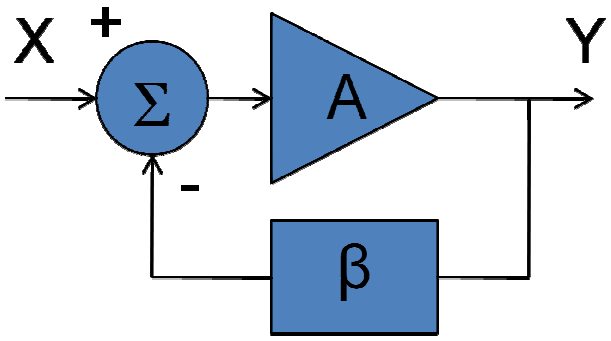


Figure 3.5 - Ideal negative feedback system

The transfer function is

$$H = \frac{Y}{X} = \frac{A}{1 + A\beta}. \tag{3.18}$$

If A is large, the function reduces to

$$H = \frac{1}{\beta}. \tag{3.19}$$

Possible magnitudes of the functions, A, β, and H as functions of frequency are shown in Figure 3.6.

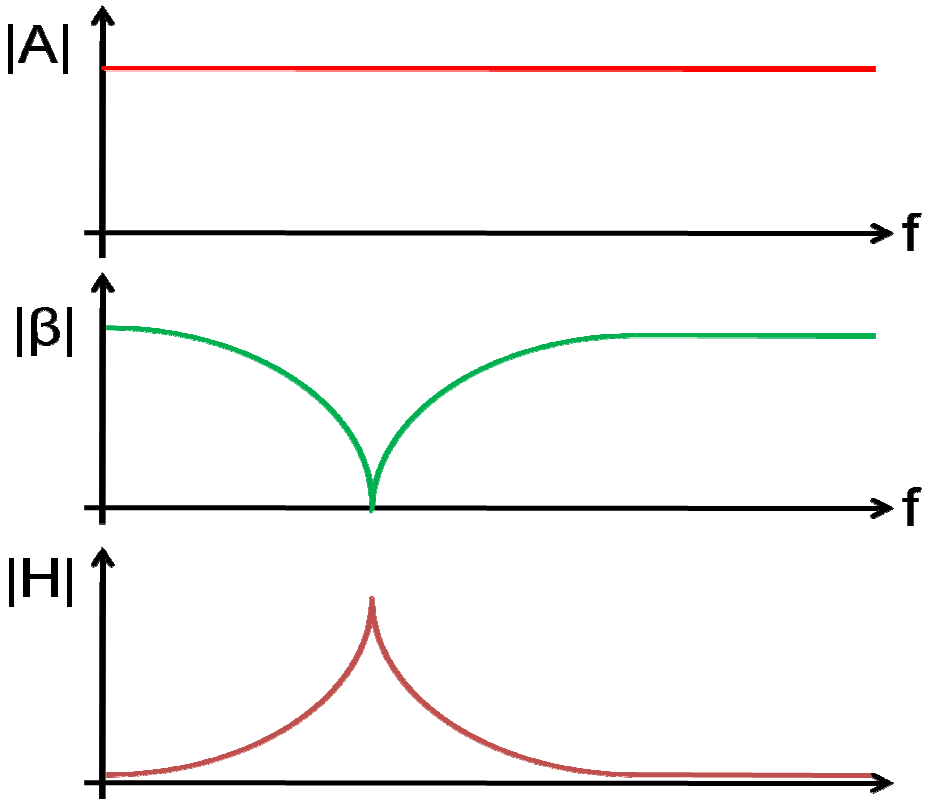


Figure 3.6 - Frequency response of negative feedback

Assuming A is large, the amplifier 'flips' the β function around creating a band-pass system.

With the open-loop common-gate stage, it is possible to bias the device such that it achieves a wide-band match. When a band-stop feedback circuit is added, the input match becomes narrow-band. Ideally, the narrowband input match would protect the FETs from strong out of band interferers. The input match and gain are determined by a single band-stop filter which is another advantage because it reduces the required number of reactive components. Reactive components take a large amount of die space and the fewer filters, the smaller the die.

3.1.2 Common-Gate Amplifier With Capacitive Feedback

An RF amplifier requires a good input match at the desired frequency of operation. Typically the source impedance is 50 Ω. The input impedance of a simple common-gate amplifier, at frequencies much lower than the unity gain frequency, is

$$Z_{IN} = \frac{1}{g_m}. \tag{3.20}$$

Therefore, for a good input match (Z_{IN}=Z_0=50 Ω)

$$g_m = \frac{1}{Z_{IN}} = \frac{1}{50} = 20mS. \tag{3.21}$$

The noise figure of the common-gate stage is

$$F = 1 + \frac{\left|I_{DN}\right|^2}{\left|V_N\right|^2} \frac{1 + \omega^2 C_{GS}{}^2 R_s{}^2}{g_m{}^2 + \omega^2 C_{DS}{}^2} \tag{3.22}$$

In a standard common-gate circuit there is a direct trade off between transconductance (and therefore gain) and input match. A good input match results in a non-optimum noise figure [10]. However, the addition of negative feedback [11] allows

the transconductance to be increased to improve noise figure but also provides a good input match. One way to implement this is through a capacitive divider as shown in Figure 3.7.

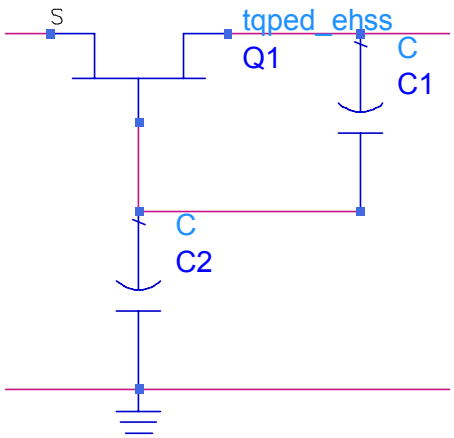


Figure 3.7 - Common-gate amplifier with capacitive feedback

With the feedback, the input impedance is

$$Z_{IN} = \frac{1}{g_m} + \frac{R_L sC_1}{R_L s^2 C_1 C_2 + s(C_1 + C_2)} = \frac{1}{g_m} + \frac{R_L C_1}{R_L sC_1 C_2 + C_1 + C_2}$$

$$Z_{IN} = \frac{1}{g_m}\left[1 + g_m R_L \frac{C_1}{C_1 + C_2}\frac{1}{\frac{R_S sC_1 C_2}{C_1 + C_2} + 1}\right] \qquad (3.23)$$

where R_L is the load impedance.

If C_1 and C_2 are small enough, their effects on the frequency response in equation (3.23 can be ignored and the equation can be simplified

$$Z_{IN} = \frac{1}{g_m} + R_L F$$

$$F = \frac{C_1}{C_1 + C_2} \qquad . \qquad (3.24)$$

The feedback increases the resistive portion of the input impedance. For instance, the g_m can be doubled, decreasing the noise figure, and the feedback will compensate for the increased transconductance and keep the input resistance large enough for a good match.

The feedback also adds a small capacitive component to the input impedance which at high frequencies can start to degrade the input match. To minimize this effect, C_2 should be chosen to be small. As C_2 decreases, C_1 must also decrease. The size of C_1 is limited, though, because C_1 is in effect in parallel with the parasitic gate-drain capacitance of the FET. One design approach is to use the parasitic drain-gate capacitor as C_1 and then determine the appropriate size of C_2 to obtain the required amount of negative feedback.

3.1.3 Common-Gate Amplifier With Cascode Feedback

The small signal schematic of the common-gate amplifier with cascode feedback is shown in Figure 3.8. The common-source stage of the cascode samples the output voltage of the main common-gate amplifier. The series inductor-capacitor circuit resonates at the chosen frequency short circuiting any signal to ground. When the LC circuit is resonating, the gate-source voltage of the common-gate in the feedback loop is zero and no current flows through the transistor. At frequencies far away from the resonant frequency, the LC circuit opens up and a voltage develops at the source of the common-gate device. A current flows through the transistor. The common-gate in the feedback essentially steals the current that would otherwise flow through the main common-gate amplifier.

The main advantage of putting the LC circuit in the feedback loop is that the LC circuit can control both the gain and input impedance. The noise contribution of Q_2 is minimized because at the resonance frequency of the LC circuit, the drain current noise of Q_2 is shorted to ground.

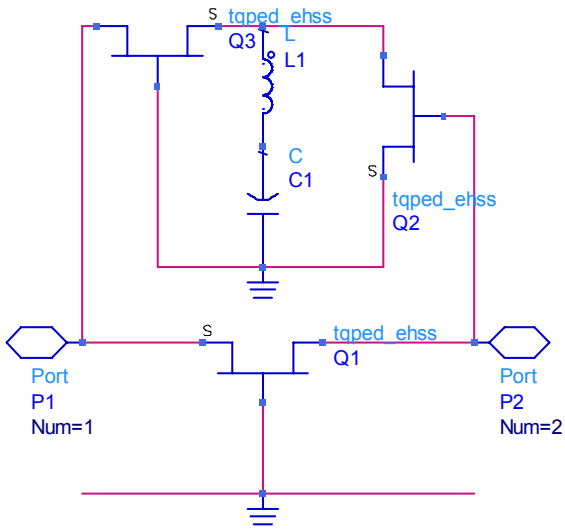


Figure 3.8 - Common-gate LNA with cascode feedback

The size of transistor Q_1 is chosen for optimal input match as will be discussed below. The size of transistor Q_2 is fundamental in determining the complete closed loop response of the amplifier. The small signal model is shown in Figure 3.9.

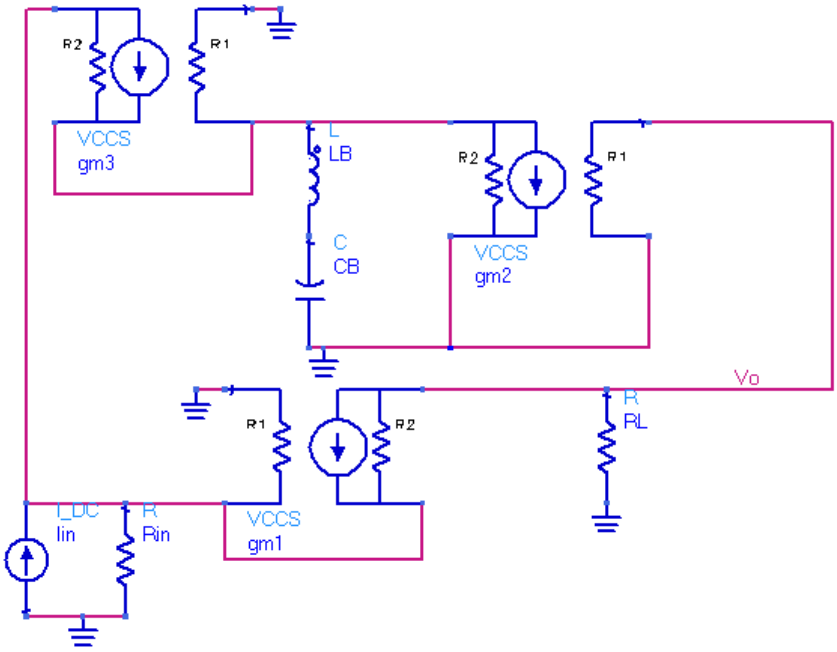


Figure 3.9 - Common gate with cascode feedback small signal model

The ratio of output voltage to input current without the feedback or reactive components is

$$H_{OPEN} = \frac{V_O}{I_{IN}} = \frac{g_{m1}R_L}{R_{IN}g_{m1}+1}R_{IN} \quad (3.25)$$

R_{IN} is the source impedance of a Norton source. Equation (3.25 is equivalent to the transfer function at the resonance frequency. With the feedback added, and at a frequency far away from the frequency at which the LC circuit resonates, the transfer function becomes

$$H_{CLOSED} = \frac{V_O}{I_{IN}} = \frac{\frac{g_{m1}R_L}{R_{IN}g_{m1}+1}R_{IN}}{1+g_{m1}R_L\frac{g_{m2}R_{IN}}{g_{m1}R_{IN}+1}}. \quad (3.26)$$

Taking the ratio of the transfer functions yields

$$\zeta = \frac{H_{OPEN}}{H_{CLOSED}} = 1 + g_{m1} R_L \frac{g_{m2} R_{IN}}{g_{m1} R_{IN} + 1} \quad (3.27)$$

Solving for g_{m2} yields

$$g_{m2} = \frac{(\zeta - 1)(g_{m1} R_{IN} + 1)}{g_{m1} R_L R_{IN}} \quad (3.28)$$

The significance of equation 3.28 is that assuming the source and load impedances are predetermined and g_{m1} is picked for a good input match, g_{m2} can be chosen for any arbitrary ζ. When the series LC circuit is added back to the feedback, the cascode ideally only affects the amplifier's behavior far from the resonance frequency. Therefore, ζ represents the out of band rejection the amplifier will display. The transconductance of Q_3 is not significant in determining out of band rejection. Its purpose is to act as a current buffer between the common-source stage and the input of the main-common gate amplifier. The goal of the feedback is to reduce the current at the node where the cascode feeds back into Q_1 and thus reduce the current into Q_1 generated by an out of band interferer.

To make the amplifier's frequency response reconfigurable, L_B and C_B can be replaced or supplemented by electronically adjustable reactive components such as active inductors or varactors.

The active feedback is not without penalty, though. The feedback can cause potential instabilities as well add noise to the circuit. Parasitic transistor capacitance, primarily the gate-source capacitance of Q_2, adds extra poles to the system which are capable of creating potential instabilities at frequencies just below the operating frequency.

The frequency response of the circuit's gain and input impedance are determined primarily by the gate-source capacitance of the common-source stage and the inductor and capacitor between the transistors of the cascode. Figure 3.10 is the small signal diagram.

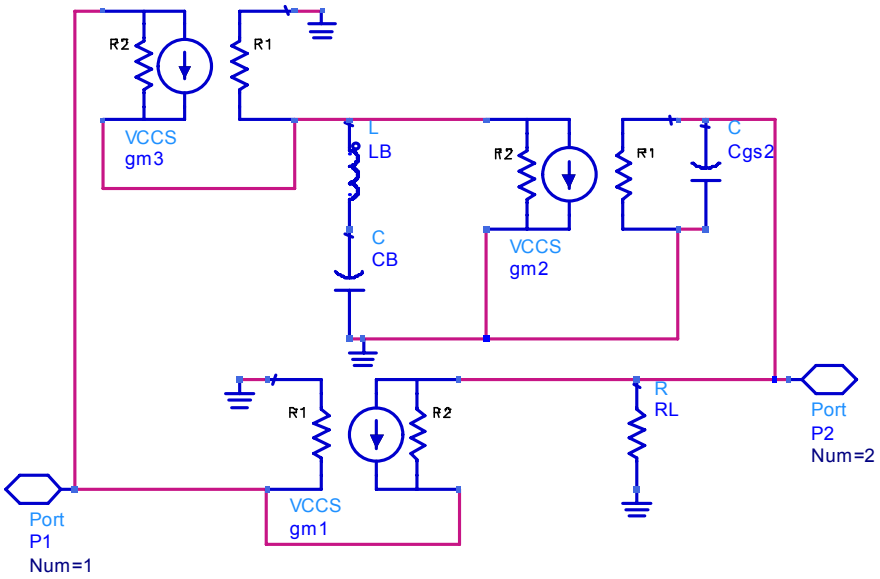


Figure 3.10 - Common-gate small signal model for gain and input impedance

The input impedance is

$$Z_{IN} = \frac{1}{g_{m1} + \dfrac{g_{m1}g_{m2}g_{m3}R_L}{g_{m3} + sC_{GS2}g_{m3}R_L + \dfrac{R_L sC_{GS2} + 1}{sL_B + \dfrac{1}{sC_B}}}}. \tag{3.29}$$

The derivation of equation 3.29 is found in Appendix 1. The equivalent circuit model with the same input impedance of the circuit of Figure 3.10 is shown in Figure 3.11 and each component value is summarized in Table 3.2.

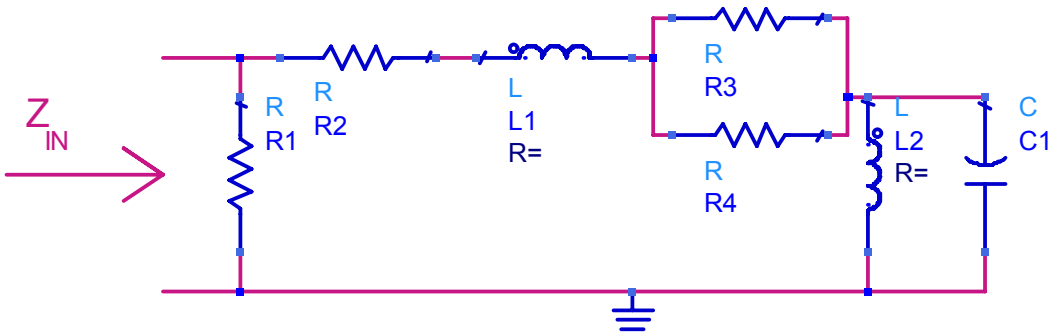


Figure 3.11 - Common gate equivalent input impedance of common-gate amplifier

Table 3.2 - Common gate equivalent input impedance parameters

$R_1 = \frac{1}{g_{m1}}$	$R_2 = \frac{1}{g_{m1}g_{m2}R_L}$	$R_3 = \frac{L_B g_{m1} g_{m2} g_{m3}}{C_{GS2}}$	$R_4 = -\frac{g_{m1} g_{m2} g_{m3}}{\omega^2 C_B C_{GS1}}$
$L_1 = \frac{C_{GS2}}{g_{m1}g_{m2}}$	$L_2 = \frac{C_B}{g_{m1}g_{m2}g_{m3}R_L}$	$C_1 = L_B g_{m1} g_{m2} g_{m3} R_L$	

Shunt resistor R_1 represents the input impedance of the main common-gate amplifier. The other leg of the equivalent circuit represents the feedback loop. Note that the negative feedback converts the gate-source capacitance into an inductance and the series LC tank is converted into a parallel LC tank. The inductor becomes the capacitor and vice versa. Ideally, the second branch would consist only of the parallel LC tank so that at the resonant frequency, the input impedance is only R_1.

A negative real part of the input impedance implies a potential instability in the circuit. Below the resonance frequency of L_2 and C_1, the negative resistance of R_4 can dominate the real part of the input impedance and in turn, cause the input resistance to be negative.

To remove the negative portion of the input resistance, another inductor can be placed in parallel with the gate-source capacitance as shown in Figure 3.12.

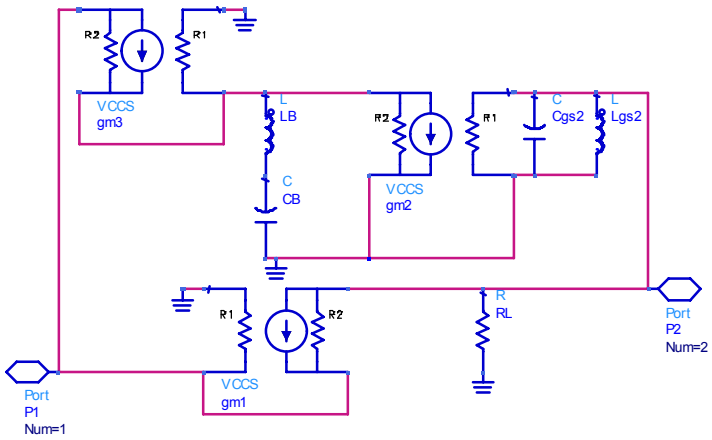


Figure 3.12 - Common-gate small signal diagram with second tank

As long as the resonance of L_{GS} and C_{GS} is close to that of L_B and C_B, the negative portions of the input impedance cancel each other out. The new input impedance, with no negative resistive part, is

$$Z_{IN} = \frac{1}{g_{m1} + g_{m1}g_{m2}g_{m3}\left(\frac{1}{R_L} + \frac{1}{sL_{GS}} + sC_{GS}\right)\dfrac{\dfrac{1}{g_{m3}}}{1 + \dfrac{1}{g_{m3}\left(sL_B + \dfrac{1}{sC_B}\right)}}}. \tag{3.30}$$

The small signal voltage gain of the circuit with the additional inductor in Figure 3.12 is

$$A_V = \frac{V_O}{V_{IN}} = \frac{g_{m1} R_L s L_{gs2} X}{(1 + g_{m1} R_S)\left(s^2 L_{gs2} C_{gs2} R_L + s L_{gs2} + R_L\right) X + W\left(s^2 L_B C_B + 1\right)}$$
$$X = s C_B + g_{m3}\left(s^2 L_B C_B + 1\right) \tag{3.31}$$
$$W = g_{m1} g_{m2} g_{m3} R_S L_{gs2} R_l$$

If $(L \cdot C)^{-1} = \omega_0^2$ and $(L_{gs2} \cdot C_{gs2})^{-1} = \omega_0^2$, then the voltage gain when $\omega = \omega_0$ reduces to

$$A_V = \frac{g_{m1} R_L}{g_{m1} R_S + 1} \tag{3.32}$$

This is the same gain equation as if there were no feedback at all which is the goal of adding the feedback. In the band of operation, the feedback is supposed to be 'invisible' to the main amplifier. But at frequencies far away from the band of operation, the feedback should lower the gain and degrade the input match. The overall effect is a narrow-band amplifier.

If the LNA requires both good input match and good noise figure, a standalone common-gate amplifier would typically fail one of the requirements. Adding the capacitive feedback allows g_m to be increased while maintaining the good input match. The increased g_m yields lower noise figure. Adding the cascode feedback adds a narrow-band match and gain.

3.1.4 Example Design

The first step in designing a common-gate LNA with two types of negative feedback is to pick the ratio, ζ, of transimpedance transfer function in band versus out of band. For this circuit, ζ was chosen to be 30.

$$g_{m2} = \frac{(\zeta - 1)(g_{m1} R_{IN} + 1)}{g_{m1} R_L R_{IN}} \quad (3.33)$$

Using equation (3.33 and choosing the load resistance to be 500 Ω and the source resistance to be 50 Ω, the transconductance of the common-source transistor is calculated to be 115 mS. To decrease the noise figure, capacitive feedback is added to the main common-gate FET. The drain-gate capacitor is used as one of the capacitors in the divider feedback.

The circuit is designed to operate at 3.6 GHz. The frequency response is determined primarily by the two LC circuits. The first tank is composed of three components: the gate-source capacitance of the common-source stage, feedback capacitance of the main common-gate amplifier, and an additional inductor. More capacitance could be added but is unnecessary. The inductor is designed to resonate with the capacitance at 3.6 GHz. The inductor winds up being 2.7 nH. The second tank can be used to control the bandwidth of the gain. The smaller the inductor is, the wider the bandwidth is. For this example, the inductor was chosen to be 1 nH and the required capacitance is 2 pF.

If the common-gate stage in the feedback cascode is too small, the gain suffers. If it is too large, the noise figure suffers because the noise from the channel can flow into the source of the main common-gate amplifier. For this design, the common-gate stage has a transconductance of 5 mS.

For this example, each transistor is biased separately using ideal DC batteries. All but one of the passive components to bias the circuit are ideal RF chokes and DC blocks. The only non-ideal RF choke is the gate bias inductor for the common-source amplifier.

To save space, the component, which is normally a large resistor, is instead the inductor that resonates with the gate-source capacitance. The transistor models are realistic 0.5 µm pHEMT models. The feedback transistors have to be biased hotter than the core common-gate transistor in order to improve the linearity. The cascode feedback potentially sees larger power signals and needs a larger bias in order to keep the RF gate-source voltages from changing the operating regimes of the transistors. The feedback transistors also create intermodulation powers which are fed back to the main amplifier.

A full schematic of the simulated circuit is shown in Figure 3.13. Simulation results for gain, input match, output match, noise figure, IIP3, OIP3 and P1dB follow and are summarized in Table 3.3.

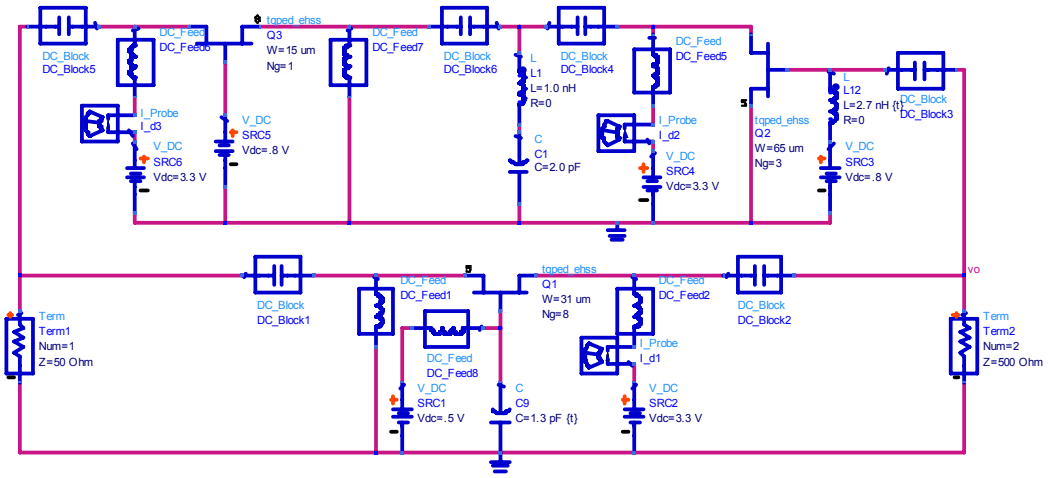


Figure 3.13 - Common-gate with both capacitive and cascode feedback

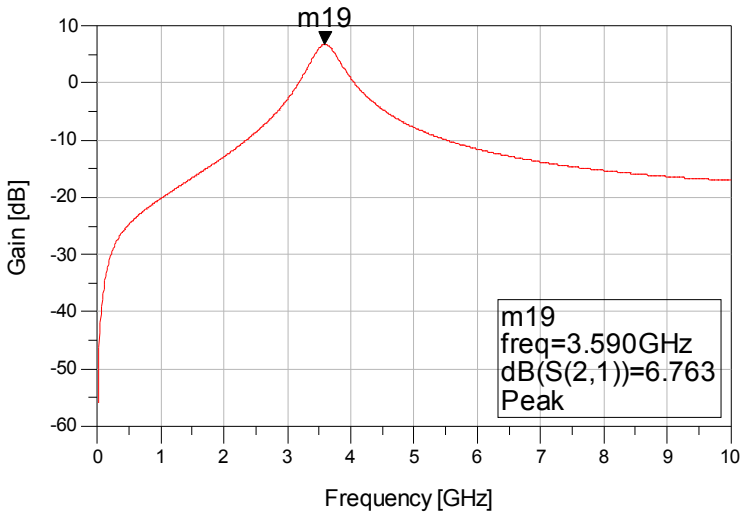


Figure 3.14 - Gain of common-gate with cascode

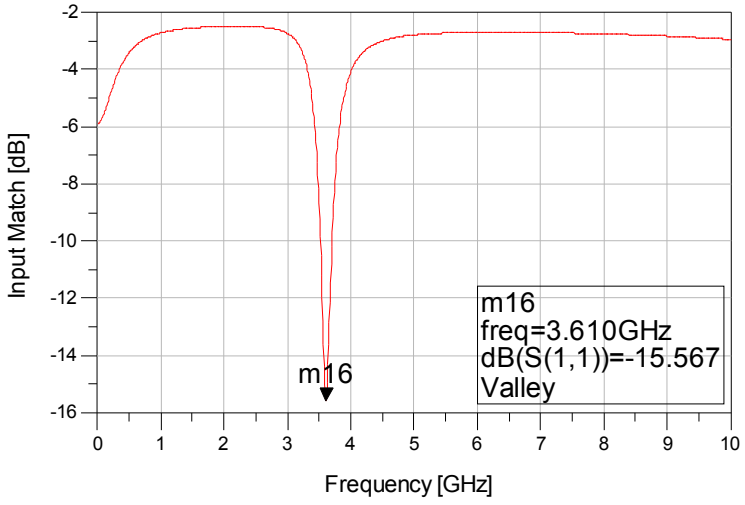


Figure 3.15 - Input match of common-gate with cascode

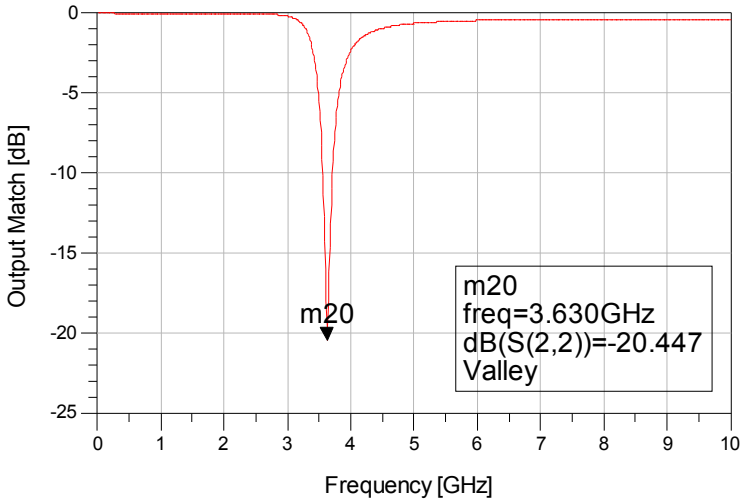


Figure 3.16 - Output match of common-gate with cascode

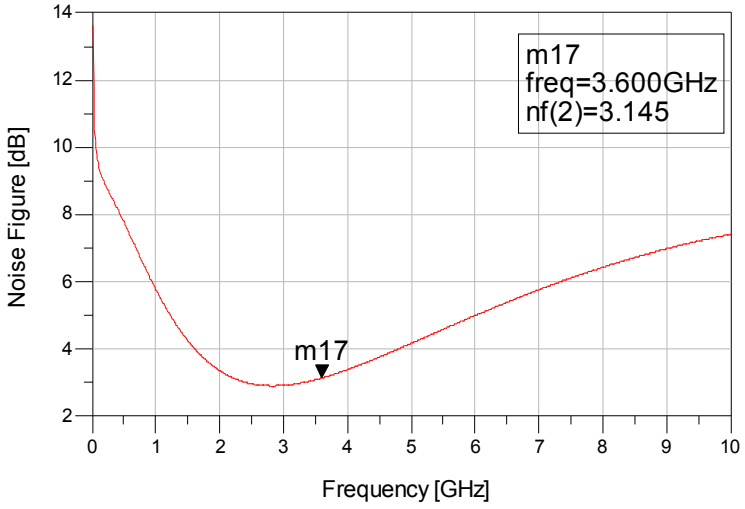


Figure 3.17 - Noise figure of common-gate with cascode

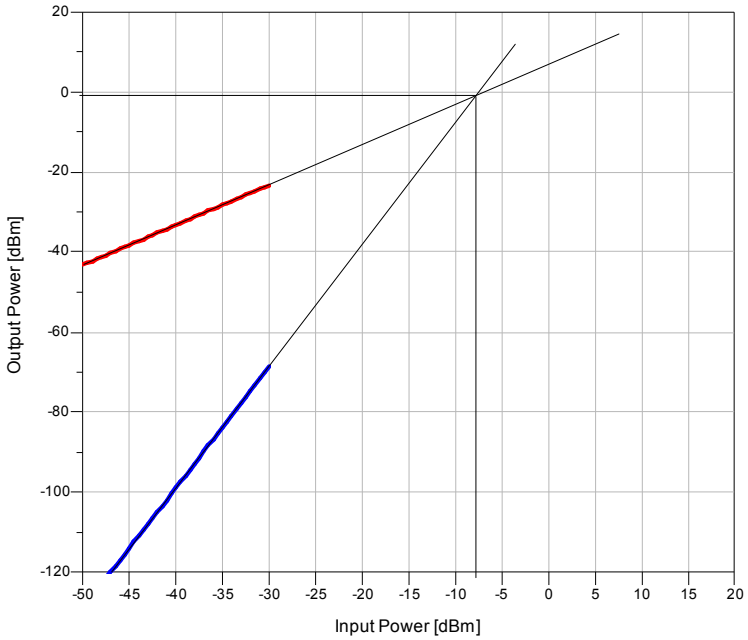


Figure 3.18 - Intermodulation distortion of common-gate with cascode (f_1 = 3.595 GHz & f_2 = 3.605 GHz)

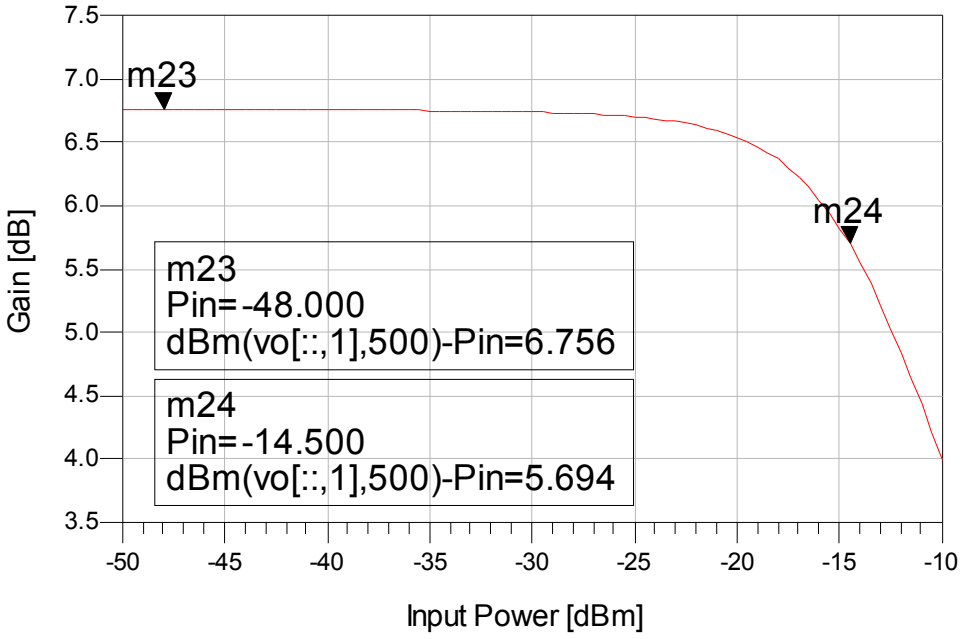


Figure 3.19 - Gain compression of common-gate with cascode

Table 3.3 - Results of common gate with cascode

Gain [dB]	Input Match [dB]	Output Match [dB]	Noise Figure [dB]	IIP3 [dBm]	OIP3 [dBm]	Input P1dB [dBm]	I_{DC}
6.7	15.6	20.5	3.1	-7.8	-1.2	-14.5	43 mA

The advantage of the common-gate LNA with cascode feedback versus a common-gate LNA without feedback is the addition of a narrow-band input match and narrow-band gain. The narrow-band input match potentially protects the LNA from strong out of band interferers. Figure 3.20 are the simulation results of an experiment

with a similar setup to that of an IM3 measurement. The figure plots output power versus input power and compares three cases of the common-gate amplifier of Figure 3.13: (i) the full common-gate amplifier with cascode feedback made with realistic FET models, (ii) the feedback completely removed, and (iii) the feedback replaced with linear lumped element components. The circuit is designed to operate at 3.6 GHz so the out-of-band interferers are placed at 2.4 GHz and 3.0 GHz so that the upper third order intermodulation product falls at 3.6 GHz. In the graph, the larger output powers are at 3 GHz and the smaller output powers are the 3.6 GHz intermodulation output powers. The intermodulation powers for both the stand-alone common-gate amplifier and common-gate with realistic feedback are similar. With linear feedback, though, the value of the narrow-band input match is recognized. The intermodulation powers are around 10 dB weaker.

The output powers for amplifiers with feedback are lower than the output powers for the simple common-gate because the feedback adds a narrow-band response to the gain and the fundamental input tone is out of this band.

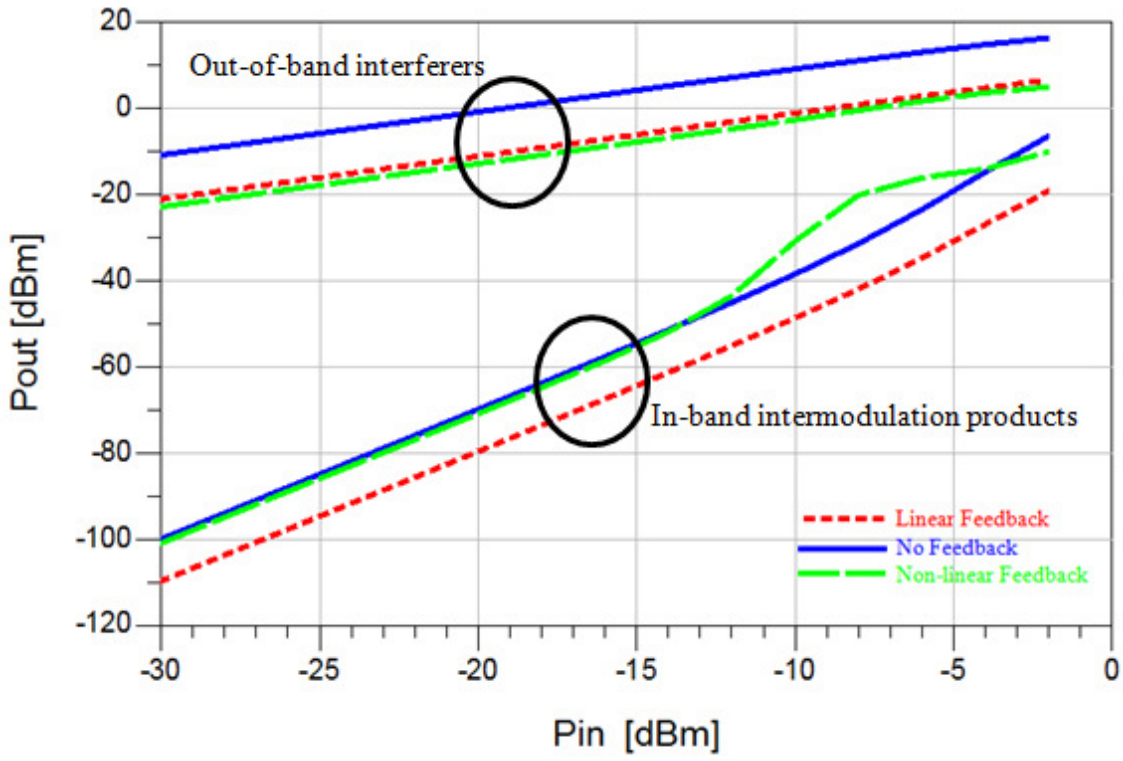


Figure 3.20 - Fundamental and intermodulation output powers for three common-gate amplifiers

When the feedback is realistic and non-linear, the feedback might add no protection from strong out-of-band interferers because the feedback adds its own significant distortion. For the design example, the feedback added as much distortion as it removed. If the non-linear effects of the feedback are minimized, the feedback shows some advantage.

Another advantage of the feedback is that the narrow-band gain provides some rejection at frequencies other than the operating frequency. The rejection helps protect other non-linear circuit elements further down the receive chain including mixers and demodulators.

In the end, though, the issues outweighed the advantages. The major problem with implementing a reconfigurable version of the circuit is the potential instability caused by the gate-source capacitance of the common-source stage in the feedback. The easiest fix (the inductor mentioned above) works well for one frequency, but to make the amplifier reconfigurable, the inductor would have to be reconfigurable. Each reconfigurable circuit element can be physically large as well as noisy or non-linear. Another attempted solution to fix the potential instability was to add a negative capacitance circuit. The negative capacitance circuit was too noisy and had a very limited bandwidth and quality factor.

3.2 Synchronous Filter Low-Noise Amplifiers

Synchronous filters work by down-converting RF signals to either baseband or IF, filtering at the lower frequency, then up-converting back to the original RF band. The final circuit is then a band-pass filter. The first advantage of the synchronous filter is that the center frequency of the entire filter is controlled by the down-conversion frequency. This frequency can be changed and the entire filter response changes. Another benefit is that the pass-band characteristics of the entire filter are controlled by whatever filter (usually low-pass) is placed between the up and down-conversion mixers. The simplest synchronous filter is shown in Figure 3.21.

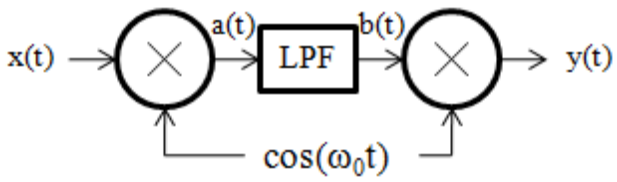


Figure 3.21 - Synchronous filter block diagram

To understand the operation of the filter, examine each signal *x(t)*, *a(t)*, *b(t)*, and *y(t)* in the frequency domain. In Figure 3.22, the top graph is an example input spectrum *X(f)*. The input spectrum has two RF signals – a square and a triangle. In the second plot *x(t)* has been multiplied by the signal $cos(\omega_0 t)$. Then, the signal is low-pass filtered so that only the baseband portion remains. The baseband signal is the desired portion of the original RF signal. Then, in the last graph, the baseband signal is up-converted back to its original RF spectrum with the second mixer.

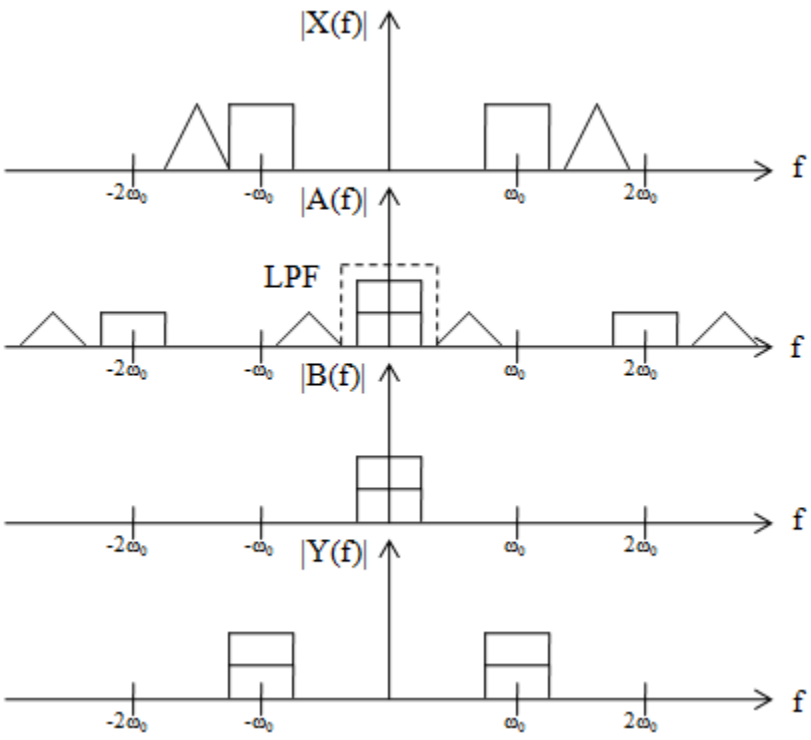


Figure 3.22 - Principle of operation for synchronous filter

The system shown in Figure 3.22 is flawed, though. The key weakness of this zero-IF receiver is that any information in signal phase can be lost when the original down-converted signals add together at baseband. This can be overcome by using a low-IF and filtering at IF but this requires a band-pass filter be built instead of a low-pass filter and additional high-pass filter is needed at the output to remove a newly formed image signal. Instead, an IQ system can be used as shown in Figure 3.23.

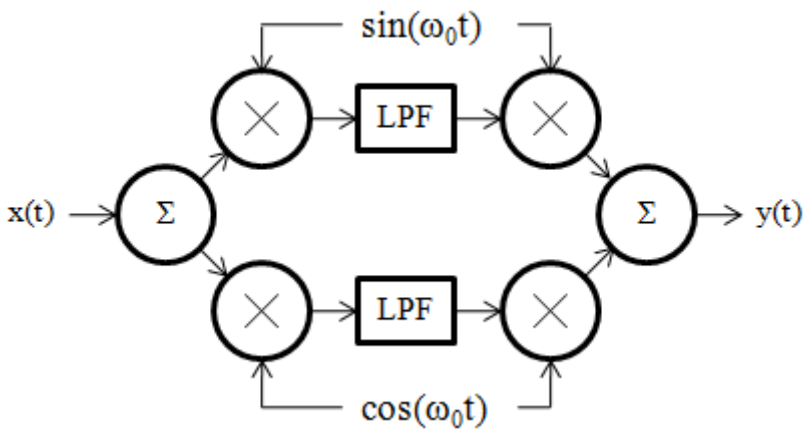


Figure 3.23 - In-phase quadrature synchronous filter

The IQ system preserves the modulation of the incoming signal and allows the system to use low-pass filters. The system, as is, would have trouble acting as a standalone LNA, though. The first circuit the antenna sees in a receiver is rarely a mixer – mixers are typically too noisy and do not have enough gain. Instead, the synchronous filter can be used similar to the feedback used with the common-gate amplifier as demonstrated in section 3.1.3. To make a band-pass LNA, the feedback filter has to be band-stop in nature. Unfortunately for the synchronous filter, the low-pass filters cannot simply be replaced with high-pass filters to switch the synchronous filter from band-pass to band-stop. Instead, though, a novel system can be designed taking a circuit like that discussed in section 2.3.4 where a synchronous filter, with internal low-pass filters, in a negative feedback loop around an amplifier is constructed to establish a band-stop filter. This filter is then used in another negative feedback loop of the main amplifier. In effect, the overall system is band-pass in nature. A block diagram of such a system is shown in Figure 3.24.

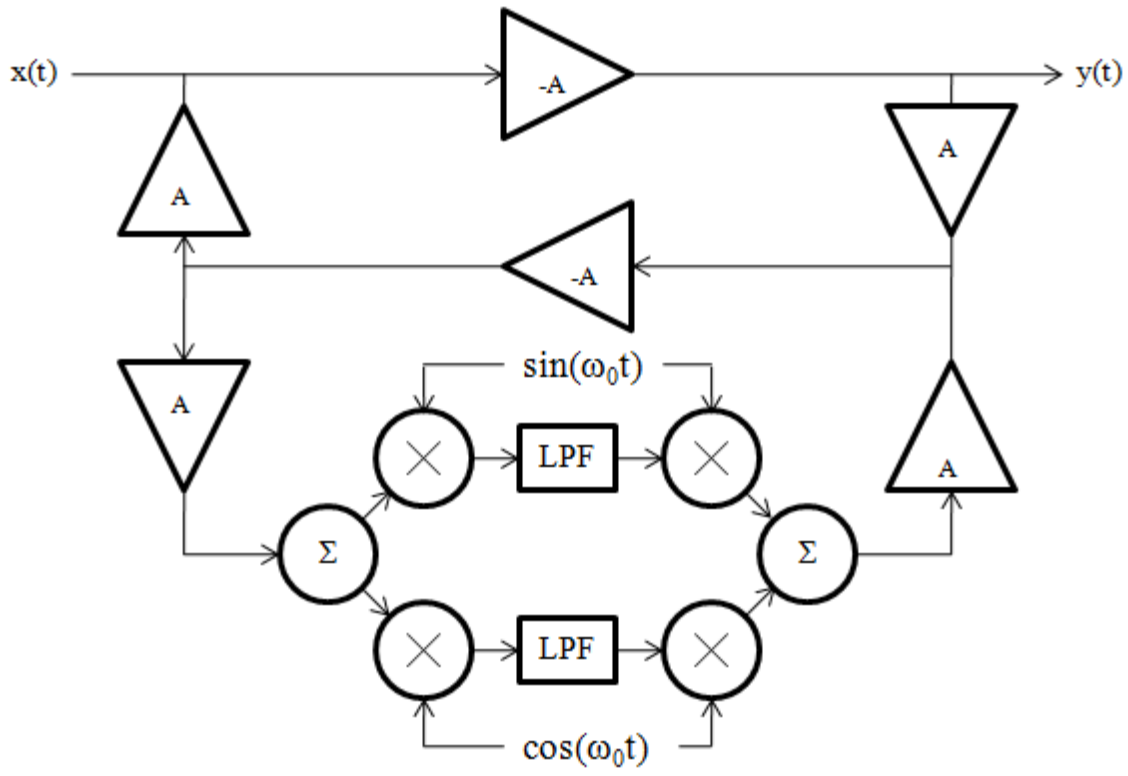


Figure 3.24 - Full LNA with embedded feedback

The system as shown in Figure 3.24 is not optimized for fewest components but drawn for the simplest explanation. Several of the amplifiers are only necessary as buffers to ensure the signal flows in the correct direction. The main amplifier could also be a common-gate. The common-gate is favorable because it has wide-band characteristics. The feedback-loop adds a band-pass characteristic to amplifier.

Figure 3.25 contains the results of a schematic simulation of the circuit in Figure 3.24 implemented in ADS. The amplifiers are ideal voltage-controlled-voltage-sources and the mixers are ideal multipliers. The low-pass filters are first order low pass filters. There are two LO frequencies (1.5 GHz and 2.5 GHz) and two low-pass filters (50 MHz and 100 MHz -3 dB cutoff).

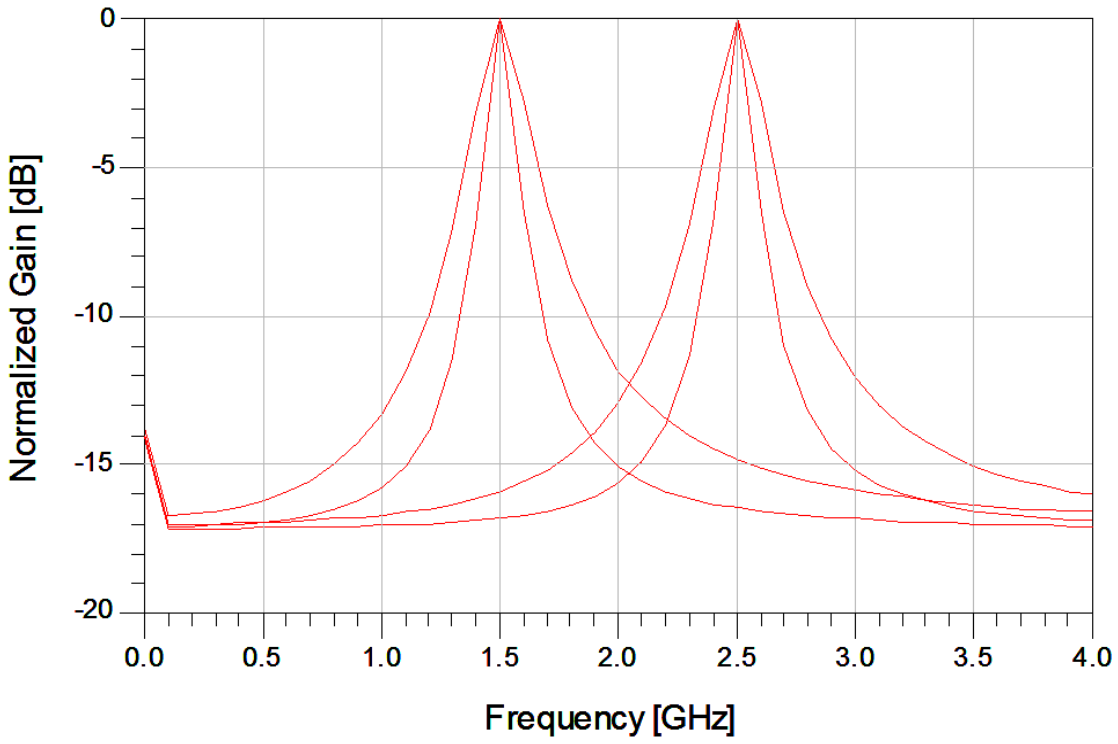


Figure 3.25 - Normalized transfer function of embedded synchronous filter

The advantage of this circuit is that by changing the LO frequency of the mixers, the center frequency of the overall amplifier correspondingly shifts. The disadvantages are clear, though. For one, the circuit requires many amplifiers – all of which consume DC power. And to keep the out of band rejection up the gain of the amplifiers must be large. Anytime there is large gain, linearity becomes a concern. Another drawback is that the circuit has many components so its physical size would be large. Finally, any system with this much active feedback can suffer from instabilities. Everything must be meticulously checked so that the Barkhausen Criterion is never met in order to keep the circuit from oscillating. A full analysis of the stability of the circuit in Figure 3.24 is beyond the scope of this thesis. Instead, the remainder of the thesis will be focused on the switchable cascode circuit.

CHAPTER 4

RECONFIGURABLE CASCODE LOW-NOISE AMPLIFIERS

The source degenerated cascode amplifier is the state of the art choice of topology at RF frequencies for low-noise amplifier design. The cascode demonstrates low noise, high gain, good input match, good linearity and low power consumption. The circuit diagram, with output buffer and without bias networks, is shown Figure 4.1. One disadvantage of the cascode is a large output impedance because of the common-gate stage. A buffer is sometimes required to be able to drive a 50 Ω load.

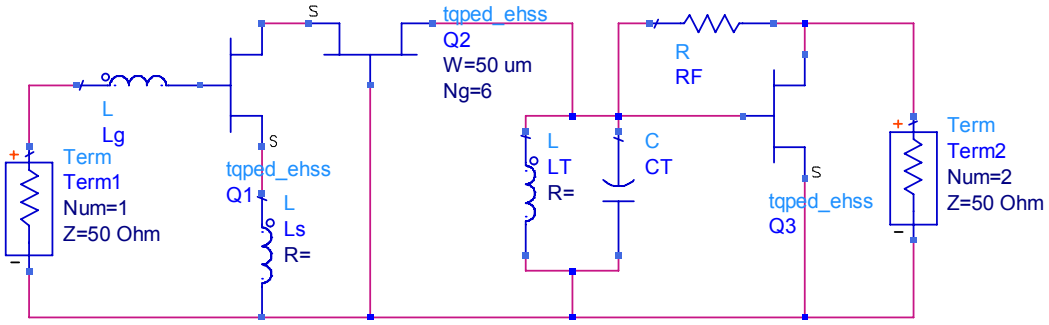


Figure 4.1 - Cascode LNA with output buffer

The common-source amplifier suffers from the Miller-Effect. With a large voltage gain, the effect of the gate-drain capacitance is greatly increased which severely limits the high-frequency gain of the amplifier. With a smaller voltage gain, the Miller-Effect is decreased. The common-gate stage has a low input impedance and when added after the common-source, lowers the voltage gain of the common-source stage. The common-gate stage is a current buffer but capable of a large voltage gain. By cascading the stages the two stages, the cascode has a large power gain.

4.1 Input Impedance

The input impedance determines the input match of the LNA. The input match describes how much power available from the source is delivered to the circuit. For narrow-band LNAs, a narrow-band input match is helpful. Since the input matching network helps reject out of band signals, any out of band interferes will have a more difficult time reaching the first gain stage. Strong interferes are one of the primary culprits responsible for gain compression. By rejecting them, the input matching network helps keep the LNA linear.

The input impedance of the cascode LNA can be roughly found using only a first order model for the cascode. As shown in Figure 4.2, the components that primarily determine the input impedance are the gate inductance, L_G, the gate-source parasitic capacitance, C_{GS}, the source degeneration inductor, L_S, and the transconductance, g_m. The common-gate stage does not play a pivotal role in determine the input impedance. The input impedance of a common-gate amplifier is the inverse of the transconductance. For devices with large transconductance, the input impedance becomes small and the common-gate device can be replaced with a short circuit.

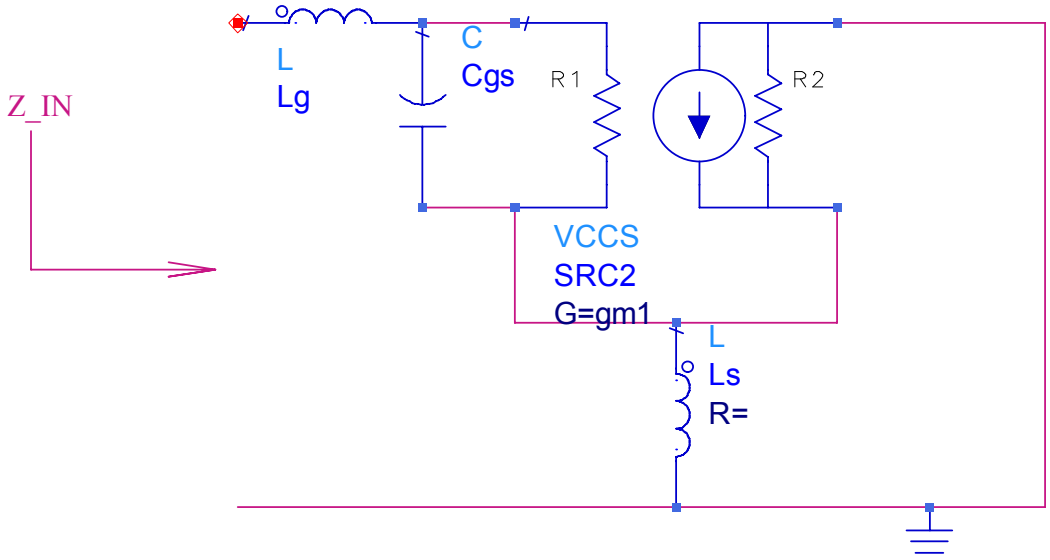


Figure 4.2 - Small signal model for calculating cascode input impedance

The input impedance is then

$$Z_{IN} = s(L_S + L_G) + \frac{1}{sC_{GS}} + \frac{g_m L_S}{C_{GS}} \quad (4.1)$$

The circuit components can be chosen so that the real part of Z_{IN} is equal to the source impedance Z_0, typically 50 Ω, and L_G is then used with L_S and C_{GS} to resonate out the imaginary impedance at the desired frequency of operation. The inductors can be picked using

$$L_S = \frac{Z_0 C_{GS}}{g_m} \quad (4.2)$$

and

$$L_G = \frac{1}{\omega_0^{\,2} C_{GS}} - \frac{Z_o C_{GS}}{g_m} \quad (4.3)$$

4.2 Gain

The gain of the cascode is predominantly determined by the transconductance of common-source transistor of the cascode and to some extent the transconductance of the output buffer. The frequency response is dominated by the input gate inductor, gate-source capacitance of the common-source cascode transistor, the source inductor, and the LC tank between the cascode and the buffer. A small signal model with these components is shown in Figure 4.3.

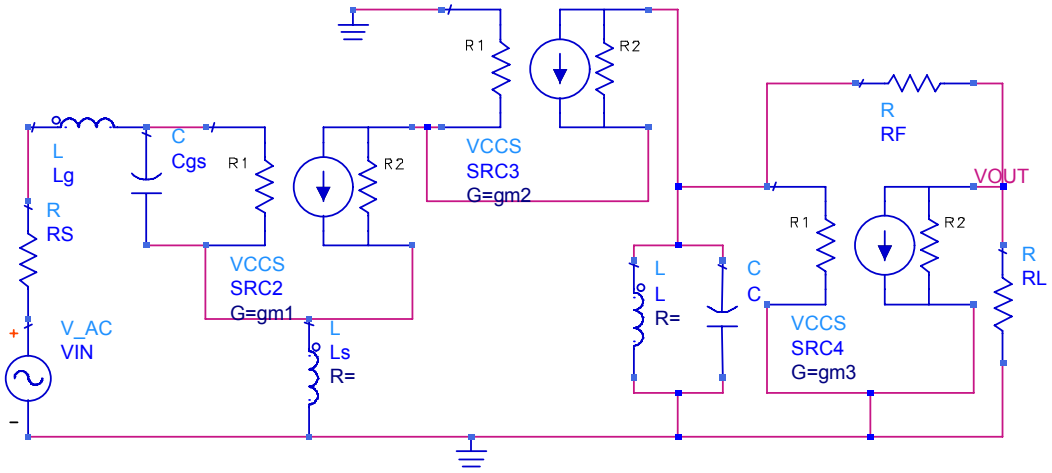


Figure 4.3 - Cascode and output buffer small signal model

The transfer function of the circuit is

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{m1}}{1 + sL_S(sC_{GS} + g_{m1}) + sC_{GS}(R_S + sL_G)} \cdot \frac{sLR_L(1 - g_{m3}R_F)}{s^2 LC(R_F + R_L) + sL(1 + g_{m3}R_L) + (R_F + R_L)} \quad (4.4)$$

The transfer function, when written as is, can be easily broken down into the recognizable parts of the circuit. The left half fraction has the transconductance g_{m1} which converts the input voltage into a current. The denominator is a second order low pass filter constructed from the gate-source capacitance, C_{GS}, and the two inductors which are used to set up the input match, L_G & L_S. The right side fraction contains the information about the output buffer and LC tank. The LC tank converts the output current of the cascode into a voltage that the output buffer then uses to convert back to a voltage across the load impedance.

In the cascode architecture, in terms of the gain, the transconductance of the common-gate transistor is not significantly important. Its primary role is to reduce the impedance seen by the common-source FET of the cascode. This effectively reduces the Miller Effect because the voltage gain of the first stage is very low. The common-gate acts as a current buffer but can contribute significantly to voltage gain, especially when the load of the cascode is a large impedance (such as a high Q tank and the gate of a small transistor in the common-source configuration).

4.3 Output Impedance

The output impedance is mostly a function of the RLC tank that is used to tailor the frequency response of the gain, the feedback resistor of the output buffer, and the buffer transconductance of the buffer FET. The resistance of the RLC tank represents the finite Q of the inductor and capacitor of the tank. If the buffer FET is small enough, the parasitics do not play a large role in determining the output impedance. A small signal model to determine the output impedance is shown in Figure 4.4.

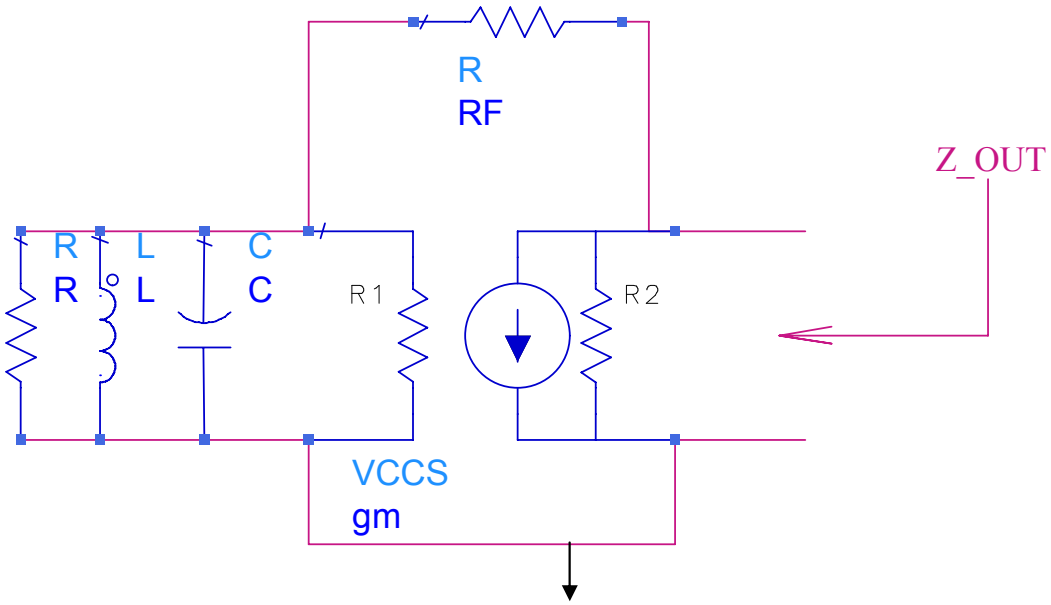


Figure 4.4 - Small signal model of output buffer for output impedance

The output admittance is determined to be

$$Y_{OUT} = \frac{1}{R_F} + \frac{g_m - \frac{1}{R_F}}{\frac{R_F}{R} + 1 + \frac{R_F}{sL} + R_F sC}. \tag{4.5}$$

If the transconductance is already chosen and the tank is designed, the feedback resistor R_F can be determined. If Z is the conjugate of the load impedance, at $\omega=\omega_0$ then

$$R_F = ZRg_m + Z - R. \tag{4.6}$$

This yields a narrow-band output match which resonates at the same resonance frequency of the tank in Figure 4.3 (the main LC tank that determines frequency response).

4.4 Noise

In the LNA, the input circuit dominates noise performance. In the cascode architecture, the series resistance of the gate input inductor and internal noise sources of the common-source stage are the primary noise contributors. A small signal model, with a simple FET model as derived in [13], is shown in Figure 4.5. Each noise source is a thermal noise source. The values of the gate and drain current sources depend on transistor parameters including transistor size and bias conditions. They are also correlated. The other two noises sources are uncorrelated.

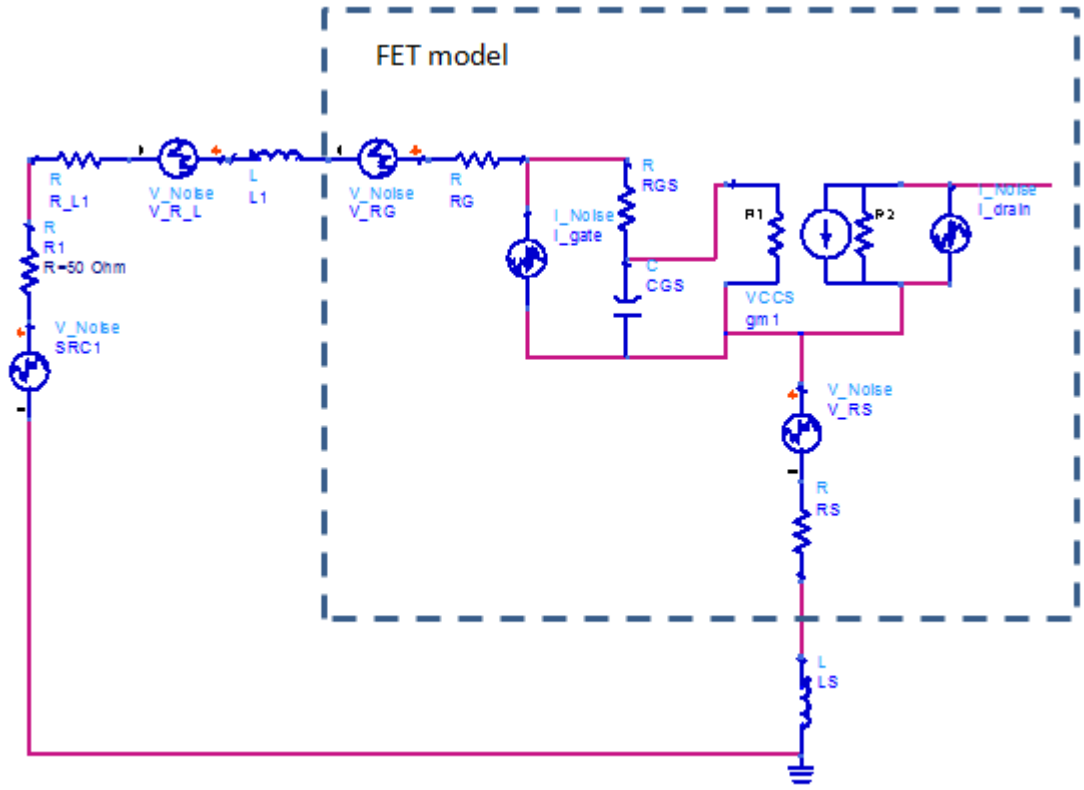


Figure 4.5 - Small signal model of cascode noise at input

For the common-source amplifier stage, there is a minimum in the curve of the minimum noise figure as a function of the drain-source current density (or gate-source

bias voltage). Figure 4.6 is a sweep of the minimum noise figure versus gate-source bias voltage for several transistors with five different gate finger widths (labeled Wx). Each device has six fingers. The simulation used a TriQuint pHEMT model which contains more detailed information about noise than the model in Figure 4.5. This curve can be used to find a bias voltage that will yield a potentially small noise figure for each device size. From 450 mV to 550 mV the minimum noise figure does not differ much for any of the devices. This gives a range of possible bias voltages for low noise performance.

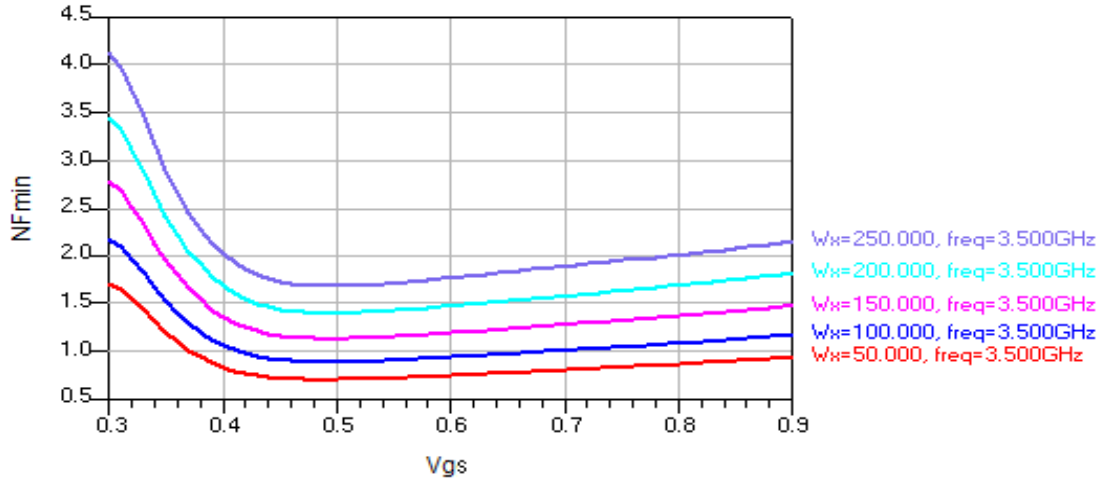


Figure 4.6 - Noise figure versus gate bias voltage for different sized devices at 3.5 GHz

The other major contributor to noise is the input gate inductor. The finite Q of the inductor implies some series resistance which adds a thermal noise source before any gain. Improving the Q of the inductor decreases the overall impact of this noise source.

4.5 Linearity

The linearity of the LNA determines the maximum size signal the amplifier can handle before the signal is distorted to a point where it is no longer useable. Since the cascode stage has a significant amount of gain, the signals seen by the output buffer are

much larger than the signals seen by the cascode. Therefore, the output buffer is the limiting factor in determining the linearity of the LNA. One way to improve the linearity of the output buffer is to bias the FET with a large gate-source voltage. As the cascode swings large signals across the gate of the common-source buffer, the operating regime of the transistor changes in a non-linear manner distorting the output signal.

The major trade offs are linearity versus DC current draw and optimizing for linearity while maintaining a high quality output match . Increasing the gate voltage and the transistor size help improve the third order output intermodulation but also increase the amount of current drawn from the battery. There is a limiting factor in how much the bias voltage can be increased because there is a limit on the drain current density in the transistor technology. Therefore, the size of the output buffer and size of feedback resistor are the factors that predominantly determines the linearity of the LNA.

Hand calculations of the output buffer would require a simple analytical model of the non-linear transconductance of the FET but no model was available. Instead, the ADS optimizer can be used instead to tune the size of the FET in the final design. The FET model used contains non-linear information. Since the feedback resistor must be set to maintain the output match, the size of the feedback resistor is also tuned as the transconductance of the FET changes. The ADS optimizer is capable of finding a combination of FET size and resistor size that yield good output match while limiting distortion. A more detailed analysis with example can be found towards the end of section 4.13.

4.6 Stability

The stability of the any amplifier is important. If the amplifier is potentially unstable, it might oscillate under certain conditions. To ensure the amplifier is stable one of many tests can be used. One simple test is the check the K-Δ test. To be unconditionally stable, the circuit must pass three tests [14]:

1. Be stable when terminated with the system impedance

2. The K factor must be greater than 1 where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|}$$

3. The |Δ| factor must be less than 1 where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}.$$

Often times it is difficult to perform step 1 of the above test. Conclusions drawn from the only steps 2 and 3 of the K-Δ test do not always tell the entire story. For instance, when looking into the drain of the common-gate stage of the cascode, the real portion of the input impedance can be negative over a certain span of frequency. If the impedance is negative enough, the circuit could oscillate and steps 2 and 3 of the K-Δ test might not display that because the negative resistance is embedded between gain stages. The cure for negative resistance is to add lossy components so that if reflected waves are larger than incident waves, there is something to attenuate the reflected waves. In the case of the cascode, the LC tank between the cascode and the buffer provides more than enough loss to cancel out the negative resistance. Care must be taken to ensure that the attenuation is enough, though, or the circuit may turn out to be potentially unstable.

4.7 Bias Networks

There are two types of biasing required for the cascode LNA with switches: amplifying transistor biasing and switch biasing. The amplifying transistors are enhancement mode transistors and require that the gate-source DC bias voltage V_{GS} be larger than zero. The switches are depletion mode devices. The depletion mode devices are "off" when their V_{GS} is negative (i.e. the channel is completely pinched off) and "on" when V_{GS} is zero.

Biasing for the depletion mode FET switch is shown in Figure 4.7. Resistor R_1 and source SRC1 "float" the transistor so that a single polarity supply can be used. DC blocking capacitors C_1 and C_2 pass RF signals while not allowing any DC current to escape which in turn could potentially bias the transistor in the saturation region instead of the linear region. DC voltage source SRC2 is the control voltage for the switch. When SRC2 is high, at V_{DD}, the switch is on and exhibits a low resistance from source to drain. When SRC2 is at ground, the switch is off and the drain-source resistance increases.

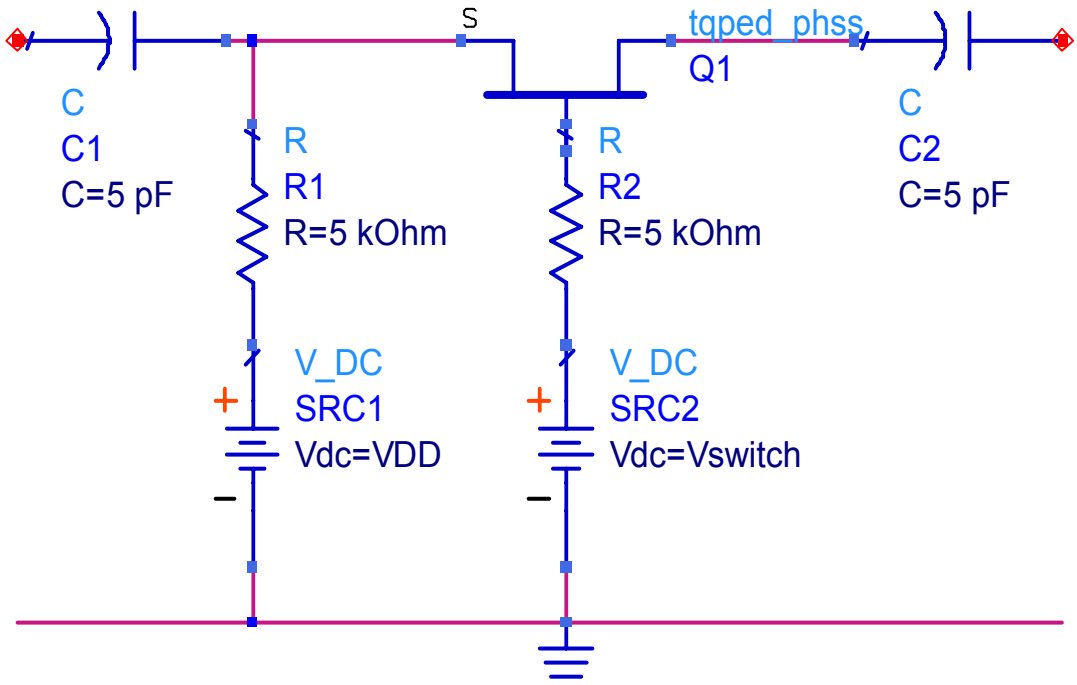


Figure 4.7 - Biasing for d-mode switch

The cascode bias requires two gate voltages. The common-source voltage needs to be precisely controlled because small changes in bias can alter the transconductance. The transconductance must be well controlled because the input match is tuned assuming a certain transconductance. To control the voltage precisely, a current mirror with a very stable current source is used. An extra source follower stage in the biasing helps compensate for changes in transistor threshold voltage (due to process variation) and transistor temperature. The bias circuit is shown in Figure 4.8. All three transistor are enhancement-mode pHEMTs. The voltage node labeled V_{gg} is applied to the gate of the common-source transistor and supplies the appropriate gate-source bias voltage. Q_1 acts like a resistor which supplies current to Q_3. The current supplied by Q_1 varies little over process variation and temperature because the current flows through a 1 µm wide channel

that is well controlled in size. When the source and gate are tied together, the transistor supplies 530 μA and drops 1.8 V. Q_3 is the mirror transistor for the common-source stage. Q_2 is the source follower that helps supply extra current to the gate of the RF FET. A small amount of DC current can flow into the gate of the common-source amplifier in the extreme corners of process variation and at high temperature [15]. If Q_2 were not included, the RF FET would try to draw current from Q_1 and Q_3 but they cannot supply a sufficient amount of current. Under nominal conditions such as room temperature operation, ideal fabrication, and low input power to the RF FET, there is no advantage to the buffer. But as conditions deviate from the ideal conditions, the buffer helps compensate for variations. The topology is very similar to a current-compensated BJT current mirror in which the base current of the mirror transistor and signal transistor must be accounted for.

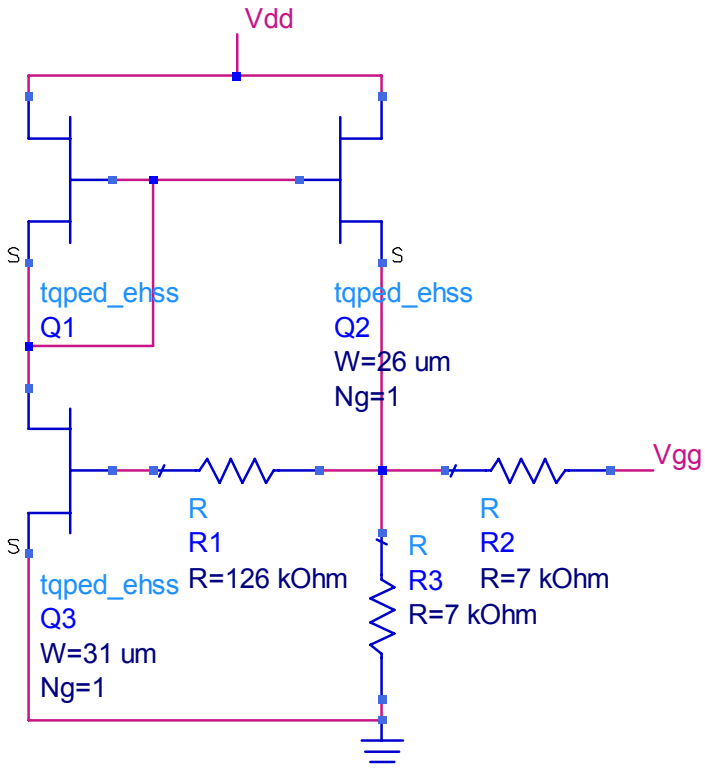


Figure 4.8 - Compensated bias for common-source gate voltage with three enhancement mode FETs

To design the current mirror, begin by designing a simplified circuit as shown in Figure 4.9. The width of FET Q_3 can be swept until V_{out} reaches the desired output voltage.

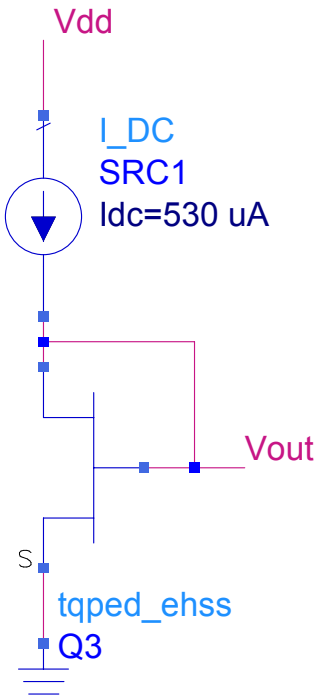


Figure 4.9 - Simple Bias Circuit

Next, the RF FET can be added with appropriate gate resistors R_1 and R_2 in Figure 4.8 can be chosen. For resistor R_2 bigger is typically better but it cannot be too large because R_1 must be proportionally large. For Q_1 to properly mirror the current through the RF FET, the size of R_1 should be

$$R_1 = R_2 \frac{W_{RF,FET}}{W_1} . \tag{4.7}$$

The size of Q_2 is not critical. Ideally, a small device is preferable to keep DC current draw low but empirical evidence suggests that a single 25 µm wide gate tracks best with variation in pinch off voltage. After final tuning, the circuit in Figure 4.8 supplies 500 mV.

The graph in Figure 4.10 demonstrates the value added by the source follower circuit. The solid line is the DC current through a 600 µm E-mode FET where V_{DD} = 1.65 V with the uncompensated bias circuit while sweeping the threshold voltage of the FET. As the threshold voltage increases, the drain current rapidly falls off. But when the source-follower is added, as shown with the dashed line, the current varies much less over threshold variation. Figure 4.11 shows the value added over temperature where the solid line is the DC current without the source follower and the dashed line is the DC current with the source follower.

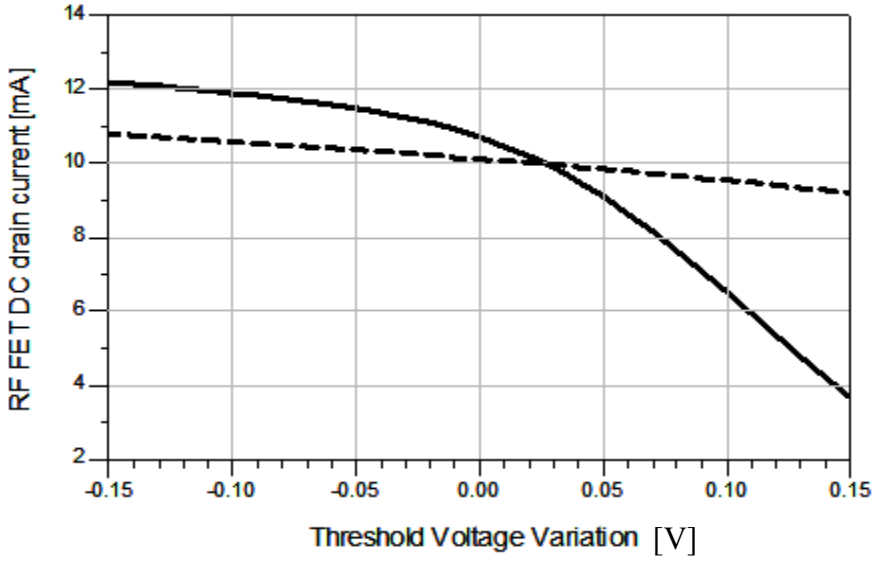


Figure 4.10 - RF FET DC current with threshold voltage variation

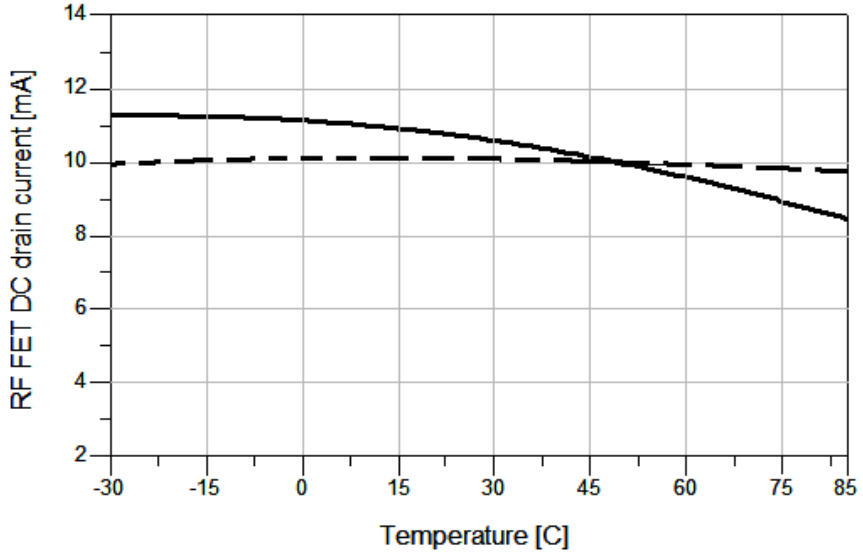


Figure 4.11 - RF FET DC current with temperature variation

The bias of the common-gate stage of the cascode is less critical. A voltage divider is satisfactory as long as the resistors are physically close so that they track together in temperature and variations in processing.

The output buffer is also a common-source stage. It is biased by another current mirror similar to the one in Figure 4.8. Since the required bias voltage is higher, Q_1 supplies more current, and the mirror transistor Q_3 is smaller. Together, the output voltage is higher.

4.8 Power Consumption

Power consumption is always an important factor in circuit design but is especially critical in portable applications where the primary power source is a battery with a limited amount of charge. There are always tradeoffs between power consumption

and other circuit parameters, particularly linearity, gain and noise figure. Typically, larger DC current draw results in better linearity. More current also means higher transconductance which translates into higher gain. And higher gain usually means better noise figure because power gain increases as the square of the transconductance and noise power increases linearly with the transconductance. Higher gain in the early stages helps negate noise further down the circuit.

The three amplifying transistors are the primary source of DC current draw. The bias networks and switch control voltages also draw a miniscule amount of DC current. The gate bias of the common-source stage of the cascode primarily determines the current through the cascode.

4.9 Switches

The switches used in the new inductors and capacitors are critical to operation of the reconfigurable cascode. The switches play a key role in the determining the Q factor of both the input gate inductor and LC tank capacitor. The non-idealities of the switches, primarily the parasitic capacitance and non-zero/non-infinite on/off resistances affect the circuit performance.

The best choice for switches is the depletion mode pHEMT. The depletion mode device exhibits a similar parasitic capacitance to the enhancement mode FET but has a lower on resistance. A small signal circuit equivalent is shown in Figure 4.12. The equivalent circuit is composed of a parallel RC circuit. In the “On” state, the resistance is small and in the “Off” state, the resistance is on the order of thousands of ohms. The

capacitor is determined only by transistor size and not whether the switch is open or closed.

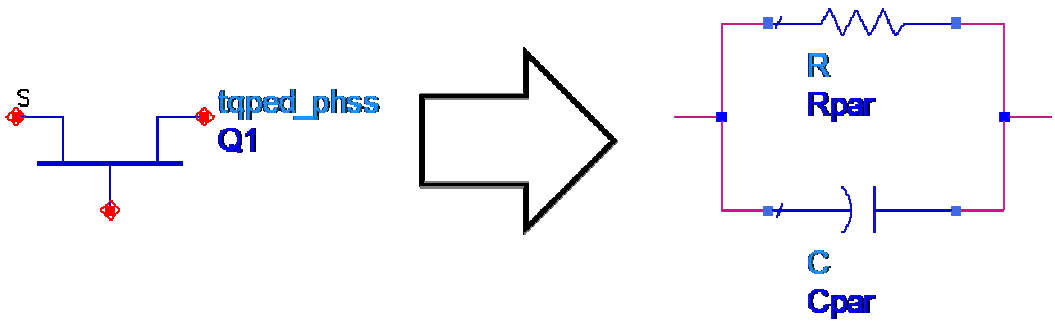


Figure 4.12 - Switch and small signal equivalent

The graphs in Figure 4.13 and Figure 4.14 are the simulation results of the on resistance of the switch and the associated parasitic capacitance for different values of gate length with a fixed number of gates (10 gates). For all FET sizes, the "off" resistance was 5000 Ω.

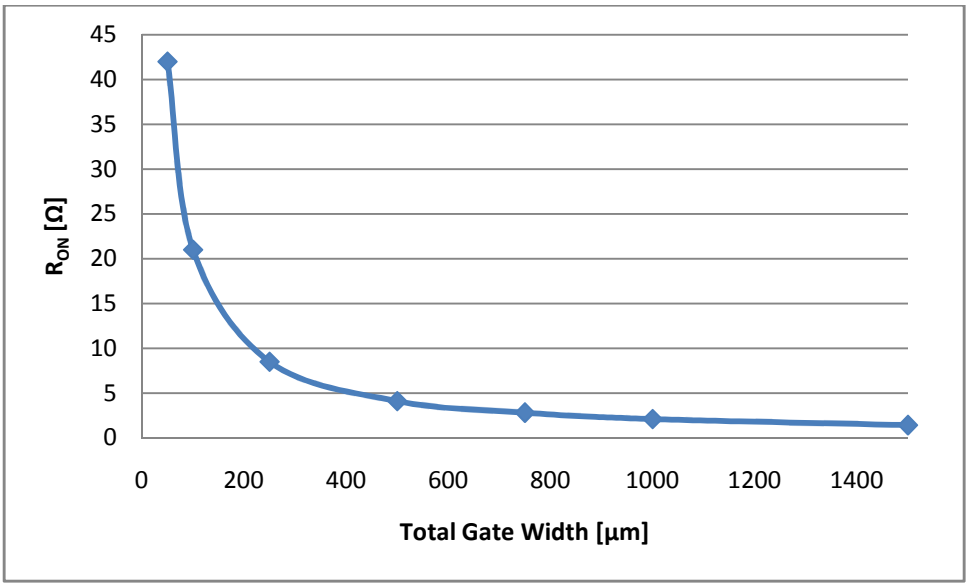


Figure 4.13 - Switch "On" resistance versus gate width.

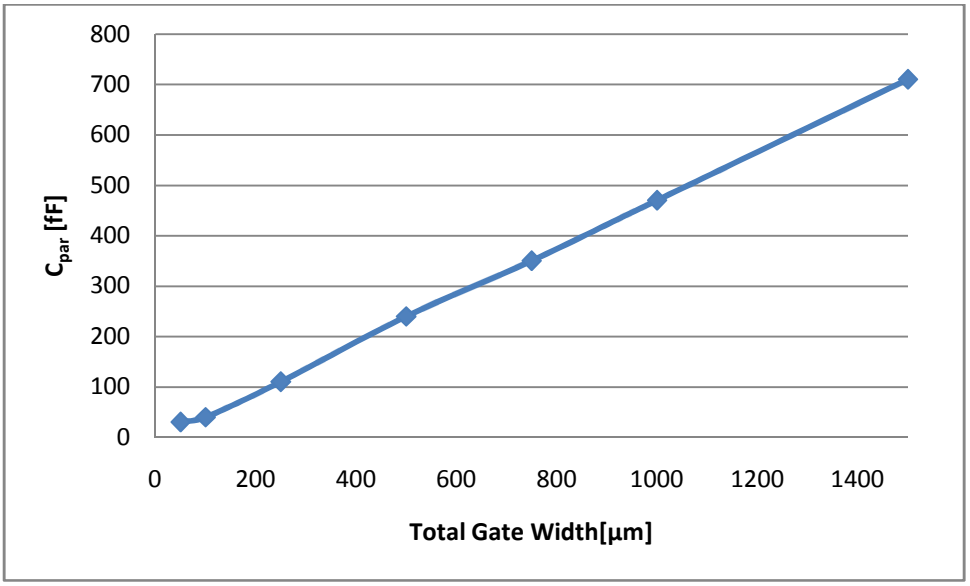


Figure 4.14 - Switch parasitic capacitance versus gate width

The design of the switches involves one main tradeoff between parasitic capacitance and series resistance. A larger switch has less “On” resistance but higher

capacitance. At lower frequencies the capacitance might not be important but at high frequencies the isolation can be degraded in the “Open” state because the high frequency signals can be shorted through the capacitance rather than being blocked by the large “Off” resistance.

4.10 Spiral Inductors with Taps

In order to create a reconfigurable amplifier, reconfigurable circuit elements are required. In a source degenerated cascode LNA, variations in the size of the gate inductance are capable of changing the resonant frequency of the input impedance of the cascode.

The concept behind the' tappable' inductor is shown in Figure 4.15.

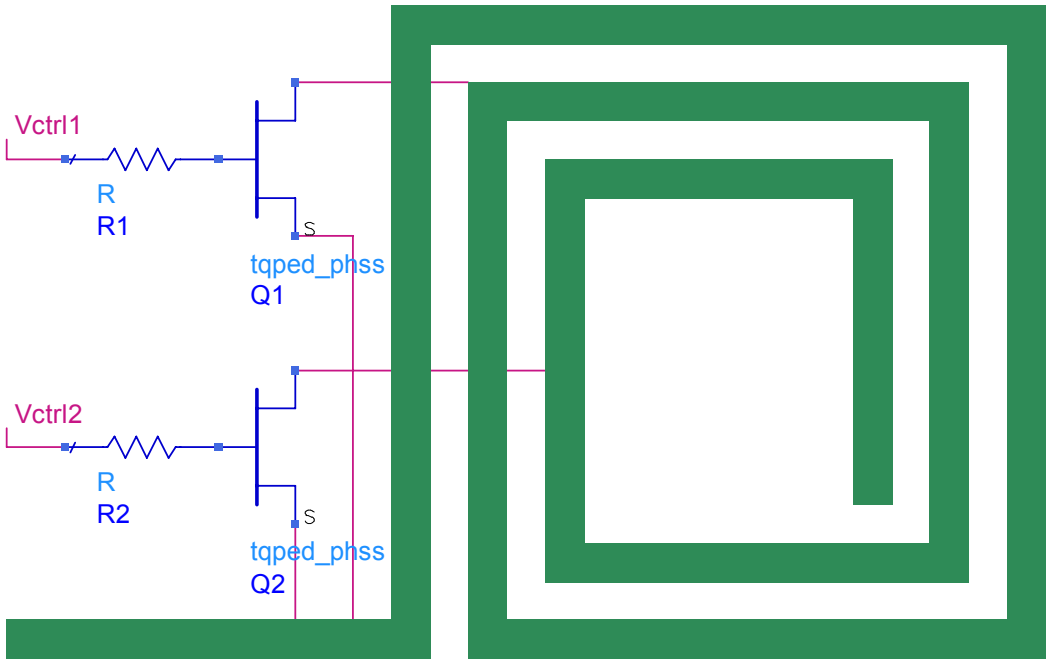


Figure 4.15 - Diagram of tappable inductor and switches

Every metal trace has some self-inductance. The inductance is increased when the metal trace is lengthened and wrapped into a spiral structure. To electronically adjust the value of a spiral inductor turns of the spiral must be shorted out in an effort to remove them from the circuit. Using FETs as switches, certain traces of the inductor can be shorted out effectively reducing the inductance of the structure. The FETs are imperfect, though, and their parasitic components affect the overall behavior of the inductor.

A three band LNA requires two switches for a total of three useable settings on the inductor. To keep the Q of the inductor as high as possible only one switch should be on at a time. Placing two switches in series to short out consecutive traces is possible but the parasitic switch resistances add together and can greatly reduce the Q factor of the

inductor. A lumped element model that closely mimics the electromagnetic simulation results of a spiral inductor without switches is shown in Figure 4.16.

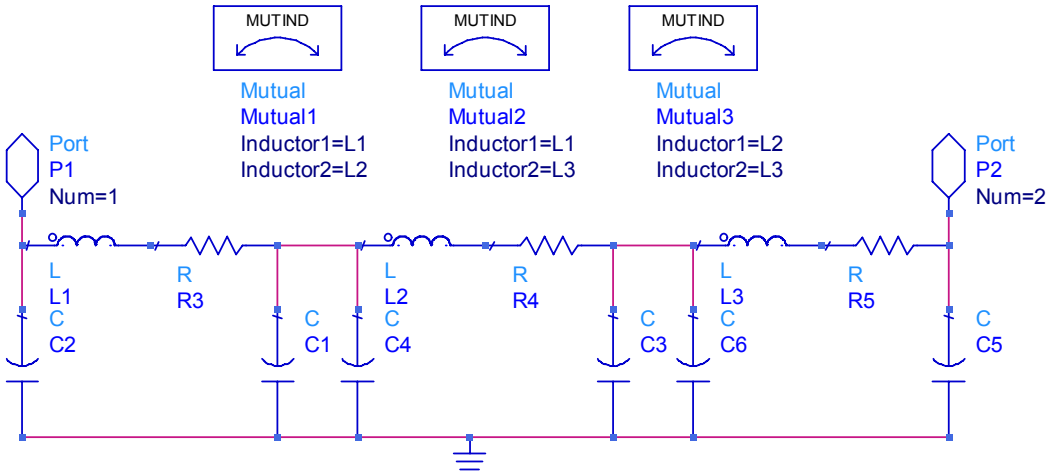


Figure 4.16 - Lumped element model of tappable spiral

The three sections of the main spiral are broken into three separate inductors that couple as any inductors in a physical vicinity do. Each inductor also has an associated series resistance and parasitic shunt capacitors on each end. The coupling plays a key role in the model when there are no switches included. Once the switches are included, the effects of the weak coupling can be removed because they are overshadowed by the effect of the parasitics of the switches.

A simple switch model is made up of a parallel RC circuit. A model of the inductor with switches is shown in Figure 4.17. The model is the same whether the switch is on or off. The resistance of resistors R_6 and R_7 is all that changes when the switch changes from an on state to an off state. For example, the on resistance will be several ohms while the off resistance will be several kilohms. The large parasitic

capacitance of the switch lowers the self resonance frequency of the inductor and also increases the effective inductance below the self resonance frequency.

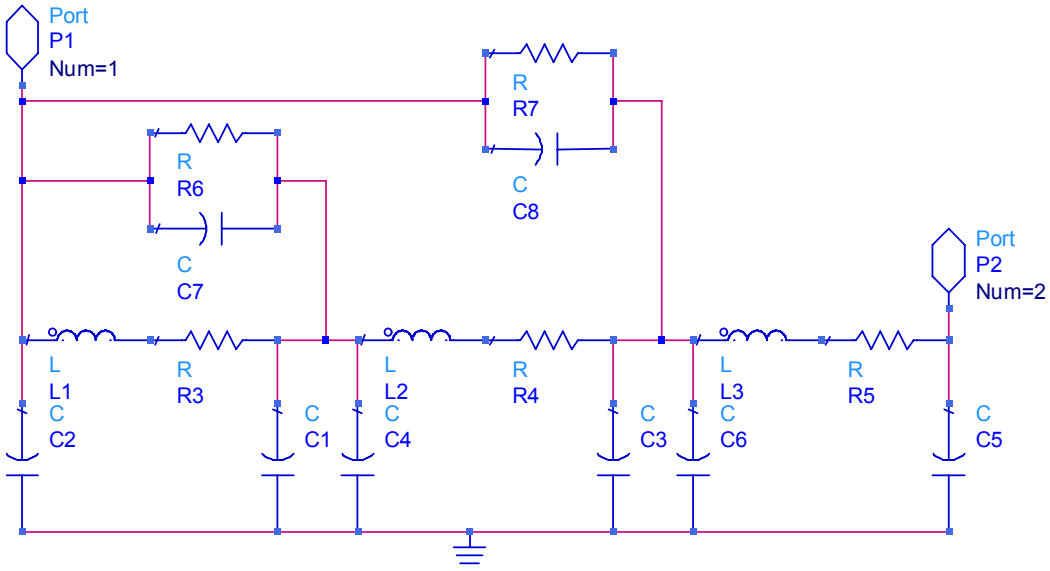


Figure 4.17 - Lumped element model of inductor and switches

There is a direct trade-off in picking the size of the FET switches. A small transistor has a low parasitic capacitance but a large "on" resistance which greatly reduces the Q factor of the inductor. A larger FET improves the Q by reducing the parasitic resistance but at the cost of lowering the self resonance frequency of the inductor.

The type of FET used for a switch is depletion mode pHEMT. The depletion mode switches have a lower "on" resistance than their enhancement mode counterparts. The lumped element model with the required biasing for the d-mode pHEMT biasing is shown in Figure 4.18. For simplification, only a single switch and biasing is shown.

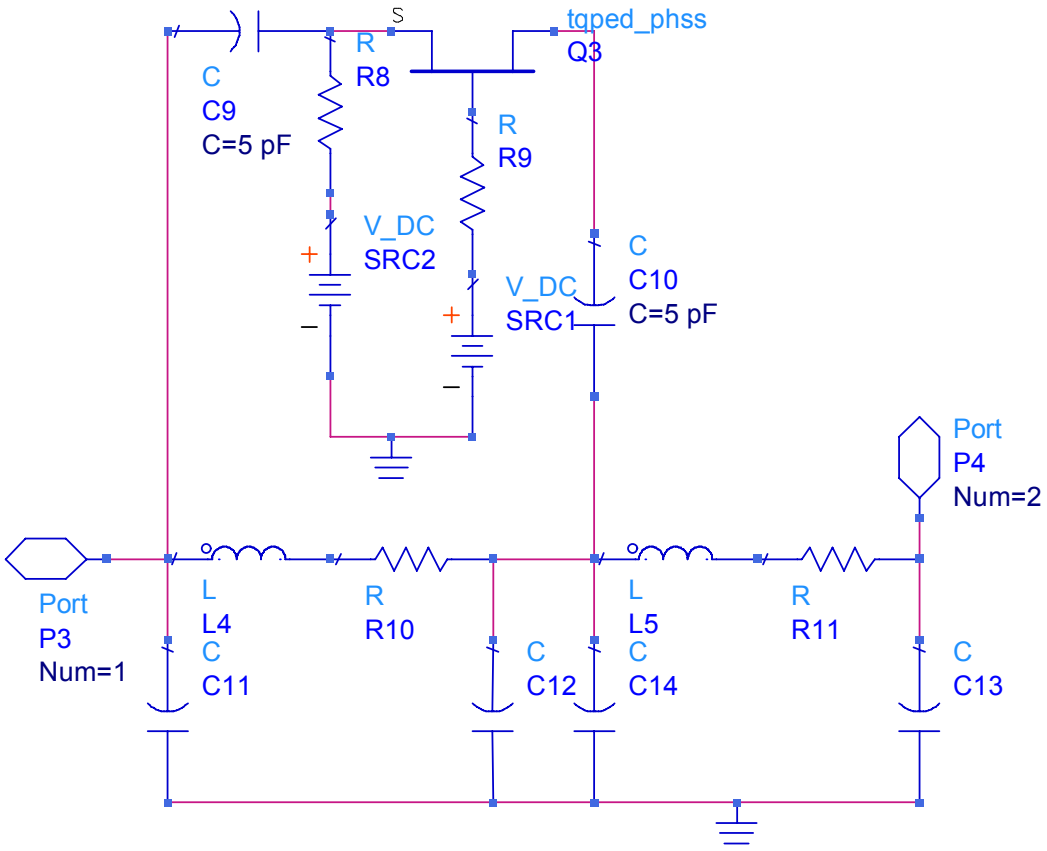


Figure 4.18 - Tappable inductor model with switch and switch bias

The first step in designing the 'tappable' inductor is to draw and simulate a spiral inductor for the low-band operation. Next, two taps are added at various points along the spiral resulting in a four-port network. In the schematic simulation, the 4-port S-parameter network is used with the FET switches. A schematic with the switches, switch biasing, and a four port data block is shown in Figure 4.19. The large 5 pF capacitors are used as DC blocking capacitors. The capacitors are chosen to be 5 pF because that is upper limit for capacitors at 5 GHz in the GaAs process used. Fine tuning involves setting the overall size of the spiral structure and number of turns, the location of the taps, and the size of the switches.

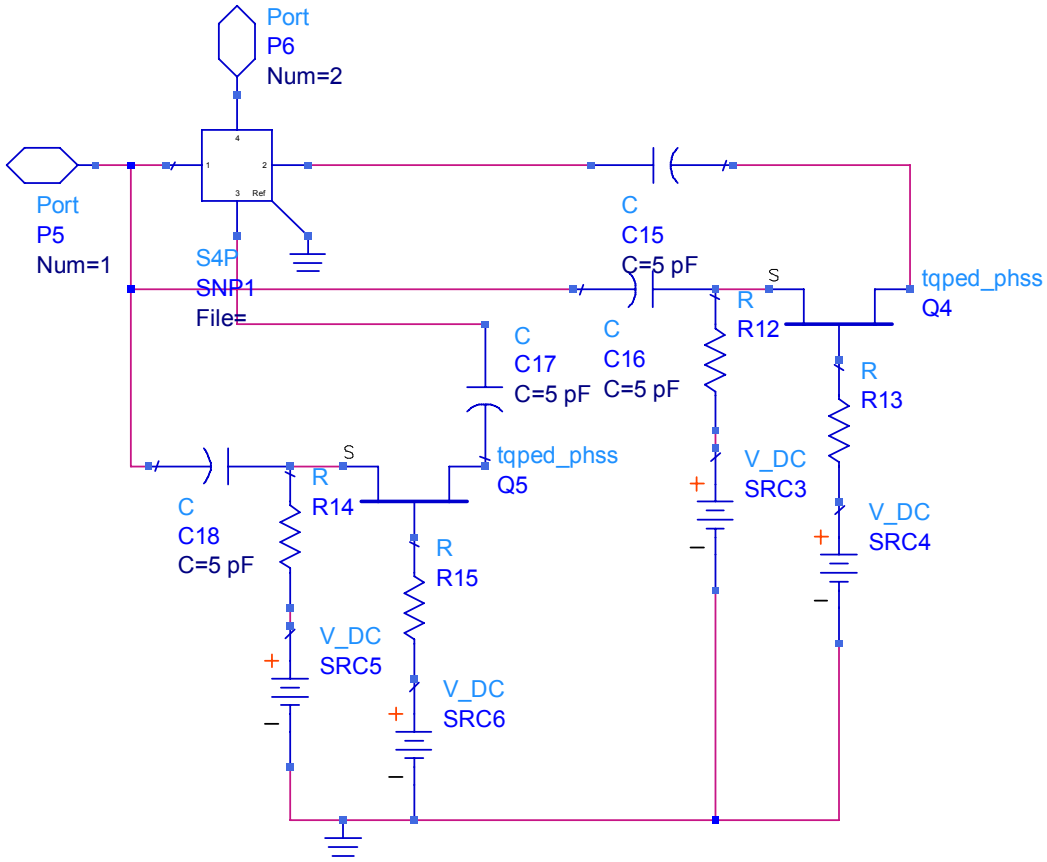


Figure 4.19 - 4 port network for inductor with switches and biasing

4.11 Switchable Capacitors

To control the frequency response of the gain, the capacitance for the tank between the cascode and output buffer is adjusted to resonate at the desired frequency of operation. The cascode has an inherent roll-off of gain as frequency increases. By adjusting the shunt capacitance instead of the inductance, the gain roll off can be compensated for because the larger capacitance settings have a lower Q. The parasitic series resistance of the switches lowers the Q of the capacitors and plays a more

significant role in determining the Q factor of the capacitance when the switch is "on" rather than "off." The schematic of the adjustable capacitor is shown in Figure 4.20.

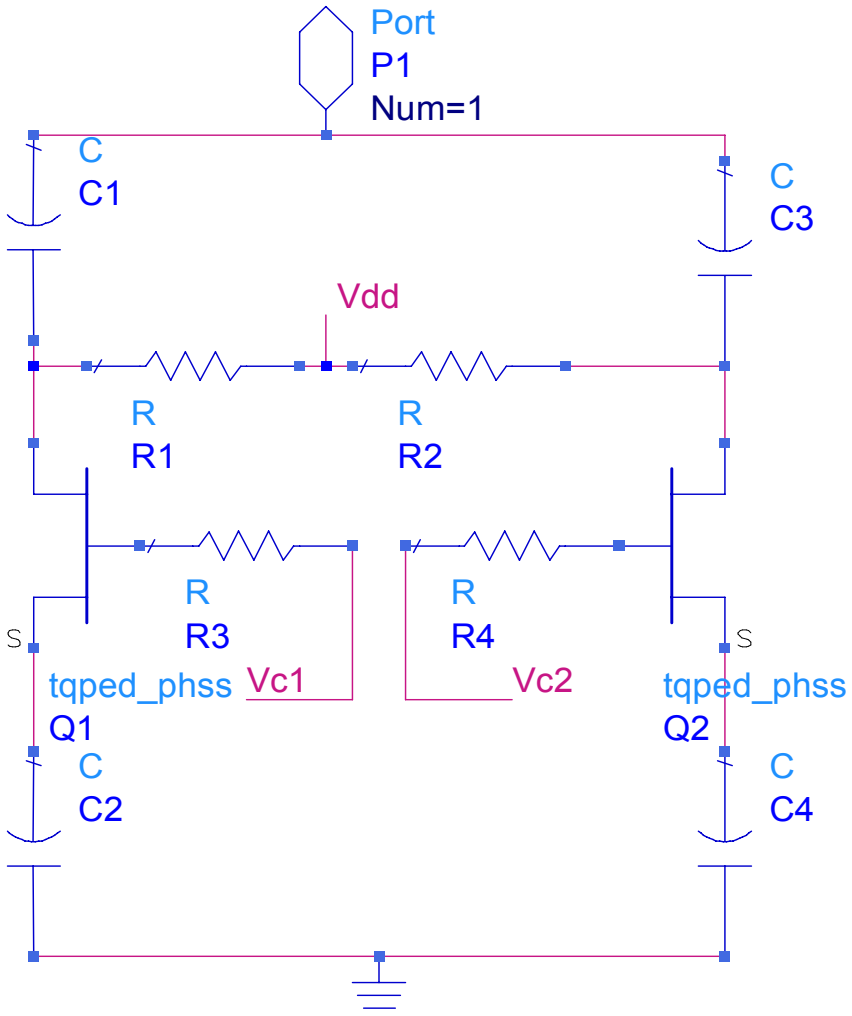


Figure 4.20 - Schematic of adjustable capacitor with switches and biasing

The entire adjustable capacitance structure is made of four capacitors and two FET switches. For low frequency mode, both switches are "on." For mid-band operation one switch is turned off while the other remains on. For high band mode, both switches are turned off. The parasitic capacitances of the switches in series with the large parallel

plate capacitors add together and total enough capacitance to resonate with the inductor at the desired frequency.

To design the adjustable capacitor, there are three degrees of freedom to take into consideration: capacitors C_1 and C_2 of Figure 4.20 which are in series with transistor Q_1, capacitors C_3 and C_4 which are in series with transistor Q_2, and transistors Q_1 and Q_2. To simplify the design several assumptions are made: C_1 is the same size as C_2, C_3 is the same size as C_4, the size of transistors Q_1 and Q_2 is the same, the parasitic capacitance of the switches is much smaller than the capacitance of the parallel plate capacitors (C_1-C_4), the "on" resistance of the switches is zero, and the "off" resistance is infinite. Figure 4.21 shows the schematic of the capacitance structure (without biasing) and the three states that the structure can be in for low-band, mid-band, and high-band operation. For low-band operation, both Q_1 and Q_2 are on. For mid-band operation, Q_1 is on and Q_2 is off. For high-band operation, both Q_1 and Q_2 are off.

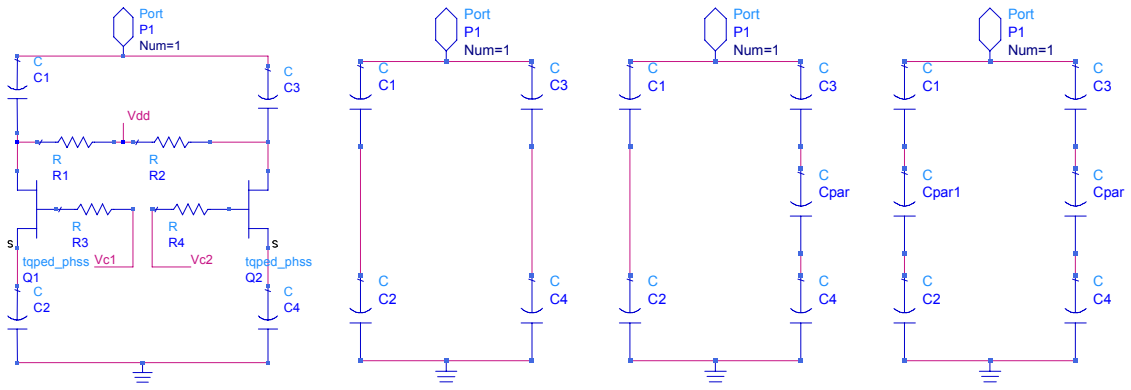


Figure 4.21 - From left to right: Switchable Capacitance circuit, low band equivalent circuit, mid band circuit, and high band circuit

Assuming that the size of the capacitance required for the three modes of operation are known, the equivalent circuits in Figure 4.21 can be used to generate three equations and three unknowns.

$$\begin{aligned} \frac{C_1}{2} + \frac{C_3}{2} &= C_{LB} \\ \frac{C_1}{2} &= C_{MB} \\ 2C_{par} &= C_{HB} \end{aligned} \quad . \tag{4.8}$$

Solving for C_1, C_3, and C_{par} yields

$$\begin{aligned} C_1 &= C_2 = 2C_{MB} \\ C_3 &= C_4 = 2\left(C_{LB} - C_{MB}\right) \\ C_{par} &= \frac{C_{HB}}{2} \end{aligned} \quad . \tag{4.9}$$

To find the required sizes of switches based on the parasitic capacitance, the graph like that of Figure 4.14 of section 4.9 can be used.

4.12 Bond Wires & ESD Protection

Figure 4.22 shows the schematic of components between the bench top power supply and V_{DD} for the LNA. Inductor L_1 represents a 1 meter cable between the power supply and the connector on the PCB. Capacitor C_1 is a large surface mount capacitor on the circuit board to supply extra current to the LNA if the power supply is too sluggish to source current at high frequency. Inductor L_{self_res} is parasitic inductance of the SMT capacitor that gives the capacitor a self resonance frequency. The bond wire is approximately 0.5 nH. C_2 is an on chip capacitor to further help keep the power supply clean. The bond wire and on chip capacitor resonate just below 2 GHz and add an out of band bump in the gain. Resistor R_1 is necessary to suppress as this resonance near the LNA's band of operation.

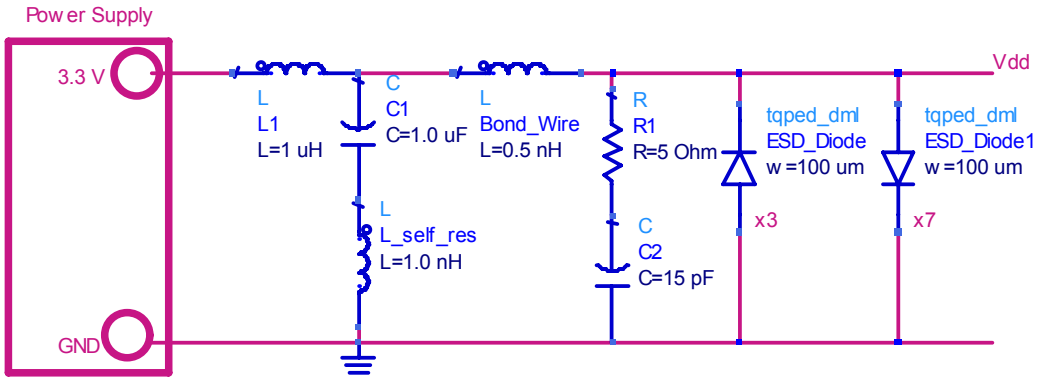


Figure 4.22 - Bond wire and ESD for V_{DD}

ESD_{Diode} and ESD_{Diode1} are on chip diodes to protect the circuit from electrostatic discharge. ESD_{Diode} is made up of three series diodes, and ESD_{Diode1} is made up of seven series diodes. The three series reverse bias diodes begin shunting current to ground if for any voltage below - 2.5 V. The seven forward bias diodes shunt any current to ground

when the voltage goes over 5 V. This ESD protection keeps the drains and sources of all the transistors safe. For the gate on the first common-source transistor, the input capacitance has been shown to be a very satisfactory protector of the transistor from ESD damage.

The switches also require ESD protection and use the same setup as the V_{DD} circuit. The on board 1 µF capacitor is not necessary and neither is the small resistance in series with the 15 pF capacitor. The schematic is shown in Figure 4.23.

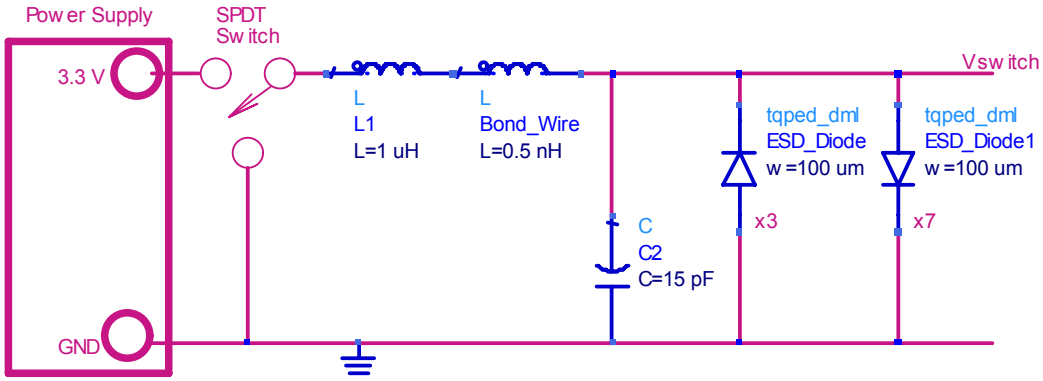


Figure 4.23 - Bond wire and ESD for switches

4.13 Design of Cascode in this Thesis

The first step in the design of a new circuit is to list the goals and specifications of the circuit. For this circuit the primary goal is to construct an LNA that is electronically reconfigurable with three bands of operation at 2.5 GHz, 3.5 GHz and 5.5 GHz. The technology used will be the 0.5 µm TriQuint Semiconductor PED pHEMT process with enhancement mode and depletion mode transistors. The LNA is to have an input match and output match of at least 20 dB, at least 15 dB of transducer gain, a noise figure better than 3 dB and an input referred compression point above -10 dBm. The input third order

intermodulation power should be at least 5 dBm. The LNA is to operate with a single 3.3 V DC power supply and draw no more than 20 mA of quiescent current not including the output buffer. The die size should be at most 2 mm by 1 mm.

The first step in designing the LNA is to design the cascode. The cascode design begins with picking the common-source transistor bias and transistor size. Using Figure 4.24, the optimum gate bias voltage for lowest noise figure is around 500 mV for devices with six gate fingers with a width ranging from 50 μm to 250 μm. Figure 4.26 is a plot of IIP3 and the DC drain current swept for various gate widths for the circuit in Figure 4.25. For each different transistor size, the gate and source inductors are tuned to give an optimum input match at 2.5 GHz. The load is 5 Ω to approximate the input impedance of the common-gate stage of the cascode. As the drain current increases, so does input power. At 600 μm, the drain current is 15 mA which gives 5 mA margin from the spec. The common-source stage of the cascode is then chosen to have 6 gate fingers each being 100 μm long. This also gives plenty of headroom for IIP3 spec of 5 dBm because at 600 μm the stage has an IIP3 of over 5 dBm.

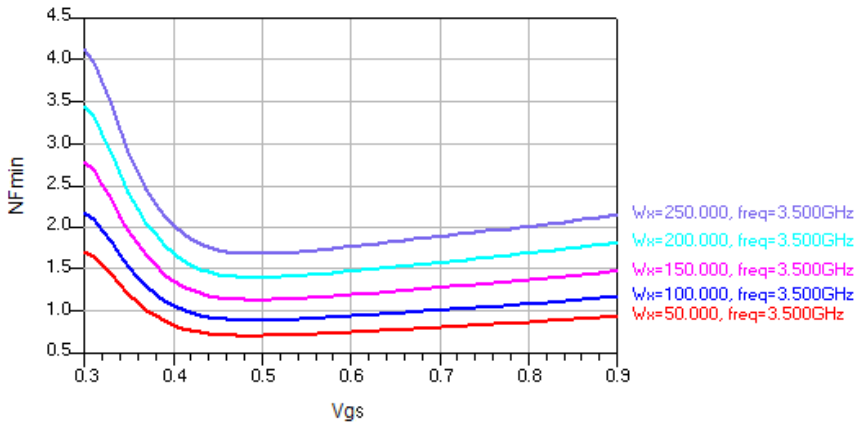


Figure 4.24 - Minimum noise figure as a function of gate-source voltage

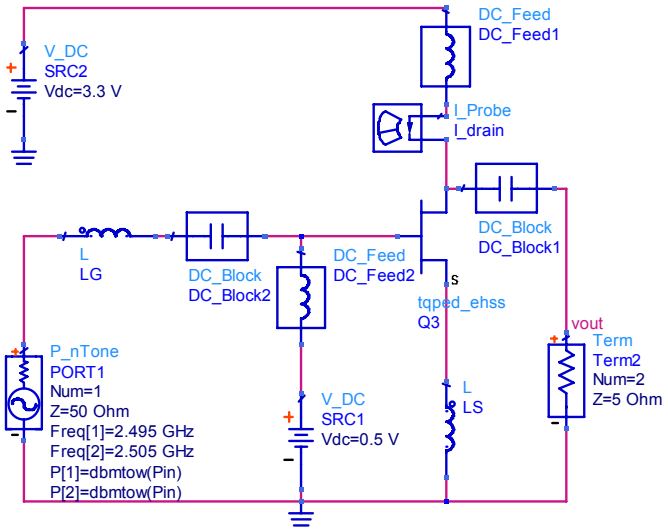


Figure 4.25 - Common-source stage for linearity measurements

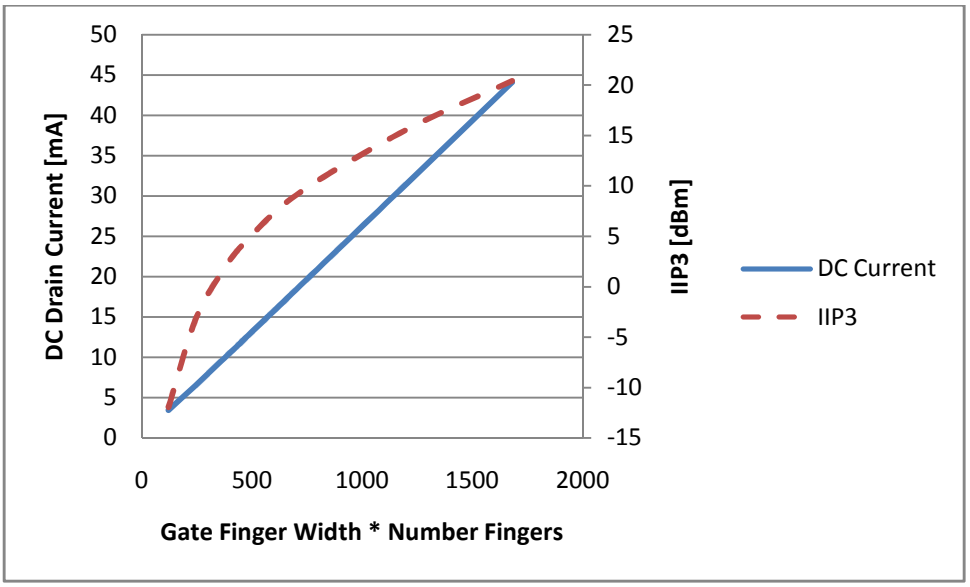


Figure 4.26 - IIP3 and DC current as a function of total gate width

The next step in the cascode design to pick the size and bias of the common-gate transistor. The bias is chosen such that half the voltage supply drops across the common-gate and the other half drops across the common-source. There is a trade off in the size of the cascode transistor. As the transistor gets larger, the transconductance increases which decreases the voltage gain of the common-source stage. The common-source stage is plagued by the Miller effect and by decreasing its load, and therefore voltage gain, the bandwidth increases. Since the highest frequency of operation is 5.5 GHz and the unity gain frequency is 30 GHz, any additional bandwidth can be extremely helpful. The tradeoff arises because as the common-gate transistor is increased in size to gain bandwidth, the linearity of the stage drops [16]. Figure 4.27 plots both the -3dB point of the cascode and the IIP3 for various sizes of common-gate transistors. The two input tones are at 2.495 GHz and 2.505 GHz. The gate and source inductors are tuned to give the input match for best return loss. The bandwidth plateaus after the transistor gets near 400 µm total length. The common gate transistor is chosen to be 65 µm width 6 fingers

(390 µm total). The IIP3 is sacrificed about 0.5 dB under the original spec in order to obtain the extra bandwidth.

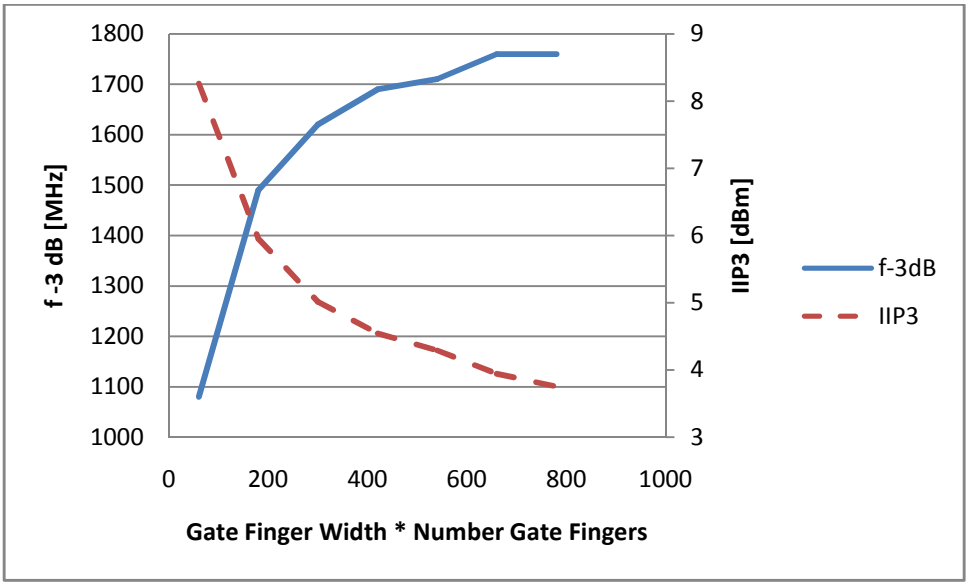


Figure 4.27 - f_{3db} and OIP3 for various sizes of common gate transistors

The gate bias of the common-gate is tuned to 2.1 VDC. This results in a 1.65 V dropping across the common-gate and 1.65 V dropping across the common-source.

The next step is to design the source-inductor of the common-source stage. This inductor increases the real portion of the input impedance of the cascode to the system impedance, 50 Ω. The transconductance of the common-source transistor is 175 mS and its gate-source capacitance is around 870 fF . To find the size of the inductor use

$$L_S = \frac{Z_0 C_{GS}}{g_m} . \tag{4.10}$$

According to equation (4.10, the source inductor should be approximately 250 pH. After final tuning, the required inductor was closer to 300 pH.

After the size of the source inductor is chosen, the gate inductor needs to be designed. The first step to designing this inductor is to find the size of inductance required for each band. They can be approximated using

$$L_G = \frac{1}{\omega_0^2 C_{GS}} - \frac{Z_o C_{GS}}{g_m} \quad . \tag{4.11}$$

Plugging in values for the three bands of operation yields the following table

Table 4.1 - Required cascode gate inductance

Band	Inductance [nH]	Inductance after tuning [nH]
2.5 GHz	4.36	5.6
3.5 GHz	2.08	3.1
5.5 GHz	0.67	1.5

The inductors need to be slightly larger than expected because there is still some Miller effect and other stray capacitance.

The next step is to design a 5.6 nH inductor. Each winding is 15 μm and the spacing between turns is 8 μm. For the GaAs process used to fabricate the LNA, these values have yielded high quality factor inductors. The final spiral shape used in the LNA has 3.5 total turns and is 470 μm long and 218 μm wide. This structure yields an inductance of only 4.7 nH and a Q of 22 at 2.5 GHz. The inductor winds up being smaller than expected because once the parasitic capacitance of the switches are in parallel with the inductor they end up increasing the amount of positive reactance below the self resonance frequency (although they do lower the self resonance frequency itself).

Extra metal traces that tap into the spiral are added and switches are added to connect the input of the inductor to the taps. The taps are tuned by sliding them up and down the sides of the main inductor until the input match is centered at the desired frequency. The ratio of the height to length of the main inductor might also need to be adjusted so that the taps can remain on the sides. Figure 4.28 shows the main inductor and the tap locations. The arrows indicate where the taps can travel to tune the match frequencies.

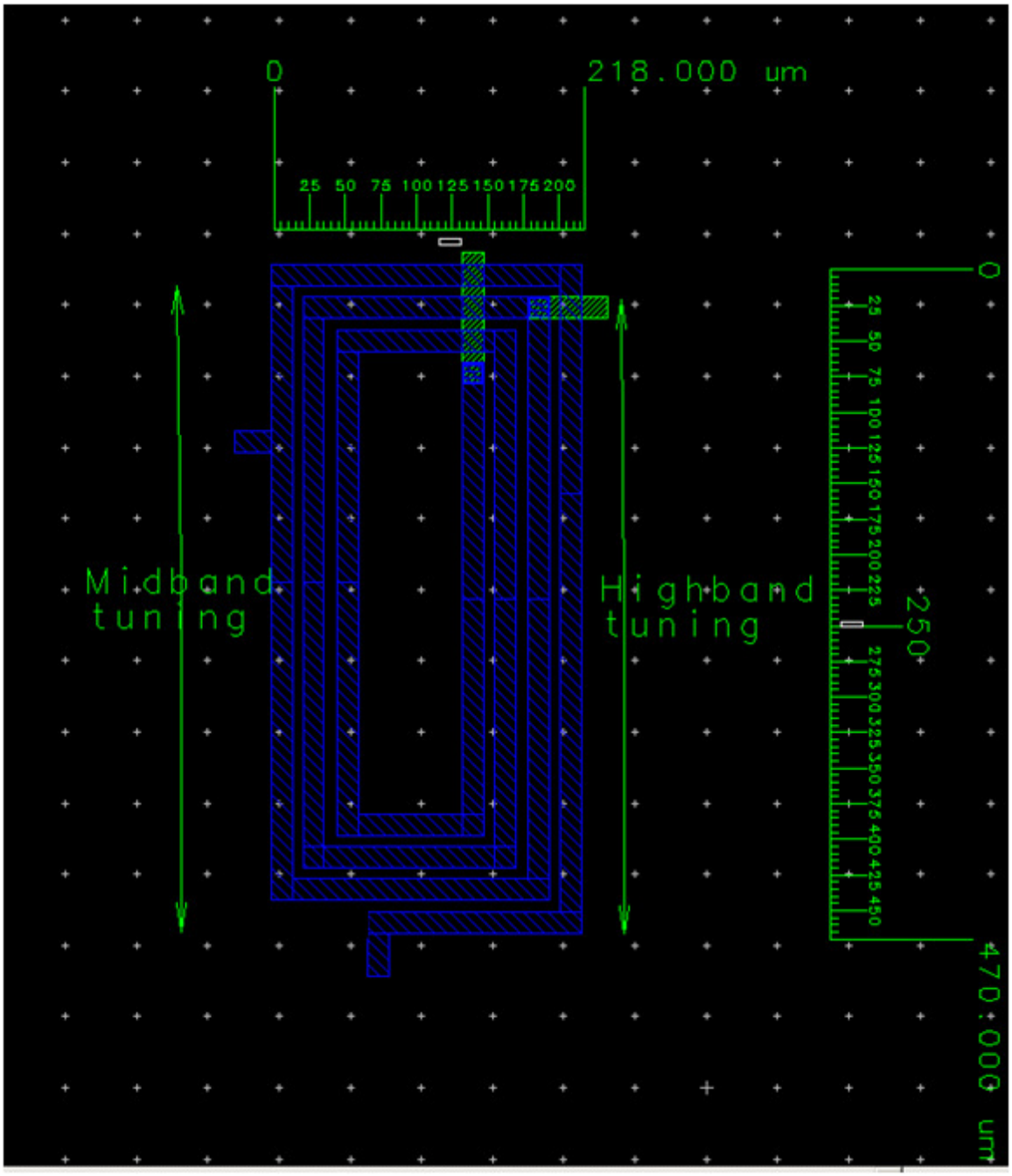


Figure 4.28 - Final cascode input inductor with taps for switches

The width of the switches is tuned so that the bottom input of the inductor is connected to one of the taps on either side of the inductor. The number of gates is also important because it, along with the gate finger width, determines the switch parasitics

which play a key role in tuning the input circuit. The switch capacitance increases the effective inductance but also decreases the self resonance frequency. The switch size also determines Q of the input inductor. For the mid-band switch, the final size has 5 gate fingers that are 300 μm wide. The switch to operate the LNA at high band has 4 gate fingers that are 470 μm long.

The input inductor is simulated in the electromagnetics simulator. The S-parameters of the input inductor and switches are then simulated in the schematic simulator and summarized in Table 4.2.

Table 4.2 - Input inductor with switches simulation results

Frequency [GHz]	Inductance [nH]	Q
2.5	4.65	5.11
3.5	2.54	2.98
5.5	1.54	3.35

Ideally the cascode's drain bias inductor would be an on-chip spiral inductor used in the LC tank that determines the frequency response of the gain. Unfortunately, the bond wire (approximately 0.5 nH) resonates with the on-chip 15 pF power supply capacitor. This resonance adds a hump to the gain around 1.8 GHz. To help suppress the resonance, the drain bias inductor must be increased greatly in size to lower the resonance frequency. The bias inductor winds up being an on-chip inductor with 8.5 turns with 8 μm spacing and 8 μm spacing trace width. At 2.5 GHz, the inductor has 23 nH of inductance and a Q of 15.

The schematic of the circuit up to this point is shown in Figure 4.29. The input inductor is shown as all three inductors in parallel (L_4, L_5, & L_6) but in the actual circuit, only one of these three inductors is ever in use.

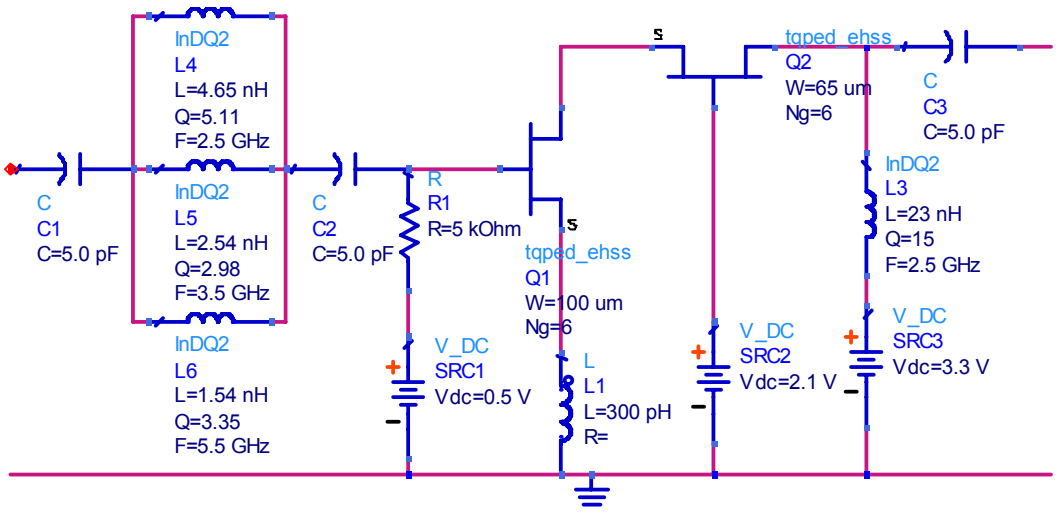


Figure 4.29 - LNA schematic - cascode half

The LC tank is the next stage to be designed. A small inductor and large capacitor yield a more narrow pass-band. The inductor is chosen to be 0.6 nH. Anything much smaller is difficult to build and keep the Q high because the trace widths must be made increasingly smaller to allow a spiral structure to form and to keep the spiral from overlapping upon itself.

The switching capacitor circuit is designed using the outline laid out in section 4.11. First the required capacitances to resonate at the desired frequencies are calculated. Then the equations give approximate values for the size capacitors and switches. Final tuning is required. The circuit used in the LNA is shown in Figure 4.30. When both Q_1 and Q_2 are on, the entire circuit acts as one large capacitor for the low band operation. For mid band operation, Q_1 is turned off and Q_2 remains on. For high band operation,

both transistors are off . The parasitics from the transistors are large enough that when both switches are off, the entire circuit acts a large enough capacitor to enable high frequency operation. Table 4.3 summarizes the total capacitance and Q at the three operating frequencies.

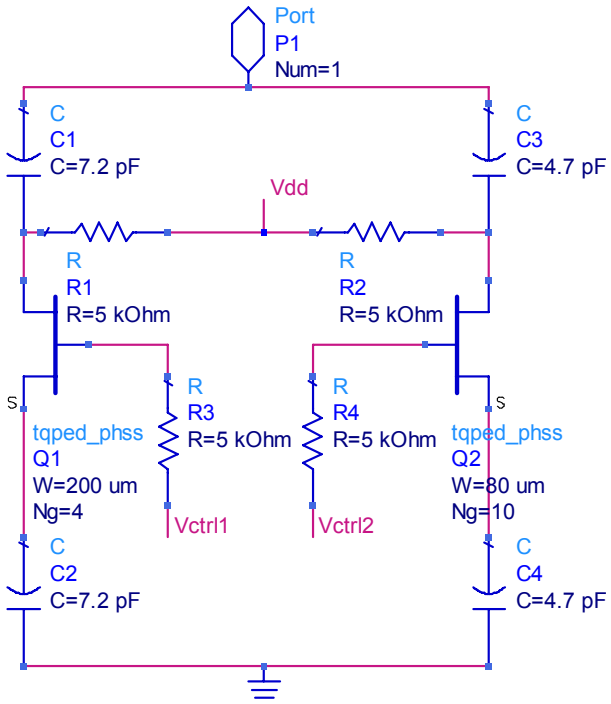


Figure 4.30 - Switchable capacitor bank

Table 4.3 - Capacitance and Q of switchable cap

Freq	Capacitance [pF]	Q
2.5	5.84	7.7
3.5	2.57	7.82
5.5	.53	31.22

The output buffer is a common-source amplifier with resistive feedback. The transistor is biased with a higher gate voltage than the previous stages to help increase the linear range of the LNA. The gate-source voltage is chosen to be 900 mV which is about 100 mV below the threshold for maximum drain current density to allow for some margin. To pick the transistor size, a device is chosen to draw 10 mA to keep the total current draw near 20 mA. This transistor has three fingers that are 14 μm long. The feedback resistor is then tuned in ADS to give the best linearity and output match but unfortunately with such a small transistor, the linearity is never up to spec.

Instead of manually tuning the size of the transistor and resistor combination, the ADS optimizer can be used to improve the output match and OIP3 by simultaneously sweeping the size of the FET and feedback resistor used in the output buffer. The goals of the optimizer are OIP3 of better than 20 dBm and S(2,2) of less than -15 dB at the center frequency. The optimizer gives a transistor with 3 gate fingers each being 40 μm long and 200 Ω feedback resistor. The complete LNA has an OIP3 of at least 15 dBm for all three bands. This is less than the target OIP3, but to keep the DC current draw low, the linearity has to be sacrificed. An output match for the two upper bands is within 1 dB of the goal. The output match of the lower band is sacrificed. The DC current draw ends up being nearly three times the original amount by drawing 28 mA. The schematic for the output buffer is shown in Figure 4.31.

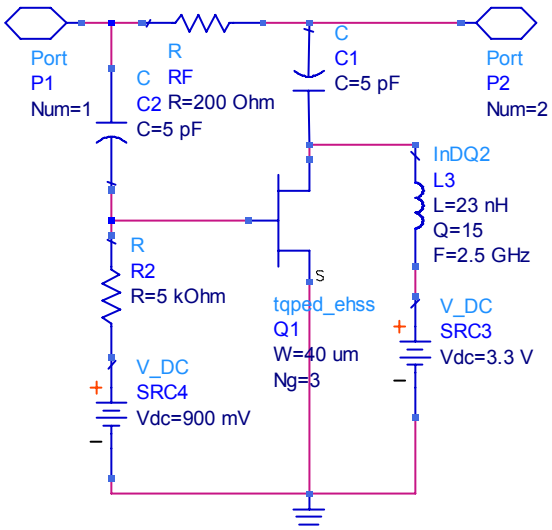


Figure 4.31 - Cascode LNA Output buffer

The bias circuits for both common-source transistors are made from the current mirrors discussed in section 4.7. The sizes of the transistors in the current mirror are tuned to give the appropriate 500 mV and 900 mV. These are then used as the gate-source bias voltages for the common-source stage of the cascode and output buffer, respectively. The bias for the common-gate stage does not need to be as well controlled and a resistive divider is satisfactory.

An additional high-pass filter at the output helps squelch the resonance created by the bond wire and on-chip power supply capacitor. The filter is a three element high pass filter with a f_{3dB} point of 2 GHz. The filter is designed using a maximally flat low-pass prototype and transformed to into a high-pass filter [17]. The schematic for the filter is shown in Figure 4.32.

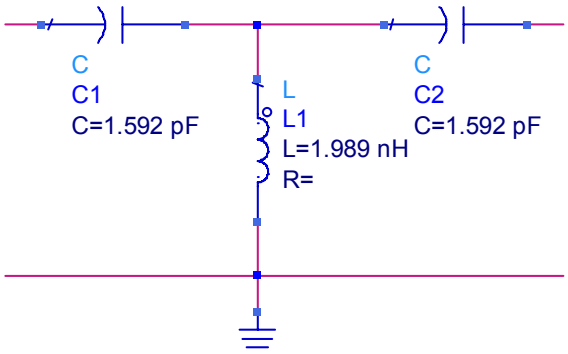


Figure 4.32 - Third order 2 GHz maximally flat high-pass filter

A full schematic of the LNA including bias circuits and ESD protection is shown in Figure 4.33.

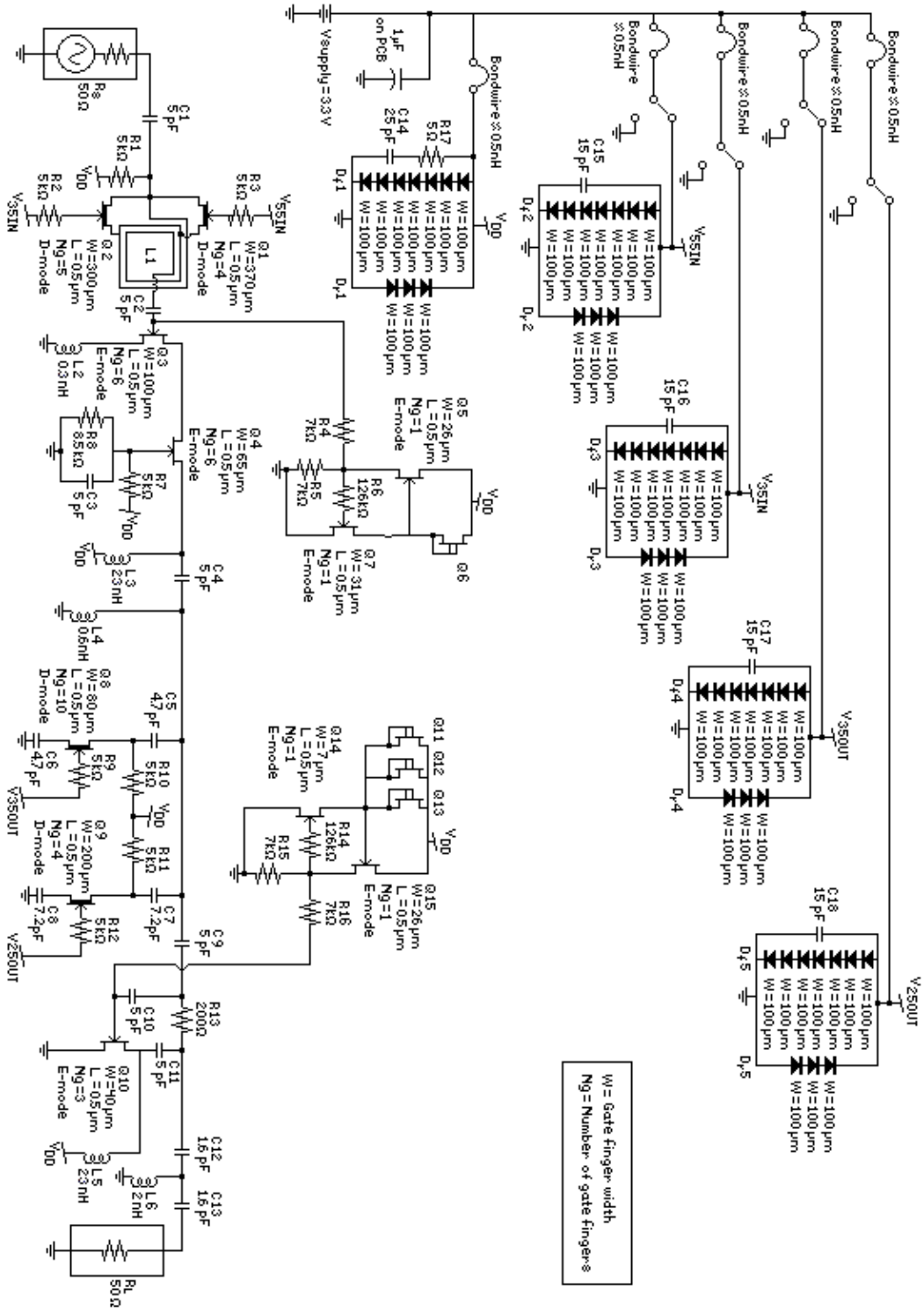


Figure 4.33 - Full LNA Schematic

Figure 4.34 summarizes the S-parameter simulation results of the LNA. The results are summarized in Table 4.4 and Table 4.5. The capacitors and inductors are simulated, one component at a time, in the electromagnetic simulator and their resulting two-port S-parameters are used in the schematic simulations. The complete set of simulation results can be found in appendix A2.

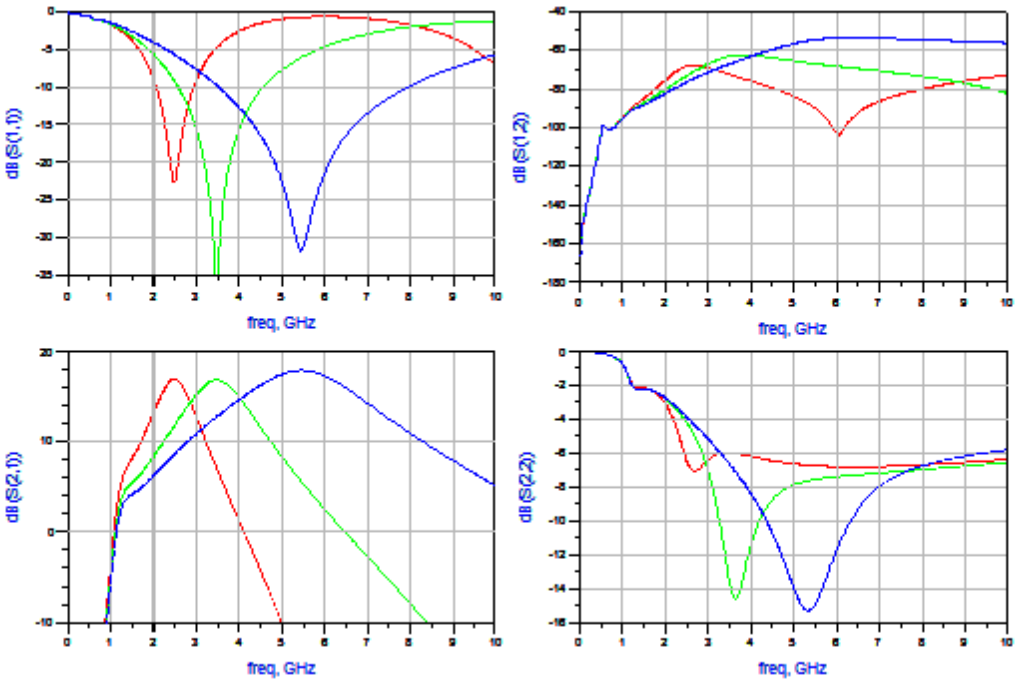


Figure 4.34 - Summary of LNA S-parameter simulations

Table 4.4 - Summary of LNA schematic simulations

Freq [GHz]	Gain [dB]	Input Match [dB]	Output Match [dB]	Noise Figure [dB]	IIP3 [dBm]	OIP3 [dBm]	Input P_{1dB} [dBm]	I_{DC} [mA]
2.5	16.98	22.84	7.04	2.08	-1.12	15.82	-11.5	42.36
3.5	16.85	36.72	14.6	2.74	0.94	17.77	-9	42.36
5.5	17.91	31.75	15.32	3.15	1.28	19.17	-8.5	42.36

The measurement frequencies for the 2.5 GHz intermodulation test were 2.495 GHz and 2.505 GHz. For the 3.5 GHz intermodulation test the measurement frequencies were 3.495 GHz and 3.505 GHz and for the 5.5 GHz intermodulation test, the test frequencies were 5.495 GHz and 5.505 GHz.

Table 4.5 compares the in-band and out-of-band gain for the LNA in its three different operating states. The low-band shows the best out-of-band rejection and the high band shows the worst rejection.

Table 4.5 - Gain of LNA in-band and out-of-band

Transducer Gain [dB]			
	Freq = 2.5 GHz	Freq = 3.5 Ghz	Freq = 5.5 GHz
Low Band Operation	**16.98**	6.96	-17.95
Mid Band Operation	11.89	**16.85**	5.44
High Band Operation	8.67	12.87	**17.91**

4.14 Two-Band LNA versus Two Single-Band LNAs with Switches

It is useful to compare the new reconfigurable LNA design to a previous standard. Instead of having a reconfigurable LNA, traditional receivers have a switching network and several single-band LNAs. The switches control which LNA is in the receiver chain. A block diagram of this is shown in Figure 4.35.

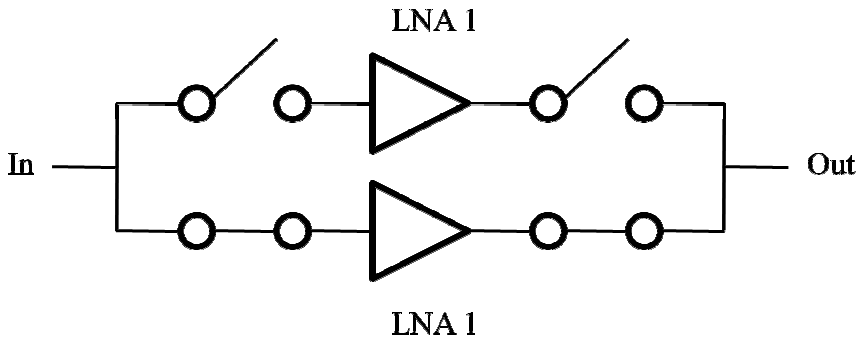


Figure 4.35 - Block diagram of switches and LNAs

For comparison purposes two systems were designed and simulated in ADS. One system had two single-band LNAs designed to operate at 2.5 GHz and 5.5 GHz. A SPST switch was also designed using a series-shunt-series configuration. The four switches and two LNAs were combined to form a section of a receiver front end. A two band reconfigurable LNA was also designed to operate at the same frequencies. The goal of the simulation is compare the traditional approach of LNA and receiver design to the newly proposed approach. The key differences between the two design is the location of switches in the circuit, the size of the switches, and the complexity of the switches. For the reconfigurable LNA, the switches are single FETs. For the traditional design, each switch needs 3 transistors to ensure low "On" resistance and good "Off" isolation. If a single FET is used as a switch in the traditional design, one of the two parameters

mentioned prior is insufficient for acceptable performance. For example, if the FET is large, the switch has a low "On" resistance but the parasitic capacitance is so large that the "Off" isolation is unacceptable. The parasitics of the switch ruin the input match that the LNA that is on presents to the input port. Since the input match is ruined, the noise figure is also worsened. The gain shape remains uneffected.

For simulation purposes, the resistors and capacitors are ideal, linear passive components. The inductors are individual electromagnetic simulations. The transistors are 0.5 µm TriQuint GaAs pHEMT models.

The schematic of one of the switch blocks is shown in Figure 4.36. Depletion mode pHEMTs are chosen because they have a lower "On" resistance than their enhancement mode counterparts. To simplify the analysis the effects of the bond wires and ESD circuitry are ignored.

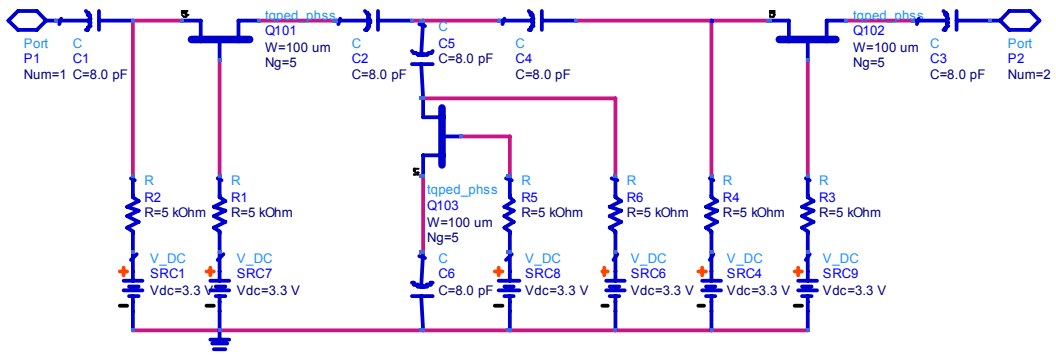


Figure 4.36 - Schematic of three FET switch

The schematic of the 2.5 GHz LNA is shown in Figure 4.37 and the 5.5 GHz in Figure 4.38. The only differences between the two circuits are the values of the components. Otherwise, the circuits are the same. They are the same type of cascode and output buffer as used prior.

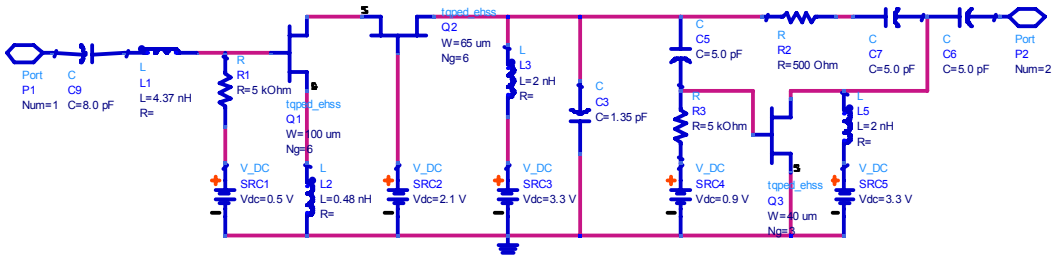


Figure 4.37 - Schematic of low-band cascode

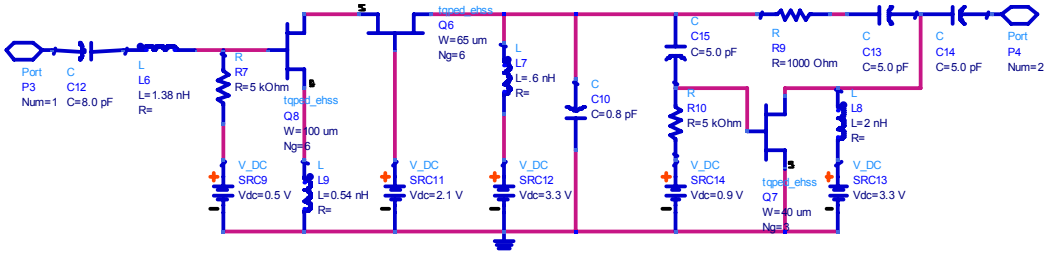


Figure 4.38 - Schematic of high-band cascode

The schematic of the reconfigurable LNA is shown in Figure 4.39 and is very similar to cascode in section 4.13. The major difference is that this LNA only operates over two bands instead of three bands. The input gate inductor is shown in Figure 4.40. This inductor only has one additional tap that is connected to a FET switch to short out a portion of the inductor traces.

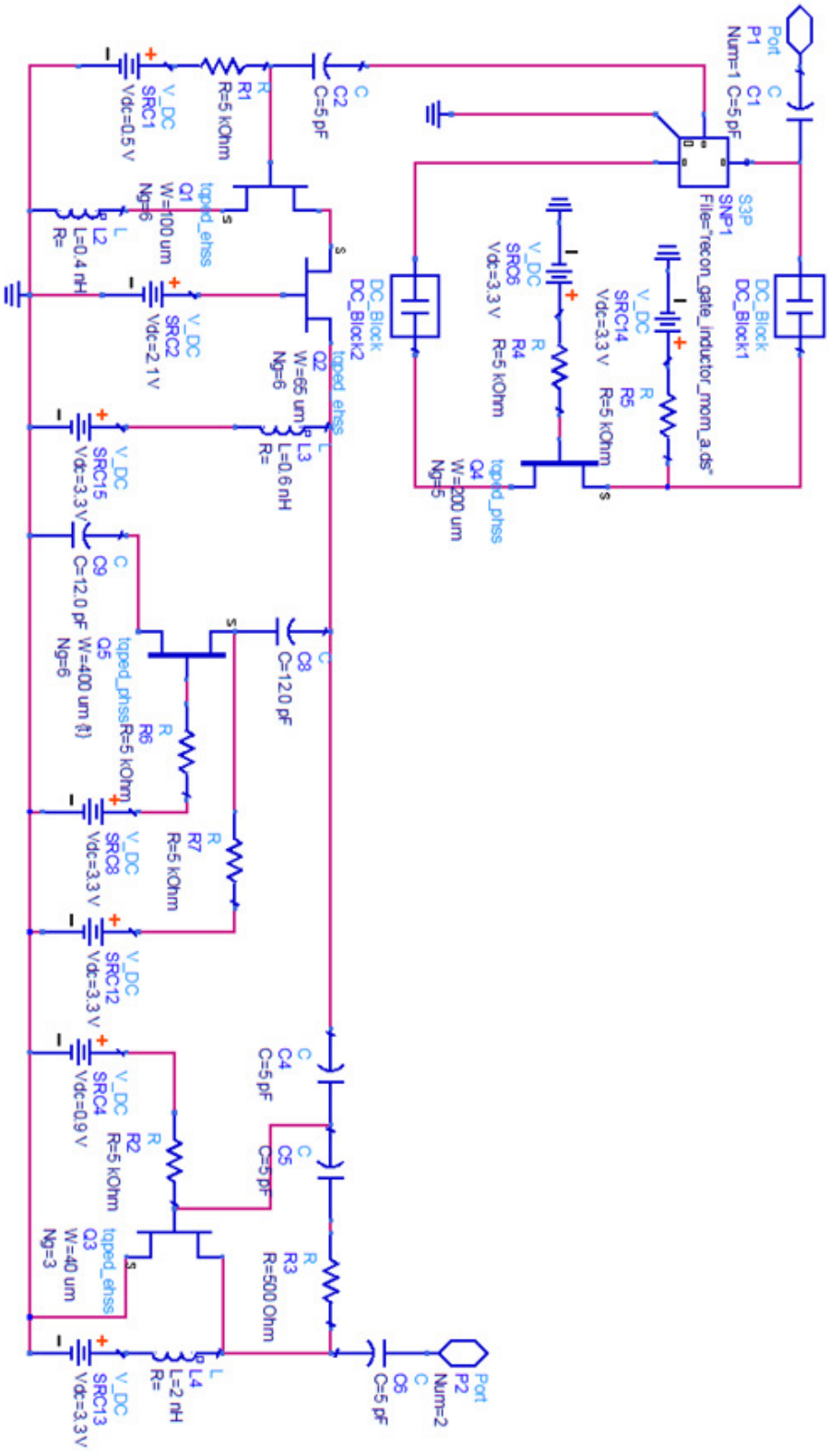


Figure 4.39 - Schematic of reconfigurable 2 band LNA

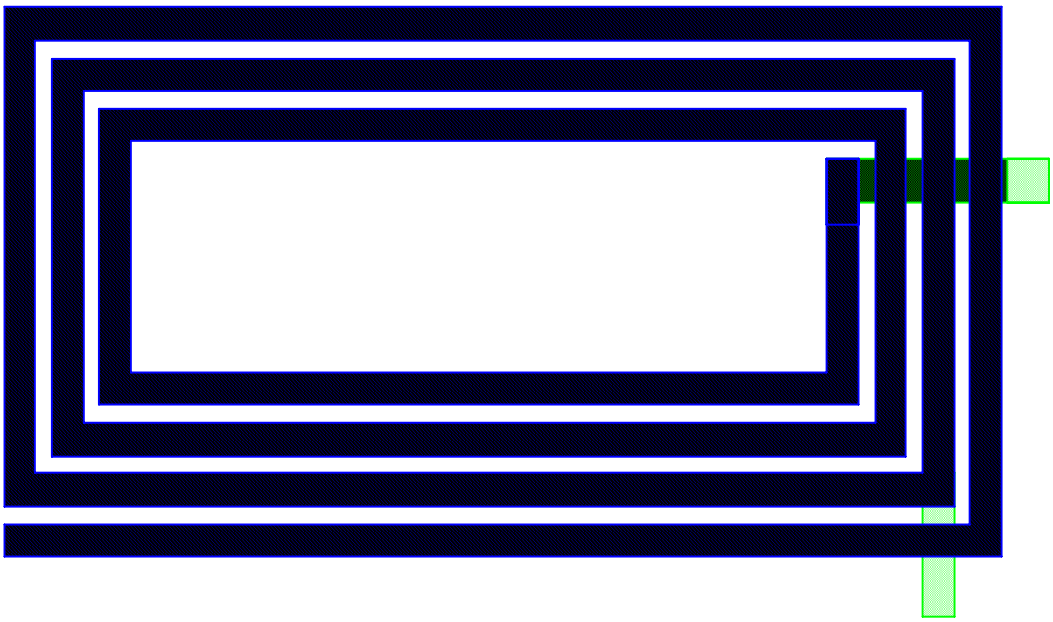


Figure 4.40 - Drawing of input spiral inductor for reconfigurable LNA

The simulation results for both circuits are compared side by side in Figure 4.41 and Figure 4.42 and the results are summarized in Table 4.6.

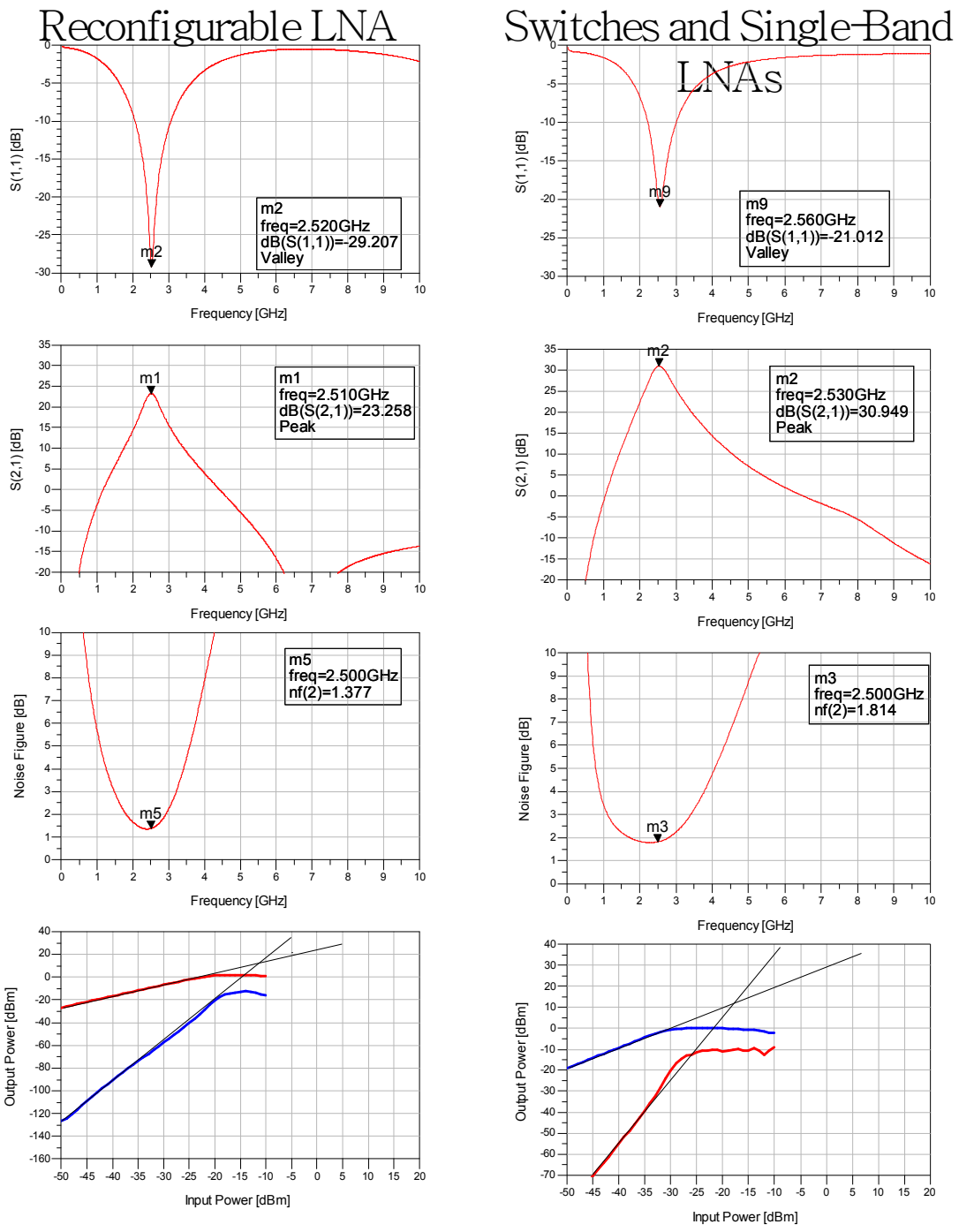


Figure 4.41 - Low-band comparison of reconfigurable LNA versus traditional LNA

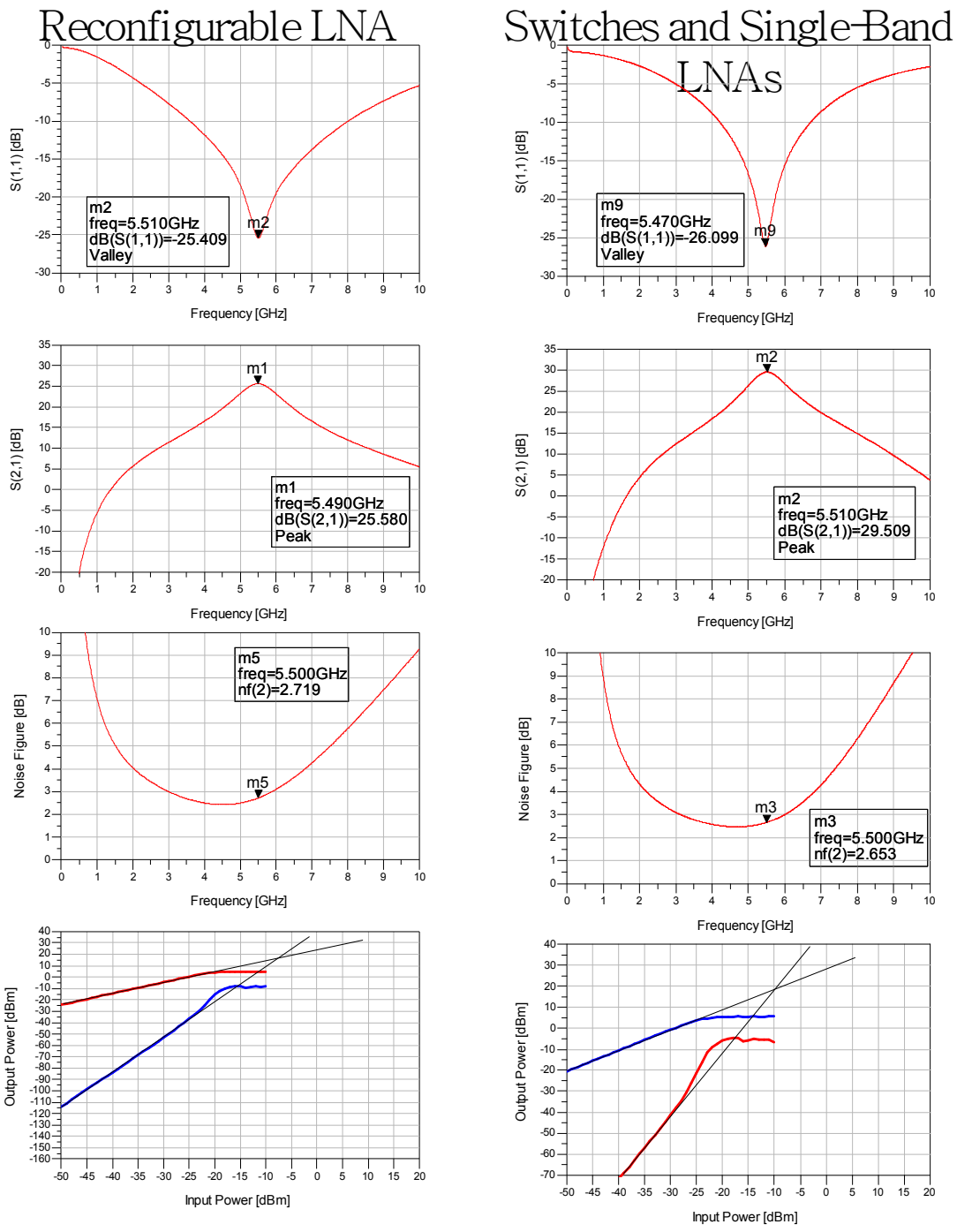


Figure 4.42 - High-band comparison of reconfigurable LNA versus traditional LNA

Table 4.6 - Comparison of reconfigurable LNA versus traditional LNA with switches

	Reconfigurable LNA	Reconfigurable LNA	Traditional LNA and Switches	Traditional LNA and Switches
Frequency [GHz]	2.5	5.5	2.5	5.5
Input Return Loss [dB]	29.2	25.4	21	26.1
Gain [dB]	23.3	25.6	30.9	29.5
Noise Figure [dB]	1.4	2.7	1.8	2.7
IIP3 [dBm]	-10	-7.8	-18	-10
OIP3 [dBm]	13	16	13.7	19
Input P1dB [dBm]	-17.2	-15.7	-17.2	-18.7
Output P1dB [dBm]	5	8.8	4.1	9.8
I_{DC} [mA]	36.6	36.6	36.7	36.7

Several interesting conclusions can be drawn from the comparison above. First, the input match and noise figure for both circuits are good over both bands. The input match is better than 20 dB in all four scenarios. For the low-band, the noise figure is always better than 2 dB and at high band better than 3 dB. The major discrepancy starts with the difference in gain between the reconfigurable architecture and the traditional LNA architecture. The problem stems from the Q factor of the capacitors in the LC tank between the cascode and the output buffer. In the reconfigurable architecture, the Q of the capacitors is lowered because of the switching FET resistances. In the circuit in Figure 4.39, in low-band operation, the Q of the switchable capacitor is only 12 at 2.5 GHz.

For the linearity, the output compression powers and OIP3 powers are similar between the new and traditional circuits. The input powers are less for the traditional topology because of the additional gain. The output buffer is main limiting factor of the linearity of the circuit. Because there is a significant amount of gain from the cascode, the output buffer must deal with large signals.

The difference in DC current between the circuits is due to different sized inductors that connect the drain of the cascode to the voltage supply. The switches do not draw a significant amount of current.

One of the advantages of the reconfigurable circuit is that it should require less die area because a large amount of circuitry is reused instead of duplicated. The list of large reused components includes the DC choke inductors, cascode FETs, cascode gate inductor, DC blocking capacitors, DC bypass capacitors, and ESD diodes. The total die space required for all these components for a single band LNA is approximately 430,000 μm^2 if simply placed side by side. A list of the components and their sizes can be found in the appendix. To make the LNA reconfigurable by adding a second band of operation, the circuit would need to be increased in size to approximately 580,000 μm^2. The additional space is required for additional FET switches, more ESD protection and more large DC bypass and blocking capacitors. In comparison, two single-band LNAs would require 860,000 μm^2 in addition to the area required for the series-shunt-series switches. Each series-shunt-series switch adds an additional 37,500 μm^2 and 4 switches are required totaling an additional 125,000 μm^2. In total, two single band LNAs and 4 switches would require over 1,000,000 μm^2 in comparison to the 580,000 μm^2 required for the reconfigurable LNA. The two band reconfigurable LNA is nearly 50% smaller

than the traditional approach. The space saving benefit of the reconfigurable LNA is further enhanced as more bands of operation are added because the additional space required for the reconfigurable LNA is much less per added band of operation.

There are also drawbacks to the new design, though. The reduction in gain due to the low Q capacitors is one problem. Also, if the specifications for the LNA are very rigorous, such as a large amount of rejection at a particular frequency (such as a harmonic of the operating frequency or possible strong interferer), the separate LNAs are easier to design because any additional circuitry added will not affect the behavior of the receiver in other operating modes.

4.15 Layout of three Band LNA

The physical layout of an LNA is a fundamental factor in determining its performance. There are many factors that influence circuit behavior including the sizes and shapes of components and where they are located in relation to each other. Software simulations help predict performance as well. Full simulations of all passive components are possible with Agilent's Momentum simulator.

The passive components used in the LNA include resistors, capacitors and inductors. Other structures include bond pads and ground vias. Resistors are made from a single layer of resistive material including Nichrome resistors (50 ohm / square) and a high resistance material (320 ohm / square). Bond bands are three metal layers thick and ground vias reach from the top metal layer to the back of the substrate in order to reach the ground plane of the PCB underneath the die.

MIM capacitors are made from sandwiching dielectric between metal plates and produce a capacitance of 630 pF/ mm^2. Spiral inductors are made from a rectangular spiral structure of a 4 µm thick metal layer. Since GaAs is a semi-insulating substrate, the Q factor of the inductors can reach as high as 30 in comparison to the Q of 5-10 commonly found in silicon RFICs.

The FETs are a multi-finger pHEMT devices with a 0.5 µm gate length. The process used supports both enhancement mode and depletion mode pHEMTs. A cross sectional view of the die is shown in Figure 4.43.

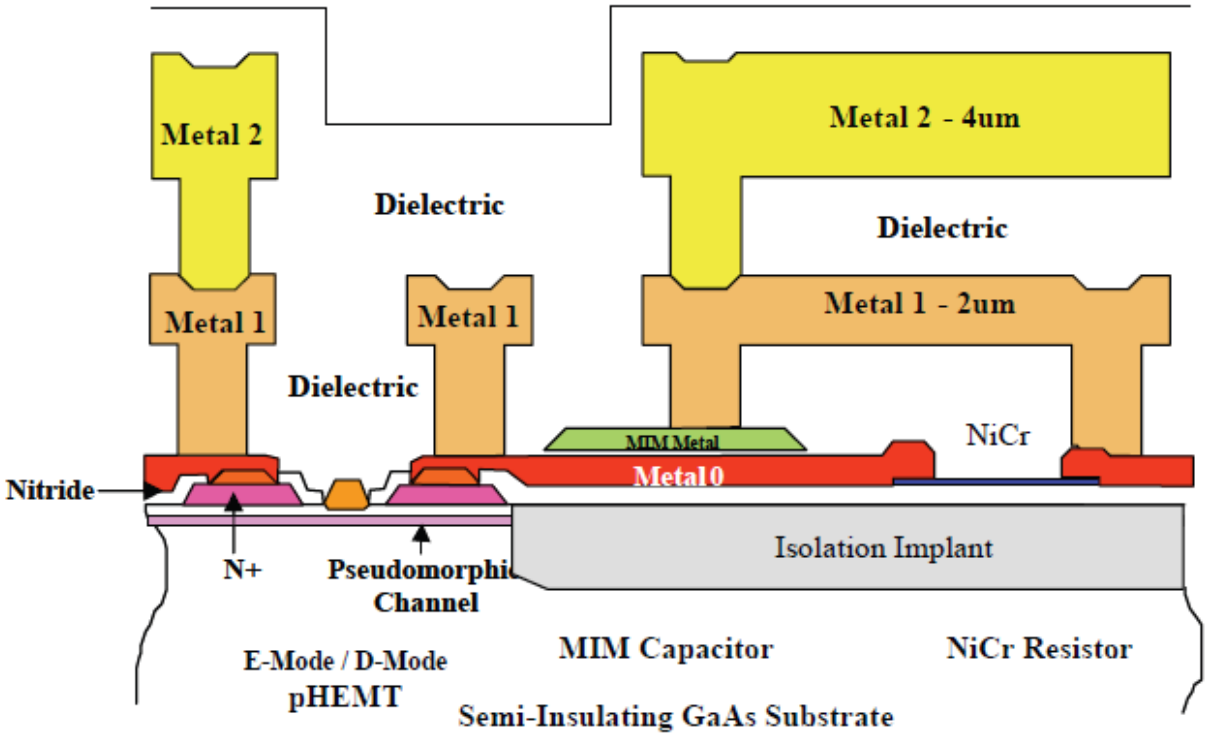


Figure 4.43 - Cross section of die [18]

To layout the LNA described in section 4.13, the first step is to set a goal size for the layout. For this design, 2 mm by 1 mm was the goal. The final design fit into a rectangle 1.85 mm by 1 mm for a total area of 1.85 mm^2. The final layout that was

fabricated as shown in Figure 4.44. Each circuit component is labeled with respect to the schematic diagram in Figure 4.33 on page 93. The components labeled "SVIA" are the substrate vias that go all the way through the substrate and typically contact the ground plane of the PCB or package to which the circuit die is attached. The ESD diodes are labeled as groups of series-connected diodes to minimize clutter.

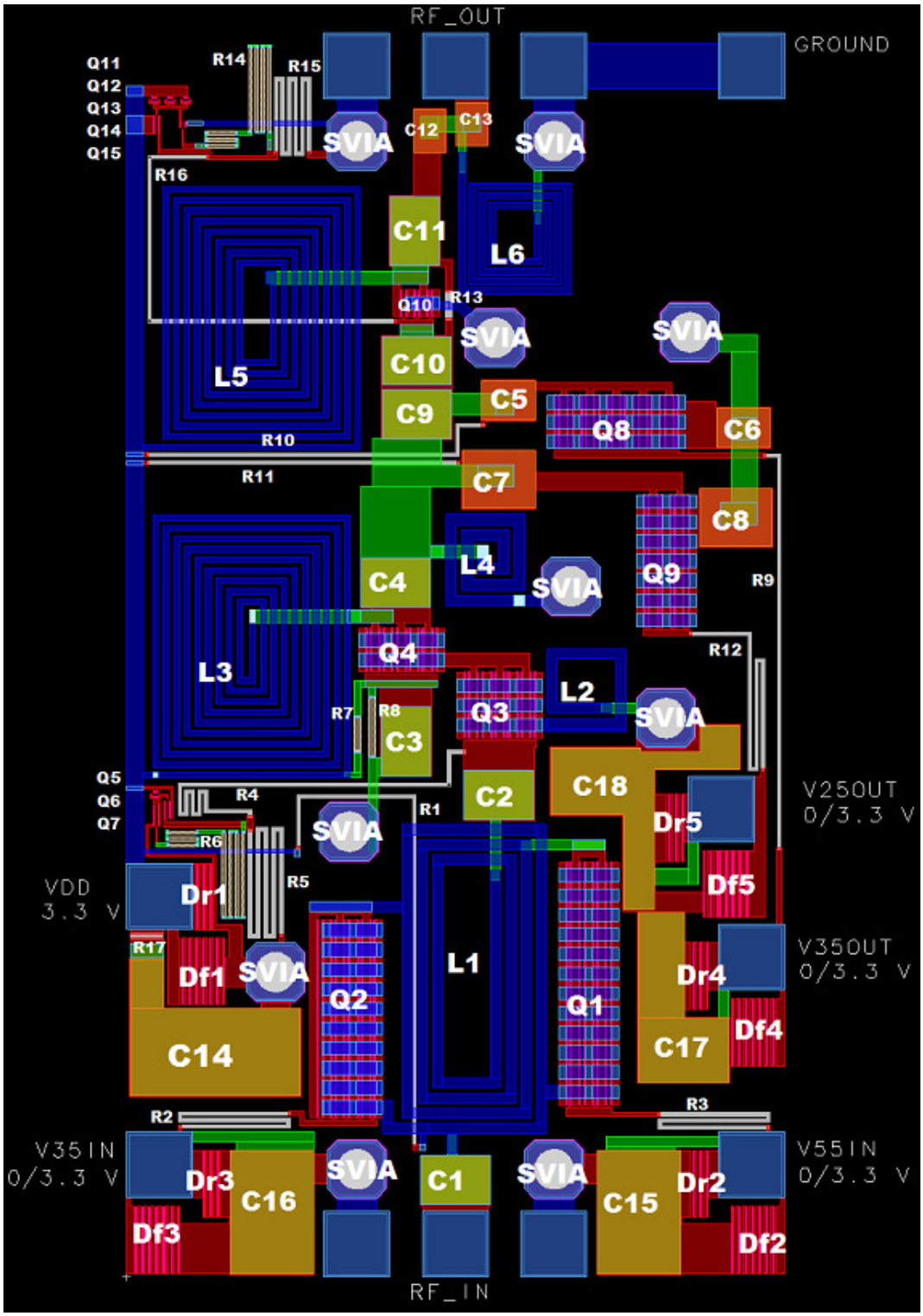


Figure 4.44 - LNA Layout

The input ground-signal-ground structure is at the bottom of the figure and the output is taken from the GSG structure at the top of the figure. The GSG structure supports the use of a probe station with a 150 μm pitch probes. The three pads are 100 μm square. The outer pads are shorted to ground with the substrate vias (octagons). The middle pad connects to the 5 pF DC blocking capacitors which subsequently connects to the switching inductor. The large switching transistors lie to either side of the inductor.

Both the bottom left and right corners contain the ESD circuitry. The 10 diodes and 15 pF capacitors make up a large portion of the die contents.

The cascode transistors are in the center of the layout. Above the cascode are the switching capacitors and their associated large switching transistors. The output buffer lies above the switching capacitors. Finally, the top GSG structure allows a probe station to probe the output signal.

The bias circuits are on the left side of the layout. They are above and below the large spiral drain inductors.

The circuit contains six spiral inductors. The spiral inductors take up a large portion of the die. In laying the circuit out, the spirals were separated as far apart as possible to avoid any mutual coupling. In an earlier design, the two smaller spirals in the middle of the layout were close together. EM simulations showed they were coupling. By moving them over 100 μm apart, the coupling lessened and the effect of the coupling waned.

The fabricated die is shown in Figure 4.45 mounted on the PCB with the bond wires for the DC signals soldered on. Figure 4.46 is zoomed out to show more of the PCB, and the on-board capacitor can be seen in the upper left corner. The dead space

(solid black area) above and below the circuit in the die were added for manufacturing reasons and the extra area is not included in the design spec. If the LNA were the only circuit to be fabricated on the wafer, the dead space would not be necessary and the die size would be smaller. The die with dead space is 1.8 mm in the horizontal direction shown in Figure 4.45 and 2 mm in the vertical direction. Without the dead-space, the die would be 1.8 mm in the horizontal and 1 mm in the vertical.

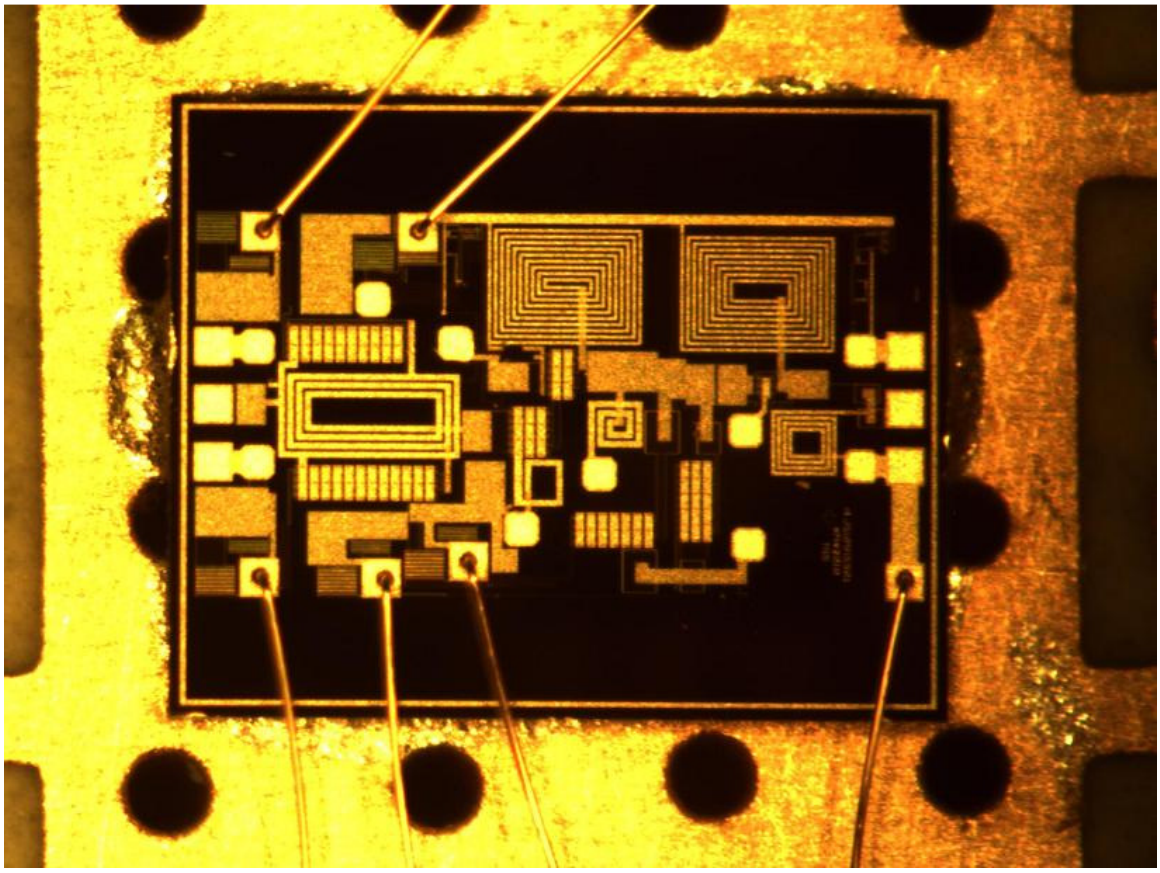


Figure 4.45 - LNA die on PCB - zoomed in

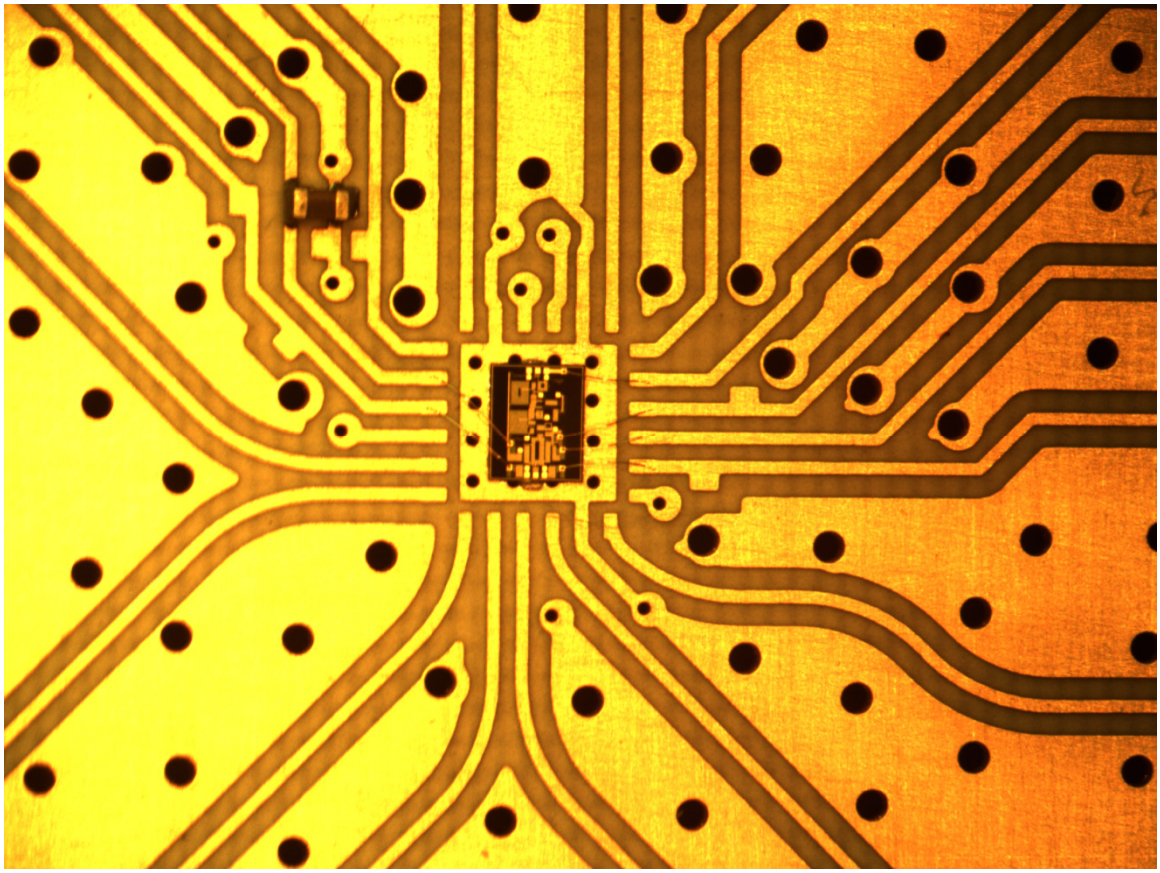


Figure 4.46 - LNA die on PCB - zoomed out

CHAPTER 5

MEASUREMENTS

5.1 Introduction

One-hundred and seventy four die were produced by TriQuint Semiconductor with the circuit layout in Figure 4.44 in section 4. Five printed circuit boards were manufactured. For each PCB, one die was soldered directly to the PCB pictured in Figure 5.1. The red area is copper and in the blue area the copper is trimmed off. An additional 1 μF surface-mount capacitor was soldered onto the board to smooth out the power supply current. This is shown in Figure 5.2 with a closer view of the center of the PCB. Figure 5.3 shows the die and bond wires that were soldered from the die to the PCB.

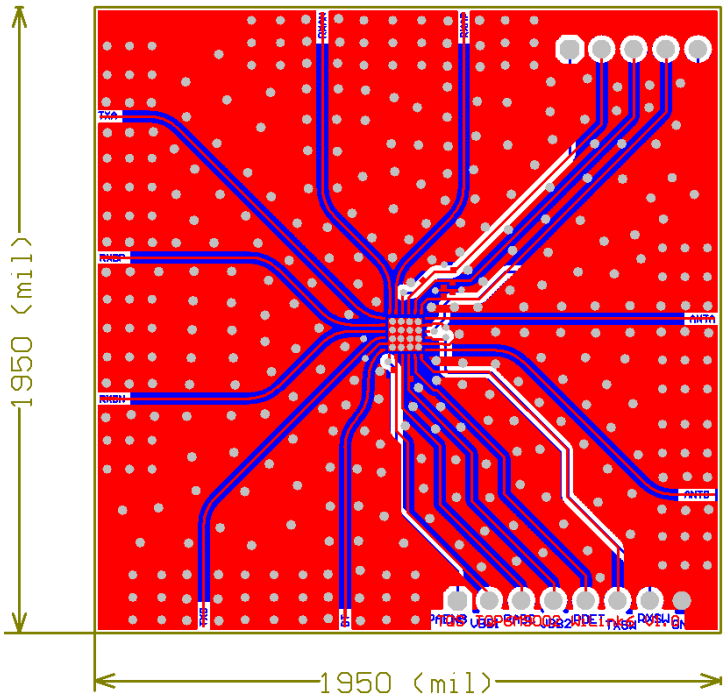


Figure 5.1 - PCB used for measurements

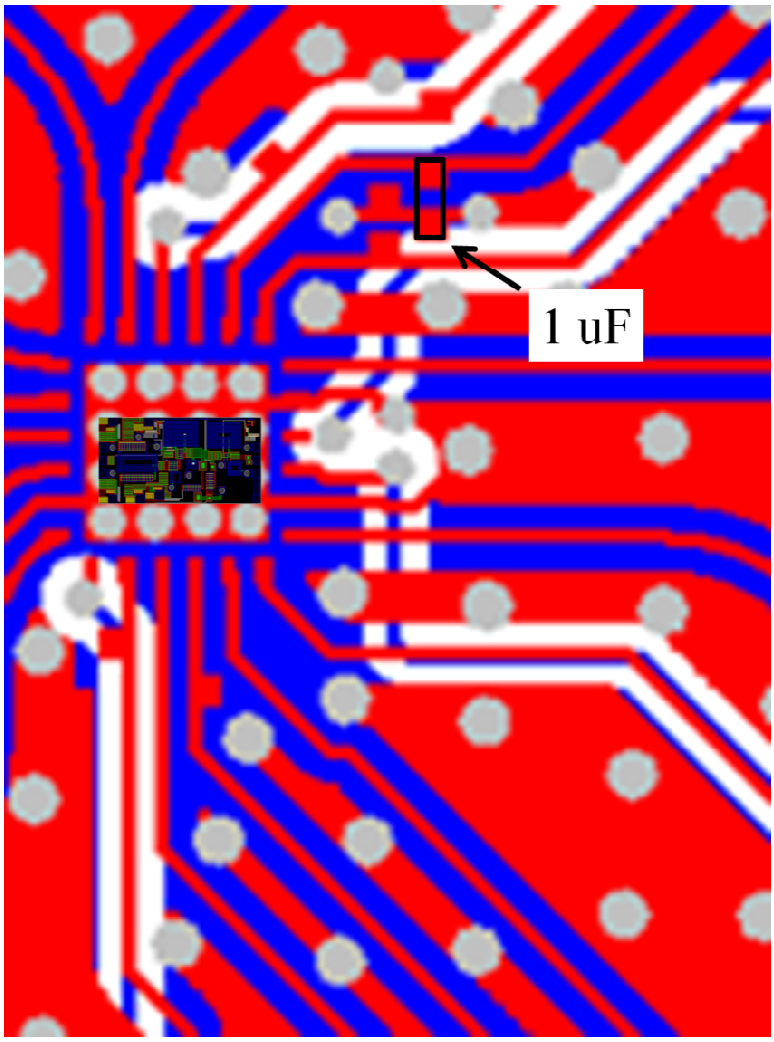


Figure 5.2 - PCB with SMT capacitor

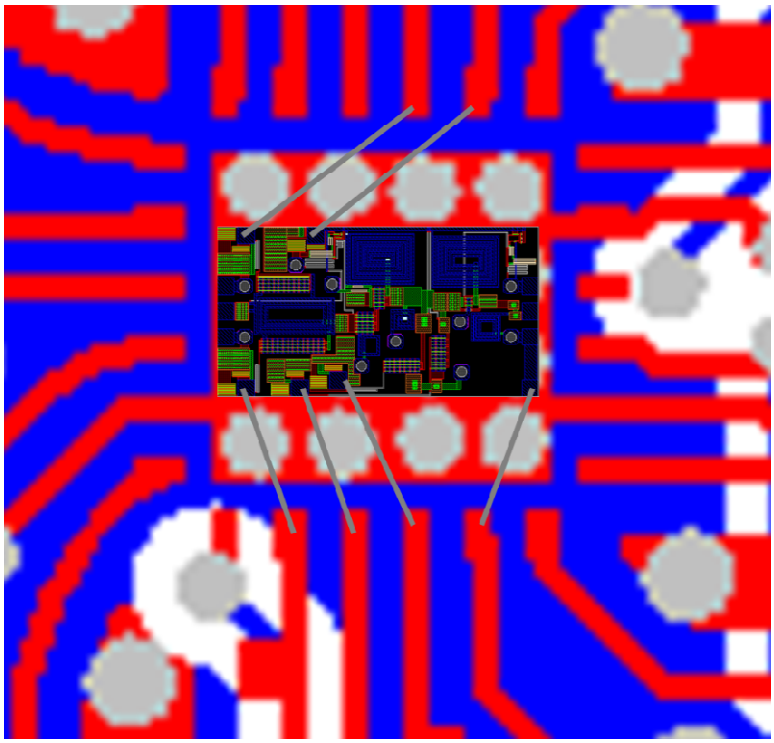


Figure 5.3 - PCB with bond wires and die

The PCBs were numbered 8256, 8257, 8258, 8259, & 8260 for easy identification. The DC power, ground, and DC control lines were wire-bonded directly to the PC board. The RF was not connected to the board and measured instead with a probe station. The input match of cascode, especially at higher frequencies, is greatly affected by the gate inductance, and wire-bonds add a significant amount of inductance. To avoid this effect, it was determined that the probe station would yield more accurate results. Also, the circuit die was not packaged. Package parasitics can also cause deviations in expected behavior. Without an enclosing package and with a little care to not destroy the IC circuit elements, the probe station measurements were a good choice.

The switches to control on-chip electronics were ubiquitous SPDT toggle switches. Each switch had three short wires soldered onto each lug. The wires were

plugged into a breadboard. The throws of the switch were attached to V_{DD} and ground. The pole of the switch went to the PCB which then ran to the circuit die through a bond wire. The onboard ESD diodes kept the IC safe from electrostatic discharge. The setup is shown in Figure 5.4.

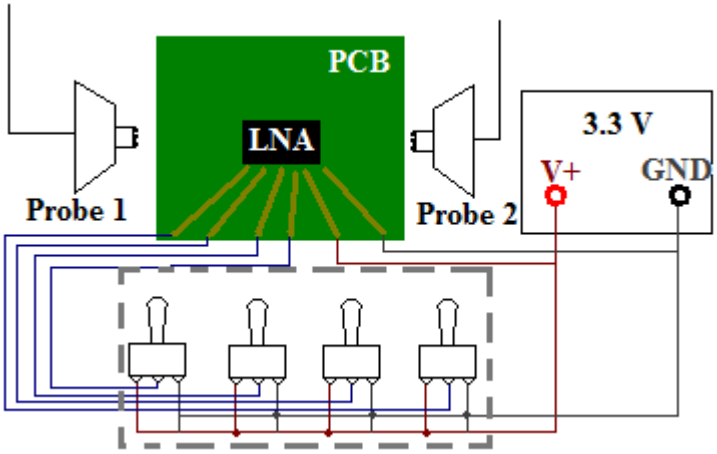


Figure 5.4 - Test setup for measurements

Four of the most important groups of circuit parameters were measured: S-parameters, noise performance, linearity, and DC power consumption. The S-parameters were measured using a network analyzer. Noise was measured with a noise figure analyzer that gave the noise figure of the LNA. The linearity was measured with a spectrum analyzer and yielded input and output intermodulation distortion and the P1dB compression point. DC current was measured with ammeter in series with the power supply.

The measurements took a toll on the five ICs. S-parameters were measured first. The probe tips destroyed the output matching network and landing pads of one of the ICs rendering it unable to be measured. Next the gain compression was measured during which another board unexpectedly quit working leaving only three complete sets of

compression measurements. The low-band and mid-band intermodulation measurements were completed, but the high-band measurements destroyed two more ICs leaving only one working IC for high-band intermodulation measurements. The noise figure was the last to be measured and was measured on the only remaining functional IC.

Great care has to be taken when using the probe station. One of the circuit dies was destroyed when probes were still landed on the die and one of the cables connected to the probe station was tugged on. The probe head only moved a few hundred micron but destroyed the output buffer by nearly smashing the circuit components.

5.2 Results

For S-parameter measurements on the network analyzer, the calibration was done at the interface of the probe tips. This was to remove any effects of the probes, the elbow connectors connecting the probes and cables, and the cables going to the network analyzer. Figure 5.5 through Figure 5.10 are the S-parameter measurements of four of the ICs at the three different bands of operation. The results are summarized in Table 5.1.

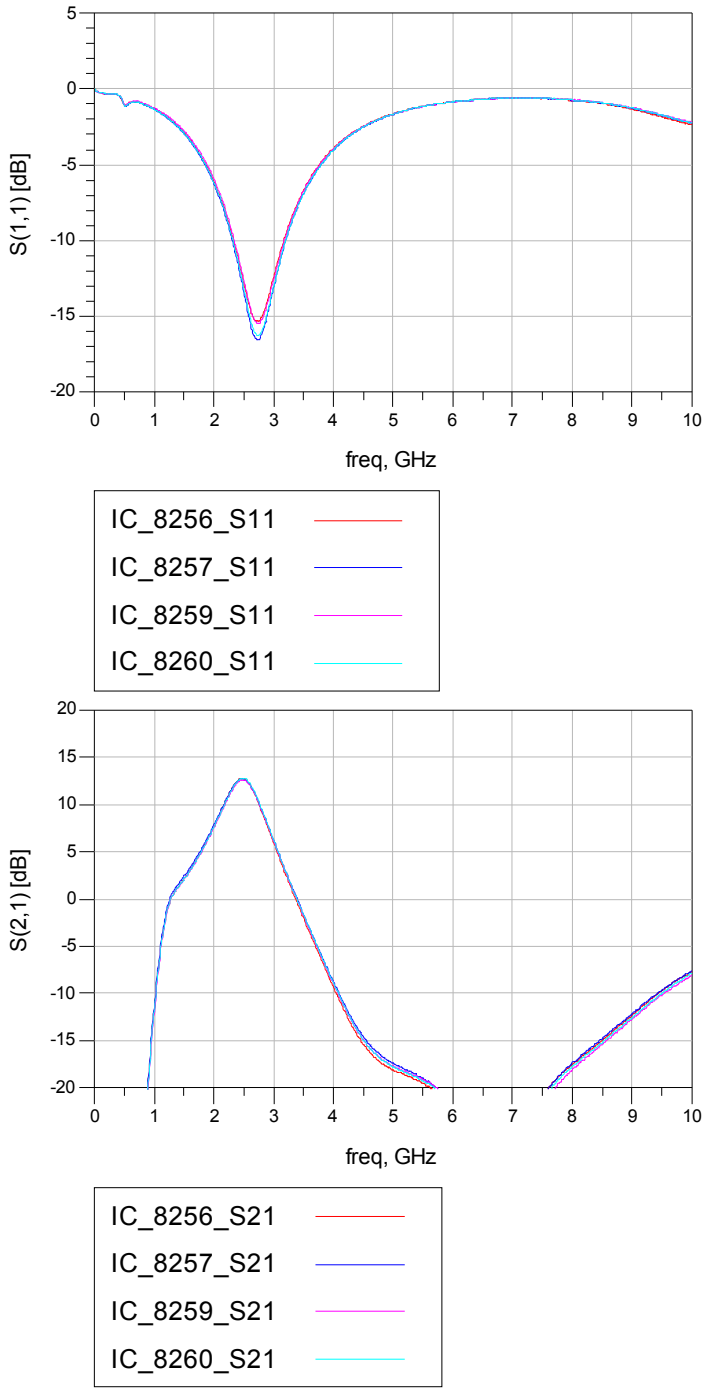


Figure 5.5 - Low band input match and gain

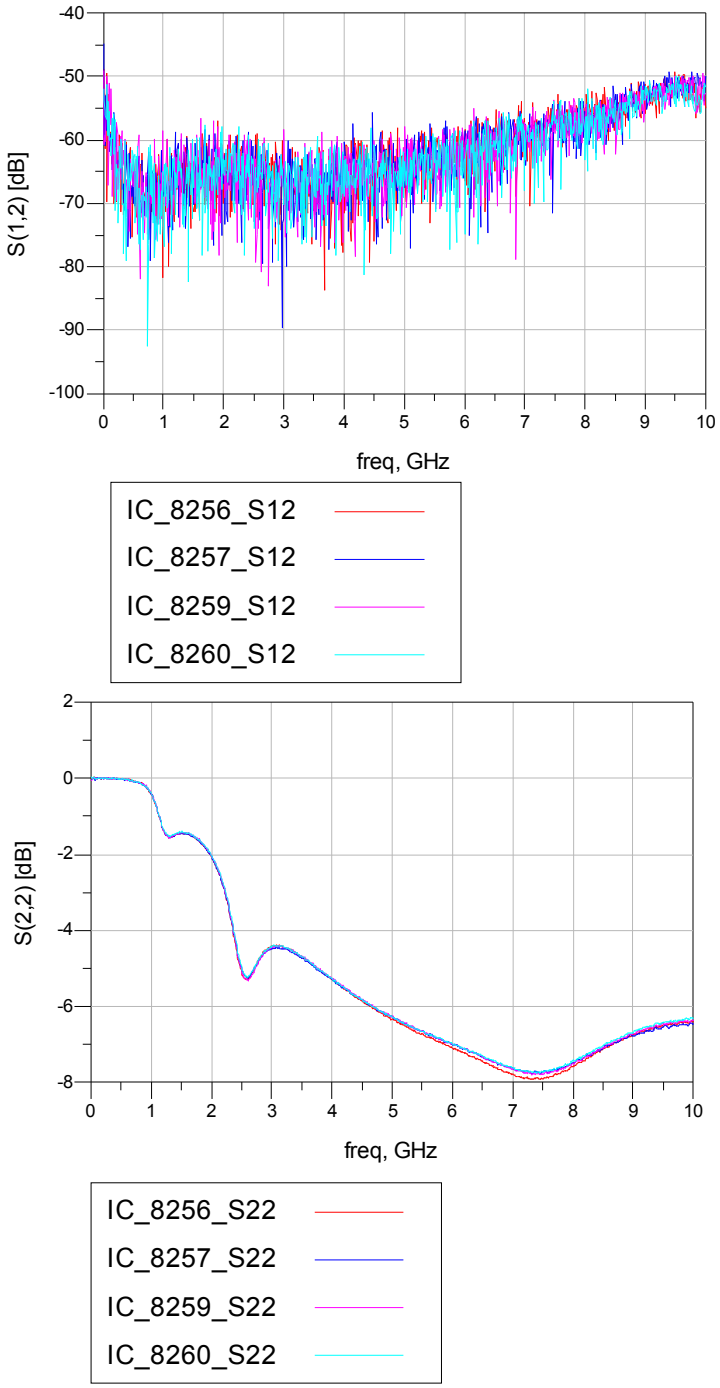


Figure 5.6 - Low-band isolation and output match

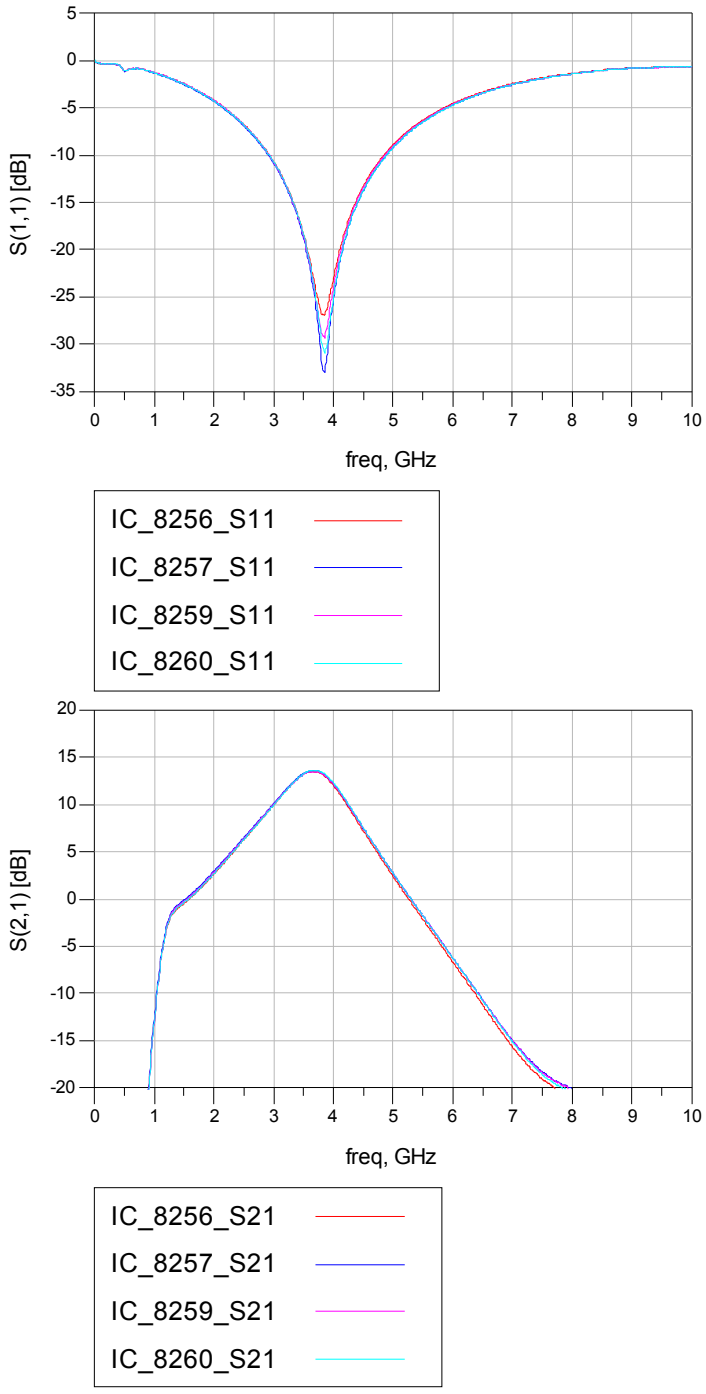


Figure 5.7 - Mid-band input match and gain

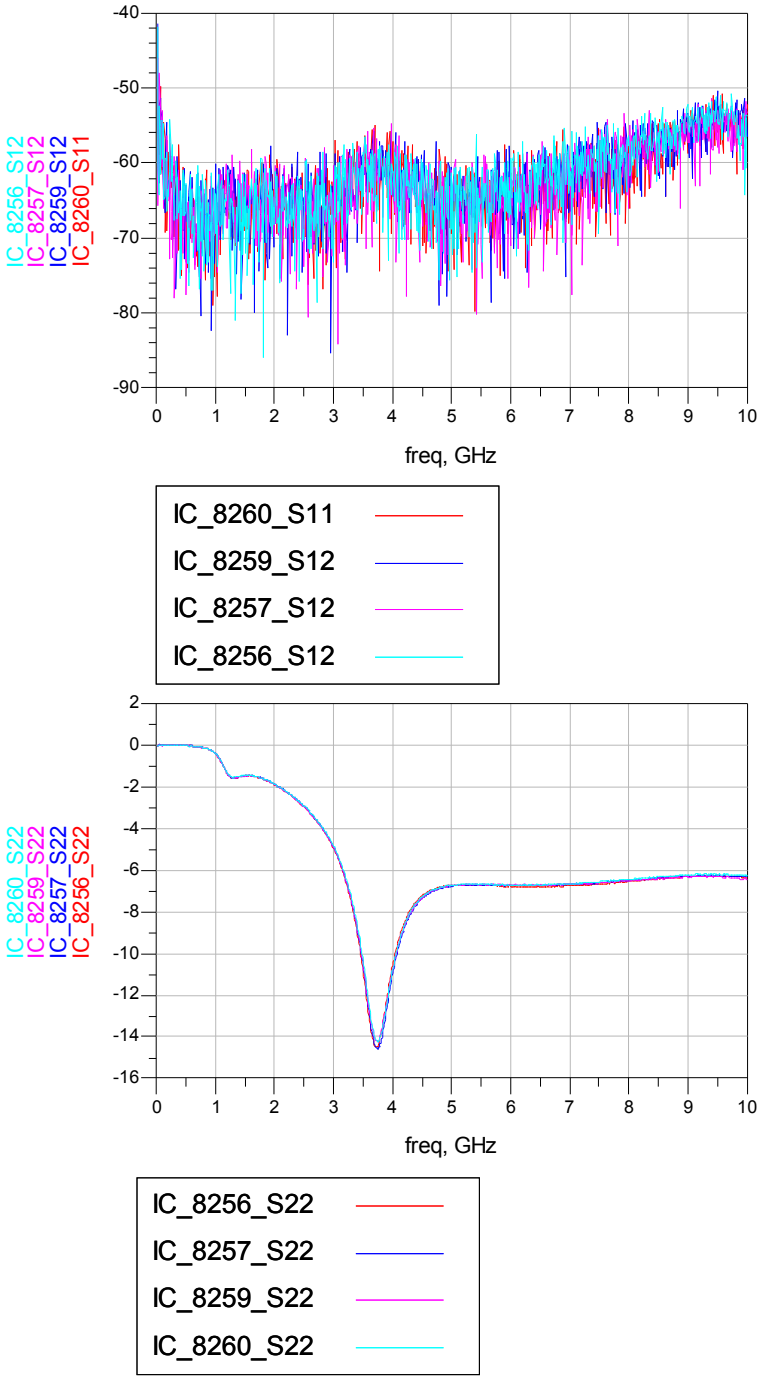


Figure 5.8 - Mid-band isolation and output match

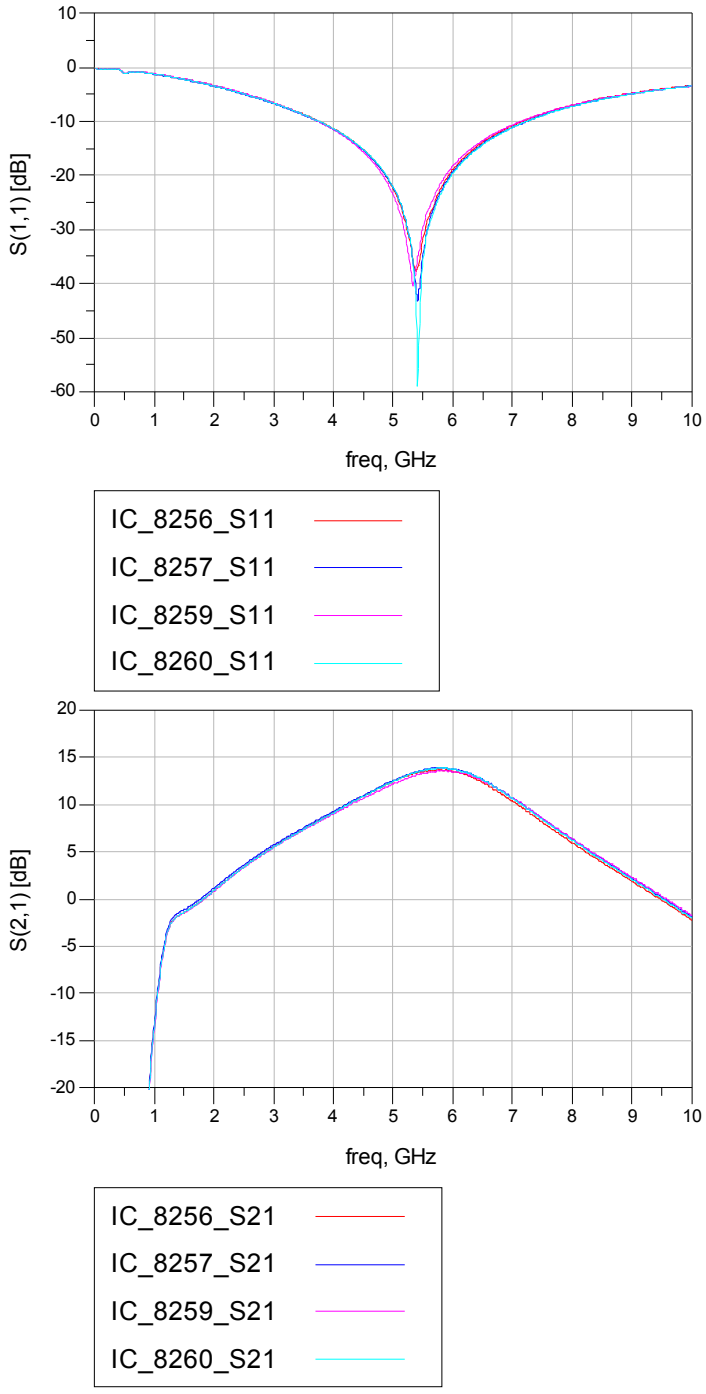


Figure 5.9 - High-band input match and gain

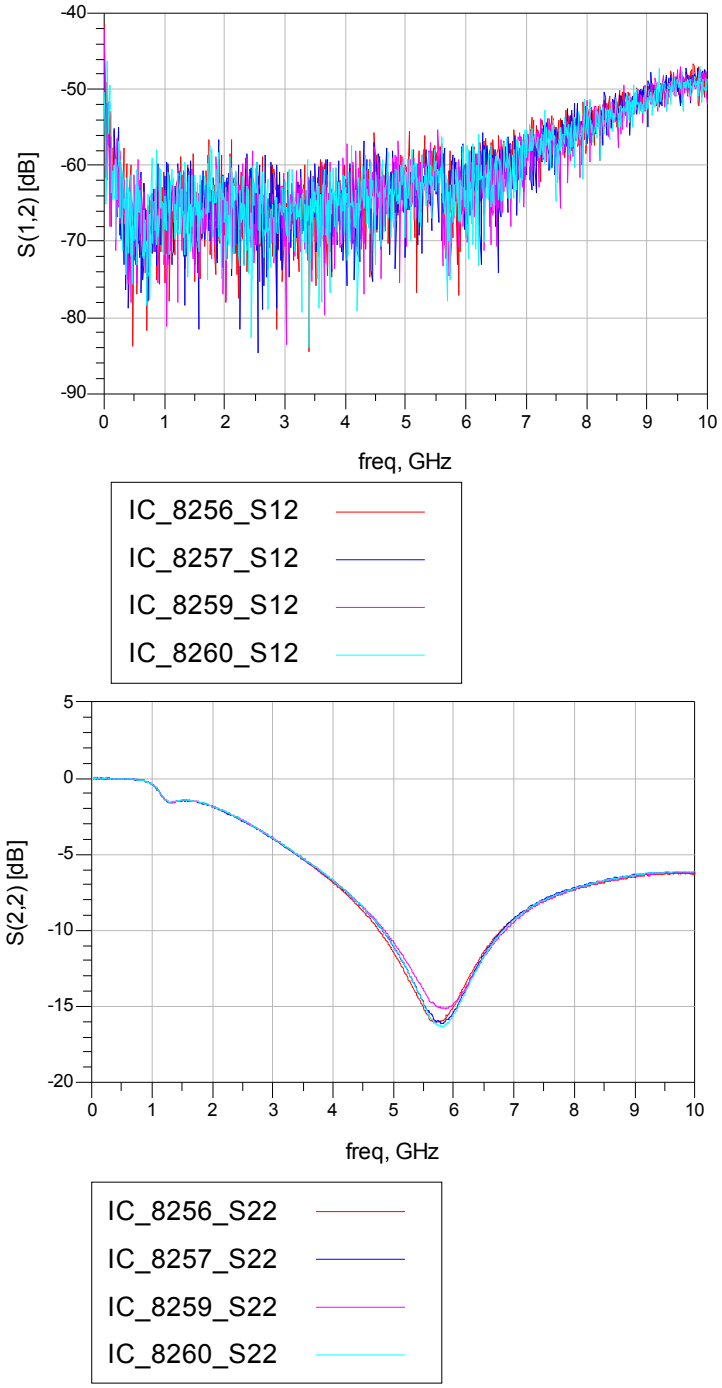


Figure 5.10 - High-band isolation and output match

Table 5.1 - Measured S-Parameter results

	Freq [GHz]	min(S(1,1)) [dB]	Freq [GHz]	max(S(2,1)) [dB]	Freq [GHz]	min(S(2,2)) [dB]
Low Band	2.7	-15.4	2.5	12.8	2.6	-5.3
Mid Band	3.88	-27	3.6	13.5	3.7	-14.5
High Band	5.4	-37.7	5.8	13.7	5.7	-16

To measure the third order intermodulation distortion, a two tone test was used with two tones 10 MHz apart centered at the frequencies 2.45 GHz, 3.65 GHz, and 5.85 GHz. Graphs of output power versus input power are shown in Figure 5.11 through Figure 5.13. For the low band and mid band graphs, the data points are the arithmetic average of measurements taken from three circuits. For the high band measurements, only one board was measured. Microsoft Excel linear trend lines were added to the data and the intersection point of the lines was used to calculate the intermodulation products. The IIP3 and OIP3 results are summarized in Table 5.2.

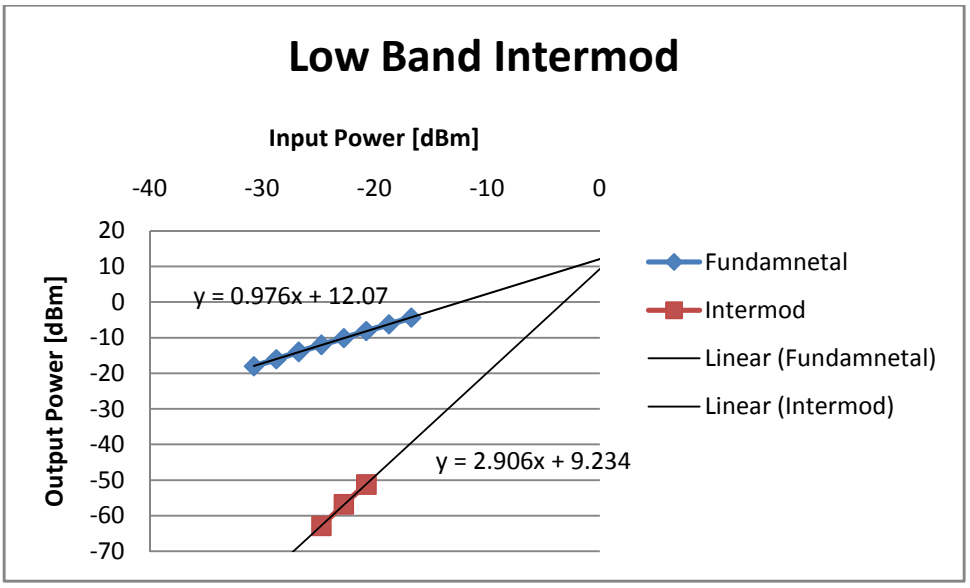


Figure 5.11 - Low band intermodulation

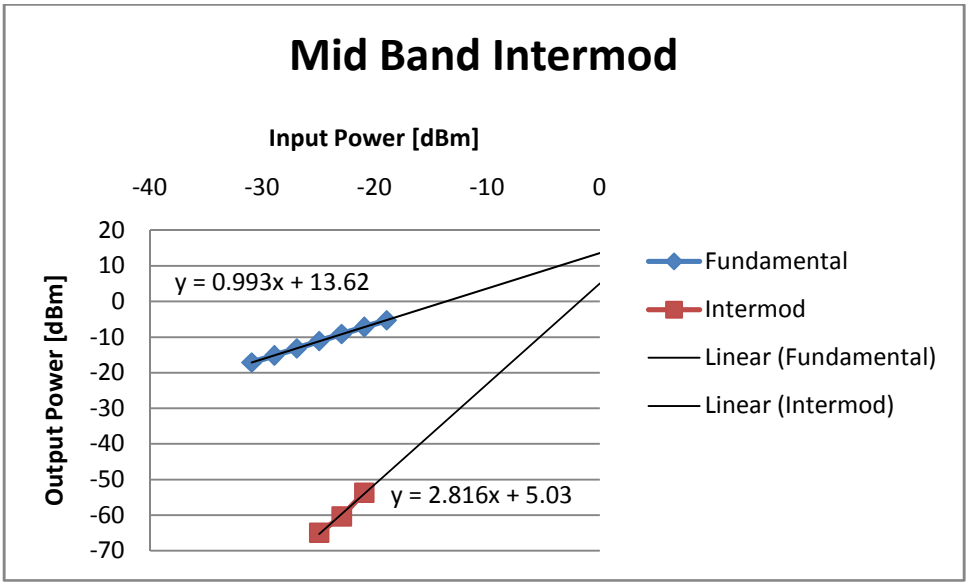


Figure 5.12 - Mid-band intermodulation

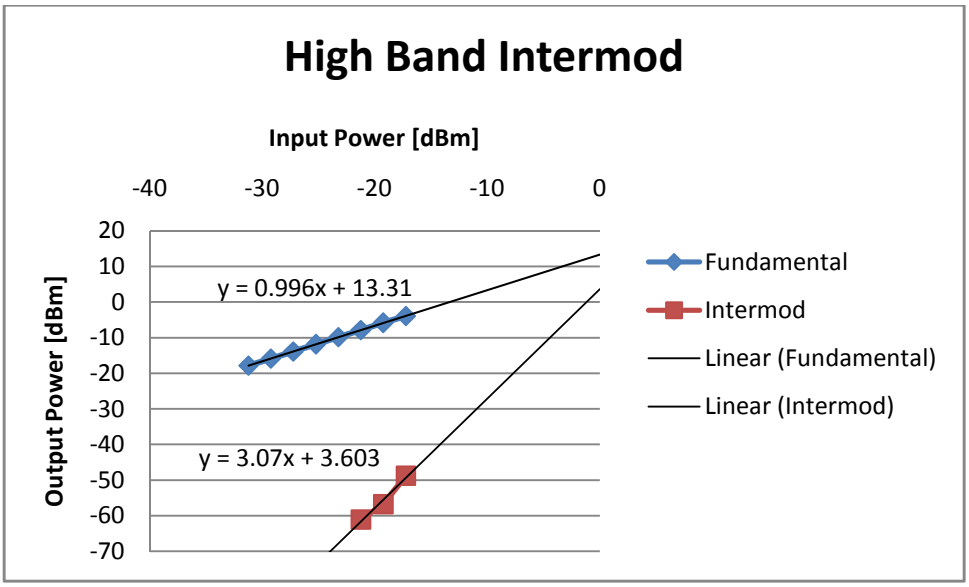


Figure 5.13 - Upper-band intermodulation

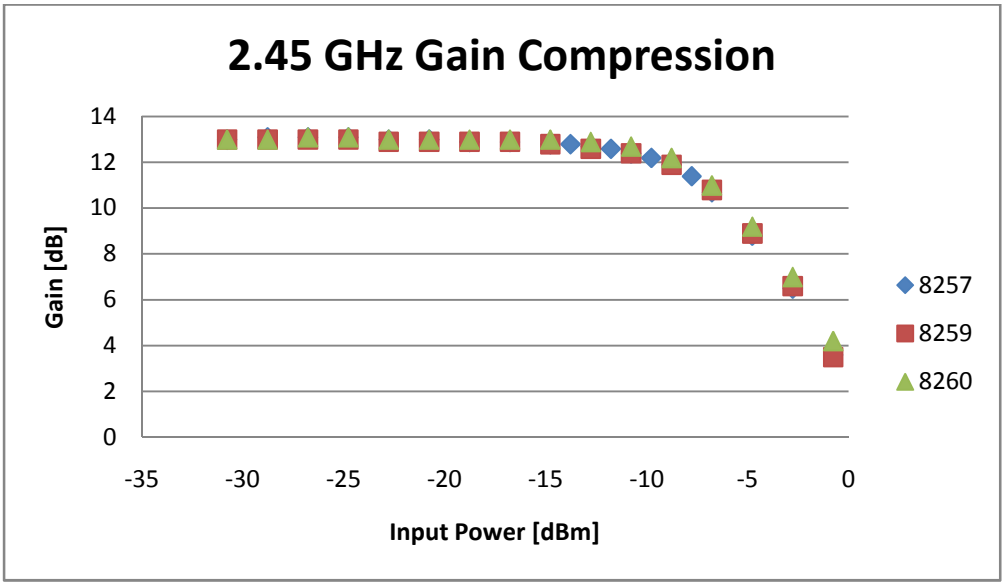
Table 5.2 - Measured intermodulation results

Frequency [GHz]	IIP3 [dBm]	OIP3 [dBm]
2.45	1.47	13.5
3.65	4.71	18.3
5.85	4.68	17.97

The frequency spacing for the intermodulation tests was 10 MHz. The test frequencies for the low band intermodulation test were 2.445 GHz and 2.455 GHz. For the mid band operation, the test tones were at 3.645 GHz and 3.655 GHz. For the high band mode, the test tones were 5.845 GHz and 5.855 GHz.

The 1 dB Compression point was measured for three circuits. The graphs of gain as a function of input power are shown in Figure 5.14 through with a wider sweep of input power shown first then a zoomed in view on the gain compression and a line

representing one dB less gain than the optimal gain at low input power. Table 5.3 summarizes the results.



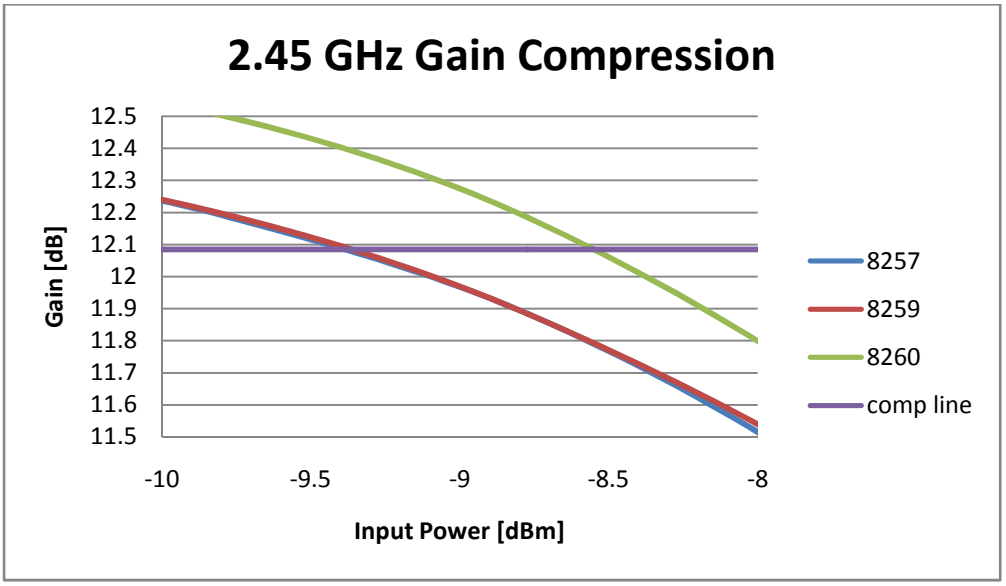
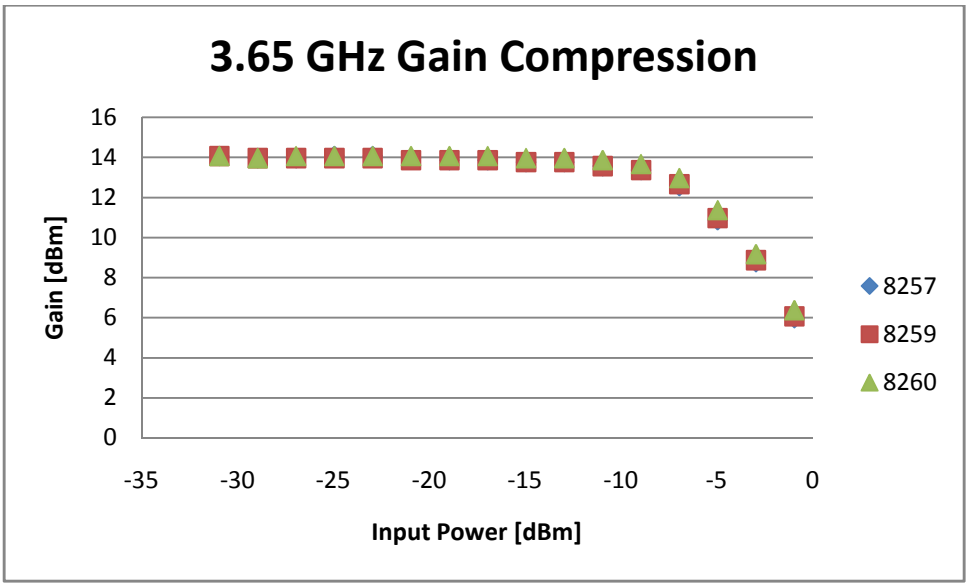


Figure 5.14 - Low-band gain compression



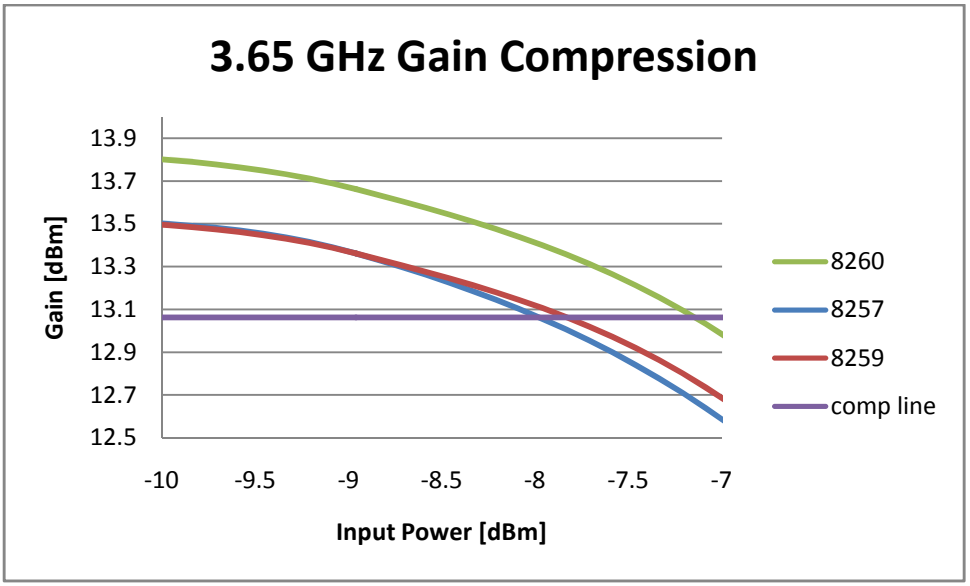
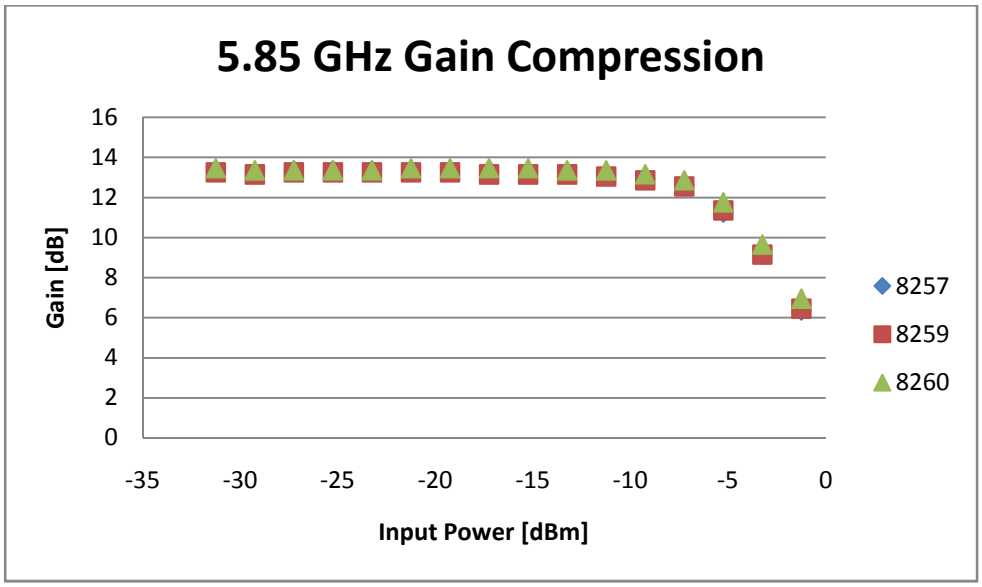


Figure 5.15 - Mid-band gain compression



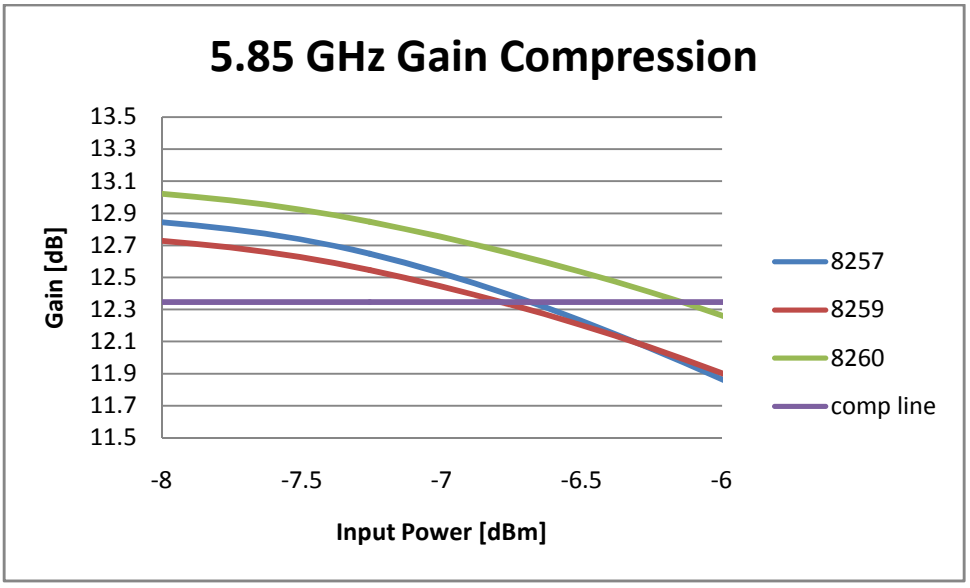


Figure 5.16 - High-band gain compression

Table 5.3 - Measured gain compression distortion

PCB Number	Frequency [GHz]	Input P1dB [dBm]	Frequency [GHz]	Input P1dB [dBm]	Frequency [GHz]	Input P1dB [dBm]
8257	2.45	-9.4	3.65	-8	5.85	-6.6
8259	2.45	-9.4	3.65	-8	5.85	-6.6
8260	2.45	-8.5	3.65	-7.2	5.85	-6.1
Average	2.45	-9.1	3.65	-7.7	5.85	-6.4

Noise figure was measured last and measured on the only remaining working IC. The results of noise figure as a function of frequency for the LNA are shown in Figure 5.17 through Figure 5.19. Table 5.4 summarizes the results.

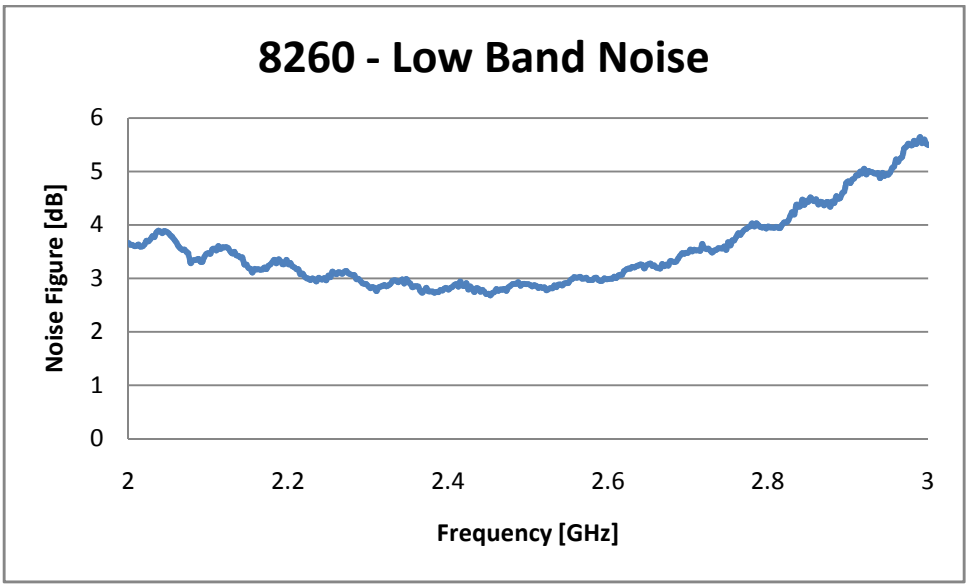


Figure 5.17 - Low band noise

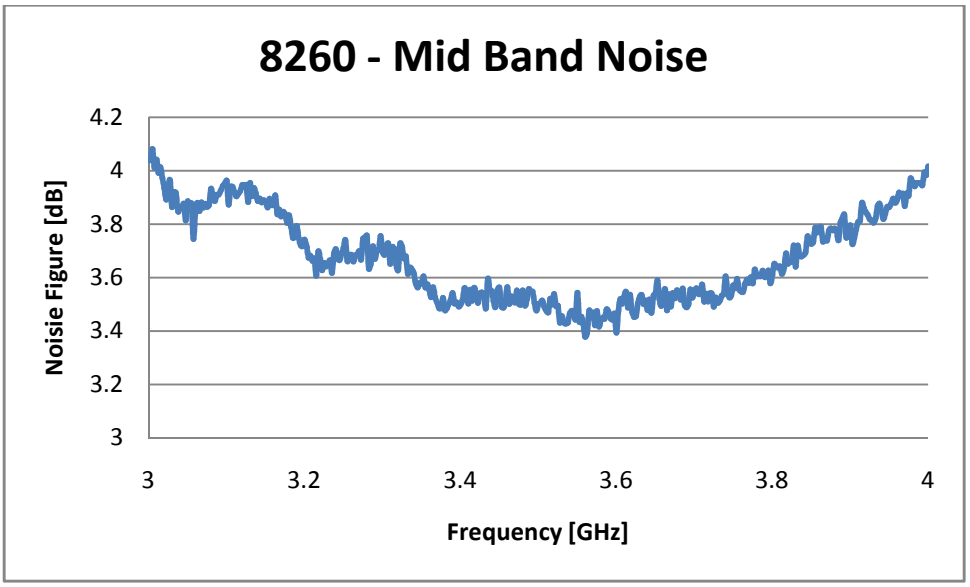


Figure 5.18- Mid-band noise

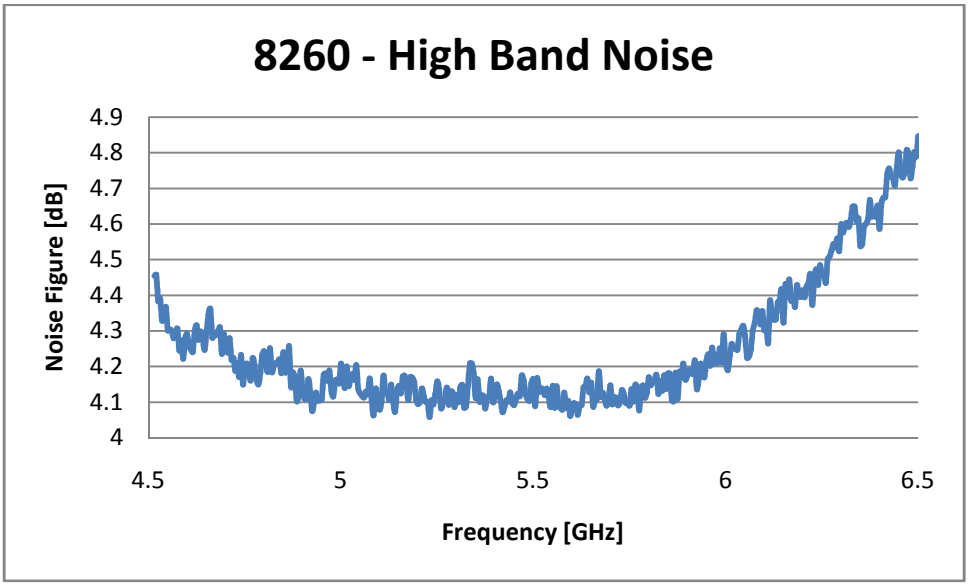


Figure 5.19 - High-band noise

Table 5.4 - Measured noise figure

Frequency [GHz]	Noise Figure [dB]
2.45 GHz	2.71
3.65 GHz	3.54
5.85 GHz	4.18

5.3 Comparison of Measurements to Simulations

Figure 5.20 through Figure 5.22 plot S_{11} and S_{21} of the LNA for four different cases: the original lumped element simulation, the original EM simulation before fabrication, the measurement results, and a post measurement backfit that better resembles the measured data. For the lumped element simulation, the individual capacitors and inductors were simulated in the electromagnetic simulator to give realistic parasitics and losses.

Table 5.5 summarizes the results. The biggest difference is between the lumped element simulation and the original EM simulation. Clearly the lumped simulation is not accurate enough for RFIC design. The original EM simulation did not include resistors, much of the metal interconnecting components and several of the large capacitors on the DC voltage pads. The post-fabrication simulation included everything except the FETs. There is no single component that appears to be responsible for large discrepancy between lumped simulation and the measurement results. Instead, it appears to be a cumulative effect of small losses throughout the design. One aspect that does have a slightly more noticeable effect is the loss in the metal connecting the source of the cascode common-source stage to ground. A small amount of resistance increases the source degeneration which in effect reduces the gain. The full electromagnetic simulation takes this into account. One thing that cannot be modeled accurately is the coupling effect between the transistor metals and the rest of the circuit. Currently there are no EM models for the transistors in the process used to fabricate the circuit. Therefore, the transistors either cannot be included in the EM simulation or their metals can be included to include coupling effects but the effects of their capacitance are counted twice in the simulation. The response of the LNA over frequency is sensitive to a certain few components: the input gate inductor and output tank capacitance. The effects are most noticeable at the high band operation where small changes in inductance and capacitance values can easily shift the response up and down in frequency. With the computing power available with modern technology more detailed simulations are achievable. And the more detailed and complete the simulation, the more of the small effects of parasitics and stray coupling show up in the simulation results.

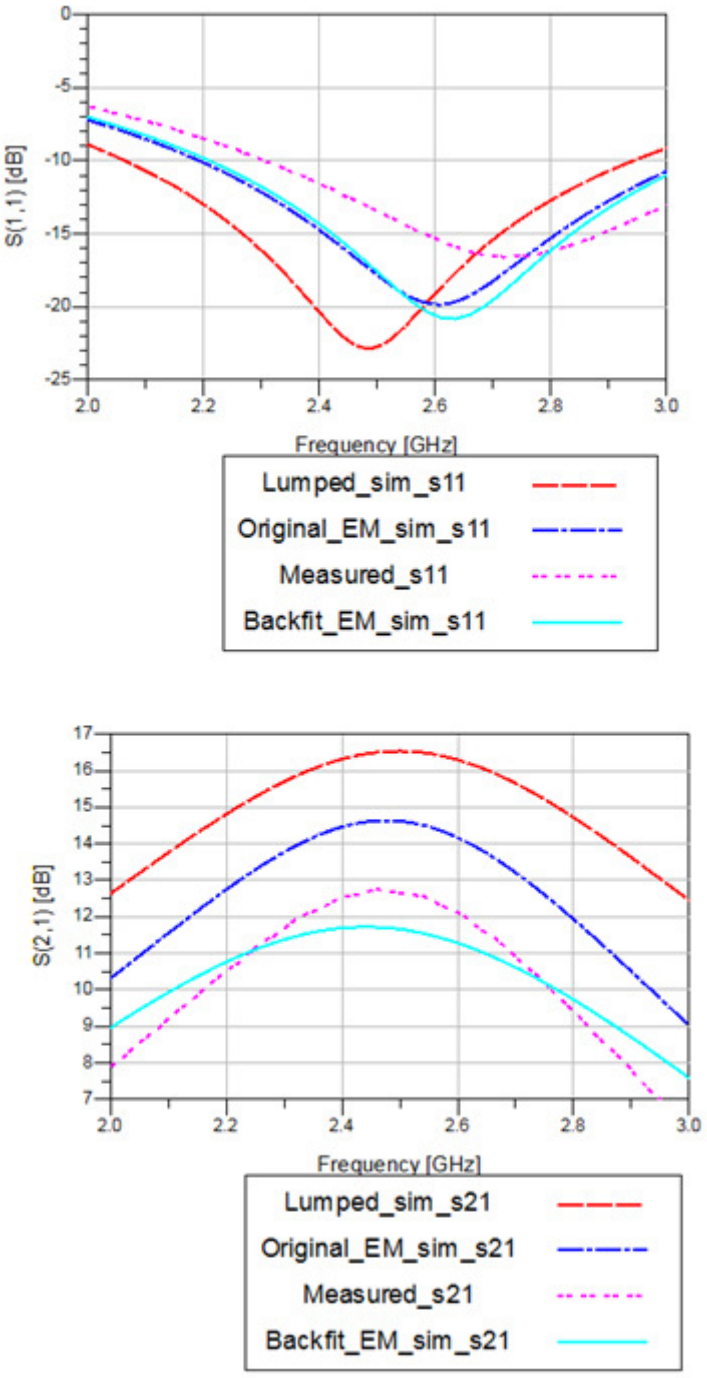


Figure 5.20 - Low Band S-Parameter Results Comparison

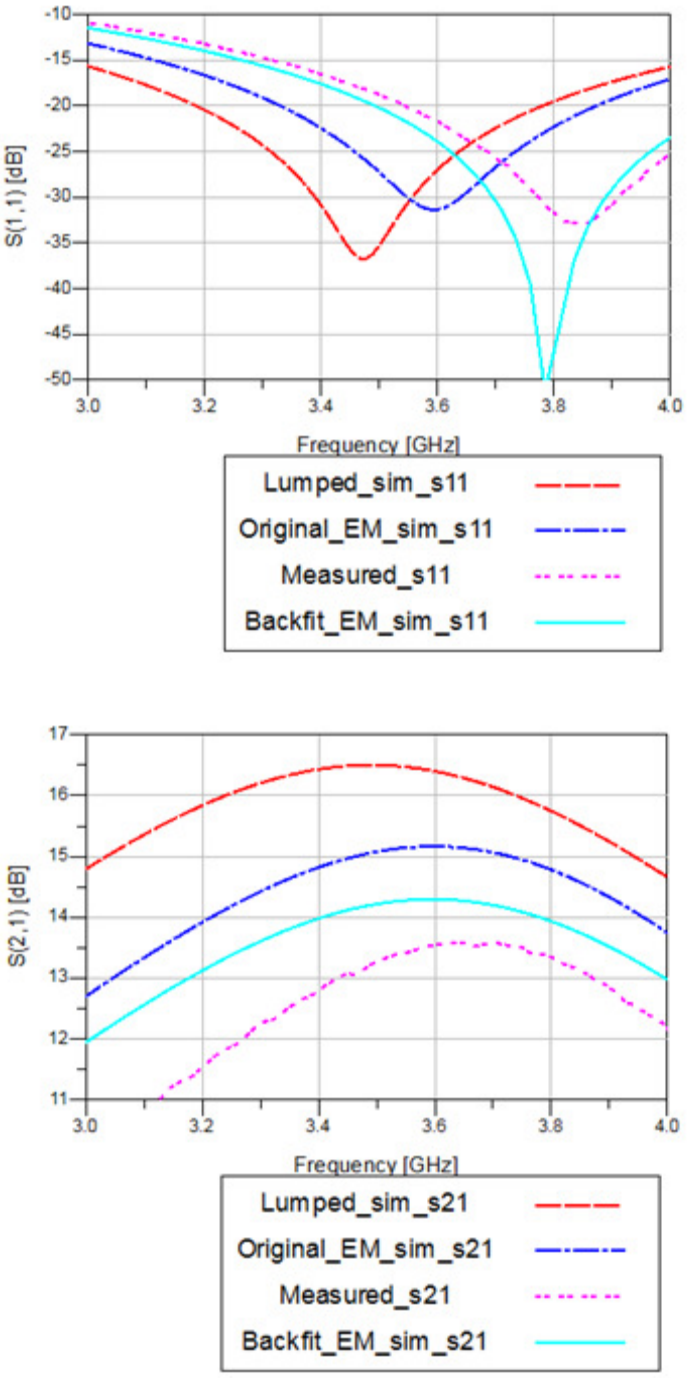


Figure 5.21 - Low Band S-Parameter Results Comparison

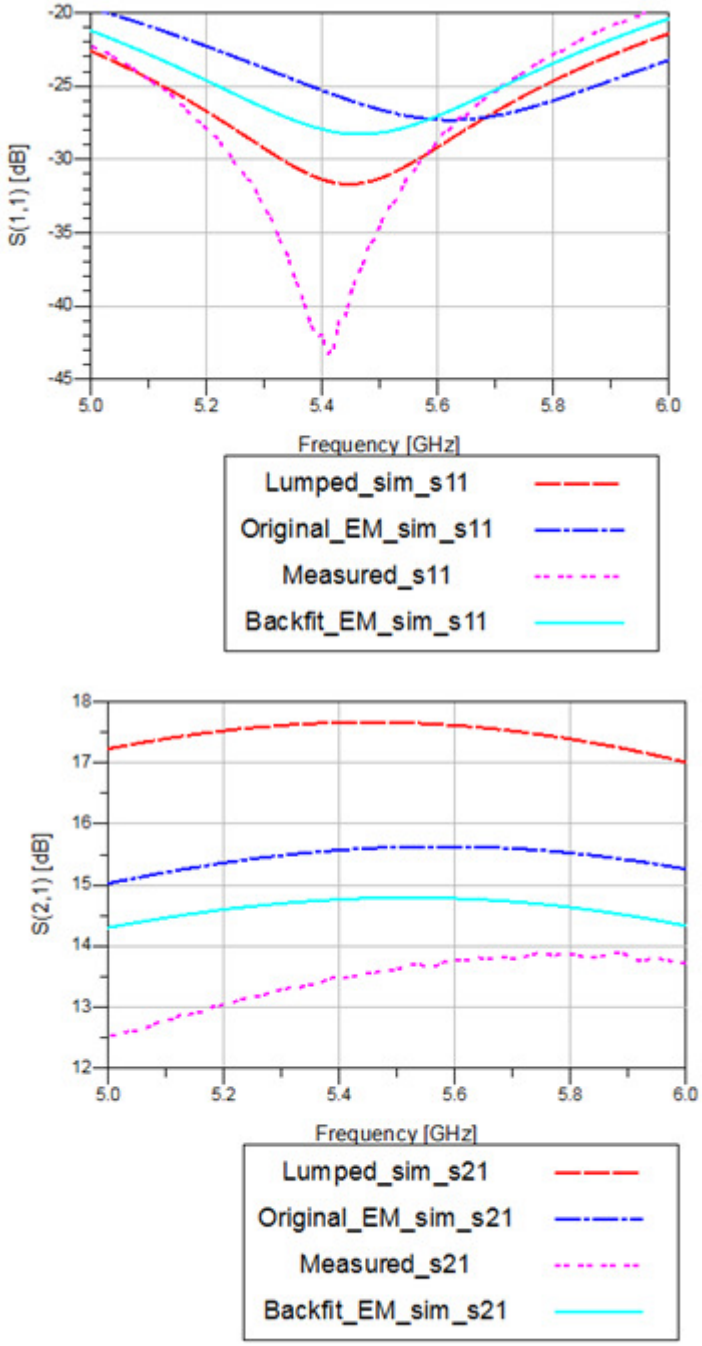


Figure 5.22- High Band S-Parameter Results Comparison

Table 5.5 - S-Parameter comparison

	Freq_S11 [GHz]	S11 [db]	Freq_S21 [GHz]	S21 [dB]
Lumped	2.48	-22.84	2.5	16.53
Original EM	2.60	-19.84	2.48	14.63
Measurement	2.72	-16.61	2.46	12.75
Backfit EM	2.64	-20.84	2.43	11.72
Lumped	3.47	-36.78	3.49	16.50
Original EM	3.59	-31.38	3.60	15.16
Measurement	3.85	-33.00	3.7	13.58
Backfit EM	3.785	-51.25	3.59	14.29
Lumped	5.45	-31.68	5.45	17.66
Original EM	5.62	-27.31	5.57	15.63
Measurement	5.41	-43.25	5.88	13.893
Backfit EM	5.46	-28.285	5.51	14.793

Table 5.6 compares the expected intermodulation distortion and gain compression measurement results derived from simulations to the results measured.

Table 5.6 - Comparison of linearity measurements and simulations

Simulated	Simulated	Measured	Measured
Frequency [GHz]	OIP3 [dBm]	Frequency [GHz]	OIP3 [dBm]

2.5	15.82	2.45	13.5
3.5	17.77	3.65	18.3
5.5	19.17	5.85	17.97

Table 5.7 compares the lumped element simulated noise figure to the measured noise figure. The frequency of measurement is different between simulation and measurement because the manufactured circuit worked best at slightly higher frequency than designed for the middle and upper bands of operation.

Table 5.7 - Comparison of noise figure measurements to simulations

Simulated Frequency [GHz]	Simulated Noise Figure [dB]	Measured Frequency [GHz]	Measured Noise Figure [dB]
2.5	2.10	2.45	2.71
3.5	2.75	3.65	3.54
5.5	3.14	5.85	4.18

The noise figure of the measured LNA is up to 1 dB worse than expected. There are numerous possibilities to explain the discrepancy between the measurements and the simulations. Unfortunately, none of them are conclusive. The list of possible culprits includes problems associated with making the measurements as well as problems with the simulations. First and foremost, a lumped element simulation is not accurate to effectively model each circuit component, its losses, and the coupling between components. A full electromagnetic simulation including all the metals on the IC gives

more accurate results. Using a full EM simulation, the noise figure results agree within 0.5 dB.

Another problem with the simulation is the transistor models. The models are derived from measurements of physical transistors, and the measurements were only taken with the transistor in the active region. The transistors were biased with the drain-source voltage greater than 1 V for the measurements. The switch-transistor is operated in the ohmic region with zero V_{DS} where no measurements were taken. The models rely on extrapolation which is not always completely accurate. If a 2 Ω resistor is placed in series with each of the switch-FETs, the noise figure of the simulations and measurements agree within 0.1 dB. The extrapolated models have an on-resistance of 1.2 Ω. It is a reach to claim that model is off by 170%.

It is also possible that there were problems with the measurements. The probes used to take the measurements are very delicate, and any mechanical problems could yield errors in the measurements. The source impedance seen by the LNA is also a critical factor in determining the noise figure. If the source impedance deviates from 50 Ω, the noise figure is affected - often worsened. A combination of poor connections in the input chain between the noise source and the LNA can affect the impedance seen by the LNA. For the measurement, there was an elbow between the noise source and the probe connector. Including the connection between the probe and the die, there were 3 interfaces. Two of the three connections were made using high quality 3.5 mm connectors, so it is not likely that these were a problem but remains a possibility. There is also the possibility that the connection between the probes and the die were unsatisfactory which could also cause a mismatch. To simulate this, a lossy transmission

line is added between the source and the LNA, and the noise figures agree within 0.15 dB. The loss of the transmission line is 0.15 dB at 2.5 GHz and 0.3 dB at 5.5 GHz. This is comparable to the loss added by the probe heads, but after adding the transmission line to the simulation, simulated and measured input match disagree by over 15 dB.

Breakout circuits would be useful tools to help find troubled areas in the circuit. Good examples of breakout circuits include switch-transistors, single inductors, and the entire reconfigurable inductor. Then, measurements and simulations of individual components and sub-circuits can be compared to find out where the discrepancy arises.

There is no certain reason why the simulations and measurements differ. It is possible that one of the above reasons is responsible, or a combination of the above reasons or something different. The lesson learned is that accurate modeling and careful measurements are required so that the end product behaves as expected.

CHAPTER 6

CONCLUSIONS

6.1 Summary & Final Thoughts

One possible future of wireless receivers in mobile devices is an electronically reconfigurable system. Reconfigurable LNAs will be required to operate over the various frequencies. Presented here were three new LNA topologies that could potentially fill this role.

The common-gate LNA has the major advantage of being wide-band. By adding frequency selective feedback, the LNA obtains a pass-band nature. The goal of the pass-band response is to protect the LNA and subsequent circuits from stronger out of band interferes. As shown, if the feedback itself is linear enough it can help protect the transistors from interferers. A truly reconfigurable LNA would be able to switch the cascode feedback off when it degraded system performance and turn it on when it improved system performance.

The synchronous filter has the advantage of having a frequency response controlled by oscillators. The synchronous filter itself would not do a good job as an LNA unless the first mixing stages are also low noise and have substantial gain. Instead, the synchronous filter can be used in a feedback loop to add a band-pass response to a wide-band amplifier.

The final new design is based on the cascode LNA which is a proven technology With the new inductor and capacitor bank it could potentially operate over several frequency bands. The high Q inductors in the semi-insulating GaAs substrate allow

simple RF switches to be added to tune the input impedance of the amplifier. Switches are also used later in the circuit with capacitors to form an adjustable capacitor which are capable of tuning the gain. When comparing the new cascode topology to a typical RF system that might have several large switches and several completely separated LNAs, the biggest advantage of the new design is the potential for saving space especially as more and more RF bands are added to the required specifications. The biggest disadvantage is the fact that the reduced Q of the adjustable inductors and capacitors has a large negative impact on the gain.

6.2 Future Work

There is still much work to be done with reconfigurable LNAs. The cascode LNA is far from complete. Several more iterations of design could help improve its electrical characteristics. Break-out circuits could help pin-point trouble spots that degrade performance. Better switch design and layout might also improve the quality factor of the adjustable reactive components. Improving the Q factor could potentially improve the noise figure and the gain of the LNA. More iterations of the layout would also reduce the required die size. A smaller die size would not only help reduce cost but also help reduce stray losses through long metal traces. The small amounts of loss compound and can significantly reduce the gain as shown in the difference between the lumped element simulations and the full electromagnetic simulations.

The synchronous filter LNA has a long way to go. The trouble of stability needs to be addressed in full and careful design of amplifiers is required to ensure they are small enough and low power enough to fit in mobile applications.

The common-gate topology needs a significant amount of work as well. First, an adjustable reactive component needs to be designed to go in the feedback loop to give it the frequency response the reconfigurable aspect. In addition, the degradation of the linearity due to the feedback needs to be addressed so that the feedback actually is advantageous. The stability is also still an issue as the solution presented here only works well for narrow-band circuits.

One interesting thing to study would be to put a reconfigurable LNA into a complete receiver architecture and compare the bit-error rate of the new receiver to that of a traditional receiver with several LNAs and switching networks. Also, the manufacturing cost analysis of a potentially well tuned reconfigurable LNA to larger, more complicated network of LNAs and switching networks would be interesting to see how advantageous the new LNA could be.

The possibility of a fully reconfigurable wireless transceiver is a dream within reason but its design will be a lengthy process. The ability for a receiver or transmitter to operate in a completely different frequency band with a different modulation scheme and at different power levels would open new doors of communication equipment.

APPENDIX A1

A1 - COMMON-GATE WITH CASCODE FEEDBACK INPUT IMPEDANCE

The small signal model for determining the input impedance of the common-gate stage with cascode feedback is shown in Figure A1.1.

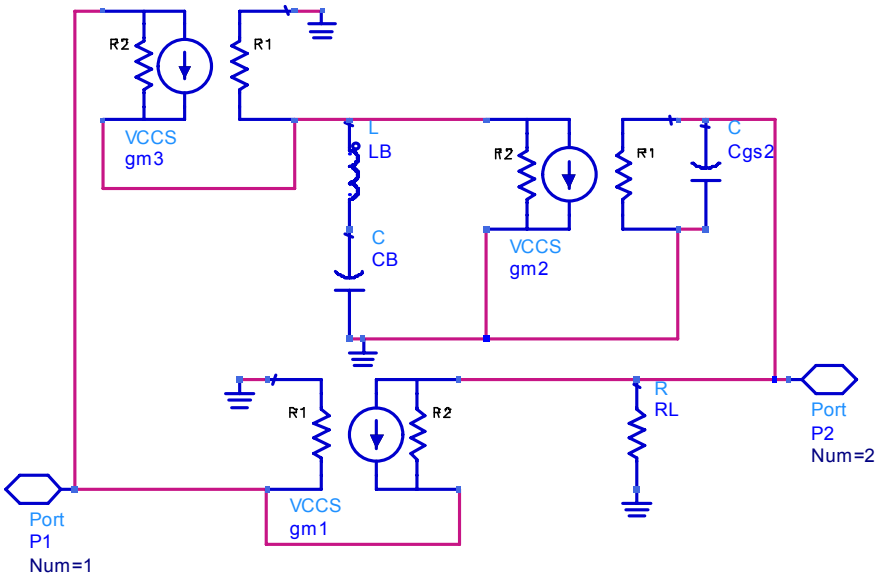


Figure A1.1 - Common-gate small signal model for input impedance

The input impedance is

$$Z_{IN} = \frac{1}{g_{m1} + \dfrac{g_{m1}g_{m2}g_{m3}R_L}{g_{m3} + sC_{GS2}g_{m3}R_L + \dfrac{R_L sC_{GS2} + 1}{sL_B + \dfrac{1}{sC_B}}}}. \qquad \text{(A1.1)}$$

The circuit in Figure A1.2 has the same input impedance.

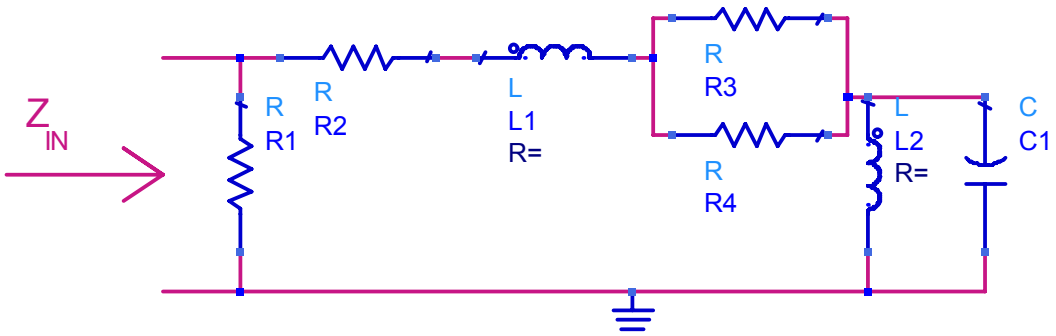


Figure A1.2 Common gate input impedance equivalent circuit

To derive the equivalent circuit, first flip the impedance into an admittance so that

$$Y_{IN} = g_{m1} + \frac{g_{m1}g_{m2}g_{m3}R_L}{g_{m3} + sC_{GS2}g_{m3}R_L + \dfrac{R_L sC_{GS2} + 1}{sL_B + \dfrac{1}{sC_B}}}. \tag{A1.2}$$

Subtracting the shunt conductance yields

$$Y_{IN} - g_{m1} = Y_{IN}' = \frac{g_{m1}g_{m2}g_{m3}R_L}{g_{m3} + sC_{GS2}g_{m3}R_L + \dfrac{R_L sC_{GS2} + 1}{sL_B + \dfrac{1}{sC_B}}}. \tag{A1.3}$$

Converting this back into an impedance yields

$$Z_{IN}' = \frac{g_{m3} + sC_{GS2}g_{m3}R_L + \dfrac{R_L sC_{GS2} + 1}{sL_B + \dfrac{1}{sC_B}}}{g_{m1}g_{m2}g_{m3}R_L}. \tag{A1.4}$$

The first two terms are a series resistor and series inductor. Subtracting this yields

$$Z_{IN}' - \frac{g_{m3} + sC_{GS2}g_{m3}R_L}{g_{m1}g_{m2}g_{m3}R_L} = Z_{IN}'' = \frac{\frac{R_L sC_{GS2} + 1}{sL_B + \frac{1}{sC_B}}}{g_{m1}g_{m2}g_{m3}R_L} \quad \text{(A1.5)}$$

$$Z_{IN}'' = \frac{1}{\left(sL_B + \frac{1}{sC_B}\right)\left(g_{m1}g_{m2}g_{m3}R_L\right)} + \frac{R_L sC_{GS2}}{\left(sL_B + \frac{1}{sC_B}\right)\left(g_{m1}g_{m2}g_{m3}R_L\right)} \quad \text{(A1.6)}$$

Z_{IN}'' is equivalent to a series combination of two parallel circuits. The first parallel circuit pair is an LC tank and the second is a parallel combination of a regular resistor and a frequency dependent negative resistor.

APPENDIX A2

A2 - CASCODE LNA DIE SIZE COMPARISON

Table A2.1 and Table A2.2 list the largest components required for a single band LNA and two-band reconfigurable LNA, respectively. The tables also list the size of each component, the quantities of the components, and the total area taken by all of the components. The size approximation only includes the largest components and does not include any interconnects.

Table A2.1 - Single Band LNA Components

Component	Size	Qty	Sub-total
DC Choke	400 μm x 300 μm	2	240,000 μm^2
Cascode CS FET	130 x 100	1	13,000 μm^2
Cascode CG FET	130 x 65	1	8,450 μm^2
DC Blocking Caps	110 x 77	5	42,350 μm^2
ESD	100 x 100	1	10,000 μm^2
V_{DD} Bypass Cap	125 x 200	1	25,000 μm^2
Gate Inductor	200 x 470	1	94,000 μm^2
			432,800 μm^2

Table A2.2 - Two-band Reconfigurable LNA Components

Component	Size	Qty	Sub-total
DC Choke	400 μm x 300 μm	2	240,000 μm^2
Cascode CS FET	130 x 100	1	13,000 μm^2
Cascode CG FET	130 x 65	1	8,450 μm^2
DC Blocking Caps	110 x 77	6	42,350 μm^2
ESD	100 x 100	3	10,000 μm^2
V_{DD} Bypass Caps	125 x 200	3	125,000 μm^2
Gate Inductor	200 x 470	1	94,000 μm^2
Input Switch	100 x 320	1	32,000 μm^2
Tank Switch	90 x 210	1	19,000 μm^2
			583,800 μm^2

APPENDIX A3

A3 - CASCODE LNA SIMULATION RESULTS

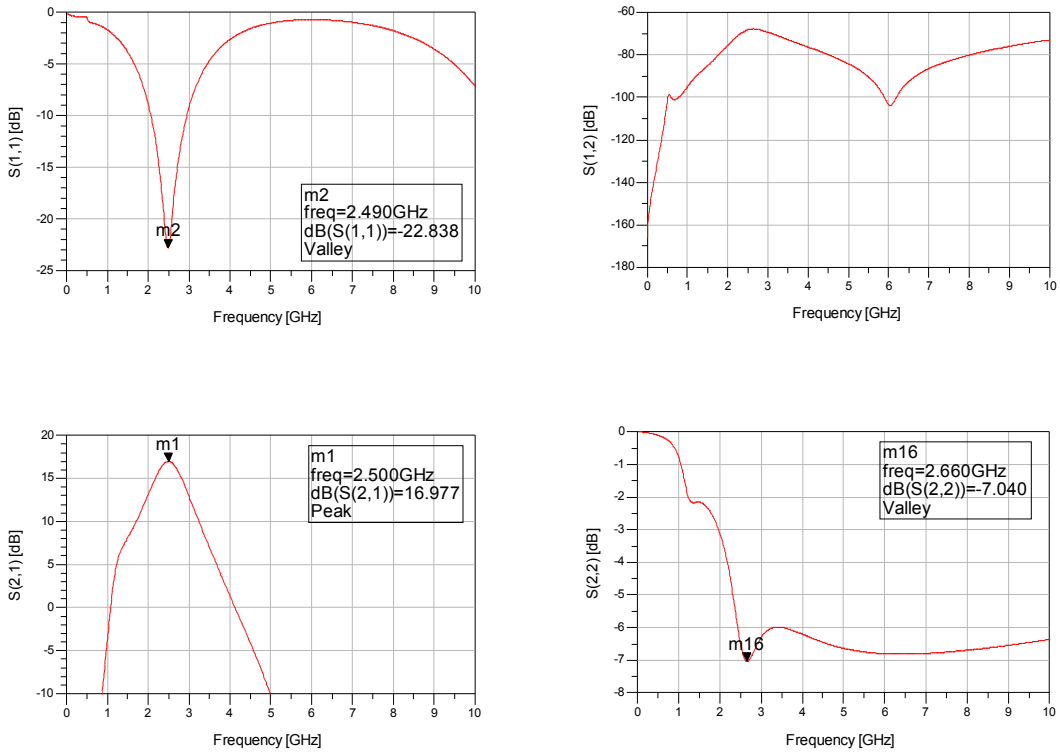


Figure A3.1 - Cascode simulation low band S-parameter Results

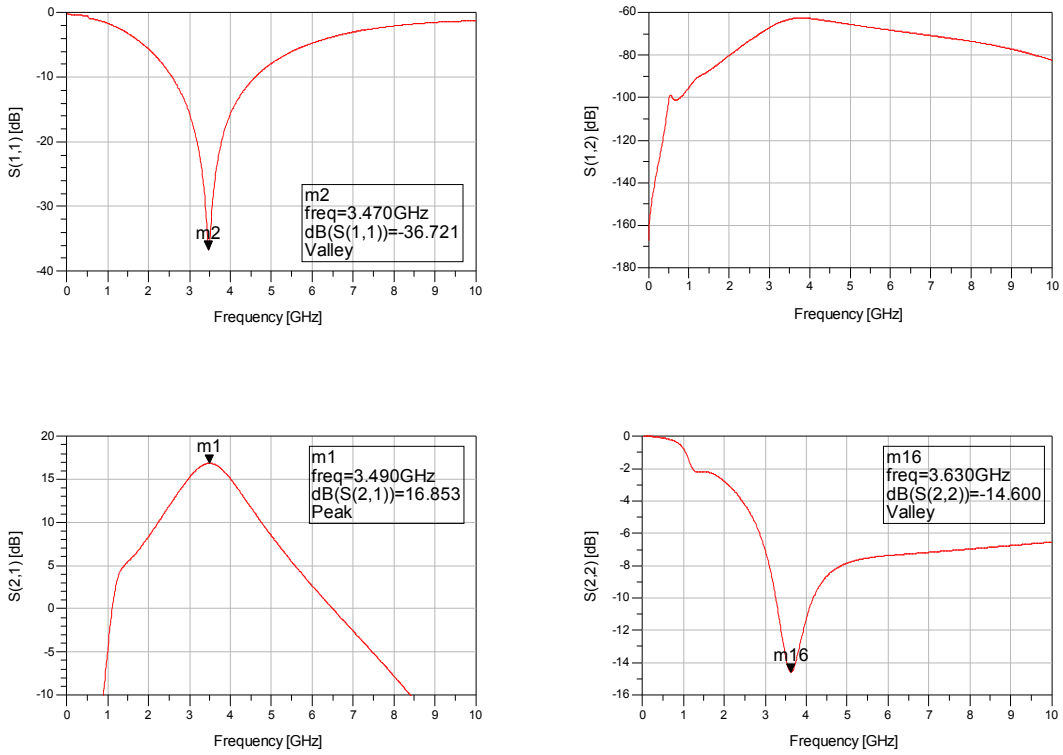


Figure A3.2 - Cascode simulation mid-band S-parameter results

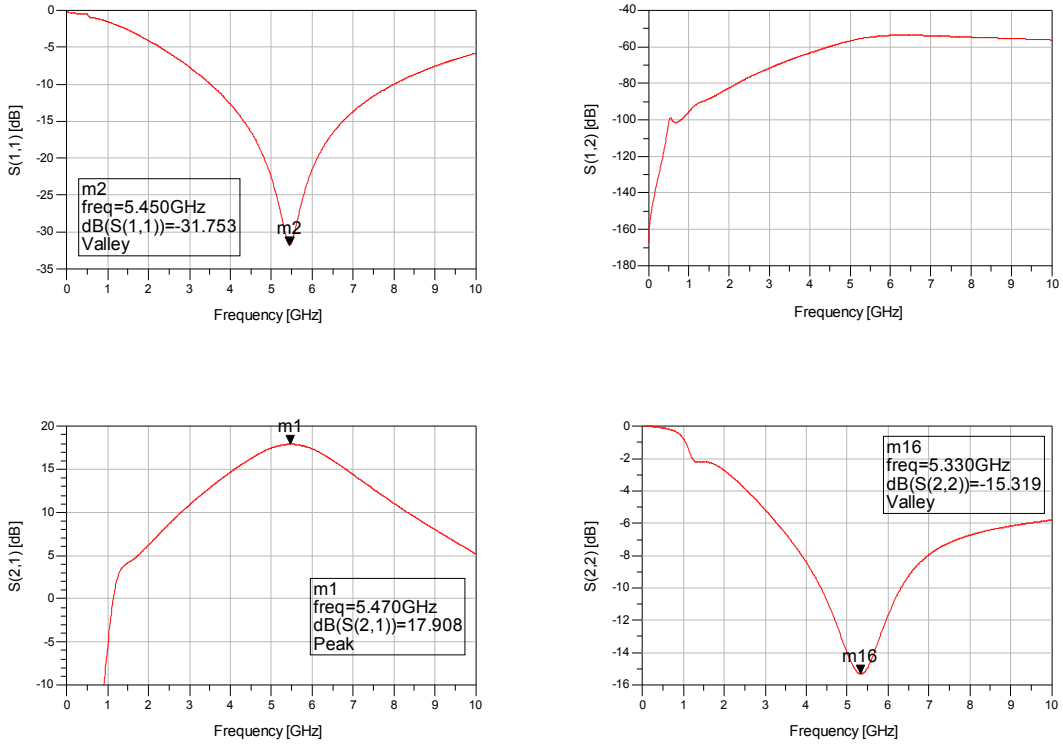


Figure A3.3 - Cascode simulation high-band S-parameter results

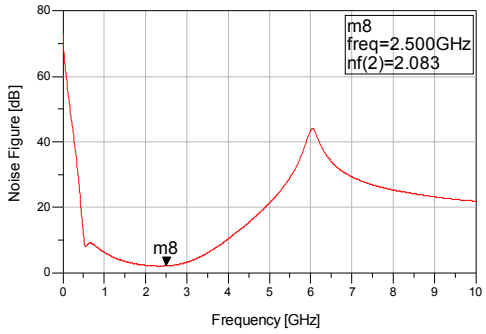


Figure A3.4 - Cascode simulation low-band noise figure

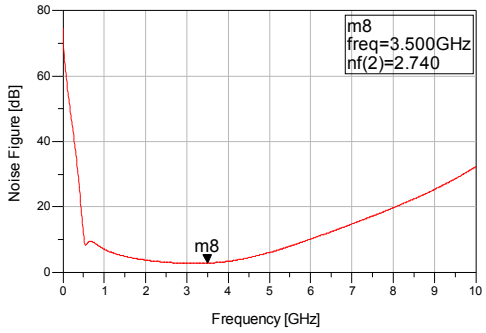


Figure A3.5 - Cascode simulation mid-band noise figure

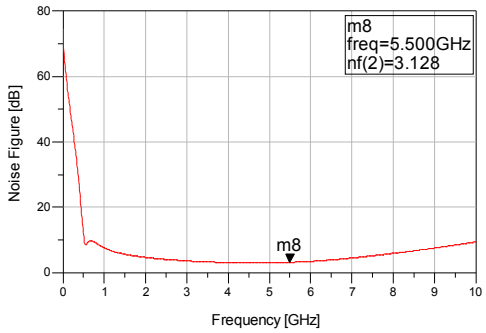


Figure A3.6 - Cascode simulation high-band noise figure

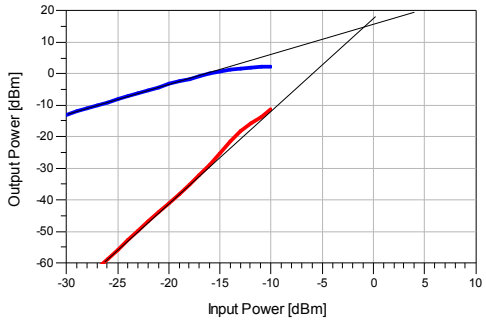


Figure A3.7 - Cascode simulation low-band intermodulation distortion

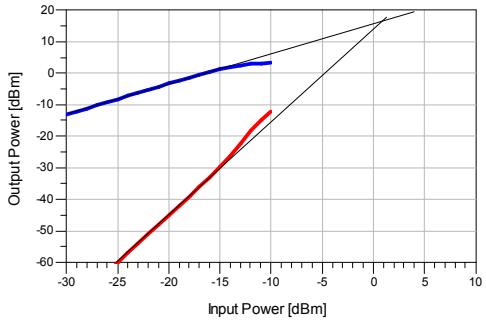


Figure A3.8 - Cascode simulation mid-band intermodulation distortion

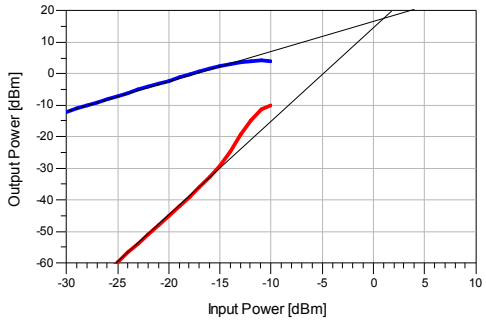


Figure A3.9 - Cascode simulation high-band intermodulation distortion

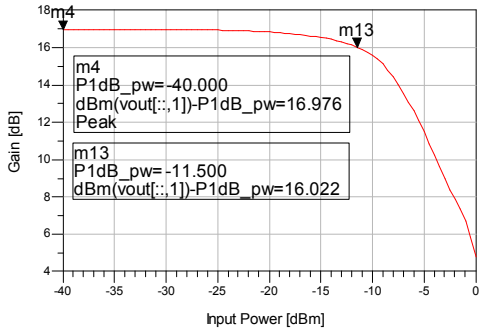


Figure A3.10 - Cascode simulation low-band gain compression

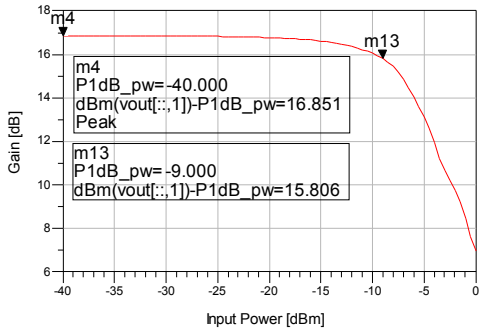


Figure A3.11 - Cascode simulation mid-band gain compression

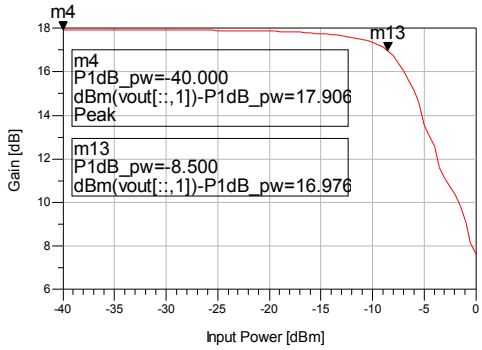


Figure A3.12 - Cascode simulation high-band gain compression

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