Pentacene Based Organic Electronic Devices

YUN, YOUNGJUN

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Youngjun Yun

Abstract

This thesis describes a study of pentacene-based organic electronic devices with poly(methyl methacrylate) (PMMA) and cross-linked PMMA (cPMMA) gate dielectrics. The electrical characteristics of pentacene-based organic thin-film transistors (OTFTs) using PMMA as the gate dielectric are reported. Uniform pinhole-free and crack-free films of PMMA could be obtained by spin-coating, with a lower limit to the thickness of about 150 nm. The effects of the insulator thickness and channel dimensions on the performance of the devices has been investigated. Leakage currents, which are present in many devices using polymeric gate dielectrics, were reduced by patterning the pentacene active layer. The resulting transistors exhibited minimal hysteresis in their output and transfer characteristics with an acceptable performance (a field-effect mobility of 0.33 cm^2 V^{-1} s^{-1}, a threshold voltage of -11 V, an on/off current ratio of 1.2×10^6 and a subthreshold slope of 1.5 V per decade). A bootstrapped inverter incorporating optimised pentacene OTFT structures, with PMMA as the gate dielectric, has been designed, fabricated and tested. The inverter uses capacitive coupling and bootstrapping effects, and exhibits superior performance to the normal diode-connected load inverter. The circuit has a 30 μs rise time and 450 μs fall time, at an operating frequency of 1 kHz and 30 V drive voltage. Pentacene-based OTFTs incorporating a PMMA gate insulator usually possess a large operating voltage, related to the thickness of the PMMA layer. A physical method, in particular ion-beam irradiation, to produce ultra-thin cross-linked layers of PMMA (33 nm) is introduced. It is demonstrated that physical cross-linking of the PMMA gate dielectric can be used to produce OTFTs with improved performance (a field-effect mobility of 1.1 cm^2 V^{-1} s^{-1}, a threshold voltage of -1 V, an on/off current ratio of 1.0×10^6 and a subthreshold slope of 220 mV per decade) and

operating at low voltages, < 10 V. Low voltage memory transistors based on various charge storage elements (gold nanoparticles, ultra-thin aluminium and silver films) with cPMMA as the gate dielectric, have been investigated. Solution-processed OTFTs based on 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene with PMMA and cPMMA as the gate dielectric were also studied.

Pentacene Based Organic Electronic Devices

by

Youngjun Yun

Ustinov College

A Thesis submitted in partial fulfilment

of the requirements for the degree of PhD

Centre for Molecular and Nanoscale Electronics

School of Engineering and Computing Sciences

University of Durham

6 December 2010

Contents

List of Figures

List of Tables

Declaration

I hereby declare that the work carried out in this thesis has not been previously submitted for any degree and is not currently being submitted in candidature for any other degree.

Signed.....
Candidate

The work of this thesis was carried out by the candidate.

Signed.....
Director of Studies

Signed.....
Director of Studies

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Candidate

Several of the chapters in this thesis are based on papers that are published. A list of papers and their corresponding chapters is provided in the **Publications**.

Acknowledgements

I would like to give grateful acknowledgements to the following people and institutions that have enabled me to pursue and complete this work. This thesis would not have been possible unless the Higher Education Funding Council for England (ORSAS Scholarship) and the School of Engineering and Computing Sciences, Durham University (PhD Scholarship) had provided tuition fees and living expenses. To my supervisors, Prof. Michael C. Petty and Dr Christopher Pearson, I am profoundly indebted. I express my gratitude to Prof. Michael C. Petty, for all his time, advice, constant encouragement and support concerning not only my research but also living in Durham. I would like to show my gratitude to Dr Christopher Pearson for his advice and guidance of experimental techniques. I really thank them from my heart.

To all the current and former colleagues in the Centre for Molecular and Nanoscale Electronics goes my gratitude. I would like to particularly thank Dr Mohammed F. Mabrook, Dr Duncan H. Cadd, Prof. David Wood, Dr Dagou Zeze, Dr Palat Ushasree and Dr Mark Rosamond. In particular, very special thanks to the best friend I have met in Durham, Dr (to be) Supachai Ritjareonwattu, for his firm friendship and kind help with various tasks. It is my pleasure to thank those who made this thesis possible by allowing me access to their facilities and sharing their knowledge, in particular Prof. Graham Sandford and Dr Richard Thompson in the Department of Chemistry.

Most importantly, my parents for encouraging and inspiring me even while they are halfway around the world. And my brand new son, Siwoo, for providing a happiness in which to study and live. Finally, I want to especially thank my loving wife, Hyeyeon, for her understanding, patience and encouragement, without which I would not have succeeded this far.

Dedicated to my wife

Chapter 1

Introduction

The current performance of organic electronic devices suggest that they can be used for existing or new applications requiring large-area coverage, structural flexibility, low-temperature processing and low-cost manufacture. Among the various organic electronic devices, the organic thin-film transistor (OTFT) might become an important element in future microelectronics technology. OTFTs possess two key advantages over devices fabricated from inorganic semiconductors: mechanical flexibility and low-cost manufacture. These properties make OTFTs promising candidates for information displays, chemical sensors and radio frequency identification tags. For these and other applications, it is important to develop OTFTs with high performance and low cost manufacture. Various organic semiconductor materials have been used as the active layer in OTFTs. These include molecular crystals such as pentacene, which can be deposited in thin film form by thermal evaporation, and 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene, which can be conveniently processed by solution-based methods, such as spin-coating and inkjet-printing [1]. The gate dielectric layer also plays a crucial role in determining the performance of OTFTs [2]; the benefits of OTFTs can easily be lost if inappropriate insulators are used. For example, the inorganic insulators silicon dioxide and silicon nitride, both common gate dielectrics in OTFTs, are formed at high temperature. This precludes the use of many organic substrates. Certain organic insulators, such as benzocyclobutene (BCB), also need a very high curing temperature.

This thesis is concerned with pentacene-based organic electronic devices with a poly(methyl methacrylate) (PMMA) gate insulator. In this thesis, three strategies have been used to obtain low voltage organic electronic devices with high perfor-

mance and low-cost manufacture. First, thermally evaporated pentacene OTFTs with a spin-coated PMMA gate dielectric are investigated for hysteresis-free devices. Secondly, thermally evaporated pentacene OTFTs with physically cross-linked PMMA (cPMMA) gate dielectrics for low voltage operating devices are studied. Thirdly, spin-coated TIPS pentacene OTFTs with PMMA and cPMMA gate dielectrics for printed electronic applications are explored.

This thesis is organised as follows:

In Chapter 2, a general introduction to organic electronics is given. The historical background and various applications of organic electronics are briefly discussed and special attention is given to OTFTs. Charge transport mechanisms in organic semiconductors are reviewed and the various structures and electrical characteristics of OTFTs are discussed. Chapter 3 begins with an overview of film formation techniques for OTFTs. The experimental details of this thesis and the techniques used to characterise thin films and OTFTs are described. Details of the organic materials which are used in this thesis are also given.

Chapter 4 is the first results' chapter and focuses on pentacene-based OTFTs with a PMMA gate dielectric. The properties of PMMA films deposited by spin-coating are described. These layers are then incorporated into pentacene OTFTs. The operation of two different inverter circuits (a simple diode-connected load inverter and a bootstrapped inverter) exploiting pentacene-based OTFTs with PMMA gate dielectrics are contrasted. Chapter 5 is concerned with cPMMA gate dielectrics for low voltage operating devices. The use of ion-beam irradiation to produce ultra-thin cross-linked layers of PMMA is introduced. The device characteristics of a pentacene-based OTFT using cPMMA as the gate dielectric are reported. In particular, the saturated field-effect mobility as a function of the thickness of the gate dielectric is detailed. The remainder of Chapter 5 focuses on low voltage operating memory devices. Low voltage operating memory transistors based on various charge storage elements (a thin aluminium film, a thin silver film and gold nanoparticles) with cPMMA as the gate dielectric are investigated. In Chapter 6, the electrical characteristics of solution-processed OTFTs based on TIPS pentacene with either PMMA or cPMMA as the gate dielectric are given.

Finally, Chapter 7 provides the conclusions derived from the thesis and some suggestions for further work.

References

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Chapter 2

A Literature Review of Organic Electronics

2.1 Introduction

According to a study conducted by the US marketing research institute IDTechEx in 2006, the global market for organic and printed electronics will grow from its current 1.18 billion US dollars to more than 40 times that, to a volume of 48.18 billion US dollars, within the next 10 years [1]. Because of the relatively low charge carrier mobilities in organic materials, organic semiconductors cannot achieve the device performance of single-crystalline inorganic semiconductors, such as silicon (Si) and gallium arsenide (GaAs), which possess mobilities about three orders of magnitude higher. However, organic electronics is largely motivated by other considerations. The first attraction is the possibility of making some silicon-like functionality at a small fraction of the cost, by the use of inexpensive solution processes. A second is to use the capabilities of organic semiconductors that are not as readily available in silicon, such as sensing and mechanical flexibility. Research into organic semiconductor devices may open the way to completely new fabrication processes, and applications where organic semiconductors may prove advantageous.

This chapter begins with the historical background of organic electronics and its various applications. Important charge transport mechanisms in organic semiconductors are then introduced. The main components of organic thin-film transistors (OTFTs), organic semiconductors for the active layer, gate dielectrics and source and drain electrodes are described in the following section. The various device structures of OTFT are then discussed. Finally, the extraction methods for field-effect mobility, threshold voltage, subthreshold slope and on/off current ratio from the

electrical characteristics of OTFTs are reviewed.

2.2 Historical Background

Organic semiconductors were identified in the late 1940s [2] but work on organic light-emitting diodes (OLEDs) [3, 4], organic photovoltaic cells (OPVCs) [5] and OTFTs [6] only emerged in the late 1980s. The initial organic devices were based on either small organic molecules, 8-hydroxyquinoline aluminium (Alq_3) for the emitting layer in OLEDs [3] for example, or conjugated polymers, such as poly(p-phenylenevinylene) (PPV) [4] and polythiophene (PT) for the active layer in OTFTs [6].

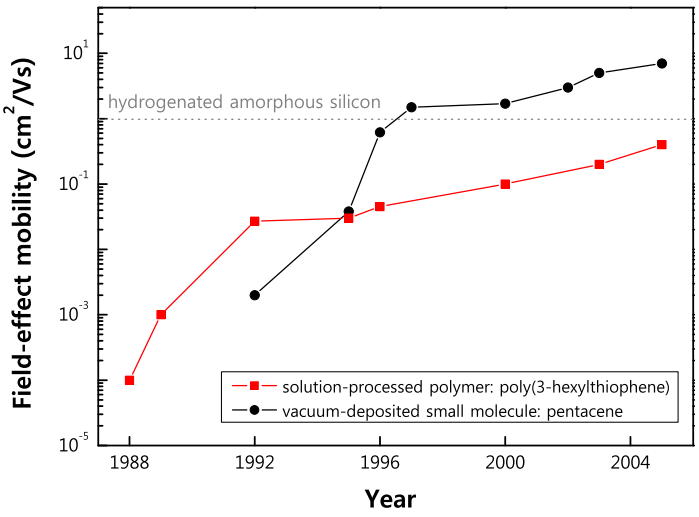


Figure 2.1: Improvement in organic semiconductor mobility since the 1980s [2,7].

The performance of organic electronic devices has continuously improved over the last 20 years, and OLEDs have now been launched onto the display market. In the case of OPVCs, power conversion efficiencies have reached over 5 % [8]. Although these efficiencies are significantly lower than those of their inorganic counterparts (10∼20 %), the prospects of cheap production by roll-to-roll or printing processes drives the development of OPVCs further in a dynamic way. The progress of OTFTs has been less intense but the performance of some OTFTs now competes

with amorphous silicon TFTs which are used in active-matrix (AM) liquid crystal displays (LCDs), as shown in Figure 2.1 [2, 7]. From now on, this review will focus on OTFTs.

2.3 Applications

The processing characteristics and performance of OTFTs so far show that they can be used for existing or novel TFT applications requiring large-area coverage, structural flexibility, low-temperature processing, and low-cost manufacture. The applications of organic semiconductors include AM flat panel displays (FPDs) based on liquid crystal pixels, organic light emitting diodes and electronic ink, low-end smart cards, electronic identification tags, sensors and perhaps all-flexible electronics.

2.3.1 Flat Panel Displays

An important potential application of OTFTs is in backplanes for displays. Despite a slowdown in the worldwide growth of FPDs, sales revenues are forecast to grow from 82.6 billion US dollars in 2009 to 111.5 billion US dollars by 2016, according to the latest results in the "Quarterly Worldwide FPD Shipment and Forecast Report" from Austin, Texas-based DisplaySearch [9]. In particular, OLED television (TV) and e-Book sales revenues may rise up to 140 % and 49 %, each year from 2008 to 2016, respectively [9].

To date, most backplanes of AM LCDs and AM OLED displays are based on TFTs comprising hydrogenated amorphous silicon (a-Si:H) or low temperature poly silicon (LTPS) as the active layer. However, OTFTs possess several advantages over structures fabricated from inorganic semiconductors: flexibility, large-area coverage and low-cost manufacture. These make OTFTs a promising candidate for inexpensive and flexible displays. For example, it is impossible to make AM LCDs based on a-Si:H TFTs on a transparent plastic substrate because of the relatively high processing temperature needed for a-Si:H deposition. However, OTFTs can be processed at room temperature and thus are compatible with flexible substrates. Furthermore, solution-processed OTFTs can enable low-cost large-area manufactur-

ing approaches, such as those based on inkjet-printing and roll-to-roll processing, for large-area AM LCD of TVs.

The first AM display based on organic semiconductors was reported in 2000 by Philips Research [10]. In 2001, Rogers et al. reported an electrophoretic flexible display using a backplane based on OTFTs [11]. Following Rogers's report, many research groups have described OTFT backplanes in combination with electrophoretic display media and simple OLED pixels. Hong et al. have also shown the possibility of an OTFT backplane with fairly large size and high resolution for AM LCDs in 2005 [12].

2.3.2 Low-End Smart Cards and Electronic Identification Tags

Devices based on organic semiconductors are still in their infancy and certain parameters such as field-effect mobility, uniformity of threshold voltage and dark currents are far inferior to those of silicon field-effect transistors (FETs). However, the performance of today's organic semiconductor technology is sufficient to develop low-cost circuits for applications that require only modest speeds such as intelligent electronic tickets, card games and product packaging. In particular, an integrated radio frequency identification (RFID) tag, which normally operates at 13.56 MHz (high-frequency, HF), and is used for providing power to the tag via inductive coupling (as used in smart cards, tickets, library book labels, passports, laundry tags and many other applications) becomes a promising candidate for organic electronics. The cost of organic RFID tags produced by solution processing could be low enough to compete with that of bar codes while providing a lot of the advantages offered by silicon-based RFID tags. Furthermore, organic RFID tags, being made of plastics, are more flexible and thinner than those based on silicon.

Baude et al. demonstrated pentacene based RFID circuits by vacuum deposition in 2003 [13]. The RFID circuits, without a rectification stage, were powered directly by RF and operated at 125 kHz. In 2004, Subramanian et al. reported 135 kHz all-printed organic RFID tags using novel pentacene and oligothiophene precursors for p-type semiconductors and ZnO nanoparticles for the n-type semiconductor [14]. Following this in 2009, Blache et al. described the first working 4 bit transpon-

der based on organic complementary metal-oxide-semiconductor (CMOS) operating at a carrier frequency of 13.56 MHz [15]. The devices were fabricated on flexible polyester substrates and all the active layers of the device consisted of soluble organic molecules deposited by spin coating.

2.3.3 Sensors

In recent years, sensors, which are used for food safety, environmental monitoring, medical diagnostics and home security, have been intensively studied. Organic semiconductors offer many advantages in comparison with their inorganic counterparts, which make them particularly attractive for sensor applications. First, organic sensors can be manufactured at room temperature on flexible substrates with large-area coverage and using low-cost processes, an important attribute for disposable sensors and artificial skin. Second, their properties can be tunable via chemical synthesis. This includes not only electronic characteristics such as energy band gap and electron affinity but also the surface energy. Of particular interest for sensors is the ability to covalently attach biologically relevant moieties to organic semiconductor molecules [16]. Such hybrid materials have the potential to lead to the fabrication of sensors with high sensitivity and specificity.

Bartic et al. described ion-selective (IS) FETs for pH monitoring using a proton sensitive OTFT as a transducer in 2002 [17]. In 2004, Someya et al. reported a large-area, flexible pressure sensor suitable for electronic artificial skin with organic transistors [18]. The organic transistors, which were integrated with a graphite-containing rubber pressure sensor layer to form a very wide area structure, were used to realise a flexible AM, which was used to read out pressure images from the sensors. The device was electrically functional when it was wrapped around a cylindrical bar with a 2-mm radius. In 2008, OTFTs for chemical and biological sensors, capable of detecting parts per billion (ppb) anyalyte concentrations in water, were demonstrated with reliable operation by Roberts et al. [19]. Organic thin-film transistors, based on a thin, cross-linked gate dielectric and a stable organic semiconductor, could detect changes in pH and low concentrations of chemicals, such as trinitrobenzene, cysteine, methylphosphonic acid and glucose in water.

2.4 Organic Thin-Film Transistors

The metal-insulator-semiconductor (MIS) structure is the core technology in modern-day microelectronics. The energy-band diagram for an ideal MIS device, based on a p-type semiconductor, is shown in Figure 2.2 [20].

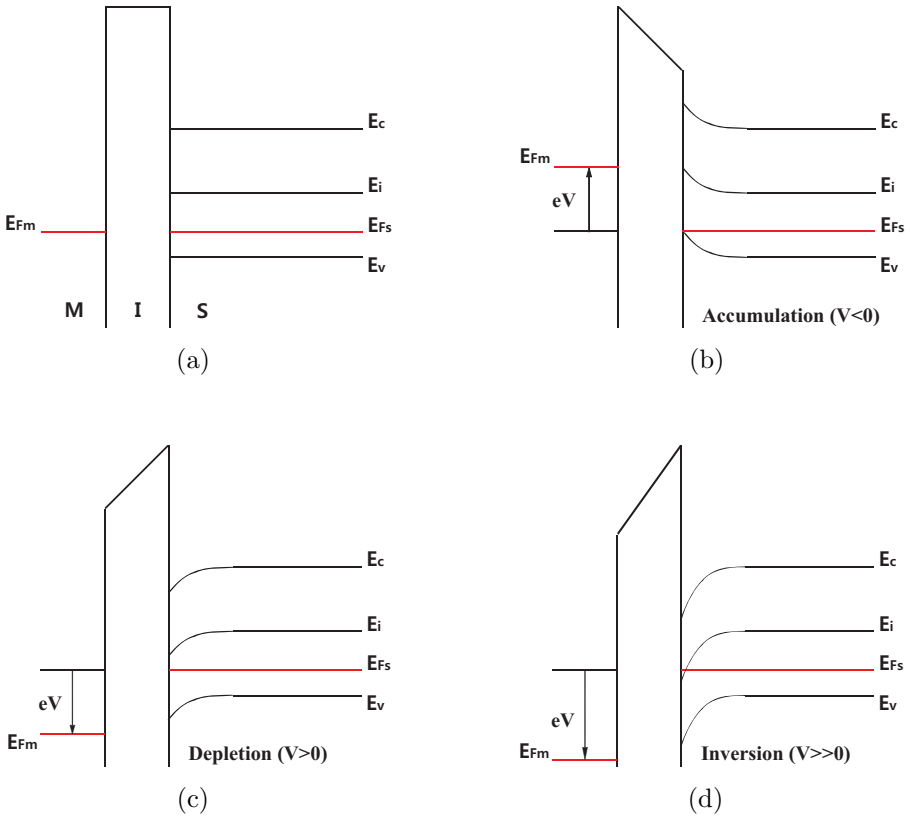


Figure 2.2: Energy band diagrams for an ideal p-type MIS device under (a) flat band, (b) accumulation, (c) depletion and (d) inversion conditions.

With no external bias, the Fermi levels of the metal and semiconductor align and the various bands are flat throughout the MIS structure (Figure 2.2(a)). When a negative voltage is applied to the metal with respect to the semiconductor (Figure 2.2(b)), the bands bend upward and the valence band moves closer to the Fermi level, causing an accumulation of holes near the insulator-semiconductor interface. A depletion of holes occurs when a positive voltage is applied to the metal (Figure 2.2(c)). If the positive voltage is increased further (Figure 2.2(d)), the bands bend down more strongly and the intrinsic level at the surface eventually becomes lower than the Fermi level. In this situation, the density of electrons exceeds that of

holes, and an inversion layer forms at the insulator-semiconductor interface. In the case of a MISFET, the inversion layer provides a conducting channel between the source and drain electrodes. One of the main advantages of the MISFET is that the depletion region between the p-type substrate and both the n-type and n^+ regions below source and drain electrodes provides isolation from any other device fabricated on the same substrate. Furthermore, very low off currents can be achieved because both n^+ regions act as reverse-biased diodes.

The concept of a TFT was proposed by Weimer in 1962 [21] and this led to the first a-Si:H TFT in 1979 by Le Comber [22]. The crucial difference between the TFT and the MISFET is that the channel is formed by the accumulation of charge carriers near the dielectric-semiconductor interface. There is no inversion of charge carriers in the channel as with MISFETs. For a p-type semiconductor, if a positive voltage is applied to the gate electrode, it operates in the depletion mode, and the channel region is depleted of charge carriers, resulting in a high channel resistance (off-state). For this reason, low off currents are only guaranteed by the low conductivity of the semiconductor. Meanwhile, if a negative voltage is applied to the gate electrode, it operates in the accumulation mode and a large concentration of charge carriers is accumulated in the channel, resulting in low channel resistance (on-state).

2.4.1 Charge Transport in Organic Semiconductors

The weak intermolecular interaction forces, normally Van der Waals bonds, result in a narrow bandwidth and strong interactions between free charge carriers and the lattice. This gives rise to polaron (self-localised charge) formation. These may be responsible for the low charge carrier mobilities in organic semiconductors. In contrast, the bonding energies in inorganic single-crystalline semiconductors are strong, due to covalent or ionic bonding, so that the charge carriers move in highly delocalised states in a wide bandwidth and have a very high charge carrier mobility.

In conventional single-crystalline inorganic semiconductors, charge transport occurs in delocalised states (band transport), and is limited by lattice vibrations, phonons, which scatter the charge carriers. Such a mechanism is not applicable to

disordered materials such as polymers. Here, charge transport may take place by hopping between localised states. Hopping is assisted by phonons and the charge carrier mobility, which increases with temperature, is given by

$$\mu = \mu_0 \exp\left[-\left(\frac{T_0}{T}\right)^{1/\alpha}\right] \tag{2.1}$$

where α is an integer ranging from 1 to 4 [23]. However, trapping attributed to grain boundaries and other structural defects in polycrystalline films significantly affects the temperature dependence of the charge carrier mobility [24].

While hopping is appropriate to describe charge transport in disordered materials, the multiple trapping and thermal release (MTR) model applies to well-ordered materials such as pentacene and oligothiophenes. Charge carriers interact with the localised levels, which act as traps, through trapping and thermal release. The effective field-effect mobility, μ_{eff} will be given by

$$\mu_{\text{eff}} = \mu_0 \alpha \exp\left[-\frac{(E_c - E_t)}{kT}\right] \tag{2.2}$$

where E_c is the energy of the transport level. In the case of a single trap level, E_t is the energy difference between the trap level and the transport level and α is the ratio of the effective density of states (DOS) at the transport level to the concentration of traps [23]. An important outcome of the MTR model is that the gate voltage dependence of the field-effect mobility can be explained by an energy distributed DOS. This will be discussed in more detail in section 2.4.6.

On the other hand, band-like transport in delocalised states becomes the dominant charge transport mechanism in single crystals of organic semiconductors. The boundary between band transport (delocalised process) and hopping (localised process) is normally defined by materials having room temperature charge carrier mobilities around 1 $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$. However, it is hard to guarantee that the mean free path l does not exceed the intermolecular distance, which is the necessary condition for the diffusive band-like transport except at very low temperatures. Podzorov et al. have made it possible to distinguish between the charge transport in delocalised

states and thermally activated hopping between localised states because of defects and impurities by measuring the Hall effect on single crystals of rubrene [25]. The results suggest a band-like transport in delocalised states as a possible charge transport mechanism in highly ordered organic semiconductors. An advantage of the Hall experiment is that it allows independent measurements of the density of charge carriers. The charge carriers, which are temporarily trapped in shallow traps, do not make a contribution to the Hall voltage. Thus, the mobility extracted from the Hall experiments should coincide with the intrinsic, trap-free mobility. Furthermore, Pernstich et al. have reported band-like transport not only in single crystals of rubrene but also in polycrystalline films of pentacene by measuring the thermopower (Seebeck coefficient) [26]. The thermoelectric voltage V_{therm} arises when two ends of a sample are held at different temperatures (ΔT) and the Seebeck coefficient S is given by

$$S = \frac{V_{therm}}{\Delta T}. \tag{2.3}$$

The general expression for the electronic contribution to the Seebeck coefficient is

$$S = \frac{k_B}{e} \int \frac{E_F - E}{k_B T} \cdot \frac{\sigma(E)}{\sigma} dE, \tag{2.4}$$

where k_B is the Boltzmann constant, $\sigma(E)$ is the electrical conductivity and includes terms describing the DOS and energy-dependent scattering mechanisms, σ is the total conductivity and T is the temperature [26]. For p-type semiconductors, the thermoelectric voltage can be given by rewriting Equations 2.3 and 2.4 in terms of valence band edge E_v and a weighted average $\mathcal{A}$ as

$$V_{therm} = \frac{k_B}{e} \left(\frac{E_F - E_v}{k_B T} + \mathcal{A} \right) \Delta T, \tag{2.5}$$

where E_F-E_v is the Fermi level position with respect to the valence band edge. The rate at which E_F changes with gate voltage depends on the trap density of the semiconductor. The quantity $\mathcal{A}$ accounts for carriers distributed beyond E_v. The

values of $\mathcal{A}$ in single crystals of rubrene (2.1∼3.6) have been found to be well within the range of the electronic contribution in conventional single-crystalline inorganic semiconductors (2∼4); depending on the nature of the scattering mechanisms up to room temperature, highlighting the similarity of transport mechanisms in single crystals of organic and conventional single-crystalline inorganic semiconductors. The values that have been found in the polycrystalline films of pentacene transistors are slightly smaller (1.7∼2.2); whereas in amorphous inorganic semiconductors the values are in the range of -7 to -11 [26].

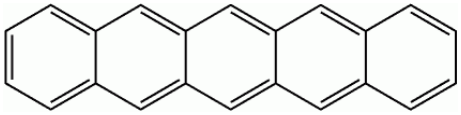
2.4.2 Organic Semiconductors

Various organic semiconductor materials have been used as the active layer in OTFTs. These include molecular crystals such as pentacene, which can be deposited in thin film form by thermal evaporation, and conductive polymers, which can be conveniently processed by solution-based methods, such as spin-coating and inkjet-printing [27].

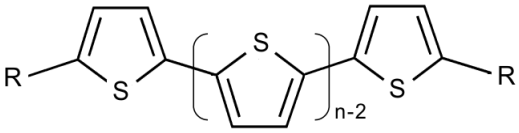
Small Molecules

Pentacene, oligothiophenes (nT, where n stands for the number of thiophene units) and phthalocyanines (Pcs) are the most representative p-type semiconductor materials based on small molecules. Vacuum deposition is the normal process for producing thin films of these materials. However, some compounds can be processed by solution-based methods using a soluble precursor molecule that may afford certain advantages in device fabrication.

Pentacene is a promising candidate for the active layer in OTFTs because of its high field-effect mobility. The molecule is a polycyclic aromatic hydrocarbon consisting of five aligned condensed benzene rings, called linear acenes or oligoacenes, as shown in Figure 2.3(a). Structurally, pentacene is one of the polyacenes, which were extensively studied as organic semiconductors during the 1960s and the 1970s. Oligothiophenes are also important small molecule p-type semiconductors for OTFTs. Oligothiophenes used in OTFTs are either non-substituted, or substituted at both ends by a linear alkyl group (Figure 2.3(b)). One of the most widely studied oligoth-



(a)



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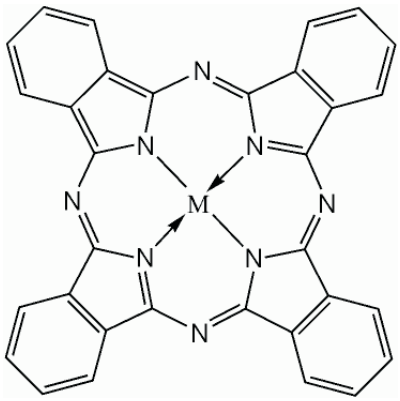


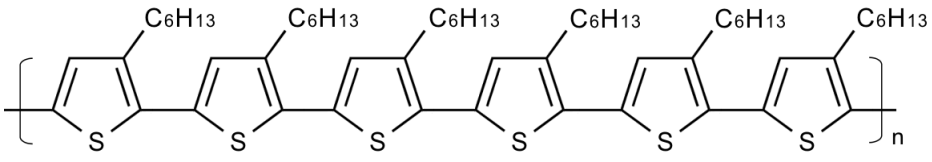
(c)

Figure 2.3: Chemical structure of (a) pentacene, (b) unsubstituted (R=H) and alkyl end-substituted (R=C_nH_{2n+1}) oligothiophenes and (c) metal phthalocyanine (Pc) where the central hydrogen atom is changed to the metal atom (M=H_2.)

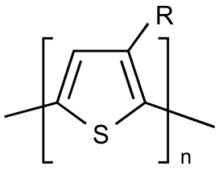
iophenes is α-6T. The outstanding performance of these small molecules has been attributed to their ability to form well-ordered polycrystalline films in a herringbone arrangement. Phthalocyanines are another of the first reported families of small molecule p-type semiconductors. The phthalocyanine molecule has the structure of a molecular cage, into which various metals can be introduced (Figure 2.3(c)). Most devices based on Pc are fabricated by vacuum deposition, i.e. thermal evaporation. However, the solution-based Langmuir-Blodgett (LB) technique has also been used. Furthermore, Pcs may be substituted with electron withdrawing groups at their periphery, such as hexadecafluoro-substituted copper Pc (R=F, M=Cu). These materials can exhibit n-type field-effect mobilities, as high as 0.03 cm^2 V^{-1} s^{-1}, under ambient conditions and with excellent stability [27].

Polymers

The carrier mobilities in polymers are still one order of magnitude lower than those of the small molecules as indicated in Figure 2.1. This can be explained by the fact that as solution-processed materials, polymers, provide poorer ordering than evaporated small molecules. This can result from the addition of soluble groups (e.g. alkyl chains) or soluble precursors.



(a)



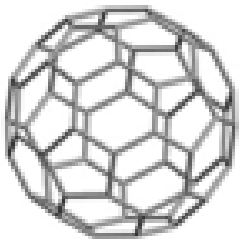
(b)

Figure 2.4: Chemical structure of (a) poly(3-hexylthiophene) (P3HT) and (b) poly(3-alkylthiophene) (P3AT) (R=C_4H_9, C_8H_{17}, $C_{10}H_{21}$ and $C_{12}H_{25}$).

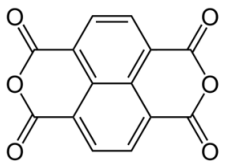
Polythiophenes (PTs) were the first solution-processed semiconductors used for OTFTs. Various derivatives have now been incorporated on the polymer backbone to impact functionality, increase solubility and induce self-assembly. The alkyl derivatives can be incorporated into a PT-based polymer chain with two types of arrangement, either head-to-tail (HT) or head-to-head (HH). A polymer with a mixture of HH and HT linkages in PT is referred to as regiorandom, while one with only HT linkages is referred to as regioregular [27]. Among PT-based polymers, poly(3-hexylthiophene) (P3HT), in which the addition of alkyl side-chains enhances the solubility of the polymer chains, is the most widely studied p-type semiconductor material (Figure 2.4(a)). Poly(3-alkylthiophene)s (P3ATs) are also important thiophene-based polymers with side chains ranging from butyl to dodecyl (Figure 2.4(b)).

n-Type Semiconductors

The development of n-type organic semiconductors will enable the fabrication of complementary logic circuits which have many advantages; high robustness, low power consumption and low noise. However, most of the organic semiconductors studied so far are p-type. Molecules such as unsubstituted pentacene or oligothiophenes are more conducive to the injection of holes than electrons. On the other hand, an n-type semiconductor is one in which electrons are more easily injected than holes.



(a)



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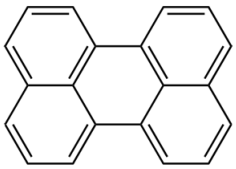
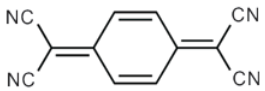


(c)



(d)

Figure 2.5: Chemical structure of (a) buckminsterfullerene (C_{60}), (b) naphthalene-tetracarboxylic-dianhydride (NTCDA), (c) perylene and (d) tetracyanoquinodimethane.

As mentioned above, substituted Pcs (R=F or Cl, M=Cu, Zn, Co or Fe) have exhibited n-type behaviour. Furthermore, ambipolar mobility has also been reported from water soluble copper Pcs substituted with sulfonic acid and methyl pyridnium groups. Fullerenes (e.g. C_{60}), which are molecules composed entirely of carbon in the form of a hollow sphere, ellipsoid or tube as shown in Figure 2.5(a), and their derivatives, were reported as n-type organic semiconductors in 1993. Since then, mobilities as high as 0.56 cm^2 V^{-1} s^{-1} have been reported for C_{60} films fabricated

by molecular beam deposition without breaking the vacuum [28]. A major problem of these materials is their strong instability with respect to oxygen, which acts as an electron trap within the C_{60} lattice. Naphthalene-tetracarboxylic-dianhydride (NTCDA), perylene and tetacyanoquinodomethane (TCNQ) have also been studied as n-type organic semiconductors and the chemical structure of these materials are shown in Figure 2.5. Recently, perfluoroalkyl substituted oligothiophenes and trifluoromethylphenyl, electron withdrawing group, based oligomers have been reported as novel n-type organic semiconductors.

2.4.3 Gate Dielectrics

The performance of OTFTs is determined by the charge carriers flowing at the interface between the active and gate dielectric layers. Consequently, the development of suitable insulating materials is an essential element in improving OTFTs. The operating voltage of the device, in particular, is determined directly by the thickness and permittivity of the gate dielectric.

In a MIS structure, the charge induced on the semiconductor surface as a function of applied voltage is given by

$$Q = CV = \left(\frac{\epsilon_0 \epsilon_r S}{d}\right) V \tag{2.6}$$

where S is the area, d is the distance between the electrode and the semiconductor, ϵ_0 and ϵ_r are the permittivity of free space and the dielectric constant of the dielectric, respectively. Increasing the capacitance, C, through the dielectric constant, ϵ_r, or reducing the film thickness, d, would reduce the voltage requirement necessary to induce the same amount of charge in the semiconductor. Besides the dielectric constant and the film thickness of the gate dielectric layer, the dielectric roughness (which is believed to reduce the mobility in organic semiconductors due to disorder induced at the accumulation layer), chemical/mechanical properties of the dielectric-semiconductor interface, ease of processing and reliability are also important factors to be considered for the selection and design of gate dielectric materials. To date, several classes of dielectric materials have been studied for OTFTs. These can be

Table 2.1: Overview of inorganic dielectric materials [2].

Material	Preparation method	Deposition temperature [°C]	Dielectric constant
SiO_2	Thermally grown	> 600	3.9
SiO_2	Ion beam sputtered	80	3.9
Al_2O_3	Sputtered	Not given	∼5.1
Al_2O_3	Anodised	Room temperature	∼4.2
TiO_2	Anodised	Room temperature	21
SiN_x	CVD	250∼350	6∼7
Ba(ZrTi)O	RF sputtered	Room temperature	17.3
Ba(SrTi)O	RF sputtered	Room temperature	16
Ta_2O_5	Sputtered	300	25

classified into inorganic (conventional or high dielectric constant) materials, organic (polymeric) materials, ultra-thin self-assembled monolayers (SAMs), multilayer and nanocomposite dielectric materials.

Inorganic Dielectrics

A wide range of inorganic dielectric materials have been studied and employed as the gate dielectric layer in OTFTs over the past decade. The availability of thermally grown silicon dioxide as the gate dielectric layer on heavily doped silicon (as the gate electrode) has made this the ideal system for the initial evaluation of almost all new organic semiconductors. Silicon dioxide has excellent insulating properties due to its large band gap (8.9 eV) and thermodynamic stability [27]. However, the advantages of organic electronics cannot be exploited fully with this material because thermally-grown silicon dioxide is not compatible with flexible substrates. As a result, a large number of other inorganic dielectric materials have been investigated. For example, silicon dioxide (SiO_2), barium zirconate titanate (Ba(ZrTi)O) and barium strontium titanate (Ba(SrTi)O) have been deposited by sputtering on transparent plastic substrates at low temperature. As another approach, alternative higher dielectric constant materials such as titanium dioxide (TiO_2) and tantalum oxide (Ta_2O_5), obtained via electrochemical anodisation of sputtered tantalum, are being considered. Some representative inorganic dielectric materials are listed in Table

Table 2.2: Overview of organic dielectric materials [27].

Material	Preparation method	Capacitance [nF/cm^{-2}]	Dielectric constant
Polystyrene	Spin-coated	19	2.6
Poly(methyl methacrylate)	Spin-coated	19.5	3.5
Poly(vinyl phenol)	Spin-coated	7.4	6.4
Poly(vinyl alcohol)	Spin-coated	17.8	10
Benzocyclobutene	Spin-coated	47	2.65
Parylene C	Vapour deposited	2.2	3.1
Cyanoethylpullulan	Spin-coated	Not given	12

2.1 [2].

Polymer Dielectrics

Polymers that can be deposited by spin-coating, dip-coating or inkjet-printing present a second major class of materials for the gate dielectric, since most organic polymers are insulators by nature. It has been reported that several polymers show excellent insulating characteristics with very low leakage currents. Representative polymers are polystyrene (PS), poly(methyl methacrylate) (PMMA), poly(vinyl alcohol) (PVA), poly(vinyl phenol) (PVP), benzocyclobutene (BCB), parylene C and cyanoethylpullulan (CYEPL). These are listed in Table 2.2 and their chemical structures are shown in Figure 2.6. Common materials such as PS and PMMA were the first polymers to be used as gate dielectrics. However, PVA and PVP are two of the most widely used polymer dielectric materials. These can be deposited onto organic semiconductors because the solvents (aqueous for PVA and ethanol for PVP) for these materials are orthogonal to those used for the semiconductor. Furthermore, the robustness of these two materials can be enhanced by cross-linking, using chemical agents such as melamine-co-formaldehyde or hexamethylene tetraamine. Such materials generally show low capacitances and the corresponding OTFTs operate at relatively high voltages. In contrast, OTFTs with siloxane cross-linked ultra-thin polymeric films generated by spin coating have recently shown the encouraging results of high capacitance (300 nF cm^{-2}), insolubility and low leakage currents (10^{-8} A cm^{-2}) [29–32]. A robust siloxane network formed by chemical agents (e.g. 1,6-

bis(trichlorosilyl)hexane) significantly improves the insulating quality, allowing films as thin as 10 nm to be produced.

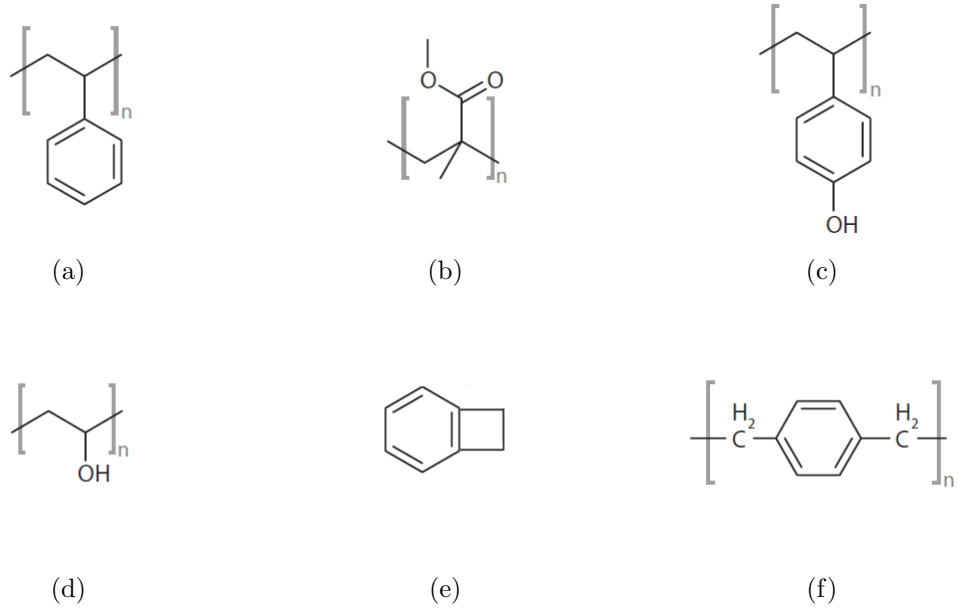


Figure 2.6: Chemical structure of (a) polystyrene (PS), (b) poly(methyl methacrylate) (PMMA), (c) poly(vinyl phenol) (PVP), (d) poly(vinyl alcohol) (PVA), (e) benzocyclobutene (BCB) and (f) parylene.

Self-assembled Monolayer (SAM) Dielectrics

Ultra-thin SAMs are also very promising dielectrics for low-voltage OTFTs because of the short chain length (∼x nm) and dense packaging of the SAMs. The SAMs, which have been used as surface treatments, can function as a dielectric under careful preparative conditions. There are two approaches for generating molecular insulating layers: bottom-up and top-down. The former technique, where the final insulating layer is created by self-assembly from a precursor followed by one or more chemical modifications, shows excellent electrical characteristics but requires multiple chemical reactions. The other approach is the use of preliminarily modified molecules which can form dense SAMs such as alkyltrichlorosilane with an aromatic end-group. It has been reported that SAMs with a thickness of 2.5 nm provide a capacitance near 1 μF cm^{-2}. The leakage current density is less than 10^{-9} A cm^{-2} for fields up to 14 MV cm^{-1} [33]. However, pathways for integration into large-volume

coating processes are less obvious because of defects in the SAMs arising from the imperfect surface of the target film.

Multilayer and Nanocomposite Dielectrics

Multilayers, which are combinations of inorganic/organic dielectrics with organic/inorganic monolayers or thin polymer phases, have been investigated to modify the surface of dielectric materials. The additional layer normally helps to smooth the roughness of the dielectric surface and improve the crystalline grain growth of the active materials. Examples of additional SAMs are octadecyl-trichlorosilane (OTS) on silicon oxide dielectrics [34], alkyl phosphonic acid monolayers on alumina dielectrics [35] and octadecyl-trimethoxysilane (OTMS) on ziconium oxide dielectrics [36]. Polymers such as polystyrene [37] or poly(α-methylstyrene) [38] on oxide dielectrics have also been used to improve the performance of OTFTs. It has been reported that the use of an additional layer has a significant improvement on the device characteristics (e.g. field-effect mobility). However, the effect on the dielectric properties is less marked because the thickness of the additional layer is much less than the thickness of the gate dielectric.

A further method is to blend ceramic and polymeric materials on the nanoscale in order to generate nanocomposite dielectrics. For example, the value of the dielectric constant can be increased from 3.5 for the traditional polymer dielectric (PVP) to 5.4 for the nanocomposite dielectric containing 7 % nanoparticles (TiO_2-PVP) [39].

2.4.4 Contact Resistance

If the source and drain contacts are ohmic, meaning the value of the contact resistance is negligibly small in comparison with the channel resistance, these can inject and retrieve all of the charge carriers through the channel under given bias conditions. According to the conventional Mott-Schottky (MS) model, contacts are expected to be ohmic when the work function of the metal is close to the highest occupied molecular orbital (HOMO) or lowest unoccupied molecular orbital (LUMO) level of the semiconductor, for p- and n-type semiconductors, respectively. Otherwise, an energy barrier forms at the metal-semiconductor interface which prevents

charge injection. However, many metal-organic semiconductor interfaces do not follow the MS model. For example, Figure 2.7 shows a proposed energy level diagram for the gold-pentacene interface, which exhibits an additional interface dipole barrier (Δ) determined by ultraviolet photoelectron spectroscopy [40]. The interface dipole barrier shifts up the gold vacuum level by more than 1 eV, hence there is a 0.85 eV large barrier for hole injection at this contact. The origin of this interface dipole barrier has several explanations, including charge transfer between the semiconductor and the metal, reduction of the metal work function by adsorption of the semiconductor and population of metal-induced mid-gap states at the interface. Despite a large barrier at the metal-semiconductor interface, it is possible to make ohmic contacts in OTFTs because charge injection mechanisms at metal-semiconductor interfaces are probably not due to thermionic emission, in which charge carriers must overcome the full potential barrier. Instead, field emission (tunnelling) through the barrier and/or defect-assisted transport in which charge carriers bypass the barrier by hopping can become possible.

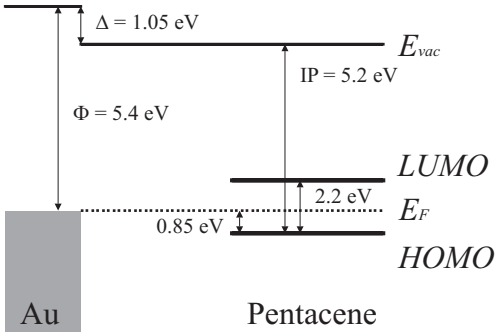


Figure 2.7: Band line-up diagram for the gold-pentacene junction [40].

Another critical issue concerning the contact resistance is the channel dimensions. In a typical OTFT, the total resistance is given by

$$R_{total} = R_{channel} + R_{contact} = R_{channel}^{sheet}\frac{L}{W} + \frac{R'_{contact}}{W} \tag{2.7}$$

where $R_{channel}^{sheet}$ is the channel sheet resistance, $R'_{\ contact}$ is the normalised contact resistance and L and W are the channel length and channel width of the device,

respectively. This equation implies that contact resistance can be a substantial part of the total resistance as the channel length is scaled down. Furthermore, the magnitude of the contact resistance compared to the channel resistance at high gate voltage must be considered in order to be ohmic because the channel resistance decreases with increasing gate voltage.

2.4.5 Device Structures of OTFTs

Figure 2.8 shows the various OTFT configurations resulting from the order in which the semiconductor layer, dielectric layer, source/drain (S/D) electrodes and the gate electrode are deposited on the substrate.

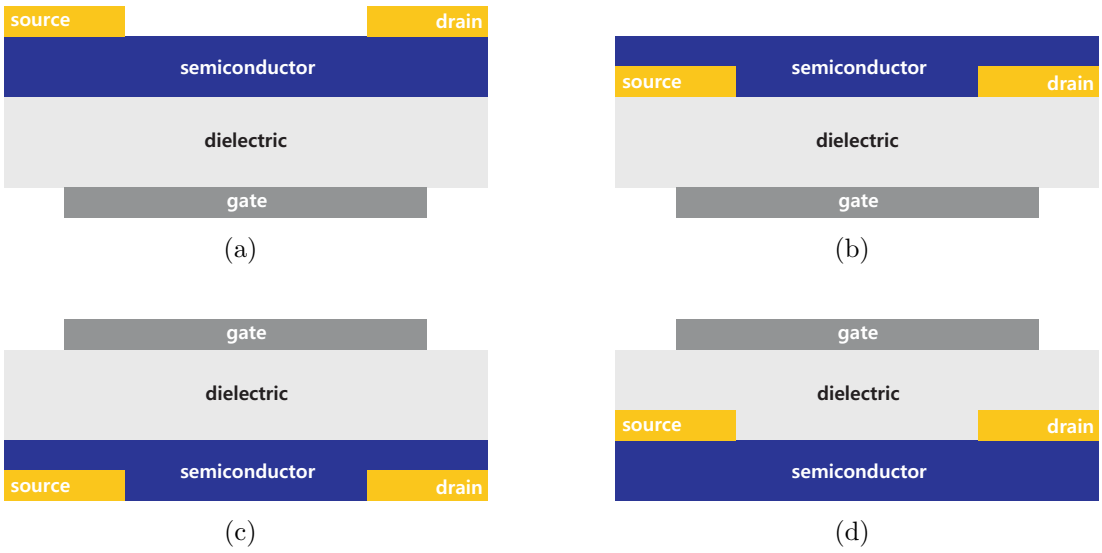


Figure 2.8: Schematic diagrams of OTFTs with (a) bottom-gate, top-contact (BG-TC) configuration, (b) bottom-gate, bottom-contact (BG-BC) configuration, (c) top-gate, bottom-contact (TG-BC) configuration and (d) top-gate, top-contact (TG-TC) configuration.

The S/D electrodes must be in direct contact with the semiconductor to inject and retrieve charge carriers; the gate electrode must be isolated from the semiconductor by the dielectric layer. In the case of the bottom-gate configuration, the gate electrode followed by the dielectric layer are first deposited onto the substrate. This can be achieved in two ways. In the first, referred to as a bottom-gate and top-contact (BG-TC) configuration (Figure 2.8(a)), the S/D electrodes are formed on top

of the semiconductor layer, whereas for the bottom-gate and bottom-contact (BG-BC) configuration (Figure 2.8(b)), the semiconductor is deposited on predeposited S/D electrodes. Each of these configurations has its advantages and drawbacks. In the BC configuration, the S/D electrodes can be patterned by fine photolithographic methods because the semiconductor is deposited on-top. However, the contact resistance has been reported to be lower in the TC configuration than in the BC configuration, giving better device performance [2]. This is likely because of the increased metal-semiconductor contact area in the TC configuration.

Another architecture is the top-gate and bottom-contact (TG-BC) configuration, as shown in Figure 2.8(c). From the process integration view, the deposition of the dielectric on the semiconductor layer is much harder than the other way around because of the relatively 'fragile' properties of the semiconductor layer. In this configuration, however, the dielectric layer not only acts as the gate insulator but also serves as a passivating layer for the semiconductor.

2.4.6 Electrical Characteristics of OTFTs

For low V_{DS} ($V_{DS} < V_{GS}$), the drain-source current is related to the drain-source voltage by

$$I_{DS(lin)} = \frac{WC_i}{L}\mu\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS} \tag{2.8}$$

where V_T is the threshold voltage, C_i is the insulator capacitance per unit area and μ is the field-effect mobility. The threshold voltage represents the value of the gate-source voltage beyond which a conductive channel forms at the pentacene surface (i.e. the transistor is turned on). This defines the linear region of device operation. For high V_{DS}, the drain-source current saturates as the conductive channel becomes 'pinched-off' as shown in Figure 2.9. The saturated drain-source current, $I_{DS(sat)}$, is given by

$$I_{DS(sat)} = \frac{WC_i}{2L}\mu(V_{GS} - V_T)^2 \tag{2.9}$$

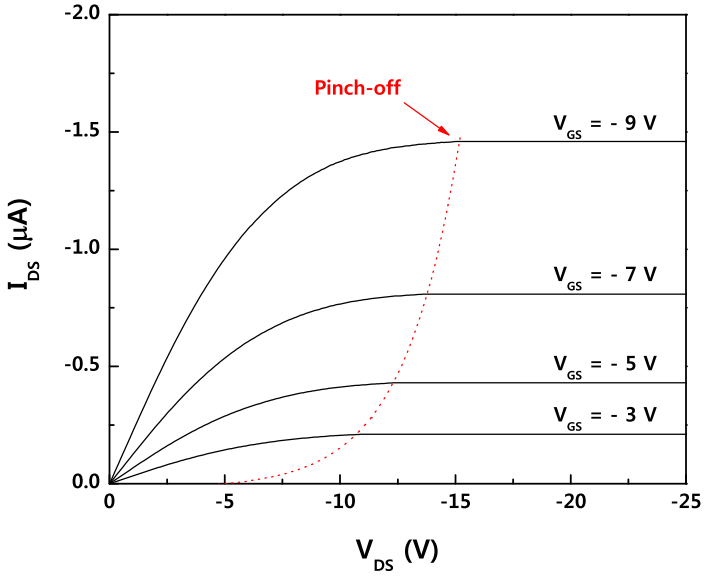


Figure 2.9: Output characteristics for a typical OTFT based on a p-type semiconductor. The dashed line indicates where the channel of the OTFT becomes pinched-off.

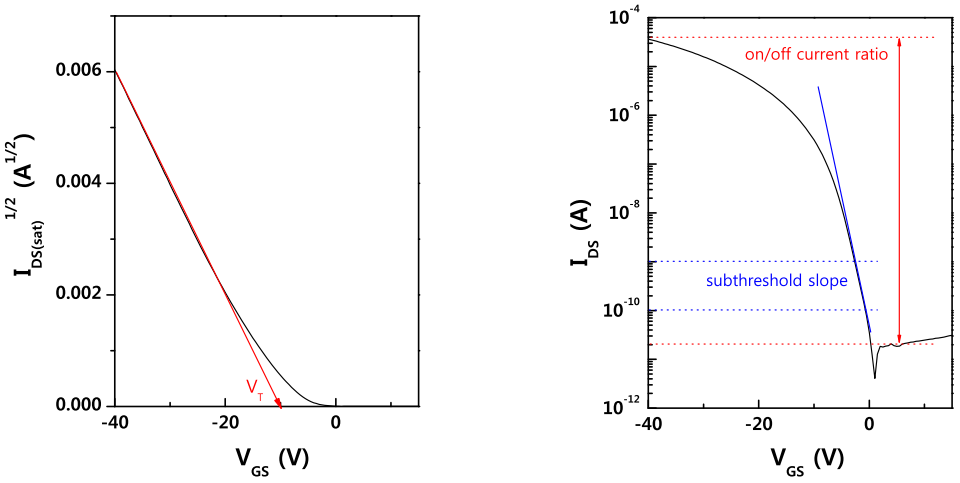
The field-effect mobility of an OTFT is typically calculated either in the linear regime where I_{DS} depends linearly on V_{DS} or in the saturation regime where I_{DS} is independent of V_{DS}. In this linear regime, the field-effect mobility, μ_{lin}, can be calculated through the transconductance, g_m, which follows from the derivative of Equation 2.8.

$$g_m = \left[\frac{\delta I_{DS}}{\delta V_{GS}}\right]_{V_{DS}=const.} = \frac{WC_i}{L}\mu_{lin}V_{DS} \tag{2.10}$$

The saturation field-effect mobility, μ_{sat}, in the saturation regime can be given by rewriting Equation 2.9 as

$$\frac{\delta(I_{DS})^{1/2}}{\delta V_{GS}} = \left(\frac{WC_i\mu_{sat}}{2L}\right)^{1/2} \tag{2.11}$$

The value of μ_{sat} may therefore be evaluated from a plot of ${I_{DS(sat)}}^{1/2}$ versus V_{GS} (Figure 2.10(a)). The intercept of this plot can be used to determine the device threshold voltage as shown in Figure 2.10(a). In this thesis, the straightest part of the plot is used to determine the values of μ_{sat} and V_T and an average value is used for the hysteresis plot. The on/off current ratio and subthreshold slope are extracted from a plot of $I_{DS(sat)}$ on a logarithmic scale versus V_{GS} (Figure 2.10(b)).



(a) (b)

Figure 2.10: Transfer characteristics for a typical OTFT based on a p-type semiconductor in the form of (a) ${I_{DS(sat)}}^{1/2}$ versus V_{GS} and (b) $I_{DS(sat)}$ on a logarithmic scale versus V_{GS}.

Although Equations 2.10 and 2.11 are still widely used to extract the field-effect mobility of OTFTs, it has now been clearly established that the field-effect mobility in most OTFTs based on small molecules is gate bias dependent [41–45]. According to the model of Necliudov and coworkers [41], in pentacene-based OTFTs operating above threshold, most of the charge carriers induced by the gate-source voltage are trapped in numerous traps and only a fraction of the charge carriers participate in the current conduction. The effect of the charge trapping is accounted for by the gate-voltage dependent field-effect mobility [41] given by

$$\mu = \mu_0 \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma} \tag{2.12}$$

where γ and V_{AA} are empirical parameters that can be extracted from the transfer characteristics and μ_0 is a constant. As V_{GS} increases, the Fermi level at the insulator-semiconductor interface moves toward the transport level and more traps are filled. Eventually, the energy separation between the filled traps and the transport level is reduced, so trapping becomes less efficient and the field-effect mobility increases [46]. This explanation is consistent with the model of polycrystalline sexithiophene (6 T) TFTs by Horowitz and coworkers [42]. Here, a MTR model is used to estimate the density of trap states and an empirical law of the form

$$\mu = \alpha(V_{GS} - V_T)^{\beta} \tag{2.13}$$

is assumed to represent the field-effect mobility. This leads to a temperature and gate voltage dependent field-effect mobility, which is given by

$$\mu = \mu_0 \frac{N_c}{N_{t0}} \left(\frac{C_i V_{GS}}{q N_{t0}} \right)^{(T_c - T)/T} \tag{2.14}$$

where N_{t0} is the total surface density of traps, N_c is the effective density of states, C_i is the insulator capacitance per unit area, V_{GS} is the gate bias and T_c is the characteristic temperature of the exponential variation of the distribution [42]. However, it is significant that in devices based on single crystals of organic semiconductors, the field-effect mobility is seldom dependent on the gate bias, which supports the view that the gate bias dependence originates from the localised levels attributed to the grain boundaries and other structural defects. Furthermore, V_{GS} modulates the contact resistance and it is observed that the contact resistance decreases with increasing V_{GS} [46].

Thus, despite their widespread use, the above equations should only be used for estimating an approximate value of the field-effect mobility in OTFTs. In this thesis, the saturation field-effect mobility is used for the comparison because the mobility

values of pentacene OTFTs most often reported in the literature are calculated in the saturation regime [7].

2.5 Methodology

It is evident from the literature review that the interface between the semiconductor and the insulator determines the performance of OTFTs. While the promise of pentacene as the semiconductor has generated great interest, there have been extensive studies on different polymeric materials as the gate insulator. Among the various polymer gate insulators, devices using PVP possess high values of charge carrier mobility. However, these can also exhibit a hysteresis behaviour that leads to a threshold voltage shift depending on the direction of the gate-source voltage sweep. Therefore PMMA, which exhibits a minimal hysteresis and facilitates good ordering of the pentacene molecules as these are deposited on the surface, is a promising candidate for organic gate insulators.

Therefore, the purpose of this work is to create a more extensive study on pentacene-based organic electronic devices with a PMMA gate dielectric. The work demonstrates (a) hysteresis-free pentacene OTFTs and (b) low voltage operating devices using physically cross-linked PMMA as the gate dielectric. Furthermore, this work reports on the electrical behaviour of cross-linked PMMA as gate dielectric for memory devices and solution processable OTFTs.

2.6 Conclusions

Organic electronics possess two key advantages over structures fabricated from inorganic semiconductors: mechanical flexibility and low-cost manufacture. These benefits generate new opportunities for organic electronics such as flexible displays, smart cards, disposable sensors and artificial skin.

Significant advances in organic electronics are being made across a broad range of activities, from enhanced understanding of very fundamental phenomena to improving manufacturing technologies. As a result, the performance of the best organic semiconductors is now competing with those of their inorganic counterparts and

industrial applications of organic electronics are emerging in the market place.

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Chapter 3

Experimental Techniques

3.1 Introduction

For most applications of organic electronics, the organic materials are required to be in the form of thin films. The term 'thin' is generally taken to describe 1 nm to 10 μm. A large number of thin film processing techniques have already been developed for the fabrication of organic electronics. The choice of process is determined by the nature of the material and the desired properties of the film. For example, small molecules can be sublimed using thermal evaporation whereas polymers are usually deposited by spin-coating and amphiphilic compounds (i.e. those incorporating both polar and nonpolar groups) can be deposited layer by layer using the Langmuir-Blodgett (LB) technique.

The physical (structural) and electrical characteristics of thin films can be investigated in many different ways. The most crucial physical properties of the thin films, such as thickness, roughness and surface morphology, are measured by ellipsometer, the quartz crystal microbalance and the atomic force microscope (AFM). Electrical properties such as conductivity (resistivity) and permittivity can be characterised by two or four-point probe methods and impedance analysis, respectively.

In this chapter, an overview of the most popular techniques that may be used to fabricate semiconductor thin films, dielectric thin films and the contact electrodes of organic thin-film transistors (OTFTs), including the interface layer between the semiconductor and dielectric, will be described. The experimental details are provided in Section 3.3 and physical characterisation methods for thin films and electrical characterisation for thin films and OTFTs are then given in Section 3.4. Finally,

Section 3.5 is concerned with the description of the semiconductor and dielectric materials that are used in this thesis.

3.2 Film Deposition

3.2.1 Physical Vapour Deposition

Physical vapour deposition (PVD) involves the deposition of molecules from the vapour phase to the solid phase onto a desired substrate. Thin films can be grown by the basic techniques of evaporation and sputtering.

Thermal Evaporation

Solid materials vaporise when heated to a sufficiently high temperature. Thin film deposition then occurs as molecules are removed from a solid or liquid (generation of the depositing species) and then travel over some distance in a vacuum chamber (transport of species from source to substrate) and impinge on the substrate (film growth on the substrate). According to the Langmuir expression, the rate of evaporation Γ (in kg m^{-2} s^{-1}) from a surface is given by

$$\Gamma = P\left(\frac{M}{2\pi RT}\right)^{\frac{1}{2}} \tag{3.1}$$

where P is the vapour pressure (in N m^{-2}) of the material at temperature T (in K), M is the molecular weight and R is the gas constant [1]. Even in a vacuum chamber, the molecules travel at high velocities making frequent collisions with residual gas molecules such as N_2, O_2, H_2O and CO_2. From kinetic theory, the mean free path of gas atoms (λ) is given by

$$\lambda = \frac{k_B T}{P\pi d^2\sqrt{2}} \tag{3.2}$$

where d is the diameter of the molecules and k_B is Boltzmann's constant [1]. Thus it is necessary to use low pressures, which lead to straight line paths between the source and the substrate. In the pressure range of 10^{-5} $\sim$$10^{-8}$ torr, the mean free

path is very large (5×10^2 to 10^5 cm) as compared to the source-to-substrate distance. Important features of thin film growth are the evaporation rate, substrate temperature and the chemical and physical natures of the substrate surface. Residual gas molecules in the chamber also have an effect − the more residual gas molecules, the more likely it is for some of these to be trapped in the film or for chemical reactions between residual gas molecules and evaporated molecules to occur.

A schematic diagram of a thermal evaporation system is shown in Figure 3.1.

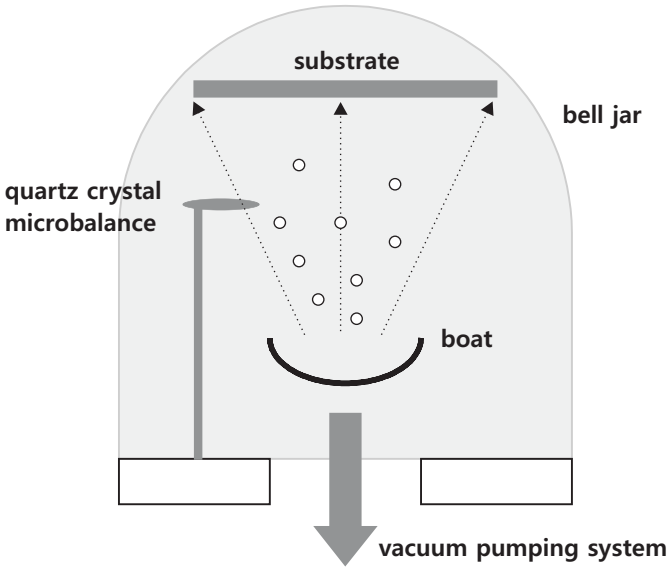


Figure 3.1: Thermal evaporation system for thin film deposition.

Typically, this consists of a bell jar, a vacuum pumping system, a 'boat' where the source material can be thermally heated to the sublimation temperature by Joule effects or sometimes with an electron gun, and a substrate mount. A quartz crystal microbalance is generally used to measure the thickness of the film by monitoring the change of its oscillating frequency as the evaporating species condenses on it.

Sputtering

Sputtering is based on the momentum exchange of accelerated ions incident on a target of source material [2]. At very low kinetic energies (< 5 eV) the interaction is confined to the outermost surface layer of the target material. Ions, such as Ar and Xe, are used for bombardment as these can be accelerated to any desired kinetic

energy with applied electric fields. A source of ions can be supplied in a number of different ways, for example by a glow discharge (diode, triode and magnetron) or an ion beam. However, non-magnetron sources, especially ion beam sources and the RF planar diode, are widely used.

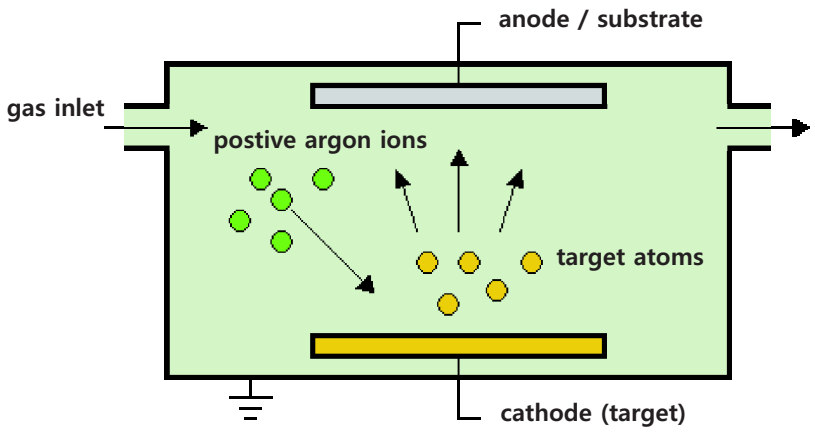


Figure 3.2: DC planar diode system for thin film deposition.

Figure 3.2 shows a schematic diagram of a simple DC planar diode sputtering system. It consists of two electrodes, the cathode and anode, within the chamber and an external high-voltage power supply. The material to be sputtered, the target, is the cathode. The chamber is pumped down by the vacuum pumping system to pressures well below the desired operation pressure. At this base pressure, gas is admitted back into the chamber to the desired pressure. A high electric field is applied between the electrodes, which causes the gas to become ionised and form a plasma. Positive gas ions are then accelerated by the electric field so that they arrive at the cathode with considerable energy and sputter the target atoms. Some secondary electrons are also produced at the cathode and these accelerate towards the anode and help to maintain the plasma. For the use of insulating materials as either sputtering targets or as substrates in the sputtering system, a DC potential cannot be used because of the accumulation of biased surface charges; RF power must be applied to the electrodes. The sputtering technique has been used with some organic polymers, such as polytetrafluoroethylene (PTFE), which are difficult to evaporate [1]. However, a relatively large amount of the material is required as a target.

3.2.2 Chemical Vapour Deposition

Chemical vapour deposition (CVD) involves introducing gaseous species into a chamber containing one or more heated substrates on which chemical reactions occur, resulting in the deposition of a thin film on the substrates [4]. The CVD process is based on the decomposition and/or radical generation of chemical species by stimulating vapour with heat (thermally activated CVD), plasma (plasma-enhanced or plasma-assisted CVD) or light (photon-assisted or laser-induced CVD).

The chemical reactions used in CVD can be divided into pyrolysis (thermal decomposition), reduction, oxidation, disproportionation and co-deposition reactions [4]. Pyrolysis reactions are the simplest. For example, silicon films can be deposited by thermally decomposing silane: $SiH_4 \rightarrow Si(s) + 2H_2$. Other pyrolysis reactions include the decomposition of methane to form diamond or diamond-like carbon: $CH_4 \rightarrow C(s) + 2H_2$ and the decomposition of nickel cabonyl to deposit nickel metal: $Ni(CO)_4 \rightarrow Ni(s) + 4CO$. Reduction reactions of halide precursors, in which a hydrogen carrier gas is used to provide the reducing agent in excess, are also commonly used reactions. One example is the formation of tungsten films from its hexafluoride: $WF_6 + 3H_2 \rightarrow W(s) + 6HF$. Oxidation and hydrolysis reactions can be used to produce oxide films. Oxygen or water is added to the system to oxidise the main chemical species, removing hydrogen or halide atoms from them. A well-known example is the oxidation of silane: $SiH_4 + 2O_2 \rightarrow SiO_2(s) + 2H_2O$. Disproportionation reactions are those in which two similar molecules, or groups of a molecule, exchange parts to form nonidentical products. Co-deposition reactions are the other common technique used for compound materials in metal organic CVD (MOCVD). One example of this kind of reaction is that between the organometallic compound trimethylgallium and arsenide to form gallium arsenide and methane: $Ga(CH_3)_3 + AsH_3 \rightarrow GaAs(s) + 3CH_4$.

Organic Vapour Phase Deposition

Low pressure organic vapour phase deposition (OVPD) has been used as an alternative to thermal evaporation and significantly improves control over doping. The method uses a carrier gas for transporting organic molecules from the source

to the substrate [3]. In OVPD, evaporation of organic material occurs in individual and decoupled quartz pipes, as shown in Figure 3.3.

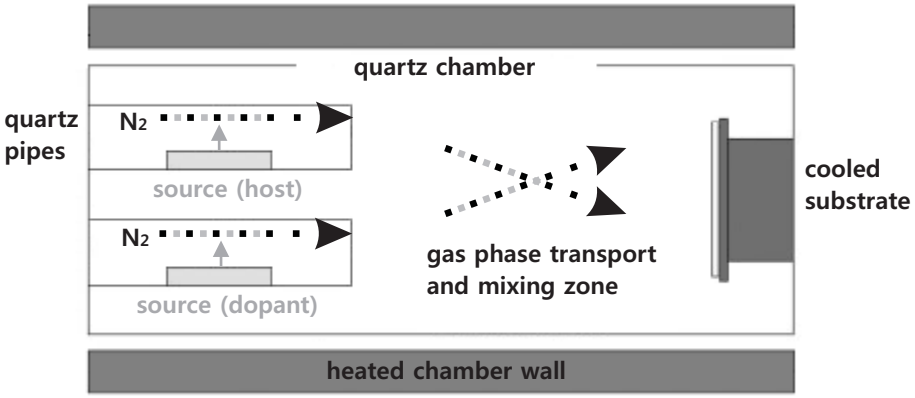


Figure 3.3: Schematic diagram of organic vapour phase deposition (OVPD) process.

A diluting and non-reactive gas stream such as nitrogen is added into each quartz pipe to transport the organic molecules into the hot-walled reactor where they are uniformly mixed and then condense on a cooled substrate.

Almost every organic material used in thin film devices possesses a sufficiently high vapour pressure to be evaporated at temperatures below 400 °C, and then to be transported in the vapour phase by a carrier gas. Thus, the evaporation source can be placed outside of the hot-walled reactor. This allows the separation of the functions of evaporation and transport. As a result, the rate of deposition of each material can be controlled as a function of the carrier gas flow, with individual evaporation temperatures and pressures. The component streams must be mixed prior to deposition to produce doped films with uniform composition across the entire substrate area. Thickness uniformity of the deposited films can be improved by carrying out the process at reduced pressure, which increases the gas diffusivity, resulting in improved rates of mass transfer between component streams and the substrate.

3.2.3 Spin-Coating

The spin-coating technique is used for depositing uniform thin films, generally polymers, onto flat substrates such as silicon wafers or glass slides. The various stages involved are shown in Figure 3.4. An excess amount of a solution is first dispensed on the substrate, which is then rotated at a fixed speed of several thousand rpm (or the solution can be applied while the substrate is slowly rotating). The solution spreads outwards, reducing the fluid layer thickness. Finally, evaporation of the solvent results in a film of uniform thickness [1]. The theoretical model for this process is given by

$$d = \left(\frac{\eta}{4\pi\rho\omega^2}\right)^{\frac{1}{2}} \left(\frac{1}{t}\right)^{\frac{1}{2}} \tag{3.3}$$

where d is the thickness of the spun film, η is the viscosity coefficient of the solution, ρ is its density, ω is the angular velocity of the spinning and t is the spinning time [5]. Thus, the film thickness is independent of the quantity of solution initially dispensed on the substrate. This equation works well for practical concentrations of solutions with the exception of dilute solutions which show pinholes in the final film.

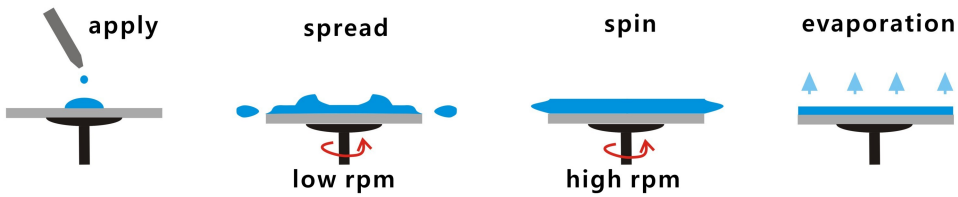


Figure 3.4: Schematic diagram of spin-coating.

3.2.4 Inkjet-Printing

Inkjet-printing is a direct marking technique for device patterning. The general operation of inkjet-printing consists of 5 steps: filling, jetting, flight, adsorption and drying as depicted in Figure 3.5. The liquid is taken from the ink reservoir to the printer dispenser through a delivery path by applying a pressure differential between the reservoir and the printer dispenser (filling) and ejected through a nozzle as a

series of droplets (jetting and flight). When the droplet strikes the substrate, it may be adsorbed (adsorption) and form a solid layer on the substrate (drying).

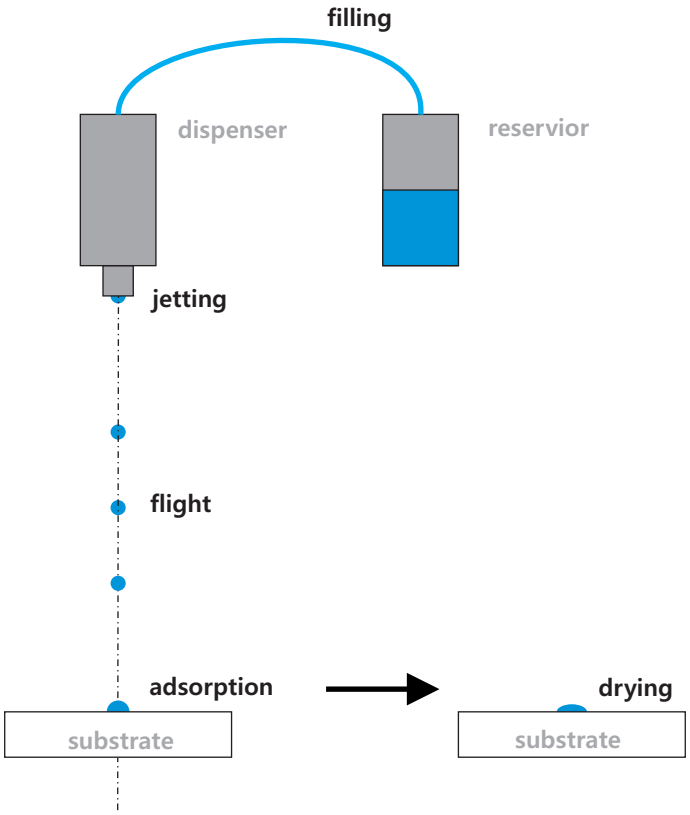


Figure 3.5: Schematic diagram of inkjet-printing.

The two common types of inkjet dispensers for drop-on-demand printers are piezoelectric crystal dispensers (piezoheads) and thermoelectric dispensers (bubble jet heads). Jetting occurs in a similar manner in both cases; a pressure wave is generated which forces ink out of a nozzle. However, the way that dispensers generate the pressure wave and the way that the pressure wave causes jetting are different. In bubble jet heads, a heater in the form of a thin film resister is used. By applying a short heating pulse through the thin film resistor, the ink is vapourised and a bubble is created. The bubble is created within a few microseconds and causes pressures typically > 1 MPa that cause jetting [6]. On the other hand, piezoheads use a piezoelectric crystal. Applying an electric potential across the piezoelectric crystal causes its shape to deform which generates the pressure wave and expels the ink droplets [7]. This type is the most suitable dispenser for the use of organic

electronics because it applies no thermal load to the ink.

The ink being printed must have suitable properties to ensure proper jetting; the boiling point, evaporation rate, surface tension and viscosity are important parameters. The viscosity must be low enough to allow for rapid refilling and the surface tension must be sufficiently high to hold the ink in the nozzle without dripping. Furthermore, viscosity and surface tension determine the amplitude and the length of the pulse to eject ink. A proper boiling point and evaporation rate are also required so as not to clog the orifice of the dispenser or cause unstable jetting.

3.2.5 Thermal Oxidation

Thermal oxidation is a technique that uses high temperatures to promote the growth of oxide layers on silicon. Silicon wafers are placed in a quartz glassware boat and are exposed to a flow of pure dry oxygen (dry oxidation), or water vapour (wet oxidation), at a temperature between 900 and 1200 °C. A schematic diagram of thermal oxidation is shown in Figure 3.6. An oxidising agent then reacts at the surface of the wafer to from a new layer of silicon dioxide. The following reactions describe the thermal oxidation of silicon in oxygen or water vapour: $Si(s) + O_2 \rightarrow SiO_2(s)$ or $Si(s) + 2H_2O \rightarrow SiO_2(s) + 2H_2$.

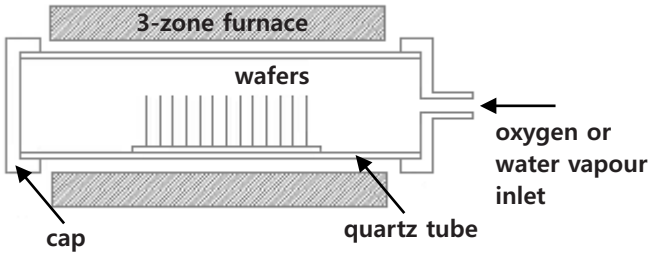


Figure 3.6: Schematic diagram of thermal oxidation.

The rate of oxide growth with time can be described mathematically by the Deal-Grove model. For oxide growing on an initially bare silicon wafer, the thickness X_{ox} at time t is given by the following equation:

$$t = \frac{{X_{ox}}^2}{B} + \frac{X_{ox}}{B/A} \tag{3.4}$$

where the constants A and B encapsulate the properties of the reaction and the oxide layer, respectively [8].

3.2.6 Langmuir-Blodgett Deposition

The LB technique, which is generally restricted to the deposition of organic materials, can provide monolayer and multilayer structures with a high degree of order of the constituent molecules [9]. The organic materials used in LB deposition are normally amphiphilic compounds (e.g. long chain fatty acids and alcohols) with hydrophilic (polar head group) and hydrophobic (nonpolar tail group) constituents. Figure 3.7 shows the chemical structure of a representative amphiphilic compound, n-octadecanoic acid (stearic acid). The nonpolar hydrocarbon -CH_2- group of the molecule is responsible for the material's repulsion from water while the polar carboxylic acid -COOH group of molecule confers some water solubility.

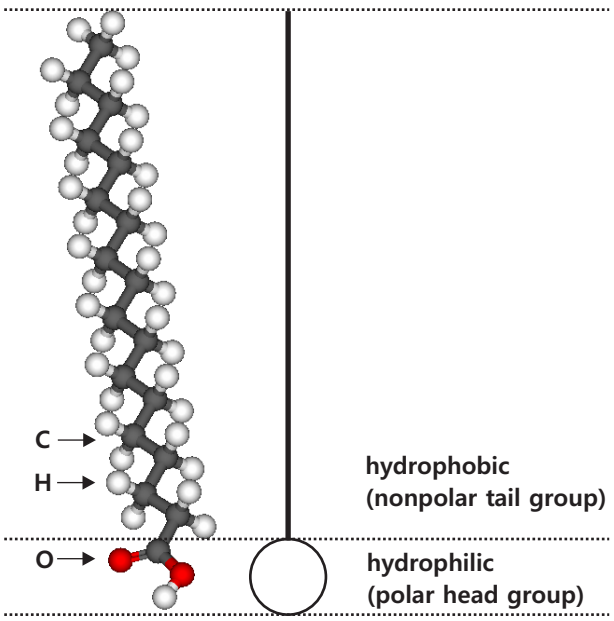


Figure 3.7: Chemical structure of n-octadecanoic acid (stearic acid).

Phase changes for the LB film formation can be provided by a plot of surface pressure (Π) as a function of the area occupied by the film (a). At very large surface

areas, the molecules are so far apart that there are negligible interactions between them (gaseous monolayer phase). As the surface area is reduced with higher pressure, the hydrocarbon chains will begin to interact (liquid expanded monolayer phase). As the surface area is progressively reduced with more pressure, the liquid becomes compressed into a close packed array of molecules on the surface corresponding to a solid state (condensed phase). This trend continues up to a point where the molecules are very closely packed and have very little room to move. Applying an increasing pressure at this point (collapse pressure, Π_c) causes the monolayer to become unstable and molecules are ejected out of the monolayer.

Three different deposition methods are observed for LB films. The most frequently encountered deposition method is Y-type deposition, where a monolayer is deposited on each traversal of the monolayer/air interface, and the molecules stack in a head-to-head and tail-to-tail pattern as shown in Figure 3.8(a). In Z-type deposition, a monolayer is transferred on the upstroke only and molecules are aligned head-to-tail with the head on the substrate. In X-type deposition, a monolayer is transferred on the downstroke only and molecules are aligned head-to-tail as with Z-type, but with the tail on the substrate. These deposition modes are illustrated in Figure 3.8(b) and Figure 3.8(c).

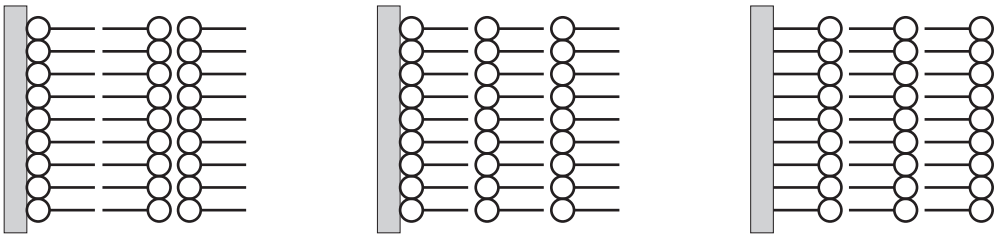


Figure 3.8: (a) Y-type (hydrophilic substrate), (b) Z-type (hydrophilic substrate) and (c) X-type (hydrophobic substrate) Langmuir-Blodgett film deposition.

3.2.7 Self-Assembly

Self-assembly is a simple process in which monolayers are formed by immersing an appropriate substrate into a solution of the surface-active material. This process is determined predominantly by strong interactions between the head group of the

self-assembling molecule and the substrate, resulting in a chemical bond between the head group and a specific surface site [1].

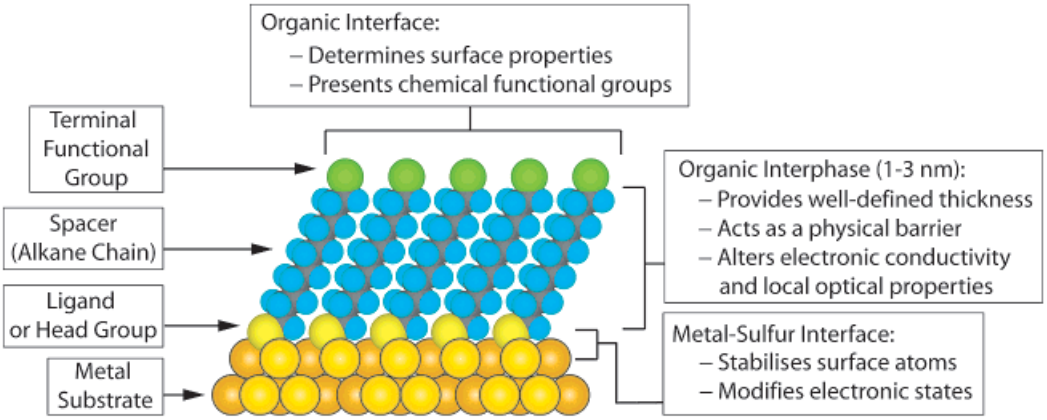


Figure 3.9: Self-assembled monolayer of alkanethiolates on a gold surface with a (111) texture [10].

An extensively studied class of SAMs is derived from the adsorption of alkanethiols, which are the most commonly used self-assembling molecules with an alkyl chain, $(C\text{-}C)^n$ chain, as the back bone, a tail group, and a S-H head group, on gold, silver, copper (Figure 3.9). Surfaces of metals and metal oxides tend to adsorb adventitious organic materials readily because these adsorbates lower the free energy of the interface between the metal or metal oxide and the ambient environment [10].

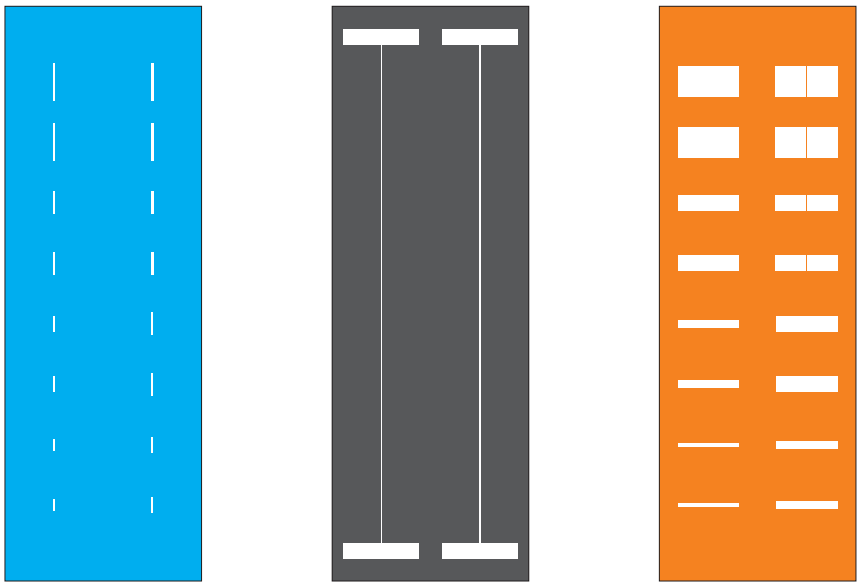
3.3 Experimental Details

3.3.1 Thermal Evaporation

In this work, pentacene was deposited by thermal evaporation at room temperature through a shadow mask (Figure 3.10(a)) using an Edwards Auto306 evaporator. An Edwards RV12 rotary pump was used for roughing the chamber down to $\sim 10^{-2}$ mbar and an Edwards EXT255H compound molecular pump was used to reach a pressure of less than 1×10^{-6} mbar. Pentacene was deposited from a ceramic, resistively-heated crucible at a temperature of around 150 °C. The pentacene layer with thickness 30-50 nm was evaporated at a rate of around 0.02∼0.05 nm s^{-1}. The film thickness and deposition rate were monitored by a quartz crystal microbalance

Table 3.1: Channel dimensions of shadow mask.

Channel length [µm]	Channel width [µm]	W/L	Channel length [µm]	Channel width [µm]	W/L
50	4000	80	200	4000	20
50	4000	80	200	4000	20
50	2000	40	200	2000	10
50	2000	40	200	2000	10
50	1000	20	100	2000	20
50	1000	20	100	2000	20
50	500	10	100	1000	10
50	500	10	100	1000	10



(a) (b) (c)

Figure 3.10: Shadow masks for (a) semiconductor layers, (b) gate contacts and (c) source/drain contacts.

connected to an Edwards film thickness monitor (FTM7) during evaporation.

Metal electrodes were deposited using an Edwards 306 thermal evaporator, through a shadow mask, at a pressure of less than 1×10^{-5} mbar. A high vacuum was achieved using an Edwards RV12 rotary pump and an Edwards E04K diffusion pump. The film thickness and deposition rate were monitored by a quartz crystal microbalance connected to an Edwards film thickness monitor (FTM7) during evaporation. An aluminium gate was defined with thickness 30-50 nm through a shadow mask (Fig-

ure 3.10(b)) for the gate contact. For source/drain contacts, 30-50 nm of gold was deposited through a shadow mask (Figure 3.10(c)). This resulted in contacts with a number of different channel dimensions as listed in Table 3.1. The overlap lengths between gate contact and source and drain contacts were designed as 25 μm for both. In top-gate, bottom-contact configuration, an additional 10 nm chromium layer was deposited under the gold film to promote good adhesion to the substrate.

3.3.2 Spin-Coating

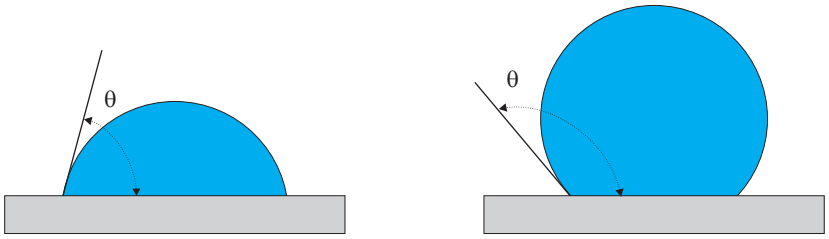
The thickness of a spun film is dependent on the viscosity coefficient and the concentration of the solution, the angular velocity of the spinning and the spinning time. The solution was dropped on the substrate before spinning and spin-coated using a Laurell Technologies WS-400A-6NPP-LITE spin-coater. Initially, a low spin speed (500 rpm) was used to spread the solution evenly on the substrate for a few seconds and afterwards, the film thickness was reduced to the desired thickness with a high spin speed (1000 - 5000 rpm) for several tens of seconds. Finally, the substrate was baked on a hot plate to cure the spun film.

In this study, 6,13-bis(triisopropyl-silylethynyl) (TIPS) pentacene and poly(methyl methacrylate) (PMMA) gate dielectric layers were deposited by spin-coating. In the case of TIPS pentacene, the angular velocity of the spinning influences the crystalline grain size, where low spin speeds (1000 rpm) result in larger grains [11]. The initial spin speed was 500 rpm for 10 seconds for solution dispersal followed by a spin at 1000 rpm for 110 seconds to get larger grains. The drying conditions for TIPS pentacene was room temperature for 1 hour. To form the gate dielectric, the substrate was initially spun at 500 rpm for 10 seconds, followed by a spin at 3000 rpm for 50 seconds to reduce the PMMA to the thickness of 150 nm. The substrate was then baked at 120 °C on a hot plate for 30-60 minutes to cure the PMMA. Concentrations of the spin-coated solutions are given in the relevant chapters.

3.3.3 Surface Treatments

Surface treatments were used for the preparation of surfaces with hydrophilic or hydrophobic properties. When a liquid droplet strikes a substrate, the edge of

the drop can be characterised as hydrophilic (wetting) or hydrophobic (dewetting) by a certain contact angle θ, as shown in Figure 3.11 [13]. For example, clean and untreated glass reveals hydrophilic properties because of unterminated OH groups on the glass surface which are ready to attach to water molecules through hydrogen bonding. This causes the water to wet the glass surface as shown in Figure 3.11(a).



(a) (b)

Figure 3.11: (a) Wetting of hydrophilic substrate surface with contact angle $\theta < \pi/2$ and (b) dewetting of a hydrophobic surface with $\theta > \pi/2$.

Silanisation of glass slides and silicon wafers with dimethyldichlorosilane (DMDCS) was used to produce hydrophobic properties on solid surfaces. Figure 3.12 shows how the surface of the glass slide is modified with the DMDCS. The samples were treated by immersion in a 2 % solution of DMDCS in 1,1,1-trichloroethane for a period of 5 minutes and carefully rinsed with isopropanol to remove any excess DMDCS. A monolayer of closely packed CH_3 groups was formed on the surface as a result of silanisation and this resulted in hydrophobic properties of the surface.

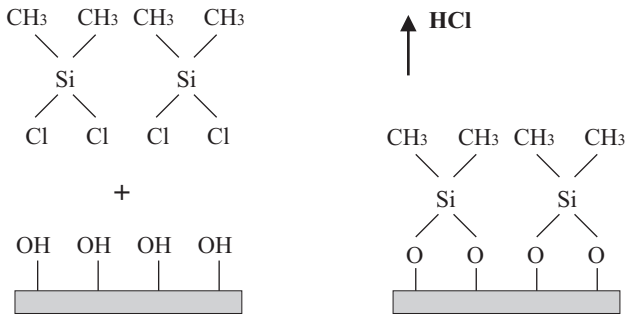


Figure 3.12: Hydrophobic treatment of a glass surface with dimethyldichlorosilane [14].

3.4 Device Characterisation

3.4.1 Physical Characterisation

Ellipsometry

Ellipsometry is based on measurements of the changes in light polarisation upon reflection from a sample surface. A basic ellipsometer configuration is shown in Figure 3.13. The method enables the measurement of the thickness and optical constants (refractive index) of the film. In this thesis, a Rudolph Research AutoEL-IV ellipsometer was used to measure the film thicknesses of silicon dioxide on silicon wafers. A monochromatic light source was generated from a white light source and a wavelength of 633 nm was used.

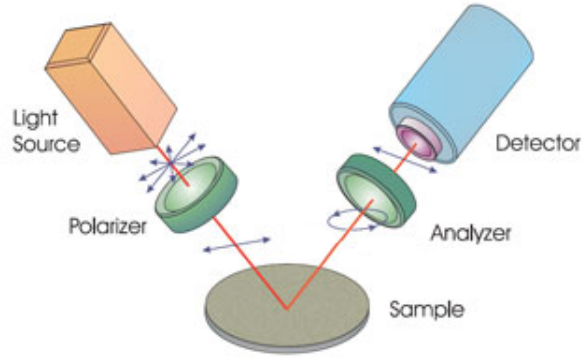


Figure 3.13: The basic configuration of the ellipsometer [15].

Atomic Force Microscopy

AFM is a high-resolution type of scanning probe microscopy for nano-meter scale science and technology. Two fundamental components of AFM are the probe and the scanner [16]. The probe used in an AFM is a sharp tip which is located at the end of a cantilever. Forces between the tip and the sample surface cause the cantilever to bend, or deflect according to Hooke's law. The force, F, will be given by

$$F = -kd \tag{3.5}$$

where d is the cantilever's displacement and k is the force constant. A light beam from a laser diode is reflected from the cantilever and incident on a position-sensitive photo-detector (PSPD). As a result, the PSPD measures the cantilever movements as the tip is scanned over the sample surface. This can generate a map of surface topography. A schematic diagram of a typical optical detection scheme for an AFM is shown in Figure 3.14.

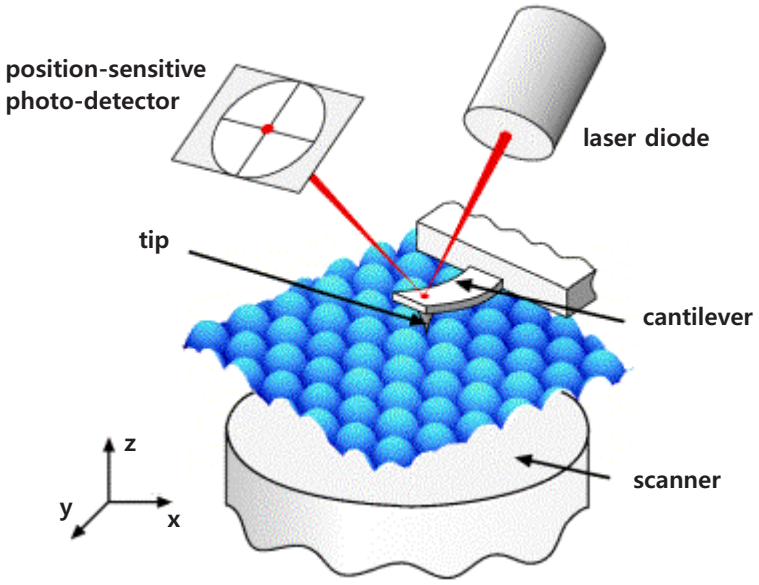


Figure 3.14: Typical optical detection scheme in atomic force microscopy [17].

There are three primary modes of use of an AFM: contact, tapping and non-contact mode [18]. In contact mode AFM, the tip contacts the sample surface during scanning. A feedback loop maintains a constant deflection between the cantilever and the sample by vertically moving the scanner and thus the force between the tip and the sample remains constant. For tapping mode AFM, the cantilever is oscillated at or slightly below its resonant frequency with an amplitude ranging typically from 20 nm to 100 nm. The tip lightly taps on the sample surface during scanning, contacting the surface at the bottom of its swing. A feedback loop maintains a constant oscillation amplitude by maintaining a constant RMS of the oscillation signal and thus a constant tip-sample interaction is maintained during scanning. On the other hand, for non-contact mode AFM, the cantilever is oscillated at a frequency which is slightly above the cantilevers resonant frequency, typically with

an amplitude of a few nanometers (< 10 nm). The tip does not contact the sample surface, but oscillates above the sample surface during scanning.

The thicknesses and morphologies of the various layers were studied using a Digital Instruments Nanoscope IV AFM. Most of the results reported in this work were measured in tapping mode using an 1 Ω cm silicon cantilever (Veeco OTESPA).

3.4.2 Electrical Characterisation

Capacitance-Voltage Characteristics

The Capacitance-Voltage *C*-*V* measurement involves the application of a small AC signal on top of a preselected DC voltage while detecting the AC current flowing through the metal-insulator-semiconductor (MIS) structure. The AC signal is typically 15 mV RMS and common signal frequencies from about 10 kHz to 10 MHz are used [19, 20]. The bias is applied as a DC voltage sweep that drives the MIS structure with classical inorganic semiconductor from its accumulation, through the depletion and into the inversion region. However, the situation is different in an organic-based device.

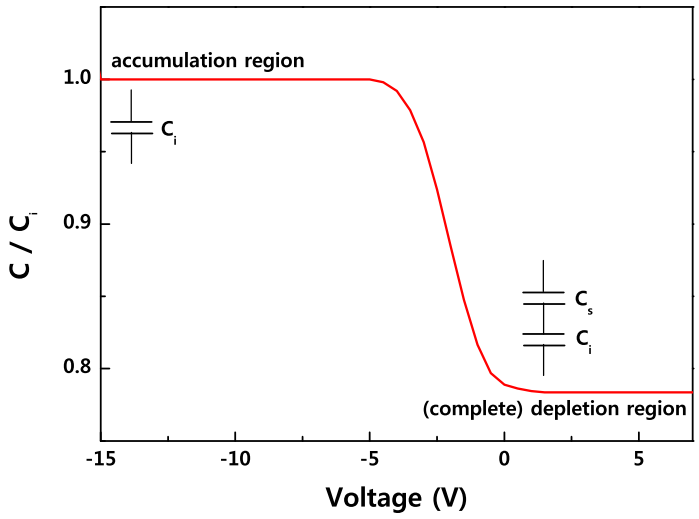


Figure 3.15: Capacitance versus voltage behaviour for an typical MIS structure based on a p-type organic semiconductor.

For a MIS capacitor based on p-type organic semiconductor, a positive DC bias causes majority carriers in the semiconductor to be repelled from the insulator interface and the capacitance falls as the depletion region expands as shown in Figure 3.15. Finally, the capacitance is at a minimum when the semiconductor is completely depleted (complete depletion region) and is determined by the series sum of the insulator and semiconductor capacitances. As the bias voltage moves toward negative values, majority carriers in the semiconductor are attracted toward the insulator interface and the capacitance reaches a maximum value (accumulation region).

The *C-V* behaviour was monitored with an HP4192A impedance analyser. The capacitance can be calculated from

$$C = \frac{I}{2\pi f V_{AC}} \tag{3.6}$$

where I is the magnitude of the AC current, f is the test frequency and V_{AC} is the magnitude and phase angle of the measured AC voltage [20]. The measurements were performed at 1 kHz or 1 MHz with a 50 mV RMS AC signal and at a voltage scan rate of 1 V s^{-1} for PMMA/pentacene samples and 0.05 V s^{-1} for cross-linked PMMA/pentacene samples. In each measurement, the scan was started from a positive gate voltage and swept toward accumulation.

Current-Voltage Characteristics

The OTFT current, *I*, versus voltage, *V*, characteristics were measured in an electrically screened chamber under ambient conditions using a HP 4140B pA meter/DC voltage source. Gold ball probes were used for connections to the sample. To measure the output characteristics of the OTFTs, a DC voltage was applied to the gate while the value of the drain-source voltage (V_{DS}) was swept in forward and reverse directions. During this time, the drain current (I_{DS}) was measured. This loop was performed several times with different gate voltages. To measure the transfer characteristics of OTFTs, a DC voltage was applied to the drain and the drain current was measured at each point of a defined gate voltage sweep for both forward and reverse directions. The *I-V* measurements for both output and transfer

characteristics of OTFTs were made using three probes.

In order to measure the leakage current density, the bias voltage were supplied by a Keithley 2400 source using a linear staircase step with a 1 second delay between measurements and the currents were measured using a Keithley 485 digital picoammeter in an electrically screened chamber. Two probes were used for the measurement of the leakage current density.

3.5 Materials

3.5.1 Pentacene

Pentacene ($C_{22}H_{14}$) is one of the most widely studied organic semiconductors, with investigations beginning in the 1970s. Pentacene is a planar molecule composed of five linearly fused benzene rings. These molecules are arranged in a herringbone pattern due to the large asymmetry of the molecule to form the bulk triclinic crystal. In evaporated films, pentacene deposits with its long axis roughly perpendicular to the substrate, resulting in strong two-dimensional interactions parallel to the substrate [21]. The parameters of the crystal structure of pentacene are listed in Table 3.2.

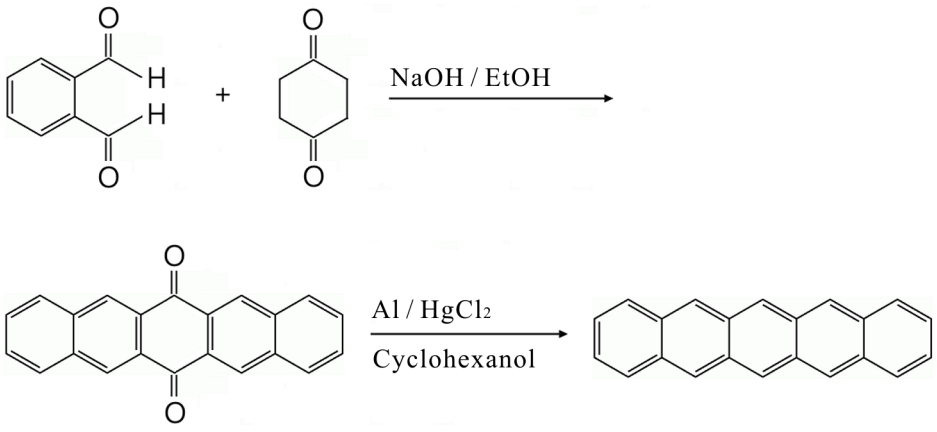


Figure 3.16: The principal synthesis of pentacene from 6,13-pentacenequinone.

Pentacene is most conveniently synthesised from 6,13-pentacenequinone, which

Table 3.2: Crystallographic data for pentacene [22, 23].

Parameter	Unit	Value
Crystal system	-	Triclinic
a	Å	7.90
b	Å	6.06
c	Å	16.01
α	°	101.9
β	°	112.6
γ	°	85.8
U (volume of unit cell)	Å ^{3}	692
Z (molecules per unit cell)	-	2
D (density)	g cm^{-3}	1.32
Space group	-	P1
Molecular weight	-	278.3

is itself easily prepared by fourfold aldol condensation between phthalaldehyde and 1,4-cyclohexanedione [24]. Pentacene is then formed from 6,13-pentacenequinone by a simple reduction reaction as shown in Figure 3.16.

In this study, pentacene (obtained from Sigma-Aldrich) was used without further purification as the semiconductor in OTFTs.

3.5.2 6,13-bis(triisopropylsilylethynyl) Pentacene

Bulky triisopropylsilylethynyl groups have been substituted at the 6,13-positions of the pentacene molecule in order to impart solubility [21]. In addition, the functionalised groups in TIPS pentacene help to disrupt the herringbone packing of the pentacene core and to interact in a face-to-face (π-stacking) orientation; this interaction enhances π-orbital overlap and potentially increases charge carrier mobility [25]. Figure 3.17 shows the chemical structure of TIPS pentacene. It is not necessary to remove the functionalised groups for TIPS pentacene after deposition because these have been substituted permanently in the pentacene molecule without destruction of the semiconducting properties of the material.

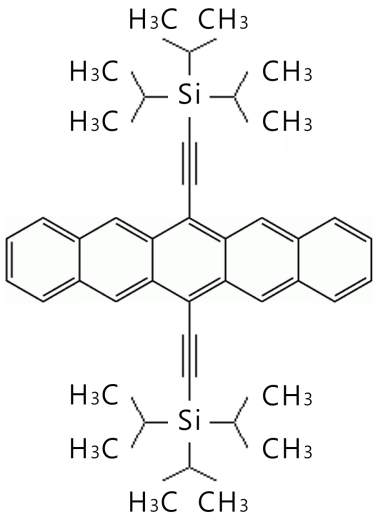


Figure 3.17: The chemical structure of 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene.

TIPS pentacene is easily prepared in a one-pot reaction from pentacenequinone [26, 27]. Pentacenequinone is added to a solution of the alkynyl Grignard reagent in tetrahydrofuran (THF) and stirred at 60 °C until it dissolves. To this solution is then carefully added a solution of 10% hydrogen chloride (HCl) that has been saturated with stannous chloride; the deep blue pentacene is formed immediately. The resulting TIPS pentacene shows high solubility (> 100 mg mL^{-1} in many organic solvents) and better stability than unfuctionalised pentacene.

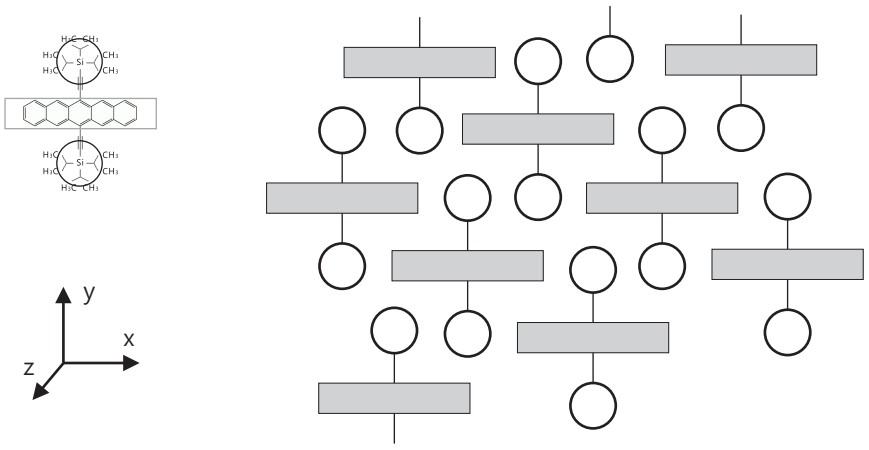


Figure 3.18: The arrangement of molecules in TIPS pentacene. View normal to plane of aromatic rings.

The unique arrangement of molecules in the TIPS pentacene crystal after deposition means that the resistivity varies according to the direction of the crystal (Figure 3.18) [26,27]. The y axis, perpendicular to the plane of the pentacene rings, has the lowest resistivity of 2.5×10^{6} Ω cm, then the x axis, parallel to the long axis of the molecules, of 5×10^{8} Ω cm. The z axis has the highest resistivity of 3×10^{10} Ω cm due to the insulating effects of the substituted side groups. However, these values are significantly lower compared to pentacene crystals (10^{12} Ω cm).

In this study, TIPS pentacene (obtained from Flexink) was used without further purification as the semiconductor in OTFTs.

3.5.3 Poly(methyl methacrylate)

PMMA is one of the most common plastic materials in electronics. PMMA was one of the first materials developed for e-beam lithography. It is the standard positive e-beam resist and still remains one of the highest resolution resists available today.

The PMMA monomer, methyl methacrylate (MMA), is made by heating acetone cyanohydrin (from the addition of hydrocyanic acid to acetone) with sulphuric acid to form methacrylamide sulfate. The latter is reacted (without separation) with water and methanol to give methyl methacrylate as shown in Figure 3.19 [28]:

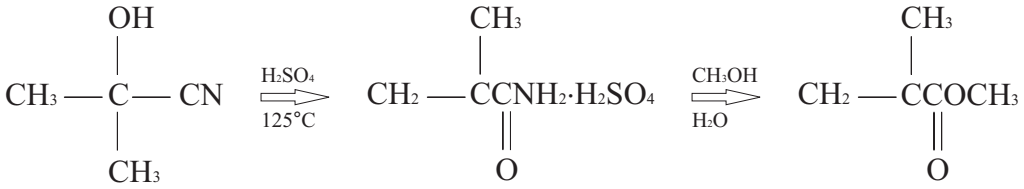


Figure 3.19: The principal synthesis for methyl methacrylate.

PMMA is the synthetic polymer of MMA. MMA, in bulk liquid form or suspended as fine droplets in water, is polymerised (its molecules linked together in large numbers) under the influence of free-radical initiators to form solid PMMA. The molecular structure of PMMA is shown in Figure 3.20. In this study, PMMA (M_w = 93,000, obtained from Sigma-Aldrich) is used for the gate dielectric layer in OTFTs.

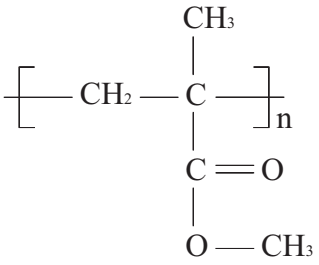


Figure 3.20: Molecular structure of poly(methyl methacrylate).

3.6 Conclusions

In this chapter, an overview of the experimental techniques used in this work has been presented. A basic description of thin film processes and the experimental details has been explained. In particular, three different techniques for the preparation of thin films have been discussed: thermal evaporation, spin-coating and surface treatments. Following this, device characterisation methods have been described. For physical characterisation, ellipsometry and AFM have been introduced for the measurement of thin film thicknesses and the study of surface morphologies. Capacitance-voltage and current-voltage measurement methods have been outlined for the electrical characterisation. Finally, a brief overview of the materials used in this study has been given.

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Chapter 4

Pentacene Thin-Film Transistors with Poly(methyl methacrylate) Gate Dielectrics

4.1 Introduction

A range of different organic materials have been investigated for use as the gate dielectric in organic thin-film transistors (OTFTs). These include poly(vinyl alcohol) (PVA), poly(vinyl phenol) (PVP) and polystyrene (PS) [1]. Hybrid organic/inorganic insulators have also been used [2]. The high resistivity ($> 2\times10^{15}$ Ω cm) and low dielectric constant (approximately 3, similar to that of silicon dioxide) of poly(methyl methacrylate) (PMMA) make it a potential candidate as the dielectric layer in OTFTs [3, 4]. Furthermore, this polymer contains hydrophobic methyl radical groups, which can play a role as moisture inhibitors, as well as encouraging good ordering of the active organic overlayer as it is deposited on the surface [5]. To date, pentacene-based OTFT devices using PMMA as the gate dielectric have shown low field-effect-mobilities (generally less than 0.1 cm^2 V^{-1} s^{-1}) due to the relatively thick film of PMMA used, low on/off current ratios (10^3) resulting from large leakage currents, and high threshold voltages (-15 to -25 V) [6–9]. However, one encouraging result is that of Huang et al. [10], who have reported a mobility of 0.24 cm^2 V^{-1} s^{-1} using a 300 nm thick PMMA layer.

In this chapter, spin-coating has been used to produce high quality thin layers of PMMA. These have been incorporated into pentacene OTFTs and the electrical characteristics studied as a function of the dielectric thickness. It is shown that leakage currents can be reduced significantly by pattering the active layer, leading to a good on/off current ratio. The influence of scaling of the channel length and

width on the transistor characteristics is reported. Finally, a diode-connected load inverter and bootstrapped inverter incorporating pentacene OTFTs with PMMA as the gate dielectric have been designed, fabricated and tested.

4.2 Experiment

In this work, bottom-gate, top-contact OTFTs were fabricated using the structure shown schematically in Figure 4.1.

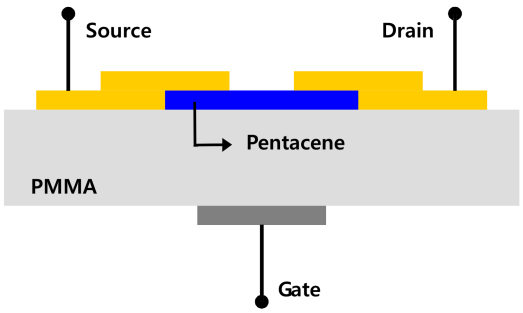


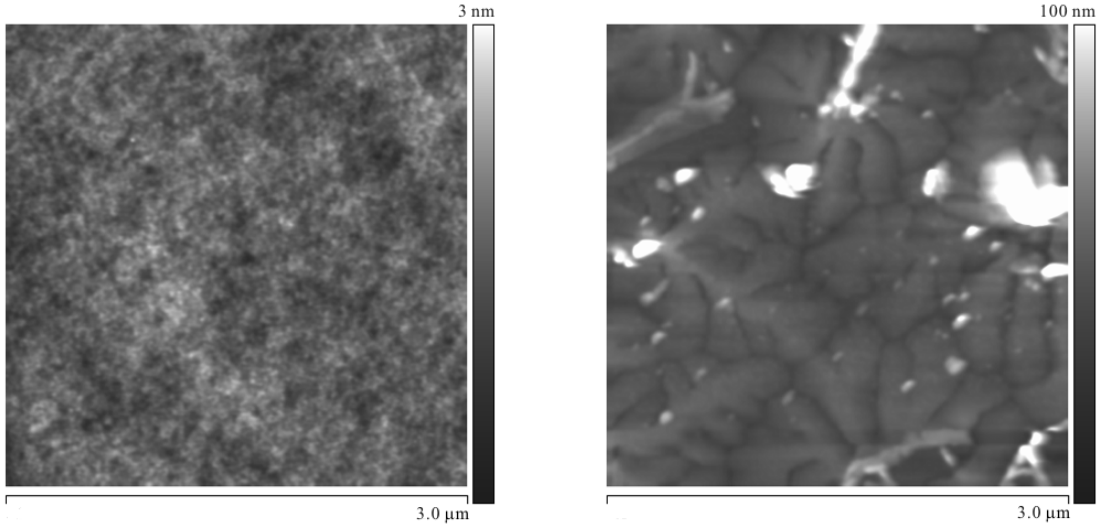
Figure 4.1: A schematic cross-section of a pentacene-based OTFT with a PMMA gate dielectric.

Device fabrication was undertaken in a Class 1,000 Clean Room. Glass slides were used as substrates onto which an aluminium gate, thickness 30 nm, was defined by thermal evaporation through a shadow mask. An anisole (methoxybenzene - obtained from MicroChem) solution of PMMA (M_w = 93,000, obtained from Sigma-Aldrich) was spin-coated on top and cured for 1 hour at 120 °C. The thickness of the PMMA film was varied from 100 nm to 2000 nm by changing the solution concentration and spin-coating speed. Following this, pentacene (Sigma-Aldrich and used without further purification) was thermally evaporated, at room temperature, to a thickness of 30 nm. To explore the effects of patterning the active layer, the pentacene was deposited with and without the use of a shadow mask. The deposition rate was 0.05 nm s^{-1} at a chamber pressure of approximately 1×10^{-6} mbar. A further shadow mask was used to define the source and drain contacts, formed by the thermal evaporation of 30 nm of gold.

4.3 Poly(methyl methacrylate) Gate Dielectrics

4.3.1 Surface Morphology

Uniform, pinhole-free and crack-free films of PMMA could be obtained by spin-coating with a lower limit to the thickness of about 150 nm. Tapping mode atomic force microscope (AFM) images of the surface of a 150 nm PMMA film and of a 30 nm pentacene film, which was subsequently evaporated onto the PMMA, are shown in Figure 4.2.



(a) (b)

Figure 4.2: Atomic force microscope images of (a) 150 nm thick PMMA film spin-coated onto a glass slide and (b) 30 nm thick pentacene film thermally evaporated on top of the PMMA.

A relatively smooth surface is evident for the PMMA (Figure 4.2(a)). The root mean square (RMS) roughness was 0.30 nm; this can be contrasted with figures of 0.45∼0.76 nm reported by Shin et al. [11] for a 140∼160 nm thick PMMA layer. The grain size for the pentacene was greater than 1 µm (Figure 4.2(b)), with an RMS roughness of 13 nm. These figures are similar to those reported by Huang et al. [10] for pentacene evaporated onto PMMA: grain size 1.0∼1.5 µm and RMS roughness 11 nm.

4.3.2 Electrical Characteristics

A parallel plate capacitor structure (Al/insulator/Au) was fabricated to investigate the dielectric properties of the PMMA. The area of the top Au electrode was 2.25×10^{-2} cm^2. Figure 4.3 shows the current density, J, versus the electric field, F, for a 150 nm thick PMMA film. These data were similar for either polarity of voltage applied to the top electrode. The leakage current density is less than 10^{-8} A cm^{-2} for fields up to 0.4 MV cm^{-1} and this remained below 10^{-6} A cm^{-2} for fields up to 2 MV cm^{-1}. Such current densities are sufficiently small to allow the use of the 150 nm PMMA film as the gate dielectric in an OTFT.

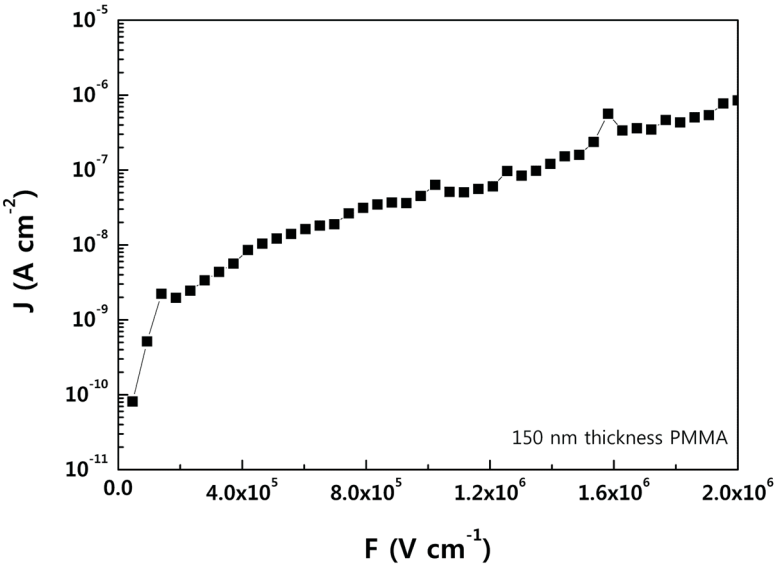


Figure 4.3: Current density versus applied electric field for an Al/PMMA/Au structure. The PMMA thickness = 150 nm.

Physical processes that might account for the current versus voltage behaviour in the presence of high electric fields are Schottky emission and the Poole-Frenkel effect [12, 13]. The former process occurs at the interface between the electrode(s) and the dielectric and has a current, I, versus voltage, V, dependence of the form

$$I \propto T^2 \exp\left(\frac{\beta_{SC} V^{1/2} - \Phi_{SC}}{k_B T}\right) \tag{4.1}$$

where Φ_{SC} is the Schottky barrier height, β_{SC} is the Schottky coefficient, T is the temperature and k_B is the Boltzmann constant. Poole-Frenkel conductivity is a similar process to Schottky emission, but it results from the lowering of the potential barriers around impurity centres in the bulk of the insulator. The I-V relationship is given by

$$I \propto V \exp\left(\frac{\beta_{PF} V^{1/2} - \Phi_{PF}}{k_B T}\right) \tag{4.2}$$

where Φ_{PF} is the potential barrier height and β_{PF} is the Poole-Frenkel coefficient.

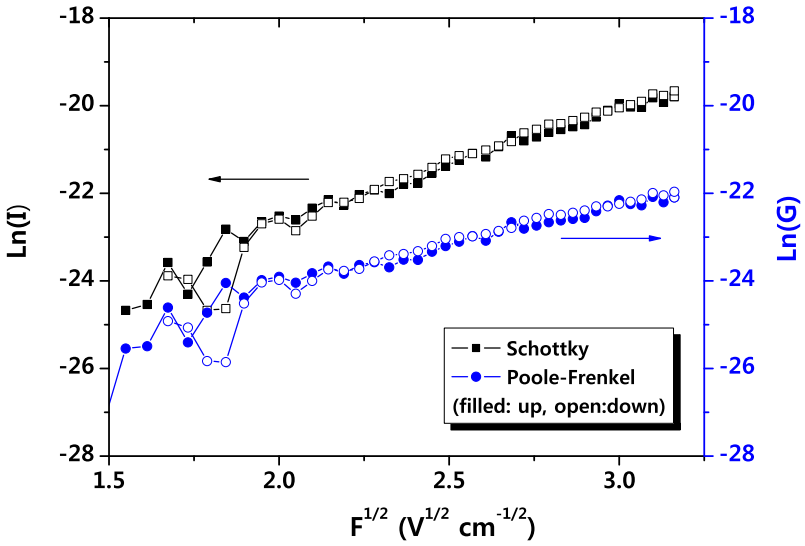


Figure 4.4: Schottky ($\ln(I)$ versus $F^{1/2}$) and Poole-Frenkel ($\ln(I/V)$ versus $F^{1/2}$) plots for an Al/PMMA/Au structure. The PMMA film thickness = 150 nm.

Figure 4.4 shows the conductivity data obtained for the 150 nm PMMA film plotted in the form of the Schottky ($\ln(I)$ versus $V^{1/2}$) and Poole-Frenkel ($\ln(I/V)$ versus $V^{1/2}$) equations. Data are shown for both increasing and decreasing applied voltages. In each case, the fit to theory is very good. However, I-V plots seems to be independent on the polarity of the applied voltage. This suggests that the dominant conduction mechanism with PMMA as the gate insulator is Poole-Frenkel type. Schottky β_{SC} and Poole-Frenkel β_{PF} field lowering coefficients are given by

$$2\beta_{SC} = \beta_{PF} = \left(\frac{e^3}{\pi\epsilon_0\epsilon_r}\right)^{1/2} \tag{4.3}$$

ϵ_0 and ϵ_r are the permittivity of free space and the relative permittivity of the insulator, respectively. If the relative permittivity is considered to be 3.66, then the theoretical values of these coefficients are β_{SC} = 1.98×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ and β_{PF} = 3.97×10^{-5} eV m$^{1/2}$ V$^{-1/2}$. The experimental value of β, which can be extracted from the plot in Figure 4.4, is 4.88×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ (corresponding to ϵ_r = 2.41) for the Schottky plot and 1.67×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ (ϵ_r = 20.64) for the Poole-Frenkel plot, respectively. This suggests that the dominant conduction mechanism in the PMMA may be Schottky emission, even though I-V plots seems to be independent on the polarity of the applied voltage. Tunnelling could equally contribute to the electronic transport. As a result, a definite conclusion cannot be drawn from the conductivity data only to identify the processes responsible for the current transport in the PMMA at high electric fields. Therefore, further work, such as insulator thickness and temperature dependence measurements, is clearly needed to ascertain the electrical conduction processes in the PMMA.

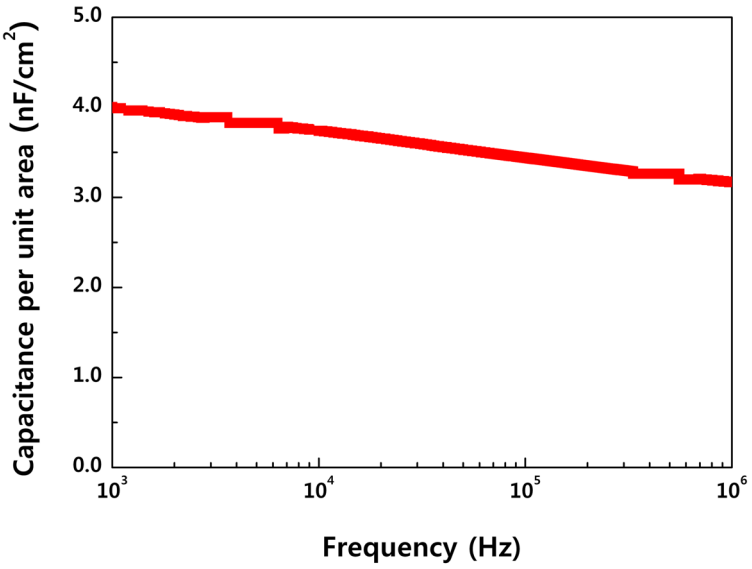


Figure 4.5: Capacitance versus frequency characteristics of a spin coated PMMA layer; thickness = 810 nm.

Figure 4.5 shows the measured capacitance per unit area as a function of frequency for a 810 nm thick PMMA layer sandwiched between Au and Al electrodes. The dielectric constant of the PMMA decreases over the frequency range of the measurements and was calculated to be 3.66 ± 0.10 at 1 kHz and 2.89 ± 0.10 at 1 MHz. These values agree well with other literature reports [4, 6, 9, 14].

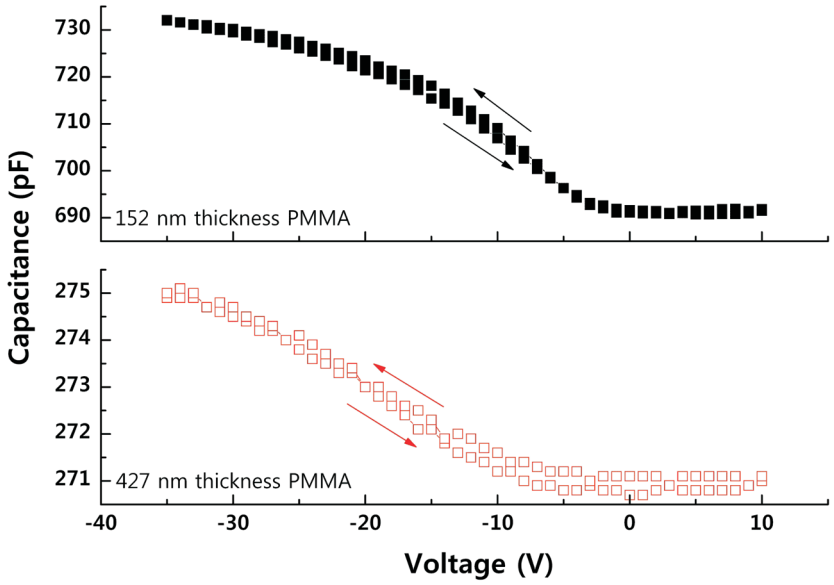


Figure 4.6: Capacitance versus voltage characteristics, measured at 1 MHz and a voltage scan rate of 1 V s^{-1} for Al/PMMA/pentacene/Au structure for two different thicknesses of PMMA. Pentacene thickness = 30 nm.

The C versus V characteristics, measured at a frequency of 1 MHz and a voltage scan rate of 1 V s^{-1}, of two Al/PMMA/pentacene/Au metal-insulator-semiconductor (MIS) structures are shown in Figure 4.6. The area of the top Au electrode was 4.4×10^{-2} cm^2. The C-V data for both samples (PMMA thickness 150 nm and 430 nm) reveal the accumulation (large negative voltage applied to Al) and depletion behaviour that is typical for MIS devices based on a p-type semiconductor with a large negative flatband voltage. The constant capacitance at large positive voltages is probably related to the depletion layer extending across the entire film thickness. A small amount of hysteresis is evident on reversing the direction of the voltage scans. The anti-clockwise direction of this hysteresis may be related to the charging and discharging of interface traps located at, or close to, the PMMA/pentacene in-

terface [15]. The accumulation capacitance values for the two MIS structures scale with the PMMA thickness and the calculated dielectric constant (2.86 ± 0.10 for 152 nm and 3.02 ± 0.10 for 427 nm thickness PMMA at 1 MHz) is consistent, within experimental errors, with the value calculated from the Au/PMMA/Al structure (Figure 4.5). Assuming a fully depleted semiconductor film, the relative permittivity of pentacene was calculated to be 9.69 ($C_{pentacene}$ = 12.59 nF) for 152 nm thickness PMMA and 11.43 ($C_{pentacene}$ = 14.85 nF) for 427 nm thickness PMMA at 1 MHz from the minimum capacitance value in Figure 4.6. These values are higher than those generally reported for pentacene (3∼6) [16, 17]. It is possible that the measured capacitance may not equal the depletion layer capacitance because of a high measurement frequency [18]. Alternatively, there could be errors in the measured semiconductor film thickness. The doping density for the pentacene can be estimated from the slope in the linear region of the *C*-*V* data, using the following relationship [19].

$$N_D = \frac{-2\Delta V}{q\epsilon_0\epsilon_s A^2(\Delta(1/C^2)} \tag{4.4}$$

where N_D is the doping density, A is the effective area and ϵ_0 and ϵ_s are the permittivity of free space and the relative permittivity of the semiconductor, respectively. The doping density for the pentacene was calculated to be 6.27×10^{17} cm^{-3} for 152 nm thickness PMMA and 4.47×10^{17} cm^{-3} for 427 nm thickness PMMA. These values are in good agreement with reported results [20, 21].

4.3.3 Thickness and Field-effect Mobility

Figure 4.7 shows the thickness of PMMA as a function of spinning speed and solution concentration. Above 15 wt% polymer, the film thickness was inversely proportional to the spinning speed. For lower PMMA concentrations, the solution concentration was much more effective than spinning speed for controlling the thickness of the polymer. In this study, 14.3 wt% (810 nm), 9.1 wt% (427 nm), and 4.8 wt% (152 nm) solutions of PMMA, spin-coated at 3000 rpm, were used to investigate the dependence of the electrical behaviour of the transistors on the PMMA

thickness.

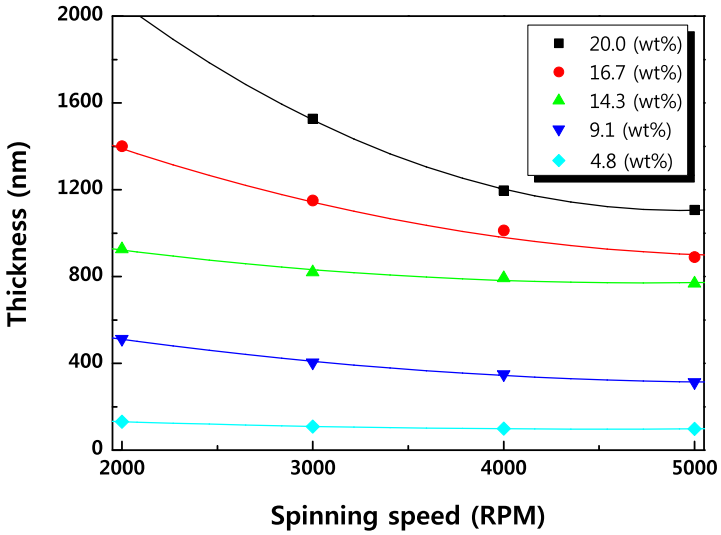
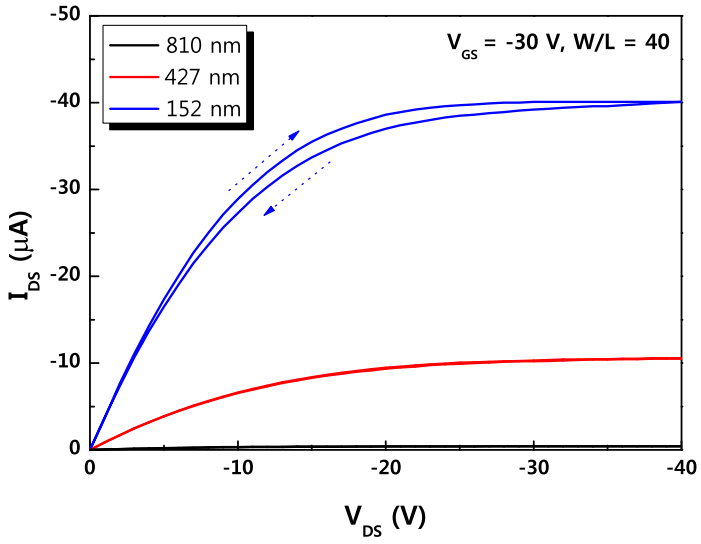
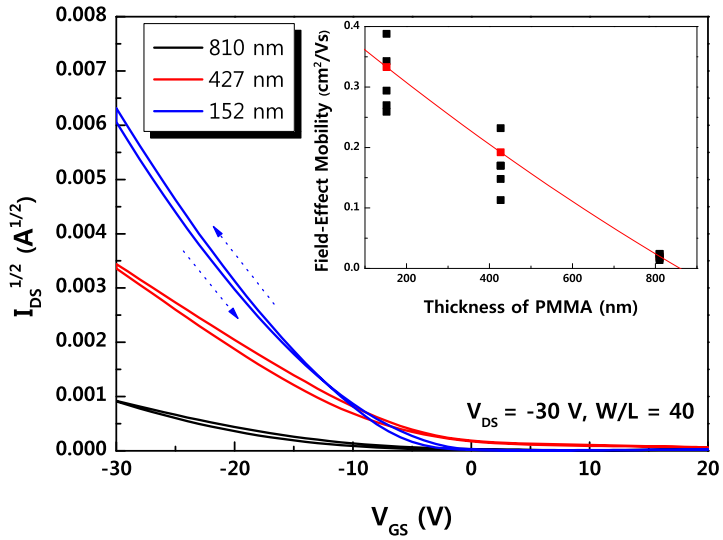


Figure 4.7: Thickness of spin-coated PMMA films as a function of spinning speed and solution concentration.

Figure 4.8 shows (a) the dependence of the drain-source current, $(I_{DS})^{1/2}$, on the drain-source voltage, V_{DS} (the OTFT output characteristics), and (b) the dependence of I_{DS} on the gate-source voltage, V_{GS} (the transfer characteristics), for devices with different thicknesses of PMMA; forward and reverse voltage scans are shown. The gate-source voltage was -30 V for the output characteristics and the drain-source voltage was -30 V for the transfer characteristics. The channel width, W, to length, L, ratio was 40 (channel length = 50 μm, width = 2000 μm). These data agree with simple thin film transistor theory [1]. As the gate dielectric thickness is reduced, C_i will increase, accounting for the larger drain to source currents evident in Figure 4.8. The inset to Figure 4.8(b) shows the variation of the field effect mobility (μ_{sat}) with dielectric thickness for a number of different devices. A clear trend showing an increase in μ_{sat} with the decrease in thickness of the gate dielectric is evident; averaged data reveal that μ_{sat} increased by about 13 times for a five-fold reduction in the PMMA thickness. This effect has been reported previously for pentacene OTFTs (see, for example [22]) and there are now a number of different



(a)



(b)

Figure 4.8: (a) Output and (b) transfer characteristics for pentacene based OTFTs having PMMA gate dielectrics with different thickness. Inset: field-effect mobility as a function of the thickness of PMMA.

explanations for the dependence of carrier mobility on gate insulator thickness. For example, the phenomenon might be due to a variation of the gate dielectric constant of the film with the concentration of the PMMA solution [23]. Veres et al. [3, 24]

have suggested that a higher dielectric constant induces a broadening of the density of states (DOS) at the polymer/insulator interface. This results in a decrease in the DOS at the Fermi energy and subsequently causes a lower hopping probability, leading to a suppression of the carrier mobility. This effect can occur for OTFTs based on both polymers and low molecular weight materials such as pentacene. More recent work suggests that a mobility dependence in pentacene transistors can result from the viscoelastic properties of the organic dielectric [25]. It is certainly possible that our very thin PMMA spin-coated layers possess different surface chain dynamics. Alternatively, the morphological properties of the thinner PMMA films may provide for improved growth of the thermally evaporated pentacene, resulting in larger grains and higher carrier mobilities. Another explanation can be the gate-voltage dependent field-effect mobility [26–28]. The number of accumulated carriers at the pentacene surface will depend on V_{GS}; an increase in V_{GS} will result in an increase in the number of surface carriers as discussed in section 2.4.6. The same effect will be obtained if V_{GS} is held constant and the gate dielectric thickness is reduced, due to an increase in the electric field in the dielectric. Hence, for the same gate-source voltage, there will be more surface carriers available to fill the traps for a thinner dielectric. Increasing the permittivity of the gate dielectric will produce similar results [22]. The thinnest PMMA layers used in this work were 150 nm, limited by the quality of the spin-coated film (devices with 32 nm cross-linked PMMA are shown later on, in Chapter 5).

The plot of ${I_{DS(sat)}}^{1/2}$ versus V_{GS} was used to determine the values of the threshold voltages for our OTFTs with different PMMA thicknesses. The trend was a decrease in V_T with a decrease in the thickness of the gate dielectric, from about -11 V for a 810 nm gate insulator to approximately -6 V for the OTFTs with PMMA thicknesses of 152 nm. However, there was much variability between the samples (a full table showing all the parameters for devices is shown later on, in section 4.4) and these figures represent average values for a number of devices. The theoretical dependence of V_T on the thin film transistor parameters is quite complex. Assuming that there is no work function difference between the gate metal and the semiconductor, the magnitude of V_T can be approximated by [29]

$$V_T = \mu_0 \left| \frac{Q_S}{C_i} \right| \tag{4.5}$$

where Q_S is the effective total charge per unit area at the dielectric/semiconductor interface at zero gate voltage. This charge (which may be positive or negative) will be made up from a number of contributions: mobile and fixed charge in the dielectric layer and interface state charge. The results reveal that the value of V_T decreases by a factor of approximately 3 for a five-fold decrease in the gate dielectric thickness. This suggests that Q_S also varies with the thickness of the PMMA.

4.4 Patterning the Organic Semiconductor

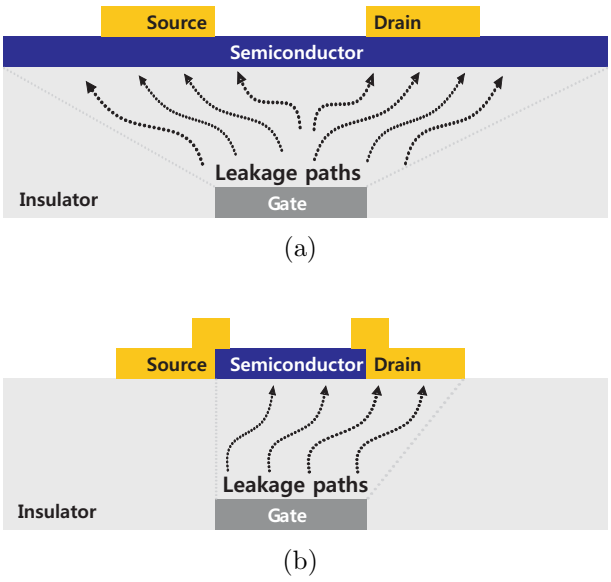
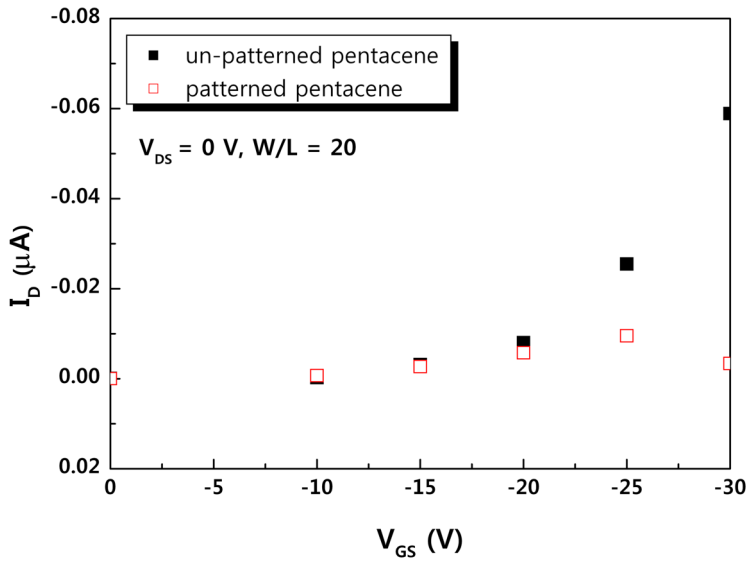


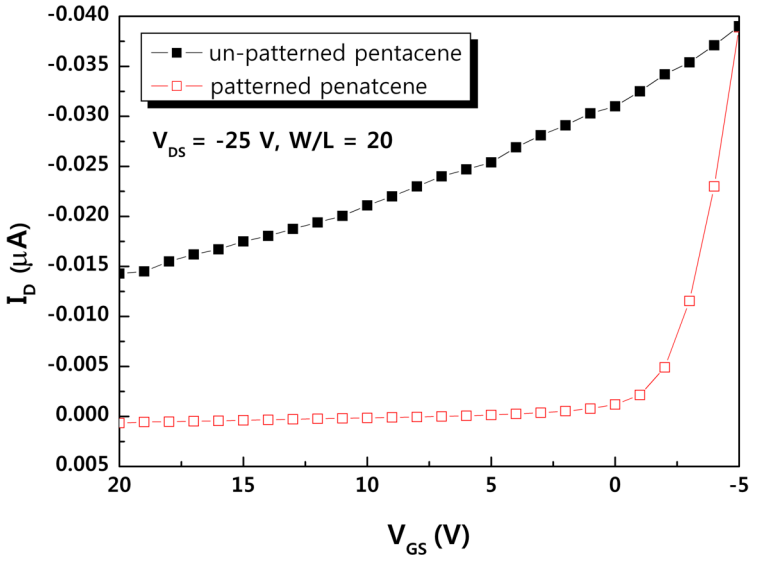
Figure 4.9: Possible leakage paths in (a) an un-patterned pentacene OTFT and (b) a patterned pentacene device.

A further problem with OTFTs using PMMA as the gate dielectric has been a low on/off current ratio. This can be related to the drain offset current, which is defined as the drain current at different gate biases when the drain-source bias is zero. For an ideal device, $I_D = 0$ A for $V_{DS} = 0$ V. The I_D offset is closely related to I_{DG} and is a convenient indicator of gate induced leakage in OTFTs. Jia et al. have reviewed the possible origins of I_D offset and concluded that the effect is related to the expansion of the source and drain electrodes by the semiconductor accumulation

layer [30]. The latter provides leakage paths and more current flows through the dielectric as a result of these, as shown in Figure 4.9(a). The leakage paths can be eliminated by patterning of the active layer, Figure 4.9(b).



(a)



(b)

Figure 4.10: (a) I_D offset (V_{DS} = 0 V) and (b) leakage current (V_{DS} = -25 V) in patterned and un-patterned pentacene OTFTs.

This was confirmed by Jia et al., who reported a substantial reduction in the

I_D offset following patterning of the organic semiconductor (poly 3-hexylthiophene) [30]. The effects of patterning the pentacene layer using shadow masks have been explored. Figure 4.10 compares the electrical behaviour of patterned and un-patterned pentacene OTFTs. Figure 4.10(a) depicts the drain current at different gate biases when the drain-source bias (V_{DS}) was zero. For the un-patterned OTFT, it is evident that the offset in the drain current increased with increasing gate voltage. Patterning markedly decreased this effect. The leakage through the bulk can also be seen in the transfer characteristics, Figure 4.10(b), for which V_{DS} = -25 V. There is a large leakage in the un-patterned device, but again, this effect is much reduced in the OTFT in which the pentacene film is confined to the region between the source and drain electrodes.

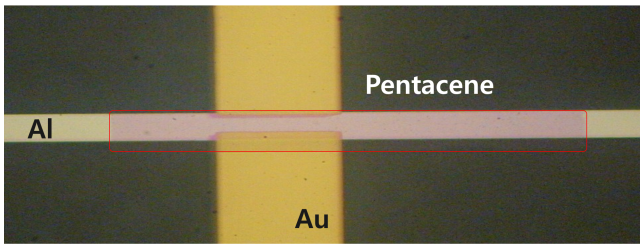


Figure 4.11: Optical micrograph of a patterned pentacene-based OTFT with PMMA gate dielectric. Channel length = 50 μm, channel width = 500 μm.

Figure 4.11 shows an optical micrograph of a patterned pentacene/PMMA device. The patterned pentacene is visible between the gold source and drain electrodes.

4.5 Channel Dimensions

Figure 4.12 shows the relationship between $I_{DS(sat)}$ and the width/length ratio W/L for a number of OTFTs with a fixed 50 μm channel length, and V_{GS} = -25 V; the PMMA thickness was 152 nm. The error bars reflect measurements on a number of different samples. The inset shows a typical set of output characteristics for these devices. Within experimental error, the saturated drain-source current varies linearly with W/L, as predicted by Equation 2.8.

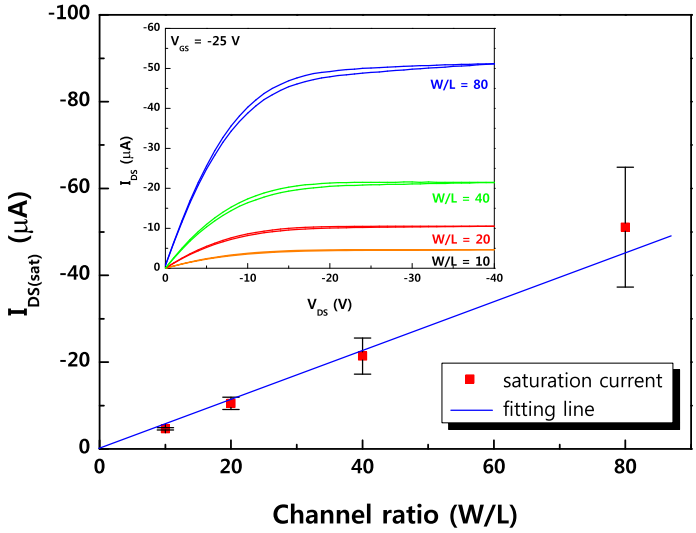


Figure 4.12: $I_{DS(sat)}$ versus channel width/length ratio W/L for pentacene OTFTs. The output characteristics are shown inset. V_{GS} = -25 V. PMMA thickness = 152 nm.

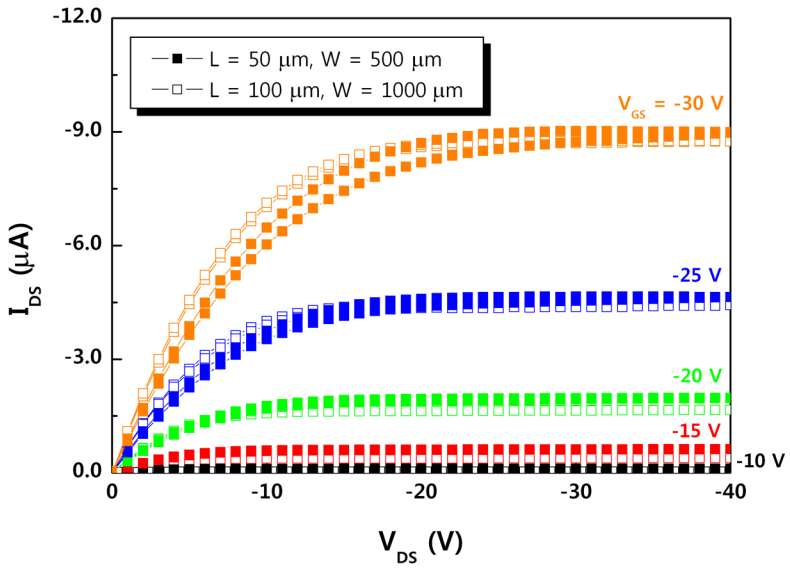


Figure 4.13: Output characteristics for OTFTs with the same channel width/length ratio but different channel lengths and widths. PMMA thickness = 152 nm.

The effects of keeping the same channel width to length ratio ($W/L = 10$), but using different absolute values, are shown in Figure 4.13: the results are for 50 μm channel length and 100 μm channel length structures. Both sets of data show

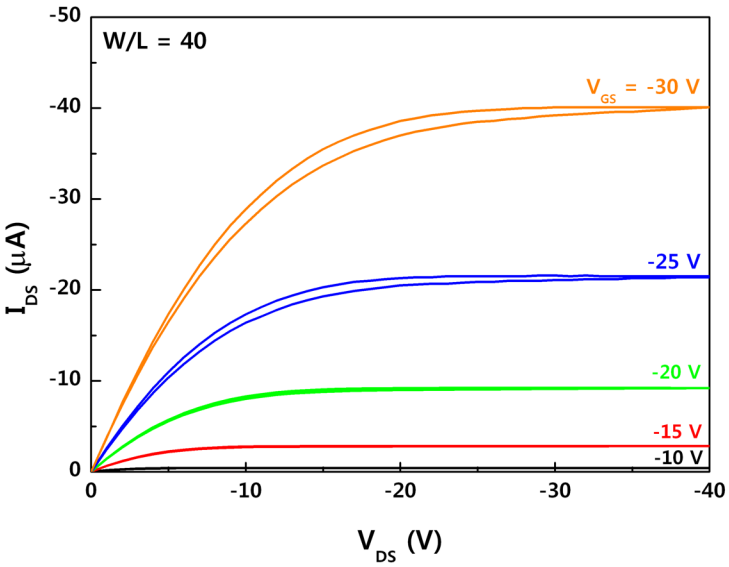
Table 4.1: Summary of pentacene/PMMA OTFT characteristics.

PMMA thickness [nm]	Channel length [μm]	Channel width [μm]	Field-effect mobility [$cm^2\ V^{-1}\ s^{-1}$]	Sub-threshold slope [$V\ dec^{-1}$]	Threshold voltage [V]	On/Off current ratio
152	50	500	0.270	2.0	-8	6.9×10^6
	50	1000	0.343	1.2	-5	9.7×10^5
	50	2000	0.333	1.5	-11	1.2×10^6
	50	4000	0.383	2.9	-7	1.5×10^5
	100	1000	0.294	1.7	-10	6.3×10^6
	200	2000	0.259	1.6	-9	5.7×10^6
427	50	500	0.151	5.2	-8	4.1×10^4
	50	1000	0.113	7.4	-7	2.1×10^4
	50	2000	0.192	5.4	-8	3.5×10^3
	50	4000	0.232	9.9	-7	5.7×10^3
	100	1000	0.170	11.0	-10	3.5×10^3
	200	2000	0.148	3.7	-9	1.6×10^6
810	50	500	0.014	4.5	-18	2.1×10^4
	50	1000	0.019	3.4	-17	3.2×10^4
	50	2000	0.020	2.6	-14	8.6×10^4
	50	4000	0.017	2.9	-11	1.1×10^5
	100	1000	0.024	2.5	-14	2.8×10^4
	200	2000	0.024	2.4	-14	5.6×10^4

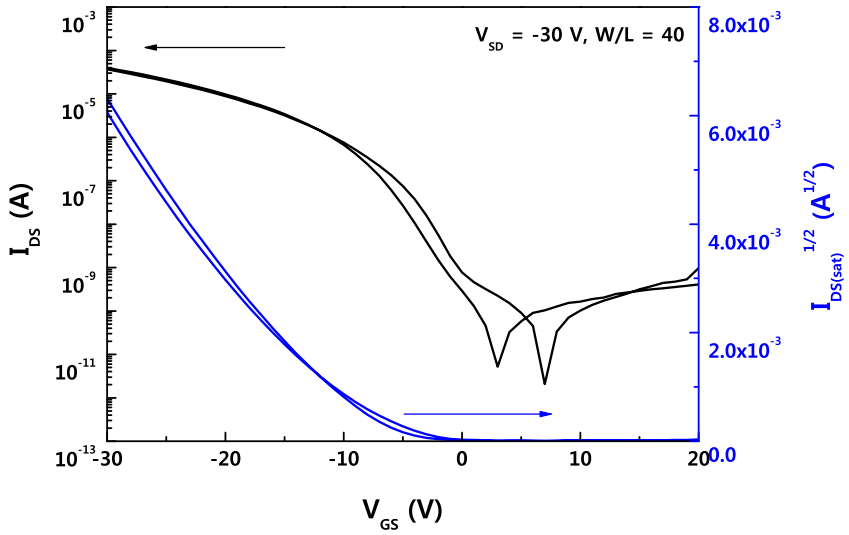
similar output characteristics. However, the device with the longer channel shows improved saturation at lower values of V_{DS} and less hysteresis (evident as the gate-source voltage is increased). These effects are attributed to the ability to align the pentacene and electrode patterns during OTFT manufacture.

4.6 Device Characteristics

Table 4.1 provides a summary of the electrical characteristics for all of the devices that were fabricated in this study. The output and transfer characteristics for an optimised OTFT are shown in Figure 4.14; PMMA thickness = 152 nm, channel dimensions L = 50 μm, W = 2000 μm. For the output characteristics (Figure 4.14(a)), linear behaviour at low V_{DS}, with good drain-source current saturation



(a)



(b)

Figure 4.14: (a) Output and (b) transfer characteristics of a pentacene-based OTFT using PMMA as the gate dielectric. Channel length = 50 μm, channel width = 2000 μm.

was observed. For gate voltages below - 25 V, minimal hysteresis is evident when the direction of the drain voltage scan is reversed. This suggests a relatively 'clean' (in an electronic sense) interface between the pentacene and the PMMA; also apparent

from the minimal hysteresis in the *C-V* characteristics of the MIS structures (Figure 4.6). Figure 4.14(b) shows the transfer characteristics of the device, measured at V_{DS} = -30 V. Plots are given in the form of both $\log(I_{DS})$ versus V_{GS} and $(I_{DS})^{1/2}$ versus V_{GS}. The on/off current ratio, field-effect mobility, threshold voltage, and subthreshold slope for this particular device were: 1.2×10^6, 0.33 cm^2 V^{-1} s^{-1}, -11 V and 1.5 V per decade. These values compare very favorably with published data for pentacene/PMMA OTFTs. [7–9] For example, Huang et al. [10] give μ = 0.24 cm^2 V^{-1} s^{-1} and V_T = -6.3 V, Puigdollers et al. [9] report μ = 0.01 cm^2 V^{-1} s^{-1} and V_T ∼-15 V and Kang et al. [7] have measured μ = 0.045 cm^2 V^{-1} s^{-1}, V_T = -27.5 V. It is interesting to note that these three investigations used gate dielectric thicknesses that are greater than the 152 nm for our optimised device; for example, 700 nm in the case of Puigollers et al. [9], and 945 nm for Kang et al. [7]. This is entirely consistent with the trend of the data shown in Table 4.1, which reveal an improvement in the OTFT characteristics as the PMMA thickness is reduced. The 300 nm film thickness figure and the mobility value of 0.24 cm^2 V^{-1} s^{-1} obtained by Huang et al. [10] fit well with the trend of the data shown in the inset to Figure 4.8(b).

4.7 Inverters

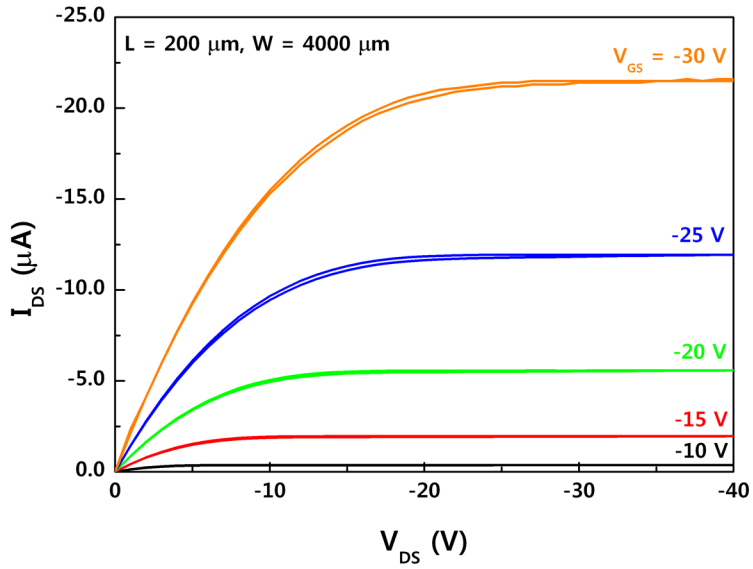
OTFTs are promising candidates for information displays, chemical sensors and radio frequency identification tags. For these and other applications, it is important to incorporate the individual OTFTs into electronic circuits, such as amplifiers and inverters [31–35]. Two inverter configurations are commonly employed with OTFTs. A complementary design can be used [36–39] if both n-channel and p-channel devices are available. Unfortunately, n-channel organic devices degrade relatively quickly in air by interaction with oxygen and/or moisture. A number of air-stable n-type compounds have been reported but, generally, these exhibit inferior charge-carrier mobilities to their p-channel counterparts [38]. As a result, most organic inverters are based on p-channel devices [40–43]. The design of such an inverter is challenging. For example, one problem with the conventional diode-connected load inverter, which uses a p-type device as the active load, is that the output voltage is not determined

by the power supply but is controlled by the threshold voltage of the load transistor. In this section, a pentacene-based bootstrapped inverter that exploits capacitive coupling and bootstrapping effects is designed, fabricated and tested. Among the various polymer gate dielectrics, devices using PVP possess high values of charge carrier mobility [44]. However, these can also exhibit a hysteresis behaviour that leads to a threshold voltage shift depending on the direction of the gate-source voltage sweep [45]. Therefore PMMA, which shows minimal hysteresis, is used as the gate dielectric in this study. The resulting devices exhibit reasonable charge carrier mobilities and minimal hysteresis [46]. The experimental results for the inverter circuits are contrasted to those obtained using computer simulation.

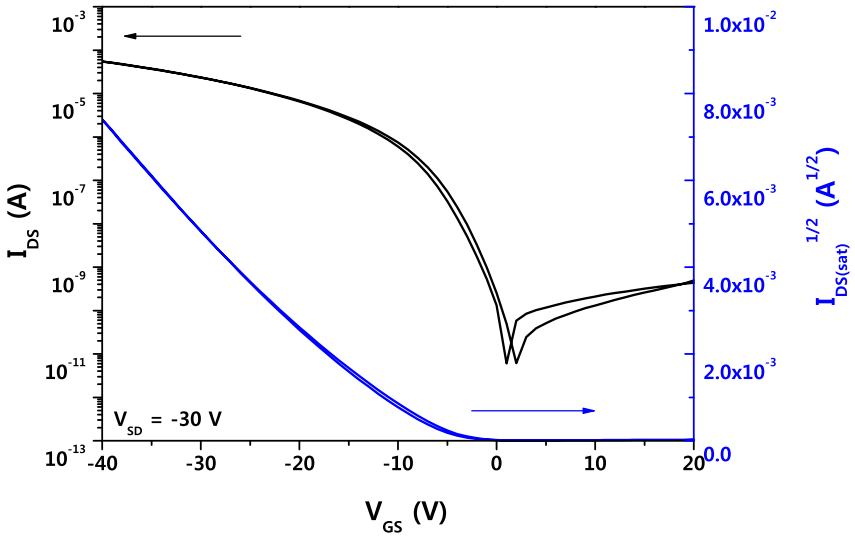
4.7.1 Device Modelling

The output and transfer characteristics of a pentacene OTFT, which were used for the extraction of the device parameters, are shown in Figure 4.15; device channel length (L) = 200 μm, channel width (W) = 4000 μm. In each case, forward and reverse voltage scans are shown. The output characteristics (Figure 4.15(a)) exhibit linear behaviour at low drain-source voltage (V_{DS}). At higher bias, good drain-source current (I_{DS}) saturation is observed with very little hysteresis evident on reversing the direction of the drain voltage scan. Figure 4.15(b) shows the transfer characteristics of the device, measured at V_{DS} = -30 V. Plots are given in the form of both $\log(I_{DS})$ versus the gate-source voltage (V_{GS}), and $(I_{DS(sat)})^{1/2}$ versus V_{GS}. The on/off current ratio, field-effect mobility, threshold voltage, and subthreshold slope for this device were: 2.2×10^6, 0.32 cm^2 V^{-1} s^{-1}, -10.0 V and 1.5 V per decade.

The electrical behaviour of the OTFTs were simulated by a SPICE model adopted for hydrogenated amorphous silicon (a-Si:H) thin film transistors. Using the output and transfer characteristics in Figure 4.15, the model parameters were extracted using commercial simulation software, AIM Extract for the AIM-SPICE a-Si TFT Model ASIA2 (level 15). A table of model parameters is given in Appendix A (Table A.1) of this thesis. Figure 4.16 compares the measured and simulated data of the OTFT which was subsequently used for the inverter circuit: 50 μm channel



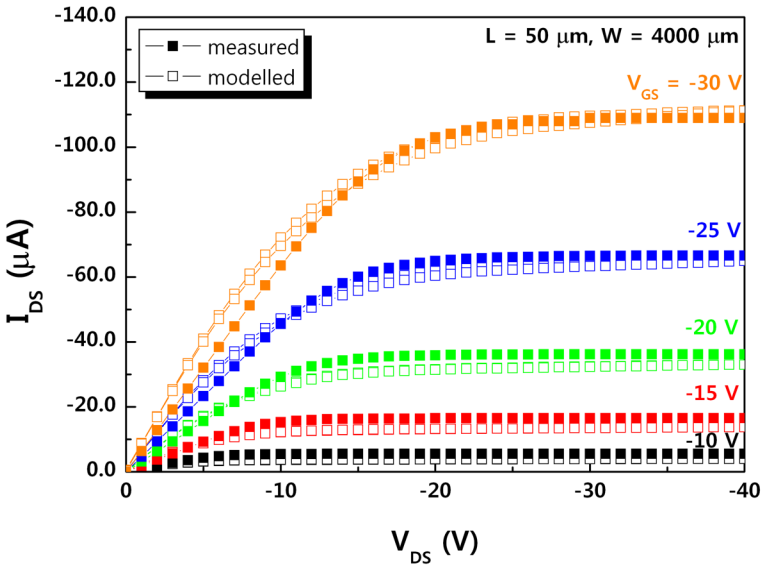
(a)



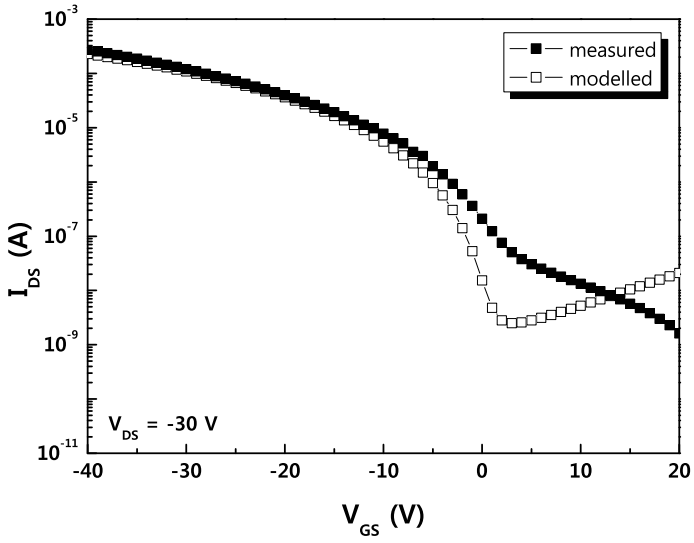
(b)

Figure 4.15: (a) Output and (b) transfer characteristics of a pentacene-based OTFT using PMMA as the gate dielectric. Channel length = 200 μm, channel width = 4000 μm.

length and 4000 μm channel width. The data represented by the filled symbols are the simulation results from AIM-SPICE using the parameters extracted from the previous sample, while the open data points are the measured results. The output



(a)



(b)

Figure 4.16: Comparison between measured (full data points) and modelled (open data points) OTFT (a) output and (b) transfer characteristics. Channel length = 50 μm, channel width = 4000 μm.

characteristics show a very good agreement between theory and experiment (Figure 4.16(a)). However, some deviation is evident in the case of the transfer characteristics for the OTFT in its off-state (Figure 4.16(b)). This is thought to be a result of

experimental variations during device manufacture.

4.7.2 Diode-Connected Load Inverter

The circuit diagram of a diode-connected load inverter is shown in Figure 4.17. When the input signal (V_{IN}) is low ($V_{IN} = V_{DD}$, the lower power rail voltage), P1 will be turned on and the output node (V_{OUT}) will be high (V_{OUT} = Ground (GND), the upper power rail voltage). P2 will also be turned on when V_{IN} is low (V_{DD}) because P2 is used as a diode-connected load. For the circuit design, transistor P1 should therefore have a larger channel W/L ratio than P2 to pull-up V_{OUT} towards the GND value. On the other hand, when V_{IN} is high (GND), P1 will be turned off ($V_{GS} = 0$) and P2 will be turned on ($V_{GS} = V_{DD}$). Consequently V_{OUT} will be low (V_{DD}).

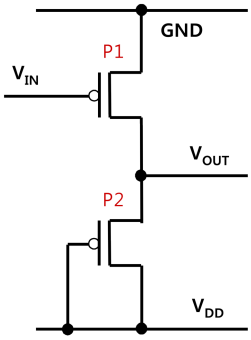


Figure 4.17: Circuit diagram of a diode-connected load inverter.

Figure 4.18 shows the dynamic switching characteristics of the diode-connected load inverter operating at a frequency of 1 kHz; the W/L channel ratios of the two transistors were 4000/50 μm for P1, and 500/50 μm for P2. The input voltage is shown in the top figure while the graph below reveals the output data; simulated (dots) and measured (solid line). It is evident that the output switching voltage range (±10 V) is significantly less than that of the input (±15 V), as predicted by the SPICE simulation. This is because the output swings are determined by the dimensions and the threshold voltage of the OTFTs; in particular, the low output level is determined by the threshold voltage of P2 (∼-10 V).

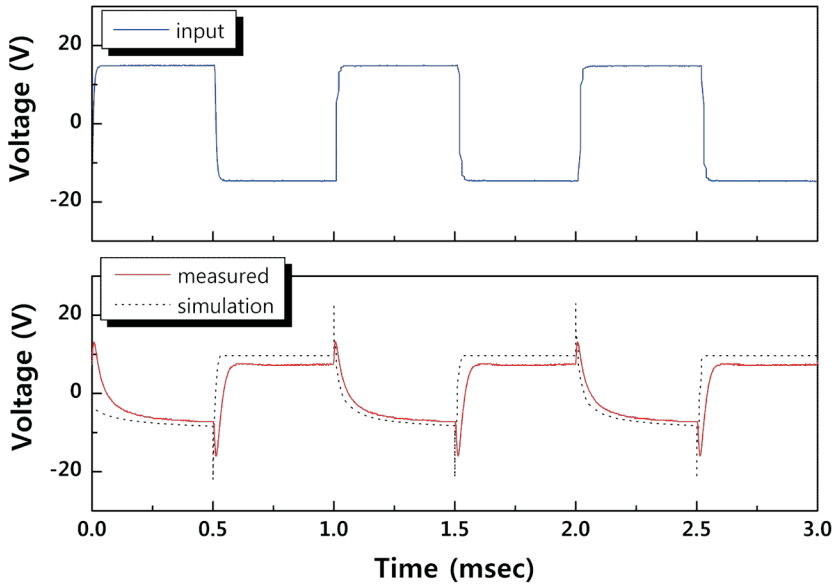


Figure 4.18: Measured and simulated output signals of a diode-connected load inverter. Operating frequency = 1 kHz; drive voltage = 30 V.

4.7.3 Bootstrapped Inverter

The circuit diagram of an alternative inverter using capacitive coupling and bootstrapping effects is shown in Figure 4.19 ; this operates like a push-pull CMOS inverter [47].

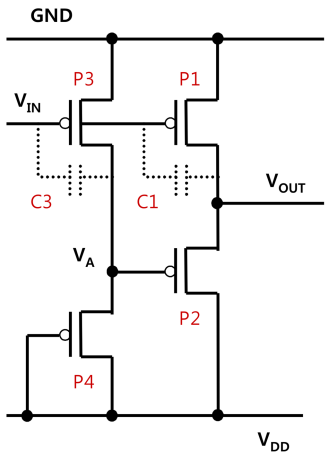


Figure 4.19: Circuit diagram of the bootstrapped inverter used in this work.

The input voltage is applied simultaneously to the gates of P1 and P3. The capacitors C1 and C3, indicated by dotted lines in Figure 4.19, are gate-drain overlap

capacitors of P1 and P3, respectively. When V_{IN} is low (V_{DD}), both P1 ($V_{GS} = V_{DD}$) and P3 ($V_{GS} = V_{DD}$) will be turned on. As a result, V_A will become high and P4 ($V_{GS} = V_{DD}$) will be turned on. In the design, P4 has a smaller W/L channel ratio than P3 in order to maintain V_A high (GND), P2 ($V_{GS} = 0$) will be turned off and V_{OUT} will go up and remain high (GND). When V_{IN} becomes high (GND), bootstrapping effects will lead to V_{OUT} becoming higher than V_A if P1 has a wider channel than P3. In this case, the capacitance of C1 is higher than C3 because gate-drain overlap capacitance is proportional to the channel width. P2 will be turned on and VOUT will go low (V_{DD}) if the difference between V_{OUT} and V_A is greater than the threshold voltage of P2. This means that the output voltage swings are determined by the GND and V_{DD} levels. Furthermore, to overcome the high threshold voltage of P2, P4 can be used to pull-down V_A. The capacitances C1 and C3 are given by

$$C = \epsilon_0 \epsilon_r \frac{S}{d} \tag{4.6}$$

where S is the area of overlap between the gate and source/drain metallisation, d is the distance between the gate and source/drain metal, and ϵ_0 and ϵ_r are the permittivity of free space and the relative permittivity of the gate dielectric, respectively.

Figure 4.20 shows the dynamic switching characteristics of the bootstrapped inverter operating at 1 kHz. As for Figure 4.18, the input voltage is shown in the top figure while the graph below reveals the output data; simulated (dots) and measured (solid line). The W/L channel ratios of the OTFTs used in the bootstrapped inverter were: 4000/50 μm for P1, 2000/50 μm for P2, P3, and 500/100 μm for P4. The overlap capacitance was designed as 20.7 pF for C1 and 10.3 pF for C3. The results demonstrate that, as a result of bootstrapping, the difference between V_{OUT} and V_A is greater than the threshold voltage of P2. This leads to operation that is not restricted by the threshold voltage of the OTFTs. Figure 4.21 compares the simulated difference voltage between nodes V_A and V_{OUT} (V_{GS} of P2), and the input signal. This demonstrates clearly that, when V_{IN} becomes high, V_{GS} is much

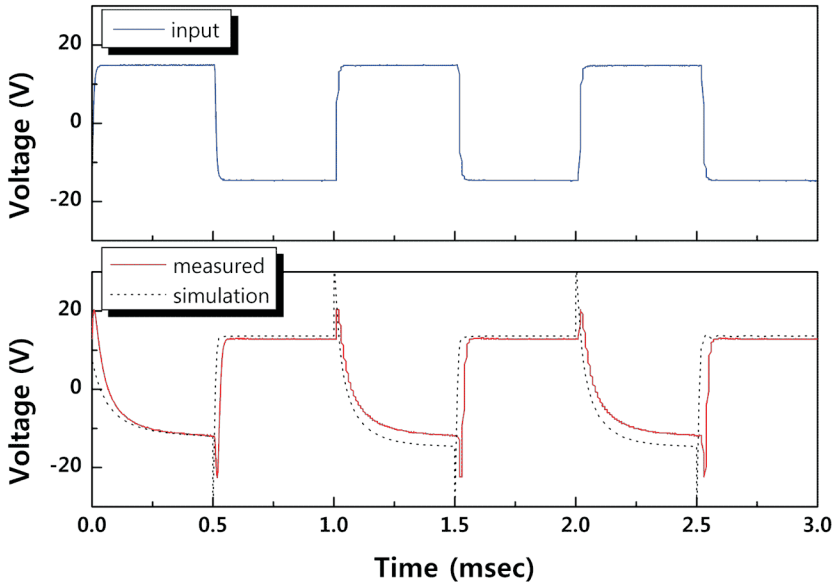


Figure 4.20: Measured and simulated output signals of a bootstrapped inverter. Operating frequency = 1 kHz; drive voltage = 30 V.

higher than the threshold voltage of P2, as a result of the coupling capacitor.

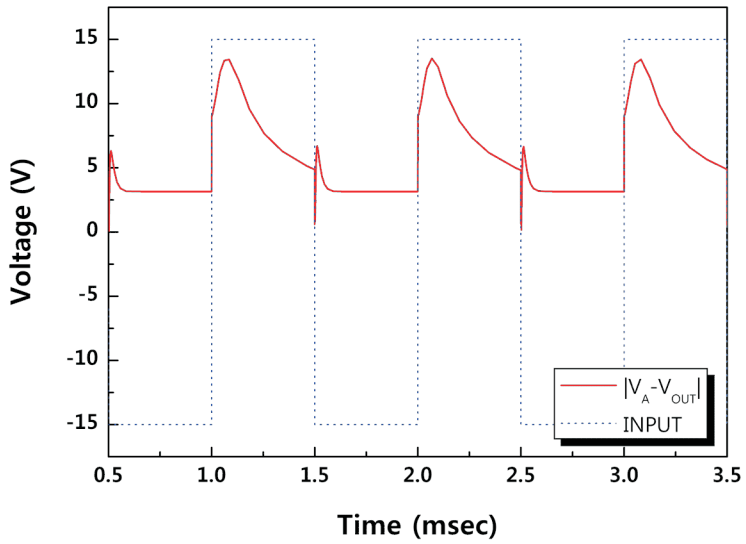


Figure 4.21: The simulated difference voltage between nodes V_A and V_{OUT} compared to the input voltage of a bootstrapped inverter.

Finally, Figure 4.22 compares the measured dynamic switching characteristics for both the diode-connected load inverter (dots) and the bootstrapped inverter

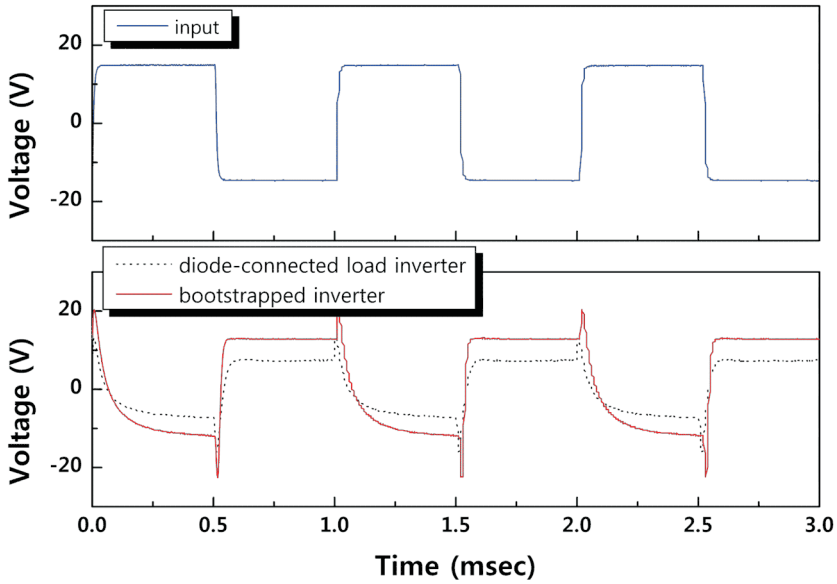


Figure 4.22: Comparison of the measured dynamic switching characteristics of a diode-connected load inverter (dots) and a bootstrapped inverter (full line). Operating frequency = 1 kHz; drive voltage = 30 V.

(solid line) operating at 1 kHz. If the rise and fall times are defined as the time required for the output voltage to rise from the 10 % to 90 % level or drop from the 90 % to 10 % level, respectively, then the bootstrapped inverter has a 30 μs rise time and a 450 μs fall time at 1 kHz with a 30 V driving voltage. The diode-connected load inverter does not reach 10 % or 90 % of the input voltage range due to the high threshold voltage of the load transistor. Published data, which use a different bootstrapping scheme, for a pentacene inverter with a gate dielectric of cross-linked PVP reveal rise and fall times of 10 μs and 125 μs, respectively [42]. However, the operating frequency was 500 Hz, somewhat less than that used in this work. It is significant that PMMA-based devices used here exhibit only one half of the field-effect mobility of the OTFTs with cross-linked PVP [42]. However, the bootstrapped inverter suggested in this thesis shows almost the same performance because of the particular circuit configuration.

4.8 Conclusions

It is shown that the thickness of the PMMA dielectric layer in pentacene OTFTs has a strong influence on the field-effect mobility. In particular, the measured mo-

bility was found to increase as the gate dielectric thickness decreased. With the thickness of the PMMA optimised to 150 nm, the OTFTs possessed a field-effect mobility > 0.3 cm^2 V^{-1} s^{-1}, a threshold voltage of around -11 V, an on/off current ratio $> 10^6$, a subthreshold slope of 1.5 V per decade and minimal hysteresis behaviour. The effect of patterning the pentacene layer during device fabrication was also investigated. This resulted in a significant reduction in leakage currents. Finally, the influence of scaling on the OTFT characteristics was investigated with respect to the channel length and width. The results agree with simple thin film transistor theory. The results show that PMMA is a very promising candidate for use as a dielectric layer in organic electronic devices.

The operations of two different inverter circuits based on pentacene thin-film transistors with a PMMA gate dielectric have been demonstrated. The simple diode-connected load inverter works well but the dynamic switching characteristics are not fully pulled-up to the high voltage rail or pulled-down to the lower voltage rail due to the high threshold voltage of the load transistor. A significant improvement in performance was achieved with a bootstrapped circuit. This exhibited a 30 µs rise time and a 450 µs fall time, operating at 1 kHz with a 30 V drive voltage. Although further work remains, such as the development of a circuit capable of high frequency and low driving voltage operation, the results shown here demonstrate that pentacene/PMMA transistors can be successfully exploited as components in integrated organic electronic circuits.

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Chapter 5

Physically Cross-linked Poly(methyl methacrylate) Gate Dielectrics

5.1 Introduction

The operating voltage of an organic thin-film transistor (OTFT) is determined directly by the thickness and permittivity of the gate dielectric, as discussed in Chapter 4. One way of reducing the gate dielectric thickness, and thereby lowering the OTFT operating voltages, is to exploit self-assembled monolayers (SAMs) [1]. However, these ultra-thin dielectrics require more complex processing than spin-coating. Another approach is to spin-coat an ultra-thin layer of a polymer and then to cross-link the film in situ to provide a more robust layer. To date, a range of different materials has been investigated, including poly-4-vinylphenol (PVP), polystyrene (PS) and polyvinyl alcohol (PVA) [2, 3].

It is difficult to cross-link poly(methyl methacrylate) (PMMA) because of the wide physical separation between radicals. So pentacene-based OTFTs incorporating a PMMA gate insulator usually possess a large operating voltage ($\sim$ -20 V), related to the thickness of the PMMA layer [4, 5]. One encouraging result is that of Noh et al., who have reported devices operating at gate voltages less than 8 V with a 30 nm thick cross-linked PMMA layer [6, 7]. The particular chemical cross-linking methodology that was used, exploiting the cross-linking agent 1,6-bis(trichlorosilyl)hexane (C_6-Si), is a rather demanding procedure as it requires processing in a very high purity inert atmosphere.

In this chapter, a physical method to cross-link PMMA was explored. The use of ion-beam irradiation to produce ultra-thin cross-linked layers of PMMA is reported

and the results show that these layers can be used as the basis of high quality, low-operating-voltage, pentacene transistors. Finally, low voltage operating memory transistors based on various charge storage elements, with cross-linked PMMA as the gate dielectric, have been demonstrated.

5.2 Experiment

Bottom-gate, top-contact OTFTs were fabricated. Glass slides were used as substrates after cleaning sequentially in an ultrasonic bath with acetone, isopropanol and deionised water. An aluminium gate, thickness 40 nm, was defined by thermal evaporation through a shadow mask. To form the gate dielectric, a 2.44 wt % anisole (MicroChem) solution of PMMA (M_w = 93,000, Sigma-Aldrich) was spin-coated at 3000 rpm spinning speed for 50 seconds on the Al and baked for 30 minutes at 120 °C; this resulted in a 57 nm thick layer with 0.65 nm rms roughness. A 1.515 MeV $^4He^+$ ion beam was delivered to the sample surface at 7° grazing incidence using a National Electrostatics Corporation 5SDH Pelletron accelerator. The total charge of the beam was 6 μC per irradiated spot and the incident beam had a diameter of 2.4 mm. The irradiated area was therefore elliptical with axes of 2.4 and 19.7 mm and a total area of 37.1 mm^2. The beam fluence was $1.0\pm0.1\times10^{14}$ ions cm^{-2} giving a linear energy transfer (LET, eV nm^{-1}) figure of about 220 eV nm^{-1} (assuming a polymer density of 1.20 g cm^{-3}). The energy loss and range of MeV ions in solids are well-documented and may be calculated using the stopping and range of ions in matter (SRIM) software made available by Ziegler et. al [8]. The calculated results by SRIM software are given in Appendix B of this thesis (Table A.2). The total range of the ion beam used would be approximately 8.6 microns in PMMA, and in these experiments the energy loss of the beam traversing 57 nm PMMA at 7° is approximately 0.1 MeV. The variation in stopping power (energy loss / distance traversed) of the ion beam over this range is less than 4 %. Therefore, it can be guaranteed that the level of radiation-induced cross linking is similar throughout the film. Pentacene (Sigma-Aldrich) was thermally deposited onto the irradiated PMMA layer at room temperature to a thickness of 40 nm using a shadow mask. The deposition rate was 0.02 nm s^{-1} at a chamber pressure of

approximately 3×10^{-7} mbar. Finally, a further shadow mask was used to define the source and drain contacts, formed by the thermal evaporation of 40 nm of gold.

5.3 Cross-linked Poly(methyl methacrylate)

During ion-beam irradiation of polymers, both cross-linking and scission occur simultaneously, but the relative effectiveness of the two processes depends upon the polymer structure and the LET from the radiation source [9,10]. In the case of high LET, spurs (the discrete energy loss entity) overlap, the probability for two radicals pairs to be in neighbouring chains is increased, and cross-linking is facilitated. For low LET, spurs develop far apart and independently, the deposited energy tends to be confined in one chain not in the neighbouring chain which leads to scission. For example, in the case of PMMA at low LET, most radicals do not cross-link because of the wide physical separation between them and chain scission predominates. These are attributable to a steric hindrance because of the methylester (CH_3OOC-) groups attached to the PMMA backbone structure [11]. However, cross-linking is possible at high LET [10] because the radical density is then higher and the separation between them is reduced. The threshold LET value for PMMA cross-linking is around 15 eV nm^{-1} and the spur distance is about 2 nm for an LET value of 15 eV nm^{-1} [10].

Figure 5.1 shows the structure of PMMA irradiated with various energies [12]. A simple thermal pyrolysis with 0.025 eV energies is shown in Figure 5.1(a). Scission begins with the pendant chain and leads to the release of pendant atoms such as $H^{\bullet}$ and $CH_3OOC^{\bullet}$. A scheme for the case of gamma irradiation, which has relatively low LET (0.2 eV nm^{-1} for ^{60}Co γ-rays), is given in Figure 5.1(b) for irradiation at 1 MeV and 1 Gy (100 rad, J kg^{-1}) over an area of 1 cm^2. Radicals and dangling bonds are created by the release of pendant atoms and by the loss of pendant groups. Thus, various gaseous molecular species are released during irradiation. At high LET, main chain scission begins to dominate as shown in Figure 5.1(c). Thereafter, cross-linking occurs when two free dangling bonds on neighbouring chains unite, whereas double or triple bonds are formed if two neighbouring radicals in the same chain unite. The transferred energy density in Figure 5.1(c) is $\sim10^{-1}$ eV $\mathring{A}^{-3}$, for 2-5 MeV He, Li and Bi ion irradiations.

In this work, the irradiation was undertaken using a 1.515 MeV $^4He^+$ ion beam to achieve a high LET (220 eV nm^{-1}) and effective cross-linking.

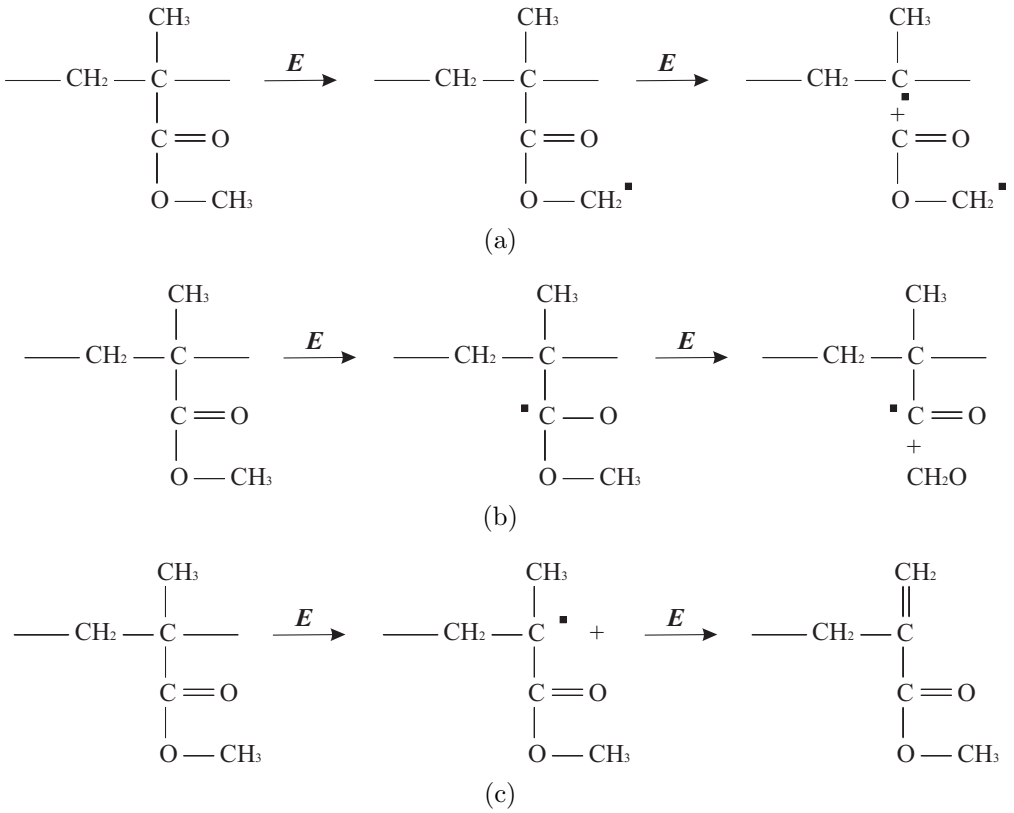


Figure 5.1: The structure of PMMA with (a) a simple thermal pyrolysis, (b) low LET (gamma ray) irradiation and (c) high LET (ion-beam) irradiation [12].

5.3.1 Surface Morphology

Figure 5.2 shows tapping mode atomic force microscope (AFM) images of the surface of a 57 nm spin-coated PMMA film (Figure 5.2(a)), the same film (now 33 nm in thickness) following ion-beam irradiation (Figure 5.2(b)), the irradiated PMMA film after development in acetone (Figure 5.2(c)) and the surface of a 40 nm pentacene film, which was subsequently evaporated onto the irradiated PMMA (Figure 5.2(d)).

Following irradiation, the thickness of the PMMA has been reduced by about one half and the film is no longer soluble in solvents such as acetone or iso-propyl alcohol (IPA):methyl iso-butyl ketone (MIBK) in a 3:1 ratio (used as a developer for PMMA). This suggests that the PMMA has become cross-linked. The ion-beam

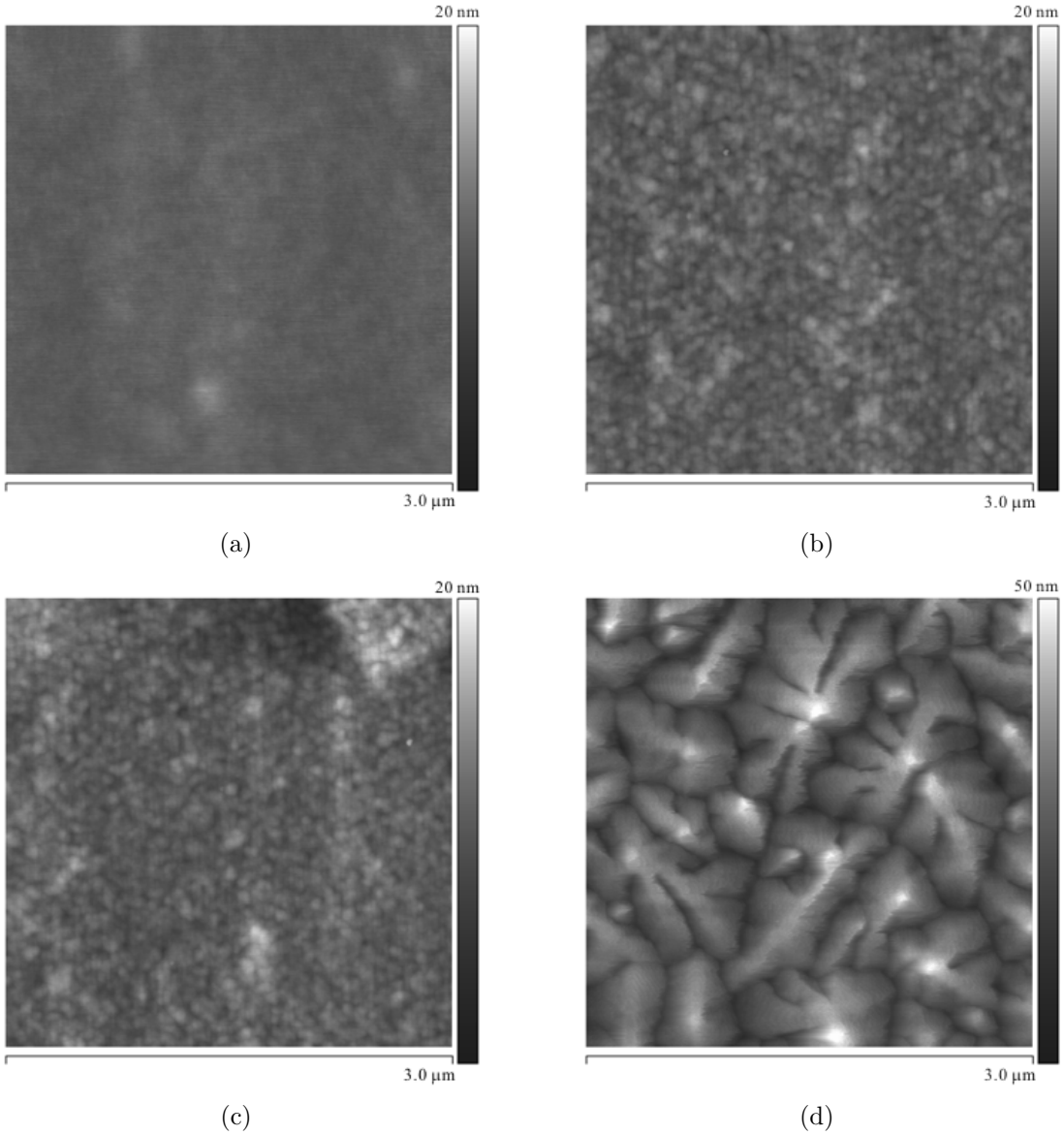


Figure 5.2: Atomic force microscope images of (a) 57 nm thick PMMA film spin coated onto a glass slide, (b) 33 nm thick cross-linked PMMA film by ion-beam irradiation, (c) 33 nm thick cross-linked PMMA film after development in acetone and (d) 40 nm thick pentacene film thermally evaporated on top of the cross-linked PMMA.

irradiation has also resulted in an increase in the RMS surface roughness - from 0.65 nm to 1.34 nm. However, subsequent evaporation of pentacene onto cross-linked PMMA reveals a high quality film with a relatively large grain size (Figure 5.2(d)). The cross-linked PMMA film is referred to as cPMMA in the forthcoming sections.

5.3.2 Electrical Characteristics

A parallel plate capacitor structure (Al/insulator/Au) was fabricated to investigate the dielectric properties of the cPMMA. The area of the capacitor was 1.8 $\times$ 10^{-3} cm^2. Figure 5.3 compares the current density J versus the electric field F behaviour for spin-coated PMMA (80 nm and 430 nm films) and for cPMMA (33 nm).

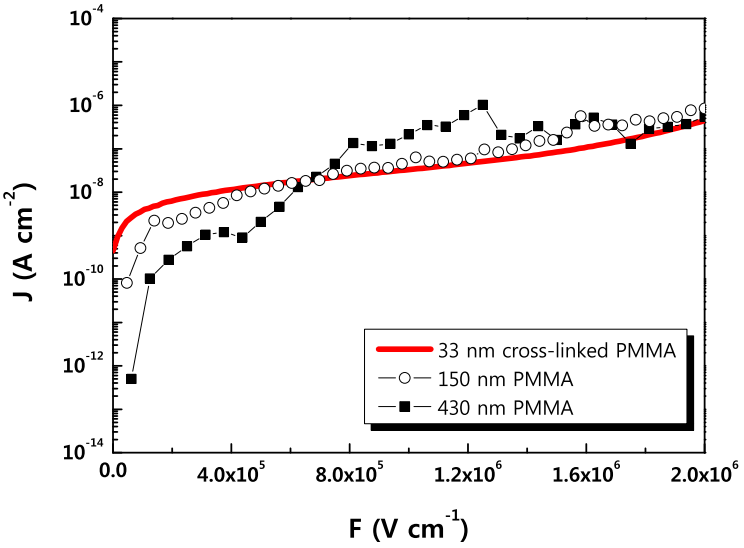


Figure 5.3: Current density versus applied electric field for PMMA films (80 nm and 430 nm in thickness) and a cross-linked PMMA film (33 nm) sandwiched between aluminium and gold electrodes.

The leakage current density of the cPMMA was less than 10^{-8} A cm^{-2} for fields up to 0.35 MV cm^{-1} and this remained below 10^{-6} A cm^{-2} for fields up to 2 MV cm^{-3}. Similar data were measured for the uncross-linked PMMA. In the previous chapter the origin of the electrical characteristics of spin-coated PMMA films have been discussed. The conclusion was that high electric field processes, resulting from Schottky emission, may dominate the electrical behaviour in thin films. In the case of Schottky emission, the conductivity will be limited by the electrodes, perhaps accounting for the similar conductivity values of our cross-linked and uncross-linked films. Further work is needed to clarify this point. However, for the purposes of this

study, the measured leakage current densities are sufficiently small to enable a 33 nm cPMMA film to be used as the gate dielectric in an OTFT.

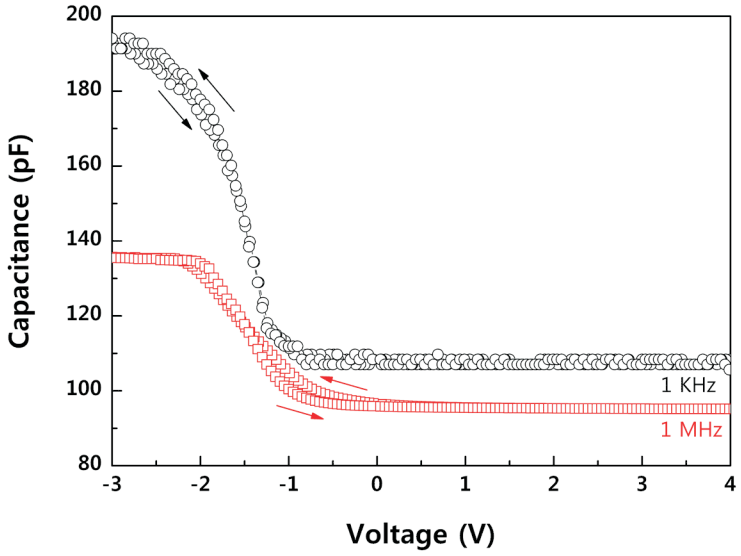


Figure 5.4: Capacitance versus voltage characteristics, measured at 1 MHz and 1 kHz and a voltage scan rate of 0.05 V s^{-1} for aluminium/cross-linked PMMA (33 nm)/pentacene (40 nm)/gold structure.

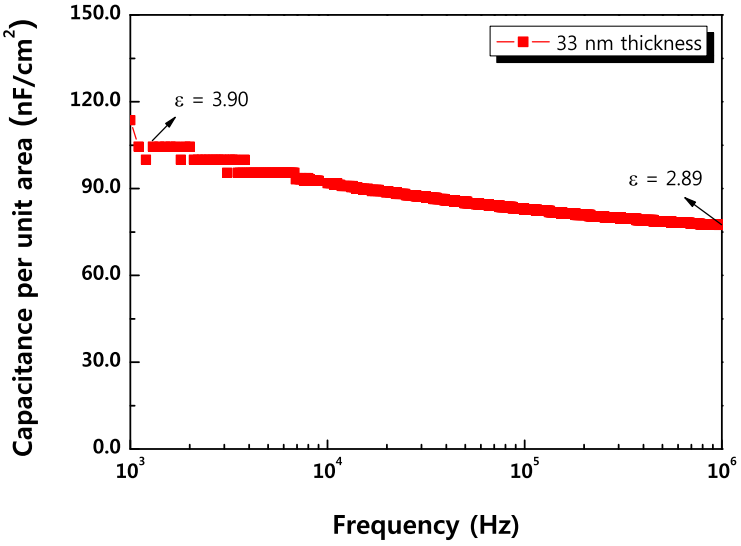


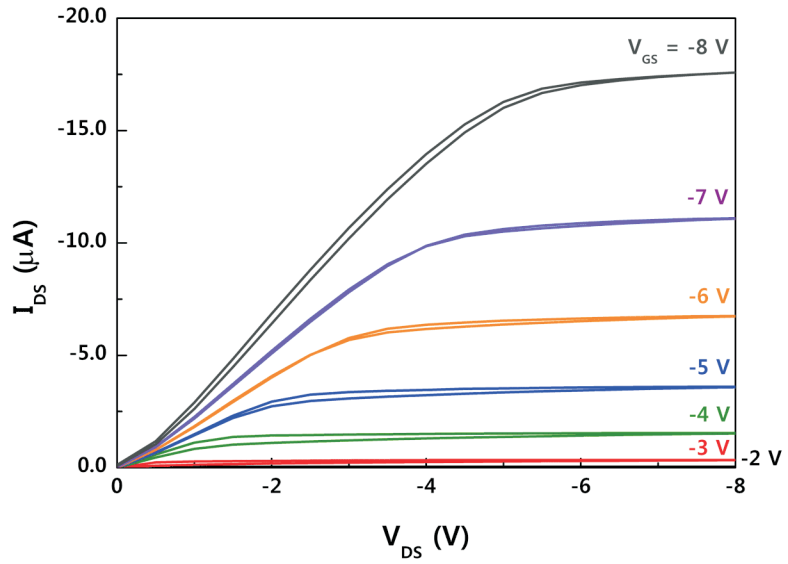
Figure 5.5: Capacitance versus frequency characteristics for 33 nm thick cross-linked PMMA layer sandwiched between aluminium and gold electrodes.

The capacitance, C, versus voltage, V, characteristic, measured at 1 MHz and at 1 kHz and a voltage scan rate of 0.05 V s^{-1}, for an aluminium/cPMMA/pentacene/gold metal-insulator-semiconductor (MIS) structure is depicted in Figure 5.4; figure 5.5 shows the measured capacitance per unit area as a function of frequency for a 33 nm thick cPMMA layer sandwiched between aluminium and gold electrodes. The C-V curves shown in Figure 5.4 reveal only a very small degree of hysteresis on reversing the voltage scan direction. This is very similar to that observed with pentacene/PMMA OTFTs and is consistent with a relatively 'clean' (in an electronic sense) interface between the pentacene and the cross-linked polymer.

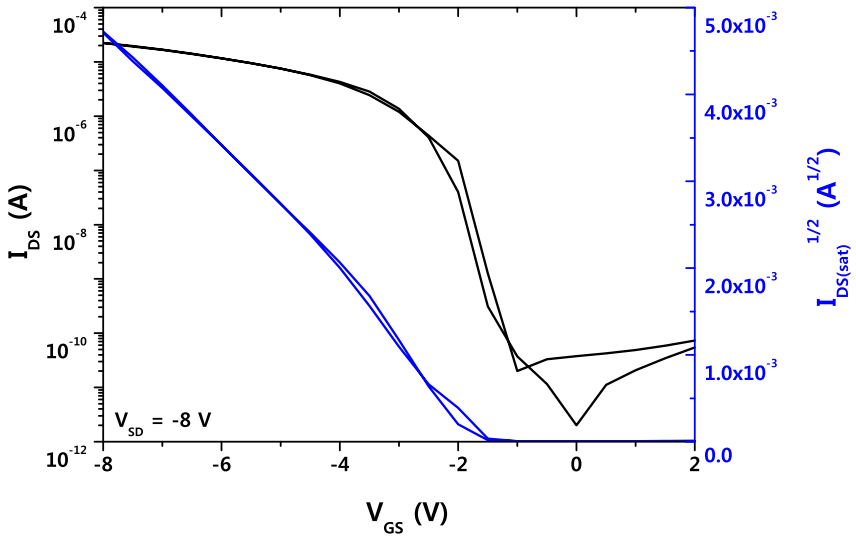
Using the latter curve, the dielectric constant of the cPMMA layer was calculated to be 3.90 ± 0.10 at 1 kHz and 2.89 ± 0.10 at 1 MHz. These values are almost the same as those reported for PMMA [4]. The accumulation capacitance for the MIS structure was found to scale with the cPMMA thickness and the calculated dielectric constant (3.80 ± 0.10 at 1 kHz and 2.70 ± 0.10 at 1 MHz) was the same, within experimental errors, as the value calculated from Figure 5.5. The dielectric constant of pentacene was calculated to be 6.07 ($C_{pentacene}$ = 250 pF) at 1 kHz and 9.32 ($C_{pentacene}$ = 384 pF) at 1 MHz from the minimum capacitance value in Figure 5.4. While the value at 1 MHz is higher than that generally reported for pentacene (3∼6) [13,14], the value at 1 kHz agrees well with other literature reports. Therefore, a low frequency should be used to ensure the measured capacitance is equal to the pentacene (fully depleted) layer capacitance (see discussion in section 4.3.2). The doping density for the pentacene can be estimated to be 4.31×10^{16} cm^{-3} at 1 kHz 8.89×10^{16} cm^{-3} at 1 MHz from the slope in the linear region in Figure 5.4, which are in good agreement with the reported results [15, 16].

5.4 Device Characteristics

The output and transfer characteristics for an OTFT with a 33 nm cPMMA gate dielectric, formed by spin-coating and ion-beam irradiation, are shown in Figure 5.6 (device channel length = 50 μm, and width = 500 μm). The output characteristics plotted in Figure 5.6(a) reveal the drain current, I_{DS}, as a function of source-drain voltage, V_{DS}, for different values of gate voltage, V_{GS}. The device shows excellent



(a)



(b)

Figure 5.6: (a) Output and (b) transfer characteristics of a pentacene-based OTFT using 33 nm cross-linked PMMA as the gate dielectric. Forward and reverse voltage scans are shown for both sets of data. Device channel length = 50 μm; channel width = 500 μm.

transistor behaviour in the linear and saturation regions. Moreover, the device operates at relatively low voltages, < 10 V. The transfer characteristics, Figure 5.6(b), are measured at V_{DS} = -8 V. Plots are given in the form of both log(I_{DS}) versus

V_{GS} and $(I_{DS(sat)})^{1/2}$ versus V_{GS}. The on/off current ratio, threshold voltage, V_T, and sub-threshold slope for the device were 1.1×10^6, -0.9 V, and 219 mV decade^{-1}. Such characteristics compare very favourably with other recently published data for pentacene/PMMA OTFTs, the insulator thicknesses of which are greater than that reported in this work [4,5,17–19]. The field-effect mobility, μ_{sat}, was estimated in the saturation region of the transistor, using Equation 2.11, i.e. from a plot of $(I_{DS(sat)})^{1/2}$ versus V_{GS}. Using the data from Figure 5.6(b) provided a mobility of 1.1 cm^2 V^{-1} s^{-1} (using a permittivity value of 3.9 for the cPMMA). This will be a mean value, as the field effect mobility will vary along the channel of the OTFT. The mobility figure obtained in this work is higher than that previously obtained with thicker PMMA films in the previous chapter.

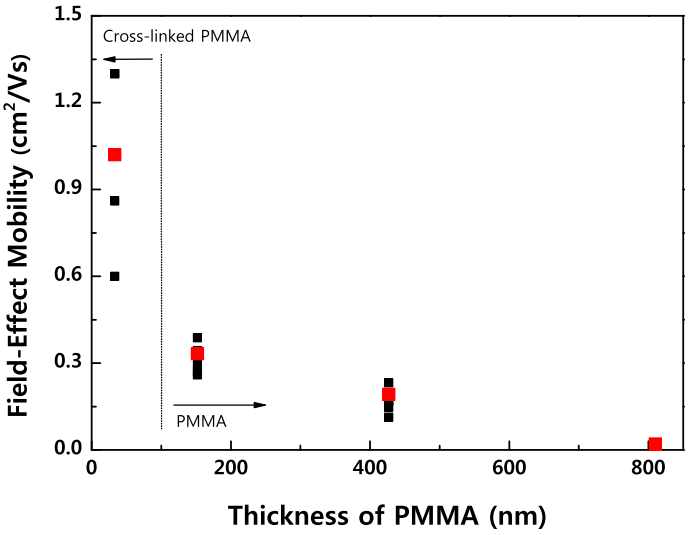
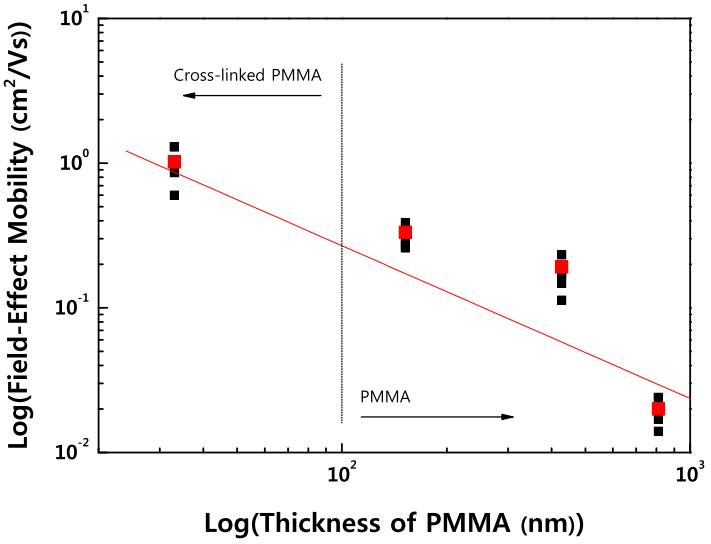


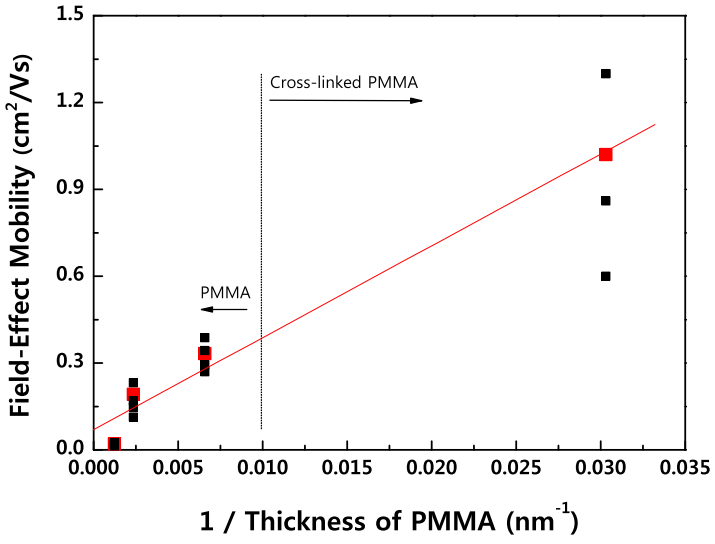
Figure 5.7: Saturated field-effect mobility as a function of the thickness of PMMA.

Figure 5.7 shows the variation in the saturated field-effect mobility (μ_{sat}) with dielectric thickness (d) of a number of different devices. A clear trend showing an increase in μ_{sat} with decrease in d is evident. Other workers on organic transistors have reported mobilities that depend on the gate voltage, even when V_{GS} exceeds V_T as discussed in section 2.4.6 [20–24]. The same effect will be obtained if V_{GS}

is held constant and the gate dielectric thickness is reduced, due to an increase in the electric field in the dielectric. This may explain the higher field-effect mobilities with decreased thickness of gate dielectric.



(a)



(b)

Figure 5.8: Saturated field-effect mobility (μ_{sat}) as a function of the thickness of PMMA (d) in the form of (a) $\log(\mu_{sat})$ versus $\log(d)$ and (b) μ_{sat} versus d^{-1}.

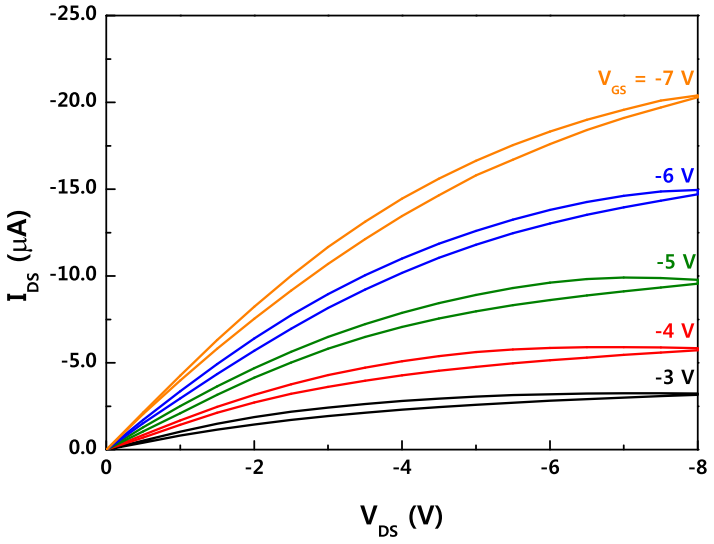
Table 5.1: The results of linear fit (yscale(Y) = A + B × xscale(X)) for the plots of log(μ_{sat}) versus log(d) and μ_{sat} versus d^{-1}.

	A value	A error	B value	B error	R	SD
log(μ_{sat}) vs log(d)	-7.96013	2.26655	-1.05562	0.33775	-0.91107	0.35483
μ_{sat} vs d^{-1}	0.07037	0.05366	3.172E-8	3.448E-9	0.98839	0.08155

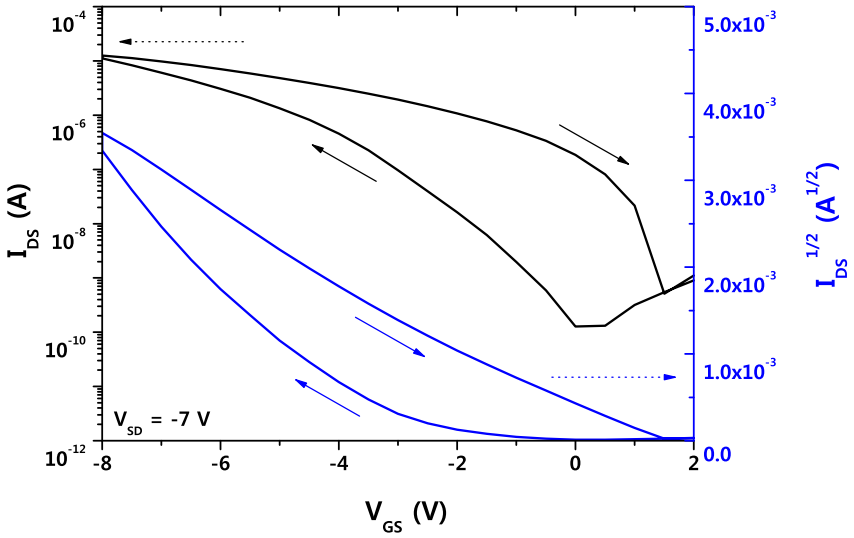
A: Intercept value and its standard error
B: Slope value and its standard error
R: Correlation coefficient
SD: Standard deviation of the fit

Various curve fitting procedures were used to identify a mathematical relationship between the saturated field-effect mobility, μ_{sat}, and the dielectric thickness, d. Figure 5.8(a) shows a plot of log(μ_{sat}) against log(d). The results suggest a relationship of the form $\mu_{sat} \propto d^{-1}$, which is supported by Figure 5.8(b) where μ_{sat} is plotted against d^{-1}. The results of the linear fit to the two plots in Figure 5.8 are given in Table 5.1. This relationship can be explained by the gate bias dependent field-effect mobility as discussed in section 2.4.6. A relationship between μ_{sat} and d can be given by rewriting Equation 2.14 and Equation 4.5 as $\mu \propto d^{-T_c/T+1}$. The field-effect mobility with traps is found to be dependent on the dielectric thickness and this dependence is a function of a characteristic temperature T_c, the steepness in the trap concentration [24, 25]. The value of T_c/T can be assumed to be around 2 for pentacene-based OTFTs.

The thinnest cPMMA layers used in this work were 30 nm, limited by the quality of the PMMA. The output and transfer characteristics for an OTFT with a 20 nm cPMMA gate insulator are shown in Figure 5.9 (device channel length = 50 μm, and width = 2000 μm). The relatively large amount of hysteresis can be attributed to charge trapping and de-trapping of the free dangling bonds or unpaired radicals which can not be cross-linked because the film is too thin. The calculated value of μ_{sat} for the 20 nm cPMMA gate insulator devices was 0.051∼0.221 $cm^2\ V^{-1}\ s^{-1}$ using a permittivity value of 3.9 for the cPMMA.



(a)



(b)

Figure 5.9: (a) Output and (b) transfer characteristics of a pentacene-based OTFT using 20 nm cross-linked PMMA as the gate dielectric. Forward and reverse voltage scans are shown for both sets of data. Device channel length = 50 μm; channel width = 2000 μm.

5.5 Low Voltage Operating Memory Devices

There is now growing interest in organic memory devices and an organic charge trapping memory transistor (i.e. flash memory) is a potential candidate for a prac-

tical memory. This can be fabricated by means of nanoparticles or nanocrystals acting as charge traps in a gate dielectric [26,27]. For example, Mabrook et al. have reported a memory transistor based on pentacene and PMMA with self-assembled gold nanoparticles (GNPs) using the organic capping layer as the tunnelling dielectric [28]. The devices exhibited a large memory window as well as good charge retention properties. However, the preparation and the deposition of GNPs involve complex processes and several tens of volts were required on the gate of the memory transistor to programme it. Therefore, in this thesis, thin aluminium with aluminium oxide as the tunnelling dielectric and silver with silver oxide as the tunnelling dielectric layers are explored as alternative charge traps, and cPMMA, which enables low operating voltage devices, is used as the blocking dielectric [29].

5.5.1 Thin Aluminium Film

In this study, 3.3 nm, 6.5 nm and 10.5 nm thick aluminium films were used to investigate the possibility of using aluminium to trap charge. Figure 5.10 shows AFM images of the surface of uncoated glass and 3.3 nm, 6.5 nm and 10.5 nm thick aluminium films, which were thermally evaporated onto the glass. These images suggest that the thinner aluminium films are less dense and have less conducting pathways. This was investigated by measuring the in-plane *I-V* electrical characteristics.

Figure 5.11 shows the *I-V* characteristics obtained from the 3.3 nm, 6.5 nm and 10.5 nm thick thermally evaporated aluminium films. Data are shown for both increasing (lines) and decreasing (dots) applied voltages. The measurements were carried out using silver paint (silver in methyl ketone from AGAR) contacts, 5 mm long and 1 mm apart, in vacuum. These results suggest that a 3.3 nm thick aluminium film may be used as the charge storage element which is isolated by the aluminium oxide for memory devices; the thicker layers seem to be too conductive.

Organic thin-film memory transistors (OTFMTs) were fabricated using the same device configuration as described in section 5.2, except that a 3.3 nm thick aluminium film was thermally evaporated onto the cPMMA before the deposition of pentacene, as shown in Figure 5.12.

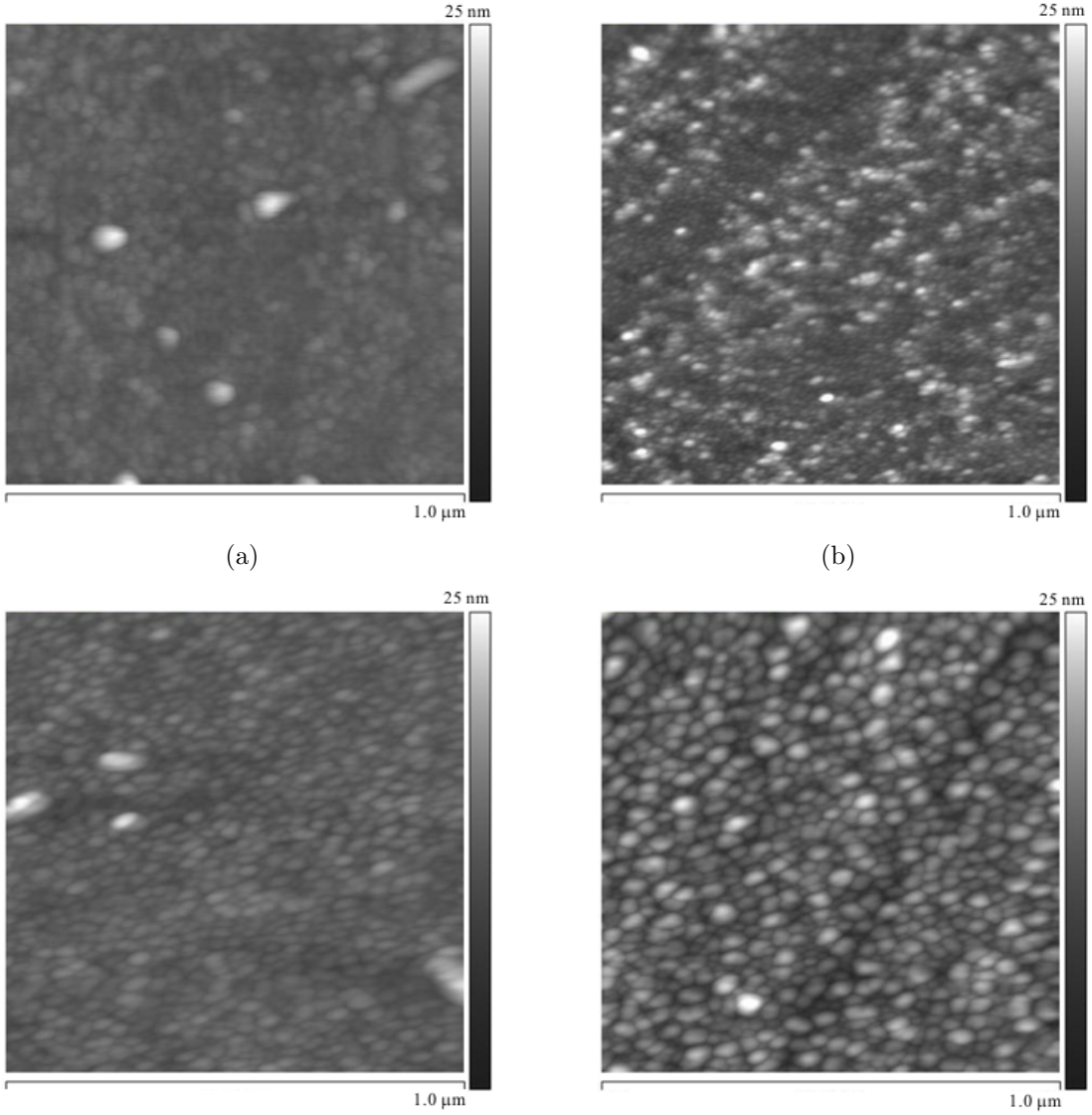


Figure 5.10: Atomic force microscope images of (a) uncoated glass, (b) 3.3 nm, (c) 6.5 nm and (d) 10.5 nm thick aluminium film thermally evaporated on the bare glass.

The output and transfer characteristics for the resulting OTFMT are shown in Figure 5.13 (device channel length = 50 µm, and width = 4000 µm). The OTFMT possesses much lower field-effect mobility values (0.0017∼0.0027 cm^2 V^{-1} s^{-1}) and reduced drain-source currents compared with OTFTs (i.e. devices without metallic nanoparticles). This suggests that the thin aluminium film adjacent to the pentacene surface has affected the current flow through the channel of the transistor [28]. A small amount of hysteresis is evident in both output and transfer characteristics,

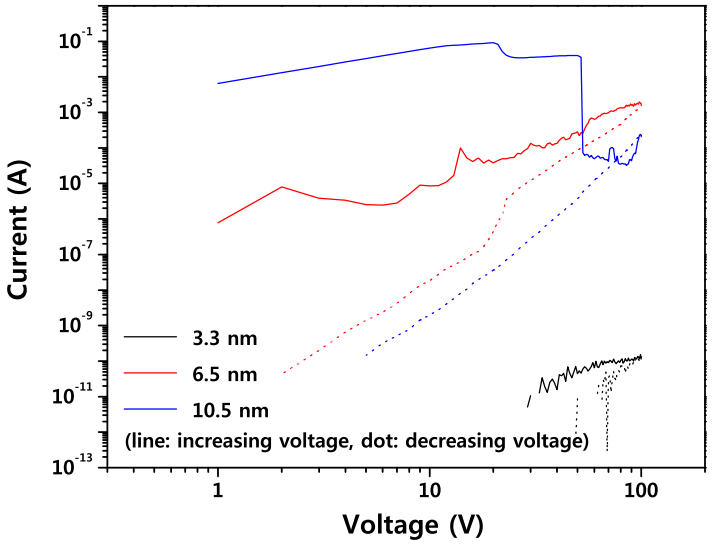


Figure 5.11: In-plane I-V electrical characteristics of 3.3 nm, 6.5 nm and 10.5 nm thermally evaporated aluminium film.

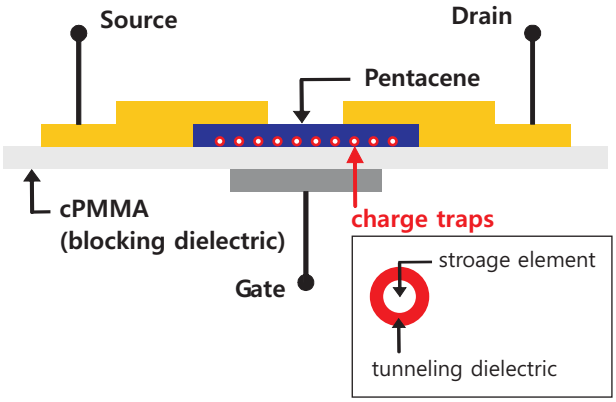
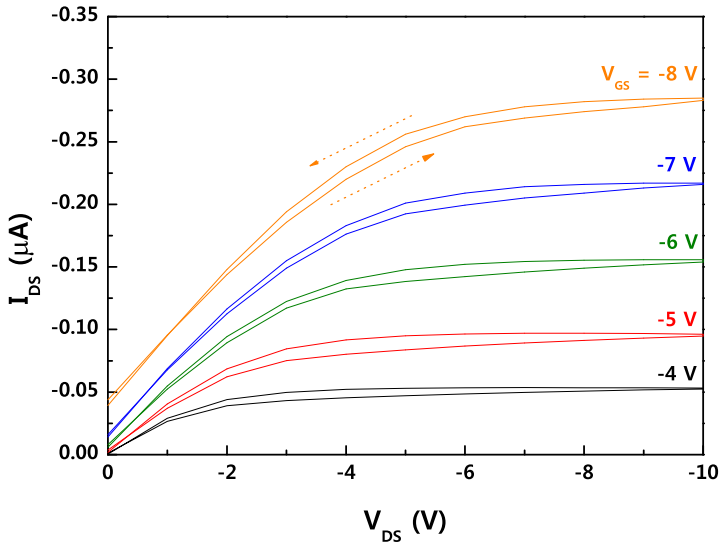
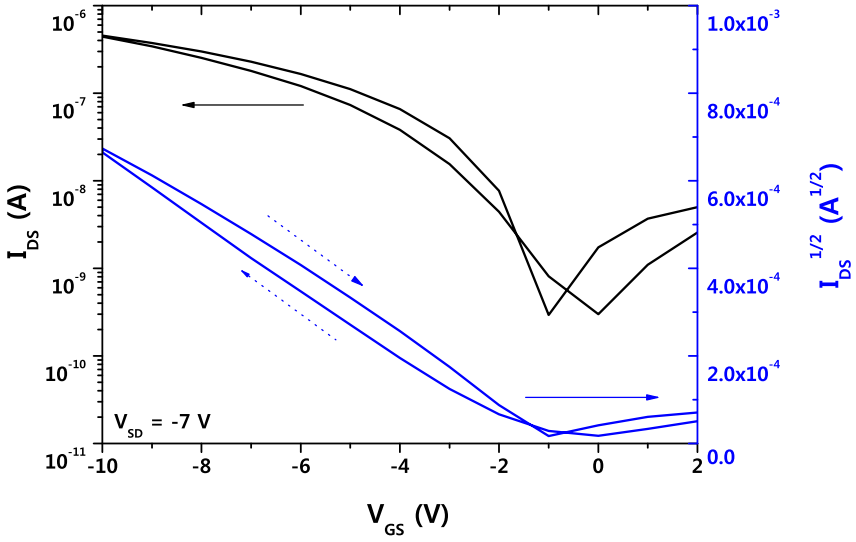


Figure 5.12: A schematic cross-section of a pentacene-based OTFMT with a cPMMA gate dielectric.

and is attributed to the presence of the thin aluminium film. Figure 5.13(b) shows a clockwise hysteresis of the transfer characteristics, in contrast to typical hole charging/discharging of memory devices from the semiconductor surface (counterclockwise hysteresis) [28, 30]. An alternative explanation may be appropriate for this clockwise hysteresis. As the bias voltage of the gate moves toward negative values, electrons are injected from the gate into the thin aluminium film, which then become negatively charged. Consequently, this leads to a shift of the threshold voltage to a less negative value. When the bias voltage is reversed, electrons are ejected from



(a)



(b)

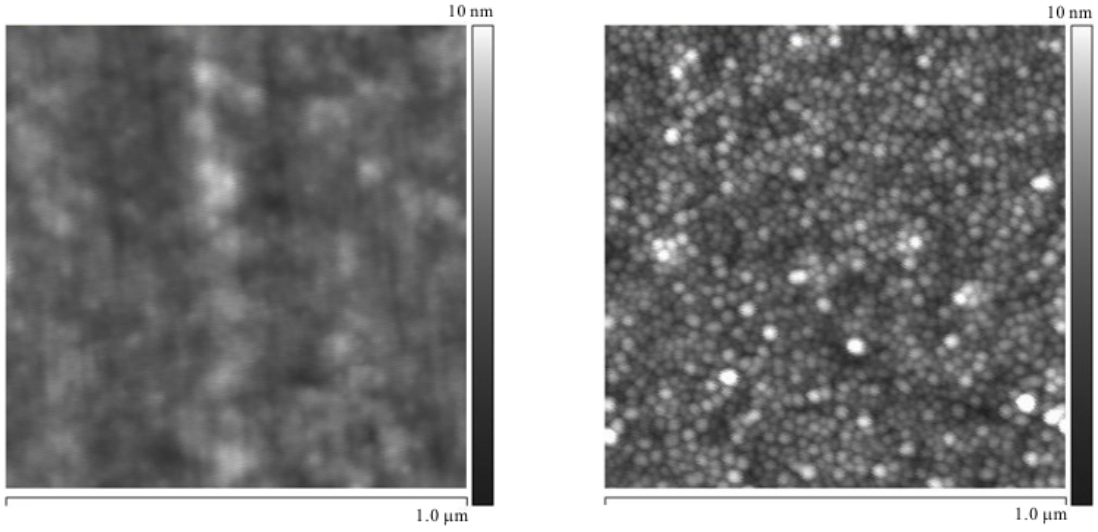
Figure 5.13: (a) Output and (b) transfer characteristics of a pentacene-based memory transistor using 43 nm cross-linked PMMA as the gate dielectric with a 3.3 nm thick aluminium film as the charge trapping layer. Forward and reverse voltage scans are shown for both sets of data. Device channel length = 50 μm; channel width = 4000 μm.

the thin aluminium film into the gate electrode resulting in a shift of the threshold voltage in a negative direction. The memory window of the OTFMT with a

3.3 nm thick aluminium film was very small, even though the device operates at relatively low voltages. This suggests that the charge storage elements may not be fully isolated by the tunnelling dielectric layer. This might be improved by the use of additional thin organic dielectric layer. However, such results demonstrate the potential of a 3.3 nm aluminium film as the charge trapping layer in an OTFMT. Further measurements (e.g., charge/discharge properties and the charge retention properties) are necessary for a full device evaluation.

5.5.2 Thin Silver Film

The same structure as described in the previous section was studied, except that a 3 nm thick layer of silver was used instead of the 3.3 nm aluminium film. Figure 5.14 shows AFM images of the surface of cPMMA and a 3 nm thick silver film, which was thermally evaporated onto the cPMMA. It appears that the 3 nm thick silver film is more dense compared to the 3.3 nm thick aluminium film (Figure 5.10(b)).



(a) (b)

Figure 5.14: Atomic force microscope images of (a) a 43 nm thick cross-linked PMMA film and (b) a 3 nm thick silver film thermally evaporated on top of the cross-linked PMMA.

This was investigated by measuring the in-plane *I-V* electrical characteristics of the 3 nm thick silver film. Contacts to the sample and the measurements were carried out in the same way as before. Figure 5.15 shows the resulting *I-V* characteristics

for both increasing (line) and decreasing (dot) applied voltages. The magnitude of the current for the 3 nm thick silver film was higher than for the 3.3 nm thick aluminium film. This is a result of the more conductive silver oxide (Ag_2O) layer.

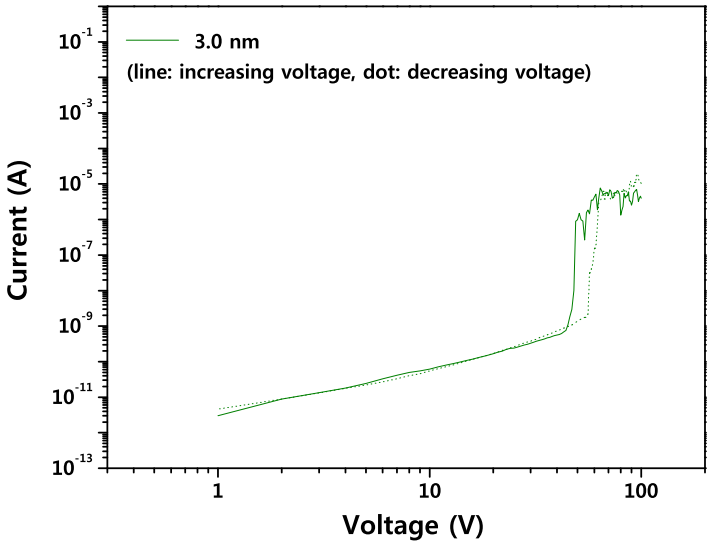
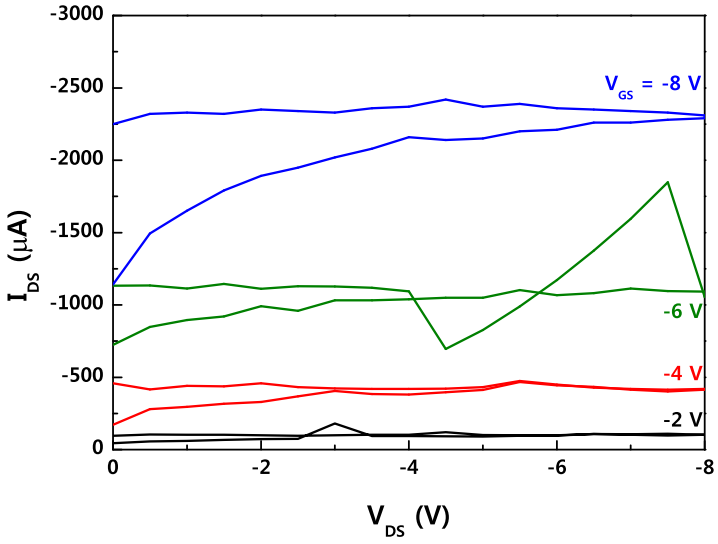


Figure 5.15: In-plane *I-V* electrical characteristics of a 3 nm thermally evaporated silver film.

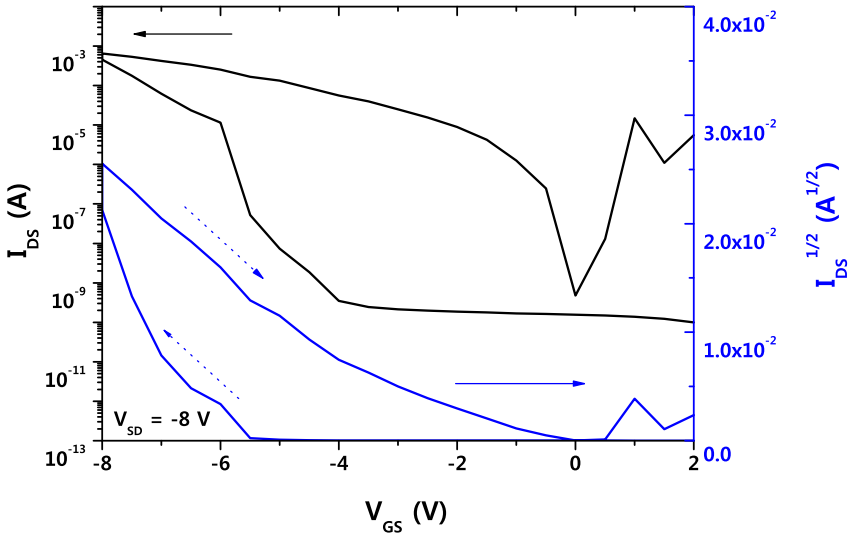
The output and transfer characteristics for an OTFMT with a 3 nm silver film, formed by thermal evaporation, are shown in Figure 5.16 (device channel length = 50 μm, and width = 2000 μm). The OTFMT with the 3 nm thick silver film does not show transistor behaviour; the drain-source current does not depend on the drain-source voltage. This suggests that 3 nm thick silver film plays a role as a parallel conducting path, not as a charge trapping layer, resulting in high leakage currents.

5.5.3 Gold Nanoparticles

OTFMTs were fabricated using the same device configuration as described in the previous section except that GNPs were deposited by a self-assembly process at room temperature before the deposition of the pentacene layer. To deposit GNPs [28], the substrate was placed in a dilute solution of (3-aminopropyl)-trimethoxysilane



(a)



(b)

Figure 5.16: (a) Output and (b) transfer characteristics of a pentacene-based memory transistor using 43 nm cross-linked PMMA film as the gate dielectric with a 3 nm thick silver film as the charge trapping layer. Forward and reverse voltage scans are shown for both sets of data. Device channel length = 50 μm; channel width = 2000 μm.

(APTMS, obtained from Sigma-Aldrich) (0.1 ml of APTMS in 1 ml methanol) for 4 hours. Then, the substrate was rinsed with methanol, immersed in the Au solution

for 20 minutes and finally rinsed with water. Figure 5.17 shows an optical micrograph of a pentacene/cPMMA+GNPs device. The cPMMA layer has clearly been affected during the deposition of GNPs. Further work (e.g., variation in immersion time and solution concentration) is clearly needed to find the reason for this. However, it is evident that the deposition process of GNPs has some critical effects on cPMMA.

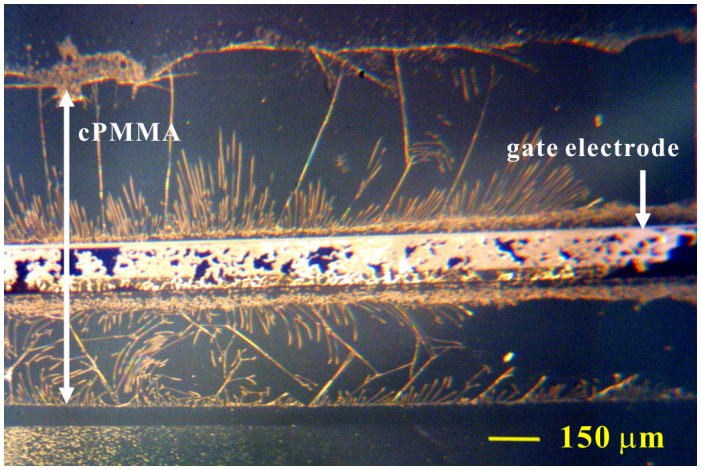
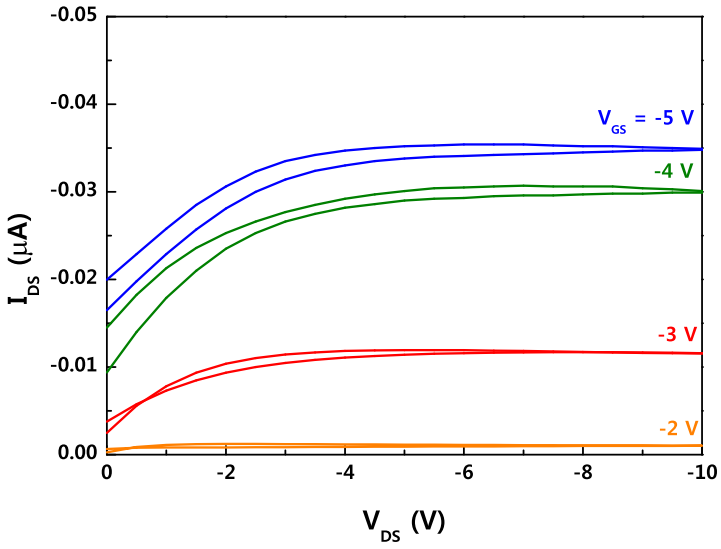


Figure 5.17: Optical micrograph of a pentacene-based OTFMT with a cPMMA gate dielectric and gold nanoparticles.

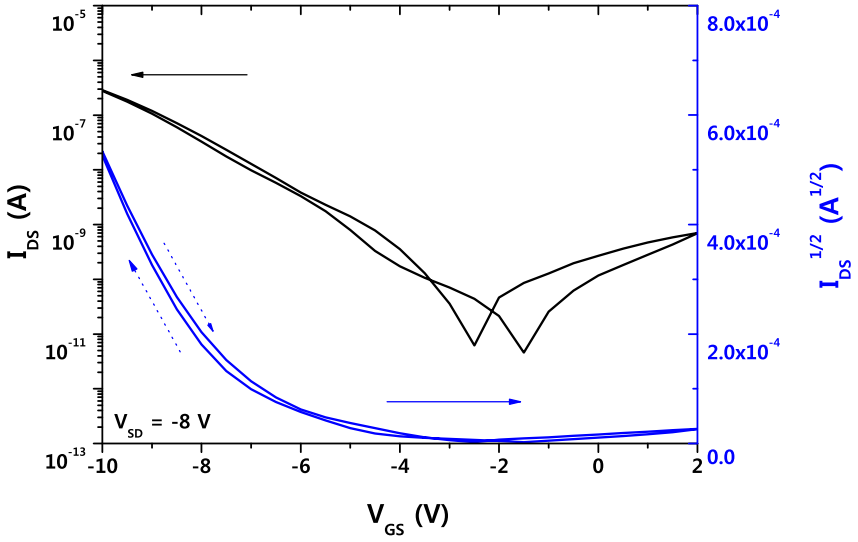
The output and transfer characteristics of a pentacene OTFMT with GNPs are shown in Figure 5.18 (device channel length = 100 μm, and width = 1000 μm). The device shows similar results to the 3.3 nm thick aluminium film; the magnitude of the drain-source current is almost the same giving consideration to the channel dimensions. However, the memory window of the device with GNPs was smaller than for the 3.3 nm thick aluminium film. Furthermore, the device shows very unstable behaviour due to cracks in the cPMMA.

5.6 Conclusions

Ion-beam radiation was used to cross-link PMMA and the resulting thin film was used as the gate dielectric in pentacene-based field effect transistors. A high-performance device, possessing a field-effect mobility of over 1 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of around -1 V, an on/off current ratio over 1.0×10^6, and a sub-threshold



(a)



(b)

Figure 5.18: (a) Output and (b) transfer characteristics of a pentacene-based memory transistor using a 43 nm cross-linked PMMA film as the gate dielectric with gold nanoparticles as charge traps. Forward and reverse voltage scans are shown for both sets of data. Device channel length = 100 μm; channel width = 1000 μm.

slope of about 220 mV decade^{-1} was achieved. The cross-linking methodology using an ion beam may not seem to fit with the low-cost rationale for organic electronics

noted earlier in this thesis. However, the experiments reported here are feasibility studies and indicate that physical cross-linking of the PMMA gate dielectric can be used effectively to produce thin-film transistors with high carrier mobility and operating at low voltages. Other solutions, e.g. based on reactive ion etching, may prove to be more appropriate for manufacture.

Low voltage operating memory transistors based on various charge storage elements (thin aluminium film, thin silver film and gold nanoparticles) with cPMMA as the gate dielectric have been demonstrated. Among these, OTFMTs with a 3.3 nm thick aluminium film as the charge trapping layer show some promise as a low voltage operating memory device. It is interesting to note that the OTFT with the 20 nm thick cPMMA without any metallic nanoparticles shows a relatively large amount of hysteresis (i.e. Figure 5.9). Further work may reveal if such a device can be usefully exploited as a memory. Although more research remains, such as investigation of the charge/discharge and charge retention properties of the OTFMT, the results shown here demonstrate the feasibility of a low voltage operating memory device based on cPMMA.

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Chapter 6

Solution-Processed Organic Thin-Film Transistors

6.1 Introduction

Organic thin-film transistors (OTFTs) based on vapour deposited pentacene have been widely used because of their relatively high field-effect mobility. However, for low-cost and large-area electronics, OTFTs should be processed by solution-based techniques such as spin-coating, inkjet-printing or roll-to-roll processes. For this reason, pentacene derivatives with soluble side groups have been synthesised. For example, bulky solubilising triisopropylsilylethynyl groups have been substituted at the 6,13-positions of the pentacene molecule to form 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene. This material has good solubility and a π-stacking structure, which potentially increases the charge carrier mobility.

In this chapter, solution-processed OTFTs based on TIPS pentacene have been studied. For the deposition of TIPS pentacene, spin-coating has been explored. The resulting thin films have been used with both poly(methyl methacrylate) (PMMA) and cross-linked PMMA (cPMMA) gate dielectrics. Well ordered layers of TIPS pentacene on PMMA and cPMMA have been produced. The results suggest that cPMMA layers can be used as the basis of solution-processed TIPS pentacene transistors operating at low voltage.

6.2 Experiments

Bottom-gate, top-contact OTFTs were fabricated. Glass slides were used as substrates after cleaning sequentially in an ultrasonic bath with acetone, isopropanol and deionised water. An aluminium gate, thickness 40 nm, was defined by thermal

evaporation through a shadow mask. A 4.8 wt% (for 150 nm thick PMMA gate dielectric) and 2.4 wt% (for 30 nm thick cPMMA gate dielectric) anisole (methoxybenzene - obtained from MicroChem) solution of PMMA (M_w = 93,000, obtained from Sigma-Aldrich) was spin-coated at 3000 rpm spinning speed for 50 seconds on the Al and cured for 1 hour at 120 °C. In the case of the 30 nm thick cPMMA gate dielectric, irradiation was undertaken using a 1.515 MeV $^4He^+$ ion beam to achieve a high LET (220 eV nm^{-1}) and effective cross-linking as addressed in section 5.2. Prior to depositing TIPS pentacene, the PMMA gate dielectric surface was treated with 2 % dimethyldichlorosilane (DMDCS) solution in 1,1,1-trichloroethane (BDH Laboratory) by exposing the film to DMDCS vapour for a period of 5 minutes and carefully rinsing in isopropanol to remove any excess DMDCS. PMMA is considered to be a hydrophilic polymer, with a water contact angle of ∼68° [1], even though PMMA contains nonpolar radical groups. However, a hydrophobic PMMA film can be obtained by DMDCS treatment, giving a water contact angle of ∼96° [2]. To form the active layer, a 3.5 wt % 1,2,3,4-tetrahydronaphthalene (tetralin - obtained from Sigma-Aldrich) solution of TIPS pentacene (Flexink) was spin-coated at 1000 rpm spinning speed for 110 seconds and dried in a solvent-rich ambient. Finally, a further shadow mask was used to define the source and drain contacts, formed by the thermal evaporation of 80 nm of gold.

6.3 Device Characteristics

6.3.1 Poly(methyl methacrylate) Gate Dielectric

Figure 6.1 shows a polarised optical micrograph of a spin-coated TIPS pentacene transistor on DMDCS treated PMMA with the bottom-gate, bottom-contact configuration in which the contacts are defined before the deposition of the organic semiconductor (device channel length = 50 μm, and width = 500 μm). The crystals of TIPS pentacene can be seen more clearly by using polarised light microscopy, which reveals large needle-shaped grains and a high degree of molecular ordering. This may be attributed to the high boiling point of tetralin (207 °C) which allows slow drying of the solution [3–5] and low spin speeds (1000 rpm) [3]. Significantly,

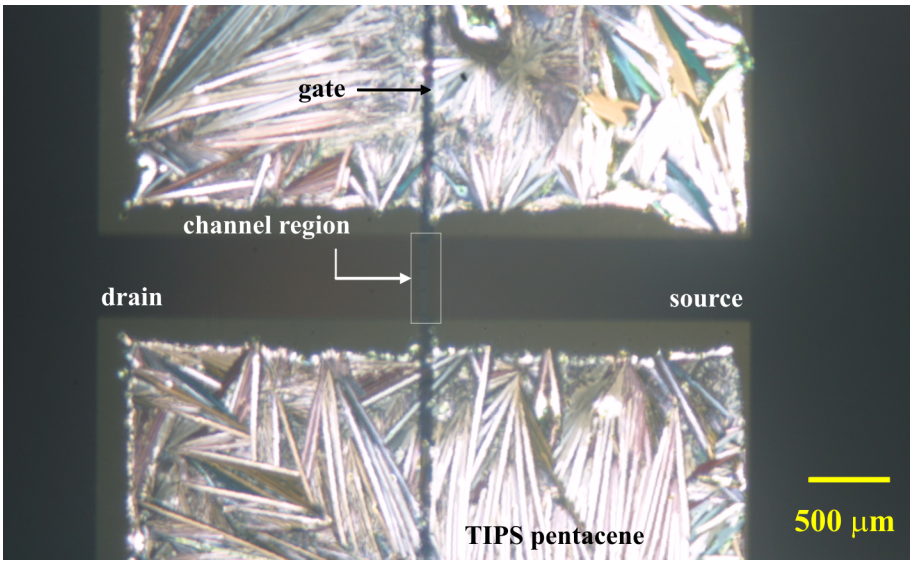
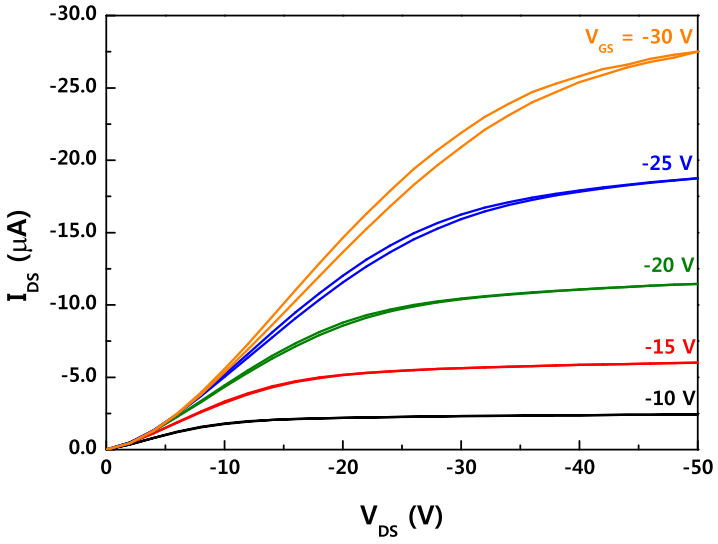


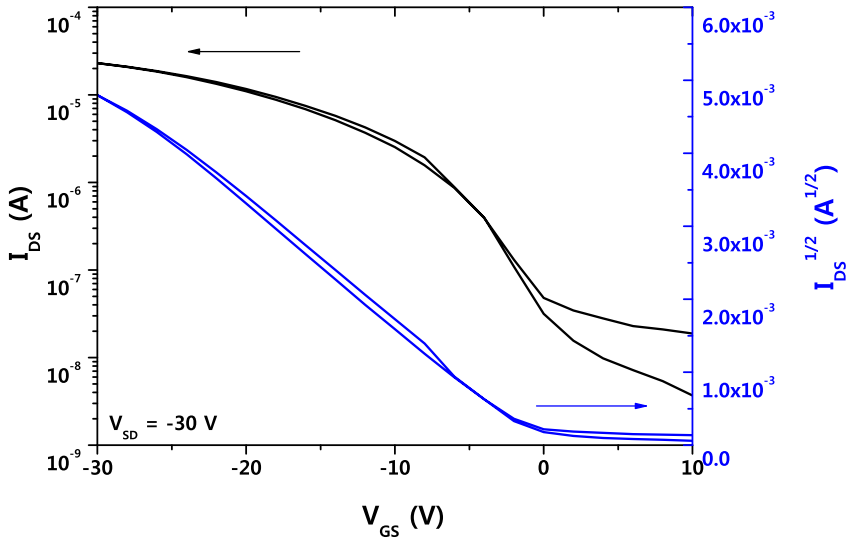
Figure 6.1: Polarised optical micrograph of spin-coated TIPS pentacene on dimethyldichlorosilane (DMDCS) treated PMMA gate dielectric with bottom-gate, bottom-contact configuration.

no crystals are deposited around the source/drain contacts. The source and drain contacts may prevent the spreading of TIPS pentacene into the channel region due to the poor metal/organic contact. It has been reported that the use of self-assembled monolayers (SAMs) of pentafluorobenzenethiol (PFBT) improves the metal/organic contact [3, 6, 7]. However, the bottom-gate, top-contact configuration of the OTFT, in which the source and drain contacts are defined after the deposition of the organic semiconductor, was used in this thesis for the lower contact resistance [8].

The output and transfer characteristics for a spin-coated TIPS pentacene transistor of bottom-gate, top-contact configuration with a 150 nm PMMA gate dielectric, treated by DMDCS, are shown in Figure 6.2 (device channel length = 50 μm and width = 1000 μm). The output characteristics plotted in Figure 6.2(a) show the drain current, I_{DS}, as a function of source-drain voltage, V_{DS}, for different values of gate voltage, V_{GS}. The non-linear behaviour in the lower bias region (< -5 V) is probably related to the poor spin-coated TIPS pentacene morphology. This rough surface may lead to Schottky-like contacts formed at the source/drain electrodes. The transfer characteristics, Figure 6.2(b), are measured at V_{DS} = -30 V. Plots are given in the form of both $\log(I_{DS})$ versus V_{GS} and $(I_{DS(sat)})^{1/2}$ versus V_{GS}. The on/off current ratio, threshold voltage, V_T, and sub-threshold slope for the device



(a)



(b)

Figure 6.2: (a) Output and (b) transfer characteristics of a spin-coated TIPS pentacene transistor using 150 nm PMMA as the gate dielectric with DMDCS treatment. Forward and reverse voltage scans are shown for both sets of data. Device channel length = 50 μm; channel width = 1000 μm.

were 1.2×10^3, -1 V, and 4.5 V decade^{-1}. The field-effect mobility, μ_{sat}, was estimated in the saturation region of the transistor, using Equation 2.11, i.e. from a plot of $(I_{DS(sat)})^{1/2}$ versus V_{GS}. Using the data from Figure 6.2(b) provided a mobility

of 0.13 cm^2 V^{-1} s^{-1}. These values compare favourably with data from evaporated pentacene/PMMA OTFTs (section 4.6). However, the device possessed a low on/off current ratio resulting from the relatively large off-current ($\sim 10^{-8}$ A evident in the transfer characteristics). This may be attributed to the fact that the active layer cannot be patterned in spin-coated devices [4]. The surface currents, which flow through the un-patterned active layer due to the fringe field between source and drain electrodes, give increased off-currents in these devices [9].

6.3.2 Cross-linked Poly(methyl methacrylate) Gate Dielectric

Figure 6.3 shows an optical micrograph for spin-coated TIPS pentacene on both DMDCS treated PMMA and cPMMA. This micrograph clearly shows crystals of TIPS pentacene on the PMMA, whereas no crystals are obtained on the cPMMA (area irradiated by the ion beam along the gate electrode). This can be explained by the fact that the reactive sites on the cPMMA surface, which would make assemblies with DMDCS, are much less than that of the uncross-linked PMMA surface. Therefore, it is less likely that DMDCS will directly attach to the cPMMA surface.

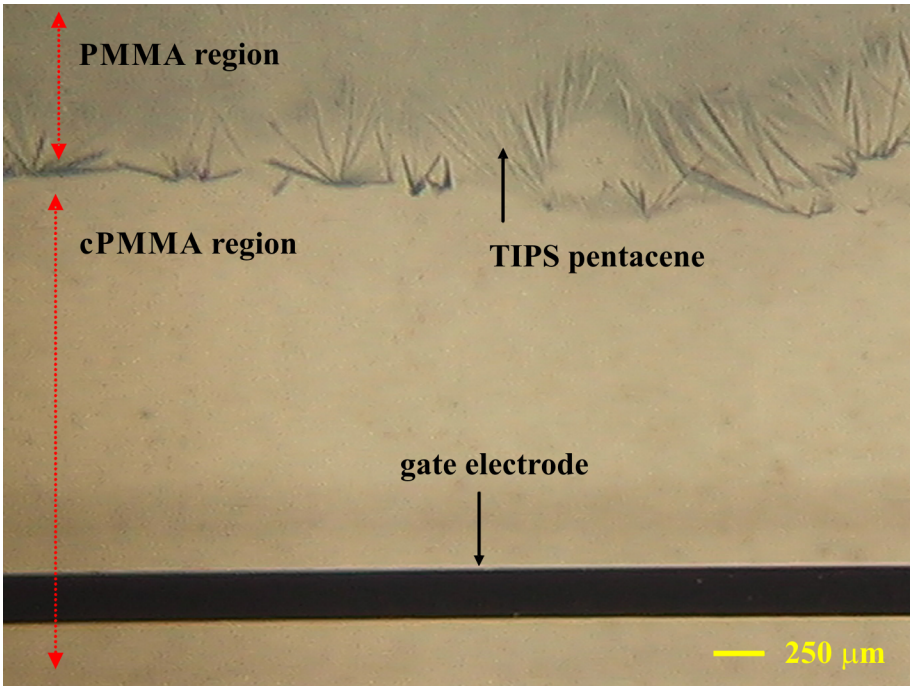


Figure 6.3: Optical micrograph of spin-coated TIPS pentacene on a DMDCS treated PMMA and cPMMA gate dielectric.

It was therefore decided to use a thin layer of PMMA as a buffer to improve the spreading of the TIPS pentacene. To form the buffer layer, a 1.64 wt % anisole solution of PMMA was spin-coated on top of the cPMMA at 3000 rpm spinning speed for 50 seconds and baked for 30 minutes at 120 °C; this resulted in a 50 nm thick layer. Then, the buffer layer was treated using the same processes as described in section 6.2. Figure 6.4 shows large grains and a high degree of molecular ordering of TIPS pentacene on the treated buffer layer.

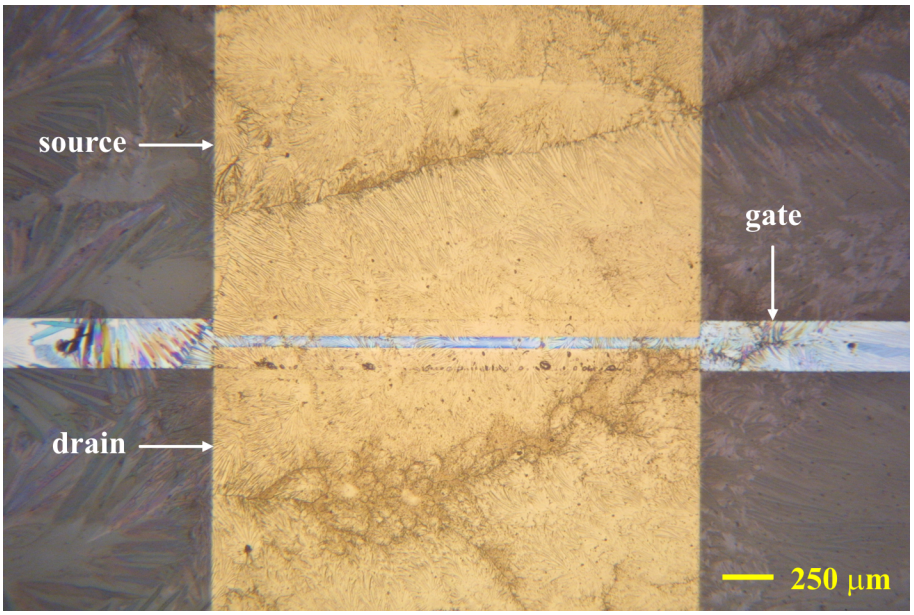
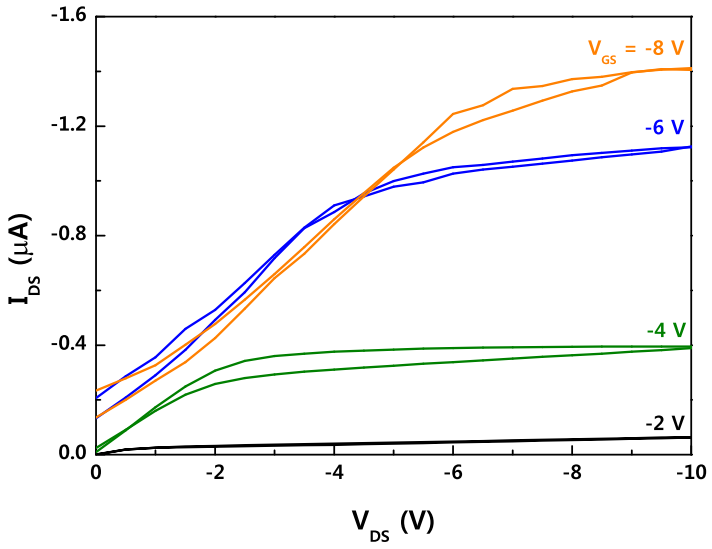
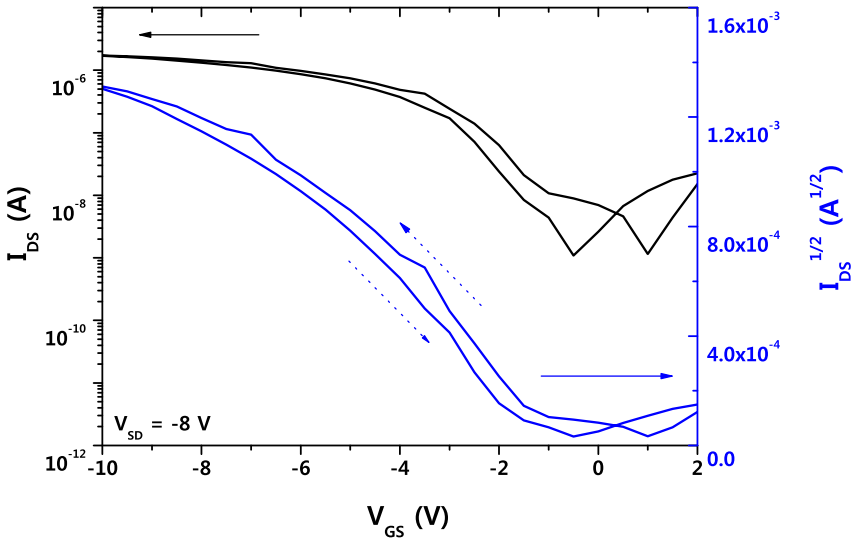


Figure 6.4: Polarised optical micrograph of spin-coated TIPS pentacene on a cPMMA gate dielectric with a DMDCS treated PMMA buffer layer.

The output and transfer characteristics of a spin-coated TIPS pentacene OTFT with a 33 nm cPMMA gate insulator and a 50 nm PMMA buffer layer treated with DMDCS are shown in Figure 6.5; device channel length (L) = 200 μm, channel width (W) = 2000 μm. In each case, the forward and reverse voltage scans are shown. The output characteristics (Figure 6.5(a)) exhibit a small amount of hysteresis and large off-state currents. The increase in I_{DS} with increasing V_{GS} at V_{DS} = 0 V may result from the cPMMA being affected during spin-coating of the TIPS pentacene. The results are clearly different from those in Figure 5.6; here, no drain offset current was observed because free dangling bonds or unpaired radicals are likely to be distributed in the bulk of cPMMA film, as illustrated in Figure 6.6(a).



(a)



(b)

Figure 6.5: (a) Output and (b) transfer characteristics of a spin-coated TIPS pentacene transistor using cPMMA gate dielectric and PMMA buffer layer with DMDCS treatment. Forward and reverse voltage scans are shown for both sets of data. Device channel length = 200 μm; channel width = 2000 μm.

However, in the case of the spin-coated device, such defects in the cPMMA layer may make direct contact with the TIPS pentacene layer at the channel interface through the thin PMMA buffer layer (Figure 6.6(b)). These will produce residual

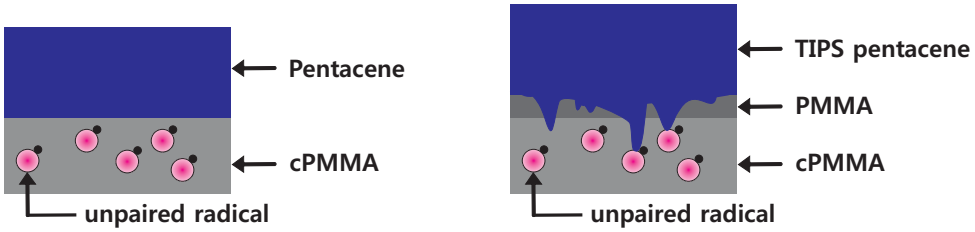


Figure 6.6: Diagrams of (a) a thermally evaporated pentacene/cPMMA and (b) a spin-coated TIPS pentacene/PMMA/cPMMA interface.

holes in the conduction channel during continuous operation of the OTFT, resulting in an increase of the drain-offset current. Nevertheless, the device operates at relatively low voltages, < 10 V and shows transistor behaviour. Figure 6.5(b) shows the transfer characteristics of the device, measured at V_{DS} = -8 V. Plots are given in the form of both $\log(I_{DS})$ versus the gate-source voltage (V_{GS}), and $(I_{DS(sat)})^{1/2}$ versus V_{GS}. The on/off current ratio, field-effect mobility, threshold voltage, and subthreshold slope for this device were: 1.56×10^3, 0.15 cm^2 V^{-1} s^{-1}, -1.0 V and 1.2 V per decade. The field-effect mobility is significantly smaller, by one order of magnitude, than that measured for a thermally evaporated pentacene transistor with a cPMMA gate dielectric. However, the results shown here demonstrate the potential for a solution-processed low voltage transistor with a cPMMA gate dielectric.

6.4 Conclusions

Spin-coating was used for the deposition of TIPS pentacene. Using a high boiling point solvent and low spin speeds, TIPS pentacene films showed good crystallinity. The performance of a spin-coated device with a PMMA gate dielectric was comparable to that of a thermally evaporated pentacene transistor. However, the performance of spin-coated TIPS pentacene devices with cPMMA gate dielectrics were not as good as evaporated pentacene devices even though they showed low voltage operation. Although further work remains, such as the development of a high performance solution-processed device, the results shown here demonstrate that TIPS pentacene/cPMMA transistors may be used to make low cost and low voltage electronic circuits.

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Chapter 7

Conclusions and Suggestions for Further Work

7.1 Conclusions

The aim of this thesis was to characterise pentacene-based organic electronic devices with poly(methyl methacrylate) (PMMA) and cross-linked PMMA (cPMMA) gate dielectrics.

Pentacene is one of the most promising organic semiconductors because of its high field-effect mobility. For this reason, pentacene was used as the active layer in organic thin-film transistors (OTFTs). PMMA was used as the gate dielectric because it has high resistivity and low dielectric constant (similar to that of silicon dioxide). Furthermore, it contains hydrophobic methyl radical groups, encouraging good ordering of the active organic overlayer as it is deposited on the surface.

Uniform, pinhole-free and crack-free films of PMMA could be obtained by spin-coating with a lower limit to the thickness of about 150 nm. The leakage current density was found to be less than 10^{-6} A cm^{-2} for fields up to 2 MV cm^{-1}. This is sufficiently small to allow the use of a 150 nm PMMA film as the gate dielectric in an OTFT. The dielectric constant of the PMMA was measured to be 3.66±0.10 at 1 kHz and 2.89±0.10 at 1 MHz. OTFTs incorporating a 150 nm layer of PMMA were optimised. Leakage currents could be reduced significantly by patterning of the pentacene layer. Scaling effects of the OTFT characteristics with respect to the channel length and width were found to agree with simple thin film transistor theory. The on/off current ratio, field-effect mobility, threshold voltage, and subthreshold slope for an optimised device were measured to be 1.2×10^6, 0.33 cm^2 V^{-1} s^{-1}, -11 V and 1.5 V per decade, thus demonstrating that PMMA has the potential to be

used as a dielectric.

The operation of two different inverter circuits based on evaporated pentacene/ PMMA OTFTs - a simple diode-connected load inverter and a bootstrapped inverter - were designed, fabricated and tested. The simple diode-connected load inverter showed that the dynamic switching characteristics were not fully pulled up or pulled down to the voltage rail because of the high threshold voltage of the load transistor. A significant improvement in performance was achieved with a bootstrapped circuit, using capacitive coupling and bootstrapping effects. This exhibited an operating frequency of 1 kHz with a 30 V drive voltage.

A physical cross-linking method was used to reduce the dielectric thickness, and thereby lower the OTFT operating voltage. Ion-beam irradiation of a 57 nm thick spin-coated PMMA layer resulted in a 33 nm thick cross-linked layer of PMMA. The leakage current density of the cPMMA was found to be similar to that of uncross-linked PMMA, less than 10^{-6} A cm^{-2} for fields up to 2 MV cm^{-1}. The dielectric constant of the cPMMA layer (3.90 $\pm$ 0.10 at 1 kHz and 2.89 $\pm$ 0.10 at 1 MHz) was also similar to the value measured for PMMA. A high performance OTFT incorporating a 33 nm thick layer of cPMMA, which possessed a field-effect mobility of 1.1 cm^2 V^{-1} s^{-1}, was achieved, with minimal hysteresis. Moreover, the operating voltage of the devices could be reduced to below -10 V due to the reduced thickness of the dielectric. The on/off current ratio, threshold voltage, V_T, and sub-threshold slope for the device were 1.1×10^6, -0.9 V, and 219 mV decade^{-1}. The relationship between the saturated field-effect mobility and the thickness of the gate insulator was found to be of the form of $\mu_{sat} \propto d^{-1}$. However, the thinnest cPMMA layers were 30 nm, limited by the quality of the PMMA.

Low voltage operating memory transistors based on various charge storage elements with cPMMA as the gate dielectric were demonstrated. Thin aluminium and silver layers and gold nanoparticles were explored as charge traps, and cPMMA, which enables low operating voltage devices, was used as the blocking dielectric. Among these configurations, organic thin-film memory transistors (OTFMTs) with a 3.3 nm thick aluminium film as the charge trapping layer showed some promise as low voltage operating memory devices.

Finally, solution-processed OTFTs based on 6,13-bis(triisopropyl-silylethynyl) (TIPS) pentacene were investigated. Spin-coating was used to deposit TIPS pentacene and PMMA and cPMMA were used as the gate dielectric. The use of a high boiling point solvent and low spin speeds produce TIPS pentacene films showing a good crystallinity. Spin-coated TIPS pentacene devices with a PMMA gate dielectric showed a field-effect mobility of 0.13 $cm^2\ V^{-1}\ s^{-1}$. The field-effect mobilities of spin-coated TIPS pentacene devices with cPMMA gate dielectrics were measured to be 0.15 $cm^2\ V^{-1}\ s^{-1}$.

7.2 Suggestions for Further Work

The research presented in this thesis has focused on thermally evaporated pentacene OTFTs with a spin-coated PMMA gate dielectric for hysteresis-free devices, thermally evaporated pentacene OTFTs with physically cross-linked PMMA gate dielectrics for low voltage operating devices and spin-coated TIPS pentacene OTFTs with PMMA and cPMMA gate dielectrics for low-cost organic electronics.

Further work might take two distinct directions. First, the use of ion-beam irradiation to produce ultra-thin cross-linked layers of PMMA may not seem to fit with low-cost organic electronics. Other solutions, e.g. based on reactive ion etching (RIE), may be more appropriate for manufacture. However, this can be achieved only when the LET value is around 15 eV nm^{-1} and the spur distance is about 2 nm for an LET value of 15 eV nm^{-1} [3]. On a second front, an improvement in the quality of the cPMMA is needed. Free dangling bonds or unpaired radical which cannot be cross-linked during irradiation can degrade the performance, in particular, of the solution-processed devices [1]. This might be improved by the use of the TIPS pentacene and a PMMA blend. The blend separates during spinning to produce a bilayer in which the PMMA layer is located under the TIPS pentacene layer [2].

For low voltage operating memory transistors, a 3.3 nm thick aluminium film as a charge trapping layer shows some promise. This could offer an advantage over gold nanoparticles from the viewpoints of cost of manufacture and process complexity. However, the memory window of the device was very small, even though the device operated at relatively low voltages. This might be improved by the use of

an oxygen plasma [4, 5] or an UV ozone [6] treatment, which will increase the electron affinity of the aluminium film. Further work involving an investigation into the charge/discharge and charge retention properties [7, 8] is also needed. The OTFT with a 20 nm thick cPMMA gate dielectric layer, but without any metallic nanoparticles, showed a relatively large amount of hysteresis due to free dangling bonds or unpaired radical in the cPMMA. Therefore, it is also important to determine whether such a device can be usefully exploited as a memory.

It is important to control the surface energy of a gate dielectric with respect to the polar nature of TIPS pentacene for solution-processed devices. This will allow simple processes, such as spin-coating or inkjet-printing for low-cost manufacture. However, there are still open issues on the choice of solvents for TIPS pentacene as well as additional treatments for the cPMMA gate dielectric. Such investigations will be needed to improve the electrical characteristics of solution-processed OTFTs, i.e. the on/off current ratio, by suppressing the physical damage to the cPMMA layer.

Overall, there is a very large amount of work required to expedite the practical application of OTFTs for the next generation of electronics. Low-power consumption and low-cost manufacture are key elements for the development of portable electronics. The approaches presented in this thesis primarily concern device fabrication and optimisation. Physically cross-linked PMMA gate dielectrics can contribute to reducing the operating voltage. Solution-processed devices with a cPMMA gate dielectric show some promise for low-cost electronics operating at reduced voltages.

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Appendices

A.1 SPICE simulation

A.1.1 Amorphous-Si TFT Model ASIA2 (level 15) [1]

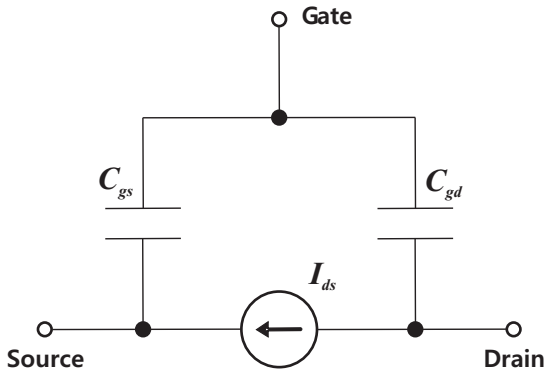

Figure A.1: An equivalent circuit of amorphous-Si TFT.

Drain Current Equations

$$I_{ds} = I_{leakage} + I_{ab} \tag{A.1.1}$$

$$I_{ab} = g_{ch} V_{dse} \left(1 + \mathrm{LAMDA} \cdot V_{ds}\right) \tag{A.1.2}$$

$$V_{dse} = \frac{V_{ds}}{\left[1 + \left(V_{ds}/V_{sate}\right)^{M}\right]^{1/M}} \tag{A.1.3}$$

$$V_{sate} = \alpha_{sat} V_{gte} \tag{A.1.4}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}\left(\mathrm{RS} + \mathrm{RD}\right)} \tag{A.1.5}$$

$$g_{chi} = q n_s \mathrm{W} \cdot \mathrm{MUBAND/L} \tag{A.1.6}$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}} \tag{A.1.7}$$

$$n_{sa} = \frac{\mathrm{EPSI} \cdot V_{gte}}{q \cdot \mathrm{TOX}} \left(\frac{V_{gte}}{V_{aat}} \right)^{\mathrm{GAMMA}} \tag{A.1.8}$$

$$n_{sb} = n_{so} \left(\frac{t_m}{\mathrm{TOX}} \frac{V_{gfbe}}{\mathrm{V0}} \frac{\mathrm{EPSI}}{\mathrm{EPS}} \right)^{\frac{2 \cdot \mathrm{V0}}{V_e}} \tag{A.1.9}$$

$$n_{so} = N_c t_m \frac{V_e}{\mathrm{V0}} \exp\left(-\frac{\mathrm{DEF0}}{V_{th}} \right) \tag{A.1.10}$$

$$N_c = 3.0 \cdot 10^{25} \mathrm{m}^{-3} \tag{A.1.11}$$

$$V_e = \frac{2 \cdot \mathrm{V0} \cdot V_{tho}}{2 \cdot \mathrm{V0} - V_{th}} \tag{A.1.12}$$

$$t_m = \sqrt{\frac{\mathrm{EPS}}{2q \cdot \mathrm{GMIN}}} \tag{A.1.13}$$

$$V_{gte} = \frac{\mathrm{VMIN}}{2} \left[1 + \frac{V_{gt}}{\mathrm{VMIN}} + \sqrt{\mathrm{DELTA}^2 + \left(\frac{V_{gt}}{\mathrm{VMIN}} - 1 \right)^2} \right] \tag{A.1.14}$$

$$V_{gt} = V_{gs} - V_T \tag{A.1.15}$$

$$V_{gfbe} = \frac{\mathrm{VMIN}}{2} \left[1 + \frac{V_{gfb}}{\mathrm{VMIN}} + \sqrt{\mathrm{DELTA}^2 + \left(\frac{V_{gfb}}{\mathrm{VMIN}} - 1 \right)^2} \right] \tag{A.1.16}$$

$$V_{gfb} = V_{gs} - \mathrm{VFB} \tag{A.1.17}$$

$$I_{leakage} = I_{hl} + I_{min} \tag{A.1.18}$$

$$I_{hl} = \mathrm{IOL} \left[\exp\left(\frac{V_{ds}}{\mathrm{VDSL}} \right) - 1 \right] \exp\left(\frac{V_{gs}}{\mathrm{VGSL}} \right) \exp\left[\frac{\mathrm{EL}}{q} \left(\frac{1}{V_{tho}} - \frac{1}{V_{th}} \right) \right] \tag{A.1.19}$$

$$I_{min} = \text{SIGMA0} \cdot V_{ds} \tag{A.1.20}$$

Temperature Dependence

$$V_{tho} = k_B \cdot \text{TNOM}/q \tag{A.1.21}$$

$$V_{th} = k_B \cdot \text{TEMP}/q \tag{A.1.22}$$

$$V_{aat} = \text{VAAexp}\left[\frac{\text{EMU}}{q \cdot \text{GAMMA}}\left(\frac{1}{V_{th}} - \frac{1}{V_{tho}}\right)\right] \tag{A.1.23}$$

$$V_T = \text{VTO} + \text{KVT}(\text{TEMP} - \text{TNOM}) \tag{A.1.24}$$

$$\alpha_{sat} = \text{ALPHASAT} + \text{KASAT}(\text{TEMP} - \text{TNOM}) \tag{A.1.25}$$

Capacitance Equations

$$C_{gs} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}}\right)^2\right] \tag{A.1.26}$$

$$C_{gd} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}}\right)^2\right] \tag{A.1.27}$$

$$C_f = 0.5 \cdot \text{EPS} \cdot \text{W} \tag{A.1.28}$$

$$C_{gc} = q\frac{dn_{sc}}{dV_{gs}} \tag{A.1.29}$$

$$nsc = \frac{n_{sac}n_{sbc}}{n_{sac} + n_{sbc}} \tag{A.1.30}$$

$$nsac = \frac{\text{EPSI} \cdot V_{gte}}{q \cdot \text{TOX}} \tag{A.1.31}$$

$$nsbc = n_{sb} \tag{A.1.32}$$

Table A.1: Amorphous-Si TFT Model ASIA2 Parameters (level 15).

Name	Parameter	Units	Default
ALPHASAT	Saturation modulation parameter	-	0.6
CGDO	Gate-drain overlap capacitance per meter channel width	F m^{-1}	0.0
CGSO	Gate-source overlap capacitance per meter channel width	F m^{-1}	0.0
DEF0	Dark Fermi level position	eV	0.6
DELTA	Transition width parameter	-	5
EL	Activation energy of the hole leakage current	eV	0.06
EMU	Field effect mobility activation energy	eV	0.35
EPS	Relative dielectric constant of substrate	-	11
EPSI	Relative dielectric constant of gate insulator	-	7.4
GAMMA	Power law mobility parameter	-	0.4
GMIN	Minimum density of deep states	m^{-3} eV^{-1}	1E23
IOL	Zero bias leakage current	A	3E-14
KASAT	Temperature coefficient of ALPHASAT	$°C^{-1}$	-0.036
KVT	Threshold voltage temperature coefficient	V $°C^{-1}$	-0.036
LAMBDA	Output conductance parameter	V^{-1}	0.0008
M	Knee shape parameter	-	2.5
MUBAND	Conduction band mobility	m^2 V^{-1} s^{-1}	0.001
RD	Drain resistance	Ω	0.0
RS	Source resistance	Ω	0.0
SIGMA0	Minimum leakage current parameter	A	1E-14
TNOM	Parameter measurement temperature	°C	27
TOX	Thin-oxide thickness	m	1.0e-7
V0	Characteristics voltage for deep states	V	0.12
VAA	Characteristics voltage for field effect mobility (determined by tail states)	V	7.5E3
VDSL	Hole leakage current drain voltage parameter	V	7
VFB	Flat band voltaage	V	-3
VGSL	Hole leakage current gate voltage parameter	V	7
VMIN	Convergence parameter	V	0.3
VTO	Zero-bias threshold voltage	V	0.0

A.1.2 SPICE code

Diode-Connected Inverter

DIODE-CONNECTED INVERTER

VDD NGND 0 DC 15V
VSS NVDD 0 DC -15V
VIN NIN 0 PULSE(-15V 15V 0 500n 500n 499u 1000u)

MP1 NOUT NIN NGND 0 PEN L=50u W=4000u
MP2 NVDD NVDD NOUT 0 PEN L=50u W=500u

.MODEL PEN PMOS LEVEL=15 ALPHASAT=0.55 DEFO=0.6 DELTA=5 EMU=0.02 EL=0.1 EPS=11 EPSI=3.5 GAMMA=0.97 GMIN=1E+023 IOL=3E-012 KVT=-0.01 LAMBDA=1E-015 M=5.5 MUBAND=0.003 RD=7000 RS=7000 SIGMAO=1E-014 TNOM=27 TOX=1.5E-007 VAA=8000 VDSL=5 VFB=-20 VGSL=7 VMIN=0.3 VO=0.1 VTO=-1 CGSO=5.16E-09 CGDO=5.16E-09

.TRAN 10n 10m 0 uic

Bootstrapped Inverter

BOOTSTRAPPED INVERTER

VDD NGND 0 DC 15V
VSS NVDD 0 DC -15V
VIN NIN 0 PULSE(-15V 15V 0 500n 500n 499u 1000u)

MP1 NOUT NIN NGND 0 PEN L=50u W=4000u
MP2 NVDD NA NOUT 0 PEN L=50u W=2000u
MP3 NA NIN NGND 0 PEN L=50u W=2000u
MP4 NVDD NVDD NA 0 PEN L=50u W=500u

.MODEL PEN PMOS LEVEL=15 ALPHASAT=0.55 DEFO=0.6 DELTA=5 EMU=0.02 EL=0.1 EPS=11 EPSI=3.5 GAMMA=0.97 GMIN=1E+023 IOL=3E-012 KVT=-0.01 LAMBDA=1E-015 M=5.5 MUBAND=0.003 RD=7000 RS=7000 SIGMAO=1E-014 TNOM=27 TOX=1.5E-007 VAA=8000 VDSL=5 VFB=-20 VGSL=7 VMIN=0.3 VO=0.1 VTO=-1 CGSO=5.16E-09 CGDO=5.16E-09

.TRAN 10n 10m 0 uic

A.2 SRIM Calculated Results

Table A.2: SRIM calculated results with helium ion source and a PMMA density of 1.20 g cm^{-3}. Stopping Units = MeV $(mg\ cm^{-2})^{-1}$.

Ion Energy [keV]	dE/dx (Electronic)	dE/dx (Nuclear)	Projected Range [nm]	Longitudinal Straggling [nm]	Lateral Straggling [nm]
10.00	4.251E-01	8.594E-02	146.9	48.3	43.8
11.00	4.462E-01	8.122E-02	160.4	51.0	46.8
12.00	4.664E-01	7.707E-02	173.6	53.4	49.6
13.00	4.858E-01	7.338E-02	186.5	55.6	52.3
14.00	5.044E-01	7.008E-02	199.2	57.7	54.8
15.00	5.225E-01	6.710E-02	211.6	59.7	57.2
16.00	5.399E-01	6.440E-02	223.9	61.5	59.6
17.00	5.568E-01	6.194E-02	235.8	63.2	61.8
18.00	5.733E-01	5.968E-02	247.6	64.9	63.9
20.00	6.048E-01	5.569E-02	270.6	67.9	67.8
22.50	6.419E-01	5.148E-02	298.4	71.2	72.4
25.00	6.767E-01	4.794E-02	325.1	74.2	76.5
27.50	7.096E-01	4.491E-02	350.9	76.8	80.3
30.00	7.406E-01	4.228E-02	376.0	79.2	83.8
32.50	7.700E-01	3.997E-02	400.3	81.3	87.1
35.00	7.978E-01	3.794E-02	423.9	83.3	90.1
37.50	8.242E-01	3.612E-02	446.9	85.1	93.0
40.00	8.493E-01	3.449E-02	469.4	86.8	95.6
45.00	8.961E-01	3.167E-02	512.9	89.8	100.5
50.00	9.390E-01	2.933E-02	554.7	92.5	104.9
55.00	9.789E-01	2.734E-02	595.1	94.9	109.0
60.00	1.017E+00	2.563E-02	634.1	97.1	112.6
65.00	1.052E+00	2.414E-02	672.0	99.0	116.0

Ion Energy	dE/dx	dE/dx	Projected Range	Longitudinal Straggling	Lateral Straggling
70.00	1.087E+00	2.283E-02	708.8	100.8	119.2
80.00	1.153E+00	2.063E-02	779.5	104.1	124.8
90.00	1.216E+00	1.886E-02	846.8	106.9	129.8
100.00	1.276E+00	1.739E-02	911.1	109.3	134.2
110.00	1.333E+00	1.615E-02	972.8	111.5	138.2
120.00	1.387E+00	1.509E-02	1030	113.4	141.8
130.00	1.439E+00	1.417E-02	1090	115.1	145.1
140.00	1.488E+00	1.337E-02	1140	116.6	148.2
150.00	1.535E+00	1.266E-02	1200	118.1	151.0
160.00	1.579E+00	1.203E-02	1250	119.3	153.6
170.00	1.621E+00	1.146E-02	1300	120.5	156.0
180.00	1.662E+00	1.095E-02	1350	121.6	158.3
200.00	1.736E+00	1.006E-02	1450	124.0	162.5
225.00	1.819E+00	9.151E-03	1560	126.8	167.1
250.00	1.892E+00	8.402E-03	1670	129.2	171.2
275.00	1.957E+00	7.776E-03	1780	131.4	174.9
300.00	2.013E+00	7.242E-03	1890	133.4	178.2
325.00	2.062E+00	6.783E-03	1990	135.2	181.3
350.00	2.105E+00	6.382E-03	2090	136.9	184.2
375.00	2.141E+00	6.029E-03	2180	138.5	186.8
400.00	2.172E+00	5.716E-03	2280	140.0	189.3
450.00	2.219E+00	5.184E-03	2470	143.9	194.0
500.00	2.250E+00	4.749E-03	2650	147.6	198.2
550.00	2.267E+00	4.386E-03	2840	151.1	202.2
600.00	2.273E+00	4.078E-03	3020	154.4	205.9
650.00	2.270E+00	3.813E-03	3200	157.6	209.4
700.00	2.260E+00	3.582E-03	3380	160.7	212.8

Ion Energy	dE/dx	dE/dx	Projected Range	Longitudinal Straggling	Lateral Straggling
800.00	2.225E+00	3.200E-03	3750	170.8	219.3
900.00	2.177E+00	2.896E-03	4130	180.6	225.5
1000.00	2.122E+00	2.648E-03	4520	190.3	231.6
1100.00	2.064E+00	2.441E-03	4920	200.0	237.6
1200.00	2.005E+00	2.267E-03	5320	209.7	243.5
1300.00	1.947E+00	2.116E-03	5750	219.4	249.5
1400.00	1.891E+00	1.986E-03	6180	229.3	255.6
1500.00	1.838E+00	1.872E-03	6620	239.3	261.7
1520.00	1.830E+00	1.856E-03	6690	239.7	262.6

Table A.3: Table for other Stopping Units.

Multiply Stopping by	for Stopping Units
1.2000E+01	eV Å $^{-1}$
1.2000E+02	keV μm^{-1}
1.2000E+02	MeV mm^{-1}
1.0000E+00	keV (μg cm^{-2})$^{-1}$
1.0000E+00	MeV (mg cm^{-2})$^{-1}$
1.0000E+03	keV (mg cm^{-2})$^{-1}$
1.1083E+01	eV (1E15 atoms cm^{-2})$^{-1}$
9.6266E-01	L.S.S. reduced units

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