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Modeling and Validation of 4H-SiC Low Voltage MOSFETs for Integrated Circuit Design

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a Concentration in Electrical
Engineering

by

Shamim Ahmed
University of Arkansas
Master of Science in Electrical Engineering, 2015

May 2017
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This dissertation is approved for recommendation to the Graduate Council.

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Abstract

Silicon Carbide is a promising wide bandgap material and gradually becoming the first choice of semiconductor for high density and high efficiency power electronics in medium voltage range (500-1500V). SiC has also excellent thermal conductivity and the devices fabricated with the material can operate at high temperature (~ 400 ^{o} C). Thus, a power electronic system built with SiC devices requires less cooling requirement and saves board space and cost. The high temperature applications of SiC material can also be extended to space exploration, oil and gas rigging, aerospace and geothermal energy systems for data acquisition, sensing and instrumentation and power conditioning and conversion. But the high temperature capability of SiC can only be utilized when the integrated circuits can be designed in SiC technology and high fidelity compact models of the semiconductor devices are a *priori* for reliable and high yielding integrated circuit design.

The objective of this work is to develop industry standard compact models for SiC NMOS and PMOS devices. A widely used compact model used in silicon industry called BSIM3V3 is adopted as a foundation to build the model for SiC MOSFET. The models optimized with the built-in HSPICE BSIM3V3.3 were used for circuit design in one tape-out but BSIM3V3 was found to be inadequate to model all of the characteristics of SiC MOSFET due to the presence of interface trapped charge. In the second tape-out, the models for SiC NMOS and PMOS were optimized based on the built-in HSPICE BSIM4V6.5 and a number of functioning circuits which have been published in reputed journal and conference were designed based on the models. Although BSIM4 is an enhanced version of BSIM3V3, it also could not model a few deviant SiC MOSFET characteristics such as body effect, soft saturation etc. The new model developed for SiC NMOS and PMOS based on BSIM4V7.0 is called BSIM4SIC and can model the entire range of device

characteristics of the devices. The BSIM4SIC models are validated with a wide range of measured data and verified using the models in the simulation of numerous circuits such as op-amp, comparator, linear regulator, reference and ADC/DAC.

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Dedication

To my beloved parents and my little sister Shamima

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CHAPTER 1 INTRODUCTION

1.1 Motivation

In recent times, the 4H poly-type of SiC has already been proven as a very useful wide-band gap material for power semiconductor device fabrication. SiC power MOSFETs [1], Schottky diodes [2], Super Junction Bipolar Transistor (SJT) [3] are already being used in commercial applications such as motor drives [4], data centers [5], hybrid electrical vehicles [6] etc. Since SiC has a large band gap and higher critical electric field compared to Si [7], SiC power devices offer low on-resistance (10's of mΩ) even with a large blocking voltage (several kilovolts) and smaller device capacitances which allows high frequency operation. This in turn reduces the size of passives in a power electronics system and significantly increases power density and efficiency. Besides, SiC devices can be operated at very high temperature (up to 400°C) [8] as it has superior thermal conductivity and very low intrinsic carrier concentration at room temperature. Also, being a radiation-hard material, SiC shows promise in harsh environment electronics application [9]. But, until recently, SiC power devices have been commercialized only for their capability for high power density and high efficiency. The use of SiC devices in harsh environment applications such as space exploration, oil and gas, avionics, automobile and geo-thermal is still in the research and development phase mainly due to a lack of reliable high temperature (more than 300°C) operation and a matured low voltage CMOS process. In order to utilize SiC devices to their full merit in analog and mixed signal domain for sensing, conditioning, instrumentation and power conversion applications, the following are necessary:

- Reliable SiC power devices that can operate efficiently at more than 300°C. Currently commercial SiC devices cannot operate beyond 175°C.

- Matured and reliable low voltage SiC CMOS process with high quality SiC-SiO_2 interface with a smooth surface at the interface.
- Well-developed Process Design Kit (PDK) with accurate and predictive models of NMOS, PMOS, diode, BJT, resistors, capacitors and parasitics.
- High temperature packaging solution both for die and module.
- High temperature passives and PCB.

Development of low voltage SiC process began in 90's but until recently the process was limited to NMOS. Wolfspeed (formerly known as Cree) launched a 2 μm NMOS process in 2010 [10]. General Electric also has a SiC NMOS process [8]. Raytheon UK announced the world first SiC CMOS process in 2012 [11]. At the University of Arkansas, integrated circuits using Raytheon high temperature 1.2 μm SiC CMOS process were designed as a part of National Science Foundation project called Building Innovation Capacity (BIC). But since the process is still maturing and in the research and development phase, Raytheon does not have accurate device models in the process design kit (PDK). This serves as the motivation of developing accurate models for SiC MOSFETs which are of paramount importance in designing sensitive analog, mixed-signal and power integrated circuits.

1.2 Research Objectives

The objective of this research is to develop a geometry and temperature scalable compact model of 4H-SiC MOSFETs for integrated circuit design and simulation. The characteristics of SiC MOSFETs are significantly different than their Si counterparts primarily due to the presence of trap sites in the SiC-SiO_2 interface. Also, the interface is not as smooth as the Si-SiO_2 one. Surface roughness and trapped charge in the interface alter the MOSFET characteristics by altering the flat band voltage, threshold voltage, mobility, subthreshold slope, body effect, thermal and

geometry behavior. Also, the presence of slow traps influence the small and large signal dynamics and the gate capacitance becomes frequency dependent in the accumulation region. This poses significant challenges not only in developing a compact model for SiC MOSFETs but also in characterizing their static and dynamic behavior. The purpose of this research is threefold – 1) accurate DC and CV characterization of SiC MOSFETs, 2) development of an accurate model for interface trap related device characteristics and global temperature and geometry scaling and 3) development of an easy parameter extraction and optimization routine for model card generation.

1.3 Key Contributions

- Development of accurate DC and CV characterization methods at high temperature in the presence of non-ideal conditions i.e. probe station parasitics, cable leakage, cable inductance and capacitance, thermal current etc.
- Verilog-A version development of BSIM470 model.
- Modification of BSIM470 Verilog-A model for SiC MOSFETs.
- Comprehensive ICCAP module development for parameter extraction and optimization.
- Extraction of slow trap information from Id-Vg characteristics.
- Development of a body bias dependent mobility model in order to take into account the effect of interface trapped charge and surface roughness.
- Significant improvement in body effect modeling of SiC NMOS and PMOS.
- Modeling of the soft transition of SiC MOSFETs from the triode region to the saturation region.
- Inclusion of interface trapped charge effects on C-V characteristics.

- Development of a new parameter extraction routine for C-V characteristics optimization.
- New parameter extraction method development for model optimization of SiC MOSFETs.
- Global scaling of temperature and geometry behavior of SiC MOSFETs

1.4 Dissertation Outline

The contents of this dissertation are divided into eight chapters and organized in the following manner:

- Chapter 2: SiC Technology – The fundamental material properties of SiC are presented and current state of device fabrication technology on SiC wafer is reviewed.
- Chapter 3: SiC Compact Models for Circuit Design – Definition of compact models and their usefulness in circuit design are described. Compact models available for different SiC devices are surveyed and their merits and demerits are discussed.
- Chapter 4: Characterization of SiC MOSFET – The test structure which is used for MOSFET and parasitic diode characterization is presented. An accurate DC and CV characterization method is also provided.
- Chapter 5: BSIM3 and BSIM4 based models of SiC MOSFET – Modeling activity based on BSIM3 and BSIM4 is presented. Parameter extraction and optimization method is provided and fitting results are shown. Limitations of BSIM3 and BSIM4 in modeling SiC MOSFETs are also provided.

- Chapter 6: Effects of interface traps on SiC MOS Device – The origin of interface states in SiC MOS structure and their effects on DC, CV and transient characteristics are presented.
- Chapter 7: Model development of SiC MOSFET with Verilog-A – Development of Verilog-A model based on BSIM4 is presented. Detail description of step by step parameter extraction is provided and fitting results are shown.
- Chapter 8: Conclusion and Future Work – The summary of the dissertation and scope of future work are presented.

CHAPTER 2 SIC TECHNOLOGY

2.1 Properties of SiC Material

SiC is one of the emerging wide band-gap materials which has shown tremendous potential in high voltage, high temperature and highly efficient circuits and systems specifically for power electronics applications. Besides having higher breakdown voltage, lower intrinsic carrier concentration, better thermal conductivity, the SiC substrate is suitable for growing high quality oxide [12]. This is partially why SiC has become primary material of choice for medium voltage (1200V) power MOSFET fabrication. In this section, fundamental material properties of silicon carbide are discussed and a brief overview of SiC process technology and semiconductor devices are outlined.

2.1.1 SiC Crystal structure

Although there are over one hundred crystalline structures (commonly known as polytypes) of SiC in nature, only a few of them are reproducible and hence are attractive for semiconductor device fabrication [13]. Also, different polytypes have different electrical characteristics despite the fact that each of the polytypes consists of 50% Si and 50% C atoms. As a result, there are only three useful SiC polytypes for electronics application which are known as 3C-SiC, 4H-SiC and 6H-SiC. SiC atomic crystal structure is composed of Si-C bilayers [14]. These bilayers are stacked in a vertical direction with different sequences and hence give rise to various polytypes. In each bilayer, one atom is covalently bonded with three neighboring atoms in the same layer and only one atom in the vertical layer. The unit cell of 4H polytype contains four Si-C bilayers in the stacking direction while the 6H polytype unit cell contains six bilayers. Both of the polytypes have a hexagonal lattice structure. SiC is a polar semiconductor which indicates that one bilayer surface normal to the vertical axis terminates in Si atoms and the opposite surface terminates in carbon

atoms. The 3C-SiC is the only polytype which has the cubic crystal lattice structure. Table 2.1 lists the fundamental electrical characteristics of different SiC polytypes. Material properties of other semiconductors are also listed in order to provide comparison. From the table, it is found that 4H-SiC has a larger bandgap, better thermal conductivity, lower intrinsic carrier concentration and higher electron and hole mobility compared to other two polytypes. Also 4H-SiC wafer has superior manufacturability and manufacturers have been successful in reducing the micropipe density and increasing the size of the wafer. This is why it has become the primary choice for SiC device fabrication [15]-[16].

Table 2.1. Comparison of SiC Polytype Electronic Properties with Si, GaAs and GaN. Data are compiled from the information found in [9], [17], [18], [19] and [20].

Property	4H-SiC	6H-SiC	3C-SiC	Si	GaAs	GaN
Bandgap (eV)	3.26	3	2.3	1.1	1.42	3.4
Breakdown field $N_D = 10^{17}$ cm^{-3}($MVcm^{-1}$)	3.0^h 2.5^v	3.2^h $>1^v$	1.8	0.6	0.6	2-3
Thermal conductivity (W/cm-K)	3.7	3-5	3-5	1.5	0.5	1.3
Relative dielectric constant	9.7	9.7	9.7	11.7	13.1	9.5
Intrinsic carrier concentration (cm^{-3})	$\sim 10^{-7}$	$\sim 10^{-5}$	~10	10^{10}	1.8×10^{6}	$\sim 10^{-10}$
Electron mobility at $N_D = 10^{16}$ cm^{-3}(cm^2/V-s)	800^h 800^v	60^h 400^v	750	1200	6500	900
Hole mobility at $N_D = 10^{16}$ cm^{-3}(cm^2/V-s)	115	90	40	420	320	200
Saturated electron velocity (10^7 cm/s)	2	2	2.5	1	1.2	2.5
Donor dopants and shallowest ionization energy (meV)	N: 45 P: 80	N: 45 P: 80	N: 45	P: 45 As: 54	Si: 5.8	Si: 20
Acceptor dopants and shallowest ionization energy (meV)	Al: 200 B: 300	Al: 200 B: 300	Al: 270	B: 45	Be,Mg, C: 28	Mg: 140
Electron Affinity at 25°C (eV)	3.7	3.44	4	4.05	4.07	4.1

2.1.2 Chemical and mechanical properties

At room temperature, SiC practically does not react with any material which makes it an excellent inert semiconductor. Molten KOH etches SiC but only at relatively higher temperature (400-600°C). SiC does not exist in liquid phase rather it sublimes to vapor above 1800°C. The vapor contains Si, Si_2C and SiC_2 but with different proportion at different temperature. It is quite difficult if not impossible to diffuse any material into SiC and thus ion implantation and epitaxial growth are the only method to dope the semiconductor from intrinsic to n- or p-type [21]. The Young modulus of SiC is 90-137 GPa which indicates that the material has tremendous mechanical strength [22].

2.1.3 Bandgap voltage and intrinsic carrier concentration

Wide bandgap and thus very low intrinsic carrier concentration (N_i) make SiC the primary choice of material for high temperature application [23]. Although N_i increases dramatically as temperature rises, it remains order of magnitude lower than the extrinsic doping concentration even at high temperature (up to 500°C) which ensures that SiC retains its semiconductor properties and prevents excessive junction leakage [24].

In a typical CMOS process aimed for integrated circuit fabrication, different parts of the semiconductor material are doped differently which influences the bandgap of the material. This phenomenon is commonly termed as bandgap narrowing [7]. The band structure (energy vs density of states) of a semiconductor material at low doping concentration is such that the density of states has a square root relationship with energy away from the band edge as illustrated in Fig. 2.1(a). At higher doping concentrations, the energy gap structure is altered by three effects – creation of activation energy bands of impurity atoms, formation of tails in the bandgap edge and screening of minority carriers by the majority carriers. When the doping concentration is very high ($>10^{18}$

cm^{-3}), the spacing between the dopant atoms decreases. This gives rise to a band of dopant energy states in the semiconductor bandgap instead of a single energy site. If the doping concentration is even higher (>10^{21} cm^{-3}), the statistical distribution of impurity atoms causes a point-by-point difference in doping and potential profile inside the lattice and thus creates a tail in the band edge. Also, the number of majority carriers is more at higher doping concentration and the electrostatic interaction between the increased majority carriers and relatively low minority carriers decreases the thermal energy required for electron-hole pair generation due to screening of the minority carriers. Lower thermal energy allows higher intrinsic carriers in the semiconductor which is an indication of band-gap narrowing. The energy band structure of a semiconductor material at higher doping concentration is illustrated in Fig. 2.1(b).

In a MOSFET device, drain and source regions are highly doped and in a BJT device the emitter region is highly doped. If the bandgap narrowing due to higher doping concentration is significant in drain/source regions, more intrinsic electron-hole pairs are generated which contribute to more junction leakage current. On the other hand, higher intrinsic carrier concentration due to bandgap reduction in the emitter region of a BJT affects it operation by injecting more carriers in the base-emitter junction. Since SiC is a wide bandgap material, higher

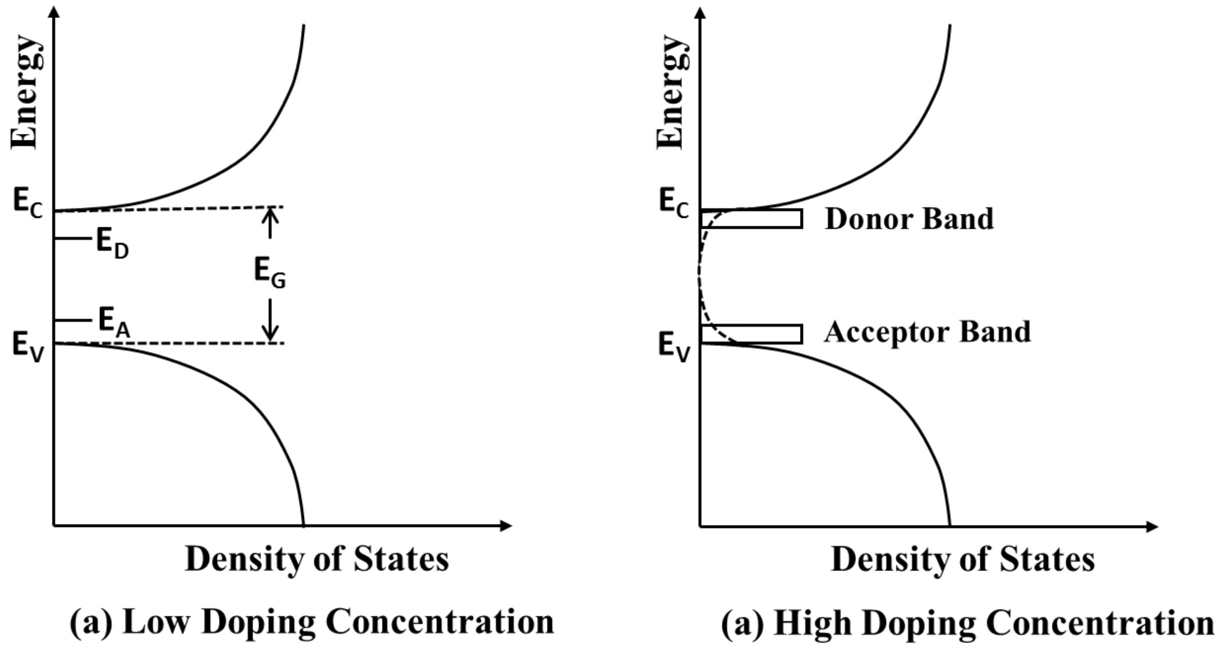


Fig. 2.1. Energy band profile with respect to density of states: (a) at low doping concentration, dopant activation energy (E_A and E_D) has discrete values and (b) at high doping concentration dopant energy has continuous range of values in a band [7].

doping concentration related bandgap narrowing is significantly smaller than that of Si and hence allows better high temperature device operation.

Intrinsic carriers are generated in a semiconductor material by thermal energy which excites an electron from the valence band to the conduction band and an electron-hole pair is created in the process. The number of carriers depends on the valence and conduction band density of states, bandgap as well as ambience temperature and can be calculated as [7]:

$$\boldsymbol{N_i = \sqrt{N_C N_V} e^{-\frac{E_G}{2kT}}} \tag{2.1}$$

where N_i is the intrinsic carrier concentration, N_C is the conduction band density of states, N_V is the valence band density of states, E_G is the bandgap of the semiconductor and T is absolute temperature in Kelvin. Taking into account the effects of temperature on N_C and N_V, N_i for silicon can be expressed as:

$$\boldsymbol{N_i = 3.87 \times 10^{16} T^{1.5} e^{-\frac{7.02\times10^3}{T}}} \tag{2.2}$$

For 4H-SiC, the relationship is as follows:

$$\boldsymbol{N_i = 1.7 \times 10^{16} T^{1.5} e^{-\frac{2.08\times10^4}{T}}} \tag{2.3}$$

From Eq. (2.2) and (2.3), it is found that the intrinsic carrier concentration of Si and SiC at room temperature (25°C) is 1.4×10^{10} cm^{-3} and 6.7×10^{-11} cm^{-3} respectively. The intrinsic temperature (T_i) is defined as the temperature at which the intrinsic carrier concentration in a semiconductor material becomes equal to its doping concentration. At T_i, the microplasma (few micrometers long current filament in the semiconductor lattice due to the non-uniform distribution of current density) becomes hot spot or mesoplasma and induces more carriers as the temperature further increases which increases the temperature even more and thus initiates positive feedback and possible thermal run away of the device [25]. For a useful doping concentration of 1×10^{15} cm^{-3} utilized in semiconductor device fabrication, T_i is 264°C and 1233°C for Si and SiC respectively which strongly indicates superior suitability of SiC for high temperature application.

2.1.4 Impact ionization coefficients

Impact ionization is the process where a highly energetic carrier imparts enough energy to an electron to move it from the valence band to the conduction band and creates an electron-hole pair. The impact ionization coefficient of a carrier is defined as the number of electron-hole pairs it generates when travelling 1 cm distance in a depletion region along the electric field. The coefficient is termed as α (α_p for hole and α_n for electron) and given by Chynoweth's Law [26]-[27]:

$$\boldsymbol{\alpha = a e^{-\frac{b}{E}}} \tag{2.4}$$

where a and b are the temperature and material dependent fitting parameters and E is the electric field.

The impact ionization coefficient is a very important material parameter for power device fabrication as it along with doping concentration, depletion width, edge termination etc. determines the breakdown voltage. For a low voltage integrated process, α determines the body current specially for a short channel device where a large electric field exists in the drain-body depletion area when the device is in saturation region [28]. Intensive efforts have been carried out to measure the hole and electron impact ionization coefficients of Silicon [29]-[30] and the fitting parameters a and b found to be 7×10^5 cm^{-1} and 1.23×10^6 Vcm^{-1} for electrons and 1.6×10^6 cm^{-1} and 2×10^6 Vcm^{-1} for holes respectively in the electric field range of 1.75×10^5 - 6×10^5 Vcm^{-1}. Efforts have also been made to measure α_p and α_n for 4H-SiC [31]-[32]. The ionization coefficients of 4H-SiC are found to be anisotropic which indicates the coefficients are different in different crystal directions [33]. Fitting parameter values of hole and electron impact ionization coefficients extracted from experiments are listed in Table 2.2. It is found that the parameter values of 4H-SiC

Table 2.2 Fitting parameter values of hole and electron impact ionization coefficients for 4H-SiC [34].

Symbol	Crystal direction	Impact ionization fitting parameter values	Parameter unit
a_n	c-axis	1.76×10^8	cm^{-1}
b_n	c-axis	3.30×10^7	Vcm^{-1}
a_p	c-axis	3.41×10^8	cm^{-1}
b_p	c-axis	2.50×10^7	Vcm^{-1}
a_n	a-axis	2.01×10^8	cm^{-1}
b_n	a-axis	1.70×10^7	Vcm^{-1}
a_p	a-axis	2.96×10^8	cm^{-1}
b_p	a-axis	1.60×10^7	Vcm^{-1}

are an order of magnitude greater than those of Si which favors SiC for high voltage and low leakage device fabrication.

2.1.5 Bulk and surface mobility

Mobility is defined as how fast a carrier responds and travels in a material when an electric field is applied. The carriers receive energy from the external electric field and moves with a fixed velocity in the direction of the field until they slow down due to scattering from the lattice vibration, coulombic force and/or the surface roughness. It is a very important parameter for majority carrier semiconductor device, such as a MOSFET, where drift is the primary mechanism of current transportation. Bulk mobility is characterized by the responsiveness of the carrier inside a semiconductor and surface mobility is characterized by the responsiveness of the carrier on any surface of the semiconductor. Surface mobility is more significant than bulk mobility in those devices where carriers are confined in a surface and current conducts along the direction of applied electric field. Examples of such devices are MOSFETs and IGBTs. Mobility is influenced by a number of material and device properties such as doping concentration, type of conduction and valence band, surface roughness, interface trapped and fixed oxide charge, resistivity, lattice structure, crystal defects etc. It is also greatly influenced by temperature and the magnitude of the applied electric field. Although the bulk electron mobility of 4H-SiC is somewhat comparable to the electron mobility of Si (800 vs. 1200 $cm^2/V\text{-}s$), the surface mobility in a 4H-SiC MOS device is significantly smaller than that of Si device (40 vs. 640 $cm^2/V\text{-}s$). The inferior surface mobility in SiC MOSFET is primarily attributed to the presence of defects and dangling bonds in the oxide-semiconductor interface and macroscopic surface roughness [35]. The poor oxide-semiconductor interface results in degraded device performance but also presents tremendous challenge in achieving reliable device operation [36]. The present state of electron and hole surface mobility in

SiC NMOS and PMOS and its dependence on process variation, temperature and external voltage stimulus will be discussed in detail in Chapter 6. A mobility model suitable for compact device model development and a complete parameter extraction method will be presented in Chapter 7.

2.2 SiC Devices and Fabrication Technology

A typical Si process technology consists of two major parts – 1) front-end-of-the-line (FEOL) and 2) back-end-of-the-line (BEOL). In the FEOL process, the basic device and component structures are formed. The process starts with wafer selection and then followed by dielectric deposition for isolation module formation, well formation, gate module definition and source/drain formation for MOS device, base/emitter/collector formation for BJT device and anode/cathode formation for diode. Resistors and capacitors are also developed in this part of the process. The FEOL process includes several unit processes such as diffusion, oxidation, ion implantation, etching, photolithography, annealing, chemical mechanical polishing and chemical vapor deposition (CVD). On the other hand, the BEOL process involves patterning and developing polysilicon and metal layers to establish interconnects between devices and components. Forming bond pads to connect the chip to the package and developing passivation layers to protect the chip from environmental contamination are also part of the BEOL process. This back-end part of the process is usually comprised of photolithography, etching and thin film deposition. Although a number of process modules such as photolithography, metallization, oxidation, passivation etc. from Si technology can be successfully utilized in SiC technology, special techniques are required in etching, dopant implantation, annealing as well as ohmic and schottky contact formation [37].

In a MOSFET device, engineering the doping profile is an essential step towards well formation, threshold voltage adjustment, drain/source formation and buried layer formation. While diffusion is a common process for selective doping in Si technology, it cannot be used in SiC

because almost all SiC dopants have very small diffusion coefficient [38]. Consequently, selective doping in intrinsic SiC can only be achieved either by ion implantation or epitaxial growth. In a modern CMOS Si process, the most widely used dopants are boron and phosphorus for p- and n-type doping respectively due to their excellent diffusibility in Si. Since diffusion is not a viable option in SiC process and boron has prohibitively large activation energy of 0.285 eV in SiC [39], Al is used as acceptor in SiC process to establish p-type region. The activation energy of Al is 0.19 eV and it has good solid solubility in SiC. In order to establish an n-type region in SiC, nitrogen is used as donor as it can be used to dope deep well and tub [40]. Also, ion implantation of nitrogen is less energy intensive and introduces less lattice damage due to its smaller atomic mass. The most challenging part of introducing dopants in SiC by ion implantation is annealing because excessively large temperatures (1500 $^{\circ}$ C to 1700 $^{\circ}$ C) are required to thermally activate the dopants in SiC. At this temperature, the SiC substrate starts to lose its crystal structure and defects and dangling bonds create surface roughness which ultimately degrade device performance. Intensive research has been carried out to develop better annealing techniques such as high temperature rapid temperature annealing (RTA) [41], aluminum nitride capping [42], dummy wafer capping using SiC powder [43] and graphite film capping [44]. In-depth descriptions of SiC process technology can be found in [16], [21], [33] and [45].

2.2.1 SiC CMOS process

SiC low voltage MOS process is still in research and development phase due to reliability issues, high temperature packaging challenges and smaller market share. As mentioned in Chapter 1, Raytheon Systems Limited UK launched the first commercial CMOS process for high temperature SiC integrated circuit design. In that process, a 100 mm n-type 4-H SiC wafer with a grown-doped epitaxial layer is used as starting substrate [46]. The devices are fabricated on the 4°

off axis Si face. The fabrication process starts with the formation of n-well and p-well regions for p-type and n-type FETs respectively by ion implantation [47]. In the next step, n+/p+ source drain regions for NMOS and PMOS are fabricated by another ion implantation. The tuning of the doping profile in the channel is also accomplished by ion implantation. In this process, aluminum is used as an acceptor dopant and nitrogen is used as a donor dopant. All the dopants are activated in a single high temperature annealing step and a carbon cap is used to prevent the surface from becoming excessively rough. The thin oxide which serves as gate oxide and thick oxide which serves as the isolation module are then formed by oxidation. The SiC CMOS process is not a self-aligned process since the source/drain region is formed before the gate dielectric formation and the source, drain and channel are not automatically aligned by the gate electrode. The gate electrodes of both NMOS and PMOS are fabricated by depositing polysilicon which marks the completion of FEOL part of the process. In the BEOL of the process, interconnect is patterned by refractory metal deposition and ohmic contacts are formed using a Nickel (Ni) based alloy. Since SiC CMOS is a high temperature process, the pads might be oxidized during probe testing at elevated temperature. In order to protect the pads from oxidation, a thin Ni layer is applied on top of the metal layer. Finally, a passivation layer is formed by oxidation to protect the chips from scratches and external contamination and the process is concluded by opening bond pads and depositing gold alloy. The cross section of the Raytheon SiC CMOS is shown in Fig. 2.2.

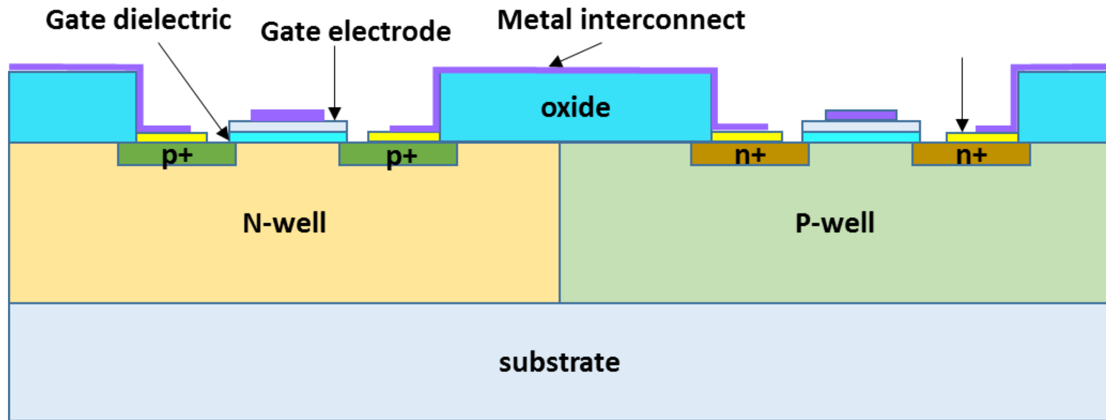


Fig. 2.2. Simplified cross section of an inverter in the Raytheon high temperature SiC CMOS process.

The Raytheon SiC CMOS process has a 1.2 µm minimum channel length and is developed to operate at temperatures up to 400 º C. A list of process parameters and accompanying device characteristics are provided in Table 2.3.

Table 2.3. Some pertinent process and device parameters of Raytheon HiTSiC SiC CMOS process.

Parameter name	Parameter values	
	NMOS	PMOS
Nominal gate voltage (V)	15	-15
Nominal drain voltage (V)	15	-15
Nominal bulk voltage (V)	-15	15
Typical threshold voltage (V)	3	-5
Gate leakage current @ 350 º C (pA)	0.7	0.8
Gate oxide thickness (nm)	40	40
Minimum channel width (µm)	4	4
Minimum channel length (µm)	1.2	1.2
Channel doping concentration (cm^{-3})	6.7×10^{16}	4×10^{17}
Body diode leakage current @ 300 º C (pA)	55	20
Nominal mobility (cm^2/V-s)	55	25

2.2.2 Power MOSFET

Until recently, the most successful application of SiC has been in the fabrication of power MOSFETs with voltage ratings in 1200 – 1700 V range and current ratings in 3 – 160 A. The wide bandgap of SiC along with low intrinsic carrier concentration and high critical electrical field is ideal for fabricating MOSFET device with large blocking voltage and small on-resistance which is practically impossible to achieve in Si. SiC power MOSFETs are now available for commercial use in power electronics systems from a number of company such as Cree/Wolfspeed/Infineon, GeneSiC Semiconductor, Microsemi Corporation, Rohm Semiconductor, STMicroelectronics etc. Although the blocking voltage of commercial SiC power MOSFET is limited to 1700 V, research is in progress to push the breakdown voltage to a higher value while keeping the on resistance low and improving the channel mobility. Howell et al. [48] have reported a large area 10-kV 4H-SiC DMOSFET with low subthreshold leakage current (4 nA at 200 ^{o} C). The low leakage was achieved by an additional epitaxial thin layer grown on top of the ion implanted p-well regions using a N_2O based oxidation process. Harada et al. [49] have demonstrated a 3.3-kV UMOSFET with superior on-resistance (8.3-9.4 mΩcm^2) and enhanced gate oxide shielding from the edge effect of the trench bottom. Mori et al. [50] have developed an innovative 4H-SiC MOSFET which has both reverse and forward blocking capability of 3 kV and can serve as a high-voltage bi-directional switch. Soler et al. [51] have applied a new Boron diffusion step based process and were successful to fabricate a large area 4.5-kV 4H-SiC VDMOS with higher channel mobility, lower on resistance and improved 3rd quadrant operation. Yen et al. [52] have reported a 1700V/30A SiC MOSFET with an integrated Schottky diode which has 1V of cut-in voltage (the parasitic body diode has 3V of cut-in voltage) and thereby contributes to significant reduction in

on-state energy loss. Cheng et al. [53] have a 4H-SiC DMOSFET which has 3.3-kV of forward blocking voltage and is capable of conducting 30 A of current at 200 W/cm^2 of power dissipation.

2.2.3 Other Devices

Although power MOSFETs occupy the major market share of SiC discrete devices, SiC Schottky diodes have been commercially available even before power MOSFETs hit the market and other devices are gradually emerging to be useful. Commercial SiC Schottky diodes with a wide range of reverse voltage rating (up to 8-kV) and forward current rating (up to 120 A) are available for purchase from Digikey [54]. Researchers also have demonstrated Schottky diodes with higher breakdown voltage by incorporating interdigitated p-n junction barrier beneath the Schottky contact. Hull et al. [55] have reported a large area (0.88 cm^2) junction barrier Schottky (JBS) diode which is able to block 10-kV of reverse voltage and has 20 A/cm^2 current density. The reported diode was found to have a positive temperature coefficient and reliable linear I-V characteristics up to 200 °C. Zhao et al. [56] have also developed a 10-kV Schottky diode using multistep junction termination extension and achieved a current density of 48 A/cm^2 at forward voltage drop of 6 V. Other SiC power devices include super junction bipolar transistor (SJT), Junction Field Effect Transistor (JFET), PiN diode, Insulated Gate Bipolar Transistor (IGBT) and gate turn off (GTO) thyristor. A 1200V/7A quasi-majority carrier super junction bipolar transistor capable of operating at 250 °C with low leakage (< 10 μA), improved switching transients (< 15 ns), high current gain of 72 and low on resistance (< 235 mΩ) has been reported in [57]. Successful development of SiC JFET and JFET based circuits have been reported in [58]-[59]. A SiC PiN diode with record breaking blocking voltage of 26.9-kV with enhanced carrier lifetimes has been reported in [60]. SiC n-channel IGBT with a 27-kV of breakdown voltage and 20 A of forward

current has demonstrated in [61]. Wolfspeed (formerly known as Cree) has developed 15-kV SiC SGTO thyristor [62].

2.3 Summary

In this chapter, a brief overview of SiC process technology was presented. SiC power devices are emerging rapidly and becoming an integral part of power electronics circuits and systems. SiC power MOSFETs and Schottky diodes are currently being used in commercial products such data center power converters, solar inverters, electric and hybrid electric vehicle battery chargers etc. SiC low voltage processes are also being developed for integrated circuit design and successful integration of low voltage control circuitry, gate drivers and power switches in the same power module and/or SiC substrate will open doors with tremendous potential towards building high power density and high power electronics circuits and systems.

CHAPTER 3 AN OVERVIEW OF SEMICONDUCTOR DEVICE MODELING

3.1 Semiconductor Device Modeling Using Numerical Method

The most accurate method of semiconductor device modeling is to self-consistently solve the drift-diffusion equations at a very large number of geometry points inside the device using a numerical method as a function of time. The drift-diffusion model includes Poisson's equation, current density equations, current continuity equations and Schrödinger's equation where the device dimension is so small that quantum mechanical effects (wave function penetration, tunneling etc.) become inevitable. Poisson's equation is used to solve for electrostatic potential inside the semiconductor for a given charge distribution and is formulated as:

$$\vec{\nabla} \cdot \left(\varepsilon \vec{\nabla} \phi\right) = -q(-n + p + N_D^+ - N_A^-) \qquad 3.1$$

where ε is the permittivity of the semiconductor, ϕ is the electrostatic potential, q is the charge, n is the electron density, p is the hole density, N_D^+ is the ionized donor dopant density and N_A^- is the ionized acceptor density.

Current density equations relate the density of current with mobility, potential and charge density as the drift component and with charge, carrier density gradient and diffusion coefficient as the diffusion component. The equation is given by:

$$\vec{J} = -qc\mu\vec{\nabla}\phi + qD\vec{\nabla}c \qquad 3.2$$

where J is the current density, c is carrier (electron or hole) concentration, μ is the carrier mobility and D is the carrier diffusion coefficient.

The current continuity equation ensures the conservation of charge and establishes a relationship between rate of change of carrier concentration, volumetric gradient of the carriers

and carrier recombination-generation rate. The continuity equation for any carrier (electron or hole) is given by:

$$\frac{\partial c}{\partial t} = \frac{1}{q}\vec{\nabla} \cdot \vec{J} - R + G \qquad 3.3$$

where c is the carrier (electron or hole) concentration, $\vec{\nabla} \cdot \vec{J}$ is volumetric gradient of the current density, R is recombination rate and G is the generation rate of the charge carriers.

The numerical simulation of the drift-diffusion system of equations begins with defining the device structure, identifying the material properties and setting up the temperature, bias voltage, doping profile etc. The equations are then discretized in space and time using finite difference techniques and solved for electrostatic potential (ϕ), electron (n) and hole (p) concentration iteratively based on the initial guesses of ϕ, n and p until the solution converges to a predefined degree of precision. For a planar device like a MOSFET, the equations are discretized in two dimensions (cross section parallel to the channel) but for a non-planer device like the Gate All Around (GAA) FET, the equations are discretized in three dimensions. It is noted that accurate models of mobility, carrier concentration and recombination-generation rate of the carriers as well as proper boundary conditions at the interface are required in order to correctly model the current transport inside the device. There are a number of commercial simulators available in the industry which can be used for numerical simulation. Example of such simulators are TCAD Sentaurus Device and Taurus Medici from Synopsys [63] and Victory Device and Atlas from Silvaco [64].

Although the numerical method is best suited for single device modeling and can serve as an excellent tool for designing a novel device, it is not suitable for circuit or system simulation which consists of multiple instances of the device due to prohibitively large simulation time. Modern day mixed signal System-On-Chip (SOC) are comprised of millions (if not billions) of

transistors and require fast and yet accurate simulation. With this end, explicit closed form equations of state variables (charge, current etc.) of the device with respect to the external stimulus (voltage) are developed based on the approximate solutions of the drift-diffusion system of equations. In the next section, a brief overview of compact models used for circuit design and their primary requirements are outlined.

3.2 Compact Models for Circuit Design and Simulation

A compact model is defined as a simple yet accurate description of the terminal characteristics of a semiconductor device as a function of the terminal bias and is used inside a circuit simulator. The circuit simulator utilizes an iterative algorithm such as Newton-Raphson to solve the Jacobian matrix (consists of node current equations) of a circuit and as such the compact model implemented inside the simulator is required to be computationally efficient and discontinuity free. Some basic requirements of a compact models are as follows:

- The model should be developed based on the physical behavior of the device so that it can accurately predict the terminal characteristics. The model equations should be derived from the solution of the drift-diffusion equations instead of using an empirical approach.
- Ideally the model equations and their derivatives should be continuous and thus they should not contain piecewise regional equations. The discontinuity in the equations may cause convergence issue when the simulator tries to solve the Jacobian matrix.
- The equations should be simple enough so that the simulation time does not become too large. This is a conflicting requirement with respect to accuracy and makes high quality compact model development really challenging.

- The compact model must be technology independent. There are hundreds of silicon foundries all over the world for integrated circuit fabrication. A semiconductor device compact model should be able to predict the device behavior even if one process is different from another.
- The model should generate realistic results in the presence of unrealistic terminal biases. The simulator might find an unreasonable value from the solution of the Jacobian matrix and if the model does not produce a reasonable value at this solution the simulation will never converge.
- A device is used in a different region of operation for different types of circuits. For example, MOSFET is used as a switch in digital circuit and as a result it is either on or off when the circuit is in operation. On the other hand, in an amplifier which is an analog circuit, the MOSFET is primarily used in moderate inversion in the saturation region and hence accurate prediction of small signal parameters such as transconductance, output resistance etc. is essential. The MOSFET is also often used in subthreshold or weak inversion region in low power circuit design. A good compact model should be able to predict the device behavior in all regions using a single continuous equation.
- A number of model parameters are used to optimize a compact model for different process nodes and variations. The parameter extraction and optimization method of a compact model should be easy and well defined. To this end, the number of model parameters should be kept as small as possible.

- The equations in a compact model should be formulated that they amount to zero current at zero terminal voltage biases. This is essential for the quasi-static modeling approach.
- The design variables for the MOSFET which are available to an integrated circuit designer are width (W) and length (L) and the design variable for BJTs and diodes is area (A). A compact model should be scalable with respect to the design variables.
- The model should contain enough physical content of the device behavior so that it can be effectively used for statistical analysis such as mismatch and Monte-Carlo simulation.
- The characteristics of a semiconductor devices significantly change if the device temperature is different from room temperature. A compact model should be able to predict the device behavior at all possible operating temperatures.

Based on the details of a compact model required for a specific application, the model can be either very simple and consists of few equations and parameters or very complicated and can have hundreds of equations and parameters. For example, a Level 3 MOSFET model has about 10 equations and less than 50 parameters [65] whereas an advanced MOSFET model such as BSIM4v4.8.0 has more than 200 equations and about 300 parameters [66]. Modern day silicon technology has predominantly evolved around the advancement of CMOS processes and thus lots of effort has been put into development of MOSFET compact model. Most of the available MOSFET models fall into one of the three following categories:

Threshold voltage based model: In this approach, instead of using the exact solution of surface potential (ϕ) obtained from Poisson's equation, it is assumed that ϕ varies linearly with gate voltage in the subthreshold region and becomes fixed when the device enters into strong

inversion. The current is calculated using an approximated solution of Eq. 3.2. and an advanced mobility model. Threshold voltage is defined as the gate bias below which the device operates in subthreshold and above which the device operates in strong inversion. In subthreshold or the weak inversion region, the dominant part of the current conduction is diffusion while in the strong inversion region drift governs the majority of current conduction. When the gate bias is within a few thermal voltages around the threshold voltage, the device operates in the moderate inversion region and both drift and diffusion play significant role in current transport. One of the drawbacks of the threshold voltage based model is poor modeling of the moderate inversion region. Another drawback of the threshold voltage based model is that it loses device symmetry under special circumstances since the model equations are derived assuming the source terminal as a reference. Some examples of threshold voltage based MOSFET compact models are BSIM3 [67], BSIM4 [68] and BSIMSOI [69]. BSIM3v3 and BSIM4 have been by far the most popular MOSFET compact models in semiconductor industry and are widely used for CMOS integrated circuit design in micron, sub-micron and sub-100 nm process nodes. This dissertation work is based on BSIM4 and a detail model formulation of BSIM3 and BSIM4 will be outlined in Chapter 5.

Inversion charge based model: In order to eliminate the asymmetry issues inherent in threshold voltage based source referenced MOSFET models, inversion charge based models were derived [70]. A lateral MOSFET device is electrically and geometrically symmetric with respect to the body node and the symmetry in device current and capacitances is achieved by deriving all the equations referring to the body node. In this modeling approach, the inversion charge (Q_i) serves as the state variable and can be expressed as a function of pinch-off voltage (V_P) and channel voltage (V_{ch}). V_{ch} is defined as the difference between the quasi-fermi potential of the carriers and V_P is defined as the V_{ch} at which inversion charge is zero for a particular gate voltage. Since V_{ch} is

equal to source voltage (V_S) at the source side and equal to drain voltage (V_D) at the drain side, the inversion charge at the source and drain side can be expressed as a function of $V_P – V_S$ and $V_P – V_D$ respectively. Inversion charge has an exponential relationship with gate bias (or equivalently V_P) in weak inversion region and has a quadratic relationship in the strong inversion region. In the moderate inversion region, Q_i is derived by linking the weak and strong inversion expressions using appropriate interpolation. The drain current is found by solving the drift-diffusion systems of equation and given by:

$$I_D = \frac{\mu_n W}{L}\left[\frac{Q_{IS}'^2 - Q_{ID}'^2}{2nC_{ox}'} - \phi_t(Q_{IS}' - Q_{ID}')\right] \quad 3.4$$

where I_D is drain current, μ_n is the electron mobility, W is the channel width, L is the channel length, Q_{IS}' is the source side inversion charge density, Q_{ID}' is the drain side inversion charge density, n is subthreshold slope and ϕ_t is the thermal voltage. One of the drawbacks of the inversion charge based model is that the inversion charge expression is an implicit function of the terminal biases and require iteration which increases the simulation time. Approximations are made in order to obtain a closed form solution of the inversion charge but it compromises accuracy. The detail derivation of the inversion charge based MOSFET compact model can be found in [71]. BSIM6 [72] and EKV [73] are two excellent examples of inversion charge based models and widely used in low power, low voltage analog and RF integrated circuit design.

Surface potential based model: This type of model formulation is the most physical in nature as device charge, current and capacitance are directly related to the exact solution of the surface potential. From the energy band-diagram or charge neutrality condition, electron and hole concentration are derived as a function of surface potential and using Poisson's equation electric field is expressed in terms of surface potential. The relationship between terminal biases and

surface potential is established using voltage balance and appropriate boundary conditions in the semiconductor. It is found that the analytical expression of surface potential is implicit and requires iteration. In order to avoid an iterative algorithm to solve the surface potential equation, an approximate formulation is used based on [74]. The most important aspect of surface potential based compact model is that a single equation is used to represent the device behavior in all regions of operation i.e. accumulation, depletion, subthreshold, moderate inversion and strong inversion without utilizing any smoothing functions. This ensures continuity not only in the drain current and channel charge but also in any derivative of the current and charge. Also, surface potential based model does not suffer from any asymmetry issue. A detail formulation of surface potential based model is found in [75]. The PSP model which was developed by the combined effort of Penn State University and NXP Semiconductors is a good example of a surface potential based model [76]. Although PSP is a very accurate model, sometimes it becomes very difficult to incorporate any secondary effect such as substrate current induced body effect, impact ionization effects etc. which is very common in modern day ultra-small MOSFETs due to its extreme physical nature.

Most of the compact models are developed based on the quasi-static approximation which does not incorporate current continuity equations as shown in Eq. 3.3. In the quasi-static approximation, it is assumed that the device charge can respond instantaneously to the external applied bias. While this is true for low frequency and low speed applications, charge cannot readily respond and redistribute itself if the transients in the terminal stimulus exceed the inherent transit time of the device. In order to accurately model the delay between the applied bias and device charge transport, a non-quasi static solution based on the current continuity equation which includes a time dependent differential equation is required. Since simulators cannot solve differential equations analytically, separate models are developed for non-quasi static large signal

transient simulation and small signal ac simulation. Formulation of non-quasi static MOSFET model can be found in [77] and [78].

When all the equations of a compact model are formulated, the model is usually implemented using a programming language that can be compiled by a circuit simulator. In the past, the compact models were written in C or FORTRAN for SPICE like simulators such as PSPICE, LTSPICE, HSPICE, Spectre, Ngspice etc. and were tightly coupled to the numerical algorithms of the simulators. It was a tedious task to write compact models in such a low level language as it required tens of thousands of lines of manual coding and most often proved to be error prone as it also required explicit hand coding of the derivatives of the current and charges. In order to alleviate these issues, hardware description languages (HDL) such as VHDL, Verilog, Verilog-A, System Verilog and Mast which were originally developed for behavioral modeling of circuits and systems have come to the rescue. As such Verilog-A has become the *de facto* standard for compact model development and most of the commercial circuit simulators now have an embedded compiler that can generate compact module interfaces from Verilog-A code. The model can be implemented in Verilog-A with fewer lines of codes and does not require hand coding of the derivatives as the compiler can accurately find symbolic expressions of the derivatives with respect to terminal voltages from the original equations. For example, the original BSIM4 C code has more than thirty thousand lines of code whereas the more complex BSIM6 model which is implemented in Verilog-A has less than seven thousands lines of codes. Another popular circuit simulator particularly used for power electronics circuit simulation is Saber from Synopsis and it can compile compact model written in Mast [79].

Although a compact model consists of current and charge equations as a function of device's terminal biases, it is convenient to view the model as an equivalent circuit representation

of the device commonly known as the model topology. The model topology is constructed using standard circuit components such as resistor, capacitor, constant current source etc. and the through (current) and across (voltage) variables of each component are related through the model equations. Also there are model parameters in a compact model which are used to optimize the model over the measured characteristics of the device. Apart from developing discontinuity free equations for a compact model, lots of subtle things are required to be taken into accounts when implementing the model with Verilog-A to ensure numerical efficiency, robustness and reduced calculation time [80]-[81]. Some critical points regarding the best practices of compact model development using Verilog-A are summarized as follows:

- Simplicity is the first rule of writing a compact model. There is no place for Laplace and Z-transform functions, ideal delay function, level crossing driven events in a compact model. This functions might be very useful in formulating behavioral description of a circuit or a system but might introduce convergence issues when used in a compact model.
- Time domain differential operator (*ddt()*) should always be used instead of integral operator (*idt()*) when a temporal relationship between voltage and current of a device is governed by differential equation. For example, an inductor voltage should be obtained by differentiating the inductor current with respect to time instead of integrating inductor voltage to find inductor current.
- If a model contains a high impedance node (either internal or external), a limiting of the impedance value should be done by appropriately setting the *gmin* parameter. The simulation might not converge if the current into a node is much smaller than the KCL convergence limit.

- Standard macros and analog functions available in the Verilog-A library should be used in writing the model equations as much as possible. Also constants such as q (electronic charge), m_e (electronic mass), ε_0 (air permittivity) etc. should be used from the definitions already available in *constants.vams* header file.
- The values of the model parameters should be limited to a range consistent with the physical nature of the parameters. For example, the saturation velocity parameter of a MOSFET model cannot be negative. Also, the parameter values should be within the range with which the model has been optimized and verified and should avoid values which might cause convergence issues.
- The circuit components used to represent the model topology should be declared as branches and through and across variables should be accessed using the branch definition. An example of declaring a resistive branch is as follows:

```
Branch (a, b) drain_res;
I(drain_res) <+ (1/Rd)*V(drain_res);
```

Where R_d is a model parameter. Avoid using following style:

```
I(a, b) <+ (1/Rd)*V(a, b);
```

- The capacitive current should always be formulated as the time derivative of the charge at a node as follows:

```
I(Cdrain) <+ ddt(qdrain);
```

The following formulations of capacitive current should be avoided:

```
I(Cdrain) <+ Cdrain*ddt(V(Cdrain));
I(Cdrain) <+ ddt(Cdrain*V(Cdrain));
```

The first formulation will violate charge conservation and the second formulation will provide wrong results if the capacitance is non-linear.

- Any potential numerical nuisance from equation evaluation such as a divide by zero, a negative number inside a square root, a non-integer power of a negative number, a logarithmic evaluation of non-positive number, an exponential overflow etc. should be sorted out and appropriate measures should be undertaken to avoid them.
- The Verilog-A compiler uses symbolic derivation to determine the derivatives and as such no quantity should be hard coded to zero values at zero bias using conditional statements. For example, charge at a particular node may be zero from the charge equation at zero voltage while the capacitance might not as the capacitance is the derivative of device charge with respect to voltage.
- If a real number data type is intended, it should be initialized with a real value (2.0 instead of 2). Verilog-A will perform integer division and return 0 if ½ is used instead of 1.0/2.0 which should be evaluated as 0.5.
- A compact model should be devoid of any hidden states. If a variable is not initialized before using it in a conditional block and the value of that variable is evaluated at a later part in the model, the variable will be assigned to a hidden state by the simulator. A model which has hidden states will suffer from convergence issues in periodic steady state (PSS) analysis. PSS is a very powerful tool for time variant RF circuit simulation. All the variables should be initialized before using them in a conditional block.

More information on how to write an efficient and organized compact model with Verilog-A and how to avoid common pitfalls can be found in [82]-[83].

3.3 Compact Models of SiC Devices

In the integrated circuit industry, there is a proverbial saying, “The simulation results are as good as the models.”, which readily emphasizes the importance of a good compact model in IC design. Since the SiC CMOS technology is still evolving, an accurate predictive model of the MOSFET is even more necessary to simulate the circuit over many process corners and a wide temperature range. The modeling of SiC lateral MOSFETs poses tremendous challenge as the device characteristics are severely altered due to the presence of trapped charge at the oxide semiconductor interface. It is extremely difficult to find stable correlation between the devices’ behavior and variation in channel length and temperature as the density of interface states are often uncontrollable and unpredictable and affects devices differently over different geometry and operating temperature. BJT and diode models are equally important if they are used in a circuit design.

On the other hand, in high frequency power electronics systems, even a few nHs of parasitic inductances significantly affect the switching characteristics and introduce ringing and electromagnetic interference (EMI). In order to predict the ringing and EMI which many a time contribute to disastrous circuit failure, it is mandatory to simulate the circuit topology with accurate power device models instead of using an ideal switch model. This is particularly true for wide bandgap semiconductor devices such as SiC power MOSFETs as this switches can operate at significantly higher frequency than Si devices in the medium voltage (1000V) application.

A brief overview of all the available compact models for SiC devices is presented in the following subsections. This includes the models of low voltage lateral MOSFETs, high voltage vertical power MOSFETs, diodes, BJTs, IGBTs etc.

3.3.1 Lateral MOSFET Models

Since SiC CMOS integrated circuits are yet to find a wide range of applications, the model development for SiC low voltage MOSFETs is still in the early stage. Kashyap et al. [84] have reported a compact model of SiC NMOS based on surface potential based model PSP. They developed a new parameter extraction method to achieve better optimization in subthreshold modeling which was required due to the softer transition of the SiC FET from weak inversion to strong inversion. However, they did not report any information on capacitance and small signal parameter (output resistance, transconductance etc.) modeling and only compared simulated and measured characteristics of the NMOS. Also, body effect modeling was not included and results on geometry scaling optimization was not presented. Besides, effects of interfaces trapped charge on device characteristics which are abundant in SiC were not discussed nor any model strategy for these effects was proposed. A more detail compact model of 4H-SiC lateral MOSFET was presented by Mudholkar et al. [85] and parameter extraction and optimization was performed both for enhancement and depletion mode NMOSs. This model was also developed based on PSP and an attempt was made to incorporate the effects of interface trapped charge on subthreshold slope and inversion charge by including bias dependent flat band voltage expression in the surface potential equation. However, this method has a severe shortcoming as the surface potential equation becomes implicit and can only be solved using iteration which introduces convergence issues and consumes more simulation time. Apart from these two references, there are not many reports on SiC lateral MOSFET compact models in the literature. Schmid et al. have presented an

integrated inverter and 17-stage ring oscillator based on 6H-SiC NMOS but these were digital circuits and no information on the model usage in circuit simulation was provided. Xie et al. [86] have also reported a number of integrated digital circuits such as binary counter, half adder, D-latch, SR flip-flop and basic digital gates (NAND, NOR, XNOR) in 6H-SiC NMOS technology but did not provide any details on the models used in the circuit simulation. An intelligent integrated gate driver which included a number of process sensitive circuits such as hysteretic comparator, bias circuit, charge pump circuit, short circuit protection circuit, under voltage and over voltage detection circuit etc. fabricated in SiC CMOS technology was published by chen et al. [87]. The HSPICE level 2 model which is inadequate for optimizing SiC MOSFETs was used for circuit simulation in that work.

3.3.2 Power MOSFET Model

Development of SiC power MOSFETs has the most attention among all the wide bandgap devices and the modeling activity has been closely in pace with the technology development. The model proposed by Mcnutt et al. [88] is considered the pioneer work in SiC power MOSFET compact modeling. They developed a unique current expression which included the low voltage turn-on effect at the corners of the square MOSFET cell and also incorporated enhanced transconductance usually found in the linear region due to carrier concentration gradient in the non-uniformly doped channel. Kraus et al. [89] have presented a physics based compact model for SiC MOSFETs and included effects of interface trapped charge on the channel charge and electron mobility in the model. Good agreement was shown between the simulated and measured device characteristics. Potbhare et al. [90] have published a physical model for 4H-SiC MOSFET which particularly formulates high temperature behavior of SiC MOSFET devices in presence of interface trapped charge. Mudholkar et al. [91] have reported a datasheet driven power MOSFET

model and proposed an easy parameter extraction recipe which is equally applicable for both Si and SiC MOSFETs. Sun et al. [92] have proposed a PSPICE macro model for SiC power MOSFET which can be used for a wide range of operating temperatures including below room temperature (-25 $^{\circ}$ C). Arribas et al. [93] have demonstrated a simple and accurate SiC power MOSFET model based on SPICE Level 1 model and reported a faster simulation time with the model compared to that of Level 3 based model. A SPICE model for SiC power MOSFET has been proposed by d'Alessandro et al. [94] which can be used for dynamic electrothermal simulation to determine the detrimental effects of interface trapped charge on the device behavior. Chen et al. [95] have shown that the non-linear junction capacitance inherent in power MOSFET structure affects device's switching transient significantly and demonstrated an improved SiC power MOSFET model by including a better model of the junction capacitance. Fu et al. [96] have developed a simplified MOSFET model where they have included a physics based formulation of the current saturation effect at the end of the channel close to the JFET region.

3.3.3 Models of Other SiC Devices

In a SiC power module, the most efficient use of power devices as a switch is the combination of power MOSFETs and antiparallel Schottky diodes [97]. The SiC Schottky diode is one of the earliest wide bandgap devices which manufacturers were able to fabricate and thus its compact modeling activity has come a long way. Mcnutt et al. [98] have reported a diode compact model for the Saber circuit simulator and validated the model with the measured characteristics of 600 V SiC Schottky diode, 1500 V SiC Merged Pin Schottky Diode and 5000 V SiC PiN diode. Excellent agreement between the simulated and measured on-state characteristics, di/dt, dv/dt and reverse recovery characteristics as well as good temperature scaling were demonstrated. Fu et al. [99] have presented a method for extracting carrier concentration, active

area and thickness of the drift region and used the parameter extraction procedure to develop a physics based SiC Schottky diode model. Leakage current which is bias dependent in Junction Barrier Schottky (JBS) diode was modeled in [100] and a detail parameter extraction sequence was proposed for optimizing temperature dependency of I-V and C-V characteristics. Jahdi et al. [101] proposed an analytical formulation of SiC Schottky diode's switching energy loss as a function of dI_{DS}/dt and temperature and incorporated the model into the diode's SPICE model. Du et al. [102] have reported an advanced modeling technique of SiC JBS diode's junction capacitance using equivalent series/parallel input impedance and controlled current source and validated the model with measured data of a 10 kV device. Saadeh et al. [103] have presented a unified compact model for IGBT device and demonstrated good agreement between simulated and measured characteristics of an n-channel Si IGBT and n- and p-channel SiC IGBTs. Miyake et al. have proposed an improved model for base carrier distribution of a punch-through IGBT based on the HiSIM-IGBT model in order to accurately predict the turn-off characteristics of the device and presented a comparison between the analytical and 2-D device simulation results. A detailed review on the available wide bandgap power devices models can be found in [104] and [105].

3.4 Summary

In this chapter, different types of semiconductor device modeling suitable for different applications was explained. Numerical simulation using detail drift-diffusion models is very attractive for designing a single device, compact models consisting of closed form equations are more suitable for circuit simulation. A summary of all techniques related to compact model development of MOSFET devices is described and best practices of implementing compact models using Verilog-A were outlined. Finally, a brief overview of all compact models available for SiC devices were presented.

CHAPTER 4 CHARACTERIZATION OF SIC MOSFET

Accurate and noise free measured data is essential for reliable parameter extraction and optimization in a compact model development process. In order to characterize the devices (MOSFET, BJT, diode) and components (capacitor, resistor) thoroughly and to monitor the process control parameters such as gate oxide thickness, junction depth, doping concentration etc., each reticle (repetitive circuit blocks on a wafer) contains dedicated test structures commonly termed as Process Control Monitoring (PCM). Since MOSFETs are the most used devices in a CMOS integrated circuit process, the PCM includes a number of NMOSs and PMOSs with a wide variety of channel lengths and widths as well as related capacitance and body diode test structures. These structures are intensively characterized to capture high quality data for the purpose of parameter extraction and optimization.

4.1 Test Structures

At the beginning of NSF BIC project, PCM structures were provided by Raytheon UK to the University of Arkansas for device characterization and compact model development as the Raytheon foundry did not have a reliable Process Design Kit (PDK). The PCM includes an array of NMOSs, PMOSs, high area and high periphery parasitic diodes, MOS caps, MOSFETs (both n- and p-type) with a large number of fingers along with other structures such as poly caps, metal caps, poly resistors, diffusion resistors etc.

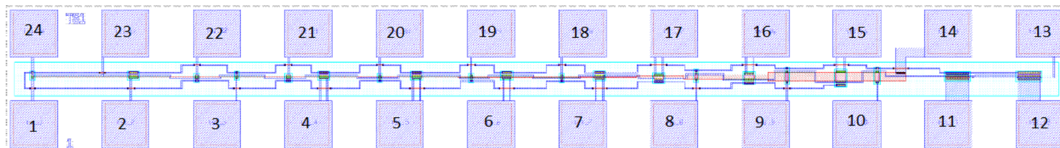


Fig. 4.1 Test structures of NMOS array with different device widths and lengths.

The NMOS array is shown in Fig. 4.1. The probe pads are marked with different numbers which indicate connections to source, drain, gate and body terminals of different MOSFETs. There are twenty NMOS devices in the structure with channel widths ranging from 4µm to 50µm and channel lengths ranging from 0.8µm to 20µm. Twelve devices among the twenty which fall into the wide/long, wide/short, narrow/long and narrow/short bin were characterized. All the MOSFETs have common source, gate and body terminals and but different drain terminals for each different geometry. An n-type wafer is used as substrate in Raytheon HiTSiC process and the NMOSs are fabricated in their own ion-implanted p-well. In Table 4.1, the corresponding probe pad of each MOSFET terminal is shown:

Table 4.1. Geometry information and corresponding pad location of NMOS devices.

Test Structure Name	NMOS Device		Bond Pad Id			
	W (µm)	L(µm)	Drain	Source	Gate	Body
htsc1_ts1	20	20	15	23	14	24
	20	10	16	23	14	24
	20	5	17	23	14	24
	20	2	7	23	14	24
	20	1.5	6	23	14	24
	20	1.2	5	23	14	24
	6.6	20	10	23	14	24
	4	20	9	23	14	24
	4	10	8	23	14	24
	4	2	18	23	14	24
	4	1.5	19	23	14	24
	4	1.2	20	23	14	24

The PMOS array has a similar structure except the devices are grown in an ion-implanted n-well and as such all the PMOSs share the substrate as their body terminal. The test structure of the PMOS array is shown in Fig. 4.2. Test structure of PMOS array with different device widths and lengths.

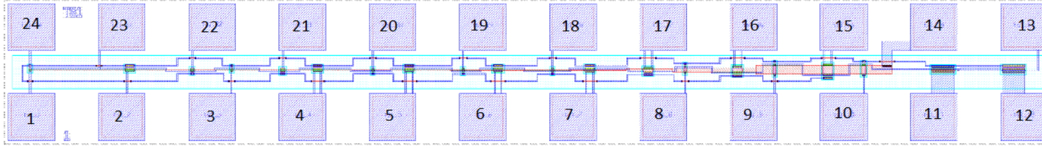


Fig. 4.2. Test structure of PMOS array with different device widths and lengths.

The PMOS device width and length and corresponding probe pad location of each FET terminal is shown in Table 4.2.

Table 4.2. Geometry information and corresponding pad location of NMOS devices.

Test Structure Name	PMOS Device		Probe Pad Id			
	W (µm)	L(µm)	Drain	Source	Gate	Body
htsc1_ts2	20	20	15	23	14	24
	20	10	16	23	14	24
	20	5	17	23	14	24
	20	2	7	23	14	24
	20	1.5	6	23	14	24
	20	1.2	5	23	14	24
	6.6	20	10	23	14	24
	4	20	9	23	14	24
	4	10	8	23	14	24
	4	2	18	23	14	24
	4	1.5	19	23	14	24
	4	1.2	20	23	14	24

A different test structure was used to characterize the MOSFET C-V since it is extremely difficult to accurately measure MOS capacitance if the device area is as small as that of the devices used for DC characterization. The oxide capacitance is given by:

$$C_{OX} = A \cdot \frac{\varepsilon_{OX}}{t_{OX}} \quad \textbf{4.1}$$

where C_{OX} is the total oxide capacitance, A is the area of the device, ε_{OX} is the permittivity of the gate dielectric and t_{OX} is the oxide thickness. From $COX = A \cdot \frac{\varepsilon_{OX}}{t_{OX}}$

4.1, it is found that the oxide capacitance of a MOSFET with 20µm of width and 2µm of length is 0.0345pF for 40nm of oxide thickness. The 34.5fF capacitance is too small for a C-V meter to measure with good precision as the noise margin is also in the fF range. This is why a test structure which includes a big device with large width and area (MOS cap) and another big device with a large number of device fingers (multi-fingered MOSFET) are usually used for C-V characterization. The MOS cap structure does not include the drain and the source terminals and hence only provides the oxide capacitance. Also, the measured capacitance can be approximated as ideal oxide capacitance since the parasitic component is very small to the large width and length of the structure. The multi-fingered MOSFET structure is used to measure the total gate capacitance which includes both the intrinsic and the parasitic components and the later component is now significant due to the small device length used in the structure. The typical layouts of the MOS cap and the multi-fingered MOSFET are demonstrated in Fig. 4.3 and Fig. 4.4 respectively. The test structure with the related pads utilized for C-V measurement is shown in Fig. 4.5.

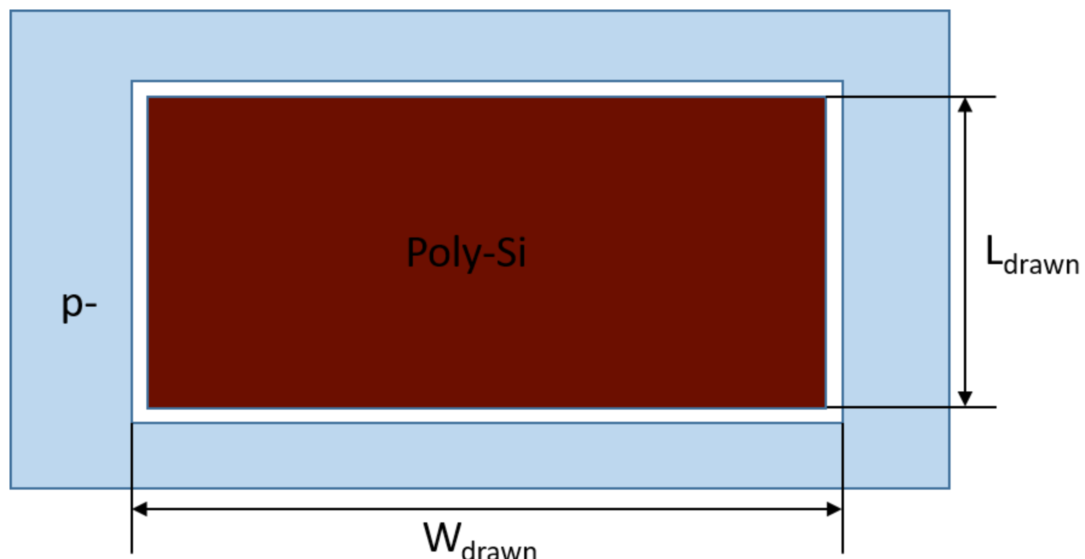


Fig. 4.3. A typical layout of the MOS cap structure. Gate oxide is underneath the poly Si.

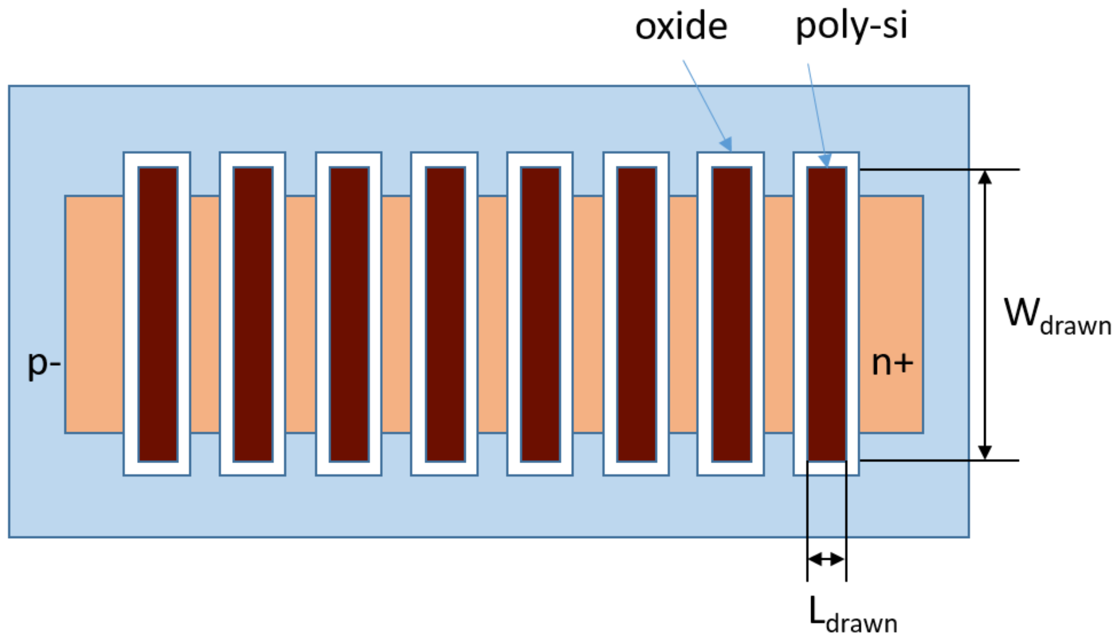


Fig. 4.4. A typical layout of the multi-fingered MOSFET. Although not shown, the drain and source terminals of all the fingers are usually shorted in this type of structure.

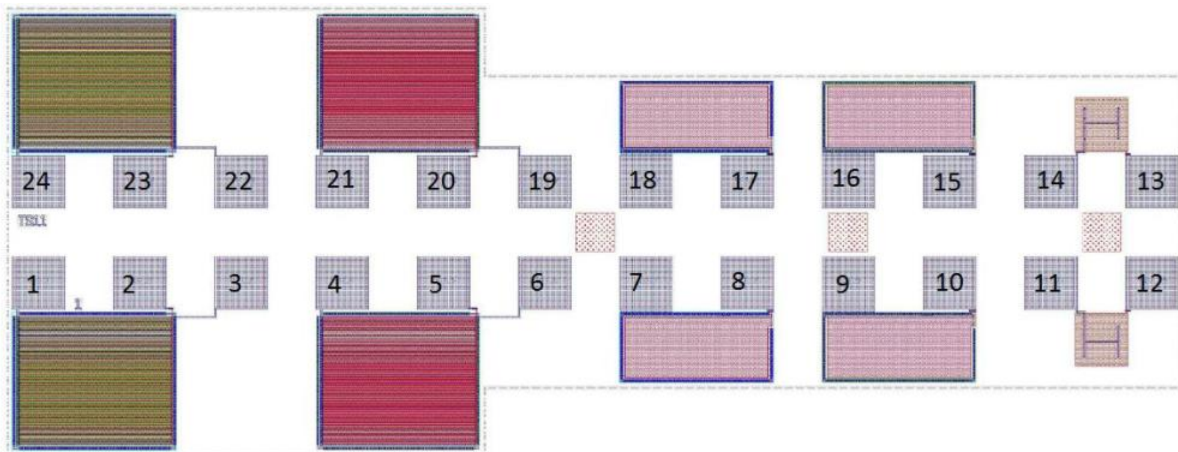


Fig. 4.5. Test structure for MOSFET C-V measurement. Devices located on the top row are used for the capacitance characterization.

In a CMOS process, the lateral MOSFET is usually a symmetric device and drain and source terminals are indistinguishable from each other. As a result, if the terminals are shorted together, it is sufficient to characterize the capacitance from the gate to the other terminals since

$C_{gd} = C_{dg}$ and $C_{gs} = C_{sg}$ when $V_{DS} = 0$. Furthermore, if the drain and source voltages are not equal and the gate voltage is above the device's threshold voltage, DC current starts to conduct in the device and ac capacitance measurement becomes almost impossible because the small ac current is masked by the large DC current. This is why all the MOSFET capacitances are measured keeping the drain and source terminals shorted together.

The capacitances of a MOSFET device can be classified as: 1) intrinsic device capacitance which consists of oxide capacitance and channel capacitance and 2) extrinsic or parasitic capacitance which consists of gate-drain/source overlap and fringing capacitance and body diode junction capacitance. Oxide capacitance is measured from a MOS cap structure with large width and length while total gate capacitance which includes oxide capacitance, channel capacitance and overlap and fringing capacitance is measured from a MOSFET structure with large width, short channel and multiple number of fingers. The detail information of the devices used for capacitance measurement is shown in Table 4.3.

Table 4.3. Device dimensions and probe pad location of devices used for capacitance measurement.

Test Structure Name	Device Type	Device Dimension			Probe Pad Id			Measured Capacitance Type
htsc1_ts11		W(µm)	L(µm)	NF	G	B	D/S	
	NMOS	300	1	74	23	22	24	Gate to DSB Cap
	NMOS	284.4	120	1	17	18	x	Oxide Cap
	PMOS	300	1	74	20	19	21	Gate to DSB Cap
	PMOS	284.4	120	1	15	16	x	Oxide Capacitance

Although in conventional analog and mixed signal circuits, the parasitic drain/source to body diode never turns on, its junction capacitance affects the transient and frequency response of the circuits. The body diode does turn on if the MOSFET is used as a synchronous rectifier in a

monolithic switch mode dc-dc converter design. The junction capacitance of the diode has two parts: 1) bottom wall capacitance which depends on the drain/source area and 2) side wall capacitance which depends on the drain/source perimeter. In order to measure the bottom wall capacitance, a body diode with large width and length is used while to measure the side wall capacitance multiple diodes each with smaller area connected in parallel are used. A test structure which includes high area and high perimeter N+/P-well and P+/N-well diodes are shown in Fig. 4.6. The typical layouts of the high area and high periphery diodes are shown in Fig. 4.7 and Fig. 4.8.

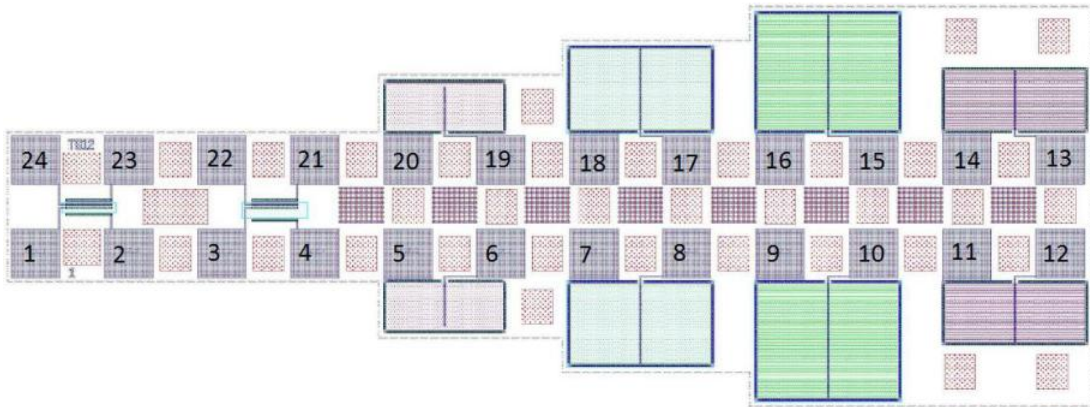


Fig. 4.6. High area and high perimeter parasitic diode structure of NMOS and PMOS. The devices located at the top row are used for characterization.

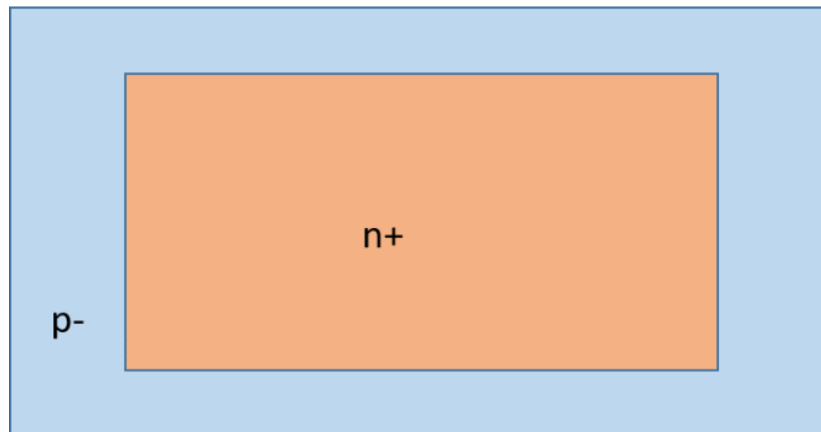


Fig. 4.7. Typical layout of a n+/p-well diode with large area and small periphery.

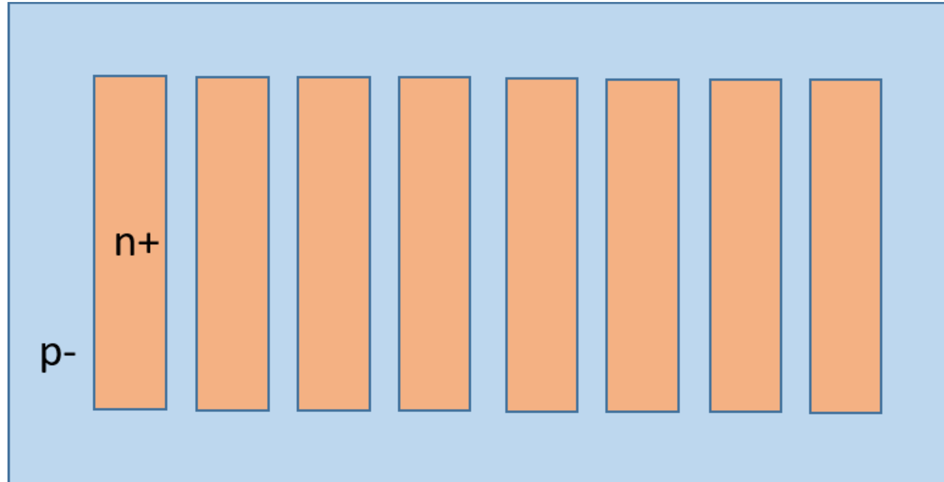


Fig. 4.8. Typical layout of a n+/p-well diode with large area and large periphery.

The area and perimeter of the diode are chosen as such that the measured capacitance is in the range of tens of pF. The dimension of the diodes and the corresponding probe pad locations are shown in Table 4.4.

Table 4.4. Parasitic diode test structure with device dimension and probe pad locations.

Test Structure Name	Device Type	Device Dimension		Probe Pad Id		Measured Capacitance Type
		Area (μm^2)	Perimeter (μm)	Anode	Cathode	
htsc1_ts12	High Area N+/P-well	51×10^{-9}	940×10^{-6}	18	17	Bottom Wall Capacitance
	High Perimeter N+/P-well	52.5×10^{-9}	21.35×10^{-3}	16	15	Side Wall Capacitance
	High Area P+/N-well	25×10^{-9}	700×10^{-6}	19	20	Bottom Wall Capacitance
	High Perimeter P+/N-well	27×10^{-9}	10.98×10^{-3}	13	14	Side Wall Capacitance

4.2 DC Characterization

The MOSFET and body diode DC characteristics were measured using a Semiprobe probe station and a Keithley 4200 Semiconductor Characterization System (SCS). Probe tips were landed

on the probe pads of the devices and connections between the device and Keithley 4200 were made by coaxial cables. The programmable Source Measure Unit (SMU) of 4200 SCS can be configured through an interactive software tool called Keithley Interactive Test Environment (KITE) to automatically apply voltages to the Device Under Test (DUT) and measure the device current. The KITE has a device library which includes MOSFET, BJT, diode, resistor, capacitor and generic device with programmable terminals and any of the devices can be configured for automatic characterization. A plethora of information on how to use Keithley can be found in [106].

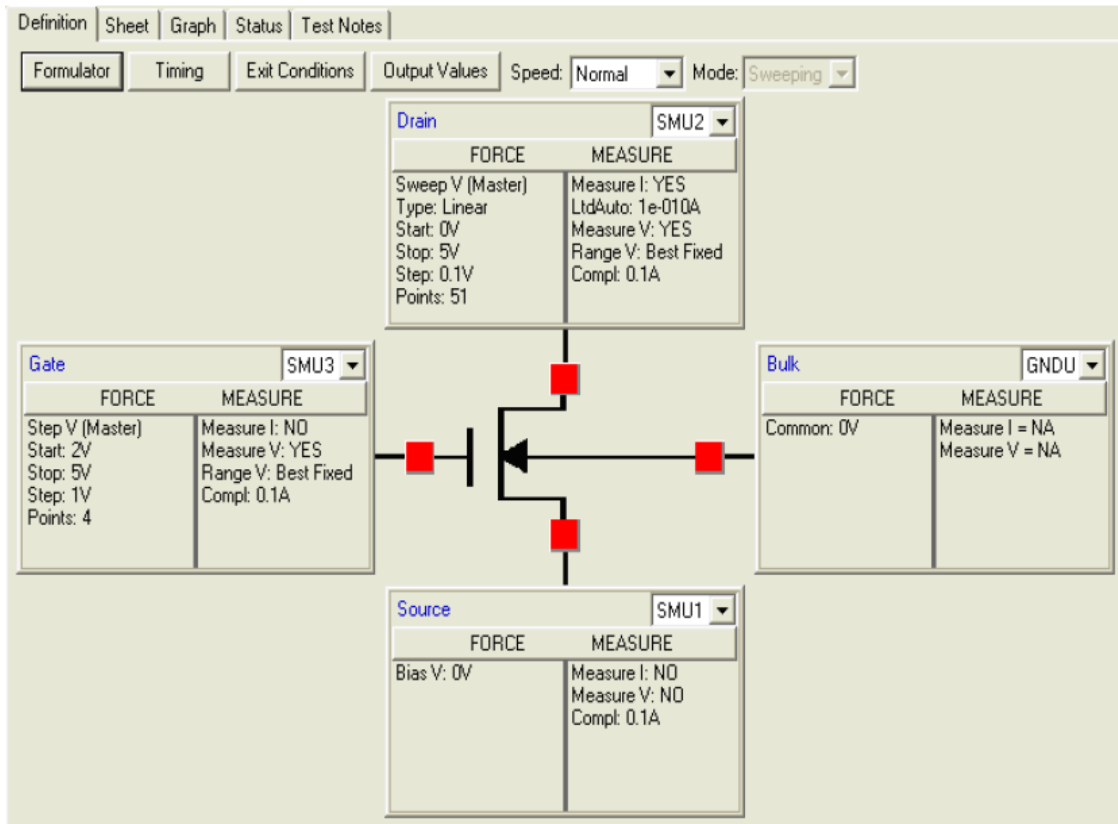


Fig. 4.9. KITE configuration for MOSFET DC characterization.

A typical configuration for measuring I-V characteristics of a MOSFET device is shown in Fig. 4.9.

4.2.1 Characterization of a MOSFET I-V

The MOSFET has four terminals – gate, drain, source and body and voltages are applied to the terminals with respect to the source terminal. The device is required to be characterized at a wide range of biases to cover all the operating regions i.e. cut-off, subthreshold, strong inversion, triode and saturation. In order to extract and optimize model parameters, three different types of drain current measurement are done:

- Drain current vs. gate voltage at different drain and body biases ($I_D – V_G$ @ different V_D and V_B) as shown in Fig. 4.10.

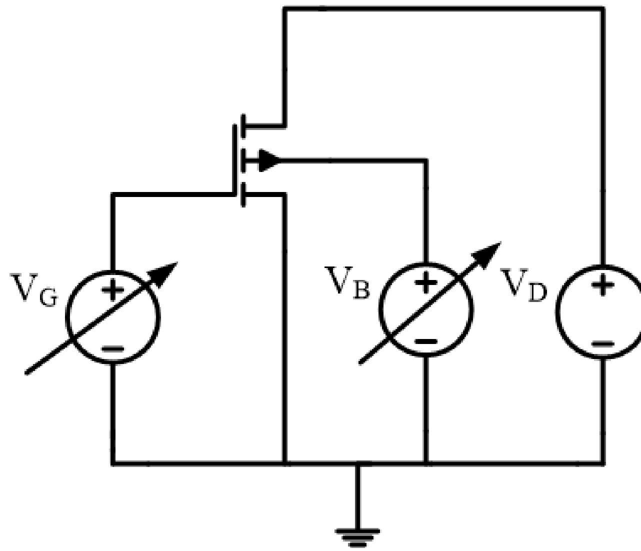


Fig. 4.10. Test bench for transfer Characteristics characterization.

- Drain current vs. drain voltage at different gate biases and zero body bias ($I_D – V_D$ @ different V_G and $V_B = 0V$) as shown in Fig. 4.11.
- Drain current vs. drain voltage at different gate biases and maximum reverse body bias ($I_D – V_D$ @ different V_G and $V_B = V_{DD}$ for PMOS and $V_B = -V_{DD}$ for NMOS) as shown in Fig. 4.12.

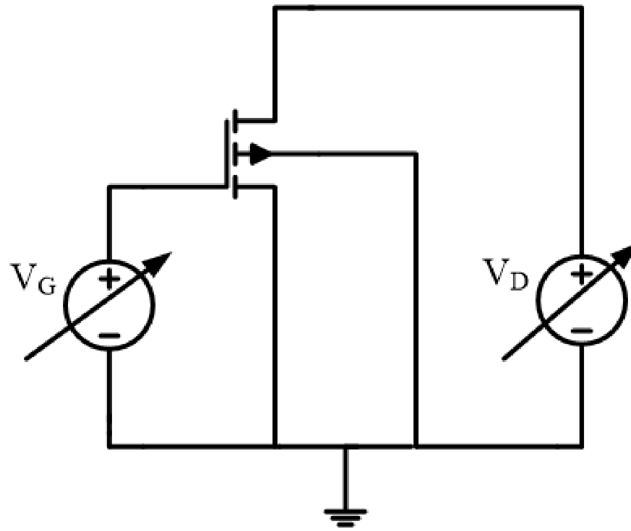


Fig. 4.11. Test bench for output characteristics characterization at zero body voltage.

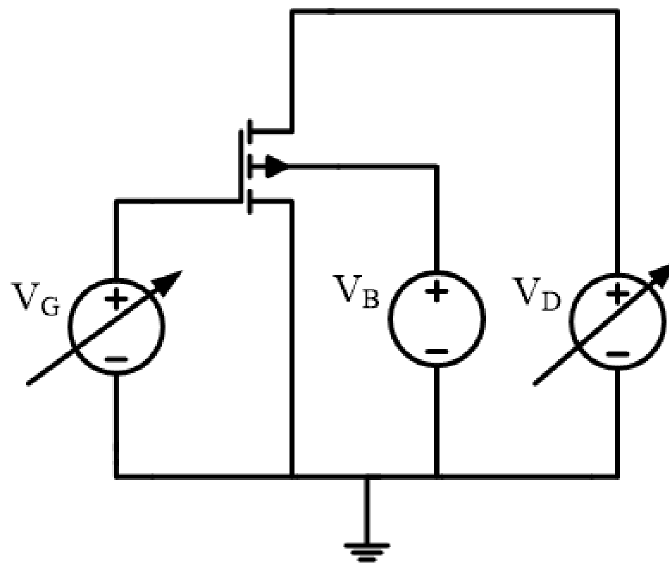


Fig. 4.12. Test bench for output characteristics characterization at maximum body voltage.

The Raytheon HiTSiC is a 15V process and for I-V measurement of the SiC MOSFETs, the voltages at the gate, drain and body terminals were applied in the range from 0V to 15V. The measurements were done at four temperatures – 25 ° C, 100 ° C, 200 ° C and 300 ° C. The KITE

was configured as a multi-site project in which each site was related to one of the twelve devices. There were eight I_D – V_G measurements and two I_D – V_D measurements and all the I-V measurements of one site were done automatically with one run from the KITE. This helped reduce user interaction and thus saved time and prevented human error. The number of data points and precision of the current measurement were chosen as such that the measurement time was reasonable and the measured data was accurate and noise free. High quality data from the I – V measurement is required because small signal parameters such as transconductance (g_m) and output conductance (g_{ds}) which are the first derivatives of I_D – V_G and I_D – V_D respectively are also required for parameter extraction and optimization. The sweeping and stepping of voltages at different terminals of the NMOS is shown in Table 4.5.

Table 4.5. Applied bias voltage ranges at NMOS terminals. The source terminal was connected to ground.

<table>
<tr><td colspan="3">Drain Bias
(V)</td><td colspan="3">Gate Bias
(V)</td><td colspan="3">Body Bias
(V)</td><td>Type of I – V Measurement</td></tr>
<tr><td colspan="3"></td><td>Start</td><td>Stop</td><td>Step</td><td>Start</td><td>Stop</td><td>Step</td><td></td></tr>
<tr><td colspan="3">0.5</td><td rowspan="8">0</td><td rowspan="8">15</td><td rowspan="8">0.5</td><td rowspan="8">-3</td><td rowspan="8">-12</td><td rowspan="8">-3</td><td rowspan="8">I_D – V_G</td></tr>
<tr><td colspan="3">1</td></tr>
<tr><td colspan="3">2</td></tr>
<tr><td colspan="3">3</td></tr>
<tr><td colspan="3">6</td></tr>
<tr><td colspan="3">9</td></tr>
<tr><td colspan="3">12</td></tr>
<tr><td colspan="3">15</td></tr>
<tr><td>Start</td><td>Stop</td><td>Step</td><td colspan="3"></td><td colspan="3"></td><td></td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">15</td><td rowspan="2">0.5</td><td>3</td><td>15</td><td>2</td><td colspan="3">0</td><td>I_D – V_D @ V_B= 0V</td></tr>
<tr><td>7</td><td>15</td><td>2</td><td colspan="3">-15</td><td>I_D – V_D @ V_B= -V_{DD} V</td></tr>
</table>

Since the magnitude of the threshold voltage of the PMOS is higher than that of the NMOS, I_D – V_D measurements required fewer gate voltages. If the magnitude of the gate voltage is below

the threshold voltage of the device, the PMOS device operates in off state and leakage current is in picoamp range. The 4200 SCS takes a very long time to measure the small leakage current and thus the measurement time becomes excessively large. The sweeping and stepping of voltages at different terminals of the PMOS is shown in Table 4.6.

Table 4.6. Applied bias voltage range at PMOS terminals. The source terminal was connected to ground.

<table>
<tr><td colspan="3">Drain Bias (V)</td><td colspan="3">Gate Bias (V)</td><td colspan="3">Body Bias (V)</td><td>Type of I – V Measurement</td></tr>
<tr><td colspan="3"></td><td>Start</td><td>Stop</td><td>Step</td><td>Start</td><td>Stop</td><td>Step</td><td></td></tr>
<tr><td colspan="3">-0.5</td><td rowspan="8">0</td><td rowspan="8">-15</td><td rowspan="8">-0.5</td><td rowspan="8">3</td><td rowspan="8">12</td><td rowspan="8">3</td><td rowspan="8">$I_D – V_G$</td></tr>
<tr><td colspan="3">-1</td></tr>
<tr><td colspan="3">-2</td></tr>
<tr><td colspan="3">-3</td></tr>
<tr><td colspan="3">-6</td></tr>
<tr><td colspan="3">-9</td></tr>
<tr><td colspan="3">-12</td></tr>
<tr><td colspan="3">-15</td></tr>
<tr><td>Start</td><td>Stop</td><td>Step</td><td colspan="3"></td><td colspan="3"></td><td></td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">-15</td><td rowspan="2">-0.5</td><td>-5</td><td>-15</td><td>-2</td><td colspan="3">0</td><td>$I_D – V_D$ @ V_B= 0V</td></tr>
<tr><td>-9</td><td>-15</td><td>-2</td><td colspan="3">15</td><td>$I_D – V_D$ @ V_B= V_{DD} V</td></tr>
</table>

4.2.2 Characterization of Parasitic D/S to Body Diode

Since a diode is a two-terminal device, the DC characterization of the device is straightforward. One important point to remember while measuring I – V characteristics of a diode is that the polarity of the voltages applied at the anode and cathode terminals has to be accurate. If a large positive voltage is applied at the anode terminal, excessive current might flow and can cause irreversible damage to the device.

The current of high area and high periphery N+/P-well and P+/N-well diodes was measured at the voltage range from -5V to 15V and the bias was applied at the cathode terminal while keeping the anode terminal grounded. The measurements were made at 25 ° C, 100 ° C, 200 ° C and 300 ° C. The junction leakage current was highest at 300 ° C and was limited to tens of pA which is typical for a wide bandgap diode. The turn-on voltage of the diode was found to be greater than 2V and the maximum on-state current was less than 10 mA. The I-V characteristics showed a negative temperature coefficient which indicates that the current through SiC diode increases with the rise in temperature.

4.2.3 Best Practices of DC Characterization

Although characterization of semiconductor devices from a bare die using a probe station at room temperature is not very challenging, accurate measurement at high temperature sometimes can be problematic. The following guidelines can be helpful to capture good quality data from a SiC MOSFET measurement:

- Proper contact between probe pad and probe tip is very important for bare die device characterization. The resistance contributed by the poor contact might be higher than the device's intrinsic resistance and can introduce error in the current measurement. Always make sure that the probe has a sharp tip and that it makes a scratch when landing on the pad.
- The Keithley 4200 has three settings related to the speed and accuracy of the measurement – fast, normal and quiet. With the 'fast' setting the measurement will be very fast but the data will be noisy and with the 'quiet' setting the measurement time will be longer but the data will be clean. The 'Quiet' setting should be chosen

for MOSFET DC characterization. The ‘Normal’ setting proves to be sufficient for diode current measurement.

- The precision of the current measurement also depends on the ‘range’ setting. For MOSFET drain current characterization, the ‘range’ setting with limited auto and 100p – 10nA of current gives the best quality data.
- Always lift the probes from the pads before increasing the measurement temperature. If the temperature is increased while the probe is landed on the pad, thermal expansion of the metal on the pad might damage the probe tips.
- Avoid making too much scratches on the probe pads. At high temperature, the metal on the pad becomes soft and it is easy to scrape off the metal from the pad. If too much metal is depleted, it will be very difficult to make proper contact with the pad.
- Always check the data before saving. At high temperature, the contact to probe pads might become unstable during a measurement and the measured data might include unexpected noise.

4.3 C-V Characterization

Capacitance measurement of a device is more difficult than DC current measurement because the instrument is required to accurately measure a small quantity ac signal. There are a number of techniques available for reliable C-V measurements [107]-[108] but the most popular one which is frequently used in commercial C-V meters is known as the auto balance bridge (ABB) method. A four-wire Kelvin connection is used for capacitance measurement and the terminals are HIPOT, LOPOT, HICUR and LOCUR. HIPOT and LOPOT are the two terminals of a voltmeter which measures the ac voltage across the device. The terminals of the ammeter which senses and

records the current through the device are HICUR and LOCUR. SMA cables are used to establish connection between the device and the C-V meter because this particular type of cables has the least parasitic capacitance compared to coaxial and triaxial cables. The Keithley CVU 4210 which was used for SiC device capacitance measurement has special red SMA cables specifically designed for C-V characterization. In Fig. 4.13., a typical configuration of how the device is connected to the 4210 C–V meter is demonstrated. It is important to note that the outer shells of the SMA cables should be tied together for high frequency (>1MHz) capacitance measurement. The HIPOT and HICUR terminals are shorted together at one end and LOPOT and LOCUR terminals are tied to the other end of the device. The interactive software provided by Keithley (KITE) is used to configure the C-V measurement settings.

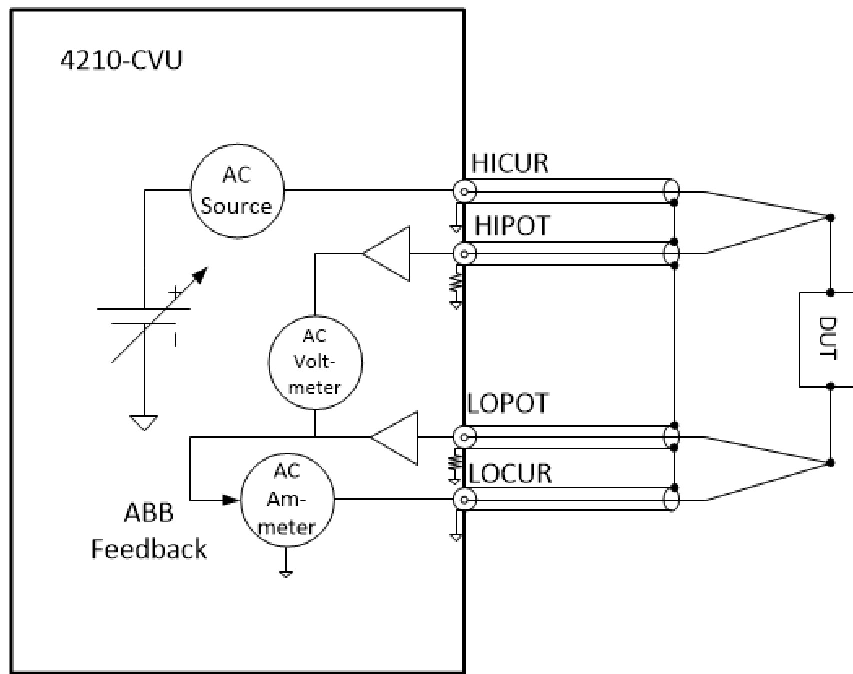


Fig. 4.13. Simplified connection diagram between the device and C-V meter [109].

A conceptual block diagram of the auto balance bridge method is shown in Fig. 4.14. An ac test voltage superimposed with the DC bias is applied at the DUT terminal where the HIPOT and HICUR terminals are connected together. At the LO terminal, the purpose of connecting a null detector circuit is to force the voltage at the terminal to zero volts and establish a virtual ground. The feedback circuit consisting of a null detector, a signal processor, the DC bias, the ac signal generator, and the range resistor sends a balancing signal to force the LO terminal to zero voltage. The feedback network in the CVU 4210 is a digital loop. If an accurate and stable virtual ground can be maintained at the LO terminal, the voltage at the HI terminal will measure as the voltage across the DUT and the voltage across the range resistor will be proportional to the current through the DUT. The phase shift between the DUT voltage and current is determined by the delay of the feedback loop. The capacitance is calculated from the measured voltage and current phasor of the DUT. More information on accurate capacitance measurement using Keithley CVU 4210 can be found in [110]-[111].

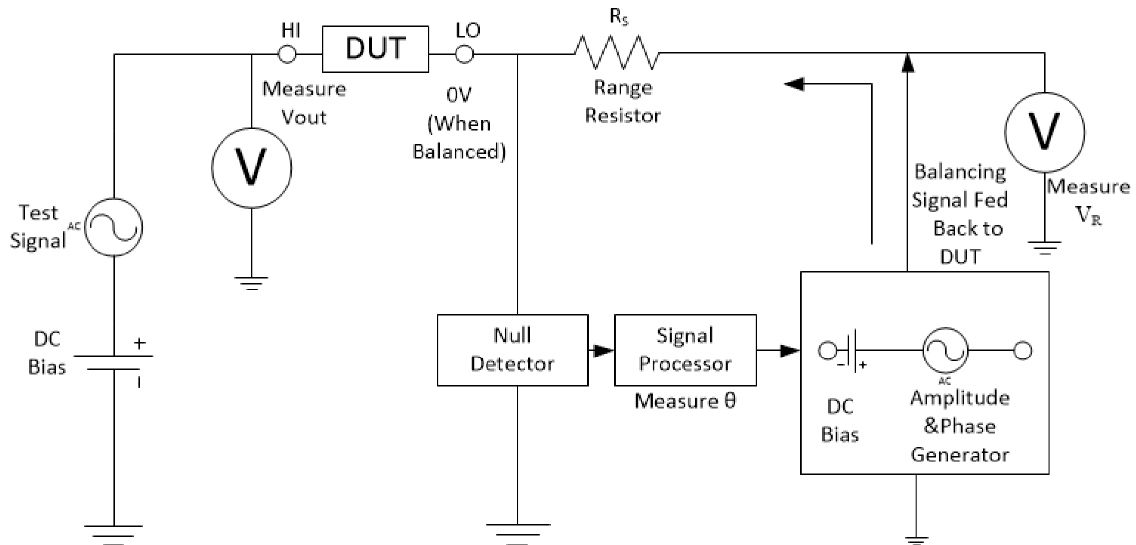


Fig. 4.14. Conceptual block diagram of the auto balance bridge capacitance measurement method [110].

4.3.1 MOSFET C-V Characterization

The structure used to measure the oxide capacitance (C_{ox}) has two terminals – 1) the polysilicon gate and 2) the P/N-well bulk. A dc bias ranging from -20V to 20V with 0.25V step was applied at the gate terminal (connected to HI) and the small ac signal was applied at the bulk terminal (connected to LO). The test bench for characterizing C_{ox} is shown in Fig. 4.15. The total gate capacitance ($C_{g\text{-}dsb}$) was measured from the structure with large number of fingers by applying -20V to 20V with 0.5V step at the gate terminal (tied to HI). The drain/source and bulk terminals were tied together to LO at which the small ac signal was applied. The test bench is shown in Fig. 4.16. The capacitance from gate to drain/source ($C_{g\text{-}ds}$) was also measured to isolate the parasitic overlap and fringing capacitance from the total gate capacitance. In this configuration, the small signal ac was applied to the drain/source terminal and the bulk or body terminal was connected to the DC ground. The test bench for measuring $C_{g\text{-}ds}$ is shown in Fig. 4.17. The capacitances were measured at four temperatures- 25 ^{o} C, 100 ^{o} C, 200 ^{o} C and 300 ^{o} C.

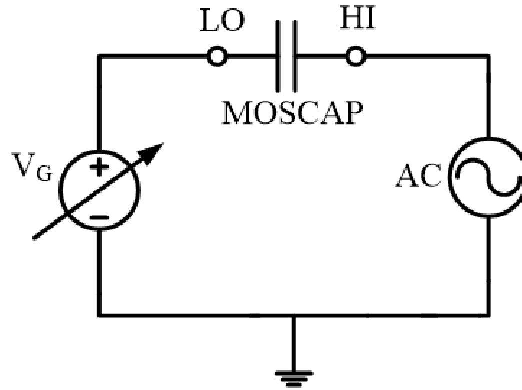


Fig. 4.15. Test bench for oxide capacitance (C_{ox}) measurement.

The oxide quality of SiC MOSFET gate is poor due to the presence of interface trapped charge and fixed oxide charge. Thus, the accuracy of the capacitance measurement is strongly

influenced by the frequency of the ac signal and other test parameters. In Table 4.7, an optimum range of test parameter values are listed.

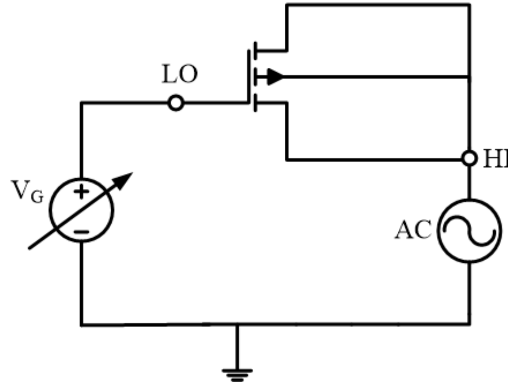


Fig. 4.16. Test bench for total gate capacitance ($C_{g\text{-}dsb}$) measurement.

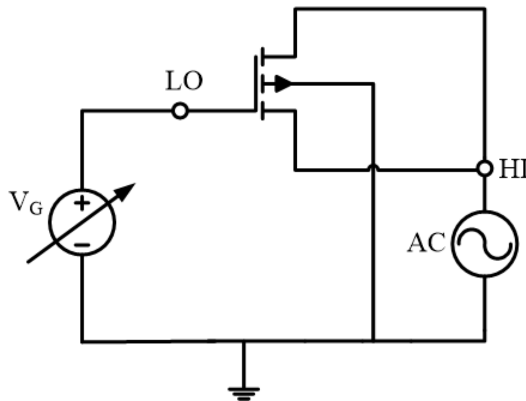


Fig. 4.17. Test bench for overlap capacitance and intrinsic gate-to-drain/source ($C_{g\text{-}ds}$) measurement.

Table 4.7. Parameter values for optimum MOSFET C-V characterization.

Test Parameter Name	Optimum Range of the Parameter Value (unit)
Hold time	0.5 – 1 (sec)
Sweep Delay Time	0.5 – 1 (sec)
Presoak voltage	Start voltage of the sweep range
Magnitude of the ac signal	50 – 100 (mV)
Frequency of the ac signal	50 – 100 (kHz)
Measured ac current limit	30 (µA)
Measurement speed	Quiet

4.3.2 Diode C-V Characterization

The parasitic body diode of the SiC MOSFET has bottom wall and side wall junction capacitances. The diode must be reverse biased while measuring the capacitance. Voltages ranging from 2V to -15V with a step of -0.1V was applied at the anode terminal (connected to HI) of the diodes and the small ac signal was applied at the cathode. The diode capacitance was measured at 25 ° C, 100 ° C, 200 ° C and 300 ° C.

4.3.3 Best Practices of C-V Measurement

A good C-V measurement is very challenging as the accuracy depends on a number of measurement conditions, cable parasitics and probe station setup. Some guidelines for accurate C-V characterization are outlined below:

- Outer conductors of the co-axial cables must be shorted in order for the ac signal to get a return path, since the ac ammeter is referenced to outer conductor of the 'LOCUR' co-axial cable. Below 100 kHz, shorting them is not very important because at those frequencies, the inductive reactance is not high. But above 1MHz the shorting becomes very important.
- For measuring leaky gate dielectrics, if the dissipation factor is in the range of 10 to 50, increase the frequency for Cp-Gp (MOSCap) model. Decrease the frequency for Cs-Rs model (diode).
- Instead of choosing auto range of 'Measure I', select a fixed range depending on the test frequency and approximate value of the device capacitance.
- Choose 'quiet' for getting better noise free measurements, for getting even better result choose 'custom' with large 'Filter Factor (3)' and 'PLC (10)' (power line cycles).

- To choose the delay times for a C-V sweep:
  - Step an applied voltage using the Sampling Mode.
  - Use initial conditions of Hold Time=0, Sweep Delay Time =0, and PreSoak V=0.
  - Plot the capacitance as a function of time.
  - Observe the settling time from the graph.
  - Use this settling time as the Hold Time for the initial applied voltage and/or as the Sweep Delay Time applied at each step in the sweep.
  - For the MOSFET capacitor measurement, apply Dual Sweep and observe the hysteresis, choose suitable 'Hold Time' and 'Delay Time' until no hysteresis is observed.
- Offset Compensation:
  - Use Open Compensation for small capacitance (< 40pF) measurement.
  - Use Short Compensation for large capacitance (> 1nF) measurement.
  - Load compensation is never needed.
- Cable length is very important, because it affects the phase of the signals as there is always a propagation delay of the signals along the cable. Use the Keithley red SMA cables that come with the unit or an equivalent.
- Grounded guard is used in the ac impedance measurement. Guard is the outer shield of the SMA cable.
- Run the kelvin point as close as possible to the sample device and short the shields as close as possible to the probe tips.

- Connect the chuck to the shield of the co-axial cables, if possible. In most cases, the residual capacitance from the pad to the chuck is insignificant, but if any anomaly in the C-V curve is observed, chuck connection becomes a concern.
- If bias is provided by the SMU, at higher frequencies, the ac impedance of the traix cable and SMU become significant. In that case keep the frequency below 1MHz.
- Connect CVL to the pad which has lowest residual capacitance to the chuck (highest isolation from the chuck).
- The measurement can be erroneous due to following cabling problems:
    - Improper cable length which is responsible for generating error in the phase measure.
    - Improper impedance which might occur if the Keithley red cables are not used.
    - Improper shield connections (not connected or not connected close enough to the DUT).
    - Bent, crimped or flattened cables (more critical at higher test frequencies).
    - SMA cable connectors not connected tight enough to the test fixture.

If the C-V measurement is not satisfactory, following troubleshooting method can be applied:

- Use the tools available in KITE: Offset Corrections, Confidence Check, Status Information.
- Ensure proper settings in KITE: sweep delay times, test frequency, ac drive voltage, dc source voltage etc.
- Ensure good DUT and proper contact to DUT: Use Confidence Check to verify.

- For measuring low capacitance: use Open Correction, high test frequency (100kHz, 1MHz), Quiet mode, guard (if applicable), lowest current (or auto range), add sufficient sweep delay time for settling.
- For higher capacitance: Use Short Correction, low test frequency (<10kHz)
- If the measured capacitance is found to be too high compared to the expected capacitance value, following things should be tried:
    - Cabling and connection can affect the capacitance measurements – Perform Offset Correction and check the option in ITM, minimize stray capacitance by reducing the cable length if possible.
    - Capacitance might be higher due to light since electrons absorb energy from the light and increase the carrier generation rate – Turn off light or close lid.
    - Unwanted capacitance from other terminals might affect measurement – Use the guard.
    - DUT might be shorted out - Try another DUT and use confidence check for verification.
- In case the measured capacitance is too low, follow the guidelines as outlined below:
    - Device is not in equilibrium – Increase delay time.
    - There is poor or no contact to device – Check probing if the capacitance is fF range and is expected to be much higher.
    - DUT is open - Try another device.
    - Coax cable shields are not connected – Connect shields near the DUT and reduce the test frequency.

- If the measured capacitance is suspected to be noisy, clean measurements can be obtained by following guidelines:
  - DUT or environment might be noisy – Use quiet or custom mode, increase or reduce the test frequency depending on the magnitude of capacitance and verify probe contact to the DUT.
  - DUT is not shielded electrostatically – Ensure proper test fixture shielding. The shield must be electrically connected to the coaxial shield.
- 'Tails' on the end of the C-V sweep can be eliminated by following these steps:
  - Device might not be in equilibrium – Set presoak voltage to the first voltage in the sweep and apply sufficient hold time to allow the DUT to charge up.
  - The device might have large leakage current – Try measuring the leakage current using the SMU and reduce the DC voltage until the leakage current is at a reasonable value.
- Always look at the dissipation factor D, if it is less than 0.1 then the measurement is good.

4.4 Summary

A detail description of the test structures used to characterize MOSFET and diode DC and C-V behavior are provided in this chapter. Basic concepts on how the measurements are made by the Keithley 4200 SCS and 4210 CVU are also reviewed. Appropriate bias ranges to make the current and capacitance measurement are listed and some useful guidelines for accurate device characterization at high temperature are also outlined.

CHAPTER 5 BSIM3 AND BSIM4 BASED MODELS OF SIC MOSFET

5.1 BSIM3V3 as a Foundation for SiC MOSFET Model Development

BSIM3v3 and BSIM4 have been by far the most popular MOSFET compact models in the semiconductor industry and are widely used for CMOS analog, mixed signal, RF and monolithic power integrated circuit design in micron, sub-micron and sub-100 nm process nodes. To emphasis the ubiquity of BSIM models in the integrated circuit world, it is worth mentioning a quotation from the cover page of a book written on BSIM4 by W. Liu and C. Hu, "BSIM, in the year of 2009 alone, was used to design about one hundred million million million (10^{20}) MOS transistors, which were shipped in about one hundred million (10^{8}) 12-inch equivalent silicon wafers worldwide". BSIM (**B**erkeley **S**hort-Channel **I**GFET **M**odel) is a family of MOSFET compact models developed by the University of California at Berkeley. Many students, professors and industry experts were involved in developing and maturing the models. To develop the compact models for SiC MOSFET which is the main part of this dissertation, BSIM3V3 was adopted as the fundamental building block. A few reasons among the many for this adaptation are as follows:

- BSIM3V3 is a proven and widely used compact model for MOS device and has been a standard for decades in the IC design industry.
- The model is very robust and rarely has convergence issues even in very complicated analog and mixed signal circuit simulations such as sigma delta ADCs, phased locked loops etc.
- The parameter extraction and optimization method for BSIM3V3 is well defined and easy to implement.
- Although the basic current and charge equations are derived based on the device physics in BSIM3V3, the model is mostly empirical in nature and it is

straightforward to modify existing equations or include some new ones in the model. For a developing process, such as Raytheon HiTSiC, the flexibility of the foundation model is very necessary.

- Since BSIM3V3 is not extremely physical like EKV or PSP models, new device phenomena can easily be implemented semi-empirically even though the exact physics of the phenomena are not well understood.
- BSIM3V3 is partitioned into many different model parts and each part has its own model flag. It is very easy and convenient to choose relevant model parts depending on which application the compact model is intended to be used.
- Since BSIM3V3 has been used for many process nodes over many years, there are many resources available on the model development, parameter extraction, capabilities and limitations of the model. The resources can serve as helpful guidelines while developing a new model based on the BSIM model.

In the industry, a macro-modeling approach is usually used when new device characteristics are included in a compact model. Circuit components such as resistor, capacitor, dependent and independent voltage and current source are patched around the device symbol at different terminals and the new phenomena are implemented by defining the voltage and current relationships of the components. This technique has less flexibility as there are limitations on the extent of new content can be added to the model. The best way of incorporating new device effects into the model is to develop physics based equations of the effects and include them into the model code. Since BSIM3V3 is originally written in C, it is an extremely tedious task to modify the model code and thus the later approach of altering the model never found much popularity. Fortunately, at the University of Arkansas (UA), Verilog-A versions of the BSIM3V3 and BSIM4 model code

were implemented using a very useful modeling tool called Paragon. The tool was developed in the Mixed-Signal Computer-Aided Design (MSCAD) lab at the UA. A compact model can be implemented in a very structured manner using the tool and the code can be exported as a Verilog-A file.

BSIM3V3 is a threshold voltage based model and the model equations are derived based on a simplified solution of Poisson's equations under the appropriate approximations. Some salient features of the model are given below:

- Single equation for formulating current in subthreshold, moderate inversion, strong inversion, triode and saturation region.
- Single charge equation for accumulation, depletion and inversion region.
- BSIM3V3 is a charged based model which indicates that charge is always conserved at all operating conditions.
- Formulation of short channel and narrow width effects on threshold voltage.
- Multiple mobility models to accurately predict the mobility reduction due to vertical electric field emanating from the gate.
- Bias dependent source/drain parasitic resistance model.
- Accurate model of bulk charge effects on threshold voltage and drain-source saturation voltage.
- Physics based formulation of short channel effects and threshold voltage shift due to drain induced barrier lowering (DIBL).
- Velocity saturation model to take into account the lateral field related mobility reduction.

- Model formulation of channel length modulation (CLM).
- Short channel effect modeling in the presence of substrate current induced body effect (SCBE).
- Inclusion of a poly silicon gate depletion model into the current and charge equations.
- Model formulation of the substrate current due to impact ionization.
- Velocity overshoot models for sub-100 nm device.
- Formulation of inversion layer quantization effects in the charge equations.
- Multiple models of flicker and thermal noise.
- DC and C-V models of parasitic source/drain diodes.
- Empirical models for temperature scaling.
- Accurate physics based models for length and width scaling.
- Separate non-quasi static models for transient and small signal analysis.
- Equivalent distributed gate resistance scalable substrate resistance network models for high frequency (RF) circuit simulation.
- Compatible for statistical modeling as many BSIM3V3 model parameters coincide with the device parameters such as oxide thickness, channel length and width variation, doping concentration, parasitic drain-source resistance etc.

In the following section, the derivation of the BSIM3V3 model equations is briefly presented. Since the SiC CMOS process is not yet matured enough to be used in high speed, high performance, low noise analog, mixed signal and RF circuits, features such as the velocity overshoot model, gate and substrate resistance model, non-quasi static model and noise model

were not used in this work and their model formulation will not be described. An in-depth analysis and detail derivation of all the model equations can be found in [112]-[113].

5.2 Model Formulation in BSIM3V3

The model formulation of DC and C-V characteristics are described separately in following subsections. A brief overview of the modeling of the parasitic and secondary effects are also outlined.

5.2.1 Core Model Development of DC Characteristics

Before the formal derivation of the model equations is outlined, it is important to qualitatively describe the theory of operation of a MOSFET device. The gate terminal of the device is the control terminal and is always used as an input. The drain terminal is usually used as an output and the voltages at the gate and the drain terminals are referred to the source potential. It should be noted that the source and body (sometimes called back gate) terminals can also be used as inputs with the gate terminal being the reference. In this discussion, the source is always assumed as the reference for the sake of consistency. The bold-faced words with all capital letters indicate model parameters.

An important term which is frequently used to describe the MOSFET device of operation is flat band voltage (**VFB**). In a long channel MOSFET device with uniform doping density in the substrate, due to the difference between the metal and the semiconductor work functions as well as due to the presence of fixed oxide charge and interface trapped charge (if any), there will be charge accumulation on the gate and inside the semiconductor even if the voltage at the gate terminal is zero. The flat band voltage is defined as the amount of voltage which is needed at the gate to get rid of the already existing charge. From the energy band diagram point of view, at the

flat band voltage, there is no bending of the energy state in the semiconductor and the oxide hence the term is called flat band voltage. This quantity is usually negative for an NMOS device and positive for a PMOS device.

If the voltage at the gate is below the flat band voltage in an NMOS device, negative charge will be accumulated on the gate and positive holes will be amassed on the oxide-semiconductor interface. This region of operation is known as accumulation and the MOSFET is in off-state. When the gate voltage exceeds the flat band voltage, positive charge starts to accumulate at the gate and positive holes get depleted by the gate charge and thus the acceptor atoms are ionized and become negatively charged. This negative bound charge is responsible for the voltage drop at the surface which is commonly known as the surface potential (ϕ_S). If the gate voltage is further increased, more and more acceptor atoms become ionized and the surface potential keeps increasing and beyond a certain point the potential is big enough to attract electrons from the n-type source region. The gate voltage at which the surface begins to attract electron from the source is defined as the threshold voltage and this marks the onset of the inversion region. At the beginning of the inversion, the number of electrons increases exponentially within few thermal voltage of the gate bias and the region is often termed as the subthreshold. As the gate voltage further increases, more and more electrons accumulate at the interface and thus a channel is formed for current conduction. An electric field in the channel which can be created by applying a voltage difference between the source and the drain induces carrier transport through the drift mechanism. The current through the device increases linearly with the drain voltage as long as the voltage difference between the gate and drain remains greater than the threshold voltage. This region of device operation is known as the triode. When the voltage across the gate and the drain falls below

the threshold voltage, ideally the current can no longer increase and the device operates in the saturation region.

A simplified 2-D cross section of an NMOS when operating in strong inversion is shown in Fig. 5.1. The direction parallel to the channel from source to drain is the y-axis and the direction perpendicular to the channel is as the x-axis. $\phi(y)$ is defined as the surface potential at an arbitrary point in the channel with respect to the source potential and $\Phi_S(y)$ is the surface potential with respect to the body potential. V_{sb} is the voltage difference between the source and the body, V_{OX} is the voltage drop across the gate oxide and **VFB** is the flat band voltage. G, S, B and D are gate, source, body and drain terminals respectively. The gate charge is denoted by Q_G while Q_I is inversion charge and Q_B is depletion or bulk charge. It is assumed that there is no interface trapped charge and fixed oxide charge. From voltage balance condition (KVL), following equation can be written from Fig. 5.1:

$$\boldsymbol{V_{GB} = VFB + V_{OX} + \Phi_S} \qquad 5.1$$

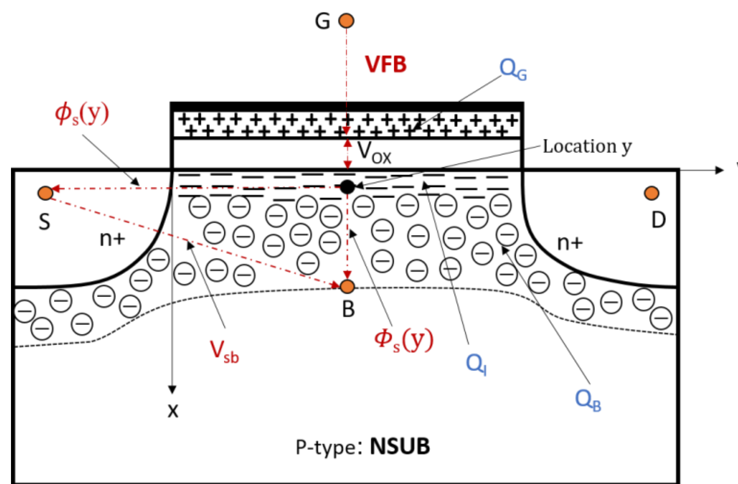


Fig. 5.1. Simplified cross section of an NMOS structure. The orange circles represent the device terminals (gate, source, drain, body) and the dark circle denotes an arbitrary point in the channel. The voltages and surface potential are identified by red lettered names. The blue lettered names indicate the charge in the device.

where Φ_S is the surface potential at the surface when drain-source voltage is zero.

From the charge neutrality condition, it can be written that:

$$\boldsymbol{Q'_G + Q'_C = 0} \quad 5.2$$

here Q'_G is the gate charge density (C/m^2) and Q'_C is the semiconductor charge density and is given by, $Q'_C = Q'_I + Q'_B$. Q'_I and Q'_B are the inversion and the depletion charge density respectively.

The gate oxide can be thought of as an insulator of a parallel plate capacitor and the voltage across the oxide V_{OX} can be written as a function of C_{OX} and Q'_G:

$$\boldsymbol{Q'_G = C'_{OX} \cdot V_{OX}} \quad 5.3$$

where C'_{OX} is the oxide capacitance per unit area.

The electron concentration n at point x can be written as [113]:

$$\boldsymbol{n(x) = n_O e^{\Phi_S(x)/\phi_t}} \quad 5.4$$

where n_o is the electron concentration at the surface. The hole concentration is given by:

$$\boldsymbol{p(x) = p_O e^{-\Phi_S(x)/\phi_t}} \quad 5.5$$

and p_o is the hole concentration at the semiconductor surface. The total charge density, $\rho(x)$ at point x in the semiconductor can be expressed as:

$$\boldsymbol{\rho(x) = q[p(x) - n(x) - NSUB]} \quad \mathbf{5.6}$$

where **NSUB** is the substrate doping concentration. From Eq. 3.1 and 5.6 the simplified Poisson's equation along the x-axis can be written as:

$$\frac{d^2\Phi}{dy^2} = \frac{-q}{\varepsilon_S}\left(p_O e^{\frac{-\Phi_S(x)}{\phi_t}} - n_O e^{\frac{\Phi_S(x)}{\phi_t}} - NSUB\right) \quad 5.7$$

Using the solution of Eq. 5.7 and using Eqs. 5.4 – 5.6, n(x), p(x), ρ(x), $\Phi_S(x)$ and Q'_C can be determined for a given Φ_S. Only Q'_C has a closed form solution and other quantities require numerical method for evaluation. The closed form solution of $Q'_C$is complex and contains many terms. The solution is given by:

$$Q'_C = \mp\sqrt{2q\varepsilon_S NSUB}\sqrt{\phi_t e^{\frac{-\Phi_S}{\phi_t}} + \Phi_S - \phi_t + e^{\frac{-2\Phi_F}{\phi_t}}\left(\phi_t e^{\frac{\Phi_S}{\phi_t}} - \Phi_S - \phi_t\right)} \quad 5.8$$

where $2\Phi_F$ is twice the fermi potential and given by:

$$2\Phi_F = 2\phi_t ln\frac{NSUB}{N_i} \quad 5.9$$

In Eq. 5.8, the negative sign must be used when the device is in depletion or inversion ($\Phi_S > 0$) and a positive sign must be used when the device operates in accumulation ($\Phi_S < 0$). Using Eqs. 5.1, 5.2, 5.3 and 5.8, V_{GB} can be expressed as an implicit function of Φ_S and thus total channel charge can be calculated at a given V_{GB}. But the solution requires an iterative numerical method. Also, the inversion charge which is responsible for current conduction cannot be quantified. Several approximations are required to simplify the relationship between the channel charge and the gate-body voltage and to obtain a closed form expression. The approximations are as follows:

- The thickness of the inversion charge layer is zero. In another term, all the inversion charge is located at the interface and this is known as charge sheet approximation. Since the depletion width is much larger than the inversion layer thickness (usually

a few hundred angstroms), this is a valid approximation. Under this assumption, voltage drop across the inversion layer is zero and thus the voltage across the depletion layer is to equal the surface potential (Φ_S).

- When the device operates in accumulation or depletion region, the contribution of the free electrons can be neglected as their number is very small.
- In strong inversion, the surface potential (Φ_S) is fixed to twice the fermi potential ($2\Phi_F$). Since Φ_S varies very little with the change in V_{GB} when the device operates in strong inversion, it is also a valid assumption.
- In the depletion region, the mobile carrier concentration can be neglected compared to the ionized acceptor concentration.
- In the inversion region, the depletion width is fixed since the surface potential is assumed to be fixed.
- Φ_S is much smaller than $2\Phi_F$ in weak inversion or subthreshold.

Under these assumptions, it can be shown that:

Depletion charge: $$\boldsymbol{Q_B = -C_{OX}\gamma\sqrt{2\Phi_F - V_{bs} + V(y)}} \qquad 5.10$$

here $V(y)$ is the channel voltage with respect to the source and is equal to V_{DS} at the drain end. γ is known as the technology dependent body bias coefficient and given by:

$$\boldsymbol{\gamma = \frac{\sqrt{2\varepsilon_S qNSUB}}{C_{OX}}} \qquad 5.11$$

Inversion charge in strong inversion:

$$\boldsymbol{Q_I(y) = -C_{OX}\left[V_{GS} - VFB - 2\Phi_F - V(y) - \gamma\sqrt{2\Phi_F - V_{bs} + V(y)}\right]} \qquad \mathbf{5.12}$$

Taylor series expansions are used on the square-root term to simplify the expression and if the higher order terms are neglected, the expression becomes:

$$\boldsymbol{Q_I(y) = -C_{OX}[V_{GS} - V_{TH} - A_{bulk}V(y)]} \quad 5.13$$

where V_{TH} is the bias dependent threshold voltage of a long and wide channel MOS transistor and is given by:

$$\boldsymbol{V_{TH} = VTH0 + \gamma\left(\sqrt{2\Phi_F - V_{bs}} - \sqrt{2\Phi_F}\right)} \quad 5.14$$

where **VTH0** is the bias independent threshold voltage and is extracted from the measured data as a model parameter. A_{bulk} is known as the bulk charge coefficient and given by:

$$\boldsymbol{A_{bulk} = 1 + \frac{\gamma}{2\sqrt{2\Phi_F - V_{bs}}}} \quad \textbf{5.15}$$

Inversion charge in weak inversion or subthreshold:

$$\boldsymbol{Q_{subVth}(y) = Q_M e^{(V_{GS} - V_{TH})/(n\phi_t)} e^{(-A_{bulk}V(y))/(n\phi_t)}} \quad \textbf{5.16}$$

where Q_M represents the upper limit of the weak inversion charge and can be written as:

$$\boldsymbol{Q_M = -\frac{\gamma C_{OX}}{2\sqrt{2\Phi_F}}\phi_t} \quad \textbf{5.17}$$

In Eq. 5.16 the subthreshold swing parameter *n* is defined as the derivative of the surface potential with respect to the gate voltage at $\boldsymbol{2\Phi_F}$.

By applying a Taylor series to the second exponential in Eq. 5.16 and keeping the first two terms, Q_I and Q_{subVth} can be combined as total channel charge and given by:

$$\boldsymbol{Q_{ch}(y) = Q_{ch0}\left[1 - \frac{A_{bulk}}{V_{gsteff}}V(y)\right]} \quad \textbf{5.18}$$

By collecting terms from Eqs. 5.13 and 5.16 and performing some mathematical manipulations and simplifications, Q_{ch0} can be written as:

$$\boldsymbol{Q_{ch0} = -C_{OX}V_{gsteff}} \qquad \textbf{5.19}$$

where V_{gsteff} is defined in such a way that Q_{ch0} is dominantly Q_{subVth} when the gate voltage is below the threshold voltage and mostly Q_I when the gate voltage is above the threshold voltage and the formulation is carried out using a smoothing function. The formulation is shown below:

$$\boldsymbol{V_{gsteff} = \frac{2n\phi_t ln\left[1+exp\left(\frac{m^*\left(V_{gseff}-V_{TH}\right)}{n\phi_t}\right)\right]}{1+2n\frac{C_{oxeff}}{C_{dep0}}exp\left[-\frac{V_{gseff}-V_{TH}-2VOFF}{2n\phi_t}\right]}} \qquad \textbf{5.20}$$

where C_{oxeff} is the effective oxide capacitance per unit area and **VOFF** is a model parameter. V_{gse} in Eq. 5.20 is given by:

$$\boldsymbol{V_{gseff} = V_{gs} - V_{poly}} \qquad 5.21$$

where V_{poly} is the voltage drop across the depletion region formed in the polysilicon gate. V_{poly} becomes significant in a short channel process (sub-100 nm) because the poly depletion width is comparable to the gate oxide thickness in those process nodes. The expressions for V_{poly} can be found in [114].

Accurate optimization of the subthreshold swing parameter n is very important for the weak and moderate inversion region modeling and the parameter is determined by depletion capacitance (C_{dep}), oxide capacitance (C_{ox}), interface capacitance (**CIT**), body-to-source voltage (V_{bs}) and drain-to-source voltage (V_{ds}). The formulation of n is given by:

$$n = 1 + NFACTOR\frac{C_{dep}}{C_{oxeff}} + \frac{CIT}{C_{oxeff}} + \frac{CDSC + CDSCB \cdot V_{bseff} + CDSCD \cdot V_{DS}}{C_{oxeff}} \times \frac{0.5}{\cosh\left(DVT1 \times \frac{L_{eff}}{l_{c1}}\right) - 1} \quad \textbf{5.22}$$

where **NFACTOR**, **CIT**, **CDSC**, **CDSCB**, **CDSCD** and **DVT1** are model parameters.

In Eq. 5.20 C_{dep0} is related to Q_M and is given by:

$$C_{dep0} = \sqrt{\frac{q \cdot NSUB \cdot \varepsilon_S}{2\Phi_F}} \quad \textbf{5.23}$$

Once the channel charge is known, current through the channel can be found from the current density equation which is shown in Eq. 3.2. If the equation is applied along the direction of the channel (y-axis), current density of an NMOSFET can be written as [115]:

$$J_{ch}(y) = -q \cdot n(x, y)\mu_n(x, y)\frac{d\varphi_{fn}}{dy} \quad 5.24$$

where *n(x, y)* and $\mu_n(x, y)$ is the electron density and mobility respectively at an arbitrary point *(x, y)* inside the channel. φ_{fn} is the quasi-Fermi potential of electrons in the channel and combines the drift and diffusion carrier transport. The difference between source end φ_{fn} and drain end φ_{fn} causes the charge carriers to drift and diffuse across the channel. Total current in the channel can be found by integrating Eq. 5.24 over the channel width, channel length (y-axis) and x-axis. By assuming a constant mobility along the x-axis and uniform current density over the channel width, total channel current can be written as:

$$I_{ch} = -\frac{W_{eff}}{L_{eff}}\int_0^{V_{ds}}[Q_{ch}(y)\mu_n(y)]dV(y) \quad 5.25$$

where the channel charge can be calculated as:

$$Q_{ch} = \int_0^{\infty}[qn(x, y)]dx \quad 5.26$$

and φ_{fn} is related to *V(y)* as follows:

$$\boldsymbol{\varphi_{fn} = V(y) - V_{bs}} \qquad 5.27$$

Eq. 5.25 includes double integration and requires a numerical method to find the solution. A generalized solution of the equation can be found by using the Pao-Sah model [116]. The charge sheet approximation simplifies the process of finding the solution but still requires numerical iteration [117]. In BSIM3V3, using the charge expression from Eq. 5.18 and integrating Eq. 5.25, the channel current is found to be:

$$\boldsymbol{I_{ch0} = \frac{W_{eff} C_{oxeff} V_{gsteff}}{L_{eff}\left(1+\frac{V_{ds}}{E_{sat} L_{eff}}\right)} \mu_{eff} V_{ds} \left[1 - \frac{A_{bulk}}{2(V_{gsteff}+2\phi_t)} V_{ds}\right]} \qquad \mathbf{5.28}$$

The following mobility equation is used in the derivation of Eq. 5.28:

$$\boldsymbol{\mu_n(y) = \frac{\mu_{eff}}{1+\frac{E(y)}{E_{sat}}}} \qquad \mathbf{5.29}$$

where *E(y)* is the electric field in the channel and is equal to the gradient of the channel voltage *V(y)*, μ_{eff} is the effective mobility, and E_{sat} is the longitudinal critical electric field beyond which the velocity of the carriers begins to saturate. Eq. 5.28 is the core model used for drain current calculation in BSIM3v3 and the drain current is called the intrinsic channel current. The equation was derived without considering the effects of drain/source parasitic resistance. BSIM3V3 includes the drain/source diffusion resistance in two ways: 1) introducing new nodes at the internal drain and source nodes and connecting the related resistances at the respective nodes and 2) including the combined effects of the drain/source resistances in Eq. 5.28. The current calculated by the later approach is called the extrinsic channel current and is given by:

$$I_{ch} = \frac{I_{ch0}}{1+\frac{R_{ds}(V)\cdot I_{ch0}}{V_{ds}}} \qquad \textbf{5.30}$$

The channel current equation as shown in Eq. 5.30 is only valid for triode or linear region of the MOSFET. If the drain source voltage is increased beyond a certain limit, the drain current and carrier velocity start to saturate. The carrier velocity v is related to the longitudinal electric field $E(y)$ as:

$$v = \mu_n(y)E(y) = \frac{\mu_{eff}}{1+\frac{E(y)}{E_{sat}}}E(y) \qquad \textbf{5.31}$$

which states that if the longitudinal field $E(y)$ is smaller than the critical field E_{sat}, the velocity increases linearly with $E(y)$ but if $E(y)$ is greater than E_{sat}, the carrier velocity saturates at a value equal to the model parameter **VSAT**. The relationship between E_{sat} and **VSAT** is given by:

$$E_{sat} = \frac{2\cdot VSAT}{\mu_{eff}} \qquad \textbf{5.32}$$

where **VSAT** is extracted from the measured data. **VSAT** is a temperature dependent parameter and the temperature effect is modeled empirically as follows:

$$VSAT(Temp) = VSAT(TNOM) + AT\times\left(\frac{Temp+273.15}{TNOM+273.15} - 1\right) \qquad 5.33$$

where **TNOM** is the nominal temperature, Temp is the operating temperature and AT is the model parameter.

The drain-source voltage at which the current saturates is denoted as V_{dsat} and is given by:

$$V_{dsat} = \frac{E_{sat}L_{eff}(V_{gsteff}+2\phi_t)}{A_{bulk}E_{sat}L_{eff}+V_{gsteff}+2\phi_t} \qquad \textbf{5.34}$$

and can be used to calculate the saturation current if it is assumed that the drain-source parasitic resistance is zero. In the extrinsic case where there is a finite amount of drain-source resistance, V_{dsat} can be written as:

$$V_{dsat} = -\frac{b+\sqrt{b^2-4ac}}{2a} \qquad 5.35$$

And a, b and c are:

$$a = A_{bulk}^2 W_{eff} VSAT C_{oxeff} R_{DS} + \left(\frac{1}{\lambda} - 1\right) A_{bulk} \qquad 5.36$$

$$b = -\left[\left(V_{gsteff} + 2\phi_t\right)\left(\frac{2}{\lambda} - 1\right) + A_{bulk} E_{sat} L_{eff} + 3A_{bulk}\left(V_{gsteff} + 2\phi_t\right) W_{eff} VSAT C_{oxeff} R_{DS}\right] \qquad 5.37$$

$$c = \left(V_{gsteff} + 2\phi_t\right) E_{sat} L_{eff} + 2\left(V_{gsteff} + 2\phi_t\right)^2 W_{eff} VSAT C_{oxeff} R_{DS} \qquad 5.38$$

In Eq. 5.36 and 5.37, λ is given by:

$$\lambda = \mathrm{A2} + \mathrm{A1} \cdot V_{gsteff} \qquad 5.39$$

where **A1** and **A2** are model parameters and are extracted as such that the value of λ attains physically meaningful values between 0 to 1.

Once V_{dsat} is known, a smoothing function is introduced in BSIM3V3 to define effective drain-to-source voltage V_{dseff} as shown below:

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - DELTA + \sqrt{\left(V_{dsat} - V_{ds} - DELTA\right)^2 + 4 \cdot DELTA \cdot V_{dsat}}\right) \qquad 5.40$$

According to Eq. 5.40, V_{dseff} attains the value of V_{ds} if the device operates in the linear region and is equal to V_{dsat} in the saturation region. Using the model parameter **DELTA**, the softness of the transition of V_{dseff} from linear to saturation region can be adjusted. The MOSFET drain current for all regions can be calculated by Eq. 5.30 if V_{ds} is replaced with V_{dseff} in the equation and in Eq. 5.28. The extrinsic drain current equation for all regions is:

$$I_{ch} = \frac{I_{ch0}}{1+\frac{R_{ds}(V)\cdot I_{ch0}}{V_{dseff}}} \quad 5.41$$

Where I_{ch0} is given by:

$$I_{ch0} = \frac{W_{eff}C_{oxeff}V_{gsteff}}{L_{eff}\left(1+\frac{V_{dseff}}{E_{sat}L_{eff}}\right)}\mu_{eff}V_{dseff}\left[1-\frac{A_{bulk}}{2(V_{gsteff}+2\phi_t)}V_{dseff}\right] \quad \mathbf{5.42}$$

5.2.2 Modeling of the Secondary DC Effects

The threshold voltage of a MOSFET might change due to a variety of reasons such as charge sharing, drain induced barrier lowering (DIBL), non-uniform lateral and vertical doping concentration in the channel, narrow width, short channel, small dimension, pocket implant etc. BSIM3V3 models this effects by including physics based equations in the threshold voltage equation as shown in Eq. 5.14.

Threshold voltage shift due to short channel – As the length of the channel decreases in a MOSFET, the influence of bulk charge from the drain side on the channel potential increases at a given drain voltage and thus reduces the threshold voltage. This is known as V_{TH} roll-off and the amount of shift in threshold voltage is given by [118]:

$$\Delta V_{TH}(roll-off) = \left[\frac{0.5DVT0}{cosh\left(DVT1\frac{L_{eff}}{l_{c1}}\right)-1}\right](V_{bi}-2\Phi_F) \quad \mathbf{5.43}$$

here **DVT0** and **DVT1** are model parameters, l_{c1} is the characteristics length and V_{bi} is the built-in potential. l_{c1} is related to the depletion width as:

$$\boldsymbol{l_{c1} = \sqrt{\frac{\varepsilon_S X_{dep} TOXE}{\varepsilon_{OX}}\left(1 + DVT2V_{bseff}\right)}} \qquad \textbf{5.44}$$

where ε_{OX} is the permittivity of the gate oxide, X_{dep} is the depletion width, **TOXE** is the equivalent electrical oxide thickness and **DVT2** is a model parameter. X_{dep} is given by the following equation:

$$\boldsymbol{X_{dep} = \sqrt{\frac{2\varepsilon_S\left(2\Phi_F - V_{bseff}\right)}{qNSUB}}} \qquad \textbf{5.45}$$

In Eq. 5.44, V_{bseff} is the effective body-to-source voltage and is defined to have values within a defined range using a smoothing function to avoid numerical issues.

$$\boldsymbol{V_{bseff} = v_{bc} + \frac{(V_{bs} - v_{bc} - \delta_1) + \sqrt{(V_{bs} - v_{bc} - \delta_1)^2 - 4\delta_1 v_{bc}}}{2}; \qquad \delta_1 = 0.001} \qquad \textbf{5.46}$$

Effect of DIBL on threshold voltage – At a given channel length, if the voltage at the drain is increased, the energy barrier at the source decreases and thus the channel is formed at a relatively lower gate voltage. In other words, the threshold voltage becomes smaller due to the drain induced barrier lowering. The DIBL effect is more prominent in short channel devices. The amount of shift in threshold voltage is given by:

$$\boldsymbol{\Delta V_{TH}(DIBL) = \left[\frac{0.5}{\cosh\left(DSUB\frac{L_{eff}}{l_{c0}}\right) - 1}\right]\left(ETA0 + ETAB \cdot V_{bseff}\right)V_{ds}} \qquad \textbf{5.47}$$

where **ETA0**, **ETAB** and **DSUB** are the parameters which model drain voltage, body voltage and length dependencies respectively.

In Eq. 5.35, l_{c0} is the characteristics length at zero body-to-source voltage and can be written as:

$$\boldsymbol{l_{c0}} = \sqrt{\frac{\varepsilon_S X_{dep} TOXE}{\varepsilon_{OX}}} \qquad \textbf{5.48}$$

Threshold voltage shift due to narrow width – If the width of the MOSFET channel is too narrow, the fringing field along the channel edges is comparable to the effective vertical field and more gate voltage is required to invert the channel as the fringing field terminates in the source or drain region. This indicates that the threshold voltage is higher in a narrow device than that of a wide device. The increase in threshold voltage due to narrow width is given by:

$$\Delta V_{TH}(narrow - width) = \left[\frac{TOXE}{W0 + W_{eff}}\right]\left(K3 + K3B \cdot V_{bseff}\right) 2\Phi_F \qquad \textbf{5.49}$$

where **W0**, **K3** and **K3B** are model parameters.

In a modern CMOS process, shallow trench isolation (STI) technology is used to isolate the device's active area and the channel is surrounded by a trench oxide. In such a process, it is found that the threshold voltage increases for a narrow device if the channel length is smaller. The threshold voltage increase due to the smaller dimension of the MOSFET in a modern process is:

$$\Delta V_{TH}(small - size) = \left[\frac{0.5 \cdot DVT0W}{\cosh\left(DVT1W \frac{L_{eff} \cdot W_{eff}}{l_{cw}}\right) - 1}\right]\left(V_{bi} - 2\Phi_F\right) \qquad \textbf{5.50}$$

Effects of non-uniform substrate doping on threshold voltage – The core drain current equation as shown in Eq. 5.28 was derived under the assumption of a uniform substrate doping concentration. But if the doping concentration is too high, the channel mobility decreases due to the increased scattering from the ionized impurity atoms. On the other hand, if the doping

concentration is too low, the depletion width becomes too big at a relatively smaller drain voltage and DIBL and V_{TH} roll-off effects become significantly stronger. To alleviate this, a higher doping concentration is used in a region close to the source and drain and a little further away from the interface and thus the doping concentration becomes non-uniform. A typical vertical and lateral doping profile is shown in Fig. 5.2 (a) and (b) respectively.

The non-uniformity of the doping concentration alters the basic threshold voltage equation which as shown in Eq. 5.14 and the equation should be modified as:

$$V_{TH} = VTH0 + K1\left(\sqrt{2\Phi_F - V_{bseff}} - \sqrt{2\Phi_F}\right) - K2 \cdot V_{bseff} \qquad \textbf{5.51}$$

where **K1** and **K2** are body effect models parameters. If either **K1** or **K2** or both are not specified in the model card, BSIM3V3 determines the value of these parameters based on the permittivity of the substrate and the oxide, equivalent substrate doping concentration, oxide thickness, depth of the delta doping and maximum body bias.

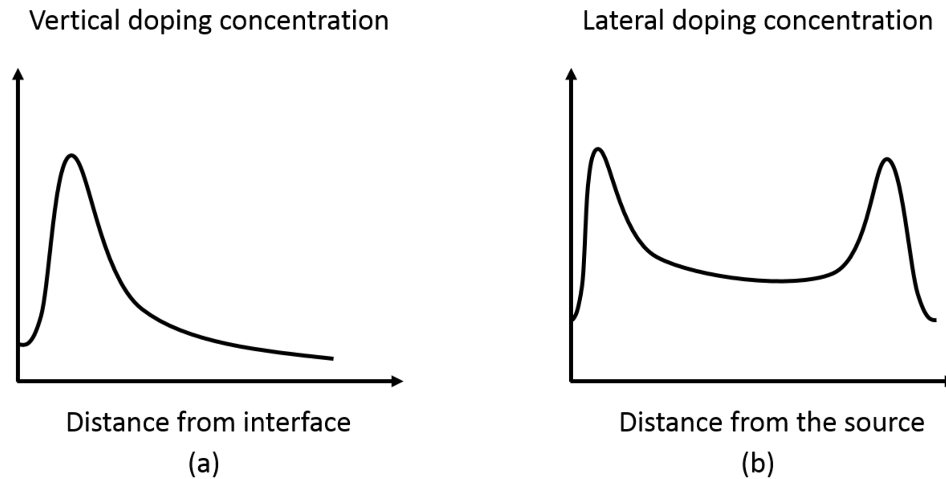


Fig. 5.2. (a) Vertical doping profile and (b) lateral doping profile in a MOSFET channel.

Since the substrate region at the drain and source is heavily doped, the equivalent doping concentration in the channel increases. It is found that the higher the doping concentration the higher the threshold voltage as the length of the device decreases. This is known as the reverse short channel effect and the combination of short channel effect and reverse short channel effect introduces a peak in the threshold voltage vs. channel length curve as shown in Fig. 5.3.

The amount of threshold voltage shift due to the reverse short channel effect can be quantified as:

$$\Delta V_{TH}(reverse_short_channel) = K1\left(\sqrt{1+\frac{NLX}{L_{eff}}}-1\right)\sqrt{2\Phi_F} \qquad 5.52$$

where **NLX** is model parameter.

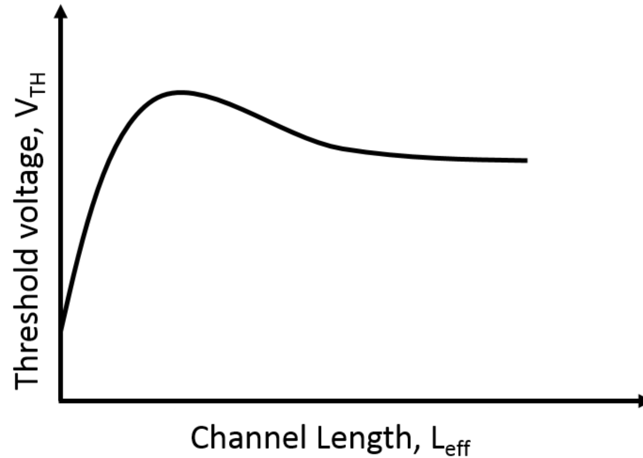


Fig. 5.3. Combined effects of lateral non-uniform substrate doping concentration and short channel on threshold voltage.

Temperature dependence of threshold voltage – Threshold voltage is a complex function of surface and Fermi potential, band-gap, built-in potential and intrinsic carrier concentration. These parameters are temperature dependent and the best approach of modeling temperature effects on threshold voltage is to model individual parameters separately and include them in the

threshold voltage equation. But this approach is not realistic as it will increase the model complexity significantly and thus increase the simulation time. BSIM3V3 models the effects of temperature on threshold voltage empirically and the model is given by:

$$\Delta \boldsymbol{V_{TH}(Temp)} = \left(\boldsymbol{KT1} + \frac{\boldsymbol{KT1L}}{\boldsymbol{L_{eff}}} + \boldsymbol{KT2} \cdot \boldsymbol{V_{bseff}} - \mathbf{1}\right)\left(\frac{\boldsymbol{Temp}}{\boldsymbol{TNOM}} - \mathbf{1}\right) \qquad \mathbf{5.53}$$

where **KT1**, **KT1L** and **KT2** are model parameters.

Modeling of the finite output resistance in the saturation region – For a long channel MOSFET, the drain current can be accurately modeled with Eq. 5.41 and 5.42. But as the length of the channel becomes smaller, several secondary effects arise and contribute to a finite output resistance which cannot be modeled with these equations. Channel length modulation is one of the secondary effects and as the name suggests L_{eff} decreases with the increase in drain-to-source voltage in the saturation region. The reduction in channel length causes the increase in drain current and the modified current equation including other secondary effects can be written as:

$$\boldsymbol{I_{ch}} = \frac{\boldsymbol{I_{ch0}}}{1+\frac{\boldsymbol{R_{ds}(V)\cdot I_{ch0}}}{\boldsymbol{V_{dseff}}}}\left(\mathbf{1} + \frac{\boldsymbol{V_{ds}-V_{dseff}}}{\boldsymbol{V_A}}\right)\left(\mathbf{1} + \frac{\boldsymbol{V_{ds}-V_{dseff}}}{\boldsymbol{V_{ASCBE}}}\right) \qquad 5.54$$

where V_A is known as the early voltage and is defined as the x-axis intercept of the tangent drawn on the MOSFET I-V output curve in the saturation region. V_A has three components – one arises from the effects of the saturation velocity, one from the drain induced barrier lowering and the other from the channel length modulation and is given by:

$$\boldsymbol{V_A} = \boldsymbol{V_{Asat}} + \boldsymbol{V_{ADIBL-CLM}} \qquad \mathbf{5.55}$$

here V_{Asat} is:

$$V_{Asat} = \frac{E_{sat}L_{eff}+V_{dsat}+2V_{gsteff}W_{eff}VSATC_{oxeff}R_{DS}}{\frac{2}{\lambda}-1+R_{DS}C_{oxeff}W_{eff}A_{bulk}VSAT} \times \left[1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff}+2\phi_t)}\right] \quad \textbf{5.56}$$

and $V_{ADIBL-CLM}$ is:

$$V_{ADIBL-CLM} = \left(1 + \frac{V_{gsteff}PVAG}{E_{sat}L_{eff}}\right) \times \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}}\right)^{-1} \quad 5.57$$

where **PVAG** is a model parameter. V_{ACLM} and V_{ADIBL} can be written as follows:

$$V_{ACLM} = \begin{cases} \frac{A_{bulk}E_{sat}L_{eff}+V_{gsteff}}{PCLMA_{bulk}E_{sat}L_{itl}}(V_{ds} - V_{dseff}) & if\ V_{ds} - V_{dseff} > 10^{-10}; \\ 5.834617425 \times 10^{14} & if\ otherwise. \end{cases} \quad 5.58$$

$$V_{ADIBL} = \begin{cases} \frac{(V_{gsteff}+2\phi_t)}{\theta_{rout}(1+PDIBLCB \cdot V_{bseff})} \times \left(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat}+V_{gsteff}+2\phi_{t}{}_{dseff}}\right) & if\ \theta_{rout} \geq 0; \\ 5.834617425 \times 10^{14} & if\ \theta_{rout} < 0. \end{cases} \quad 5.59$$

where **PCLM** and **PDIBLCB** are model parameters. L_{itl} in Eq. 5.58 is given by:

$$L_{itl} = \sqrt{\frac{\varepsilon_S}{\varepsilon_{OX}} TOX \cdot XJ} \quad \textbf{5.60}$$

And θ_{rout} in Eq. 5.59 is:

$$\theta_{rout} = PDIBLC1 \times \left[exp\left(-DROUT\frac{L_{eff}}{2l_{c0}}\right) + 2 \cdot exp\left(-DROUT\frac{L_{eff}}{l_{c0}}\right)\right] + PDIBLC2 \quad \textbf{5.61}$$

here **PDIBLC1**, **PDIBLC2** and **DROUT** are model parameters.

V_{ASCBE} is another early voltage contributed by the substrate current induced body bias effect and causes large increase in drain current when the drain-to-source voltage is close to the supply voltage. The equation for V_{ASCBE} is given by:

$$V_{ASCBE} = \begin{cases} \frac{L_{eff}}{PSCBE2} exp\left(\frac{PSCBE1 \cdot L_{itl}}{V_{ds} - V_{dseff}}\right) & if\ PSCBE2 > 0; \\ 5.834617425 \times 10^{14} & if\ otherwise. \end{cases} \qquad 5.62$$

PSCBE1 and **PSCBE2** in Eq. 5.62 are model parameters.

Bulk charge effects – The bulk charge coefficient A_{bulk} as shown in Eq. 5.15 was derived assuming a long channel and a uniform channel doping profile for zero drain-source voltage. But as the drain-source voltage varies, the threshold voltage and the inversion charge across the channel also vary. A more detail model than the one presented in Eq. 5.15 is required for better accuracy. BSIM3V3 takes into account the effects of channel length and width, gate bias and body bias and includes more model parameters in the formulation of bulk charge coefficient. The equation is given by:

$$A_{bulk} = \left\{1 + \frac{K1}{2\sqrt{2\Phi_F - V_{bseff}}}\left[\frac{A0 \cdot L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}} \times \left(1 - AGS \cdot V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}}\right)^2\right) + \frac{B0}{W_{eff} + B1}\right]\right\} \times \frac{1}{1 + KETA \cdot V_{bseff}} \qquad \mathbf{5.63}$$

where **A0** models the length dependency, **B0** and **B1** incorporates the width dependency and **AGS** and **KETA** model the effects of gate bias and body bias respectively.

Effective mobility – The mobility in a MOSFET channel is influenced by different scattering mechanisms. The ionized impurity atoms have charge and scatter the free carriers when they are in motion. This is known as the Coulomb scattering. The atoms in the substrate material vibrate in the lattice by absorbing thermal energy and act as scattering centers. The carriers lose energy and slow down when they traverse through these centers and thus mobility is reduced. This mechanism of mobility reduction is called phonon scattering. The free charge carriers also lose

energy when they collide with the interface and the reduction of the mobility is significant in presence of surface roughness. The metal-semiconductor interface is a material discontinuity in a MOS device along the path of the carrier transport and if the lattice mismatch at the interface is not tightly controlled the device performance will degrade due to the smaller number of inversion charge carrier and mobility reduction. There are three mobility models in BSIM3V3 and any of the models can be selected by assigning either 1, 2 or 3 to the model parameter **MOBMOD**.

For **MOBMOD** = 1, the model is:

$$\mu_{eff} = \frac{U0(Temp)}{(UA+UC\cdot V_{bseff})\left(\frac{V_{gsteff}+2\phi_t}{TOX}\right)+UB\left(\frac{V_{gsteff}+2\phi_t}{TOX}\right)^2} \quad \textbf{5.64}$$

For **MOBMOD** = 2, the model is:

$$\mu_{eff} = \frac{U0(Temp)}{(UA+UC\cdot V_{bseff})\left(\frac{V_{gsteff}}{TOX}\right)+UB\left(\frac{V_{gsteff}}{TOX}\right)^2} \quad \textbf{5.65}$$

For **MOBMOD** = 3, the model is:

$$\mu_{eff} = \frac{U0(Temp)}{\left[UA\left(\frac{V_{gsteff}+2\phi_t}{TOX}\right)+UB\left(\frac{V_{gsteff}+2\phi_t}{TOX}\right)^2\right](1+UC\cdot V_{bseff})} \quad \textbf{5.66}$$

where **U0, UA**, **UB** and **UC** are model parameters. Mobility is strongly influenced by temperature and the dependency is modeled by empirical equations of the mobility related model parameters. The formulations are as follows:

$$U0(Temp) = U0(TNOM)\times\left(\frac{Temp+273.15}{TNOM+273.15}\right)^{UTE} \quad 5.67$$

$$UA(Temp) = UA(TNOM) + UA1\times\left(\frac{Temp+273.15}{TNOM+273.15} - 1\right) \quad \textbf{5.68}$$

$$UB(Temp) = UB(TNOM) + UB1 \times \left(\frac{Temp+273.15}{TNOM+273.15} - 1\right) \qquad \textbf{5.69}$$

$$UC(Temp) = UC(TNOM) + UC1 \times \left(\frac{Temp+273.15}{TNOM+273.15} - 1\right) \qquad \textbf{5.70}$$

here **UTE**, **UA1**, **UB1** and **UC1** are model parameters.

Bias dependency of drain/source parasitic resistances – The parasitic resistances of the drain/source region of a MOSFET device consist of three components – metal-to-source/drain contact resistance, diffusion resistance of the heavily doped drain/source and diffusion resistance of the extended low doped drain/source (LDD) regions. The drain/source resistance for the extrinsic case in BSIM3V3 is calculated as:

$$R_{DS} = \frac{RDSW\left[1+PRWG(V_{GS}-V_T)+PRWB(\sqrt{2\Phi_F-V_{BS}} - \sqrt{2\Phi_F})\right]}{\left(10^6 \times W_{eff}\right)^{WR}} \qquad \textbf{5.71}$$

where **RDSW** is a model parameter and is extracted from the drain-source resistance per µm of gate width, **PRWG** is the gate bias coefficient, **PRWB** is the body bias coefficient and **WR** is the exponent of the effective device width. **RDSW** also depends on temperature and the dependency is given by:

$$RDSW(Temp) = RDSW(TNOM) + PRT \times \left(\frac{Temp+273.15}{TNOM+273.15} - 1\right) \qquad 5.72$$

where **PRT** is a model parameter.

Modeling of the body diode DC characteristics – The parasitic drain-to-body and source-to-body diodes are an integral part of the MOSFET. The diodes contribute to the substrate leakage current when the device is off and adds an additional current component to the drain current when it is on. The leakage current is proportional to the drain/source area and perimeter of the MOSFET.

In BSIM3V3, the body diode is modeled by the ideal exponential equation if the model parameter **IJTH** is equal to zero. The diode current I_{jDB} is:

$$\boldsymbol{I_{jDB} = \left\{I_{satDB}\left[exp\left(\frac{V_{BD}}{NJ\cdot\phi_t}\right) - 1\right] + GMIN\cdot V_{BD}\right.} \quad 5.73$$

where V_{BD} is the voltage across the body diode, **NJ** is the emission coefficient and a model parameter. $\boldsymbol{I_{satDB}}$ in Eq. 5.73 is the reverse saturation current and is given by:

$$\boldsymbol{I_{satDB} = \begin{cases} JS\times AD + JSSW\times PD & if\ the\ result \geq 0 \\ 10^{-14} & if\ AD\ and\ PD\ are\ both\ \leq 0 \\ 0 & if\ JS\times AD + JSSW\times PD < 0 \end{cases}} \quad \mathbf{5.74}$$

When the model parameter **IJTH** is set to a value greater than zero, the diode current follows the exponential relationship until the voltage across the diode is less than V_{IJTH}**.** V_{IJTH} is defined as the diode voltage at which the exponential diode current becomes equal to **IJTH** and can be found by:

$$\boldsymbol{V_{IJTH} = NJ\cdot\phi_t\cdot ln\left(\frac{IJTH}{I_{satDB}} + 1\right)} \quad \mathbf{5.75}$$

If the diode voltage is greater than V_{IJTH} and the model parameter IJTH is set to a positive value, the diode current is calculated using a linear relationship. The current equations for IJTH>0 is:

$$\boldsymbol{I_{jDB} = \begin{cases} I_{satDB}\left[exp\left(\frac{V_{BD}}{NJ\cdot\phi_t}\right) - 1\right] + GMIN\cdot V_{BD} & if\ V_{BD} < V_{IJTH} \\ IJTH + \frac{IJTH + I_{satDB}}{NJ}\times\frac{V_{BD} - V_{IJTH}}{\phi_t} + GMIN\cdot V_{BD} & if\ otherwise \end{cases}} \quad \mathbf{5.76}$$

Any negative value of IJTH is unrealistic and BSIM3V3 issues an error message when the model parameter is assigned to a value less than zero.

5.2.3 Intrinsic Charge Modeling

Although the best method for analyzing the transient characteristics of a device is to numerically solve the current continuity equation as shown in Eq. 3.3, it is not realistic for SPICE simulation due to large simulation time and poor convergence. BSIM3V3 uses closed form analytic equations of the device's terminal charges under the quasi-static assumption. Once the charge equations are derived, the time varying current of a node can be found by differentiating the terminal charge with respect to time. For example, the dynamic gate current $i_G(t)$ can be written as:

$$\boldsymbol{i_G(t) = \frac{d}{dt} Q_G\big(V_{GS}(t), V_{GD}(t)\big)} \qquad \textbf{5.77}$$

where $Q_G\big(V_{GS}(t), V_{GD}(t)\big)$ is the time varying charge at the gate node and source node is the reference. Eq. 5.77 can be accurately used to calculate the displacement current in the oxide capacitance if the DC leakage current through the oxide is zero. When the voltage at the gate is increased, more charge transports from the voltage source to the gate and accumulates on the metal plate and cannot penetrate through the oxide due to the large potential barrier. Under this circumstances, the quasi-static assumption is not violated. But the same argument cannot be applied for the drain charge. For example, let us assume that the transient drain current $i_D(t)$ can be written as:

$$\boldsymbol{i_D(t) = \frac{d}{dt} Q_D(t)} \qquad \textbf{5.78}$$

where $Q_D\big((t)\big)$ is the time dependent charge at the drain terminal. Eq. 5.78 cannot be correctly used to calculate the DC drain current without violating the quasi-static assumption. To find the constant DC current by the equation, the charge must increase linearly with respect to time even

though the voltages at all the terminals are fixed. It is a clear violation of the quasi-static assumption because under this assumption the charge only responds to the time variation of the node voltages without any delay. The aforementioned problem can be solved by defining an alternative transient drain current using the first moment technique [119]-[120]. By applying the technique, the drain current be written as:

$$\boldsymbol{i_D\big(V_{GS}(t), V_{GD}(t)\big) = I_D\big(V_{GS}(t), V_{GD}(t)\big) + \frac{\partial}{\partial t}\frac{W}{L}\int_0^L xQ_{ch}(x,t)dx} \quad 5.79$$

Where $Q_{ch}(x,t)$ is the quasi-static channel charge density as defined in Eq. 5.26, W and L are the channel width and length respectively. Eq. 5.79 dictates that the transient current is comprised of two components. The first component is a steady state current which continuously flows from the source contact to the channel and then to the drain and finally back to the source through the supply and thus completing a loop. The second component is the capacitive displacement current and only flows when there is a time variation in the drain charge $Q_D(t)$. Thus $Q_D(t)$ can be defined as:

$$\boldsymbol{Q_D(t) = \frac{W}{L}\int_0^L xQ_{ch}(x,t)dx} \quad 5.80$$

$Q_S(t)$ can also be calculated by applying the first moment technique and is given by:

$$\boldsymbol{Q_D(t) = \frac{W}{L}\int_0^L (L-x)Q_{ch}(x,t)dx} \quad 5.81$$

In BSIM3V3, the model formulation of gate charge, inversion charge and bulk charge are accomplished following a similar method as used in the DC equations derivation but the partitioning of the channel inversion charge into the drain and source charge are done by using the first moment technique. There are minor differences between some of the definitions used in the C-V charge equations from those used in the DC current equations and the differences are included

to add flexibility in parameter extraction and optimization. BSIM3V3 includes several C-V models and by assigning different values to the model parameter **CAPMOD**, different models can be selected. In this work, the C-V characteristics of SiC devices were optimized using the finite charge thickness capacitance model and can be selected by activating **CAPMOD** = 3 (In BSIM4, it is **CAPMOD** = 2).

Several smoothing functions are used to define various voltages in the BSIM3V3 charge model to avoid discontinuity and convergence issues. The body-to-source effective voltage in the C-V model is:

$$V_{bseffcv} = \begin{cases} V_{bseff} & if \quad V_{bseff} < 0 \\ 2\Phi_F - 2\Phi_F \frac{2\Phi_F}{2\Phi_F + V_{bseff}} & if \quad V_{bseff} \geq 0 \end{cases} \qquad \textbf{5.82}$$

where the definition of V_{bseff} is given in Eq. 5.46. It is noted from Eq. 5.82 that the effective body-to-source voltage is pinned to the constant surface potential used in strong inversion when the voltage is positive.

Although theoretically flat band voltage is bias dependent, the use of such a definition is found to cause convergence issues and thus a zero-bias flat band voltage is defined in BSIM3V3 to calculate the thickness of the accumulation and inversion charge:

$$V_{fbzb} = V_{TH}(V_{gs} = V_{ds} = V_{bs} = 0) - 2\Phi_F - K1\sqrt{2\Phi_F} \qquad \textbf{5.83}$$

The gate-to-body effective voltage which is necessary for the formulation of accumulation charge is defined in BSIM3V3 as:

$$V_{gbeffcv} = V_{gseff} - V_{bseffcv} \qquad \textbf{5.84}$$

The definition of V_{gseff} is shown in Eq. 5.21. A different definition of the flat band voltage than the one shown in Eq. 5.82 is used in the accumulation charge expression and is given as:

If $V_{fbcv} \geq 0$, then

$$\boldsymbol{V_{fbeffcv} = V_{fbcv} - \frac{1}{2}\left(V_{fbcv} - V_{gbeffcv} - \delta_3 + \sqrt{\left(V_{fbcv} - V_{gbeffcv} - \delta_3\right)^2 + 4 \cdot \delta_3 \cdot V_{fbcv}}\right)}$$

5.85

If $V_{fbcv} \geq 0$, then

$$\boldsymbol{V_{fbeffcv} = V_{fbcv} - \frac{1}{2}\left(V_{fbcv} - V_{gbeffcv} - \delta_3 + \sqrt{\left(V_{fbcv} - V_{gbeffcv} - \delta_3\right)^2 - 4 \cdot \delta_3 \cdot V_{fbcv}}\right)}$$

5.86

In Eqs. 5.85 and 5.86, V_{fbcv} is equal to the model parameter **VFBCV**. The effective gate-to-source voltage in the C-V model is different than the one used in the DC current equation and is given by:

$$\boldsymbol{V_{gsteffcv} = NOFF \cdot n \cdot \phi_t \cdot ln\left[1 + exp\left(\frac{V_{gseff} - V_{TH} - VOFFCV}{NOFF \cdot n \cdot \phi_t}\right)\right]} \quad \textbf{5.87}$$

where **NOFF** and **VOFFCV** are model parameters.

The bulk charge coefficient in the drain current equation is gate voltage dependent as shown in Eq. 5.63. In the C-V model, the dependency is removed from the coefficient to avoid unnecessary complexity and convergence issues. The new bulk charge coefficient can be written as:

$$\boldsymbol{A_{bulkcv} = A_{bulk0}\left[1 + \left(\frac{CLC}{L_{effcv}}\right)^{CLE}\right]} \quad \textbf{5.88}$$

where **CLC** and **CLE** are channel length dependent model parameters. A_{bulk0} in Eq. 5.88 is given by:

$$\boldsymbol{A_{bulk0}} = \left\{\mathbf{1} + \frac{\boldsymbol{K1}}{\mathbf{2}\sqrt{\mathbf{2}\boldsymbol{\Phi_F} - \boldsymbol{V_{bseff}}}}\left[\frac{\boldsymbol{A0 \cdot L_{eff}}}{\boldsymbol{L_{eff}} + \mathbf{2}\sqrt{\boldsymbol{XJ \cdot X_{dep}}}} + \frac{\boldsymbol{B0}}{\boldsymbol{W_{eff}} + \boldsymbol{B1}}\right]\right\} \times \frac{\mathbf{1}}{\mathbf{1} + \boldsymbol{KETA \cdot V_{bseff}}} \qquad \mathbf{5.89}$$

The drain-to-source saturation voltage for charge equations is defined as:

$$\boldsymbol{V_{dssatcv}} = \frac{\boldsymbol{V_{gsteffcv}}}{\boldsymbol{A_{bulkcv}}} \qquad \mathbf{5.90}$$

A similar smoothing function for effective drain-to-source voltage as used in the drain current equation is also used in the C-V model and is given by:

$$\boldsymbol{V_{dseffcv}} = \boldsymbol{V_{dssatcv}} - \frac{(\boldsymbol{V_{dssatcv}} - \boldsymbol{V_{ds}} - \boldsymbol{\delta_4})}{\mathbf{2}} + \sqrt{\frac{(\boldsymbol{V_{dssatcv}} - \boldsymbol{V_{ds}} - \boldsymbol{\delta_4})^2 + \mathbf{4} \cdot \boldsymbol{\delta_4} \cdot \boldsymbol{V_{dssatcv}}}{\mathbf{4}}} \qquad \mathbf{5.91}$$

In the derivation of DC current equations, it is assumed that the inversion charge is located at the oxide and semiconductor interface and the thickness of the inversion layer is zero. But in reality, from the energy band diagram in the substrate it is found that there is a quantum well at the interface and according to the solution of the Schrodinger equation there is a finite probability of the wave function penetration into the oxide. Thus, the peak of the inversion charge is no longer at the interface and the assumption of a zero-charge layer thickness becomes erroneous. This quantum mechanical phenomena are more pronounced in modern CMOS technology where the gate oxide thickness is very small (~ 1nm). Although the gate oxide in the SiC MOSFET is very thick (~ 40nm), the sheet charge approximation is not entirely accurate due to the presence of interface states. Some of the inversion charges get trapped within a few nm of the gate oxide and thus the peak of the inversion charge moves away from the interface. This is why the charge thickness C-V model is used for optimizing the SiC MOSFET capacitances. The wave function

penetration in ultra-thin modern MOSFETs and charge trapping in SiC MOS devices are also found in the accumulation region. BSIM3V3 defines different charge layer thicknesses for accumulation and inversion. Taking into account the effects of finite thickness of the charge layer, the effective oxide thickness per unit area in accumulation is written as:

$$\boldsymbol{C_{oxeff} = \frac{\varepsilon_{ox}}{TOX} // \frac{\varepsilon_s}{X_{DCeff}}} \quad \textbf{5.92}$$

where the **TOX** is the oxide thickness and X_{DCeff} is the effective thickness of the accumulation layer and is defined by a smoothing function as:

$$\boldsymbol{X_{DCeff} = X_{DCmax} - \frac{(X_{DCmax} - X_{DC} - \delta_x) + \sqrt{(X_{DCmax} - X_{DC} - \delta_x)^2 + 4\delta_x X_{DCmax}}}{2}} \quad \textbf{5.93}$$

here X_{DC} is the average thickness of the charge layer and can be derived from the 1-D self-consistent solution of the Schrodinger and Poisson equations using Fermi-Dirac statistics for high carrier concentration [121]. The approximated solution is given by:

$$\boldsymbol{X_{DC} = \frac{L_{Debye}}{3} exp\left[ACDE\left(\frac{NCH}{2\times10^{16}}\right)^{-1/4} \cdot \frac{V_{gbeff} - V_{fbzb}}{10^8 \times TOX}\right]} \quad \textbf{5.94}$$

In Eq. 5.94, L_{Debye} is known as the Debye length and can be written as:

$$\boldsymbol{L_{Debye} = \sqrt{\frac{\varepsilon_s \cdot \phi_t}{qNCH \cdot 10^{16}}}} \quad \textbf{5.95}$$

X_{DCmax} in Eq. 5.93 is the maximum charge layer thickness and is formulated as:

$$\boldsymbol{X_{DCmax} = \frac{L_{Debye}}{3}} \quad \textbf{5.96}$$

δ_x is a smoothing parameter used in Eq. 5.93 and the value is adjusted to $10^{-3} \cdot TOX$.

The total effective oxide capacitance for the accumulation charge calculation is found to be:

$$C_{oxefft} = L_{effcv} W_{effcv} C_{oxeff} \qquad 5.97$$

where L_{effcv} and W_{effcv} are effective channel and width length respectively used in the BSIM3V3 C-V model. The total accumulation charge is given as:

$$Q_{acc} = C_{oxefft}\left(V_{fbeffcv} - V_{FBcv}\right) \qquad 5.98$$

The depletion charge is calculated as:

$$Q_{sub0} = \begin{cases} C_{oxefft} K1 \left[\sqrt{\frac{1}{4}K1^2 + Tmp} - \frac{1}{2}K1\right] & if\ Tmp \geq 0 \\ C_{oxefft} Tmp & if\ Tmp < 0 \end{cases} \qquad 5.99$$

where *Tmp* is given by:

$$Tmp = V_{gse} - V_{fbeffcv} - V_{bseffcv} - V_{gsteffcv} \qquad 5.100$$

The purpose of defining *Tmp* is to make the depletion charge zero when the device operates in deep accumulation or strong inversion.

The per unit area oxide capacitance C_{oxinv} for inversion charge calculation requires a different charge layer thickness. C_{oxinv} can be written as:

$$C_{oxinv} = \frac{\varepsilon_{ox}}{TOX} // \frac{\varepsilon_s}{X_{DCinv}} \qquad 5.101$$

where X_{DCinv} is the thickness of the inversion charge layer and is given by:

$$X_{DCinv} = \begin{cases} \dfrac{1.9\times10^{-9}}{\left[1+\frac{V_{gsteffcv}+4\left(V_{TH}-V_{fbzb}-2\Phi_F\right)}{2\times10^{8}\cdot TOX}\right]^{0.7}} & if\ \left(V_{TH}-V_{fbzb}-2\Phi_F\right)\geq 0 \\ \dfrac{1.9\times10^{-9}}{\left[1+\frac{V_{gsteffcv}+10^{-20}}{2\times10^{8}\cdot TOX}\right]^{0.7}} & if\ \left(V_{TH}-V_{fbzb}-2\Phi_F\right)\geq 0 \end{cases} \quad 5.102$$

The total effective oxide capacitance in the inversion charge equation is found by multiplying the device area to the per unit oxide capacitance and can be written as:

$$C_{oxinvt} = L_{effcv}W_{effcv}C_{oxinv} \quad 5.103$$

When deriving the drain current equation for DC analysis, it is assumed that the surface potential is fixed when the devices operates in strong inversion. But in the C-V model, a fractional increment of the surface potential with respect to the gate voltage is semi-empirically defined as:

$$\Phi_\delta = \begin{cases} \phi_t ln\left[1+\frac{V_{gsteffcv}\left(V_{gsteffcv}+2\cdot K1\cdot\sqrt{2\Phi_F}\right)}{MOIN\cdot K1^{2}\cdot\phi_t}\right] & if\ K1>0 \\ \phi_t ln\left[1+\frac{V_{gsteffcv}\left(V_{gsteffcv}+\sqrt{2\Phi_F}\right)}{0.25\cdot MOIN\cdot\phi_t}\right] & if\ K1\leq 0 \end{cases} \quad 5.104$$

where **MOIN** is a model parameter and is used to adjust the extent of the surface potential increment with the gate voltage change. The drain-to-source saturation voltage as shown in Eq. 5.90 is modified to take into account the effect of the incremental surface potential and can be written as:

$$V_{dssatcv} = \frac{V_{gsteffcv}-\Phi_\delta}{A_{bulkcv}} \quad 5.105$$

And $V_{dseffcv}$ is calculated by Eq. 5.91 using $V_{dssatcv}$ found in Eq. 5.105. The total charge in the weak, moderate and strong inversion is then found from Eq. 5.106.

$$Q_{inv} = -C_{oxinvt}\left[\left(V_{gsteffcv} - \Phi_{\delta} - \frac{A_{bulkcv}V_{dseffcv}}{2}\right) + \frac{A_{bulkcv}^2 V_{dseffcv}^2}{12\left(V_{gsteffcv}-\Phi_{\delta}-\frac{A_{bulkcv}V_{dseffcv}}{2}+10^{-20}\right)}\right] \quad 5.106$$

The 10^{-20} factor in Eq. 5.105 is added in the denominator to ensure that the term does not become negative when the term without the factor is negative and close to zero. As the drain bias in a MOSFET device is increased, the depletion width of the drain-body junction extends further into the substrate and thus the space charge contributes more to the overall MOSFET bulk charge. The extra component of bulk charge from the drain-body junction is given by:

$$\delta Q_{sub} = C_{oxinvt}\left[\frac{1-A_{bulkcv}}{2}V_{dseffcv} - \frac{(1-A_{bulkcv})A_{bulkcv}V_{dseffcv}^2}{12\left(V_{gsteffcv}-\Phi_{\delta}-\frac{A_{bulkcv}V_{dseffcv}}{2}+10^{-20}\right)}\right] \quad \mathbf{5.107}$$

It is noted from Eq. 5.107 that the excess bulk charge contribution from the drain side junction is zero when there is no voltage difference between the drain and source.

After all the charges in accumulation, depletion and inversion are found, the charge at each terminal can be calculated from the principle of charge conservation. The total charge at the gate terminal is given by:

$$Q_G = -Q_{inv} - \delta Q_{sub} + Q_{acc} + Q_{sub0} \quad \mathbf{5.108}$$

and the total bulk charge is:

$$Q_B = \delta Q_{sub} - Q_{acc} - Q_{sub0} \quad \mathbf{5.109}$$

The charge at the drain and source can be calculated by the first moment technique as demonstrated in Eqs. 5.80 and 5.81. The total charge at the source terminal is:

$$Q_S = -\frac{C_{oxinvt}}{2\left(V_{gsteffcv}-\Phi_\delta-\frac{A_{bulkcv}V_{dseffcv}}{2}\right)^2} \times \left[\left(V_{gsteffcv}-\Phi_\delta\right)^3 - \frac{4}{3}\left(V_{gsteffcv}-\Phi_\delta\right)^2 A_{bulkcv}V_{dseffcv} + \frac{2}{3}\left(V_{gsteffcv}-\Phi_\delta\right)A_{bulkcv}^2V_{dseffcv}^2 - \frac{2}{15}A_{bulkcv}^3V_{dseffcv}^3\right] \quad 5.110$$

and the total drain charge is:

$$Q_D = -\frac{C_{oxinvt}}{2\left(V_{gsteffcv}-\Phi_\delta-\frac{A_{bulkcv}V_{dseffcv}}{2}\right)^2} \times \left[\left(V_{gsteffcv}-\Phi_\delta\right)^3 - \frac{5}{3}\left(V_{gsteffcv}-\Phi_\delta\right)^2 A_{bulkcv}V_{dseffcv} + \left(V_{gsteffcv}-\Phi_\delta\right)A_{bulkcv}^2V_{dseffcv}^2 - \frac{1}{5}A_{bulkcv}^3V_{dseffcv}^3\right] \quad 5.111$$

The sum of drain and source charge is equal to the total inversion charge and from Eqs. 5.110 and 5.111, it is found that the ratio of the drain to source charge is 40/60 in the saturation region. This charge partitioning is known as 40/60 partition scheme and the scheme can be chosen by assigning a value less than 0.5 to the model parameter **XPART**. BSIM3V3 has two other partition schemes – 0/100 and 50/50. When **XPART** is greater than 0.5, the 0/100 partition scheme is selected and $Q_S(t)$ and $Q_D(t)$ are given by:

$$Q_S = -C_{oxinvt}\left[\frac{V_{gsteffcv}-\Phi_\delta}{2} + \frac{A_{bulkcv}V_{dseffcv}}{4} - \frac{A_{bulkcv}^2V_{dseffcv}^2}{24\left(V_{gsteffcv}-\Phi_\delta-A_{bulkcv}V_{dseffcv}/2+10^{-20}\right)}\right] \quad 5.112$$

$$Q_D = -C_{oxinvt}\left[\frac{V_{gsteffcv}-\Phi_\delta}{2} - \frac{3A_{bulkcv}V_{dseffcv}}{4} + \frac{A_{bulkcv}^2V_{dseffcv}^2}{8\left(V_{gsteffcv}-\Phi_\delta-A_{bulkcv}V_{dseffcv}/2+10^{-20}\right)}\right] \quad 5.113$$

The 50/50 charge partitioning scheme is activated when **XPART** is equal to 0.5 and the inversion charge is equally divided between the drain and source nodes:

$$Q_S = Q_D = \frac{Q_{inv}}{2} \quad 5.114$$

The 40/60 partition scheme is the only physical model in BSIM3V3 and is used in the transient and small signal analyses of sensitive analog and mixed signal circuits. The other two schemes do not have any physical origin and are used in digital circuits for fast simulation.

5.2.4 Small Signal Capacitance Modeling

The MOSFET is an active device and its capacitances have some important general characteristics. The small signal capacitance of the MOSFET is defined as:

$$\boldsymbol{C_{xy} = \delta_{xy} \frac{\partial Q_x}{\partial V_y}} \qquad \textbf{5.115}$$

where $\delta_{xy} = 1$ if $x = y$ and -1 if $x \neq y$. For example, $C_{gg} = +\frac{\partial Q_G}{\partial V_g}$, and $C_{gd} = -\frac{\partial Q_G}{\partial V_d}$. Eq. 5.115 suggests that since the MOSFET is a four-terminal device, there are sixteen capacitances which are used for small signal analysis. The first property is that the capacitances are not reciprocal except when the voltage across the drain and the source terminals is zero. For example, in saturation region $C_{gd} \neq C_{dg}$. When the device enters into the saturation region, the channel at the drain end region is pinched off and the inversion charge is zero. If the voltage at the drain is increased while keeping all the node voltages constant, the channel charge does not change and thus Q_G remains constant. Thus C_{gd} which is defined as the variation in the gate charge with respect to the change in the drain voltage is zero. But if the gate voltage is increased while keeping the other voltages constant, the channel charge increases significantly and much of the charge is supplied by the drain node. So C_{dg} $(= \partial Q_D \backslash \partial V_g)$ is expected to be a large number. It should be noted that the capacitance of a two-terminal parallel plate capacitor is always reciprocal.

The other property of the MOSFET small signal capacitances comes from the charge neutrality and the principle of charge conservation which dictates that under all circumstances the sum of the charges at the MOSFET terminals are zero. Thus, it can be written that:

$$Q_G + Q_D + Q_B + Q_S = 0 \quad \textbf{5.116}$$

If Eq. 5.116 is differentiated with respect to time it is shown that the sum of the capacitive currents is also zero:

$$\frac{dQ_G}{dt} + \frac{dQ_D}{dt} + \frac{dQ_B}{dt} + \frac{dQ_S}{dt} = 0 \quad \textbf{5.117}$$

Eq. 5.117 reveals some interesting properties of the MOSFET capacitances. For example, if under a fixed operating point, the voltage of the gate node is varied while keeping the voltages at all the other nodes constant, using Eq. 5.115 it can be written that:

$$\frac{dQ_G}{dt} = \frac{d}{dt}\left[C_{gg} \cdot v_g(t)\right] \quad \textbf{5.118}$$

$$\frac{dQ_D}{dt} = \frac{d}{dt}\left[C_{dg} \cdot v_g(t)\right] \quad \textbf{5.119}$$

$$\frac{dQ_B}{dt} = \frac{d}{dt}\left[C_{bg} \cdot v_g(t)\right] \quad \textbf{5.120}$$

$$\frac{dQ_S}{dt} = \frac{d}{dt}\left[C_{sg} \cdot v_g(t)\right] \quad \textbf{5.121}$$

Replacing the values of the charge derivatives from the Eqs. 5.118 – 5.121 in the Eq. 5.117, it can be shown that:

$$\left[C_{gg} + C_{dg} + C_{bg} + C_{sg}\right] \cdot \frac{dv_g(t)}{dt} = 0 \quad \textbf{5.122}$$

Since the gate voltage varies with time, Eq. 5.118 is only true if the sum of the capacitances is zero:

$$C_{gg} + C_{dg} + C_{bg} + C_{sg} = 0 \quad \textbf{5.123}$$

Using the same arguments, it can be shown that:

$$C_{gd} + C_{dd} + C_{bd} + C_{sd} = 0 \quad \textbf{5.124}$$

$$C_{gb} + C_{db} + C_{bb} + C_{sb} = 0 \quad \textbf{5.125}$$

$$C_{gs} + C_{ds} + C_{bs} + C_{ss} = 0 \quad \textbf{5.126}$$

In other case when the voltage at all the nodes is changed by the same amount in the same direction and at the same time, the node charges will not change. The total incremental charge can be shown as:

$$\Delta Q_G = C_{gg}\Delta v_g - C_{gd}\Delta v_d - C_{gb}\Delta v_b - C_{gs}\Delta v_s \quad 5.127$$

$$\Delta Q_D = -C_{dg}\Delta v_g + C_{dd}\Delta v_d - C_{db}\Delta v_b - C_{ds}\Delta v_s \quad \textbf{5.128}$$

$$\Delta Q_B = -C_{bg}\Delta v_g - C_{bd}\Delta v_d + C_{bb}\Delta v_b - C_{bs}\Delta v_s \quad \textbf{5.129}$$

$$\Delta Q_S = -C_{sg}\Delta v_g - C_{sd}\Delta v_d - C_{sb}\Delta v_b + C_{ss}\Delta v_s \quad \textbf{5.130}$$

Since the change in the charge at each terminal is zero and the voltage changes by the same amount at all the nodes, it can be written that:

$$\Delta Q_G = \Delta Q_D = \Delta Q_B = \Delta Q_S = 0 \quad \textbf{5.131}$$

$$\Delta v_g = \Delta v_g = \Delta v_g = \Delta v_g = \Delta v \quad \textbf{5.132}$$

Using the relationships from Eqs. 5.131 and 5.132 in the Eqs. 5.127-5.130, it is concluded that:

$$\boldsymbol{C_{gg} - C_{gd} - C_{gb} - C_{gs} = 0} \quad \textbf{5.133}$$

$$\boldsymbol{C_{gg} - C_{gd} - C_{gb} - C_{gs} = 0} \quad \textbf{5.134}$$

$$\boldsymbol{C_{gg} - C_{gd} - C_{gb} - C_{gs} = 0} \quad \textbf{5.135}$$

$$\boldsymbol{C_{gg} - C_{gd} - C_{gb} - C_{gs} = 0} \quad \textbf{5.136}$$

From the discussion on the MOSFET small signal capacitances, the following important properties of the capacitances are revealed:

- The charge expressions for only three terminals of the MOSFET are required. The charge at the fourth node can be found from the charge neutrality condition.
- Eqs. 5.123 – 5.126 and Eqs. 5.133 – 5.136 suggest that only nine out of sixteen capacitances are independent and thus require the derivation from the charge equations using the relationship as shown in 5.115. The rest of the capacitances can be calculated from different linear combinations of the nine capacitances.

In the C-code implementation of BSIM3V3, these two powerful properties are implemented to provide model accuracy and simulation efficiency.

5.2.5 Parasitic Capacitance Modeling

The small signal capacitances as explained in the previous section are intrinsic to the MOSFET device. There are also unavoidable parasitic capacitances in a MOSFET and these capacitances affect both transient and high frequency performance of the device. In Fig. 5.4, the

dominant parasitic capacitances in a MOSFET are illustrated. The description of the capacitances and their origin are as follows:

- C_f – fringing capacitance. Part of the electric field lines generated by the gate charge terminate on the source and drain from the edges of the gate poly and thus gives rise to the fringing capacitance.
- C_{OV} – overlap capacitance. There is always an overlap between the gate oxide and the source and drain regions as a part of the process requirement. The electric field lines which terminate on the overlap regions from the gate electrode do not contribute to the formation of the channel and thereby introduce parasitic capacitances.
- C_{gbp} – gate-to-bulk parasitic capacitance. In a CMOS process, the active transistor is surrounded by the isolation oxide and some part of the gate poly overlaps with the oxide. The bottom of the isolation oxide is usually the bulk. As a result, a parasitic capacitance is formed between the oxide where the bulk and the gate poly act as the electrodes of a parallel plate capacitor.
- C_{jdbbw}, C_{jsbbw} – drain-to-bulk and source-to-bulk bottom wall capacitances. This is the p-n junction capacitances formed between the bottom of the source/drain and the bulk.
- C_{jdbsw}, C_{jsbsw} - drain-to-bulk and source-to-bulk side wall capacitances at the isolation oxide side. The side wall of the source /drain doped region forms a junction with the semiconductor adjacent to the isolation oxide and thus forms parasitic capacitances.

- C_{jdbswg}, C_{jsbswg} - drain-to-bulk and source-to-bulk side wall capacitances at the gate side. The side wall of the drain/source region at the channel side also forms a parasitic p-n junction capacitance.

Accurate modeling of the parasitic capacitances and related charge is of paramount importance. For example, although the intrinsic gate-to-drain capacitance C_{gd} is zero in the saturation region, the parasitic overlap and fringing capacitance will add to the total gate-to-drain

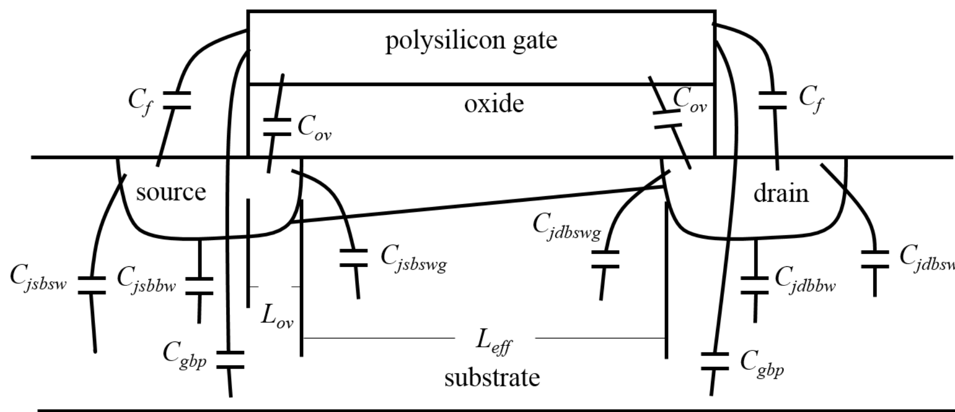


Fig. 5.4. Parasitic capacitances in a MOSFET device.

capacitance and significantly influence the high frequency and transient operations of an amplifier (devices are usually biased in saturation in an amplifier).

In order to model the overlap capacitance and associated charge, a smoothing function for the gate-to-drain overlap voltage is defined:

$$V_{gdoverlap} = \frac{1}{2}\left[V_{GD} + \delta_1 - \sqrt{(V_{GD} + \delta_1)^2 + 4\delta_1}\right]; \qquad \delta_1 = 0.02 \qquad 5.137$$

where V_{GD} is the gate-to-drain voltage. The overlap charge is modeled as:

$$Q_{ovgd} = W_{effcv} \times \left\{ CGD0 \cdot V_{gd} + CGD1 \left[V_{gd} - V_{gdoverlap} - \frac{CKAPPA}{2} \left(-1 + \sqrt{1 - \frac{4 \cdot V_{gdoverlap}}{CKAPPA}} \right) \right] \right\} \qquad 5.138$$

here **CGDO**, **CGD1** and **CKAPPA** are model parameters. The overlap capacitance between the gate and the drain terminal is calculated by:

$$C_{ovgd} = \frac{\partial Q_{ovgd}}{\partial V_{gd}} \qquad 5.139$$

The overlap charge and capacitance between the gate and the source can also be calculated by Eqs. 5.137 – 5.139 if the *d* (drain) is replaced by *s* (source).

The fringing capacitance is given by:

$$C_f = W_{effcv} \cdot CF \qquad 5.140$$

Where **CF** is a model parameter and can be extracted from the measured capacitance. The corresponding fringing charge of the drain side is calculated by:

$$Q_{fgd} = \int_0^{V_{gd}} C_f dV_{gd} = W_{effcv} \cdot CF \cdot V_{gd} \qquad 5.141$$

Eq. 5.141 is also used to determine the gate-to-source fringing charge by replacing V_{gd} with V_{gs}.

The gate-to-bulk parasitic capacitance and charge can be calculated by Eq. 5.142 and 5.143 respectively.

$$C_{gb0} = L_{effcv} \cdot CGB0 \qquad 5.142$$

$$Q_{gbp} = \int_0^{V_{gb}} C_{gb0} dV_{gs} = L_{effcv} \cdot CGB0 \cdot V_{gb} \quad \textbf{5.143}$$

When all the intrinsic and parasitic charges are known, the total charge at each node can be calculated as:

$$Q_{Gt} = Q_G + Q_{ovgs} + Q_{ovgd} + Q_{fgs} + Q_{fgd} + Q_{gbp} \quad \textbf{5.144}$$

$$Q_{Dt} = Q_D - Q_{ovgd} - Q_{fgd} - Q_{jdb} \quad \textbf{5.145}$$

$$Q_{St} = Q_S - Q_{ovgs} - Q_{fgs} - Q_{jsb} \quad \textbf{5.146}$$

$$Q_{Bt} = Q_B + Q_{jsb} + Q_{jdb} - Q_{gbp} \quad \textbf{5.147}$$

The capacitances and related charge equations of the side wall and bottom wall source/drain-to-bulk p-n junctions can be derived by applying the Poisson's equation in a one sided abrupt junction. The junction capacitance is non-linear in nature and behaves differently in forward and reverse bias region.

If $V_{bd} < 0$, then the total junction capacitance is:

$$C_{jdb} = \frac{CJ}{\left(1 - \frac{V_{bd}}{PB}\right)^{MJ}} AD + \frac{CJSW}{\left(1 - \frac{V_{bd}}{PBSW}\right)^{MJSW}} \left(PD - W_{effcv}\right) + \frac{CJSWG}{\left(1 - \frac{V_{bd}}{PBSWG}\right)^{MJSW}} W_{effcv} \quad \textbf{5.148}$$

where **AD** and **PD** are the area and the perimeter of the source/drain region respectively, **CJ**, **CJSW**, **CJSWG**, **MJ**, **MJSW**, **MJSWG**, **PB**, **PBSW** and **PBSWG** are model parameters. The total space charge in the junction can be calculated by integrating the non-linear junction capacitance with respect to the voltage across the capacitance and is given by:

$$Q_{jdb} = \int_0^{V_{bd}} C_{jdb}(V_{bd})dV_{bd} = \frac{CJ \cdot AD \cdot PB}{1-MJ}\left[1-\left(1-\frac{V_{bd}}{PB}\right)^{1-MJ}\right] + \frac{CJSW \cdot (PD - W_{effcv}) \cdot PBSW}{1-MJSW}\left[1-\left(1-\frac{V_{bd}}{PBSW}\right)^{1-MJSW}\right] + \frac{CJSWG \cdot W_{effcv} \cdot PBSWG}{1-MJSWG}\left[1-\left(1-\frac{V_{bd}}{PBSWG}\right)^{1-MJSWG}\right] \quad 5.149$$

If $V_{bd} \geq 0$, the junction capacitance is linearized and the formulation becomes:

$$C_{jdb} = CJ\left(1 + MJ\frac{V_{bd}}{PB}\right)AD + CJSW\left(1 + MJSW\frac{V_{bd}}{PBSW}\right)(PD - W_{effcv}) + CJSWG\left(1 + MJSWG\frac{V_{bd}}{PBSWG}\right)W_{effcv} \quad 5.150$$

and the deletion region charge is given by:

$$Q_{jdb} = CJ \cdot AD\left(V_{bd} + \frac{MJ}{PB}\frac{V_{bd}^2}{2}\right) + CJSW \cdot (PD - W_{effcv})\left(V_{bd} + \frac{MJSW}{PBSW}\frac{V_{bd}^2}{2}\right) + CJSWG \cdot W_{effcv}\left(V_{bd} + \frac{MJSWG}{PBSWG}\frac{V_{bd}^2}{2}\right) \quad 5.151$$

5.2.6 Parameter Extraction and Optimization with HSPICE BSIM3V3

At the University of Arkansas, the first batch of integrated circuits and test structures in the Raytheon 1.2 µm HiTSiC CMOS process were taped out using the custom PDK developed at the MSCAD (Mixed Signal Computer Aided Design) lab. The models for the MOSFET were developed based on the HSPICE built-in Level 49 BSIM3V330 and added to the PDK by setting up a HSPICE model library. The parameter extraction and optimization method used for the model card generation with BSIM3V3 is very similar to the method utilized in the BSIM4 parameter extraction and optimization (described in section 5.3) and is not outlined in this section in order to avoid redundancy.

5.2.7 Model Optimization Results with BSIM3V3

In Fig. 5.5, the simulated and measured transfer characteristics (I_d - V_g) of a 20µm×2µm SiC NMOS at low drain voltage (0.25 V) and room temperature are plotted. It is found that although the model predicts the drain current well in the absence of body voltage (red curve), it cannot be optimized with acceptable mismatch in presence of the body bias. The voltages at the bulk terminal in the graph are -3V (blue curve) and -6V (pink curve).

The simulated transfer characteristics (I_d - V_g) at different drain voltages (0.25V, 3.2V, 6.15V, 9.1V, 12.05V and 15V) and the output characteristics (I_d – V_d) at different gate voltages (5V, 7V, 9V, 11V, 13V and 15V) are plotted in Fig. 5.6 with the measured data for the 20µm×2µm NMOS device. The mismatch between the simulated and measured characteristics is small except in the transition from triode to saturation at higher gate voltages as found in the I_d – V_d curve.

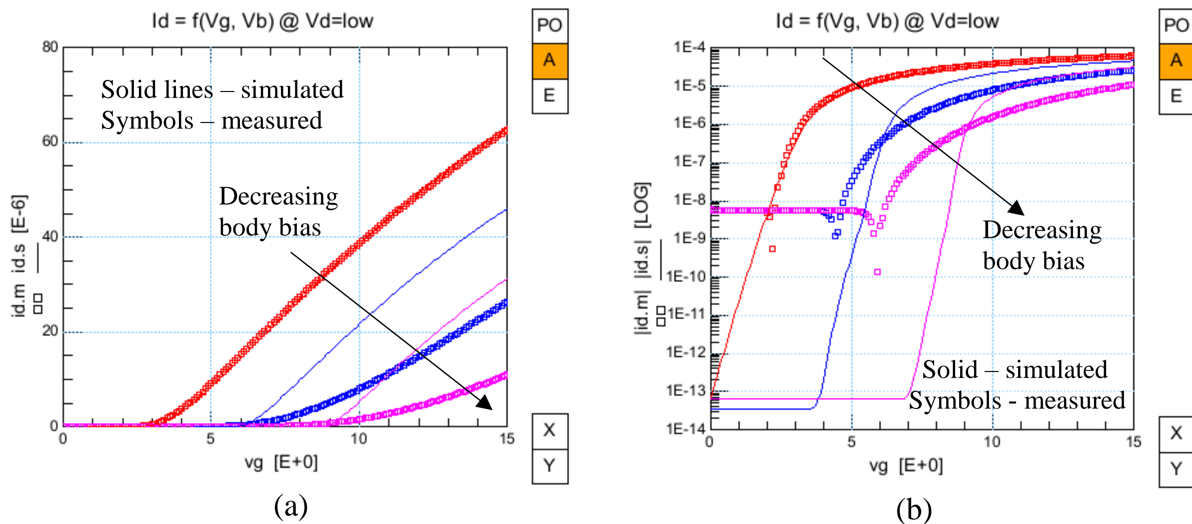
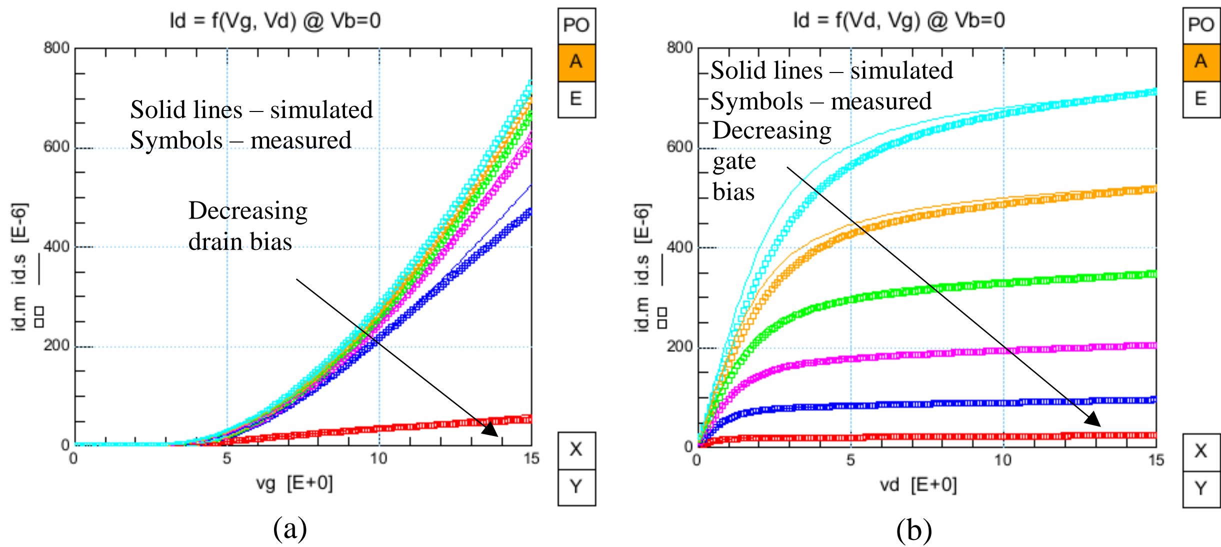


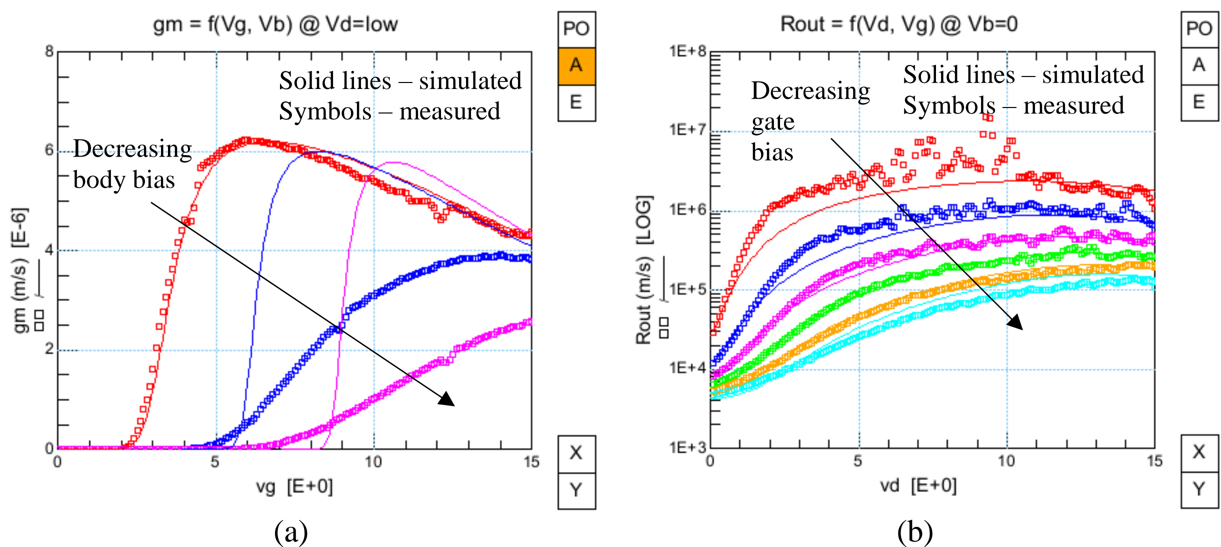
Fig. 5.5. The simulated transfer characteristics at 0.25 V drain voltage of the 20µm/2µm SiC NMOS are overlaid with the measured characteristics: (a) in linear scale to demonstrate the strong inversion region and (b) in log scale to demonstrate the subthreshold region.



(a) (b)

Fig. 5.6. (a) The measured and simulated $I_d - V_g$ characteristics of the 20µm/2µm NMOS at different drain voltages and zero body voltage and (b) the output characteristics ($I_d - V_d$) of the NMOS at different gate biases and zero bulk voltage.

The simulated small signal DC parameters such as transconductance (g_m) and output resistance (r_{out}) are displayed in Fig. 5.7 with their measured counterparts. The simulated transconductance curves at non-zero body biases have large discrepancy with the measured data.



(a) (b)

Fig. 5.7. (a) Transconductance (g_m) vs. gate voltage (V_g) characteristics at different body bias and (b) output resistance (r_{out}) vs. drain voltage (V_d) at different gate voltage of the NMOS.

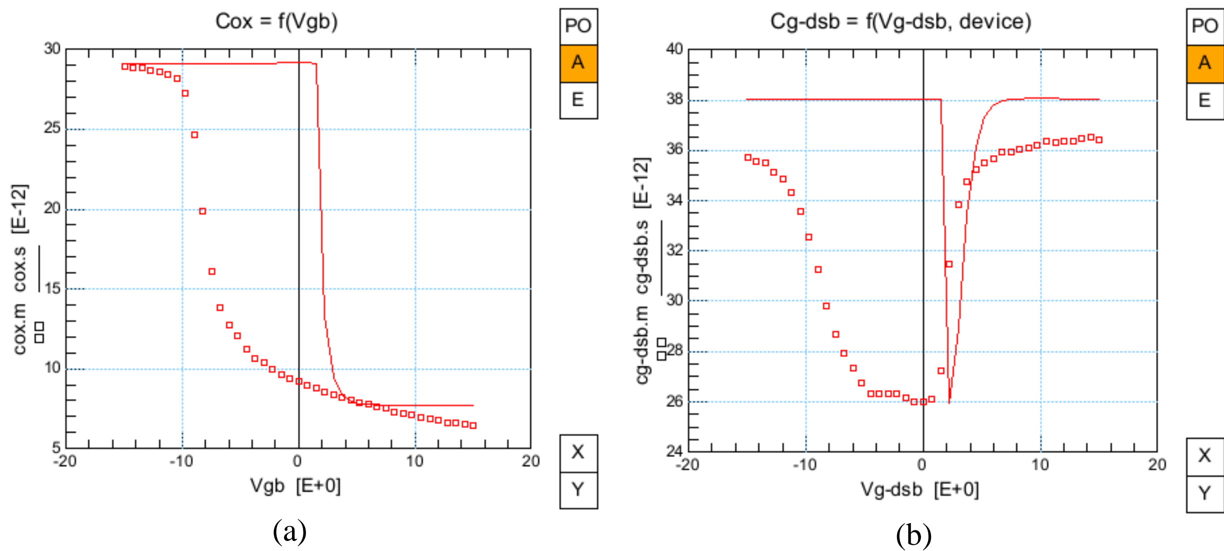


Fig. 5.8. Simulated and measured (a) oxide capacitance (Cox) vs. gate-to-bulk voltage (V_{gb}) and (b) total gate capacitance (Cgg) vs. gate-to-drain/source/bulk voltage ($V_{g\text{-}dsb}$). Solid lines and symbols represent simulated and measured characteristics respectively.

The measured capacitances are overlaid with the simulated characteristics in Fig. 5.8. The oxide capacitance is displayed in Fig. 5.8(a) and the total gate capacitance is plotted in Fig. 5.8(b). It is found that BSIM3V cannot be optimized to accurately model the C-V behavior of SiC MOSFETs.

5.2.8 Limitations of BSIM3V3 in Modeling SiC MOSFET

As shown in Fig. 5.5 - Fig. 5.8, BSIM3V3 has severe shortcomings in modeling the DC and C-V characteristics of SiC MOSFETs. Some of the pertinent reasons are summarized below:

- BSIM3 was specifically developed for Si technology. There is no option to provide SiC material parameters in BSIM3 as inputs. As a result, material dependent parameters like intrinsic carrier concentration, surface potential at strong inversion, flat band voltage etc. which primarily determine C-V behavior could not be accurately calculated.

- In presence of body bias, at low currents when the device is in the onset of strong inversion region, mobility is strongly influenced by interface trapped charge induced coulomb scattering. There is no advanced mobility model in BSIM3v3 which can model this phenomenon. This is why Id-Vg characteristics at non-zero body bias could not be modeled accurately.
- SiC devices have very soft transition from sub-threshold to strong inversion region when the body is biased. BSIM3 does not have any formulation that can model this behavior.

Also, the PMOSs available for characterization at the time of the model development based on BSIM3V3 had design optimization issues and were found to have unusual bumps during turn-on which is uncharacteristic to MOSFET devices. This is why PMOS models were developed based on the information provided by the foundry on the device characteristics expected in the following run.

5.3 BSIM4 for SiC MOSFET Modeling

Since BSIM3v3.3 has some limitations in accurately predicting SiC MOSFET behavior, BSIM4 was chosen for the modeling efforts in the second tape-out. In BSIM4.6.0 and later versions, many new features and enhancements were added in order to model the physical effects of MOSFET devices in the sub-100 nm process nodes. The complete list of the additional features added in BSIM4.8.0 can be found in [122].

One of the new features which is useful for this work is the inclusion of a new model for non-Si substrate and non-SiO_2 gate oxide. Using the model parameter **MTRLMOD**, a non-silicon channel can be chosen in BSIM4. If a non-zero value is assigned to **MTRLMOD**, the model for

non-silicon substrate will be activated. New equations for the material specific characteristics such as band-gap and intrinsic carrier concentration were introduced in the non-silicon model. The band-gap at the nominal temperature in the new model is given by:

$$E_{g0}(TNOM) = BG0SUB - \frac{TBGASUB \times TNOM^2}{TNOM + TBGBSUB} \qquad \mathbf{5.152}$$

where **BG0SUB** is the band-gap of the substrate material at 0 ° K, **TBGASUB** and **TBGBSUB** are temperature coefficients. The band-gap at a higher temperature is:

$$E_g(Temp) = BG0SUB - \frac{TBGASUB \times Temp^2}{Temp + TBGBSUB} \qquad 5.153$$

and the intrinsic carrier concentration at nominal temperature is:

$$N_i(TNOM) = NI0SUB \times \left(\frac{TNOM}{300.15}\right)^{3/2} \times exp\left(\frac{E_g(300.15) - E_{g0}(TNOM)}{2\phi_t}\right) \qquad \mathbf{5.154}$$

where **NI0SUB** is the intrinsic carrier concentration at 300.15 ° K.

The inversion charge layer thickness (X_{DC}) which is introduced in section 5.2.3 is also modified and given by:

$$X_{DC} = \frac{ADOS \times 1.9 \times 10^{-9}}{1 + \left(\frac{V_{gsteff} + (VTH0 - VFB - 2\Phi_F)}{2TOXP}\right)^{0.7 \times BDOS}} \qquad \mathbf{5.155}$$

where **ADOS** and **BDOS** are model parameters related to the density of states and are used to adjust the charge centroid. **VFB** is the flat-band voltage used in the DC equations. **TOXP** is another model parameter and denotes the physical oxide thickness. In the ultra-thin oxide (~1nm) MOSFET, high-κ gate dielectric such as HfO_2 is used to prevent excessive leakage current. To take into accounts the difference between SiO_2 and high-κ gate dielectric, BSIM4 introduces three

parameters for oxide thickness – effective oxide thickness (**EOT**), physical oxide thickness (**TOXP**) and electrical oxide thickness (**TOXE**). Any value can be assigned to **EOT** and **TOXE** through model card. BSIM4 uses an algorithm to calculate **TOXP** from **EOT** and **TOXE**. With the new definition of the oxide thickness, two different oxide capacitances per unit area are defined and one of the two is calculated as follows:

$$C_{oxe} = \frac{EPSROX \cdot \varepsilon_0}{TOXE} \tag{5.156}$$

where **EPSROX** is the relative permittivity of the gate dielectric. C_{oxe} is used in the calculation of threshold voltage V_{TH}, subthreshold swing factor n, effective gate-to-source voltage V_{gsteff}, mobility μ_{eff}, bulk charge coefficient A_{bulk}, drain-to-source saturation voltage V_{dsat}, modified body effect coefficient $K1_{ox}$ (= **K1·TOXE/TOXM**) etc. The other capacitance per unit area is:

$$C_{oxp} = \frac{EPSROX \cdot \varepsilon_0}{TOXP} \tag{5.157}$$

and C_{oxp} is used to calculate C_{oxeff} as shown in Eq. 5.42 for drain current and in **CAPMOD**=2 through the charge-layer thickness model as indicated in section 5.2.3.

A new mobility model was introduced in BSIM4 to implement coulomb scattering related mobility reduction which is resulted by the presence of interface trapped charge in III-V MOS devices. The model also includes the formulation of mobility reduction contributed by surface roughness. The new mobility model can be selected by assigning 3 to the model parameter **MOBMOD**. The mobility according to this model is:

$$\mu_{eff} = \frac{\mu 0(Temp,L)}{1+(UA+UC \cdot V_{bseff})\left[\left(\frac{V_{gsteff}+C_{n,p}(VTH0-VFB-2\Phi_F)}{6 \cdot TOXE} \cdot 10^{-8}\right)\right]^{EU} + \frac{UD}{\left[0.5 \cdot \left(1+V_{gsteff}/V_{gs_on}\right)^{UCS}\right]}} \tag{5.158}$$

In Eq. 5.158, the coefficient $C_{n,p}$ is an empirical parameter and it is found that the value of the parameter is 2 for NMOS and 2.5 for PMOS. **EU** is a model parameter with a default value of 1.67. The model parameters **UD** and **UCS** can be used to optimize the interface trapped charge and surface roughness related mobility reduction.

There are several other modifications which were included in BSIM4 to increase the parameter extraction flexibility and model predictability. The effective gate-to-source voltage which is shown in Eq. 5.20 for BSIM3V3 was modified in BSIM4 as follows:

$$V_{gsteff} = \frac{n\phi_t ln\left[1+exp\left(\frac{m^*\left(V_{gseff}-V_{TH}\right)}{n\phi_t}\right)\right]}{m^*+n\frac{C_{oxeff}}{C_{dep0}}exp\left[-\frac{(1-m^*)\left(V_{gseff}-V_{TH}\right)-V^*_{off}}{n\phi_t}\right]} \quad \textbf{5.159}$$

In Eq. 5.159, m^* is added to improve the model accuracy in the moderate inversion region and V^*_{off} is included to model the length dependency of subthreshold leakage at zero gate bias. The equations for m^* and V^*_{off} are:

$$m^* = 0.5 + \frac{arctan(MINV)}{\pi} \quad \textbf{5.160}$$

$$V^*_{off} = VOFF + \frac{VOFFL}{L_{eff}} \quad \textbf{5.161}$$

here **MINV**, **VOFF** and **VOFFL** are model parameters.

The surface potential in the strong inversion is also modified and given by:

$$2\Phi_F = 0.4 + \phi_t ln\frac{NDEP}{N_i} + PHIN \quad 5.162$$

where **NDEP** is the average doping density in the channel region and **PHIN** is a model parameter.

5.3.1 Parameter Extraction and Optimization with HSPICE BSIM4

Prior to the modeling efforts with BSIM4, suggestions were sought from the circuit designers about their expectation from the model. It was understood that the models would be primarily used for analog and digital circuit design and hence the RF modeling part of BSIM4 was completely ignored. Built-in HSPICE BSIM4, version 6.5 was chosen. Based on the suggestions provided by the designers, the following aspects were given more importance and corresponding parameters were optimized for modeling SiC FETs:

- Unlike sub-100nm Si devices, bulk leakage and gate leakage currents are very small in the SiC devices and hence they were not modeled.
- Temperature range of 25 ^{o} C to 300 ^{o} C was chosen for modeling over temperature.
- As previously mentioned, unlike Si devices, body effects of SiC devices are not merely linear shifts of the transfer curve along the voltage axis. Sub-threshold slope and mobility (especially in NMOS) change significantly when there is a voltage across the source and the body. BSIM4 is not capable of modeling this behavior and hence modeling of the body effect was chosen over sub-threshold modeling for the PMOS. Since the NMOS has an isolated well in this process, the body effect of the NMOSs were not intensively modeled.
- The device with 1.2 μm channel length was chosen as the prime device for digital design and the device with 2 μm channel length was chosen for analog design by the designers. Special attention was paid when modeling these devices.
- Due to the presence of interface traps, the C-V behavior is frequency dependent. BSIM4 can't model this oddity. As a result, C-V modeling was performed with measured capacitance taken at one specific frequency (10 kHz).

- For the same reason mentioned above, C-V behavior also changes over temperature. A separate C-V model was optimized for each separate temperature.
- All the DC characteristics were optimized for -5 V to 20 V gate voltage steps although more focus was on the gate voltages at or below 15 volts.
- Analog designers expected to bias the devices such that the PMOSs provide 0.5 µA to 1.5 µA per finger and the NMOSs provide 5 µA to 15 µA per finger at the edge of saturation. Special attention was paid to model the small signal quantities (gm and r0) in this region.
- Since no more than two PMOSs were intended to stack in analog design, body effect modeling was accurately done for 2-4 V source-body biases. The models have acceptable accuracy at other source-body biases up to 12 volts.
- An offset was observed between the measured output ($I_d - V_d$) data and the transfer ($I_d - V_g$) data. For example, at the same drain and gate voltages, the currents found from I_d-V_d and I_d-V_g curve were different by few microamps. At V_g = 15 V, V_d = 15 V and Vbs = 0 V, I_d is 1.572 mA from the transfer curve but it is 1.517 mA from the output curve of 20 µm / 1.2 µm device. This is the result of slow interface trapped charge (some of the interface states have lifetime in the order of seconds). Measured current varies depend on how long the gate is kept at a specific bias. The I_d-V_g curve was chosen as the reference for optimization of the model.

The detailed description of the parameter extraction and optimization process for SiC MOSFET with BSIM4 is given in section 7.6. To avoid repetition, the extraction steps are briefly summarized in Table 5.1 for an NMOS device with a specific length and different channel widths. Similar extraction method is also applied for PMOS devices.

Table 5.1. Parameter extraction steps of SiC NMOS using HSPICE BSIM4.6.5

Step No.	Parameter Name	Extraction Curves	Extraction Region
1	**EOT**, **TOXE**, **ACDE, VFB**	C_{ox} vs V_g	Deep accumulation
2	**CF**, **CGDO**, **CGSO**	C_{gds} vs. V_g	$V_g = 0$ V
3	**CGDL**, **CGSL, CKAPPAD, CKAPPAS**	C_{gds} vs. V_g	Deep accumulation
4	**LINT**	C_{gds} vs. V_g	Strong inversion
5	**K1**	C_{gdsb} vs. V_g	Depletion
6	**VOFF**, **NFACTOR**	I_d vs. V_g at V_d = 0.5V and V_b = 0V of a wide (20 µm) channel device	Subthreshold
7	**VTH0**	I_d vs. V_g at V_d = 0.5V and V_b = 0V of a wide (20 µm) channel device	Moderate inversion
8	**U0**, **UA**, **UD**, **UCS**, **EU**	I_d vs. V_g at V_d = 0.5V and V_b = 0V of a wide (20 µm) channel device	Strong inversion
9	**K2**	I_d vs. V_g at V_d = 0.5V and V_b = -3, -6 and -9V of a wide (20 µm) channel device	Strong inversion
10	**VOFFCV, NOFF**	C_{gdsb} vs. V_g	Transition from depletion to strong inversion
11	**CDSC, CDSCD, DVT1**	I_d vs. V_g at V_d = VDD and V_b = 0V of a wide (20 µm) channel device	Subthreshold
12	**CDSCB**	I_d vs. V_g at V_d = VDD and V_b = -3, -6 and -9V of a wide (20 µm) channel device	Subthreshold
13	**DSUB, ETA0**	I_d vs. V_g at V_d = VDD and V_b = 0V of a wide (20 µm) channel device	Moderate inversion

Table 5.2. (Cont.)

Step No.	Parameter Name	Extraction Curves	Extraction Region
14	**ETAB**	I_d vs. V_g at V_d = VDD and V_b = -3, -6 and -9V of a wide (20 μm) channel device	Moderate inversion
15	**A0, AGS**	I_d vs. V_g at V_d = VDD and V_b = 0V of a wide (20 μm) channel device	Strong inversion
16	**KETA**	I_d vs. V_g at V_d = VDD and V_b = -3, -6 and -9V of a wide (20 μm) channel device	Strong inversion
17	**DELTA, VSAT**	I_d vs. V_d at V_g = 3, 5, 7, 9, 11, 13, 15V and V_b = 0V of a wide (20 μm) channel device	Transition from linear to saturation
18	**PCLM, PVAG, PDIBLC1**	I_d vs. V_d at V_g = 3, 5, 7, 9, 11, 13, 15V and V_b = 0V of a wide (20 μm) channel device	Few volts of the drain voltage beyond the beginning of the saturation region
19	**RDSW, RDSWMIN, A1, A2, PSCBE1, PSCBE2**	I_d vs. V_d at V_g = 3, 5, 7, 9, 11, 13, 15V and V_b = 0V of a wide (20 μm) channel device	Saturation region near V_d = VDD
20	**WINT**	$1/R_{DS}$ vs. W_{drawn} when devices are in linear and strong inversion region	Intercept of the x-axis
21	**K3, W0**	I_d vs. V_g at V_d = 0.5V and V_b = 0V of a narrow (4 μm) channel device	Moderate inversion
22	**K3B**	I_d vs. V_g at V_d = 0.5V and V_b = -3, -6, -9V of a narrow (4 μm) channel device	Moderate inversion
23	**B0, B1**	I_d vs. V_g at V_d = VDD and V_b = 0V of a narrow (4 μm) channel device	Strong inversion

Table 5.3. (Cont.)

Step No.	Parameter Name	Extraction Curves	Extraction Region
24	**CJD (CJS), MJD (MJS), PBD (PBS)**	C_{bd} vs. V_{bd} of high area junction diode	Reverse bias
25	**CJSWD (CJSWS), MJSWD (MJSWS), PBSWD (PBSWS)**	C_{bd} vs. V_{bd} of high periphery junction diode	Reverse bias
26	**NJD (NJS), JSD (JSS)**	Log(I_b) vs. V_{db} of high area junction diode	Forward bias
27	**JSWD (JSWS)**	Log(I_b) vs. V_{db} of high periphery junction diode	Forward bias
28	**IJTHDFWD (IJTHSFWD)**	I_b vs. V_{db} of high area junction diode	Forward bias

5.3.2 Model Optimization Results of SiC MOSFET with HSPICE BSIM4.6.5

Based on the extraction sequence outlined in section 5.3.1, parameters were extracted for both NMOSs and PMOSs and the model cards were added in the model library. Following is a brief description of the SiC MOSFET models developed based on BSIM4.6.5 HSPICE:

- PMOS models have good I_d-V_d, I_d-V_g, g_m-V_g, g_{ds}-V_d characteristics predictability. The models were generated by extracting and optimizing parameters from the measured data for a wide range of gate, drain and body biases. NMOS models have similar capability except the body effect could not be modeled quite accurately.
- As described in Chapter 4, three kinds of C-V measurements were taken for modeling purpose: oxide capacitance (C_{ox}), gate-to-source/drain/body capacitance (C_{gdsb}) and gate-to-source/drain (C_{gds}) capacitance. The gate drain overlap capacitance which significantly contributes to an amplifier's poles and zeroes, the gate-source capacitance which determines the switching speed of the digital circuits and the input capacitance (Cgs + Cgd) which is an important characteristic of a

power FET that could be optimized with the BSIM4's most advanced C-V model (**CAPMOD = 2**). The drain-body and the source-body junction capacitances were also modeled well.

- The parasitic drain-bulk and source-bulk diodes (body diode) which are very important when the FETs are used as power switches in a monolithic converter design were also modeled.
- The parasitic drain/source diffusion resistance was also modeled.
- For geometry scaling, a binning approach was followed since the process was found to have too much variation (especially PMOS) and could not be scaled globally. For NMOSs, five binning regions of channel length were chosen: 1.19 µm to 1.98 µm, 1.99 µm to 4 µm, 4.01 µm to 9 µm, 9.01 µm to 18 µm and 18.01 µm to 21 µm. For PMOSs, due to dramatic shift of threshold voltage (3-4 volts), four binning regions were chosen: 1.19 µm to 1.48 µm, 1.49 µm to 1.98 µm, 1.99 µm to 4.98 µm and 4.99 µm to 6.01 µm. For each region, channel width was chosen from 4 µm to 60 µm. Thus, any NMOS with channel length of 1.19 µm to 21 µm and any PMOS with channel length of 1.19 µm to 6.01 µm, in both cases with channel width of 4 µm to 60 µm, can be used in circuit simulation.
- For temperature scaling, the binning approach was also followed. Both NMOS and PMOS models are available for 25 ° C, 100 ° C, 200 ° C and 300 ° C temperature points.
- Significant aging was observed in the PMOSs at high temperatures. Model cards were generated for aged and non-aged versions at 200 ° C and 300 ° C.

- Since there is process variation from die to die, model cards were generated for slow and typical corners of NMOS and fast and typical corners of PMOS.

The accuracy of the model optimization for both NMOS and PMOS are shown in Fig. 5.9 Fig. 5.90. In the plots, solid lines and symbols represent simulated and measured data respectively.

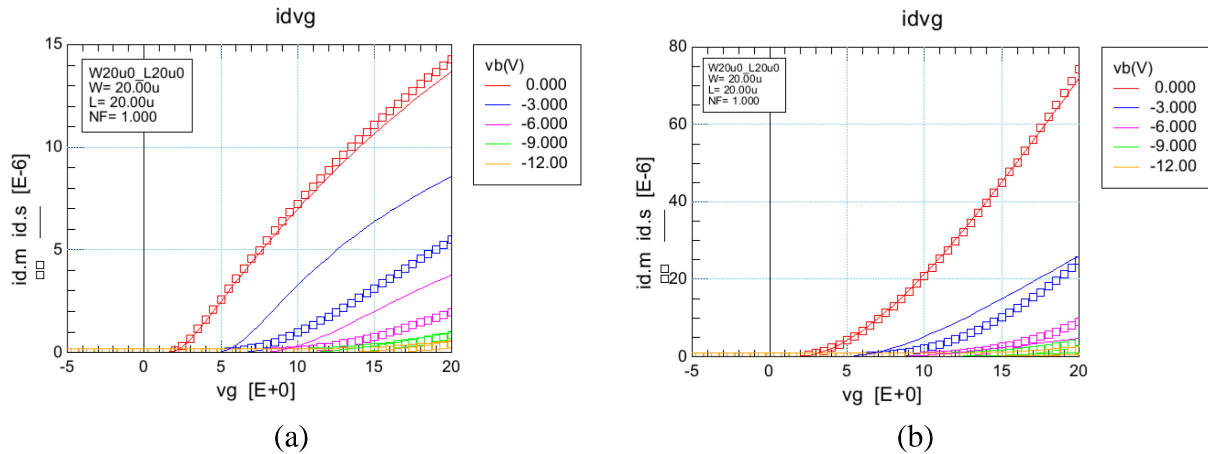


Fig. 5.9. Transfer characteristics of a 20 µm / 20 µm (wide and long) NMOS at 25 º C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

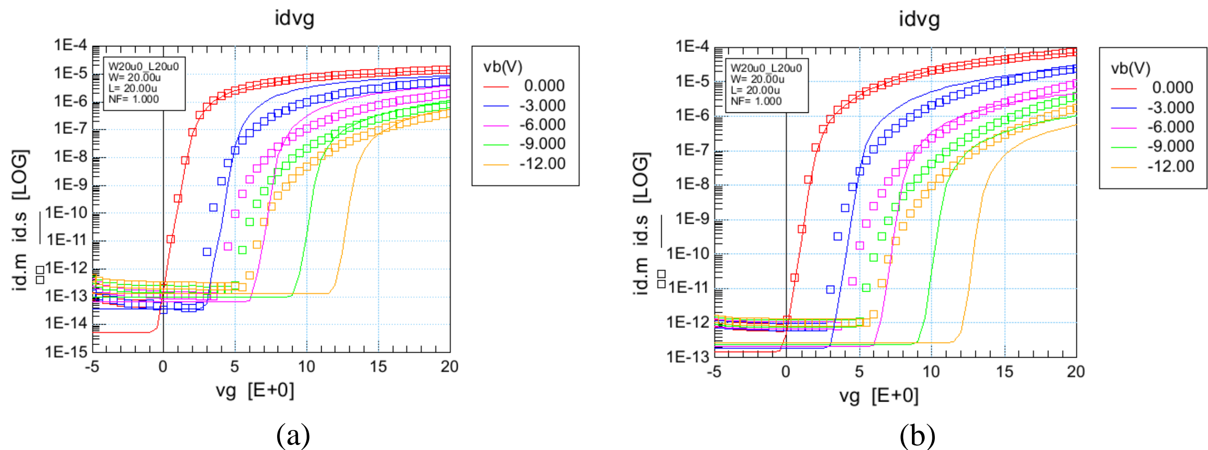
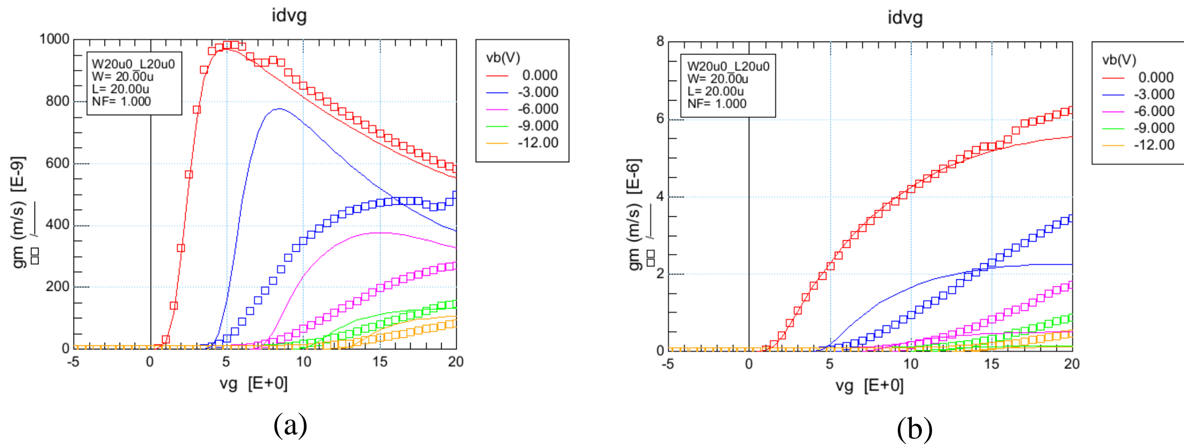
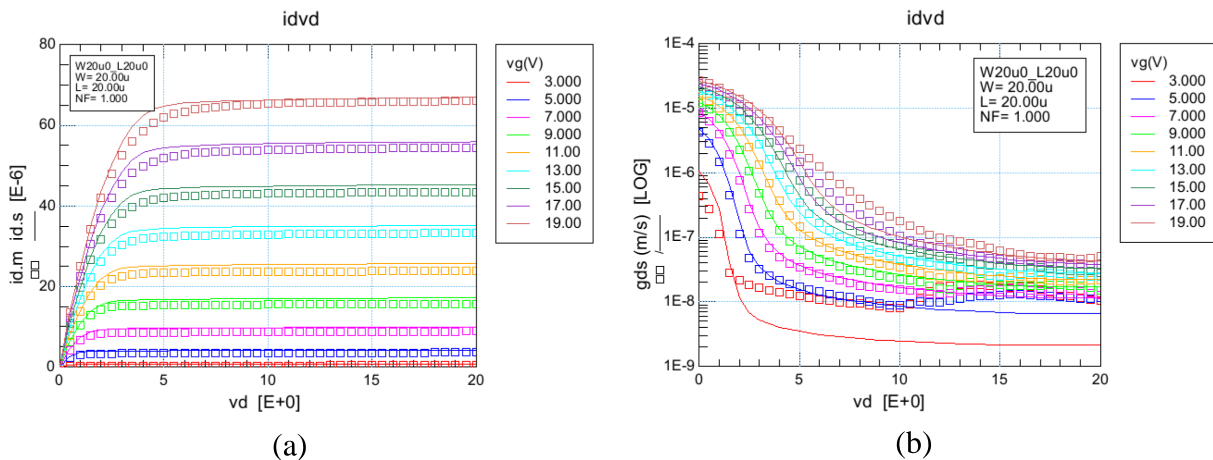


Fig. 5.10. Transfer characteristics of a 20 µm / 20 µm (wide and long) NMOS at 25 º C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



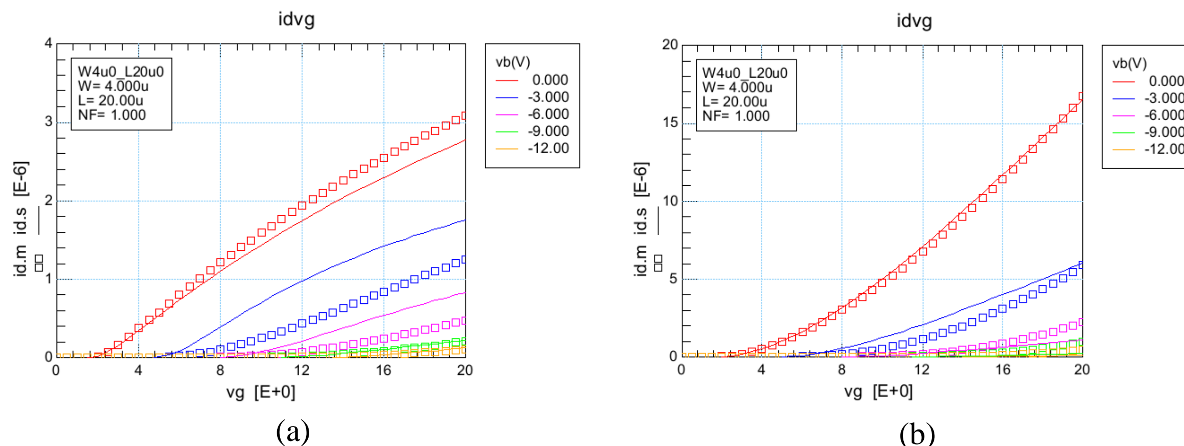
(a) (b)

Fig. 5.11. Transconductance of a 20 µm / 20 µm (wide and long) NMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 5.12. (a) Output characteristics and (b) output conductance of a 20 µm / 20 µm (wide and long) NMOS at 25 ° C.



(a) (b)

Fig. 5.13. Transfer characteristics of a 4 µm / 20 µm (narrow and long) NMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

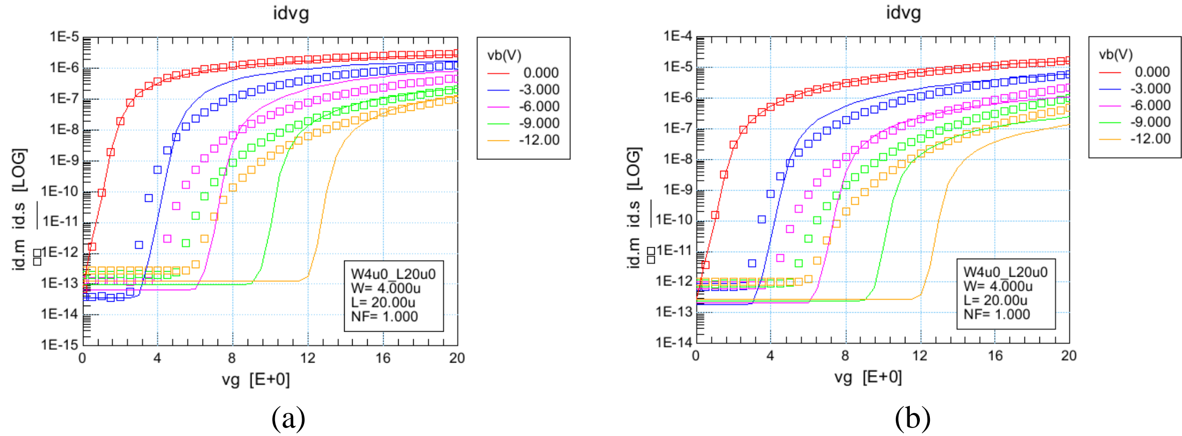


Fig. 5.14. Transfer characteristics of a 4 µm / 20 µm (narrow and long) NMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

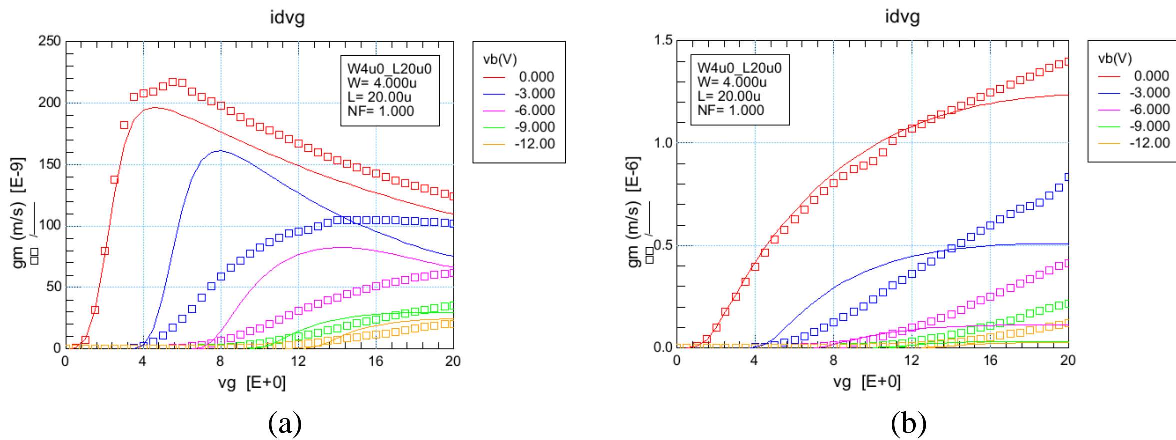


Fig. 5.15. Transconductance of a 4 µm / 20 µm (narrow and long) NMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

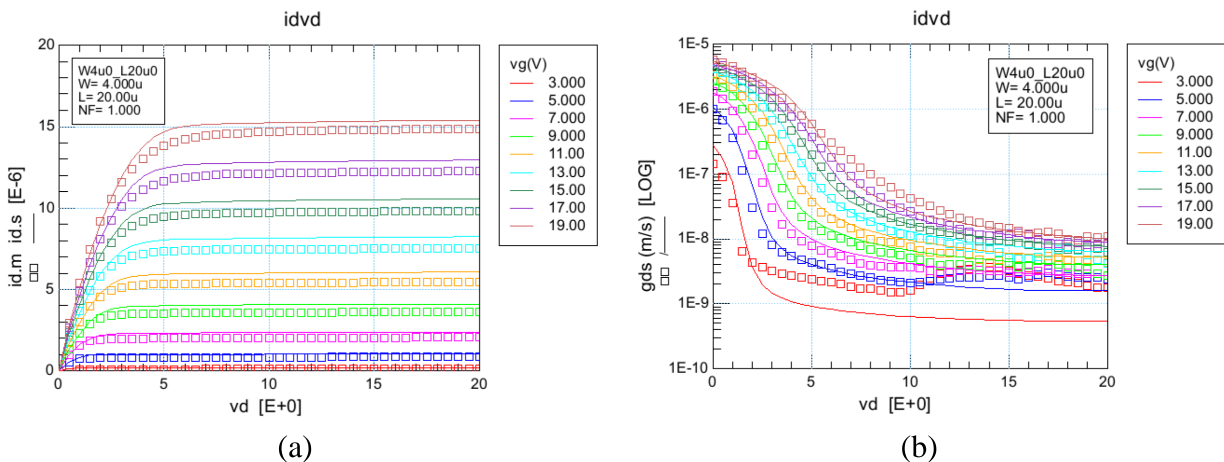
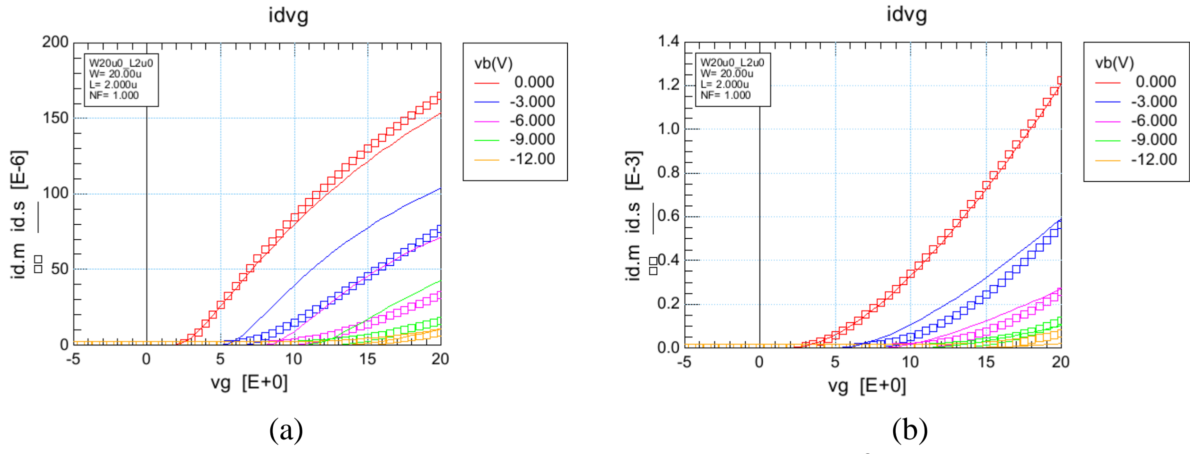
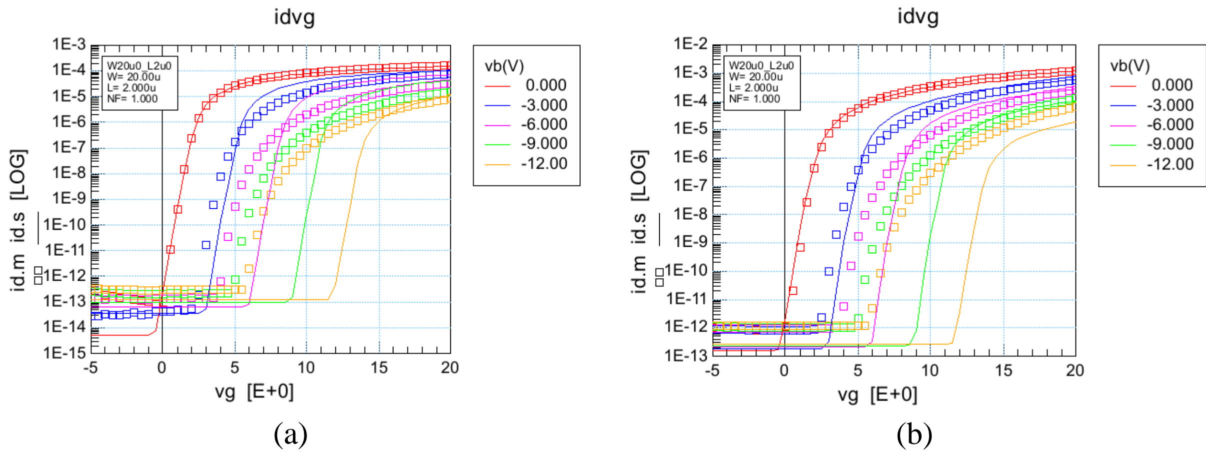


Fig. 5.16. (a) Output characteristics and (b) output conductance of a 4 µm / 20 µm (narrow and long) NMOS at 25 ° C.



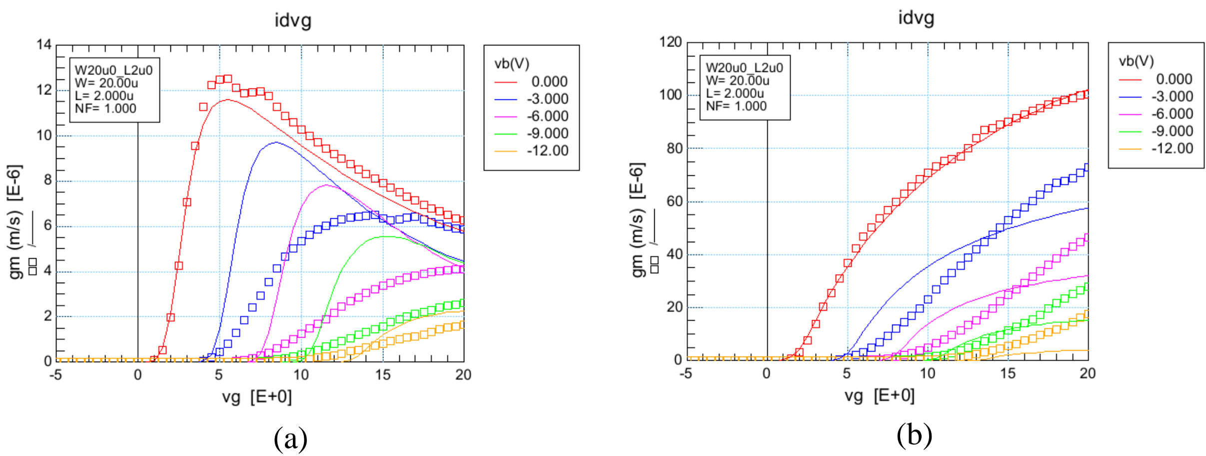
(a) (b)

Fig. 5.17. Transfer characteristics of a 20 µm / 2 µm NMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



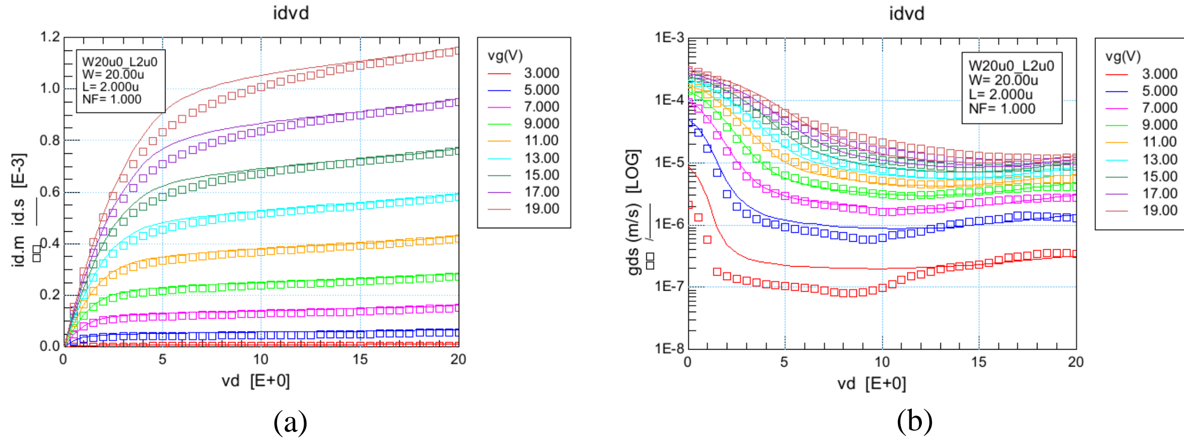
(a) (b)

Fig. 5.18. Transfer characteristics of a 20 µm / 2 µm NMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



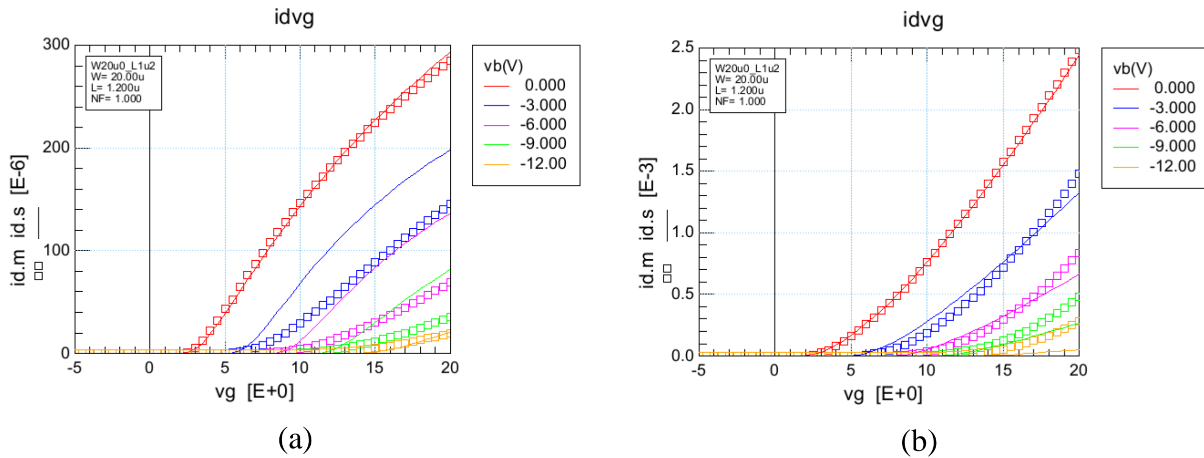
(a) (b)

Fig. 5.19. Transconductance of a 20 µm / 2 µm NMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



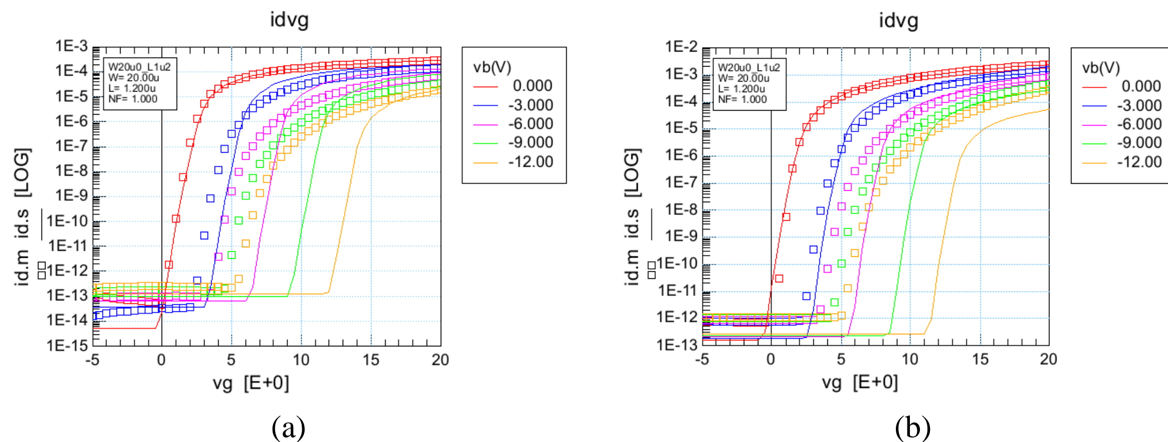
(a) (b)

Fig. 5.20. (a) Output characteristics and (b) output conductance of a 20 μm / 2 μm NMOS at 25 ⁰ C.



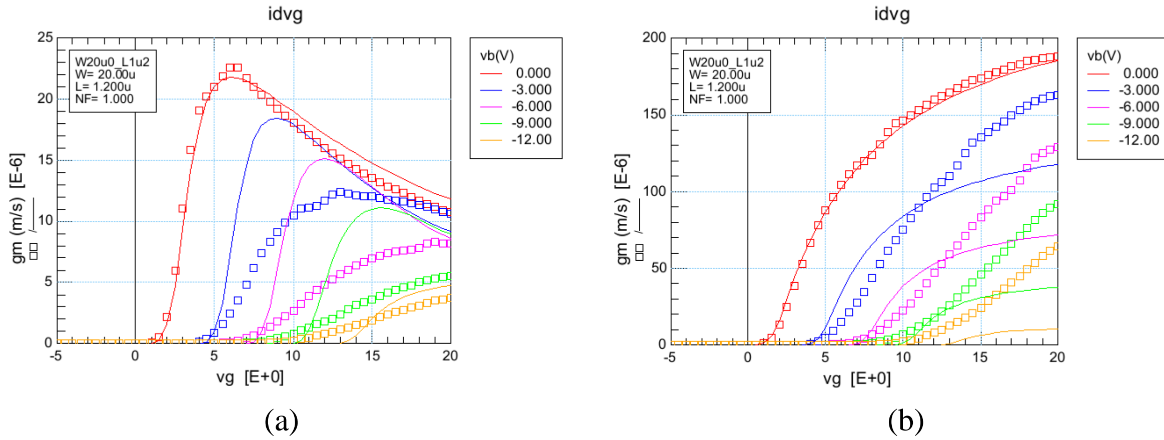
(a) (b)

Fig. 5.21. Transfer characteristics of a 20 μm / 1.2 μm (wide and short) NMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



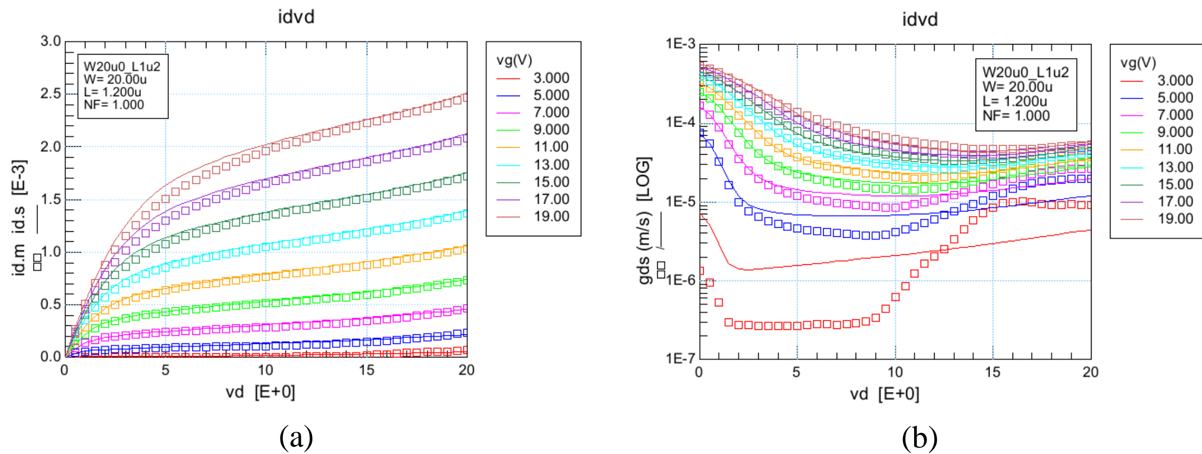
(a) (b)

Fig. 5.22. Transfer characteristics of a 20 μm / 1.2 μm (wide and short) NMOS at 25 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



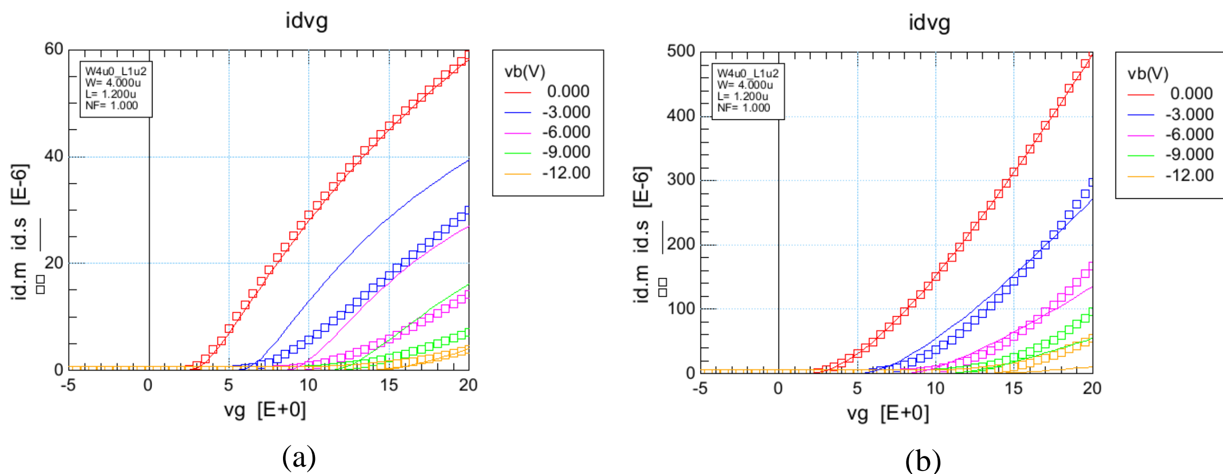
(a) (b)

Fig. 5.23. Transconductance of a 20 µm / 1.2 µm (wide and short) NMOS at 25 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



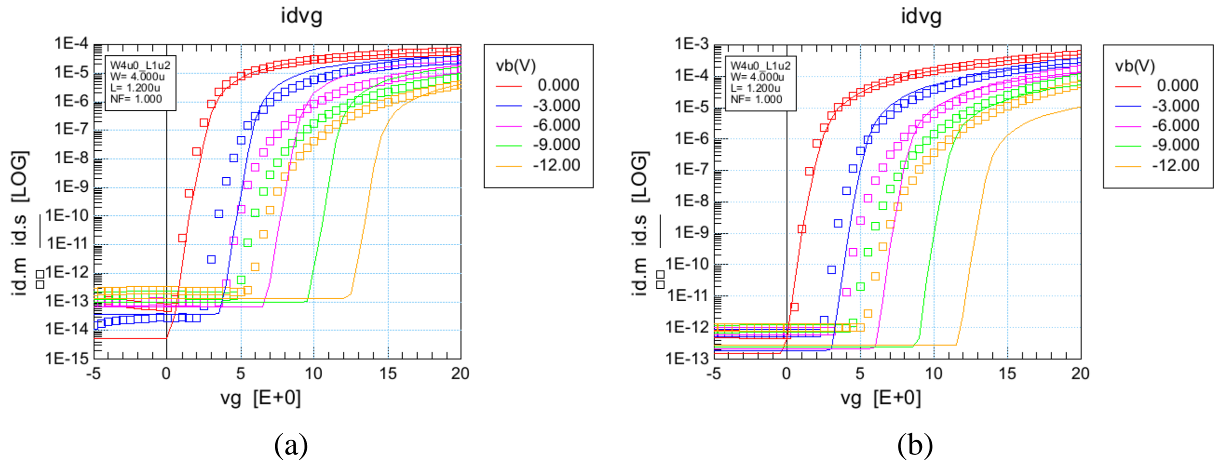
(a) (b)

Fig. 5.24. (a) Output characteristics and (b) output conductance of a 20 µm / 1.2 µm (wide and short) NMOS at 25 ⁰ C.



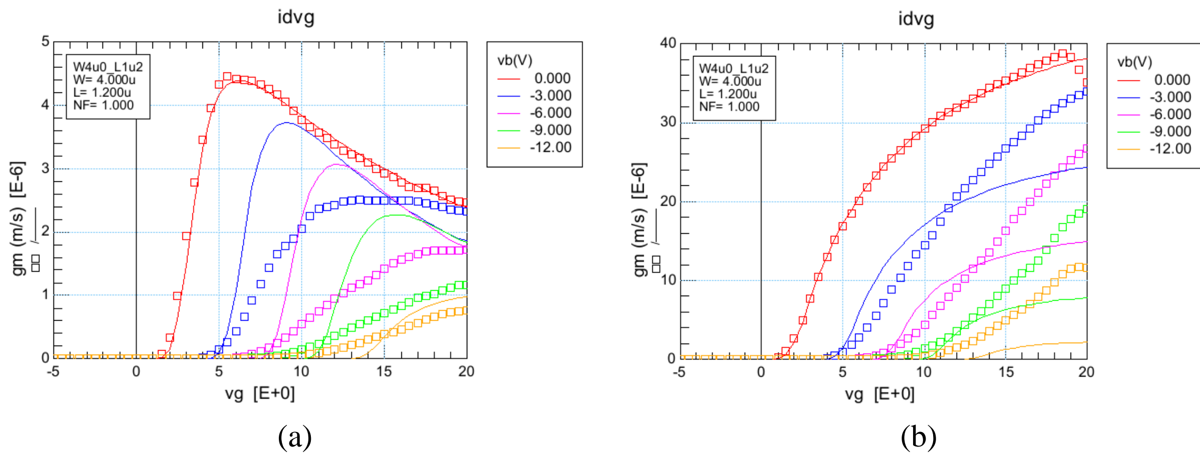
(a) (b)

Fig. 5.25. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



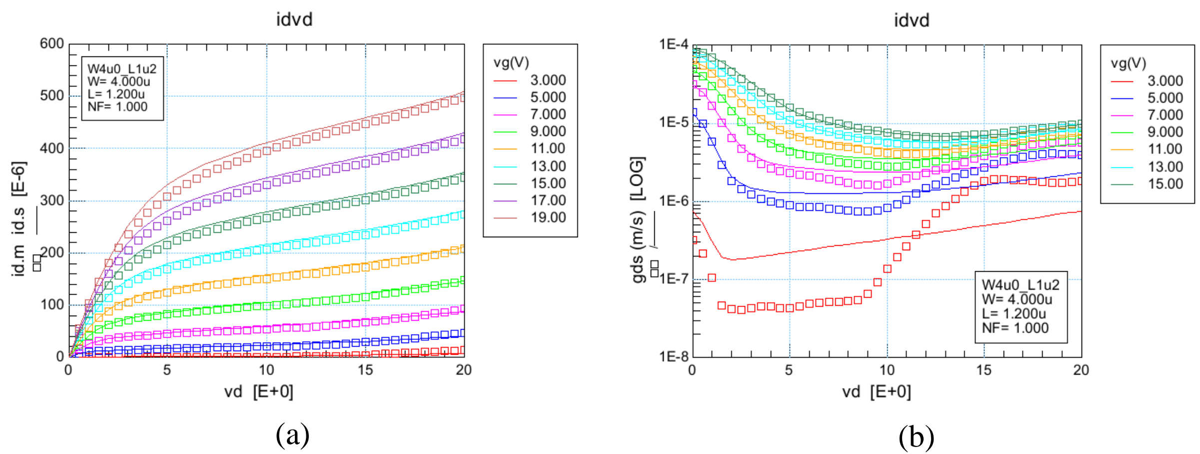
(a) (b)

Fig. 5.26. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



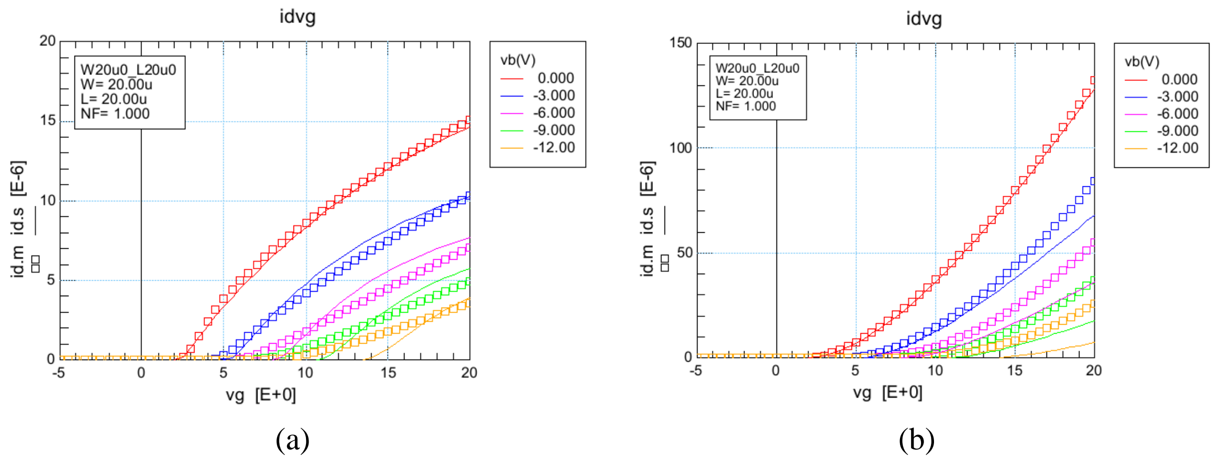
(a) (b)

Fig. 5.27. Transconductance of a 4 µm / 1.2 µm (narrow and short) NMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



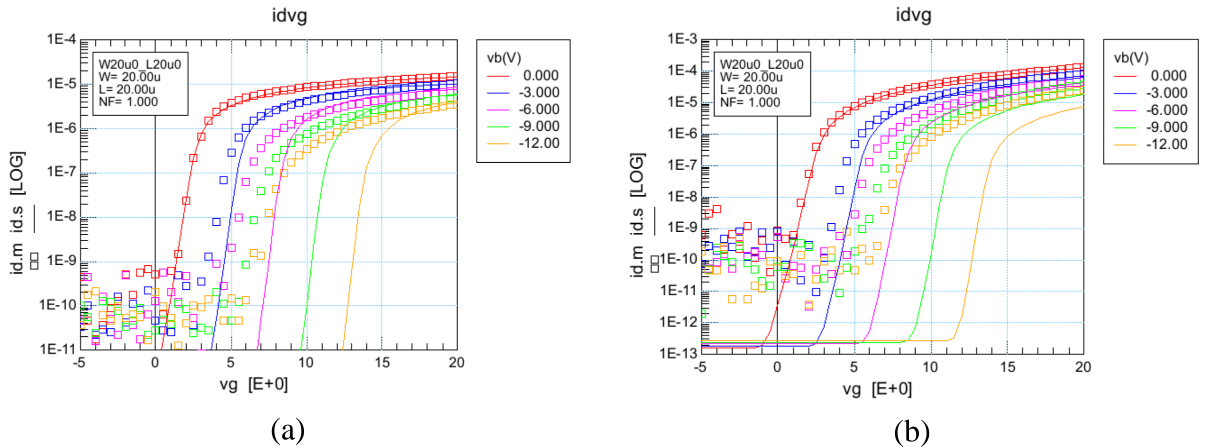
(a) (b)

Fig. 5.28. (a) Output characteristics and (b) output conductance of a 4 µm / 1.2 µm (narrow and short) NMOS at 25 ° C.



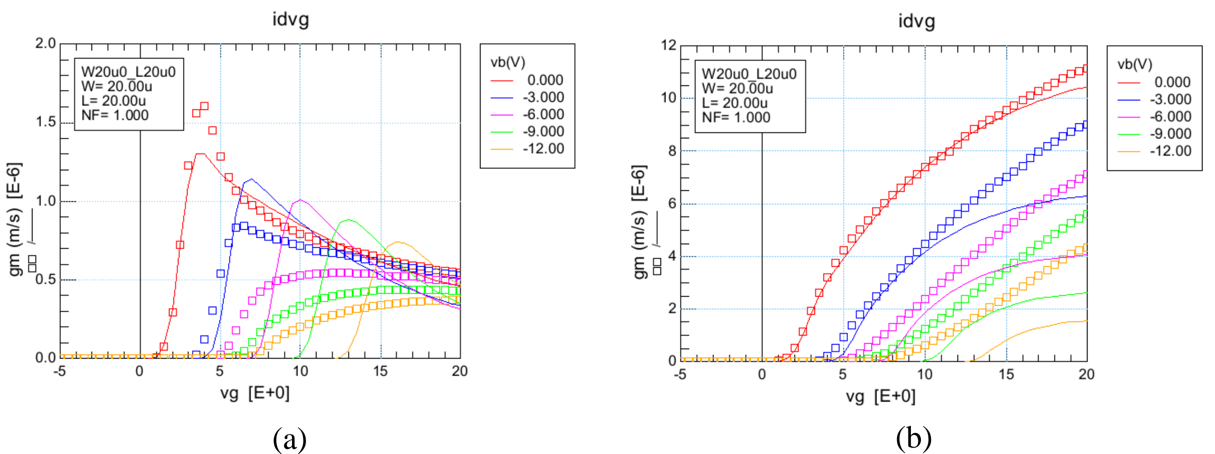
(a) (b)

Fig. 5.29. Transfer characteristics of a 20 µm / 20 µm (wide and long) NMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



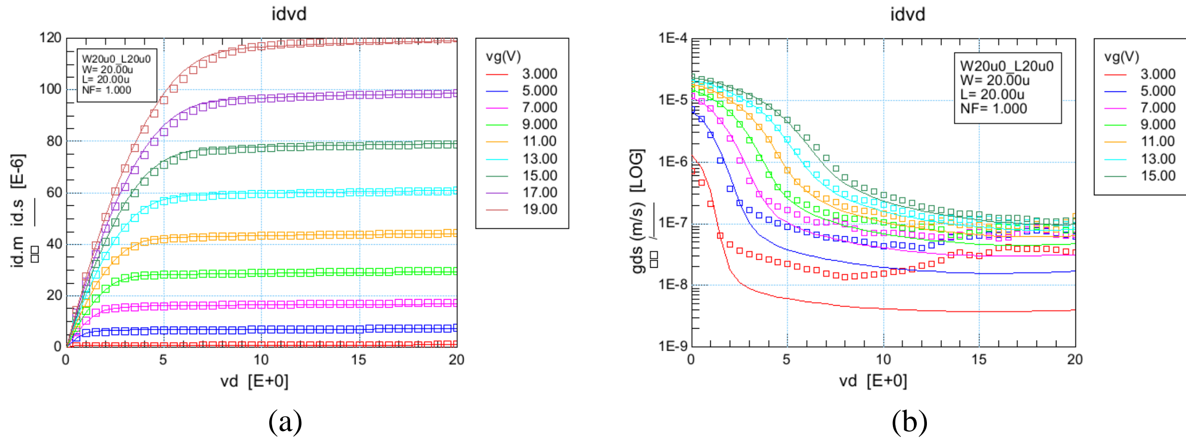
(a) (b)

Fig. 5.30. Transfer characteristics of a 20 µm / 20 µm (wide and long) NMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



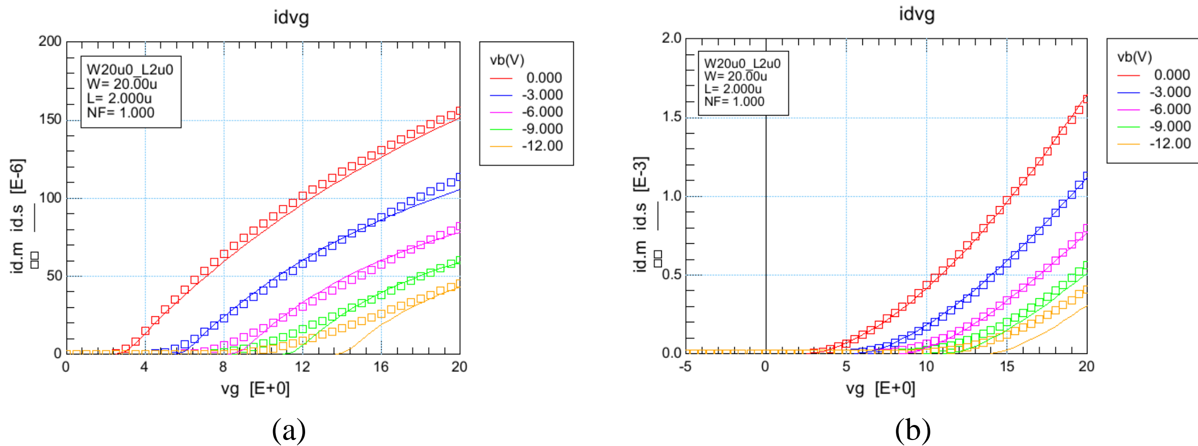
(a) (b)

Fig. 5.31. Transconductance of a 20 µm / 20 µm (wide and long) NMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



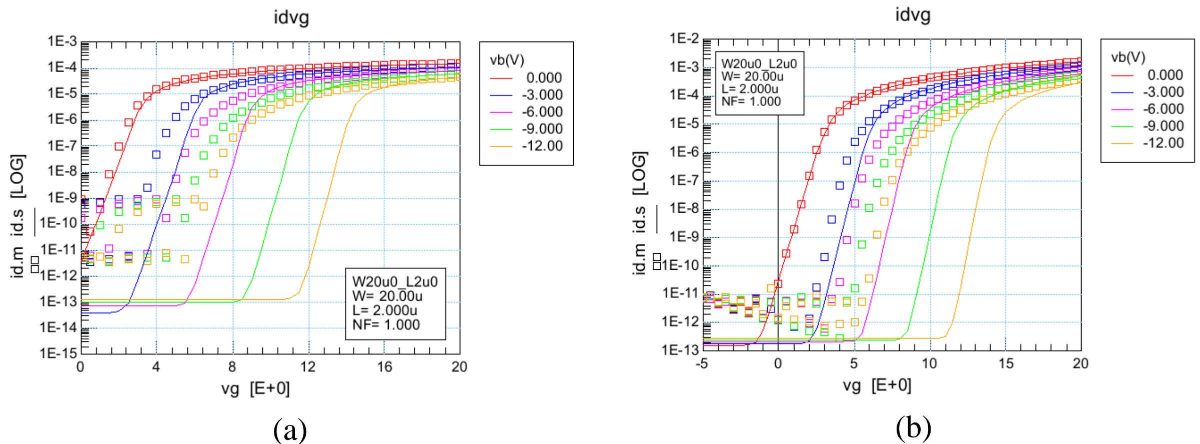
(a) (b)

Fig. 5.32. (a) Output characteristics and (b) output conductance of a 20 μm / 20 μm (wide and long) NMOS at 300 ⁰ C.



(a) (b)

Fig. 5.33. Transfer characteristics of a 20 μm / 2 μm NMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 5.34. Transfer characteristics of a 20 μm / 2 μm NMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

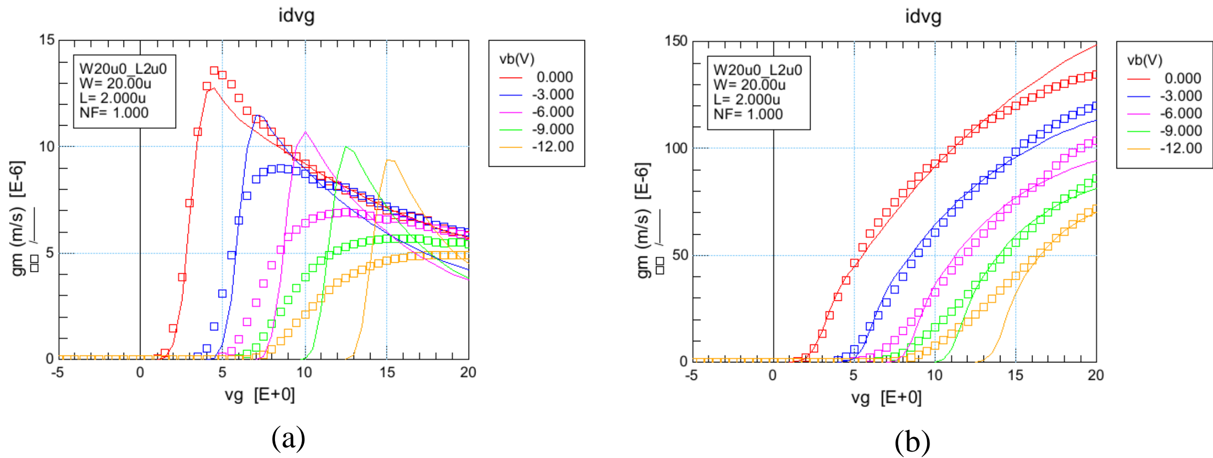


Fig. 5.35. Transconductance of a 20 µm / 2 µm NMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

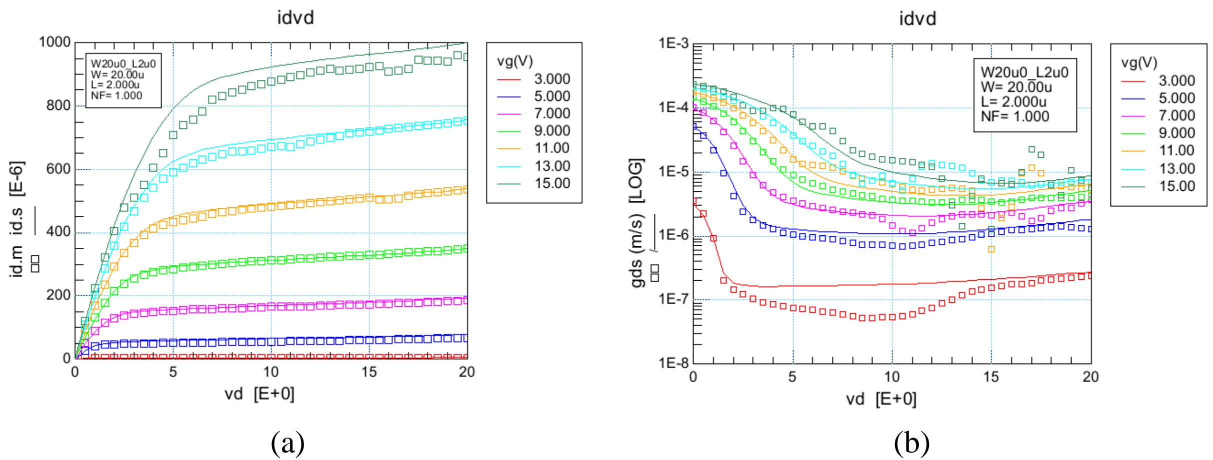


Fig. 5.36. (a) Output characteristics and (b) output conductance of a 20 µm / 2 µm NMOS at 300 ⁰ C.

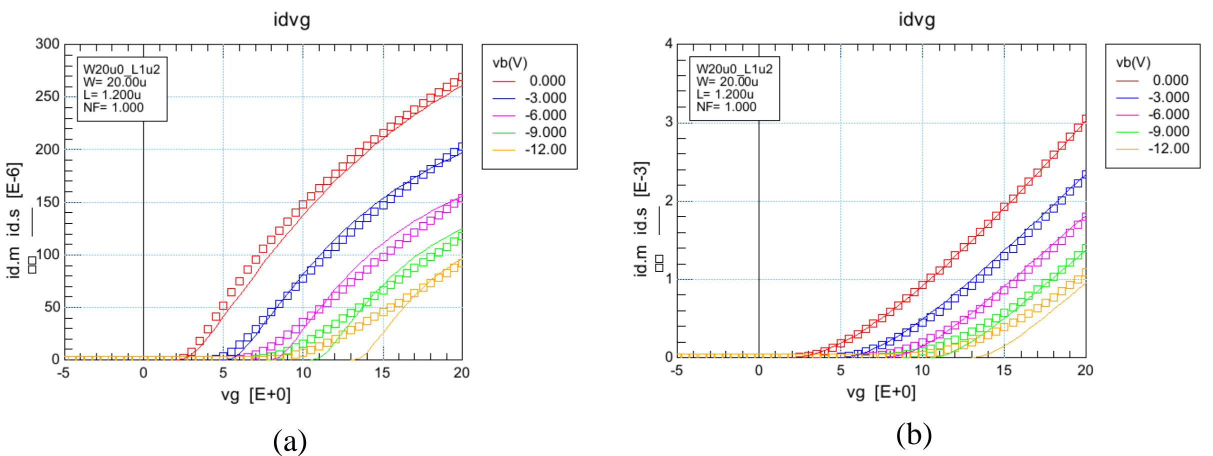
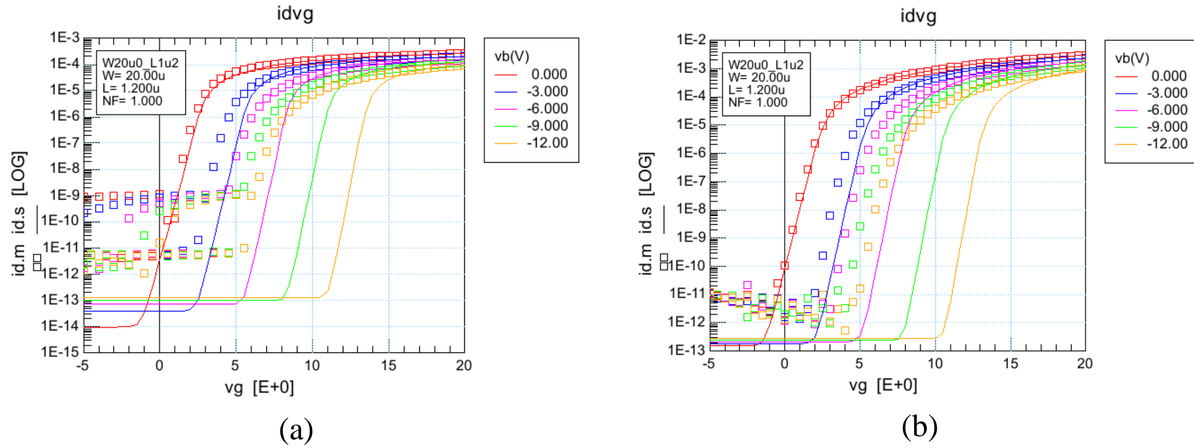
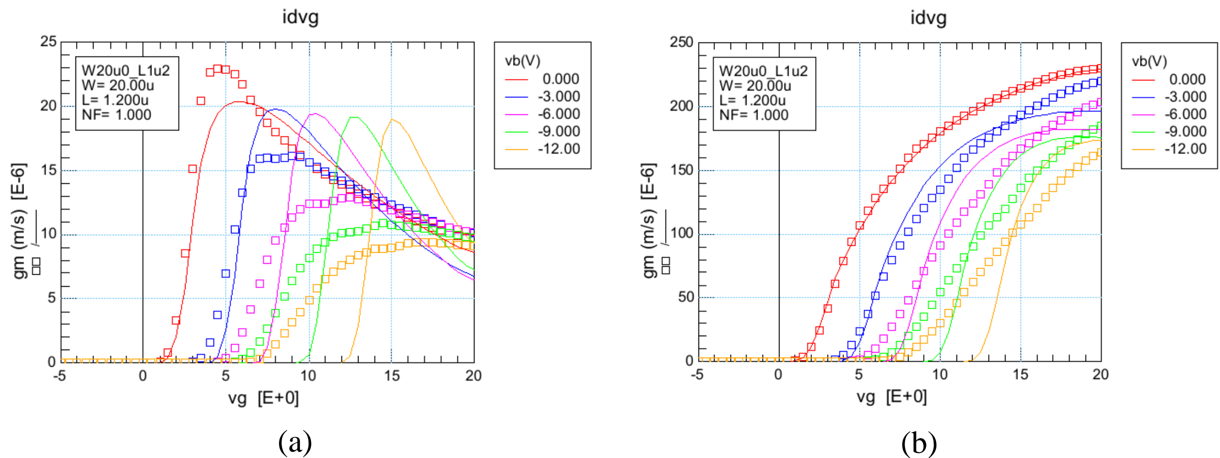


Fig. 5.37. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



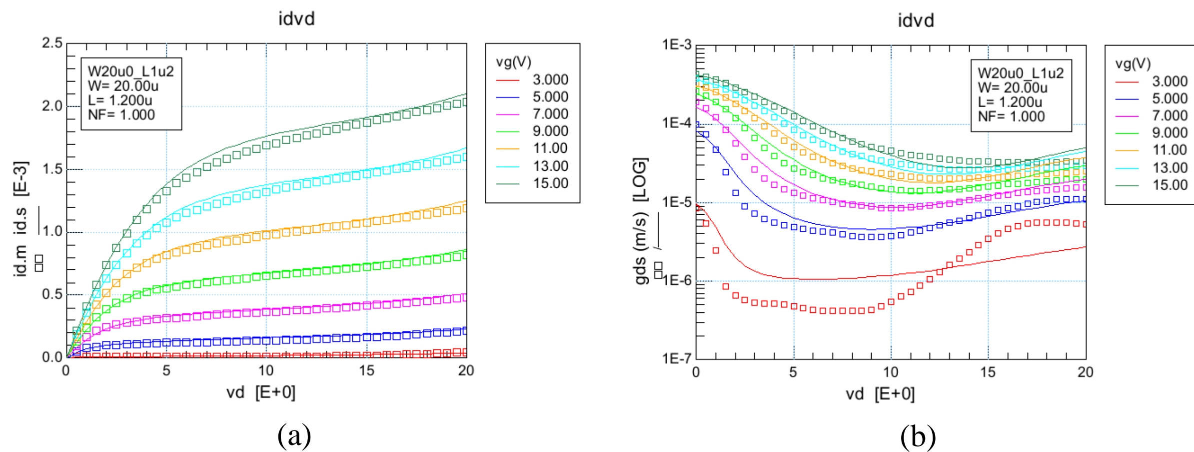
(a) (b)

Fig. 5.38. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



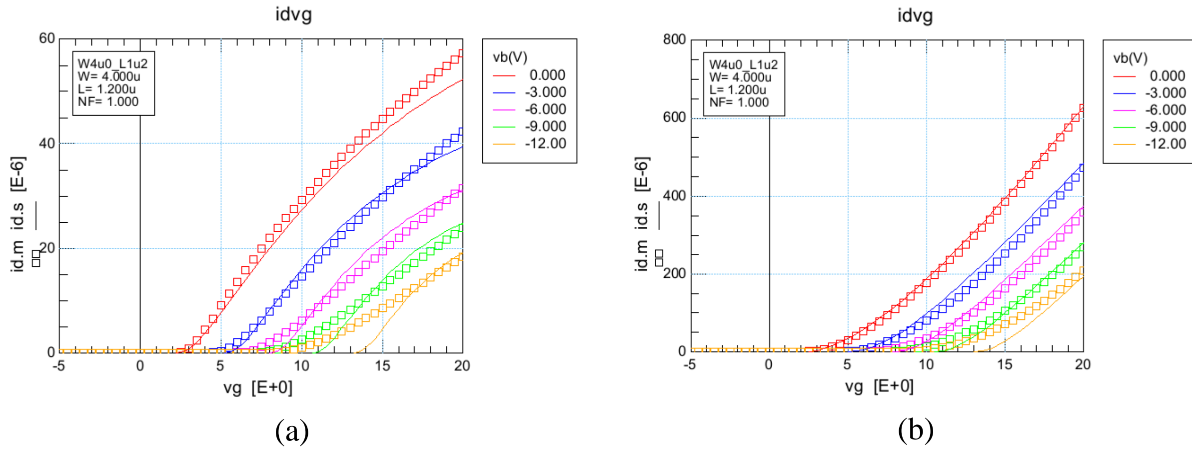
(a) (b)

Fig. 5.39. Transconductance of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



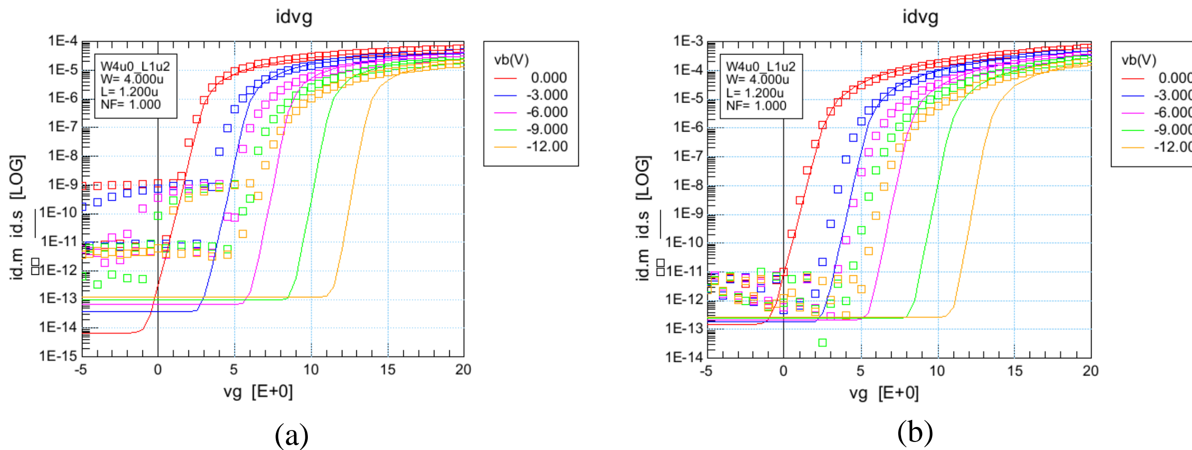
(a) (b)

Fig. 5.40. (a) Output characteristics and (b) output conductance of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ° C.



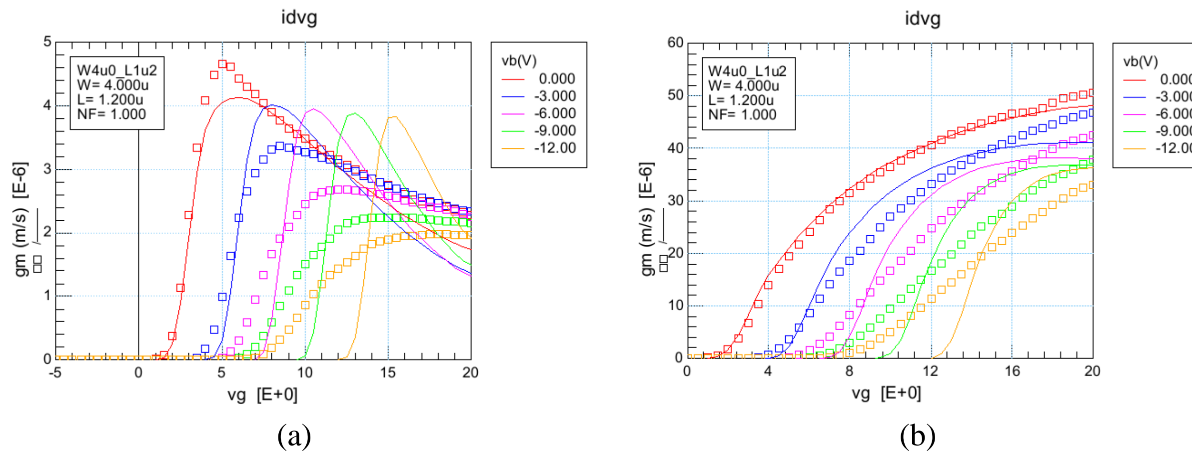
(a) (b)

Fig. 5.41. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



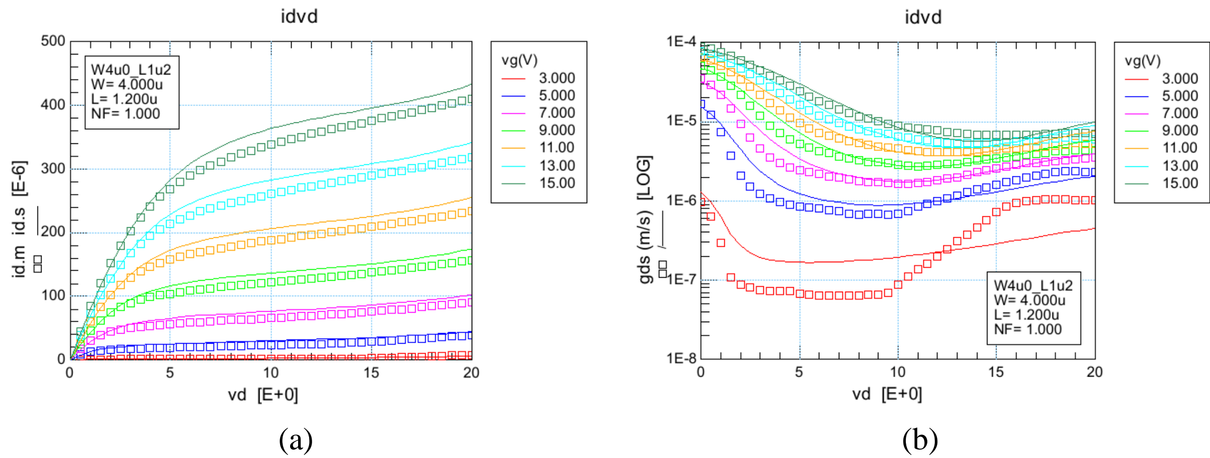
(a) (b)

Fig. 5.42. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



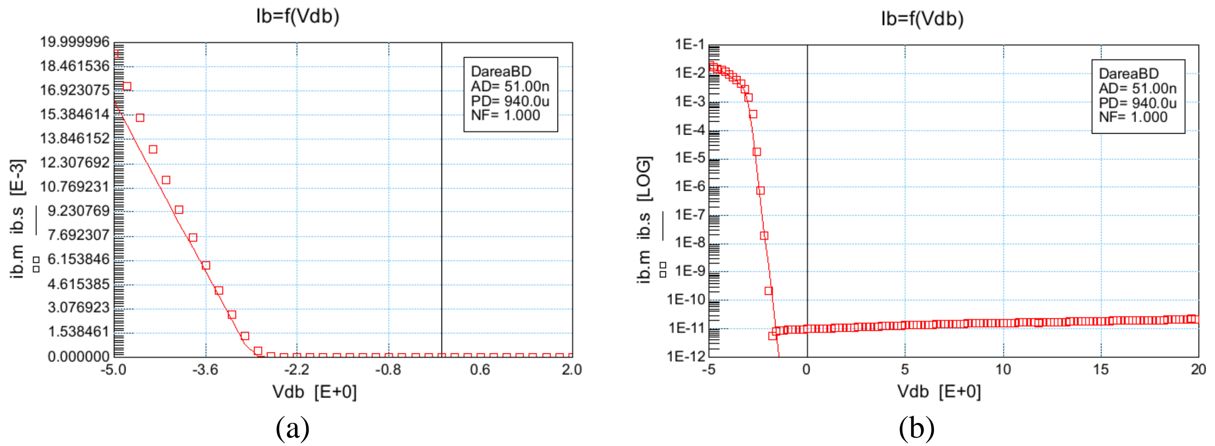
(a) (b)

Fig. 5.43. Transconductance of a 4 µm / 1.2 µm (narrow and short) NMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



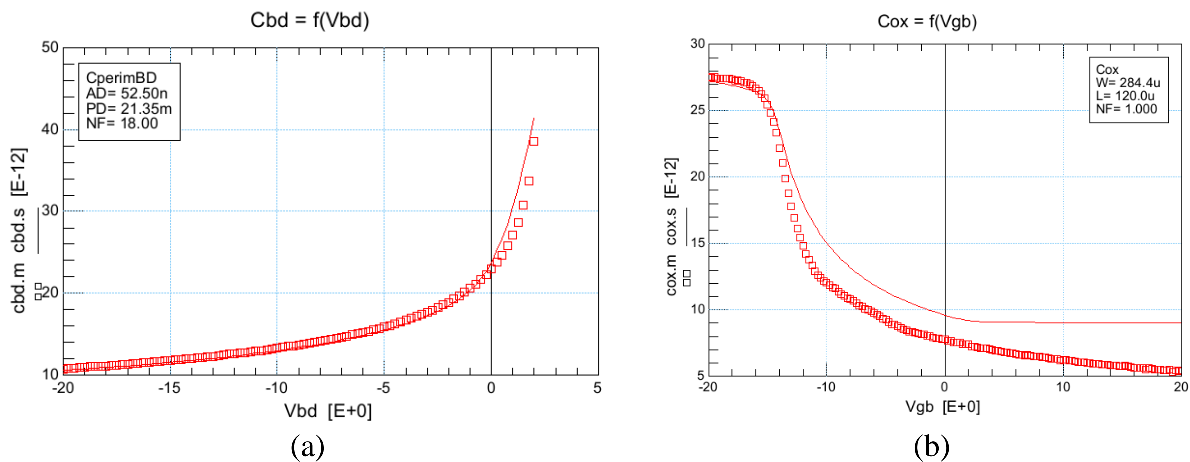
(a) (b)

Fig. 5.44. (a) Output characteristics and (b) output conductance of a 4 μm / 1.2 μm (narrow and short) NMOS at 300 ° C.



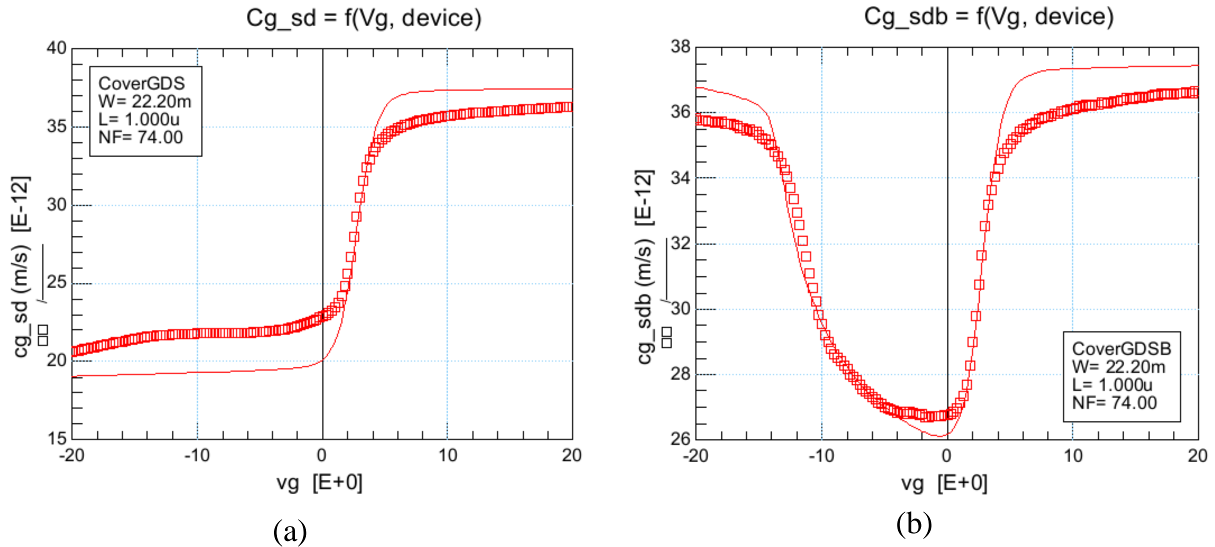
(a) (b)

Fig. 5.45. Drain/source (n+)-to-body (p-well) diode I – V characteristics in (a) linear scale and (b) log scale.



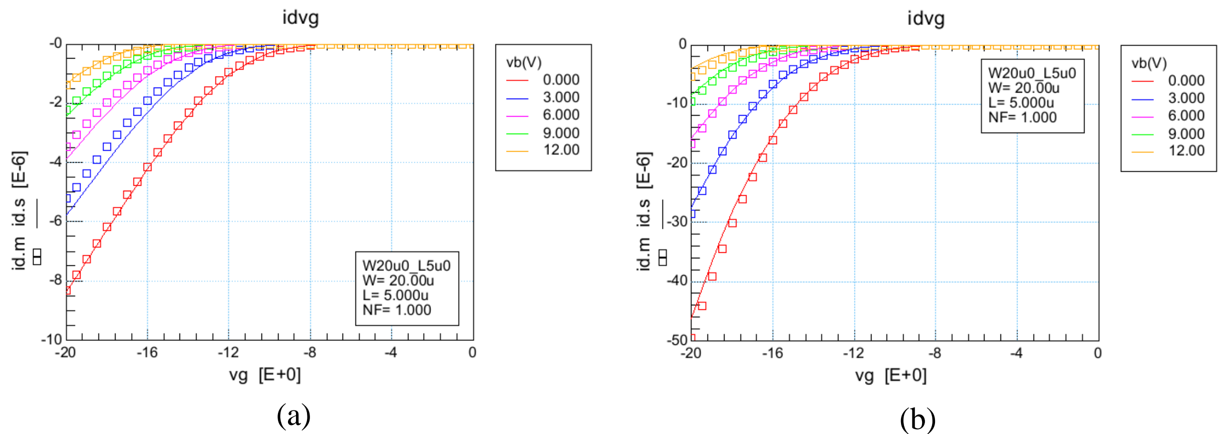
(a) (b)

Fig. 5.46. (a) Drain/source (n+)-to-body (p-well) junction diode C – V and (b) NMOS oxide capacitance.



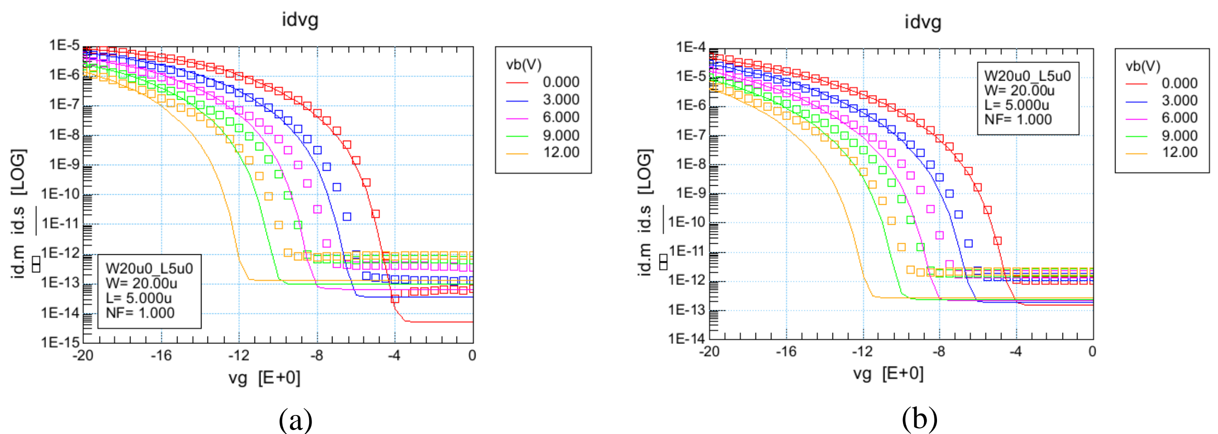
(a) (b)

Fig. 5.47. (a) Gate-to-drain/source overlap and intrinsic capacitance and (b) gate-to-drain/source/body total capacitance of an NMOS.



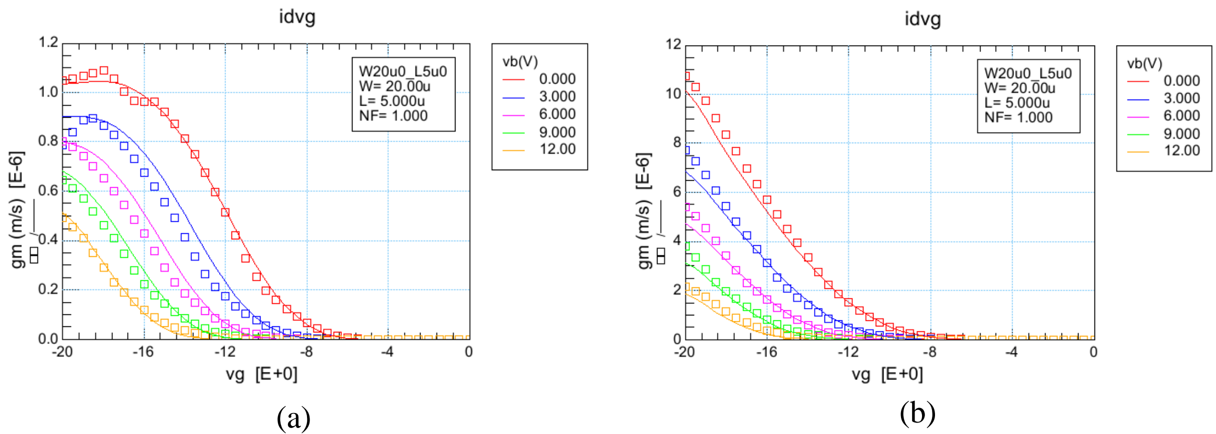
(a) (b)

Fig. 5.48. Transfer characteristics of a 20 μm / 5 μm (wide and long) PMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



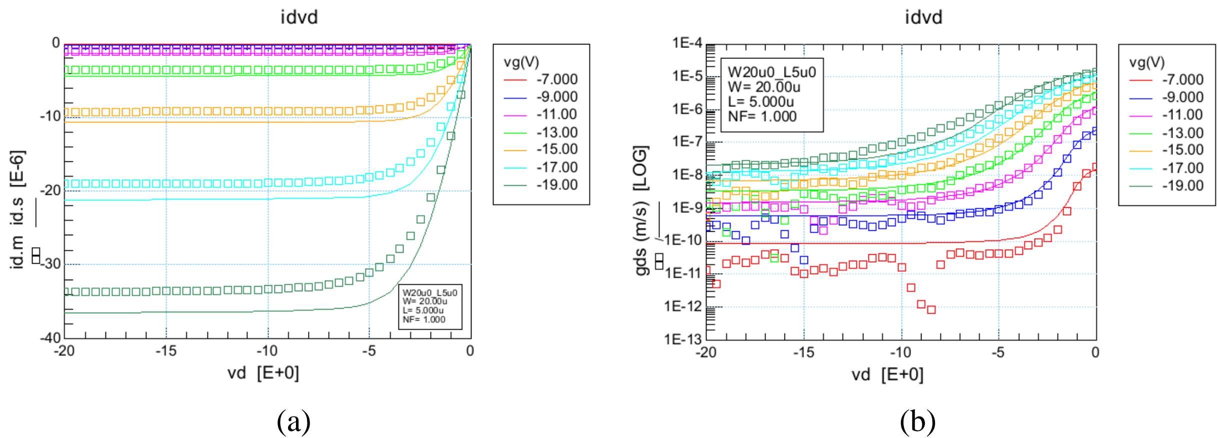
(a) (b)

Fig. 5.49. Transfer characteristics of a 20 μm / 5 μm (wide and long) PMOS at 25 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



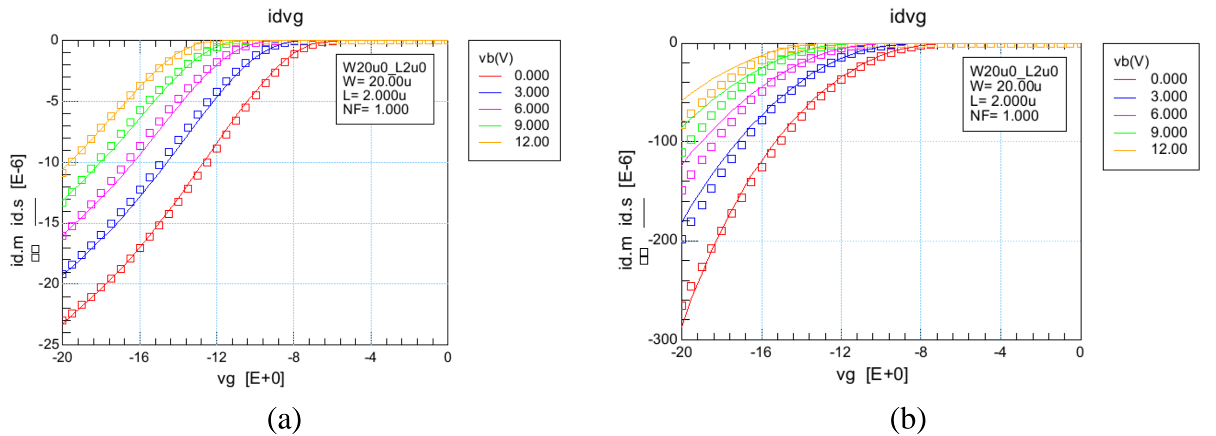
(a) (b)

Fig. 5.50. Transconductance of a 20 µm / 5 µm (wide and long) PMOS at 25 º C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



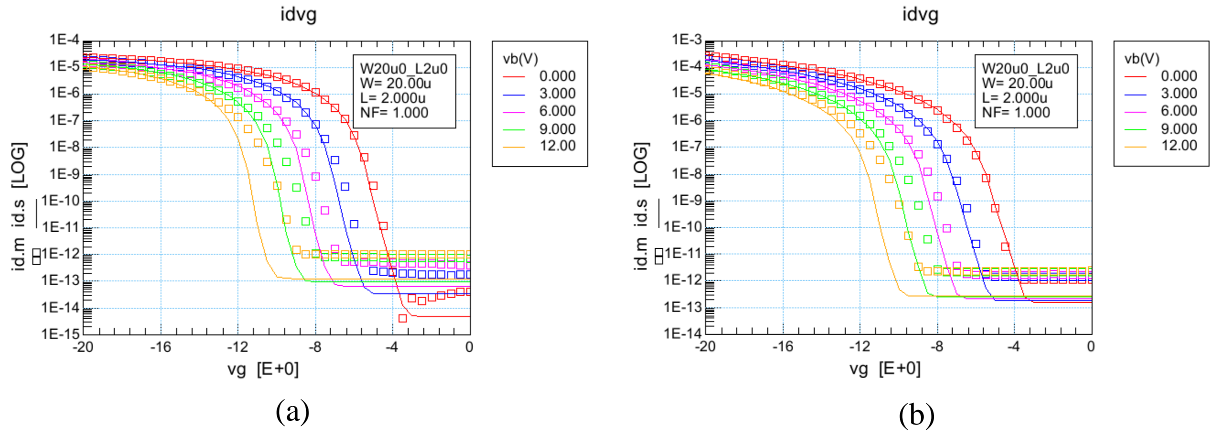
(a) (b)

Fig. 5.51. (a) Output characteristics and (b) output conductance of a 20 µm / 5 µm (wide and long) PMOS at 25 º C.



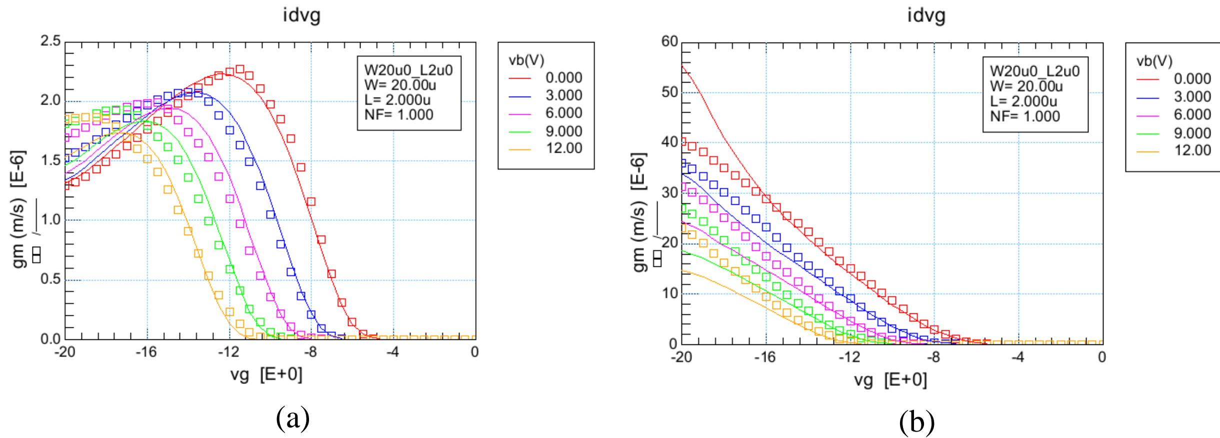
(a) (b)

Fig. 5.52. Transfer characteristics of a 20 µm / 2 µm PMOS at 25 º C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



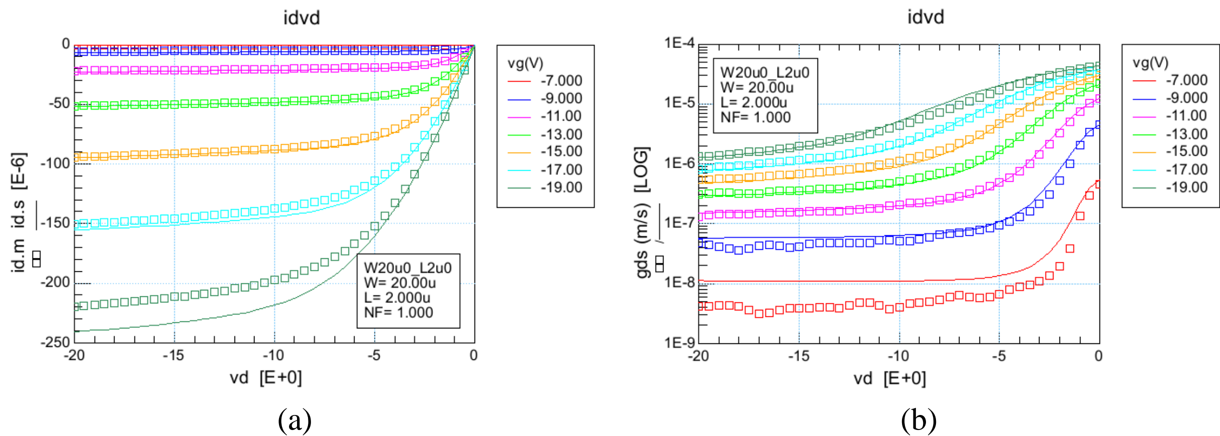
(a) (b)

Fig. 5.53. Transfer characteristics of a 20 μm / 2 μm PMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



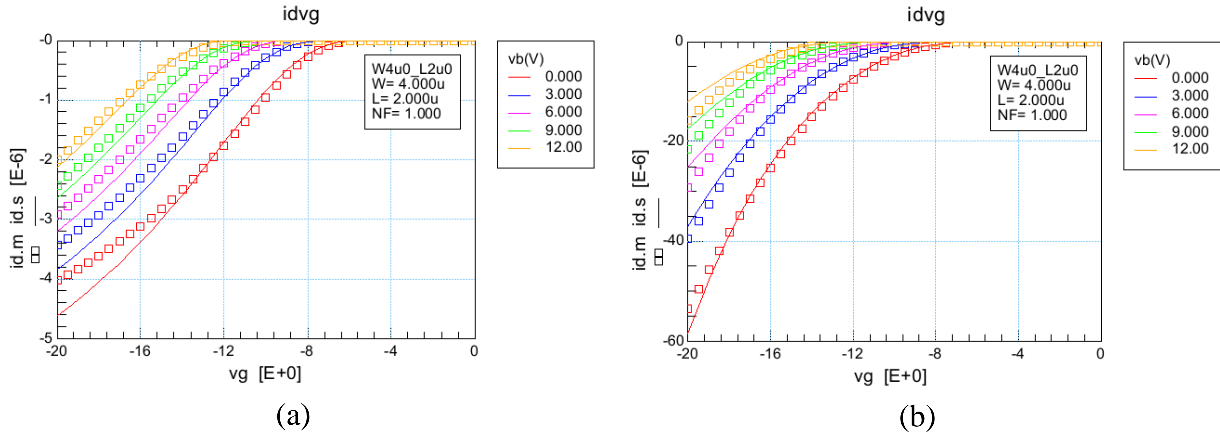
(a) (b)

Fig. 5.54. Transconductance of a 20 μm / 2 μm PMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



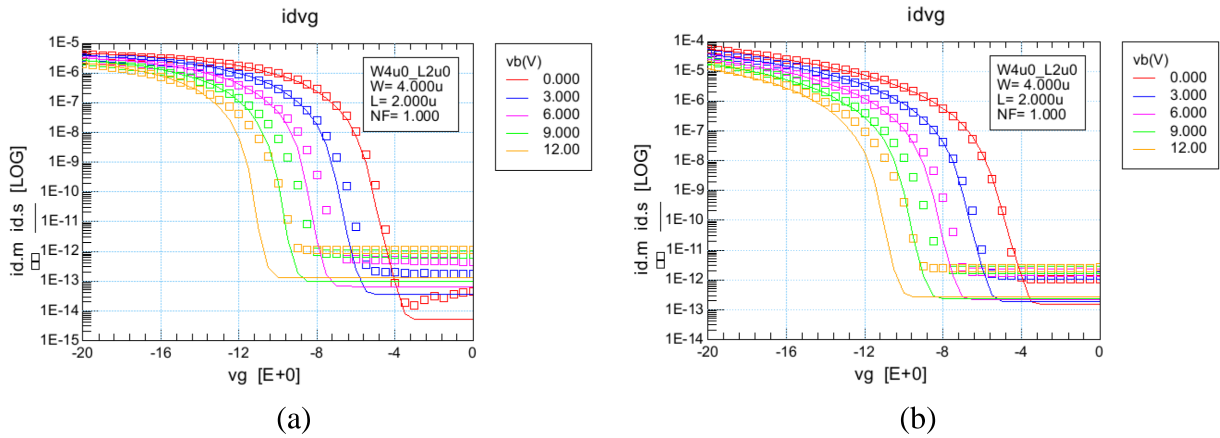
(a) (b)

Fig. 5.55. a) Output characteristics and (b) output conductance of a 20 μm / 2 μm PMOS at 25 ° C.



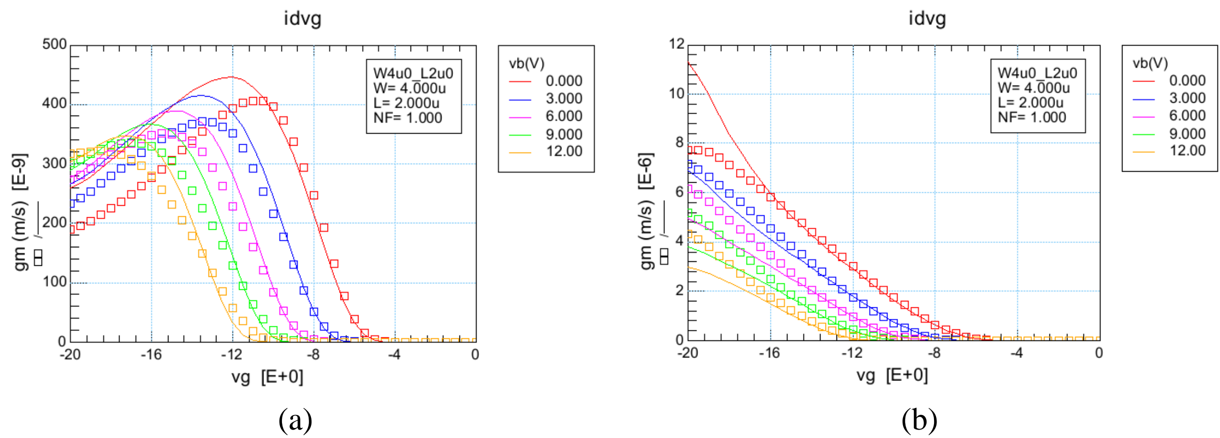
(a) (b)

Fig. 5.56. Transfer characteristics of a 4 µm / 2 µm PMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



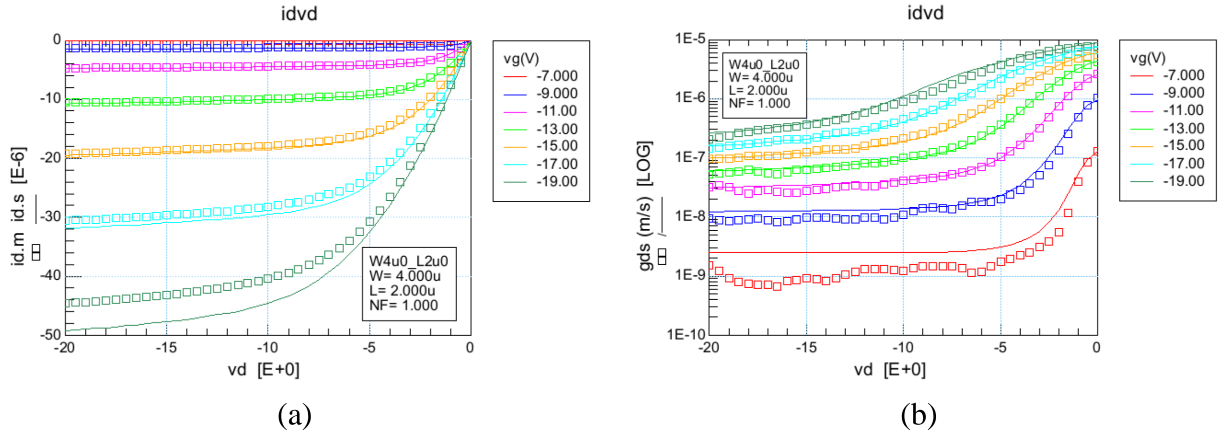
(a) (b)

Fig. 5.57. Transfer characteristics of a 4 µm / 2 µm PMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



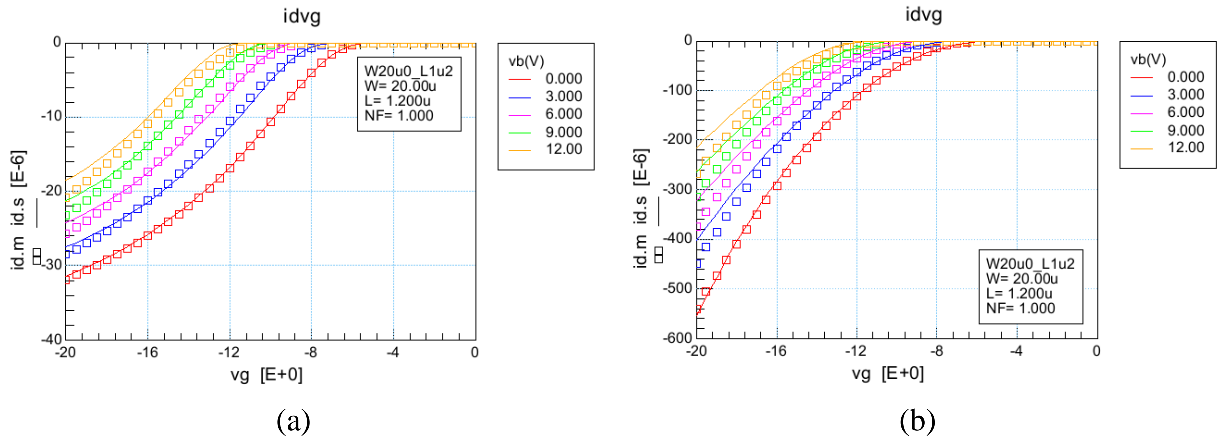
(a) (b)

Fig. 5.58. Transconductance of a 4 µm / 2 µm PMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



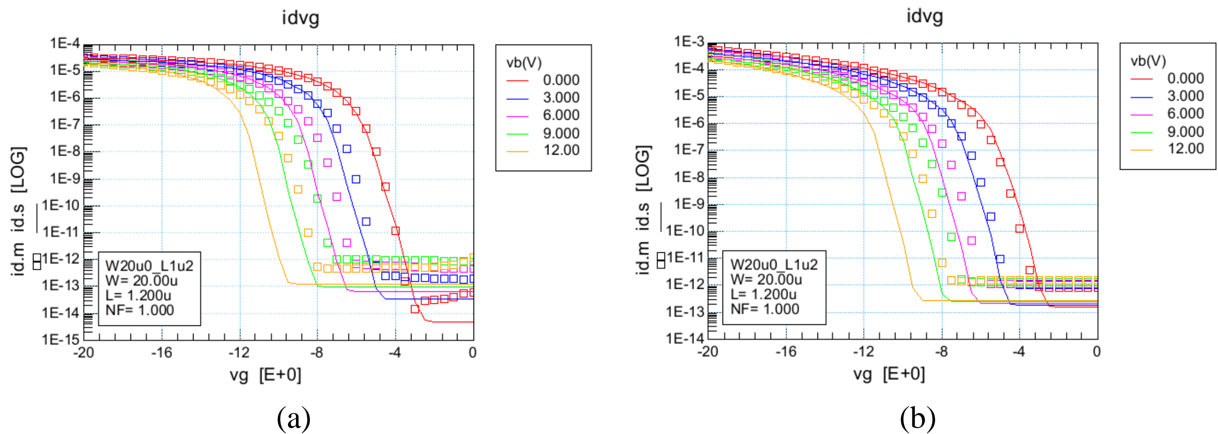
(a) (b)

Fig. 5.59. a) Output characteristics and (b) output conductance of a 4 µm / 2 µm PMOS at 25 ° C.



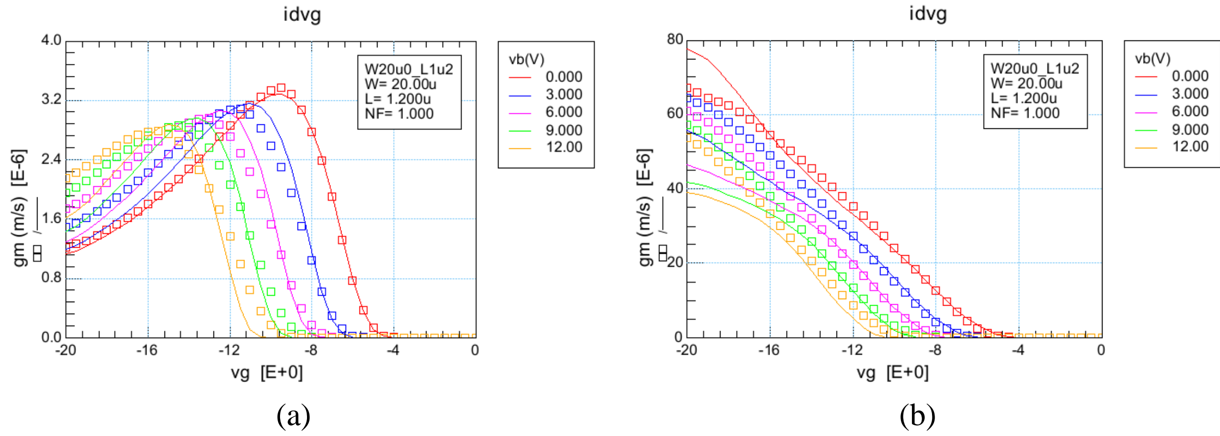
(a) (b)

Fig. 5.60. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) PMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



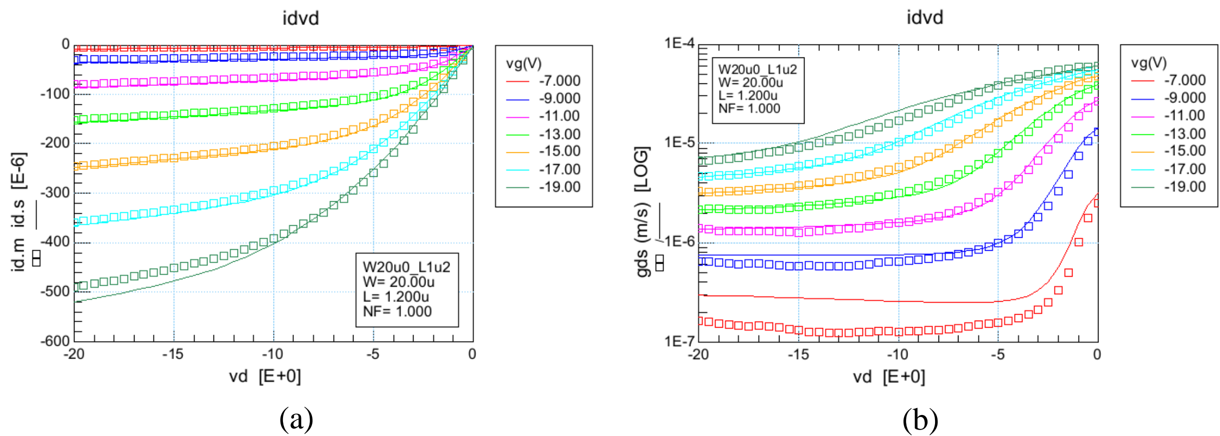
(a) (b)

Fig. 5.61. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) PMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



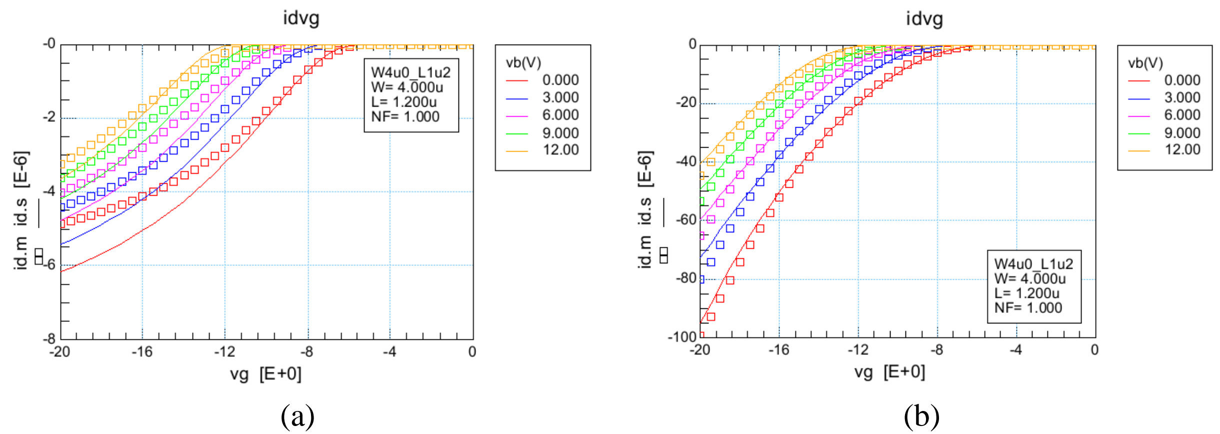
(a) (b)

Fig. 5.62. Transconductance of a 20 μm / 1.2 μm (wide and short) PMOS at 25 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 5.63. a) Output characteristics and (b) output conductance of a 20 μm / 1.2 μm (wide and short) PMOS at 25 ⁰ C.



(a) (b)

Fig. 5.64. Transfer characteristics of a 4 μm / 1.2 μm (narrow and short) PMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

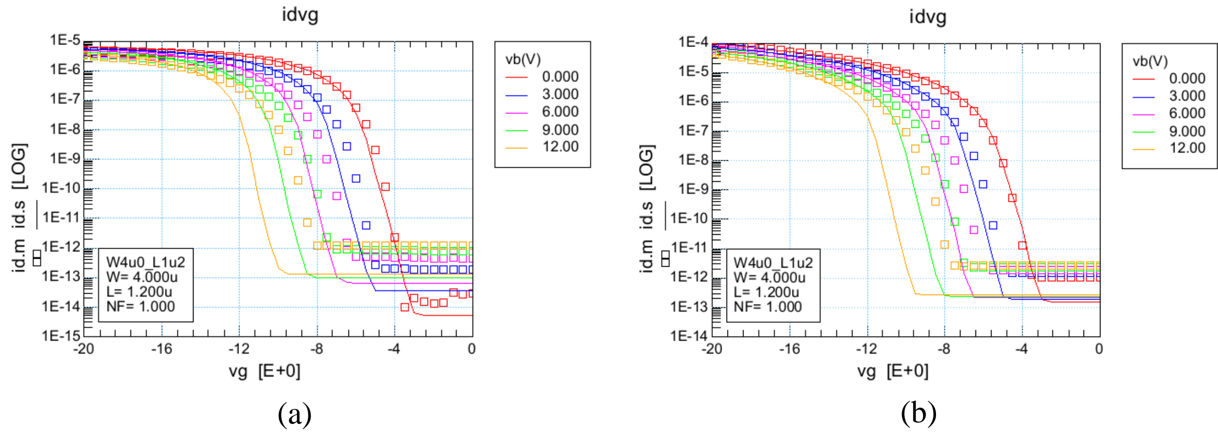


Fig. 5.65. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) PMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

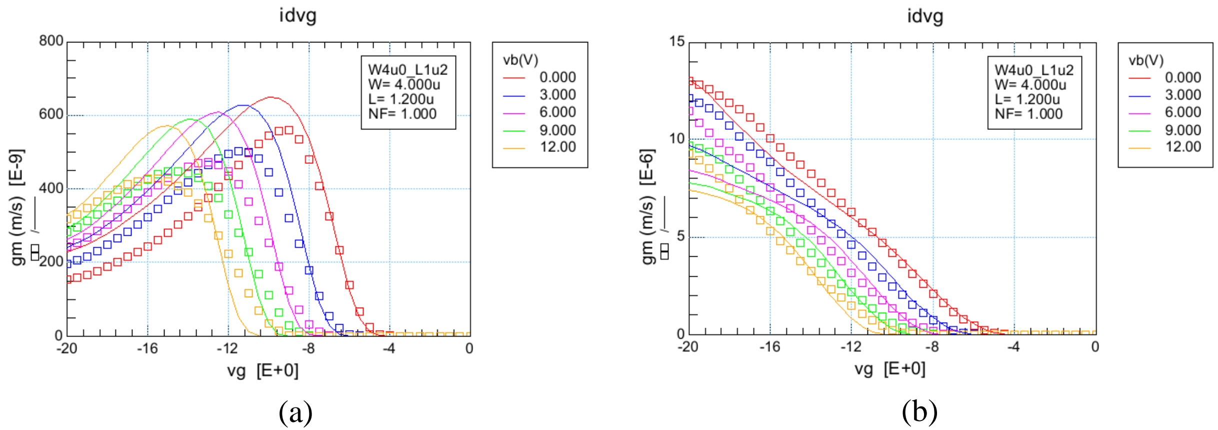


Fig. 5.66. Transconductance of a 4 µm / 1.2 µm (narrow and short) PMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

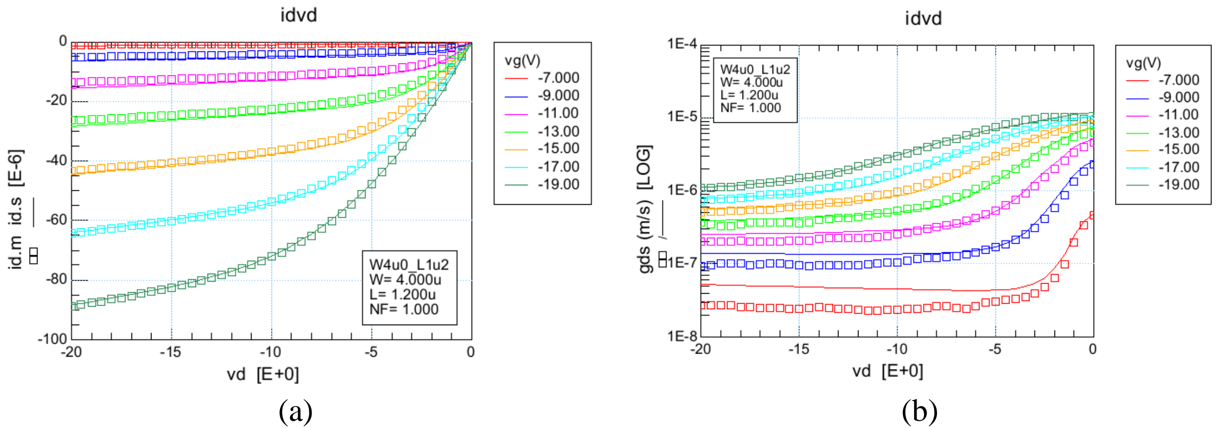
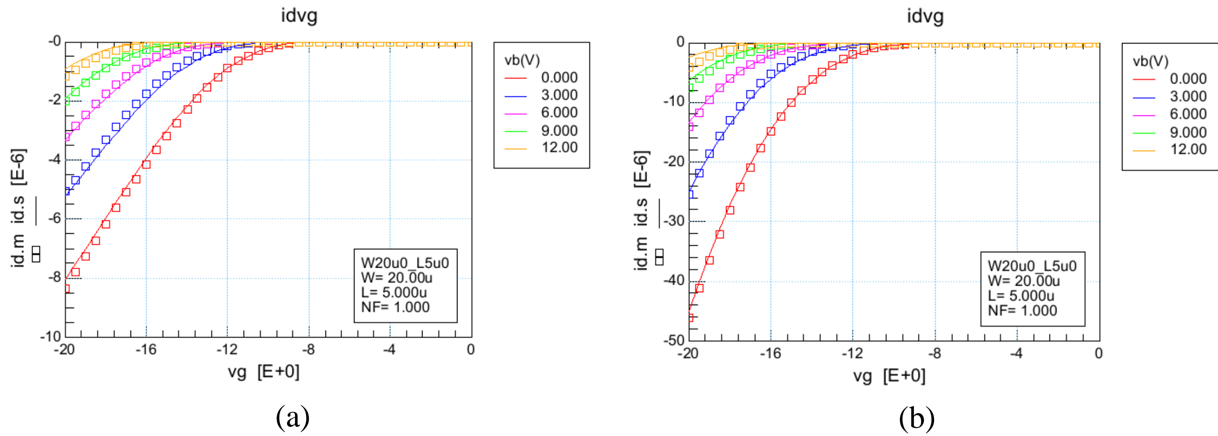
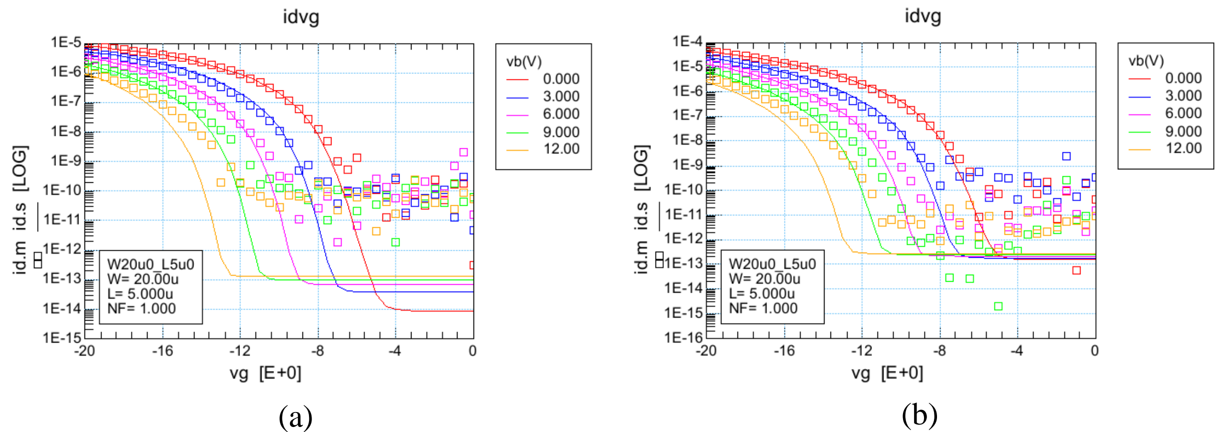


Fig. 5.67. a) Output characteristics and (b) output conductance of a 4 µm / 1.2 µm (narrow and short) PMOS at 25 ° C.



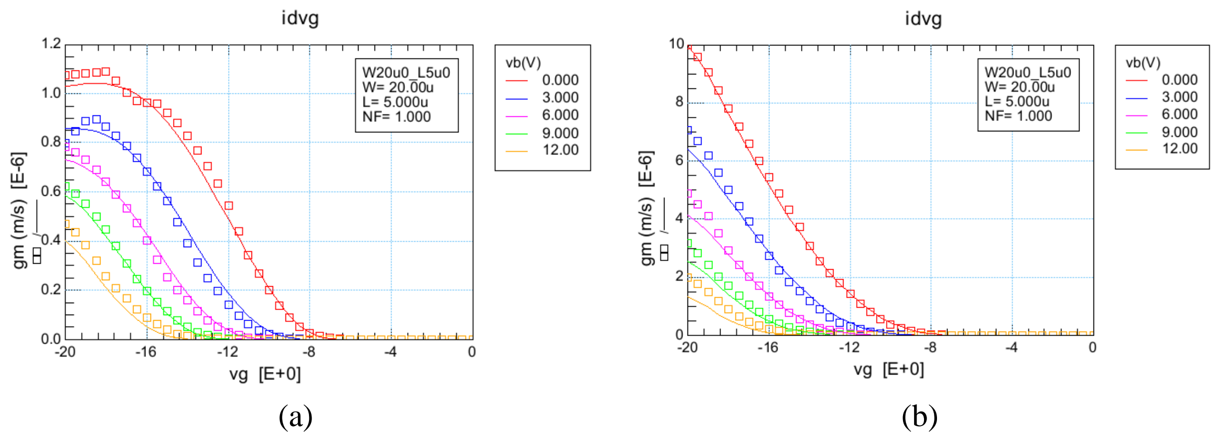
(a) (b)

Fig. 5.68. Transfer characteristics of a 20 µm / 5 µm (wide and long) PMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



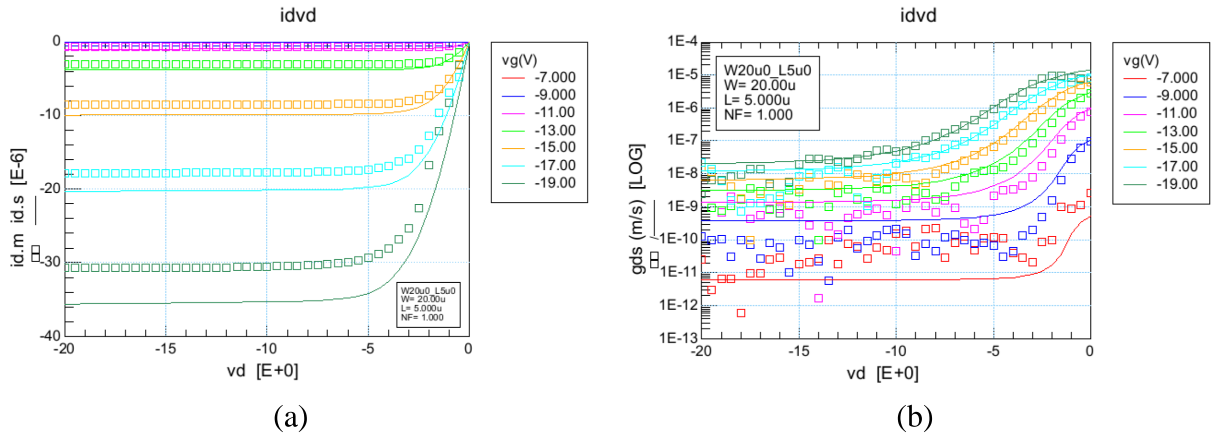
(a) (b)

Fig. 5.69. Transfer characteristics of a 20 µm / 5 µm (wide and long) PMOS at 300 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



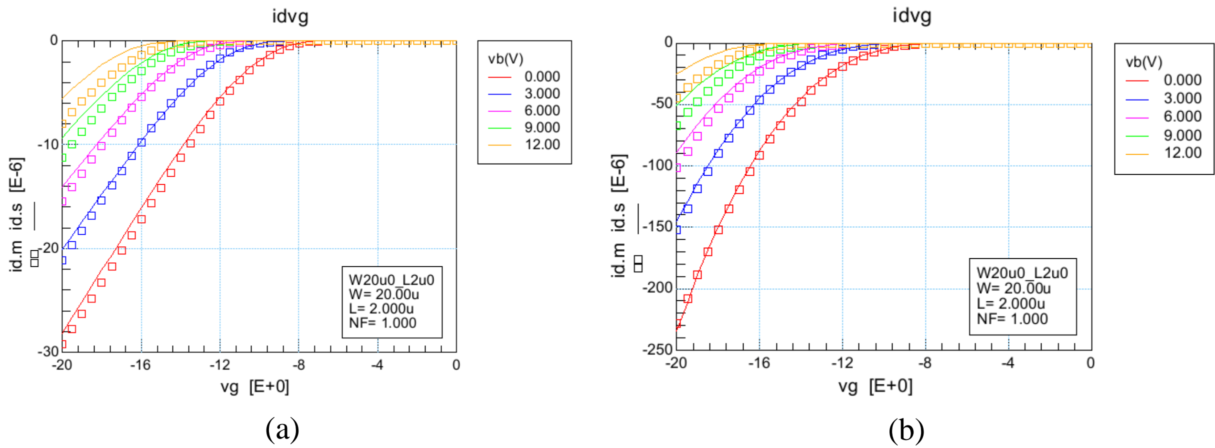
(a) (b)

Fig. 5.70. Transconductance of a 20 µm / 5 µm (wide and long) PMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



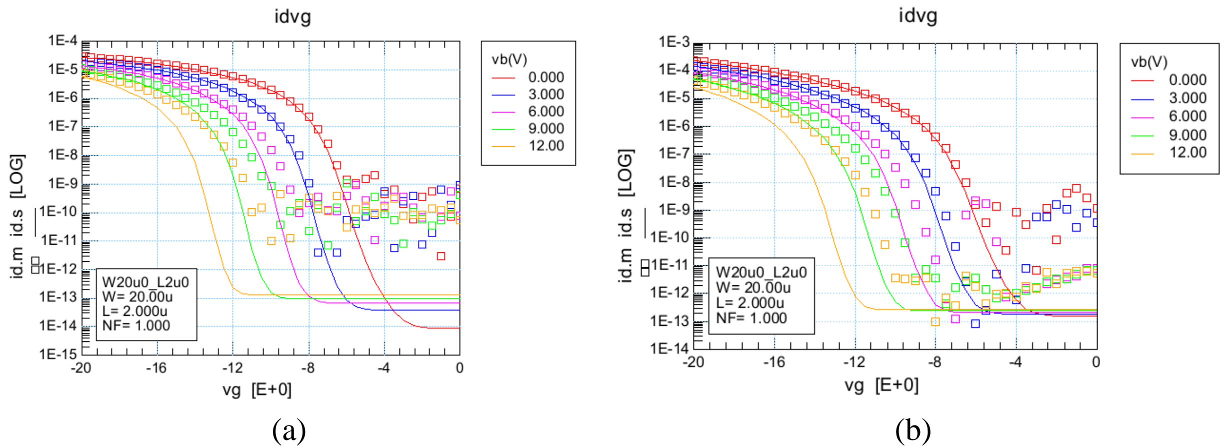
(a) (b)

Fig. 5.71. a) Output characteristics and (b) output conductance of a 20 µm / 5 µm (wide and long) PMOS at 300 ⁰ C.



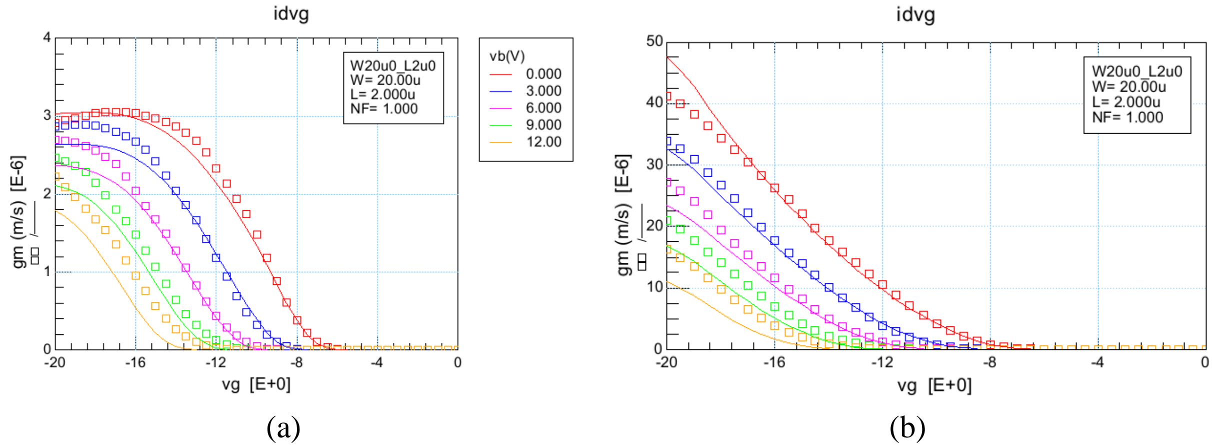
(a) (b)

Figure 5.72. Transfer characteristics of a 20 µm / 2 µm PMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



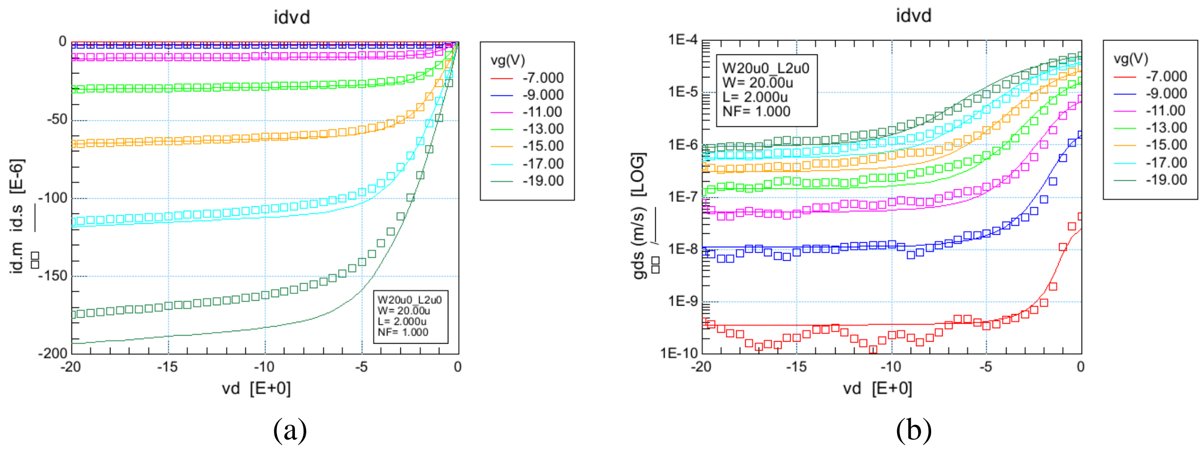
(a) (b)

Fig. 5.73. Transfer characteristics of a 20 µm / 2 µm PMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



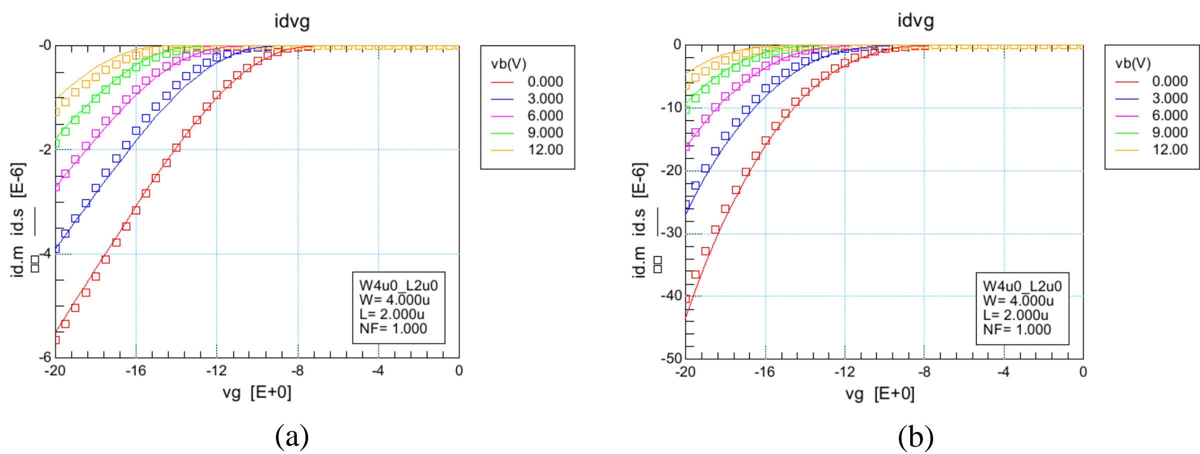
(a) (b)

Fig. 5.74. Transconductance of a 20 μm / 2 μm PMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



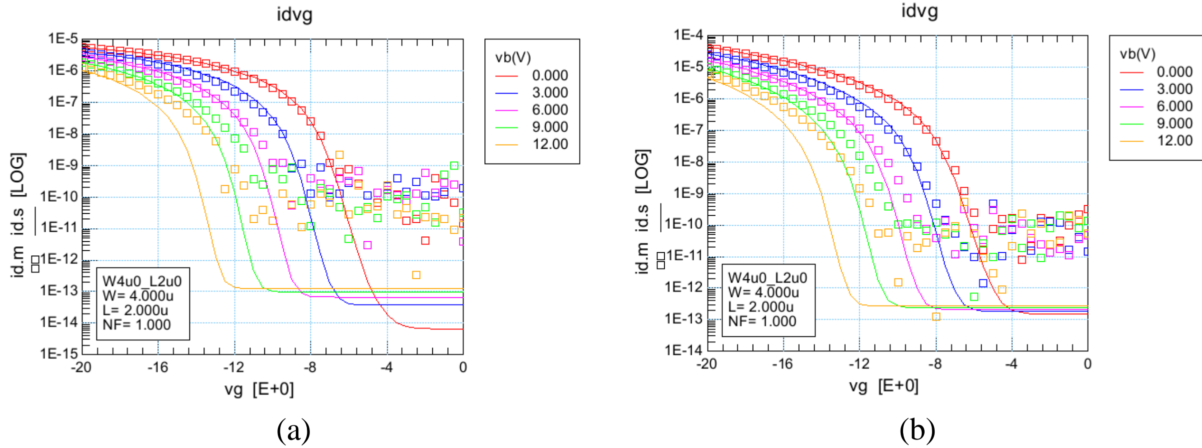
(a) (b)

Fig. 5.75. a) Output characteristics and (b) output conductance of a 20 μm / 2 μm PMOS at 300 ⁰ C.



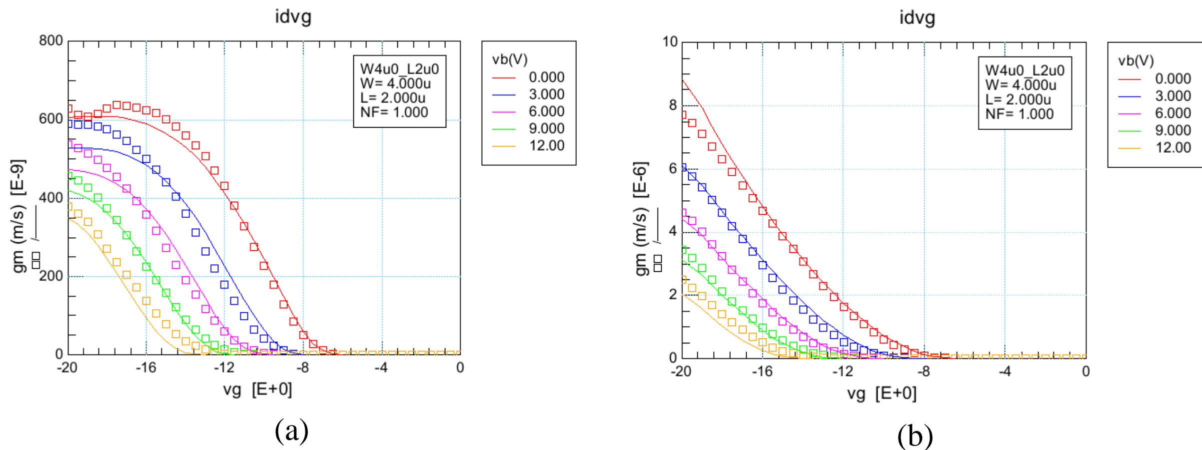
(a) (b)

Fig. 5.76. Transfer characteristics of a 4 μm / 2 μm PMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



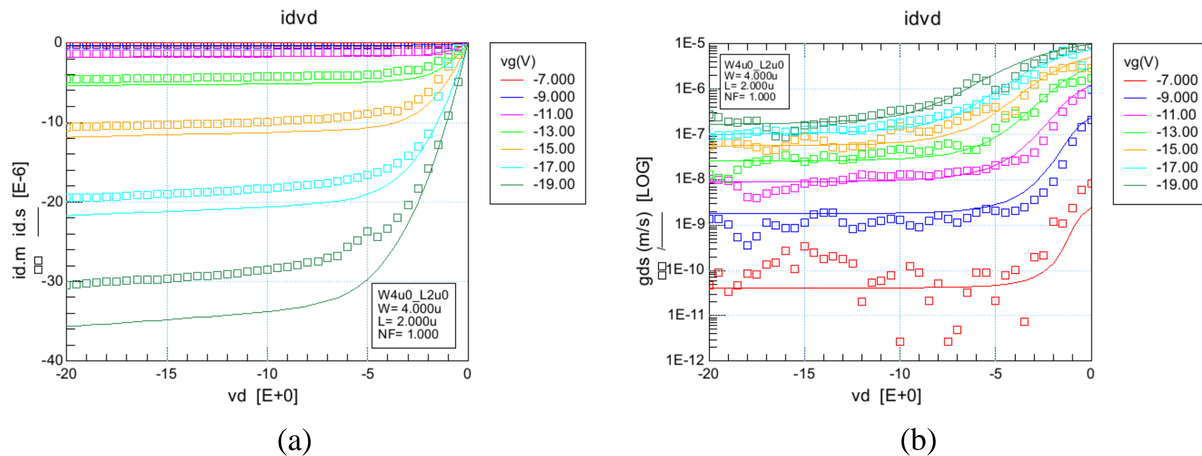
(a) (b)

Fig. 5.77. Transfer characteristics of a 4 µm / 2 µm PMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



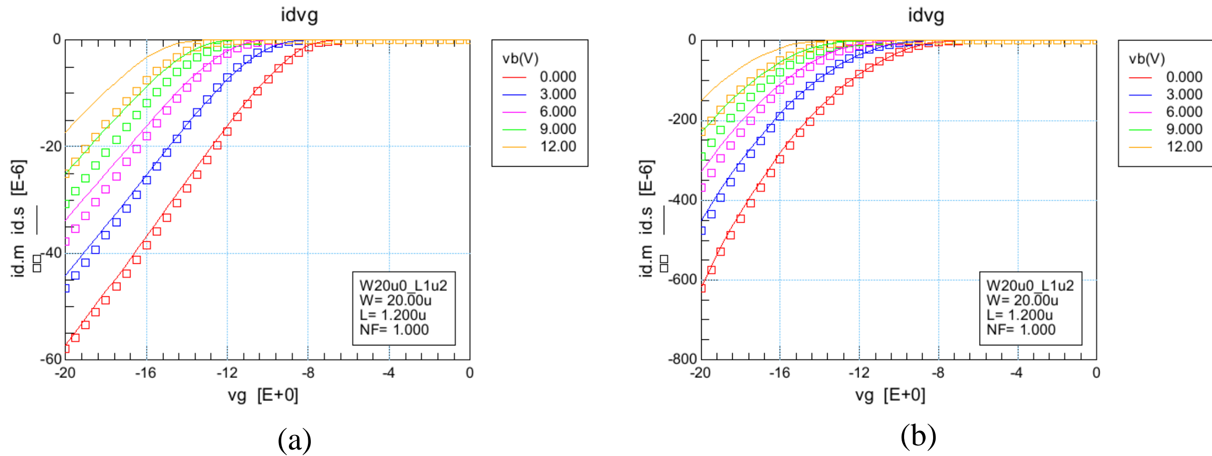
(a) (b)

Fig. 5.78. Transconductance of a 4 µm / 2 µm PMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



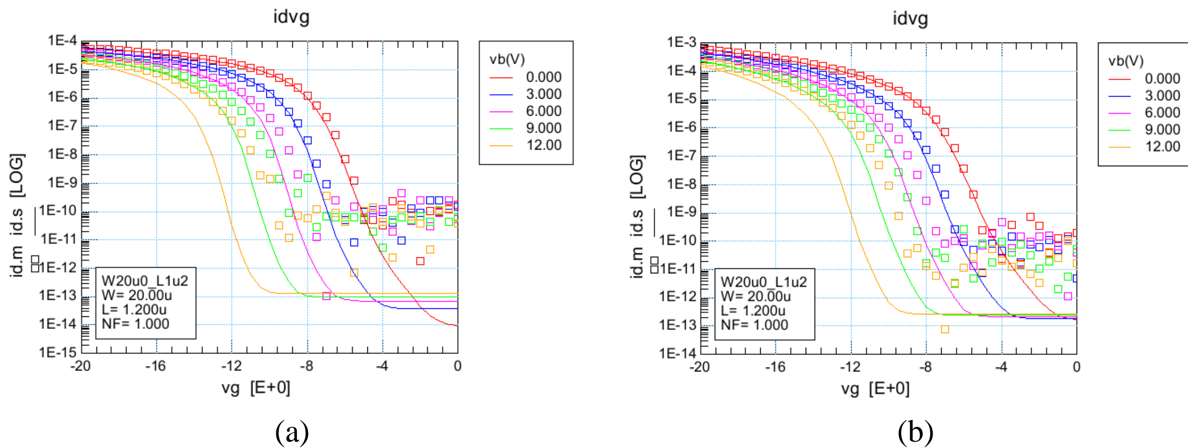
(a) (b)

Fig. 5.79. a) Output characteristics and (b) output conductance of a 4 µm / 2 µm PMOS at 300 ⁰ C.



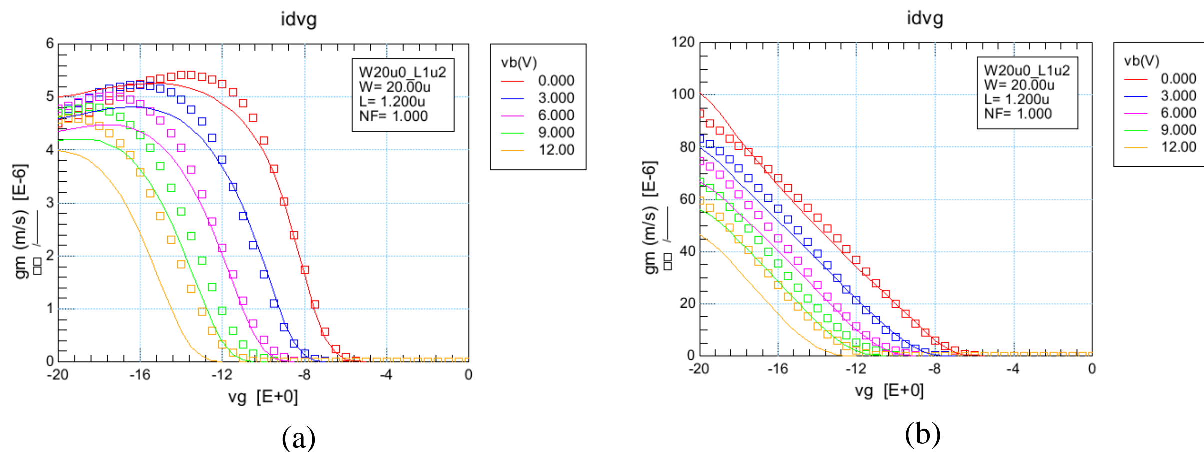
(a) (b)

Fig. 5.80. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) PMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



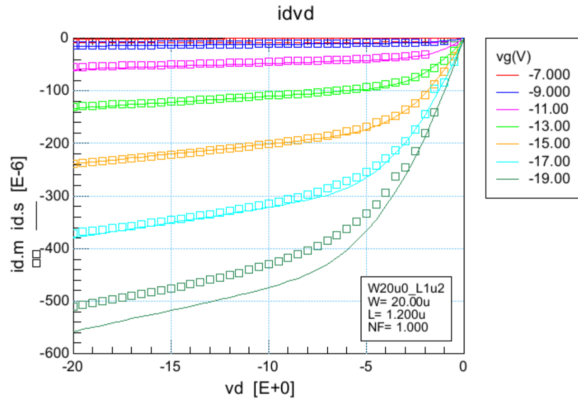
(a) (b)

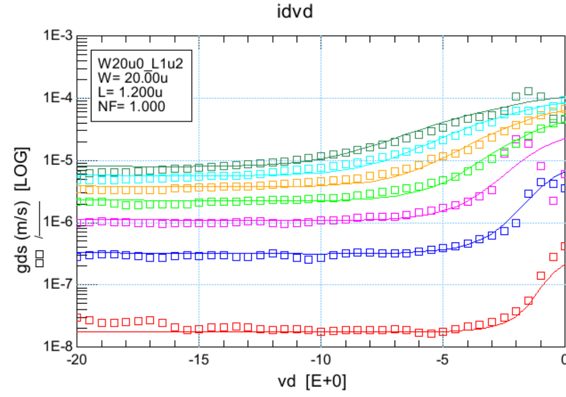
Fig. 5.81. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) PMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

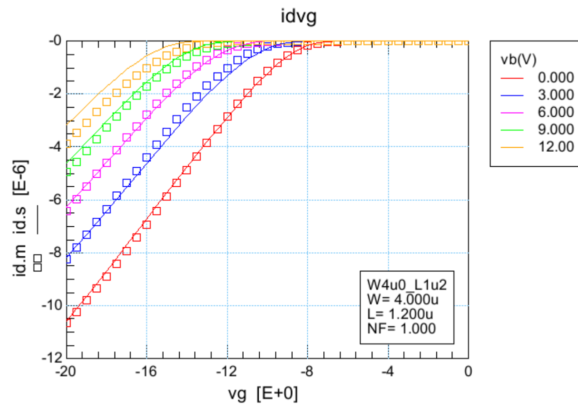
Fig. 5.82. Transconductance of a 20 µm / 1.2 µm (wide and short) PMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

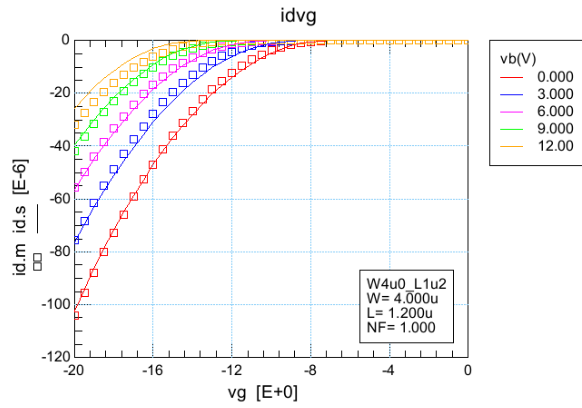




(a) (b)

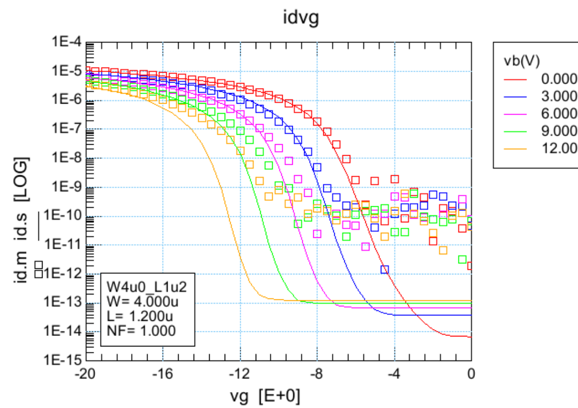
Fig. 5.83. a) Output characteristics and (b) output conductance of a 20 µm / 1.2 µm (wide and short) PMOS at 300 ° C.

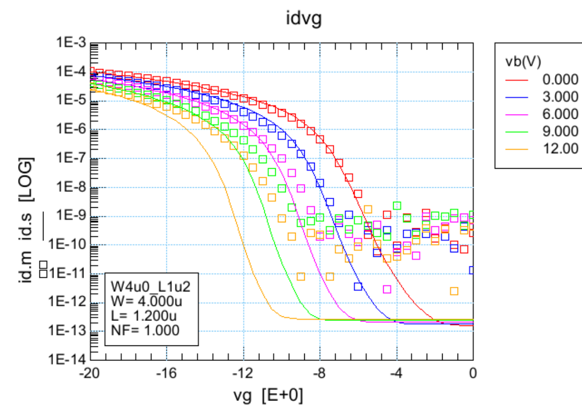




(a) (b)

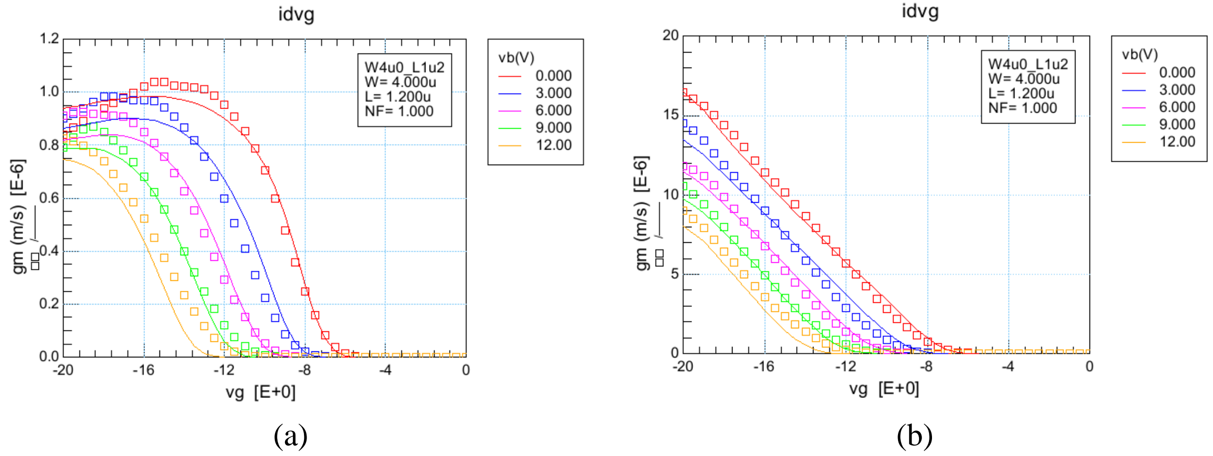
Fig. 5.84. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) PMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.





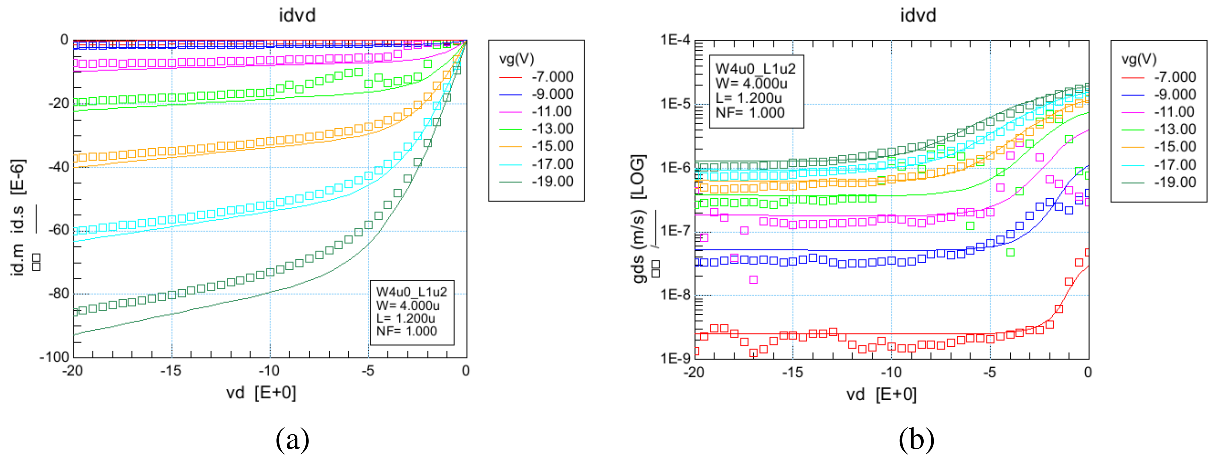
(a) (b)

Fig. 5.85. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) PMOS at 300 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



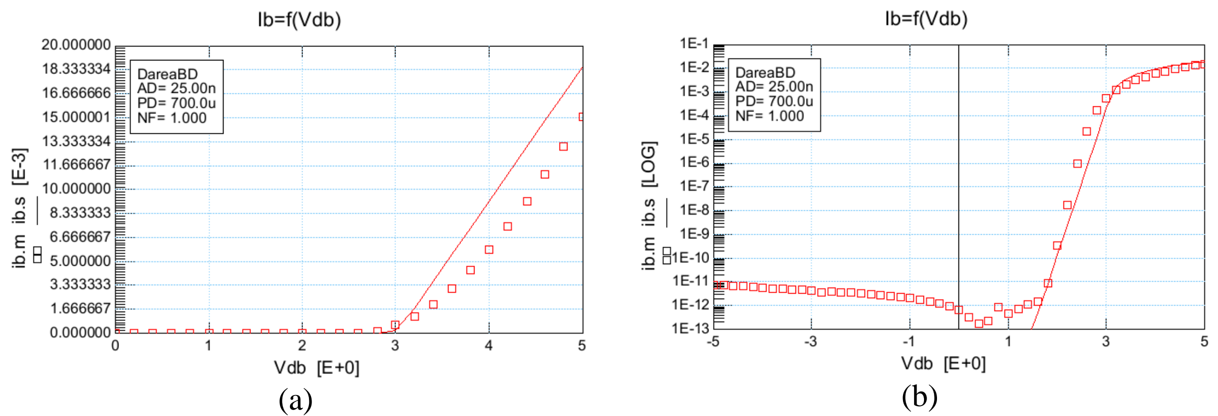
(a) (b)

Fig. 5.86. Transconductance of a 4 μm / 1.2 μm (narrow and short) PMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



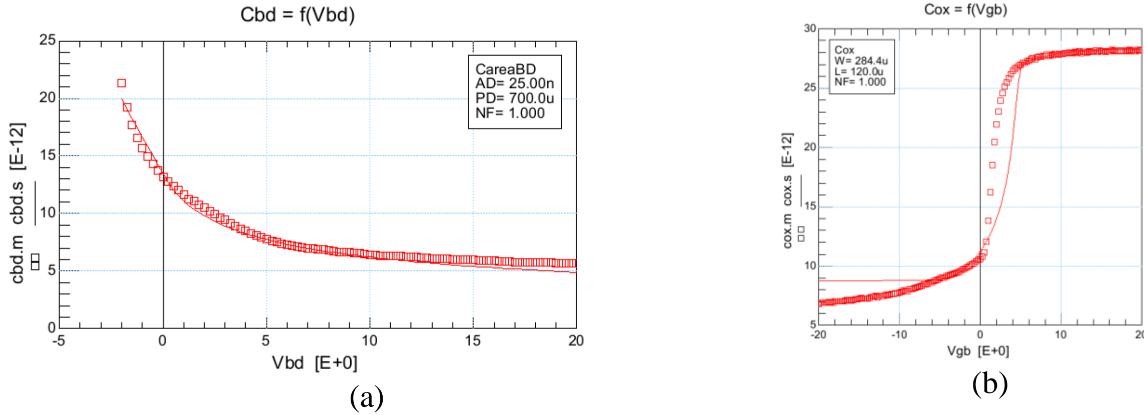
(a) (b)

Fig. 5.87. a) Output characteristics and (b) output conductance of a 4 μm / 1.2 μm (narrow and short) PMOS at 300 ° C.



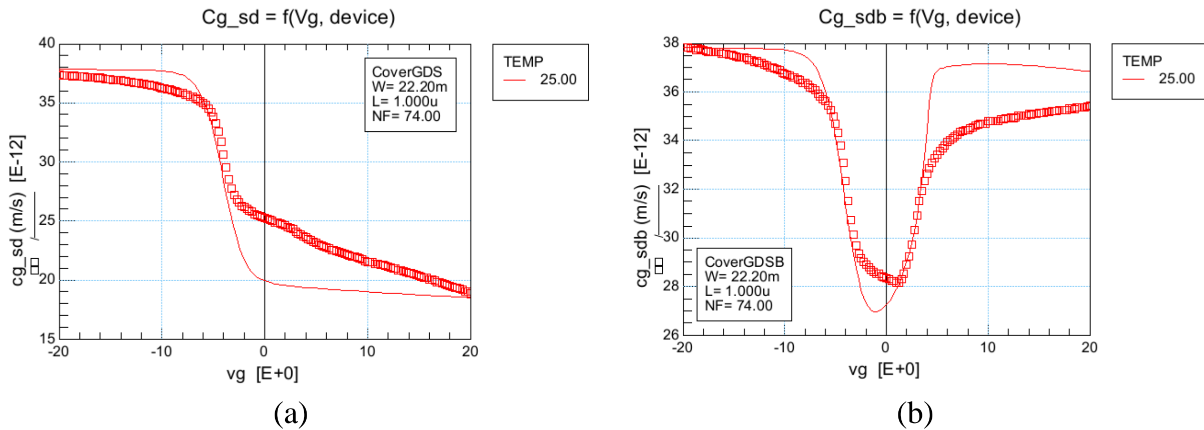
(a) (b)

Fig. 5.88. Drain/source (p+)-to-body (n-well) diode I – V characteristics in (a) linear scale and (b) log scale.



(a) (b)

Fig. 5.89. a) Drain/source (p+)-to-body (n-well) junction diode C – V and (b) PMOS oxide capacitance.



(a) (b)

Fig. 5.90. (a) Gate-to-drain/source overlap and intrinsic capacitance and (b) gate-to-drain/source/body total capacitance of a PMOS.

5.3.3 Limitations of BSIM4 in Modeling SiC MOSFET

The major limitation of BSIM4 is that it cannot model the body effect of the SiC NMOS. Especially if the device is biased in strong inversion, BSIM4 cannot even predict the trend in the drain current when the body terminal is biased with a finite amount of voltage. For the PMOS, although the inversion characteristics in the presence of a body bias can be modeled with reasonable accuracy, the subthreshold characteristics cannot be predicted well. The gate capacitance optimization also is not very accurate. These limitations of BSIM4 prompted the

development of new model equations and their implementation in the Verilog-A code as the major part of this work.

5.4 Circuit Design with BSIM3V3 and BSIM4 Based Models

In tape-out1, basic analog and digital circuits were designed with the BSIM3V3 models. Some of the circuits are voltage and current references [123], standard digital cells [124] and two stage operational amplifier [125]. A phase locked loop was also designed in the first tape-out [126]. In the second tape-out, a wide variety of analog, mixed signal and power integrated circuits were designed using the BSIM4 models. The test results from the circuits are within a few percentage of the simulated results. The notable circuits designed in tape-out2 include comparators [127], a gate driver [128], a linear regulator [129], R-2R DAC [130] and SAR ADC.

5.5 Summary

In this chapter, a detail description of the BSIM3V3 and BSIM4 is provided. The physics based derivation of the MOSFET device charge and current equations used in BSIM3V3 is also outlined. Modeling of the prominent secondary effects such as the threshold voltage shift, short channel effects, parasitic capacitance etc. is also discussed. The enhancements added in BSIM4 to take into account the effects of non-silicon substrate and non-SiO_2 gate dielectric are demonstrated. The optimization results of SiC MOSFET DC and C-V characteristics using BSIM3V3 and BSIM4 are presented and the limitations of the models are identified.

CHAPTER 6 EFFECTS OF INTERFACE TRAPS ON SIC MOS DEVICES

6.1 Origin of the interface states in SiC MOSFET

The Si/SiO_2 interface in a Si MOSFET is almost defect free because SiO_2 is a native oxide of Si. Moreover the lattice mismatch between Si and SiO_2 crystals is minimal and does not create significant cracks or broken bonds due to excessive stress or strain [131]. Also, decades of research have resulted in numerous innovative passivation techniques to reduce the post annealing defects generated by the dangling bonds in the Si/SiO_2 interface. Unfortunately, the interface between SiC and SiO_2 in a SiC MOSFET is not of highest quality due to three primary reasons – 1) sp^2-bonded carbon clusters or precipitates, 2) near interface traps and 3) dangling bonds [132]. A thin layer of carbon atoms are formed at the interface during the growth of SiO_2 on SiC by thermal oxidation [133]. This cluster of carbon atoms which bear resemblance to graphite gives rise to a high density of allowed energy states in the bottom half of the SiC bandgap. The sharp increase in the energy states near the SiC conduction band is a result of the excess Si atoms in the oxide close to the interface. The Si atoms diffuse in the oxide due to the stress generated by the lattice mismatch between SiC and SiO_2 crystal structures and form an intermediate layer of Si-Si bonds [134]. The energy states generated by the Si-Si bonds are called the near interface traps (NIT) and have been experimentally observed in the thermally oxidized SiC polytypes [135]. Although the presence of NITs in 6H- and 15R- polytypes are not detrimental, the trap sites are responsible for many performance degradations of 4H-SiC MOSFET device. The valence bands of SiC polytypes and SiO_2 are energetically aligned and the location of the NITs is above the conduction bands of 6H- and 15R- SiC polytypes. As a result, the electrons from the conduction bands cannot move to the trap states. But 4H-SiC has higher bandgap and the NITs are within the energy gap of the polytype as illustrated in Fig. 6.1 and thus the conduction electrons can migrate to the sites and get trapped.

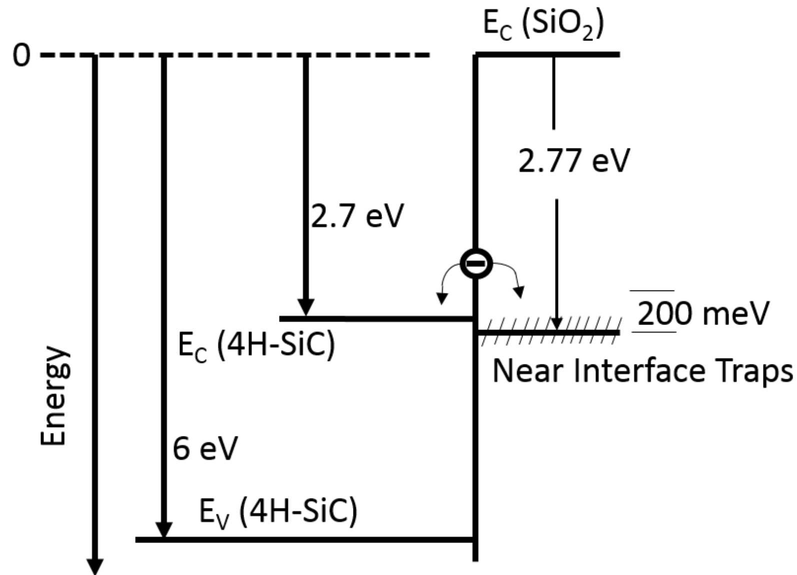


Fig. 6.1. Illustration of near interface trap sites in an n-type SiC MOS structure [132].

The NIT energy states are located in the oxide about 15Å to 20Å away from the interface. The occupation of some conduction electrons by the NITs reduce current, degrade mobility and decrease the speed of a 4H-SiC MOSFET. The dangling bonds are generated from the damage created by the ion implantation process and create energy states within the SiC bandgap. Although the hydrogen annealing technique can be successfully used to repair the damage from ion bombardment in a Si MOSFET, the technique does not significantly passivate the dangling bonds in the SiC/SiO_2 interface. The interface state density (D_{it}) in a Si MOSFET is approximately 2-10×10^{10} /eV·cm^2 [136] and the trap density in a SiC MOSFET is at least two orders of magnitude greater than that of Si.

D_{it} can be extracted from a DC measurement using the sub-threshold characteristics or from a C-V measurement by comparing the ideal and experimental capacitance profile. Deng et al. [137] has demonstrated a method of extracting the D_{it} profile of 4H- and 6H-SiC MOSFETs annealed in dry O_2, NO and CO_2 from the subthreshold slope of the device. An improved D_{it} extraction

technique using the rising edge of the gate-channel capacitance from the low frequency C-V characteristics is described in [138]. More D_{it} extraction techniques can be found in [139].

6.2 Effects of the interface trapped charge on 4H-SiC MOSFET Characteristics

The effects of the interface states in a MOSFET device is best described by the concept of an energy band diagram. The bending of the energy states when the device operates in accumulation is shown in Fig. 6.2(a). When the gate voltage is negative in an n-type MOSFET, the negative charge on the gate electrode attracts positive holes on the oxide-semiconductor interface and the substrate becomes more positive at the interface than it is in the bulk. Thus, the Fermi level (a hypothetical energy level in a material ideally below which the probability of finding an electron is one and above which the probability is zero at absolute zero temperature) moves closer to the valence band at the interface and the valence band and conduction band bend downward. The depletion region is achieved in an NMOS when the gate voltage is greater than the flat band voltage and in this region the positive charge on the gate pushes away the majority carrier holes from the interface to the p-type substrate. The depleted acceptor ions become negatively charged and turn the substrate more negative at the interface than it is deep in the bulk. This can only happen when the Fermi level is further away from the valence band at the interface than it is in the substrate and thus results into the upward bending of the valence and conduction bands. The band diagram of the n-type MOS device in depletion is shown in Fig. 6.2(b). When the NMOS operates in the inversion region, a large positive gate voltage attracts electrons at the oxide semiconductor interface and the p-type substrate acts as an n-type semiconductor at the interface. As a result, the Fermi level is closer to the conduction band at the interface than it is in the substrate and this can be caused by the large upward bending of the valence and conduction bands as shown in Fig. 6.2(c).

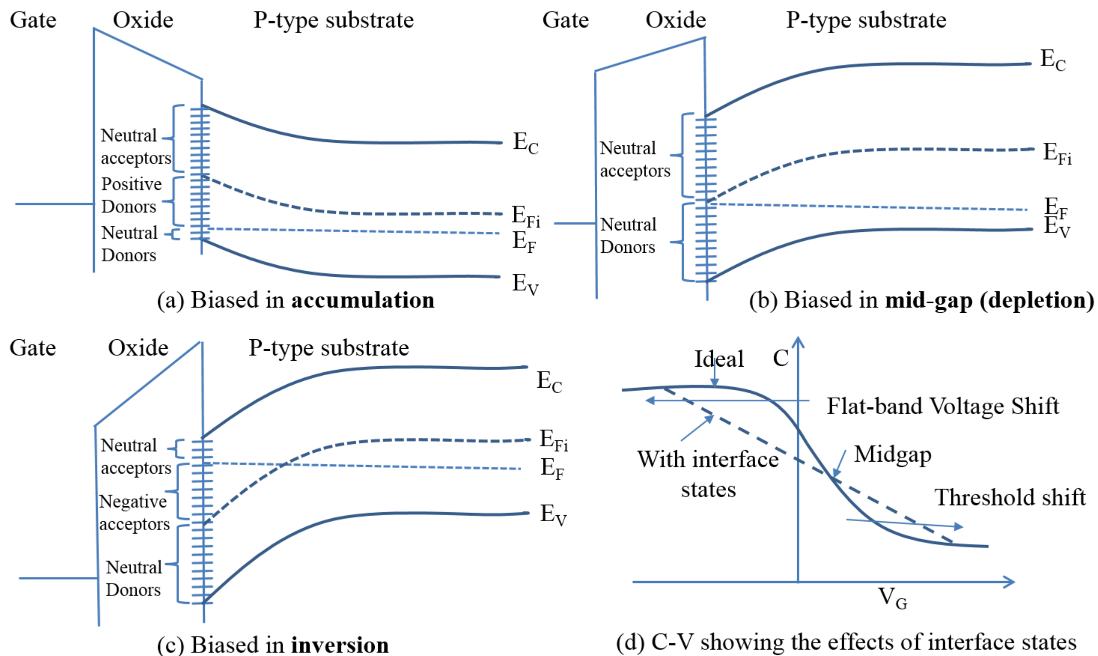


Fig. 6.2. Energy band diagram including the distribution of interface states of a MOS cap drawn along perpendicular direction of the oxide-semiconductor interface; (a) in accumulation, (b) in depletion, (c) in inversion and (d) the smeared C – V curve in presence of interface trapped charge [140].

Generally, the upper half of the bandgap is occupied by the acceptor states and the bottom half is occupied by the donor states. Acceptor states can accept electrons or donate holes and become negatively charged. The donor states, on the other hand can donate electrons or accept holes and become positively charged. Ideally as previously mentioned, the probability of an electron residing in an energy state is zero if the state is above the Fermi level and one if the state is below the Fermi level. This is why an acceptor state is neutral if the Fermi level is below the state and contains negative charge if the Fermi level is above the energy state. The opposite is true for the donor states. When the device is in accumulation, since some of the donor states are above the Fermi level, those states will become positively charged. This is indicated in Fig. 6.2(a). The positive charges contributed by the donor states add up to the accumulated holes and thus in order to make the band flat or make the p-type substrate space charge free, more negative charges are

needed at the gate. The flat band voltage (the voltage needed to make the band flat) shifts left which is shown in Fig. 6.2(d). When the device enters the inversion region, the Fermi level moves into the upper half of the bandgap and the acceptor states below the Fermi level are occupied by the inversion electrons and become negatively charged as demonstrated in Fig. 6.2(c). In order to make the same inversion level as it is without the presence of interface states, more positive voltage is required at the gate. Thus, the threshold voltage increases in an NMOS when there is a significant amount of interface states in the interface as indicated in Fig. 6.2(d). In summary, the interface states get occupied and de-occupied by the charge carriers and become negatively or positively charged depending on the position of the Fermi energy level which moves upward or downward in the bandgap with respect to the applied gate bias. Hence, the trapped charge affects the operation in sub-threshold, strong inversion, linear and saturation region as well as alters the C-V behavior of the MOS device. Also, as the temperature increases, the probability of the states being trapped decreases and makes the effects of interface states on the device characteristics less prominent at higher temperature. In subsequent sections, the extent of the interface trapped charge effects on major device characteristics such as subthreshold slope, threshold voltage, mobility etc. is discussed.

6.2.1 Mobility Reduction

The parameter which suffers the most from the poor oxide-semiconductor interface is the mobility. The bulk mobility of SiC material and the channel mobility of a SiC MOSFET should be compared as a measure of the detrimental effects of interface trapped charge on the mobility. From Table 2.1, it is found that the bulk mobility of 4H-SiC MOSFET is 800 cm^2/V-s. Fiorenza et al. [141] have reported a 4H-SiC lateral MOSFET with 108 cm^2/V-s of channel mobility but the fabrication procedure requires an innovative oxidation and annealing process. Thomas et al. [142]

demonstrated only 40 cm^2/V-s channel mobility using a novel 1500 ^{o} C gate oxidation process. Chung et al. [143] have used a high temperature annealing technique in nitric oxide and reported 30-35 cm^2/V-s channel mobility. Although the mobility of an n-channel lateral SiC MOSFET is in the range of 30 to 50 cm^2/V-s, the mobility of the p-channel device is only about 10 cm^2/V-s. The ideal mobility in PMOS is less than that of NMOS due to the higher effective mass of holes. In addition, the quality of the SiC PMOS oxide-semiconductor interface is worse compared to the interface of an NMOS device.

Mobility can be extracted from the measured transfer characteristics of a MOSFET device. When the device operates in strong inversion and linear (or triode) region, the drain current of an NMOS can be expressed as follows [144]:

$$\boldsymbol{I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]} \quad \textbf{6.1}$$

where $\mu_n$is the channel mobility and assumed to be constant, $C_{ox}$is the oxide capacitance per unit area, W and L are channel width and length respectively, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage and $V_{TH}$is the threshold voltage. If Eq. 6.2 is differentiated with respect to V_{GS} (which gives the transconductance g_m), for a sufficiently small V_{DS}, the mobility $\mu_n$can be written as:

$$\boldsymbol{\mu_n = \frac{g_m}{C_{ox}\frac{W}{L}V_{DS}}} \quad \textbf{6.2}$$

Eq. 6.3 can also be applied for the mobility extraction of a PMOS. The mobility of Raytheon HiTSiC PMOS and NMOS are plotted in Fig. 6.3. The mobility was extracted from the maximum transconductance and thus indicate the highest low lateral field mobility. The primary

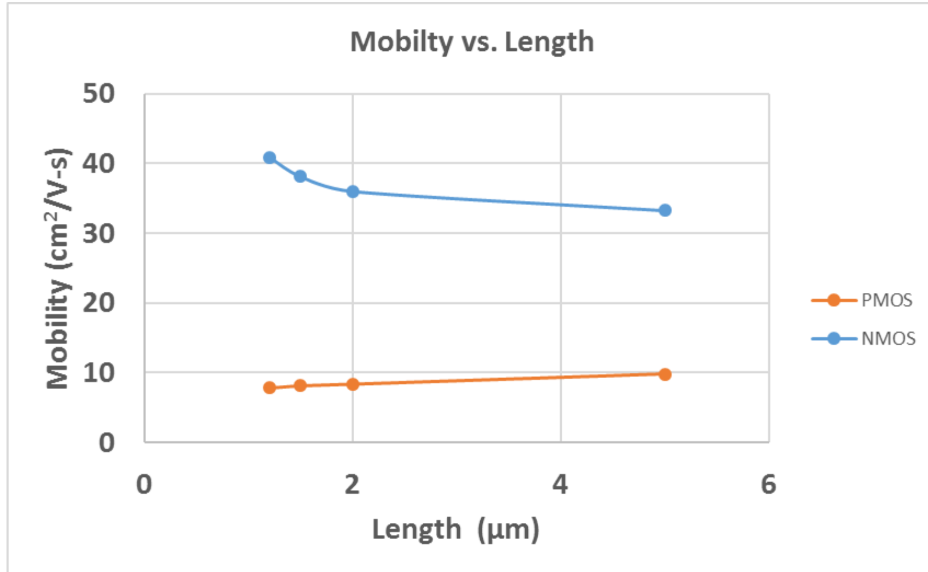


Fig. 6.3. Mobility of SiC MOSFETs for different channel lengths at 25 ° C. Width is 20 μm.

reason for the drastic mobility reduction due to interface trapped charge is the coulomb scattering [145]. At the onset of inversion, the electrons get trapped by the acceptor states located in the upper half of the bandgap at the interface and act as scattering centers. The mobility reduction from coulomb scattering is more dominant at low vertical field and low temperature [146]. Other mechanism that contributes to the reduction of channel mobility is the surface roughness [147].

6.2.2 Subthreshold Slope Reduction

The subthreshold slope of a MOSFET device is a measure of the current increase with respect to the gate-to-source voltage in the weak inversion region when the device turns on. The MOSFET drain current during the turn-on follows an exponential relationship as demonstrated in section **Error! Reference source not found.** and from the relationship the subthreshold slope *SS* can be expressed as:

$$SS = ln(10) \cdot n \cdot \phi_t \tag{6.3}$$

where ϕ_t is the thermal voltage and n is the subthreshold swing factor as shown in Eq. 5.22. The minimum value of n according to Eq. 5.22 is one and as such the ideal minimum subthreshold slope is 60 mV/decade at room temperature. If a MOSFET device has higher subthreshold slope, the device will have greater subthreshold leakage current and a larger threshold voltage and thus dissipates more power in digital circuits and provides less voltage swing in analog circuits. As a result, a smaller subthreshold slope is of paramount importance for a MOSFET.

Unfortunately, the interface trapped charge degrade the MOSFET subthreshold characteristics significantly [148]. Since the acceptor states occupy some of the inversion electrons during the turn-on of the device, a larger gate-to-source voltage increment is required to achieve the similar increase in the drain current that could be achieved without the presence of interface states. Since SiC is a wide bandgap material, the subthreshold leakage is not a big concern but the threshold voltage is higher especially for the PMOS device. The subthreshold slopes (SS) of a 20/1.2 NMOS and PMOS from Raytheon HiTSiC process are plotted in Fig. 6.4. It is found that the SS of SiC MOSFET (253.4 mV/decade for NMOS and 269.7 mV/decade for PMOS) is significantly higher than that of Si MOSFET (lower than 100 mV/decade).

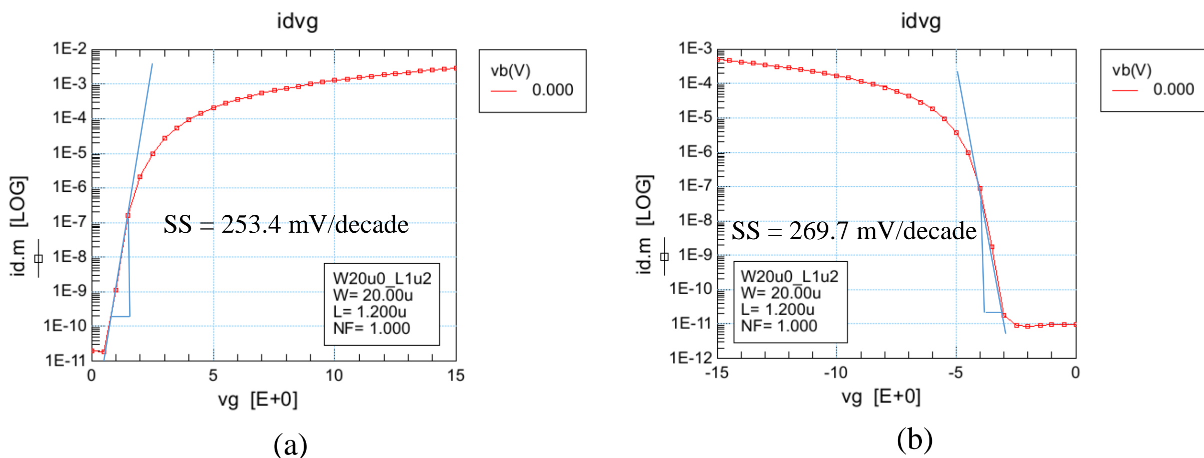


Fig. 6.4. Subthreshold slope of SiC MOSFET; (a) NMOS and (b) PMOS

6.2.3 Body Effect Alteration

As demonstrated in Eq. 5.14, the main body effect in a MOSFET device is the increase in the threshold voltage. Qualitatively the effect of applying a voltage between the source and body

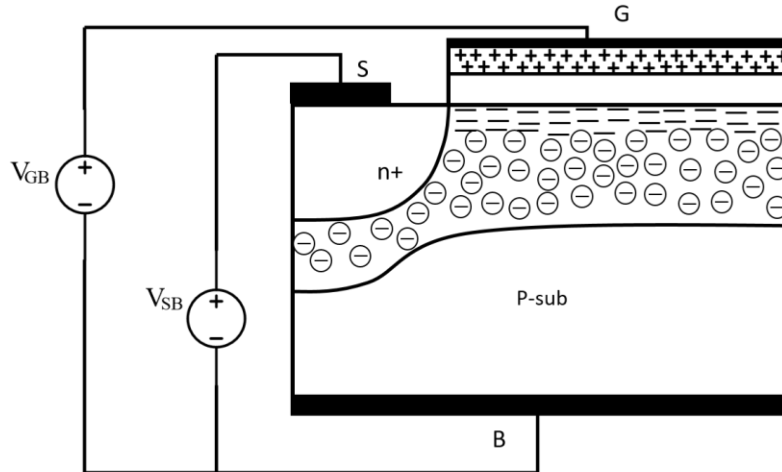


Fig. 6.5. Illustration of body effect when the gate and the source terminals are biased with respect to the body terminal in a hypothetical three terminal MOS structure.

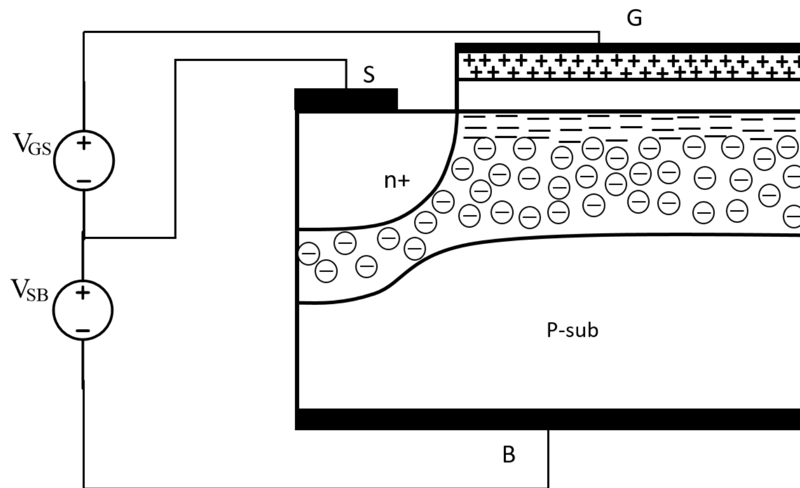


Fig. 6.6. Illustration of body effect when the gate and the body terminals are biased with respect to the source terminal in a hypothetical three terminal MOS structure.

terminals can be explained with the help of Fig. 6.5 and Fig. 6.6 [113]. In Fig. 6.5, voltage is applied at the gate and the source with respect to body terminal in an n-channel MOSFET. First,

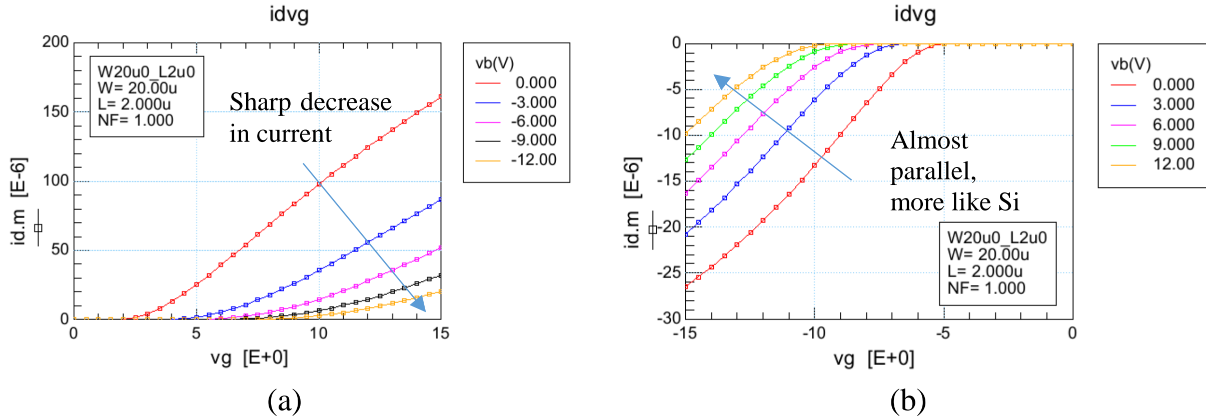
it is assumed that the device is in strong inversion and the voltage across the gate and the body V_{GB} is held constant which makes the surface potential fixed. Now if the voltage between the source and the body V_{SB} is increased, the potential in the n+ source region will become more positive compared to the surface potential. So some of the inversion electrons will be attracted by the source region and eventually will flow to the positive terminal of the V_{SB} voltage source. This results a decrease in the inversion level and with a sufficient increase in V_{SB} the channel might be devoid of all the inversion electrons. The only way to achieve the similar level of inversion as it was with no voltage across the source and body is to increase the V_{GB}. In other words, the gate and the body terminals have competing role against each other. A positive voltage at the gate in an NMOS tends to increase the inversion level and a positive voltage at the body decreases the inversion level. The body terminal is sometimes also called the back gate for this reason.

The body effect can also be intuitively explained when the voltage is applied at the gate and the body with respect to the source terminal as shown in Fig. 6.6. Again, it is assumed that the voltage at the gate is large enough to bring the device in strong inversion. The difference between Fig. 6.5 and Fig. 6.6 is that the gate-to-body voltage is fixed in the former and the gate-to-source voltage is kept constant in the latter. In the strong inversion, the oxide and the substrate are isolated by the inversion charge layer and can be thought of as a series combination of a parallel plate capacitor and a junction capacitor. The junction formed by the inversion electron and p-type substrate is known as the field induced n^+p junction and the voltage V_{SB} acts as reverse bias across the junction. When V_{SB} is increased the depletion region in the p-sub under the strongly inverted channel will widen. Although increasing V_{SB} will increase V_{GB}, V_{GS} will remain constant under the assumption of strong inversion which can be guaranteed by keeping the change in V_{SB} small. A constant V_{GS} ensures a fixed voltage across the gate oxide and thus the total charge on the gate

electrode will remain unchanged. But the wider depletion region in the substrate due to higher V_{SB} will contribute more negative charge to the channel charge and to balance the charge at the top and the bottom of the oxide fewer inversion electrons will be required. Thus, some of the free electrons from the channel will flow to the V_{SB} and the inversion level will decrease. If the inversion layer is intended back to the previous level, the voltage V_{GS} needs to be increased. The body effect is more pronounced in a MOS device with higher substrate doping concentration and thicker gate oxide because higher doping contributes to more depletion charge density and thicker oxide results in less influence of the gate terminal on the channel charge. The effects of substrate doping and gate oxide thickness are quantified in Eq. 5.11 through the body effect coefficient γ.

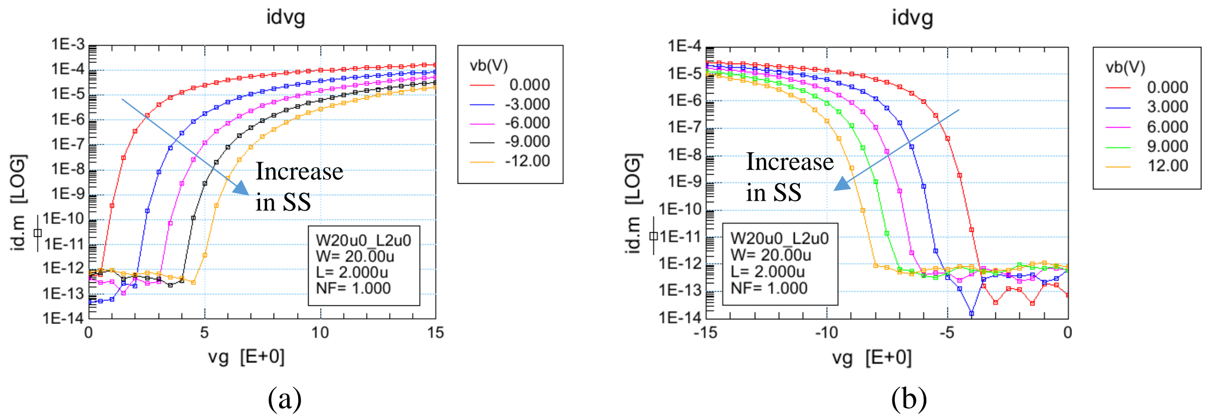
The discussion on the body effect indicates that a higher gate voltage is required to turn on the device when the voltage at the source terminal is higher than the voltage at the body terminal. In a silicon MOSFET, the $I_d - V_g$ curves moves right along the voltage axis as V_{SB} is increased and remain parallel to one another. The body effects in such case can be modeled by an increase in the threshold voltage as shown in Eq. 5.14. Unfortunately, in a SiC MOSFET where interface states are abundant and surface is rough, the body effect is not merely a threshold voltage shift.

In SiC devices, the body effect tends to alter the sub-threshold slope as well as the low field mobility. The transfer characteristics of SiC MOSFETs demonstrating strong inversion and subthreshold for different body biases are plotted in Fig. 6.7 and Fig. 6.8 respectively. If a negative voltage is applied at p-body, it tends to push the mobile carriers closer to the interface, so the carriers now experience more scattering from coulomb attraction and surface roughness. At low gate bias, when the number of inversion charges are low, coulomb scattering dominates. At high gate bias, when the number of inversion charge is significant, the trapped charges are screened out



(a) (b)

Fig. 6.7. Transfer charteristics in strong inversion of SiC (a) NMOS and (b) PMOS.



(a) (b)

Fig. 6.8. Transfer charteristics in subthreshold of SiC (a) NMOS and (b) PMOS.

and the reduction in mobility is primarily caused by the surface roughness. The mobility reduction in presence of body bias is more detrimental in NMOS than in PMOS as evident in Fig. 6.7(a) for NMOS compared to that in Fig. 6.7(b) for PMOS. Mobility reduction translates into less current as more body and gate bias are applied. In NMOS, the p-well is doped by an Aluminum implantation and in PMOS the n-well is doped by a Nitrogen implantation. Al being heavier than N causes more damage at the NMOS surface which results into more surface roughness. Thus, reduction in mobility at higher body bias is more severe in NMOS.

6.3 Effects on CV Characteristics

Apart from the fact that the C-V curve smears due to the presence of interface states as demonstrated in Fig. 6.2(d), the slow and fast trap sites also make the device capacitance frequency

dependent [149]. The equivalent MOSFET gate capacitance in presence of interface trapped charge is shown in Fig. 6.9. When an incremental voltage is applied at the gate, the change in the voltage is distributed between the voltage across the oxide and the surface potential. The semiconductor charge which consists of bulk depletion charge and inversion layer charge and the interface trapped charge only respond to a change in the surface potential. Thus, the gate capacitance can be expressed as the series combination of oxide capacitance C_{ox} and equivalent parallel combination of semiconductor capacitance C_s and interface capacitance C_{it}. If C_{it} increases or decreases, so does the total gate capacitance.

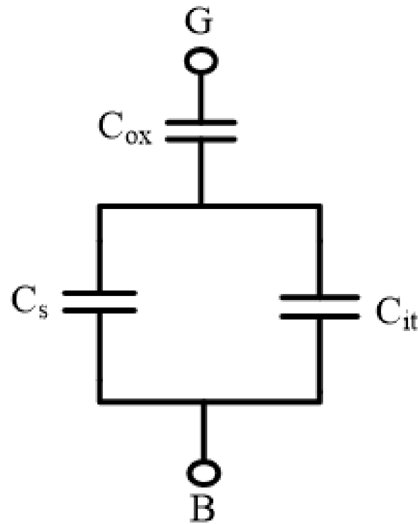


Fig. 6.9. Equivalent circuit representation of the gate capacitance of a MOSFET device in presence of interface trapped charge.

In Fig. 6.10, it is found that, as the frequency increases, capacitance of an NMOS in accumulation region decreases. Also, the curve moves downward when the frequency exceed 300 kHz. When the device moves from accumulation to depletion region, the Fermi level moves upward from the valence band to the conduction band and the donor states become gradually filled with electrons. These donor states which are created by the graphite-like carbon cluster are generally slow. The states cannot respond to the fast varying ac signal if the frequency is too high.

The interface capacitance C_{it} being the change in the interface trapped charge with respect to the change in surface potential thus decreases at higher frequencies. Hence the total gate capacitance ($C_{g\text{-}dsb}$) in accumulation decreases when the measurement frequency is increased. In strong inversion, the Fermi level is very close to the conduction band and the negatively charged acceptor states that are very few in number compared to the large number of inversion electrons. So the change in interface trapped charge with respect to the surface potential is insignificant compared to the change in the inversion charge. Besides, the acceptor states which are created by the near interface traps (NIT) are relatively fast trap sites. Consequently, the total gate capacitance in inversion does not change much until a certain measurement frequency. The downward shift of the curve at high frequencies is a result of the measurement limitations. At higher frequencies, the parasitic cable inductances become significant and thus a minor calibration error and mismatch in wire length affect the measured capacitance.

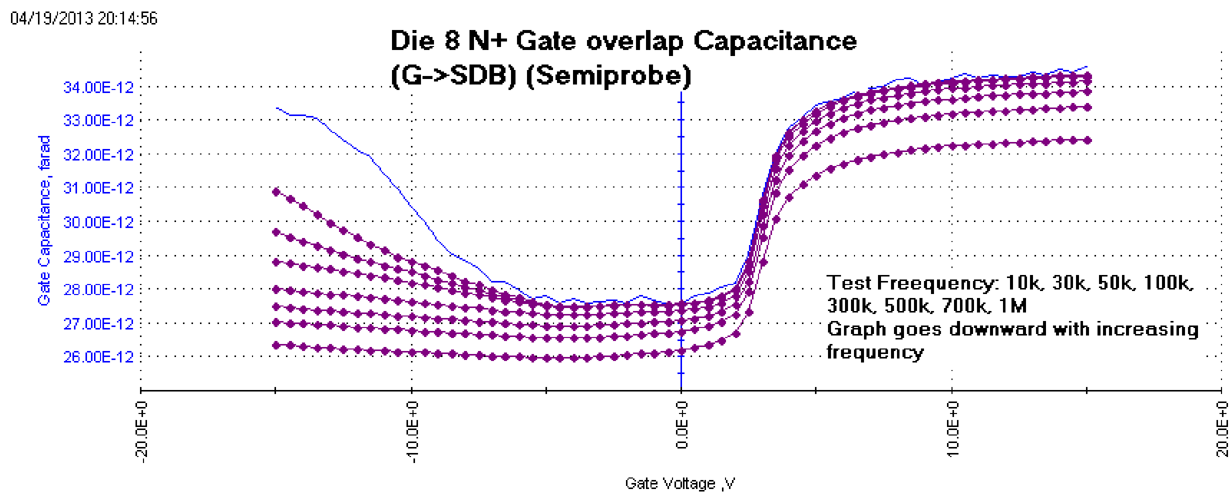
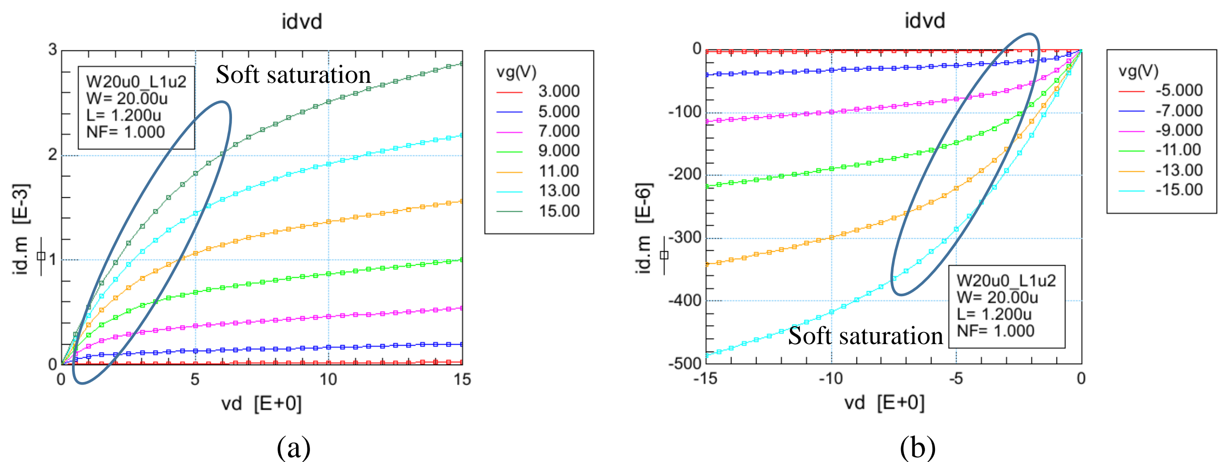


Fig. 6.10. Measured gate-to-drain/source/body (total gate capacitance) of SiC NMOS at different frequencies.

6.4 Soft transition from triode to saturation

The electric field generated by the interface trapped charge is two dimensional. The vertical component of the electric field affects the mobility, threshold voltage, flat band voltage and subthreshold slope but the lateral field shapes the total electric field near the drain end. The carrier velocity **VSAT** is influenced by the lateral electric field at the drain and it has been found that the velocity of the carriers saturates softly in presence of the interface trapped charge [150]. Since the trapped charge distribution is gate bias dependent, the extent of the velocity saturation also becomes gate voltage dependent. In addition, the diffusion resistance and contact resistance are higher and the effective mass of the charge carriers ($0.37*m_0$ vs $0.22*m_0$ in Si for electron) is greater in SiC material [151]. As such the transition from triode to saturation in a SiC MOSFET is relatively soft. The soft saturation of SiC NMOS and PMOS are shown in Fig. 6.11.



(a) (b)

Fig. 6.11. Illustration of soft saturation in SiC (a) NMOS and (b) PMOS

6.5 Effects on High Temperature Behavior

Besides the interface trapped charge, there is also fixed charge in the oxide if the gate dielectric is contaminated during the device fabrication. The interface trapped charge along with the fixed oxide charge not only change the threshold voltage of a MOS device but also play a significant role in device reliability. Lelis et al. [152] has demonstrated that due to the presence of

interface trapped charge and fixed oxide charge the threshold voltage of a MOSFET drifts if the device is stressed under bias at high temperature (above 200 ° C) over a long period of time. Yano et al. [153] have also reported threshold voltage instability in 4H-SiC MOSFETs annealed with $POCl_3$ and NO and attributed near-interface traps as the primary cause. Although the reliability testing in these reports was done for a SiC power MOSFET the observation is equally true for any SiC MOS device which has poor interface quality. The p-type MOSFET from the Raytheon HiTSiC process suffers from similar threshold voltage shift as demonstrated in Fig. 6.12. It is found that the threshold voltage of the PMOS initially decreases with temperature but if the device is kept biased at higher temperature the threshold voltage starts to increase. In the measurement as shown in Fig 6.13, the PMOS has already passed several hours under bias when the measurement at 300 ° C was taken. Under voltage and temperature stress, some of the interface or near interface states can be permanently charged and thus cause a permanent shift in the threshold voltage. The threshold voltage of a SiC NMOS over temperature is shown in Fig. 6.13. The steady decrease in threshold voltage indicates that the effects of interface trapped charge is less severe in SiC NMOS.

Without the secondary effects as described in Chapter 5 the threshold voltage of a MOSFET device is related to the device and material property as follows [154]:

$$\boldsymbol{V_{TH} = \Phi_{ms} - \frac{Q_B}{C_{OX}} + 2\Phi_F - \frac{Q_o}{C_{OX}}} \qquad \textbf{6.4}$$

where Φ_{ms} is the metal-semiconductor work function difference, Q_B is the total depletion charge, C_{OX} is the total oxide capacitance, $2\Phi_F$ is the strong inversion surface potential and Q_o is the sum of fixed oxide charge and interface trapped charge. In a SiC MOSFET the dominant part of $Q_o$is the trapped charge and as such fixed charge can be neglected. For an NMOS, $Q_o$is negative and for a PMOS $Q_o$is positive and by Eq. 6.1 threshold voltage increases in both NMOS and

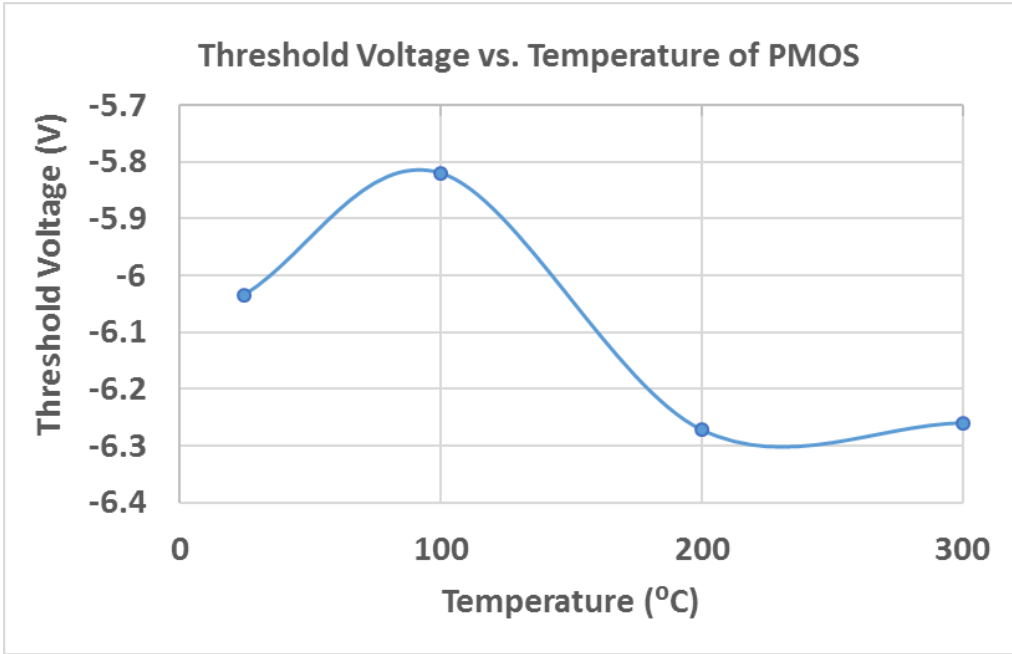


Fig. 6.12. The threshold voltage of a 20 µm/2µm SiC PMOS over temperature showing aging issues.

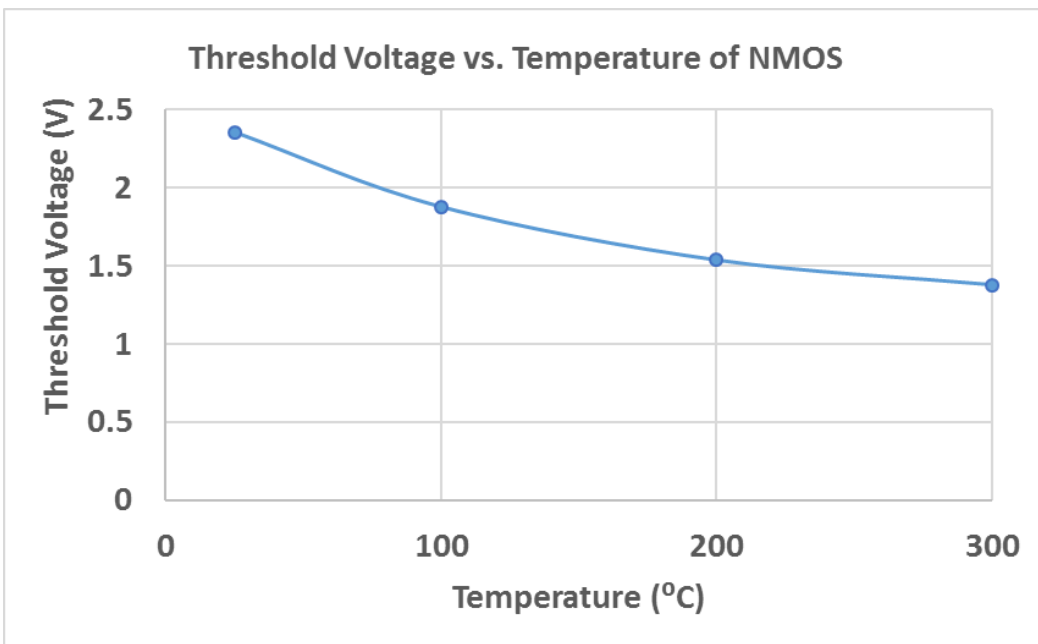


Fig. 6.13. The threshold voltage of a 20µm/2µm SiC NMOS over temperature.

PMOS due to the interface trapped charge. $Q_o$is a complicated function of the Fermi level and the density of states and thus depends on the gate bias. At higher temperature, the intrinsic carrier concentration increases and the surface potential decreases and thus threshold voltage in a MOS device tends to decrease at higher temperatures. Also, the probability of the interface states being occupied by the carriers is less at higher temperature. So, the decrease in threshold voltage should be more pronounced when the temperature is increased unless the device displays aging issues.

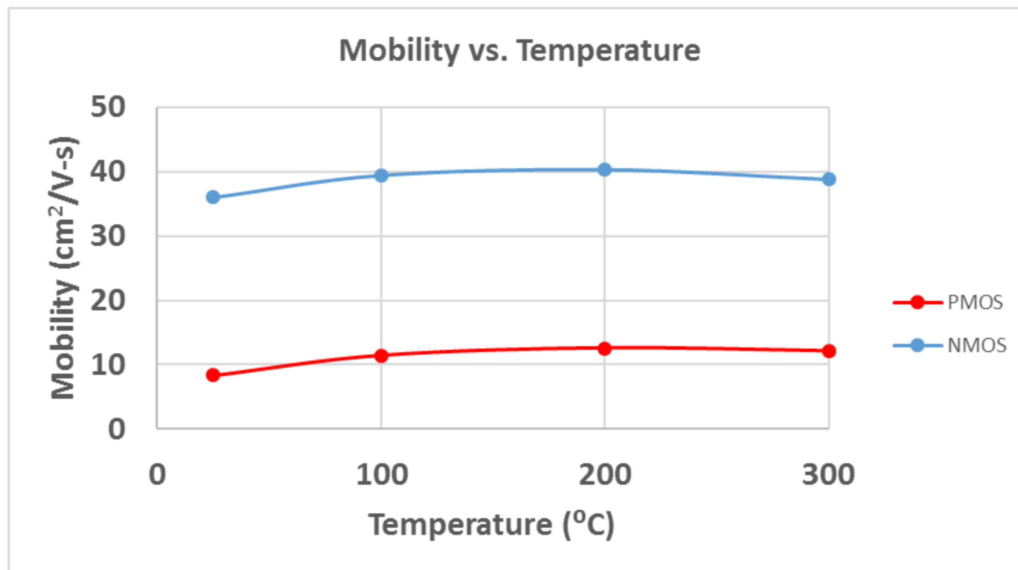


Fig. 6.14. Mobility of 20 µm/2µm SiC NMOS and PMOS over temperature.

The dependence of mobility on temperature in a SiC MOSFET is completely different than that in a Si MOSFET. In a Si device, the mobility is decreased due to the increase in phonon scattering which is resulted by the increased lattice vibration at higher temperature. But in SiC MOSFETs, the mobility is primarily determined by the coulomb scattering from the interface trapped charge and as previously mentioned the interface states are less likely to be occupied by the charge carriers at elevated temperature. This ensures less trapped charge and less coulomb scattering and thus an increase in mobility at higher temperatures as shown in Fig. 6.14. The

smaller influence of interface trapped charge at higher temperatures can also be found from the C-V curve which is demonstrated in Fig. 6.15. The C-V curves become narrower at high temperature which indicates that the flat band voltage increases and the threshold voltage decreases in an NMOS.

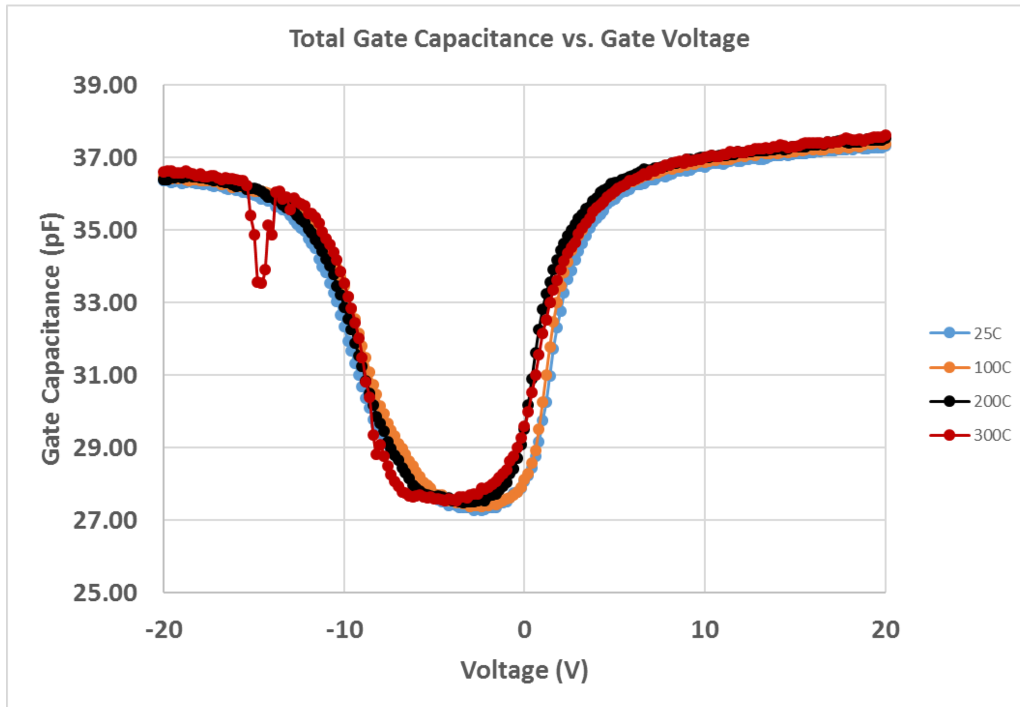


Fig. 6.15. The measured total gate capacitance ($C_{g\text{-}dsb}$) of an NMOS over temperature.

6.6 Summary

The origin of the interface states in a SiC MOSFET is discussed and the theory of interface trapped charge related physics is described. It is found that the interface trapped charge affects the mobility, threshold voltage, subthreshold slope, saturation characteristics and temperature behavior of a MOS device. The effects are demonstrated for SiC MOSFETs with measured device characteristics.

CHAPTER 7 MODEL DEVELOPMENT OF SIC MOSFET WITH VERILOG-A

7.1 Implementation of BSIM470 in Verilog-A

The roadblock of using the BSIM4 model as a foundation for model development in a new process is the unavailability of the model code in Verilog-A. Fortunately, at the University of Arkansas, the C code of BSIM430 was converted to Verilog-A [155] using a software tool called Paragon and the foundation for implementing new models related to SiC MOSFET was already available. This work is based on the BSIM470 and a significant number of enhancements were added to the version over BSIM430. The enhancements which are related to the SiC MOSFET are implemented in the Verilog-A version of the BSIM470. Those enhancements include:

- Non-silicon substrate and non-SiO_2 gate dielectric model using the model flag **MTRLMOD**. Assigning 1 to the parameter activates the new model.
- A new mobility model which includes the effects of coulomb scattering resulted by the presence of interface trapped charge. The model can be selected by assigning 3 to the model parameter **MOBMOD.**
- Trap assisted leakage current modeling of the junction diodes.
- A new definition of effective gate-to-source voltage for C-V model.
- Effective oxide thickness model for high- κ gate dielectric, electric and physical oxide thickness model to take into account the effects of process variation.
- A charge centroid model for quantum mechanical tunneling of inversion carriers into the oxide
- A new temperature dependent bandgap model.
- Enhancement of the threshold voltage shift model due to pocket implant.

- A new channel length and temperature dependent zero bias mobility model.
- A new temperature scaling model.

The enhancements related to gate tunneling, substrate resistor network, noise, well proximity effects and velocity overshoot are specific to deep sub – 100nm process node and were not implemented in the Verilog-A version of BSIM470. The new enhancements required almost two thousand lines of Verilog-A code. There were few crucial bugs in the Verilog-A version of the BSIM4.3.0 such as the junction capacitance at zero V_{bs} and the total drain-to-gate capacitance at zero V_{dg} are zero. The bugs resulted from the hard coding of the charge expressions to zero for zero biases. Although this was necessary for the C code implementation, it is not necessary for the Verilog-A implementation. The bugs are fixed by removing the conditional hard coding.

7.2 Modeling of Interface Traps Related Effects

The physical means to include the effects of interface trapped charge is to include the related charge in the charge neutrality equation as shown in Eq. 5.2 so that:

$$\boldsymbol{Q'_G + Q'_C + Q'_0 + Q'_{it} = 0} \qquad 7.1$$

where Q'_0 and Q'_{it} are fixed oxide charge density and interface trapped charge density respectively. Q'_0 is typically bias independent and can be lumped into the flat band voltage equation. But $Q'_{it}$is bias dependent and alter the MOSFET device characteristics dramatically as explained in section 6.2. If the relationship between the surface potential and the interface trapped charge is included in Eq. 7.1 then an expression of the inversion charge with respect to the gate bias can be established using the voltage balance equation, charge balance equation, Eq. 5.3 and the solution of Poisson's equation. The interface trapped charge density can be found from the density from interface states and the Fermi-Dirac function. The density of interface states is given by [156]:

$$\boldsymbol{D_{it}(E) = D_{it,mid} + D_{it,edge} exp\left(\frac{E-E_C}{\sigma_{it}}\right)} \qquad 7.2$$

where $D_{it,mid}$is the mid-gap density of state and generally a constant value, $D_{it,edge}$is the constant density of state near the conduction band edge and $\sigma_{it}$is a fitting parameter which models the tail of the density of states exponential. Eq. 7.2 provides a bowl-shaped density of states distribution in the bandgap at the interface. The Fermi-Dirac function describes the probability of charge carriers being occupied by a state is given by:

$$\boldsymbol{f(E) = \frac{1}{exp\left(\frac{E-E_F}{kT}\right)+1}} \qquad 7.3$$

The interface trapped charge per unit area can be found by integrating the multiplication of Eq. 7.2, 7.3 and q under the assumption of a sheet charge layer of interface charge and is found as:

$$\boldsymbol{Q_{it}(\Phi_S) = q\int_{E_i}^{E_F} f(E) D_{it}(E) dE = q\left\{D_{it,mid}\Phi_S + D_{it,edge}\sigma_{it} exp\left(\frac{E_i-E_C}{\sigma_{it}}\right)\left[exp\left(\frac{\Phi_S}{\sigma_{it}}\right) - 1\right]\right\}} \qquad 7.4$$

There are numerous issues in this physical means of incorporating the effects of interface trapped charge in the core BSIM4 model equations. Some of the issues are:

- Eq. 7.4 indicates a dramatically different relationship of the interface trapped charge with the surface potential than the relationship of the inversion charge with the surface potential as demonstrated in Eqs. 5.13 and 5.16. The definition of effective gate-to-source voltage V_{gsteff} which is derived from the relationship between inversion charge and surface potential breaks down as do all the other current and charge equations. A completely new set of model equations and

parameter extraction sequence are required and the model no longer holds to the foundation of BSIM4. This is definitely not a realistic approach.

- It is also extremely difficult to find appropriate approximations under which a closed form expression between inversion charge, interface trapped charge and terminal biases exists. An implicit model equation which require numerical methods is not attractive for compact modeling.
- The inclusion of interface trapped charge equations into the intrinsic current and charge equations will make the model very complex and as such the simulation time will increase significantly. Besides, it is not uncommon to have convergence issues when the model equations are complex and implicit.

The strategy to modify the BSIM4 model for including the effects of interface trapped charge adopted in this work is as follows:

- A comprehensive effort is undertaken to model the SiC MOSFET device characteristics with the built-in HSPICE BSIM465 as demonstrated in section 5.3 and found what characteristics the BSIM4 version fails to model.
- The physical origin of the failure is investigated. For example, the low vertical field mobility is reduced due to coulomb scattering and the high vertical field is decreased by the scattering from the surface roughness.
- In the next step, it is identified if there are model formulations in BSIM4 for the related physics. As an example, BSIM470 has an advanced mobility model which takes into account the effects of coulomb scattering in the mobility reduction. The already existing equations are modified appropriately or new equations are added to remove the discrepancy as found with the BSIM470 model. Such an example is

the addition of body bias related terms in the new mobility equation so that the reduction in mobility for non-zero body bias can be modeled.

- A correct parameter extraction sequence is determined since after modifying or adding new equations the conventional sequence is no longer very effective.

The BSIM4 model can easily be broken if caution is not exercised when the model is used for new technology. Some important points which should be kept in mind while implementing new equations in a complicated model like BSIM4 are:

- BSIM4 uses a single continuous charge and current equations which are valid for all region of operations. Under no circumstances, the new equations should include piece-wise formulation.
- In BSIM4, smoothing functions are used for the terminal biases to formulate continuous functions. The effective gate-to-source voltage V_{gsteff}, effective drain-to-source voltage V_{dseff} and effective body-to-source voltage V_{bseff} should be used instead of external V_{gs}, V_{ds} and V_{bs} if new bias dependent equations are introduced.
- To keep the simulation time reasonable, the use of bias dependent equations should be limited since introduction of such equations add more overhead to the Jacobian matrix.
- The number of new parameters added in the model should kept as small as possible since the more parameters the more complicated the extraction sequence.

The modifications relevant to SiC MOSFETs are added in the Verilog-A version of BSIM470 using a model flag called SICMOD. If the flag is set to “0”, none of the changes will be

activated and the model will act as the BSIM470 model. By assigning "1" to the model flag, the SiC MOSFET related enhancement can be activated. The modified model is called BSIM4SIC.

7.2.1 Body Effects Modeling

Mobility modeling – The **MOBMOD** = 3 mobility model as shown in Eq. 5.158 is:

$$\mu_{eff} = \frac{\mu 0(Temp, L)}{1+\left(UA+UC \cdot V_{bseff}\right)\left[\left(\frac{V_{gsteff}+C_{n,p}(VTH0-VFB-2\Phi_F)}{6 \cdot TOXE} \cdot 10^{-8}\right)\right]^{EU} + \frac{UD}{\left[0.5 \cdot \left(1+V_{gsteff}/V_{gs_on}\right)^{UCS}\right]}} \qquad 7.5$$

To introduce the body bias dependent mobility reduction, **UD** is replaced by:

$$\mathbf{UD} + UDSIC \cdot \left(\sqrt{\varphi_s - V_{bseff}} - \sqrt{\varphi_s}\right) \qquad 7.6$$

where **UDSIC** is a model parameter and is used to adjust the transfer characteristics at low gate bias. **UCS** is replaced by:

$$UCS + \frac{UCSSIC \cdot V_{bseff}}{1+\left(\sqrt{\varphi_s - V_{bseff}}\right)^{UCSSIC1}} \qquad 7.7$$

Where **UCSSIC** and **UCSSIC1** are model parameters and are used to adjust the transfer characteristics in medium gate bias. To adjust the peak in the transconductance curve, V_{gs_on} is replaced by:

$$V_{gs_on} + UBEGMPKSIC \cdot V_{bseff} \qquad 7.8$$

where **UBEGMPKSIC** is a model parameter.

Bulk charge effects modeling – It has been found that the effects of bulk charge when the body is biased at non-zero voltage is more prominent in the short channel devices as demonstrated in Fig. 7.1 for a SiC PMOS.

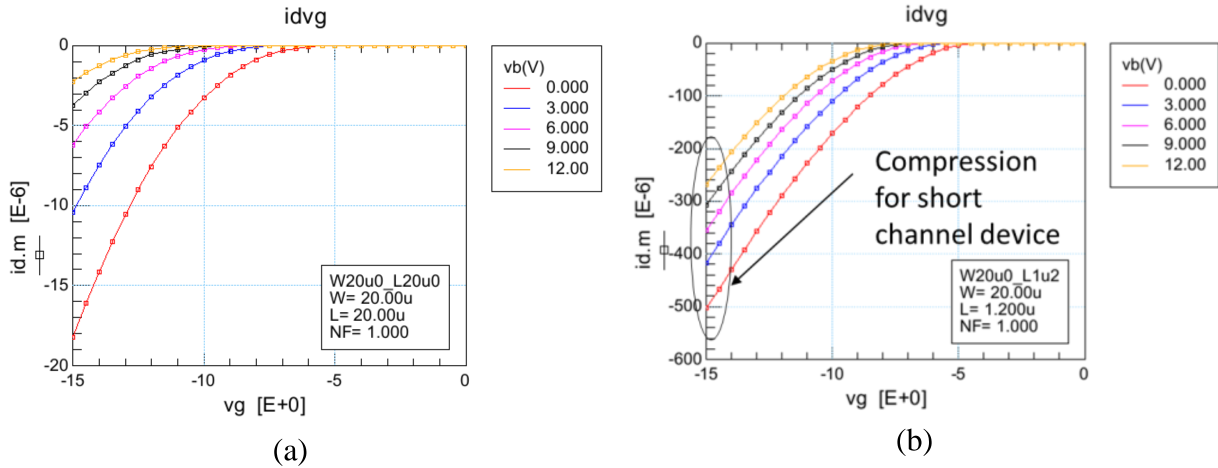


Fig. 7.1. Transfer characteristics of SiC PMOS in saturation; (a) long channel and (b) short channel device.

The bulk charge coefficient as shown in Eq. 5.63 is:

$$\boldsymbol{A_{bulk}} = \left\{\boldsymbol{1} + \frac{\boldsymbol{K1}}{\boldsymbol{2\sqrt{2\Phi_F - V_{bseff}}}}\left[\frac{\boldsymbol{A0 \cdot L_{eff}}}{\boldsymbol{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}}} \times \left(\boldsymbol{1 - AGS \cdot V_{gsteff}}\left(\frac{\boldsymbol{L_{eff}}}{\boldsymbol{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}}}\right)^{\boldsymbol{2}}\right) + \frac{\boldsymbol{B0}}{\boldsymbol{W_{eff} + B1}}\right]\right\} \times \frac{\boldsymbol{1}}{\boldsymbol{1 + KETA \cdot V_{bseff}}} \qquad 7.9$$

To model the transfer characteristics compression in short channel devices, $\boldsymbol{KETA} \cdot V_{bseff}$ is replaced by:

$$\boldsymbol{KETA \cdot V_{bseff} + KETASIC \cdot \left(\sqrt{\varphi_s - V_{bseff}} - \sqrt{\varphi_s}\right)} \qquad 7.10$$

where **KETASIC** is a model parameter. By adjusting relative strength of the first and second term in Eq. 7.10, the transfer characteristics of the SiC MOSFET at different body biases in saturation region can be made more dispersed or compressed.

7.2.2 Flat band Voltage Shift Modeling

In BSIM470, the flat band voltage for accumulation charge calculation as shown in Eq.5.83 is:

$$V_{fbzb} = V_{TH}\left(V_{gs} = V_{ds} = V_{bs} = 0\right) - 2\Phi_F - K1\sqrt{2\Phi_F} \qquad 7.11$$

Eq. 7.11 is modified as follows to include the shift in flat band voltage:

$$V_{fbzb} = V_{TH}\left(V_{gs} = V_{ds} = V_{bs} = 0\right) - 2\Phi_F - K1CVSIC \cdot K1\sqrt{2\Phi_F} + DELVFBSIC \qquad 7.12$$

where **DELFBSIC** is a model parameter and can be adjusted according to the interface trapped charge related flat band voltage shift. Since body effect coefficient parameter **K1** is also used in drain current calculation, another model parameter **K1CVSIC** is introduced in Eq. 7.12 to decouple the effect of the **K1** parameter from DC current model. **K1CVSIC** is added in all the charge equations where **K1** has been used.

7.2.3 Modeling of triode-to-saturation soft transition

The transition from triode to saturation in the output curve can be tuned by **A1** and **A2** parameters as shown in Eq. 5.39 and by **DELTA** parameter through Eq. 5.40. Although Eq. 5.39 has a dependency on the effective gate-to-source voltage, it is not strong enough to model the soft transition found in the SiC MOSFET output characteristics. A much better optimization is achieved by making **DELTA** dependent on the V_{gsteff} as follows:

$$DELTA_{NEW} = DELTA_{OLD} + DELTASIC \cdot V_{gsteff}^{DELTASIC1} \qquad 7.13$$

where **DELTASIC** and **DELTASIC1** are model parameters.

7.2.4 Intrinsic carrier concentration model

The intrinsic carrier concentration model included in BSIM465 as a part of the new **MTRLMOD** model cannot be used for SiC MOSFET. A new model is included for the temperature dependent intrinsic carrier concentration as follows [7]:

$$n_i = 1.7\times10^{16} \cdot Temp^{TNIASIC} \cdot e^{-TNIBSIC/Temp} \tag{7.14}$$

where **TNIASIC** and **TNIBSIC** are model parameters.

7.3 A new parameter extraction method for MOSFET C-V

The parameter extraction method used in BSIM470 does not include the extraction of the overlap length L_{OV} and also fail to isolate fringing capacitance and overlap capacitance from the parasitic gate-to-drain/source/body capacitance [157]. The new parameter extraction method proposed in this work solves this issues and allows it to achieve better MOSFET gate C-V optimization results. The extraction sequence is as follows:

Step 1 – The effective oxide thickness **EOT** is calculated from the accumulation capacitance which can be extracted from the $C_{ox} - V_{gb}$ curve (Fig. 7.2) using the following equation:

$$C_{ox,acc} = \frac{\varepsilon_{ox} \cdot \mathrm{EOT}}{W_{drawn} \cdot L_{drawn}} \tag{7.15}$$

The extracted value is also assigned to **TOXE** and **TOXP** and the model parameter **DTOX** is assigned to "0". The model parameter **ACDE** is extracted from the transition region between accumulation and depletion in the $C_{ox} - V_{gb}$ as shown in Fig. 7.2.

Step 2 – The total gate capacitance C_{gg} is extracted from the deep inversion region of $C_{g\text{-}dsb}$ *vs.* $V_{g\text{-}dsb}$ curve at $V_{g\text{-}dsb} = VDD$ as shown in Fig. 7.3.

Step 3 – The total parasitic gate capacitance ($C_{ov} + C_f$) is extracted from the measured $C_{g\text{-}ds}$ *vs.* $V_{g\text{-}ds}$ curve at $V_{g\text{-}ds} = 0V$ as demonstrated in Fig. 7.4.

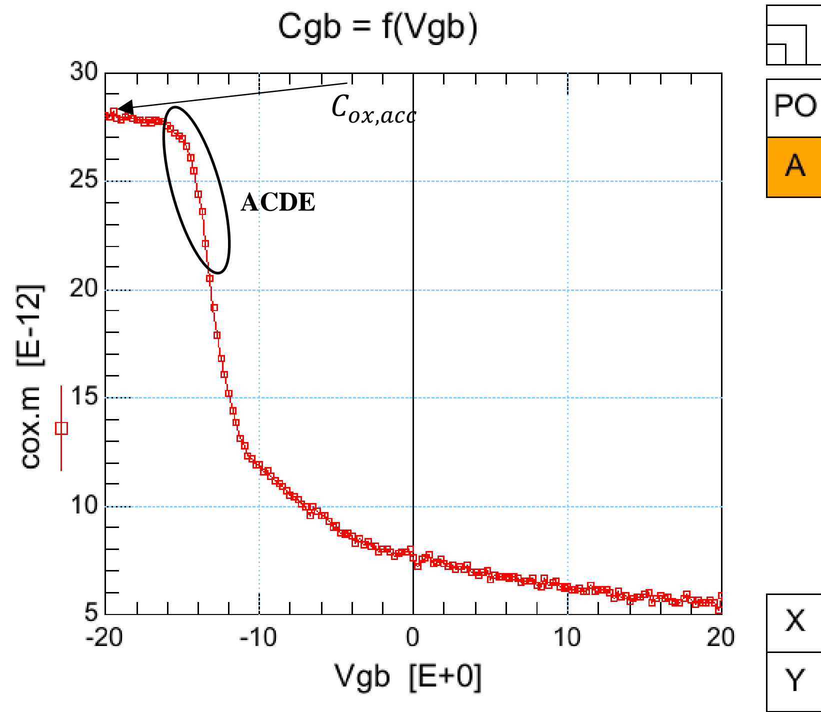


Fig. 7.2. Measured oxide capacitance vs. gate-to-body voltage an NMOS cap.

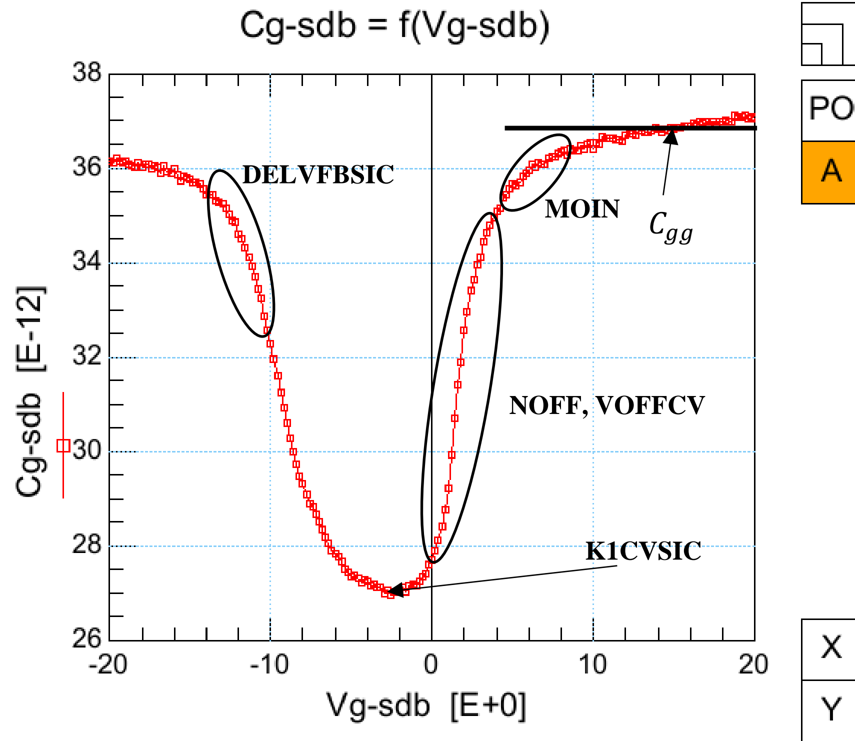


Fig. 7.3. Measured total gate capacitance vs. gate-to-drain/source/body voltage.

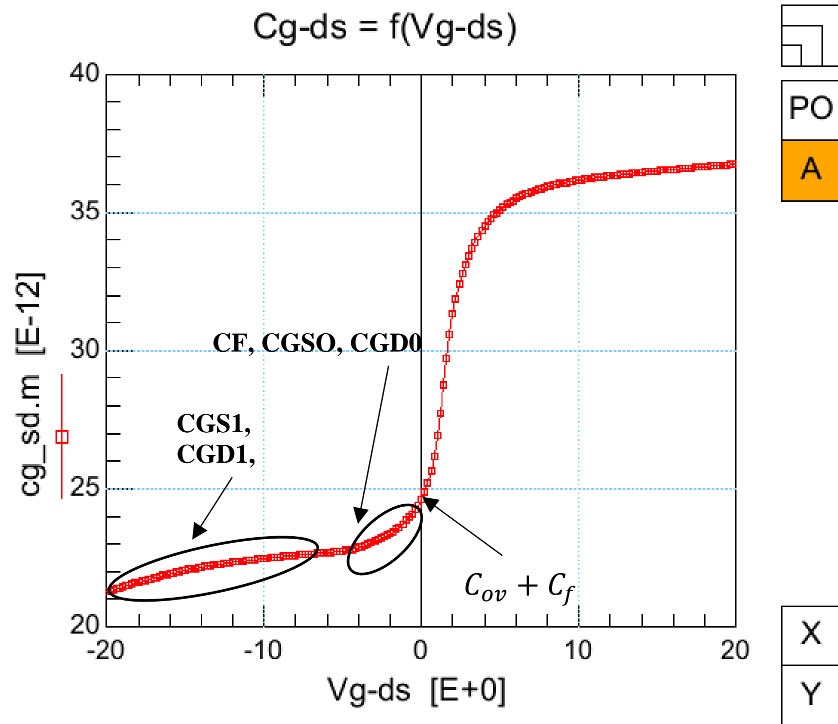


Fig. 7.4. Measured gate-to-drain/source capacitance vs. gate-to-drain/source voltage of an n-type MOSFET.

Step 4 – The total inversion capacitance C_{inv} is found by subtracting the total parasitic gate capacitance $C_{ov} + C_f$ from the total gate capacitance C_{gg}.

Step 5 – The effective length L_{eff} is calculated from the total inversion capacitance using the following equation:

$$C_{inv} = \frac{\varepsilon_{ox} \cdot EOT}{W_{drawn} \cdot L_{eff}} \tag{7.16}$$

The difference between the drawn dimension and the effective dimension is apparent in Fig. 7.5. The effective width is also found by subtracting the total oxide encroachment length from the drawn length. It should be noted that the device structure used for total gate capacitance measurement consists of multiple fingers with a large width of each finger and thus the effective width is approximately equal to the drawn width.

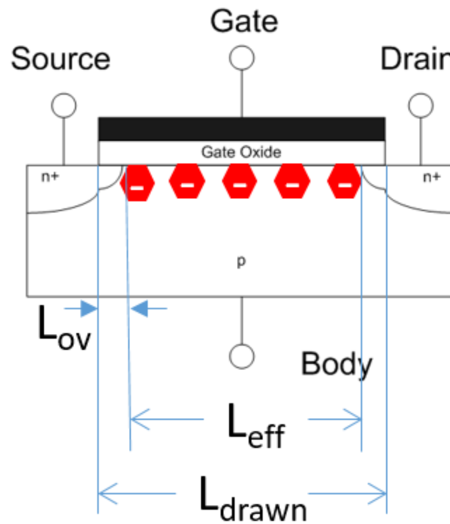


Fig. 7.5. The definitions of drawn, effective and overlap length dimension in a MOSFET device.

Step 5 – The effective length L_{eff} is subtracted from L_{drawn} to find L_{ov} and the overlap capacitance is calculated using the following equation:

$$\boldsymbol{C_{ov}} = \frac{\boldsymbol{\varepsilon_{ox} \cdot EOT}}{\boldsymbol{W_{drawn} \cdot L_{ov}}} \qquad 7.17$$

Step 6 – The fringing capacitance C_f is calculated by subtracting C_{ov} from the total gate parasitic capacitance as found in step 3.

Step 7 – All the capacitances thus far calculated are the combined capacitances from both the drain and source side. Since MOSFET is a symmetrical device, the capacitances can be equally distributed to the source and drain terminals. Also, the unit of parasitic capacitance related parameter is F/m. Therefore, the fringing and overlap parasitic capacitance related model parameters are extracted as shown in Table 7.1.

Table 7.1. Model parameter extraction of overlap and fringing capacitances.

Parameter name	Extracted estimated value	Optimization region
CF	$\frac{C_f}{2W_{drawn}}$	See Fig 7.4
CGS0 + **CGS1**, **CGD0** + **CGD1**	$\frac{C_{ov}}{2W_{drawn}}$	See Fig 7.4
CKAPPAD, CKAPPAS	Adjusted according to the decrease in overlap capacitance as the device moves into deep accumulation	See Fig 7.4

The partitioning of **CGS0** (or **CGD0**) and **CGS1** (**CGD1**) depends on the decrease of C_{g-ds} (Fig 7.4) from the point where V_{g-ds} is zero to $V_{g-ds}=VDD$.

Step 8 – The intrinsic capacitance related model parameters such as **K1CVSIC**, **NOFF**, **VOFFCV** and **MOIN** are optimized from the regions as indicated in **Error! Reference source not found.**. These parameters are extracted after some DC parameter extraction steps and will be discussed in section 7.6. By adjusting the value of **K1CVSIC**, the minimum value of the total gate capacitance can be optimized. **NOFF** adjusts the slope of the transition of the C_{g-dsb} *vs.* V_{g-dsb} curve

when the device turns on and **VOFFCV** can be varied to adjust the parallel shift of the transition. **MOIN** is used to adjust the transition in the moderate inversion region as shown in **Error! Reference source not found.**.

7.4 Temperature scaling

The thermal dynamics of the charge carriers in a semiconductor device is very complex and requires rigorous numerical method for accurate modeling. In a Si MOSFET device, the optimum range of temperature at which the device can adequately perform is -40 ⁰ C to 150 ⁰ C. Typically the device characteristics such as mobility, threshold voltage, saturated velocity, drain/source parasitic resistance etc. are linearly dependent on temperature and can be empirically modeled using some monotonic equations. Unfortunately, as explained in section 6.5, the high temperature behavior of SiC MOSFET is not monotonic over the wide range of temperature at which the device can function. Potbhare et al. [158] has proposed a comprehensive high temperature model for SiC MOSFET for numerical simulation but the equations are implicit in nature and not suitable for compact modeling. In this work, a fully empirical approach was adopted for temperature scaling. At first, it is investigated which model parameters can be tuned to optimize the behavior of the SiC MOSFET. Then the parameters are extracted at four different temperature points. The temperature coefficients for each parameter is then calculated using a third order polynomial of the following form:

$$\boldsymbol{PARAM(Temp) = PARAM(TNOM) + TPARAMSIC1(Temp - TNOM) + TPARAMSIC2(Temp - TNOM)^2 + TPARAMSIC3(Temp - TNOM)^3} \quad 7.18$$

For example, if the parameter is **U0**, then Eq. 7.18 can be written as:

$$U0(Temp) = U0(TNOM) + TU0SIC1(Temp - TNOM) + TU0SIC2(Temp - TNOM)^2 + TU0SIC3(Temp - TNOM)^3 \quad 7.19$$

where **TU0SIC1**, **TU0SIC2** and **TU0SIC3** are first, second and third order temperature coefficients respectively of the model parameter **U0**. The list of parameters which are used for temperature scaling is shown in Table 7.2.

Table 7.2. MOSFET models parameters used for temperature scaling.

DC parameters	**VTH0, K2, U0, UA, UC, UD, UDSIC, UCS, UCSSIC, A0, AGS, NFACTOR, VSAT, KETA, KETASIC, PCLM, PVAG, B0, K3**
C-V parameters	**DELVFBSIC, NOFF, VOFFCV**

A new temperature scaling model was developed for the parasitic drain/source-to-body diode as the model available in BSIM4 is too complicated and was not very useful to model the wide bandgap SiC diode DC characteristics. The model parameters which are used for the temperature scaling of diode characteristics are **NJS**, **NJD**, **IJTHDFWD** and **IJTHSFWD**. The scaling is of the form as shown in Eq. 7.20.

$$NJD(Temp) = NJD(TNOM) \cdot \left(\frac{TNOM+273.16}{Temp+237.16}\right)^{TNJDSIC} \quad 7.20$$

where **TNJDSIC** is the temperature exponent.

7.5 Geometry Scaling

BSIM470 has a good width scaling option and it can be successfully used to achieve good width scaling of SiC MOSFET. Although the length scaling model of BSIM4.7.0 is quite advanced and comprehensive, it is not capable of globally scaling the SiC MOSFET channel lengths. There is few order of magnitude difference between the output conductance of the long channel and short

channel devices and one set of model parameters cannot model the characteristics of all channel lengths. The binning approach is used for length scaling and six different model parameter sets are extracted and optimized to include all different channel lengths.

7.6 Parameter Extraction and Optimization

The parameter extraction and optimization is performed using a graphical user interface (GUI) which is developed in the industry standard modeling tool ICCAP [159] based on the built-in BSIM4 module available in the tool. Unfortunately, the data files generated by the Keithley 4200 is in excel format and cannot be recognized by ICCAP. A python script was used to convert the data files into ICCAP recognizable format (.mdm). The python codes are provided in the Appendix. The extraction sequence is modified according to the enhancements made in the model since the sequence described in [160] can no longer be applied. The model parameters of the parasitic body diode are independent of the MOSFET parameters and thus are extracted and optimized first.

Diode parameter extraction and optimization – The extraction sequence is as follows:

Step 1 – The DC parameter **NJD** (emission coefficient) and **JSD** (reverse saturation current density) are extracted from the measured Gummel plot (log(idiode) vs. vdiode) of the high area diode and **JSWD** is extracted from the same plot of the high periphery diode. The forward current parameter **IJTHDFWD** is extracted from the idiode vs. vdiode plot of either high area or high periphery diode. The extraction region is illustrated in Fig. 7.6.. Since the drain-to-body diode and the source-to-body diode are interchangeable due to the symmetric nature of the MOSFET device, the parameter values extracted for one diode are also assigned to the other diode.

Step 2 – The diode capacitance related model parameters are extracted from the measured junction capacitance. **CJD**, **MJD** and **PBD** are extracted from the high area diode capacitance curve and **CJSWD**, **MJSWD** and **PBSWD** are extracted from the high periphery junction capacitance data. The region of extraction is shown in Fig. 7.7. The parameters for drain side diode are also used for the source side diode.

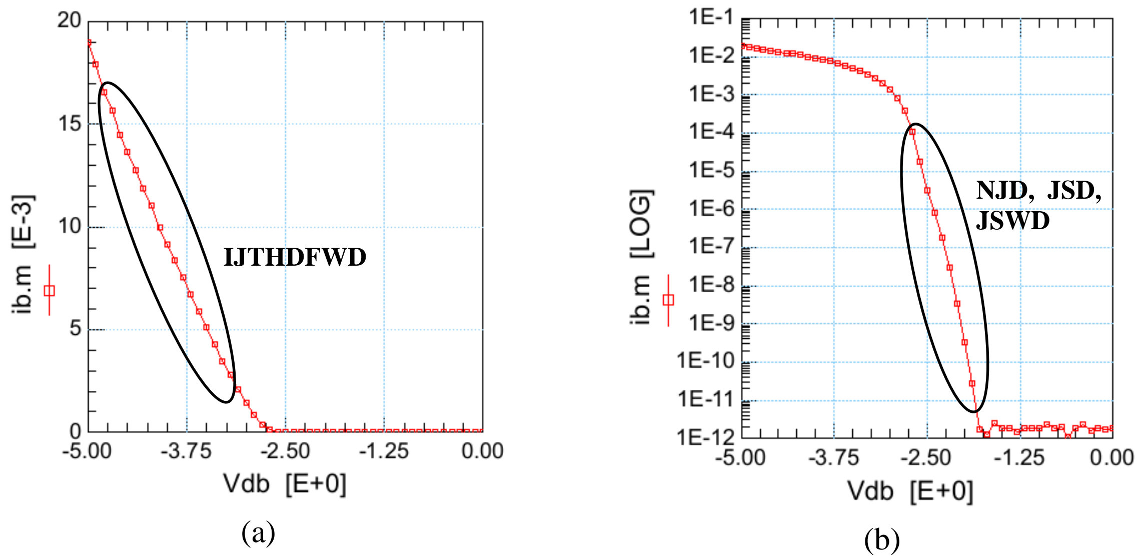


Fig. 7.6. Diode DC parameter extraction region; (a) forward current parameter and (b) emission coefficient and reverse saturation current density parameter.

Step 3 – The temperature scaled parameters **TNJDSIC** (**TNJSSIC**) is extracted from the Gummel plot (log(idiode) vs. vdiode) of the diode I-V characteristics measured at high temperature and **TIJTHDFWDSIC** (**TIJTHSFWDSIC**) is extracted from the linear region of idiode vs. vdiode also measured at high temperatures.

MOSFET parameter extraction and optimization - Once the diode parameters are extracted, the parameter set is used for all the length bins. The parameters related to the parasitics MOSFET gate capacitances as described in section 7.3. are then extracted following the first seven steps. These extracted parameters are also used for all the binning regions of length scaling. The parameter extraction and optimization of a particular length bin can then be done along with width

scaling and temperature scaling. In this part of the parameter extraction sequence, measured data for devices with fixed length and at least two widths at four different temperature points are required. The extraction sequence is as follows:

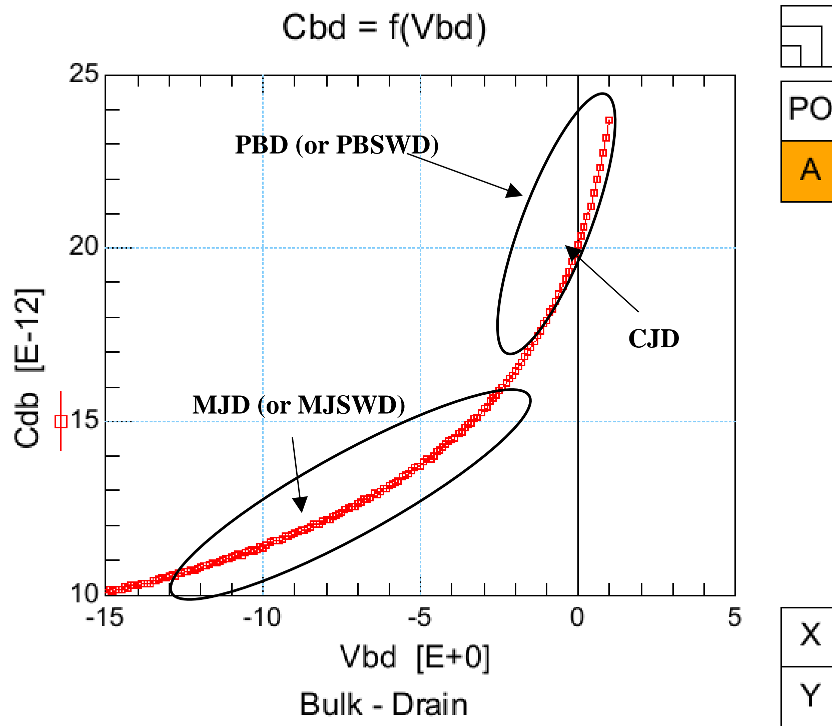


Fig. 7.7. Measured junction capacitance vs. body-to-drain voltage.

Step 1 – In the first step, the overlap width parameter **WINT** is extracted to calculate the effective channel width for drain current calculation. The parameter is extracted from measured $1/R_{DS}$ *vs.* W_{drawn} curve and is shown in Fig. 7.8.Fig. 7.8. Inverse of the drain-to-source resistance vs. drawn channel width. The length of the devices should be long. R_{DS} is the triode region resistance and calculated from the drain current at a low drain-to-source voltage. The x-axis intercept in the curve is equal to 2***WINT**. The overlap length parameter **LINT** is equal to the half of the value found in step 5 of section 7.3. The C-V overlap parameters **DLC** and **DWC** are equal to **LINT** and **WINT** respectively.

Step 2 – This step is started with the widest device. There are different ways to extract the threshold voltage from the measured transfer characteristics of a MOSFET device. Although the most popular method is the g_m - based approach [161], the method is not suitable for SiC MOSFET

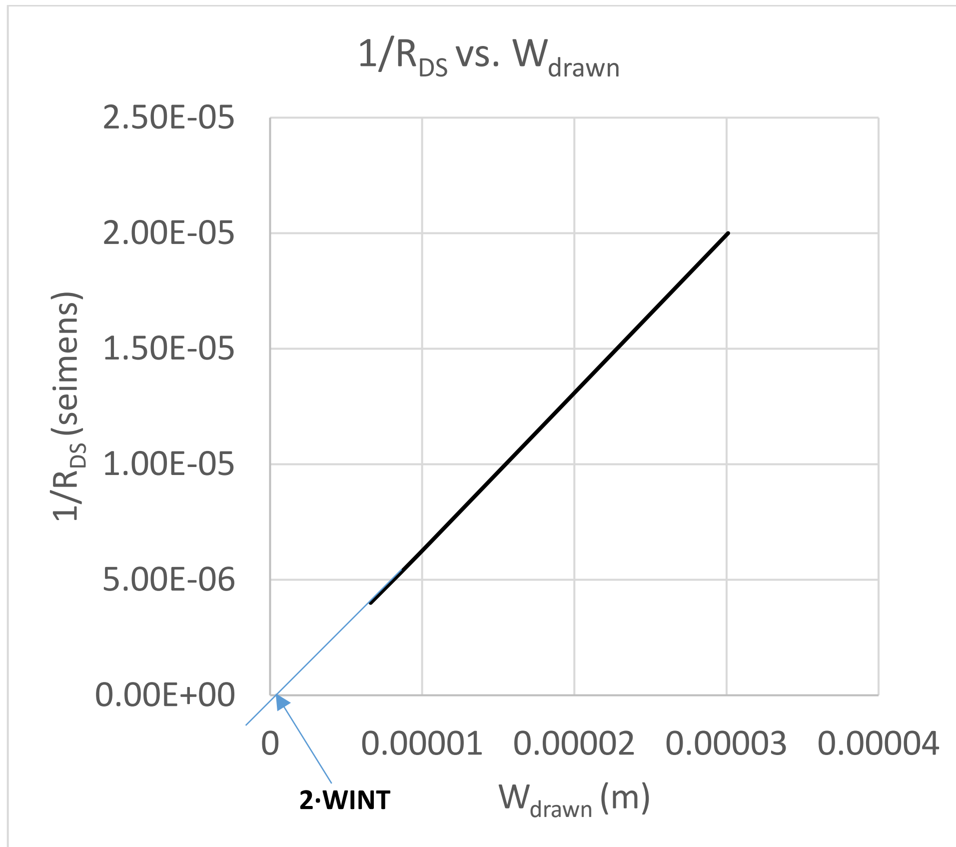


Fig. 7.8. Inverse of the drain-to-source resistance vs. drawn channel width. The length of the devices should be long.

since the long channel PMOS devices do not have a peak in the transconductance curve at low drain voltage. A rough estimate of the threshold voltage of the device is given by the gate-to-source voltage when the device operates in triode (V_{ds} = 0.5V) and the drain current is equal to:

$$\boldsymbol{I_{device}} = \frac{\boldsymbol{W_{eff}}}{\boldsymbol{L_{eff}}}\boldsymbol{I_{ref}} \qquad 7.21$$

where I_{ref} is the current of a wide and long device with W_{eff}=L_{eff}. 100 nA drain current of 20 μm/ 20 μm device is a good choice for this work. With this estimated value, **VTH0**, **K1** and **K2**

are extracted and optimized in this step from the regions as shown in Fig. 7.9.. The $I_d - V_g$ curve is measured at $V_{ds} = 0.5V$.

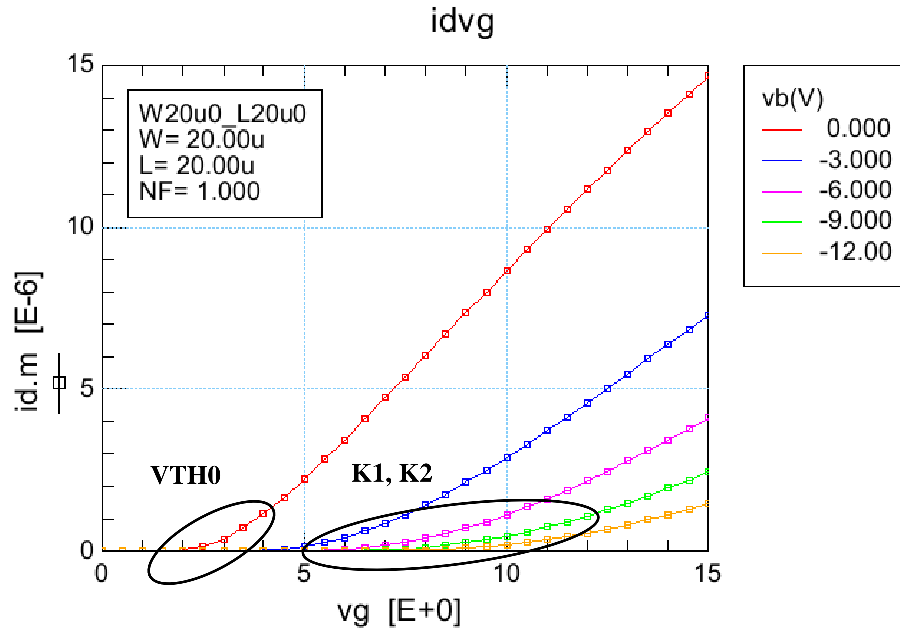


Fig. 7.9. Bias independent threshold voltage parameter VTH0 and body effect parameters K1 and K2 extraction.

Step 3 – The subthreshold parameters **VOFF**, **NFACTOR**, **DVT1** and **CDSCB** are extracted from the subthreshold regions of the curve as used in Step 2. The regions are illustrated in Fig. 7.10.. **VOFF** determines the subthreshold leakage at $V_{gs} = 0V$, **NFACTOR** adjusts the slope of the turn-on transition in $log(i_d) - V_g$ curve and **DVT1** and **CDSCB** are used to tune the subthreshold slope at non-zero body bias. The parameter **MINV** is used to optimize the moderate inversion region.

Step 4 – The mobility parameters **U0**, **UA**, **UC**, **UD**, **UCS**, **UDSIC**, **UCSSIC**, **UCSSIC1** and **UBEGMPKSIC** are extracted from the $I_d - V_g$ curve at $V_{ds} = 0.5V$. A rough estimation of **U0** can be obtained using the method described in section 6.2.1. The regions of optimization are shown in Fig. 7.11. It is also extremely important to track the corresponding $g_m - V_g$ curve while optimizing the mobility parameters.

Step 5 – The $I_d - V_g$ characteristics at *0.5V* drain-to-source voltage in strong inversion, subthreshold and the $g_m - V_g$ curve are investigated in this step and minor tweaking of the model

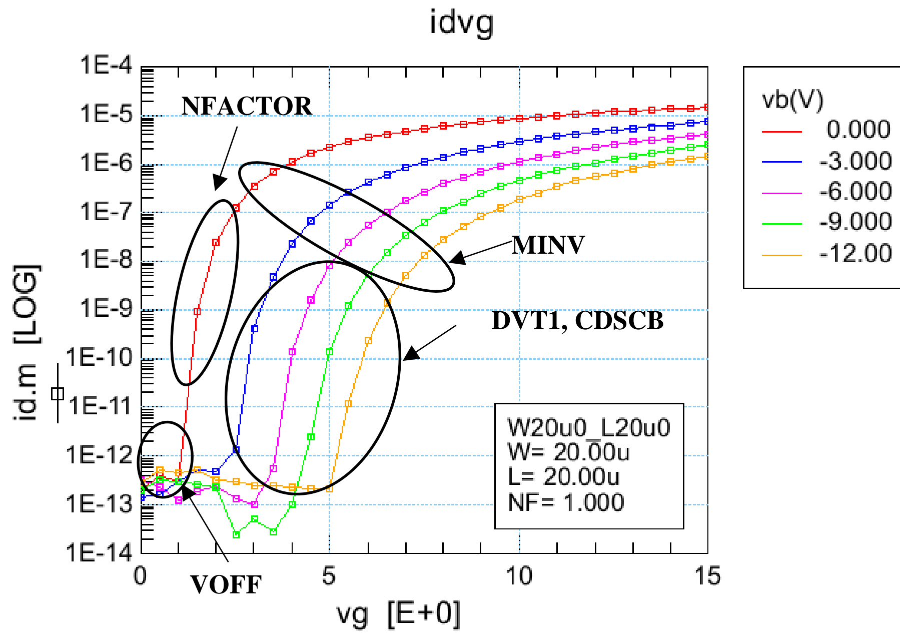


Fig. 7.10. Extraction of the weak and moderate inversion parameters.

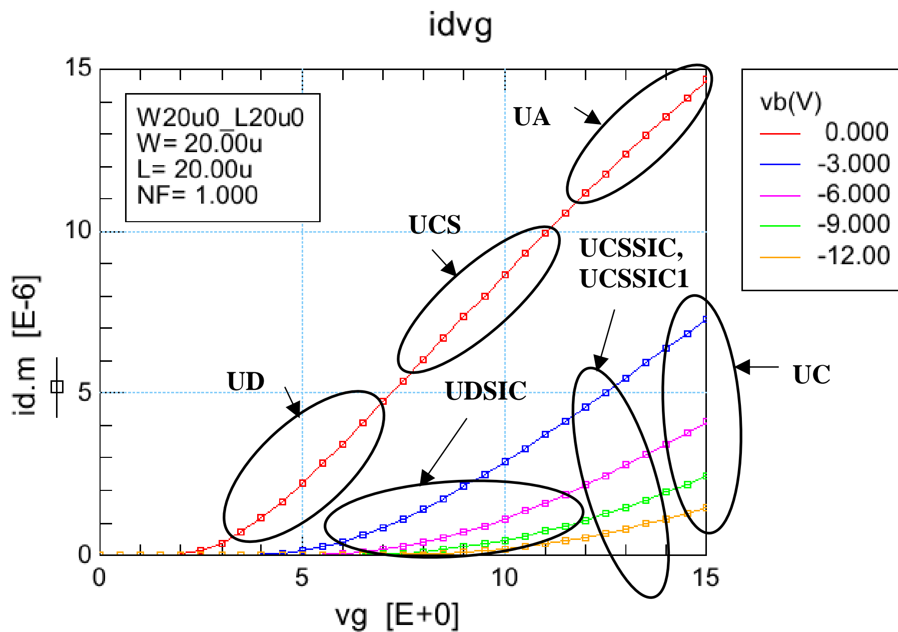


Fig. 7.11. Extraction of the mobility parameters.

parameters extracted in step 1 to 4 is done if major discrepancies are found between the measured and simulated data.

Step 6 – Threshold voltage shift parameter due to drain induced barrier lowering at high *Vds (15V)* and at different body biases are extracted from the $I_d - V_g$ characteristics at $V_{ds} = 15V$

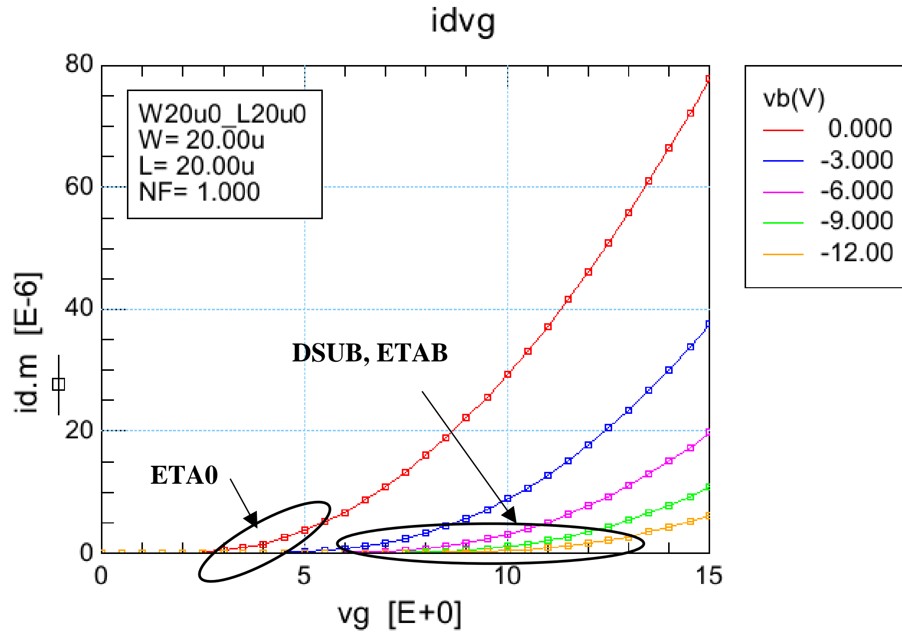


Fig. 7.12. Extraction of the threshold shift parameters due to drain induced barrier lowering.

in the strong inversion region. The parameters are **DSUB**, **ETA0** and **ETAB** and their regions of extraction are shown in Fig. 7.12.

Step 7 – The subthreshold slope in the $I_d - V_g$ curve at high V_{ds} *(15V)* is adjusted by the model parameter **CDSCD** as shown in Fig. 7.13.

Step 8 – The bulk charge coefficient parameters **A0**, **AGS**, **KETA** and **KETASIC** are extracted from the strong inversion region of $I_d - V_g$ curve characterized at $V_{ds} = 15V$. The optimization regions are demonstrated in Fig. 7.14. For devices with long channels, these three parameters are sufficient to model the transfer characteristics in saturation. But for short channel devices, the current at the large gate-to-source voltage is reduced due to parasitic drain-to-source resistance and the transfer curve becomes linear at the high current end. Thus, **RDS, PRWG** and

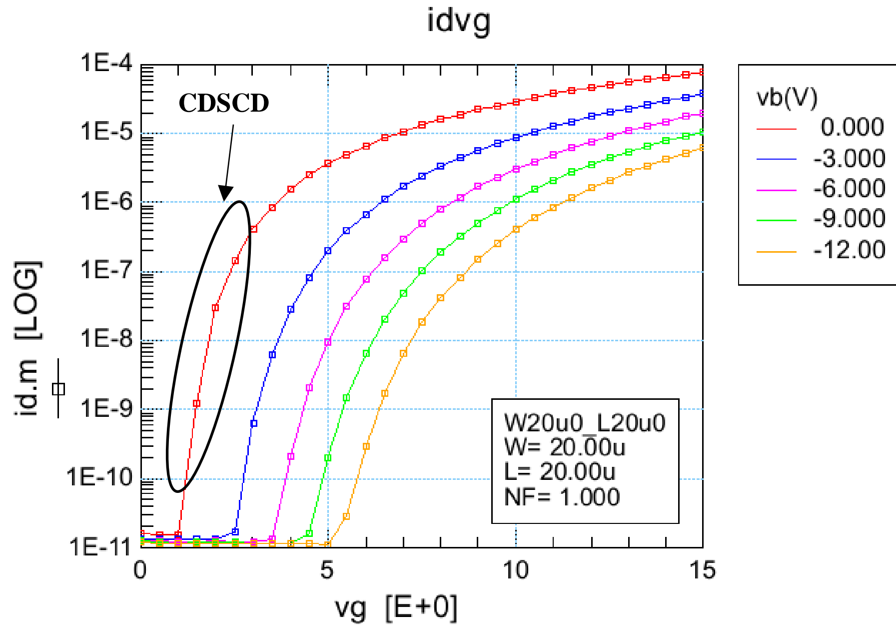


Fig. 7.13. Subthreshold slope adjustment in $I_d - V_g$ curve in saturation.

PRWB are also required to extract in this step when the channel length is 2 μm or below. **PRWG** is the gate bias coefficient and **PRWB** is the body bias coefficient. The extraction regions for parasitic drain-to-source resistance related parameters are also marked in Fig. 7.14. The corresponding transconductance curve ($g_m - V_g$) must be tracked in this extraction step because good optimization results in transfer characteristics do not guarantee good results in transconductance.

Step 9 – The saturation velocity parameter **VSAT** is usually extracted from the V_{dsat} values obtained from the measured $I_d - V_d$ curve at different gate voltages. But due to soft transition from triode to saturation in SiC MOSFET, the extracted values of V_{dsat} tend to have ambiguity and **VSAT** cannot be reliably extracted. Any value from 50×10^3 to 120×10^3 cm/s can be used and the value can be tuned by optimizing the spacing between output conductance curves ($g_d - V_d$) at different V_{gs}. A smaller **VSAT** makes the $g_d - V_d$ curve more compressive.

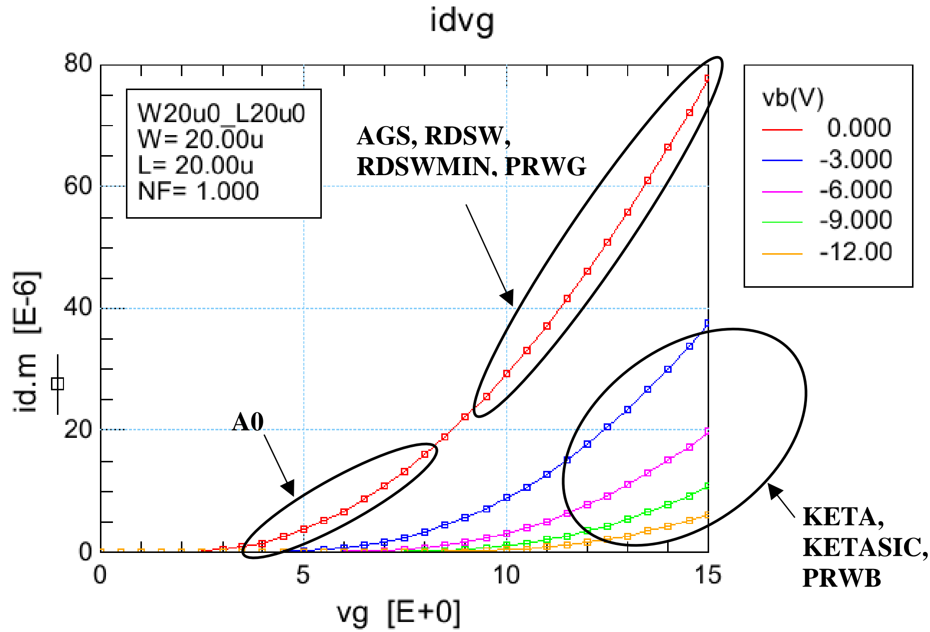


Fig. 7.14. Extraction of the bulk charge coefficient parameters and R_{DS} related parameters.

Step 10 – The output conductance parameters which are very important for short channel devices are extracted in this step. **DELTA**, **DELTASIC**, **DELTASIC1**, **A1** and **A2** are extracted from the knee of the output curves. **PCLM** and **PVAG** are extracted from the few volts of V_{ds} after the device enters saturation. The next few volts of the V_{ds} region is used for the optimization of **DROUT**, **PDIBLC1** and **PDIBLC2**. The output conductance parameters related to substrate current induced body effect **PSCEB1** and **PSCBE2** are extracted from the output curve a few volts before $V_{ds} = VDD$. Both $I_d - V_d$ and $g_d - V_d$ curves must be tracked when output conductance parameters are optimized. The optimization regions are shown in Fig. 7.15.

Step 11 – The transfer characteristics at low V_{ds} are revisited in this step. Although the bulk charge coefficient parameters and output conductance parameters should not significantly alter the $I_d - V_g$ curves in triode region, a minor tuning might be necessary to achieve better optimization results.

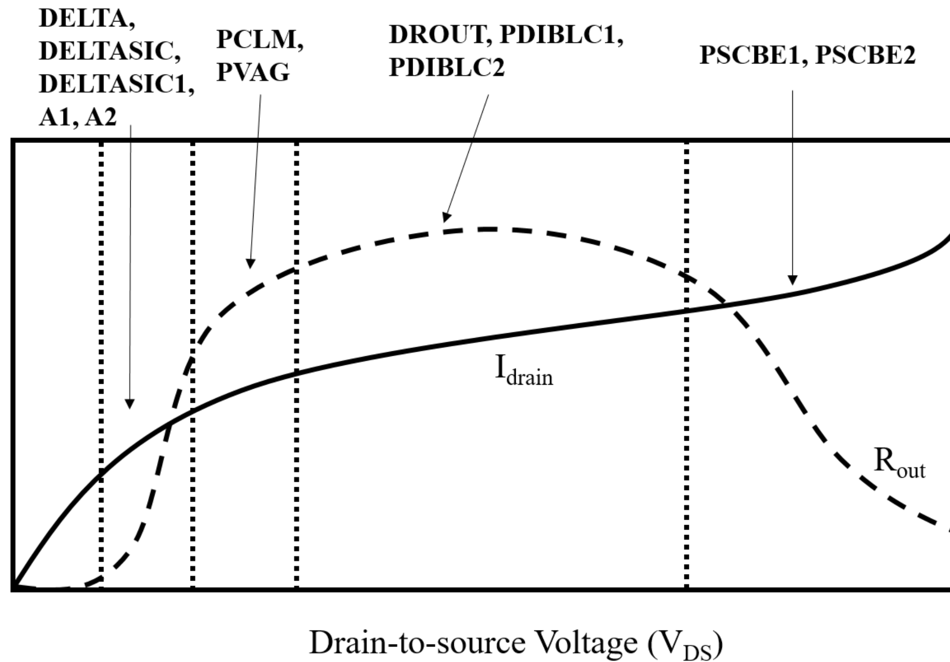


Fig. 7.15. Optimization regions for output conductance related parameters.

Width scaling – Once the model parameters are extracted for a wide device of a particular bin, width scaling parameters can be optimized. The parameters are extracted from the measured data of a narrow device in the same length bin. The extraction sequence is as follows:

Step 1 – The parameters for threshold voltage shift due to narrow width **K3**, **K3B** and **W0** are extracted from the $I_d - V_g$ curves of the narrowest device in the length bin at $V_{ds} = 0.5\ V$. The regions for optimization are illustrated in Fig. 7.16.

Step 2 – The bulk charge coefficient parameters related to narrow width **B0** and **B1** are extracted from the saturation region transfer characteristics ($I_d - V_g$) measured at $V_{ds} = VDD$. The transconductance (g_m - Vg) and output ($I_d - V_d$ and $g_d - V_d$) must be tracked in this step. The optimization region is demonstrated in Fig. 7.17.

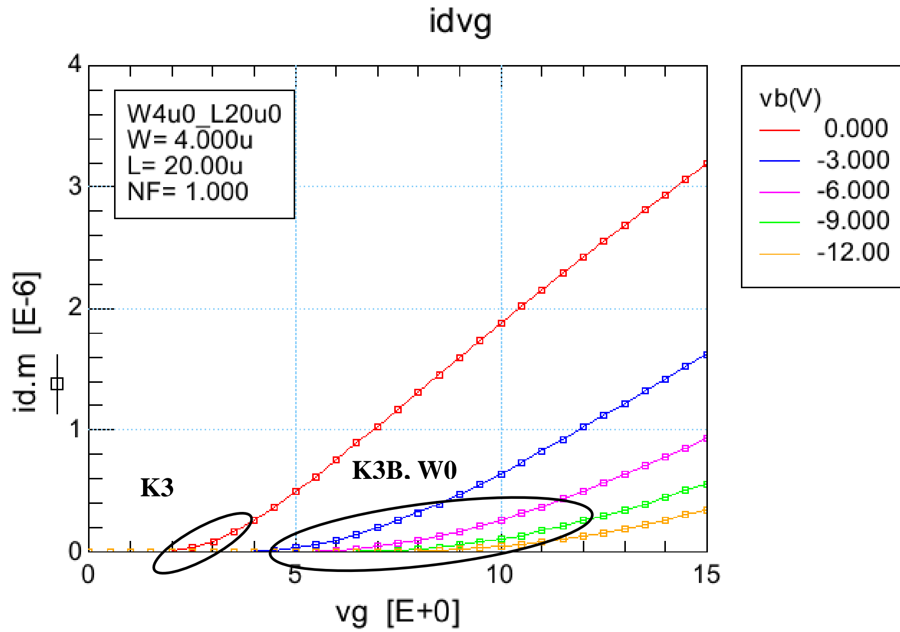


Fig. 7.16. Extraction of the narrow width related threshold voltage shift parameters.

Temperature scaling – After the width scaling is completed, the parameter extraction and optimization of a specific length bin at the room temperature is finalized. The steps described in “MOSFET parameter extraction and optimization” and “width scaling” in this section is repeated for all the remaining temperatures. The parameters tabulated in section 7.4 are usually required to be extracted. Once the parameter values at each temperature is known, the temperature coefficients can be found by a curve fitting tool such as MATLAB *cftool* [162].

Summary of the parameter extraction and optimization process – As explained in Chapter 5, the current measurement at a specific bias condition from the transfer and the output characteristics might be a little different due to the presence of slow interface trapped charge. In this case, the parameters are optimized as such that the simulated characteristics are in between the two measurements. The complete extraction sequence is summarized in Table . A total of six model parameter bins are extracted for geometry scaling both for NMOS and PMOS devices. The summary of the extracted model parameter sets is presented in Table 7.4.

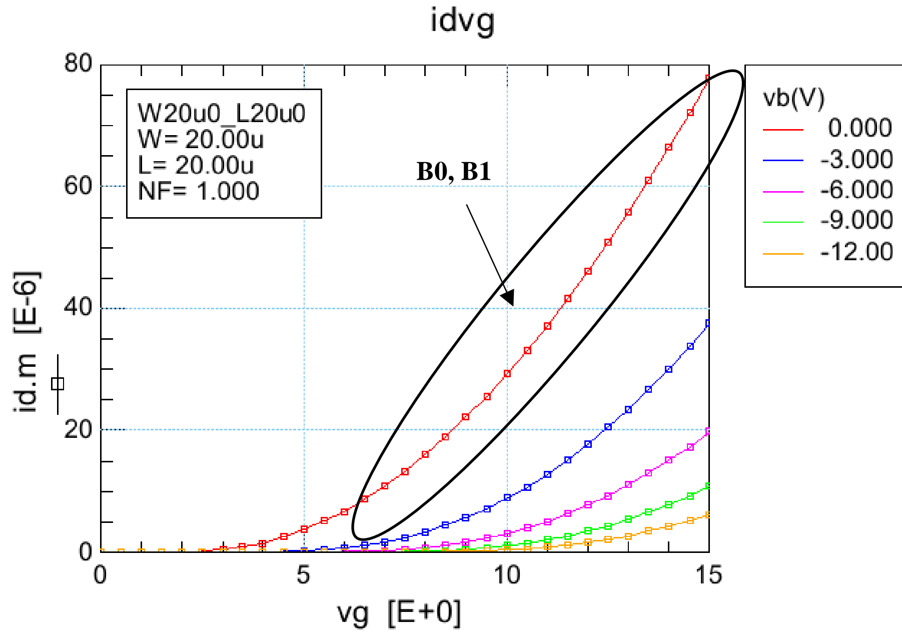


Fig. 7.17. Extraction of width dependent bulk charge coefficient parameters.

Table 7.3. Extraction sequence of the BSIM4SIC model for SiC NMOS and PMOS

Step No.	Parameter Name	Extraction Curves	Extraction Region
1	**CJD (CJS), MJD (MJS), PBD (PBS)**	C_{bd} vs. V_{bd} of high area junction diode	Reverse bias
2	**CJSWD (CJSWS), MJSWD (MJSWS), PBSWD (PBSWS)**	C_{bd} vs. V_{bd} of high periphery junction diode	Reverse bias
3	**NJD (NJS), JSD (JSS)**	Log(I_b) vs. V_{db} of high area junction diode	Forward bias
4	**JSWD (JSWS)**	Log(I_b) vs. V_{db} of high periphery junction diode	Forward bias
5	**IJTHDFWD (IJTHSFWD)**	I_b vs. V_{db} of high area junction diode	Forward bias
6	**TNJDSIC (TNJSSIC)**	Log(I_b) vs. V_{db} of high area and periphery junction diode	Forward bias at different temperatures

Table 7.3. (cont.)

Step No.	Parameter Name	Extraction Curves	Extraction Region
7	**TIJTHDFWDSIC (TIJTHSFWDSIC)**	I_b vs. V_{db} of high area junction diode	Forward bias at different temperatures
8	**EOT**, **TOXE, TOXP, DTOX, ACDE**	C_{ox} vs V_g	Deep accumulation
9	**DELVFBSIC**	C_{gdsb} vs. V_g	Knee in the accumulation
10	**DLC, LINT**	C_{gds} vs. V_g	$V_g = 0$ V
11	**CF**, **CGDO**, **CGSO**	C_{gds} vs. V_g	$V_g = 0$ V
12	**CGD1**, **CGS1, CKAPPAD, CKAPPAS**	C_{gds} vs. V_g	Deep accumulation
13	**WINT, DWC**	$1/R_{DS}$ vs. W_{drawn}	X-axis intercept
14	**VTH0**	I_d vs. V_g at $V_d = 0.5$V and $V_b = 0$V of a wide (20 µm) channel device	Moderate inversion
15	**K1, K2**	I_d vs. V_g at $V_d = 0.5$V and $V_b = -3, -6, -9$ and -12V of a wide (20 µm) channel device	Strong inversion
16	**VOFF**, **NFACTOR**	I_d vs. V_g at $V_d = 0.5$V and $V_b = 0$V of a wide (20 µm) channel device	Subthreshold
17	**DVT1, CDSCB**	I_d vs. V_g at $V_d = 0.5$V and $V_b = -3, -6, -9$ and -12V of a wide (20 µm) channel device	Subthreshold
18	**MINV**	I_d vs. V_g at $V_d = 0.5$V and $V_b = -3, -6, -9$ and -12V of a wide (20 µm) channel device	Moderate inversion
19	**U0**, **UA**, **UD**, **UCS**	I_d vs. V_g at $V_d = 0.5$V and $V_b = 0$V of a wide (20 µm) channel device	Strong inversion
20	**UDSIC, UCSSIC, UCSSIC1, UC**	I_d vs. V_g at $V_d = 0.5$V and $V_b = -3, -6, -9$V and -12V of a wide (20 µm) channel device	Strong inversion

Table 7.3. (cont.)

Step No.	Parameter Name	Extraction Curves	Extraction Region
21	**CDSCD**	I_d vs. V_g at V_d = VDD and V_b = 0V of a wide (20 µm) channel device	Subthreshold
22	**DSUB, ETA0**	I_d vs. V_g at V_d = VDD and V_b = 0V of a wide (20 µm) channel device	Moderate inversion
23	**ETAB**	I_d vs. V_g at V_d = VDD and V_b = -3, -6, -9 and -12V of a wide (20 µm) channel device	Moderate inversion
24	**A0, AGS, RDSW, RDSWMIN, PRWG**	I_d vs. V_g at V_d = VDD and V_b = 0V of a wide (20 µm) channel device	Strong inversion
25	**KETA, KETASIC**	I_d vs. V_g at V_d = VDD and V_b = -3, -6, -9 and -12V of a wide (20 µm) channel device	Strong inversion
26	**VSAT, DELTA, DELASIC, DELTASIC1, A1, A2**	I_d vs. V_d at V_g = 3, 5, 7, 9, 11, 13, 15V and V_b = 0V of a wide (20 µm) channel device	Transition from linear to saturation
27	**PCLM, PVAG**	I_d vs. V_d at V_g = 3, 5, 7, 9, 11, 13, 15V and V_b = 0V of a wide (20 µm) channel device	Few volts of the drain voltage beyond the beginning of the saturation region
28	**DROUT, PDIBLC1, PDIBLC2**	I_d vs. V_d at V_g = 3, 5, 7, 9, 11, 13, 15V and V_b = 0V of a wide (20 µm) channel device	Few volts of the drain voltage beyond the region as indicated in the last step
29	**PSCBE1, PSCBE2**	I_d vs. V_d at V_g = 3, 5, 7, 9, 11, 13, 15V and V_b = 0V of a wide (20 µm) channel device	Saturation region near V_d = VDD

Table 7.3 (cont.)

Step No.	Parameter Name	Extraction Curves	Extraction Region
30	**K1CVSIC**	C_{gdsb} vs. V_g	At the plateau
	VOFFCV, NOFF	C_{gdsb} vs. V_g	Transition from depletion to strong inversion
31	**MOIN**	C_{gdsb} vs. V_g	Moderate inversion
32	**K3, W0**	I_d vs. V_g at V_d = 0.5V and V_b = 0V of a narrow (4 µm) channel device	Moderate inversion
33	**K3B**	I_d vs. V_g at V_d = 0.5V and V_b = -3, -6, -9 and -12V of a narrow (4 µm) channel device	Moderate inversion
34	**B0, B1**	I_d vs. V_g at V_d = VDD and V_b = 0V of a narrow (4 µm) channel device	Strong inversion
35	**Temperature scaled parameters**	Follow steps 14 to 34 for the remaining temperatures	
36	**Temperature coefficients**	Find temperature coefficients from the temperature scaled parameters using MATLAB cftool	

Table 7.4. Description of the length bins extracted for SiC NMOS and PMOS

Wmin (µm)	Wmax (µm)	Lmin (µm)	Lmax (µm)	Devices used for model verification	Temp Scaled (Range: 25C – 300 ^{0}C)	Corners
4	60	1.2	1.4	20/1.2 4/1.2	Yes	Fast NMOS and Slow PMOS
4	60	1.41	1.6	20/1.5 4/1.5	Yes	Fast NMOS and Slow PMOS
4	60	1.61	3.6	20/2 4/2	Yes	Fast NMOS and Slow PMOS
4	60	3.61	7.2	20/5	Yes	Fast NMOS and Slow PMOS

Table 7.4 (cont.)

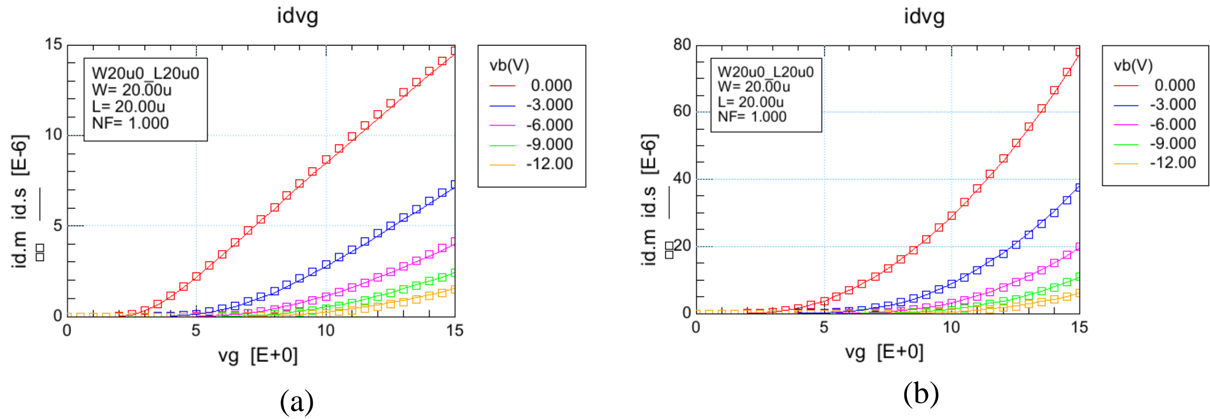
Wmin (µm)	Wmax (µm)	Lmin (µm)	Lmax (µm)	Devices used for model verification	Temp Scaled (Range: 25C – 300 °C)	Corners
4	60	14.41	20	20/20 4/20	Yes	Fast NMOS and Slow PMOS
4	60	7.21	14.4	20/10 4/10	Yes	Fast NMOS and Slow PMOS

The process information of the characterized devices is:

Devices: NMOS and PMOS
Fabrication Run: Vulcan II
Wafer No. 36
Die Location: Row 4, Column 2

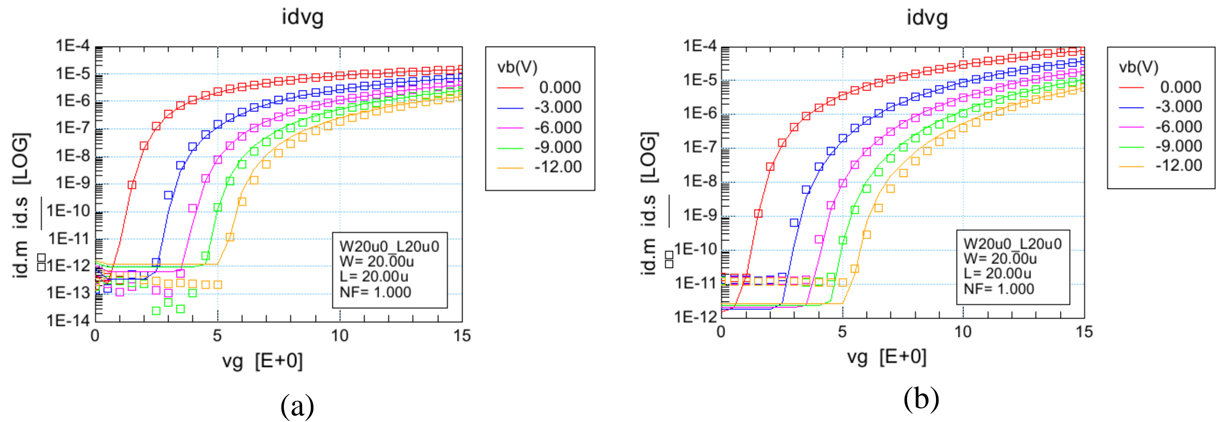
7.7 Model Optimization Results

The optimization results in this section are presented to validate the model performance over geometry and temperature in all the operating conditions. The DC characteristics of NMOS and PMOS are presented first followed by gate C-V and diode characteristics. The DC characteristics include subthreshold and strong inversion operations both in linear and saturation region. The DC plots are presented for 20µm/20µm (wide and long), 4µm/20µm (narrow and long), 20µm/2µm (typical analog), 20µm/1.2µm (wide and short) and 4µm/1.2µm (narrow and short) NMOS and PMOS devices at 25 and 300 ° C.



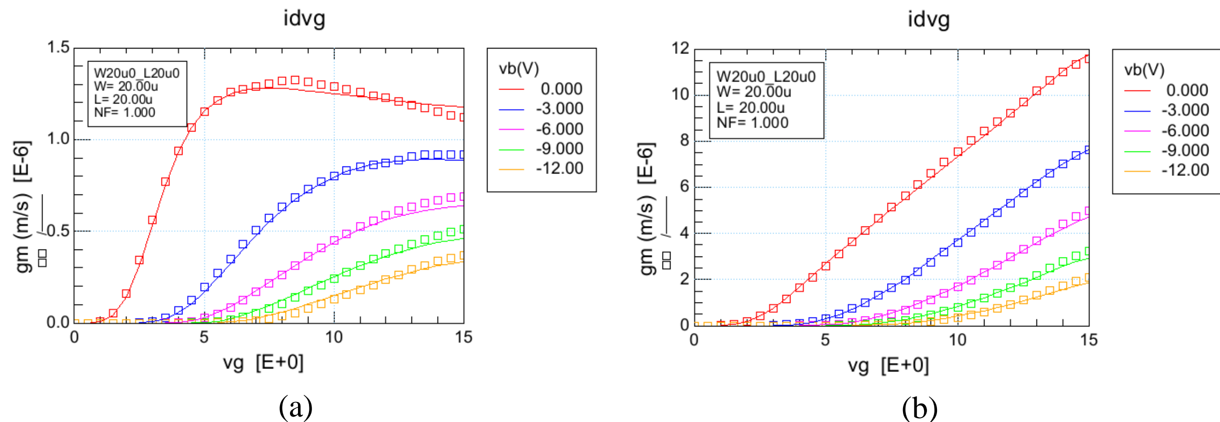
(a) (b)

Fig. 7.18. Transfer characteristics of a 20 µm / 20 µm (wide and long) NMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.19. Transfer characteristics of a 20 µm / 20 µm (wide and long) NMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.20. Transconductance of a 20 µm / 20 µm (wide and long) NMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

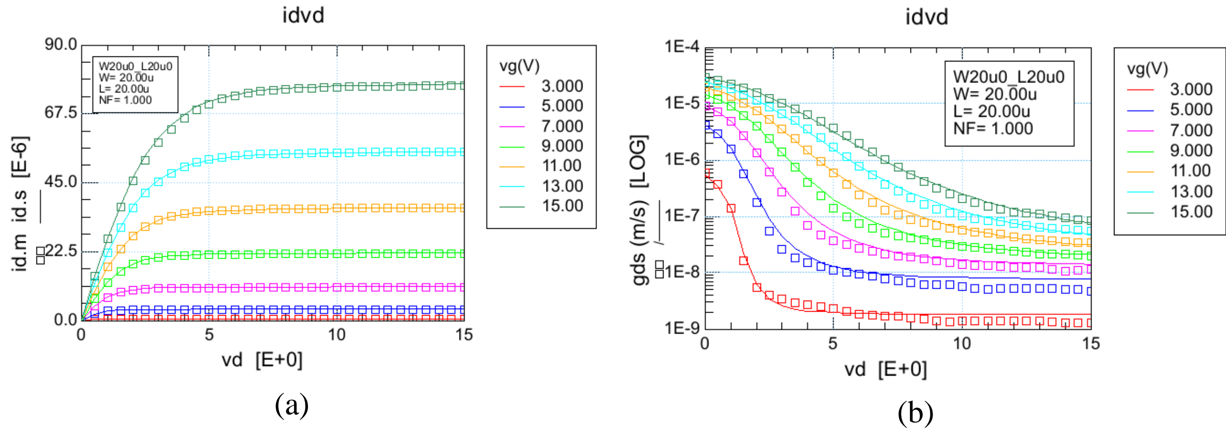


Fig. 7.21. (a) Output characteristics and (b) output conductance of a 20 µm / 20 µm (wide and long) NMOS at 25 ° C.

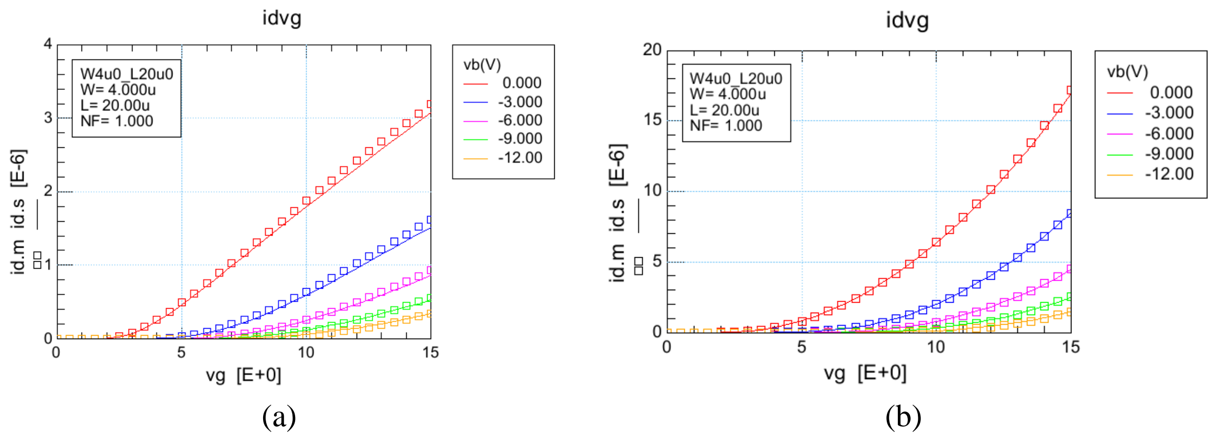


Fig. 7.22. Transfer characteristics of a 4 µm / 20 µm (narrow and long) NMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

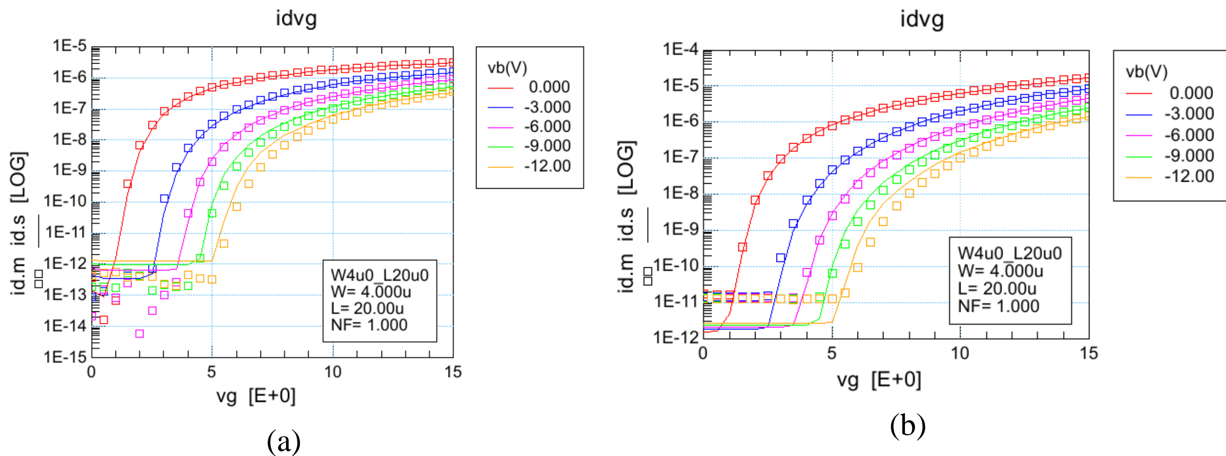
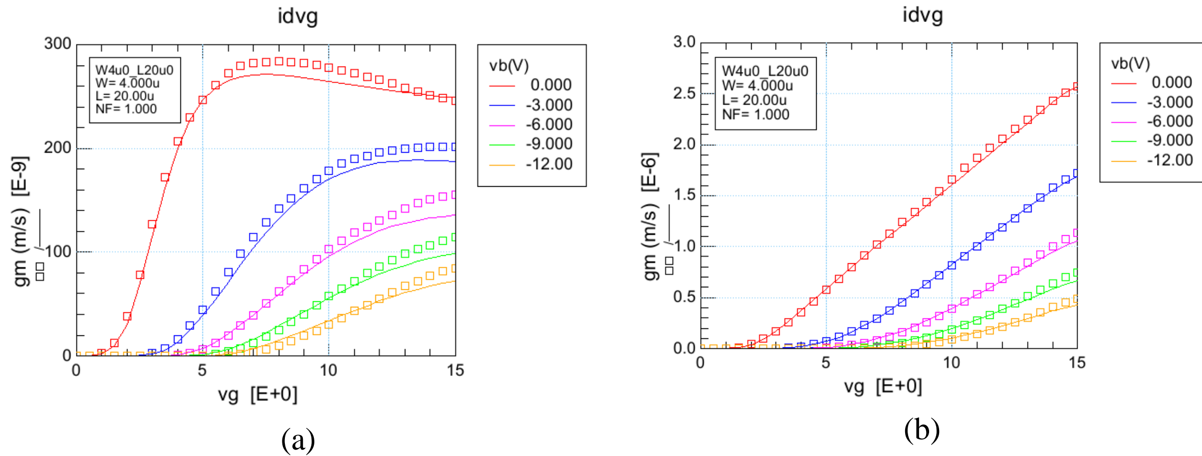
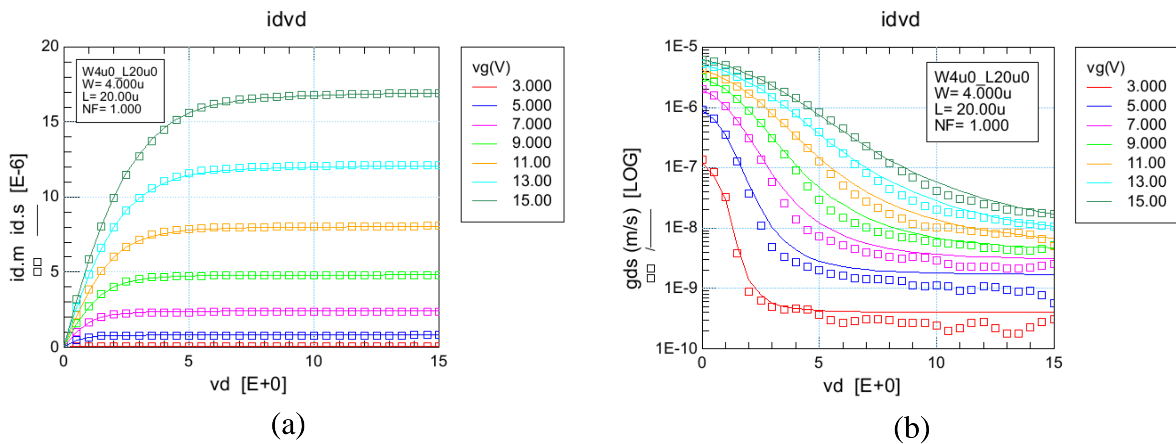


Fig. 7.23. Transfer characteristics of a 4 µm / 20 µm (narrow and long) NMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



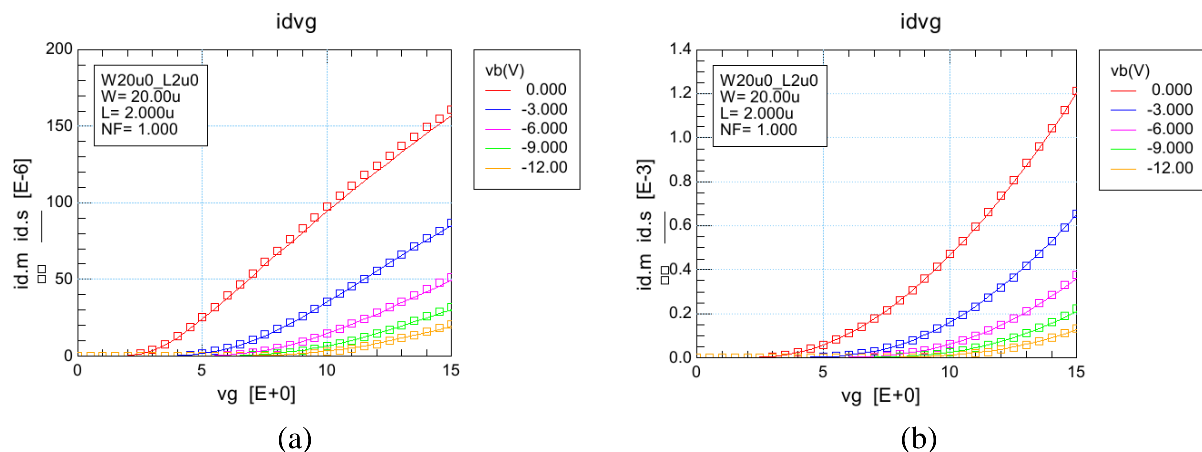
(a) (b)

Fig. 7.24. Transconductance of a 4 µm / 20 µm (narrow and long) NMOS at 25 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.25. (a) Output characteristics and (b) output conductance of a 4 µm / 20 µm (narrow and long) NMOS at 25 ⁰ C.



(a) (b)

Fig. 7.26. Transfer characteristics of a 20 µm / 2 µm (typical analog device) NMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

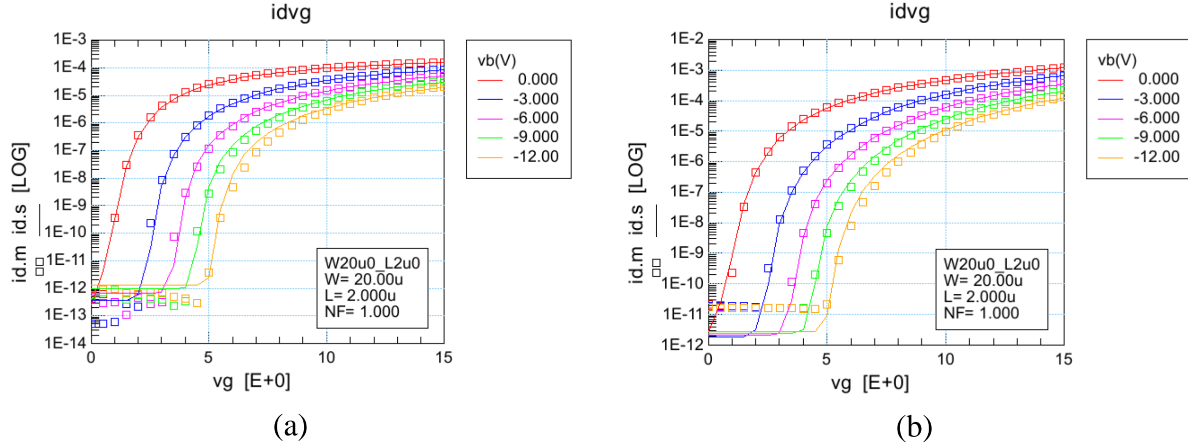


Fig. 7.27. Transfer characteristics of a 20 µm / 2 µm (typical analog device) NMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

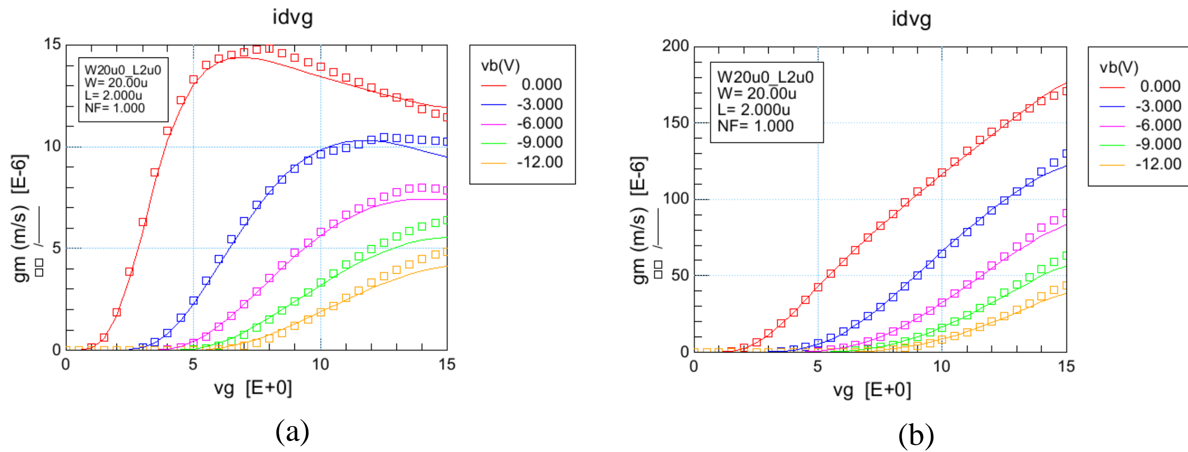


Fig. 7.28. Transconductance of a 20 µm / 2 µm (typical analog device) NMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

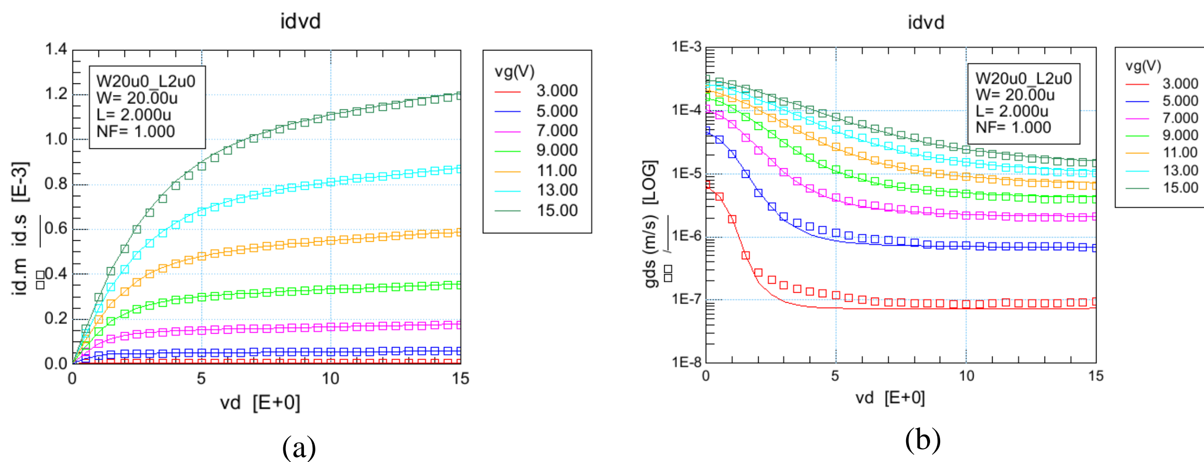


Fig. 7.29. (a) Output characteristics and (b) output conductance of a 20 µm / 2 µm (typical analog device) NMOS at 25 ° C.

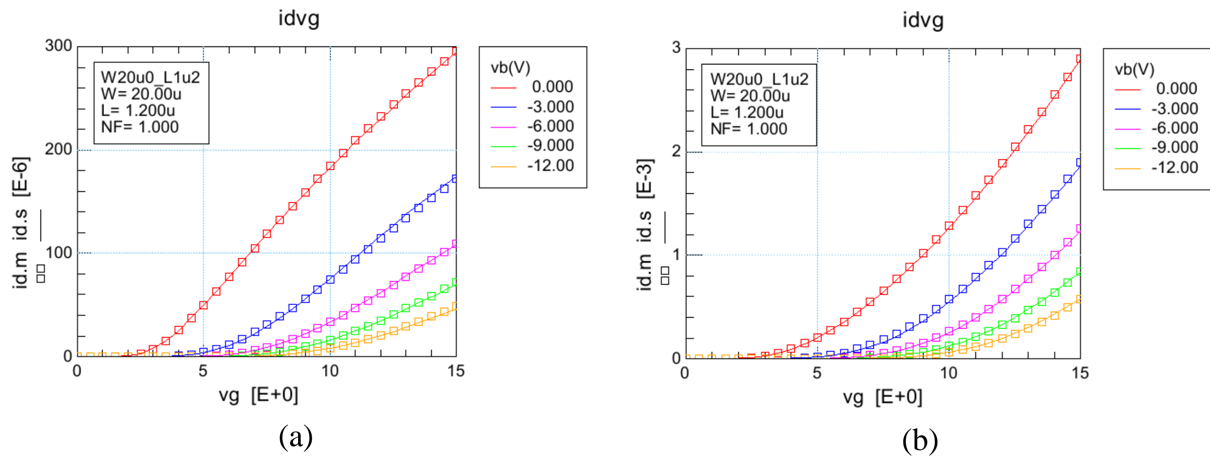


Fig. 7.30. Transfer characteristics of a 20 μm × 1.2 μm (wide and short) NMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

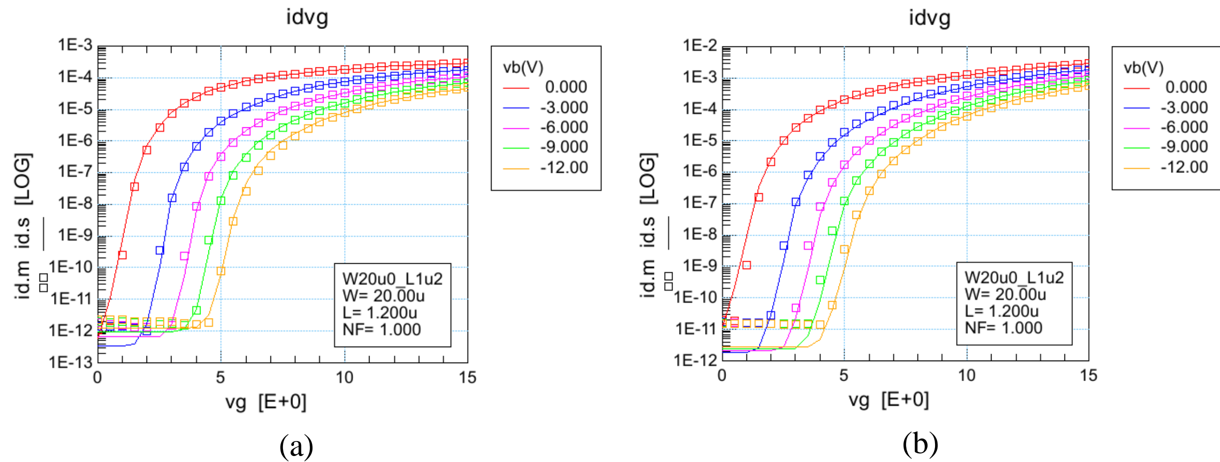


Fig. 7.31. Transfer characteristics of a 20 μm × 1.2 μm (wide and short) NMOS at 25 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

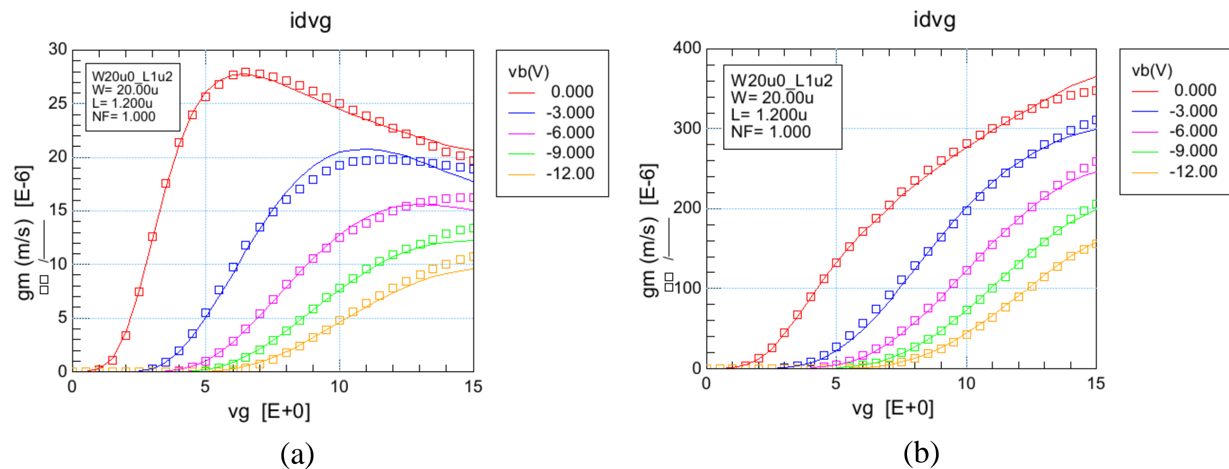
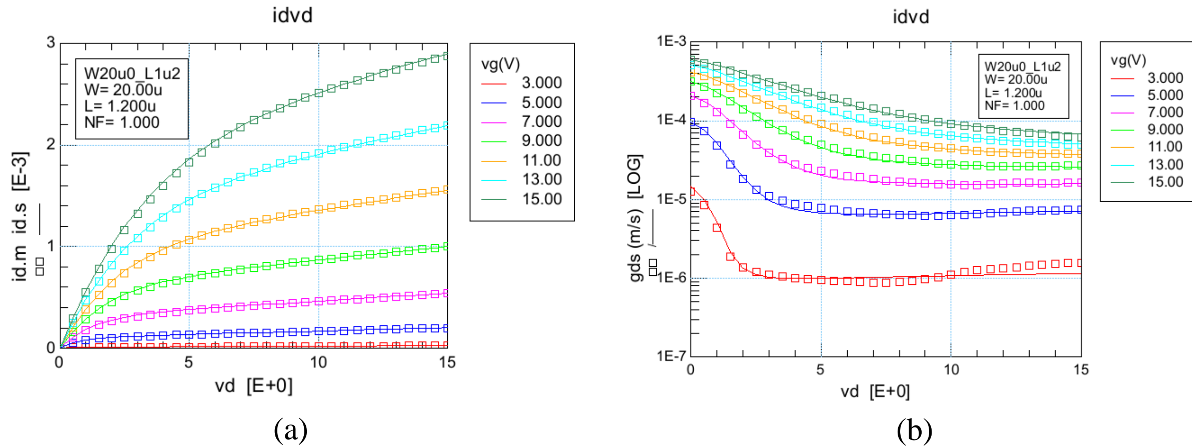
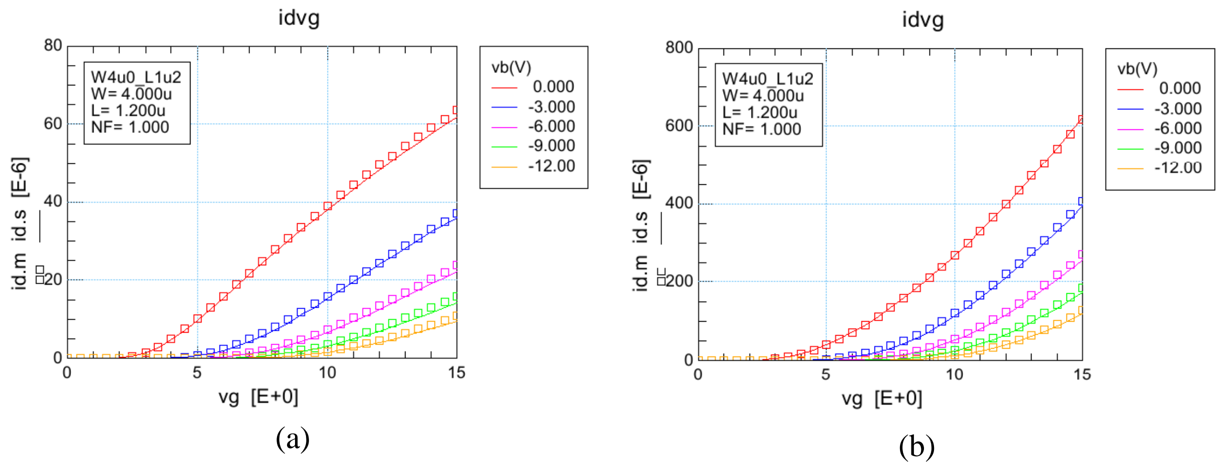


Fig. 7.32. Transconductance of a 20 μm / 1.2 μm (wide and short) NMOS at 25 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



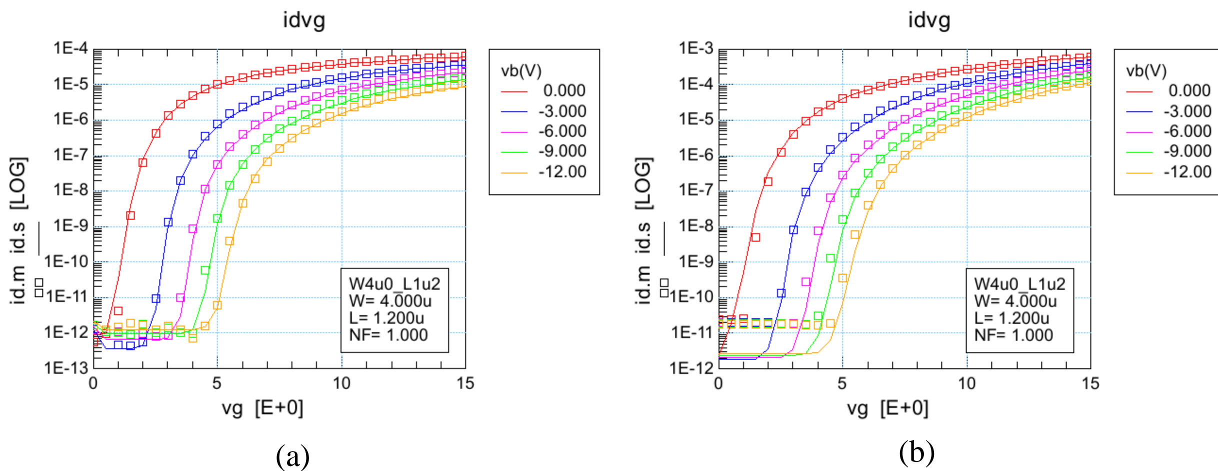
(a) (b)

Fig. 7.33. (a) Output characteristics and (b) output conductance of a 20 µm / 1.2 µm (wide and short) NMOS at 25 ° C.



(a) (b)

Fig. 7.34. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.35. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

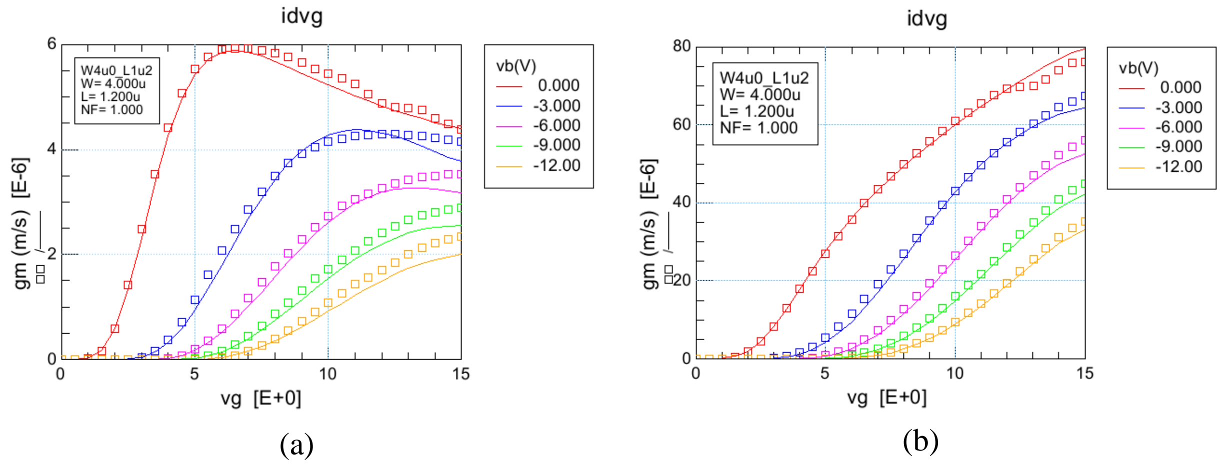


Fig. 7.36. Transconductance of a 4 μm / 1.2 μm (narrow and short) NMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

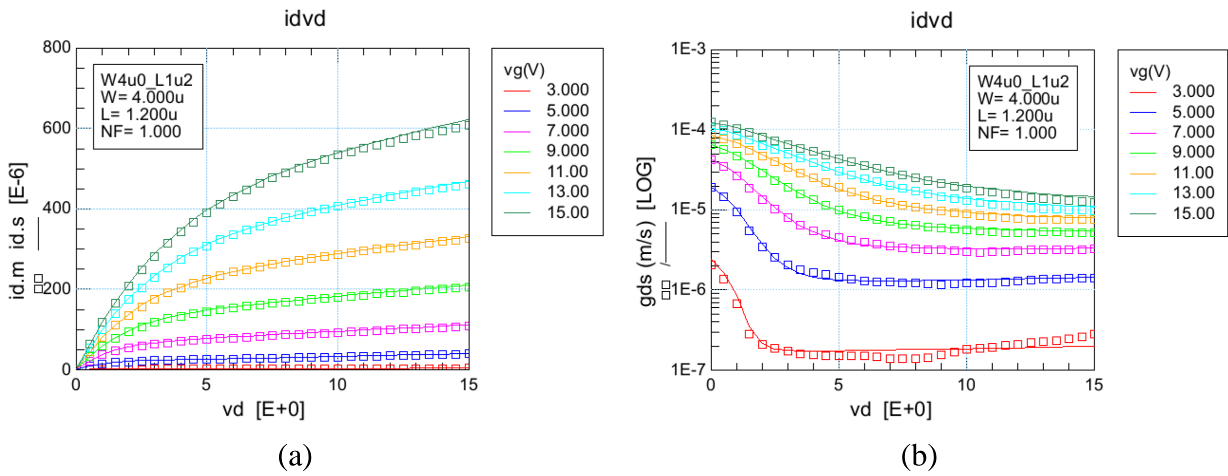


Fig. 7.37. (a) Output characteristics and (b) output conductance of a 4 μm / 1.2 μm (narrow and short) NMOS at 25 ° C.

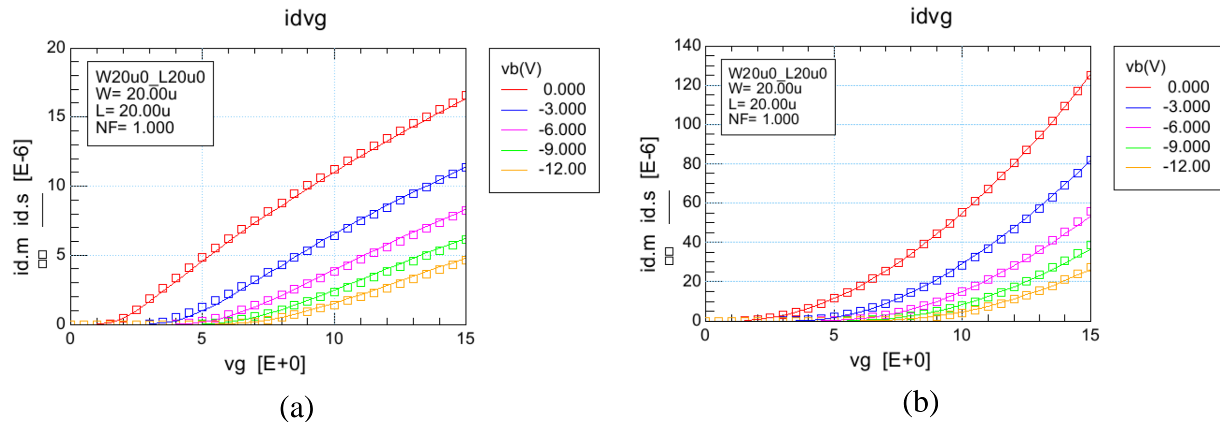


Fig. 7.38. Transfer characteristics of a 20 μm / 20 μm (wide and long) NMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

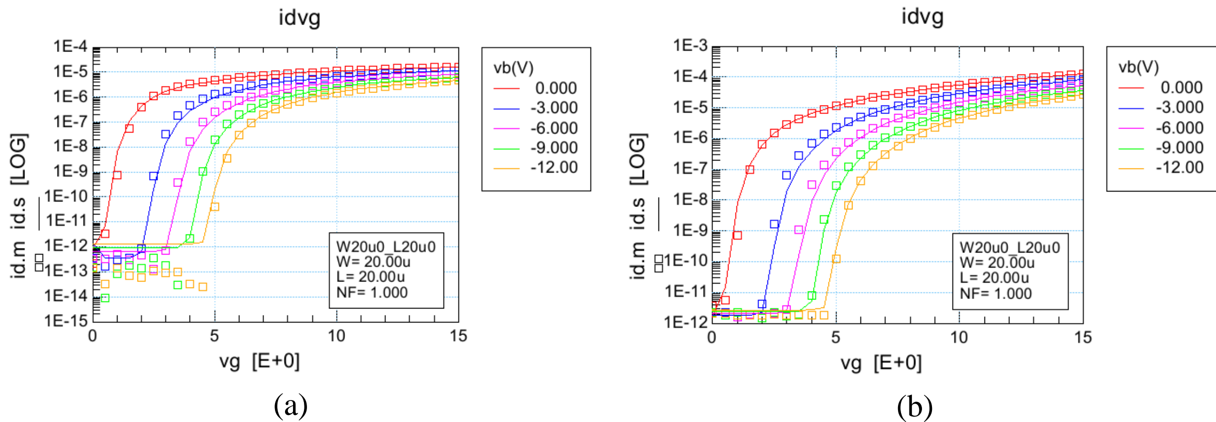


Fig. 7.39. Transfer characteristics of a 20 μm / 20 μm (wide and long) NMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

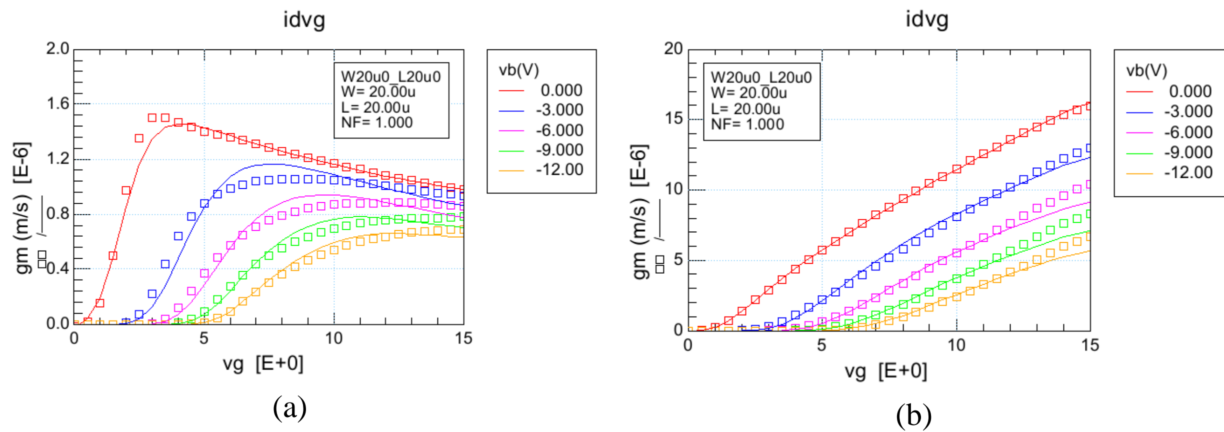


Fig. 7.40. Transconductance of a 20 μm / 20 μm (wide and long) NMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

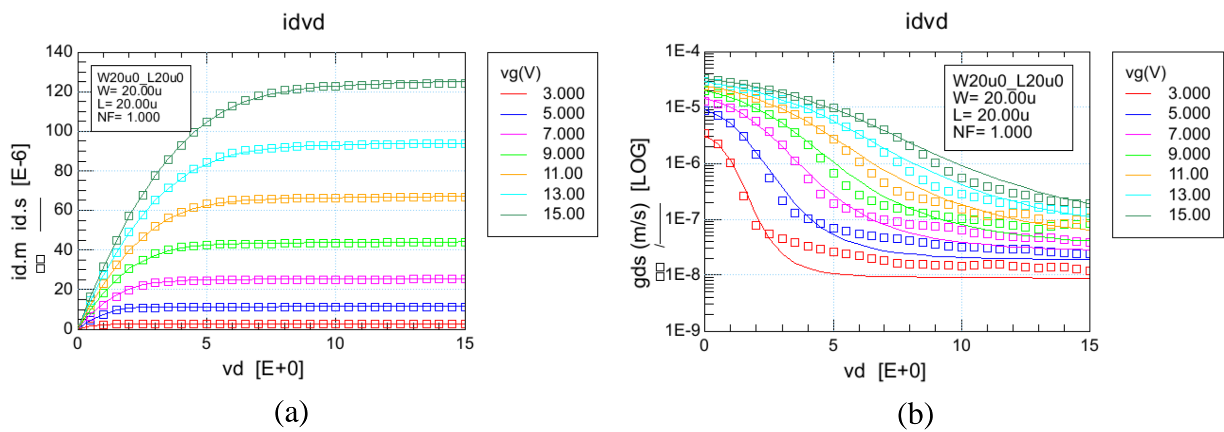
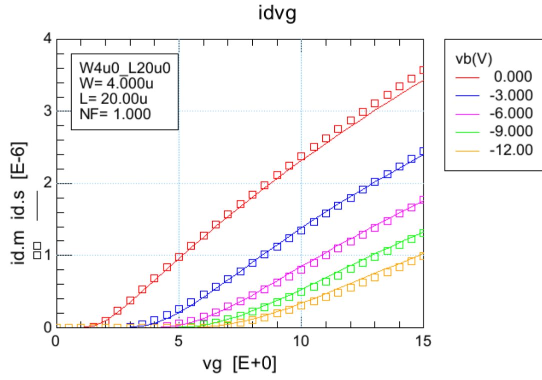
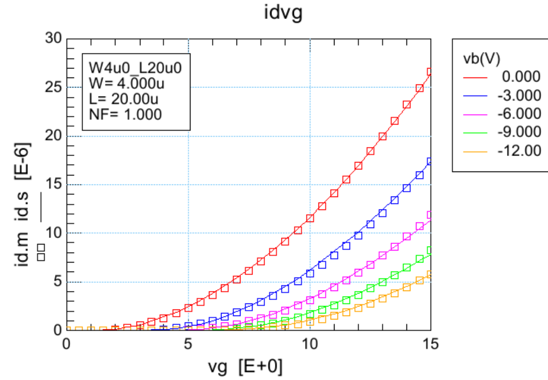


Fig. 7.41. (a) Output characteristics and (b) output conductance of a 20 μm / 20 μm (wide and long) NMOS at 300 ⁰ C.

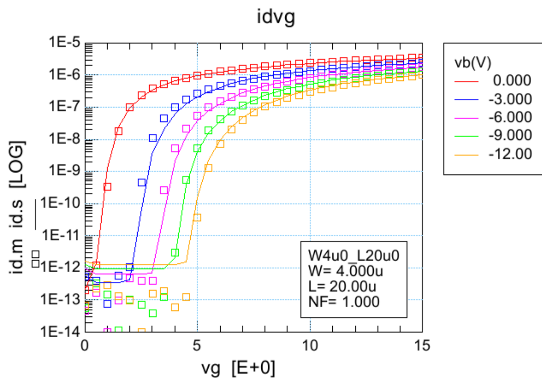


(a)

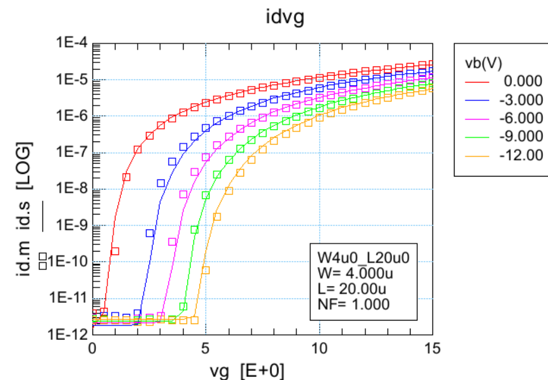


(b)

Fig. 7.42. Transfer characteristics of a 4 µm / 20 µm (narrow and long) NMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

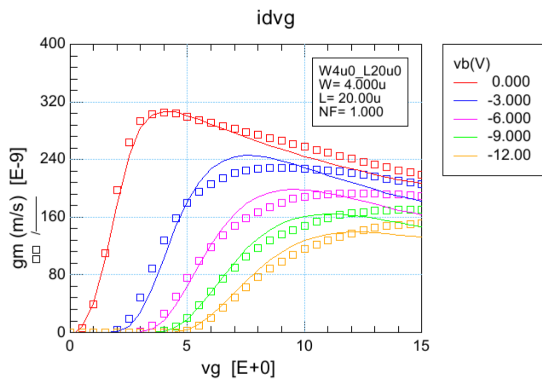


(a)

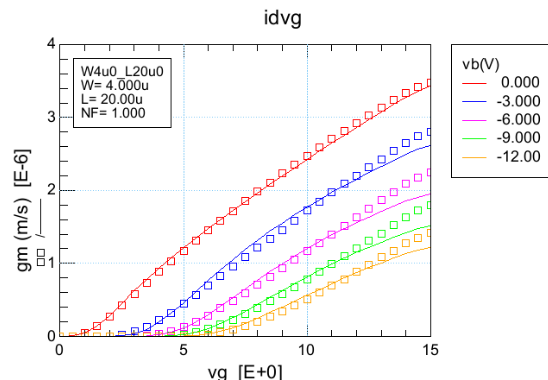


(b)

Fig. 7.43. Transfer characteristics of a 4 µm / 20 µm (narrow and long) NMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

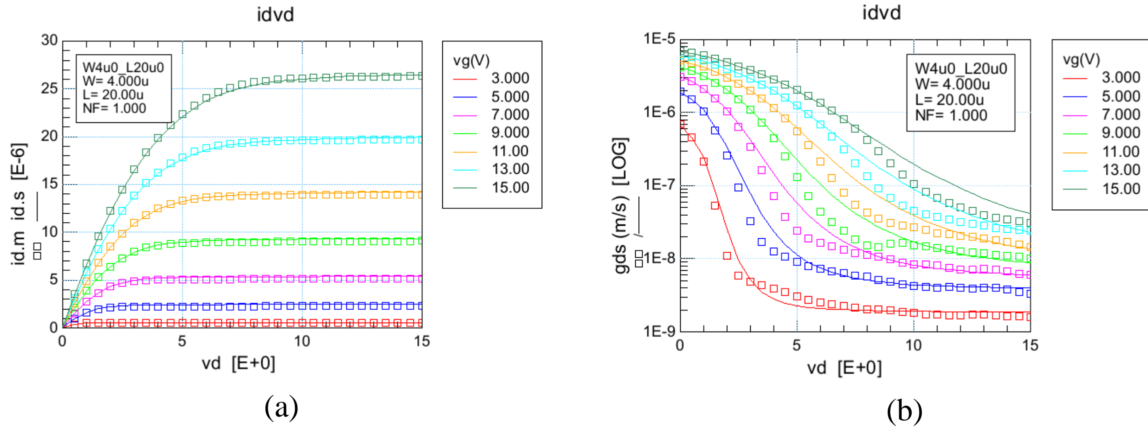


(a)



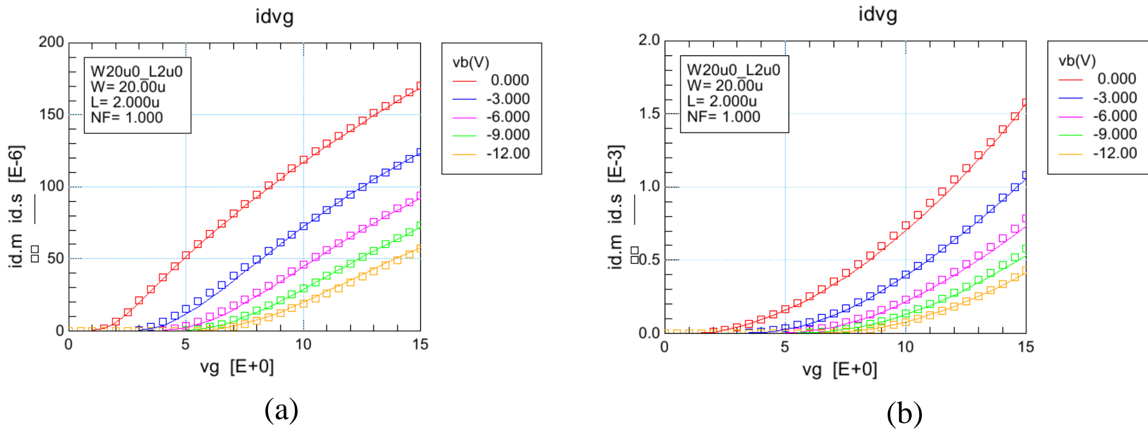
(b)

Fig. 7.44. Transconductance of a 4 µm / 20 µm (narrow and long) NMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



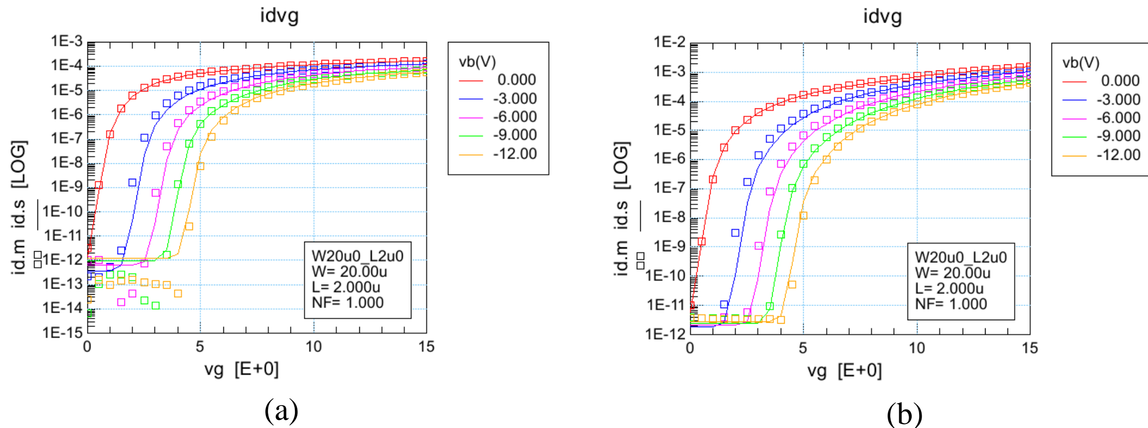
(a) (b)

Fig. 7.45. (a) Output characteristics and (b) output conductance of a 4 µm / 20 µm (narrow and long) NMOS at 300 ⁰ C.



(a) (b)

Fig. 7.46. Transfer characteristics of a 20 µm / 2 µm (typical analog device) NMOS at 300 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.47. Transfer characteristics of a 20 µm / 2 µm (typical analog device) NMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

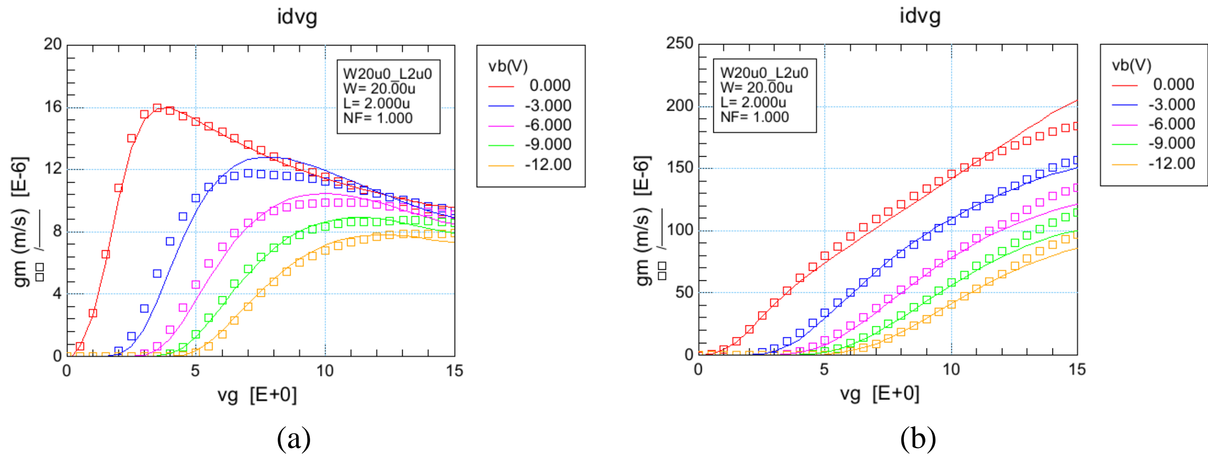


Fig. 7.48. Transconductance of a 20 µm / 2 µm (typical analog device) NMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

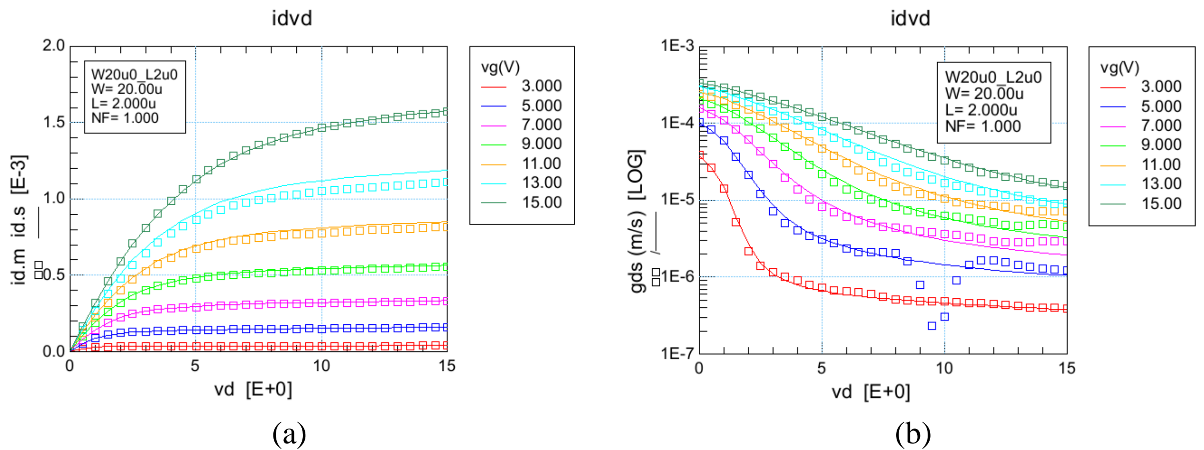


Fig. 7.49. (a) Output characteristics and (b) output conductance of a 20 µm / 2 µm (typical analog device) NMOS at 300 ° C.

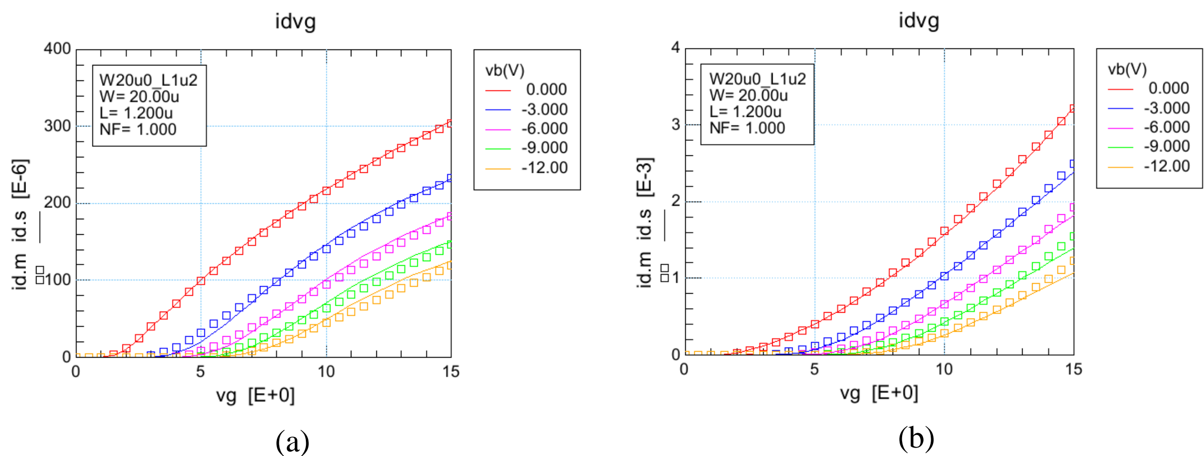


Fig. 7.50. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

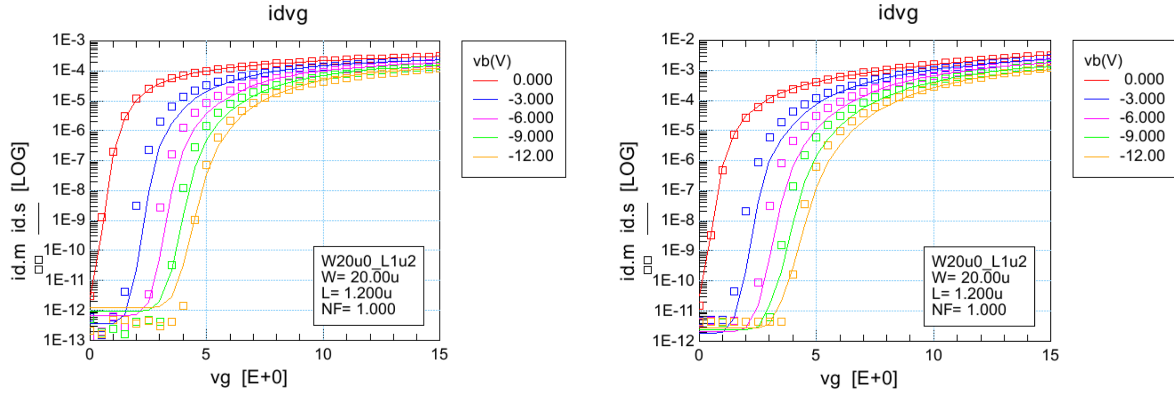


Fig. 7.51. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

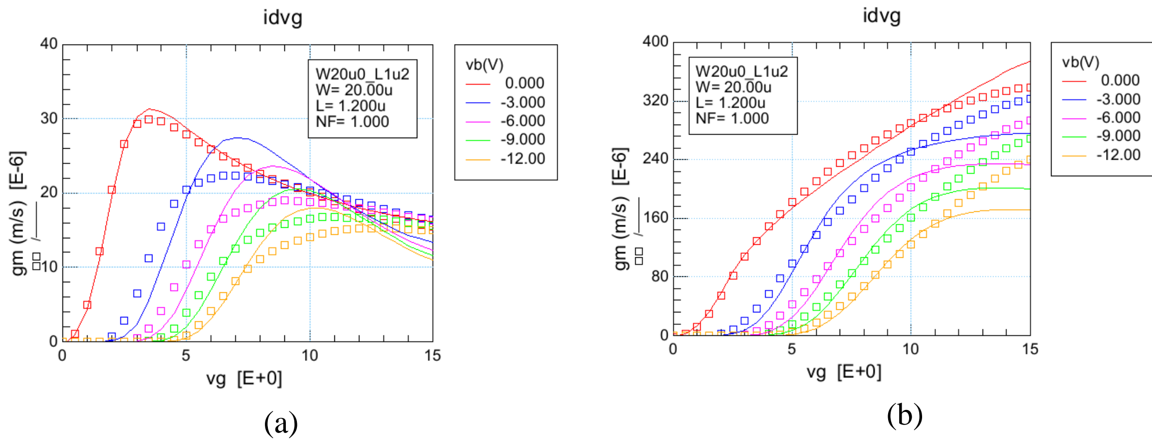


Fig. 7.52. Transconductance of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

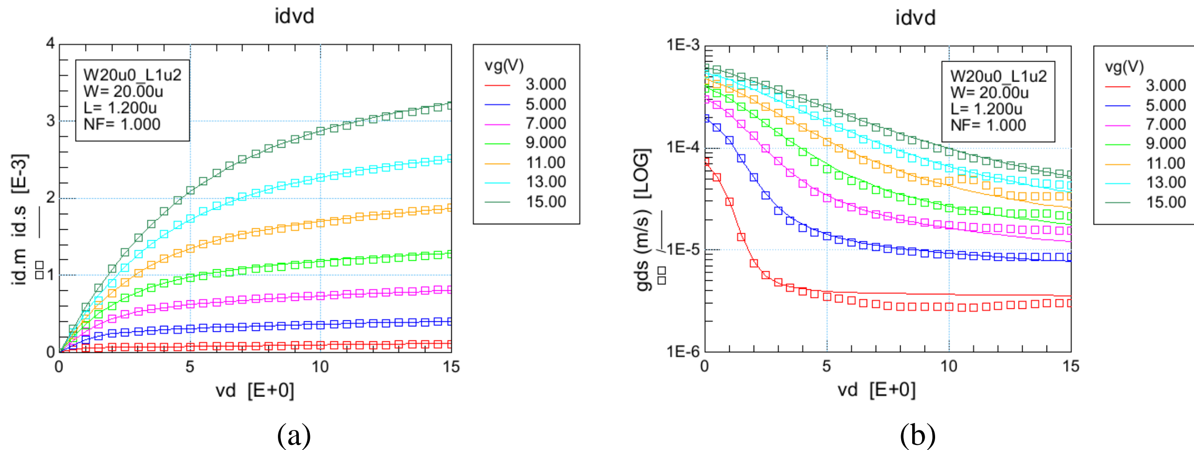


Fig. 7.53. (a) Output characteristics and (b) output conductance of a 20 µm / 1.2 µm (wide and short) NMOS at 300 ⁰ C.

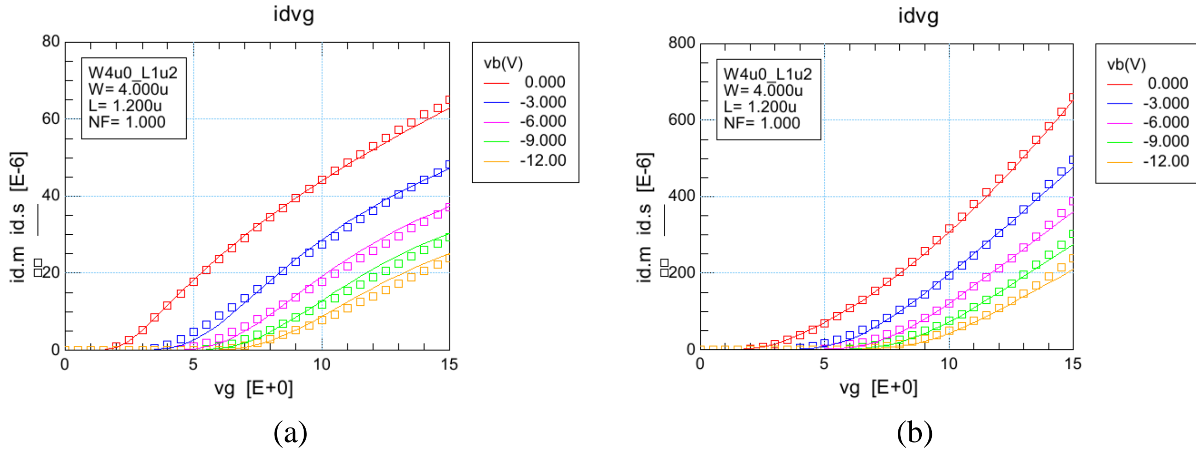


Fig. 7.54. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

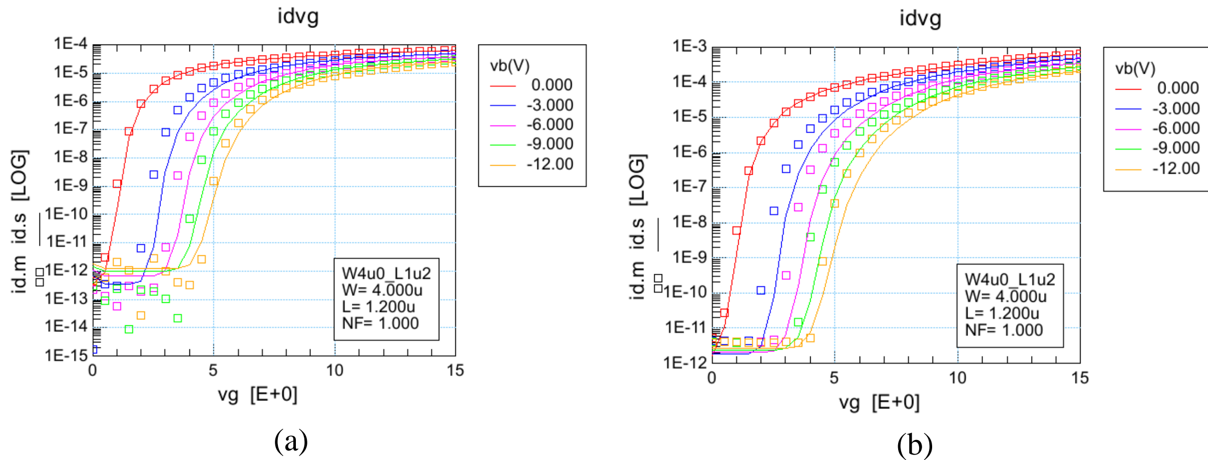


Fig. 7.55. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) NMOS at 300 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

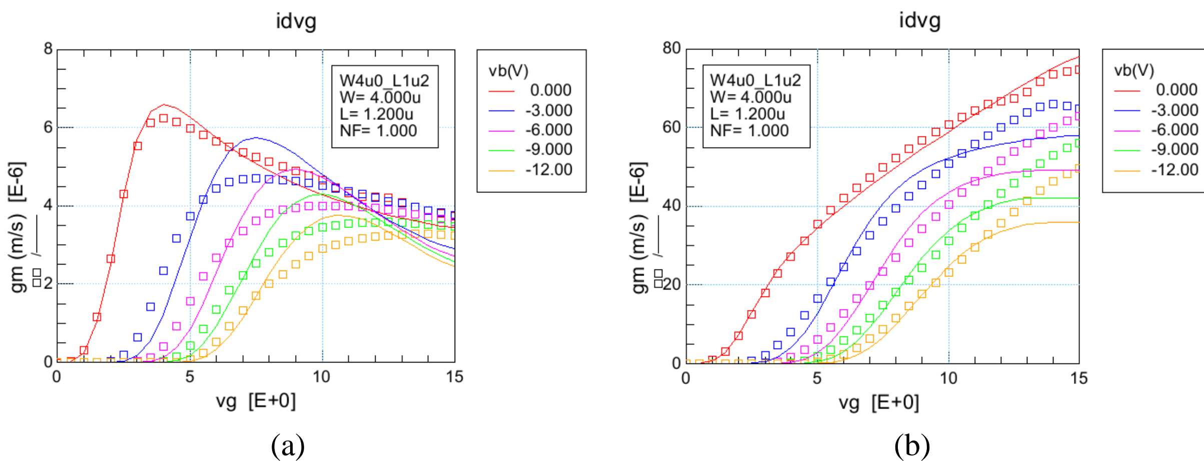
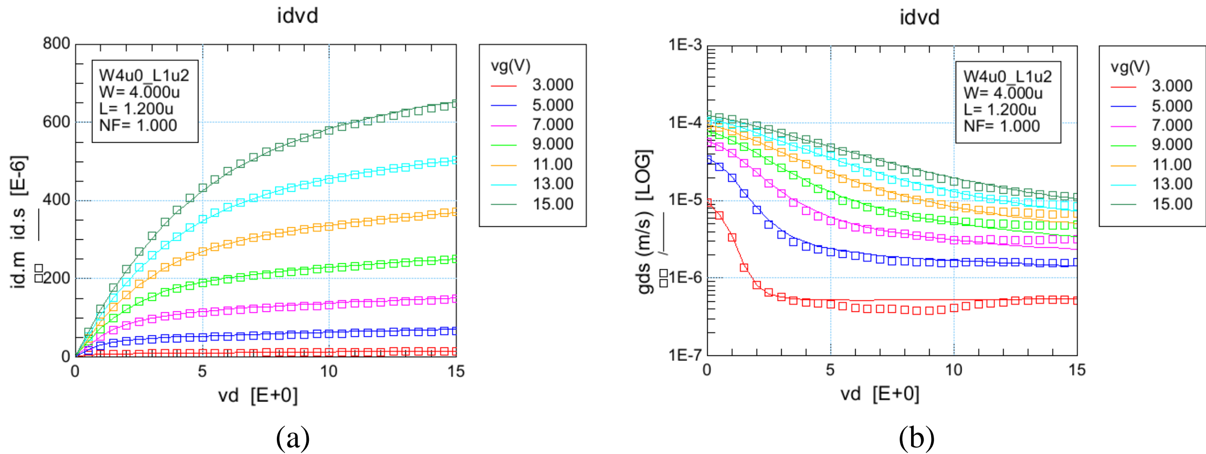
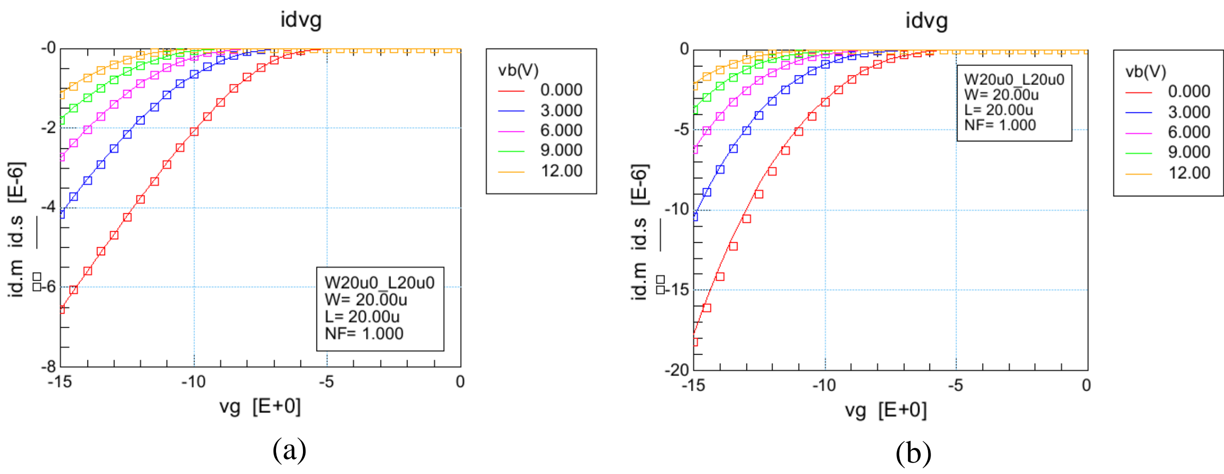


Fig. 7.56. Transconductance of a 4 µm / 1.2 µm (narrow and short) NMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



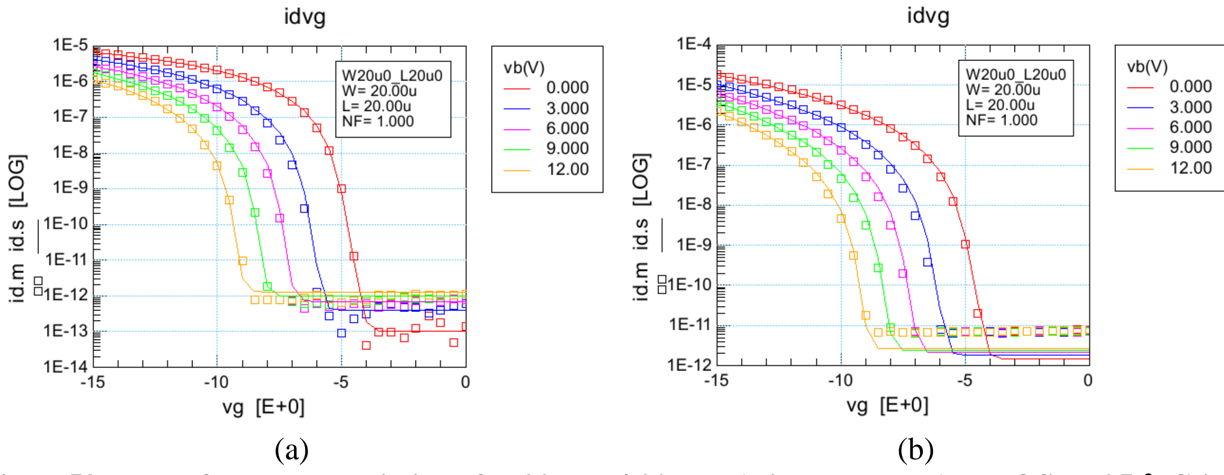
(a) (b)

Fig. 7.57. (a) Output characteristics and (b) output conductance of a 4 μm / 1.2 μm (narrow and short) NMOS at 300 ° C.



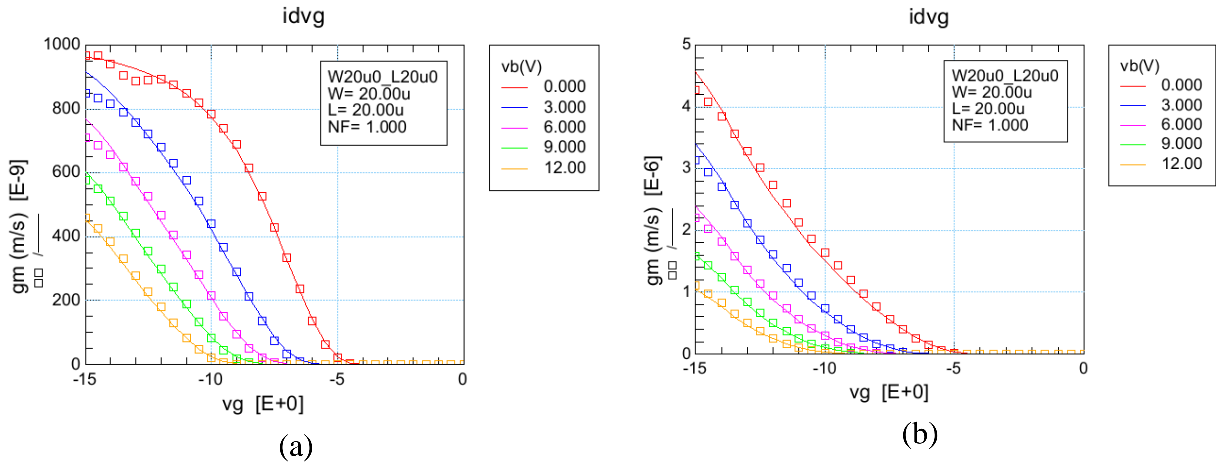
(a) (b)

Fig. 7.58. Transfer characteristics of a 20 μm / 20 μm (wide and long) PMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



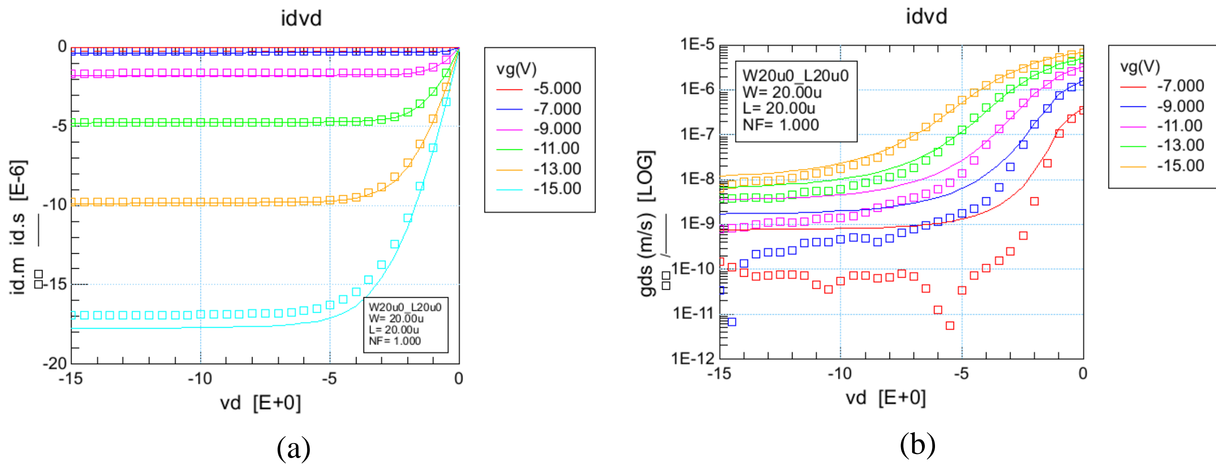
(a) (b)

Fig. 7.59. Transfer characteristics of a 20 μm / 20 μm (wide and long) PMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



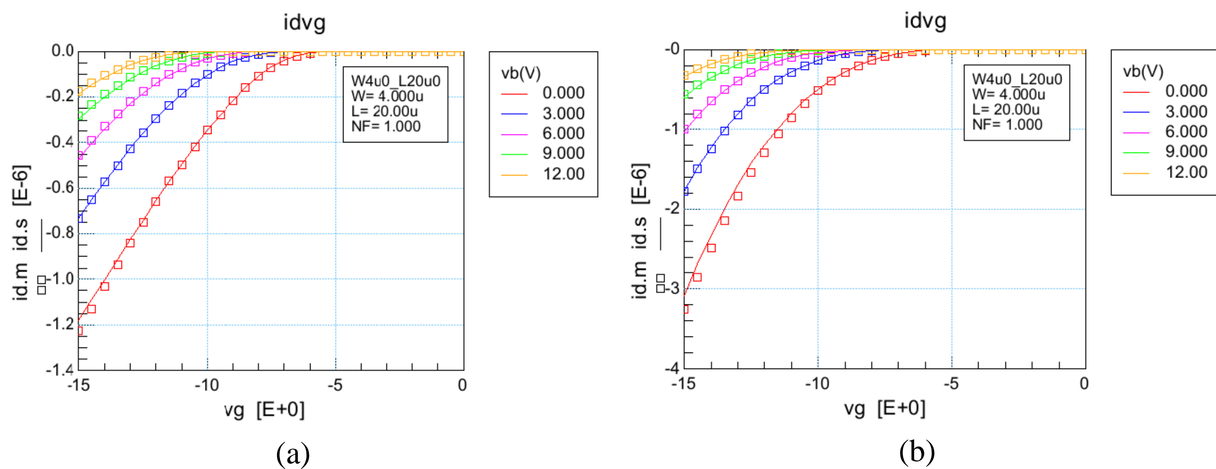
(a) (b)

Fig. 7.60. Transconductance of a 20 µm / 20 µm (wide and long) PMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.61. (a) Output characteristics and (b) output conductance of a 20 µm / 20 µm (wide and long) PMOS at 25 ° C.



(a) (b)

Fig. 7.62. Transfer characteristics of a 4 µm / 20 µm (narrow and long) PMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

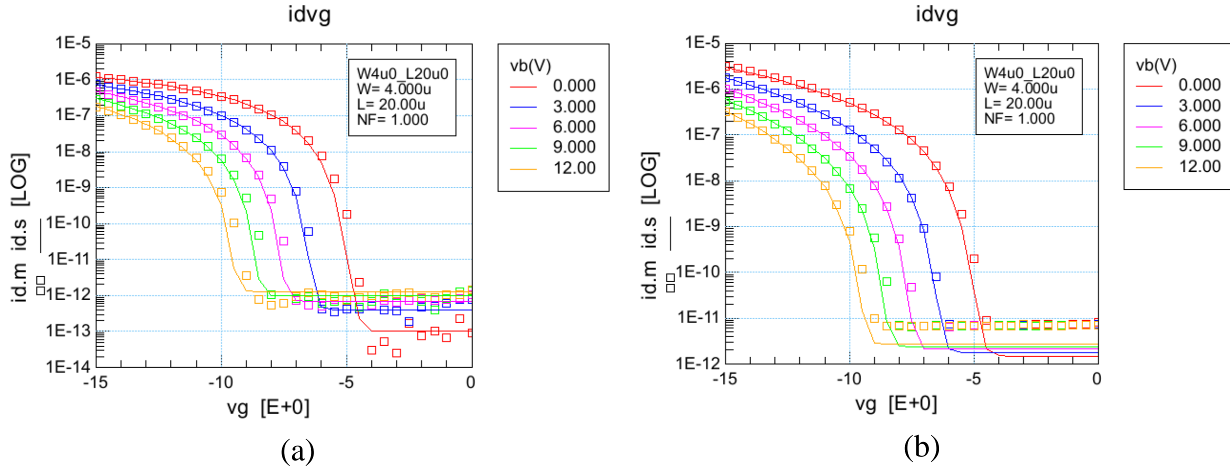


Fig. 7.63. Transfer characteristics of a 4 µm / 20 µm (narrow and long) PMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

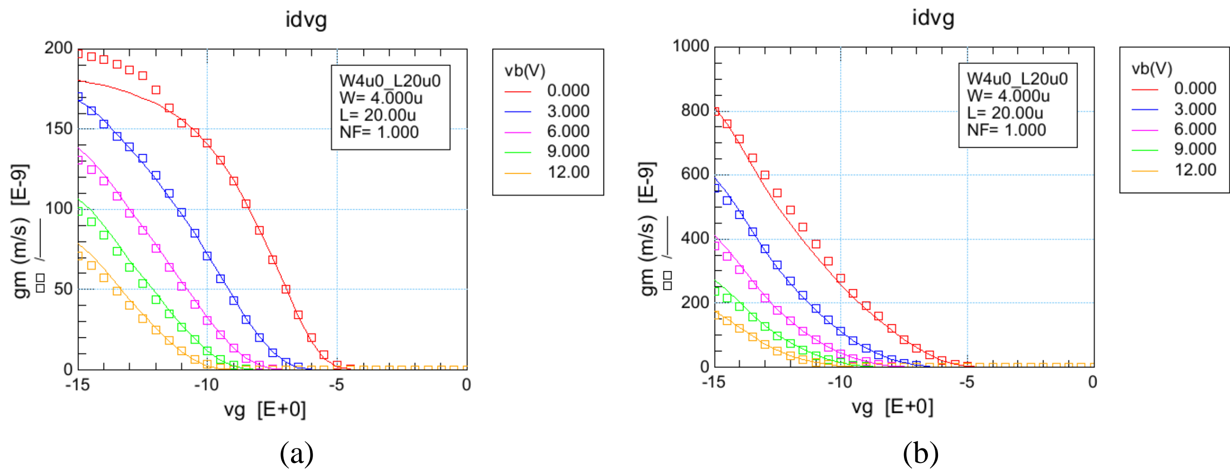


Fig. 7.64. Transconductance of a 4 µm / 20 µm (narrow and long) PMOS at 25 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

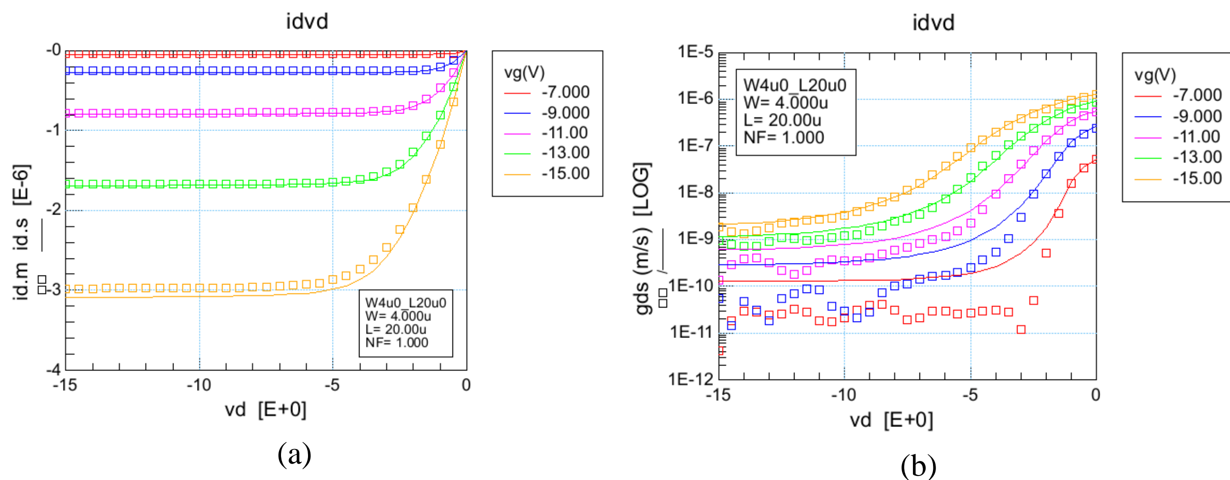


Fig. 7.65. (a) Output characteristics and (b) output conductance of a 4 µm / 20 µm (narrow and long) PMOS at 25 ° C.

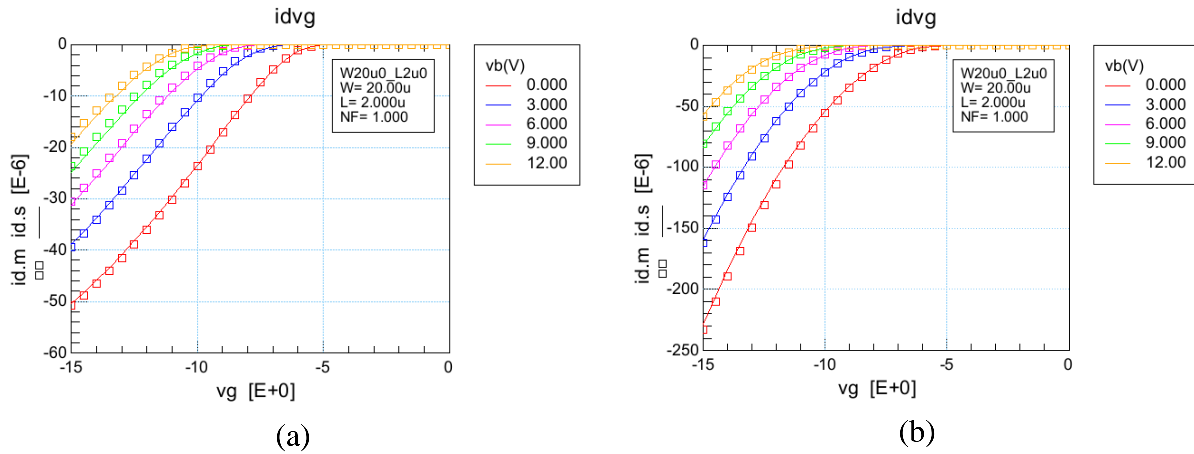


Fig. 7.66. Transfer characteristics of a 20 µm / 2 µm (typical analog device) PMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

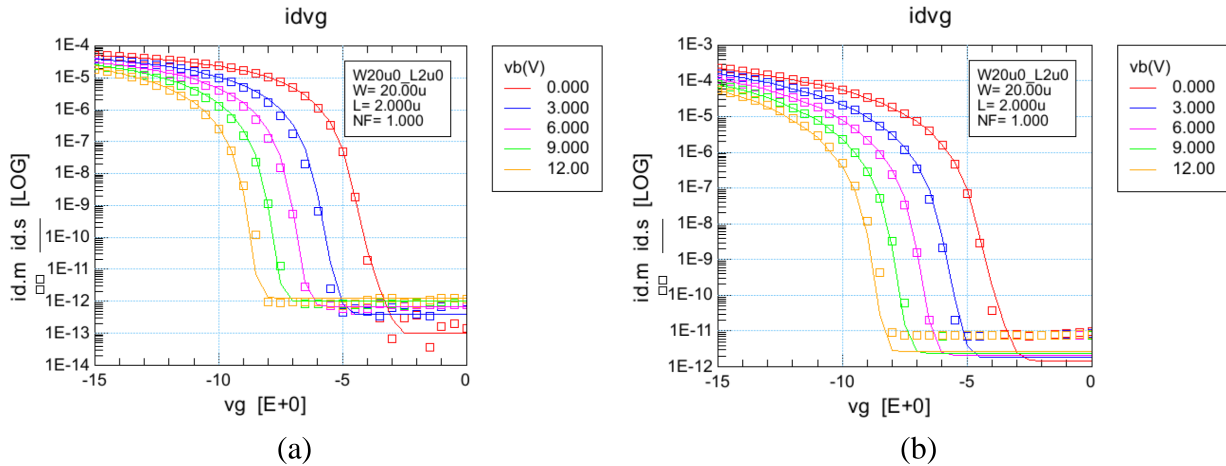


Fig. 7.67. Transfer characteristics of a 20 µm / 2 µm (typical analog device) PMOS at 25 ⁰ C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

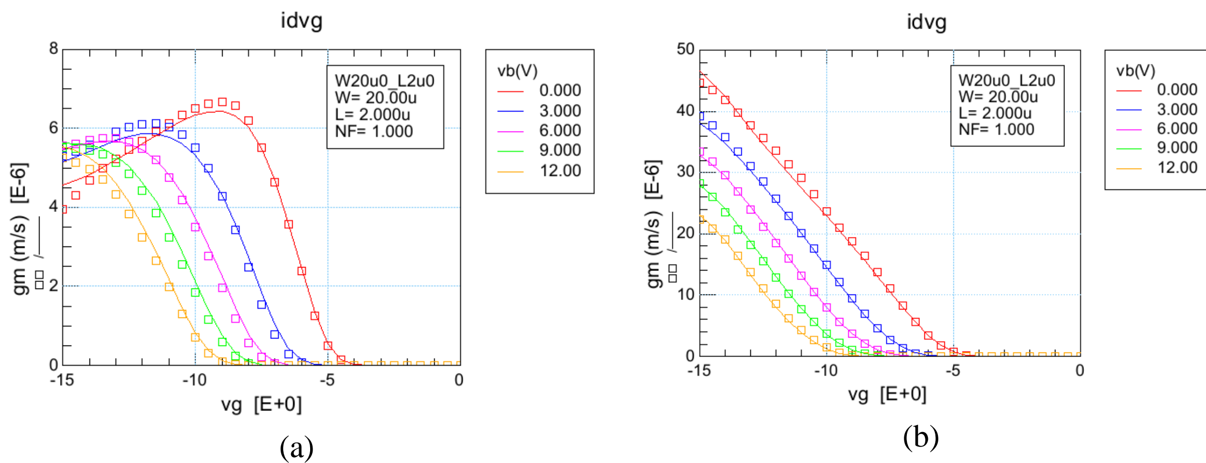
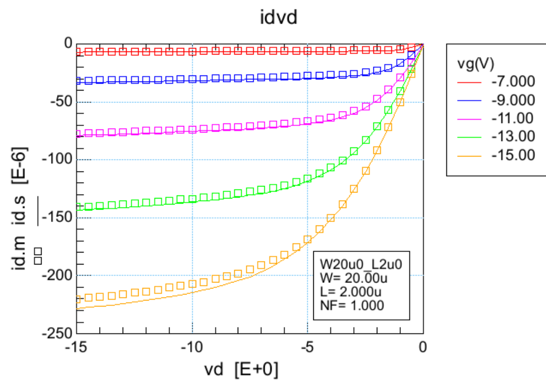
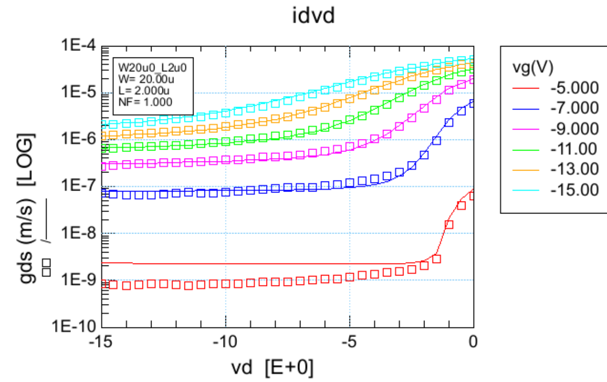


Fig. 7.68. Transconductance of a 20 µm / 2 µm (typical analog device) PMOS at 25 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

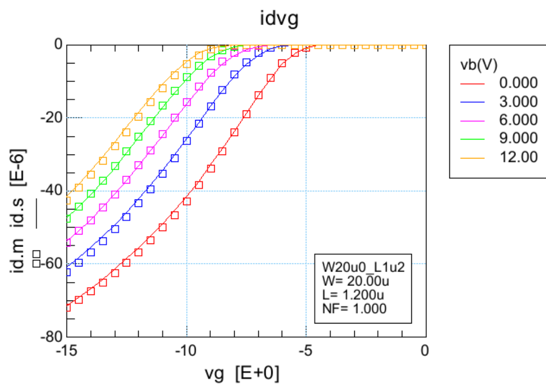


(a)

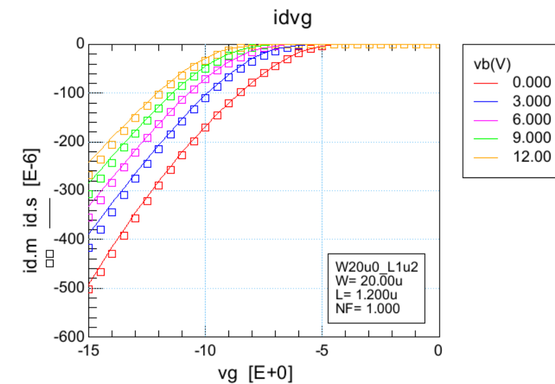


(b)

Fig. 7.69. (a) Output characteristics and (b) output conductance of a 20 µm / 2 µm (typical analog device) PMOS at 25 ° C.

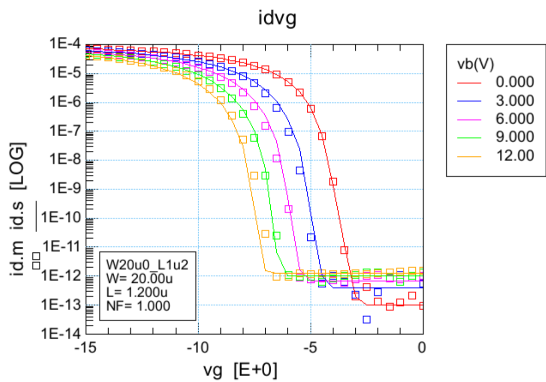


(a)

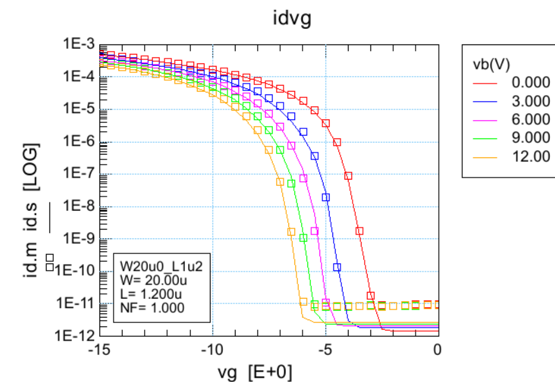


(b)

Fig. 7.70. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) PMOS at 25 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

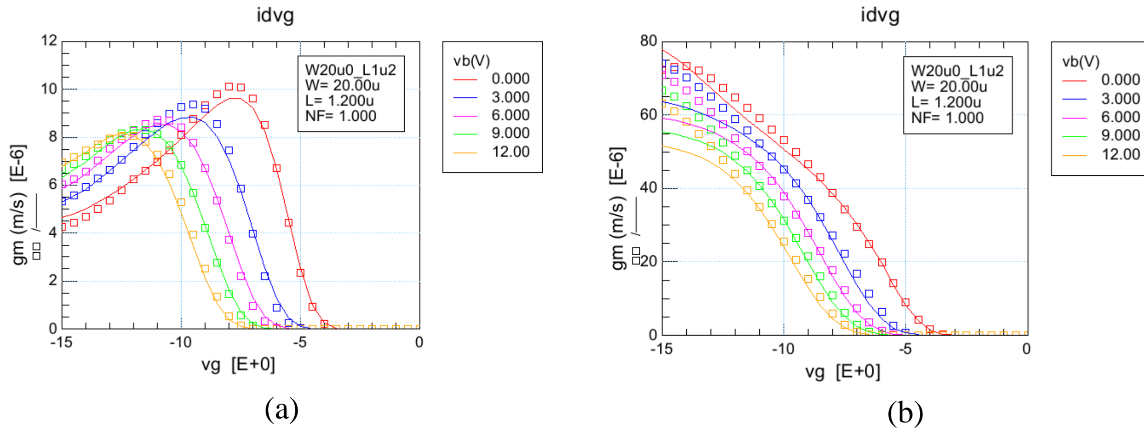


(a)



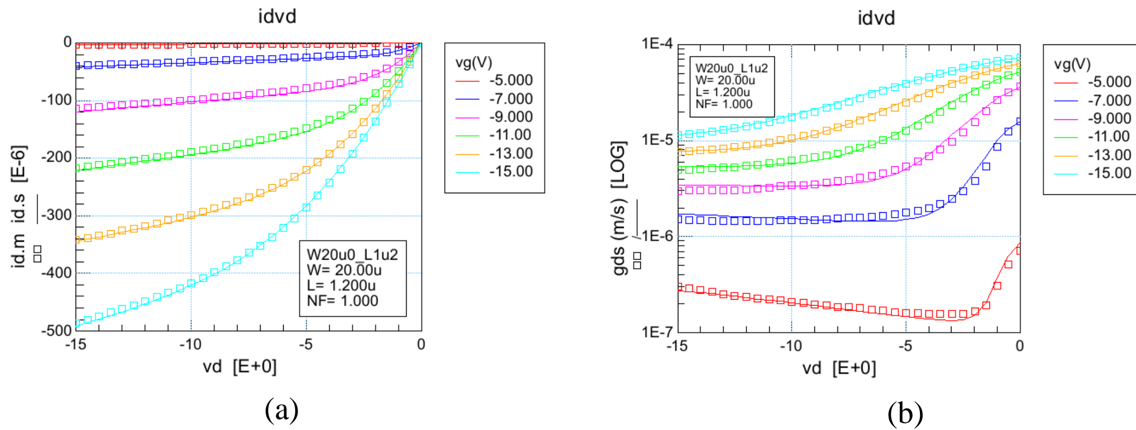
(b)

Fig. 7.71. Transfer characteristics of a 20 µm / 1.2 µm (wide and short) PMOS at 25 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



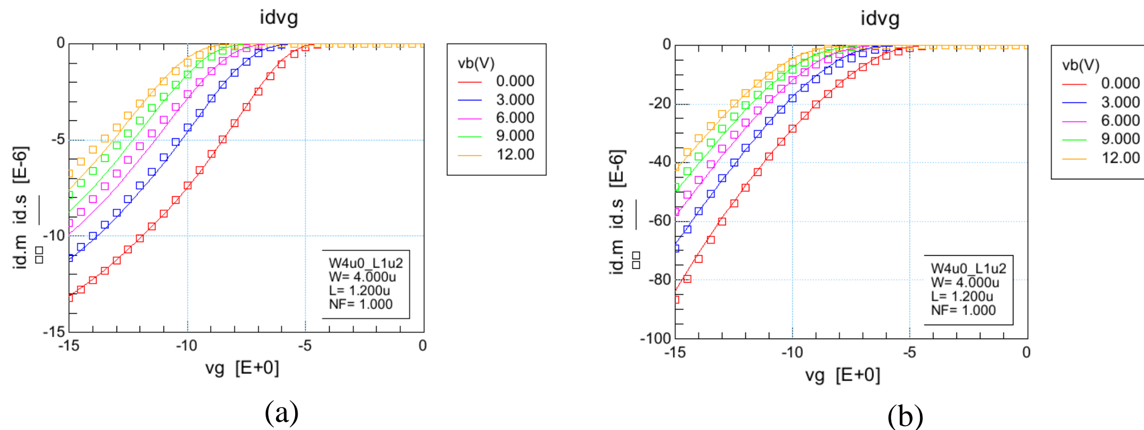
(a) (b)

Fig. 7.72. Transconductance of a 20 µm / 1.2 µm (wide and short) PMOS at 25 ⁰ C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.73. (a) Output characteristics and (b) output conductance of a 20 µm / 1.2 µm (wide and short) PMOS at 25 ⁰ C.



(a) (b)

Fig. 7.74. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) PMOS at 25 ⁰ C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

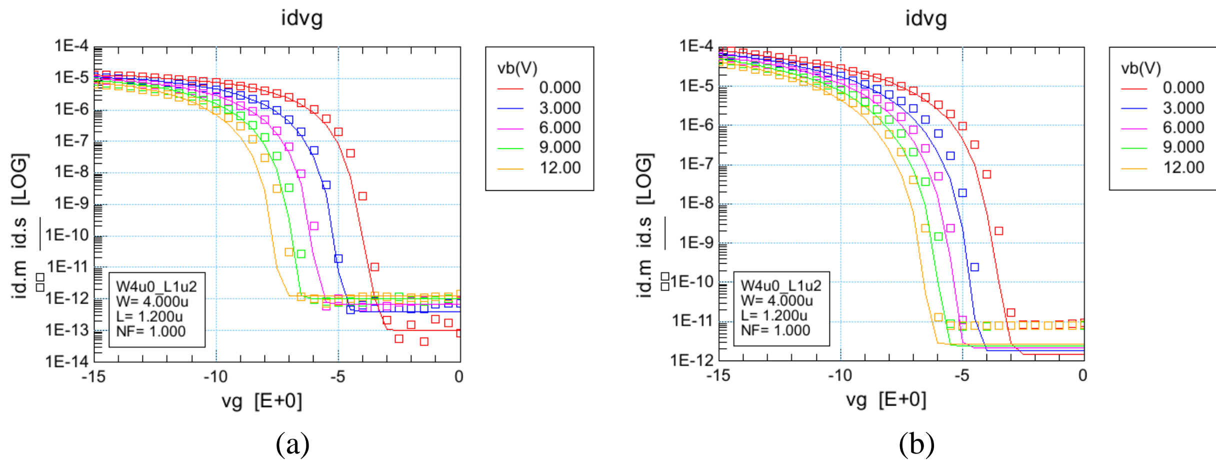


Fig. 7.75. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) PMOS at 25 º C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

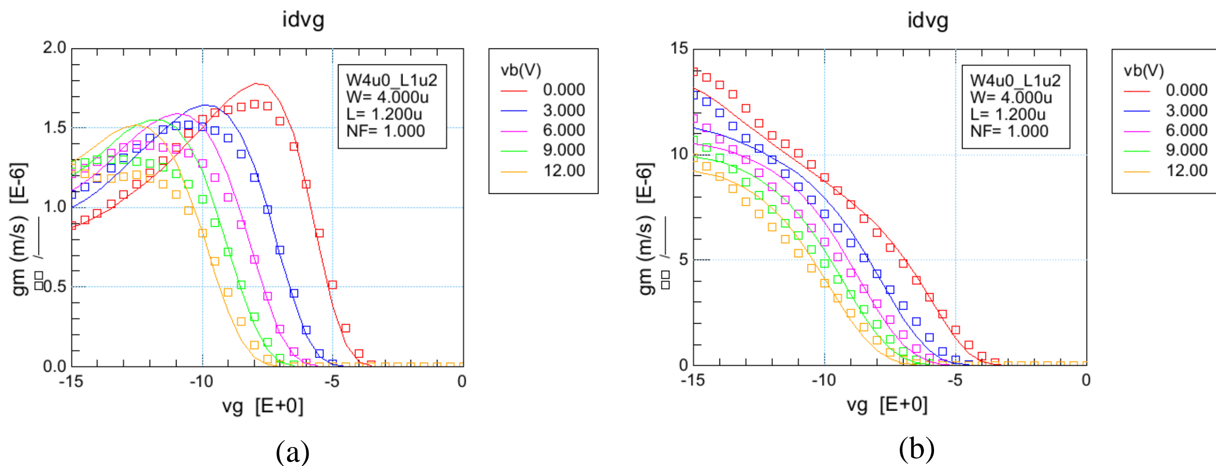


Fig. 7.76. Transconductance of a 4 µm / 1.2 µm (narrow and short) PMOS at 25 º C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

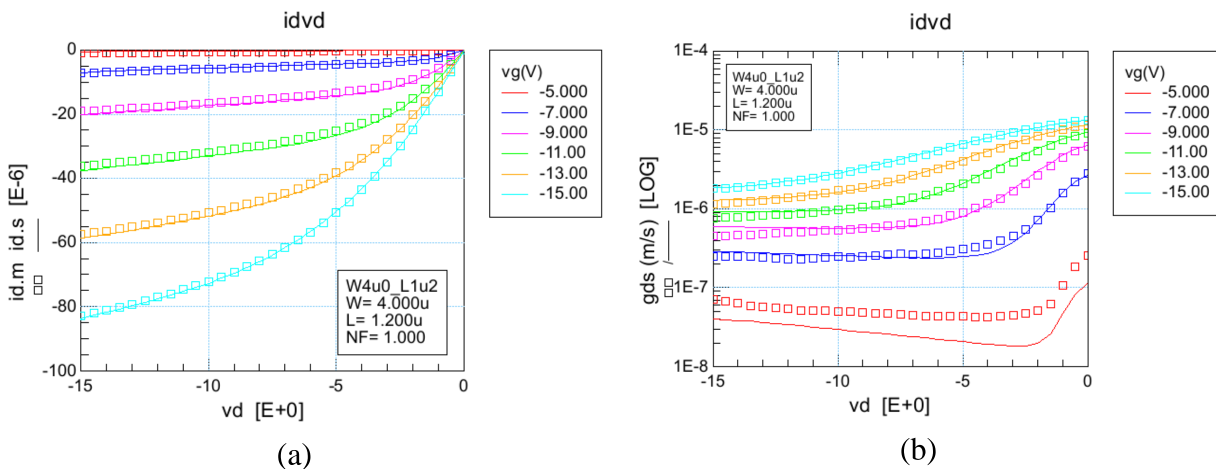


Fig. 7.77. (a) Output characteristics and (b) output conductance of a 4 µm / 1.2 µm (narrow and short) PMOS at 25 º C.

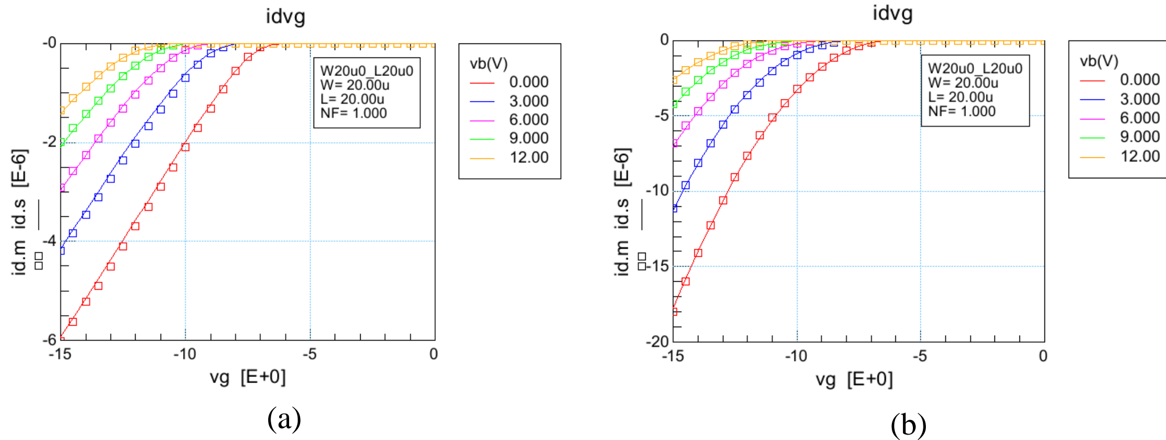


Fig. 7.78. Transfer characteristics of a 20 μm / 20 μm (wide and long) PMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

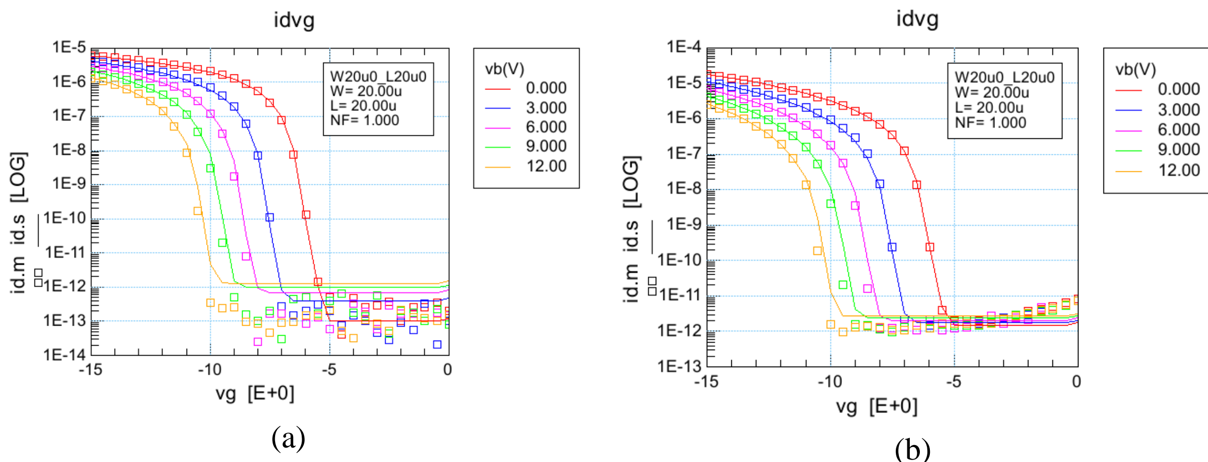


Fig. 7.79. Transfer characteristics of a 20 μm / 20 μm (wide and long) PMOS at 300 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

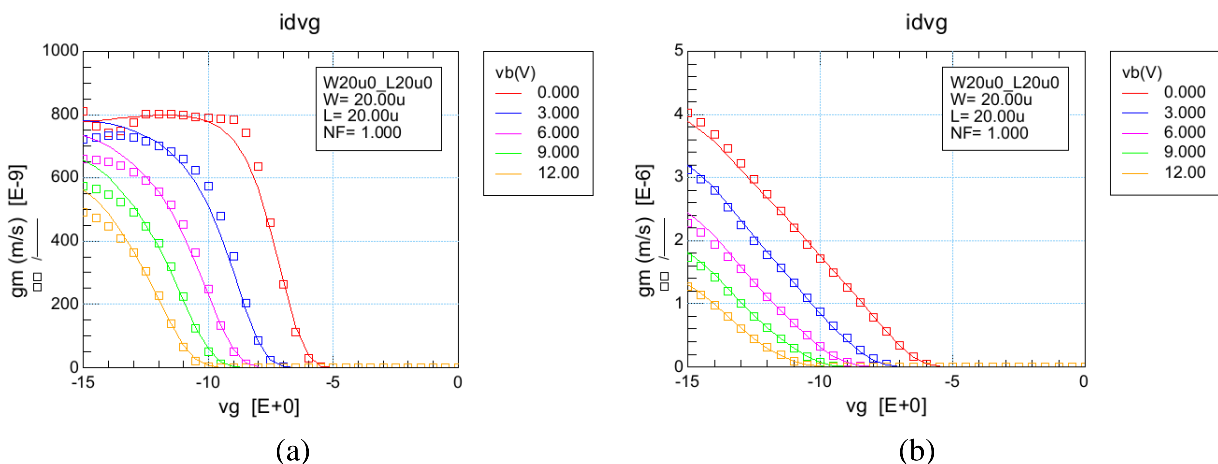
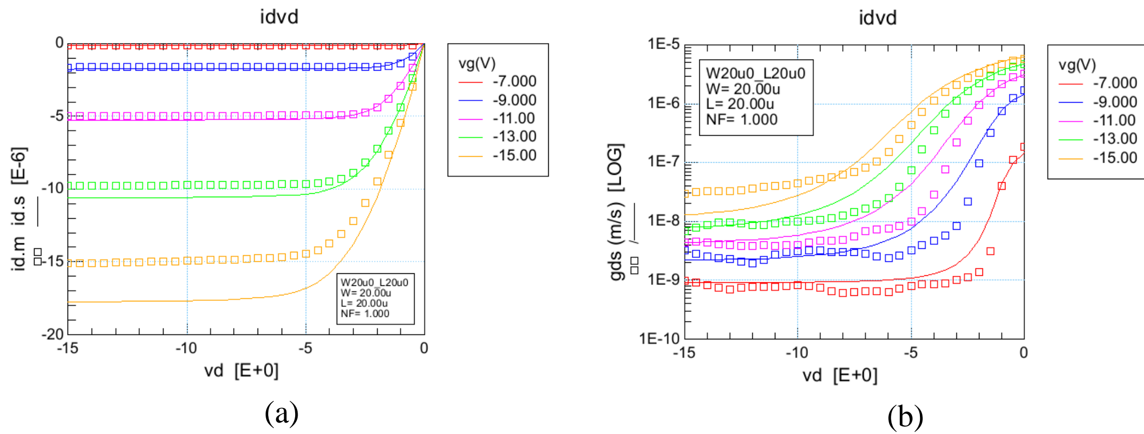
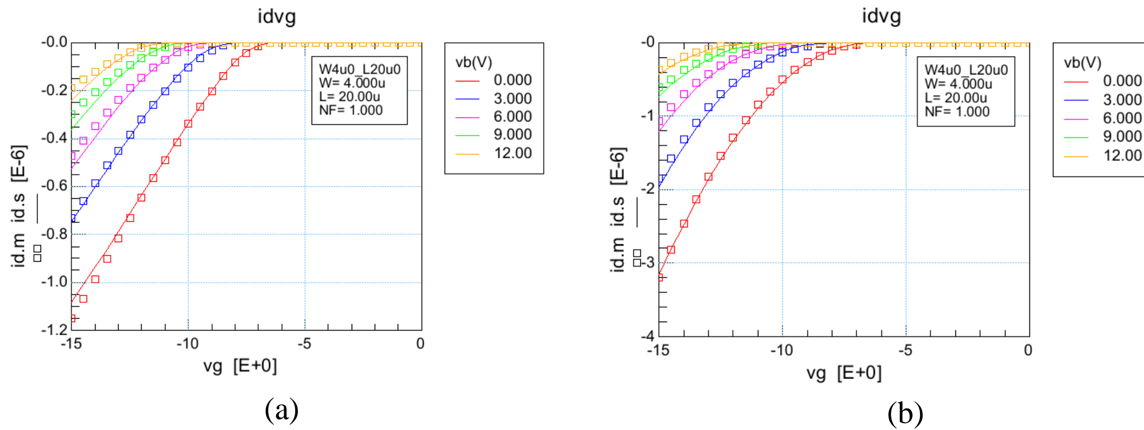


Fig. 7.80. Transconductance of a 20 μm / 20 μm (wide and long) PMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



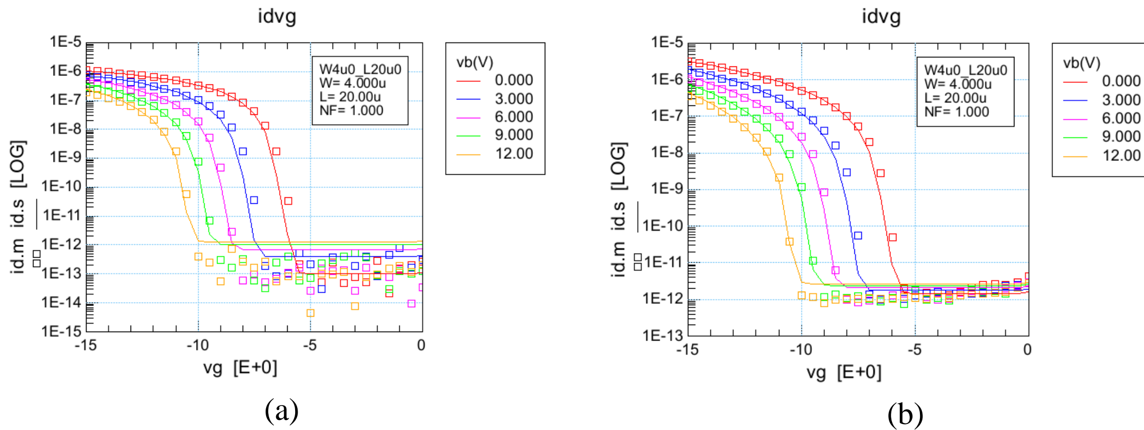
(a) (b)

Fig. 7.81. (a) Output characteristics and (b) output conductance of a 20 µm / 20 µm (wide and long) PMOS at 300 º C.



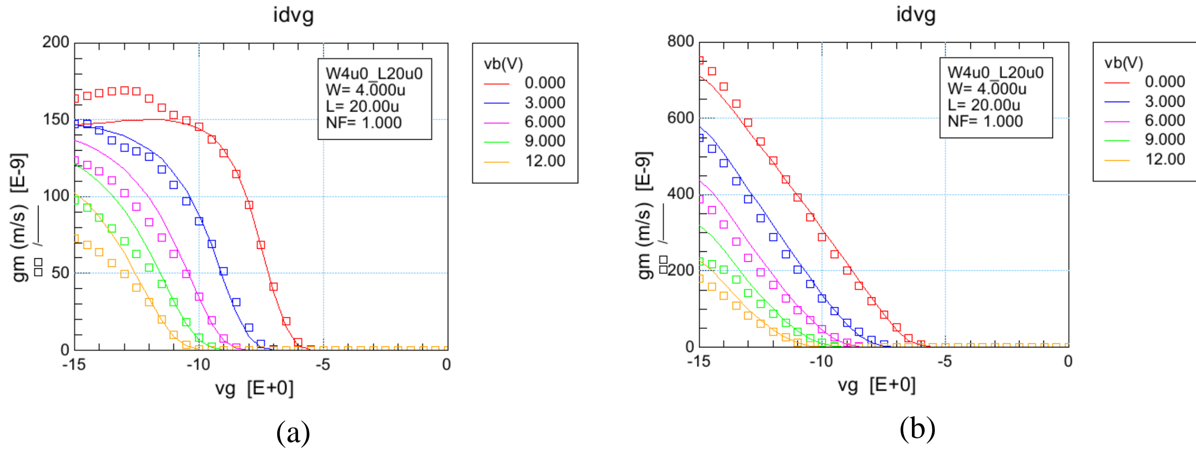
(a) (b)

Fig. 7.82. Transfer characteristics of a 4 µm / 20 µm (narrow and long) PMOS at 300 º C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



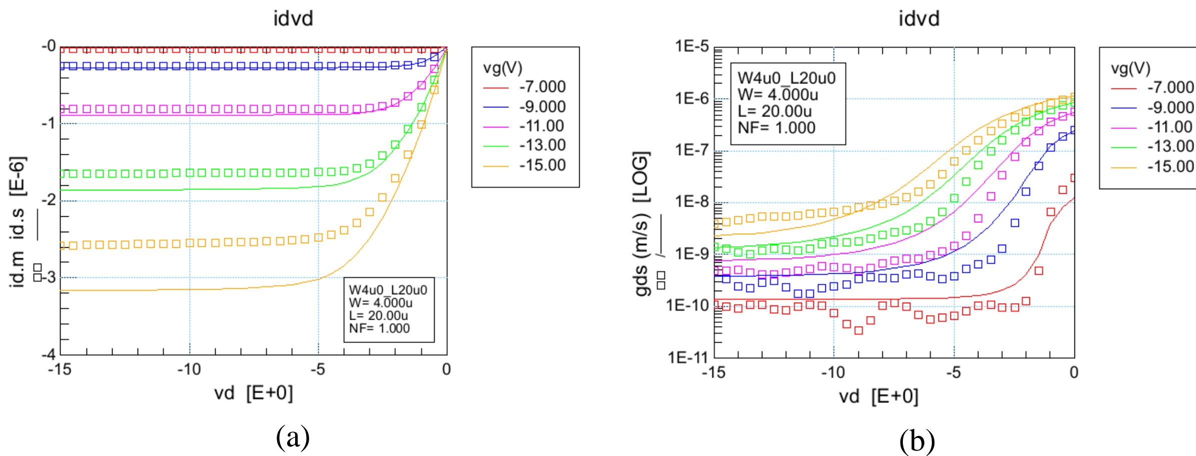
(a) (b)

Fig. 7.83. Transfer characteristics of a 4 µm / 20 µm (narrow and long) PMOS at 300 º C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



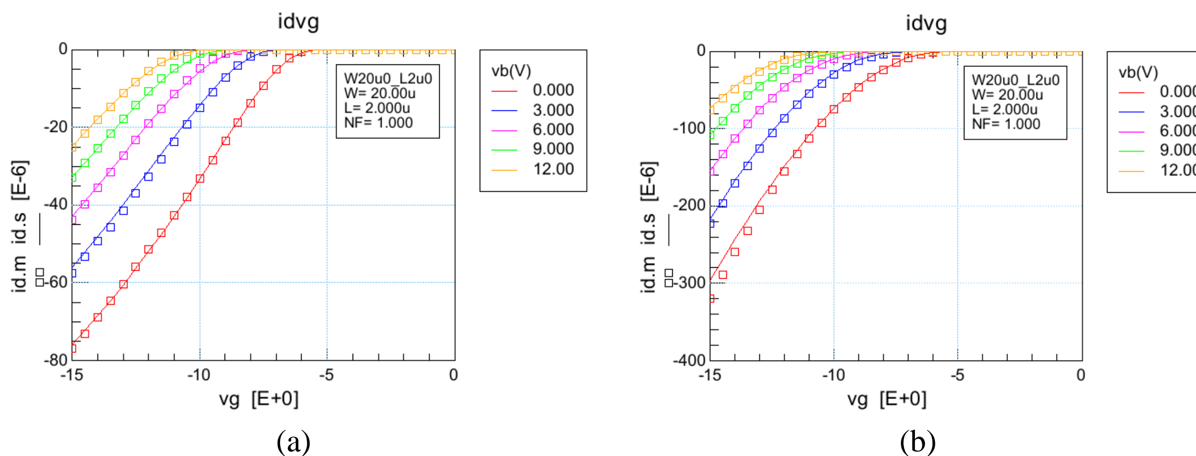
(a) (b)

Fig. 7.84. Transconductance of a 4 µm / 20 µm (narrow and long) PMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.85. (a) Output characteristics and (b) output conductance of a 4 µm / 20 µm (narrow and long) PMOS at 300 ° C.



(a) (b)

Fig. 7.86. Transfer characteristics of a 20 µm / 2 µm (typical analog device) PMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

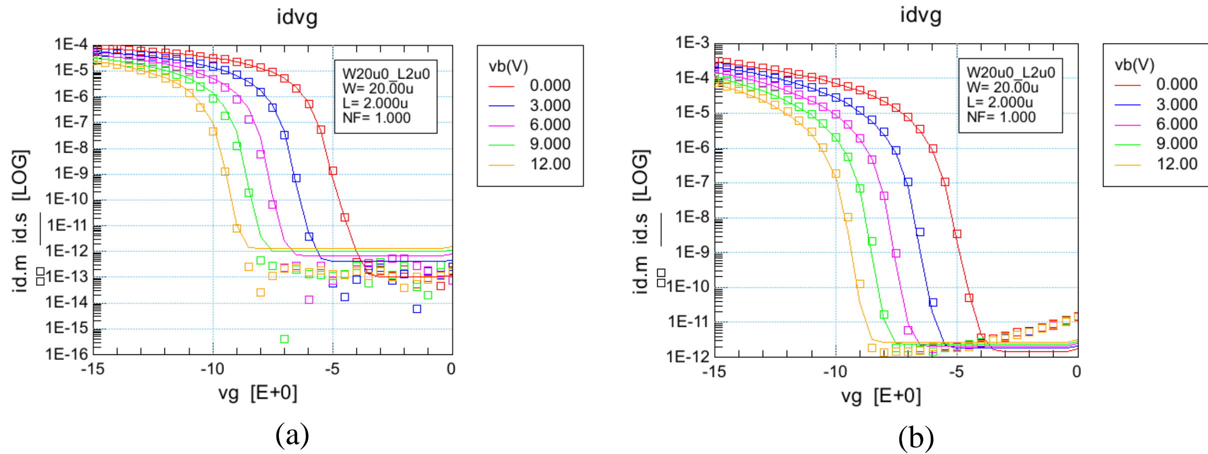


Fig. 7.87. Transfer characteristics of a 20 μm / 2 μm (typical analog device) PMOS at 300 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.

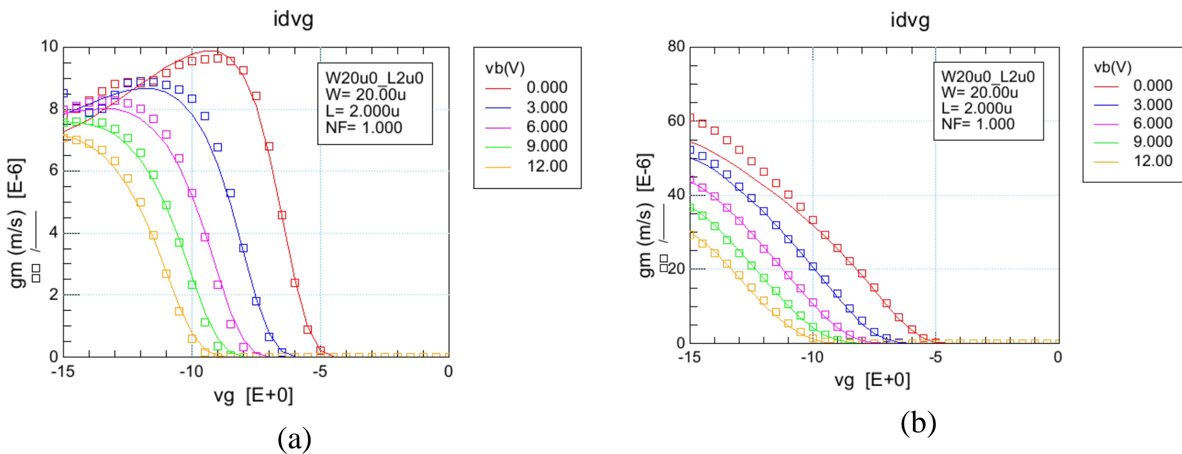


Fig. 7.88. Transconductance of a 20 μm / 2 μm (typical analog device) PMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

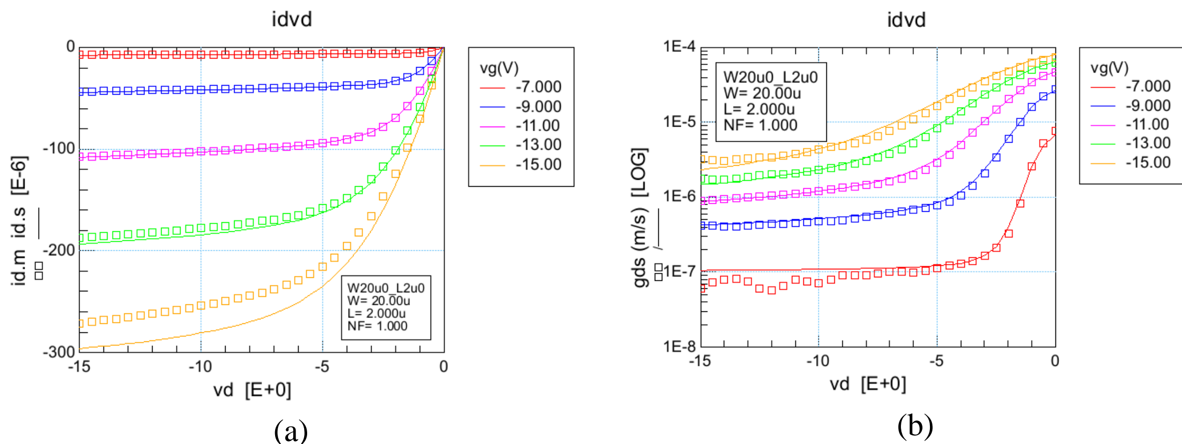
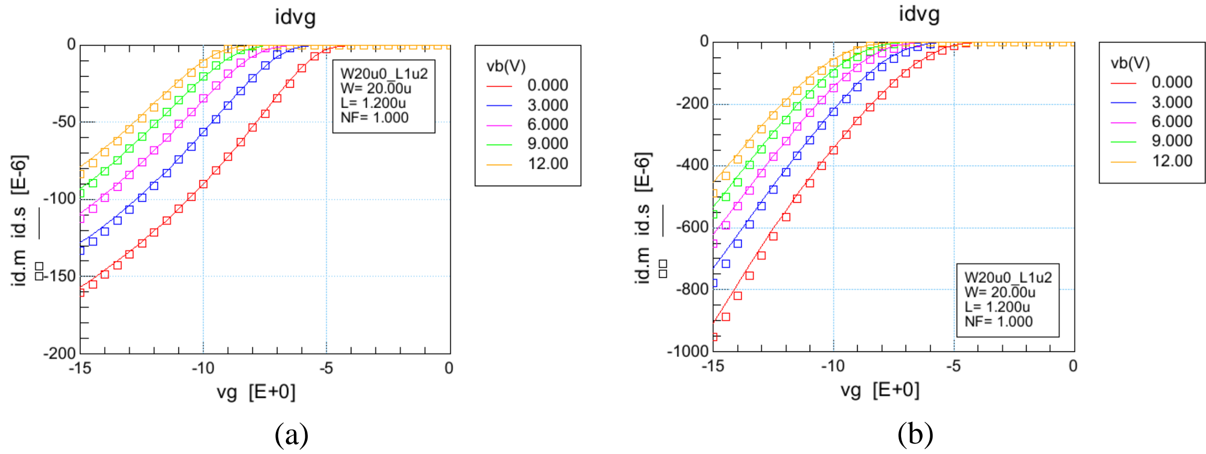
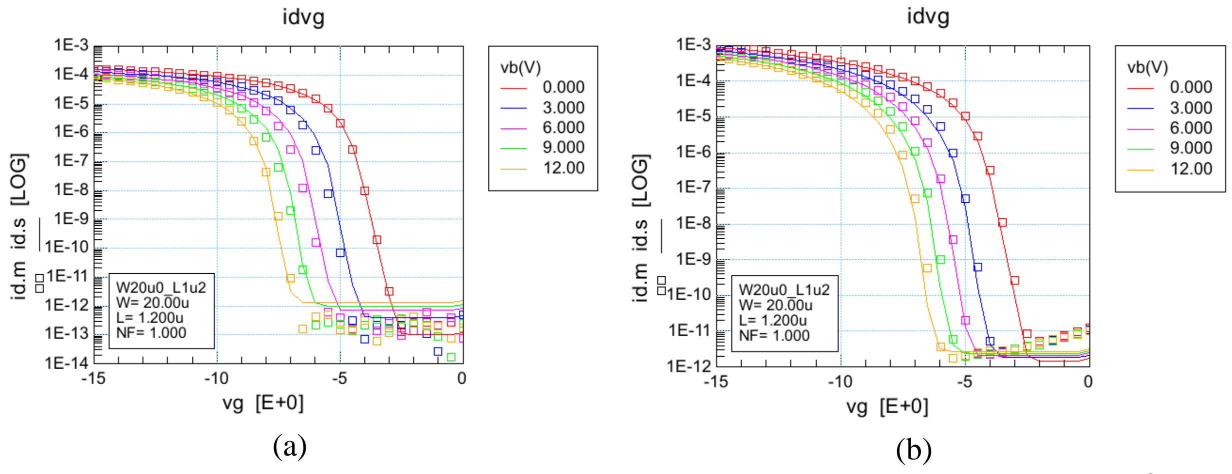


Fig. 7.89. (a) Output characteristics and (b) output conductance of a 20 μm / 2 μm (typical analog device) PMOS at 300 ° C.



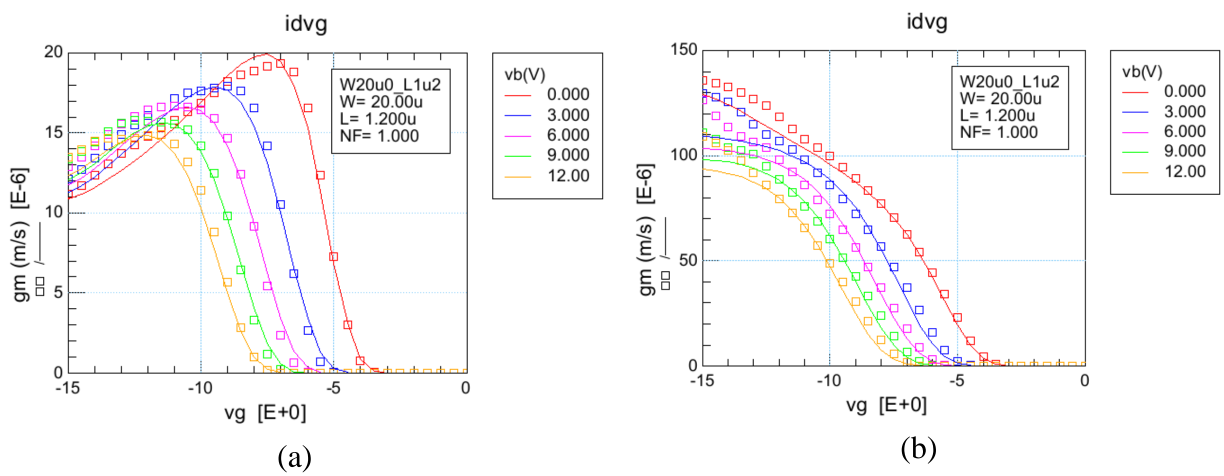
(a) (b)

Fig. 7.90. Transfer characteristics of a 20 μm / 1.2 μm (wide and short) PMOS at 300 ^{o} C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.91. Transfer characteristics of a 20 μm / 1.2 μm (wide and short) PMOS at 300 ^{o} C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a) (b)

Fig. 7.92. Transconductance of a 20 μm / 1.2 μm (wide and short) PMOS at 300 ^{o} C; (a) at 0.5 V and (b) 15V drain-to-source voltage.

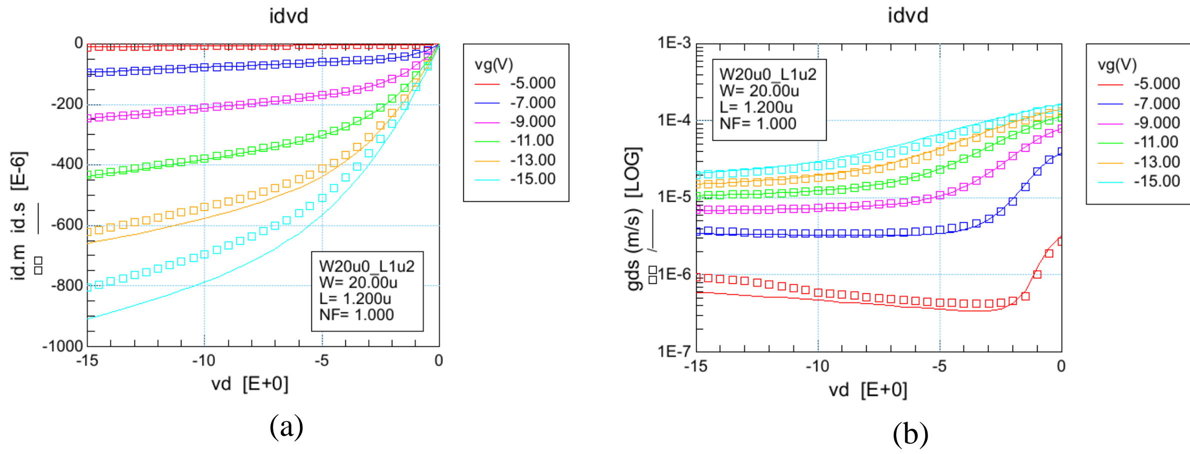


Fig. 7.93. (a) Output characteristics and (b) output conductance of a 20 µm / 1.2 µm (wide and short) PMOS at 300 ° C.

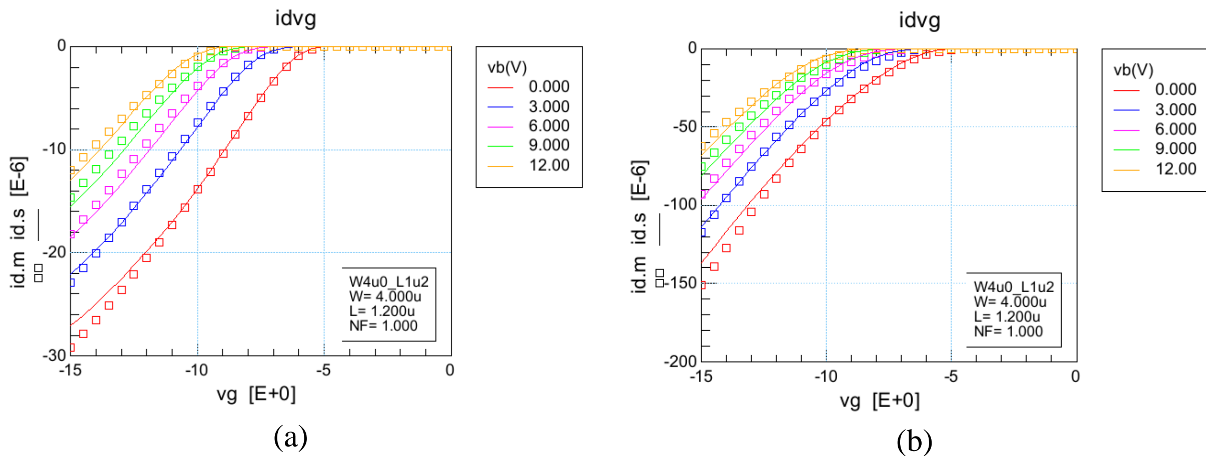


Fig. 7.94. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) PMOS at 300 ° C in strong inversion; (a) at 0.5 V and (b) 15V drain-to-source voltage.

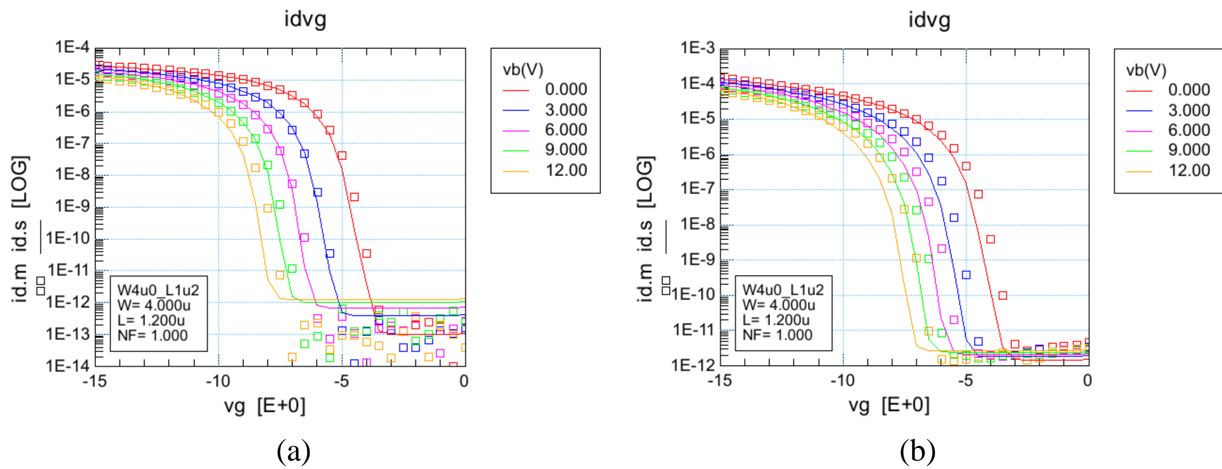
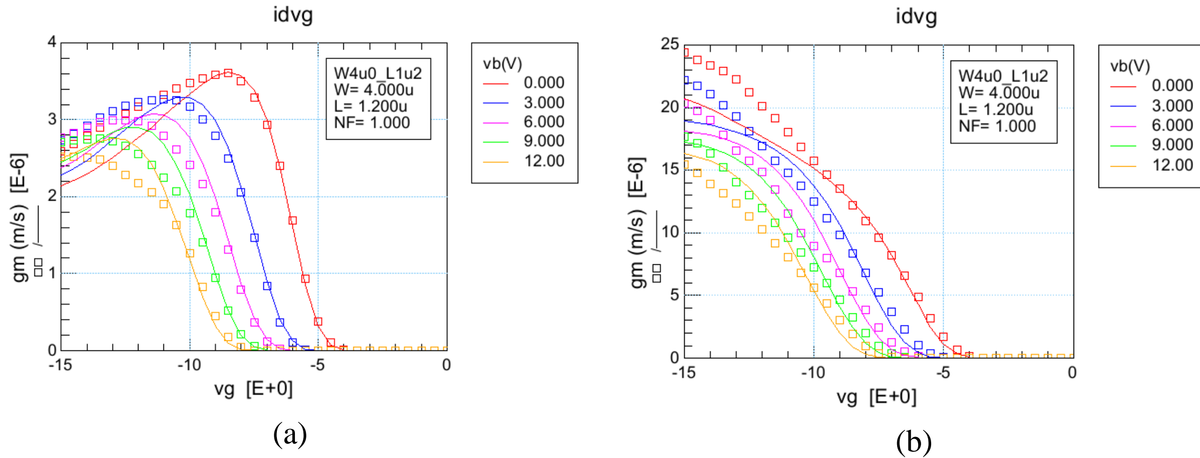


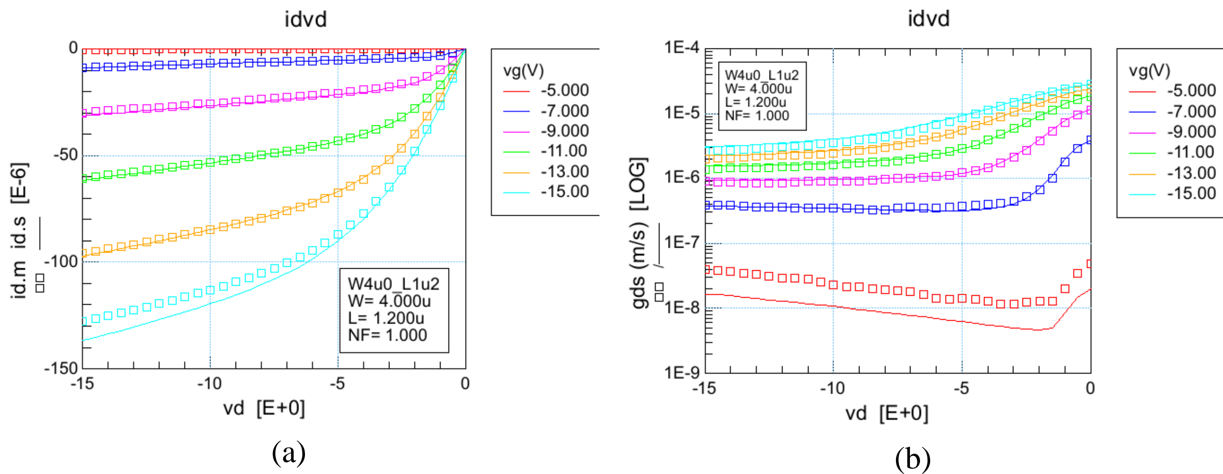
Fig. 7.95. Transfer characteristics of a 4 µm / 1.2 µm (narrow and short) PMOS at 300 ° C in subthreshold; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a)

(b)

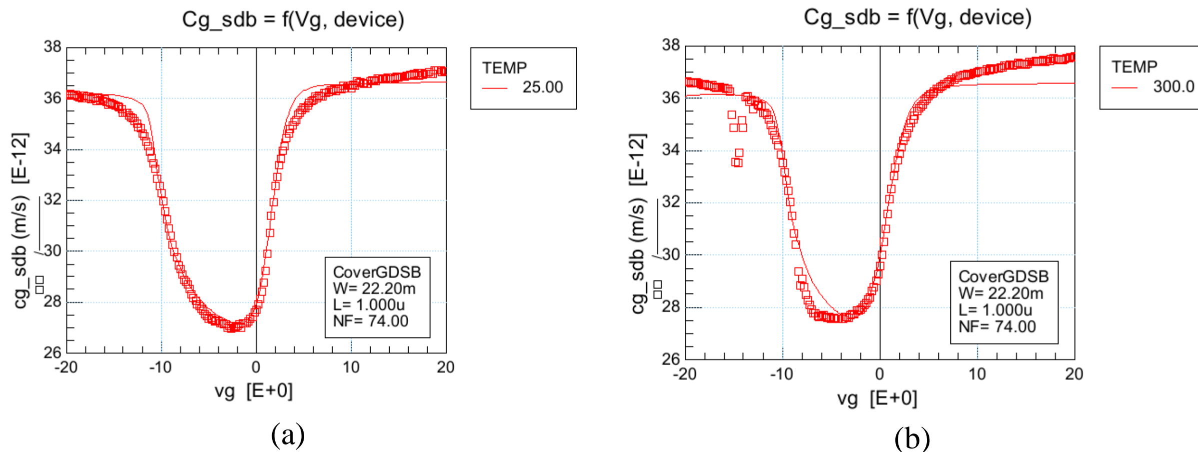
Fig. 7.96. Transconductance of a 4 µm / 1.2 µm (narrow and short) PMOS at 300 ° C; (a) at 0.5 V and (b) 15V drain-to-source voltage.



(a)

(b)

Fig. 7.97. (a) Output characteristics and (b) output conductance of a 4 µm / 1.2 µm (narrow and short) PMOS at 300 ° C.



(a)

(b)

Fig. 7.98. Total gate capacitance ($C_{g\text{-}dsb}$ vs. $V_{g\text{-}dsb}$) of NMOS at (a) 25 ° C and (b) 300 ° C.

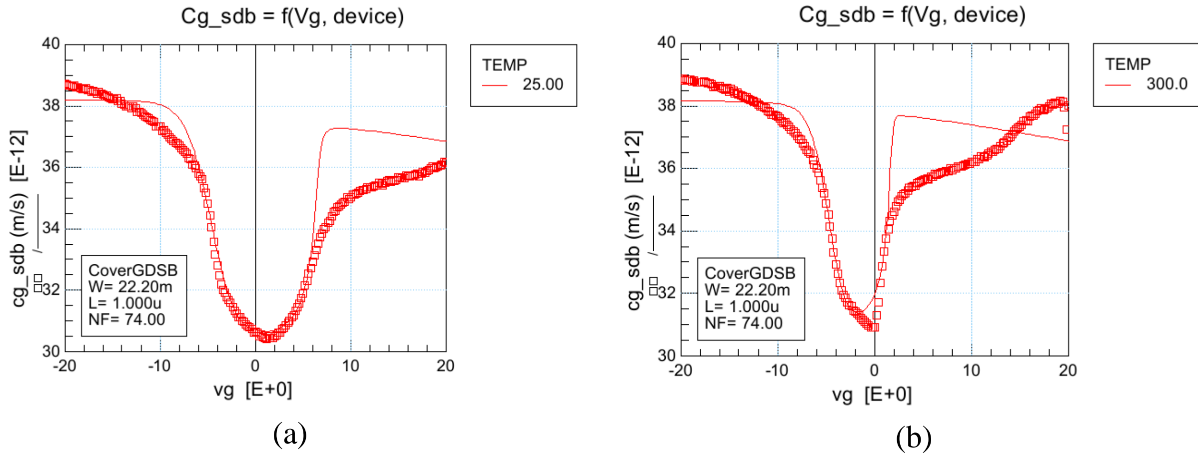


Fig. 7.99. Total gate capacitance ($C_{g\text{-}dsb}$ vs. $V_{g\text{-}dsb}$) of PMOS at (a) 25 ⁰ C and (b) 300 ⁰ C.

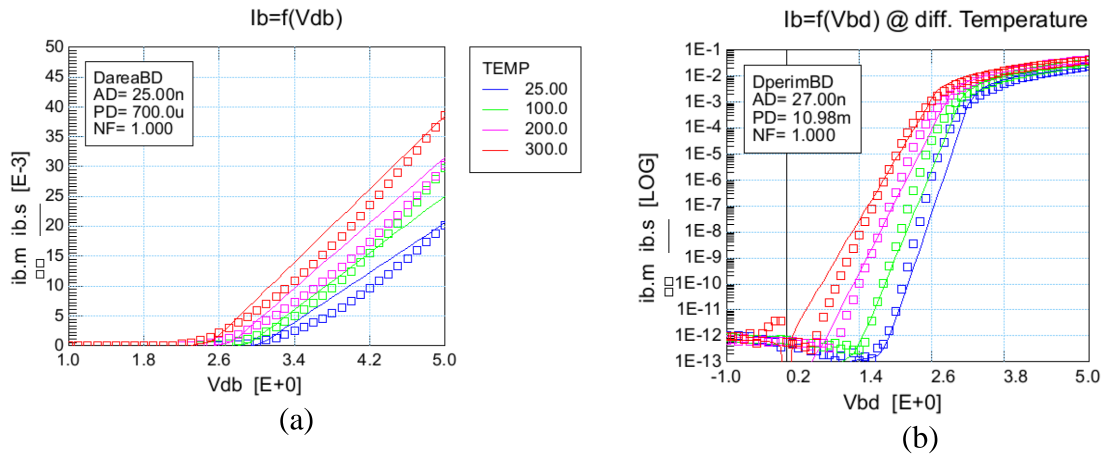


Fig. 7.100. The DC current characteristics of P+/N-well diode in (a) linear scale and (b) log scale.

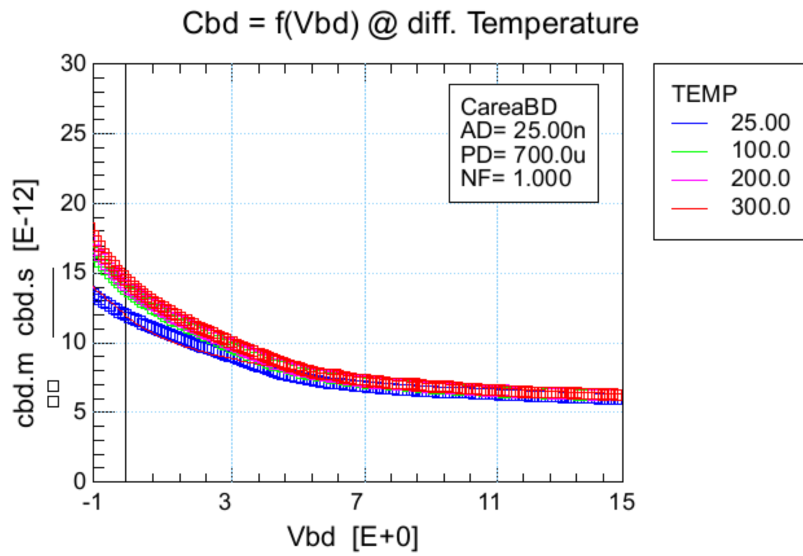


Fig. 7.101. The junction capacitance of P+/N-well diode at different temperatures.

7.8 Model Verification

The Verilog-A models were installed in the Raytheon HitSiC PDK and verified with both HSPICE and the Spectre circuit simulator. All the previously designed circuits such as opamp, comparator, voltage and current references, linear regulator, switch mode regulator and data converter were simulated with the new models. The simulation results were as expected and no convergence issues were found. The simulation time was a bit longer than it was with the built-in HSPICE BSIM4.6.5 models. The delay was mainly from the Verilog-A compilation by the simulator. The bias dependent new models that were added in the BSIM4 model to accommodate the SiC MOSFET might also increase the simulation time.

7.9 Discussion on the model performance

The model performance of the BSIM4SIC is good except for an extreme corner. The body effect modeling in the transconductance curve for short channel NMOS and PMOS at 300 ^{o} C has some discrepancies (Fig. 7.52, Fig. 7.56., Fig. 7.92 and Fig. 7.96). The device characteristics at high temperature in a short channel SiC MOSFET are significantly different due to the small influence of the interface trapped charge. The MOBMOD = 3 mobility model which takes into account the effects on interface trapped charge no longer performs well. This limitation should not be a big problem since the transconductance curves match well at the peak transconductance which is necessary for accurate simulation of digital circuits which typically employ the short channel transistors. There is also a mismatch between the measured and simulated total gate capacitance curve of the PMOS (Fig. 7.99). The discrepancy in the accumulation region is due to the bias dependent flat band voltage. It is more severe in PMOS because the effect of interface trapped charge which makes the flat band voltage bias dependent is more prominent in a p-type SiC MOSFET. Also, due to poor oxide quality of PMOS, the device exhibits more leakage current at

higher gate biases. This will introduce some error in the capacitance measurement. The discrepancy in the inversion region is because the surface potential in strong inversion is assumed to be constant in BSIM4. Although there is an option for an incremental surface potential change in the C-V model of BSIM4, the amount of change that can be achieved by varying the related model parameter MOIN is very small and thus the moderate inversion region cannot be modeled properly.

7.10 Summary

The implementation of the BSIM4.7.0 model in Verilog-A is discussed in this chapter. The strategy of modifying the BSIM4 model with the proposed changes relevant to the SiC devices is outlined. A detail description of the proposed changes is also provided. The parameter extraction and optimization sequence is demonstrated with the help of the related plots of the device characteristics. The model performance is verified by presenting the optimization results of a wide variety of devices at 25 and 300 ^{o} C.

CHAPTER 8 CONCLUSION AND FUTURE WORK

8.1 Research Summary

A comprehensive study of SiC MOSFET is performed in this work for the purpose of developing good compact models for integrated circuit design. The MOS devices are thoroughly characterized over a wide temperature range. From the investigation of the measured data it is found that the characteristics of SiC MOSFET is significantly different from their Si counterpart. The oddity mainly arises from the presence of interface trapped charge which is practically non-existent in modern day Si MOSFETs. The interface trapped charge is responsible for flat band voltage shift, increase in subthreshold slope (mV/decade), mobility reduction, non-monotonic temperature behavior, soft velocity saturation and non-ideal body effect. The poor-quality oxide and interface are also responsible for aging issues of the SiC PMOS.

Instead of attempting to develop a compact model for the SiC MOSFET from scratch, BSIM3V3 was selected as the foundation. The models optimized based on BSIM3V3 were used for circuit design in one tape-out with Raytheon HiTSiC process. Since BSIM3V3 could not adequately model the characteristics of SiC MOSFET, later the model was replaced by the BSIM4 model. The BSIM4.6.5 based models were used for numerous circuits and systems design in another tape-out. But BSIM4 also has some limitations and could not accurately model the entire device characteristics of SiC MOSFET. New models were developed for the body effect and soft saturation of the devices and added in the Verilog-A version of the model (BSIM4SIC) following a proper strategy. The Verilog-A version of the model was developed using a software tool called Paragon which was created in the University of Arkansas. The parameters for the BSIM4SIC model were extracted and optimized using an industry standard modeling tool ICCAP. The models are temperature and width scalable but a binning approach is used for length scaling. The models

are validated with the measured device characteristics of a large number of devices characterize at four different temperature points.

8.2 Major Conclusions

The BSIM4 model was successfully used as a foundation for developing compact models for SiC devices. Since BSIM4 is a semi-empirical model and not intensively physical, it can be used for the development of the MOSFET models in a new technology. The compact models such as PSP are not suitable this purpose.

8.3 Future Work

In this work, the parameter extraction and optimization process was mostly manual. The entire extraction process might be automated in the future when the process and the device characteristics are properly understood and the process variations are predictable.

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APPENDIX

The following file is used to input the source directory of the measured data in xls form and output the generated mdm files for ICCAP in a destination directory.

```
from k4200parser import *
parser=KeithelyDataParse(plotOut=None, histOut=None)

# Directory and file name construction of mdm files
path_mdm=
"/home/sxa031/models/BSIM4_470/BSIM4SIC_Model_Optimization_Vulca
nII/W36_R4C2/NFET/vulcanII_w36_r4c2/"
mdm1 = "vulcanII_w36_r4c2_nfet~"
mdm_device    =    ["W20u0_L1u2",    "W4u0_L1u2",    "W4u0_L1u5",
"W20u0_L1u5",     "W20u0_L2u0",     "W4u0_L2u0",     "W20u0_L5u0",
"W4u0_L10u0",    "W4u0_L20u0",    "W20u0_L10u0",    "W20u0_L20u0",
"W6u6_L20u0"]
mdm2 = "~dc_id"
mdm_setup = ["vg", "vd", "vd_vbmin"]
mdm3 = "~"
mdm_temp = ["298K", "373K", "473K", "573K", "673K"]
mdm4 = ".mdm"

# Directory and file name construction of excel files
path_xls                                                         =
["//home/sxa031/models/BSIM4_470/Characterization_data_W36_R4C2/
MOSFET/25C/DC/data/",
"/home/sxa031/models/BSIM4_470/Characterization_data_W36_R4C2/MO
SFET/100C/DC/data/",
"/home/sxa031/models/BSIM4_470/Characterization_data_W36_R4C2/MO
SFET/200C/DC/data/",
"/home/sxa031/models/BSIM4_470/Characterization_data_W36_R4C2/MO
SFET/300C/DC/data/"]
xls1 = "Id_"
xls_setup = ["Vg_", "Vd", "Vd_Vbmin"]
xls_vd  =  ["Vd_0p5",  "Vd_1",  "Vd_2",  "Vd_3",  "Vd_6",  "Vd_9",
"Vd_12", "Vd_15"]
xls11 = "_N"
xls2 = "#1@"
xls_device = ["1", "2", "3", "4", "5", "6", "7", "8", "9", "10",
"11", "12"]
xls3 = ".xls"
```

```
# function to stream data from excel files
def xls_to_stream (directory, stream, setup):
     workbook = xlrd.open_workbook(directory)
     data,biasVals=parser.parseDataSheet(workbook)
     parser.parseSettingsSheet(workbook)
     if setup=="vg":
          stream = parser.data2mdmFile_v3(data,biasVals,stream)
     else:
          stream = parser.data2mdmFile_v4(data,biasVals,stream)
     return stream

# Data conversion from excel to mdm
for temp in range(len(mdm_temp)-1):
     for device in range(len(mdm_device)):
          for setup in mdm_setup:
               fp                     =                    open
(path_mdm+mdm1+mdm_device[device]+mdm2+setup+mdm3+mdm_temp[temp]
+mdm4, "r+")
               stream = parser.xls2mdm_editing(fp)
               if setup=="vg":
                    for vd in xls_vd:
                         stream          =          xls_to_stream
(path_xls[temp]+xls1+xls_setup[0]+vd+xls11+xls2+xls_device[devic
e]+xls3, stream, setup)

                    parser.mdmfile_generator(stream, fp)
               elif setup == "vd":
                    stream             =               xls_to_stream
(path_xls[temp]+xls1+xls_setup[1]+xls11+xls2+xls_device[device]+
xls3, stream, setup)

                    parser.mdmfile_generator(stream, fp)
               else:
                    stream             =               xls_to_stream
(path_xls[temp]+xls1+xls_setup[2]+xls11+xls2+xls_device[device]+
xls3, stream, setup)

                    parser.mdmfile_generator(stream, fp)
```

The following file is used to convert the xls files to the mdm file:

```
import os,sys
import pylab as pp
from matplotlib.backends.backend_pdf import PdfPages
import xlrd
```

```
import numpy
FATAL=False #Stop on ERRORS
SHOW=False #Show plots, otherwise only create PDF
DEBUG=True
DOHIST=False
LOAD_FROM_EXCEL=False

class KeithelyDataParse:
    def __init__(self,plotOut=None,histOut=None):
              if plotOut != None:
               self.ppdf=PdfPages(plotOut)
               if histOut:
                   self.ppdf2=PdfPages(histOut)
               else:
                   self.ppdf2=None
               self.report=[('\t'.join(
[str('title'),str('set'),str('bias'),str('biasVal'),str('wafer')
,str('MaxVal')]))]
               self.MS=""
              else:
               self.ppdf=None
               self.ppdf2=None
    def initData(self,data,wafer,type,size):
        if type not in data.keys():
            data[type]={}
        if size not in data[type].keys():
            data[type][size]={}
        if wafer not in data[type][size].keys():
            data[type][size][wafer]={}
        return data
    def
checkStoreBias(self,biasLen,type,size,ef,numbias,file=""):
        if type not in biasLen.keys():
            biasLen[type]={}
        if size not in biasLen[type].keys():
            biasLen[type][size]={}
        if ef not in biasLen[type][size].keys():
            biasLen[type][size][ef]=numbias
        if numbias != biasLen[type][size][ef]:
            self.MS=self.MS+ "\nWARNING: Bad number of bias steps
(inconsistent) in file %s %s" %(file,ef)
            self.MS=self.MS+ "\n            Last, %s New %s" %
(numbias, biasLen[type][size][ef])
            if numbias> biasLen[type][size][ef]:
                biasLen[type][size][ef]=numbias
        return biasLen
```

```
def
getExcelData(self,topdirs,skip,subsets=[('type',[""]),('size'),(
'wafer')]):
                """ Can sort by up to 3 fields, type,size,wafer +
charset""
        #Data in individually named folders
        data={}
        biasLookup={}
        for topdir in topdirs:
            files=os.listdir(topdir)
            #Matt's data
            for f in files:
                #print f
                ddir=os.path.join(topdir,f)

                doit=True
                for sk in skip:
                    if f.find(sk)>=0:
                        doit=False
                        self.MS=self.MS+ "\nNOTE: Skipping "+ f
               #Sort by fields
               if f.find("_") != -1 and len(subsets) > 1:
                    sp=f.split("_")
                    wafer="_".join(sp[0:3])
                    addr="_".join(sp[2:3])
                    size=sp[3]
                    if len(sp) > 4:
                        attr=sp[4]
                        print "This set marked!", attr
                    #print wafer
                    #print addr
                    #print size

                    if addr in pfets:
                        type="pfet"
                    else:
                        type="nfet"
                    #print type
                    #data[size]={}
                #sys.exit(-1)
               else:
                    wafer=f
                    size=""
                    type=""
                    addr=""
                if doit and os.path.isdir(ddir):
```

```
data=self.initData(data,wafer,type,size)
biasLookup=self.initData(biasLookup,wafer,type,size)
                    if os.path.isdir(ddir):
                        for ef in os.listdir(ddir):
                         #print ef
                         efile,ext=os.path.splitext(ef)
                         efile=os.path.join(ddir,ef)
                         if ext == ".xls":
                             #data[type][size][wafer][ef]={}

#biasLookup[type][size][wafer][ef]={}
                             workbook = xlrd.open_workbook(efile)
                             #print workbook.sheet_names()
                             if    workbook.sheet_names()[0]    ==
"Data":

              sheetData,biasVals=self.parseDataSheet(workbook,bi
asCheck=(type,size,ef))

              data[type][size][wafer][ef]=sheetData

              biasLookup[type][size][wafer][ef]=biasVals
               return data, biasLookup
    def parseDataSheet(self,workbook,biasCheck=None):
               """
               Parses a data sheet from k4200 and returns data as
dictionary of data lists by header name
               """
               data={}
               biasVals={}

               worksheet =workbook.sheet_by_name("Data")
               cols=worksheet.ncols
                    for nrow in range(worksheet.nrows):
                    #worksheet.cell_value
                    row = worksheet.row(nrow)

                    #Get the header data
                    if nrow == 0:
                        header={}

                        for c in range(cols):
                         header[c]= str(row[c].value)
                         data[header[c]]=[]
                        if biasCheck != None:
                             (type,size,ef)=biasCheck
```

```
self.checkStoreBias(biasLen,type,size,ef,c-1,f)
                    #Get the rest of the data
                    else:

                        for c in range(cols):
                         data[header[c]].append(row[c].value)
                         #Lookup bias details
                         if nrow == 2:

                             #print data[type][size][wafer][ef]
                             if data[header[c]][0]==row[c].value:
                              biasVals[header[c]]=row[c].value
                              #print row[c].value
               #print data['Vg(1)']
               return data,biasVals

    def parseSettingsSheet(self,workbook,SMUS=4):
               """
               Parses a settings sheet from k4200 and returns data
as dictionary by signal name
               """
               settings={}
               testSettings={}
               sources={}

               worksheet =workbook.sheet_by_name("Settings")
               cols=worksheet.ncols
               col2name={}
                    for nrow in range(worksheet.nrows):
                    #worksheet.cell_value
                    row = worksheet.row(nrow)
                    if len(row)==2:
                         key=str(row[0].value)
                         testSettings[key]=row[1].value

                    elif len(row) >2:
                         if row[0].value == "Device Terminal":
                              terminals=row[1:]
                         elif row[0].value == "Instrument":
                              instrument=row[1:]
                         elif row[0].value == "Name":
                              for i in range(len(row)-1):
                                   col2name[i+1]=row[i+1].value

              settings[str(row[i+1].value)]={}
                         else:
```

```
                              for i,name in col2name.items():
               settings[str(name)][str(row[0].value)]=row[i].valu
e
               for i,name in col2name.items():
                    print i, terminals
                    settings[name]["Device
Terminal"]=terminals[i-1]
                    settings[name]["Instrument"]=instrument[i-1]

               self.settings=settings
               self.testSettings=testSettings
               print settings.keys()
               print settings["DrainV"]
               return settings,testSettings
    def data2mdmFile(self,data,biasVals,outputFile):
               settings=self.settings

               stream="""
! VERSION = 6.00
BEGIN_HEADER
 ICCAP_INPUTS
"""
               signal2name={}
               for signal in self.settings.keys():
               name=signal[0]
               if  settings[signal]["Forcing  Function"]=="Voltage
Bias":
                    type = "V"
                    forceType="CON"
                    values=[settings[signal]["Start/Level"]]


                    biased=signal

               biasValue=float(settings[signal]["Start/Level"])
               if     settings[signal]["Forcing     Function"]==
"Common":
                    type="V"
                    forceType="CON"
                    values=["0"]
               if settings[signal]["Forcing Function"]== "Voltage
Sweep":
                    type="V"
                    forceType="LIN"
                    print settings[signal].keys()

               values=["1",settings[signal]["Start/Level"],settin
```

```
gs[signal]["Stop"],settings[signal]["Number                    of
Points"],settings[signal]["Step"]]

                    swept=signal

                if     settings[signal]["Forcing     Function"]==
"Voltage Step":
                        type="V"
                        forceType="LIN"

values=["2",settings[signal]["Start/Level"],settings[signal]["St
op"],settings[signal]["Number                                  of
Points"],settings[signal]["Step"]]

                    stepped=signal

               compliance=settings[signal]["Compliance"]
               smu=str(settings[signal]["Instrument"].value)


               stream=stream+"  v%s        %s  %s GROUND %s %s %s
%s\n"
%(name.lower(),type,name,smu,compliance,forceType,"\t".join(valu
es))

              stream=stream+"""
 ICCAP_OUTPUTS
"""
              for signal in settings.keys():
               if settings[signal]["Measure I"] == "Measured":
                    name=signal[0]
                    stream=stream+"  i%s\tI %s  GROUND %s B\n" %
(name.lower(),name,str(settings[signal]["Instrument"].value))
                    measured=signal.replace("V","I")

              stream=stream+"""
END_HEADER

"""
              for step in range(int(settings[stepped]["Number of
Points"])):
               print step


              currentStep=float(settings[stepped]["Step"])*float
(step) + float(settings[stepped]["Start/Level"])
               stream=stream+"""
```

```
BEGIN_DB
"""
               stream=stream+"  ICCAP_VAR  v%s                 %s" %
(stepped[0].lower(),currentStep)
               stream=stream+"\n  ICCAP_VAR  v%s                %s" %
(biased[0].lower(),biasValue)
               for signal in self.settings.keys():
                    if signal not in [swept,stepped,biased]:

                         #TODO: do biases
                         stream=stream+"\n     ICCAP_VAR     v%s
%s" % (signal[0].lower(),"0")

               sweptkey="%s(%s)" % (swept,step+1)
               measurekey="%s(%s)" % (measured,step+1)


               stream=stream+"\n\n  #v%s                    i%s"  %
(swept[0].lower(),measured[0].lower())

               for i in range(len(data[sweptkey])):
                    stream=stream+"\n  %e                     %e" %
(data[sweptkey][i],data[measurekey][i])


               stream=stream+"""
END_DB
"""

               fp=open(outputFile,'w')
               fp.write(stream)
               fp.close()
################################################################
    def data2mdmFile_v3(self,data,biasVals,stream):
               settings=self.settings

               #stream="""
#! VERSION = 6.00
#BEGIN_HEADER
 #ICCAP_INPUTS
#"""
               signal2name={}
               for signal in self.settings.keys():
               name=signal[0]
               if  settings[signal]["Forcing  Function"]=="Voltage
Bias" and signal!="SubstrateV":
                    type = "V"
```

```
                    forceType="CON"
                    values=[settings[signal]["Start/Level"]]


                    biased=signal

               biasValue=float(settings[signal]["Start/Level"])
                if     settings[signal]["Forcing     Function"]==
"Common":
                    type="V"
                    forceType="CON"
                    values=["0"]
                if settings[signal]["Forcing Function"]== "Voltage
Sweep":
                    type="V"
                    forceType="LIN"
                    print settings[signal].keys()

               values=["1",settings[signal]["Start/Level"],settin
gs[signal]["Stop"],settings[signal]["Number                    of
Points"],settings[signal]["Step"]]

                    swept=signal

                 if     settings[signal]["Forcing     Function"]==
"Voltage Step":
                        type="V"
                        forceType="LIN"

values=["2",settings[signal]["Start/Level"],settings[signal]["St
op"],settings[signal]["Number                                  of
Points"],settings[signal]["Step"]]

                    stepped=signal

                compliance=settings[signal]["Compliance"]
                smu=str(settings[signal]["Instrument"].value)


                #stream=stream+"  v%s         %s  %s GROUND %s %s
%s                                                          %s\n"
%(name.lower(),type,name,smu,compliance,forceType,"\t".join(valu
es))

               #stream=stream+"""
 #ICCAP_OUTPUTS
#"""
```

```
               for signal in settings.keys():
                if settings[signal]["Measure I"] == "Measured":
                     name=signal[0]
                     #stream=stream+"  i%s\tI %s  GROUND %s B\n" %
(name.lower(),name,str(settings[signal]["Instrument"].value))
                     measured=signal.replace("V","I")

#              stream=stream+"""
#END_HEADER

#"""
               for step in range(int(settings[stepped]["Number of
Points"])):
                print step
               currentStep=float(settings[stepped]["Step"])*float
(step) + float(settings[stepped]["Start/Level"])
                stream=stream+"""

BEGIN_DB
"""
                stream=stream+" ICCAP_VAR v%s              %s" %
(stepped[0].lower(),currentStep)
                stream=stream+"\n ICCAP_VAR v%s            %s" %
(biased[0].lower(),biasValue)
                for signal in self.settings.keys():
                     if signal not in [swept,stepped,biased] and
signal!="SubstrateV":
                          #TODO: do biases
                          stream=stream+"\n     ICCAP_VAR     v%s
%s" % ("s","0")

                sweptkey="%s(%s)" % (swept,step+1)
                measurekey="%s(%s)" % (measured,step+1)
                stream=stream+"\n\n #v%s          %s         %s
i%s" % (swept[0].lower(), "ig", "ib", measured[0].lower())

                for i in range(len(data[sweptkey])):
                     stream=stream+"\n %e          %s
%s                        %e"  %  (data[sweptkey][i],"0",  "0",
data[measurekey][i])
                stream=stream+"""
END_DB
"""
               return stream
#              fp=open(outputFile,'w')
#              fp.write(stream)
#              fp.close()
```

```
##################################################################
    def data2mdmFile_v4(self,data,biasVals,stream):
                settings=self.settings

                #stream="""
#! VERSION = 6.00
#BEGIN_HEADER
 #ICCAP_INPUTS
#"""
                signal2name={}
                for signal in self.settings.keys():
                 name=signal[0]
                 if  settings[signal]["Forcing  Function"]=="Voltage
Bias" and signal!="SubstrateV":
                      type = "V"
                      forceType="CON"
                      values=[settings[signal]["Start/Level"]]


                      biased=signal

                biasValue=float(settings[signal]["Start/Level"])
                 if      settings[signal]["Forcing      Function"]==
"Common":
                      type="V"
                      forceType="CON"
                      values=["0"]
                 if settings[signal]["Forcing Function"]== "Voltage
Sweep":
                      type="V"
                      forceType="LIN"
                      print settings[signal].keys()

                values=["1",settings[signal]["Start/Level"],settin
gs[signal]["Stop"],settings[signal]["Number                    of
Points"],settings[signal]["Step"]]

                      swept=signal

                  if     settings[signal]["Forcing     Function"]==
"Voltage Step":
                          type="V"
                          forceType="LIN"

values=["2",settings[signal]["Start/Level"],settings[signal]["St
```

```
op"],settings[signal]["Number                                    of
Points"],settings[signal]["Step"]]
                    stepped=signal
               compliance=settings[signal]["Compliance"]
               smu=str(settings[signal]["Instrument"].value)
               #stream=stream+"  v%s         %s  %s GROUND %s %s
%s                                                      %s\n"
%(name.lower(),type,name,smu,compliance,forceType,"\t".join(valu
es))
               #stream=stream+"""
 #ICCAP_OUTPUTS
#"""
               for signal in settings.keys():
               if settings[signal]["Measure I"] == "Measured":
                    name=signal[0]
                    #stream=stream+"  i%s\tI %s  GROUND %s B\n" %
(name.lower(),name,str(settings[signal]["Instrument"].value))
                    measured=signal.replace("V","I")

#              stream=stream+"""
#END_HEADER

#"""
               for step in range(int(settings[stepped]["Number of
Points"])):
               print step
               currentStep=float(settings[stepped]["Step"])*float
(step) + float(settings[stepped]["Start/Level"])
               stream=stream+"""
BEGIN_DB
"""
               stream=stream+"  ICCAP_VAR  v%s              %s" %
(stepped[0].lower(),currentStep)
               stream=stream+"\n  ICCAP_VAR  v%s            %s" %
(biased[0].lower(),biasValue)
               for signal in self.settings.keys():
                    if  signal  not  in  [swept,stepped,biased]  and
signal!="SubstrateV":
                         #TODO: do biases
                         stream=stream+"\n     ICCAP_VAR     v%s
%s" % ("s","0")
               sweptkey="%s(%s)" % (swept,step+1)
               measurekey="%s(%s)" % (measured,step+1)
```

```
               stream=stream+"\n\n #v%s           i%s
%s              %s" % (swept[0].lower(), measured[0].lower(), "ig",
"ib")
               for i in range(len(data[sweptkey])):
                    stream=stream+"\n %e          %e
%s              %s" % (data[sweptkey][i],data[measurekey][i], "0",
"0")
               stream=stream+"""
END_DB
"""
              return stream
#             fp=open(outputFile,'w')
#             fp.write(stream)
#             fp.close()


#################################################################
#Extra addition: Read the mdm file, copy the header, truncate the
rest, and write the measured value

#################################################
    def xls2mdm_editing(self, mdmfile):
              stream = ""
              mdmfile.seek(0)
              for line in mdmfile:
               stream = stream + line
               if line == "END_HEADER\n":
                    break
              #mdmfile.seek(0)
              #mdmfile.truncate()
              return stream
#################################################################
    def data2mdmFile_v2(self,data,biasVals,stream):
              settings=self.settings
#             stream="""
#! VERSION = 6.00
#BEGIN_HEADER
 #ICCAP_INPUTS
#"""
              signal2name={}
              for signal in self.settings.keys():
               name=signal[0]
               if  settings[signal]["Forcing  Function"]=="Voltage
Bias":
                    type = "V"
                    forceType="CON"
```

```
                    values=[settings[signal]["Start/Level"]]

                    biased=signal

               biasValue=float(settings[signal]["Start/Level"])
                if     settings[signal]["Forcing     Function"]==
"Common":
                    type="V"
                    forceType="CON"
                    values=["0"]
                if settings[signal]["Forcing Function"]== "Voltage
Sweep":
                    type="V"
                    forceType="LIN"
                    print settings[signal].keys()

               values=["1",settings[signal]["Start/Level"],settin
gs[signal]["Stop"],settings[signal]["Number                    of
Points"],settings[signal]["Step"]]
                    swept1=signal
               swept=signal.replace(signal,"V"+signal[0].lower())
                 if     settings[signal]["Forcing     Function"]==
"Voltage Step":
                        type="V"
                        forceType="LIN"

values=["2",settings[signal]["Start/Level"],settings[signal]["St
op"],settings[signal]["Number                                  of
Points"],settings[signal]["Step"]]
                    stepped=signal
                compliance=settings[signal]["Compliance"]
                smu=str(settings[signal]["Instrument"].value)

                #stream=stream+"  v%s         %s  %s GROUND %s %s
%s                                                         %s\n"
%(name.lower(),type,name,smu,compliance,forceType,"\t".join(valu
es))

               #stream=stream+"""
 #ICCAP_OUTPUTS
#"""
               for signal in settings.keys():
                if settings[signal]["Measure I"] == "Measured":
                    name=signal[0]
                    #stream=stream+"  i%s\tI %s  GROUND %s B\n" %
(name.lower(),name,str(settings[signal]["Instrument"].value))
```

```
                measured=signal.replace(signal,"I"+name.lower())
                #stream=stream+"""
#END_HEADER
#"""
                measured=[]
                for step in range(int(settings[stepped]["Number of
Points"])):
                print step
                currentStep=float(settings[stepped]["Step"])*float
(step) + float(settings[stepped]["Start/Level"])
                stream=stream+"""

BEGIN_DB
"""
                stream=stream+"  ICCAP_VAR  v%s              %s" %
(stepped[0].lower(),currentStep)
                stream=stream+"\n  ICCAP_VAR  v%s            %s" %
(biased[0].lower(),biasValue)
                for signal in self.settings.keys():
                     if signal not in [swept1,stepped,biased]:

                          #TODO: do biases
                          stream=stream+"\n     ICCAP_VAR     v%s
%s" % (signal[0].lower(),"0")

                     if    settings[signal]["Measure    I"]     ==
"Measured":
                          name=signal[0]
                     #stream=stream+"  i%s\tI %s  GROUND %s B\n" %
(name.lower(),name,str(settings[signal]["Instrument"].value))

                measured.append(signal.replace(signal,"I"+name.low
er()))

                sweptkey="%s(%s)" % (swept,step+1)
                print sweptkey
                measurekey0="%s(%s)" % (measured[0],step+1)
                measurekey1="%s(%s)" % (measured[1],step+1)
                measurekey2="%s(%s)" % (measured[2],step+1)
                #stream=stream+"\n\n #v%s         i%s         i%s
i%s"                                                            %
(swept[0].lower(),measured[0].lower(),measured[1].lower(),measur
ed[2].lower())
                stream=stream+"\n\n #%s                          %s
%s                                                     %s"   %
```

```
(swept.lower(),measured[0].lower(),measured[1].lower(),measured[
2].lower())
               for i in range(len(data[sweptkey])):
                    #stream=stream+"\n %e          %e          %e
%e" % (data[sweptkey][i],data[measurekey][i])
                    stream=stream+"\n %e          %e          %e
%e"                                                            %
(data[sweptkey][i],data[measurekey0][i],data[measurekey1][i],dat
a[measurekey2][i])
               stream=stream+"""
END_DB
"""
              return stream
    def mdmfile_generator(self, stream, mdmfile):
              mdmfile.seek(0)
              mdmfile.truncate()
              mdmfile.write(stream)
              mdmfile.close()
#################################################################
    def
doFigure(self,dataSet,title,theSet,theX,theY,theBias,biasVal,bia
sList=[],simSet=None,biasLookup=None):
        theN=""
              xKey="%s" % (theX)
        yKey="%s" % (theY)
        bKey="%s(%s)" % (theBias,theN)
        doit=True
        markers={}
        markers["10"]=""
        markers["1"]="x"
        markers["4"]="v"
        markers["2"]="o"
        markers["8"]="t"
        noFig=True
        i=0
        wafers=dataSet.keys()
        wafers.sort()
        #print wafers
        lastStyle="-"
        lineStyle="--"
        lastAddr="999"
        vals=[]
        histlabels={}
              print "WAFERS", wafers

        for wafer in wafers:
                  print dataSet[wafer].keys()
```

```
                print theSet
            for dataset in dataSet[wafer].keys():
                   if dataset.find(theSet) == 0:
                        print "DATASET", dataset
                        try:
                         x=dataSet[wafer][dataset][xKey]
                         y=dataSet[wafer][dataset][yKey]
                        except:
                         print "ERROR: data does not exist in set,
check worksheet!"
                         if FATAL:
                             sys.exit(-1)
                         #sys.exit(-1)
                         print wafer, dataset, xKey, yKey
                         x=None
                         y=None

                        #if wafer.find("ka") == 0:
                        #    print "sjipped", wafer
                        print "PLOTTING WAFER", wafer
                        if x and y:
                             if noFig:
                              #print "Creating Figure"
                              pp.figure()
                              ax = pp.subplot(111)
                              noFig=False

                             #addr=wafer.split("_")[1]
                             #if marker in markers.keys():
                             #    marker=markers[]

                             #if addr != lastAddr:
                             #    cur=lineStyle
                             #    lineStyle=lastStyle
                             #    lastStyle=cur
                             #    lastAddr=addr
                             if (i < 7) and doit:

              ax.plot(x,y,label=wafer,linestyle=lineStyle )
                             #    print "plot1"
                             elif doit:

              ax.plot(x,y,label=wafer,linestyle=lineStyle,
marker = "o")
```

```
                             self.report.append('\t'.join(
[str(title),str(theSet),str(theBias),str(biasVal),str(wafer),str
(y[-1])]))                   vals.append(y[-1])
                             histlabels[y[-1]]=wafer
                             #    print "plot2"
                             i=i+1
                             #else:
                             #    print x, y
                             #
ax.plot(x,y,label=wafer.replace("_ua_","_uampu_").replace("_1_1"
,''))
              if simSet:
            #print simSet
            for simulator in simSet[theSet].keys():
                for corner in simSet[theSet][simulator].keys():
                    if                'i(vs)'                 in
simSet[theSet][simulator][corner].keys():
                        try:
                            x,y=
simSet[theSet][simulator][corner]['i(vs)'][biasVal]

ax.plot(x,y,linestyle="",label='simulated                 level3
'+corner,marker="x")
                        except:
                            print "Error! no simulation data for"
                            print theSet
                            print simulator
                            print corner
                            print 'i(vs)'
                            print biasVal, " : possibilities : ",
simSet[theSet][simulator][corner]['i(vs)'].keys()
                    else:
                        print "BADDDDDD"
                        print
simSet[theSet][simulator][corner].keys()
                        sys.exit(-1)
                        #sys.exit()
            #x,y,sig,typ,name=simSet
            #x,y=simSet[type]
        if noFig:
            return
        #pp.xlim(2)
        #pp.title(r'$\frac{32u}{2u}$    EPI    %s    @    %s=%sV'%
(theSet,theBias,bias) )
        pp.title(r'                       %s %s @ %s=%sV   )'%
(title,theSet,theBias,biasVal) )
        if theSet.find("Vgs") != -1:
```

```
            pp.xlabel(r"$V_{gs}$")
        else:
            pp.xlabel(r"$V_{anode}$")
        pp.ylabel(r"$I_{anode}$")
        # Shink current axis by 20%

        from matplotlib.font_manager import FontProperties #For
font on legends

        handles=[]
        labels=[]
        hand, lab = ax.get_legend_handles_labels()
        handles.extend(hand)
        labels.extend(lab)
        fontP = FontProperties()
        fontP.set_size('10')
        box = ax.get_position()
        ax.set_position([box.x0,   box.y0,   box.width   *   0.75,
box.height])
        ax.legend(handles,labels,'upper  left',bbox_to_anchor=(1,
1),prop=fontP)

        #pp.legend(loc='upper left')
        pp.savefig(self.ppdf, format='pdf')

        if DOHIST and self.ppdf2:

            pp.figure()
            pp.title(r'                      %s %s @ %s=%sV  )'%
(title,theSet,theBias,biasVal) )

            vals.sort()
            labels=[]
            valSet=[]

            for v in vals:
                valSet.append([v])
                labels.append(histlabels[v])

                #pp.hist([v],label=[histlabels[v]])
            pp.hist(valSet,label=labels)
            pp.legend()
            pp.savefig(self.ppdf2, format='pdf')

        self.report.append("Avg   %s   Mean   %s   StdDev   %s"   %
(numpy.average(vals),numpy.mean(vals),numpy.std(vals)))
```

```
    def plotSet(self,ef,Type,X,Y,S,skips=[],simData=None):
        for ttype in data.keys():
            for size in data[ttype].keys():
                #ef='IdsVds#1@1.xls'
                biasVals=[]
                #Find  all  of  the  possible  bias  steps  (real
numbers)
               if len(biasLookup[ttype][size].keys()) > 0:
                    for wafer in biasLookup[ttype][size].keys():
                        print
biasLookup[ttype][size][wafer].keys()
                        if                  ef                   in
biasLookup[ttype][size][wafer].keys():
                         for                  bl                 in
biasLookup[ttype][size][wafer][ef].keys():
                             if
biasLookup[ttype][size][wafer][ef][bl] not in biasVals:
                              if
biasLookup[ttype][size][wafer][ef][bl] not in skips:
                                  if
biasLookup[ttype][size][wafer][ef][bl] == "":
                                   print "FATAL: Incomplete data
in set %s in %s %s %s (Always Fatal, fix before continuing)" %
(ef,ttype, size,wafer)
                                   sys.exit(-1)
                                  else:

              biasVals.append(biasLookup[ttype][size][wafer][ef]
[bl])
                        else:
                         print "ERROR Data Missing for set %s in
%s  %s  %s  (Always  Fatal,  fix  before  continuing)"  %  (ef,ttype,
size,wafer)
                         sys.exit(-1)

                    biasVals.sort()
               else:
                    biasVals=['None']
               if len(biasVals) == 0:
                    biasVals=['None']

                for bias in biasVals:

                    title="%s %s" % (ttype,size)
                    if simData:
                        print simData[ttype].keys()
```

```
                        print                                size
theSimData=simData[ttype]["w="+size.replace("x","_l=")]
                    else:
                        theSimData=None
self.doFigure(data[ttype][size],title,Type,X,Y,S,bias,[],theSimD
ata,biasLookup[ttype][size])
```