12-2017

# Power Interface Design and System Stability Analysis for 400 V DC-Powered Data Centers

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Power Interface Design and System Stability Analysis for 400 V DC-Powered Data Centers

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a concentration in Electrical Engineering

by

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# ABSTRACT

The demands of high performance cloud computation and internet services have increased in recent decades. These demands have driven the expansion of existing data centers and the construction of new data centers. The high costs of data center downtime are pushing designers to provide high reliability power supplies. Thus, there are significant research questions and challenges to design efficient and environmentally friendly data centers with address increasing energy prices and distributed energy developments.

This dissertation work aims to study and investigate the suitable technologies of power interface and system level configuration for high efficiency and reliable data centers.

A 400 V DC-powered data center integrated with solar power and hybrid energy storage is proposed to reduce the power loss and cable cost in data centers. A cascaded totem-pole bridgeless PFC converter to convert grid ac voltage to the 400 V dc voltage is proposed in this work. Three main control strategies are developed for the power converters. First, a model predictive control is developed for the cascaded totem-pole bridgeless PFC converter. This control provides stable transient performance and high power efficiency. Second, a power loss model based dual-phase-shift control is applied for the efficiency improvement of dual-active bridge converter. Third, an optimized maximum power point tracking (MPPT) control for solar power and a hybrid energy storage unit (HESU) control are given in this research work. The HESU consists of battery and ultracapacitor packs. The ultracapacitor can improve the battery lifetime and reduce any transients affecting grid side operation.

The large signal model of a typical solar power integrated datacenter is built to analyze the system stability with various conditions. The MATLAB/Simulink™-based simulations are used

to identify the stable region of the data center power supply. This can help to analyze the sensitivity of the circuit parameters, which include the cable inductance, resistance, and dc bus capacitance. This work analyzes the system dynamic response under different operating conditions to determine the stability of the dc bus voltage. The system stability under different percentages of solar power and hybrid energy storage integrated in the data center are also investigated.

# ACKNOWLEDGMENTS

First and foremost, I would like to express my sincere appreciation to my advisor, Prof. H. Alan Mantooth, who inspires my study, work, and life so much with his insightful vision, broad knowledge, professionalism, and creative thinking. I benefit a lot from Prof. Mantooth not only in many good projects but also his great personalities and leadership. I really enjoyed my five years of study and work with Prof. Mantooth's guidance and mentorship. He will be an inspiring role model for my future career growth.

I am very grateful to my other committee members, Prof. Juan C. Balda, Prof. Simon S. Ang, and Prof. Roger Dougal for their technical assistance, valuable suggestions and helpful discussion during my Ph.D. study. I'd like to offer my special thanks to Prof. Balda for his technical support, time and encouragement for my Ph.D. project. I'd also like thank Prof. Ang for his help for my Little Box Challenge project. I want to thank Prof. Dougal, at the University of South Carolina, for his help regarding my projects in the GRAPES NSF research center.

I am thankful to all my colleagues with whom I have worked together on many interesting projects. I'd like to thank Chris Farnell and Sayan Seal in regard to the Arkansas Powerbox project. I also appreciate the help from my other professors, colleagues, and friends: Prof. Yue Zhao, Prof. Roy A. McCann, Prof. Shui-Qing (Fisher) Yu, Prof. Randy Brown, Mrs. Connie Howard, Dr. Tao Yang, Haoyan Liu, Janviere Umuhoza, Joe Moquin, Tavis Clemmer, Shuang Zhao, Audrey Dearien, Ramchandra Kotecha, Nan Zhu, Yusi Liu and Fahad Hossain. I'd also like to thank Dr. Liang Jia, Udaya Kiran Ammu, and Neilus O'Sullivan for their help and guidance during my internship at Google's Mountain View office.

I’d like to thank Shan Xu for supporting me through days and nights spent accomplishing my research work and making my Ph.D. study a happy journey.

Finally, and most importantly, I am extremely grateful to the University of Arkansas for supporting me during my Ph.D. Study.

# DEDICATION

This dissertation is dedicated to my parents, Naizhu Zhang and Xiange Guo. My heartfelt gratitude goes to them for their everlasting love, strength and support through my entire life. This dissertation is also dedicated to my brother, Yuhua Zhang and my sisters, Qingxiu Zhang, Qingmei Zhang, Guiqing Zheng, Xinhua Zhang.

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# CHAPTER 1

# INTRODUCTION AND THEORETICAL BACKGROUND

## 1.1 Background: The Challenge and Opportunity of Data Center Power Conversion

### *1.1.1 Quantity and capacity expansion of data centers*

The popularity of internet services and cloud computing is leading to continuous expansion of data centers. To meet the demands of high computation speed and data storage capacity, the quantity and capacity of data centers is rapidly increasing. Larger IT companies such as Microsoft, Google, Facebook, Alibaba, and Baidu are building more data centers around the world. At the same time, the energy required by data centers is climbing very quickly. The Lawrence Berkeley National Laboratory, in collaboration with experts at Stanford, Carnegie Mellon, and Northwestern published a figure showing the rising energy consumption by data centers, which is given in Fig. 1-1 [1.1]. In 2013, the electricity used by data centers increased to 70 billion kilowatt-hours (kWh). The amount of 70 billion kWh is close to 1.8% of total electricity usage in the U.S. in 2014. The report shows the electricity consumption is expected to continue increasing to up to 4% of total electricity usage of the U.S. by 2020.

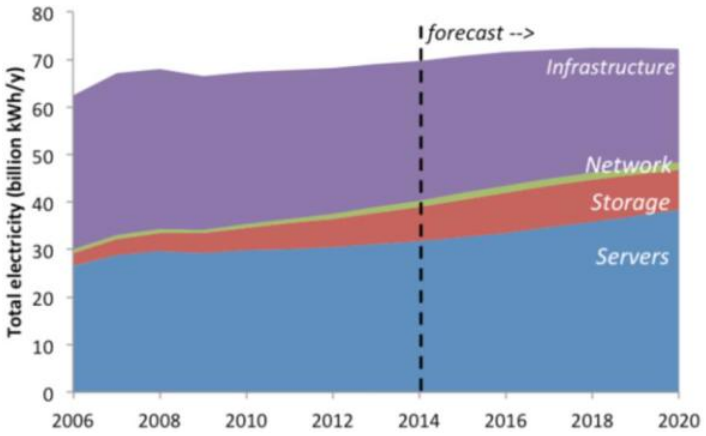


Fig. 1-1 Total Electricity Consumption of Data Centers in U.S. [1.1]

### *1.1.2 Climbing electricity price*

From the electricity data provided by the U.S. Energy Information Administration, illustrated in Fig. 1-2 [1.2], the energy prices are climbing every year. From 2001 to 2014, the average retail price of industrial electricity increased from 5.05 cents per kWh to 7.1 cents per kWh. For example, the actual monthly critical average power of a 10 MW data center often is 4-6 MW [1.3]. The monthly average power is selected as 5 MW. The industrial electricity price is 7.1 cents per kWh. If the power converter reaches 5% power loss reduction, then the electricity cost reduction will be $155,098 per data center per year, and the related cost will also be further reduced, like the costs of operational and cooling systems.

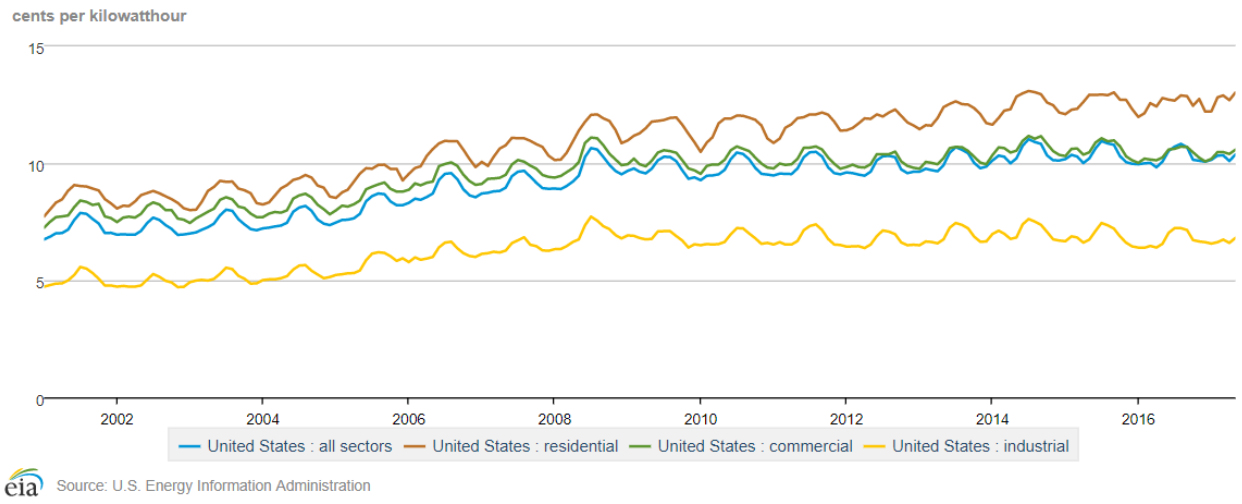


Fig. 1-2 Annual Average Retail Price of Electricity [1.2]

The efficiency is the key element to reduce the total power consumption, increase the power density and lead to small footprint of data centers. The design of high efficiency data centers includes power transmission, conversion, and distribution development.

### *1.1.3 High cost of data center power supply downtime*

Due to the power capacity and expansion of data centers, the reliability of data centers is becoming increasingly important. Due to the growing quantity and density of data centers, the consequences of outages are increasing. Emerson Company reports, data centers have an average downtime of 2.34 hours, and an average of 2.5 outages per year [1.4]. For 500,000 data centers, the Emerson Company estimated $2.84 million in annual outage costs for data centers. Designing a more reliable power supply would reduce expensive downtime and avoid associated costs.

To meet the requirements of high performance and low power loss, many researchers have been working on power topology development, integration with renewable energy, system level stability analysis, etc. The detailed research status is summarized in the following section.

## 1.2 Previous Research

### *1.2.1 Power distribution bus: 120 VAC or 400 VDC*

The typical efficiencies obtainable through the ac system technologies in data centers are given in Fig. 1-3. A traditional Uninterruptible Power Supply (UPS) architecture is utilized. It employs at least two stages. Ac voltage from the grid side is converted to dc voltage first. An energy storage device, like lead-acid batteries, is connected to the dc bus. The dc bus is then inverted to an ac bus which is the Power Distribution Unit (PDU). The advantage of this traditional four stages architecture is robustness. However, the end-to-end efficiency is a relatively low 71%. From article [1.3], about 15% of data center's power is wasted and dissipated as heat.

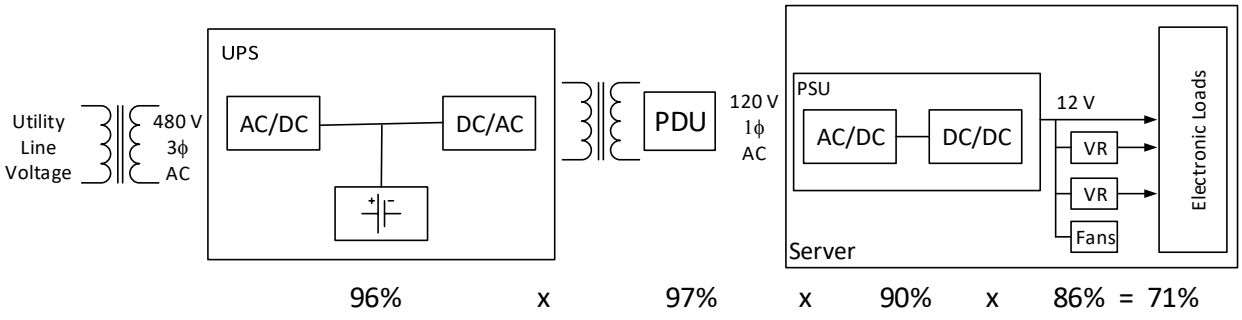


Fig. 1-3 Traditional ac Distribution Efficiency

Dc distribution is attractive, it eliminates at least one power inversion stage, resulting in higher efficiency. The efficiency performance of dc distribution is shown in Fig. 1-4. Compared with the ac distribution, the efficiency is improved from 71% to 90%. This 19% efficiency increase leads to significant cost reduction of the cooling system. What's more, as the power distribution voltage is increased to 400 V dc, the conduction loss can be reduced, allowing the use of lighter and more economic cables. The power cable comparison between 48 V dc and 400 V dc is shown in Fig. 1-5.

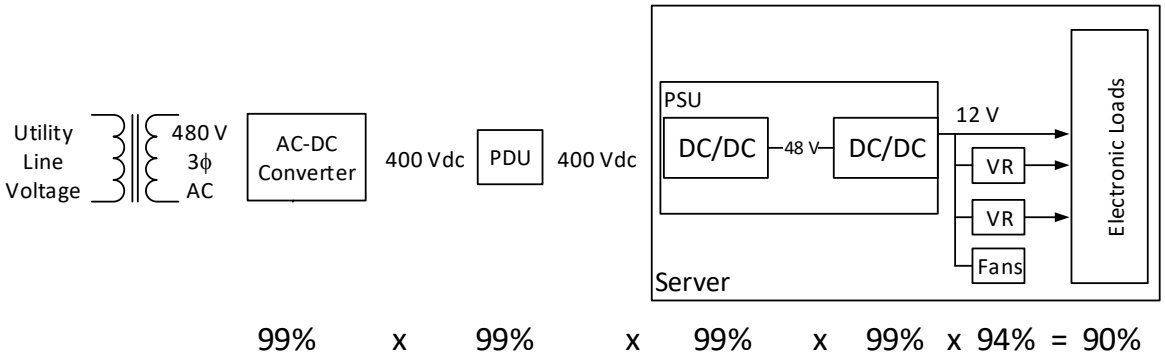


Fig. 1-4 Efficiency of 400 V DC Distribution Architecture


Fig. 1-5 Cable Size Comparison between 48 V and 400 V with 100 kW Load

Another merit of the dc distribution architecture is its ease in integrating with distributed energy sources, such as solar photovoltaic, wind turbine, fuel cell, etc. In current commercial technologies, dc equipment is available, but the costs are higher than comparable ac equipment.

In this dissertation, a 400 V bus is selected due to higher efficiency consideration. The power topology development and design is analyzed and designed in detail in Chapters 2 to 5.

### *1.2.2 Integration with renewable energy and stability consideration*

Usually, data centers are built in a place with reliable and sustainable sources of power; protected from hazards, environment friendly and so on. Unfortunately, those places are not the best choice for renewable energy generation where the data center has better efficiency

performance. What's more, data center operation needs reliable power, but solar power is only available during the daytime and wind power is only available when the wind is blowing. The truth of the 'Green Data Center' mentioned from the industrial side is that these companies purchase at least an equivalent amount of power from renewable energy companies and sell the energy back into the grid at a wholesale price [1.3]. Given the large size of many data centers, the large roofs offer excellent real estate for solar panel placement. This dissertation considers solar panels on the roof as green power and utilizes energy storage to reduce the electricity cost and the non-green emissions from the grid. Due to the randomness and fluctuation of solar power generation, the effects to the system stability will be investigated in this dissertation.

### *1.2.3 Energy storage in data center*

Energy storage, such as batteries, play an important role in the UPS system. It supplies the uninterrupted power to critical loads. Power transients, due to solar irradiance transients or load changes, need to be smoothed by the energy storage. Lead-acid batteries are widely used in the data center due to their low cost. However, rapid charging and discharging degrade the life expectancy of a battery pack. To overcome this drawback, ultracapacitor packs are considered in this work. The ultracapacitor application market is shown in Fig. 1-6 [1.5]. The global ultracapacitor consumption is fast growing. This market is expected to grow from $500M in 2015 to $1.5B around 2020. One type of ultracapacitor module from Schneider is shown in Fig. 1-7. With more technological advancements, both the cost and maintenance of ultracapacitors have gone down.

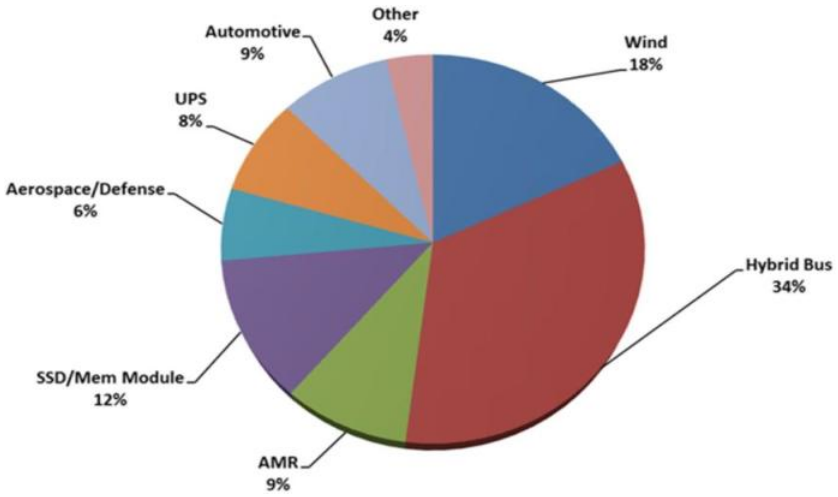


Fig. 1-6 Ultracapacitor Consumption by Market [1.5]

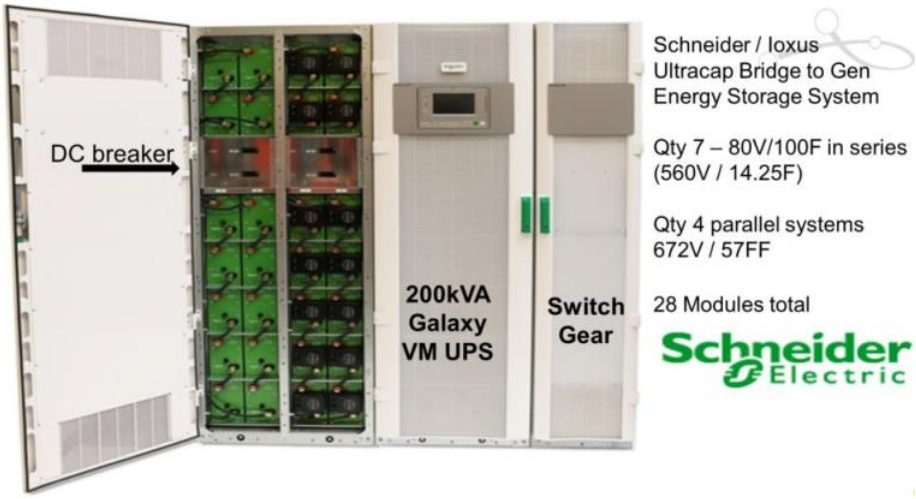


Fig. 1-7 Ultracapacitor Module from Schneider [1.5]

Ultracapacitors allow more charge/discharge cycles and have a higher power density, which are desirable for fast power smoothing. In this dissertation, an investigation is conducted for the design of high frequency ripple reduction and battery lifetime improvment, which are both compensated by ultracapacitors.

## 1.3 Proposed 400 V DC-powered Data Center with Solar Power Integration

As mentioned, the traditional ac bus data center configured as shown in Fig. 1-8 has low efficiency in the distribution unit. For high efficiencies and high power densities, high-power dc distribution, such as 400 V in DC-powered data centers, is becoming more attractive. Due to the high power levels of data centers, the input of the ac/dc converter is usually connected to a medium-voltage power grid through bulky low-frequency step-up transformers. Recently, high-frequency transformers in multilevel converters are investigated due to their small size, light weight, high power density and capability for integrating multiple functions [1.6][1.7]. The proposed 400 V DC-powered data center is shown in Fig. 1-9. Compared with traditional ac bus data centers, the low-frequency transformer is replaced by a solid-state transformer and the power distribution is improved with a higher voltage 400 V bus, thus the current in the bus bars are decreased. The conduction power loss and cable cost in the distribution bus bars are reduced as well. To reduce the voltage stresses on switches and increase the current carrying capabilities, different multilevel converter topologies have been investigated by various groups [1.8][1.9]. Some topologies utilize high breakdown voltage IGBTs. However, IGBTs are inherently slow devices and have a tail current. The tens of kV power MOSFETs are rarely available in the market and mostly under investigation in the research environment. For high efficiency and switching speed considerations, commercial SiC power MOSFETs rated from 0.9 kV to 1.7 kV are adopted in this paper.

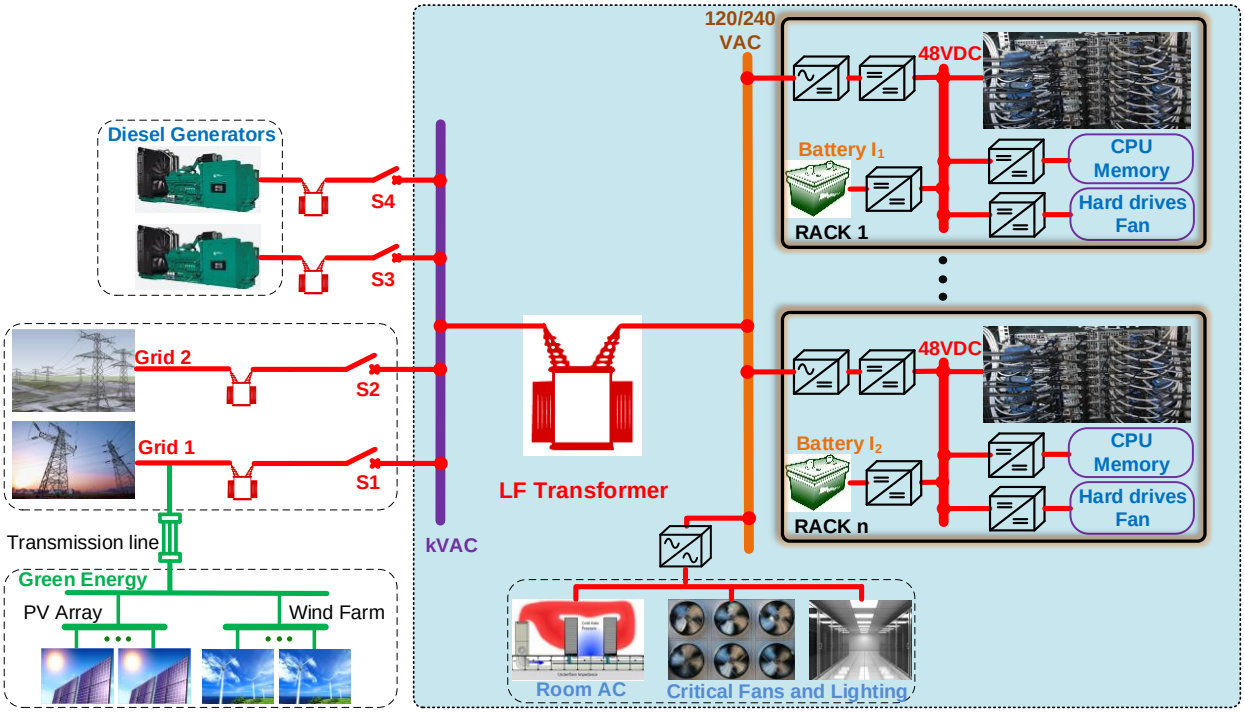


Fig. 1-8 Conventional AC-powered Data Center

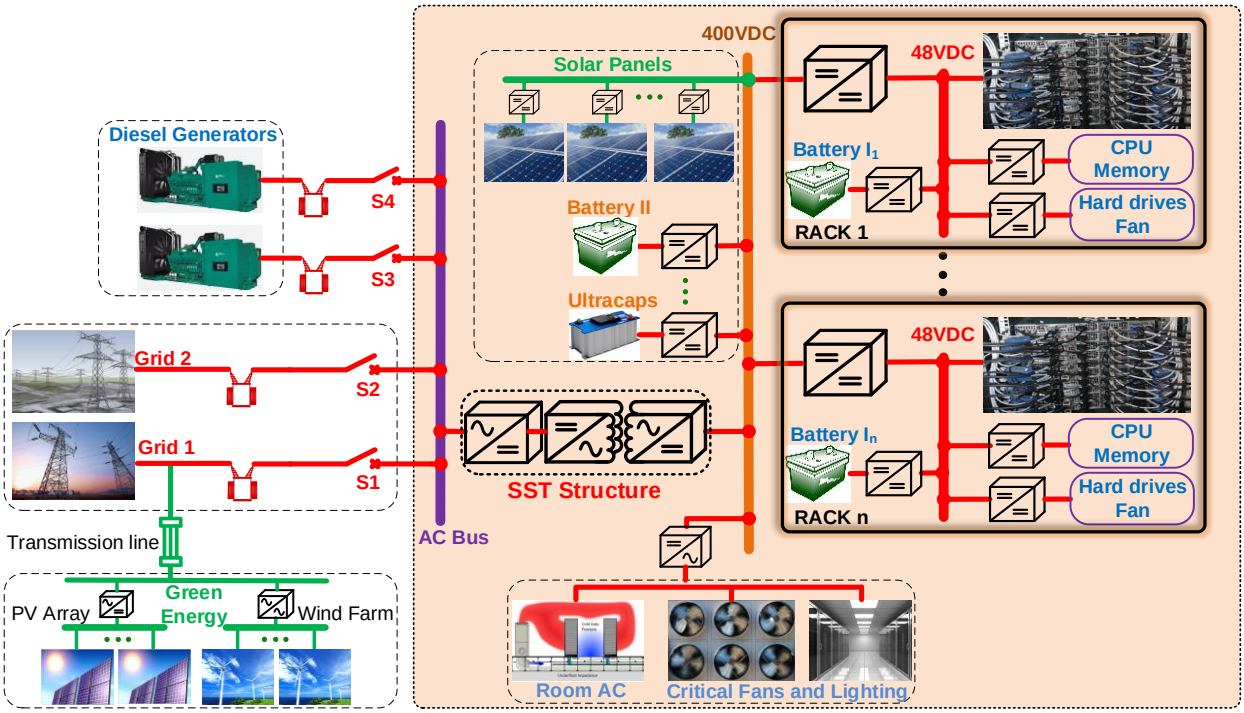


Fig. 1-9 400 V DC-powered Data Center Integrated with Solar Power and Energy Storage

Furthermore, to build a real ‘green’ data center and reduce the energy consumption from grid side, in the evaluated system the locally produced solar power is interfaced to the 400 V dc bus through dc/dc converters. To maintain the 400 V dc bus, the battery and ultracapacitor packs are interfaced with the same 400 V dc bus through dc/dc converters. A high-power active-front-end rectifier is utilized at the grid side. The existing 48 V telecom power supply is recognized as a more economical and practical option. To minimize the revision from the existing power supply in data center, 48-V dc bus is kept in the rack. The battery as back-up energy is on the 48-V dc bus as well. A dc/dc converter steps down 400 V to 48 V in the server racks.

## 1.4 Problem Definitions

There are many research topics in a data center. The high reliability, efficiency and green data center are identified as the main topics in this dissertation.

### *1.4.1 Topology consideration*

#### *1.4.1.1 The issue in ac/dc voltage conversion*

For ac/dc voltage conversion, Power Factor Correction (PFC) converters are widely adopted. The most popular and conventional PFC converter is the diode bridge rectifier in series with a boost converter. The benefit of this topology is that just one switch needs to be controlled. The drawback is that at least two diodes are on in every power delivery circle, leading to inefficient power conversion. Some soft-switching controllers are investigated to reduce the reverse recovery of Si diodes [1.10][1.11]. Complicated auxiliary circuits and more complex controls are needed to realize soft-switching.

#### *1.4.1.2 Proposed solution for ac/dc voltage conversion*

In this dissertation, two different types of bridgeless PFC converters are carefully compared with the diode full bridge rectifier. The dual boost bridgeless PFC (DBP) converter has better efficiency performance by reducing the conduction loss on the diodes. It requires more components, which means the need of auxiliary gate drivers and higher cost. Two high frequency diodes are required in the DBP converter.

Another bridgeless PFC converter is the totem-pole bridgeless PFC (TPBP) converter. The challenge of TPBP converter is that it usually works in discontinuous-current mode (DCM) or critical-current mode (CRM) due to efficiency consideration. The poor reverse recovery time of MOSFETs are reduced in SiC MOSFETs and the on-state resistance of SiC MOSFETs are also less than the Si MOSFET. These two features allow the TPBP converter to work in continuous-current mode (CCM) with much greater efficiency. The TPBP converter has the lowest volume of components. If the two diodes in the TPBP converter are switched at ac voltage frequency, then the power loss is further reduced.

### ***1.4.2 Controller consideration: Proportional-Integral Control vs Model Predictive Control***

#### *1.4.2.1 The issue in controller design for load or voltage transient*

In the power supply design of power converters for data center applications, the transient response capability is the key requirement. The conventional proportional-integral (PI) control is very popular in the area of power converter controller design. Usually, it has two loops: voltage loop and current loop. The challenge in regarding PI controllers is that different load power or voltage transient needs different phase and gain compensation, thus the controller design varies

from light load to heavy load. What's more, the controller complexity is increased if compensating for the aforementioned load variances.

#### *1.4.2.2 Proposed solution for transient performance*

To overcome these disadvantages, a model predictive control (MPC) is proposed in this dissertation. MPC is a real time control algorithm. It predicts the expected control variable and determines the optimized control period. The mathematical model of the controlled converter is utilized in MPC control. Different from the conventional PI control, the frequency of MPC control is variable which is dependent on the feedback. However, the maximum frequency can be less or equal to the conventional PI control, thus MPC can improve the efficiency. Another merit of MPC is that the multi-goal control can be realized. The coefficient of different goals need to be investigated.

### ***1.4.3 Efficiency consideration***

#### *1.4.3.1 Issue in power conversion efficiency*

The typical total energy usage of a conventional datacenter includes the IT equipment, cooling system, uninterrupted power supply (UPS), power distribution, and ancillary systems. The detailed percentages of different power consumption is given in Fig. 1-10. The power usage effectiveness (PUE) presents the ratio of IT power to the total power, which reflects the efficiency of a datacenter infrastructure. The IT power is the power consumed by the servers. The power converter is the key factor to improve the power efficiency, thus guaranteeing lower PUE. Many researches have been working on the efficiency improvement in power converters in the data center, such as development of new power topology, soft switching, control strategy, etc. For example, there are two popular efficiency improvement methods for the isolated dc/dc power converter known as the

dual-active bridge (DAB). The first method is a current stress optimizing algorithm and the second is a flow-back power minimization strategy. The DAB is used in final stage of the proposed topology in this work.

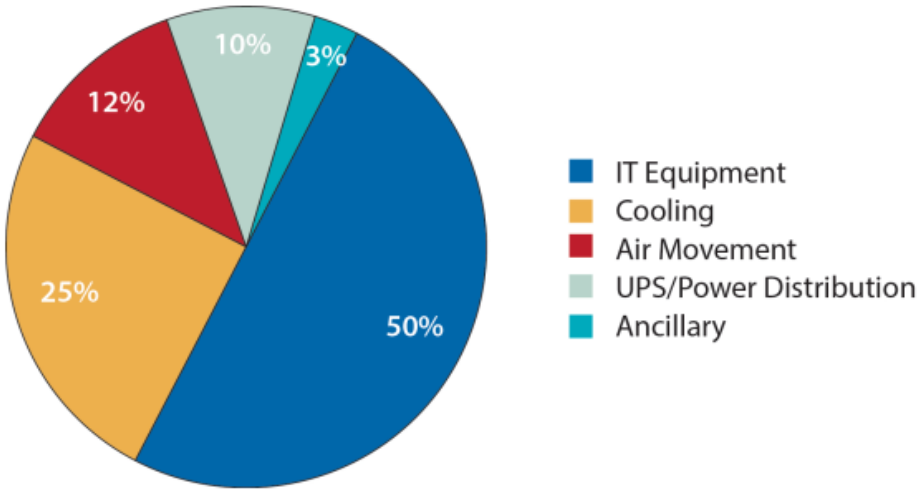


Fig. 1-10 A Typical Power Losses in a Data Center [1.3]

### *1.4.3.2 Proposed solution for efficiency improvement*

In this dissertation, the improvement of the efficiency performance in a dual-active bridge for the data center power supply is discussed. Different from the reported methods, an accurate loss model is developed in this work for the power converter to find the expected phase-shift angle for the switches. The accurate loss model method is developed from three aspects which are the conduction loss model, switching loss model, and a high frequency transformer loss model. The better loss model leads to the more accurate prediction of phase-shift in the dual-active bridge, and thus smaller losses.

### *1.4.4 Green data center*

#### *1.4.4.1 Issue in current 'green' data centers*

The integration of solar power and data centers can highly reduce the electricity cost and emissions of data centers. However, solar power is not stable and heavily depends on the environment. Battery energy storage has relatively high energy density. It is usually utilized to smooth the power output from solar systems. However, the lifetime of batteries is a major issue, leading to cost increases.

#### *1.4.4.2 Proposed solution for ac/dc voltage conversion*

The ultracapacitor has a high power density and can be quickly charged and discharged without harming its lifetime. In this dissertation, the battery and ultracapacitor are used as hybrid energy storage devices to smooth the solar power. The controller design for each energy storage device is developed as well to achieve high performance.

## 1.5 Outline

Chapter 2 describes the rectifier power stage and the control strategies for the cascaded totem -pole PFC converter. The conventional PI control design and the proposed model predictive control are developed, analyzed and compared. A discrete time mode of a cascaded totem-pole PFC converter is derived and utilized to design the model predictive control. The control goals include unity power factor, dc bus voltage balance, power loss minimization, etc.

Chapter 3 illustrates the dc/dc stage in the proposed topology. The operation principle of a dual-active bridge converter is analyzed. The single and dual phase-shift control is compared. To improve the efficiency performance, the backflow power reduction and current stress minimization methods are given. The loss model optimization method is proposed to achieve better efficiency

performance. Simulation and testing results are given to verify the proposed control strategy. For the control of transient performance, the conventional PI control and proposed K-factor control are designed and compared. A scaled-down prototype is tested to verify the proposed K-factor control.

Chapter 4 is about the solar power and hybrid energy storage integration in the data center. The controllers for solar power, battery, ultracapacitor and data center loads are developed. The simulation results are given to validate the effectiveness of the proposed topology and its control strategies.

Chapter 5 shows the system level stability analysis of a data center. The large signal model of a large-scale data center is built. The stability criterion is introduced and the stable region is given through the MATLAB/Simulink$^{TM}$ simulation results.

Chapter 6 is the summary of this dissertation and the outlook of the future work.

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# CHAPTER 2

# DESIGN, MODELING AND CONTROL OF RECTIFIER STAGE

## 2.1 Introduction and Motivation

### *2.1.1 Ac/dc voltage conversion with low-frequency transformer*

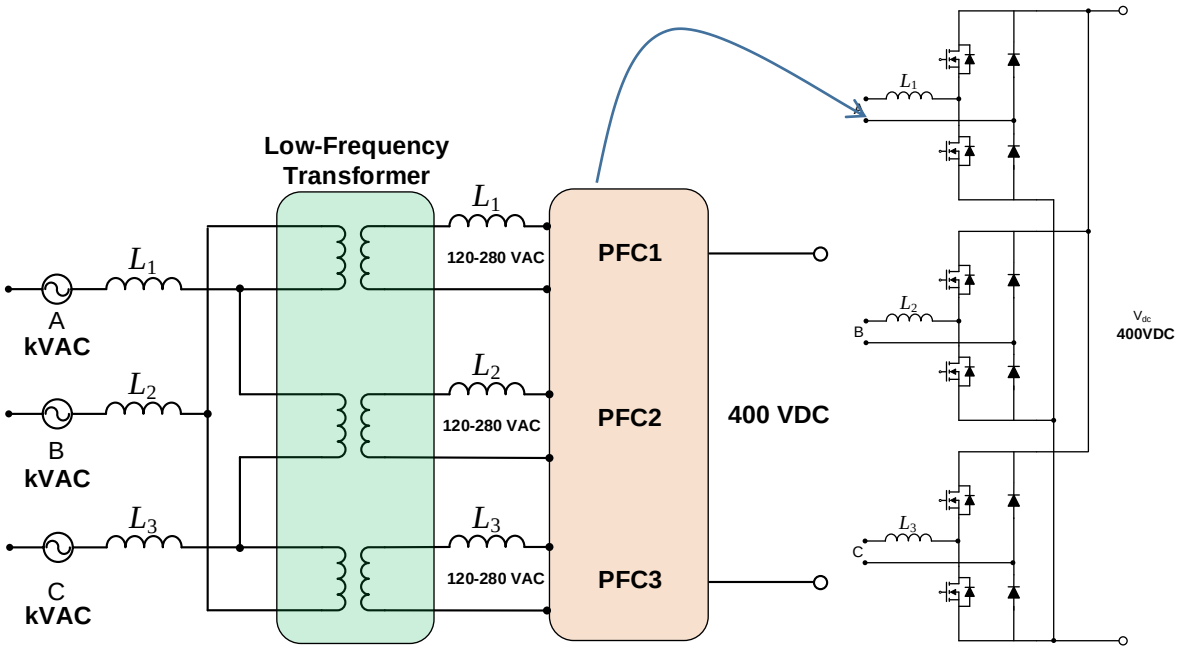
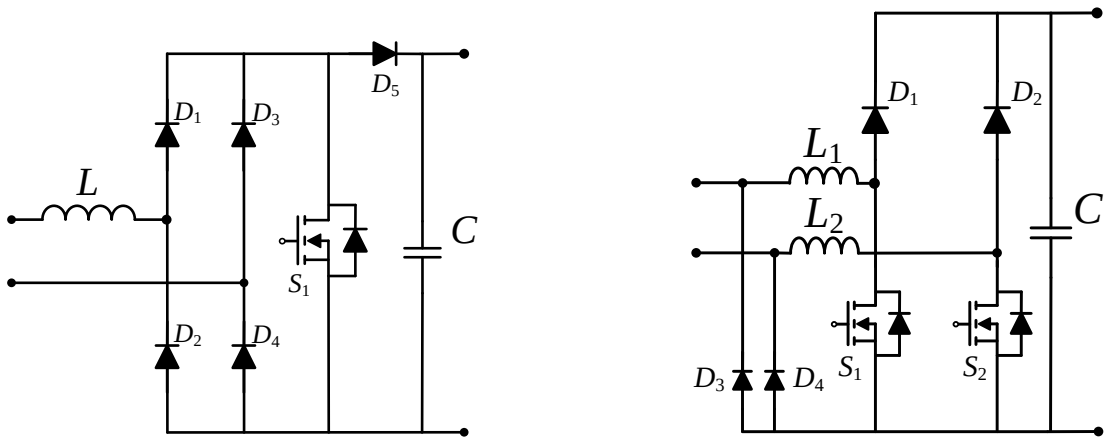



Fig. 2-1 Ac/dc Power Conversion: with Low-Frequency Transformer Application

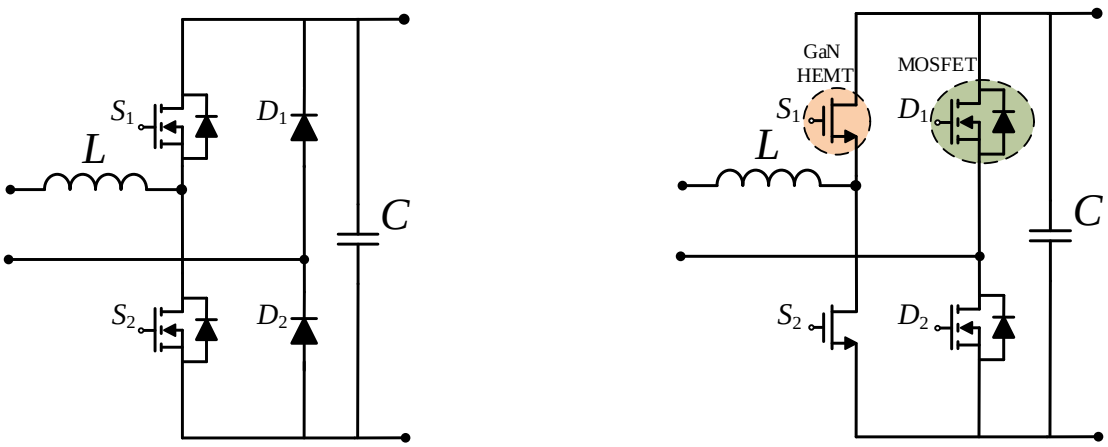
A typical system configuration is shown in Fig. 2-1. A Low-Frequency Transformer (LFT) is utilized to step down the high ac voltage to the low ac voltage, then the low ac voltage is rectified to 400 V dc. To reduce the voltage stress and increase the current carrying capability, each PFC topology can be connected in series or parallel. For single-phase ac/dc voltage conversion in data centers, the Power Factor Correction (PFC) converter is widely adopted. The conventional PFC converter is diode bridge rectifier. The efficiency needs to be improved for these devices due to

the power loss from diodes. To eliminate the requirement of using a diode bridge rectifier, bridgeless PFC topologies are reviewed. There are two popular topologies: Dual-boost Bridgeless PFC (DBP) which is shown in Fig. 2-2 (a) and totem-pole bridgeless PFC (TPBP) which is given in Fig. 2-3 [2.1]-[2.3]. Both DBP and TPBP have only two switches conducting in every cycle. Compared with the classic PFC converter, the DBP converter has good efficiency performance, but it needs two more choke coils and two more diodes to reduce the large common-mode noise, thus the size and cost are increased. Due to the poor reverse recovery performance of the body diode in Si switches, the TPBP topology did not attract widespread implementation in the past, especially in the continuous-current mode (CCM). With the advent of wide bandgap devices, such as GaN or SiC switches, which have very good reverse recovery characteristics and relative low on-state resistance [2.4]-[2.6], the TPBP topology has better efficiency performance and has attracted more widespread attention [2.7]-[2.9]. If the two diodes are replaced by two active switches, the conduction loss caused by diodes can be further reduced.




(a) Classic Boost-type Rectifier (b) Dual-Boost Bridgeless PFC

Fig. 2-2 Classic Boost-type Rectifier




(a) Totem-pole Bridgeless PFC (b) Totem-pole Bridgeless PFC with SiC and GaN Devices

Fig. 2-3 Totem-pole Bridgeless PFCs with Wide Bandgap Devices

The four typical types of PFC stage are summarized in Table 2.1. To further investigate the efficiency performance of different PFC converters, the efficiency simualtion is performed in the simulator PLECS$^{TM}$. Three toplogies are adopted in the simuation: (a) Classic boost-type rectifier, (b) Dual-Boost Bridgeless PFC, and (c) Totem-pole Bridgeless PFC only with one leg using SiC MOSFETs. The power loss model of the MOSFET is from Wolfspeed which is built in PLECS$^{TM}$. The efficiency simulation results are shown in Fig. 2-4. It shows that the totem-pole PFC converter has the highest efficiency performance.

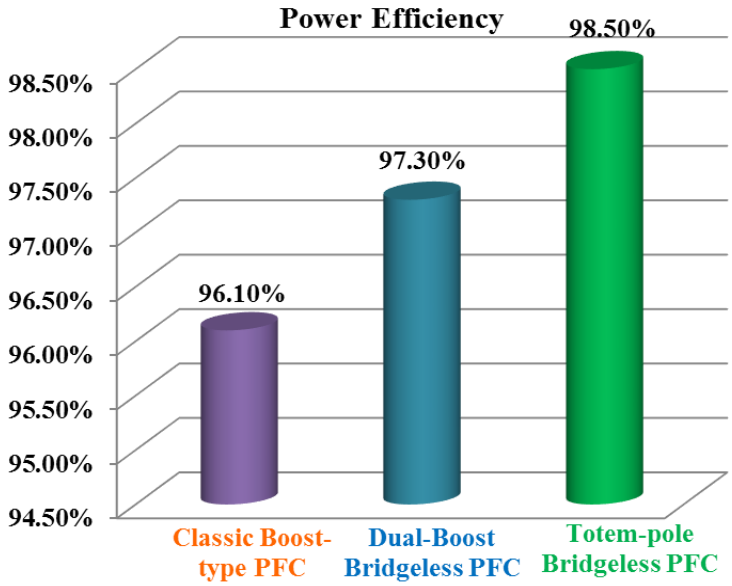



Fig. 2-4 Simulation Results of Efficiency Comparison: 240 V ac to 400 V dc with 5 kW Load

Table 2.1 Comparison of Three Typical PFC Converters

| Topology | (1) Classic PFC | (2) Dual-Boost Bridgeless PFC | (3) Totem-pole Bridgeless PFC without GaN | (4) Totem-pole Bridgeless PFC with GaN |
|---|---|---|---|---|
| Number of components | 7 | 8 | 5 | 5 |
| Device | 5 Si Diodes<br>1 Si MOSFET<br>1 Inductor<br>1 Capacitor | 4 Si Diodes(2 are grid voltage frequency, 2 are switching frequency)<br>2 Si MOSFETs<br>2 Choke Inductors<br>1 Capacitor | 2 SiC Diodes (grid voltage frequency)<br>2 SiC MOSFETs<br>1 Inductor<br>1 Capacitor | 4 GaN FETs or<br>4 SiC MOSFETs<br>1 Inductor<br>1 Capacitor |
| Loss on Diodes | 1 recovery and 2 conduction losses | 1 recovery and 2 conduction losses | 1 conduction loss | None |
| Efficiency | 95-97% | 96-97% | 97-98% | 98-99% |

### *2.1.2 Ac/dc voltage conversion with high-frequency transformer*

The disadvantage of Fig. 2-1 is the necessity of a large foot print, high weight and bulky transformer. High-frequency transformers attract attention due to their small size, light weight and high power density. They also can work as both a bus bar voltage regulator and a reactive power compensator. The challenge of using high-frequency transformers is that the control complexity is increased and more semiconductor devices are needed. However, the cost of high-frequency transformers is high and the efficiency is somehow lower than the low-frequency transformer. The system configuration with a medium- or high-frequency transformer is given in Fig. 2-5.

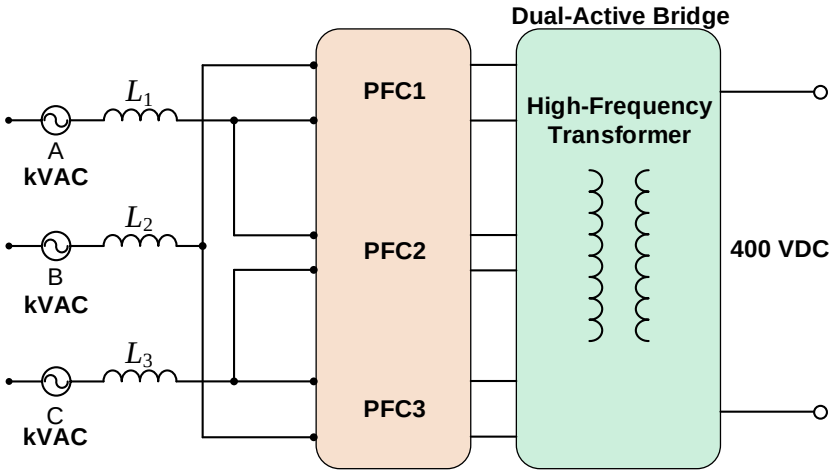



Fig. 2-5 System Configuration Using Medium- or High-frequency Transformer

The PFC converter in high-frequency transformer applications can be divided to three types as shown below.

#### *2.1.2.1 Non-modular topology*

In the non-modular topology, it usually requires high breakdown voltage rated switches to rectify high ac voltage to dc voltage. The advantage of this topology is that less switches are required and which leads to less complexity and control effort. For example, a five-level ac/dc

topology is given in Fig. 2-6, which is reported by ETH Zurich [2.10]-[2.12]. The voltage stresses of switches are relatively high and it usually requires many switches connected in series to increase the breakdown voltage. Thus, the auxiliary driver circuits are required to symmetrically turn-on or off the switches.

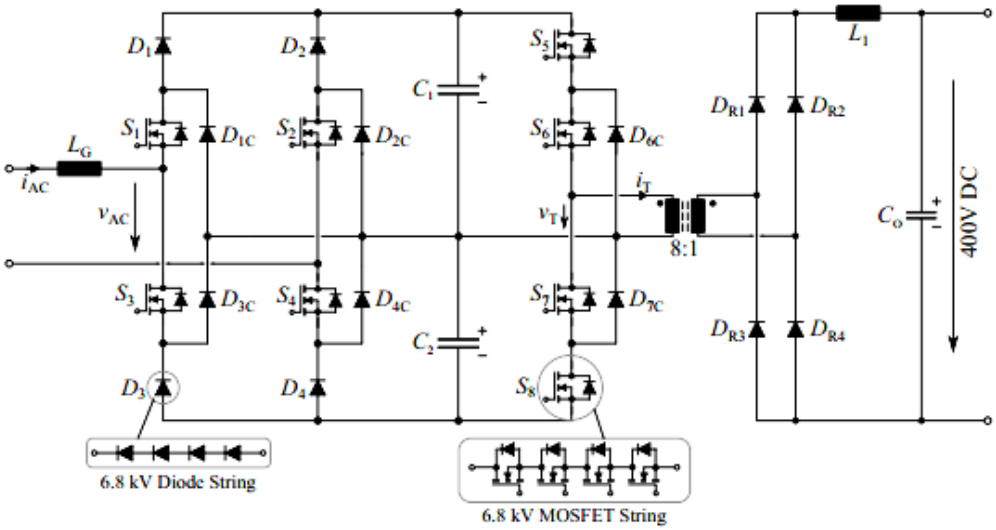


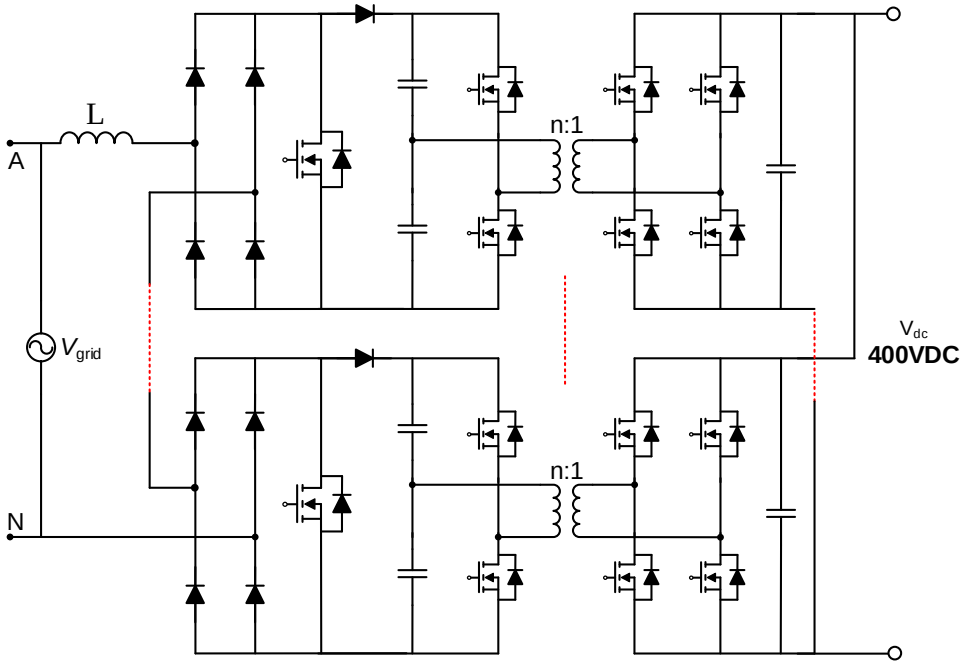

Fig. 2-6 Five-level NPC ac/dc Topology

### *2.1.2.2 Modular multilevel topology*

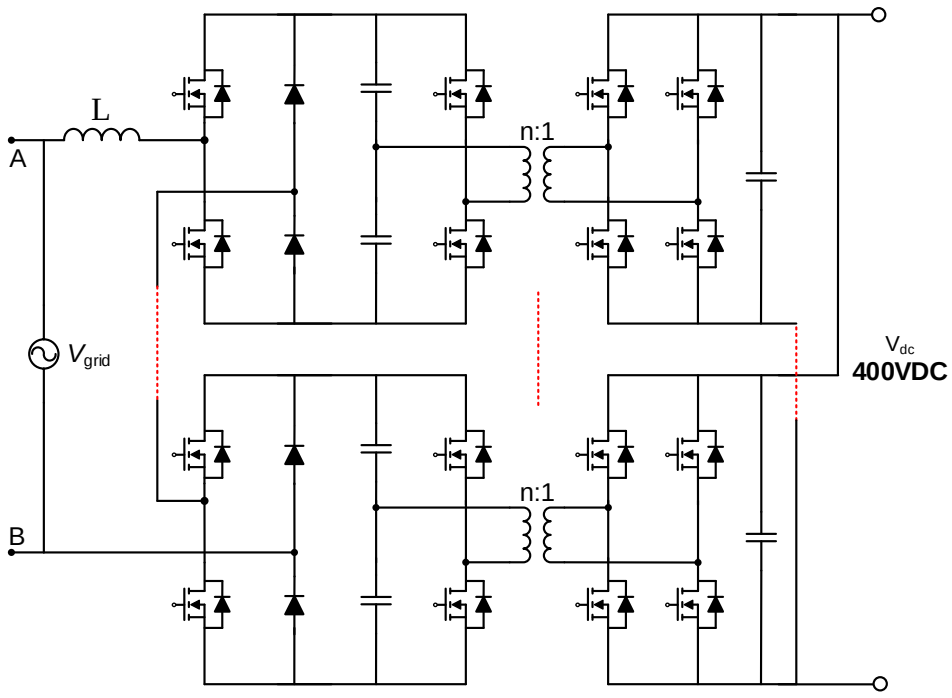
The modular multilevel topology attracts attention due to it being scalable and modular. The voltage stress is decided by the amplitude of input ac voltage level and the levels of modulation. Low voltage switches can be utilized in this topology. Three typical topologies are shown in Fig. 2-7. To reduce the number of switches and further improve the efficiency performance, a cascaded bridgeless totem-pole PFC through a dual-active bridge feeding a common 400-V dc bus is proposed as shown in Fig. 2-7 (b) and (c). Different from most of the recent literature, which is focused on the single TPBC or interleaved TPBC [2.13]-[2.15], is that there are several totem-pole bridgeless PFC converters connected in series. The dc voltage will be divided by the number of PFC converters. Hence, voltage stresses of the switches can be reduced to a more managable value.

For example, if the PFC output voltage is controlled to 400 V, then 650 V rated devices can be utilized. The output voltage of PFC converters are integrated with dual-active bridges connected in parallel to increase the current capability. The galvanic isolation is provided by high-frequency transformer. There are two differences between Fig. 2-7 (b) and (c): (1) Si MOSFET is replaced by wide bandgap devices such as GaN or SiC, to overcome the reverse recovery problem; (2) Diodes are replaced by Si MOSFETs for better efficiency performance.

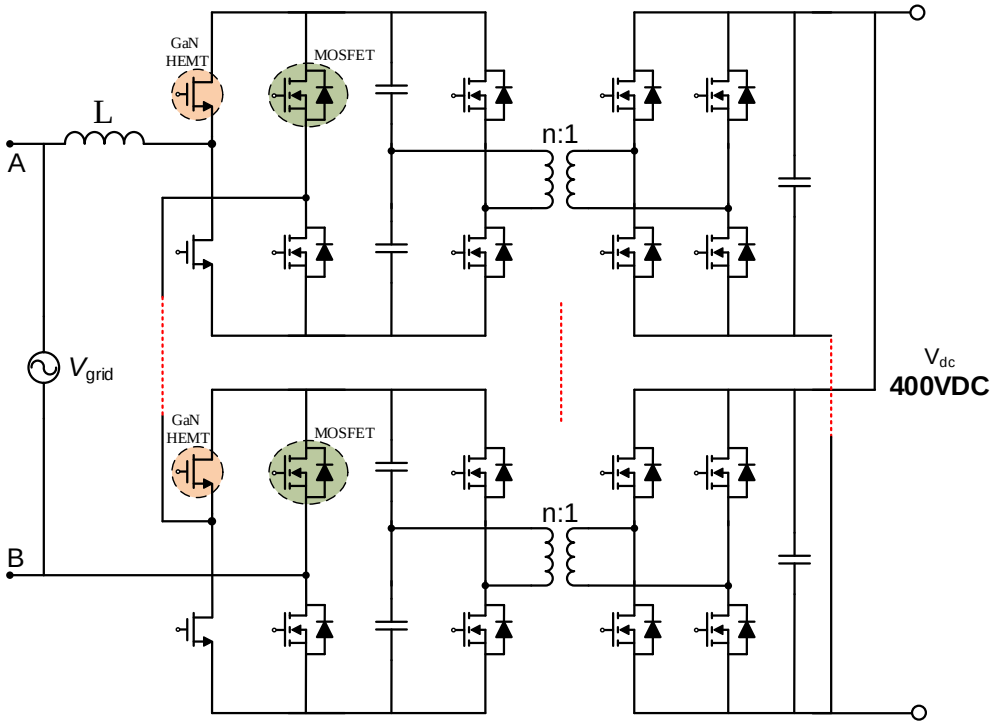
In the dc/dc stage, cascaded totem-pole converters convert grid voltages to primary dc-bus voltages $v_{oi}$ dual-active bridges, whose outputs are connected in parallel to increase the current capability, produce a secondary dc output voltage. In the dual-active bridge stage, it can be a half-bridge or a full-bridge on the primary or secondary side. Regarding the kV-level input ac voltage, the full-bridge of the DAB primary side may be replaced by a half-bridge topology to further reduce the high-frequency transformer turns ratio.




(a) Series Diode Bridge and Boost PFC




(b) Proposed Series Totem-pole Bridgeless PFC with SiC MOSFET




(c) Proposed Series Totem-pole Bridgeless PFC with GaN HEMT and Si MOSFET

Fig. 2-7 Modular Multilevel PFC Converters

*2.1.2.3 Hybrid topology*

As shown the configuration of Fig. 2-8 [2.11], the input ac of the hybrid topology is rectified by a diode full bridge, then through a modular isolated dc/dc converter to generate the dc bus to loads. The diodes, with appropriate voltage ratings, are required in the hybrid topology.

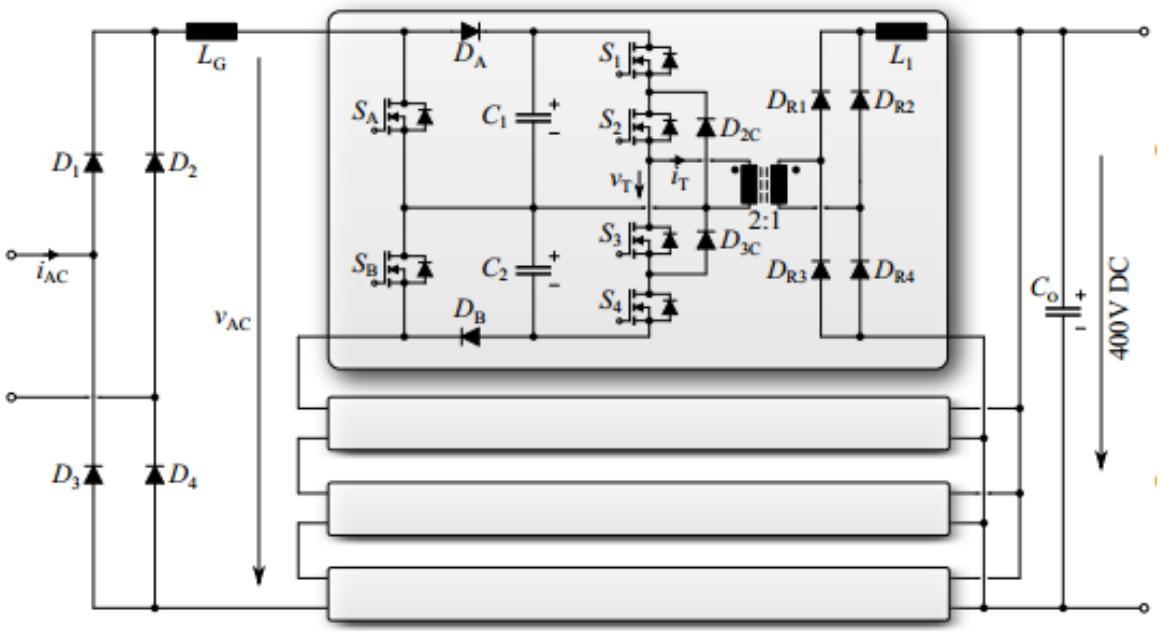



Fig. 2-8 Multi-Cell Boost Topology with Four Input Series Output Parallel Connected Converter

In summary, a modular multilevel H-bridge converter topology and series dual-boost bridgeless PFC are investigated in this dissertation. Compared with existing topologies in Fig. 2-6, Fig. 2-7(a) and Fig. 2-8, along with the modularity and scalability, the proposed topology has additional merits such as:

(a) Better reverse recovery performance of diode by utilizing wide bandgap devices to improve efficiency performance;

(b) In each cell, two switches are operated at line frequency thereby further reducing power losses;

(c) Fewer active switches. The auxiliary gate driver circuit and power supply are reduced;

(d) Low complexity and low control effort.

#### *2.1.2.4 The proposed topology in low, medium and high power rated data centers*

According to [2.16] and [2.17], the sizes of data centers vary widely. Two thirds of data centers in US are rated at less than 1 MW critical power. To reduce the construction and operation cost of data centers, multiple companies are sharing one data center, the resulting arrangement is called co-location data centers. The critical power of co-location data center is usually rated from 10-20 MW. Very few data centers exceed a power rating of 30 MW. At different power ratings, the prosed topology is modular to achieve high power capability. Three examples are given in the flowing sections for 1 MW, 10 MW and 30 MW power data centers.

##### *2.1.2.4.1 Low power rating data center (≤ 1 MW)*

The proposed topology for a 1 MW data center is shown in Fig. 2-9. If the grid side voltage is 2.4 kV per phase, then the minimum dc bus voltage in the rectifier stage is 3.771 kV. The dc reference voltage of each totem-pole PFC is set as 800 V, thus at least five cells of totem-pole PFC converters connected in series to realize 800 V dc output in each PFC stage. To step down 800 V to 400 V and provide galvanic isolation, a dual-active bridge converter is applied in dc/dc stage. The 1.2 kV or 1.7 kV SiC MOSFET can be utilized in the proposed topology.

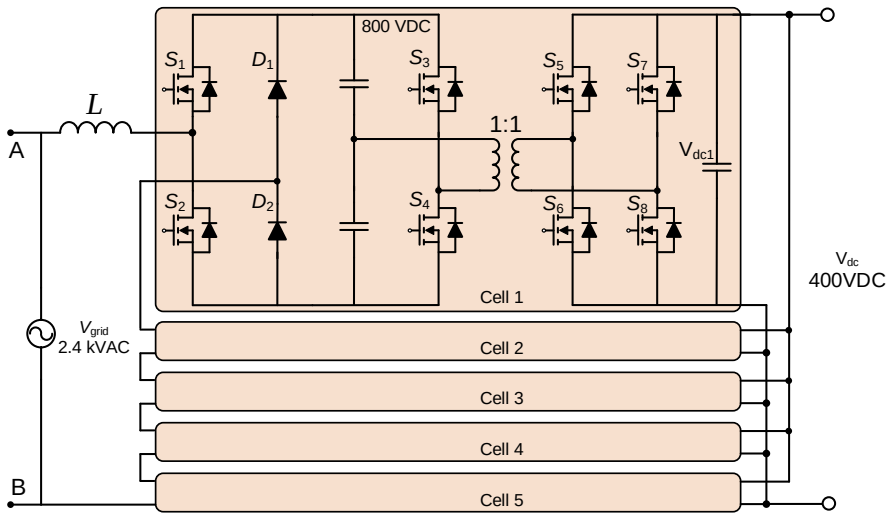



Fig. 2-9 Proposed Topology for 1 MW Power Data Center

The rectifier dc bus voltage is calculated below:

The rms voltage of the input ac voltage $v_{ac.rms}$ is 2400 V, if the modulation index $M$ is selected as 0.9, then the minimum voltage of the rectifier dc bus should be:

$$v_{ac2dc} = \frac{\sqrt{2}v_{ac.rms}}{M} = \frac{\sqrt{2}\times 2400}{0.9}V = 3.771kV \tag{2-1}$$

The reference voltage of each PFC dc bus is selected as 800 V, then the stages of PFC converter is:

$$n_{PFC,ideal} = \frac{3.771kV}{800V} = 4.71 \tag{2-2}$$

So at least a 5-stage PFC is required. In the three-phase ac grid connected to a 1 MW data center with a desired efficiency of 99%, the power rating of each stage of the dual-active bridge or PFC converter is:

$$p_{PFC,DAB} = \frac{1MW}{3\times 99\%} = 0.3367MW \tag{2-3}$$

Then the rms current rating for each phase is calculated as shown below:

$$i_{ac,rms} = \frac{p_{PFC,DAB}}{v_{ac.rms}} = \frac{0.3367MW}{2400V} = 140.3A \tag{2-4}$$

The peak current is:

$$i_{ac,peak} = \sqrt{2} i_{ac,rms} = \sqrt{2} \times 140.3A = 198.4A \tag{2-5}$$

If the secondary side dc bus voltage of the dual-active bridge is 400 V, then the current rating of the switching is:

$$i_{DAB,out} = \frac{p_{PFC,DAB}}{n_{PFC} v_{ac.rms}} = \frac{0.3367MW}{5 \times 400V} = 168.35A \tag{2-6}$$

The voltage/current stress and the available manufacturer of switches are summarized in Table 2.2.

Table 2.2 Switch Specification in 1 MW Data Center

| Switch | $S_1$-$S_2$, $S_3$-$S_4$ | $D_1$~$D_2$ | $S_5$-$S_6$, $S_7$-$S_8$ |
|---|---|---|---|
| Voltage stress | 800 V | 800 V | 400V |
| Current stress | 198.4 A | 198.4 A | 168.35 A |
| Manufacturer | CREE, Wolfspeed  | Powerex Inc.  | CREE, Wolfspeed  |
| Part No. | CAS300M17BM2 | LS411860 | CAS300M17BM2 |
| Voltage Rating | 1.7 kV | 1.8 kV | 1.7 kV |
| Current Rating | 225 A(90 ℃), 325 A(25 ℃) | 600 A(25 ℃) | 225 A(90 ℃), 325 A(25 ℃) |

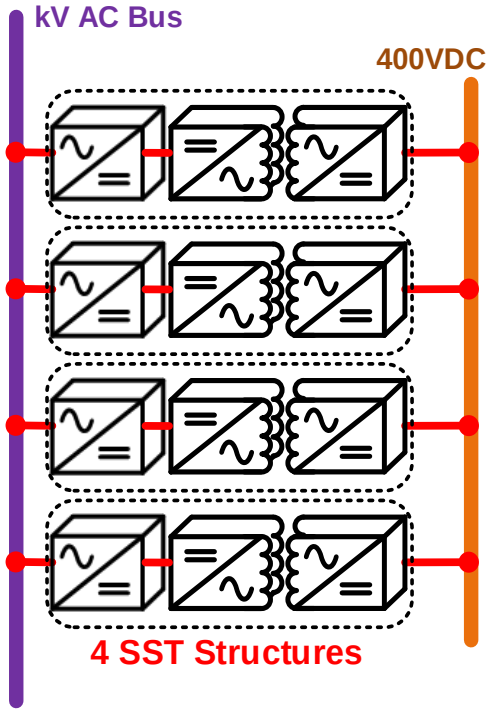
Table 2.2 (Cont.) Switch Specification in 1 MW data center

| | | | |
|---|---|---|---|
| Manufacturer | ROHM  | IXYS  | ROHM  |
| Part No. | BSM300D12P2E001 | MDO500-22N1 | BSM300D12P2E001 |
| Voltage Rating | 1.2 kV | 1.8 kV | 1.2 kV |
| Current Rating | 300 A(60℃) | 560 A(25 ℃) | 300 A(60 ℃) |
| Manufacturer | Semikron  | Microsemi Power Products Group  | Semikron  |
| Part No. | SKM500MB120SC | APT30SCD120B | SKM500MB120SC |
| Voltage Rating | 1.2 kV | 1.2 kV | 1.2 kV |
| Current Rating | 541 A(25 ℃), 431 A(80 ℃) | 99 A(25 ℃), parallel three switches = 297 A | 541 A(25 ℃), 431 A(80 ℃) |

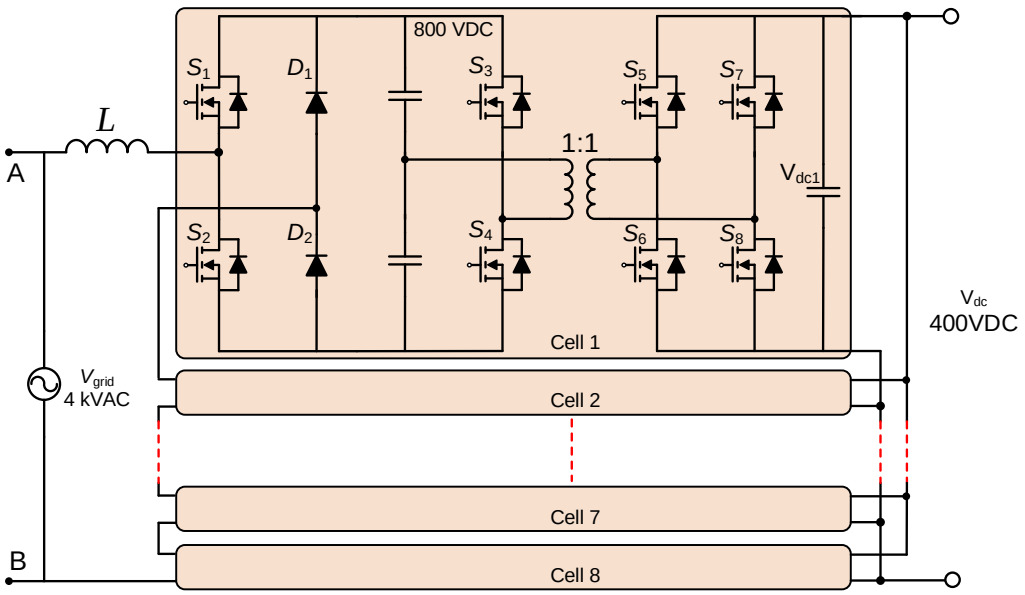
*2.1.2.4.2 Medium and high power rating data center (1~30 MW)*

Due to the high power rating, to reduce the current stress of switches, higher ac voltage is considered. The tradeoff is that the higher the ac voltage, the higher the output dc voltage of the PFC stage, then more PFC converters and high voltage rating devices are required. This dissertation evaluates the available 1.2 kV or 1.7 kV SiC MOSFET devices and 4 kV grid side voltage for a 10 MW data center. The proposed topology is shown in Fig. 2-10. Compared with the 1 MW data center, to further reduce the current stress of switches, there are four cells of SST converters, and the number of PFC converters are increased to eight.

In the 30 MW data center which is shown in Fig. 2-11, the grid voltage is increased to 6 kV. There are 12 cells of PFC converters, and 6 cells of SST converters. The equations to calculate the switch voltages and currents are similar with the previous section. The available switches are summarized in Table 2.3. With the development of high voltage rating SiC modules, such as the 3.3 kV, 6 kV, 10 kV and 15 kV voltage levels, the number of stages of the proposed topology can be greatly reduced.




(a) Four cells of SST Converter ac to dc Voltage

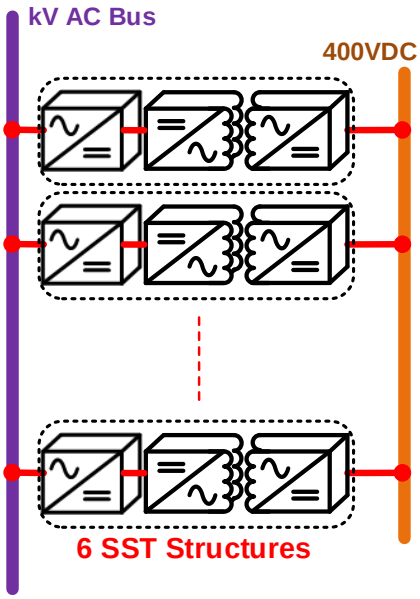



(b) Each cell has 8 PFC+DAB Converters

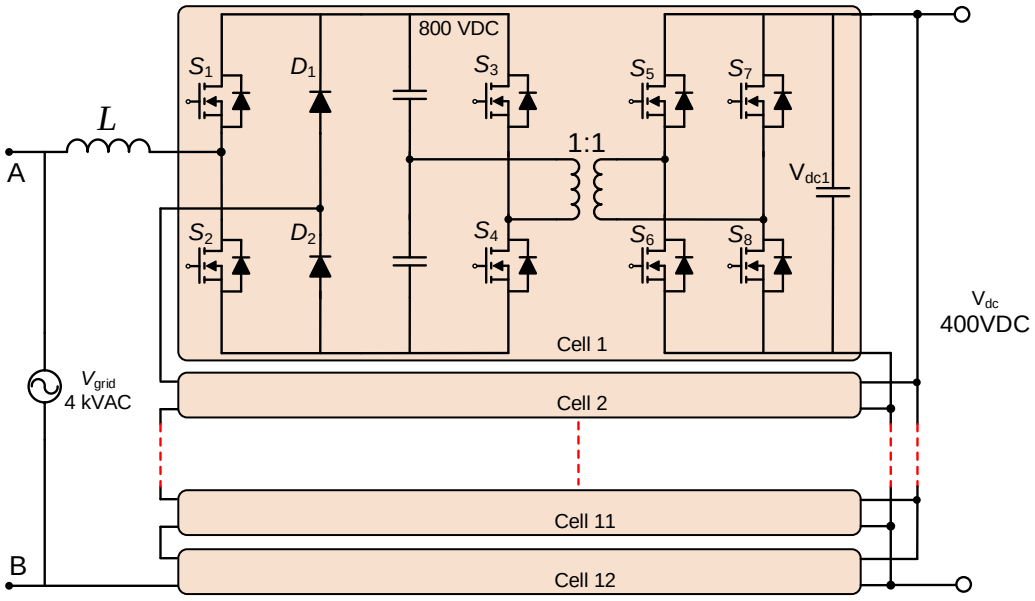
Fig. 2-10 Proposed Topology for 10 MW Power Data Center

Table 2.3 Switch Specification in 10 MW Data Center

| Switch | $S_1$-$S_2$, $S_3$-$S_4$ | $D_1$~$D_2$ | $S_5$-$S_6$, $S_7$-$S_8$ |
|---|---|---|---|
| Voltage rating | 800 V | 800 V | 400V |
| Current rating | 297.7 A | 297.7 A | 263.1 A |
| Manufacturer | CREE, Wolfspeed | Powerex Inc. | CREE, Wolfspeed |
| Part No. | CAS300M17BM2 | LS411860 | CAS300M17BM2 |
| Parallel Device | Yes, two switches | No | Yes, two switches |
| Manufacturer | ROHM | IXYS | ROHM |
| Part No. | BSM300D12P2E001 | MDO500-22N1 | BSM300D12P2E001 |
| Parallel Device | Yes, two switches | No | Yes, two switches |
| Manufacturer | Semikron | Microsemi Power Products Group | Semikron |
| Part No. | SKM500MB120SC | APT30SCD120B | SKM500MB120SC |
| Parallel Device | Yes, two switches | Yes, three switches | Yes, two switches |




(a) 6 cells of SST Converter ac to dc Voltage




(b) Each Cell Has 12 PFC+DAB Converters

Fig. 2-11 Proposed Topology for 30 MW Power Data Center

### *2.1.3 Design of cascaded scaled-down totem-pole multilevel converter*

In order to evaluate the proposed topology, a scaled-down prototype was developed and constructed. Two totem-pole Bridgeless PFC converters are connected in series, shown in Fig. 2-12.

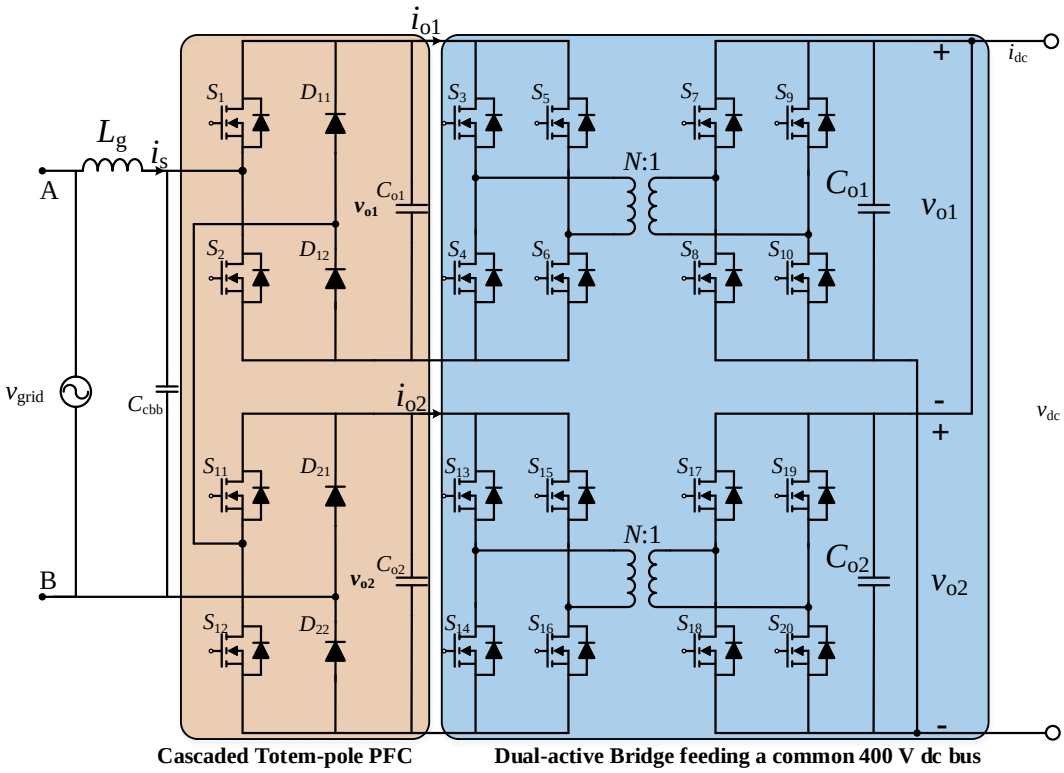



Fig. 2-12 Totem-pole Bridgeless PFC Converter, Two Cells

The circuit design of the proposed topology is introduced in the following section.

#### *2.1.3.1 Switch selection*

The switch current $i_{s\_peak}$ is given by Eq. (2-7).

$$i_{s\_peak} = \sqrt{2}\, P_s / \left( v_{grid} \eta_s \right) \tag{2-7}$$

where, $P_s$ is the power rating of the proposed topology, $v_{grid}$ is the rms voltage and frequency of grid, $\eta_s$ is the system designed efficiency.

Based on this calculation, the selection of switches are shown in Table 2.4.

Table 2.4 Switch Specification in the Scaled-down ac/dc Converter

| Switch | MOSFETs in primary side | Diodes in primary side | MOSFETs in secondary side |
|---|---|---|---|
| Voltage rating | 400 V | 400 V | 400V |
| Current rating | 6 A | 6 A | 2.53 A |
| Manufacturer | CREE, Wolfspeed | Fairchild Semiconductor | CREE, Wolfspeed |
| Part No. | C3M0065090D | L RHRP15120 | C3M0065090D |
| Voltage Rating | 900 V | 1.2 kV | 900 V |
| Current Rating | 36 A(25 ℃), 23 A(100 ℃) | 15 A(25 ℃) | 36 A(25 ℃), 23 A(100 ℃) |

*2.1.3.2 Grid side inductor design*

The grid side inductor is used to reduce the current ripple and reduce the THD of input current. The inductance is calculated as follows.

The duty cycle for the peak voltage is:

$$D_{PFC} = \frac{V_{o\_ref} n_{PFC} - \sqrt{2} v_{grid}}{V_{o\_ref} n_{PFC}} \tag{2-8}$$

where $n_{PFC}$ is the number of the cascaded bridgeless totem-pole converters and $V_{o\_ref}$ is the desired dc bus voltage.

The required PFC inductor is analyzed in [2.18]:

$$L_g = \frac{\sqrt{2} v_{grid} D_{PFC}}{i_{s\_ripple}} f_{PFC} \tag{2-9}$$

where $f_{PFC}$ is the switching frequency of ac/dc stage. $i_{s\_ripple}$ is the input current ripple requirement.

For 10% ripple:

$$i_{s\_ripple} = 10\% i_{s\_peak} \tag{2-10}$$

*2.1.3.3 Rectifier dc bus capacitance requirement*

There is a double-line frequency ripple voltage in the output dc voltage of the PFC due to the utilization of single phase rectifier. A capacitor is needed to suppress this voltage ripple. The following equations are used to calculate the required capacitance. The required dc bus capacitance is given in the following equation:

$$C_{oi} = \frac{P_s}{2\pi f_{grid} \eta_s n_{PFC} v_{DC.ripple} V_{o\_ref}}, i = 1,2 \tag{2-11}$$

where $v_{dc.ripple}$ is the dc voltage ripple requirement. If the acceptable ripple is 5% of dc bus voltage, then:

$$v_{DC.ripple} = 5\% v_{o\_ref} \tag{2-12}$$

*2.1.3.4 Input CBB capacitor selection*

The input capacitor on the grid side is utilized to reduce the voltage ripple caused by the switches [2.18]. The equation to calculate the capacitance is shown below:

$$C_{in} = \frac{k_{rip} i_{SD.ac.pk}}{2\pi f_{SD.PFC} r v_{SD.ac.rms}} \tag{2-13}$$

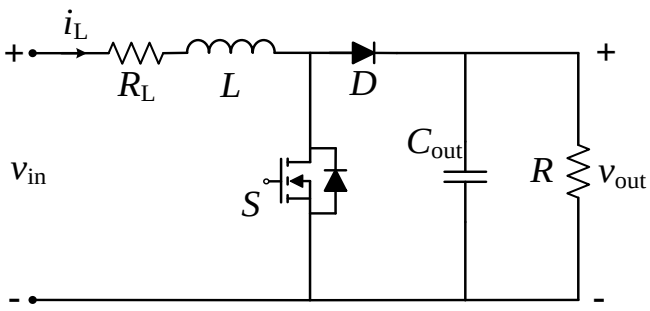
where $k_{rip}$ is the inductor current ripple coefficient and is selected as 20%, $r$ is ac voltage ripple coefficient and is chose as 5%.

## 2.2 Control Strategy: PI Control vs Model Predictive Control

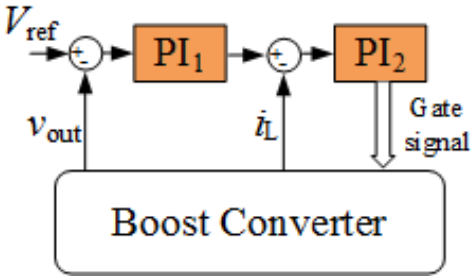
### *2.2.1 Conventional PI control*

In many literatures, the conventional PI controllers are investigated for power converters [2.19][2.20]. A boost converter is used as an example in the following discussion. Usually, there

are two control loops, which are shown in Fig. 2-13. The inner loop is the current loop, which regulates the inductor current along its reference and prevents overcurrent conditions. The outer loop is the voltage loop, which controls the output voltage to an expected value. The inner and outer PI controllers are designed based on the state-space equations of the power converter. Despite the reasonable effectiveness, simple scheme and design procedure of the PI control methods, some issues still need to be addressed, in particular: too many controller parameters need adjustment during tuning, switching losses and the stability region is usually changed by circuit conditions. Another disadvantage is that classical PI control is only suitable for single-input, single-output and linear systems. Significant control design and parameter tuning efforts are needed for the non-linear and multi-input, multi-output system.



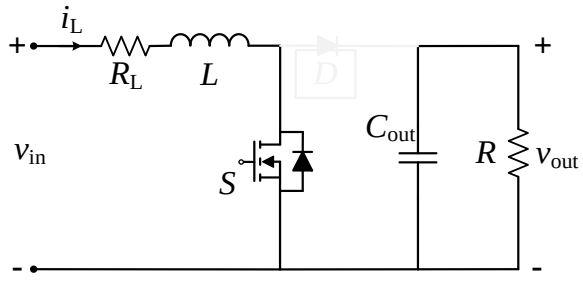

(a) Boost Converter



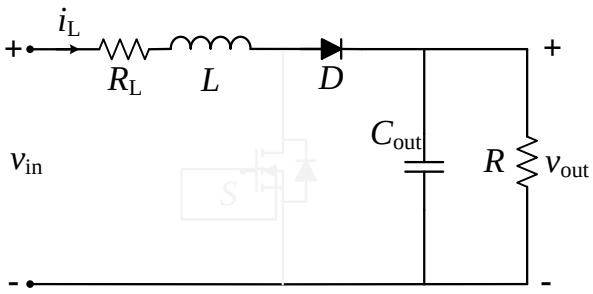

(b) Boost Converter with Classical PI Control

Fig. 2-13 Boost Converter Topology as Example

### *2.2.2 Conventional PI controller design steps for a boost converter*




(a) Switch *S* On




(b) Switch *S* Off

Fig. 2-14 Equivalent Circuits with Switch On and Off

First, the designer needs to develop the mathematical model of the boost converter. Considering continuous current mode, when the switch is on, the inductor is charged by the dc source $v_{in}$. The equivalent circuit is shown in Fig. 2-14(a). The equations of inductor current and capacitor voltage are given by

$$\begin{cases} v_{in}(t) = R_L i_L(t) + L\dfrac{di_L(t)}{dt} \\ C_{out}\dfrac{dv_{out}(t)}{dt} = -\dfrac{v_{out}(t)}{R} \end{cases} \tag{2-14}$$

where: $v_{in}$ is the input voltage, $R_L$ and $L$ are the boost inductor resistance and inductance, respectively. $i_L$ is inductor current, $C_{out}$ is the output dc capacitor, $R$ is resistive load, $v_{out}$ is the output dc voltage.

When the switch is off, the inductor is connected to the load, which results in the following equations:

$$\begin{cases} v_{in}(t) = \left( R_L i_L(t) + L \dfrac{di_L(t)}{dt} \right) + v_{out}(t) \\ C_{out} \dfrac{dv_{out}(t)}{dt} = i_L(t) + \dfrac{v_{out}(t)}{R} \end{cases} \tag{2-15}$$

Combination of Eqs. (2-14) and (2-15) lead to the following solution for the state-space equations in continuous-time domain:

$$\begin{cases} \dfrac{dx(t)}{dt} = [A_1 + A_2 u]x(t) + Bw(t) \\ y(t) = Cx(t) \end{cases} \tag{2-16}$$

where:

$$x(t) = \begin{bmatrix} i_L(t) \\ v_{out}(t) \end{bmatrix},$$

$$A_1 = \begin{bmatrix} -\dfrac{R_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C_{out}} & -\dfrac{1}{C_{out}R} \end{bmatrix},$$

$$A_2 = \begin{bmatrix} 0 & \dfrac{1}{L} \\ -\dfrac{1}{C_{out}} & 0 \end{bmatrix},$$

$$u = \begin{cases} 0, \text{switch off} \\ 1, \text{switch on} \end{cases},$$

$$B = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix},$$

$$w(t) = v_{in}(t),$$

$$y(t) = v_{out}(t),$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix}.$$

Use the mathematical model to calculate the required phase and magnitude margin. This step can be realized in MATLAB™ or PLECS™. The phase and magnitude margin can be easily read from the simulation results. For example, Fig. 2-15 shows the phase margin of 81.617 degrees, and a magnitude of 3.14 dB. The last step is tuning PI parameters to meet the phase and magnitude margin.

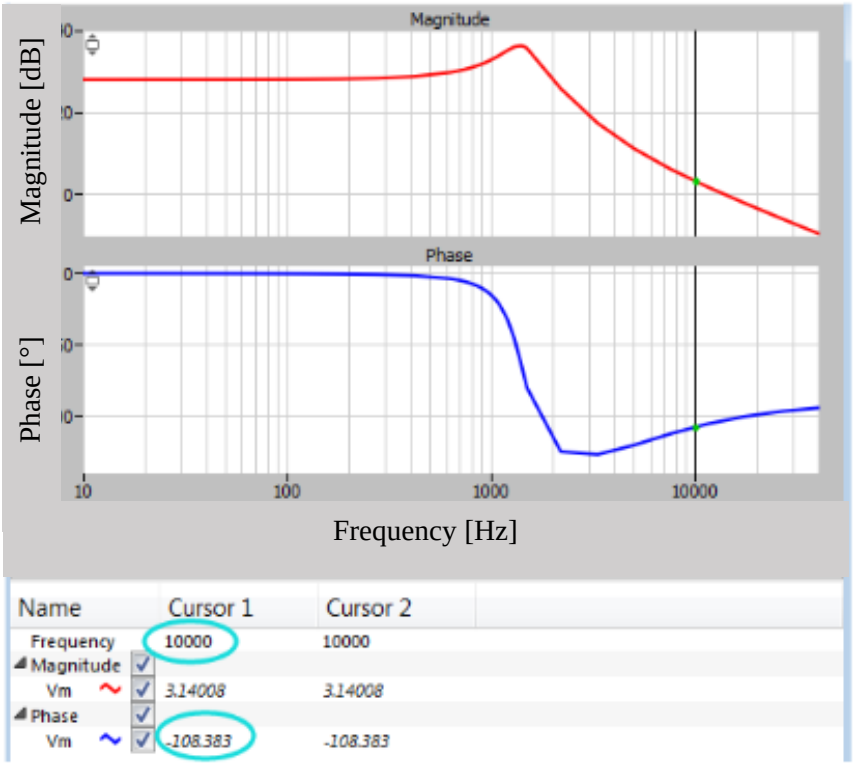



Fig. 2-15 Bode-plot of a Boost Converter in PLECS

In summary, both the control scheme and design procedure of PI controller are simple and reasonably effective. However, the PI controller is only suitable for linear systems and require significant efforts with regard to controller parameters tuning. For these reasons, a more effective and straightforward method of model predictive control is introduced and developed in the next section.

### *2.2.3 Model predictive control*

Model predictive control is a real time control algorithm to overcome the aforementioned disadvantages. It utilizes the mathematical model of the plant and selects the appropriate device switching state to achieve the desired control goals. There are four main elements of model predictive control. First is the mathematical model of the controlled plant. It is a power converter continuous-time model which specifies the input-output relation of the voltages and currents. Then the discrete-time model is derived from continuous-time model to predict the system behavior in the next switching cycle. Second is the design of the control objectives or cost functions. The cost functions account for the targeted circuit behaviors. For example, the output voltage of power converter should accurately track the reference, and the input current should be sinusoidal and achieve unity power factor. The lower the cost value, the better circuit performance is achieved. Third, it is based on the control goals to sense the feedback signals. The circuit status such as the voltage of capacitors or current of inductors are feedback signals which are applied in the mathematical model to predict the future behavior of the controlled variables.

### *2.2.4 Discretization method: from continuous-time domain to discrete-time domain*

The switching period is relatively small when compare with grid frequency and leads to

$$\begin{cases} dx(t) = x(k+1) - x(k) \\ dt = T_s \end{cases} \tag{2-17}$$

Then:

$$\frac{dx(t)}{dt} = \frac{x(k+1) - x(k)}{T_s} \tag{2-18}$$

where, '$k$' means the current switching cycle, and '$k$+1' means the next switching cycle. $T_s$ is one switching period.

$$\begin{cases} \dfrac{dx(t)}{dt} = [A_1 + A_2 u]x(t) + Bw(t) \\ y(t) = Cx(t) \end{cases} \tag{2-19}$$

$$\begin{cases} \dfrac{x(k+1) - x(k)}{T_s} = [A_1 + A_2 u]x(k) + Bw(k) \\ y(k) = Cx(k) \end{cases} \tag{2-20}$$

$$\begin{cases} x(k+1) = T_s[A_1 + A_2 u]x(k) + Bw(k) + x(k) \\ y(k) = Cx(k) \end{cases} \tag{2-21}$$

The discretization of continuous-time state-space Eq. (2-16) is illustrated by

$$\begin{cases} x(k+1) = T_s[A_1 + A_2 u]x(k) + Bw(k) + x(k) \\ y(k) = Cx(k) \end{cases} \tag{2-22}$$

where:

$$x(k+1) = \begin{bmatrix} i_L(k+1) \\ v_{out}(k+1) \end{bmatrix},$$

$$x(k) = \begin{bmatrix} i_L(k) \\ v_{out}(k) \end{bmatrix},$$

$$w(k) = v_{in}(k).$$

From the discretized Eq. (2-22), the required feedback signals are inductor current $i_L$ and the output voltage $v_{out}$. The objective of boost converter is to regulate the output dc voltage $v_{out}$. The cost function is defined as the absolute voltage error between output voltage and reference voltage. Thus, the cost function is given by

$$Cost = \left| V_{ref} - v_{out}(k+1) \right| \tag{2-23}$$

The expression of $v_{out}(k+1)$ is given by Eq. (2-24) which is rewritten as

$$v_{out}(k+1) = \frac{T_s(1-u)}{C_{out}} i_L(k) + v_{out}(k)\left(2 - \frac{T_s}{C_{out}R}\right) \tag{2-24}$$

The switching state $u$ has two status 1 and 0. Thus:

$$\begin{cases} v_{out}(k+1) = v_{out}(k)\left(2 - \frac{T_s}{C_{out}R}\right), \text{switch S is on} \\ v_{out}(k+1) = \frac{T_s}{C_{out}} i_L(k) + v_{out}(k)\left(2 - \frac{T_s}{C_{out}R}\right), \text{switch S is off} \end{cases} \tag{2-25}$$

where $v_{out}$(k) is the feedback signal at time k. $v_{out}$(k+1) is the predicted value at time k+1. S is the switch state, when S=1, switch is on, otherwise S=0, switch is off.

The corresponding cost functions:

$$\begin{cases} Cost_{u=1} = \left| V_{ref} - v_{out}(k)\left(2 - \frac{T_s}{C_{out}R}\right) \right|, \text{switch S is on} \\ Cost_{u=0} = \left| V_{ref} - \frac{T_s}{C_{out}} i_L(k) - v_{out}(k)\left(2 - \frac{T_s}{C_{out}R}\right) \right|, \text{switch S is off} \end{cases} \tag{2-26}$$

The procedure to choose the proper switching state is shown in Fig. 2-16. $v_{out}(k)$ is the sensed signal at the beginning of one switching cycle. Assume switch *S* will be on or off in this switching cycle, then the predicted output voltage $v_{out}(k+1)$ can be obtained by Eq. (2-25), respectively. Through comparing $Cost_{u=1}$ and $Cost_{u=0}$, the switching state with the lower cost value is chosen as the gate single to switch *S*. In Fig. 2-16, at time of $k$+1, because $Cost_{u=0}$ is lower than $Cost_{u=1}$, the 'off' control signal is selected for switch *S*. At time of $k$+2, $Cost_{u=1}$ is lower than $Cost_{u=0}$, the 'on' state is the better choice to achieve smaller voltage error. At time of $k$+3, $Cost_{u=0}$ is higher than $Cost_{u=1}$, then the switch should be on. However, there is no switching action needed in this switching period due to the fact that the switch is already on at time $k$+2. In this case, the switching speed is reduced.

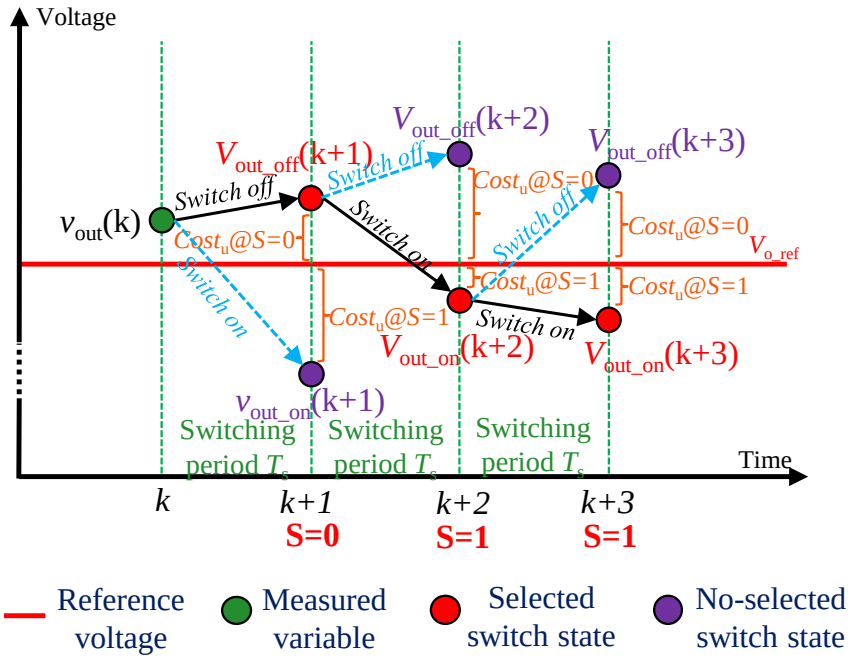



Fig. 2-16 The Procedure to Choose the Proper Switching State

In summary, the model predictive control is suitable for both linear and non-linear systems. It also has fewer control parameters. With the design of cost functions, it can easily realize the multi-objective control. Despite the disadvantages of the model predictive control, such as the requirement of both high calculation ability of a controller and the accurate modeling of the system, it provides the significantly better control performance.

### *2.2.5 Comparison of PI and MPC*

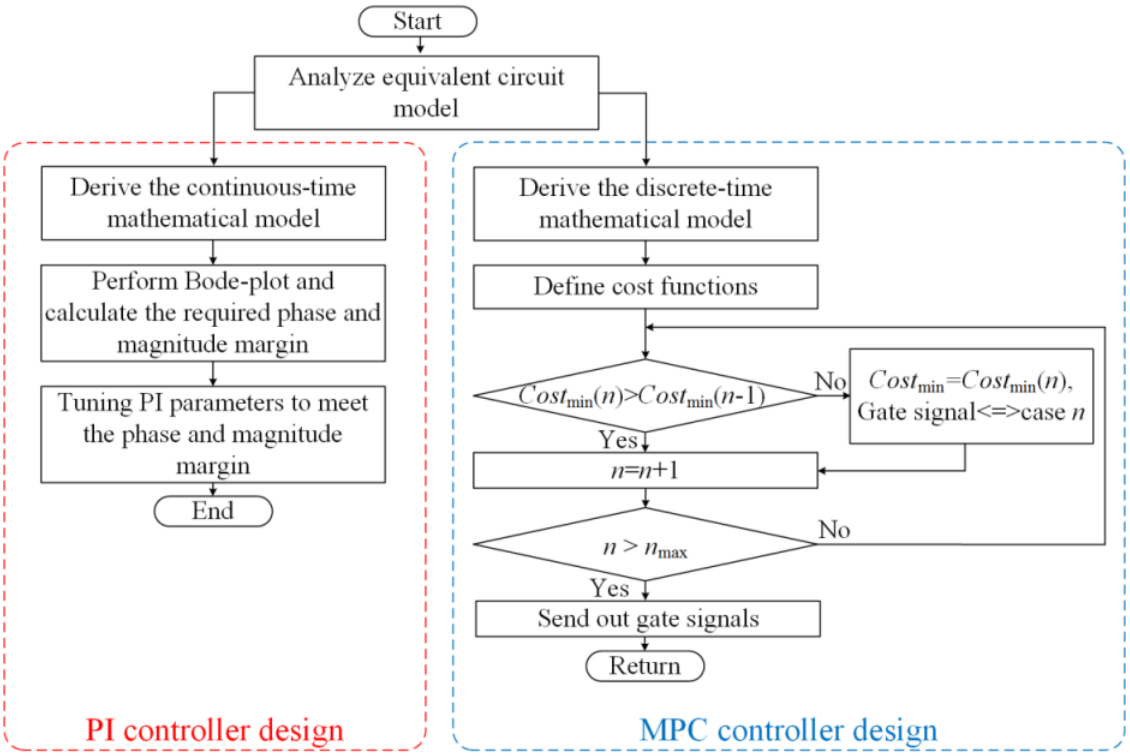



Fig. 2-17 Design Flowcharts of PI and MPC Control

The design flowchart is given in Fig. 2-17. All the steps have been discussed in the previous section. Both control methods require the mathematical model of the system. The MPC needs more steps to find the best switching state. However, the PI controller parameter is unchanged during operation, so it is hard to meet all the circuit conditions. The MPC controller is based on the desired feedback and circuit model, and the gate control signal is optimized during every switching cycle to realize the expected circuit performance. What's more, the hardware cost is similar for both PI and MPC controllers.

In summary, a simple boost converter is used first to help understand the control theory behind these two controllers. The controller design for the proposed cascaded bridgeless totem-pole

multilevel converter, which is more complicated and has more active switches, will be introduced in the next section.

## 2.3 MPC design for Cascaded Bridgeless Totem-Pole Multilevel Converter

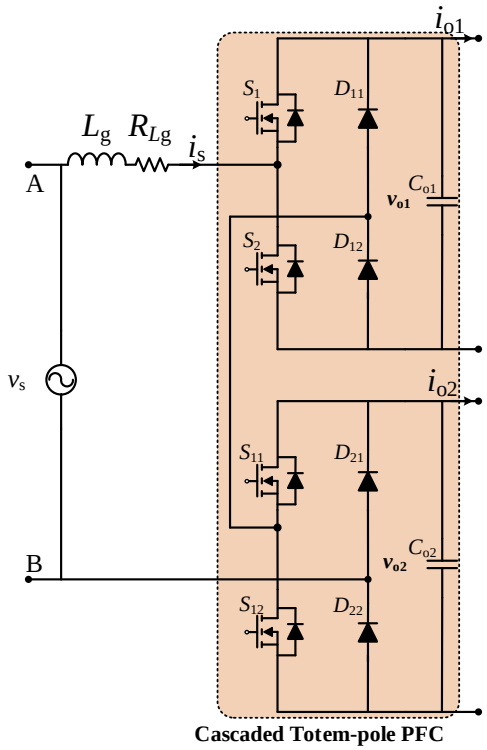



Fig. 2-18 Scaled-down Prototype: ac/dc Stage, Two Cells

Several control strategies for cascaded converters, such as level-shift pulse-width modulation (LSPWM), phase-shift PWM, or sliding mode control, have been developed [2.21][2.22]. Despite the effectiveness of the developed control methods, some issues still need to be addressed, in particular: voltage balancing, voltage error elimination and switching losses. A model predictive control through the selection of the appropriate switching state to achieve the control goals has been applied in motor drives, dc/dc converters and so on [2.23][2.24]. The main characteristic of the MPC algorithm is predicting the future behavior of the controlled variables whose values will

be used to calculate the cost function that represents the control objectives of system. The desired switching states will be obtained by selecting the minimal cost function. In this paper, a real-time MPC is designed for the proposed cascaded bridgeless totem-pole converter to achieve a better dynamic performance.

This section is organized as follows: the circuit design of the proposed topology is described first. Second, the control strategy of the MPC is presented. Third, the simulation and experimental results of the conventional PI and proposed MPC controller are illustrated. The conclusion and future work are given in the last part of this section.

### *2.3.1 Cascaded totem-pole converter modeling*

The procedure to design the MPC controller for a two-cell cascaded totem-pole converter will be discussed in this section. Based on KCL and KVL, in Fig. 2-18, the input-output relationship of the currents and voltages are given by Eqs. (2-27) (2-28) and (2-29).

$$L_g \frac{di_s(t)}{dt} + R_{Lg} i_s(t) = v_s(t) - (u_1 - u_2) v_{o1}(t) - (u_{11} - u_{12}) v_{o2}(t) \tag{2-27}$$

$$C_{o1} \frac{dv_{o1}(t)}{dt} = \left[ (u_1 - u_2) i_s(t) - i_{o1}(t) \right] \tag{2-28}$$

$$C_{o2} \frac{dv_{o2}(t)}{dt} = \left[ (u_{11} - u_{12}) i_s(t) - i_{o2}(t) \right] \tag{2-29}$$

where, $i_s$ is the grid current, $L_g$ is the grid side inductor, $R_{Lg}$ is the resistance of inductor, $v_{o1}$ and $v_{o2}$ are the 1st cell and 2nd cell output voltages, respectively. Capacitors $C_{o1}$ and $C_{o2}$ are the 1st cell and 2nd cell dc-bus capacitor voltages, respectively. $u_1$ and $u_2$ are the switch states of $s_1$ and $s_2$, respectively. $u_{11}$ and $u_{12}$ are the switch states of $s_{11}$ and $s_{12}$, respectively.

From the time-domain equations, the state-space equations of the cascaded totem-pole converter are shown in Eq. (2-30).

$$\begin{cases} \dfrac{dx(t)}{dt} = \left[A_1 + A_2 u(t)\right] x(t) + Bw(t) \\ y(t) = Cx(t) \end{cases} \tag{2-30}$$

The expression of $x(t)$, $u(t)$, $A_1$, $A_2$, $B$, and $C$ are shown below.

$$x(t) = \begin{bmatrix} i_s(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix} \tag{2-31}$$

$$A_1 = \begin{bmatrix} -R_{L_g} / L_g & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2-32}$$

$$A_2 = \begin{bmatrix} 0 & 0 & -1/L_g \\ 1/C_{o1} & 0 & 0 \\ 0 & 1/C_{o2} & 0 \end{bmatrix} \tag{2-33}$$

$$B = \begin{bmatrix} 1/L_g & 0 & 0 \\ 0 & -1/C_{o1} & 0 \\ 0 & 0 & -1/C_{o2} \end{bmatrix} \tag{2-34}$$

$$w(t) = \begin{bmatrix} v_s(t) \\ i_{o1}(t) \\ i_{o2}(t) \end{bmatrix} \tag{2-35}$$

$$y(t) = \begin{bmatrix} v_{o1}(t) \\ v_{o2}(t) \end{bmatrix} \tag{2-36}$$

$$C = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{2-37}$$

The discrete-time models from the continuous-time model are given in Eqs. (2-38), (2-39) and (2-40).

$$\begin{cases} i_s(k+1) = \dfrac{T_s}{L_g}\left[\Delta_1 - \Delta_2 - \Delta_3\right] + i_s(k) \\ \Delta_1 = v_s(k) - R_L i_s(k) \\ \Delta_2 = (u_1 - u_2) v_{o1}(k) \\ \Delta_3 = (u_{11} - u_{12}) v_{o2}(k) \end{cases} \tag{2-38}$$

$$v_{o1}(k+1) = \frac{T_s}{C_{o1}}\left[(u_1 - u_2) i_s(k) - i_{o1}(k)\right] + v_{o1}(k) \tag{2-39}$$

$$v_{o2}(k+1) = \frac{T_s}{C_{o2}}\left[(u_{11} - u_{12}) i_s(k) - i_{o2}(k)\right] + v_{o2}(k) \tag{2-40}$$

where, '$k$' means the current switching cycle, and '$k$+1' means the next switching cycle. Eqs. (2-39) and (2-40) are to predict the desired control variables $v_{o1}(k+1)$ and $v_{o2}(k+1)$, respectively.

### *2.3.2 Cost function of totem-pole converter*

The control goals of the cascaded totem-pole converter are shown below:

(a) The input current should be sinusoidal and achieve unity power factor.

(b) The output voltage of each totem-pole should accurately track the reference value. The voltages of the dc buses should be balanced.

(c) Maintain a low switching frequency in order to reduce power losses.

(d) Have a very good dynamic performance against load changes.

#### *2.3.2.1 Unity power factor control*

The goal of power factor correction control is to make the input current waveform sinusoidal and in phase with the input voltage. The reference current $i_{s\_ref}$ is controlled by the output of voltage loop. Then the cost function of PFC control in the proposed topology is given in Eq. (2-41).

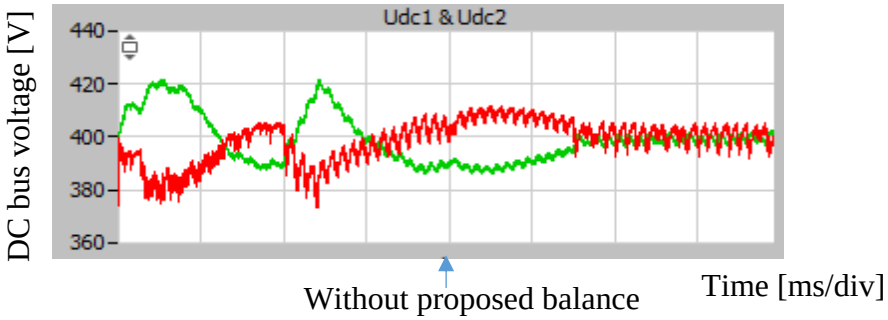
$$Cost_{current} = \left| i_{s\_ref} - i_s(k+1) \right| \tag{2-41}$$

#### *2.3.2.2 Voltage balance control*

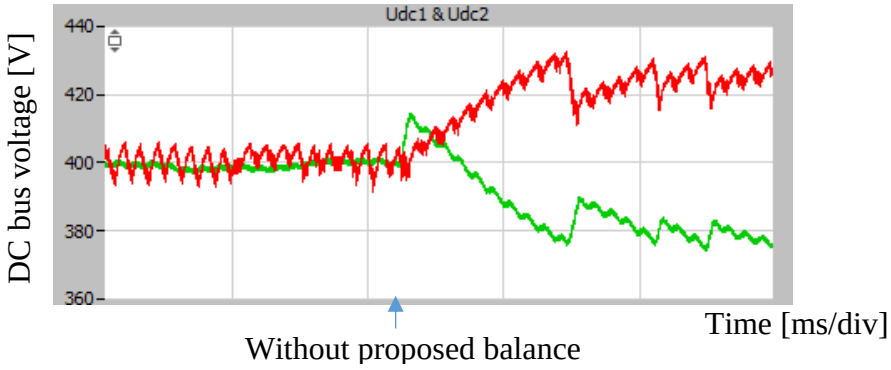
If the PFC rectifier converters are connected in series, the voltage unbalance in the PFC output side voltage will happen without proper control. The unbalance issue is due to the varied active power of the DAB and the unequal switching losses in each PFC converter. The difference of these voltages will lead to the overvoltage of switches and capacitors. There are many papers which discuss about controlling the voltage unbalance. The existing normal control is utilizing PI or Proportional-Resonant (PR) control to track dc voltage reference or power reference [2.25]. The disadvantage of the PI or PR method is that it is not easy to find the proper parameters and the stability region is usually changed by circuit conditions. What's more, if the system is nonlinear, significant parameter design changes are required in PI or PR control. To overcome the aforementioned disadvantages, the model predictive control is developed in this dissertation. Without any PI or PR controller, the cost function of the voltage tracking control and voltage balance are given in Eq. (2-42) and Eq. (2-43), respectively. The simulation results are shown in Fig. 2-19.

$$Cost_{dc} = \left| V_{o\_ref} - v_{o1}(k+1) \right| + \left| V_{o\_ref} - v_{o2}(k+1) \right| \tag{2-42}$$

$$Cost_{dc,balance} = \left| v_{o2}(k+1) - v_{o1}(k+1) \right| \tag{2-43}$$




(a) Without to With Voltage Balance Control




(b) With to Without Voltage Balance Control

Fig. 2-19 Simulation Results of 400 dc Bus Balance Performance

*2.3.2.3 Switching sequence*

As shown in Table 2.5, there are 16 cases of switching states for switches $S_1$, $S_2$, $S_{11}$, and $S_{12}$. However, $S_1$ and $S_2$ or $S_{11}$ and $S_{12}$ should not be ON at the same time to prevent a short circuit, thus the switching cases 10 to 16 should be avoided. The possible switching states are from cases 1 to 9. The minimum cost function and the related switch positions are applied to the circuit to achieve the optimized performance of the power converter.

Table 2.5 Switching Cases of Cascaded Bridgeless Totem-pole PFC

| Switching case *n*<br>1: switch on<br>0: switch off | $u_1$ | $u_2$ | $u_{11}$ | $u_{12}$ |
|---|---|---|---|---|
| **Case 1:** | 0 | 0 | 0 | 0 |
| **Case 2:** | 0 | 0 | 0 | 1 |
| **Case 3:** | 0 | 0 | 1 | 0 |
| **Case 4:** | 1 | 0 | 0 | 0 |
| **Case 5:** | 1 | 0 | 0 | 1 |
| **Case 6:** | 1 | 0 | 1 | 0 |
| **Case 7:** | 0 | 1 | 0 | 0 |
| **Case 8:** | 0 | 1 | 0 | 1 |
| **Case 9:** | 0 | 1 | 1 | 0 |
| **Case 10:** | 0 | 0 | **1** | **1** |
| **Case 11:** | 1 | 0 | **1** | **1** |
| **Case 12:** | 0 | 1 | **1** | **1** |
| **Case 13:** | **1** | **1** | 0 | 0 |
| **Case 14:** | **1** | **1** | 0 | 1 |
| **Case 15:** | **1** | **1** | 1 | 0 |
| **Case 16:** | **1** | **1** | **1** | **1** |

#### *2.3.2.4 Overall system cost function*

In summary, by combining the aforementioned cost functions, the overall system cost function is given in Eq. (2-44).

$$\begin{cases} Cost_{dc,balance} = \left| v_{o2}(k+1) - v_{o1}(k+1) \right| \\ Cost_{dc} = \left| V_{o\_ref} - v_{o1}(k+1) \right| + \left| V_{o\_ref} - v_{o2}(k+1) \right| \\ Cost_{current} = \left| i_{s\_ref} - i_s(k+1) \right| \\ Cost_{swicth1,2} = \left| u_1(k) - u_1(k+1) \right| + \left| u_2(k) - u_2(k+1) \right| \\ Cost_{swicth11,12} = \left| u_{11}(k) - u_{11}(k+1) \right| + \left| u_{12}(k) - u_{12}(k+1) \right| \\ Cost_{\min} = Cost_{dc} + Cost_{current} + Cost_{swicth1,2} + Cost_{swicth11,12} + Cost_{dc,balance} \end{cases} \tag{2-44}$$

The flowchart of the MPC strategy is illustrated in Fig. 2-20. First, the current $i_s(k)$ of inductor $L_g$, and the totem-pole PFC output voltage $v_{o1}(k)$ and $v_{o2}(k)$ are the measured variables at the beginning of the $k^{th}$ switching cycle. Second, from the discrete-time model in Eqs. (2-38), (2-39) and (2-40), the variables $i_s(k+1)$, $v_{o1}(k+1)$ and $v_{o2}(k+1)$ in the $(k+1)^{th}$ switching cycle are predicted. Third, there are 9 switching cases leading to 9 sets of predictive variables. From each set of predictive variables, the cost function $Cost_{min}$ is calculated separately. The minimal cost function is selected and the related switching signals are sent to the gate drive circuit to regulate the expected dc bus voltage.

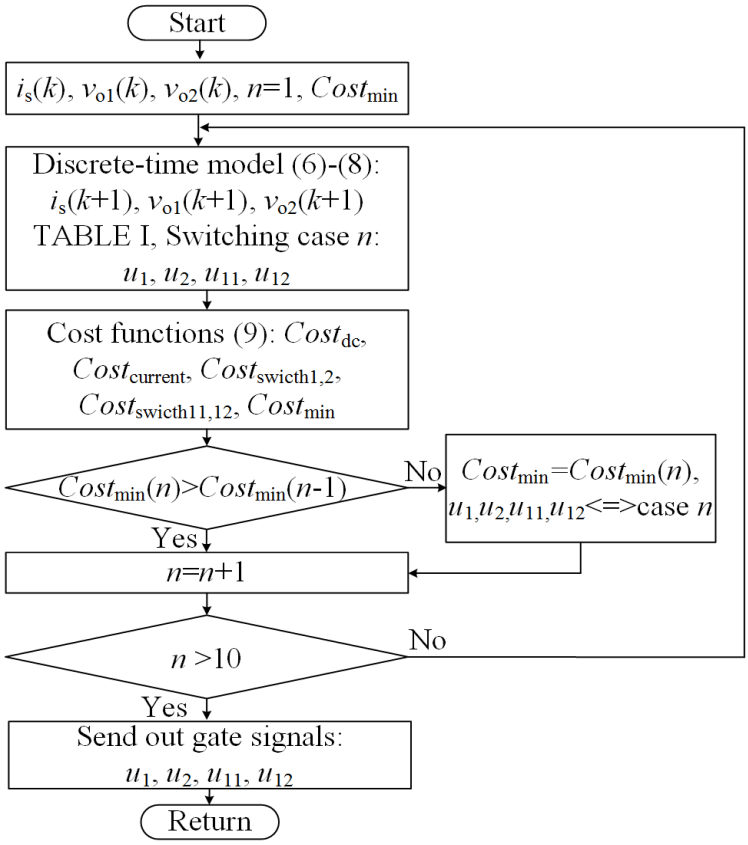
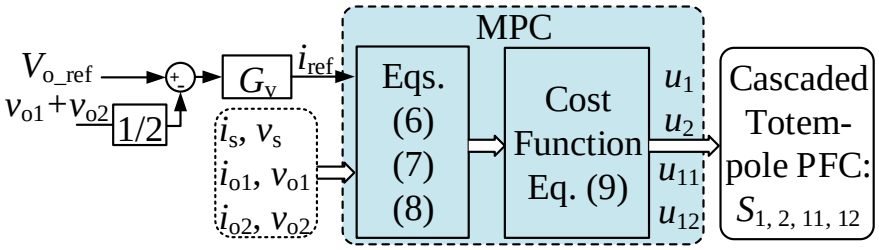


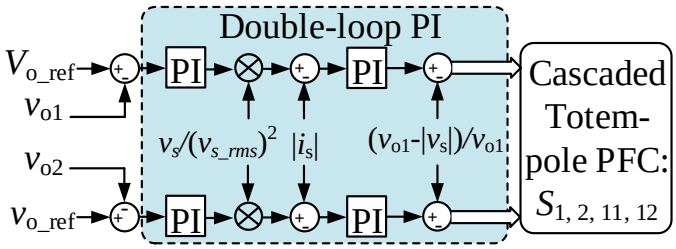

Fig. 2-20 The Flowchart of MPC

### *2.3.3 Block diagram of controllers*

The block diagram of the MPC control for the proposed topology is illustrated in Fig. 2-21 (a). The reference $i_{ref}$ in the current-loop is generated by the dc voltage-loop. The voltage-loop aims to maintain the primary dc bus $v_{oi}$. The controller $G_v$ can be a simple PI or PR control. The conventional double-loop PI control is also given in Fig. 2-21 (b) for comparison purposes. A more detailed control loop design given in [2.26]. There are four controllers that need to be designed which are cumbersome and dependent on each other. The control diagram for the DAB is using conventional phase-shift control [2.27].




(a) MPC Algorithm for the Proposed Topology




(b) Conventional PI Control for the Proposed Topology

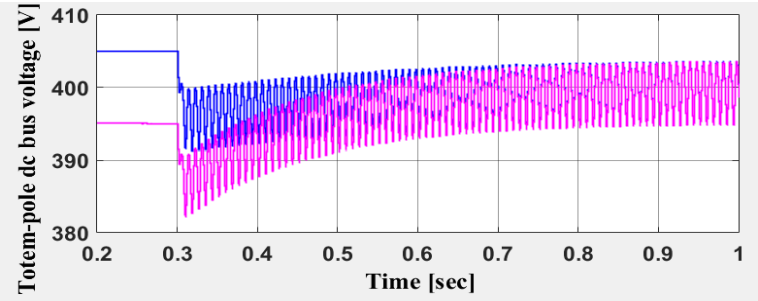
Fig. 2-21 The Block Diagram of MPC and Conventional PI for the Proposed Topology

### *2.3.4 Simulation and experiment verification*

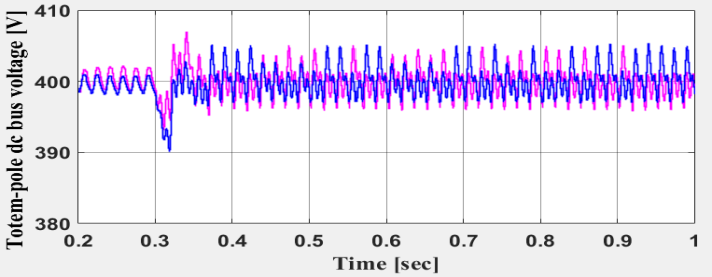
In order to verify the effectiveness of the proposed MPC strategy, both simulation and experimental results are presented. The simulation results are introduced first. MATLAB/Simulink™ is used to verify the proposed MPC strategy in the scaled-down 5 kW prototype. The grid voltage is 480 V and the frequency is 60 Hz. Using Eqs. (2-9) and (2-11), the boost inductor $L_g$ is 7.2 mH, and the capacitors $C_{o1}$ and $C_{o2}$ on the dc side of the totem-pole converter are 680 μF. Each cell's dc reference voltage is $V_{o\_ref}$ = 400 Vdc. A resistive load is connected in the secondary side of the DAB. Conventional PI control and MPC are applied in the cascaded totem-pole PFC, respectively. The same controller for the DAB is used for both the PI and MPC controllers.

*2.3.4.1 Simulation: dc bus voltage balance*

Before 0.3 s, the converter operates under no-load condition. At 0.3 s, a 5 kW load is connected. As shown in Fig. 2-22(a), there is a voltage imbalance issue between $v_{o1}$ and $v_{o2}$ before 0.3 s when using the conventional PI control. Auxiliary and complex balance control is needed in the conventional PI control. Fig. 2-22(b) shows that the voltage is always balanced between the two totem-pole converters under MPC control. During the step-up load, the conventional PI control needs at least 0.3 s to stabilize the output voltage of each totem-pole converter, while the MPC requires less than 0.05 s to stabilize these voltages. The 120 Hz voltage ripple in the dc bus is limited to 10 V. The simulation results verified that the transient performance of the MPC controller is much better than that of the PI controller.




(a) Conventional PI Control




(b) Model Predictive Control

Fig. 2-22 Normal Operation to Step-up Load of the Two Controllers

### *2.3.4.2 Simulation results of switching frequency*

The switching frequency of the conventional PI control is set at 20 kHz. The switching frequency of the MPC is variable and depends on the system feedback. The simulation results of the gate signal from each controller are shown in Fig. 2-23 and Fig. 2-24. The maximum switching frequency of the MPC is about 8 kHz. This is less than half of the switching frequency in the conventional PI control, so the switching loss can be greatly reduced. The current THD of both controllers are all within the IEEE 519-2014 standard. It is worth mentioning that the minimum switching frequency of MPC algorithm should be set to meet the THD requirements.

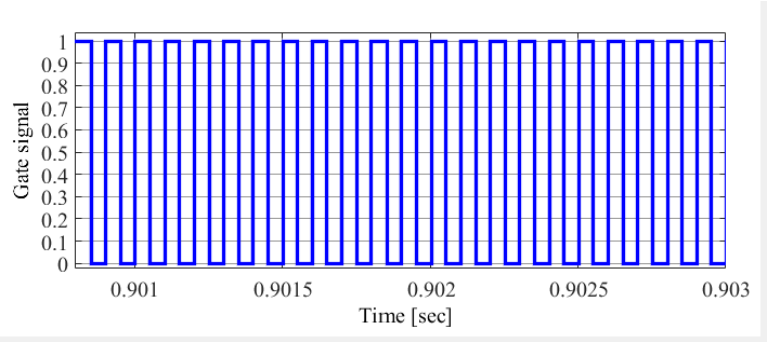



Fig. 2-23 Gate Signals For a Selected Switch Position For Conventional PI Control

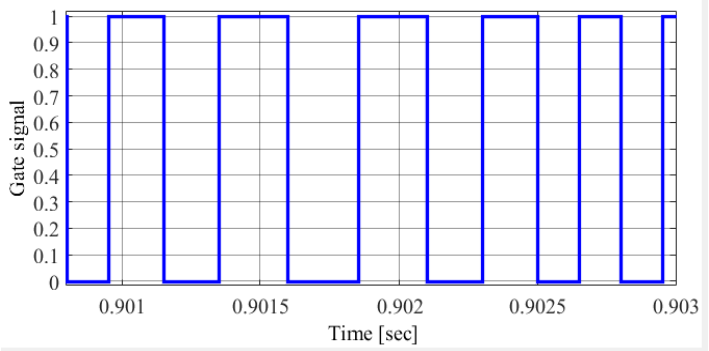



Fig. 2-24 Gate Signals for a Selected Switch Position for Model Predictive Control

*2.3.4.3 Experiment: dc bus voltage balance*

The experimental setup is shown in Fig. 2-25 which includes the hardware-in-loop (HIL) simulator Typhoon HIL402, a TI DSP TMS320F28335 control card, and oscilloscope. The MPC algorithm is programmed in the DSP. The proposed cascaded bridgeless totem-pole PFC and dual-active bridge converter are modeled in Typhoon HIL 402. The circuit parameters are the same as those in the simulation setup. The test results of $v_{o1}$ and $v_{o2}$ are shown in Fig. 2-26 and Fig. 2-27, respectively. Similarly to the simulation results, the experimental results exhibit that the proposed MPC strategy has smaller overshoot and much faster response when the load power changes from 0 to 5 kW.

Fig. 2-25 Experimental Setup: Typhoon Simulator and DSP Control Card

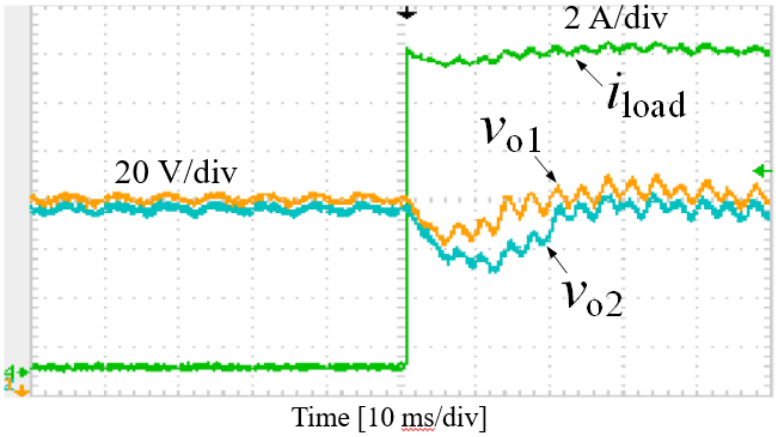



Fig. 2-26 Hardware-In-Loop Testing Results of Conventional PI Control (Time: 25 ms/div, $v_{o1}$=$v_{o2}$=400 V, $i_{load}$: 0 to 12.5 A)

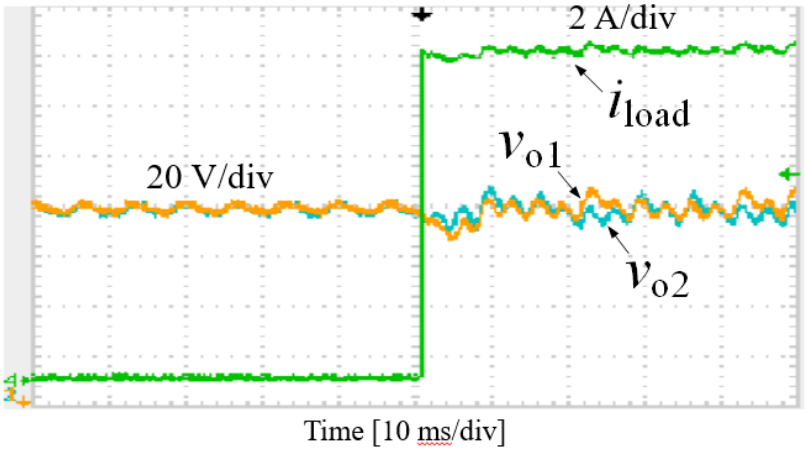



Fig. 2-27 Hardware-In-Loop Testing Results of The Proposed Model Predictive Control (Time: 25 ms/div, $v_{o1}$=$v_{o2}$=400 V, $i_{load}$: 0 to 12.5 A)

## 2.4 Conclusion

A model predictive control for a novel cascaded bridgeless totem-pole multilevel converter for 400 V DC-powered data centers was presented. The procedures to design MPC control in power converter application are:

(a) Determination of power converter model to specify the input-output relation of the voltages and currents.

(b) Determination of discrete-time model from continuous-time model to predict the system future behavior.

(c) Designing the cost functions. In the proposed topology, the first cost function can be that the sinusoidal input current to meet a unity power factor requirement. Second, the output voltage of each totem-pole should accurately track the reference value. The third cost function is to limit the switching frequency to a set range to minimize loss while optimizing filter performance. Fourth, is to ensure good dynamic response during load changes.

(d) Select the switch position to have the minimum cost function and apply it to circuit to achieve the preferred performance of power converter.

Compared with existing multilevel converters, totem-pole converters, by utilizing the advantages of wide bandgap devices, were cascaded to achieve high efficiency and reduce the number of active switches. Compared to the conventional PI control, the proposed MPC strategy had better transient and voltage balance performance and required lower switching frequencies which translates to lower switching losses. Both simulation and experimental results were been presented to validate the effectiveness of the proposed topology and its optimized MPC strategy. The disadvantage of MPC is that it requires high calculation ability of a controller and accurate modeling of the system. Thanks to the rapid development of the micro-processor, the computational ability of state-of-the-art DSPs have been greatly improved. For example, the clock frequency of TMS320F28377D DSP is 200 MHz, the MPC algorithm can be easily implemented in such a DSP.

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# CHAPTER 3

# MODELING AND CONTROL OF SOLID STATE TRANSFORMER DC/DC STAGE: EFFICIENCY IMPROVEMENT

## 3.1 Introduction and Motivation

In the dc/dc stage, the dual-active bridge converter is well adapted for this application due to its excellent performance in voltage conversion, flexibility, high power density, galvanic isolation, modularity and high efficiency [3.1]-[3.4].

The conventional single phase-shift (SPS) modulation control is simple and easy to implement in many applications [3.5]-[3.7]. In order to improve the efficiency performance of the DAB, the SPS has been improved by using the multi-phase-shift control, such as extended phase-shift (EPS), dual phase-shift (DPS) and triple phase-shift (TPS) controls [3.8]-[3.10]. These three phase-shift control methods are classified by the different phase-shift angles, reducing the current stress and circulating energy in the circuits, thus the efficiency performance is improved. The TPS control is recognized as a unified phase-shift control, but the penalty of this control method is much complexity and increased design efforts. Compare with other phase-shift strategies, the DPS control has been popular due to its efficiency performance and its acceptable level of complexity. To further increase the power efficiency of the DAB, the multi-phase-shift controls are designed with the goal of minimum current stress [3.11] or minimum reactive power flow [3.12]. These two efficiency optimization methods can reduce the power loss in the DAB, but neither is a straightforward method. A more optimal strategy which can find the desired phase-shift angles

directly from the power loss model of the DAB. In the paper [3.13], a conventional loss model is utilized in an IGBT-based DAB. The saturation voltage of the IGBT along with the voltage drop of the diode are assumed as constant values. These assumptions may prevent the algorithm from calculating the expected phase-shift angle and couldn't guarantee the high efficiency performance. To increase the power density of the DAB wide bandgap devices, such as SiC MOSFETs or GaN FETs, are usually utilized today. Different from the IGBT, the MOSFET can have bidirectional current flow when its gate voltage is high enough, thus the operation of the MOSFET version of the DAB also differs from the DAB which utilizes IGBTs.

Compared with the aforementioned studies, a more accurate loss model is developed in this work to further improve the efficiency performance of the SiC-based dual-active bridge. A comprehensive operational analysis of the SiC-based DAB is also presented in this work. A detailed improved conduction loss model and switching loss model are given to construct a more accurate loss model of the DAB. For example, the loss model of a DAB will consider the effect of junction temperature, gate resistance, and gate voltage to the power loss. Furthermore, the impact of harmonic currents, as they relate to the losses, on auxiliary circuits and transformers is illustrated. According to the comparison of the proposed loss model with the aforementioned control of a SiC-based DAB from the experimental prototype testing results, the efficiency of the DAB is improved with varying input voltages and/or load power.

This chapter is organized as follows: Section II introduces the SiC MOSFET-based DAB operation principle. A simplified power loss model and an improved power loss model are presented in Section III, and finally, the simulation and experimental results are included in Section IV.

## 3.2 Dual Active Bridge Operation

### *3.2.1 Single phase-shift control*

The single phase-shift control is widely used in the dual-active bridge converter due to its simplicity. The switches $S_1$-$S_8$ are controlled with a 50% duty cycle. Leg 1 and Leg 3 have the phase-shift, and leg 2 and leg 4 have the same phase-shifts which are shown in Fig. 3-1. $v_{pri}$ is the voltage output from the primary side full bridge, and $v_{sec}$ is the voltage input to the secondary side full bridge. As shown in Fig. 3-2, with changing the phase-shift angle, the voltage across the inductor $L_k$ will change and then the power flows between the primary and secondary sides. The disadvantage of single phase-shift control is that the RMS and peak current of the switches are high due to the circulating power flow in the circuit [3.13], thus the efficiency of DAB with single phase-shift control is relatedly low.

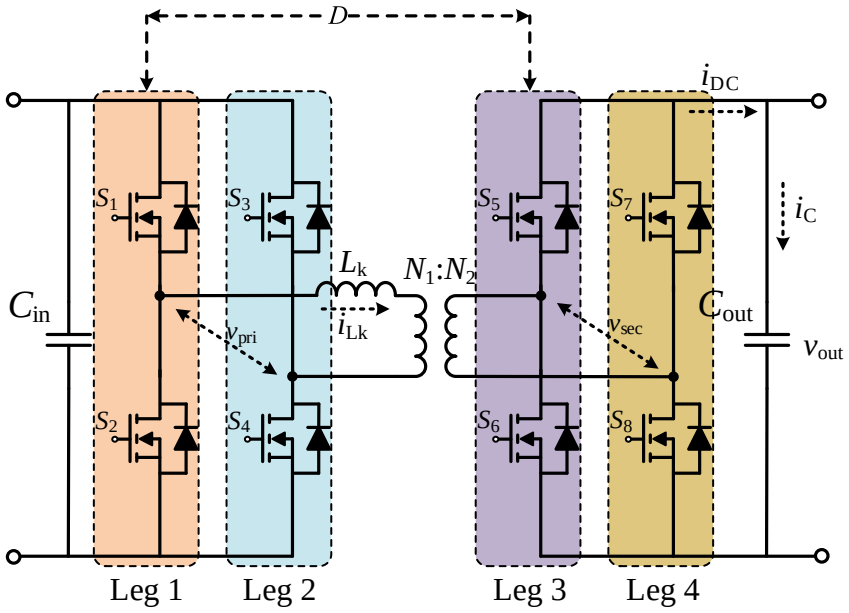



Fig. 3-1 Dual-Active Bridge with Single Phase-Shift Control

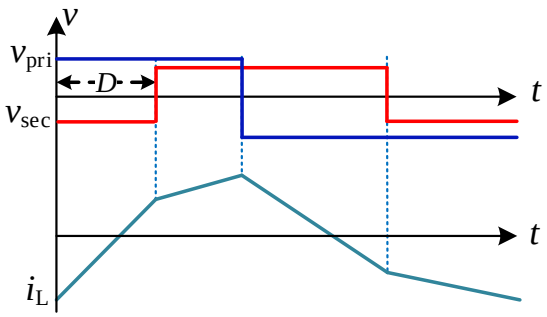



Fig. 3-2 Single Phase-Shift Control: The Transformer Input/Output Voltage and Inductor $L_k$ Current

### *3.2.2 Extended phase-shift control*

To reduce the RMS and peak current stress of the switches, while also improving the efficiency, the EPS control has been investigated in [3.8][3.14]. Comparing with SPS, EPS has the phase-shift between leg1 and leg2 which is shown in Fig. 3-3. There are two degrees of freedom to change the voltage difference, thus controlling the power flow. The first degree $D_o$ is used to control the magnitude and direction of power flow. The second degree $D_i$ is applied to reduce the circulating power and current stress of the converter. The detailed inductor voltage and current waveforms are given in Fig. 3-4.

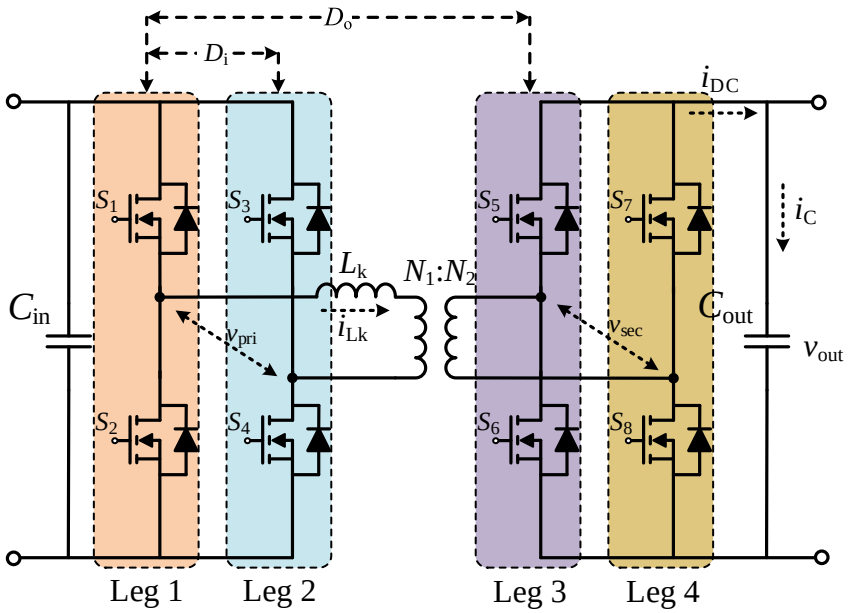



Fig. 3-3 Dual-Active Bridge with Extended Phase-Shift Control

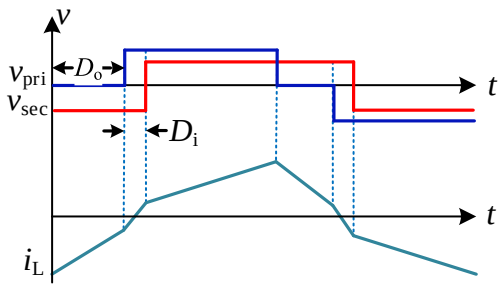



Fig. 3-4 Extended Phase-Shift Control: The Transformer Input/Output Voltage and Inductor $L_k$ Current

### *3.2.3 Dual-phase-shift control*

Another control method which gives two degrees of freedom using the phase-shift control method is DPS control. The difference between DPS and EPS is the phase-shift also exit in leg3 and leg4 and is the same phase-shift angle as leg1 and leg2 which is illustrated in Fig. 3-5. Compared with SPS control, DPS can effectively reduce the circulating energy and current stress,

however it also expands the soft-switching range [3.9][3.15]. The inductor voltage and current waveforms with DPS control is given in Fig. 3-6.

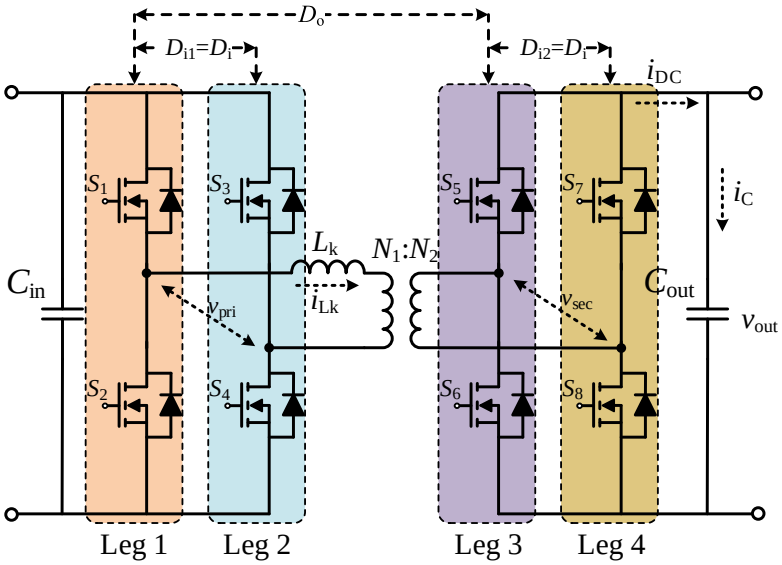



Fig. 3-5 Dual-Active Bridge with Dual Phase-Shift Control

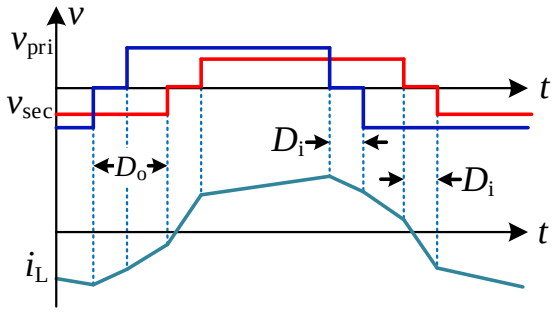



Fig. 3-6 Dual Phase-Shift Control: The Transformer Input/Output Voltage and Inductor $L_k$ Current

### *3.2.4 Triple phase-shift control*

As shown in Fig. 3-7, the TPS control method has three degrees of freedom [3.16]-[3.18]. The phase-shift $D_{i1}$ between leg1 and leg 2 is different with the phase-shift $D_{i2}$ between leg3 and leg4. In TPS control, the current stress is reduced and the soft-switching range is wider. The tradeoff is

that the design of TPS control is much more complicated than that of the SPS, EPS and DPS control methods. The input and output voltages of the transformer and inductor $L_k$ current are given in Fig. 3-8.

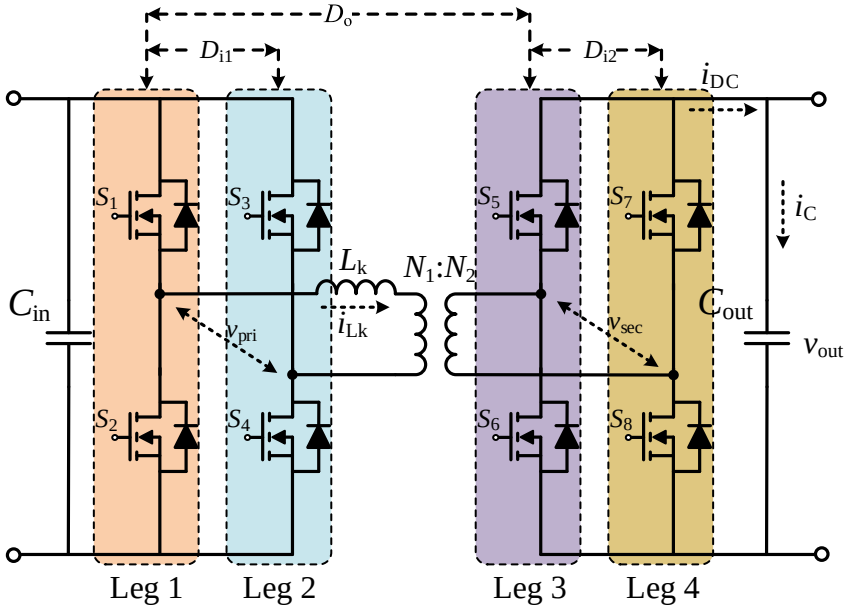



Fig. 3-7 Dual-Active Bridge with Triple Phase-Shift Control

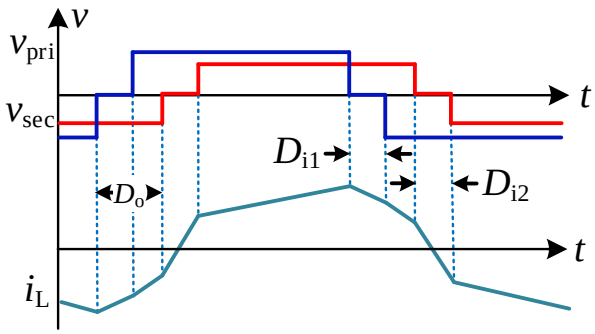



Fig. 3-8 Triple Phase-Shift Control: The Transformer Input/Output Voltage and Inductor $L_k$ Current

### *3.2.5 Conclusion*

Comparing these four phase-shift control strategies, the performance of TPS is the best but also the most complicate. The SPS control is the simplest but the high circulating currents and RMS or peak current stress. Compare EPS with DPS, the control state of the two full bridges are changed when the required power or voltage is changed, but DSP control doesn't, with this reason, the DPS control is adopted in the following section to achieve a relatively simple, effective and high efficiency control strategy.

## 3.3 Efficiency Optimization Methods

To improve the efficiency performance of the dual-active bridge converter, two popular methods are reported in [3.11][3.19][3.20]: (1) Peak current minimization method and (2) circulation power reduction method. The drawback of these two methods are the efficiency is not optimal in the wide range of the load power. A loss model based method is reported in [3.20][3.21]. In the paper [3.20], it is applied with an IGBT based-circuit and simple loss model. It assumed that the saturation voltage of IGBT and voltage drop of the diode are constant values, thus it may not realize the optimized efficiency performance. In the last few years, the wide bang-gap device has been widely used due to its fast switching capability and low on-state resistance, thus it is very suitable for the dual-active bridge converter application. In this section, a SiC MOSFET based dual-active bridge is analyzed and a more accurate loss model is developed to achieve better efficiency performance.

### *3.3.1 Current stress minimization method*

The control diagram of current stress minimization control is given in Fig. 3-9. The PI control is adopted in the voltage loop to regulate the dc bus voltage at the secondary side. The solved $D_i$

is fed as the forward signal added plus with the output of PI controller. The final stage of this control strategy is the phase-shift generator which can be realized by the controller.

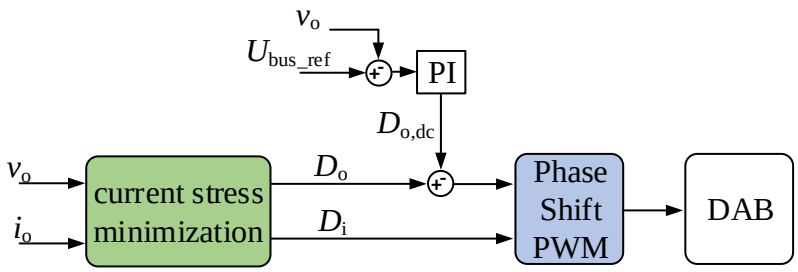



Fig. 3-9 Control Diagram of Current Stress Minimization

The phase-shift $D_i$ and $D_o$ are calculated by the Lagrangian expression. Lagrangian function is a strategy to find the minimum or maximum value of an object with some constraints. The normal Lagrangian expression is shown in Eq. (3-1).

$$L(x_1, x_2, ..., x_n, \lambda_1, \lambda_2, ..., \lambda_m) = f(x_1, x_2, ..., x_n) + \sum_{k=1}^{m} \lambda_k (g_k(x_1, x_2, ..., x_n) - c) \quad (3\text{-}1)$$

where the function $L$ is called the "Lagrangian", $f(x_1, x_2, \ldots, x_n)$ is the objective function, $g(x_1, x_2, \ldots, x_n)$ is the constraint function, $\lambda$ is defined as Lagrange multiplier, $c$ is the desired constant value of constraint function $g(x_1, x_2, \ldots, x_n)$.

In order to realize the control goal, set the gradient of Lagrangian expression equal to zero:

$$\begin{cases} \dfrac{\partial L(x_1, x_2, ..., x_n, \lambda_1, \lambda_2, ..., \lambda_m)}{\partial x_1} = 0 \\ \dfrac{\partial L(x_1, x_2, ..., x_n, \lambda_1, \lambda_2, ..., \lambda_m)}{\partial x_2} = 0 \\ \quad . \\ \quad . \\ \quad . \\ \dfrac{\partial L(x_1, x_2, ..., x_n, \lambda_1, \lambda_2, ..., \lambda_m)}{\partial x_n} = 0 \\ \dfrac{\partial L(x_1, x_2, ..., x_n, \lambda_1, \lambda_2, ..., \lambda_m)}{\partial \lambda_1} = 0 \\ \dfrac{\partial L(x_1, x_2, ..., x_n, \lambda_1, \lambda_2, ..., \lambda_m)}{\partial \lambda_2} = 0 \\ \quad . \\ \quad . \\ \quad . \\ \dfrac{\partial L(x_1, x_2, ..., x_n, \lambda_1, \lambda_2, ..., \lambda_m)}{\partial \lambda_m} \end{cases} \tag{3-2}$$

By solving Eq. (3-2), the desired $x_1$, $x_2$, …, $x_n$ can be found to achieve the minimum or maximum value of control objective.

In the DPS control, the two degrees of control variables are $D_i$ and $D_o$, and the Lagrangian expression is shown in Eq. (3-3).

$$L(D_i, D_o, \lambda) = i_{peak}(D_i, D_o) + \lambda(P_{out} - P_{ref}) \tag{3-3}$$

where $i_{peak}(D_i, D_o)$ is the peak current in the DPS control, $P_{out}$ is the power output of the DPS control, $P_{ref}$ is the reference power of the dual-active bridge.

The expression of $i_{peak}$ and $P_{out}$ can be derived from the current and voltage waveform of the leakage inductor. By solving Eq. (3-4), the calculated values $D_i$ and $D_o$ are the desired phase-shifts which can be realized with the minimum peak current stress.

$$\begin{cases} \dfrac{\partial L}{\partial D_i} = \dfrac{\partial i_{peak}}{\partial D_i} + \lambda \dfrac{\partial P_{out}}{\partial D_i} = 0 \\ \dfrac{\partial L}{\partial D_o} = \dfrac{\partial i_{peak}}{\partial D_o} + \lambda \dfrac{\partial P_{out}}{\partial D_o} = 0 \\ \dfrac{\partial L}{\partial \lambda} = P_{out} - P_{ref} = 0 \end{cases} \tag{3-4}$$

### *3.3.2 Circulating power reduction method*

Similar to the current stress minimization control, the Lagrangian expression of the circulating power reduction method is shown in Eq. (3-5). The circulating power $P_{\text{circutlation}}$ and output power of DAB $P_{\text{out}}$ can be derived from the current and voltage waveform of the leakage inductor.

$$L(D_i, D_o, \lambda) = P_{circulation}(D_i, D_o) + \lambda(P_{out} - P_{ref}) \tag{3-5}$$

Similar with the current stress optimization control, the desired phase-shift of $D_{\text{i}}$ and $D_{\text{o}}$ are solved by Eq. (3-6).

$$\begin{cases} \dfrac{\partial L}{\partial D_i} = \dfrac{\partial P_{circulation}}{\partial D_i} + \lambda \dfrac{\partial P_{out}}{\partial D_i} = 0 \\ \dfrac{\partial L}{\partial D_o} = \dfrac{\partial P_{circulation}}{\partial D_o} + \lambda \dfrac{\partial P_{out}}{\partial D_o} = 0 \\ \dfrac{\partial L}{\partial \lambda} = P_{out} - P_{ref} = 0 \end{cases} \tag{3-6}$$

The control diagram of circulating power reduction method is given in Fig. 3-10. The difference with the current stress minimization control is that the desired phase-shift is based on the control of minimization of the circulating power.

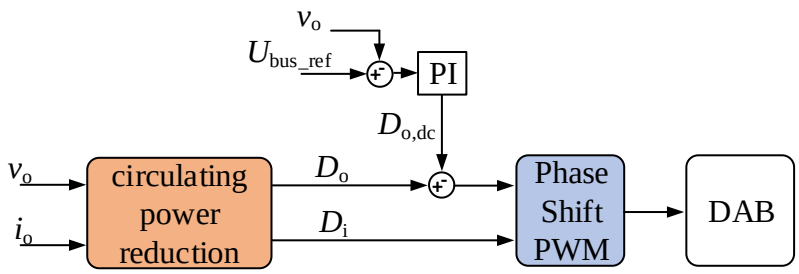



Fig. 3-10 Control Diagram of Circulating Power Reduction

In the next section, a loss model based on the efficiency optimization method is proposed. In order to build the loss model, the operation principle of the dual-active bridge is introduced first, then the simple and more accurate loss model are developed and compared.

## 3.4 SiC MOSFET-based DAB Operation Principle

There are two operational conditions of the dual-phase-shift control method, which are $D_o<D_i$ and $D_i<D_o$, where $D_i$ is the inner phase-shift and $D_o$ is the outer phase-shift. This dissertation mainly discusses the case of $D_i<D_o$. The analysis steps of $D_o<D_i$ are the same. The operation principle of dual-active bridges in the dual-phase-shift model is given in Fig. 3-12. From $t_0$ to $t_{10}$, there are 10 stages.

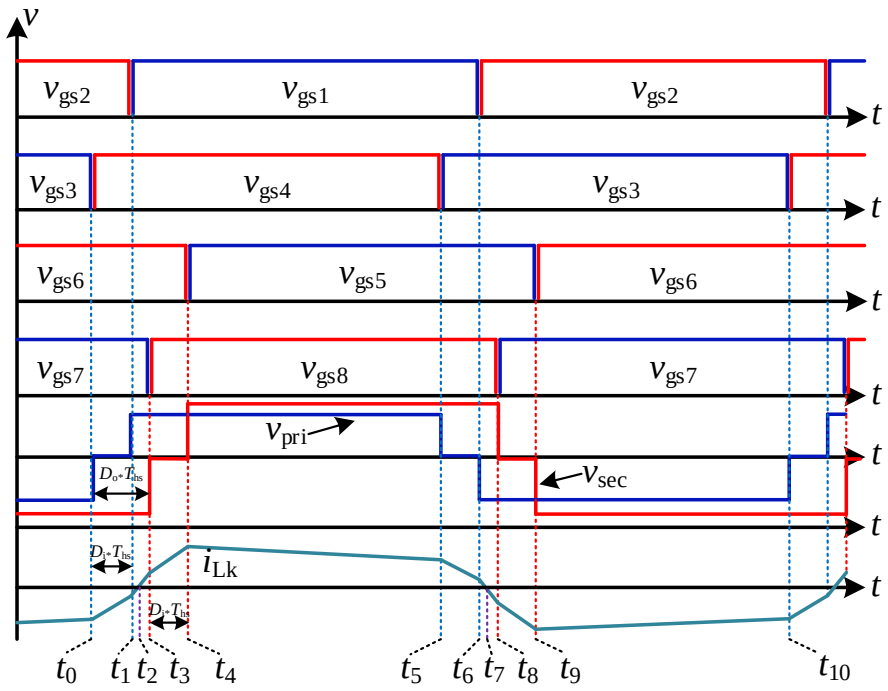
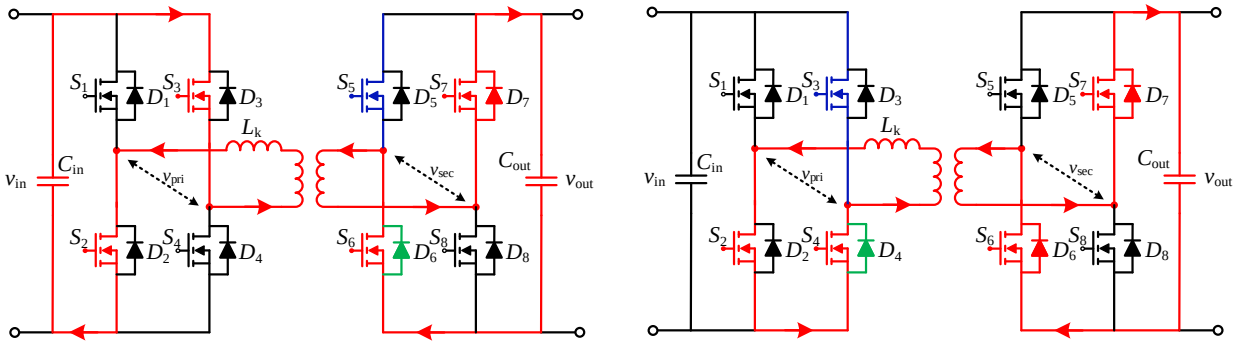
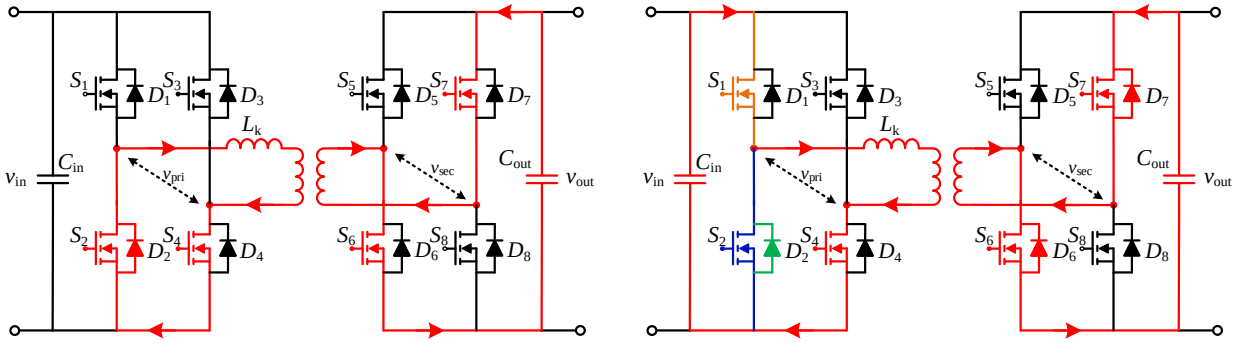



Fig. 3-11 Control Signal and Circuits Waveform when $D_i$<$D_o$



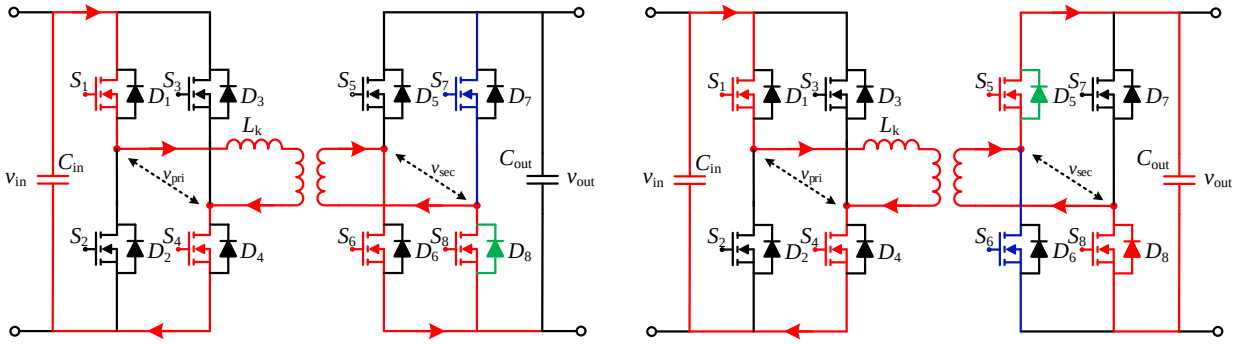

(a) Stage 10: $t_9$<$t_{10}$

(b) Stage 1: $t_0$<$t_1$




(c) Stage 2: $t_1$<$t_2$

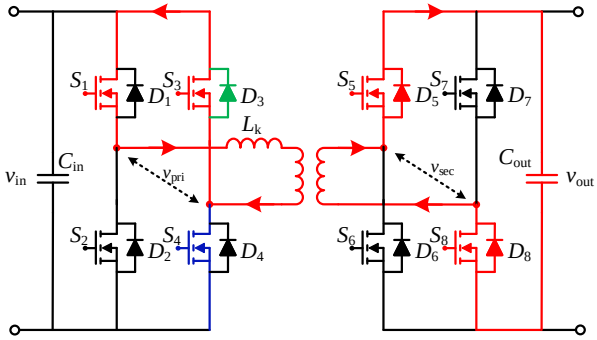
(d) Stage 3: $t_2$<$t_3$



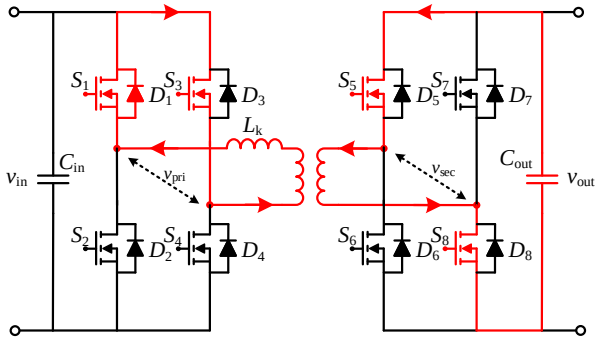

(e) Stage 4: $t_3$<$t_4$



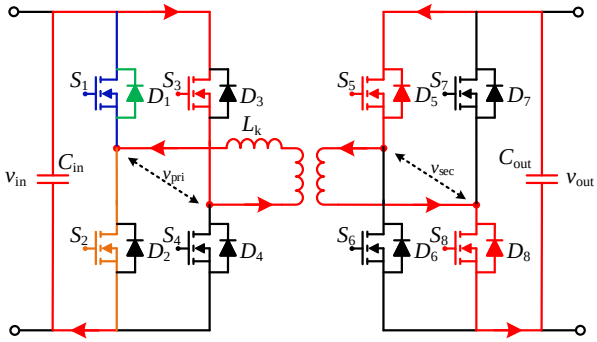

(f) Stage 5: $t_4$<$t_5$



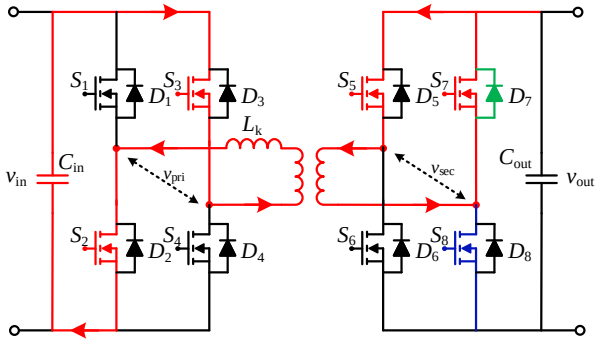

(g) Stage 6: $t_5$<$t_6$




(h) Stage 7: $t_6$<$t_7$




(i) Stage 8: $t_7$<$t_8$




(j) Stage 9: $t_8$<$t_9$

Fig. 3-12 10 Operational Stages when $D_i$<$D_o$

The current equations for 10 stages are given in Table 3.1.

.

Table 3.1 The Inductor $L_k$ Current Equations, $D_i<D_o$

| Time | Primary side ac voltage, $v_{pri}$ | Secondary side ac voltage, $v_{sec}$ | Current equation |
|---|---|---|---|
| $t_9 \sim t_{10}$ | $-v_{in}$ | $-N*v_{out}$ | $v_L = L_k \frac{di}{dt} \Rightarrow (v_{pri} - v_{sec}) = L_k \frac{i_{Lk}(t) - i_{Lk}(t_9)}{t - t_9}$ $\Rightarrow i_{Lk}(t) = i_{Lk}(t_9) + \frac{-v_{in} + Nv_{out}}{L_k}(t - t_9)$ |
| $t_0 \sim t_1$ | 0 | $-N*v_{out}$ | $i_{Lk}(t) = i_{Lk}(t_0) + \frac{Nv_{out}}{L_k}(t - t_0)$ |
| $t_1 \sim t_2$ | 0 | $-N*v_{out}$ | $i_{Lk}(t) = i_{Lk}(t_1) + \frac{Nv_{out}}{L_k}(t - t_1)$ |
| $t_2 \sim t_3$ | $v_{in}$ | $-N*v_{out}$ | $i_{Lk}(t) = i_{Lk}(t_2) + \frac{v_{in} + Nv_{out}}{L_k}(t - t_2)$ |
| $t_3 \sim t_4$ | $v_{in}$ | 0 | $i_{Lk}(t) = i_{Lk}(t_3) + \frac{v_{in}}{L_k}(t - t_3)$ |
| $t_4 \sim t_5$ | $v_{in}$ | $N*v_{out}$ | $i_{Lk}(t) = i_{Lk}(t_4) + \frac{v_{in} - Nv_{out}}{L_k}(t - t_4)$ |
| $t_5 \sim t_6$ | 0 | $N*v_{out}$ | $i_{Lk}(t) = i_{Lk}(t_5) + \frac{-Nv_{out}}{L_k}(t - t_5)$ |
| $t_6 \sim t_7$ | 0 | $N*v_{out}$ | $i_{Lk}(t) = i_{Lk}(t_6) + \frac{-Nv_{out}}{L_k}(t - t_6)$ |
| $t_7 \sim t_8$ | $-v_{in}$ | $N*v_{out}$ | $i_{Lk}(t) = i_{Lk}(t_7) + \frac{-v_{in} - Nv_{out}}{L_k}(t - t_7)$ |
| $t_8 \sim t_9$ | $-v_{in}$ | 0 | $i_{Lk}(t) = i_{Lk}(t_8) + \frac{-v_{in}}{L_k}(t - t_8)$ |

Stage 1, $t_0<t<t_1$: At time $t<t_0$, $S_2$, $S_3$, $S_6$, and $S_7$ are on. At $t_0$, $S_3$ turns off first. To prevent the dc bus voltage short through, a short dead time $t_d$ is set between $S_3$ and $S_4$. The diode $D_4$ is conducting in freewheeling mode during the dead time. At time $t_0+t_d$, the gate signal of $S_4$ is high level, then

$S_4$ is turned on at zero-voltage switching (ZVS). Due to the fact that MOSFETs allow bidirectional current flow, a large proportion of current will flow from source to the drain when the gate voltage is much higher than the threshold voltage. Then diode $D_4$ turns off and leads to reverse-recovery loss.

Stage 2: The MOSFETs in the primary and secondary sides are still conducting, but the current direction at both sides are changed at time $t_1$.

Stage 3: At time $t<t_2$, $S_2$, $S_4$, $S_6$ and $S_7$ are on, $S_2$ turns off at time $t_1$, then $D_2$ is conducting as freewheeling diode. After time $t_1+t_d$, $S_1$ is turned on at hard switching mode and $D_2$ turns off.

Stage 4: The primary side switches keep the same status as the previous stage, the secondary side switch $S_7$ is turned off at time $t_2$, $D_7$ conducts during the dead time. At time $t_2+t_d$, $S_8$ turns on and $D_7$ is off.

Stage 5: During this stage, $S_1$ and $S_4$ only have conducting loss. $S_6$ turns off at time $t_4$, $D_5$ is on immediately. At time $t_4+t_d$, $S_5$ turns on at ZVS.

Stage 6: The secondary side switches $S_5$ and $S_8$ are always on during this stage. $S_4$ turns off and $D_3$ is on at time $t_5$. $S_3$ turns on at ZVS.

Stage 7: In this stage, the current direction changed in the primary and secondary sides. Only conduction loss is happened in this stage.

Stage 8. The MOSFET $S_1$ turns off at time $t_6$, then the diode $D_1$ is conducting during dead time. $S_2$ turns on with hard switching at time $t_6+t_d$. The status of secondary side switches are the same as stage 7.

Stage 9: The switches of primary side stay the same status as in stage 7. The secondary side switch $S_8$ turns off at time $t_7$, the diode $D_8$ conducts the current until $S_7$ soft switching turns on.

Stage 10: This stage is the last stage in one switching period. The status of primary side's switches are same as in stage 9. $S_5$ is turned off at $t_9$ then $D_6$ is conducting the current. $S_5$ is turned at ZVS.

From the operational principle of the dual-phase-shift control in the dual-active bridge, the switching actions are summarized in Table 3.2. The conduction actions are shown in Table 3.3.

Table 3.2 The Switching Actions in One Switching Period

| Hard turn-off | Soft turn-off | Hard turn-on | Soft turn-on | Diode reverse recovery |
|---|---|---|---|---|
| $S_3$ at $t_0$,<br>$S_7$ at $t_3$,<br>$S_6$ at $t_4$,<br>$S_4$ at $t_5$,<br>$S_8$ at $t_8$,<br>$S_5$ at $t_9$ | $S_2$ at $t_2$,<br>$S_1$ at $t_7$ | $S_1$ at $t_2$,<br>$S_2$ at $t_7$ | $S_4$ at $t_0$,<br>$S_8$ at $t_3$,<br>$S_5$ at $t_4$,<br>$S_3$ at $t_5$,<br>$S_7$ at $t_8$,<br>$S_6$ at $t_9$ | $D_4$ at $t_0$,<br>$D_2$ at $t_2$,<br>$D_8$ at $t_3$,<br>$D_5$ at $t_4$,<br>$D_3$ at $t_5$,<br>$D_1$ at $t_7$,<br>$D_7$ at $t_8$,<br>$D_6$ at $t_9$ |

Table 3.3 The Conduction Actions in One Switching Period

| Time | $t_0$-$t_1$,<br>$t_1$-$t_2$ | $t_2$-$t_3$ | $t_3$-$t_4$ | $t_4$-$t_5$ | $t_5$-$t_6$,<br>$t_6$-$t_7$ | $t_7$-$t_8$ | $t_8$-$t_9$ | $t_9$-$t_{10}$ |
|---|---|---|---|---|---|---|---|---|
| MOSFET | $S_2$, $S_4$,<br>$S_6$, $S_7$ | $S_1$, $S_4$,<br>$S_6$, $S_7$ | $S_1$, $S_4$,<br>$S_6$, $S_8$ | $S_1$, $S_4$,<br>$S_5$, $S_8$ | $S_1$, $S_3$,<br>$S_5$, $S_8$ | $S_2$, $S_3$,<br>$S_5$, $S_8$ | $S_2$, $S_3$,<br>$S_5$, $S_7$ | $S_2$, $S_3$,<br>$S_6$, $S_7$ |

## 3.5 Simplified Power Loss Model and Improved Power Loss Model

### *3.5.1 Switching loss analysis and modeling*

#### *3.5.1.1 Turn-on loss model*

The main turn-on or turn-off power loss happens when the gate voltage is between the thresh hold voltage $V_{th}$ and plateau voltage $V_{plateau}$. During the turn-on process, when $V_{gs}$ reaches $V_{th}$, the current path is changed from the body diode to MOSFET. During this period, the power loss can be calculated as turn-on loss of the MOSFET and reverse-recovery loss of free-wheeling diode. From the simple turn-on loss calculation method, the current rise time and voltage fall time is assuming constant values. Thus, from switching scenarios in Fig. 3-11 and Fig. 3-12, the Eq. (3-7) is presented as the turn-on loss.

$$P_{on\_MOS\_simple} = \frac{v_{in}\left(i(t_2)+i(t_7)\right)\left(t_{d,on}+t_r\right)}{2} f_s, \text{ when } D_i<D_o \tag{3-7}$$

where, $t_{d,on}$ is turn-on delay time, $t_r$ is rise time of switch.

In this work, the more accurate turn-on loss model is considered with the contribution of the gate voltage, gate resistance and dc bus voltage to the switching loss. The gate resistance should be adjusted to realize fast turn-on and turn-off but acceptable $V_{ds}$ overshoot. The gate current during turn-on is shown in Eq. (3-8). The voltage fall time can be calculated in Eq. (3-9). Then, the turn-on energy loss and the power loss in a switching period are given in Eq. (3-10).

$$i_{g,on} = \frac{V_{driver} - V_{plateau}}{R_{driver} + R_{gate}} \tag{3-8}$$

$$\begin{cases} i_c = C\dfrac{dv}{dt} \Rightarrow dt = C\dfrac{dv}{i_c} \\ t_{fu1} = C_{gd1}\dfrac{v_{in} - R_{on,MOS}(T_j)i(t)}{i_{g,on}} \\ t_{fu2} = C_{gd2}\dfrac{v_{in} - R_{on,MOS}(T_j)i(t)}{i_{g,on}} \end{cases} \tag{3-9}$$

$$\begin{cases} E_{on\_MOS} = \int_0^{t_{on}} v_{ds}(t)i(t)dt = \dfrac{v_{in}i(t)\left(t_{ri} + (t_{fu1} + t_{fu2})/2\right)}{2} \\ E_{rr\_diode} = Q_{rr}v_{ds}(t) \qquad \text{when } D_i<D_o \\ E_{on} = E_{on\_MOS} + E_{rr\_diode} \\ P_{on\_MOS\_accurate} = E_{on}f_s \end{cases} \tag{3-10}$$

where $V_{drive}$ is the supplied gate voltage, $R_{gate}$ is the internal gate resistance, and $R_{driver}$ is the external gate resistance. $C_{gd1}$ and $C_{gd2}$ are the associated gate capacitance which can be read from the datasheet. $t_{ri}$ is the current rise time which is given in the device datasheet.

### *3.5.1.2 Turn-off loss model*

Same as the turn-on loss model, as given in the Table 3.2, the turn-off loss simple and more accurate model of SiC MOSFET are given in Eqs. (3-11)(3-12) and Eqs. (3-13)(3-14), respectively. In the Eq. (3-11), the switch turn-off time parameters are red from the datasheet directly. In the accurate model as shown in Eq. (3-14), the junction temperature is considered as variable in the accurate loss model. The gate resistance and voltage are used in the turn-off loss model.

$$P_{off\_MOS\_simple} = \frac{\left(v_{in}\left(i(t_0) + i(t_3) + i(t_4)\right) + Nv_{in}\left(i(t_5) + i(t_8) + i(t_9)\right)\right)\left(t_{d,off} + t_f\right)}{2} f_s, \text{ when } D_i<D_o \tag{3-11}$$

where, $t_{d,off}$ is the turn-off delay time, $t_f$ is the switch fall time of switch.

$$i_{g,off} = \frac{-V_{plateau}}{R_{driver} + R_{gate}} \tag{3-12}$$

$$\begin{cases} i_c = C\dfrac{dv}{dt} \Rightarrow dt = C\dfrac{dv}{i_c} \\ t_{ru1} = C_{gd1}\dfrac{v_{in} - R_{on,MOS}(T_j)i(t)}{i_{g,off}} \\ t_{ru2} = C_{gd2}\dfrac{v_{in} - R_{on,MOS}(T_j)i(t)}{i_{g,off}} \end{cases} \tag{3-13}$$

$$\begin{cases} E_{off\_MOS} = \displaystyle\int_0^{t_{off}} v_{ds}(t)i(t)dt = \frac{v_{in}i(t)\left(t_{ri} + (t_{ru1} + t_{ru2})/2\right)}{2} & \text{when } D_i < D_o \\ P_{off\_MOS\_accurate} = E_{off\_MOS} f_s \end{cases} \tag{3-14}$$

### *3.5.2 Conduction loss analysis and modeling*

The conventional way to calculate the MOSFET conduction loss is assuming the on-stage resistance $R_{dson}$ is a constant value, which is based on constant junction temperature $T_j$ and drain-source current. However, the $R_{dson}$ may vary greatly when $T_j$ changes. For example, the $R_{dson}$ of C2M0080120D at 25℃ is about 80 mΩ, but increased about 18% when the junction temperature is 75℃. Through the curve-fit method, the relationship of $R_{dson}$ verses $T_j$ of C2M0080120D is given in Eq. (3-15). If $T_j$ is sensed as feedback, then the more accurate $R_{dson}$ can be predicted. Based on the aforementioned operational scenarios, the conduction loss based on constant and varied $R_{dson}$ from SiC MOSFET can be derived as Eqs. (3-16) and (3-17), respectively.

$$R_{on,MOS}(T_j) = 0.08\left(0.95358 + 0.00109\,T_j + 0.0000208\,T_j^2\right) \tag{3-15}$$

$$P_{cond\_MOS\_simple} = \left( \frac{\int_{t_0}^{t_1} |i_{Lk}(t)|dt + \int_{t_1}^{t_2} |i_{Lk}(t)|dt + \int_{t_2}^{t_3} |i_{Lk}(t)|dt + \int_{t_3}^{t_4} |i_{Lk}(t)|dt + \int_{t_4}^{t_5} |i_{Lk}(t)|dt}{T_s/2} \right)^2 R_{on,MOS} \quad (3\text{-}16)$$

$$P_{cond\_MOS\_accurate} = \left( \frac{\int_{t_0}^{t_1} |i_{Lk}(t)|dt + \int_{t_1}^{t_2} |i_{Lk}(t)|dt + \int_{t_2}^{t_3} |i_{Lk}(t)|dt + \int_{t_3}^{t_4} |i_{Lk}(t)|dt + \int_{t_4}^{t_5} |i_{Lk}(t)|dt}{T_s/2} \right)^2 R_{on,MOS}(T_j) \quad (3\text{-}17)$$

where, $R_{on.MOS}$ is the switch on-sate resistance.

### *3.5.3 The power loss from the transform and auxiliary inductor*

The two main losses associated with the transformer are core and copper losses. The core loss calculation is based on the Improved Generalised Steinmetz Equation (IGSE) using the parameters for the core materials as shown in Eq. (3-18).

$$P_C = 2^{a+b} k_i f_{DAB}^{a} B_m^{b} D^{1-a} \quad (3\text{-}18)$$

where,

$a$, $b$, $k_i$ are the Steinmetz coefficients.

$B_m$ is the peak flux amplitude.

$f_{DAB}$ is the frequency of transformer.

$D$ is the duty ratio of DAB.

The windings are considered to be composed of circular Litz wire arranged in a concentric manner. The calculation for ac winding loss is based on the simplified approach used in [3.22]

(valid for low penetration ratios) which is a development of the approach outlined by Lammeraner and Stafl in [3.23] as presented in Eqs. (3-19) and (3-20). The calculation of losses include the harmonic content of the current in the transformer.

$$P_{wp} = \sum_{v=1}^{n} \left( \frac{I_v}{\sqrt{2}} \right)^2 F_{rv} R_p \tag{3-19}$$

$$P_{ws} = \sum_{v=1}^{n} \left( \frac{I_v}{\sqrt{2}} \right)^2 F_{rv} R_s \tag{3-20}$$

where, $I_v$ is the each current harmonic. $R_p$, $R_s$ are the resistance for each of the windings. $F_{rv}$ is the resistance factor.

There are core and copper losses in the high-frequency transformer and auxiliary inductor. The core loss $P_{core}$ can be derived as Eq. (3-21) [3.24].

$$P_{core} = \frac{2N^2 V_e mu_o^2 I_{rms}^2 f_s}{g^2} \tag{3-21}$$

where $I_{rms}$ is the root mean square value of the auxiliary inductor current.

The copper loss from high-frequency transformer and auxiliary inductor are shown in Eqs. (3-22) and (3-23), respectively.

$$P_{copp} = (R_{au} + R_{tr}) I_{rms}^2 \tag{3-22}$$

Thus the total loss of the high-frequency transformer and auxiliary inductor is:

$$P_{TX,L,loss} = P_{core} + P_{copp} \tag{3-23}$$

## 3.6 The Total Loss Model

According to the aforementioned loss analysis, the global loss of the dual-active bridge is the sum of power losses from switches, the high-frequency transformer, and the auxiliary inductor. Combine the turn-on loss equations (3-7)(3-10), turn-off loss equations (3-11)(3-14), conduction loss equations (3-16)(3-17) and transformer and inductor loss equation (3-23), the total loss equation with simple and accurate loss models are given in Eqs. (3-24) and (3-25), respectively.

$$P_{global\,loss,simple} = (P_{on\_MOS\_simple} + P_{off\_MOS\_simple}) + P_{cond\_MOS\_simple} + P_{TX,L,loss} \tag{3-24}$$

$$P_{global\,loss,accurate} = (P_{n\_MOS\_accurate} + P_{off\_MOS\_accurate}) + P_{cond\_MOS\_accurate} + P_{TX,L,loss} \tag{3-25}$$

## 3.7 Efficiency Optimized Method: Lagrangian Objective Function

### *3.7.1 Power delivery capability*

When $D_i<D_o$, the output power of the DAB is calculated as shown in Eq. (3-26). When $D_o<D_i$, the output power can be derived as the similar method which is given in Eq. (3-27).

$$P_{out,D_i<D_o} = \frac{\int_{t_0}^{t_{10}} v_{pri} i_{Lk}(t)dt}{T_s} = -\frac{(D_i^2 + 2(-1+D_o)D_o)nT_sV_iV_o}{4L} \tag{3-26}$$

$$P_{out,D_o<D_i} = -\frac{D_o(-2+2D_i+D_o)nT_sV_iV_o}{4L} \tag{3-27}$$

The output power curve of Eq. (3-26) is plotted in Fig. 3-13. It can be seen that, dual-phase-shift has many sets of $D_i$ and $D_o$ to meet the output power requirement. The related power loss curves are illustrated in Fig. 3-14. It can be seen that the DAB converter has different power loss with different sets of $D_i$ and $D_o$, which means if the phase-shift is calculated properly, the DAB will not only deliver the desired power, but also the lowest power loss is minimized.

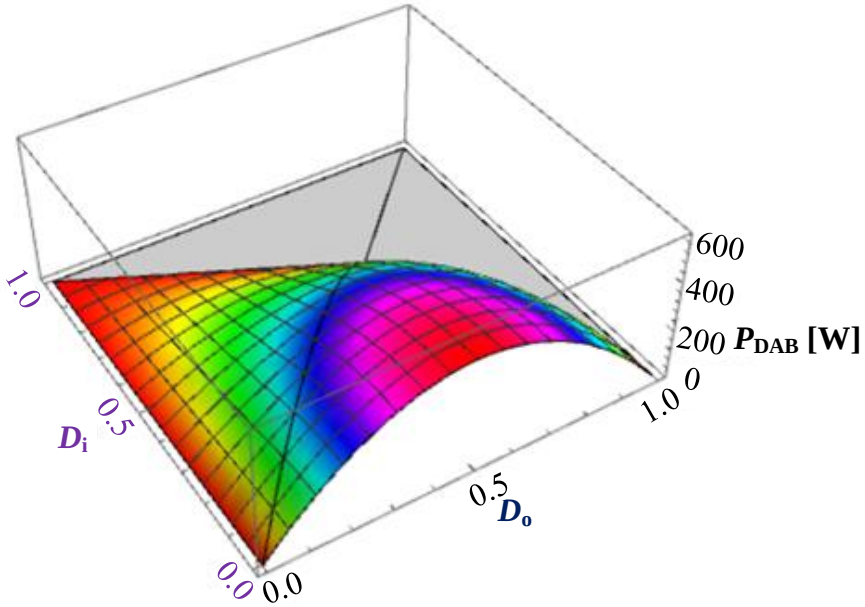



Fig. 3-13 Power Curve of the DAB with Dual-Phase-Shift Control

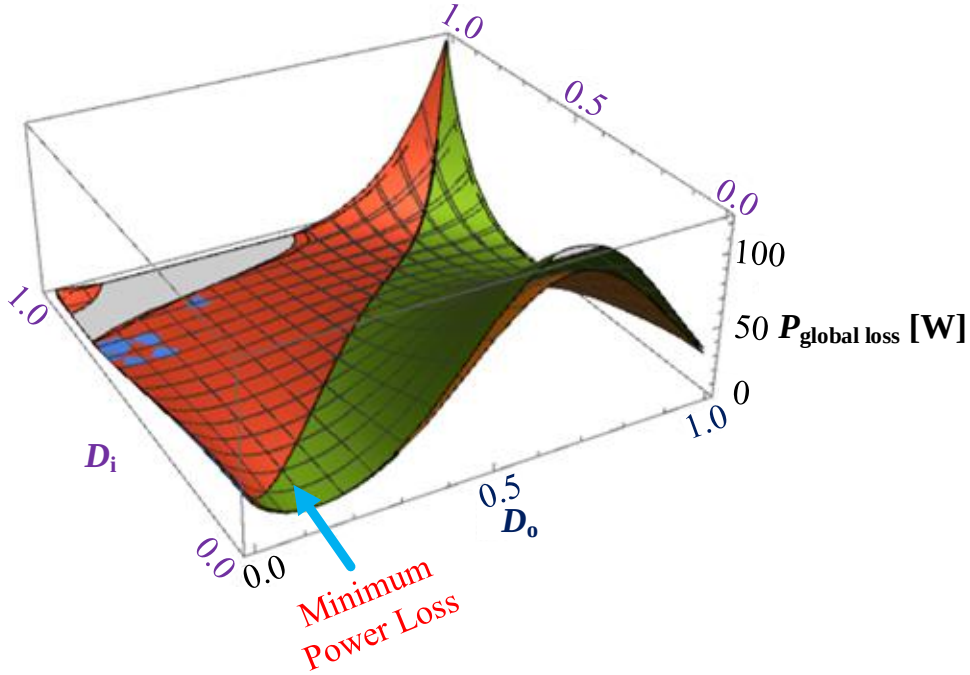



Fig. 3-14 Power Loss 3D Plot when DAB with Dual-Phase-Shift Control

### *3.7.2 Minimum power loss design*

To find the desired dual-phase-shift $D_i$ and $D_o$, the Lagrangian expression of the power loss minimization is utilized in this paper. The main idea is to adjust the efficiency $\lambda$ to satisfy the minimum power loss constraint. The simple loss model and the accurate loss based Lagrangian expression is given in Eq. (3-28) and Eq. (3-29), respectively.

$$L_{simple}(D_i, D_o, \lambda) = P_{global\ loss,simple}(D_i, D_o) + \lambda(P_{out,D_i<D_o} - P_{ref}) \tag{3-28}$$

$$L_{accurate}(D_i, D_o, \lambda) = P_{global\ loss,accurate}(D_i, D_o) + \lambda(P_{out,D_i<D_o} - P_{ref}) \tag{3-29}$$

Then the equations to resolve the $D_i$ and $D_o$ with simple loss model and accurate loss model are shown in Eq. (3-30) and Eq. (3-31), respectively.

$$\begin{cases} \dfrac{\partial L_{simple}}{\partial D_i} = \dfrac{\partial P_{global\ loss,simple}}{\partial D_i} + \lambda \dfrac{\partial P_{out,D_i<D_o}}{\partial D_i} = 0 \\ \dfrac{\partial L_{simple}}{\partial D_o} = \dfrac{\partial P_{global\ loss,simple}}{\partial D_o} + \lambda \dfrac{\partial P_{out,D_i<D_o}}{\partial D_o} = 0 \\ \dfrac{\partial L_{simple}}{\partial \lambda} = P_{out,D_i<D_o} - P_{ref} = 0 \end{cases} \tag{3-30}$$

$$\begin{cases} \dfrac{\partial L_{accurate}}{\partial D_i} = \dfrac{\partial P_{global\ loss,accurate}}{\partial D_i} + \lambda \dfrac{\partial P_{out,D_i<D_o}}{\partial D_i} = 0 \\ \dfrac{\partial L_{accurate}}{\partial D_o} = \dfrac{\partial P_{global\ loss,accurate}}{\partial D_o} + \lambda \dfrac{\partial P_{out,D_i<D_o}}{\partial D_o} = 0 \\ \dfrac{\partial L_{accurate}}{\partial \lambda} = P_{out,D_i<D_o} - P_{ref} = 0 \end{cases} \tag{3-31}$$

For example, for 155 V input voltage and 60 V output voltage, with the same load power 240 W, the calculation results of dual-phase-shift ($D_i$, $D_o$) from the simple loss model and the accurate loss model are (0.0411, 0.2074) and (0.0554, 0.2086). Since there is only one solution from the Lagrangian expression, if the loss model is not good enough, the calculated $D_i$ and $D_o$ will not

result in the lowest power loss, thus the best efficiency performance cannot be achieved. The experimental results will verify this in the section.

### *3.7.3 Control strategy of DAB with loss model*

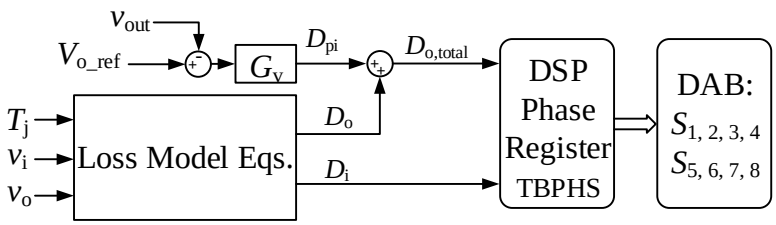



Fig. 3-15 Control Diagram of Power Loss Minimization

The control scheme of the DAB is given in Fig. 3-15. The inner phase-shift and outer phase-shift is calculated by Eqs. (3-30) and (3-31). In order to maintain the output bus voltage during input voltage or load power transients, a PI control is utilized to modify the outer phase-shift. The calculated $D_o$ as feed forward phase-shift and added with the output of PI controller to improve the transient performance. In the steady state, the output $D_{o,total}$ should be equal to $D_o$ to realize the goal of the smallest power loss.

## 3.8 Experimental Verification

The experimental results of the DAB converter are shown in Fig. 3-16 and Fig. 3-17. These results were obtained using a TI DSP TMS320F28335 and CREE SiC MOSFET. The switching frequency is 50 kHz. Since the expression of $D_o$ and $D_i$ are very complicated, in order to save the calculation time of the DSP, a look-up table is built based on the circuit parameters. In every switching cycle, the optimized $D_o$ and $D_i$ are selected based on the feedback of $T_j$, $V_i$ and $V_o$. To measure the efficiency, the multi-channel power analyzer PA3000 from Tektronix is utilized. In

the experiment, the simple and accurate loss models of the SiC MOSFET are tested and compared. These two loss models are tested in two cases:

(a) Same $V_{out\_ref}$ and same load power, different $V_{in}$.

(b) Same $V_{in}$, different $V_{out\_ref}$, or Same $V_{in}$, different load power.

### *3.8.1 Same $V_{out\_ref}$ and same load power, different $V_{in}$*

In this scenario, the input voltage increases from 100 V to 250 V, the reference output voltage is set as 60 V. Then the voltage ratio is varied. The transmission power is 500 W. With different dc input voltages, the efficiency testing results are shown in Fig. 3-16. It is demonstrated that the efficiency has increased at least 1% with the accurate loss model control. It can be concluded that the more accurate loss model helps to predict the correct inner and outer phase-shift to maximize the system efficiency.

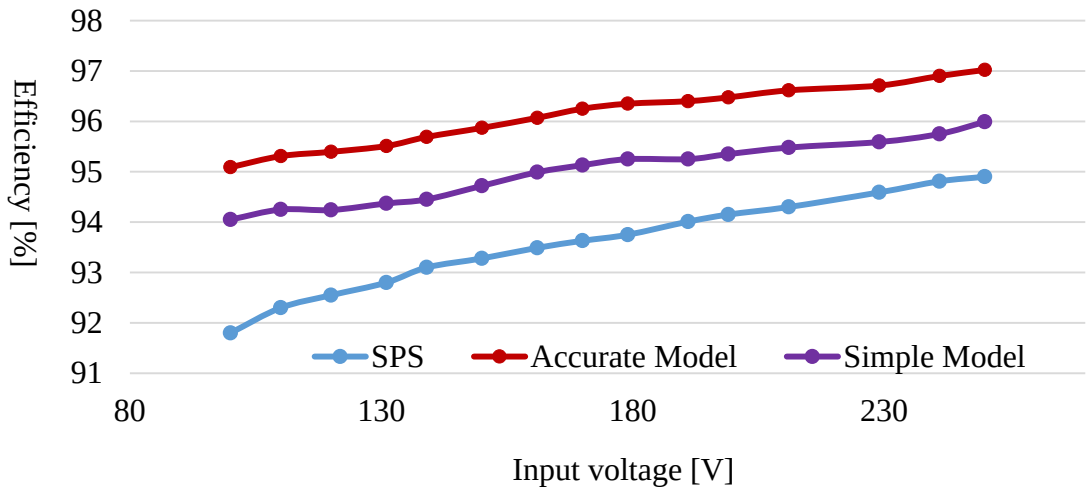



Fig. 3-16 Efficiency Testing Results of SPS, Accurate Model and Simple Model with Vary Input Voltage

### *3.8.2 Same $V_{in}$, different load power*

The input and output voltage are fixed at 200 V and 60 V, respectively. The load power is varied from 135 W to 480 W. The measured efficiency is compared with the different loads as shown in Fig. 3-17. The efficiency is again shown to be improved by utilizing the accurate loss model of DAB.

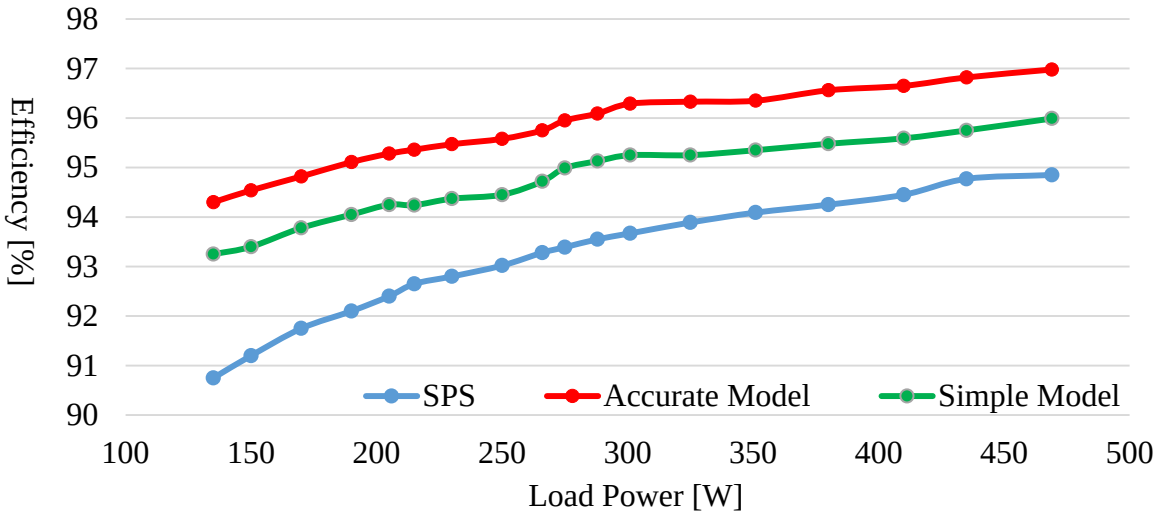



Fig. 3-17 Efficiency Testing Results of SPS, Accurate Model and Simple Model with Varying Load Power

## 3.9 Loss Model Based Efficiency Improvement Conclusion

The optimized and accurate loss model is developed for a dual-active bridge converter to improve efficiency performance. The accurate loss model is improved from three aspects: conduction loss model, switching loss model, and high frequency transformer loss model. Compared with the simple loss model, the proposed accurate loss model can predict the more accurate inner and outer phase-shift. From the theoretical and experimental results, the proposed accurate loss model can effectively increase the system efficiency by reducing the power loss. The power losses are mainly effected by the conduction loss.

## 3.10 Transient Performance Improvement Methods

In this section, a novel control strategy to improve dynamic and efficiency performance of dual-active bridge converters is investigated. The proposed control method is based on a new virtual capacitance concept with K-factor approach for obtaining better stability and performance for a closed-loop DAB. Because the capacitor is not real, a large capacitance can be obtained without taking much space and cost. Moreover, a virtual capacitance can be designed to have nonlinear characteristics and respond selectively to the desired signals. And the K-factor control can provide the desired phase boost to get the targeted phase margin at the crossover frequency. The efficiency is optimized through the power loss model of the DAB. Dual phase-shift control is designed to maximum the efficiency performance in the DAB. The closed-loop control system has been implemented in a real hardware experiment. The comparative closed-loop performances of a DAB converter with classical PI, single K-factor and virtual capacitor based K-factor controllers have been produced. Simulations and experimental results are provided to demonstrate the effectiveness of the DAB small signal model and K-factor virtual capacitor for the proposed DAB converter. Design and implementation of K-factor virtual capacitor controller for DAB converters has not been reported in any literature before.

### *3.10.1 Introduction*

The controller design is critical to the performance of DAB converters. The classic PI and other control methods have been applied to DAB converters in solid-state transformers (SST) applications [3.25]-[3.28]. However, very limited papers have presented the detailed controller design procedures and validated the effectiveness under varying operating conditions. In addition, the major studies on the controller design for DAB converters are focused on the use of classic PI controllers. Qin et al., analyzed the closed-loop gain of a DAB converter controlled by a PI

controller and also highlighted its limitations in [3.29]. It has been shown that it is difficult for the PI controllers to track and reject disturbances induced by 120 Hz double-line frequency harmonic current from the inverter due to the limited controller bandwidth.

The classic PI controller design relies on the small-signal model and parameters of the DAB converters. Consequently, load variations and parametric uncertainties may degrade its performance [3.30]. The PI controller can ensure system stability around an equilibrium point. However, large external perturbations, such as fast load current pulsations and large input voltage variations, can make the system unstable [3.31], [3.32]. Several methods [3.33]-[3.39], have been proposed to improve the robustness of the controller of the dc-dc converters against various disturbances. However, they were usually quite complicated to implement. As an alternative, it is well known that increasing the value of the output filter capacitor improves output voltage regulation. This method, however, not only increases the system cost and size, but also may degrade the dynamic response of the converter when sudden changes of the output voltage is desired. A virtual capacitance concept was introduced in [3.40] and [3.41] to improve the output voltage robustness of dc-dc converters that does not require increasing the size of the bulky filter capacitor.

The K-factor control, which integrates three different type of controllers [3.42]-[3.45], is well suited to address the aforementioned issues of the classical the PI controller. Various K-factor controllers have been designed to improve the performance of converters and other power electronic systems. However, it has not been applied to DAB converters yet. In this work, a novel K-factor controller is designed to improve the dynamic response and the transient performance of DAB converters, in particular, to track the reference dc output voltage with fast transient response

and significantly reduced the overshoot under various operating conditions compared to PI controllers. To further enhance the robustness of the K-factor controller against various disturbances, an additional control loop is proposed based on the virtual capacitance concept, which makes the DAB converter behave as if there is a large filter capacitor.

Comprehensive theoretical analysis, modeling, design and experimental verification of a DAB converter with the proposed virtual capacitor based K-factor (K+VC) controller are presented in this paper. The main objective of the study is to determine the most suitable controller to handle normal and transient operating conditions. The closed-loop performances of a DAB converter with classic PI, K-factor and K+VC controllers are evaluated. Both simulation studies using MATLAB/ Simulink$^{TM}$ and experimental studies on a 0.6-kVA, 200-V DAB converter prototype are performed to validate the feasibility and the effectiveness of the proposed methods. By using the proposed K+VC control scheme, short transient and zero steady-state errors can be achieved simultaneously.

As aforementioned, the classical SPS control in DAB is widely adopted due to it is simple and easy to apply. However, the efficiency performance of SPS need to be improved. Thus the multi-phase-shift control, such as EPS, DPS, and TPS are investigated by many scholars. These three controllers have different degrees of freedom. Compared to other phase-shift controllers, TPS has the best performance. But its design is most complicated. The DPS control has two degrees of freedom and its performance is very close to that of the TPS control in terms of the current stress and reactive power reductions [3.46][3.47]. In this work, a DAB power loss model is developed and an optimized controller is then proposed to integrate the DPS and K+VC controllers. Thus, the proposed control algorithm can improve the efficiency as well as the transient performance of

the DAB.

The section is structured as follows: First, the DAB topology with K-factor control and the virtual capacitor control concept is introduced. Then, the comparative analysis and simulations of transit response characterization of K-factor virtual capacitor control and PI control is presented. The efficiency optimization method based DPS is analyzed and the experimental results are presented. Finally, the conclusion is given about the proposed control.

### *3.10.2 Proposed K-Factor control with the virtual capacitor for a DAB*

#### *3.10.2.1 Operation principle of DPS control in DAB*

A single module, single-phase DAB converter consists of two H-bridges connected by a medium/high frequency transformer. The H-bridge converter on the primary side converts the dc voltage into a medium/high frequency ac voltage; the H-bridge converter on the secondary side converts the ac voltage back to the dc voltage. There are many ways of controlling the DAB converter. The SPS control is the most straightforward and widely adopted control method for the DAB. The phase-shift between the two active H-bridges is used to control the amount of power flow from one dc voltage source to the other. The control objective for the DAB converter in an SST is to regulate the output dc voltage by adjusting the phase-shift between the two active H-bridges. The topology of a typical DAB converter is depicted in Fig. 3-18. The transformer connects the two H-bridges in a DAB converter, and therefore, the DAB current and voltage waveforms can have a significant impact to the efficiency of the transformer.

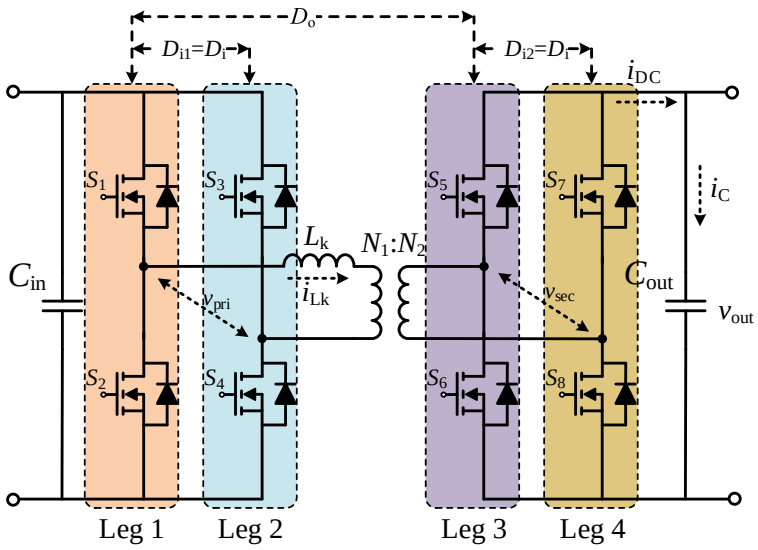



Fig. 3-18 DAB Converter with Phase-Shift Control

When using DPS control, there are two operating conditions of dual-phase-shift due to the desired power flow, i.e., $0 \le D_o < D_i \le 1$ and $0 \le D_i \le D_o \le 1$[3.46], where $D_i$ is the inner phase-shift ratio, $D_o$ is the outer phase-shift ratio. The same analysis method can be applied to the $D_o \le D_i$ and $D_i < D_o$ operating conditions. In this paper, $D_i \le D_o$ case is discussed as an example. There is phase-shift of gate driver signal between Leg 1 and Leg 3 and a different phase-shift angle between leg1 and leg 2, as illustrated in Fig. 3-18. The inductor current and voltage waveforms under DPS control is given in Fig. 3-19. It displays the transformer primary voltage $v_{pri}$, and the secondary voltage $v_{sec}$, and transformer input current $i_{Lk}$ waveforms for the single-phase DAB. The voltage across the inductance $L_k$ during the different bridge conduction periods determines the shape of current waveform. Due to the symmetry of transformer current and voltage waveforms, only the expressions for the first half switching cycle are given in (3-32) and (3-33).

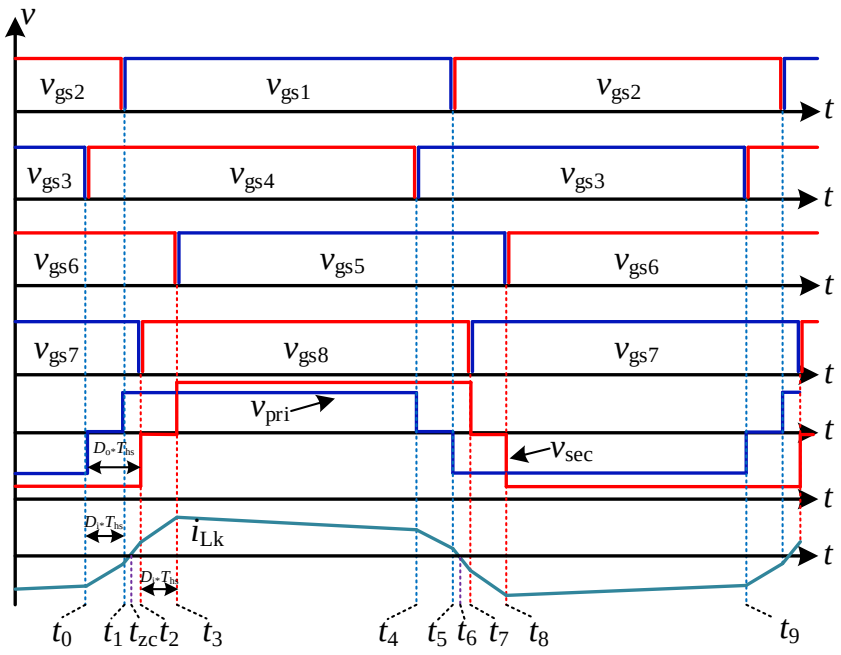



Fig. 3-19 Transformer Primary and Secondary Voltages, DAB Inductor Current with DPS Control

$$L\frac{di_L(t)}{dt}=\begin{cases}-v_{out}, t_0\le t<t_1\\ v_{in}-(-v_{out}), t_1\le t<t_2\\ v_{in}, t_2\le t<t_3\\ v_{in}-v_{out}, t_3\le t<t_4\end{cases} \tag{3-32}$$

$$C_{out}\frac{dv_{out}}{dt}=\begin{cases}-i_L(t)-\dfrac{v_{out}}{R}, t_0\le t<t_1\\ -i_L(t)-\dfrac{v_{out}}{R}, t_1\le t<t_2\\ -\dfrac{v_{out}}{R}, t_2\le t<t_3\\ i_L(t)-\dfrac{v_{out}}{R}, t_3\le t<t_4\end{cases} \tag{3-33}$$

where $t_0 = 0$, $t_1 = D_iT_s/2$, $t_2 = D_oT_s/2$, $t_3 = (D_i + D_o)T_s/2$, $t_4 = T_s/2$, $v_{in}$ and $v_{out}$ are the input and output dc voltage, respectively.

The output power of the DAB, $P_{DAB}$, is calculated as shown in (3-34). For any particular power

level, switching frequency, input and output voltages, the phase angle and leakage inductance of the transformer must be decided so as to achieve the required power transfer. Usually, the input voltage range, switching frequency and leakage inductance are fixed by system design. To regulate the output voltage, there are two different techniques can be used such as pulse-width or phase-shift modulation [3.46]. Considering the current stress and efficiency requirement, phase-shift modulation is considered in this paper. It is assumed that the input voltage of the DAB has already been regulated as a constant value by the front end rectifier, and the output voltage is regulated as a fixed value by the DAB controller.

$$P_{DAB} = \frac{\int_{t_0}^{t_4} v_{pri} i_{Lk}(t) dt}{T_s/2} = -\frac{(D_i^2 + 2(-1 + D_o)D_o) n T_s v_{in} v_{out}}{4L} \tag{3-34}$$

where,

$n$: turns ratio of the transformer

$T_s$: Switching period

$L$: The primary-referred leakage inductance

*3.10.2.2 Modeling of the DAB*

For conventional control techniques for dc-dc converters, it is of interest to determine the effects of variations in the input voltage, the load current, and the duty cycle upon the output voltage. Unfortunately, understanding the converter dynamic behaviour is difficult due to the non-linear time-varying nature of the switching and phase difference through the PWM process, and the conventional averaging technique for dc-dc converters, requiring negligible current ripple are not applicable to DAB design as the transformer primary and secondary currents are purely ac

quantities. Using time averaging and small signal analysis can overcome these issues. A well-known converter modelling technique [3.42] is briefly described in this section. From this average model, a linear time-invariant small-signal model can be derived by means of linearization around a well-defined operating point.

*3.10.2.2.1 Averaging model for DAB*

Considering the symmetry of current waveform in the DAB transformer over one switching period, the inductor current is given by:

$$i_L(t_4) = i_L(t_0) \tag{3-35}$$

Combining (3-32) and (3-35), the inductor current at time $t_0$, $t_1$, $t_2$, $t_3$, and $t_4$ are calculated as shown below:

$$\begin{cases} i_L(t_0) = i_L(t_4) = \dfrac{T_s(-v_{in} + D_i v_{in} + n v_{out} D_i D_o - n v_{out} D_i^2 D_o - 2 n v_{out} D_i D_o^2)}{4L} \\ i_L(t_1) = \dfrac{T_s(-v_{in} + D_i v_{in} + n v_{out} D_i D_o + n v_{out} D_i^2 D_o - 2 n v_{out} D_i D_o^2)}{4L} \\ i_L(t_2) = \dfrac{T_s(v_{in} + D_i v_{in} + 2 D_o v_{in} - n v_{out} D_i D_o + n v_{out} D_i^2 D_o)}{4L} \\ i_L(t_3) = \dfrac{T_s(-v_{in} + D_i v_{in} + 2 D_o v_{in} + n v_{out} D_i D_o - n v_{out} D_i^2 D_o)}{4L} \end{cases} \tag{3-36}$$

Due to symmetry of the waveform, the average value of the inductive current $i_L$ in a switching period is zero at steady state, thus the normal average modelling method for a switching cycle cannot be used directly. In this dissertation, the inductor current is derived first, which is given in (3-37). Then, (3-36) and (3-37) are used to eliminate the inductor current $i_L$ in Eq. (3-33). After that, the order of the voltage average model is reduced. The voltage expression in (3-33) is rewritten as given in (3-38).

$$i_L(t)=\begin{cases} -\dfrac{v_{out}}{L}t+i_L(t_0), t_0\le t<t_1 \\ \dfrac{v_{in}+v_{out}}{L}t+i_L(t_1), t_1\le t<t_2 \\ \dfrac{v_{in}}{L}t+i_L(t_2), t_2\le t<t_3 \\ \dfrac{v_{in}+v_{out}}{L}t+i_L(t_3), t_3\le t<t_4 \end{cases} \tag{3-37}$$

$$C_{out}\frac{dv_{out}}{dt}=\begin{cases} -\dfrac{v_{out}}{R}t+i_L(t_0)-\dfrac{v_{out}}{R}, t_0\le t<t_1 \\ -\left(\dfrac{v_{in}+v_{out}}{R}t+i_L(t_1)\right)-\dfrac{v_{out}}{R}, t_1\le t<t_2 \\ -\dfrac{v_{out}}{R}, t_2\le t<t_3 \\ \left(\dfrac{v_{in}-v_{out}}{R}t+i_L(t_3)\right)-\dfrac{v_{out}}{R}, t_3\le t<t_4 \end{cases} \tag{3-38}$$

According to the average definition of the switching period of the variable, the mean value of the switching period of the output voltage $v_{out}$ is derived in (3-39).

$$C_{out}\frac{d\langle v_{out}\rangle_{Ts/2}}{dt}=\frac{\int_{t_0}^{t_4}C_{out}\dfrac{d\langle v_{out}\rangle}{dt}dt}{T_s/2}= \\ -\frac{\left(\begin{array}{l}-4L\langle v_{out}\rangle-RT_s\langle v_{out}\rangle+nRT_s\langle v_{out}\rangle D_iD_o+2D_iD_oRT_s\left(-3\langle v_{in}\rangle+\langle v_{out}\rangle-2n\langle v_{out}\rangle D_iD_o\right)+ \\ 2D_oRT_s\left(2\langle v_{in}\rangle-n\langle v_{out}\rangle D_iD_o\right)+2D_o^2RT_s\left(-2\langle v_{in}\rangle+n\langle v_{out}\rangle D_iD_o\right)+D_i^2T_s\left(\langle v_{in}\rangle+\langle v_{out}\rangle+n\langle v_{out}\rangle D_iD_o\right)\end{array}\right)}{4RL} \tag{3-39}$$

*3.10.2.2.2 Small-signal model of DAB with DPS control*

Eq. (3-39) gives a relation between the output voltage, input voltage, inner phase-shift, outer phase-shift, and inductor current which is a time invariant nonlinear equation. Therefore, a small-signal model to calculate the system transfer function is always desirable for closed-loop controller design and stability analysis of power electronic converters.

According to (3-39), a small perturbation can cause a deviation from its steady-state value. Lowercase letters are used to represent large-signal variables, the small-signal states and the steady-state quantities are represented by Δ and uppercase letters, respectively. The definitions of the state variables are:

$$\langle v_{out} \rangle = V_{out} + \Delta v_{out} \tag{3-40}$$

$$\langle v_{in} \rangle = V_{in} + \Delta v_{in} \tag{3-41}$$

$$\langle D_i \rangle = D_i + \Delta D_i \tag{3-42}$$

$$\langle D_o \rangle = D_o + \Delta D_o \tag{3-43}$$

Because the multiplication of control input and state variables are contained in (3-39), with a small perturbation, the nonlinear term can be approximated using (3-40) to (3-43). The small-signal model of the DAB converter could be achieved in (3-44) by substituting (3-40) to (3-43) into Eq. (3-39), which is a transfer function given by:

$$G_{vDo} = \frac{\Delta v_{out}}{\Delta D_o} = -\frac{2RT_s\left(\left(-2+3PD_i+4PD_o\right)v_{in} - PD_i v_{out} + nv_{out}D_iD_o + 2nPv_{out}D_i^2D_o - 2nPv_{out}D_iD_o^2\right)}{4L(1+C_{out}Rs)+(1-PD_i^2-2P^2D_iD_o)RT_s} \tag{3-44}$$

*3.10.2.3 K-factor with virtual capacitor control*

To design the closed-loop control of the DAB, the PID control is widely adopted because it can eliminate steady-state errors and is simple to design. However, the DAB converter is a non-minimum phase system and the PID controller couldn't guarantee the fast dynamical and low overshoot requirements. In this paper, the K-factor approach is developed to ensure control stability and meet the required specifications. It has three different types of transfer functions. The type of transfer function is decided by the required phase and magnitude margins. To further improve the transient performance of output voltage in DAB, a virtual capacitor concept will be

developed in this section.

*3.10.2.3.1 K factor theory*

To design the control algorithm for the DAB, the voltage tracking error, which is the difference between the reference output voltage and the sensed output voltage, is utilized. Then, a controller is designed to amplify the error signal to the desired phase-shift in the DAB. Thus, the performance of a controller is the key to regulate the expected output in DAB. Depending on the required amplitude and phase margins, there are three typical types of amplifiers [3.43]:

(1) Type I:

The transfer function of Type I K-factor controller is given by (3-45). The Bode plot is shown in Fig. 3-20. The gain is rolled off at -20 dB/dec due to the signal pole at origin.

$$G_{KI}(s) = \frac{k_c}{s} \tag{3-45}$$

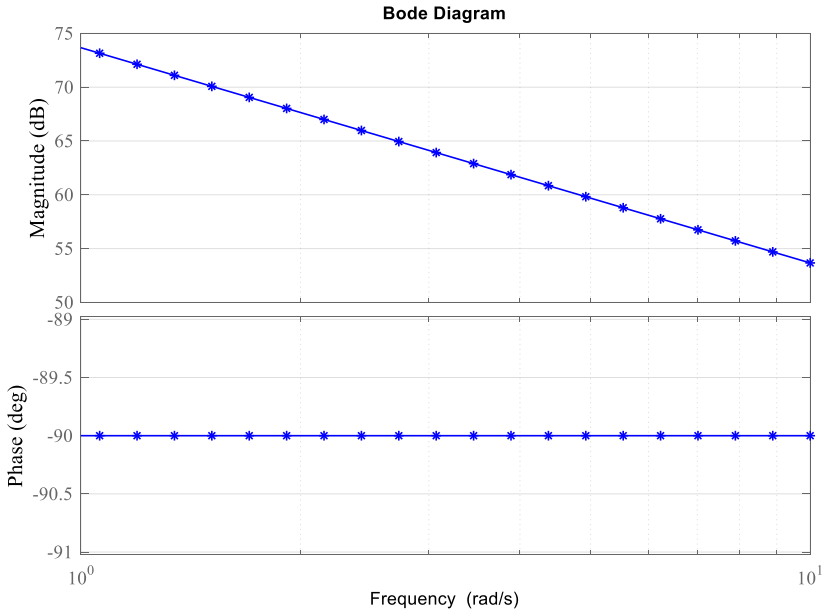



Fig. 3-20 Bode plot of Type I K-factor controller

(2) Type II:

The transfer function of Type II K-factor controller is given as (3-46). The Bode plot is shown in Fig. 3-21. Different from Type I, it has one more pole at frequency $\omega_p$ and one zero at frequency $\omega_z$. Thus, the Type II can boost phase angle up to 90 degrees.

$$G_{KII}(s) = \frac{k_c \omega_p}{\omega_z}\left(\frac{\omega_z + s}{s(\omega_p + s)}\right) \tag{3-46}$$

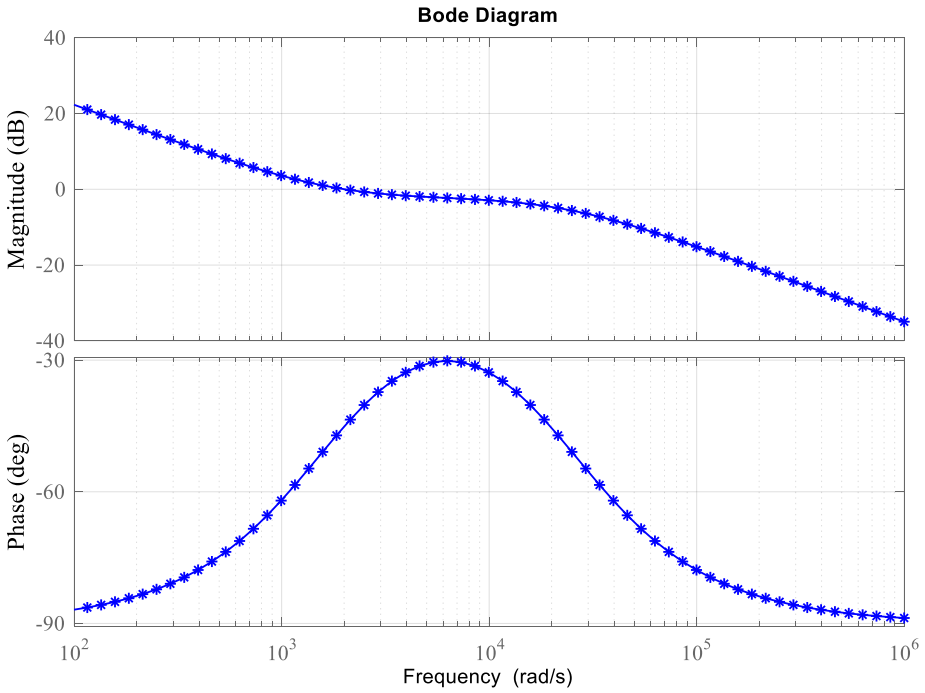



Fig. 3-21 Bode Plot of K-factor Type II Control

(3) Type III:

The transfer function of Type III K-factor controller is given by (3-47). The Bode plot is shown in Fig. 3-22. Different with Type II, it has one zero, two poles at frequency $\omega_p$ and two zeros at frequency $\omega_z$. Thus, the Type III can boost phase angle more than 90 degrees.

$$G_{KIII}(s) = \frac{k_c \omega_p^2}{\omega_z^2}\frac{(\omega_p + s)^2}{s(\omega_p + s)^2} \tag{3-47}$$

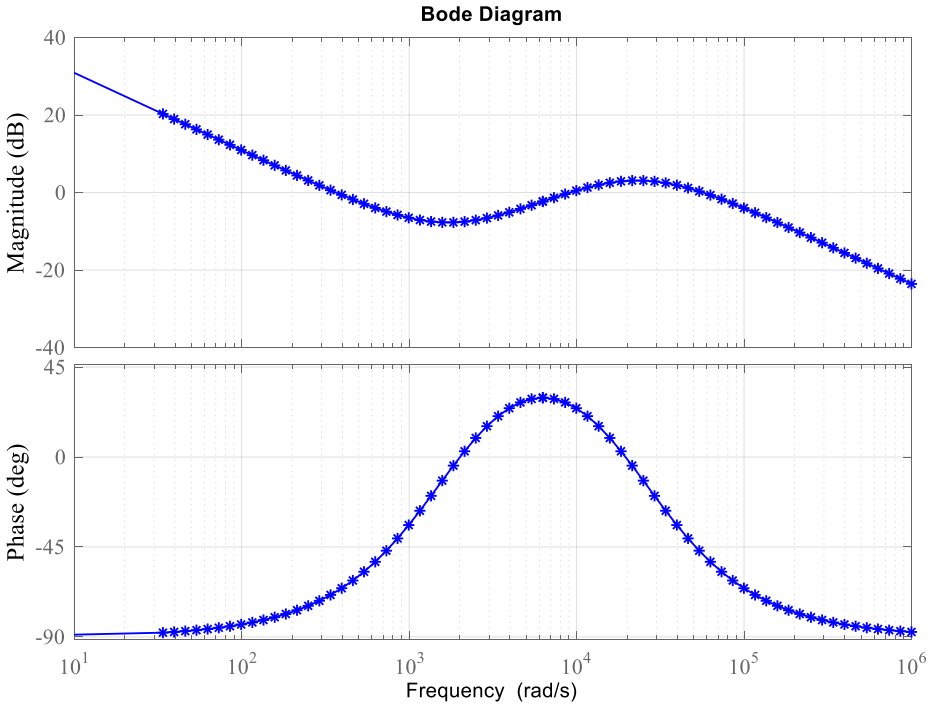



Fig. 3-22 Bode Plot of K-factor Type III Control

(4) The factor K calculation

From the transfer functions as shown in (3-45), (3-46), and (3-47), the desired K-factor can be derived as shown in (3-48), (3-49), and (3-50). K-factor for Type I is given by:

$$k_c = 1 \tag{3-48}$$

For Type II amplifier:

$$k_c = \tan\left[\frac{Phaseboost}{2} + 45^\circ\right] \tag{3-49}$$

For Type III amplifier:

$$k_c = \left[\tan\left(\frac{Phaseboost}{2} + 45^\circ\right)\right]^2 \tag{3-50}$$

where, *Phaseboost* is the required phase boost in the controller:

$$Phaseboost = P_d - P_c - 90^\circ \tag{3-51}$$

where $P_d$ is the desired phase margins, $P_c$ is the phase-shift of system at the crossover frequency, The frequency at the pole and zero can be calculated as given in (3-52) and (3-53), respectively.

$$\omega_p = k_c \omega_c \tag{3-52}$$

$$\omega_z = \frac{\omega_c}{k_c} \tag{3-53}$$

where, $\omega_c$ is the crossover frequency of the system.

*3.10.2.3.2 Virtual capacitor control*

The output dc-link voltage stability improvement depends on the following design requirements: minimum voltage deviation and its response time for a given load power disturbance. To reduce the equivalent series resistance (ESR) of the dc-bus capacitor, there are several capacitors in parallel forming the dc bus. Although the paralleled capacitors can reduce the dc-bus voltage ripple and supply the transient power, the shortcomings are increased cost and size. The proposed stabilization approach is to improve the system stability by virtually increasing the dc-link capacitance. To enhance the stability or the transient response, a virtual capacitor C_v was introduced in Fig. 3-23. A virtual capacitor is used to replace the actual capacitor. The function of virtual capacitor is realized in the controller design. It also allows adjusting the system damping ratio and so, controlling the system response during the transient mode with the proposed K-factor control. The main advantage of the virtual capacitor is the capacitance can be easily adjusted based on the system response requirement. Also, these are no cost and voltage limitations for the virtual capacitor

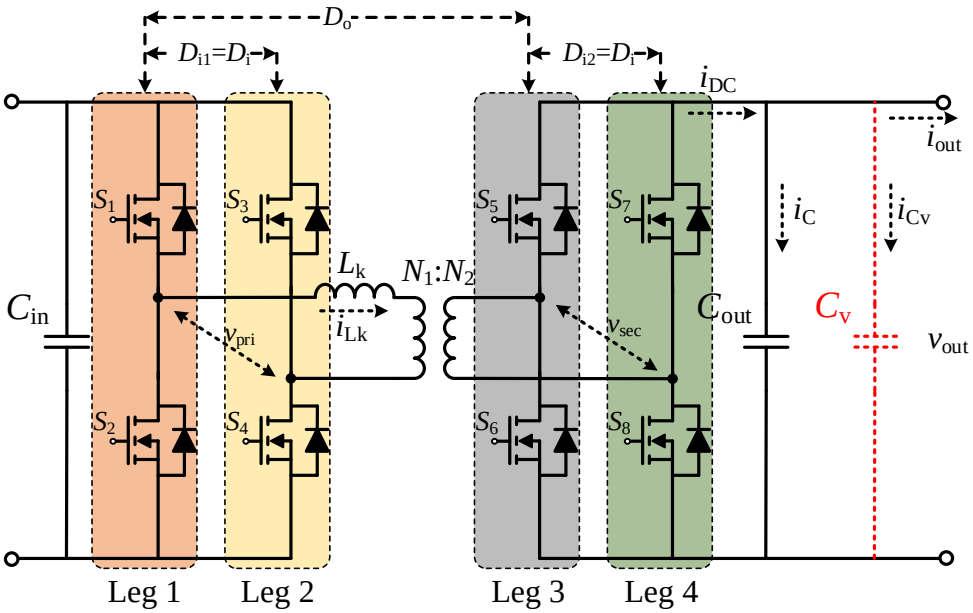



Fig. 3-23 DAB System with Virtual Capacitor

The small signal model of DAB with virtual capacitor by using (3-44) could be derived as shown in (3-54).

$$G_{vDo}=\frac{\Delta v_{out}}{\Delta D_o}=-\frac{2RT_s\left(\left(-2+3PD_i+4PD_o\right)v_{in}-PD_iv_{out}+nv_{out}D_iD_o+2nPv_{out}D_i^2D_o-2nPv_{out}D_iD_o^2\right)}{4L(1+C_{out}Rs+C_vRs)+(1-PD_i^2-2P^2D_iD_o)RT_s} \tag{3-54}$$

Therefore, the closed-loop transfer function of K-factor virtual capacitor control can be written as follows, with Type I, II, and III factor controllers, separately.

$$G_{KFI+C}=G_{vDo}G_{KI}=\frac{k_c2RT_s\left(\left(2-3PD_i-4PD_o\right)v_{in}+PD_iv_{out}-nv_{out}D_iD_o-2nPv_{out}D_iD_o\left(D_i-D_o\right)\right)}{(C_{out}R+C_vR)s^2+(4L+1-PD_i^2-2P^2D_iD_o)RT_ss} \tag{3-55}$$

$$G_{KFII+C}=G_{vDo}G_{KII}=-\frac{k_c}{\omega_z}\frac{2RT_s\left(\left(-2+3PD_i+4PD_o\right)v_{in}-PD_iv_{out}+nv_{out}D_iD_o-2nPv_{out}D_iD_o\left(D_i-D_o\right)\right)}{A_{II}s^3+B_{II}s^2+C_{II}s} \tag{3-56}$$

$$G_{KFIII+C}=G_{vDo}G_{KIII}=\frac{2RT_sk_c\omega_p\left(\left(2-3PD_i-4PD_o\right)v_{in}+PD_iv_{out}-nv_{out}D_iD_o-2nPv_{out}D_iD_o\left(D_i-D_o\right)\right)\left(\omega_z+s\right)}{\omega_z^2\left(A_{III}s^4+B_{III}s^3+C_{III}s^2+D_{III}s\right)} \tag{3-57}$$

where, $A_{II}=(C_{out}R+C_vR)$, $B_{II}=\left(\omega_p(C_{out}R+C_vR)+(4L+1-PD_i^2-2P^2D_iD_o)RT_s\right)$,

$C_{II}=\omega_p(4L+1-PD_i^2-2P^2D_iD_o)RT$ ,

$A_{III}=(C_{out}R+C_vR)$, $B_{III}=\left(2\omega_p(C_{out}R+C_vR)+(4L+1-PD_i^2-2P^2D_iD_o)RT_s\right)$,

$C_{III}=\omega_p\left(\omega_p(C_{out}R+C_vR)+2(4L+1-PD_i^2-2P^2D_iD_o)RT_s\right)$,

$DIII=\omega_p^2(4L+1-PD_i^2-2P^2D_iD_o)RT$ .

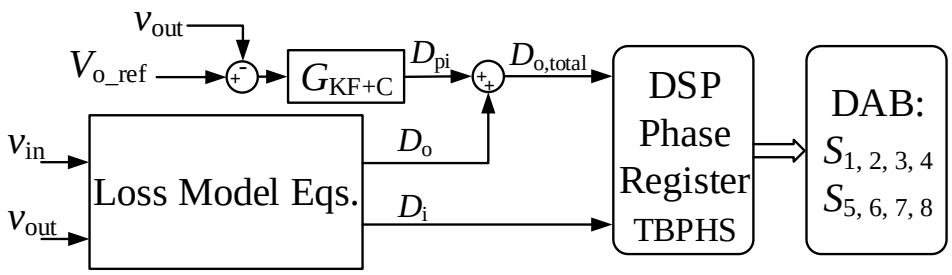



Fig. 3-24 Control Diagram of Power Loss Minimization

The control scheme of the DAB is given in Fig. 3-24. The reference value of inner phase-shift $D_i$ and outer phase-shift $D_o$ is calculated by Eq. (3-30). In order to maintain the output bus voltage during input voltage or load power transient, a K+VC control is utilized to modify the outer phase-shift $D_o$. The calculated $D_o$ as feed forward phase-shift and plus with the output of K+VC controller to improve the transient performance. In the steady state, the output $D_{o,total}$ should be equal to $D_o$ to realize the goal of the smallest power loss.

### *3.10.3 Comparative analysis of transit response characterization*

#### *3.10.3.1 System parameters*

The circuit parameters for simulation are given in Table 3.4.

Table 3.4 Parameters for Simulation

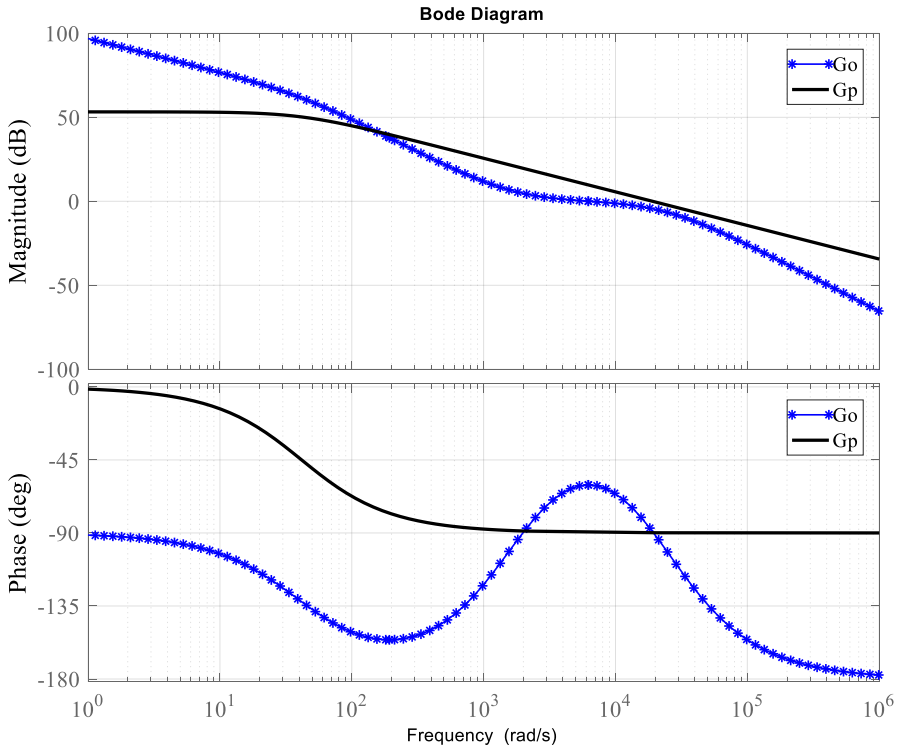
| Variables | Value | Variables | Value |
|---|---|---|---|
| Rated Power | 1 kVA | $C_{out}$, Cv | 50 μF, 800 μF |
| $C_{in}$ | 180 μF | $f_s$ | 50 kHz |
| Input DC voltage | 200 V | $L_k$ | 150 μH |

*3.10.3.2 K-factor control –system stability*

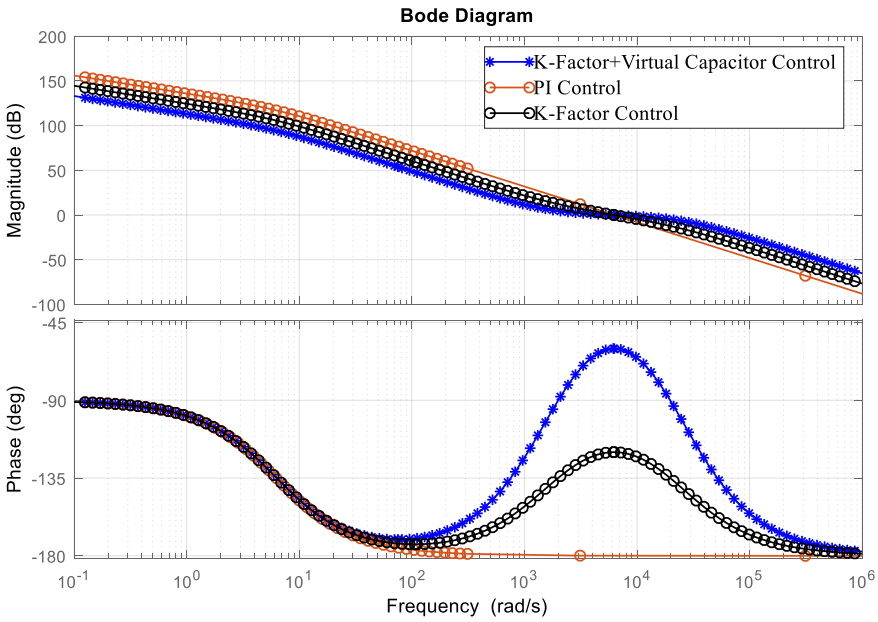
The closed-loop SPS control system needs a high controller bandwidth which is desirable to maximize performance. Controller bandwidth is defined as the frequency at which the forward path transfer function has unity gain ($\omega_c$). The transient performance achieved by the controller (in terms of rise time, settling time, overshoot, etc.) is governed by the available phase margin (PM) at this crossover frequency. In general, large phase margins give less oscillatory response but slower rise times, while smaller phase margins give faster rise times at the cost of a more oscillatory response. The controller design process therefore aims to maximize controller bandwidth while still achieving a phase margin that provides good performance.

By using PI control alone, the PI controller gives the forward path a pole at the origin, this will further subtract another 90° phase and would go below -180° if no phase boost is applied. Therefore, proper design of the K-factor controller and K+VC controller can provide the desired phase boost to get the targeted phase margin at the crossover frequency. And its Bode plot represents its characteristics below in Fig. 3-25. The comparison of Bode plots of DAB $G_p(s)$ and closed-loop transfer function $G_o(s)$, which includes the K-factor controller transfer function $G_c(s)$, along with $G_p(s)$, are shown in Fig. 3-25 (a). The closed-loop transfer function $G_o(s)$ has a phase margin (PM) of 60° at $\omega_c$ = 31416 rad/s. The gain margin (GM) is 0 dB at 31416 rad/s. From the values of PM and GM, the closed-loop system is stable. As shown in Fig. 3-25 (b), the K-factor

virtual capacitor controller generates a maximum phase margin (120°) and highest gain crossover frequency (31416 rad/s) in the frequency domain analysis. A large phase margin leads to a stable closed-loop system. Increasing the phase margin to obtaining real poles, with small overshoot and ringing.




(a) The open-loop (Black solid) and closed-loop (Blue star) K+VC

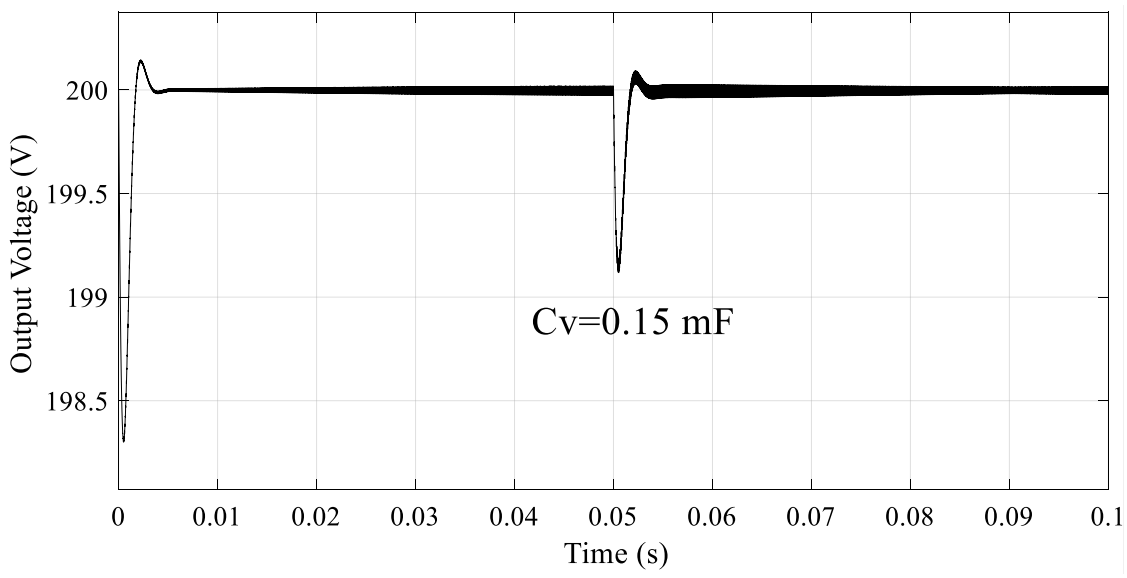



(b) The bode-plot of three closed-loop controllers

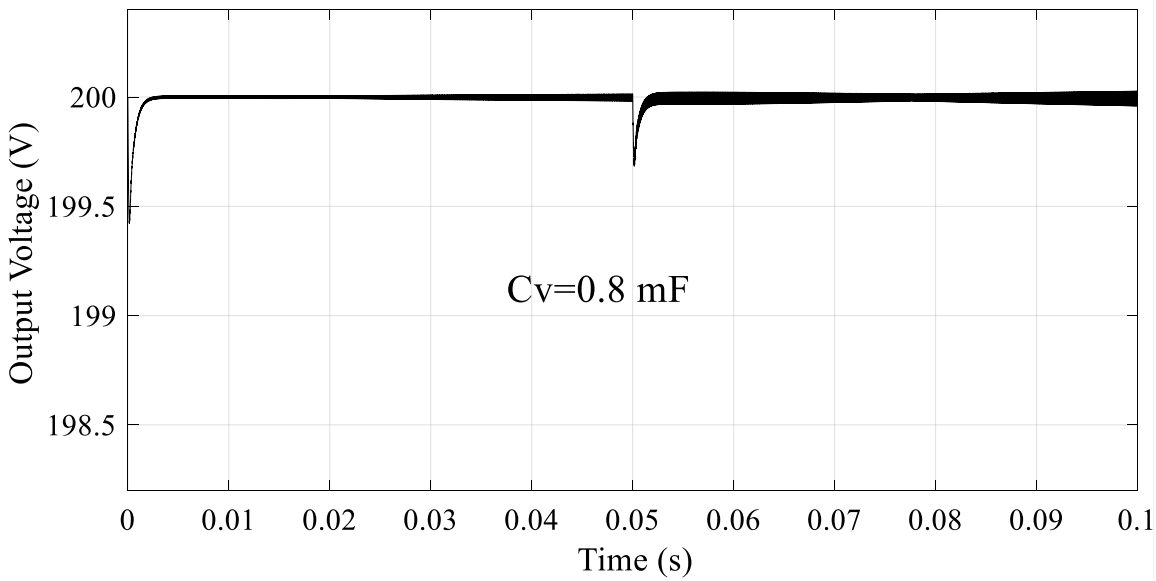
Fig. 3-25 Bode plot of DAB with Different Controllers

### *3.10.3.3 Transient response of K+VC control*

As discussed in the previous section, although the transient performance can be achieved by the K-factor controller with enough phase margin (PM) at the crossover frequency, industrial standards often impose quality requirements on current and voltage waveforms, and particularly on their overshoot and settling time during a transition. The system-damping ratio should be adjusted to satisfy these requirements. Nevertheless, a high damping ratio requires high resistor and capacitor values and this is in contradiction with other requirements on weight and volume in transportation systems. As the proposed method in this paper permits to change virtually the dc-link capacitance, it can be used to obtain a satisfactory damping ratio for the system. Fig. 3-26 shows that small voltage sag and settling time could be achieved by adjusting $C_v$. From this point of view, the virtual capacitor $C_v$ can be considered as the design parameter allowing adjusting the damping factor of the system.




(a) $C_V$=0.15 mF



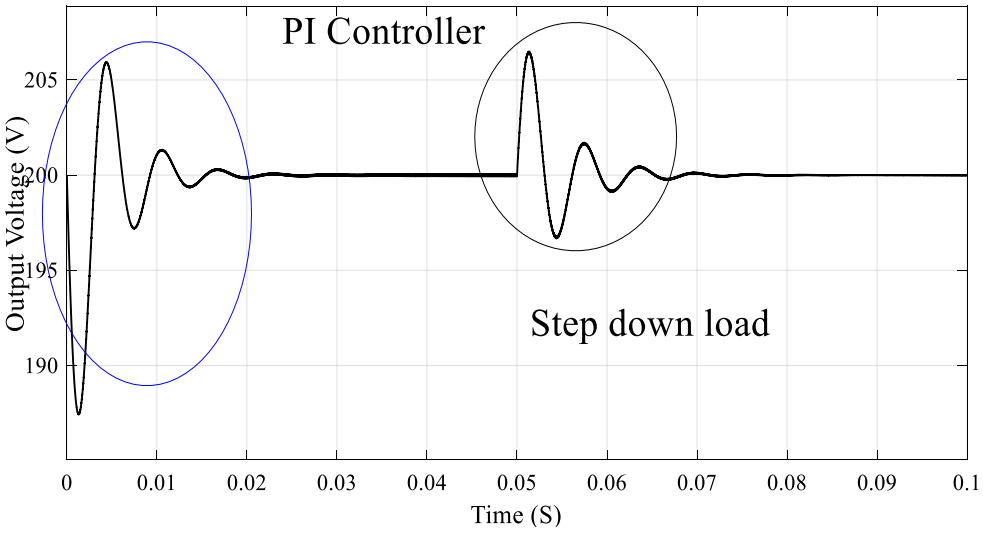

(b) $C_V$=0.8 mF

Fig. 3-26 Step-up Load, Output Voltage Transit with Virtual Capacitor

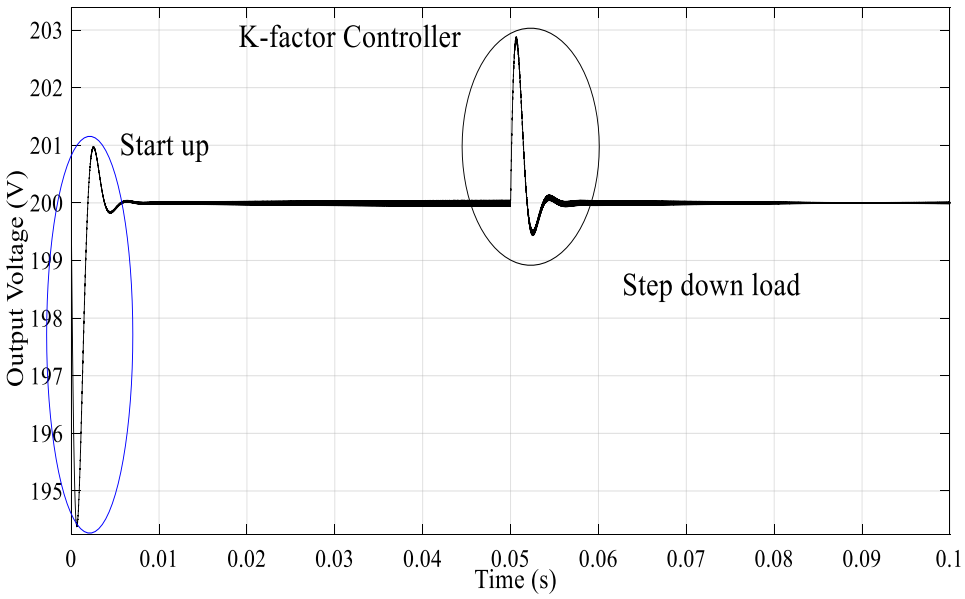
*3.10.3.4 Simulation results and discussion*

Simulations based on the parameters presented in Table 3.4 have been carried out to compare the performance of PI control, K-factor control and K-factor plus virtual capacitor control. The

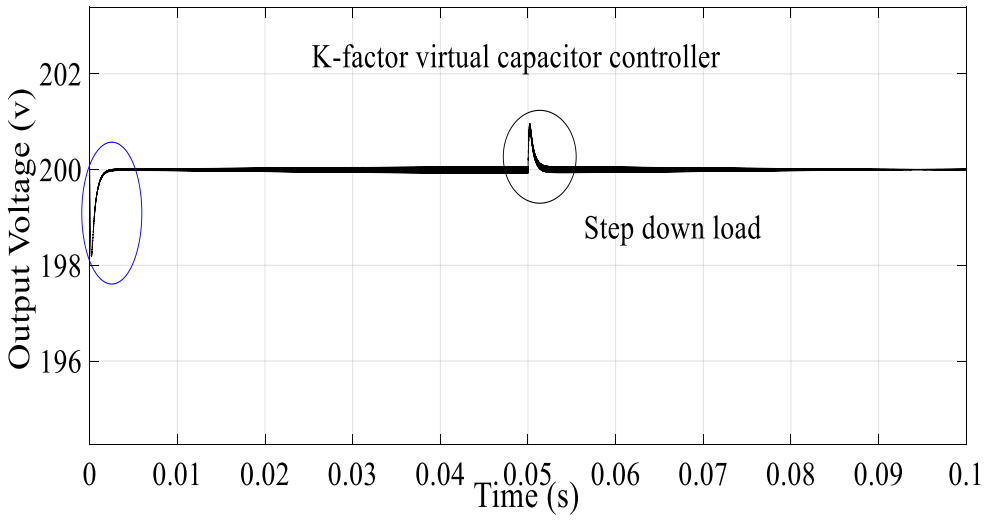
closed-loop performance of the converter becomes satisfactory. The dynamic performances in terms of step and frequency responses of the DAB converter with the three controllers have been reported in Fig. 3-27 and Fig. 3-28. It is clear that the K-factor plus virtual capacitor controller provides the best dynamic response than the other controllers. The time response with K-factor plus virtual capacitor controllers shows very fast response with very small overshoot and zero steady-state error.



(a) PI Controller

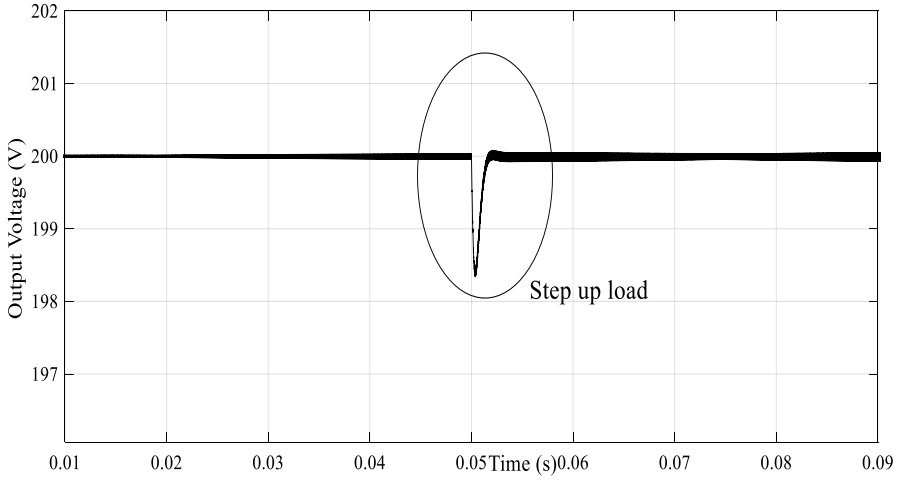


(b) K-factor Controller

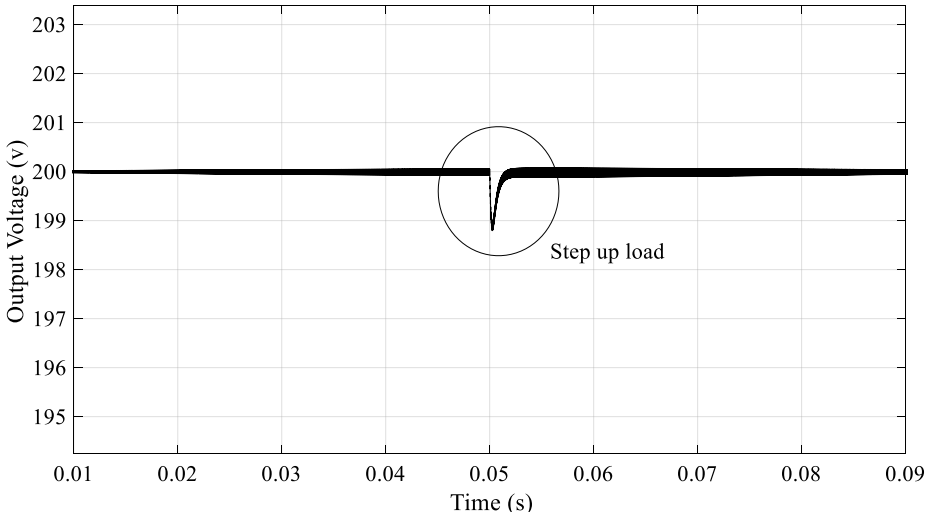



(c) K+VC

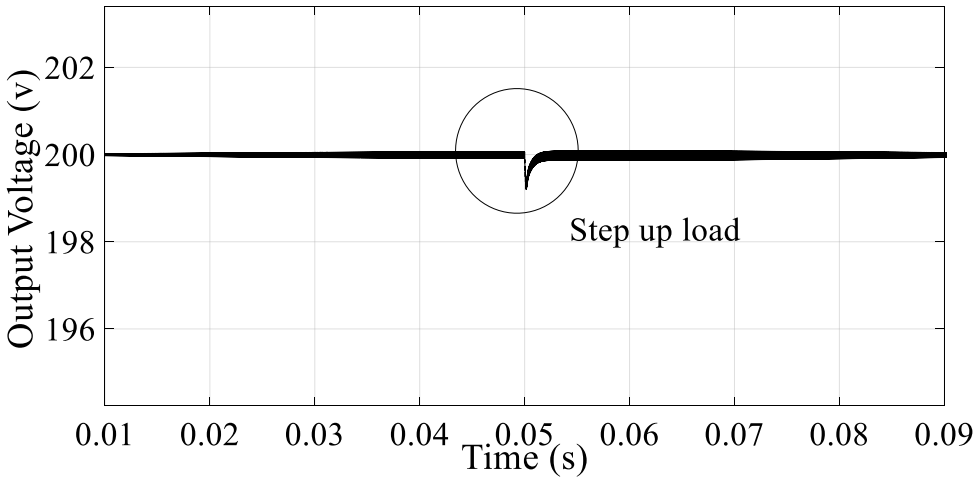
Fig. 3-27 Step-down Loads Response for Three Controllers




(a) PI Controller




(b) K-factor Controller




(c) K+VC

Fig. 3-28 Step-up Loads Response for Three Controllers

It is to be mentioned here that the K-factor approach is a standard method for design of different type controllers and in the present case it worked well for the closed-loop boost converter. However, keeping in view the demand for very fast response of power supplies, the controller performance are further improved by adding the virtual capacitor in parallel with dc-link capacitors. From the simulation results, it is clear that the performance of the virtual capacitor based K-factor controller is better than the PI and single K-factor controllers for the proposed DAB converter.

### *3.10.4 Hardware experimental validation of the proposed control*

In order to further verify the preceding analysis and test the validity of the proposed controller, a 0.2 kV 0.6 kW DAB prototype has been designed and built. The current/voltage controller is implemented in a TMS320F28335 DSP. Wolfspeed SiC MOSFET C2M0080120D are the semiconductor switches of choice. The oscilloscope is a Techtronix TPS2024, which is used to reduce the noise/offset of the current sensor, and the high-precision current probe PEM CWT6 is the current sensor. Tektronix THDP0200 probes are chosen as the high voltage probes and the YOKOGAWA WT1600 power meter is used for the efficiency measurement and analysis. The prototype main parameters are same as Table 3.4. A picture of the overall scaled-down laboratory prototype is depicted in Fig. 3-29.

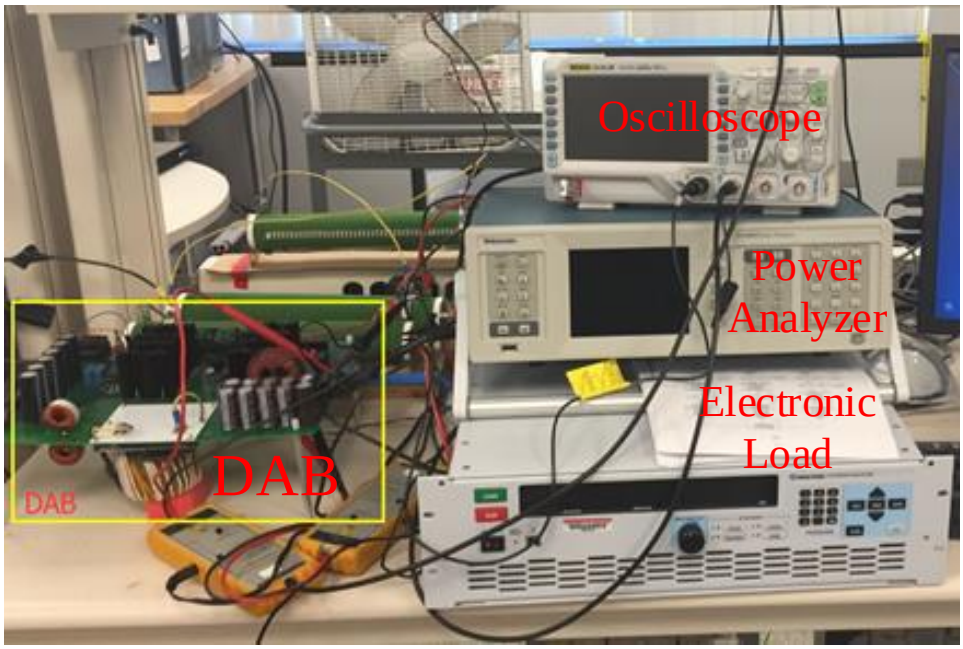



Fig. 3-29 The Scaled-down Prototype of DAB

To verify the developed small signal based average model of DAB, the output power comparison between the experimental results and the simulation results from the model is shown

in Fig. 3-30. The circuit parameters are same as Table 3.4. Due to loss in the DAB converter is not considered in the model, the simulation results from the average model is slightly higher than the experimental results. However, with different power references, the simulation results of small-signal model based average model fits with the experimental result very well.

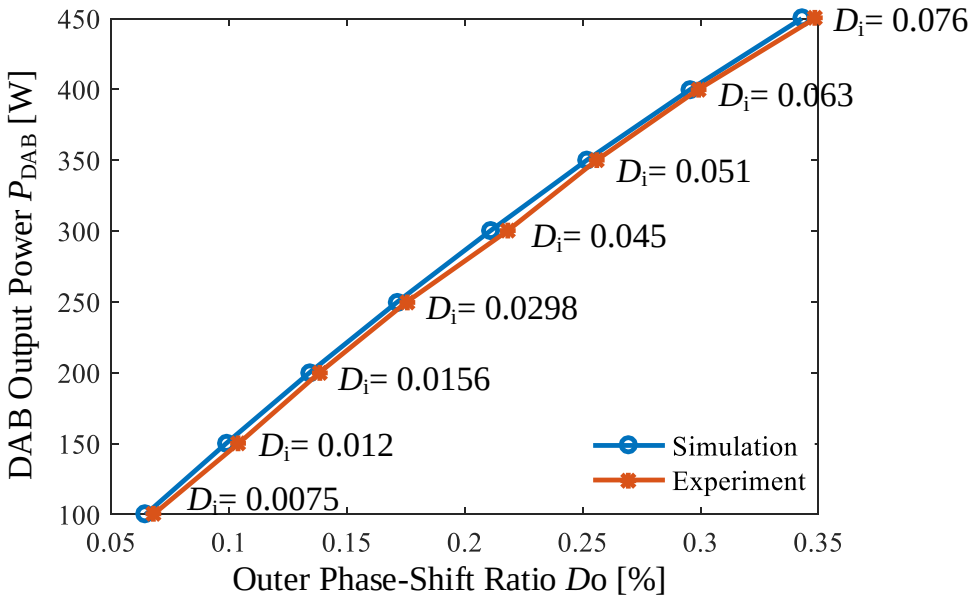
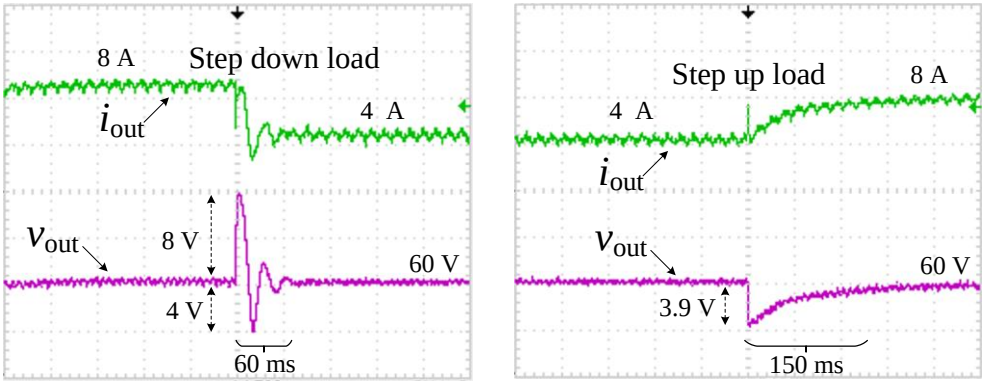


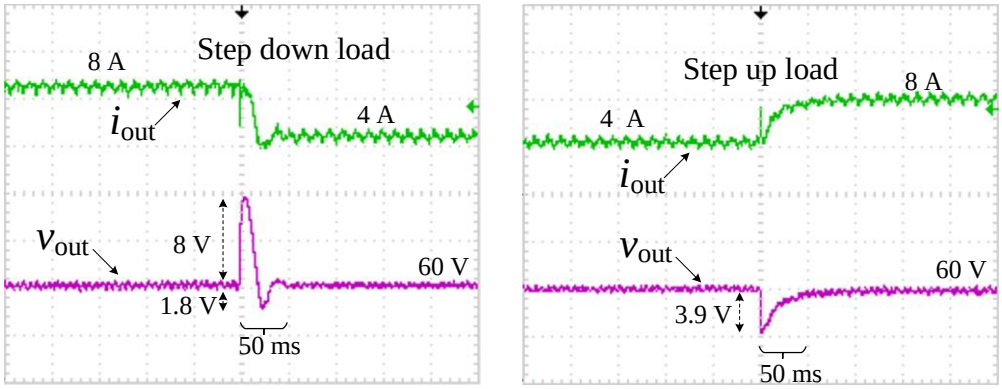

Fig. 3-30 Comparison betweed the output power in closed-loop avergae model and experimental results

Fig. 3-31 shows the dynamic responses of the output voltage and load current in step-down and step-up load modes. Three controllers are applied to the DAB converter: (a) classical PI controller, (b) Single K-factor controller and (c) K+VC. In the step-down load mode, the voltage overshoot is reduced from 8 V to 6.4 V with the virtual capacitor based K-factor controller. The settling time is reduced from 60 ms to 32 ms. In the step-up load mode, the volatge sag is reduced some but the settling time is reduced from 150 ms to 15 ms. It validates that proposed virtual-capacitor based K-factor controller exhibits the fastest response with little overshoot; the worst result in terms of sluggishness and overshoot is noted in the case of the PI classical controller. As expected, there is significant overshoot in the output voltage response due to step changes in the

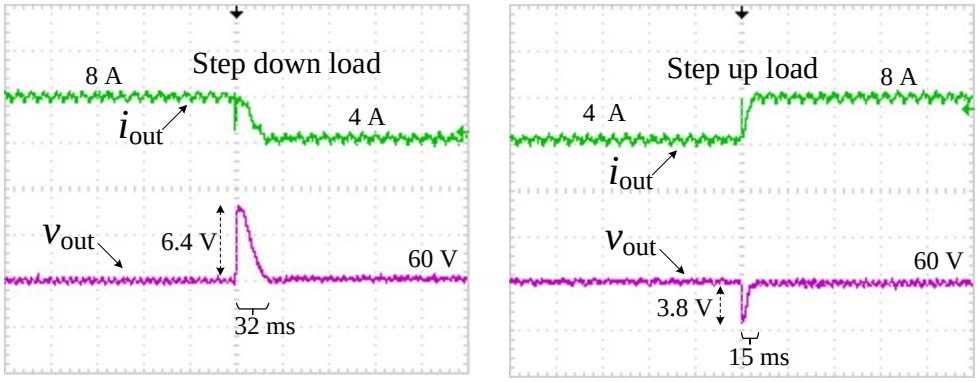
load in the case of single K-factor and PI controllers.




(a) PI Control




(b) Single K-factor Control




(c) Virtual Capacitor Based K-factor Control

Fig. 3-31 Transient Reponse with Step Load Results With PI, K-factor, and K+VC

### *3.10.5 Conclusion of virtual capacitor based K-factor control*

A new approach to improve the robustness of the output voltage of the DAB against various disturbances has been presented, associated theory analyzed and validated by simulations and experimental results. The proposed approach was the K+VC controller based on the K-factor method and a new parallel virtual capacitance concept for enhancing stability and performance. The virtual capacitance can be designed as large as possible without requiring any space and cost. The virtual capacitance can be designed to respond selectively against certain signals. It could be concluded that the K-factor virtual capacitor controller exhibits the best closed-loop performance, highest system bandwidth and largest margin of stability.

## 3.11 Other Testing Results

The hardware of the system has been built as shown in Fig. 3-32, which is based on the aforementioned ac/dc and dc/dc stages design. The cascaded totem-pole converter and dual-active bridge converter are marked in the figure. The control algorithm is programmed in the TI DSP. The power supply for the control card, sensing circuit, gate driver and relay are generated from the input ac voltage. The SiC MOSFET is Wolfspeed C2M0080120D.

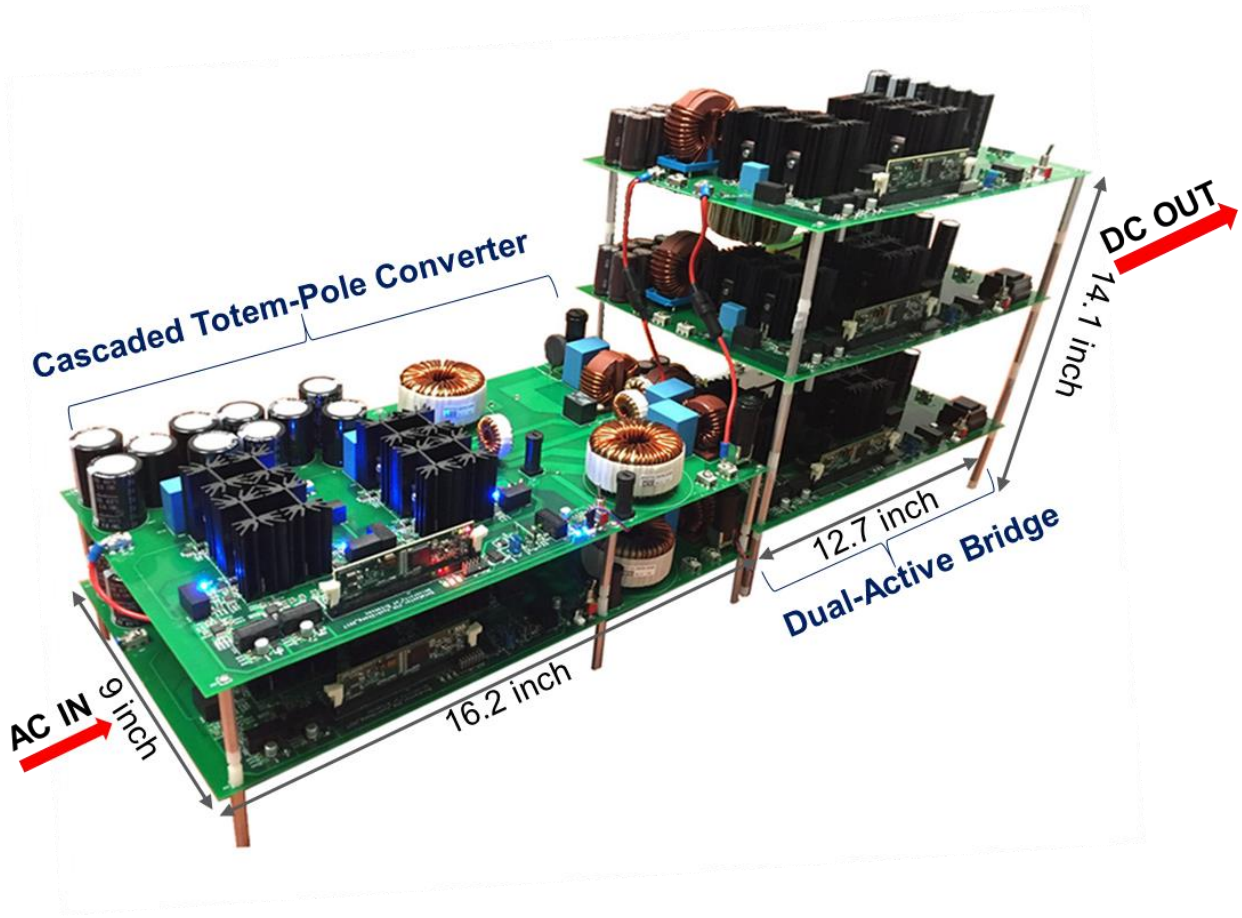



Fig. 3-32 The Scaled Down Prototype of Overall System

The circuit parameters are summarized in Table 3.5.

Table 3.5 Circuit Parameters for the Scaled Down Prototype

| Grid voltage | Grid voltage frequency | Switching frequency of cascaded totem-pole converter | Switching frequency of dual-active bridge | PFC output voltage reference |
|---|---|---|---|---|
| 240 VAC | 60 Hz | 50 kHz | 50 kHz | 200 |
| PFC inductor | Input capacitor | Output capacitor | Switch dead time | DC output voltage reference |
| 5 mH | 470 uF | 470 uF | 200 ns | 50 |

The testing results of grid voltage and current from the cascaded totem-pole converter are shown in Fig. 3-33. The THD of grid voltage is 1.2%, and the current THD is 3.8%. The power factor is 0.98. All the testing results show the efficacy of the proposed model predictive control.

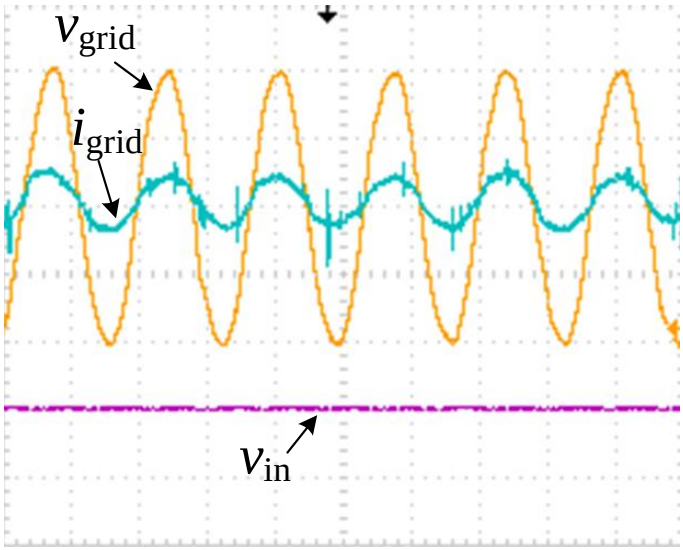



Fig. 3-33 Yellow: Grid voltage $v_{grid}$= 240 VAC, Blue: Grid current $i_{grid}$= 2.1 A, Purple: DAB primary side dc voltage $v_{in}$=200 VDC

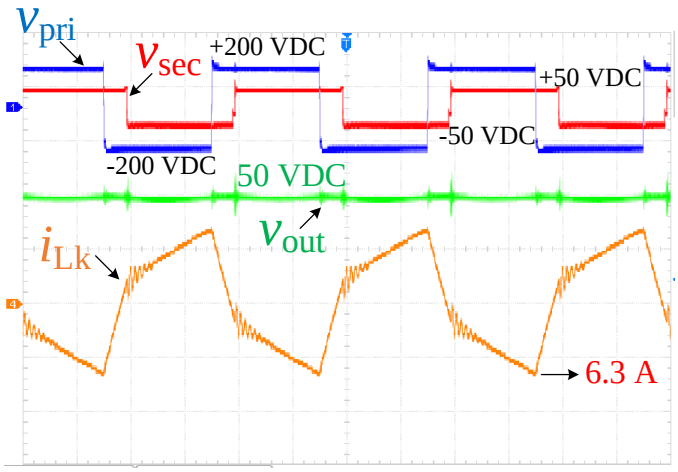



Fig. 3-34 Testing results of DAB with SPS control

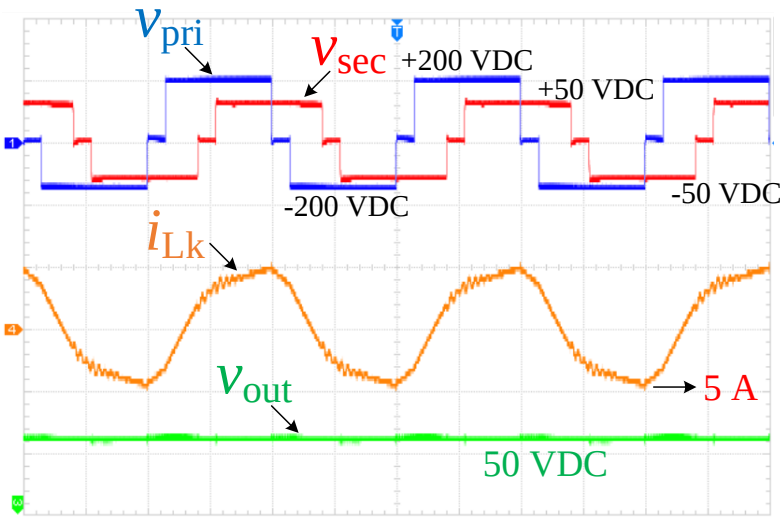



Fig. 3-35 Testing results of DAB with Loss Model Based-DPS control

The dc/dc stage with the dual-active bridge and the testing results are shown in Fig. 3-34 and Fig. 3-35. $v_{pri}$ is the primary side voltage of transformer, $v_{sec}$ is the primary side voltage of transformer, $i_{Lk}$ is the leakage inductor current, $v_{out}$ is the secondary side dc voltage of the DAB. The peak current of the leakage inductor with using the SPS control is 6.5 A. As shown in Fig. 3-35, the dual-phase-shift control is applied in the DAB stage to reduce the current stress to 5 A for the switches. Therefore, the power loss can be reduced as well.

In this chapter, the MPC control strategy is designed to improve the transient performance and realize multi-goal control. The loss model based DPS control is designed to improve the efficiency performance of DAB, then the virtual capacitor based K-factor is developed to achieve better transient performance for the DAB with step up/down loads. The scaled down prototype is designed and built. The simulation and experimental results are given to verify the proposed topology and aforementioned control algorithms.

## 3.12 Reference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# CHAPTER 4

# DISTRIBUTED ENERGY INTEGRATION AND HYBRID ENERGY MANAGEMENT STRATEGY FOR 400 V DATA CENTER

## 4.1 Introduction and Motivation

Integrating renewable energy sources like solar power into the distribution system of a data center is of interest to reduce electric energy cost and carbon emissions [4.1][4.2]. Compared with ac distribution, the efficiency of dc distribution could be higher leading to significant cost reduction of the required cooling system. Furthermore, with increasing the power distribution voltage to 400 V dc, the conduction loss can be reduced and the less costly cables can be utilized. Last but not least, the main merit of the dc distribution architecture is that it promotes integration with distributed energy sources such as photovoltaics (PV), wind turbines, fuel cells, and etc. The tradeoff is that the current commercial technologies for dc equipment have higher costs than comparable ac equipment.

Energy storage units such as batteries play an important role in UPS systems. They supply uninterrupted power to the important loads. Power transients, due to solar irradiance transients or load changes, need to be smoothed by energy storage. Lead-acid battery packs are widely used in data centers due to their low costs. However, batteries should not be rapidly charged or discharged to avoid reducing their life expectancy. To overcome this drawback, ultracapacitor packs are considered in this work to compensate the high-frequency power transients in order to improve the

battery lifetime. The integration of solar power and energy storage units into the distribution system of a 400 V DC-powered data center was evaluated in the following sections.

## 4.2 Description of Green Data Center

In this chapter, integrating the PV power, a battery pack, and an ultracapacitor pack into a 400 V DC-powered data center is evaluated. Due to solar irradiance transients or load changes, the power transients are smoothed by proper control of the battery and ultracapacitor packs with the former providing compensation of medium-frequency power transients and the latter compensating for high-frequency power transients. This strategy should extend the life expectancy of the battery pack. Four typical weather conditions and related controllers are investigated; namely, cloudy, rainy, overcast, and clear days.

Fig. 4-1 illustrates the evaluated configuration with renewable energy generation and energy storage systems. There are two voltage buses in the system. One is the kV ac bus (i.e., the ac utility feeder) and the other one is the 400 V dc bus. Grid and (remote) renewable energy through a transmission system connect to the kV ac bus. Since diesel engines may have a high failure rate, the diesel generator and grid supply are connected through two separate paths of cabling to enhance the supply reliability. A high-power centralized active-frond-end (AFE) rectifier is utilized at the grid side to feed the 400 V dc bus. The PV power is interfaced to the 400 V dc bus through a boost converter that is equipped with a maximum power point tracking (MPPT) algorithm. The battery and ultracapacitor packs are interfaced using the buck/boost converters connected to the same 400 V dc bus. The critical fans, lighting and room air conditioners are powered by an inverter. The existing 48 V telecom power supply is recognized as a more economical and practical option. To minimize the revision of the existing power supply in the data center, the 48 V dc bus is kept in the rack. The battery as back-up energy is on the 48 V dc bus as well [4.3]-[4.6].

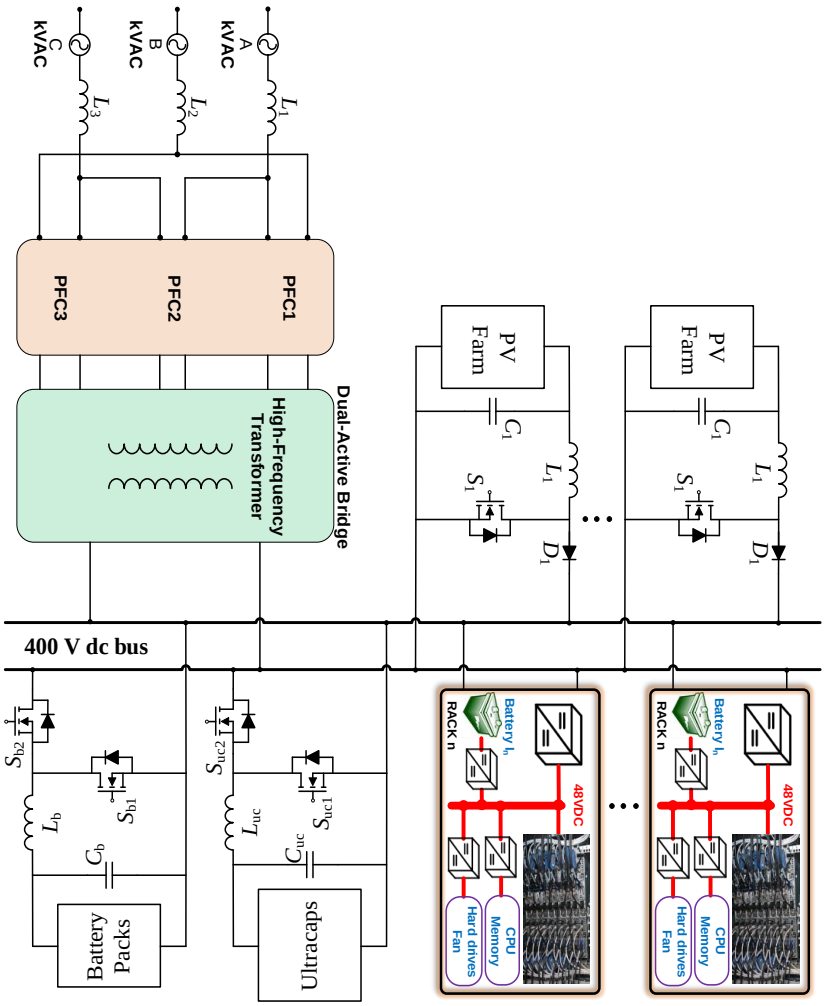



Fig. 4-1 Generic Configuration of A 400 V DC-Powered Data Center Integrated With Solar Power and Energy Storage Units

In this chapter, the general system configuration of a 400 V DC-powered green data center is described firstly. Secondly, the control strategies of the PV, ultracapacitor packs and grid-side converters are presented. Thirdly, the simulation results of the designed controllers are illustrated, and conclusions are given in the last section.

## 4.3 PV Topology and MPPT Control

Maximum power point tracking systems are widely used to maximize output power of photovoltaic arrays. A crucial issue of these systems is an algorithm of maximum power point

seeking. The well-known perturb and observe technique is an optimal solution in terms of the ratio of cost and efficiency. However, this algorithm has some disadvantages such as oscillation around a maximum power point and a decrease in efficiency occurring under low levels of solar irradiance. In this section, an improved MPPT method has been used. It is based on combination of the perturb-observe variable duty cycle step-size algorithm and constant voltage algorithm. According to this technique, a simple constant voltage method is implemented in case of low levels of solar irradiation, otherwise the system operates under the variable duty cycle step-size perturb and observe algorithm. The simulation results shown here prove the superior performance of variable duty cycle step-size of P&O over constant duty cycle step-size P&O.

The block diagram for the PV farm is shown in Fig. 4-2. The module 1Soltech 1STH-215-P is selected for each PV array that has 40 parallel strings with 10 series-connected modules per string. The dc/dc converter is chosen as a boost converter to realize the maximum power point tracking (MPPT) control. The MPPT control algorithm for the PV is improved by using constant voltage tracking (CVT) to track the maximum power-point of photovoltaic output. Then, it is transferred to a variable duty cycle step-size perturbation and observation (P&O) method to quickly track the maximum power. This method can quickly and accurately track the maximum power.

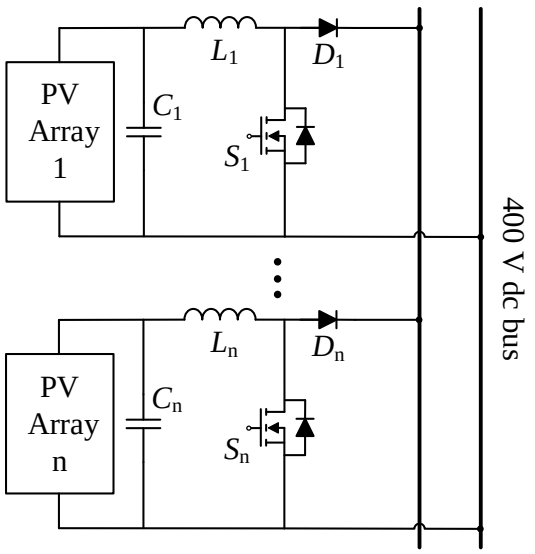



Fig. 4-2 Circuit Diagram of the Considered PV Farm

Fig. 4-3 illustrates the circuit block diagram for PV farm. MPPT of the PV array is regulated by controlling the duty cycle of switches. Two traditional and popular MPPT control algorithms are the CVT and P&O methods. The CVT method is easy to process, but if the temperature changes rapidly this method cannot track the maximum power point very well. Another method, P&O, is widely used in engineering applications since it simplifies control structure and requires fewer parameter measurements [4.7]. The disadvantage of this strategy is that oscillations easily occur when the system reaches its maximum power point due to a constant duty cycle step-size. This dissertation combines these two MPPT control algorithms to realize a more suitable MPPT performance. The detailed MPPT control diagram is displayed in Fig. 4-3. First, the CVT method controls the PV to produce a stable power output, with voltage reference ($U_{\text{ref}}$) set at $0.85U_{\text{oc}}$. The duty cycle step of switch in CVT control is $\Delta D$. Then, the controller switches to the P&O method, the output voltage and current of PV panels are sensed. In order to improve the accuracy and reduce the power loss, the variable duty cycle $\Delta D_1$ and $\Delta D_2$ is adopted.

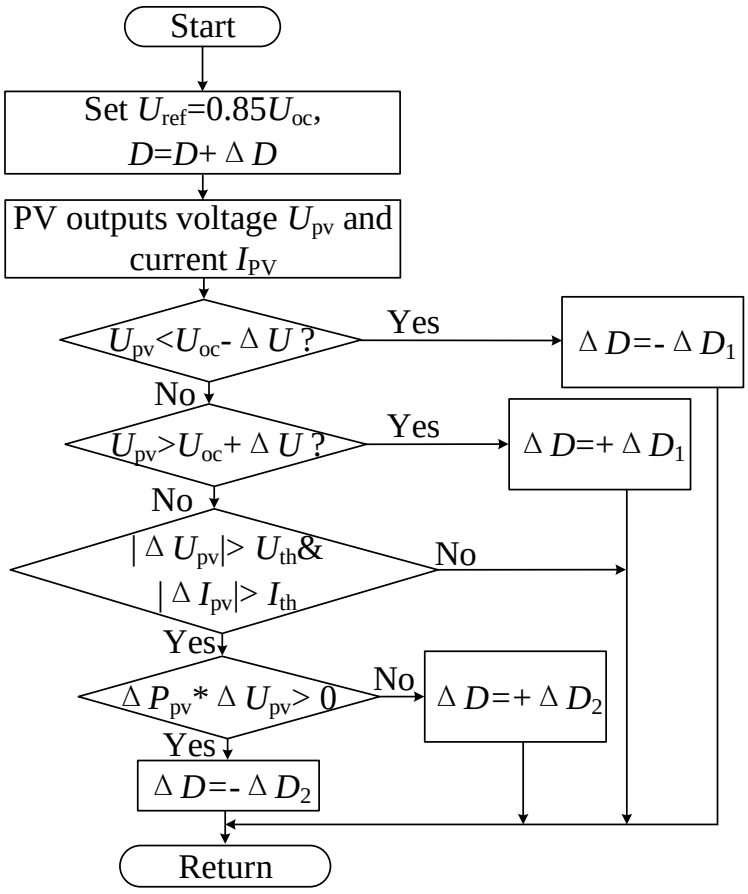


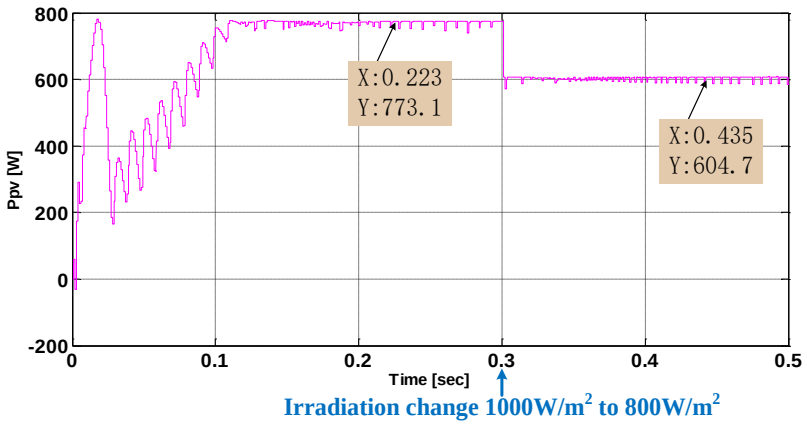

Fig. 4-3 Flowchart for the Calculation of the Duty Cycle of the Boost Converter

Generally, a large perturbation requires a longer settling time after the perturbation is triggered in a PV system with the MPPT control. A small perturbation requires a shorter settling time. Considering a 10% steady-state error, a perturbation period higher than the settling time of the system was chosen. The system transient response occurs with high step-sizes in the duty cycle thus increases the amplitude of the steady-state oscillation. The step-size needs to be calculated based on the energy utilization efficiency optimization, the optimum step-size is the one at which the algorithm will not be confused when solar irradiance changes. The controller algorithm adapts the MPPT perturbation period to the duty cycle perturbation step-size. The MPPT perturbation period is smaller when the duty cycle perturbation step-size is smaller and vice versa.

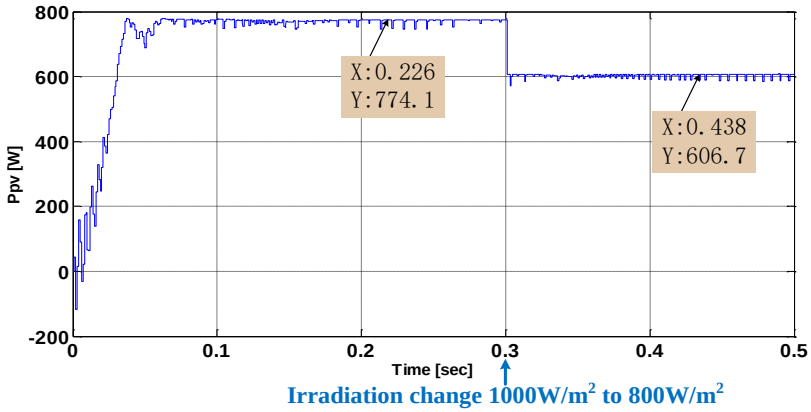
The simulation parameters of the PV panels are given in Table 4.1. Fig. 4-4 shows the comparison of both the constant duty cycle step-size P&O and the variable duty cycle step-size P&O with CVT control. From Fig. 4-4 (b), notice that when using the variable duty cycle step-size, P&O has a much more stable power tracking capability; there is also little oscillation at the beginning.

Table 4.1 The PV Panels Simulation Parameters

| | | | |
|---|---|---|---|
| Module | 1STH-215-P | Maximum power (W) | 213.15 |
| Open circuit voltage (V) | 36.3 | Voltage at maximum power point Vmp (V) | 29 |
| Current at maximum power point Imp (V) | 7.35 | Temperature coefficient of Voc (%/deg.C) | -0.36099 |
| Cells per module (Ncell) | 60 | Short circuit current Isc (A) | 7.84 |
| Temperature coefficient of Isc (%/deg.C) | 0.102 | Light-generated current IL (A) | 7.865 |
| Diode saturation current Io (A) | $2.9259\times10^{-10}$ | Diode ideality factor | 0.98117 |
| Shunt resistance Rsh (Ω) | 313.4 | Series resistance Rs (Ω) | 0.394 |




(a) Constant Duty Cycle Step-Size P&O




(b) Variable Duty Cycle Step-Size of P&O

Fig. 4-4 PV Simulation Results with Constant and Variable Duty Cycle Step-Size P&O MPPT Methods

## 4.4 PV Power Spectrum Analysis

To aid in the design of the system controller, a typical set of PV data was collected over a period of 24 hours from a PV farm, then imported into the FFT simulation block in MATLAB/Simulink™, and an FFT analysis was performed to identify the different frequency ranges of the PV power data. The PV power spectrum analysis results are shown in Fig. 4-5. The high-frequency power should be absorbed by the ultracapacitor pack. The power rate of the ultracapacitor pack is designed based on the peak value of the PV farm power and load profile. The medium-frequency power transients

are only absorbed by the battery pack to optimize its lifetime. Then, the power from ac grid side can be very smooth, and thus, representing low-voltage disturbances for the 400 V dc bus.

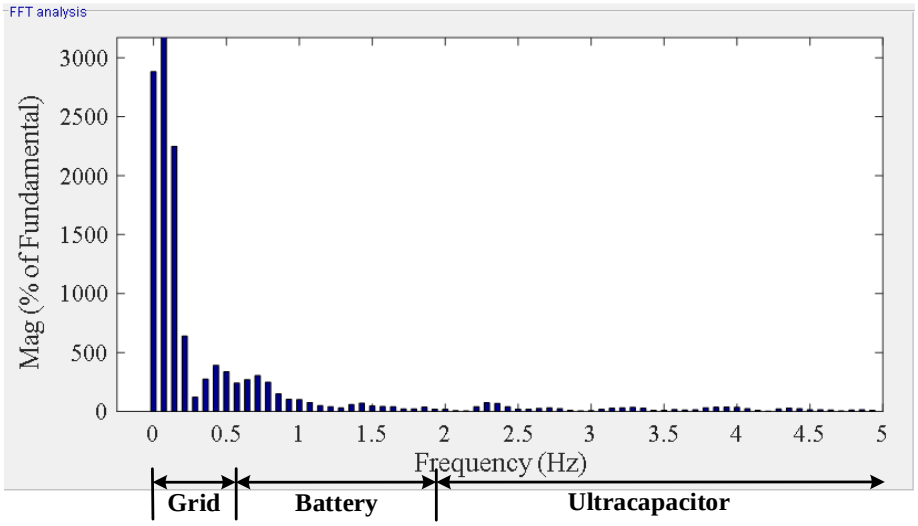



Fig. 4-5 Frequency Spectrum Analysis of PV Power Over A 24-Hour Period

## 4.5 Hybrid Energy Storage

High quality and reliable power is the standard for data centers. Energy storage devices such as batteries, flywheel energy storage, air compressor or fuel cells are used to smooth the power output from the sources. In a DC-powered data centers, due to the energy storage device batteries have relatively lower cost and high energy density, batteries are widely used for voltage regulation and bulk energy storage [4.8]-[4.10]. However, batteries have limited lifetime and shouldn't be deeply charged or discharged. Recently, ultracapacitor technology attracts much attention due to its much higher power density and fast response capability [4.11]-[4.13]. It also can be deeply charged and discharged without harming its lifetime. The disadvantage of ultracapacitor is the low energy density. Considering the tradeoff between power density and energy density, a hybrid energy storage becomes an optimal solution. In this section, both batteries and ultracapacitors are

utilized to maintain the dc bus voltage and provide the reliable and high quality power to data center.

### *4.5.1 Controller design of the buck/boost converter for the battery and ultracapacitor packs*

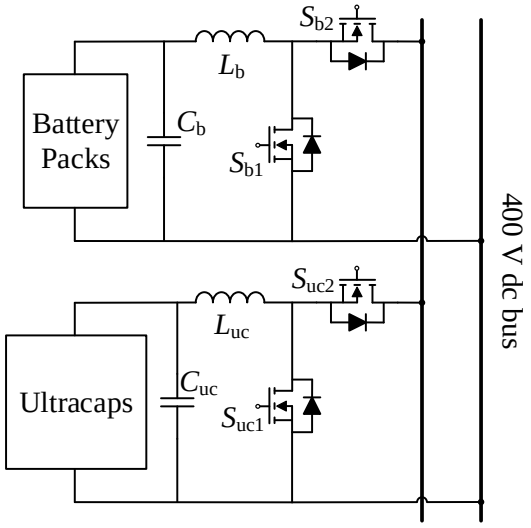



Fig. 4-6 Circuit Diagram of the Energy Storage Packs

As shown in Fig. 4-6, the battery and ultracapacitor packs are connected through bidirectional dc/dc converters feeding a common 400 V dc bus.

The control block diagram of the battery and ultracapacitor packs are illustrated in Fig. 4-7 and Fig. 4-8, respectively. There are two control loops for the bidirectional dc/dc converter. The outer loop is a power loop whose objective is to track the reference power. The inner loop performs current control and a limitation should be included to prevent any overcurrent in the battery or ultracapacitor packs.

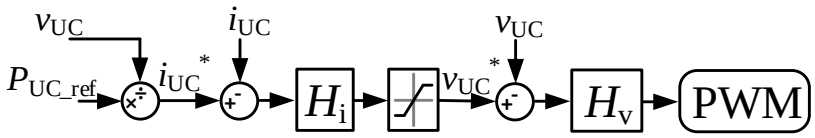



Fig. 4-7 Control Diagram of the Battery Pack

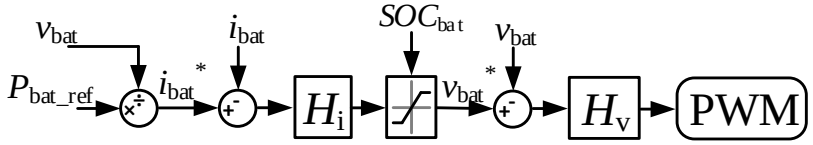



Fig. 4-8 Control Diagram of the Ultracapacitor Pack

### *4.5.2 Power reference calculation*

The power relationship of solar power, grid, battery, ultracapacitor and data center load are shwon below:

$$P_{load} = P_{PV} + P_{Battery} + P_{Ultracaps} + P_{Grid}\text{, without ultracapacitor pack} \quad (4\text{-}1)$$

$$P_{load} = P_{PV} + P_{Battery} + P_{Grid}\text{, with ultracapacitor pack} \quad (4\text{-}2)$$

The power reference is designed as shown in

Fig. 4-9. The power references for battery and ultracapacitor packs are given by Eqs. (4-3) and (4-4), respectively. The battery pack compensates for the power transients in the frequency range from $f_{c1}$ to $f_{c2}$ ($f_{c1} < f_{c2}$). Similarly, the ultracapacitor pack compensates for transients whose frequencies are higher than $f_{c2}$. Lastly, the grid supplies power at frequencies smaller than $f_{c1}$.

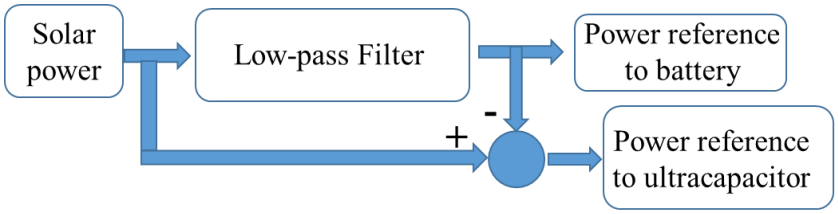



Fig. 4-9 Power Reference Generation for Battery and Ultracapacitor

$$P_{Bat\_ref} = \frac{\tau_{f_{c1}} s}{\tau_{f_{c2}} \tau_{f_{c1}} s^2 + \left(\tau_{f_{c2}} + \tau_{f_{c1}}\right) s + 1} P_{PV} \tag{4-3}$$

$$P_{UC\_ref} = \frac{\tau_{f_{c2}} \tau_{f_{c1}} s^2}{\tau_{f_{c2}} \tau_{f_{c1}} s^2 + \left(\tau_{f_{c2}} + \tau_{f_{c1}}\right) s + 1} P_{PV} \tag{4-4}$$

$$\tau_{f_{cn}} = \frac{1}{2\pi f_{cn}}, n = 1,2 \tag{4-5}$$

where $\tau_{fcn}$ is the time constant at the cutoff frequency $f_{cn}$ which is defined in Fig. 4-5 and determined by the frequency spectrum of the PV power.

## 4.6 Grid-Side Converter Design

The grid-connected converter operates as a voltage source converter to regulate the 400 V dc bus. The topology can be a conventional three-phase rectifier (AFE) or a multilevel converter [4.14]-[4.16]. The aforementioned multilevel solid-state transformer converter structure is utilized in this paper. Its block diagram is given in Fig. 4-10. Each PFC topology is connected in series in order to reduce the voltage stresses. A dual-active bridge is feeding a common 400 V dc bus to increase the current carry capability. A high-frequency transformer is used to reduce the system size.

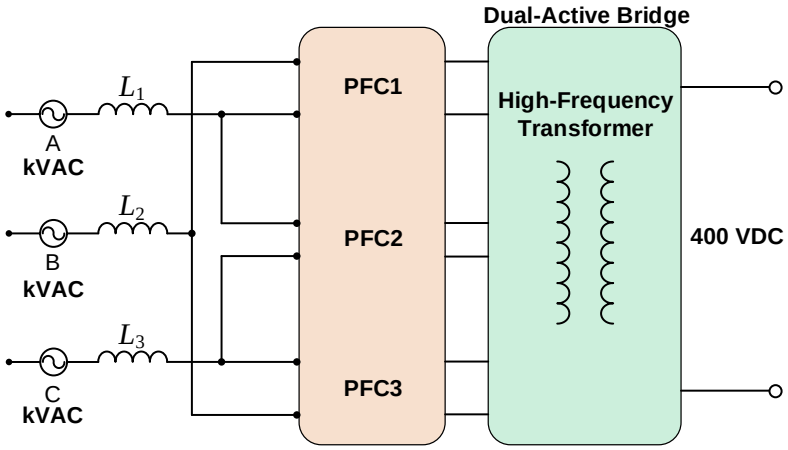



Fig. 4-10 Block Diagram of the Grid-Side Converter

The control algorithm for the grid side converter is shown in Fig. 4-11. It applies the conventional phase-shift PWM control. The outer loop is a dc bus voltage feedback control. The dc bus voltage is measured as feedback and compared with the reference voltage $U_{\text{bus\_ref}}$. The controller $H_{\text{v}}$ is a typical PI control. The output of $H_{\text{v}}$ is as the reference current to the inner loop which is the current loop to achieve the fast response capability. The feedback signals are the $i_{\text{d}}$ and $i_{\text{q}}$ which are transferred from the currents $i_{\text{a}}$, $i_{\text{b}}$ and $i_{\text{c}}$ to grid side. The controller $H_{\text{i}}$ is used to generate the voltage reference for the gate driver circuit.

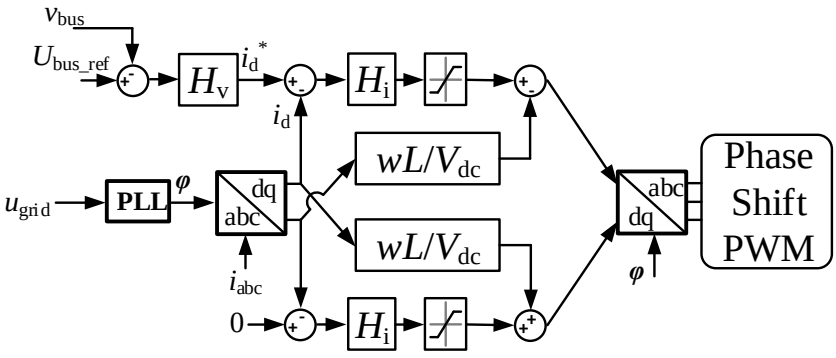



Fig. 4-11 The Control Algorithm of the Grid-side Converter

The phase angle is sensed from grid voltage and the control structure of phase-locked loop (PLL) is shown in Fig. 4-12. The grid voltages are transformed to *αβ* frame and *dq* frame , then through a PI control, ccompared with the reference electric speed which is $2\pi f_{grid}$. The integration of the PI output is the electric speed.

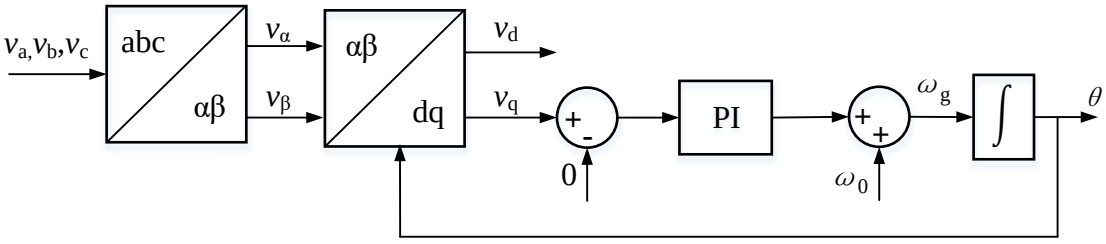



Fig. 4-12 Control Strategy of PLL

## 4.7 Case Study and Simulation Verification

### *4.7.1 Data center integrated with solar power and hybrid energy storage*

To simulate the overall system, the solar power input is simulated in different weather conditions. There are four typical weather conditions: cloudy day, rainy day, overcast day, and clear day. The load profile of a data center is built for Matlab/Simulink™ simulations. Solar irradiation simulations for four typical weather conditions are given in Fig. 4-13-Fig. 4-16 [4.17]. Considering the power fluctuation, the clear day is the lowest and the cloudy day is the highest.

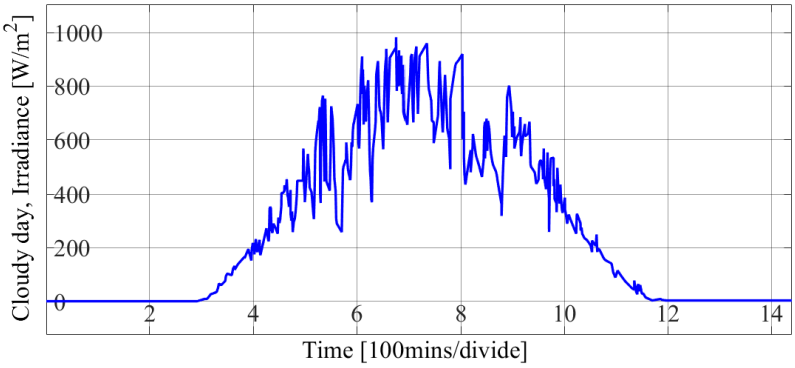



Fig. 4-13 Solar Irradiance on a Cloudy Day

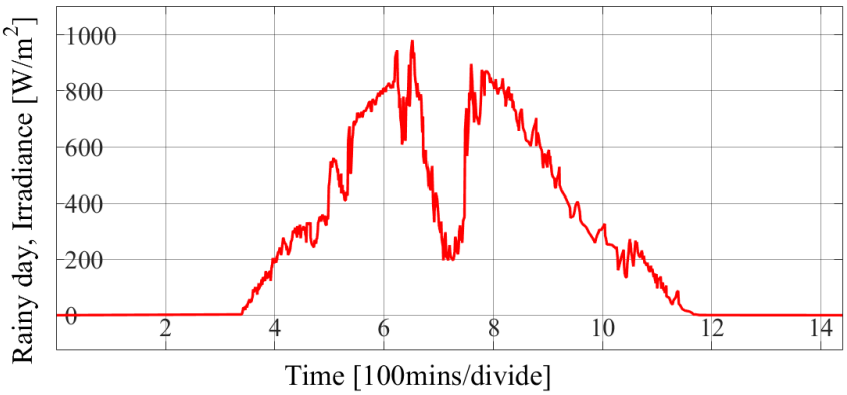



Fig. 4-14 Solar Irradiance on a Rainy Day

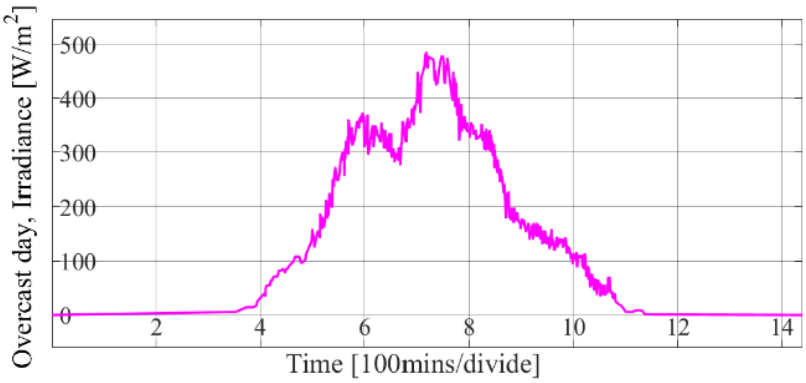



Fig. 4-15 Solar Irradiance on an Overcast Day

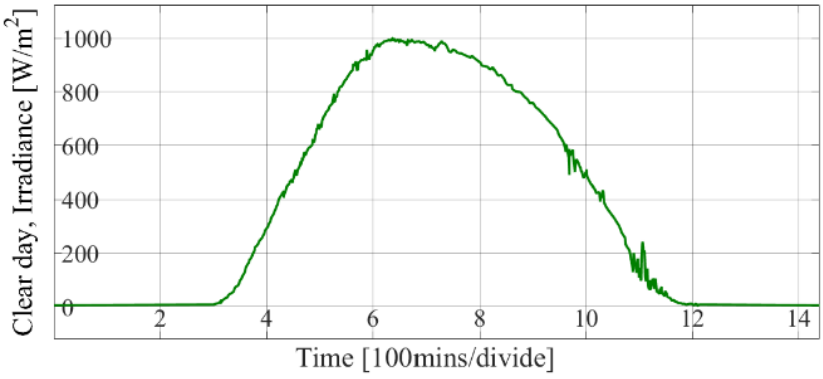



Fig. 4-16 Solar Irradiance on a Clear Day

The PV output power in a cloudy day always has the highest fluctuations, thus itis considered in the system level simulation. The load profile of a typical data center is shown in Fig. 4-17.

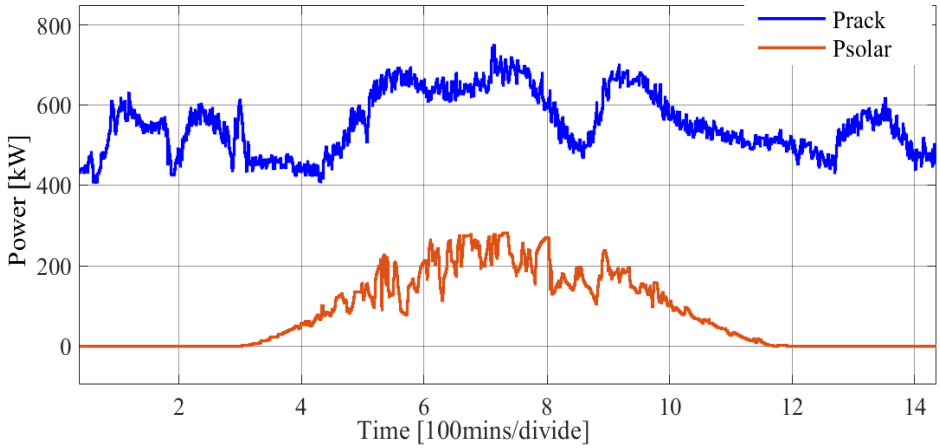



Fig. 4-17 Rack Power and PV Power on a Cloudy Day Over 24 Hours

The simulation results of the power flows from the ac grid and battery pack over 24 hours are given in Fig. 4-18 and Fig. 4-19. Fig. 4-18 is no ultracapacitor mode and shows all the high- and medium-frequency power are absorbed by the battery. Fig. 4-19 shows the power from grid and batteries in ultracapacitor pack connected mode.

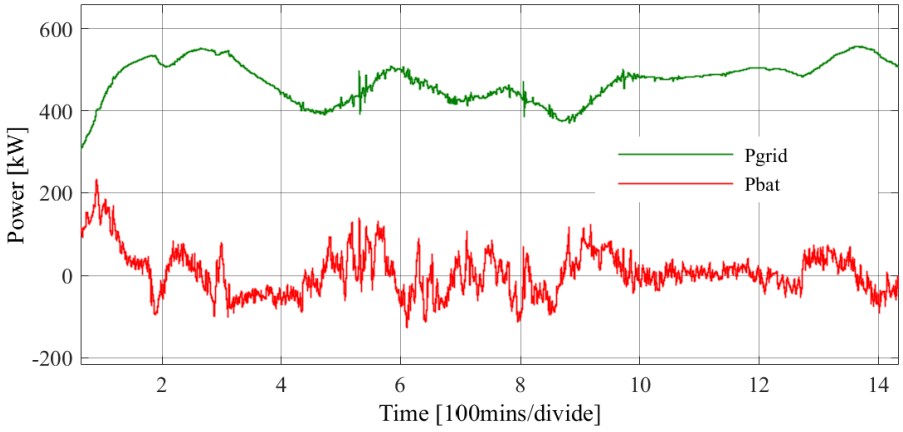



Fig. 4-18 Power Flows of the Grid and Battery without Ultracapacitor Pack

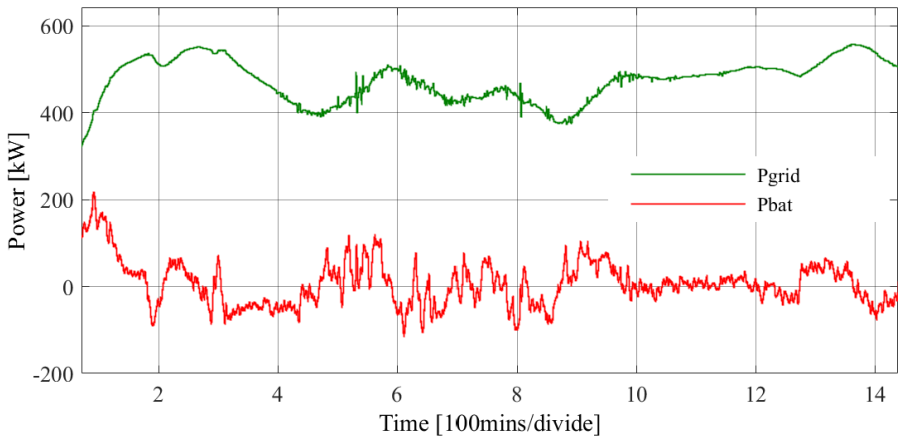



Fig. 4-19 Power Flows of the Grid and Battery with Ultracapacitor Pack

The simulation results of the 400 V dc bus stability and ultracapacitor power are illustrated in Fig. 4-20, which is used to verify the effective of controller for ultracapactiors and batteries. It shows that all the high- and medium- frequency powers can be smoothed by the battery pack without the ultracapacitor. However, this leads to the frequent charge and discharge operations in the battery pack which can reduce the lifetime of the battery. The voltage spike with a high-frequency component in the dc bus is increased to 22 V. This will easily activate the low or over voltage protection operations, and reduce the system reliability. As shown in Fig. 4-21, the high- and medium-frequency power transients absorbed by the ultracapacitor and battery packs with the application of the ultracapacitor on the 400 V dc bus. The 400 V dc bus is stabilized with a maximum voltage transient of 12 V which is only 3% of the 400 V reference dc voltage.

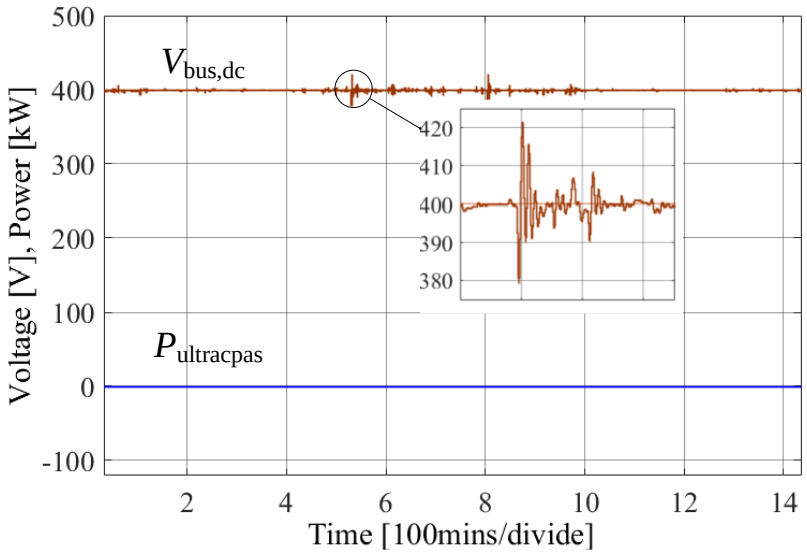



Fig. 4-20 The 400-V DC Bus Voltage without Ultracapacitor Compensation

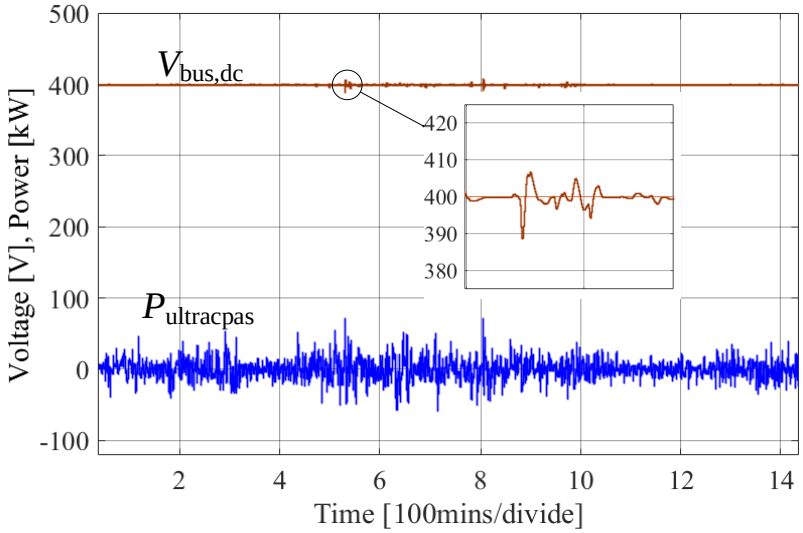



Fig. 4-21 The 400-V DC Bus Voltage and Ultracapacitor Powers with Ultracapacitor Compensation

### *4.7.2 Different percentages of solar power in data center*

The simulation of different percentages of distributed solar power in data centers are performed to analyze the system dynamic response. Three power levels of data center are simulated in

Matlab/Simulink™: 0.5 MW, 1.5 MW, and 3 MW. The maximum voltage ripple on the dc bus is monitored during the solar fluctuation period. The data are collected and shown in the tables.

Table 4.2 DC Bus Ripple of 0.5 MW Data Center with Variable Solar Power

| | Solar power [MW] | Maximum voltage ripple on 400 V dc bus [V] |
|---|---|---|
| Data center power rating 0.5 MW | 0.069 | 3 |
| | 0.138 | 5.8 |
| | 0.206 | 8.65 |
| | 0.276 | 11.5 |
| | 0.345 | 14.3 |
| | 0.415 | 17.1 |
| | 0.49 | 20 |

Table 4.3 DC Bus Ripple of 1.5 MW Data Center with Variable Solar Power

| | Solar power [MW] | Maximum voltage ripple on 400 V dc bus [V] |
|---|---|---|
| Data center power rating 1.5 MW | 0.275 | 6.8 |
| | 0.345 | 8.4 |
| | 0.415 | 9.8 |
| | 0.485 | 11 |
| | 0.555 | 12.5 |
| | 0.708 | 15.5 |
| | 0.85 | 18 |

Table 4.4 DC Bus Ripple of 3 MW Data Center with Variable Solar Power

| | Solar power [MW] | Maximum voltage ripple on 400 V dc bus [V] |
|---|---|---|
| Data center power rating 3 MW | 0.55 | 6 |
| | 0.76 | 8.1 |
| | 0.98 | 10.1 |
| | 1.285 | 12 |
| | 1.47 | 14.2 |
| | 1.61 | 15 |
| | 1.835 | 18 |

Considering 3% voltage ripple, in 0.5 MW data center, 0.25 MW of solar power (50% of data center power) is acceptable for dc bus stability. In the 1.5 MW and 3 MW data center, the acceptable solar power flows are about 35% and 42% of data center power rating, respectively. The tradeoff is the cost of the dc bus capacitor and battery. Better dc bus voltage transient performance could be achieved with the more energy storage devices.

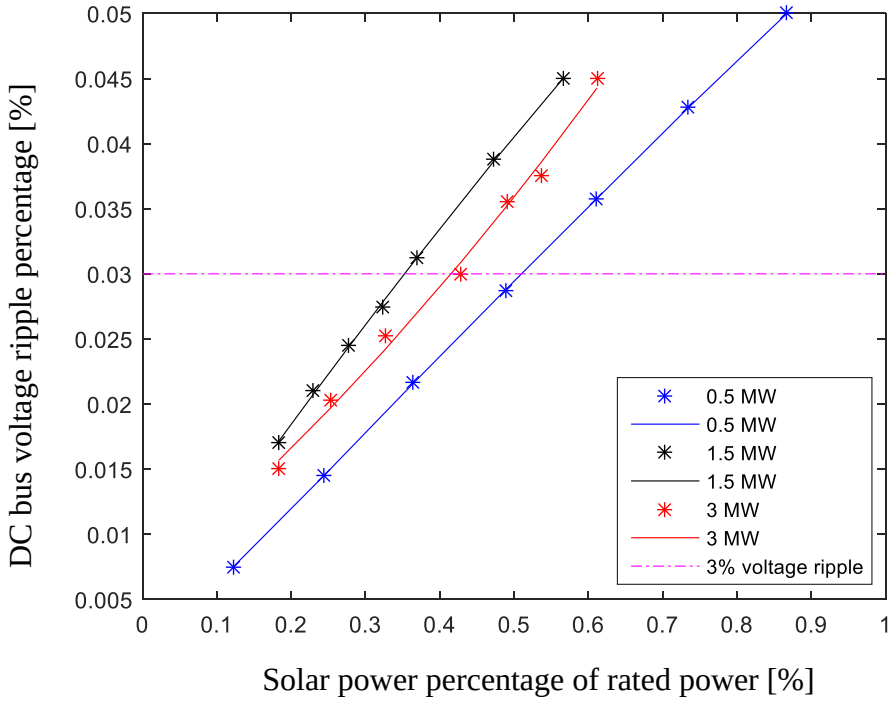



Fig. 4-22 DC Bus Voltage Performance of 0.5 MW, 1.5 MW, and 3 MW Data Center with Solar Power

## 4.8 Conclusion

The integration of solar power, batteries and ultracapacitors for a 400 V DC-powered data center is investigated in this chapter. Four typical weather conditions are simulated for solar power generation. The availability of ultracapacitors which have very high power densities and charge/discharge cycling capability characteristics are investigated to smooth the output power intermittencies from solar panels. Battery and ultracapacitor packs are used to compensate the medium- and high-frequency power transients, respectively. This combination should maintain the desired lifetime of the battery pack, while reducing any transients affecting at the ac grid side. It can improve the dc bus stability with the PV power and/or load transients. Simulation results verified that the designed 400 V DC-powered data center system and its optimized control strategy

performed as predicted. The stability performance of data center with different solar power flows were also investigated.

## 4.9 Reference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# CHAPTER 5

# SYSTEM LEVEL STABILITY ANALYSIS FOR 400 V DATA CENTER

## 5.1 Stability Issue in a Data Center

As mentioned previously, the cost of power supply downtime in data center is very high. Reliability is the top priority in data center application. In the power distribution of a data center, since there are many dc/dc converters connected dc bus to a load, it is important to control converters to cooperate with each other to increase the system stability. A model with circuit parameters, number of dc/dc converters and server loads will be investigated to characterize the dynamic and steady-state behaviors of the power supply system in a data center. The theory behind the unstable DC-powered system is that there is a negative input impedance of the power supplies. In other words, if the converter's loop has the right-half-plane poles, the converter will be unstable. The system poles are determined by circuit parameters, controller parameters and load dynamic changes.

## 5.2 Mathematical Model: Large Signal Modeling of Large-Scale Data Center

To analyze the necessary stable condition, a large signal model of a 400 V DC-powered data center is built as shown in Fig. 5-1 [5.1]. The power converters for the grid, battery, and ultracapacitor are simplified as voltage source converters. $v_{dc1}$ is the output voltage from the power converter of grid side and paralleled with a capacitor $C_{s1}$. Similarly, $v_{dc2}$ presents the output voltage of PV converter. $v_{dc3}$ and $v_{dc4}$ are the voltage of battery and ultracapacitor, respectively. The power demand from the different racks are modelled as current sources. The input voltage to the racks is

$v_i$, $i$=1, 2… $n$. The bus bar for the connection of each power source is relatively short, thus the impedance is neglected. However, the bus bar for the high power racks are long and large which is modeled as series RL branch presents.

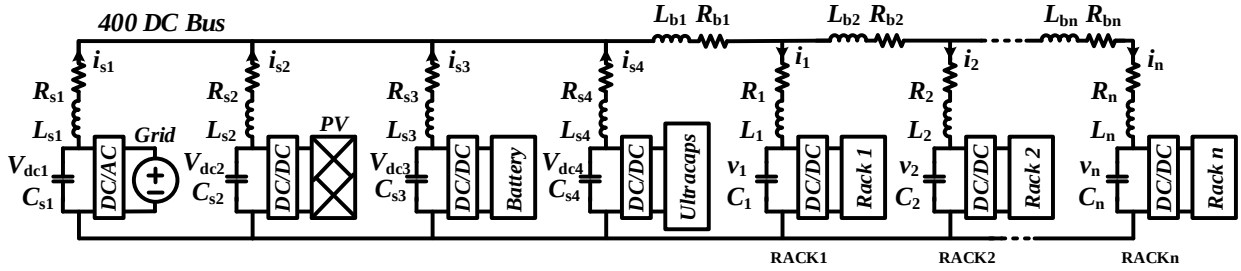



Fig. 5-1 Large Signal Model of 400 V DC-Powered Data Center

By utilizing KCL and KVL, the differential equations that describe the dynamics of the 400 V DC-powered data center are shown in Eqs. (5-1) to (5-5).

$$-V_{dci}+R_{si}i_{si}+L_{si}\,di_{si}/dt+(-R_{s(i+1)}i_{s(i+1)}-L_{s(i+1)}\,di_{s(i+1)}/dt+V_{dc(i+1)})=0, i=1,2,3. \tag{5-1}$$

$$-V_{dc3}+R_{s3}i_3+L_{s3}\,di_3/dt+\left(R_{b1}\sum_{k=1}^{n}i_k+L_{b1}\sum_{k=1}^{n}di_k/dt\right)+(R_1i_1+L_1\,di_1/dt+v_1)=0 \tag{5-2}$$

$$-v_i-R_ii_i-L_i\,di_i/dt+\left(R_{b(i+1)}\sum_{k=i+1}^{n}i_k+L_{b(i+1)}\sum_{k=(i+1)}^{n}di_k/dt\right)+(R_{i+1}i_{i+1}+L_{i+1}\,di_{i+1}/dt+v_{i+1})=0, i=1,2,\cdots,n-1. \tag{5-3}$$

$$C_i\,dv_i/dt+P_i/v_i-i_i=0, i=1,2,\cdots,n. \tag{5-4}$$

$$C_{si}\,dv_{si}/dt+P_{si}/v_{si}-i_{si}=0, i=1,2,\cdots,n. \tag{5-5}$$

To investigate the stability of overall system, linearize the Eqs. (5-1) to (5-5) and eigenvalues of the system are calculated in MATLAB™. The criterion of stability is introduced before analyzing the stability in the next section.

## 5.3 Stability Criterion Introduction

The system transfer function poles or the eigenvalues of system matrix defines the stability of the system [5.2]-[5.6]. Different locations of the eigenvalues leads to different homogeneous responses. Usually, there are six locations of eigenvalues.

Case (a): A complex conjugate pair in the left-half plane. The response component is $Ce^{-at}\sin(\omega t+\psi)$, $a>0$. It is a decaying sinusoid signal and the decay speed is decided by $a$.

Case (b): When the response component is $Ce^{at}\sin(\omega t+\psi)$, $a>0$. It results the exponentially increasing signal, thus the system is unstable. In this case, the poles locate the right-half plane.

Case (c): The eigenvalue locates on the left side real axis. The response component is $-C$ and the system is stable.

Case (d): Opposite of case (c), the response component is $C$ which is in the right side real axis and leads to unstable system.

Case (e): The eigenvalues located on the imaginary axis and the response component is $\pm j\omega$. The system can be represented as a sinusoid signal with constant amplitude.

Case (f): The eigenvalues locate at the origin is with a constant amplitude component.

The specification of the system pole location on the pole-zero plot is illustrated in Fig. 5-2 [5.6]. A stable system is that all the eigenvalues should be on the left-half plane.

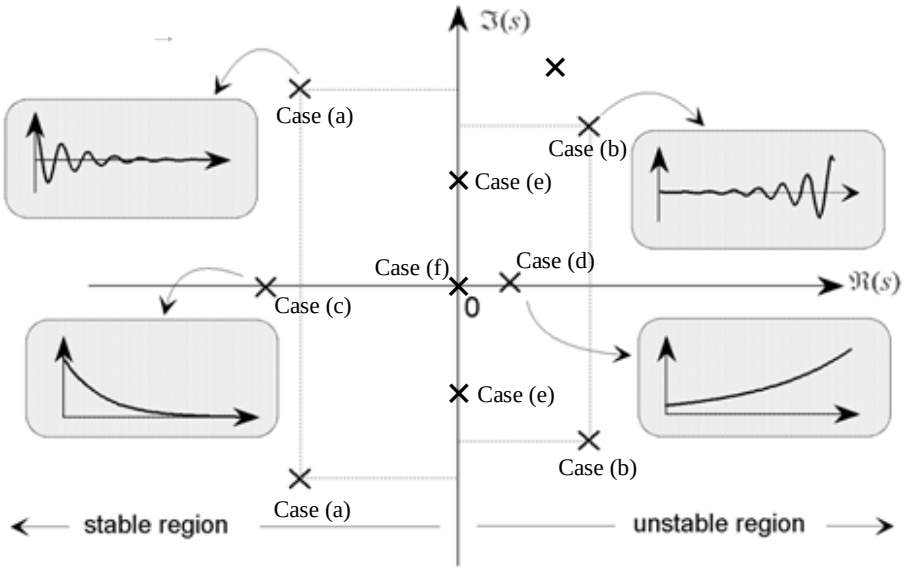



Fig. 5-2 The Specification of Pole Location [5.6]

For example, a pole on the right-half plane is corresponding to an exponentially increasing in voltage/current, this results in the system becoming unstable. Even from a small disturbance, it will lead to large current spike in capacitor ($C*dv/dt$) or large voltage spike in the inductor ($L*di/dt$), then the system will be unstable. The simulation results of eigenvalue and the related voltage response is shown in Fig. 5-3. When eigenvalues are very closed to the right-half plane, the dc bus voltage is not stable during the step-down load transient.

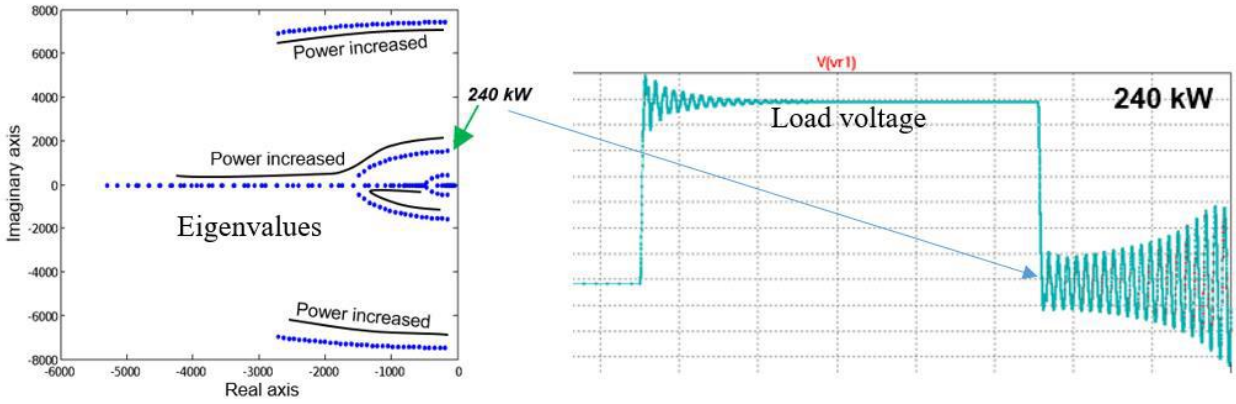



Fig. 5-3 System Stability: Eigenvalue and Voltage Response

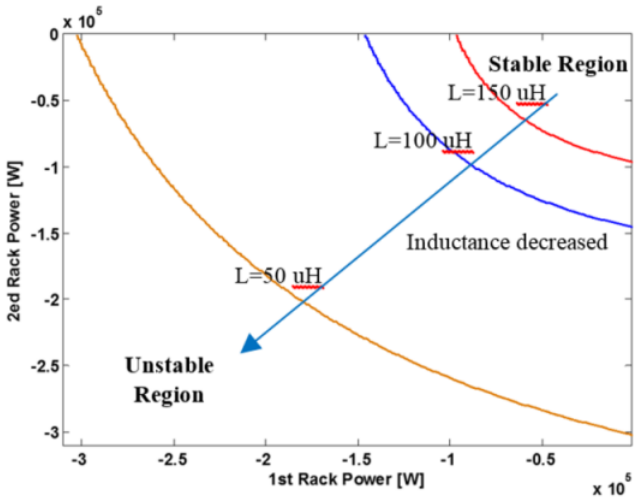
## 5.4 Simulation Results and Stability Analysis

To evaluate the sensitivity of the cable impedance and the dc bus capacitance in the controller, a simulation is performed in MATLAB/Simulink$^{TM}$. To simplify the simulation, two racks are considered as server loads. The simulation parameters are given in the Table 5.1. The bus impedance is estimated by the cable length and resistance/inductance per unit length.

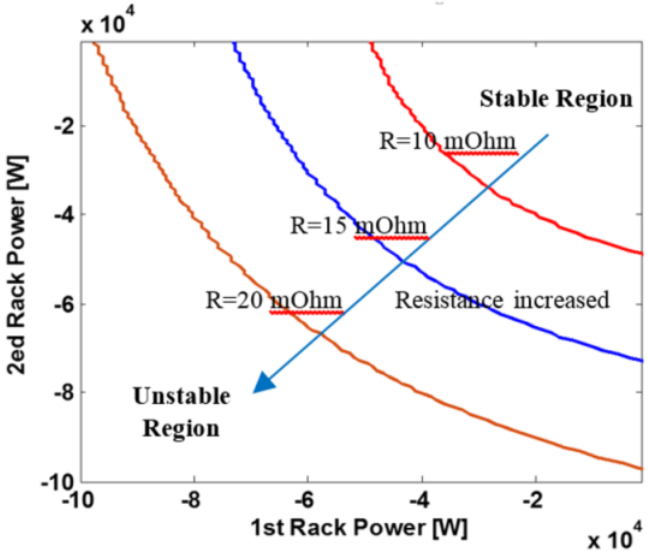
Table 5.1 Simulation Parameters

| Name | Variable | Value |
|---|---|---|
| dc bus voltage | $V_{dci}$, $i$=1,2,3,4<br>$v_1$,$v_2$ | 400 V |
| Power source impedance | Resistance $R_{si}$, $i$=1,2,3,4 | 2.5 mΩ |
| | Inductance $L_{si}$, $i$=1,2,3,4 | 80 μF |
| Distribution bus impedance | Resistance $R_{bi}$, $i$=1,2 | 15 mΩ |
| | Inductance $L_{bi}$, $i$=1,2 | 100 μF |
| dc bus to rack cable impedance | Resistance $R_i$, $i$=1,2 | 10 mΩ |
| | Inductance $L_i$, $i$=1,2 | 60 μF |
| Rack power rating | $P_i$, $i$=1,2 | 300 kW |

Fig. 5-4 (a) and (b) shows that the system will change from the stable region to the unstable region with the increased power requirement of rack power. The color curve is the boundary between stable region and unstable region. If the cable inductance decreases or cable resistance increases, the area of stable region will become larger. The tradeoff is the higher resistance in the cable, the more power loss in the distribution bus. Fig. 5-5 depicts that the higher dc bus capacitance, the larger stable region. If dc bus capacitance decreases too much, the system will be unstable which is shown in Fig. 5-5.




(a) DC Bus Cable Inductance Increasing: 50 μH (Orange), 100 μH (Blue), 150 μH (Red)




(b) DC Bus Cable Resistance Increasing: 10 mΩ (Orange), 15 mΩ (Blue), 20 mΩ (Red)

Fig. 5-4 Stable Boundary of Different dc Bus Cable Impedance

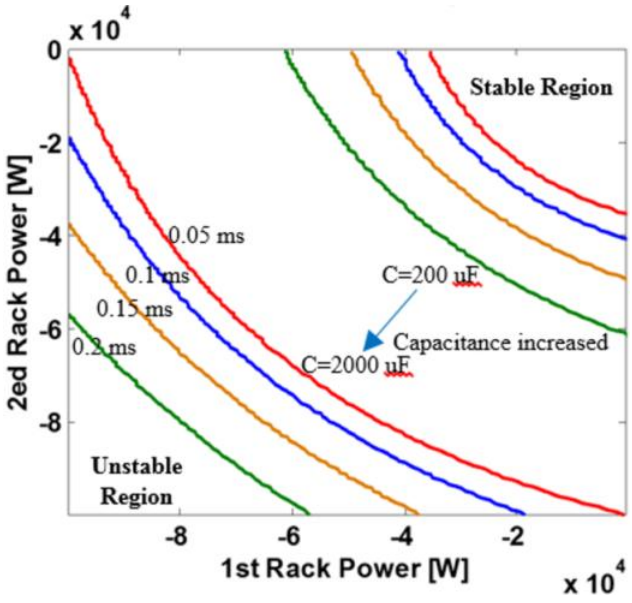



Fig. 5-5 Stable Boundary of DC Bus Capacitor. 200μF: 0.2 ms (Green), 0.15 ms (Orange), 0.1 ms (Blue), 0.05 ms (Red). 2000μF: 0.2 ms (Green), 0.15 ms (Orange), 0.1 ms (Blue), 0.05 ms (Red)

## 5.5 Conclusion

In this chapter, the system level stability analysis for a 400 V data center is presented. The large signal model of the proposed system level configuration is developed. The differential equations that describe the dynamics of data center with solar power, battery, and ultracapacitor. To analyze the system stability, the stability criterion is introduced firstly. In order to analyze the sensitivity of the circuit parameters, such as the cable inductance, resistance, dc bus capacitance, the converter controller time constant, the simulation results are given to demonstrate the stable region of the data center.

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# CHAPTER 6

# CONCLUSION FUTURE WORK

## 6.1 Conclusion

The key contributions of this dissertation are summarized as below:

(a) The limits of the power density and efficiency for the dc/dc converters as part of the power supplies in data centers are investigated. A 400 V DC-powered data center is proposed in order to reduce power loss and cable cost from the distribution. 48 V dc bus is kept in the rack in order to minimize the revision from the existing power supply in data center.

(b) Cascaded totem-pole bridgeless PFC converters is proposed as a power interface converter grid ac voltage to the 400 V dc voltage. It can have better efficiency performance and minimize the number of switching devices needed.

(c) Model predictive control is developed for the cascaded totem-pole bridgeless PFC converter to realize a better transient performance and higher power efficiency.

(d) A more accurate loss model of dual-active bridge converter is proposed. The proposed method has better efficiency performance (1~1.5% improvement) compared with the previous research work.

(e) K-factor control with a small signal model of the dual-active bridge is proposed and results in improved transient performance. A control strategy using a virtual capacitor based K-factor control is proposed to reduce the dc bus capacitance and maintain good transient performance.

(f) Solar power is integrated in the 400 V dc bus to reduce the electricity consumption from the grid side. Battery and ultracapacitor packs are used together to maintain the expected lifetime of battery and dynamic performance of the system.

(g) Built a large signal model to analyze the necessary stable conditions: maximum output power, cable parameters, and minimum dc bus capacitance.

(h) A scaled down prototype of the proposed topology is built and tested. The simulation and experimental results are presented to validate the proposed topology and control algorithms.

## 6.2 Future work

(a) Test the topology with higher ac voltage (> 480 VAC). If the phase voltage is unbalanced, control of the ac/dc converter will be an interesting topic.

(b) The model predictive control also can be utilized for the overall system. The challenge is how to build the discrete model for the overall system.